Flux compensation for interleaved parallel-connected multilevel converters using cross-coupled inductors

by

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Abstract

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To meet the continuously growing energy demand for both industrial and civilian use, parallel-connected voltage source converters (VSCs) using interleaved switching techniques have become increasingly popular over the single module VSC for a variety of applications: electric vehicles, aerospace, and renewable energy systems. With poorly designed switching patterns, the inductors required to connect paralleled converters together can have a size and weight higher than they need to be. The switching patterns used in parallel modules can also produce low-quality pulse-width-modulated (PWM) voltage outputs, which adversely affect the system output currents and result in higher than necessary power losses in the output filter inductors and machine loads.

Pulse-width-modulated (PWM) switching patterns are presented for parallel-connected VSCs that are used to reduce the size and weight of the converter output inductors. These inductors are magnetically coupled to reduce the flux in their magnetic cores, resulting in a much smaller size and weight. The winding connections of these cores are magnetically cross-coupled. This results in a large inductance between the converter outputs, reducing

circulating currents that increase the converter power losses. Conversely, the cross-coupled windings also result in a very low series out impedance, hence lowering fundamental voltage drops and increasing the voltage reaching the load. Switching patterns, using interleaved carriers and either: (a) carrier swapping techniques; or (b) reference signal modification, are used to lower the output voltage harmonics, hence improve the quality of the output multi-level line voltages in 3-phase systems.

For the switching patterns described, the flux in the coupled inductor cores can experience rapid jumps that increase the peak flux experienced in the cores. The most significant contribution of this thesis is the modified switching patterns presented that suppress these flux jumps, referred to as flux jump compensation techniques. Controlled predictable flux patterns allow the core cross-sectional area to be significantly reduced with the core size and weight.

In addition to modified PWM control using continuous switching, discontinuous switching patterns are presented (DPWM), which can be used to reduce the converter average switching frequency and significantly reducing the converter switching losses. The inverter switching patterns in DPWM are held high or low for two 60^{o} periods in a fundamental cycle. The transitions from no switching to continuous switching cause flux jumps in the cores. The reference signals are modified to provide flux jump compensation for these transitions as well as for carrier swapping. The modified DPWM control lowers the peak flux in the CI core, hence reduces the core size and weight.

The effectiveness of the various proposed PWM methods described are verified using both simulations and experimental results for a 3-phase parallel-connected coupled inductor converter prototype.

Preface

This research was carried out under the supervision of Dr. John Salmon from the Department of Electrical and Computer Engineering at the University of Alberta. Parts of this thesis have been published or will be submitted to IEEE conference or journal publications:

Journals

1) **Chenhui Zhang**, Marius Takongmo, John Salmon, "Flux Compensation for Parallel-Inverter Legs using Carrier-based Interleaved PWM", submitted to *IEEE Trans. on Power Electronics*, 8 pages, July 2021.
2) Marius Takongmo, **Chenhui Zhang**, John Salmon, "Coupled Inductor Design for High-Speed and Ultra-High-Speed Electric Drives" to be submitted to *IEEE Trans. on Power Electronics*, prepared 9 pages, July 2021
3) Takongmo**, Chenhui Zhang**, John Salmon, "Parallel connected inverters using a dc choke and a 3 limb coupled inductor", to be submitted to *IEEE Trans. on Power Electronics*, prepared 9 pages, July 2021.

Letters

1) **Chenhui Zhang,** Marius Takongmo, John Salmon, "High-Quality PWM Scheme for High-Speed Electric Drives", *IEEE Letters on Power Electronics*, 4 pages, July 2021.

Conferences

1) **C. Zhang,** M. Takongmo and J. Salmon, "Enhanced Interleaved Pulse Width Modulation Scheme for Parallel Connected Voltage Source Converters", *IEEE Energy Conversion Congress and Exposition.* 8 pages, October 2021.
2) M. Takongmo, **C. Zhang,** J. Salmon,"Parallel Inverters using a DC Common Mode PWM Filter with an AC Differential Mode PWM Filter," *IEEE Appl. Power Elect. Conf.* (APEC 2021), 8 pages, June 2021.

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Chenhui Zhang, July 2021

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Abbreviations

APOD	Alternate Phase Opposition Disposition
CB-DPWM	Carrier-Based DPWM
CI	Coupled Inductor
CII	Coupled Inductor Inverter
CI_{SL}	Coupled Inductor With Coupled Windings on Separate Limbs
CI_{CCW}	Coupled Inductor With Coupled Windings on Separate Limbs
CPWM	Continuous PWM
DPWM	Discontinuous Pulse Width Modulation
DSP	Digital Signal Processor
FPGA	Field-programmable Gate Array
ILPP	Inverter Leg Per Phase
NPC	Neutral Point Clamped Converter
LS-PWM	Level-Shifted PWM
3L-NPC VSC	Three-level Neutral Point Clamped VSC
3L-FLC VSC	Three-Level Flying Capacitor Voltage Source Converter
2L-VSC	Two-level voltage source converter
THD_f	Total Harmonic Distortion (Fundamental)
PS-PWM	Phase-shifted Pulse Width Modulation
PWM	Pulse Width Modulation
PD-PWM	Phase Disposition PWM
POD-PWM	Phase Opposition Disposition
APOD-PWM	Alternate Phase Opposition Disposition
SHE	Selective Harmonic Elimination

SVC	Space Vector Control
SVM	Space Vector Modulation
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

Chapter 1 Introduction

In recent years, the demand for more highly efficient high-power converters has been increasing in a wide range of industrial applications [1], [2]-[5]. Novel power electronic converter designs have been one way of meeting this demand. Parallel-connected voltage source converters (VSCs) using interleaved PWM switching is an example of how to increase a converter power rating without changing the system voltage rating [6]-[13]. The output terminals of parallel-connected converters, or inverter legs in dc to ac systems, are usually connected using inductors. These inductors are normally designed to: (a) have a high impedance to suppress circulating currents between the parallel converters, (b) reduce the output high-frequency harmonics with the help of interleaved pulse-width-modulation (PWM) techniques. Their dual function of limiting circulating currents while filtering the output harmonics, requires careful design to: (a) avoid a significant drop in the converter output voltage, and (b) increasing the size and weight of the converter by the use of these inductors [6]-[7], [15]-[18]. Coupled inductor techniques can combine the useful characteristics of: (a) a high impedance between the inverter output terminals, (b) a low series output impedance. These two basic characteristics can be achieved using coupled inductors while lowering the weight and size of the magnetics. Applications where such converter designs are useful, include most mobile applications, electric vehicles, motor drives, industrial machines, and aerospace [16]-[17]. Special PWM switching strategies are required when paralleled converters are connected using inductors. Traditional sinusoidal Phase-shifted PWM (PS-PWM) is often used in converters using ripple current cancellation to improve output power quality. In this situation, separate inductors are normally used in each converter output, and the combined requirements of the inductor design to limit circulating currents while minimizing the output voltage droop are often conflicting. The coupled inductor designs considered producing multi-level output voltages rather than using ripple current cancellation. PS-PWM, essentially using multiple interleaved carriers to generate switching patterns, does not necessarily generate the highest quality output line voltage in 3-phase systems. The non-ideal output voltage quality increases the load current THD (Total Harmonic Distortion). Thus, it is highly desirable to improve the PWM switching

control of parallel-connected converters to not only improve the quality of the output 3-phase line voltages but also to lower the size and weight of the coupled inductor designs being used.

1.1. Voltage source converter classification

Different types of multilevel voltage source converters have been widely used in medium voltage applications [1], [2], [19], see Fig. 1.1 The basic 2-level voltage source converter (2L-VSC) is normally used in low/medium applications as the voltage, and current ratings of power semiconductors are large enough without resorting to complicated power converter structures. A single functional switch can consist of several power semiconductor switches connected in series to obtain a higher voltage rating in the 2L-VSC circuit. However, connecting extra components in series is difficult to maintain equal voltage stress across each semiconductor. It is more useful to add extra modules, or multiple power converters, to better equalize the current and voltage stress between the modules. Consequently, separate modules can then use different switching patterns to improve the quality of the PWM output voltages and currents [20]. Therefore, different topologies have been developed over the years that use extra components to generate higher quality output voltages, such as three-level Neutral Point Clamped VSC (3L-NPC VSC), three-level flying capacitor VSC (3L-FLC VSC), Cascaded H-bridge VSC, and parallel-connected 2L-VSC, etc, see Fig. 1.1.

The multilevel VSC system can generally increase the rated power with two different approaches: (a) stacking converters in series to increase the system voltage level or (b) connecting converters in parallel to increase the system current level. The former is usually achieved using series-connected converters that use floating capacitors as the voltage source, while the latter uses parallel-connected converters connected together using inductors. In this thesis, a parallel-connected multilevel VSC with n inverter legs in each phase is used to generate high-quality multilevel PWM output voltages, where *n* is the number of inverter legs per phase (ILPP).

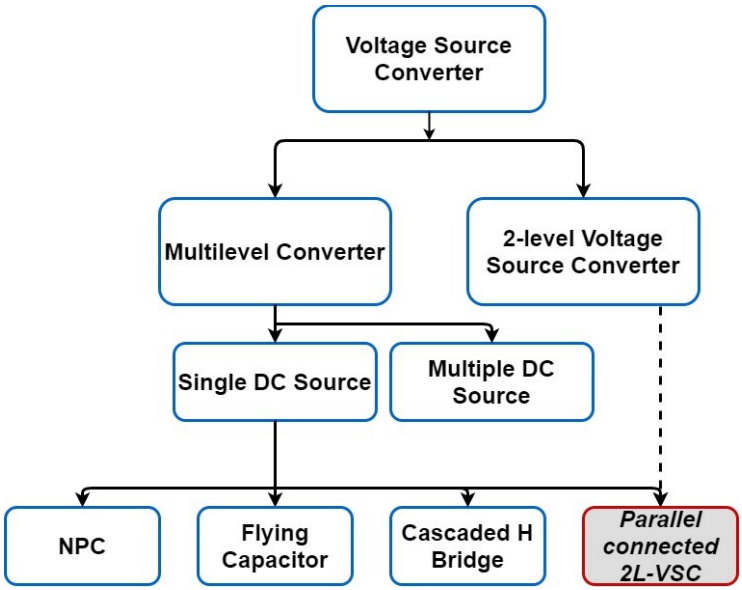


Figure. 1.1. Voltage Source Converter classification.

The conventional three-phase 2L-VSC consists of three inverter legs, each leg with two switches corresponding to one phase, see Fig. 1.2. In this circuit, only one switching function is needed for the switches in each leg because of their complementary switching. The number of switching states can be calculated by the number of phases (Ph) and switch number in each leg (phase) (1.1). Each phase of this circuit can generate 2 level phase voltages; hence 3 level line PWM output voltage can be obtained.

$$\boldsymbol{Number\ of\ switching\ states = n^{Ph} = 2^3 = 8} \tag{1.1}$$

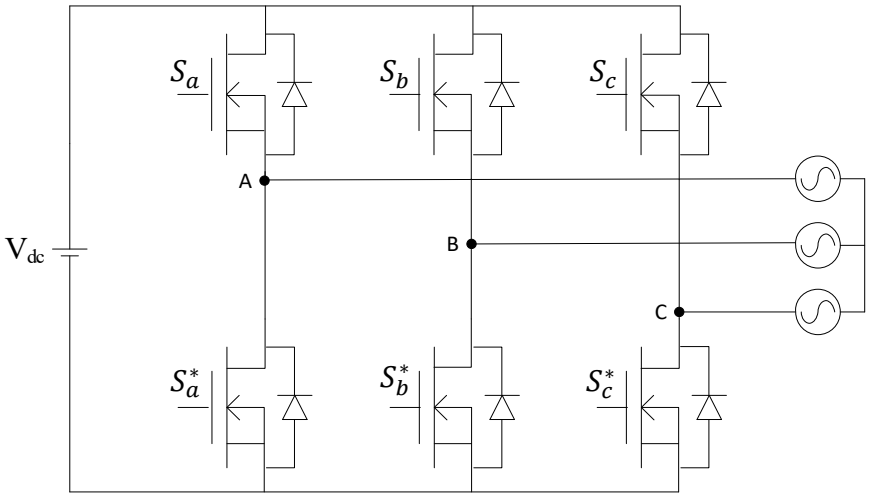


Figure. 1.2. The 2-level Voltage source converter circuit diagram.

To increase the current handling capability hence increasing the rated power, 2L-VSCs are often connected in parallel, as mentioned. Compared with a single 2L-VSC, multiple parallel-connected converters can have a better performance in terms of higher power ratings, reduced output harmonics, and higher power conversion efficiency [21].

1.2. Inductors in paralleled VSC

Voltage source converters using parallel connected inverter legs or modules are widely used to increase the output current, hence increase the output power without changing the system voltage rating. [7], [16]-[17], [21]-[26]. As a result, paralleled converters can better share the system currents, reduce the current ratings of individual devices and reduce conduction losses. Interleaved switching of parallel converters results in the phase-shift of certain high-frequency harmonics, which cancels at the load. 3-phase ac systems are considered in this study, so parallel-connected systems are considered in relation to having parallel-connected inverter legs in each phase. Interleaved switching of parallel-connected inverter legs in each phase can produce high-frequency circulating currents between the inverter legs [22], [27]-[29]. These currents increase the power losses in the switches and diodes; therefore, it is common to suppress these circulating currents to lower the losses and improve power conversion efficiency. Inductors are inserted in the circulating current paths to limit these currents. Coupled inductors can introduce a large inductance in series with the inverter leg outputs to reduce the circulating currents but also has the characteristic of a low series inductance in each phase output [16]-[17], [22], [24], [28], [30]-[31].

Separate inductors can be placed at the output of each inverter leg to act as a standard filter inductor, see Fig. 1.3. However, the same inductors filter the output current and the circulating currents, leading to a design conflict choosing their size. In addition, the load output fundamental current flowing through these inductor windings, generates a significant fundamental flux in the core. This increases the core size due to the higher peak core flux, see Fig. 1.4, than would occur if the circulating currents only produced the core flux. As a design, the use of separate inductors can be said to be larger than required for controlling circulating currents. If high frequency circulating currents only

produced flux in the cores, as is the case for coupled inductors, then the inductance value can be increased to reduce the circulating currents better while using a physically much smaller inductor size. Alternatively, if separate inductors are sized to control the circulating currents, their inductance is also in series with the output current. This can result in a much lower transient response time [22] and large fundamental voltage drops that reduce the effective output voltage of the system. This voltage drop can be a serious issue for applications that use a high fundamental frequency. To compensate for this voltage drop, a higher dc-link voltage is required, which will increase the applications' implementation difficulty. Especially for the mobile applications, where the battery voltage range is usually limited within the 200V-450V range [32]-[34]. In consequence, an inductor structure to avoid fundamental flux created by the fundamental current is highly desirable.

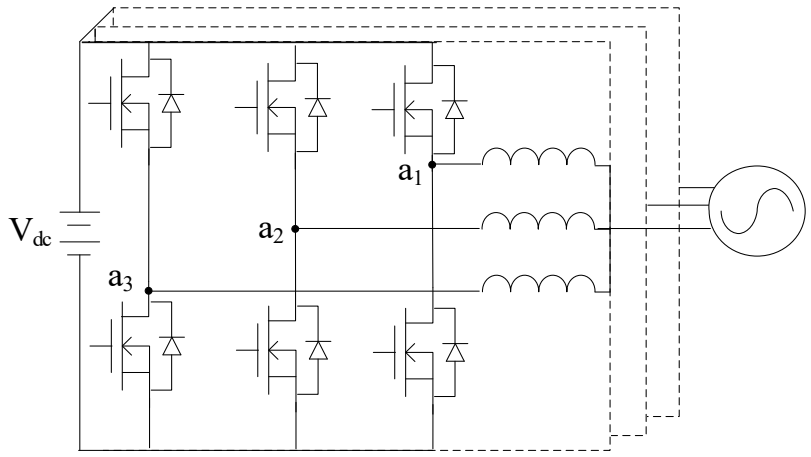


Figure. 1.3. The circuit diagram of the 3 paralleled ILPP VSC with uncoupled inductors.

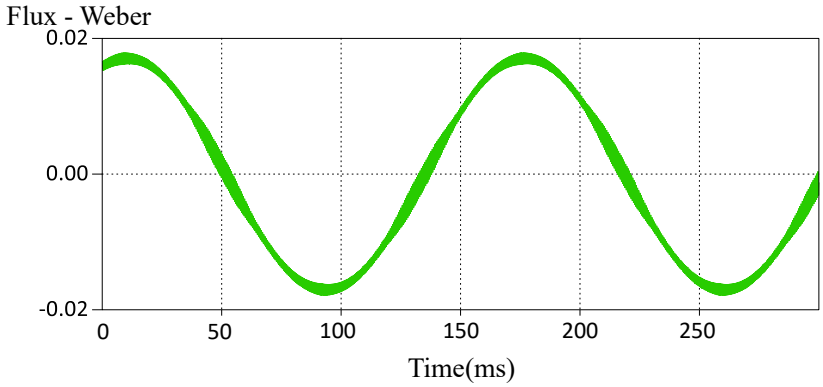


Fig. 1.4. Three-phase interleaved parallel VSC flux waveform with the separate inductor.

Coupled Inductors are widely used to suppress the flow of high frequency circulating currents between parallel-connected inverter legs while generating multilevel PWM output voltages [7], [16]-[17], [22], [28], [35]-[38]. The flux produced by the fundamental currents cancels in the CI core, which significantly reduces the required inductor size and weight. Two different coupled inductors configurations are widely used. Coupled windings can be located on separate core limbs (CI_{SL}) [22]-[23], see Fig. 1.5. The second one is presented in [16], [17], [40] as CI with cross-coupled windings (CI_{CCW}), see Fig. 1.6.

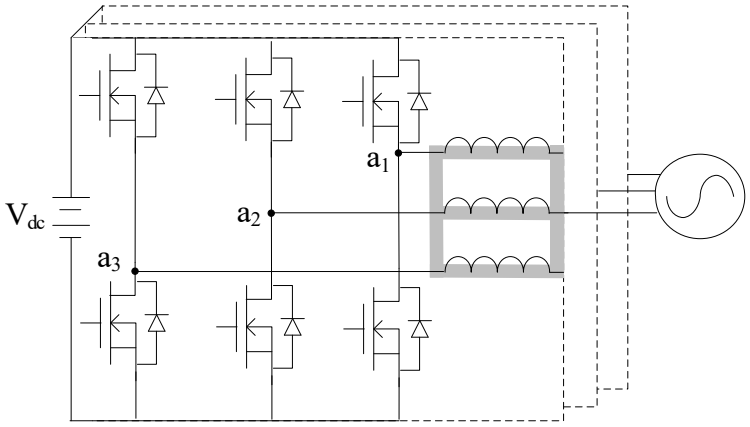


Figure. 1.5. Circuit diagram of CII with coupled windings on separate core limbs.

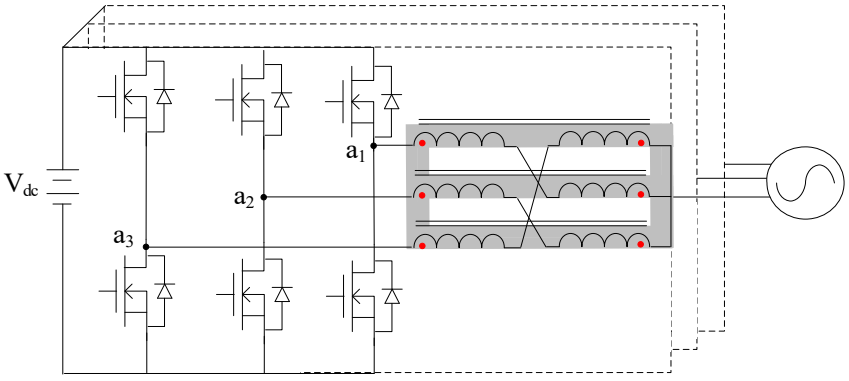


Figure. 1.6. Circuit diagram of CII with cross-coupled inductors.

The CI_{SL} can be used to suppress high-frequency circulating current. Balanced fundamental currents flowing to the output through parallel paths produce no significant flux in the core and encounter leakage inductance, otherwise referred to as inter-limb leakage inductance between coupled windings located on separate limbs. Unbalanced fundamental currents produce flux in the core flowing through separate limbs and can be

referred to as magnetizing or self-inductance. The ratio between this inductance relative to the inter-limb leakage inductance is the mechanism by which the fundamental currents are kept relatively balanced in the parallel paths from each inverter leg. This inductance is large and helps to suppress circulating currents. However, the inter-limb leakage inductance (between windings located on separate limbs) can still be considered large relative to windings located on the same limb (intra-limb leakage inductance: the inter-limb coupling coefficient is lower than the intra-limb coupling coefficient). Inter-limb leakage inductance can result in significant voltage drops in the fundamental output voltage, becoming more significant as the system operating frequency is increased. The fundamental part of the flux is eliminated; however, the flux is also affected by the fundamental voltage drop and behaves as the sinusoidal waveform, see Fig. 1.7.

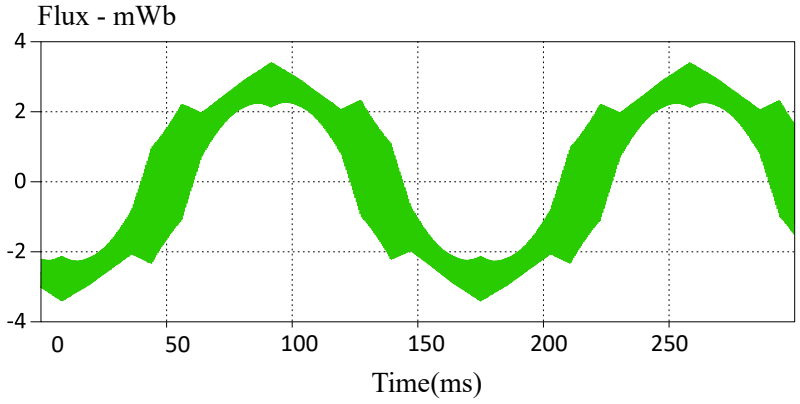


Fig. 1.7. Three-phase interleaved parallel CII flux waveform with CI_{SL}.

The CI considered in this thesis uses cross-coupled windings, where the term "*cross-coupled*" refers to two windings connected in series with one inverter leg and the phase outputs that are located on two separate limbs, hence cross-coupled windings and in short CI_{CCW}, see Fig. 1.5. The main benefit of using such a winding arrangement is that it presents a very low series inductance to the fundamental currents, but presents a high inductance to the unbalanced circulating currents. Compared with CI_{SL}, CI_{CCW} has its effective series inductance related to the intra-limb leakage inductance, which is much smaller than the inter-limb leakage inductance. Therefore, the fundamental voltage drops across the windings are very low, where the flux will not be affected by the voltage drop, see Fig. 1.8.

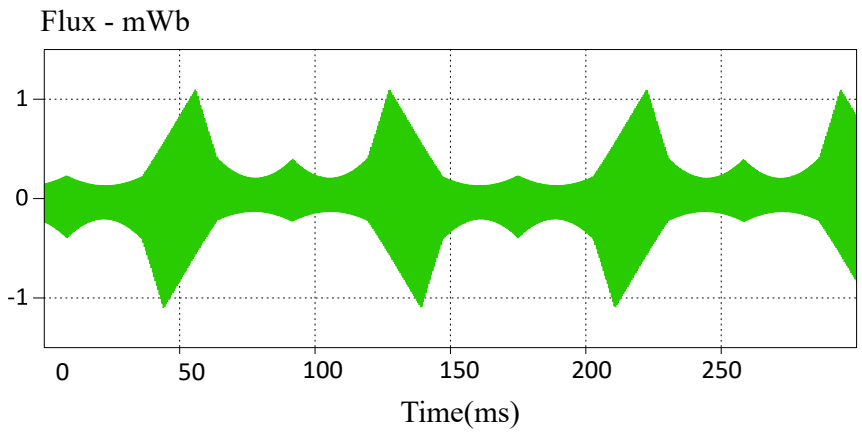


Fig. 1.8. Three-phase interleaved parallel CII flux waveform with CI_{CCW}.

In addition, by using CI_{CCW} in the interleaved three-phase paralleled VSC, the multi-level output voltage produced in each phase output n+1 levels phase, with $2n$+1 level in the line voltage (n is the number of ILPP). The PWM voltage steps are smaller than the dc-link voltage, and the line PWM frequency is $2n$ times greater than the carrier frequency. Although the output voltage has a higher PWM frequency, the frequency of the flux in the inductor cores remains at the switching frequency (f_{sw}). These characteristics can significantly reduce the size, weight, and material cost of output ac filters. The CIs used in this thesis for 3 ILPP VSC is given in Fig. 1.9.

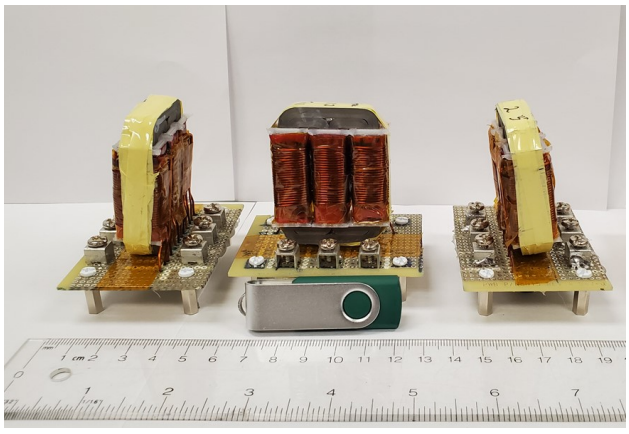


Fig. 1.9. Coupled inductor with cross-coupled windings (CI_{CCW}).

1.3. Multilevel Modulation techniques

Multi-level converter switching techniques have been extensively researched over the last decades [1], [2], [19], [39]. Different modulation methods have been developed based on different power requirements, switching/fundamental frequency, and different circuit topologies. A brief classification summary based on operating switching frequency for multilevel modulation schemes is given in Fig. 1.10. To generate multilevel PWM, multiple carriers are used. The use of multiple carriers means that several carriers are used and phase-shifted relative to one another to control the switching of separate inverter legs (PS-PWM): often referred to as interleaved switching. There are two main techniques under this category: PS-PWM and level-shifted PWM(LS-PWM). The PS-PWM scheme uses *n* evenly phase-shifted carriers with identical amplitude and frequency to control the switching pattern of each parallel-connected inverter leg. Except for the time domain phase shifting, the carriers can also be arranged to shift in amplitude within the range of the reference signals, which is called LS-PWM. Three different LS-PWM techniques are developed based on different disposition methods: phase disposition (PD-PWM) PWM, phase opposition disposition (POD-PWM), and alternate phase opposition disposition (APOD-PWM) [40]-[43].

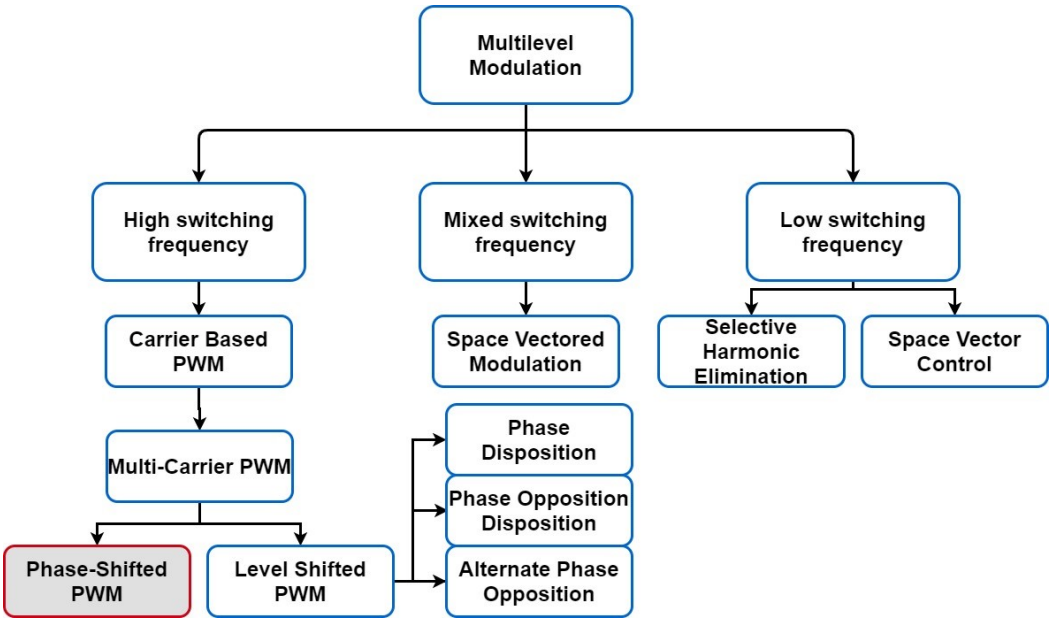


Figure. 1.10. Multilevel modulation techniques classification summary.

Space vector modulation is a scheme that uses a reference vector to represent a reference voltage. This scheme involves several discrete switching states, and each of them corresponds to a possible voltage vector [46]-[48]. For low switching frequency multilevel modulation, some algorithms have been developed for some specific applications. For instance, selective harmonic elimination (SHE) is used for very high-power applications due to its low switching losses [49]-[50]. However, due to the difficulty and the complexity of the design, the SHE technique is usually designed for VSCs with a limited number of levels [2]. On the other hand, multilevel space vector control (SVC) can be designed with a higher number of levels by using a high number of voltage vectors [51]. However, as the number of levels increases, multilevel space vector control complexity becomes too great, and reference carrier-based PWM is preferred. In addition, if PWM control requires some custom modifications, such as described in this thesis for flux compensation, space vector control becomes very complex.

Numerous PWM schemes for interleaved paralleled multilevel inverters have been researched. However, most of the modulation schemes generate unexpected issues such as low-quality output line voltages, generating large high-frequency circulating currents, requiring complicated converter modification [7], [17]-[18]. To overcome these issues, reference/carrier manipulation techniques are presented in this thesis. The signal manipulation features can improve the output PWM voltage quality; however, they also bring flux jumping issues to the CIs core and increases the required cross-sectional area for the CIs, which also increases the weight of the inductors. Therefore, developing generalized flux balancing schemes with minor effects on the circuit output is highly desirable.

Besides the continuous PWM techniques for multilevel VSC, the discontinuous PWM (DPWM) is also widely used in the last few decades. Research has been done from the last few decades to prove the advantages of the DPWM over continuous PWM (CPWM) [51]-[53]. One of the main benefits of using such a DPWM technique is to reduce the switching losses and increase the VSC system's overall efficiency. A DPWM scheme designed for a two-level VSI is described in [54]-[55], where the proposed modulation algorithm can detect the current vector position relative to the inverter voltage reference

to calculate the optimum clamped duration. Therefore, the resultant clamped switching pattern can reduce the switching losses. An improved carrier-based DPWM (CB-DPWM) method for Vienna rectifiers is proposed in [56]. The proposed DPWM method can be operated with all modulation index (m_a) values and is simpler than the DPWM based on space vectors. Furthermore, a modulation scheme that combines the carrier-based space vector modulation and CB-DPWM is presented in [57] for rectifier application. The advantages of DPWM have also been researched for the multilevel VSC field. The operation and analysis for a three-level NPC converter described in [58] use both conventional 60^o DPWM and an alternative three-level 60^o DPWM. In addition, DPWM based on two-level space vector modulation for multilevel inverters (Five-level and seven-level) using zero-sequence offset voltages is shown in [59]. More recently, DPWM techniques have also been implemented for paralleled multilevel VSCs [6], [53]. The comparative analysis of DPWM and SVPWM operating with paralleled multilevel converters is presented in [53]. The peak flux in the CIs is proved to be smaller by using the DPWM scheme. A parallel three-phase VSI with three coupled inductors system presented in [6] uses altered DPWM 60^o reference signals to control the connected CIs. For all DPWM schemes, the total duration of the clamped (discontinuous) region per phase is 120^o. Consequently, one period of 120°, two periods of 60°, and four periods of 30° are generated, respectively. However, by using parallel-connected inverter legs with CIs and DPWM scheme, the flux in the CIs will also experience a jump because of the clamping periods (The sudden reference change). Therefore, the flux compensation technique can be useful for the DPWM technique for CI size reduction purposes.

1.4. Thesis contribution and organization

This thesis addresses the key issues of using cross-coupled inductors in the paralleled VSC system with reference/carrier manipulated interleaved PWM schemes. Additionally, discontinuous PWM (DPWM) is also described. Significant contributions of this thesis are as follows:

- By implementing the conventional PS-PWM to the paralleled CII, the PWM output line voltage has poor quality. In Chapter 2, two enhanced PWM schemes

are presented: (a) PS-PWM with carrier swapping, (b) PS-PWM with reference modification. The former one was initially proposed in [7], while the latter one originated from this thesis and the author's other publication. The proposed enhanced PWM schemes can generate the same high-quality PWM output phase and line voltages, which helps reduce the ac filter inductor size, weight, and material cost. In addition, due to the generality of the PWM schemes, they can be operated with any number of ILPP systems. More details about the design, logic, comparison, and analysis are presented in Chapter 2.

- Although the enhanced PWM schemes described in Chapter 2 can produce high-quality PWM output phase/line voltages, it also brings flux jumping issues to the CI core. The flux jumps significantly increase the peak flux in the CI, which requires a larger cross-sectional area for the CI to avoid core saturation. To balance the flux hence reduce the core size/weight, Two different flux compensation techniques designed for proposed PWM schemes are presented in Chapter 3: (a) Carrier frequency manipulation, (b) pulse injection compensation. Each compensation technique has its own advantages, and both of them can easily be implemented with digital controllers such as a Digital signal processor (DSP), Field-programmable gate array (FPGA), and Plecs RT box. Additionally, due to these compensation techniques' generality, both compensation techniques can be applied to the *n* ILPP system.
- For the proposed coupled inductor inverter (CII) topology, the discontinuous PWM can be a potential solution to reduce the switching loss further. Chapter 4 presents a dual inverter legs CII with modified carrier swapping DPWM (Two saturations of 60°) that operates at a high modulation index, which can be used for grid-connected applications. Flux compensations are added for segment clamping and carrier swapping to reduce the CI size while maintaining output voltages quality.

Chapter 2 Interleaved PWM techniques for CII

Interleaved VSCs have numerous attractive features, such as multilevel PWM voltage outputs, which can be more easily filtered. Consequently, the size and weight of filter components can be reduced. Conventional PWM techniques using interleaved carriers, PS-PWM, can be generally utilized for VSC with any number of parallel-connected legs located in each phase of a three-phase system. High-quality Multilevel PWM phase voltages can result; However, the quality of the PWM line voltage can still be poor due to imperfect aligning of the line voltage PWM switching states.

Two enhanced PS-PWM are used to improve the line voltages in a 3-phase system: (a) PS-PWM with carrier swapping; (b) PS-PWM with reference modification. The former was first proposed in 2015 [7], while the latter originated from this thesis. Both cases change the switching patterns of the inverter legs in each phase over specific magnitude ranges of the modulating signal used in each phase. This results in an improved alignment of the PWM switching edges in the line voltage. The control logic changing the inverter switching patterns depends on the magnitude of the modulating reference signals and the number of ILPP. The control logic details are given for cases using 2, 3, and 4 ILPP. The quality of the modified switching patterns is compared with a standard PS-PWM where no carrier or reference signal modification is used. A sample parallel converter system uses three parallel inverter legs per phase, see Fig. 2.1.

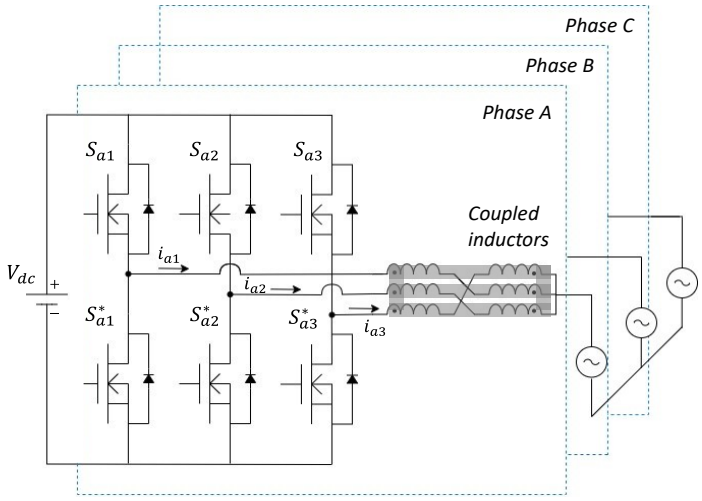


Fig. 2.1. Three-phase three ILPP CII circuit diagram.

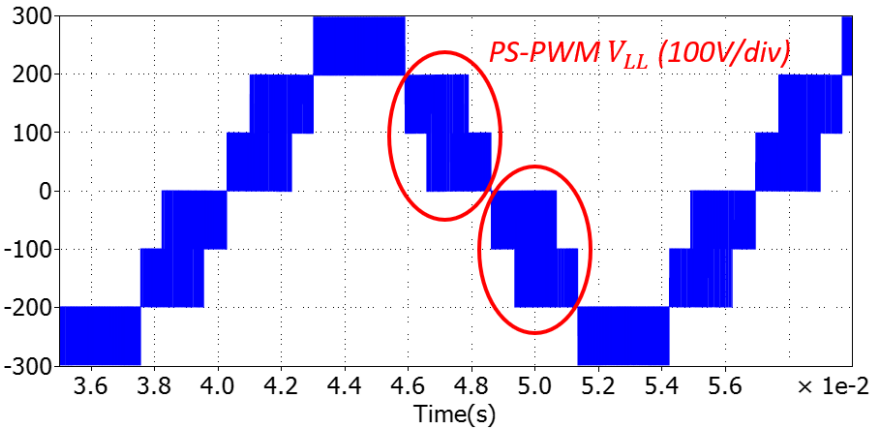
2.1. Conventional PS-PWM for CII

Different modulation schemes for multilevel converters have been researched in the last few decades, such as space vector modulation (SVM), phase-disposition PWM (PD-PWM), phase-shifted PWM (PS-PWM), etc. The conventional PS-PWM scheme interleaves n parallel-connected inverter legs. Correspondingly, *n* evenly phase-shifted carriers are used in each phase. The phase-shift angle for *n* parallel inverter legs per phase is determined by (2.1). This scheme can produce *n*+1 level phase and 2*n*+1 level line PWM output voltages, with PWM line frequencies 2*n* times higher than the switching frequencies. All the inverter legs in each phase use the same reference signal and are compared with a fixed set of carrier signals to generate the output voltage. The equivalent phase voltage is determined by (2.2), where the number of ILPP determines the number of levels of the PWM output phase/line voltages. In addition, the PS-PWM-based technique shifts certain harmonics, which cancels at the load but generates huge high-frequency circulating currents between the parallel-connected inverter legs and increases the conduction losses in the VSC. To suppress the circulating currents, coupled inductors are used at the output of each inverter leg to suppress the large circulating currents.

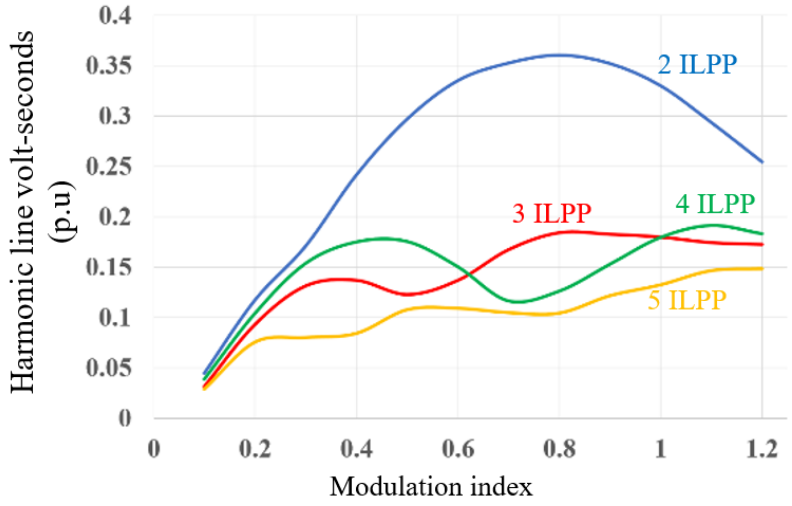
$$(360^{o} * [0, \frac{1}{n}, \frac{2}{n} \dots, \frac{n-1}{n}]) \qquad (2.1)$$

$$v_A = \frac{1}{n} \sum_{x=1}^{n} v_{Ax} \qquad (2.2)$$

In a three parallel-connected inverter leg CII system, three carriers are used (0^{o}, 120^{o}, 240^{o}) to determine the switching pattern of each inverter leg in each phase. This PWM scheme produces high-quality PWM phase voltage, but the quality of the PWM line voltage is poor, Fig. 2.2 (a). Similarly, for *n* ILPP cases, the line voltage will always experience undesired switching for certain intervals, which can lead to a worse current THD_f and harmonic line volt-seconds (p.u). The harmonic volt-second results with 2, 3, 4, and 5 parallel-connected ILPP are presented in Fig. 2.2 (b). Thus, developing an interleaved PWM technique that can generate both high-quality PWM phase and line voltages is highly desirable.



(a)



(b)

Fig. 2.2. Performance of a VSC with PS-PWM (a) PWM line voltage of the VSC with three inverter legs in each phase, (b) Harmonic volt-second of the VSC's PWM line voltage having 2, 3, 4, and 5 inverter legs in each phase(V_{dc} = 300V, f_{sw} = 20kHz, f_1 = 60Hz, Y-connected, L_f = 30 µH).

2.2. Enhanced PS-PWM with carrier swapping

The enhanced PS-PWM with carrier swapping was firstly proposed in [7] that uses two sets of evenly phase-shifted carriers to determine the switching pattern of *n* parallel-connected inverter legs, where the carriers can be expressed as (2.3) and (2.4). The reference signals range (-1 to +1) is divided into *n* regions. The set of carriers used in each phase is changed as the phase reference signal moves between the different regions.

As a result, this modified PS-PWM can avoid switching between three adjacent levels and produce high-quality n+1 level phase and 2n+1 level line PWM voltages.

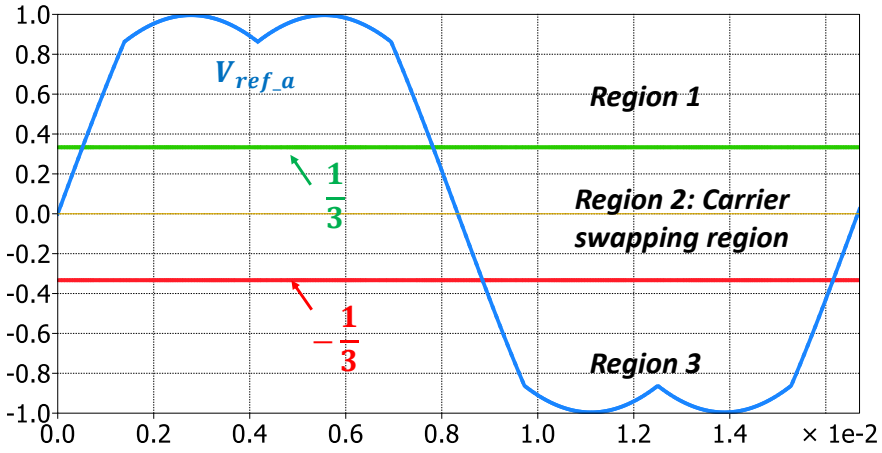
In a CII with 3 ILPP example, the reference signal is divided into three regions; region 1 is between 1 and +1/3, region 2 is between +1/3 and -1/3, and region 3 is between -1/3 and -1, see Fig. 2.3 (a). In addition, two sets of carriers (0º, 120 º, 240 º & 60 º, 180 º, 300 º) are used to control the switching pattern in each leg. When the reference signals are in regions 1 and 3, 0 º, 120 º, 240 º phase-shifted lagging carriers are used. When the reference signals are in region 2, 60 º, 180 º, 300 º phase-shifted leading carrier signals are used. Consequently, compare with Fig. 2.2(a), the high-quality 4-level phase and 7-level line PWM output voltages are generated, see Fig. 2.3 (b). The sets of phase-shifted carriers' details for n parallel-connected ILPP are given in Table I. Compare with the results shown in Fig. 2.2(b), the enhancement of this modulation scheme can be appreciated with lower harmonic volt-seconds (p.u.) of the PWM line voltage, see Fig. 2.3 (c).

$$\text{Lagging Carrier: } (360^{*}[0, \tfrac{1}{n}, \tfrac{2}{n}\ldots, \tfrac{n-1}{n}]) \tag{2.3}$$

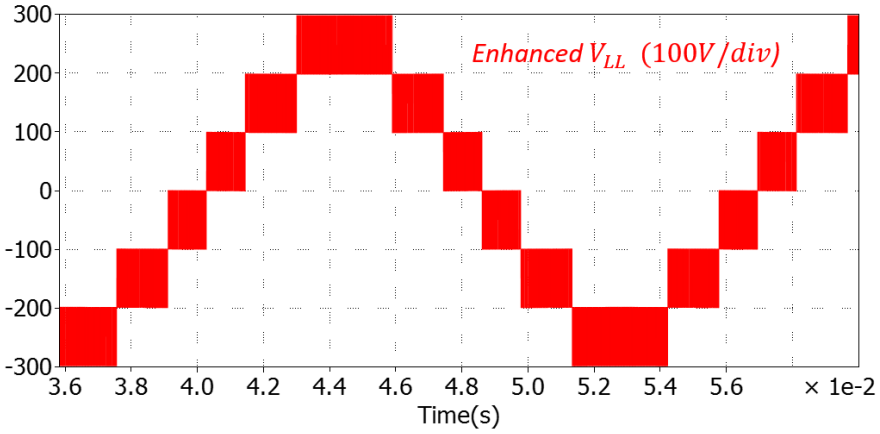
$$\text{Leading Carrier: } (360^{*}[0, \tfrac{1}{2n}, \tfrac{3}{2n}\ldots, \tfrac{2n-1}{2n}]) \tag{2.4}$$

Table 2.1: DETAILED PHASE-SHIFTED CARRIERS USED FOR ENHANCED PWM SCHEME

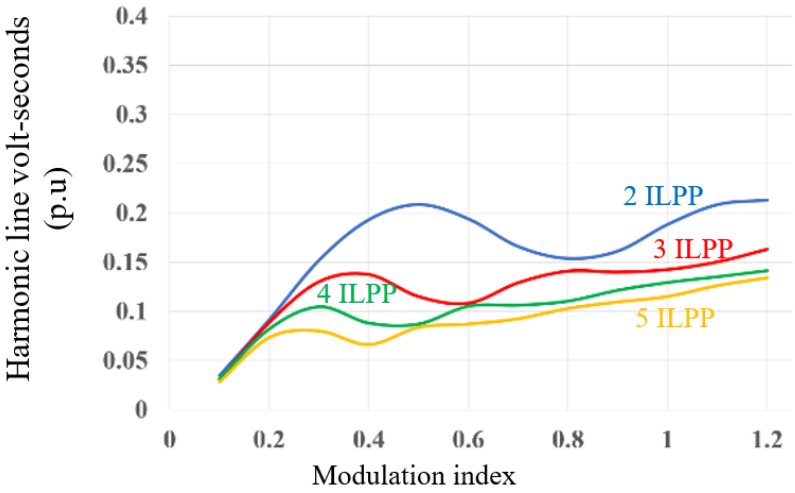
Number of parallel-connected ILPP	**Lagging carriers**	**Leading carriers**
2	0º, 180º	90º, 270º
3	0º, 120º, 240º	60º, 180º, 300º
4	0º, 90º, 180º,270º	45º, 135º, 225º,315º
n	$360^{\circ}*[0, \frac{1}{n}, \frac{2}{n}\ldots, \frac{n-1}{n}]$	$360^{\circ}*[0, \frac{1}{2n}, \frac{3}{2n}\ldots, \frac{2n-1}{2n}]$



(a)



(b)



(c)

Fig. 2.3. Performance of a VSC with enhanced PS-PWM and carrier swapping (a) regions of the reference signal, (b) PWM line voltage of the VSC with three inverter legs in each phase, (c)Harmonic volt-second of the VSC's PWM line voltage having 2, 3, 4 and 5 inverter legs in each phase (f_{sw}= 20kHz, f_l = 60Hz, Y-connected, L_f = 30 µH).

2.3. Enhanced PS-PWM with Reference Modification

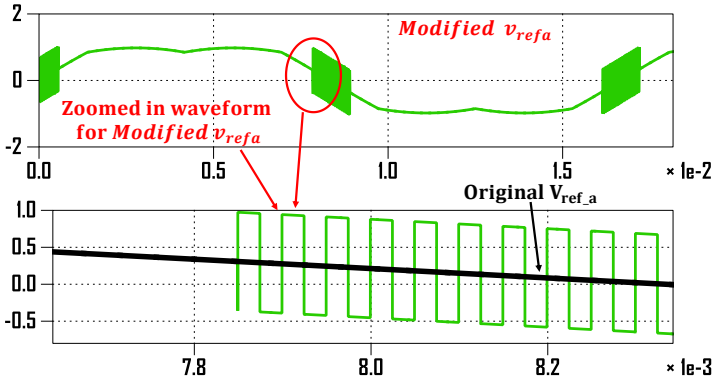
The PS-PWM with reference modification technique developed for the topology under consideration in Fig. 1.3 is also designed to improve the quality of the PWM line voltages. Instead of using an additional set of evenly phase-shifted carriers, the reference modification uses the same carrier as PS-PWM. To avoid switching among three adjacent levels, the reference domain (-1 to +1) is equally divided into *n* regions, and the additional modification will then be added to certain regions to mimic the carrier swapping.

Due to the generality of this PWM technique, it can be implemented with *n* ILPP, but the modification logic is different with different numbers of inverter legs in each phase. The technique logic is generally divided into two big groups based on whether the number of ILPP is odd or even. The odd number ILPP system is more straightforward in logic than the even number ILPP system. To better explain the difference between those two cases, 3 ILPP, 2 ILPP, and 4 ILPP systems are discussed in this subsection as examples. The feasibility of the technique is verified with the PLECS simulation, and the experimental results are also presented in the next chapter with flux compensation.

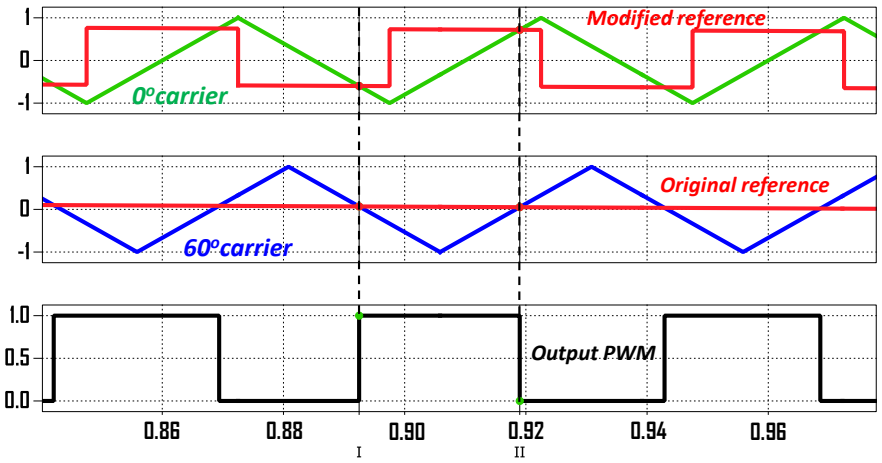
2.3.1. Odd number ILPP

For a VSC with 3 ILPP, only one set of three evenly phase-shifted carriers (0^o, 120^o, 240^o) is needed. The reference domain is equally divided into three regions like the enhanced PS-PWM with carrier swapping shown in Fig. 2.3 (a). Whenever the reference signals are within regions 1 and 3, the reference signals are compared with the 120^o phase-shifted carriers to control the switching of the parallel-connected inverter leg in each phase. However, whenever the reference signals are in region 2, 120^o phase-shifted square wave pulses with an absolute magnitude of 2/3 and frequency identical to the carrier frequency (f_s) are added to original reference signals, see Fig. 2.4 (a). The resultant reference signals are used to compare with the carriers to control the switching of each inverter leg. If the 0^o, 120^o, and 240^o carriers are respectively allocated to the 1st, 2nd, and 3rd inverter legs in each phase, then the 0^o, 120^o, and 240^o phase-shifted pulses

are added to the reference signals that control the switching in 1st,2nd, and 3rd inverter legs accordingly. This modulation scheme mimics the carrier swapping, which can produce the same PWM output as the carrier swapping technique, see Fig. 2.4 (b). The reference modification technique avoids the problem of switching among three adjacent levels and generates high-quality 4-level phase and 7- level line PWM output voltages in a 3 ILPP example, see Fig. 2.5. Similarly, the logic for an odd number of ILPP is to divide the reference into n regions. The carriers used can be generated with the expression (2.1). Among those regions, $\frac{n}{2}-1$ even order regions need reference modification with square pulses that have an absolute magnitude of $2/n$ (e.g., 5 ILPP system requires regions 2 and 4 to be modified). The resultant high-quality line output voltage is useful to reduce the size of ac filters.



(a)



(b)

Fig. 2.4. The proposed 3 ILPP reference modifications: (a) modified reference signal, (b) detailed logic that reference modification mimics carrier swapping.

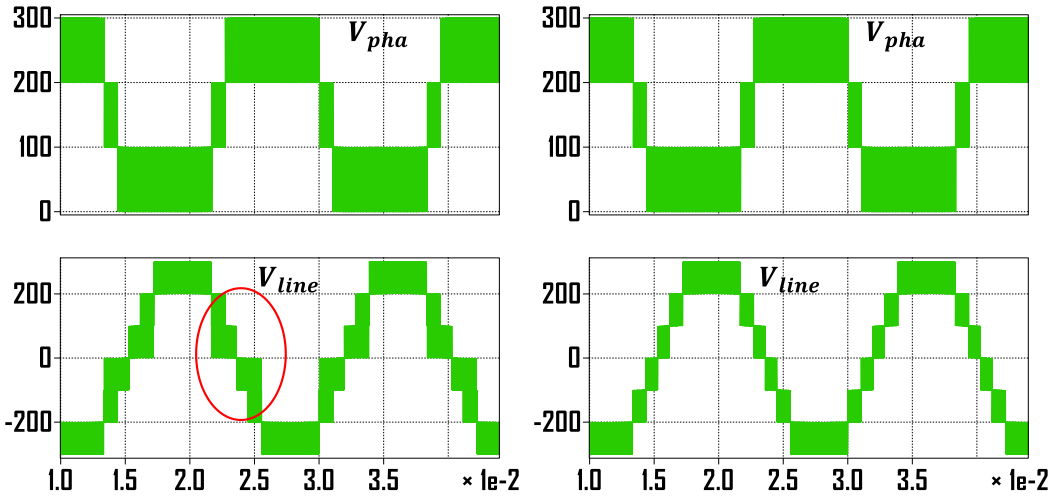


Fig. 2.5. Phase and line PWM voltages for CII with 3 ILPP using reference modification PWM technique.

2.3.2. Even number ILPP

For a VSC with an even number ILPP, simply using phase-shifted square wave pulses can no longer produce the high-quality line voltages due to the overmodulation. Therefore, a different logic will be applied for the modification pulses instead. This subsection compares the interleaved PS-PWM performance and the reference modification PWM on a 2 ILPP example, see Fig. 2.6.

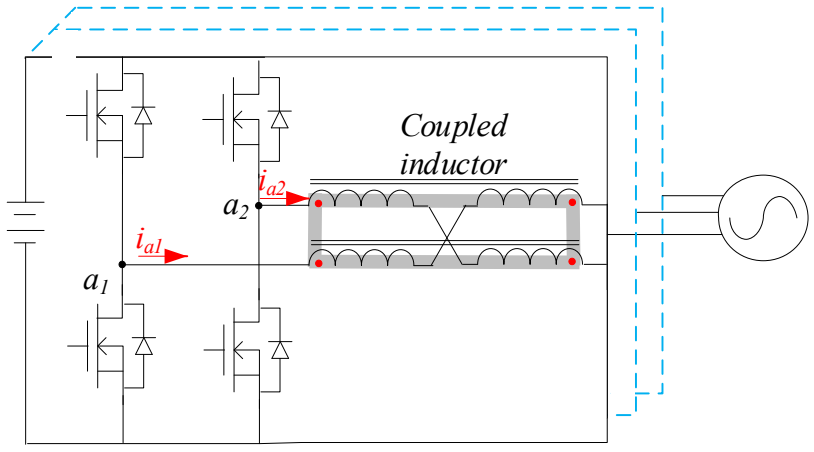
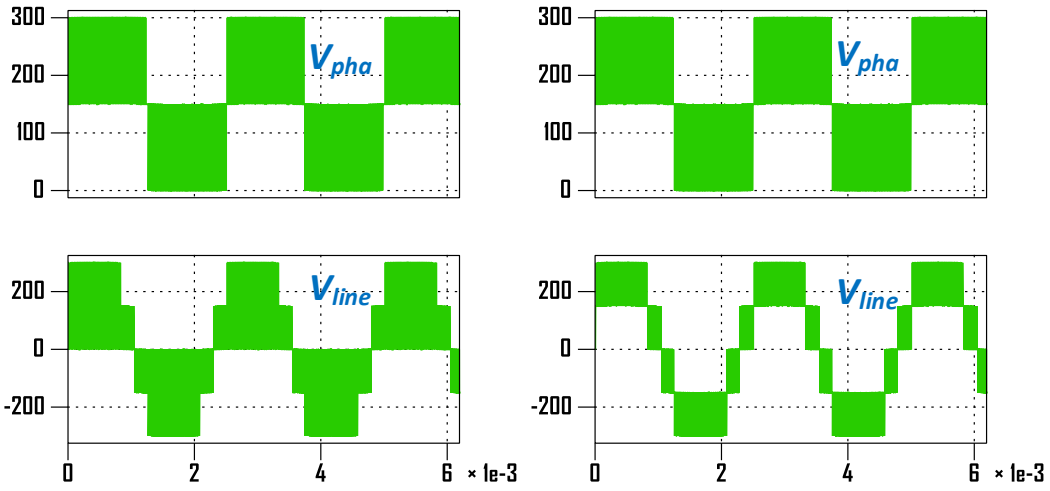


Fig. 2.6. The 2 inverter legs per phase CII circuit diagram.

The interleaved PS-PWM uses two carriers with a phase angle of 0° and 180° to control the switching of the parallel-connect inverter legs in each phase. The 120° phase-shifted sinusoidal reference signals (v_{refa}, v_{refb}, v_{refc}) are compared with their respective carrier to set the gate pulse of the switches. This modulation scheme generates high-quality 3-level PWM phase voltages (v_{phA}), and low-quality 5-level PWM line voltage (v_{LL}) due to the undesired switching, see Fig. 2.7 (a). The reference modification PWM technique (v_{refm}) for 2 ILPP produces both high-quality 3-level phase and 5-level PWM line voltages without changing carriers, see Fig. 2.7 (b). This scheme uses a fixed set of phase-shifted carriers (0° and 180°) to determine the switching in each inverter leg like the PS-PWM scheme. The 120° phase-shifted sinusoidal reference signals (v_{refa}, v_{refb}, v_{refc}) are divided into two regions, +1 to 0 for region 1 and 0 to -1 for region 2, see Fig. 2.8. When the reference signals are in region 1, they are compared with their respective carriers to control the switching in each inverter legs. However, when the reference signals are in region 2, a modified variable pulses train with an absolute magnitude of 1, a variable duty cycle (D_{var}) expressed as (2.5), and a phase shift of 90° is added to the reference signals controlling the switching in the inverter legs a_1,b_1, and c_1. A logic diagram is given in Fig. 2.9 to illustrate the pulses generation process for one inverter leg in Phase A. Likewise, pulses with the same magnitude, variable duty cycle, and a phase shift of 270° are added to the reference signals that determine the switching in the inverter legs a_2, b_2, and c_2. In addition, a saturation function is used to limit the range of the modified reference signals within the range of -1 to1. Such a modification mimics the 90° carrier swapping, which generates the same PWM output as the carrier swapping does, see Fig. 2.10. This modulation method generates high-quality 3(n+1) levels phase and 5(2n+1) levels PWM line output voltages quality like the enhanced PS-PWM with carrier swapping technique described in the previous subsection.

$$D_{var} = \frac{1}{2} \times (1 - |V_{ref}|) \qquad (2.5)$$



(a) (b)

Fig. 2.7. Phase and line PWM voltage for 2ILPP system: (a) PS-PWM, (b) enhanced PS-PWM with reference modification PWM.

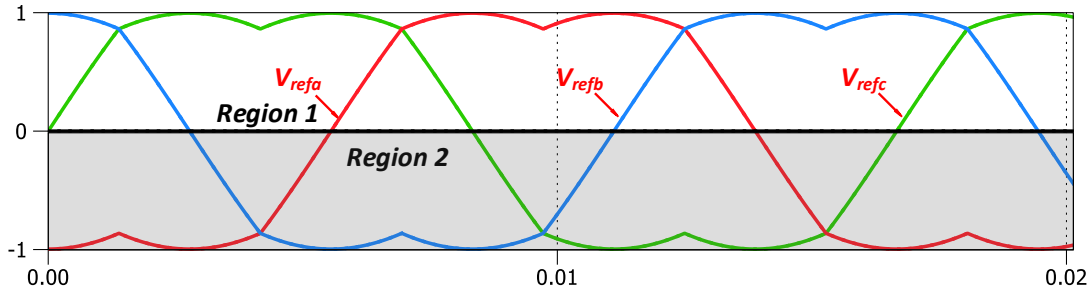


Fig. 2.8. Region division for 2 ILPP coupled inductor inverter.

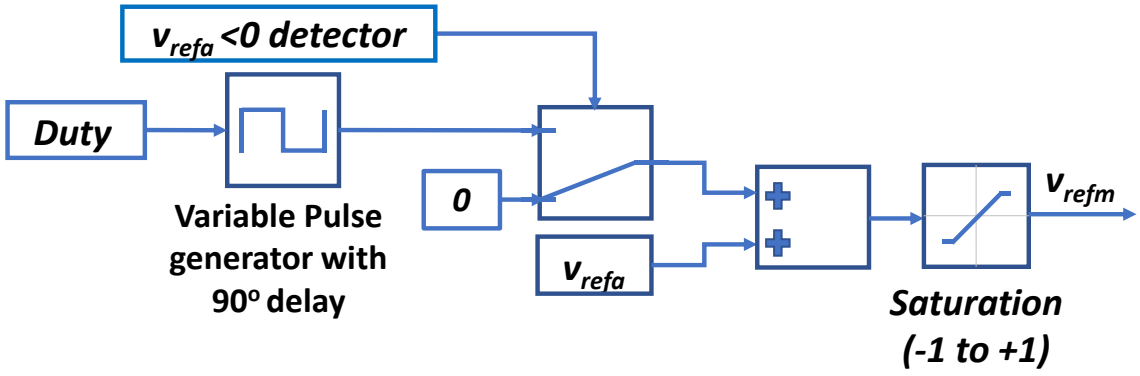
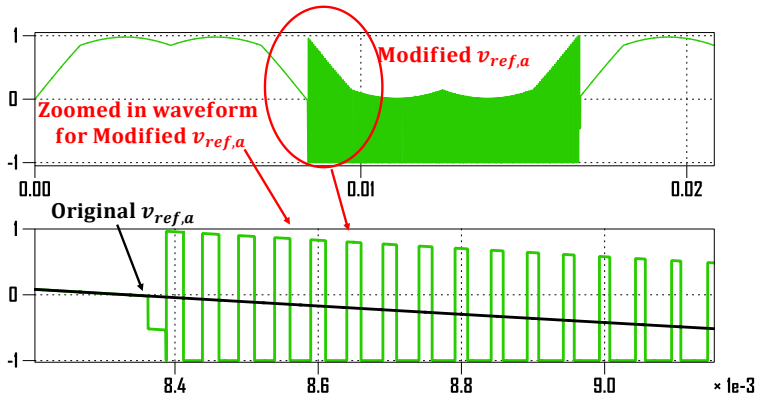
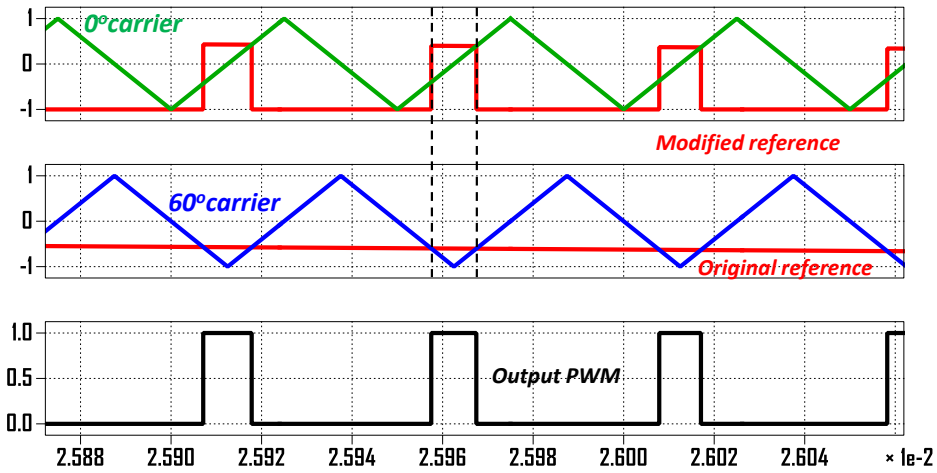


Fig. 2.9. Logic block diagram for reference modification.



(a)

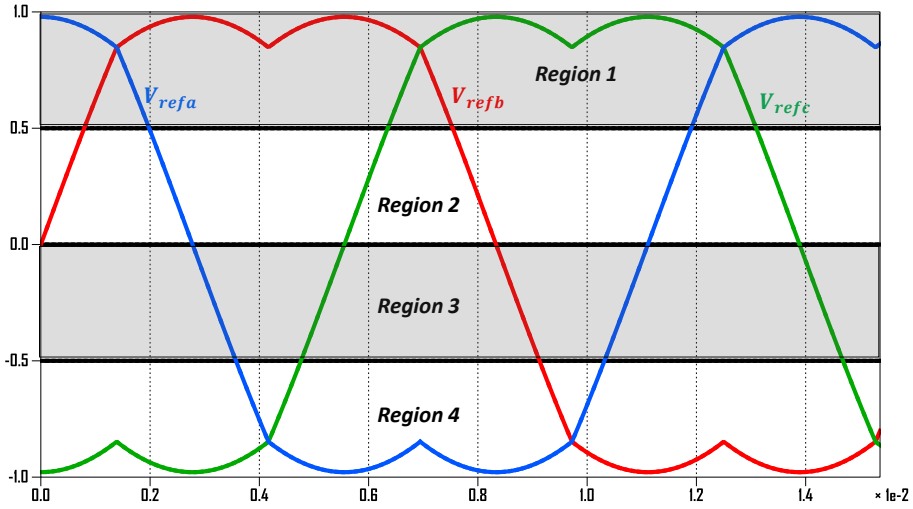


(b)

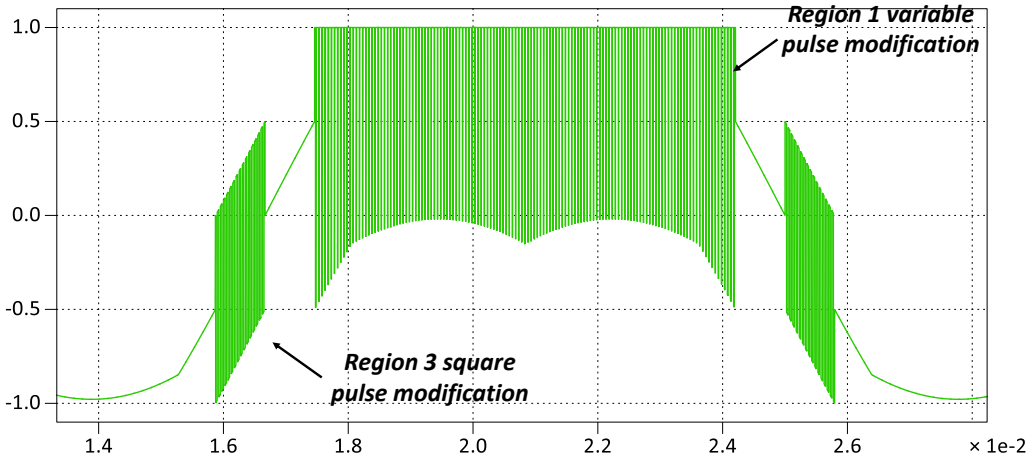
Fig. 2.10. The proposed 2 ILPP reference modification: (a) modified reference signal, (b) detailed logic that reference modification mimics carrier swapping.

Due to the generality of the technique, it can be implemented to an *n* ILPP system. However, when *n* is an even number and greater or equal to 4, two or more regions need to be modified. Among those regions, only one region includes maximum or minimum reference signal requiring variable duty pulses (The regions that need modification can be either region 1,3 or region 2,4). Besides the regions mentioned, Other regions will only need the fixed pulse width modification, like the one introduced for the odd number ILPP system. For a 4 ILPP system example, the 120° phase-shifted sinusoidal reference signals (v_{refa}, v_{refb}, v_{refc}) are divided into four regions, see Fig. 2.11 (a). Region 1 includes the maximum region, which requires variable duty pulses modification expressed by (2.5). On the other hand, since region 3 does not touch maximum or minimum, it only needs

the fixed pulse width (50% duty) modification, where the magnitude of the pulses is ½ (2/*n*), see Fig. 2.11 (b). Similar to other inverter legs, the logic is the same, except the phase delay for the pulses is different. Additionally, a similar principle can also be applied to 6, 8, 10... ILLP system, where the modification logic is combined by fixed square/variable pulse modification. By using this PWM technique, the quality of the PWM line voltage quality is significantly improved, see Fig. 2.12.

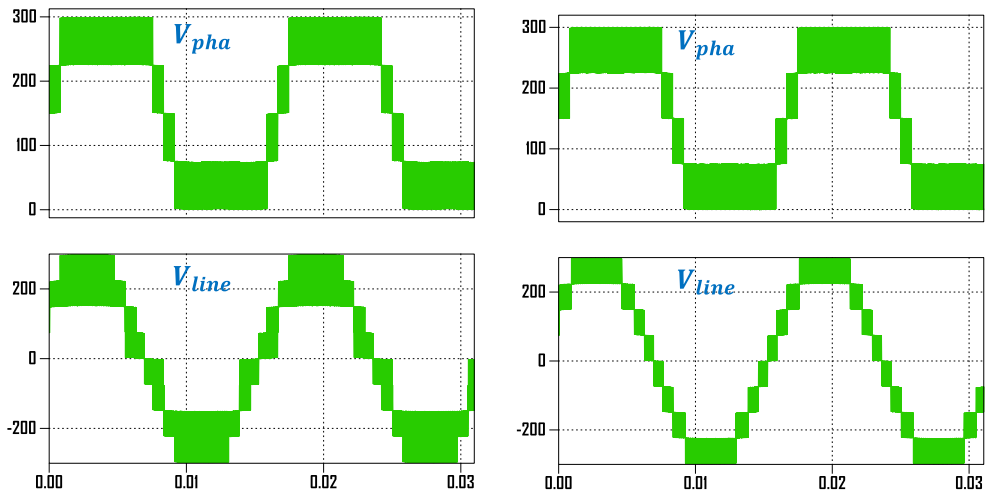


(a)



(b)

Fig. 2.11. 4 ILPP coupled inductor inverter example: (a) Region division, (b)reference signal v_{refa} after modification.



(a) (b)

Fig. 2.12. Phase and line PWM voltage for 4ILPP system: (a) PS-PWM, (b) enhanced PS-PWM with reference modification PWM.

2.4. Conclusion

Three different PWM techniques are presented for parallel-connected CII: (a) PS-PWM; (b) enhanced PS-PWM (carrier swapping); (c) enhanced PS-PWM using reference signal modification. When used in 3-phase applications, the line voltage in conventional PS-PWM can switch between three adjacent voltage levels, which lowers the quality of the PWM line voltages. The performance of two modified PS-PWM schemes is tested. The carrier swapping enhanced PS-PWM controller is proposed in 2015 [7], and PS-PWM using reference signal modification is proposed in the thesis. Both methods produce high-quality n+1 level PWM phase and 2n+1 level PWM line voltages with a PWM voltage step of V_{dc}/n, and a PWM frequency of 2n higher than the switching frequency (f_{sw}): V_{dc} represents the dc-link voltage, and f_{sw} represents the converter switching frequency. Overall, the enhanced PS-PWM schemes provide a higher-quality PWM line voltage in terms of better line voltage harmonics. In addition, it can also provide lower current THD_f(%) (the analysis curve is shown together in Chapter 3 with compensated waveforms), which can favor the use of the small ac filter inductor and reduce the overall size /weight for the system.

Chapter 3 Pre-processing Compensation techniques for Flux Jumping in CII

Enhanced PS-PWM with carrier swapping and reference modification both improve the quality of 3-phase PWM line voltages in parallel connected converters. However, during transitions from an unmodified PWM region to a modified region, a jump in the coupled inductor flux can occur. At the very least, this represents a sudden increase in the inductor peak flux above those that can be predicted from the controlled flux patterns experienced when using PS-PWM alone. At worst, these jumps can accumulate in successive transitions, representing a drift in the core dc flux: this is more pronounced if high fundamental frequencies are used. These flux jumps significantly increases the peak flux in the CIs, which can saturate the CIs or require larger cores to be used. Two different pre-processing PWM techniques are described to compensate for these flux jumps: (a) Carrier frequency manipulation, (b) Pulse injection. Where (a) only involves enhanced PS-PWM with carrier swapping and (b) involves both enhanced schemes (carrier swapping and reference modification). The peak core flux in the CI is reduced and returned to the predictable pattern associated with using PS-PWM alone. This results in a more reliable core design procedure that reduces the size, weight, and cost of the CIs.

3.1. Coupled Inductor flux jumps during transition regions

To avoid core saturation for the CI, the flux jump dc offset components must be controlled to be zero. Since the fundamental flux produced by the flow of the ac currents in the CIs cancels, only the high-frequency flux generated by the high-frequency PWM voltage across the CIs goes through the CI magnetic cores. Therefore, the natural flux balancing is achieved when PS-PWM is used for the parallel CII [22], see Fig. 3.1 (a). However, by using the PWM techniques mentioned in the previous chapter. The carrier swapping/ reference modification during region transition will lead to a sudden change in the switching pattern and high-frequency PWM voltage across the CI, which leads to a sudden change for the flux in the CIs. Consequently, a dc flux injection is added to the

flux pattern and changes the dc offset of the flux waveform. The dc flux injection significantly increases the peak flux in the CI during the transition and can saturate the CI, see Fig. 3.1(b). The jump issue becomes even worse when operating the system at a high fundamental frequency, where the flux jump could accumulate infinitely. The peak flux density in the CIs is expressed as (3.1), where V_{dc} is the dc-link voltage, N is the number of turns, A_c is the core cross-sectional area, and f_c is the carrier frequency.

$$B_{max} = \frac{V_{dc}}{16NA_c f_c} \tag{3.1}$$

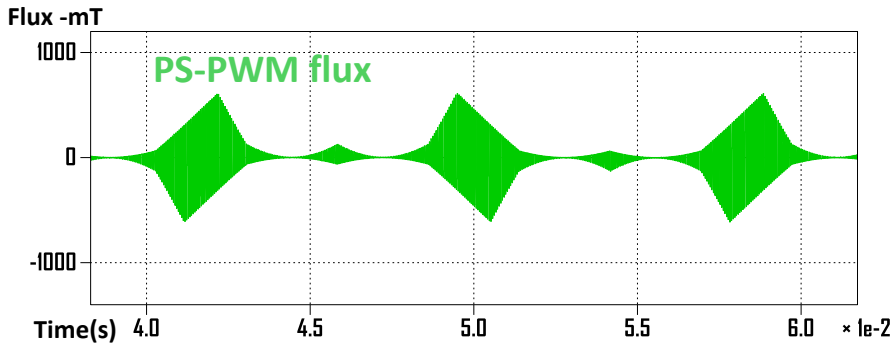
Furthermore, the flux jump results in current jumps in CIs, which can exceed the current rating of the switching devices. The current jumps will increase conduction losses in the switches and CI windings in advance. A simulation of the peak flux in the CIs produced by the PWM schemes under consideration is shown in Fig. 3.2 frequency (Note, all analysis is obtained with f_1 = 60Hz). The simulation parameters used for the peak flux plot are given in Table. 3.1(For all the simulation results shown in this chapter, the simulation parameters are identical to this Table unless mentioned in the figure name/Label). For a 3 ILPP example, The per-unit peak flux density generated by the enhanced PS-PWM with carrier swapping is 270% higher than the peak flux density generated by the PS-PWM scheme for a 3 ILPP system. Therefore, it is highly desirable to develop compensation techniques that can suppress the flux jump.

Table. 3.1 3 ILPP Simulation and experimental parameters

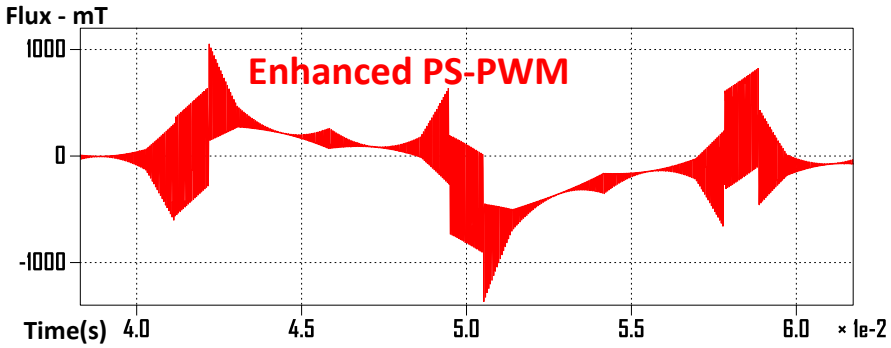
Parameter	**Value**
DC link voltage	300V
Switching frequency	20kHz
Fundamental frequency	60Hz
Winding inductance	0.2mH
L-load	30μH

PWM techniques with carrier/reference manipulation and flux balancing control in CIs have been researched in [22], [27], [52]. The existing techniques can be generally divided into two approaches: Post-processing, where the compensation is added by external devices/algorithm after each sampling; And pre-processing, where the compensation is predesigned to be added during the flux jumping period directly on the PWM technique. A PD strategy that involves double commutations at every zero crossings is presented in [27]. The modification compensates for the differential mode current and the flux in the CIs during the band transition. However, the PD strategy introduces undesired disturbances on the line voltage during the band transition, which degrades the quality of the line voltage. A PD strategy that injects a square wave to the reference signals and uses a post-processing state machine to correct the switching pattern of each leg is described in [50]. The proposed scheme controls and maintains the required dc common-mode current and flux for a three-phase CI converter. A state machine is used to implement the PD-PWM techniques described in [27] and [50]. The flux in the CIs are well controlled by using such a technique. However, the complexity of the technique and the calculation load for the state machine increases when the number of ILPP increases. On the other hand, A phase-disposition PWM scheme (PD-PWM) is described in [22] with pre-processing flux balancing technique, where the reference signals are modified during the PD band transition to balance the flux in the CIs.

In this thesis, two different pre-processing techniques are presented to compensate for the flux jump issue. The first compensation technique is named as carrier frequency manipulation, where the frequency of the carrier is modified whenever the reference signals transit into a new region (carrier swapping happens). The second one is introduced as pulse injection, where this technique injects pluses on the reference signals when they move between regions. The pulse injection method can be applied to both enhanced PWM schemes mentioned in Chapter 2, where it has similar principles but different logic for each of them. Therefore, totally three compensation approaches are presented in this chapter. The compensation techniques are verified with simulation and experimental results, and the laboratory prototype is designed in the lab to verify the proposed techniques, see Fig. 3.3.



(a)



(b)

Fig. 3.1. Flux density in the CIs for 3 ILPP CII system at f_{sw} = 20 kHz, f_1 = 60 Hz: (a) PS-PWM without jumping (b) Enhanced PS-PWM with carrier swapping PWM flux jumping.

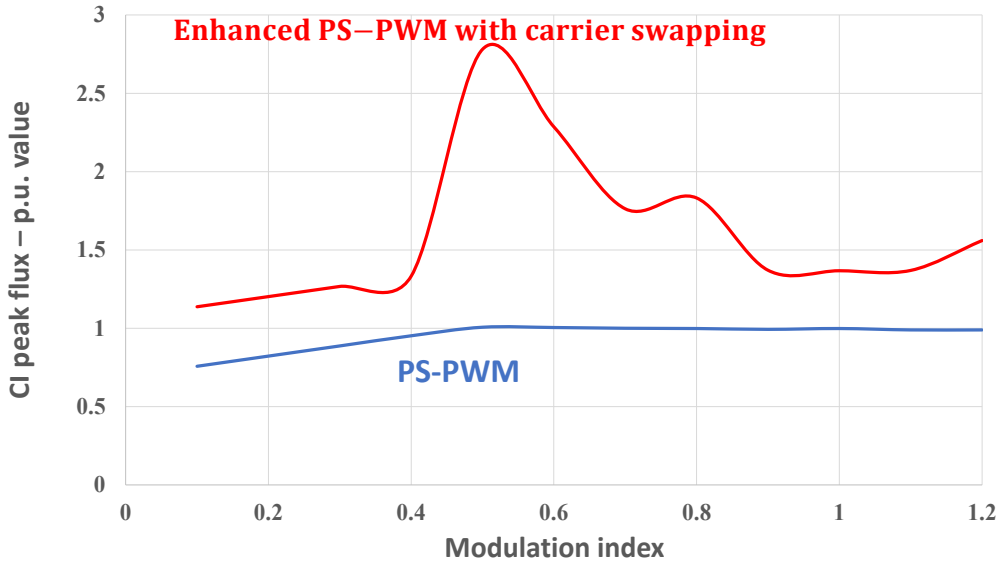


Fig. 3.2. The p.u peak flux density in the CI cores produced by both the PS-PWM and the enhanced PWM schemes for 3 ILPP system operating at f_1 = 60Hz, f_{sw} = 20 kHz.

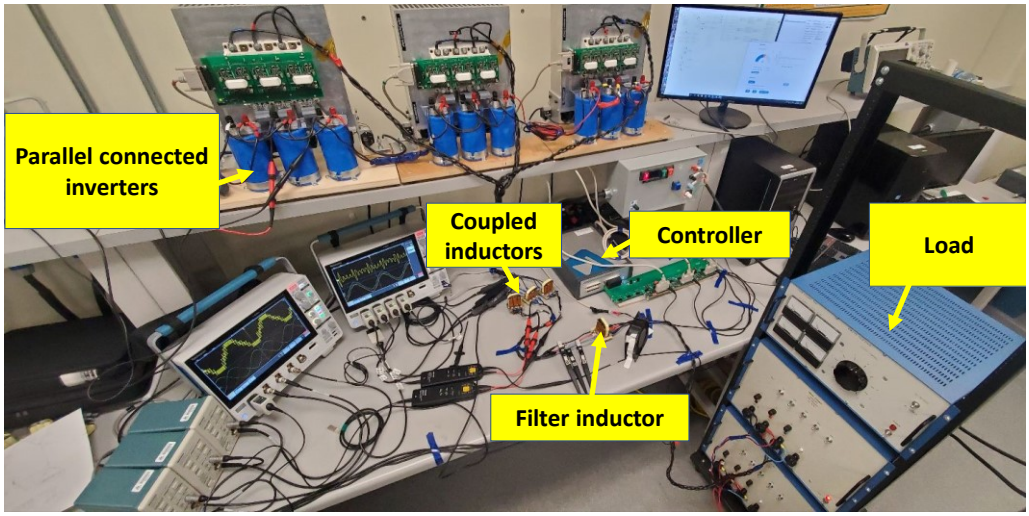


Fig. 3.3. Experimental setup for 3ILPP CII.

3.2. Carrier frequency manipulation

The carrier frequency manipulation approach is designed based on the enhanced PS-PWM with carrier swapping to balance the flux jump in CIs. The explanation given in this subsection is based on the three-phase 3 ILPP system, where lagging carriers are used while reference signals are in the region 2, see Fig. 2.4(a).

3.2.1. Logic details

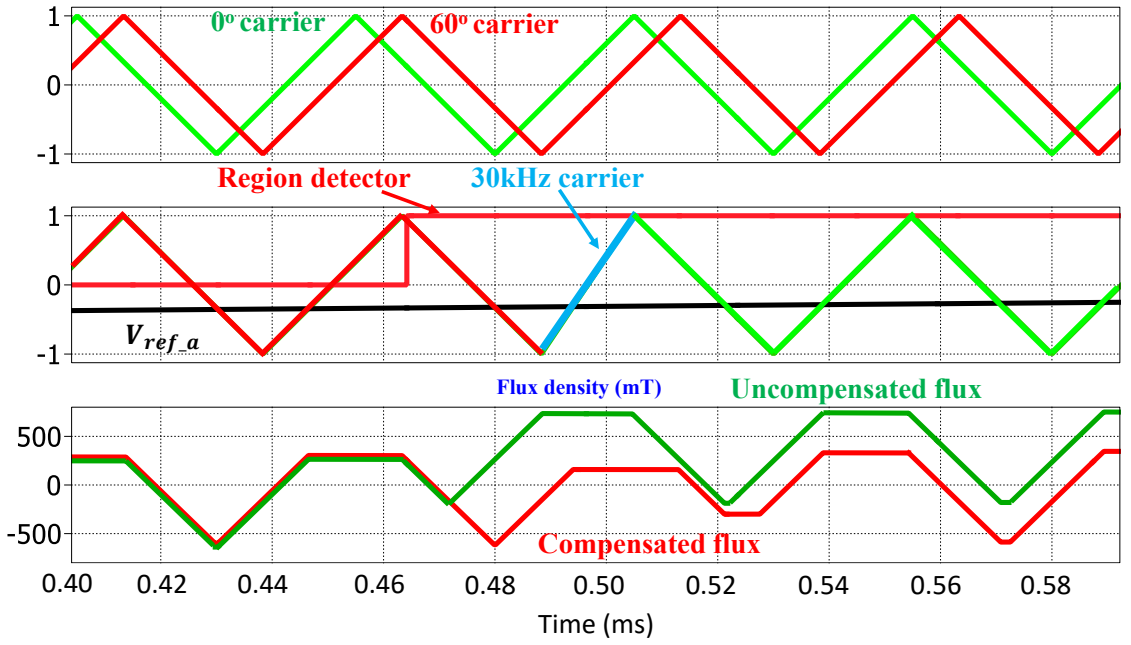
As the reference signals move between the regions, the carrier used to control the switching pattern in each inverter leg is changed, see Fig. 2.3(a). Instead of instantaneously changing the phase-shifted carrier as the reference signal moves into a new region, the change is delayed until the carrier reaches its first maximum or minimum point. A new carrier with a higher/lower frequency is then used, for only half the carrier cycle, to connect the previous carrier's maximum/minimum point with the upcoming carrier's minimum/maximum point, Fig. 3.4. When the reference signal moves into region 2, a higher frequency carrier (blue line) connects the peak of the 60° carrier and the minimum point of 0° carrier, see Fig. 3.4(a). When the reference signal leaves region 2, a

lower frequency carrier connects the minimum point of the 0° carrier and peak of the 60° carrier, Fig. 3.4(b). These manipulations also apply to the other two inverter legs similarly when the lagging carriers (120°, 240°) and the leading carriers (180°, 300°) are switched. By using such a carrier manipulation, the sudden change of the switching pattern/PWM high-frequency voltage becomes a gradually smooth change. This compensating technique makes sure switches have the appropriate on/off period to follow the jump-free switching pattern, reducing the peak flux in the CIs. The enhanced PS-PWM with carrier swapping and this compensation technique generates high-quality 4 (n+1) levels phase and 7 (2n+1) levels line PWM output voltages for a three-phase 3 ILPP system.

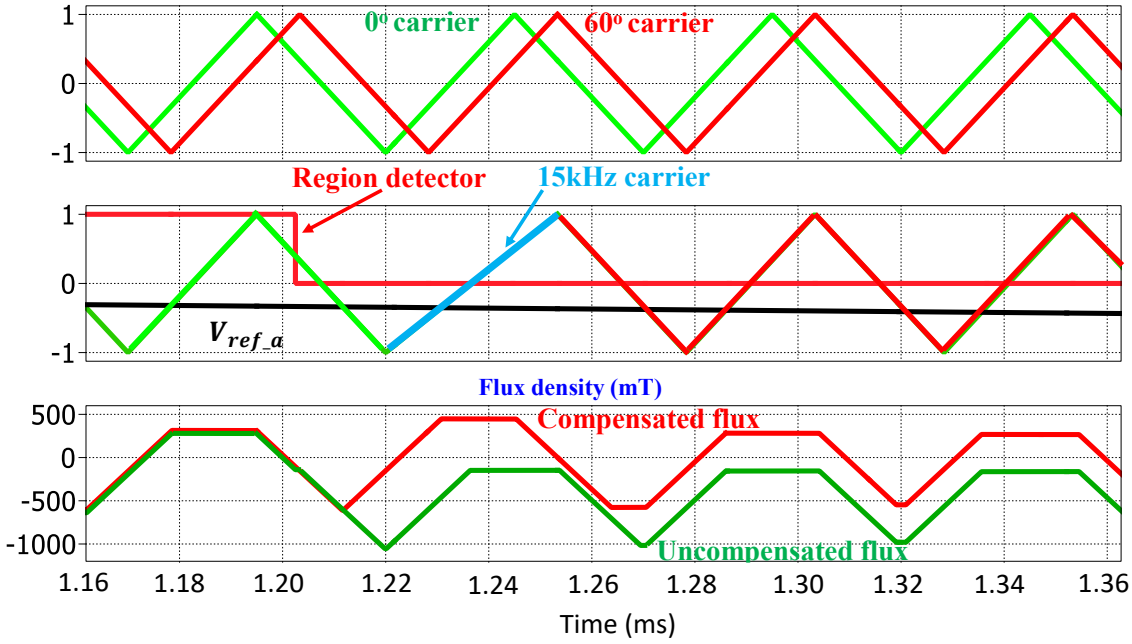
The frequencies of the carriers used during the transition to connect the leading and lagging carriers depend on the number of parallel-connected ILPP and the switching frequency of the system. In the example above, the system is running with a switching frequency (f_{sw}) of 20kHz, and the frequencies of the modified carriers are 30kHz and 15kHz. This technique could also be used in a system with n parallel-connected ILPP. Table 3.2 presents the frequencies that should be used for n parallel-connected ILPP.

Table 3.2: Modified transition carrier frequencies for the carrier frequency manipulation technique

Number of parallel-connected ILPP	**Lagging carriers to Leading carrier**	**Leading carriers to Lagging carriers**
2	0.6667 f_{sw}	2 f_{sw}
3	0.75 f_{sw}	1.5 f_{sw}
4	0.8 f_{sw}	1.333 f_{sw}
n	$\frac{n}{n+1} f_{sw}$	$\frac{n}{n-1} f_{sw}$



(a)



(b)

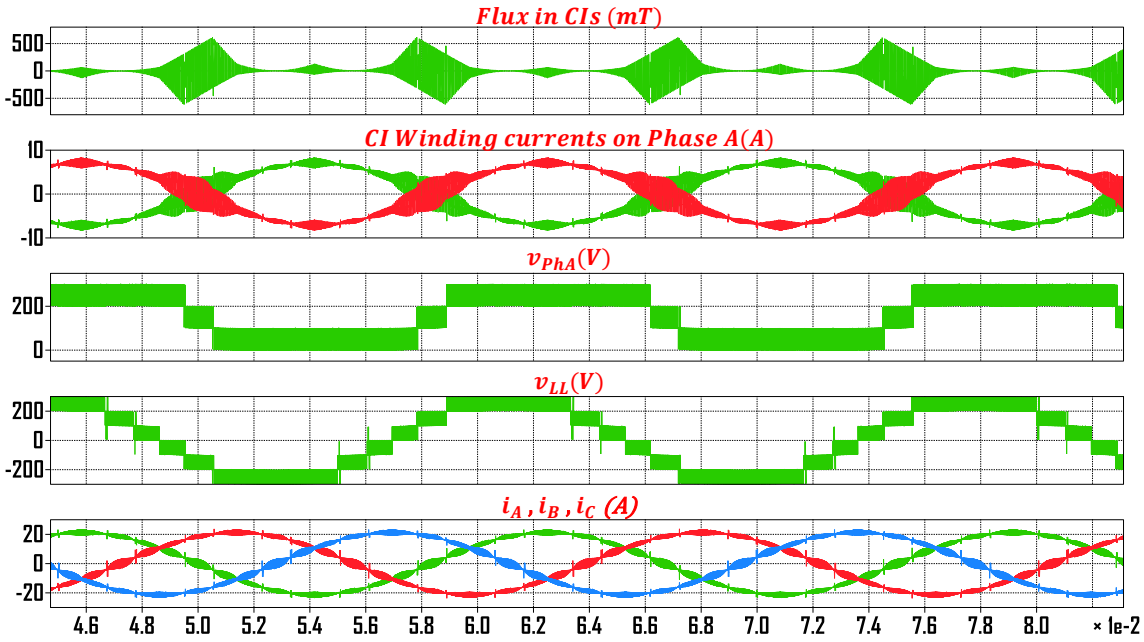
Figure. 3.4. Carrier frequency manipulation compensation technique illustration: (a) reference signal moving into region 2, (c) reference signal moving out from region 2.

3.2.2. Simulation results and performance analysis

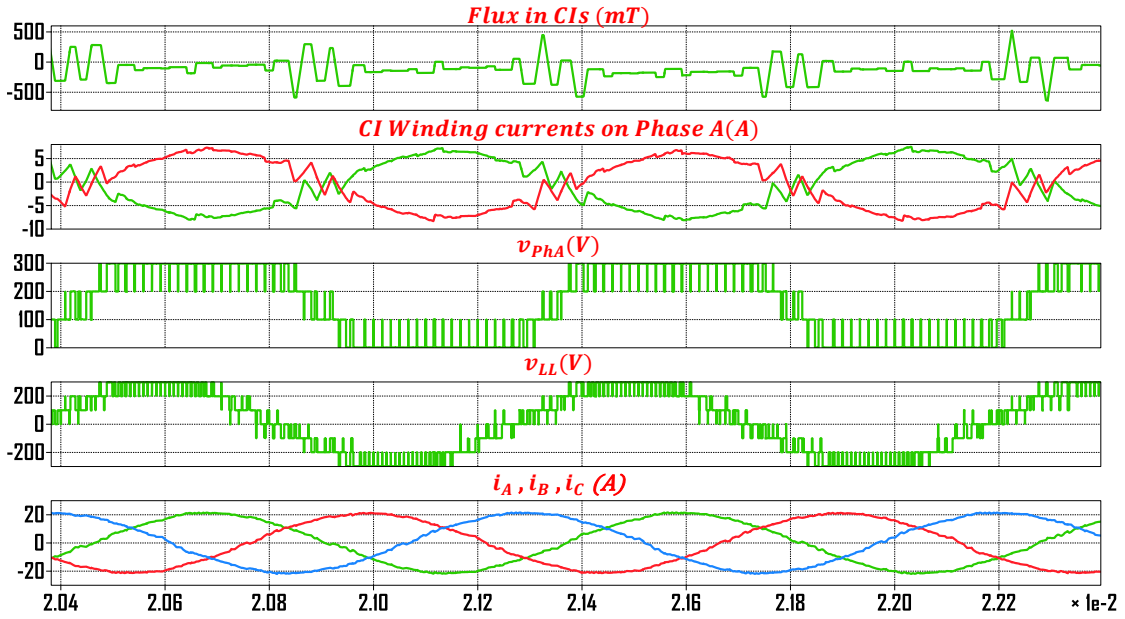
The simulated CII specifications that mentioned in Table. 3.1 was chosen to approximate the results of an 11kw laboratory prototype. The flux in the CIs, the CI winding currents (i_{a1}, i_{a2}), phase/line output voltage (v_{phA}/v_{LL}), and the load currents (i_A, i_B, i_C) are shown in Fig. 3.5. Two groups of simulation results are given below. One group is running at f_1 = 60 Hz, L_f = 30 μH. The second group runs at f_1 = 600Hz, which requires a larger filter inductor L_f = 0.2 mH. The Simulation shows the feasibility of the system at both low and high fundamental frequencies.

The compensation techniques effectively control the transition between different phase-shifted carriers and eliminates the flux jump in the CIs when generating high-quality 4-level (n+1) phase and 7-level (2n+1) line PWM output voltages. The flux patterns produced by the compensated enhanced PS-PWM are very similar to the flux produced by the PS-PWM scheme in the CIs. The CIs winding currents, therefore, do not experience the current jump as well.

The harmonic volt-seconds plot of the PWM line voltages and the current THD_f(%) plot of the system are compared with the PS-PWM scheme, see Fig. 3.6 and Fig. 3.7. Although the enhanced PS-PWM with carrier swapping with carrier frequency manipulation has slightly worse results than the pure enhanced PS-PWM with carrier swapping, it is still significantly better than the PS-PWM waveform. Especially for the harmonic volt-seconds plot, the results are almost the same at high modulation index for cases with/without compensation. More importantly, since the PWM scheme is based on enhanced PS-PWM with carrier swapping, high-quality multilevel PWM outputs voltages are obtained. This can favor the use of a small filter inductor at the output of each inverter leg to reduce the total weight of the VSC system.



(a)



(b)

Fig. 3.5. The simulated waveform of a Y-connected CII (carrier frequency manipulation) having 3 ILPP operated at f_{sw} = 20 Hz, V_{dc} = 300 V, R = 5.5 Ω, m_a = 1.13, and (a) f_1 = 60 Hz, L_f = 30 µH (b) f_1 = 1.1 kHz, L_f = 0.2 mH.

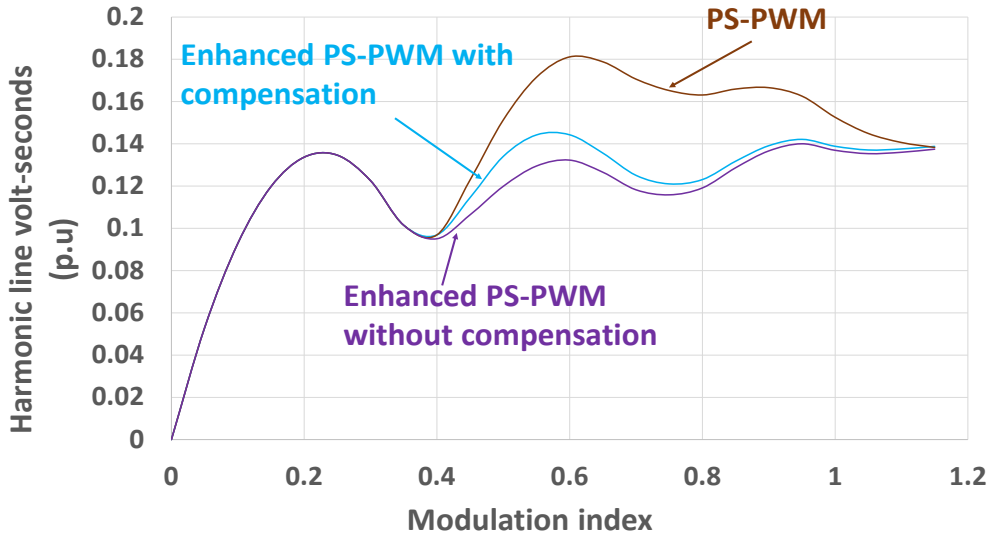


Fig. 3.6. Harmonic volt-second Performance the VSC operating with PS-PWM, the enhanced PS-PWM (carrier swapping) with/without compensation techniques (f_1 = 60, f_{sw} = 20kHz, L_f = 30 µH, I_{phase} = 30.6 A, Y-connected).

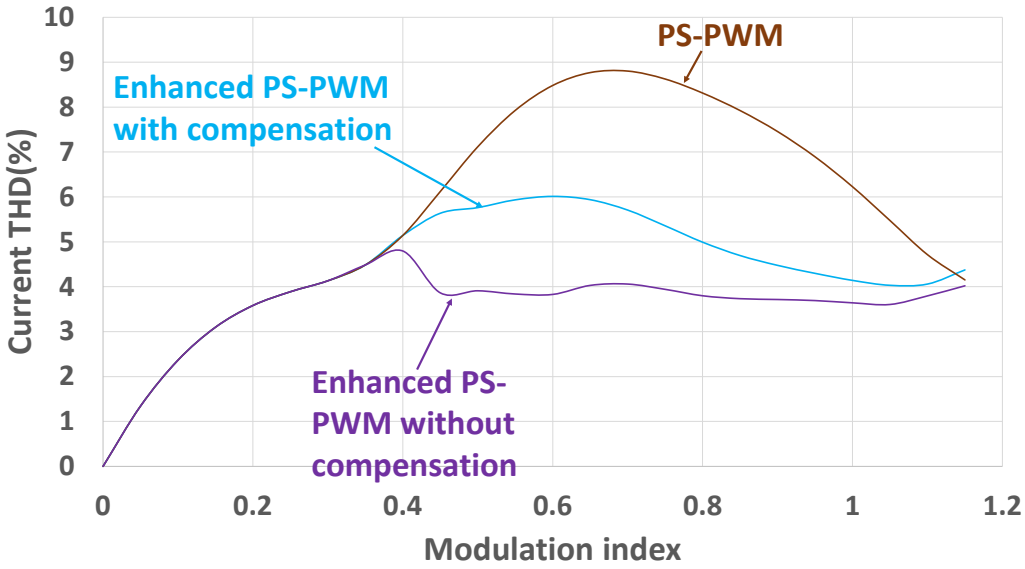


Fig. 3.7. Current THD_f (%) Performance of the VSC operating with PS-PWM, the enhanced PS-PWM (carrier swapping) with/without compensation techniques (f_1 = 60 Hz, f_{sw} = 20 kHz, L_f = 30 µH, I_{phase} = 30.6 A, Y-connected).

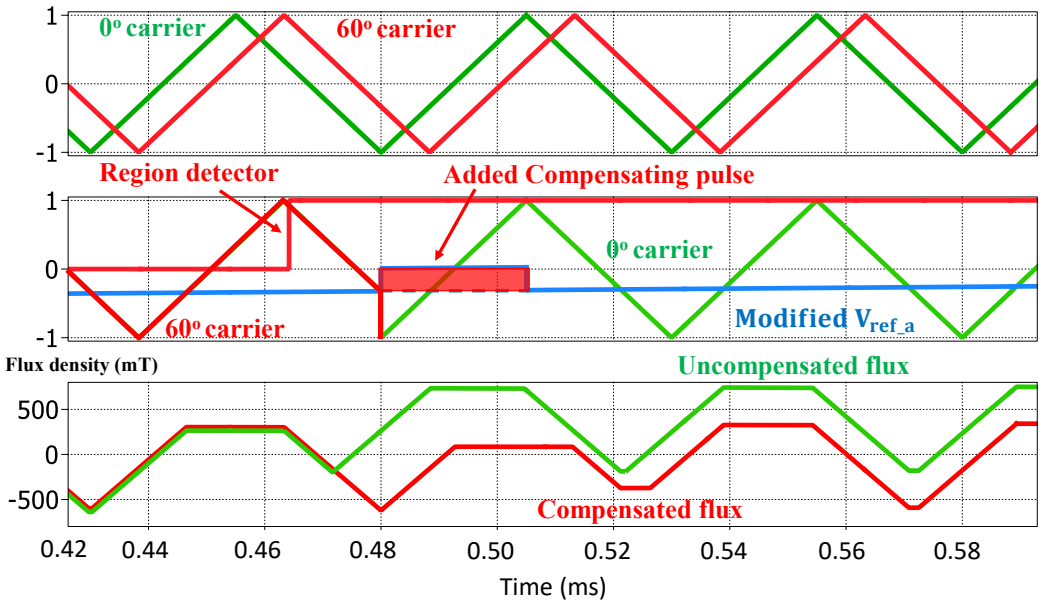
3.3. Enhanced PS-PWM (carrier swapping) with pulse injection

The pulse injection compensation technique is also designed based on the enhanced PS-PWM with carrier swapping to prevent flux jumps in the CIs. However, instead of modifying the carrier signal, this compensation technique modifies the reference signals to achieve compensating goal. The Simulation and experimental results for a three-phase 3 ILPP system are given below to verify the feasibility of the technique.

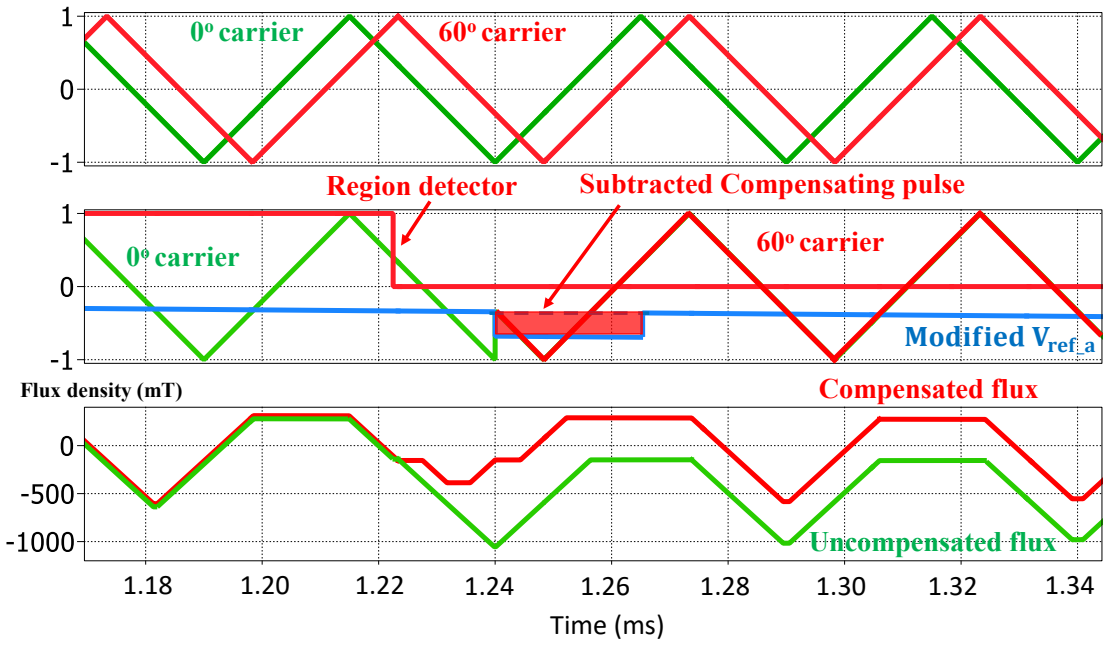
3.3.1. Technique logic details

During the region transition process of the reference signals, the compensation technique is applied to the reference signals. Instead of instantaneously changing all the phase-shifted carriers allocated to each inverter leg as the reference signal moves between the *n*-regions, the carrier change is delayed until the carriers reach their first minimum point after the region detector is triggered. In addition, a compensating pulse with an absolute magnitude of $1/n$ is added to the reference signals. The width of the compensating pulse equals half the carrier period. When the reference signals move from region 2 to the other regions, the 0^o carrier changes to the 60^o carrier when the 0^o carrier reaches the first minimum point. Likewise, the 120^o and 240^o carriers change to the 180^o and 300^o carriers when the 120^o and 240^o carriers reach their first minimum point, see Fig. 3.8 (a). When the reference signal moves into region 2, the leading carriers (60^o, 180^o, 300^o) change back to the lagging carriers (0^o, 120^o, 240^o) when the lagging carriers reach their first minimum point, see Fig. 3.8 (b). For phase A, a compensating pulse with a magnitude of 1/3 is added to the reference signals when the lagging carriers change to the leading carriers; On the other hand, a compensating pulse with a magnitude of 1/3 is subtracted from the reference whenever the leading carriers switch to the lagging carriers. The logic for phase B is inverted compared with the logic for phase A, which subtracts 1/3 pulses when lagging carriers change to the leading carriers, and adds 1/3 pulses when leading carriers change to lagging carriers. The logic for phase C is exactly the same as

phase A. The compensating pulse is injected into the reference during the change of carriers to prevent the flux in the CI's core from jumping.



(a)



(b)

Fig. 3.8. Pulse injection compensation scheme (carrier swapping) (a) reference signal moving into region 2, (c) reference signal moving out from region 2.

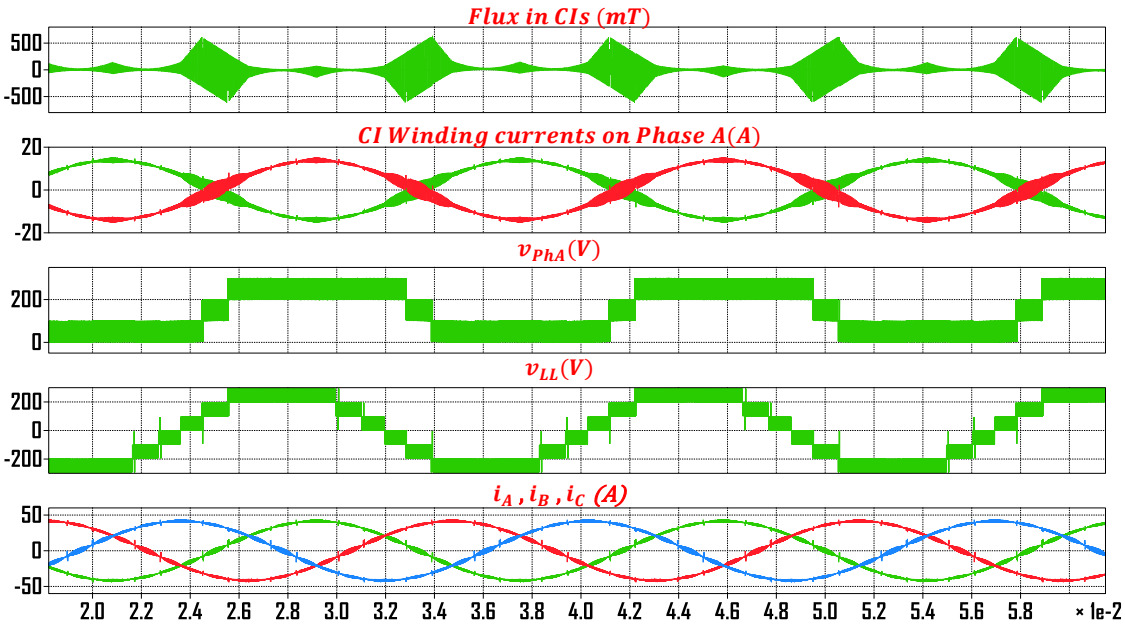
3.3.2. 3 ILPP Simulation and experimental results with performance analysis plot

The simulated CII specifications that mentioned in Table. 3.1 was chosen to approximate the results of an 11kw laboratory prototype. This compensation technique equally generates high-quality 4-level (n+1) phase and 7-level (2n+1) line PWM output voltages without any flux jump in the CIs core. The flux in the CIs, the CI winding currents (i_{a1}, i_{a2}), phase/line output voltage (v_{phA}/v_{LL}), and the load currents (i_A, i_B, i_C) are shown in Fig. 3.9. Two groups of simulation results are shown. The first group was running at f_1 = 60 Hz, L_f = 30 μH, with m_a=1.13. In addition, since this approach has the best performance at a high fundamental frequency, the high-frequency stimulation running at f_1 = 1.1 kHz, L_f = 0.2mH is presented. The harmonic volt-seconds plot of the PWM line voltages and the current THD_f(%) plot of the system are given to compare the PWM output quality, see Fig. 3.10 and Fig. 3.11. The performance plots and simulation results confirmed the feasibility of the technique.

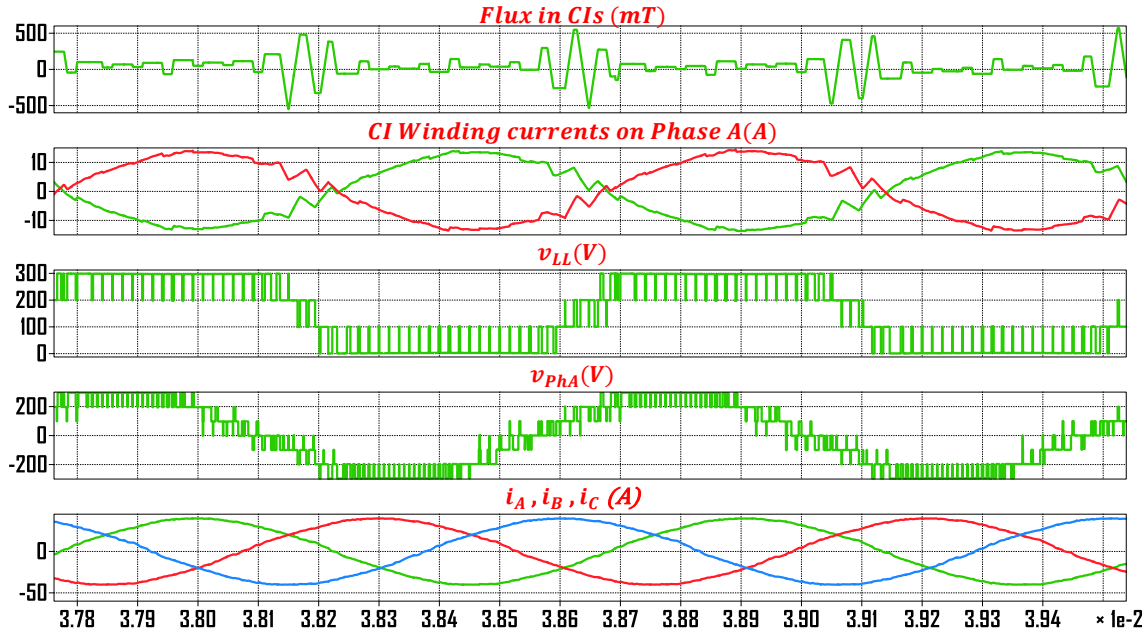
The experimental work was verified by using the laboratory prototype presented in Fig. 3.3. The parameter for the experimental work is the same as the simulation parameter to verify the feasibility in real life. Two groups of experimental results are obtained. Each group of results includes the CI winding currents (i_{a1}, i_{a2}), phase/line output voltage (v_{phA}/v_{LL}), the load currents (i_A, i_B, i_C), and the circulating currents from one inverter leg ($I_{a1,c}$). The first group ran at f_1 = 60 Hz, L_f = 30 μH, see Fig. 3.12. The second group ran at a high fundamental frequency at f_1 = 1.1 kHz, L_f = 70μH, see Fig. 3.13.

The experimental results are very similar to the simulation results. Since the flux cannot be measured directly with the scope, the flux compensation is verified by observing the waveform of the circulating current between the inverter legs. The difference between circulating currents between inverter legs is given for flux waveform validation. The waveform pattern of the circulating current is very similar to the flux pattern obtained with the simulation, see Fig. 3.9, 3.12, 3.13. This confirms that the compensation techniques successfully balance the flux in the CIs and reduce the peak

flux in the core. Additionally, we can barely observe the fundamental voltage drop effect to the flux and output voltage from the simulation and experimental results. This verifies that the CI used in this thesis has a very low series output inductance.



(a)



(b)

Fig. 3.9. The simulated waveform of a Y-connected CII (pulse injection on carrier swapping) having 3 ILPP operated at m_a = 1.13, f_{sw} = 20Hz, V_{dc} = 300V, R = 5.5Ω, and (a) f_l = 60 Hz, L_f = 30 µH (b) f_l = 1.1 kHz, L_f = 0.2 mH.

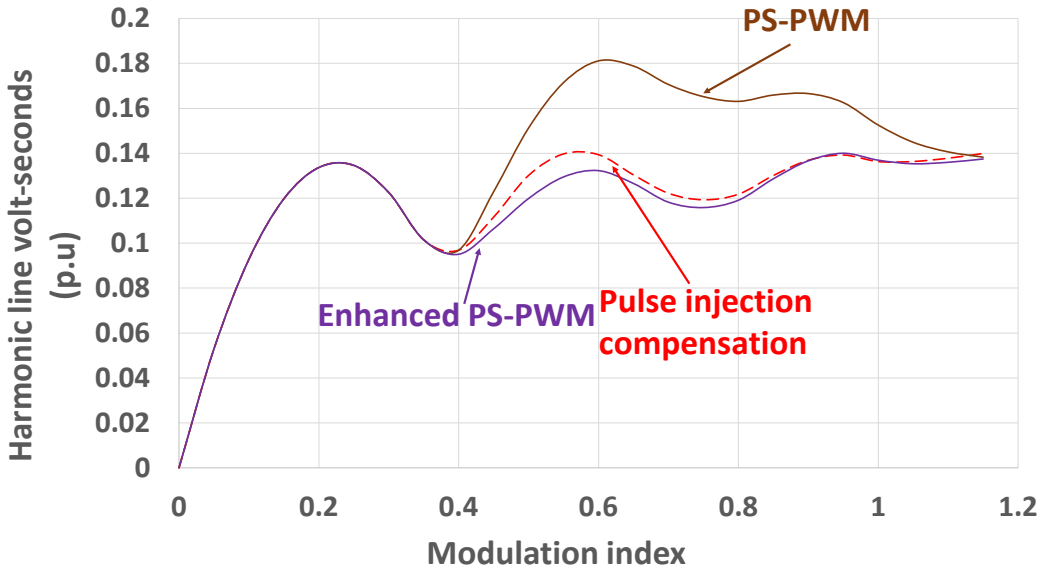


Fig. 3.10. Harmonic volt-second Performance for the VSC operating with PS-PWM, the enhanced PS-PWM (carrier swapping) with/without pulse injection compensation (f_1 = 60, f_{sw} = 20kHz, L_f = 30 µH, I_{phase} = 30.6 A, Y-connected).

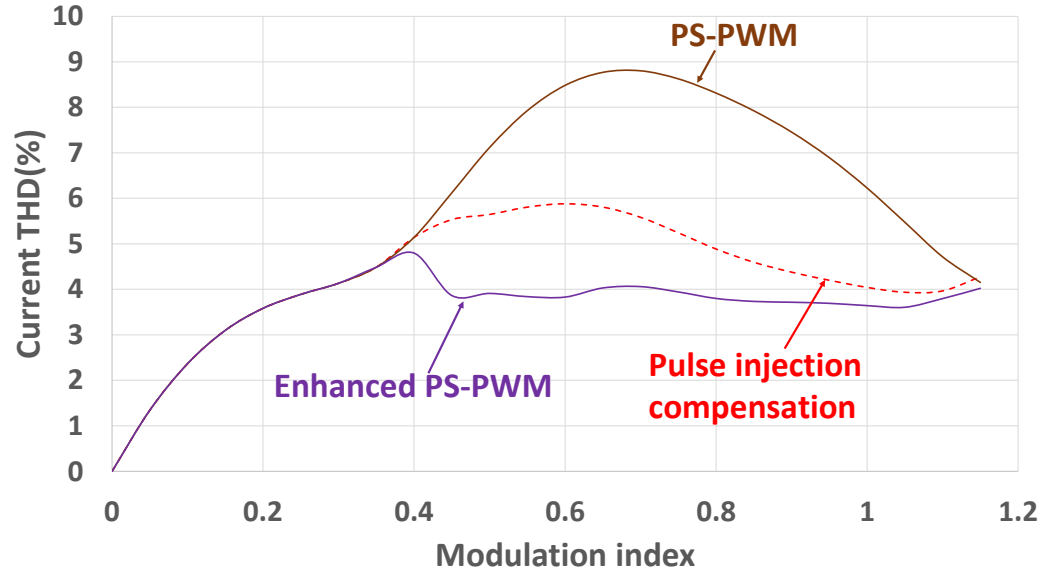
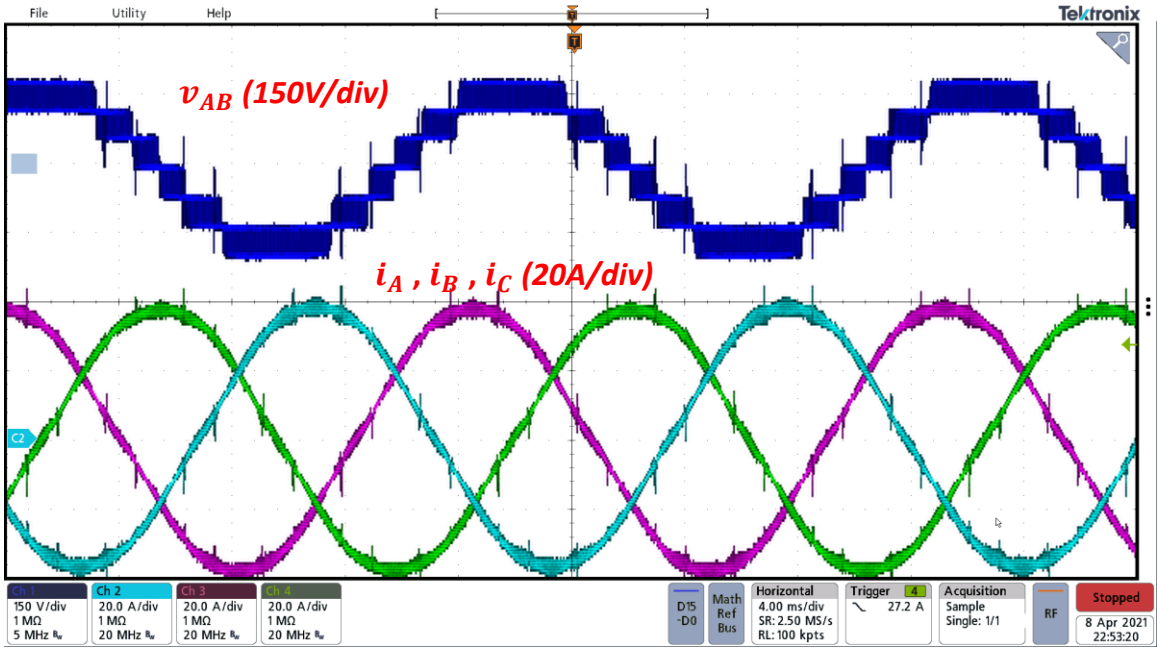
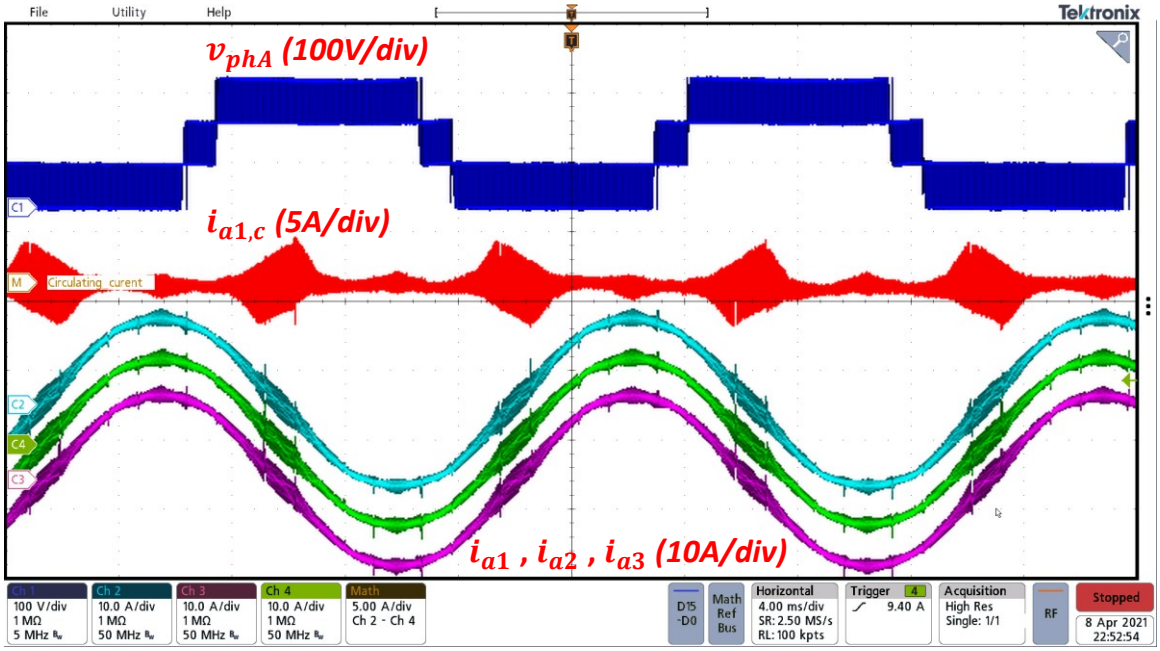


Fig. 3.11. Current THD_f (%) Performance the VSC operating with PS-PWM, the enhanced PS-PWM with (carrier swapping) with/without pulse injection compensation (f_1 = 60, f_{sw} = 20 kHz, L_f = 30 µH, I_{phase} = 30.6 A, Y-connected).

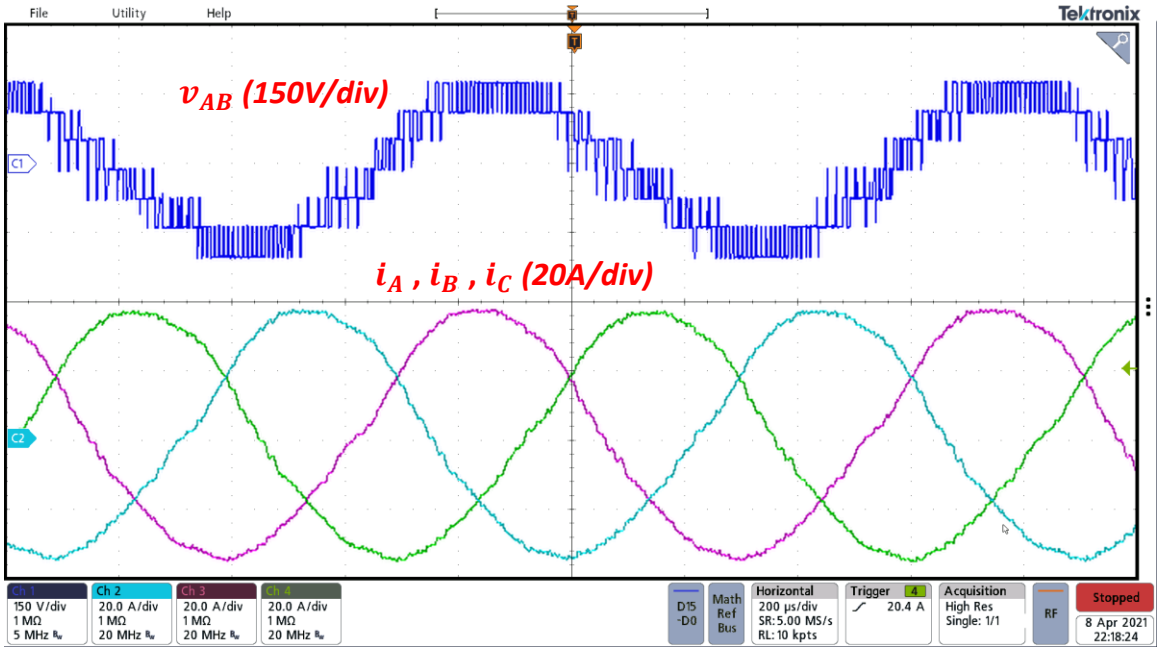


(a)

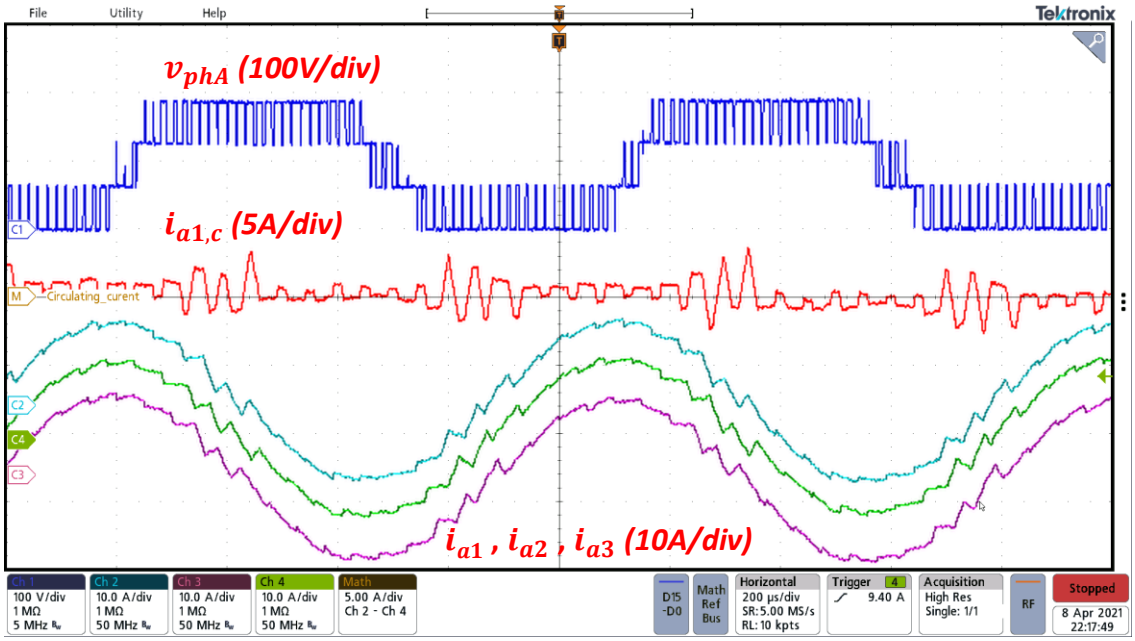


(b)

Figure. 3.12. Experimental waveforms of the laboratory prototype operating with the pulse injection compensation PWM scheme, (a) PWM line voltage and load currents, (b) PWM phase voltage, i_{cir} and CI winding currents (V_{dc} =300 V, m_a = 1.13, f_{sw} = 20 Hz, f_1 = 60 Hz, Y-connected R-L load (R = 5.5 Ω, L_f = 30 μH), L_{CI} = 0.2mH).



(a)



(b)

Figure. 3.13. Experimental waveforms of the laboratory prototype operating with the pulse injection compensation PWM scheme, (a) PWM line voltage and load currents, (b) PWM phase voltage, i_{cir} and CI winding currents (V_{dc} =300 V, m_a = 1.13, f_{sw} = 20 Hz, f_1 = 60 Hz, Y-connected R-L load (R = 5.5 Ω, L_f = 30 µH), L_{CI} = 0.2mH).

3.3.3. 2 ILPP: experimental results

Instead of 3 ILPP, 2 ILPP system is also tested experimentally for this pulse injection compensation to confirm the feasibility and the generality of the technique (Note the proposed technique can be implemented with *n* ILPP VSC). The specification of the target VSC is given in Table 3.3. Same as the 3 ILPP example, the 2 ILPP also ran experiments at f_1 = 60 Hz and 1.1 kHz with m_a=1.13. Each group of results includes the CI winding currents (i_{a1}, i_{a2}), phase/line output voltage (v_{phA}/v_{LL}), the load currents (i_A, i_B, i_C). The smooth CI winding currents confirm that flux is well balanced, Fig. 3.15 & Fig. 3.16. Again, there are a few glitches on the line voltage, but the quality of the line voltage is significantly better than the line voltage obtained from the PS-PWM scheme, see Fig. 3.14. The filter inductor used in the experiment is L_f = 0.2 mH, where this filter can lower the Current THD_f (%) to 2~3%, see Fig. 3.16 (Note this is enhanced PS-PWM (carrier swapping) with pulse injection compensation technique, the Current THD_f, and volt-sec harmonic performance curves are different compare with reference modification with flux compensation).

TABLE 3.3: VSC'S PARAMETERS FOR 2 ILPP SYSTEM

Parameters	values
V_{DC}	$300V_{DC}$
V_{Line}	$208V_{RMS}$
I_{phase}	$15A_{RMS}$
f_c	20 kHz

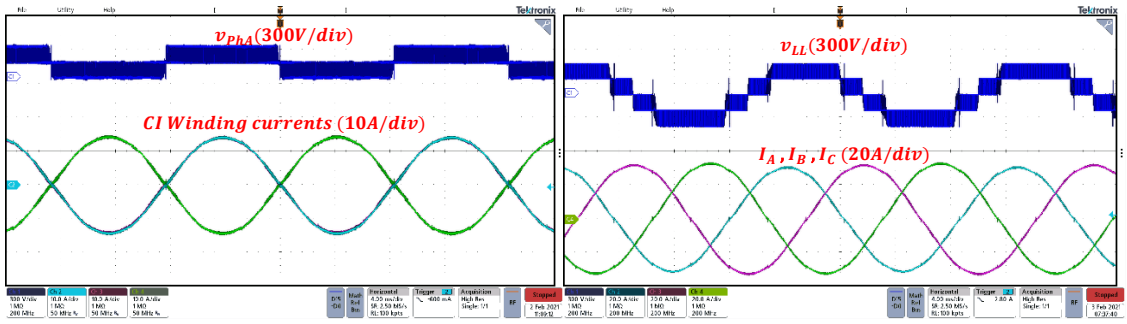
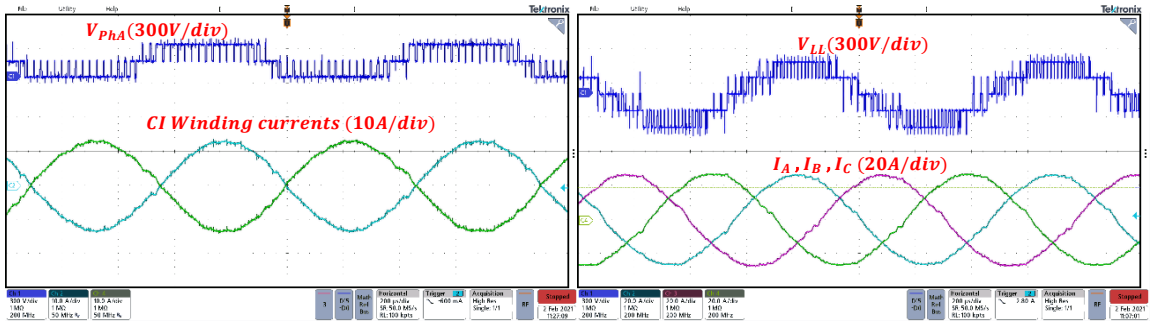


Fig. 3.14. 2 ILPP Experimental results for enhanced PS-PWM with carrier swapping and pulse injection compensation(m_a=1.13, f_1 =60Hz, Y-connected R-L load (R= 5.5 Ω, L_f = 0.2mH), L_{CI}= 0.2mH).



(c) (d)

Fig. 3.15. 2 ILPP Experimental results for enhanced PS-PWM with carrier swapping and pulse injection compensation(m_a=1.13, f_1 =1.1kHz, Y-connected R-L load (R= 5.5 Ω, L_f = 0.2mH), L_{CI}= 0.2mH).

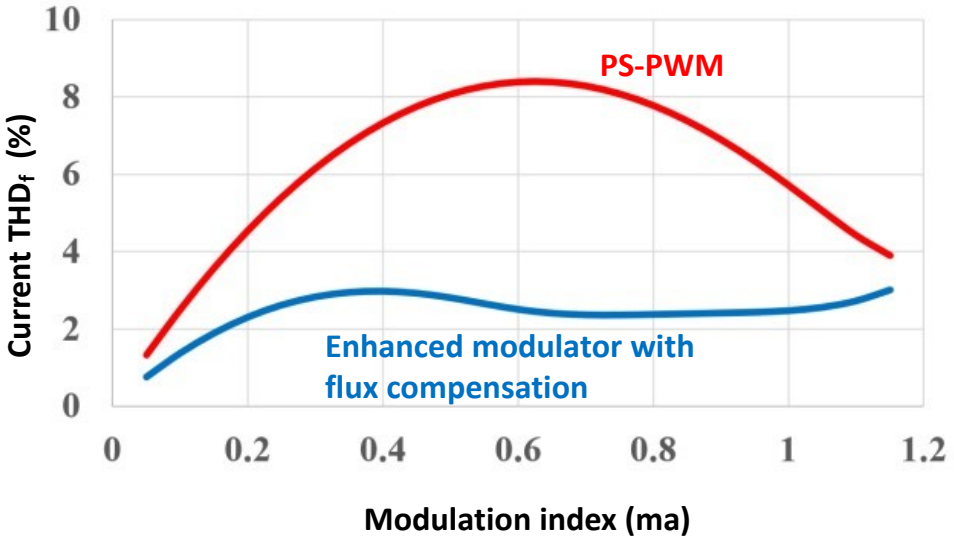
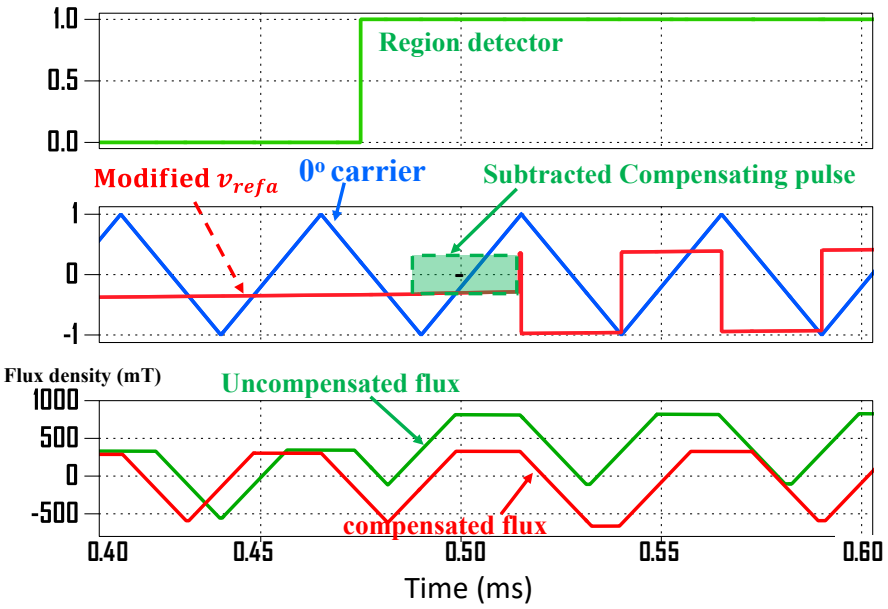


Fig. 3.16. 2 ILPP CII Current THD_f (%) of the load currents, f_1 = 60Hz, f_{sw} = 20 kHz I_{phase} = 15A, Y-connected R-L load (L_f = 0.2mH, L_{CI} = 0.2mH).

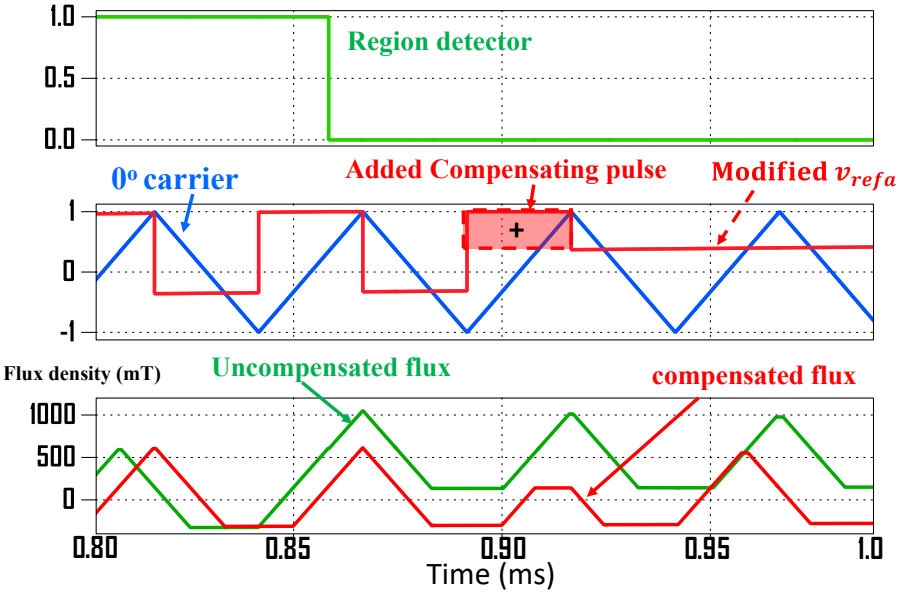
3.4. Compensation using enhanced reference modification PWM

The pulse injection compensation can also be implemented based on the enhanced PS-PWM with reference modification. The compensation logic is illustrated in Fig. 3.17 (compensating pulses are doubled, and polarity is reversed compared with the one discussed in the previous section). In addition, Fig. 3.18 compares the CI winding

currents and the high-frequency flux in the CIs when the reference modification PWM with and without pulse compensation is implemented.

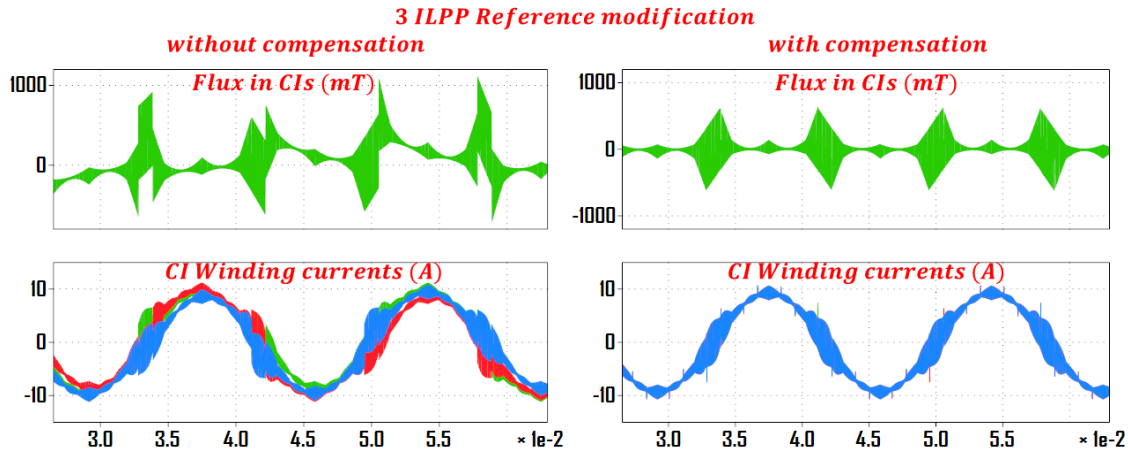


(a)



(b)

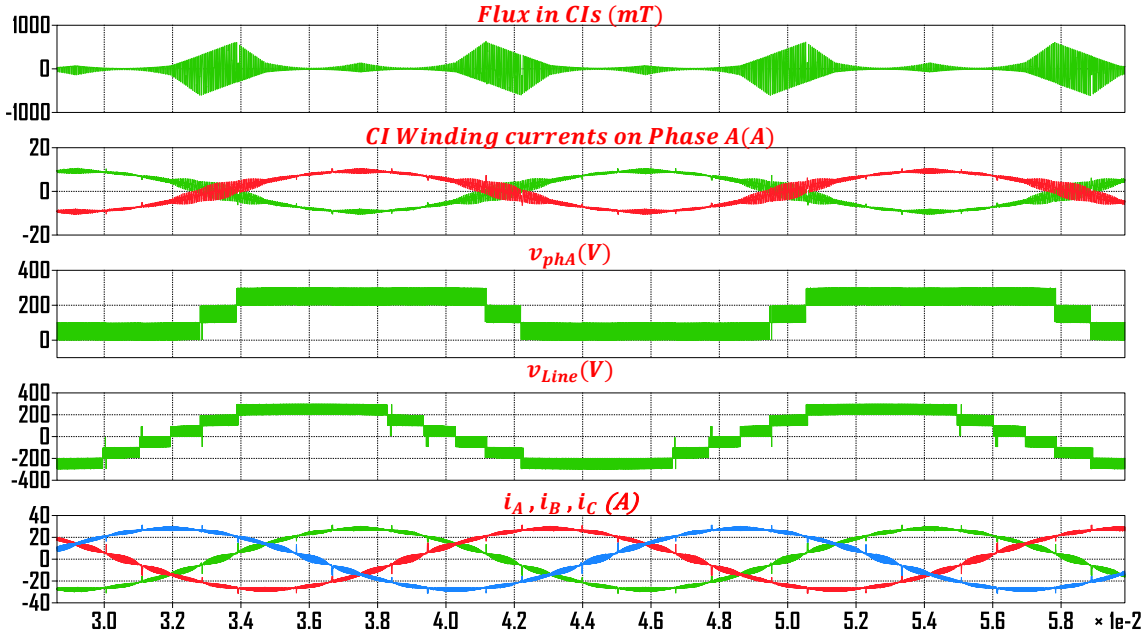
Fig. 3.17. Pulse injection compensation technique (Reference modification): (a) Transition region 3 to region 2, (b) transition from region 2 to region 1.



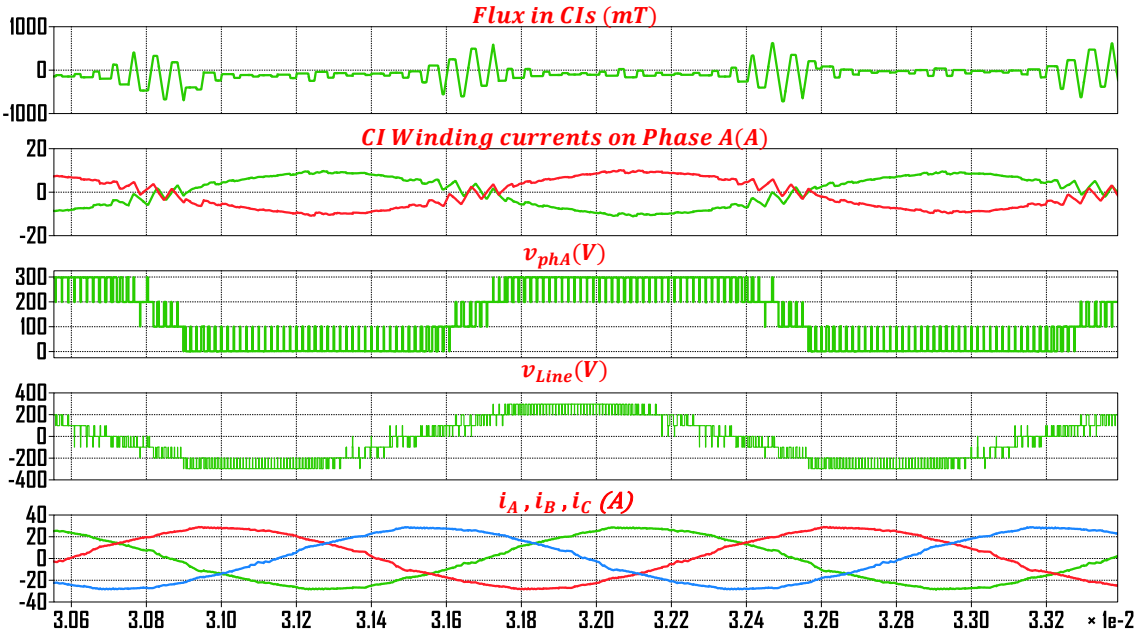
(a) (b)

Fig. 3.18. Simulated waveforms for reference modification PS-PWM: (a) Without flux compensation, (b) with flux compensation (f_{sw}= 20Hz, V_{dc} = 300V, R = 5.5Ω, f_1 = 60 Hz, and L_f = 30 μH).

For the 3ILPP test results, reference modification enhanced PWM with pulse injection compensation technique produces very similar results like those two techniques mentioned previously in this chapter when operating at a high carrier/fundamental frequency ratio (20kHz/60Hz). However, when operating at a low carrier/fundamental frequency ratio (e.g., 20kHz/1.1kHz), the number of carrier cycles in region 2 is very limited, which decreases the effectiveness of the compensation techniques and makes it difficult to balance the flux in the CIs. Consequently, 3 ILPP reference modification enhanced PWM techniques are limited to grid-connected rectifiers and low-speed drives with a high carrier/fundamental frequency ratio. Simulation results are given in Fig. 3.19, and the same experimental measurement results are given in Fig. 3.20 and Fig. 3.21 (operating at f_1 = 60Hz & 600Hz), except the flux waveform is substituted by circulating current between the parallel inverter legs (i_{cir}). In addition, the harmonic volt-seconds plot of the PWM line voltages and the current THD_f plot of the system are given to compare with reference modification without compensation and PS-PWM scheme, see Fig. 3.22.

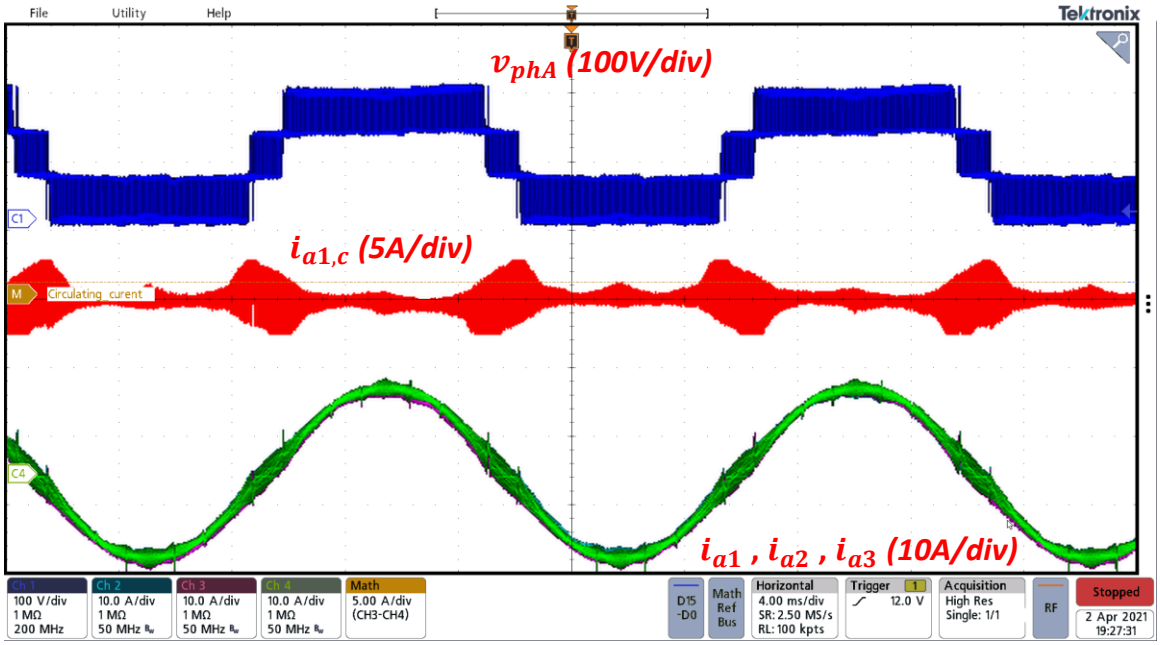


(a)

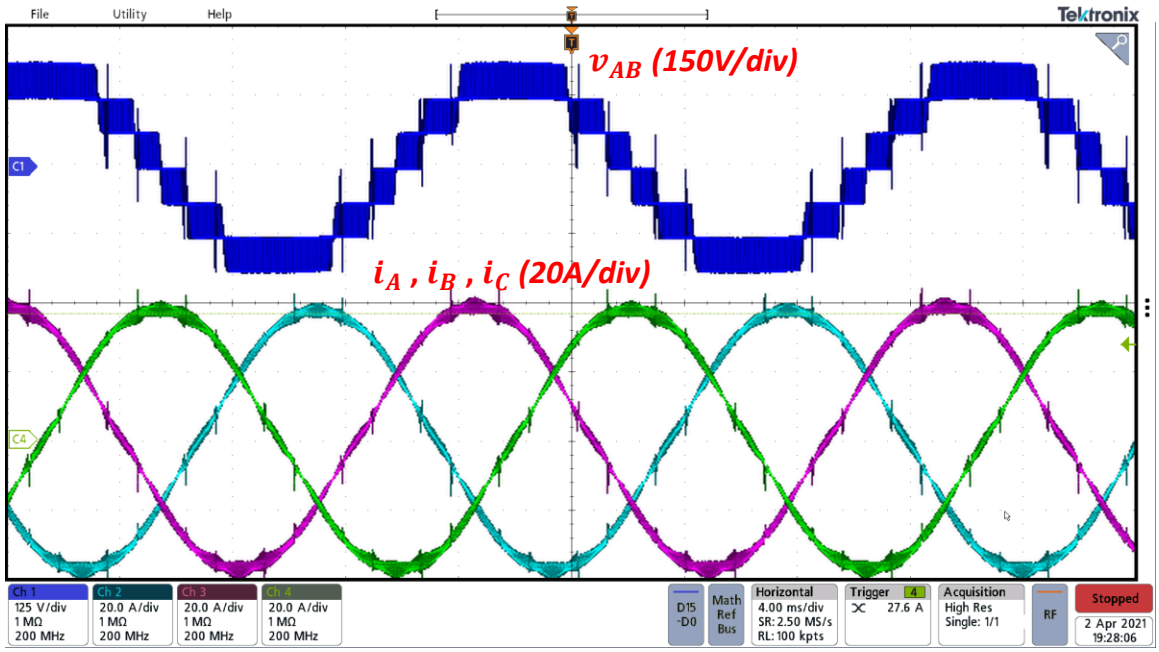


(b)

Figure. 3.19. The simulated waveforms of the Y-connected 3 ILPP (enhanced PS-PWM with reference modification) with flux compensation at f_{sw} = 20Hz, V_{dc} = 300V, R = 5.5Ω, and (a) f_l = 60 Hz, L_f = 30 μH (b) f_l = 600Hz, L_f = 0.2mH.

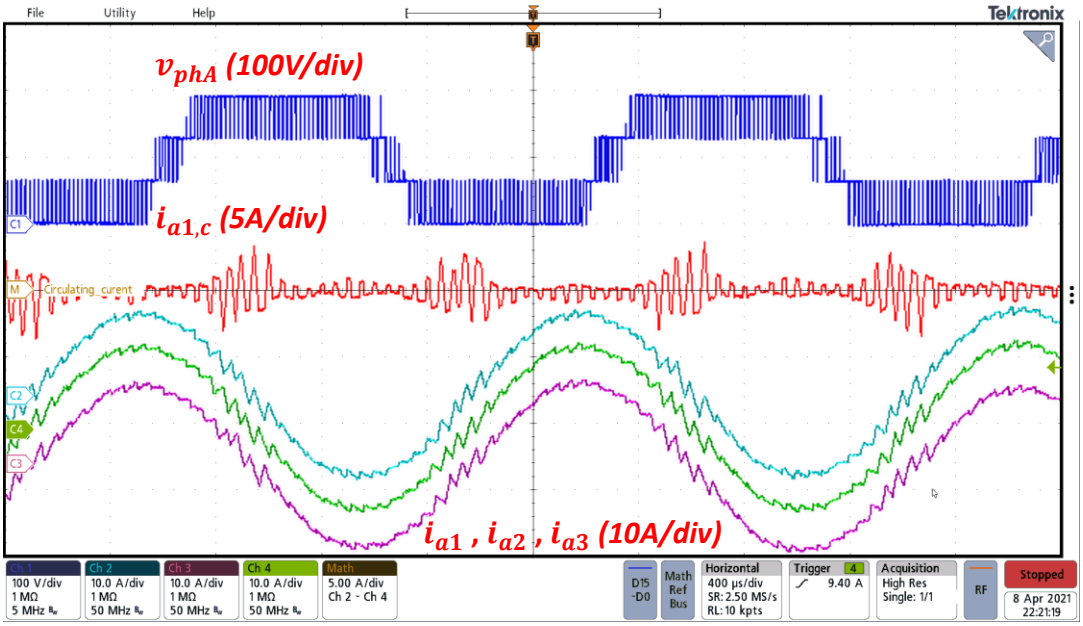


(a)

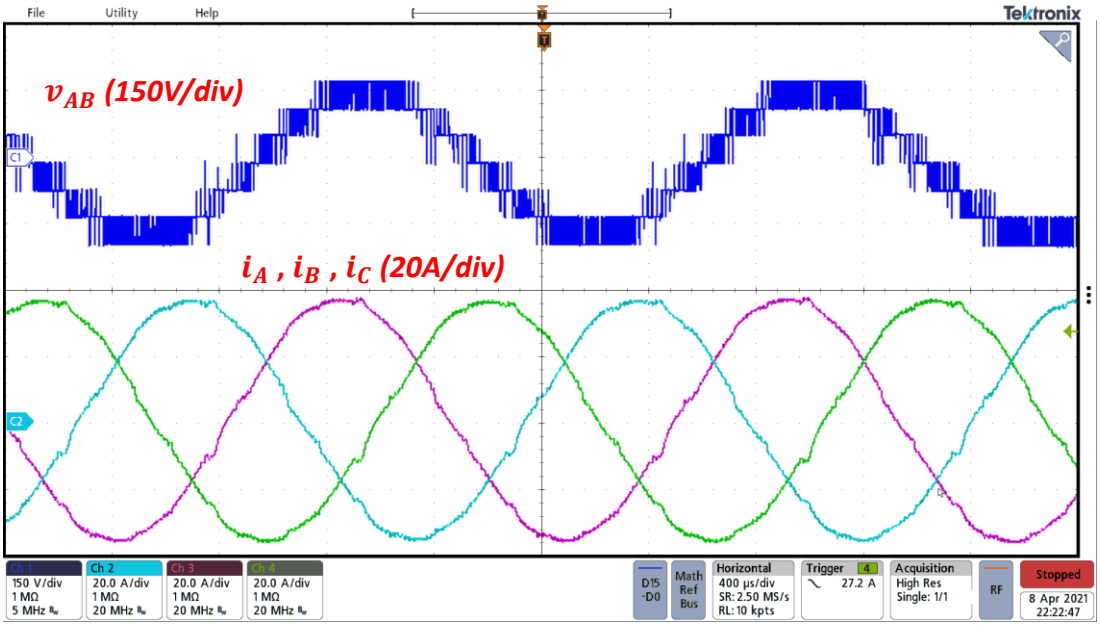


(b)

Figure. 3.20. Experimental waveforms of the 3 ILPP laboratory prototype operating with the reference modification PS-PWM with flux compensation, (a) PWM phase voltage, circulating current and CI winding currents, (b) PWM line voltage and load currents. V_{dc} = 300 V, f_{sw} = 20kHz, f_1 = 60 Hz, Y-connected R-L load (R= 5.5 Ω, L_f = 30 μH), L_{CI} = 0.2mH.

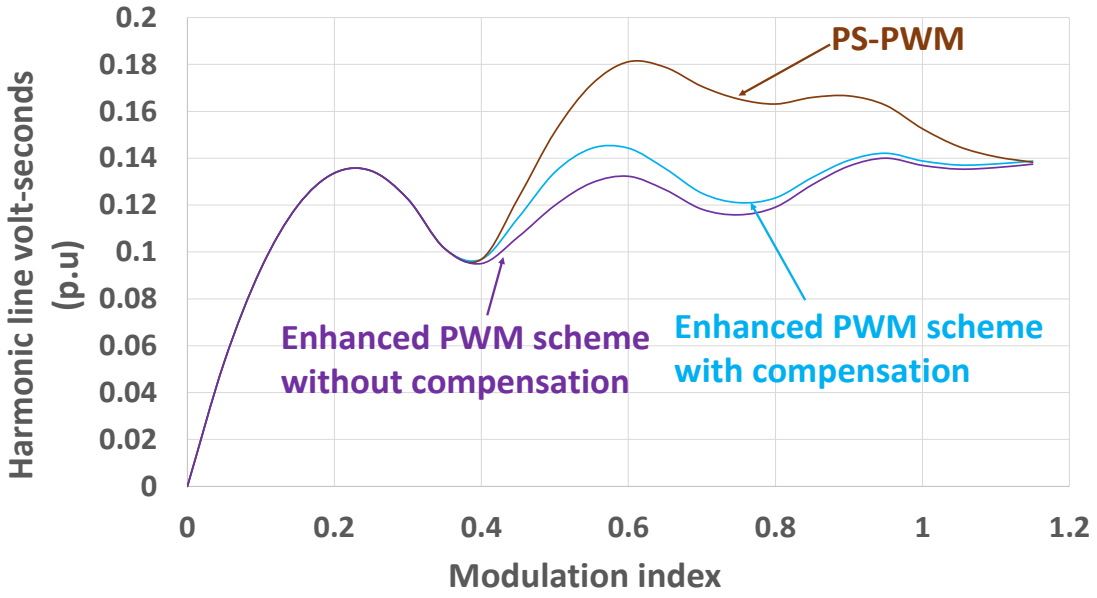


(a)

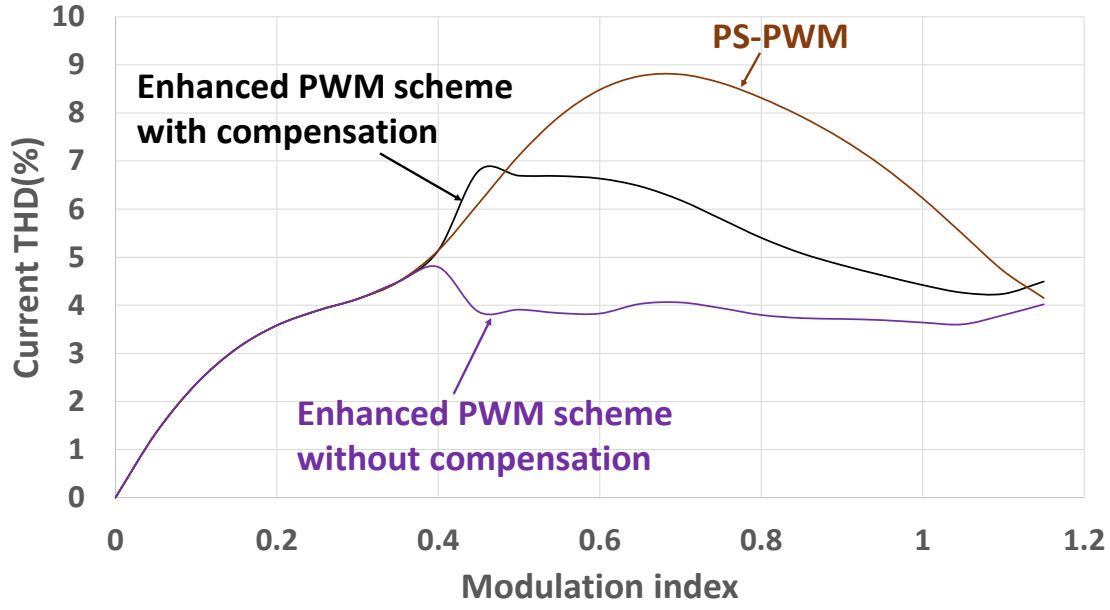


(b)

Figure. 3.21. Experimental waveforms of the 3 ILPP laboratory prototype operating with the reference modification PS-PWM with flux compensation, (a) PWM phase voltage, circulating current and CI winding currents, (b) PWM line voltage and load currents. V_{dc} = 300 V, f_{sw} = 20kHz, f_1= 600 Hz, Y-connected R-L load (R= 5.5 Ω, L_f = 70 μH), L_{CI} = 0.2mH.



(a)



(b)

Fig. 3.22. Performance of the VSC operating with PS-PWM and the enhanced PWM scheme (reference modification) with f_{sw} = 20kHz, f_1= 60 Hz, Y-connected I_{phase} = 30.6 A, L_f =30 μH : (a) Harmonic volt-second of the PWM line voltage (b) Current THD_f.

For 2 ILPP VSC, there are only two regions for the reference signal(see Fig. 2.9). This indicates that the reference modification lasts ½ of a fundamental cycle rather than 1/3 of a fundamental cycle. This increases the time length of the reference modification and flux compensation; therefore, the 2 ILPP VSC with reference modification can be used for high-speed VSC applications such as electric drive up to f_1 = 2 kHz (f_{sw} = 20 kHz). The feasibility of the 2 ILPP VSC (reference modification with flux compensation) was demonstrated with simulation and experimental results of a 10kW (208 Vac/ 28 A, 300 Vdc) laboratory prototype. The Simulation results are given in Fig. 3.23. And experimental results are given in Fig. 3.24 and Fig. 3.25 for the same measurement waveforms, except the flux waveform is substituted by circulating current between the parallel inverter legs ($i_{a1,c}$). The current THD_f(%) plot and the harmonic volt-seconds plot of the PWM line voltages are provided with a significant improvement compared with standard PS-PWM results. Due to the spikes on the line voltage, the current THD_f performance for with/without flux compensation is different, which can be explained as the price for the compensation, see Fig. 3.26 and Fig. 3.27.

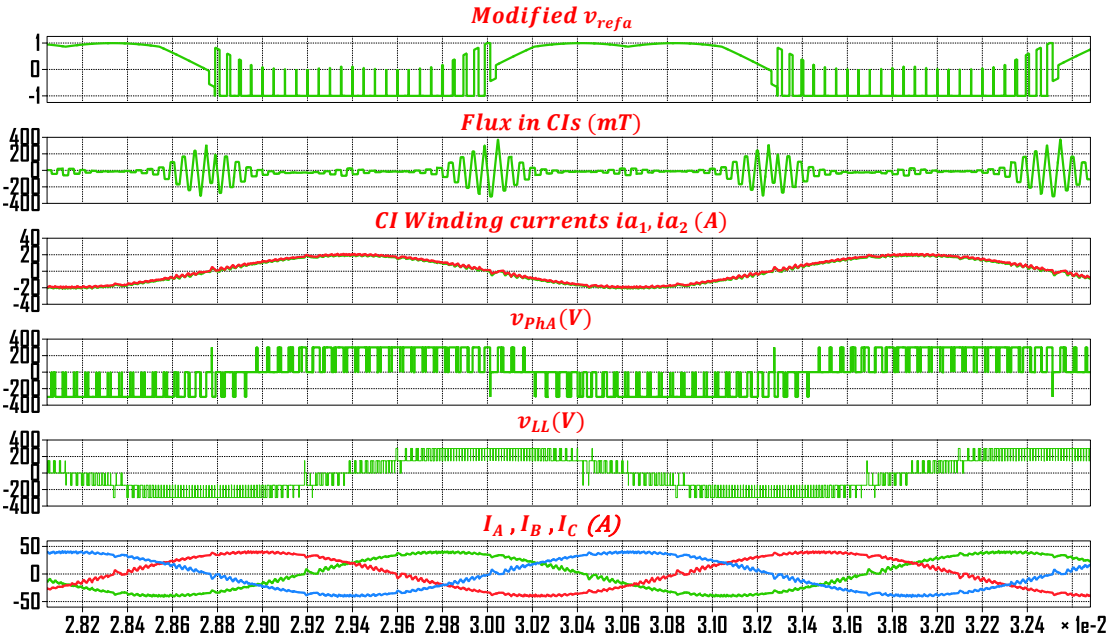


Fig. 3.23. Simulated waveform for a 2 ILPP VSC with reference modification PS-PWM, the simulation uses m_a = 1.13, V_{dc} = 300V, f_{sw} = 20kHz, f_1 = 400 Hz with a Y-connected R-L load (3.5Ω, 70uH).

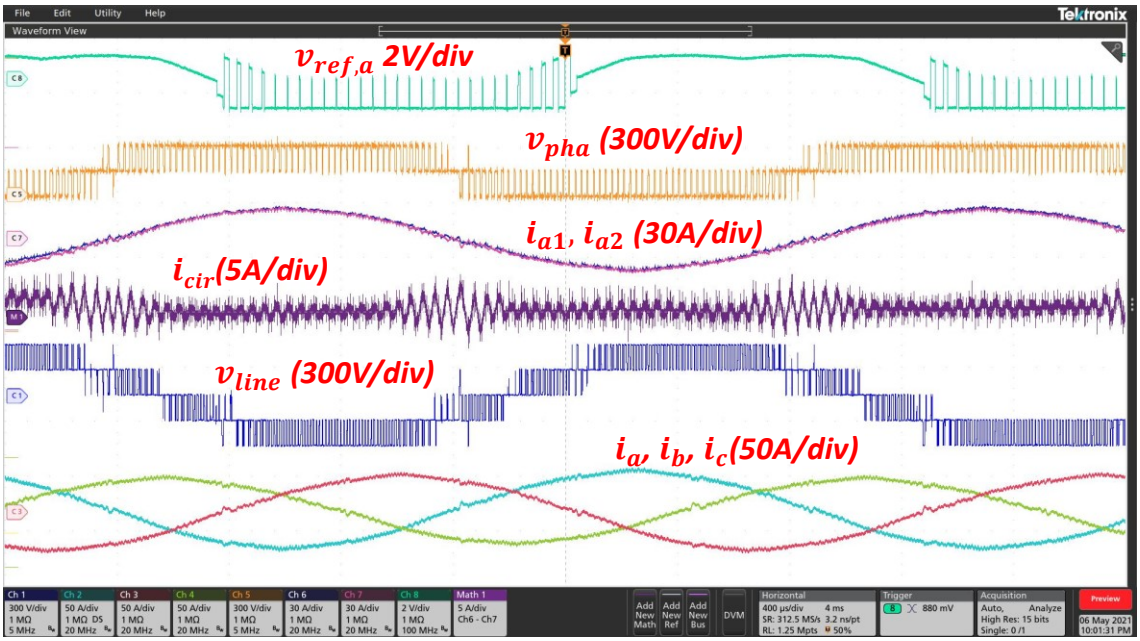


Fig. 3.24. Experimental waveforms of 2 ILPP using reference modification PS-PWM with flux compensation at m_a = 1.13, V_{dc} = 300 V, f_{sw} = 20kHz, f_1 = 400 Hz with a Y-connected R-L load (3.5Ω, 70uH).

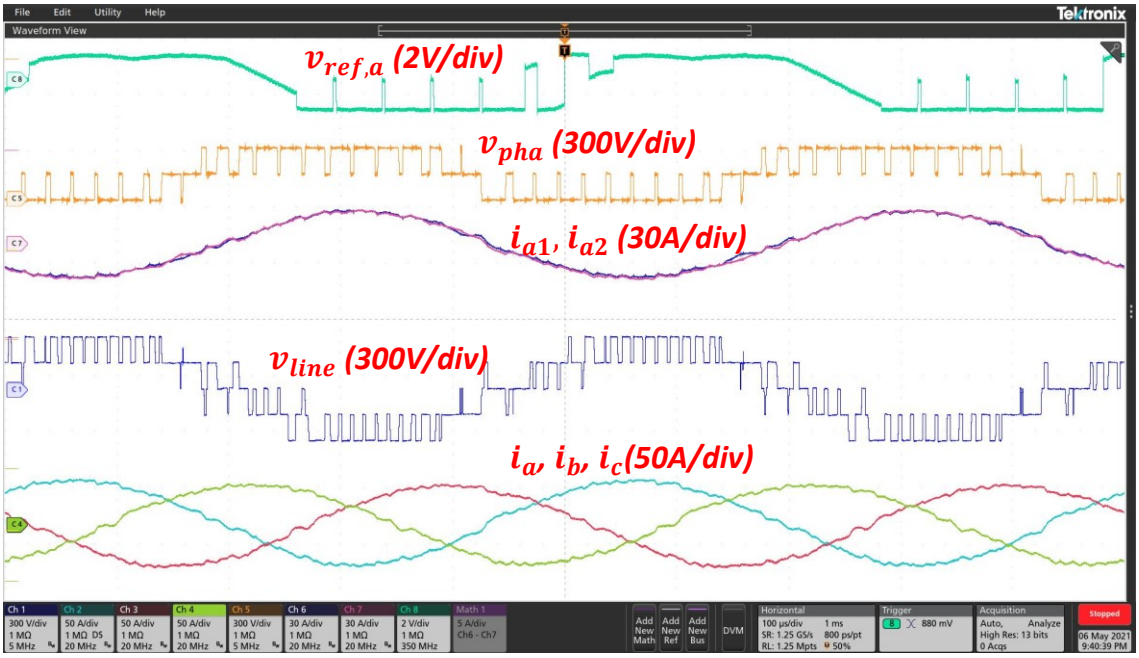


Fig. 3.25. Experimental waveforms of 2 ILPP using reference modification PS-PWM with flux compensation at m_a = 1.13, V_{dc} = 300V, f_{sw} = 20kHz, f_1 = 2kHz with a Y-connected R-L load (3.5Ω, 70uH).

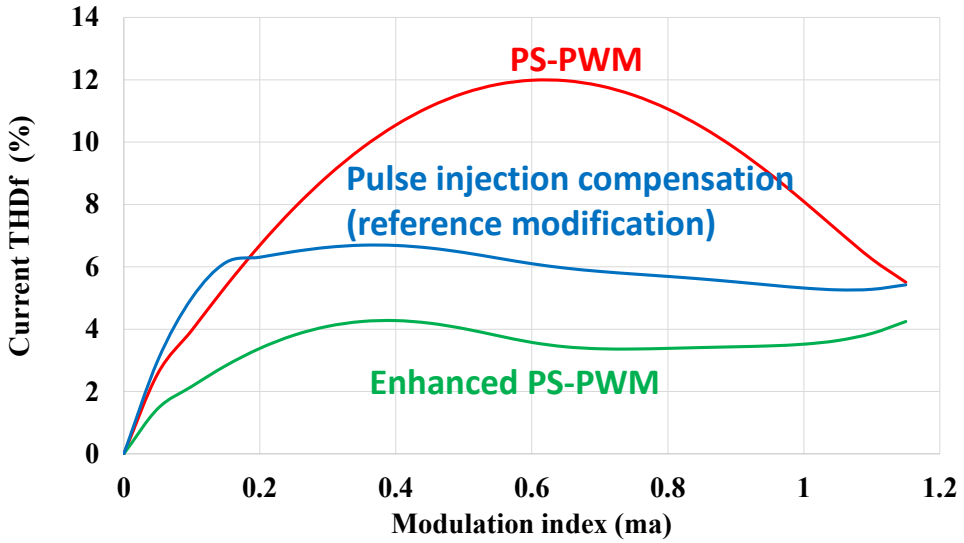


Fig. 3.26. Current THD_f(%) curves of PS-PWM, reference modification PS-PWM PWM with/without compensation, Y-connected, I_{phase} = 28 A, L_f = 70 μH.

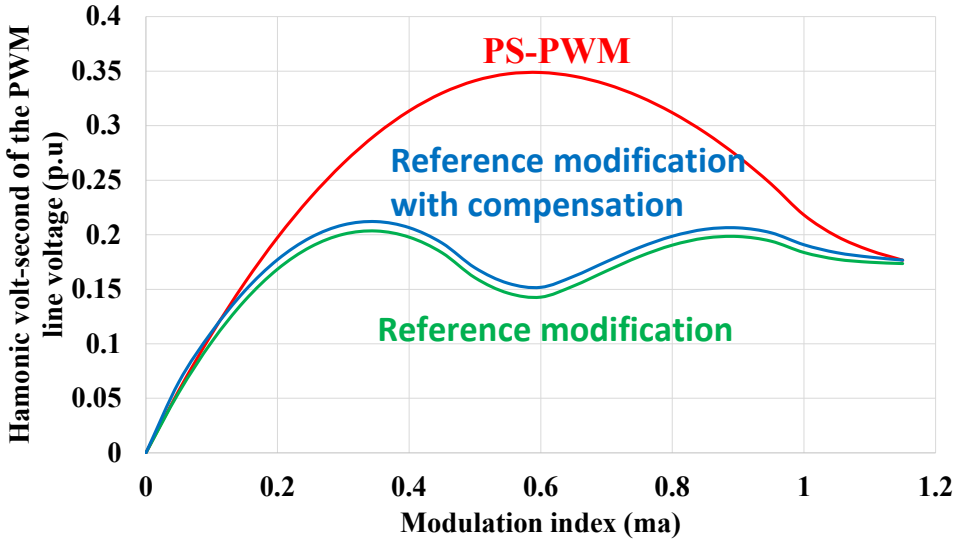


Fig. 3.27. Harmonic volt-second of v_{Line} (p.u.) curves of PS-PWM, reference modification PS-PWM with/without compensation for Harmonic volt-second of v_{Line} (p.u.), f_{sw} = 20kHz, f_1= 60 Hz Y-connected, I_{phase} = 28 A, L_f = 70 μH.

3.5. Comparison between the CII and NPC

The quality of the PWM output voltages of the CII under consideration in Fig. 2.1 is compared with a three-phase NPC converter in this section, see Table. 3.4. Both topologies have the same number of switching devices: The three-phase NPC converter has 12 switches and 6 diodes, while the CII has 18 switches. The three-phase NPC

converter generates 3-level phase and 5-level PWM line voltages with a PWM voltage step of $V_{dc}/2$ and the frequency of the PWM line voltages four times higher than the carrier frequency. However, the coupled inductor inverter (CII) generates 4-level phase and 7-level line PWM voltages with PWM voltage steps much smaller than the dc-link voltage ($V_{dc}/3$). In addition, the frequency of the PWM line voltage is six times greater than the carrier frequency. Consequently, the PWM outputs voltages of the CII can easily be filtered with a smaller filter inductor and hence reduce the size and weight of the drive magnetics.

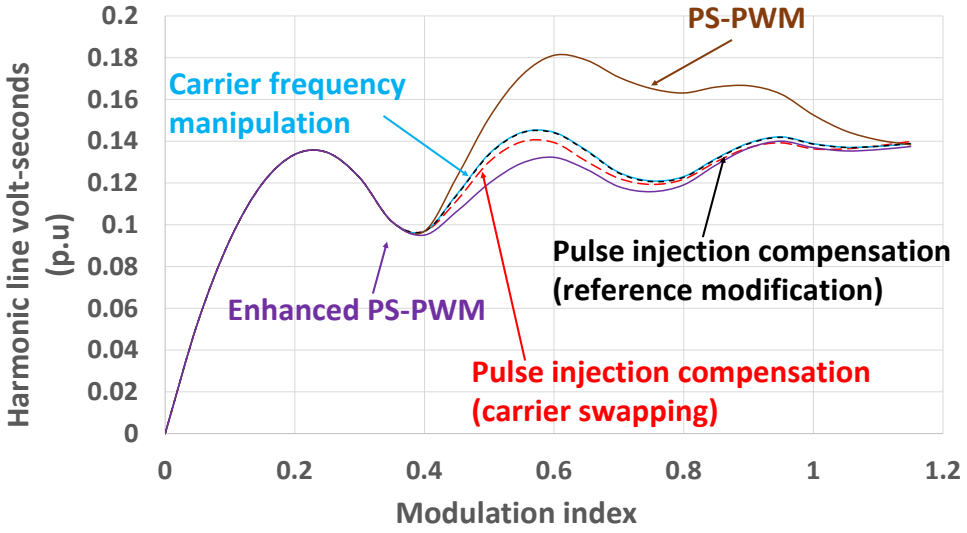
TABLE. 3.4. SPECIFICATIONS FOR NPC INVERTER AND INTERLEAVED PARALLELED CI

Parameters	**CII (18 switches)**	**NPC (12 switches + 6 diodes)**
f_{PWM}	$6*f_c$	$4*f_c$
V_{step}	$V_{dc}/3$	$V_{dc}/2$
V_{ph}	4-levels	3-levels
V_{line}	7-levels	5-levels

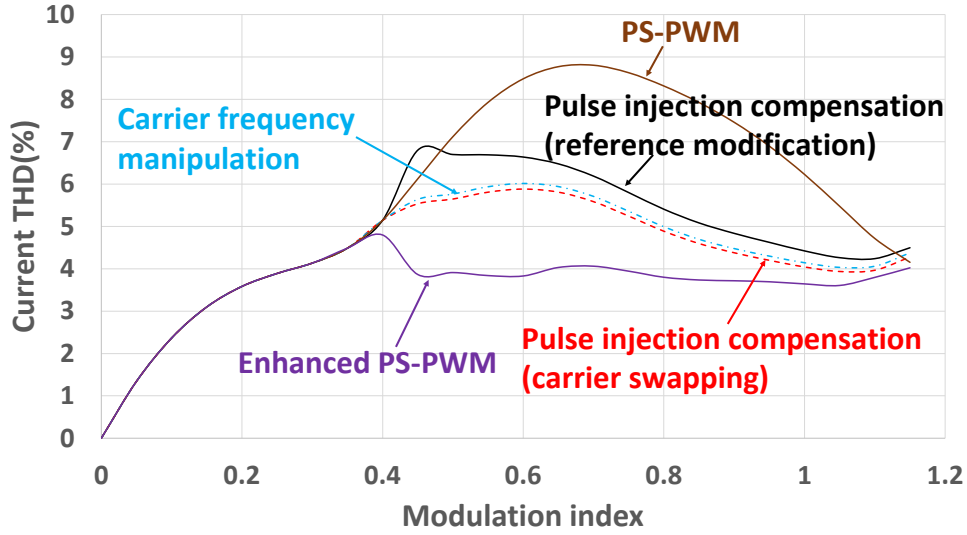
3.6. Performance curve comparative analysis

The flux compensation techniques successfully balance the flux dc offset injection based on the simulation/experimental results and performance analysis curve. The only drawback of these compensation techniques is that they produce some glitches on the PWM output voltages due to the manipulation of carrier/reference signals slightly change the switching patterns. However, these glitches have an insignificant effect on the harmonic volt-seconds of the PWM line voltages, see Fig. 3.28 (a). These glitches slightly distort the load current and increase the current THD_f (%) when compared with the enhanced PS-PWM with carrier swapping , but have significantly better performance than PS-PWM, see Fig. 3.28 (b). The current THD_f (%) of the system at high modulation indexes is controlled to be lower than 5% with a very small filter inductor (L_f = 30 μH), which is acceptable for grid-connected applications. Based on the observation from plots, the enhanced PS-PWM with carrier swapping and pulse injection compensation has the

best quality, while the reference modification enhanced PWM with pulse injection compensation has the worst performance among the three techniques. However, using reference modification avoids carrier swapping, hence eliminates complications in controlling the digital PWM modulators and eases the flux compensation control required to eliminate flux jumps. This can be beneficial for reducing the cost of the digital controller. In addition, the carrier frequency manipulation technique has moderate performance among the three, but it presents a different approach to eliminate the flux jump, which could be beneficial for some carrier-based digital controllers.



(a)



(b)

Fig. 3.28. 3 ILPP CII Performance comparison (f_{sw} = 20kHz, f_1= 60 Hz, Y-connected I_{phase} = 30.6 A, L_f =30 μH): (a) Harmonic volt-second (b) Current THD_f.

3.6. Summary and Conclusion

Flux compensation techniques are presented for CII using *n* parallel-connected inverter legs per phase with enhanced PS-PWM. Each technique has its own advantage, Table 3.5:

- Carrier frequency manipulation uses carrier swapping and carrier temporary frequency changes. This approach can work well with high fundamental frequencies.
- Pulse injection compensation (carrier swapping) has the best current THD_f performance and works well at high fundamental frequencies, but it requires modification for both carrier and reference.
- Pulse injection compensation (reference modification) only modifies the reference signals, but it does not work at high fundamental frequencies.

In conclusion, the proposed pre-processing techniques can easily be implemented with a digital controller like a DSP or FPGA without any complicated control. They can significantly reduce the peak flux in the CIs, hence reduce the size, weight, and material cost of the CIs. Meanwhile, because of the high-quality output character of the proposed PWM techniques mentioned in the previous chapter, the ac filter inductor size can be reduced. Consequently, the interleaved CII system can be built with extremely small passive components (The experimental results and performance analysis in this chapter use a 30uH small filter inductor for CII operating at f_l=60Hz).

Table. 3.5. Characteristics comparison for three compensation techniques

Technique / Characteristic	Carrier swapping with Carrier frequency manipulation	Carrier swapping with pulse injection	Reference modification with pulse injection
High-frequency operating ability (>1kHz)	√	√	×
Carrier swapping/ manipulation	√	√	×
Reference manipulation	×	√	√

Chapter 4 Discontinuous PWM with flux compensation

A PS-PWM-based DPWM controller is presented using two saturation regions of 60º. Carrier swapping within parallel-connected dual inverter legs CII is used to improve the quality of the multi-level PWM line voltages. Flux compensation techniques are applied with two aspects: first, compensation for reference signals clamping during the transitions from continuous PWM to discontinuous PWM regions; second, compensation for carrier swapping. With these two flux compensation techniques, spikes in the CIs flux patterns can be controlled. According to the DPWM peak flux information from [60], the flux magnitude is naturally low when running at a low modulation index. The technique considered focuses on the situation when using high modulation index, which is a suitable assumption when considering grid-connected applications. For verification, performance plots are presented for peak flux, harmonic volt-seconds, and Current THD (%). The feasibility of the system is verified in simulations and experimental results using a laboratory prototype with two inverter legs per phase CII circuit, see Fig. 4.1.

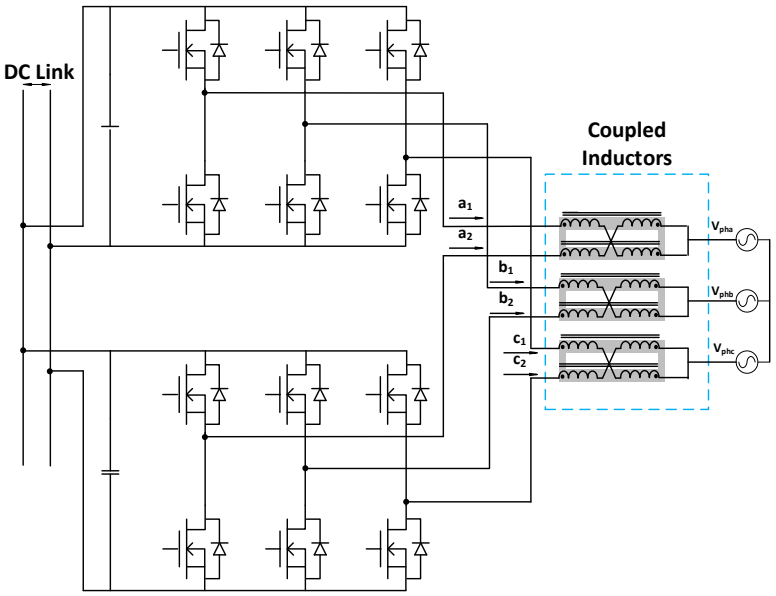


Fig. 4.1. Circuit diagram for a 2 ILPP parallel-connected inverter with crossed-coupled arrangement CIs.

4.1. Discontinuous Modulation Schemes

The principle of the DPWM is to have a 120° discontinuous period of a 360° period. Three DPWM schemes are widely used: One period of 120°, two periods of 60°, and four periods of 30°. During the transition, the reference signals suddenly jump to either positive or negative dc rails to obtain the switching discontinuity without affecting the quality of DPWM output line voltages. In this thesis, two discontinuous periods of 60° strategy with a 2 ILPP VSC is selected for explanation and presentation, see Fig. 4.2.

Three sinusoidal reference signals used in three-phase are based on the expression given in (4.1), where each of them is 120° phase-shifted:

$$v_{refA} = m_a sin\,(\omega t)$$

$$v_{refB} = m_a sin\,(\omega t - \tfrac{2\pi}{3})$$

$$v_{refC} = m_a sin\,(\omega t - \tfrac{4\pi}{3}) \qquad (4.1)$$

A common mode offset that is added to all three-phase reference signals is expressed as:

$$v_{offset} = sign(v_{max}) - v_{max} \qquad (4.2)$$

where the v_{max} in defined as:

$$v_{max} = \begin{cases} v_{refA}, & when\ |v_{refA}| \geq |v_{refB}| \& |v_{refC}| \\ v_{refB}, & when\ |v_{refB}| \geq |v_{refA}| \& |v_{refC}| \\ v_{refC}, & when\ |v_{refC}| \geq |v_{refB}| \& |v_{refA}| \end{cases} \qquad (4.3)$$

The final discontinuous reference signals can be expressed as:

$$v_{ref,DPWM} = \begin{cases} v_{refA} + v_{offset} \\ v_{refB} + v_{offset} \\ v_{refC} + v_{offset} \end{cases} \qquad (4.4)$$

This DPWM strategy allows the reference signals to have two 60° clamping periods for both positive and negative rails, which can significantly reduce the number of commutations and reduce the total switching losses, see Fig. 4.2. This chapter focuses on the compensation technique.

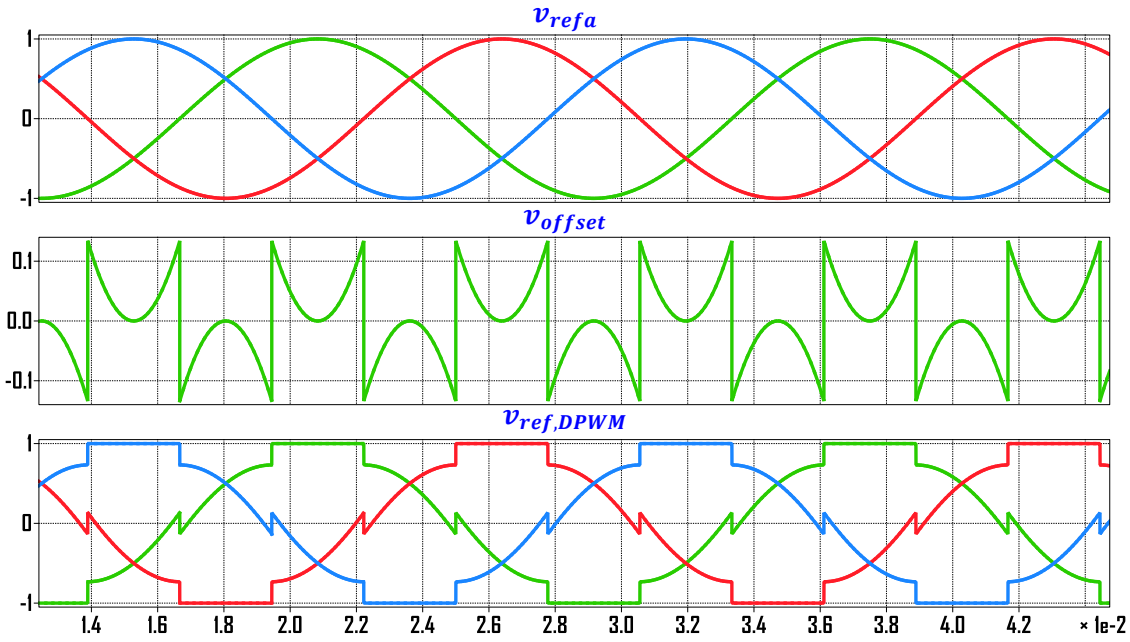


Fig. 4.2. Waveforms of DPWM with two 60° discontinuous periods

4.2. Flux jump and compensation techniques

The peak flux going through the magnetic core is one of the essential things for CI design and selection. The instantaneous carrier swapping and reference signals jump (Before and after the saturation region) changes the switching pattern for switches and injects flux jump in the CIs. To avoid undesired flux dc offset injections and reduce the peak flux, compensation techniques are designed and applied to the aforementioned DPWM strategy. The reference signals jumps are compensated by delaying the beginning and end of the reference saturation region to their first upcoming carriers' minimum point, see Fig. 4.3. There are two different cases, one is for the positive rail (+1), and one is for the negative rail (-1). By applying such a delay, the number of cycles that experience

discontinuity will be the same for all saturation periods in each inverter leg, which helps balance the dc offset injection, see Fig. 4.4.

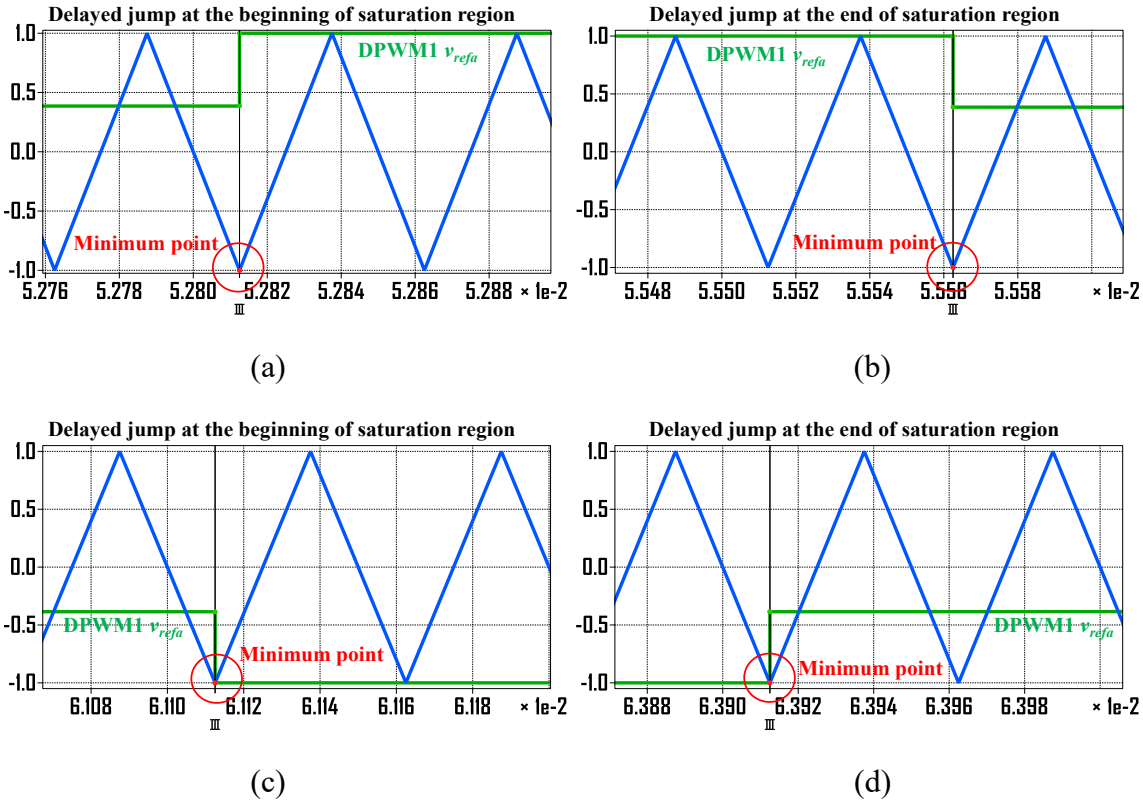


Fig. 4.3. Reference signals jump compensation logic($m_a = 0.8$). (a)&(b):Positive rail (+1) cases; (c)&(d): Negative rail (-1) cases.

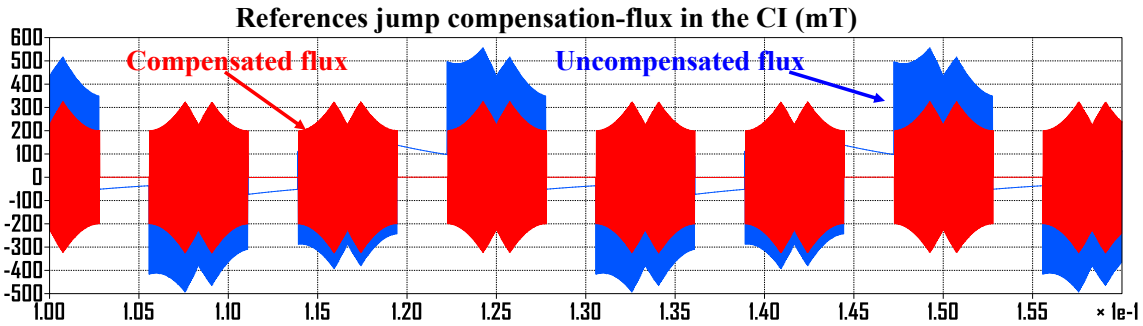


Fig. 4.4. Flux waveforms for Reference signals jump with/without compensation ($m_a = 0.8$).

The second step carrier swapping compensation logic is the same as the one described in section 3.3. Additional compensating pulses are added to reference when the first minimum point of carriers is reached (After the region detector). This helps the flux to be balanced at zero-crossings where carrier swapping is applied, see Fig. 4.5 (Note that both flux waveforms have reference jump compensation applied in this figure). In addition, both compensations applied and no compensation applied flux waveforms are given in Fig. 4.6.

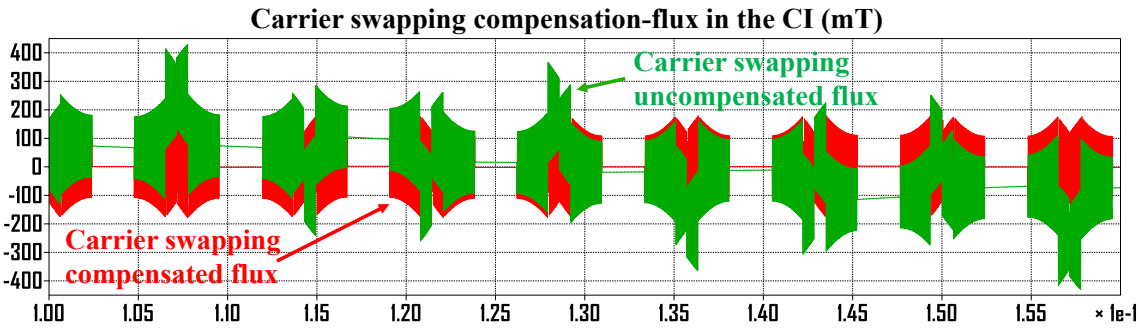


Fig. 4.5. DPWM with carrier swapping compensated/uncompensated flux waveform ($m_a = 0.8$).

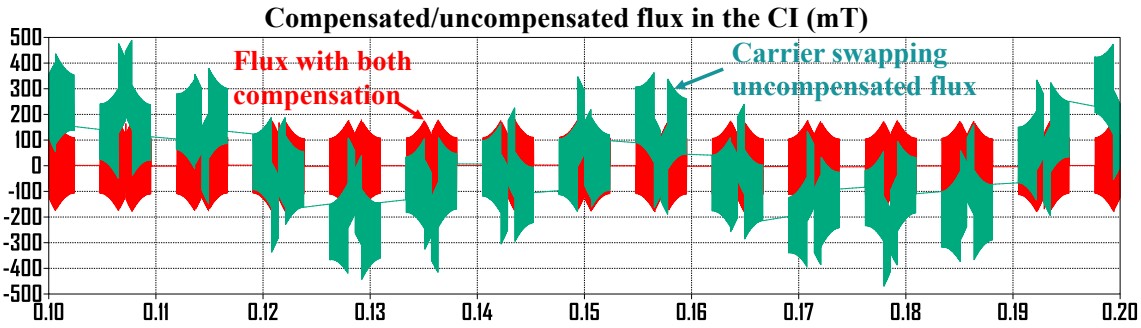


Fig. 4.6, Flux waveforms in the CI with/without both compensation (m_a=0.8).

4.3. Simulation and experimental results

The CII topology presented in Fig. 4.1 was simulated using PLECS to validate the feasibility of the proposed flux compensated DPWM. The simulation in Fig. 4.7 uses a dc-link voltage of 300V, a carrier frequency of 20 kHz, a Y-connected R-L load (3.75Ω, 0.2mH), and CIs whose parameters are summarized in Table. 4.1. Based on the

simulation work, the per-unit peak flux plot is given, where it shows the peak flux can be maximumly reduced 100% with the compensation technique; Furthermore, by using DPWM, the peak flux in the CI core is 400% less than the continuous PWM with carrier swapping and flux compensation, see Fig. 4.8. In addition, the line voltage harmonics plot is given in Fig. 4.9, where the DPWM with flux compensation has a better performance than the one without compensation. The Current THD_f (%) plot of the DPWM method is given in Fig. 4.10, where it is slightly worse than the one without compensation as the price for compensating, but it is lower than 5% and can be generally accepted in the power electronic application. The experimental results were obtained using the same parameter as the simulation, where the results behave the same as the simulation, which proves the feasibility of the proposed DPWM technique, see Fig. 4.11.

Table. 4.1. Coupled inductor parameters

Parameters	**Value**
Number of turns per windings	23 turns
Self-inductance (L_s)	0.7 mH
Effective series output inductance (L_{eq})	2.1 uH
Effective inductance between the inverter legs (L_{cir})	2.45 mH

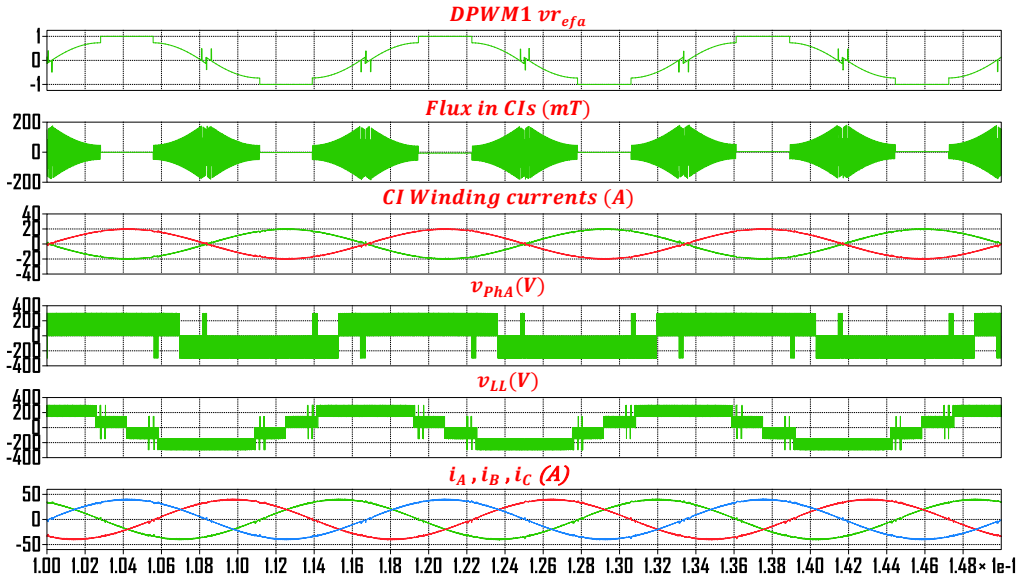


Fig. 4.7. The simulated DPWM waveform on a paralleled 2 ILPP VSC with carrier swapping and flux compensation: V_{dc} = 300V, f_{sw} = 20 kHz, f_1 = 60Hz, m_a =1, Y-connected R-L load (3.75Ω, 0.2mH).

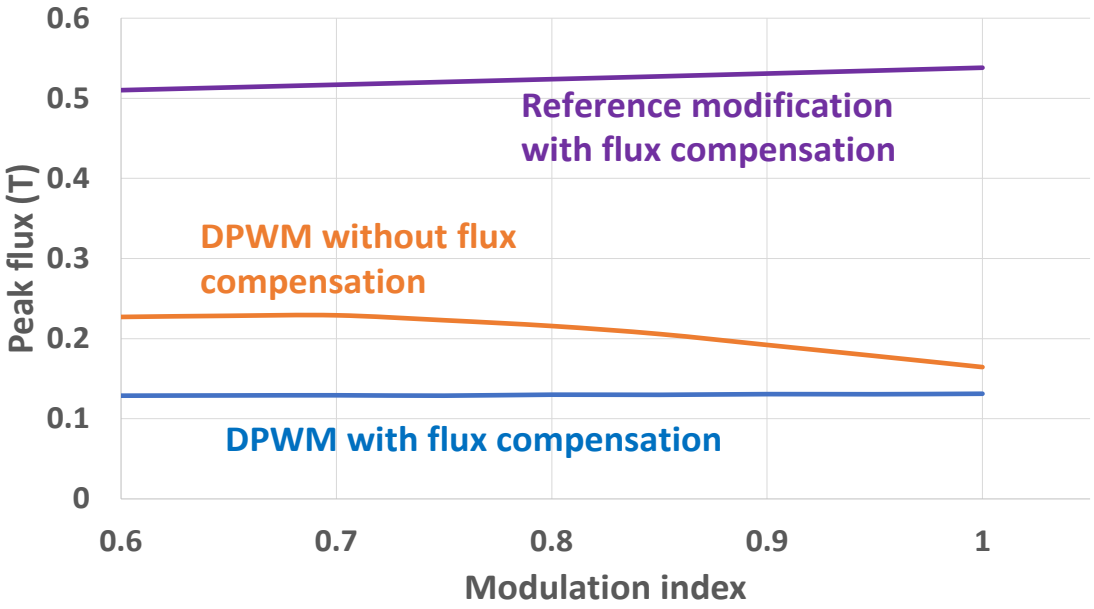


Fig. 4.8. The (p.u.) peak flux in the CIs with/without flux compensation (m_a>0.6): Y-connected, I_{phase} = 31A. L_f = 0.2mH, f_1 = 60Hz, f_{sw} = 20kHz,L_{CI} = 0.2mH.

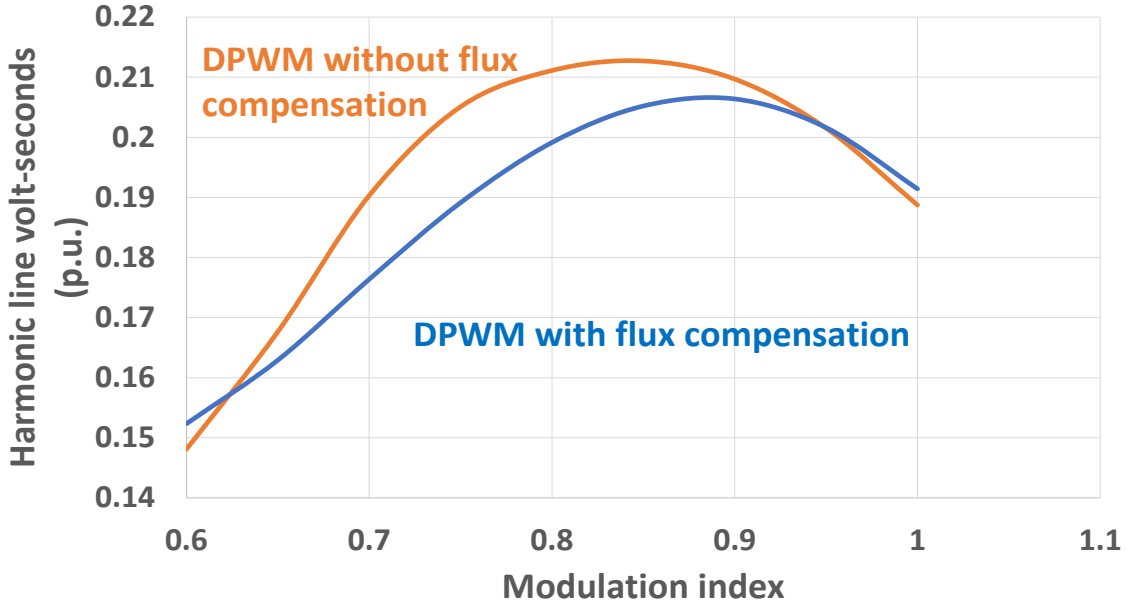


Fig. 4.9. Harmonic volt-second plot for the 2 ILPP CII operating with DPWM with/without flux compensation: Y-connected, I_{phase} = 31A. L_f = 0.2mH, f_1 = 60Hz, f_{sw} = 20kHz,L_{CI} = 0.2mH.

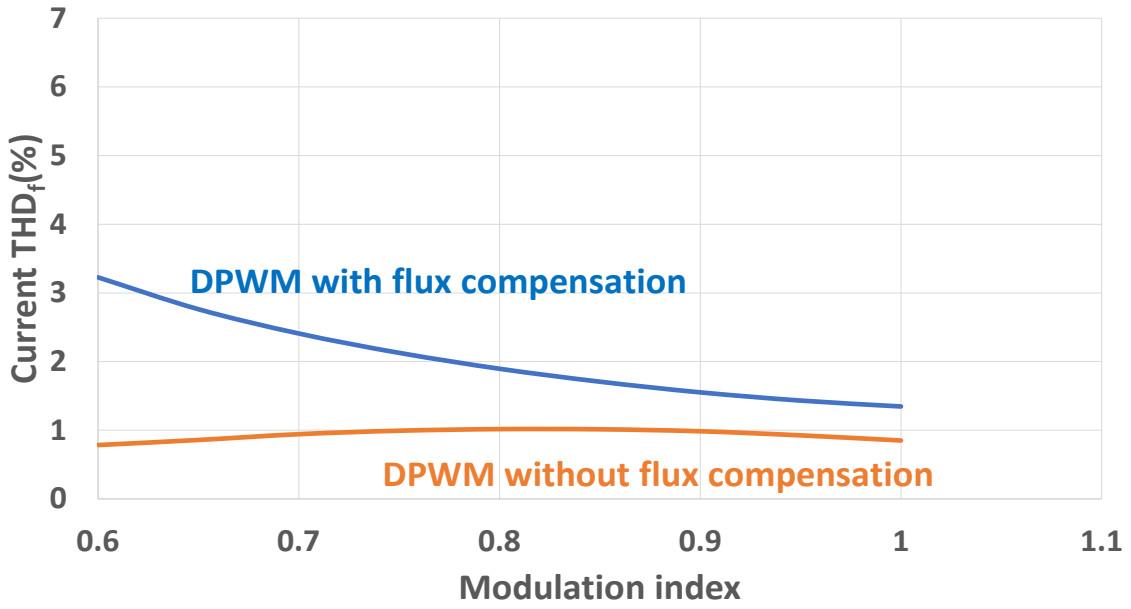


Fig. 4.10. Current THD_f (%) plot for the 2 ILPP CII operating with DPWM with/without flux compensation: Y-connected, I_{phase} = 31A. L_f = 0.2mH, f_1 = 60Hz, f_{sw} = 20kHz, L_{CI} = 0.2mH.

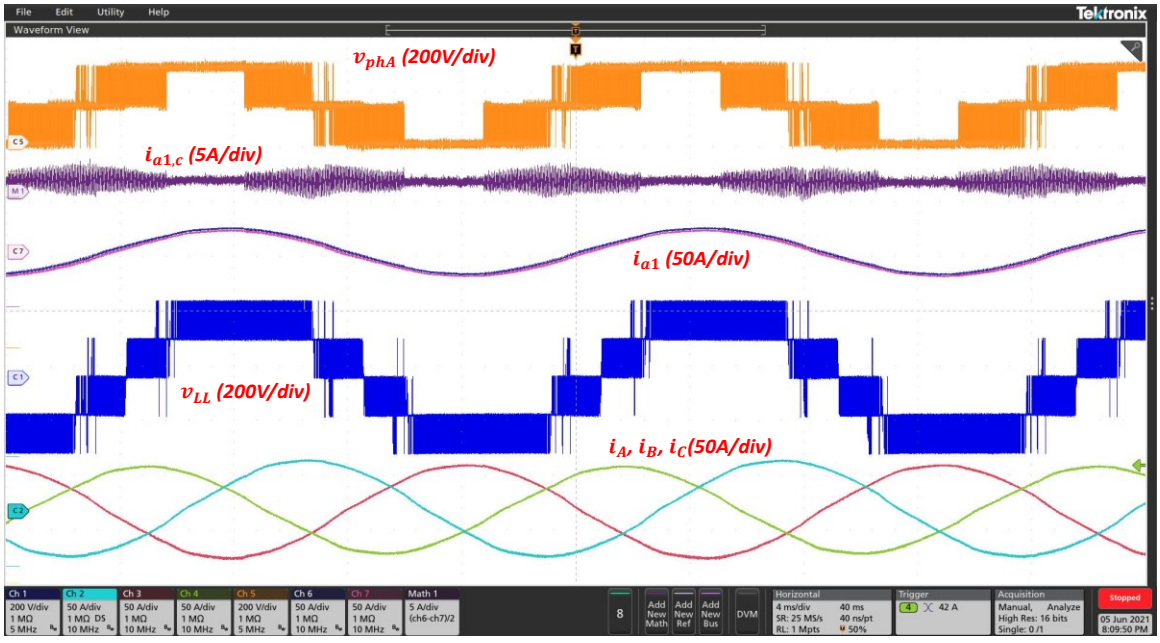


Fig. 4.11. The experimental waveform on a paralleled 2ILPP VSC (m_a = 1.13, f_1 = 60Hz, V_{dc} = 300V, f_{sw} = 20kHz, L_{CI} = 0.2mH, Y-connected R-L load (3.5Ω, 0.2mH).

4.5. Summary

A PS-DPWM controller is described for paralleled 2 ILPP CII operating at a high modulation index (m_a>0.6). Carrier swapping and flux compensation techniques are presented to obtain high-quality multi-level line voltages and controlled flux patterns in the magnetic cores. The simulation and experimental results verify the feasibility of the proposed control methods. The peak flux can be reduced by 100% relative to the uncompensated DPWM and 400% relative to using carrier swapping in PS-PWM with the same operating condition. The multi-level line voltage is improved with a slightly worse current THDf (2%) being the price for providing flux compensation. The discontinuous PWM scheme considered normally lowers the converter switching losses when connected to the utility grid application. The proposed DPWM techniques and CII topology also allow smaller gird magnetics to be used.

Chapter 5 Conclusion & Future work

A 3-phase parallel-connected multilevel voltage source converter that uses coupled inductors is discussed as the target topology. Coupled inductors with one core per inverter leg have two windings magnetically cross-coupled between two parallel paths. This results in the ac output current producing no fundamental flux in the core. The core flux consists of high frequency and is related to the switching frequency of the converters. As a result, the magnetic cores can be drastically reduced in size, weight, and material cost. The interleaved switching of parallel inverter legs in each phase results in multi-level phase output voltages with a very low series inductance related to intra-limb leakage inductance between two windings. A high inductance is experienced between the inverter legs related to the self (magnetizing) inductance of the windings. This inductance is very effective at controlling circulating currents between the parallel inverter legs. The low series output inductance, combined with the high inductance between inverter legs, allows the ac output currents to be balanced between the parallel paths.

Three main topics are presented in this thesis: (a) Enhanced interleaved PWM technique, (b) Flux compensation techniques, (c) DWPM with carrier swapping and flux compensation.

5.1. High-quality multi-level line voltages

Standard interleaved PWM switching of parallel inverter legs (PS-PWM) produces good multi-level phase but decent multi-level line voltages. The voltage steps in the phase and line voltages are less than the dc supply voltage, and the PWM frequency is larger than the switching frequency. This represents a significant improvement in the harmonic quality of the output voltages as compared with standard 2 level converters by themselves. Because the fundamental flux is canceled in the CI core, the leftover high-frequency flux in the CIs is much lower than using separate inductors in series with each inverter leg output. In addition, the cross-coupled inductor windings resulting in a low fundamental voltage drop the inductors, and more voltage can reach the load.

When using PS-PWM, the harmonic quality of the line voltages is significantly less than they could be. Techniques are therefore presented to improve the quality of the line voltages. Two PWM schemes are presented based on PS-PWM. PS-PWM using carrier swapping is shown to produce high-quality multi-level line voltages. Alternatively, PS-PWM using reference signal modification is proposed as achieving the same result. Avoiding carrier swapping is a new approach that eliminates complications in controlling the digital PWM modulators, making it easier to implement with digital controllers such as a DSP or FPGA. By using such modulation schemes, the quality of the multi-level output voltage is significantly improved compared with PS-PWM. This favors using a smaller ac filter inductor.

5.2. Anti-saturation flux compensation

Parallel inverters using coupled inductors need to be carefully designed to avoid core saturation caused by large flux jumps in the magnetic core. The flux going through the CI is determined by the switching pattern of each inverter leg, where any sudden change of the switching pattern can result in a flux jump in the CI. The switching pattern changes when the reference signals relocate to a different region for enhanced PS-PWM with carrier swapping and reference modification schemes. Such a change will cause a flux dc offset injection to the CIs, significantly increasing the peak flux. Consequently, an inductor with a larger cross-sectional area is needed to reduce the flux density, increasing the size, weight, and material cost of the overall CII system. To avoid flux jump and the problems it brings, three different pre-processing flux compensation approaches are proposed: (a) Carrier frequency manipulation, (b) Pulse injection (carrier swapping), (c) Pulse injection (reference modification). The compensation techniques eliminate the flux dc offset in the CIs, which lowers the peak flux and allows a smaller CI to be used in the VSC system. Both simulation and experimental results are used to verify the feasibility of the techniques.

5.3. Discontinuous PWM

Besides the continuous PWM techniques, research also extends to a discontinuous modulation technique modified based on DPWM with two saturations of 60^{o}. The proposed DPWM technique with carrier swapping and flux compensation can produce multilevel output voltages without flux jump in the CIs. According to the simulation and experimental results, the peak flux can be significantly reduced with better performance for line voltage harmonics. The DPWM technique focuses on high modulation index due to its low flux nature at a low modulation index. Thus it can be utilized for grid-connected applications. Additionally, its discontinuous characteristic reduces the number of commutations and therefore reduces the switching loss for VSC.

5.4. Future work

The potential future works are listed below:

1. The experimental test is not given for the carrier frequency flux compensation technique. The experimental work can be implemented by using DSP or FPGA-based controller
2. The pre-processing flux compensation techniques can be improved, where the delay time can be reduced to half the carrier cycle. With less time for the delay, the compensation logic might be a bit more complicated. However, since less delaying time, less voltage distortion will be achieved. This potential future work can reduce the number of spikes on the phase and line voltages. Therefore, the line voltage harmonics and Current THD_f (%) will be further improved.
3. Besides the carrier swapping and reference modification techniques discussed in this thesis, different PWM/DPWM logic can be designed to improve the output voltage quality.
4. The experimental work can extend to running the inverters with a high-speed machine. That will help to prove the low fundamental voltage drop benefits for the cross-coupled inductor.

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