University of Alberta

HIGH-SPEED CONFIGURABLE ANALOG BLOCK DESIGN FOR A FIELD-PROGRAMMABLE ANALOG ARRAY

by

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To my family for all their support and encouragement
and
To Linda, without you I never would have finished

Abstract

This thesis is an exploration into the design of configurable analog block (CAB) for field programmable analog arrays (FPAAs) designed in modern complementary metal-oxide-semiconductor (CMOS) technologies. Specifically, this thesis develops a single configurable analog block (CAB) using an operational transconductance amplifier (OTA). A fully differential OTA is selected for its flexibility and the reliability of differential signals with respect to noise when compared to single-ended signals. The OTA is combined with a set of switches, controlled by a serial shift register, to allow for reconfiguration of the internal wiring, and two capacitor arrays used to fine-tune the frequency response of the circuit. Simulation results are provided for an OTA, the OTA operating *in situ*, and a band-pass filter, thus demonstrating the use of the CAB. A single CAB is constructed on a 0.13 μm CMOS chip.

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List of Acronyms

ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
AP Circuits	Alberta Printed Circuits Ltd.
ASIC	Application-Specific Integrated Circuit
CAB	Configurable Analog Block
CDMA	Code Division Multiple Access
CLB	Configurable Logic Block
CMOS	Complimentary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DC	Direct Current
DIP	Dual Inline Package
DRC	Design Rule Checker
DSP	Digital Signal Processor
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EPAC	Electronically Programmable Analog Circuit
ESD	Electrostatic Discharge
ETANN	Electronically Trainable Neural Network
FM	Frequency Modulation
FPAA	Field-Programmable Analog Array
FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
HF	High Frequency
I/O	Input/Output
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ISM	Industrial, Scientific, and Medical
LSB	Least Significant Bit
LTE	Long Term Evolution
LVS	Layout Versus Schematic
MIMO	Multiple Input, Multiple Output
MSB	Most Significant Bit
NMOS	n-Channel Metal-Oxide-Semiconductor
OpAmp	Operational Amplifier

OTA	Operational Transconductance Amplifier
OTA-C	Operational Transconductance Amplifier-Capacitor
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PMOS	p-Channel Metal-Oxide-Semiconductor
RAM	Random Access Memory
RF	Radio Frequency
SC	Switched Capacitor
SDR	Software-Defined Radio
SINCGARS	Single-Channel Ground and Airborne Radio System
SPICE	Simulation Program with Integrated Circuit Emphasis
SR	Software Radio
SRAM	Static Random Access Memory
TACFIRE	Tactical Fire Direction System
TRAC	Totally Reconfigurable Analog Circuit
TSPC	True Single Phase Clocking
UHF	Ultra-High Frequency
USB	Universal Serial Bus
VHDL	Very-High-Speed Integrated Circuit Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuit
VHF	Very-High Frequency
W/L	Width-to-Length Ratio
WLAN	Wireless Local Area Network

List of Symbols

λ	Transistor channel length modulation
a	Transmission gate enable signal
A_I	Current Gain
A_v	Voltage gain
C_L	Load capacitance
g_m	Transconductance of a transistor
I	Current
I_{BIAS}	Bias current
I_D	Transistor drain current
I_{IN}	Input Current
I_{out}	Output Current
k_n	Process transconductance parameter for NMOS
k_p	Process transconductance parameter for PMOS
$k'_{n,p}$	Process transconductance parameter for either NMOS or PMOS depending on the transistor being examined.
L	Transistor length
M_n	Transistor n of a circuit
N	Number of inputs and outputs of an interconnection network
O	Complexity of an interconnection network
P	Power
r_o	Transistor output resistance
V	Voltage
$V_{B,n}$	The n bias voltage
V_{BIAS}	Bias voltage
V_d	Transistor drain voltage
V_{DD}	Source voltage
V_g	Transistor gate voltage
V_{IN}	Input voltage
V_{OD}	Overdrive voltage
V_{OUT}	Output voltage
V_s	Transistor source voltage
V_{SS}	Lowest source voltage, or ground
V_{swing}	Input swing voltage
W	Transistor width

Chapter 1

Introduction

1.1 Reconfigurable Analog circuits

Field-programmable gate arrays (FPGAs) have been commercially available since 1985 [1]. Their introduction enabled rapid prototyping and development of digital circuit designs, and more recently reconfigurable computing [2]. The FPGA has changed the design process of digital circuits by allowing designers to test and re-test designs before realizing a finished product; before FPGAs copious amounts of simulations and paper calculations were needed as well as lengthy prototyping.

Reconfigurable analog circuits similar to FPGA designs have also been attempted. In 1988 the first Field-programmable analog array (FPAA) was proposed by Sivilotti [3]. Then in 1996, IMP released the first commercially available FPAA [4]. This was a large step in analog system design. Typically analog circuits need to be custom designed, and as a result, they take a long time to develop [3]. An FPAA enables quick development of analog circuits, allowing the implementation of analog circuits in quickly developed designs.

While FPAAs would be extremely useful, their development does pose some problems. Analog circuit designers usually create analog circuits for specific applications, and generic analog circuits capable of implementing a large number

of functions are difficult to design compared to generic digital circuits. Generic analog circuits tend to be quite large; therefore, commercially developed FPAAs usually have a small number of elements, reducing the flexibility of their designs.

This thesis is interested in exploring the design of FPAAs in modern CMOS technologies that have not been previously considered, in order to see if FPAAs could become applicable to emerging applications, such as, but not limited to, software-defined radio (SDR). The main focus of this thesis will be on the design and characterization of a configurable analog block (CAB) in a 0.13um CMOS technology.

The goal of this thesis is to design and characterize some of the circuits which researchers can use in future development of FPAAs. Specifically, the design for an operational transconductance amplifier (OTA) for use in a CAB is presented with the goal of operating in the 402 to 405 MHz industrial, scientific, and medical (ISM) band. This goal is sought through the simulation of circuits and CAB designs in a standard CMOS design process. The CAB design proposed and characterized in this thesis is then used to implement other circuits, specifically a band-pass filter.

1.2 Thesis Layout

This thesis is laid out in five chapters. The first chapter is the introduction, and introduces the topic examined in this thesis. The second chapter provides the reader with background information on analog circuits, FPAAs, SDR, and the

work proposed in this thesis. Chapter 3 describes the circuits and their design used in the design of the CAB. Testing and implementation are presented in the fourth chapter, including the testing setup and the results from testing. Finally, chapter five concludes the thesis and presents an interpretation of the results, future work, and the uses of the proposed design.

Chapter 2

Field-Programmable Analog Arrays and Related Circuits

2.1 Analog Complimentary Metal-Oxide-Semiconductor Circuits

Natural signals are inherently analog [5]. To process natural signals, sensors, often constructed with analog circuits, are used to interpret the natural signal and convert it into an electrical signal which can be processed. In general much of the processing of signals is done in the digital domain; however, many signals require some analog processing before converting them into digital signals and processing them with a digital signal processor (DSP) [6].

Digital communications require some use of analog systems for transmission [6]. If transmission distance is long enough, then distortion often occurs in the signal. Using a multilevel system to transmit the digital signal reduces the required bandwidth and offers some improvement to the signal quality. Incorporating a multi-level system requires the use of ADCs and digital-to-analog converters (DACs). ADCs and DACs naturally require the use of analog circuits in their design.

Radio frequency (RF) signals operate at very high frequencies, often in the GHz range [7]. RF communication signals need to be translated into digital signals using analog circuits. In addition, other RF signals being transmitted over the

same medium often interfere with the desired signal. To provide the necessary amplification, frequency, and noise immunity analog circuits need to be used [6].

There is a multi-dimensional design trade-off in analog circuits [6]. For instance, improving the speed of an analog circuit can limit the performance of power, gain, precision, voltage supply, and many other parameters. In digital circuitry there is generally a trade-off between speed and power [6]. The interdependency of the various parameters of analog circuits often means that automating the process of designing and creating analog circuits is not easy. As a result, most analog designers create analog circuits from the ground up, leading to longer development time and a higher cost for the research and development of analog circuits when compared to digital circuits.

The cost of analog circuits is also limited to the simulation technology that exists for analog circuits. Analog simulations are often inaccurate and problematic compared to their digital counterparts due to the large number of effects that must be simulated. Often it is not known whether a circuit will work until after it has been built. This can lead to increased costs in developing multiple versions of chips before a working prototype is made.

One possible solution to the cost and development time problems of analog circuits is the development of an FPAA. An FPAA is conceptually similar to an FPGA that is used to prototype, test, and develop digital circuitry. The FPGA

provides an array of configurable logic blocks (CLBs), which are connected together with programmable interconnections [8]. The reconfigurable architecture allows for quick, inexpensive prototyping, which in turn makes the FPGA invaluable in the testing and prototyping of digital circuitry design.

2.2 Field-Programmable Analog Arrays

The FPAA was originally conceived to rapidly prototype analog circuits [3], much like FPGAs in the context of digital systems. A few FPAAs have been developed commercially [9] [10] [11]. However, these FPAAs tend to be limited in their applications. Lattice Semiconductor used to offer the ispPAC series of FPAAs, which perform signal processing and conditioning [11] [12]. The Lattice design has four instrumentation amplifiers and two DACs, allowing the ispPAC to implement amplifiers, filters, integrators, or comparators. A linear or biquadratic filter can be programmed on the ispPAC circuits without any external components, and other analog systems such as a temperature control system or a bridge sensor interface are implemented with some external circuitry [13]. However, in 2007 Lattice discontinued the ispPAC series of FPAAs, and consequently they are currently unavailable [14]. Lattice does offer a series of programmable power supplies, which do offer some programmability of the analog components [15]; however, this programmability is limited to control of comparators and does not use an FPAA.

Zetex created the totally reconfigurable analog circuit (TRAC) design implemented in bipolar technology, which is more expensive than complimentary

metal-oxide-semiconductor (CMOS) [11] [12]. The TRAC design operates in continuous time, like the ispPAC, but in the log domain, and can operate up to 12 MHz. 20 CABs in two rows of 10, make up the TRAC design. A CAB is the basic building block of an FPAA, and in the TRAC design each of the CABs can perform log, anti-log, non-inverting pass, addition, negating pass, operational amplifier (OpAmp), and half-wave rectification functions. One of the serious drawbacks to the TRAC design is that most of the interconnections between CABs need to be wired externally, rather than programming them on the chip, as with the ispPAC [11] [12].

The Motorola MPAA020 FPAA design uses switched capacitors, and contains 20 switched capacitor (SC) cells [11] [16]. There are many techniques available for SC designs that limit the effect of parasitics, allowing for minimal signal loss on arbitrary routing paths. The switched capacitor design allows for a larger variety of circuits to be implemented than the Lattice device, but a discrete time analog design, resulting from the use of switched capacitor circuits, limits the bandwidth of the circuits implemented on the FPAA [13] [17].

IMP developed the electronically programmable analog circuit (EPAC) in 1996 [4]. The EPAC device was designed specifically for data conditioning, signal processing, and data/signal monitoring [4] [12]. As with the Motorola MPAA020, the IMP EPAC uses the SC method to program the individual cells. The data for the cells is stored in a non-volatile electronically erasable programmable read-

only memory (EEPROM) memory and loaded into static random access memory (SRAM) when the device is started up to initialize the EPAC. The Motorola design uses only SRAM on the chip, and therefore needs an external memory to store circuit configurations, or the designs need to be loaded every time the device is started up. The design of the EPAC allows multiple EPAC devices to work together in tandem, and initialize at the same time [4]. Each cell uses an OpAmp to perform operations like amplification and comparison. While the design of the EPAC provides the same benefits as the Motorola device, it is still limited in its bandwidth as it is an SC design.

Table 1 - Commercially Available FPAAs

Company	Product	CAB Design	Technology	Applications	Bandwidth
Lattice	ispPAC	OpAmp	CMOS	Signal processing and conditioning	1.5 MHz
Zetex	TRAC	Log Domain Continuous Time	Bipolar	General signal processing	4 – 12 MHz
Motorola	MPAA020	Switched Capacitor	CMOS	General signal processing	200 kHz
IMP	EPAC	Switched Capacitor	1.2 µm CMOS	Signal conditioning and monitoring	125/150 kHz
Anadigm	AN10E40	Switched Capacitor	CMOS	Signal processing and conditioning	10 MHz
A. Basu & C. M. Twigg [18]	RASP 2.8	OTA	0.35 µm Floating-Gate CMOS	Signal Processing	50 MHz

The Anadigm AN10E40 is another SC design [11] [12]. AN10E40 is very similar in design to the Motorola MPAA020, but it does not have a comparator [11]. As with the Motorola design, there is no onboard non-volatile memory on the AN10E40, and as a result configurations must be stored off-chip, and loaded into the onboard SRAM at start-up [12].

A summary of commercially available FPAAs is shown in Table 1. Unfortunately most of the designs shown on the table are no longer available. The discontinuation of the production of FPAAs is likely due to the limited number of applications the commercially available FPAAs can be applied to, and the advancements in digital circuits have made microprocessors and FPGAs able to accomplish these applications cheaper and more easily. Anadigm still offers a range of FPAAs in discrete components [19], and Lattice offers some programmable analog components on their power manager designs [15]. The final row of the table shows one of the most advanced academic designs in literature today. This design by Basu et al. provides a large array of 32 CABs and uses floating-gate transistors to functions as switches and easy programmable elements [20].

2.2.1 Generic Field-Programmable Analog Array Design

A generic FPAA containing an $m \times n$ array of CABs is shown in Figure 2-1, where m is the number of rows and n is the number of columns. An FPAA design generally has CABs which perform specific or multiple analog functions [17] [21]. Different tasks are performed by an FPAA by combining various specific-function CABs or by programming a multiple-function CAB to accomplish the desired task. Both techniques have advantages. A multiple-function CAB requires more area than a single-function CAB, but can perform many different tasks, while a single-function design often takes multiple CABs to perform a similar task.

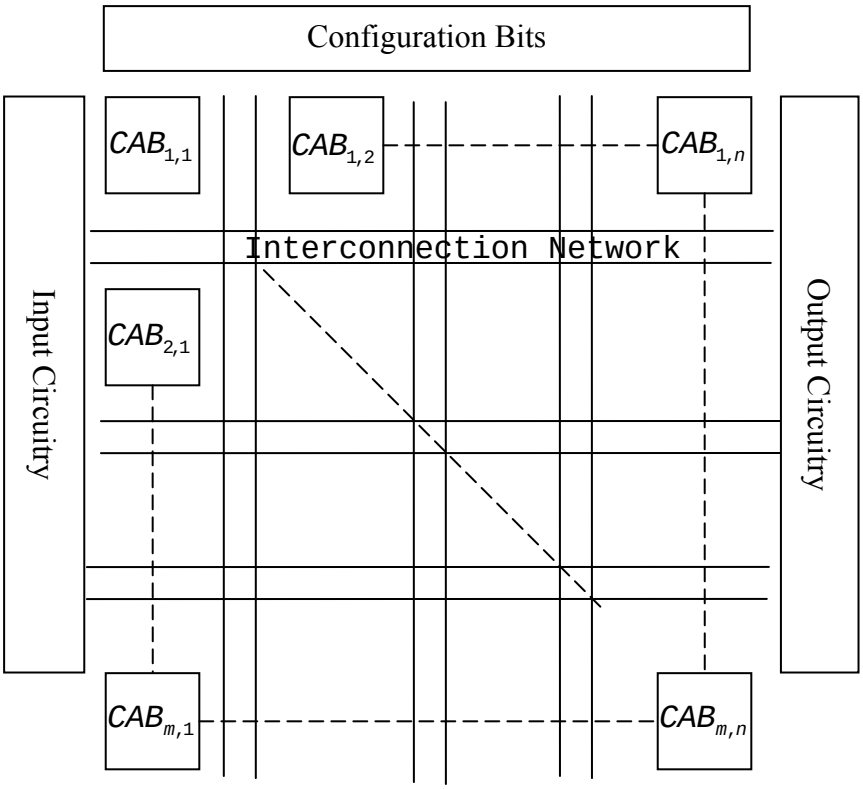

Figure 2-1 - Generic m × n FPAA design, the configurable analog blocks are shown in m rows and n columns. Each block contains configurable analog circuitry and is connected using an interconnection network represented as lines between the CABs. The supporting input and output circuitry connecting the FPAA with the outside world is also shown.

While the CABs perform the functions of the FPAA, there is another important part of the FPAA, namely the routing between the cells. The routing configuration needs to be flexible enough to provide the needed connections between the CABs to create the desired analog circuits without introducing too many parasitics, non-linearities, and noise to make the FPAA function as the designer desires.

One of the most popular methods of designing FPAAs is the switched capacitor (SC) method [4] [16] [22] [23]. The SC method allows for easy programmability and insensitivity to parasitic capacitances [24]. As the SC relies on switching to perform operations, digital circuits can easily control SC circuits leading to easy

programmability. However, SC circuits function in a discrete-time domain and are therefore limited to the Nyquist sampling rate: the signal must be sampled at twice the signal frequency or more [25], limiting the bandwidth of the analog circuit.

A G_m-Cell design works in continuous time and removes the Nyquist sampling problems [17] [26], since sampling is not required in a continuous-time system. Therefore, the bandwidth of the G_m-Cell design is increased when compared to discrete-time designs like the SC. Also, G_m-Cells do not require switches removing the problems with parasitics that switches introduce. However, G_m-Cells often use SRAM cells to store information about circuit configuration, which consumes surface area on an integrated circuit (IC) [27] [28]. As described in [28], each cell is connected to 6 other cells. Turning on and off different cells accomplishes routing between the cells; therefore, switches are not required in routing the array.

A system using lasers is one way to get around the problem of switches or SRAM cells. This method uses LaserLink's MakeLink™ technology [29]. MakeLink™ is an antifuse technology that uses a laser to program all of the switches when programming the FPAA. This results in a permanent circuit that is radiation-hardened, has a low resistivity compared to switched capacitor circuits, uses area efficiently, works reliably, and is compatible with commercial CMOS processes when using an antifuse cell [30]. However, this process is not reprogrammable,

and, therefore, is not well suited to create prototypes rapidly as once the FPAA is programmed no changes can be made to it.

The switched-current method has been around since the 1980s and has been proposed for use in FPAAs [31]. The switched-current method is able to operate with a lower supply voltage and uses a standard CMOS digital process to implement analog functions. To implement different functions, current memory cells, or current copiers are used, shown in Figure 2-2. Initially the current copier was used to match with continuous time current mirrors, but using switching techniques filtering and arithmetic functions can be realized [31] [32]. However, like SC circuits, switched-current circuits also hold the disadvantage of being discrete-time circuits.

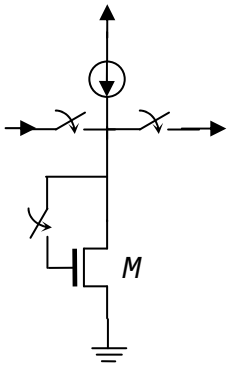

Figure 2-2 - Traditional switched-current memory cell

Floating-gate transistors were introduced in 1967 by Kahng and Sze [33]; since then they have been used largely in erasable programmable read only memories (EPROMs), EEPROMs, and Flash memory [34]. In 1989, floating-gate transistors were shown to be a valuable resource for more than just memory [34]. The

electronically trainable neural network (ETANN) chip used floating-gate transistors to create an array to produce currents usable by multiplier circuits [34], creating an array of analog memory elements. The analog memory element not only stores a '1' or a '0' seen in digital memories, but a continuous range of values found in analog signals. This technique has since been used to provide bias voltages with arrays of programmable floating-gate voltages [35]. Designers have created various computational units, including differential amplifiers [36], a multiplier [37], DAC converters [38], and translinear circuits [39] with floating-gate transistors as well. One of the more novel uses of floating-gate devices is in adaptive circuits, including adaptive amplifiers [40]. However, the most notable use of floating-gate transistors is in creating FPAAs. They are very useful as switches, since they require no memory to support them and can be programmed directly [41]. Also, as shown with the above examples, floating-gate transistors can create adaptable and programmable analog devices. The biggest drawback to the use of floating-gate transistors is that they do not use a standard digital CMOS process.

Currently, work is being done to develop a large scale FPAA using floating-gate transistors [20] [18]. Floating-gate transistors allow for programmable elements as switches and memory elements. Due to the nature of the floating-gate transistor, less area is used in implementing a floating-gate transistor system compared to a more traditional approach using memory and transmission gate switches [27]. Also, a transmission gate switch is only capable of operating between two states;

"on" and "off". This is because of the use of digital memory to control the switches. A floating gate switch is capable of operating at any arbitrary state between "on" and "off" as it functions as both the switch and the memory element [27]. Basu describes a floating gate FPAA which consists of 32 CABs connected together using multi-level routing [18]. This design described in Table 1 allows for the implementation of a wide range of functions including amplification, multiplying, and filtering [18].

There are many potential applications for high-speed FPAAs, one of which is as one among many reconfigurable components in an SDR. Therefore, Section 2.3 goes over some background information on SDR.

2.3 Software Defined Radio

Mitola first proposed SR 1992 [42]. An ideal SR would be able to operate with any communications service or bandwidth simply by running an algorithm that specifies the desired bandwidth and communication protocol. Mitola describes an SR as being a collection of DSP primitives, an overlying system to convert the primitives into communications functions, and processors to host SR real-time communications. Digital circuits are able to use various forms of software to perform different functions, and by completing the majority of processing in software develops a radio more flexible than traditional radio systems performing their signal processing in hardware. Figure 2-3 shows the ideal version of Mitola's SR.

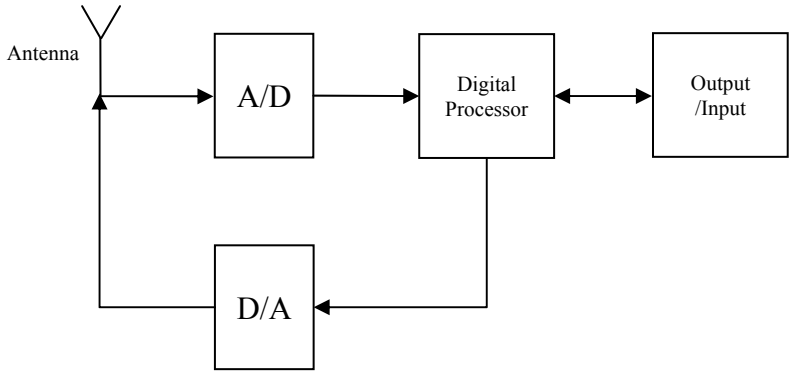

Figure 2-3 - Mitola's ideal software radio. This design converts the analog input signal into a digital signal as soon as possible, and then does all of the signal processing in the digital domain.

The flexibility of an SR leads to many advantages over a traditional hardware radio. For example, a variety of different standards could be implemented on a single radio, reducing the need to have different sets of hardware. The military has shown particular interest in this technology, as they have a large number of different standards such as very-high frequency (VHF) and ultra-high frequency (UHF) operating frequencies, and single-channel ground and airborne radio system (SINGCARS) and tactical fire direction system (TACFIRE) transmission modes [42]. Not only can multiple standards be implemented on SRs, but also the software can be updated to add new standards and modify existing standards. For instance, the wireless local area network (WLAN) Institute of Electrical and Electronics Engineers (IEEE) standards have been updated from 802.11 to 802.11n, with 802.11a/b/g in between. With a WLAN card for a PC implemented in an SR, a single software update would allow the card to update to a new standard, provided there are no major hardware changes. The transition from 802.11g to 802.11n did include a major hardware change, moving to a multiple input and multiple outputs (MIMO) system.

The development of a true SR is difficult due to the wide range of frequencies and standards which need to be supported by the SR. To overcome these difficulties, SDR was developed. SDR is an SR designed to work with specific standards, rather than with all standards. The bandwidth of an SDR is considerably narrower than the large bandwidth required by a SR; therefore, SDR designers are capable of producing SDRs which consume much less power than SRs. However, this limits the SDR to specific applications.

In order to increase the flexibility of radio systems and move away from an SDR and towards an SR, more frequencies need to be accessible. This is not possible with the current speed and precision of ADCs. In order to work over a 5 GHz bandwidth, the ADC would need to operate at 10 GS/s, and with a high level of precision, approximately 16 bits [43]. Currently commercially produced ADCs operate at 250 MS/s with 16 bits of precision, or 400 MS/s with 12 bits of precision [44] [45]. The current academic designs operate with 6 bits of precision at 40 GS/s, although this is for an optical channel, or with 6 bits of precision at 2.2 GS/s [46] [47]. Therefore, the current state-of-the-art ADCs do not operate at the required sampling frequency, nor do they have the required precision.

One of the ways that digital circuits circumvent this problem is to use a technique known as undersampling or band-pass sampling [48]. Rather than sample a signal directly, undersampling samples the signal at its bandwidth frequency. This

circuit technique allows for a simplification of the digital circuitry rather than using analog mixers to convert the signal to a lower IF or baseband [48] [49]. However, this technique often consumes hundreds of mW of power, and needs complex anti-aliasing filters.

In order for an SDR to operate in multiple bands, there are some design specifications that need to be met. Current designs have been developed to operate in the high frequency (HF) range and the UHF range [50] [51]. The HF band is 3 – 30 MHz, which is slow enough to operate in the manner that Mitola envisioned [52]. The ADC used in the design developed by Davies operates at 60 MS/s, allowing for the entire HF band to be digitally captured [50]. This system requires a sensitivity of at least 16 dB, provided that the receiver is operating in a quiet receiving site. The upper range of the received signal then needs to be 113 dB to avoid damaging the radio system. To avoid interference, the selectivity needs to be greater than 110 dB. The $IP3_{in}$ should be greater than 20 dBm, which leads to a spurious free dynamic range of 100 dB.

Other designs have been proposed to operate at a much higher frequency. Bagheri's design operates in the 800 MHz to 6 GHz range [51]. This band contains all of today's cellular and WLAN channels [52]. In order to operate in this range, the signal needs to be down-converted into the ADC's Nyquist range. Once at a lower range, the band is much more manageable with the 802.11g channels occupying a 20 MHz bandwidth and the global system for mobile

communications (GSM) channels occupying 200 kHz. To properly amplify GSM signals, the SDR needs to provide at least 43 dB of gain and have a variable range of 31 dB [52]. Filtering eliminates any aliasing and interference from other signals. If the user desires a GSM signal, then filtering needs to attenuate the close code division multiple access (CDMA) band by 80 dB and any images by 70 dB.

The current development of FPAAs does not allow the integration of FPAAs into SDR designs. The flexibility of current FPAAs does not allow the implementation of enough circuits to include FPAAs in SDR. Also the current frequency response of FPAAs, around 50 MHz, is lower than currently available ADCs [18]. As a result, more research is needed in the development of FPAAs before SDRs could include FPAAs.

2.4 Thesis Research

Current FPAA designs are not capable of performing at RF levels [12]. However, this thesis postulates that they could be used in the IF range of a radio receiver.

Most of the FPAA designs in the literature today focus on creating filters [26] [53] or using specialized processes [41] [54]. An FPAA that creates filters is useful in developing an SDR. SDRs can use programmable filters to select the appropriate bands for the desired standard. However, a linear filter-based FPAA is unable to perform many of the signal processing functions like multipliers, or phase-lock loops that could be required. Other FPAAs of a more general design tend to require a specialized process [29] [41] [55] [56] or only operate up to

approximately 130 MHz [56]. This is in the VHF for radio systems, which ranges from 30 MHz to 300 MHz, and includes the international FM radio band, the military VHF-FM Band, and the Air and Marine Bands. Also, these FPAAs can operate in many of the commonly used IF bands such as in microwave receivers at 70 MHz and 75 MHz and some RF test equipment at 21.4 MHz.

This thesis presents a CAB for an FPAA that was designed to ideally function in the industrial, scientific, and medical (ISM) band from 402 MHz to 405 MHz. This band would allow development of SDR for use in medical equipment such as pace makers, or scientific equipment such as wireless sensors. Switched analog circuits, like SC or switched-current circuits, can limit the frequency response of the analog circuits due to the required Nyquist rate; therefore, a continuous-time circuit was chosen over a switched analog circuit. To create a continuous time FPAA with a large amount of flexibility, an operational transconductance amplifier-capacitor (OTA-C) design was used in this thesis. OTAs use a voltage input and have a current output. The OTA is able to produce filters and variable gain amplifiers more easily than a traditional OpAmp due to the current output of an OTA. In order to function in the 402 to 405 MHz ISM band, the OTA design would ideally have a DC gain of 50 dB and a -3B gain of 405 MHz. An OTA with a gain bandwith product of 405 MHz would offer some functionality in the desired frequency range.

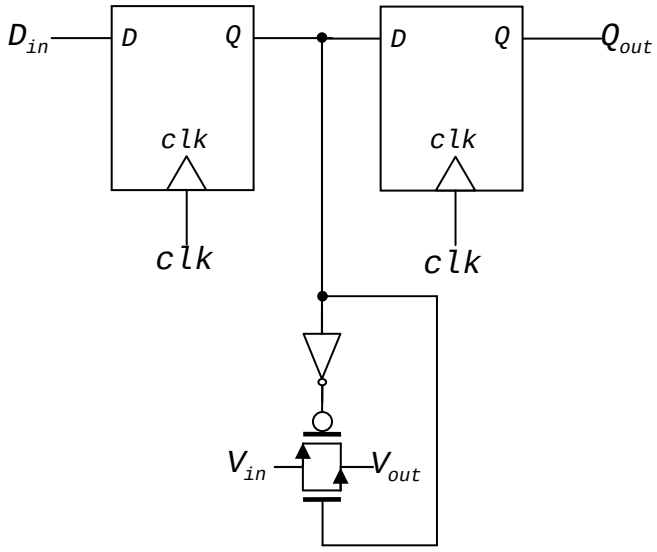

Figure 2-4 Connection from shift register to transmission gate switch.

OTAs have been demonstrated in the literature to operate at the desired band [57]. Therefore, an OTA provides the heart of the CAB. The CAB design also includes a capacitor array to provide adjustments to the frequency response of the CAB, a shift register which provides digitally programmable memory for the CAB, and switches made from transmission gates to allow for reconfiguration of the routing

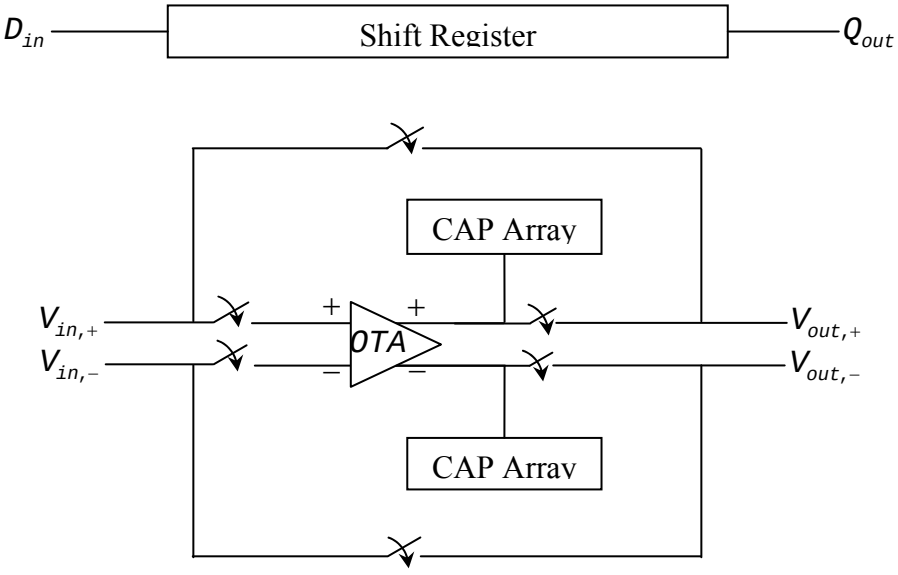

Figure 2-5 - Block diagram of CAB. The shift register is connected to the switches as shown in Figure 2-4.

Implementing a full array would make testing the design for flaws difficult as any errors could be from a single CAB or in the routing between the CABs. In order to properly test the design, a chip implementing a single CAB was designed. This CAB can then be tested to ensure its functionality for use in a large scale FPAA. Also, in order to test the use of the CAB in an array at the simulation stage, multiple copies of the CAB were created in our simulation.

Chapter 3

Proposed Circuits

This thesis proposes a CAB design for an FPAA for use in signal processing applications, such as filtering. The structure of the CABs depends on the purpose of the FPAA; for instance an FPAA created for filtering could be constructed using G_m-C cells [53], while an FPAA that focuses on data conditioning could use a SC OpAmp circuit [4]. There are two major theories behind the design of the CAB; a CAB may include multiple circuit primitives, such as the design from Lee and Gulak [21], or a CAB can have a single primitive, where combining multiple CABs can create different circuit combinations [17].

Our proposed circuit uses an OTA as the basis for the CAB. An OTA is capable of performing various operations, including filtering, and has been shown to operate at high frequencies. Other current-mode devices, such as switched-current cells, SC cells, current conveyors, or differential amplifiers can implement linear and non-linear circuits for an FPAA, but an OTA offers an excellent choice for high frequency resistorless analog designs, and the simplicity and controllability of the OTA makes it the better choice [55]. Also, combining the OTA CAB with other CABs can create various types of circuits such as band-pass filters.

3.1 Folded-Cascode Operational Amplifier

OpAmps are one way of providing a basis for CABs to be used in an FPAA. The ideal voltage OpAmp has an infinite open-loop gain, infinite bandwidth, infinite input impedance, infinite slew rate, infinite common mode rejection ratio (CMRR), infinite power supply rejection ratio, zero input current, zero input offset voltage, zero output impedance, and zero noise. Voltage OpAmps created in practice have various tradeoffs that need to be taken into consideration. While the ideal voltage OpAmp can be used as a base to implement many different functions, the actual creation of a voltage OpAmp needs a design for a specific purpose.

The folded-cascode OpAmp can be used as an OTA [58]. The OTA is a voltage controlled current source because the voltage at the input of the amplifier produces a proportional current at the output. This differs from the voltage OpAmp in that there is ideally an infinite output impedance to drive the output current as opposed to the zero output impedance ideal in a voltage OpAmp.

In a cascode amplifier, a common-source-connected transistor feeds a common-gate-connected transistor [58]. The cascode design often has very large output impedance for a single stage gain, and this configuration limits the voltage across the drain of the input drive transistor, M_2 in Figure 3-1 (a), minimizing the short-channel effects.

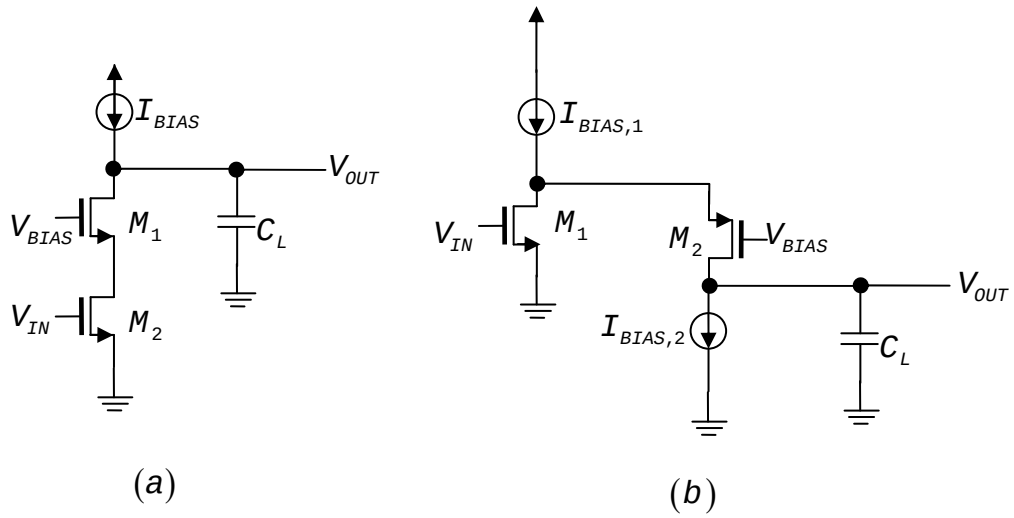

Figure 3-1 - (a) Cascode amplifier configuration (b) folded-cascode amplifier configuration

The folded-cascode configuration allows for the direct current (DC) level of the input to be the same as the output, and can be used to realize the folded-cascode OpAmp. Figure 3-1 shows the cascode and folded-cascode circuit configurations. The cascoded design of the OpAmp yields a single stage gain in the range of 700 to 3000 V/V. The design presented in this thesis is slightly under 700 V/V. The single stage keeps the area used by an OTA to a minimum, which is a requirement for implementing an array of OpAmps for an FPAA.

OTA based circuits are capable of implementing a wide range of functions, including filters, multipliers, dividers, exponentiation blocks, roots, and piecewise-linear function generators [59]. The bias voltages control the gain produced by the OTA, leading to its programmability. For example, changing V_{B_3} in Figure 3-2 changes the amount of current flowing through transistors M_7 and

M_8. The change in current alters the g_m of the transistor, and as a result, changes the gain of the overall design.

There are two different versions of OTAs: single-ended and differential. A single-ended OTA has two inputs, but only one output. In contrast, differential OTAs have two inputs and two outputs, and it provides a better immunity to noise than that of the single-ended design [5]. The resistance to noise comes from the signal being the difference between two inputs. Any noise which affects the two inputs does not affect the signal itself since the noise will be cancelled out from the difference between them. Also, the differential design allows the circuit to be biased without the need for bypass and coupling capacitors [5]. A differential OTA can be transformed into a single-ended OTA by tying one of the outputs to ground. The ability to create a single-ended design from a differential design means that no functionality is lost in using a differential OTA rather than a single-ended OTA.

3.1.1 Differential OTA Design

P-channel metal-oxide-semiconductor (PMOS) input transistors were chosen for the amplifier which reduces the input transconductance, and as a result, increases the input voltage swing of the amplifier compared to having n-channel metal-oxide-semiconductor (NMOS) input transistors. In this process technology, a single-ended OTA with NMOS input transistors has an input voltage swing of 0 to 1.4 V and using PMOS input transistors the using the same design has an input voltage swing of 0 to 1.7 V. Having a large input swing is important in the design

of the FPAA where as there are a large number of OTAs connected together. With a small input swing the signal can be truncated at the input of the OTA resulting in information loss from the signal. Figure 3-2 shows the initial differential design.

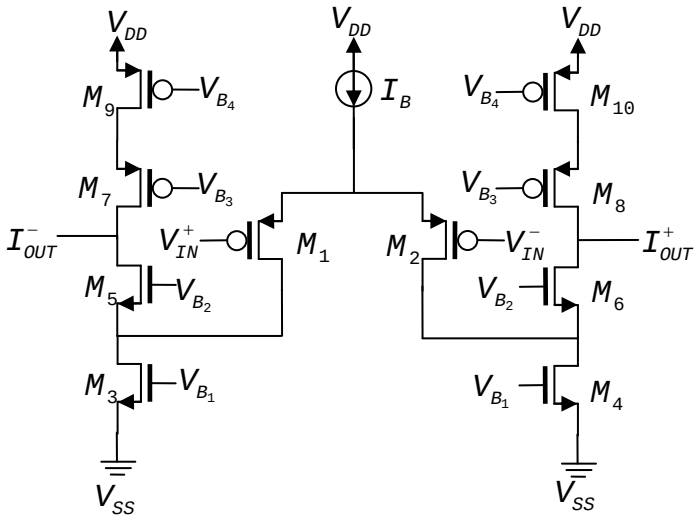

Figure 3-2 - Fully differential OTA. Uses a bias current of I_B and uses PMOS input transistors to increase the input voltage swing.

Designing the folded-cascode amplifier began with defining the specifications of the circuit. Most of the specifications are provided, and can be seen in Table 2.

Table 2 - OTA Specifications

Specification	Value
V_{DD}	1.2 V
I_B	100 µA
P	120 µW
V_{swing}	0.6 V
A	50 dB
G_m	500 µS

After choosing the specifications, the maximum power consumption of the amplifier was determined. In the case of this design, it was necessary to keep the power consumption to a minimum, as the final FPAA design will have a large number of amplifiers. A power consumption of 120 μW would allow the final FPAA design to contain a large number of CABs. 120 μW provides a low power draw from the OTA and allows for easier calculations for the OTA design. From the power consumption, the amount of current used by the OTA can be determined using the power equation:

$$P = VI \tag{3-I}$$

Using equation (3-I) and the constant V_{DD}, with V_{DD} = 1.2 V in our chosen technology (0.13 μm CMOS), the required source current was calculated as 100 μA.

The overdrive voltages (V_{OD}) for the transistors were then determined. The voltage swing of the circuit provides the limiting factor for calculating the overdrive voltages for the transistors. In order to provide the largest voltage swing at the output of the circuit requires a swing of 0.6 V on each half output. This yields a total output voltage swing of 1.2 V for the differential signal. The output swing for one half of the circuit was calculated from the equation:

$$V_{swing} = V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}| \tag{3-II}$$

The top end of the voltage swing was found from:

$$V_{Swing,Max} = V_{DD} - |V_{OD7}| - |V_{OD9}| \quad \textbf{(3-III)}$$

The bottom end of the voltage was calculated using:

$$V_{Swing,Min} = V_{OD3} + V_{OD5} \quad \textbf{(3-IV)}$$

If the voltage swing is 0.6 V, then by setting the minimum voltage to 0.3V and the maximum voltage to 0.9 V, the overdrive voltages can be set. Since more current goes through M_3 than M_5, M_7, and M_9, a higher overdrive voltage is desired for M_3; therefore, the overdrive voltage for M_3 is set to 0.2 V. This results in M_5 having an overdrive voltage of 0.1 V. M_1, M_7, and M_9 have the same amount of current flowing through them, and therefore the overdrives are set to –0.15 V.

With the overdrive voltages calculated and the amount of current chosen, the width-to-length ratios for the transistors in the OpAmp can be calculated. The main equation to calculate the width-to-length comes from the transistor drain current equation:

$$I_D = \frac{1}{2} k'_{n,p} \frac{W}{L} V_{ov}^2 \quad \textbf{(3-V)}$$

In equation (3-V), using the overdrive voltages from above and $k'_{n,p}$ is a process parameter giving the transconductance of the NMOS or PMOS transistors. This equation forms a relationship between the size of a transistor, the voltage across a transistor, and the current which flows through a transistor. The width-to-length ratios are determined and shown in Table 3.

Table 3 - Transistor Widths

for Differential OTA

Transistor	Width-to Length Ratio (W/L)
M_1	31.97
M_3	4.60
M_5	18.40
M_7	31.98
M_9	31.98

The chosen overdrive voltages and currents also allow us to calculate the transconductance (g_m) and output resistance (r_o) of the different transistors using:

$$g_m = \frac{I_D}{V_{ov}} \quad \textbf{(3-VI)}$$

and,

$$r_o = \frac{1}{\lambda I_D} \quad \textbf{(3-VII)}$$

Where λ is the channel length modulation, and λ is assumed to be 0.1. Then the gain of the circuit is calculated using the values for g_m and r_o in equation (3-VIII):

$$A_v = g_{m1}\left\{\left[\left(g_{m5} + g_{mb5}\right) r_{o5}\left(r_{o1} \,||\, r_{o3}\right)\right] ||\, \left(g_{m7} + g_{mb7}\right) r_{o7} r_{o9}\right\} \quad \textbf{(3-VIII)}$$

Using the above equation (3-VIII) and the overdrive voltages, the gain of the circuit calculates to:

$$A_v = 751\frac{V}{V} = 58dB \quad \textbf{(3-IX)}$$

58 dB of gain is capable of performing a variety of signal processing applications, such as filtering and amplification. The goal of 50 dB of gain is based on the

GSM requirements outlined by Bagheri based on input signals as low as -102 dBm [51]. As a result this design was simulated in Cadence first.

The overdrive voltages were also used to calculate the bias voltages required for the transistors.

$$V_{B_1} = V_{ov,3} + V_{tn} \quad \textbf{(3-X)}$$

$$V_{B_2} = V_{ov,1} + V_{ov,5} + V_{tn} \quad \textbf{(3-XI)}$$

$$V_{B_3} = V_{DD} - \left(\left|V_{ov,7}\right| + \left|V_{ov,9} + V_{tp}\right|\right) \quad \textbf{(3-XII)}$$

$$V_{B_4} = V_{DD} - \left(\left|V_{ov,9} + V_{tp}\right|\right) \quad \textbf{(3-XIII)}$$

Figure 3-3 shows the simulation of the differential OTA. The lengths and widths of the transistors are limited by the minimum feature size of the process being used; the process being used in this thesis has an L_{min} of 120 nm and a W_{min} of 140 nm. In this instance a length of 240 nm was used for the transistors, twice the minimum length (L_{min}) allowed by the design rules, and the widths used followed the ratios given in Table 3. Having the transistors operate at L_{min} did not allow the OTA to operate with all of the transistors in saturation, and thus a value of twice L_{min} was selected for use in subsequent simulation.

However, when the design, shown in Figure 3-3, was simulated in the process and the schematic was tested, the results were less than ideal. The unloaded voltage gain of the OTA was found to be 39 dB, with a power consumption of 173.5 μW, a -3 dB bandwidth of 21.91 MHz, a unity gain bandwidth of 2.09 GHz, and a

GBW of 1.74 GHz. This is a much lower value than desired for the operation of the OTA. Originally, a value of 0.1 was used for λ in hand calculations of transistor sizes. However the simulated value of λ was later found to be 0.577, resulting in a lower output resistance leading to a lower-than-anticipated gain.. As a result, modifications needed to be made to the design.

3.1.2 Gain-Boosted Differential OTA

A paper by Burger [57] proposes a method of gain enhancement by using single-

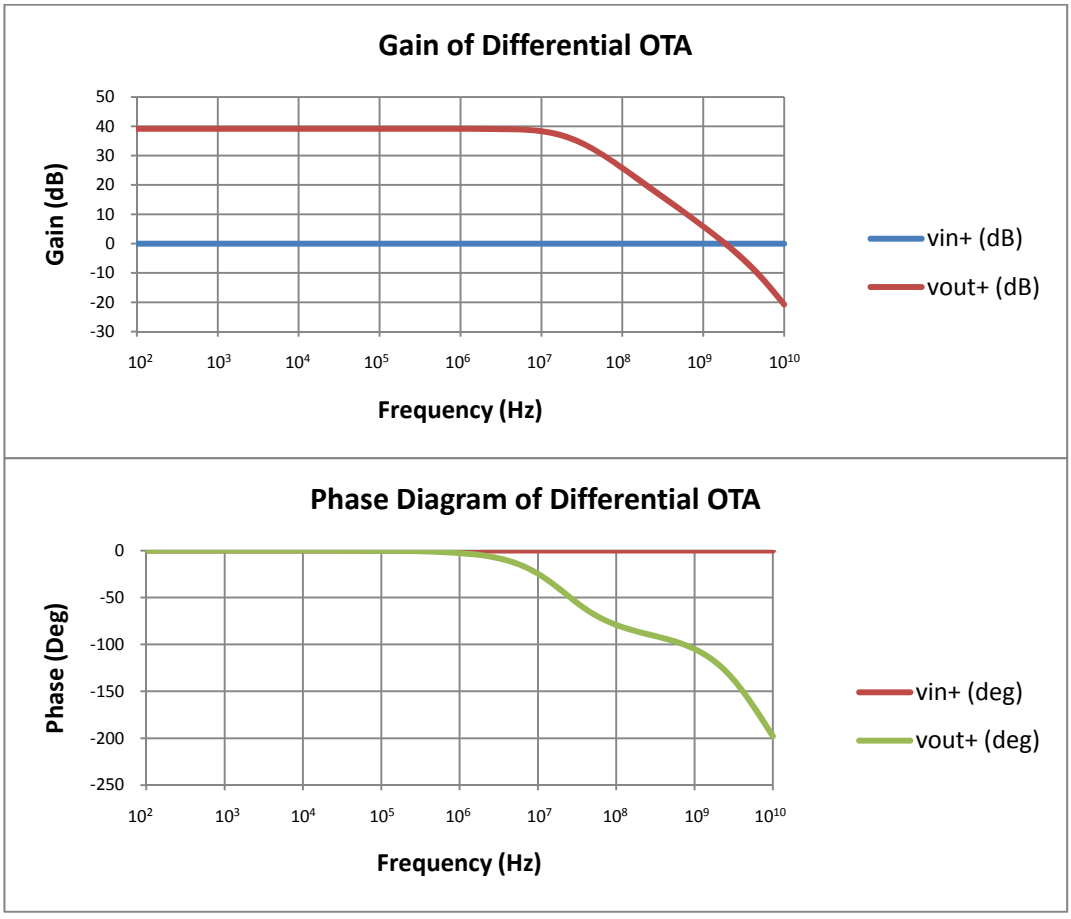

Figure 3-3 - Bode plot of differential OTA. This bode plot shows the differential OTA design to have a gain of 38 dB with a roll off of about -20 dB/decade. This design has a -3 dB bandwidth of 21.91 MHz and a unity gain bandwidth of 2.09 GHz, and a phase margin of 60^{o}.

ended OTAs at the input to increase the DC gain of the OpAmp by increasing the gain response of the transistors M_5 to M_8 in Figure 3-2.

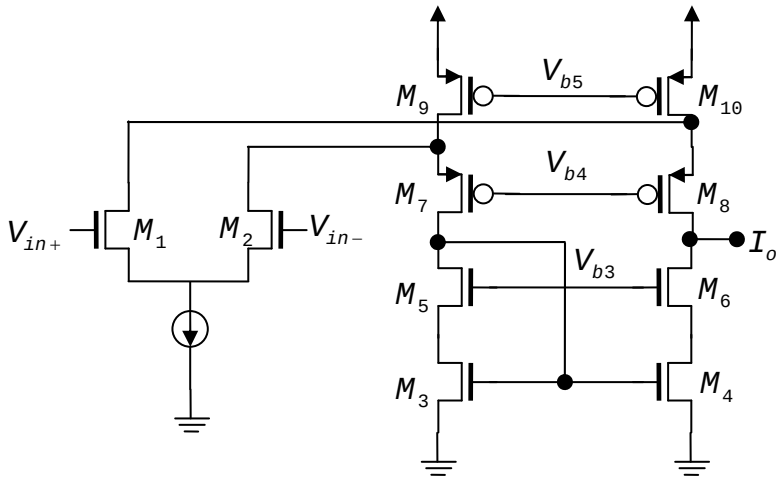

Figure 3-4 – PMOS Gain-Boosting OTA

Figure 3-4 shows the design of the OTA used to boost the DC gain for the PMOS transistors in the differential OTA, and Figure 3-5 shows the OTA used to boost the DC gain for the relatively lower voltage NMOS transistors on the differential OTA from Figure 3-2. When these are connected with the differential OTA, the DC gain can be boosted considerably, up to 80 or 90 dB [57].

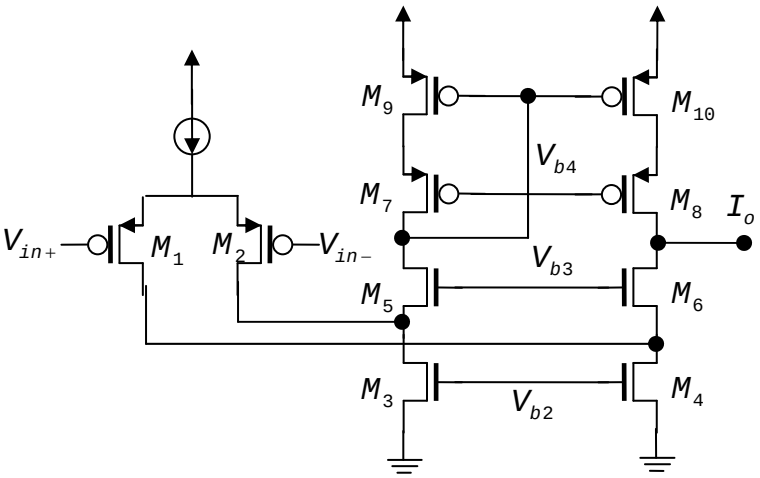

Figure 3-5 – NMOS Gain-Boosting OTA

The PMOS based input design in Figure 3-5 has a gain of 35 dB and a -3 dB bandwidth of 510 kHz. The NMOS based input design in Figure 3-4 has a 34 dB gain with a -3 dB bandwidth of 795 kHz. One of the advantages of these OTAs is that the same bias voltages can be used, meaning less need for extra voltage sources than if separate voltage sources were required for the gain-boosting OTAs. These designs are then connected to the differential OTA design in the configuration shown in Figure 3-6.

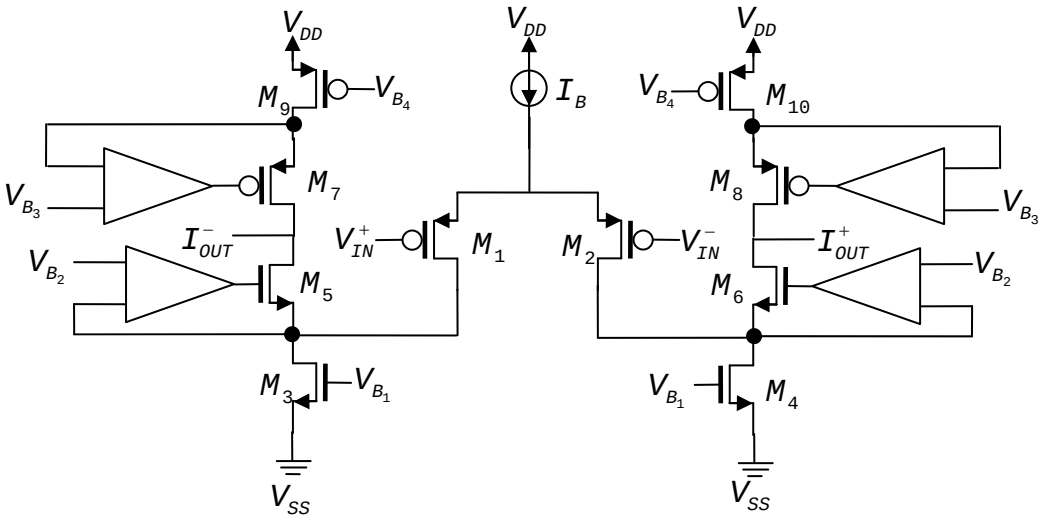

Figure 3-6 -- DC Gain Boosted OTA. The gain-boosting OTAs for M_5 and M_6 are shown in Figure 3-5 and the gain-boosting OTAs for M_7 and M_8 are shown in Figure 3-4.

This design increased the gain of the differential circuit to 798 V/V or 58 dB with a -3 dB bandwidth of 31.05 kHz, a unity gain bandwidth of 2.03 GHz as shown in the Bode plot in Figure 3-7, and a GBW of 24.7 MHz. The power consumption of this design is increased to 405.6 µW from the 173.5 µW of the original design. This results in an increase of the gain by about eight times. Even with this increase in gain, the OTA's gain is still much lower than the gain increase shown in the work done by Burger [57].

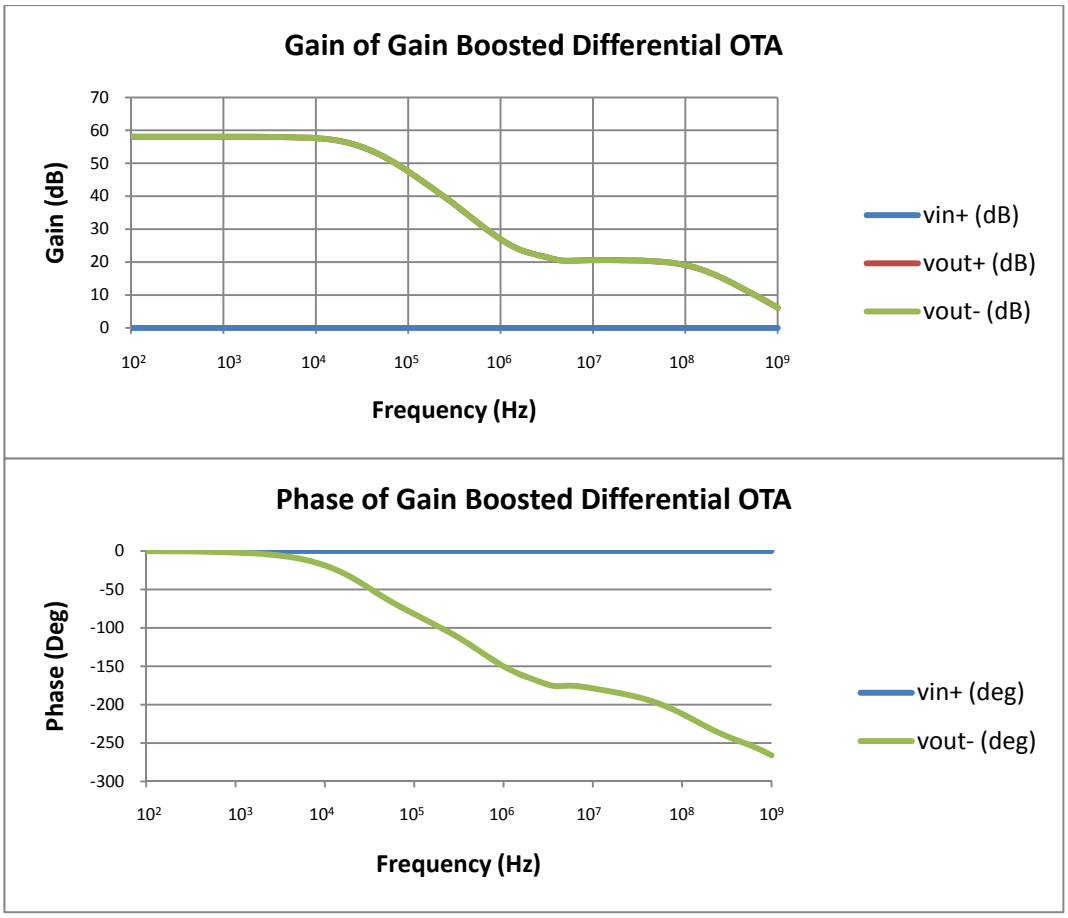

Figure 3-7- Bode plot of gain-boosted OTA. This graph shows that the gain has been boosted from the 38 dB of gain in Figure 3-3 to 58 dB with a -3 dB bandwidth of 31.05 kHz and a unity gain bandwidth of 2.03 GHz. However, the phase diagram of the Bode plot shows that the OTA is unstable.

The DC gain-boosted OTA provides 58 dB of gain, giving the amplifier enough gain to amplify small signals for detection by an ADC. If a larger gain is required, then more amplifiers can be combined to increase the gain.

3.1.3 Redesigning the Operational Transconductance Amplifier

Due to the limited frequency response of the gain-boosted OTA, the increased power consumption, and the inherent instability of the gain-boosted design, the folded-cascode OpAmp without gain-boosting required a redesign and more simulations. Even adding compensating capacitors to the gain-boosted OTA did

not result in a stable OTA. The frequency response of the OTA without gain-boosting provided the desired results, but the gain was not high enough.

Increasing the size of the transistors in the OTA also increased the gain of the OTA. Increasing the size of the transistors affects two different components of the frequency response. First, increasing the size of the transistors affects the value of λ, as $\lambda \propto \frac{1}{L}$, and as a result, increases the value of r_o. Therefore, increasing the size of the transistors increases the output resistance of the transistors, and in turn increases the gain of the OpAmp. However, the second effect of increasing the size of the transistors is an increase of the parasitic capacitances of the transistors. This increase in the parasitic capacitances decreases the unity gain frequency and the -3 dB frequency of the OpAmp.

Figure 3-8 shows the simulation results of varying the transistor sizes in the OTA without gain-boosting. The bode plots of the varying transistor sizes show that the larger sized transistors reduce the unity gain and -3 dB frequencies, and also increase the instability of the OTA. Increasing the output capacitance of the OTA decreases the unity gain and -3 dB frequencies even further, but this increase solves the problem of instability in the OTA. A transistor sizing of 5 times the minimum length achieves the desired 50 dB DC gain.

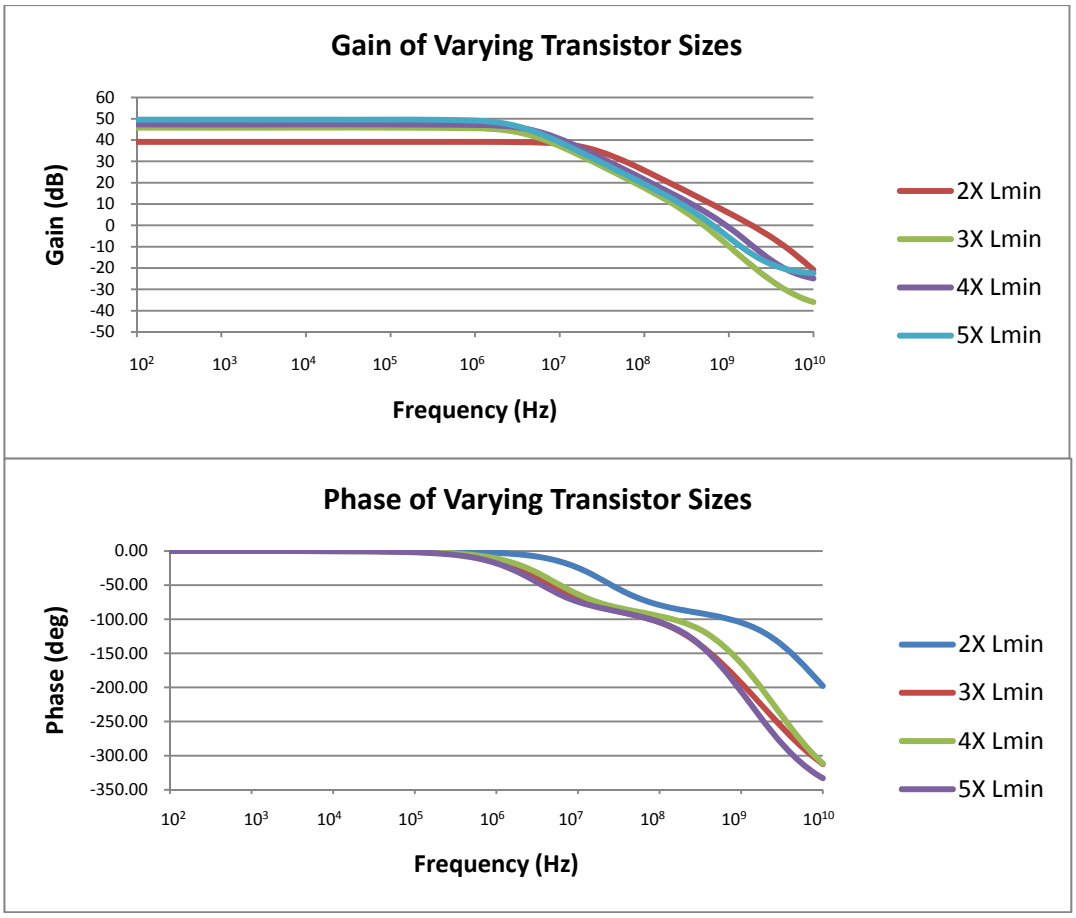

Figure 3-8- Bode plot of OTA with varying transistor sizes. This Bode plot shows the increase in the gain of the differential OTA shown in Figure 3-2 by increasing the size of the transistors. This also lowers the stability of the OTA but can easily be compensated for by changing the load capacitance.

The design was refined to achieve a better frequency response using a 4 times the minimum transistor length OTA. Increasing the width-to-length (W/L) ratio of the input transistors only increases the gain of the OTA without dramatically affecting the frequency response compared to increasing the length of all of the transistors.

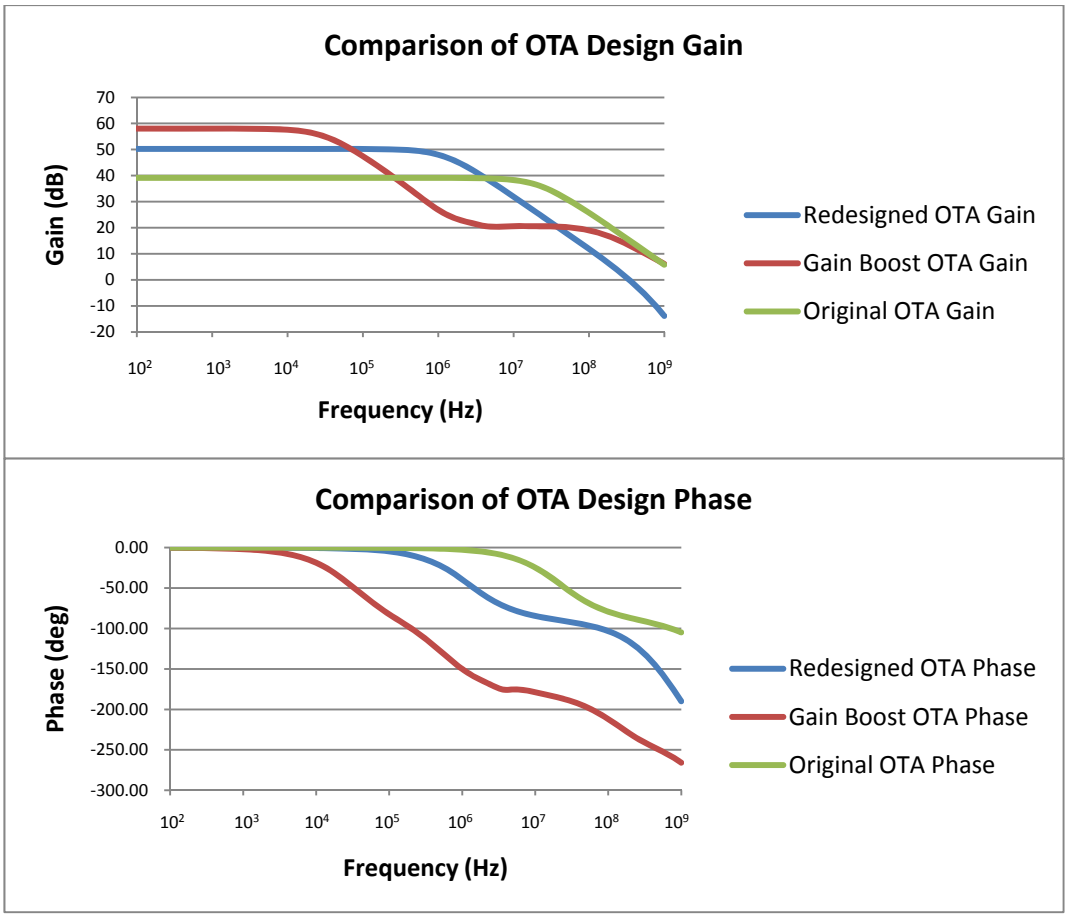

Figure 3-9 - Bode plot comparing OTA designs. This shows the original design of OTA, the Gain-boosted design, and the new design using 4 times minimum length transistors and a 90 W/L input transistor ratio. The graphs show that the response of the redesign gives 50 dB of gain with a -3 dB bandwidth of 1.217 MHz and a unity gain bandwidth of 344.36 MHz. The phase margin is about 50^{o} and the roll off is -20 dB/decade.

Figure 3-9 shows the bode plot of the final OTA simulation compared with previous design simulations. This design has a DC gain of 50.26 dB with a -3 dB bandwidth of 1.217 MHz, a unity gain bandwidth of 344.36 MHz, a GBW of 384.8 MHz a power consumption of 156.2 µW, and an input voltage swing of 0 to 1.6 V for the transistors to remain in saturation. Figure 3-10 shows a transient simulation of the OTA. This simulation demonstrates that a signal amplitude of more than 0.7 mV results in signal clipping.

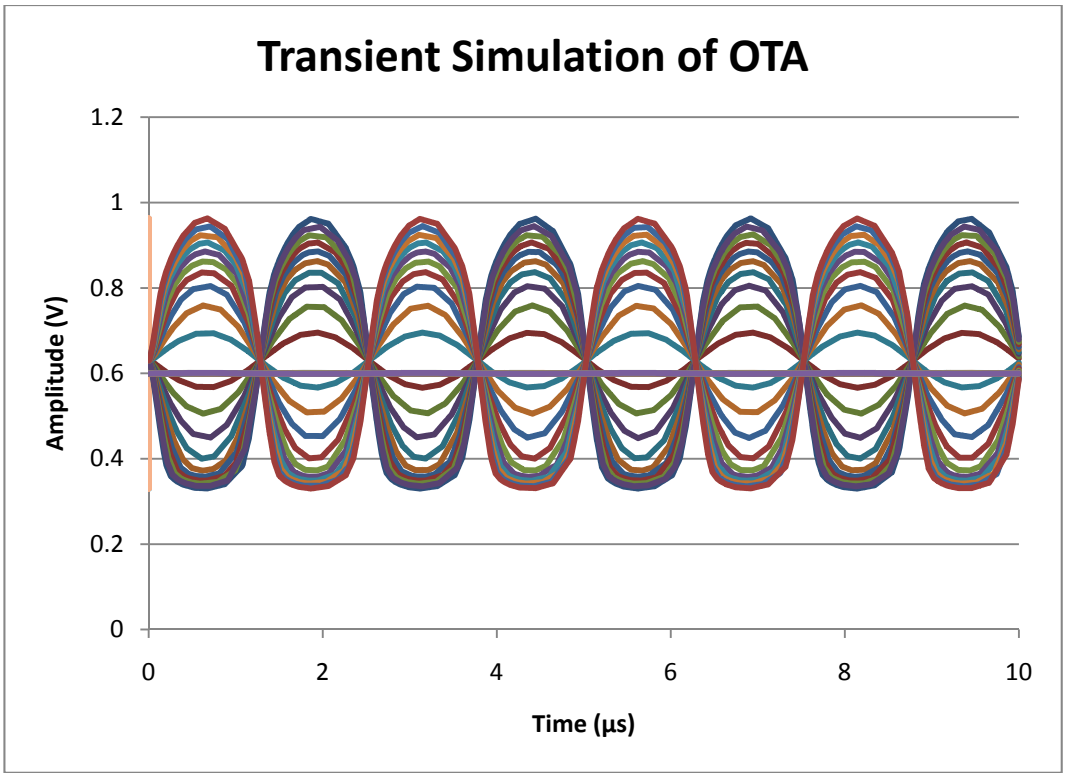

Figure 3-10 - Transient simulation of the OTA showing output signal clipping. The input signal amplitude ranges from 0.1 mV to 1 mV. Once the signal increases above an amplitude of 0.7 mV, the signal starts to be compressed in the lower range on the output signal.

The transconductance of the OTA was simulated using the test bench shown in Figure 3-11. An input signal is sent into the OTA and the resulting current is measured over the DC voltage sources used to bias the outputs.

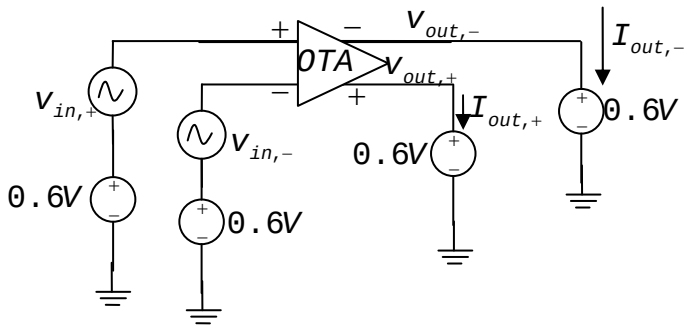

Figure 3-11 - Test bench for measuring the transconductance of the OTA. The output voltage sources are used to properly bias the output and measure the current of the outputs.

A simulation of the test bench shown in Figure 3-11 with the outputs floating rather than having a load lets the OTA self-bias point be measured. The transient

simulation of the floating output is shown in Figure 3-12, and the self-bias point is 0.63 V.

The transconductance simulation is shown in Figure 3-12 and Figure 3-13. The bottom graph in Figure 3-12 displays the output current of the OTA with an input signal at 100 kHz, an amplitude of 0.1 mV, and a DC bias of 0.6 mV. Figure 3-13 shows the frequency response of the OTA's transconductance. The transconductance is 705 µS with a -3 dB point at 705 MHz.

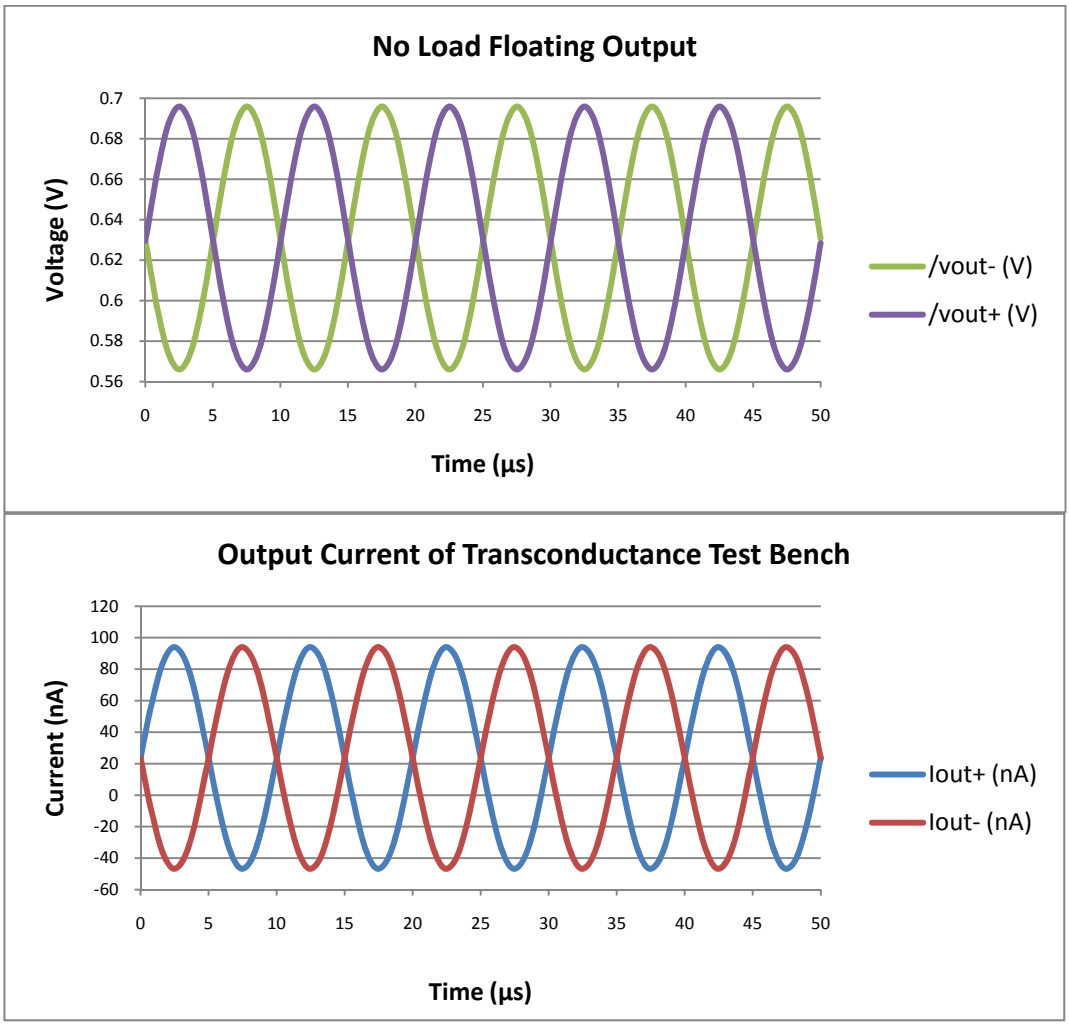

Figure 3-12 - The top graph shows the output voltage of the test bench shown in Figure 3-11 when there is no load at the ouput. This demonstrates that the OTA biases itself at 0.63 V. The second graph shows the transient simulation of the output current with an input voltage signal with a 0.1 mV amplitude, a DC bias of 0.6 V and a frequency of 100 kHz.

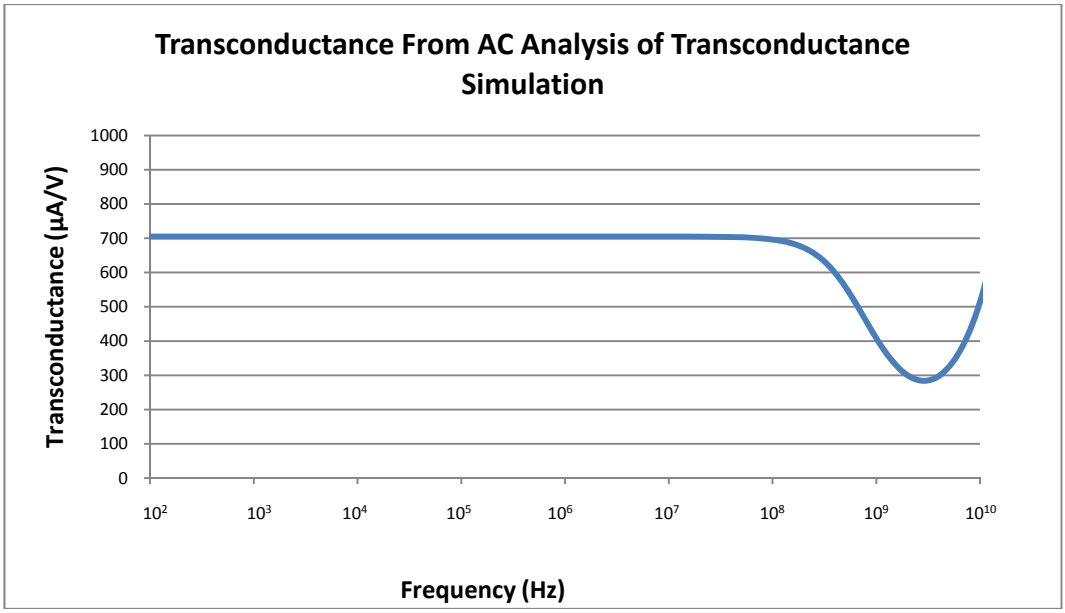

Figure 3-13 - This is the AC analysis of the transconductance test bench shown in Figure 3-11. The transconductance is found to be 705 µS and has a -3 dB point at 707 MHz.

A comparison of the OTA designs is shown in Table 5. This design gives the desired 50 dB gain and provides a larger bandwidth than other design iterations performed in the development of the OTA presented in this thesis which have the same gain with lower power consumption. A summary of the gains and bandwidths based on transistor lengths is shown below in Table 4.

Table 4 - Table of variation in transistor sizes of OTA

Multiple of Minimum Length	W/L Ratio of Input Transistors	DC Gain (dB)	-3 dB Bandwidth (MHz)
2X	31.98	39.14	21.90
3X	31.98	45.82	3.979
4X	31.98	47.29	5.142
4X	60	49.28	1.661
4X	90	50.26	1.217
5X	31.98	49.61	0.9731
5X	60	51.95	0.6587

Table 5 - Comparison of OTA Designs

	Original OTA	Gain-boosted OTA	Redesigned OTA
Technology	0.13 µm	0.13 µm	0.13 µm
Supply voltage	1.2 V	1.2 V	1.2 V
Input W/L	31.98	31.98	90
-3 dB Bandwidth	21.91 MHz	31.05 kHz	1.217 MHz
Unity Gain Bandwidth	2.09 GHz	2.03 GHz	344.35 MHz
DC Gain	38 dB	58 dB	50 dB
Phase Margin	60^o	Unstable	50^o
GBW	1.74 GHz	24.7 MHz	384.8 MHz
Power	173.5 µW	405.6 µW	156.2 µW

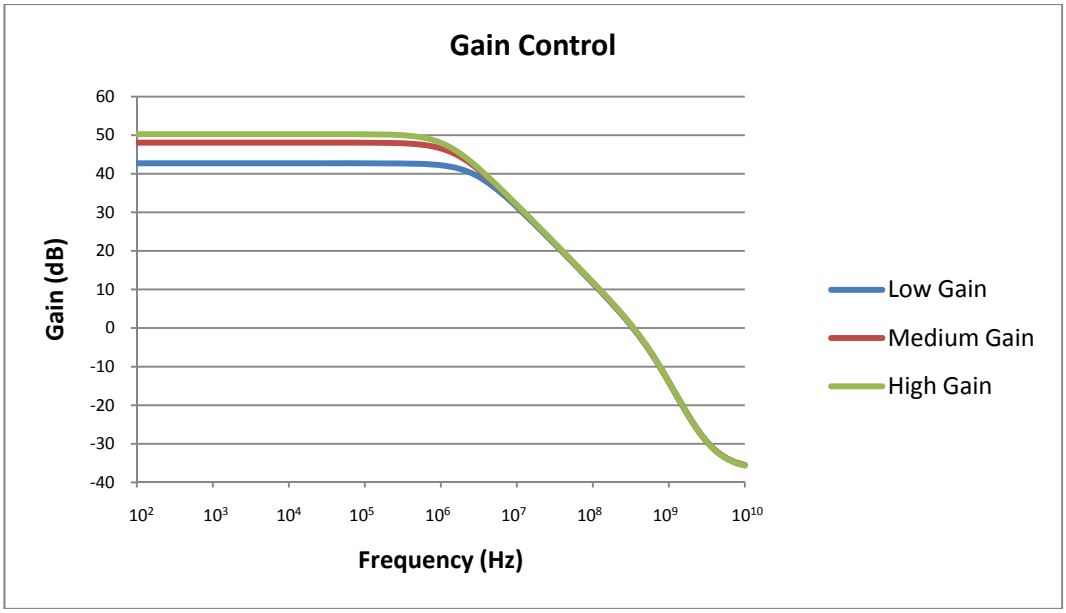

Figure 3-14 - Gain control of OTA by varying bias voltages. This shows the ability to change the gain of the OTA by varying the bias voltage $V_{B,3}$ from Figure 3-2. Here the gain varies from 42.71 dB to 50.26 dB while $V_{B,3}$ ranges from 0.58 V to 0.6 V.

The adaptability of the OTA in the final design can be demonstrated through the ease with which the gain of the OTA can be controlled. Figure 3-14 shows the variation in gain for the OTA from 42.71 dB to 50.26 dB by changing the value of V_{B_3} in Figure 3-2. The transistors are properly biased in all cases leaving them in saturation. Changing the bias voltage alters the value of g_m of the individual

transistors. Since the gain of the circuit is directly proportional to the value of g_m, the gain is controlled through the variation of the bias voltages, specifically V_{B_3} ranging from 0.58 V to 0.60 V.

3.2 Configurable Analog Block

A CAB should be able to be programmed alone, or with other CABs to create different analog circuit configurations. This thesis proposes a design using a highly configurable CAB design.

The CAB proposed in this thesis consists of an OTA, a D Flip-Flop chain, and a programmable capacitor array. One of the principal uses of an OTA is to construct a G_m-C filter. The construction of a filter requires the use of capacitors of various values at the output of the OTA. The capacitor in a G_m-C filter controls the corner frequency of the filter. Increasing the capacitance lowers the corner frequency and decreasing the capacitance increases the corner frequency. Having the ability to change the capacitance of the G_m-C filter would allow the corner frequency to be changed to match the frequency for a desired application, such as wireless communication on the ISM band. As a result, a programmable capacitor array can be used. One of the benefits of G_m-C capacitors is that they can be grounded. This means that another bias voltage is not needed, and that adding more capacitance is easier since there is a common voltage for all of the capacitors, in this case ground.

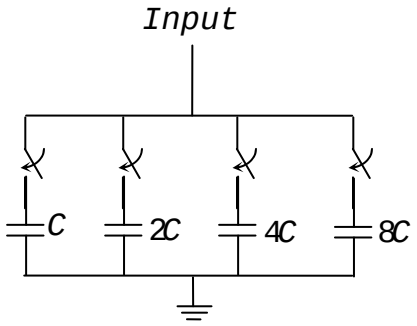

Figure 3-15 - Capacitor Array

The capacitor array consists of four capacitors connected in parallel as shown in Figure 3-15. This binary capacitor array allows for the fine tuning of filter bandwidth. One of the capacitor arrays is included at each of the OTA outputs. The unit capacitance used in this array was approximately 26.6 fF resulting from an equal length and width of a NMOS capacitor. This was the design kit's default size of the NMOS capacitor, and the symmetry of the design allowed for easy scaling of the capacitance by increasing the length and the width. The switches in Figure 3-15 are transmission gates, shown in Figure 3-16, controlled by the outputs of the shift register. This allows the switches to be programmed digitally by the end user of the CAB.

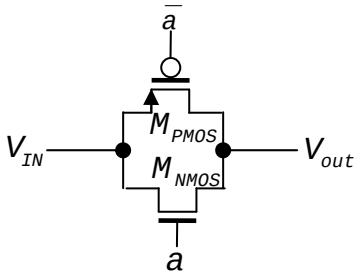

Figure 3-16 - Transmission Gate

Transmission gates allow for transmission of signals from V_{IN} to V_{out} without problems arising from the threshold voltage of the PMOS or the NMOS

transistors [6]. The transmission gates used in this thesis have an ON resistance of 125 Ω and an off resistance of 62 kΩ. The operation of the transmission gate shown in Figure 3-16 is displayed in Figure 3-17.

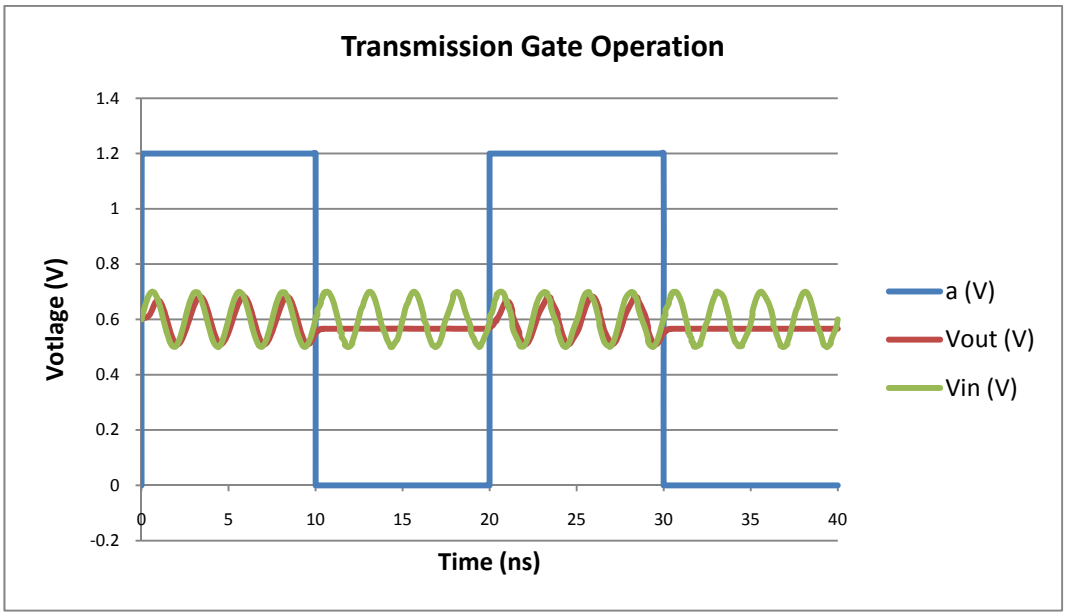

Figure 3-17 - Transmission gate operation, transient SPICE simulation, the top signal shows the clock signal in blue, the input signal in green, and the output of the transmission gate in red.

Combining these components yields the design shown in Figure 3-18. The placement of the switches allows each of the inputs to be selected, as well as to have feedback from the outputs to the inputs. This design also allows for the OTA

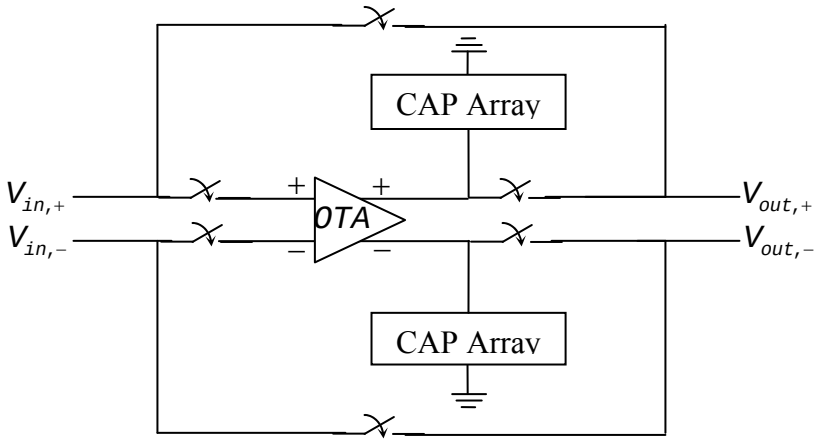

Figure 3-18 - CAB Overview. This shows the generic block diagram of the CAB. The switches shown here are implemented with transmission gates and controlled with a shift register.

to be bypassed completely if the need is there to create the appropriate analog circuit.

Figure 3-18 shows a design which requires 14 bits of memory. Six switches control the routing around the OTA, and then another eight switches control the capacitor arrays. Therefore, the memory is then controlled with a 14-bit D Flip-Flop chain and 14 transmission gate switches.

Not all of the 64 states available from the routing switches are defined. However, using a single bit to control each of the switches allows for more flexibility in testing and application than reducing the number of bits and defining only a few states.

Once the CABs are placed in the array, then controlling the routing between the different CAB cells creates different analog circuits.

3.2.1 CAB Circuits

The operation of the OTA *in situ* can be demonstrated using the test bench shown in Figure 3-19. The test bench in Figure 3-19 shows 2 OTAs connected together in a negative feedback configuration with current inputs.

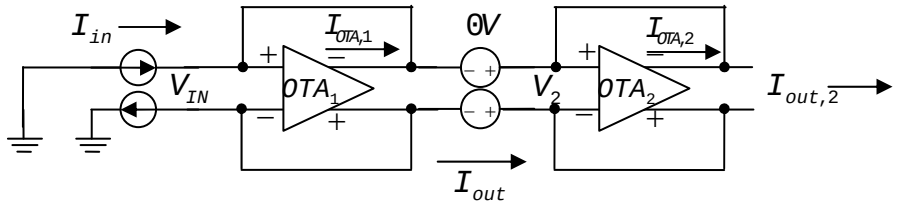

Figure 3-19 – This figure shows a test bench of the OTA in a negative feedback configuration. This tests the OTA for functionality *in situ*.

Describing the current gain (A_I) in Figure 3-19 requires 2 assumptions. The first assumption is that the OTAs are ideal. An ideal OTA has no current entering the input, which means,

$$I_{out} = I_{IN} + I_{OTA,1} \quad \textbf{(3-XIV)}$$

$$I_{out,2} = I_{out} + I_{OTA,2} \quad \textbf{(3-XV)}$$

Since the output of OTA_2 is left floating,

$$I_{out,2} = 0 = I_{out} + I_{OTA,2} \quad \textbf{(3-XVI)}$$

$$I_{out} = -I_{OTA,2} \quad \textbf{(3-XVII)}$$

Also using the assumption that the OTAs are ideal,

$$I_{OTA,1} = G_{M,1}V_{IN} \quad \textbf{(3-XVIII)}$$

$$I_{OTA,2} = G_{M,2}V_2 \quad \textbf{(3-XIX)}$$

Where $G_{M,1}$ and $G_{M,2}$ are the transconductances of OTA_1 and OTA_2 respectively. It is also known that,

$$V_{IN} = V_2 \quad \textbf{(3-XX)}$$

The second assumption is,

$$G_{M,1} = G_{M,2} \quad \textbf{(3-XXI)}$$

Therefore, using equations (3-XVII), (3-XVIII), (3-XIX), (3-XX), and (3-XXI),

$$I_{OTA,1} = G_{M,1}V_{IN} = G_{M,2}V_2 = I_{OTA,2} = -I_{out} \quad \textbf{(3-XXII)}$$

And using equations (3-XIV) and (3-XXII), the current gain can be solved for.

$$I_{out} = I_{in} - I_{out} \quad \text{(3-XXIII)}$$

$$A_I = \frac{I_{out}}{I_{IN}} = \frac{1}{2} \quad \text{(3-XXIV)}$$

The currents simulated in Cadence are shown in Figure 3-20. The currents are shown in a transient simulation with the input current having a frequency of 400 kHz and amplitude of 49.3 nA. The output current has an amplitude of 24.65 nA, half of the input current and as predicted by equation (3-XXIV).

The analysis of the AC voltage characteristics are shown in Figure 3-21. This analysis demonstrates the functionality of the test bench shown in Figure 3-19.

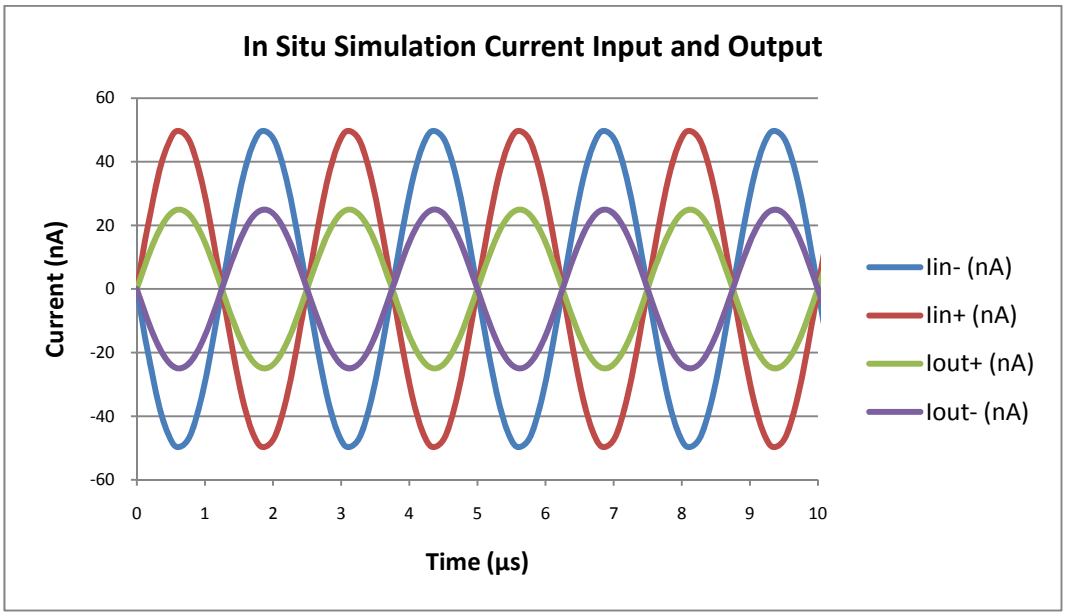

Figure 3-20 - This graph demonstrates the current gain of the test bench shown in Figure 3-20. The input current has an amplitude of 49.3 nA with a frequency of 400 kHz and the output current has an amplitude of 24.65 nA.

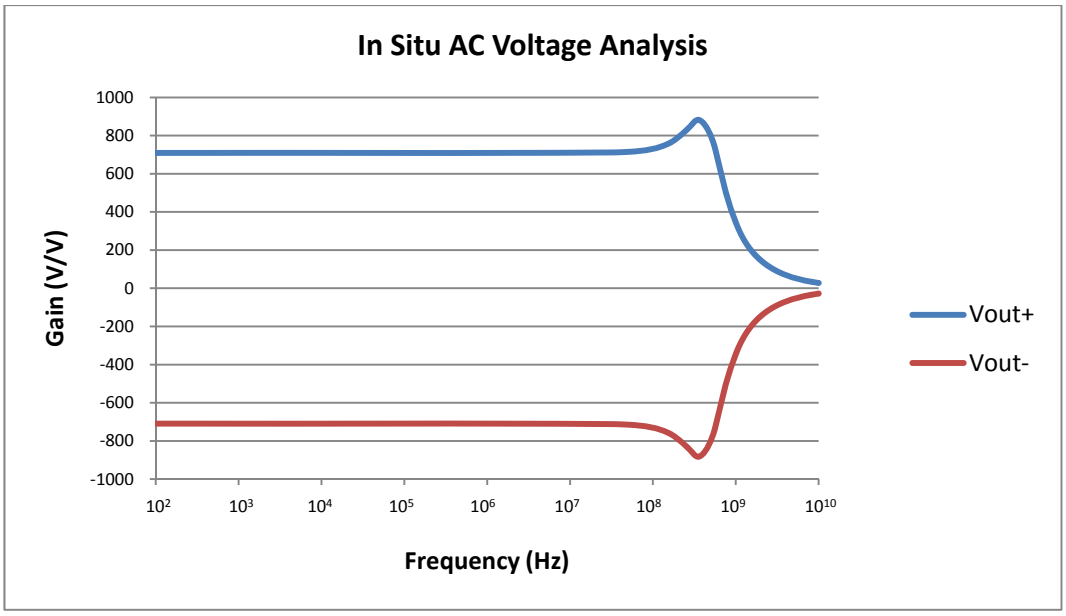

Figure 3-21 - This graph shows the AC analysis of the test bench shown in Figure 3-20. It demonstrates the functionality of the test bench in terms of the AC voltage response

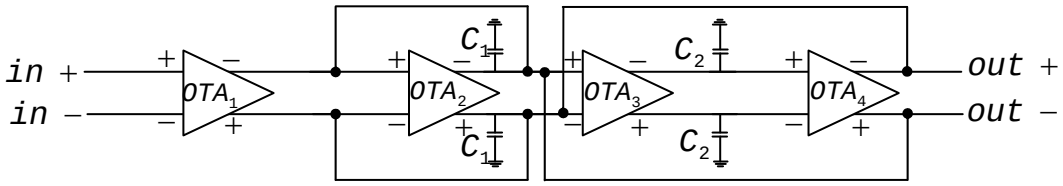

Figure 3-22 - Band-pass filter configuration using 4 CABs

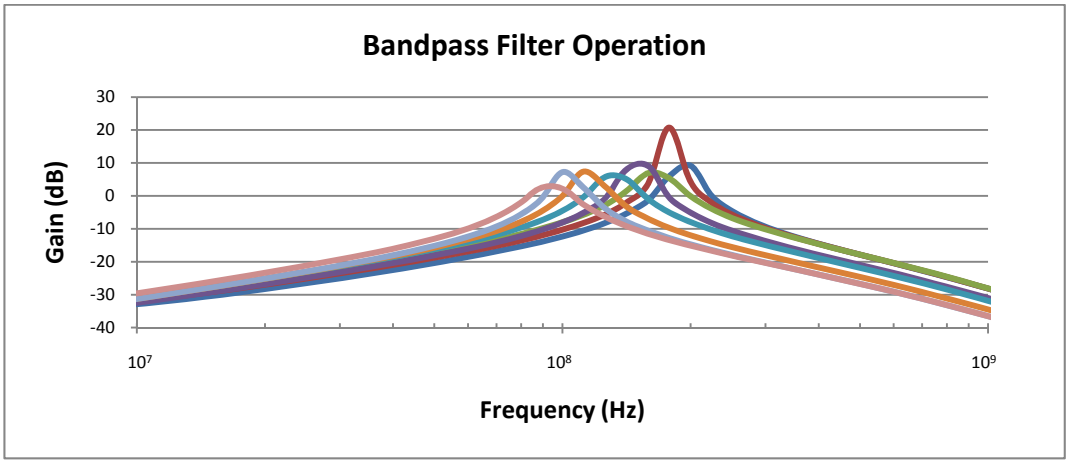

Figure 3-23 - This graph shows the operation of band-pass filter at select frequencies. The centre frequency of the band-pass filter ranges from 89.1 MHz to 200 MHz, with bandwidths ranging from 2.31 MHz to 59.7 MHz by controlling the capacitance from the capacitor arrays in the four CABs used to create the band-pass filter.

A band-pass filter is often useful in selecting different frequencies in communications systems. Connecting 4 of the CABs together can yield a band-pass filter.

Figure 3-22 shows the band-pass filter configuration of OTAs, and Figure 3-23 shows the operation of the band-pass filter at select frequencies. C_1 in Figure 3-22 are formed from the capacitor arrays from the CABs for OTA_1, OTA_2, and OTA_4, while C_2 is formed from the capacitor arrays from the CAB for OTA_3. Changing the capacitance of the capacitor arrays alters the centre frequency of the band-pass filter as can be seen from the transfer function of the band-pass filter shown below in equation (3-XXV) [26],

$$\frac{V_{out}}{V_{in}} = \frac{\frac{sG_{m4}C_1}{G_{m1}G_{m2}}}{\frac{s^2C_1C_2}{G_{m1}G_{m2}} + \frac{sG_{m3}C_1}{G_{m1}G_{m2}} + 1} \qquad \textbf{(3-XXV)}$$

The highest frequency occurs when most of the capacitance is switched off, while the lowest frequency occurs when all of the capacitance available is switched on. The final amount of capacitance used is selected based on the end use of the filter. The band-pass filter ranges from a centre frequency of 89.1 MHz up to a centre frequency of 200 MHz, and the -3 dB bandwidths of the band-pass filter ranges from 2.31 MHz to 59.7 MHz. The Q-factor of the band-pass filter ranges from 2.48 to 41.0.

3.3 Field-programmable Analog Array

There are various forms of interconnection networks that can connect the different CABs together in the FPAA. The most flexible routing method is a crossbar interconnection network [21].

The crossbar interconnection network connects all of the elements together, allowing for any two elements to be connected [21] [55]. This provides a large amount of flexibility compared to other interconnection networks such as a hierarchical (multistage) network. The cost of a crossbar interconnection network is area and a large amount of parasitics introduced by all of the dangling switches. The crossbar network exhibits a complexity of $O(N^2)$ where N inputs are being connected to N outputs [21]. Other routing methods may save on area, most notably the hierarchical interconnection networks.

Hierarchical interconnection networks use a number of switch stages to connect the different cells together [60]. Some of the most popular multistage networks include Banyan, omega, and delta [61] [62] [63]. The major advantage of the multistage networks is the reduction of area when compared to the single stage of the crossbar network, since the area has a complexity of $O(N \log N)$ [21]. The major disadvantage of the multistage network is that the signals traveling through the interconnections must travel through multiple stages (layers) to reach their final destination, and the signal cannot travel between elements of the same layer [21] [64]. This results in some loss of performance in the routing network;

however, the savings in the area consumed by the interconnection network can often make up for the loss in performance.

For the design of this FPAA, a mesh network was considered. The mesh network connects the elements of an array to its nearest neighbour. Figure 3-24 shows a 4 × 4 mesh network of CABs with two inputs and two outputs. This design offers many of the benefits of the crossbar network in terms of flexibility, but does not take up as much area or introduce as many parasitic as a full crossbar network.

The design of our CAB allows for blocks to be bypassed, and therefore any number of CABs can be used in a design. If a simple amplifier or filter is desired then only one CAB needs to be implemented; however, if a fourth-order filter is required, the correct number of CABs can be connected together.

The design of the networking also requires memory to control the switches between the configurable analog blocks. As with the switches in the CABs, the switches used to control the routing between the cells are transmission gates. Again, this helps to eliminate problems with the threshold voltages of the PMOS or NMOS transistors.

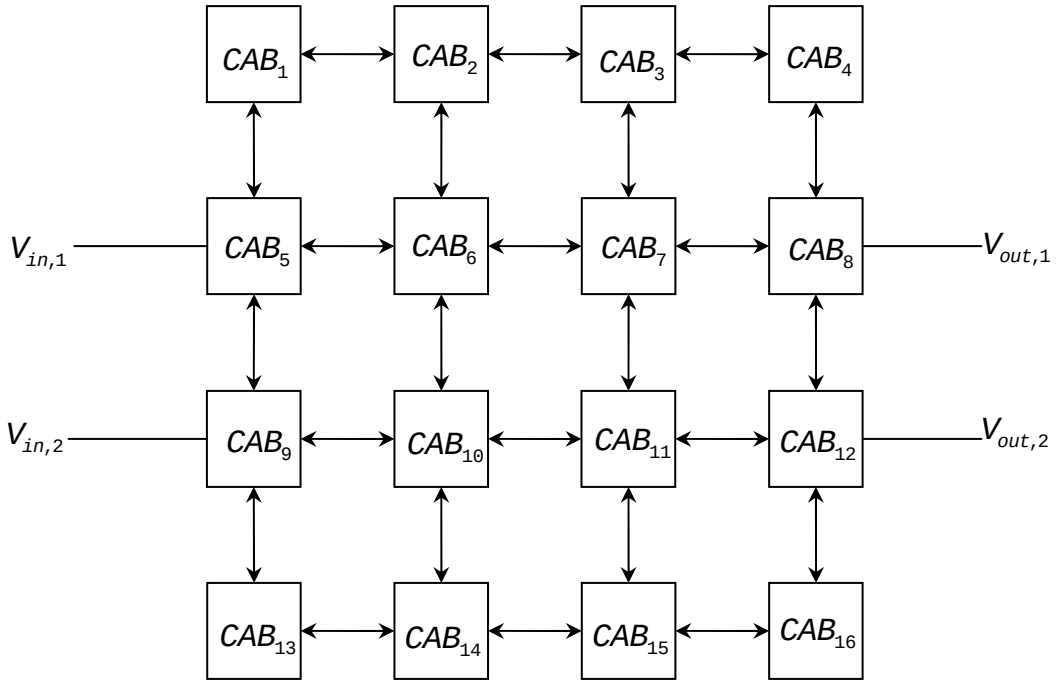

Figure 3-24 – 4 × 4 Mesh Network. This network of CABs connects each CAB to its neighbour as shown in Figure 3-25. This keeps from using a large crossbar network which consumes a large amount of area and introduces lots of parasitic without sacrificing a lot of flexibility.

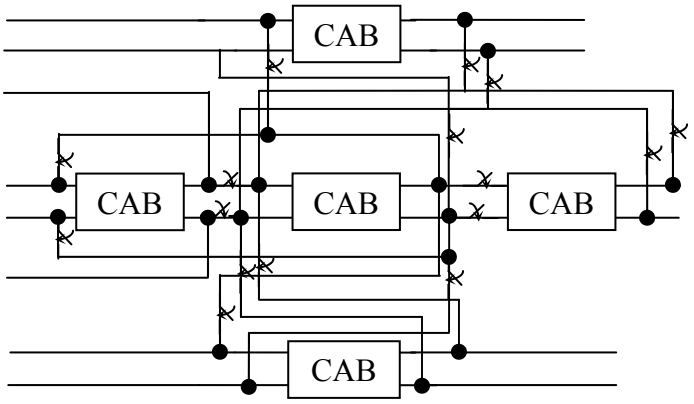

Figure 3-25 – Local interconnection between neighbouring CABs, where each switch represents a configurable transmission gate.

In the 4 × 4 array design of CABs shown in Figure 3-24, which are wired as in Figure 3-25, the routing requires a total of 192 switches. While using a shift register to program the entire CAB would allow for serial programming of the

entire FPAA. If the switches in the CABs are included in the chain, then the number of flip-flops required grows to 416. One flip-flop occupies 40 μm^2; therefore, for an array of 4×4 CABs, the flip-flops would occupy 640 μm^2.

There are supporting elements may be included in future designs of the FPAA as well. All of the CABs contain a capacitor array; however, some applications require larger capacitor arrays or capacitor arrays with finer granularity than the capacitor arrays provided in the CABs. As a result, some of the CABs can be replaced with a larger capacitor array before fabrication. Along the same line, other supporting elements may be implemented. A phase-locked loop (PLL) is useful in many signal processing applications, as well as interfacing with digital components and a fixed PLL may be included rather than implementing one using CABs. Other useful components include inductors for use in filtering and signal matching, and resistors, which are useful for filtering and amplification.

To avoid wasting silicon and to help debug problems with the CAB, the full FPAA design was not implemented. Instead a single CAB was implemented on silicon to test the capabilities of the OTA and the viability of the CAB design for use in a full FPAA implementation.

3.4 Final Integrated Circuit Implementation

An IC design for a single CAB design was fabricated. Implementing a single CAB allows for easier testing of the CAB design in view of a future full implementation.

In addition to the single CAB, the IC requires a current mirror for proper operation of the OTAs. Also, current mirrors helped to eliminate some pads from the design. 20 pads were available on the chip, and not using current mirrors would have required at least 3 pads, one for each amplifier, rather than the 2 pads used for the current mirror. An off-chip reference current is provided for the IC, and current mirrors distribute the current to the OTAs, and scale the currents for the OTAs. The reference current was placed off-chip to help control the current more accurately and remove one variable from the chip for testing purposes.

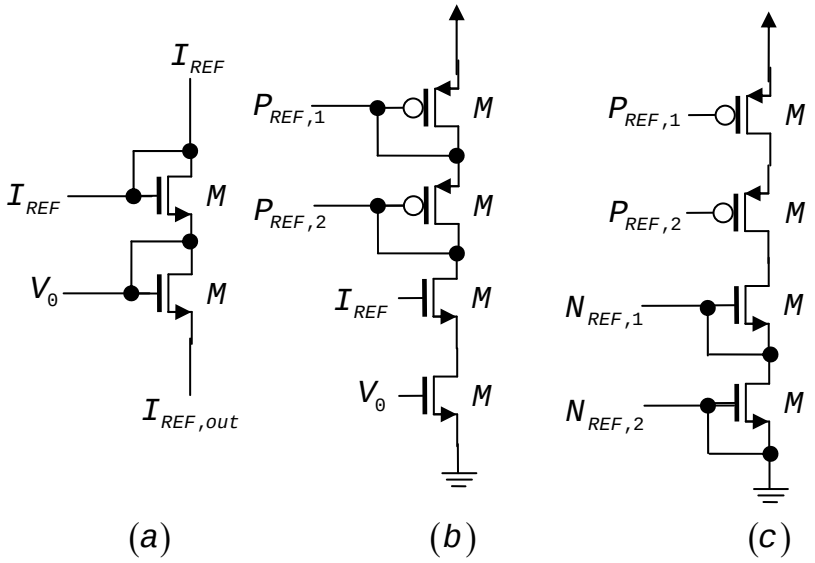

Figure 3-26 - (a) input current mirror (b) PMOS circuit mirror (c) NMOS circuit mirror

Figure 3-26 shows the current mirror circuits used in the design of this chip. The first mirror, shown in (a), receives the input from an external current source. An external current source helps eliminate a variable in the design of the CAB, and the design of a current mirror is not the focus of this thesis. The second mirror, shown in (b), mirrors the current to the circuits driven by a PMOS mirror, and (c) shows the mirror used to distribute the current to all of the NMOS mirrors.

Using the cascoded current mirror helps to eliminate channel length effects from the transistors [6]. The disadvantage of using the cascoded current mirror is the increase in overhead voltage of the circuit [5] [6]. Originally, a single transistor current mirror was used to transfer the voltages to the rest of the circuit; however, the single current mirror did not have the driving power in this process. As a result, the cascoded current mirror was used.

An external power supply combined with voltage dividers provided the bias voltages required by the OpAmp. Having the voltages off-chip allows for easier testing of the chip: first, an error in an on-chip voltage divider would be difficult to detect, and second off-chip voltages allow for more accurate control of the bias voltages in order to fine tune the values to respond to process variations. While the final design of the FPAA will likely provide the bias voltages on-chip, it was more beneficial to have them off-chip in the design of the CAB.

3.5 Summary

This chapter presents the design of a fully differential cascode amplifier to be used as an OTA in a CAB. The fully differential design offers more flexibility and better noise immunity than a single ended OTA. The cascode design also offers better gain over a single stage than other amplifier designs.

The first OTA design was stable and had sufficient frequency response with a -3 dB bandwidth of 21.91 MHz and power consumption at 173.5 μW, although the gain of the amplifier was lower than desired at 38 dB. As a result, a gain-boosted OTA was designed in an effort to increase the DC gain. The gain-boosted design increased the gain of the OTA to 58 dB, above the desired 50 dB, but the frequency response had a -3 dB bandwidth of only 31.05 kHz as well as an unstable response and a power consumption of 405.6 μW. Finally, the original design without gain-boosting was altered to increase the gain to 50 dB with a -3 dB bandwidth of 1.217 MHz and a GBW of 384.8 MHz while only consuming 156.2 μW of power.

A CAB was presented which used transmission gate switches to alter the circuit configuration of the CAB and also a capacitor array at each output. The capacitor arrays allowed for fine tuning of the frequency response of the CAB. The CAB design was then shown to implement a band-pass filter using CABs. This design offered a range of centre frequencies from 89.1 MHz to 200 MHz by altering the capacitances from the capacitor arrays.

Chapter 4

Chip Implementation

This thesis presents a custom design of a high-speed CAB for FPAA design. The philosophy behind the design was to use blocks which could be replicated throughout the design, similar to the design of a full-scale FPAA where the CAB is replicated many times. This can be seen in the design of the gain-boosting amplifiers, the transmission gate switches, the D flip-flops, and the capacitor arrays, all of which are replicated multiple times in the CAB layout.

Design libraries in our IBM 130 nm CMOS technology provided all of the components used in the circuit designs presented in this thesis. Using some of the basic components provided in the design kit, such as pre-drawn transistors, resistors, and capacitors, makes designing the required circuits easier than drawing these components from scratch. As a result, the LayoutXL tool included with Cadence allows the easy incorporation of pre-designed components.

The LayoutXL tool places all of the included components into the layout. The components were then organized to help eliminate as many wires as possible, and reduce the length of the interconnections. The interconnections get drawn by hand. The resistance must be considered and capacitance when drawing the interconnections. As a result, symmetry and balance needs to be the primary

design consideration when drawing the wires. Also, large connections require multiple vias to help reduce the errors that can develop in fabrication.

4.1 Folded-Cascode Operational Amplifier

Section 3.1 describes the design of the folded-cascode OpAmp. This section describes the layout of the OTA and some of the challenges encountered in the design of the OTA. The first design was the gain-boosting single-ended OTAs.

4.1.1 Gain-Boosting OTAs

The gain-boosting OTAs are small blocks used in the design of the fully differential OTA, which is used as the basis for the CAB. The schematics used as the basis for the layout were shown in Figure 3-4 and Figure 3-5.

The layout began with synthesizing the transistors in the design with the LayoutXL tool. This created the pads that were needed for the inputs and outputs of the circuit. Then the transistors were then connected in such a way as to combine the active regions where possible. This helps to eliminate some of the resistance between the two transistors and reduce the space consumed by the interconnection.

Two layouts were designed for gain-boosting OTAs. The first design was a PMOS based input pair. The PMOS input pair works better for the input into lower voltage levels, like those seen on the NMOS transistors in the differential OTA. A PMOS input pair has the ability to accommodate common mode levels as

low as zero [6]. As a result, the PMOS input pair design biased the NMOS transistors, and the Bode plot for the finished OTA is shown in Figure 4-1.

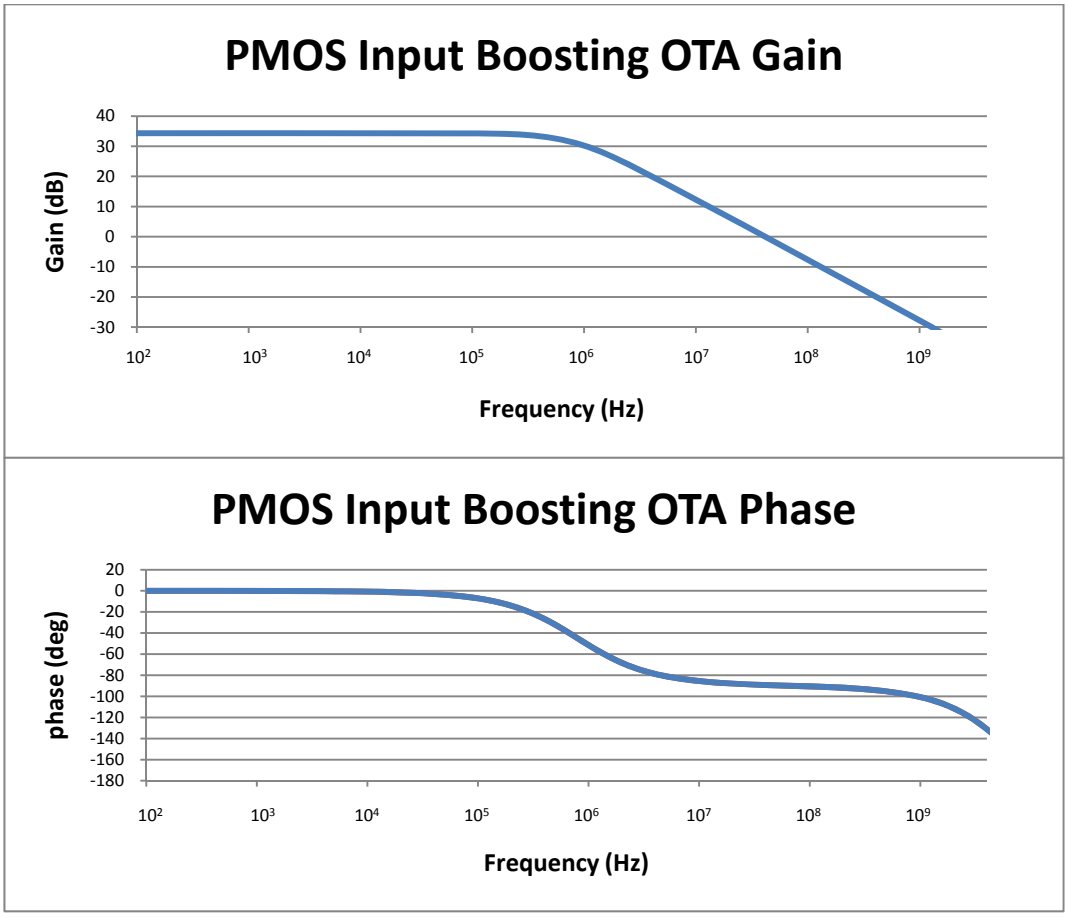

Figure 4-1 - Bode plot of PMOS input pair gain-boosting amplifier. The gain of the amplifier is 34 dB with a -3 dB point of 730 kHz and a unity gain frequency of 45 MHz and a phase margin of 90°.

The second layout uses an NMOS input pair. Just as the PMOS is ideal for use in lower voltage levels, the NMOS pair can operate with higher input voltage levels, up to VDD [6]. As a result, the NMOS input pair biased the PMOS transistors with the Bode plot of the OTA shown in Figure 4-2.

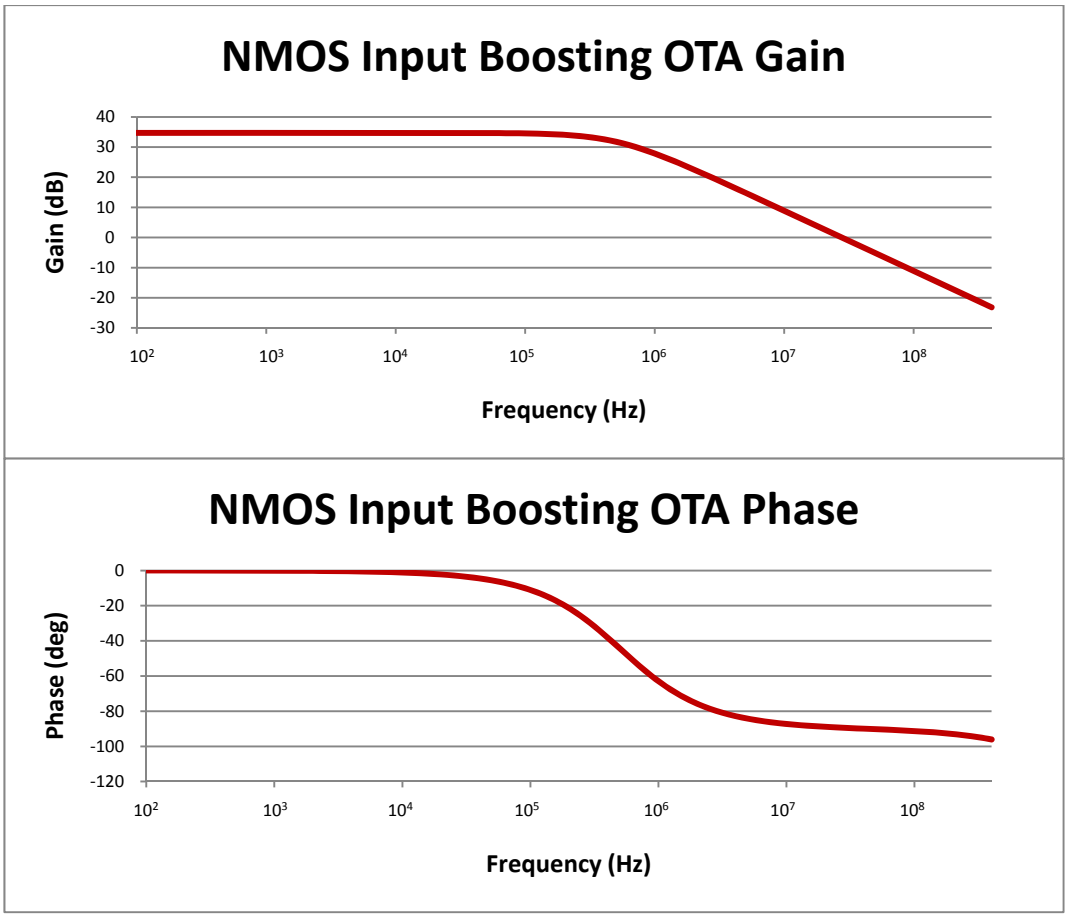

Figure 4-2 – This graph is the Bode plot of NMOS input pair gain-boosting amplifier. This biasing OTA has a gain of 35 dB with a-3 dB bandwidth of 500 kHz, a unity gain bandwidth of 28 MHz and a phase margin of about 90º.

The layout of the gain-boosting amplifiers provided little trouble in design. Since the amplifiers were used to bias transistors, the bandwidth was not nearly as important as the bandwidth in the differential OTA. In order to keep the designs similar, the distance between the V_{DD} and V_{SS} rails was kept to 7 µm. The final PMOS input design had an area of 7 × 4.92 µm^2, as shown in Figure A-6 with the schematic shown in Figure B-6 while the NMOS input design had an area of 7 × 5.08 µm^2 as shown in Figure A-7 with schematic shown in Figure B-7.

4.1.2 Differential Operational Transconductance Amplifier

Multi-fingered transistors were used to keep the size of some of the transistors down. Also, the multi-finger transistors help to reduce the gate resistance of the transistors. In general, the gate resistance should be around $1/10^{th}$ to $1/5^{th}$ of $\frac{1}{g_m}$ [6]. In the case of the multi-finger transistors, the gates, sources, and drains needed to be connected together. Often the connections led to the use of long strips of poly and metal, balancing these traces with vias help to limit offsets. Another good practice was to include multiple connections along these traces to help minimize the effect of process variations, and to help balance the circuit.

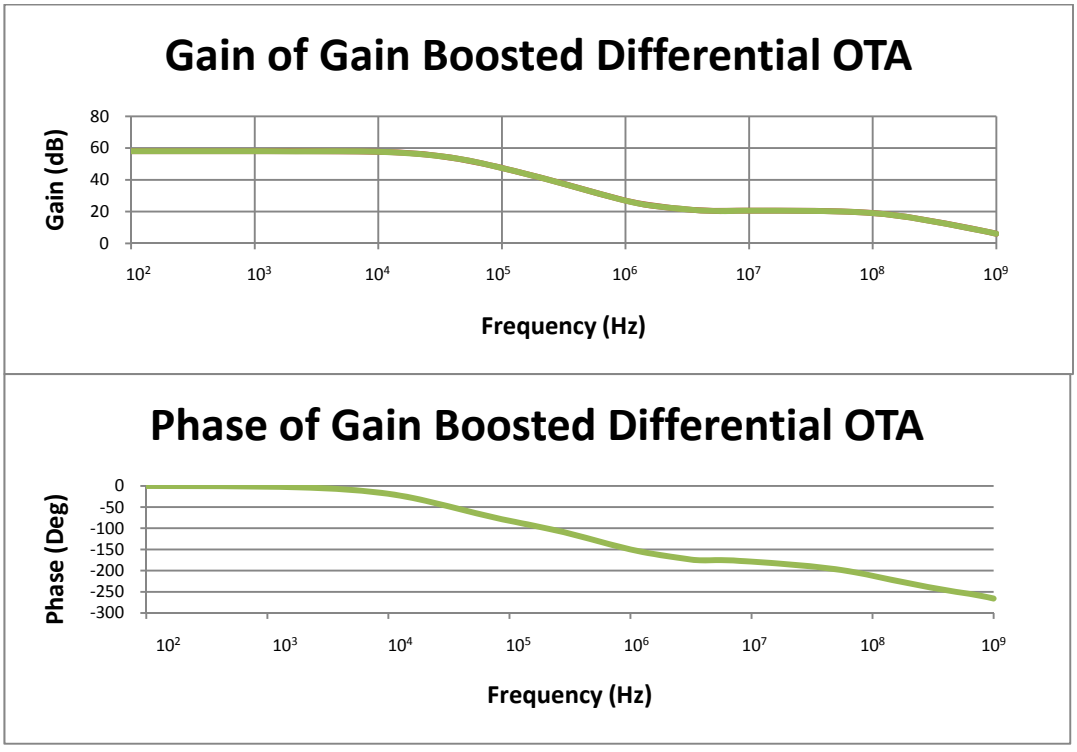

Figure 4-3 – Bode plot of gain boosted differential OTA. This final gain-boosted amplifier has a gain of 58 dB with a -3 dB bandwidth of 31 kHz and unity gain bandwidth of 2 GHz. However, the phase graph shows that the OTA is unstable.

The gain of the OTA shown in the Bode plot in Figure 4-3 was measured by simulating an input AC voltage of 1 V at the positive input, and the corresponding voltage gain at the output across a 1 fF capacitor at the negative output. The final layout is shown in Figure A-4 with the schematic shown in Figure B-4 and Figure B-5.

4.2 D Flip-Flop

The D flip-flops in this design were used to control the switches in the CAB. This gives control over the configuration of the circuit to the digital domain, making the CAB easier to interface with computers and to control. Unfortunately, no libraries were available at the University of Alberta during the design of the chip presented in this thesis to provide a premade version of a flip-flop for use in the design. As a result, a true single phase clocking (TSPC) D Flip-Flop design was created from scratch using the schematic shown in Figure 4-4 and Figure B-8.

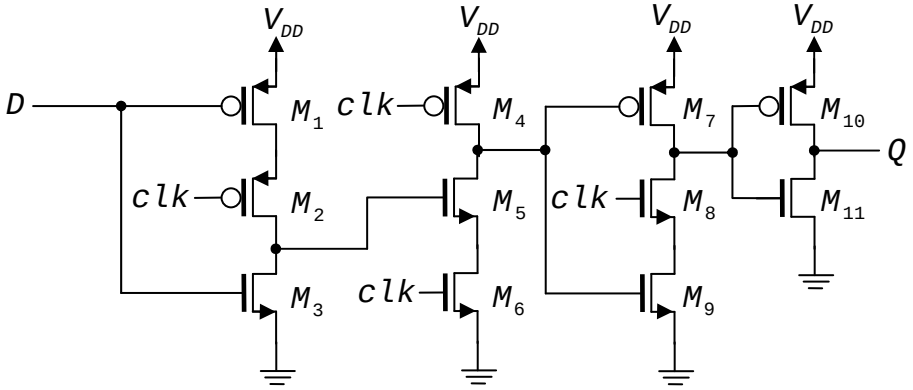

Figure 4-4 – TSPC D flip-flop schematic

The initial flip-flop design used a rising edge triggered D flip-flop. The first step was to use LayoutXL to synthesize the transistors in the layout from the schematic. The PMOS and NMOS transistors were combined into their own areas

respectively. The design of the layout only used the poly layer and one metal layer. Reducing the number of layers used allowed us to easily combine the flip-flops without crossing the traces used to layout the single D flip-flops. The single D flip-flop occupied an area of $6.43 \times 5.89\ \mu m^2$.

However, this D flip-flop is a dynamic design. The data in the shift register needs to be refreshed periodically, otherwise the data is lost. The retention time was simulated by shifting in a series of 1's into a flip-flop and then freezing the clock high and low. The retention time is the time taken for the stored data to drop V_{th}. The design used in this thesis has a retention time of 58 μs when the clock is held low and 90 μs when the clock is held high. Using a dynamic D flip-flop for the shift register was a mistake and is quite likely a possible cause for the failure of the final chip design.

A shift register was then created using a chain of 14 flip-flops. The 14 flip-flops control all of the switches in a CAB. Having a layout of a 14 flip-flop chain allows us to easily combine the available memory for the CAB with the OTA design. An array of 2×7 flip-flops was connected with V_{SS} running in between the two rows and V_{DD} running around the outside. Connecting the flip-flops together using the second metal layer, avoided any cross connections when routing over the flip-flops. There is a clock line, which connects all of the clock inputs for the different flip-flops. Each of the transmission gates controlled by the flip-flops requires an enable signal and an inverted enable signal; therefore, the

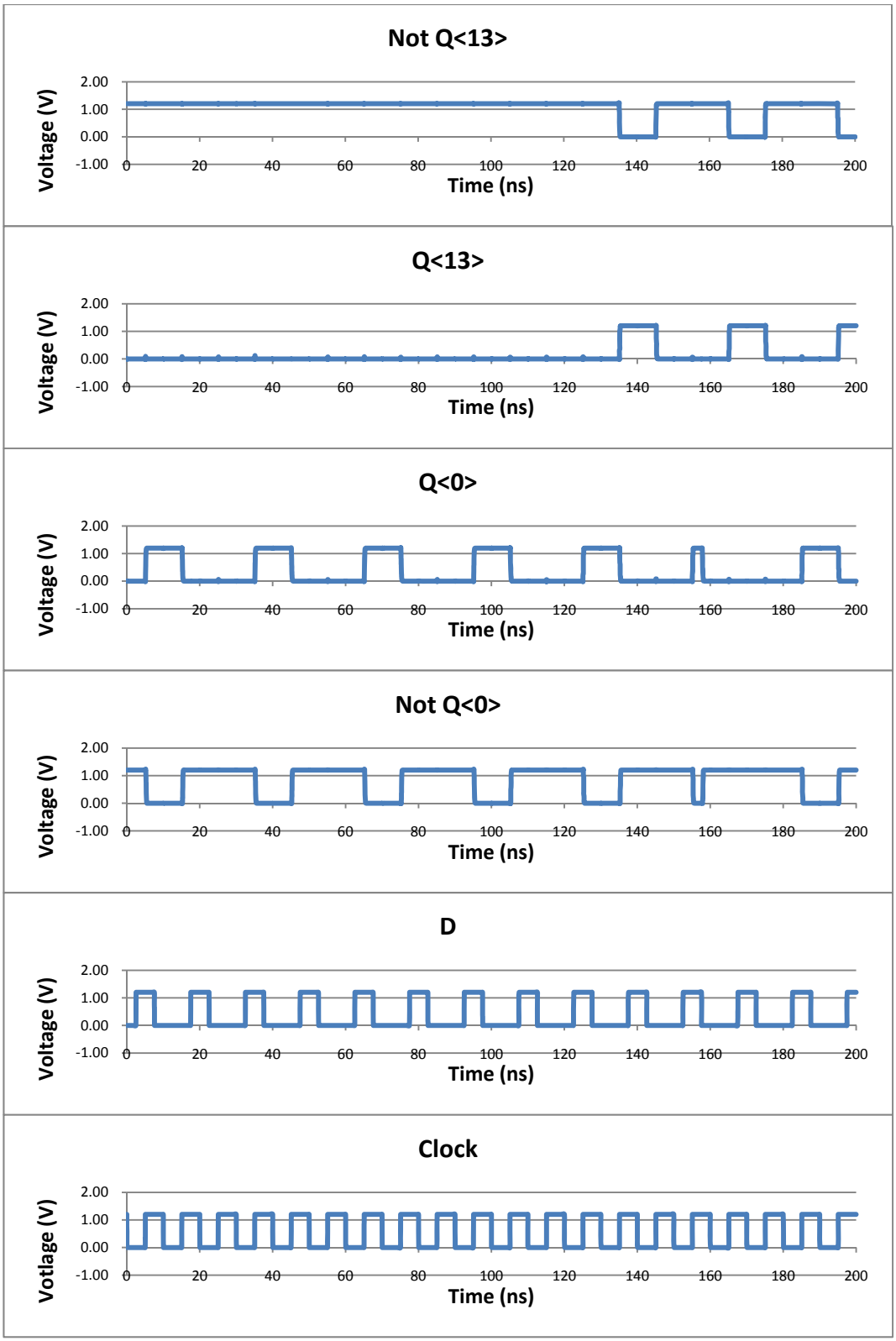

Figure 4-5 - Operation of shift register following the propagation of an input signal *D* through the shift register.

output Q of the flip-flops connects to an inverter and the next flip-flop in the chain to propagate the bit signal. The full operation of the shift register is shown in Figure 4-5 and shows the propagation of bits through the shift register. Overall, the full flip-flop chain occupied an area of $56.25 \times 12.86\ \mu m^2$.

4.3 Configurable Analog Block

The CAB layout includes the layouts from the flip-flops and the differential OTA as described above. It also includes the layout of the transmission gates to provide switches.

The transmission gate layout used relatively large transistors compared to the transistors used in the OTAs. To help keep the gate resistance of the transistors in check, multi-finger transistors were used like in the OTAs. Overall the transmission gates occupied an area of $12.16 \times 4.29\ \mu m^2$.

The capacitor array was chosen to contain only 4 capacitors to help keep the size down. The smallest capacitor has a capacitance of 26 fF and the largest capacitor has a capacitance eight times larger at 213 fF. This capacitor array, allows for digital control, and is also controlled by transmission gates. The capacitor array without any of the switches, measures in at $14.65 \times 11.26\ \mu m^2$. With the switches in place, the capacitor array measures $19.19 \times 23.86\ \mu m^2$. Two of the capacitor arrays are included in each of the CABs, one array on each of the outputs.

The capacitor arrays were balanced on either side of the OTA, although most of the switches were concentrated on the right side of the OTA. The final area of the CAB with the capacitor arrays, switches, and differential OTA was 46.08 × 83.23 μm^2.

The memory was attached to the CAB. 2 layers of metal were used while attaching the outputs from the flip-flop chain to the switches. This involved attaching the outputs from both the flip-flops and the inverters to the NMOS and PMOS transistors of the transmission gates respectively. This ended with the CAB occupying an area of 83.23 × 70.31 μm^2.

4.4 Final Chip Design

The final chip design used the CAB layout combined with a current mirror. The current mirror used a selection of mirrors based on an input reference current as shown in the previous chapter. The mirror from the input reference current and the base current mirrors, the ones that provided a reference for the rest of the chip occupied an area of 16.24 × 17.72 μm^2 and is shown in Figure A-3.

The final chip layout also included a pad frame. The design libraries provided the frame provided, and provided the required surrounding metal layers. However, the pad frame did not include pads; therefore, the pads needed to be designed. The pad design began with the provided bond pad. The bond pad provides a place to solder the bond wires to the chip, connecting the chip to the packaging. The chip

also needed some electrostatic discharge (ESD) protection. When an IC interacts with the outside world there is a possibility of ESD, which can be potentially damaging to the chip. In order to prevent this, a set of diodes clamps the discharge to V_{SS} or V_{DD} as shown in Figure 4-6. In this case, the discharge was clamped to V_{DD}.

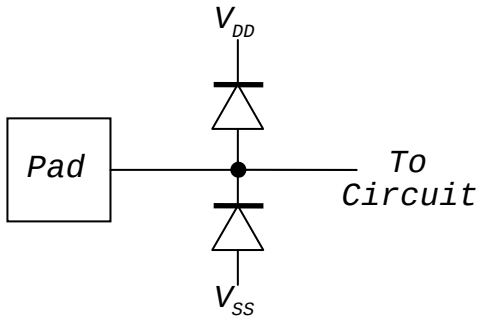

Figure 4-6 - ESD Protection

The pads used in this layout were created using a bond pad provided in the standard library, and were combined with a double diode ESD protection circuit also provided with the standard library. In addition, each of the pads required a tie down to the substrate. Connecting the bond pad to the substrate involved connecting it down through each of the metal layers. The final metal layer was then connected to the substrate through a guard ring.

Twenty pads were placed around the outside of the design. The pads were evenly distributed, with five pads on each side of the chip. Then, the pads were connected to the needed pins on the inside of the circuit. Wide wires connect the internal pins to the external pads. Using wide wires to connect to the external pads helps

to lower the resistance from the pads to the internal circuitry. The final design occupied an area of 1 × 1 mm^2, and the final implemented design is shown in Figure 4-7, and the layout is shown in Figure A-1 with the schematic in Figure B-1 showing the connections to the pads, Figure B-2 showing the connection of the CAB to the shift register, and Figure B-3 showing the schematic of the CAB.

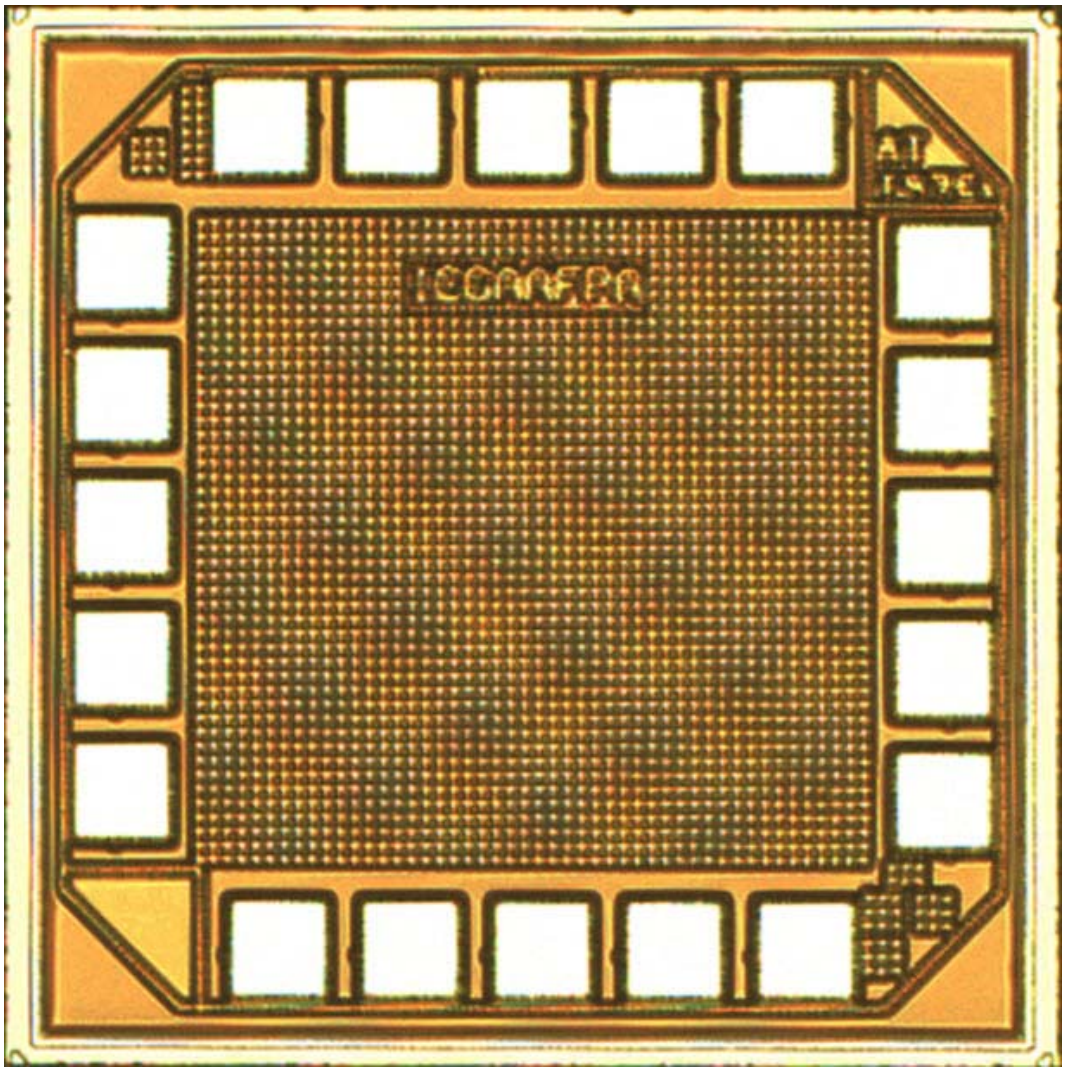

Figure 4-7 - Die photo of completed chip with metal fill

4.5 FPGA Interface

A PC was used to analyze the data from the FPAA. Unfortunately, because a PC works digitally, the FPAA required an interface to connect to the PC. An FPGA board allowed us to connect the FPAA to the PC. The FPGA board provides a reconfigurable architecture to adapt to the chip and allow testing. Also, in order to measure the analog signals from the FPAA design, the FPGA requires an ADC to translate the analog signals to digital signals that can be read by the PC.

The FPGA chosen to provide the interface was a Xilinx Spartan 3E-100, mounted on a Digilent Basys2 board. The Spartan 3E provides a low cost, flexible FPGA [65]. The Digilent Basys2 board permits easy interfacing between the Spartan 3E and the PC through a universal serial bus (USB) interface, and it also provides 4 6-pin input/output (I/O) headers [66]. The 6-pin headers are also compatible with the Digilent Pmod accessory circuit boards [66]. The Pmod accessory boards include an ADC and a DAC board, as well as the supporting very-high-speed IC (VHSIC) hardware description language (VHDL) to interface the Basys2 board with the Pmod boards [67] [68].

The Pmod accessory boards provide an easy way to connect additional supporting circuits to the FPGA development board. For this research, the FPGA board needs to have access to an ADC and a DAC. The ADC Pmod provided by Digilent uses 2 12-bit ADCs from National Semiconductor [69] [70]. Having two ADCs available on a single board allows for both differential signals on the amplifier to

be connected to the FPGA, without needing to have two separate boards, risk losing some accuracy by splitting processing the signals, or only processing one of the signals. Similarly, the DAC Pmod provided by Digilent contains 2 12-bit DACs from National Semiconductor [71] [72].

In addition to providing a place for the Pmod accessories, the 6-pin headers provided on the Basys2 board can also be controlled to provide digital outputs or inputs if needed. In this case, 1 of the 6-pin headers is used to provide an input for the D Flip-Flop chain.

Using an FPGA allowed the storage of test vectors to check the functionality of the CAB. The FPGA can send test vectors through the DAC to the CAB, and the FPGA can receive the responses from the CAB through the ADC. These responses can then be stored in memory on the FPGA and retrieved later by the PC via USB connection for analysis. The FPGA can also control the flip-flop chain. The FPGA can store test vectors for configuring the CAB and then sent to the CAB to control its circuit configuration. The Basys2 board provides a set of manual switches and buttons which, can program the CAB on the fly.

VHDL used for testing was based on the VHDL provided by Digilent. The provided code supplied subroutines to connect with the Pmod accessory boards as well as the basic support structure to interact with the Basys2 board. Modification of this code allowed us to develop the necessary programming to test the CAB

design on the chip the code could easily be designed with the Xilinx ISE Design Suite, and then the Adept software from Digilent loads the VHDL on to the Spartan 3E FPGA on the Basys2 board.

The first set of VHDL code programmed the shift register on the FPAA, which controls the configuration of the circuit on the CAB. A state machine was developed to provide a programming interface between the FPGA and the CAB, through 1 of the 6-pin headers. A clock signal shifts the data out from the FPGA the shift register. The clock is offset by half a cycle from the data signal. This prevents any setup and hold time violations. The FPGA generated the clock signal by dividing the 50 MHz signal the FPGA uses as a clock. The FPGA can send the 50 MHz clock directly to the FPAA, or the FPGA can send a divided clock signal. A clock signal from 2 MHz down to 3 Hz was tested. The shift register required a clock frequency of at least 13 kHz for proper operation based on the retention time of the flip-flops.

The second method of loading data into the shift register was to use stored data from the FPGA, or to send a sequence of data generated by the FPGA. Both of these methods did not involve a user input. The FPGA could store specific configurations for the CAB that needed to be tested. The sequence data generation was meant to test the functionality of the shift register. Using a data sequence checks the propagation of data through the shift register. By looking at the output of the shift register, the next sequence of data can be predicted from the current

data being outputted. If the data is different, then there is an error in the shift register.

The Basys2 board offers a 4-digit 7-segment display. This display was set up to show the data being transmitted from the FPGA to the shift register in a hexadecimal format. Displaying the data being shifted into the shift register allows the contents of the shift register to be known, and can be compared to the data being shifted out.

All of the timing was done on the rising edge of the clock. The shift register design on chip triggered on the rising edge of the clock; therefore, the FPGA was set to trigger on the rising edge of the clock signal to create consistency between the chip and the FPGA.

While Digilent provided the interface VHDL to the ADC and the DAC, some supporting VHDL needed to be written. The DAC required the generation of test vectors for testing the CAB. The Pmod accessory comes equipped with two DAC chips. Since there are two DAC chips, the FPGA can produce the two test signals independently of each other. The test signal was generated on the FPGA in sequence. The positive data signal cycled up from 0 to 1.2 V, and the negative signal cycled down from 1.2 V to 0. This signal tests the range of values on the inputs of the CAB. The FPGA can also produce other test signals as needed. The

VHDL needs to carefully regulate the output signal as the FPGA runs on a 3 V supply and the chip runs on a 1.2 V supply.

The ADC takes the data from the outputs and then stores them in memory on the FPGA. Like the DAC, the ADC Pmod from Digilent comes with two ADC chips, and can therefore take the two differential outputs from the CAB simultaneously. The provided code from Digilent inputted the data from the ADC, and then further VHDL stored the data in a defined memory space on the FPGA. A defined memory space needed to be implemented on the block random access memories (RAMs) on the FPGA. If the block RAMs are not used, then the VHDL creates a large group of registers using the slices on the FPGA. This quickly overwhelms the FPGA, leaving no more resources for the programming. The VHDL accessed the block RAMs using the code provided by Xilinx, to create a 2k × 8 memory space. The data from the CAB is stored in the memory space until the memory space is filled, where a PC can access the data through the Digilent Adept software. Once the FPGA uploads the data, the memory will refill with data from the CAB.

The uploaded data can be analyzed on the PC. The data can be imported into programs like Matlab or Excel, and then graphed and analyzed to test the functionality of the CAB.

4.6 Printed Circuit Board Interface

The FPGA cannot interact with the chip from the Basys2 board directly. While the Basys2 board provides an excellent framework to work from, there are some problems with connecting it to the chip.

One of the first major problems is that the FPGA runs on a 3 V supply, while the designed chip runs on a 1.2 V supply. If the FPGA was connected directly to the chip, it is likely that the power from the FPGA would overwhelm the chip and burn it out, destroying the transistors inside and making it useless. As a result, the input voltages need to be stepped down. A simple voltage divider can step down the voltages to the appropriate level. The FPGA output connects to a variable resistor before going into the CAB on the chip. The variable resistor and the circuitry on the chip create a voltage divider. Using the variable resistor allows the voltage coming from the FPGA to be fine tuned to 1.2 V, and avoids manufacturing errors that may occur in single value resistors and in the manufacturing of the chip. The outputs from the DAC do not need to be run through a voltage divider as the VHDL can regulate the output voltage previously stated above.

The second problem is that the Basys2 board does not have a socket to connect the 40-pin dual-inline pin (DIP) that the chip was packaged in directly. The Basys2 board requires a connection network to connect to the chip packaging. A PCB is an ideal candidate to connect the two systems together. The PCB provides

a framework for the 40-pin DIP socket with which to mount the chip. The PCB can then provide the needed connections to the DAC, ADC and the programming output on the Basys2 board. The necessary voltage dividers can also easily be mounted on the PCB to step down the voltages from the Basys2 board.

The PCB design began in a program called Eagle. Eagle is a schematic capture program, which allows an engineer to design a schematic of the desired circuit and then convert it into a PCB. A generic 40-pin DIP socket was placed in the schematic to represent the designed chip. However, the chip design contains only 20 pins. Unfortunately no 20-pin DIP packaging was available at the time, and as a result the chip was mounted in a 40-pin package. The pins that were not connected to the chip were connected to ground to help avoid any noise from the power supply and isolate the signal pins from each other. Also a ground plane was used in between the signal lines which helped to isolate the signals from one another.

To connect the chip to the FPGA, three 6-pin headers were included, since the output ports from the FPGA are also 6 pins. The first header provided a connection from the ADC. The documentation of the ADC Pmod gave the details of the order the pins came from the ADC [68]. The pins were appropriately labelled on the schematic, connecting them to the chip. Any unused pins were connected to ground to prevent crosstalk, and to prevent any of the unused pins from becoming floating nodes. The second header connected the DAC to the chip.

Again, the reference manual from Digilent provided the necessary pin details to label the connections on the schematic, and connect it to the chip [67].

The third and final header was used to connect the programming data from the FPGA to the shift register on chip. The pins were described in the VHDL, and they were labelled accordingly on the PCB schematic. In this case, the unused pins connected to a resistor before connecting to ground. Since the pin was connected directly to the FPGA, it would be unwise to connect the pin directly to ground. If the pin was set to '1' by the FPGA, then there would be conflicting driving forces to the pin, which could result in damage to the FPGA. The pull-down resistor prevents this damage. The data pins from the FPGA needed to be connected to the voltage dividers before connecting the data pins to the chip. 2 additional pins were included on the PCB to provide power to the chip and to connect the ground from the power supply to the chip.

Once all of the connections were made on the schematic, Eagle could be used to synthesize the PCB from the schematic. Eagle imports the footprints of the components from the schematic, where they are manually placed on the PCB. The autorouter in Eagle connected the components together once they were placed. The autorouter takes the rules from the PCB manufacturer, in this case Alberta Printed Circuits Ltd. (AP Circuits), and uses those rules to connect the pins appropriately. After double checking all of the connections, the appropriate files could be exported to send to AP Circuits for manufacturing.

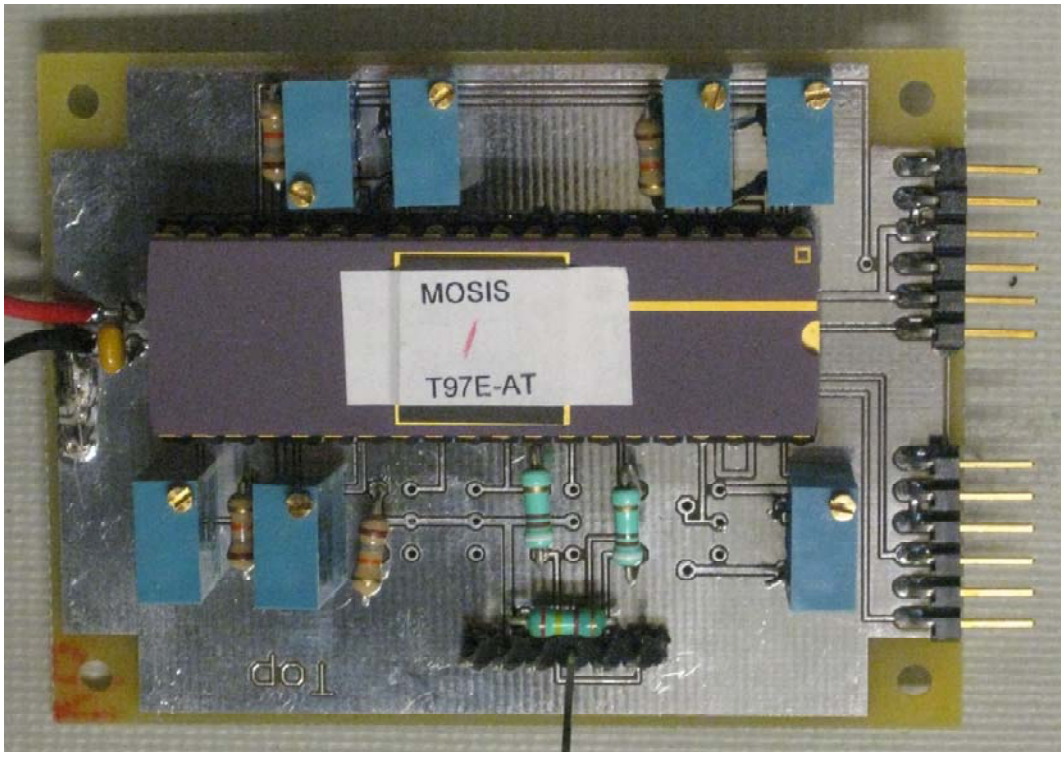

Figure 4-8 - Photo of completed test PCB. The headers on the right and on the bottom are used to connect to the FPGA board, while the blue variable resistors are used to create the necessary bias voltages.

The manufactured PCB does not come with the components attached. As a result, the components were soldered into place by hand. Figure 4-8 shows the manufactured PCB.

4.7 Results From Testing

The PCB was able to directly plug into the FPGA's DAC and ADC ports using 6-pin connectors, while the connection to the programming port was accomplished with the use of a 6-pin cable. The power could be connected through the use of 2 pins on the PCB connected to a bench top variable power supply and alligator clips. The voltage of the 1.2 V supply and the biasing voltages for the analog

components on chip was verified using a multi-meter to measure the DC voltages. The DC voltages could be adjusted appropriately using the variable resistors on the PCB. Also, a multi-meter was used to verify the proper voltage step-down of the voltage dividers on the output ports from the FPGA to program the shift register.

The first step in testing the CAB design was to ensure the proper functioning of the shift register. The shift register controls the circuit configuration of the CAB, and without proper functioning of the shift register, the CAB would be unable to function. The shift register was tested by sending a data signal from the FPGA to the shift register and then looking at the output from the shift register. In proper operation, the shift register should output the previously stored data when new data is shifted in. An oscilloscope allowed us to observe the output signal and the input signal. Figure 4-9 displays the results from the oscilloscope.

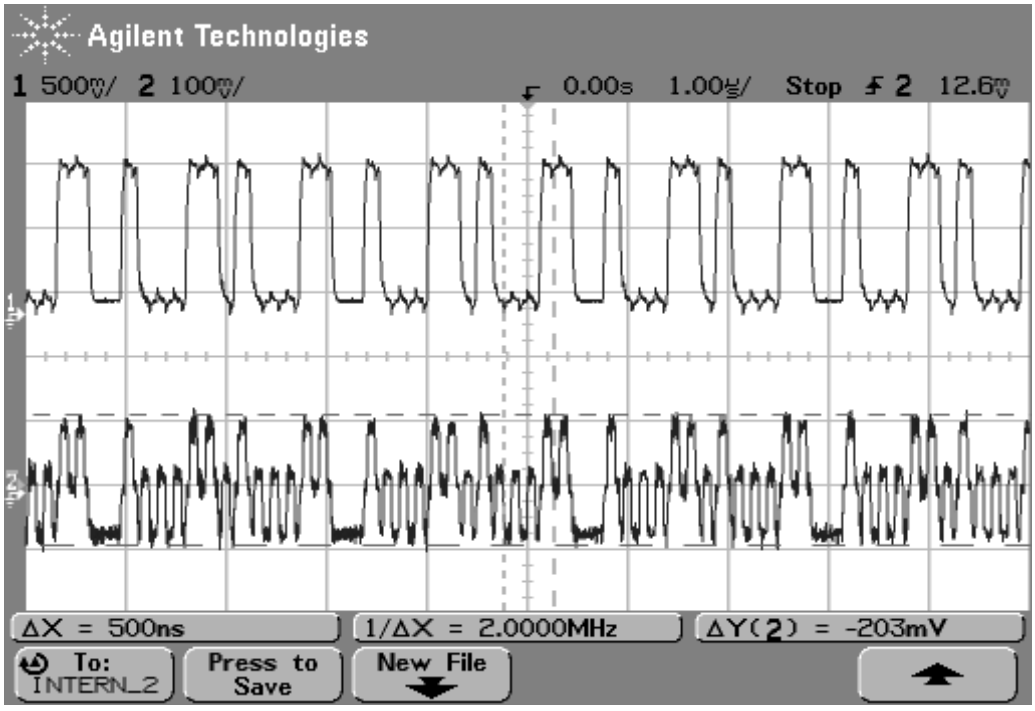

Figure 4-9 - Results from oscilloscope testing. The input, signal 1, into the shift register should be carried through to the output, signal 2. However, in this instance the amplitude of the output signal is very weak, only 200 mV, and there is a large amount of clock feed through in relation to the signal.

Figure 4-9 shows the input signal into the shift register, signal 1, as well as the output signal from the shift register, signal 2. In this test, the FPGA sent the input signal repeatedly into the shift register so that the output should be the same as the input. However, in the case shown above, the output signal was at a much lower level than it should have been; 200 mV peak-to-peak rather than 1.2 V peak-to-peak. Also, a large amount of clock feed through can be observed in the output signal. Figure 4-10 shows the results obtained from a logic analyzer, which better illustrates the clock feed through from the shift register. In this case, the threshold voltage for the input signal was set to 90 mV. The results from the logic analyzer show that the output from the shift register follows the clock signal.

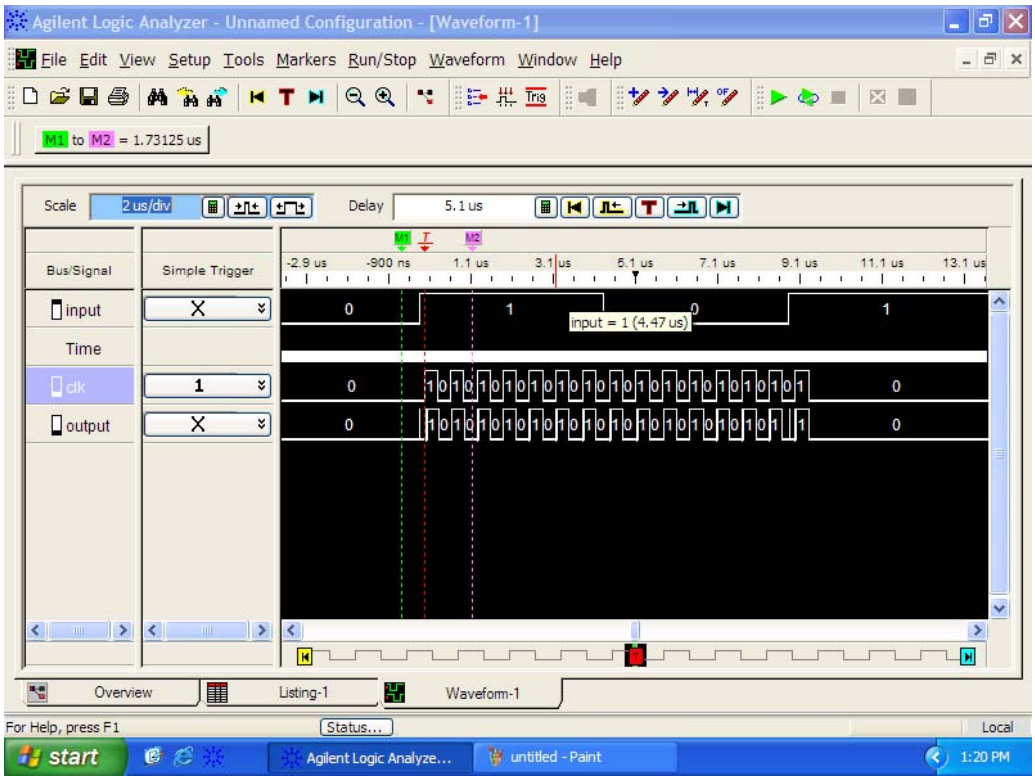

Figure 4-10 - Logic analyzer results showing clock feed through. The logic analyzer shows a cleaner view of the clock feed through.

Based on these results, there is an error either in the chip or the testing equipment. Simulations in Cadence show that there is likely a break in the power supply to the shift register. The simulations in Cadence when the power supply is disconnected from the shift register show similar results to those from the oscilloscope.

Upon examination of the PCB and testing equipment, no errors in the testing equipment could be detected. A multi-meter measured the connectivity of the pins by testing the resistance between two points. In each instance, the pins were connected to the appropriate wires and other pins. Since the testing equipment checked out, it is likely that there is an error on the layout of the chip.

4.8 Summary

This chapter presents a layout, fabrication, and testing of a CAB. A gain-boosted OTA design was designed for fabrication in a 0.13 μm process. A TSPC D flip-flop was used to create a shift register to control the CAB design. Unfortunately, the dynamic nature of the flip-flop was not suited to long term storage of configuration bits on an FPAA device.

An FPGA on a Digilent Basys2 board was programmed in VHDL to provide testing for the fabricated design. The FPGA was able to provide programming for the CAB through the shift register, as well as provide test vectors for the CAB. The results from the CAB could then be stored on the FPAA and transferred to a PC for analysis.

A PCB was fabricated to provide the bias circuitry as well as an interface between the CAB and the FPGA. A set of voltage dividers using variable resistors provided the appropriate bias voltages for the CAB, and 3 six-pin headers were used to interface with the FPGA. A ground plane was also implemented to help isolate signals from each other.

The fabricated CAB was then tested using the FPGA, an oscilloscope, and a logic analyzer. Based on the outputs of the shift register, the chip was found to be non-functioning.

Chapter 5

Conclusions and Future Work

This thesis presents a design for a CAB to be used in an FPAA, specifically for use in signal processing applications. The CAB design provides a fully differential OTA combined with an array of capacitors, which can fine tune the frequency response of the OTA. A gain-boosting technique increased the gain-bandwidth product of the fully differential OTA. The increase in the gain-bandwidth product allowed the OTA to function at a higher frequency than was otherwise attainable. While this design performed short of the desired target, other FPAA designs that have been published have not functioned at as high a frequency.

The fully differential design provides more flexibility than its single-ended counterpart. This increases the applications that the FPAA can implement. Also, the use of a standard CMOS process rather than a more specialized process helps to keep the FPAA design more available and flexible so it can interact with more systems. The differential design of the OTA also helps to reduce the environmental noise compared to single ended OTAs.

One of the other advantages of this design over static analog circuits is its digital programmability. Since a shift register controls the transmission gates, the FPAA could be integrated into digital designs. The transmission gates and shift register

of the CAB allows software in a digital processor to control the programming of the FPAA, allowing for updates of hardware designs to easily be implemented.

5.1 Meaning of Results

The results from testing the implemented design proved that there is an error in the OTA proposed in this thesis. While there was clock feed through on the shift register, no signal propagated through the shift register. When the output from the testing is compared to the simulation results, it is likely that there is an improperly connected voltage source somewhere on the chip or that the output from the shift register is not driven properly at the pin.

However, the initial simulation results from the design do show promise. The bandwidth of the OTA approached the desired bandwidth of operating in the 402 - 405 MHz ISM band. The final redesign of the OTA shows a DC gain of 50 dB with a -3 dB frequency of 1.217 MHz, a GBW of 384.8 MHz, and a power consumption of 156.2 μW. While this simulation does not meet the desired -3dB bandwidth, the GBW is close to 405 MHz. The operation of the band-pass filter shows a useful circuit operating up to 200 MHz, a higher frequency than other designs have shown and which approaches the target ISM band. The simulations of the shift register controlling the transmission gates also shows promise. The transmission gates allow the signal to pass with very little degradation. The small amount of signal degradation shows that there is promise for an array of the CAB design, which can be used to implement a full FPAA design.

5.2 Uses of Proposed Design

The most notable projected use of the proposed design is an SDR. The digital programmability and the flexibility of the OTA design make the future FPAA ideal for use in an SDR. The current trend in SDRs is to move as much of the signal processing to the digital side of the circuit. However, with the use of a programmable analog circuit like an FPAA, not all of the signal processing needs to be done digitally. Since the analog circuit is digitally programmable, the flexibility of a digital circuit is maintained, and the benefits of some analog front-end processing become available.

Generic signal processing chips would also benefit from including the proposed FPAA. Many of the DSP chips do not have access to supporting analog components on chip. Including an FPAA on the DSP chip would help keep the generic architecture, but increase the functionality of the chip. Many of the RF functions could be performed without the need for external circuitry. This also has the benefit of likely reducing the power consumption in an SDR compared to an all digital system. Analog components often function using less power than their digital counterparts, and in a world where mobile devices are becoming more common place, the low power systems are in greater demand. However, an FPAA can consume power in the switches and routing required for greater flexibility meriting further study.

An FPAA design would also help to get signal processing products to the market quicker. The design of analog circuits is currently a very arduous process. Many of the automated systems that make designing digital systems relatively easy are not available for analog circuits, due to their dependence on a large variety of parameters. With the development of an FPAA, much of the design challenges are removed. This means that products are very quick to market, similar to the way FPGAs revolutionised the design of digital circuits.

5.3 Future Research and Implementation of Design

The first step would be to produce a functioning implementation of the CAB proposed here. Also, the design of the CAB may also be improved by the testing of other amplifier designs. Other amplifier designs may perform at higher bandwidths, or use less power than the design proposed in this thesis. By producing a functioning CAB, there will be much stronger evidence that the development of FPAAs would help to produce better SDRs in the future. The functioning design can also connect with other CABs to test the functionality of an array of the CABs.

In designing a new CAB different memory should be used from the design presented in this thesis. A shift register using static flip-flops rather than the dynamic flip-flops would not require the data to be refreshed. Also using SRAM would provide a more stable design, use fewer transistors, and have a lower static and dynamic power consumption than using a shift register. Using a larger

capacitor array at the output of the OTA in the CAB would also allow for a larger range of frequencies to be accessed.

Once the demonstration of a functioning CAB is successful, the next logical step is to create a small array of the CABs to test the interconnections between the blocks. The implementation of a small array helps to eliminate the possibility that an error has occurred somewhere in the interconnection network. Proving the array functions properly, a full array should be implemented to demonstrate the full functionality of an FPAA. Other discrete components could be included to work in conjunction with the CABs, including a PLL, larger capacitor arrays, inductors, and resistors.

Then an SDR design can include the full array. This SDR design would highlight the benefits of using reconfigurable analog architecture. The analog front-end would be digitally programmable, retaining the programmability of digital circuits. In addition, the FPAA may prove to consume less power than an all digital circuit, making the design more portable for inclusion in mobile devices.

The feature size of the technology used to design the FPAA can be smaller. The 130 nm process used in this thesis is one of the larger processes available today. There are digital processes available that include feature sizes as low as 32 nm and possibly even smaller. Incorporating the design of an FPAA into smaller

technologies would allow it to interface more easily with the newer digital technologies, as well as reducing the area consumed by the FPAA design.

In the end, the design of an FPAA provides a promising view of the future. Reconfigurable analog architecture allows for quick development of analog circuits, which can perform at faster speeds and use less power than similar digital circuits. Consequently, the FPAA could revolutionize not only the design of analog circuits specifically, but also the communication industry in general.

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Appendix A

Layouts

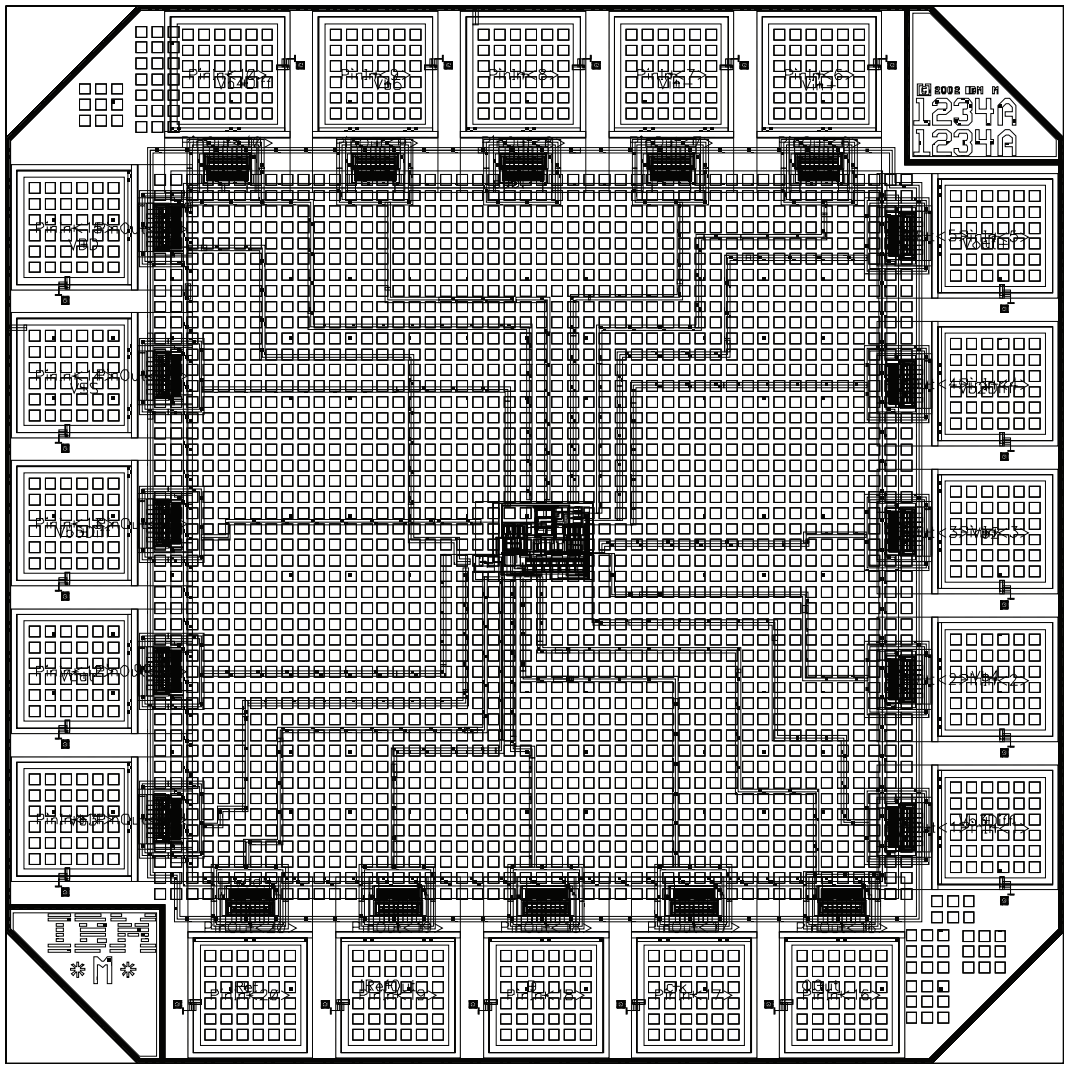

Figure A-1 - Layout of final chip design

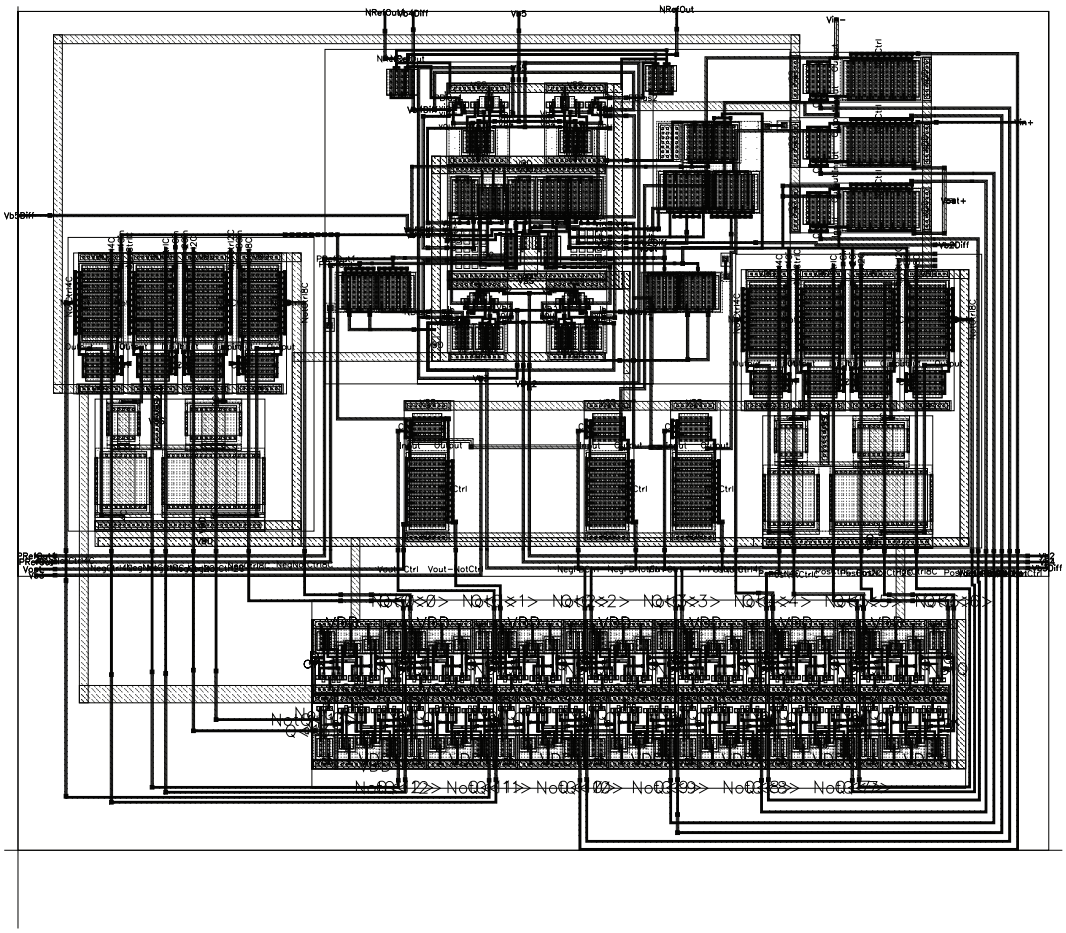

Figure A-2 - CAB Layout including memory

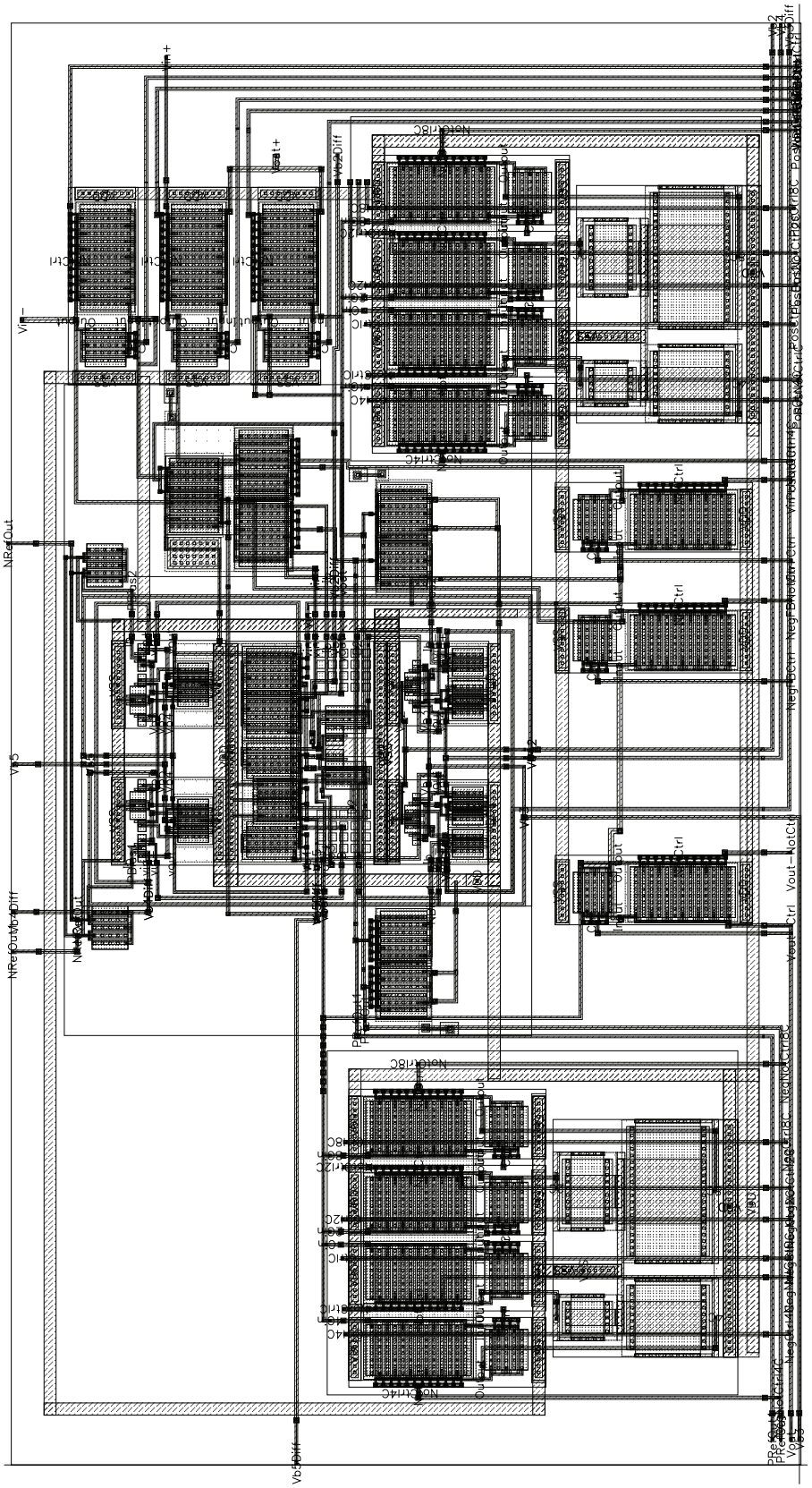

Figure A-3 - CAB Layout

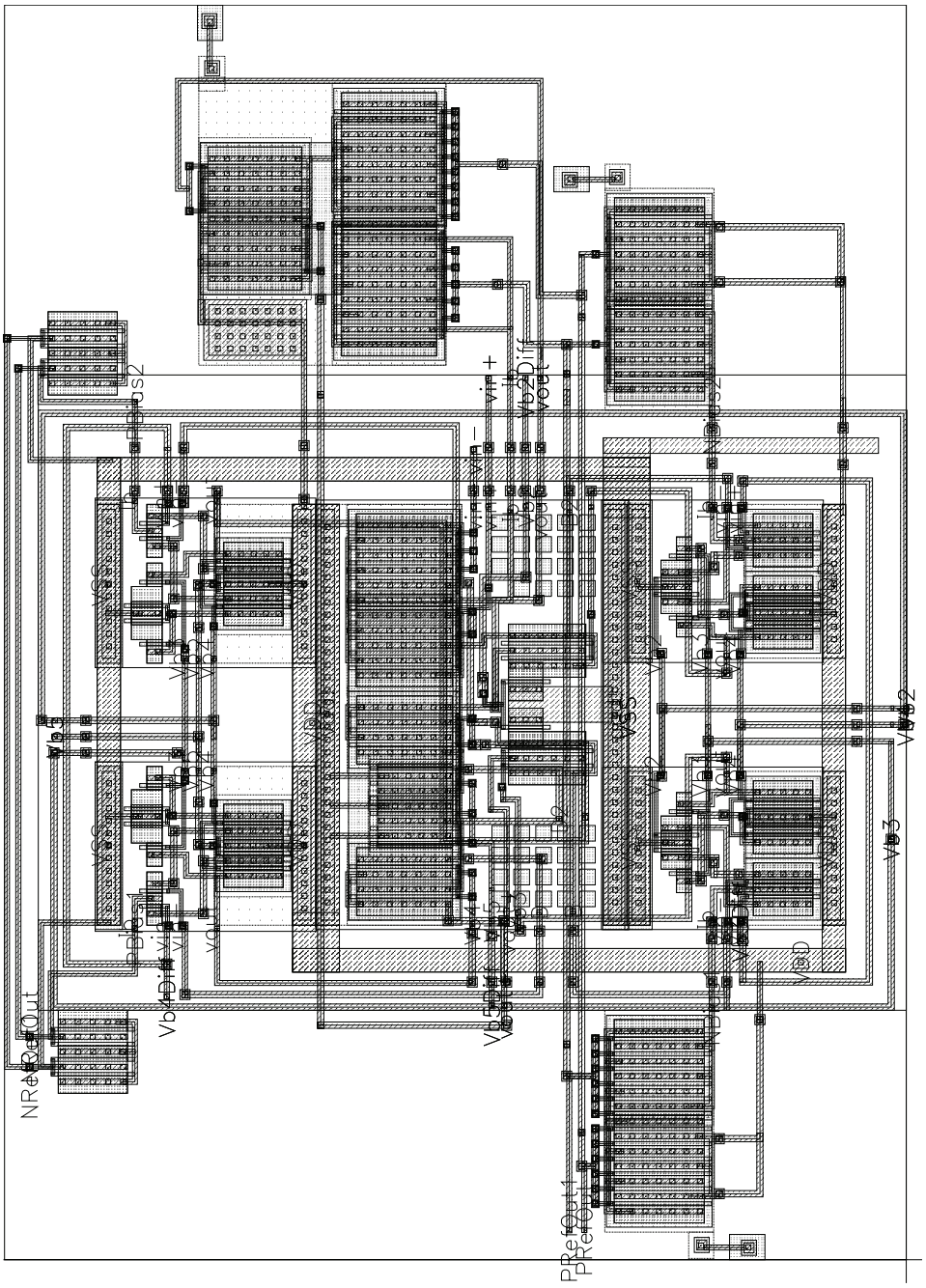

Figure A-4 - OTA with gain-boosting layout

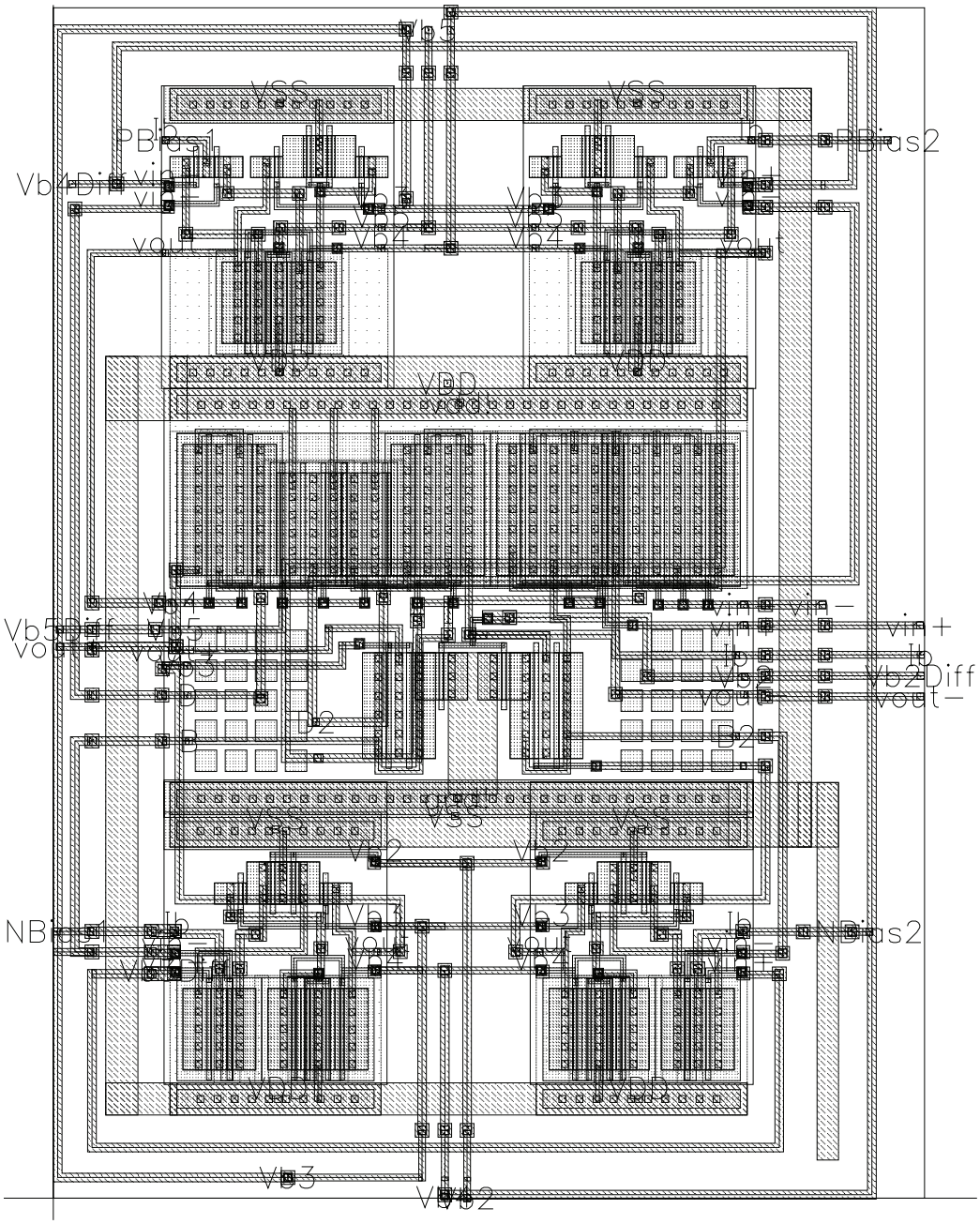

Figure A-5 - Differential OTA Layout

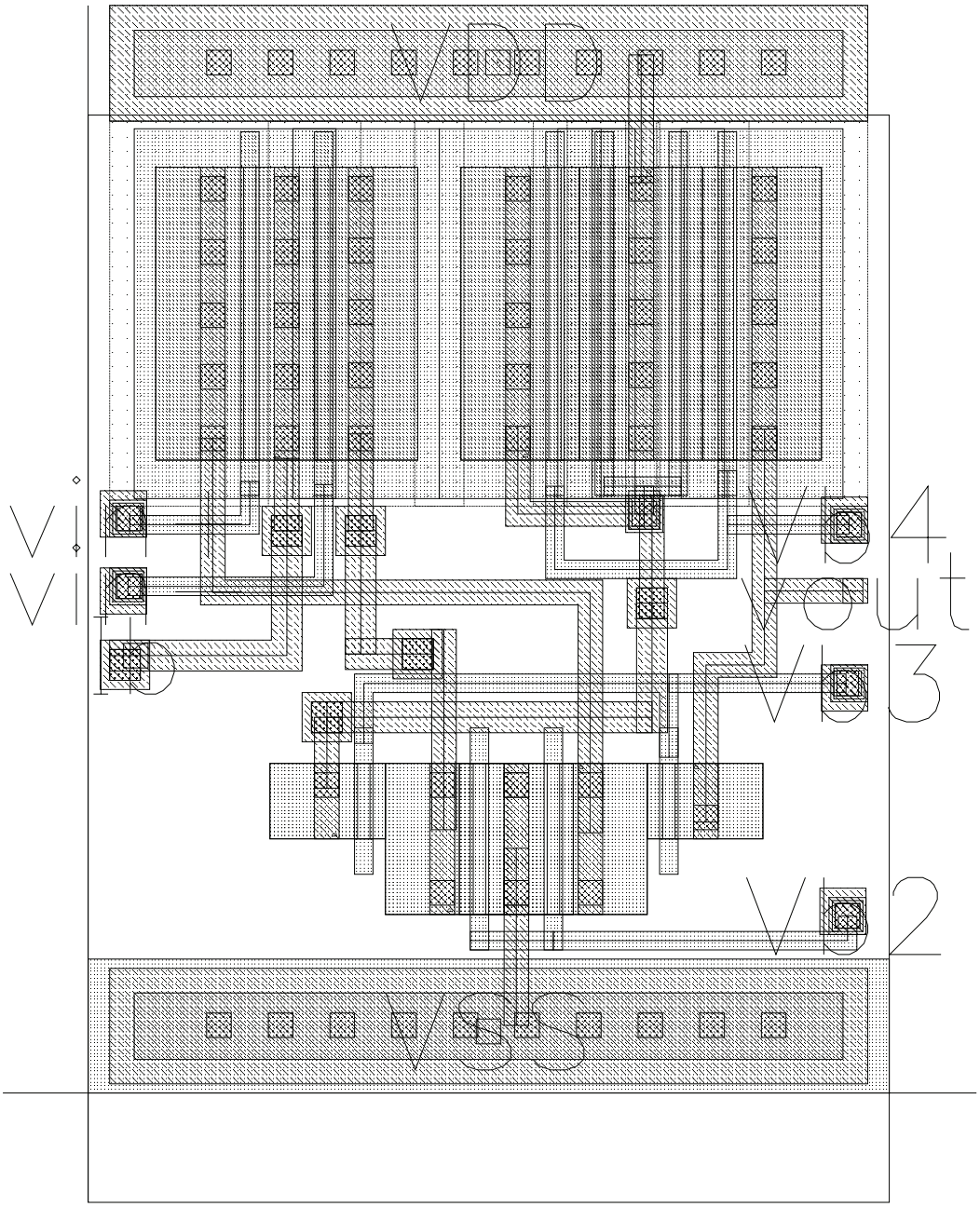

Figure A-6 - Bias OTA for NMOS transistors

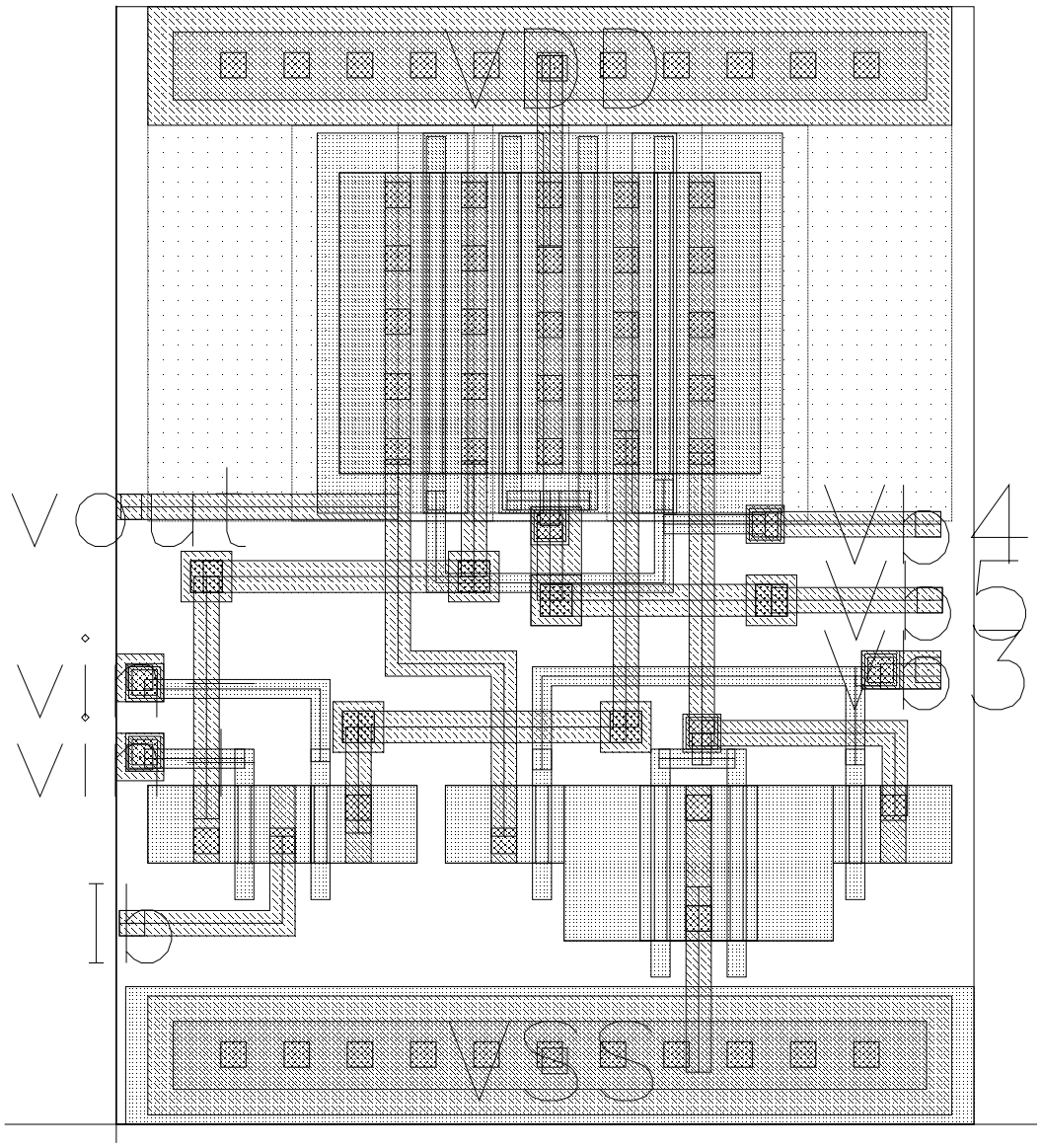

Figure A-7 - Bias OTA for PMOS transistors

Appendix B

Schematics

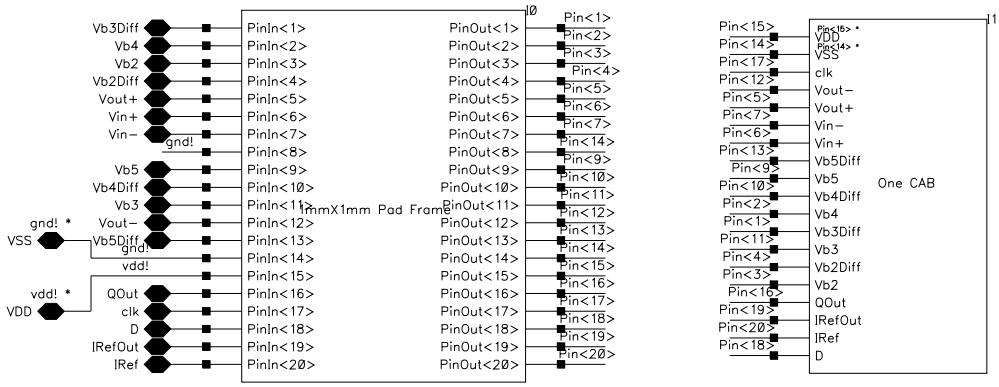

Figure B-1 - Schematic of final chip

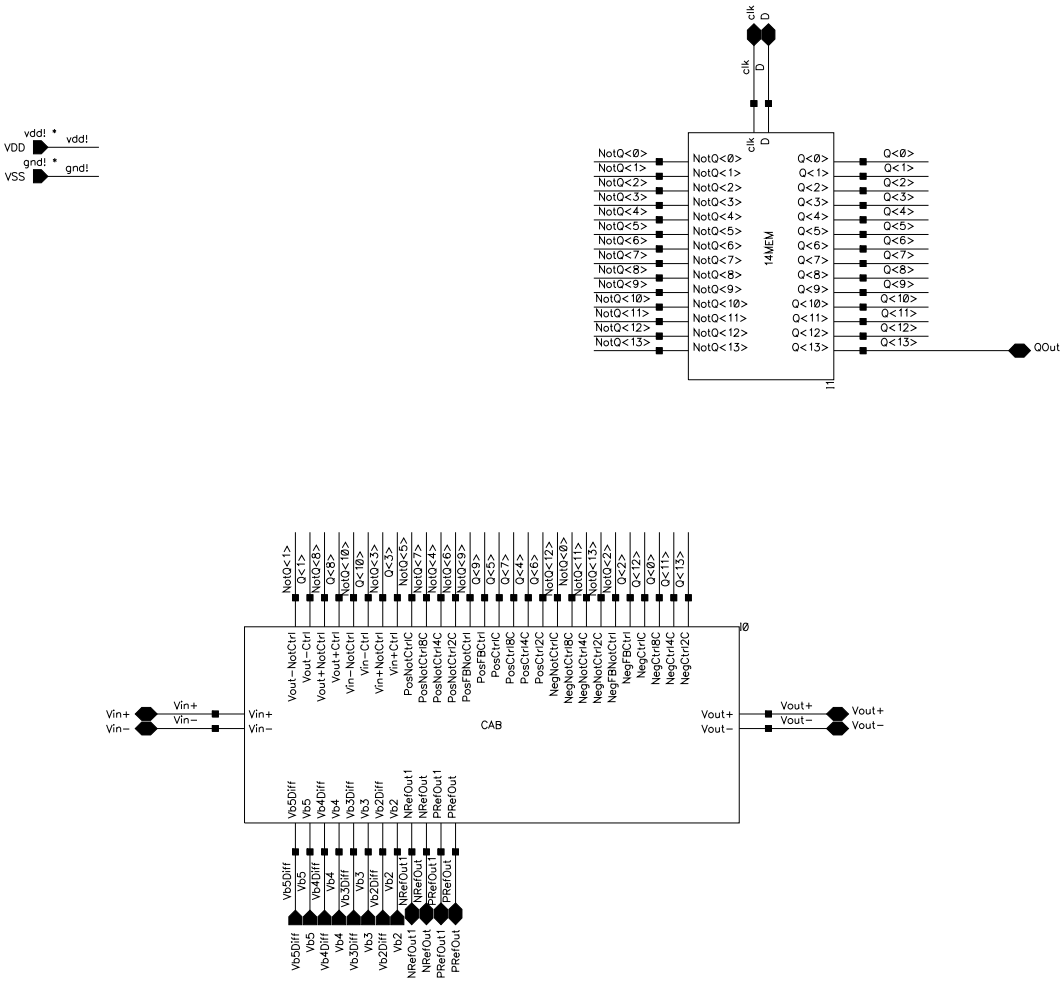

Figure B-2 - Schematic of CAB with memory.

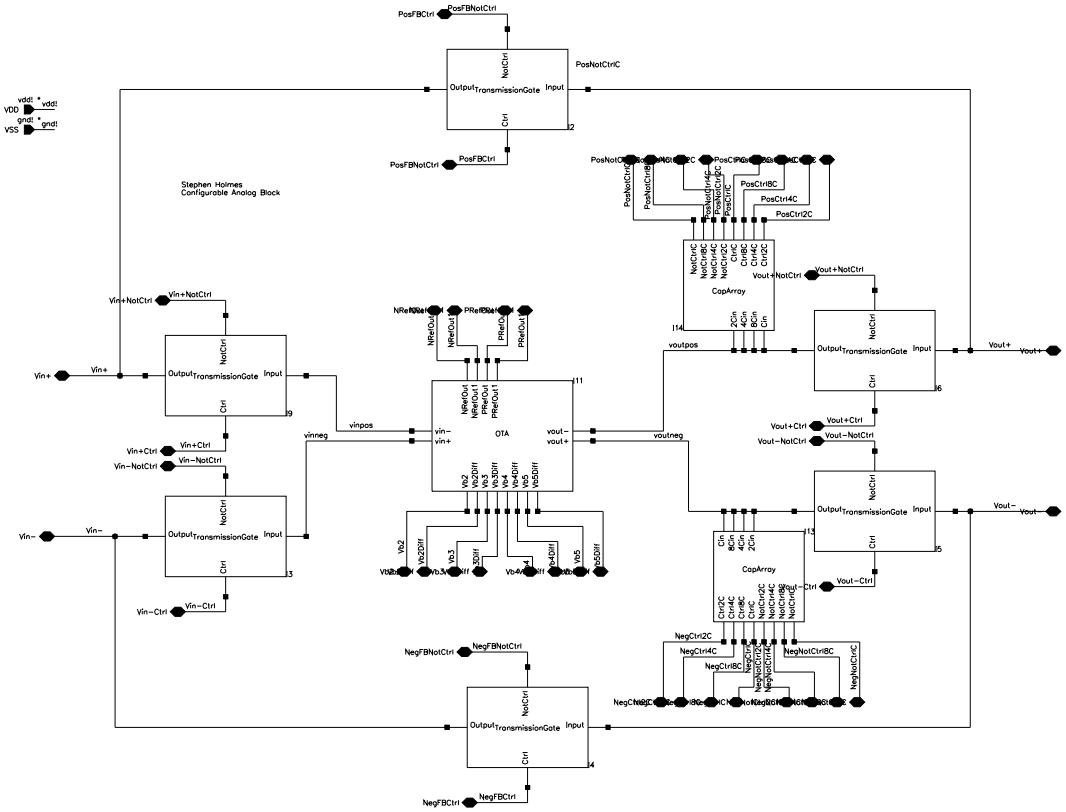

Figure B-3 - Schematic of CAB

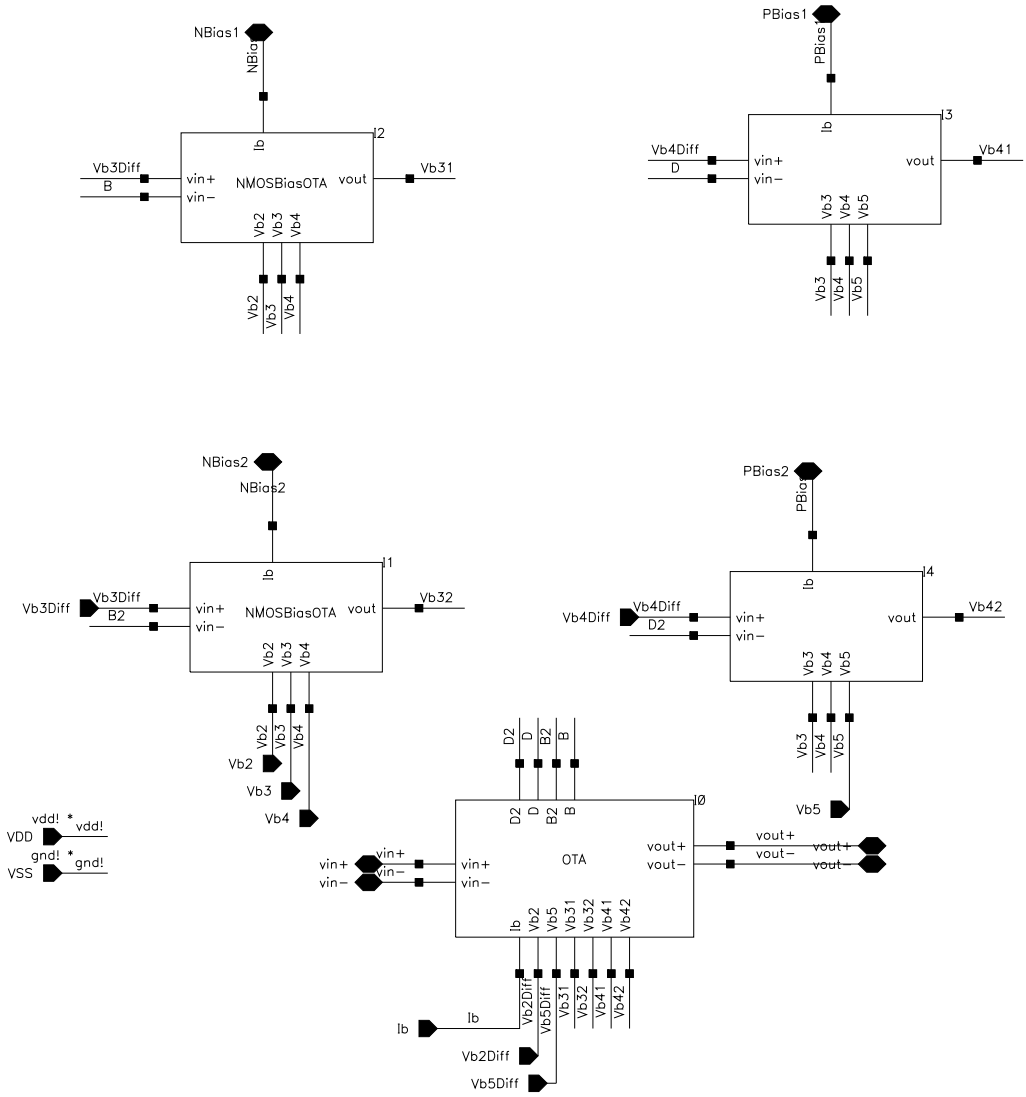

Figure B-4 - Schematic of gain boosted OTA

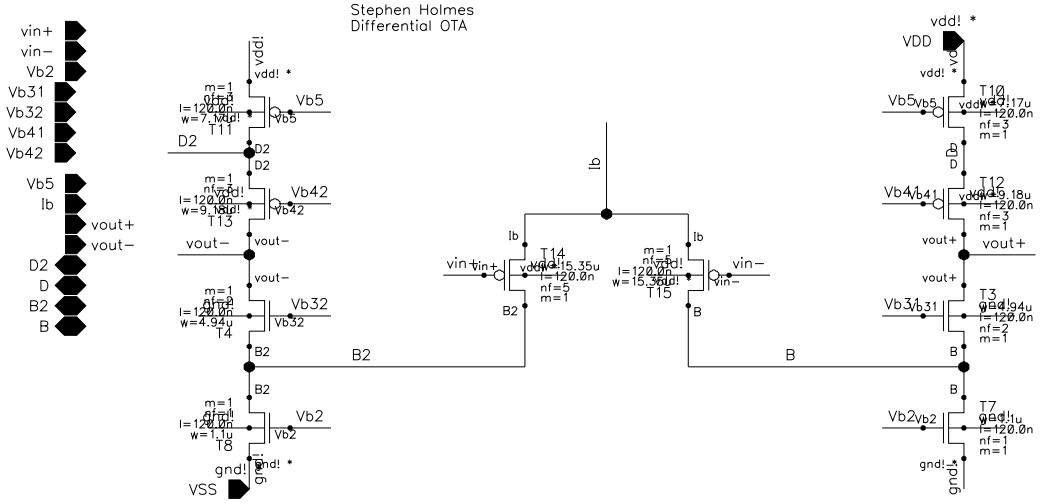

Figure B-5 - Differential OTA schematic

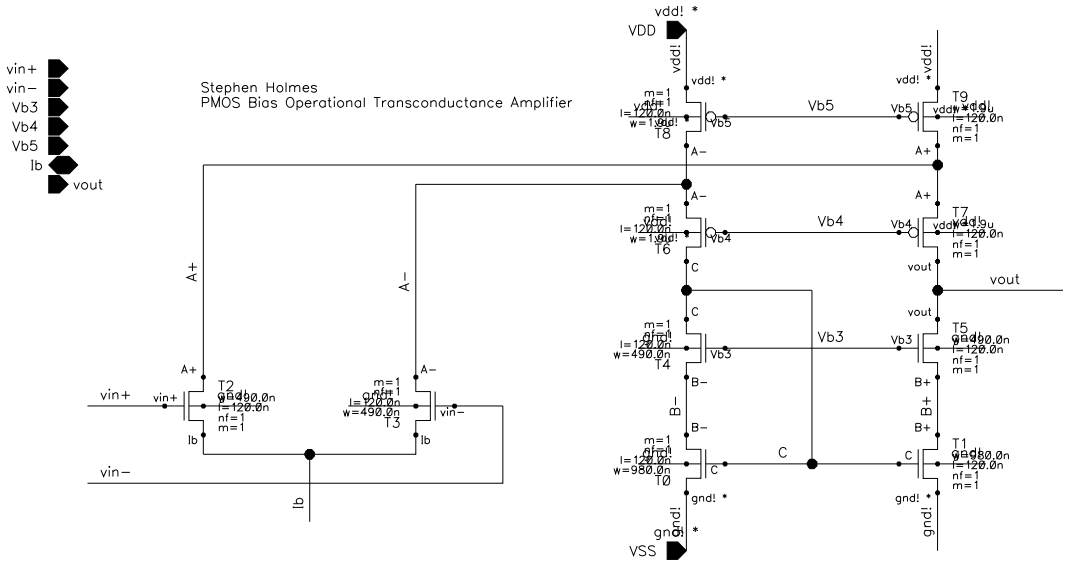

Figure B-6 - PMOS input pair bias OTA

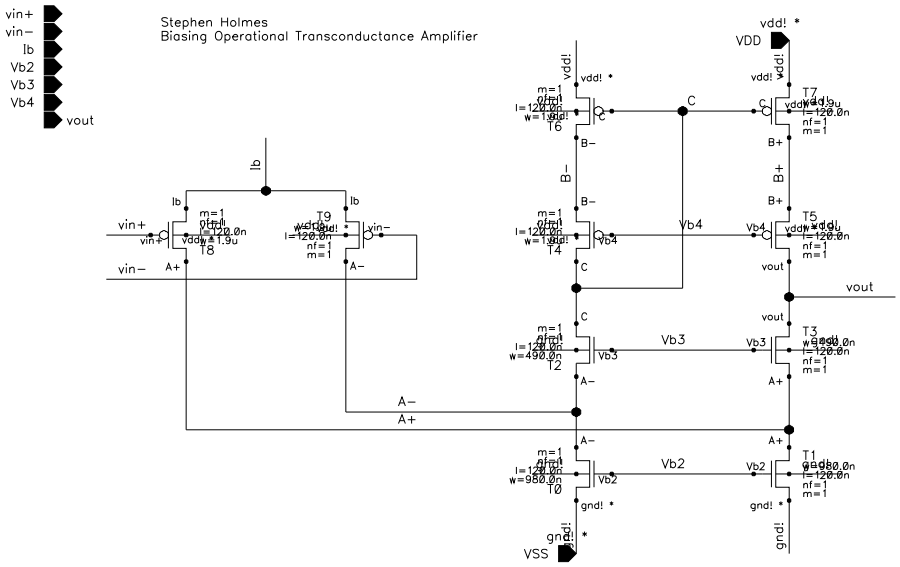

Figure B-7 - NMOS input pair bias OTA

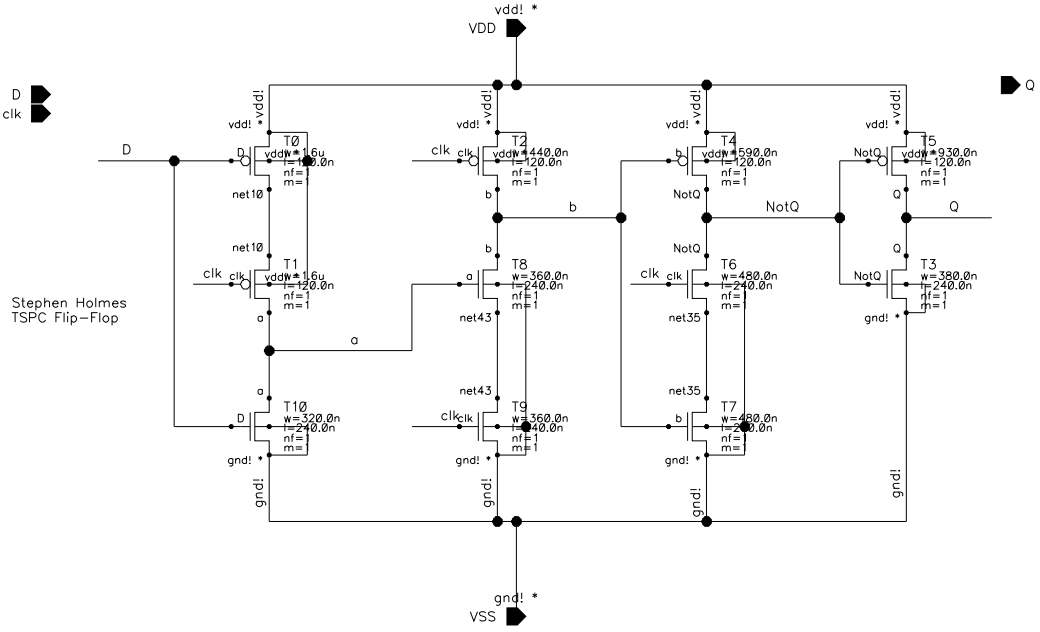

Figure B-8 - Schematic of D flip-flop