Design, Analysis, and Control of the Modular Multilevel DC/DC Converter for Medium- and High-Voltage DC Grids

By

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Abstract

Nowadays, renewable energy sources have gained escalating importance due to environmental and economic reasons. However, these energy sources are primarily located in remote areas and distant from load centers. High-voltage dc (HVDC) and medium-voltage dc (MVDC) systems have been proposed in the last decades for efficient and reliable integration of renewable energy resources. To date, a noticeable number of these dc systems are established around the world. Recently, researchers have proposed the concept of "DC grids," which can be realized by connecting the existing point-to-point dc systems. This structure can improve the efficiency and stability of the power system. However, one of the most concerning challenges related to this concept is the interconnection of already built dc systems. Because existing dc systems are built through time, they possibly have different voltage levels and grounding systems. To address this challenge, the dc/dc modular multilevel converter (MMC) is proposed in the literature as one of the most promising solutions. This converter offers the advantages of modularity, scalability, and high efficiency.

Few studies have been conducted on the modeling and control of the dc/dc MMC. The literature falls short in several aspects, such as improved design, analysis of operation limits, fault-tolerant operation, converter analysis under uncertainty, and development of advanced controllers and efficient fault-blocking capability. This research aims to 1) develop an augmented design approach that considers both control and hardware aspects of the converter, 2) investigate the operation limit of the hybrid dc/dc MMC caused by the capacitors voltages unbalance, 3) develop a tailored fault-tolerant operation strategy without additional submodules (SMs), 4) analyze the unsymmetrical operation of the dc/dc MMC caused by

parametric uncertainty, 5) develop an advanced controller based on the model predictive control for the dc/dc MMC, and 6) realize an efficient fault-blocking capability by proper selection of SMs.

The first study in this thesis facilitates the dc/dc MMC design with a smaller number of SMs and higher efficiency. Unlike the previous literature, the analytical results of the second study show that the capacitors voltages balance in the hybrid dc/dc MMC limits the operation range of the converter. In the third study, first, the unique features of the dc/dc MMC are investigated. These features make the fault-tolerant operation possible without the need for additional SMs. Then, utilizing these features, a tailored fault-tolerant operation strategy is developed to cope with several SMs failures. When the parametric uncertainty comes into action, it can force the converter to work in unsymmetrical conditions. The fourth study develops steady-state models representing the behavior of the converter in unsymmetrical conditions, and then the maximum tolerable variation of parameters is found in different practical cases. An advanced controller based on the model predictive control is developed in the fifth study to improve the steady-state and transient performances of the dc/dc MMC. Finally, an efficient fault-blocking capability is realized by adequately selecting the number and type of SMs. Detailed time-domain simulations under the MATLAB/Simulink environment validate the analytical results. This research contributed to the fundamental understanding of the dc/dc MMC operation and significantly improved the converter efficiency, reliability, and steady-state and dynamic performances.

Preface

This thesis is an original work by Ramin Razani. As detailed in the following, some chapters of this thesis have been published or submitted for publication as scholarly articles in which Professor Yasser Abdel-Rady I. Mohamed was the supervisory author and has contributed to concepts formation and the manuscript composition.

Chapter 3 has been published as R. Razani and Y. A-R. I. Mohamed, "Augmented Design of DC/DC Modular Multilevel Converter Improving Efficiency and Reducing Number of SMs," in *IEEE Transactions on Power Delivery*, vol. 35, no. 6, pp. 2905-2915, Dec. 2020.

Chapter 4 has been published as R. Razani and Y. A-R. I. Mohamed, "Operation Limits of the Hybrid DC/DC Modular Multilevel Converter for HVdc Grids Connections," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4459-4469, Aug. 2021.

Chapter 5 has been published as R. Razani and Y. A-R. I. Mohamed, "Fault-Tolerant Operation of the DC/DC Modular Multilevel Converter Under Submodule Failure," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 6139-6151, Oct. 2021.

Chapter 6 has been published as R. Razani and Y. A-R. I. Mohamed, "Analysis of the Unsymmetrical Operation of the DC/DC MMC Considering the DC-Link Impedance," in *IEEE Transactions on Power Delivery*, vol. 37, no. 3, pp. 1723-1733, June 2022.

Chapter 7 has been published as R. Razani and Y. A-R. I. Mohamed, "Model Predictive Control of Non-Isolated DC/DC Modular Multilevel Converter Improving the Dynamic Response," in *IEEE Open Journal of Power Electronics*, vol. 3, pp. 303-316, 2022.

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Chapter 1 Introduction

New clean and renewable energy resources, such as wind, photovoltaic, and energy storage systems will be significant parts of close-future grids. For example, in Alberta, more than 5000 MW of new wind power generation is already contracted or under development, whereas wind-based generation is going to be 20% of the total power generation capacity in Canada by 2025 [1], [2]. The renewable energy resources are mostly far located from load centers, and, therefore, the generated power must travel long distances to reach consumers. In this regard, high-voltage dc (HVDC) and medium voltage dc (MVDC) systems are introduced to transmit harvested power from renewable resources with better stability and reliability as compared to the conventional high-voltage ac (HVAC) transmission systems. To date, a considerable number of point-to-point dc systems have been installed around the world, which has inspired researchers to introduce a new concept of "DC grids" [3]. One of the main challenges of the dc grid is to interconnect two already installed point-to-point dc systems, which might have different voltage levels and grounding systems. To address this problem, different types of high voltage/power dc/dc converters were proposed in the literature [4]. These converters will play a significant role in interfacing and integrating renewable resources into power grids [4]. One of the most promising topologies, which is inspired by the renowned dc/ac modular multilevel converter (MMC) [5], [6] is the dc/dc MMC [7]. This newly emerged dc/dc converter inherited the prominent advantages of the well-known dc/ac MMC, such as high reliability, high efficiency, and scalability [8]. However, several challenges related to this converter still need to be addressed.

1.1 Research Motivations

The available literature on the dc/dc MMC falls short in the following aspects:

- The dc/dc MMC can work in different operating points while transmitting a fixed amount of power. However, the operation at each operating point requires a different

number of submodules (SMs) in each arm. Moreover, the ac circulating current is different at each operating point. This will affect the initial cost and efficiency of the converter. As a result, it is crucial to find the proper operating point.

- The operation and control of the hybrid dc/dc MMC are investigated in the literature. Previous results showed that the hybrid dc/dc MMC could limitlessly extend the power transfer capability. However, analytical and simulation results show that the operation of this converter is limited by the capacitors voltages unbalance. Therefore, this phenomenon needs to be studied thoroughly.

- In general, MMCs are susceptible to SM failures. As a result, it is critical to develop a fault-tolerant operation strategy for the dc/dc MMC. To date, the fault-tolerant operation of the dc/dc MMC under SM failure is not investigated in the literature.

- The dc/dc MMC operation is not studied in the unsymmetrical condition. The unsymmetrical condition is referred to the situation in which the phase-legs operate at different operating points because of varying system parameters.

- The development of an advanced controller based on the model predictive control (MPC) for the dc/dc MMC is still lacking in the literature. Several studies showed that this control method improved the steady-state and transient operation of power electronic converters.

- To date, only the hybrid dc/dc MMC with full-bridge-based SMs in the upper arm is introduced for fault-blocking. However, this topology has very high semiconductor losses due to the large number of switches in the upper arm. A topology that offers the fault-blocking capability and high-efficiency operation is still missing.

1.2 Research Objectives

The following objectives are identified for this research work to address the difficulties mentioned above:

- Develop an augmented design approach considering the control aspects (different operating points) and the hardware aspects (number of SMs) of the dc/dc MMC. This approach results in a more efficient and cheaper converter compared to the conventional topology.
- Study the effect of capacitors voltages unbalance on the hybrid dc/dc MMC operation limit, and develop a systematic approach to determine the maximum power that the hybrid dc/dc MMC can transfer.
- Develop a tailored fault-tolerant operation strategy that does not require any redundant SMs and only utilizes the unique characteristics of the dc/dc MMC.
- Study the unsymmetrical operation of the dc/dc MMC to facilitate converter analysis and modeling in the presence of parametric uncertainty.
- Develop a decoupled discrete-time dynamic model of the dc/dc MMC, and design an advanced controller based on the MPC method.
- Find a straightforward process to determine the number and type of SMs in the dc/dc MMC to yield the bidirectional fault-blocking capability and high-efficiency operation.

1.3 Research Methodology

First, using the available phasor-domain model of the dc/dc MMC, the number of needed SMs and conduction and switching losses are found at different operating points. The results are used to build a new design approach that yields a more efficient converter. Second, by conducting analytical studies, the capacitors voltages of the hybrid dc/dc MMC in the steady-state are investigated, and the maximum transmitted power for which the capacitors voltages can be balanced is found. Third, by conducting analytical studies, it is shown that the fault-

tolerant operation with the same transmitted power is possible without the need for additional SMs. Furthermore, the required arms voltages are calculated based on the transmitted power to prove that, in severe SMs faults conditions, the converter can continue its operation with reduced power transmission. Fourth, by considering dc-links impedance, new detailed and simplified models are developed to study the behavior of the dc/dc MMC in the presence of parametric uncertainty. The maximum tolerable variation of the parameters is found using the developed models. Fifth, by decoupling and discretizing the dynamic model of the dc/dc MMC using the forward Euler method, the first controller based on the MPC method is proposed to control the dc/dc MMC. Finally, the appropriate number and type of SMs are selected by analytical studies to satisfy the fault-blocking requirements and high-efficiency operation.

1.4 Research Contributions

The main contributions of this research work are the development of

1) A new design approach that reduces the number of active components and power losses and extends the operating range of the dc/dc MMC [9],
2) An analytical method to determine the operation limit of the hybrid dc/dc MMC caused by the capacitors voltages unbalance [10],
3) A fault-tolerant approach that uses the dc/dc MMC's unique characteristics without the need for redundant SMs [11],
4) Detailed and simplified models that can express the behavior of the dc/dc MMC in the presence of parametric uncertainty [12], and
5) A model predictive control of the dc/dc MMC that improves both the steady-state operation and dynamic response of the converter.
6) An efficient hybrid dc/dc MMC topology with bidirectional fault-blocking capability.

1.5 Thesis Organization

This thesis focuses on the design, analysis, and control of the dc/dc MMC. It is organized as shown in Figure 1.1. In Chapter 2, different topologies of the dc/dc converters and a literature

survey on the dc/dc MMC are presented. In Chapter 3, the proposed augmented design of the dc/dc MMC is presented. The operation limit of the hybrid dc/dc MMC is investigated in Chapter 4. The proposed SM fault-tolerant operation is elaborated in Chapter 5. Chapter 6 studies the dc/dc MMC operation in the unsymmetrical condition. The developed MPC controller for the dc/dc MMC is presented in Chapter 7. The proposed efficient topology with fault current blocking capability is introduced in Chapter 8. Finally, Chapter 9 concludes the thesis and provides directions for future works.

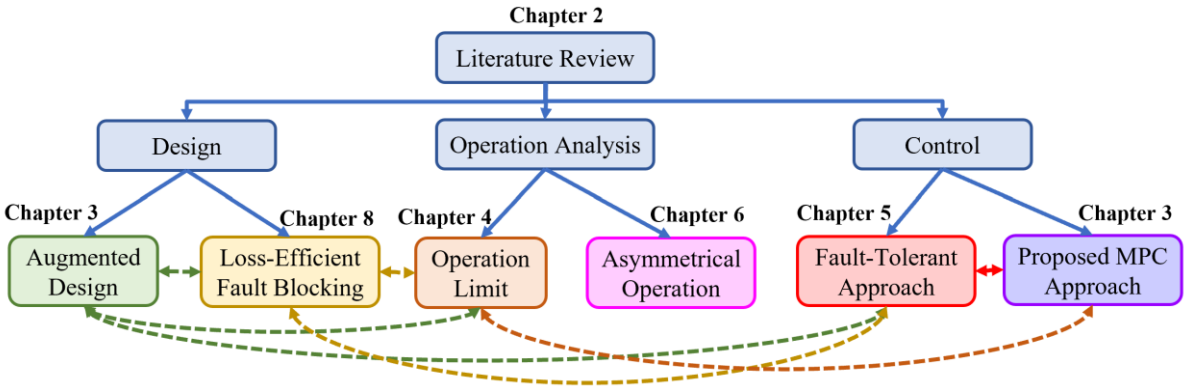


Figure 1-1 Organization of the thesis.

Chapter 2 Literature Survey

This chapter presents an overview of different topologies of the dc/dc converters for medium- and high-voltage applications and a detailed literature survey on the dc/dc MMC.

2.1 Isolated Topologies

The isolated topologies are based on two stages of the ac-dc conversion. The galvanic isolation is achieved by the ac transformer or coupled inductors. Safety and grounding are the main reasons for the isolation. These topologies make it possible to have different grounding systems on both sides of the converter. Furthermore, a high conversion ratio can be easily achieved by proper design of the ac transformer, and it provides inherent dc-fault block capability. The isolated topologies can be categorized as the different variations of the dual active bridge (DAB) and those operating based on flyback/forward converter principles.

2.1.1 Dual Active Bridge (DAB) Topologies

Two-level high-voltage DAB and modular multilevel DAB are the most common types of DAB topologies. In the following, the advantages and disadvantages of these topologies are explained.

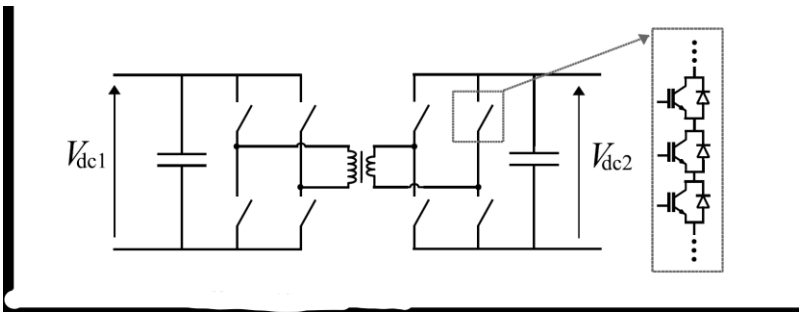


Figure 2-1 Two-level high-voltage DAB [3].

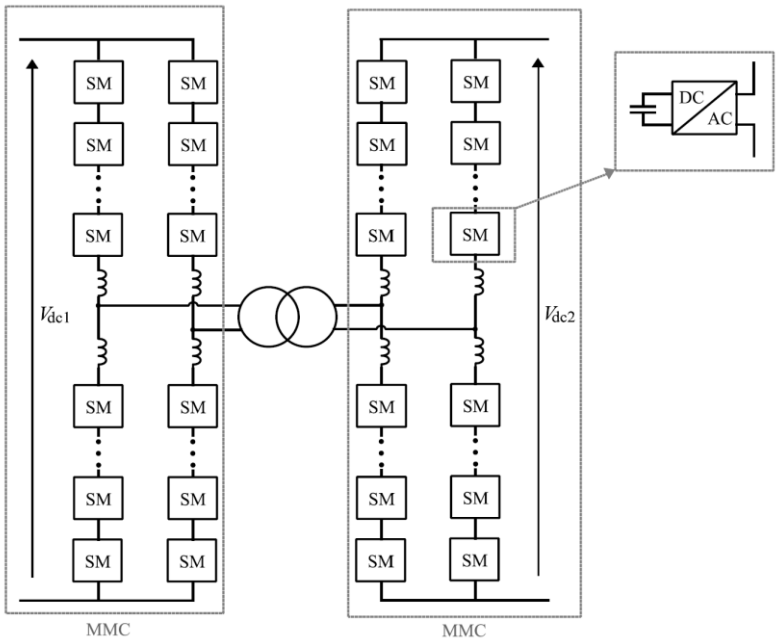


Figure 2-2 Modular Multilevel DAB [3].

2.1.1.1 Two-Level High-Voltage DAB

As shown in Figure 2-1, this topology is based on two two-level voltage-source converters (VSC) interconnected via an ac transformer. In HVDC applications, this topology has multiple downsides. The most important of them is the insulation and the electromagnetic interference (EMI) caused by high *dv*/*dt* in this topology [3].

2.1.1.2 Modular Multilevel DAB

The modular multilevel DAB consists of two ac/dc modular multilevel converters (MMCs) connected via an ac transformer, as depicted in Figure 2-2. The transferred power is controlled by applying an appropriate ac waveform at the terminals of the transformer [13]. The challenge of this topology is to design a high-voltage/power transformer operating at medium frequency. This challenge can be addressed by making a tradeoff between the size of the transformer and the switching losses of the MMCs [14]. As the modular multilevel DAB requires two fully rated MMCs, the overall size and cost of the system are significant. The main advantages of this topology are reliability, modularity, and scalability, making it an excellent solution for high-power/voltage applications at small conversion ratios [15].

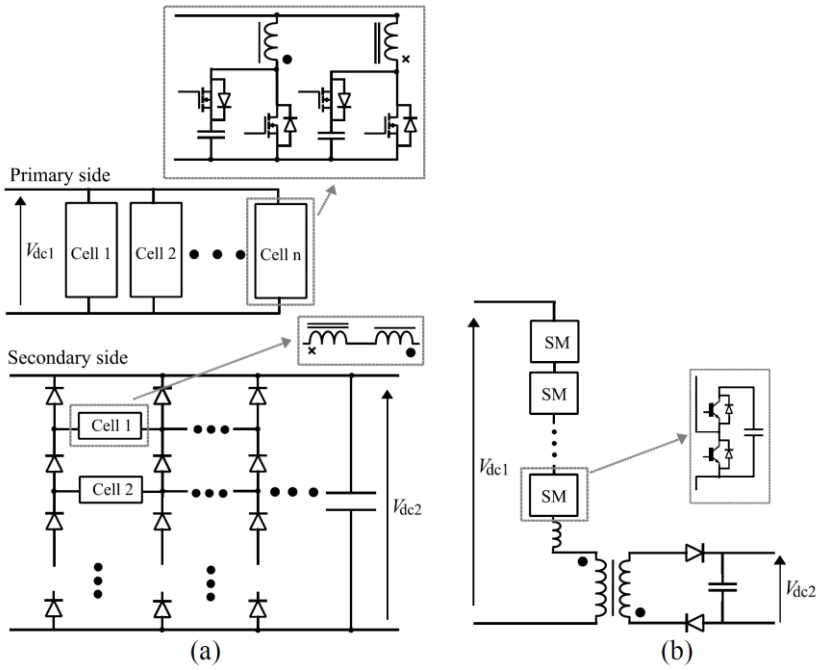


Figure 2-3 a) Modular dc/dc converter based on flyback/forward, b) dc/dc converter based on the flyback/forward with centralized coupled inductor [4].

2.1.2 Flyback/Forward Based Topologies

For high-voltage levels, some circuits are designed based on one coupled inductor and a string of SMs. Others use multiple coupled inductors in an isolated modular structure [16]. These two types are illustrated in Figure 2-3. These structures are suitable for high conversion ratios. However, having a high current in the centralized inductor and insulation requirements in the modular structure limits the application of these topologies to low-power cases [17].

2.2 Non-Isolated Topologies

There exist many types of non-isolated dc/dc converters, categorized as dc autotransformer, resonant converter, and dc modular multilevel.

2.2.1 DC Autotransformer

This topology consists of two high-voltage dc/ac converters connected in series on the dc ports and connected via an ac transformer on the ac side, as shown in Figure 2-4. The difference

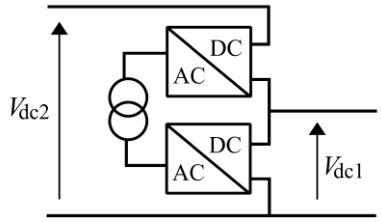


Figure 2-4 DC autotransformer [4].

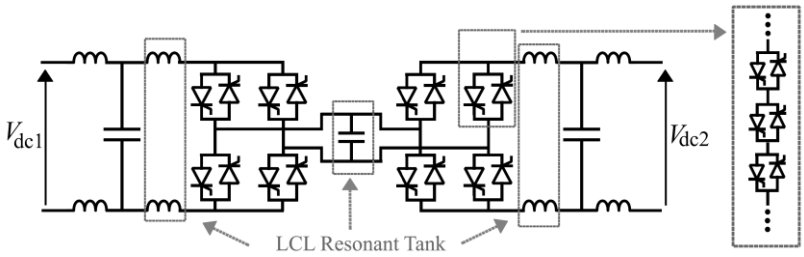


Figure 2-5 Single-stage resonant converter [15].

between this topology and DAB topologies is that only part of the transmitted power is processed by the ac transformer, reducing overall losses and the transformer rating. Moreover, the rating of the dc/ac converters is decreased because of their series connection. The advantages of this topology disappear when the conversion ratio increases; hence it is suitable for medium and low conversion ratios [15].

2.2.2 Resonant Converter

The idea behind this topology is to use the resonance to step up the voltage and achieve soft switching. As illustrated in Figure 2-5, the dc-dc conversion is accomplished using a dc-ac-dc chain. This topology offers a high conversion ratio. However, the passive components must tolerate high electrical stresses, and since all the power passes through the resonant elements, their current and voltage ratings are very high. These downsides limit this converter to medium power application at a medium conversion ratio [18].

2.2.3 DC Modular Multilevel Converter

This topology uses the main idea of the dc/ac MMC to generate voltages and currents at different frequencies. As shown in Figure 2-6, two different current loops exist, dc and ac loops. The dc current is responsible for the exchange of power between dc-links. The ac current is

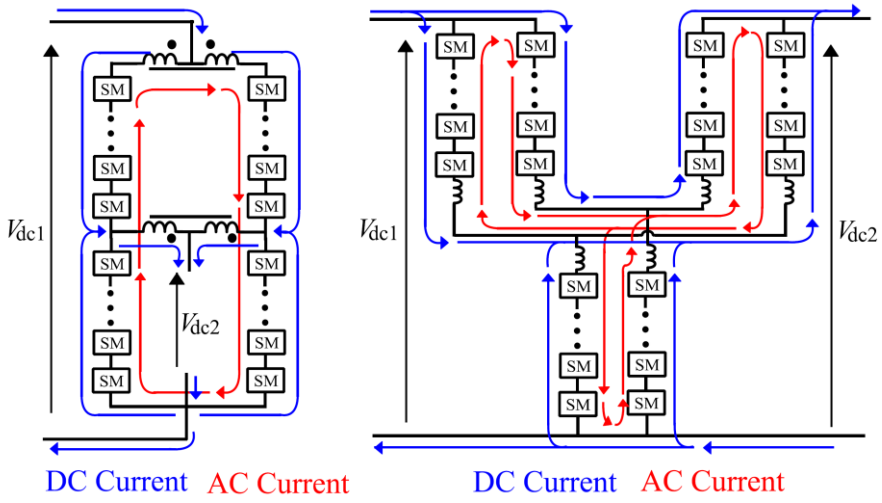


Figure 2-6 dc modular multilevel, a) ac current filtering with filter, b) ac current filtering by control actions [3].

generated to neutralize the dc power flow and make the average absorbed power by the arms zero [19]. To prevent the ac current from leaking into dc-link, two approaches can be used 1) use of passive filters [19], [7]. 2) control actions [20]. These two approaches are depicted in Figure 2-6. The size of passive components can be reduced by increasing the switching frequency. The dc modular multilevel has the advantages of scalability, modularity, and high reliability. However, the need for high ac circulating current in applications with high conversion ratios limits its operation to low or medium conversion ratios [3].

2.2.4 DC/DC MMC

The dc/dc MMC with passive filters has the lowest number of components and the simplest structure compared to the other MMC-based dc/dc converters (like the modular multilevel DAB and the dc MMC without the passive components). Therefore, it is selected as the focus of this study. From now on, the dc modular multilevel converter with passive filters is called the dc/dc MMC. The literature on the dc/dc MMC is reviewed from different perspectives in the following subsection.

2.2.4.1 Design

Different control methods were proposed for the dc/dc MMC [21-24], which tried to reduce the ac circulating current. The minimization of the ac circulating current is one common interest among researchers because it increases converter losses and the current rating of electrical

components. However, there exists a serious limitation in the conventional topology of the dc/dc MMC (i.e., the dc/dc MMC proposed in [7], which uses an equal and fixed number of half-bridge based submodules (HBSMs) in each arm) which prevents further reduction of the ac circulating current as explained in the following. In [25], it was shown that as the phase difference gets closer to 180^{o}, the amplitude of the circulating current reduces; however, a higher ac voltage is required to be generated by the arms. In [23], it was stated that because the required amplitude of the arm ac voltage increases when the phase-difference approaches 180^{o}, the number of feasible operation points in the conventional topology of the dc/dc MMC is limited. This is because, at some operating points, the generation of the required maximum and minimum voltages of the arms is not feasible by the conventional topology of the dc/dc MMC. Two major limitations of the conventional topology of the dc/dc MMC are

1. Due to the fixed number of HBSMs in the conventional dc/dc MMC, the number of feasible operating points is limited, especially those located near a phase difference of 180^{o}. This problem becomes more severe when the conversion ratio is near 1. This problem imposes higher conduction losses and current rating in the converter.

2. In each operating point, arms are required to generate a specific range of voltages which are not equal for upper and lower arms. Therefore, each arm needs a different number and even types of submodules (SMs) (e.g., half-bridge or full-bridge). However, the inefficient design of the conventional topology assumes the use of an equal number of HBSMs in both arms which increases the total number of SMs and the conduction losses.

Motivated by the aforementioned problems, an augmented design method for the dc/dc MMC that considers both the control (the phase-difference between arms ac voltages) and the hardware (type and number of SMs) aspects of the converter needs to be developed.

2.2.4.2 Operation of the Hybrid DC/DC MMC

To bring more functionality to the dc/dc MMC, the concept of hybrid topologies was proposed in [7, 9, 23, 26]. A typical hybrid topology of the dc/dc MMC employs a combination of full-bridge-based submodules (FBSMs) and HBSMs. In [7], it was shown that when the conversion

ratio is close to unity, a combination of the FBSMs and HBSMs is needed for the converter to operate properly. The authors in [26] proposed a hybrid dc/dc MMC with FBSMs in the upper arm and HBSMs in the lower arm to provide fault-blocking capability and step-up operation. To increase the power transfer capability and attenuate the ac circulating current in the dc/dc MMC, a hybrid topology with a combination of HBSMs and FBSMs in each arm was presented in [23]. Adding FBSMs enables the arms to generate negative voltages, which is the key to extend the swing range of arms voltages. In [9], an augmented design of the dc/dc MMC, which tries to remove the limitations of the conventional topology, was proposed. This is realized by selecting the number of HBSMs and FBSMs based on the minimum and maximum arms voltages. The previous studies did not determine any limitation on reducing the ac circulating current and increasing the power transmission in the hybrid dc/dc MMC. They assumed that each arm voltage could be generated by having enough HBSMs and FBSMs. However, the simulation studies show that the operation of the hybrid dc/dc MMC is limited by the capacitors voltages unbalance. An analytical study of the capacitors voltages balance of the hybrid dc/dc MMC is missing in the literature.

2.2.4.3 Fault-Tolerant Operation

The dc/dc MMC and the dc/ac MMC benefit from a modular structure that contains many semiconductor switches. In such topologies, switch failure is a common issue which is referred to as SM fault. As these converters usually transmit a large amount of power, they should remain operational in the event of SM failure. Fault-tolerant operation of the dc/ac MMC was investigated in [5, 27-33]. Adding redundant SMs to the converter was proposed in [27-29]. In this strategy, all the SMs are treated equally in normal operation. When one of the SMs fails, it can be bypassed without harming the converter operation because there already exist additional SMs. The authors of [30] proposed an optimized version of the redundant SMs strategy, which reduces SM capacitor voltage, decreases switching frequency in normal operation, and provides a fast fault restoration in the case of SM fault. In [31], a resilient framework is realized by adding a new SM to each arm to smooth the transient mode and handle multiple SMs faults. A dc/ac MMC based on a novel SM circuit is proposed in [32], which guarantees the operation of the converter despite multiple SM faults. The authors of [33]

attempted to remove the need for communication systems in fault-tolerant operation by using only arms electrical parameters without knowing the number of faulty SMs. In [5], a full-bridge-based SM with half of the voltage rating of the half-bridge-based SMs is added to each arm to suppress the excessive ac circulating current in $2N+1$ modulation and provide fault-tolerant operation which can only handle a few SMs failure in the arm.

Research on the dc/dc MMC is limited to the converter modeling [9, 10, 25, 34, 35] and different converter control methods [21-24]. However, the fault-tolerant operation of this converter has not been studied yet. Although the dc/dc MMC is similar to the dc/ac MMC, its operation principle is mostly different. Therefore, the fault-tolerant operation of dc/dc MMC needs to be studied separately.

2.2.4.4 Asymmetrical Operation

In power systems, parameters of different components may have $\pm 5\%$ tolerance, and it could increase to $\pm 30\%$ worst-case tolerance due to aging, temperature stresses, field stress, radiation, and distorted operation [34], [35]. Moreover, because of control malfunctioning and components failure [11], the generated voltages by the dc/dc MMC might deviate from the reference value by a few percent. With these uncertainties, the dc/ac and the dc/dc MMC can be forced to operate in an unsymmetrical condition. This condition means that the impactful parameters like the generated ac voltage and/or the arm inductance are not equal in different phase-legs, and each phase-leg operates at different operating points. Some studies investigated the operation of the dc/ac MMC in the unsymmetrical condition. Authors in [36] designed a robust controller based on an optimum guaranteed cost control theory to ensure the safe operation of the dc/ac MMC in unsymmetrical conditions. In [37], modeling and design of the dc/ac MMC with parametric uncertainties were discussed. However, with the available steady-state models of the dc/dc MMC [21, 22, 25], the unsymmetrical operation of this converter cannot be studied. This is because the connection between the operation of different phase-legs is lost by ignoring the dc-link impedance. It means changes in the operating point of one phase-leg would not affect the other ones. As a result, a steady-state model that, unlike the previous models, can show the dc/dc MMC behavior in the unsymmetrical condition is demanded.

2.2.4.5 Control

Recently, design [25], [9], and modeling [12, 38, 39] aspects of the dc/dc MMC have been studied. The control aspect of the dc/dc MMC is studied in [21-24]. In [24], a capacitor voltage balancing strategy that reduces the circulating current was proposed. The operation principle of the hybrid dc/dc MMC was explained in [23], where the power transfer capability is improved by utilizing the elevated capacitors voltages. In [22], the full-state regulation of the dc/dc MMC was proposed to minimize the ac circulating current. Authors in [21] introduced a new closed-loop control of the dc/dc MMC to ensure energy balancing in the load transient and steady-state. To date, all the suggested control approaches are based on proportional-integral (PI) controllers. This type of controller suffers from the complexity of handling multiple control objectives and poor transient performance. As the number of control objectives grows, the number of needed PI loops increases resulting in the complexity of the overall control structure and the difficulty of PI parameters tuning.

In the previous literature, to overcome the disadvantages of the PI-based controllers, researchers widely used the model predictive control (MPC) for the control of the dc/ac MMC [40-45]. In [40], the computational burden of the MPC was reduced by decoupling the capacitors voltage balancing from the MPC algorithm. This task was realized in a separate sorting algorithm. By solving the Diophantine equations, the online optimization and presence of the weighting factors were avoided in [41], which resulted in a lower computational burden and enhanced reliability. A new modulated MPC for the dc/ac MMC was proposed in [44], where it used two predetermined voltage levels to build the voltage reference. To improve the computational burden and steady-state performance and eliminate the need for weighting factors, a new MPC approach, called the sliding-discrete control set, was introduced in [45]. To date, a few studies [46, 47] developed MPC methods for the isolated dc/dc MMC. In general, this topology is built of two dc/ac MMCs which are connected via an ac transformer. In [46], a modulated MPC approach was proposed for the inductor-less MVDC MMC, which reduces the computational burden by reformulating the underlying optimization problem. The author in [47] proposed a Finite Control Set MPC to regulate the output voltage. This is

achieved by defining a cost function, including the output voltage, which yields the optimum number of SMs in the next control period.

Despite extensive studies on the application of the MPC method in the control of the MMC-based converters, the MPC method has never been used for the control of the dc/dc MMC introduced in [7]. Although these converters, the dc/dc and the other MMC-based converters, share a similar topology, crucial differences exist in the operation principle. Moreover, the control objectives and the control variables of these two converters are different. Therefore, the developed MPC methods for the other MMC-based converters cannot be used directly for the dc/dc MMC. Therefore, developing a tailored MPC approach for the dc/dc MMC would be beneficial to improve the dynamic performance.

2.2.4.6 Fault-Blocking Capability

Fault-blocking capability is an important feature that should be realized in the dc/dc MMC. This feature allows the dc/dc MMC to block the fault current from both dc sides. The past literature [7, 21, 26] proposed that using FBSMs in the upper arm of the dc/dc MMC would provide the bidirectional fault-blocking capability. However, replacing the HBSMs with the FBSMs will increase the losses significantly; this is because FBSMs have twice the number of semiconductor switches compared to the HBSMs. Moreover, in these studies, the FBSMs are treated as HBSMs in the normal operation mode, while they can generate negative voltages, unlike the HBSMS. Therefore, realizing an efficient fault-blocking capability is still missing in the literature.

Chapter 3 Augmented Design of the DC/DC MMC

In this chapter, first, the operation principle and the mathematical model of the conventional dc/dc MMC are presented. Then the proposed augmented design is explained in detail. This approach includes two main parts, analytical and semi-analytical, which are elaborated in this report. In the end, two different case studies are presented to verify the effectiveness of the proposed method. In the first case study, a medium voltage dc/dc MMC is designed by the proposed augmented approach. The results from the analytical and semi-analytical parts are compared with the results from the simulation study. In the second case study, the impact of system parameters on the converter performance is studied.

3.1 Topology and Mathematical Modeling of the Conventional DC/DC MMC

3.1.1 Topology

The circuit of a dc/dc MMC with two phase-legs is illustrated in Figure 3-1. Each phase-leg includes two arms consisting stack of HBSMs and an arm inductor L, which is necessary for injecting an ac circulating current. The voltage of dc-link 2 V_{DC2} (input side) is assumed to be greater than that of dc-link 1 V_{DC1} (output side). The midpoints of the phase-legs are connected to the output dc-link via a large inductor L_0, which acts as a filter and prevents the leakage of the ac circulating current into the output side. The dc-link currents are denoted by I_{DC1} and I_{DC2}. The voltages generated by the upper and lower arms of phase-leg-j are denoted by $v_{j,u}$ and $v_{j,l}$, and arms current are denoted by $i_{j,u}$ and $i_{j,l}$. In the rest of the chapter, superscripts related to the phase-leg are removed, and due to similarity, the operation of one phase-leg is analyzed.

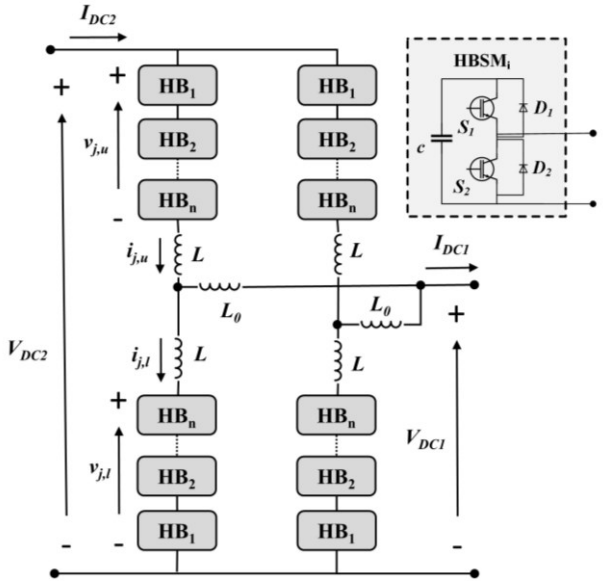


Figure 3-1 Conventional topology of the dc/dc MMC.

3.1.2 Mathematical Modeling

Assuming that the converter transmits the nominal power P from dc-link 2 to dc-link 1, each arm processes an equal portion of power P_{DC} which can be calculated as follows:

$$P_{DC} = \frac{1-D}{M}.P, D = \frac{V_{DC1}}{V_{DC2}} \tag{3-1}$$

where M is the number of phase-legs, and D is the dc-links voltage ratio. In the dc/dc MMC, to neutralize the effect of the dc power flow, the upper and lower arms of each phase-leg should exchange active ac power P_{AC}. To stabilize the capacitors voltages of each arm, the summation of P_{DC} and P_{AC} must be zero. The exchange of an active ac power can be possible by adding an ac voltage to the arms reference voltage generating an ac circulating current, which ideally only flows through the arms and does not penetrate the dc links. The arm ac voltage could have any frequency. Higher frequencies decrease the size of passive components, and on the other hand, increase the switching frequency and losses. The exchanged active ac power between arms can be calculated as

$$P_{AC} = -P_{DC} \tag{3-2}$$

$$P_{AC} = \frac{X_{L0}}{2(X_L^2 + 2X_L X_{L0})} \hat{v}_{u,AC}.\hat{v}_{l,AC}.\sin(\varphi) \tag{3-3}$$

where $\hat{v}_{u,AC}$ and $\hat{v}_{l,AC}$ are the amplitudes of the upper and lower arms ac voltages, respectively; and X_L and X_{L0} are the reactances of the inductors L and L_0, respectively. To enable the exchange of active ac power, there should be a phase difference φ between the arms ac voltages. When P is positive, it could change between π to $3\pi/2$; and when P is negative, it could vary from $\pi/2$ to π creating different operating points [24]. Changing the phase difference φ while the converter transmits the same amount of power can affect the converter performance significantly.

The arms reference voltages in the time-domain are shown in (3-4) and (3-5).

$$v_u(t) = (V_{DC2} - V_{DC1}) + \hat{v}_{u,AC}\cos(\omega t + \varphi) \tag{3-4}$$

$$v_l(t) = V_{DC1} + \hat{v}_{l,AC}\cos(\omega t) \tag{3-5}$$

where the arms reference voltages are denoted by v_u and v_l, respectively. The dc components of the arms voltages regulate the dc power flow. In the steady-state, these dc voltages are almost constant; however, in the transients, they may have different values to regulate the dc power flow. In this study, the steady-state operation of the dc/dc MMC is investigated. The arms currents also have dc and ac components. The dc part enables the exchange of the dc power between dc links, and the ac part balances the capacitors voltages. The ac and dc components of the upper and lower arms can be calculated by

$$I_{u,DC} = \frac{P}{M \cdot V_{DC2}} \tag{3-6}$$

$$I_{l,DC} = \frac{P}{M}\left(\frac{1}{V_{DC2}} - \frac{1}{V_{DC1}}\right) \tag{3-7}$$

$$\vec{i}_{u,AC} = -\frac{(X_0 + X_L)\vec{v}_{u,AC} + (X_0)\vec{v}_{l,AC}}{j(X_L^2 + 2 \cdot X_L \cdot X_0)} \tag{3-8}$$

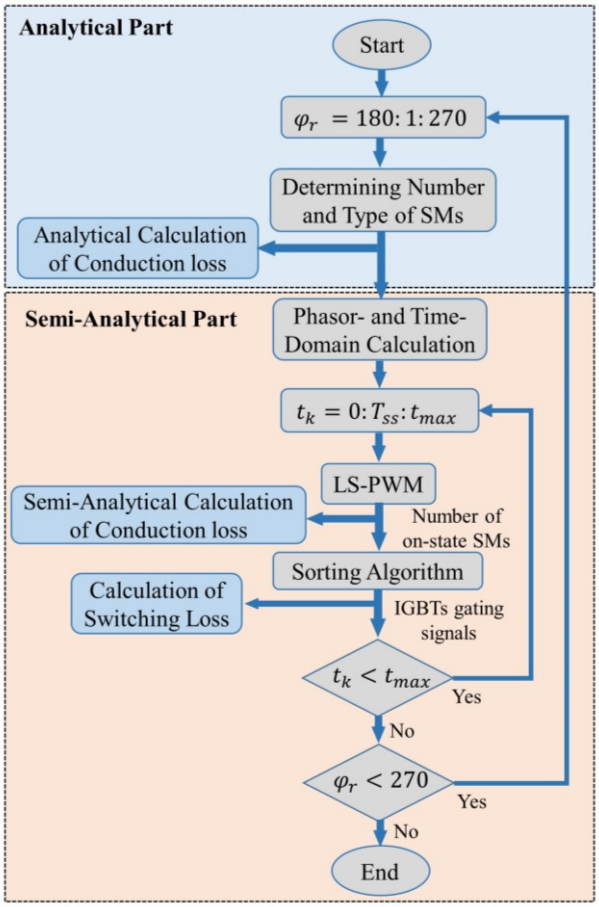


Figure 3-2 Flowchart of the proposed augmented design.

$$\vec{i}_{l,AC} = -\frac{(X_0 + X_L)\vec{v}_{l,AC} + (X_0)\vec{v}_{u,AC}}{j(X_L^2 + 2 \cdot X_L \cdot X_0)} \tag{3-9}$$

where $I_{u,DC}$ and $I_{l,DC}$ are the dc components of the arms current. The expressions in (3-8) and (3-9) are obtained using the steady-state equations in [25], in which $\vec{i}_{u,AC}$ and $\vec{i}_{l,AC}$ are the upper and lower arms ac currents in the phasor-domain. Similarly, $\vec{v}_{u,AC}$ and $\vec{v}_{l,AC}$ are the upper and lower arms ac voltages in the phasor-domain, respectively.

3.2 Proposed Augmented Design

The proposed augmented design, shown in Figure 3-2, is composed of two major parts: analytical and semi-analytical. Both parts are computationally efficient and are executed for all

possible operating points, i.e., phase differences. In the analytical part, the number and types of SMs are specified, and an approximation of the conduction loss is calculated. In the semi-analytical part, the switching loss is found, and the accuracy of the conduction loss calculation is improved as compared to the analytical method. The semi-analytical part uses the simplified steady-state equations of the dc/dc MMC beside the modulation algorithm (e.g., pulse-width modulation (PWM)) and the sorting algorithm for capacitors voltages balancing. The PWM and sorting algorithms are modeled in detail to account for their central effect on the switching frequency of the converter. In the end, having the converter losses, the amplitude of circulating current, and the number of SMs at different phase differences, the optimum operating point, and the corresponding topology can be found.

3.2.1 Analytical Part

At each operating point, this module 1) calculates the needed arm ac voltage, 2) determines the number and type of SMs, and 3) estimates the converter conduction loss via analytical expressions.

3.2.1.1 Determining Number and Type of SMs

Earlier studies showed that the ac circulating current is minimized when the upper and lower arms ac voltages are equal. Hence, in this study, this approach is adopted [23, 24]. With this assumption, the needed ac voltage can be calculated from (3-3) as follows:

$$v_{AC} = \sqrt{\frac{2.P_{DC}.X_e}{\sin\varphi}} \tag{3-10}$$

$$X_e = \frac{X_{L0}}{X_L^2 + 2X_L X_{L0}} \tag{3-11}$$

Using the calculated ac voltage, the minimum and maximum voltages of each arm can be obtained by

$$v_{arm,min} = V_{arm,DC} - v_{AC} \tag{3-12}$$

$$v_{arm,max} = V_{arm,DC} + v_{AC} \tag{3-13}$$

As the phase difference approaches 180°, from one point onwards, the ac component of arm voltage v_{AC} would be higher than the dc component $V_{arm,DC}$. In this case, the arm minimum voltage would be a negative voltage. To empower the arm to generate negative voltage, full-bridge-based SMs (FBSMs) must be used. To be efficient, the number of the needed FBSMs at each operating point is calculated regarding the minimum arm voltage. Accordingly, the number of FBSMs $n_{arm,f}$ can be found by

$$n_{arm,f} = ceil\left[-\frac{v_{arm,min}}{V_{CN}}\right] \tag{3-14}$$

where *ceil*[A] finds the closest integer greater than A, and V_{CN} is the SM nominal voltage. Total number of SMs n_{arm} at each operating point is calculated based on the needed maximum arm voltage $v_{arm,max}$ as shown in (3-15). As discussed earlier, $n_{arm,f}$ number of total SMs must be FBSMs to enable the generation of the minimum arm voltage. As a result, to reduce losses, HBSMs are selected for the rest of the required SMs. The number of HBSMs $n_{arm,h}$ are found by (3-16).

$$n_{arm} = ceil\left[\frac{v_{arm,max}}{V_{CN}}\right] \tag{3-15}$$

$$n_{arm,h} = n_{arm} - n_{arm,f} \tag{3-16}$$

3.2.1.2 Analytical Calculation of Conduction Loss

At each time instant, the arm current flows through either an IGBT or diode of an SM depending on the current direction and SM status. In HBSM, the current passes through only one semiconductor switch. While in FBSM, it flows through two semiconductor switches. Assuming an equal voltage drop for diodes and IGBTs, V_{drop}, the total voltage drop caused by semiconductor switches $V_{arm,drop}$ in the current path can be expressed as

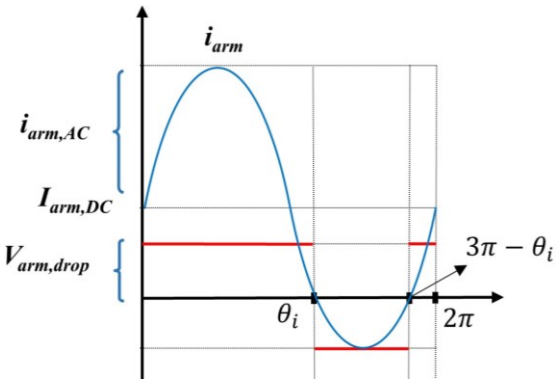


Figure 3-3 Arm current and voltage drop due to arms semiconductor switches.

$$V_{arm,drop} = (n_{arm,h} + 2.n_{arm,f}) \cdot V_{drop} \tag{3-17}$$

The arm current and the total voltage drop are both illustrated in Figure 3-3. The conduction loss caused by the total voltage drop can be calculated by

$$P_{arm,cond}^{loss} = (\int_0^{2\pi} V_{arm,drop} \cdot |i_{arm}|\, d\theta)\ /(2\pi) \tag{3-18}$$

After taking the integration, the following terms appear for the conduction loss in the upper and lower arm:

$$P_{u,cond}^{loss} = 2V_{u,drop} \cdot \left(I_{u,DC} \cdot (\theta_{iu} - \pi) - \hat{\imath}_{u,AC} \cdot \cos\theta_{iu}\right)/(\pi) \tag{3-19}$$

$$P_{l,cond}^{loss} = V_{l,drop} \cdot \left(-I_{l,DC} \cdot \theta_{il} + 2\hat{\imath}_{l,AC} \cdot cos\,\theta_{il}\right)/(\pi) \tag{3-20}$$

$I_{u,DC}$ and $I_{l,DC}$ can be obtained using (3-6) and (3-7); and the amplitude of arms ac currents, $\hat{\imath}_{u,AC}$ and $\hat{\imath}_{l,AC}$, can be calculated from (3-8) and (3-9). θ_{iu} and θ_{il} are the angles at which the arms currents become zero, and they can be calculated by the following expression:

$$\theta_{i,arm} = \sin^{-1}\left(\frac{-I_{arm,DC}}{i_{arm,AC}}\right) \tag{3-21}$$

The derived analytical expressions for the conduction losses facilitate fast conduction loss estimation at each operating point without detailed simulation of the converter.

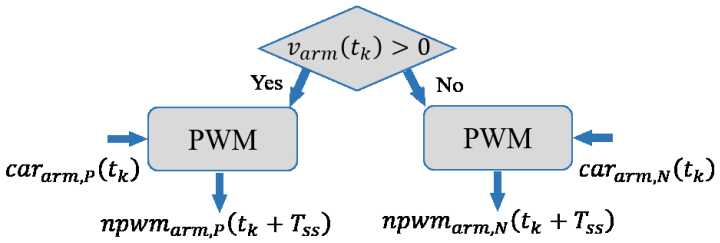


Figure 3-4 Implementation of the PWM in the semi-analytical approach.

3.2.2 Semi-Analytical Part

The main goal of this part is to estimate the switching frequency of the converter to calculate the switching losses at each operating point. In the dc/dc MMC, the switching frequency is influenced by two nonlinear functions: the modulation technique (e.g., PWM) and the sorting algorithm used for capacitors voltages balancing. Therefore, to estimate the switching frequency accurately, unlike the converter dynamic, which is simplified by the steady-state equations, the PWM and sorting algorithm are modeled in detail. The main idea is to simulate the simplified converter for a short period of time at each operating point and then calculate the switching frequency.

3.2.2.1 Phasor- and Time-Domain Calculations

The arms reference voltages in the time-domain can be calculated using (3-4) and (3-5). To find the arms currents in the time-domain, the phasor equations (3-8) and (3-9) should be transformed into the time-domain equations as follows:

$$i_u(t) = I_{u,DC} + \left|\vec{i}_{u,AC}\right| \cdot \cos(\omega t + \measuredangle \vec{i}_{u,AC}) \tag{3-22}$$

$$i_l(t) = I_{l,DC} + \left|\vec{i}_{l,AC}\right| \cdot \cos(\omega t + \measuredangle \vec{i}_{l,AC}) \tag{3-23}$$

By ignoring the high order harmonics of the arm current and the effect of capacitors voltages fluctuations, the arms current can be estimated by (3-22) and (3-23).

3.2.2.2 PWM

In this step, using a PWM technique, the number of SMs that should be turned on in the next sampling time is determined. Because the exact modulation technique is implemented in this

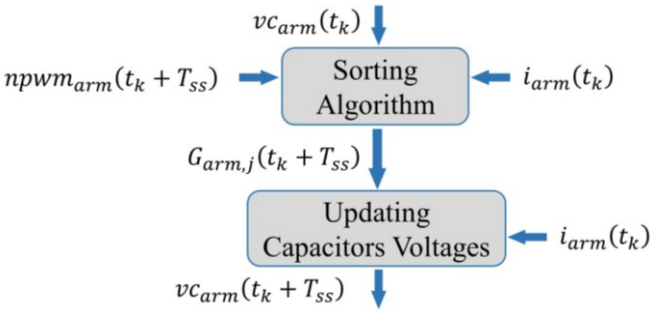


Figure 3-5 Sorting algorithm and updating capacitors voltages in the semi-analytical approach.

study, any type of PWM techniques can be considered without modeling difficulties. Each arm needs two different sets of carriers, one for positive values of the reference voltage $car_{arm,P}$ and another one for negative values $car_{arm,N}$. $car_{arm,P}$ considers FBSMs and HBSMs whereas $car_{arm,N}$ only considers FBSMs. By comparing the arm reference voltage with the appropriate set of carriers at $t=t_k$, the number of on-state SMs $npwm_{arm}$ in the next sampling time $t=t_k+T_{ss}$ can be obtained. In Figure 3-4, a flowchart of this process is presented.

3.2.2.3 Sorting Algorithm

In a dc/dc MMC, the sorting algorithm determines the on-state SMs in the next switching period. Each sorting algorithm has a distinctive notion, but almost all of them use capacitors voltages and arms current. To account for the effect of the sorting algorithm on the switching frequency, the capacitor voltage fluctuations around the nominal voltage should be considered. In the proposed semi-analytical approach, the exact sorting algorithm is implemented, making it possible to use this approach for any other sorting algorithm. In this study, the sorting algorithm proposed in [48, 49] is used. The overall procedure of this part is depicted in Figure 3-5. When the arm voltage is positive, the sorting algorithm specifies the on-state SMs among HBSMs and FBSMs. However, when the arm voltage is negative, the sorting algorithm only takes FBSMs into consideration. The capacitors voltages of each arm vc_{arm}, the arm current i_{arm}, and the number of on-state SMs $npwm_{arm}$ are given to the sorting algorithm to determine the gating signals of all switches in the next sampling time $G_{arm,i}(t_k + T_{ss})$. Eventually, based on the SM status and the arm current, the capacitors voltages will be updated for the next sampling period. The capacitors voltages of off-state SMs remain without change, and for on-state SMs, the capacitors voltages change with respect to the arm current.

3.2.2.4 Semi-Analytical Calculation of Conduction Loss

In the presented analytical calculation of the conduction loss, an equal voltage drop is considered for IGBTs and diodes, which is not accurate. To improve the accuracy, the conduction loss can be calculated using the semi-analytical approach. The main idea is to determine the number of diodes and IGBTs conducting current at each time instant to estimate the conduction loss. The device conducting current in the SM can be determined based on the current direction and the SM status. As this is well-known for researchers, further explanation is avoided.

To find the voltage drop caused by HBSMs and FBSMs, first, the number of on-state HBSMs and FBSMs should be specified. Afterward, the voltage drops due to HBSMs, $Vd_{arm,h}$, and FBSMs, $Vd_{arm,f}$, can be calculated as follows:

$$Vd_{arm,h}(t_k) = o_{arm,h}(t_k).Vd_{h,on}(t_k) + (n_{arm,h} - o_{arm,h}(t_k)).Vd_{h,off}(t_k) \quad (3\text{-}24)$$

$$Vd_{arm,f}(t_k) = o_{arm,f}(t_k).Vd_{f,on}(t_k) + (n_{arm,f} - o_{arm,f}(t_k)).Vd_{f,off}(t_k) \quad (3\text{-}25)$$

where $o_{arm,h}$ and $o_{arm,f}$ denote the number of on-state HBSMs and FBSMs, respectively. The voltage drops of an on-state HBSM and FBSM are denoted by $Vd_{h,on}$ and $Vd_{f,on}$, and similarly, $Vd_{h,off}$ and $Vd_{f,off}$ are the voltage drop of a single off-state HBSM and FBSM. The wasted energy E_{arm} by $Vd_{arm,h}$ and $Vd_{arm,f}$ can be obtained by

$$E_{arm}(t_k) = (Vd_{arm,h}(t_k) + Vd_{arm,f}(t_k)).i_{arm}(t_k).T_{ss} + E_{arm}(t_k - T_{ss}) \quad (3\text{-}26)$$

Eventually, the conduction loss of one arm can be calculated by

$$P_{arm,cond}^{loss} = E_{arm}/t_{max} \quad (3\text{-}27)$$

where t_{max} is the upper bound of the simulation time.

3.2.2.5 Calculation of Switching Loss

By counting the rising edges of the switches gating signals $G_{arm,i}$ produced by the sorting algorithm and dividing by the upper bound of simulation time t_{max}, the switching frequency

of each IGBT and diode can be obtained. Using the obtained switching frequencies, the switching loss of each HBSM and FBSM can be calculated, and the total switching loss in one arm would be the summation of SMs' losses. This study has ignored the effect of conjunction temperature and collector current on the calculation of switching and conduction losses.

3.3 Design Example 1: 20 MW DC/DC MMC

In this section, using the proposed augmented method, an efficient dc/dc MMC is designed for a medium-voltage application. Then, the designed converter is simulated in the MATLAB/Simulink environment to analyze its steady-state and transient performances. Finally, to verify the accuracy of the estimated losses and amplitude of ac current, the results from simulation studies are compared with the results of the augmented design method. In this chapter, the losses are calculated based on the datasheet in [50].

3.3.1 Optimum Converter Design Using the Augmented Method

Using the proposed semi-analytical approach, approximated information on the performance of the conventional topology and the converters designed by the augmented approach at each phase difference are obtained, as shown in Figure 3-6. This information includes the converter total loss, number and type of SMs, and the amplitude of the ac circulating current. In this study, the number of SMs is defined as the number of HBSMs plus twice that of FBSMs. The goal is to find the optimum operating point (phase difference) with respect to the total loss, the number of SMs, and the amplitude of ac circulating current. In the intended application, the nominal power is 20 MW, and the dc-links voltages are 20 kV and 14 kV. As shown in Table 3-I, the SM capacitance is selected so that the stored energy in each SM is 40 kJ/MVA, as suggested in [51]. The phase-inductance is chosen large enough to suppress the ac circulating current from reaching the dc-link 1. The arm inductance is selected as a fixed value, and in the next section, the effect of the arm inductance will be discussed further.

Assuming that the SM nominal voltage is 2 kV, the conventional topology of the dc/dc MMC would have 10 HBSMs in each arm. This structure limits the operation of the converter, as shown in Figure 3-6. The optimum operating point in this topology is when the phase difference

equals 219°, which has the lowest total loss, and ac circulating current. This operating point in the conventional topology is called point B and is selected for comparison purposes. The augmented design provides the opportunity to extend the operation range of the converter, as demonstrated in Figure 3-6. To find the optimum operating point which leads to the optimum converter in the augmented design, the following guidelines can be adopted.

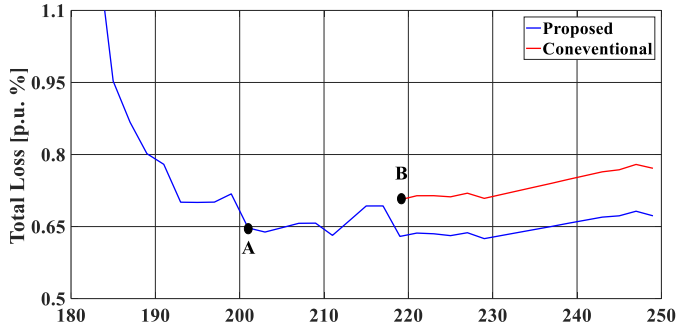
1. As shown in Figure 3-6, in the vicinity of 180°, although the ac circulating current is so small, the number of needed SMs is extremely large, which leads to operation with efficiency less than the conventional topology at point B. Therefore, there is no point in choosing operating points very close to 180°. Accordingly, operating points from 180° to 193° are removed from consideration in this case study.

2. One of the main purposes of the augmented design is to reduce the ac circulating current by extending the operating range of the converter. As a result, the optimum operating point should be a phase difference equal to or smaller than the closest operating point to 180° in the conventional topology. In this case study, it means that a phase difference larger than 219° (point B in the conventional topology) cannot be considered for the optimum operating point.

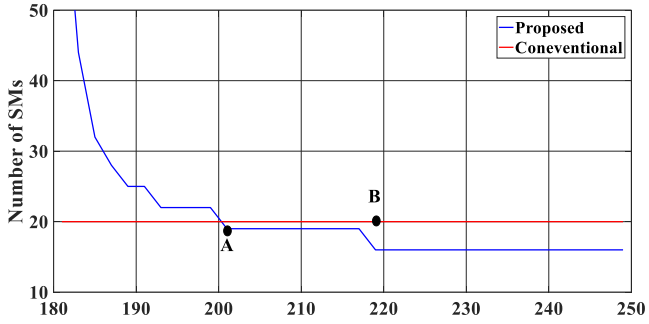
3. The two above conditions determine the lower and upper bounds of the optimum operating point. In this example, the optimum operating point can be selected from 193° to 219°. The preferred operating point in this range is the one that yields to lower total loss and number of SMs as compared to the conventional topology. In this study, the optimum operating point is selected as 201° (operating point A). By selecting this operating point, the number of HBSMs and FBSMs in each arm can be found. As shown in Table 3-I, the upper arm needs 6 HBSMs and 1 FBSMs, and the lower arm requires 11 HBSMs to operate at point A.

3.3.2 Simulation Results of the Designed Converter

The designed converter by the proposed augmented design method is simulated to investigate the converter performance in steady-state and transient modes. The main parameters of the designed converter are given in Table 3-I, and the simulation results are shown in Figure 3-7.



(a)



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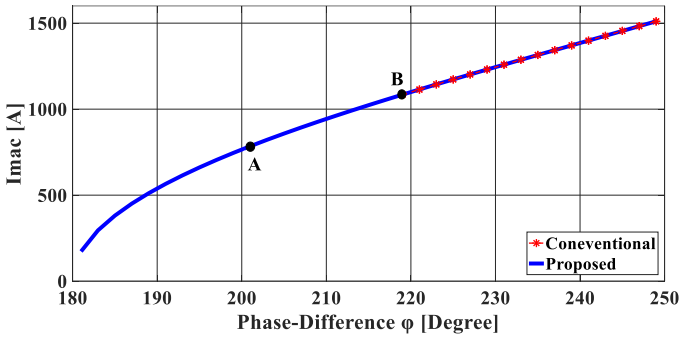


(c)

Figure 3-6 (a) Total loss comparison (b) Number of SMs (c) Amplitude of ac circulating current.

The number and type of SMs in each arm are determined by the augmented design method. The results are for medium voltage application of dc/dc MMC.

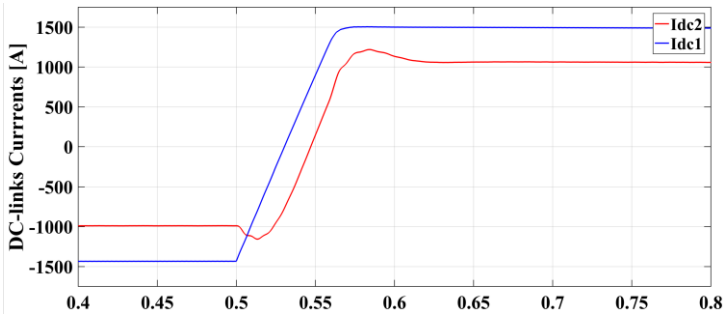
The dc links are modeled by the ideal dc voltage sources. Before t=0.5 s, P = -20 MW, and afterward, the direction of the power flow changes, and P = 20 MW. The dc links and arms currents are shown in Figure 3-7(a) and Figure 3-7(b), respectively. As shown, $I_{DC1}$and I_{DC2} follow the new reference after t=0.5 s quickly, and reach the steady-state after 0.5 s. Moreover, the rates of change of the dc-links currents are relatively slow, which is due to the large

Table 3-I
Main Parameters of the Simulated Converter

Common Parameter	**Symbol**	**Value**
Rated Power	S	20 MW
DC-Link1	V_{DC1}	14 kV
DC-Link2	V_{DC2}	20 kV
Arm Inductance	L	0.8 mH
Phase Inductance	L_0	0.26 H
SM Capacitance	C	10 mF
SM Nominal Voltage	V_{CN}	2 kV
Operating Frequency	f_S	360 Hz
Designed Converter at A	**Symbol**	**Value**
Number of Upper Arm HBSMs	n_u	6
Number of Upper Arm FBSMs	n_{uf}	1
Number of Lower Arm SMs	n_d	11
Conventional Topology at B	**Symbol**	**Value**
Number of Upper Arm HBSMs	n_u	10
Number of Lower Arm SMs	n_d	10

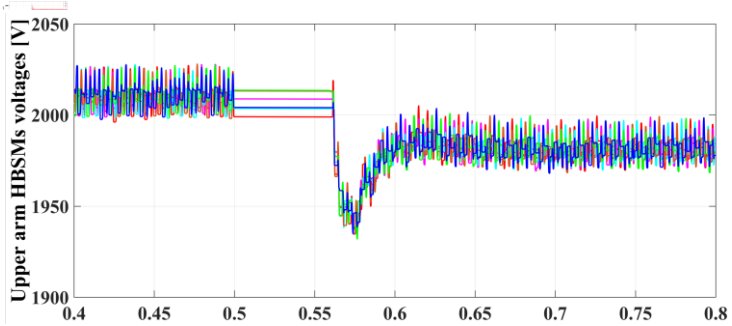
inductors implemented in each phase-leg. As shown, the arms currents have two components: the dc and ac parts. The amplitude of the ac part remains unchanged. After t=0.5 s, the dc part increases to accommodate the change in the power flow direction. In Figure 3-7(c) and (d), the capacitors voltages of HBSMs and FBSM in the upper arm are shown; all capacitors are bypassed for a while after the power change and after passing the transient-state, the capacitors voltages reach the steady-state. Finally, the phase difference between arms ac voltages is illustrated in Figure 3-7(e). In the steady-state, when P is -20 MW, φ =159°; when P is 20 MW, φ =201° (the selected optimum point). During the transient, the controller tries to maximize the exchanged ac power between arms; therefore, the phase difference is equal to 90° when the transferred power is a negative value, and similarly, the phase difference equals 270° when P is positive.

(a)

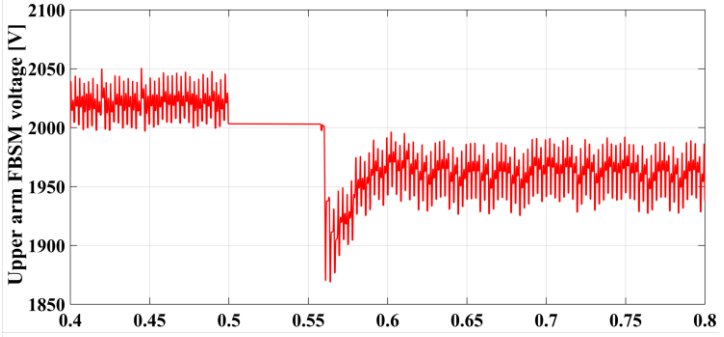


(b)

(c)



(d)



(e)

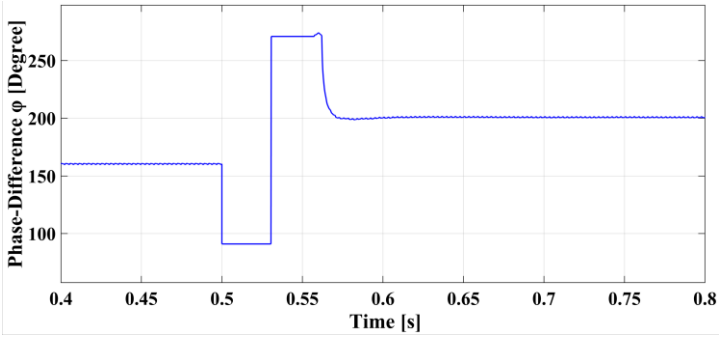
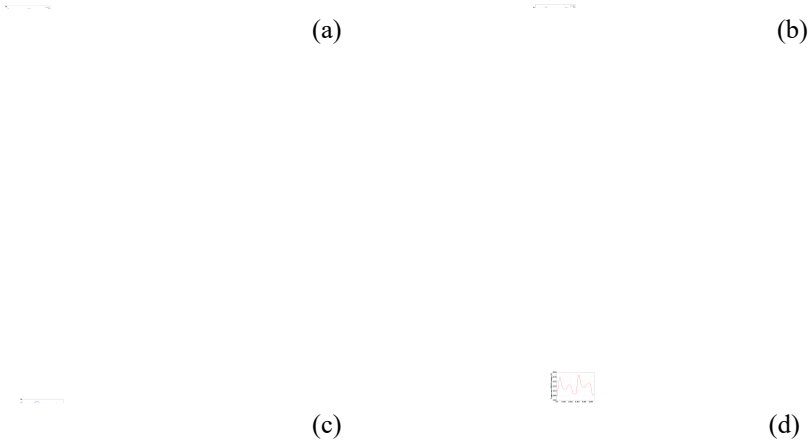


Figure 3-7 Simulation results of the 20 MW converter designed by the proposed augmented method, (a) DC links currents, (b) Arms current, (c) Capacitors voltages of HBSMs in the upper arm, (d) Capacitor voltage of FBSM in the upper arm, (e) Phase difference between ac voltage of upper and lower arms.



(a) (b)

(c) (d)

Figure 3-8 Zoomed in results of the designed converter, (a) The arms voltages, (b) The arms currents, (c) The upper arm HBSMs voltages, (d) The upper arm HBSMs capacitor voltages.

In Figure 3-8, two cycles of the simulation results, when P=-20 MW, are shown to explain the basic operation principle of the converter. The arms voltages are illustrated in Figure 3-8(a). As shown, the arms voltages have dc and ac components in which the dc component controls the dc power flow, and the ac component induces the ac circulating current. The upper arm voltage has a dc part of 6 kV and an ac component of 8 kV. The used FBSMs in the upper arm make the generation of negative voltage possible, which is important to improve the converter performance. The dc component in the lower arm is equal to 14 kV, and the ac part is equal to 8 kV, which is the same as the upper arm. The arms currents are shown in Figure 3-8(b). Like the arms voltage, they have ac and dc components. The ac part is induced to neutralize the effect of dc power flow, and the dc power is responsible for exchanging power between dc links. The HBSMs and FBSMs voltages are exhibited in Figure 3-8(c) and Figure 3-8(d). As can be seen, the SMs capacitor voltages fluctuate with respect to the arm current.

Table 3-II
Comparison of the Conventional Topology at Operating Points A and the Designed Converter at Operating Point B (Design Example 1)

Operating points	**Operating point A (Modified topology)**		**Operating point B (Conventional topology)**	
	Augmented design	**Simulink**	**Augmented design**	**Simulink**
Conduction loss	Analytical: 23.4 kW, Semi-analytical: 24.4 kW	24.5 kW	Analytical: 33 kW, Semi-analytical: 34.3 kW	34 kW
Switching loss	40 kW	38.5 kW	36 kW	34.6 kW
Total loss (p.u. %)	0.64	0.63	0.7	0.69
Amplitude of ac current	0.78 kA	0.8 kA	1.08 kA	1.1 kA
Capacitance voltage ripple	26	28	48	52
Phase difference	201°		219°	
Number of SMs	19		20	

3.3.3 Comparison between Calculated Losses by Simulation and the Proposed Augmented Design

This subsection aims to 1) verify the accuracy of the calculated parameters by the analytical and the semi-analytical approaches against the time-domain simulation results of the detailed switching model of the converter, and 2) compare the performance of the conventional topology with the designed converter. The results are summarized in Table 3-II. The key parameters used in this comparative study are the switching losses, conduction losses, total losses, amplitude of the ac circulating current, and the number of needed SMs. The results are presented for two different cases, the conventional topology operating at point B and the designed converter operating at point A (see Figure 3-6).

In the augmented design method, the conduction loss is calculated in two ways, the analytical and the semi-analytical approaches. The analytical approach offers a very simple calculation of conduction loss using (3-19) and (3-20), whereas the semi-analytical approach provides a more precise estimation of conduction loss using (3-27). The switching loss is calculated by finding the switching frequency of switches from the gating signals G_{arm} generated by the

sorting algorithm. In the simulation studies, all the losses are calculated using the provided loss calculation model in MATLAB/Simulink without considering the thermal effect on the characteristics of switches [52]. The results in Table 3-II confirm the satisfactory accuracy of the proposed analytical and semi-analytical approaches.

As shown in Table 3-II, the switching loss is almost constant for both cases, whereas the designed converter has lower conduction loss as compared to the conventional topology. This reduction in conduction loss is due to a lower number of SMs and smaller amplitude of ac circulating current in the designed converter. Thanks to the augmented design method, the designed converter operates at the phase difference (201°) closer to 180° compared to the conventional topology (219°). As a result, the amplitude of ac circulating current in the designed converter is 27% less than the conventional topology. Moreover, having a smaller ac current in the arm, the voltage fluctuations of the SMs capacitors are reduced in the designed converter, as shown in Table 3-II. As can be seen, the reduction in the SM capacitor voltage ripple is not significant despite a drastic decrease in the ac circulating current. This is because, in the conventional topology, more SMs exist to share the absorbed energy. Finally, the designed converter operates more efficiently compared with the conventional topology. Although the reduction in total loss made by the augmented design might seem negligible, it should be noticed that the conventional topology of the dc/dc MMC is already one of the most efficient dc/dc converters, which is proposed up to date. Therefore, the improvements made in the total loss and the number of SMs are still superior.

3.4 Design Example 2: 300 MW DC/DC MMC

To demonstrate the full potential of the proposed augmented method, a design example of a large-scale dc/dc MMC with hundreds of SMs for a HVDC application is presented. In this section, the effect of the dc-link voltage ratio and arm inductance on the dc/dc MMC is investigated.

Table 3-III
Main Parameters of Analyzed Large-Scale DC/DC MMC

Common Parameter	**Symbol**	**Value**
Rated Power	S	300 MW
DC-Link2	V_{DC2}	200 kV
Arm Inductance	L	2.4 mH
Phase Inductance	L_0	0.26 H
SM Capacitance	C	20 mF
SM Nominal Voltage	V_{CN}	2 kV
Operating Frequency	f_S	360 Hz
Conventional Topology	**Symbol**	**Value**
Number of Upper Arm HBSMs	n_u	100
Number of Lower Arm HBSMs	n_d	100

3.4.1 Effect of DC-Link Voltage Ratio

The main parameters of the converter are depicted in Table 3-III. In this case study, the voltage of dc-link 1 varies in different case studies ($V_{DC1} = D.V_{DC2}$), and the arm inductance is fixed at 0.24 mH. Using the semi-analytical approach, the performance of the conventional topology, which has 100 HBSMs in each arm, is assessed in each feasible phase difference. The obtained results from the conventional topology are compared with the converters designed by the augmented method at each operating point.

In Figure 3-9, the total converter losses in per-unit (p.u.), calculated by the proposed semi-analytical approach, are shown for cases with different voltage ratios *D*. In all operating points, the converter designed by the augmented method have less total losses as compared to the conventional topology. Efficiency improvement in the designed converters becomes more significant when *D* approaches 1. Moreover, as *D* gets closer to 1, the number of operating points that the conventional topology could not operate in increases. On the contrary, all the operating points are available in the proposed approach. The total losses of the designed converters are extremely high in operating points around 180^o, making them impractical. Overall, the dc/dc MMC is more efficient when *D* approaches 1, and theoretically, the worst efficiency happens when *D*=0.5.

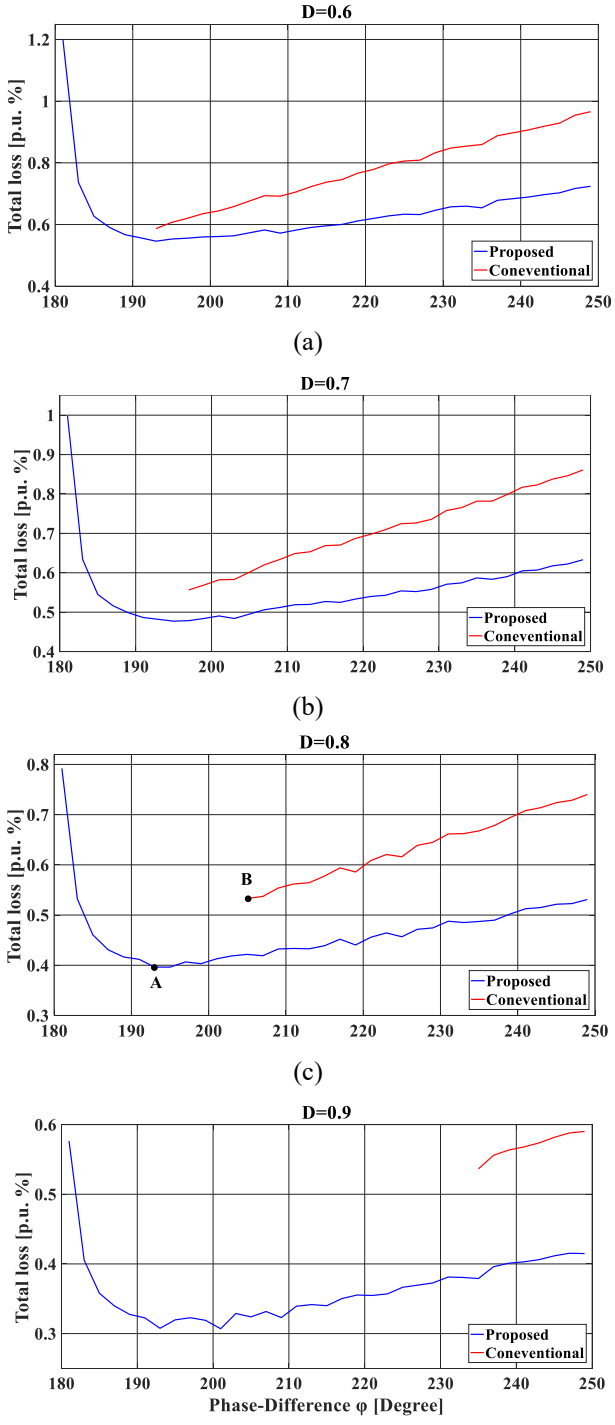


Figure 3-9 Total losses at each operation point for the conventional topology and the converters designed by the proposed augmented method, (a) DC-link voltage ratio D=0.6, (b) D= 0.7, (c) D=0.8, (d) D=0.9.

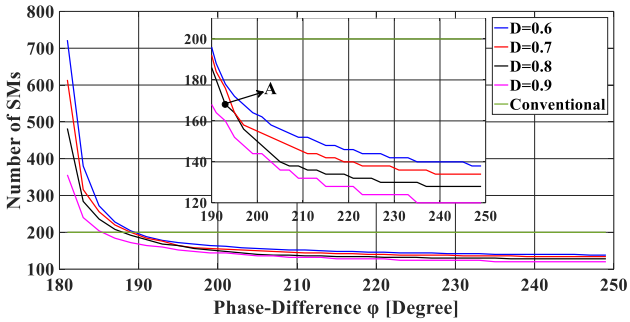


Figure 3-10 Number of SMs at each operation point for the conventional topology and the converter designed by the proposed augmented method.

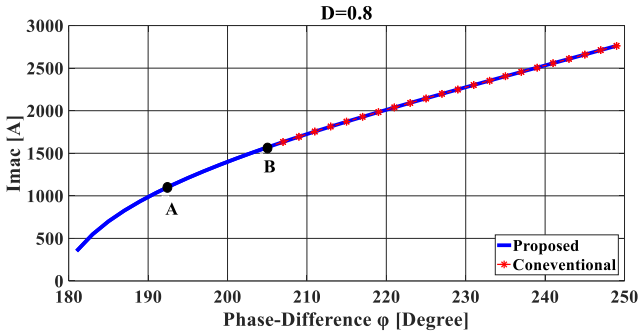


Figure 3-11 Amplitude of the ac circulating current when D=0.8.

In Figure 3-10, the number of SMs in each phase-leg of the designed converter is compared with the conventional topology. As the phase difference increases, the number of SMs decreases to the extent that it becomes smaller than the number of SMs in the conventional topology. Because the proposed design procedure has eliminated unnecessary SMs, the designed converters are more efficient than the conventional topology.

As shown, the number of SMs is extremely high in the vicinity of 180°; therefore, the designed converters operate impractically with high total losses. In general, the converters designed with greater D need fewer SMs in the same operating points, and they are more efficient.

To compare the current rating, the amplitude of the ac circulating current is shown in Figure 3-11. The dc component of the arm current depends on the dc-link voltages and transmitted power, and it has the same value in the conventional topology and the designed converters. Hence, the only difference in the arm current is the ac circulating current. As shown in Figure 3-10, when the phase difference approaches 180°, the amplitude of the circulating current reduces. However, due to the inherent limitation of the conventional topology, it is not possible to cover all the operating points losing the opportunity to reduce further the ac circulating

Table 3-IV
Comparison of Operating Points A and C (Design Example 2).

Operating points	Designed converter at point A	Conventional topology at point B
Total loss [p.u. %]	0.39	0.53
Number of SMs	168	200
Amplitude of ac current [A]	1126	1570

current. On the other hand, using the augmented design method, the converter can operate with phase differences close to 180°. Hence, the amplitude of the ac circulating current can be further reduced.

To present another design example, the case study of D=0.8 is considered. In the conventional topology, the lowest total losses and ac circulating current are yielded when φ=205°; point B in Figure 3-9 (c), 10, and 11. In the proposed design, the operation with φ =192° yields minimum total losses; point A in Figure 3-9(c), 10, and 11. In Table 3-IV, the total losses, number of SMs, and amplitude of the ac current are presented for the conventional topology operating at point A and the designed convert by augmented design operating at B. The proposed design yields a converter with minimum losses and a reduced number of SMs. By comparing Table 3-II and IV, it can be understood that the achieved improvements by the augmented design are more significant in large-scale MMCs.

3.4.2 Effect of Arm Inductance

To analyze the effect of the arm inductance on the design procedure, using the proposed semi-analytical approach the total losses, number of SMs, and amplitude of ac circulating current for three different values of arm inductance are estimated at each operating point. This analysis is carried out for phase differences between 183° and 250°. In this case study, the dc-link voltage ratio is fixed at 0.8. The other system parameters are depicted in Table 3-III.

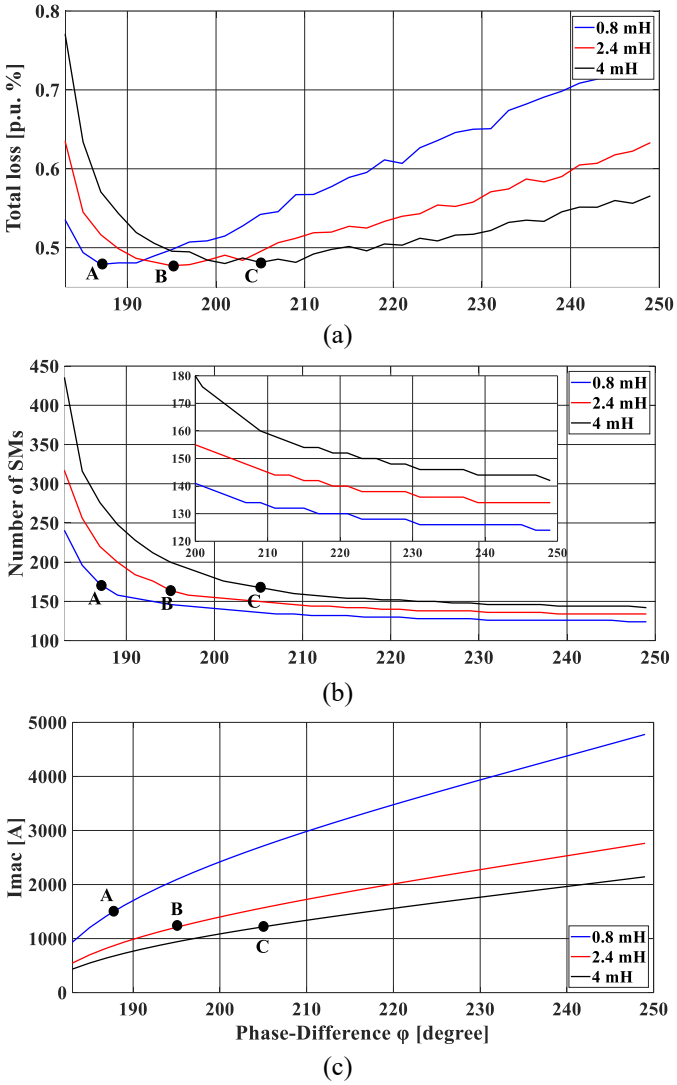


Figure 3-12 Effect analysis of the arm inductance on the converter performance, (a) Total loss in p.u., (b) required number of SMs at each phase difference and (c) Amplitude of ac circulating current.

In Figure 3-12(a), the total loss of the designed converters by the augmented method at each operating point is illustrated for three values of the arm inductance. As can be seen, the increase of the arm inductance pushes the point of minimum total loss towards 270°. After the minimum total loss point (A, B, and C), the rate of change of the total loss with respect to the phase difference is smaller in converters with a larger arm inductance. This is because, in these converters, the rate of increase of the ac circulating current with respect to the phase difference is slower, as shown in Figure 3-12(c). At each phase difference, the required number of SMs in the converter with a larger arm inductance is higher. A larger arm inductance necessitates a larger amplitude of the arm ac voltage to induce the ac circulating current (see Figure 3-12(b)).

As illustrated in Figure 3-12(a) and (b), points A, B, and C (points of minimum loss) have almost equal total loss and number of SMs. However, the amplitude of the circulating current is slightly higher in converters with a smaller arm inductance. Therefore, if the steady-state operation of the converter is considered for selecting the size of the arm inductance, there is no significant difference between optimum operating points in converters with different arm inductances. Nevertheless, it should be noticed that a small arm inductance (in this case, 0.8 mH) makes the control of the converter harder. Because the rate of change of the ac circulating current with respect to the phase difference is high, fast controllers are needed to stabilize the converter. On the other hand, a large arm inductance (4 mH) increases the converter cost without adding useful features. In the end, an arm inductance of 2.4 mH is selected in this study.

3.5 Summary

This chapter presented an augmented design method for the dc/dc MMC to improve the converter efficiency and reduce the number of SMs. The proposed design determines the number of SMs and their types (e.g., half- or full-bridge) in each arm and the phase difference between arms ac voltages that minimize the total converter losses. Computationally-efficient analytical and semi-analytical methods were developed to estimate the conduction and switching losses. As compared to the detailed simulation results of the switching converter model, the analytical and semi-analytical methods yielded a fast and accurate calculation of the converter losses. As compared to the conventional topology of the dc/dc MMC, the proposed design method yielded a converter with lower total losses and number of SMs and extended the range of possible operating points (phase differences between arms ac voltages) helping the converter to operate with a lower current rating and conduction losses.

Chapter 4 Operation Limits of the Hybrid DC/DC MMC

In this chapter, first, the topology and mathematical equations of the hybrid dc/dc MMC are presented. Then, the proposed analytical approach to determine whether the capacitors voltages of the dc/dc MMC can be maintained balanced in a specific operating point is elaborated. The results from the proposed analytical method are compared with the results from the simulation studies to verify the accuracy of the analytical study. In the end, the impact of system parameters on the operation range of the hybrid dc/dc MMC is investigated.

4.1 Hybrid DC/DC MMC

4.1.1 Structure

The configuration of a typical hybrid dc/dc MMC with two phase-legs is illustrated in Figure 4-1. The overall structure is similar to the conventional dc/dc MMC. Each arm is composed of

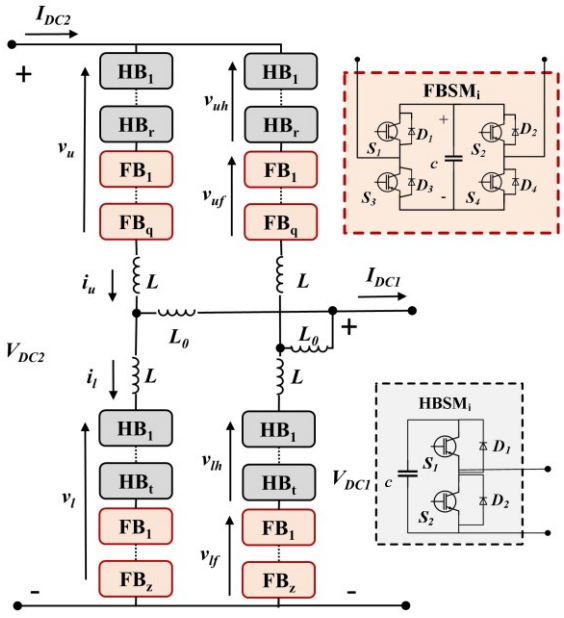


Figure 4-1 Structure of the hybrid dc/dc MMC.

several HBSMs and FBSMs. The number of HBSMs and FBSMs in the upper and the lower arms could be different, which can be found based on the needed arm ac voltage and dc-links voltages [23]. The voltages generated by the upper and the lower arms SMs are denoted by v_u and v_l. The equivalent voltage of HBSMs and FBSMs in the upper and the lower arms are v_{uh}, v_{uf} and v_{lh}, v_{lf}, respectively. The upper and lower arms currents are also represented by i_u and i_l. In this study, the operation of one phase-leg is investigated; therefore, subscripts related to phase-legs are avoided.

4.1.2 Mathematical Modeling

In this chapter, the capacitor voltage balancing strategy proposed in [24] is used, which adds ac voltages with equal amplitude and specified phase difference to arms reference voltages to induce an ac circulating current and neutralize the dc power flow. The reference voltages of upper v_u and lower v_l arms are expressed in (4-1) and (4-2).

$$v_u(t) = (V_{DC2} - V_{DC1}) + \hat{v}_{u,AC}\cos(\omega t + \varphi) \tag{4-1}$$

$$v_l(t) = V_{DC1} + \hat{v}_{l,AC}\cos(\omega t) \tag{4-2}$$

$$\hat{v}_{u,AC} = \hat{v}_{l,AC} = \hat{v}_{AC} \tag{4-3}$$

where $\hat{v}_{u,AC}$ and $\hat{v}_{l,AC}$ denote the amplitude of upper and lower arms ac voltages, and φ is the phase difference between them. The angular frequency of the arms ac voltages is ω. This frequency is a design parameter that can be selected arbitrarily. High frequencies decrease the size of arm and phase inductors, while it increases the switching losses of the converter [25]. Assuming that the converter transmits the rated power P from the dc-link 2 to dc-link 1, each of the upper and lower arms processes P_{DC} amount of power, which can be calculated as follows:

$$P_{DC} = \frac{1 - D}{M}.P, D = \frac{V_{DC1}}{V_{DC2}} \tag{4-4}$$

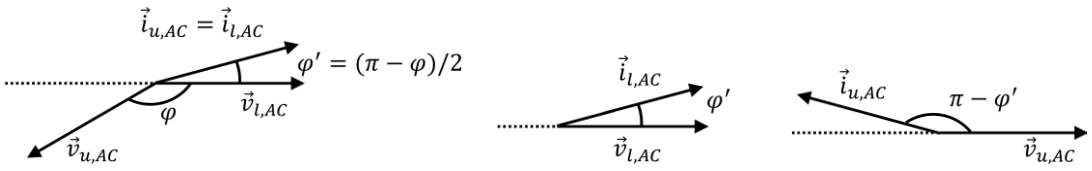


Figure 4-2 Phasor diagram of (a) upper and lower arms when the lower arm voltage is the reference (b) lower arm when the lower arm voltage is the reference (c) upper arm when the upper arm voltage is the reference.

where *D* indicates the dc-links voltage ratio, and *m* denotes the number of phase-legs. As shown in earlier studies [7], to stabilize the capacitors voltages of each arm, the upper and lower arms need to exchange an active ac power P_{AC}, which can be calculated as

$$P_{AC} = -P_{DC} \tag{4-5}$$

$$P_{AC} = \frac{1}{2X_e}\hat{v}_{AC}^2.\sin(\varphi) \tag{4-6}$$

$$X_e = \frac{(X_L^2 + 2X_L X_{L0})}{X_{L0}} \tag{4-7}$$

where X_e is the equivalent reactance.

To enable the exchange of dc power between dc-links and the ac active power between the upper and lower arms, the arms currents need dc and ac components as expressed in (4-8) and (4-9).

$$i_u(t) = I_{u,DC} + i_{u,AC} \tag{4-8}$$

$$i_l(t) = I_{l,DC} + i_{l,AC} \tag{4-9}$$

where $I_{u,DC}$ and $I_{l,DC}$ are the dc components of the upper and lower arms currents, and $i_{u,AC}$ and $i_{l,AC}$ denote the ac components. The ac and dc components of arms currents can be calculated by (4-10), (4-11), (4-12), and (4-13). Equations (4-12) and (4-13) are obtained using the steady-state equations and presented in the phasor-domain [25],

$$I_{u,DC} = \frac{P}{M \cdot V_{DC2}} \tag{4-10}$$

$$I_{l,DC} = \frac{P}{M}\left(-\frac{1}{V_{DC1}} + \frac{1}{V_{DC2}}\right) = \frac{P}{M.V_{DC2}}.\frac{-1+D}{D} \tag{4-11}$$

$$\vec{i}_{u,AC} = -\frac{(X_{L0}+X_L)\vec{v}_{u,AC} + (X_{L0})\vec{v}_{l,AC}}{j.(X_L^2 + 2\cdot X_L \cdot X_{L0})} \tag{4-12}$$

$$\vec{i}_{l,AC} = -\frac{(X_{L0}+X_L)\vec{v}_{l,AC} + (X_{L0})\vec{v}_{u,AC}}{j(X_L^2 + 2\cdot X_L \cdot X_{L0)}} \tag{4-13}$$

where $\vec{v}_{u,AC}$ and $\vec{v}_{l,AC}$ are the upper and lower arms ac voltages in the phasor-domain which can be found from (4-1) and (4-2). Assuming that X_L can be ignored relative to X_{L0}, (4-12) and (4-13) are approximated by

$$\vec{i}_{l,AC} = \vec{i}_{u,AC} = -\frac{\vec{v}_{l,AC} + \vec{v}_{u,AC}}{j2X_L} \tag{4-14}$$

By substituting the arms ac voltages in (4-14) the upper and lower arms ac circulating currents in the time-domain can be calculated

$$i_{u,AC}(t) = i_{l,AC}(t) = \hat{i}_{AC} \cdot \cos(\omega t + \frac{\varphi}{2} - \frac{\pi}{2}) \tag{4-15}$$

$$\hat{i}_{AC} = \frac{\hat{v}_{AC}}{2X_L}\sqrt{2(1+\cos(\varphi))} \tag{4-16}$$

To clearly show the angles of the arms ac currents and voltages, a phasor diagram is presented in Figure 4-2.

4.1.3 Determining the Number of HBSMs and FBSMs

The ideas of improving the power transfer capability and attenuating the ac circulating current using FBSMs and HBSMs are first proposed in [23]. The hybrid topology can neutralize the dc power flow at any condition (any phase difference and any transmitted power) with the cost of using FBSMs and adding extra HBSMs. Knowing the dc-links voltages and the transmitted power, the arm ac voltage with respect to the phase difference can be derived using (4-6).

Similarly, the amplitude of ac circulating current with respect to the phase difference is obtained using (4-6) and (4-16) as

$$\hat{i}_{AC} = 2\sqrt{\frac{(1-D)P}{M.X_e.\tan\left(\frac{\varphi}{2}\right)}} \tag{4-17}$$

Assuming that the suitable value for the ac circulating current is $\hat{i}_{AC,n}$, the phase difference that the converter must operate at is found using (4-17). Then, the arm ac voltage is calculated from (4-6). Having the arm ac voltage, the maximum and minimum voltages that each arm must generate, $v_{arm,min}$ and $v_{arm,max}$, can be found. The FBSMs are only used when one arm needs to generate a negative voltage. Therefore, the number of FBSMs $n_{arm,f}$ is obtained based on the minimum voltage of the arm as follow

$$v_{arm,min} = V_{arm,DC} - \hat{v}_{AC} \tag{4-18}$$

$$n_{arm,f} = ceil\left\lceil -\frac{v_{arm,min}}{V_{CN}} \right\rceil \tag{4-19}$$

where V_{CN} is the nominal voltage of SM. The total number of SMs n_{arm} depends on the arm maximum voltage, and it is calculated in (4-21). Having the total number of SMs and number of FBSMs, the number of HBSMs $n_{arm,h}$ is obtained in (4-22).

$$v_{arm,max} = V_{arm,DC} + \hat{v}_{AC} \tag{4-20}$$

$$n_{arm} = ceil\left\lceil \frac{v_{arm,max}}{V_{CN}} \right\rceil \tag{4-21}$$

$$n_{arm,h} = n_{arm} - n_{arm,f} \tag{4-22}$$

Table 4-I
Exchanged Energy by the Arm and Associated Areas

Arm current	$i_{arm} > 0$	$i_{arm} \leq 0$	$i_{arm} > 0$	$i_{arm} \leq 0$
Arm voltage	$v_{arm} > 0$	$v_{arm} > 0$	$v_{arm} \leq 0$	$v_{arm} \leq 0$
Area	A_1	A_3	A_2	A_4
Exchanged Energy by arm	$E_{1arm} > 0$	$E_{3arm} < 0$	$E_{2arm} < 0$	$E_{4arm} > 0$

4.2 Capacitors Voltages Balance Analysis of the Hybrid DC/DC MMC

The phase reference of both arms currents and voltages in (4-1), (4-2), and (4-14) is the lower arm ac voltage, as shown in Figure 4-2(a). To simplify the calculations, the phase reference of the upper arm (current and voltage) is changed to $-\varphi$, and $\frac{\varphi}{2} - \frac{\pi}{2}$ is defined as φ' (see Figure 4-2(b) and (c)). Therefore, the arms currents and the arms reference voltages can be rewritten as

$$i_u(t) = I_{u,DC} - \hat{i}_{AC} \cdot \cos(\omega t - \varphi') \tag{4-23}$$

$$v_u(t) = (V_{DC2} - V_{DC1}) + \hat{v}_{AC} \,.\cos(\omega t) \tag{4-24}$$

$$i_l(t) = -I_{l,DC} + \hat{i}_{AC} \cdot \cos(\omega t + \varphi') \tag{4-25}$$

$$v_l(t) = V_{DC1} + \hat{v}_{AC} \,.\cos(\omega t) \tag{4-26}$$

In general, the arms currents and voltages can have positive and negative values in one period. Therefore, one period can be segmented as presented in Table 4-I, in which the subscript *arm* indicates the upper and lower arms ($arm \in \{u, l\}$). Theoretically, by increasing the arm ac voltage, the amplitude of ac circulating current can be reduced to the extent that it becomes less than the dc component of arm current. Hence the capacitors voltages balance of hybrid topology can be studied in two situations.

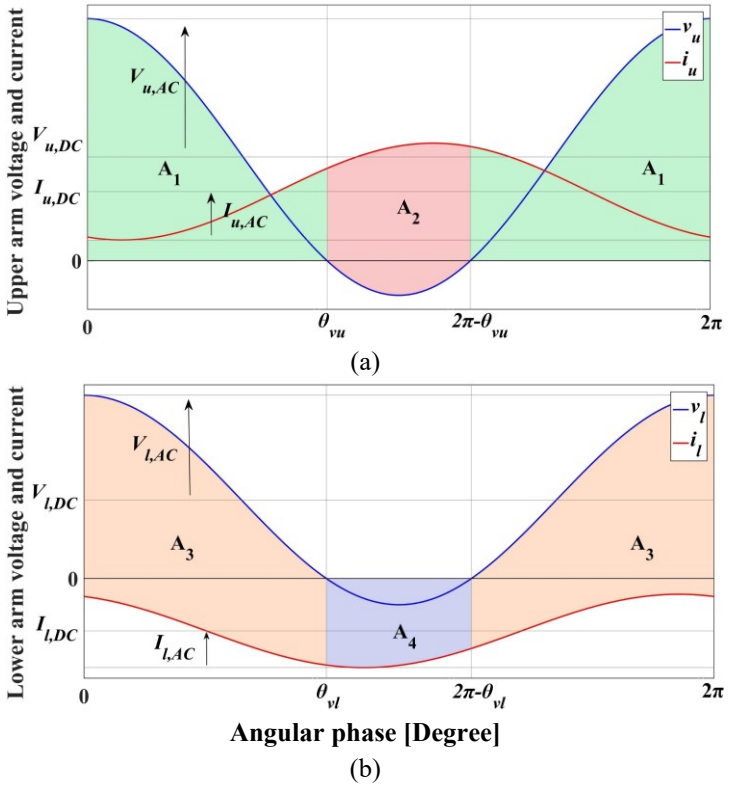


Figure 4-3 Voltage and current of (a) Upper arm and (b) Lower arm, when the dc component of arm current is higher than the ac component.

4.2.1 DC Component of Arm Current Higher Than the AC Component

The currents and voltages of both arms are illustrated in Figure 4-4. These waveforms are obtained using (4-1), (4-2), and (4-15). As shown, the upper arm current is always positive, and the lower arm current always has a negative value. In the upper arm, when the arm voltage is positive (A_1), the SMs (HBSMs and FBSMs) absorb E_{1u}; and when the arm voltage is negative (A_2), only the FBSMs inject E_{2u} to the system. Similarly, in the lower arm, when the arm voltage is positive (A_3), the arm injects E_{3l}, and when the arm voltage is negative (A_4), the FBSMs absorb E_{4l}. Thanks to the power balance controller, summations of E_{1u} and E_{2u} in the upper arm, and E_{3l} and E_{4l} in the lower arm are zero. However, the fact that E_{1u} and E_{2u} in the upper arm, and E_{3l} and E_{4l} in the lower arm are not exchanged by the same type of SMs unbalances the capacitors voltages. In other words, in the upper arm, the HBSMs only absorb energy, and in the lower arm, they only inject energy. Therefore, the capacitors voltages cannot be maintained balanced despite using the power balance controller and sorting algorithm. In

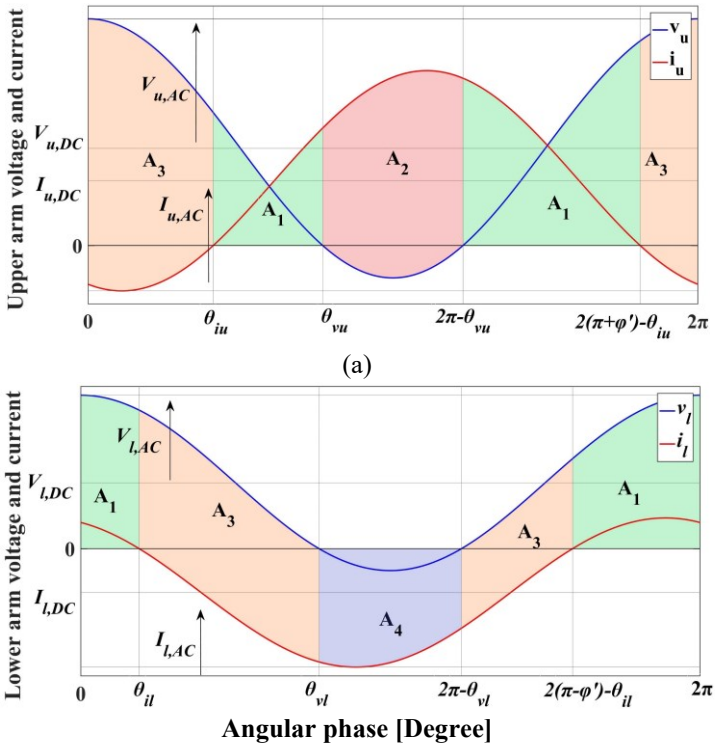


Figure 4-4 Voltage and current of (a) Upper arm and (b) Lower arm, when the ac component of arm current is higher than the dc component.

this chapter, the sorting algorithm proposed in [53, 54] is used. Based on the presented explanations, an obvious condition of stable operation is that the ac component of arm current must be larger than the dc component.

4.2.2 DC Component of Arm Current Smaller Than the AC Component

In this case, as shown in Figure 4-3, the arms currents can have positive and negative values in one period. The voltages of the upper and lower arms cross the horizontal axis at $\theta_{vu}$and θ_{vl}, and similarly, the arms currents intersect the horizontal axis at θ_{iu} and θ_{il}. Using (4-1), (4-2) and (4-15), these angles are calculated.

$$\theta_{vu} = \cos^{-1}\left(\frac{-V_{DC2} + V_{DC1}}{\hat{v}_{AC}}\right) \tag{4-27}$$

$$\theta_{vl} = \cos^{-1}\left(\frac{-V_{DC1}}{\hat{v}_{AC}}\right) \tag{4-28}$$

$$\theta_{iu} = \cos^{-1}\left(\frac{I_{u,DC}}{\hat{\imath}_{AC}}\right) + \varphi' \tag{4-29}$$

$$\theta_{il} = \cos^{-1}\left(\frac{I_{d,DC}}{\hat{\imath}_{AC}}\right) - \varphi' \tag{4-30}$$

From the above equations, it can be understood that $\theta_{iu}, \theta_{il} \epsilon \left(0, \frac{\pi}{2}\right)$ and $\theta_{vu}, \theta_{vl} \epsilon \left(\frac{\pi}{2}, \pi\right)$. In the upper arm, when the arm voltage is negative (A_2), the FBSMs inject E_{2uf}. When the arm voltage is positive, they absorb energy in A_1 and inject energy in A_3. To make the average absorbed energy by the FBSMs zero in one period, the sorting algorithm activates the FBSMs in a way that they absorb a total energy of E_{2uf} in A_1 and A_3. If the maximum energy that can be absorbed by the FBSMs in A_1 and A_3 becomes less than E_{2uf}, despite using the sorting algorithm, the capacitors voltages of the FBSMs cannot be maintained balanced. The FBSMs absorb the maximum total energy in A_1 and A_3, when they absorb maximum energy in A_1 (E_{1ufmax}) and lose minimum energy in A_3 (E_{3ufmin}). To keep the capacitors voltages of the upper arm balanced, the maximum total absorbed energy by the FBSMs, when the arm voltage is positive (A_3 and A_1), must be larger than the energy that is lost when the arm voltage is negative (A_2). If this condition is satisfied, the sorting algorithm would be able to regulate the total absorbed energy by the FBSMs in A1 and A_3, to neutralize the injected energy in A_2. By extending this condition to the lower arm, the following inequalities must hold

$$-E_{2uf} < E_{1ufmax} + E_{3ufmin} \tag{4-31}$$

$$E_{4lf} < -E_{3lfmax} - E_{1lfmin} \tag{4-32}$$

where E_{2uf} and E_{4lf} are the energies that the FBSMs in the upper and lower arms exchange with the system when the arm voltage is negative. E_{1ufmax} (E_{3lfmax}) is the maximum possible energy that the FBSMs in the upper (lower) arm can absorb (inject) in A_1 (A_3). E_{3ufmin} (E_{1lfmin}) indicates the minimum energy that the FBSMs in the upper (lower) arm can inject (absorb) in A_3 (A_1). For the sake of simplicity, E_{us} and E_{ls} are defined as

$$E_{us} = E_{1ufmax} + E_{3ufmin} + E_{2uf} \tag{4-33}$$

$$E_{ls} = -E_{3lfmax} - E_{1lfmin} - E_{4lf} \tag{4-34}$$

As long as E_{us} and E_{ls} are positive, the capacitors voltages can be kept balanced. When one of them becomes negative, the capacitors voltages of the associated arm cannot be balanced. In the following, the defined energies in (4-33) and (4-34) are calculated analytically. Since the conduction and switching losses in the dc/dc MMC are relatively small, they are ignored in this study. Moreover, it is assumed that many SMs exist in the arm so that the generated waveform is perfectly sinusoidal.

4.2.2.1 Calculation of E_{2uf} and E_{4lf}

E_{2uf} and E_{4lf} can be easily calculated by integrating the multiplication of the arm current and FBSMs equivalent voltage during the period in which the arm voltage is negative ([θ_{vu}, $2\pi - \theta_{vu}$] for the upper arm, and [θ_{vl}, $2\pi - \theta_{vl}$] for the lower arm). In this period, the equivalent voltage of FBSMs is equal to the arm voltage. E_{2uf} and E_{4lf} are calculated as

$$E_{2uf} = \int_{\theta_{vu}}^{2\pi-\theta_{vu}} \frac{1}{\omega}.i_u.v_u\, d\theta \tag{4-35}$$

$$E_{4lf} = \int_{\theta_{vl}}^{2\pi-\theta_{vl}} \frac{1}{\omega}.i_l.v_l\, d\theta \tag{4-36}$$

The calculated formula for E_{2uf} is provided in Appendix.

4.2.2.2 Calculation of E_{1ufmax} and E_{3lfmax}

The FBSMs will exchange the maximum energy in an area when the sorting algorithm prioritizes them in activation over the HBSMs. For further explanation, assume that there exists n_{armf} ($arm \in \{u, l\}$) number of FBSMs in one arm and the maximum voltage that they can generate is $V_{armfm} = V_{CN}.n_{armf}$. When the arm voltage is smaller than V_{armfm}, the number of required on-state SMs is less than n_{armf}. To prioritize the FBSMs in activation, all the

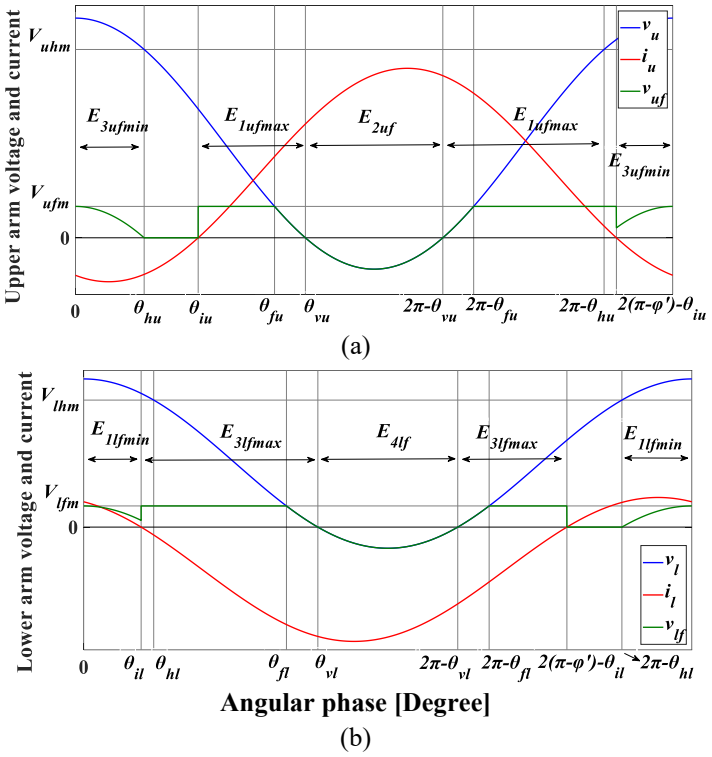


Figure 4-5 Voltage, current and FBSMs equivalent voltage of (a) Upper arm and (b) Lower arm.

required on-state SMs should be selected among FBSMs. When the arm voltage is larger than V_{armfm}, the number of needed on-state SMs is larger than n_{armf}. Therefore, all the FBSMs should be activated for the whole period, and the rest of the on-state SMs can be activated from the HBSMs. These two conditions and the equivalent voltage of FBSMs are demonstrated in Figure 4-5. The equivalent voltage of FBSMs v_{armf} can be expressed as

$$v_{armf} = \begin{cases} v_{arm} & v_{arm} < V_{armfm} \\ V_{armfm} & v_{arm} > V_{armfm} \end{cases} \tag{4-37}$$

Using (4-37), the equivalent voltage of upper arm FBSMs in A_1 and lower arm FBSMs in A_3 can be found, when they exchange the maximum energy, as shown in Figure 4-5. Having the equivalent voltage of FBSMs, the maximum exchanged energy can be calculated by the following equations:

$$E_{1ufmax} = \frac{1}{\omega}\left(\int_{\theta_{iu}}^{\theta_{fu}} i_u . V_{ufm}\, d\theta + \int_{\theta_{fu}}^{\theta_{vu}} i_u . v_u\, d\theta + \int_{2\pi-\theta_{vu}}^{2\pi-\theta_{fu}} i_u . v_u\, d\theta + \int_{2\pi-\theta_{fu}}^{2(\pi+\varphi')-\theta_{iu}} i_u . V_{ufm}\, d\theta\right) \quad (4\text{-}38)$$

$$E_{3lfmax} = \frac{1}{\omega}\left(\int_{\theta_{il}}^{\theta_{fl}} i_l . V_{lfm}\, d\theta + \int_{\theta_{fl}}^{\theta_{vl}} i_l . v_l\, d\theta + \int_{2\pi-\theta_{vl}}^{2\pi-\theta_{fl}} i_u . v_u\, d\theta + \int_{2\pi-\theta_{fl}}^{2(\pi-\varphi')-\theta_{il}} i_l . V_{lfm}\, d\theta\right) \quad (4\text{-}39)$$

where θ_{fu} and θ_{fl} are the angles that the upper and lower arms voltages become equal to V_{ufm} and V_{lfm}. For instance, the calculated formula for E_{1ufmax} is provided in the Appendix.

4.2.2.3 Calculation of E_{3ufmin} and E_{1lfmin}

For the FBSMs to exchange the minimum energy with the system in an area, they should be deprioritized in activation over the HBSMs. Let us assume that there exists n_{armh} number of HBSMs in one arm which can generate the maximum voltage of $V_{armhm} = V_{CN}.n_{armh}$. When the arm voltage is less than V_{armhm}, the number of required on-state SMs is smaller than n_{armh}. To minimize the exchanged energy by FBSMs, the on-state SMs should be selected among HBSMs so that FBSMs remain in the off-state. When the arm voltage is larger than V_{armhm}, the number of required on-state SMs is higher than n_{armh}. In this situation, the FBSMs exchange the minimum energy with the system if all the HBSMs are activated. Only the remainder of needed on-state SMs is activated from the FBSMs. In this case, the equivalent voltage of FBSMs v_{armf} is

$$v_{armf} = \begin{cases} 0 & v_{arm} < V_{armhm} \\ v_{arm} - V_{armhm} & v_{arm} > V_{armhm} \end{cases} \quad (4\text{-}40)$$

Using (4-40), the equivalent voltage of upper arm FBSMs in A_3 and lower arm FBSMs in A_1 can be calculated in the case of exchanging the minimum energy, as shown in Figure 4-5. By

having the equivalent voltage of FBSMs, the minimum exchanged energy by the FBSMs of upper and lower arms in A_3 and A_1 are be obtained by

$$E_{3ufmin} = \frac{1}{\omega}\left(\int_0^{b_{1u}} i_u.(v_u - V_{uhm})\,d\theta + \int_{b_{2u}}^{2\pi} i_u.(v_u - V_{uhm})\,d\theta\right) \tag{4-41}$$

$$E_{1lfmin} = \frac{1}{\omega}\left(\int_0^{b_{1l}} i_l.(v_l - V_{lhm})\,d\theta + \int_{b_{2l}}^{2\pi} i_l.(v_l - V_{lhm})\,d\theta\right) \tag{4-42}$$

In (4-41) and (4-42), some boundaries can change in different situations and can be found by

$$b_{1arm} = \min\{\theta_{harm}, \theta_{iarm}\} \tag{4-43}$$

$$b_{2arm} = \max\{2\pi - \theta_{harm}, 2(\pi \pm \varphi') - \theta_{iarm}\} \tag{4-44}$$

where θ_{hu} and θ_{hl} are the angles that the upper and lower arms voltages become equal to V_{uhm} and V_{lhm}. For the lower arm $\pm\varphi'$ should be $-\varphi'$, and for the upper, it should be $+\varphi'$. For instance, the calculated formula for E_{3ufmin} is provided in the Appendix.

4.2.3 Finding the Minimum Feasible Phase Difference

To find the minimum feasible phase difference in the hybrid dc/dc MMC, first, the vulnerable arm in which the capacitors voltages unbalance is more likely to happen should be found. The vulnerable arm can be found based on the value of D. If $D > 0.5$, the upper arm is the vulnerable arm, and if $D < 0.5$, the lower arm is the most endangered arm. To explain it, in the case of $D > 0.5$, the dc component of the upper arm voltage is smaller than the lower arm (see (4-1) and (4-2)). Assuming an equal ac voltage for both arms, the minimum voltage of the upper arm is smaller than the minimum voltage of the lower arm (see (4-18)). Therefore, in general, the upper arm must generate a larger amplitude of the negative voltage. It requires the upper arm to have a higher number of FBSMs. Because the capacitors voltages unbalance is results from excessive usage of FBSMs, in this case, the upper arm is more subjected to the capacitors voltages unbalance. Similar observations are held when $D < 0.5$. To be efficient, the calculation would be executed only for the vulnerable arm.

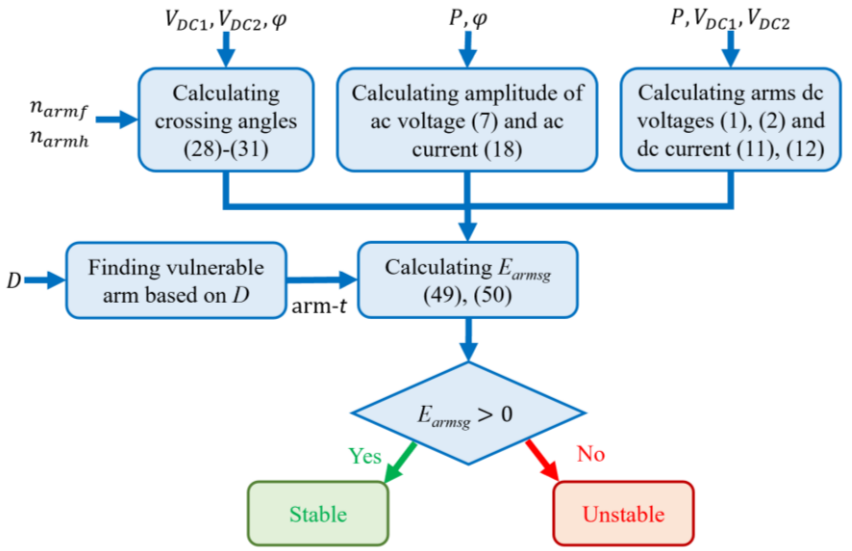


Figure 4-6 The overall procedure of finding stable operating points.

In Figure 4-6, the overall procedure of finding the operation limit is illustrated. As shown, using the converter parameters (e.g., dc-links voltages, number of HBSMs and FBSMs, operating power) and derived equations, the crossing angles and the ac and dc components of arms currents and voltages are calculated. The corresponding formula for each step is exhibited in Figure 4-6. Then, based on D, the vulnerable arm is determined. Accepting a ±5% error in the calculation of the defined energy due to the switching actions, E_{us} and E_{ls} are redefined in (4-45) and (4-46) to prevent any miscalculation.

$$E_{usg} = 0.95 * E_{1ufmax} + 1.05 * (E_{3ufmin} + E_{2uf}) \tag{4-45}$$

$$E_{lsg} = -0.95 * E_{3lfmax} - 1.05 * (E_{1lfmin} + E_{4lf}) \tag{4-46}$$

Afterward, E_{armsg} is calculated for the vulnerable arm- t ($t \in \{u, l\}$). This could be the upper or the lower arm depending on D. If E_{armsg} is a positive value, the converter can operate with balanced capacitors voltages. Otherwise, the capacitors voltages in the vulnerable arm cannot be maintained balanced. In this chapter, the term "stable" refers to the situation where the capacitors voltages of the converter can be balanced. The term "unstable" is used when the capacitors voltages of the vulnerable arm cannot be kept balanced. By calculating E_{armsg} for the whole range of phase differences, the minimum phase difference at which capacitors voltages can be balanced is determined.

Table 4-II
Main Parameters of the Simulated Converter

Parameter	**Symbol**	**Value**
Rated Power	S	20 MW
DC-Link1	V_{DC1}	14 kV
DC-Link2	V_{DC2}	20 kV
Arm Inductance	L	0.7 mH (0.09 p.u.)
Phase Inductance	L_0	0.26 H (29.4 p.u.)
SM Capacitance	C	1 mF
SM Nominal Voltage	V_{CN}	2 kV
Operating Frequency	f_S	360 Hz
Hybrid Converter at C and D	**Symbol**	**Value**
Number of Upper Arm HBSMs	n_{uh}	8
Number of Upper Arm FBSMs	n_{uf}	2
Number of Lower Arm SMs	n_{lh}	12
Conventional Topology	**Symbol**	**Value**
Number of Upper Arm HBSMs	n_{uh}	10
Number of Lower Arm SMs	n_{dh}	10

4.3 Verification of the Proposed Method

4.3.1 Operation Range of Hybrid DC/DC MMC

To find the operation range of hybrid dc/dc MMC, the capacitors voltages balance is analyzed using the proposed approach. The main parameters of the converter are given in Table 4-II. In Figure 4-7(a), E_{usg}, the number of HBSMs and FBSMs and, dc and ac components of upper arm current are shown for a wide range of phase differences [180°, 250°]. The phase difference is used as a representation of different operating points where the number of HBSMs and FBSMs, and the amplitude of ac circulating current, are different. Figure 4-7(a), (b), and (c) are segmented into three areas, conventional, hybrid, and unstable. The conventional area indicates the range of operating points in which the conventional topology of the dc/dc MMC is capable of operating. The hybrid region shows the range of phase difference, which is only

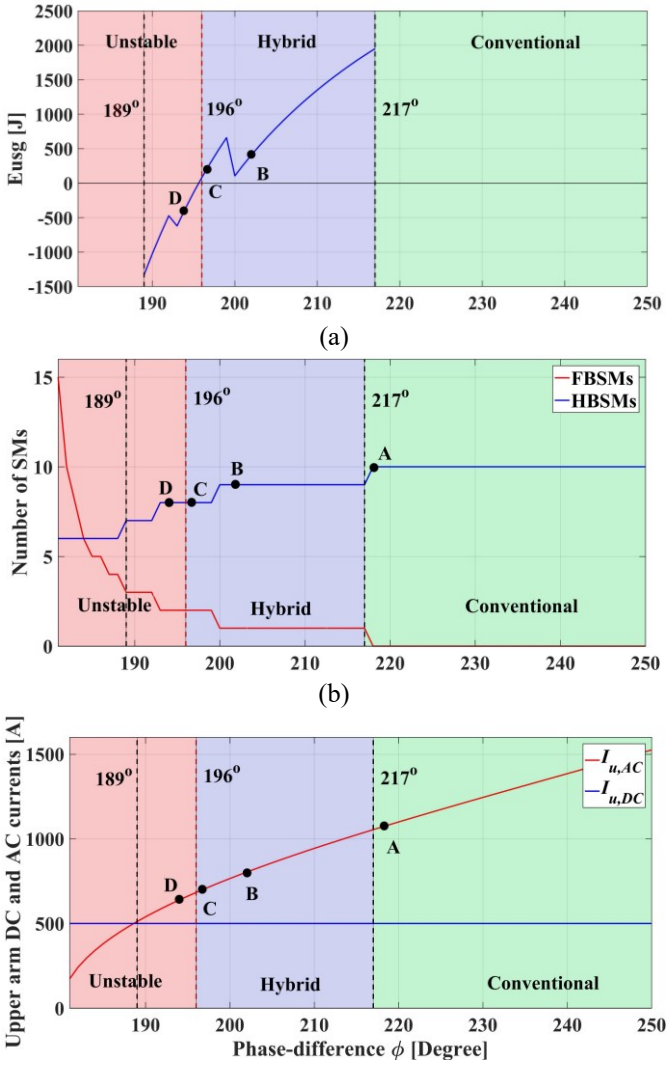


Figure 4-7 (a) E_{usg}, (b) Number of HBSMs and FBSMs and (c) Upper arm dc and ac currents.

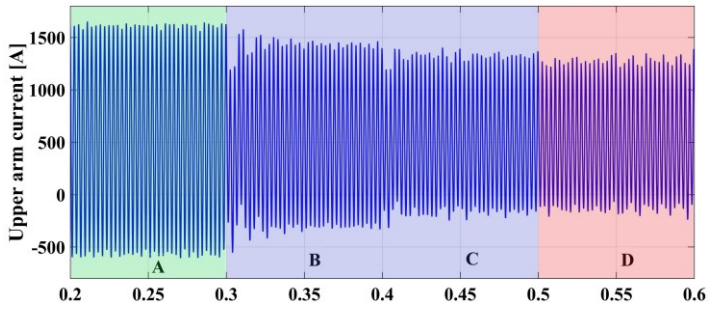
achievable by using the hybrid topology. Finally, the unstable part is the range of operating points in which the capacitors voltages of the upper arm cannot be maintained balanced.

When φ is between 217° and 250°, the needed arm ac voltage can be generated by the conventional topology of the dc/dc MMC; hence, this structure is used in this range of operating points. Fortunately, the capacitors voltages of the conventional topology are stable in the whole range of phase differences. However, it has higher ac circulating current as compared to the hybrid topology (see Figure 4-7(c)).

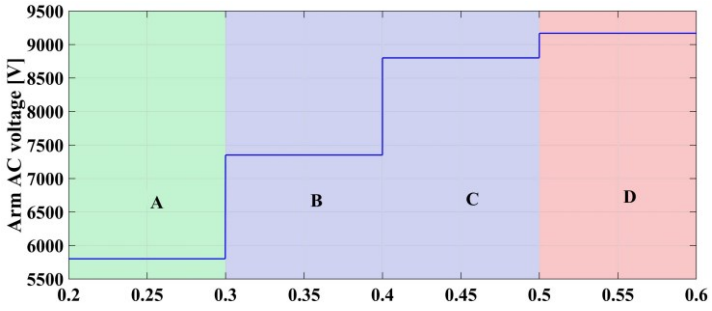
When the phase difference is between 180° and 217°, the needed arm ac voltage cannot be generated by the conventional topology. As a result, the converter needs FBSMs beside HBSMs to operate (hybrid area). In this operation range, at each phase difference, the number of HBSMs and FBSMs is calculated based on (4-19) and (4-22). As shown in Figure 4-7(c), from φ =180° to 189°, the ac circulating current is less than the dc component; therefore, the capacitors voltages of the converter are unstable. In Figure 4-7(a), E_{usg} is calculated for each phase difference between 189° and 217° (phase differences at which the converter may be unstable because of using FBSMs). From 189° to 196°, E_{usg} has a negative value, which indicates that the capacitors voltages of the upper arm could not be balanced. From 196° to 217°, E_{usg} is positive, which guarantees the stable operation of the hybrid topology. Eventually, based on the obtained results, the minimum feasible phase difference is 196° (point C). One important result of this study is that although the selected number of HBSMs and FBSMs at point C can also neutralize the dc power flow at point D, the capacitors voltages cannot be balanced at this point. Therefore, it is compulsory to ensure that the arm ac voltage is limited by the control actions to avoid operation at point D. This contradicts the idea that operation with maximum feasible arm ac voltage has the best performance [23, 24].

4.3.2 Simulation Results

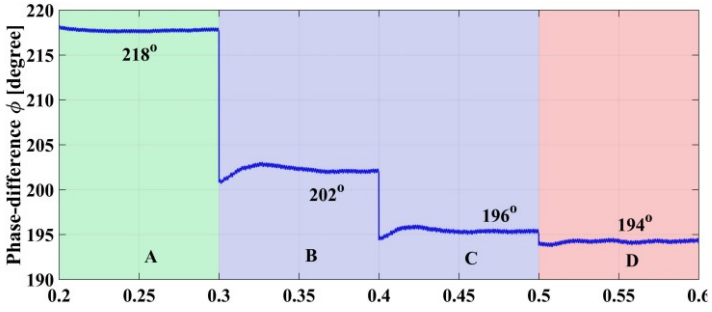
The hybrid dc/dc MMC detailed in Table 4-II is simulated in the MATLAB\Simulink environment. The number of HBSMs and FBSMs in the simulated converter is selected from the operating points C and D (see Figure 4-7). In the conducted simulation study, the hybrid converter operates at points A, B, C, and D (see Figure 4-7). The operating point A has the minimum phase difference in the conventional topology area. Points B and C exist in the hybrid topology range; the latter one is the minimum stable phase difference obtained from the capacitors voltages balance analysis. The operating point D is in the unstable area.


Upper arm current [A]
1500
1000
500
0
-500
A
B
C
D
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6

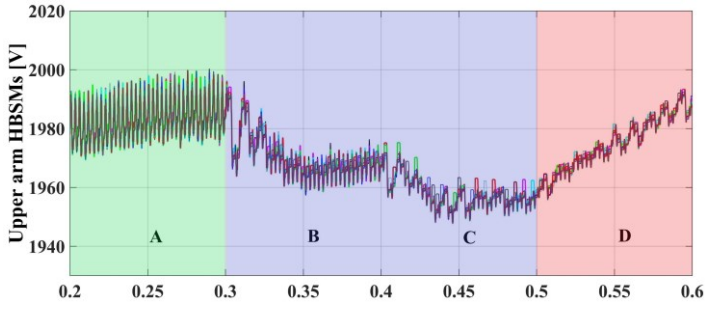
(a)


Arm AC voltage [V]
9500
9000
8500
8000
7500
7000
6500
6000
5500
A
B
C
D
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6

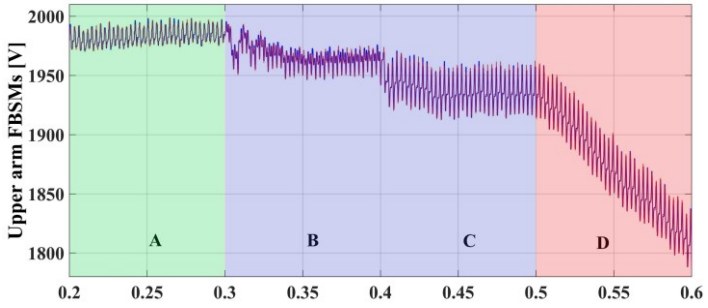
(b)


Phase-difference ϕ [degree]
220
215
210
205
200
195
190
218°
202°
196°
194°
A
B
C
D
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55

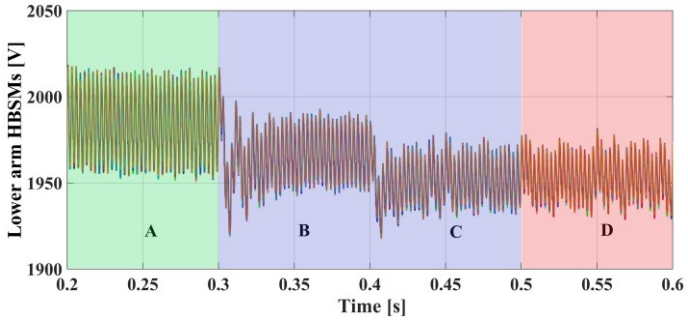
(c)


Upper arm HBSMs [V]
2020
2000
1980
1960
1940
A
B
C
D
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6

(d)



(e)



(f)

Figure 4-8 Simulation results, (a) Upper arm current, (b) Arm ac voltage, (c) Phase difference between upper and lower arms AC voltages., (d) Voltages of upper arm HBSMs, (e) Voltages of upper arm FBSMs and (f) Voltages of lower arm HBSMs.

The simulation results illustrated in Figure 4-8 are segmented into four areas in which, each one is associated with one operating point. As shown in Figure 4-8(a), the ac component of the upper arm current becomes smaller when the phase difference approaches 180^{o} reducing the conduction loss and the current rating of electrical components. The arm ac voltage and phase difference are illustrated in Figure 4-8(b) and (c). The four operating points are created by applying an appropriate arm ac voltage. As the phase difference gets closer to the 180^{o}, a higher arm ac voltage is required. The phase difference at operating points A, B, C, and D are close to the values calculated by analytical studies (see Figure 4-7), confirming the precision of the proposed method. Because $D > 0.5$, the upper arm is the vulnerable arm. The capacitors voltages of the HBSMs and FBSMs in the upper and lower arms are illustrated in Figure 4-8(d), (e) and (f). Although the average voltages of HBSMs and FBSMs are slightly changed at different operating points (A, B, and C), the capacitors voltages are maintained balanced. As expected, at point D, the upper arm capacitors voltages cannot be balanced, where the HBSMs voltages increase, and FBSMs voltages decrease gradually. However, the lower arm HBSMs are still kept balanced at operating point D.

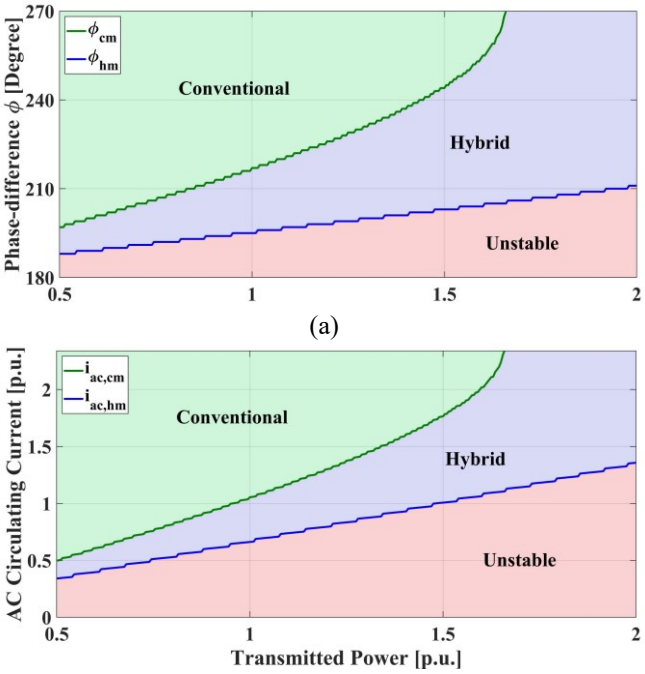


Figure 4-9 Analytical studies results, (a) The minimum feasible phase difference of the conventional (φ_{cm}) and hybrid (φ_{hm}) topologies, (b) The minimum amplitude of ac circulating current in the conventional ($i_{ac,cm}$) and hybrid ($i_{ac,hm}$) topologies, when the transmitted power changes between [0.5, 2].

4.4 Effect Analysis of the Converter Parameters on the Operation Limitation

4.4.1 Transmitted Power

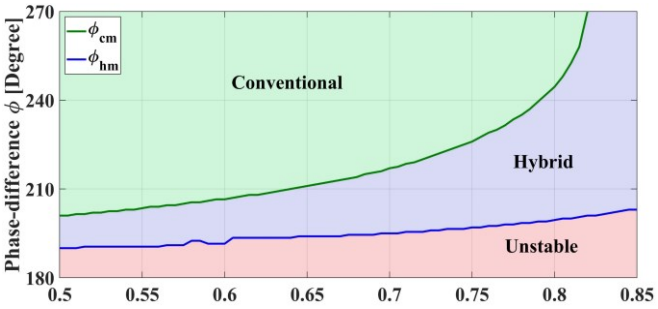
To study the operation limits, the detailed hybrid dc/dc MMC in Table 4-II is analytically investigated for the transmitted powers between 0.5 p.u. and 2 p.u. At each transmitted power, the same analysis performed in Subsection 4.3.1 is carried out to determine the range of operating points associated with the conventional and hybrid topologies. Moreover, the phase differences that the hybrid topology can be designed for, but the capacitors voltages cannot be balanced are highlighted by the term "unstable."

In Figure 4-9(a), the minimum phase differences that can be achieved by the conventional and hybrid topology are depicted by φ_{cm} and φ_{hm} respectively. φ_{hm} is calculated by performing capacitors voltages balance analysis at each transmitted power. The area above φ_{cm} (green area) is the phase differences that can be achieved by conventional topology, and the area

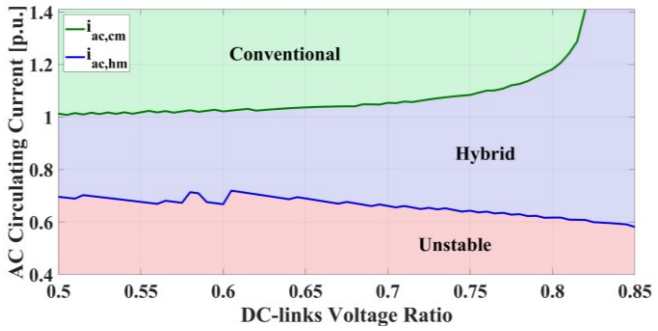
between φ_{cm} and φ_{hm} (blue area) is associated with the phase differences that are only feasible by using the hybrid topology. The red area is the range of phase differences that the capacitors voltages of hybrid topology cannot be balanced. In the steady-state operation, both conventional and hybrid topologies are desired to operate at the minimum phase difference to have the minimum ac circulating current. As shown in Figure 4-9(a), by increasing the transmitted power, the minimum phase difference of both conventional and hybrid topologies increases. Moreover, the unstable area grows because the larger transmitted power requires a higher amplitude of arm ac voltage to neutralize the dc power flow resulting in a higher number of FBSMs. This would unbalance the capacitors voltages at higher phase differences. As illustrated in Figure 4-9(a), the maximum power that can be transmitted by the conventional topology is around 1.65 p.u. while the hybrid topology can transmit more than 2 p.u.. In Figure 4-9(b), the minimum amplitudes of ac circulating current in conventional and hybrid topologies, $i_{ac,cm}$ and $i_{ac,hm}$, with respect to transmitted power are illustrated. At each transmitted power, the minimum ac circulating current is achieved by operating at the minimum phase difference. As shown, in the whole range of transmitted power, the hybrid topology has smaller ac circulating current. As the power transmission increases, the minimum ac current that can be achieved increases. Because larger ac power is needed to neutralize the dc power flow. Although the hybrid topology can be designed to have a very small ac current, the unbalance in the capacitors voltages limits the range of phase differences that the hybrid topology can be designed for.

4.4.2 Conversion Ratio

To study the effect of the conversion ratio, the hybrid dc/dc MMC (detailed in Table 4-II) with conversion ratios between 0.5 and 0.85 are investigated in the same way as in the previous subsection. In Figure 4-10(a), the minimum phase difference that can be achieved by the conventional and hybrid topologies at different conversion ratios are exhibited. As can be seen, by increasing the conversion ratio, the minimum phase difference in both topologies increases. Furthermore, the unstable area in which the capacitors voltages in the hybrid topology cannot be balanced is expanded. From $D = 0.815$ on, the conventional topology is not operational, whereas the hybrid topology is still able to operate at small phase differences. In Figure 4-10(b),



(a)



(b)

Figure 4-10 Analytical studies results, (a) The minimum feasible phase difference of the conventional (φ_{cm}) and hybrid (φ_{hm}) topologies, (b) The minimum amplitude of ac circulating current in the conventional ($i_{ac,cm}$) and hybrid ($i_{ac,hm}$) topologies, when the conversion ratio changes between [0.5, 0.85].

the minimum ac circulating current that can be achieved by operating at the minimum phase difference is shown for the conventional and the hybrid topologies. As illustrated, the hybrid topology has a smaller ac current in the whole range of conversion ratios as compared to the conventional topology. One of the interesting features of the hybrid topology is that the minimum ac circulating current is reduced by increasing the conversion ratio. While in the conventional topology, the minimum ac current increases by increasing the conversion ratio. This is because, in the conventional converter, the feasible arm ac voltage becomes more and more limited by the increase of the conversion ratio due to structural restrictions. However, in the hybrid converter, the arm ac voltage can be freely selected and generated using FBSMs beside the HBSMs. In the hybrid topology, the only limitation is the capacitors voltages balance, which prevents the converter from operating stably in the whole range of phase difference [180°, 270°].

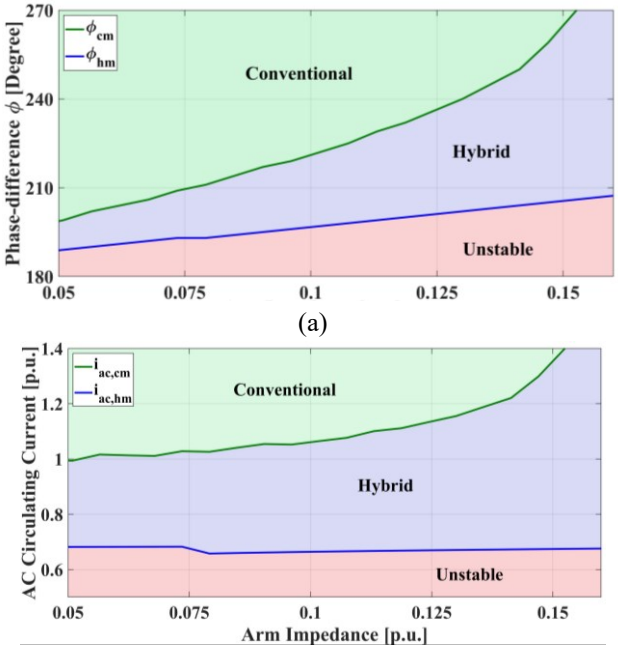


Figure 4-11 Analytical studies results, (a) The minimum feasible phase difference of the conventional (φ_{cm}) and hybrid (φ_{hm}) topologies, (b) The minimum amplitude of ac circulating current in the conventional ($i_{ac,cm}$) and hybrid ($i_{ac,hm}$) topologies, when the arm inductance varies between [0.05, 0.16].

4.4.3 Arm Inductance

Using the proposed analysis method, the effect of the arm inductance on the operation of dc/dc MMC is investigated. In this case, converters with different arm inductances are analyzed, and the ranges of operating points that the conventional and the hybrid topologies can operate are determined. To fully show the impact of the arm inductance on the converter operation, it varies between 0.05 p.u. and 0.16 p.u. From the previous studies [9, 23, 24], it is known that the suitable range of arm inductance is between [0.05 p.u., 0.12 p.u.]. The results are illustrated in Figure 4-11. The minimum achievable phase differences of the conventional and hybrid topologies in each case study are shown in Figure 4-11(a). As the arm inductance increases, the minimum feasible phase difference of both topologies increases. By increasing the arm inductance, the impedance of ac current path becomes larger, and to exchange the same amount of active ac power, $\sin(\varphi)$ must increase (see (7)). Therefore, the corresponding controller pushes φ towards 270°. Moreover, the range of phase differences in which the capacitors voltages of the hybrid topology cannot be kept balanced is enlarged by increasing the arm inductance. The minimum amplitude of the ac circulating current achieved by operating at the

minimum phase difference is illustrated in Figure 4-11(b). As shown, the minimum ac circulating current in the conventional topology increases in response to the increase of the arm inductance whereas the minimum ac circulating current in the hybrid topology is almost constant through different case studies.

4.5 Summary

This chapter studied the capacitors voltages balance of the hybrid dc/dc MMC and characterized the associated operation limits. The proposed approach analytically determines, at each operating point, whether the capacitors voltages of HBSMs and FBSMs could be maintained balanced or not. The phase differences at which the capacitors voltages can be balanced are found using this approach. Detailed simulation results confirmed the results of the analytical study where the operation limits are found. Furthermore, the impact of transmitted power, conversion ratio, and arm inductance on the operation limitation was investigated by performing the capacitors voltages balance analysis in different case studies. The obtained results showed that increasing the transmitted power makes the operation range more limited. Similarly, in converters with a higher conversion ratio and larger arm inductance, the range of phase differences at which capacitors voltages in the hybrid dc/dc MMC can be balanced is smaller. The important outcomes of this study can be highlighted as follows.

- This study found the operation limits of the hybrid dc/dc MMC and determined the minimum phase difference that the converter can operate at. This is necessary for finding the minimum amplitude of the ac circulating current. Moreover, it helps to calculate the current rating of components and estimate the conduction loss.

- Despite the findings in the previous literature, which suggest operating at the maximum arm ac voltage, in some designed hybrid dc/dc MMCs, the arm ac voltage must be limited to avoid operation at phase differences at which capacitors voltages cannot be balanced.

Chapter 5 Fault-Tolerant Operation of the DC/DC MMC

This chapter sheds light on the dc/dc MMC's unique characteristics, which enable fault-tolerant operation. Since the fault detection and localization in the dc/dc MMC is pretty much the same as the dc/ac MMC, this part is ignored in this project. First, it is shown by mathematical analysis that there already exists redundant SMs in one of the arms, which helps the converter to continue the operation after the SM fault without degraded performance. Then, it is discussed that the dc/dc MMC can operate at different operating points with fixed power transmission. Using this feature, the fault-tolerant operation is realized by changing the operating point in the post-fault condition to one, which requires fewer SMs in the faulty arm. Finally, in the worst cases, it is shown that the needed number of SMs can be reduced by decreasing the power transmission. This could help in keeping the converter operational despite several SMs faults. By putting all these features together, a tailored fault-tolerant operation strategy is proposed. The proposed strategy is investigated through three different case studies.

5.1 SM Fault Analysis

In general, failures of IGBTs can happen in two forms: open-circuit faults and short-circuit faults. Modern-day gate drivers mostly include short-circuit protection, which can immediately shut down the faulty IGBT in case of short-circuit fault. In contrast, the open-circuit fault can remain undetected and damage the whole system [55]. Here, an SM fault analysis considering

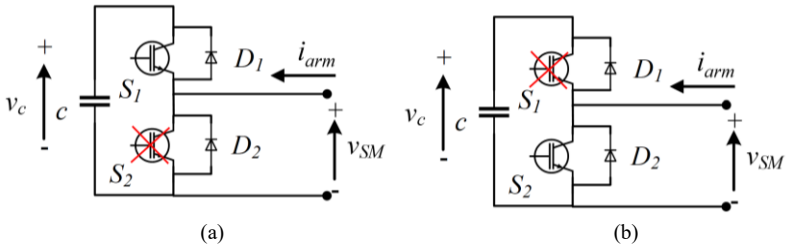


Figure 5-1 Half-bridge-based SM under open-circuit faults, a) S_2 fault and b) S_1 fault.

Table 5-I
Behaviour of Half-Bridge SM Fault Under S1 and S2 Fault

Operation Mode	Switches Status	i_{arm}	v_c	v_{SM}
Normal	**S_1=1, S_2=0. (Inserted)**	>0	Increased	+ v_c
		<0	Decreased	+ v_c
	S_1=0, S_2=1. (Bypassed)	>0	Unchanged	0
		>0	Unchanged	0
S_1 Fault	**S_1=1, S_2=0. (Inserted)**	>0	Increased	+ v_c
		<0	Unchanged	0
	S_1=0, S_2=1. (Bypassed)	>0	Unchanged	0
		<0	Unchanged	0
S_2 Fault	**S_1=1, S_2=0. (Inserted)**	>0	Increased	+ v_c
		<0	Decreased	+ v_c
	S_1=0, S_2=1. (Bypassed)	>0	Increased	+ v_c
		<0	Unchanged	0

one open-circuit fault at a time is presented. As shown in Table 5-I, an open-circuit fault can occur in either of S_1 and S_2 switches, and based on the arm current direction and SM status, it can change the behavior of the faulty SM. To investigate this, Table 5-I is provided where the SM capacitor voltage v_c and the SM output voltage v_{SM} are analyzed in various conditions. As can be seen, in the case of having an open-circuit fault in S_1, the only difference relative to the normal condition occurs when i_{arm}<0 and the SM is inserted. In this situation, D_2 conducts the arm current instead of S_1, and the capacitor voltages remain unchanged. In the case of S_2 fault, the difference relative to the normal operation happens when i_{arm}>0 and the SM is bypassed. In this situation, D_1 conducts the arm current instead of S_2, and the SM capacitor charges.

5.2 Fault-Tolerant Operation of the DC/DC MMC

Unlike the well-known dc/ac MMC, the dc/dc MMC has unique features that allow fault-tolerant operation without the need to add extra SMs. Inherent redundant SMs, and the ability

to reduce the required number of SMs by decreasing the arm ac voltage and the power transmission are the main features which will be elaborated in the following.

5.2.1 Fault-Tolerant Operation Using the Inherent Redundant SMs

In the dc/dc MMC, based on the conversion ratio, always one of the arms has some redundant SMs. If a submodule fault occurs in this arm, the existing redundant SMs empower the faulty arm to generate the same arm voltage as in the pre-fault condition. Therefore, the converter can continue its operation with maximum arm ac voltage despite SM failure. To find the inherent redundant SMs, the basic idea is to find the gap between the maximum arm peak voltage generated by the controller and the maximum voltage which the arm can generate. The maximum arm peak voltage can be found when the arm is generating the maximum ac voltage because the dc part is fixed in steady-state, and only the ac component can change within a range. The maximum voltage that the arm can generate is limited by the converter structure and equals to V_{DC2}. Using this gap voltage, the number of SMs that are not necessary for the operation of the converter with the maximum arm ac voltage can be found. These SMs are the redundancy that naturally exists in the dc/dc MMC.

To calculate the maximum ac voltage, which can be generated by the arm, two points should be noticed. First, because the conventional topology of the dc/dc MMC uses only HBSMs, the arms voltage cannot be negative. Second, the maximum voltage which can be generated by the arm is limited to V_{DC2}. Due to these two restrictions, the maximum arm ac voltage is derived in (13). Figure 5-2 shows the arms voltages when the maximum arm ac voltage is applied for two cases of D (D≥0.5 and D<0.5).

$$v_{AC,max} = min\{V_{DC1}, V_{DC2} - V_{DC1}\} = \begin{cases} V_{DC1} & D < 0.5 \\ V_{DC2} - V_{DC1} & D \geq 0.5 \end{cases} \quad (5\text{-}1)$$

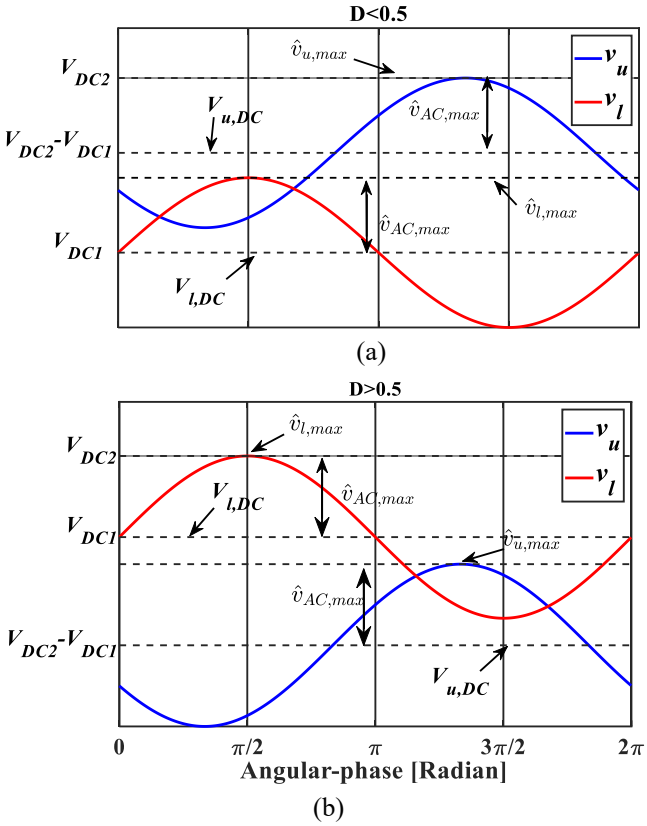


Figure 5-2 The arms voltages when the maximum arm ac voltage is applied, (a) D<0.5, (b) D>0.5.

When the maximum arm ac voltage is applied, the obtained phase difference is the closest one to π, and it is called the minimum achievable phase-difference φ_{min}. This phase difference is calculated using (3-2) and (3-3) as follows:

$$\varphi_{min} = \sin^{-1}\left(\frac{2P_{DC}.X_e}{v_{AC,max}^2}\right), \qquad \text{while } X_e = \frac{X_L^2+2X_LX_{L_0}}{X_{L_0}} \tag{5-2}$$

To find the arm in which the redundancy exists and the number of redundant SMs, two conditions are studied.

- $D \geq 0.5$

By substituting the obtained maximum arm ac voltage in (3-4) and (3-5), the maximum arms peak voltages generated by the controller, $\hat{v}_{u,max}$ and $\hat{v}_{l,max}$, are obtained as

$$\hat{v}_{u,max} = 2(V_{DC2} - V_{DC1}) \tag{5-3}$$

$$\hat{v}_{l,max} = V_{DC2} \tag{5-4}$$

Based on the maximum arm peak voltage, the maximum required number of SMs in the upper and the lower arms, $n_{u,max}$ and $n_{l,,max}$, are

$$n_{u,max} = \left\lceil \frac{\hat{v}_{u,max}}{V_{CN}} \right\rceil = \left\lceil \frac{2N(V_{DC2} - V_{DC1})}{V_{DC2}} \right\rceil < N \tag{5-5}$$

$$n_{l,,max} = \left\lceil \frac{\hat{v}_{l,max}}{V_{CN}} \right\rceil = \left\lceil \frac{N.V_{DC2}}{V_{DC2}} \right\rceil = N \tag{5-6}$$

where N is the number of SMs in the arm and V_{CN} is the SM nominal voltage which is equal to V_{DC2}/N. When the converter operates with $v_{AC,max}$, all the SMs in the lower arm are needed, whereas the required number of SMs in the upper arm is less than N. Therefore, some of the SMs are redundant, and the number of them can be calculated as

$$n_{u,R} = N - n_{u,max} = \left\lceil \frac{N.(2V_{DC1} - V_{DC2})}{V_{DC2}} \right\rceil \tag{5-7}$$

- $D < 0.5$

In this condition, the maximum arms peak voltages are:

$$\hat{v}_{u,max} = V_{DC2} \tag{5-8}$$

$$\hat{v}_{l,max} = 2V_{DC1} \tag{5-9}$$

The maximum required number of SMs can be obtained as follows:

$$n_{u,max} = \left\lceil \frac{\hat{v}_u}{V_{CN}} \right\rceil = \left\lceil \frac{N.V_{DC2}}{V_{DC2}} \right\rceil = N \tag{5-10}$$

$$n_{l,max} = \left\lceil \frac{\hat{v}_l}{V_{CN}} \right\rceil = \left\lceil \frac{2N.V_{DC1}}{V_{DC2}} \right\rceil < N \tag{5-11}$$

When the converter operates with $v_{AC,max}$, the upper arm needs all the SMs, whereas the lower arm requires less than N number of SMs. Hence, some of the SMs are redundant in the lower arm, and the number of them can be calculated by

$$n_{l,R} = N - n_{l,max} = \left\lceil \frac{N.(V_{DC2} - 2V_{DC1})}{V_{DC2}} \right\rceil \tag{5-12}$$

As long as the number of failed SMs in the arm, in which redundancy exists is less than the number of redundant SMs, the converter can continue the operation with $v_{AC,max}$ in the same way as the pre-fault condition. Therefore, SMs failure would not affect converter performance.

5.2.2 Fault-Tolerant Operation with Reduced Arm AC Voltage

The conventional topology of the dc/dc MMC can operate within a range of arm ac voltage while transferring the same amount of power. This feature allows the converter to operate with the nominal power despite the SMs failure. From the fault-tolerant operation perspective, it is important to find the minimum arm ac voltage, which satisfies the internal stability condition. If the maximum feasible ac voltage, which can be generated by the faulty arm, becomes smaller than the minimum allowable value, the converter would not be able to transmit the nominal power.

5.2.2.1 Minimum Allowable Arm AC Voltage

Knowing $\varphi \in [180°, 270°]$ when $P > 0$, the minimum allowable arm ac voltage $v_{AC,min}$ can be found by substituting $\varphi_{max} = 270°$ in (3-10). φ_{max} is the maximum phase-difference that can be achieved when $P > 0$. $v_{AC,min}$ is obtained as

$$v_{AC,min} = \sqrt{2P_{DC}.X_e} \tag{5-13}$$

The dc/dc MMC can operate stably with the arm ac voltage between $v_{AC,min}$ to $v_{AC,max}$. In a nutshell, the upper bound of arm ac voltage $v_{AC,max}$ is limited by the converter structure, and the lower bound results from the stability condition. As earlier studies suggested [24], operation at $v_{AC,max}$ is preferred. Because at this operating point, the converter has the lowest current

rating and conduction loss. Arising from this fact, in the proposed fault-tolerant operation, it is tried to always operate with the maximum feasible arm ac voltage. Moreover, by finding the maximum feasible arm ac voltage in the post-fault condition, it can be determined whether the converter can operate with nominal power or not.

5.2.2.2 Maximum Feasible Arm AC Voltage in Post-Fault Condition

When the number of faulty SMs in the arm in which redundancy exists becomes larger than the number of redundant SMs, or SMs in the arm without redundancy fails, the faulty phase-leg cannot operate with $v_{AC,max}$. To find the maximum feasible ac voltage after SM fault $v'_{AC,max}$, two cases of D are investigated. The associated phase-difference to $v'_{AC,max}$ is called the minimum achievable phase difference in the post-fault condition and is denoted by φ'_{min}.

a) $D \geq 0.5$

As shown earlier, when D ≥ 0.5, $n_{u,R}$ SMs in the upper arm are redundant. Before SMs failure, $v_{AC,max}$ is equal to $V_{DC2} - V_{DC1}$. After SMs failure, this voltage cannot be generated, and the value for the maximum feasible arm ac voltage must be recalculated. In this condition, two different cases of SM failure can occur.

- ***SM Failure in the Upper Arm:*** By failure of n_f SMs in the upper arm, the maximum voltage which can be applied by the upper arm SMs is reduced to $V_{DC2} - n_f.V_{CN}$. Assuming that the number of faulty SMs n_f is higher than the number of redundant SMs $n_{u,R}$, the maximum feasible arm ac voltage is limited by the upper arm maximum voltage, and it is equal to $V_{DC1} - n_f.V_{CN}$.

- ***SM Failure in the Lower Arm:*** Any failure in the lower arm while $D > 0.5$ would result in disability of the respective phase-leg in the generation of $v_{AC,max}$. When n_f SMs fails, the maximum voltage that the lower arm can generate is reduced to $V_{DC2} - n_f.V_{CN}$. Therefore, the maximum feasible arm ac voltage is limited by the lower arm maximum voltage, and it is equal to $V_{DC2} - V_{DC1} - n_f.V_{CN}$.

b) $D < 0.5$

When $D < 0.5$, $n_{l,R}$ SMs in the lower arm is redundant. Before SMs fault, the maximum ac voltage is V_{DC1}. After a fault, the capability of the respective phase-leg in the generation of ac voltage would be reduced. To recalculate the maximum ac voltage, two cases are investigated.

- ***SM Failure in the Upper Arm:*** Even a single SM failure in the upper arm while $D < 0.5$ would disable the converter from operating with $v_{AC,max}$. Assuming that n_f number of SMs in the upper arm fails, the maximum feasible arm ac voltage is restricted by the upper arm maximum voltage, and it equals to $V_{DC1} - n_f.V_{CN}$.

- ***SM Failure in the Lower Arm:*** When n_f SMs fail in the lower arm, the maximum voltage that can be generated reduces to $V_{DC2} - n_f.V_{CN}$. Knowing that $n_f > n_{l,R}$, the maximum ac voltage is limited by the lower arm maximum voltage, and it is $V_{DC2} - V_{DC1} - n_f.V_{CN}$.

5.2.2.3 Current Harmonics in DC-link 1 and 2

When one phase-leg of the converter is required to reduce the arm ac voltage from $v_{AC,max}$ to $v'_{AC,max}$ in the post-fault condition, the phase difference between the arms ac voltages would also change from φ_{min} to φ'_{min}. However, the healthy phase-legs can still operate at φ_{min} by applying $v_{AC,max}$. If the phase legs of the converter operate with different phase differences, the induced circulating current in the phase legs will not cancel out each other, and it will leak into dc-link 2, which is not acceptable. In the following, it will be shown how the ac circulating current leaks into dc-link 2 and not into dc-link 1.

Assuming that X_L is negligible relative to X_{L_0}, the ac circulating current in the upper and lower arms would be equal as

$$\vec{i}_{l,AC} = \vec{i}_{u,AC} = -\frac{\vec{v}_{l,AC} + \vec{v}_{u,AC}}{j2X_L} \tag{5-14}$$

Finally, using (3-3) and (5-14), the amplitude of arm ac current is derived based on the phase difference and the transmitted power.

$$\hat{i}_{AC} = 2\sqrt{\frac{(1-D)P}{M.2X_L.\tan\left(\frac{\varphi}{2}\right)}} \tag{5-15}$$

To find the leaked ac circulating current into the dc-links, it is assumed that the dc/dc MMC has two phase-legs. Phase-leg 1 is the faulty one that operates with $v'_{AC,max}$ (φ'_{min}), and phase-leg 2 is healthy operating with $v_{AC,max}$ (φ_{min}). Based on Figure 3-1, the leaked ac circulating current from phase-leg 1 and 2 into the dc-link 1, $\vec{i}_{1o,AC}$ and $\vec{i}_{2o,AC}$, are obtained in the phasor-domain by

$$\vec{i}_{1o,AC} = \vec{i}_{1u,AC} - \vec{i}_{1l,AC} \tag{5-16}$$

$$\vec{i}_{2o,AC} = \vec{i}_{2u,AC} - \vec{i}_{2l,AC} \tag{5-17}$$

The leaked ac current from the converter into dc-link 1, $i_{DC1,AC}(t)$, is calculated by

$$\vec{i}_{DC1,AC} = \vec{i}_{1o,AC} + \vec{i}_{2o,AC} \tag{5-18}$$

Using (5-14), the following equation can be derived

$$\begin{aligned}\vec{i}_{DC1,AC} &= \frac{-\vec{v}_{1u,AC} - \vec{v}_{2u,AC} + \vec{v}_{1l,AC} + \vec{v}_{2l,AC}}{j(X_L + 2\cdot X_{L_0})} \\ &= \frac{-v'_{AC,max}\angle\varphi'_{min} - v_{AC,max}\angle(\varphi_{min}+\pi) + v'_{AC,max} + v_{AC,max}\angle(\pi)}{j(X_L + 2\cdot X_{L_0})}\end{aligned} \tag{5-19}$$

In the pre-fault condition, $\vec{i}_{DC1,AC}$ is zero because between the arms ac voltages, of the two phase legs, there exists a 180° phase-shift and the amplitude of arms ac voltages is equal to $v_{AC,max}$. However, in the post-fault condition, the arms ac voltage in the two phase-legs is not equal due to SMs failure, and therefore the phase legs operate at different phase differences. As a result, the nominator of (5-19) would not be zero anymore. Because X_{L_0} is a very large impedance, the leaked ac current into the dc-link1 is still negligible.

The leaked ac circulating current into the dc-link 2 in the phasor-domain $\vec{i}_{DC2,AC}$ can be found as

$$\vec{i}_{DC2,AC} = \vec{i}_{1u,AC} + \vec{i}_{2u,AC} \tag{5-20}$$

Using (5-14), the following equation can be derived:

$$\vec{i}_{DC2,AC} = \frac{(X_L + X_{L_0}).(\vec{v}_{1u,AC} + \vec{v}_{2u,AC}) + X_{L_0}(\vec{v}_{1l,AC} + \vec{v}_{2l,AC})}{j(X_L^2 + 2X_{L_0}.X_L)} \tag{5-21}$$

Assuming $X_{L_0} \gg X_L$, (5-21) can be approximated by

$$\vec{i}_{DC2,AC} = \frac{(\vec{v}_{1u,AC} + \vec{v}_{2u,AC}) + (\vec{v}_{1l,AC} + \vec{v}_{2l,AC})}{j2X_L} \tag{5-22}$$

Replacing the phasor-domain values of the arms voltages in (5-22), it will be

$$\vec{i}_{DC2,AC} = \frac{v'_{AC,max}\angle\varphi'_{min} + v_{AC,max}\angle(\varphi_{min} + \pi) + v'_{AC,max} + v_{AC,max}\angle(\pi)}{j2X_L} \tag{5-23}$$

As can be seen, the nominator of (5-23) in the pre-fault condition is equal to zero, whereas, in the post-fault condition, it would not be zero anymore. Unlike (5-19), the denominator in (5-23) is not big enough to make $\vec{i}_{DC2,AC}$ negligible. Therefore, if the phase-legs operate with different phase-differences, the induced ac circulating current would leak into the dc-link 2, which is not acceptable. To avoid this issue, the arms ac voltages in the healthy arm should also change in response to the reduction of arm ac voltage in the faulty phase-leg. In this way, the leakage of the ac circulating current into dc-link 2 can be suppressed.

5.2.3 Fault-Tolerant Operation with Reduced Power Transmission

If the number of failed SMs increases such that the maximum feasible arm ac voltage in the post-fault condition, $v'_{AC,max}$, becomes smaller than the minimum allowable arm ac voltage, $v_{AC,min}$, the converter should either be shut down or operate with reduced power transmission. By reducing the transmitted power, the amount of needed ac power to satisfy the internal stability condition is decreased. Accordingly, the minimum allowable arm ac voltage can be

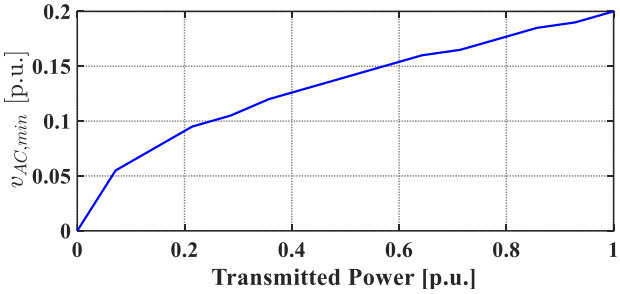


Figure 5-3 The minimum allowable arm ac voltage with respect to the transmitted power in p.u..

reduced. In Figure 5-3, the minimum allowable arm ac voltage with respect to the transmitted power is illustrated for a typical dc/dc MMC. The base values for power and voltage are equal to 14 MW and 20 kV. As can be seen, when the converter transmits nominal power, $v_{AC,min}$ equals to 0.2 p.u., and by decreasing the transmitted power, it is reduced. Using this feature, the converter can continue its operation with reduced power transmission. Assuming that the maximum feasible arm ac voltage in the post-fault condition is $v'_{AC,max}$, the maximum amount of the ac power which can be exchanged between the arms in the post-fault condition,P'_{AC}, is calculated by

$$P'_{AC} = -\frac{1}{2X_e}\left(v'_{AC,max}\right)^2 \tag{5-24}$$

Equation (5-24) is derived by considering $\varphi = 270°$ in (3-3). Using (3-1), the maximum power which the converter can transmit in the post-fault condition is found as

$$P' = \frac{M}{1-D}.P'_{AC} \tag{5-25}$$

The dc/dc MMC can operate with any power less than P' in the post-fault condition. In this way, the required arm ac voltage would be smaller than $v'_{AC,max}$ which can be generated by the faulty phase-leg.

5.2.4 Fault-Tolerant Operation Considering the Arm Peak Current Limit

The arms currents have two parts, the dc and ac components. The dc part is determined by the dc power flow, and it is constant when the converter transmits a fixed amount of power. However, the ac part can change with respect to the changes in the arm ac voltage. In some

cases, the arm peak current may be limited by the switches current rating. From the control perspective, it is easier to deal with the limit on the arm ac current, which can be calculated by deducting the arm dc current from the maximum safe peak current of the switches. In other words, since the arm dc current is fixed, the limit on the arm peak current can be translated to the limit on the arm ac current $\hat{\imath}_{AC,n}$.

To elucidate the relation between the arm ac voltage and the arm ac current, assume that P and P_{AC} are fixed and $P > 0$ so $\varphi \in [180°, 270°]$. When the arms ac voltage increases, φ would decrease and move toward 180°. From (5-15), it can be seen that by decreasing φ, $\hat{\imath}_{AC}$ would also decrease. Therefore, in general, by increasing the arm ac voltage, the ac circulating current is reduced. As mentioned earlier, the arm ac voltage in the dc/dc MMC can vary within the range of $[v_{AC,min}, v_{AC,max}]$. Accordingly, the resulted ac circulating current would be in the range of $[i_{AC,min}, i_{AC,max}]$, which $i_{AC,min}$ occurs when $v_{AC,max}$ is applied and $i_{AC,max}$ is resulted when $v_{AC,min}$ is generated by the arms. In Figure 5-4, the ac circulating current with respect to the arm ac voltage is shown for a typical dc/dc MMC. The base values for power and voltage are equal to 14 MW and 20 kV. As can be seen, the amplitude of ac current can change from 1.3 to 0.7 p.u. when the arm ac voltage changes from 0.2 to 0.3. This wide range of ac current heavily affects the conduction loss and current rating of the components. Therefore, having a limit on the arm ac current sounds reasonable to increase the life span of the components by limiting the conduction loss or even to reduce the current rating of electrical devices, cutting the initial cost. Let's assume that a limit on the ac circulating current, $\hat{\imath}_{AC,n}$, is considered for the converter. This current limit can also be translated to the arm ac voltage. In other words, to always have an ac current smaller than $\hat{\imath}_{AC,n}$, the arm voltage should be larger than $v_{AC,n}$ which can be calculated from (5-15). If the faulty phase-leg cannot generate $v_{AC,n}$ in the post-fault condition, the transmitted power should be reduced. The new transmitted power should be calculated considering the maximum feasible arm ac voltage $v'_{AC,\max}$ and the arm ac current limit $\hat{\imath}_{AC,n}$. From (5-14), the arm ac current can be obtained based on the phase-difference and the arm ac voltage as

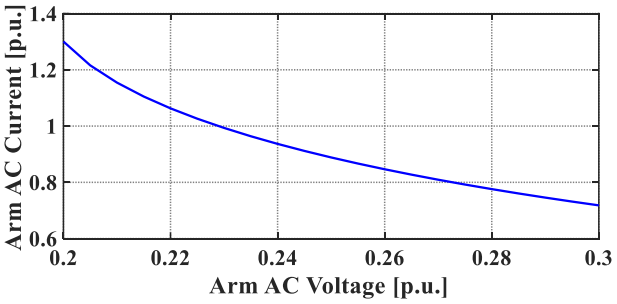


Figure 5-4 The arm ac current with respect to the arm ac voltage in p.u..

$$\hat{i}_{AC} = \frac{1}{X_L} v_{AC} \,.\cos(\frac{\theta}{2}) \tag{5-26}$$

By substituting $v'_{AC,\max}$ and $\hat{i}_{AC,n}$ in (5-26), the phase difference is calculated. Then, by using (3-3), the new power transmission that satisfies the arm ac current limit is achieved.

5.2.5 The Proposed Fault-Tolerant Operation Strategy

In Figure 5-5, the flowchart of the proposed fault-tolerant operation strategy is presented. First, the location and number of faulty SMs are determined. If the redundant SMs exist in the faulty arm, the minor reference adjustment is applied. If there are no redundant SMs, the maximum feasible arm ac voltage $v'_{AC,max}$ must be calculated. If the calculated arm voltage can satisfy the internal stability condition ($v'_{AC,max} > v_{AC,min}$), it would be applied, and the major reference adjustment should be executed. When there is a limit on the ac circulating current, the maximum feasible arm ac voltage $v'_{AC,max}$ must be larger than the minimum permitted ac voltage ($v_{AC} > v_{AC,n}$) so that the converter can operate with nominal power. When the maximum feasible arm ac voltage $v'_{AC,max}$ in the post-fault condition is less than $v_{AC,min}$ or $v_{AC,n}$, the transmitted power by the converter must be reduced. To accomplish this, the maximum power at which the converter can operate is obtained from (5-25) based on the calculated $v'_{AC,max}$. Then, by changing the dc current references, the power transmission is reduced to P'.

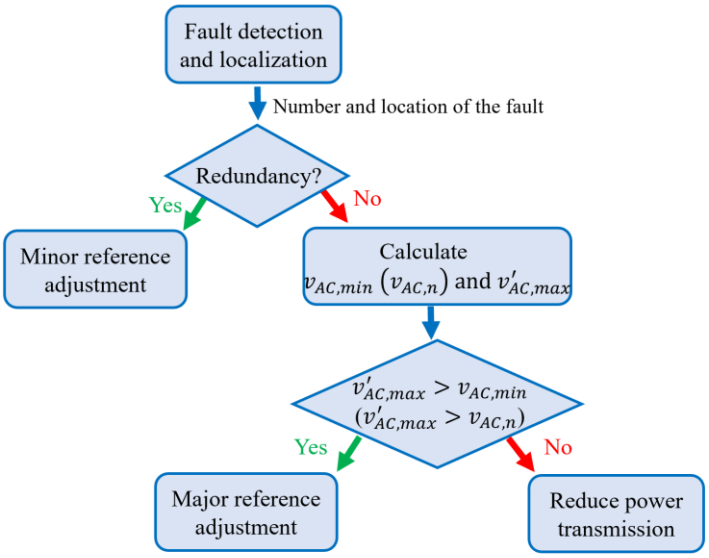


Figure 5-5 Flowchart of the proposed fault-tolerant operation.

5.2.5.1 Minor Reference Adjustment

When the number of failed SMs n_f in the arm in which the redundancy exists is less than the number of redundant SMs n_R, the only necessary modification in the control procedure is to remove the faulty SM from the sorting algorithm. This will stop sending gating signals to the failed SM. Moreover, the number of redundant SMs should be updated to $n_R - n_f$. In this condition, the converter can continue its operation with $v_{AC,max}$.

5.2.5.2 Major Reference Adjustment

When the number of failed SMs in the arm in which redundancy exists exceeds the number of redundant SMs or one of the SMs in the arm without redundancy fails, a major reference adjustment is needed. Here is the list of modifications needed to ensure the stable operation of the converter in the post-fault condition.

- After the fault detection, the first action to take is to remove the faulty SM from the sorting algorithm.

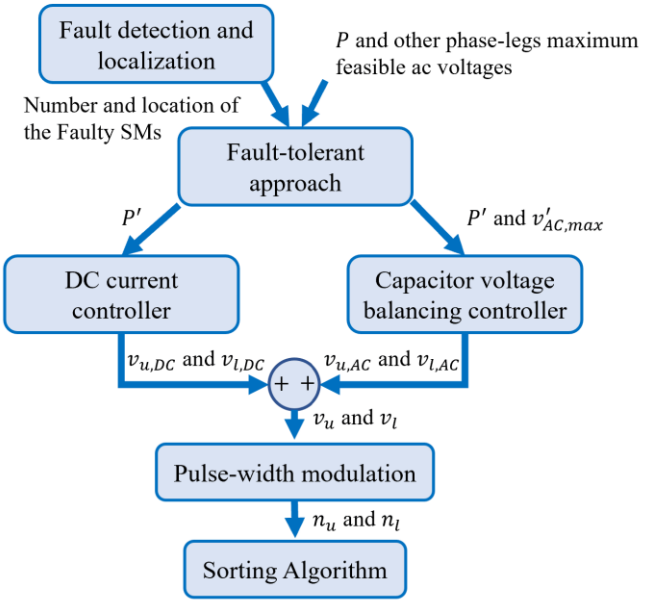


Figure 5-6 One phase-leg controller including the proposed fault tolerant approach.

- As the converter is not able to operate with $v_{AC,max}$ (φ_{min}) in the post-fault condition, the calculated maximum feasible arm ac voltage $v'_{AC,max}$ would be used as the reference value.

- As shown earlier, when the dc/dc MMC phase-legs operate at different phase differences, the induced ac circulating current leaks into the dc-link 2; therefore, to avoid this, the arm ac voltage in all phase-legs should be equal. It means that the arm ac voltage in the healthy phase-legs should also change to the post-fault value of the faulty phase-leg ($v'_{AC,max}$).

5.2.6 Closed-Loop Controller Beside the Proposed Fault-Tolerant Approach

The overall control diagram of one phase-leg, including the proposed fault-tolerant approach, is demonstrated in Figure 5-6. In this study, the proposed closed-loop control in [24] is used. As shown, the number and location of the faulty SMs in the phase-leg is determined by the fault detection and localization section, and the data is sent to the fault-tolerant algorithm. Moreover, the maximum feasible arm ac voltages of other phase-legs are also sent to this section. Then, the fault-tolerant algorithm decides on the maximum arm ac voltage $v'_{AC,max}$

and the transmitted power P' in the post-fault condition. If the arm ac voltage or the transmitted power is reduced by the other phase-legs, the fault-tolerant algorithm changes $v'_{AC,max}$ and P' to prevent ac current leakage. The operation of the proposed fault-tolerant approach is explained in Figure 5-5. Afterward, the dc current control regulates the dc-links currents to enable transmission of P' power by changing the arms dc voltages. At the same time, the capacitors voltages balancing control tries to balance the upper and lower arms capacitors voltages by injecting proper ac circulating current. This block determines the arms ac voltages, which generate the proper ac current. A level-shift modulation is used to determine the number of active SMs in each arm. To balance the capacitors voltages in one arm, the sorting algorithm proposed in [54] is used, which determines the gating signals of switches. In normal conditions, when there is no faulty SM, the transmitted power in post-fault condition P' would be equal to the main reference P, and the maximum feasible arm ac voltage $v'_{AC,max}$ would be the same as the maximum arm ac voltage in the pre-fault condition $v_{AC,max}$. Therefore, the proposed fault tolerant approach does not affect the normal operation of the converter.

In the dc/dc MMC, each phase-leg has its own controller equipped with the proposed fault-tolerant approach. Furthermore, each phase-leg controller operates almost independently of the other phase-leg controllers. Therefore, the proposed fault-tolerant approach can be implemented in the dc/dc MMC with any number of phase-legs by simply adding the fault-tolerant algorithm to the phase-leg controller.

5.3 Simulation Studies

To investigate the fault-tolerant operation of the dc/dc MMC, three scenarios are simulated in the MATLAB\Simulink environment. The main parameters of the converter are illustrated Table 5-II. In the simulation studies, it is assumed that the fault detection and localization are realized by another part of the controller, and to replicate the SM fault, the open-circuit fault occurs in the switch S_1 (see Figure 5-1) of the HBSM. To have realistic simulation studies, a 2 ms delay is considered for the fault detection part, and after this time, the converter would operate based on the proposed fault-tolerant strategy. This time delay is adopted from the available fault detection methods proposed in [56-58], considering 360 Hz operation frequency.

Table 5-II
Main Parameters of the Simulated Converter

Common Parameter	Symbol	Value	Per Unit
Rated Power	P	14 MW	1
DC-Link1	V_{DC1}	14 kV	0.7
DC-Link2	V_{DC2}	20 kV	1
Arm Inductance	L	0.8 mH	0.067
Phase Inductance	L_0	0.26 H	21.67
SM Capacitance	C	10 mF	-
SM Nominal Voltage	V_{CN}	2 kV	0.01
Operating Frequency	f_S	360 Hz	-
Number of Upper Arm HBSMs	n_u	10	-
Number of Lower Arm SMs	n_d	10	-

Table 5-III
A Brief Illustration of Simulation Case-Studies

Case Study	Fault Incident and Limitation	Arm AC Voltage	Power Transmission
Case I	• Upper arm SM Failure at t=0.4 s. • Lower arm SM Failure at t=0.7 s.	Reduced from 6 kV to 4 kV at t=0.7 s.	Fixed at 14 MW
Case II	• Lower arm SM Failure at t=0.4 s. • 850 A limit on the ac circulating current.	Reduced from 6 kV to 4 kV at t=0.4 s.	Reduced from 14 MW to 10.5 MW at t=0.4 s.
Case III	• Lower arm SM Failure at t=0.4 s. • Lower arm SM Failure at t=0.7 s.	Reduced from 6 kV to 4 kV at t=0.4 s and from 4 kV to 2 kV at t=0.7 s.	Reduced from 14 MW to 3.5 MW at t=0.7 s.

The simulation studies focus on the steady-state operation of the dc/dc MMC operating with the proposed fault-tolerant strategy in the post-fault condition. Three different case studies are investigated to fully analyze the post-fault operation of the converter. The fault incidents and limitations, the arm ac voltage, and the transmitted power in each case are exhibited in Table 5-III.

5.3.1 Case I: Fixed Power Transmission

In this case study, the dc/dc MMC operation in the post-fault condition with fixed power transmission is analyzed. The simulation results are shown in Figure 5-7, where at $t = 0.4$ and $0.7\ s$, one of the SMs in the upper and lower arms fails, respectively. When one of the upper arm SMs fails at $t = 0.4$, the converter continues the operation with the same arm ac voltage

and transmitted power. Because based on the analysis presented in this study, the upper arm has two redundant SMs, and only minor reference adjustment is required. However, when one of the lower arm SMs fails at $t = 0.7$, the lower arm cannot generate the 6 kV arm ac voltage since there is no redundancy. Therefore, the arm ac voltages of both phase-legs are reduced to 4 kV, while the converter still transmits 14 MW (major reference adjustment).

The dc-links and arms currents are presented in Figure 5-7(a) and (b). As can be seen, the dc-link 1 current experiences a negligible transient since it is constantly regulated by the main controller. The dc-link 2 current oscillates after each fault incident and reaches a steady state within 0.2 s. The arms currents also experience a transient mode after $t = 0.4$ and $0.7\ s$. As illustrated, the amplitude of ac circulating current is increased at $t = 0.7\ s$, because the available arm ac voltage is reduced due to the SM failure. The amplitude of arm ac circulating current in the pre-fault condition is 690 A, and after the fault incident, it is increased to 1272 A. In Figure 5-7 (c), the arms voltages are depicted where it is shown that the amplitude of arm ac voltage is reduced from 6 kV to 4 kV at $t = 0.7\ s$ due to SM failure in the lower arm. It is noteworthy that the SM failure in the upper arm does not affect the arm ac voltage. Because in the pre-fault condition, the arm peak voltage is 12 kV and noticing the capability of the upper arm in the generation of voltage up to 20 kV, four redundant SMs exist in the upper arm. The phase differences of phase-legs 1 and 2 are presented in Figure 5-7 (d). As analyzed earlier in this chapter, to avoid the leakage of the ac circulating current into dc-link 2, the two phase-legs of the dc/dc MMC should operate at the same phase difference. To accomplish this, the amplitude of arm ac voltage in the healthy phase-leg (phase-leg 2) is reduced to 4 kV at $t = 0.7\ s$. As shown, the phase differences of phase-leg 1 and 2 have the same steady-state value, whereas, during the transient mode, they oscillate with a 180° phase shift. The capacitors voltages of the upper and lower arms are illustrated in Figure 5-7(e) and (f), respectively. The

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5-7 Simulation results of case I, (a) the dc links currents, (b) the upper and lower arms current, (c) the upper and lower arms voltages, (d) the phase-differences of the two phase-leg, (e) the capacitors voltages of HBSMs in the upper arm, (f) the capacitor voltage of HBSM in the lower arm.

capacitors voltages of both arms experience a transient mode after the fault incident and reach the steady-state within 0.2 s. As shown, at $t = 0.4$ and $0.7\ s$, an open-circuit fault happens in one of the upper and lower arms SMs, respectively. After 2 ms of fault incident, the faulty SMs are isolated, and their voltages remain constant.

5.3.2 Case II: Limited AC Circulating Current

As mentioned earlier, some designers may desire to limit the arm peak current to reduce the initial cost and conduction losses. To make an example of this strategy, the amplitude of the ac circulating current with respect to the arm ac voltage, is depicted in Figure 5-8. This study is carried out on the dc/dc MMC detailed in Table 5-II operating with the nominal power. As shown, the maximum arm ac voltage ($v_{AC,max}$) is 6 kV in the pre-fault condition, which results in minimum ac circulating current ($\hat{\imath}_{AC,min}$) 0.71 A. The minimum arm ac voltage ($v_{AC,min}$) which satisfies the internal stability condition is 3.9 kV, which generates the maximum ac circulating current ($\hat{\imath}_{AC,max}$) 1.55 kA. Assume that there is a 1.2 kA limit on the arm peak current due to the switches current rating. When the converter transmits 14 MW, the upper and lower arms dc currents are equal to 350 A and 150 A. Therefore, if the converter transmits 14 MW, the arm ac current in the upper and lower arms should not exceed 0.85 kA and 1.05 kA, respectively. This current limit does not affect the steady-state operation of the converter since it operates with the maximum arm ac voltage ($v_{AC,max} = 6$ kV) which generates the minimum ac circulating current ($\hat{\imath}_{AC,min}$= 0.71 A). However, when one of the lower arm SMs fails, the maximum feasible arm ac voltage ($v'_{AC,max}$) would reduce to 4 kV, which results in the ac

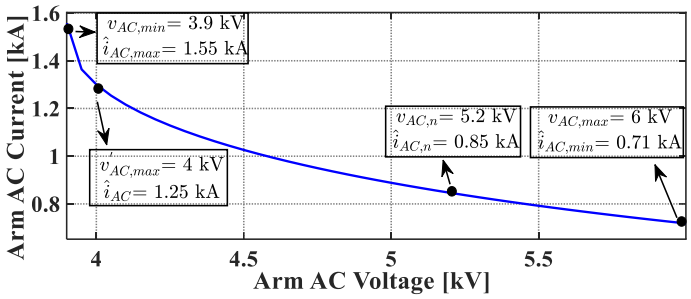


Figure 5-8 The arm ac circulating current with respect to the arm ac voltage for the dc/dc MMC.

(a)

(b)

(c)

(d)

(e)

Figure 5-9 Simulation results of case II, (a) the dc links currents, (b) the upper and lower arms current, (c) the upper and lower arms voltages, (d) the capacitors voltages of HBSMs in the upper arm, (e) the capacitor voltage of HBSM in the lower arm.

circulating current of 1.25 kA (see Figure 5-8). Based on the applied current limit on the circulating current, this operating point is not acceptable. Therefore, the proposed fault-tolerant strategy reduces power transmission from 14 MW to 10.5 MW to have the same arm peak current as in the pre-fault condition.

The simulation results are shown in Figure 5-9. The dc-links and arms currents are presented in Figure 5-9 (a) and (b). As can be seen, dc-link 2 current starts oscillating after the fault and damps within 0.1 s. The current oscillation of dc-link 1 is negligible, and it reaches the steady-state value after 0.05 s. The dc-links currents are decreased in response to the power transmission reduction command. Although the ac circulating current increased from 690 A to 780 A, the arms peak currents remained around 1 kA to enable the safe operation of the converter. This is because the dc currents in the upper and lower arms are reduced from 350 A and 150 A to 260 A and 115 A, respectively. The arms voltages in pre- and post-fault conditions are shown in Figure 5-9 (c). As shown, the arm ac voltage is reduced to 4 kV in the post-fault condition. The capacitors voltages of the upper and lower arms are illustrated in Figure 5-9(d) and (e). All the capacitors voltages experience a transient mode after $t = 0.4\ s$ but reach the steady-state value in less than 0.1 s. As can be seen, one of the lower arm SMs fails at $t = 0.4\ s$, and its voltage remains constant for the rest of the simulation.

5.3.3 Case III: Reduced Power Transmission

In this case study, the operation of the dc/dc MMC in the post-fault condition with reduced power transmission is analyzed. The simulation results are shown in Figure 5-10, where at

(a)

(b)

(c)

(d)

(e)

Figure 5-10 Simulation results of case III, (a) the dc links currents, (b) the upper and lower arms current, (c) the upper and lower arms voltages, (d) the capacitors voltages of HBSMs in the upper arm, (e) the capacitors voltages of HBSMs in the lower arm.

$t = 0.4$ s and 0.7 s, one of the SMs in the lower arms fails. As mentioned earlier, there are no redundant SMs in the lower arm. Therefore, when the first SM failure happens at $t = 0.4$ s, the arm ac voltage is reduced from 6 kV to 4 kV, and the power transmission is remained intact (major reference adjustment). When the second SM failure occurs at $t = 0.7\ s$, the maximum feasible arm ac voltage is reduced to 2 kV, which is smaller than the minimum allowable arm ac voltage 3.9 kV (see Figure 5-8). Therefore, the proposed fault-tolerant approach reduces the transmitted power from 14 MW to 3.5 MW to enable operation after the second SM failure.

The dc-links and arms currents are shown in Figure 5-10 (a) and (b). The transient mode in the dc-link 2 current is more severe than the dc-link 1 current. Moreover, the transient mode duration is longer after the second SM failure. Because, in this condition, the converter utilizes a relatively smaller arm ac voltage (2 kV instead of 4 kV) to balance capacitors voltages. As shown in Figure 5-10 (b), the arms currents increase after $t = 0.4$ s, due to the reduction in the arm ac voltage. After $t = 0.7$ s, the arms currents experience a relatively long transient (1 s), which is because of the slow dynamic of the capacitor voltage balancing controller. The arms voltages are illustrated in Figure 5-10 (c). After each fault incident, 2 kV is deducted from the arm ac voltage. The upper and lower arms capacitors voltages are depicted in Figure 5-10 (d) and (e). As can be seen, the transient mode is much longer and more severe after the second fault. This is because the arm ac voltage, which is necessary to balance capacitors voltages, is extremely reduced compared to the pre-fault condition (from 6 kV to 2 kV). Therefore, it takes longer for the controller to reach a steady state. After $t = 0.7$ s, the capacitors voltages of the upper arm jump to 2.1 kV and turn back to 2 kV within 1.5 s. The capacitors voltages of the lower arm experience minor transient, which enables them to get back to nominal voltage in a shorter time.

5.4 Summary

This chapter proposed a fault-tolerant operation strategy for the dc/dc MMC using its unique characteristics. It was shown that, unlike the dc/ac MMC, the dc/dc MMC could continue its operation after the SM fault without the need to add redundant SMs. Three key features of the dc/dc MMC helping the post-fault operation are 1) inherent redundancy, 2) capability of

operating within a range of arm ac voltage, and 3) reduction in the needed number of SMs by decreasing the power transmission. The satisfactory performance of the proposed strategy was observed in the three simulated scenarios. The first scenario showed that if the faulty arm has redundant SMs, the converter continues its operation with the maximum arm ac voltage. In the case of not having redundant SMs in the faulty arm, by reducing the arm ac voltage, the post-fault operation is realized at the cost of increased ac circulating current. The second case study showed that when the ac circulating current is limited, the fault-tolerant operation cannot be realized by only reducing the arm ac voltage. To satisfy the applied current limit, the power transmission must decrease to prevent increasing the circulating current. In the third scenario, a severe SMs fault was simulated, where two consecutive SMs faults occurred in the lower arm. This study showed that by reducing the power transmission and the arm ac voltage, the converter could tolerate several SMs faults in one arm.

From the power loss perspective, when one of the SMs fails, the number of available SMs will reduce. Therefore, having the same power transmission, the switching frequency would increase. Moreover, in cases where power transmission remains constant in the post-fault condition, an increase in the arm ac circulating current is observed, which increases the conduction loss. In summary, it can be stated that the converter power losses in the post-fault condition are likely to be higher than in the pre-fault condition. However, this condition is temporary, and the efficiency would return to the nominal value as soon as the faulty SMs are replaced.

Chapter 6 Unsymmetrical Operation of the DC/DC MMC

This chapter aims to develop detailed and simplified steady-state models that, unlike the previous models, can show the dc/dc MMC behavior in the unsymmetrical condition. The developed models are verified by the simulation results and compared with the presented steady-state model of the dc/dc MMC in [25].

6.1 Detailed Steady-State Model of the DC/DC MMC

6.1.1 Average Model of the Phase-leg

Assume that the dc/dc MMC has many SMs in each arm, which enable the arm to generate a solid sinusoidal waveform. Moreover, the sorting algorithm works properly so that the SMs capacitors voltages of each arm are equal at any time instant. With these assumptions, the average model of one phase-leg of the dc/dc MMC can be obtained as presented in Figure 6-1. The modulated voltage of arm-*t,* v_t, and the modulated current of arm-*t,* i_{ct}^{Σ}, are defined as

$$v_t = m_t . v_{ct}^{\Sigma} \tag{6-1}$$

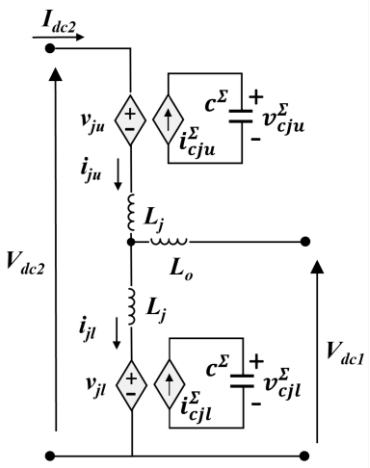


Figure 6-1 Averaged model of phase-leg-*t* in the dc/dc MMC.

$$i_{ct}^{\Sigma} = m_t . i_t \tag{6-2}$$

where, v_{ct}^{Σ} and i_t are the sum of capacitors voltages of arm-*t* and the arm-*t* current, and m_t is the modulation signal. By writing the voltage-current equation for the equivalent capacitor and using (6-2), the following equation can be obtained

$$c^{\Sigma} . \frac{dv_{ct}^{\Sigma}}{dt} = m_t . i_t \qquad \text{where} \quad c^{\Sigma} = \frac{c}{N} \tag{6-3}$$

in which c^{Σ} is the equivalent capacitance of *N* serried SMs with *c* capacitance. Assuming that the controllers can regulate the average SMs voltages at nominal value, V_{dc2}/N, the sum of capacitors voltages in arm-*t* can be approximated by the dc and the first harmonics as,

$$v_{ct}^{\Sigma} = V_{dc2} + v_{ct} \cos(\omega t + \theta_{ct}) \tag{6-4}$$

where v_{ct} and θ_{ct} are the amplitude and phase difference of the first harmonic. The arms reference voltages, v_u^* and v_l^*, are defined as

$$v_u^* = (V_{dc2} - V_{dc1}) + v_{ac} \cos(\omega t + \varphi) \tag{6-5}$$

$$v_l^* = (V_{dc1}) + v_{ac} \cos(\omega t) \tag{6-6}$$

where v_{ac} is the amplitude of arm ac voltage, and φ is the phase-difference between the upper and lower arms ac voltages. ω is called the operating frequency and can be selected arbitrarily. The amplitude of the upper and lower arms ac voltages is chosen to be equal. Because based on the [24], the amplitude of arm ac circulating current can be minimized. The ac part of the arm reference voltage is responsible for generating an appropriate ac circulating current, which counteracts the dc power flow and makes the arm average power zero. In this way, the capacitors voltages can be kept balanced. The dc part regulates the dc power flow. By dividing the reference voltage by the nominal voltage of the arm V_{dc2}, the modulations signals of the upper and lower arms, m_u and m_l, are found.

$$m_u = (1 - D) + m_{ac} \cos(\omega t + \varphi) \tag{6-7}$$

$$m_l = (D) + m_{ac}\cos(\omega t) \tag{6-8}$$

in which D is the conversion ratio and equals to V_{dc1}/V_{dc2}. The ac modulation signal is shown by m_{ac}. Using the modulation signals, the arms modulated voltages are found as

$$\begin{aligned} v_u = (1-D)V_{dc2} + \frac{1}{2}m_{ac}\,v_{cu}\cos(\varphi - \theta_{cu}) \\ +(1-D)\,v_{cu}\cos(\omega t + \theta_{cu}) + m_{ac}\,V_{dc2}\cos(\omega t + \varphi) \\ +\frac{1}{2}m_{ac}\,v_{cu}\cos(2\omega t + \varphi + \theta_{cu}) \end{aligned} \tag{6-9}$$

$$\begin{aligned} v_l = DV_{dc2} + \frac{1}{2}m_{ac}\,v_{cl}\cos(\theta_{cl}) \\ +D\,v_{cl}\cos(\omega t + \theta_{cl}) + m_{ac}\,V_{dc2}\cos(\omega t) \\ +\frac{1}{2}m_{ac}\,v_{cl}\cos(2\omega t + \theta_{cl}) \end{aligned} \tag{6-10}$$

As can be seen, the arms modulated voltages have a second-order harmonic, which is ignored in this study. The two terms associated with the first-order harmonic of v_u and v_l are denoted by $v_{u,ac}$ and $v_{l,ac}$ in the rest of the chapter.

6.1.2 Arms Currents

The arms currents are approximated by the dc and first-order harmonics, as presented in (6-11). The dc component enables power exchange between the dc-links, and the ac circulating current is induced to balance the capacitors voltages. The dc and ac components are calculated for both arms of phase-leg 1 in the following.

$$i_{tj} = I_{jt,dc} + \hat{i}_{jt,ac}\cos(\omega t + \theta_{t,ac}) \tag{6-11}$$

6.1.2.1 AC Circulating Current

If the controllers work properly and the capacitors voltages are balanced, the generated voltage by each arm can be considered an independent voltage source in the steady-state. Because by changing the modulation signal, the arm voltage can be regulated at any value in the acceptable range. Assuming that the dc-links voltages are perfectly tuned at the nominal values by the host

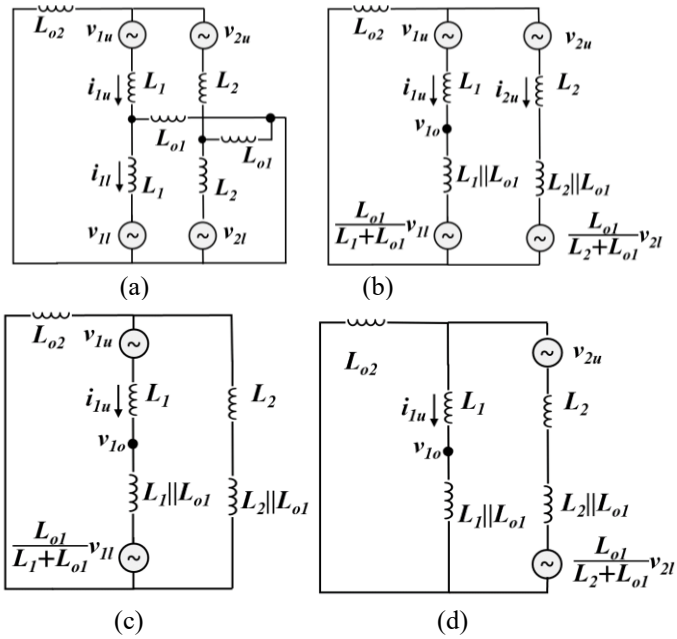


Figure 6-2 (a) ac equivalent circuit of a dc/dc MMC with two phase-legs considering the dc-link 2 inductance, (b) Simplified ac circuit, (c) ac circuit ignoring the ac voltage sources of phase-leg 2, (d) ac circuit ignoring the ac voltage sources of phase-leg 1.

dc system, the equivalent ac circuit of the system is presented in Figure 6-2(a) and (b), where L_{o2} accounts for the dc-link 2 inductance, including the line inductance and the current limiting inductor. In short transmission lines, the π model can be approximated by an inductor. This assumption also helps to present the equations in a more comprehensible way. These inductances are ignored in the dc-link 1 because the equivalent inductance of dc-link 1 can be ignored in front of the large phase inductance L_{o1}. For the sake of simplicity, only the arms ac currents in phase-leg 1 are calculated here. In the previous studies [25], by ignoring the dc-link 2 inductance, the ac currents in the phase-leg 1 ($i_{1u,ac}$ and $i_{1l,ac}$) are only stemmed from the phase-leg 1 ac voltages ($v_{1u,ac}$, $v_{1l,ac}$), and the operation of the phase-legs in one converter is considered completely independent. However, as shown in Figure 6-2 (b), by considering the dc-link 2 inductance, $i_{1u,ac}$ is also affected by the arms ac voltages of the phase-leg 2. This means that the operation of the phase-legs is not independent anymore, and parameters of one phase-leg can impact the operation of the other phase-leg. To find $i_{1u,ac}$, first, it is defined as

$$i_{1u,ac} = i^1_{1u,ac} + i^2_{1u,ac} \tag{6-12}$$

where $i^1_{1u,ac}$ is the ac current stemmed from the ac voltages of phase-leg 1 and $i^2_{1u,ac}$ is resulted from the ac voltages of phase-leg 2. To calculate each component of $i_{1u,ac}$, the superposition theorem is used. First, the arms ac voltages of phase-leg 2 are ignored, and the ac current produced by the ac voltages of phase-leg 1 is calculated in (6-13). The equivalent circuit is shown in Figure 6-2 (c).

$$i^1_{1u,ac} = \frac{-1}{jx_{e1}}\left(v_{1u,ac} + \frac{x_{o1}}{x_{o1}+x_1}.v_{1l,ac}\right) \tag{6-13}$$

$$x_{e1} = x_1 + x_1||x_{o1} + x_{o2}||(x_2 + x_2||x_{o1}) \tag{6-14}$$

in which, $v_{1u,ac}$ and $v_{1l,ac}$ are the first harmonic of the arms modulated voltages in the phase-leg 1. x_{e1} shows the equivalent reactance from the phase-leg 1 perspective, and x_1 and x_2 are the arms reactances of phase-legs 1 and 2, respectively. The phase reactances of the phase-legs 1 and 2 are equal and denoted by x_{o1}. The equivalent reactance of the dc-link 2 is shown by x_{o2}. Similarly, to find the ac current stemmed from phase-leg 2, the arms ac voltages of phase-leg 1 are ignored, as shown in Figure 6-2 (d). $i^2_{1u,ac}$ as

$$i^2_{1u,ac} = \frac{a_1}{jx_{e2}}\left(v_{2u,ac} + \frac{x_{o1}}{x_{o1}+x_2}.v_{2l,ac}\right) \tag{6-15}$$

$$x_{e2} = x_2 + x_2||x_{o1} + x_{o2}||(x_1 + x_1||x_{o1}) \tag{6-16}$$

$$a_1 = \frac{x_{o2}}{x_{o2} + x_1 + x_1||x_{o1}} \tag{6-17}$$

where $v_{2u,AC}$ and $v_{2l,AC}$ are the first harmonic of the modulated voltages in the upper and lower arms of the phase-leg 2. x_{e2} shows the equivalent reactance from the phase-leg 2 perspective. Having $i^1_{1u,AC}$ and $i^2_{1u,AC}$, $i_{1u,AC}$ is obtained using (6-12). To find the lower arm ac current in the phase-leg 1, first, the voltage of the midpoint, v_{1o}, is calculated in (6-18). Then, the lower arm current is obtained by (6-19).

$$v_{1o,ac} = j(x_1||x_{o1}).i_{1u,ac} + \frac{x_{o1}}{x_{o1}+x_1}.v_{1l,ac} \tag{6-18}$$

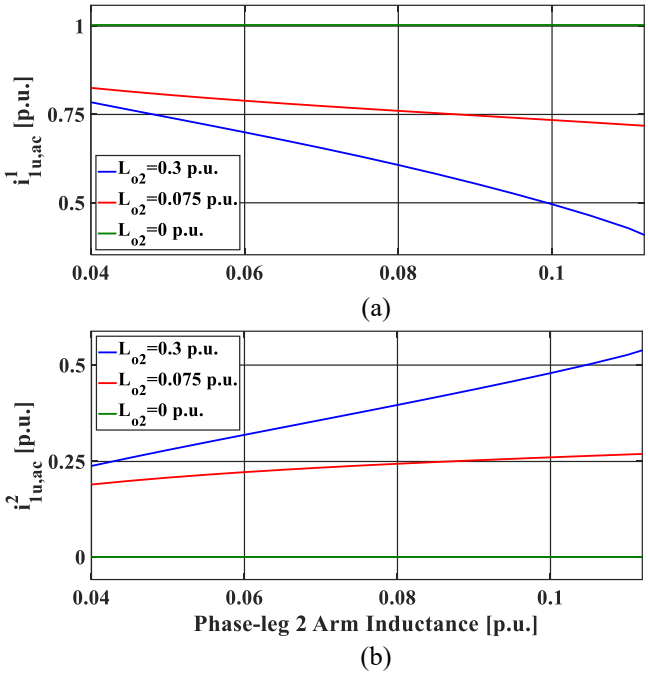


Figure 6-3 The ac current of the upper arm in the phase-leg 1 induced by the arms ac voltages of phase-leg 1 (self-induced), (b) The ac current of the upper arm in the phase-leg 1 induced by the arms ac voltages of phase-leg 2 (cross-coupling).

$$i_{1l,ac} = \frac{v_{1o,ac} - v_{1l,ac}}{jx_1} \tag{6-19}$$

The arms ac currents are calculated without ignoring x_1 relative to x_{o1}, which provides a more precise steady-state model.

To have a quantitative comparison, Figure 6-3 is presented showing the self-induced ac current $i^1_{1u,ac}$ and the cross-coupling ac current $i^2_{1u,ac}$ for various case studies. In this figure, the results are presented in p.u. to give the readers a general sense. The base values for the power and voltage are selected as 17 MW and 20 kV. While the arm inductance in phase-leg 1 is fixed at 0.08 p.u., the arm inductance in phase 2 is changing from 0.04 p.u. to 0.11 p.u. to emulate the unsymmetrical operation condition. Moreover, the results are presented for different values of the dc-link 2 inductance, 0.3 p.u., 0.075 p.u. and 0. As one can see, by increasing the dc-link 2 inductance, the cross-coupling current $i^2_{1u,ac}$ is increased, and the self-induced current $i^1_{1u,ac}$ is reduced. Similar observations are held when the arm inductance of phase-leg 2 increases. In general, the increase of the phase 2 arm inductance and the dc-link 2 inductance tighten the connection between the operation of the phase legs. As shown, when the dc-link 2 inductance

is zero, the cross-coupling current is zero indicating that the connection between the phase-legs is removed.

6.1.2.2 DC Component

If the dc/dc MMC transmits *P* amount of power from the dc-link 2 to the dc-link 1, the dc-links 1 and 2 currents would be equal to P/V_{dc1} and P/V_{dc2}, respectively. Assuming an equal power-sharing between the two phase-legs, the dc component of phase-legs output currents, $I_{1o,dc}$ and $I_{2o,dc}$, can be calculated by

$$I_{1o,dc} and\ I_{2o,dc} = P\left(\frac{1}{2.V_{dc1}}\right) \tag{6-20}$$

To accommodate power transmission from dc-link 2 to dc-link 1, two conditions stated in following should be satisfied,

$$I_{1o,dc} = I_{1u,dc} - I_{1l,dc} = I_{2u,dc} - I_{2l,dc} \tag{6-21}$$

$$I_{2,dc} = I_{1u,dc} + I_{2u,dc} = I_{1l,dc} + I_{2l,dc} \tag{6-22}$$

where $I_{1u,dc}$ and $I_{1l,dc}$ are the dc components of the upper and lower arms currents in the phase-leg 1 and $I_{2u,dc}$ and $I_{2l,dc}$ are the arms dc currents of phase-leg 2. As can be seen, by knowing one of the arms dc currents, the rest can be calculated. Therefore, $I_{1u,dc}$ is considered the only unknown, and the others are formulated based on it.

6.1.3 First Harmonic of the Sum of Capacitors Voltages

Using (6-3), the amplitude and the phase difference of the first harmonic in the sum of capacitors voltages can be obtained. Using (6-4), the left side of (6-3) is rewritten as

$$c^{\Sigma}.\frac{dv_{ct}^{\Sigma}}{dt} = -\omega.v_{ct}^{\Sigma}\sin(\omega t + \theta_{ct}) \tag{6-23}$$

The right-side of (6-3) is found using (6-7), (6-8), and (6-11), in which the simplified equations are shown in the following

$$m_{1u}.i_{1u} = (1-D)I_{1u,dc} + 0.5\,m_{ac1}\hat{i}_{1u,ac}\cos(\varphi_1 - \theta_{1u,ac}) \\ (1-D)\hat{i}_{1u,ac}\cos(\omega t + \theta_{1u,ac}) + m_{ac1}I_{1u,dc}\cos(\omega t + \varphi_1) \\ +0.5\,m_{ac1}\hat{i}_{1u,ac}\cos(2\omega t + \varphi_1 + \theta_{1u,ac}) \tag{6-24}$$

$$m_{1l}.i_{1l} = I_{1l,dc} + 0.5\,m_{ac1}\hat{i}_{1u,ac}\cos(\theta_{1u,ac}) \\ \hat{i}_{1l,ac}\cos(\omega t + \theta_{1u,ac}) + m_{ac1}I_{1l,dc}\cos(\omega t) \\ +0.5\,m_{ac1}\hat{i}_{1l,ac}\cos(2\omega t + \theta_{1l,ac}) \tag{6-25}$$

Since the first harmonic of both right- and left-sides should be equal, the amplitude and phase difference of the first harmonic existing in the sum of capacitors voltages can be found based on system parameters.

6.1.4 Internal Stability Condition

For the converter to operate stably, the average absorbed power by each arm in one cycle should be zero. The instantaneous exchanged power by the arm-*t* can be found as

$$p_t = v_t.i_t \tag{6-26}$$

The moving average of arm power is calculated by

$$P_t = < v_t.i_t >_T \tag{6-27}$$

Using (6-9) and (6-10), the moving average power exchanged by the upper and lower arms of phase-leg 1 are calculated as

$$P_{1u} = (1-D)V_{dc2}I_{1u,dc} + 0.5m_{ac1}v^{\Sigma}_{c1u,ac}I_{1u,dc}\cos(\varphi_1 - \theta_{c1u}) \\ 0.5(1-D)v^{\Sigma}_{c1u}\,\hat{i}_{1u,ac}\cos(\theta_{c1u} - \theta_{1u,ac}) \\ 0.5m_{ac1}V_{dc2}\hat{i}_{1u,ac}\cos(\varphi_1 - \theta_{1u,ac}) \tag{6-28}$$

$$P_{1l} = DV_{dc2}I_{1l,dc} + 0.5m_{ac1}v^{\Sigma}_{c1l}I_{1l,dc}\cos(\theta_{c1u}) \\ 0.5Dv^{\Sigma}_{cl1}\,\hat{i}_{1l,ac}\cos(\theta_{c1l} - \theta_{1l,ac}) \\ 0.5m_{ac1}V_{dc2}\hat{i}_{1l,ac}\cos(\theta_{1l,ac}) \tag{6-29}$$

To find the converter parameters at each operating point in the steady-state, there exist eleven unknowns that are φ_1, $I_{1u,dc}$, v^{Σ}_{cu1}, v^{Σ}_{cl1}, θ_{c1u}, θ_{c1l}, φ_2, v^{Σ}_{cu2}, v^{Σ}_{cl2}, θ_{c2u}, θ_{c2l}. These variables can be calculated by solving (6-3) for the upper and lower arms of the phase-legs 1 and 2, and (6-28) and (6-29) for the phase-legs 1 and 2.

6.2 Simplified Model and Unsymmetrical Operation of the DC/DC MMC

6.2.1 Simplified Model

A simplified model is presented to shed light on the unsymmetrical operation of the dc/dc MMC. In this model, the first-order harmonic in the sum of the capacitors voltages is neglected. Therefore, the unknown variables of the system are reduced to φ_1, φ_2 and $I_{dc,1u}$. To find these variables, the average power of the arms must be zero, which means the absorbed energy via the dc current $P_{jt,dc}$ plus the absorbed energy via the ac current $P_{jt,ac}$ should be zero, as demonstrated in the following

$$P_{jt,dc} + P_{jt,ac} = 0 \tag{6-30}$$

The arms absorbed energy via the dc current is calculated by multiplying the dc part of arms modulated voltages by the dc component of arms currents as follow

$$P_{1u,dc} = (1 - D)V_{dc2}.I_{1u,dc} \tag{6-31}$$

$$P_{1l,dc} = DV_{dc2}.(I_{1u,dc} - I_{1o,dc}) \tag{6-32}$$

$$P_{2u,dc} = (1 - D)V_{dc2}.(I_{dc2} - I_{1u,dc}) \tag{6-33}$$

$$P_{2l,dc} = DV_{dc2}.(I_{dc2} - I_{1u,dc} - I_{1o,dc}) \tag{6-34}$$

As can be seen in the above equations, the dc part of arms currents is formulated based on $I_{dc,1u}$.

To find the active ac power exchanged by the arms via the ac circulating current, the modulated voltages are needed to be simplified as

$$v_{1u} = (1 - D)V_{dc2} + v_{ac1}\cos(\omega t + \varphi_1) \tag{6-35}$$

$$v_{1l} = DV_{dc2} + v_{ac1}\cos(\omega t) \tag{6-36}$$

$$v_{2u} = (1 - D)V_{dc2} + v_{ac2}\cos(\omega t + \varphi_2 + \pi) \tag{6-37}$$

$$v_{2l} = DV_{dc2} + v_{ac2}\cos(\omega t + \pi) \tag{6-38}$$

where v_{ac1} and v_{ac2} show the arms ac voltages of the phase-legs 1 and 2. By multiplying the arms currents by the modulated voltages, the arms active ac powers are found as

$$P_{1u,ac} = P_{1u,ac}^{1l} + P_{1u,ac}^{2l} + P_{1u,ac}^{2u} \tag{6-39}$$
$$= \frac{1}{jx_{e1}} v_{ac1}^2 \sin(\varphi_1) + \frac{a_1}{jx_{e2}} v_{ac1} v_{ac2} (\sin(\varphi_1) - \sin(\varphi_2 - \varphi_1))$$

$$P_{1l,ac} = P_{1u,ac}^{1u} + P_{1u,ac}^{2u} \tag{6-40}$$
$$= \frac{-1}{jx_{e1}} v_{ac1}^2 \sin(\varphi_1) - \frac{a_1}{jx_{e2}} v_{ac1} v_{ac2} \sin(\varphi_2)$$

$$P_{2u,ac} = P_{1u,ac}^{2l} + P_{1u,ac}^{1l} + P_{1u,ac}^{1u} \tag{6-41}$$
$$= \frac{1}{jx_{e2}} v_{ac2}^2 \sin(\varphi_2) + \frac{a_2}{jx_{e1}} v_{ac1} v_{ac2} (\sin(\varphi_2 - \varphi_1) + \sin(\varphi_2))$$

$$P_{2l,ac} = P_{1u,ac}^{2u} + P_{1u,ac}^{1u} \tag{6-42}$$
$$= \frac{-1}{jx_{e2}} v_{ac2}^2 \sin(\varphi_2) - \frac{a_2}{jx_{e1}} v_{ac1} v_{ac2} \sin(\varphi_1)$$

$$a_2 = \frac{x_{o2}}{x_{o2} + x_2 + x_2 || x_{o1}} \tag{6-43}$$

where the superscript jt refers to the arm that the active power is generated because of its ac voltage. For example, $P_{ac,1u}^{2l}$ refers to the power that the upper arm of phase-leg 1 absorbs via the generated ac current by the lower arm ac voltage of phase-leg 2. As one can see, the arms of the phase-legs 1 and 2 can exchange active ac power. These new terms in the active ac power appear because the high-voltage side inductance is taken into account. Unlike the developed model in [25], the presented model in this chapter shows the connection between the operation of the phase-legs. As can be seen in (6-39)-(6-42), by assuming $x_{o2} = 0$, the equations would be transformed to the developed steady-state model in [25].

By looking at the obtained equations, it can be understood that (6-39)-(6-42) and (6-31)-(6-33) are independent equations. By solving (6-30) for the upper and lower arms of phase-leg 1 and

the upper arm of phase-leg 2, the three unknown variables of the system, φ_1, φ_2 and $I_{dc,1u}$, can be calculated at each operating point in the steady-state.

6.2.2 Simplified Model for a DC/DC MMC with N-Phase-Legs

To conduct the same analysis on a dc/dc MMC with *N* phase-legs, first, the ac equivalent circuit of the converter should be derived. Then the arms ac currents should be found considering the dc-link 2 impedance. The obtained arms ac currents would have terms associated with all the arms ac voltages. The dc currents can also be formulated in the same way as presented in (6-21) and (6-22). Having the arms currents, the exchanged power via the ac and dc currents can be found. In a dc/dc MMC with *N* number of phase-legs, there exist *N* phase differences and *N*-1 arms dc currents as the system unknowns. In total, the system will have 2*N*-1 unknowns, which can be found by solving the internal stability condition (6-30) for 2*N*-1 arms.

6.2.3 Symmetrical Operation

In this study, the symmetrical operation is referred to the condition that all the parameters involved in the ac power exchange are the same in the phase-legs of the dc/dc MMC. In this sense, the phase-legs operate with the same phase difference φ and the same amplitude of arm ac voltage v_{ac}. As a result, (6-39)-(6-42) can be reduced to

$$P_{ac,jt} = \frac{(1+a)}{jx_e} v_{ac}^2 \sin(\varphi) \quad \text{while } a = a_1 = a_2 \tag{6-44}$$

By simplifying $\frac{(1+a)}{x_e}$ to $\frac{1}{2x}$, (6-44) would be the same as the equation presented for the active ac power in [25]. Therefore, when the converter is in the symmetrical operation mode, the operation of the phase-legs can be considered independent. In this condition, each arm processes an equal amount of power.

6.2.4 Unsymmetrical Operation

This condition happens when the parameters involved in the exchange of ac power are not equal in the phase-legs of the dc/dc MMC. As one can see in (6-39)-(6-42), the arm inductance and the arm ac voltage are the main parameters involved in the generation of the ac power.

Table 6-I
Main Parameters of the Simulated System

Converter Parameters	Symbol	Value
Rated Power	P	17 MW
DC-Link1	V_{DC1}	14 kV
DC-Link2	V_{DC2}	20 kV
Arm Inductance	L	0.8 mH
Phase Inductance	L_0	0.26 H
DC-link 2 Current Limiting	L_d	4 mH
SM Capacitance	C	10 mF
SM Nominal Voltage	V_{CN}	2 kV
Operating Frequency	f_S	360 Hz
Number of Upper Arm	n_u	10
Number of Lower Arm SMs	n_d	10
DC-link 2 Line Inductance	l	0.5 mH/km
DC-link 2 Line Resistance	r	0.036 Ω/km
DC-link 2 Line Capacitance	c	0.394

Therefore, even a small variation in these two parameters will put the converter in an unsymmetrical operation. In this condition, the phase-legs operate with different phase differences (φ_1 and φ_2), and the exchanged ac power by the arms are formulated in (6-39)-(6-42). As one can see, the operation of phase-legs 1 and 2 are tightly connected. Therefore, to find the parameters of the converter in the steady-state, the internal stability condition (6-30) must be solved for the phase-legs 1 and 2 at the same time. It can be concluded that in the unsymmetrical condition, the operations of phase-legs 1 and 2 are not independent, and the previously developed model cannot fully show the behavior of the converter in the steady-state.

6.3 Verification of the Developed Steady-State Models

To verify the presented steady-state models, a dc/dc MMC with two phase-legs is simulated in the MATLAB/Simulink environment. In the simulated system, the dynamic of the dc-links voltage sources is ignored, and they are considered as the fixed dc sources. The main parameters of the converter are designed based on [25], as exhibited in Table 6-I. For the control of the converter, the closed-loop control presented in [24] and the sorting algorithm proposed in [5] are used. The verification process is carried out in two case studies that focus on the unsymmetrical operation of the dc/dc MMC. In these two case studies, the converter is forced to operate unsymmetrically by varying the arm inductances and the arm ac voltage of

phase-leg 2. In each case, the obtained simulation results from the detailed and simplified models and the steady-state model presented in [25], which is referred to as the "Old Model," are compared.

6.3.1 Unsymmetrical Operation: Variation in Arm Inductances

In this case study, it is assumed that the arm inductances of phase-leg 1 are fixed at 0.8 mH, and the arm inductances of phase-leg 2 vary from 0.4 mH to 1.2 mH. The obtained results are shown in Figure 6-4, where the *x*-axis is the difference between L_1 and L_2 and normalized based on L_1. For example, the *x*-axis at -12.5 % means that L_2 is 12.5% less than L_1, which equals 0.7 mH. In Figure 6-4(a), the upper arm dc current is shown. As can be seen, the obtained dc current from the developed models and the simulation studies increase as L_2 increases. Whereas the dc current in the old model is fixed at 425 A. The leaked ac circulating current into dc-link 2 is presented in Figure 6-4(b), where it increases whenever the L_2 deviates from L_1. This leakage occurs because the summation of the upper arms ac currents (phase-leg 1 and 2) is not zero in the unsymmetrical operation. The phase differences of phase-legs 1 and 2 are illustrated in Figure 6-4(c) and (d). As L_2 increases, the obtained φ_1 from the simplified and detailed models decreases following the simulation results. However, φ_1 from the old model remains unchanged despite an increase in L_2. All the obtained φ_2 increases in response to an increase in L_2; however, the result from the detailed model is the best one that tracks the simulation results. The first-order harmonic of the sum of capacitors voltages is shown in Figure 6-4(e), which confirms the precision of the detailed model. In summary, it is observed that the old model ignores the correlation between the operation of the phase-legs. However, the developed models in this chapter and the simulation results confirm that variation in the arm inductance influences the steady-state operating point of the converter and heavily impacts the operation of phase-leg 1.

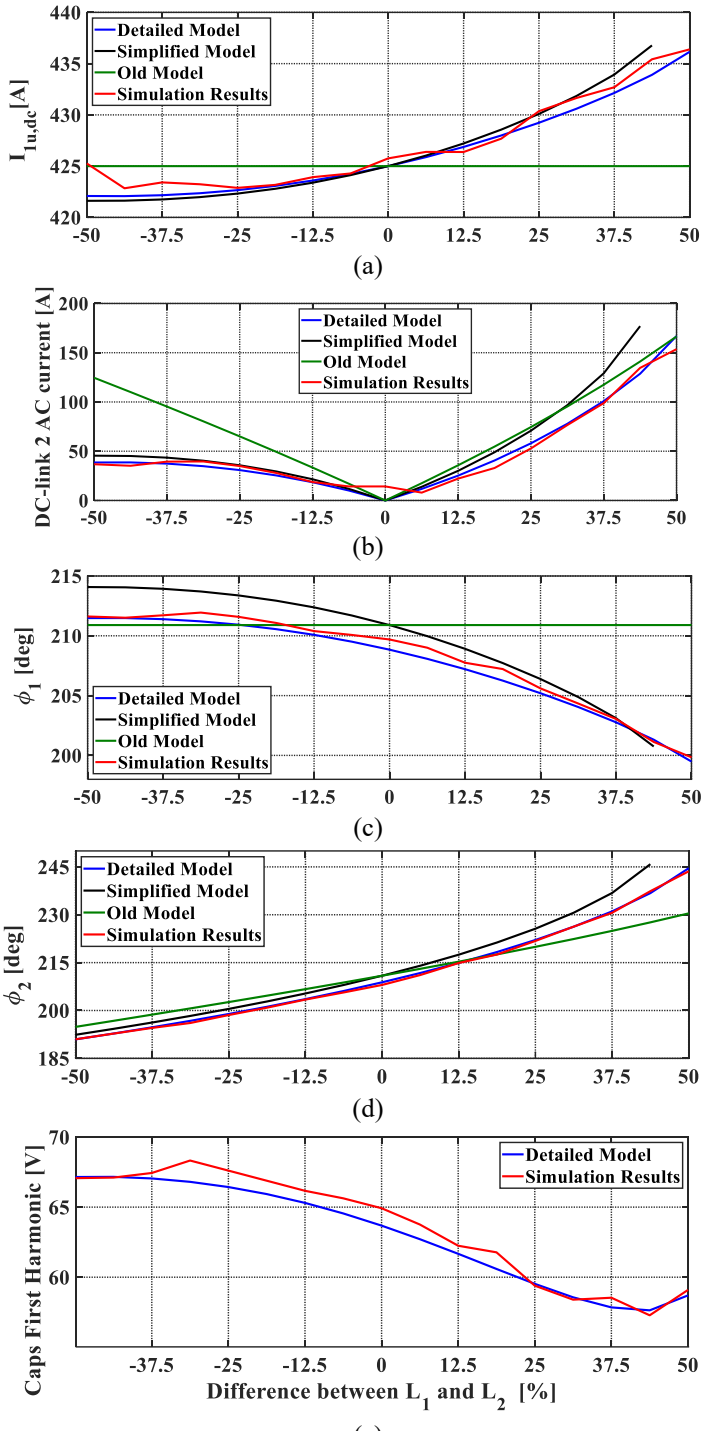


Figure 6-4 Simulation results of unsymmetrical operation of the dc/dc MMC with different arm inductances, (a) the upper arm dc component, (b) the leaked ac current into dc-link 2, (c) the phase-difference of phase-leg 1, (d) the phase-difference of phase-leg 2, (e) the first order harmonic of sum capacitors voltages.

6.3.2 Unsymmetrical Operation: Variation in Arm AC Voltage

In this case, it is assumed that the arm ac voltage of the phase-leg 1 is fixed at the maximum value, which is 6 kV, and the arm ac voltage of the phase-leg 2 varies from 6 kV to 5.22 kV. This situation can happen due to controller malfunction or SMs faults. The results are exhibited in Figure 6-5. The upper arm dc current is shown in Figure 6-5(a), where the dc currents obtained from the detailed and simplified models and the simulation studies increase in response to the decrease of the v_{ac2}. The old model yields to a fixed upper arm dc current in the whole range of the v_{ac2}. In Figure 6-5(b), the leaked ac current into the dc-link 2 is illustrated. All the obtained results have the same trend with respect to v_{ac2}. However, the detailed model follows the simulation results with higher precision. In Figure 6-5 (c) and (d), the phase differences of phase-legs 1 and 2 are presented. As shown, obtained φ_1 from the developed models and the simulation studies decrease when v_{ac2} is reduced, whereas the old model results in a fixed phase difference. All the obtained φ_2 show the same behavior in response to a decrease of v_{ac2}. However, the detailed and simplified models can follow the simulation results with higher accuracy. Finally, the first-order harmonic of the sum of capacitors voltages obtained from the detailed model is compared with the simulation results in Figure 6-5(e), which confirms the precision of the presented model. Like the previous case study, the old model sees the operation of the phase-legs as completely independent. The results from the developed models follow the simulation results showing the connection between the two phase-legs.

6.3.3 Maximum Tolerable Variation of the Parameters

Each of the compared models tolerates a degree of variation in the parameters, the arm inductance, and the arm ac voltage. In this sense, the converter can continue its operation up to a certain amount of parameter variation. One important observation made from Figure 6-4 is that the converter would face an operational problem when the arm inductances of phase-leg 2 increase to values larger than the nominal inductance. Otherwise, the only problem is the leaked ac current into the dc-link 2. Therefore, the maximum tolerable variation of the arm inductance ΔL_{max} is referred to the maximum normalized deviation that the arms inductances of phase-leg 2 can make from the nominal value $L_{arm\,,nom}$ while the converter is still able

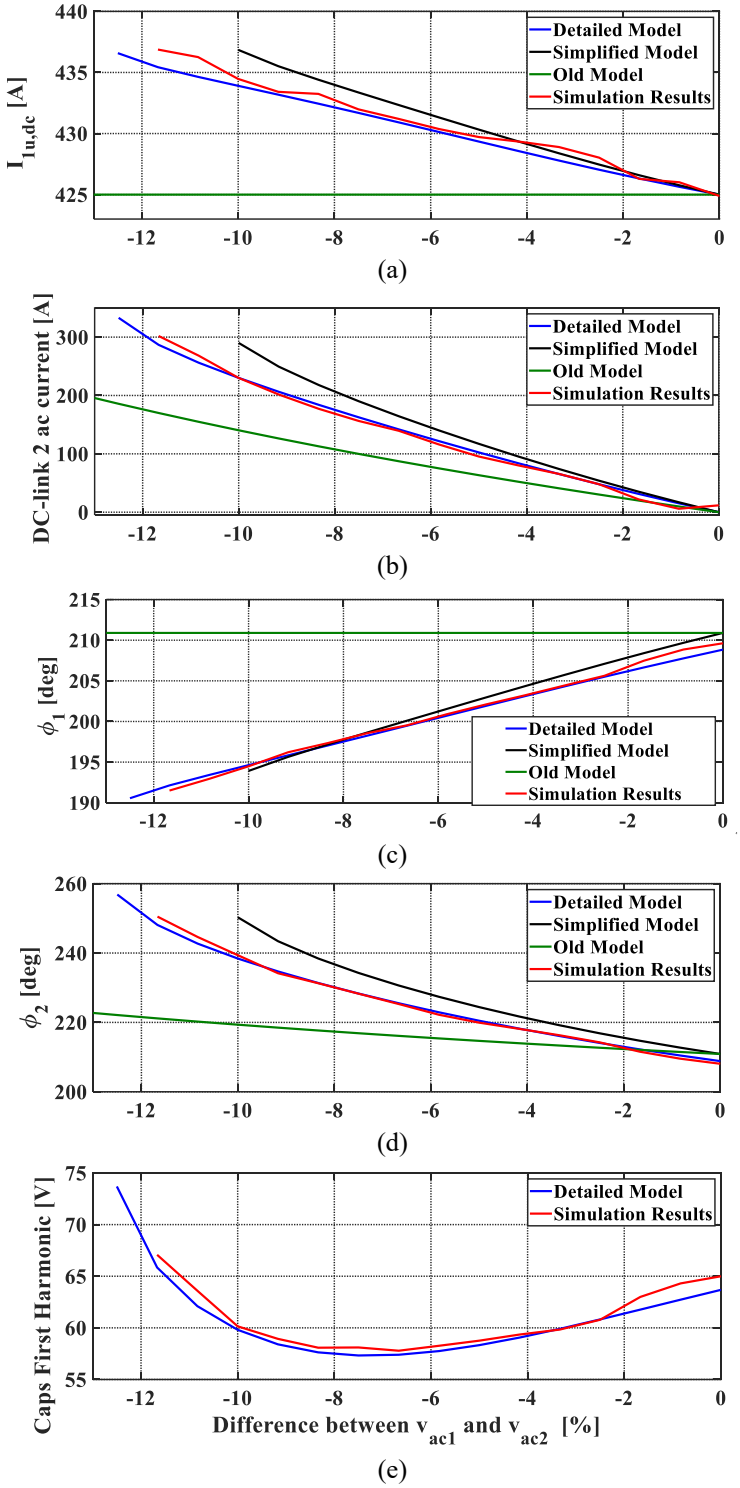


Figure 6-5 Simulation results of unsymmetrical operation of the dc/dc MMC with different arm voltages, (a) the upper arm dc component, (b) the leaked ac current into dc-link 2, (c) the phase-difference of phase-leg 1, (d) the phase-difference of phase-leg 2, (e) the first-order harmonic of the sum of capacitors voltages.

Table 6-II
The Maximum Tolerable Variation of Parameters

	Detailed Model	**Simplified Model**	**Old Model**	**Simulation Results**
ΔL_{max}	50 %	43.75 %	93 %	50 %
Δv_{max}	-12.5 %	-10 %	-28 %	-11.6 %

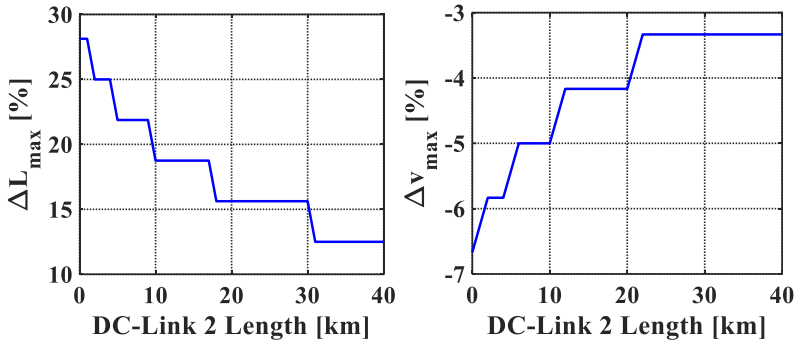
to operate. Similarly, the maximum tolerable variation of arm ac voltage Δv_{max} is referred to the maximum normalized deviation, which the arm ac voltage of phase-leg 2 can make from the maximum arm ac voltage $V_{arm\,,max}$ while the converter is still operational. ΔL_{max} and Δv_{max} can be calculated as

$$\Delta L_{max} = \frac{L_{2\,,max} - L_{arm\,,nom}}{L_{arm\,,nom}} \times 100 \tag{6-45}$$

$$\Delta V_{max} = \frac{v_{2\,,min} - V_{arm\,,max}}{V_{arm\,,max}} \times 100 \tag{6-46}$$

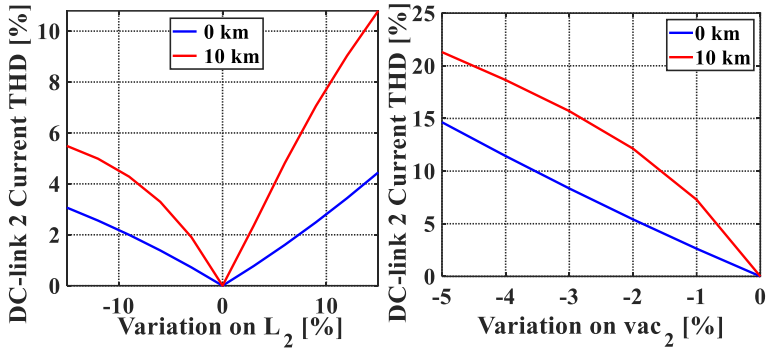
where $L_{2\,,max}$ is the maximum operational arm inductance of the phase-leg 2 and $v_{2\,,min}$ is the minimum operational arm ac voltage of phase-leg 2. Since the converter already operates with the maximum arm ac voltage, it is assumed that the arm ac voltage of phase-leg 2 can only decrease. The maximum tolerable variation of the parameters obtained from Figure 6-4 and Figure 6-5 is presented in Table 6-II. As expected, the old model [25] is not able to explain the behavior of the converter in unsymmetrical operation and resulted ΔL_{max} and Δv_{max} are far from the simulation results. However, the obtained results from the presented detailed and simplified models are close to the simulation results.

In the simulated cases of Figure 6-4 and Figure 6-5, ΔL_{max} and Δv_{max} are large enough so that the parameter variation would not jeopardize the operation of the converter. However, ΔL_{max} and Δv_{max} can be significantly reduced by different factors putting the normal operation of the converter in danger. The closed-loop control cannot help the converter in this situation. The problem is that the generated active ac power cannot cancel out the injected dc power by the arms in the whole range phase differences.



(a) (b)

Figure 6-6 The maximum tolerable variation of (a) the arm inductance and (b) the arm ac voltage, when the dc-link 2 length changes from 0 to 200 km.



(a) (b)

Figure 6-7 The dc-link 2 current THD (a) when variation of L_2 is between -15% to 15%, (b) when variation of v_{ac2} is between -5% to 0%, for the dc-link 2 lengths of 0 km and 10 km.

6.4 Effect of the System Parameters on the Unsymmetrical Operation

In general, three system parameters, which are elucidated in the following, can affect the unsymmetrical operation of the converter. In each case, the maximum tolerable variation of parameters and the leaked ac current into dc-link 2 are presented. The conducted studies are carried out on the dc/dc MMC detailed in Table 6-II. π model is used for the dc-link 2 transmission line, and the line parameters are extracted from [59]. All the results in this section are obtained from the presented detailed model.

6.4.1 DC-Link 2 Length

As the length of dc-link 2 increases, the equivalent inductance of the line increases. Therefore, the generated ac power in one phase-leg would be more affected by the other phase-leg (see

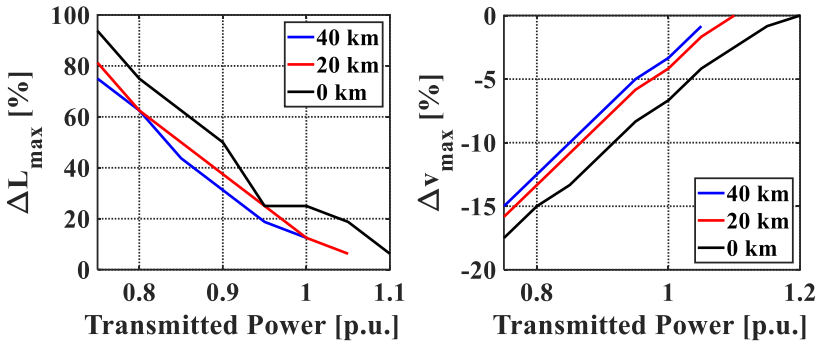
(38)-(41)). This situation aggravates the vulnerability of the converter operation against the parameter variation. For further investigation, the maximum tolerable variation of arm inductance and arm ac voltage are presented in Figure 6-6 (a) and (b), where the dc-link 2 length changes from 0 to 200 km. As shown, ΔL_{max} and ΔV_{max} are significantly reduced in long transmission lines. The threatening condition appears when ΔL_{max} is below 10% and ΔV_{max} is above -5 %, which means that even a very small difference between the arm inductances and ac voltages of the two phase-legs can stop the normal operation of the converter. On the other hand, when ΔL_{max} and ΔV_{max} are large enough, the parameters variation is not a big concern. In Figure 6-7 (a) and (b), the dc-link 2 current THD is presented for a small variation of the arm inductance and arm ac voltage. This study is carried out for dc-link 2 lengths of 0 km and 10 km. As shown, in longer dc-link 2, the ac current leakage into the dc-link 2 is more severe.

6.4.2 Transmitted Power

ΔL_{max} and Δv_{max} are illustrated in Figure 6-8(a) and (b) when the transmitted power changes from 0.75 p.u. to 1.2 p.u. In this study, the nominal power 17 MW is considered as 1 p.u. As can be seen, when the transmitted power by the dc/dc MMC reduces, ΔL_{max} and ΔV_{max} are both increased. This means the converter operating with less power is less sensitive to the parameters variation. The worst situation happens when the dc-link 2 is long, and the converter is required to operate with more than the nominal power. The dc-link 2 current THD with respect to the variation of arm inductance and arm ac voltage is shown in Figure 6-9(a) and (b), for the transmitted powers of 1.1, 1, and 0.9 p.u. As one can see, the dc/dc MMC is more sensitive to parameter variation when it transmits larger power. This is because the leaked ac current into dc-link 2 is higher for the converter transmitting larger powers.

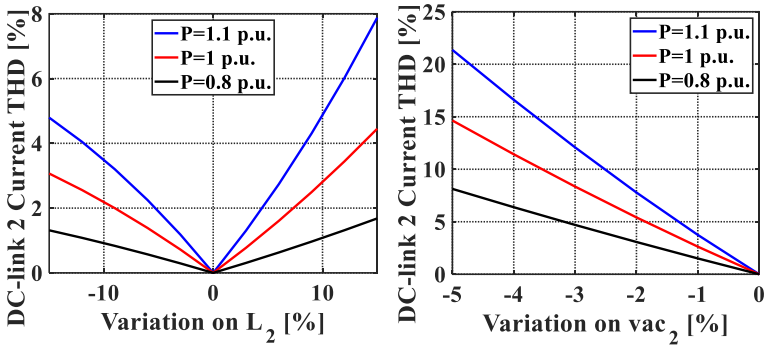
6.4.3 Conversion Ratio

To assess the effect of the conversion ratio, it is assumed that the dc link 2 voltage is fixed at 20 kV, and the dc-link 1 voltage changes to create converters with conversion ratios between 0.65 to 0.75. When the conversion ratio approaches 1, the available arm ac voltage would be smaller [24]. Therefore, the converter would be more sensitive to the parameters that affect the



(a) (b)

Figure 6-8 The maximum tolerable variation of (a) the arm inductance and (b) the arm ac voltage, when the transmitted power changes from 0.75 to 1.2 p.u..



(a) (b)

Figure 6-9 The dc-link 2 current THD (a) when variation of L_2 is between -15% to 15%, (b) when variation of v_{ac2} is between -5% to 0%, for the transmitted powers of 1.1 p.u., 1 p.u. and 0.8 p.u..

ac power generation. As shown in Figure 6-10(a) and (b), the converter with a larger conversion ratio has a smaller ΔL_{max} and ΔV_{max}. The dc-link 2 current THD is illustrated in Figure 6-11(a) and (b), for the conversion ratios of 0.6, 0.65, and 0.7. As shown, the leaked ac current is always higher in the cases with larger conversion ratios confirming the higher sensitivity to the parameter variations.

6.5 Summary

This chapter developed detailed and simplified steady-state models that can fully show the behavior of the dc/dc MMC in the unsymmetrical condition. These models were developed by taking the dc-link impedance into account, where the connection between the phase-legs becomes apparent. Using the developed models, variation in the arm inductance and the arm ac voltage were identified as the main reasons for putting the converter in the unsymmetrical condition. The obtained results confirmed the capability of the developed models in the

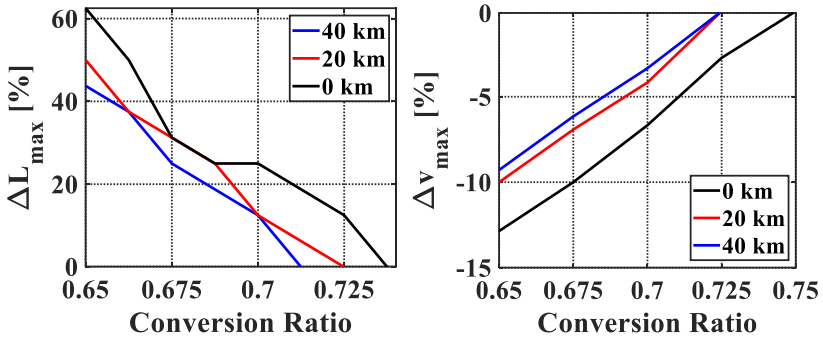


Figure 6-10 The maximum tolerable variation of (a) the arm inductance and (b) the arm ac voltage, when the conversion ratio changes from 0.65 to 0.75.

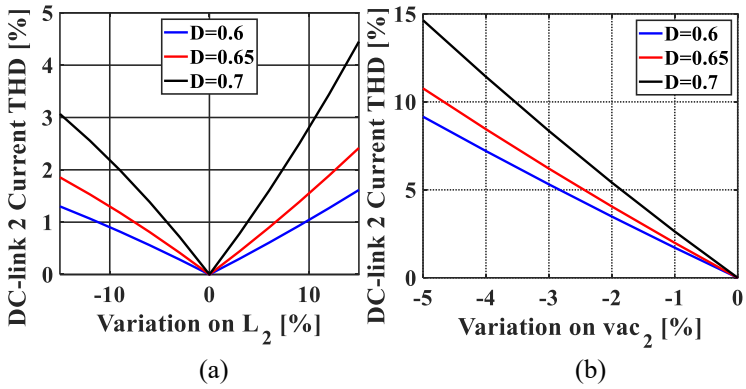


Figure 6-11 The dc-link 2 current THD (a) when variation of L_2 is between -15% to 15%, (b) when variation of v_{ac2} is between -5% to 0%, for conversion ratios of 0.6, 0.65 and 0.7.

illustration of the unsymmetrical operation. The maximum tolerable variation of the arm inductance and the arm ac voltage and the leaked ac current into the dc-link 2 were found in cases with different dc-link 2 lengths, transmitted powers, and conversion ratios. The following observations are obtained:

With an increase in the length of dc-link 2, the transmitted power and the conversion ratio all reduce the maximum tolerable variations of the arm inductance and the arm ac voltage. In other words, it aggravates the vulnerability of the converter operation against the parameter variation.

- When the maximum tolerable variation of the arm inductance is less than 15%, and this value for the arm ac voltage is less than 5%, it can jeopardize the operation of the converter. In this condition, the converter is very sensitive to the parameters so that a very small variation can stop the normal operation.

- The ac circulating current can leak into dc-link 2 even with a very small variation of the arm inductance and the arm ac voltage. This can distort dc-link 2 current and increase the system conduction loss.

Chapter 7 Model Predictive Control of the DC/DC MMC

This chapter presents the first MPC algorithm for the dc/dc MMC. First, the internal and external dynamic equations of the converter are extracted. Then, a new set of variables are introduced to decouple the equations, and by using the Forward Euler method, these equations are discretized. Then, using the developed equations, a tailored MPC approach is proposed for the control of the dc/dc MMC. The proposed MPC method is investigated in steady-state and transient modes. Finally, the simulation results are compared with those obtained from the conventional PI-based controller.

7.1 Dynamic Model

7.1.1 Currents and Voltages

By writing KVL equations in the dc-links 1 and 2 loops and from dc-link 2 to dc-link 1, the following dynamic equations are derived:

$$V_{DC1} - v_l + L_0 \frac{d}{dt}(i_u - i_l) - L \frac{d}{dt} i_l = 0 \tag{7-1}$$

$$V_{DC2} - v_u - v_l - L \frac{d}{dt}(i_u + i_l) = 0 \tag{7-2}$$

$$V_{DC2} - V_{DC1} - v_u - L_0 \frac{d}{dt}(i_u - i_l) - L \frac{d}{dt} i_u = 0 \tag{7-3}$$

As can be seen, in this study, the resistance of the arm and phase inductors is ignored. By subtracting (7-1) from (7-3), the following equation is obtained.

$$-V_{DC2} + 2V_{DC1} + v_u - v_l + 2L_{eq}\frac{d}{dt}(i_u - i_l) = 0 \tag{7-4}$$

In which L_{eq} is defined as $L_0 + \frac{L}{2}$. To have decoupled equations, a new set of variables are defined as

$$v_{diff} = \frac{v_u + v_l}{2} \tag{7-5}$$

$$v_s = \frac{v_u - v_l}{2} \tag{7-6}$$

$$i_{diff} = \frac{i_u + i_l}{2} \tag{7-7}$$

$$i_s = i_u - i_l \tag{7-8}$$

In which v_{diff} and v_s show the differential and output voltages, and i_{diff} and i_s are the differential and output currents. By replacing (7-5)-(7-8) in (7-2) and (7-4), the following equations can be derived.

$$L\frac{di_{diff}}{dt} = \frac{V_{DC2}}{2} - v_{diff} \tag{7-9}$$

$$L_{eq}\frac{di_s}{dt} = \frac{V_{DC2}}{2} - v_{DC1} - v_s \tag{7-10}$$

v_{diff}, v_s, i_{diff} and i_s have dc and ac parts just like the arms voltages and currents. To have control over the dc part of i_{diff} and i_s ($i_{diff,dc}$ and $i_{s,dc}$), the dc parts of variables in (7-9) and (7-10) can be separated from the ac parts, and these equations can be rewritten by the dc parts as:

$$L\frac{di_{diff,dc}}{dt} = \frac{V_{DC2}}{2} - v_{diff,dc} \tag{7-11}$$

$$L_{eq}\frac{di_{s,dc}}{dt} = \frac{V_{DC2}}{2} - v_{DC1} - v_{s,dc} \tag{7-12}$$

Using the Forward Euler equation, (7-11) and (7-12) can be discretized as

$$i_{diff,dc}(t+T_s) = i_{diff,dc}(t) + \frac{T_s}{L}\left(\frac{V_{DC2}}{2} - v_{diff,dc}(t)\right) \tag{7-13}$$

$$i_{s,dc}(t+T_s) = i_{s,dc}(t) + \frac{T_s}{L_{eq}}\left(\frac{V_{DC2}}{2} - V_{DC1} - v_{s,dc}(t)\right) \tag{7-14}$$

7.1.2 SMs Energies

The stored energies in each arm can be found using

$$\frac{dW_u}{dt} = v_u . i_u \tag{7-15}$$

$$\frac{dW_l}{dt} = v_l . i_l \tag{7-16}$$

Then, by defining sum and differential energies, W^{Σ} and W^{Δ}, in (7-17) and (7-18), (7-15) and (7-16) can be rewritten as demonstrated in (7-19) and (7-20).

$$W^{\Delta} = W_u - W_l \tag{7-17}$$

$$W^{\Sigma} = W_u + W_l \tag{7-18}$$

$$\frac{dW^{\Delta}}{dt} = p^{\Delta} = v_{diff} . i_s + 2v_s . i_{diff} \tag{7-19}$$

$$\frac{dW^{\Sigma}}{dt} = p^{\Sigma} = 2v_{diff} . i_{diff} + v_s . i_s \tag{7-20}$$

In which p^{Σ} and p^{Δ} are the sum and the differential instantaneous powers of the upper and lower arms. The sum and differential energies include dc and ac components. The ac parts of energies are caused by the capacitors voltages fluctuation around the nominal voltage. However, the dc parts are the control objectives in the dc/dc MMC, and they need to be controlled to ensure the capacitors voltages balance. In this sense, (7-19) and (7-20) are required to be rewritten by only dc components. To accomplish this, the ac components of

differential and output voltages and currents need to be found. From (7-5) and (7-6), the ac component of v_{diff} and v_s is formulated as:

$$v_{diff,ac}(t) = v_{ac}\cos\left(\frac{\varphi}{2}\right).\cos\left(wt+\frac{\varphi}{2}\right) \tag{7-21}$$

$$v_{s,ac}(t) = -v_{ac}\sin\left(\frac{\varphi}{2}\right).\sin\left(wt+\frac{\varphi}{2}\right) \tag{7-22}$$

Since the control of the sum and the differential energies are not meant to be fast, the ac component of differential and output currents can be calculated using steady-state equations in the phasor-domain as

$$\vec{i}_{diff,ac} = -\frac{\vec{v}_{diff,ac}}{jX_L} \tag{7-23}$$

$$\vec{i}_{s,ac} = -\frac{\vec{v}_{s,ac}}{jX_{eq}} \tag{7-24}$$

where X_L and X_{eq} denote the reactances of L and L_{eq}. (7-23) and (7-24) are derived by keeping only ac components in (7-9) and (7-10) and taking them to the phasor-domain. The ac currents can be reformulated in the time-domain as

$$i_{diff,ac}(t) = \frac{-v_{ac}}{X_L}\cos\left(\frac{\varphi}{2}\right).\cos\left(wt+\frac{\varphi}{2}-\frac{\pi}{2}\right) \tag{7-25}$$

$$i_{s,ac}(t) = \frac{v_{ac}}{X_{eq}}\sin\left(\frac{\varphi}{2}\right).\cos\left(wt+\frac{\varphi}{2}\right) \tag{7-26}$$

The dc part of p^{Σ} and p^{Δ} are the average powers, P^{Σ} and P^{Δ}, and can be calculated by

$$\frac{dw_{DC}^{\Delta}}{dt} = P^{\Delta} = v_{diff,dc}.i_{s,dc} + 2v_{s,dc}.i_{diff,dc} + \langle v_{diff,ac}.i_{s,ac}\rangle_{T_{sw}} + \langle 2v_{s,ac}.i_{diff,ac}\rangle_{T_{sw}} \tag{7-27}$$

$$\frac{dw_{DC}^{\Sigma}}{dt} = P^{\Sigma} = 2v_{diff,dc}.i_{diff,dc} + v_{s,dc}.i_{s,dc} \tag{7-28}$$

$$+\langle 2v_{diff,ac}.i_{diff,ac}\rangle_{T_{sw}} + \langle v_{s,ac}.i_{s,ac}\rangle_{T_{sw}}$$

where w_{DC}^{Δ} and w_{DC}^{Σ} are the dc parts of the differential and the sum energies and $\langle g\rangle_{T_{sw}}$ exhibits the average value of g over T_{sw} which is the switching period ($T_{sw} = \frac{1}{f}$). Using the obtained equations, $\langle v_{diff,ac}.i_{s,ac}\rangle_{T_{sw}}$ and $\langle 2v_{s,ac}.i_{diff,ac}\rangle_{T_{sw}}$ are found as

$$\langle 2v_{s,ac}.i_{diff,ac}\rangle_{T_{sw}} = \frac{v^2{}_{ac}}{2X_L}\sin(\varphi) \tag{7-29}$$

$$\langle v_{diff,ac}.i_{s,ac}\rangle_{T_{sw}} = \frac{v^2{}_{ac}}{4X_{eq}}\sin(\varphi) \tag{7-30}$$

Based on the obtained equations, it can be understood that between $v_{diff,ac}$ and $i_{diff,ac}$, and $v_{s,ac}$ and $i_{s,ac}$, there exists a 90-degree phase difference. Therefore, $\langle 2v_{diff,ac}.i_{diff,ac}\rangle_{T_{sw}}$ and $\langle v_{s,ac}.i_{s,ac}\rangle_{T_{sw}}$ are equal to zero. In the end, (7-27) and (7-28) are rewritten as

$$\frac{dw_{DC}^{\Delta}}{dt} = P^{\Delta} = v_{diff,dc}.i_{s,dc} + 2v_{s,dc}.i_{diff,dc} + \frac{v^2{}_{ac}}{4}\sin(\varphi)\left(\frac{1}{X_{eq}} + \frac{2}{X_L}\right) \tag{7-31}$$

$$\frac{dw_{DC}^{\Sigma}}{dt} = P^{\Sigma} = 2v_{diff,dc}.i_{diff,dc} + v_{s,dc}.i_{s,dc} \tag{7-32}$$

Using the Forward Euler equation, (7-31) and (7-32) can be discretized as

$$w_{DC}^{\Delta}(t+T_s) = w_{DC}^{\Delta}(t) + T_s.(v_{diff,dc}(t).i_{s,dc}(t) + 2v_{s,dc}(t).i_{diff,dc}(t) + \frac{v^2{}_{ac}(t)}{4}\sin\big(\varphi(t)\big)\,(\frac{1}{X_{eq}} + \frac{2}{X_L})) \tag{7-33}$$

$$w_{DC}^{\Sigma}(t+T_s) = w_{DC}^{\Sigma}(t) + T_s.(v_{s,dc}(t).i_{s,dc}(t) + 2v_{diff,dc}(t).i_{diff,dc}(t) \tag{7-34}$$

Equations (7-13), (7-14), (7-33), and (7-34) set up the discrete-time model of the dc/dc MMC.

7.2 Proposed MPC Method for the DC/DC MMC

From the developed discrete-time model, $i_{s,dc}$, $i_{diff,dc}$, w_{DC}^{Δ} and w_{DC}^{Σ} are the control objectives and $v_{s,dc}$, $v_{diff,dc}$ and φ are the control variables in the dc/dc MMC. To regulate each of them, first the control set should be found based on the existing error. Then, the control set, which minimizes the defined cost function, is selected as the optimum state.

7.2.1 Output Current

By looking at (7-14), it can be understood that the dc output current $i_{s,dc}(t+T_s)$ can be regulated by a proper value of dc output voltage $v_{s,dc}(t)$. In (7-14), V_{DC1} and V_{DC2} are constant values and the dc output current $i_{s,dc}(t)$ is measured from the circuit. At each time instant *t*, the control algorithm evaluates three different values of $v_{s,dc}$ including the current state $v_{s,dc}(t-T_s)$. The evaluated control set $V_{s,dc}(t)$ at time instant *t* is shown as

$$V_{s,dc}(t) = [v_{s,dc}(t-T_s) - \Delta v_{s,dc}(t), v_{s,dc}(t-T_s), v_{s,dc}(t-T_s) + \Delta v_{s,dc}(t)] \qquad (7\text{-}35)$$

where $\Delta v_{s,dc}(t)$ is the voltage step change at time instant *t* which is found by the control algorithm. Large values of $\Delta v_{s,dc}$ improve the dynamic performance, while small values enhance the steady-state performance. Therefore, an adaptive search step proposed in [45] is used. $\Delta v_{s,dc}(t)$ can be found by

$$\Delta v_{s,dc}(t) = \begin{cases} v_{s,dc}^{up} & \gamma_s . E_s(t) > v_{s,dc}^{up} \\ \gamma_s . E_s(t) & v_{s,dc}^{up} > \gamma_s . E_s(t) > v_{s,dc}^{lw} \\ v_{s,dc}^{lw} & \gamma_s . E_s(t) < v_s^{lw} \end{cases} \qquad (7\text{-}36)$$

where $v_{s,dc}^{up}$, $v_{s,dc}^{lw}$ are the upper and lower limits of $\Delta v_{s,dc}$, and γ_s is a constant which translates the dc output current error E_s into a meaningful output voltage. $E_s(t)$ is calculated by

$$E_s(t) = \frac{\left|i_{s,dc}(t) - i^*_{s,dc}\right|}{i^*_{s,dc}}, i^*_{s,dc} = \frac{P}{2V_{DC1}} \tag{7-37}$$

In which $i^*_{s,dc}$ is the dc output current reference of one phase-leg. $v^{up}_{s,dc}$, $v^{lw}_{s,dc}$ and γ_s are the design parameters which can be tuned to reach the desired steady-state and dynamic performances. Further explanation of the adaptive search step is not provided here, and it can be found in [45] and [60]. In this study, $v^{up}_{s,dc}$, $v^{lw}_{s,dc}$ and γ_s are selected as $0.1V_{DC2}$, $0.005V_{DC2}$ and $0.5V_{DC2}$.

To evaluate each control set, the following cost function $C_s(t)$ is designed.

$$C_s(t) = \left|i_{s,dc}(t + T_s) - i^*_{s,dc}\right| + \beta_s\left|v_{AC,max}(t + T_s) - v_{AC,ss}\right| \tag{7-38}$$

where β_s is a soft weighting factor. The first term regulates the dc component of output current. The second term improves the converter performance by maximizing the arm ac voltage during transient and steady states. Furthermore, it eliminates unnecessary changes in $v_{s,dc}$. Maximizing the arm ac voltage helps the controller to have better control over the differential energy, which will be discussed later. At each time instant *t*, $i_{s,dc}(t + T_s)$ is estimated by replacing each control set in (7-14). To find $v_{AC,max}(t + T_s)$, it is assumed that $v_{diff,dc}$ is equal to $\frac{V_{DC2}}{2}$, since from a control perspective, it should always be around $\frac{V_{DC2}}{2}$. The arms voltages, $v_{u,DC}$ and $v_{l,DC}$, are calculated using (7-5) and (7-6). Then $v_{AC,max}(t + T_s)$ is found from (5-1). For each control set, $C_s(t)$ is calculated, and the one minimizing the cost function is chosen. In this way,$v_{s,dc}(t)$ can be found.

7.2.2 Differential Current and Sum Energy

From (7-13), it can be understood that by choosing a proper $v_{diff,dc}$, the dc component of differential current can be regulated. Similar to the control of output current, the control sets $V_{diff,dc}(t)$ are defined as

$$V_{diff,dc}(t) = [v_{diff,dc}(t - T_s) - \Delta v_{diff,dc}(t), v_{diff,dc}(t - T_s), v_{diff,dc}(t - T_s) + \Delta v_{diff,dc}(t)] \tag{7-39}$$

where $v_{diff,dc}(t-T_s)$ is the current state. $\Delta v_{diff,dc}(t)$ is the search step and can be found by

$$\Delta v_{diff,dc}(t) = \begin{cases} \gamma_{diff}.E_{diff}(t) & \gamma_{diff}.E_{diff}(t) > v_{s,dc}^{lw} \\ v_{diff}^{lw} & \gamma_{diff}.E_{diff}(t) < v_{s,dc}^{lw} \end{cases} \quad (7\text{-}40)$$

where $v_{diff,dc}^{lw}$ is the lower limit of $\Delta v_{diff,dc}$, and γ_{diff} is a constant. As shown, unlike the control of output current, in the control of differential current, large steps are voided ($v_{diff,dc}^{up}$ is eliminated). Since the inductance path of the differential current (L) is very small, even a small deviation of $v_{diff,dc}$ from $\frac{V_{DC2}}{2}$ is enough to regulate $i_{diff,dc}$. In this study, $v_{s,dc}^{lw}$ and γ_s are selected as $10^{-5}V_{DC2}$ and $10^{-4}V_{DC2}$. $E_{diff}(t)$ is calculated in

$$E_{diff}(t) = \frac{\left|i_{diff,dc}(t) - i_{diff,dc}^{*}(t)\right|}{i_{diff,dc}^{*}} \quad (7\text{-}41)$$

In which $i_{diff,dc}^{*}$ is the differential current reference.

To evaluate each control set, the following cost function is defined.

$$C_{diff}(t) = \left|i_{diff,dc}(t+T_s) - i_{diff,dc}^{*}(t+T_s)\right| \quad (7\text{-}42)$$

At each time instant *t*, $i_{diff,dc}(t+T_s)$ is estimated for each control set using (7-13). The differential current reference in the next sampling period $i_{diff,dc}^{*}(t+T_s)$ can be defined so that the sum energy can be regulated. In this regard, (7-34) is written at time instant $t+T_s$ and $i_{diff,dc}(t+T_s)$ is formulated as

$$i_{diff,dc}(t+T_s) = \left(\frac{1}{2v_{diff,dc}(t+T_s)}\right)\left(\frac{w_{DC}^{\Sigma}\ (t+T_s) - w_{DC}^{\Sigma}\ (t+2T_s)}{T_s} + v_{s,dc}(t+T_s).i_{s,dc}(t+T_s)\right) \quad (7\text{-}43)$$

Since the control of sum energy should be slow, the dynamics of $v_{diff,dc}$ and $v_{s,dc}$ can be ignored. As a result, instead of $v_{diff,dc}(t+T_s)$ and $v_{s,dc}(t+T_s)$, the steady-state values, $\frac{V_{DC2}}{2}$

and $\frac{V_{DC2}}{2} - V_{DC1}$, are replaced in (7-43). $i_{s,dc}(t+T_s)$ is estimated by replacing the obtained $v_{s,dc}(t)$ in the previous stage in (7-14). $w_{DC}^{\Sigma}(t+T_s)$ is also estimated by replacing the steady-state values of $v_{diff,dc}(t)$ and $v_{s,dc}(t)$ and the measured values of $i_{s,dc}(t)$ and $i_{diff,dc}(t)$ in (7-34). $w_{DC}^{\Sigma}(t+2T_s)$ needs to be replaced with the reference value of w_{DC}^{Σ} at time instant $t+2T_s$. To find it, $w_{DC}^{\Sigma}(t+2T_s)$ can be formulated as

$$w_{DC}^{\Sigma}\ (t+2T_s) = \frac{T_s}{T_{sw}}\left(\sum_{k=0}^{\frac{T_{sw}}{T_s}-1} W^{\Sigma}\quad (t+2T_s-kT_s)\right) \tag{7-44}$$

$$= \frac{T_s}{T_{sw}}\left(\sum_{k=1}^{\frac{T_{sw}}{T_s}-1} W^{\Sigma}(t+2T_s-kT_s) + W^{\Sigma}(t+2T_s)\right.$$

As demonstrated in (7-44), $w_{DC}^{\Sigma}(t+2T_s)$ is split into two parts. The first part is the summation of W^{Σ} from the time instant $t+3T_s-T_{sw}$ to $t+T_s$. This term can be calculated using the estimated average sum energy $w_{DC}^{\Sigma}(t+T_s)$ as

$$\sum_{k=1}^{\frac{T_{sw}}{T_s}-1} W^{\Sigma}(t+2T_s-kT_s) = \left(\frac{T_{sw}}{T_s}-1\right).w_{DC}^{\Sigma}(t+T_s) \tag{7-45}$$

Equation (7-45) is derived using the fact that between time instants $t+3T_s-T_{sw}$ and $t+T_s$ the average sum of energy is $w_{DC}^{\Sigma}(t+T_s)$. Instead of $W^{\Sigma}(t+2T_s)$, the reference value, which is equal to $Nc(\frac{V_{DC2}}{N})^2$ is replaced. c shows the SM capacitance. In the end, the sum energy reference at time instant $t+2T_s$ is calculated by

$$w_{DC,ref}^{\Sigma}(t+2T_s) = \left(1-\frac{T_s}{T_{sw}}\right).w_{DC}^{\Sigma}(t) + \frac{T_s}{T_{sw}}Nc(\frac{V_{DC2}}{N})^2 \tag{7-46}$$

The defined sum energy reference pushes the sum energy towards the reference value at time instants $t+2T_s$. In this way, after some sampling period, the average sum energy will settle

down on the reference value $Nc(\frac{V_{DC2}}{N})^2$. This method lets the sum energy slowly approaches the reference value and prevents harsh transient and instability issues caused by fast changes in $v_{diff,dc}$. At the end of this stage, the dc differential voltage at the time instant-t $v_{diff,dc}(t)$ is found. Having $v_{s,dc}(t)$ and $v_{diff,dc}(t)$, the dc component of each arm voltage can be obtained. Then, the maximum ac voltage is found by (5-1), and it is used as the arm ac voltage for this switching cycle.

7.2.3 Differential Energy

By fixing the arm ac voltage at the maximum feasible value, the differential energy is regulated by the phase difference between the arms ac voltages. At each time instant, three different values of φ are evaluated. The control set $\Phi(t)$ is defined in

$$\Phi(t) = [\varphi(t - T_s) - \Delta\varphi(t), \varphi(t - T_s), \varphi(t - T_s) + \Delta\varphi(t)] \tag{7-47}$$

In which, $\varphi(t - T_s)$ is the current state. The search step $\Delta\varphi(t)$ is found based on the error of differential energy at time instant *t*. Since the process of finding $\Delta\varphi(t)$ is the same as output current, further explanation in this regard is avoided. In this study, $\varphi_{s,dc}^{up}$, $\varphi_{s,dc}^{lw}$ and γ_φ are selected as 0.1π, 0.001π, and 0.1π.

To evaluate each control set, the following cost function is defined.

$$C_{w^\Delta}(t) = \left|w_{DC}^{\Delta}(t + T_s) - w_{DC,ref}^{\Delta}(t + T_s)\right| + \beta_{w^\Delta}\left|\hat{\imath}_{diff,ac}(t + T_s)\right| \tag{7-48}$$

In (7-48), $w_{DC,ref}^{\Delta}(t + T_s)$ is the reference differential energy, and β_{w^Δ} is a soft weighting factor. $\hat{\imath}_{diff,ac}(t + T_s)$ denotes the ac circulating current. The first term in (7-48) controls the differential energy, and the second term tries to minimize the circulating current in the transient mode and the steady-state. $w_{DC}^{\Delta}(t + T_s)$ is estimated for each control set using (7-43). From (7-25), $\hat{\imath}_{diff,ac}(t + T_s)$ is derived as $\frac{v_{AC,max}}{X_L}\cos\left(\frac{\varphi(t)}{2}\right)$, and it is calculated for each control set. $w_{DC,ref}^{\Delta}(t + T_s)$ can be obtained by expanding $w_{DC}^{\Delta}(t + T_s)$ as follows:

$$w_{DC}^{\Delta}(t+T_s) = \frac{T_s}{T_{sw}} \sum_{k=1}^{\frac{T_{sw}}{T_s}-1} W^{\Delta}(t+T_s-kT_s) \tag{7-49}$$

$$= \frac{T_s}{T_{sw}} \left(\sum_{k=1}^{\frac{T_{sw}}{T_s}-1} W^{\Delta}(t+T_s-kT_s) + W^{\Delta}(t+T_s) \right)$$

The first term is calculated using the measured dc sum energy $w_{DC}^{\Sigma}(t)$ in (7-50). This equation is derived using the fact that between time instants t and $t+2T_s-T_{sw}$, the average differential energy is $w_{DC}^{\Delta}(t)$.

$$\sum_{k=1}^{\frac{T_{sw}}{T_s}-1} W^{\Delta}(t+T_s-kT_s) = \left(\frac{T_{sw}}{T_s}-1\right).w_{DC}^{\Delta}(t) \tag{7-50}$$

Instead of the second term in (7-49), the reference value of W^{Δ} is replaced, which is equal to zero. This is because, ideally, each arm should store an equal amount of energy. In the end, $w_{DC,ref}^{\Delta}(t+T_s)$ is formulated in

$$w_{DC,ref}^{\Delta}(t+T_s) = \left(\frac{T_{sw}}{T_s}-1\right).w_{DC}^{\Delta}(t) \tag{7-51}$$

By calculating $C_{w^{\Delta}}$ for each control set, the optimum phase-difference $\varphi(t)$ which minimizes the cost function is chosen.

7.2.4 Overall Control Diagram

As one can see in Figure 7-1, the presented MPC approach for the dc/dc MMC has three parts, the dc output current, the dc differential current, and the dc differential energy. The first control stage is the output current regulation. Using the measured $i_{s,dc}(t)$, the search step of the output -voltage is determined by (7-35), and then the control sets at time instant *t* are found by (7-36). The output current in the next sampling period $i_{s,dc}(t+T_s)$ is estimated by (7-14), and the cost function (7-38) is calculated for each of the control sets. The one minimizing the cost function

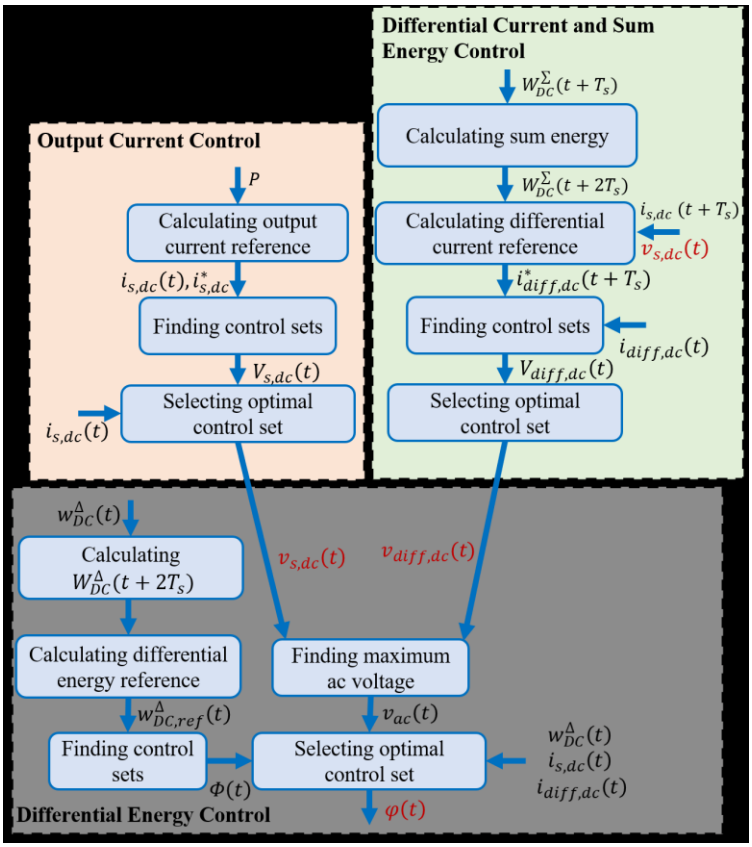


Figure 7-1 Overall flow chart of the proposed MPC of the dc/dc MMC.

is selected as the optimum output voltage $v_{s,dc}(t)$. In the control of dc differential current, the first task is to find the differential current reference $i_{diff,dc}(t+T_s)$ based on the sum energy using (7-43). The search step and control sets are calculated by (7-39) and (7-40). To find the optimum control set, the dc differential current in the next sampling period $i_{diff,dc}(t+T_s)$ is estimated by (7-13), and the cost function (7-42) is calculated for each control set. The one minimizing the cost function is selected as the optimum control set $v_{diff,dc}(t)$. After finding $v_{diff,dc}(t)$ and $v_{s,dc}(t)$, the maximum ac voltage $v_{AC,max}(t)$ is found using (5-1). At the same time, based on the measured dc component of differential energy, the control sets of phase-difference $\Phi(t)$ are found by (7-47). Finally, by estimating the differential energy by (7-33) and calculating the cost function (7-38), the optimum control set $\varphi(t)$ is determined.

The overall control diagram of the dc/dc MMC is demonstrated in Figure 7-2. As shown, a low-pass filter with a bandwidth of 100 Hz is used to extract the dc component of measured variables. The proposed MPC method uses the dc variables to determine the control parameters

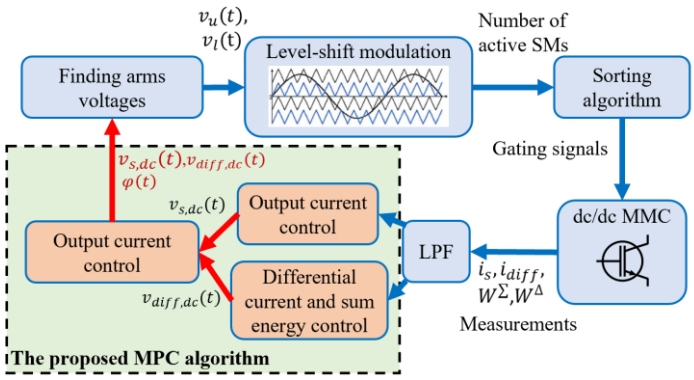


Figure 7-2 Overall control of the dc/dc MMC.

$v_{s,dc}(t)$,$v_{diff,dc}(t)$ and $\varphi(t)$. Using (7-5) and (7-6), the arms voltages at time instant-t are calculated. Then, using the level-shift PWM technique, the number of active SMs at the next sampling period in each arm is found. Finally, using the sorting algorithm proposed in [5], the switched-on and -off SMs are determined based on the capacitors voltages of SMs.

7.2.5 Time-Delay Compensation

So far, it is assumed that the system has no delay, and the calculated control voltages at time instant t can be applied instantaneously. However, in the real world, a time delay exists due to the A/D conversion delay, the calculation delay, and the zero-order-hold delay of the modulation process [61]. To account for the system delay, the calculated control voltages at time instant t must be applied at time instant $t + T_s$. The delay compensation is done using the method presented in [62]. An estimation step is added to the control algorithm, which is based on the known state of the system at time instant t. The system parameters are estimated at a time instant $t + T_s$. Then based on the estimated parameters, the control voltages are calculated for the time interval between $t + T_s$ and $t + 2T_s$. In this condition, the microprocessor have one sampling period T_s to calculate the control voltages.

7.2.6 Calculation Time [63-65]

To assess the computational efficiency of the proposed MPC algorithm, the calculation time of the MPC algorithm is found based on the calculation time of the basic mathematical operations. The number of cycles required for each mathematical operation is presented in Table 7-I [45].

Table 7-I
calculation Time of the Basic Mathematical Operations

Mathematical Operation	**Cycles**
Sum\Subtraction	1
Multiplication	1
Comparison	1
Assignment	1
Absolute	2

Table 7-II
Comparison of calculation Time

	Methods	**Calculation Time**
dc/ac MMC	Switching status based FCS-MPC [33]	$(5N+12).C_{2N}^{N}-1$
	Indirect FCS-MPC [34]	$161N^2+321N+160$
	Preselection based FCS-MMC [20]	$N^2+N+246$
	Modulated MPC based on the duty cycle [35]	$12N+160$
dc/dc MMC	Presented MPC method	$8N+169$

Using this Table, the calculation time of the proposed MPC algorithm is calculated. Because this chapter proposes the first MPC approach for the control of the non-isolated dc/dc MMC, there are no other MPC methods to be compared with. Therefore, the calculation time of the proposed approach is compared with the methods developed for the control of the dc/ac MMC in Table 7-II. As these two converters, the dc/dc MMC and the dc/ac MMC, share a lot of similarities (topology and control structure), this comparison can show how much the proposed MPC approach is computationally efficient. However, it is noteworthy that the operation principle, control objectives, and control variables are different in these two converters, which means the proposed MPC methods for the dc/ac MMC cannot be used directly for the dc/dc MMC. The presented calculation time is based on the number of SMs *N* and is calculated for one phase-leg. As can be seen, the proposed method has the lowest calculation time making it computationally efficient to be applied in large systems with hundreds of SMs.

Table 7-III
Parameters of the Simulated DC/DC MMC

Common Parameter	**Symbol**	**Value**
Nominal Power	P	15 MW
DC-Link1 Nominal Voltage	V_{DC1}	14 kV
DC-Link2 Nominal Voltage	V_{DC2}	20 kV
Arm Inductor	L	1.2 mH
Phase Inductor	L_0	0.26 H
SM Capacitor	C	7 mF
SM Rated Voltage	V_{CN}	2 kV
AC Voltage Frequency	f	360 Hz
Number of Arm HBSMs	n	10
Sampling Frequency	$f_s\ (1/T_s)$	10 kHz
Weighting Factors	**Symbol**	**Value**
Output Current Cost Function	β_s	0.00001
Differential Energy Cost Function	β_{w^Δ}	0.1
PI Parameters	**Symbol**	**Value**
Proportionl Gain of Power Balance Controller	-	10
Integral Gain of Power Balance Controller	-	200
Proportionl Gain of DC-link Current Regulator	-	10
Integral Gain of DC-link Current Regulator	-	50

7.3 Simulation Studies

To verify the effectiveness of the presented MPC approach, a dc/dc MMC with two phase-legs is simulated in MATLAB\Simulink. The dc sides of the converter are connected to an ideal voltage source for the sake of simplicity. In the first case study, the steady-state performance of the presented MPC approach is investigated and compared with the results of the PI-based controller [24]. In the second case study, the transient performance of both the presented MPC approach and the conventional PI-based controller is compared. The converter parameters and the control parameters of both the proposed MPC approach and the PI-based controller are exhibited in Table 7-III. In the developed MPC method, the designed cost functions have only one weighting factor associated with the secondary term. To find the weighting factors, they are initially set to zero. Starting from zero, the weighting factors are increased to improve the

converter performance. At some point, the regulation of the main control objective will be deteriorated because of the excessive increase of the weighting factor. Having this in mind, the soft weighting factors can be determined with try and error [66]. The optimum PI-controller parameters are found based on the process proposed in the original paper [24].

7.3.1 Case Study I: Steady-State

The results of the steady-state operation when the proposed MPC approach is employed are presented in Figure 7-3. In this case, the converter transmits the nominal power (15 MW). The dc-links currents (i_{DC1} and i_{DC2}) and the output current of phase-leg 1 (i_{1o}) are exhibited in Figure 7-3 (a). As shown, a small amount of ac current is leaked from the phase-leg 1 (see the waveform of i_{1o}). However, because there exists a 180-degree phase difference between the

output currents of the phase-legs 1 and 2, the leaked circulating currents from the phase-legs canceled out each other at the conjunction point, providing very smooth dc currents in the dc-links. The arms currents are depicted in Figure 7-3 (b), which have dc and ac parts. The dc components of arms voltages regulate the dc part, enabling transmission of dc power. The ac part is generated by the arms ac voltages, and it intends to offset the exchanged dc power in the arms. Figure 7-3 (c) presents the arms voltages. As shown, the lower arm has a higher dc voltage (14 kV), and this arm voltage varies from 8 kV to 20 kV in one fundamental period. The upper arm voltage changes from 0 to 12 kV. The dc part is equal to 6 kV. The amplitude of arm ac voltage is 6 kV, and this is the maximum possible value since the arms voltages are extended to the upper limit (20 kV) and the lower limit (0). The arms capacitors voltages are exhibited in Figure 7-3 (d) and 5(e). The SMs voltages of the lower arm fluctuate in a wider range compared to the SMs voltages of the upper arm. The results confirm the effectiveness of the presented MPC method in keeping the capacitors voltages balanced.

(a)

(b)

(c)

(d)

(e)

Figure 7-3 The steady-state operation of the proposed MPC approach, (a) the dc-links currents and the phase-leg 1 current, (b) the arms currents, (c) arms voltages, (d) the SMs voltages of the upper arm, (e) the SMs voltages of the lower arm.

Table 7-IV
Comparison of the PI controller and the Presented MPC Approach in the Steady-State

Parameters	Conventional PI Controller	Proposed MPC
THD of I_{DC1} [%]	0.05	0.03
THD of I_{DC2} [%]	0.03	0.07
THD of i_{1o} [%]	1.76	1.78
Amplitude of Circulating Current [A]	796.5	717
Conduction Loss [kW]	50.5	47.3
Switching Frequency [Hz]	Upper arm: 650	Upper arm: 630
	Lower arm: 880	Lower arm: 857
Switching Loss [kW]	15.4	14.9
Total Loss [kW]	65.9	62.1

To compare the steady-state operation of the proposed MPC with the PI-based controller, Table 7-IV is presented. In this Table, the switch loss characteristics are extracted from [50], and all the losses are calculated using the provided loss calculation model in MATLAB/Simulink [52] without considering the thermal effect. As can be seen, the THDs of dc-links 1 and 2 currents are very small for both approaches. The THD of the output current of phase-leg 1 for both methods is exhibited in Table 7-IV, confirming that these two approaches have almost the same performance. The amplitude of the circulating current in the proposed MPC method is smaller than the PI-based controller (10 % smaller). It shows that the proposed MPC is more capable of reducing the ac circulating current. Accordingly, the conduction loss is calculated for both cases. The converter controlled by the proposed MPC approach has less conduction loss than the converter controlled by the PI controller due to smaller ac circulating current. The switching frequency and switching losses are also calculated for both cases, showing that both approaches have almost the same switching losses. The obtained total loss confirms that the converter controlled by the proposed MPC approach operates more efficiently.

7.3.2 Case Study II: Transient Mode Performance

The main advantage of using the MPC method is the fast dynamic response. This scenario shows the ability of the proposed MPC approach to respond to severe transient conditions.

Initially, the converter transmits -15 MW. At t=0.3 s, the power reference of the converter changes to +15 MW. The simulation results of the presented MPC approach and the PI-based controller are illustrated in Figure 7-4 and Figure 7-5. The dc-links currents and the phase-leg 1 output currents are illustrated in Figure 7-4(a) and Figure 7-5(a). As shown, the proposed MPC approach offers a faster dynamic response compared to the PI-based controller. In the converter controlled by PI controller, the dc-link 1 current and the phase-leg 1 currents reach the steady-state after 81 ms. While, in the converter controlled by the proposed MPC approach, they get to the steady-state in 60 ms. Similar observations are hold for the dc-link 2 current. As it reaches the steady-state in 120 and 85 ms in the PI controller and the proposed MPC approach, respectively. As can be seen, the proposed MPC approach improved the dynamic response by more than 25 %. The improvement made in the dynamic response is not as expected from the MPC method. Because the external dynamic, i.e., the dc-links currents, heavily depend on the large phase-inductor. As a result, the dynamic response of dc-links currents is slow, and the MPC approach cannot further improve the dynamic response. The arms currents are presented in Figure 7-4(b) and Figure 7-5(b). The MPC method offers a smoother transient mode and a faster dynamic response. The arms voltages are presented in Figure 7-4(c) and Figure 7-5(c), where both methods show the same behavior in the transient phase. The SMs voltages are demonstrated in Figure 7-4 (d) and (e) and Figure 7-5 (d) and (e). As shown, in the proposed MPC approach, the dynamic response is much faster, and the overshoot of capacitors voltages is eliminated. This observation confirms that the presented MPC approach has better control over the sum and the differential energies than the PI-based controller.

(a)

(b)

(c)

(d)

(e)

Figure 7-4 PI-based controller in transient mode, (a) dc-links currents and the phase-leg 1 current, (b) arms currents, (c) arms voltages, (d) the SMs voltages of the upper arm, (e) the SMs voltages of the lower arm.

(a)

(b)

(c)

(d)

(e)

Figure 7-5 The proposed MPC in transient mode, (a) the dc-links currents and the phase-leg 1 current, (b) the arms currents, (c) arms voltages, (d) the SMs voltages of the upper arm, (e) the SMs voltages of the lower arm.

7.3.3 Case Study III: Parametric Uncertainty

In the power system, designed components may have $\pm 20\%$ tolerance because of aging, temperature stresses, radiation, and distorted operation [34], [35]. Therefore, the proposed MPC approach for the dc/dc MMC should tolerate a degree of parametric uncertainty. By looking at the obtained discrete model of the dc/dc MMC, two system parameters, the arm inductance, and the phase inductance can be found. Because the phase inductor is usually designed very large to filter the ac current, tolerance in this inductor is not impactful. However, variations in the arm inductance heavily influence the generation of the circulating current and the active ac power. Therefore, two different analyses are carried out to investigate the converter performance under parametric uncertainty. In the first one, the steady-state operation of the dc/dc MMC controlled by the proposed MPC approach is studied. In the second analysis, the transient response of both approaches, the PI controller and the proposed MPC, is compared when parametric uncertainty exists.

7.3.3.1 Sensitivity Analysis

In this analysis, four different scenarios are assumed while the arm inductance changes between 80 % and 120% of the nominal value. The main purpose of defining these scenarios is to find the worst situation that the parametric uncertainty can happen. Scenario 1 is defined when the parametric uncertainty happens in one of the arm inductances in phase-leg 1. Scenario 2 refers to the situation in which both arms inductance in phase-leg 1 have uncertainty. In scenario 3, in addition to the arm inductances of phase-leg 1, one of the arm inductances in phase-leg 2 also varies between 80 % and 120% of the nominal value. In scenario 4, the parametric uncertainty occurs in all the arm inductances.

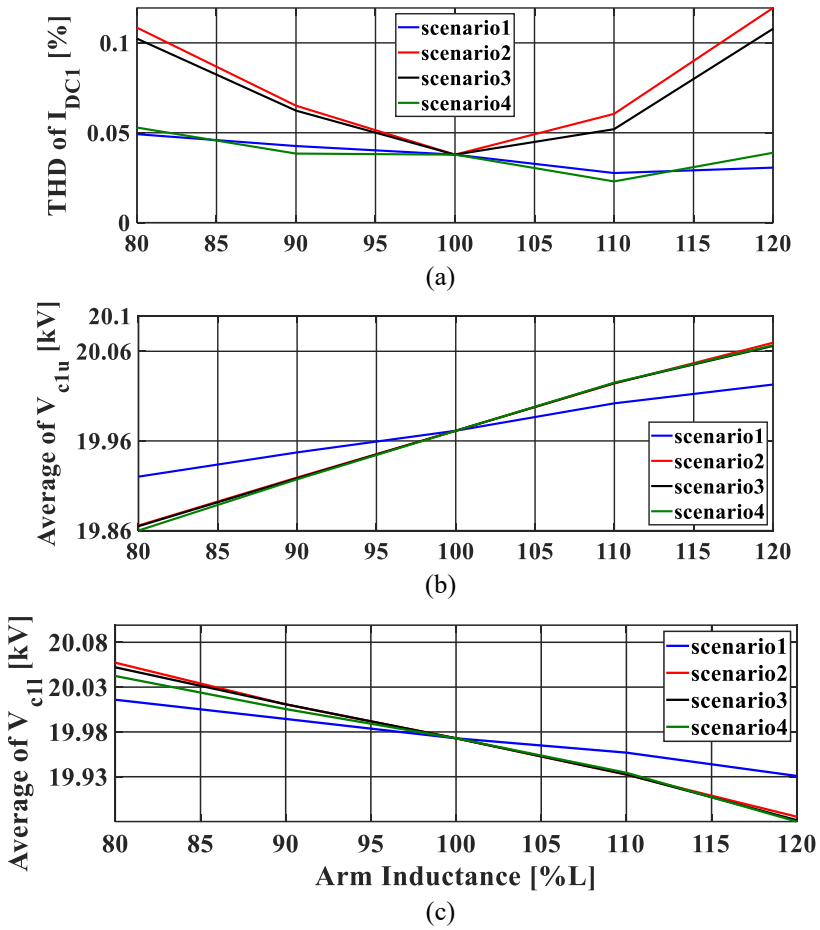


Figure 7-6 Sensitivity analysis, (a) THD of dc-link 1 current, (b) Average voltage of upper arm capacitors, (c) Average voltage of lower arm capacitors.

The results are illustrated in Figure 7-6. The THD of dc-link 1 current is found for all the scenarios as the arm inductance varies between 80% and 120% of the nominal value in Figure 7-6 (a). Scenario 2 has the worst current THD in the whole range of arm inductance. Scenarios 1 and 4 have almost the same current THD, which is the lowest among the defined scenarios. As can be seen, even in the worst condition, the THD of dc-link 1 current is less than 0.2% showing the satisfactory performance of the proposed MPC approach despite parametric uncertainty. In Figure 7-6 (b) and (c), the average voltage of upper arm capacitors and lower arm capacitors are exhibited. As can be seen, scenario 1 is the closest to the reference voltage (20 kV), while the behaviors of scenarios 2, 3, and 4 are very similar. The change in the average capacitors voltages due to the parametric uncertainty is negligible, confirming that the proposed MPC approach is robust against the arm inductance variations.

(a)

(b)

(c)

Figure 7-7 The proposed MPC approach in transient mode under parametric uncertainty, (a) dc-links currents and the phase-leg 1 current, (b) the SMs voltages of the upper arm, (c) the SMs voltages of the lower arm.

7.3.3.2 Transient Response

The transient responses of the control methods, the PI controller, and the proposed MPC, while parametric uncertainty exists, are illustrated in Figure 7-7 and Figure 7-8. Initially, the converter transmits -15 MW. At t=0.3 s, the power reference of the converter changes to +15 MW. These simulation studies are carried out by considering that the arm inductances of the phase-leg 1 are 120% of the nominal value. As shown in Figure 7-7(a) and Figure 7-8(a), the parametric uncertainty does not impact the dc-links currents, and the response to the load transient is still faster in the converter controlled by the proposed MPC approach. The upper arm capacitors voltages are presented in Figure 7-7(b) and Figure 7-8(b). In the converter controlled by the PI controller, the transient response worsens compared to the case without

(a)

(b)

(e)

Figure 7-8 Conventional PI-based controller in transient mode under parametric uncertainty, (a) dc-links currents and the phase-leg 1 current, (b) the SMs voltages of the upper arm, (c) the SMs voltages of the lower arm.

the parametric uncertainty as the capacitors voltages reaches 2175 V in the transient period. Due to the parametric uncertainty, the average capacitors voltages of the upper arm is a little less than 2 kV before the load transient, and it is a little higher after the load transient. As shown in Figure 7-7(c) and Figure 7-8(c), the lower arm capacitors voltages are not impacted by the parametric uncertainty. In the end, it can be concluded that the performance of the converter controlled by the MPC approach is still superior despite of 20% variation in the arm inductance.

7.4 Summary

This chapter developed an MPC algorithm for the dc/dc MMC. First, the dynamic equations were extracted, and then, using the Forward Euler method, they were discretized. Using the

discrete-time dynamic model of the converter, an MPC approach was developed to satisfy the control objectives by minimizing three separate cost functions. The simulation results of the presented MPC method and the conventional PI-based controller were compared in transient and steady-state conditions. The advantages of the presented MPC approach are:

- The internal dynamic, i.e., capacitors voltages and arms currents, and external dynamic, i.e., the injected currents into dc-links, are improved with the proposed MPC method is used.
- The proposed MPC approach is more competent in reducing the circulating current in the steady-state. As a result, this improves the overall system efficiency.
- Unlike the PI-based controllers with multiple parameters to be tuned, the proposed MPC approach offers a very straightforward implementation. Because the designed cost functions include one primary term and one secondary term with less importance, the tuning process of the weighting factors is very simple [66].

The robustness of the proposed MPC approach against parameter variation was investigated. The arm inductance was identified as the most effective element, where its variations impact the converter operation. According to the obtained results, the proposed approach can tolerate 20% tolerance in the arm inductance.

Chapter 8 Realization of an Efficient Fault-Blocking Capability

In this chapter, first, the behavior of the dc/dc MMC in cases of short-circuit faults is investigated. Then, the number and types of SM in each arm are determined with respect to fault-blocking requirements and the efficient operation of the converter. The designed converter is studied in different cases, including steady-state operation, load-transient, and short circuit faults.

8.1 DC Fault Analysis

In Figure 2-2, the fault current path in the case of short-circuit fault at the dc-links 1 and 2 is shown. As all the IGBTs are turned off immediately after a fault detection, the current path within the SM depends on the fault current direction and the SM topology. When the short-circuit fault happens at dc-link 1, the fault current I_{F2} flows through the SM's capacitor (both HBSM and FBSM). Therefore, both the HBSM and FBSM in the upper arm are able to suppress

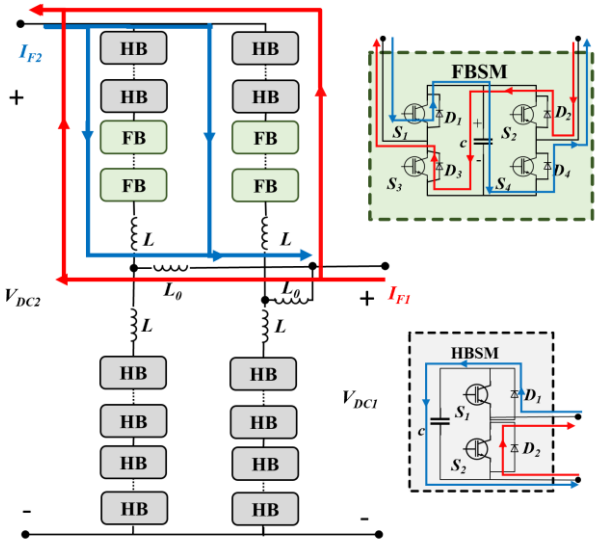


Figure 8-1 The dc/dc MMC and fault currents paths.

the fault current. On the other hand, when the short-circuit fault occurs at dc-link 2, the fault current I_{F1} would path through diode D_2 in HBSMs and the capacitor in FBSMs. Therefore, only FBSMs in the upper arm can block I_{F1}.

8.2 Proposed Efficient Topology

To find an efficient topology that provides the fault-blocking capability, the number of SMs and their topologies are determined based on two criteria. The first one is that the modified topology of the dc/dc MMC must be able to suppress the fault current at both dc-links. The other criterion is that the modified topology should utilize the added FBSMs to generate greater arm ac voltage in the normal operation mode. In this way, the converter would operate more efficiently.

8.2.1 Fault-Current Blocking Requirements

As discussed earlier, the fault current passes only through the upper arm. Therefore, the SMs in the upper arm can only suppress the fault current. In the case of short-circuit fault at the dc-link 1, either HBSMs or FBSMs in the upper arm can suppress the fault current. However, the number of SMs should be high enough to withstand the dc-link 2 voltage. Assuming that the nominal voltage of each SM is V_{CN}, the total required number of SMs to suppress the fault current in case of dc-link 1 fault is calculated by

$$n_u^{fb} = ceil\left[\frac{V_{dc2}}{V_{CN}}\right] \tag{8-1}$$

On the other hand, the short-circuit fault at dc-link 2 necessitates using FBSMs to suppress the fault current. By looking at Figure 2-2, it can be understood that as long as the total voltage of FBSMs is larger than V_{dc1}, the fault current can be blocked. Considering V_{CN} as the nominal voltage of FBSMs, the number of FBSMs can be found by

$$n_{u,f}^{fb} = ceil\left\lceil \frac{V_{dc1}}{V_{CN}} \right\rceil \tag{8-2}$$

Due to the fact that the FBSM has twice the number of semiconductors as the HBSM, the number of FBSMs is kept as low as possible. It improves the converter efficiency by reducing both conduction and switching losses. As a result, only $n_{u,f}$ number of upper SMs is selected as the FBSMs, and the rest is HBSMs.

$$n_{u,h}^{fb} = n_u^{fb} - n_{u,f}^{fb} \tag{8-3}$$

8.3 Improving the Efficiency

As explained earlier, the number and type of the upper arm SMs are determined based on the fault-blocking requirements. As the fault current does not pass through the lower arm, the lower arm SMs are not involved in the fault current suppression. However, by careful selection of the number and type of lower arm SMs, the converter would be able to operate with higher arm ac voltage. The range of upper arm voltage is already expanded by using the FBSMs. These will allow the upper arm to generate negative voltages. As thoroughly explained in the previous chapters, when the converter applies higher arm ac voltage, the phase-difference between arms ac voltages would be reduced (approaches to 180°). Accordingly, the ac circulating will decrease; this will improve the efficiency of the converter significantly. Although it seems that the converter can operate at any phase difference by adding additional SMs and generating the required arm ac voltage, based on the analytical studies provided in Chapter 4, the operation of the hybrid dc/dc MMC is limited because of capacitors voltages unbalance. There is a phase difference below that the converter cannot keep the capacitors voltages balanced. Therefore, the first step in determining the number of SMs in the lower arm is to find the minimum achievable phase difference. By conducting the analytical studies presented in Chapter 4, the minimum phase-difference φ_{min}, which the converter can operate at is found. Then, based on this phase difference and assuming that the converter transmits *P* amount of power, the arm ac voltage is obtained by

$$\hat{v}_{AC} = \sqrt{\frac{P_{AC.}2X_e}{\sin(\varphi_{min})}} \tag{8-4}$$

Having the arm ac voltage, the minimum and maximum arms voltages that each arm must generate are found as

$$v_{arm,min} = V_{arm,DC} - \hat{v}_{AC} \tag{8-5}$$

$$v_{arm,max} = V_{arm,DC} + \hat{v}_{AC} \tag{8-6}$$

Accordingly, the number of HBSMs and FBSMs in each arm can be found as

$$n'_{arm,f} = ceil\left\lfloor -\frac{v_{arm,min}}{V_{CN}} \right\rfloor \tag{8-7}$$

$$n'_{arm} = ceil\left\lceil \frac{v_{arm,max}}{V_{CN}} \right\rceil \tag{8-8}$$

$$n'_{arm,h} = n_{arm} - n_{arm,f} \tag{8-9}$$

As can be seen, the number of HBSMs and FBSMs in the upper arm are calculated in two ways. The number of HBSMs and FBSMs in the upper arm should not be less than $n_{u,h}^{fb}$ and $n_{u,f}^{fb}$ in order to provide the fault-current blocking capability. In the case that $n_{u,f}^{fb} > n'_{u,f}$ and $n_{u,h}^{fb} > n'_{u,h}$, $n_{u,f}^{fb}$ and $n_{u,h}^{fb}$ are selected as the number of upper arm SMs. The number of SMs in the lower is calculated based on the maximum arm ac voltage that can be generated by the upper arm. When $n_{u,f}^{fb} < n'_{u,f}$ and $n_{u,h}^{fb} < n'_{u,h}$, additional SMs can be added to the upper arm to improve the converter performance in the steady-state. This process is illustrated in Figure 8-2.

Based on the obtained phase difference φ_{min}, the amplitude of ac current is calculated by

$$\hat{i}_{AC} = 2\sqrt{\frac{(1-D)P}{M.X_e.\tan\left(\frac{\varphi_{min}}{2}\right)}} \tag{8-10}$$

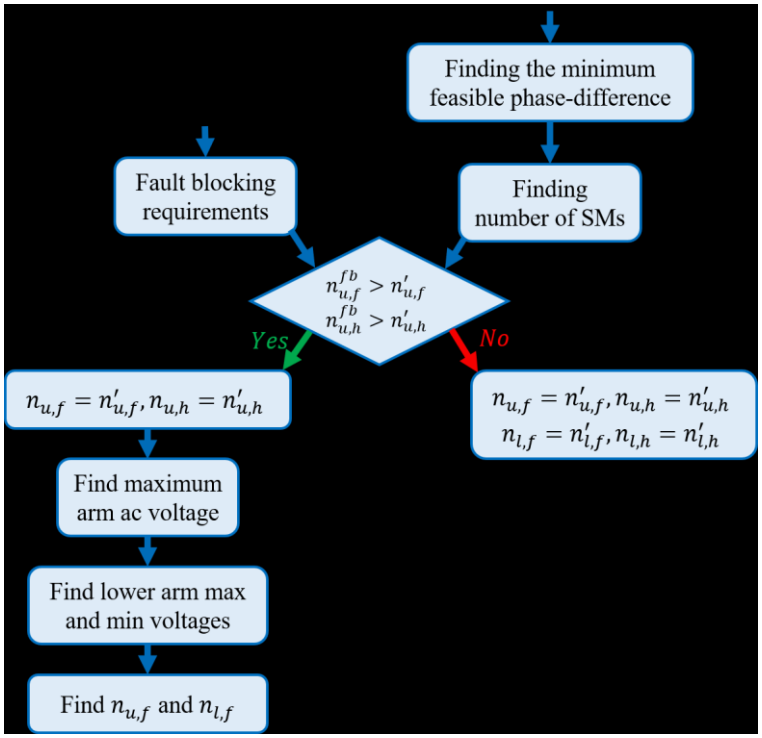


Figure 8-2 Flow chart of SM selection.

Table 8-I
Main Parameters of the Simulated Converter

Parameter	**Symbol**	**Value**
Rated Power	S	15 MW
DC-Link1	V_{DC1}	14 kV
DC-Link2	V_{DC2}	20 kV
Arm Inductance	L	1.2 mH
Phase Inductance	L_0	0.26 H
SM Capacitance	C	10 mF
SM Nominal Voltage	V_{CN}	2 kV
Operating Frequency	f_S	360 Hz
Proposed Modified Topology	**Symbol**	**Value**
Number of Upper Arm HBSMs	n_{uh}	3
Number of Upper Arm FBSMs	n_{uf}	7
Number of Lower Arm HBSMs	n_{lh}	12
Conventional Topology	**Symbol**	**Value**
Number of Upper Arm FBSMs	n_{uh}	10
Number of Lower Arm HBSMs	N_{lh}	10

8.4 Simulation Studies

Several simulation studies are carried out to investigate the proposed modified topology of the dc/dc MMC. The main parameters of a 15 MW dc/dc MMC with two phase-legs are shown in Table 4-II. The performance of the modified converter is compared with the topology used in [21] for fault current blocking. This topology is called conventional topology in the comparison studies and has an equal number of SMs in each arm and uses only FBSMs in the upper arm.

8.4.1 Load Transient Operation

In Figure 8-3, the simulation results of the proposed modified topology are presented. Before t=0.4 s, the converter transmits -15 MW (power extracted from dc-link 1 and delivered to dc-link 2). After t=0.4 s, the converter transmits +15 MW to the dc-link 1. The dc-links currents and the output current of phase-leg 1 are demonstrated in Figure 8-3 (a). The converter successfully follows the power reference, and the dc-link 1 and the phase-leg 1 currents reach a steady state after 50 ms. It took a little longer for the dc-link 2 current to enter steady-state, which happens after 75 ms. As shown in Figure 8-3 (b), the arms currents have dc and ac components which enable the power exchange between the dc-links and balance the capacitors voltages. Because of added SMs to the lower arm and having FBSMs in the upper arm, the arms currents still have a small ac current in the transient, which helps maintain the capacitors voltages. The upper and lower arms capacitors voltages are presented in Figure 8-3 (a) and (b), where the capacitors in the upper arm have a 7.5 % overshoot and lower arm capacitors experience a very subtle transient. All the capacitors voltages reach steady-state after 0.1 s.

8.4.2 Steady-State Operation

In Table 8-II, the results of the steady-state operation of the proposed modified topology and the conventional topology are compared. As can be seen, both converters provide a very smooth dc current to the dc-links. As the modified topology operates with 10 kV of arm ac voltage, the phase difference is reduced from 221° to 194.5°. As a result, the ac circulating

(a)

(b)

(c)

(d)

Figure 8-3 Load transient operation, (a) the dc-links currents and the phase-leg 1 current, (b) the arms currents, (c) the SMs voltages of the upper arm, (d) the SMs voltages of the lower arm.

current in the modified topology is significantly smaller than that in the conventional topology. Accordingly, the conduction loss is reduced from 62.5 kW to 36 kW in the proposed modified topology. In addition, the switching frequency in the modified topology is smaller than the conventional topology due to the reduction in the ac circulating current. Therefore, the total

Table 8-II
Steady-State Comparison of the Proposed Modified Topology and the Conventional Topology

Parameters	Conventional Topology	The Proposed Modified Topology
Phase-Difference [Degree]	221	194.5
Arm ac Voltage [kV]	6	10
Amplitude of Circulating Current [A]	820	465
Conduction Loss [kW]	62.5	36
Upper Arm Switching Frequency [Hz]	FBSMs: 470	FBSMs: 420
	HBSMs: -	HBSMs: 360
Lower Arm Switching Frequency	HBSMs: 504	HBSMs: 480
Switching Loss [kW]	Upper arm: 52	Upper arm: 28
	Lower arm: 28	Lower arm: 32
	Total: 80	Total: 60
Total Loss [kW]	142.5	96.5

switching loss is reduced by 25 % in the modified topology. In the end, the total loss is decreased by 30 % in the modified topology.

8.4.3 Fault Analysis

The proposed modified topology is able to block the fault current in the cases of short-circuit fault occurring in the dc-links 1 and 2. To thoroughly investigate the fault-blocking capability of the modified topology, the designed hybrid topology in Table 4-II is simulated in two different case studies.

8.4.3.1 Short-Circuit Fault in the Low-Voltage Side

The results for the case where the short-circuit fault occurs in dc-link 1 are illustrated in Figure 8-4. In this case study, the short-circuit fault happens at t=0.2 s, remains for 0.1 s, and clears at t=0.3 s. The dc-links currents and the phase-leg 1 current are shown in Figure 8-4 (a); after the fault incident, they go to zero. The dc currents are zero during the fault, and when the fault is cleared, they follow the current references. As shown, the proposed

(a)

(b)

(c)

(d)

(e)

Figure 8-4 Low-voltage side short-circuit, (a) the dc-links currents and the phase-leg 1 current, (b) the arms currents, (c) the arms voltages, (d) the SMs voltages of the upper arm, (e) the SMs voltages of the lower arm.

modified topology was able to suppress the fault current. As presented in Figure 8-4 (b), the arms currents are also zero during the fault, and after fault clearance, they experience a transient and then reach steady-state after 50 ms. Figure 8-4 (c) demonstrates the arms voltages, where the upper arm voltage is at the maximum voltage (20 kV), and the lower arm voltage sinks to zero during the fault. Having the maximum voltage in the upper arm suppresses the fault current. The upper arm SMs voltages are presented in Figure 8-4 (d). Immediately after the fault, the capacitors are charged up to approximately 2050 V and remain at this voltage during the fault. After fault clearance, the upper arm capacitors voltages have an overshoot of 7.5 % and then settle down to the steady-state after 0.1 s. The lower arm capacitors are exhibited in Figure 8-4 (e). They show the same behavior as the upper arm capacitors, except they do not charge up after the fault incident.

8.4.3.2 Short-Circuit Fault at the High-Voltage Side

The simulation results of the designed converter detailed in Table 4-II are illustrated in Figure 8-5. In this case study, a short-circuit fault occurs at the high voltage side at t=0.2 s, and the fault is cleared at t=0.3 s. the dc-links currents and the phase-leg 1 current are shown in Figure 8-5(a), where the results confirm the fault-blocking capability of the designed converter. After the t=0.3 s, the dc links current follows the power reference while the dc-link 2 experiences an overshoot. The arms currents are exhibited in Figure 8-5(b). The arms currents go to zero after the fault incident and remain zero during the fault. After fault clearance, the arms currents have a short transient and reach steady-state after 50 ms. As demonstrated in Figure 8-5(c), the upper arm voltage is fixed at -14 kV, and the lower arm voltage is remained at +14 kV to suppress the fault current. The upper and lower arms capacitors voltages are presented in Figure 8-5(d) and (e). The capacitors voltages are constant during the fault, and after fault clearance, they have a 7.5 % overshoot. The capacitors voltages reach the steady-state after 0.1 s.

(a)

(b)

(c)

(d)

(e)

Figure 8-5 High-voltage side short-circuit, (a) the dc-links currents and the phase-leg 1 current, (b) the arms currents, (c) the arms voltages, (d) the SMs voltages of the upper arm, (e) the SMs voltages of the lower arm.

8.5 Summary

This chapter proposed a modified topology of the dc/dc, which offers high efficiency and fault-blocking capability. In the proposed topology, the number and type of the upper arm SMs were selected based on the fault-blocking requirements, whereas the number and type of SMs in the lower arm were chosen to improve the steady-state operation of the converter. To improve the converter efficiency, the converter was designed to operate with higher arm ac voltage utilizing the used FBSMs in the upper arm and added SMs in the lower arm. The transient performance of the designed converter was investigated in the case of sudden load change. The obtained results confirmed that the designed converter is able to follow the changes in the power reference. The steady-state performance of the designed converter was studied, where the conduction and switching losses are compared with the conventional topology of the dc/dc MMC proposed for fault-blocking. The results confirmed that the ac circulating current is significantly reduced in the proposed topology, and accordingly, the conduction loss is also decreased. The switching losses were also reduced in the proposed topology, resulting in a 30% improvement in the total loss. Simulation results verified the fault-blocking capability of the proposed topology is verified when short-circuit fault occurs at dc-links 1 and 2.

Chapter 9 Conclusion and Future Work

9.1 Conclusion

This chapter summarizes the contributions of this thesis and provides suggestions for future works. The focus of this study was on the design, analysis, and control of the dc/dc MMC. This study helped improve the performance of the dc/dc MMC and facilitated the reliable application of this converter in the near future grids.

In Chapter 3, an augmented design method for the dc/dc MMC was proposed, which considers the converter's hardware and control aspects. This design approach improved the converter efficiency and reduced the number of SMs. The results from the detailed simulation of the switching converter model confirmed the results from the proposed analytical and semi-analytical methods. In addition to the reduced number of SMs and losses, the proposed augmented design approach expanded the range of appliable phase differences helping the converter to operate with a lower current rating.

Chapter 4 investigated the capacitors voltages balance of the hybrid dc/dc MMC and the associated operation limits. The conducted analytical study can determine whether the capacitors voltages of HBSMs and FBSMs could be maintained balanced or not at each operating point. The range of phase differences at which the capacitors voltages can be balanced is found using this approach. The results from the analytical study were confirmed by the ones from the simulation studies. The obtained results showed that the operation range becomes more limited as the transmitted power increases. Similarly, as the conversion ratio and arm inductance increase, the range of phase differences at which the capacitors voltages in the hybrid dc/dc MMC can be balanced becomes smaller.

Chapter 5 proposed a fault-tolerant operation strategy for the dc/dc MMC using its unique characteristics. It was shown that, unlike the dc/ac MMC, the dc/dc MMC could continue its operation after the SM fault without the need to add redundant SMs. The satisfactory

performance of the proposed strategy was observed in the three simulated scenarios. The first scenario showed that if the faulty arm has redundant SMs, the converter continues its operation with the maximum arm ac voltage. In the case of not having redundant SMs in the faulty arm, by reducing the arm ac voltage, the post-fault operation is realized at the cost of increased ac circulating current. The second case study showed that when the ac circulating current is limited, the fault-tolerant operation cannot be realized by only reducing the arm ac voltage. To satisfy the applied current limit, the power transmission must decrease to prevent increasing the circulating current. In the third scenario, a severe SMs fault was simulated, where two consecutive SMs faults occurred in the lower arm. This study showed that by reducing the power transmission and the arm ac voltage, the converter could tolerate several SMs faults in one arm.

In Chapter 6, detailed and simplified steady-state models were developed which can fully show the behavior of the dc/dc MMC in the unsymmetrical condition. The obtained results confirmed the capability of the developed models in the illustration of the unsymmetrical operation. The maximum tolerable variation of the arm inductance and the arm ac voltage, and the leaked ac current into the dc-link 2 were found in cases with different dc-link 2 lengths, transmitted powers, and conversion ratios.

In Chapter 7, an MPC algorithm improving the internal and external dynamics of the dc/dc MMC converter was developed. The simulation results of the presented MPC method and the conventional PI-based controller were compared in transient and steady-state. They showed that the converter controlled by the proposed MPC approach has a smaller circulating current and faster response time. Moreover, unlike the PI-based controllers with multiple parameters to be tuned, the proposed MPC approach offers a very straightforward implementation.

In Chapter 8, a modified topology of the dc/dc MMC was proposed to facilitate high efficiency and fault-blocking capability. In the proposed topology, the number and type of the upper arm SMs were selected based on the fault-blocking requirements. The number and type of SMs in the lower arm were chosen so that the converter operates with higher arm ac voltage. In this way, FBSMs in the upper arm can also be useful in normal operation. The results of the steady-state operation indicated that the ac circulating current and conduction loss are significantly

reduced in the proposed modified topology. The switching frequency and switching losses also decreased in the proposed topology, improving the overall efficiency of the converter. The designed converter was simulated in cases where short-circuit fault occurs at dc-links 1 and 2 confirming that the proposed topology has the bidirectional fault-blocking capability.

9.2 Future Work

The following research studies can be conducted in continuation of the work presented in this thesis:

- Improving the dynamic performance of the dc/dc MMC by reducing the size of phase inductors. The conventional topology of the dc/dc MMC contains a relatively large phase-inductor to filter out the ac circulating current. However, there exists a potential to reduce the filtering requirements by proper control actions.
- Extending the proposed augmented design approach to find the optimum submodule capacitance.
- Expanding the proposed unsymmetrical models and analysis to other modular multilevel converter topologies.
- Developing learning-based controllers for the dc/dc MMC. Such controllers have an excellent potential to address the complex and uncertain nonlinear dynamics of large-scale dc grids.

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Appendix

The calculated formulas for E_{2uf}, E_{1ufmax} and E_{3ufmin} are presented here.

$$E_{2uf} = \frac{1}{\omega}.[2(\pi - \theta_{vu}).V_{u,DC}.I_{u,DC} + 2\sin(\theta_{vu}).\left(2V_{u,DC}.I_{u,AC}.\cos(\phi') - 2V_{u,AC}.I_{u,DC}\right) + V_{u,AC}.I_{u,AC}.\cos(\phi').\left(\frac{1}{2}\sin(2\theta_{vu}) - (\pi - \theta_{vu})\right)] \quad \text{(A-1)}$$

$$E_{1ufmax} = 2I_{u,DC}\left[V_{ufm}.\left(\theta_{fu} - \theta_{iu} + \varphi'\right) + V_{u,DC}.\left(\theta_{vu} - \theta_{fu}\right)\right] - 2\hat{\imath}_{AC}.[V_{ufm}.\left(\sin\left(\theta_{fu}\right).\cos(\varphi') + \sin(-\theta_{iu} + \varphi')\right) + V_{u,DC}\cos(\varphi')\left(\sin(\theta_{vu}) - \sin\left(\theta_{fu}\right)\right)] + 2I_{u,DC}\hat{v}_{AC}\left(\sin(\theta_{vu}) - \sin\left(\theta_{fu}\right)\right) - \hat{\imath}_{AC}.\hat{v}_{AC}.\cos(\varphi')\,[\theta_{vu} - \theta_{fu} + \frac{1}{2}\left(\sin(2\theta_{vu}) - \sin(2\theta_{fu})\right)] \quad \text{(A-2)}$$

$$E_{3ufmin} = -2\hat{\imath}_{AC}.\left(V_{u,DC} - V_{uhm}\right).\sin(\theta_{hu}).\cos(\varphi') + 2I_{u,DC}.\left(V_{u,DC} - V_{uhm}\right).\theta_{hu} + 2I_{u,DC}.\hat{v}_{AC}.\sin(\theta_{hu}) - \hat{\imath}_{AC}.\hat{v}_{AC}.\cos(\varphi')\left(\theta_{hu} + \frac{1}{2}.\sin(2\theta_{hu})\right) \quad \text{(A-3)}$$