Soft-Switching Technique for a Three-Phase Isolated Matrix Rectifier

by

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Abstract

Matrix converters (MC) have attracted more attention recently in high-power applications. Matrix converters can perform direct AC to AC electrical power conversion without DC-link capacitors, which reduce the size of the converter. Matrix rectifiers (MR) inherit all the advantages of traditional matrix converters and are promising in AC-DC applications such as telecommunication systems, front-end power converters for high-voltage direct current (HVDC), and aircraft systems.

In this thesis, a novel ZVS operation method for a three-phase isolated matrix-type rectifier is proposed. The presented pulse width modulation (PWM) scheme realized ZVS for all twelve MOSFET devices. The ZVS operation of MOSFET switches is analyzed and operating states during switch transitions is discussed. The operation principle of the converter is addressed. The comparison between the proposed PWM and existing 8-segment PWM and 6-segment PWM is presented to show the differences. The effectiveness of ZVS operation of the proposed PWM scheme is verified by both simulation and experimental results.

Preface

Some of the research conducted for this thesis forms part of a research collaboration between University of Alberta, led by my supervisor Professor Yunwei (Ryan) Li, and Ryerson University, led by Professor Dewei (David) Xu. The experiments referred to in chapter 5 were carryout of at Ryerson University's hardware platform through my visiting research there. PhD student Jahangir Afsharian also assisted in the experiment. The analysis in chapter 3 and comparison analysis in chapter 4 are solely my original work, as well as the literature review in chapter 2.

Acknowledgement

First and foremost, I would like to express my deepest appreciation to my supervisor, Dr. Yunwei (Ryan) Li for his continuous guidance and enthusiastic encouragement during my study and research in University of Alberta. The door to Dr. Li's office was always open whenever I ran into a trouble spot or had a question about my research or writing.

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I also thank all of the generous people who have shared their time and resources with me. This includes (although not limited) to my friends and colleagues in Dr. Li's research group, especially Rouzbeh Reza Ahrabi, Fanxiu Fang, Zhongyi Quan, Hao Tian, Li Ding, Yuzhuo Li, for their discussion and advices on my research as well as assistance on writing correction.

Finally, I must express my very profound gratitude to my parents and siblings, to my aunt's family, and to my husband, Kun-Long Chen, for providing me with unfailing support and continuous encouragement throughout my years of study and through the process of writing this thesis. This accomplishment would not be possible without them. Thank you.

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List of Symbols

h	Harmonic order
i_P	Transformer primary side current
$S_{11} \dots S_{26}$	Twelve MOSFETs in the three-phase isolated matrix rectifier
$\overrightarrow{I_1} \dots \overrightarrow{I_6}$	Active vectors
$\overrightarrow{I_0}$	Zero vector
$\overrightarrow{I_{x+}}$	Active vectors in positive direction
$\overrightarrow{I_{x-}}$	Active vectors in negative direction
i_a, i_b, i_c	Three phase input currents
θ	Displacement angle
$\overrightarrow{I_{ref}}$	Current reference vector
T_S	Sampling period
T_x	Dwell time of $\overrightarrow{I_x}$
T_y	Dwell time of $\overrightarrow{I_y}$
T_0	Dwell time of $\overrightarrow{I_0}$
m_a	Modulation index
i_L	Output inductor current
I_m	Peak of fundamental frequency component in i_a
V_P	Transformer primary side voltage
V_s	Transformer secondary side voltage
v_A, v_B, v_C	Phase voltage of three phases
V_o	Output voltage
SQ_1	Traditional 8-segment PWM scheme
SQ_2	6-segment PWM scheme
SQ_3	Improvement of traditional 8-segment PWM scheme
v_{AB}, v_{AC}, v_{BC}	Line voltages
ΔD_x	Duty-cycle loss time interval from $\overrightarrow{I_0} - \overrightarrow{I_x}$

ΔD_y	Duty-cycle loss time interval from $\overrightarrow{I_0} - \overrightarrow{I_y}$
ΔD_{total}	Total duty-cycle loss
$d_x(\theta)$	Total duty-cycle of sub-topology *x*
$d_y(\theta)$	Total duty-cycle of sub-topology *y*
$d_0(\theta)$	Total duty-cycle of zero vectors
$d_{sx}(\theta)$	Total duty-cycle of sub-topology *x* in secondary side
$d_{sy}(\theta)$	Total duty-cycle of sub-topology *y* in secondary side
I_o	Load current
L_{lk}	Transformer leakage inductance
n	Transformer turns ratio
V_m	The peak value of input phase voltage
C_0	Output capacitance of each switch
C_{TR}	Transformer parasitic capacitor.
I_{p_min}	The primary current i_p at the end of the off-time of each Switching cycle
ΔI_{min}	Minimum output current ripple
ΔI_{max}	Maximum output current ripple
$C_{11} - C_{26}$	Parasitic capacitances of MOSFETs
$D_{11} - D_{26}$	Parasitic diodes of MOSFETs
E_{l_min}	Minimum energy stored in L_{lk}
E_{c_max}	Maximum energy need to charge capacitances
E_{on}	Turn-on energy loss
E_{off}	Turn-off energy loss
τ	Deadtime
P_C	Conduction loss
P_{CM}	MOSFET conduction loss
P_{CD}	Diode conduction loss
R_{ds}	Drain-source on-state resistance
$i_{ds(t)}$	Instant value of the MOSFET on-state current
t_duty	Conduction time of the MOSFET

U_{d0}	Diode on-state zero-curent voltage
R_d	Diode on-state resistance
C_{oss}	Output capacitance of MOSFET
P_{total}	Total power loss

List of Abbreviations

MC	Matrix Converters
MR	Matrix Rectifiers
SVM	Space Vector Modulation
ZVS	Zero-Votlage Swiching
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
AC	Alternating Current
DC	Direct Current
THD	Total Harmonic Distortion
GTO	Gate Turn-off Thyristors
EV	Electrical Vehicle
PFC	Power Factor Correction
HVDC	High-Voltage Direct Current
CSR	Current Source Rectifier
FB	Full Bridge
PWM	Pulse Width Modulation
SQ	Sequence
HTL	High To Low

Chapter 1

Introduction

Matrix converters (MC) have attracted more attention recently in high-power applications. Much of the research related to matrix converters focuses on new topologies, modulation and control strategies, and commutation and stability analysis. Matrix rectifiers (MR) inherit all the advantages of traditional matrix converter. The isolated matrix rectifier is attractive in high-power high-frequency industry applications. The soft-switching technique can significantly decrease or totally remove the severe switching loss caused by high switching frequency.

In this introductory chapter, an overview of the matrix converter and matrix rectifier is presented. Secondly, commonly practiced modulation strategies are discussed, especially the space vector modulation (SVM) strategy for the three-phase isolated matrix rectifier. Then, the zero-voltage switching (ZVS) technique is introduced. Finally, this chapter presents the scope and outline of this thesis.

1.1 Matrix Converter

Matrix converters can perform direct AC to AC electrical power conversion without dc-link capacitors. The conventional matrix converter is a direct three-phase to three-phase AC-AC converter, which consists of nine bidirectional voltage-blocking current-conducting matrix switches to provide bidirectional power flow between grid and ac loads. This is so that any input phases can be connected to any output phases at any time, as shown in Figure 1.1. The matrix converter requires switches that have the capacity for conducting and blocking function to the voltage and current in both directions. In practice, because no bidirectional switches are available as yet, the most commonly used bidirectional switches are composed of two reverse connected IGBT/MOSFET devices. This bidirectional structure has a lower voltage drop and lower conduction loss

compared with other bidirectional configurations. Compared with traditional AC/AC converters, the matrix converter has many attractive features. Firstly, it does not have the large capacitor for DC link and energy storage which is bulky, heavy, and susceptible to failure. The bidirectional power flow between grid and ac loads is provided by a set of bidirectional switches. All loads can operate in the full four quadrants. The power factor is controllable, and enables the unity power factor. The amplitude and frequency of output voltage is adjustable. The input and output current and voltage are sinusoidal, and have lower total harmonic distortion (THD). With these features, the matrix converter has promising applications in industry, like for the motor drive system, power supply, wind system, and power quality control, etc.

The topology of the matrix converter was first proposed in the 1970s [1]. In 1976, the study in [2] introduced this topology in detail, and this book is regarded as the start of the matrix converter theory. However, at that time, the power switches used gate turn-off thyristors (GTO), which featured low switching frequency, low reliability, and was bulky and heavy; as a result, it did not attract wide attention. In 1980, the name and concept of the matrix converter was again presented by Venturini and Alesina [3]. They provided the mathematical background and introduced the term “matrix converter”, and described how the low-frequency behaviours of the voltages and currents are generated at the load and source. At the same time, the basic matrix converter modulation strategy/direct transfer function modulation method was proposed [3], giving new momentum to research in this area. In the next several decades, much of the research on matrix converters has been dedicated to development of different topologies [20-24], modulation and control strategies [4-19], commutation, and stability analysis, etc.

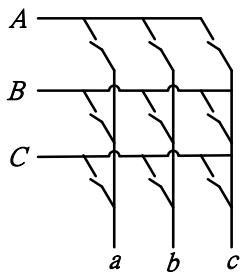


Figure 1.1 Topology of traditional matrix converter.

1.2 Matrix Rectifier

The matrix rectifier (MR) is derived from the conventional matrix converter. Compared with traditional three-phase rectifiers, the matrix rectifier has no energy storage elements, so that it features a simple and compact structure. The utilization of bidirectional power transistors enables bidirectional power flow, and produces a dramatic simplification of the circuits. The traditional rectifier features low switching frequency as a result of poor controllability of thyristors, which causes more serious harmonic pollution to the power grid.

The matrix rectifier has two main topologies: the non-isolated matrix rectifier [25-31] and the isolated matrix rectifier [14], [32-43], [48]. The non-isolated matrix rectifier employs a reduced AC/AC matrix converter as an AC-DC converter, which is achieved by setting the output frequency to zero, leaving one output phase unconnected, and allowing a dc load to be connected across the connected two phases. Compared with the isolated matrix rectifier, it removes the transformer so that there is no leakage inductance. The application is mostly for bidirectional battery chargers in the electrical vehicle (EV) industry, aircraft systems, and vehicle-to-grid (V2G) systems. The isolated matrix rectifier consists of an input filter, three-phase to single-phase matrix converter, high-frequency transformer to provide isolation between source and load, full bridge rectifier, and output filter. By changing the turns ratio of the transformer, the desired output voltage can be obtained. Because improved power density and higher power frequency is desirable in applications where isolation is required (for example, telecommunications systems), the isolated matrix-type rectifiers are most favourable.

In this thesis, the isolated matrix rectifier is selected. The transformer leakage inductance in the isolated matrix rectifier is utilized to achieve ZVS operation of the converter.

The isolated matrix-type rectifiers can be classified into four major categories [44, Figure 1]:

(a) Quasi single-stage buck-derived bridge (indirect) matrix rectifiers, as shown in Figure 1.2 (a);
(b) Single-stage buck-derived (direct) matrix rectifiers, as shown in Figure 1.2 (b);
(c) Quasi single-stage boost-derived bridge (indirect) matrix rectifiers, as shown in Figure 1.2 (c);
(d) Single-stage boost-derived (direct) matrix rectifiers, as shown in Figure 1.2 (d).

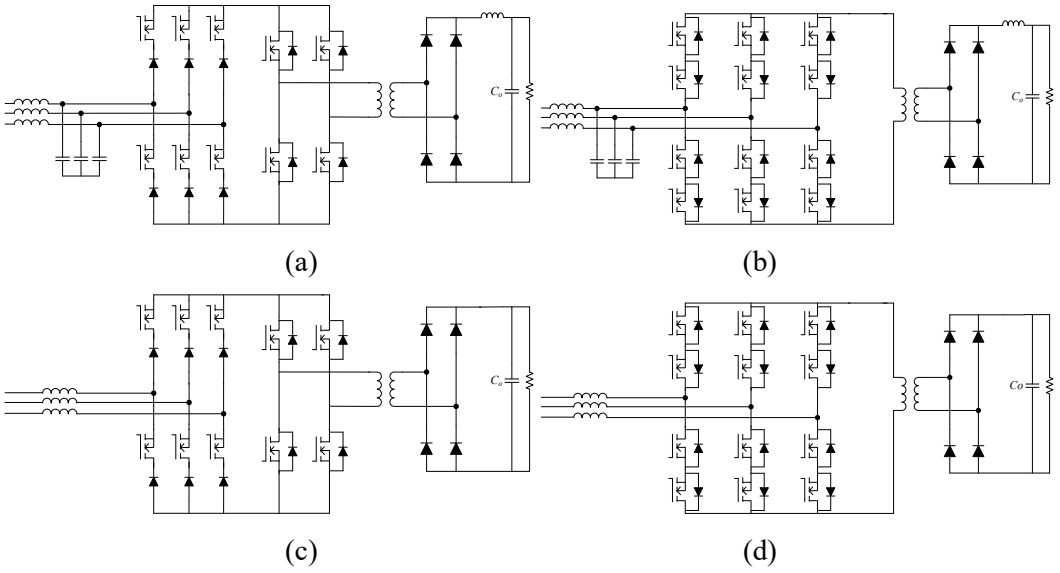


Figure 1.2 Basic structures of isolated matrix rectifier systems: (a) indirect buck-type matrix rectifier, (b) direct buck-type matrix rectifier, (c) indirect boost-type matrix rectifier, (d) direct boost-type matrix rectifier.

For buck-derived matrix rectifier systems (Figure 1.2(a) and (b)), the current on the primary side is impressed by the output inductance. For the boost-derived matrix rectifier systems (Figure 1.2 (c) and (d)), the voltage for controlling the main circuit current is impressed by the output capacitor.

In this thesis, the buck-derived matrix rectifier [32-36] (Figure 1.2 (b)) is adopted, which is suitable for typical telecommunication and HVDC (380V-400V) applications where the output is usually connected to a battery with large voltage fluctuations [45], the input line voltage is high, and the variable output DC voltage is a necessary.

In Figure 1.2 (b), the single-stage power conversion can directly convert the mains-frequency ac voltage into a high-frequency ac voltage, and then connected with a high-frequency isolation transformer, whose secondary side voltage is rectified to the desired dc output voltage, with the direct matrix-type rectifier.

The bidirectional switches of the matrix rectifier that are normally used to realize are insulated-gate bipolar transistors (IGBTs) [27], [32-33], [37-40] and metal-oxide-semiconductor field-effect transistors (MOSFETs) [14], [31], [34-35], [43], [47]. Comparing between the two power transistors, IGBT is a slower device, to the extent that it cannot operate at higher switching frequency. The maximum operating frequency of IGBT is 20 kHz, while the maximum operating frequency of MOSFET is 200 kHz. Furthermore, IGBT has greater conduction loss for medium power.

For high-power density applications, higher switching frequency is desirable. However, the increase of switching frequency will increase switching loss so that it reduces efficiency. The switching loss can be reduced or ideally eliminated if the zero-voltage-switching (ZVS) technique can be applied in the matrix rectifier circuit [14], [35], [37-38], [43], [48-53]. The power circuit capable of ZVS operation is proposed in [34] and [35] as shown in Figure 1.3, which is derived from the topology described in [32] and [33]. The ZVS operation can be realized by utilizing the parasitic capacitances of the switching devices and the transformer leakage inductance. In addition, the MOSFET parasitic body diodes can be utilized during the ZVS implementation process, instead of additional fast recovery diodes, which makes the ZVS operation cost-effective.

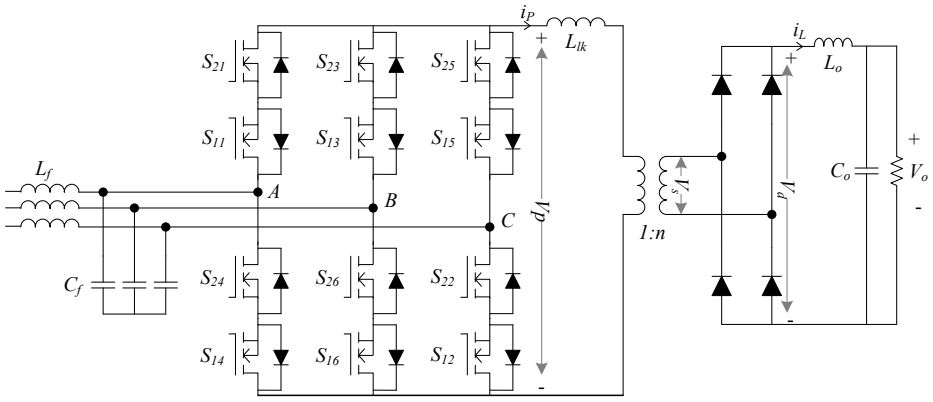


Figure 1.3 Topology of isolated matrix rectifier.

1.3 Modulation Methods

For the matrix converters, one of the most challenging problems is modulation methods, which can be considered the basis of designing a matrix converter. Years of continuous effort on matrix converters have been dedicated to the development of different modulation and control methods. The basic idea of a modulation strategy for the matrix converter is to use the input voltage to synthesize output voltage, while using the output current to synthesize the input current. When Venturini first proposed the matrix converter concept [3], he also proposed the direct transfer function modulation method. According to different synthesis methods, there are several major modulation methods, including switching function modulation strategy [54-56], space vector modulation (SVM) strategy [57-63], carrier-based modulation strategy [4], [64-70], two-phase switching modulation strategy [71-75], direct torque control [76-80], and predictive control [81-88], as shown in Figure 1.4. Many other modulation methods can be derived from these main schemes.

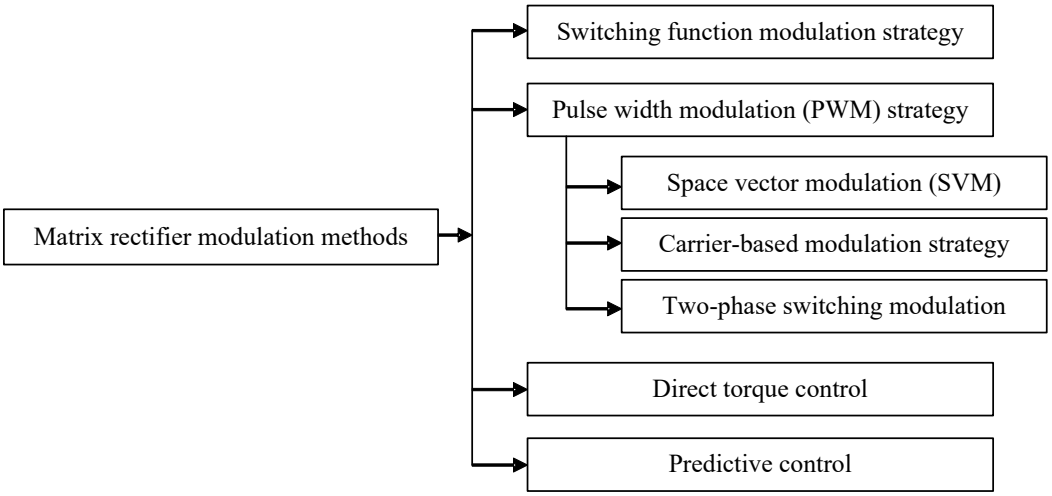


Figure 1.4 Matrix rectifier modulation methods.

The modulation methods for traditional direct matrix converters can also be applied to isolated matrix type rectifiers. The modulation scheme based on space vector modulation (SVM) is especially suited for the three-phase isolated matrix rectifier. [15] and [91] have developed the SVM for the traditional three-phase to three-phase matrix converter. [10], [14], and [48] presented the SVM for the isolated matrix rectifier, which is derived from the SVM of the matrix converter.

The SVM analysis for the isolated matrix rectifier is based on the assumption that the DC current is constant, so it can use the traditional current vector-based SVM stated in [92]. Thus, the three-phase isolated matrix rectifier can be regarded as equivalent to the traditional current-source rectifier (CSR), except that all the switching devices are bidirectional. In this section, the principle and implementation of the SVM technique are presented.

1.3.1 Switching States

For the three-phase isolated buck-derived matrix rectifier, the bidirectional switches are controlled separately, so that there are twelve switching devices in the transformer's primary side. For the PWM switching pattern shown in Figure 1.3, there are four switches in the converter conduct at any time: two switches of one phase leg in the top half bridges and the other two of one phase leg in the bottom half. The three-phase matrix rectifier has a total of fifteen switching states as listed

in Table 1.1.

There are three zero switching states: [AA], [BB], and [CC]. In zero state [AA], the four switches in phase *A* conduct simultaneously and other switches are off. The current i_P is bypassed by phase *A*. The other two zero states are with the same principle with state [AA]. Different from the active switching states in CSR, the three-phase isolated matrix rectifier has a total of twelve active states due to the bidirectional current flow. State [AB] indicates that the two switches in upper leg of phase A, S_{21} and S_{11}, and two switches in lower leg of phase B, S_{26} and S_{16}, are on. The transformer primary side current i_P flows through S_{11} and S_{21}, the transformer, S_{16} and S_{26}, then back to the source. The definition of other switching states is given in the table.

Table 1.1. Switching states and space vectors

Type	Switching states	On-state switch	Current i_P	Space vector
Zero states	AA	$S_{21}, S_{11}, S_{24}, S_{14}$	0	$\overrightarrow{I_0}$
	BB	$S_{23}, S_{13}, S_{26}, S_{16}$		
	CC	$S_{25}, S_{15}, S_{22}, S_{12}$		
Active states	AB	$S_{21}, S_{11}, S_{26}, S_{16}$	$i_P > 0$	$\overrightarrow{I_{1+}}$
	AC	$S_{21}, S_{11}, S_{22}, S_{12}$		$\overrightarrow{I_{2+}}$
	BC	$S_{23}, S_{13}, S_{22}, S_{12}$		$\overrightarrow{I_{3+}}$
	BA	$S_{23}, S_{13}, S_{24}, S_{14}$		$\overrightarrow{I_{4+}}$
	CA	$S_{25}, S_{15}, S_{24}, S_{14}$		$\overrightarrow{I_{5+}}$
	CB	$S_{25}, S_{15}, S_{26}, S_{16}$		$\overrightarrow{I_{6+}}$
	-AB	$S_{24}, S_{14}, S_{23}, S_{13}$	$i_P < 0$	$\overrightarrow{I_{1-}}$
	-AC	$S_{24}, S_{14}, S_{25}, S_{15}$		$\overrightarrow{I_{2-}}$
	-BC	$S_{26}, S_{16}, S_{25}, S_{15}$		$\overrightarrow{I_{3-}}$
	-BA	$S_{26}, S_{16}, S_{21}, S_{11}$		$\overrightarrow{I_{4-}}$
	-CA	$S_{22}, S_{12}, S_{21}, S_{11}$		$\overrightarrow{I_{5-}}$
	-CB	$S_{22}, S_{12}, S_{23}, S_{13}$		$\overrightarrow{I_{6-}}$

1.3.2 Space Vectors

The switching states can be represented by space vectors. The space vector diagram for the three-phase isolated matrix converter is shown in Figure 1.5 (a) and (b), where the active states can be represented by active vectors $\overrightarrow{I_1}$ to $\overrightarrow{I_6}$, and zero states can be represented by zero space vectors $\overrightarrow{I_7}$, $\overrightarrow{I_8}$, and $\overrightarrow{I_9}$. The six equal active

vectors form a regular hexagon, and the zero vector lies on the centre of the hexagon.

Depending on the direction of the transformer primary side current i_P, there are two possible switching states for each active vector, as shown in Figure 1.5 (a) and (b).

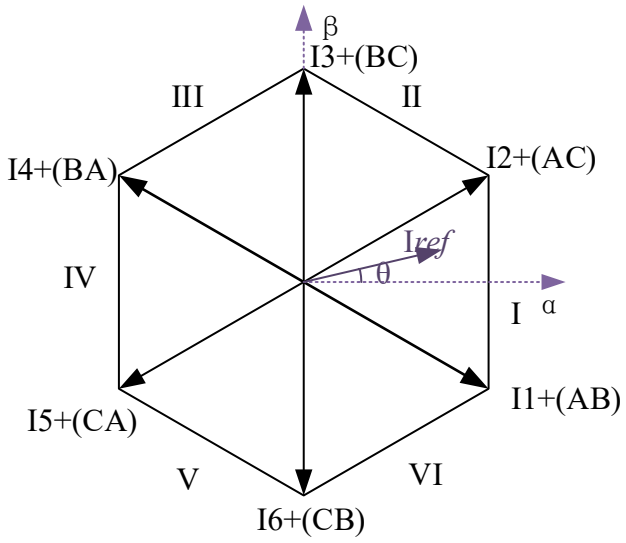
The current space vector can be expressed in terms of the three input currents i_a, i_b, i_c:

$$\vec{I}(t) = \frac{2}{3}[i_a(t)e^{i0} + i_b(t)e^{i2\pi/3} + i_c(t)e^{i4\pi/3}] \quad (1.1)$$

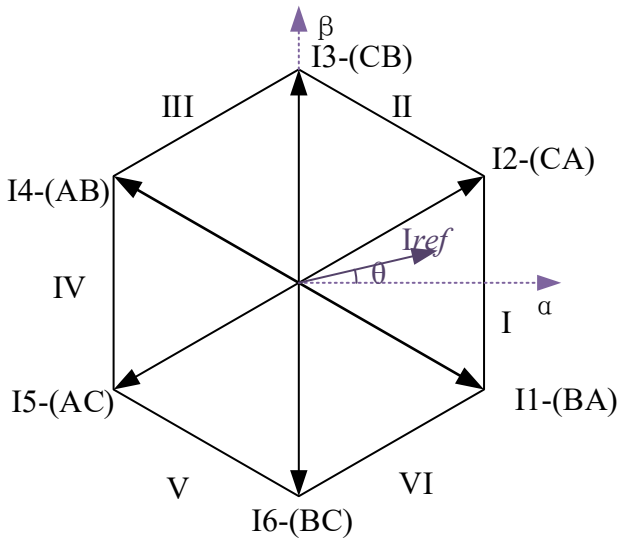
Based on different switching states, the six active vectors can be expressed as:

$$\overrightarrow{I_n} = \frac{2}{\sqrt{3}} i_P e^{i(\frac{n\pi}{3} - \frac{\pi}{2})} \quad (1.2)$$

where *n*=1, 2,…, 6 for sectors I, II, …, VI, respectively.



(a) $i_P > 0$



(b) $i_P < 0$

Figure 1.5 Space vector diagram for isolated matrix rectifier.

On the contrary, the current reference vector $\overrightarrow{I_{ref}}$ rotates in space at the same angular velocity as the grid voltage vector in order to get the sinusoidal input current. The unity power factor can be achieved by aligning the reference vector with the grid voltage vector. As shown in Figure 1.6, the reference vector $\overrightarrow{I_{ref}}$ can be synthesized by three adjacent stationary vectors based on the sector it located. For example, in sector I, $\overrightarrow{I_{ref}}$ is synthesized by active vectors $\overrightarrow{I_1}$ and $\overrightarrow{I_2}$, and zero vector $\overrightarrow{I_0}$. When $\overrightarrow{I_{ref}}$ passes through sectors one by one, different switches are turned on and off.

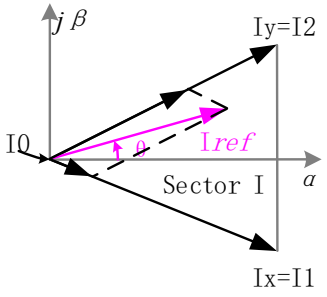


Figure 1.6 Synthesis of $\overrightarrow{I_{ref}}$ by $\overrightarrow{I_1}$, $\overrightarrow{I_2}$, and $\overrightarrow{I_0}$.

1.3.3 Dwell Time Calculation

The dwell time of stationary vectors represents the duty-cycle time of the operating switches during a sampling period T_S. In this section, all the analysis is done in sector I, so that the three stationary vectors are $\overrightarrow{I_1}, \overrightarrow{I_2}$, and $\overrightarrow{I_0}$ respectively. Assuming that the output inductor current I_L is constant, and the sampling period T_S is small enough, so that $\overrightarrow{I_{ref}}$ can be considered as constant during T_S. the ampere-second balancing equation is thus given by:

$$\overrightarrow{I_{ref}}T_S = \overrightarrow{I_1}T_1 + \overrightarrow{I_2}T_2 + \overrightarrow{I_0}T_0 \tag{1.3}$$

$$T_S = T_1 + T_2 + T_0 \tag{1.4}$$

where T_1, T_2, and T_0 are the dwell times for vectors $\overrightarrow{I_1}$, $\overrightarrow{I_2}$, and $\overrightarrow{I_0}$, respectively. The dwell time for $\overrightarrow{I_1}$, $\overrightarrow{I_2}$, and $\overrightarrow{I_0}$ can be calculated as below:

$$T_x = T_1 = m_a T_S \sin(\frac{\pi}{6} - \theta) \tag{1.5}$$

$$T_y = T_2 = m_a T_S \sin(\frac{\pi}{6} + \theta) \tag{1.6}$$

$$T_0 = T_S - T_x - T_y \tag{1.7}$$

For $-\frac{\pi}{6} \leq \theta \leq \frac{\pi}{6}$

where m_a is the modulation index, given by

$$m_a = \frac{I_{ref}}{n i_L} = \frac{I_m}{i_P}, 0 \leq m_a \leq 1 \tag{1.8}$$

where I_m represent the peak of fundamental-frequency component in i_a.

1.4 Zero-Voltage-Switching Technique

The isolated matrix converter is widely used in high-power high-frequency applications. However, the increasing switching frequency is accompanied by the reduction of efficiency caused by increased switching losses. The switching losses can be significantly reduced or totally removed if the zero-voltage-switching (ZVS) technique can be implemented in the power circuit. The ZVS operation of full-

bridge (FB) phase-shifted PWM DC-DC converters was investigated in [49-53]. This soft-switching technique can be extended to the three-phase converters [14], [35], [48].

For an ideal power converter, if both the diode and the switch device were ideal, the switching waveforms of voltage and current should look as in Figure 1.7. There would be no overlap between the current and voltage waveforms during switching. Therefore, in an ideal case, all waveforms would be square, and there would be no switching losses.

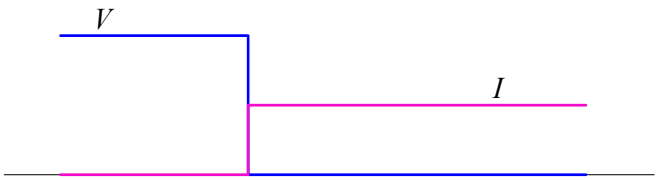


Figure 1.7 The waveforms in an ideal ZVS case.

However, in reality, the finite transistor and diode switching speed cause current-voltage overlap, and result in switching losses, switching noise, and switching stresses, especially during high-frequency applications. Figure 1.8 shows an experiment result of a hard-switching operation. The overlapping of drain-source voltage V_{ds} and gate-source voltage V_{gs}, E_{on}, causes turn-on loss. This problem can be solved if the soft-switching technique is implemented, which allows for operation at a higher frequency without sacrificing efficiency.

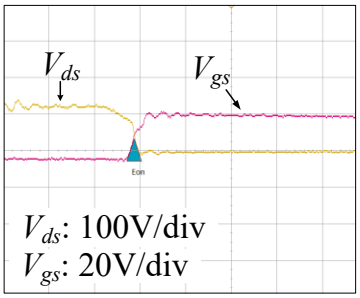


Figure 1.8 Turn-on loss.

The soft-switching is achieved by adding an auxiliary commutation network to the existing power switches, thus creating a resonance circuit between them, and

shaping the voltage across the switches. The ZVS operation of the three-phase isolated matrix rectifier is stated in Chapter 2 and Chapter 3.

1.5 Research Objectives and Thesis Organization

The isolated matrix rectifier is attractive in high-power high-frequency industry applications. The soft-switching technique can significantly decrease or totally remove the severe switching loss caused by high-switching frequency. The existing PWM schemes have the drawback of two hard-switching actions in each switching cycle. The research objective of this thesis to remove the hard-switch actions and achieve ZVS operation for all switches.

In 6-segment PWM schemes, the vector transitions between zero vector and active vector are all under ZVS. However, the vector transitions between two active vectors have one hard-switch action. Inspired by this phenomenon, a PWM scheme with all vector transitions between zero vector and active vector is proposed. In this manner, all vector transitions are under ZVS. The comparison between the three PWM schemes is also carried out.

The organization of this thesis is as follows. Chapter 2 describes a comprehensive review of existing PWM schemes for ZVS operation of the three-phase isolated matrix-type rectifiers, including the traditional 8-segment PWM scheme, and 6-segment PWM scheme. Their operation principles, steady-state analyses, and ZVS operations are presented, addressing their features and drawbacks. Chapter 3 illustrates details of the proposed 8-segment PWM scheme. Chapter 4 presents the comparison between the three PWM schemes. Chapter 5 presents the simulation and experiment results verifying the effectiveness of the proposed PWM scheme. The conclusions of the research and future work are presented in Chapter 6.

Chapter 2

Review of Existing PWM Schemes

The desirable ZVS PWM schemes for the three-phase buck type matrix-based rectifier should meet the following requirements:

- By using circuit inductance and devices junction capacitance and switch's body diodes to permit the switching devices to operate under zero-voltage switching;
- Transformer primary voltage must be alternating positive and negative in high-frequency;
- Low primary side switching loss;
- High switching frequency;
- Unity input displacement factor;
- Low harmonic distortion of input currents;
- Tight output voltage regulation;
- High-efficiency and high-power density.

Before discussing the proposed PWM scheme in this work, available PWM methods in literature are reviewed in this chapter. Their features and drawbacks are discussed. Section 2.1 presents the traditional 8-segment PWM scheme. Section 2.2 introduces a 6-segment PWM scheme. The disadvantages of these two types of PWM scheme are briefly analyzed.

2.1 Traditional 8-Segment PWM Schemes [34], [35]

The traditional 8-segment PWM scheme is firstly proposed in [34], [35]. The modulation method used in this PWM scheme is space vector modulation (SVM). The switching sequence is $\overrightarrow{I_{x+}}, \overrightarrow{I_0}, \overrightarrow{I_{x-}}, \overrightarrow{I_0}, \overrightarrow{I_{y+}}, \overrightarrow{I_0}, \overrightarrow{I_{y-}}, \overrightarrow{I_0}$, during interval of $-30^\circ \leq \theta < 0^\circ$, and $\overrightarrow{I_{y+}}, \overrightarrow{I_0}, \overrightarrow{I_{y-}}, \overrightarrow{I_0}, \overrightarrow{I_{x+}}, \overrightarrow{I_0}, \overrightarrow{I_{x-}}, \overrightarrow{I_0}$ during interval of $0^\circ \leq \theta < 30^\circ$. This switching

sequence is denoted as SQ_1. The operation principle and commutation of the PWM scheme are described in the following sections.

2.1.1 Principle of Operation

Within any 60˚ interval between two successive zero crossing of input phase voltages as shown in Figure 2.1, there are two input line voltages do not change sign.

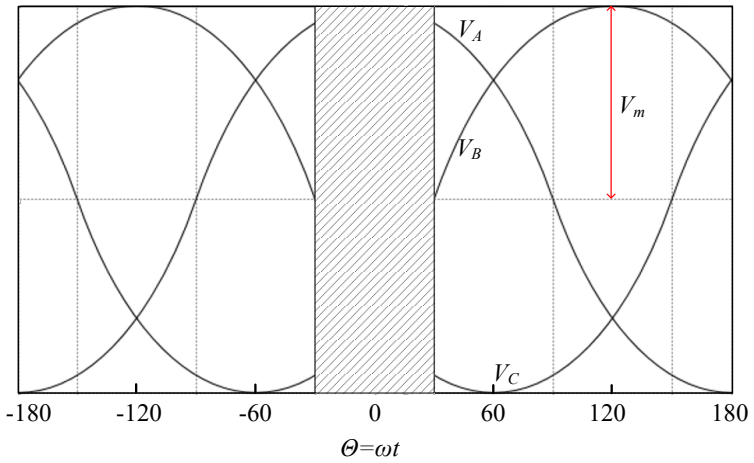
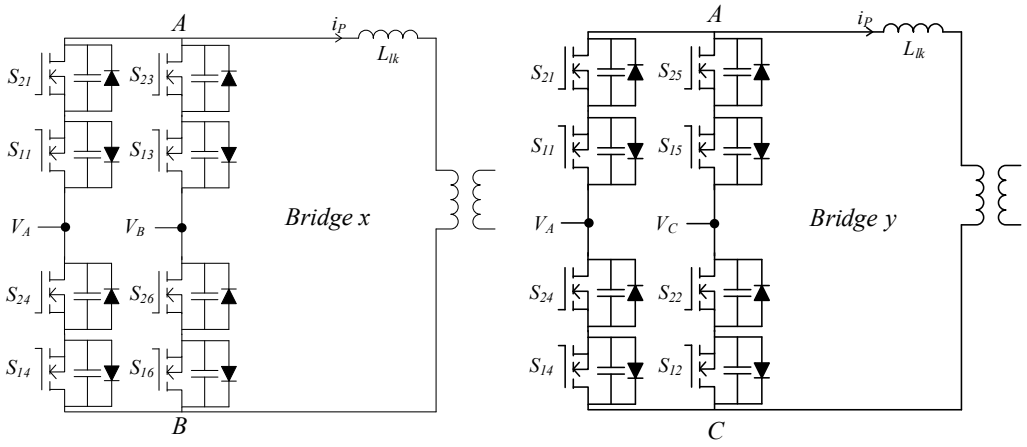


Figure 2.1 Input phase voltages.

For example, in sector I, -30˚ < θ < 30˚ interval, the shade area in Figure 2.1, the line voltages $v_{AB} = v_A - v_B$, and $v_{AC} = v_A - v_C$ are positive, and they both attain their maximum in this interval. The two line voltages can be treated as slowly varying dc voltages because that the switching frequency of the matrix converter is much higher than line frequency. Therefore, within any 60˚ interval, the three-phase to single-phase matrix converter can be analyzed as two full-bridge (FB) converter sub-topologies operating alternatively within the switching cycle [49-53]. In each sector, one of the phase legs which has the extremum voltage potential is shared by the two sub-topologies. For example, in sector I, phase *A* has the highest voltage potential so it is the common leg of sub-topology *x* and sub-topology *y*, as shown in Figure 2.2(a) and Figure 2.2(b) respectively. The active vectors $\overrightarrow{I_{x+}}$ and $\overrightarrow{I_{x-}}$ are generated by sub-topology *x* while active vectors $\overrightarrow{I_{y+}}$ and $\overrightarrow{I_{y-}}$ are generated by sub-topology *y*. The zero vector $\overrightarrow{I_0}$ are generated by turning on all the switches in one

of the three phases.



(a) Sub-topology *x* (b) Sub-topology *y*

Figure 2.2 Two sub-topologies similar to the ZVS-FB-PWM converter.

In the 8-segment PWM scheme, the two sub-topologies are used alternatively to generate expecting waveforms according to the different sequence arrangements. Figure 2.3 shows the circuit principal waveforms within 60˚ interval, with excessively decreased switching frequency f_{sw} so that the PWM details can be observed. Different shades are used to represent different sub-topologies, which are used to generate different parts of the waveforms.

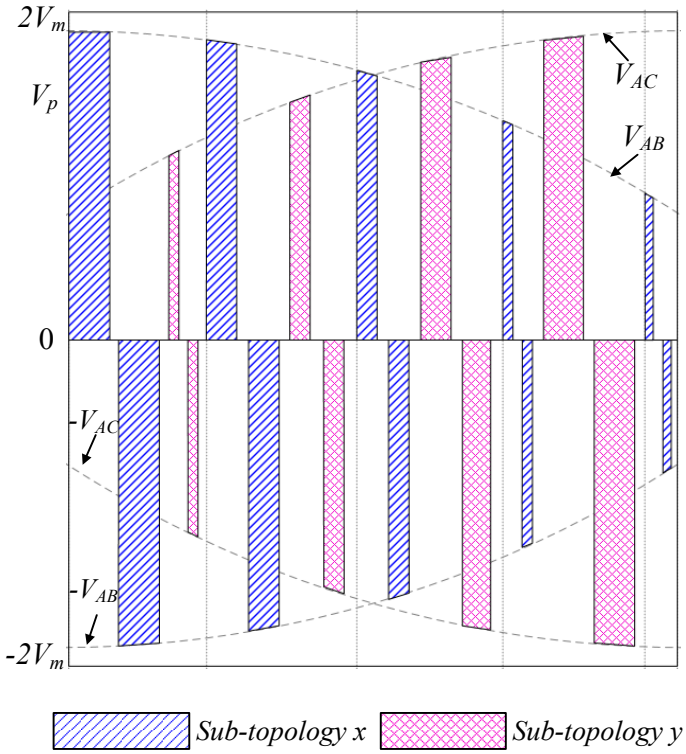


Figure 2.3 PWM waveforms: primary side voltages.

At the beginning of each switching cycle sub-topology *x* is used. The upper leg of phase A and lower leg of phase *B* are used to creating a positive voltage pulse and a current pulse flowing from phase *A* to phase *B*. Switches S_{11} and S_{16} in Figure 2.2 (a) are on during this time interval. In order to keep the transformer flux balanced, a negative voltage pulse of the same duration is next generated by turning on switches S_{26} and S_{21}. The two pulses are separated by a zero-volt interval. The time interval of the zero-volt is chosen so that the distance between adjacent pulses is even throughout the switching cycle. In the remaining part of the switching cycle, the sub-topology *x* is used to create another two voltage pulses across points *A* and *B* and two current pulses flowing from phase *A* into phase *B*. Every adjacent voltage pulses are separated by a zero-volt interval.

The complete operation of the three-phase circuit during a high-frequency switching period is illustrated in Figure 2.4 and Figure 2.5. Figure 2.4 shows the transformer primary side voltage V_P and current i_P, the rectified secondary side voltage V_S, and current of phase *A*, i_a. The gate drive signals for all twelve switches

are shown in Figure 2.5 with the same time scale. Figure 2.5(a) illustrates the operation of the sub-topology *y*, and Figure 2.5(b) shows the operation of the sub-topology *x* (the gate signals for switches S_{11} and S_{24} are repeated for clarity).

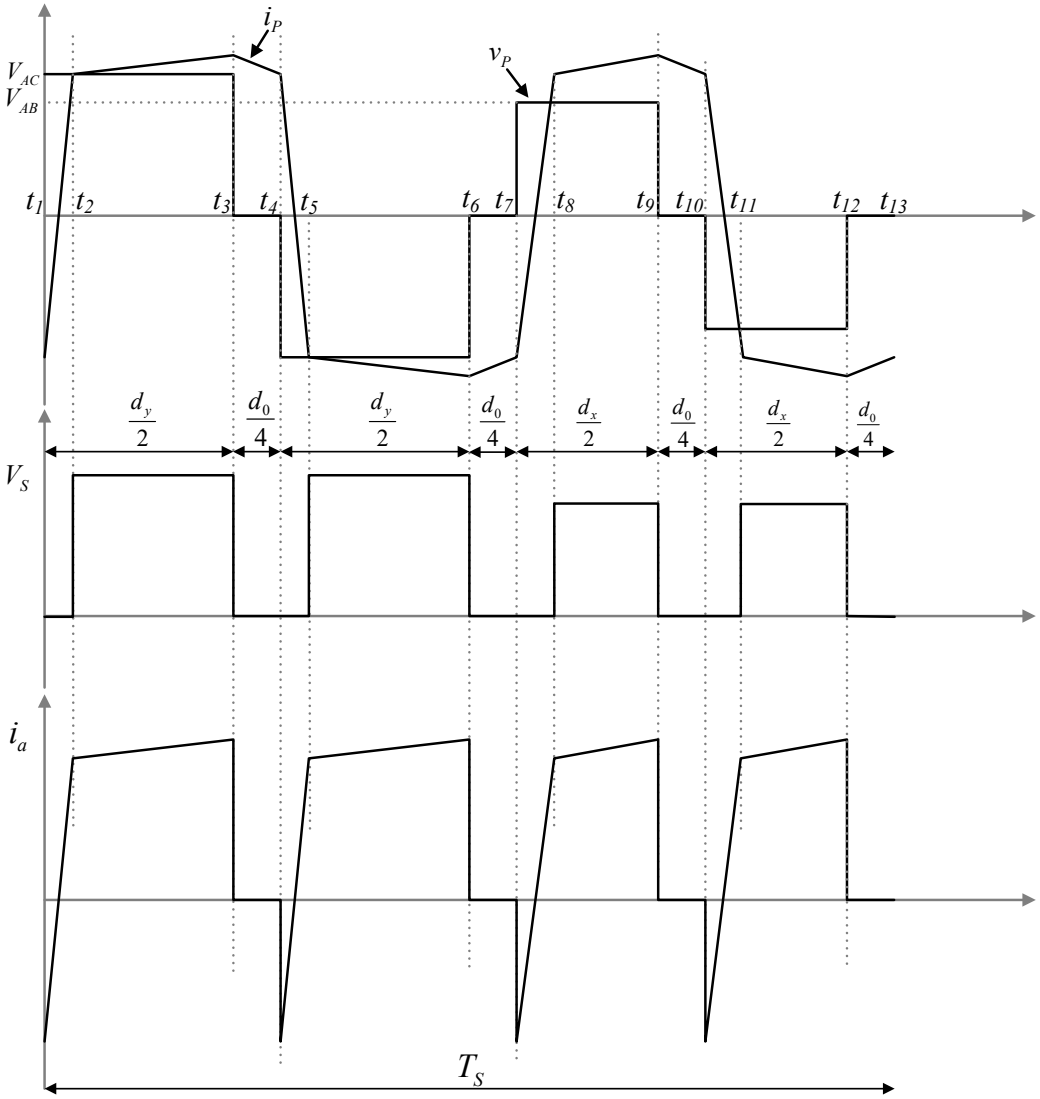


Figure 2.4 Circuit waveforms: Primary voltage (top), rectified secondary voltage (middle), and current of phase *A* (bottom).

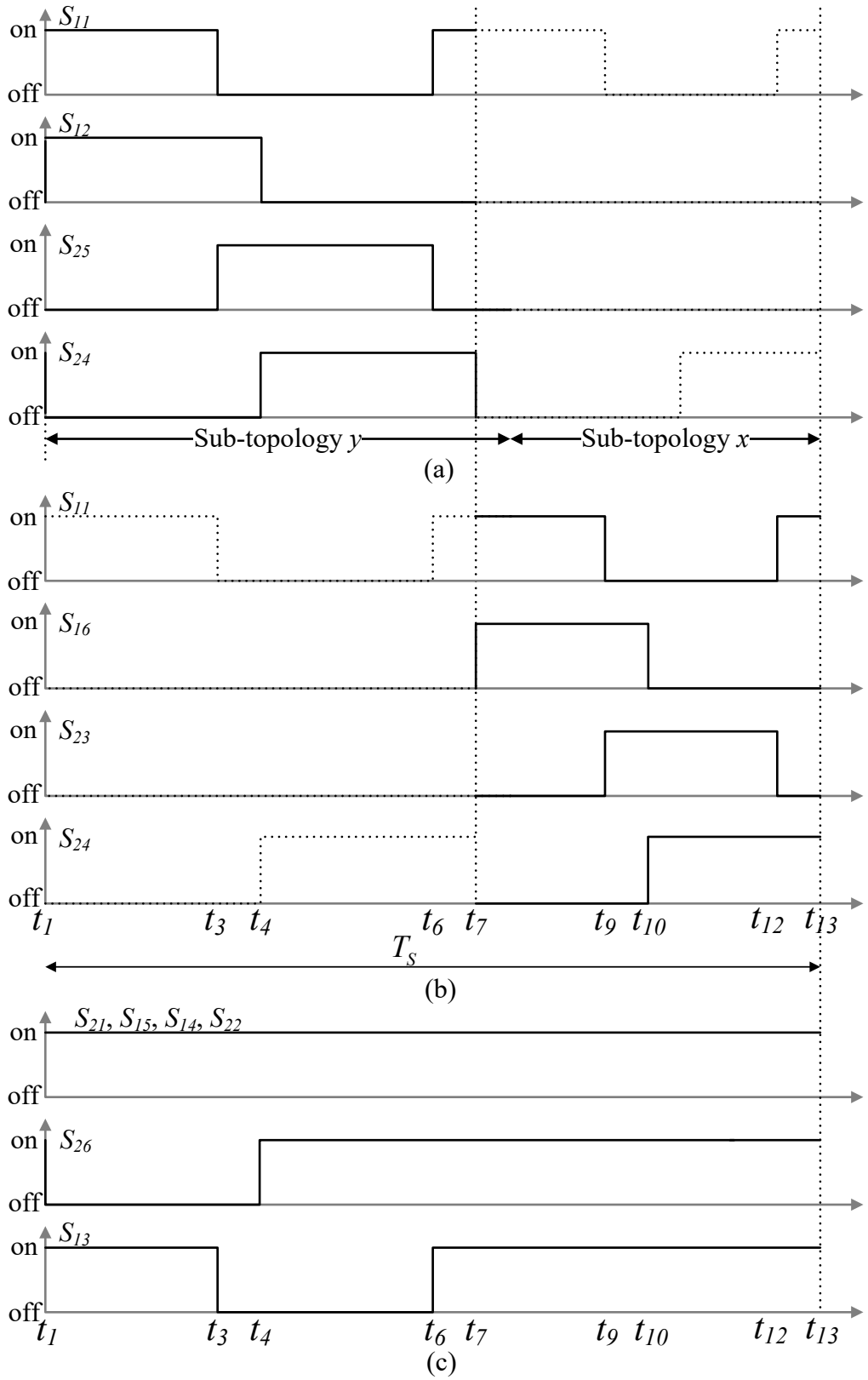


Figure 2.5 Switch gate drive waveforms during switching period in Figure 2.4: (a) Sub-topology y gate signals, (b) sub-topology *x* gate signals, (c) remaining gate signals.

From the figures above, there're only six out of twelve two-quadrant switches in the converter operate in any given 60˚ interval. The other six switches should be kept on during the entire interval. However, in a 30˚ sub-interval, there's one input phase voltage lies between the other two phase voltages, so that the two switches connected to this input phase have to be turned off when the sub-topology corresponding to this phase is not used. For example, in Figure 2.1, during $0^\circ \leq \theta \leq 30^\circ$, switches S_{21}, S_{14} in phase A, S_{13}, S_{26} in phase B, and S_{15}, S_{22} in phase C are kept on all the time. However, voltage v_B lies between v_A and v_C, that means, S_{13} and S_{26} in phase B can be kept on during the whole interval except when the switches S_{25} and S_{12}, respectively, are on, as shown in Figure 2.5 (c), when sub-topology y is used. In this way, it prevents the short circuit between phase B and phase C through the antiparallel diodes of S_{23} or S_{16}, as shown in Figure 2.6. In Figure 2.6, during $0^\circ \leq \theta \leq 30^\circ$ interval, when phase B is not used, corresponding to [t_4, t_6] in Figure 2.5, if S_{13} is turned on, the current will flow in from phase B, through the antiparallel body diode of switch S_{23}, then flow out from phase C. The short circuit between phase B and phase C will destroy the MOSFET devices. During this interval, switches S_{13} and S_{26} are not switched under zero-voltage conditions. The switching loss would be analyzed in Chapter 4.

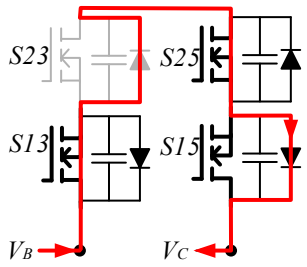


Figure 2.6 Short circuit description between phase B and phase C.

The switching states and corresponding space vectors for this PWM scheme during $0^\circ \leq \theta < 30^\circ$ interval are summarized in Table 2.1 based on the space vector modulation method, where "1" represents on-state, and "0" represents off-state.

Table 2.1. Switching states and space vectors during $0^\circ \leq \theta < 30^\circ$ of SQ_1

Space vectors	S_{21}	S_{11}	S_{24}	S_{14}	S_{23}	S_{13}	S_{26}	S_{16}	S_{25}	S_{15}	S_{22}	S_{12}
$\overrightarrow{I_{y+}}$	1	1	0	1	0	1	0	0	0	1	1	1
$\overrightarrow{I_0}$	1	0	0	1	0	0	0	0	1	1	1	1
$\overrightarrow{I_{y-}}$	1	0	1	1	0	0	1	0	1	1	1	0
$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
$\overrightarrow{I_{x+}}$	1	1	0	1	0	1	1	1	0	1	1	0
$\overrightarrow{I_0}$	1	0	0	1	1	1	1	1	0	1	1	0
$\overrightarrow{I_{x-}}$	1	0	1	1	1	1	1	0	0	1	1	0
$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0

2.1.2 Steady-State Analysis

Because of the transformer isolation and leakage inductance, the duty-cycles of the transformer primary side voltage pulses are always longer than the duty-cycles of the corresponding rectified secondary side voltage pulse, as can be seen in Figure 2.4. The duty-cycle differences are analyzed in this section, and the output current ripple is also analyzed in this section.

The analysis in this section is based on the assumption that the transformer is ideal and the forward voltage drop across all the diodes and the MOSFETs is zero. It is also assumed that the output voltage V_o is constant.

(a) Duty-cycle analysis

From Figure 2.4, the total duty-cycle of primary side voltage v_P is defined as

$$d(\theta) = d_x(\theta) + d_y(\theta) \tag{2.1}$$

where $d_x(\theta)$ and $d_y(\theta)$ represent the sum of duty-cycles of the voltage pulses created by sub-topology *x* and sub-topology *y*, respectively. The duty-cycle of the four voltage pulses are $d_y(\theta)/2$, $d_y(\theta)/2$, $d_x(\theta)/2$, and $d_x(\theta)/2$, correspondingly. The four pulses are separated by four zero-volt intervals with equal duration of $d_0/4$ as marked in Figure 2.4. The secondary voltage duty-cycle is defined as:

$$d_s(\theta) = d_{sx}(\theta) + d_{sy}(\theta) \tag{2.2}$$

where $d_{sx}(\theta)$ and $d_{sy}(\theta)$ are the sum of duty-cycles of the two pairs of pulses in the secondary side, which can be defined as:

$$d_{sx}(\theta) = d_x(\theta) - \Delta d_x(\theta) \tag{2.3}$$

$$d_{sy}(\theta) = d_y(\theta) - \Delta d_y(\theta) \tag{2.4}$$

where $\Delta d_x(\theta)$ and $\Delta d_y(\theta)$ are the duty-cycle loss of the two pairs of pulses.

The total duty-cycle loss is then defined as:

$$\Delta d(\theta) = \Delta d_x(\theta) + \Delta d_y(\theta) \tag{2.5}$$

During these duty loss intervals, the small triangular parts, t_1 to t_2, t_4 to t_5, etc. as shown in Figure 2.4 bottom figure, will cause input current distortion. However, the effect to the total harmonic distortion (THD) is less than 2%.

(b) Output inductor current ripple

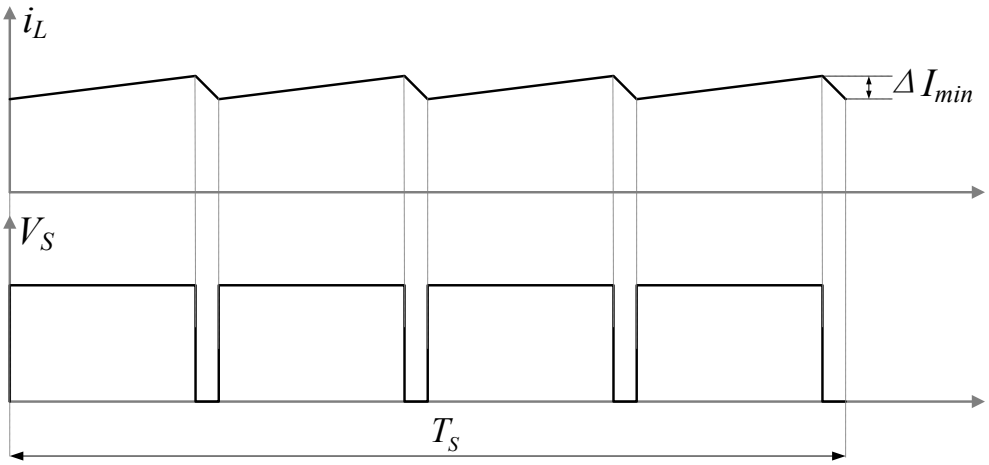
For a given output voltage, the output inductor current ripple is determined by the off-time of the secondary voltage V_S. The off-time of V_S is the dwell time of zero vectors, $d_0(\theta)$, and the duty-cycle loss time intervals, $\Delta d(\theta)$. For the current ripple analysis, it is assumed that the duty-cycle loss Δd is relatively small and can be ignored. It is necessary to know at which phase angle θ of the input voltage does the dwell time of zero vectors reach its extremum, thereby, the output filter current ripple reaches its maximum and minimum points. Figure 2.7 shows the secondary voltage and the corresponding output current ripple for θ=0 and θ=π/6, respectively. At θ=0˚, since $v_{AB} = v_{AC}$, secondary voltage V_S consists of four equal-amplitude voltage pulses evenly distributed within one switching cycle T_S. The duty-cycle of each voltage pulse is $m_a/4$, where m_a is the effective modulation index. In this case, the total off-time of the secondary voltage V_d is minimum and is given by (1-m_a)T_S. Therefore, the current ripple is minimum, as shown in Figure 2.7 (a), is given by

$$\Delta I_{min} = \frac{V_o(1-m_a)T_S}{4L_o} \tag{2.6}$$

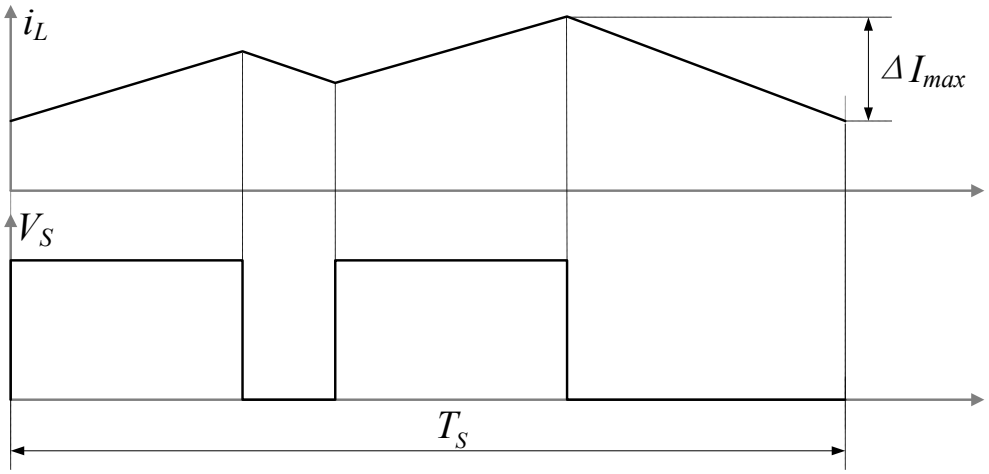
At $\theta = \pi/6$, secondary voltage V_S consists of two voltage pulses, each having a

duty-cycle of $(\sqrt{3}m_a)/4$. The other pair of voltage pulses disappear, so the three zero vectors merged into one large interval, as shown in Figure 2.7 (b). The total off-time of the secondary voltage V_S is $(1-\sqrt{3}m_a/2)T_S$. The maximum current ripple can be derived by:

$$\Delta I_{max} = \frac{3V_o(1-\sqrt{3}m_a/2)T_S}{4L_o} \tag{2.7}$$



(a) θ=0



(b) θ=π/6

Figure 2.7 Output inductor current ripple.

2.1.3 ZVS Operation

The ZVS operation by using the SQ_1 PWM scheme are analyzed in this section. The analysis in this section was not presented in the reference papers, which is

according to the operation in Figure 2.5 in Section 2.1.1. It should be noted that in the same switching cycle, the bypassing circuit are through different phase legs, that is, the switching states corresponding to four zero vectors are different. The analysis is focus on the first half cycle in sector I (b), corresponding to interval $0^{\circ} \leq \theta \leq 30^{\circ}$. The operations in second half cycle and the rest sectors are similar to the presented half cycle. The MOSFET parasitic capacitors and diodes are denoted by C_{xx} and D_{xx}. For example, the parasitic capacitor and diode of S_{11} are denoted as C_{11} and D_{11}, respectively.

Mode 0: Before starting the switching cycle, the current is freewheeling through phase A, and is in negative direction, as shown in Figure 2.8 (a). The transformer primary side voltage V_P is clamped to zero. The corresponding current vector is $\overrightarrow{I_0}$.

Mode 1: This mode starts when switch S_{24} is turned off. It starts the charging/discharging between leakage inductance L_{lk} and parasitic capacitances C_{24}, C_{26}, C_{16} and C_{12}. When voltage across S_{12} reaches zero, D_{12} conducts, as shown in Figure 2.8 (b) and (c). In order to achieve ZVS operation, the energy stored in leakage inductance should be large enough to charge the equivalent capacitance of the four capacitors. Before the primary current i_p changing direction, S_{12} can be turned on under ZVS, as shown in Figure 2.8 (d).

Mode 2: At this mode, the primary current i_p changes direction from negative to positive, and flows through S_{11}, D_{21}, S_{12}, D_{22}. The current vector is $\overrightarrow{I_{y+}}$. The transformer primary side voltage V_P is clamped to v_{AC}, as shown in Figure 2.8 (e).

Mode 3: This mode starts when S_{11} is turned off. The energy stored in leakage inductance starts charging/discharging C_{11}, C_{13}, C_{23}, and C_{25} (Figure 2.8 (f)). When voltage across S_{25} reaches zero, D_{25} starts conducting (Figure 2.8 (g)). Then, S_{25} could turn on at zero voltage (Figure 2.8 (h)). The primary voltage is clamped to zero. The current vector is $\overrightarrow{I_0}$, and the current is bypassed by phase C, instead of phase A, which has maximum voltage potential.

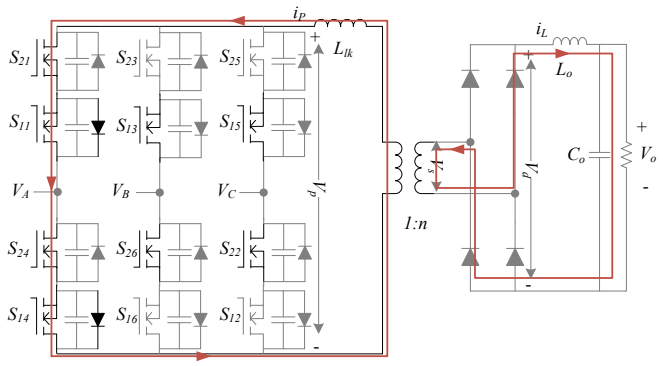
Mode 4: At the time S_{12} turns off, S_{26} turns on under hard-switching condition

to prepare for next step. Then, the energy transferring between L_{lk} and C_{24}, C_{16}, and C_{12} starts (Figure 2.8 (i)). When voltage across C_{24} discharged to zero, D_{24} conducts (Figure 2.8 (j)). At the end of this mode, S_{24} turns on under ZVS (Figure 2.8(k)).

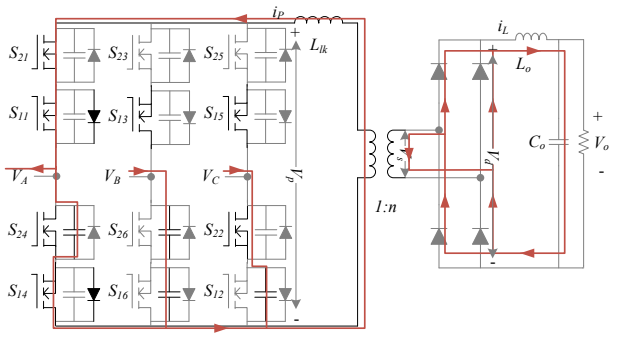
Mode 5: The primary current i_P changes direction. The current vector is $\overrightarrow{I_{y-}}$, as shown in Figure 2.8 (l). The primary voltage V_P is clamped to $-v_{AC}$.

Mode 6: This mode starts when S_{25} turns off and S_{13} turns on (Figure 2.8(m)). The voltage across S_{11} will reach zero due to the energy transferring between the inductance and capacitances. Then, D_{11} starts conducting (Figure 2.8(n)), and S_{11} can turn on under ZVS. It should be noted that S_{13} is turned on under non-ZVS condition. The current vector is $\overrightarrow{I_0}$.

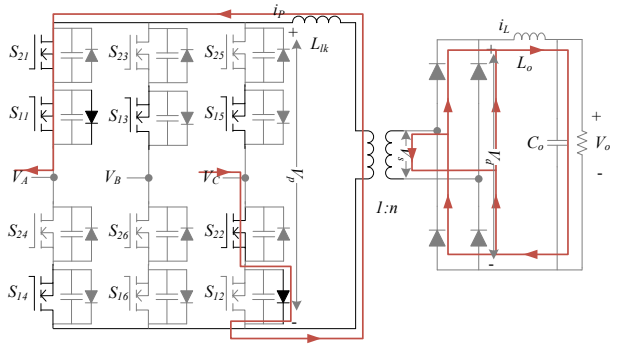
This completes the first half cycle ZVS operation. In the second half cycle, the bypassing phase is phase *B* and phase *A*. The three phases are all used as bypassing circuit in one switching cycle. The operation in rest sectors are similar to the presented half cycle.



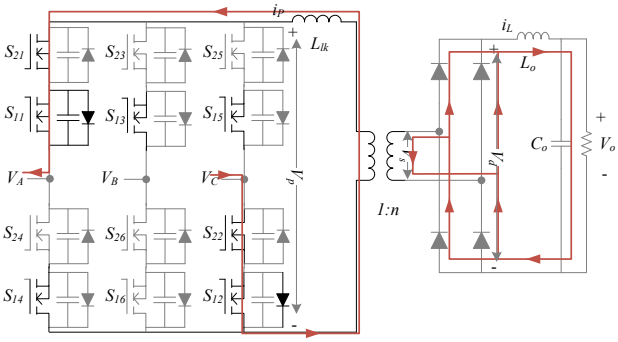
(a) Current vector $\overrightarrow{I_0}$



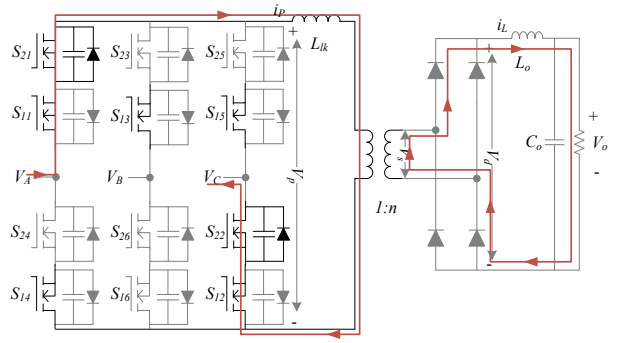
(b) Energy transferring between inductor and capacitors



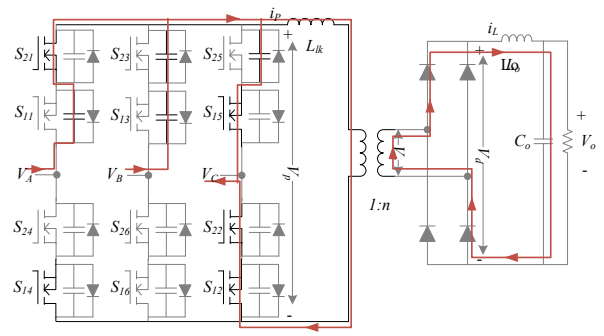
(c) Diode conducts



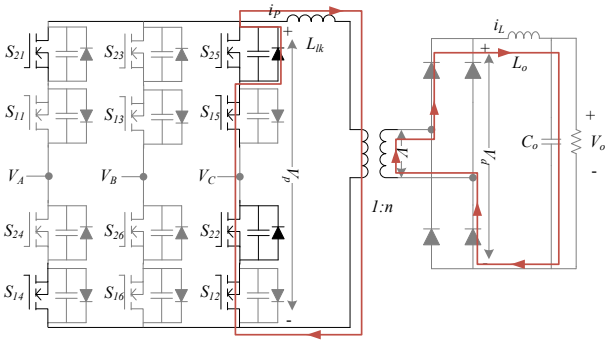
(d) S_{12} turns on at ZVS



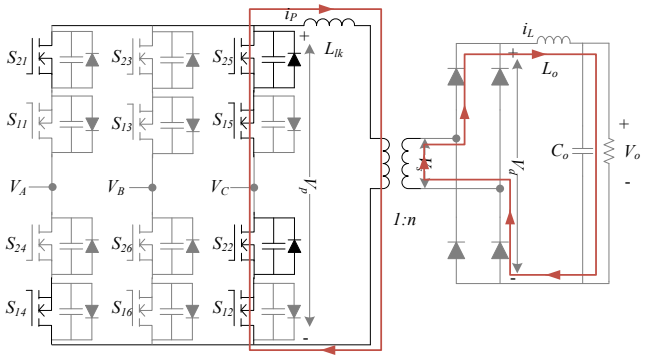
(e) Primary current changes direction, current vector $\overrightarrow{I_{2+}}$



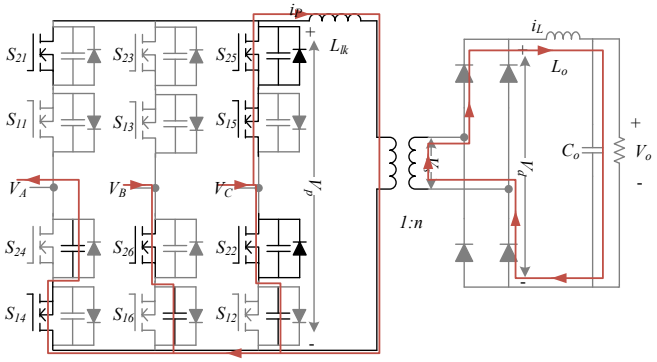
(f) Energy transferring between inductor and capacitors



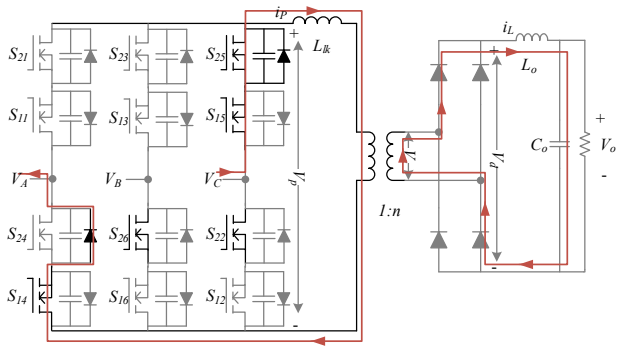
(g) Diode conducts



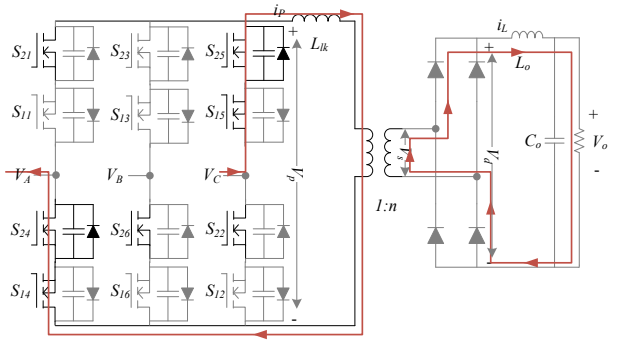
(h) Current vector $\overrightarrow{I_0}$



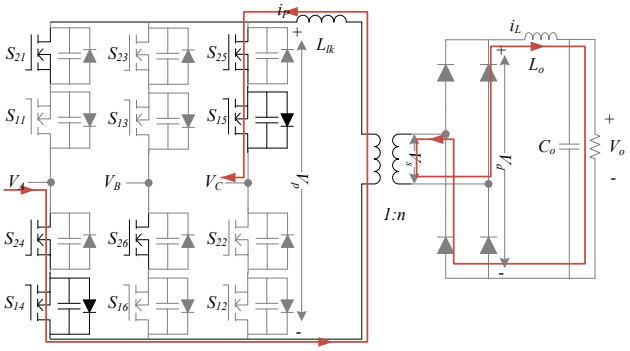
(i) S_{26} turns on when S_{24} turns off



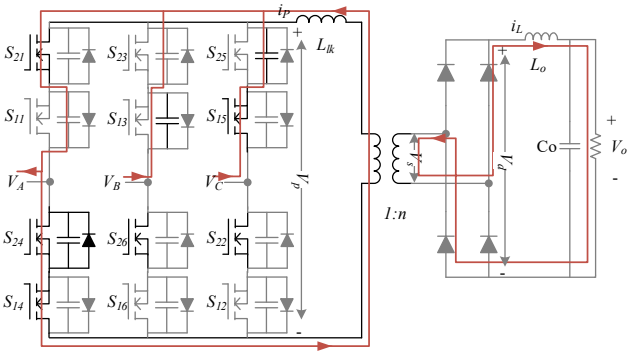
(j) Diode conducs



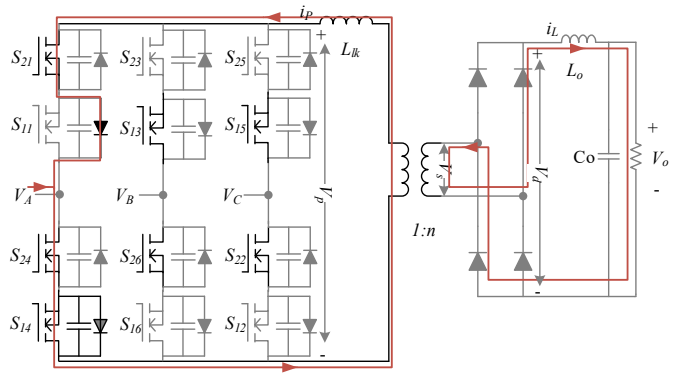
(k) S_{24} turns on at ZVS



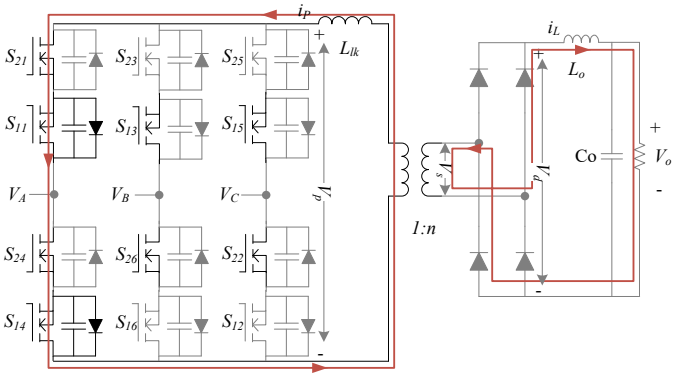
(l) Current vector $\overrightarrow{I_{2-}}$



(m) Energy transferring between inductor and capacitors



(n) Diode conducts



(o) S_{11} turns on at ZVS

Figure 2.8 ZVS operation of SQ_1.

2.2 6-Segment PWM Schemes [14], [48]

Based on the same idea as the 8-segment PWM scheme, by rearranging the operating sequence of sub-topology *x* and sub-topology *y*, different PWM scheme can be generated. The switching patterns can be identified by the transformer primary side voltage waveforms. 6-segment switching patterns are identified by the transition between two adjacent active vectors. A high to low (HTL) pattern, which means the step change of transformer primary voltage caused by vector transition from higher voltage magnitude to lower voltage magnitude, is the most commonly practiced 6-segment pattern [14], [48]. This switching pattern is denoted as SQ_2.

2.2.1 Principle of Operation

With the same idea of SQ_1, the 6-segment PWMs can also be analyzed as two

full-bridge (FB) sub-topologies [49-53]. The PWM details with excessively increased switching period can be observed in Figure 2.9. In sector I (a), interval -30˚ ≤ θ < 0˚, the current flows through sub-topology *x* from phase *A* into phase *B* creating a positive voltage pulse $V_P = v_{AB}$. Then, MOSFETs S_{11}, S_{21}, and S_{12}, S_{22} of sub-topology *y* turn on creating another voltage pulse $V_P = v_{AC}$ and current flow through phase *A* into phase *C*. In order to keep the transformer flux balanced, negative voltage pulses with same duration should be generated next. In sector I (b), during interval 0˚ ≤ θ < 30˚, the sequence of two sub-topologies is swapped in order to achieve ZVS operation of switches in high to low (HTL) pattern.

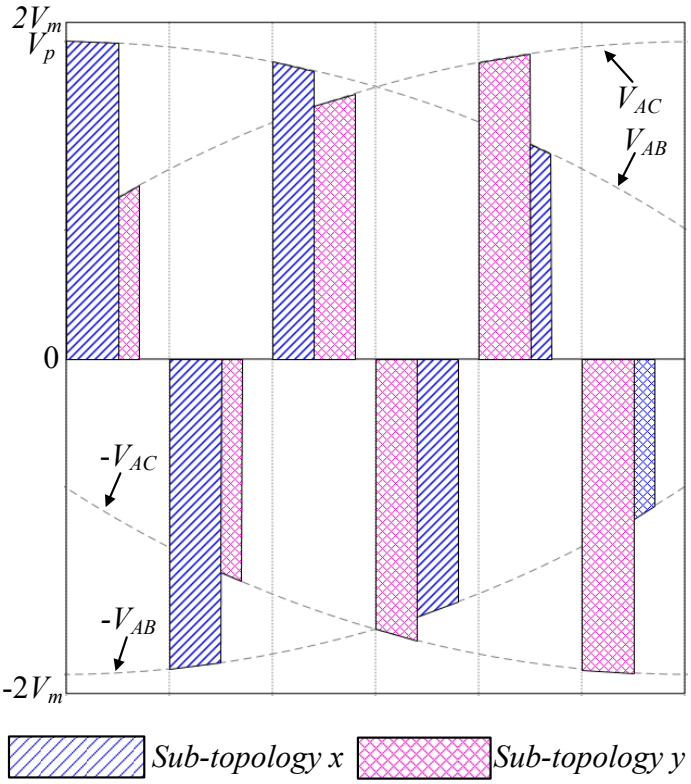
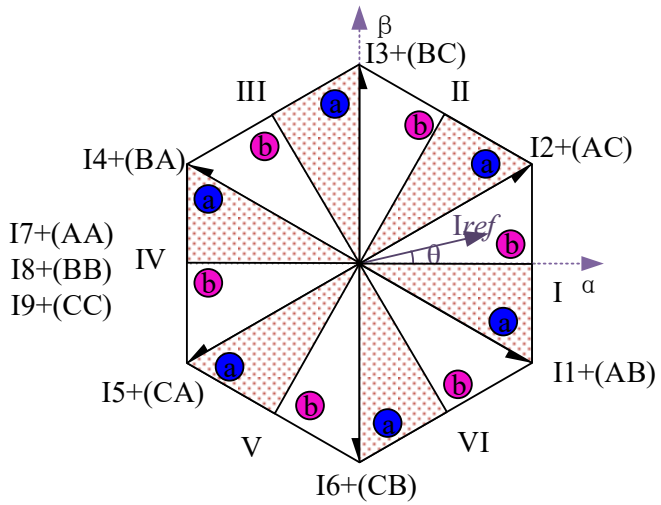


Figure 2.9 6-segment PWM waveforms with excessively increased switching period T_S.

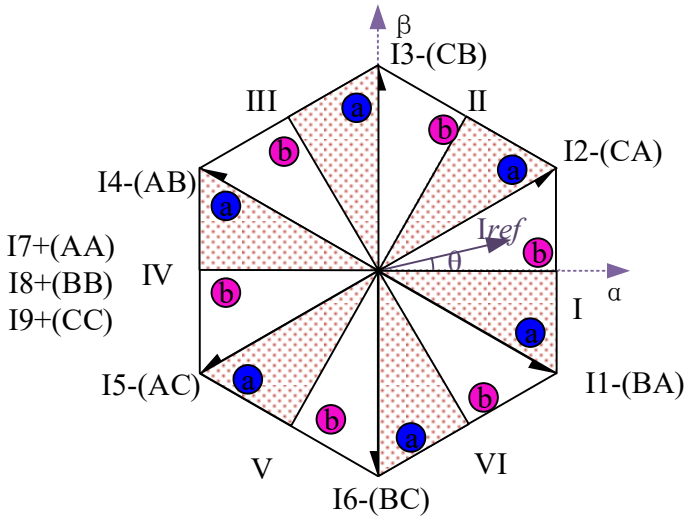
Space vector modulation (SVM) technique is used at input and output voltage regulation to achieve unity power factor. The SVM technique is stated in Chapter 1.

The space vector diagrams of SQ_1 and SQ_2 are the same, and are shown in Figure 2.10. In Figure 2.10, the space vector is divided into six large sectors, and each

sector is divided into ‘a’ and ‘b’ sub-sectors. In each sector, the switching sequence in the two parts are swapped, and the switching states are different.



(a) $i_P = nI_L$, $i_P > 0$



(b) $i_P = -nI_L$, $i_P < 0$

Figure 2.10 Space vector diagram of SQ_2.

To maintain volt-sec balance and use transformer isolation, the vector sequence in every sampling period is divided into $\overrightarrow{I_{x+}}$, $\overrightarrow{I_{y+}}$, $\overrightarrow{I_0}$, $\overrightarrow{I_{x-}}$, $\overrightarrow{I_{y-}}$, $\overrightarrow{I_0}$ in ‘a’ part of each sector, and $\overrightarrow{I_{y+}}$, $\overrightarrow{I_{x+}}$, $\overrightarrow{I_0}$, $\overrightarrow{I_{y-}}$, $\overrightarrow{I_{x-}}$, $\overrightarrow{I_0}$ in ‘b’ part of each sector, as shown in Figure 2.11. The corresponding dwell time would be $T_x/2$, $T_y/2$, $T_0/2$, $T_x/2$, $T_y/2$, $T_0/2$

in ‘a’ part and $T_y/2$, $T_x/2$, $T_0/2$, $T_y/2$, $T_x/2$, $T_0/2$ in ‘b’ part respectively.

The switching states and corresponding space vectors in sector I is shown in Table 2.2, where “1” and “0” represent on-state and off-state respectively.

Table 2.2. Switching states and space vectors for *SQ2* in sector I (a) and (b)

Sector	Space vectors	S_{21}	S_{11}	S_{24}	S_{14}	S_{23}	S_{13}	S_{26}	S_{16}	S_{25}	S_{15}	S_{22}	S_{12}
I(a)	$\overrightarrow{I_{x+}}$	1	1	0	1	0	1	1	1	0	1	0	0
	$\overrightarrow{I_{y+}}$	1	1	0	1	0	1	1	0	0	1	1	1
	$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
	$\overrightarrow{I_{x-}}$	1	0	1	1	1	1	1	0	0	0	1	0
	$\overrightarrow{I_{y-}}$	1	0	1	1	0	1	1	0	1	1	1	0
	$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
I(b)	$\overrightarrow{I_{y+}}$	1	1	0	1	0	1	0	0	0	1	1	1
	$\overrightarrow{I_{x+}}$	1	1	0	1	0	1	1	1	0	1	1	0
	$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
	$\overrightarrow{I_{y-}}$	1	0	1	1	0	0	1	0	1	1	1	0
	$\overrightarrow{I_{x-}}$	1	0	1	1	1	1	1	0	0	1	1	0
	$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0

In sector I (a), during -30˚ ≤ θ < 0˚, v_A>v_C>v_B, switches S_{21} and S_{14} in phase *A*, and S_{13} and S_{26} in phase *B* are kept on all the time, due to voltage forward biased. Constrains need to be applied to switches S_{15} and S_{22} to prevent short circuit between phase *B* and phase *C* for the same reason with traditional 8-segment PWM scheme. S_{15} should be complimentary to S_{23}, and S_{16} should be complimentary to S_{22}.

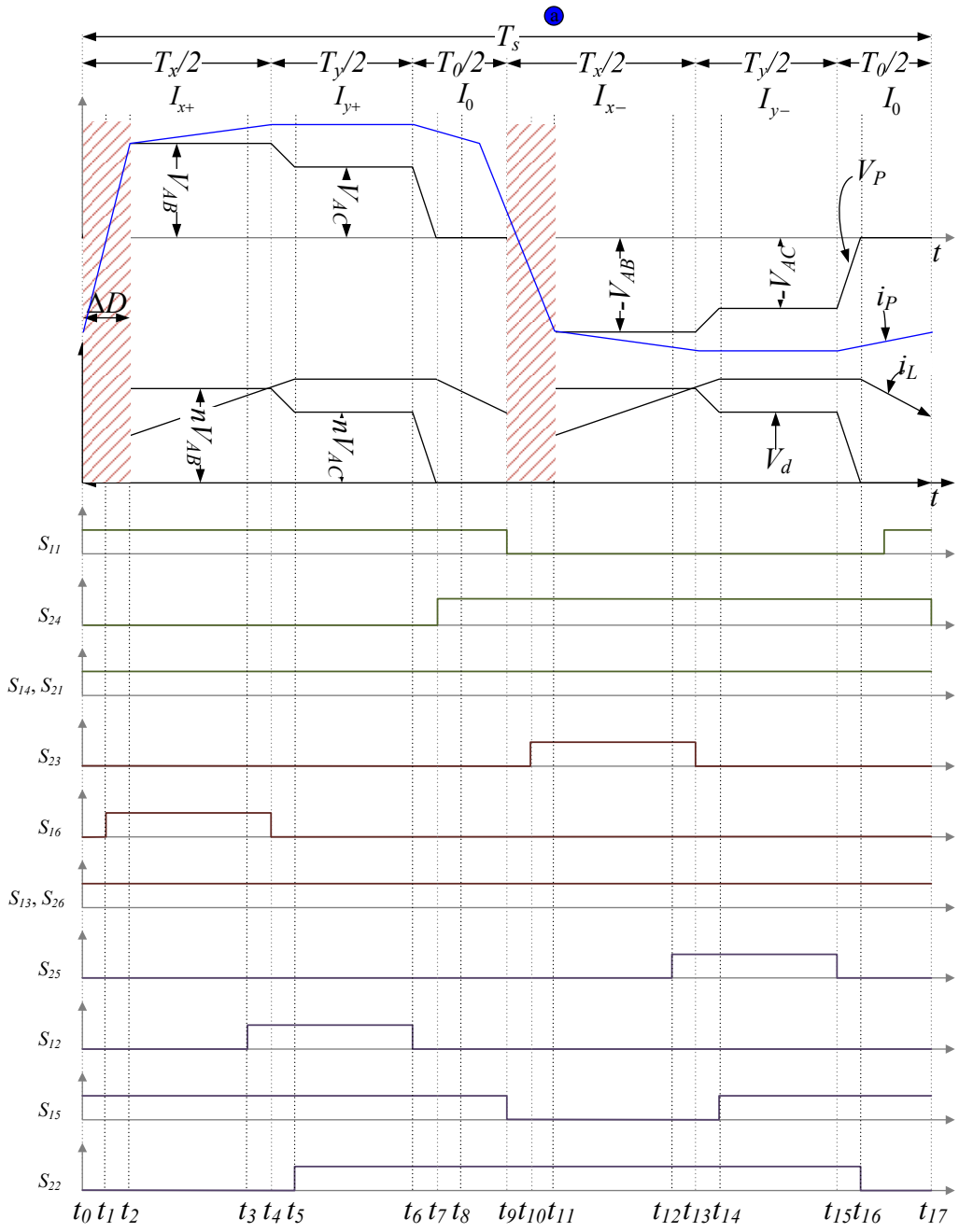
For the same reason, in sector I (b), during 0˚ ≤ θ < 30˚, v_A>v_B>v_C, switches S_{21} and S_{14} in phase *A*, and S_{15} and S_{22} in phase *C* are kept on all the time. Constrains need to be applied to switches S_{13} and S_{26} to prevent short circuit between phase *B* and phase *C*. S_{26} should be complimentary to S_{12}, and S_{13} should be complimentary to S_{25}.

2.2.2 Steady-State Analysis

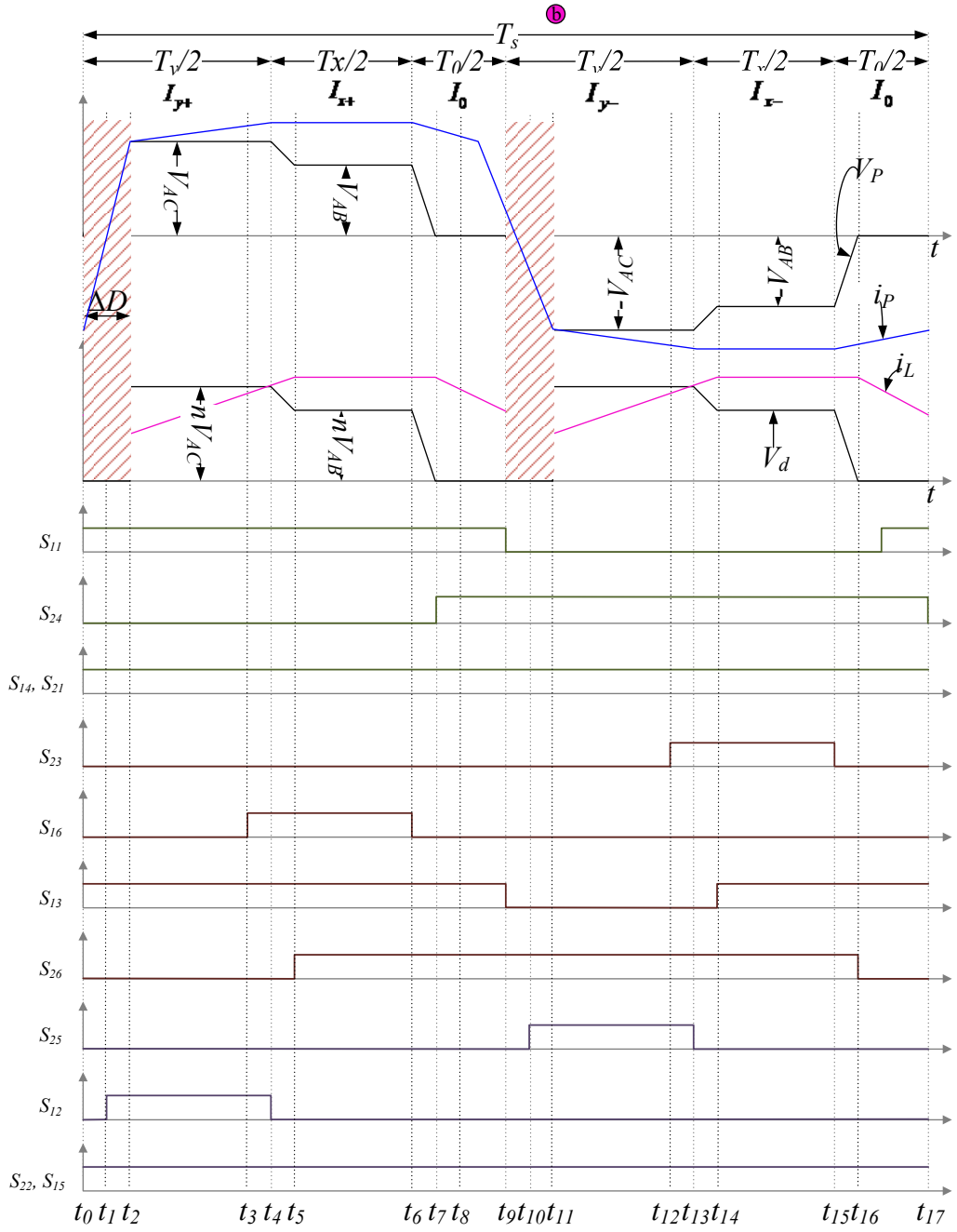
The analysis performed here is based on the assumption that the forward voltage

drop across the diodes and the MOSFETs is zero, and the rectifier diode capacitances are zero. In addition, it is also assumed that the output voltage is constant.

The complete operation of the three-phase converter during one switching period T_S by using HTL 6-segment PWM scheme is illustrated in Figure 2.11. Figure 2.11 shows the circuit waveforms of the transformer primary side voltage V_P and current i_P, the rectified secondary voltage V_d and output inductor current i_L and the all switch gate signals in sector I (a) and (b). The duty loss caused by leakage inductance can be seen in the shade areas.



(a) Sector I (a) when -30˚ ≤ θ < 0˚, $v_{AB} > v_{AC}$



(b) Sector I (b) $0^\circ \leq \theta < 30^\circ$, $v_{AC} > v_{AB}$

Figure 2.11 Circuit waveforms: primary side voltage and current, rectified secondary voltage and output inductor current and corresponding switch gate driver.

(a) Duty-cycle loss analysis

The duty-cycle loss ΔD_x, as shown in shade area in Figure 2.12, happens at vector transition from zero vectors to active vectors. During this interval, the

transformer secondary voltage V_S is clamped to zero, and the primary current i_P swing from one direction to another, as a result, the input current contains two triangles A_1 and A_2, as shown in Figure 2.12. These two areas during interval ΔD_x generate loss in the circulating current.

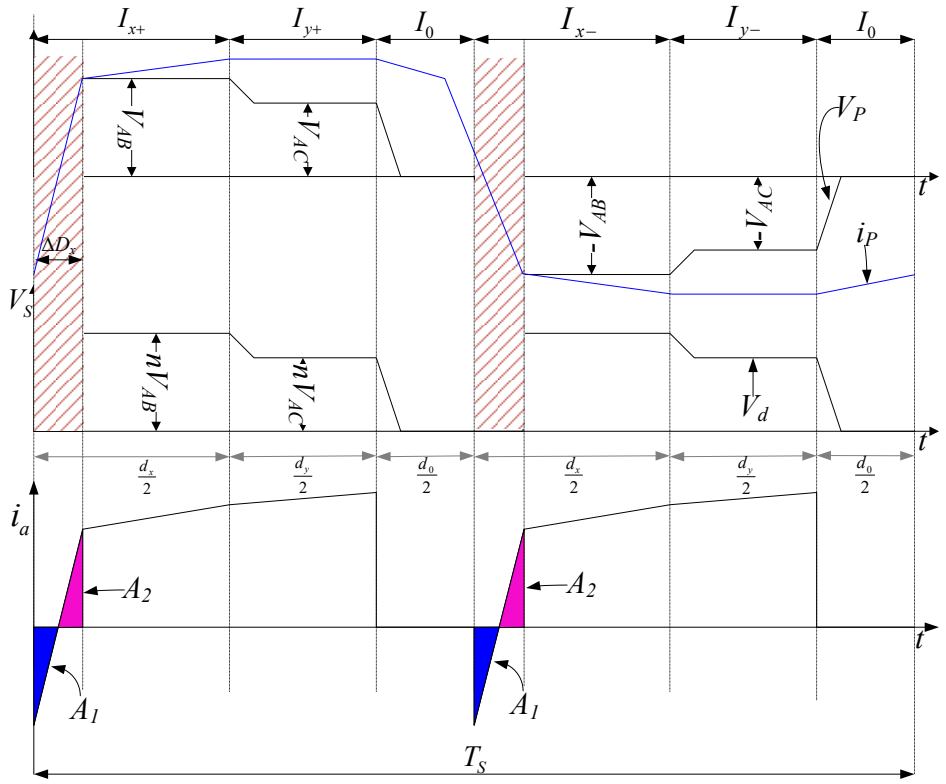


Figure 2.12 Waveforms of steady state operation in sector I(a) with 6-segment PWM scheme.

The effective cycle is lower than he applied duty-cycle duty to the duty loss. If the applied duty-cycle is in sinusoidal shape, the effective duty-cycle is distorted. However, the phase current is determined by the effective duty-cycle, so the phase current is distorted and affect the input phase current THD.

In 6-segment PWM, the vector transition from zero vector to active vector only contains $\overrightarrow{I_0}$ to $\overrightarrow{I_x}$, and only two transitions each switching cycle, so the primary duty-cycle can be denoted as

$$d_x(\theta) = d_{sx}(\theta) + 2\Delta D_x(\theta) \tag{2.8}$$

$$d_y(\theta) = d_{sy}(\theta) \tag{2.9}$$

where $d_x(\theta)$ and $d_y(\theta)$ denotes the primary side total duty-cycle of sub-topology x and y respectively, $d_{sx}(\theta)$ and $d_{sy}(\theta)$ denote the secondary side total duty-cycle of sub-topology x and y respectively, $\Delta D_x(\theta)$ denotes the duty loss caused by vector transition from zero vector to active vector.

It is assumed that the output current ripple is small compared to the load current, so that

$$i_L \cong I_o \tag{2.10}$$

where i_L is the output inductor current, and I_o is the load current.

The total duty-cycle loss of 6-segment PWM can be derived as:

$$\Delta D_{total} = 2\Delta D_x = \frac{4nI_oL_{lk}}{V_P(\theta)T_s} \tag{2.11}$$

where n is the transformer turns ratio, L_{lk} is the leakage inductance, T_s is switching period, $V_P(\theta)$ is the voltage across L_{lk} during ΔD_x, and θ is the angle displacement between $\overrightarrow{I_{ref}}$ and α-axis of α-β plane. The waveform of $V_P(\theta)$ during interval -30° $\leq \theta <$ 30° is shown in Figure 2.13. According to the PWM scheme, the solid lines in Figure 2.14 can be derived to use to calculate the duty loss. At θ=0°, the magnitude of $V_P(\theta)$ is minimum of $\frac{3}{2}V_m$, so the maximum duty loss is

$$\Delta D_{total\_max} = \frac{8nI_oL_{lk}}{3V_mT_s} \tag{2.12}$$

where V_m is the peak value of input phase voltage.

At θ=$\pm\frac{\pi}{6}$, the magnitude of $V_P(\theta)$ is maximum of $\sqrt{3}V_m$, so the minimum duty-cycle loss is

$$\Delta D_{total\_min} = \frac{4nI_oL_{lk}}{\sqrt{3}V_mT_s} \tag{2.13}$$

Because the six sectors are symmetrical, the duty-cycle range of the 6-segment PWM scheme is $[\frac{4nI_oL_{lk}}{\sqrt{3}V_mT_s}, \frac{8nI_oL_{lk}}{3V_mT_s}]$.

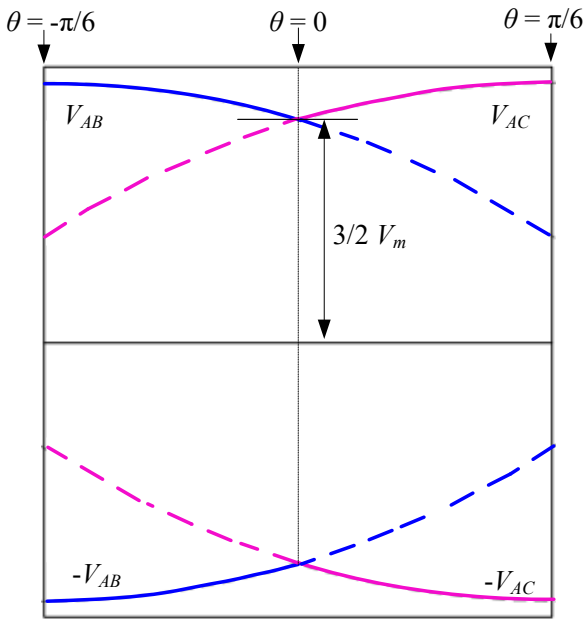


Figure 2.13 Envelope of transformer primary voltage $V_P(\theta)$.

(b) Output inductor current ripple

At θ=0˚, the off-time of secondary voltage V_d is minimum of $(1-m_a)T_s$. Therefore, the current ripple at θ=0˚ reaches minimum. Because the off-time of V_d is divided by two zero-volt intervals, the minimum current ripple is given by

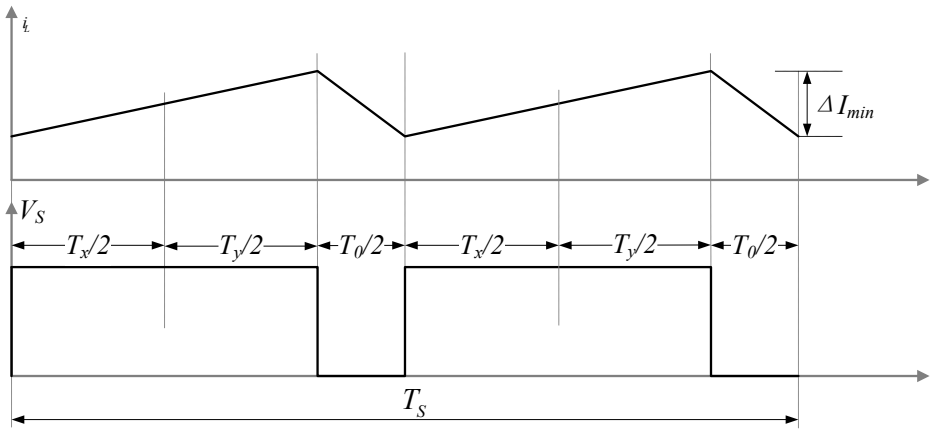
$$\Delta I_{min} = \frac{V_o(1-m_a)T_S}{2L_o} \tag{2.14}$$

The minimum current ripple of 6-segment PWM is shown in Figure 2.14 (a).

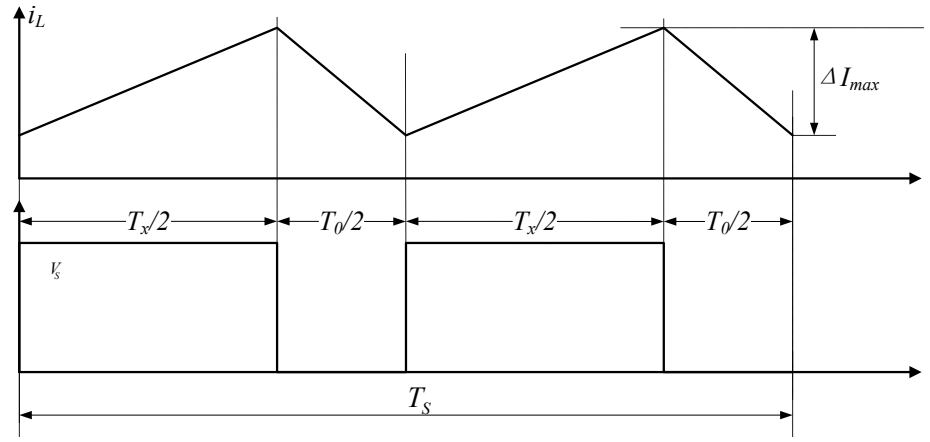
At θ=$\pm\frac{\pi}{6}$, the total off-time of V_d is maximum of $(1-\frac{\sqrt{3}}{2}m_a)T_s$, so the current ripple reaches maximum and can be derived as

$$\Delta I_{max} = \frac{V_o(1-\frac{\sqrt{3}}{2}m_a)T_S}{2L_o} \tag{2.15}$$

As shown in Figure 2.14 (b), at θ=$-\frac{\pi}{6}$, the 6-segment PWM scheme reaches maximum current ripple.



(a) At θ=0



(b) At θ=$-\frac{\pi}{6}$

Figure 2.14 Waveforms of output inductor current ripple for 6-segment PWM.

2.2.3 ZVS Operation Analysis

The ZVS operation of the MOSFET switches are analyzed by using space vector modulation technique. The analysis is for sector I (a), interval -30˚≤ θ<0˚, and the analysis in sector I (b) and the rest of other five sectors are the same with the anlysis in sector I (a). In sector I (a), the three vectors involved in the ZVS operation are $\overrightarrow{I_x} = \overrightarrow{I_1}$, $\overrightarrow{I_y} = \overrightarrow{I_2}$, and $\overrightarrow{I_0} = \overrightarrow{I_0}$. The MOSFET parasitic capacitors are denoted as C_{xx}. For example, the parasitic capacitor of S_{11} is denoted as C_{11}. And D_{xx} represents the parasitic diodes.

Mode 1: As shown in Figure 2.15 (a), before the beginning of the switching cycle, at time t_{0-} in Figure 2.11(a), the primary side current i_P is freewheeling through the

four MOSFETs in phase *A* in negative direction, and switches S_{13} and S_{26} in phase *B*, and S_{15} and S_{22} in phase *C* are in on status due to voltage potential between the three phases. The primary voltage V_P are clamped to zero. The current vector in this mode is $\overrightarrow{I_0}$.

Mode 2: At the beginning of this mode, switch S_{24} is turned off. Then, the energy stored in the inductance L_{lk} starts to charge/discharge the parasitic capacitance of S_{24}, S_{16}, S_{12}, and S_{22} because of the resonant between them, as shown in Figure 2.15 (b). The primary current i_P starts falling down towards zero. At t_1, the voltage across S_{16} reaches zero, and the parasitic diode D_{16} starts conducting, the voltage across S_{16} is clamped to zero.as shown in Figure 2.15 (c). At this time, the current i_P is still in negative direction. S_{16} turns on under zero voltage before i_P changing direction. In order to achieve ZVS operation of S_{16}, the energy stored in L_{lk} needs to be enough to charge the total capacitance of the four capacitors. The equivalent circuit of the process can be simplified as Figure 2.15 (d). The capacitors C_{12} and C_{22} are series connected and then parallel connected with C_{24} and C_{16}. The transformer parasitic capacitors also need to be considered. During this process, the source voltages are constant, so they can be considered as short circuit. The equivalent capacitances can be calculated as:

$$C_{eq} = \frac{5}{2}C_0 + C_{TR} \tag{2.16}$$

where C_0 is the output capacitance of each switch, C_{TR} is the transformer parasitic capacitor. The energy stored in L_{lk} should be enough to charge C_{eq} from t_0 to t_1 status, that is, voltage from 0 to v_{AB}. The minimum energy stored in L_{lk} required for ZVS is

$$E_{l\_min} = \frac{1}{2}L_{lk}{I_{p\_min}}^2 \tag{2.17}$$

The current I_{p_min} is the primary current i_p at the end of the off-time of each switching cycle (at θ=π/6). I_{p_min} can be determined according to a few factors: such as the desired range of ZVS operation, and the duty cycle loss due to very large leakage inductance value. The energy in the capacitance is proportional to the

square of input line voltage. To achieve ZVS for all devices, the worst case occurs when v_{AB} is at highest value, the energy at the peak of v_{AB} is

$$E_{c\_max} = \frac{1}{2}(\sqrt{3}V_m)^2 C_{eq} \tag{2.18}$$

Therefore, the minimum energy stored in L_{lk}, E_{l_min}, should be equal to the maximum energy needed by the equivalent capacitance, E_{c_max}.

Equating E_{l_min} and E_{c_max}, and solving for L_{lk}, gives

$$L_{lk} = \frac{(\sqrt{3}V_m)^2 C_{eq}}{I_{p\_min}{}^2} \tag{2.19}$$

At full load condition, the minimum value of leakage inductance, L_{lk}, is around 5.7μH. The value of L_{lk} also related to the load conditions, and it has to be adjusted to achieve desired ZVS range. At the end of this mode, the voltages across switches S_{24}, S_{26}, S_{12}, and S_{22} are v_{AB}, 0, $(v_{AC} - \frac{1}{2}v_{AB})$, $\frac{1}{2}v_{AB}$ respectively.

Mode 3: During this mode, the primary current i_P ramps up from negative to positive direction. Before i_P cross zero, S_{16} turns on at zero voltage (Figure 2.15(e)). At the end of this mode, i_P reaches i_L, and v_{AB} appears across transformer primary side. Vector transition from $\overrightarrow{I_0}$ to $\overrightarrow{I_1}$ complete (Figure 2.15(f)).

Mode 4: Current vector $\overrightarrow{I_1}$ (Figure 2.15(f)). During this mode, the current flows from phase *A* to phase *B*, and energy transfers from primary side to secondary side. Before the end of this mode, S_{12} is turned on at t_3 to prepare for the next step (Figure 2.15(g)). There is turn on loss on S_{12} because the voltage across S_{12} is not zero when it is turned on. This mode ends when S_{16} is turned off at t_4.

Mode 5: Vector transition from $\overrightarrow{I_1}$ to $\overrightarrow{I_2}$. At t_4, S_{16} is turned off, and the current i_P starts charging/discharging C_{24}, C_{16} and C_{22} (Figure 2.15(h)). The total equivalent capacitance can be calculated as

$$C_{eq} = 3C_0 + C_{TR} \tag{2.20}$$

During this interval, L_{lk} is in series with the secondary output inductor L_o, so

that the capacitors are charged/discharged by the combined energy stored in both L_{lk} and L_o. Because the energy in L_o is significantly larger than the energy stored in L_{lk}, the ZVS operation can be easily achieved in this step.

At t_5, voltage across C_{22} is discharged to zero, D_{22} starts conducting (Figure 2.15(i)). S_{22} are turned on under ZVS. At the end of this mode, vector transition from $\overrightarrow{I_1}$ to $\overrightarrow{I_2}$ completes. The transformer primary side voltage is equal to line voltage v_{AC}.

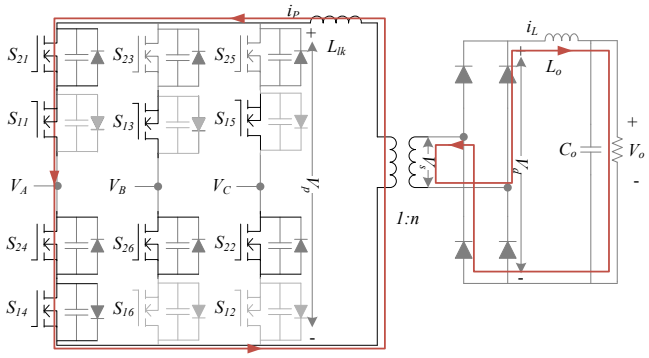
Mode 6: Current vector $\overrightarrow{I_2}$ (Figure 2.15(j)). During this mode, the energy transfers from primary side to secondary side, and the line voltage v_{AC} appears across the transformer primary side. The AC current enters into phase *A* and returns from phase *C*. this mode ends when S_{12} is turned off.

Mode 7: After S_{12} is turned off, current i_P starts charging/discharging C_{12}, C_{16} and C_{24} (Figure 2.15(k)). When voltage across C_{24} reduces to zero and D_{24} starts conducting (Figure 2.15(l)). The voltage across S_{24} are clamped to zero, then S_{24} is turned on at zero voltage.

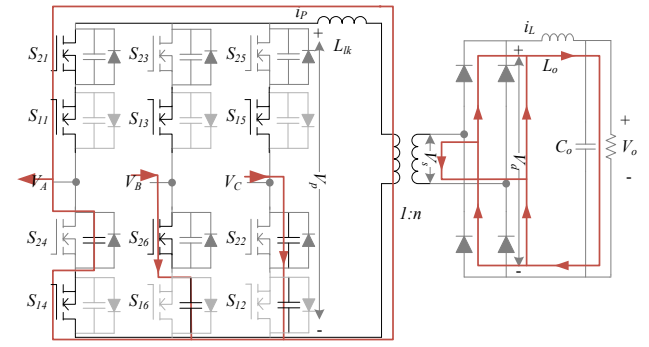
The total equivalent capacitance is the same as that in *mode 5*. And the combined energy in both L_{lk} and L_o are used to charge/discharge capacitance. The ZVS can be easily achieved in this mode.

Mode 8: Current vector $\overrightarrow{I_0}$.

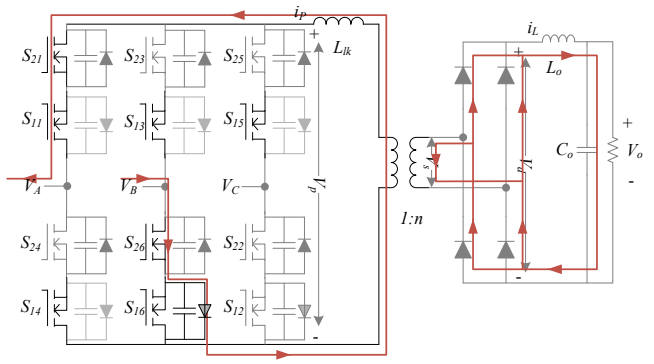
At this mode, the primary current is bypassed by phase *A* (Figure 2.15(m)). The primary voltage V_P is clamped to zero. This mode ends when S_{11} is turned off, which the half cycle operation is completed. The second half cycle operation is similar to the first half and will not be discussed here.



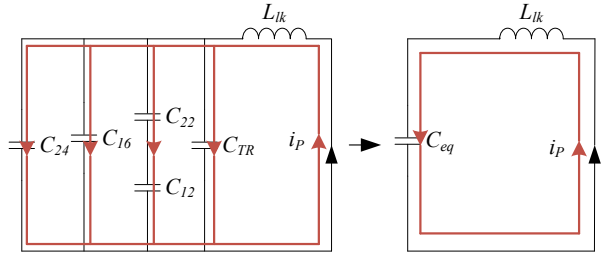
(a) At t_0-



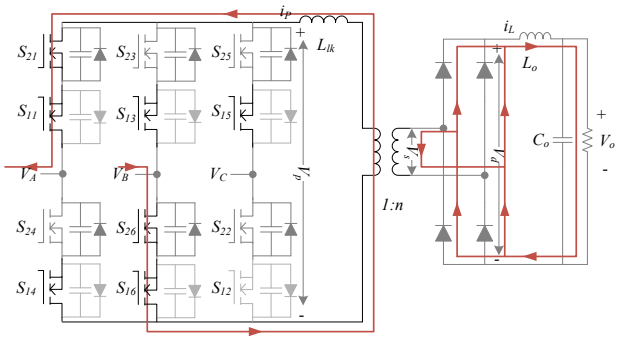
(b) At t_0-t_1



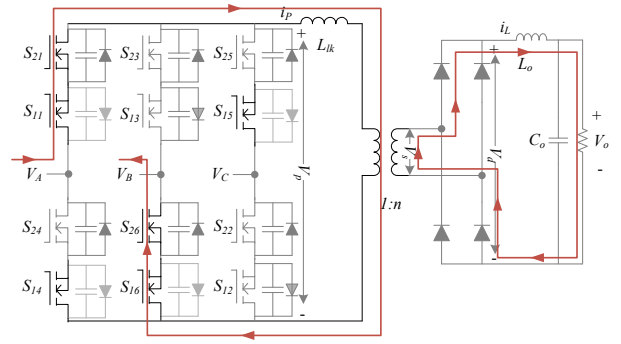
(c) Diode conducts



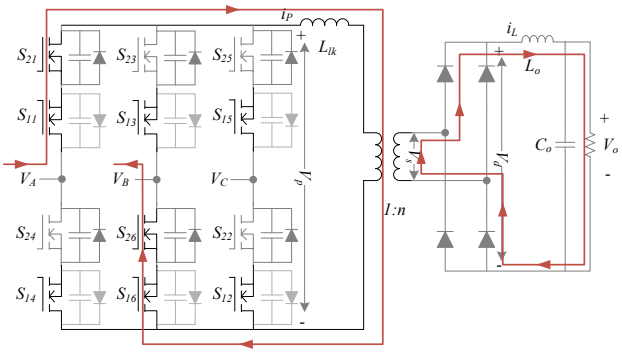
(d) Equivalent circuit of the energy transferring process



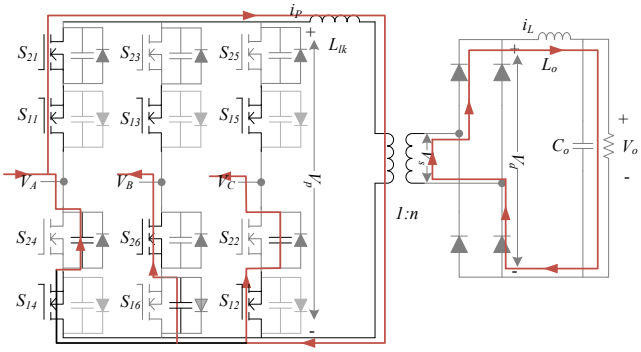
(e) S_{16} turns on at zero voltage condition



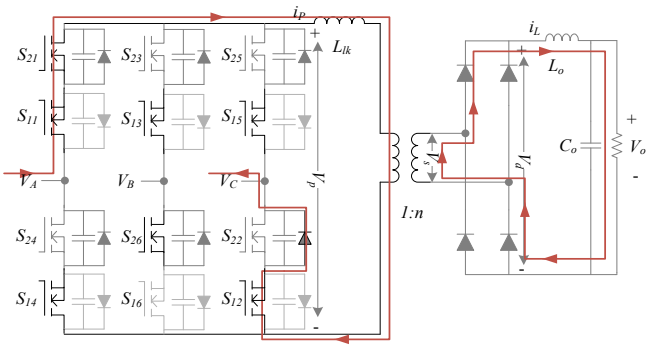
(f) Primary current i_P changes direction



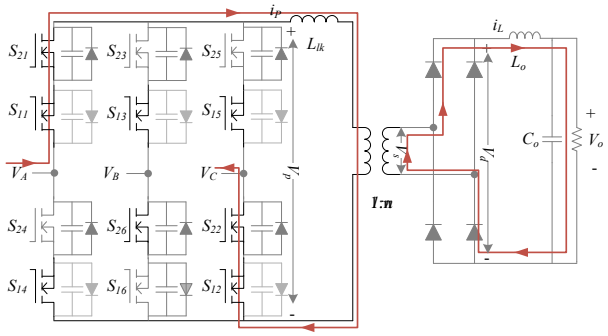
(g) Current vector $\overrightarrow{I_1}$. S_{12} turns on under non-ZVS



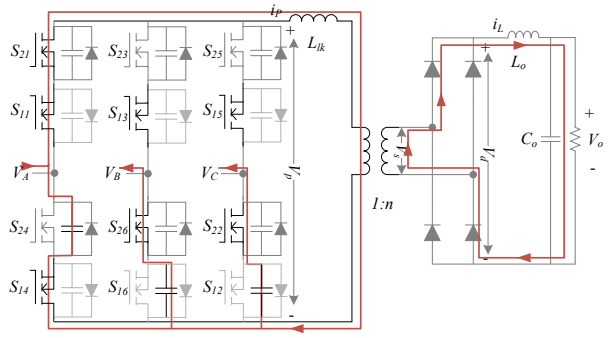
(h) At t_4-t_5



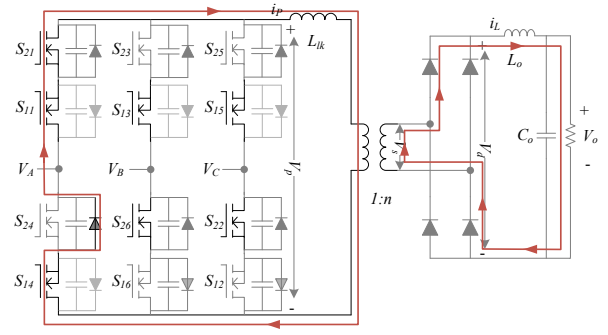
(i) D_{22} conducts



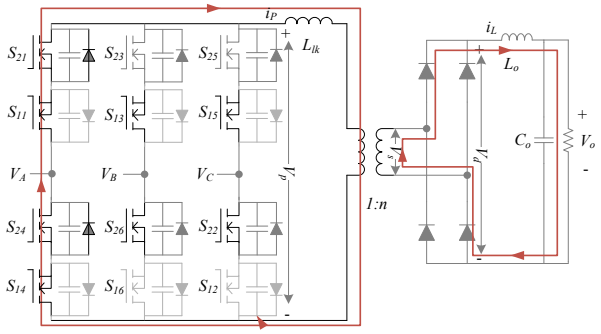
(j) Current vector $\overrightarrow{I_2}$



(k) Energy transferring between L_{lk} and parasitic capacitors



(l) D_{24} starts conducting



(m) Current vector $\overrightarrow{I_0}$

Figure 2.15 ZVS operations of SQ_2.

2.3 Summary

In this chapter, the two main ZVS PWM schemes for the three-phase isolated buck type matrix rectifier is presented. The operation principle, steady-states analysis, and ZVS operation are introduced in detail. For SQ_1, there are two hard-switch actions in each switching cycle. The minimum output inductor current ripple is lower than that of SQ_2. However, the maximum output current ripple is higher than the maximum current ripple in SQ_2. SQ_2 only has two vector transition actions from zero vector to active vector, and SQ_1 has four, so the duty-cycle loss of SQ_2 is lower than duty-cycle loss of SQ_1. For the same transformer, SQ_1 could achieve two times of the switching frequency than SQ_2.

Inspired by the ZVS operation in SQ_2 PWM, if removing the two switch actions between two active vectors, the ZVS operation for all switch actions could be achieved. By inserting a zero vector between the two active vectors, a new switching scheme by achieving all switching action operation under ZVS is proposed. The details of the proposed PWM scheme is described in Chapter 3.

Chapter 3

Proposed Improvement PWM Scheme of the Traditional 8-Segment

This chapter presents an improved PWM scheme of a traditional 8-segment PWM scheme with ZVS operation for a three-phase matrix rectifier. The switching sequence is $\overrightarrow{I_{x+}}, \overrightarrow{I_0}, \overrightarrow{I_{y-}}, \overrightarrow{I_0}, \overrightarrow{I_{y+}}, \overrightarrow{I_0}, \overrightarrow{I_{x-}}, \overrightarrow{I_0}$, denoted as SQ_3. In SQ_1, the traditional 8-segment PWM scheme, there are a total of ten switch actions in each switching cycle, including two hard-switch actions. The three phases are all utilized to bypass the current in each switching cycle. The proposed switching method has three switch actions during each vector transition, which are two turn-off actions and one turn-on action when vector transits from zero vector to active vector, and two turn-on actions and one turn-off action when vector transits from active vector to zero vector. There are a total of twelve switch actions in each switching cycle. The bypassing zero vector used in each switching cycle is the same phase leg. By pre-turn-on some unused MOSFET devices, the ZVS operation of all devices can be achieved.

The operation principle, steady-state analysis, and ZVS operations of SQ_3 are presented in detail in this chapter.

3.1 Operation Principles

For the existing PWMs, all six sectors are divided into two parts, and the switching sequence is swapped in the middle of the sector. To prevent short circuit, some constrains need to be applied to the switching states. With the proposed PWM, the switching sequence and switching states in each sector are the same, which is much easier to implement. The proposed switching method also avoids the short-circuit problem, and no constrains are needed. All switch states are decided by the

space vector and the transformer primary current direction. For example, in sector I, voltage potential v_A is always higher than v_B and v_C. Switches S_{14} and S_{21} can be kept on all the time since the body diodes are forward biased. If i_P>0, switches S_{13} and S_{15} can be kept on because the body diodes are forward biased. For the same reason, if i_P<0, switches S_{26} and S_{22} can be kept on.

The state of synchronous rectification switches is only decided by the voltage of one phase. This method not only avoids the short-circuit problem, it also can easily achieve ZVS for all switches.

Figure 3.1 shows the circuit operation waveforms within a 60˚ interval, with excessively decreased switching frequency f_{sw} so that the PWM details can be observed. Different shades are used to represent different sub-topologies, which are used to generate different parts of the waveforms.

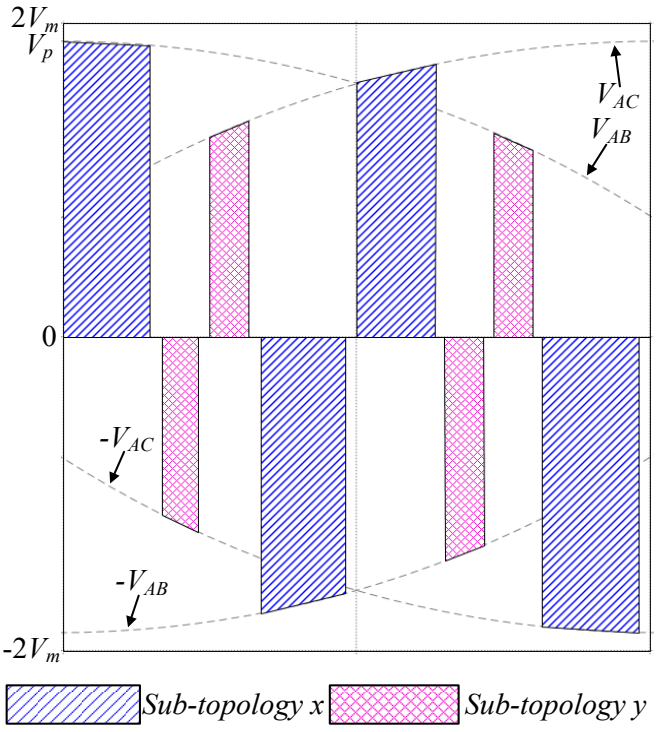


Figure 3.1 SQ_3 PWM waveforms: primary side voltages.

Figure 3.2 shows the complete operation of the three-phase converter during one switching period T_S. It shows the circuit waveforms of primary voltage V_P and

current i_p, the rectified secondary voltage V_d and output inductor current i_L and the corresponding switch gate signals in sector I. Duty loss (shaded area) caused by leakage inductance can be observed when the primary side current changes directions. Duty loss will influence effective dwell time, and that can cause grid side current distortion.

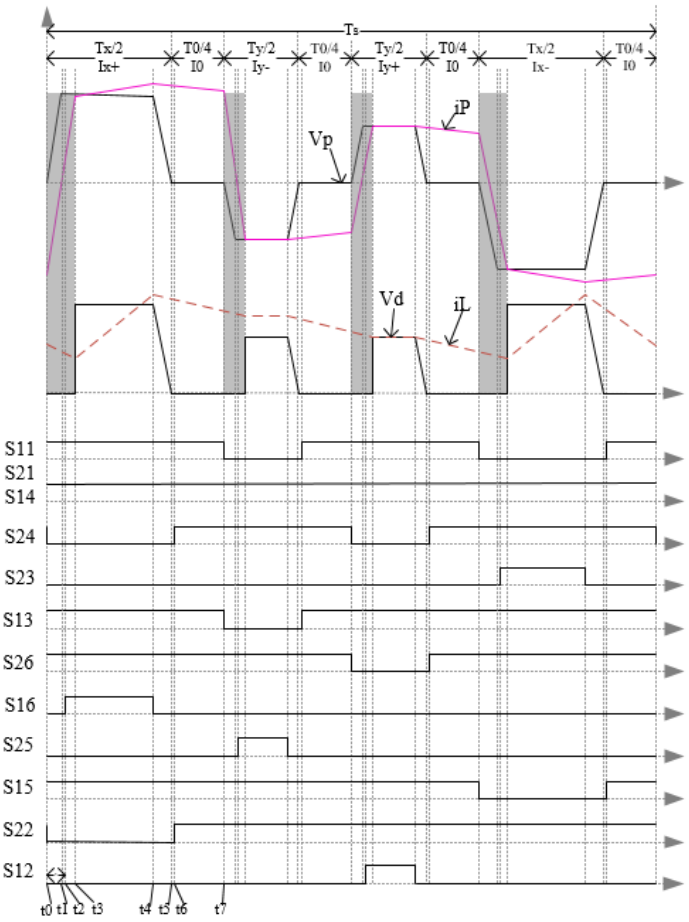


Figure 3.2 Circuit waveforms: primary voltage and current, rectified secondary voltage and output inductor current and corresponding switch gate driver in Sector I.

In sector I, due to the highest voltage potential of v_A, switches S_{21} and S_{14} are kept on all the time. The commutation state machine is shown in Figure 3.3. The switching states and space vectors for the SQ_3 PWM scheme in sector I are summarized in Table 3.1, where "1" represents on-state, and "0" represents off-state.

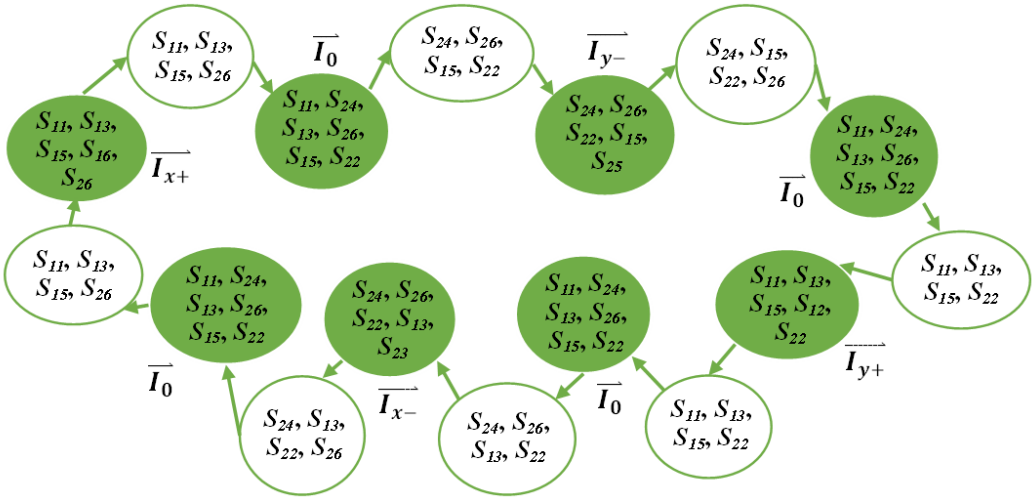


Figure 3.3 Finite commutation state machine in Sector I for SQ_3. (S_{21}, S_{14} are kept on all the time).

Table 3.1. Switching states and space vectors of SQ_3 in Sector I

Space vectors	S_{21}	S_{11}	S_{24}	S_{14}	S_{23}	S_{13}	S_{26}	S_{16}	S_{25}	S_{15}	S_{22}	S_{12}
$\overrightarrow{I_{x+}}$	1	1	0	1	0	1	1	1	0	1	0	0
$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
$\overrightarrow{I_{y-}}$	1	0	1	1	0	0	1	0	1	1	1	0
$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
$\overrightarrow{I_{y+}}$	1	1	0	1	0	1	0	0	0	1	1	1
$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0
$\overrightarrow{I_{x-}}$	1	0	1	1	1	1	1	0	0	0	1	0
$\overrightarrow{I_0}$	1	1	1	1	0	1	1	0	0	1	1	0

3.2 Steady-State Analysis

The transformer leakage inductance causes duty-cycle loss when vector transition is from zero vector to active vectors, as shown in the shade area of Figure 3.2. As a result, the secondary side voltage pulses are shorter than the primary side. The duty-cycle losses and current ripple are analyzed in this section.

The analysis in this section is based on the assumption that the transformer is ideal and the forward voltage drop across all diodes and MOSFETs is zero. It is also assumed that the output voltage V_o is constant.

3.2.1 Duty-Cycle Analysis

The ZVS operation of the converter is achieved by utilizing transformer leakage inductance, which reduces the effective duty-cycle. The duty loss increases the conduction loss and limits the conversion efficiency and power density. The duty-cycle loss happened at the vector transition from zero vectors to active vectors due to the finite transition time depending on the value of L_{lk} and the primary voltage V_P as shown in Figure 3.4 in the shaded area ΔD_x and ΔD_y. During these intervals, primary current i_P changes direction and there is no energy transfer from the AC side to the DC side.

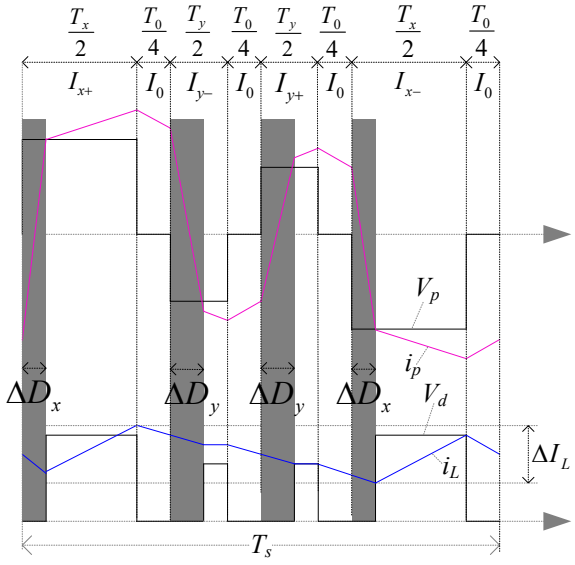


Figure 3.4 Duty losses of SQ_3 when $\overrightarrow{I_{ref}}$ located at -30° < θ < 0°.

During the duty loss interval, the transformer primary current i_P is linearly ramping from one direction to another. It is assumed that the output current ripple is ignorable compared to the load current. I_d is the total variation of i_P which is determined by the load current, and is given by:

$$I_d = 2nI_o \tag{3.1}$$

The duty-cycle loss in each transition can be calculated as [43]:

$$\Delta D = \frac{2nI_oL_{lk}}{v_P(\theta)T_S} \tag{3.2}$$

where $v_P(\theta)$ is the voltage across the leakage inductance L_{lk} during the duty loss interval, and the angle θ is the angle displacement between the current reference vector $\overrightarrow{I_{ref}}$ and the angle of α-axis of the α-β plane. $v_P(\theta)$ is depending on the angle θ as shown in Figure 3.5. The blue curve is used to calculate ΔD_x, and pink curve is used to calculate ΔD_y.

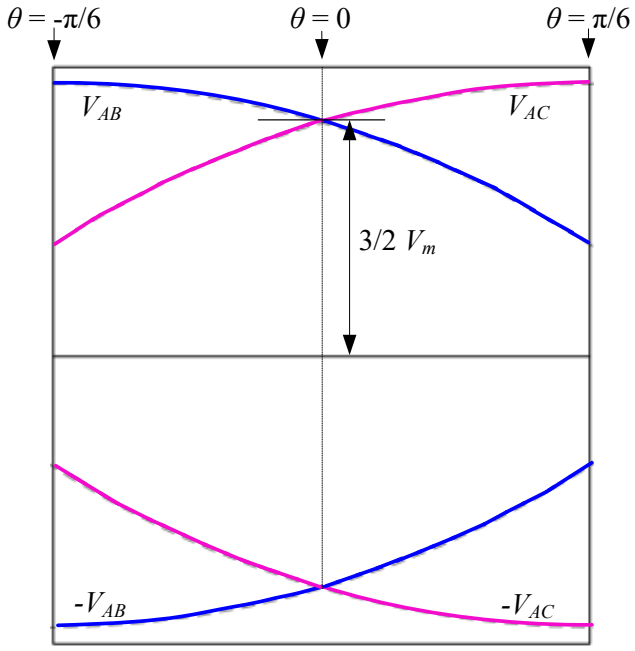


Figure 3.5 Envelope of transformer primary voltage $V_P(\theta)$.

The maximum duty loss of SQ_3 is obtained when the magnitude of $v_P(\theta)$ is minimum at $\theta = \pm 30°$. The magnitudes of $v_P(\theta)$ for two voltage pulses are $\sqrt{3}V_m$, and $\frac{\sqrt{3}V_m}{2}$ respectively.

$$\Delta D_{total\_max} = \frac{12nI_oL_{lk}}{\sqrt{3}V_mT_S} \tag{3.3}$$

The minimum duty loss happens at $\theta = 0°$, and is given by:

$$\Delta D_{total\_min} = \frac{16nI_oL_{lk}}{3V_mT_S} \tag{3.4}$$

Under the same condition, the duty losses of SQ_1 and SQ_3 are the same, because they both have two vector transitions from $\overrightarrow{I_0}$ to $\overrightarrow{I_x}$, and two vector transitions

from $\overrightarrow{I_0}$ to $\overrightarrow{I_y}$.

3.2.2 Output Inductor Current Ripple

The output inductor current ripple at steady state is determined by the off-time of the secondary voltage V_d. The off-time of V_d consists of the dwell time of zero vectors and the duty loss time. Compared with the dwell time of zero vector, the duty loss interval is very small, to the point that it is ignored. Figure 3.6 shows the output current ripple of SQ_3 PWM varying with phase angle θ due to the variable off-time of V_d.

At θ=0˚, the total off-time of the secondary voltage V_d is at the minimum and is given by $(1 - m_a)T_s$, therefore the current ripple reaches the minimum value at θ=0˚. The off-time of V_d is divided into four intervals.

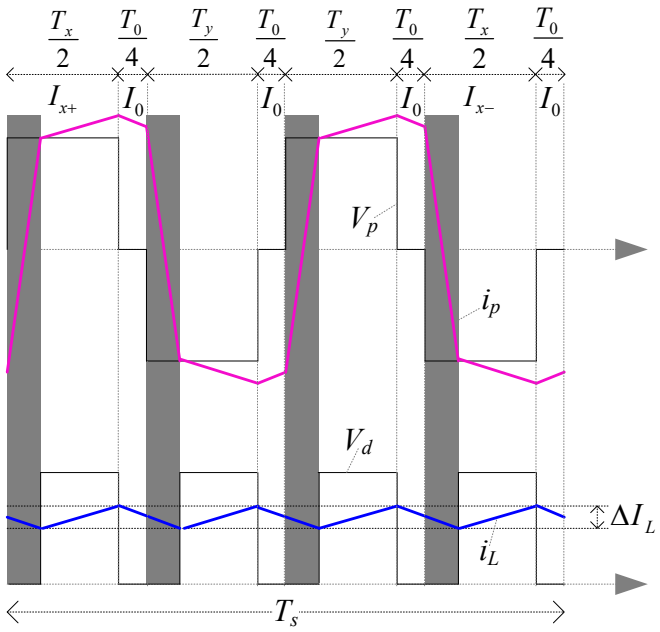
The minimum current ripple is

$$\Delta I_{min} = \frac{V_o(1-m_a)T_S}{4L_o} \tag{3.5}$$

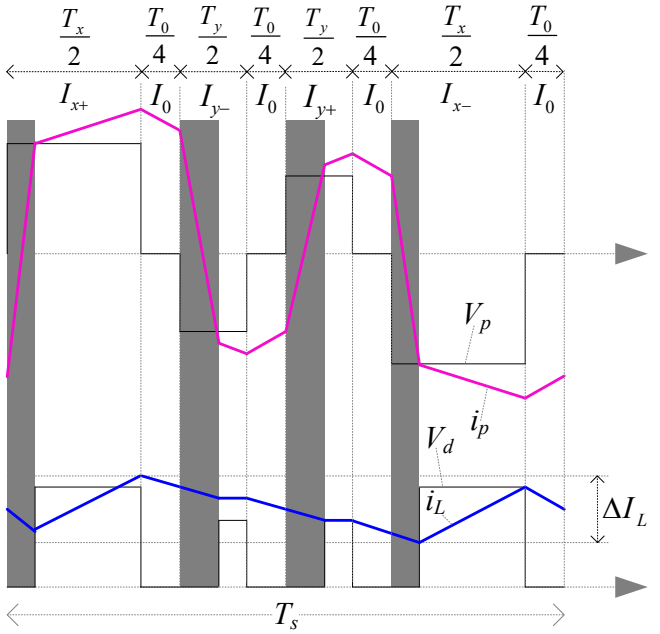
At θ=$\pm$30˚, the total off-time of secondary voltage V_d is the maximum and can be derived as $(1 - \frac{\sqrt{3}}{2}m_a)T_s$. Therefore, the output current ripple reaches maximum value. The two pulses of $I_{y+}$and I_{y-}on the secondary side disappear so that the three off-time intervals merge into one large interval as shown in Figure 3.6 (c).

The maximum current ripple of SQ_3 is

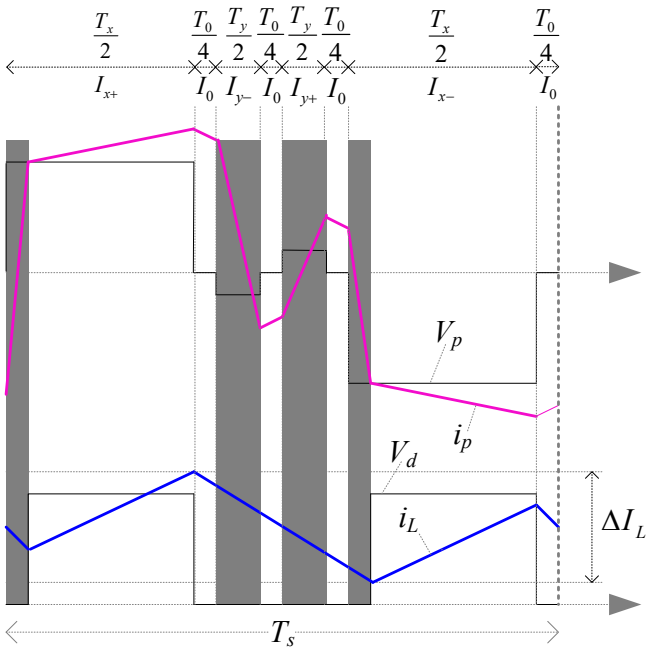
$$\Delta I_{max} = \frac{3V_o(1-\frac{\sqrt{3}}{2}m_a)T_S}{4L_o} \tag{3.6}$$



(a) θ=0˚



(b) $-30° \leq \theta < 0°$



(c) θ=−30°

Figure 3.6 Waveforms of the duty-cycle loss and the output current ripple for *SQ₃* PWM schemes.

3.3 ZVS Operation Analysis

Since for the proposed PWM scheme, with the only vector transition being between active vector and zero vector, the ZVS operation analysis only focuses on one example of vector transition from zero vector to active vector ($\overrightarrow{I_{0-}}$ to $\overrightarrow{I_{1+}}$) and one example from active vector to zero vector ($\overrightarrow{I_{1+}}$ to $\overrightarrow{I_{0+}}$) in sector I. The same analysis can be applied to the other vector transitions and the rest of other five sectors. "C_{xx}" and "D_{xx}" represent the output capacitance and parasitic diode of "S_{xx}".

(a) Vector transition from zero vector $\overrightarrow{I_{0-}}$ to active vector $\overrightarrow{I_{1+}}$ (*t₀* to *t₃* in Figure 3.2)

At *t₀-*, the transformer primary side current i_P is circulating through phase *A*. The primary side voltage v_P is clamped to zero. The current vector is $\overrightarrow{I_{0-}}$ in this mode, as shown in Figure 3.7 (a).

At t_0, S_{24} and S_{22} are turned off. Energy stored in leakage inductance L_{lk} starts transferring to output capacitances of S_{24}, S_{16}, S_{22}, and S_{12} as shown in Figure 3.7 (b). The primary current i_P also starts resonating down to zero.

At t_1, when voltage across S_{16} reaches zero, D_{16} starts conducting as shown in Figure 3.7 (d), and the voltage of switch S_{16} is clamped to zero. At t_2, before i_P cross zero, S_{16} is turned on at zero voltage. In order to achieve ZVS of S_{16}, energy stored in L_{lk} should be enough to charge the total equivalent capacitance of C_{24}, C_{16}, C_{22}, and C_{12}. The simplified circuit of resonant process is shown in Figure 3.7 (c). The transformer capacitance is also considered part of the total equivalent capacitance. The total equivalent capacitance can be calculated as

$$C_{eq} = \frac{5}{2}C_o + C_{TR} \tag{3.7}$$

where C_o is output capacitance of MOSFET. C_{TR} is the transformer capacitance. The optimum deadtime τ (t_0 to t_2) can be estimated as [35]

$$\tau = \frac{\pi}{2}\sqrt{L_{lk}C_{eq}} \tag{3.8}$$

At t_3, i_P reaches i_L and as a result line voltage v_{AB} appears across the transformer primary side and vector transition from $\overrightarrow{I_{0-}}$ to $\overrightarrow{I_{1+}}$ complete. At this moment, the voltage across S_{24}, S_{16}, S_{22}, and S_{12} are v_{AB}, 0, $\frac{1}{2}v_{AB}$, and ($v_{AC} - \frac{1}{2}v_{AB}$) respectively.

(b) Vector transition from active vector $\overrightarrow{I_{1+}}$ to zero vector $\overrightarrow{I_{0+}}$ (t_4 to t_6)

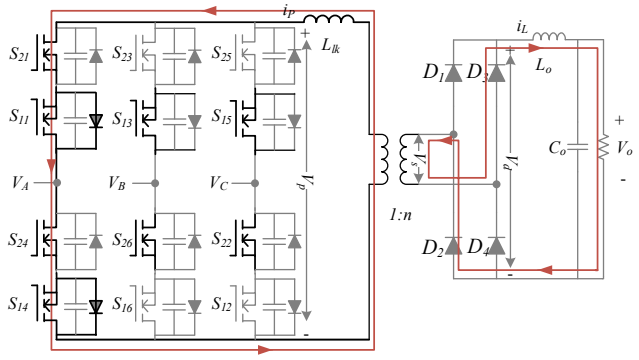
At t =[t_3, t_4], the current vector is $\overrightarrow{I_{1+}}$. At t_4, S_{16} is turned off, and the transformer primary side current i_P starts charging capacitances, as shown in Figure 3.7 (g).

At t_5, voltage across C_{24} reduces to zero and D_{24} starts conducting (Figure 3.7 (k)). At the same time, voltage across capacitance C_{22} reduces to zero, and D_{22} starts conducting. S_{24} and S_{22} are turned on at zero voltage at t_6. The primary voltage v_P is clamped to zero. Vector transition from active vector to zero vector operation is completed. At this moment, the voltage across S_{24}, S_{16}, S_{22}, and S_{12} are 0, v_{AB}, 0,

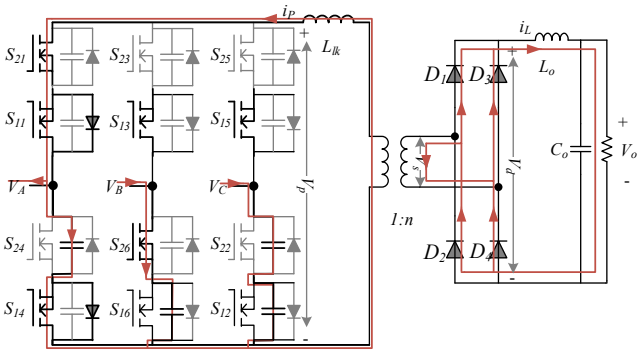
and v_{AC} respectively. The total equivalent capacitance to be charged to achieve ZVS is the same as that from zero vector to active vector, and the combined energy stored in both L_{lk} and L_o is used to charge/discharge equivalent capacitance. ZVS can be easily achieved.

During t=[t_6, t_7], the primary voltage v_P is clamped to zero. Primary current freewheeling is through S_{11}, D_{21}, S_{14} and D_{24}. The current vector is $\overrightarrow{I_{0+}}$.

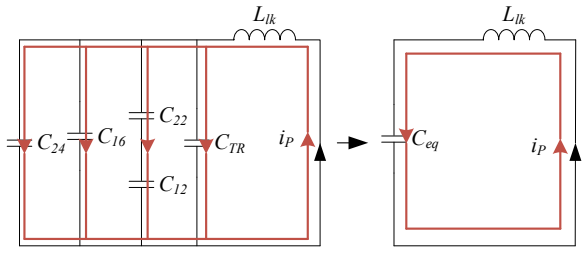
The rest of the vector transitions between active vector and zero vector operation are similar to the analyzed part and will not be discussed here.



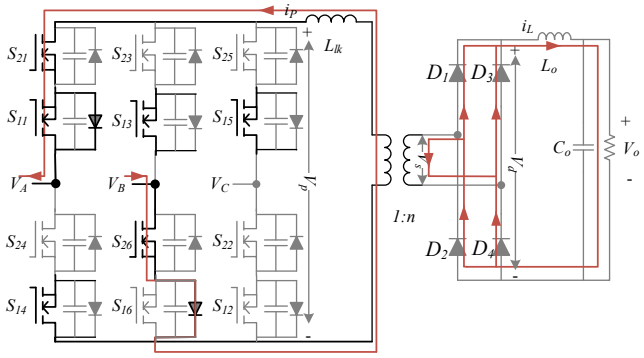
(a) Current vector $\overrightarrow{I_{0-}}$



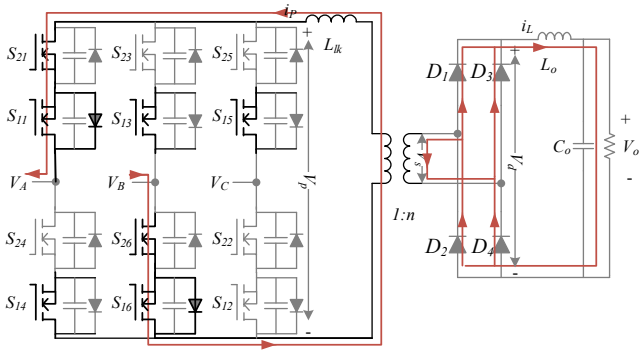
(b) Resinance between inductor and capacitors



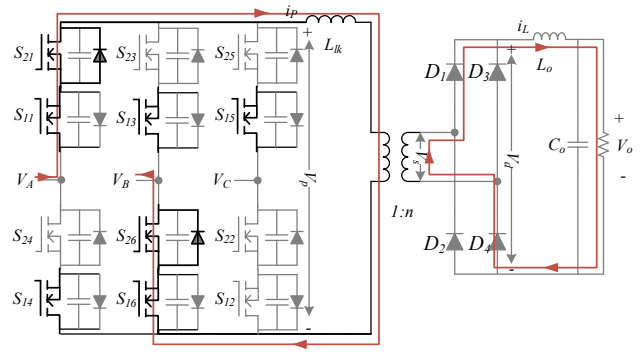
(c) Equivalent circuit



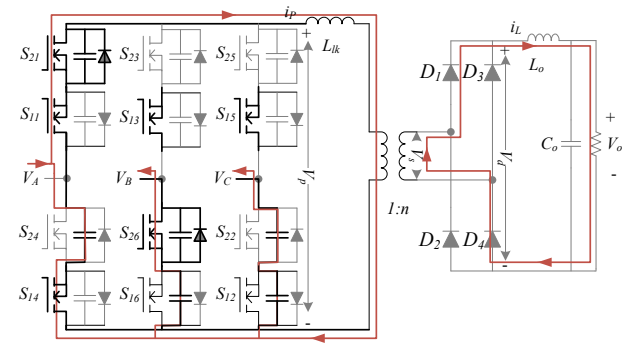
(d) D_{16} conducts



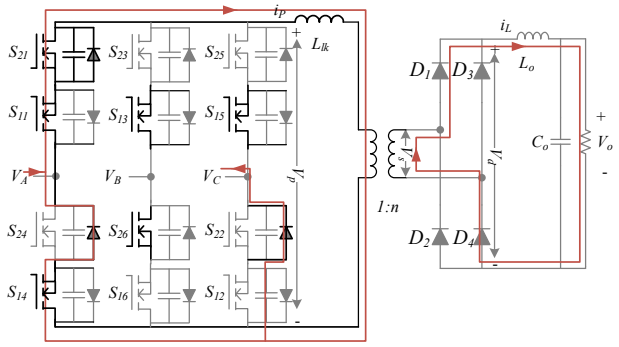
(e) S_{16} turns on under ZVS



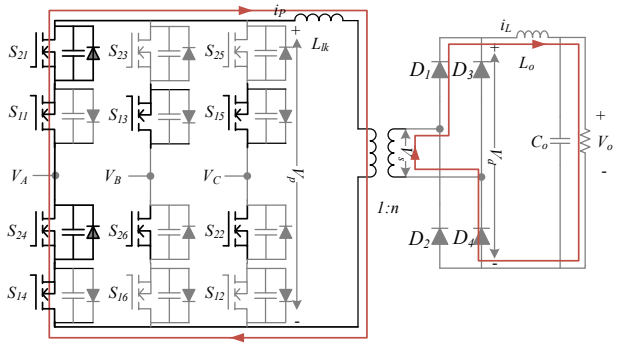
(f) Current changes direction



(g) Resoncance between inductance and capacitances



(h) D_{24} and D_{22} conduct



(i) S_{24} and S_{22} turn on under ZVS

Figure 3.7 ZVS operation of SQ_3.

3.4 Summary

In this chapter, a novel PWM ZVS scheme for the three-phase isolated matrix rectifier is proposed. The proposed PWM scheme is inspired by the 6-segment PWM scheme described in Chapter 2. By inserting a zero vector between two active vectors, the two hard-switching actions can be removed. Thus, all twelve switches can be turned on under ZVS at any time during each switching cycle. The turn-on switching loss can be totally removed. As a result, this PWM scheme can be used at a higher switching frequency than the 6-segment PWM scheme. Different from the traditional 8-segment PWM scheme, the proposed PWM is symmetrical each half switching cycle, so that the implementation is easier.

This chapter presented a detailed analysis of the proposed PWM scheme, including operation principle, steady-state analysis, and ZVS operation. The

comparison between three PWM schemes is presented in the next chapter.

Chapter 4

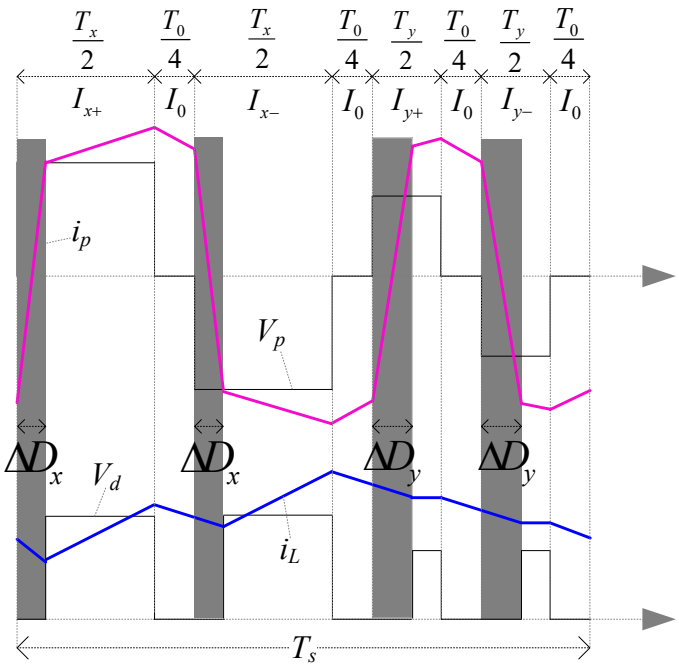
Comparison of Three PWM Schemes

This chapter presents a comparison between two existing PWM schemes in Chapter 2 and the proposed PWM scheme in Chapter 3 for the three-phase buck-type isolated matrix rectifier. The duty-cycle loss, power quality, and power loss of the three PWMs are compared.

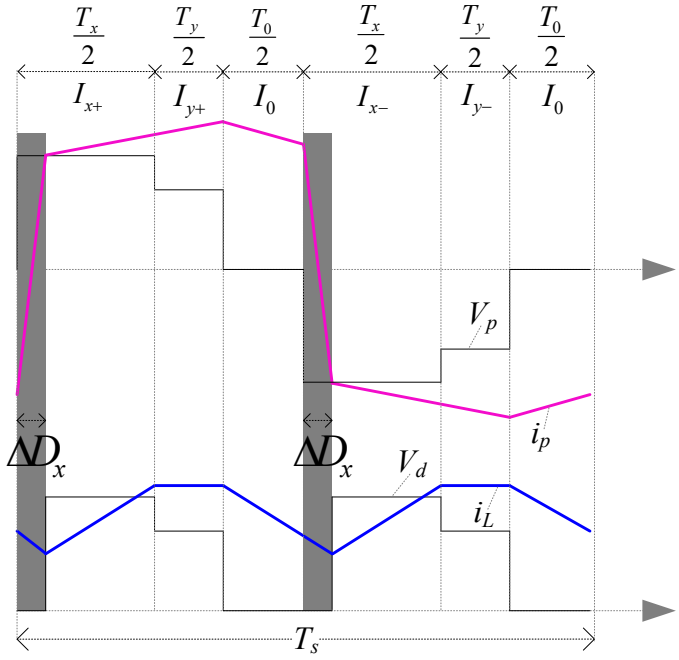
4.1 Analysis of Duty-Cycle Loss

The three-phase converter uses the resonance between transformer leakage inductance and parasitic capacitances to achieve ZVS at a price of reduction of effective duty-cycle. Duty-cycle loss happens at vector transition from zero vectors to active vectors due to the finite transition time which depends on the value of L_{lk} and the primary voltage V_P, as shown in the shaded areas of Figure 4.1. During this interval, the primary side current changes direction. The current mismatch between the transformer primary side current and secondary output inductor current causes duty-cycle loss. All four diodes on the secondary side are in on-state as shown in the previous chapters, and no power is delivered to the load side. The duty-cycle loss increases the circulating current and conduction losses and decreases the conversion efficiency and power density.

The shaded areas of Figure 4.1 show the duty-cycle losses of three different PWM schemes in one switching cycle during the interval $-30° \leq \theta < 0°$. For the two 8-segment PWMs, SQ_1 and SQ_3, there are four duty-cycle loss intervals. For the 6-segment PWM, SQ_2, there are two duty-cycle loss intervals.


$\frac{T_x}{2}$
$\frac{T_0}{4}$
$\frac{T_x}{2}$
$\frac{T_0}{4}$
$\frac{T_y}{2}$
$\frac{T_0}{4}$
$\frac{T_y}{2}$
$\frac{T_0}{4}$
I_{x+}
I_0
I_{x-}
I_0
I_{y+}
I_0
I_{y-}
I_0
i_p
V_p
ΔD_x
V_d
ΔD_x
ΔD_y
ΔD_y
i_L
T_s

(a) SQ_1


$\frac{T_x}{2}$
$\frac{T_y}{2}$
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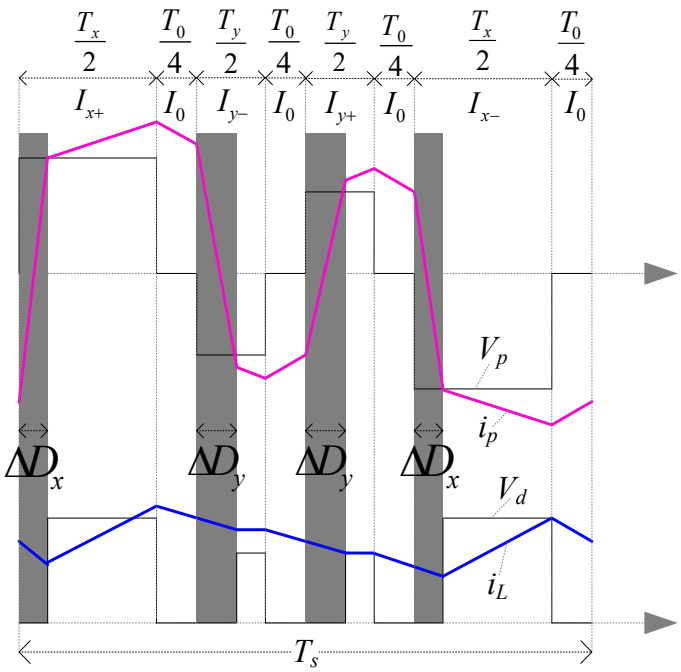
$\frac{T_x}{2}$
$\frac{T_y}{2}$
$\frac{T_0}{2}$
I_{x+}
I_{y+}
I_0
I_{x-}
I_{y-}
I_0
V_p
i_p
ΔD_x
ΔD_x
V_d
i_L
T_s

(b) SQ_2



(c) *SQ₃*

Figure 4.1 Duty-cycle losses in three PWMs during $-30° \leq \theta < 0°$.

As stated in Chapter 3, the 8-segment PWMs have four duty-cycle loss intervals. The total duty-cycle loss of *SQ₁* and *SQ₃* can be derived as:

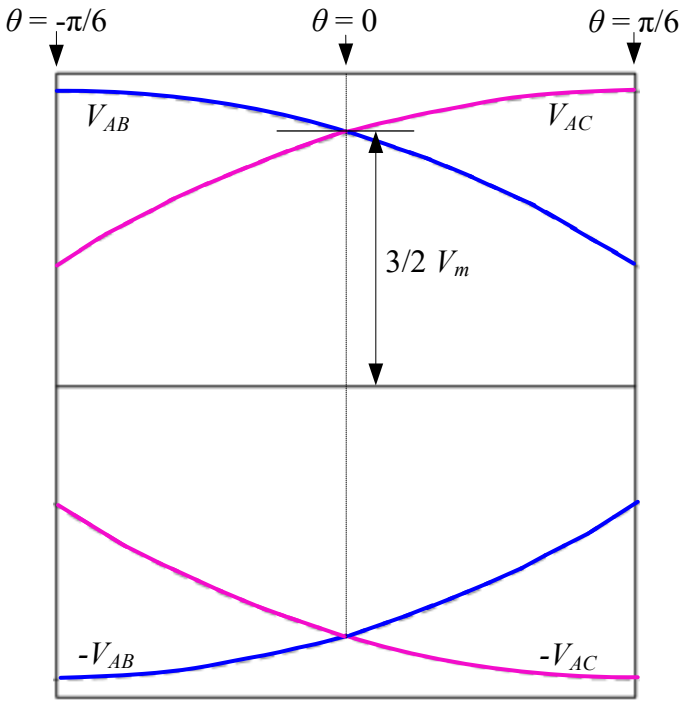
$$\Delta D_{total} = 2\Delta D_x + 2\Delta D_y = \frac{4nI_oL_{lk}}{V_P(\theta)_{\_x}T_S} + \frac{4nI_oL_{lk}}{V_P(\theta)_{\_y}T_S} \quad (4.1)$$

where $V_P(\theta)_{\_x}$ and $V_P(\theta)_{\_y}$ are the voltage across the leakage inductance during interval ΔD_x and ΔD_y, respectively. The voltage $V_P(\theta)$ is one of the three line voltages depending on the angle θ as shown in Figure 4.2 (a); the blue curve indicates $V_P(\theta)_{\_x}$ and the pink curve indicates $V_P(\theta)_{\_y}$ during sector I.

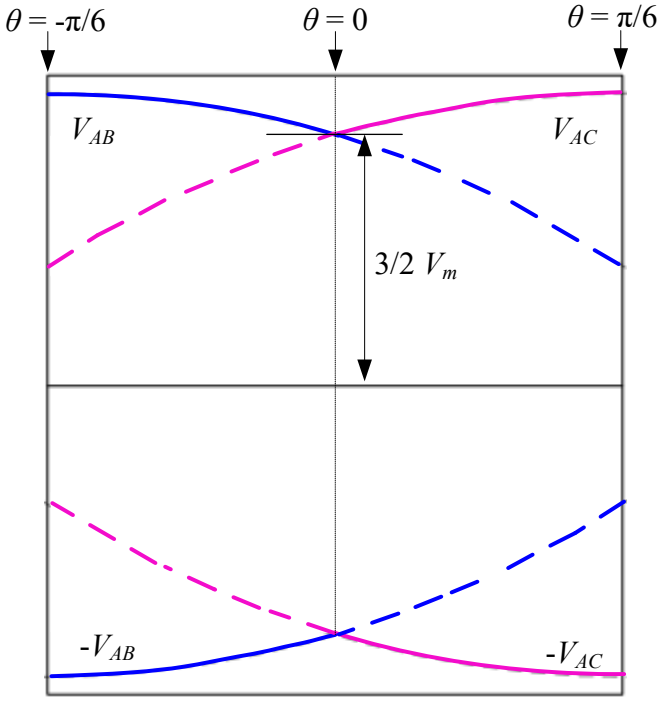
The 6-segment PWM only has two vector transitions from zero vector to active vector, so that only two intervals ΔD_x contribute to the duty loss, as shown in Figure 4.1(b). The transformer voltage $V_P(\theta)$ corresponding to angle θ is shown in Figure 4.2 (b), the solid curve.

The total duty-cycle loss of *SQ₂* can be expressed as:

$$\Delta D_{total} = 2\Delta D_x = \frac{4nI_oL_{lk}}{V_P(\theta)T_S} \quad (4.2)$$



(a) Envelope of $V_P(\theta)_{-x}$ and $V_P(\theta)_{-y}$ in 8-segment PWMs



(b) Envelope of $V_P(\theta)_{-x}$ in 6-segment PWMs

Figure 4.2 Envelope of $V_P(\theta)$.

As shown in equation 4.1 and 4.2, the maximum duty-cycle loss happens at $V_P(\theta)$ is the minimum, and minimum duty loss that happens at $V_P(\theta)$ is the maximum.

For 8-segment PWMs, SQ_1 and SQ_3, at θ=0˚, $\mathrm{V_P(\theta)_{\_x}} = \mathrm{V_P(\theta)_{\_y}} = \frac{3}{2}\mathrm{V_m}$, the duty loss reaches the minimum, which is:

$$\Delta D_{total\_min\_8seg} = \frac{16nI_oL_{lk}}{3V_mT_S} \tag{4.3}$$

At $\theta = \pm 30°$, $V_P(\theta)_{\_x}$ and $V_P(\theta)_{\_y}$ reach extremum $\sqrt{3}V_m$ and $\sqrt{3}/2V_m$. The duty loss reaches a maximum of:

$$\Delta D_{total\_max\_8seg} = \frac{12nI_oL_{lk}}{\sqrt{3}V_mT_S} \tag{4.4}$$

For the 6-segment PWM, SQ_2, the maximum duty-cycle loss happens at θ=0˚, $V_P(\theta) = \frac{3}{2}V_m$, and is given by:

$$\Delta D_{total\_max\_6seg} = \frac{8nI_oL_{lk}}{3V_mT_S} \tag{4.5}$$

At $\theta = \pm 30°$, $V_P(\theta)$ reaches the maximum $\sqrt{3}V_m$, and the minimum duty loss is:

$$\Delta D_{total\_min\_6seg} = \frac{4nI_oL_{lk}}{\sqrt{3}V_mT_S} \tag{4.6}$$

The total duty losses of the three presented PWMs are compared in Table 4.1 at a different angle θ. The total duty-cycle loss is related to transformer leakage inductance, L_{lk}, transformer turns ratio, n, and modulation index, m_a, and PWM switching frequency, f_{sw}. For SQ_2, the PWM switching frequency and transformer switching frequency are the same, f_{sw}. For SQ_1 and SQ_3 with f_{sw} PWM switching frequency, the transformer switching frequency is $2f_{sw}$. Table 4.1 shows the duty loss of the 8-segment PWMs and 6-segment PWM with PWM switching frequency f_{sw}, and 8-segment PWMs with PWM switching frequency $\frac{1}{2}f_{sw}$, that is, with same transformer switching frequency as for the 6-segment. In order to make the comparison clear, the total duty loss of SQ_2 at θ=0˚ with PWM switching frequency f_{sw} is set as a base.

Table 4.1. Comparison of normalized total duty-cycle losses

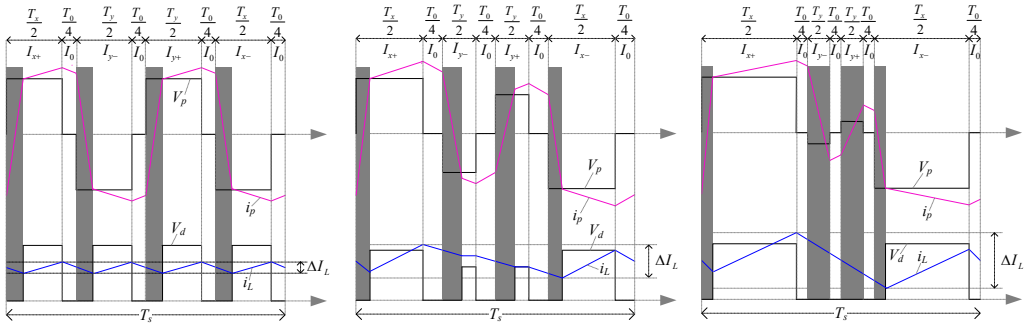
Total duty losses	SQ_1 and SQ_3 (f_{sw})	SQ_2(f_{sw})	SQ_1 and SQ_3 ($\frac{1}{2}f_{sw}$)
θ=±30°	2	1 (base)	1
-30° ≤ θ < 0°, 0° ≤ θ < 30°,	$2<\Delta D_{total}<\frac{3\sqrt{3}}{2}$	$\frac{\sqrt{3}}{2}<\Delta D_{total}<1$	$1<\Delta D_{total}<\frac{3\sqrt{3}}{4}$
θ=±30°	$\frac{3\sqrt{3}}{2}$	$\frac{\sqrt{3}}{2}$	$\frac{3\sqrt{3}}{4}$

4.2 Power Quality

The comparison in this section consists of two parts: the first part is the output inductor current ripple comparison within one sector, and the second part is the power quality comparison during sector crossing.

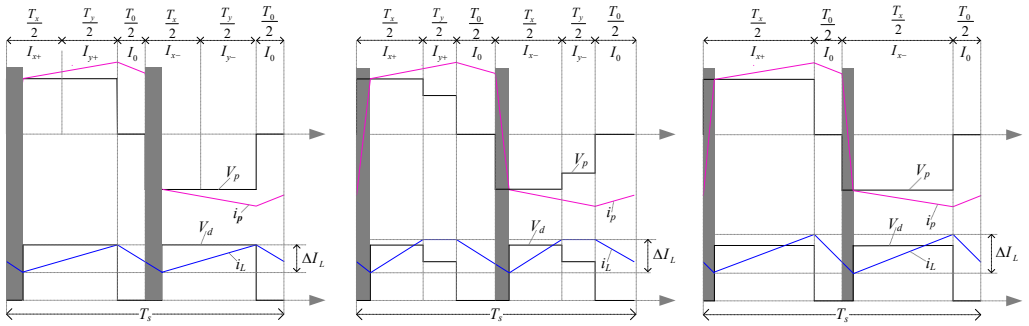
4.2.1 Output Inductor Current Ripple within Each Sector

The output inductor current ripple at steady state varies with the phase angle θ. It can be calculated by using the equation $V = L\frac{di}{dt}$, where V and L are constants, so that the current ripple is determined by the off-time of secondary voltage V_d. The off-time of secondary voltage consists of the dwell time of zero vectors and the duty loss time intervals. The 6-segment PWM, SQ_2, has two zero vectors, so the off-time of V_d is divided into two intervals as shown in Figure 4.3 (b). The 8-segment PWMs, SQ_1 and SQ_3, contains four zero vectors, so the off-time of V_d is divided into four intervals as shown in Figure 4.3 (a) and (c).

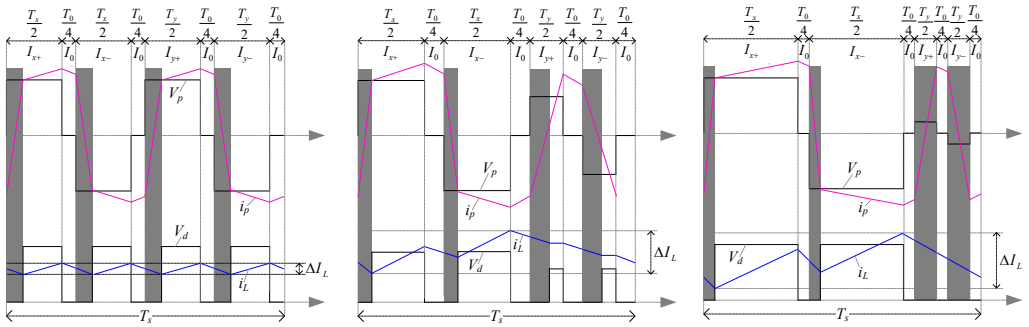


θ=0° -30° ≤ θ < 0° θ=-30°

(a) SQ_1



(b) SQ_2



(c) SQ_3

Figure 4.3 Waveforms of output inductor current ripple for three PWMs.

For all three PWMs, at θ=0°, the off-time of V_d is the minimum and is given by (1-m_a)T_S. Therefore, the current ripple for all three PWMs reach the minimum at θ=0°. The minimum current ripple for 6-segment PWM, SQ_2, and 8-segment PWM, SQ_1 and SQ_3, can be expressed as ΔI_{min_6seg} and ΔI_{min_8seg} respectively, and are given by [48]:

$$\Delta I_{min\_6seg} = \frac{V_o(1-m_a)T_S}{2L_o} \tag{4.7}$$

$$\Delta I_{min\_8seg} = \frac{V_o(1-m_a)T_S}{4L_o} \tag{4.8}$$

The minimum current ripple of SQ_1 and SQ_3 are only half of that of SQ_2.

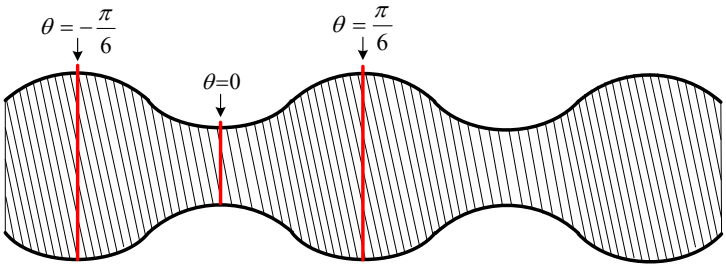
At θ=±30°, the off-time of V_d is the maximum and is given by (1-$\frac{\sqrt{3}}{2}m_a$)T_S. Therefore, the current ripple for all three PWMs reach the maximum at θ=±30°. For SQ_2, the off-time is still divided by two intervals. However, for SQ_1 and SQ_3,

two of the voltage pulses disappear at θ=$\pm$30°, so that three zero vector intervals merge into one large interval as shown in Figure 4.3. Assuming that the duty-cycle losses are relatively small and can be ignored, the maximum current ripple of the 6-segment PWM, SQ_2, and 8-segment PWM, SQ_1 and SQ_3, can be expressed as ΔI_{max_6seg} and ΔI_{max_8seg} respectively, and are given by [48]:

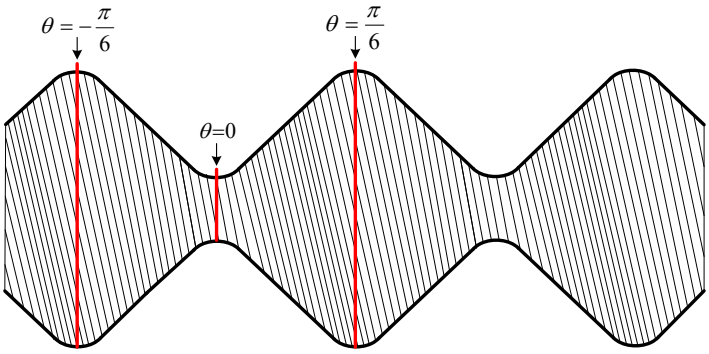
$$\Delta I_{min\_6seg} = \frac{V_o(1-\frac{\sqrt{3}}{2}m_a)T_S}{2L_o} \tag{4.9}$$

$$\Delta I_{min\_8seg} = \frac{3V_o(1-\frac{\sqrt{3}}{2}m_a)T_S}{4L_o} \tag{4.10}$$

The envelope of the output inductor current ripple of the 6-segment PWM and 8-segment PWMs is shown in Figure 4.4. The minimum envelope of the current ripple at $\theta = 0°$ in SQ_1 and SQ_3 is lower than SQ_2, while the maximum current ripple at $\theta = \pm 30°$ in SQ_1 and SQ_3 is higher than in SQ_2. The missing two voltage pulses cause larger ripples at $\theta = \pm 30°$ in SQ_1 and SQ_3.



(a) SQ_2



(b) SQ_1 and SQ_3

Figure 4.4 Envelope of output inductor current ripple.

4.2.2 Power Quality during Sector Crossing

This section analyzed the power quality of the input phase current during sector crossing. Take sector transition from sector I to sector II as an example, as shown in the shaded area of Figure 4.5, when phase angle θ is across 30˚, with an excessively increased switching period, PWM details can be observed.

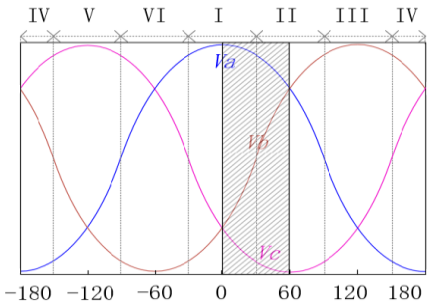


Figure 4.5 Input phase voltage.

Figure 4.6 shows the secondary side voltage V_d and current I_L during four switching periods near θ=30˚ of the three PWMs. The first two switching cycles are in sector I, and the last two switching cycles belong to sector II. The secondary side current reflects the primary side current because of the relationship $I_p = nI_L$, and thereby reflects the power quality of the input phase currents.

As can be seen in Figure 4.6, in SQ_1, before sector crossing, the two voltage pulses corresponding to the current vector $\overrightarrow{I_1}$ disappear, and the other two voltage pulses corresponding to the current vector $\overrightarrow{I_2}$ reach the maximum. In the first cycle of sector II, the first two voltage pulses corresponding to $\overrightarrow{I_2}$ are in their maximum, while the second two pulses corresponding to vector $\overrightarrow{I_3}$ disappear. The combination of the four pulses causes a large current ripple in the input phase current. For SQ_2, the vector sequence is swapped in the center of each sector. For example, in sector I, the vector sequence in the first half of the sector is $\overrightarrow{I_{1+}}, \overrightarrow{I_{2+}}, \overrightarrow{I_0}, \overrightarrow{I_{1-}}, \overrightarrow{I_{2-}}, \overrightarrow{I_0}$, while in the second half of the sector the sequence is swapped to $\overrightarrow{I_{2+}}, \overrightarrow{I_{1+}}, \overrightarrow{I_0}, \overrightarrow{I_{2-}}, \overrightarrow{I_{1-}}, \overrightarrow{I_0}$ to maintain the voltage waveform in an HTL pattern. In this way, the amplitude of voltage V_d reaches the maximum during sector crossing. As a result, the secondary current ripple does not experience a sudden jump, and will not cause oscillation in

the input current. In SQ_3, the sequence patterns before and after sector crossing do not change, so that the input current oscillation is smaller compared to the current oscillation in SQ_1.

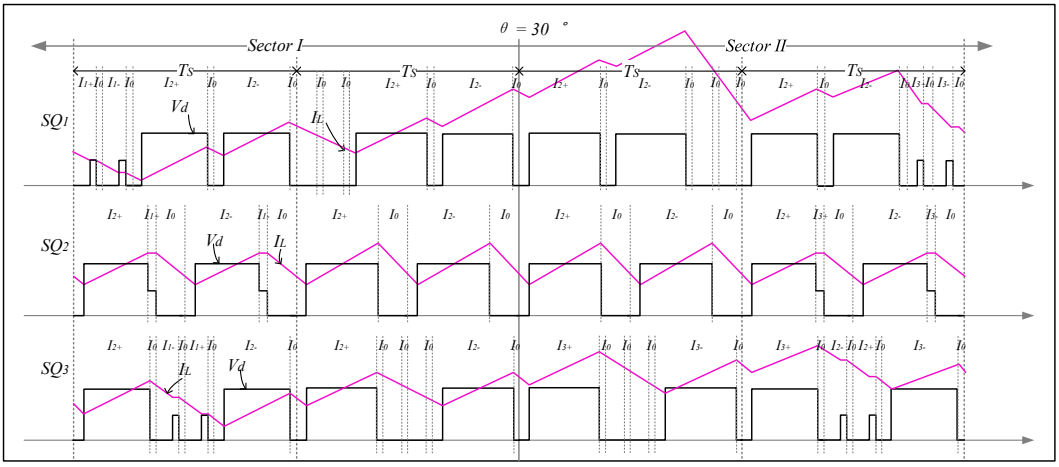


Figure 4.6 Secondary side voltage and current of three PWMs during sector crossing.

Figure 4.7 shows two sets of waveforms of SQ_2 in four switching cycles: the first set is during sector crossing when θ=30˚, and the second set is in the center of sector I when θ=0˚. Because the vector sequence swapped in the middle of sector, as discussed earlier, the voltage waveform is in an HTL pattern and reaches the maximum during sector crossing. As a result, the secondary current ripple does not experience a sudden jump, and will not cause oscillation in the input current. When the reference vector crosses sub-sectors, at θ=0˚, the vector sequence is swapped to maintain a voltage HTL pattern, which causes a small sudden jump in current between the two phases.

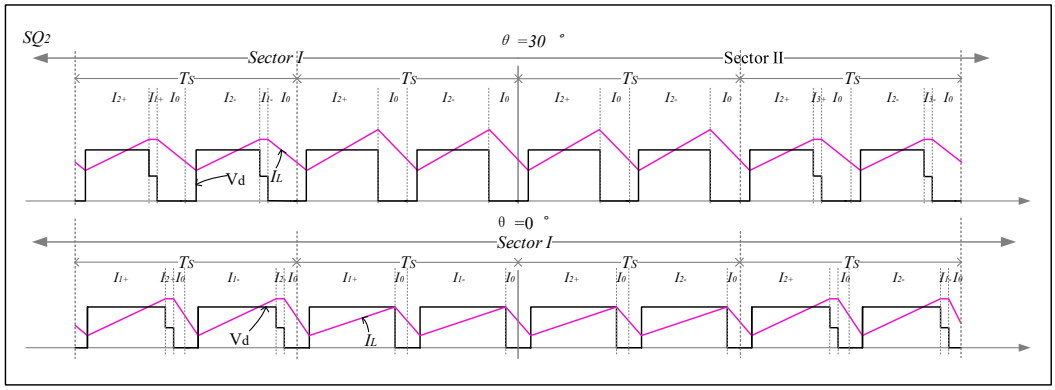
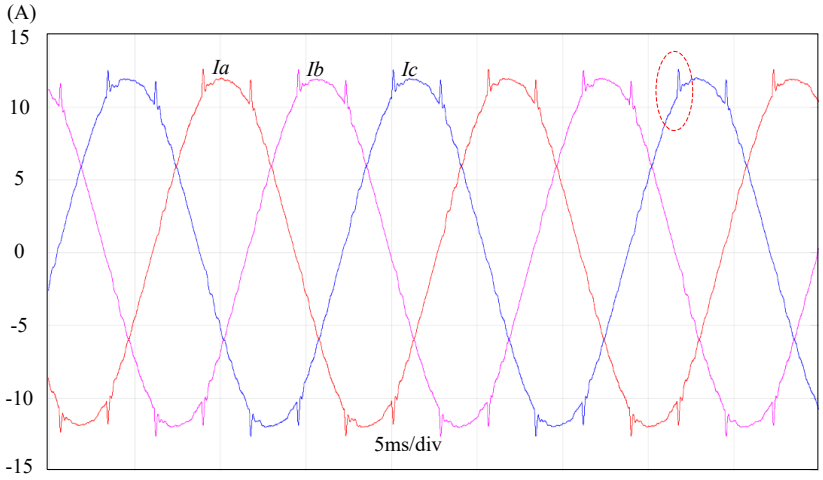
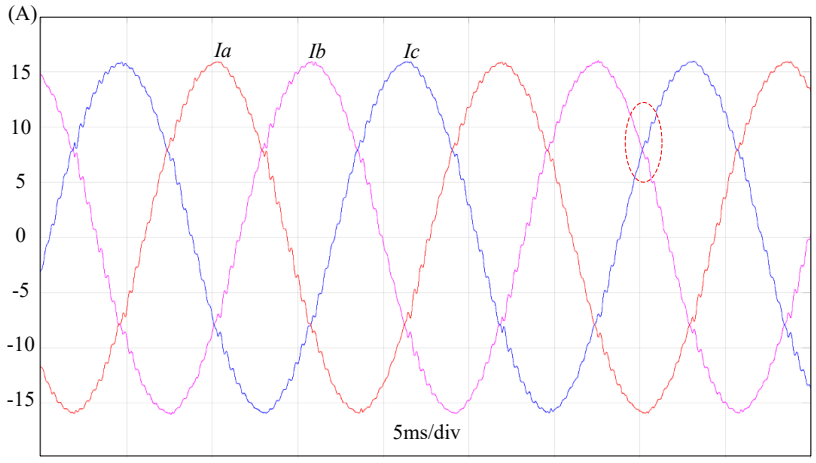


Figure 4.7 Secondary side voltage and current of SQ_2 when θ=30˚ and θ=0˚.

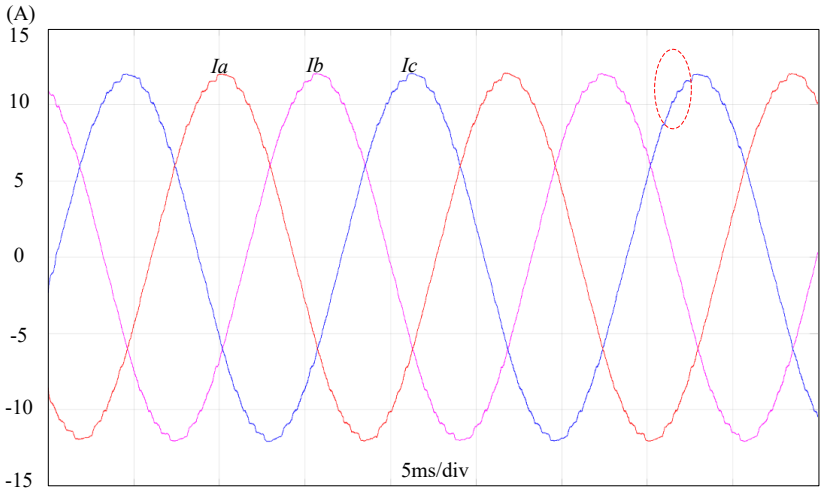
Figure 4.8 shows the simulation results of the input phase current of the three PWMs; the current oscillations at different locations can be observed as shown in red circles. For SQ_1 and SQ_3, the current spikes happen at sector crossing, while for SQ_2 the current sudden jump is near the center of each sector. Compared with SQ_1, the vector sequence of SQ_3 partly lowers the input current oscillation, thereby the power quality of SQ_3 is improved.



(a) SQ_1



(b) SQ_2



(c) SQ_3

Figure 4.8 Simulation results of the input phase current of three PWMs.

4.3 Power Loss Comparison

The power loss comparison of the three PWMs are analyzed in this section. The analysis is based on the switching operation during the interval $-30° \leq \theta < 0°$, corresponding to sector I (a), and this remains true for all the sectors due to the symmetry of the switching patterns. All the data used to calculate the power loss are from the data-sheet and the simulation.

The power loss in the converter mainly can be divided into two groups: conduction loss, P_C, and switching loss, P_S. The conduction loss of each power device is the power loss when the device is in on-state, which includes conduction loss of MOSFETs, P_{CM}, and conduction loss of diodes, P_{CD}. The switching loss includes MOSFETs turn-on loss and turn-off loss, diode turn-on and turn-off loss.

The ZVS operation of the converter with SQ_1 PWM partly removed the turn-on loss, so only two MOSFETs are counted to calculate the turn-on loss. For SQ_3 PWM, all twelve MOSFETs are turned on at zero voltage, so there is no turn-on loss with this PWM scheme. For SQ_2 PWM, there are also two hard-switch actions in each switching cycle.

4.3.1 Conduction Loss

The conduction loss of the converter consists of MOSFET conduction loss and diode conduction loss. The MOSFET conduction loss, P_{CM} , can be calculated by using the equation below:

$$P_{CM} = R_{ds} * {i_{ds}}^2 * \frac{t\_duty}{T_s} \tag{4.11}$$

where R_{ds} is the drain-source on-state resistance, and i_{ds} is the MOSFET on-state current, which is sampled from the simulation. t_duty is the conduction time of the MOSFET, and T_s is the switching period.

The conduction loss of the diode can be calculated as [94]:

$$P_{CD} = (U_{d0} * i_{ds} + R_d * {i_{ds}}^2) * \frac{t\_duty}{T_s} \tag{4.12}$$

where U_{d0} is the diode on-state zero-current voltage. R_d is the diode on-state resistance.

Table 4.2, 4.3, and 4.4 list the conduction devices of each space vector and corresponding dwell time in sector I (a) of SQ_1, SQ_2,and SQ_3 respectively.

Table 4.2. Conduction devices of SQ_1

Space vector	Gate signals on conduction devices				Conduction diode		Conduction MOSFET		Dwell time
I_{1+}	g_{21}	g_{11}	g_{26}	g_{16}	D_{21}	D_{26}	S_{11}	S_{16}	1/2*d_1
I_{0+}	g_{23}	g_{13}	g_{26}	g_{16}	D_{23}	D_{26}	S_{13}	S_{16}	1/4*d_0
I_{1-}	g_{24}	g_{14}	g_{23}	g_{13}	D_{13}	D_{14}	S_{23}	S_{24}	1/2*d_1
I_{0-}	g_{21}	g_{11}	g_{24}	g_{14}	D_{11}	D_{14}	S_{21}	S_{24}	1/4*d_0
I_{2+}	g_{21}	g_{11}	g_{22}	g_{12}	D_{21}	D_{22}	S_{11}	S_{12}	1/2*d_2
I_{0+}	g_{25}	g_{15}	g_{22}	g_{12}	D_{25}	D_{22}	S_{15}	S_{12}	1/4*d_0
I_{2-}	g_{24}	g_{14}	g_{25}	g_{15}	D_{14}	D_{15}	S_{24}	S_{25}	1/2*d_2
I_{0-}	g_{21}	g_{11}	g_{24}	g_{14}	D_{11}	D_{14}	S_{21}	S_{24}	1/4*d_0

Table 4.3. Conduction devices of SQ_2

Space vector	Gate signals on conduction devices				Conduction diode		Conduction MOSFET		Dwell time
I_{1+}	g_{21}	g_{11}	g_{26}	g_{16}	D_{21}	D_{26}	S_{11}	S_{16}	$1/2*d_1$
I_{2+}	g_{21}	g_{11}	g_{22}	g_{12}	D_{21}	D_{22}	S_{11}	S_{12}	$1/2*d_2$
I_{0+}	g_{21}	g_{11}	g_{24}	g_{14}	D_{21}	D_{24}	S_{11}	S_{14}	$1/2*d_0$
I_{1-}	g_{24}	g_{14}	g_{23}	g_{13}	D_{13}	D_{14}	S_{23}	S_{24}	$1/2*d_1$
I_{2-}	g_{24}	g_{14}	g_{25}	g_{15}	D_{14}	D_{15}	S_{24}	S_{25}	$1/2*d_2$
I_{0-}	g_{21}	g_{11}	g_{24}	g_{14}	D_{11}	D_{14}	S_{21}	S_{24}	$1/2*d_0$

Table 4.4. Conduction devices of SQ_3

Space vector	Gate signals on conduction devices				Conduction diode		Conduction MOSFET		Dwell time
I_{1+}	g_{21}	g_{11}	g_{26}	g_{16}	D_{21}	D_{26}	S_{11}	S_{16}	$1/2*d_1$
I_{0+}	g_{21}	g_{11}	g_{24}	g_{14}	D_{21}	D_{24}	S_{11}	S_{14}	$1/4*d_0$
I_{1-}	g_{24}	g_{14}	g_{23}	g_{13}	D_{13}	D_{14}	S_{23}	S_{24}	$1/2*d_1$
I_{0-}	g_{21}	g_{11}	g_{24}	g_{14}	D_{11}	D_{14}	S_{21}	S_{24}	$1/4*d_0$
I_{2+}	g_{21}	g_{11}	g_{22}	g_{12}	D_{21}	D_{22}	S_{11}	S_{12}	$1/2*d_2$
I_{0+}	g_{21}	g_{11}	g_{24}	g_{14}	D_{21}	D_{24}	S_{11}	S_{14}	$1/4*d_0$
I_{2-}	g_{24}	g_{14}	g_{25}	g_{15}	D_{14}	D_{15}	S_{24}	S_{25}	$1/2*d_2$
I_{0-}	g_{21}	g_{11}	g_{24}	g_{14}	D_{11}	D_{14}	S_{21}	S_{24}	$1/4*d_0$

4.3.2 Switching Loss

The switching loss consists of MOSFET turn-on and turn-off loss, diode turn-on and turn-off loss.

A. MOSFET turn-on loss

The MOSFET turn-on loss includes two parts: the turn-on loss without taking the reverse recovery process into account, and the turn-on loss caused by diode reverse recovery. Figure 4.9 shows the MOSEFT hard-switched process.

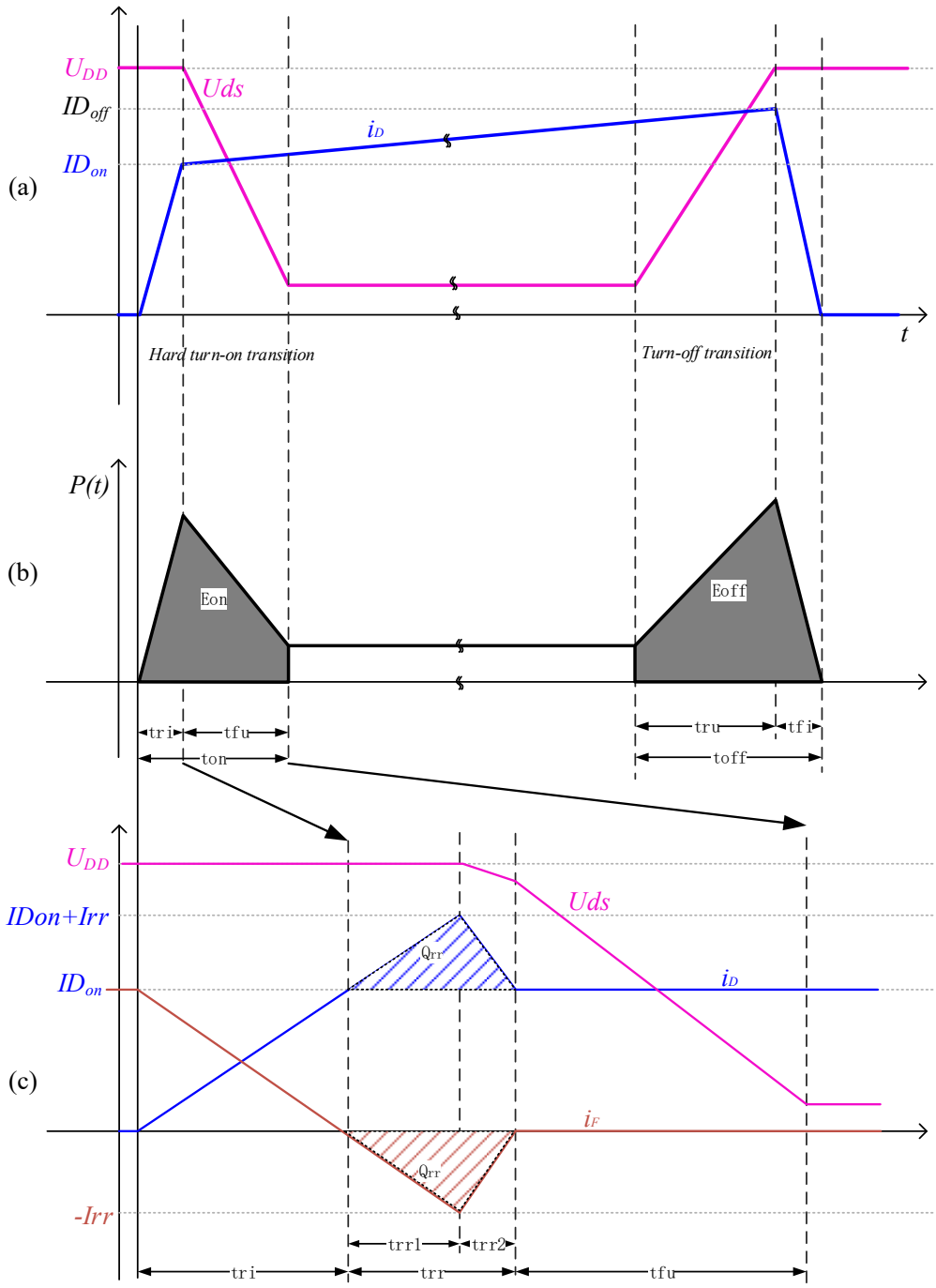


Figure 4.9 Switching transients of MOSFET [94].

In Figure 4.9 (a) and (b), the free-wheeling diode is assumed to be ideal. Figure 4.9 (a) shows the drain-source voltage and current without taking reverse recovery of the free-wheeling diode into account. Figure 4.9 (b) gives the power losses corresponding to the switching process in Figure 4.9 (a). The overlap of voltage

and current causes switching loss. Figure 4.9 (c) shows the diode reverse recovery effects on the switching losses, and the diode turn-off loss.

The MOSFET turn-on loss can be calculated as [94]:

$$P_{onM} = \frac{1}{2} V_{ds\_on} I_{ds\_on} t_{on} f_{sw} + Q_{rr} V_{ds} f_{sw} \tag{4.13}$$

Where t_{on} is the switch turn-on time interval, including current rise time *tri*, and voltage fall time *tfu*. Q_{rr} is the reverse recovery charge. V_{ds_on} is the MOSFET drain-source voltage before turning the switch on, and I_{ds_on} is the drain-source current after turning the switch off.

For zero-voltage turn-on actions, the drain-source voltage decreased to zero before the device conducting, so that the turn-on loss was zero. Consequently, SQ_3 does not have MOSFET turn-on loss.

Moreover, with regard to MOSFET turn-on loss, the output capacitor loss during the switch turn-on process should also be considered in the power loss calculation. The output capacitance loss is incurred by charging and discharging the MOSFETs' output capacitances C_{oss}. For hard-switched cases, all energy stored in C_{oss} is lost and discharged into the MOSFET channel during the switching cycle. However, for ZVS cases, the energy stored in C_{oss} is transferred to other capacitors prior to turning on the MOSFET [95]. For example, in Figure 3.7 (a)-(f), before the S_{16} turning on under ZVS, the energy stored in the parasitic capacitor C_{16} is transferred to C_{24} and C_{12}.

The output capacitance loss can be expressed as:

$$P_{Coss} = \frac{1}{2} C_{oss} {V_{ds}}^2 f_{sw} \tag{4.14}$$

Where C_{oss} is the output capacitance of MOSFET with the gate and source terminals shorted.

B. Diode turn-on loss

During each switching cycle for all three PWM schemes, diode turn-on actions happen in two situations:

1) During ZVS operation: the diode conducts when voltage across MOSFET output capacitance is zero, then when MOSFET turn-on is at ZVS.

2) Transformer primary current i_P changes direction.

For both situations, the diodes are turned on at zero voltage, so the diode turn-on loss is negligible.

$$P_{on\_D} = 0 \tag{4.15}$$

C. MOSFET turn-off loss

As shown in Figure 4.9, turn-off loss in MOSFET can be calculated in a similar manner. Therefore:

$$P_{offM} = \frac{1}{2} V_{ds\_off} I_{ds\_off} t_{off} f_{sw} \tag{4.16}$$

Where t_{off} is the switch turn-off interval, including voltage rise time *tru*, and current fall time *tfi*. V_{ds_off} is the MOSFET drain-source voltage after turning off of the switch, and I_{ds_off} is the drain-source current before turning off of the switch.

D. Diode turn-off loss

Diode turn-off action happens when MOSFET turns on, as shown in Figure 4.9. The waveform of diode current i_F during the diode turn-off process is shown in Figure 4.9 (c). The turn-off loss in the diode mostly consists of reverse recovery loss, and is given by:

$$P_{offD} = \frac{1}{4} Q_{rr} V_{ds} f_{sw} \tag{4.17}$$

The total power loss in the matrix converter can be expressed as:

$$P_{total} = P_{onM} + P_{offM} + P_{Coss} + P_{offD} \quad (4.18)$$

Take sector I as an example, in one switching cycle, the device switching actions in each vector transition of three PWMs are listed in Table 4.5, 4.6, and 4.7 respectively.

Table 4.5. Switching actions in SQ_1

Vector transit	Turn-on MOSFET		Turn-off MOSFET	
I_{1+} to I_{0-}	S_{23}		S_{11}	S_{15}
I_{0-} to I_{1-}	S_{24}	S_{22}	S_{16}	
I_{1-} to I_{0-}	S_{11}	S_{15}	S_{23}	
I_{0-} to I_{2+}	S_{12}		S_{24}	
I_{2+} to I_{0+}	S_{25}		S_{11}	
I_{0+} to I_{2-}	S_{24}		S_{12}	
I_{2-} to I_{0-}	S_{11}		S_{25}	
I_{0-} to I_{1+}	S_{16}		S_{24}	S_{22}

Table 4.6. Switching actions in SQ_2

Vector transit	Turn-on MOSFET		Turn-off MOSFET	
I_{1+} *to* I_{2+}	S_{12}	S_{22}	S_{16}	
I_{2+} *to* I_{0+}	S_{24}		S_{12}	
I_{0+} *to* I_{1-}	S_{23}		S_{11}	S_{15}
I_{1-} *to* I_{2-}	S_{25}	S_{15}	S_{23}	
I_{2-} *to* I_{0-}	S_{11}		S_{25}	
I_{0-} *to* I_{1+}	S_{16}		S_{24}	S_{22}

Table 4.7. Switching actions in SQ_3

Vector transit	Turn-on MOSFET		Turn-off MOSFET	
I_{1+} to I_{0-}	S_{22}	S_{24}	S_{16}	
I_{0+} to I_{2-}	S_{25}		S_{11}	S_{13}
I_{2-} to I_{0-}	S_{11}	S_{13}	S_{25}	
I_{0-} to I_{2+}	S_{12}		S_{24}	S_{26}
I_{2+} to I_{0+}	S_{24}	S_{26}	S_{12}	
I_{0-} to I_{1-}	S_{23}		S_{11}	S_{15}
I_{1-} to I_{0-}	S_{11}	S_{15}	S_{23}	
I_{0-} to I_{1+}	S_{16}		S_{22}	S_{24}

In Table 4.5 and Table 4.7, SQ_1 has ten turn-on and ten turn-off actions, including

two hard-switching actions. SQ_3 has twelve turn-on actions and twelve turn-off actions. All twelve turn-on actions in SQ_3 are under ZVS, so that the turn-on loss is zero. SQ_3 has two more turn-off actions than SQ_1. However, in SQ_3, S_{13}, S_{15}, S_{26}, and S_{22}, they are turned off at zero current. So a total of eight turn-off actions contribute to the turn-off loss. For SQ_1, among the ten turn-off actions, eight turn-off actions also contribute to the turn-off loss. In Table 4.6, SQ_2 has eight turn-on actions and eight turn-off actions, including two hard-switched actions.

Table 4.8 shows the power loss of all switching devices and the total conduction and switching loss in three PWMs. The simulation model is set up at the rated power of 3.4kW. The PWM switching frequency for all PWMs is 50kHz. The MOSFET type is IPW60R041P6. Device types may affect power losses, as can be observed from the calculations.

Table 4.8. Power loss comparison of three PWMs

Converter power loss (W)		SQ_1	SQ_2	SQ_3
$P_{Conduction}$	P_{CM}	8.06	9.07	8.25
	P_{CD}	5.06	5.29	5.04
	P_{C_total}	13.12	14.36	13.29
$P_{Switching}$	P_{on_M}	0.02	104.66	0
	P_{off_M}	6.43	3.79	6.49
	P_{off_D}	0	25.92	0
	P_{Coss}	0.28	0.19	0
	P_{S_total}	6.73	134.56	6.49
Total power loss		19.85	148.92	19.78

As shown in Table 4.8, the total converter power loss of the 6-segment PWM, SQ_2, is around 4.38%. However, for the two 8-segment PWMs, the total converter power loss is around 0.58%.

For SQ_1, there are also two hard-switching actions; however, when the switch turns on, no current goes through the device, so the diode reverse recovery causes power loss corresponding to the shaded areas in Figure 4.9 (c) that is zero. For

example, in Figure 2.8 (i), MOSFET S_{26} in phase B turns on at the hard-switching condition. Then, in the next mode (Figure 2.8 (j)), the current flows through phase A and phase C. There is no current flowings through S_{26}, so that the reverse recovery charge Q_{rr} is zero, as shown in Figure 4.9. As a result, the turn-on loss caused by the diode reverse recovery is zero in *SQ1*.

For the 6-segment PWM, *SQ2*, the diode reverse recovery caused energy loss in one switching cycle that is very high. In the simulation, there is no deadtime between the turn-off actions and hard-switching turn-on actions. The conversion efficiency can be improved by pre-turning on the hard-switching devices. Because the hard-switching turned-on device has no impact on the primary current, it can be turned on before the energy transfer starts. For example, in previous analysis, MOSFET S_{16} turns on under non-ZVS before S_{12} turns off; in this way, there is no current going through the device when it turns on under the hard-switching condition, so that the energy loss caused by the diode reverse recovery can be removed. Using this method, the power loss of the three PWMs is shown in Table 4.9.

Table 4.9. Power loss of three PWMs

Converter power loss (W)		*SQ1*	*SQ2*	*SQ3*
$P_{Conduction}$	P_{CM}	8.06	9.07	8.25
	P_{CD}	5.06	5.29	5.04
	P_{C_total}	13.12	14.36	13.29
$P_{Switching}$	P_{on_M}	0.02	0.98	0
	P_{off_M}	6.43	3.79	6.49
	P_{off_D}	0	0	0
	P_{Coss}	0.28	0.19	0
	P_{S_total}	6.73	4.96	6.49
Total power loss		19.85	19.32	19.78

By adding a deadtime, the converter power loss of *SQ2* is decreased from 4.38% to 0.57%. Under the same switching frequency, the switching loss is similar to that of the 8-segment switching loss. However, the transformer frequency of *SQ2* is half

of the transformer frequency of SQ_1 and SQ_3. If the same transformer frequency is considered, the switching loss will double.

4.4 Summary

In this chapter, the three PWMs for the three-phase isolated matrix rectifier are compared in terms of duty-cycle loss, output inductor current ripple, power quality, and power loss.

In each switching cycle, SQ_1 and SQ_3 PWM contain four vector transitions from zero vector to active vector, which causes the duty-cycle loss, whereas SQ_2 has only two vector transitions from zero vector to active vector. As a result, SQ_2 has lower duty-cycle loss than SQ_1 and SQ_3.

For power quality comparison, within each sector, the two voltage pulses in SQ_1 and SQ_3 shrink to zero due to reaching to the end of sector, so that three zero vector intervals merge into one large interval, which causes a higher current ripple. During sector crossing, because of the sequence organization, SQ_3 has lower current oscillations in the input phase current than SQ_1. SQ_2 has no current oscillation during sector crossing; however, the oscillation happens in sub-sector crossing due to the sequence swapped. In conclusion, within each sector, the current of SQ_2 has a better performance. However, during sector crossing, SQ_3 has lower input current oscillation.

Under the same switching frequency, the power loss of SQ_2 is higher than SQ_1 and SQ_3. However, the conversion efficiency of SQ_2 can be improved by pre-turning on the hard-switching devices; in that way, the power loss of the 6-segment PWM would be lower than that of the 8-segment PWMs. However, the transformer frequency of the 6-segment PWM is lower than the 8-segment PWMs. Compared to SQ_1, SQ_3 does not have two hard-switching actions in each cycle; therefore, the switching loss is 14.42% less than the switching loss of SQ_1.

Chapter 5

Simulation and Experiment Verification

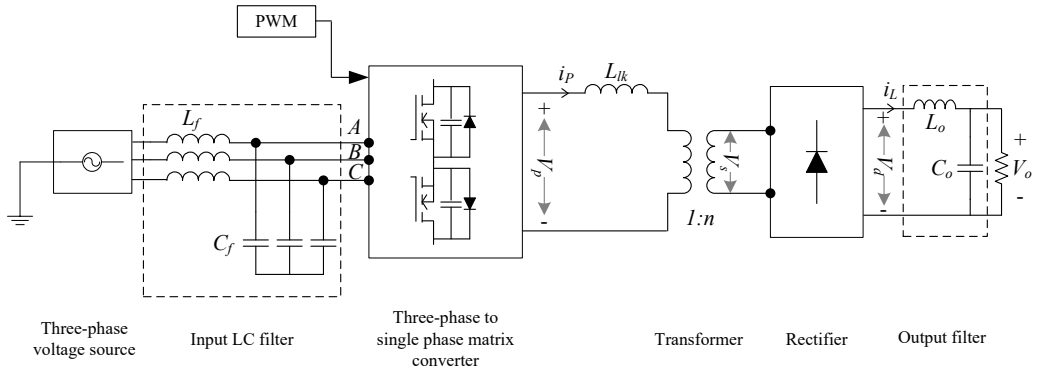
In this chapter, simulation and experiment verification of proposed PWM scheme are presented. The system is simulated in MATLAB/SIMULINK. The experiment is carried out on a platform verified the simulation results. Key parameters used in the simulation and experiment are given.

5.1 Simulation Verification

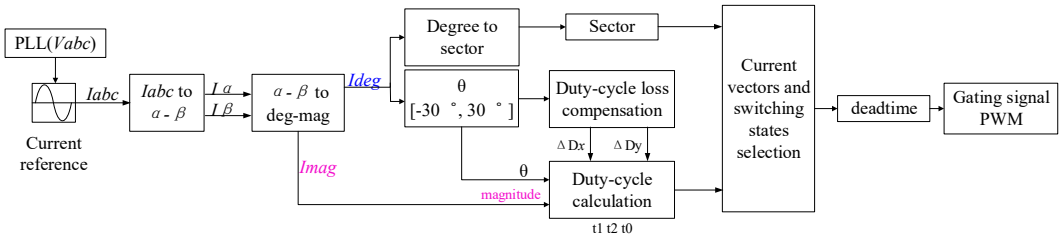
To verify the previous analysis of ZVS operation of proposed switching method, simulations are conducted on a 100 kHz three-phase buck type matrix based rectifier topology. Simulation parameters are listed in Table 5.1. The circuit configuration of the system is shown in Figure 5.1. The system was simulated using MATLAB/SIMULINK.

Table 5.1. Simulation parameters

Symbol	Parameter	Value
L_f	Input filter inductor	90 μH
C_f	Input filter capacitor	10 μF
f_{sw}	Switching frequency	100 kHz
V_o	Rectifier output voltage	330 V
L_{lk}	Transformer leakage inductance	5.7 μH
L_o	Output filter inductor	450 μH
C_o	Output filter capacitor	220 μF
f_{grid}	Grid side frequency	60 Hz
$V_{ll,rms}$	Grid voltage, rms value	180 V
n	Transformer turns ratio	2
m_a	Modulation index	0.8
P	Output power	3.3 kW



(a) Circuit configuration.



(b) PWM block diagram.

Figure 5.1 Circuit configuration used in simulation.

As illustrated in Figure 5.1, the power circuit of the three-phase matrix rectifier is powered by a three-phase AC voltage source, then connect to a three-phase to single-phase matrix converter through a LC filter. The output of matrix converter is connected to a high-frequency transformer. The secondary side of the transformer is a rectifier.

Figure 5.2 shows the simulation waveforms of transformer primary side voltage V_P, current I_P and secondary side voltage V_s and current I_s in two switching cycles. The simulation results at steady state are the same as the analysis in Chapter 3.

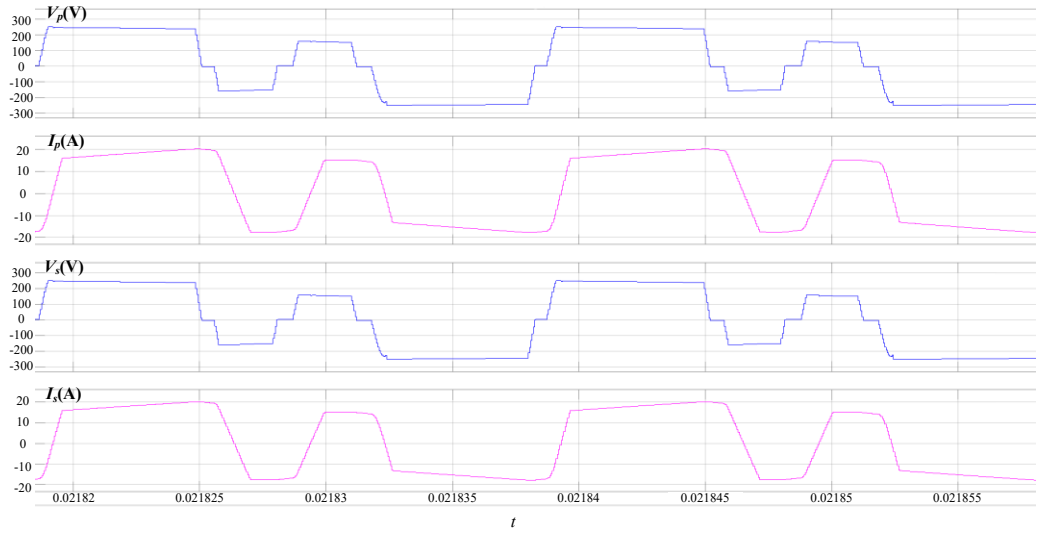


Figure 5.2 Simulation waveforms of transformer primary and secondary side voltage and current.

Figure 5.3 shows the grid side current of the proposed PWM scheme. The THD of the AC current is 1.54% with compensation. However, there're still some current spikes during sector crossing, which is caused by the hard switch actions during sector crossing.

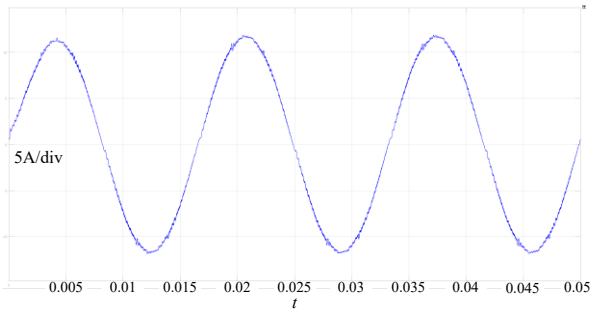


Figure 5.3 Simulation waveform of AC current with proposed PWM method.

To observe the ZVS operation of MOSFET switches, one switch S_{11} on phase A is selected, thereby showing the ZVS of all active switches. Figure 5.4 shows the simulation waveforms of phase A current i_a, the transformer primary side voltage v_p and the drain-source voltage V_{ds} of MOSFET S_{11} in six sectors operation. For traditional 8-segment PWM scheme, SQ_1, S_{11} is turned on under non-ZVS condition in sector III, so the MOSFET turn-on actions with proposed sequence are

analyzed at three locations of t_1, t_2, and t_3 as shown in Figure 5.5 for comparison.

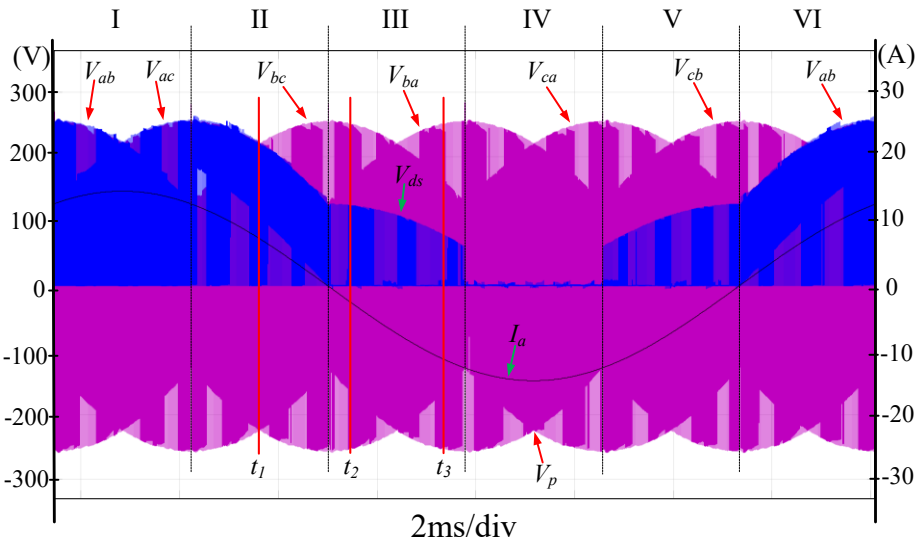
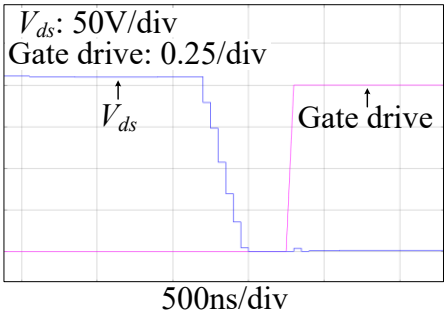


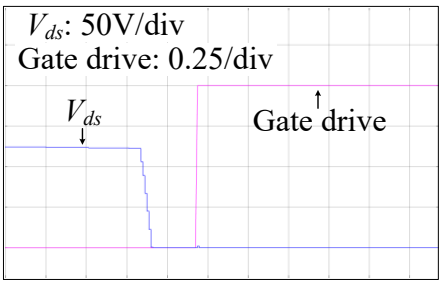
Figure 5.4 Simulation waveforms of V_P, i_a, and V_{ds} of S_{11}.

At t_1, S_{11} turn-on action represents the ZVS turn-on action for transitions within sectors other than sector III. At t_2 and t_3, S_{11} turn-on represents the ZVS turn-on actions during Sector III.

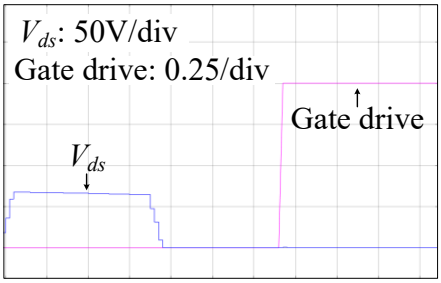
Figure 5.5 (a), (b), (c) represent the simulation results of MOSFET S_{11} at t_1, t_2, and t_3 respectively.



(a) at t_1



(b) at t_2



(c) at t_3

Figure 5.5 Simulation results of S_{11} turn-on actions during six sectors.

In the simulation results above, drain-source voltage V_{ds} tends to zero before gate-drive signals approaches high, which means that the body diode is on before the switch is turned on such that ZVS is realized.

5.2 Experiment Results

The experiment of this thesis is in collaboration with Ryerson University. Experiments are conducted on a 100kHz/180V isolated matrix rectifier system. The ZVS operation of the improvement 8-segment PWM scheme is digitally implemented using DSP and Field Programmable Gate Array (FPGA). The experiment parameters are listed in Table 5.2, which is the same parameters with the simulation. As shown, the PWM switching frequency is 100 kHz at rated output power 3.3 kW. The modulation strategies of the converter are the same as the ones adopted in simulation. The ZVS waveforms are also utilized to verify the analysis.

Table 5.2. Experimental prototype parameters

Symbol	Parameter	Value
L_f	Input filter inductor	90 µH
C_f	Input filter capacitor	10 µF
f_{sw}	Switching frequency	100 kHz
V_o	Rectifier output voltage	330 V
L_{lk}	Transformer leakage inductance	5.7 µH
L_o	Output filter inductor	450 µH
C_o	Output filter capacitor	220 µF
f_{grid}	Grid side frequency	60 Hz
$V_{ll,rms}$	Grid voltage, rms value	180 V
n	Transformer turns ratio	2
m_a	Modulation index	0.8
P	Output power	3.3 kW
T_r	Transformer	ZP47313TC
$S_{11} - S_{26}$	Matrix converter MOSFET	IPW60R041P6
$D_1 - D_4$	Rectifier diode	SCS215KG

Figure 5.6 shows the waveforms obtained from prototype operating at full load, including transformer primary side voltage V_p ,the drain-source voltage V_{ds} of MOSFET S_{11} in six sectors operation and one input phase current i_a in front of the input filter at light load condition. Figure 5.7 shows the transformer primary side voltage V_p and current i_p in two switching cycle with proposed PWM scheme.

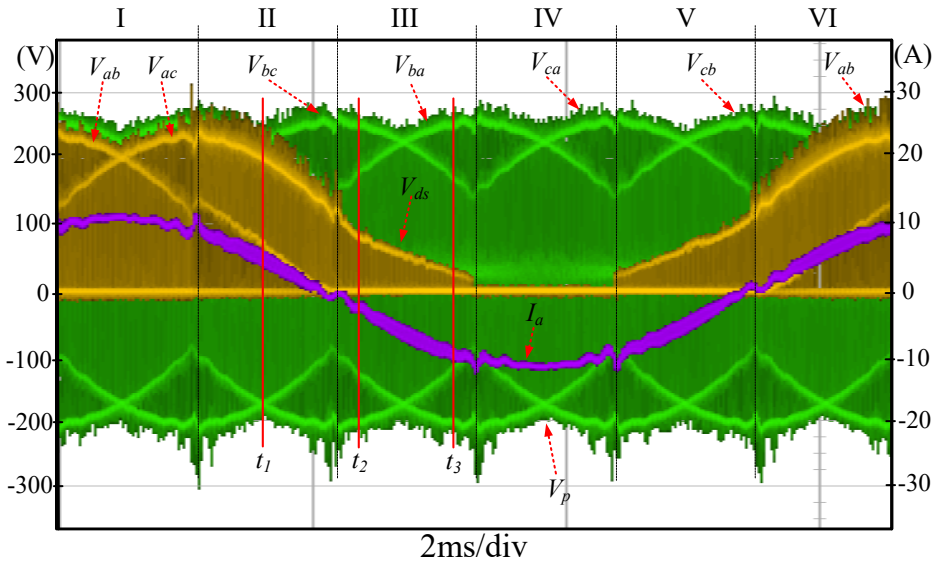


Figure 5.6 Experimental waveforms of V_P, i_a, and V_{ds} of S_{11} at full load.

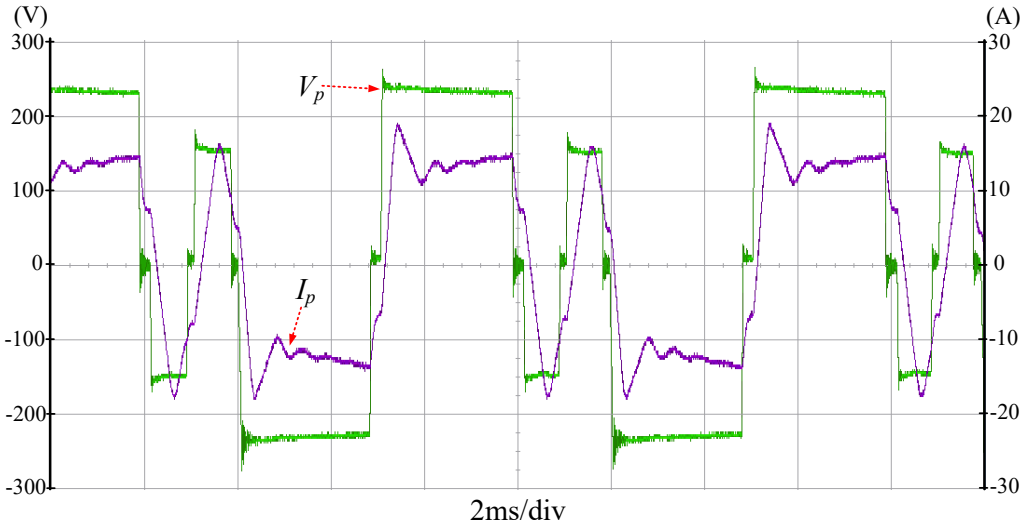
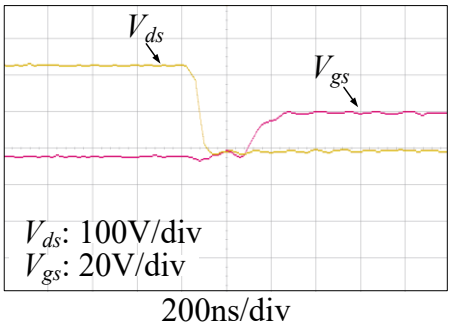
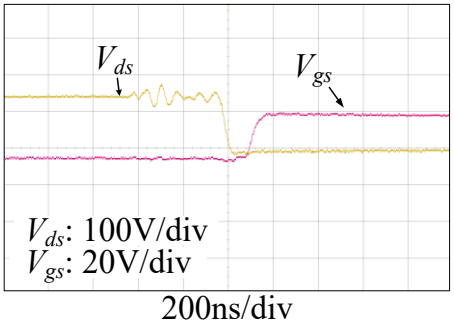


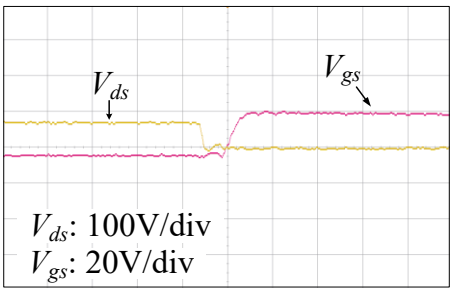
Figure 5.7 Experimental waveforms of V_P and i_p in two switching cycle.



(a) at t_1



(b) at t_2



(c) at t_3

Figure 5.8 Experimental results of S_{11} turn-on actions during six sectors.

Figure 5.8 (a), (b), (c) represent the experimental results of MOSFET S_{11} at t_1, t_2, and t_3 respectively. In the experimental results above, drain-source voltage V_{ds} tends to zero before gate-source voltage V_{gs} approaches high, which is the same as the simulation results.

Figure 5.9 shows the experimental waveforms of transformer primary side voltage v_p ,the drain-source voltage V_{ds} of MOSFET S_{11} in six sectors operation and one input phase current i_a in front of the input filter at light load condition (45% load). The shade area in Figure 5.9 is caused by the hard-switching actions at light load condition.

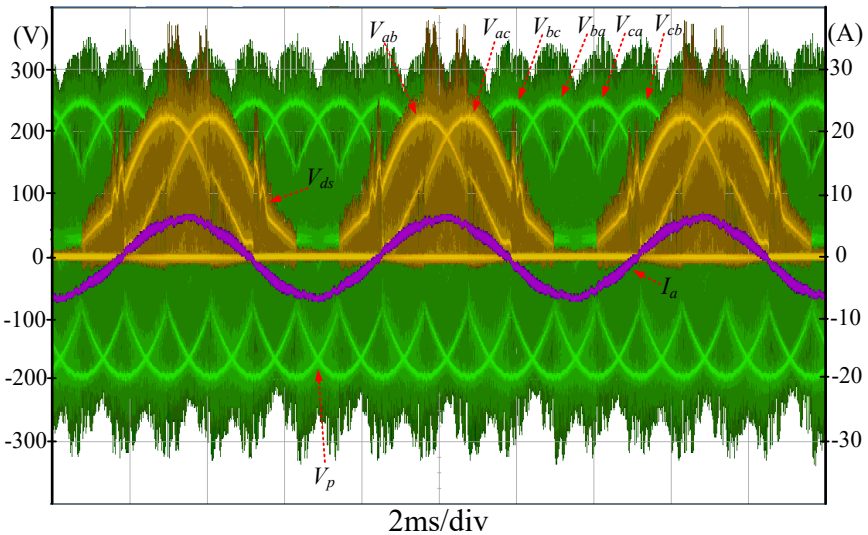
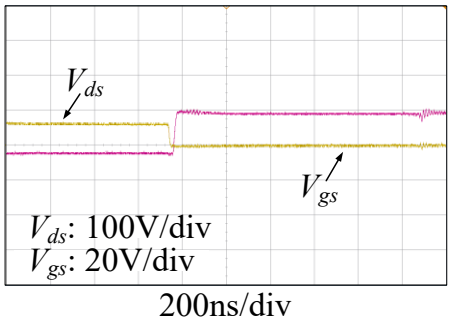
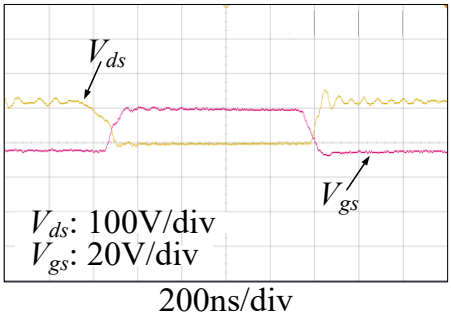


Figure 5.9 Experimental waveforms of V_P, V_a, and V_{ds} of S_{11} at 45% load.

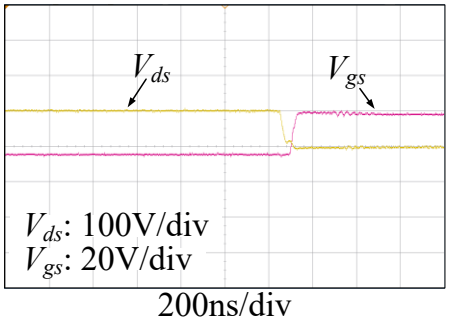
Figure 5.10 shows the detailed turn-on actions of S_{11} at different locations. In Figure 5.10 (a), the MOSFET are turned on under ZVS. In Figure 5.10 (b) and (c), the switch turns on before the drain-source voltage V_{ds} reaches zero.



(a)



(b)



(c)

Figure 5.10 Experimental results of S_{11} turn-on actions at 45% load.

Figure 5.11 shows the input phase current waveforms with proposed PWM scheme implementation under full load condition. The total harmonic distortion of the input phase current is 2.4%.

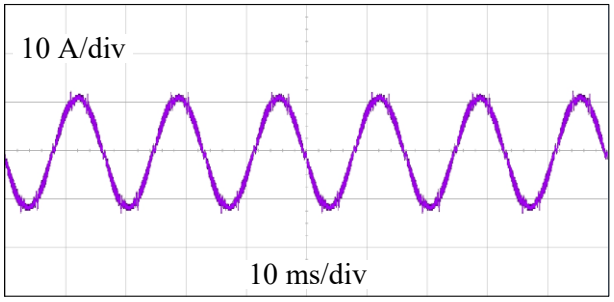


Figure 5.11 Experimental waveform of input phase current.

5.3 Summary

This chapter illustrates simulation and experimental results related to the proposed PWM scheme in Chapter 3. Circuit configurations and control parameters used in simulation and experiment are also presented.

The results confirm that the proposed PWM scheme is able to realize ZVS operation for all twelve MOSFET devices at full load condition.

The experimental results are analyzed under two different load conditions. At full load condition, all switches are turned on under zero voltage switching. At light load condition, the devices are turned on before the gate-source voltages reaches zero, so it’s not under ZVS.

Chapter 6

Conclusions and Future Work

This chapter summarizes the main contribution of this thesis and provides suggestions for future work.

6.1 Conclusions

This thesis presented topics related to the ZVS operation of the three-phase isolated matrix rectifier. As reviewed in Chapter 2, the traditional 8-segment PWM scheme utilizes all three phases as bypassing circuit in one switching cycle, which creates two hard-switch actions. As a result, the power loss is increased. The 6-segment PWM scheme has vector transitions between two active vectors. During this transition, in order to prepare for the ZVS operation of the next step, one switch should turn on under a non-ZVS condition. Thus, the 6-segment PWM has two hard-switch actions in each switching cycle. Furthermore, with the same PWM switching frequency, the transformer frequency of the 8-segment PWM is double that of the switching frequency of the 6-segment PWM, so that the 8-segment PWM has a smaller core.

Inspired by the 6-segment PWM, if inserting a zero vector between the two active vectors with the same operation principle, the two hard switch actions can be removed, so that a novel 8-segment PWM is proposed. A detailed analysis of ZVS operation is in Chapter 3. Due to all of the ZVS turn-on transitions, the switching loss is decreased, so that the proposed PWM can be applied in higher switching frequency applications. Furthermore, the proposed PWM sequence is symmetrical each half cycle, which makes the design progress easier. The comparison between the three PWM schemes is conducted in Chapter 4 from duty-cycle loss, output inductor current ripple, and switching and conduction loss.

The simulation and experimental results in Chapter 5 show that the proposed

PWM is able to realize ZVS operation for all devices. The THD of the grid side current is lower than 5%.

6.2 Future Work

Based on the research presented in this thesis, several extensions and modifications can be explored as follows:

Firstly, more work can be focused on reducing the switch actions under the ZVS condition in one switching cycle. In the traditional 8-segment PWM and proposed PWM, there are ten and twelve switch actions in each switching cycle, respectively. The power loss of the converter can be further reduced with reduced switch actions if all switches can turn-on under ZVS. Thus, the converter can work under a higher switching frequency.

Secondly, the detailed ZVS operation range of each PWM scheme can be specified, including modulation index range, maximum switching frequency of each PWM scheme, and load range.

Finally, the matrix rectifier can work under different PWM schemes, not only 6-segment and 8-segment PWMs. By rearrangement of the switching sequence, more PWM schemes can be created. The matrix converter output voltage is closer to a sinusoidal shape, and the system is more reliable.

Bibliography

[1] L. Gyugyi, "Generalized theory of static power frequency changers," Ph.D. dissertation, Univ. Salford, Manehester, UK, 1970.

[2] L. Gyugyi and B. R. Pelly, *Static Power frequency changers-theory, performance and application*. John Wiley & Sons, USA, 1976.

[3] M. Venturini, "A new sine wave in sine wave out conversion technique which eliminates reactive elements," in *Proc. International Conference on Power System Technology (Powercon)*, 1980, pp. E3.1–E3.15.

[4] Y. D. Yoon, and S. K. Sul, "Carrier based modulation technique for matrix converter," *IEEE Trans. Power Electron.*, vol. 21, no.6, pp. 1691–1703, Nov. 2006.

[5] C. Piao, and J. Y. Hung, "A unified carrier based modulation method for direct matrix converter," in *Proc. 2015 IEEE International Conference on Electro/Information Technology (EIT)*, Dekalb, USA, May 21–23 2015, pp. 122–128.

[6] K. Kobravi and R. Iravani, "A novel modulation strategy to minimize the number of commutation processes in the matrix converter," in *Proc. 2010 IEEE Energy Conversion Congress and Exposition,* Atlanta, USA, Sept. 12–16 2010, pp. 1867–1874.

[7] G. Li, "PWM algorithms for indirect matrix converter," in *Proc. 2012 IEEE 7th International Power Electronics and Motion Control Conference-ECCE Asia*, Harbin, China, Jun. 2–5, 2012.

[8] J. Haruna and H. Funato, "A direct space vector modulation method for three phase AC to single-phase AC isolated matrix converter," in *Proc. 2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC),* Taipei, Taiwan, Nov. 1–4, 2015.

[9] L. Xu, J. C. Clare, E. Lee, and Y. Li, "Capacitor clamped multilevel matrix converter space vector modulation," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 105–115, Jan. 2012.

[10] T. Zhao, X. Guo, J. Su, and D. Xu, "Improved Space Vector Modulation for Matrix Converter based Isolated Rectifiers," in *Proc. 40th Annual Conference of the IEEE Industrial Electronics Society*, Dallas, USA, Oct. 29–Nov. 1 2014, pp. 1532–1536.

[11] F. Gruson, P. Delarue, P. Le Moigne, and X. Cimetiere, "Matrix converter modulation minimizing switching losses and including the 6 rotating vectors of the Space Vector

representation," in *Proc. 2015 17th European Conference on Power Electronics and Applications,* Geneva, Switzerland, Sept. 8–10 2015, pp. 1–10.

[12] D. Casadei, G. Serra, A. Tani, and L. Zarri, "Matrix converter modulation strategies: a new general approach based on space-vector representation of the switch state," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 370–381, Apr. 2002.

[13] F. Yue, Patrick W. Wheeler, and J. C. Clare, "Relationship of modulation schemes for matrix converters," in *Proc. 3rd IET International Conference on Power Electronics, Machines and Drives*, Montreal, Canada, Sept. 4–6 2006, pp. 2477–2484.

[14] J. Afsharian, D. Xu, B. Gong, and Z. Yang, "Space vector demonstration and analysis of zero-voltage switching transitions in three-phase isolated PWM rectifier," in *Proc. 2015 IEEE Energy Conversion Congress and Exposition*, Montreal, Canada, Sept. 20–24 2015.

[15] L. Huber and D. Borojevic, "Space vector modulated three-phase to three-phase matrix converter with input power factor correction," *IEEE Trans. Ind. Appl.*, vol. 31, no. 6, pp. 1234–1246, Nov. 1995.

[16] M. Y. Lee, P. Wheeler, and C. Klumpner, "Space-vector modulated multilevel matrix converter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp.3385–3394, Oct. 2010.

[17] Y. Guo, J. Zhu, and C. Deng, "Three modulation modes of SVM for AC-AC matrix converter," in *Proc. 2008 IEEE Conference on Robotics, Automation and Mechatronics*, Chengdu, China, Sept. 21–24 2008, pp. 382–386.

[18] Y. Sun, W. Xiong, M. Su, X. Li, H. Dan, and J. Yang, "Topology and modulation for a new multilevel diode-clamped matrix converter," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6352–6360, Dec. 2014.

[19] X. Liu, P. C. Loh, F. Z. Peng, and P. Wang, "Optimal modulation of indirect Z-source matrix converter," in *Proc. 2010 International Power Electronics Conference (IPEC)*, Sapporo, Japan, Jun. 21–24 2010, pp. 3049–3056.

[20] M. Muroya, K. Shinohara, K. Iimori, and H. Sako, "Four-step commutation strategy of PWM rectifier of converter without DC link components for induction motor drive," in *Proc. 2001 IEEE International Electric Machines and Drives Conference (IEMDC)*, Cambridge, MA USA, Jun. 17-20, 2001, pp. 770–772.

[21] J. Holtz and U. Boelkens, "Direct frequency converter with sinusoidal line currents for speed-variable motors," *IEEE Trans. Ind. Electron.*, vol. 36, no. 4, pp. 475–479, Nov. 1989.

[22] L. Wei and T. A. Lipo, "A novel matrix converter topology with simple commutation," in *Proc. 36th IAS Annual Meeting*, Chicago, USA, Sept. 30–Oct. 4, 2001, vol. 3, pp.1749–1754.

[23] L. Wei, and T.A. Lipo, "Matrix converter with reduced number of switches," in *Proc. of Conf. Record of the 20th WEMPEC anniversary meeting*, Madison, USA, Oct. 24–25, 2001.

[24] J. W. Kolar, M. Baumann, F. Schafmeister, and H. Ertl, "Novel three-phase AC-DC-AC sparse matrix converter," in *Proc. 17th IEEE Applied Power Electronics Conference and Exposition (APEC)*, Dallas, USA, Mar. 10–14, 2002, vol. 2, pp. 777–791.

[25] J. Rodriguez, "High performance dc motor drive using a PWM rectifier with power transistors," *IEE Proc. B, Elect. Power Appl.*, vol. 134, no. 1, pp. 9–13, Jan. 1987.

[26] D. G. Holmes and T. A. Lipo, "Implementation of a controlled rectifier using AC-AC matrix converter theory," *IEEE Trans. Power Electron.*, vol. 7. no.1, pp. 240–250, Jan.1992.

[27] M. Su, H. Wang, Y. Sun, J. Yang, W. Xiong, and Y. Liu, "AC/DC matrix converter with an optimized modulation strategy for V2G applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5736–5745, Dec. 2013.

[28] R. Metidji, B. Metidji, and B. Mendil, "Design and implementation of unity power factor fuzzy battery charger using ultrasparse matrix rectifier," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2269–2276, May 2013.

[29] K. You, D. Xiao, M. F. Rahman, and M. N. Uddin, "Applying reduced general direct space vector modulation approach of AC–AC matrix converter theory to achieve direct power factor controlled three-phase AC–DC matrix rectifier," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 2243–2257, May-Jun. 2014.

[30] A. K. Singh, E. Jeyasankar, P. Das, and S. K. Panda, "A novel matrix based non-isolated buck-boost converter for more electrix aircraft," in *Proc. 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Florence, Italy, Oct. 23–26, 2016, pp. 1233–1238.

[31] A. K. Singh, E. Jeyasankar, P. Das, and S. K. Panda, “A matrix based nonisolated three phase ac-dc rectifier with large step-down voltage gain,” *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4796–4811, Jun. 2017.

[32] S. Manias and P. D. Ziogas, “A novel sinewave in AC to DC converter with high-frequency transformer isolation,” *IEEE Trans. Ind. Electron.*, vol. IE-32, no. 4, pp. 430–438, Nov. 1985.

[33] K. Inagaki, T. Furuhashi, A. Ishiguro, M. Ishida, and S. Okuma, “A new PWM control method for AC to DC converters with high-frequency transformer isolation,” *IEEE Trans. Ind. Appl.*, vol. 29, no. 3, pp. 486–492, May-Jun. 1993.

[34] V. Vlatković and D. Borojević, “Digital-signal-processor-based control of three-phase space vector modulated converters,” *IEEE Trans. Ind. Electron.*, vol. 41, no. 3, pp. 326–332, Jun. 1994.

[35] V. Vlatković, D. Borojević, and F. C. Lee, “A zero-voltage switched three-phase isolated PWM buck rectifier,” *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 148–157, Mar. 1995.

[36] K. Wang, F. C. Lee, D. Boroyevich, and X. Yan, “A new quasi-single-stage isolated three-phase ZVZCS buck PWM rectifier,” in *Proc. 27th Annual IEEE Power Electronics Specialists Conference (PESC)*, Baveno, Italy, Jun. 23–27, 1996, vol. 1, pp. 449–455.

[37] S. E. Joung, S. H., Huh, “A soft-switched DSP based isolated three phase PWM buck rectifier,” in *Proc. 19th International Telecommunications Energy Conference (INTELEC)*, Melbourne, Australia, Oct. 23, 1997, pp. 338–343.

[38] R. García-Gil, J. M. Espí, E. J. Dede, and E. Sanchis-Kilders, “A bidirectional and isolated three-phase rectifier with soft-switching operation,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 765–773, Jun. 2005.

[39] S. Ratanapanachote, H. J. Cha, and P. N. Enjeti, “A digitally controlled switch mode power supply based on matrix converter,” *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 124–130, Jan. 2006.

[40] Z. Yan, K. Zhang, J. Li, and W. Wu, “A novel absolute value logic SPWM control strategy based on De–Re-coupling idea for high frequency link matrix rectifier,” *IEEE Trans. Ind. Inform.*, vol. 9, no. 2, pp. 1188–1198, May 2013.

[41] T. Zhao, X. Guo, J. Su, and D. Xu, “Improved space vector modulation for matrix converter based isolated rectifiers,” in *Proc. 40th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Dallas, USA, Oct. 29–Nov. 1 2014, pp. 1532–1536.

[42] T. Zhao, J. Su, D. Xu, and Meiqin Mao, “Commutation compensation for matrix based rectifier due to leakage inductances of isolation transformer,” in *Proc. 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Seoul, South Korea, Jun. 1–5 2015, pp. 1803–1808.

[43] J. Afsharian, D. Xu, B. Gong, and Z. Yang, “Reduced duty-cycle loss and output inductor current ripple in a ZVS switched three-phase isolated PWM rectifier,” in *Proc. 2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, USA, Mar. 20–24, 2016, pp. 33–37.

[44] J. W. Kolar, U. Drofenik, and F. C. Zach, “VIENNA rectifier II-a novel single-stage high-frequency isolated three-phase PWM rectifier system,” *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 674–691, Aug. 1999.

[45] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar, “Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V dc distribution systems,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1732–1744, Apr. 2012.

[46] K. D. T. Ngo, “Topology and analysis in PWM inversion, rectification, and cycloconversion,” Ph.D. dissertation, California Inst. Technol., Pasadena, USA, May 1984.

[47] Y. Matsui, K. Suzuki, and T. Takeshita, “ PWM strategy and loss reduction of high-frequency link ac-dc converter using SiC-MOSFET,” in *Proc. 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Florence, Italy, Oct. 23–26, 2016, pp. 1400–1405.

[48] J. Afsharian, D. Xu, B. Wu, B. Gong, and Z. Yang, “The optimal PWM modulation and commutation scheme for a three-phase isolated buck matrix-type rectifier,” *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 110–124, Jan. 2018.

[49] Z. D. Fang, D. Y. Chen, and F. C. Lee, “Designing a high frequency snubberless FET power inverter,” in *Proc. International Conference on Power System Technology (Powercon)*, 1984, pp. D1.4.1–D1.4.10.

[50] R. A. Fisher, K. D. T. Ngo, and M. H. Kuo, “500 KHz 250 W dc-dc converter with multiple output controlled by phase-shift PWM and magnetic amplifiers,” in *Proc. High Frequency Power Conversion Conf.*, May 1988, vol. 3, pp. 100–110.

[51] L. H. Mweene, C. A. Wright, and M. F. Schlecht, “A 1 kW 500 kHz front-end converter for a distributed power supply system,” *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 398–407, Jul. 1991.

[52] J. A. Sabaté, V. Vlatković, R. B. Ridley, F. C. Lee, and B. H. Cho, “Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter,” in *Proc. Fifth Annual Applied Power Electronics Conference and Exposition (APEC)*, Los Angeles, USA, Mar. 11–16, 1990, pp. 275–284.

[53] J. A. Sabaté, V. Vlatković, R. B. Ridley, and F. C. Lee, “High-voltage high-power ZVS full-bridge PWM converter employing an active snubber,” in *Proc. Sixth Annual Applied Power Electronics Conference and Exposition (APEC)*, Dallas, USA, Mar. 11–16, 1990, pp. 158–163.

[54] L. Zhang, C. Watthanasaran, and W. Shepherd, “Control of AC-AC matrix converter for unbalanced and/or distorted supply voltage in *Proc. 2001 IEEE 32nd Annual Power Electronics Specialists Conference (PESC)*, Vancouver, Canada, Jun. 17–21, 2001, vol. 2, pp. 1108–1113.

[55] S. Bemet, S. Ponnaluri, and R. Teichmann, “Design and loss comparison of matrix converters and voltage-source converters for modem AC drives,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 304–314, Apr. 2002.

[56] J. Rodriguez, E. Silva, F. Blaabjerg, P. Wheeler, J. Clare, and J. Pontt, ”Matrix converter controlled with the direct transfer function approach: analysis, modelling and simulation,” *International Journal of Electronics*, vol. 92, no. 2, pp. 63–85, Feb. 2005.

[57] K. Huang and Y. He, “Investigation of a matrix converter excited brushless doubly-fed machine wind-power generation system,” in *Proc. Fifth International Conference on Power Electronics and Drive Systems (PEDS)*, Singapore, Nov. 17–20, 2003, vol. 1, pp. 743–748.

[58] Y. Wang, Z. Lu, H. Wen, and Y. Wang, “Dead-time compensation based on the improved space vector modulation strategy for matrix converter,” in *Proc. 2005 IEEE 36nd Annual Power Electronics Specialists Conference (PESC)*, Recife, Brazil, Jun. 12–16, 2005, vol. 2, pp. 1108–1113.

[59] H. J. Cha and P. N. Enjeti, “An approach to reduce common-mode voltage in matrix converter,” *IEEE Trans. Ind. Appl.*, vol. 39, no. 4, pp. 1151–1159, Jul.-Aug. 2003.

[60] F. Blaabjerg, D. Casadei, C. Klumpner, and M. Matteini, “Comparison of two current modulation strategies for matrix converters under unbalanced input voltage conditions,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 289–296, Apr. 2002.

[61] E. P. Wiechmann, P. D. Ziogas, and V. R. Stefanovic, “A novel bilateral power conversion scheme for variable frequency static power supplies,” *IEEE Trans. Ind. Appl.*, vol. IA-21, no. 5, pp. 1226–1233, Sept. 1985.

[62] D. Casadei, G. Serra, A. Tani, and L. Zarri, “Optimal use of zero vectors for minimizing the output current distortion in matrix converters,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 326–336, Feb. 2009.

[63] L. Wang, D. Zhou, K. Sun, and L. Huang, “A novel method to enhance the voltage transfer ratio of matrix converter,” in *Proc. 2004 IEEE Region 10 Conference TENCON*, Chiang Mai, Thailand, Nov. 21–24, 2004, vol. 4, pp. 81–84.

[64] Z. Idris, M. Hamzah, and A. Omar, “Implementation of single-phase matrix converter as a direct AC-AC converter synthesized using sinusoidal pulse width modulation with passive load condition,” in *Proc. International Conference on Power Electronics and Drives Systems (PEDS)*, Kuala Lumpur, Malaysia, Nov. 28–Dec. 1, 2005, vol. 2, pp. 1536–1541.

[65] P. C. Loh, R. Rong, F. Blaabjerg, and P. Wang, “Digital carrier modulation and sampling issues of matrix converters,” *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1690–1700, Jul. 2009.

[66] P. Kiatsookkanatorn and S. Sangwongwanich, “A unified PWM strategy for matrix converters and its dipolar PWM realization,” in *Proc. 2010 International Power Electronics Conference (IPEC)*, Sapporo, Japan, Jun. 21–24, 2010, pp. 3072–3079.

[67] Y. D. Yoon and S. K. Sul, “Carrier-based modulation method for matrix converter with input power factor control and under unbalanced input voltage conditions,” in *Proc. Twenty Second Annual IEEE Applied Power Electronics Conference (APEC)*, Anaheim, USA, Feb. 25–Mar. 1, 2007, pp. 310–314.

[68] S. Thuta, K. Mohapatra, and N. Mohan, “Matrix converter over-modulation using carrier-based control：Maximizing the voltage transfer ratio,” in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, Jun. 15–19, 2008, pp. 1727–1733.

[69] T. Satish, K. Mohapatra, and N. Mohan, “Steady state over—modulation of matrix converter using simplified carrier based control,” in *Proc. 33rd Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Taipei, Taiwan, Nov. 5–8, 2007, pp. 1817–1822.

[70] P. Loh, R. Rong, F. Blaabjerg, L. Shan, and P. Wang, “Carrier-based modulation schemes for various three-level matrix converters,” in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, Jun. 15–19, 2008, pp. 1720–1726.

[71] J. Oyama, X. Xia, T. Higuchi, and E. Yamada, “Displacement angle control of matrix converter,” in *Proc. 28th Annual IEEE Power Electronics Specialists Conference (PESC)*, Saint Louis, USA, Jun. 22–27, 2007, vol. 2, pp. 1033–1039.

[72] X. Ma, G. Tan, X. Wu, Y. Fang, X. Zhang, and Y. Han, “Research on improved four-step commutation strategy of matrix converter based on two line voltage synthesis,” in *Proc. Second International Conference on Innovative*

Computing, Information and Control (ICICIC), Kumamoto, Japan, Sept. 5–7, 2007.

[73] J. K. Kang, H. Hara, A. M. Hava, E. Yamamoto, E. Watanabe, and T. Kume, "The matrix converters drive performance under abnormal input voltage conditions," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 721–730, Sept. 2002.

[74] J. K. Kang, H. Hara, E. Yamamoto, E. Watanabe, and J. Oyama, "Input harmonics damping for high power quality applications of matrix converter," in *Proc. 38th IAS Annual Meeting*, Salt Lake City, USA, Oct. 12–16, 2003, vol. 3, pp. 1498–1503.

[75] H. Hara, E. Yamamoto, J. K. Kang, and T. Kume, "Improvement of output voltage control performance for low-speed operation of matrix converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1372–1378, Nov. 2005.

[76] C. Ortega, A. Arias, C. Caruana, J. Balcells, and G. M. Asher, "Improved waveform quality in the direct torque control of matrix-converter-fed PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2101–2110, Jun. 2010.

[77] D. Xiao and F. Rahman, "A modified DTC for matrix converter drives using two switching conngurations," in *Proc. 13th European Conference on Power Electronics and Applications (EPE)*, Barcelona, Spain, Sept. 8–10, 2009.

[78] K. B. Lee and F. Blaabjerg, "Sensorless DTC-SVM for induction motor driven by a matrix converter using a parameter estimation strategy," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 512–521, Feb. 2008.

[79] J. Wang and J. Jiang, "Variable-structure direct torque control for induction motor driven by a matrix converter with over modulation strategy," in *Proc. IEEE 6th International Power Electronics and Motion Control Conference (IPEMC)*, Wuhan, China, May 17–20, 2009, pp. 580–584.

[80] D. Xiao and F. Rahman, "An improved DTC for matrix converter drives using multi-mode ISVM and unity input power factor correction," in *Proc. 2009 13th European Conference on Power Electronics and Applications*, Barcelona, Spain, Sept. 8–10, 2009.

[81] M. E. Rivera, R. E. Vargas, J. R. Espinoza, and J. R. Rodriguez, “Behavior of the predictive DTC based matrix converter under unbalanced AC supply,” in *Proc. 42nd IAS Annual Meeting*, New Orleans, USA, Sept. 23–27, 2007, pp. 202–207.

[82] R. Vargas, J. Rodriguez, U. Ammann, and P. W. Wheeler, “Predictive current control of an induction machine fed by a matrix converter with reactive power control,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4362–4371, Dec. 2008.

[83] F. Morel, J. M. Retif, X. Lin-Shi, B. Allard, and P. Bevilacqua, “A predictive control for a matrix converter-fed permanent magnet synchronous machine,” in *Proc. IEEE Power Electronics Specialists Conference (PESC)*, Rhodes, Greece, Jun. 15–19, 2008, pp. 15–21.

[84] R. Vargas, U. Ammann, J. Rodriguez, and Jorge Pontt, “Predictive strategy to control common-mode voltage in loads fed by matrix converters,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4372–4380, Dec. 2008.

[85] R. Vargas, U. Ammann, and J. Rodriguez, “Predictive approach to increase efficiency and reduce switching losses on matrix converters,” *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 894–902, Apr. 2009.

[86] P. Correa, J. Rodriguez, M. Rivera, J. R. Espinoza, and J. W. Kolar, “Predictive control of an indirect matrix converter,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1847–1853, Jun. 2009.

[87] M. Rivera, P. Correa, J. Rodriguez, I. Lizama, and J. Espinoza, “Predictive control of the indirect matrix converter with active damping,” in *Proc. IEEE 6th International Power Electronics and Motion Control Conference (IPEMC)*, Wuhan, China, May 17–20, 2009, pp. 1738–1744.

[88] J. Rodriguez, J. Kolar, J. Espinoza, M. Rivera, and C. Rojas, ”Predictive current control with reactive power minimization in an indirect matrix converter,” in *Proc. IEEE International Conference on Industrial Technology (ICIT)*, Vina del Mar, Chile, Mar. 14–17, 2010, pp. 1839–1844.

[89] A. Alesina and M. Venturini, “Solid-state power conversion: an analysis approach to generalized transformer synthesis,” *IEEE Trans. Circuits Syst.*, vol. 28, no. 4, pp. 319–330, Apr. 1981.

[90] A. Alesina and M. G. B. Venturini, “Analysis and design of optimum amplitude nine switch direct AC-AC converters,” *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 101–112, Jan. 1989.

[91] L. Huber and D. Borojević, “Space vector modulator for forced commutated cycloconverters,” in *Proc. IAS Annual Meeting*, San Diego, USA, Oct. 1–5, 1989, vol. 1, pp. 871–876.

[92] B. Wu, *High-power converters and ac drives. Hoboken*. John Wiley & Sons, NJ, USA, 2006.

[93] V. Vlatkovic, “Three-phase power conversion using soft-switching PWM Techniques,” Ph.D. dissertation, Virginia Polytechnic Institute and State Univ., Blacksburg, Virginia, USA, 1994.

[94] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: converters, applications and design*, Third Edition, John Wiley & Sons, USA, 2002.

[95] J. B. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, “Coss related energy loss in power MOSFETs used in zero-voltage-switched applications,” in *Proc. Twenty-Ninth Annual IEEE Applied Power Electronics Conference (APEC)*, Fort Worth, USA, Mar. 16–20, 2014, pp. 150–156.