Grid-Interfacing Converter System Leveraging Parallel Modularity and Interleaving Technique

by

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Abstract

Grid-tied power converter system is the key link in many power conversion applications such as renewable energy power generation, changing of electric vehicle, and industry motor drives. The performance of the grid interfacing converter has a substantial impact on the overall performance of the entire system. One popular design concept of the grid-tied converter system is adopting modular parallel converters. With such design, system reliability can be enhanced and efficiency improvement is achievable. To further elevate system performances, interleaving technique is a promising approach to operate the parallel converters. In spite of the advantages of parallel modularity and interleaving technique, recent development trend has imposed further challenging requirements on converter system design.

High power density is one of the key challenges. Specifically for modular parallel converters, the common mode circulating current (CMCC), as a side effect of interleaving technique, will increase the size of the common mode (CM) choke in each converter module. To fulfill the power density requirement, minimizing CMCC is a mandate.

In parallel to the power density requirement, stable operation of grid-tied converters is another critical issue. With the increasing penetration of LCL-filtered power converters in the utility grid, the filter resonance issue has become a sever challenge. Eliminating the LCL filter, and thus the filter resonance related issues, while maintaining small filter size and grid code compatible current quality is highly desirable, but also a challenging task.

The focus of this thesis is thus situated on the addressing above challenges and seeking potential opportunities for further improvements. To reduce CMCC while preserving parallel modularity, the first step is a comprehensive harmonic distribution analysis for generalized pulse width modulation (PWM) schemes. The analysis results in a two-degree-of-freedom (2DoF) interleaving scheme which can effectively minimize the CMCC in modular parallel converter system regardless the number or type of the converters. In addition, leveraging the interleaving technique, a new system design concept is proposed to eliminate the LCL filter in each converter module. A comprehensive system level design analysis indicates that only small L filter is required to meet the grid code when there are five or six interleaved converter modules in a system. As such, the filter resonance related issues can be completely eliminated. More importantly, the total filter size with the proposed design can be substantially reduced as compared to the LCL filter based design. To further enhance system performances, a novel multilevel converter topology concept, i.e. internal parallel converter (IPC), is proposed to integrate parallel modularity and interleaving technique into one multilevel converter. A high density Gallium Nitride (GaN) device based IPC prototype is also developed in this thesis as a demonstration.

Preface

This thesis is an original work by Zhongyi Quan under the supervison of Prof. Yunwei Li. Some parts of this thesis have been published as journal publications. These publications are reorganized in this thesis for better and clearer presentations.

Part of Chapter 1 and Appendix A have been published as:

- Z. Quan and Y. W. Li, "A Three-Level Space Vector Modulation Scheme for Paralleled Converters to Reduce Circulating Current and Common-Mode Voltage," IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 703-714, Jan. 2017.

Chapter 3 combines two published journal papers:

- Z. Quan and Y. W. Li, "Suppressing Zero-Sequence Circulating Current of Modular Interleaved Three-Phase Converters Using Carrier Phase Shift PWM," IEEE Transactions on Industry Applications, vol. 53, no. 4, pp. 3782-3792, July-Aug. 2017.

- Z. Quan and Y. W. Li, "Impact of PWM Schemes on the Common-Mode Voltage of Interleaved Three-Phase Two-Level Voltage Source Converters," IEEE Transactions on Industrial Electronics, vol. 66, no. 2, pp. 852-864, Feb. 2019.

Chapter 2 and Chapter 4 are merged and have been accepted for publication as:

- Z. Quan and Y. W. Li, "Phase-Disposition PWM based 2DoF Interleaving Scheme for Minimizing High Frequency ZSCC in Modular Parallel

Three-level Converters," IEEE Transactions on Power Electronics, in press.

Part of Chapter 5 has been accepted for publication at APEC 2019, and submitted as a journal paper.

- Z. Quan, Y. W. Li, C. Jiang, "Design of Interleaved Converters with Minimum Filtering Requirement," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019.
- Z. Quan, Y. W. Li, C. Jiang, "Reconsideration of Grid-Friendly Low Order Filter Enabled by Parallel Converters", IEEE Transactions on Power Electronics, under review.

Chapter 6 and part of Chapter 7 have been published/submitted in the following papers.

- Z. Quan, Y. W. Li, "Multilevel Voltage Source Converter Topologies with Internal Parallel Modularity," IEEE Transactions on Industry Applications, under review.
- Z. Quan and Y. W. Li, "Multilevel Converter Topologies with Internally Paralleled Power Stages," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 5651-5656.

To my family.

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trust they have put in me. To my loving and supportive wife Jinman, no words are enough to express my gratitude for your love, understanding, and support, and for making my life so much more enjoyable. With you, I can always find my strength. To my lovely daughter Olivia, thank you for coming to my life. Watching you grow up little by little gives me so much joy.

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Acronyms

ANPC	Active neutral point clamped
APOD	Alternative phase opposition disposition
CHB	Cascaded H-bridge
CM	Common mode
CMCC	Common mode circulating current
CMO	Common mode offset
DFI	Double Fourier Integral
DM	Differential mode
DMCC	Differential mode circulating current
DoF	Degree-of-freedom
DPWM	Discontinuous PWM
EMI	Electromagnetic interference
FC	Flying capacitor
GaN	Gallium Nitride
HSF	High switching frequency
HVDC	High voltage direct voltage
IPC	Internal parallel converter
LSF	Low switching frequency
MMC	Modular multilevel converter
MVD	Medium voltage drive
NPC	Neutral point clamped

PD	Phase disposition
POD	Phase opposition disposition
PWM	Pulse-width modulation
S1DoF	Symmetrical one-degree-of-freedom
S2DoF	Symmetrical two-degree-of-freedom
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse-width modulation
SST	Solid state transformer
SVM	Space vector modulation
SVPWM	Space vector pulse-width modulation
VSC	Voltage source converter
WBG	Wide band-gap
ZSCC	Zero-sequence circulating current

Chapter 1

Introduction

Transition towards a more efficient and more sustainable energy world has been a primary goal in our society. To achieve this goal, much effort has been made. In recent decades, we have witnessed the increasing penetration of renewable energy in the utility grid, the rapid growth of electric vehicle market, the increased efficiency of data center, the implementation of energy storage units, and the wide installation of industrial drives. Behind these major innovations, is the power electronics technology serving as one of the key driving forces.

On the other hand, the rapid deployment of the emerging applications has imposed increasing requirements on system the power density, reliability, and cost of the power electronics system. Taking three-phase solar string inverter as an example, the state-of-the-art commercial product is around 0.5kW/L for volume and 1.4kW/kg for weight [1], which requires two well trained workers to install. As the number of string inverters can reach up to several thousands, the installation cost will be significant [2]. To lower the power generation cost, further improvements in system power density, as well as efficiency, are highly desirable. To achieve higher performance, recent trend in power electronics system is to fractionalize the power conversion process with modular architecture [3–9]. In medium (1kV $\sim$ 100kV) and high voltage ($>$ 100kV) applications such as locomotive traction [9, 10], medium voltage drives (MVD) [11–14], and high voltage DC (HVDC) transmission applications [15, 16], the modular system has been well established as the cascaded H-bridge (CHB) converter [17–

19], the solid state transformer (SST) [9, 20], and the modular multilevel converter (MMC) [3, 21, 22] have been widely implemented due to the limited semiconductor voltage rating. For low voltage (< 1kV) applications, on the other hand, new designs become more prone to incorporate modularity owing to the increased requirements on system power density, efficiency, and reliability [8, 23–26]. Particularly with the emergence of wide band-gap (WBG) devices like Silicon Carbide (SiC) [26, 27] and Gallium Nitride (GaN) [25], and the new Silicon high speed devices like CoolMOS [28, 29], the modular architecture becomes more suitable considering the limited voltage and current ratings of these new devices. Moreover, with proper operation principle, a modular system can also achieve lower harmonic distortion and electromagnetic interference (EMI) [30, 31], which are particularly attractive for WBG devices that can produce severer overvoltage and EMI issues than their Silicon equivalents [32, 33].

Modularity in a power conversion system can be realized through series connection or parallel connection of module converters. Architecture with series modularity is usually applied to reduce the voltage stress over the semiconductor devices. With the topologies like CHB and MMC, series architecture has been widely applied in applications such as telecom rectifier [24], data center power supply [34], integrated modular motor drives [35, 36], etc. On the other hand, parallel-modularity is able to reduce the current stress over the devices. It has been popular in applications such as motor/generator drives [37–40], consumer electronics [41], and many grid-tied applications [27, 30, 42, 43]. This thesis focuses on addressing the key issues of modular parallel converter system for the grid-interfaced power conversion applications.

1.1 Modular Parallel Converters in Grid-Tied Applications

The typical structure of modular parallel converters can be illustrated in **Fig. 1.1 (a)**, where one can see that the key feature of such an architecture is that the parallel converters share the same DC bus. Each converter can be seen as a

converter module. The typical configurations of a converter module are shown in **Fig. 1.1 (b) and (c)**. In this thesis, the voltage source converter (VSC) is considered since it is the most commonly adopted technology in practical applications. The topology of the VSC can be either a two-level (2L) one or a multilevel one. Usually the converter modules in the same system have the same topology. To attenuate the switching harmonics, each converter module is equipped with a differential mode (DM) output filter, which is usually an LCL type [44]. In addition to the LCL filter, a common mode (CM) choke is usually required in each converter module to suppress the CM noises and CM current [45]. Note that the CM choke can be placed at either the AC side or the DC side of each converter module. If the amplitude of the CM current is small enough, L_c can be further fabricated as three-limb inductors [37], which may have smaller size as compared to single-phase inductors [46, 47]. The CM choke and three-phase output filter can be integrated with the same core to further reduce filter size [48–50]. It is worthwhile to note that in some occasions, each converter module may only contain a DM filter made of single-phase inductors, and the CM choke may not be adopted since 1/3 of the output filter inductance will be serving as CM inductance.

With the configuration shown in **Fig. 1.1**, the converter modules are decoupled with each other, modularity, and therefore multiple power channels, become available. The power flow in modular parallel converters can be illustrated in **Fig. 1.2 (a)**, where each converter module bears a portion of the total power. The power can be equally or unequally shared among the converter modules, depending on the requirement during the operation. An inherent benefit of the modular parallel converter architecture is the fault tolerant capability, which is an important feature for applications where down-time cost is significant [51]. As shown in **Fig. 1.2 (b)**, when one converter module experiences a fault, the other modules can still operate normally. Compared to non-parallel system, the parallel converters also have the capability of enhancing system reliability and extending system lifetime by over 30% by implementing one or more redundant converter modules [52]. In some other cases, one or more converter modules can also be shut down to improve system

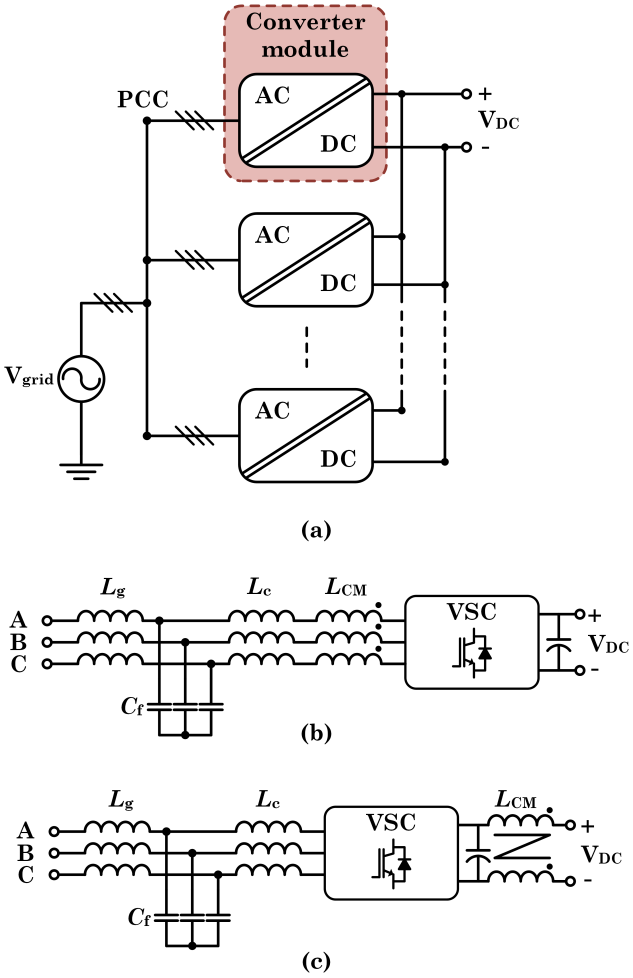


Figure 1.1. The modular parallel converter system, (a) the general structure, (b) the typical configuration of a converter module with CM choke at AC side, and (c) converter module with DC side CM choke.

efficiency in light load condition [40].

1.2 Interleaving Operation

The converter modules can be operated in two modes, i.e. the synchronous mode or the interleaving mode. In synchronous mode, the carrier signals of the converters are synchronized. As such, the combined output voltage of the converters will be the same as that of one converter module. For example, if the converter modules are 2L converters, then the combined output voltage is still a 2L one. On the other hand, if operated in interleaving mode, the carrier signals of the converters will be phase-shifted from each other. Usually, this

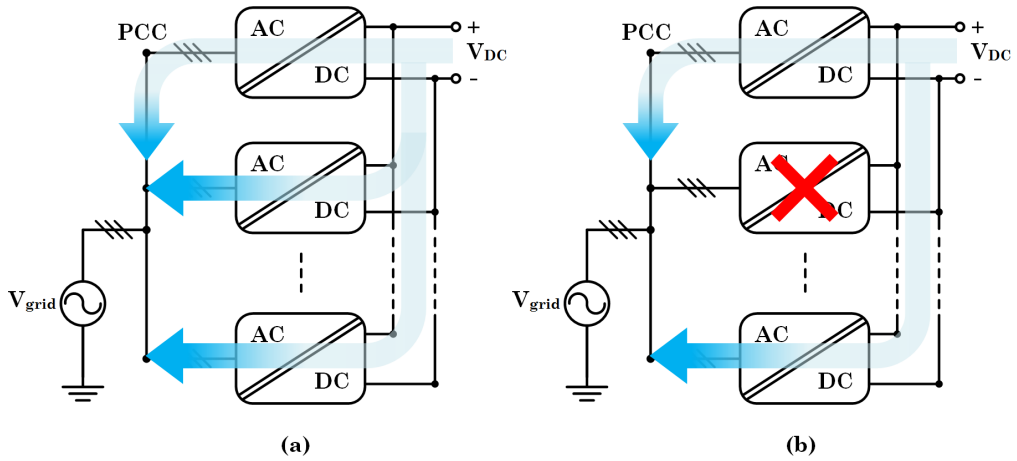


Figure 1.2. Illustration of the power flow in modular parallel converters, (a) under normal operation; (b) with fault in one converter module.

interleaving angle is a fixed value. Depending on the topology and modulation strategy of the converter module, the most popular interleaving angle can be either $2\pi/N$ or π/N with N being the number of converter modules. It should be noted that both modes require the communication channel among the converters to maintain the phase-difference (0 or the interleaving angle) between the carriers of each pair of converters. This communication channel can be established with the communication standard like RS485 or CAN bus [53].

An example of interleaving operation can be found in **Fig. 1.3** using two parallel 2L phase-legs. The combined output voltage, v_o can be obtained with (1.1). The carriers of the two leges are phase-shifted by $\pi = 2\pi/2$, and the resultant v_o becomes a 3L one due to the extra zero-state as shown in **Fig. 1.3**. With more phase-legs in parallel, the number of levels in the output voltage can be further increased. Note that the phase-shift angle can also be any other values. However, the symmetrical interleaving case shown in **Fig. 1.3** has been the most commonly adopted one.

$$v_o = \frac{v_{AO} + v_{BO}}{2} \tag{1.1}$$

Besides the output voltage waveform, the interleaving mode can also be understood from the frequency domain. Harmonic cancellation is an important feature of interleaving, which can be observed from **Fig. 1.4** where both

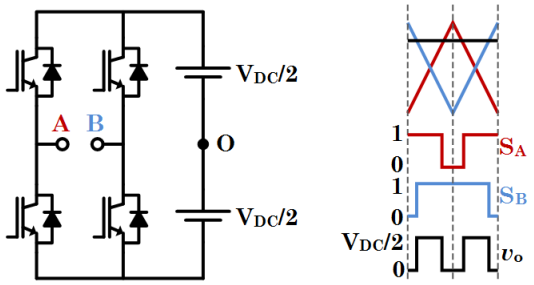


Figure 1.3. Illustration of the interleaving operation and its impact on the output voltage waveform, an example with two parallel 2L phase-legs. S_A and S_B are the PWM pulses for phase-leg A and B respectively.

output voltage waveform and its harmonic spectrum for a given N are shown. The magnitudes of the time domain waveforms and the harmonic spectrums are normalized to the DC link voltage. It can be seen that with higher number of converters, the number of levels in the output voltage waveform can be increased accordingly. Also, the dominant harmonics can be pushed further with higher N. As a result, the quality of the output voltage can be improved. Similarly, other issues like EMI [54], DC link current ripple [55, 56], and CM voltage [57] can also be reduced through interleaving. The harmonic cancellation effect will be further elaborated in the Chapter 2 of this thesis, from the perspective of frequency domain.

As can be seen from **Fig. 1.3**, the voltage difference between leg A and leg B will be translated into ripple current, i.e. circulating current, through the filter inductors. Although many studies have treat the circulating current as an adverse effect, it is merely the ripple in the output current of each converter module, which is similar to the converter side current ripple when using an LCL filter. Also, since there is no capacitive components in the circulating current loop, the circulating current does not induce any EMI or noise issues.

1.3 Challenges of Modular Parallel Converter System

Although modular parallel converters have been widely implemented in practical applications, there are still unaddressed issues limiting the performance

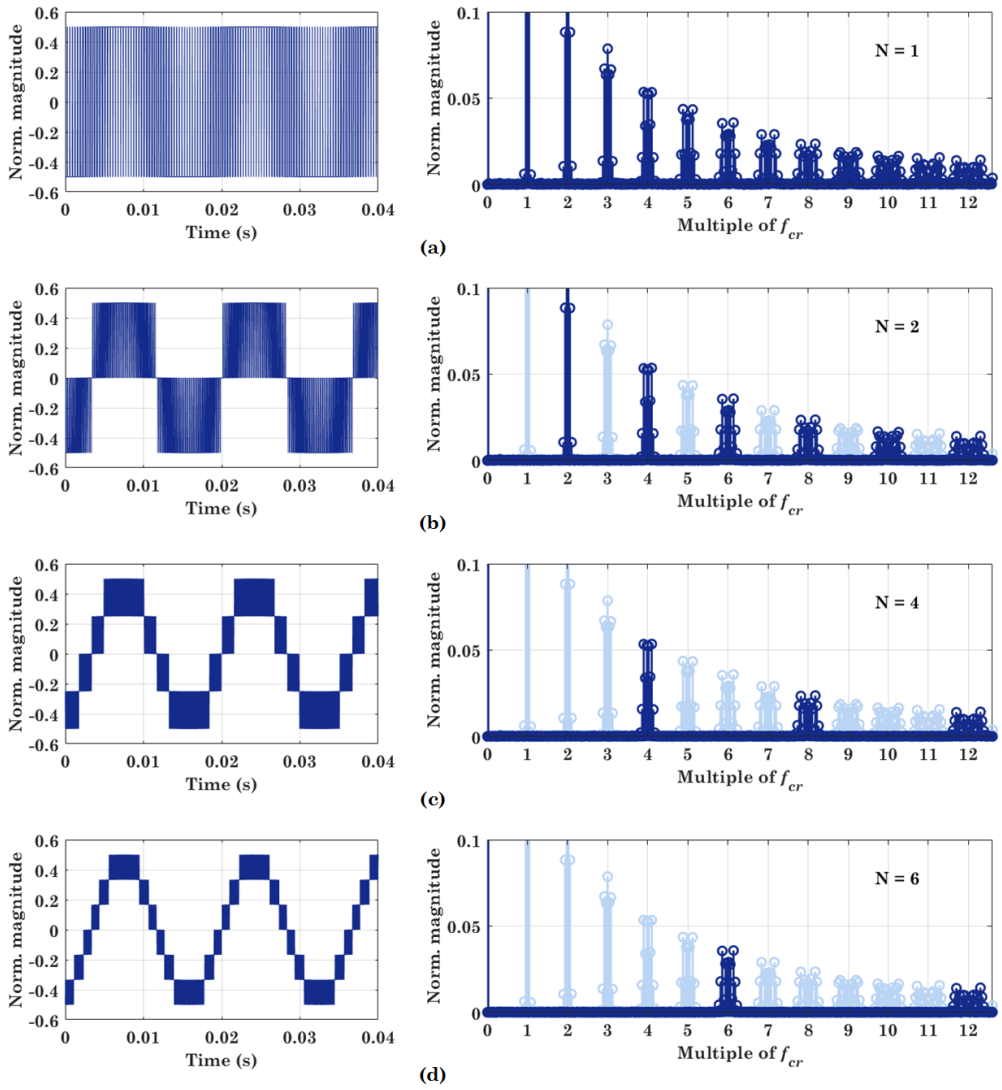


Figure 1.4. Impact of interleaving on the output voltage waveform and spectrum, (a) $N = 1$, (b) $N = 2$, (c) $N = 4$, (d) $N = 6$. The light-colored harmonics are those from a single converter, i.e. $N = 1$. The dark-colored harmonics are those generated with given N. The magnitudes of the waveforms and harmonics are normalized to the DC link voltage.

of the system. Two most important issues are the common mode circulating current (CMCC) and the filter resonance related issues of individual converter module and the system.

1.3.1 Common Mode Circulating Current

The circulating current will be generated with interleaving technique. As can be seen from **Fig. 1.3**, the voltage difference between leg A and leg B will be translated into ripple current, i.e. circulating current, through the filter inductors. Circulating current can be further decomposed into differential mode circulating current (DMCC) and common mode circulating current (CMCC). Essentially, the circulating current is merely the ripple in the output current of each converter module, which is similar to the converter side current ripple when using an LCL filter. However, as CMCC is still in the CM domain, the CM choke in each converter module (see **Fig. 1.1**) must be sized properly to prevent saturation [58].

CMCC is also known as zero-sequence circulating current (ZSCC) in literature. It can be obtained by summing the output currents of an individual converter [59]. The CMCC of the $j$the converter in a system can be obtained with (1.2). The CMCC of other converters in the same system will have the same amplitude, but different phase angle. For a balanced three-phase system, the sum of the CMCCs of all converters will be 0, as given in (1.3).

$$i_{CMCC,j} = i_{A,j} + i_{B,j} + i_{C,j} \tag{1.2}$$

$$\sum_{j=1}^{N} i_{CMCC,j} = 0 \tag{1.3}$$

It should be noted that the CMCC is not the CM leakage current of a converter system. When the converters are interleaved, large high frequency CMCC[1] will be generated by the instant CM voltage differences among the converters. CMCC will be kept within the converter system and will not flow into the grid side or DC side stray capacitances. On the other hand, the CM leakage current is the result of the total CM voltage of the converter system,

[1]Low frequency CMCC will also present in practical applications due to the control and hardware parameter mismatches among the converters [60]. However, it can be easily eliminated with a closed-loop controller in the zero-sequence, and will not be a challenging issue. In the rest of this thesis, the term $CMCC$ only stands for the high frequency CMCC unless otherwise stated.

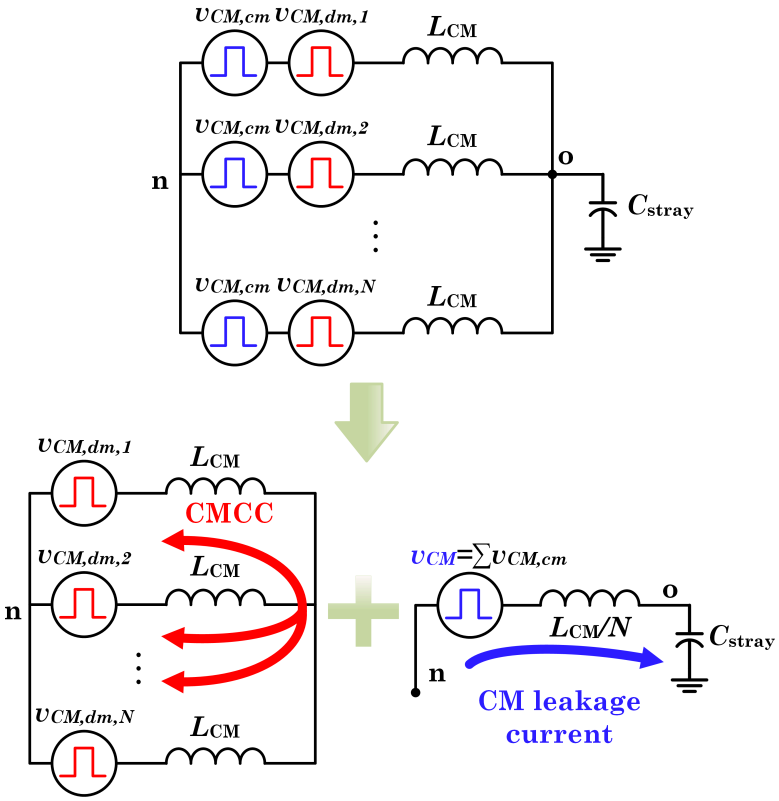


Figure 1.5. Decomposition of the CM loop of interleaved converters.

which in the case of interleaved converters is the common component of the CM voltages of the converters. This effect can be illustrated with **Fig. 1.5**, where $v_{CM,cm}$ is the common component of the CM voltages of the converters, $v_{CM,dm,x}$ (x is the converter sequential number) is the differential component in the CM voltage of the converters, and C_{stray} is the stray capacitance.

In a normal power electronics system, the CM choke can take up to 25% of the system volume [61]. With CMCC, the size of the CM choke can be even larger. A size analysis of the CM choke is presented in Appendix A, suggesting that the reduction of the CMCC can lead to significant reduction of the CM choke size. Considering the increasing high power density requirement in modern power electronics, it is desirable to suppress the maximum value of CMCC by modifying the modulation schemes[2], since the dominant frequency

[2]If CM choke is not adopted in each converter module, active reduction of CMCC is unnecessary since the CM impedance is provided by the single-phase inductors and the CMCC is only a part of the converter side current ripple.

of the CMCC is beyond the bandwidth of the controller.

In literature, many CMCC reduction methods have been reported [59, 60, 62–64], focusing on the 2L VSCs. The performance of the existing methods, given the same CM inductance and system parameters, can be generally illustrated in **Fig. 1.6**, in terms of the CMCC peak value as a function of modulation index. Note that maximum modulation index is 1.15 in the figure as common mode offset (CMO) injection or space vector modulation (SVM) is assumed. Among these methods, the space vector PWM (SVPWM) and the discontinuous PWM (DPWM) are the two conventional methods [59]. With SVPWM the maximum CMCC occurs when modulation index is 0. The maximum CMCC with DPWM is lower than that with SVPWM, but it occurs in the mid modulation index range. Although a grid-interfaced converter typically operates at high modulation index range (≥ 0.9) to efficiently use the DC link, operating modulation index can be low in the occasion grid fault and low-voltage ride through (LVRT) operation. If the CM choke is only sized at high modulation index range, saturation will occur in the LVRT condition, and system failure will be inevitable. As a consequence, the CM choke have to be over-designed at the design points 1 and 2 with the conventional methods. It is worth noting that it is suggested in [45] that using CM choke with interleaved SVPWM can help reduce the size of the converter side inductor in an LCL filter. However, this is in fact misleading as the contribution of CMCC to the output current ripple of each converter is negligible in the nominal operation range of a grid-tied system. As a result, reducing the converter side inductor will in fact increase the output current ripple of each converter, leading to increased conduction loss.

To reduce the maximum CMCC value and shift the CM choke design point to higher modulation index range (optimally the maximum modulation index point i.e. 1.15), two methods have been proposed in literature. A modified DPWM (MDPWM) is proposed in [63], and capable of shifting the design point to the optimal one, as shown in **Fig. 1.6**. However, this method is specially designed for system with two converters and relies on coordinated control of the two converters to reduce CMCC. As such, it is not available for system with

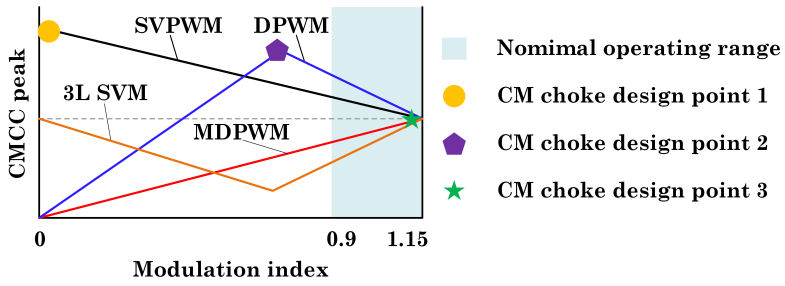


Figure 1.6. CMCC peak value as a function of modulation index in different methods provided the same CM inductance and system parameters.

more than two converters and cannot be extended to a modular architecture where coordinated control is difficult to realize. Also, it has lower efficiency than the conventional methods as it introduces multiple switching actions within one switching period, and thus the switching loss will be significantly increased. On the other hand, by treating the parallel converters as one single multilevel converter, optimal modulation scheme can be derived through the space vector diagram. In this regard, a 3L SVM scheme is proposed in [59] for the system with two parallel converters. The CM choke can be designed at the optimal point and the maximum CMCC value is the same as that with the MDPWM. But the efficiency of the 3L SVM is much higher than that of MDPWM. Although the 3L SVM can be extended to higher-level for system with more parallel converters, the design procedure will become more complicated.

Besides 2L converter, parallel multilevel converters are gaining popularity in practical applications such as solar inverter and medium voltage drives. Based on the illustration in **Fig. 1.5**, if the CM voltage of each converter module can be eliminated to zero, the CMCC will also be eliminated. Therefore, the zero CM voltage (ZCMV) modulation technique can be applied to eliminate CMCC. However, due to the shortened modulation index range, the ZCMV modulation strategies are not practical for real applications. As of today, a practical solution for reducing CMCC in interleaved multilevel converters has not been discussed yet. Only a CMCC reduction method proposed for two interleaved 3L converters has been reported [64], whereas the perfor-

mance of this method for an arbitrary number of converters is still unknown. Also, possibility of further CMCC reduction has not been investigated.

In summary, for either 2L VSC or multilevel VSC, there is no CMCC suppression method available for system with an arbitrary number of converters. The cause of this research gap is the lack of a unified analyzing approach for modular system with any number or type of converters. Existing studies all adopt time-domain based analyzing approach which will become significantly more complicated when more converters and/or multilevel converters are considered.

1.3.2 Negative Impact of Filter Resonance

Due to the increasing penetration of renewable energy resources in utility grid and the rapid development of grid interfaced infrastructures like charging station and hybrid AC/DC micro-grid, the power grids have experienced increasing utilization of grid-tied VSCs, of which most are LCL-filtered. It is well known that the filer resonance of the LCL filter can induce issues such as instability and poor power quality. These filter resonance related issues will become more severe, when multiple LCL-filtered VSCs are put in parallel [65].

First of all, the control of each individual converter must face the challenge of multiple resonant frequencies [65, 66]. The stability of one converter will be affected by the operation status of the other converters. For example, a step change in the output power of one converter will induce resonances in the output currents of the other converters. With the knowledge of the number of converters, active damping can be applied to mitigate the multi-resonance issue. However, as the resonant frequency is related to the number of converters, the damping controller may be ineffective since the actual number of the active converters can vary depending on the operation condition. Secondly, the system level stability will also be undermined due to the interactions of the parallel converters [67, 68]. This issue requires further damping to address. Finally, recent studies suggest that interleaving the LCL-filtered converters could induce instability of certain sideband harmonics in the output current of each individual converter, whereas these harmonics are eliminated if

the parallel converters are synchronized [69]. Thus far, a dedicated mitigating method for this issue is not available yet, and operating the parallel converters in synchronous mode is recommended [69].

With large amount of VSCs connected to the power grid in the near future, and especially considering that in most applications the VSCs are connected in parallel with either modular structure (see **Fig. 1.1**) or with separate DC links (see Appendix C), the best design will be completely eliminate the filter resonance by using L filter. However, the practical implementation of L filter is prohibited by its large size and high cost. Therefore, it is necessary to rethink the system level design to eliminate the filter resonance without increasing size and cost of the filter.

1.4 Thesis Contributions and Outline

The main objective of this thesis is to address the key issues associated with modular parallel converters, as above introduced. Both 2L VSC and multilevel VSC based systems are considered in the study. A new interleaving PWM scheme is proposed to reduce CMCC in system with any number or type of converters. A system level design using only L filter is presented to eliminate the filter resonance. Finally, a new type of multilevel converter topology, the internal parallel converter (IPC), is proposed, offering a new approach to implement parallel modularity with multilevel converters. The main contributions and outline of the thesis are summarized as follows:

- To facilitate the investigation of modular converter system, a harmonic distribution analysis is presented in this thesis. Different from the existing studies in time domain, the frequency domain analysis in this thesis can be easily applied to study the system with any number and type of converters. Based on the harmonic distribution analysis approach, the modulation strategies can also be evaluated easily from all aspects, e.g. output quality, circulating current, and common mode voltage, which can significantly simplify the investigation of multilevel converters. The details regarding the analysis is presented in Chapter 2 of this thesis.

- Based on the findings in the harmonic distribution analysis, a 2-degree-of-freedom (2DoF) interleaving technique is proposed for reducing the CMCC peak value in modular parallel converters with an arbitrary number of either 2L or multilevel VSCs. The technique can substantially reduce the maximum value of CMCC regardless the number of converters. Compared to the existing approaches, the CM choke design point can be successfully shifted to the 'point 3' in **Fig. 1.6** for 2L converters. For interleaved multi-level converters, the phase disposition (PD) based 2DoF scheme also produces the lowest CMCC as compared to other methods. Moreover, the overall performance of the 2DoF scheme is comparable to or even better than the existing methods. In Chapter 3, the 2DoF interleaved scheme is comprehensively evaluated for 2L converters. The implementation of 2DoF scheme in 3L and higher-level converters will be evaluated and discussed in Chapter 4.

- Rather than continuously exploring the LCL filter related issues from the control point of view, this thesis takes advantage of the interleaving technique to replace the LCL filter with small size L filter and thereby completely eliminating filter resonance and its associated problems. An L filter based design concept for the modular parallel converter system is proposed. An investigation of the system design reveals that by interleaving a certain number of converters, only L filter with small size will be sufficient to satisfy the grid code. More importantly, the total size of the L filters in the proposed design can be significantly smaller than the conventional LCL filter. The detailed analysis and benchmark based comparative results are elaborated in Chapter 5.

- To integrate parallel modularity into multilevel converters, a new multilevel converter topology synthesizing concept, the internal parallel converter (IPC), is proposed. The new topologies derived from this concept feature several merits including modularity, fault tolerant capability, better utilization of power semiconductor devices, and simple control and modulation. The new topologies also provide an alternative solution for

redundant multilevel converter system. Owing to above merits, the IPC topologies are competitive candidates for a wide range of applications, from low voltage ones such as solar string inverter and electric vehicle drives to medium voltage motor and wind turbine drives. The features of the new topologies will be introduced in Chapter 6. The design and lab-scale test of a high density prototype using one embodiment of the new topologies are presented in Chapter 7.

Chapter 2

PWM Harmonic Distribution Analysis

As introduced in Chapter 1, time-domain based analysis is inefficient in analyzing modular parallel converter system with an arbitrary number of converters, especially when multilevel converters are considered. To provide a tool for studying modular parallel converters, a frequency-domain based harmonic distribution analysis is presented in this Chapter. The analysis takes advantage of the double Fourier integral (DFI) theory, which has been widely applied for analyzing and designing various PWM strategies for single converters, owing to the merit that the DFI analysis is not subject to specific switching frequency or fundamental frequency. In this chapter, harmonic distribution terms, which are universal for two-level (2L) and multilevel converters, are derived based on DFI considering an arbitrary number of interleaved converters. In addition, the generalized PWM scheme, which is difficult to analyze in time-domain, is considered in the analysis, revealing an additional degree-of-freedom for designing PWM strategies for interleaved converters. As such, a two degrees-of-freedom (2DoF) interleaving scheme is identified in this chapter. The 2DoF interleaving scheme has the potential to improve the overall performance of the interleaved converters as compared to the conventional approaches. To simplify the analysis, 2L VSC is adopted, and simulation results are presented to verify the analysis. The analysis in this chapter will serve as a theoretical foundation for the CMCC suppression methods in the following Chapter 3 and Chapter 4.

2.1 Double Fourier Integral

The DFI theory is firstly introduced in [70]. Distinguished from the basic Fourier analysis, DFI is irrelevant to specific system parameters such as the switching frequency and the fundamental frequency. As such, the analysis can be significantly simplified. With DFI, the order of a harmonic can be simply represented by two parameters in the form like (m, n), where m is the integer index of carrier frequency, f_{cr} or ω_c, and n is the integer index of fundamental frequency, f_1 or ω_1. With the aid of DFI, the order of carrier frequency (i.e. f_{cr}) harmonic can be written as (1, 0), and the order of harmonic at the frequency $(2f_{cr} - 5f_1)$ can be written as (2, -5).

DFI offers closed-form analytical solutions for calculation of the amplitude of harmonic (m, n), i.e. A_{mn}. The calculation can be carried out with (2.1), where $f(x, y)$ is the modulating reference signal function defined in contour plane, K is the number of segments that the modulating waveform can be decomposed into. Depending on the specific modulation strategy, the form of $f(x, y)$ and the value of K can be different. As $f(x, y)$ is only determined by the modulating signal waveform and carrier configuration in one phase, the calculated A_{mn} will be universal for all phases in a multiphase system.

$$A_{mn} = Re\left[\frac{1}{2\pi^2}\sum_{i=1}^{K}\int_{y}^{y}\int_{x}^{x} f\left(x, y\right) e^{j(mx+ny)} dxdy\right] \quad x = \omega_c t \quad y = \omega_1 t \quad (2.1)$$

The analytical expression of A_{mn} can be different depending on the values of m and/or n and on the type of studied converter. For the 2L SPWM (see **Fig. 2.1**), A_{mn} can be directly calculated with (2.2), where V_{DC} is the DC link voltage, M is the modulation index, and J_n is the Bessel function of the first kind [71]. The solutions for common mode offset (CMO) injected PWM and multilevel PWM are more complicated. The detailed derivations of solutions for different converter and PWM approaches are out of the scope of this thesis and can be found in [72]. But the harmonic distribution analysis that will be introduced in the rest of this chapter is irrelevant to the specific amplitude of a harmonic. As such, the 2L SPWM will be used as an example for simplicity.

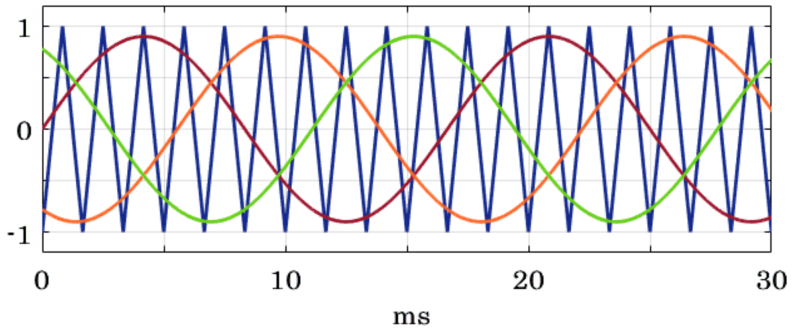


Figure 2.1. The SPWM scheme for single 2L VSC.

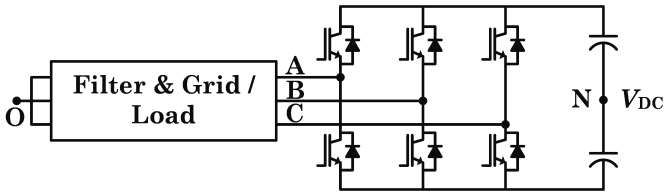


Figure 2.2. Schematic of a three-phase VSC.

$$A_{mn}(m,n) = \frac{2V_{DC}}{m\pi} J_n\left(m\frac{\pi}{2}M\right)\sin\left((m+n)\frac{\pi}{2}\right) \tag{2.2}$$

2.2 Harmonic Distribution in Single VSC

In this section, the harmonic distribution analysis in a single three-phase VSC is analyzed with the aid of DFI theory. The 2L VSC, shown in **Fig. 2.2**, is adopted as an example. The analysis will help to understand how output voltage quality and common mode (CM) voltage are related.

According to the basic principle of the modulation process, the harmonic spectrum of the phase voltage (v_{AN}) of an individual phase-leg contains the entire harmonic information. For a three-phase converter, the relationship expressed in (2.3) holds true. As such, the harmonics generated from each phase-leg are then distributed into two different domains, i.e. differential mode (DM) and common mode (CM), which correspond to the output phase voltage (e.g. v_{AO}) and the CM voltage (e.g. v_{ON}) for a single converter. The CM voltage can be calculated with (2.4). Then two phase voltages produce the line-to-line voltage v_{LL} (e.g. v_{AB}).

$$v_{AN} = v_{AO} + v_{ON} \tag{2.3}$$

$$v_{ON} = \frac{v_{AN} + v_{BN} + v_{CN}}{3} \tag{2.4}$$

Taking SPWM as an example, the simulated waveforms of v_{AN}, v_{AO}, and CM voltage, and their harmonic spectra are shown in **Fig. 2.3**. One can see that the harmonics originated from v_{AN} are all distributed into v_{AO} and v_{ON}, with the same amplitude. To be specific, harmonics (1, 0), (2, -3), and (2, 3) go to the CM domain, whereas harmonics (1, -2), (1, 2), and the other four harmonics with $m = 2$ are placed in DM domain. The harmonics in the line-to-line voltage v_{AB} has the same order of harmonics as those in v_{AO}, but the amplitudes are higher. The reason of such distribution can be explained with formulas (2.5) to (2.9), where ω_1 and ω_c are the angular fundamental frequency and angular carrier frequency respectively, θ_1 and θ_c are the initial angle of the fundamental reference and carrier signals. The output voltage of three phase-legs (e.g. v_{AN}) can be generally expressed with (2.5). Depending on the phase angle of the reference waveforms, θ_1 can be 0, $-2\pi/3$, or $2\pi/3$. For SPWM, all three phases adopt the same carrier signal. As such, the initial angle of carrier signal θ_c can be assumed as 0 for all three phases. In (2.5), the first term on the right side represents the fundamental component, whereas the second term represents the sum of the harmonics around multiples of carrier frequency. The amplitude of harmonic (m, n) is still determined by (2.2). Based on (2.4) and (2.5), the CM voltage, i.e. v_{ON}, can be expressed as (2.6). As the fundamental components are canceled out, only high frequency harmonics remain in the spectrum of CM voltage. Likewise, the line voltage (e.g. v_{AB}) can be derived as (2.7). Based on (2.6) and (2.7), the amplitude of high frequency harmonics can be extracted as written in (2.8) and (2.9) for CM voltage and v_{LL} respectively. Note that the subscripts of (2.8) and (2.9) are changed to 'CM' and 'LL' to indicate CM voltage and v_{LL}, as these harmonics are common in all three-phases. Also, only the absolute amplitude of each harmonic is of interest.

$$\begin{aligned} v_{AN} =& \frac{V_{DC}}{2} M \cos\left(\omega_1 t + \theta_1\right) \\ &+ \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} A_{mn} \cos\left[m\omega_c t + n\omega_1 t + m\theta_c + n\theta_1\right] \end{aligned} \tag{2.5}$$

$$v_{ON} = \frac{1}{3} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} A_{mn} \cos\left(m\omega_c t + n\omega_1 t\right) \times \left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right] \tag{2.6}$$

$$\begin{aligned} v_{AB} =& \frac{\sqrt{3}}{2} V_{DC} M \cos\left(\omega_1 t + \frac{\pi}{6}\right) \\ &+ 2 \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} A_{mn} \cos\left[m\omega_c t + n\omega_1 t - \frac{n}{3}\pi + \frac{\pi}{2}\right] \times \sin\left(\frac{n}{3}\pi\right) \end{aligned} \tag{2.7}$$

$$v_{CM}\left(m, n\right) = abs\left\{\frac{1}{3} A_{mn}\left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right]\right\} \tag{2.8}$$

$$v_{LL}\left(m, n\right) = abs\left[2A_{mn} \sin\left(\frac{n}{3}\pi\right)\right] \tag{2.9}$$

From (2.8) and (2.9), one can see that the distribution of harmonics is determined by the number of n. The amplitude of each harmonic in the CM voltage is either A_{mn} or 0, whereas the amplitude is increased in the v_{LL}, as compared in the phase voltage. Substituting different values of n into (2.8) and (2.9), the harmonic distribution pattern as shown in **Fig. 2.3** can be obtained.

SPWM is the most commonly used PWM scheme. However, it is just one special case where the three phase modulating waveforms share the same carrier signal. A more generalized PWM scheme, shown in **Fig. 2.4**, involves a phase shift angle of the carriers, i.e. θ_{ps}. For a three-phase converter, the phase-shift angle means that there will be three carriers, each of them is assigned to one phase. For each one of the three phases, the modulation strategy is the same as that in SPWM, which means that the resultant phase voltage harmonics are the same as in SPWM. Therefore, (2.2) is still valid for calculating the amplitude of source harmonics. However, the CM voltage and v_{LL} are both the results of three-phase operation, and their harmonics can be

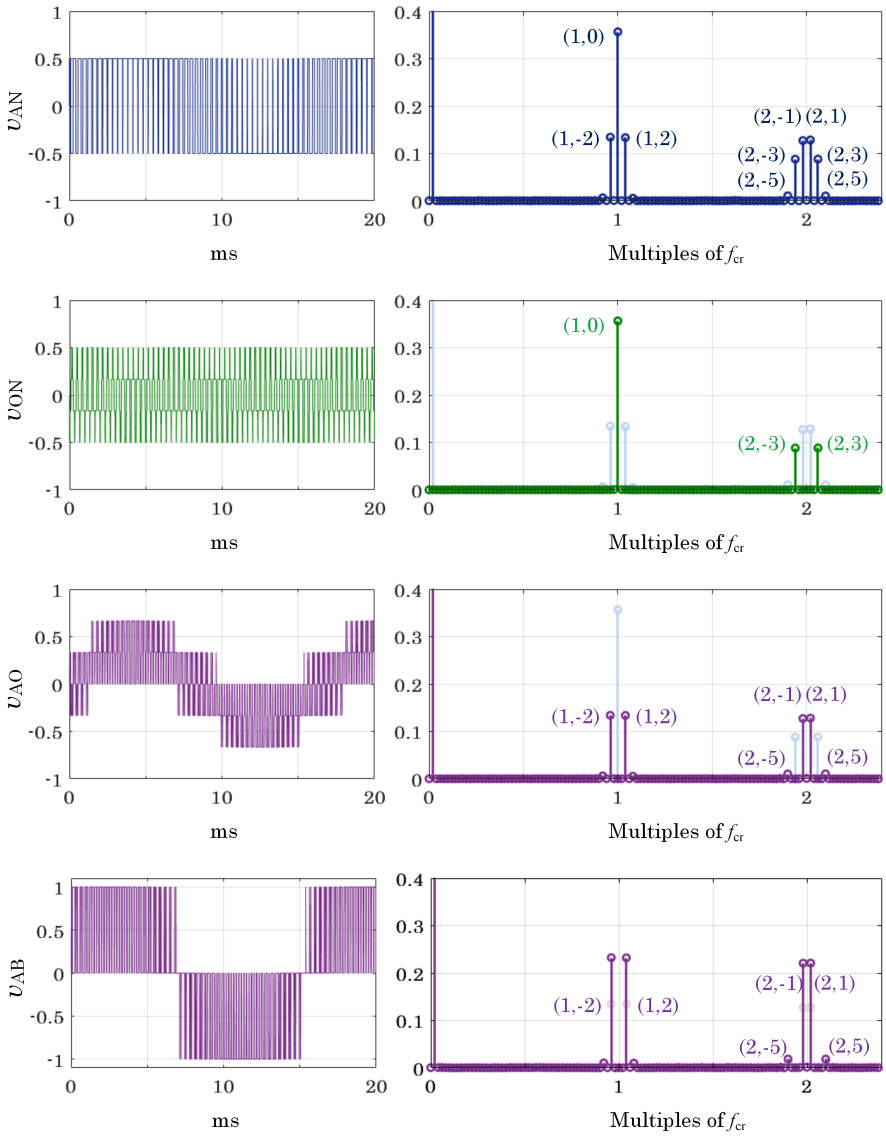


Figure 2.3. Harmonic distribution in a three-phase 2L VSC. The amplitudes are normalized to V_{DC}. The harmonics of v_{AN} are shown in light color as the background of the spectral of v_{AO} and CM voltage. Modulation index in the simulation is 0.9.

altered by changing θ_{ps}. Compared to conventional SPWM, the generalized PWM scheme offers an extra degree-of-freedom, i.e. θ_{ps}, to design or operate a converter. Considering sinusoidal references, the resultant harmonics in CM voltage and v_{LL} are expressed in (2.10) and (2.11), considering two harmonic distribution terms. After some mathematical derivation, the distribution terms can be obtained as in (2.12) and (2.13).

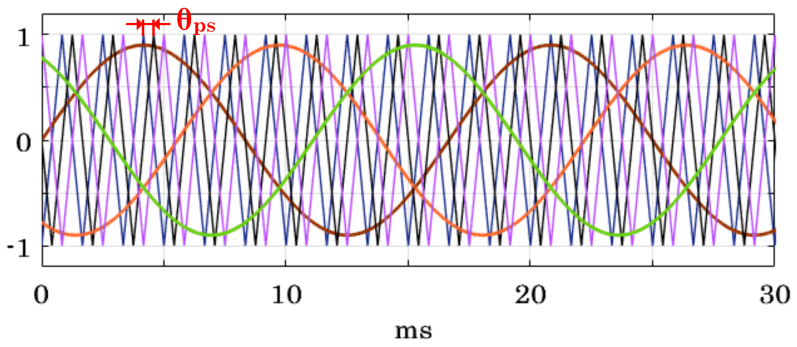


Figure 2.4. The generalized SPWM scheme with phase shift angle θ_{ps} between carriers.

$$v_{CM}\left(m,n\right)=abs\left[A_{mn}\cdot D_{mn,CM}\right] \tag{2.10}$$

$$v_{LL}\left(m,n\right)=abs\left[A_{mn}\cdot D_{mn,LL}\right] \tag{2.11}$$

$$D_{mn,CM}=\frac{1}{3}\left[1+2\cos\left(m\theta_{ps}+\frac{2}{3}\pi n\right)\right] \tag{2.12}$$

$$D_{mn,LL}=2\sin\left(\frac{m\theta_{ps}+2\pi n/3}{2}\right) \tag{2.13}$$

By sweeping θ_{ps} from $-\pi$ to π, the amplitudes of distribution term for harmonic (1,0) in CM voltage and v_{LL} are compared in **Fig. 2.5**. One can see that it is possible that harmonic (1,0) appears in both CM voltage and v_{LL}, which may increase the filtering requirements for both since harmonic (1,0) has much higher magnitude than other harmonics.

The simulated harmonic spectral of CM voltage (v_{ON}) and v_{LL} (v_{AB}) when θ_{ps} is $\pi/2$ are shown in **Fig. 2.6**, where one can see that v_{ON} and v_{AB} share the same order of harmonics, but the amplitudes are different. Taking harmonic (1, 0) as an example, its amplitude is 0.1187 in v_{ON} and is 0.5037 in v_{AB}. Based on DFI, the source harmonic amplitude A_{10} can be calculated, which equals to 0.3564. Based on (2.12), the distribution term for CM voltage is 0.3333, and the calculated amplitude is 0.3564*0.3333 = 0.1188, which is very

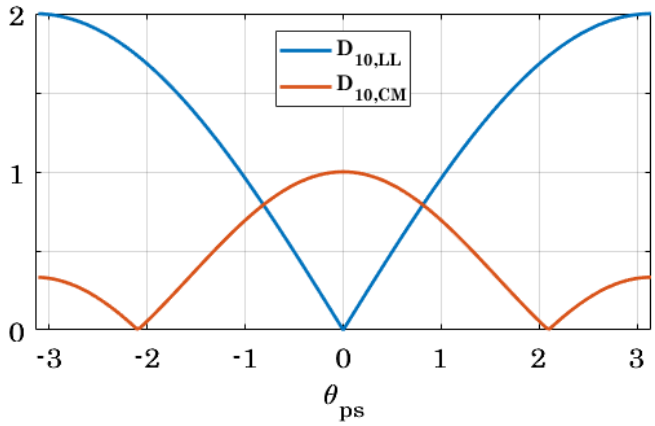


Figure 2.5. Amplitude of the distribution terms for harmonic (1, 0).

close to the simulation result. Likewise, the calculation result based on (2.11) for CM voltage also complies well with the simulation result.

It is worth noting that one special case where $\theta_{ps} = 2\pi/3$ is particularly interesting. In this case, all harmonics can be fully shifted, meaning that a harmonic will be either in v_{LL} or in CM voltage. As the switching frequency harmonic (1, 0), which has much higher amplitude than other harmonics, can be transferred from CM voltage to v_{LL}, this scheme has been proposed in literature to mitigate the CM voltage issue in single 2L VSC [73]. For single multilevel converters, similar technique can also be applied [74]. However, due to the significantly increased harmonic energy in v_{LL}, the output current with this method will contain large ripple. As such, LCL filter with larger attenuation rate and size will be required in order to meet the grid code. For single converter, as the CM current or noises can be easily attenuated with a CM filter due to the capacitance in the CM loop, the increase of the size of the LCL filter will significantly undermines the power density of the converter [75]. Therefore, PWM strategies with non-zero θ_{ps} is in fact not recommended for single converter.

2.3 Harmonic Distribution with Interleaving

An example structure showing N paralleled 2L VSCs is illustrated in **Fig. 2.7**, where only L filter is used for simplification. With interleaving, one

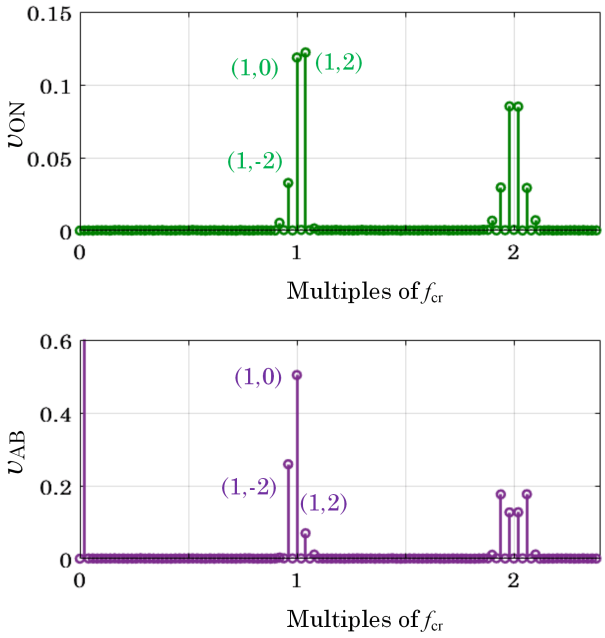


Figure 2.6. Harmonic distribution when θ_{ps} is $\pi/2$. The amplitudes are normalized to the DC link voltage.

more degree-of-freedom for harmonic distribution can be obtained, i.e. the interleaving angles θ_{int}. Therefore, with the generalized PWM scheme, there are in total two degrees-of-freedom available to design and operate interleaved converters. With an non-zero θ_{int}, certain harmonics will be distributed into circulating current. The distribution due to interleaving can be generalized by assuming an arbitrary number of converters. The generalized interleaving principle can be illustrated in **Fig. 2.8**, where harmonics with the same m and n and amplitude have different phase angles in different converters. The angle is determined by both m and the interleaving angle θ_{int} since it is the carriers that are phase shifted. Therefore, interleaving affects the distribution of a group of harmonics with the same m. Based on **Fig. 2.8**, the common harmonics that are not cancelled with interleaving, i.e. v_{LL} and CM voltage, are determined by the term T_{com} as given in (2.14); whereas the harmonics that distributed into circulating current are determined by T_{cc} given in (2.15). With symmetrical interleaving where $\theta_{int} = 2\pi/N$, T_{com} is 1 when m = multiples of N, otherwise T_{com} is 0; while T_{cc} is 0 when m = multiples of N and is 0 in other conditions.

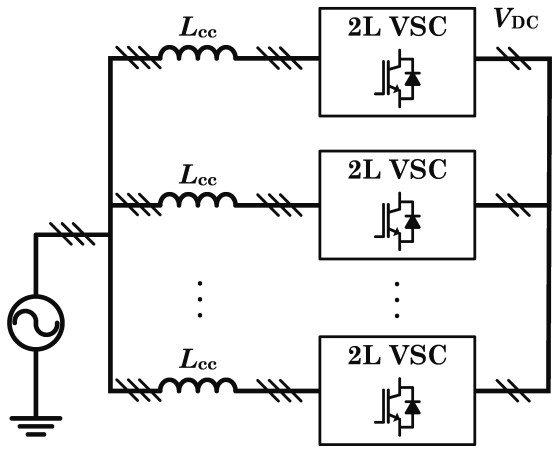


Figure 2.7. An example structure with N paralleled 2L VSCs, each VSC is equipped with an L filter, i.e. L_{cc}.

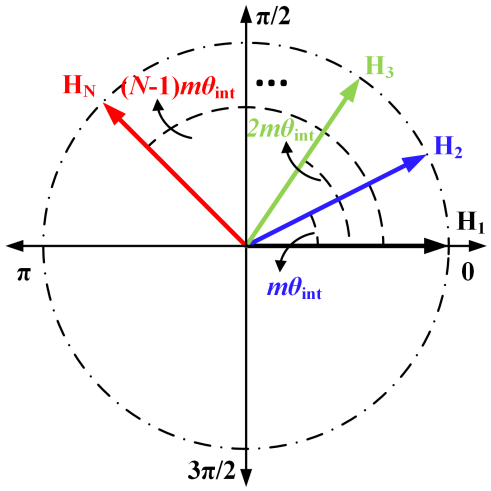


Figure 2.8. Illustration of generalized interleaving scheme.

$$T_{com} = \frac{1}{N}\sum_{k=1}^{N} e^{jm(k-1)\theta_{\text{int}}} \tag{2.14}$$

$$T_{cc} = 1 - \frac{1}{N}\sum_{k=1}^{N} e^{jm(k-1)\theta_{\text{int}}} \tag{2.15}$$

As introduced in Chapter 1, the circulating current can be decomposed into DMCC and CMCC. For practical filter designs, the harmonic content of CMCC is typically of great interest [60]. The circuit loop for CMCC can be illustrated as **Fig. 2.9** for simplicity. Note that the inductance of L_{CM} can be provided by $L_{cc}/3$ or a separate CM choke. As the CMCC is driven by

the differences among the CM voltage of the converters, the CMCC in the j^{th} converter can be expressed with (2.16). In (2.16), Z_{CM} denotes the CM impedance of each converter.

$$i_{CMCC,j} = \frac{(N-1)\, v_{CM,j} - \sum_{k=1,k\neq j}^{N} v_{CM,k}}{N Z_{CM}} \tag{2.16}$$

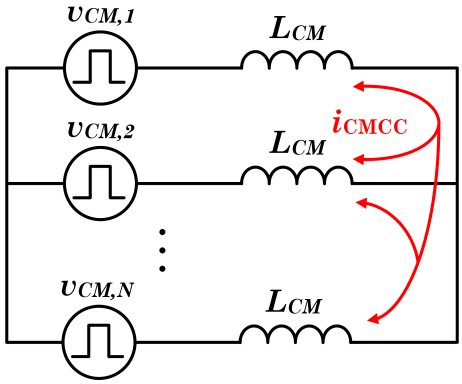


Figure 2.9. Illustration of the CMCC loop in modular parallel converters.

Based on above analysis, the harmonic distribution of interleaved 2L converters can be expressed in (2.17) to (2.19). Based on (2.19), one can find that the distribution of CMCC follows the same distribution term in (2.12).

$$v_{LL}\,(m,n) = abs\,[A_{mn} \cdot D_{mn,LL} \cdot T_{com}] \tag{2.17}$$

$$v_{CM}\,(m,n) = abs\,[A_{mn} \cdot D_{mn,CM} \cdot T_{com}] \tag{2.18}$$

$$i_{CMCC}\,(m,n) = abs\left[\frac{A_{mn} \cdot T_{cc} \cdot D_{mn,CM}}{(m\omega_c + n\omega_1)\, L_{CM}}\right] \tag{2.19}$$

Assuming two converters are interleaved. One can simplify (2.14) and (2.15) to (2.20) and (2.21). The values of (2.20) and (2.21) can be calculated by sweeping θ_{int} from $-\pi$ to π. The results with $m = 1$ and $m = 2$ are shown in **Fig. 2.10 (a)** and **(b)**, respectively. One can see that it is possible that a group of harmonics appears in both V_{LL} or CM voltage and circulating current, resulting in incomplete harmonic cancellation.

Table 2.1. System specs in simulation

Parameter	Value
DC link voltage, V_{DC}	600V
Carrier frequency, f_{cr}	3000Hz
Fundamental frequency, f_1	60Hz
Current sharing inductance, L_{cc}	5mH

$$T_{com,N=2} = \cos\left(\frac{m\theta_{\text{int}}}{2}\right) \tag{2.20}$$

$$T_{cc,N=2} = \sin\left(\frac{m\theta_{\text{int}}}{2}\right) \tag{2.21}$$

Further considering the distribution term in generalized scheme as shown in **Fig. 2.4**, it is possible that a harmonic will appear in every aspect of interleaved converters. For example, with $\theta_{ps} = \pi/3$ and $\theta_{int} = \pi/2$, the simulated spectra of V_{LL}, CM voltage, circulating current, and CMCC are shown in **Fig. 2.11**. Simulation parameters are listed in **Table 2.1**. Seen from **Fig. 2.11**, both V_{LL} and CM voltage have harmonic (1,0). Also, 1/3 of the amplitude of harmonic current (1,0) in CMCC is less than the amplitude in the entire circulating current, indicating that a portion of harmonic (1,0) is also distributed into DMCC.

Above frequency domain analysis also indicates that harmonics cannot be cancelled and the total injected harmonic energy is the same for any θ_{ps} and θ_{int} since it is determined by A_{mn}, i.e. the modulation technique and reference signal per phase. With different θ_{ps} and θ_{int}, the harmonics are distributed to different part of the system. If an entity, e.g. V_{LL}, has less harmonic energy, it will have better quality. However, the quality of other entities will be undermined since they will share greater portion of the total input harmonic energy. Therefore, performance trade-offs can be obtained by properly distribute harmonics based on the specific design and filtering requirements. For example, the study in [54] has suggested that $\theta_{int} = 22^\circ$ leads to the smallest EMI filter size for system requiring DC side filter, whereas symmetrical interleaving is favorable if the filter is at AC side. In most studies

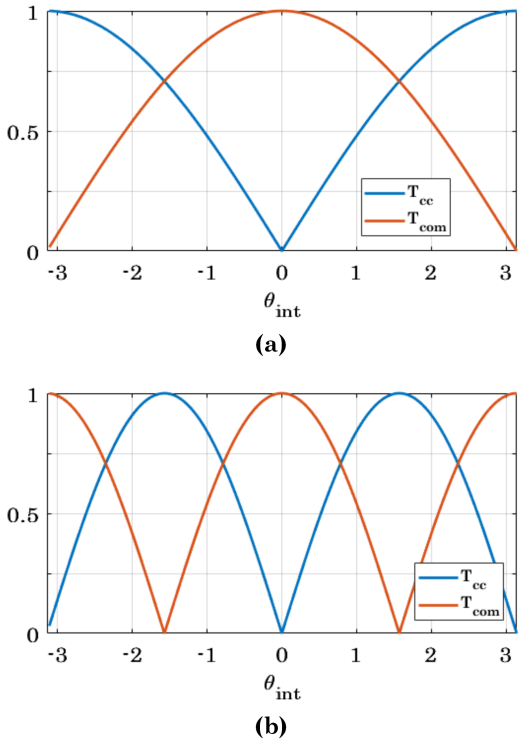


Figure 2.10. Amplitude of T_{cc} and T_{com} with different θ_{int}, (a) $m = 1$, (b) $m = 2$.

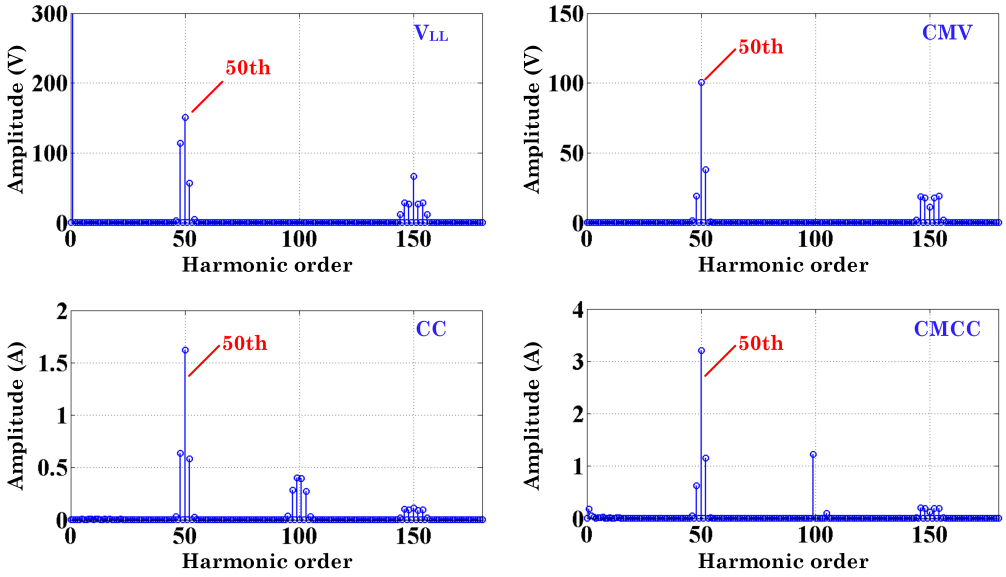


Figure 2.11. Simulated spectra with $\theta_{ps} = \pi/3$ and $\theta_{int} = \pi/2$.

and applications, symmetrical interleaving, i.e. $\theta_{int} = 2\pi/N$, has been the most popular choice due to its simple implementation and complete harmonic cancellation performance.

2.4 Summary

In this chapter, a harmonic distribution analysis is performed for three-phase 2L VSC. The relationship between the line voltage and CM voltage is revealed in frequency domain for single 2L VSC. In addition, interleaving has also been considered. Analysis shows that the distribution of harmonics in different domains can be manipulated by varying the phase-shift angle, i.e. θ_{ps} in each individual converter and the interleaving angle, i.e. θ_{int}, among the parallel converters. The detailed harmonic distribution with certain angles can be calculated with the distribution terms derived in this chapter. As such, the angles can be carefully selected for a given application scenario and purposes. Although 2L VSC is adopted as an example in this chapter, the derived distribution terms are valid for multilevel converters. This chapter serves as a theoretical foundation for the subsequent Chapter 3 and Chapter 4, where two carrier-based PWM schemes are proposed for reducing CMCC in interleaved 2L VSCs and multilevel VSCs, respectively. As the generalized interleaving scheme involves carrier phase-shift within individual converter and among paralleled converters, it is named as two degrees-of-freedom (2DoF) interleaving in the subsequent chapters. As a comparison, the SPWM based interleaving is named as one degree-of-freedom (1DoF) interleaving since only θ_{int} can be adjusted.

Chapter 3

Symmetrical 2DoF Interleaving for Modular Parallel 2L VSCs

As identified in Chapter 2, the 2DoF interleaving scheme provides an extra degree-of-freedom for designing PWM strategy for interleaved converters. This chapter proposes a symmetrical 2DoF (S2DoF) interleaving scheme for modular parallel 2L VSCs. In this scheme, the two phase-shift angles are both determined symmetrically. For a three-phase 2L VSC, θ_{ps} is set as $2\pi/3$. As such, the harmonics in DM and CM domains are completely decoupled. For N parallel 2L VSCs, θ_{int} is set as $2\pi/N$. As a comparison, the conventional SPWM based interleaving scheme is named as symmetrical 1DoF (S1DoF) interleaving, where θ_{ps} is 0 and θ_{int} is $2\pi/N$.

A comprehensive evaluation of the S2DoF interleaving scheme is conducted in this chapter. When compared to S1DoF interleaving, the foremost advantage of the S2DoF interleaving is its CMCC reduction performance. Analysis in this chapter reveals that the S2DoF interleaving can provide CMCC reduction regardless the number of interleaved converters. More importantly, the maximum value of CMCC with S2DoF interleaving always present at the maximum modulation index point. In terms of output quality and CM voltage, the performances of the S2DoF scheme are competitive to that of the S1DoF interleaving. That said, no performance sacrifice is made to reduce CMCC. Because of above merits, the S2DoF interleaving allows interleaving technique to be better implemented in modular parallel 2L VSCs.

3.1 Symmetrical 2DoF-Interleaving Scheme

Considering two converters are interleaved, the carrier configurations and resulted PWM signals of the S2DoF scheme are shown in **Fig. 3.1 (a)**, where S_{xy} (x is 1 or 2; y is A, B or C) denotes the PWM signal for the phase y of converter x. As a comparison, the S1DoF scheme based on SPWM is shown in **Fig. 3.1 (b)**. An example of the implementation of S2DoF scheme in two parallel 2L VSCs is shown in **Fig. 3.2**. The S2DoF schemes can be generalized to N converters by keeping θ_{ps} as $2\pi/3$. With the aid of digital controllers like DSP or FPGA, S2DoF interleaving can be easily implemented in system with an arbitrary number of converters without any complicated programming. In addition, as a carrier-based PWM strategy, it allows simple and flexible implementation of low-frequency CMCC control strategies. Common mode offset (CMO) injection is also available for increasing DC voltage utilization ratio.

In the following sections, the S2DoF scheme is comprehensively evaluated. The system parameters in **Table 3.1** are used in the analysis and simulation, which was conducted with Simulink. The system structure adopted in analysis and simulation can be found in **Fig. 2.7**. Experimental verifications have been conducted with two interleaved converters. The parameters of the experimental setup are also listed in **Table 3.1**. The S2DoF interleaving scheme was implemented in DSP TMS320F28335. Note that resistive load is used to better visualize the output current ripple with different methods. This will not affect the evaluation of CMCC peak value since the load is outside of the CMCC loop.

Table 3.1. System parameters for analysis and verifications.

Parameter	Simulation	Experiment
DC link voltage, V_{DC}	600V	120V
Carrier frequency, f_{cr}	3000Hz	3000Hz
Fundamental frequency, f_1	60Hz	60Hz
Current sharing inductance, L_{cc}	7mH	5mH
Load resistance,R_L	10Ω	29Ω

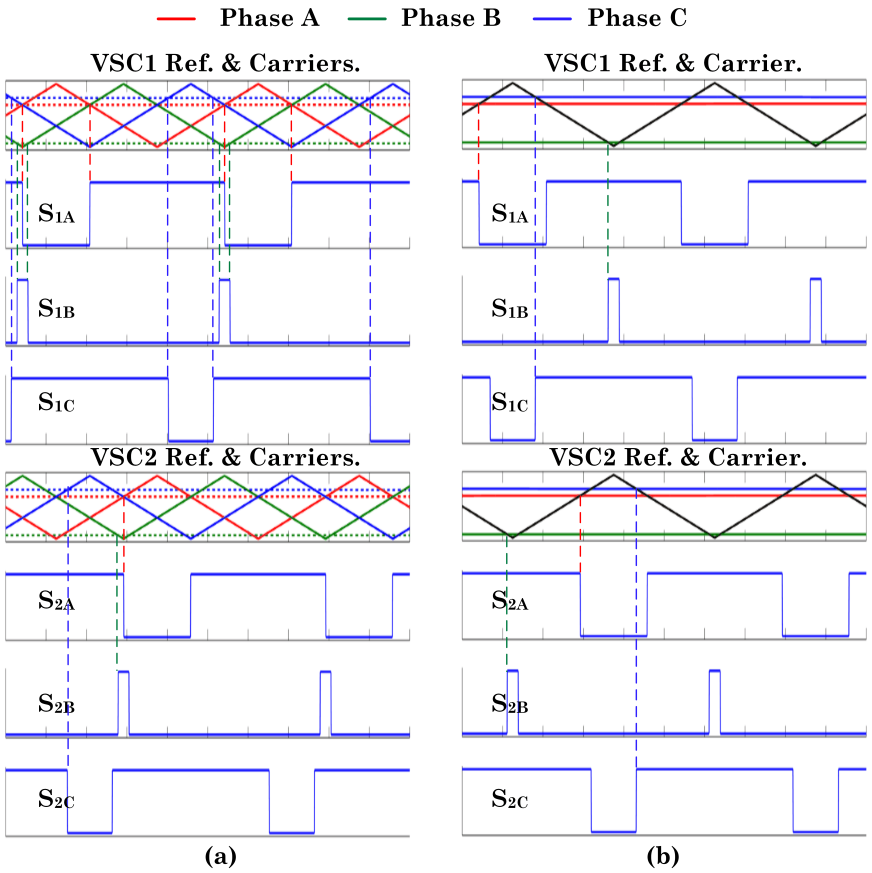


Figure 3.1. The carriers and PWM signals with different schemes, (a) S2DoF interleaving scheme, and (b) S1DoF interleaving scheme.

3.2 Impact on CMCC Peak Value

Based on the harmonic distribution analysis in Chapter 2, the harmonics in DMCC and CMCC of two interleaved 2L converters can be readily obtained. All harmonics with odd m values are distributed to the circulating current with both S1DoF and S2DoF schemes. Following (2.12), (2.13), and (2.19), the harmonic distribution in DMCC and CMCC can be visualized in **Fig. 3.3** for two interleaved converters.

To examine the peak value of the resultant CMCC with different methods, the amplitudes of dominant harmonic are calculated based on the system parameters and compared in **Fig. 3.4**. Note that the magnitudes are normalized to V_{DC}. It is clear to see that harmonic (1, 0) has the highest magnitude, and the lower M, the higher its magnitude. Therefore, by excluding harmonic (1,

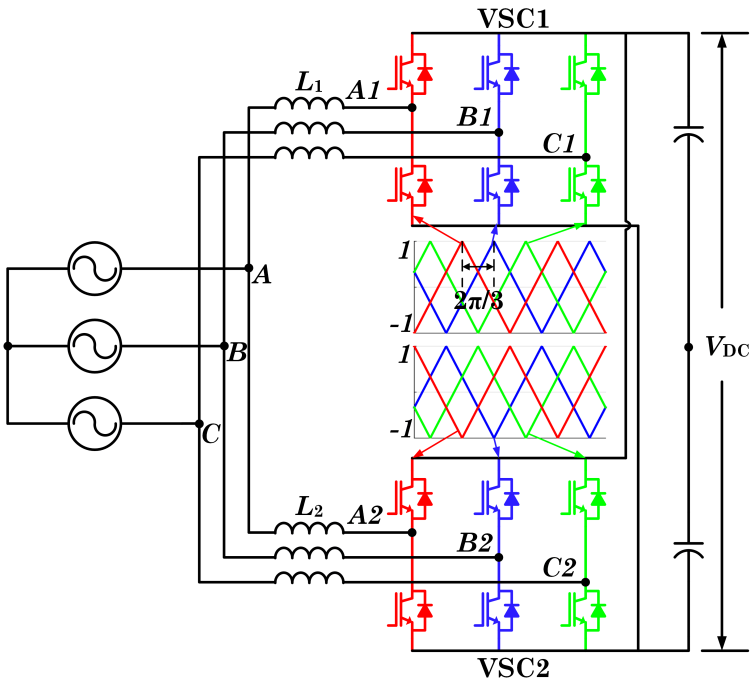


Figure 3.2. Implementation example of the S2DoF scheme in two parallel 2L VSCs.

DMCC CMCC

(m, n)	(1, -4)	(1, -2)	(1, 0)	(1, 2)	(1, 4)	(3, -6)	(3, -4)	(3, -2)	(3, 0)	(3, 2)	(3, 4)	(3, 6)
S1DoF												
S2DoF												

Figure 3.3. Harmonic distribution in the circulating current of two interleaved 2L VSC with different modulation schemes.

0) from CMCC, the S2DoF scheme can significantly reduce the peak value of CMCC. Also, contrary to the CMCC with S1DoF scheme, the peak value of CMCC with S2DoF scheme should decrease with M, indicating that the maximum CMCC value with S2DoF will be much smaller than that with S1DoF. Moreover, since harmonic (1, 0) will always be distributed into circulating current regardless the number of converters, it can be concluded that the S2DoF scheme will always result in lower CMCC than the S1DoF scheme.

Above analysis considers the case without CMO injection. But the comparison between S1DoF and S2DoF schemes will not be affected with CMO. For one, the some low-order triplen harmonics (e.g. 3rd and 9th) created by CMO will not appear in the harmonic content of CMCC as harmonics with

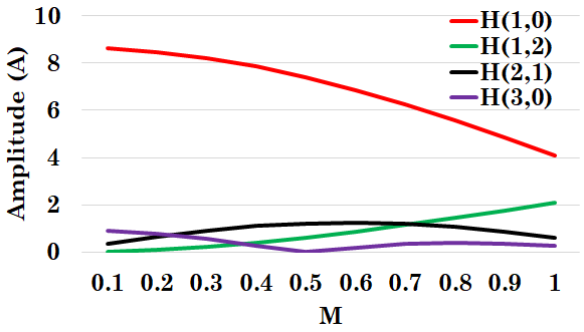


Figure 3.4. Comparison of the amplitudes of different harmonics that may appear in CMCC.

$m = 0$ cannot be cancelled through interleaving. For another, the harmonic amplitudes in S1DoF and S2DoF will be altered to the same degree by CMO. As such, the S2DoF will still result in much lower CMCC than S1DoF, though the actual amplitude of CMCC will change. The simulation and experimental verifications will be presented in the following two subsections to demonstrate the CMCC suppression performance of the proposed S2DoF scheme.

3.2.1 Simulation Results

To verify the harmonic distribution in CMCC, simulated spectra of CMCC with two interleaved converters and different schemes are shown in **Fig. 3.5**. One can see that harmonic (1, 0), which appears in the spectrum of CMCC with S1DoF scheme, is replaced by harmonic (1, 2) in the CMCC spectrum with the S2DoF scheme.

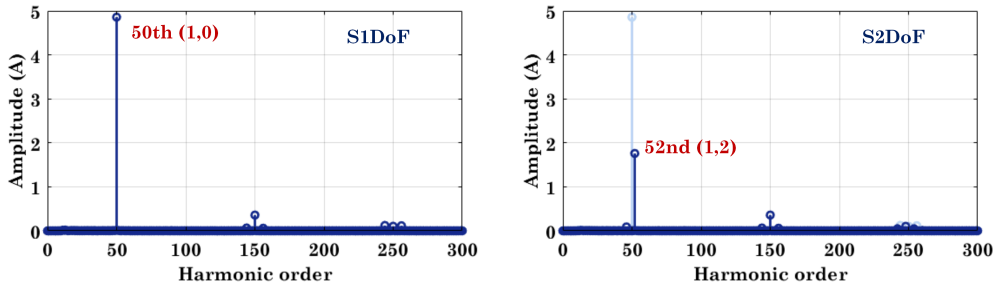


Figure 3.5. Simulated spectra of CMCC with two interleaved converters. Modulation index of 0.9 is used to obtain the spectra.

When CMO injection is not considered, simulation results with N = 2 to 6

are obtained and shown in **Fig. 3.6**. It is evident that the proposed S2DoF interleaving scheme always produces lower CMCC than the conventional S1DoF scheme, regardless the number of converters.

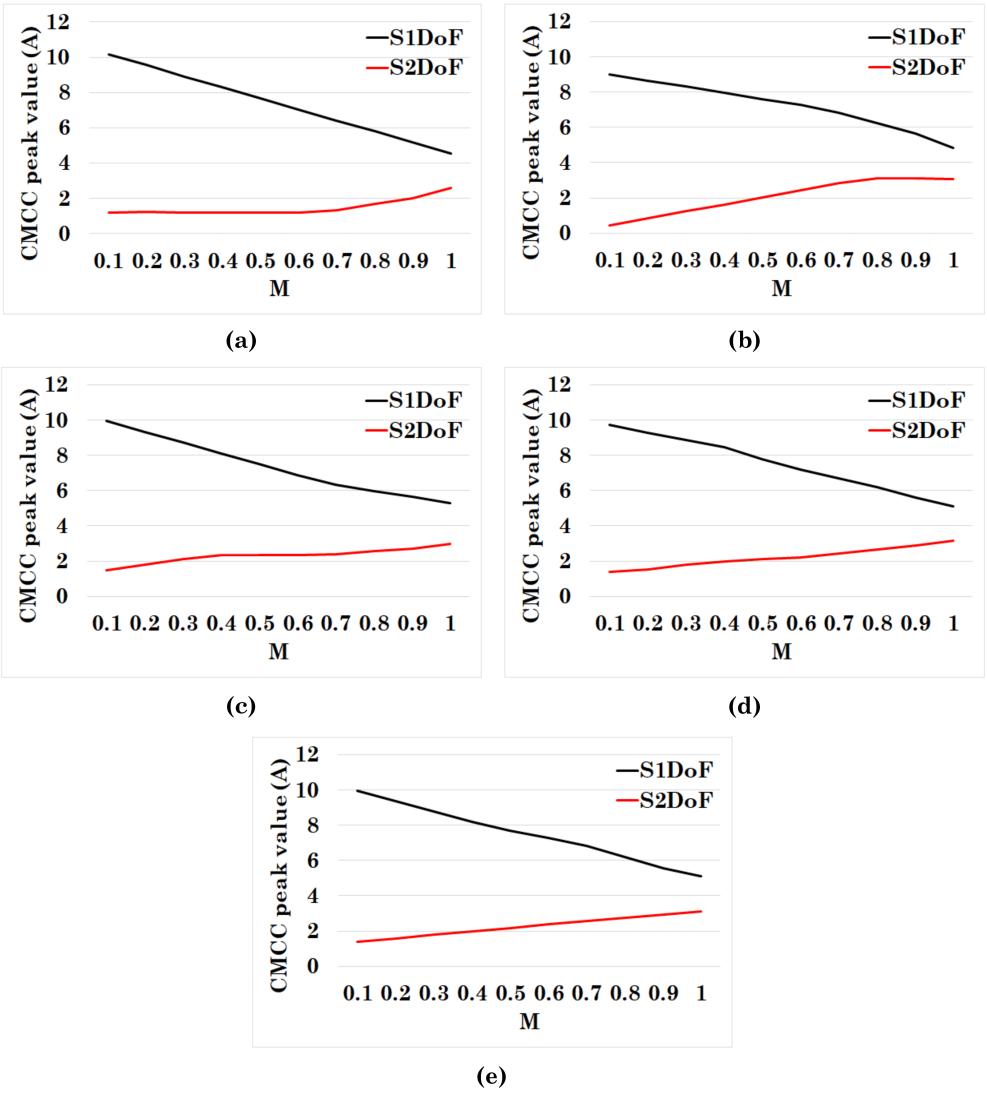


Figure 3.6. Simulation results of CMCC peak value when CMO is not injected: (a) $N = 2$, (b) $N = 3$, (c) $N = 4$, (d) $N = 5$, and (e) $N = 6$.

The simulation results with CMO injection are shown in **Fig. 3.7**, confirming that the S2DoF scheme still results in the lowest CMCC. Different types of CMO signals can be found in Appendix B. Note that only the CMO for continuous modulation is injected to the S2DoF scheme, leading to a continuous S2DoF (CS2DoF) scheme. The other two schemes are the continuous S1DoF (CS1DoF) scheme (i.e. SVPWM [70]) and discontinuous S1DoF (DS1DoF)

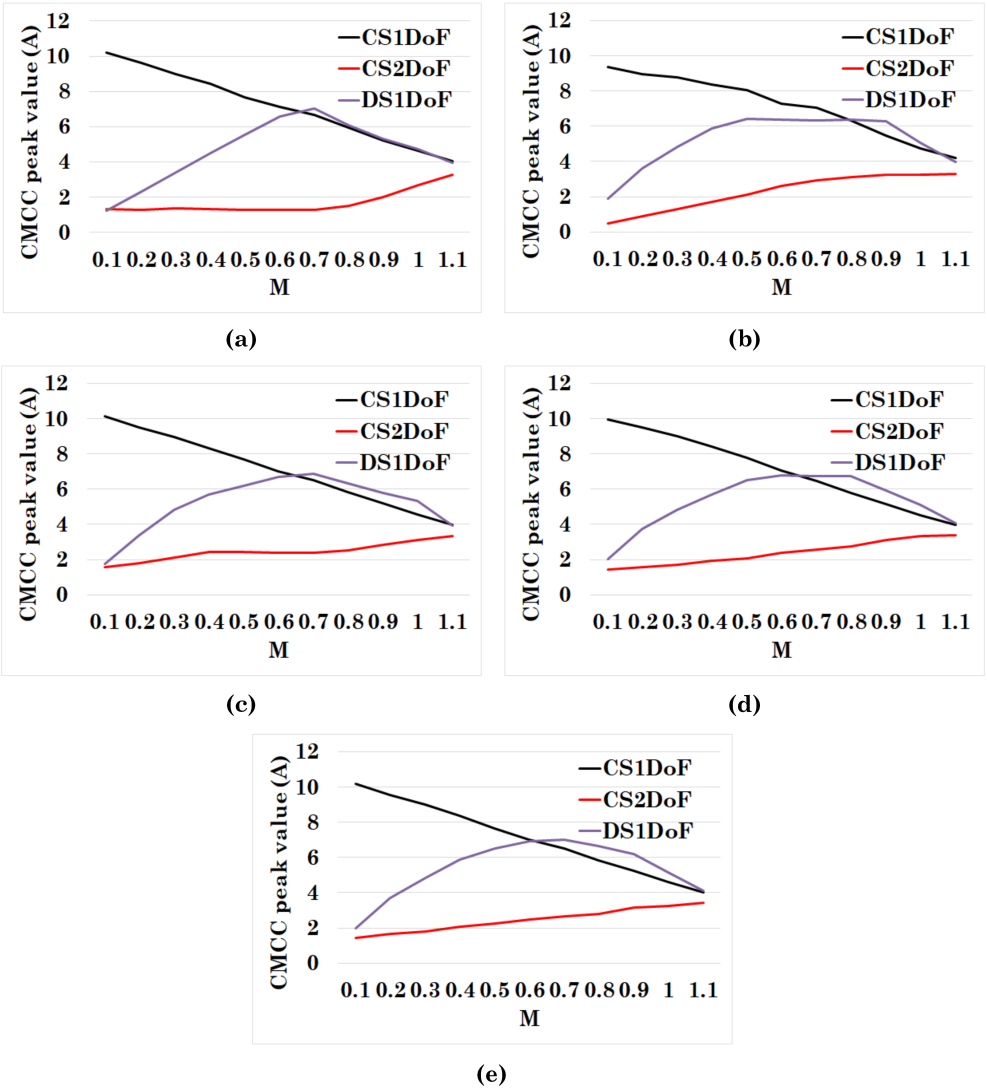


Figure 3.7. Simulation results of CMCC peak value with CMO injection: (a) $N = 2$, (b) $N = 3$, (c) $N = 4$, (d) $N = 5$, and (e) $N = 6$.

scheme. In this thesis, the CMO resulting in DPWM1 scheme is applied [76]. Note that there also are other types of discontinuous CMO signals, though not as popular as the DPWM1 scheme, that can be applied [70, 77].

3.2.2 Experimental Results

The experimental waveforms without CMO injection are shown in **Fig. 3.8**. The comparison of two schemes is shown in **Fig. 3.9**. Evidently, the proposed S2DoF interleaving scheme produces much lower CMCC than the S1DoF scheme. The maximum CMCC peak with S2DoF is even lower than the min-

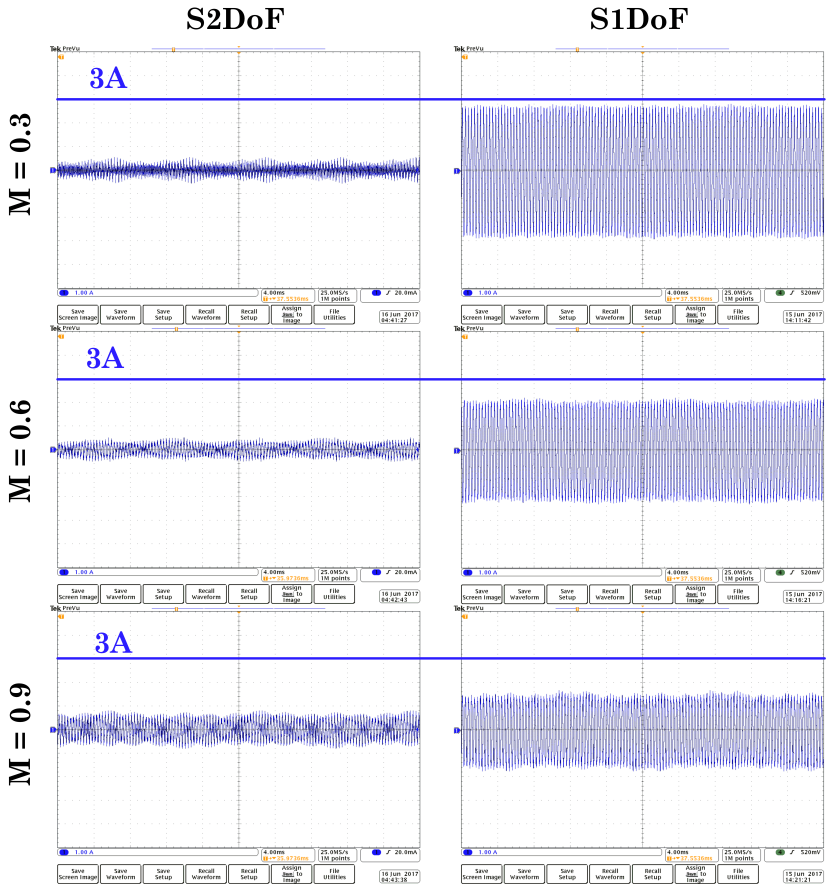


Figure 3.8. Measured CMCC waveforms without CMO injection under different modulation indices.

imum peak value produced by S1DoF. The spectra of the measured CMCC waveforms are shown in **Fig. 3.10**, demonstrating good agreement with the analysis.

When CMO injection is adopted. The measured waveforms are shown in **Fig. 3.11**. The results with different methods are compared in **Fig. 3.12**, showing that the proposed CS2DoF scheme can significantly reduce the maximum value of CMCC as compared to CS1DoF and DS1DoF schemes.

3.3 Quality of Output Voltage & Current

With interleaving, the output voltage and current quality can generally be improved as a great portion of harmonics are distributed into the circulating current, and thus will not appear in the output voltage and current. Based

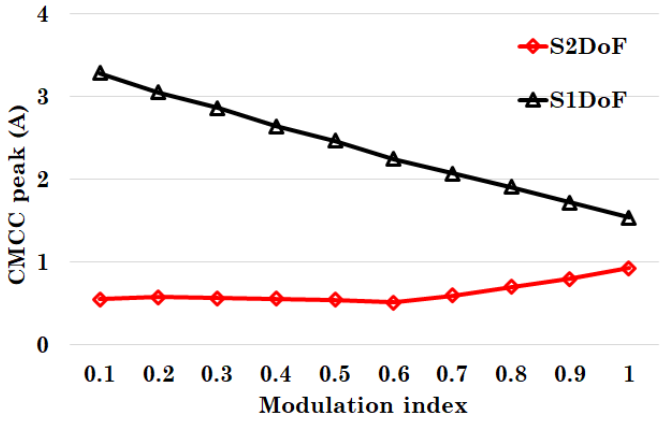


Figure 3.9. Comparison of the CMCC peak values resultant from S1DoF and S2DoF schemes.

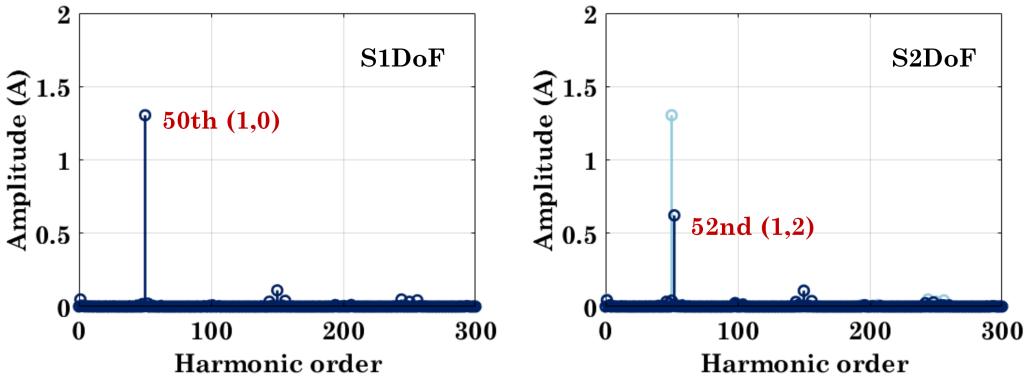


Figure 3.10. Spectra of measured CMCC waveforms with two interleaved converters. Modulation index of 1 is used to obtain the spectra.

on (2.17) in Chapter 2, it is straightforward that all harmonics with $m \neq N$ will be removed from the output. As such, the more converters in parallel, the better the output quality will be. For two interleaved converters, harmonics with $m =$ even values remain in the output voltage and current. With conventional S1DoF interleaving scheme, the dominant harmonics will be $(2, \pm 5)$ and $(2, \pm 1)$. However, when the proposed S2DoF interleaving scheme is applied, the distributions of harmonics in DM domain and CM domain will be altered. As a result, the dominant harmonics become (2, -1), $(2, \pm 3)$, and (2, -5).

To compare the two schemes in terms of voltage quality, the amplitudes of above dominant harmonics are calculated based on DFI. Note that the amplitudes are normalized to the DC link voltage. The calculated results

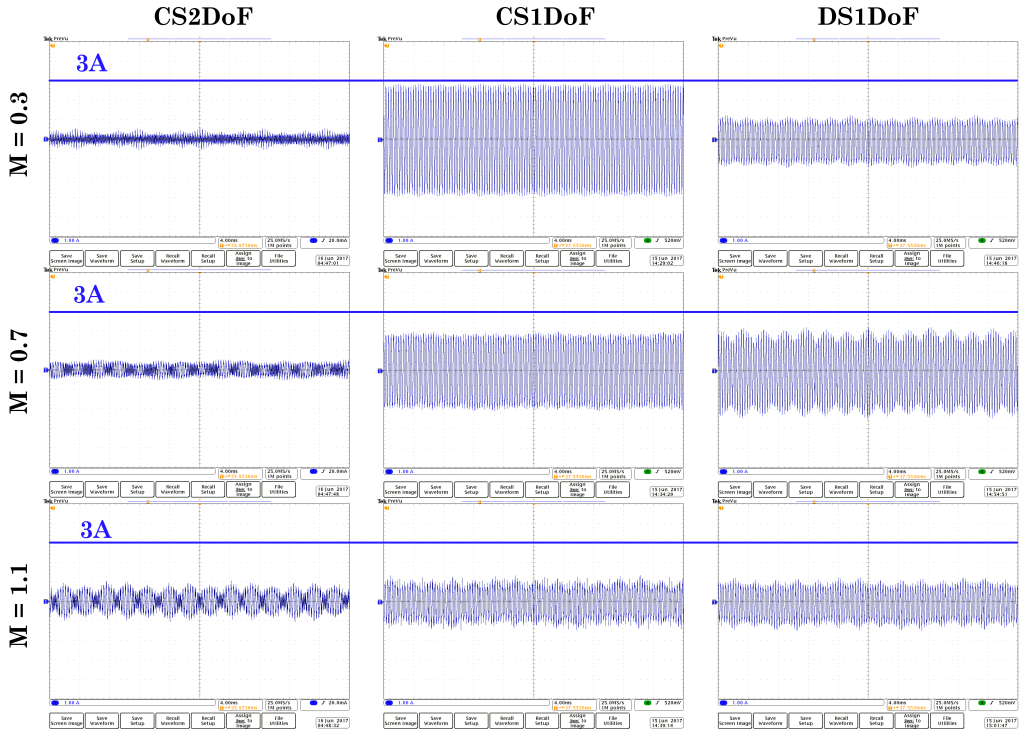


Figure 3.11. Measured CMCC waveforms with CMO injections under different modulation indices.

when CMO is not injected are shown in **Fig. 3.13**. It can be seen that the harmonic $(2, \pm 1)$ are much higher than harmonics $(2, \pm 3)$, especially in mid and low modulation index ranges. As such, elimination of $(2, 1)$ may improve the quality of output voltage, though harmonics $(2, \pm 3)$ are introduced.

With more converters, the results can be different. But since higher-order harmonics tend to have reduced amplitudes, the performances with S1DoF and S2DoF schemes should be comparable. It is worth noting that when $m =$ multiples of 3, the two schemes should produce the same output quality. As indicated by (2.17), the distributions of the harmonics with $m =$ multiples of 3 are the same with the two schemes.

3.3.1 Simulation Results

With two interleaved converters, the output line voltage waveforms and their spectra are shown in **Fig. 3.14**. As can be seen from the spectra, the harmonics are distributed following the rule identified in Chapter 2.

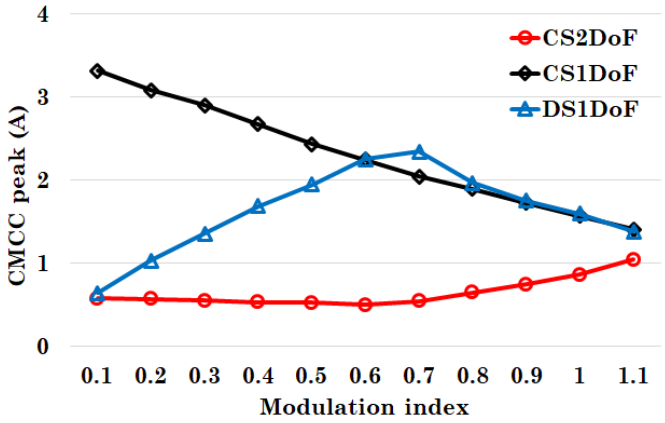


Figure 3.12. Comparison of the CMCC peak value resultant with different schemes.

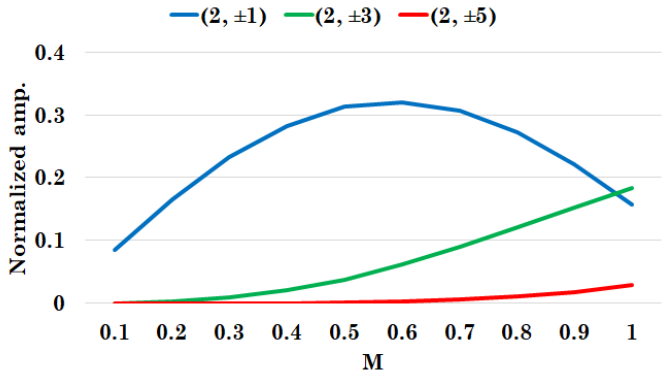


Figure 3.13. Amplitudes of dominant harmonics in the output voltage of two interleaved 2L VSCSs in respect to modulation index.

The simulated THD results of output line voltage with different N are shown and compared in **Fig. 3.15**. One can see that for two interleaved converters, the voltage quality with S2DoF interleaving scheme is better than that with the S1DoF scheme. With more converters in parallel, the performances of the two methods are comparable in general. With $N = 3$ or 6, the two methods produce the same voltage quality. Same conclusion can be found from the weighted THD (WTHD) results shown in **Fig. 3.16**. But when $N = 2$, the S1DoF scheme shows a slightly lower WTHD value when modulation index is higher than 0.9, indicating that the output current quality will be better in this operation range. But in general, the current quality with S2DoF is better for two interleaved converters.

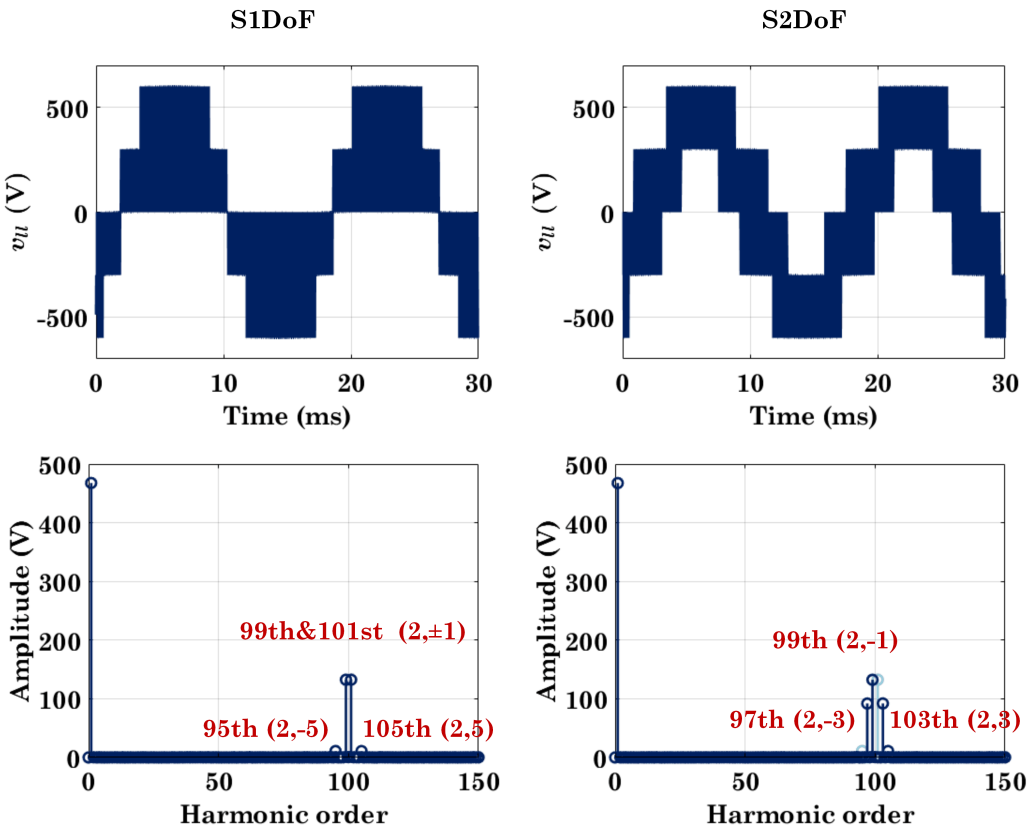


Figure 3.14. Simulated line-to-line voltage waveforms and spectra of two interleaved converters with different methods.

The simulated results of output current THD with different N are shown in **Fig. 3.17**. With CMO injection, the results are shown in **Fig. 3.18**. As expected, S2DoF and CS2DoF show better performance than S1DoF and CS1DoF when $N = 2$. When $N = 3$ and 6, the two methods deliver the same results. With other values of N, the two methods are in general comparable. The DS1DoF scheme shows overall similar performances to the other two methods. Note that only resistive load is used here. In practical applications, the load or grid can be inductive, and as such the performances of the above methods should be similar.

3.3.2 Experimental Results

Experimental results with two interleaved converters have been obtained. **Fig. 3.19** shows the measured waveforms of the line voltage and current with S1DoF

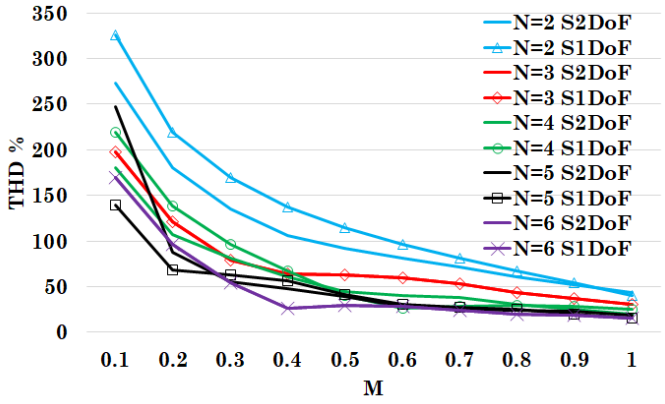


Figure 3.15. Simulated line-to-line voltage THD results with different N and methods.

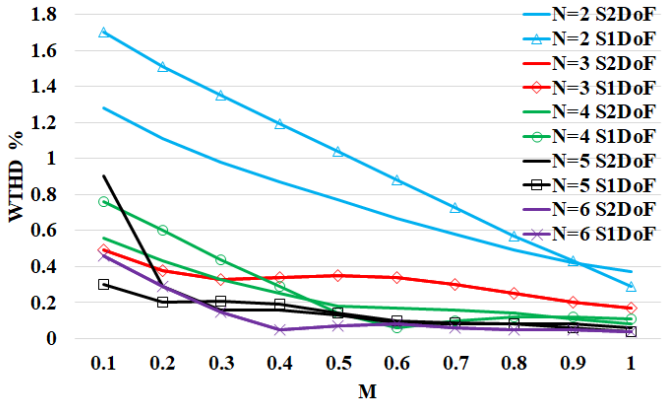


Figure 3.16. Simulated line-to-line voltage WTHD results with different N and methods.

and S2DoF schemes. Corresponding spectra with modulation index being 0.9 are shown in **Fig. 3.20**, from which one can see that the results are in accordance with the analysis and simulation results. The line voltage THD results with the two methods are compared in **Fig. 3.21**. As expected from analysis and simulation, the proposed S2DoF scheme delivers better overall performance than the S1DoF scheme. When CMO injections are applied, the comparison results are shown in **Fig. 3.22**. As can be seen, the DS1DoF scheme has s lightly better performance than the proposed CS2DoF scheme. But both methods have higher line voltage quality than the CS1DoF scheme.

The output current waveforms are also measured. Without CMO injection, the waveforms are shown in **Fig. 3.23**. Evidently, the S1DoF scheme results

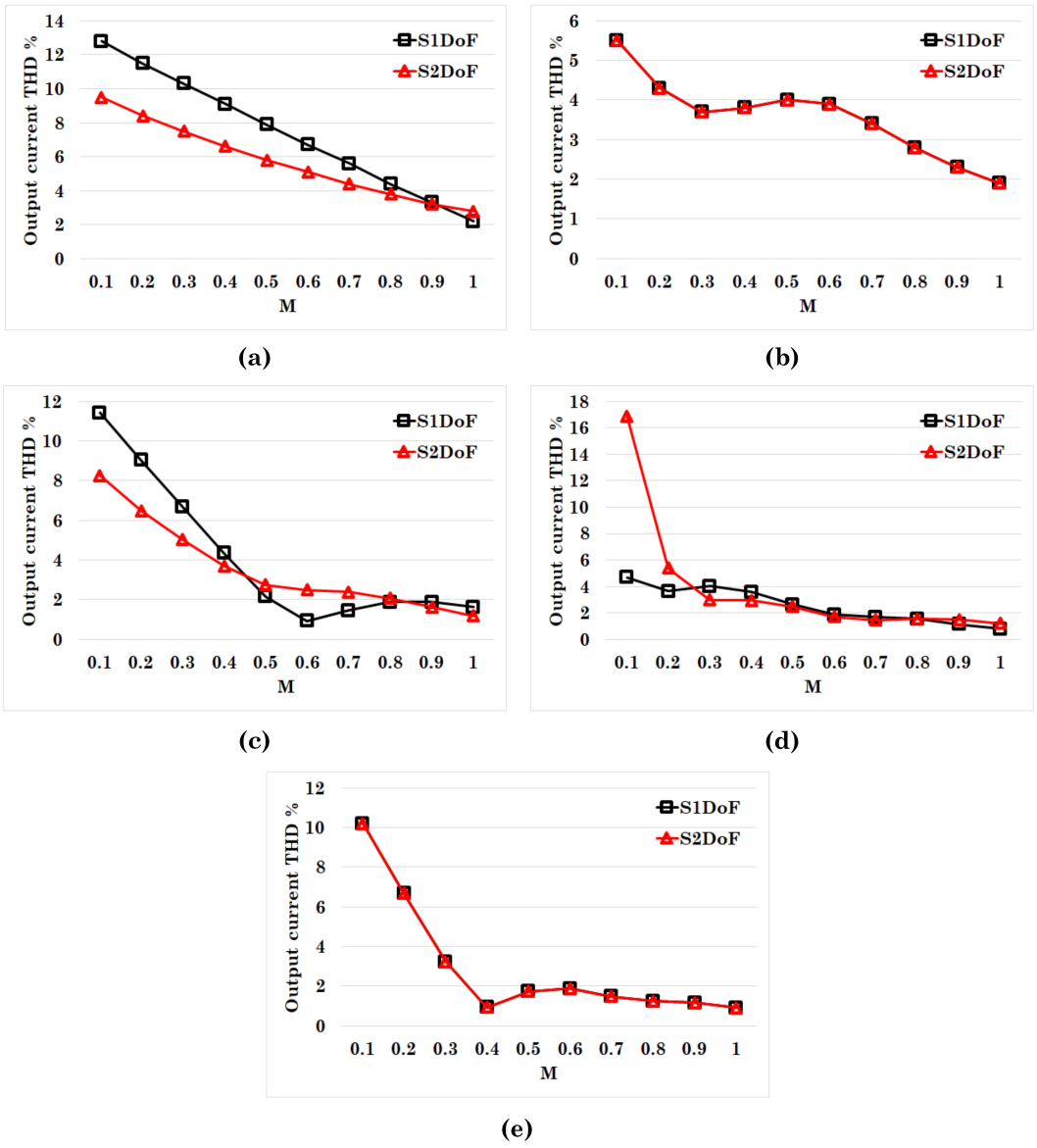


Figure 3.17. Simulated output current THD results with different N and methods: (a) $N = 2$, (b) $N = 3$, (c) $N = 4$, (d) $N = 5$, and (e) $N = 6$.

in larger output current ripple than the S2DoF scheme. This is translated to higher THD values with the S1DoF scheme, as shown in the comparison results in **Fig. 3.24**.

When CMO injections are applied, the measured waveforms are presented in **Fig. 3.25**. Correspondingly, the comparison results of the three methods are shown in **Fig. 3.26**. As can be seen, the comparison results are in accordance with the simulation results. Note that if inductive load is used, all

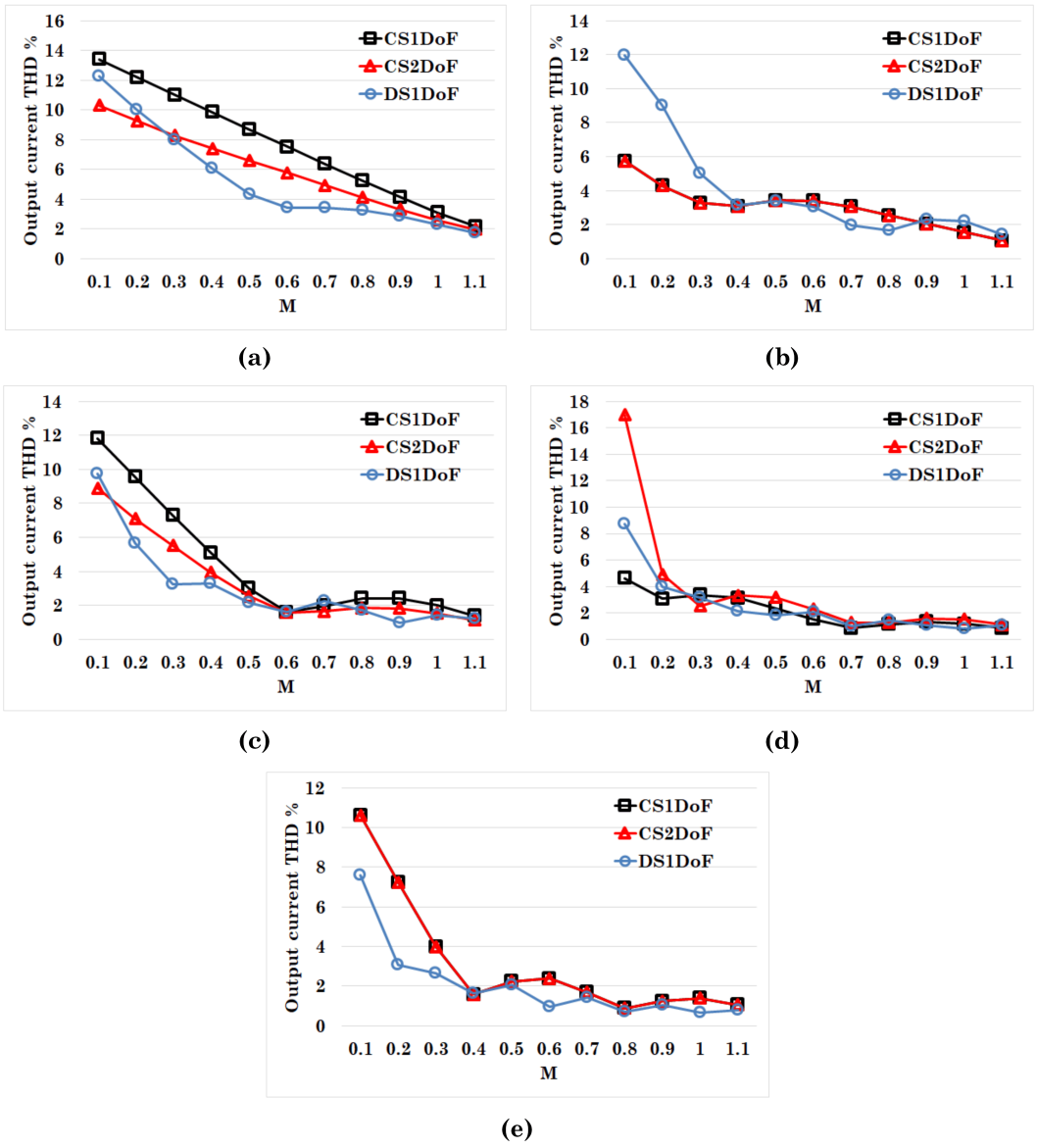


Figure 3.18. Simulated output current THD results with CMO injection and different N and methods: (a) $N = 2$, (b) $N = 3$, (c) $N = 4$, (d) $N = 5$, and (e) $N = 6$.

three methods should have comparable performances.

3.4 Evaluation of the Resultant CM Voltage

In symmetrical interleaving schemes, the harmonics on CM voltage are those excluded from the output voltage. Therefore, improved output quality usually implicates an increased CM voltage, since more harmonics are transferred into

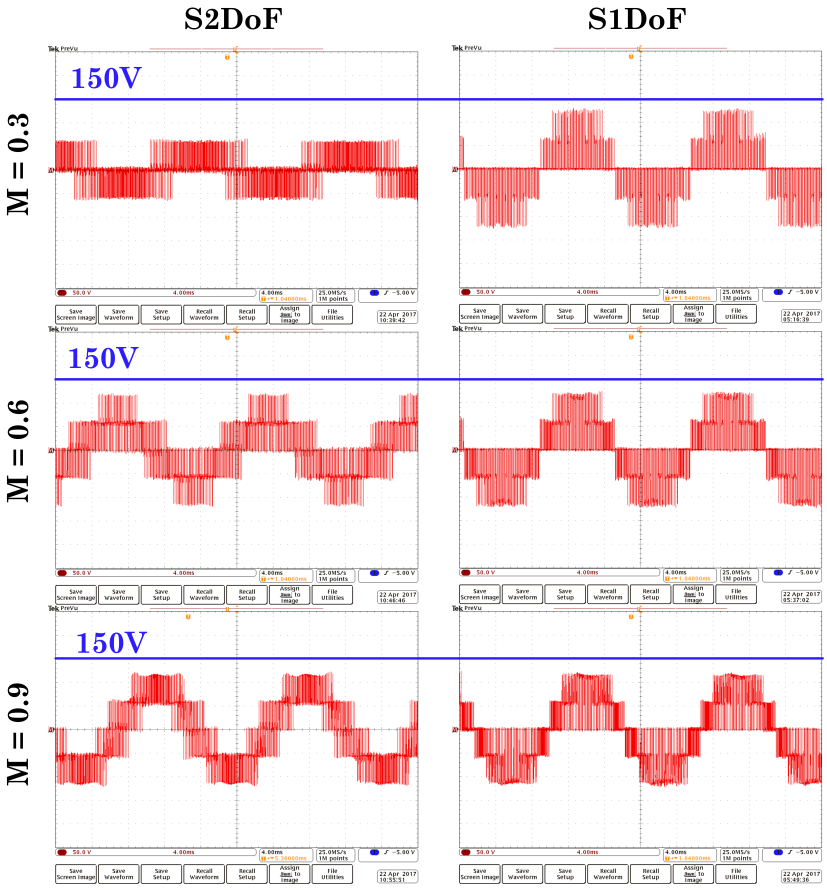


Figure 3.19. Measured waveforms of output line voltage under different modulation indices.

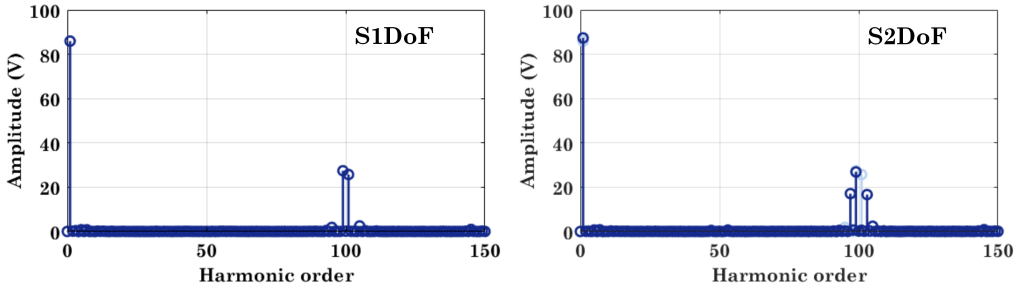


Figure 3.20. Harmonic spectra of the line voltages resultant with the two methods. Modulation index is 0.9.

CM voltage. Visualized in **Fig. 3.27** is the harmonic distribution in line voltage v_{LL} and CM voltage v_{CM} with two interleaved converters. As detailed in the previous analysis, S2DoF scheme provides improved output quality as compared to the S1DoF scheme. As such, it can be expected that the CM

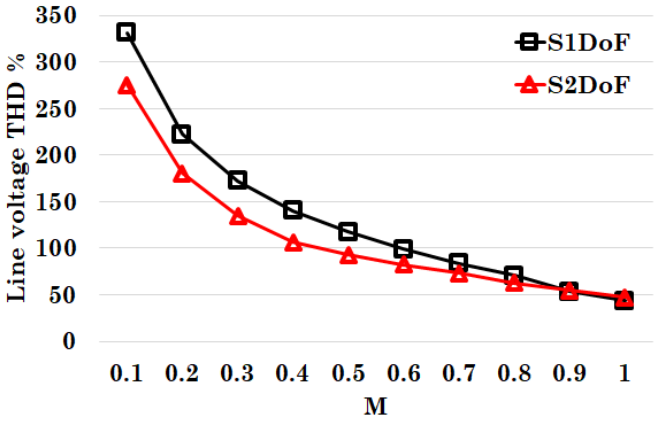


Figure 3.21. Comparison in terms of the line voltage THD results resultant without CMO injection.

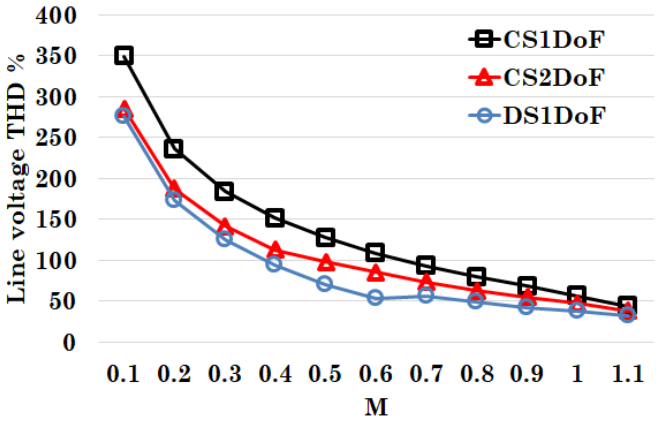


Figure 3.22. Comparison in terms of the line voltage THD results when CMO injections are applied.

voltage resultant with S2DoF scheme will be higher.

3.4.1 Without CMO Injection

Examining the amplitudes of the dominant harmonics in CM voltage confirms the expectation. As shown in **Fig. 3.28**, harmonic (2, 1) is much larger than the harmonics $(2, \pm 3)$ in most of the modulation index range. Hence the resultant CM voltage with S2DoF scheme should be higher than that with S1DoF when $N = 2$. Note that the amplitudes are normalized to the DC link voltage in **Fig. 3.28**. For other values of N, same analysis can be performed.

The simulation CM voltage magnitudes with $N = 2$ to 6 are shown in **Fig.**

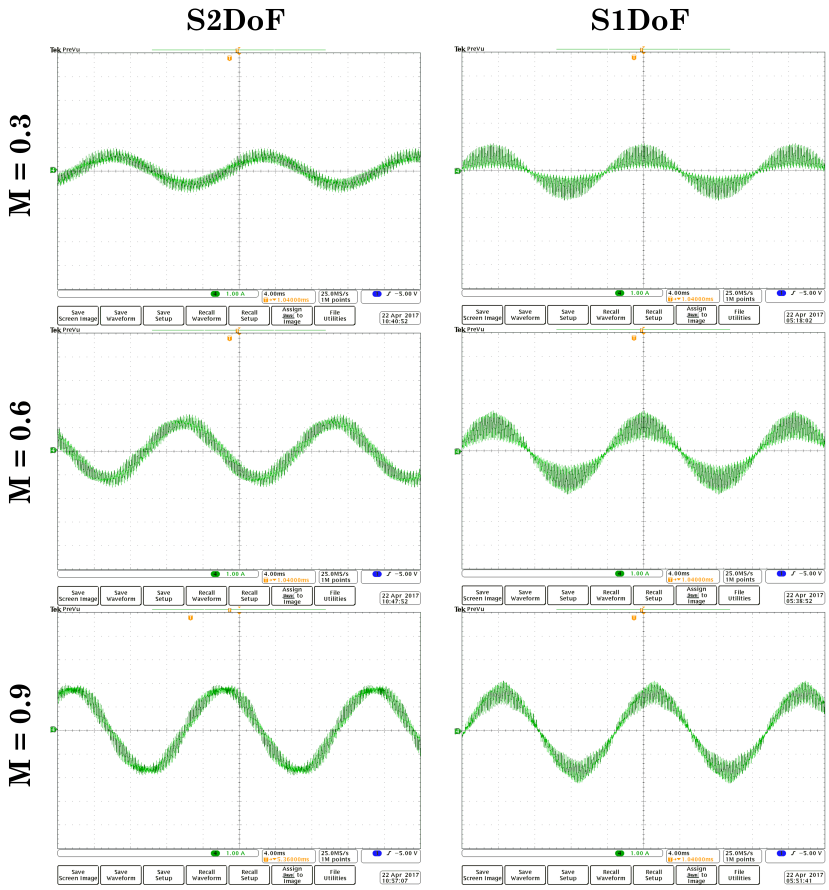


Figure 3.23. Measured output current waveforms with different modulation indices. CMO injection is not applied. Scale: 1A/div.

3.29. Note that the magnitudes are normalized to the DC link voltage. As analyzed, when N is 2, the resultant CM voltage with S2DoF is higher than that with S1DoF. Also, it can be seen that when N is multiples of 3, the resultant CM voltage magnitudes are same with the two methods. For other values of N, the two methods have comparable performances.

In addition, it is interesting to note that the magnitude of CM voltage is not always reduced with the increase of N. For example, when modulation index is higher than 0.6, the CM voltage with S1DoF and $N = 3$ is higher than that when $N = 2$. This is because the output is four-level, which is an even value, when $N = 3$, and the resultant CM voltage has no zero state. In both methods, the normalized CM voltage is always lower than 0.5, indicating that compared to single converter, the CM voltage can be reduced by interleaving.

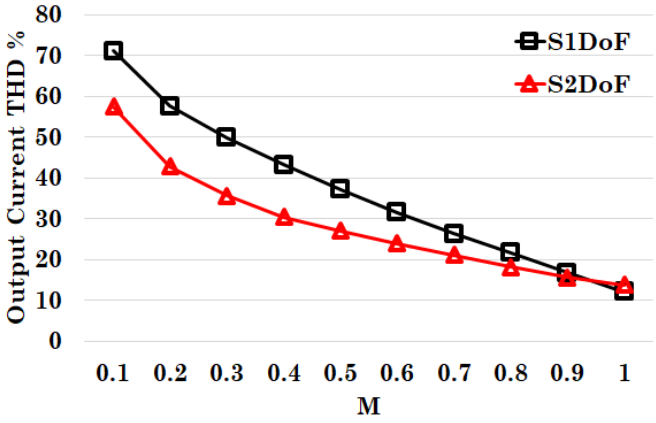


Figure 3.24. Comparison in terms of the output current THD results without CMO injection.

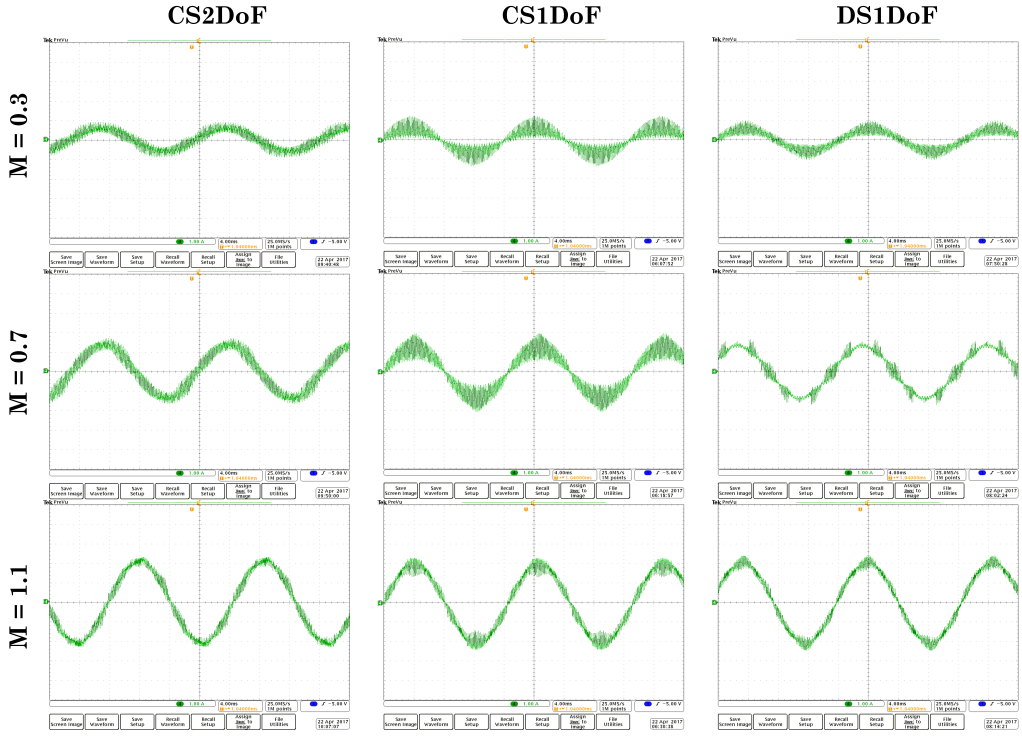


Figure 3.25. Measured output current waveforms with different modulation indices. CMO injections are applied. Scale: 1A/div.

The experimental waveforms and corresponding spectra are shown in **Fig. 3.30**, demonstrating the analysis and simulation results. The magnitudes with different modulation indices are the same as the simulation results, and thus are not repeated.

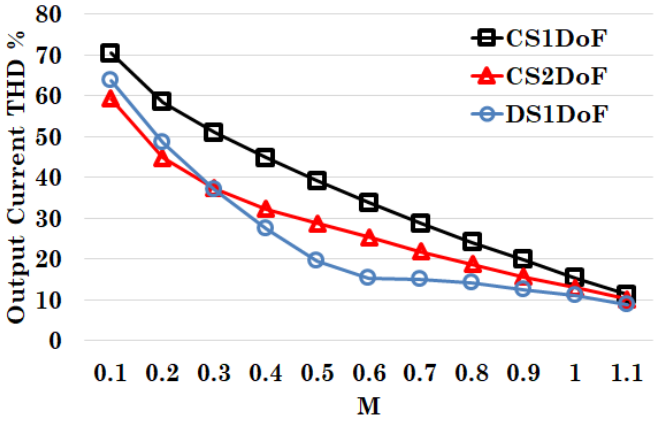


Figure 3.26. Comparison in terms of the output current THD results when CMO injections are applied.

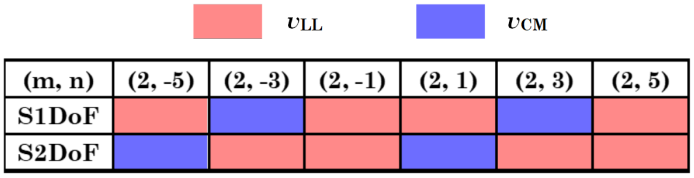


Figure 3.27. Harmonic distribution in v_{LL} and v_{CM} with two interleaved converters.

3.4.2 With CMO Injection

Different from the analysis for CMCC and output quality, the impact of CMO injection needs to be investigated in particular for the CM voltage. As interleaving cannot cancel the harmonics with $m = 0$, the low-order triplen harmonics induced by CMO signals are all distributed into the CM voltage.

The calculated amplitudes of harmonic (0, 3) with respect to the modulation index are shown in **Fig. 3.31 (a)**. It can be seen that the harmonic (0, 3) with DS1DoF is increasing while modulation index is decreasing. Also, its amplitude is much higher than that with CS2DoF or CS2DoF, especially in low modulation index range. This can be explained from the nature of the injected CMO signals. The magnitude of the injected CMO signal in CS1DoF and CS2DoF is decreasing as modulation index drops. Thus, the third-order component in the CM voltage spectrums also decreases with modulation index. However, in the DS1DoF scheme, in order to keep the modulating signal

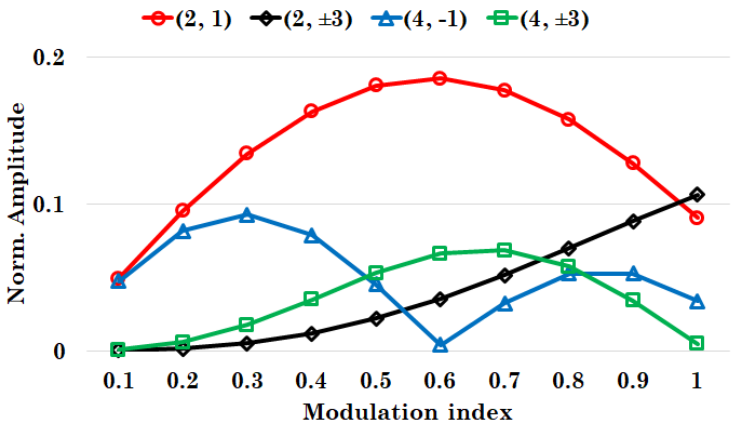


Figure 3.28. Calculated amplitudes of the dominant harmonics in CM voltage as a function of modulation index.

clamped to the upper or lower DC rail, the magnitude of the injected CMO signal is actually increasing as modulation index decreases. Therefore, the third-order component becomes higher in low modulation index range. Accompanying the harmonic (0, 3), intensive low order harmonics are also generated with DS1DoF scheme. **Fig. 3.31 (b)** shows the amplitude of other low-order triplen harmonics in DS1DoF, where one can see that the amplitudes of these harmonics are also significant.

The amplitudes of high-order dominant harmonics are also calculated and are shown in **Fig. 3.32**. It can be seen that the amplitude of harmonic $(2, \pm 3)$ with DS1DoF is obviously different from that with CS1DoF due to the impact of the CMO signal. The amplitude of $(2, \pm 3)$ with DS1DoF is much higher than that with CS1DoF in high and low modulation index ranges, but is lower in the mid modulation index range.

Further comparing the amplitudes of low-order harmonics and high-order harmonics, it is found that the high-order harmonics with CS1DoF scheme is approximately at the same level with its low-order harmonics, whereas the CS2DoF scheme results in higher high-order harmonics, indicating the CM voltage with CS2DoF should be higher than that with CS1DoF. On the contrary, DS1DoF produces significantly increased low-order harmonics. As such, the resultant CM voltage will be much higher than that with CS1DoF or CS2DoF. More importantly, since these low-order harmonics will also appear

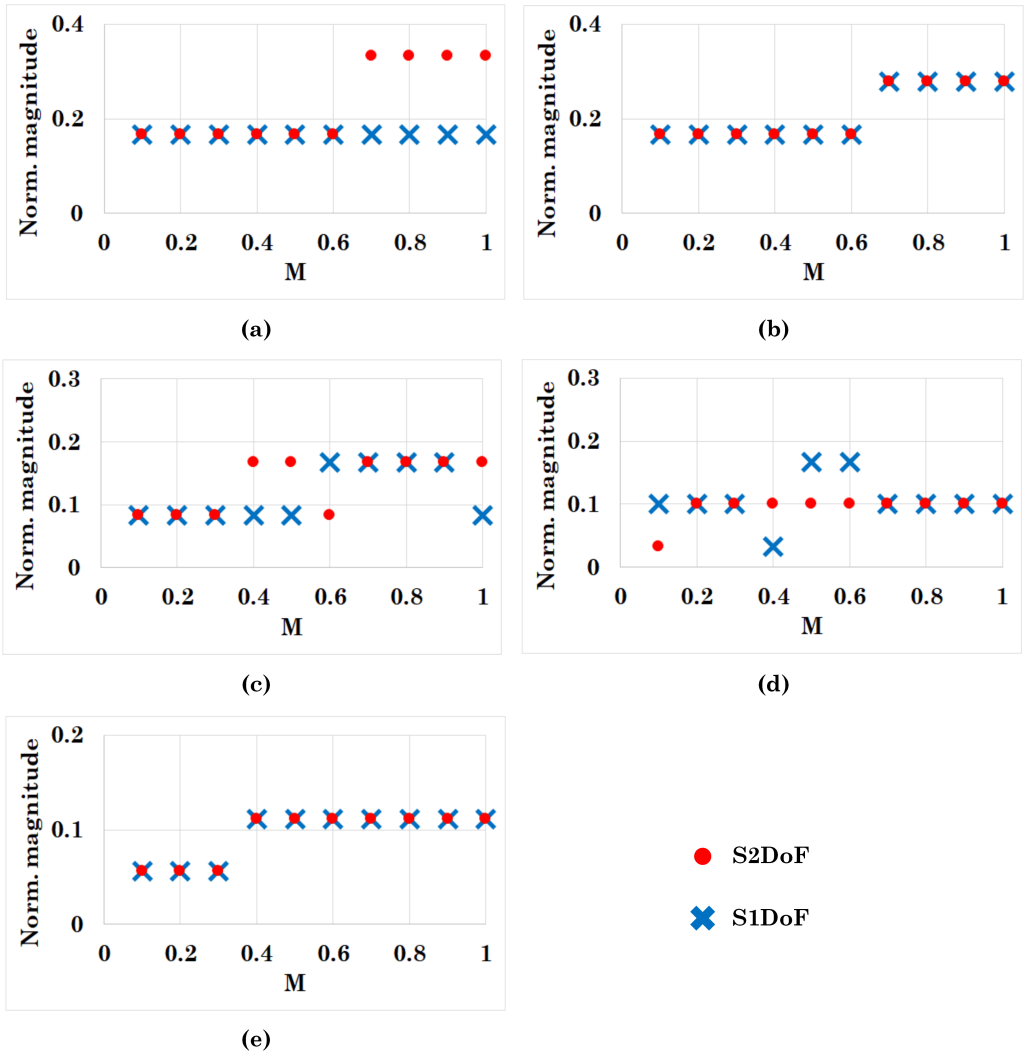


Figure 3.29. Simulated CM voltage magnitude with respect to modulation index when CMO is not injected, (a) N=2; (b) N=3; (c) N=4; (d) N=5; (e) N=6.

in the CM voltage, the CM voltage with DS1DoF scheme cannot be reduced with interleaving. To verify the analysis, simulation results and experimental results are shown in **Fig. 3.33** and **Fig. 3.34**, respectively. The simulation and experimental results well confirm the analysis.

3.5 Summary

This chapter proposes and evaluates the 2DoF interleaving schemes for the modular parallel 2L converters. The foremost advantage of the proposed

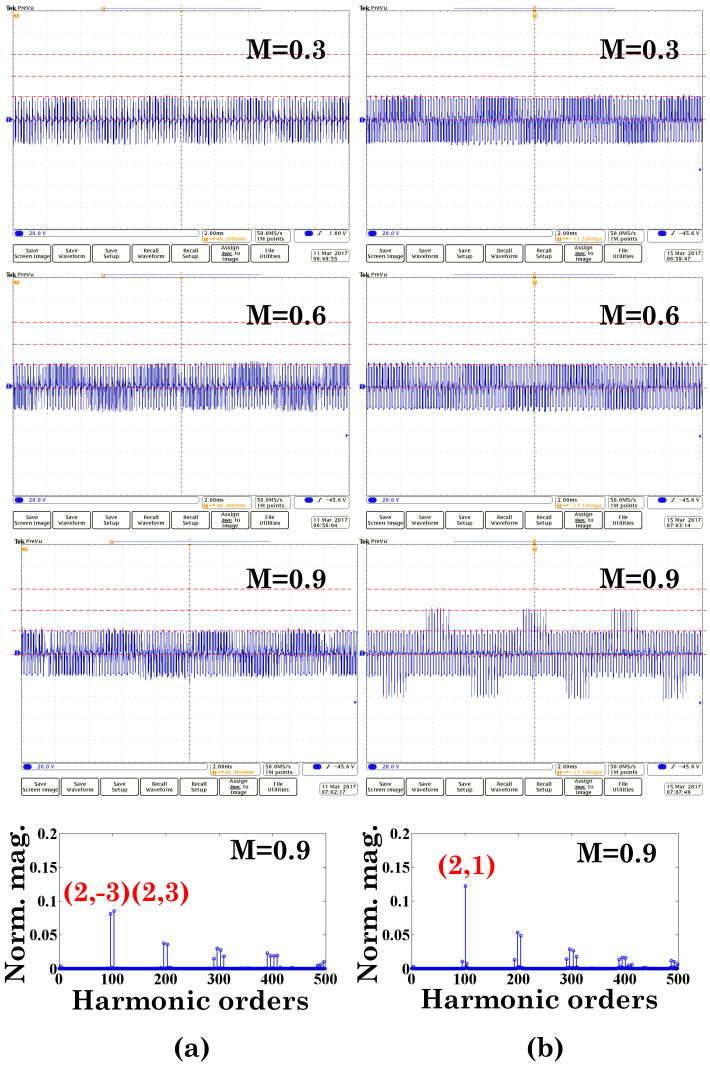


Figure 3.30. Experimental waveforms and spectra of CM voltage with, (a) S1DoF and (b) S2DoF. (20V/div)

method is that it can suppress CMCC regardless the number of converters in parallel. With CMO injection, this advantage is still valid. Unlike S1DoF scheme, CS1DoF scheme, and DS1DoF scheme, the S2DoF and CS2DoF schemes produce the maximum CMCC peak value when modulation index is at its max point, i.e. 1 for S2DoF and 1.15 for CS2DoF. As such, interleaving becomes applicable in the modular parallel converters.

Besides their superior performances in CMCC suppression, the 2DoF interleaving schemes also deliver comparable or even better performances in terms of output quality and CM voltage than the conventional schemes. For the

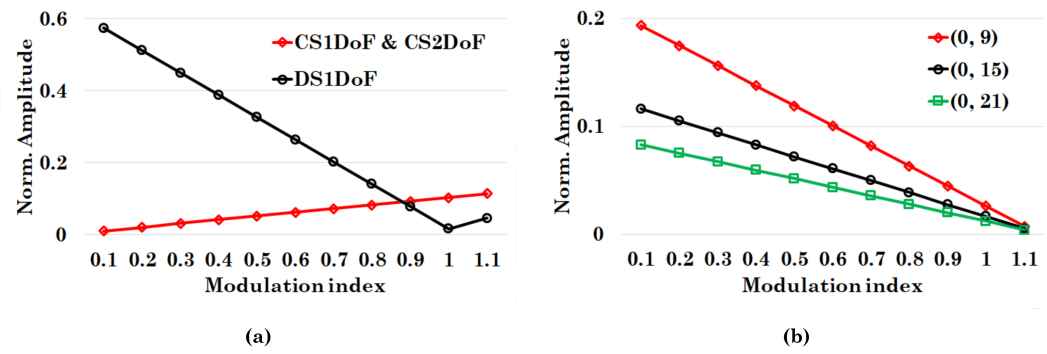


Figure 3.31. Calculated amplitudes of the low-order harmonics in CM voltage as a function of modulation index: (a) harmonic (0, 3) with different schemes, (b) other triplen harmonics with DS1DoF scheme.

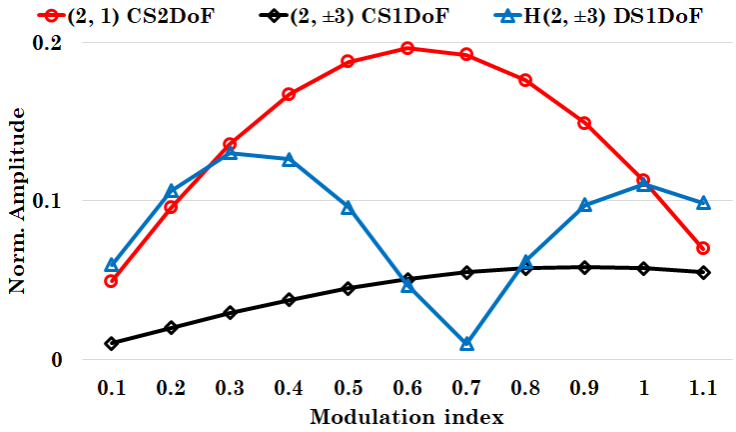


Figure 3.32. Calculated amplitudes of the high-order dominant harmonics in CM voltage as a function of modulation index when CMO injections are applied.

output quality, when only two converters are in parallel, the output voltage with S2DoF has lower THD values in nearly entire modulation index range than that with S1DoF scheme. With CMO injections, the CS2DoF scheme still achieves better output quality than the CS1DoF scheme. The DS1DoF scheme has the best performance in this case. But the performance of CS2DoF is very close to that of the DS1DoF. For system with more than two converters, all methods deliver similar performances in general.

As for the CM voltage, the 2DoF interleaving schemes result in higher CM voltage than the S1DoF scheme and CS1DoF scheme when only two converters are in parallel, since more harmonics are transferred into the CM voltage. But

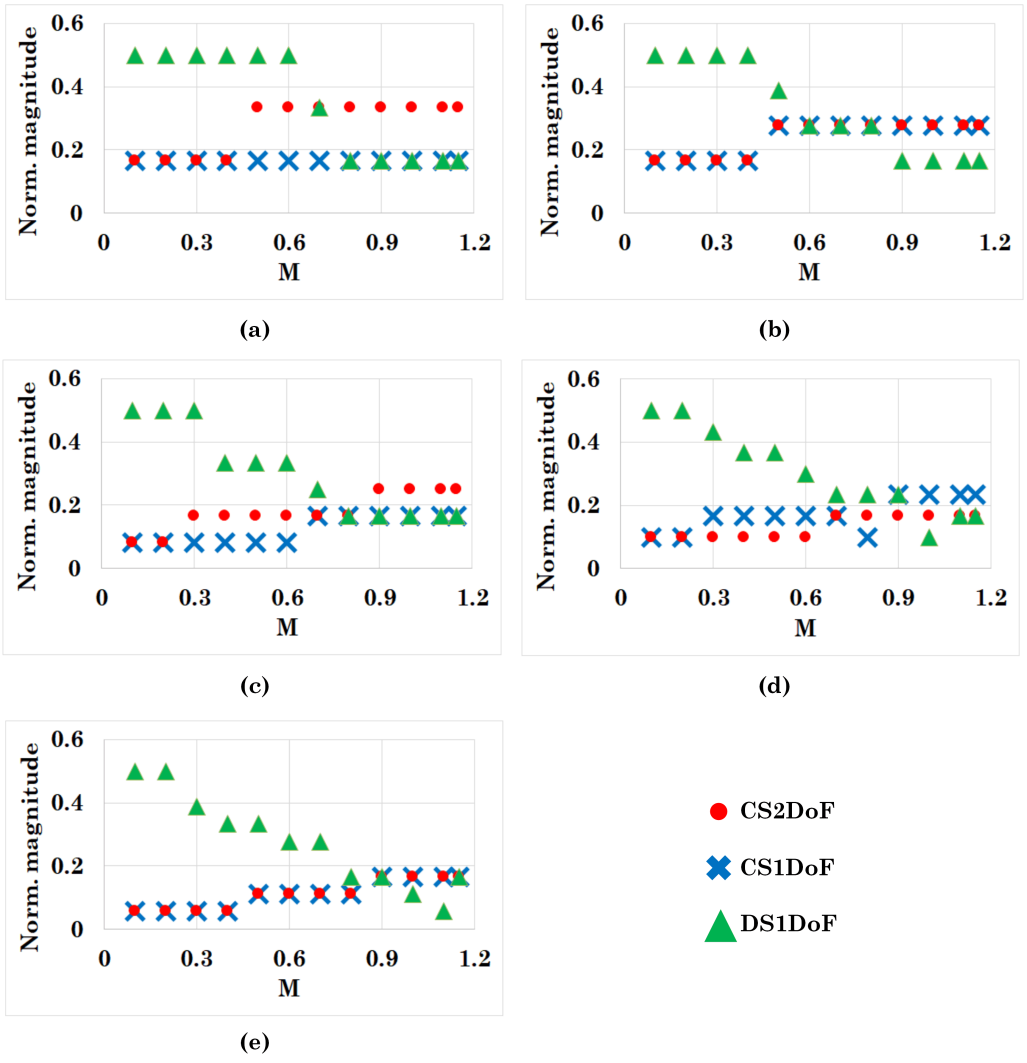


Figure 3.33. Simulated CM voltage magnitude with respect to modulation index when CMO injections are applied, (a) N=2; (b) N=3; (c) N=4; (d) N=5; (e) N=6.

for system with more converters, their performances are generally comparable. Moreover, it is interesting to see that the CM voltage cannot be mitigated with the DS1DoF interleaving scheme, as its dominant CM harmonics are low-order triplen ones that cannot be cancelled through interleaving. Since the magnitudes of these low-order harmonics are much higher than the high-order ones, the CM voltage with DS1DoF scheme will always be larger than that with CS1DoF or CS2DoF scheme. Finally, the number of the converters also plays an important role in determining the overall CM voltage of the system. It is preferable to avoid using three or five or other odd number of

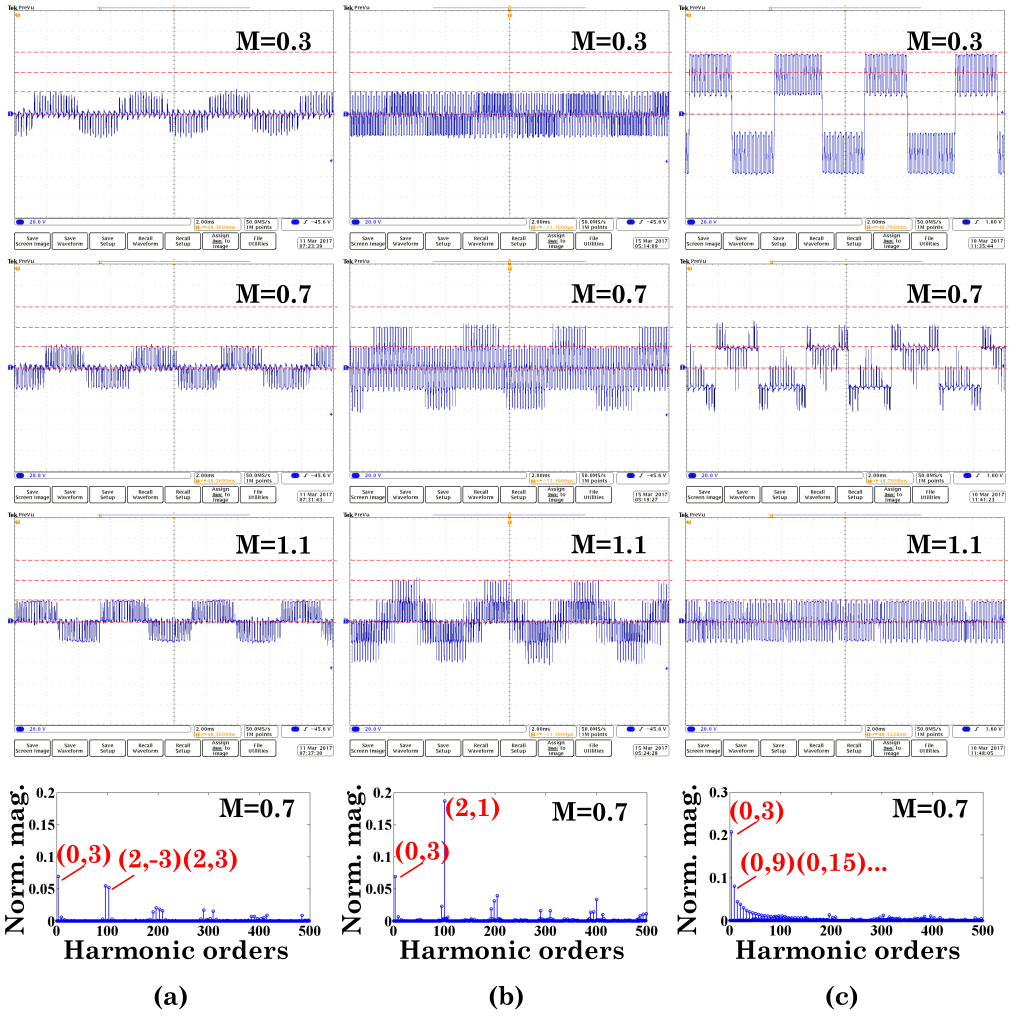


Figure 3.34. Experimental waveforms and spectra of CM voltage with, (a) CS1DoF, (b) CS2DoF, and (c) DS1DoF. (20V/div)

converters as these designs tend to result in higher CM voltage.

Chapter 4

Evaluation of 2DoF Interleaving in Modular Parallel Multilevel VSCs

In Chapter 3, the S2DoF scheme (and the CS2DoF scheme) demonstrated promising performances for the modular parallel 2L VSCs. Besides 2L VSC, modular parallel multilevel converters are increasingly adopted in practical applications. Same as in parallel 2L converters, the CMCC issue in interleaved multilevel converters needs to be looked into. However, multilevel converters have several different modulation options, e.g. phase disposition (PD), phase opposition disposition (POD), alternative phase opposition disposition (APOD), and Phase-shift (PS) PWM. Each of them can be generalized into a 2DoF scheme. Therefore, it is necessary to evaluate and compare these methods in order to design or select the proper interleaving strategy.

This chapter presents a comprehensive study on the interleaved multilevel converters. The analysis starts with 3L VSC as an example and is generalized to higher-level converters. The DFI expressions for the multilevel converters are significantly more complex than those for a 2L converter. As such, derivation and computation for the three-phase results will be complicated. But with the aid of the harmonic distribution analysis in Chapter 2, the analysis can be simplified to a great extent. The study in this chapter reveals that the PD based S2DoF (PD-S2DoF) interleaving scheme is the best fit for the 3L VSC based modular parallel converter system owing to its superior performance

in CMCC suppression. A generalized analysis considering high-level (beyond 3L) converters reveals that the PD-S2DoF's advantage in CMCC suppression will still be valid. However, further discussion indicates that integrating 2DoF scheme with PS-PWM will not bring significant performance improvements. Therefore, considering the wide implementation of PS-PWM in high-level (beyond 3L) converters, the implementation range of 2DoF interleaving scheme is limited to only 2L and 3L converters.

4.1 Potential Multilevel Modulation Schemes

Conventionally, three types of modulation schemes can be applied, i.e. PD PWM, POD PWM, and APOD PWM. These methods can be referred as level-shift PWM[1]. Similar to the SPWM for 2L converter, all three multilevel schemes can be generalized by introducing an additional phase shift angle θ_{ps} within an individual converter.

The generalized modulation scheme of the PD PWM for one three-phase 5L converter is shown in **Fig. 4.1**, where θ_{ps} is the phase shift angle among the carrier groups. Conventionally, all three phases share the same group of carriers. However, in the generalized scheme, each phase is assigned a group of carriers. Each group then has four carrier signals stacked in phase from top to bottom. Similar to the PD scheme, the POD scheme and the APOD scheme can both be generalized, as shown in **Fig. 4.2** and **Fig. 4.3**, respectively.

Conventionally, PD results in the best output voltage quality, whereas it produces the highest CM voltage among the three methods. On the contrary, POD and APOD has lower output quality but the CM voltage generated from either one is also lower. However, by setting θ_{ps} as $2\pi/3$, the results will be different, as indicated by the harmonic distribution analysis in Chapter 2. For single multilevel converter, conventional PD modulation usually is the best choice as the CM voltage can be mitigated by various kinds of CM filters.

[1]Phase-shift (PS) PWM can also be applied for flying capacitor based topologies, but is not included here. For one, flying capacitor converter is not as popular as NPC, TNPC, or ANPC converters in practical applications. For another, the DM harmonics and CM harmonics are evenly distributed with PS-PWM. A such, using 2DoF-interleaving will not bring significant performance improvements.

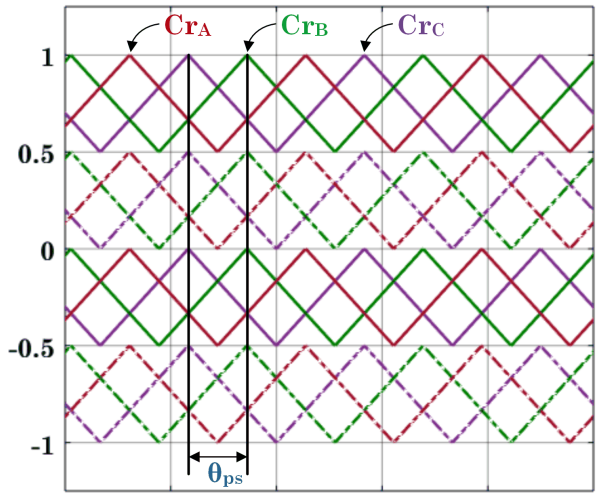


Figure 4.1. The generalized PD modulation scheme. The phase shift angle θ_{ps} used to generate this figure is $2\pi/3$. The carriers for the same phase are shown in the same color.

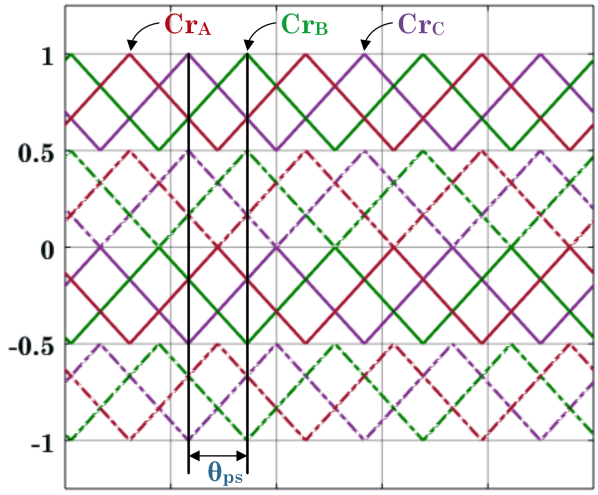


Figure 4.2. The generalized POD modulation scheme. The phase shift angle θ_{ps} used to generate this figure is $2\pi/3$. The carriers for the same phase are shown in the same color.

But when multiple converters are interleaved, the CMCC issue becomes a detrimental issue, which can only be suppressed with the inductance in CM loop. In the next section, the 3L VSC based modular parallel converter system is studied to reveal the most suitable solution.

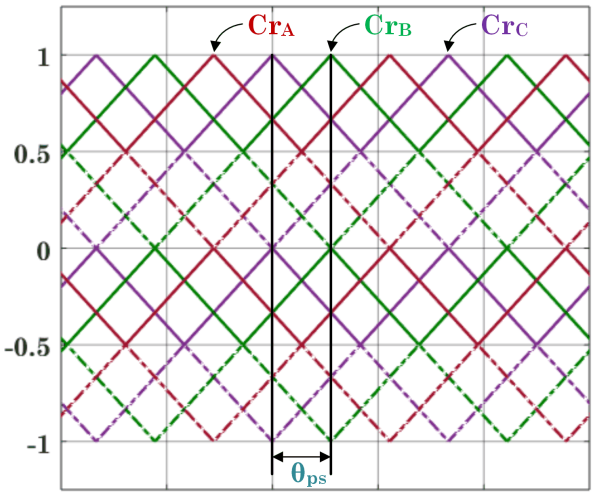


Figure 4.3. The generalized APOD modulation scheme. The phase shift angle θ_{ps} used to generate this figure is $2\pi/3$. The carriers for the same phase are shown in the same color.

4.2 Performance of 3L S2DoF Schemes

For 3L NPC or TNPC converter, APOD scheme is not applicable. Therefore, only two types of schemes, i.e. the PD based and the POD based, will be considered in this section. To compare the performances of conventional S1DoF interleaving schemes and the 2DoF-interleaving schemes, the amplitudes of the dominant harmonics need to be evaluated. The DFI expressions of the single phase-leg harmonic voltage are written in (4.1) and (4.2), respectively for PD and POD [70]. Following (2.12) and (2.13), when $\theta_{ps} = 2\pi/3$, harmonics with $(m + n) = 0$ or multiples of 3 will appear in the CM domain, whereas the others will be distributed into the DM domain. As such, it is easy to find the harmonic distributions, as visualized in **Fig. 4.4** and **Fig. 4.5** for PD and POD based schemes respectively. Note that only non-zero harmonics are illustrated. One can see that PD and POD has different harmonics with $m = 1$ and other odd values, whereas they are the same when $m =$ even values, as can be explained with their analytical expressions in (4.1) and (4.2). In the following subsections, the performances of four methods are evaluated based on the system parameters in **Table 4.1**. Proof-of-concept experimental

verifications have been conducted on two interleaved 3L converters. The interleaving schemes were implemented in DSP controller TMS320F28335. System parameters are also listed in **Table 4.1**. In both simulation and experiment, 3L T-type NPC (TNPC) converter topology is adopted.

$$A_{mn,PD}(m,n) = \begin{cases} -\frac{2V_{DC}}{m\pi^2}\left[1-\cos(m\pi)\right]\sum_{k=1}^{\infty}\frac{J_{2k-1}(m\pi M)}{2k-1} & m>0 \quad n=0 \\ \frac{V_{DC}}{2m\pi}\left[1-\cos((m+n)\pi)\right]J_n(m\pi M)\sin\left(\frac{\pi}{2}n\right) & \\ +\frac{2}{\pi}\cos\left(\frac{\pi}{2}n\right)\sum_{k=1}^{\infty}\frac{J_{2k-1}(m\pi M)(2k-1)}{(2k-1)^2-n^2} & m>0(odd) \quad n\neq 0(even) \\ \frac{V_{DC}}{2m\pi}\left[1-\cos((m+n)\pi)\right]J_n(m\pi M)\sin\left(\frac{\pi}{2}n\right) & m>0(even) \quad n\neq 0(odd) \end{cases} \tag{4.1}$$

$$A_{mn,POD}(m,n) = \frac{V_{DC}}{m\pi}J_n(m\pi M)\cos\left(\frac{n-1}{2}\pi\right) \tag{4.2}$$

DM CM

(m, n)	(1, -6)	(1, -4)	(1, -2)	(1, 0)	(1, 2)	(1, 4)	(1, 6)	(2, -7)	(2, -5)	(2, -3)	(2, -1)	(2, 1)	(2, 3)	(2, 5)	(2, 7)
PD-S1DoF															
PD-S2DoF															

Figure 4.4. Harmonic distribution in DM and CM domains with PD-S1DoF scheme and PD-S2DoF scheme.

DM CM

(m, n)	(1, -5)	(1, -3)	(1, -1)	(1, 1)	(1, 3)	(1, 5)	(2, -7)	(2, -5)	(2, -3)	(2, -1)	(2, 1)	(2, 3)	(2, 5)	(2, 7)
POD-S1DoF														
POD-S2DoF														

Figure 4.5. Harmonic distribution in DM and CM domains with POD-S1DoF scheme and POD-S2DoF scheme.

Table 4.1. System parameters for analysis and verifications.

Parameter	Simulation	Experiment
DC link voltage, V_{DC}	600V	120V
Carrier frequency, f_{cr}	3000Hz	3000Hz
Fundamental frequency, f_1	60Hz	60Hz
Current sharing inductance, L_{cc}	5mH	5mH
Load resistance,R_L	10Ω	29Ω

4.2.1 Impact on CMCC Peak Value

The harmonic distributions in circulating current can be visualized as in **Fig. 4.6** and **Fig. 4.7** for PD based schemes and POD based schemes respectively. Based on (2.19), the amplitudes of the harmonics in CMCC domain can be calculated and compared. The results are shown in **Fig. 4.8 (a)** for PD and in **Fig. 4.8 (b)** for POD. The harmonic amplitudes are normalized to $(m\omega_c + n\omega_1)L_{CM}$. Also, only those with $m = 1$ are compared as harmonics with $m = 3$ or higher will be suppressed by larger impedance. From **Fig. 4.8 (a)**, it is clear that harmonic (1, 0) is much higher than the others. Further comparing **Fig. 4.8 (a) and (b)**, one can see that the dominant harmonics in POD-S1DoF are lower than the harmonic (1, 0) in PD-S1DoF in mid and low modulation index range. That said, POD-S1DoF will result in lower CMCC than PD-S1DoF in this range. But since both harmonics $(1, \pm 3)$ appear in CMCC, and they have high amplitudes at high modulation index range, the CMCC with POD-S1DoF at this range may be close to that with PD-S1DoF. As a result, PD-S1DoF and POD-S1DoF may result in similar maximum CMCC peak values.

DMCC CMCC

(m, n)	(1, -6)	(1, -4)	(1, -2)	(1, 0)	(1, 2)	(1, 4)	(1, 6)	(3, -6)	(3, -4)	(3, -2)	(3, 0)	(3, 2)	(3, 4)	(3, 6)
PD-S1DoF														
PD-S2DoF														

Figure 4.6. Harmonic distribution in DMCC and CMCC with PD-S1DoF scheme and PD-S2DoF scheme.

DMCC CMCC

(m, n)	(1, -5)	(1, -3)	(1, -1)	(1, 1)	(1, 3)	(1, 5)	(3, -7)	(3, -5)	(3, -3)	(3, -1)	(3, 1)	(3, 3)	(3, 5)	(3, 7)
POD-S1DoF														
POD-S2DoF														

Figure 4.7. Harmonic distribution in DMCC and CMCC with POD-S1DoF scheme and POD-S2DoF scheme.

When S2DoF interleaving is applied, further CMCC reduction can be achieved with PD-S2DoF interleaving scheme since the dominant harmonic (1, 0) is completely transferred from the CM domain to the DM domain. As such, the dominant harmonics in CMCC become (1, -4) and (1, 2), which have even

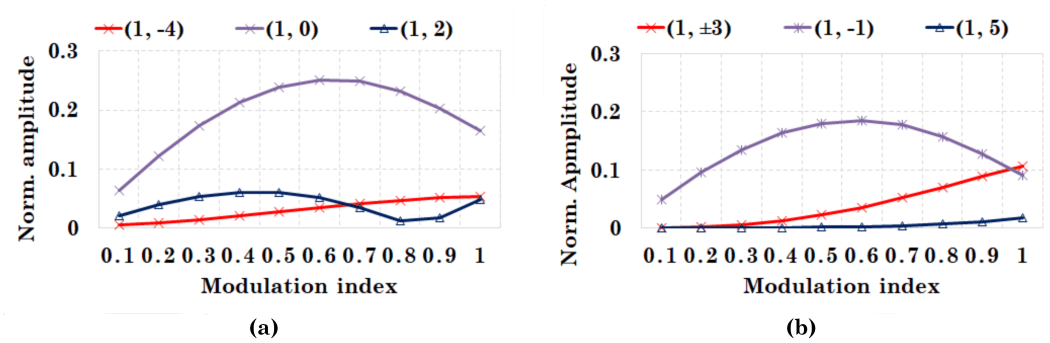


Figure 4.8. Calculated amplitudes of dominant harmonics in CMCC with (a) PD based schemes and (b) POD based schemes.

lower amplitudes than the harmonics $(1, \pm 3)$ in POD-S1DoF scheme. More importantly, since harmonics with $m = 1$ will be kept in the circulating current regardless the number of converters, it is obvious to see that PD-S2DoF interleaving will always produce the lowest CMCC. On the contrary, POD-S2DoF scheme will bring (1, -1) into CMCC, which obviously will increase the peak value of CMCC. As such, the POD-S2DoF scheme is not included in the following evaluations.

The simulation results of CMCC peak values with different number of converters are shown in **Fig. 4.9**. It is evident that the PD-S2DoF interleaving scheme produces the lowest CMCC regardless the number of converters. Compared to the S1DoF based schemes, more than 50% reduction of the maximum CMCC peak value can be achieved. Also, as expected from the analysis, the maximum CMCC with POD-S1DoF is close to that with PD-S1DoF when only two converters are interleaved.

The experimental waveforms of CMCC with two interleaved 3L TNPC converters are shown in **Fig. 4.10**. Due to the imperfection of system parameters, small low frequency CMCC variations exist. Such low frequency variation can be eliminated with a CMCC controller. As the proposed PD-S2DoF interleaving scheme is essentially a carrier based PWM, existing CMCC controller can be easily implemented. The peak values of all three methods are compared in **Fig. 4.11**. It is clear that the PD-S2DoF interleaving scheme produces the lowest maximum CMCC peak value. The harmonic spectra of the measured

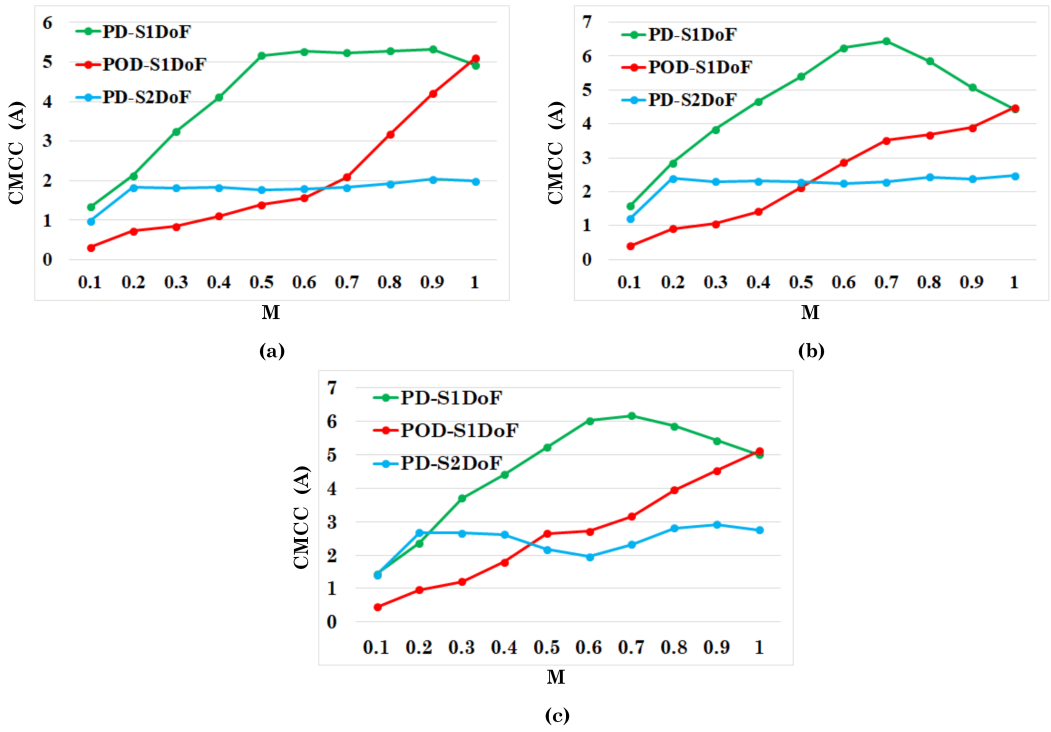


Figure 4.9. Simulation results of CMCC peak value with (a) $N = 2$, (b) $N = 3$, and (c) $N = 4$.

CMCC when $M = 0.9$ are shown in **Fig. 4.12**, from which one can see the impact of S2DoF interleaving on the harmonic distribution in CMCC. Evidently, harmonic (1, 0), i.e. the 50th harmonic, shown as the light colored background in the spectrum of PD-S2DoF, is eliminated in CMCC, whereas harmonic (1, -4), i.e. the 46th harmonic, appears. The experimental results are consistent with the analysis and simulation results, demonstrating the CMCC reduction performance of the proposed PD-S2DoF interleaving scheme.

4.2.2 Output Voltage & CM voltage

The output quality can be evaluated by comparing the dominant harmonics in the output voltage. Comparing **Fig. 4.4** and **Fig. 4.5**, one can see that the harmonic profiles with even m values are same in PD-S1DoF and POD-S1DoF, which can also be proved by (4.1) and (4.2). That said, PD-S1DoF and POD-S1DoF will result in the same output voltage (and current) when N is an even value. But when PD-S2DoF scheme is adopted, harmonics (2, -5)

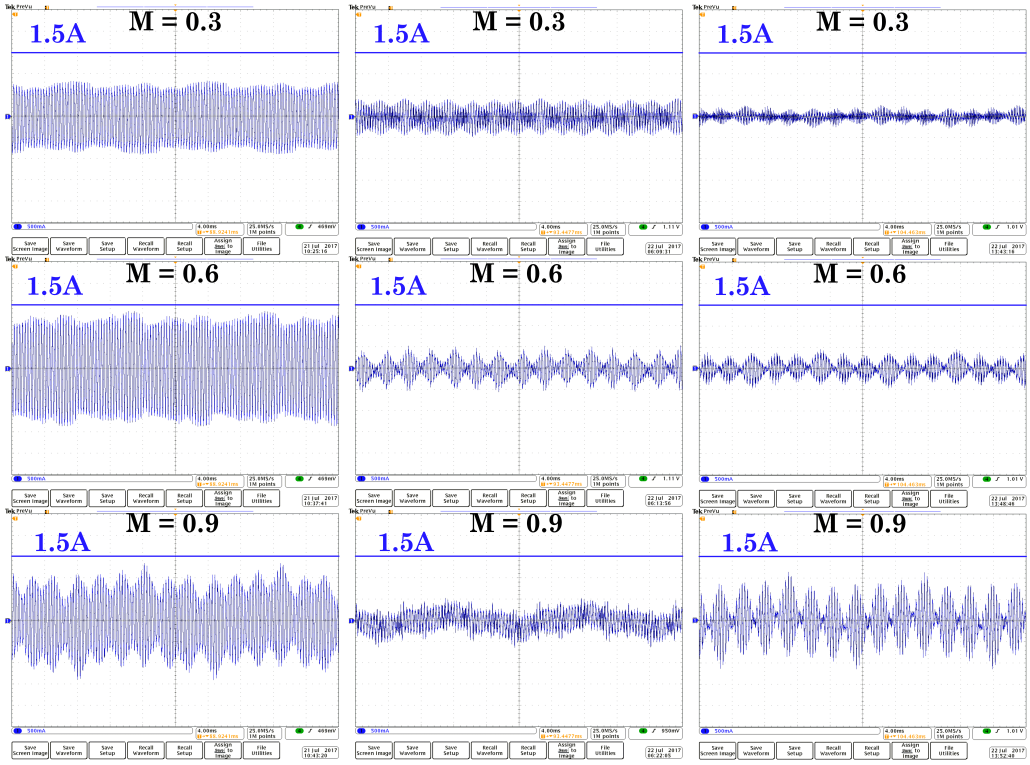


Figure 4.10. Measured CMCC waveforms under different modulation indices with (a) PD-S1DoF, (b) PD-S2DoF, (c) POD-S1DoF.

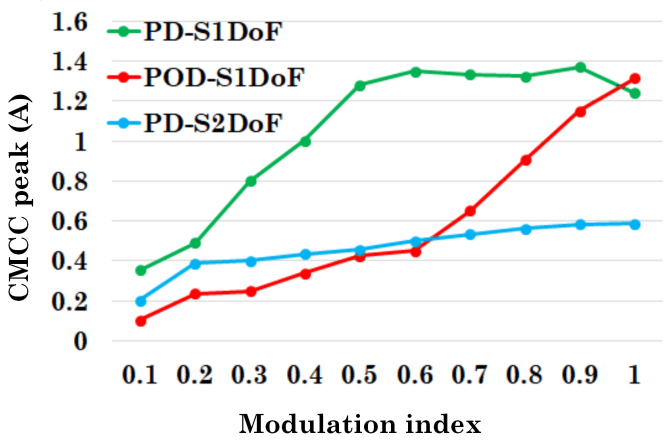


Figure 4.11. Comparison of the resultant CMCC peak values with different methods.

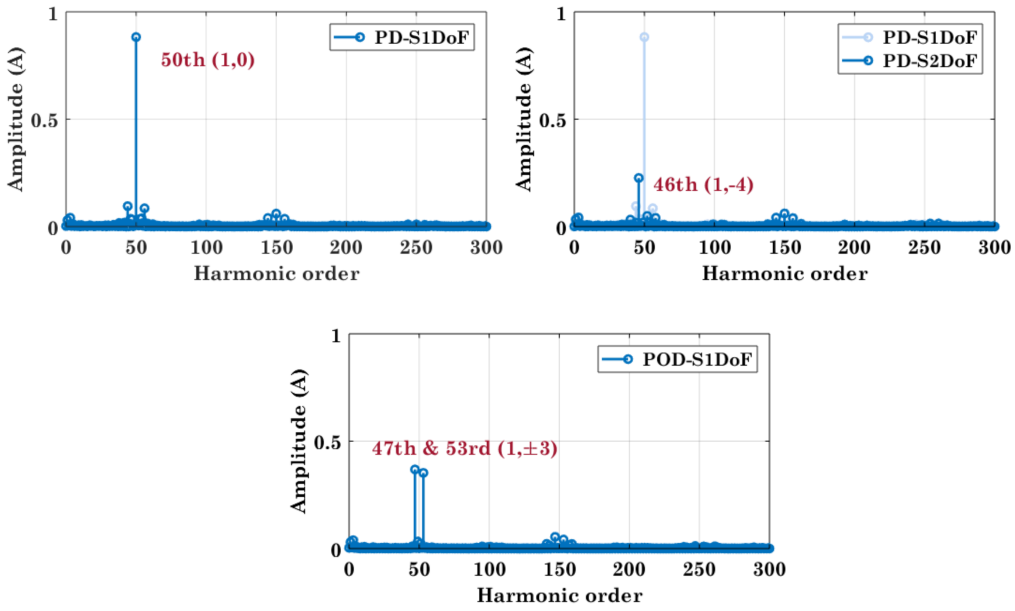


Figure 4.12. Harmonic spectrums of the measured CMCC when modulation index is 0.9.

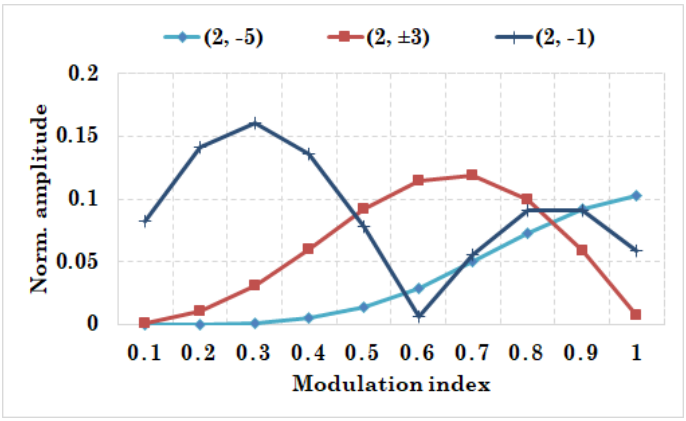


Figure 4.13. Calculated amplitudes of the harmonics with $m = 2$.

and (2, -1) replace the harmonics $(2, \pm 3)$ in the spectrum. Based on (2.17), the amplitudes of these harmonics in the line voltage can be calculated, as shown in **Fig. 4.13**. One can see that the amplitudes are in general comparable, meaning that the line voltage quality with PD-S2DoF scheme will also be comparable to that with PD-S1DoF. If the number of interleaved converters is multiples of 3, PD-S2DoF will have the same performance as PD-S1DoF in terms of line voltage quality, as they will have the same harmonic content. The performances of PD-S1DoF and POD-S1DoF will be different, but comparable.

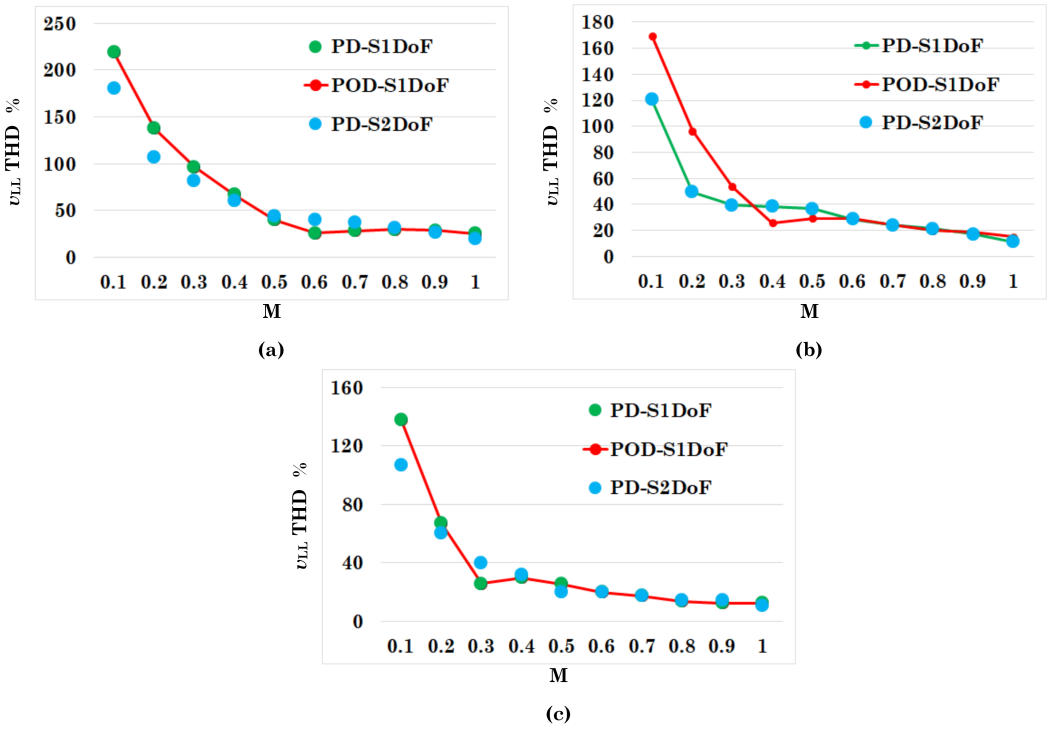
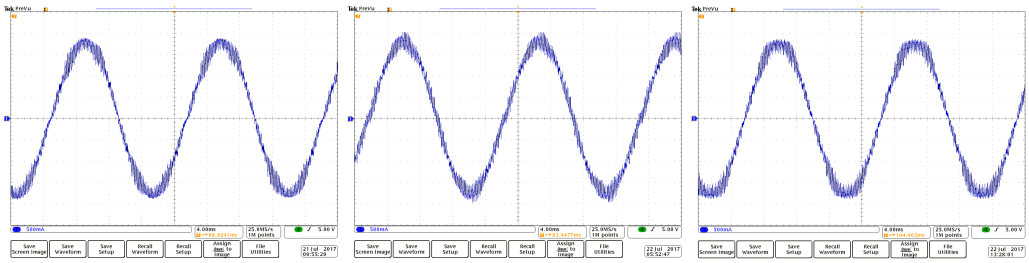


Figure 4.14. Simulation results of line voltage THD with (a) $N = 2$, (b) $N = 3$, and (c) $N = 4$.

Above analysis can be verified with the simulation results of line voltage THD as shown in **Fig. 4.14**. With $N = 2$ or 4, PD-S1DoF and POD-S1DoF deliver the same performance. With $N = 2$, PD-S2DoF scheme shows slightly better performance than the other two, especially in low modulation index range. With $N = 3$, PD-S1DoF and PD-S2DoF result in the same THD values, and both are better than POD-S1DoF in general.

The experimental waveforms of output current are shown in **Fig. 4.15**. As expected, the waveforms resultant from PD-S1DoF and POD-S1DoF are very similar. Comparison of the two methods in terms of output current THD is presented in **Fig. 4.16**. The result, showing good agreement with the simulation results, indicates that the PD-S2DoF scheme has better performance in low modulation index range, whereas PD-S1DoF (or POD-S1DoF) is better in mid modulation index range. In high modulation index, where grid-tied converters typically operate at, the three methods deliver similar performances.

The CM voltage issue can be evaluated in a similar way. Similar to the line



(a) (b) (c)

Figure 4.15. Measured output current with different modulation = 0.9, (a) PD-S1DoF, (b) PD-S2DoF, and (c) POD-S1DoF. Scale of all figures: 0.5A/div.

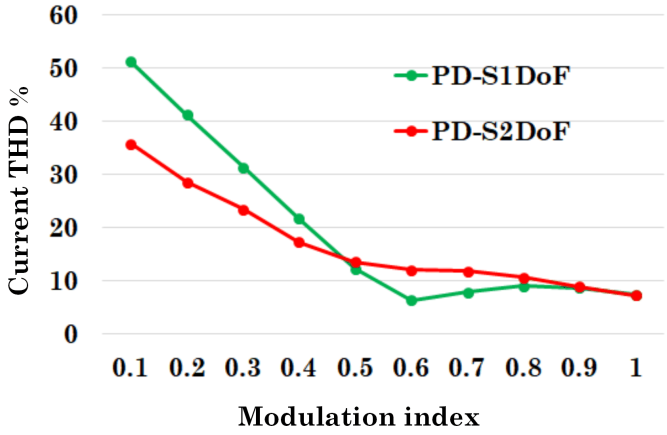


Figure 4.16. Comparison of the resultant output current THD values with different methods.

voltage, the CM voltage magnitude with PD-S1DoF and POD-S1DoF will be the same when N = even values, since the two schemes have the same CM voltage harmonic profile. With m = multiples of 3, PD-S1DoF and PD-S2DoF have the same CM voltage magnitude. The simulation results shown in **Fig. 4.17** verify the analysis and show that all three methods deliver comparable performances. Experimental results of the CM voltage magnitude are shown in **Fig. 4.18**, showing the same results as in simulation.

4.2.3 Performance with CMO Injection

Same as in 2L converters, CMO signal is usually injected to improve the DC voltage utilization ratio in the 3L converters [78]. The two most popular CMO signals for the 3L converters are introduced in Appendix B, section B.2. Their

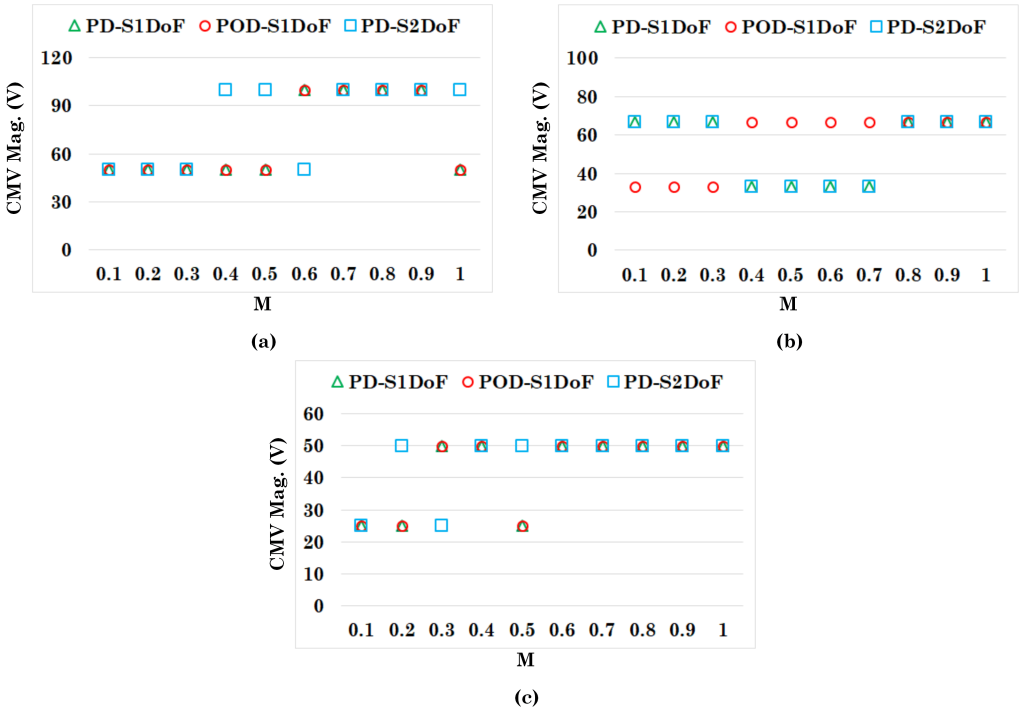


Figure 4.17. Simulation results of CM voltage magnitude with (a) $N = 2$, (b) $N = 3$, and (c) $N = 4$.

Figure 4.18. Comparison of the resultant CM voltage magnitude with different methods.

impact can be investigated analytically. However, the derivation of the analytical solution for the 3L converters is significantly more complicated than that for the 2L converters. As such, a simulation based comparative study has been carried out. The results for two interleaved 3L converters are shown below. For more converters, the comparison results in CMCC will not change much

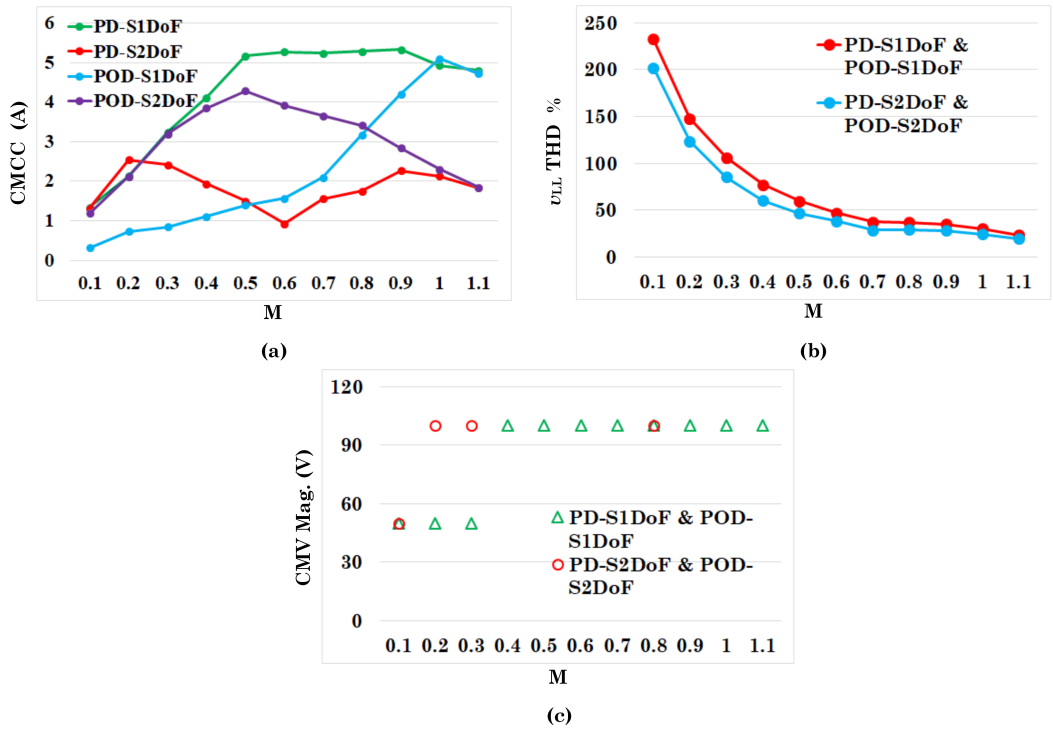


Figure 4.19. Performance comparisons of different methods when continuous type CMO is injected, (a) CMCC peak value, (b) output line voltage THD, and (c) CM voltage magnitude.

since the most dominant harmonics are already included in the case with two converters. Also, the performances of different methods in terms of output quality and CM voltage will also be comparable.

The performances of different methods with continuous type CMO are compared in **Fig. 4.19**. The results show that the proposed PD-S2DoF scheme also achieves the lowest CMCC maximum value. With discontinuous type CMO, the performances of different methods are compared in **Fig. 4.20**, which also verifies that the proposed PD-S2DoF is the best solution.

Further comparing **Fig. 4.19** and **Fig. 4.20**, one can see that the CMCC maximum values resultant from the two methods are close. However, the average device switching frequency is lower with the discontinuous type CMO. If the switching frequencies are the same, the discontinuous type CMO will result in even lower CMCC. Moreover, the output quality can be improved with the discontinuous type CMO. Based on above results, it is recommended to employ the discontinuous type CMO in practical applications.

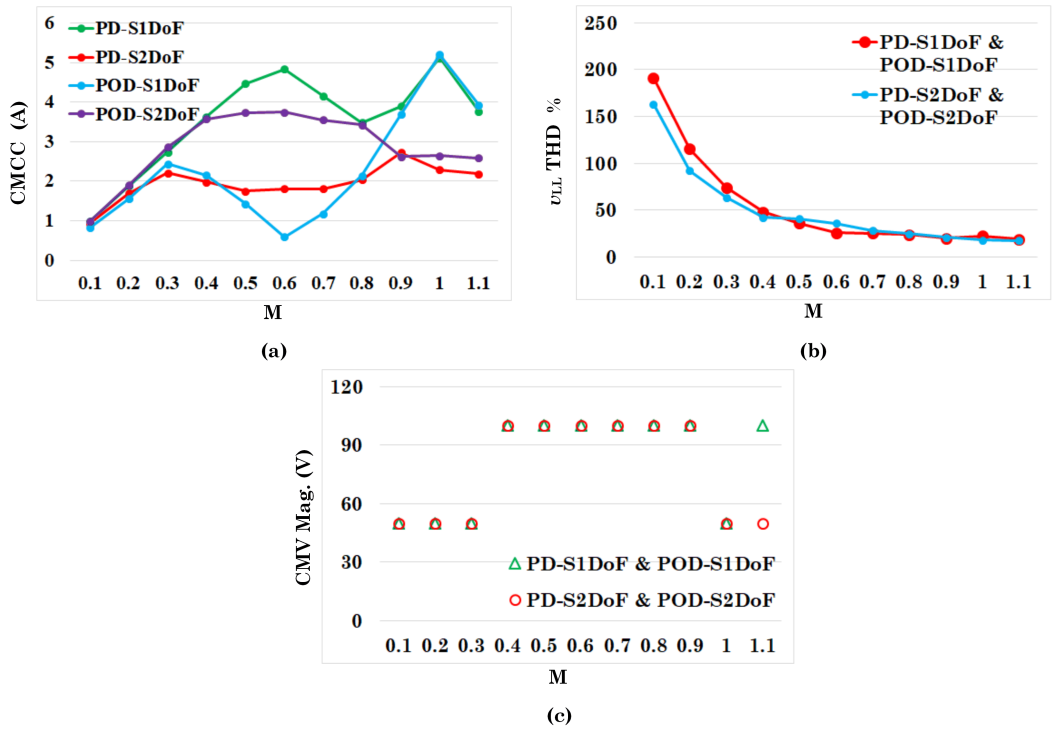


Figure 4.20. Performance comparisons of different methods when discontinuous type CMO is injected, (a) CMCC peak value, (b) output line voltage THD, and (c) CM voltage magnitude.

4.3 Generalization to High-Level Converters

The CMCC peak value reduction performance of the PD-S2DoF scheme can be generalized to higher-level converters. As explained in the harmonic distribution analysis in Chapter 2, the redistribution of DM and CM harmonics with the S2DoF interleaving scheme is applicable with any PWM methods. As such, the CMCC reduction performance of PD-S2DoF scheme should be valid for any high-level converters. Taking five-level (5L) modulation as an example, the harmonic spectra of the phase-leg voltage originated from PD based, POD based, and APOD based schemes are shown in **Fig. 4.21**, with unity modulation index. It can be seen that the dominant harmonic in PD based schemes is still at the order (1, 0), whereas $(1, \pm 3)$ and $(1, \pm 1)$ are the large harmonics in the spectrum with POD. The dominant harmonics of APOD locate at $(1, \pm 7)$, $(1, \pm 5)$, and $(1, \pm 1)$. Following the analysis in Chapter 2, the harmonic distributions with different methods can be readily obtained, and

harmonics with (m+n) is 0 or multiples of 3 will be distributed into the CM domain with S2DoF schemes. Same as in 3L PD-S2DoF scheme, the harmonic (1, 0) can be redistributed to the DM domain with 5L PD-S2DoF. With 5L POD-S2DoF, harmonic (1, -1) becomes part of the CMCC. With 5L APOD-S2DoF interleaving, the harmonics (1, -7), (1, -1), and (1, 5) will appear in the spectrum of CMCC, while with conventional APOD-S1DoF scheme, the CMCC will only include harmonics $(1, \pm 3)$.

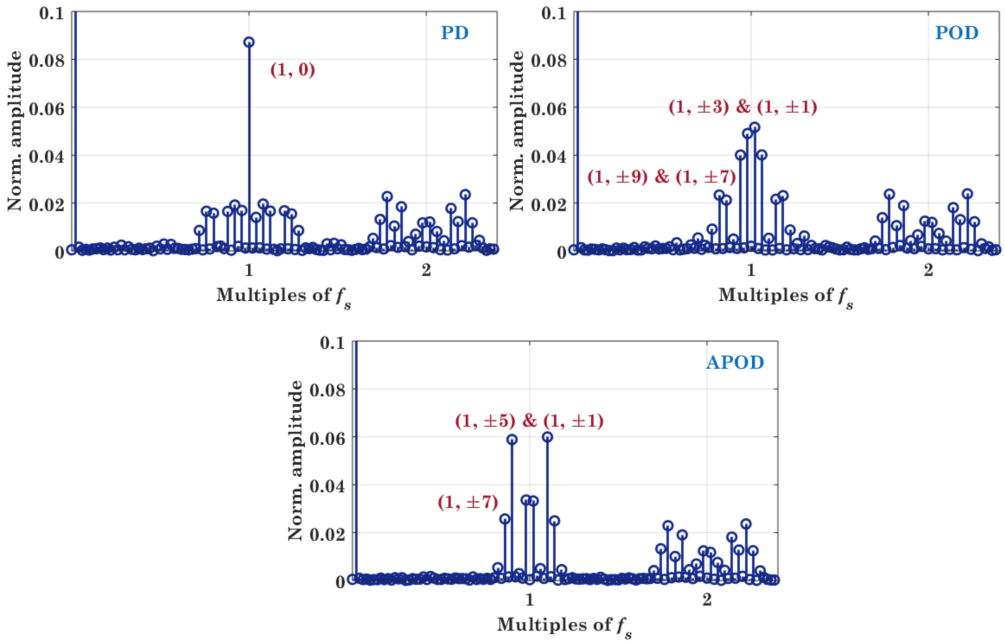


Figure 4.21. Harmonics originated from 5L schemes. The amplitudes are normalized to DC link voltage, and f_s is the carrier frequency.

Following the same analysis approach for the 3L converter, the amplitudes of these dominant harmonics can be compared, as shown in **Fig. 4.22**. As the dominant harmonics with PD-S2DoF are smaller than those in other methods within the entire modulation index range, the 5L PD-2DoF scheme should produce the lowest CMCC maximum peak value. The simulated results with different methods are compared in **Fig. 4.23**. As PD-S1DoF and POD-S1DoF apparently result in higher CMCC maximum values than the other, they are not included in the comparison. The comparison clearly shows that the PD-S2DoF scheme produces the lowest CMCC maximum peak, which well complies with the analysis. Since harmonics with $m = 1$ will always stay in

CMCC, PD-S2DoF will always yield the lowest CMCC regardless the number of converters.

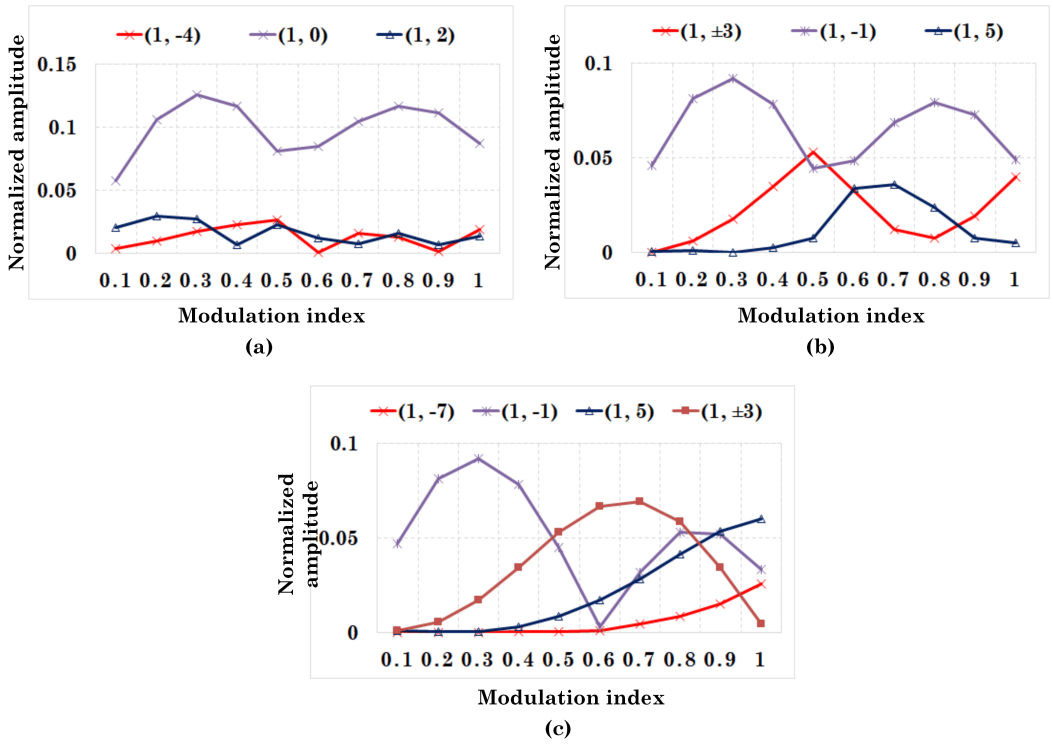


Figure 4.22. Amplitudes of the dominant harmonics produced by 5L schemes: (a) PD based, (b) POD based, and (c) APOD based. The amplitudes are normalized to DC link voltage.

Although the PD-S2DoF interleaving scheme has demonstrated superiority in CMCC reduction, it may not always be applicable for high-level converter (beyond 3L). Many high-level converters, e.g. the 5L ANPC converter and the flying capacitor (FC) converter, most likely will adopt PS-PWM for the sake of flying capacitor voltage balancing. In general, the PS-PWM results in a more even harmonic distribution in the DM and CM domains than the level-shift PWMs. As such, introducing the 2DoF interleaving to those converters may not bring further reduction of CMCC. For example, **Fig. 4.24** shows the comparison of CMCC peak values with 5L PS-1DoF and 5L PS-2DoF scheme based on the simulation parameters in **Table 4.1**. Note that symmetrical interleaving of PS-PWM does not provide any harmonic cancellation effect. Therefore, asymmetrical interleaving with $\theta_{int} = \pi/2$ is applied in

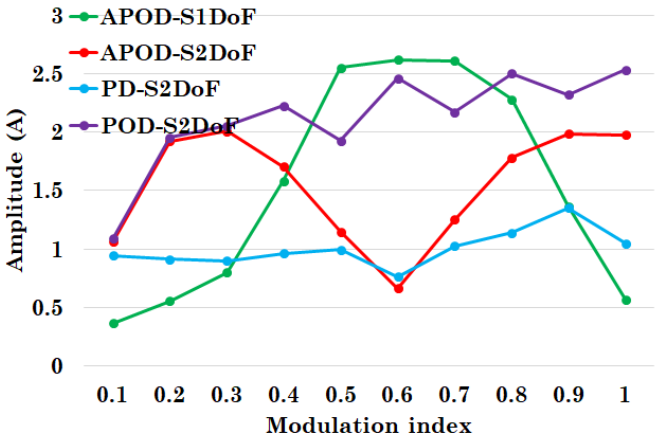


Figure 4.23. Comparison of simulated CMCC peak values with two interleaved 5L converters.

the simulation. The maximum CMCC peak value with the PS-2DoF scheme is only slightly lower than that with the PS-1DoF. Since the most dominant harmonics are already included in the CMCC with two interleaved converters, the performances of the two methods will still be similar when more converters are in parallel. Therefore, the PS-2DoF interleaving does not show obvious advantage over the conventional PS-1DoF scheme.

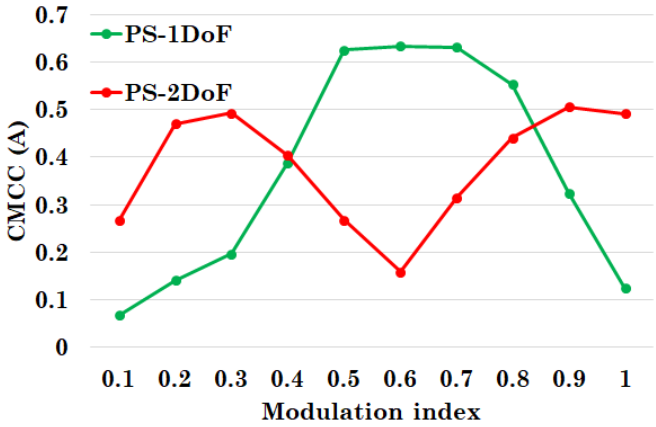


Figure 4.24. The resultant CMCC peak values from 2 interleaved 5L FC converter with PS-1DoF and PS-2DoF schemes.

4.4 Summary

This chapter investigates the application of S2DoF interleaving schemes in modular parallel multilevel converters. Analysis and results reveal that the PD-S2DoF scheme can minimize the CMCC peak value regardless the number of parallel converters. Compared to existing methods, more than 50% reduction in CMCC peak value can be achieved with the PD-S2DoF scheme. Because of its carrier-based nature, the PD-S2DoF scheme can be easily implemented in system with an arbitrary number of converters. More importantly, the proposed method delivers comparable performances in output quality and CM voltage magnitude when compared to existing methods. The promising performances of the S2DoF interleaving schemes for both 2L and multilevel converters open the opportunities to apply interleaving in modular parallel converters. In the next chapter, system level design of the modular parallel converter system with either 2L or multilevel converters will be investigated with the consideration of interleaving technique.

Chapter 5

L Filter based Modular Parallel Converter System Enabled by Interleaving

The previous chapters have demonstrated the superiority of 2DoF interleaving schemes for CMCC suppression. Particularly for interleaved 2L converters, the CMCC peak value has a negative correlation with the modulation index. As such, for system using CM choke in each converter module, the inductance, thereby the size, of the CM choke can be substantially reduced. Interleaving operation can thus be better implemented in the modular parallel converters. However, as discussed in Chapter 1, the resonance of the LCL filter at the output of each converter imposes several challenges to each individual converter and the entire system. In light of the increasing penetration of parallel converters in the utility grid, it is expected that more and severer filter resonance related issues may emerge. Also, eliminating the filter capacitors will also improve system reliability [79]. Therefore, it is necessary to rethink the system design to see if L filter is possible, and thus the filter resonance can be completely eliminated.

In this chapter, a new system design is proposed taking advantage of the modular parallel converter system and the interleaving technique. With a certain number of interleaved converters, only L filter should be sufficient to satisfy the grid code. This number can be found for different types of converters through an analytical study, which will be discussed in this chapter. Design

of parallel converters with separate DC links is presented in Appendix C.

5.1 Design Considerations of L Filtered Modular Parallel 2L VSCs

A parallel converter system with N 2L VSCs will be designed considering only L filter in each converter module. To find the minimum value of N that can satisfy the grid code, a generalized analysis without pre-defining system parameters is conducted. In the following subsections, I_{tt} is the total rms current at point of common coupling (PCC); ΔI_{pp} is the maximum peak-to-peak current ripple of each converter unit; K_{rp} is the ratio of ΔI_{pp} over the peak value of fundamental current of each converter unit; $I_{h,N}$ is the amplitude of the dominant high frequency harmonic current seen at PCC with N converters; $V_{h,N}$ is the amplitude of the dominant high frequency harmonic voltage seen at PCC with N converters; $Z_{rq,N}$ is the required filtering impedance to limit $I_{h,N}$ within the grid code; $L_{c,2L}$ is the filter inductance of each converter; $Z_{c,eq,2L}$ is the equivalent filtering impedance at PCC provided by N parallel converters; f_{cr} is the carrier frequency; f_s is the average device switching frequency; λ_N is the ratio of maximum $V_{h,N}$ over DC link voltage V_{DC} with different N and within a certain range of modulation index M.

The PCC current harmonic limits defined by the grid code IEEE519 (or IEEE1547) are listed in **Table 5.1** [80], where SCR is the short circuit ratio. Note that the limits are defined as the ratio of current harmonic amplitudes over the rated fundamental current amplitude. The limits set in the table are only valid for odd order harmonics. The even order harmonics are limited to 25% of the odd order harmonic limits. As can be seen from the grid code, the lower the SCR is, the stricter the limit is. In the worst case where SCR is lower than 20, the harmonics beyond 35th order must be lower than 0.3% of the rated current. For most 2L VSCs, the switching frequency is usually greater than the 35th order frequency (2.1kHz). Particularly when WBG devices are applied, the switching frequency can be up to hundreds of kilohertz. In addition, interleaving will push the dominant high frequency harmonics further

away from the fundamental frequency. Therefore, the harmonics over 35th order are mainly considered in the design. For applications where switching frequency is only a few hundreds hertz, the same analysis procedure can be carried out to find the proper design. On the other hand, the SCR is affected by the grid impedance, which usually varies over time. In the subsequent analysis, the grid impedance is not included, resulting in a conservative design, which is usually adopted in commercial products.

Table 5.1. Current harmonic limits defined by grid code.

SCR	**h<11**	**11≤h<17**	**17≤h<23**	**23≤h<35**	**35≤h**	**THD**
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20...50	7.0	3.5	2.5	1.0	0.5	8.0
50...100	10.0	4.5	4.0	1.5	0.7	12.0
100...1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

5.1.1 Converter Side Current Ripple with Interleaving

When multiple 2L VSCs are interleaved, the output current of each converter is dominated by the circulating current (CC). The value of ΔI_{pp} can be determined according to **Fig. 5.1**, where the ripple current waveform i_{ripple} within one switching cycle is illustrated. As circulating current is irrelevant to the load, no-load condition is assumed in **Fig. 5.1**. Note that only two converters are assumed with $Cr1$ and $Cr2$ being their carriers. Also, for 2L VSCs, the switching cycle period $T_s = 1/f_s = 1/f_{cr}$.

With sinusoidal reference, T_1 and T_2 can be given in (5.1) and (5.2), respectively, where ω_1 is the fundamental angular frequency. Based on **Fig. 5.1**, the peak-to-peak current ripple can be expressed in (5.3). It can be seen that ΔI_{pp} is a fixed value, which can be given as (5.4). Note that this result is also valid for other PWM strategies (e.g. various S2DoF schemes[1]) and system with more than two interleaved converters.

[1]With S2DoF schemes, the current ripple is determined by both DM and CM inductances, and thus is different from (5.4). However, such difference is negligible since only a small portion of harmonics appears in CMCC. In this case, the DM inductance can be used as $L_{c,2L}$ in calculation.

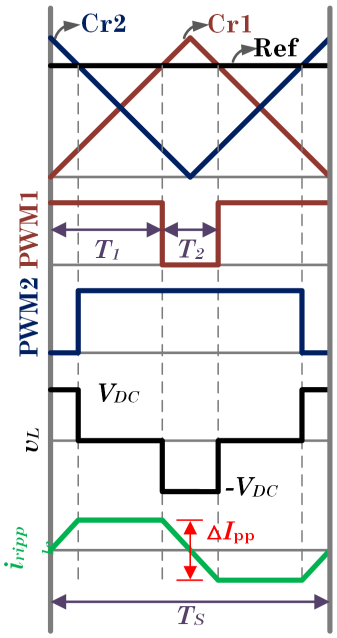


Figure 5.1. Illustration of the converter side current ripple in each converter when interleaving is applied. $N = 2$ is assumed.

$$T_1 = \frac{1}{2} T_s \left(M \sin\left(\omega_1 t\right) + 1 \right) \tag{5.1}$$

$$T_2 = \frac{1}{2} T_s \left(1 - M \sin\left(\omega_1 t\right) \right) \tag{5.2}$$

$$i_{ripple} = \frac{V_{DC} T_2}{2 L_{c,2L}} = \frac{V_{DC} T_s}{4 L_{c,2L}} \left(1 - M \sin\left(\omega_1 t\right) \right) \tag{5.3}$$

$$\Delta I_{pp} = \frac{V_{DC} T_s}{4 L_{c,2L}} = \frac{V_{DC}}{4 L_{c,2L} f_s} \tag{5.4}$$

5.1.2 Determination of N

In filter designs, the converter side current ripple ratio K_{rp} is usually adopted to define the allowed current ripple. This can be written in (5.5) for a modular parallel converter system with N 2L VSCs. As such, the filtering inductance of each converter can be given in (5.6). The equivalent filtering impedance at PCC can then be determined as written in (5.7).

$$\Delta I_{pp} = \frac{\sqrt{2} K_{rp} I_{tt}}{N} \tag{5.5}$$

$$L_{c,2L} = \frac{V_{DC} N}{4\sqrt{2} K_{rp} I_{tt} f_s} \tag{5.6}$$

$$Z_{c,eq,2L} = 2\pi f_s \frac{L_{c,2L}}{N} N = \frac{2\pi V_{DC} N}{4\sqrt{2} K_{rp} I_{tt}} \tag{5.7}$$

Without considering the grid impedance, to meet the grid code, $Z_{c,eq,2L}$ must satisfy (5.8), where $Z_{rq,N}$ can be given by (5.9). Substituting (5.7) and (5.9) into (5.8) gives the determination of the minimum N in (5.10).

$$Z_{c,eq,2L} \geq Z_{rq,N} \tag{5.8}$$

$$Z_{rq,N} = \frac{V_{h,N}}{I_{h,N}} = \frac{\lambda_N V_{DC}}{0.3\% \sqrt{2} I_{tt}} \tag{5.9}$$

$$N \geq \frac{4 K_{rp} \lambda_N}{2\pi \times 0.3\%} \approx 212.21 K_{rp} \lambda_N \tag{5.10}$$

It is interesting to see that N is irrelevant to the system parameter, e.g. V_{DC}, f_s, or I_{tt}. The value of K_{rp} is normally determined based on the requirement of conduction loss and the allowed filter inductor size. The higher K_{rp} is, the smaller filter inductor is, but the higher conduction loss will be. In most designs, the range of K_{rp} is usually within 50% to 20%. For λ_N, the DFI analysis can be carried out to find the maximum value for a given range of M. Two scenarios must be considered in the analysis as has been indicated in Chapter 1. **(1)** When each converter is equipped with a CM choke (the CM choke can also be placed at the DC side of each converter) (cf. **Fig. 5.2**), S2DoF interleaving scheme must be applied. **2)** If only three separate single-phase inductors are applied in each converter module (cf. **Fig. 5.3**), there is no need to suppress the CMCC, and therefore, S1DoF interleaving scheme can be adopted. The value of λ_N for both schemes are calculated in the following analysis. The selected range of M is from 0.3 to 1.1, considering the possible grid-sag and fault ride through condition.

Case 1: With CM choke in converter module In this case, the CS2DoF interleaving scheme should be selected. Based on the harmonic distribution analysis introduced in Chapter 2, harmonics with $m + n \neq 0$ or triplen values are distributed in the output voltage. The values of λ_N within the selected M range for different N can be summarized in **Table 5.2**.

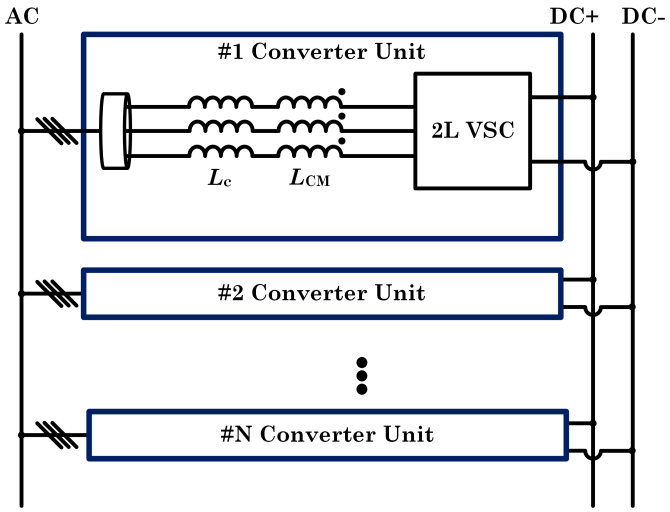


Figure 5.2. Structure of the modular parallel converter system with CM choke in each converter module.

Table 5.2. The values of λ_N with respect to N for CS2DoF scheme.

N	2	3	4	5	6
λ_N	0.196	0.0732	0.0982	0.0821	0.0565

Case 2: No CM choke in converter module In this case, CS1DoF can be applied. Harmonics with $n \neq 0$ or triplen values appear in the output voltage. Based on the DFI calculation, the values of λ_N for different N can be obtained in **Table 5.3**.

Table 5.3. The values of λ_N with respect to N for CS1DoF scheme.

N	2	3	4	5	6
λ_N	0.196	0.0732	0.0982	0.0439	0.0565

According to the results in **Table 5.2** and **Table 5.3**, the value of N can be determined based on (5.10). Assuming K_{rp} is 50%, which stands for the

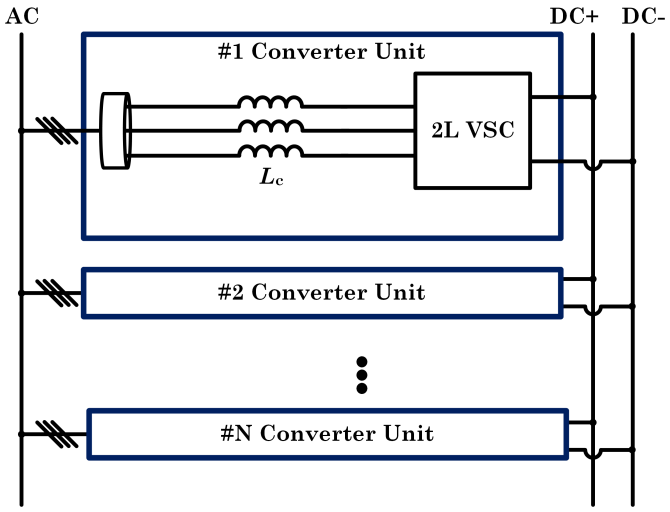


Figure 5.3. The modular parallel converter system when no CM choke is applied in each converter module.

minimum filtering inductance, N should be equal or higher than 6 for **case 1** in order to meet the grid code, and should be equal or higher than 5 for the **case 2**. However, as investigated in Chapter 3, odd value of N leads to an even-level output and increased CM voltage. Therefore, for both cases, N equals to or higher than 6 will be more desirable. On the other hand, the impact of K_{rp} is not significant. Assuming $K_{rp} = 20\%$, the required N is still 6 as $N = 4$ is insufficient to meet the grid code. As such, $N = 6$ as the next desirable value should be selected.

5.1.3 Filter Size Comparison with LCL Filter

The design of LCL filter for 2L VSC has been discussed in many literatures [81–84]. Basically, the converter side inductance $L_{c,LCL,2L}$ is first selected according to the requirement of K_{rp}. When the parallel converters are synchronized, the maximum converter side current ripple $\Delta I_{pp,LCL}$ is given by (5.11) [81]. As a result, $L_{c,LCL,2L}$ can be designed following (5.12).

$$\Delta I_{pp,LCL} = \frac{V_{DC}}{6L_{c,LCL,2L}f_s} \tag{5.11}$$

$$L_{c,LCL,2L} = \frac{V_{DC}N}{6\sqrt{2}K_{rp}I_{tt}f_s} \tag{5.12}$$

To minimize the total size of the LCL filter, the grid side inductance $L_{g,LCL,2L}$ is usually the same as the converter side inductance [82]. Therefore, the total inductance required in an LCL filter $L_{tt,LCL,2L}$ can be obtained as (5.13). Comparing to (5.6), it is clear that the LCL filter based design uses greater inductance than the L filter based design for the same K_{rp}. The ratio between $L_{c,2L}$ and $L_{tt,LCL,2L}$ is 0.75. Note that in practical applications, LCL filter with larger $L_{c,LCL,2L}$ and smaller $L_{g,LCL,2L}$ is normally adopted for the sake of stable control under various grid conditions. This results in even larger filter size than the proposed L filter based design.

$$L_{tt,LCL,2L} = \frac{V_{DC}N}{3\sqrt{2}K_{rp}I_{tt}f_s} \tag{5.13}$$

On the other hand, the volumes of the two designs can be compared based on the area product [85]. The area product of an inductor, A_p, is given by (5.14), where A_w is the winding area, A_c is the core cross sectional area, K_j is the winding current density, k_f is the filling factor of the winding area, and B_m is the maximum flux density. The relationship between the volume and area product of an inductor can be expressed in (5.15).

$$A_p = A_w A_c = \frac{LI^2}{K_j k_f B_m} \tag{5.14}$$

$$Vol \propto {A_p}^{3/4} \tag{5.15}$$

Given the same S, k_f, B_m, and I, the total volumes resultant from the two designs can be obtained as (5.16). Note that the inductance values are normalized to unity value L_b such that the total inductance of L filter based deign requires $1.5L_b$ in each converter module, and both inductors in an LCL filter will be equal to L_b. Consequently, the ratio of Vol_L over Vol_{LCL} can be calculated as 0.678, which suggests that the filter size of L filter based design results in filter size reduction by 32%. This also implies that the cost of filter can be lower with the proposed design. If further considering the filter capacitors, which are normally realized with bulky and costly film capacitor,

the size and cost reduction resultant from the proposed L filter based design can be even significant.

$$\begin{aligned} Vol_L &\propto (1.5L_b)^{3/4} \\ Vol_{LCL} &\propto 2{L_b}^{3/4} \end{aligned} \tag{5.16}$$

5.2 System Design with Multilevel VSCs

5.2.1 Circulating Current Scaling Law

With higher-level converter, circulating current (CC) will be lower given the same carrier frequency, since the voltage driving the CC becomes lower. The same conclusion can be made for the maximum value of CMCC. A general relationship between the maximum amplitude of CC or CMCC, and the number of converter levels can be given as (5.17), where V_{DC} is the DC link voltage, R_{sw} is the equivalent switching frequency ratio, f_s is the average switching frequency of each device, N_L is the number of converter levels, and L_f is the filter inductance. Note that L_f can be the CM inductance or 1/3 of single phase filer inductance for CMCC, or the DM filter inductance for CC.

$$MAX_{CC/CMCC} \propto \frac{V_{DC}}{R_{sw} * f_s \left(N_L - 1\right) L_f} \tag{5.17}$$

Based on (5.17), given the same filter and device switching frequency, the amplitudes of CMCC and CC are determined by R_{sw} and N_L, which are further defined by the topology of the converter. For example, the 5L ANPC converter results in $R_{sw} = 2$ and $N_L = 4$, whereas the 5L FC converter has $R_{sw} = 4$ and $N_L = 4$. As a result, the CMCC and CC produced by 5L ANPC will be twice of that with 5L FC converter, assuming the device switching frequencies are the same. This scaling law also reflects the scaling of the converter side current ripple since it is dominated by CC when converters are interleaved.

5.2.2 Required N for Multilevel Converters

Based on the scaling law of CC, (5.10) for the 2L VSC can be generalized to multilevel converters without considering the impact of grid impedance.

For example, N can be determined by (5.18) for 3L converters, and for 5L converters, the equation becomes (5.19). Note that (5.19) is applicable for both 5L FC and 5L ANPC converters. Although these two topologies have different R_{sw}, the average device switching frequency or carrier frequency is cancelled out in the final equation, leading to the same result.

$$N_{3L} \geq 424.43 K_{rp} \lambda_{N,3L} \tag{5.18}$$

$$N_{5L} \geq 848.83 K_{rp} \lambda_{N,5L} \tag{5.19}$$

Similar to the analysis for interleaved 2L VSCs, the values of λ_N for 3L and 5L VSCs can be obtained through calculation or simulation to determine the required N. The values are presented in **Table 5.4**. CMO injection is applied to obtain the values in **Table 5.4**. Also, two types of modulation schemes, i.e. PD-S1DoF and PD-S2DoF, are considered for 3L VSC. Whereas for the 5L VSCs, only PS-PWM is considered.

Table 5.4. The values of λ_N with respect to N for 3L and 5L VSCs.

N	2	3	4	5	6
$\lambda_{N,3L,PD-S1DoF}$	0.0913	0.0408	0.0365	0.0215	0.0233
$\lambda_{N,3L,PD-S2DoF}$	0.0893	0.0408	0.0350	0.0343	0.0233
$\lambda_{N,5L,PS-PWM}$	0.0380	0.0279	0.0181	0.0159	0.00727

Assuming K_{rp} is 50% for all types of converters, the required N can then be calculated.

- For 3L converters with PD-S1DoF scheme, $N_{3L,PD-S1DoF} = 5$.
- For 3L converters with PD-S2DoF scheme, $N_{3L,PD-S2DoF} = 6$.
- For 5L ANPC converters, $N_{5L,ANPC} = 6$.
- For 5L FC, $N_{5L,FC} = 6$.

It is interesting to see that the number of required converters does not necessarily decrease as the number of levels increases. The reason is that

when a high-level converter is adopted, the required filtering inductance can be reduced to achieve the same K_{rp} as in a low-level converter. Consequently, the equivalent filtering inductance seen by the grid is also reduced. On the other hand, for the same N, λ_N of a high-level converter is lower than that of a low-level converter. Such reduction in λ_N is approximately proportional to the number of levels. As a result, the required N for a high-level converter ends up at a similar value as that for a low-level converter.

5.3 Simulation Results

This section presents the simulation results to demonstrate the effectiveness of the proposed design. The control architecture of the modular parallel converters is first introduced. Afterwards, the comparative results with an LCL based benchmark design are presented and discussed.

5.3.1 Control of Interleaved Converters

The interleaving of the carriers can also be achieved through the conventional techniques for synchronizing parallel converters, e.g. communication channels, a centralized controller, or decentralized control techniques. These techniques have been extensively investigated in literature. For control of multiple interleaved converters, conventional approaches for parallel converters are still applicable. In this study, each converter is controlled individually. The control scheme of the jth converter is shown in **Fig. 5.4**. The references for the d-axis current and q-axis current can be determined by a centralized controller or a master converter, depending on the control architecture of the system. For this simulation, this high-level control is not included.

5.3.2 Comparative Results with LCL based Benchmark

To demonstrate the performance of the proposed design, a benchmark design for LCL filter reported in [86] is selected. The objective of the benchmark was to minimize the weight of the LCL filter of a 1.2MVA single 2L inverter product manufactured by ABB for the 50Hz system. For comparison with the proposed

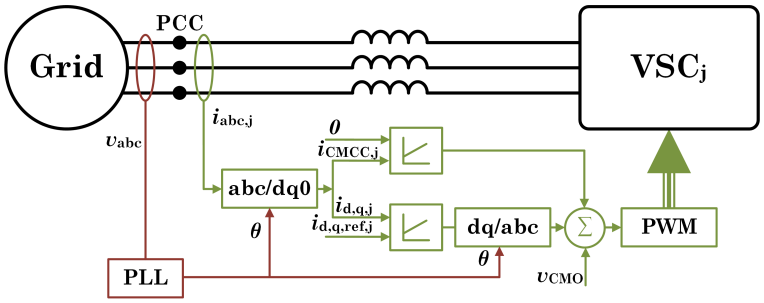


Figure 5.4. Control scheme of the jth converter of a L filter based modular parallel converter system.

interleaving based designs, this benchmark is split into 6 parallel 200kVA 2L VSCs and the filter parameters are scaled accordingly. The system parameters are shown in **Table 5.5**. Note that for the benchmark, both original and scaled designs are shown in the same column.

Table 5.5. System parameters for simulation.

Parameter	Benchmark	Interleave 2L	Interleave 3L
Line-to-line voltage		690V	
DC link voltage		1100V	
Rated total power		1.2MW	
Power factor		1.0	
Grid frequency		50Hz	
Carrier frequency		2600Hz	
K_{rp}		50%	
CM inductance	N/A	5mH	5mH
N	1/6 (scaled)	6	6
PWM strategy	SVPWM	CS2DoF	PD-S2DoF*
L_c	104uH/624uH	895uH	447uH
Filter capacitance	552uF/92uF	N/A	N/A
Grid side inductance	105uH/630uH	N/A	N/A
Total inductance**	209uH	150uH	75uH

* With CMO injection.
** At rated current of the total system.

With rated output, the simulated waveforms with the benchmark design are shown in **Fig. 5.5**. With LCL filter, the grid side current of each converter is free from switching harmonics. The total current injected into the grid is then the sum of the grid side currents of all converters. The harmonic spectrum of the total current under rated operation is shown in **Fig. 5.6**, where the

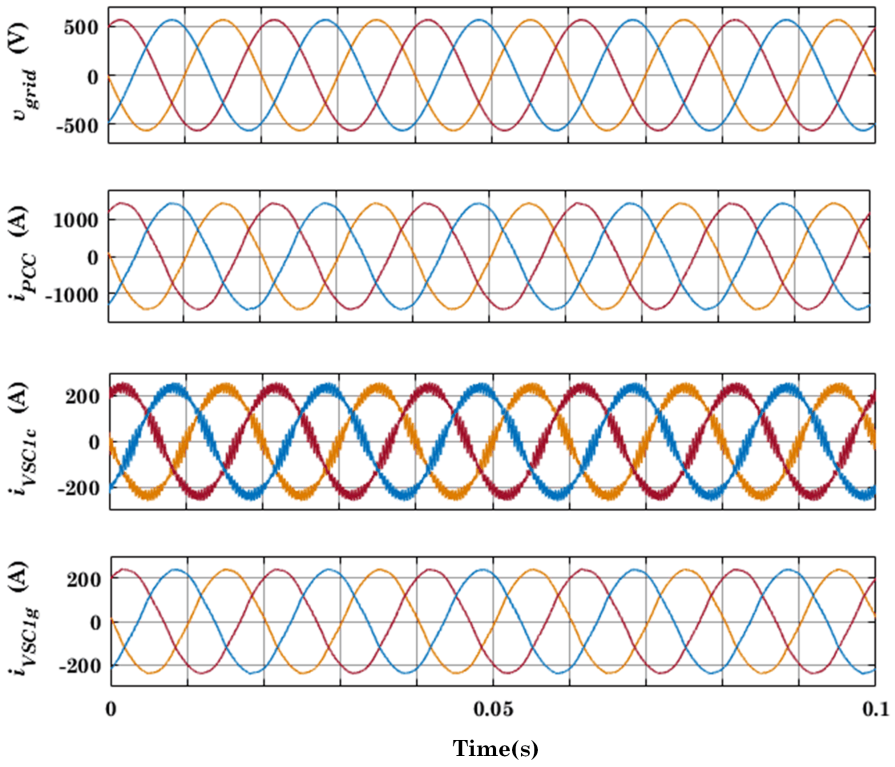


Figure 5.5. Simulated waveforms with the benchmark design. v_{grid} is the grid voltage. i_{PCC} is the total current injected into PCC. i_{VSC1c} and i_{VSC1g} denote the converter side and grid side currents, respectively, of converter 1.

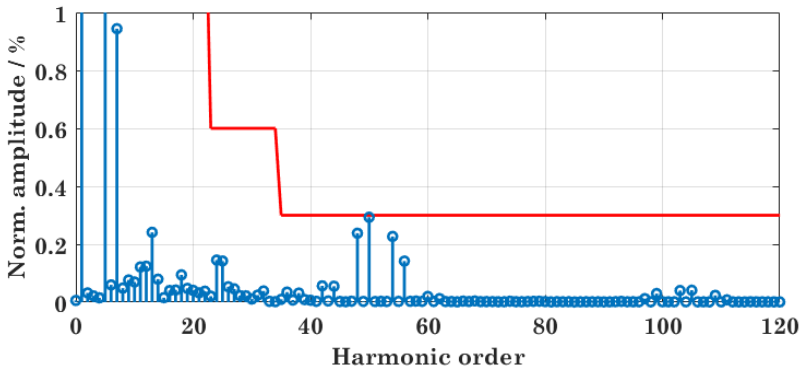


Figure 5.6. Harmonic spectrum of i_{PCC} resultant with the benchmark design. The red line indicates the limits of odd order harmonics set by grid code.

amplitudes of the harmonics are normalized to the fundamental current. As can be seen, the PCC current successfully meet the grid code, indicating the effectiveness of the benchmark design.

The simulation results with 6 interleaved 2L converters are shown in **Fig.**

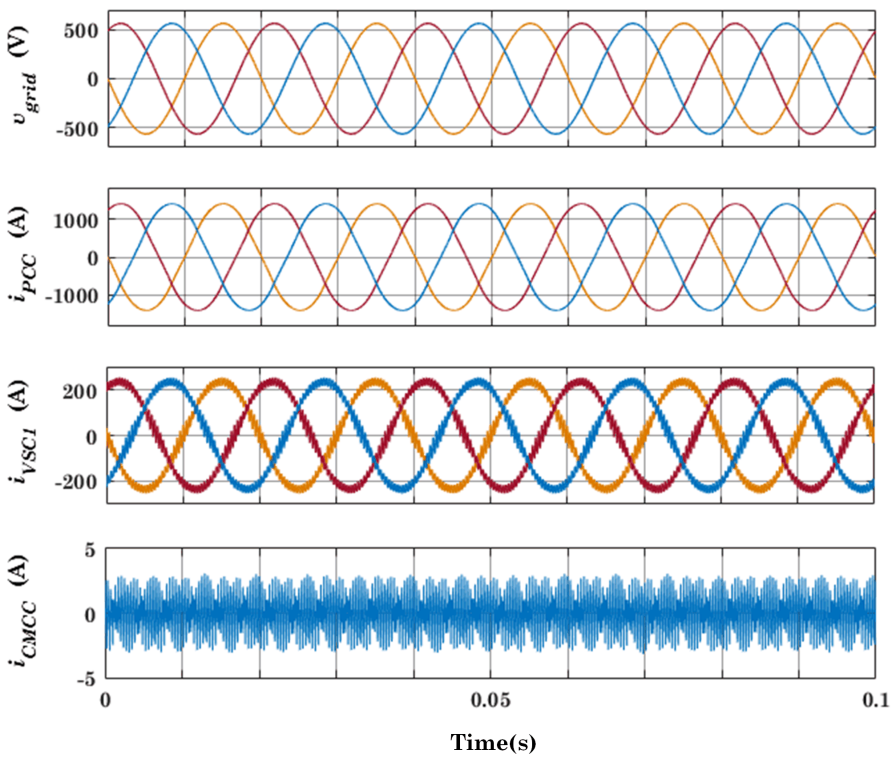


Figure 5.7. Simulated waveforms with 6 interleaved 2L converters modulated by CS2DoF scheme. v_{grid} is the grid voltage. i_{PCC} is the total current injected into PCC. i_{VSC1} is the output current of converter 1. i_{CMCC} is the CMCC measured from converter 1.

5.7 for the rated operation condition. As shown in the figure, the output current of one converter has obvious switching frequency ripples. However, the current flowing into PCC is clean. The harmonic spectrum of the PCC current is shown in **Fig. 5.8**, where one can see that the dominant switching frequency harmonics are pushed to the 6th order of the switching frequency. More importantly, the grid code is satisfied.

It should be noted that the output current ripple shown in i_{VSC1} is not at its maximum value when the modulation index is high in normal operation. However, when there is a grid-sag condition, the modulation index will drop to a lower value, and the current ripple will increase. **Fig. 5.9** shows the simulation results when the grid voltage drops by 70%. As has been analyzed in Chapter 3, the CMCC in this case is reduced such that the CM choke will not be saturated. Also, the output current ripple of individual converter

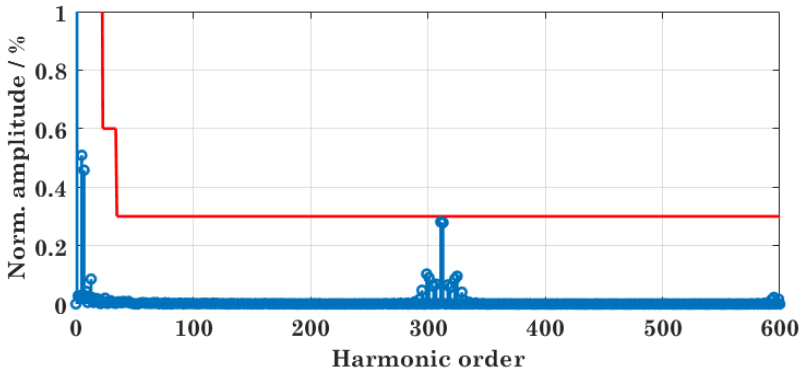


Figure 5.8. Harmonic spectrum of i_{PCC} resultant with 6 interleaved 2L converters and CS2DoF scheme. The red line indicates the limits of odd order harmonics set by grid code.

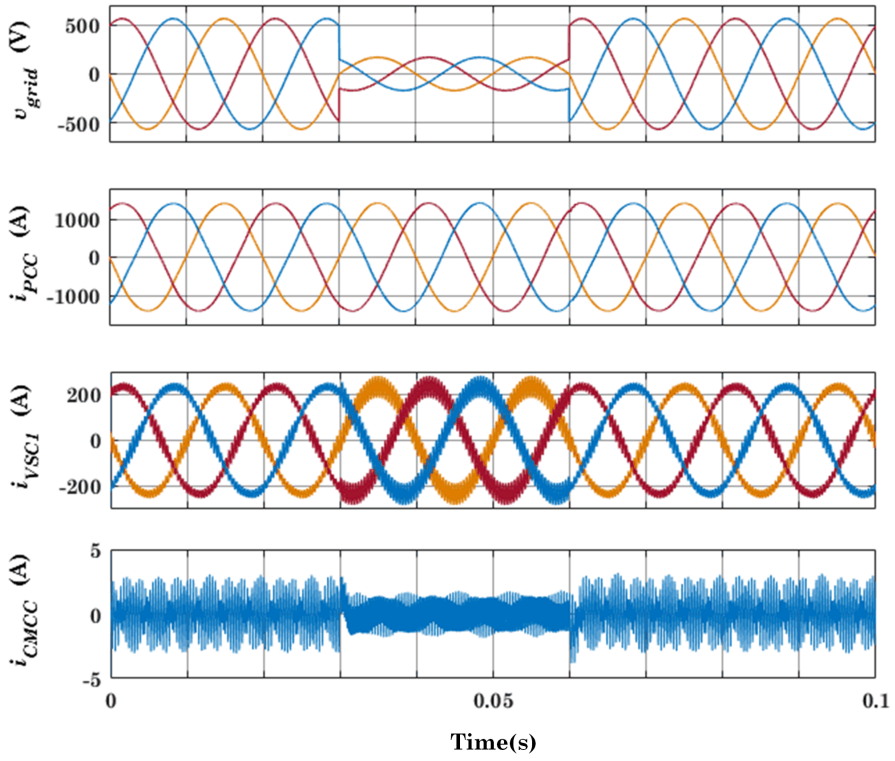


Figure 5.9. Simulation results of 6 interleaved 2L converters with CS2DoF scheme in grid voltage sag condition. v_{grid} is the grid voltage. i_{PCC} is the total current injected into PCC. i_{VSC1} is the output current of converter 1. i_{CMCC} is the CMCC measured from converter 1.

is increased. As K_{rp} is selected as 50%, the ripple component will be close to 50% in the grid voltage-sag condition. This also means that the actual converter ripple is less than 50% in normal operation condition, as shown in

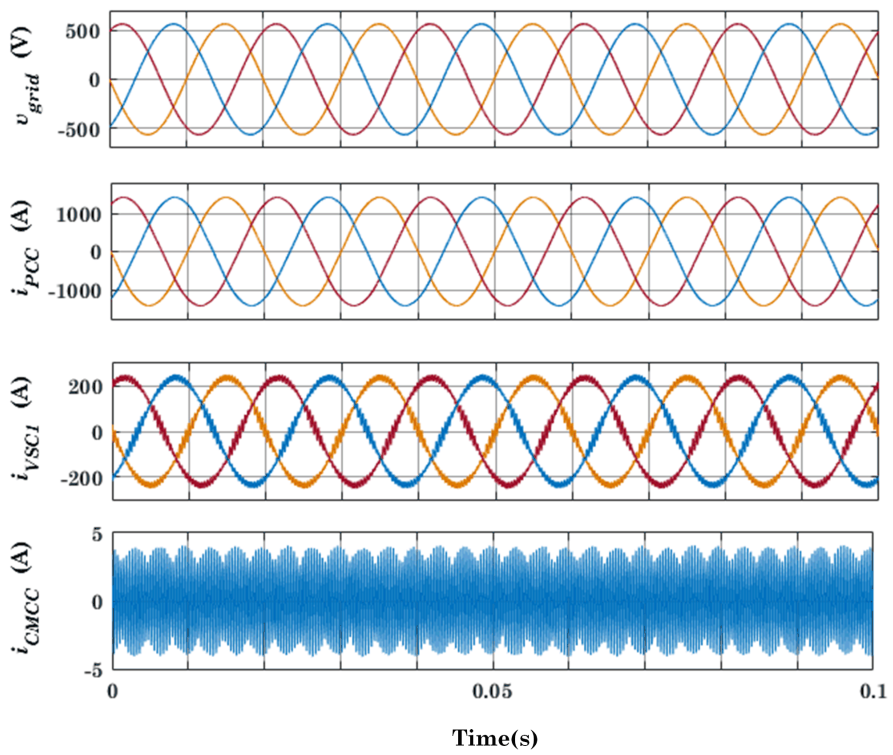


Figure 5.10. Simulation results of 6 interleaved 2L converters with CS1DoF in normal operation condition. v_{grid} is the grid voltage. i_{PCC} is the total current injected into PCC. i_{VSC1} is the output current of converter 1. i_{CMCC} is the CMCC measured in converter 1.

Fig. 5.9.

With the same system parameters, **Fig. 5.10** shows the simulated waveforms when 6 interleaved converters are modulated by CS1DoF scheme. Comparing **Fig. 5.9** to **Fig. 5.10**, one can see that in normal operation condition, the two schemes result in the same peak output current in each converter module, which also means the same conduction losses. As a result, using CS1DoF scheme with CM choke cannot actually reduce the size of the DM filter, otherwise the conduction loss will be increased. In grid voltage-sag condition, the peak current of each converter module will be smaller with CS1DoF as the larger harmonics will be processed by the CM choke. However, the voltage-sag duration is normally short and the overall converter loss and temperature rise will be negligible in such short time. On the other hand, the CM choke will be much larger if CS1DoF is used due to higher CMCC peak value.

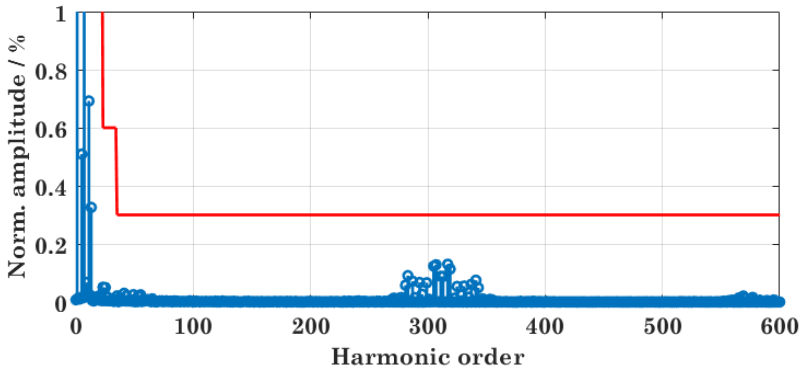


Figure 5.11. Harmonic spectrum of i_{PCC} resultant with 6 interleaved 3L converters. The red line indicates the limits of odd order harmonics set by grid code.

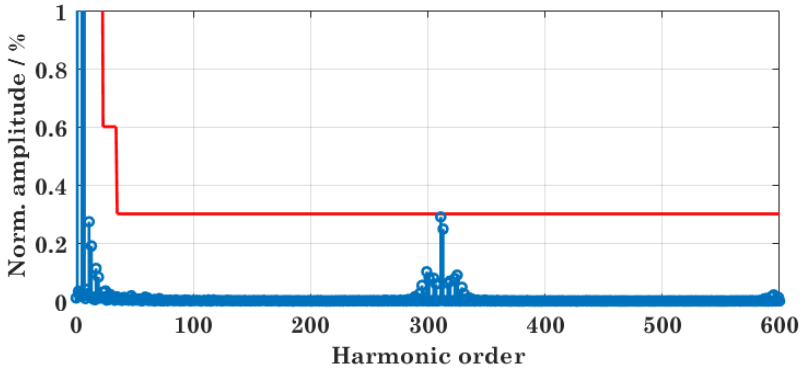


Figure 5.12. Harmonic spectrum of i_{PCC} resultant with 6 interleaved 3L converters and grid voltage at 350V. The red line indicates the limits of odd order harmonics set by grid code.

As for the 3L converters, the harmonic spectrum of the PCC current under normal operation condition is shown in **Fig. 5.11**, showing that the dominant harmonics are much lower than the limits in grid code. The reason is that the dominant harmonics in this case only reach their maximum amplitudes when modulation index is around 0.55. Therefore, to verify the design, simulation with grid voltage at 350V was carried out and the resultant PCC current spectrum is shown in **Fig. 5.12**. One can see that the magnitude of the dominant harmonic reaches closer to, but is still lower than, the limit, demonstrating the effectiveness of the proposed design.

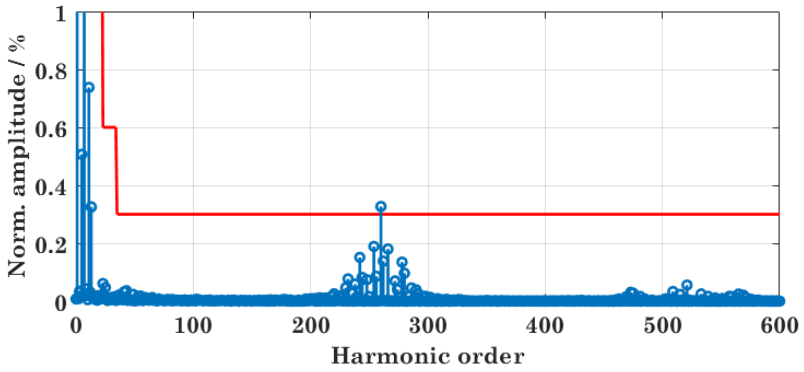


Figure 5.13. Harmonic spectrum of i_{PCC} resultant with 5 interleaved 3L converters modulated by PD-S2DoF scheme. The red line indicates the limits of odd order harmonics set by grid code.

5.3.3 Results with Different Schemes and N

To verify the analysis regarding the determination of N, designs with different N were also simulated. For a system with 5 interleaved 3L converters, the filter inductance for each converter, L_c, is 373uH if $K_{rp} = 50\%$. Based on the previous analysis and λ_N values in **Table 5.4**, system can only meet the grid code with PF-S1DoF. The spectra of PCC current with two schemes are shown in **Fig. 5.13** and **Fig. 5.14**, respectively. The results show good agreement with the analysis.

On the other hand, if the requirement on K_{rp} is 25% (i.e. $L_c = 596uH$), $N = 4$ will be sufficient to allow PD-S2DoF scheme to meet the grid code. Corresponding spectrum of the PCC current in this case is shown in **Fig. 5.15**, which indicates the effectiveness of the design.

5.4 Practical Considerations of the Proposed Design

The effectiveness of L filter based interleaving converter system has been verified through above analysis and simulation results. In this section, the practical applicability of the proposed design concept is discussed.

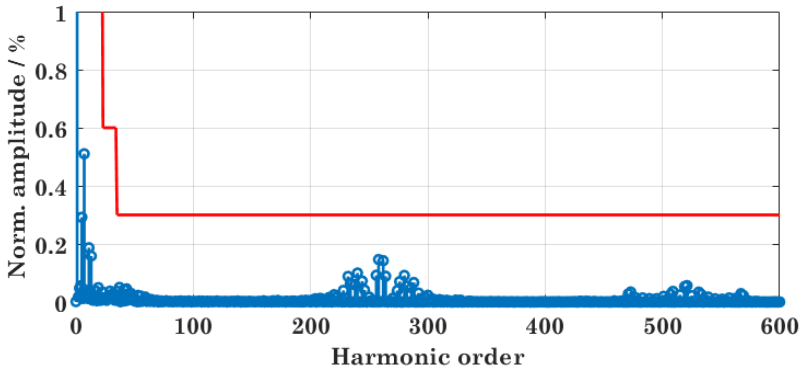


Figure 5.14. Harmonic spectrum of i_{PCC} resultant with 5 interleaved 3L converters modulated by PD-S1DoF scheme. The red line indicates the limits of odd order harmonics set by grid code.

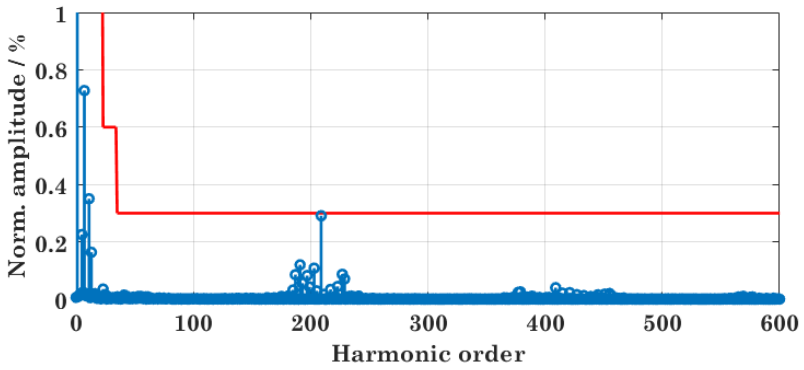


Figure 5.15. Harmonic spectrum of i_{PCC} resultant with 4 interleaved 3L converters modulated by PD-S2DoF scheme. $\lambda_N = 25\%$ is adopted in this case. The red line indicates the limits of odd order harmonics set by grid code.

5.4.1 Light Load Operation

Light load operation is a very normal condition for grid connected converters. In this condition, the output current is lower than the rated value. As such, it is anticipated that the ratio of the harmonic currents over fundamental current (herein defined as Γ) will exceed the limits set by the grid code. As earlier mentioned, the grid code is defined at the rated output current. That said, it is unnecessary to satisfy the grid code in light load condition. However, it is still necessary to examine the performances of both LCL filter based and L

filer based designs. Four operating schemes can be considered[2].

- $LCL1$ **scheme**: Single full power converter with an LCL filter.
- $LCL2$ **scheme**: Multiple parallel converters with unit shading scheme.
- $L1$ **scheme**: All converters are active with equal power sharing regardless the load condition.
- $L2$ **scheme**: Adjusting the number of active converters based on the load condition. The actual interleaving angle is determined by the number of active converters. When only 1 unit is active, adopt SVPWM as modulation scheme.

With $LCL1$ scheme, it is straightforward that Γ will scale with the fundamental current. Assuming $\Gamma_{LCL1} = 0.3\%$ when output current is at rated value, its scale can be given by (5.20), where ϵ is the percentage of actual output current, $I_{tt,act}$, over the rated value I_{tt}. Note that $L1$ scheme shows the same behaviour.

$$\Gamma_{LCL1} = \frac{0.3\%}{\epsilon} \quad \epsilon \in [0, 1] \tag{5.20}$$

With $LCL2$ scheme, the system operates with Q converters (equal power sharing) when the actual output power is between the range $[(Q-1)/Q, 1]$ of the rated total power. When the actual output power is lower falls outside of this range, one converter will be shut down to ensure that the other converters will still operate close to the rated condition. Note that, Q is a varying number in this case and $Q \leq N$. As rated output current of each converter can meet the grid code, in some operating points, e.g. $(Q-1)/Q$ of full load, the quality of the total PCC current can still satisfy the grid code if some of the converters are shut down while others are operating with rated output. But in other cases, i.e. one or some of the converters operate with light load, the

[2]For interleaved converters, another operating scheme is keeping all converters active whereas the power is not equally shared. Some converters can serve as high frequency active power filters. However, harmonics around multiple switching frequency may exceed the limits due to incomplete cancellation. Therefore, this scheme is not considered.

high frequency harmonics in the PCC current will exceed the limits. The scale of Γ can then be obtained as (5.21), where the range of ϵ, as a function of N, is also given.

$$\Gamma_{LCL2} = \frac{0.3\%}{\epsilon} \quad \epsilon \in [\frac{Q-1}{Q}, 1] \tag{5.21}$$

With $L2$ scheme, the scale of harmonics is more complicated. For a system designed with N converters, operating with only Q activated converters will not change the equivalent filter impedance seen by the PCC. Taking 2L converter as a example, the impedance at PCC, $Z_{c,eq,2L,Q}$ with Q activated converters can be expressed as (5.22), which is the same as that given by (5.7).

$$Z_{c,eq,2L,Q} = 2\pi f_s \frac{L_{c,2L}}{Q} Q = \frac{2\pi V_{DC} N}{4\sqrt{2} K_{rp} I_{tt}} \tag{5.22}$$

In addition, the magnitude of the dominant harmonic varies with Q, which can be found in **Table 5.6**. For clear presentation, Q and λ_Q are used here to indicate the varying number of active converters. Note that in this table, CS2DoF scheme is adopted for $Q \geq 2$ and SVM is adopted when $Q = 1$. Based on previous analysis, Γ in $L2$ scheme can be derived as (5.23).

Table 5.6. The values of λ_Q with different number of active converters.

Q	1	2	3	4	5	6
λ_Q	0.196	0.196	0.0732	0.0982	0.0821	0.0565

$$\Gamma_{L2} = \frac{4\lambda_Q K_{rp}}{2\pi N \epsilon} \quad \epsilon \in [0, 1] \tag{5.23}$$

The scale of harmonic with each operation scheme has been calculated as shown in **Fig. 5.16**, when $N = 6$ and $K_{rp} = 50\%$. Also in the figure, ***Output current level*** means the range of actual output current. The red pentagons indicate the simulated operating points with $L2$ scheme. In these cases, the line voltage is not at its rated value as these dominant harmonics reach their maximum magnitudes when modulation index is low. The results

of the simulated operating points, along with the calculated results, are also included in the figure, showing the good agreement.

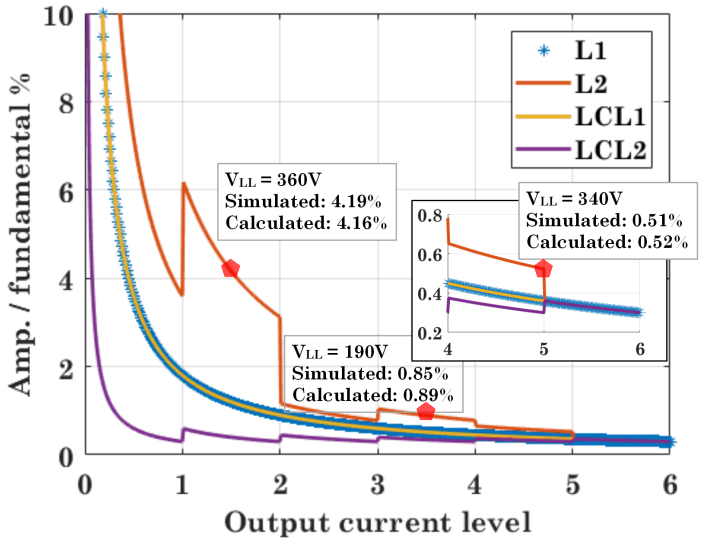


Figure 5.16. Scales of the switching frequency harmonics with respect to the actual fundamental output current with different operating schemes. The pentagons indicate the simulated operating points.

As can be seen from **Fig. 5.16**, the $LCL2$ scheme shows the best performance in terms of PCC current quality over then entire power range. In particular, the value of Γ can be kept within 1% until the actual output current is only 8% of the rated total current. The $LCL1$ scheme and $L1$ scheme have the same performance. Although both result in higher harmonics than the $LCL2$ scheme, their performances are close to that with $LCL2$ scheme when actual output current is higher than 50% of the rated current. On the other hand, the $L2$ scheme results in much higher harmonics when only 2 converters are active, though its performance can be close to that of the other schemes when there are 3 or more active converters. Note that **Fig. 5.16** corresponds the worst case where $K_{rp} = 50\%$. If smaller K_{rp} is selected, the performance of $L2$ scheme can be better. It is also worth noting that the grid code defines the amplitudes of harmonics as a ratio over the rated output current. In this regard, the scale of the harmonics can be illustrated in **Fig. 5.17**, indicating that the except the $L2$ scheme, the other three schemes all well comply with the grid code within all operation range. With $L2$ scheme, the increase of har-

monics in light load condition is not significant especially when the number of active converters is higher than 2.

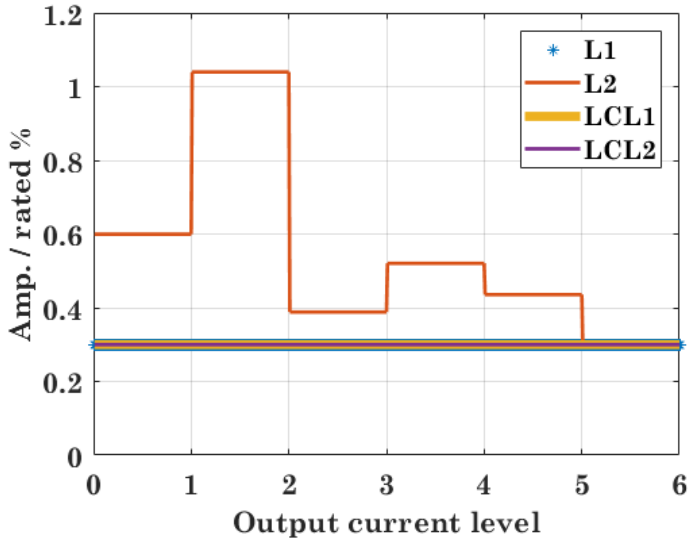


Figure 5.17. Scales of the harmonics around switching frequency in respect to the rated output current with different operating schemes.

In summary, the analysis in light load condition implies that replacing a single LCL filtered converter by multiple interleaved converters with only L filters can be a possible, and even optimal solution considering modularity, fault tolerance, control complexity, and light load operation.

5.4.2 System with Modular Parallel High-Level Converters

Based on the analysis in sections 5.1 and 5.2, adopting multilevel converters can significantly reduce the size of filters to achieve the same K_{rp} and PCC current quality. The reduction of filter inductance is basically proportional to the number of converter levels. That said, with parallel 5L converters, the filter inductance can be reduced by 50% as compared to that in parallel 3L converters. As such, adopting high-level converters will offer a great chance to increase the power density of the system.

On the other hand, it is also indicated in Section 5.2 that given the same K_{rp}, the required N for 5L converters is in fact the same as that for interleaved

3L converters. This means system with high-level converters will require significantly higher number of components, which possibly will undermine the reliability of the system. To design a system with parallel high-level converters, the reliability of the system must be taken into account.

Finally, from the perspective of multilevel converter topology, high-level converter based system is not technological ready yet. Although there are already a few decent 5L topologies reported in industry and academia, topologies with practical values are rarely seen beyond 5L (e.g. 7L, 9L, etc.). Therefore, the topological issues, as will be summarized in the next chapter, should also be addressed to enable practical implementation of modular parallel high-level converters.

5.5 Summary

In this chapter, a system level design, taking advantage of the L filter and interleaving technique, for the modular parallel converter system is proposed. Analysis is presented for different types of converters. As anticipated, when the number of the interleaved converters reaches a certain value, the total current of the system can meet the grid code with only L filter. It is found that the required number of converters is irrelevant to specific system parameters like switching frequency, rated power, or DC link voltage. Rather, it is only determined by the maximum harmonic amplitude after interleaving, which can be found analytically through DFI, and the converter side current ripple ratio K_{rp}, which can be tuned in the system design stage. It is also interesting to see that the required numbers of multilevel converters are similar or same as that for 2L converters, although multilevel converters will require less inductance. Practical design considerations, including the light load operation and concerns of multilevel converters, are also discussed in this chapter.

Chapter 6

Multilevel Converter Topologies with Internal Parallel Modularity

As discussed in the last chapter, connecting multilevel converters in parallel is a desirable choice to reduce the size of filter. However, with high device count of multilevel converter, system reliability may be undermined. In recent years, practical high-level (beyond 5L) converter topologies have been called for in both industry and academia. Yet, only a handful of them have found practical values. Moreover, modularity has not yet been realized in full DC link type multilevel converters. To provide a practical high-level topology synthesis approach and create modularity in multilevel converters, an internal parallel converter (IPC) concept is proposed in this chapter. It is identified that the parallel modularity can be created inside a converter by decoupling certain topologies into low switching frequency (LSF) stage and high switching frequency (HSF) stage. By only paralleling multiple HSF stages into one LSF stage, a new multilevel topology synthesis concept incorporating internal parallel modularity can be obtained. The main features of the IPC include reduced device current stress, improved reliability, fault tolerance, and modularity. It also allows the hybrid utilization of two types of devices in LSF stage and HSF modules respectively, making this concept particularly attractive to high speed devices like WBG devices and new Silicon MOSFETs. As these high speed devices tend to have much lower voltage and current ratings than

devices like IGBT, GTO or IGCT, hybrid device implementation (e.g. IGBT and WBG) will allow the emerging high speed devices bring their benefits to applications with higher power level. Interleaving operation of HSF modules is also applicable which can effectively mitigate the overvoltage and EMI issues induced by the use of high speed devices. In this thesis, two types of IPC topologies have been identified. One is called half-bridge based IPC (HB-IPC), while the other is flying capacitor based IPC (FC-IPC). The operation and features of the IPC topologies will be discussed in detail in this chapter.

6.1 Existing Topology Synthesis Principles

To search for new and practical topologies, the topological issues of existing topologies are first overviewed in this section. Depending on the synthesis approaches, existing topologies are classified into three categories. Note that these three principles are not exclusive from each other. Rather, they can be applied at the same time to derive a new topology.

6.1.1 Creating Levels through Additional DC Link Neutral Points

It is well known that by splitting DC link into multiple DC levels, multiple output voltage levels can be created. Examples of this topology synthesis approach includes the famous diode clamped converter and the active clamped converter, as shown in **Fig. 6.1** [87]. This principle is the most straightforward one. Also, PWM design of generalized ANPC is flexible. Hybrid utilization of low speed, e.g. IGBT, and high speed, e.g. WBG, devices is also allowed. However, a significant limitation is that when the number of neutral points (NP) is higher than two, it is difficult to achieve NP voltage balancing. This challenge can be addressed to some extent with certain control or modulation methods [88, 89], but still complicating the operation of the system. Alternatively, a balancing circuit can be applied to assist NP voltage balancing [90, 91]. However, these circuits must be rated at full power and usually process large amount power [90]. As such, the cost will be increased whereas efficiency

can be undermined. Due to the difficulty in NP voltage balancing, topologies with more than two NPs are rarely adopted in practical applications. It is worth mentioning that the four-level topology proposed in [92] adopts an additional flying capacitor (FC) to create a new current path to balance the NP voltages. Thus, the voltage of both NPs can be naturally balanced with PS-PWM. One limitation of this topology is that all devices are switched under PWM frequency. As such, hybrid utilization of different types of devices is not allowed. In addition, even-level topologies are usually less attractive as compared to odd-level ones since the CM voltage resultant from even-level PS-PWM is normally higher [93].

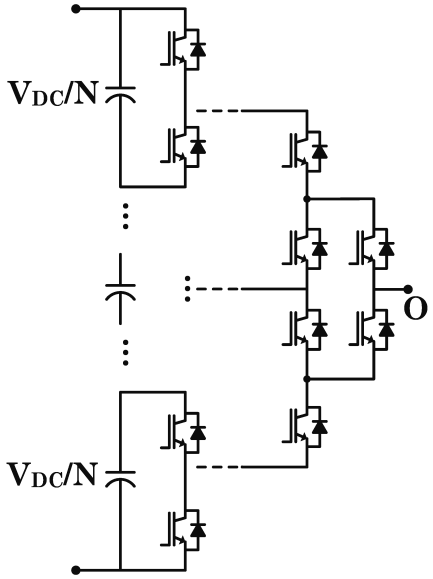


Figure 6.1. The generalized topology of active clamped converter.

6.1.2 Topology Generalization with Repeating Switch Cells

The second topology synthesis principle has been identified in [94], where derivations of many existing topologies are introduced. In general, a topology can be generalized by connecting more switch cells. For example, the flying capacitor based ANPC (FC-ANPC) converter [95] can be generalized in the way shown in **Fig. 6.2**. By opening circuit the output terminal of a low-level topology, and inserting a 2L switch cell, a high-level one can be

created. Similarly, the 5L stacked multicell converter (SMC), also known as nested neutral point polited (NNPP) converter, can be generalized as shown in **Fig. 6.3**. Following the same principle, the hybrid-clamped topology reported in [92] and [96] can be generalized as shown in **Fig. 6.4**. Although not shown here, the traditional FC converter can also be generalized in the same way.

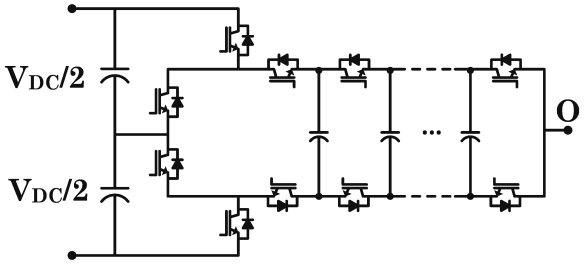


Figure 6.2. Synthesis of high-level FC-ANPC.

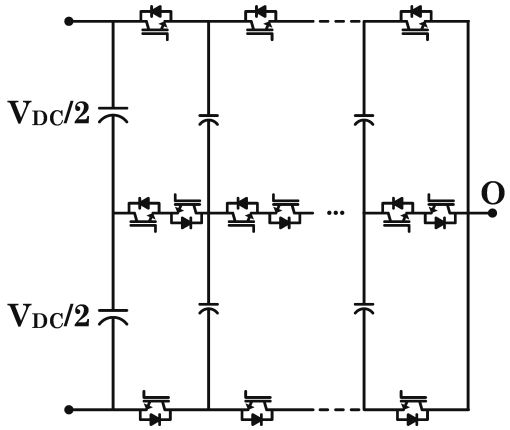


Figure 6.3. Synthesis of high-level SMC.

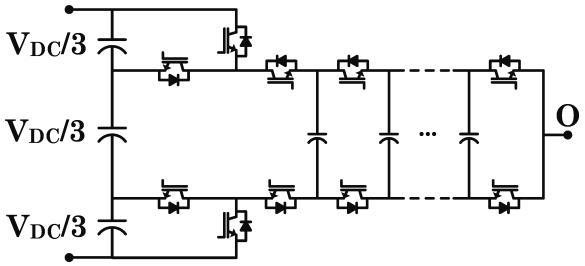


Figure 6.4. Synthesis of high-level hybrid-clamped topology.

By inserting more cells, the number of output levels can be effectively increased, whereas the device voltage stress can be reduced. With some topolo-

gies, e.g. FC-ANPC converter and FC converter, the voltages of the FCs can be naturally balanced through the PS-PWM. Therefore, a high-level FC-ANPC or FC converter will not face increased control burden, making them popular solutions for high speed devices like WBG and CoolMOS [97, 98]. On the other hand, some other topologies (e.g. SMC) require active balancing of the FC voltages. With multiple FCs in one phase, the balancing controls are coupled and complicated in these topologies. High bandwidth voltage sensing is also a challenging issue, making these topologies unsuitable for high switching frequency. Finally, the topology generalized with this principle are not modular, even though same switch cells are utilized.

6.1.3 Cascading H-bridge Building Blocks

The third popular method generates more levels by cascading H-bridge building blocks (HBBBs) at the output terminal of a base converter, as illustrated in **Fig. 6.5**. The base converter can be of any topology, e.g. 4L converter [99], 5L converter [100], or even MMC [101].

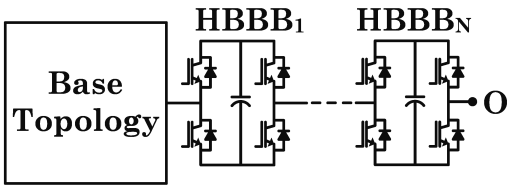


Figure 6.5. Generalized structure of the HBBB based topologies.

The HBBBs do not affect some of the basic features, e.g. device voltage stress and voltage balancing capability, of the base topology. The key performance of the generalized topology is mainly determined by the base converter. For example, if the NP voltage of the base converter can be balanced, the HBBB based version will also have such capability. The number of voltage levels can be increased following (6.1), where $N_{L,HBBB}$ is the number of output voltage levels, K_L is the level base topology, H is the number of cascaded HBBBs.

$$N_{L,HBBB} = 2^H(K_L - 1) \tag{6.1}$$

This method is component-efficient in generating more levels. Topologies with only one HBBB can be possible candidate for medium voltage applications. However, a number of limitations have to be considered when adopting HBBB based topologies, especially with high switching frequency.

- 1. Each HBBB has a different voltage rating, and hence the topology is not modular. If too many HBBBs are used, there may not be suitable semiconductors available. Therefore, in practical applications, it is neither realistic, nor necessary to cascade more than one HBBBs.

- 2. As all devices must switch at frequency higher than fundamental frequency, modulation of the base part and the HBBBs have to be coupled. Since the devices in the base topology are usually rated at higher voltage, the carrier frequency and deadtime must be selected based on these devices. This leads to poor utilization of the HBBB devices as they can actually be switched at much higher frequency. Particularly, this limitation will not allow the hybrid device selection, e.g. Silicon and WBG. Therefore, it is either full WBG design, which is costly, or full Silicon design, which has degraded performance

- 3. Most HBBB based topologies can achieve the natural balancing of FC voltage, however, at the expense of efficiency. To achieve natural balancing, the scheme in **Fig. 6.6** must be applied. The half bridge HB1 can be part of the base topology or the previous HBBB. With this scheme, the topology becomes equivalent to a FC converter. With phase shift PWM, natural balancing is achieved. But the four devices in HB1 and HB2 must be modulated as a single half bridge. That said, they have the same switching frequency. However, the voltage rating of HB1 is higher than (normally more than two times of) that of HB2. Switching them at the same frequency is apparently undesirable.

- 4. To balance the FC voltage, active balancing based on redundant switching states have to be adopted, making these topologies less attractive when higher switching frequency is desired. For high power

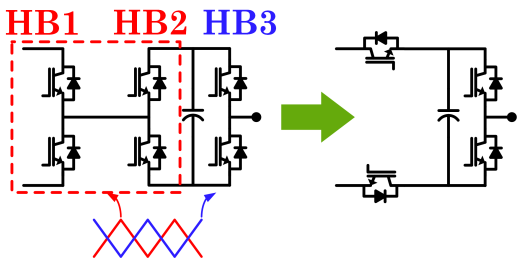


Figure 6.6. Modulation scheme for natural balancing of flying capacitor voltage balancing in HBBBs.

applications where switching frequency is low, it may be feasible, as accurate FC voltage sensing is achievable. However, if high switching frequency is adopted, e.g. when WBG devices are implemented, the HBBB based topologies become impractical, not only because it will increase the computational burden, but also because of the difficulty of accurate high bandwidth voltage sensing. In practice, the FC voltage must be acquired with Hall Effect sensor or isolated amplifier. High bandwidth Hall Effect sensor is bulky and costly, whereas high bandwidth isolated amplifier suffers poor accuracy and noise rejection ability.

- 5. Topologies with multiple FCs must address the coupled capacitor voltage balancing issue. For HBBB based topologies, this issue becomes more complicated as balancing of multiple FCs can only be achieved by properly selecting redundant switching states. However, multiple FCs will significantly increase the number of redundant switching states, and thus the PWM scheme design can be very complicated.

6.2 Basic Internal Parallel Topologies

The review over the existing topologies suggest that the commonly used three topology synthesis principles have various limitations. The high-level topologies derived with them are normally less attractive or impractical. A common limitation of existing topologies is the lack of modularity. Besides, they can only reduce the voltage stress over the devices, whereas current stress remains the same. For emerging high speed devices, whose current ratings are much

lower than existing high power devices like IGBT, the achievable power rating will be limited with existing topologies. Following the previous chapters, parallel connection of converters can effectively reduce device current stress and provide modularity. However, paralleling multilevel converters will significantly increase the device count, and therefore undermine system reliability. As such, topologies with reduced current stress and enhanced reliability are highly valuable.

To alleviate the reliability stress and at the same time leveraging the parallel modularity to reduce device current stress, the internal parallel converter (IPC) concept is proposed, by taking advantage of the topological decoupling feature of conventional 3L and 5L ANPC topologies. Based upon the IPC concept, two types of topologies, namely the half-bridge based IPC (HB-IPC) and the flying capacitor based IPC (FC-IPC), can be obtained. The basic embodiment of each type will be introduced in the following. The generalized topologies and the implementation of IPCs in multi-segment motors are introduced in Appendix D.

6.2.1 Half-Bridge based IPC

The 3L ANPC converter can be operated under several modulation schemes, among which, one scheme keeps the DC side four devices switching at fundamental frequency, while switch the AC output side two switches at high frequency. With this operating scheme, the HB-IPC can be derived from parallel 3L ANPC converters, as shown in **Fig. 6.7**, using two parallel 3L ANPC converters as an example. As can be seen, each 3L ANPC converter can be decoupled into two parts, a low switching frequency (LSF) part and a high switching frequency (HSF) part. When the output voltage is in positive half cycle, devices S_1 and S_3 of each converter will be turned-on, whereas S_2 and S_4 will be on during the negative cycle. As such, the voltage V_{XY} is always maintained at $V_{DC}/2$. Since the port voltage V_{XY} of the two converters are always buffered by the same DC link capacitors, the LSF parts of the two converters can be merged, leading to the HB-IPC topology with two HSF modules.

In practical applications, due to the presence of parasitic inductance be-

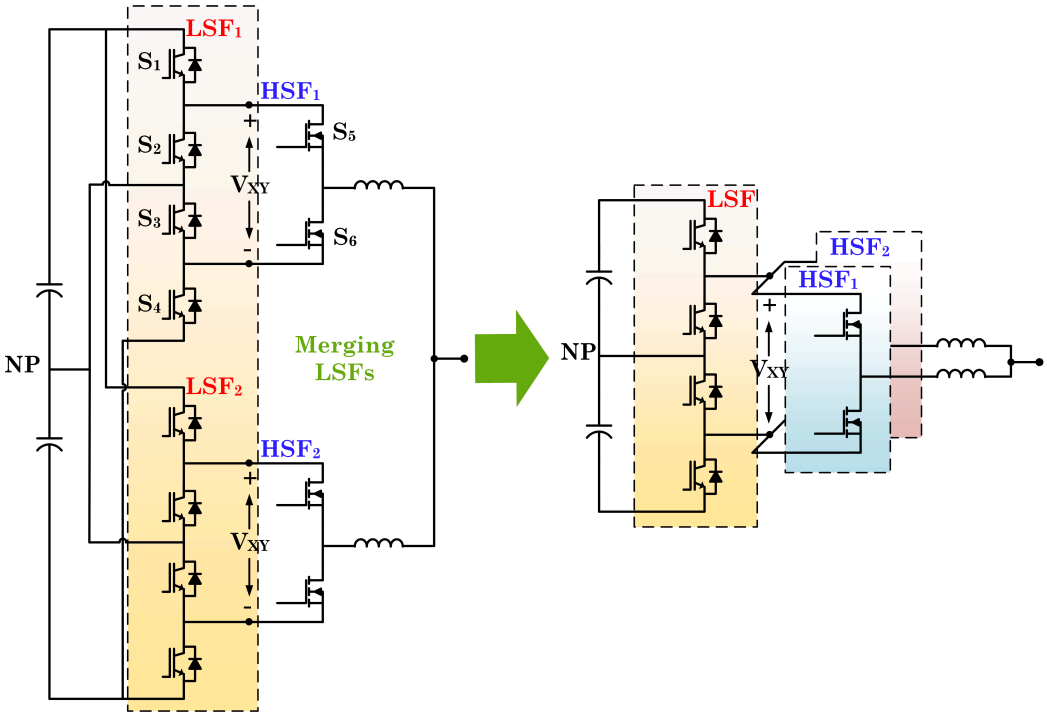


Figure 6.7. Derivation of the HB-IPC topology with two HSF modules.

tween the LSF part and the HSF modules, decoupling capacitors in each HSF module may be necessary to fully decouple the HSF modules from the LSF part. But with proper layout design, these decoupling capacitors may also be unnecessary. The basic HB-IPC topology can be formed as shown in **Fig. 6.8**. Note that only two HSF modules are shown in **Fig. 6.8**, but more can be paralleled if necessary. To prevent short circuit between the HSF modules, each HSF module should have an inductive filter. Similar to that in parallel converters, this filter will also suppress the circulating current between the HSF modules. Also, different types of filters, i.e. coupled inductor or single phase inductor, can be applied, as illustrated in **Fig. 6.8**.

The HSF modules can be synchronized to produce a 3L output voltage. Also, they can be interleaved to increase the number of output voltage levels. As an example, the interleaving operation of the HB-IPC with two HSF modules is shown in **Fig. 6.9**. After interleaving, the output voltage becomes a 5L one. The scale of the number of output voltage ($N_{L,HBIPC}$) as a function of the number of HSF modules (N_{HSF}) can be given in (6.2). Note that the

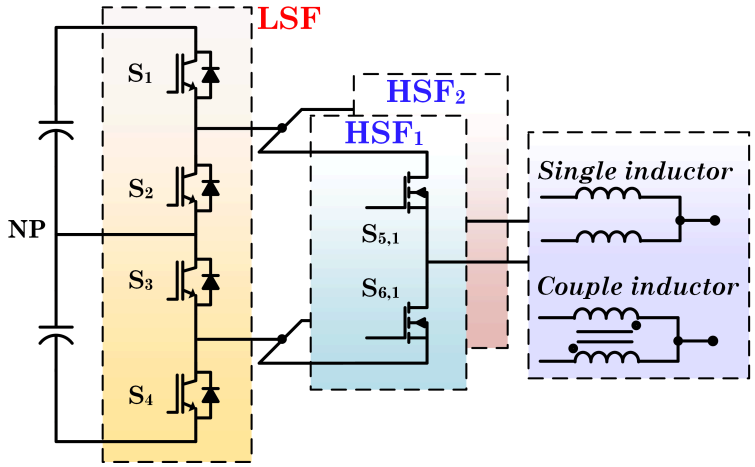


Figure 6.8. A basic embodiment of the HB-IPC topology with two HSF modules.

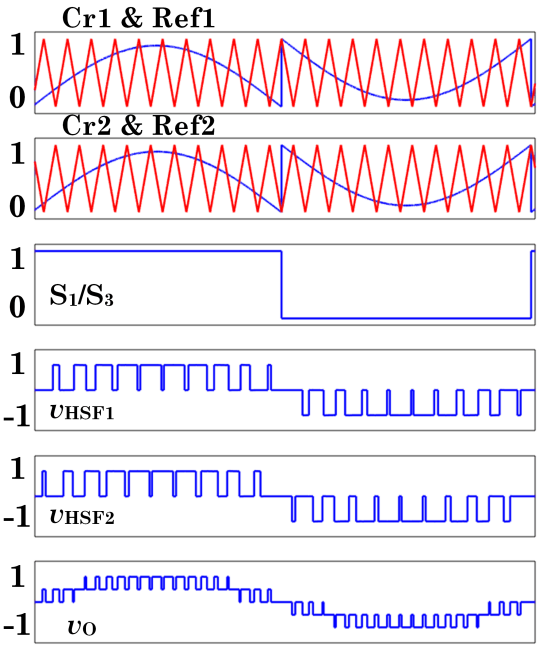


Figure 6.9. Example interleaved PWM schemes for the HB-IPC with two HSF modules.

interleaving angle for HB-IPC is $2\pi/N_{HSF}$.

$$N_{L,HBIPC} = 2(N_{HSF} + 1) - 1 \tag{6.2}$$

6.2.2 Flying Capacitor based IPC

The FC-IPC can be derived from parallel 5L ANPC converters in the same principle for the HB-IPC topology. Therefore, the derivation process is not included here. The basic topology of a FC-IPC with two HSF modules is the shown in **Fig. 6.10**. Again, coupled inductor or single phase inductor should be applied to prevent short circuit and suppress circulating current.

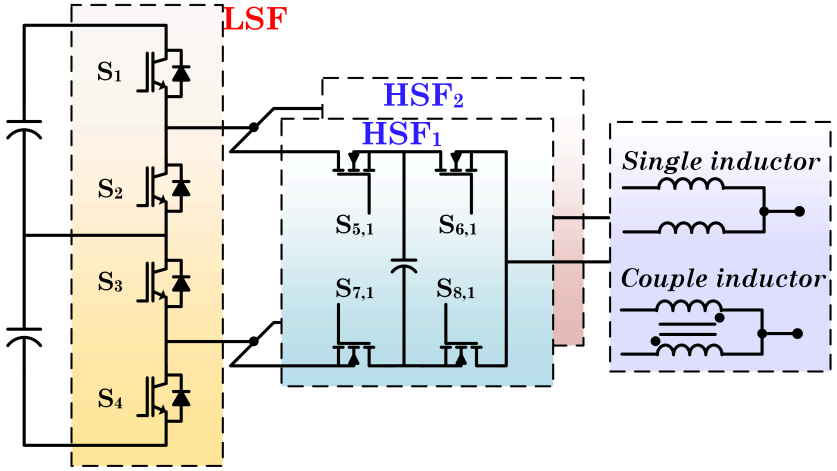


Figure 6.10. A basic embodiment of the FC-IPC topology with two HSF modules.

The HSF modules of a FC-IPC converter can also be synchronized or interleaved. If synchronized, the FC-IPC will output a 5L voltage. But with interleaving, the number of output voltage levels can be increased. In practical applications, each HSF module will normally be modulated by the PS-PWM to achieve natural FC voltage balancing[1]. As such, the interleaving angle of the FC-IPC should be π/N_{HSF}. Given two HSF modules, the example interleaving scheme is illustrated in **Fig. 6.11**, showing a 9L output voltage. Also, since PS-PWM is applied in FC-IPC, the multilevel 2DoF interleaving scheme will not have significant performance improvement, as discussed in Chapter 4. The scaling law of the FC-IPC is given by (6.3).

$$N_{L,FCIPC} = 4N_{HSF} + 1 \tag{6.3}$$

[1]For interleaving operation, the PS-PWM is more desirable since the resultant harmonics from interleaved PS-PWM are the same or similar as that from interleaved PD-PWM.

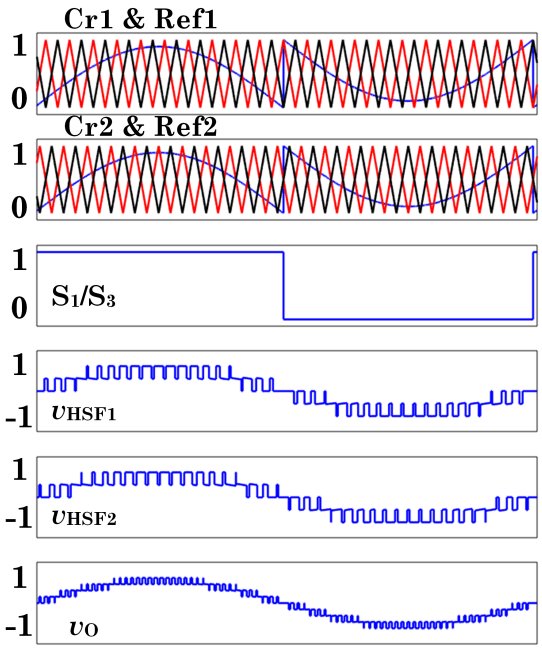


Figure 6.11. Example interleaved PWM schemes for the FC-IPC with two HSF modules.

A key feature of the FC-IPC is that the FC voltage balancing is simple, which can be reflected in twofold. First, the FC voltage of each HSF module can be balanced naturally with PS-PWM. More importantly, even if active balancing is preferred, there is no need to adopt redundant switching state based PWM scheme. On the contrary, control based balancing scheme can be applied [96] without the need of high bandwidth FC voltage sensing, and thus is still practical for high switching frequency occasions. Secondly, the FCs in different HSF modules are decoupled with each other. That said, the balancing of the FC voltage in one HSF module does not require the voltage information of another HSF module. This brings significantly reduced computational burden as compared to existing topologies with multiple FCs.

6.3 Key Features of the IPC Topologies

6.3.1 Flexible Device Selection

Device selection for IPC is flexible. Due to the decoupling of LSF part and HSF modules, the IPCs allow the hybrid use of two type of devices, which is particularly attractive for low voltage high power applications like string and solar inverter, and electric vehicle drive. In such applications, high speed low current devices can be applied in HSF modules, while LSF part can be realized with IGBT. If WBG devices are chosen as HSF devices, the total cost of the system can be reduced as compared to the full WBG design [102].

For high power applications like multi-MW wind power generation, the LSF part can be built with devices like gate turnoff thyristors (GTO) or integrated gate-commutated thyristors (IGCT), whereas the HSF modules can be built by insulated-gate bipolar transistor (IGBT) [103]. Since that GTO and IGCT can handle higher current than IGBT, the total current rating of the HSF modules can be matched with the rating of LSF part with the IPC topologies. As such, total power capacity can be increased effectively.

6.3.2 Potential Efficiency Improvement Opportunities

Possible efficiency improvement is considered from several aspects. Reduction of total switching losses of high speed devices is the primary potential. Light load efficiency improvement is also available if the HSF modules are not coupled. Flying capacitor loss reduction is another possible benefit.

Reduction of total switching losses With parallel connection of HSF modules, there is an opportunity to reduce the total switching losses of the high speed devices like WBG and CoolMOS [29]. It is straightforward that devices with lower current rating will have smaller silicon area and lower parasitic capacitances. As such, capacitive switching losses will be lower. In addition, assuming same switching frequency and same switching speed, the total switching energy of N HSF modules (each with $1/N$ current rating) is approximately $1/N$ of that with single full current HSF module, as the overlap period of voltage and current is reduced [104].

In practical designs, the gate resistors can be tuned according to the switching loss budget. However, when the HSF module is realized with high speed WBG devices or new Si Mosfets, e.g. CoolMOS, the dv/dt issue should also be taken into account. As such, same gate resistors are usually selected regardless the current ratings, as these devices already switch fast enough and reducing the gate resistance could lead aggravated dv/dt issue. Particularly for medium and high power applications, increasing switching speed for high current device will introduce additional design challenges caused by EMI and ringing effect. As such, the total switching energy of several low current devices will be much lower than that from a high current device, under the same condition. As an example, two GaN devices, GS661508T (650V/30A) and GS661516T (650V/60A) from GaN Systems are compared. The experimental results of the switching energy of two separately driven GS661508T devices and one GS661516T are illustrated in **Fig. 6.12**. The drain-source voltage is 400V, and turn-on and turn-off gate resistances are 10Ω and 2Ω, respectively. The total switching energy of two separately driven GS661508T is approximately half of that of one GS661516T. Therefore, the total switching losses can be reduced significantly. This also implies that switching frequency can be increased without undermining efficiency. Note that the total conduction losses of two cases are the same.

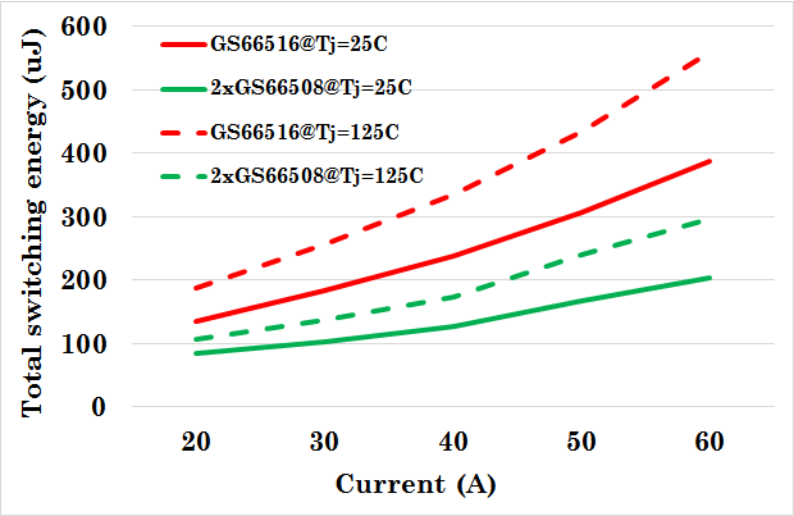


Figure 6.12. Switching energy comparison of two GaN HEMTs from GaN Systems.

On the other hand, for IGBTs, especially the high power IGBTs, gate resistors are usually selected based on device's current rating. Usually smaller resistance will be used for device with higher current rating. As such, the total switching loss reduction will not be as significant as in high speed devices. The efficiency improvement from the parallel connection of HSF modules may not be available when using IGBTs as HSF devices. However, in high power applications, the HSFs are most likely to be un-coupled, and light load efficiency improvement can be obtained by shutting down one or more HSF modules.

As for LSF part, their switching losses are negligible, thus it is unnecessary to put them in parallel. Together with the necessity of parallel connection of HSF modules, the IPC concept becomes a reasonable choice.

Reduction of total FC losses In practical applications, FCs are normally built with film capacitors. To improve reliability, a FC bank is usually realized with only one film capacitor. In this case, the total FC loss reduction can also be achieved with parallel HSF modules as compared to single HSF stage case. The equivalent series resistance (ESR) of a film capacitor can be expressed as a function of its capacitance, as written in (6.4) [105], where k_1 and k_2 are two coefficients that can be obtained from fitting the capacitors' data in datasheets. Based on the finding in [105], for EPCOS B3277x series, $k_1 = 2.29e-4\Omega$ and $k_2 = -2.76e-1\Omega$. With parallel connection, the current through each capacitor is reduced by half, and thus the required capacitance in each HSF module can be reduced by half without increasing the FC voltage ripple. As such, 40% total FC loss reduction can be achieved. It should be noted that film capacitors from other manufactures may have different values for where k_1 and k_2. But the potential of FC loss reduction should still be available. On the other hand, if the FC bank is realized by multiple parallel film capacitors, the total FC losses of a FC-IPC can be the same as that of a single HSF stage case.

$$ESR_C = k_1(C/Farad)^{k_2} \tag{6.4}$$

6.3.3 Modularity and Reliability Improvement

As all HSF modules are identically designed, modularity can be achieved from the hardware point of view. This inherent modularity will facilitate the system design and meanwhile enable the fault tolerant capability. In addition, the HSF modules are designed with partial power and lower cost, which could alleviate the pressure of manufacture, maintenance, and repair.

The reliability of the proposed concept can be evaluated through the mean time between failures (MTBF) of different topologies [106]. The MTBF of a component, MTBF_c, can be calculated by (6.5), where $R_c(t)$, expressed in (6.6), is the probability that a component does not fail over time, and λ_c is failure rate of the component.

$$\text{MTBF}_c = \int_0^\infty R_c\left(t\right) dt = \frac{1}{\lambda_c} \tag{6.5}$$

$$R_c\left(t\right) = e^{-\lambda_c t} \tag{6.6}$$

For system with redundancy, further calculation of the impact of redundancy must be included. Assuming a system with N necessary components and X redundant components, the survival probability of the system becomes (6.7) [106].

$$R_{sys}\left(t\right) = \sum_{i=0}^{X} \binom{N+X}{i} R_c^i (1-R_c)^{N+X-i} \tag{6.7}$$

The LSF part and the HSF modules in the proposed topologies are connected in series. As such, the probability that the topology survives over time, $R_{sys}(t)$, can be written as (6.8), where $R_{LSF}(t)$ and $R_{HSF}(t)$ are the probabilities that the LSF part and the HSF modules do not fail, respectively. Since each LSF part or each HSF module has 4 devices, they can be given by (6.9)and (6.10), respectively, where λ_{HSF} is the failure rate of each device in HSF module and λ_{LSF} is the failure rate of each device in LSF part.

$$R_{sys}\left(t\right) = R_{LSF}\left(t\right) R_{HSF}\left(t\right) \tag{6.8}$$

$$R_{LSF}(t) = e^{-4\lambda_{LSF}t} \tag{6.9}$$

$$R_{HSF}(t) = e^{-4\lambda_{HSF}t} \tag{6.10}$$

For conventional topologies without internal parallel connection, redundancy is not available. Using the 5L ANPC as an example, the survive probability of the system (device only) can be written as (6.11). The MTBF is then given in (6.12). Note that only single phase is considered. The MTBF of a three-phase system is 1/3 of (6.12).

$$R_{5LANPC}(t) = R_{LSF}(t) \cdot R_{HSF}(t) = e^{-4(\lambda_{LSF}+\lambda_{HSF})t} \tag{6.11}$$

$$\text{MTBF}_{5LANPC} = \frac{1}{4(\lambda_{LSF} + \lambda_{HSF})} \tag{6.12}$$

The reliability of the FC-IPC can be discussed in twofold. First, for a system that conventionally is built by N parallel converters, an alternative design solution is that using the FC-IPC topology with N parallel HSF modules. The MTBF expressions of the two solutions can be given as (6.13)and (6.14), respectively, where $\text{MTBF}_{5LANPC,N}$ stands for the design with N parallel 5L ANPC converters and $\text{MTBF}_{IPC,N}$ is the MTBF value of FC-IPC with N HSF modules.

$$\text{MTBF}_{5LANPC,N} = \frac{1}{4N(\lambda_{LSF} + \lambda_{HSF})} \tag{6.13}$$

$$\text{MTBF}_{IPC,N} = \frac{1}{4\lambda_{LSF} + 4N\lambda_{HSF}} \tag{6.14}$$

Fig. 6.13 shows the value of $\text{MTBF}_{IPC,N}/\text{MTBF}_{5LANPC,N}$ with respect to the ratio of the failure rate between HSF and LSF modules ($\lambda_{HSF}/\lambda_{LSF}$). Apparently, the FC-IPC topology shows higher reliability than the parallel converter configuration in this case. Note that with practical considerations, the ratio $\lambda_{HSF}/\lambda_{LSF}$ is typically around 5 as the LSF part normally faces less thermal stress than the HSF modules [107]. With WBG devices, this ratio,

though still unknown, can be even higher since the technology of WBG device is not mature yet. Also, as has been pointed out earlier in the introduction, the FC-IPC converter can also be connected in parallel, offering one additional degree-of-freedom for system architecture design.

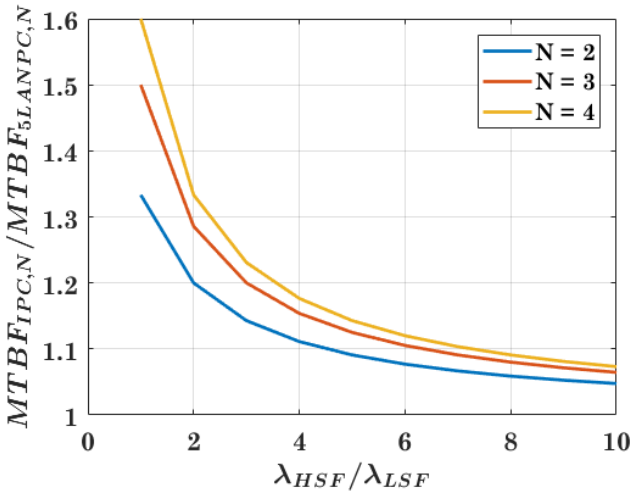


Figure 6.13. $\text{MTBF}_{IPC,N}/\text{MTBF}_{5LANPC,N}$ as a function of $\lambda_{HSF}/\lambda_{LSF}$. Results with different N are also shown.

Design redundancy is highly desirable in high power and critical applications [52, 106]. Therefore, the second evaluation case considers the FC-IPC topology with redundancy. Based on (6.7), the survival probability of the FC-IPC with one normal HSF module and one redundant HSF module (N = 1 and X = 1) can be written as (6.15). Correspondingly, the MTBF in this case is given by (6.16).

$$R_{IPC,X=1}(t) = 2e^{-4(\lambda_{LSF}+\lambda_{HSF})t} - e^{-(4\lambda_{LSF}+8\lambda_{HSF})t} \tag{6.15}$$

$$\text{MTBF}_{IPC,X=1} = \frac{2}{4(\lambda_{LSF}+\lambda_{HSF})} - \frac{1}{4\lambda_{LSF}+8\lambda_{HSF}} \tag{6.16}$$

Based on (6.12) and (6.16), the ratio $\text{MTBF}_{IPC,X=1}/\text{MTBF}_{5LANPC}$ as a function of $\lambda_{HSF}/\lambda_{LSF}$ can be plotted in **Fig. 6.14**. One can see that with one redundant HSF module, the FC-IPC topology has at least 33% improvement in reliability when compared to the conventional 5L ANPC converter. If the redundant HSF modules are able to be repaired during the fault interval,

the system reliability can be boosted to even higher level [52]. It also should be noted that the redundancy obtained through the IPC topologies is cost effective, since only redundant HSF module is necessary.

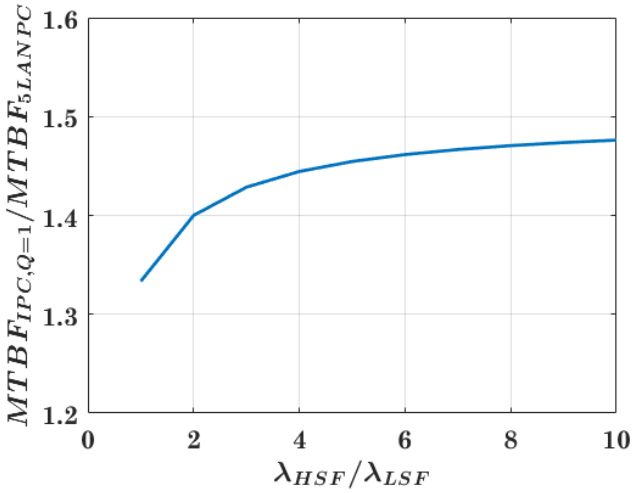


Figure 6.14. $\text{MTBF}_{IPC,X=1}/\text{MTBF}_{5LANPC}$ as a function of $\lambda_{HSF}/\lambda_{LSF}$ when $N = 1$ and $X = 1$.

6.3.4 Potential Power Density Improvement

First, power density can be potentially improved as the IPC topologies allow high speed devices to be used in higher power applications where Silicon based designs are now dominating. The filter size could be reduced owing to high frequency switching. In addition, interleaving provides increased number of levels in the output voltage, which can alleviate the overvoltage issue at motor terminal. Moreover, high frequency CM harmonics can be cancelled by interleaving, mitigating the CM noise issue. This will also in turn help to improve system power density, as CM filter size can be reduced.

Moreover, in many applications where high power density or natural convection is preferred, paralleling switching devices has been a common practice to reduce the total conduction losses [28] or to achieve even thermal distribution [108]. With the proposed IPC topologies, such function can be realized at the HSF module level, rather than the device level. As such, fault tolerance and modularity can be achieved in addition to the reduction of total conduc-

tion losses. Note that IPC may need more gate driver ICs. However, compared to the volume and weight of the heatsink, the additional space occupied by the ICs is normally negligible.

6.4 Simulation Verifications

Simulation results have been obtained to verify the proposed topologies. The system parameters are listed in **Table 6.1**, emulating a three-phase PV inverter with new high speed devices in HSF modules. The open-loop simulation results of HB-IPC with 2 and 3 HSF modules are shown in **Fig. 6.15**. As one can see, with 2 HSF modules, the output voltage is 5L while it is 7L with 3 HSF modules. Likewise, the results of FC-IPC shown in **Fig. 6.16** verifies that the output voltage is 9L with 2 HSF modules and is 13L with 3 HSF modules.

Table 6.1. System parameters in simulation.

Parameter	**Value**
DC voltage	900V
Power rating	50kW
Carrier frequency	30kHz
Grid frequency	60Hz
Grid voltage	480V

Closed-loop simulation results are obtained with a FC-IPC that has 2 HSF modules. Two types of filter architectures are considered. One is the modular architecture with single phase inductors at the converter side, as shown in **Fig. 6.17 (a)**. The other one is coupled architecture using coupled inductor (CI), as shown in **Fig. 6.17 (b)**. The filter parameters of these two architectures are listed in **Table 6.2**. The converter side inductance, L_c, is selected based on 30% of current ripple in the converter output current.

The simulation results are shown in **Fig. 6.18**. As evidenced in the harmonic spectrums, the resultant output output current qualities can meet the grid code in both cases. In particular, the grid side inductance of the modular architecture can be provided by the grid impedance in practical applications. Due to higher circulating current, the converter side current with single phase

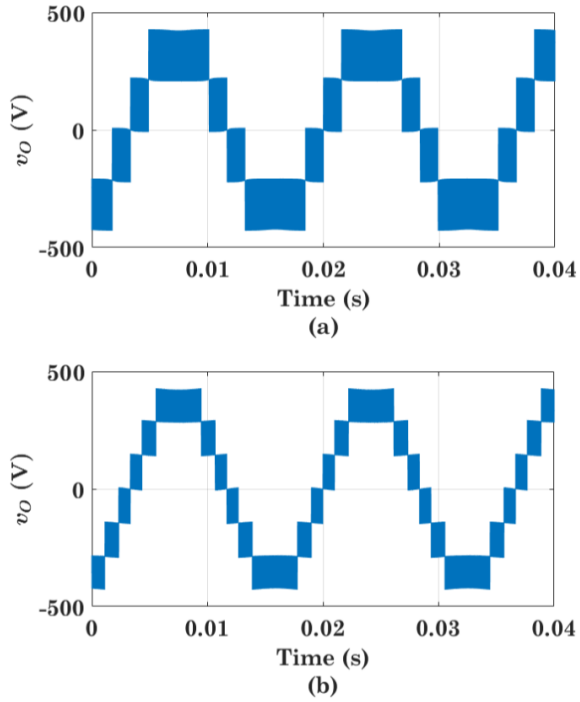


Figure 6.15. Phase-leg voltage of HB-IPC with (a) 2 HSF modules and (b) 3 HSF modules. Modulation index in simulation is 0.9.

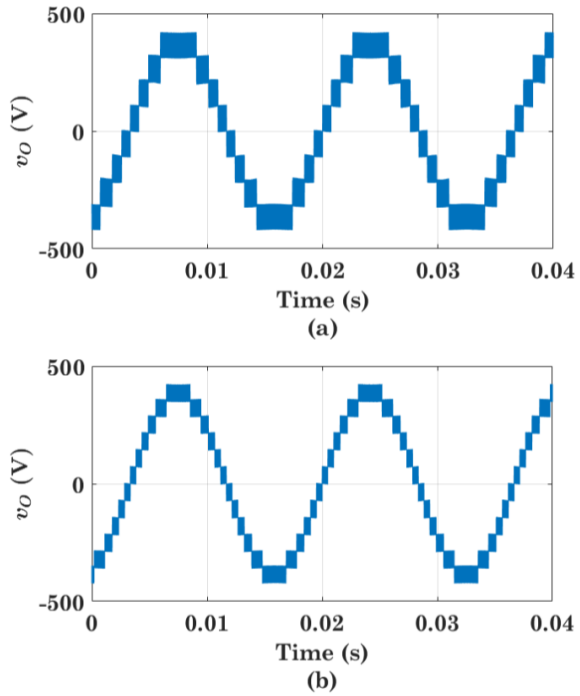


Figure 6.16. Phase-leg voltage of FC-IPC with (a) 2 HSF modules and (b) 3 HSF modules. Modulation index in simulation is 0.9.

Table 6.2. Filter parameters in simulation.

Parameter	Modular	Coupled
CI	N/A	5mH
L_c	80uH	15uH
C_f	12uF	18uF
L_g	3uH	10uH

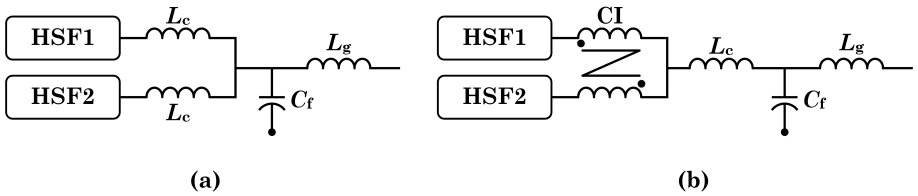


Figure 6.17. Illustration of two filter architectures, (a) modular architecture and (b) coupled architecture.

inductors shows higher ripple components than that with CI. However, the peak values of individual HSF module currents in the two cases are very close to each other, suggesting that the resultant conduction losses should be similar.

A comparative analysis of the filer utilization can be carried out between the modular architecture based FC-IPC and the 5L ANPC. Given the same converter side current ripple requirement and carrier frequency, a 5L ANPC converter will need 27uH at the converter side. If the same filer capacitance, i.e. 12uF, is used, a 55uH grid side inductor is required to meet the grid code. Following the area product based inductor volume evaluation approach introduced in the last chapter [85], the inductor volume required by the FC-IPC is only 59% of that required by the 5L ANPC. On the other hand, with an optimal filter design, the 5L ANPC converter requires 38uH inductors at both converter side and grid side, and 28uF (5% p.u.) as filter capacitance. Given the same converter output current ripple requirement, the converter side inductance in the FC-IPC will be increased to 113uH. In this case, the inductor volume required in the FC-IPC based system is still only 80% of that in the 5L ANPC based design. Note that in this case the filter capacitance in the FC-IPC will be much less than that with 5L ANPC. Also, if WBG or CoolMOS is used, the total switching losses of the 5L ANPC may be higher than that of the FC-IPC. Although only FC-IPC is adopted in simulation, the

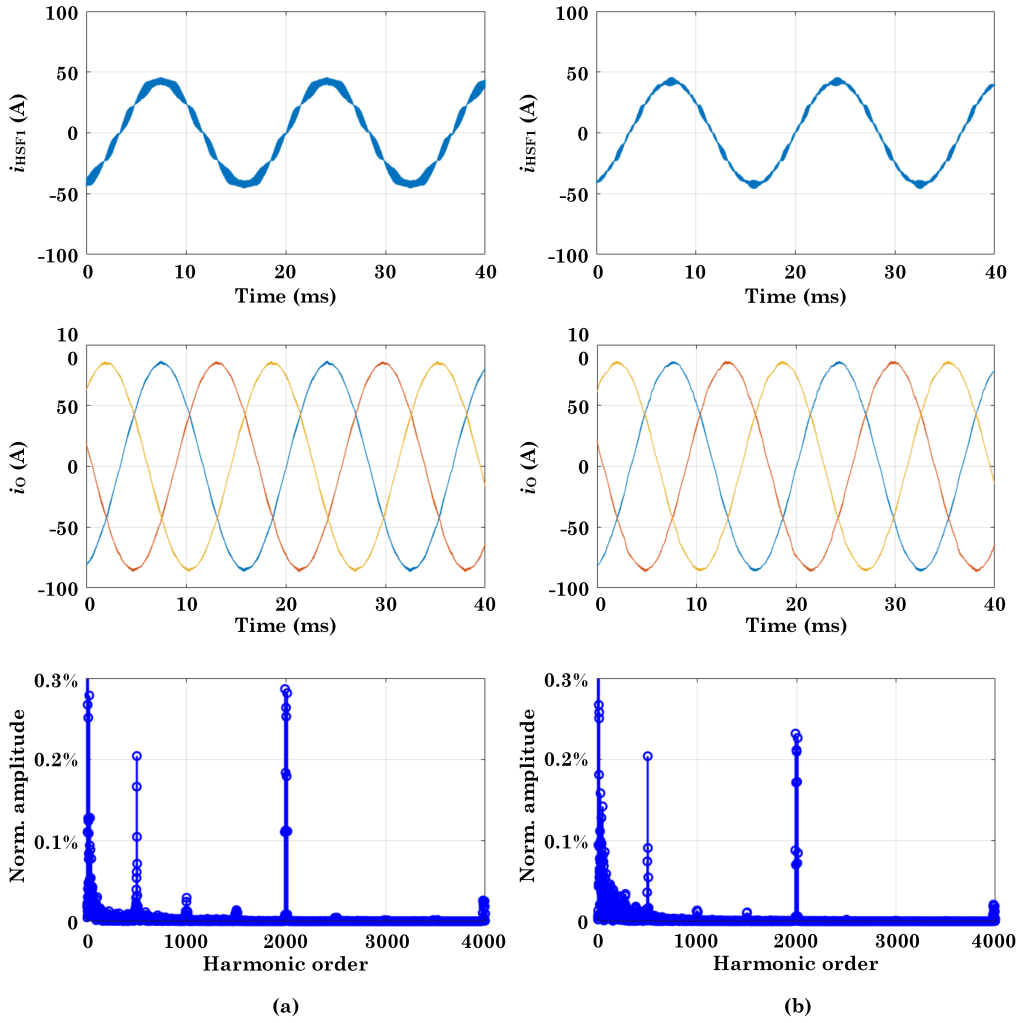


Figure 6.18. Simulated waveforms of the individual HSF module current i_{HSF1}, the total output current at the grid side i_O, and the spectrum of i_O, with (a) modular architecture and (b) coupled architecture.

filter size reduction performance is also achievable with HB-IPC.

6.5 Summary

A novel internal parallel converter (IPC) concept is proposed in this chapter. The IPC concept leverages the topological decoupling feature of the conventional ANPC converters and the merits of parallel connectivity. Based on this concept, a family of new high-level topologies can be derived. The foremost advantages of the IPC concept include design modularity, fault tolerance, en-

hanced reliability, flexible device selection, and reduced current stress over high switching frequency devices. Simulation has been conducted to verify the functionality of the proposed converter. A comparative analysis based on simulation results shows that compared to conventional non-parallel topologies (i.e. ANPC topologies), the proposed IPCs can effectively reduce the size of filter through interleaving operation. Besides the basic embodiments introduced in this chapter, more IPC topologies can be found in the Appendix D. As discussed in this chapter, the IPC topologies are attractive to new high speed devices like WBG and CoolMOS. Therefore, in the next chapter, a high density demonstration prototype of the FC-IPC topology will be designed using GaN HEMT as HSF device.

Chapter 7

FC-IPC Prototype Design and Validation

In the previous chapter, the IPC concept is proposed for synthesizing new high-level converter topologies. A key feature of the IPC concept is that Silicon and WBG devices can be used together in the same topology. In this chapter, a high density FC-IPC prototype is designed as the demonstrator of the proposed IPC concept.

The targeted application of the prototype is the emerging three-phase 1500V class photovoltaic (PV) string inverter with typical power range between 30kW to 100kW. For this type of inverter, conventional design normally adopts Silicon IGBT based three-level converter. In order to get higher efficiency, the switching frequency tends to low. As a result, the maximum power density that the commercial string inverters can reach is only 0.5kW/L for volume and 1.4kW/kg for weight [1]. Installation and maintenance of such an inverter require at least two workers. Considering that a solar farm can have thousands of such inverters, the cost of installation and maintenance will be substantial. As such, increasing power density has been a major thrust of the research.

On the other hand, adopting WBG devices to increase the power density while keeping high efficiency has been another trend in power electronic system design. For the 1500V class inverter, 1200V SiC MOSFET are applicable with the HB-IPC topology shown in **Fig. 6.8**, whereas with the FC-IPC topology shown in **Fig. 6.10**, the 650V GaN High Electron Mobility Transistor

(HEMT) is sufficient. In this thesis, the design based on FC-IPC and GaN is selected as a demonstrator.

7.1 Design Considerations of the Prototype

In this section, the design considerations of the prototype are discussed. The specifications of the prototype are presented in **Table 7.1**[1]. Based on the system specifications, the 650V/60A GaN device GS66516 is selected as the HSF device [109], and the Silicon IGBT IKQ50N120CT2XKSA1 with 1200V/100A rating is selected as LSF device [110]. To meet the total power rating, two HSF modules are required in each phase. Different from many other high density designs, where the semiconductor devices are usually over-selected to reduce the total losses, the device selection for the prototype at hand is not an over-design.

Table 7.1. Key design parameters of the prototype.

Parameter	Value
Maximum DC voltage	1500V
Nominal AC voltage	690V
Rated power	70kW

The major design considerations of the prototype include the loss estimation and flying capacitor bank sizing. The loss information is important for cooling system design. Whereas the flying capacitor must be properly sized to ensure reliable operation and high power density.

7.1.1 Device Power Loss Estimation

The power losses of the prototype consist of three parts, i.e. the switching losses of HSF modules ($P_{sw,HSF}$), the conduction losses of the HSF modules ($P_{cond,HSF}$), and the conduction loss of the LSF part ($P_{cond,LSF}$). The switching losses at the LSF stage can be negligible since the switching frequency is only

[1]Some commercial products adopt 800V as nominal AC voltage [1]. With 800V AC output, the rated power rating of the prototype will be 83kW.

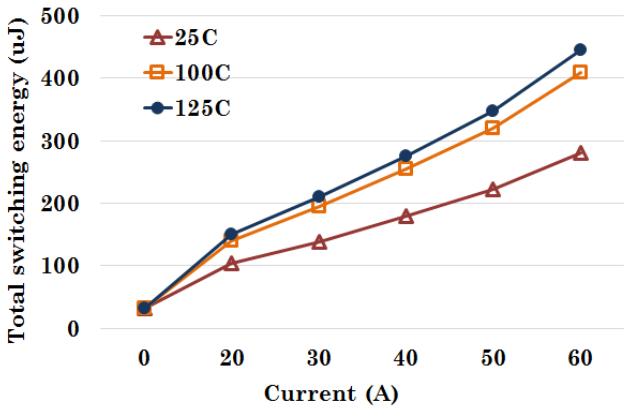


Figure 7.1. The total switching energy of GaN HEMT GS66516 under different device junction temperature.

60Hz. The modeling and estimation of these three types of losses are given below.

The switching losses resultant from the HSF modules are dominating the total switching losses of the system. For a GaN device, the switching loss, P_{sw} can be estimated with (7.1).

$$P_{sw} = f_s \sum_{i=1}^{f_s/f_1} \left[E_{sw,on}\left(I_{ds,on,i}, V_{ds}, T_j\right) + E_{sw,off}\left(I_{ds,off,i}, V_{ds}, T_j\right)\right] \tag{7.1}$$

where $E_{sw,on}$ and $E_{sw,off}$ are the turn-on and turn-off energy respectively, $I_{ds,on,i}$ and $I_{ds,off,i}$ are the currents at turn-on and turn-off instant, respectively, T_j is the device junction temperature, V_{ds} is the switching voltage of the device, which is a constant value equals to the device blocking voltage. Note that GaN has zero reverse recovery loss. Considering that the turn-off energy of a GaN HEMT is much lower than its turn-on energy, and that $I_{ds,on,i} \approx I_{ds,off,i}$ in a hard switching case, and the switching loss can be estimated with the total switching energy. Note that the switching energy is temperature dependent. Higher device junction temperature results in larger switching energy, as illustrated in **Fig. 7.1** for GaN HEMT GS66516. Typical gate resistances, i.e. 10Ω for device turn-on and 2Ω for device turn-off, are applied in **Fig. 7.1**. Also, the switching voltage is assumed as 375V, which is the nominal voltage stress over the HSF devices in the designed prototype.

The conduction loss of a GaN HEMT, $P_{cond,GaN}$ can be estimated with

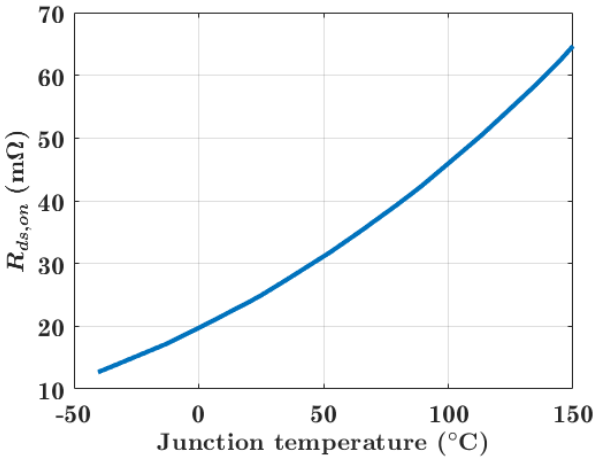


Figure 7.2. The $R_{ds,on}$ of GaN HEMT GS66516 as a function device junction temperature.

(7.2), where $R_{ds,on}$ is the on-state resistance of the device, $I_{rms,GaN}$ is the RMS value of the current through the GaN device [111]. For GaN HEMT, the reverse conduction mode (act as a diode but with gate turned on) has the same on-state resistance as in forward conduction. Therefore, it is unnecessary to separately calculate the RMS current in switch mode and diode mode. Assuming the power factor seen by the converter is 1, the RMS current then can be calculated based on (7.3), where $\hat{i}_{O,HSF}$ is the peak value of the AC output current in one HSF module [97].

$$P_{cond,GaN} = I^2_{rms,GaN} R_{ds,on} \tag{7.2}$$

$$I_{rms,GaN} = \frac{\hat{i}_{O,HSF}}{2} \tag{7.3}$$

The on-state resistance of the GaN HEMT also varies with the device junction temperature, as shown in **Fig. 7.2**. It is therefore necessary to take device junction temperature into account when estimating the conduction loss.

The conduction loss of the Silicon IGBT in the LSF part, $P_{cond,IGBT}$ can be estimated with with (7.4).

$$P_{cond,IGBT} = v_{CE0} I_{avg,IGBT} + R_{on,IGBT} I^2_{rms,IGBT} \tag{7.4}$$

where v_{CE0} is the zero-current forward voltage drop of the IGBT, $R_{on,IGBT}$ is

the on-state resistance of the IGBT, $I_{avg,IGBT}$ is the average current flowing through the device, and $I_{rms,IGBT}$ is the RMS value of the device current. Note that in unity power factor condition, the anti-parallel diodes of the IGBTs do not conduct current, and therefore their losses are not given. Both v_{CE0} and $R_{on,IGBT}$ can be obtained based on the output characteristic in the device's datasheet. Note that both parameters are temperature-dependent.

For unity power factor condition, the RMS current of the two outer IGBTs ($S1$ & $S4$ in **Fig. 6.10**) can be given in (7.5), where $\hat{i}_{O,tt}$ is the peak of total output current and M is the modulation index. The RMS current of the inner two IGBTs ($S2$ & $S3$) can be calculated with (7.6) [111].

$$I_{rms,IGBT,out} = \frac{\hat{i}_{O,tt}}{\sqrt{2}}\sqrt{\frac{4M}{3\pi}} \tag{7.5}$$

$$I_{rms,IGBT,in} = \frac{\hat{i}_{O,tt}}{\sqrt{2}}\sqrt{\frac{1}{2} - \frac{4M}{3\pi}} \tag{7.6}$$

The average current of the outer two IGBTs and the inner two IGBTs are expressed in (7.7) and (7.8) respectively.

$$I_{avg,IGBT,out} = \frac{\hat{i}_{O,tt}M}{4} \tag{7.7}$$

$$I_{avg,IGBT,in} = \frac{\hat{i}_{O,tt}}{\pi} - \frac{\hat{i}_{O,tt}M}{4} \tag{7.8}$$

7.1.2 Switching Frequency Selection and Efficiency Estimation

The switching frequency should be selected based an overall consideration of the system's efficiency. **Fig. 7.3** shows the calculated switching loss per GaN HEMT at the rated output with respect to different switching frequencies and junction temperature values. Clearly, with higher junction temperature, the switching loss will be higher. The figure also shows the advantage of GaN devices in terms of low switching loss.

The conduction loss of each GaN HEMT can also be calculated based on the estimation model. With the on-state resistance obtained from **Fig. 7.2** for

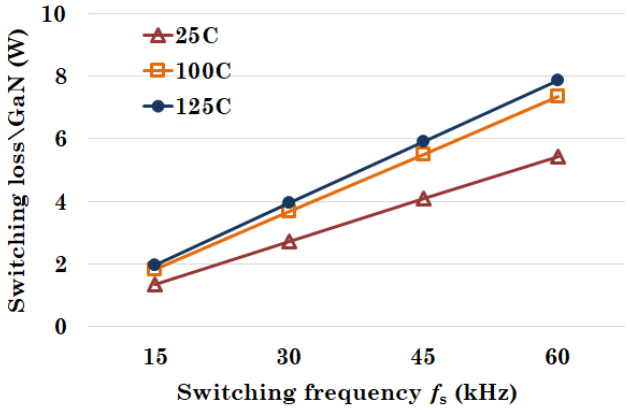


Figure 7.3. Calculated switching loss of each GaN HEMT under different switching frequencies and device junction temperature values.

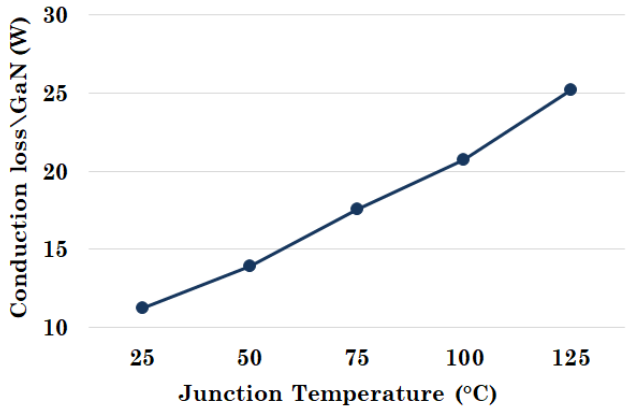


Figure 7.4. Calculated conduction loss of each GaN HEMT under different junction temperature values.

different temperature values, the conduction loss per GaN device in the HSF module is shown in **Fig. 7.4**. Due to the positive relationship between the on-state resistance and the junction temperature of GaN device, the conduction loss of GaN is also very sensitive to the temperature and can vary in a wide range.

The conduction losses of the IGBTs are shown in **Fig. 7.5**. Same as that of GaN, the conduction loss of IGBT also increases with the junction temperature. The datasheet of IKQ50N120CT2XKSA1 only provides output characteristic information under 25°C and 175°C, but the data for 100°C can be estimated from the figure showing the relationship between the collector-emitter saturation voltage and the junction temperature. The conduction loss

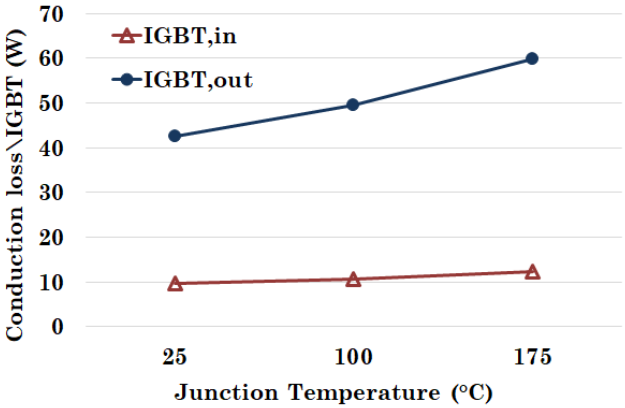


Figure 7.5. Calculated conduction loss of the inner and outer IGBTs under different junction temperature values.

under other temperature condition can also be estimated since it is basically in proportion to the junction temperature.

With all the losses calculated, the converter efficiency and total loss with different switching frequencies can be obtained for the rated output condition. The results are shown in **Fig. 7.6**. As can be seen, the impact of switching frequency on the overall efficiency is not significant since the switching losses only occur in the HSF modules, and the considered switching frequency is only around tens of kHz. However, due to the high total power rating of the prototype, higher switching frequency results in more power losses, which will challenge the design of cooling system. Considering that the physical flying capacitor design is in fact limited by the capacitor current rating rather than the capacitance (see subsection 7.1.3), and that the limited control algorithm execution time with high switching frequency, a moderate switching frequency, i.e. 30kHz, is selected.

With the 30kHz as switching frequency, the converter efficiency can be estimated as shown in **Fig. 7.7** assuming the DC link voltage is 1500V. Note that the estimated values have already taken the losses from fan (see subsection 7.2.3) and power supply into account. The peak efficiency is 99.25% when junction temperature is 25°C, and is 99.15% under 100°C junction temperature. To achieve higher efficiency, it is important to keep the device junction temperature low. Also, in light load condition, the total power losses from the

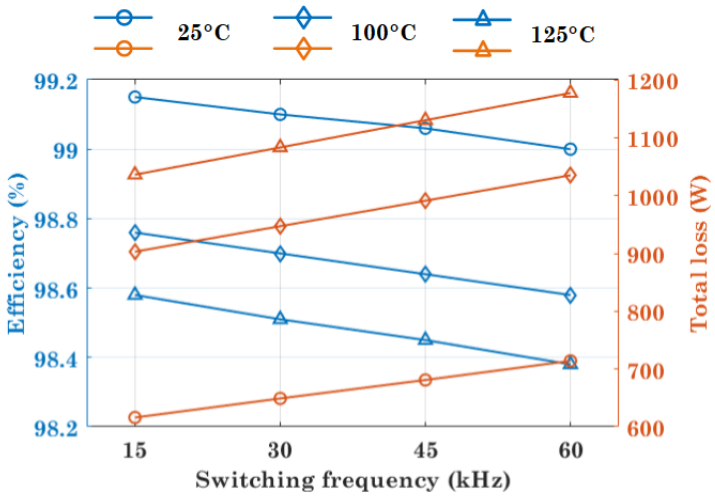


Figure 7.6. Estimated converter efficiency and total semiconductor loss with different switching frequencies for the rated output condition.

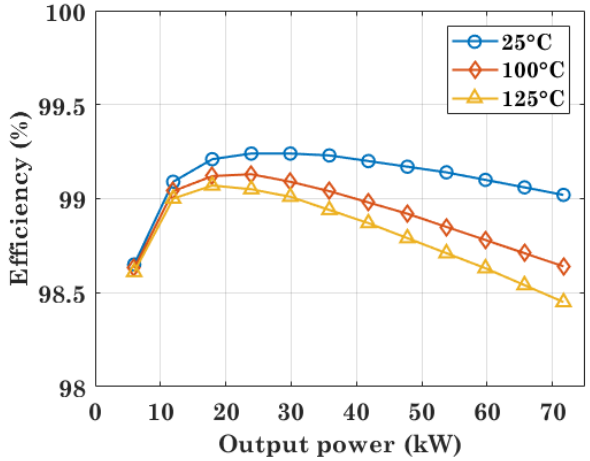


Figure 7.7. Estimated converter efficiency in full power range and 1500V DC link voltage.

devices are low, and the junction temperature of the devices should be low as well. Therefore, the peak efficiency of the converter should be around 99.2%[2].

7.1.3 Flying Capacitor Sizing and Design

The flying capacitor must be properly sized according to the voltage ripple requirement and the current rating of the physical capacitor. The voltage

[2]If 800V AC output voltage is employed as in many commercial 1500V class string inverters, the rated output power of the prototype will be boosted to 83kW, and the peak efficiency can be even higher. Also, with lower DC link voltage, e.g. 1200V, higher efficiency can also be achieved.

ripple requirement will determine the minimum capacitance $C_{FC,min}$, which can be calculated based on (7.9).

$$C_{FC,min} \geq \frac{\hat{i}_{O,HSF}}{(N_L - 1) f_s \Delta V_{FC,max}} \tag{7.9}$$

where N_L is the number of converter levels which is 5 in the FC-IPC topology, and $V_{FC,max}$ is the maximum allowed voltage ripple over the flying capacitor. For this design, $V_{FC,max}$ is selected as 5% of the nominal flying capacitor voltage, i.e. 375V. Given the selected 30kHz switching frequency, the minimum capacitance is 23μF assuming the output current ripple is 30% of the fundamental current.

The required current rating of the physical flying capacitor is defined by the maximum RMS current through the capacitor. The RMS value of the flying capacitor current is affected by both power factor and modulation index. It can be found analytically in frequency domain. However, due to the interactions between the AC output current harmonics and the flying capacitor current harmonics, the analytical solution will be very sophisticated. Therefore, simulation has been carried out assuming 30% ripple at the AC output current of each HSF module. The result is shown in **Fig. 7.8**, where the RMS flying capacitor current, $I_{FC,rms}$, is normalized to the RMS value of the total fundamental output current. It can be seen that the maximum value occurs when the power factor is 1 and the modulation index is around 0.5. Considering the possible grid voltage-sga and ride through operation, the fling capacitor must be sized at this point. For this design, the RMS value of the AC output current is 60A, and thus the maximum flying capacitor current is around 28A RMS.

To physically realize the flying capacitor, three types of capacitors, i.e. ceramic capacitor, electrolytic capacitor (ECap) and filter capacitor (FCap), have been applied as flying capacitor in literature. Ceramic capacitor has much lower capacitance especially when rated voltage is high, making it inappropriate for realizing flying capacitors with high nominal voltage. Between ECap and FCap, the ECap has the higher energy density and is often selected for energy buffer application. However, when applied as flying capacitor, the

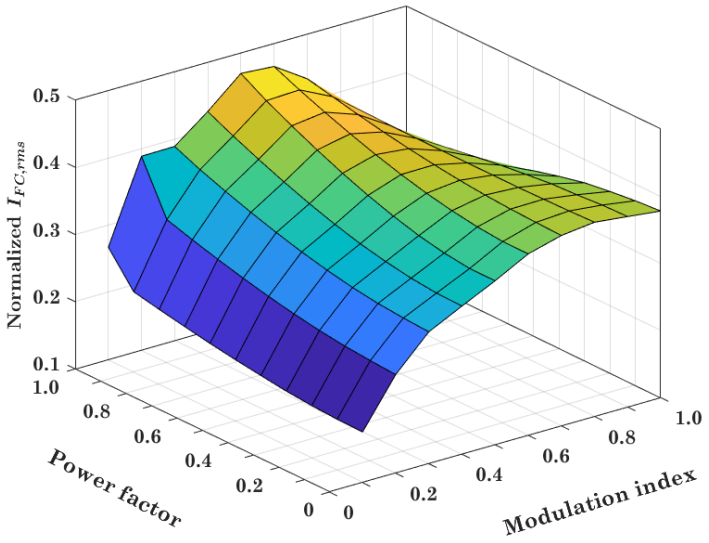


Figure 7.8. The normalized flying capacitor current $I_{FC,rms}$ with respect to modulation index and output power factor.

current rating is the primary concern in design. Shown in **Fig. 7.9** are the comparisons between ECap and FCap in terms of current density and current/capacitance. The data was collected from major capacitor manufacturers[3]. Evidently, the FCap has better performances in both indices, indicating that the flying capacitor bank will be smaller with FCap.

In the final physical realization, five 450V/10μF FCaps (part number: C4AEGBU5100A1XK) are connected in parallel, leading to a 50μF flying capacitor bank. The major reason of this design is that it results in the minimum size. The increase in capacitance as compared to the minimum capacitance is mainly because of the positive relationship between the capacitance and the current rating. With lower capacitance, the allowed current ripple will be smaller. For the design in this work, and other high current designs, the flying capacitor is dominated by the current rating. After searching the suitable part, it is found that any design that meets the 28A current rating requirement will

[3]The FCap data was retrieved from the datasheets of Vishay MKP series, TDK MKP series (B32794-B32798 and B32674-B32678), Panasonic EZPE series, and Illinois Capacitor MHBA series. The ECap data was collected based on the datasheets of Illinois Capacitor's BPS, CKH/CKE, and TXK series, KEMET ALS30 series, Panasonic EE-A series, CDE 450C series, and the Nichicon LNX series.

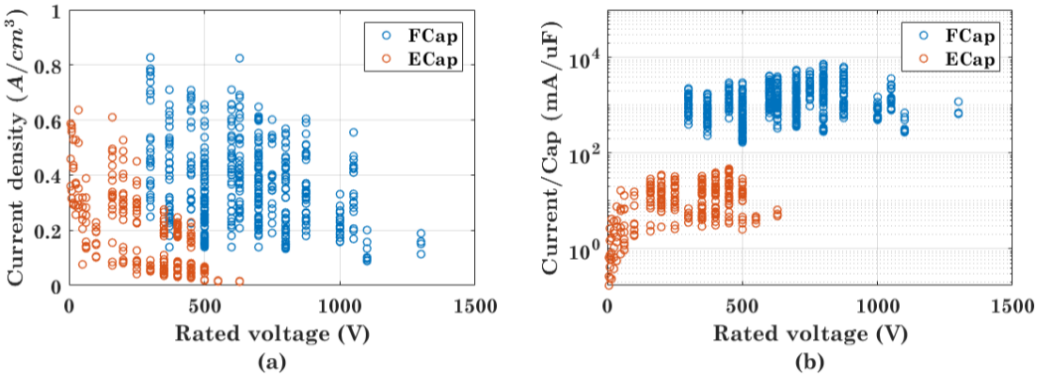


Figure 7.9. Comparison between FCap and ECap, (a) current density and (b) current/capacitance.

lead to an increased total capacitance, which is in fact a positive impact on the design and operation of the prototype. It also means that increasing the switching frequency will not actually reduce the size of the flying capacitor bank since the current rating requirement will not change.

The total current rating of five capacitors in this work is 32.5A, which is above the required 28A. The total equivalent series resistance (ESR) is $1.62m\Omega$, resulting in a maximum power loss of 1.27W in each flying capacitor bank. The temperature rise of the capacitors is low and cooling for them is unnecessary.

7.2 Hardware Realization of the Prototype

With the above design considerations, the hardware fabrication has been carried out to physically realize the prototype. As can be seen from the loss and efficiency estimation results (see subsection 7.1.2), keeping device junction temperature low is very important to ensure higher efficiency. Therefore, much effort has been put into the thermal design, which will be introduced from two aspects, i.e. the design of GaN power board with insulated metal substrate (IMS) circuit board and the design of heatsinks. The overall design of the HSF module and the LSF stage will also be introduced.

7.2.1 HSF Module Structure

The structure of the HSF module is first determined. A three-layer stack structure is employed as shown in **Fig. 7.10**, the 2D illustration of the HSF structure. The power board is placed at the bottom, with gate driver board attached closely above to minimize the parasitic inductance in the gating loop. The flying capacitor board is placed at the top of the HSF module. Note that some connection pins and terminals are not shown for better presentation. The selected structure requires the cooling system being placed beneath the GaN power board. Therefore, the bottom-cooled GaN HEMT GS66516B is used.

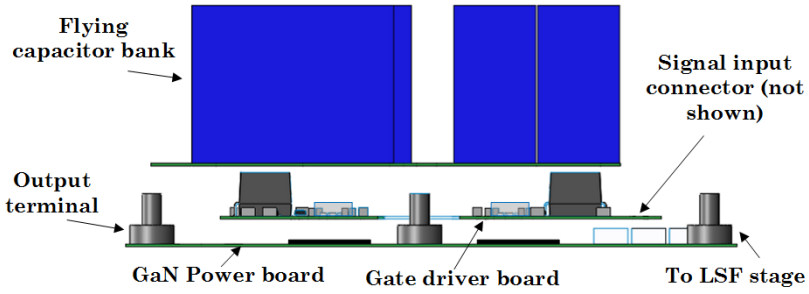


Figure 7.10. Structure of the HSF module.

7.2.2 GaN Power Board Design

The GaN power board has been designed with considerations in thermal and switching performances. To minimize the rise of the junction temperature of the GaN devices, the thermal resistance from the device junction temperature to the heatsink surface, R_{jHS}, should be minimized. In addition, the circuit layout must be properly designed to keep the parasitic inductance low. Decoupling capacitors should also be placed on the board to mitigate the impact of parasitic inductance.

GaN HEMTs have very small footprint, and therefore small heat dissipating surface area, which can be a challenging issue for thermal design. Moreover, the GaN devices in one HSF module must be insulated from each other. The conventional design technique for the bottom-cooled GaN HEMTs adopts the

printed circuit board (PCB) based power board with thermal vias facilitating the heat dissipation. The heatsink is attached under the power board. Due to the thermal vias, thermal interface material (TIM) with insulation ability must be filled between the power board and the heatsink. The structure of this conventional design is shown in **Fig. 7.11**.

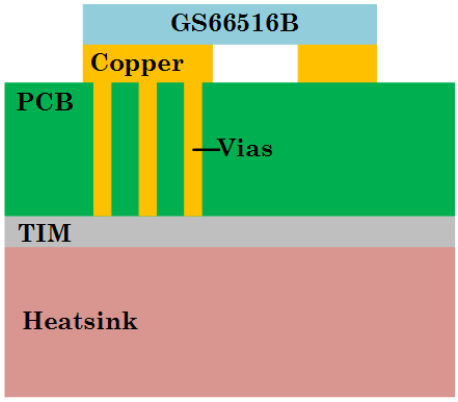


Figure 7.11. Structure of the conventional PCB based power board solution.

With this structure, the major barrier of cooling is the thermal conductivity performances of the typical RF4 material based PCB board and the TIM. The thermal conductivity of the typical RF4 PCB is only 0.35W/mK. With thermal vias, the effective conductivity can be improved depending on the diameter and the number of the vias. However, due to the small footprint of the GaN HEMTs, only thin and small amount of vias can be used, leading to poor cooling performance. Moreover, the thermal conductivity of the TIM is normally within 2W/mK, which also contributes a significant portion of the thermal resistance.

To improve the thermal performance of the power board, the insulated metal substrate (IMS) circuit board [112] is adopted in this work. The cross-sectional structure of the IMS based design is shown in **Fig. 7.12**. An IMS board consists of three layers, i.e. the copper trace layer, the dielectric layer, and the metal substrate layer (typically aluminium based). Both copper and aluminium substrate layers have high thermal conductivity, and therefore has negligible contributions to R_{jHS}. The bottleneck is the thermal conductivity of the dielectric layer, which provides insulation among the GaN HEMTs. The

thermal conductivity of the commercial dielectric layer material can reach 3W/mK. Compared to the RF4 PCB based design, significant improvement can be achieved. Also, due to the inherent insulation capability of IMS, TIM with insulation function can be eliminated. Instead, a thin layer of highly thermal conductive grease can be used to fill the voids between the aluminium substrate and the heatsink.

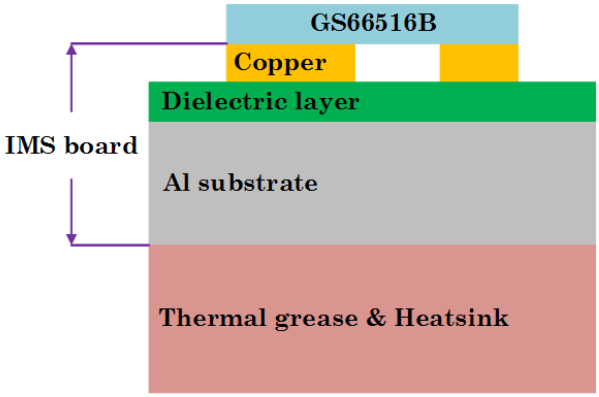


Figure 7.12. Structure of the IMS based power board solution. The flying capacitor is not included in the illustration.

The dielectric breakdown voltage of the selected dielectric layer material is 6kV, which is high enough for the prototype in this study. The thickness and thermal conductivity of each layer in the designed IMS power board are presented in **Table 7.2**. The R_{jHS} can be estimated with (7.10).

$$R_{jHS} \approx \frac{T_{Dielec}}{S_{GaN}K_{Dielec}} + \frac{T_{Al}}{S_{GaN}K_{Al}} + \frac{T_{TG}}{S_{GaN}K_{TG}} + R_{jC} = 1.45\text{K/W} \qquad (7.10)$$

where R_{jC} is the junction-to-case thermal resistance of the device, which is 0.27K/W for GS66516B. The area of the thermal pad of GS66508B, S_{GaN}, is approximately $44mm^3$.

Table 7.2. Specifications used for estimating R_{jHS} with the IMS based design.

Layer	**Thermal conductivity** (K)	**Thickness** (T)
Copper	-	140μm (4oz)
Dielectric	3W/mK	75μm
Aluminium	220W/mK	1.5mm
Thermal grease	5W/mK	0.1mm

Besides the thermal design, the circuit layout has been carefully designed. The high speed switching capability of GaN, while providing much reduced switching losses, makes the switching performance of the device sensitive to the parasitic inductances. The commutation loops in the prototype can be illustrated in **Fig. 7.13**, where L_{par1} and L_{par2} are the parasitic inductances in the HSF power board, L_{par3} is the parasitic inductance caused by the terminals connecting the LSF stage and the HSF modules, and L_{par4} is parasitic inductance mainly attributed to the PCB based DC bus bar and the relatively longer trace in the LSF stage. To mitigate the impact of these parasitic inductances, decoupling capacitors are distributed along the commutation loops as shown in **Fig. 7.13**. The effect of L_{par3} and L_{par4} can be easily attenuated by the decoupling capacitors C_{dec3} and C_{dec4}. As such the HSF module only sees a small amount of parasitic inductance from the LSF stage. By putting the decoupling capacitor C_{dec2} on the HSF power board, the HSF module and the LSF stage can be completely decoupled. Another benefit of the distributed decoupling capacitors is that C_{dec3} and C_{dec4} can be placed on the power board of the LSF stage. Since the space utilization requirement is relatively loose in the LSF stage, larger values can be selected for C_{dec3} and C_{dec4}. In this design, C_{dec3} is realized with 2.7μF film capacitor and C_{dec4} is 0.6μF realized with ceramic capacitors. Note that by decoupling the LSF stage and the HSF modules, the impact of parasitic inductances L_{par3} and L_{par4} is mainly imposed on the LSF devices. As Silicon IGBT has smaller dv/dt, the overvoltage issue will not be significant.

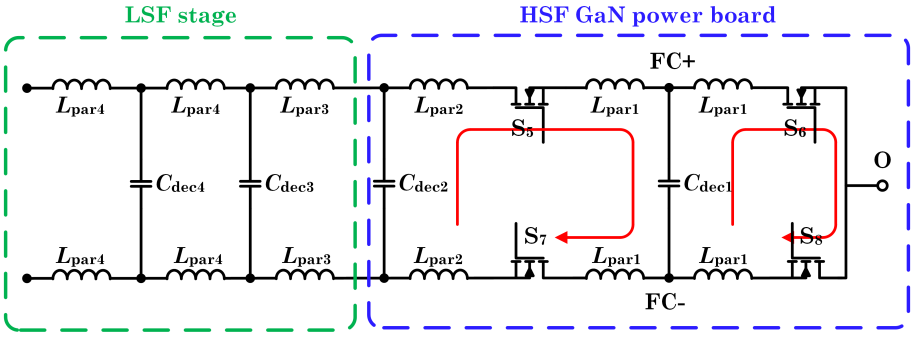


Figure 7.13. The parasitic inductances and the placed decoupling capacitors in the commutation loops of the prototype. The flying capacitor is not shown.

The major design challenge exhibits in the layout design of the HSF power board. As the IMS board only allows a single layer layout, all components are placed on the top layer of the board. As such, parasitic inductance reduction by cancelling electromagnetic field in multi-layer design is not applicable. The only available option is then to reduce the length of the trace while increasing its width. The designed layout is shown in **Fig. 7.14** with annotations. The length and width of one HSF power board is 97mm and 40mm, respectively.

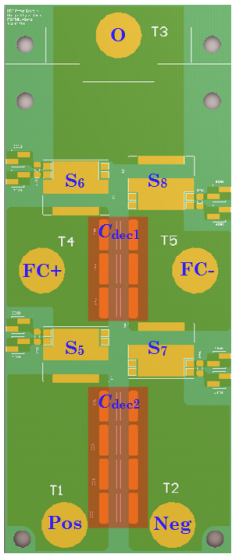


Figure 7.14. Circuit layout of the HSF GaN power board.

In the prototype, C_{dec1} is realized with 3 630V/1μF ceramic capacitors, and C_{dec2} is composed of 4 2kV/0.1μF ceramic capacitors. The estimated values of L_{par1} and L_{par2} are both around 8.7nH. The resultant overvoltage, V_{ov} can be calculated with (7.11). Assuming a peak current of 50A (with ripple current), the overvoltages imposed on both loops are less than 10V, which is only 2.7% of the nominal blocking voltage (375V) of the GaN devices.

$$V_{ov} = \hat{i}_{O,HSF}\sqrt{\frac{L_{par}}{C_{dec}}} \tag{7.11}$$

7.2.3 Cooling System Design

The cooling system consists of six fan-heatsinks. Each heatsink is made of copper and has a dimension of 40mm wide, 130mm long, and 46mm high. A

fan is attached to each heatsink, consuming 10W at the maximum speed. In full load operation, the total power loss caused by fans is 60W. However, in light load condition, the fan speed can be reduced by 2/3, and therefore the fan power loss can be reduced to 20W. A CFD simulation has been conducted through the Genie system from Aavid [113]. The simulated temperature contour image is shown in **Fig. 7.15**. Based on the loss calculation results in subsection 7.1.2, the total loss from six devices (4 GaN HEMTs and 2 IGBTs) is assumed as 160W, representing a total loss equivalent to the case with 100°C device junction temperature. An air flow rate of 27CFM is considered in the simulation. Ambient temperature is 25°C. The maximum temperature rise is 24°C. Temperature difference between the two IGBTs is caused by the uneven loss distribution (one with 47W loss and the other with 13W). The loss of each GaN HEMT is 25W.

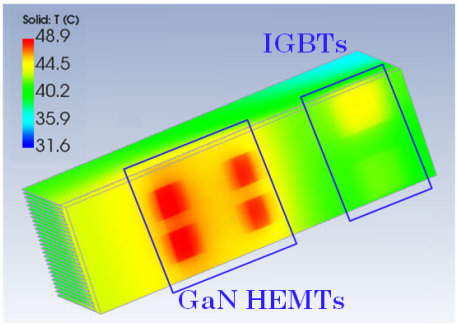


Figure 7.15. Simulated heatsink surface temperature distribution.

Based on the previously estimated value of R_{jHS} of GaN, the junction temperature at full load output is around 87°C, which is below the assumed 100°C in the CFD simulation. This means the performance of the cooling system should be able to limit the device junction temperature within 100°C at full load output.

7.2.4 LSF Stage Design and Final Assembly

The LSF stage design is relatively less challenging. All three phases are on the same four-layer power board. Also, the DC bus is integrated into the LSF stage to save the space of DC link bus bars. The layout of the LSF stage

is shown in **Fig. 7.16**. The size of the LSF power board is 240mm width and 120mm length. The Pos and Neg terminals are the connection points to one HSF module. As can be seen, each phase in the LSF stage is connected with two HSF modules. The decoupling capacitors C_{dec3} and C_{dec4}, as earlier explained, are placed on the LSF stage. The discrete IGBTs with TO-247 package are connected to the LSF board from the back side with thermal pad facing down. The gate driver boards for the LSF devices will be placed on top of the LSF power board.

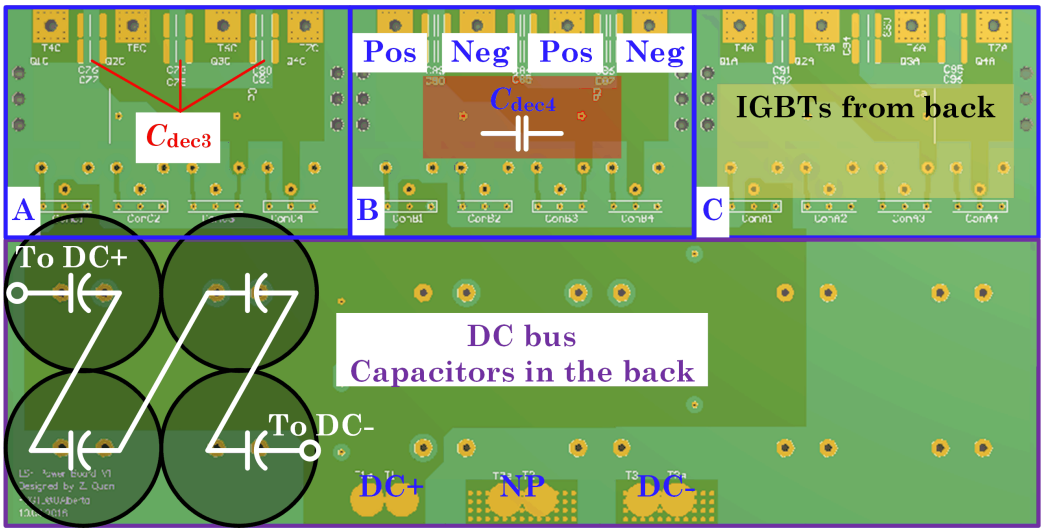


Figure 7.16. The annotated circuit layout of LSF stage.

The DC link capacitance is sized based on the the neutral point (NP) voltage ripple at 180Hz. For the FC-IPC or the 5L ANPC converter, the sizing approach of the DC link capacitance is similar to that in a NPC converter. Therefore, (7.12) can be employed to calculate the buffer capacitance at each half DC link in the worst case, and the total equivalent capacitance for the full DC link will be $C_{DC,half}/2$.

$$C_{DC,half} \geq \frac{0.0297 i_{O,tt}}{\Delta V_{NP} f_1} \tag{7.12}$$

where ΔV_{NP} is the allowed peak-to-peak NP voltage ripple at 180Hz. In this design, the desired ΔV_{NP} is within 2% of the full DC link voltage considering the possible operation state with reduced DC link voltage, leading to a minimum capacitance of 990μF.

The PCB based DC bus adopts a four-layer design, as illustrated in **Fig. 7.17**. ECap with 1mF capacitance is applied. The resultant $C_{DC,half}$ is 1500mF. As the height for the DC link capacitors is already defined by the height of the heatsink, using smaller capacitance will not save much space. Shown in **Fig. 7.17 (b)** is the series/parallel connection of the ECaps. The voltage rating of each ECap is 420V. With four in series, the maximum voltage rating is 1680V. Note that ECaps normally do not require significant voltage derating to operate safely as they are usually made with formation voltages over 35% higher than their rated voltages [114].

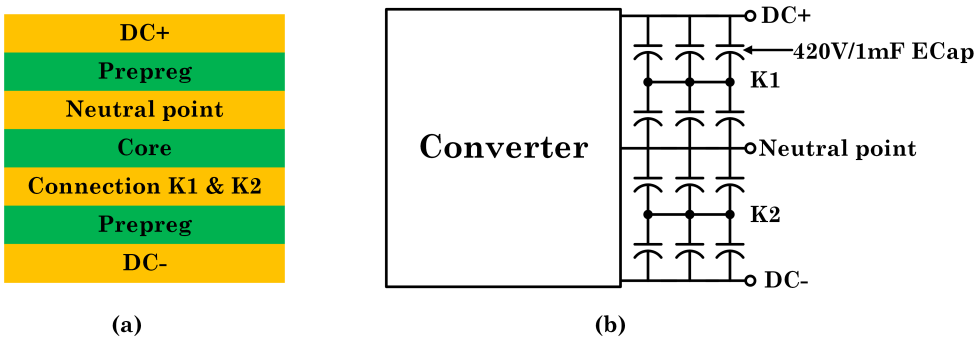


Figure 7.17. The cross-sectional structure of the four-layer PCB based DC bus.

The 3D construction of the converter part of the prototype is shown in **Fig. 7.18**. Note that the heatsink in the 3D model is only for size illustration, and does not show the actual looking of the designed heatsink. The box volume of the converter is 4.37L, leading to a volumetric power density over 16kW/L.

The photo of the physical prototype with coupled inductors is shown in **Fig. 7.19**. The coupled inductors are made of nanocrystalline core and copper foil winding. Although not shown in the photo, single-phase inductors have also been manufactured based on FeNi powder core and the results with them will be shown in the next section. The total volume of the fans and filters is less than 0.8L, leading to a theoretical volumetric prototype power density of 13.5kW/L. However, due to the unused space, the box volume of the prototype will increase to around 5.8L and the power density drops to 12kW/L.

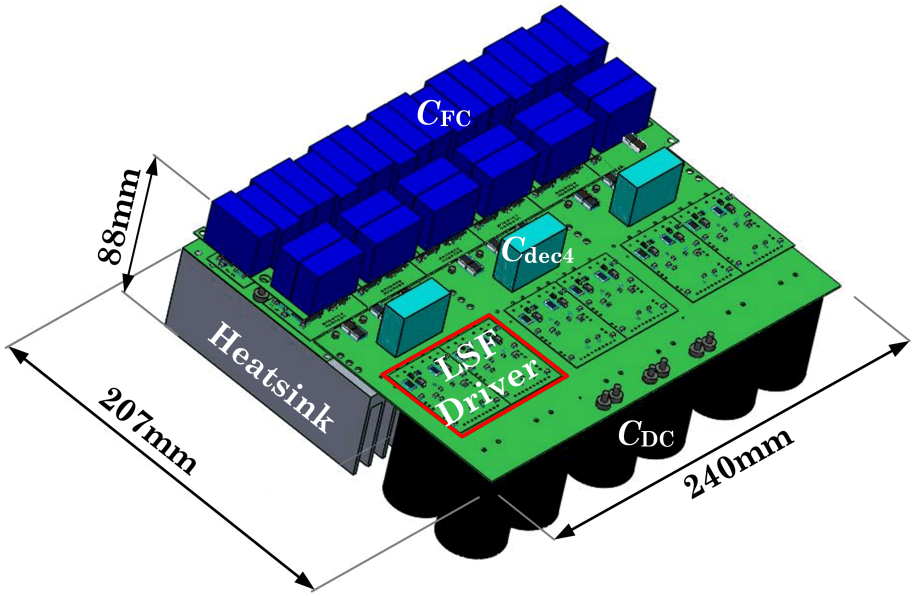


Figure 7.18. The 3D construction of the prototype. The Filters, fans, and controller board are not included.

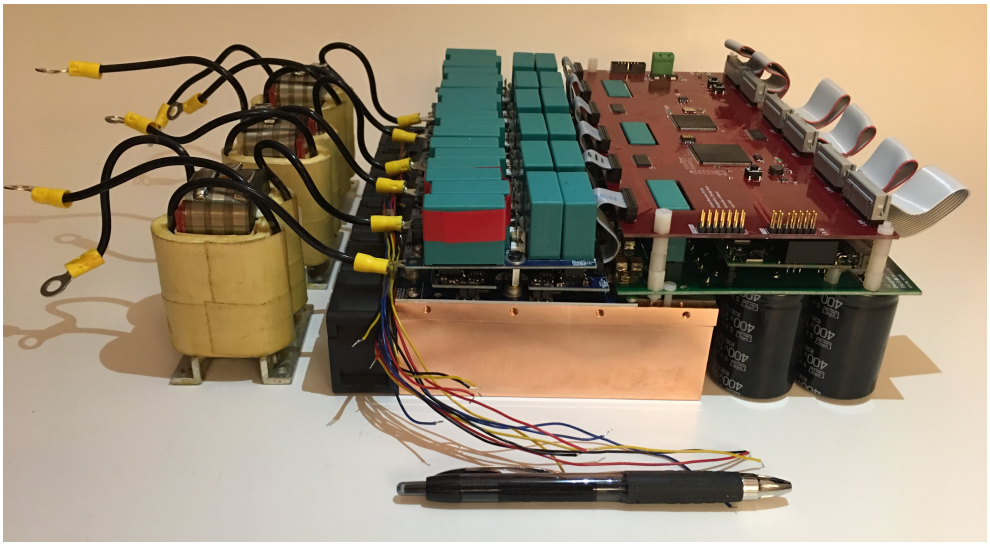


Figure 7.19. The photo of the physical prototype with coupled inductors.

7.3 Lab-scale Experimental Validation

Lab scale experimental verifications of the prototype have been conducted. The verifications include both three-phase tests and single-phase tests. The system parameters used in the experiment are listed in **Table 7.3**.

Table 7.3. Filter parameters in simulation.

Parameter	Three-phase	Single-phase
DC voltage	140V	
R load	6Ω	2.3Ω
L_{CI}	8mH	-
L_{SPI}*	80uH	

* SPI means single-phase inductor.

The measured waveforms of three-phase total output current with coupled inductors are shown in **Fig. 7.20**. In addition, the output current of one HSF module and corresponding total current are compared in **Fig. 7.21**. As one can see, the current ripple of the output current in one HSF module is in the save level as that in the total output current, as the coupled inductors have suppressed the circulating current to very small value. This can also be reflected from the spectra of the total current and individual HSF module current, as presented **Fig. 7.22 (a)** and **(b)**, respectively. As can be seen from the spectra, the harmonics around 60kHz (1000-order) have been suppressed to negligible level by the coupled inductor. The reconstructed waveform of circulating current is shown in **Fig. 7.23**, which confirms that its maximum amplitude is only 0.2A. Small low-frequency circulating current also presents in the waveform due to the imperfect system parameters. If such low-frequency circulating current is large, balancing control should be applied.

Measured results with single-phase inductors have also been obtained. The waveforms of three-phase currents are shown in **Fig. 7.24**. Comparing to the waveforms in **Fig. 7.20**, the current ripple with single-phase inductors is smaller since the single-phase inductors have larger inductance than the leakage inductance of the coupled inductors. As expected, the individual HSF module current with single-phase inductors shown in **Fig. 7.25** has much higher ripple than that with coupled inductors (see **Fig. 7.21**). However,

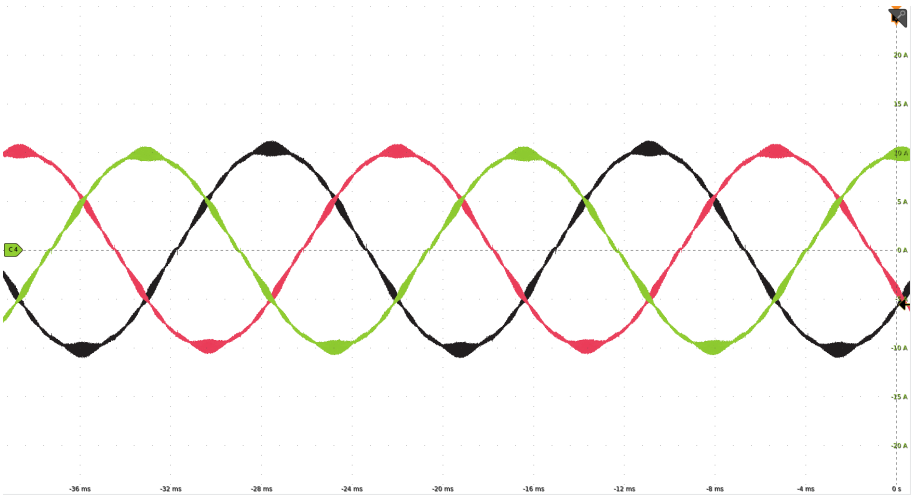


Figure 7.20. Measured three-phase total output current filtered by coupled inductors. Scale: 5A/div.

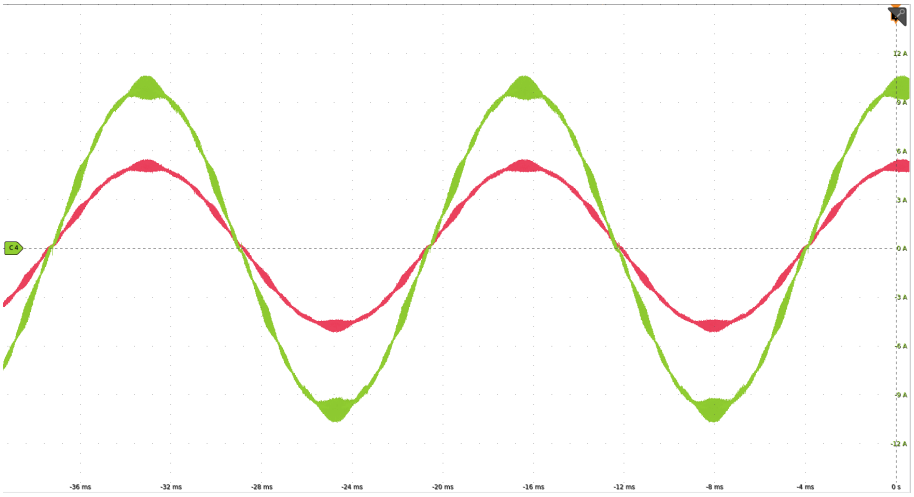


Figure 7.21. Measured output current of one HSF module (red) and the total output current (green) in the same phase when using coupled inductors. Scale: 3A/div.

those ripple are cancelled in the output current and become circulating current, which is reconstructed and shown in **Fig. 7.26**. The harmonic spectra of the total current and individual HSF module current shown in **Fig. 7.27** also confirm the efficacy of interleaving.

The measured waveform of CM voltage when modulation index is 0.9 is shown in **Fig. 7.28**. Its spectrum is presented in **Fig. 7.29**. It is clear that the dominant CM harmonics are around 120kHz as the harmonics around 60kHz are cancelled by interleaving.

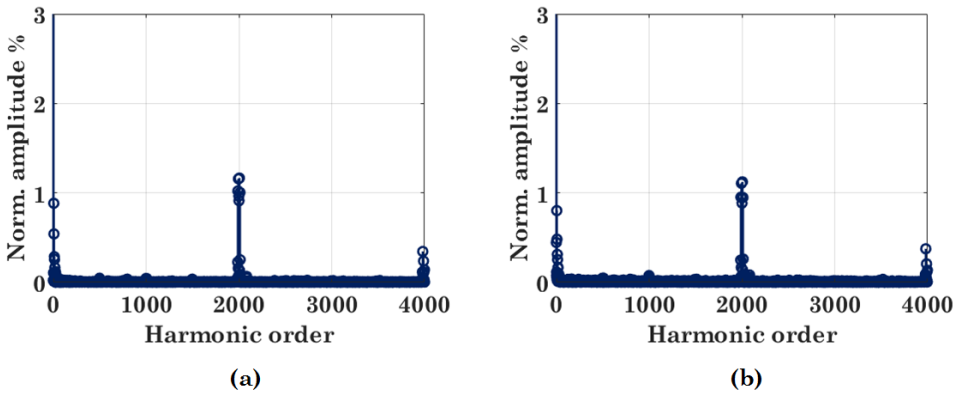


Figure 7.22. The spectra of (a) total output current and (b) individual HSF module output current when coupled inductors are applied.

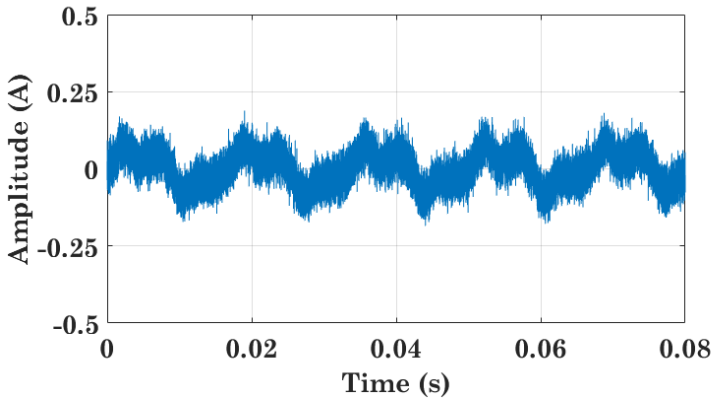


Figure 7.23. The waveform of circulating current when coupled inductors are applied. The waveform is reconstructed based on the waveforms of total current and individual HSF current in the same phase.

Experimental tests with single-phase operation were conducted in order to drive the output current to higher level and to present details on the output voltage waveforms. The waveforms with 2.3Ω load are shown in **Fig. 7.30**. As can be seen from the waveforms, when modulation index is 0.7, the total output voltage has seven voltage levels, whereas it becomes nine-level when modulation index is 0.9. In both cases, the output voltage of each HSF module is five-level. But due to the interleaving effect, the number of voltage levels in the total output voltage is increased. The spectrum of the output voltage when modulation index is 0.9 is shown in **Fig. 7.31**, confirming that the dominant harmonics are around 120kHz after interleaving.

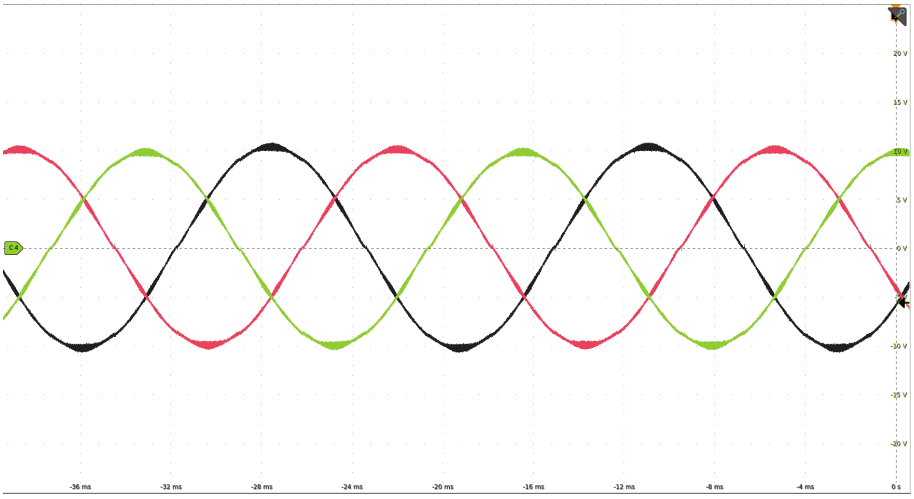


Figure 7.24. Measured three-phase total output current using single-phase inductors. Scale: 5A/div.

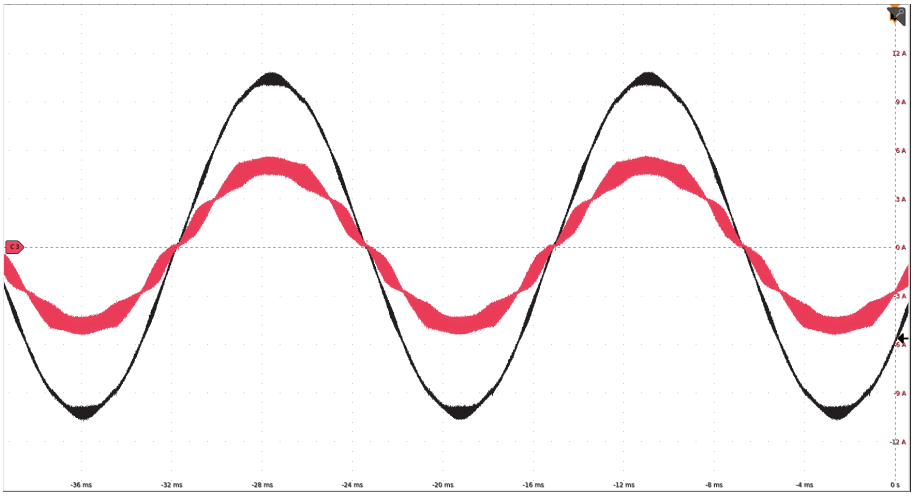


Figure 7.25. Measured output current of one HSF module (red) and the total output current (black) in the same phase when using single-phase inductors. Scale: 3A/div.

In the experimental voltage waveforms, voltage spikes can be observed at zero-crossing instants, as can be seen from **Fig. 7.30**. These voltage spikes are caused by the deadtime and can be explained with **Fig. 7.32**, which shows the switching pattern when the output voltage is crossing zero from the positive cycle to the negative half cycle. During this transition period, the turn-on of device S_2 and S_4 (see **Fig. 6.10**) is delayed due to the deadtime. In addition, the PWM pulse for device S_6, which ideally should exist, is missing because of the deadtime, since the duration of this pulse is too short at the zero-crossing

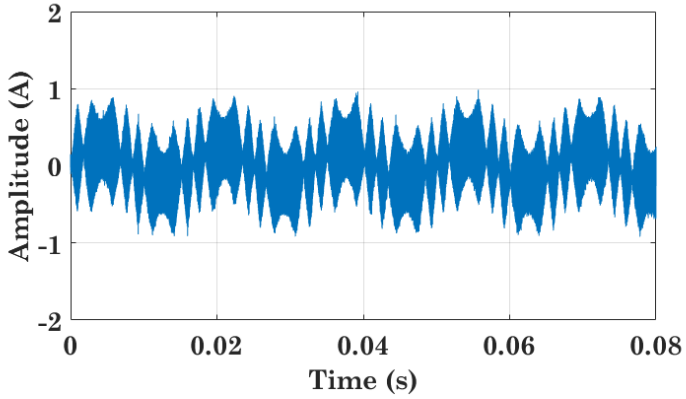


Figure 7.26. The waveform of circulating current when single-phase inductors are applied. The waveform is reconstructed based on the waveforms of total current and individual HSF current in the same phase.

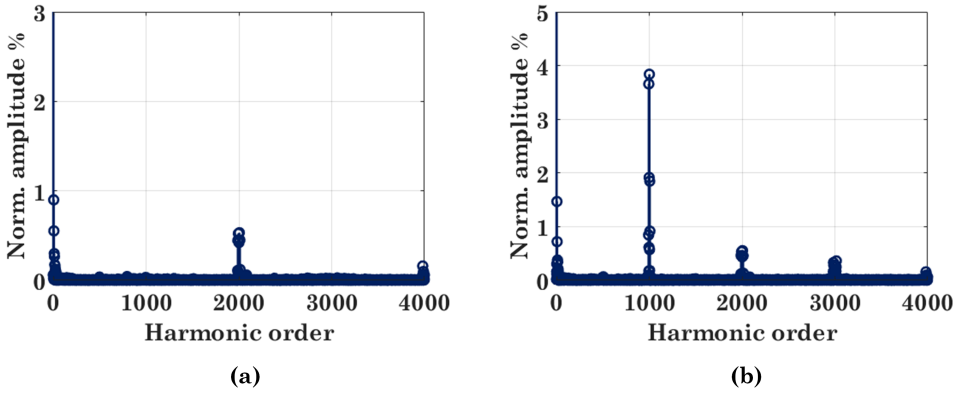


Figure 7.27. The spectra of (a) total output current and (b) individual HSF module output current with single-phase inductors.

point. As a result, during the deadtime, all LSF devices and the HSF devices S_5, S_6, and S_8 are off. Device S_7 may be off or on, depending on the position of the reference signal. However, the state of S_7 will not affect the result. Since the converter sees an inductive load (including the filter), the output current during the deadtime is still positive. As such, the current will flow through the anti-parallel diode of S_4, and the device S_7 (if it is off then it conducts current in diode mode) and S_8 (if an IGBT or a Mosfet is used, it is the anti-paralleled diode of S_8 that carries the current), leading to a voltage spike at $-V_{DC}/2$. When the voltage is crossing zero from negative cycle to positive cycle, the voltage spike will be at $V_{DC}/2$. Note that the maximum duration of

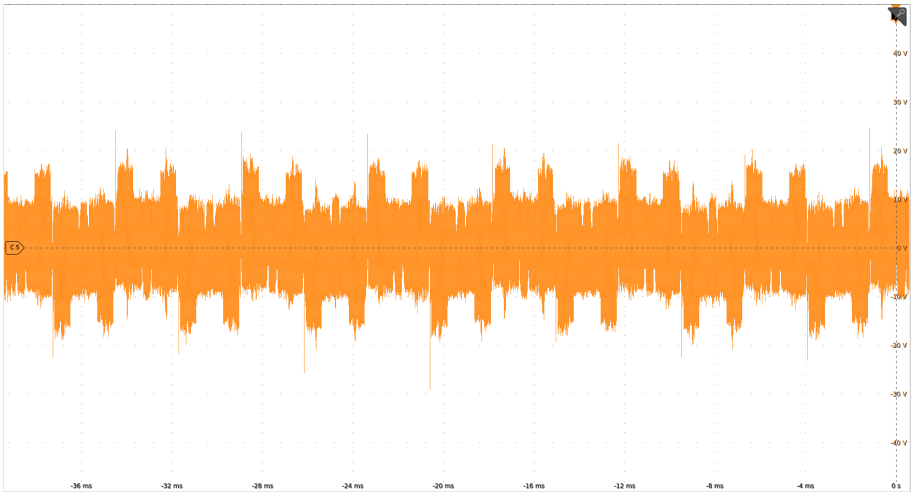


Figure 7.28. Measured CM voltage when modulation index is 0.9. Scale: 10V/div.

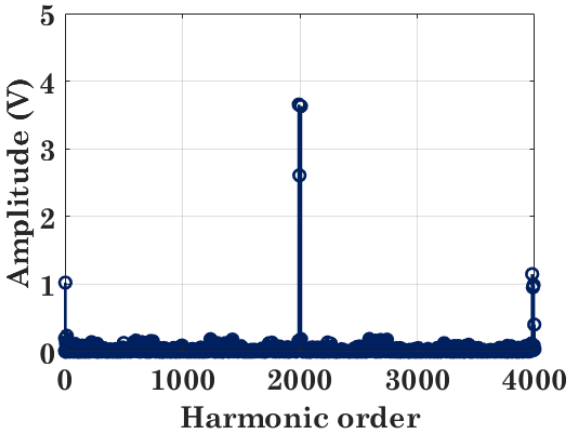


Figure 7.29. The spectra of the CM voltage when modulation index is 0.9.

the voltage spike is the length of deadtime. The zoomed-in waveform during zero crossing instant is shown in **Fig. 7.33**, where one can see that the duration of the voltage spike is very short since the deadtime is only 500ns in the experiment. Note that the waveform in the scope is updated from right to left. Therefore, the circled positive voltage spike is at a negative-to-positive zero-crossing instant.

For medium power applications with WBG devices, this voltage spike will not affect the output current quality since the deadtime is usually very short. However, in high power applications, the deadtime can be large, and as a consequence, the long voltage spike will distort the output current waveform.

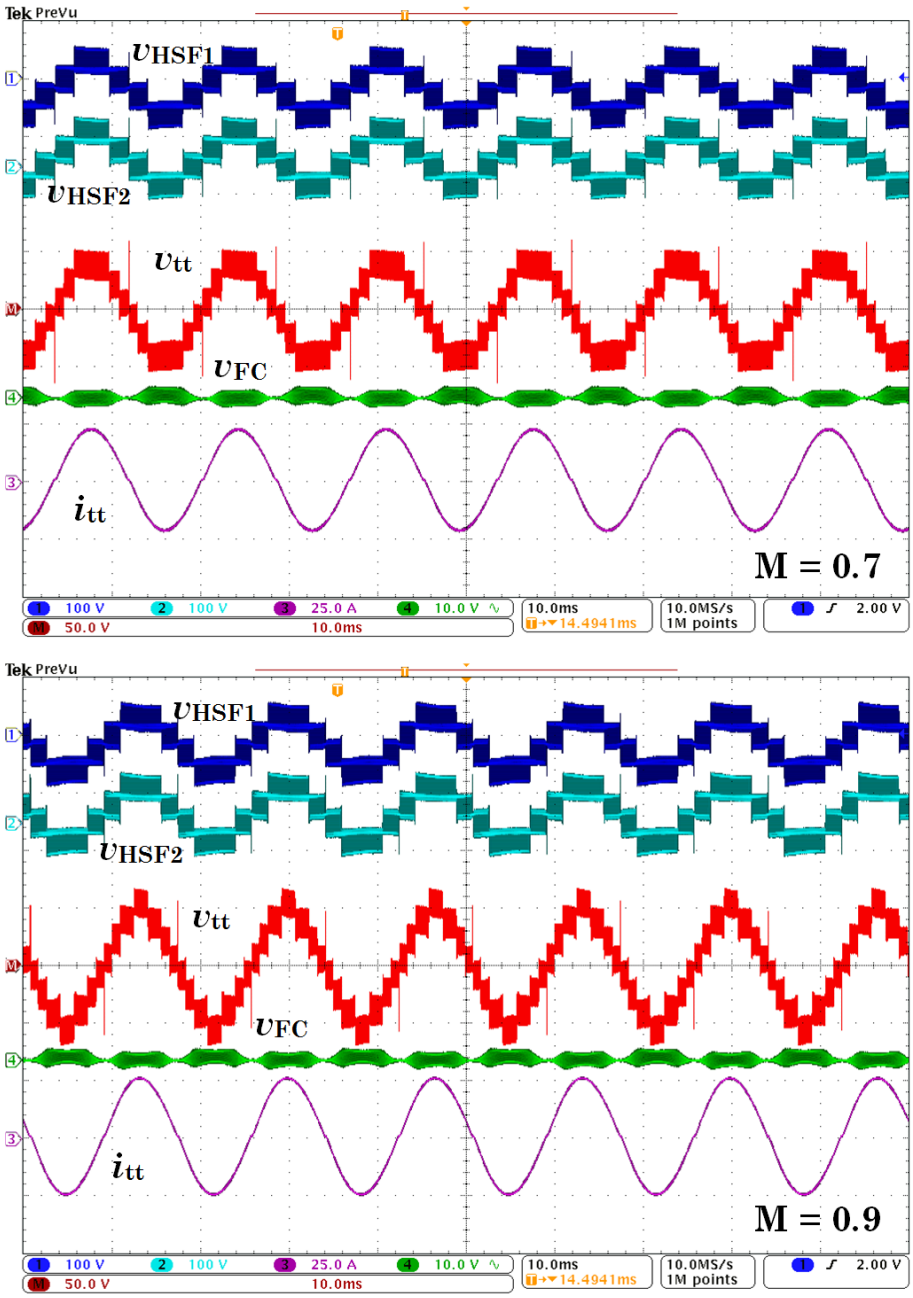


Figure 7.30. The measured waveforms of single-phase test. In the figure, v_{HSF1} and v_{HSF2} are the output voltage of two HSF modules (100V/div); v_{tt} is the total output voltage (50V/div); v_{FC} is the AC component of flying capacitor voltage (10V/div); and i_{tt} is the total output current (25A/div).

As such, this spike should be mitigated. In this regard, a feasible solution, which changes the turn-on or turn-off sequence of the LSF device and HSF device during the zero crossing period, has been proposed in [103]. The basic principle of this method is to switch the HSF devices before the LSF devices,

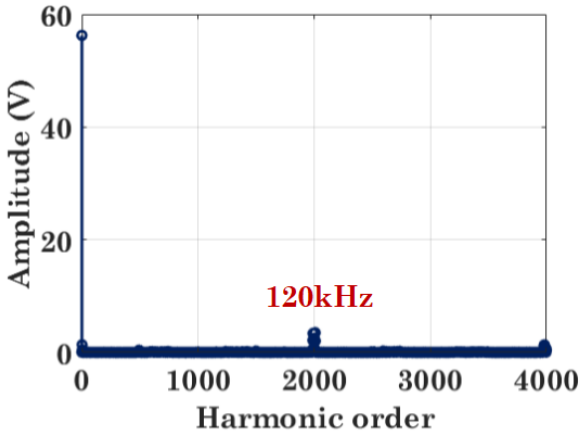


Figure 7.31. The spectra of total output voltage when modulation index is 0.9.

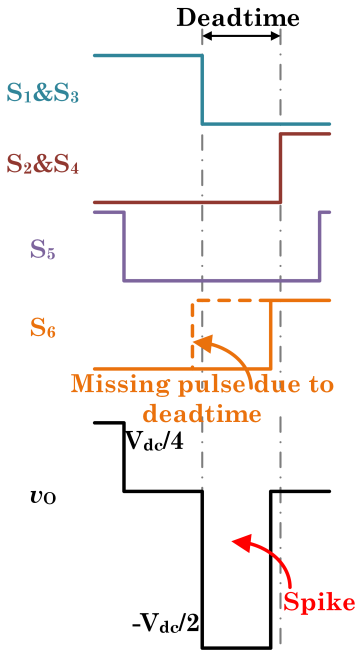


Figure 7.32. The switching pulse pattern when output voltage crosses zero level from positive to negative cycle.

such that at least two LSF devices are on and the output voltage at half DC link voltage can be prevented. To realize this, one can either delay the switching of the LSF devices by a period of deadtime, or use pre-programmed PWM patterns.

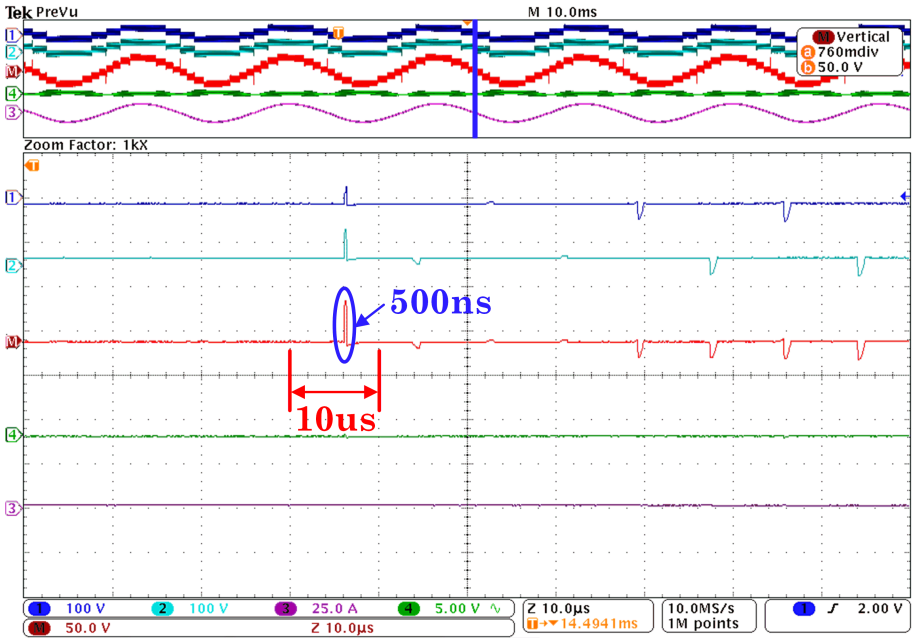


Figure 7.33. Zoomed-in view of voltage spike during voltage zero crossing. The time scale of one grid is 10us as indicated in the figure. The duration of the spike is less than 500ns.

7.4 Summary

The hardware design of a high density 70kW FC-IPC prototype is presented in this Chapter. The targeted application of the developed prototype is three-phase solar string inverter with 1500V DC input voltage. Comprehensive power loss modeling of the prototype is presented, upon which the thermal design is carried out. To minimize the temperature rise of the device, the IMS board is adopted for realizing the GaN HEMT based HSF modules. The estimation of the efficiency, sizing analysis of the FC bank, circuit layouts, and final assembly of the prototype are also presented in this Chapter. Lab-scale experimental verifications of the prototype have been conducted.

Chapter 8

Conclusions and Future Work

Modular parallel converter system, featuring the advantages such as modularity, fault tolerant capability, and efficiency improvements, has been widely applied in power electronics system designs. To further improve the performance of the parallel converters in grid-tied applications, interleaving of module converters has shown promising performances in terms of current quality improvement and power density improvement. However, these performance improvements may be undermined due to some challenging issues associated with interleaving. Two critical issues are the common mode circulating current (CMCC) which requires large common mode (CM) choke to suppress and the LCL filter resonance induced issues. The development of this thesis is focused on addressing the existing key challenges and also further improving system performance based on new system design concept and novel multilevel converter topologies.

8.1 Thesis Conclusions

To provide a tool for analyzing modular parallel converter system with any number or type of converters, this thesis first looks into the modular parallel converters in the frequency domain based on the generalized harmonic distribution analysis approach established in Chapter 2. Regardless the type of the converter (two-level or multilevel), the analysis reveals that the frequency-domain relationship among the output voltage, CM voltage, and circulating current, which are the three independent performance indices. The analysis

also indicates that the distribution of the harmonics in above three indices can be manipulated by employing the generalized modulation schemes where each phase of a converter is assigned an independent carrier signal. This generalized modulation scheme offers an additional degree-of-freedom for system design, and for the interleaved converters, 2 degrees-of-freedom (i.e. the carrier phase shift angle among the converters and the carrier phase shift angle within each converter) are available. By altering the phase angle of the carriers, the harmonic energy distribution among the three indices can be altered. The benefits of doing this can be perceived from the filter design point-of-view. The basic rule-of-thumb is that the size of a filter is in a positive relationship with the harmonic energy processed by it. In the particular case of the modular parallel converters studied in this thesis, setting the proper carrier phase angle to each phase of a converter module can reduce the harmonic energy processed by the CM choke, and thereby reduce its size.

Based on the harmonic distribution analysis, a new interleaving scheme, i.e. 2DoF interleaving scheme, is proposed in this thesis for minimizing the CMCC peak value of modular interleaved converters regardless the number of converters. The efficacy of the 2DoF interleaving scheme in reducing CMCC of two-level converter and three-level converter based systems is verified in Chapter 3 and Chapter 4 respectively. The reduction of CMCC allows the parallel converters to employ interleaving technique with improved power density. Further investigation of the application of 2DoF scheme in high-level converters suggests non-significant performance improvement due to the wide adoption of phase-shift PWM in high-level converters. Therefore, the 2DoF interleaving scheme is only recommended for two-level converter or three-level converter based modular parallel converter systems.

Leveraging the interleaving technique, a new L filter based system level design approach is proposed in Chapter 5 to eliminate the necessity of using LCL filter, and thereby eliminating the known and potential filter resonance related issues. A comprehensive investigation involving two-level and multi-level converters reveals that the the minimum number of converters that can meet the grid code is not related to the specific system parameters like switch-

ing frequency or power rating. Rather, it is only determined by the converter side current ripple ratio and the harmonic amplitude resultant from a certain PWM strategy. With 50% converter side current ripple ratio, the number of required converters is 5 or 6 regardless the level of the converter. The efficacy of the proposed design approach is validated with benchmark based simulation.

The analysis in Chapter 5 suggests that adopting higher-level converter can reduce the size of filter inductors. However, the non-modular structure and the other weaknesses of existing high-level topologies have limited their practical values. To derive practical high-level and modular topologies, a new multilevel converter topology synthesis concept, the internal parallel converter (IPC), is proposed. The concept incorporates the parallel modularity inside the multilevel converter. Different from the existing topologies, the IPC topologies feature the merits such as flexible device selection, reduced device current stress, availability of modularity and redundancy, simple modulation and control requirements, and potential efficiency and power density improvements. The implementation of interleaving technique will also help to reduce the filter size as compared to the conventional topologies.

The design and development of a high density GaN and IGBT based FC-IPC prototype is presented in Chapter 7. It is shown that with the FC-IPC topology, 650V/60A GaN HEMT, which conventionally is only used in low DC input voltage and low power applications, can now be applied in a 1500V input 70kW level PV string inverter. Taking advantage of the high frequency switching capability of GaN, the power density of the inverter can be substantially improved. With suitable thermal and hardware design, the power density of the developed prototype can reach 12kW/L with high efficiency (estimated peak efficiency is over 99.2%).

8.2 Outlook and Recommendations for Future Work

Shifting towards a more efficient society demands the widespread use of power electronics systems in both power generation and consumption ends. In the

future electricity grid, there will be large amount of grid-tied converters serving as the interlinking systems between AC and DC micro-grid, as grid-interface of renewable energy resources or storage elements, as power supplies for various kinds of loads, etc. With such increased demand of power electronics in the utility grid, it is necessary to rethink the design of power electronics system. In both converter level and system level, it is envisioned that the modular parallel converter system will become an ideal candidate to achieve robust control and ultra-high efficiency, density, and reliability. Tradition single full power converter with medium and high power capacity can be built with extreme modularity, as indicated in Chapter 5.

In addition, high-level converters will keep finding new places in low voltage applications where currently two-level and three-level converters have been prevailing. In some applications, e.g. solar farm, single converters with separate DC links are paralleled. To ensure system robustness, each single converter should be able to satisfy the grid code by using small size L filter. In this regard, the IPC concept can be a promising solution. The power density improvement brought by the IPC topologies will also reduce the installation and maintenance cost, shortening the payback period of renewable energies.

Above outlook pictures a bright future of the modular parallel converter system in both system level and converter level implementations. To further enhance the performance, there are also many potential research topics that can be explored in the future.

1. Full scale tests of the designed high density converter with 1500V DC input and 70kW output will be carried out to fully verify the design.

2. Practical implementations and field tests of the L filter based modular parallel converter system in applications such as active frond end (AFE) of low voltage drives should be conducted in the near future.

3. In this thesis, unbalanced grid voltage condition is not considered. For modular parallel converters based grid-tied system, the CMCC issue and related control techniques under unbalanced grid voltage condition will be interesting topics that worthy of future exploration.

4. Parallel modularity enables flexible power and energy management for applications like smart-grid. An optimal system level design can be carried out considering both hardware design and system management. Integrating more functions, such as virtual synchronous generator, into the parallel converters will also be an interesting research topic.

5. The modular nature of modular parallel converter system as well as the internal-parallel converters desires integrated design of modules (converter module or high switching frequency modules in IPC). In this regard, power electronics building block (PEBB) concept could be implemented. A more advanced topic involves the power module packaging technology.

6. Thermal management design is an essential part when designing a power converter. As indicated in Chapter 7, the fans in a forced air cooling system have nontrivial power loss. It may also affects the reliability of the system if the targeted applications in harsh environment. Therefore, thermal management design that allows natural cooling will have important practical value.

7. Besides the grid-tied applications, modular parallel converters as well as the internal-parallel converters are applicable in industry and electric vehicle motor drives. Optimal integration and co-design of the converters and multi-segment motor will be an exciting topic.

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Appendix A

Common Mode Choke Size Analysis

In most power electronic systems, the common mode (CM) choke is normally required to attenuate the CM leakage current, EMI, or other CM voltage induced issues. In the modular parallel converters, the CM choke is usually applied to suppress the common mode circulating current (CMCC). With higher CMCC, larger CM choke will be required, undermining the power density and increasing the cost of the system. A simplified CM choke scaling analysis is introduced here to show the importance of CMCC reduction.

The three-phase CM choke is used as an example here. The symbol of an ideal CM choke, ignoring the winding capacitance and the equivalent series resistance, is shown in **Fig. A.1 (a)**, with i_A, i_B, and i_C standing for the three-phase currents. Correspondingly, the The typical structure of a three-phase CM choke is shown in **Fig. A.1 (b)** and **(c)**. As can be seen, all three windings are wound over the same toroidal core. The cross-sectional area of the core is denoted as A_c, and the diameter of the core is d_c. Also, the number of turns in the winding of each phase is denoted as N_c.

Ideally, the sum of the three-phase currents should be zero in a balanced system. However, due to the presence of CM voltage and other parasitic issues (e.g. grounding capacitance), the sum of three-phase currents will be an non-zero CM current, which is denoted as i_{CM} here. In a modular parallel converter system with interleaved operation, i_{CM} will be the CMCC. The CM current will induce a CM flux, Φ_{CM}, inside the core, as shown in **Fig. A.1**

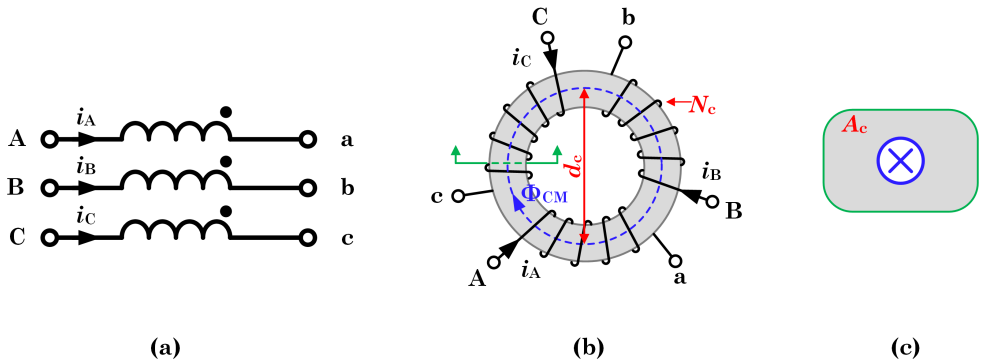

Figure A.1. The three-phase CM choke, (a) symbol of an ideal CM inductor, (b) shape, winding configuration and the magnetic flux inside the core, and (c) cross-sectional view of the core.

(b). To prevent from saturation, the resultant CM flux density, B_{CM} must be smaller than the saturation density of the core, B_{sat}. In general, higher i_{CM} will induce larger Φ_{CM}, and thus larger B_{CM} for a given A_c. If B_{CM} becomes larger than the saturation limit of the core, A_c must be increased, resulting in an increased CM choke size.

A clear relationship between i_{CM} and the CM choke size can be analyzed as follows. The CM inductance, L_{CM}, is determined by the parameters of the choke as given in (A.1).

$$L_{CM} = \frac{N_c^2 \cdot \mu \cdot A_c}{\pi \cdot d_c} \tag{A.1}$$

where μ is the permeability of the core material. To avoid core saturation, the maximum ratio of the maximum CM current, $i_{CM,max}$, and the core diameter d_c must satisfy (A.2) defined according to the Ampere's Law [58].

$$\left(\frac{i_{CM,max}}{d_c}\right)_{\max} < \frac{\pi}{N_c} \cdot \frac{B_{sat}}{\mu} \tag{A.2}$$

To achieve the same L_{CM} with the same core material (B_{sat}) and N_c, smaller $i_{CM,max}$ leads to reduced d_c, as indicated by (A.2). Moreover, based on (A.1), A_c can also be reduced with d_c to keep L_{CM} unchanged. The volume of a toroidal CM choke, $\mathrm{Vol_{CM}}$, is given by (A.3), indicating that if $i_{CM,max}$ can be reduced without increasing L_{CM}, smaller CM choke can be used.

$$\mathrm{Vol_{CM}} = \pi d_c A_c \tag{A.3}$$

Above analysis also shows that the volume of the CM choke is proportional to the second power of the maximum CM current $i_{CM,max}$, as expressed in (A.4). That said, 50% reduction of $i_{CM,max}$ will lead to quadruple reduction of the CM choke size.

$$\mathrm{Vol_{CM}} \propto i_{CM,max}^2 \tag{A.4}$$

Appendix B

Common Mode Offset Signals for Different PWM Schemes

Common mode offset (CMO) offset signal is usually required in practical applications to efficiently utilize the DC link voltage. With CMO signal injected, a carrier-based PWM scheme becomes equivalent to a space vector modulation (SVM) scheme. This signal is only determined by the three-phase references, and will not be affected by the carrier configuration. As such, the CBPWM, e.g. the S2DoF interleaving scheme described in section 3.1, can have the same practical value as SVM based strategies, while keeping the flexibility in carrier configuration. For different type of converters, the injected CMO signal can be different. The realization methods of the CMO signals for two-level (2L) VSC is introduced in section B.1. The signals that can be applied with the three-level (3L) level-shift PWM schemes (i.e. PD and POD) are presented in section B.2

B.1 CMO Signal for Two-Level Converter

For a two-level (2L) converter, two types of CMO signals can be injected to the sinusoidal reference waveforms, i.e. the continuous type and the discontinuous type. Both will be introduced in this section. In the following, M_A, M_B, and M_C denote the original sinusoidal reference waveforms in phase A, B, and C, and $\hat{M}_A$, $\hat{M}_B$, and $\hat{M}_C$ are the modified three-phase reference waveforms after

injecting the CMO signal, as given by (B.1).

$$\begin{aligned} \hat{M}_A &= M_A + \text{CMO} \\ \hat{M}_B &= M_B + \text{CMO} \\ \hat{M}_C &= M_C + \text{CMO} \end{aligned} \tag{B.1}$$

B.1.1 Continuous Type CMO

With the continuous type CMO, the original sinusoidal PWM (SPWM) strategy becomes equivalent to the conventional seven-segment space vector PWM (SVPWM) [70], which is the most popular modulation strategy for a 2L converter. In a digital processor, e.g. DSP, the continuous type CMO can be obtained from the instantaneous values of original modulating signals with the calculation method in (B.2).

$$\text{CMO} = -\frac{1}{2}\left[\max\left(M_A, M_B, M_C\right) + \min\left(M_A, M_B, M_C\right)\right] \tag{B.2}$$

The sinusoidal reference signals and the resultant continuous type CMO signal are presented in **Fig. B.1 (a)**. After injecting the CMO signal into the sinusoidal references, the modified modulation signals are shown in **Fig. B.1 (b)**.

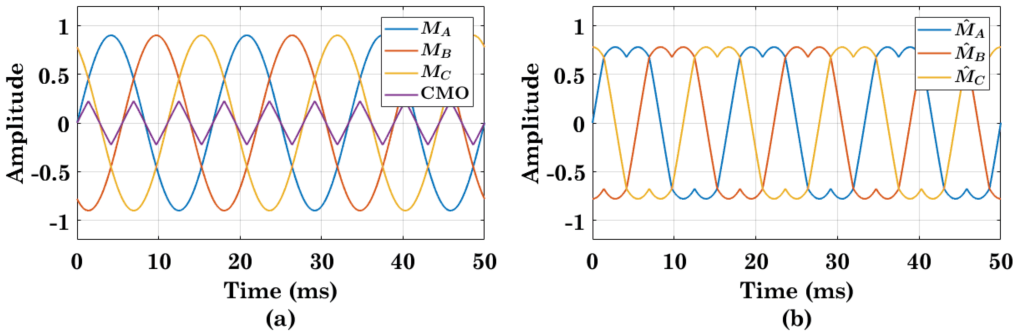

Figure B.1. Modulation scheme based on the continuous type CMO, (a) original references and the CMO signal, (b) the modified modulation signals. Waveforms are obtained with modulation index at 0.9.

B.1.2 Discontinuous Type CMO

The main feature of the discontinuous type CMO is that the modified references will be clamped at the upper and/or lower band of the carrier signal to make the PWM pulses suspended for a period of time. In literature, several variations of the discontinuous type CMO signals have been reported to get discontinuous PWM (DPWM) strategies with different pulse suspension period and/or the polarity [70]. The DPWMMIN the DPWMMAX methods will clamp the references to the lower and upper band, respectively, for 1/3 of the fundamental period [77]; whereas the DPWM1 and DPWM2 methods can clamp the references (with different waveform shape) to each band for 1/6 of the fundamental period [76]. Among these methods, the DPWM1 is the most representative one and has been widely applied in practice. The injected CMO signal for DPWM1 can be calculated with (B.3). The resultant modulation scheme is shown in **Fig. B.2**.

$$\text{CMO} = sign\left[\max\left(M_A, M_B, M_C\right)\right]\left(\frac{1}{2}\right) - \max\left(M_A, M_B, M_C\right) \tag{B.3}$$

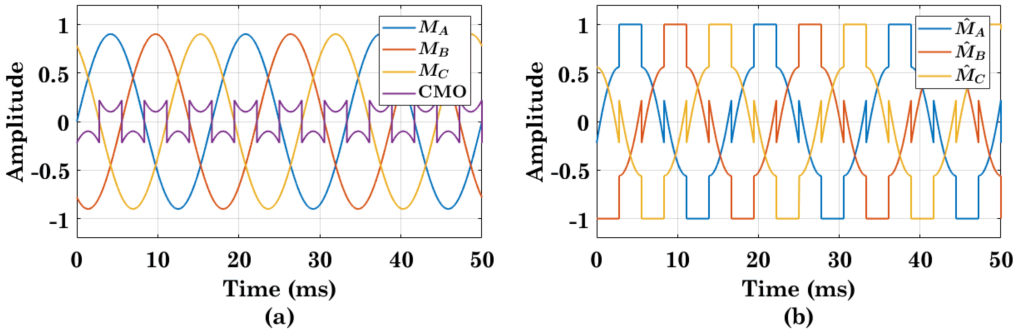

Figure B.2. Modulation scheme based on the discontinuous type CMO, (a) original references and the CMO signal, (b) the modified modulation signals. Waveforms are obtained with modulation index at 0.9.

B.2 CMO Signal for Three-Level Converters

In three-level and high-level converters, the CMO signals for two-level converters are still applicable, and desirable particularly when PS-PWM is applied. Besides these two CMO signals, there are other CMO signals, including both

continuous type and discontinuous type, specialized for level-shift PWMs [78]. The implementations of both CMO signals need to find M_{max}, M_{mid}, and M_{min}, as given in (B.4) and the intermediate reference signals as given in (B.5). Note that in unbalanced output condition, M_{mid} may also be found through a sorting operation of the references.

$$\begin{aligned} M_{max} &= \max\left(M_A, M_B, M_C\right) \\ M_{min} &= \min\left(M_A, M_B, M_C\right) \\ M_{mid} &= -(M_{max} + M_{min}) \end{aligned} \tag{B.4}$$

$$\begin{aligned} M'_{max} &= M_{max} - \frac{1}{2} \\ M'_{min} &= M_{min} + \frac{1}{2} \\ M'_{mid} &= \begin{cases} M_{mid} + \frac{1}{2} & \text{if} M_{mid} < 0 \\ M_{mid} - \frac{1}{2} & \text{if} M_{mid} \geq 0 \end{cases} \end{aligned} \tag{B.5}$$

To find the continuous type CMO, the intermediate references then sorted again to produce the final CMO signal based on (B.6), which is in a similar way as in (B.2). The resultant CMO signal and reference waveforms are shown in **Fig. B.3**.

$$\text{CMO} = -\frac{1}{2}\left[\max\left(M'_{max}, M'_{min}, M'_{mid}\right) + \min\left(M'_{max}, M'_{min}, M'_{mid}\right)\right] \tag{B.6}$$

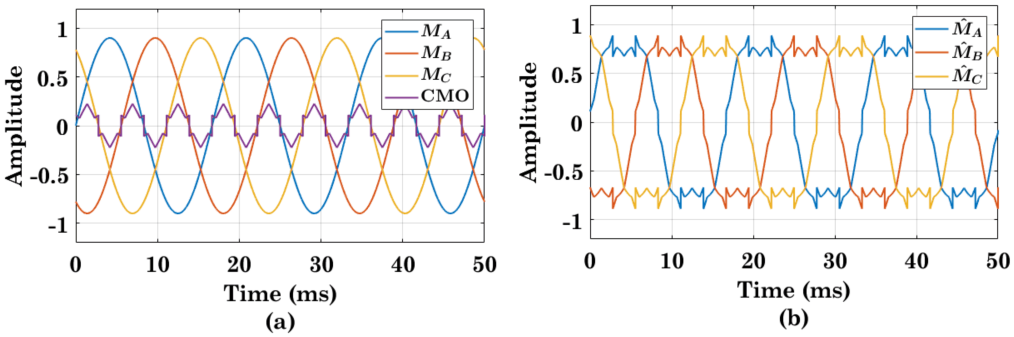

Figure B.3. Continuous type modulation references for a three-level converter, (a) original references and the CMO signal, (b) the modified modulation signals. Waveforms are obtained with modulation index at 0.9.

The discontinuous type CMO can be found based on the algorithm provided in (B.7). The resultant CMO signal and reference waveforms are shown in **Fig. B.4**.

$$\text{CMO} = \begin{cases} -\frac{1}{2} - \min\left(M'_{max}, M'_{min}, M'_{mid}\right) & \text{if} M_{mid} \geq 0 \\ \frac{1}{2} - \max\left(M'_{max}, M'_{min}, M'_{mid}\right) & \text{if} M_{mid} < 0 \end{cases} \tag{B.7}$$

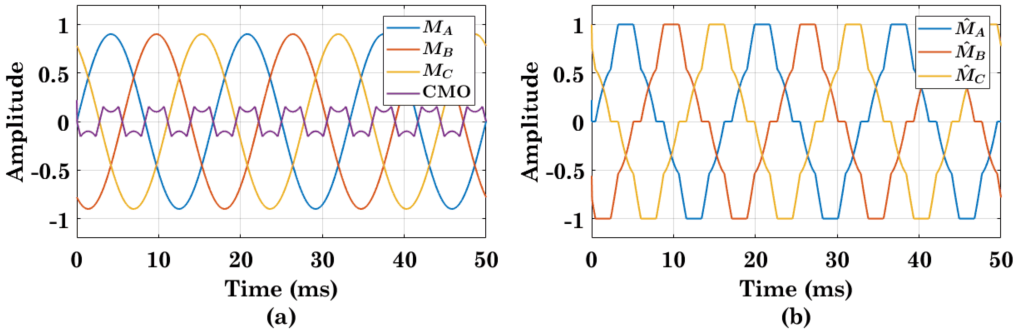

Figure B.4. Discontinuous type modulation references for a three-level converter, (a) original references and the CMO signal, (b) the modified modulation signals. Waveforms are obtained with modulation index at 0.9.

Appendix C

System Design of Parallel Converters with Separate DC Links

Besides parallel converters with common DC bus, those with separate DC links, as illustrated in **Fig. C.1 (a)**, are also popular in applications such as AFE based low voltage drive and string inverter based solar farm. Conventionally, the output of each converter module is filtered by an LCL filter, which induces instability issues in the control loop, though the DC links are separated. Therefore, replacing the LCL filter with only L filter through interleaving the converter modules is also a promising approach for such system, especially considering that the separate DC links will naturally eliminate the common mode circulating current (CMCC). With only L filter, the configuration of each converter module is shown in **Fig. C.1 (b)**, where the common mode (CM) choke may still be required to suppress any CM noises or leakage current. Also, since CMCC is eliminated, it is unnecessary to adopt CS2DoF modulation, and thus only CS1DoF scheme is considered in the following analysis.

Since the CMCC is eliminated, the converter side current ripple of a 2L converter module, $\Delta I_{pp,SDC}$, becomes (C.1), which is the same as that with LCL filter.

$$\Delta I_{pp,SDC} = \frac{V_{DC,nom}}{6L_{c,SDC,2L}f_s} \tag{C.1}$$

where 'SDC' stands for the separate DC links, $V_{DC,nom}$ is the nominal DC

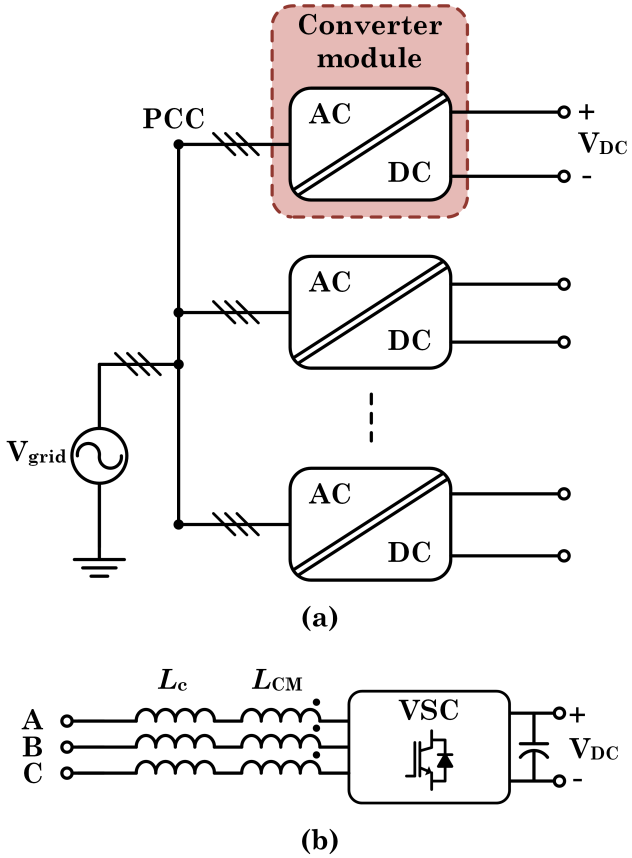

Figure C.1. Parallel converters with separate DC links, (a) the general structure; (b) the configuration of one converter module with only L filter.

link voltage of the system, $L_{c,SDC,2L}$ is the filtering inductance in one converter module, and f_s is the carrier frequency. Following the same analyzing procedure as in Chapter 5, the number of converters that can ensure grid code-compatible output current can be determined by (C.2), assuming all converters have the same DC link voltage, which is $V_{DC,nom}$ in an ideal case.

$$N_{SDC} \geq 318.31 K_{rp} \lambda_N \tag{C.2}$$

The harmonics in the output voltage of interleaved converters are irrelevant to the DC link configuration. That said, the results in **Table 5.3** are also applicable, and repeated here in **Table C.1** with N extended to 7. Substituting the values in **Table C.1** reveals that the required N is 7 when K_{rp} is 50%. Compared to the results in Chapter 5, the increase in N is caused by the reduction of filter inductance when the DC links are separate.

Table C.1. The values of λ_N with respect to N for CS1DoF scheme.

N	2	3	4	5	6	7
λ_N	0.196	0.0732	0.0982	0.0439	0.0565	0.0314

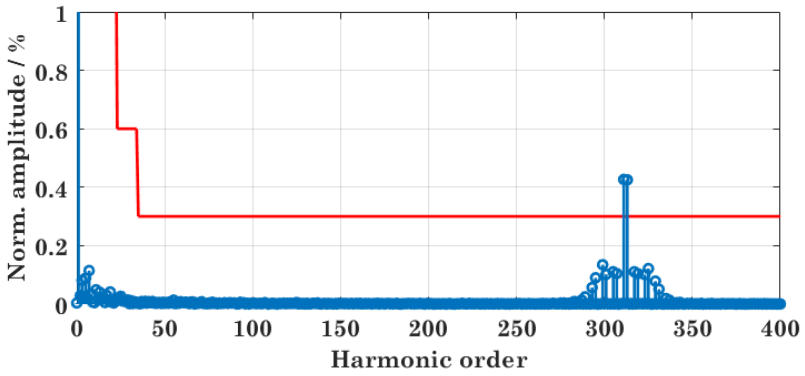

Figure C.2. Harmonic spectrum of i_{PCC} resultant with 6 interleaved 2L converters with separate DC links. The red line indicates the limits of odd order harmonics set by standard IEEE519.

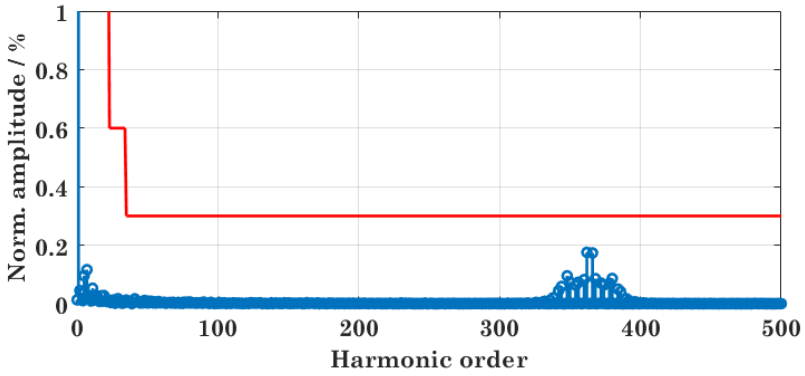

Figure C.3. Harmonic spectrum of i_{PCC} resultant with 7 interleaved 2L converters with separate DC links. The red line indicates the limits of odd order harmonics set by standard IEEE519.

Based on the same benchmark parameters in Chapter 5, the simulated spectra with $N = 6$ and $N = 7$ are shown in **Fig. C.2** amd **Fig. C.3** respectively. Note that the results are obtained with $K_{rp} = 50\%$. If $K_{rp} = 30\%$ is adopted, $N = 6$ will be sufficient to meet the grid code. Since the design criteria of the L filter is the same as that of the converter side inductor in an LCL filter, the filter size can be reduced as the grid side inductor in the LCL filter becomes unnecessary.

Appendix D

Generalized Embodiments of Internal Parallel Converters

Besides the basic embodiments introduced above. There are other embodiments and implementations can be adopted. The generalized embodiments of HB-IPC and FC-IPC are shown in **Fig. D.1**. Besides driving conventional three-phase motor and generator, the proposed IPC topologies are also suitable for driving multi-segment motor or generator. As the stator windings are completely isolated in multi-segment motor [33], circulating current will not be an issue, and interleaving of HSF modules can be easily applied to provide further performance improvement. In **Fig. D.2**, two-segment motor drives based on the HB-IPC converter and the FC-IPC converter are shown as examples. Finally, the IPC topologies can also be implemented in single phase condition, as shown in **Fig. D.3**. By connecting the single phase embodiments in **Fig. D.3** in cascaded H-bridge (CHB) configuration, new CHB topologies with parallel connectivity and enhanced fault tolerant capability can be obtained, as shown in **Fig. D.4**. The new CHB topologies are potential candidate for high-power medium voltage drives. Note that in this case, synchronizing the HSF modules may be a better option.

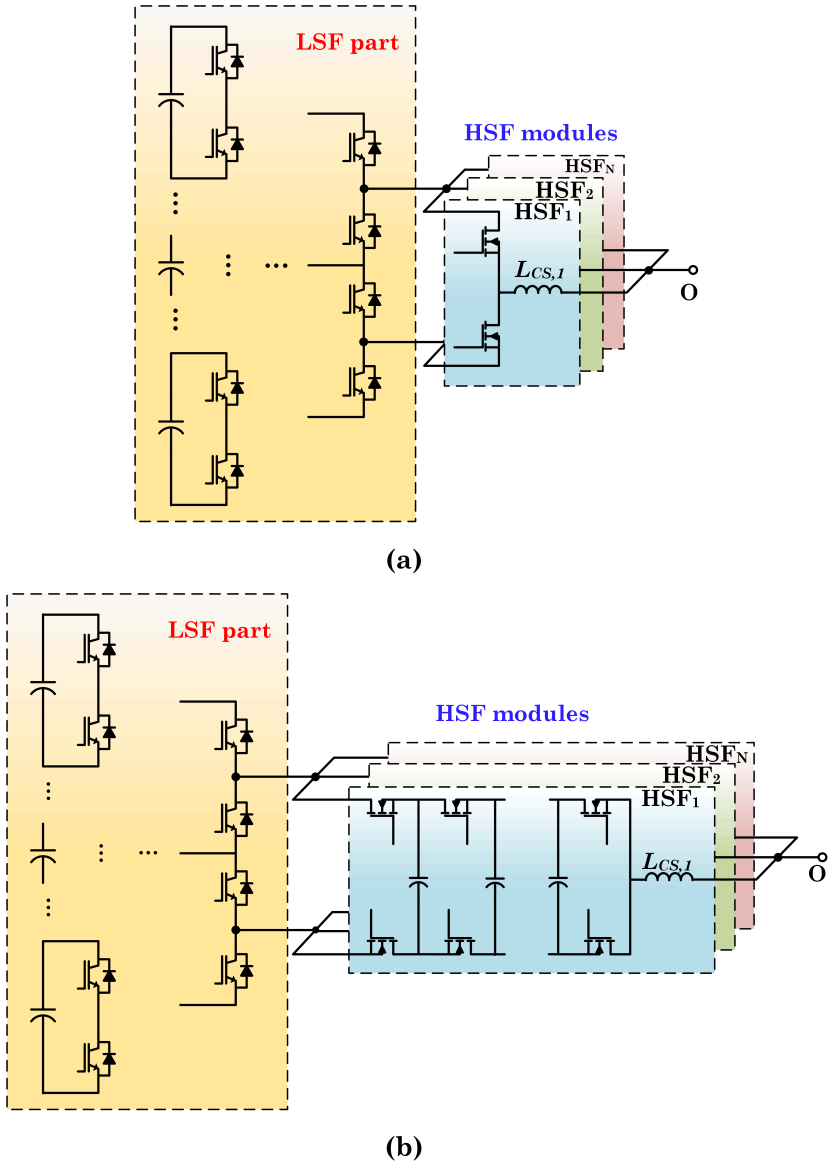

Figure D.1. The generalized IPC topologies, (a) HB-IPC and (b) FC-IPC. The HB-IPC can only be generalized from the DC side, whereas the FC-IPC can be extended from both or either of DC and AC side. By introducing additional neutral points at the DC link, active balancing of the neutral points voltages must be applied.

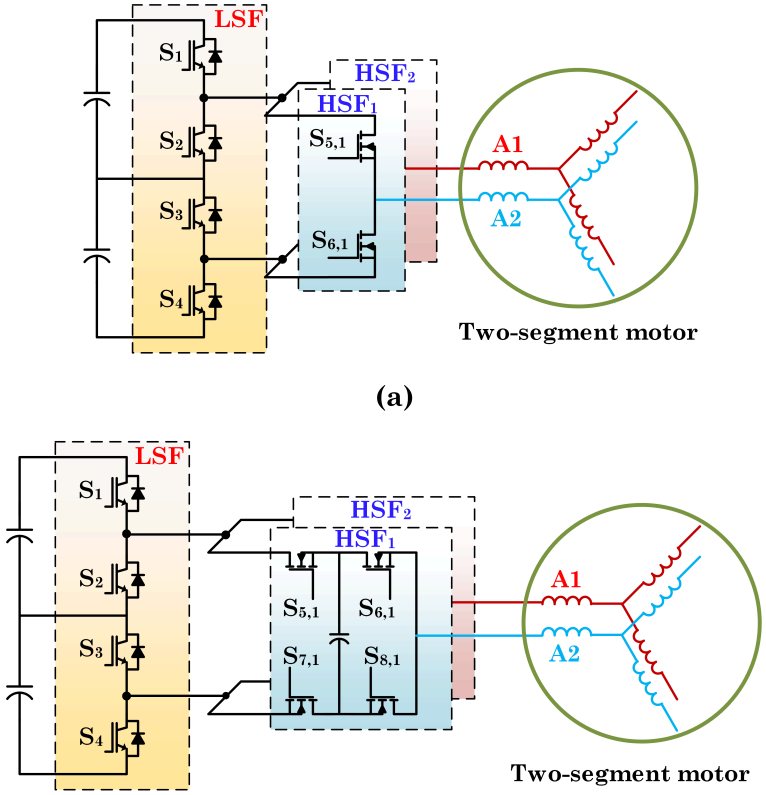

Figure D.2. Multi-segment motor drive with (a) HB-IPC and (b) FC-IPC. An example with two-segment motor is shown. With IPC based drive, the stator windings in the same phase should have the same phase angle to ensure proper operation. As the stator-sets are electrically and magnetically isolated with each other, no circulating current will present. Thus, interleaving is preferred for torque ripple, noise, and vibration reduction.

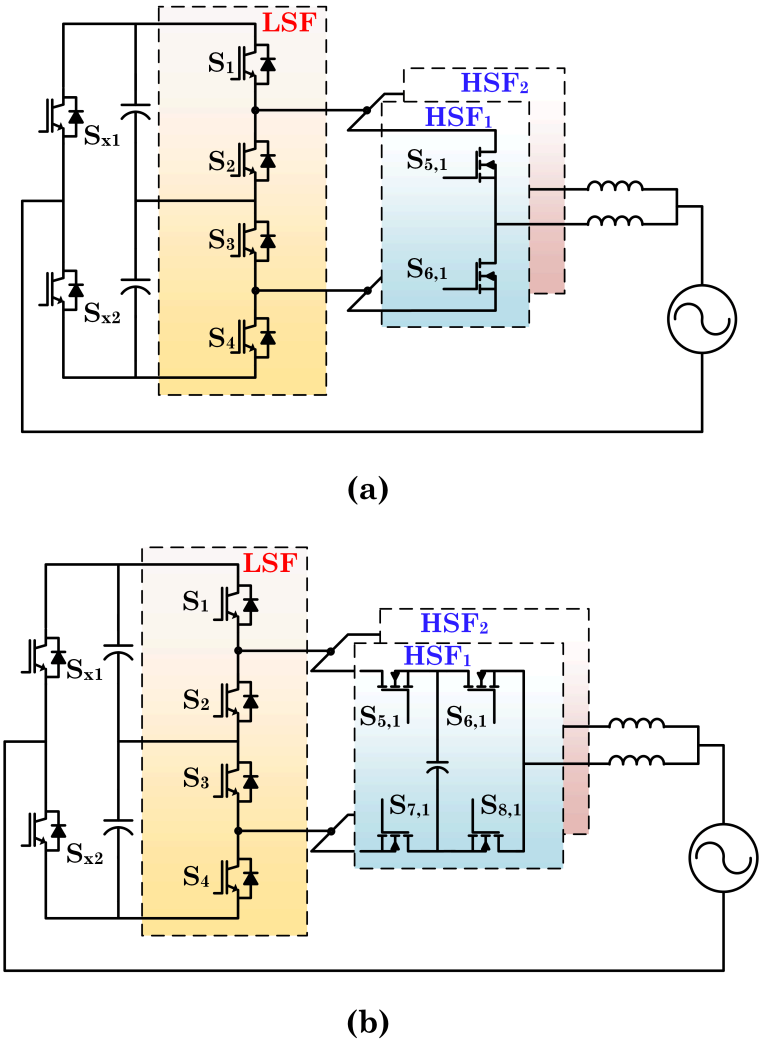

Figure D.3. New single phase topologies based on (a) HB-IPC and (b) FC-IPC. The extra devices S_{x1} and S_{x2} are switching at the fundamental frequency, but need to block the full DC link voltage.

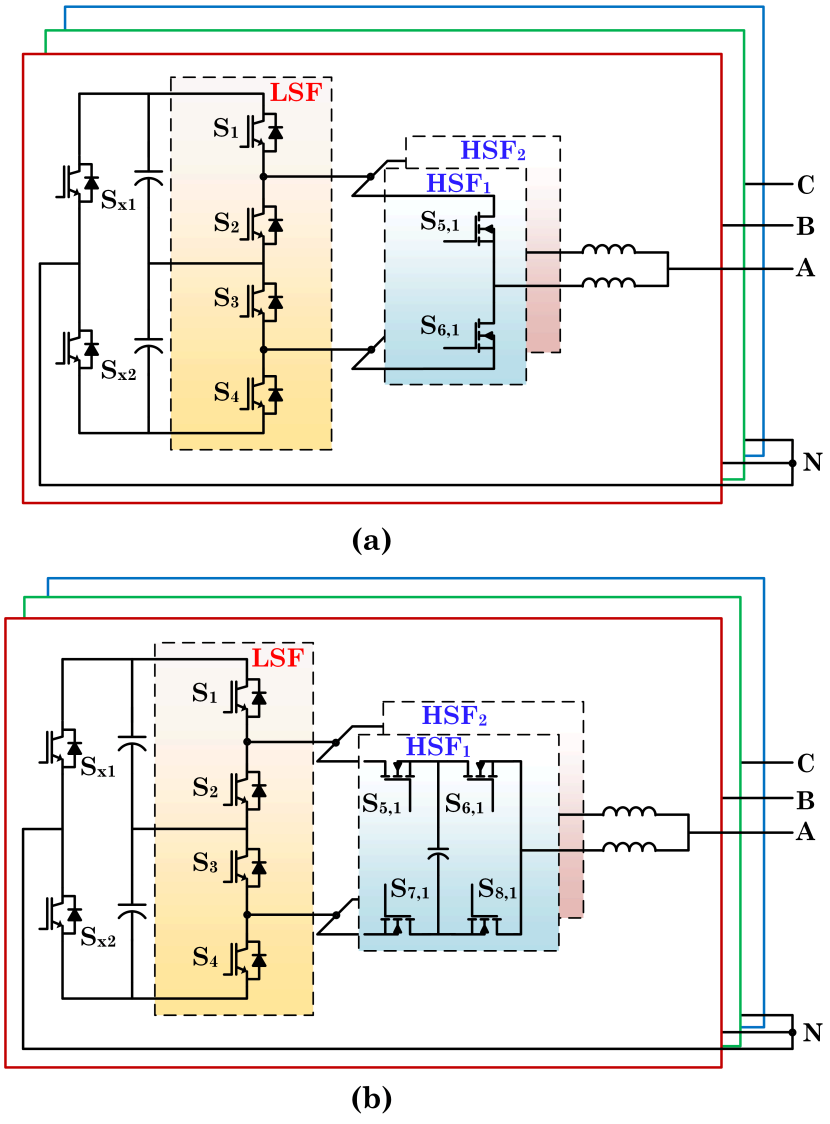

Figure D.4. New type of CHB topologies based on (a) HB-IPC and (b) FC-IPC.