Real-Time MPSoC-Based Electrothermal Transient Simulation of Fault Tolerant MMC Topology

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***Abstract*—Among different modular multilevel converter (MMC) submodule (SM) topologies, the clamp double submodule (CDSM) has the capability of dc fault current limiting and utilizes a relatively small number of switching devices. Since CDSM has a more complex circuit structure than half-bridge or full-bridge SM, it is a significant challenge for the real-time electromagnetic transient (EMT) simulation for a multiterminal dc (MTDC) system containing CDSM MMC. This paper proposes the device-level electrothermal model of CDSM for real-time EMT simulation, which can accurately present the power losses, the junction temperatures, and the switching transient waveforms of individual switches consuming more computation resources. The individual insulated-gate bipolar transistors of the CDSM MMC during fault clearance transient are evaluated from both electromagnetic and thermal perspectives, which interact with each other dynamically. To ensure the real-time performance of the proposed model, the equivalent circuit model is combined with the device-level model. The system-level and device-level waveforms during normal operation and dc fault transient for a three-terminal dc system are both presented and compared with PSCAD/EMTDC and SaberRD. The simulation system was implemented on the Xilinx Zynq UltraScale+ ZCU102 multiprocessor system-on-chip (MPSoC) platform, and the results were captured by the oscilloscope in real-time.**

***Index Terms*—Clamp double submodule (CDSM), electrothermal model, modular multilevel converter (MMC), multi-terminal DC (MTDC) system, real-time systems, multi-processor system-on-chip (MPSoC).**

I. Introduction

HIGH voltage DC transmission (HVDC) has been widely used for long-distance bulk power transfer due to its low power losses, low overall investment, and high controllability [1], [2]. When integrating renewable energy sources, such as off-shore wind power plant, HVDC transmission is the preferred option due to the feasibility of long-distance DC cable. Modular multi-level converter (MMC) is a promising technology for the converter stations, due to its low switching frequency, low power losses, and low harmonics. A major challenge of implementing multi-terminal DC (MTDC) system is the strict demand of safe operation under contingencies, especially the DC side fault, which can lead to a complete malfunction of the MTDC system and cause severe damage to the converter stations [2]. Besides the usage of the DC breaker, which can be expensive and has high power losses for hybrid topology [3], the control of the converter station can provide the short-circuit current reduction with specific submodule (SM) topologies. This work focuses on the clamp double SM (CDSM) topology, which provides the fault current limiting capability with smaller number of additional switching devices and consumes fewer power losses compared with other fault tolerant topologies [4], [5]. The fault protection control strategy is also straightforward. These features make the CDSM topology a competitive candidate for MMC design and development.

An accurate and efficient electromagnetic transient simulation is critical for the comprehensive and rigorous analysis and validation of MTDC systems [6], [7]. The CDSM has the most complex structure compared with half-bridge SM (HBSM) and full-bridge SM (FBSM), which makes the modeling process all the more challenging. Simplified or equivalent circuit schemes are commonly used for the off-line and the real-time simulation of the MMC station, such as Thévenin equivalence method, surrogate network method, and equivalent circuit method [8]–[10]. The calculation of power losses and the utilization of the electrothermal model for HBSM MMC have be presented in literature [11]–[13].

This work proposes the device-level electrothermal model to the real-time simulation of CDSM MMC. Such an improvement is necessary due to the distinct temperature dependent characteristics of power electronic devices. The real-time calculated junction temperatures influence the electrical parameters of the device model, which can improve the overall simulation accuracy. The thermal information such as junction temperatures and power losses are the significant indicators not only for energy efficiency but also the safety and security of converter stations. Besides the extreme over-voltage which can breakdown the devices, IGBT modules can be damaged due to overheating during the fault transients. The junction temperatures provide the direct evidence to evaluate the fault tolerance performance of the CDSM MMC and the protection strategy. Using a detailed electrothermal modeling scheme is also helpful for the system designer to choose appropriate IGBT modules and heatsinks, and for the control designer and operator to evaluate the system efficiency and security. Real-time simulation using the device-level electrothermal model provides the most reliable and efficient method to accomplish the above objectives. Applying electrothermal model can expand the functionality of

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the real-time simulator to verify the basic function, the security, and the economy of the converter control and protection system under hardware-in-the-loop (HIL) test. The proposed modeling scheme can be used to verify the converter efficiency with certain control algorithm and parameters, and to verify the effectiveness of the protection scheme by observing the junction temperature as the direct indicator. While real-time implementation may not be required in the design stage considering the thermal effect, it can substantially accelerate the design iterations.

This work adopts the datasheet based electrothermal model proposed in [6] and improves the model by using piece-wise polynomial curve fitting scheme for the electrical model, which can increase the modeling accuracy especially for the low current range. The first contribution of this work is the above improved modeling scheme and the methodology exploration and development to combine the electrothermal model of IGBT module to CDSM MMC. When considering the complex topology of CDSM MMC, it is critical to determine the appropriate modeling scheme and interface to maximize the algorithm parallelism and to ensure the real-time performance.

For the real-time implementation of the CDSM MMC system, the Xilinx Zynq UltraScale+ ZCU102 board using XCZU9EG multi-processor system-on-chip (MPSoC) device is chosen as the platform due to its high parallelism, high flexibility, and relative low design cost [14]. Various processing units and interfaces, such as the ARM quad-core Cortex-A53 and rich FPGA logic resources are fabricated on the same chip, which provides the features which conventional CPU or FPGA alone do not have and requires partition skills to maximize its capability. Using both CPU and FPGA on different boards for real-time EMT simulation have been presented in [15], [16]. Compared with using discrete CPU and FPGA devices [15], [16], the MPSoC device provides substantially larger communication bandwidth between the processing system and the programmable logic, and an integrated design environment. The reduced communication latency is beneficial for the flexible computation task partition and the realization of the complex electrothermal model. The second contribution is the introduction of the new MPSoC platform, and the system partition and implementation methods to achieve the fast sequential calculation and high parallelism simultaneously with minimum communication cost.

A three-terminal MTDC system composed of one CDSM MMC and two HBSM MMCs is used as the case study with 20 μs as the system simulation time-step. The system is decomposed into three subsystems, and each contains one converter station. The electrothermal model can consume higher logic resource, which can be mitigated by using hybrid SM modeling scheme with certain requirement of MMC level number. The 32-bit floating point precision is used for the simulation system, except for the switching transient waveform generation, which uses fixed-point data and can update the values on every FPGA clock cycle (10 ns). PSCAD/EMTDC and SaberRD are employed to validate both system-level and device-level results captured on the oscilloscope for steady-state operation and DC fault transients. The third contribution of this work is applying the electrothermal transient simulation results for the fault transient analysis of the MMC in real-time. Conventionally, the

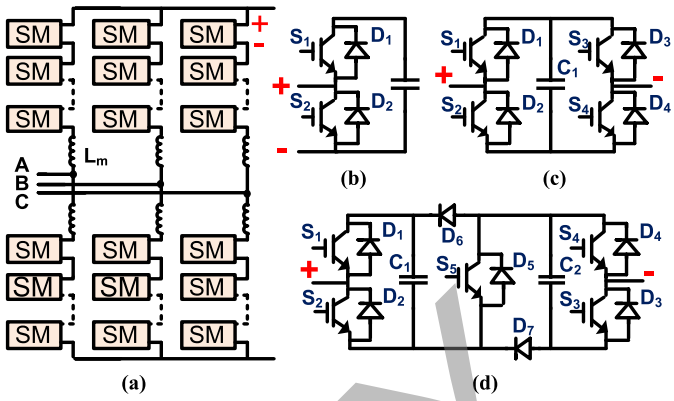

Fig. 1. MMC and SM topologies. (a) Modular multi-level converter. (b) Half-bridge submodule. (c) Full-bridge submodule. (d) Clamp double submodule.

thermal calculation is used to determine the converter efficiency of MMC. As previously explained, such results are important for the protection performance evaluation. This work particularly chooses CDSM as the study object due to its complexity, although the proposed modeling method, implementation skills as well as the electrothermal transient study can be used for other type of MMC SM, or other circuit topology. The paper is organized as follows. Section II describes the operation principles of CDSM. Section III introduces the proposed device-level electrothermal model for CDSM. Section IV introduces the MPSoC device and Section V presents the MTDC system case study and its detailed partitioning and implementation on the MPSoC platform. Section VI presents the real-time results and their validation, followed by the conclusion in Section VII.

II. Operation Principle of CDSM

The MMC is composed of multiple SMs in each converter arm as shown in Fig. 1(a). Breaking the over-current during DC fault is one of the major challenges for the HVDC transmission system. If the capacitor voltage in the SM can be negatively inserted into the converter arm, the DC fault current can be decreased and limited rapidly due to the reversed DC side voltage at the converter. Multiple submodule topologies exist in literature and in practical projects [4], [5]. Among them, HBSM, FBSM, and CDSM are the most popular ones shown in Fig. 1(b)–(d). The half-bridge topology is the simplest one, however it can not reverse the polarity of the inserted capacitor voltage. The full-bridge submodule has the fault-tolerant capability with the cost of doubling the power electronic switches. In addition, the full-bridge SM provides the capability of eventually changing the DC voltage rating and polarity, although it is normally not required for an HVDC system. As the name indicates, the CDSM contains two half-bridge SMs and a clamping circuit composed of two additional diodes and one IGBT module. One CDSM is equivalent to two FBSM providing the same voltage rating and levels; therefore the CDSM MMC utilizes fewer switches than FBSM MMC.

Fig. 2 presents some cases of the normal operation mode and the protection mode during faults. In normal operation, the IGBT gate signal of $\mathbf{S}_5$ is always on as shown in Fig. 2(a)–(b).

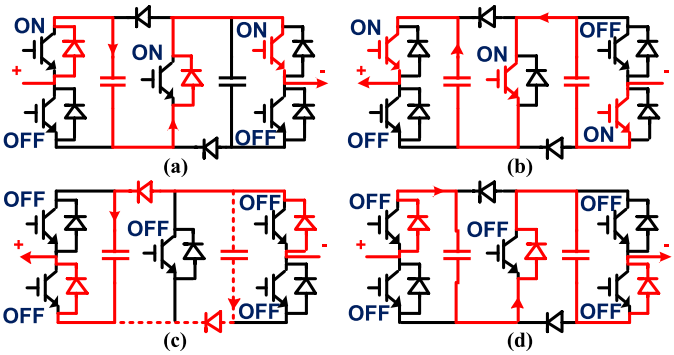

Fig. 2. CDSM operation demonstration with active routes in color red. (a) Normal operation with positive arm current. (b) Normal operation with negative arm current. (c) Protection mode with negative arm current. (d) Protection mode with positive arm current.

TABLE I
OPERATION MODE OF EACH HALF-BRIDGE STRUCTURE: CASE I ($\mathbf{S}_5$ TURNED-ON COMBINED WITH ANY SM CURRENT DIRECTION) AND CASE II ($\mathbf{S}_5$ TURNED-OFF COMBINED WITH POSITIVE SM CURRENT)

Mode	$\mathbf{S}_1/\mathbf{S}_3$	$\mathbf{S}_2/\mathbf{S}_4$	Current direction	Inserted voltage
Insert	1	0	+/-	$+Vc_1/+Vc_2$
Bypass	0	1	+/-	0
Block	0	0	+	$+Vc_1/+Vc_2$
	0	0	-	0
Fault	1	1	+/-	0

1 (0) means turned-on (turned-off), and + (−) means current flows from SM positive side to negative side (negative side to positive side).

The existence of Diodes $\mathbf{D}_6$ and $\mathbf{D}_7$ can clamp the capacitor voltage to positive values and can prevent internal loop current. Thus, the two half-bridge structures are connected in series, and can be controlled independently. The IGBT modules of the half-bridge structures are numbered in such a way that if the odd number switches are turned on, the corresponding capacitor is inserted in the converter arm. By doing so, the control scheme of HBSM MMC is compatible to the CDSM MMC during normal operation. When a fault is detected, $\mathbf{S}_5$ and other gate signals will be turned off. The capacitor voltages are inserted into the arm limiting the fault current with opposing polarity. In Fig. 2(c), current flows from the negative side to the positive side with $-Vc$ inserted, which will go through capacitors C_1, C_2 or both in parallel based on the comparison of the capacitor voltages. In Fig. 2(d), current flows from the positive side to the negative side with $+2Vc$ inserted. The operation of CDSM is complex especially when the current is negative, and all conditions shall be considered for modeling process [4], [5]. Table I lists the operation modes of each half-bridge structure for Case I when $\mathbf{S}_5$ is on combined with any SM current direction and Case II when $\mathbf{S}_5$ is off combined with positive SM current, while Table II lists the modes of CDSM for Case III when $\mathbf{S}_5$ is off combined with negative SM current.

III. DEVICE-LEVEL ELECTROTHERMAL MODEL OF CDSM

This section proposes the device-level electrothermal model of CDSM, which can accurately simulate the thermal conditions

TABLE II
OPERATION MODE OF CDSM: CASE III ($\mathbf{S}_5$ TURNED-OFF COMBINED WITH NEGATIVE SM CURRENT)

Mode	$\mathbf{S}_1$	$\mathbf{S}_2$	$\mathbf{S}_3$	$\mathbf{S}_4$	$Vc_1 vs Vc_2$	Inserted voltage
Positive Insert	1	0	1	0	$Vc_1 < Vc_2$	$+Vc_1$
					$Vc_1 = Vc_2$	$+Vc_1/+Vc_2$
					$Vc_1 < Vc_2$	$+Vc_2$
Negative Insert	0	1/0	0	1/0	$Vc_1 < Vc_2$	$-Vc_2$
					$Vc_1 = Vc_2$	$-Vc_1/-Vc_2$
					$Vc_1 < Vc_2$	$-Vc_1$
Bypass	1	0	0	1/0	Any	0
	0	1/0	1	0		
Fault	1	1	1/0	1/0	Any	0 or Vc_2
	1/0	1/0	1	1		0 or Vc_1

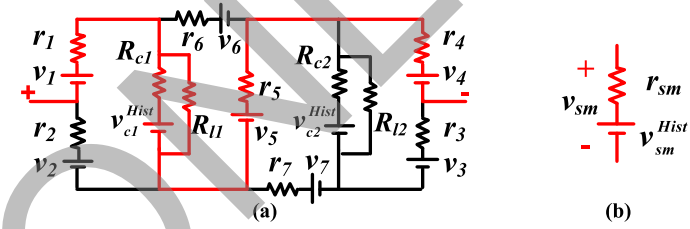

Fig. 3. CDSM models. (a) Complete circuit model with active route. (b) Simplified SM interface model.

of the IGBT modules. It describes the proposed modeling schemes and explains the parallelism from algorithm perspective, which includes device-level, SM-level, and converter-level modeling schemes. At the beginning of each time-step, the temperature dependent electrical parameters for interface model are calculated for each IGBT and diode devices based on the junction temperatures obtained from the last time-step. Then the equivalent circuit model is applied to the CDSM according to the gate signals and arm current direction shown in Table I and II. With obtained electrical interface model for the arm, the system matrix can be established and solved using EMT algorithm. The calculated current and voltage values are then used to compute the power losses and junction temperatures, which in-turn update the temperature-dependent parameters for the next time-step. Due to the real-time requirement of the electrothermal transient simulation, iteration is not applied. Since the rate of change of temperature is relatively slow compared with other variables, the effect of using the temperature of the last time-step can be neglected. The detailed modeling schemes are presented in the following sub-sections.

A. Device-Level Modeling Scheme

Device-level modeling refers to the generation of the circuit model of individual IGBT modules and diodes, which are the voltage source v_{sw} (subscript sw indicates the IGBT module or diode) in series with the resistor r_{sw} as shown in Fig. 3(a). In this work, the detailed device-level electrothermal model of the IGBT modules for CDSM MMC is built using the information obtained from the manufacture's datasheet for the

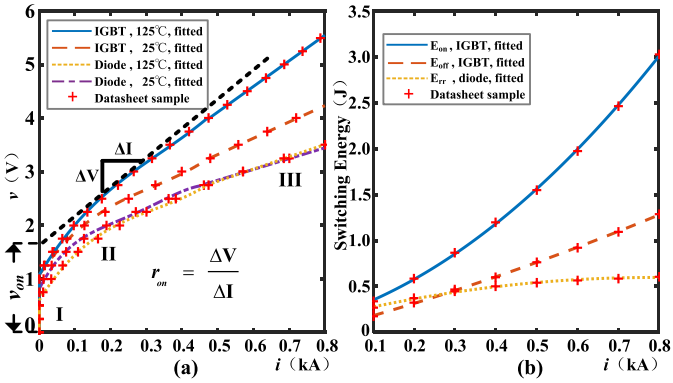

Fig. 4. Datasheet sample and fitted curves of the Infineon FZ400R33KL2C_B5 IGBT and diode characteristics. (a) Output characteristics of IGBT and diode at 125 °C and 25 °C. (b) switching energy losses of IGBT turn-on, IGBT turn-off and diode reverse recovery processes at 125 °C.

Infineon FZ400R33KL2C_B5 IGBT module [17]. The algorithm contains the temperature-dependent electrical interface parameter calculation, the power loss calculation, the thermal network calculation, and the device-level linearized transient waveform calculation.

1) Temperature-Dependent Electrical Interface Parameter Calculation: The electrical interface of the IGBT or diode is composed of the voltage source v_{sw} in series with a resistance r_{sw}. The temperature-dependent IGBT and diode output characteristics can be obtained from the datasheet, as shown in Fig. 4(a). The piece-wise polynomial curve fitting scheme is applied, with the following equations:

$$v(i) = \sum_{i=0}^{n} a_n i^n,\ r_{sw} = \frac{\mathrm{d}v}{\mathrm{d}i} = \sum_{i=0}^{n-1} b_n i^n,\ v_{sw} = v(i) - r_{sw} i, \tag{1}$$

where v and i are the voltage and current across the device; a_n and b_n are the correspondent polynomial coefficients. In this work, the curve is divided into three sections: the threshold section, the nonlinear section, and the linear section. In the threshold section, since the current is very small and has negligible influence on the electrical and thermal performance, the device is simply modeled as a large fixed resistor. In the nonlinear section, a third- or a fourth-order polynomial function is used, while the first-order fitting is applied when current is large in the linear section or section III as shown in Fig. 4(a). Since the datasheet only provides the characteristics at $T_1 = 25$ °C and $T_2 = 125$ °C, linear interpolation is applied to calculate the values at arbitrary temperatures, which can also be used for other temperature-dependent variables given in datasheet, such as switching energy, IGBT current rise, fall time, etc. Taking the example of r_{sw}, the interpolation equation is given as:

$$r_{sw}(T_{vj}) = \frac{T_{vj} - T_2}{T_2 - T_1}(r_{sw}^{T_2} - r_{sw}^{T_1}) + r_{sw}^{T_2}, \tag{2}$$

where T_{vj} is the junction temperature.

2) Power Loss Calculation: After solving the system circuit matrix, the arm current is obtained, and the SM capacitor voltage can be updated. This data along with the IGBT gate signals can be used to calculate the power losses of the individual IGBTs and diodes. The power losses of the power electronic switches are mostly composed of the conduction power losses and the switching power losses. The conduction power loss P_{cond} is given as:

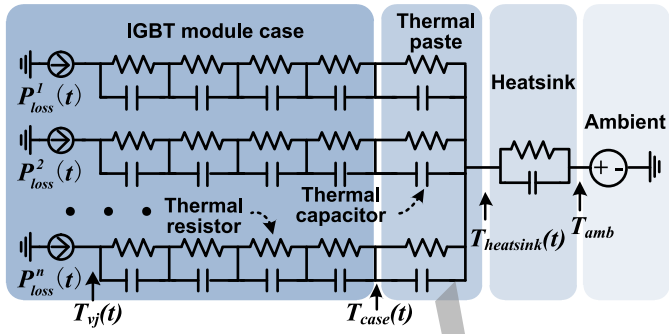

Fig. 5. Equivalent circuit for IGBT module thermal network.

$$P_{cond}(t) = (r_{sw}(T_{vj})i(t) + v_{sw}(T_{vj}))i(t). \tag{3}$$

The switching energy at 125 °C is given by the datasheet as shown in Fig. 4(b). The switching energy E_{switch} is assumed to be proportional to the voltage between the device when turned off. The fitting equation using second-order polynomial function is given as:

$$E_{switch}(i(t), v(t)) = \left(\sum_{i=0}^{2} a_n i^n\right) \frac{v(t)}{v_{rated}}, \tag{4}$$

where v_{rated} is 1800 V in this work. The switching energy at 25 °C is also given at the rated test condition, where current is 400 A when IGBT/diode turned on. The switching energy at an arbitrary temperature can then be estimated using linear interpolation similar to (2).

The total power loss is calculated as:

$$P_{loss}(T_{vj}) = P_{cond}(T_{vj}) + \frac{E_{sw}(T_{vj})}{\Delta t}, \tag{5}$$

where Δt is the simulation time-step.

3) Thermal Network Calculation: As shown in Fig. 5, the obtained power losses of the individual switches are the inputs to the thermal network which contains 6 stages series-connected thermal impedances from the semi-conductor junction to the case, the thermal paste, the heatsink, and the ambient [6], [17]. Each thermal impedance is composed of a thermal resistor and a thermal capacitor, and multiple devices can be mounted on the same heatsink. In this work, multiple IGBT modules are connected in parallel and in series to provide sufficient current and voltage rating for the MMC system. It is assumed that the paralleled IGBT modules are mounted on the same heatsink. The junction temperature is calculated using the Trapezoidal

TABLE III
THERMAL IMPEDANCES OF THE THERMAL NETWORK

Device	Parameter	i=1	i=2	i=3	i=4	i=5	i=6
IGBT	$R^i_{th}[K/kw]$	11.475	6.375	1.53	6.12	12	5
	$\tau^i_{th}[s]$	0.03	0.1	0.3	1	3	45
diode	$R^i_{th}[K/kw]$	22.95	12.75	3.06	12.24	24	5
	$\tau^i_{th}[s]$	0.03	0.1	0.3	1	3	45

integration rule as follows:

$$T_{vj}(t)=\sum_{i=1}^{5}\left(\frac{R^i_{th}\cdot\Delta t}{2\tau^i_{th}+\Delta t}(P_{loss}(t)+P_{loss}(t-\Delta t))+\frac{2\tau^i_{th}-\Delta t}{2\tau^i_{th}+\Delta t}\Delta T^i_{th}(t-\Delta t)\right)+\frac{R^6_{th}\cdot\Delta t}{2\tau^6_{th}+\Delta t}(P_{total}(t)+P_{total}(t-\Delta t))+\frac{2\tau^6_{th}-\Delta t}{2\tau^6_{th}+\Delta t}\Delta T^6_{th}(t-\Delta t)+T_{amb}, \tag{6}$$

where P_{loss} and P_{total} is the power loss of the device and the total power losses of the devices on the same heatsink; T_{amb} is the ambient temperature; $\Delta T^i_{th}(t-\Delta t)$ is the history temperature across impedance Z^i_{th}, which is expressed by the resistance R^i_{th} and capacitor time constant τ^i_{th} shown in Table III. The calculated junction temperatures are then used to update the temperature-dependent parameters. Although the time constant of thermal network is relatively large, the junction temperature can still change significantly during the fault transient due to the large over-current, which in turn affects the electrical parameters dynamically. Therefore, the electrothermal model can have better accuracy than post processing the electrical waveforms to obtain the thermal data.

4) Device-Level Transient Waveform Calculation: This work utilized linearized waveforms for the IGBT transients as given in [6], [18]. The rise time and fall time of the IGBT are obtained from the datasheet, which are temperature dependent. The slope of the transient is assumed to remain constant, therefore the rise time and fall time of the current and voltage waveform are proportional to the values of the turn-on current and turn-off voltage of the device, respectively. Since the datasheet only provides the rise time and fall time of the current waveform, the corresponding fall time and rise time of the voltage waveform are estimated by the switching energy losses.

B. SM-Level Modeling Scheme

The task of SM-level modeling is to obtain the simplified SM model composed of the voltage source and resistor. Multiple simplification schemes were developed in the literature such as Thévenin equivalence method, surrogate network method, and equivalent circuit method [8]–[10]. The computation effort of determining Thévenin equivalent is similar to solving the matrix equation of the SM circuit model. The number of effective nodes is calculated as the total nodes of the circuit topology minus one, which is assumed to be the ground node. The HBSM only contains two effective nodes, while the CDSM topology contains 5 effective nodes. The computation effort increases cubically with the matrix size to be solved, which is the same as the number of effective nodes. Therefore, it can be computationally expensive to use Thévenin equivalence method to calculate for all the CDSMs.

This work uses multiple equivalent circuits for different switching combinations, which is essentially the same as the surrogate network method, and the equivalent circuit method. With a certain switching combination, current flows into some determined branches. The leakage current of the IGBT module can be as small as several milliamperes, and is therefore neglected. Under most operating conditions, there is only one current path between the terminal nodes. Fig. 3(a) shows the CDSM circuit model, and the black path indicates the active current route, when $\mathbf{S}_1$ and $\mathbf{S}_4$ are turned on. The capacitor is modeled as the impedance $\mathbf{R}_c$ in series with the history voltage source v_c^{Hist} using Trapezoidal rule, and a leakage resistance $\mathbf{R}_l$ is also included. The history voltage source v_c^{Hist} is updated as:

$$v_c^{Hist}(t)=v_c^{Hist}(t-\Delta t)+R_c\cdot(k\cdot i_{arm}(t)-v_c^{Hist}(t-\Delta t)\cdot G_l), \tag{7}$$

where, i_{arm} is the arm current; $\mathbf{G}_l$ is the conductance of the leakage resistor; k is determined by the switching condition.

The SM-level model can be obtained by summing the circuit model elements of the devices in the active path to a voltage source in series with a resistor, as shown in Fig. 3(b). The determination of the circuit topology is based on the gate signals of the IGBTs, the current direction and the relation between the two capacitor voltages as listed in Tables I and II. Occasionally, symmetrical current paths may happen, which can be easily combined by adding the conductances of the two paths.

C. Converter-Level Modeling Scheme

The MMC has a large number of switching devices and relatively complex circuit topology, which is a major challenge for its modeling and simulation. To accelerate the computation speed, the size of the system matrix shall be minimized. In this work, equivalent voltage sources and impedances are used for all SMs. Using the arm current of the last time-step, the simplified SM model in a converter arm can be summed to a single voltage source to interface with the external circuit, calculated as:

$$v_{arm}(t)=\sum_{i=1}^{n}\left(r_{sm(i)}\cdot i_{arm}(t-\Delta t)+v^{Hist}_{sm(i)}\right), \tag{8}$$

where n is the SM number in one arm; $r_{sm(i)}$ and $v^{Hist}_{sm(i)}$ are the i_{th} sub-module electrical model elements shown in Fig. 3(b). Therefore, the nodes of the interface elements for the converter arms are substantially decreased, and all SMs can be calculated in parallel. The iterative scheme for relatively complex MMC is not applied for the purpose of meeting real-time simulation requirement [19]–[21].

Fig. 6 illustrates the major algorithm of the proposed electrothermal CDSM MMC model. The complete electromagnetic

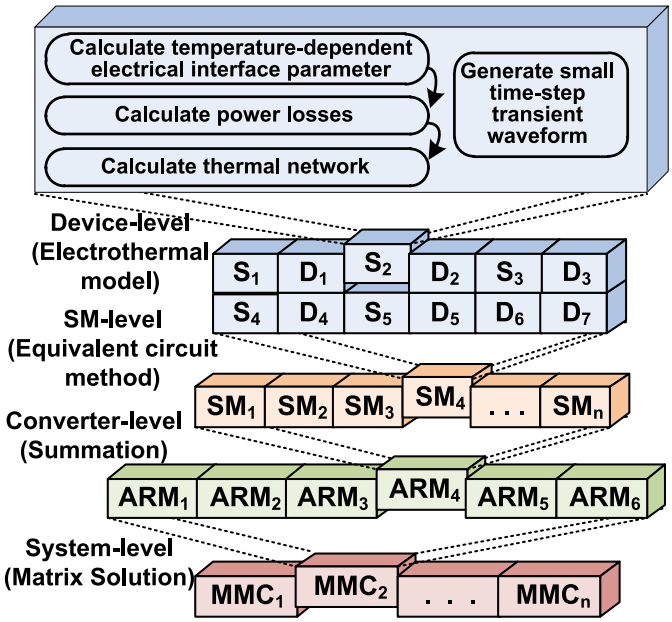

Fig. 6. Illustration of hierarchical MMC modeling scheme.

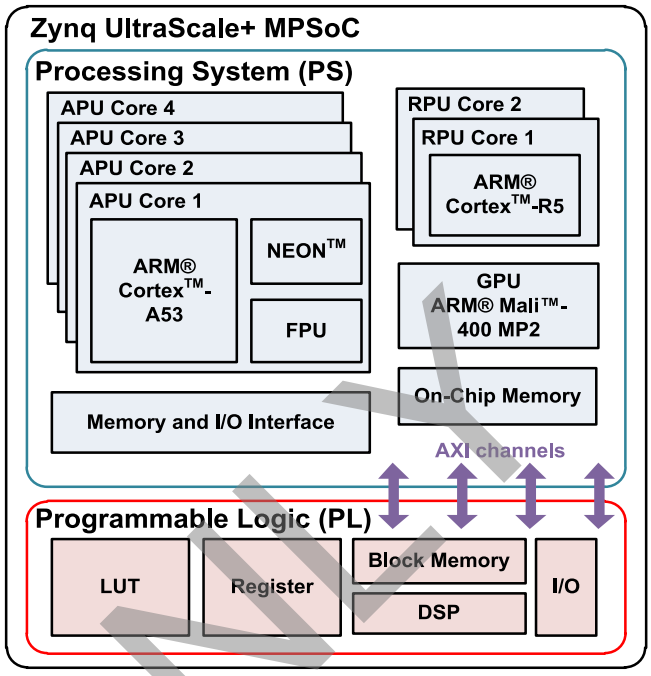

Fig. 7. Block diagram of Xilinx Zynq UltraScale+ MPSoC device.

transient simulation of MMC system is composed of device-level, SM-level, converter-level, and system-level calculation. A sequential relation exists between different levels, which means only when the interface elements of the fundamental level are obtained, the results of the next level can be accomplished. The calculation among the units of the same level can be parallelized well. When expanding each level, the amount of the paralleled device-level units is substantial and requires large computation capability. The parallelism also exists in each calculation step of the device-level modeling scheme. The complete system is then solved by the matrix equation for electromagnetic transient simulation, as follows:

$$\mathbf{G} \cdot \mathbf{v}(t) = \mathbf{I}_{eq}, \tag{9}$$

where, $\mathbf{G}$ is the conductance matrix, $\mathbf{v}(t)$ is the node voltages, and the $\mathbf{I}_{eq}$ is the equivalent current source.

IV. Hybrid Hardware Architecture of MPSoC

Both multi-core CPU and FPGA have been used in real-time electromagnetic transient simulation in both industry and academia [6], [9], [10], [18]. The CPU is optimized for general-purpose sequential tasks running at high clock frequency. Although multi-core CPU can provide the parallelism to some extent, the communication latencies between multiple cores exist. FPGA containing a large amount of programmable logic resource can provide highly parallel computation capability, while the clock frequency is much lower than that of CPU. The design and programming effort for FPGA is also higher. It is critical to analyze the characteristics of the algorithm before determining the implementation platform. The EMT program contains the one-time initialization stage and periodic calculation stage for every time-step. Since the parallelism exists in both stages, FPGA may work faster with optimized design. The usage rate of FPGA resources can be low if the implemented functions are not frequently used. The resource is a major limitation for the simulation of complex and large-scale systems on FPGA. Therefore, it is more efficient to use CPU for the infrequent tasks such as the system initialization, and complex sequential tasks, such as control algorithm.

Using both discrete CPU and FPGA devices for real-time simulation, which are mounted on separate boards communicated by PCIe bus, has been presented in literature [15], [16]. Due to the high communication bandwidth and the integrated design environment, using the *single-chip* combination of CPU and FPGA is a more efficient and cost-effective solution for real-time transient simulation, compared with discrete CPU and FPGA solution. The communication latency can significantly affect the calculation partitioning scheme and the feasibility of complex modeling scheme. The Zynq UltraScale+ MPSoC is used in this work, which integrates the ARM application processing unit (APU) and Xilinx FPGA on the same chip as shown in Fig. 7. The communication latency between the processing system (PS) and the programmable logic (PL) is minimized due to the high bandwidth of the interconnection channels within the same chip using Advanced eXtensible Interface (AXI) protocol with either master or slave interfaces. In the MPSoC device, there are in total 10 AXI channels with 128-bit data width for each channel. This work uses all three channels with the master interface, which are controlled by the processing system.

The processing system contains the quad-core APU, the dual-core real-time processing unit (RPU), the graphical processing unit (GPU), the on-chip memory (OCM), and the memory and I/O interface, etc. The programmable logic contains numerous distributed look-up-tables (LUTs), flip-flops (FFs), block RAM (BRAM), DSP slices, and I/O interfaces. High-level-synthesis (HLS) is used to accelerate the FPGA design process, which uses

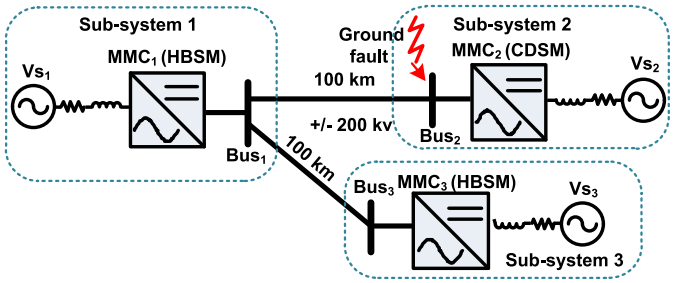

Fig. 8. Circuit topology of MMC-based three-terminal MTDC system.

C/C++ programming language instead of VHDL or Verilog [22]. Arbitrary-precision data and various directives, such as pipeline, loop unroll, etc., are provided in HLS to optimize the design for specific latency and resource requirements.

V. Case Study and Hardware Implementation

A three-terminal DC system is used as the case study shown in Fig. 8, which is composed of two HBSM MMC stations and one CDSM MMC station connected by two 100 km +/− 200 kV DC transmission lines. The major parameters are listed in Appendix. A ground fault of both poles at $\mathbf{Bus}_2$ is applied as the test condition. Since this work is focused on the modeling of CDSM MMC, the electrothermal model is used for $\mathbf{MMC}_2$, while $\mathbf{MMC}_1$ and $\mathbf{MMC}_3$ uses the equivalent circuit models. All MMCs have 17 levels, which means that each MMC arm has 16 HBSMs or 8 CDSMs. To provide sufficient current rating and voltage rating, four FZ400R33KL2C_B5 IGBT modules or diode are connected in parallel, and 14 such paralleled structures are connected in series [17]. A conventional breaker is added in each converter arm of CDSM MMC, which is modeled as a two-state resistor. The transmission lines are modeled using a distributed line model.

A. Design Partition

The computation of the MTDC system is allocated to the four APU cores and programmable logic resources of the Zynq UltraScale+ MPSoC device. The major challenge of the partition process is minimizing the exchanged data between different computation units to decrease the communication latency. Programmable logic is more suited for highly paralleled tasks, which are the MMC SMs related computation. To save the PL resource, other computations are located in PS, though some of them can also be accelerated in PL.

With the above consideration, the system design is first partitioned into the three sub-systems separated by the distributed line model. Besides the process control signals for synchronizing purpose, the exchanged data during periodic calculation is only the history current of the transmission line model. The system matrix can also be divided into three smaller sub-matrices. One APU core is responsible for the calculation of each subsystem, and the fourth core is used for the system-level control calculation which generates the modulation signals for valve-level control. The valve-level control requires the SM capacitor voltage sorting process and generates gate signals for all SMs, which needs a large amount of data exchange from the SM calculation units. Therefore the valve-level control is located in PL to avoid the long latency between PS-PL communication.

Fig. 9 shows the major computation processes of all applied units in Zynq UltraScale+ MPSoC. In this design, bare-metal configuration alone with the default board support package is applied for all four APU cores without using the operating system. In the default setting, the 32 KB instruction cache, 32 KB data cache of all cores, and the 1MB L2 cache are enabled. $\mathbf{APU}_1$ is the master core which controls the simulation processes. At the beginning, it executes the hardware initialization, which includes waking up other cores, setting system counter, and initializing the PL module. Then it begins the initialization of the application, which are the calculation of the circuit element parameters, and the variable initialization. The initialized data is sent to other cores during the receiving process.

Then the periodic calculation begins. $\mathbf{APU}_{1-3}$ can execute simultaneously for the correspondent sub-systems. First they exchange the transmission line data, and then calculate the variables for other components, such as the transmission lines, arm inductances, voltage sources, etc. In the meantime, the valve-level control, HBSM MMC, CDSM MMC modules of the subsystems on PL will start their respective calculations. With all variables calculated, the system matrix equations are calculated and the history data of the transmission lines and the inductances are then updated. $\mathbf{APU}_1$ will first wait for the accomplishment of other cores and then wait until the next time-step comes in real-time before entering to the next loop. The system-level control can have its independent time-step, and can transfer its system-level control data with a fixed delay. It uses classical dq-axis decomposition and PI controllers for the DC voltage and power outer loop control and the inner current loop control [23], [24]. In this work, the control on $\mathbf{APU}_4$ uses the same time-step as the simulation time-step, and transfers its control variables during the component calculation process of other cores.

On PL, the valve-level control module generates the gate signals for the HBSM MMC and CDSM MMC module using phase-disposition sinusoidal pulse width modulation (PD-SPWM) scheme [23]. This scheme requires capacitor voltage sorting, and uses 2000 MHz as the carrier frequency. Hardware sorting of n capacitor voltages in one converter arm is implemented with full $\frac{n(n-1)}{2}$ times comparison, which can be conducted in parallel. By adding the corresponding one-bit comparison results, the sequence is generated. Compared with sequential software sorting, hardware sorting is substantially faster, which uses two FPGA clock cycles (20 ns) for the SMs in one arm. It is noted that software sorting can also use $\frac{n(n-1)}{2}$ times comparison in the worst case scenario, which must be considered for real-time application. In HBSM MMC module, the major tasks are the SM capacitor voltage update and MMC arm interface calculation. The interface calculation for SMs in one arm is conducted in parallel. The interface voltage sources of SMs are summed to generate the arm interface, and then sent back to corresponding APU cores. The general process of CDSM MMC is similar to the more complex process of the SM

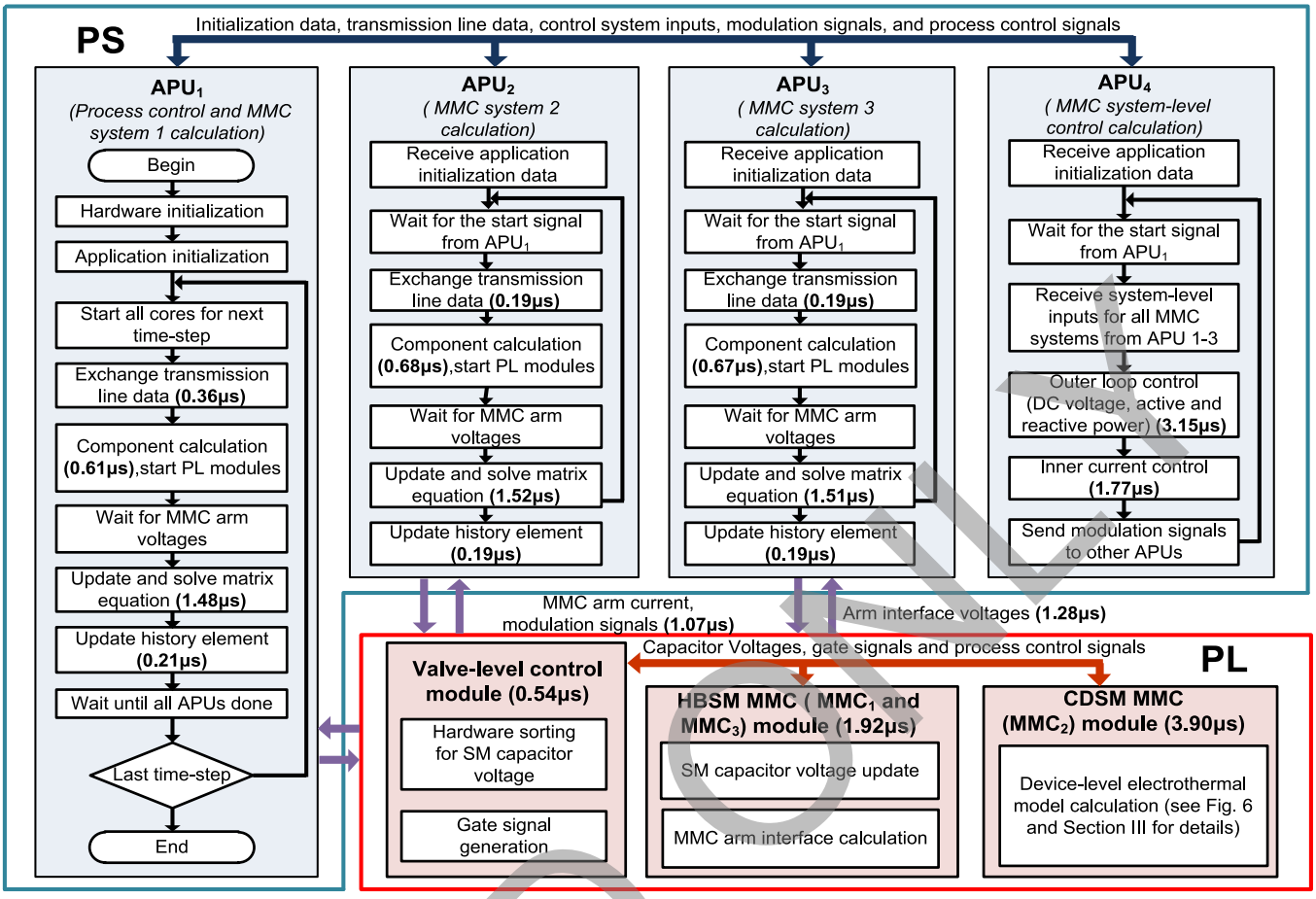

Fig. 9. Design partition of the MTDC system on the MPSoC device (latencies are shown in parentheses).

interface generation, where the device-level electrothermal model is applied.

B. Latency and Resource Consumption

The latencies of the major processes during the periodic calculation are shown in Fig. 9. The calculation time on different APU cores has slight variance due to the minor difference of the included components. Although the computation can be fully paralleled on FPGA resources as long as the algorithm allows, it may not be necessary and can consume much hardware resource. Multiplexing and pipelining are used for the resource optimization. The valve-level control module for one arm takes 30 ns, and it takes 540 ns for 18 arms in 3 MMCs by multiplexing, and consumes 9.0% of LUT, 1.5% of FF on XCZU9EG device. The HBSM MMC module includes three sets of the paralleled arm calculation units, which consumes 5.1% of LUT, 2.3% of FF, 5.4% of DSP slices. The CDSM MMC module has two sets of arm calculation units, which consumes 77.7% of LUT, 29.3% of FF, 38.5% of DSP slices. The resource consumption is relevant to the allocation of corresponding arm-level units.

VI. Real-Time Emulation Results and Analysis

In the hardware setup of the simulation system, a host computer downloads the programming files including the bitstream to the Xilinx UltraScale+ ZCU102 MPSoC board through the USB cable and the on-board JTAG chip. On the Zynq device, the APU cores run at 1.2 GHz, while the FPGA clock frequency is 100 MHz. The real-time results from the MPSoC board are converted to analog signals by the digital-to-analog converter (DAC) and then captured by the oscilloscope. The system-level results are validated by comparing with PSCAD/EMTDC with the same system configuration, and the device-level results are validated with SaberRD using detailed dynamic thermal IGBT and diode models. Since the complete system cannot converge in SaberRD due to the complex nonlinear algorithm, a single CDSM circuit with external SM current source and gate signals is applied for the verification.

A. Normal Operation Results

Fig. 10(a)–(c) presents the CDSM MMC AC voltages, AC current, and the first SM capacitor voltages of the upper and lower arm in phase-A. The real-time simulation results in blue solid lines are compared with the PSCAD/EMTDC results in sienna dashed lines. The overall waveforms match quite well, however the harmonics can have small differences due to the accumulated control error, which is caused by the different algorithm and implementation method among various programs. The accumulated control system error can significantly affect the gate signals, which leads to the relatively large difference

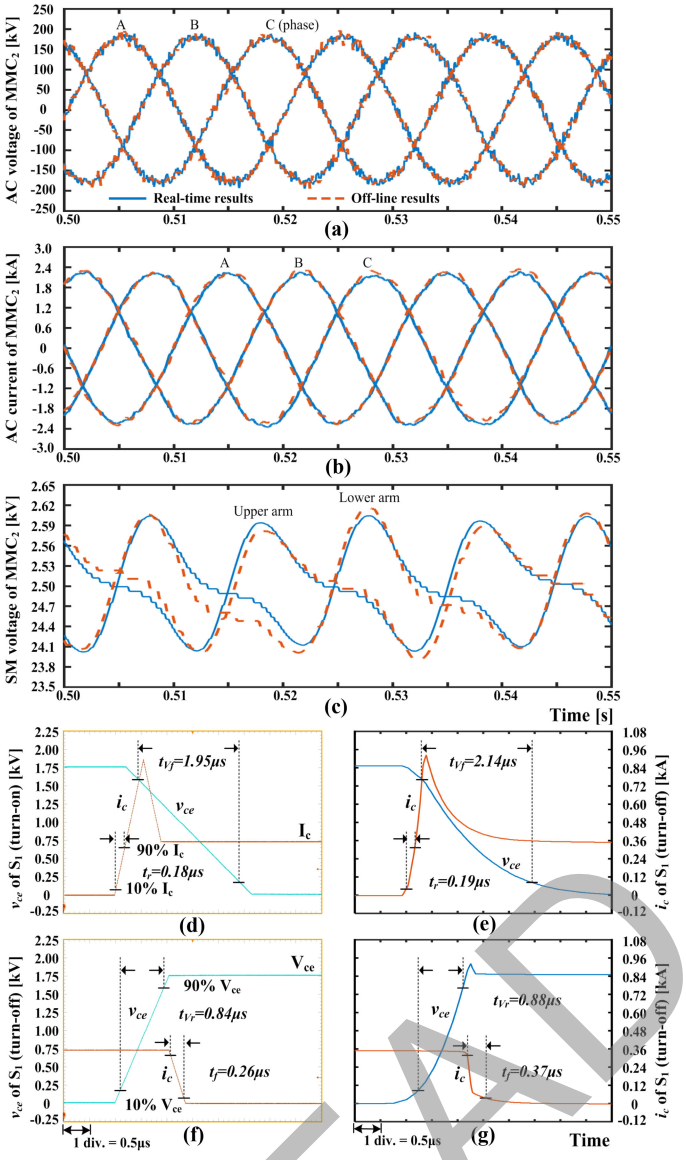

Fig. 10. Steady state results. (a) AC voltages. (b) AC currents. (c) SM voltages. (d) (e) Turn-on switching transients of $\mathbf{S}_1$. (f) (g) turn-off switching transients of $\mathbf{S}_1$. (In (a) (b) (c), the solid lines are real-time results, and the dashed lines are offline PSCAD/EMTDC results. (d) (f) are real-time results, and (e) (g) are offline SaberRD results.)

for SM capacitor voltages. Fig. 10(d)–(g) presents the turn-on and turn-off switching transients of $\mathbf{S}_1$. The results are compared with SaberRD, which uses detailed datasheet-based device-level behavior model for IGBT and diode. The current rise time t_r, current fall time t_f, voltage rise time t_{Vr}, voltage fall time t_{Vf} are measured, with the definition of 10% to 90% change of the steady-state I_c and V_{ce}. The overshoot current during the turn-on process is generated due to the reverse-recovery current of the turn-off of D_2. The linearized waveforms can give a good estimation of the switching transients based on the datasheet. The averaged powers of the AC and DC sides of CDSM MMC during steady-state operation are -600 MW and -589.4 MW for the real-time results using electrothermal model, and -600.0 MW and -594.9 MW for the PSCAD/EMTDC using ideal IGBT

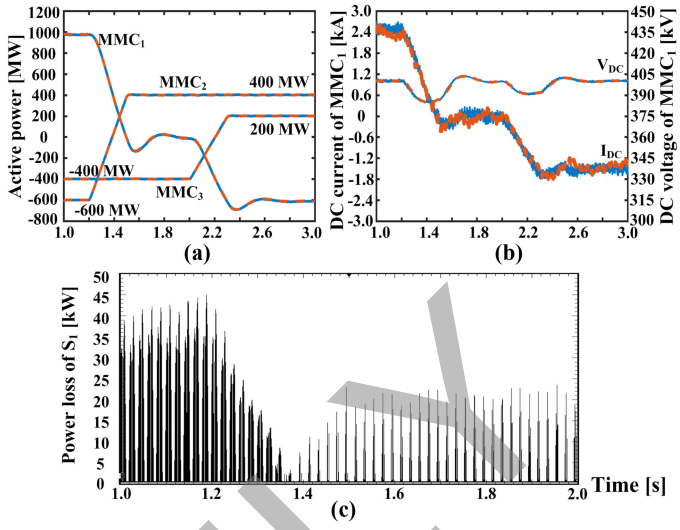

Fig. 11. Power flow control real-time results. (a) Active power of $\mathbf{MMC}_1$, $\mathbf{MMC}_2$ and $\mathbf{MMC}_3$. (b) DC current and DC voltage of $\mathbf{MMC}_1$. (c) Power losses of $\mathbf{S}_1$ of $\mathbf{MMC}_2$. (In (a) (b), the solid lines are real-time results, and the dashed lines are offline PSCAD/EMTDC results.)

module model, respectively. Fig. 11 shows the real-time results of power flow tracking performance, DC voltage stabilization performance, and the power losses of S_1 during the power flow change. The reference active power of $\mathbf{MMC}_2$ and $\mathbf{MMC}_3$ changes from 1.2 s to 1.5 s and 2.0 s to 2.3 s, respectively. $\mathbf{MMC}_1$ can effectively maintain the DC voltage and balance the active power flow.

B. DC Fault Transient Results

A DC ground fault is applied to the case study system at 0.8 s of the simulation run. Once the instantaneous over-current is detected which is +/−10 kA in this work, the protection mode is activated and $\mathbf{S}_5$ is turned off. Once the arm current reaches 0, the breaker in the converter arm is opened to prevent the disturbances from other phases and DC side. Fig. 12(a)–(b) show the comparison of the upper and lower arm current fault transients between the real-time results and the PSCAD/EMTDC results. It is observed that the rate changes during the decrease of the current; this happens because when the other arm current in the same converter leg reaches 0, the effective circuit topology is changed. Fig. 12(c)–(d) present the on-state resistance r_{sw} of IGBT during both steady-state and fault transient, which are influenced by both the arm current and the junction temperature. Fig. 12(e)–(f) present the power losses of $\mathbf{S}_1$ and $\mathbf{S}_5$ in the first CDSM of phase-A upper arm. In Fig. 12(e), the switching power losses can be observed during normal operation, which are shown as the dense spikes. The relatively small conduction losses are presented in the zoomed figures. The $\mathbf{S}_5$ combined with $\mathbf{D}_5$ provides the path to connect the two half-bridge structure in CDSM, which does not switch during normal operation. When the fault happens, the conduction loss increases and then $\mathbf{S}_5$ is turned-off showing the switching power loss.

Fig. 13 shows the junction temperatures of all devices in the first CDSM in phase-A upper arm, which are compared with SaberRD results. Due to the difference of the switching pattern,

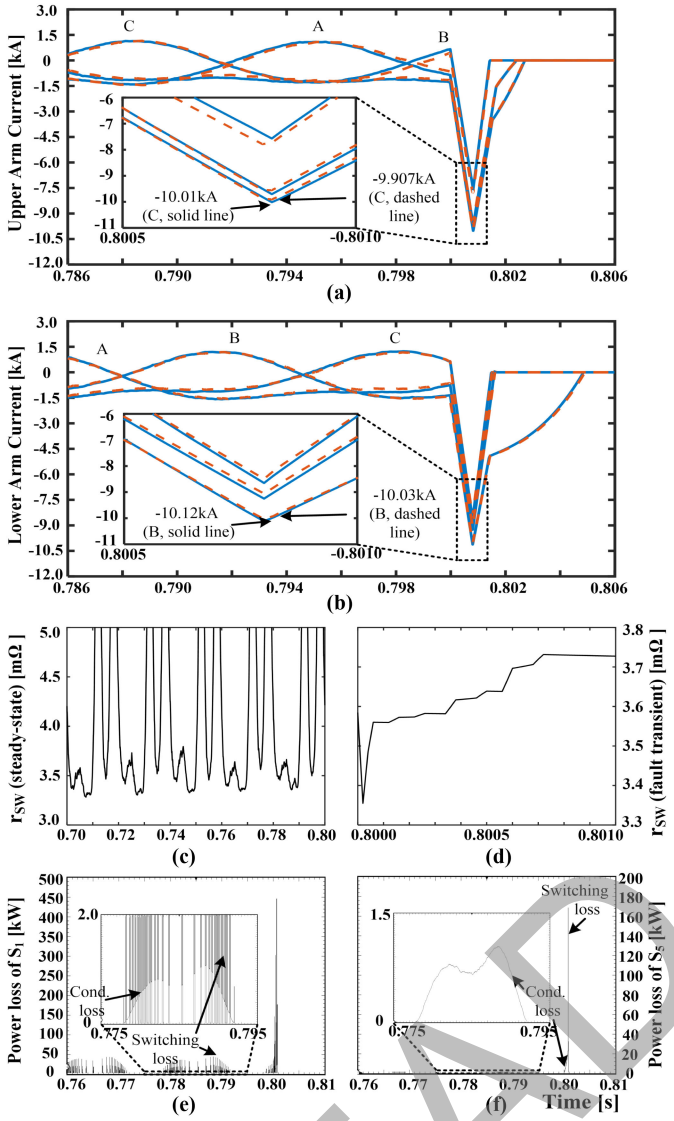

Fig. 12. Fault transient results. (a) Upper arm currents. (b) Lower arm currents. (c) IGBT resistance r_{sw} of $\mathbf{S}_1$ during steady-state. (d) IGBT resistance r_{sw} of $\mathbf{S}_1$ during fault transient. (e) Power loss of $\mathbf{S}_1$. (f) Power loss of $\mathbf{S}_5$.(In (a) (b), the solid lines are real-time results, and the dashed lines are offline PSCAD/EMTDC results. (c)-(f) are real-time results.)

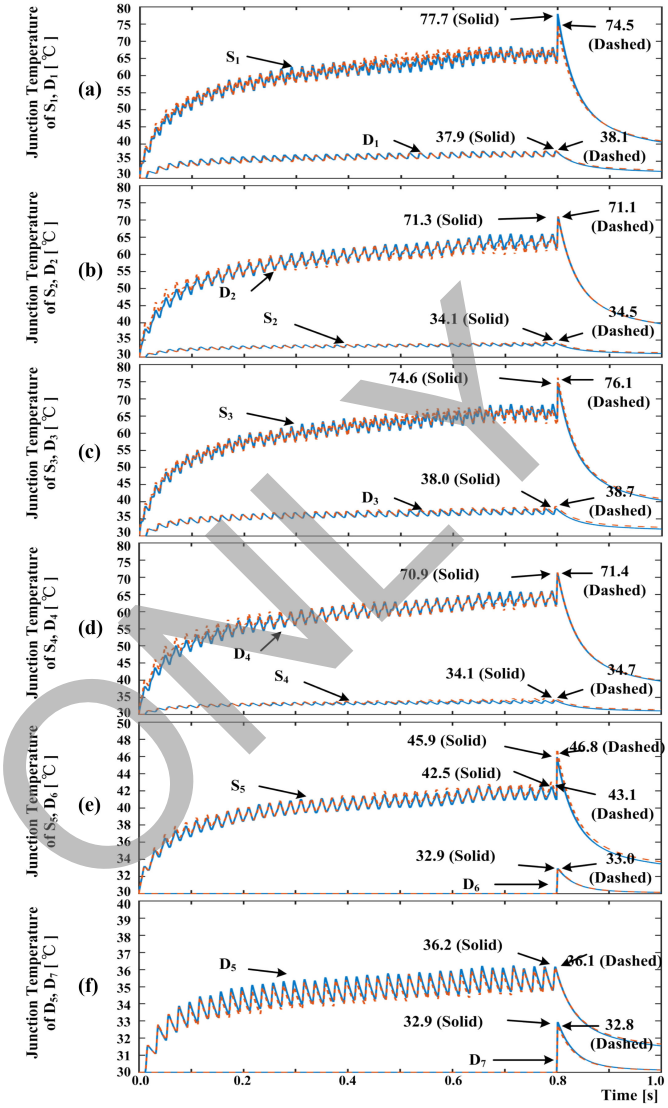

Fig. 13. Junction temperatures. (a) Of $\mathbf{S}_1$, $\mathbf{D}_1$. (b) Of $\mathbf{S}_2$, $\mathbf{D}_2$. (c) Of $\mathbf{S}_3$, $\mathbf{D}_3$. (d) Of $\mathbf{S}_4$, $\mathbf{D}_4$. (e) Of $\mathbf{S}_5$, $\mathbf{D}_6$. (f) Of $\mathbf{D}_5$, $\mathbf{D}_7$. (The solid lines are real-time results, and the dashed lines are offline SaberRD results.)

the existence of the MMC loop current, the junction temperatures can be quite different for the devices though they may have same electrothermal characteristics. When the fault happens, the junction temperatures of the active devices first rise sharply due to the abnormally high power losses, then decrease to a lower value since the converter is shut down. Due to the assumption that the paralleled devices are mounted on the same heatsink, the junction temperatures of $\mathbf{D}_6$ and $\mathbf{D}_7$ are not influenced by other devices and do not change until the fault mode is active. Due to the difference of the modeling schemes and solution methods between the proposed method and SaberRD, a small amount of error is expected. It is noted that the simulation lasts for 1s due to the convergence and memory limitation of SaberRD, which do not exist for the proposed real-time simulation. A malfunction or improper parameter setting of the protection could lead to the large temperature rise, which damages the devices.

VII. Conclusion

This paper proposed the device-level electrothermal model for CDSM MMC for the real-time simulation of MTDC system on an MPSoC device. The design and partition of the MTDC system are described in detail. The system-level waveforms, device-level waveforms, power losses, and junction temperatures of individual switches were collected and validated with PSCAD/EMTDC and SaberRD. The detailed device-level results can be further used to evaluate the switch condition under normal operation and contingency for the control and protection schemes. In future work, hybrid modeling scheme using both the electrothermal model and equivalent circuit model for different SMs can be applied to reduce the computation resources for the MMC with high level number. The proposed MPSoC-based MTDC system transient simulation can be interfaced with additional FPGA resources for the simulation of large-scale DC grids.

APPENDIX

Parameters of the case study: Vs amplitude (RMS) and frequency, R_s, L_s (same for the three sub-systems): 220 kV, 50 Hz, 0.6 Ω, 30 mH; arm inductor L_m and SM capacitance: 18.9 mH, 2 mF; Transmission line voltage rating, distance, surge impedance: +/−200 kV, 100 km, 394 Ω.

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