Exploration of Ferroelectric Devices for Use in Radio-Frequency Nanoelectronics

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Solid State Electronics

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Abstract

Since the 1970s, the rapid advancement of semiconductor electronic devices has facilitated an explosive growth of computation power in chips, which is exemplified by the rapid advancement of electronics such as high-tech consumer electronics including personal computers, smartphones, and other smart devices in the past few decades. Historically, this incredible advancement was driven by the geometrical downscaling of transistor dimensions, which allowed more transistors to be packed into the same chip area, thereby improving performance. However, numerous challenges have arisen in recent years, resulting in a gradual slowdown of downscaling. For example, the transistor gate length, a critical dimension affecting device performance, is predicted to stop scaling at 12 nm in 2028. To meet the increasing computational demand of current and emerging applications such as Artificial Intelligence and Internet-of-Things, further innovation at the device level is required.

One important direction to improve device performance that has recently emerged is the proposed use of ferroelectric materials in nanoelectronic devices. Ferroelectric materials are predicted by the Landau-Khalatnikov (LK) model to exhibit negative capacitance. Recently, the integration of ferroelectrics into field-effect-transistors (MOSFETs), creating so-called "negative-capacitance FETs (NCFETs)," has been proposed. Due to negative capacitance, NCFETs are expected to exhibit a higher on-current and a lower subthreshold slope compared to standard FETs, both of which are extremely desirable characteristics for increasing the performance of chips.

Since the inception of NCFETs in 2008, numerous studies have examined the performance of these novel devices for use in digital applications, However, one facet that has not yet been thoroughly explored is their radio-frequency (RF) performance. As such, this work will explore the potential for ferroelectric devices to be used in future RF systems.

In the first stage of this work, an initial assessment of RF performance of NCFETs is conducted using calibrated numerical simulations. Through the comparison of the important figures of merit $f_{T,}$ $f_{\max}$, and $g_m f_T / I_D$, where f_T is the unity-current-gain frequency, $f_{\max}$ is the unity-power-gain frequency, g_m is the transconductance, and I_D is the dc bias current, NCFETs were found to be able to exhibit similar f_T and $f_{\max}$, but a higher $g_m f_T / I_D$ compared to a standard MOSFET, demonstrating their potential as strong candidates for future RF electronics.

In the second stage of this work, a further in-depth assessment of RF performance for NCFETs is conducted in terms of f_T and $g_m f_T / I_D$, with an emphasis on the potential for NCFETs to mitigate the effects of parasitic capacitances. Through a comparison of f_T and $g_m f_T / I_D$ between an NCFET and a standard MOSFET, it is predicted that NCFETs can indeed mitigate the effects of parasitic capacitances and improve f_T and $g_m f_T / I_D$ over a standard MOSFET. This second study further emphasizes the importance of NCFETs for future RF applications, as parasitic capacitance continues to increase as dimensions are scaled down.

In the third stage of this work, the applications of ferroelectrics beyond their use in the gate stack of a FET is explored by examining the potential to use negative capacitance in constructing a tunable oscillator. It was found that tunable oscillations with an extremely wide tuning range can be achieved by replacing the inductor in a standard oscillator with a

ferroelectric capacitor, which is much smaller than the inductor. The proposed design is an important step both towards exploring the RF applications of ferroelectrics outside of NCFETs and towards a new oscillator circuit that can address the challenges of existing inductor-based designs.

Overall, this work explores the potential for ferroelectric devices to be used in future RF applications by examining the RF performance of NCFETs and by exploring the use of ferroelectrics for the construction of a tunable oscillator. The results provide important insights and predictions that motivate the continued exploration and optimization of novel ferroelectric devices in the on-going effort to improve the performance of nanoscale electronics to meet the demand of current and future applications.

Preface

Versions of Chapter 2 and Chapter 3 have been published in *IEEE Transactions of Electron Devices* as

- J. K. Wang *et al.*, “RF performance projections of negative-capacitance FETs: f_T, $f_{\max}$, and $g_m f_T / I_D$,” *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3442–3450, Aug. 2020, doi: 10.1109/TED.2020.3001248.

- J. K. Wang *et al.*, “Potential Enhancement of f_T and $g_m f_T / I_D$ via the Use of NCFETs to Mitigate the Impact of Extrinsic Parasitics,” *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4153–4161, Aug. 2022, doi: 10.1109/TED.2022.3187374.

In stages 1 and 2 of this work, I was the primary researcher, responsible for problem definition, simulation setup and execution, data analysis, and manuscript composition.

A version of Chapter 4 will also be submitted for publication to an IEEE journal.

In stage 3 of this work, I was a primary researcher together with my colleague Collin VanEssen. I was responsible for problem definition, and was jointly responsible for simulation setup and execution, data analysis, and manuscript composition.

Dedicated to my friends, family, and the glittering brilliances that have constantly guided me; without whom, this journey would not have been possible.

Acknowledgements

Firstly, I would like to thank my supervisor, Dr. Mani Vaidyanathan, for inspiring me constantly throughout my Ph.D. degree, and for offering an enormous amount of feedback throughout. You have taught me numerous critical skills that are not only important for scientific research, but for any field of professional work. Furthermore, the guidance you have provided throughout my degree has made the extremely challenging journey of graduate studies easier, and I was only able to deal with the enormous amounts of uncertainty associated with research because of your kind advice. These lessons that I have learned over the past seven years will guide my path for a long time to come into my career.

I would also like to thank Dr. Prasad Gudem and Dr. Diego Kienle for their extensive feedback and technical discussions over these years. Prasad, without your tireless guidance over these years, I would not have been able to effectively relate my work to real-world applications and develop a sense of intuition that is critical for any engineer. Diego, without your detailed feedback on my work, I would not have been able to develop an appreciation for details and precision in the process of research. I will always be grateful for the feedback and critiques that I have received from both of you over these years, and the lessons that I have learned will be with me throughout my career.

Furthermore, I would like to thank my Ph.D. examination committee, Dr. Sandipan Pramanik, Dr. Ray Decorby, Dr. Xihua Wang, Dr. Jason Myatt, and Dr. Youngki Yoon for taking time out of their busy schedule to evaluate and give feedback on my thesis research.

I would also like to thank my colleagues at the Nanoelectronics Research Laboratory and our collaborators, Dr. Kyle Holland, Dr. Michael Wong, Dr. Jason Yuan, Thomas Cam, Shahriar Rizwan, Collin VanEssen, Keith Ferrer, Riley Stuermer, Nuoyi Yang, for their support and discussions. Without your inputs, these studies would not have been possible.

To my mother, Weiyu Hao, and my father, Honggang Wang, thank you for all the support throughout this journey. It is only with your support, that I am able to pursue this career path.

To my close friends outside of research: Andrew Han, Soon-Ping Wang, Nathan Lee, Philmo Gu, Neon Li, Christopher Chow, Muyu Luhuang, Yuxuan Jiang, Benjamin Tsui, and Bismarck Leung. Thank you for your support, it is only because of you that I was able to be successful in overcoming the challenges of a Ph.D. degree.

To those who have constantly inspired me: クララ, カレン, thank you. And to you, フィアラ, thank you.

Finally, I would like to thank the Natural Sciences and Engineering Research Council of Canada (NSERC), Alberta Innovates, and the Queen Elizabeth II Scholarship for the financial support through this work.

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Chapter 1

Introduction

1.1 Overview

In recent years, the continuous increase of transistor density on a single chip has dramatically increased the computational power of modern high-tech consumer electronics such as smartphones and personal computers. This trend of increasing transistor density is known as Moore's Law [1] and was primarily enabled through the continuous downscaling of transistor dimensions. The downscaling of transistor dimensions allows for more transistors to be packed into the same area, which increases overall chip performance. However, numerous challenges, such as the increase in power density as transistor density increases, continue to arise with this trend of downscaling. As a result, it is widely believed that Moore's Law is no longer sustainable. As seen in the International Roadmap for Devices and Systems (IRDS) [2], [3] , transistor gate lengths are no longer expected to shrink after 2028, and there are currently no manufacturable solutions for achieving many performance requirements beyond 2025. To satisfy the continuous demand of higher performance and lower energy consumption for use in current and emerging applications such as Artificial Intelligence and Internet-of-Things, further innovation at the device level is required.

While many emerging technologies are being pursued in parallel, the use of ferroelectric materials in micro- and nano-electronic devices has been considered a promising option in recent years, primarily in the form of negative-capacitance field-effect transistors (NCFETs) [4]. While further experimental work is still necessary to fully optimize NCFETs for commercial fabrication, theoretical work utilizing detailed simulations is also necessary both to enhance the understanding of physical phenomena in these devices, and to rapidly predict device performance without employing the extremely costly process of fabricating high-quality prototypes. Towards this end, we will use a variety of simulation tools to investigate the potential of ferroelectric materials for use in radio-frequency applications, primarily focusing on NCFETs.

The rest of this chapter and report is structured as follows: Section 1.2 will cover the necessary background information about negative capacitance in ferroelectrics and outline the basic operating principle of NCFETs, Section 1.3 will summarize the overall aims of this work, and Section 1.4 will summarize each stage of this work. Chapter 2 will be a detailed examination of the general RF performance of NCFETs, Chapter 3 will be a detailed examination of a method to enhance the unity-current-gain, cut-off frequency via the use of NCFETs, Chapter 4 will examine the use of ferroelectrics to construct a tunable oscillator, and Chapter 5 will summarize the key conclusions of this work and propose a future study on the RF linearity of NCFETs.

1.2 Background

1.2.1 Overview of Ferroelectric Materials

Ferroelectric materials are materials that can sustain two equal and opposite polarizations without an applied electric field. This sustained polarization is caused by the displacement of one or more ions in the lattice structure from the position required for the unit cell to have no distinctive positively or negatively charged sides [5]. Under the application of a sufficiently large electric field, the ions can be made to move into another configuration, which switches the sustained polarization into a new value that is equal and opposite to that of the initial polarization [5], [6].

Using HfO_2 as an example, a sketch of the two polarization states is illustrated in Fig. 1.1 (approximate atom positions adapted from [5]). On the left-hand side of Fig. 1.1, the ferroelectric is in one polarization state (State A), with the polarization pointing up. In this case, the positively charged side is on the top of the unit cell, and the negatively charged side is on the bottom of the unit cell. Upon application of a sufficiently large electric field antiparallel to the polarization, oxygen ions in the unit cell are shifted to a new arrangement where the polarization is equal in magnitude but opposite in direction compared to the initial state (State B). This opposing state is sketched on the right-hand side of Fig. 1.1, where the polarization points down. Once the transition from State A to State B occurs, the ferroelectric will remain in State B even if the applied electric field is removed. A transition back to State A from State

B can be induced via an application of a sufficiently large electric field antiparallel to the polarization in State B.

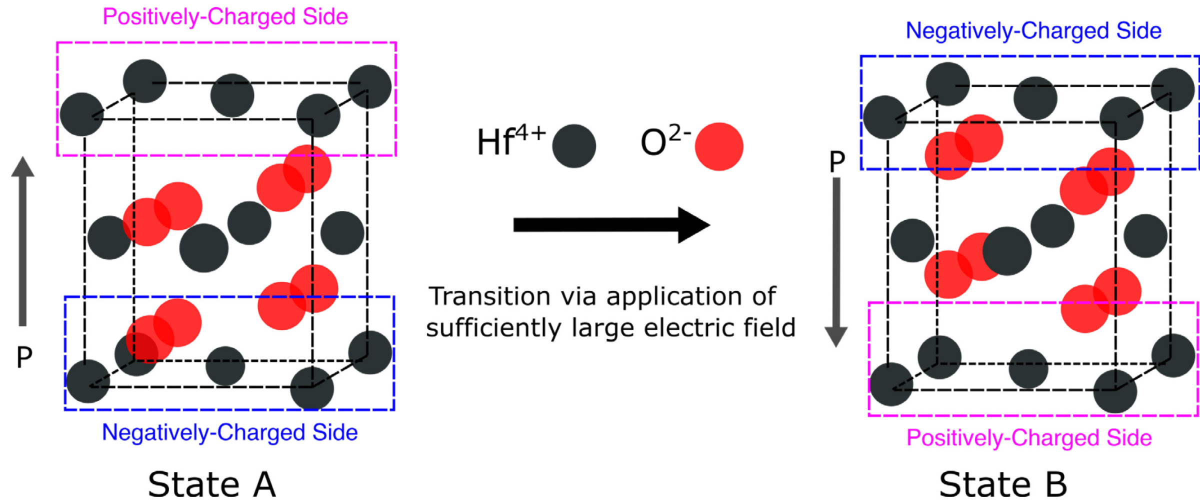


Fig. 1.1 Sketch of the lattice structure and the switching process of ferroelectric HfO_2.

With the aim of exploiting this switchable polarization, ferroelectric materials have been researched since the 1950s for potential applications in non-volatile memory devices. However, early research was mainly focused on lead zirconium titanate (PZT) or barium titanate (BTO) [5], which are not useful for modern applications due to their limited scalability [7]. Modern NCFET research mainly focuses on ferroelectric materials based on HfO_2, which were discovered in 2011 [8], where ferroelectric behavior is commonly induced via doping of pure HfO_2 [9].

1.2.2 The Landau-Khalatnikov Equation for Ferroelectrics

The relationship between polarization and electric field in a ferroelectric can be described using the phenomenological Landau-Khalatnikov (LK) equation [10], [11]:

$$E(t) = 2\alpha P(t) + 4\beta P^3(t) + 6\gamma P^5(t) + \rho \frac{dP(t)}{dt} \tag{1.1}$$

where E is the applied electric field, P is the polarization, $\alpha, \beta,$ and γ are material parameters that characterize lossless behavior of the ferroelectric, and ρ is the damping parameter that characterizes loss within the ferroelectric. It is important to point out that the value of α is

negative for ferroelectric materials, which has implications on their behavior, as explained below.

In the steady state, where the time derivative vanishes, the electric field versus polarization relationship follows an "S"-shape as seen in the red line in Fig. 1.2, with a region of negative dP/dE appearing near the origin because of the negative α term. In addition to this simple description, further details, such as the spatial variation of the polarization throughout the ferroelectric, can also be added to enhance the accuracy of the LK model [10]–[13]. However, since the simplified version of the model is sufficient to illustrate the basic principles of NCFET operation, it will be used throughout this introductory chapter.

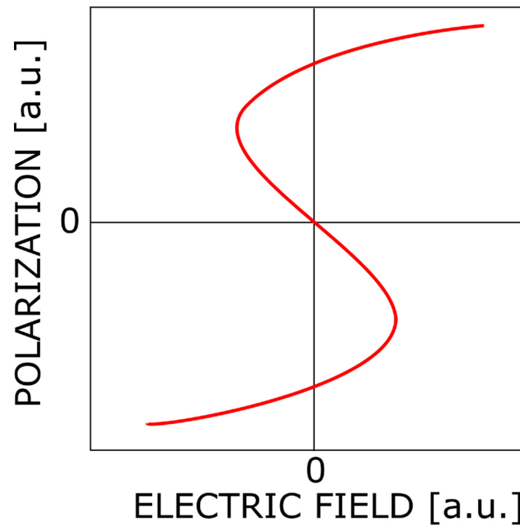


Fig. 1.2 S-shaped curve from the LK equation.

1.2.3 Negative Capacitance in the Ferroelectric

To understand the basic principles of NCFETs, it is first important to see how negative capacitance manifests in the ferroelectric material. Using the S-shaped curve as shown in Fig. 1.2, along with basic electrostatic relations, we will show in this section that the center region of the S-shaped curve that has a negative dP/dE slope corresponds to a negative capacitance.

In a parallel-plate capacitor with an insulator material sandwiched between two metal plates, the charge on the plates of the capacitor can be approximated as follows:

$$Q \approx PA \tag{1.2}$$

where Q is the charge on the metal plate, P is the polarization of the dielectric material, and A is the area of the capacitor.

Similarly, the voltage applied across the capacitor can be approximated as follows:

$$V = \frac{E}{t} \tag{1.3}$$

where E is the electric field inside the dielectric, and t is the thickness of the dielectric material.

Utilizing (1.2) and (1.3), we can see that the charge Q on a capacitor is proportional to the polarization P, and the voltage V is proportional to the electric field E. As such, capacitance, which is expressed by dQ/dV, is proportional to dP/dE, which is in turn the slope of the line shown in Fig. 1.2. Therefore, we can see that the middle region near the origin in Fig. 1.2 effectively exhibits a negative capacitance.

The value of this negative capacitance near the origin can be obtained by ignoring the P^3 and P^5 terms in (1.1) along with the time-derivative term, and substituting (1.2) and (1.3) into (1.1):

$$C'_{\mathrm{FE,n}} = \frac{1}{2\alpha t_{\mathrm{FE}}} = -\frac{1}{2|\alpha| t_{\mathrm{FE}}} \tag{1.4}$$

where $C'_{\mathrm{FE,n}}$ is the negative capacitance of the ferroelectric normalized to the cross-sectional area, t_{FE} is the thickness of the ferroelectric, and α is a material parameter as previously defined.

1.2.4 Illustration of Benefits of NCFETs

The NCFET device, first proposed in 2008 [4], is a traditional MOSFET device with a ferroelectric layer incorporated in addition to the gate dielectric layer. The goal of this device is to exploit the negative capacitance near the origin of the S-shaped curve to enhance the performance of existing FETs. A schematic diagram of an NCFET can be found in Fig. 1.3(a).

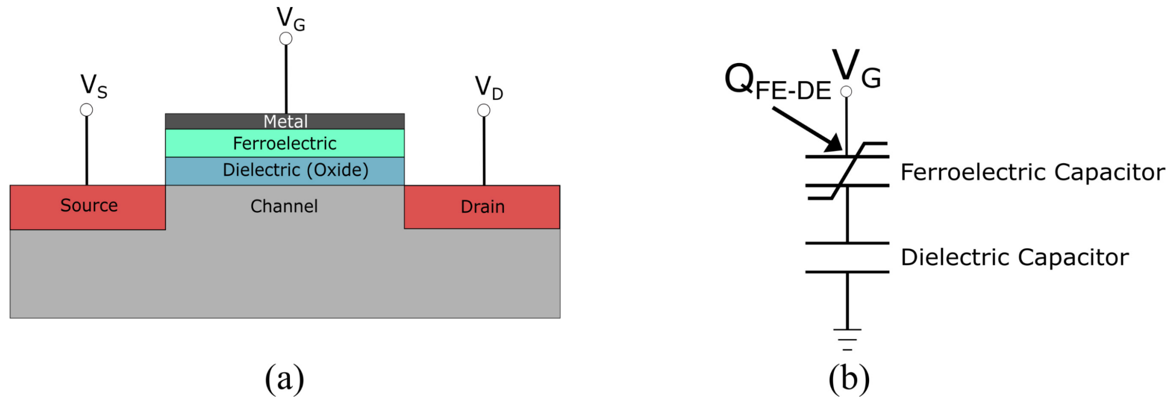
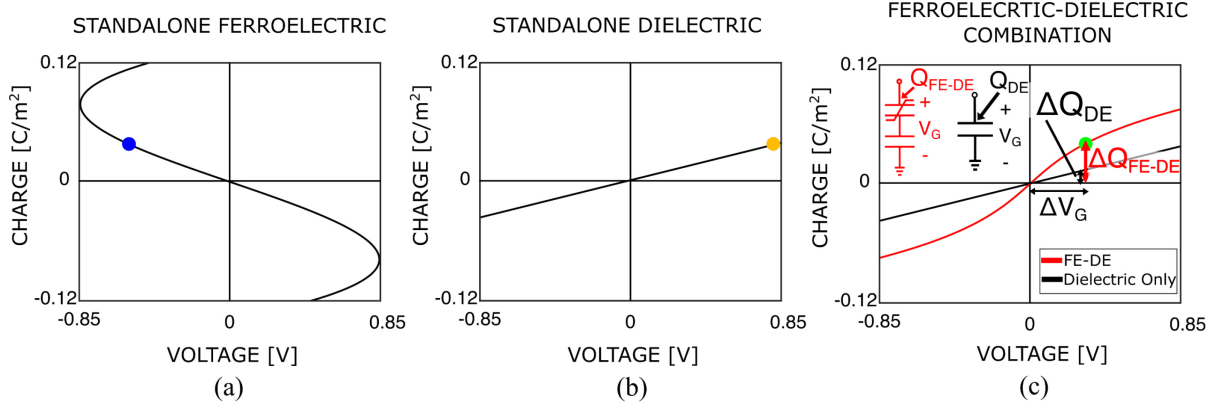


Fig. 1.3 (a) Schematic diagram of an NCFET device. (b) Simplification of the NCFET structure into two series capacitors, where in this formulation the gate oxide stack of the MOSFET has been simplified to a linear dielectric capacitor, and the three-terminal transistor is simplified to two terminals (*e.g.*, corresponding to $V_D = V_S = 0$).

The benefits of NCFETs can be established through a zeroth-order analysis, where the usual input capacitance of the MOSFET is simplified to a linear dielectric capacitance arising from the dielectric layer, and the ferroelectric, which gives rise to its own non-linear capacitance, is placed in series with this layer, as seen in Fig. 1.3(b). Correspondingly, the gate voltage of the transistor is represented by the voltage applied across the two capacitors, and the charge in the transistor channel is represented by the charge on the bottom plate of the dielectric capacitor and is equal in magnitude to the charge on the top plate of the capacitor stack.

Using this representation, the performance improvement in NCFETs can be visualized through an analysis of the charge-voltage relationship of the simplified capacitor stack. In Fig. 1.4(a), the charge-voltage characteristic of the ferroelectric is shown. It has the same shape as the polarization-electric field relation of Fig. 1.2 because polarization is directly proportional to charge, and electric field is directly proportional to voltage, as previously discussed in Section 1.2.3. The well-known linear charge-voltage relation of the dielectric capacitor is shown in Fig. 1.4(b). Finally, to obtain the charge-voltage relation of the combined stack, the fact that charge is uniform across all capacitors in a series stack can be utilized, and the combined charge-voltage relation can be obtained by summing the voltage values from Fig. 1.4(a) and (b) at the same charge values. For example, the green dot on Fig. 1.4(c) is obtained by adding the voltage values of the blue dot in Fig. 1.4(a) and orange dot in Fig. 1.4(b). The result of this procedure can be seen in the red curve of Fig. 1.4(c).



(a) (b) (c)

Fig. 1.4 (a) The charge-voltage relationship for a standalone ferroelectric capacitor. (b) The charge-voltage relationship for a standalone dielectric capacitor. (c) The charge-voltage relationship for a ferroelectric-dielectric series stack plotted on the same axes as the standalone dielectric capacitor. The ferroelectric-dielectric series stack is represented by the red curve. The circuit configurations corresponding to the black and red curves are drawn as insets.

The potential performance improvement in NCFETs can be seen by comparing the charge vs. voltage curves of the NCFET and MOSFET, represented by the red and black curves in Fig. 1.4(c), respectively. As seen from these two curves, the NCFET has a higher charge $Q_{\mathrm{FE-DE}}$ for a given gate voltage V_G in comparison to the MOSFET. In addition, the NCFET has a higher change in charge $\Delta Q_{\mathrm{FE-DE}}$ for a given change in gate voltage ΔV_G near the origin. It is also worth noting that the result for the charge vs. voltage curve shown in Fig. 1.4 is expected given the fact that the ferroelectric exhibits a negative capacitance near the origin, *i.e.*, the result discussed here can also be derived by using the capacitance formula for two capacitors in series and giving a negative capacitance to one of the capacitors.

The characteristics seen in the charge-voltage behavior can be translated to the on-current I_{on} of a FET via the classical FET relation, where in the on-state, the drain current only consists of drift current:

$$I_{\mathrm{on}} = -v|Q_{\mathrm{ch}}|W \tag{1.5}$$

where Q_{ch} is the charge in the channel, W is the width of the channel, and v is the drift velocity of electrons in the channel.

As seen from (1.5), the drain current is proportional to the charge in the channel, the latter being equal in magnitude to $Q_{\mathrm{FE-DE}}$. Therefore, an NCFET is expected to have a higher on-

current according to (1.5) and Fig. 1.4(c), which is beneficial for performance because a higher on-current allows a FET to charge a load capacitance faster.

Further, the higher $\Delta Q_{\mathrm{FE-DE}}$ for a given ΔV_G for NCFETs near the origin can be translated to better subthreshold slope. Classically, the subthreshold slope of a transistor can be approximated as follows:

$$\text{Subthreshold Slope} = \frac{\partial V_G}{\partial \log_{10}(I_D)} = 2.3V_T * \left(1 + \frac{C_S}{C_{\mathrm{ox}}}\right) \quad (1.6)$$

where C_S is the semiconductor capacitance of the FET in the subthreshold region, C_{ox} is the capacitance of the oxide layer, and V_T is the thermal voltage.

Using the results from Fig. 1.4(c), the higher $\Delta Q_{\mathrm{FE-DE}}$ for a given ΔV_G compared to the MOSFET signifies a higher capacitance in NCFETs compared to MOSFETs, which translates to an effectively higher C_{ox} value in (1.6). As such, it can be inferred from (1.6) that the NCFET is also expected to have a lower subthreshold slope compared to the MOSFET. A lower subthreshold slope will allow NCFETs to be turned on with a lower gate voltage compared to standard FETs, which is beneficial in helping to reduce the supply voltage. Further, given similar on-current, lower subthreshold slope can also yield a lower off-current [*e.g.*, as illustrated in Fig. 1.5(a)], which is beneficial for reducing the standby power of FETs.

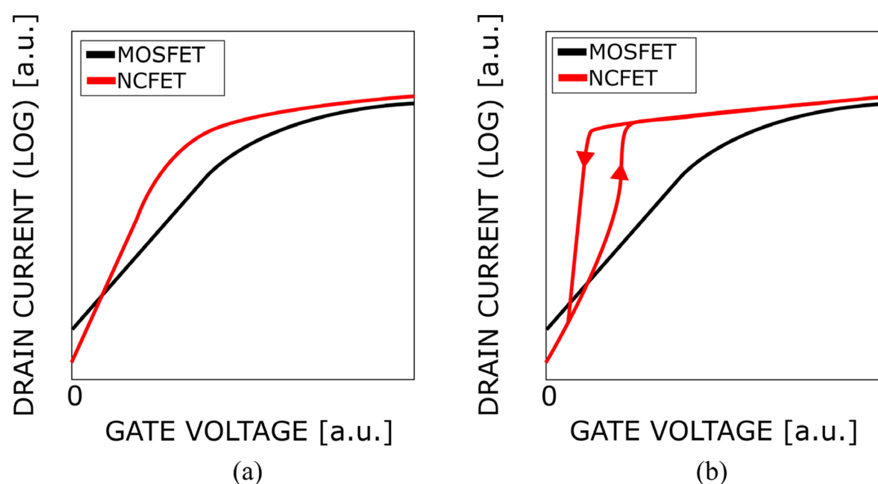
In addition to these two basic performance benefits in on-current and subthreshold slope, other advantages of the NCFET more recently unveiled will be discussed in Section 1.2.6.

1.2.5 Capacitance Matching, Hysteresis, and Stability in NCFETs

One important caveat to the potential performance benefits of an NCFET is that the ferroelectric and gate dielectric layers must be carefully picked for the NCFET to function as expected. This process, known as "capacitance matching" in the literature [4], is necessary to ensure that the I_D-V_G behavior of the FET is *non-hysteretic*.

In the non-hysteretic case, the NCFET I_D-V_G characteristic will behave like a normal MOSFET, albeit with a steeper subthreshold slope and higher on-current, as discussed in Section 1.2.4. In the hysteretic case, the NCFET will follow two different current trajectories

when turning on and turning off, which is generally not desirable. The non-hysteretic and hysteretic I_D-V_G NCFET characteristics can be found in Fig. 1.5 (a) and (b) below, respectively.



(a) (b)

Fig. 1.5 (a) Illustration of the non-hysteretic I_D-V_G behavior. (b) Illustration of the hysteretic I_D-V_G behavior, where the arrow indicates direction of travel on the hysteresis when V_G is increased and decreased.

Physically, hysteresis could manifest in an NCFET because the negative capacitance region in the ferroelectric is in fact *unstable*, and the overall ferroelectric polarization exhibits a bistable, hysteretic behavior [14]. In an NCFET configuration, this unstable negative capacitance becomes accessible because it is *stabilized* by a suitable positive capacitance from the underlying FET capacitance, which consists of the capacitance of the gate dielectric layer and the semiconductor capacitance from the channel. As such, if the gate dielectric layer of the FET is *unsuitable*, *i.e.*, capacitance matching between the ferroelectric and dielectric layers is not properly conducted, then the negative capacitance cannot be stabilized. In this case, the FET will exhibit bistable behavior akin to the ferroelectric, manifesting as a hysteretic I_D-V_G behavior [4], [14].

Thus far, numerous works have studied the conditions under which hysteresis manifests in the NCFET. In its most basic form, the condition to avoid hysteresis in an NCFET involves ensuring that the series capacitance of the ferroelectric-dielectric stack is positive, *i.e.*,

$$C_{\mathrm{tot}} = \left(\frac{1}{C'_{\mathrm{FE,n}}} + \frac{1}{C_{\mathrm{DE}}}\right)^{-1} > 0 \tag{1.7}$$

$$C'_{\mathrm{FE,n}} = \frac{1}{2\alpha t_{\mathrm{FE}}} = -\frac{1}{2|\alpha| t_{\mathrm{FE}}} \tag{1.8}$$

where $C'_{\mathrm{FE,n}}$ is the negative capacitance of the ferroelectric, which can be approximated by (1.4), repeated here as (1.8), and C_{DE} is the capacitance of the dielectric layer in the MOSFET.

Alternatively, the capacitance matching condition illustrated in (1.7)–(1.8) can be visualized as requiring the combined Q-V curve near the origin in Fig. 1.4(c) to exhibit a positive slope [4]. In addition to the most basic capacitance matching condition illustrated above, it has also been discovered that leakage current through the ferroelectric and domain formation in the ferroelectric could also have a significant impact on whether or not hysteresis is observed [15], [16]. The impacts of these more recent discoveries on the field will be discussed in Section 1.2.6.

1.2.6 Recent Progress

Since the inception of NCFETs in 2008, significant progress has been made on all fronts of research on these novel devices, including the design of the device structure, the choice of relevant figures of merit, and alternative applications of the negative-capacitance effect beyond their use in a gate stack. This section will briefly summarize these recent developments in the literature, to further establish context for the current work. While research related to devices will be the primary focus of this section to keep the summary concise, it is important to point out that this research is often interconnected with research that focuses on understanding the nature of negative capacitance, such as those into ferroelectric domains (*e.g.*, [17]–[19]) and those into alternatives to the LK model (*e.g.*, [20]–[22]), and both research directions equally contribute toward potential adoption of these devices in the future.

In early experimental works [23]–[25], NCFETs had widely used the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure for the gate stack, seen in Fig. 1.6(a). This closely mimics the initial idea of connecting a ferroelectric capacitor to the gate of a traditional transistor and allows for experiments to be conducted using separately fabricated ferroelectric capacitors and transistors, lowering the overall fabrication difficulty. However, these experiments typically produced large hysteresis in the I_D-V_G characteristics of the transistor, which is undesirable [14]. Recently [15], [16], it has been shown that the MFMIS structure destabilizes the ferroelectric-dielectric stack due to leakage currents and ferroelectric domain formation. As a result, investigations have since been shifted to the metal-ferroelectric-

insulator-semiconductor (MFIS) structure shown in Fig. 1.6(b), where the stabilization of the stack is unaffected by these effects.

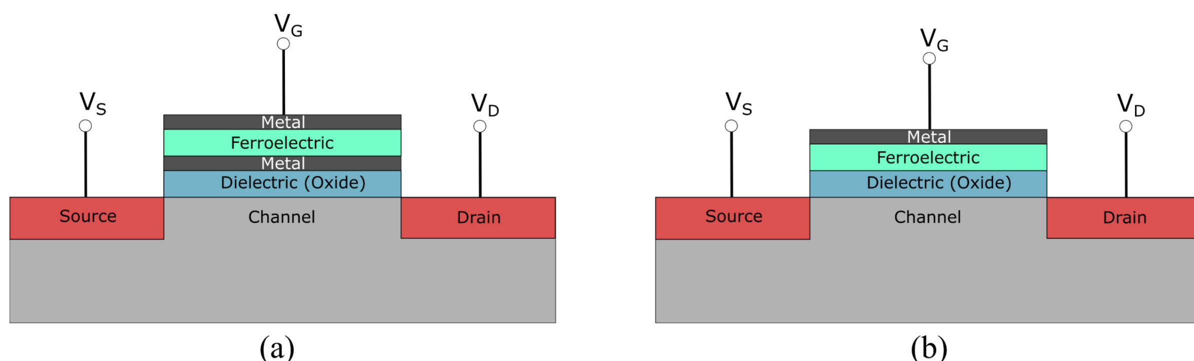


Fig. 1.6 (a) The metal-ferroelectric-metal-insulator-semiconductor NCFET and (b) the metal-ferroelectric-insulator-semiconductor NCFET.

As a result of this shift in device structure, recent experimental works with the MFIS configuration have shown negligible hysteresis compared to early experimental works [26]–[28]. Simultaneously, while early experimental works focused on planar transistors with relatively large dimensions [29], [30], recent experimental work focused on smaller transistor nodes of the IRDS, and particularly on FinFETs, which are used in state-of-the-art transistor nodes. Successful integration into a commercial 14-nm process was also shown in 2017 by Global Foundries [31], further demonstrating the promise of these novel devices.

In terms of device figures of merit, early works focused on the reduction of subthreshold slope (SS) below the thermionic limit of 60 mV/dec at room temperature, and NCFETs were seen as a promising steep-slope device [4], [23], [24]. However, it was recently shown that NCFETs are in fact unlikely to be suitable as steep-slope devices [32]. This is because if the capacitance matching is constructed in such a way to accomplish sub-thermionic SS, the capacitance matching criteria in (1.7)–(1.8) is difficult to satisfy once the transistor is turned on, due to the non-linear behavior of the FET input capacitance. As such, NCFETs designed to achieve sub-thermionic SS will likely be hysteretic. Therefore, recent studies have shifted focus away from achieving sub-thermionic SS, and instead on the potential for NCFETs to improve short-channel effects such as drain-induced barrier lowering (DIBL) and r_o at a given channel length [14], [33], [34], as well as simply improving SS without necessarily being

below the thermionic threshold (*i.e.*, not necessarily below 60 mV/decade at room temperature) [26], [27]. Furthermore, recent studies have demonstrated the promising effect of using the ferroelectric negative capacitance as a way to continue to decrease the effective oxide thickness (EOT) of modern FET gate stacks to improve performance, while avoiding the negative effects of the current state-of-the-art solution known as interfacial layer scavenging [28], [35].

As channel length continues to scale down, NCFETs have also been shown to be more resilient to the negative effects of short channel effects [36], [37] and demonstrate potential for extremely scaled nodes down to the end of the IRDS [34]. In addition to scaled silicon FETs, NCFETs have also demonstrated improved performance with 2-D channel materials [20], [38], [39], further demonstrating the promising potential of these devices.

Thus far, one direction for NCFETs that has not yet been thoroughly investigated in the literature is their radio-frequency (RF) performance. As the field of NCFETs continues to mature, it is beneficial to also explore the RF performance of these novel devices to evaluate their potential in future RF nanoelectronics.

In addition to NCFETs, which is inherently a front-end-of-the-line (FEOL) application, where the ferroelectric layer is integrated with the transistor and fabricated together, the use of ferroelectric as a standalone, back-end-of-the-line (BEOL) element is also an important direction, as it avoids the need to fabricate a high-quality ferroelectric directly on top of the gate oxide of an advanced FET. Thus far, most of the exploration of BEOL applications have been focused on their use as a memory element [40]–[42]. However, it has been recently proposed that a negative capacitance from a standalone ferroelectric capacitor, when used in conjunction with active feedback, can be used to improve the cut-off frequency of a transistor [43]. Given that there have not yet been any other explorations into the BEOL use of ferroelectric negative capacitance, and given the promising results of [43], it is valuable to explore how a standalone ferroelectric capacitor in BEOL could be used to improve existing RF circuitry in addition to investigating the RF performance of NCFETs.

1.3 This Work

Based on the discussion thus far, this work explores the potential of ferroelectric materials for applications in future radio-frequency (RF) nanoelectronics, with a primary focus on NCFETs. To rapidly forecast the performance of these novel devices without employing the costly process of fabricating high-quality prototypes, this work utilizes a variety of numerical simulation tools to explore ferroelectric devices for use in future RF nanoelectronics. To achieve this goal, the following specific tasks are completed:

1. An initial assessment of the general RF performance potential of NCFETs constructed with the MFIS structure by evaluating three critical figures of merit: the cut-off frequency (f_T), the maximum oscillation frequency ($f_{\max}$), and $g_m f_T / I_D$. The final figure of merit is one is that captures DC power consumption in addition to RF performance.
2. A further in-depth assessment of the RF performance of NCFETs by investigating their potential to improve the extrinsic cut-off frequency ($f_{\mathrm{T,e}}$) and $g_m f_T / I_D$ via mitigating the impact of extrinsic parasitic capacitances.
3. An exploration of the potential of utilizing ferroelectric negative capacitance in BEOL RF applications by investigating the possibility of using a ferroelectric to build a highly tunable oscillator.

These three tasks naturally form the three stages of this Ph.D. research, with each stage achieving the goals outlined above. Together, these three stages aim not only to enhance the understanding of physical effects in these novel ferroelectric devices and provide further insights with regards to operating principles, but also to serve as first steps towards future experimental investigation and fabrication of ferroelectric devices for use in RF nanoelectronics. Overall, the results of this work will contribute to the on-going efforts of improving the performance of nanoscale devices and circuits, which will be crucial towards enabling computationally demanding emerging and future applications.

So far, the first stage of this work is complete and has led to publication in *IEEE Transactions on Electron Devices* [44]. The second stage of this work is also complete and has

led to publication in *IEEE Transactions on Electron Devices* [45]. The third stage of this work is also complete and will be submitted for publication to an IEEE journal.

1.4 Stages of Work

For the convenience of the readers, a summary of all three stages of this work will be provided in this section.

1.4.1 RF Performance Projections of Negative-Capacitance FETs: f_T, $f_{\max}$, and $g_m f_T/I_D$

Summary:

In recent years, NCFETs have garnered much attention as a solution to continue the scaling of supply voltage. While investigations into dc and digital performance, as well as investigations into the behavior of individual small-signal parameters are abundant in the literature, the general RF performance of NCFETs is an area that has not yet been thoroughly explored. This is especially true for MFIS NCFETs, where there is no metal present between the ferroelectric and the dielectric layer. Investigation using the MFIS structure is of critical importance because it is the more suitable structure for RF applications compared to the MFMIS structure, which was the initial focus of literature on NCFET RF performance [46]–[49]. The MFMIS structure is unsuitable for RF applications because NCFETs with this structure would exhibit hysteresis [16].

Towards this end, this stage utilizes simulations via COMSOL Multiphysics and small-signal circuits to investigate the RF performance of MFIS NCFETs using three critical figures of merit: the well-known unity-current-gain cut-off frequency f_T, the well-known maximum oscillation frequency $f_{\max}$, and another important figure of merit specified by $g_m f_T/I_D$, where g_m is the transconductance, and I_D is the dc drain current. This third metric captures dc power consumption in addition to RF performance and has recently become prominent as an RF metric [50], [51], especially for analog/RF circuits [51]. Through this stage, we found that NCFETs can achieve similar f_T and $f_{\max}$ compared to traditional MOSFETs, but can offer a significant advantage in $g_m f_T/I_D$.

A schematic diagram of a baseline MOSFET (Device A) can be found in Fig. 1.7(a), where the dimensions have been set according to the IRDS 10-nm node. To investigate the RF performance of NCFETs in general, rather than evaluating a specific NCFET design, a variety of possible NCFET devices need to be considered.

For this purpose, three different NCFET devices, with lower (Device B1), similar (Device B2), and higher (Device B3) total oxide capacitances were investigated; a schematic diagram of the NCFET devices is shown in Fig. 1.7(b). The total oxide capacitance is calculated as a series combination of the ferroelectric capacitance, approximated as $-1/2|\alpha|t_{\mathrm{FE}}$ [4], and the dielectric oxide capacitance. For each NCFET device, the total oxide capacitance is adjusted by varying the ferroelectric layer thickness t_{FE} and dielectric layer thickness t_{DE}; values for t_{FE} and t_{DE} can be found in Table 1.1. Here, the total stack thickness $t_{\mathrm{stack}} = t_{\mathrm{FE}} + t_{\mathrm{DE}}$ of the NCFETs is kept as the same as the baseline device to accommodate the fact that there are limited amounts of space between fins in advanced nodes. Further details on how the NCFET devices have been selected will be discussed in Chapter 2.

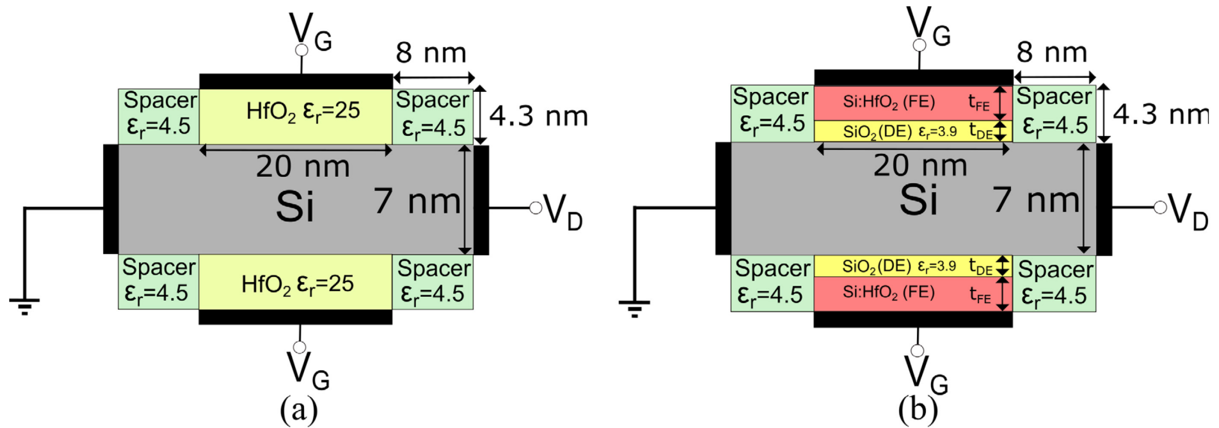


Fig. 1.7 (a) The schematic diagram of the baseline device for this stage. (b) The schematic diagram of the NCFET devices for this stage. The specific values of t_{DE} and t_{FE} can be found in Table 1.1.

Device	Physical Dielectric Thickness (t_{DE})	Physical Ferroelectric Thickness (t_{FE})	Total Oxide Capacitance per Area
A (Baseline)	4.30 nm ($\epsilon_r = 25$)	0 nm	0.0515 $\mathrm{F/m^2}$
B1 (NCFET)	1.00 nm ($\epsilon_r = 3.9$)	3.30 nm	0.0376 $\mathrm{F/m^2}$
B2 (NCFET)	0.67 nm ($\epsilon_r = 3.9$)	3.63 nm	0.0595 $\mathrm{F/m^2}$
B3 (NCFET)	0.39 nm ($\epsilon_r = 3.9$)	3.91 nm	0.1179 $\mathrm{F/m^2}$

Table 1.1 Device dimensions for all devices used in this stage.

All devices are simulated using a modified version of the classical velocity-saturated drift-diffusion equations in COMSOL Multiphysics. The equations are modified to account for quantum confinement effects in the fin width direction using the modified-local-density approximation (MLDA) [52], [53]. The ferroelectric is simulated using the multi-domain LK equation [11], [12].

To evaluate RF performance, the well-known small-signal MOSFET model has been used for the baseline MOSFET [54], and can be seen in Fig. 1.8(a). For the NCFET, an additional resistor $R_{\rho,\text{eff}}$ has been added at the gate to account for damping in the ferroelectric [11], [55], and can be seen in Fig. 1.8(b). The resistance of the damping resistor is determined using an equivalent circuit approach, which accounts for the interaction of the ferroelectric with the non-uniform nature of the FET's channel. Further details regarding the modeling of the damping resistor can be found in Chapter 2.

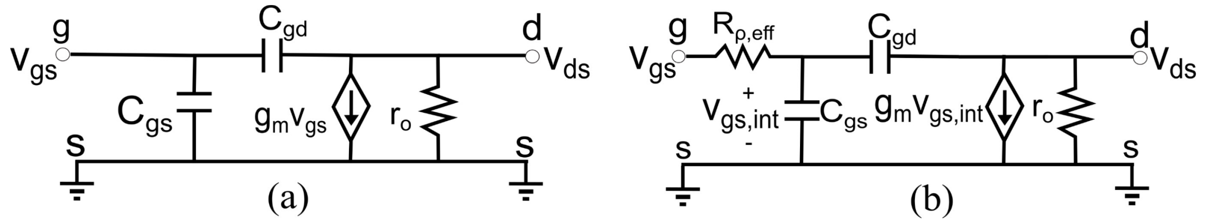


Fig. 1.8 (a) The intrinsic small-signal model used for the baseline MOSFET in this stage. (b) The intrinsic small-signal model used for the NCFETs in this stage.

Extrinsic parasitic elements outside the immediate vicinity of the channel have also been modeled in this stage, with the extrinsic structure shown in Fig. 1.9 below, along with the extrinsic equivalent circuit. Details regarding the extraction process to obtain the values of extrinsic circuit elements shown in Fig. 1.9(b) will be discussed in Chapter 2.

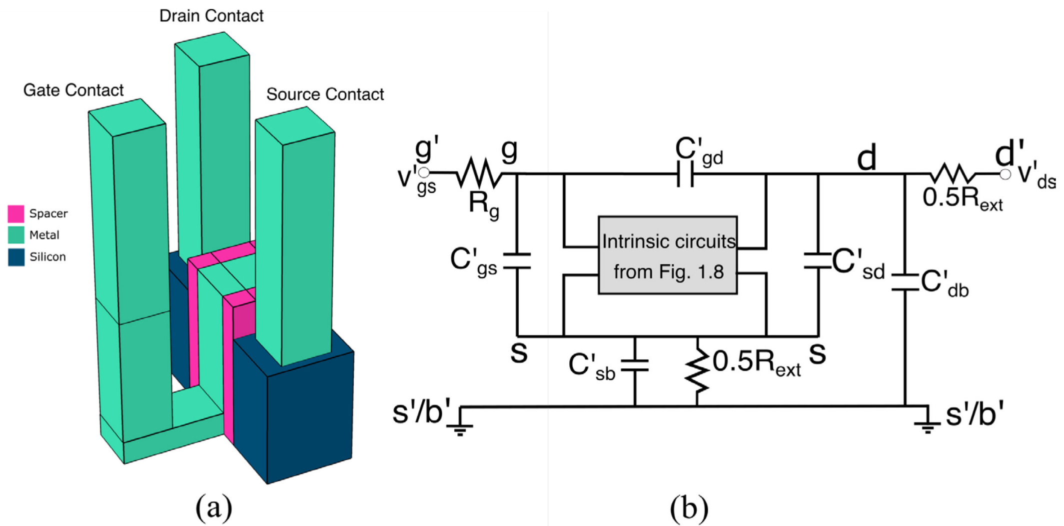


Fig. 1.9 (a) A 3-D schematic of the extrinsic structure. (b) The extrinsic equivalent circuit.

The results for f_T, and $g_m f_T/I_D$ obtained via simulation of equivalent circuits in Fig. 1.8 and Fig. 1.9 can be found in Fig. 1.10 below. As seen from the figures, the f_T of the NCFET devices are very similar to that of the baseline MOSFET, both with and without extrinsic parasitic elements. However, the $g_m f_T/I_D$ values of the NCFETs can be much higher, with up to 51% improvement when compared to the baseline MOSFET.

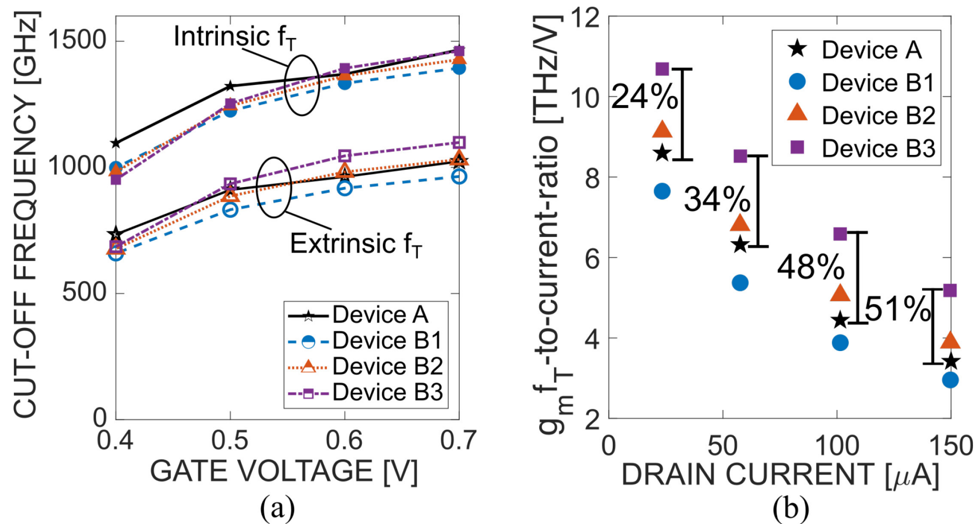


Fig. 1.10 (a) The intrinsic (without extrinsic parasitic elements) and extrinsic (with extrinsic parasitic elements) cut-off frequencies of the devices. (b) The $g_m f_T/I_D$ of the devices.

The reason for the similarity in f_T follows from the approximate formula for f_T [54, Ch. 8]:

$$f_T \approx \frac{g_m}{2\pi C_{\mathrm{gg}}} \tag{1.9}$$

where g_m is the transconductance, and C_{gg} is the input capacitance of the transistor. For an NCFET, negative capacitance from the ferroelectric enhances both the g_m and C_{gg} of the transistor to a similar degree. Since f_T is calculated via a ratio of these two parameters, the simultaneous increases of g_m and C_{gg} counteract each other and lead to similar f_T performance between the two classes of devices. The improvement in $g_m f_T / I_D$ is because g_m / I_D vastly improves while f_T remains similar. These results will be discussed in more detail in Chapter 2.

The results for $f_{\max}$ can be seen in Fig. 1.11(a) below. It is evident from these plots that NCFETs have a lower $f_{\max}$ compared to the baseline MOSFET, which can be attributed to the fact that ferroelectric materials have an additional damping term ρ, which acts as a resistor in an equivalent circuit. This additional damping term effectively increases the gate resistance of an NCFET versus that of the baseline MOSFET, which results in decreased $f_{\max}$. We found that this impact on $f_{\max}$ from the ferroelectric damping can be mitigated through lower damping constant ρ. As seen in Fig. 1.11(b) below, with lower damping constant, NCFETs can achieve similar $f_{\max}$ as the baseline device at a given current.

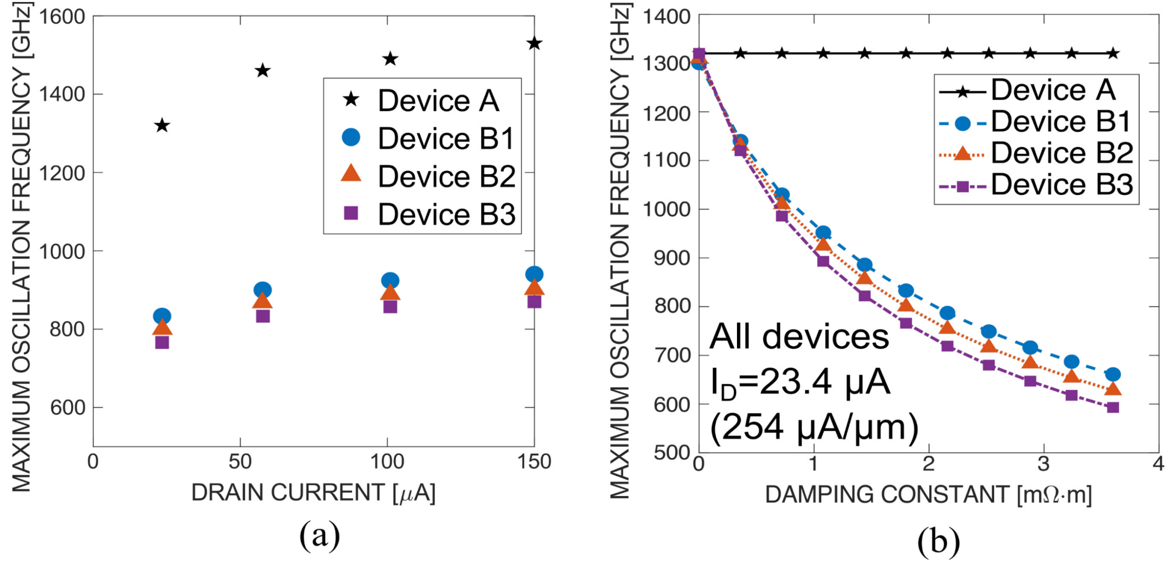


Fig. 1.11 (a) The $f_{\max}$ for each device, showing the NCFET devices (B1 – B3) have a decreased $f_{\max}$ due to ρ. (b) $f_{\max}$ for each device as a function of ρ, showing lower ρ leads to similar performance between the NCFET devices (B1 – B3) and baseline device (A). The dc drain current in each device is the kept the same at 23.4 μA (254 μA/μm).

<u>Key Contributions:</u>

The specific contributions from the first stage of this work, "RF Performance Projections of Negative-Capacitance FETs: f_T, $f_{\max}$, and $g_m f_T/I_D$," are as follows:

1. The f_T, $f_{\max}$, and $g_m f_T/I_D$ performance of NCFETs with the MFIS structure, which is the more practical structure for RF applications, have been investigated, providing a previously unavailable baseline for future studies into the RF performance of NCFETs.

2. Utilizing a combination of physics-based device simulation and small-signal circuits, the f_T of MFIS NCFETs was found to be similar compared to a baseline device for a given technology, as seen from Fig. 1.10 (a).

3. The $f_{\max}$ of NCFETs was found to be negatively impacted by the ferroelectric damping constant, as seen from Fig. 1.11(a). However, it was also found that similar $f_{\max}$ versus a baseline MOSFET device can be achieved if the damping constant is sufficiently low, as seen from Fig. 1.11(b).

4. The $g_m f_T/I_D$, a metric that can simultaneously capture the dc power consumption and RF performance, has been investigated for MFIS NCFETs. The value of $g_m f_T/I_D$ for MFIS NCFETs was found to be much higher compared to that of a baseline device, showing promise for next-generation RF applications with NCFETs, as seen from Fig. 1.10 (b).

1.4.2 Potential Enhancement of f_T and $g_m f_T/I_D$ via the Use of NCFETs to Mitigate the Impact of Extrinsic Parasitics

Summary:

One characteristic that emerged from the general investigation in the first stage, as well as from various studies in the literature, is the ability for NCFETs to simultaneously increase *both* the small-signal parameters g_m and C_{gg}, defined in this context as parameters obtained for an "intrinsic" or core transistor structure (excluding external parasitics). This simultaneous increase in g_m and C_{gg} led to an observation that similar levels of f_T can be attained by an MFIS NCFET compared to a traditional MOSFET in the previous stage; however, this analysis is only applicable for a structure with little or no parasitic capacitances beyond the intrinsic transistor, such as the simple extrinsic structure used in the previous stage for an initial benchmarking of NCFET RF performance.

In this stage, the potential for NCFETs to attain higher f_T in the presence of non-negligible parasitic elements is investigated. This investigation is a natural extension to the general investigation in the previous stage and serves to further unveil the RF performance potential of NCFETs in the context of f_T and $g_m f_T/I_D$.

The intrinsic f_T ($f_{\mathrm{T,i}}$) of a transistor, as seen from the previous stage, can be calculated as follows:

$$f_{\mathrm{T,i}} = \frac{g_m}{2\pi C_{\mathrm{gg}}} \quad (1.10)$$

where a simultaneous increase of g_m and C_{gg} in the NCFET has led to similar values of $f_{\text{T,i}}$ to be observed when compared to a baseline MOSFET. [1]

As we will detail below, when considering an extrinsic structure with non-negligible parasitic elements, the ability to maintain a similar $f_{\text{T,i}}$ while simultaneously having a higher C_{gg} would in fact allow NCFETs to potentially achieve a higher *extrinsic* f_T ($f_{\text{T,e}}$) compared to MOSFETs. Here, "extrinsic" refers to elements arising outside the intrinsic or core transistor structure, and $f_{\text{T,e}}$ is defined as the f_T found with the effects of all extrinsic parasitic elements included.

The potential increase of $f_{\text{T,e}}$ from a *higher* C_{gg} can be intuitively understood through an analysis of the well-known formula for $f_{\text{T,e}}$ [56]:

$$f_{\text{T,e}} = \frac{1}{2\pi} \frac{g_m}{C_{\text{gg}} + C'_{\text{gg}} + \left[\frac{1}{\text{r}_\text{o}}\left(C_{\text{gg}} + C'_{\text{gg}}\right) + g_m\left(C_{\text{gd}} + C'_{\text{gd}}\right)\right](R_s + R_d)} \tag{1.11}$$

where g_m, C_{gg}, and r_o represent the transconductance, gate capacitance, and output resistance taken at the intrinsic terminals (without extrinsic parasitic resistance or capacitance) of the device, C'_{gg} and C'_{gd} represent the extrinsic parasitic capacitances, and R_s and R_d represent the extrinsic parasitic resistances.

Ignoring the effects of the term multiplied by the sum of R_s and R_d, which is typically small compared to the C'_{gg} and C_{gg} terms, and rearranging the formula, the following result can be obtained:

$$f_{\text{T,e}} \approx f_{\text{T,i}} \frac{1}{1 + \frac{C'_{\text{gg}}}{C_{\text{gg}}}} \tag{1.12}$$

Since NCFETs can be fabricated with similar fabrication procedures as standard MOSFETs, a similar device layout can be used, and the value of extrinsic parasitic capacitance C'_{gg} between NCFETs and MOSFETs would therefore be similar. However, NCFETs are expected to have a higher intrinsic capacitance C_{gg} and similar $f_{\text{T,i}}$ compared to MOSFETs, as discussed

[1] In the previous stage, only minimal parasitic elements were modeled in order to simplify the model for an initial probing of NCFET RF performance. To distinguish the results presented in this stage with those presented in the previous stage, all results on f_T from the previous stage, *including* those marked with "extrinsic f_T" in Fig. 1.10, will be redefined as "intrinsic f_T ($f_{\text{T,i}}$)" for the purposes of this stage.

earlier. Using these two observations, it can be seen directly from (1.12) that compared with MOSFETs, NCFETs could potentially achieve a higher $f_{\mathrm{T,e}}$, because a higher C_{gg} will cause the second term of the denominator in (1.12) to decrease, effectively *mitigating* the effects of the extrinsic parasitic capacitance C'_{gg}.

To explore this promising effect, which will be important as transistors continue to scale down and parasitic capacitances become increasingly dominant [51], [57], a simulation strategy similar to the first stage is employed.

Compared to the first stage, the basic approach of using a physics-based MOSFET model in conjunction with a small-signal circuit is unchanged, *i.e.*, for the intrinsic transistor, the same basic approach is used to simulate the devices. However, the intrinsic NCFET structure in this stage differs by being designed to maximize C_{gg} and hence to maximize the potential improvements to $f_{\mathrm{T,e}}$ of an overall extrinsic structure, via the mechanism explained through (1.12). Furthermore, a pair of NCFET and MOSFET devices at the 7-nm node have been simulated in addition to 10-nm devices, which was the node used for the previous stage. Further details of these methodologies, such as the specific design strategy of the NCFET and exact design parameters, are discussed in Chapter 3.

To account for further parasitic capacitance beyond what was modeled in the previous stage, the extrinsic device structure used to obtain parasitic elements in the small-signal circuit has also been refined for this stage. Specifically, a representative multi-finger extrinsic structure [58, Ch. 4] comprised of interconnects up to the M3 metal level has been modeled. This structure can be seen in Fig. 1.12, where the intrinsic structure shown in Fig. 1.7 is a top view of the region enclosed in the dashed box seen in Fig. 1.12(a).

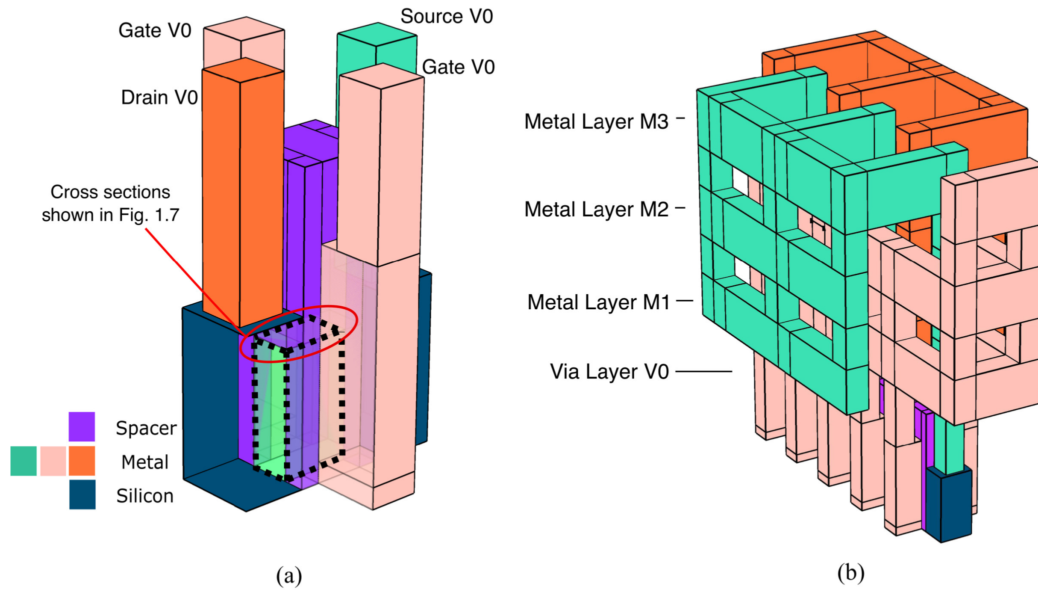


Fig. 1.12 (a) Perspective view of one fin of the refined extrinsic structure. The cross sections of Fig. 1.7 are a top view of the dashed box. (b) Perspective view of the refined structure, with all fins and interconnects up to M3, constructed by putting five units in Fig. 1.12(a) in a row, and building interconnects around them.

The basic results for f_T and $g_m f_T / I_D$ can be seen in Fig. 1.13,[2] where a 20% improvement of $f_{\mathrm{T,e}}$, and an 80% improvement of $g_m f_T / I_D$ can be observed in the NCFETs in comparison to the baseline MOSFET. It is worth noting that for this stage, the variable plotted on the x-axis has been changed from V_G to I_D to allow for comparison under the same power consumption, calculated as $P = V_{\mathrm{DD}} I_D$. The I_D values of the MOSFET and NCFET devices are matched by tuning the gate voltage of the NCFET until its I_D matches that of the MOSFET.

[2] It is worth clarifying that the quantity $g_m f_T / I_D$ is calculated with the "extrinsic" versions of the variables g_m, f_T, and I_D, where the effects of the structure beyond the "core" transistor are included. Specifically, this means that the quantity $f_{\mathrm{T,e}}$ is to be used for f_T in this calculation.

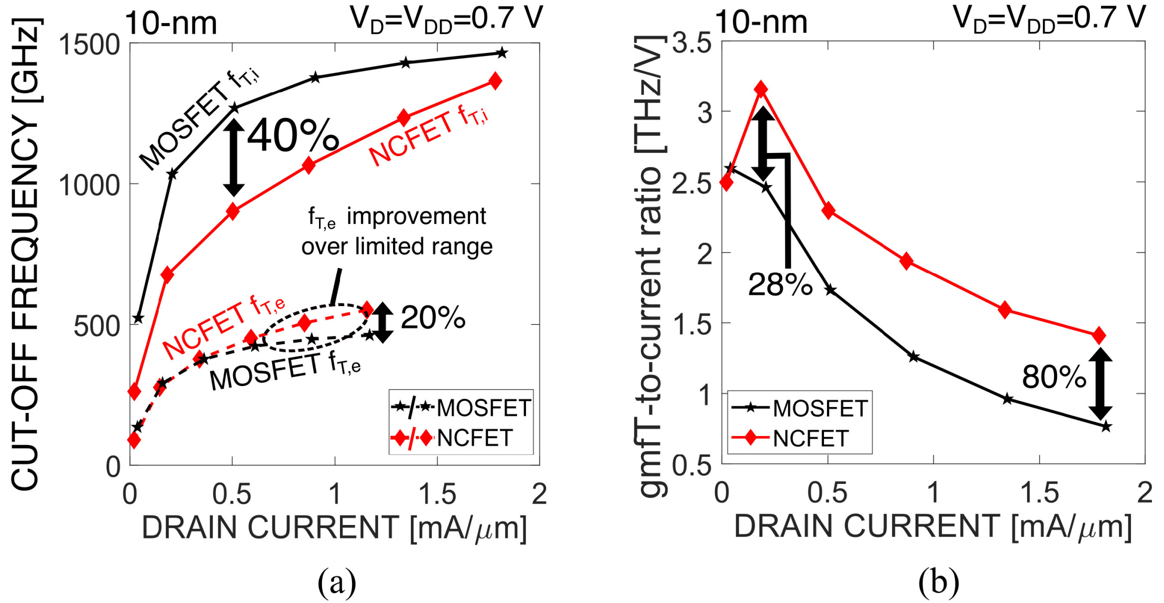


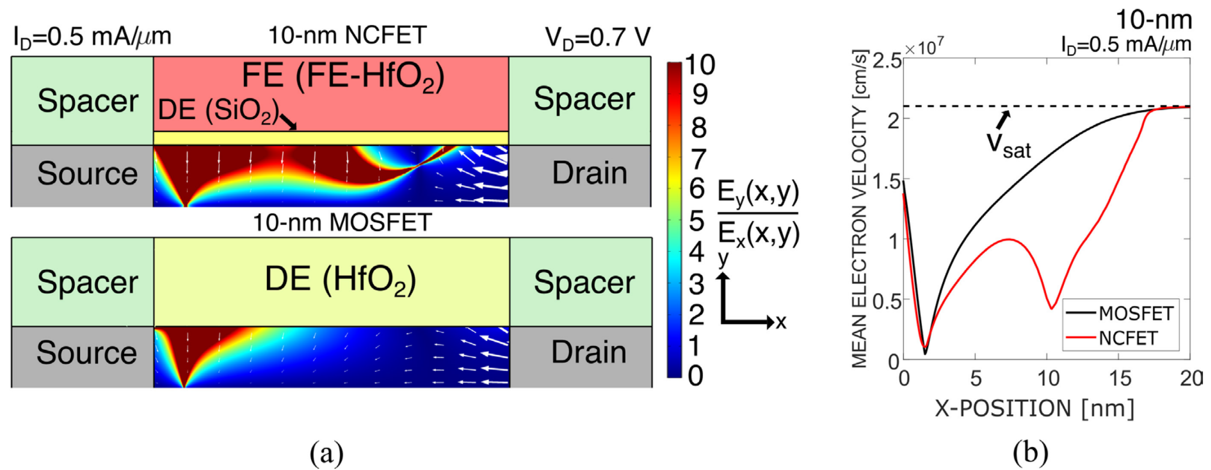
Fig. 1.13 (a) $f_{\mathrm{T,e}}$ and $f_{\mathrm{T,i}}$ of the 10-nm MOSFET and NCFETs used in this stage. (b) $g_m f_T / I_D$ of 10-nm MOSFET and NCFET used in this stage.

These observations follow from the basic premises of (1.12), with the NCFET sustaining a similar $f_{\mathrm{T,i}}$ but with its higher intrinsic gate capacitance C_{gg} used to mitigate the degradation of $f_{\mathrm{T,e}}$ from $f_{\mathrm{T,i}}$ due to C'_{gg}. In technology nodes utilizing FinFETs, the $f_{\mathrm{T,e}}$ is expected to decrease as devices scale down due to excessive parasitic capacitances. In this case, a 20% improvement is sufficient in bringing the $f_{\mathrm{T,e}}$ values back to similar levels of a prior node [57].

One undesirable feature observed in Fig. 1.13(a) is a general reduction of $f_{\mathrm{T,i}}$ for NCFETs. This reduction can be seen most prominently at lower currents in Fig. 1.13(a), *e.g.*, at $I_D = 0.5\ \mathrm{mA/\mu m}$, the NCFET $f_{\mathrm{T,i}}$ is 40% lower than that of the MOSFET. Following from the discussions surrounding (1.12), even if NCFETs offer a decrease of $C'_{\mathrm{gg}}/C_{\mathrm{gg}}$ ratio, improvement in $f_{\mathrm{T,e}}$ is diminished if $f_{\mathrm{T,i}}$ decreases.

The diminishing performance due to a reduction of $f_{\mathrm{T,i}}$ is evident from the lower two curves of Fig. 1.13(a) and the curves in Fig. 1.13(b), where the NCFET only exhibits an advantage to $f_{\mathrm{T,e}}$ for a limited range of higher operating currents, and where the $g_m f_T / I_D$ of NCFETs is only 28% higher than that of the MOSFET at the lower currents compared to 80% in the fully-on state. As such, this reduction of $f_{\mathrm{T,i}}$ in NCFETs could limit the potential of improvement in $f_{\mathrm{T,e}}$ explained via (1.12), and therefore will need to be addressed.

The origin of this decrease in $f_{\mathrm{T,i}}$ stems from the unconventional electrostatics of the NCFET. In essence, fields from the drain of the NCFET, in conjunction with the negative capacitance of the ferroelectric, serve to *effectively* increase the *electrical* channel length of the NCFET compared to a traditional MOSFET, despite both devices having the same *physical* channel length. This increase in electrical channel length is supported by various physical quantities plotted in Fig. 1.14, where the NCFET would have a more dominant gate (vertical direction) field as well as a lower electron velocity compared to that of the MOSFET. Further details with regards to this increase in electrical channel length will be discussed in Chapter 3.



(a) (b)

Fig. 1.14 (a) Electric-field ratio between the gate-direction (y-direction) and transport-direction (x-direction) field for 10-nm NCFET and MOSFET at $I_D = 0.5$ mA/μm. (b) Electron velocities in the channel region for the 10-nm MOSFET and NCFET at $I_D = 0.5$ mA/μm.

In previous studies, this effective increase in electrical channel length has been observed through the improvement of drain-induced barrier lowering (DIBL), and the improvement of r_o [26], [31], [33], [34], [59]. Here, this increase in *electrical* channel length decreases $f_{\mathrm{T,i}}$ in the NCFET, analogous to the well-known effect where a longer physical channel leads to a decrease of $f_{\mathrm{T,i}}$.

To alleviate the degradation in $f_{\mathrm{T,i}}$, two strategies are explored. The first strategy is to consider what occurs when the physical channel length L_G of both the NCFET and the MOSFET are downscaled, which exploits the fact that the $f_{\mathrm{T,i}}$ of both MOSFET and NCFET devices are expected to converge towards the short-channel limit of $(3/2) \times v_{\mathrm{sat}}/2\pi L_G$ as channel length decreases [54, Ch. 8]. A second strategy is to adjust the threshold voltage V_{th}

and supply voltage V_{DD} of the NCFET such that it will have a higher current at the same dc power. This second strategy is expected to alleviate the degradation in $f_{\mathrm{T,i}}$ because $f_{\mathrm{T,i}}$ generally increases with current as seen from Fig. 1.13(a). Further details to both strategies are discussed in Chapter 3.

The effects of both strategies outlined above can be seen in Fig. 1.15. In Fig. 1.15(a), the degradation of $f_{\mathrm{T,i}}$ as a function of gate length is investigated, and it is evident that as L_G decreases, the degradation of $f_{\mathrm{T,i}}$ is alleviated, especially for FETs operating at low powers. In Fig 1.15(b), it is evident that the adjustment of V_{DD} and V_{th} also helps to alleviate $f_{\mathrm{T,i}}$ degradation, primarily for devices operating at higher powers near the fully-on state.

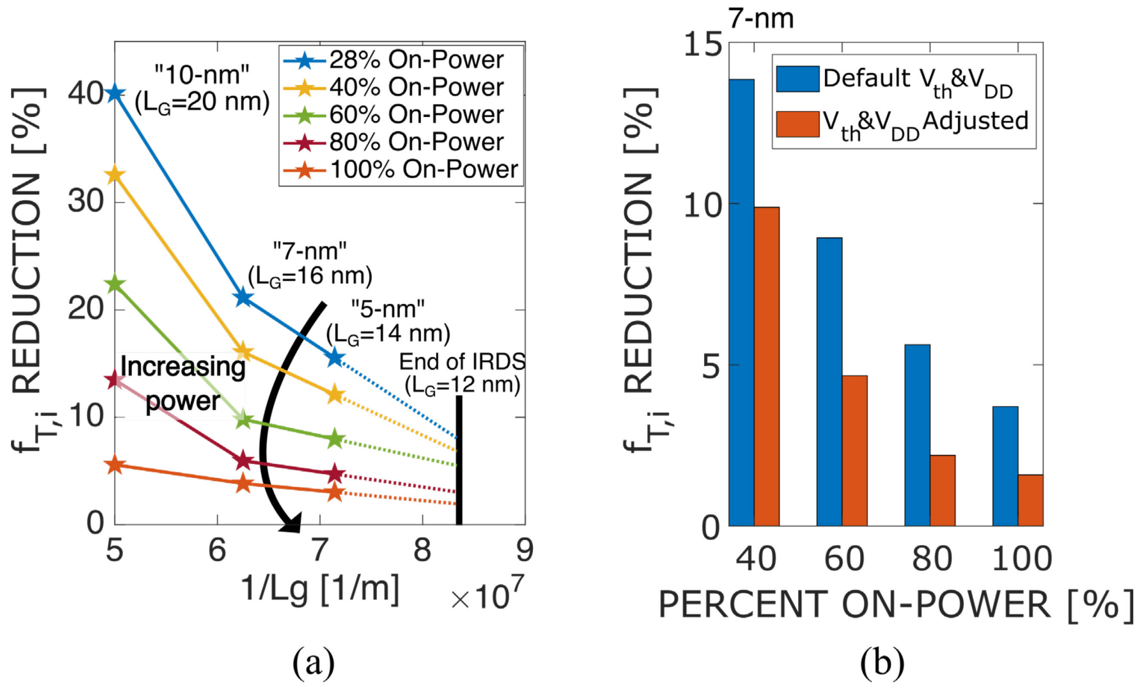


Fig. 1.15 (a) Degradation of $f_{\mathrm{T,i}}$ in the intrinsic NCFET vs. MOSFET as channel length scales down, extrapolated linearly to the end of the IRDS. The top left point at 40% corresponds to the arrow shown at $I_D = 0.5$ mA/μm in Fig. 1.13(a). (b) Comparison of $f_{\mathrm{T,i}}$ degradation between an NCFET with default V_{th} and V_{DD} and one with adjusted V_{th} and V_{DD}, shown at various levels of operating power.

Utilizing the strategies outlined above to maximize performance gain, the results for f_T and $g_m f_T / I_D$ of 7-nm devices can be seen in Fig. 1.16. As seen in Fig. 1.16(a), it is evident that the NCFETs exhibit a higher $f_{\mathrm{T,e}}$ over a larger range of operating powers compared to Fig. 1.13(a). A similar improvement can also be seen in $g_m f_T / I_D$, which is shown in Fig. 1.16(b),

where the improvement at the peak value of $g_m f_T / I_D$ has increased from 28% in Fig. 1.13(b) to 35% in Fig. 1.16(b).

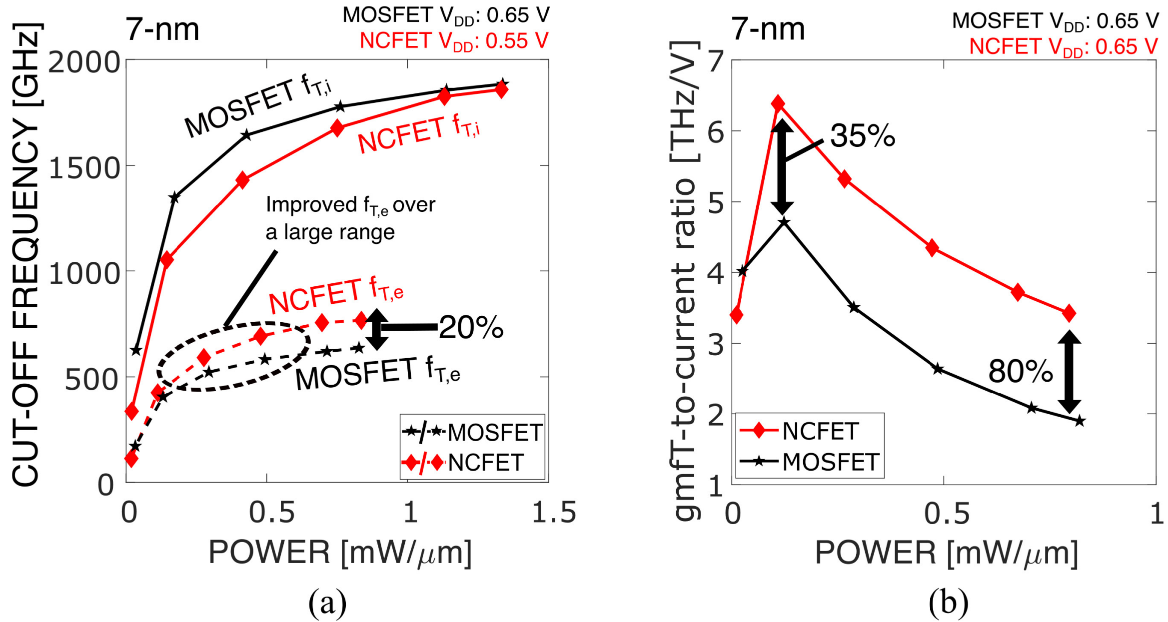


Fig. 1.16 (a) The $f_{\mathrm{T,e}}$ and $f_{\mathrm{T,i}}$ results for the 7-nm device with adjusted V_{th} and V_{DD}. An improvement in $f_{\mathrm{T,e}}$ over a larger range can be seen compared to Fig. 1.13(a). (b) The $g_m f_T / I_D$ results for the 7-nm devices.

In addition to the device characteristics presented so far with fixed nominal values of parasitic capacitances and resistances, the effects of varying parasitic elements is also investigated, and can be seen in Fig. 1.17. As seen from Fig. 1.17(a), an increase in the extrinsic parasitic *resistance* decreases the advantages NCFETs can provide for peak $f_{\mathrm{T,e}}$, emphasizing the importance of keeping these resistances as low as possible. As extrinsic parasitic *capacitance* increases, it is evident from Fig. 1.17(b) that the NCFET brings increasing advantages, showing that NCFETs will be more beneficial as scaling continues, where extrinsic parasitic capacitances are expected to increase [57].

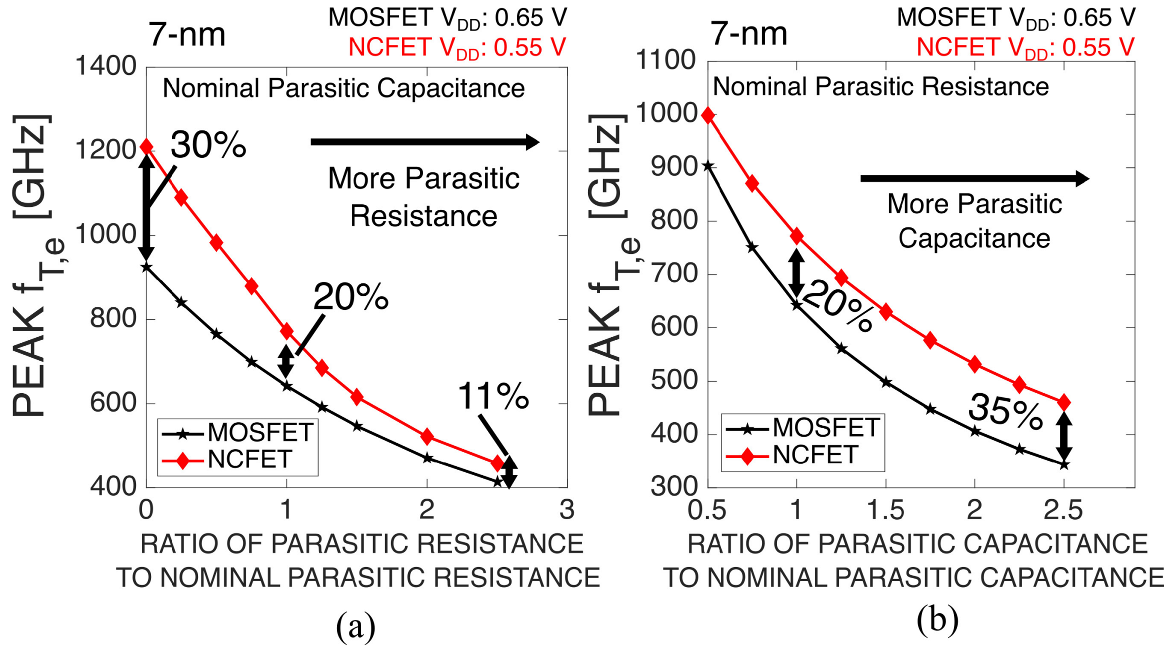


Fig. 1.17 (a) The effect of parasitic resistance on peak $f_{\mathrm{T,e}}$ for 7-nm MOSFET and NCFET devices. (b) The effect of parasitic capacitance on peak $f_{\mathrm{T,e}}$ for 7-nm MOSFET and NCFET devices.

Key Contributions:

The specific contributions from the second stage of this work, "Potential Enhancement of f_T and $g_m f_T/I_D$ via the Use of NCFETs to Mitigate the Impact of Extrinsic Parasitics," are as follows:

1. Extending from the general benchmarks of the first stage, the potential for NCFETs to improve $f_{\mathrm{T,e}}$ by mitigating the effects of extrinsic parasitic capacitances via a higher intrinsic gate capacitance C_{gg} have been investigated. An intuitive understanding of the idea has been provided in the discussions surrounding (1.12).

2. Using the basic idea surrounding (1.12) and numerical simulations, the $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ of the NCFET was found to be up to 20% higher for $f_{\mathrm{T,e}}$ and up to 80% higher for $g_m f_T/I_D$ as seen in Fig. 1.13. This increase in $f_{\mathrm{T,e}}$ is comparable to improvements seen between technology nodes.

3. The increases of $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ in NCFETs are accompanied by an undesirable decrease of $f_{\mathrm{T,i}}$, which is a result of the ferroelectric electrostatics near the drain effectively increasing the electrical channel length of NCFETs. Two ways of

alleviating the undesirable decrease of $f_{\mathrm{T,i}}$ were examined, one as an outcome of channel length scaling and the other from adjustments to V_{th} and V_{DD} of the NCFET, with the results shown in Fig. 1.15.

4. It was found that the performance gain of NCFETs is decreased as extrinsic parasitic resistance increases, as seen from Fig. 1.17 (a). This trend emphasizes the importance of keeping parasitic resistances as low as possible to maximize performance gain from NCFETs.

5. It was found that as parasitic capacitance increases, the performance gain in NCFETs is more pronounced. Hence, the benefits of using an NCFET is expected to increase as scaling continues, demonstrating the promises of NCFETs for uses in next-generation RF applications.

1.4.3 Toward a GHz-Frequency BEOL Ferroelectric Negative Capacitance Oscillator with a Wide Tuning Range

Summary:

Compared to the well-studied FEOL application of ferroelectric negative capacitance in NCFET configurations, a possible alternative approach is to use ferroelectrics as standalone negative capacitance elements in BEOL applications, which can decrease the overall difficulty of fabrication because it avoids the need to integrate a high-quality ferroelectric layer into an advanced transistor structure. Toward this end, it has been shown recently [43] that by placing a ferroelectric in parallel to a MOSFET gate, and stabilizing its negative capacitance using active feedback, the f_T of a transistor can be improved. Building upon this promising result, the third stage of this work will focus on understanding the operation and potential benefits of a tunable ferroelectric oscillator utilizing a BEOL ferroelectric, drawing from experience gained regarding ferroelectric negative capacitance from the study of NCFETs in the previous two stages.

In modern radio-frequency circuits, a tunable oscillator is essential to mixers, serializer/deserializers, and analog-to-digital converters. Traditionally, the tunable oscillator is realized by placing an inductor-capacitor (LC) resonator between the gates of cross-coupled

MOSFETs, as shown in Fig. 1.18. The oscillations would be generated by the resonator circuit, and the cross-coupled MOSFETs would generate an effective negative resistance to counteract loss within the resonator such that oscillations can be sustained. Typically, the capacitor portion of the resonator would be implemented using a capacitor bank, such that the frequency can be tuned by changing the capacitance, with less capacitance corresponding to a higher oscillation frequency.

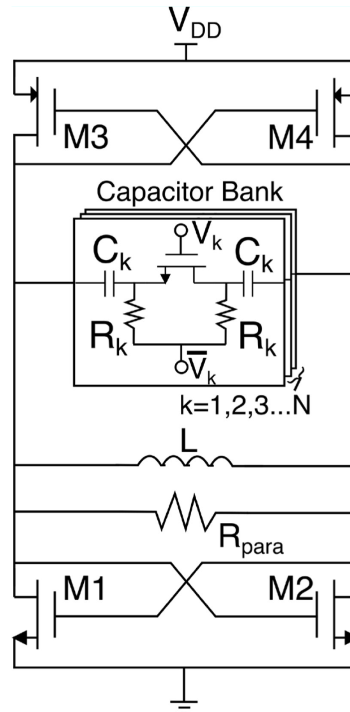


Fig. 1.18 Schematic diagram for a classical VCO with an inductor, R_{para} represents parasitic resistance from the inductor.

While this classical LC oscillator structure is widely used in modern IC processes, there are several important challenges for this architecture that need to be addressed. Typically, an on-chip, integrated inductor is required, which is much larger compared to other elements in the circuit. As an example, a photograph of a modern transceiver chip built using 28-nm technology is shown in Fig. 1.19 (directly taken from [60, Fig. 1.7]), where the size of the chip is approximately 8.41 mm^2. As seen from Fig. 1.19, the inductors are visible in the photograph, with each inductor coil having a diameter of approximately 150 μm or more and taking up approximately 15000 μm^2 or more. In comparison, transistors for this technology node have a gate length on the order of 30 nm [61], and are therefore not at all visible in the photograph.

As the result of this stage will show, each of these large inductors could potentially be replaced by a ferroelectric capacitor that has an area of less than 50 μm^2.

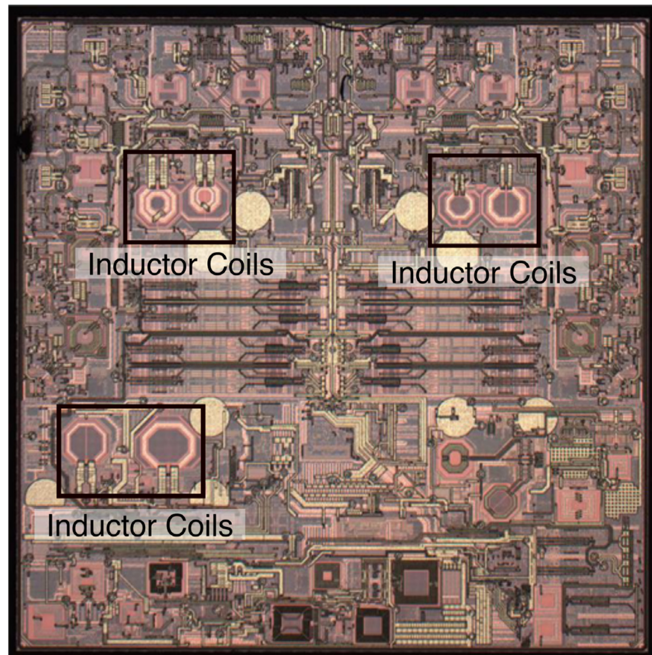


Fig. 1.19 Photograph of a RF transceiver built using the 28-nm technology. The photograph has sizes on the order of millimetres. The photograph is taken directly from [60, Fig. 1.7].

A second important challenge associated with traditional LC oscillators is that a large tuning range is usually required by modern applications. To increase the tuning range of LC oscillators, either multiple oscillators [62], or a multi-inductor designs [63], [64] can be utilized, both of which further increase the footprint required for the oscillator.

Motivated by the potential of using ferroelectrics as BEOL elements, and the importance of addressing the challenges associated with modern tunable oscillators, this stage aims to exploit single-domain ferroelectric dynamics for the construction of a tunable oscillator. The proposed digitally controlled ferroelectric oscillator (FE-DCO) is simulated using Cadence Virtuoso using the Global Foundries 65-nm process development kit (PDK) for all non-ferroelectric elements (with more details described in Chapter 4). In this novel oscillator design, the inductor in an LC oscillator is replaced with a ferroelectric capacitor, as shown in Fig. 1.20(a). Like an LC oscillator, the oscillation frequency is controlled by tuning the capacitances in a capacitor bank in parallel, with less capacitance corresponding to a higher frequency, as shown in Fig. 1.20(b).

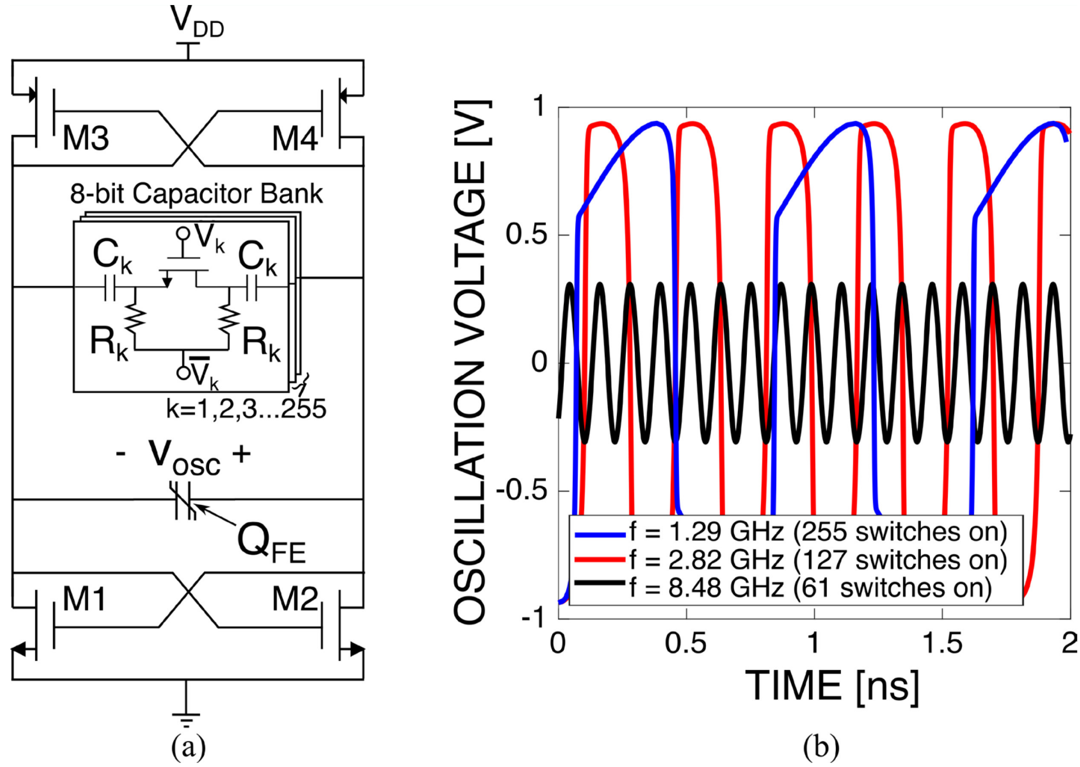


Fig. 1.20 (a) Schematic of the proposed FE-DCO. The ferroelectric capacitor is modeled as a non-linear charge storage device storing charge Q_{FE}. (b) Oscillation waveforms from the FE-DCO.

While the superficial characteristics of the FE-DCO are similar to the LC oscillator, the underlying oscillation mechanisms are very different in the FE-DCO, as it is not a resonator circuit. To systematically investigate the underlying operating principles of the FE-DCO, the circuit is first simplified to a basic oscillator circuit, where the negative resistance generated by the cross-coupled MOSFET pair is replaced by a negative linear resistor R_N, and the capacitor bank is replaced by a linear tuning capacitor C_{tune}, as shown in Fig. 1.21(a). If the values of R_N and C_{tune} are appropriately picked, the simplified circuit can exhibit the same oscillations as the full circuit, as shown in Fig. 1.21(b), thereby making the simplified circuit a good candidate to use for the analysis of the FE-DCO's principles of operation.

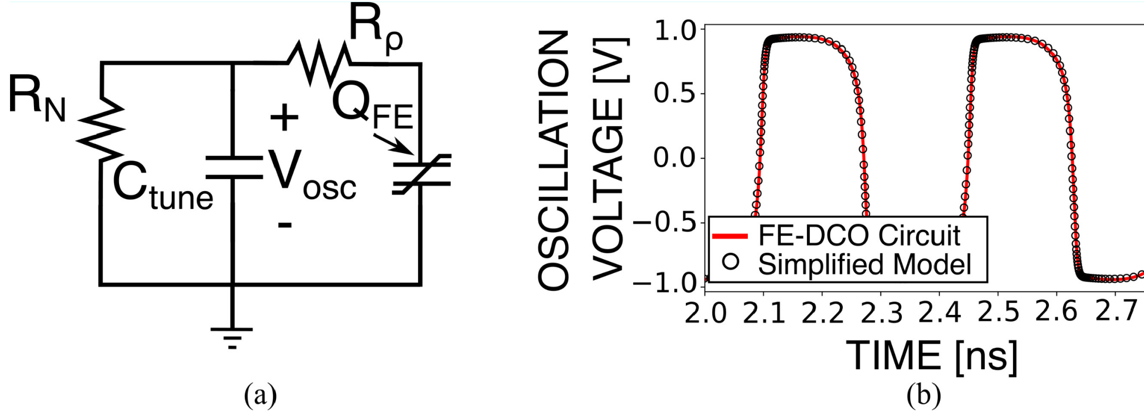


Fig. 1.21 (a) Simplified circuit of the FE-DCO. (b) Comparison of oscillation waveform between the simplified circuit and the full FE-DCO circuit at 2.82 GHz.

To analyze the simplified circuit, a coupled pair of non-linear differential equations can be formulated using elementary circuit analysis:

$$\frac{dQ_{\text{tune}}}{dt} = -\left(\frac{R_N + R_\rho}{R_N R_\rho C_{\text{tune}}}\right) Q_{\text{tune}} + \frac{2\alpha t_{\text{FE}}}{A_{\text{FE}} R_\rho} Q_{\text{FE}} + \frac{4\beta t_{\text{FE}}}{A_{\text{FE}}^3 R_\rho} Q_{\text{FE}}^3 \tag{1.13}$$

$$\frac{dQ_{\text{FE}}}{dt} = \frac{1}{R_\rho C_{\text{tune}}} Q_{\text{tune}} - \frac{2\alpha t_{\text{FE}}}{A_{\text{FE}} R_\rho} Q_{\text{FE}} - \frac{4\beta t_{\text{FE}}}{A_{\text{FE}}^3 R_\rho} Q_{\text{FE}}^3 \tag{1.14}$$

where Q_{tune} and Q_{FE} denotes the charge on the top plate of the tuning capacitor and ferroelectric capacitor; α and β are the Landau parameters of the ferroelectric as seen in (1.1); A_{FE} is the area of the ferroelectric capacitor; and all other symbols are labeled in the simplified circuit in Fig. 1.21.

To obtain useful results that would help designers in designing the FE-DCO, (1.13) and (1.14) are analyzed using techniques commonly utilized in the field of non-linear dynamics [65]. The full analysis process will be discussed in detail in Chapter 4, with only the important outcomes summarized in this section.

The first important outcome of the analysis is that a criterion for oscillation is developed. Due to the unique system dynamics of the FE-DCO, oscillations may not always be possible depending on various circuit parameters, and as such, a criterion that needs to be satisfied for oscillations to occur needs to be developed to aid designers in ensuring that the FE-DCO can function as expected. Through detailed analysis, we have found that a sufficient criterion for oscillation is

$$\frac{2}{5} < \left|\frac{(R_N + R_\rho)C_N}{R_N C_{\text{tune}}}\right| < 1 \tag{1.15}$$

where $C_N \equiv A_{\text{FE}} C'_{\text{FE,n}}$, with $C'_{\text{FE,n}}$ as defined in (1.4) and (1.8), is the linearized negative capacitance of the ferroelectric, and all other symbols are as previously defined in (1.13) and (1.14).

Beyond a criterion for oscillation, the analysis has also yielded insights into the control of amplitude and frequency of the oscillation generated by the FE-DCO. In terms of amplitude, it can be shown that the amplitude is directly proportional to the coercive field of the ferroelectric capacitor, which is the electric field at which the atoms in a ferroelectric transition between its polarization states, as discussed in Section 1.2.1, *i.e.*

$$V_{\max} = E_C t_{\text{FE}} \tag{1.16}$$

where $V_{\max}$ is the amplitude, E_c is the coercive field, and t_{FE} is the thickness of the ferroelectric layer in the capacitor.

In terms of frequency, it was found that the maximum frequency of the oscillator can be predicted via the circuit elements using the following expressions:

$$2\pi f_{\max} = \sqrt{\frac{1}{|(R_{N0} + R_\rho) R_\rho C_N^2|}} \tag{1.17}$$

$$\frac{1}{R_{\text{N0}}} = -\left(\frac{g_{\text{m,n}}}{2} + \frac{g_{\text{m,p}}}{2}\right) \tag{1.18}$$

where $f_{\max}$ is the maximum frequency, [3] $g_{\text{m,n}}$ and $g_{\text{m,p}}$ are respectively the transconductances of the NMOS and PMOS transistors at the dc bias point, and all other variables are as previously defined in Fig. 1.21 and in conjunction with (1.15). This expression can be used as another tool to design the ferroelectric oscillator to satisfy a given specification.

In addition to these key expressions, we have also found several other important design considerations for the FE-DCO in terms of its frequency and amplitude. First, we have found that as oscillation frequency increases, the oscillation amplitude decreases, which is shown in

[3] The symbol $f_{\max}$ is used here to represent the maximum frequency at which the FE-DCO can oscillate and is *unrelated* to the transistor figure of merit with the same name discussed in the summary to stage 1.

Fig. 1.20(b). We have found that this is a result of the system dynamics of the FE-DCO and can be rigorously supported in the derivation process of (1.16), which will be discussed in more detail in Chapter 4. Furthermore, we have found that non-linear characteristics of the negative resistance generated by the cross-coupled MOSFETs, which is ignored in the analysis of the simplified circuit presented in Fig. 1.21(a), will eventually act to limit the ultimate amplitude achievable by the FE-DCO, much like how non-linear effects of the FETs also limit the amplitude of the traditional LC oscillator.

To benchmark the FE-DCO and explore its applicability for modern RF circuits, the proposed design shown in Fig. 1.20(a) is compared against a carefully designed equivalent LC-DCO using important oscillator metrics of phase noise and tuning range. The results of these comparisons can be found in Fig. 1.22 below. Compared to the LC-DCO, the FE-DCO exhibits a much higher tuning range of 149% (1.29 GHz – 8.75 GHz) compared to the 50% achieved by the LC-DCO (2.29 GHz – 3.81 GHz), as shown in Fig. 1.22(a), at the cost of a worse phase noise performance, which is around 20–25 dB worse, as shown in Fig. 1.22(b). When the tuning range and phase noise of the two oscillators are simultaneously compared using the standard figure of merit FOM_2 [66, Ch. 8], the two oscillators were found to be within 6 dB of each other, as shown in Fig. 1.22(c), which shows that the FE-DCO has similar overall performance as the traditional LC-DCO. Considering that the ferroelectric capacitor in this design only has an area of 35 $\mu\mathrm{m}^2$, whereas the inductor of the equivalent LC-DCO has an area of approximately 49087 $\mu\mathrm{m}^2$, this similar overall performance indicates that the proposed FE-DCO design could be an attractive alternative to the traditional LC-DCO design as its footprint would be vastly smaller.

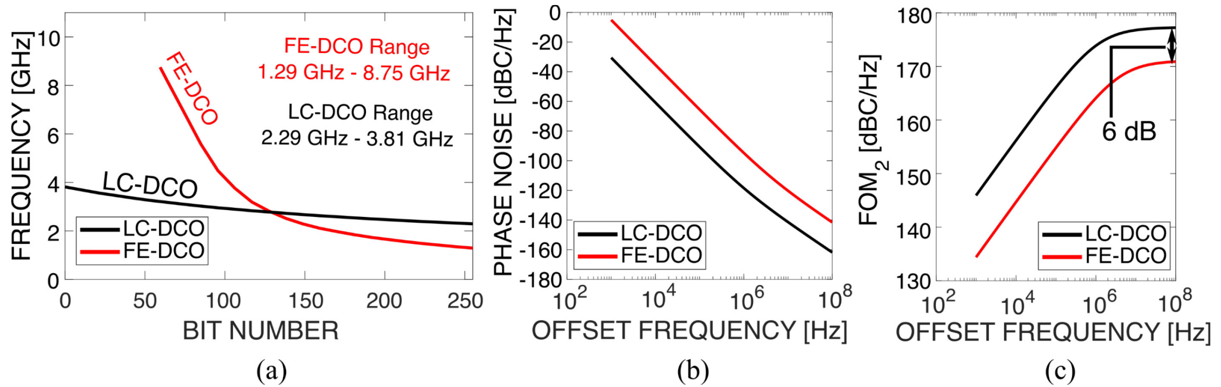


Fig. 1.22 (a) Tuning range comparison between the proposed FE-DCO and the traditional LC-DCO. (b) Phase noise comparison between the FE-DCO and the LC-DCO. (c) Comparison of FOM_2 between the FE-DCO and the LC-DCO.

Key Contributions:

The specific contributions from the third stage of this work, "Toward a GHz-Frequency BEOL Ferroelectric Negative Capacitance Oscillator with a Wide Tuning Range," are as follows:

1. Utilizing expertise gained with respect to negative capacitance devices developed in the previous two stages, the potential for single-domain ferroelectric dynamics to be exploited for use in a tuned oscillator is explored. It was found that tuned oscillation can be achieved using the circuit shown in Fig. 1.20(a).

2. The operating principles of the proposed ferroelectric oscillator were analyzed using techniques applicable in non-linear dynamics, and it was found that a criterion must be satisfied for oscillation to occur. This sufficient criterion for oscillation is shown in (1.15).

3. The amplitude of oscillation was found to be proportional to the coercive field of the ferroelectric, as shown in (1.16), and the maximum oscillation frequency of the oscillator can be predicted using (1.17). Both results can be used by designers in designing the proposed ferroelectric oscillator to meet required performance metrics.

4. The performance of the oscillator was compared to an equivalent traditional LC oscillator. It was found that the tuning range can be vastly higher at the cost of

worse phase noise. If both tuning range and phase noise are considered, the overall performances of the two oscillators are shown to be similar, meaning that the proposed ferroelectric oscillator can be an attractive alternative to the traditional LC oscillator as it has a much smaller footprint from its inductor-less design.

Chapter 2

RF Performance Projections of Negative-Capacitance FETs: f_T, $f_{\max}$, and $g_m f_T / I_D$

2.1 Introduction

Ferroelectric negative-capacitance field-effect transistors (NCFETs) have been proposed as candidates for future low-power nanoelectronics since 2008 [4], based on their potential of continuing supply-voltage scaling via amplification of the applied gate voltage. Recently [31], the integration of NCFETs into an advanced industrial node, and the demonstration of performance improvements of ring oscillators employing them over conventional FinFETs, points to the continuing promise of NCFET technology for digital circuit applications.

While demonstrations and investigations of the dc and digital behavior of NCFETs are abundant in the literature, the radio-frequency (RF) potential of NCFETs has not yet been thoroughly investigated. Investigation into this direction is important for future RF applications of NCFET technology.

Thus far, numerous studies [13], [26], [27], [30], [31], [33], [46]–[49], [52], [59], [67]–[76],have made observations on a number of individual small-signal quantities for NCFETs that could impact their overall RF performance. Specifically, increases in the input capacitance C_{gg} [27], [30], [31], [48], [67]–[71], transconductance g_m [27], [30], [33], [47]–[49], [72]–[75], and output resistance r_o [13], [26], [30], [33], [52], [59], [71], [72], [76], have been observed. Furthermore, numerous studies [13], [30], [33], [46], [47], [69], [71], [76], have noted the possibility of negative differential resistance (NDR) in NCFET output characteristics. Temperature-dependent effects of these parameters have also been examined in the context of self-heating [46] and temperature-dependent parasitic capacitances [47]. A possibility of improved RF performance by controlling NDR through asymmetrical parasitic capacitances has also been proposed [33].

Beyond individual small-signal parameters, a few papers have also examined the overall RF potential of NCFETs through simulations [46]–[49], [76]–[79], and experiments [72]. For device-level figures of merit, similar or superior values of the unity-current-gain cut-off frequency f_T have been observed [46]–[49], [72], and in terms of the maximum oscillation frequency $f_{\max}$, there has been a single report of a decrease in $f_{\max}$ when the ferroelectric is integrated into the NCFET [46]. For circuit-level figures of merit, investigations have shown that NCFETs can perform better for comparators [76], [79], sample-and-hold circuits [77], analog switches [49], [78], differential amplifiers [49], voltage-to-time converters [79], and current mirrors [49], [76], [78].

Although these advancements show great promise for NCFETs in RF applications, most of the studies thus far have considered a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [46]–[49], [76]. While the MFMIS structure simplifies modeling due to the uniform potential at the ferroelectric-insulator surface, dc leakage currents would make the ferroelectric negative capacitance unstable [16]. This instability makes biasing of MFMIS devices and circuits difficult, and hence makes the MFMIS structure undesirable for RF applications. Furthermore, due to multidomain effects, an additional restriction on the length of the ferroelectric to avoid hysteresis in an MFMIS structure has been reported in the literature, further limiting the usefulness of this structure [15].

By contrast, a metal-ferroelectric-insulator-semiconductor (MFIS) structure mitigates these problems [15], [16] and yields different overall device characteristics arising from a spatially varying ferroelectric potential vs. those in MFMIS structures [52], [74], [80], [81]. The MFIS structure has also been the choice thus far for integration into advanced nodes [31].

A few studies have also examined the RF performance of MFIS NCFETs [46], [72], [78], [79]. A small improvement in f_T was reported through experiments in [72], and [77]–[79] reported on circuit-level figures of merit through simulations, with [77], and [79] employing a single-domain ferroelectric model that does not capture spatial variation of potential in the ferroelectric. These promising results further strengthen the need for a more detailed investigation into the device-level RF performance metrics of MFIS NCFETs.

Motivated by the deficiencies of the MFMIS structure and the promising results of [72], [77], [78], and [79], this study takes the next step in unveiling the full RF potential of NCFETs by considering an MFIS NCFET structure simulated using a physics-based model that includes a spatially varying potential in the ferroelectric, and with the baseline model calibrated to the experimental results in [82], in conjunction with small-signal circuits. The focus will be on three important RF device figures of merit: the conventional metrics f_T and $f_{\max}$, including one important implication of the ferroelectric damping constant ρ on $f_{\max}$, and the metric $g_m f_T / I_D$, an important metric that captures RF performance in the context of required dc power consumption [50], [51], [83], where I_D is the dc drain current. The results of this work will be useful for the development and optimization of NCFET technology for future RF applications.

This chapter is organized into four sections. Section 2.2 will summarize the methodologies used for the construction and calibration of our overall modeling approach, including choices of NCFET devices, physical modeling of the MOSFET and NCFET devices, and various intrinsic and extrinsic small-signal models used to obtain the relevant RF figures of merit. Section 2.3 will summarize the results with regard to dc performance, small-signal parameters, intrinsic and extrinsic f_T, $f_{\max}$, and $g_m f_T / I_D$. Section 2.4 will summarize the main conclusions.

2.2 Methodologies

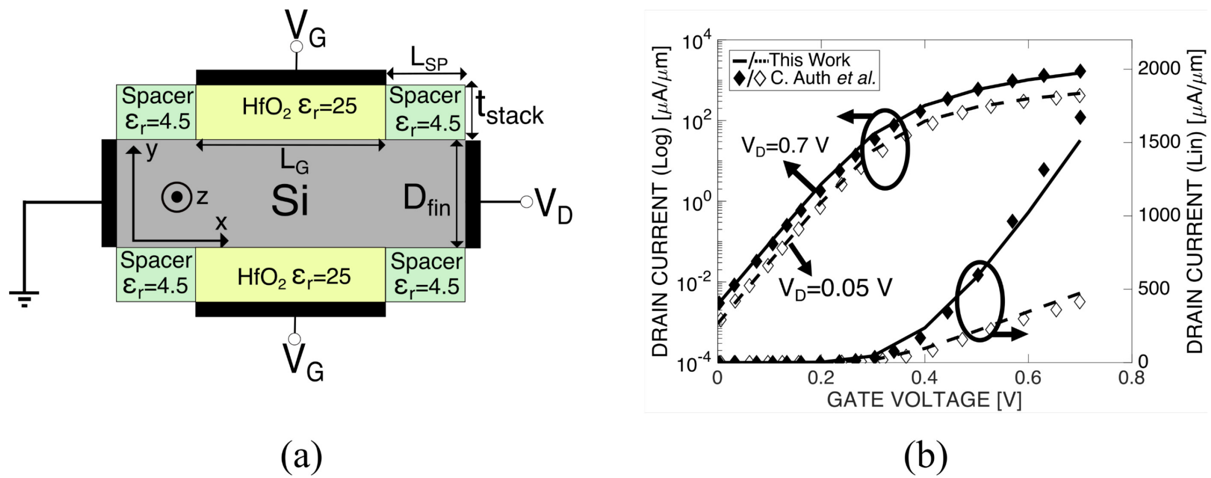
2.2.1 Overview of Approach

The dc model of the baseline MOSFET and NCFETs are numerically simulated using COMSOL Multiphysics [84], which is then used to obtain a quasi-static intrinsic small-signal model for the devices, with the component values found from perturbed dc solutions in the usual way [54, pp. 359–438]. For the NCFET, this intrinsic small-signal model includes the impact of small-signal perturbation of the ferroelectric about a stable operating point at the center of its lossless S-shaped curve [4]; this small-signal lossless operation is augmented by a series damping resistor (described in Section 2.2.5-B) to account for the loss in the ferroelectric. Extrinsic parasitic elements will then be added to the intrinsic small-signal model

to form extrinsic MOSFET and NCFET circuits that will be simulated to assess the RF performance of each type of device.

2.2.2 Baseline FET Design and Modeling

The baseline FET in this study is an n-type FinFET with dimensions set to the 10-nm node [82], [85] with a dielectric constant of 25 for HfO_2 [86]. The overall device structure can be seen in Fig. 2.1(a), with important parameters listed in Table 2.1. Device simulations are conducted in 2-D using COMSOL Multiphysics with the drift-diffusion formalism [52], [80], assuming a geometrical invariance in the fin height direction.



(a) (b)

Fig. 2.1 (a) Schematic diagram of the baseline MOSFET device, where the fin height extends into the z-direction. (b) Calibration of baseline MOSFET device with the experimental results of [82].

Symbol	Parameter	Value
L_G	Gate Length	20 nm
D_{fin}	Fin Width	7 nm
H_{fin}	Fin Height	46 nm
L_{SP}	Spacer Length	8 nm
t_{stack}	Oxide Stack Thickness	4.3 nm
ϕ_m	Metal Work Function	4.416 eV
$N_{\text{S/D}}$	Source and Drain Doping Concentration	10^{20} cm^{-3}
N_{ch}	Channel Doping Concentration	5 x 10^{17} cm^{-3}
μ_{eff}	Low-Field Effective Mobility	320 cm^2/Vs
β	Velocity Saturation Exponent	2 (electron) / 1 (hole)

v_{sat}	Saturation Velocity	2.1 x 10^7 cm/s
L_G	Gate Length	20 nm

Table 2.1 Device and transport parameters.

To account for quantum confinement in the fin width direction, the modified local-density approximation [52], [53] has been used. This formalism corrects for both geometrical and energetic confinement effects by assuming an infinite barrier at the silicon-oxide interface and has been shown to have good agreement with Schrödinger-Poisson solvers for FinFET devices [52], [53]. Effective mass values have been taken from [52], with the z-direction assumed to be [1 0 0].

The baseline device has been calibrated to an experimental device in [82] through the adjustment of mobility parameters, as shown in Fig. 2.1(b). Transport parameters are also listed in Table 2.1, and these same parameters are used throughout this study.

2.2.3 Comparison Methodology

Thus far, studies have shown different ways of comparing performance between a baseline MOSFET and an NCFET device. These differences are important to note, as they can lead to different impressions of performance superiority or inferiority for the NCFET technology.

In certain studies, *e.g.*[46], [47], [49], [76], [77], the underlying MOSFET is not modified and the ferroelectric layer is directly introduced on top of the stack to produce an NCFET, which changes the total oxide stack thickness t_{stack} of the device. This method results in an NCFET whose dielectric capacitance $C_{\mathrm{ox,DE}}^{\mathrm{NC}}$, which is the capacitance of the stack with the ferroelectric removed, is the same as the oxide capacitance $C_{\mathrm{ox}}^{\mathrm{MOS}}$ of the baseline MOSFET.

In other studies, *e.g.*,[27], [70], [72], [87], the NCFET is constructed by replacing a portion of the MOSFET oxide stack with a ferroelectric, while keeping t_{stack} the same. This results in an NCFET device where $C_{\mathrm{ox,DE}}^{\mathrm{NC}}$ may be different from $C_{\mathrm{ox}}^{\mathrm{MOS}}$.

In this study, t_{stack} is kept the same between the baseline and the NCFET. In practice, due to the limited space between fins in advanced nodes, it may be difficult to deposit a thick layer of ferroelectric on top of the existing FET structure [31]. Therefore, our method helps to assess the RF performance of NCFETs in a technologically relevant way. Hence, in this work, to

obtain an NCFET, the HfO_2 of the structure in Fig. 2.1(a) is replaced by a ferroelectric-dielectric heterostructure having a ferroelectric thickness of t_{FE} and a dielectric thickness of t_{DE} that sums to a total thickness of t_{stack}. We also note that the exact value of t_{stack}, impacted (for example) by the exact value for the dielectric constant of HfO_2 in the baseline device [86], would not affect the qualitative conclusions of this work.

Since various process-compatible ferroelectric materials [9] and thicknesses exist, and no gate-stack optimization approach has yet been proposed for the RF performance of MFIS NCFETs, a logical method to obtain meaningful initial calibration points that can serve as the basis for future optimization is to consider NCFETs with varying degrees of static performance improvements. The expected static performance improvement can be evaluated through the total oxide capacitance of the NCFET stack $C_{ox,tot}^{NC}$, with this total specified by the series combination of the ferroelectric negative capacitance $C_{ox,FE}^{NC}$ and the dielectric capacitance $C_{ox,DE}^{NC}$. By selecting ferroelectric and dielectric materials, thicknesses, or both, an increase in the total $C_{ox,tot}^{NC}$ could be realized, *e.g.*, via an increase in $C_{ox,DE}^{NC}$ compared to the baseline, or better capacitance matching such that $C_{ox,FE}^{NC}$ and $C_{ox,DE}^{NC}$ are closer in magnitude. As $C_{ox,tot}^{NC}$ increases, static performance improvement in the NCFET is intuitively expected based on classical velocity-saturated MOSFET theory [54, pp. 248–309].

We will consider NCFETs with silicon-doped HfO_2 [31] as the ferroelectric, and SiO_2 [27], [70], [87] as the dielectric, both of which have been shown to be compatible for the fabrication of modern MFIS NCFETs. Three example NCFETs, created by varying t_{DE} to achieve successively increasing $C_{ox,tot}^{NC}$, and hence successively improved static performance, will be used to benchmark the RF performance of NCFETs. These are devices B1 – B3 in Table 2.2, where for B1, $C_{ox,tot}^{NC}$ is smaller than C_{ox}^{MOS}; for B2, $C_{ox,tot}^{NC}$ is similar to C_{ox}^{MOS}; and for B3, $C_{ox,tot}^{NC}$ is greater than C_{ox}^{MOS}.

Device	**Physical Dielectric Thickness (t_{DE})**	**Physical Ferroelectric Thickness (t_{FE})**	**Total Oxide Capacitance per Area**
A (Baseline)	4.30 nm ($\epsilon_r = 25$)	0 nm	$0.0515\ F/m^2$
B1 (NCFET)	1.00 nm ($\epsilon_r = 3.9$)	3.30 nm	$0.0376\ F/m^2$

B2 (NCFET)	0.67 nm ($\epsilon_r = 3.9$)	3.63 nm	0.0595 $\mathrm{F/m^2}$
B3 (NCFET)	0.39 nm ($\epsilon_r = 3.9$)	3.91 nm	0.1179 $\mathrm{F/m^2}$

Table 2.2 NCFET device parameters.

2.2.4 NCFET Model and Solution Approach

2.2.4-A. Ferroelectric Electrostatics

The static ferroelectric is modeled using the multidomain Landau-Khalatnikov (LK) equation [11]–[13], [73] for the y-direction polarization, with the time derivative component set to zero

$$E_y(x,y) = 2\alpha P_y(x,y) + 4\beta P_y^3(x,y) + 6\gamma P_y^5(x,y) - k\nabla^2 P_y(x,y) \tag{2.1}$$

where $\alpha = -3.60 \times 10^8\ \mathrm{m \cdot F^{-1}}$, $\beta = 2.25 \times 10^{10}\ \mathrm{m^5 \cdot F^{-1} \cdot C^{-2}}$, and $\gamma = 1.67 \times 10^9\ \mathrm{m^9 \cdot F^{-1} \cdot C^{-4}}$ are the LK parameters calibrated to silicon-doped HfO_2 [9], [11], $k = 1 \times 10^{-8}\ \mathrm{m^3 \cdot F^{-1}}$ is the multidomain interaction parameter [59], P_y is the y-direction polarization, and E_y is the y-direction electric field. The x-direction polarization for the ferroelectric is modeled as an ordinary dielectric [13]

$$E_x(x,y) = \frac{1}{(\epsilon_r - 1)\epsilon_0} P_x(x,y) \tag{2.2}$$

where $\epsilon_r = 25$ is the dielectric constant for the x-direction, equal to that for a dielectric HfO_2 [86], ϵ_0 is the permittivity of free space, P_x is the x-direction polarization, and E_x is the x-direction electric field. In this formulation, variations of polarization and potential in the ferroelectric are allowed in both the x- and y- directions. Using (2.1) and (2.2), the ferroelectric electrostatics are self-consistently coupled into the overall FET simulation in the usual way through Poisson's equation.

2.2.4-B. Devices

The different combinations of t_{DE} and t_{FE} used to realize B1 – B3 are listed in Table 2.2. Here, we note that the thickness per cycle of deposition of SiO_2 can be around 0.1 nm [88] and silicon-doped HfO_2 can stay ferroelectric down to 3 nm [31]. Hence, the devices chosen here are all representative of possible devices given this material composition. The thicknesses t_{FE} and t_{DE} satisfy the capacitance matching condition for non-hysteretic operation [4]. Moreover,

a higher t_{FE} and lower t_{DE} lowers the magnitude of the ferroelectric negative capacitance $C_{\text{ox,FE}}^{\text{NC}} = 1/(2\alpha t_{\text{FE}})$ [4] and increases the magnitude of the dielectric capacitance $C_{\text{ox,DE}}^{\text{NC}} = \epsilon_r \epsilon_0 / t_{\text{DE}}$. This results in progressively better capacitance matching in devices B1, B2, and B3, which combined with the progressive increase of $C_{\text{ox,DE}}^{\text{NC}}$, causes these devices to have progressively larger total oxide capacitances, as seen in Table 2.2.

2.2.5 Intrinsic Small Signal Models

2.2.5-A. Baseline Intrinsic Model

For the baseline MOSFET, the classical small-signal model is used [54, pp. 359–438], as seen in Fig. 2.2(a). The small-signal quantities in this model are extracted using dc solutions corresponding to small voltage perturbations on the terminals and the following formulas: $C_{\text{gg}} = \Delta Q_G / \Delta V_G$, $C_{\text{gd}} = \Delta Q_G / \Delta V_D$, $C_{\text{gs}} = C_{\text{gg}} - C_{\text{gd}}$, $g_m = \Delta I_D / \Delta V_G$, and $r_o = \Delta V_D / \Delta I_D$, where Q_G is the charge on the gate terminals, I_D is the dc drain current, and the other symbols are identified in Figs. 2.1(a) and 2.2(a).

For the NCFET, the same method used for the MOSFET is used to extract intrinsic capacitive components. However, to account for the effects of ferroelectric damping under dynamic operation, a resistor $R_{\rho,\text{eff}}$ has been added in series with the gate, as seen in Fig. 2.2(b).

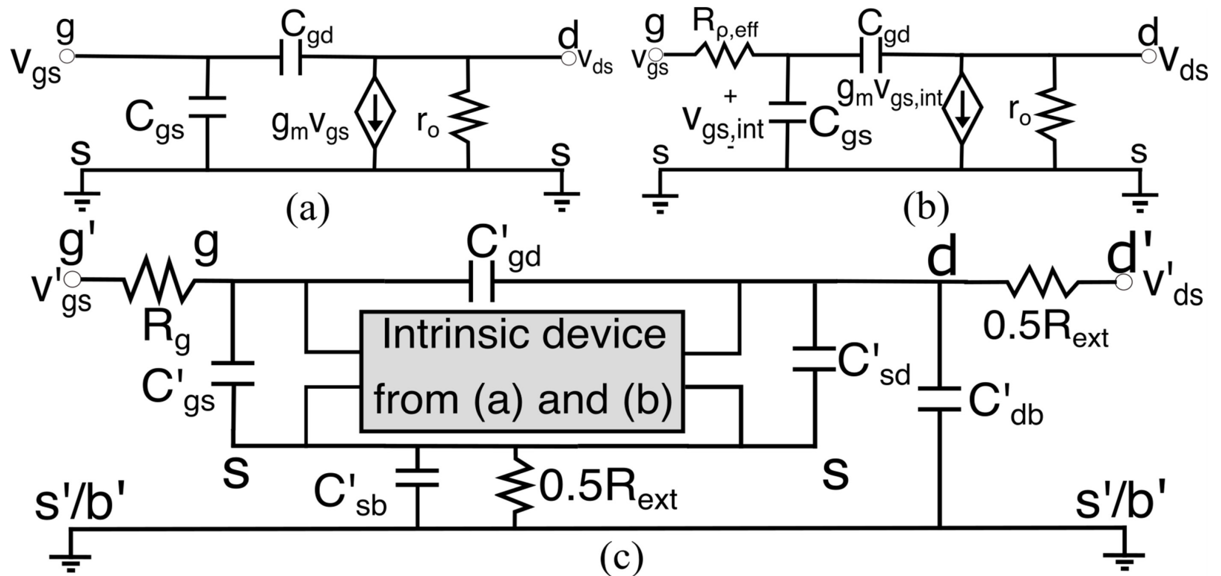


Fig. 2.2 Small-signal circuits for: (a) intrinsic MOSFET; (b) intrinsic NCFET; (c) extrinsic circuit for both MOSFET and NCFET, where the damping resistor $R_{\rho,\text{eff}}$ is inside the intrinsic box.

2.2.5-B. Damping Resistor for NCFET

The damping resistor for a lumped ferroelectric can be modeled by $R_\rho = \rho t_{\mathrm{FE}}/A_{\mathrm{FE}}$ [11], where A_{FE} is the area of the ferroelectric. For an MFMIS structure, since the transistor can be considered as a separate circuit element from the ferroelectric with a common node between them, the use of $R_{\rho,\mathrm{eff}} \equiv R_\rho$ is an appropriate representation. However, since damping is distributed throughout the ferroelectric, strictly speaking, the lumped value may not be applicable for an MFIS NCFET. To account for the distributed effect, the correct value of an effective damping resistor $R_{\rho,\mathrm{eff}} \neq R_\rho$ should be investigated for the MFIS small-signal model.

To make a first-order estimate for the value of $R_{\rho,\mathrm{eff}}$, an equivalent circuit approach is used. As seen in Fig. 2.3(a), when a small perturbative voltage is applied at the gate of the MFIS NCFET, a charge response $\Delta Q(x, y)$ occurs throughout the intrinsic structure, leading to a non-uniform distribution of the total input capacitance, $C_{\mathrm{gg}}(x, y) = H_{\mathrm{fin}} \times \Delta Q(x, y)/\Delta V_G$. This input capacitance includes capacitive effects from both the ferroelectric layer, the dielectric layer, and fringing fields through the ferroelectric and spacers.

From the distributed capacitance $C_{\mathrm{gg}}(x, y)$, a few further assumptions can be made to obtain the first-order input circuit model seen in Fig. 2.3(b). First, the relatively small vacuum capacitance of the ferroelectric can be ignored, which allows each damping resistor R_n to be directly attached to each input capacitance C_n. Second, variation of the charge in the y-direction is neglected, which allows us to collapse $C_{\mathrm{gg}}(x, y)$ into $C_{\mathrm{gg}}(x) = \int C_{\mathrm{gg}}(x, y)\, dy$. Finally, ferroelectric damping is assumed to be uniformly distributed in the x-direction, and hence among all capacitors, making $R_n = \rho t_{\mathrm{FE}}/2H_{\mathrm{fin}}dx$.

By evaluating the input resistance as the real part of the input impedance of Fig. 2.3(b), we have found that the value of $R_{\rho,\mathrm{eff}}$ is constant in the frequency range used to extract f_T and $f_{\max}$. The exact value depends on the device and bias point, and is between 22 and 32% *above* R_ρ for every bias point in all devices. Further, we have also confirmed that a lack of distribution in capacitance leads to $R_{\rho,\mathrm{eff}} = R_\rho$, as expected.

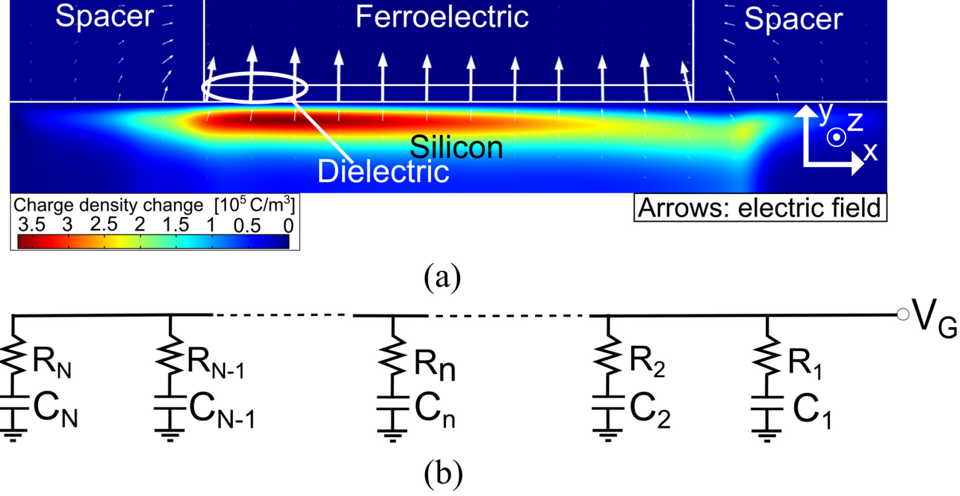


Fig. 2.3 (a) Change of charge as a function of position for device B2 (as specified in Table 2.2) at $V_G = V_D =$ 0.7 V and with $\Delta V_G = 0.02$ V, where the white arrows represent the electric field associated with these charges. Only the top half of the device is shown since the bottom half has symmetrical characteristics. The field lines in the ferroelectric region are too small to be visible. (b) Equivalent circuit used to evaluate $R_{\rho,\mathrm{eff}}$.

While further refinements to the model can be made to capture effects such as horizontal field lines, as seen near the vertical edges of the ferroelectric region in Fig. 2.3(a), or the possibility of fringing fields that completely bypass the ferroelectric, these are neglected as second-order effects.

Therefore, to first order, we will use the equivalent circuit model presented in Fig. 2.3(b) and the corresponding device-dependent, bias-dependent $R_{\rho,\mathrm{eff}} \sim 1.22$ to $1.32 \times R_\rho$ derived from the input resistance to benchmark the RF performance of NCFETs. However, to further preserve generality and account for any remaining uncertainty in the exact value to use for $R_{\rho,\mathrm{eff}}$, we note that a change in $R_{\rho,\mathrm{eff}}$ is analogous to a change in the damping constant ρ, and we have hence modulated ρ in this study. For initial benchmarks, a relatively low ρ of 1.80 $\mathrm{m\Omega \cdot m}$ that does not affect digital operation has been chosen [55].

2.2.6 Modeling of Extrinsic Components

To account for parasitic resistances and capacitances not captured in the intrinsic model, an extrinsic circuit model is constructed using the classical method [54, Ch. 8], with the extrinsic source and body terminal shorted, as seen in Fig. 2.2(c). Here, we assume that the integration of the ferroelectric does not change extrinsic parasitic elements, which are bias-independent and depend only on the geometry of the extrinsic structure.

To obtain appropriate values for the elements, a 3-D single-fin extrinsic structure up to the access vias for each terminal has been used, similar in geometry to the test structure used in [72]. This structure can be seen in Fig. 2.4, with critical dimensions given in Table 2.3 and Table 2.1. For reference, the diagram in Fig. 2.1(a) is a 2-D representation of the intrinsic device region with translational invariance in the z-direction, contained within the dash-boxed region in Fig. 2.4(b). This intrinsic region has been hollowed for the extraction of extrinsic parasitic capacitances to avoid double counting of intrinsic capacitances.

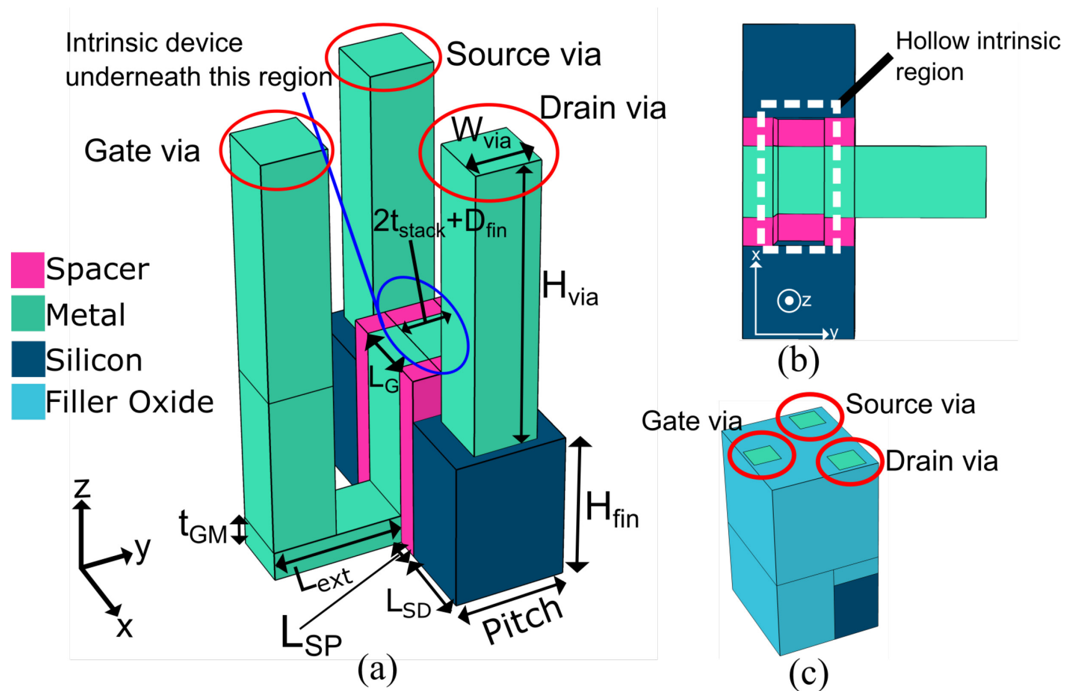


Fig. 2.4 (a) Extrinsic structure 3-D diagram. (b) Bottom view of extrinsic structure (c) The extrinsic structure after oxide fill.

Parameter	**Value**	**Parameter**	**Value**
Pitch	34.0 nm	C'_{gd}	7.70 aF
H_{via}	88.0 nm	C'_{gs}	7.70 aF
W_{via}	19.5 nm	C'_{sd}	1.32 aF
L_{SD}	26.0 nm	C'_{sb}	1.87 aF
L_{ext}	40.0 nm	C'_{db}	1.45 aF ($V_D = 0.7$ V)
t_{GM}	9.2 nm	R_{ext}	880.86 Ω
		R_g	836.43 Ω

Table 2.3 Extrinsic structure parameters.

Extrinsic contact-to-contact capacitances C'_{gd}, C'_{gs},and C'_{sd} are obtained by applying small voltage perturbations at the terminals and examining changes of terminal charge. The source- and drain-to-wafer junction capacitances C'_{sb} and C'_{db} are obtained using classical formulas for depletion capacitance of p-n junctions [89]. Values for all these capacitances can be found in Table 2.3.

Extrinsic resistances are obtained through the physical geometry in Fig. 2.4(a). For source and drain resistances, the resistance value is calculated by separating the resistance into three portions – via resistance, contact resistance, and epitaxial silicon resistance. The via is assumed to be tungsten, and the values of resistivity for the via and the contact used are $3 \times 10^{-5}\ \Omega \cdot \mathrm{cm}$ [90] and $1 \times 10^{-9}\ \Omega \cdot \mathrm{cm}^2$ [91], respectively. The epitaxial silicon resistance on each side is 10% of the total channel resistance, a reasonable choice considering the proportions shown in [91]. For the value of gate resistance R_g, the metal layer is also assumed to be made of tungsten [92], with a thickness-dependent resistivity from [90], and the distributed effects from a single gate contact have been taken into account in the calculation [54, pp. 440–508]. Values for the extrinsic resistances used can also be found in Table 2.3.

While the neglect of further layers of high-density interconnects beyond the terminal contacts and their associated parasitic capacitances in the extrinsic structure may cause an overestimation of f_T and $f_{\max}$ values, general trends concluded in this study will not be affected by this approximation.

2.3 Results

2.3.1 Static Results

As shown from Fig. 2.5(a), all NCFET devices B1 – B3 have a lower off-current I_{off} and subthreshold slope (SS) compared to the baseline. In terms of on-current I_{on}, devices B1 – B3 respectively exhibit lower, similar, and higher I_{on} compared to the baseline. We also note that the non-hysteretic operation of the NCFET devices have been confirmed by dual-direction dc sweeps of V_G. These results are expected and in line with literature, but will be briefly discussed for completeness.

The lower I_{off} in NCFETs is consistent with results in the literature [13], [38], [59], [80]. In addition to the enhancement of the total oxide capacitance that already suppresses I_{off}, drain coupling in NCFETs at low gate voltage leads to a suppression of channel potential and a raise in barrier energy that gets stronger as capacitance matching becomes better, which further suppresses the I_{off} [13], [59], [80]. Due to this additional effect, device B1 exhibits a lower I_{off} compared to the baseline despite having a lower total oxide capacitance compared to the baseline. In addition, since devices B1 – B3 have progressively better capacitance matching, this trend of progressively lower I_{off} is expected and also agrees with literature [59].

The results for I_{on} compared to the baseline can be intuitively interpreted through classical velocity-saturated MOSFET theory, where current in the inversion regime is proportional to the total oxide capacitance of the device [54, pp. 248–309]. Since devices B1, B2, and B3 respectively have lower, similar, and higher total oxide capacitance, as listed in Table 2.2, the same trend is exhibited in the I_{on} of these devices.

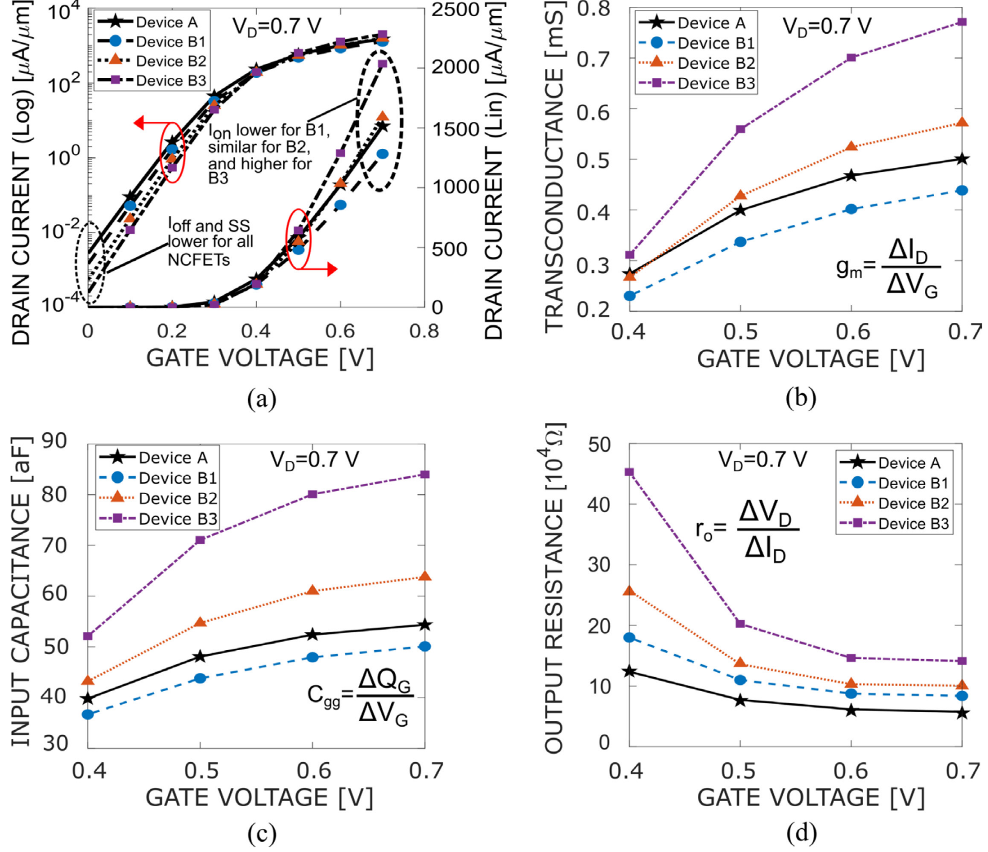


Fig. 2.5 Static and small-signal characteristics at various V_G with $V_D = 0.7$ V: (a) dc characteristics; (b) transconductance; (c) input capacitance; (d) output resistance.

2.3.2 Results for Small-Signal Parameters

Small-signal parameters for the devices are obtained using the method prescribed in Section 2.2.5-A. The small-signal results for g_m, C_{gg}, and r_o can be seen in Figs. 2.5(b) – (d), for $V_D = 0.7$ V [48]. These results are in line with observations made in the previous literature [13], [26], [27], [30], [31], [33], [46]–[49], [52], [59], [67]–[76], mentioned in Section 2.1.

As seen from Fig. 2.5(b) and Fig. 2.5(c), compared to the baseline, the transconductance g_m and the input capacitance C_{gg}, the latter a combination of the ferroelectric capacitance, dielectric capacitance, and any fringing capacitances through the spacers, are lower for device B1, and higher for devices B2 and B3. Since both quantities are also directly proportional to the total oxide capacitance of the devices as described by classical velocity-saturated MOSFET theory [54, pp. 359–438], this result can be understood by the same approach used to explain the I_{on} trends in Section 2.3.1.

As seen from Fig. 2.5(d), devices B1 – B3 exhibit progressively higher r_o compared to that of the baseline. This phenomenon can be intuitively understood through the concept of drain coupling, as explained in detail in [33], where the increase in r_o is directly proportional to a coupling factor ζ_D that increases as matching improves. Since devices B1 – B3 have progressively better matching, this result is expected.

2.3.3 Cut-off Frequency f_T and $g_m f_T / I_D$

The cut-off frequency of the devices are obtained by simulating the circuits in Fig. 2.2. For each bias point, the cut-off frequency is extracted by extrapolating the magnitude of the short-circuit, common-source current gain to unity in the -20 dB/decade roll-off region, between 100 kHz and 3.3 GHz.

As seen in Fig. 2.6(a), the intrinsic (excluding parasitic components) cut-off frequency $f_{\mathrm{T,i}}$ of the NCFETs are very similar to that of the MOSFETs at all bias points, with a maximum difference of 13% between the two classes of devices. To understand this result, the following approximate formula for $f_{\mathrm{T,i}}$ can be utilized [54, pp. 359–438]:

$$f_{\mathrm{T,i}} \approx \frac{g_m}{2\pi C_{\mathrm{gg}}} \tag{2.3}$$

As seen from (2.3), $f_{\mathrm{T,i}}$ is directly proportional to g_m and inversely proportional to C_{gg}, meaning that a simultaneous change in g_m and C_{gg} in similar proportions would result in no change in $f_{\mathrm{T,i}}$. As observed in Figs. 2.5(b) and (c) and discussed in Section 2.3.2, the g_m and C_{gg} of an NCFET are both proportional to the total oxide capacitance per area. Therefore, the changes in these two parameters compensate each other in their impact on $f_{\mathrm{T,i}}$, leading to the observed performance parity between NCFETs and the baseline MOSFET.

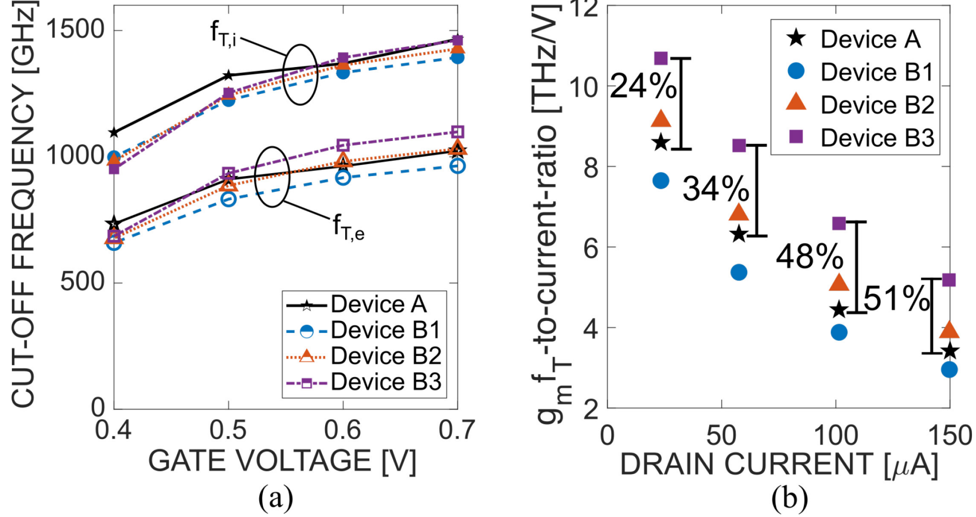


Fig. 2.6 (a) Cut-off frequency plotted against dc gate voltage at $V_D = 0.7$ V. (b) $g_m \times f_{\mathrm{T,e}}/I_D$ plotted against dc drain current, with $V_D = 0.7$ V for all devices and the same I_D between devices achieved by adjusting V_G.

For the extrinsic cut-off frequency $f_{\mathrm{T,e}}$, a degradation for both the baseline and the NCFET can be observed due to the addition of additional parasitic elements, as expected. Despite this drop, similar performance between the NCFET and the baseline continues to be observed, as seen from Fig. 2.6(a).

We have also confirmed through simulations that the addition of $R_{\rho,\mathrm{eff}}$ does not impact $f_{\mathrm{T,e}}$. This is consistent with the formula developed in [56], where $f_{\mathrm{T,e}}$ is unaffected by resistances on the gate terminal, and can be approximated by

$$f_{\mathrm{T,e}} \approx \frac{1}{2\pi} \frac{g_m}{C_{\mathrm{gg}} + C'_{\mathrm{gg}} + \left[\frac{1}{r_o}\left(C_{\mathrm{gg}} + C'_{\mathrm{gg}}\right) + g_m\left(C_{\mathrm{gd}} + C'_{\mathrm{gd}}\right)\right](R_{\mathrm{ext}})} \tag{2.4}$$

where $C'_{\mathrm{gg}} = C'_{\mathrm{gd}} + C'_{\mathrm{gs}}$ is the total extrinsic input capacitance and the other components are those shown in Fig. 2.2(c).

For low-power RF applications, especially receiver LNAs [51], another important figure of merit to consider is $g_m f_T / I_D$, which captures dc power consumption in addition to RF performance [50], [51], [83], and is calculated here using $g_m \times f_{\mathrm{T,e}}/I_D$. As seen in Fig. 2.6(b), for a given I_D, $g_m f_T / I_D$ follows the same trend as I_{on}, with device B3 achieving up to 51% higher values compared to the baseline. These trends can also be explained by the total oxide capacitance values listed in Table 2.2, as done for I_{on} in Section 2.3.1. Therefore, while

NCFETs are expected to have similar f_T as the baseline, NCFETs with a high total oxide capacitance, *e.g.*, achieved through good capacitance matching, can achieve higher $g_m f_T / I_D$.

These results of similar f_T performance but higher $g_m f_T / I_D$ show consistency with previous literature for MFMIS devices [48], [49] despite the ferroelectric having a spatially dependent potential along the channel in an MFIS structure. The reason for this similarity can be explained by the capacitance of the ferroelectric at each of the bias points. While the potential variations along the length of the channel do cause the ferroelectric to have a spatially dependent polarization in an MFIS structure, as shown in Fig. 2.7, if we examine the limits of these polarizations, it can be seen in the inset that under all bias conditions and across all NCFET devices, the ferroelectric stays within the negative capacitance region. Therefore, from a capacitance viewpoint, the ferroelectric can be intuitively considered as a linear negative capacitor in series with a conventional MOSFET, which coincides with the MFMIS view of the structure.

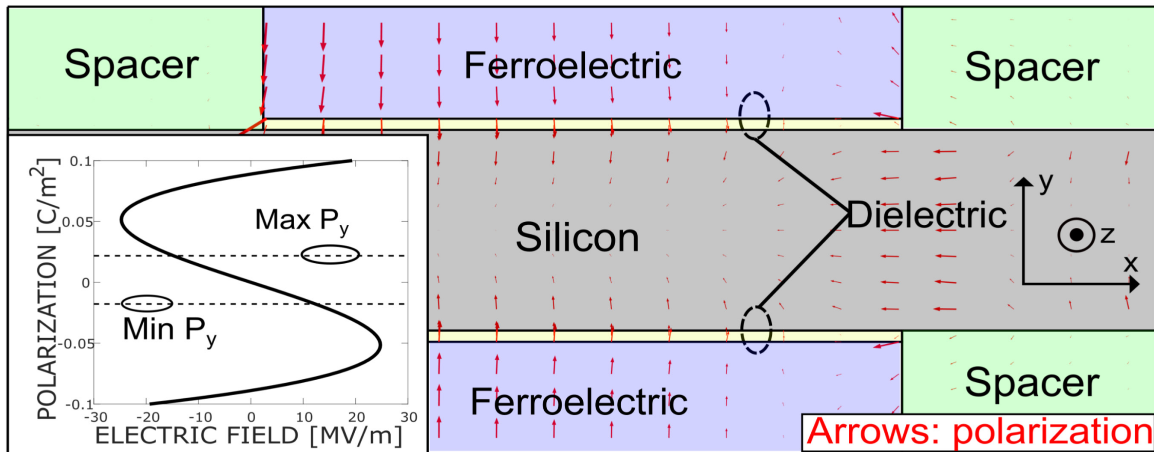


Fig. 2.7 Polarization as a function of position for device B3 at $V_G = V_D = 0.7$ V. Inset: Minimum and maximum ferroelectric polarization P_y across all bias points and all devices with the ferroelectric S-curve for a single lossless dipole, defined by (2.1) with $k = 0$.

Overall, our results thus show that while MFIS NCFETs would have a similar f_T performance, those with a higher total oxide capacitance can achieve a higher $g_m f_T / I_D$ than their baseline MOSFET counterparts.

2.3.4 Maximum Oscillation Frequency

The maximum oscillation frequency $f_{\max}$ of the devices are also extracted through simulation of Fig. 2.2(c) and extrapolation of Mason's unilateral gain [93] to unity from its −20 dB/decade roll-off region, between 100 kHz and 3.3 GHz.

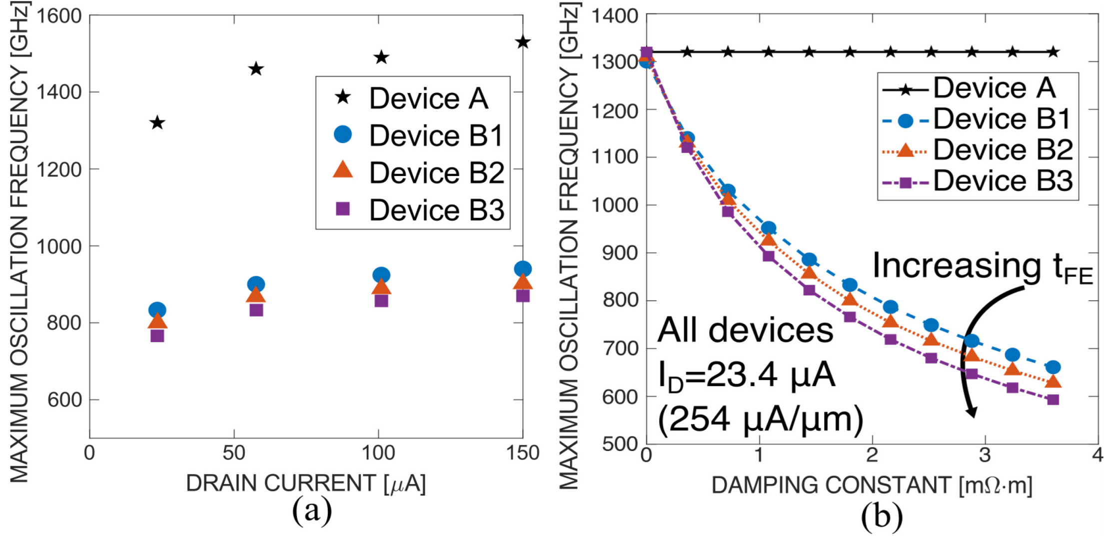


Fig. 2.8 (a) $f_{\max}$ plotted vs. dc drain current for each device. (b) $f_{\max}$ for different values of ρ for each device for a given current.

The $f_{\max}$ of each device plotted against dc current can be seen in Fig. 2.8(a). It is evident from this plot that NCFET devices all have lower $f_{\max}$ compared to the baseline, with a larger decrease as t_{FE} increases. This is a direct consequence of the ferroelectric damping constant ρ and $R_{\rho,\mathrm{eff}}$.

To understand this phenomenon, the following approximate formula for the $f_{\max}$ of a MOSFET can be used [56]

$$f_{\max} \approx \frac{f_{\mathrm{T,e}}}{\sqrt{\frac{4}{r_O}R_g + 8\pi f_{\mathrm{T,e}}\left(C_{\mathrm{gd}}+C'_{\mathrm{gd}}\right)\left[R_g+\eta_D R_d\right]}} \tag{2.5}$$

where $R_d = 0.5R_{\mathrm{ext}}$ is the resistance on the drain side of the small-signal model in Fig. 2.2(c), and $\eta_D = (C_{\mathrm{gd}} + C'_{\mathrm{gd}} + C'_{\mathrm{sd}})/(C_{\mathrm{gg}} + C'_{\mathrm{gg}})$ is the ratio of capacitances looking into the drain to those looking into the gate.

From (2.5), we can see that if gate resistance increases, f_{max} degrades. While the insertion of $R_{\rho,\mathrm{eff}}$ degrades the accuracy of directly applying (2.5) to NCFETs, we have found that a simple replacement of R_g with $R_g + R_{\rho,\mathrm{eff}} \times \left[C_{\mathrm{gg}}/(C_{\mathrm{gg}} + C'_{\mathrm{gg}})\right]^2$ is sufficient for intuitive understanding and making first-order predictions, yielding results that are within 15% of the markers in Fig. 2.8(a) for devices B1, B2, and B3. With the replacement, we find the resulting increase in gate resistance due to ρ is the central cause of the observed decrease in f_{max} for NCFETs.

2.3.5 Effect of Damping Constant on f_{max}

While $R_{\rho,\mathrm{eff}}$ is observed to decrease f_{max}, the effects of the damping parameter is still an actively studied field for NCFETs, with methods still being developed to accurately extract the damping constant ρ [11], [55]. In the future, lower ρ may be discovered or engineered. To comprehensively evaluate the effects of ferroelectric damping, we have modulated ρ and evaluated the f_{max} performance of NCFETs in comparison to the baseline and the results have been plotted in Fig. 2.8(b).

To establish a meaningful comparison between NCFET and MOSFET devices for practical RF applications in which I_{D} is used to bias the device at its dc operating point, the gate voltages of the NCFET devices have been adjusted such that all devices carry the same dc bias current I_{D}. While an I_{D} corresponding to the baseline MOSFET biased at $V_G = 0.4$ V has been selected as an example, we have found that the choice of I_{D} does not change the general trend.

As seen from Fig. 2.8(b), as ferroelectric damping becomes lower, the f_{max} performance improves as expected. At high ρ, the resistor $R_{\rho,\mathrm{eff}}$ dominates f_{max} performance for NCFETs, and therefore, for any given ρ, NCFETs with a smaller t_{FE} tend to perform better compared to those with a higher t_{FE}.

As ρ decreases, the f_{max} for devices with thicker ferroelectric layers start to converge to those with a thinner ferroelectric, as seen in Fig. 2.8(b), where the curves for devices B1 – B3 (ordered from lowest to highest t_{FE}) show vanishing differences as ρ decreases. This convergence occurs because while a higher t_{FE} leads to a higher $R_{\rho,\mathrm{eff}}$, it simultaneously leads

to better capacitance matching for a given ferroelectric-dielectric combination, which leads to a higher r_o. As ρ becomes smaller and hence $R_{\rho,\mathrm{eff}}$ becomes smaller, this difference in r_o has greater impact, and ultimately leads to the convergence of the curves.

If the ferroelectric has extremely low damping, corresponding to ρ approaching zero, one may expect from (2.5) that the NCFET can achieve a superior $f_{\max}$ performance compared to the baseline MOSFET due to an increase in r_o. However, this expected improvement is not observed, primarily because the product of total gate resistance and gate-drain capacitance, appearing algebraically as the second term in the denominator of (2.5), and well-known to dominate the $f_{\max}$ of FETs, remains sufficiently large to limit $f_{\max}$ despite the improvements to r_o.

Overall, it can be concluded through these results that the suppression of the damping constant ρ is important for the optimization of NCFETs for RF applications. With adequate suppression, similar $f_{\max}$ performance between NCFETs and the baseline MOSFET can be expected.

2.4 Conclusions

The following conclusions can be drawn from this study that investigates the RF performance of NCFETs with an MFIS stack structure, using a simulation methodology calibrated to the experimental results of [82]:

1. The intrinsic and extrinsic f_T of MFIS NCFET can be expected to be similar compared to the baseline MOSFET in a given technology, as shown in Fig. 2.6(a).

2. In comparison to a baseline MOSFET, the $f_{\max}$ of MFIS NCFETs can be additionally impacted by the ferroelectric damping term ρ, which effectively increases the gate resistance of an NCFET; however, if damping is adequately suppressed, NCFETs can achieve similar performance compared to the baseline MOSFET, as seen in Fig. 2.8(b).

3. MFIS NCFETs with a high total oxide capacitance, *e.g.*, achieved via good capacitance matching, are expected to have a substantially higher $g_m f_T / I_D$ [50], [51], [83] compared to the baseline MOSFET – by up to 51% for our devices, as shown in Fig. 2.6(b).

Overall, for NCFETs with high total oxide capacitance and low ρ, similar f_T and $f_{\max}$ performance but higher $g_m f_T/I_D$ is to be expected. With a performance parity in f_T and $f_{\max}$, and an improvement in $g_m f_T/I_D$, which is an important metric for RF performance [50], [51], [83], this work thus finds promise for next-generation, low-power RF applications with NCFETs.

Chapter 3

Potential Enhancement of f_T and $g_m f_T/I_D$ via the Use of NCFETs to Mitigate the Impact of Extrinsic Parasitics

3.1 Introduction

Negative-capacitance field-effect transistors (NCFETs) are seen as promising next-generation devices because of their abilities to alleviate undesired short-channel effects and decrease subthreshold slope (SS) [4], [14]. Recently, numerous studies have investigated various aspects, including dc, digital, and radio-frequency (RF) performance, of these novel devices. In addition to theoretical studies, promising results of NCFET performance have also been reported experimentally [26], [31].

A major area of interest for NCFETs is their performance potential for RF applications. Towards this end, previous works have extensively examined key small-signal parameters, circuit performance, as well as device-level RF figures of merit. In terms of small-signal parameters, NCFETs were found to have higher transconductance g_m [27], [28], [33], [44], [47]–[49], [72], [94], [95], higher gate capacitance C_{gg} [28], [31], [44], [48], [67], [69], [94], [96], and higher or negative output resistance r_o [13], [33], [34], [47], [69], [94]–[96]. An improved performance in linearity metrics [94], and in various analog circuits has also been found [48], [49], [76], [78], [79], [96].

At the device level, the unity-current-gain cut-off frequency (f_T), the maximum oscillation frequency ($f_{\max}$), and the $g_m f_T$-to-current ratio ($g_m f_T/I_D$) have been examined [44], [46]–[49], [94], [95]. Specifically, NCFETs were found to have similar f_T compared to baseline MOSFETs due to a simultaneous increase in g_m and C_{gg} [44], [46]–[49], [94], [95], a substantial improvement in $g_m f_T/I_D$ due to higher g_m [44], [94], and a lower $f_{\max}$ due to the impacts of the ferroelectric damping parameter ρ [44], [46], [94].

Through these investigations of small-signal parameters and key RF figures of merit, one feature that emerged was the simultaneous increase of g_m and C_{gg} compared to baseline MOSFETs, defined in this context as parameters obtained for the device *without* extrinsic parasitic elements, *i.e.*, for an intrinsic or core transistor structure. This allows NCFETs to maintain a similar *intrinsic* cut-off frequency ($f_{\mathrm{T,i}}$) compared to MOSFETs, calculated via $f_{\mathrm{T,i}} = g_m/2\pi C_{\mathrm{gg}}$ [54, Ch. 8], despite having a higher C_{gg} [44], [49], [94].

As we will detail in Section 3.2 and as suggested by [28, Fig. 19(a)], the ability to maintain a similar $f_{\mathrm{T,i}}$ while simultaneously having a higher C_{gg} enables NCFETs to potentially achieve a higher *extrinsic* cut-off frequency ($f_{\mathrm{T,e}}$), *i.e.*, the cut-off frequency found with the effect of all extrinsic parasitic elements included, [4] when compared to traditional MOSFETs. As extrinsic parasitic capacitances become increasingly dominant in aggressively scaled nodes [51], [57], the $f_{\mathrm{T,e}}$ of traditional MOSFETs will continue to be degraded. Therefore, technologies that can increase resiliency to this degradation by improving $f_{\mathrm{T,e}}$ will be important for future RF transistors.

To date, most studies of f_T in NCFETs have focused on the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [46]–[49], which is undesirable for circuit applications due to dc leakage currents destabilizing the ferroelectric negative capacitance [14], [15]. Studies using the more preferrable metal-ferroelectric-insulator-semiconductor (MFIS) structure have examined f_T through simulations [44], [94], [95] and experiments [28], [72], [97] but have not focused on the use of an NCFET to mitigate the impacts of extrinsic parasitics.

Motivated by the opportunity of improving $f_{\mathrm{T,e}}$ for scaled nodes, and the lack of examinations thus far on this promising effect, this study uses physics-based simulations in conjunction with small-signal circuits to understand the limit to which $f_{\mathrm{T,e}}$ can be improved using NCFETs.

[4] In this chapter, "f_T" will be used as a synonym for "cut-off frequency," and used when distinction between intrinsic and extrinsic versions of the quantity is not required. In cases where a distinction between intrinsic and extrinsic quantities is important, $f_{\mathrm{T,i}}$ and $f_{\mathrm{T,e}}$ will be used.

We will examine both f_T, as well as $g_m f_T/I_D$, which has recently become prominent as an RF metric [50], [51], especially for analog/RF circuits [51].

This chapter is organized into five sections. Section 3.2 will lay out a simple analytical view of the mitigation effect. Section 3.3 will summarize the methods used for the construction of the NCFET and MOSFET models, including details of the intrinsic models, ferroelectric electrostatics, and extrinsic models. Results with regards to f_T and $g_m f_T/I_D$ will be presented in Section 3.4, and the conclusions will be stated in Section 3.5.

3.2 Analytical Motivation

One intuitive way to understand the extrinsic parasitic mitigation effect is through the analytical formula for $f_{\mathrm{T,e}}$ [56]:

$$f_{\mathrm{T,e}} \approx \frac{1}{2\pi} \frac{g_m}{C_{\mathrm{gg}} + C'_{\mathrm{gg}} + \left[\frac{1}{r_o}\left(C_{\mathrm{gg}} + C'_{\mathrm{gg}}\right) + g_m\left(C_{\mathrm{gd}} + C'_{\mathrm{gd}}\right)\right](R_s + R_d)} \quad (3.1)$$

where g_m, C_{gg}, and r_o represent the transconductance, gate capacitance, and output resistance taken at the intrinsic terminals (without extrinsic parasitic resistance or capacitances) of the device, C'_{gg} and C'_{gd} represent the extrinsic parasitic capacitances, and R_s and R_d represent the extrinsic parasitic resistances.

Ignoring the effects of the term multiplied by the sum of R_s and R_d, which is typically small compared to the C'_{gg} term, and rearranging the formula, the following result can be obtained:

$$f_{\mathrm{T,e}} \approx f_{\mathrm{T,i}} \frac{1}{1 + \frac{C'_{\mathrm{gg}}}{C_{\mathrm{gg}}}} \quad (3.2)$$

Since NCFETs can follow the same fabrication procedures as standard MOSFETs, a similar device and layout structure can be used, and the extrinsic parasitic element C'_{gg} can be assumed to be similar between the devices. As seen directly from (3.2), a form of which first appeared in [28, Fig. 19(a)], the higher intrinsic gate capacitance C_{gg} in NCFETs [28], [44], [48], [67], [94], [96] will lead to a higher $f_{\mathrm{T,e}}$, since they are expected to have a similar $f_{\mathrm{T,i}}$ to

MOSFETs [44], [46]–[49], [94], [95], but the second term in the denominator of (3.2) will be smaller.

3.3 Methodology

3.3.1 Intrinsic Device Modeling

3.3.1-A. MOSFET Design and Modeling

MOSFET devices based on the IRDS 10-nm and 7-nm node have been modeled with key parameters picked based on literature values [2], [82], [85], [98]–[102]. A schematic of the intrinsic device can be found on the left side of Fig. 3.1(a). Simulation of devices have been conducted in the same manner as our previous work, which was calibrated to an experimental device [44]. For this work, the intrinsic MOSFET devices have been calibrated by matching the on-current (I_{on}) and off-current (I_{off}) to high-performance devices in the literature [98], [99], [103] through the adjustment of the low-field mobility μ_n, saturation velocity v_{sat}, and metal work function ϕ_m. Specifically, the 10-nm device has an I_{on} of 1.81 mA/μm, and the 7-nm device has an I_{on} of 2.05 mA/μm. The I_{off} of both MOSFET devices have been set to 100 nA/μm. The drain current (I_D) to gate voltage (V_G) characteristic of the 10-nm and 7-nm device can be found in Figs. 3.1(b) and (c), respectively, and important simulation parameters for both the 10-nm and the 7-nm device can be found in Table 3.1.

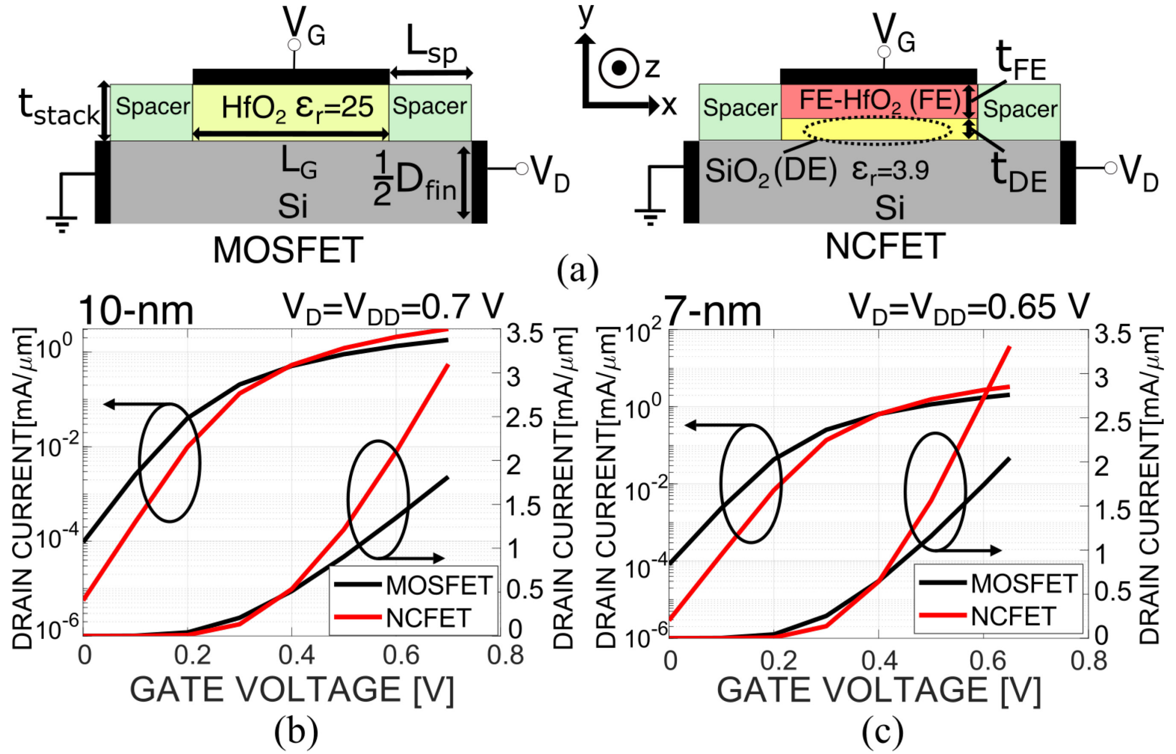


Fig. 3.1 (a) Schematic diagram of the intrinsic MOSFET and NCFET, where the fin height extends into the *z*-direction. Only half of the devices are shown, as all device structures are symmetrical. All labels are shared between devices. (b) I_D-V_G results for the 10-nm intrinsic NCFET and MOSFET. (c) I_D-V_G results for the 7-nm intrinsic NCFET and MOSFET.

Parameter	10-nm Node Value	7-nm Node Value
Gate Length (L_G)	20 nm	16 nm
Fin Width (D_{fin})	7 nm	5.5 nm
Fin Height (H_{fin})	46 nm	50 nm
Spacer Length (L_{sp})	8 nm	6.5 nm
Stack Thickness (t_{stack})	5 nm	4 nm
Effective Oxide Thickness	0.78 nm	0.62 nm
Spacer Permittivity	4.5	4.0
Source and Drain Doping Concentration ($N_{\text{S/D}}$)	10^{20} cm^{-3}	10^{20} cm^{-3}
Channel Doping Concentration (N_{ch})	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}
Low-Field Mobility (μ_{n})	300 cm^2/Vs	340 cm^2/Vs
Velocity Saturation Exponent (β)	2 (electron) /1 (hole)	2 (electron) /1 (hole)
Saturation Velocity (v_{sat})	2.1 x 10^7 cm/s	2.1 x 10^7 cm/s
Metal Work Function (ϕ_m)	4.328 eV	4.325 eV

Supply Voltage (V_{DD})	0.7 V	0.65 V
Remnant Polarization (P_r)	$0.14\ \mathrm{C/m^2}$	$0.14\ \mathrm{C/m^2}$
Coercive Field (E_c)	$2 \times 10^8\ \mathrm{V/m}$	$2 \times 10^8\ \mathrm{V/m}$
Multidomain Parameter k	$10^{-8}\ \mathrm{m^3/F}$	$10^{-8}\ \mathrm{m^3/F}$
NCFET Dielectric Thickness (t_{DE})	0.78 nm	0.62 nm
NCFET Ferroelectric Thickness (t_{FE})	4.22 nm	3.38 nm

Table 3.1 Device and transport parameters.

3.3.1-B. NCFET Design

A schematic of the intrinsic NCFET device can be seen on the right side of Fig. 3.1(a). The NCFET devices have been designed with the same oxide stack height t_{stack} of the reference MOSFETs, because t_{stack} will be limited by the amount of space between fins in advanced nodes [31], [44].

For these NCFETs, ferroelectric $\mathrm{HfO_2}$ and $\mathrm{SiO_2}$ have been chosen as the ferroelectric and dielectric layers [26], [87], respectively. Leakage current through the ferroelectric layer has not been modeled, because it would not destabilize an MFIS NCFET [14], [15], and the magnitude of the leakage current is also shown to be negligible compared to the drain current [26], [27]. The capacitance of the combined ferroelectric-dielectric stack has been selected such that the series combination of the linear ferroelectric negative capacitance [4] and the dielectric layer capacitance is nominally a factor of 3.3 × higher than that of the MOSFET oxide capacitance. This ratio is picked as a compromise between maximizing $f_{\mathrm{T,e}}$ and avoiding hysteresis. To clarify, maximizing the ratio, and thus maximizing C_{gg} [44], would maximize $f_{\mathrm{T,e}}$ as seen from (3.2), but a ratio that is too large would require too close a match between the ferroelectric and dielectric capacitances, making the match vulnerable to variations during fabrication, which may inadvertently violate the matching condition [4], [15] required to avoid hysteresis.

While a variety of layer thicknesses, t_{DE} and t_{FE}, and material combinations can be used for the oxide stack [44], it is expected that the results will be the same to first order if the choice made is within the constraints of attaining the nominal capacitance increase of 3.3 × and with realistic materials. This outcome is based on the observation that f_T and $g_m f_T / I_D$ are primarily governed by the final series capacitance combination of the ferroelectric and dielectric layers, rather than individual layer thicknesses [44] or specific materials yielding the capacitances. In

our case, the value of t_{DE} is chosen to match the SiO_2-normalized effective oxide thickness of the MOSFET.

3.3.1-C. Ferroelectric Modeling and Parameters

The ferroelectric HfO_2 layer in NCFETs has been modeled using the multi-domain Landau-Khalatnikov equation [13], [44], [52], [104], implemented in the same manner as [44]. Ferroelectric parameters α and β have been picked to attain the nominal capacitance ratio as discussed in Section 3.3.1-B, and their values have been calculated using the remnant polarization P_r and coercive voltage E_c of the ferroelectric layer [29]. Out of a variety of possible E_c and P_r value pairs that are consistent with literature ranges [9] and that satisfy the nominal capacitance ratio, the pair that maximizes the width of the negative capacitance region is picked in order to maximize bias ranges in which the device is operating in the negative capacitance region. In addition, these specific values for E_c and P_r are consistent (within 10%) with those obtained experimentally for Sr-doped HfO_2 [105] and are shown in Table 3.1. It is expected that the trends would not qualitatively change provided the *ratio* of E_c to P_r, which dictates the nominal capacitance ratio by dictating the ferroelectric parameter α [106], is similar. Multidomain effects in the form of coupling between adjacent dipoles are modeled using the k parameter [13], [44], [59], [104], picked to be consistent with literature ranges [13], [44], [59], [104], and also shown in Table 3.1.

3.3.2 Extrinsic Structure

To model parasitic capacitance and resistance outside of the intrinsic FET region, a representative multi-finger extrinsic structure [58, Ch. 4] comprised of interconnects up to the M3 metal level has been modeled. In the immediate area surrounding the intrinsic region, a raised source and drain structure has been chosen, with parameters obtained from [107]. A schematic diagram of the structure can be seen in Fig. 3.2, where the intrinsic regions depicted in Fig. 3.1(a) correspond to a top view of the dashed box in Fig. 3.2(a).

By connecting five units of the structure depicted in Figs. 3.2(a) and 3.2(b) in a row, and building metal lines around them, five gate fingers with one row of fins have been modeled, as shown in Fig. 3.2(c). Here, two gate contacts have been utilized, and metal lines for each

contact have been stacked to minimize resistance. Important parameter values for this overall structure are listed in Table 3.2 [2], [82], [85], [99]–[101], [103], [108].

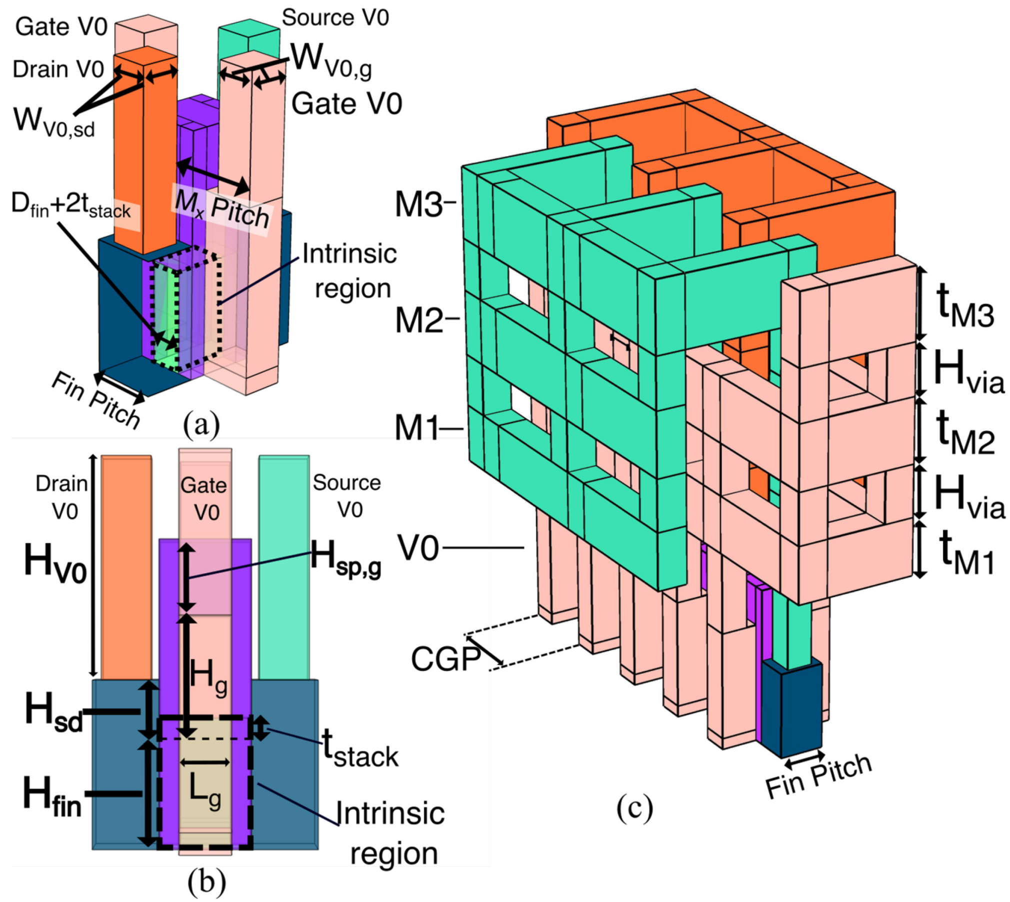


Fig. 3.2 (a) Perspective view and (b) side view of one fin of the extrinsic structure. (c) 3-D view of the extrinsic structure with interconnects up to M3.

Parameter	10-nm Node Value	7-nm Node Value
Fin Pitch	34 nm	27 nm
Contacted Gate Pitch (CGP)	62 nm	51 nm
Gate Height (H_g)	40 nm	40 nm
Source and Drain Height (H_{sd})	20 nm	20 nm
Spacer Height Above Gate ($H_{sp,g}$)	30 nm	30 nm
M_x Pitch	35 nm	28 nm
M_x Width	23 nm	18 nm
V0 Height (H_{V0})	88 nm	88 nm
Source Drain V0 Width ($W_{V0,SD}$)	19.5 nm	16.5 nm

Gate V0 Width ($W_{\text{V0,G}}$)	20 nm	16 nm
M1/M2/M3 Thickness ($t_{\text{M1}}, t_{\text{M2}}, t_{\text{M3}}$)	44 nm/50 nm/55nm	44 nm/50 nm/55nm
Interlayer Via Height (H_{via})	40 nm	40 nm
Interlayer Dielectric Constant	2.5	2.5

Table 3.2 Extrinsic structure parameters.

3.3.3 Small-Signal Circuits

To find f_T, a small-signal circuit simulation approach is used. The MOSFET and NCFET small-signal circuits follow from [44], and the same methods have been used to extract intrinsic circuit elements. A diagram of the circuit can be found in Fig. 3.3. The effects of all important device physics are reflected in the values of the small-signal circuit parameters, *e.g.*, the effects of drain-induced barrier raising in NCFETs is reflected via values of r_o. Note that for this study, the ferroelectric damping resistor and the gate resistance, which have previously been modeled [44], have been omitted. This is done to simplify the simulation procedure, and will not at all alter the results, as it is well-known that the gate resistance does not change f_T [109]. We have also verified through simulations in [44] that a change in the ferroelectric damping parameter ρ does not change f_T.

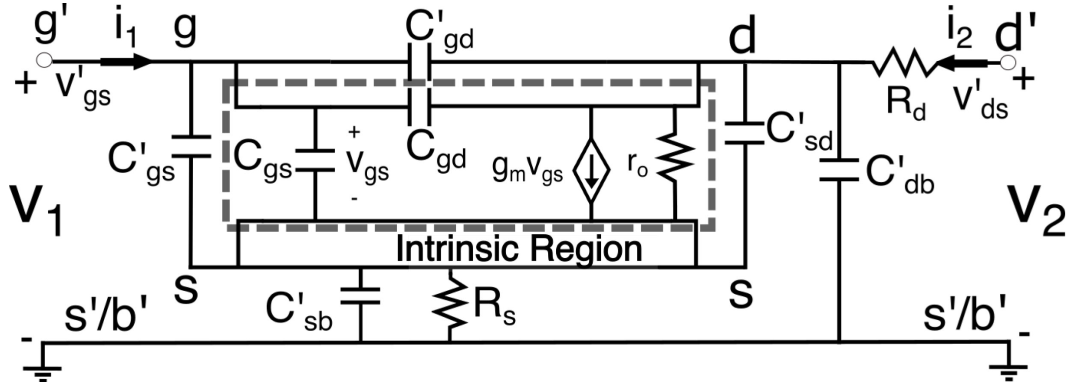


Fig. 3.3 Small-signal circuit for both the MOSFET and NCFET.

The extrinsic parasitic capacitances, C'_{gs}, C'_{gd}, C'_{sd}, C'_{db}, and C'_{sb} have been obtained in the same way as [5]. The R_s and R_d of 10-nm devices have been obtained by a microscopic Ohm's law [110] simulation of the structure shown in Fig. 3.2(c), with literature values for resistivities [2], [85], [90], [91]. Specifically, the line resistances for M1, M2 and M3 metal lines are 130 $\Omega/\mu\text{m}$, normalized to the line cross section, and all via resistances are 30 Ω/via [2], [85]. The

material of via layer V0 is assumed to be tungsten, and its resistivity taken to be $3 \times 10^{-7} \Omega \cdot$ cm [90]. The contact resistivity between V0 and silicon is set to $10^{-9}\, \Omega \cdot \mathrm{cm}^2$, and the epitaxial silicon resistance of the source and drain extension region is set to 20% of the channel resistance, both of which are consistent with literature values [91]. R_s and R_d of the 7-nm devices are obtained by reducing the width-normalized R_s and R_d of the 10-nm devices by 15%, following IRDS predictions [2], [85]. Width-normalized values of the parasitics are listed in Table 3.3.

Parameter	**10-nm Node Value**	**7-nm Node Value**
C'_{gs}	338.24 aF/μm	290.44 aF/μm
C'_{gd}	296.95 aF/μm	255.09 aF/μm
C'_{sd}	73.81 aF/μm	64.04 aF/μm
C'_{sb}	11.33 aF/μm	7.13 aF/μm
C'_{db} ($V_D = V_{\mathrm{DD}}$)	8.77 aF/μm	5.60 aF/μm
R_s	96.4 Ωμm	84.0 Ωμm
R_d	96.4 Ωμm	84.0 Ωμm

Table 3.3 Width normalized parasitic values.

3.4 Results

3.4.1 Baseline Results

The f_T of all devices have been extracted through simulation of the small-signal circuit in Fig. 3.3 and extrapolation of the resulting two-port h_{21} parameter in the range of 100 kHz to 5 GHz. For the discussion of this section, the focus will be on the 10-nm MOSFET and NCFET devices, which suffice to make the initial observations.

The f_T values are plotted versus I_D at a fixed drain voltage of $V_D = V_{\mathrm{DD}}$ to allow comparison under the same power consumption, calculated as $P = I_D \times V_{\mathrm{DD}}$. This iso-power condition will be used as the basis for comparison throughout this study, as power consumption is equally as important as performance metrics. The I_D values of the MOSFET and NCFET devices are matched by tuning the gate voltage V_G of the NCFET until its I_D matches with that of the MOSFET.

The f_{T} values of the NCFET and MOSFET are shown in Fig. 3.4(a), with both $f_{\mathrm{T,i}}$ (upper two solid lines) and $f_{\mathrm{T,e}}$ (lower two dashed lines) displayed. Here, the right-most points for both sets of lines correspond to the maximum possible V_G, *i.e.*, $V_G = V_D = V_{\mathrm{DD}}$, and hence the $f_{\mathrm{T,e}}$ lines do not extend as far as the $f_{\mathrm{T,i}}$ lines because R_s and R_d limits I_D at maximum V_G and V_D. As seen from the dashed lines, the peak $f_{\mathrm{T,e}}$ of the 10-nm NCFET is 20% higher than that of the MOSFET, demonstrating the ability for NCFETs to improve $f_{\mathrm{T,e}}$ by mitigating the effects of parasitic capacitances, following the basic premise from (3.2), *i.e.*, with the NCFET sustaining $f_{\mathrm{T,i}}$ but with its higher intrinsic gate capacitance C_{gg} used to mitigate the usual degradation of $f_{\mathrm{T,e}}$ from $f_{\mathrm{T,i}}$ due to C'_{gg}. We will explore this outcome in detail, but first note that this 20% improvement is comparable to the improvement in peak $f_{\mathrm{T,e}}$ when technology advances to the next node in planar technologies [57]. For FinFETs, excessive parasitic capacitance causes peak $f_{\mathrm{T,e}}$ to degrade as nodes advance, and 20% improvement would be sufficient to bring the peak $f_{\mathrm{T,e}}$ back to similar levels of a prior node [57]. We also note that in many prior simulation works [44], [47], [48], [94], [95], this type of increase in $f_{\mathrm{T,e}}$ was not prominently observed because there were only small amounts of parasitic capacitances included outside of the intrinsic device. However, this type of improvement in $f_{\mathrm{T,e}}$ *was* observed in [72], where measurements were done on an experimental structure, which would include numerous parasitic components.

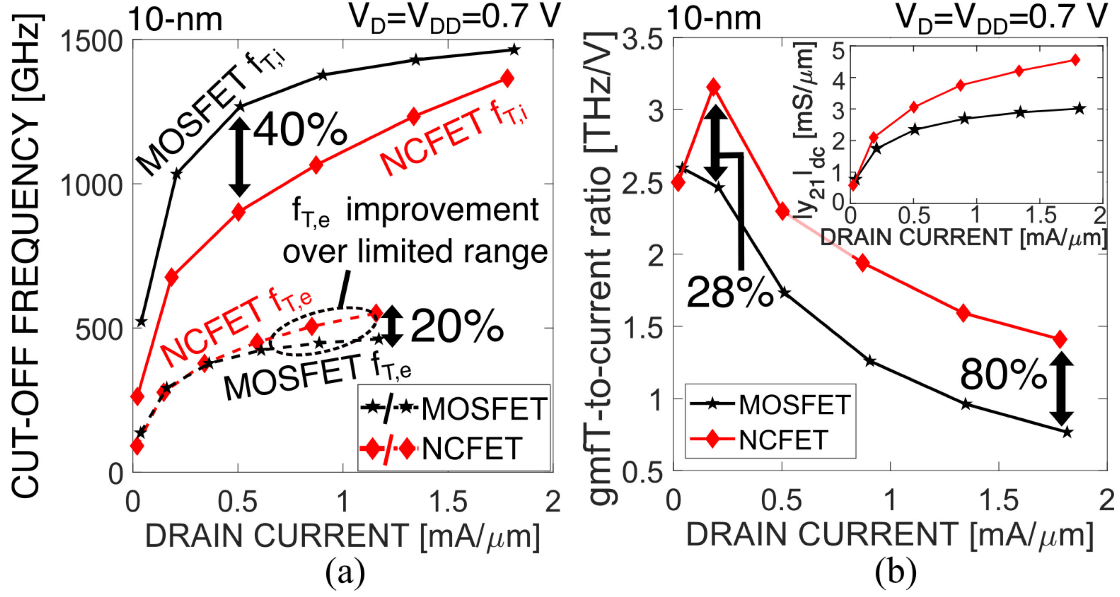


Fig. 3.4 (a) $f_{\mathrm{T,e}}$ and $f_{\mathrm{T,i}}$ of the 10-nm MOSFET and NCFET. (b) $g_m f_T/I_D$ for the 10-nm MOSFET and NCFET. Inset: $|y_{21}|_{\mathrm{dc}}$ of devices.

Comparison of $g_m f_T/I_D$ can be seen in Fig. 3.4(b). Here, $g_m f_T/I_D$ is calculated via $|y_{21}|_{\mathrm{dc}} \times f_{\mathrm{T,e}}/I_D$, where $|y_{21}|_{\mathrm{dc}}$ is the transconductance including parasitic elements and is found via the magnitude of the y_{21} parameter of Fig. 3.3 at dc. As seen from Fig. 3.4(b), the NCFET displays a significant improvement of $g_m f_T/I_D$ of up to 80%, owing to both the improvements in $f_{\mathrm{T,e}}$ and in $|y_{21}|_{\mathrm{dc}}$, the latter of which is directly related to the well-known improvements of g_m in NCFETs.

One undesirable feature apparent from Fig. 3.4(a) is a general reduction of $f_{\mathrm{T,i}}$ in NCFETs; from (3.2), even if NCFETs offer a decrease in the $C'_{\mathrm{gg}}/C_{\mathrm{gg}}$ ratio, improvement in $f_{\mathrm{T,e}}$ is diminished if $f_{\mathrm{T,i}}$ decreases. As seen from the solid curves in Fig. 3.4(a), the $f_{\mathrm{T,i}}$ of the 10-nm NCFET is 40% lower than that of the reference MOSFET at $I_D = 0.5\ \mathrm{mA/\mu m}$, and this disparity in $f_{\mathrm{T,i}}$ continues to increase for lower bias currents. This reduction limits performance potential by limiting the bias ranges in which the NCFETs would display an improved $f_{\mathrm{T,e}}$, as seen in the dotted lines of Fig. 3.4(a). Stemming from the reduction in $f_{\mathrm{T,i}}$, the $g_m f_T/I_D$ of the NCFETs is also hindered at lower currents. As seen from Fig. 3.4(b), the NCFET $g_m f_T/I_D$ is only 28% higher than the MOSFET when comparing at the low current corresponding to the peak values, and the NCFET $g_m f_T/I_D$ drops below the MOSFET at ultra-

low currents. Overall, this reduction of $f_{\mathrm{T,i}}$ is caused by the unique electrostatics of the NCFET, which will be further discussed in the next section.

3.4.2 Intrinsic Analysis

3.4.2-A. $f_{\mathrm{T,i}}$ Degradation

The reduction of $f_{\mathrm{T,i}}$ observed in Fig. 3.4(a) is echoed in the behavior of the g_m and C_{gg} of the intrinsic NCFET and the MOSFET. As seen in Figs. 3.5(a) and (b), at low bias ($I_D = 0.5\ \mathrm{mA/\mu m}$), g_m is only increased by 50% in the NCFET, whereas C_{gg} is increased by 111%; for higher biases ($I_D = 1.8\ \mathrm{mA/\mu m}$), this situation improves, and the g_m increase of 92% is close to the C_{gg} increase of 111%. Since $f_{\mathrm{T,i}}$ is calculated via a ratio between g_m and C_{gg} [54, Ch. 8], this results in a large reduction of the NCFET $f_{\mathrm{T,i}}$ at low biases, and a smaller reduction at high biases, as seen in Fig. 3.4(a).

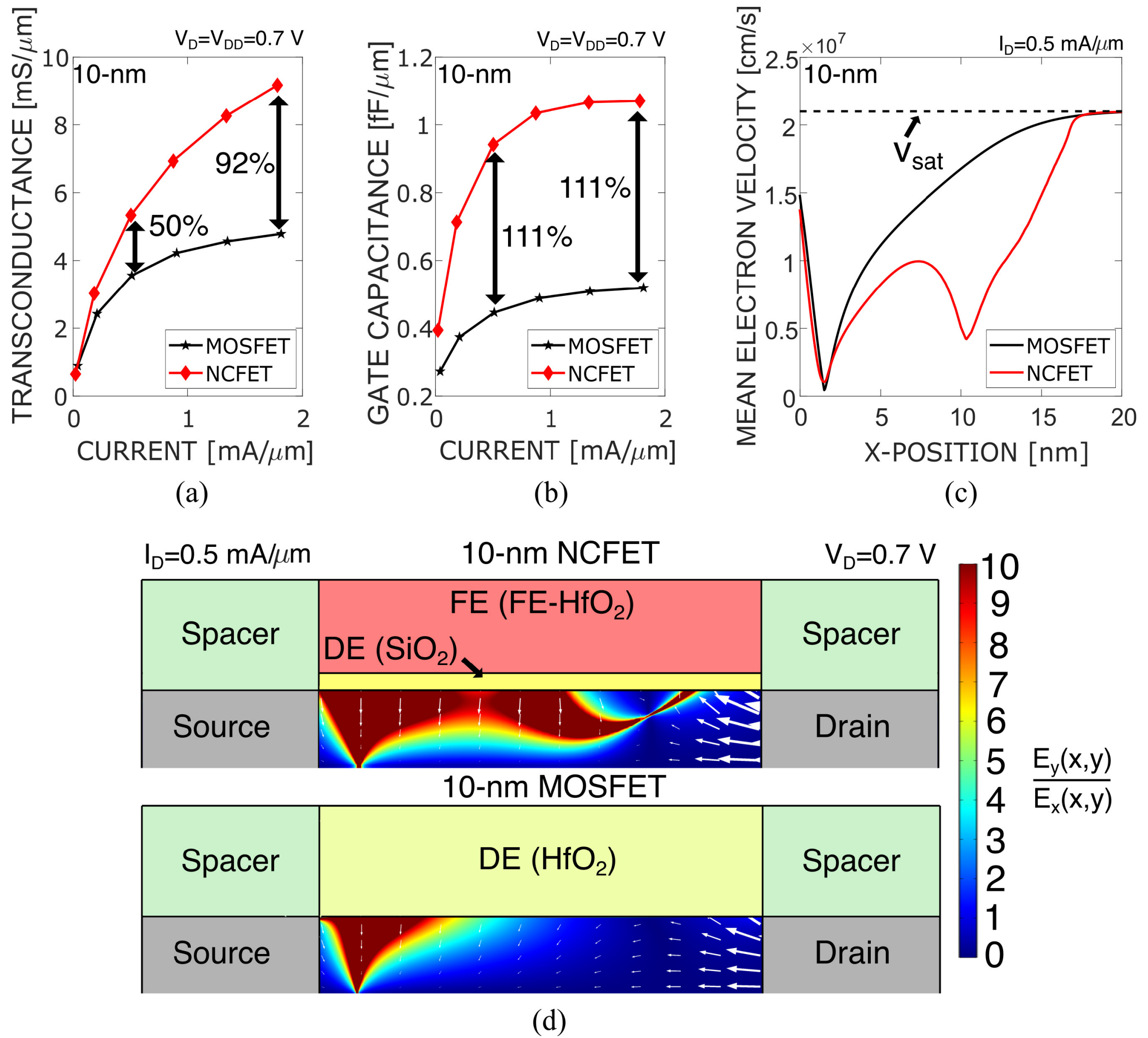


Fig. 3.5 (a) Width-normalized transconductance of 10-nm MOSFET and NCFET. (b) Width-normalized gate capacitance of 10-nm MOSFET and NCFET. (c) Average electron velocity of 10-nm MOSFET and NCFET, at $I_D = 0.5$ mA/μm. (d) Electric-field ratio of 10-nm MOSFET and NCFET, at $I_D = 0.5$ mA/μm. Arrows represent electric-field lines. Only the top half of each device is shown; the bottom half is symmetrical to that of the top half.

This phenomenon can be explained by the unconventional electrostatics of the NCFET, which has been examined in numerous studies in terms of improvement of drain-induced barrier lowering (DIBL) and r_o, *e.g.*, [26], [31], [33], [34], [36], [37], [59], and which originates from the *de*-amplification of channel potential near the drain side of the channel [34] due to a combination of fringing field from the drain and the negative capacitance of the ferroelectric.

This electrostatic effect can be considered as causing the NCFET to *electrically behave* like a longer channel device compared to a reference MOSFET, with the NCFET electrostatics *effectively* increasing the channel length, despite both devices having the same *physical* channel length.

Device characteristics, such as electron velocity and electric field distribution, support this concept of a higher effective channel length. As seen in Fig. 3.5(c), the NCFET has a lower electron velocity compared to the MOSFET, which has also been previously observed in [95]. Further, as seen in Fig. 3.5(d), the gate-direction (vertical in the figure) electric field is more dominant across a larger portion of the channel in the NCFET. Both these characteristics are consistent with the notion of an effectively longer channel. Overall, this effective increase in channel length from NCFET electrostatics can be used to intuitively explain the degradation of $f_{\mathrm{T,i}}$ in NCFETs, analogous to the well-known effect where a longer physical channel leads to a decrease of $f_{\mathrm{T,i}}$.

To explain the bias dependence of the degradation of $f_{\mathrm{T,i}}$, the concept of gate control versus drain control can be utilized. At lower currents, and hence lower V_G, the drain dominates channel electrostatics. Since $f_{\mathrm{T,i}}$ degrades due to the unconventional drain electrostatics explained earlier, the disparity between $f_{\mathrm{T,i}}$ value is high in this region of operation. As current increases, the gate starts to control channel electrostatics, and the two $f_{\mathrm{T,i}}$ values start to converge.

3.4.2-B. Strategies for Overcoming the $f_{\mathrm{T,i}}$ Discrepancy

To overcome the undesirable $f_{\mathrm{T,i}}$ degradation in NCFETs, which limits the $f_{\mathrm{T,e}}$ performance benefits, two strategies will be discussed here, which will be tested via simulations in subsequent subsections. While we will only discuss two potential strategies here, we note there may be other device tuning strategies (*e.g.*, tuning of channel mobility [28]).

First, consider downscaling of the physical channel length L_G, which will decrease the disparity in $f_{\mathrm{T,i}}$ between the NCFET and MOSFET. In previous studies [26], [36], [37], [52], it was observed that both DIBL and SS of NCFETs, while improved over MOSFETs, will still increase as L_G decreases at very short channel lengths, *i.e.*, that short-channel effects affect

NCFETs in a similar way compared to standard MOSFETs. Therefore, as L_G decreases, a larger proportion of the channel will become velocity saturated for both the MOSFET and the NCFET, and the electron velocities of both devices will eventually converge towards the limit of a fully velocity-saturated channel. This convergence of velocities will in turn decrease the difference in $f_{\mathrm{T,i}}$ between the devices, with the $f_{\mathrm{T,i}}$ values both approaching the fully velocity-saturated limit of $1.5 \times v_{\mathrm{sat}}/2\pi L_G$ [54, Ch. 8].

Second, as seen from Fig. 3.4(a), $f_{\mathrm{T,i}}$ is higher for devices operating at higher I_D, which can also be exploited to alleviate the degradation of $f_{\mathrm{T,i}}$ in NCFETs. Since NCFETs have a much lower I_{off} than that of the baseline MOSFET, as seen in Fig. 3.1, their threshold voltage V_{th} can be lowered without compromising standby power versus MOSFETs, which will allow for an increase in I_D for a given V_G. This increase in current will in turn increase $f_{\mathrm{T,i}}$, as seen from Fig. 3.4(a). However, lowering V_{th} alone will not be sufficient, as a higher I_D at the same V_{DD} will increase the power consumption of the NCFET above the MOSFET, which will violate the basis of iso-power comparison as discussed in Section 3.4.1. Hence, it is also necessary to simultaneously decrease V_{DD} in the NCFETs along with their V_{th}.

3.4.2-C. Scaling Effects

To investigate the first of the above two strategies, *i.e.*, how L_G scaling affects $f_{\mathrm{T,i}}$, an intrinsic device at the 5-nm node is simulated in addition to the 10- and 7-nm devices. Since dimensions for the 5-nm node are scarce, a representative 5-nm device was built with parameters derived from the 7-nm parameters in Table 3.1, by scaling each dimension by 0.87× to 0.9×, consistent with trends in the IRDS [2], [85].

To visualize the effects of L_G scaling, the reduction of $f_{\mathrm{T,i}}$ in NCFETs for various operating powers as a function of gate length is plotted in Fig. 3.6(a), with the top-left point corresponding to the 40% seen in Fig. 3.4(a). As seen from the figure, as L_G scales down, the disparity in $f_{\mathrm{T,i}}$ decreases, and this effect is especially prominent for devices operating at low powers. Therefore, aggressive L_G scaling will be beneficial in maximizing the $f_{\mathrm{T,e}}$ benefits of NCFETs, as it alleviates the undesirable effects from the reduction of $f_{\mathrm{T,i}}$.

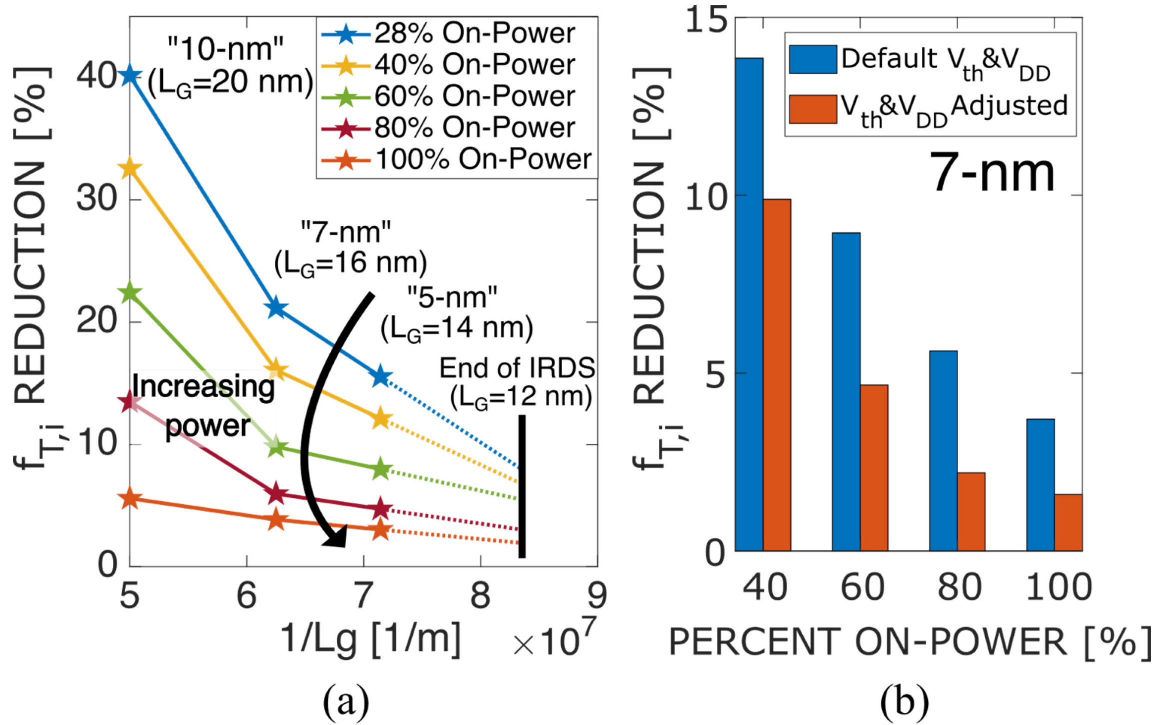


Fig. 3.6 (a) Changes in $f_{\mathrm{T,i}}$ reduction in the intrinsic NCFET vs. the MOSFET as channel length scales down for different levels of operating power, extrapolated linearly to the end of the IRDS. (b) Differences in $f_{\mathrm{T,i}}$ reduction between default NCFET and NCFET with adjusted V_{th} and V_{DD}, demonstrated using the 7-nm device.

3.4.2-D. V_{th} and V_{DD} Adjustment

As discussed in Section 3.4.2-B, another strategy of decreasing the disparity in $f_{\mathrm{T,i}}$ between the NCFET and MOSFET is to simultaneously decrease the V_{DD} and V_{th}. To investigate this approach, we have adjusted the V_{th} of the 7-nm NCFET device in Fig. 3.1(c) such that I_{off} of the NCFET matches up with the MOSFET, and have lowered V_{DD} from 0.65 V to 0.55 V, corresponding to the predicted value for the end of the IRDS [2], [85]. The result of this adjustment can be seen in Fig. 3.6(b), where the V_{th} and V_{DD} adjusted devices have attained minor improvements of $f_{\mathrm{T,i}}$, primarily for devices operating at high operating power. Overall, this is an additional strategy that can maximize the $f_{\mathrm{T,e}}$ benefits of the NCFET. However, since the improvement to $f_{\mathrm{T,i}}$ is small, this adjustment will not maximize $g_m f_T / I_D$, as the detriment of the increase in I_D will outweigh the benefits of the increase in $f_{\mathrm{T,e}}$.

3.4.3 Extrinsic Analysis

3.4.3-A. Nominal Parasitic Results

To examine the effects of extrinsic parasitic elements on the potential for NCFETs to provide enhancements of $f_{\mathrm{T,e}}$, 7-nm devices with nominal extrinsic elements will be used as the baseline for comparison. The 7-nm devices are used because as discussed in Section 3.4.2, the NCFETs will have less degradation in $f_{\mathrm{T,i}}$, which will lead to more pronounced performance benefits for $f_{\mathrm{T,e}}$. To further maximize the performance of NCFETs, V_{DD} and V_{th} adjustment according to Section 3.4.2 will also be applied to devices that are used for the comparison of f_T, but not to devices that are used for the comparison of $g_m f_T/I_D$. This approach will demonstrate the best-case performance potential for each figure of merit.

The f_T and $g_m f_T/I_D$ of these 7-nm devices can be seen in Fig. 3.7. Since some comparisons are done for devices operating at different V_{DD}, the x-axis has been changed from current to power. As seen in Fig. 3.7(a), the improvement of $f_{\mathrm{T,e}}$ for NCFETs occurs across a larger bias range compared to the 10-nm devices in Fig. 3.4(a) due to less disparity in $f_{\mathrm{T,i}}$ between the devices. Similarly, as seen in Fig. 3.7(b), the $g_m f_T/I_D$ performance is also better for the 7-nm devices at lower power, and the improvement in $g_m f_T/I_D$ increased from 28% to 35% at the peak value.

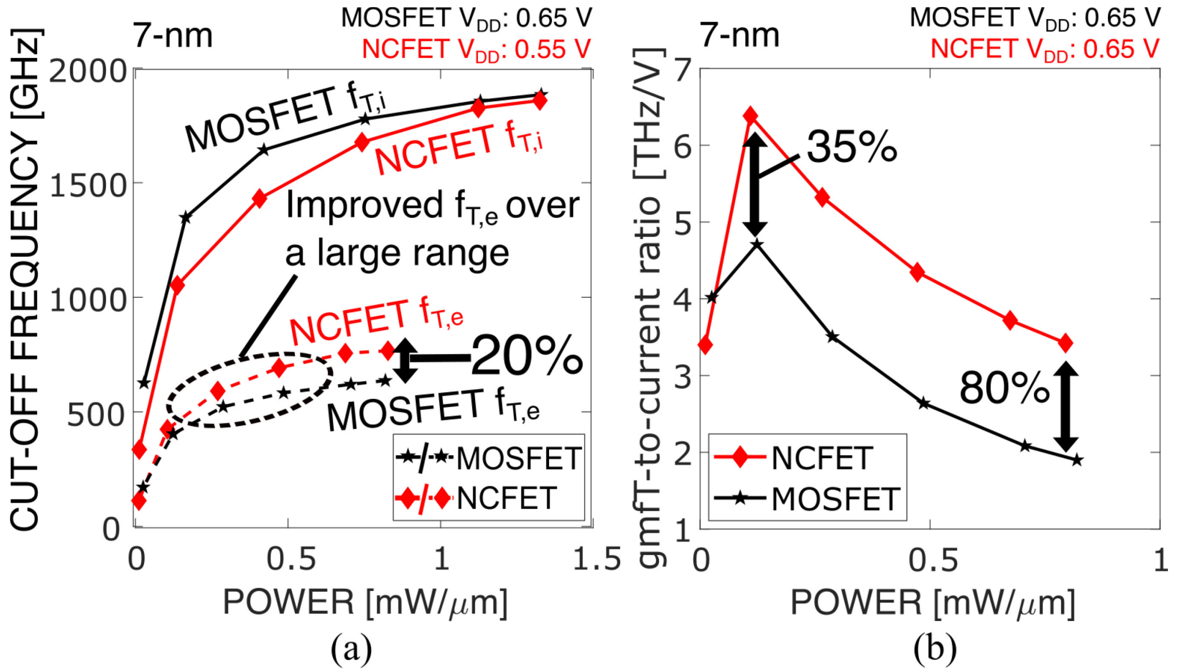


Fig. 3.7 (a) $f_{\mathrm{T,e}}$ and $f_{\mathrm{T,i}}$ for 7-nm device with adjusted V_{th} and V_{DD} for the NCFET; a much greater range of improvement in $f_{\mathrm{T,e}}$ can be observed compared to Fig. 3.4(a). (b) $g_m f_T / I_D$ for 7-nm device with normal V_{th} and V_{DD}.

3.4.3-B. Effect of Parasitic Resistances

As downscaling of devices continue, one of the most important engineering challenges is the reduction of the extrinsic parasitic resistances of the source and drain, R_s and R_d. To investigate the effect of these extrinsic parasitic resistances on the degree of advantage NCFETs can provide, we have varied the values of R_s and R_d between the ideal value of 0 Ω and 2.5 × the nominal value shown in Table 3.3. Throughout this test, the extrinsic parasitic capacitances C'_{gs} and C'_{gd} have been kept at their nominal values, and the results of peak $f_{\mathrm{T,e}}$ can be found in Fig. 3.8(a). As seen in the figure, the extrinsic parasitic resistances can hinder the improvement of $f_{\mathrm{T,e}}$ offered by NCFETs, with a 30% improvement of peak $f_{\mathrm{T,e}}$ in the ideal case decreasing to 20% at the nominal extrinsic parasitic resistances, and 11% at 2.5× the nominal value. Similarly, we found the maximum improvement in $g_m f_T / I_D$ is reduced from 144% in the ideal case to 80% in the nominal case, and 60% at 2.5× the nominal value. These reductions occur because higher R_s and R_d lower the peak operating current of both devices, which in turn lowers peak power. Since the $f_{\mathrm{T,i}}$ of NCFETs suffer a greater degradation at

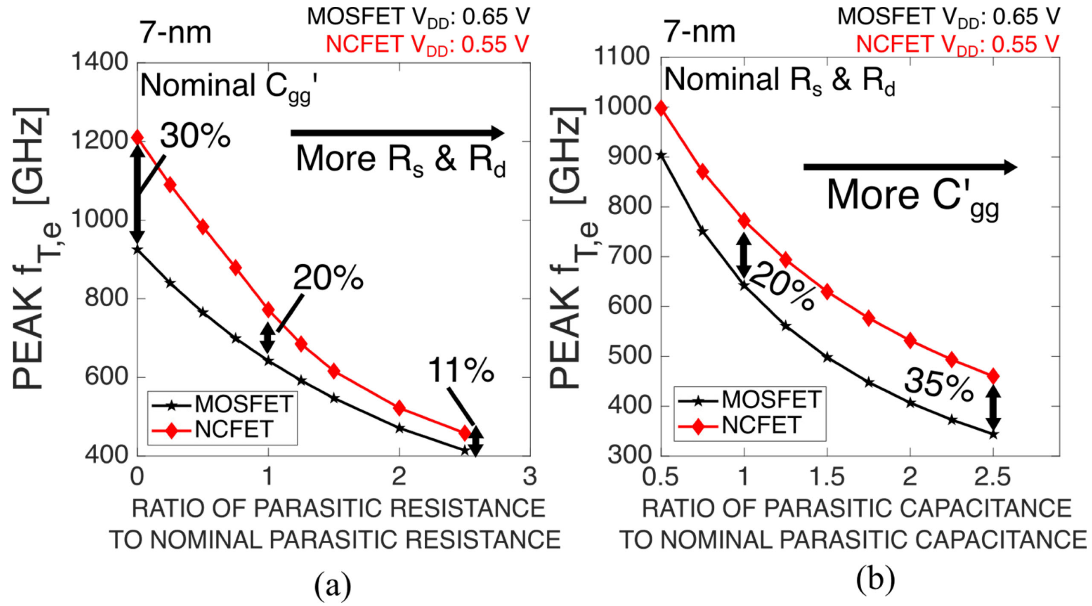


Fig. 3.8 Peak $f_{\mathrm{T,e}}$ for 7-nm devices with adjusted V_{th} and V_{DD} for various (a) R_s and R_d, and (b) C'_{gs} and C'_{gd}, normalized to the nominal values seen in Table 3.3.

lower powers as seen from Fig. 3.7(a), the peak $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ boost degrades as R_s and R_d increases.

3.4.3-C. Effect of Parasitic Capacitances

Another important extrinsic factor to consider is capacitance, which is highly layout dependent. To investigate the effects of extrinsic parasitic capacitances on the potential benefits of the NCFET, we have swept the values of C'_{gs} and C'_{gd}, the dominant extrinsic parasitic capacitances, between 0.5× and 2.5 × of the nominal values shown in Table 3.3. The result for the peak $f_{\mathrm{T,e}}$ of the 7-nm V_{th} and V_{DD} adjusted device can be seen in Fig. 3.8(b), where the *x*-axis is the ratio between a potentially achieved extrinsic parasitic gate capacitance C'_{gg} and the nominal value calculated using the sum of C'_{gs} and C'_{gd} in Table 3.3. As seen from the figure, benefits of the NCFET from mitigating the effects of parasitic capacitances will be more pronounced if the extrinsic parasitic capacitance is large, a result consistent with [28, Fig. 19(b)]. In our tests, NCFETs can provide up to 35% of peak $f_{\mathrm{T,e}}$ improvement if extrinsic parasitic capacitance is high and the extrinsic parasitic resistances are kept at nominal values. In this case, up to 98% of $g_m f_T/I_D$ improvement can also be observed. These enhancements of peak $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ show that an NCFET structure will be more beneficial in mitigating

extrinsic parasitics for RF performance as scaling continues, where extrinsic capacitance from high-density interconnects is expected to increase [57].

3.5 Conclusions

With our key results in Figs. 3.4 – 3.8, the following conclusions can be drawn from this study that investigates the potential for NCFETs to offer improvements to f_T and $g_m f_T/I_D$ by mitigating extrinsic parasitic capacitances:

1. The basic idea of mitigation is to achieve a similar intrinsic cut-off frequency $f_{\mathrm{T,i}}$ with the NCFET, but a higher extrinsic cut-off frequency $f_{\mathrm{T,e}}$, by leveraging a higher intrinsic gate capacitance C_{gg} to mitigate the extrinsic gate capacitance C'_{gg}, as shown via (3.2).

2. The $f_{\mathrm{T,e}}$ and $g_m f_T/I_D$ of an NCFET, the latter calculated using extrinsic quantities, can be improved by up to 20% for $f_{\mathrm{T,e}}$ and up to 80% for $g_m f_T/I_D$ for our 10-nm devices, as shown in Fig. 3.4.

3. The increases of $f_{\mathrm{T,e}}$ in NCFETs is accompanied by a decrease of $f_{\mathrm{T,i}}$, shown in Fig. 3.4, which is a result of the ferroelectric electrostatics near the drain that effectively increases the channel length of NCFETs, as shown in Fig. 3.5. Two ways of alleviating this reduction of $f_{\mathrm{T,i}}$, via channel length scaling, and via adjustments to V_{th} and V_{DD} of the NCFET, were discussed, with results shown in Figs. 3.6.

4. Utilizing 7-nm devices with nominal characteristics shown in Fig. 3.7, we find that higher extrinsic parasitic resistances may decrease the benefits provided by NCFETs, as shown in Fig. 3.8(a), emphasizing the importance of keeping these resistances as low as possible.

5. The performance gain seen in NCFETs is more pronounced as extrinsic parasitic capacitances increase, as shown in Fig. 3.8(b). Hence, the benefits of using NCFETs to increase $f_{\mathrm{T,e}}$ will increase as scaling continues, due to increases in extrinsic parasitic capacitances [57].

Overall, this study demonstrates the potential for NCFETs to bring substantive gain in f_T and $g_m f_T/I_D$ from mitigating the effects of extrinsic parasitic capacitances. As the transistors for RF applications continue to advance, the use of smaller nodes will naturally help to alleviate the issue of $f_{\mathrm{T,i}}$ degradation in NCFETs that might otherwise limit the mitigation. Further, as the field of NCFETs advance, other methods of alleviating the $f_{\mathrm{T,i}}$ reduction (*e.g.*, mobility enhancement [28]) may also emerge. Given the encouraging experimental work done on NCFETs thus far [26], [31], the expected increase of extrinsic parasitic capacitances for future nodes [57] will also enhance the benefits of NCFETs. From these results, this work thus finds promise for NCFET structures in significantly reducing the impact of extrinsic parasitics for next-generation RF applications.

Chapter 4

Toward a GHz-Frequency BEOL Ferroelectric Negative-Capacitance Oscillator with a Wide Tuning Range

4.1 Introduction

Ferroelectric materials have garnered a lot of interest in recent years as they are potentially useful for future nanoelectronic devices such as negative-capacitance FETs (NCFETs) for logic applications [4], [14] and ferroelectric FETs (FeFETs) for memory applications [5].

Thus far, most of the simulations and experiments (*e.g.*, [26], [31], [45], [94], [95]) investigating the use of ferroelectric negative capacitance in such devices have been aimed toward front-end-of-the-line (FEOL) applications, where the ferroelectric would be integrated with a transistor. However, one innate challenge to FEOL applications is the fabrication and *in situ* integration of a high-quality ferroelectric layer into advanced FET architectures.

A possible alternative approach is to use ferroelectrics as standalone back-end-of-the-line (BEOL) elements, where fabrication constraints are comparatively more relaxed. In recent discussions [111], it has been predicted that BEOL implementations of ferroelectrics will be the first to be used in modern integrated circuits.

Toward this end, we have shown in [43] that a BEOL ferroelectric, when used in conjunction with active feedback, has the potential to improve the cut-off frequency of a transistor. As another step toward exploring BEOL ferroelectric applications, we will now explore the use of single-domain, Landau-Khalatnikov (LK) negative capacitance dynamics of a ferroelectric in a tunable oscillator.

While domain formation and dynamics in ferroelectric materials, and how they affect negative capacitance, is still a subject of active research [17], [18], [112], recent theoretical studies utilizing the phase-field model have shown that even if the ferroelectric is intrinsically

multi-domain, the aggregated properties of polarization and electric field can still be consistent with the simple single-domain LK model under low-frequency dynamic excitations [18]. Further, given the relatively relaxed fabrication constraints when the ferroelectric does not need to be integrated into the gate stack of a FET, it is also possible that as fabrication techniques advance, single-domain ferroelectrics could first be realized as BEOL elements, especially given that static crystal structures consistent with a single domain have also been shown in standalone perovskite nanocrystals [113]. As such, even though further work is required to investigate domain dynamics under high frequency, and to investigate the required fabrication techniques that would lead to aggregate behavior describable by single-domain LK dynamics, it is valuable to investigate the potential of such a component for use in future circuits and systems.

In modern radio-frequency communication circuits, a tunable oscillator is essential to mixers, serializer/deserializers, and analog-to-digital converters. Traditionally, these oscillators for RF applications often utilize inductor-based LC circuits to generate the desired periodic waveform. However, since an on-chip, integrated inductor is needed for the circuit, substantial footprint is required for the implementation of the LC oscillator. This substantial footprint can be seen in the die photograph of a 14-nm commercial transceiver in [114, Fig. 15], where each inductor would take approximately $40000\ \mu m^2$ in area. As we will show in this work, the inductor can be replaced by a ferroelectric capacitor less than $50\ \mu m^2$ in area. In addition, with traditional LC oscillators, to cover the large range of oscillation frequencies usually required by RF applications, either multiple oscillators will need to be built [62], or a multi-inductor design will need to be utilized [63], [64], both of which further increase the chip footprint required.

Recently, low-frequency tunable oscillator designs utilizing the hysteretic transfer characteristic of FeFETs [115]–[117], or negative differential output conductance of NCFETs [117] have been proposed for use in neuromorphic applications. For the design in [117], a maximum frequency of 1 GHz was demonstrated in simulations. For the design in [115] and [116], oscillation frequencies in the range of Hz to kHz were demonstrated in simulations [115], and an oscillation frequency in the Hz range was demonstrated in experiment [116].

Furthermore, both these oscillator designs were shown to have oscillation amplitudes in the range of half the supply voltage or less.

Motivated by the potential of using ferroelectrics as BEOL elements, and the importance of exploring novel oscillator designs, a digitally controlled negative-capacitance ferroelectric oscillator (FE-DCO) based on single-domain LK dynamics is proposed and explored in this work. The use of a ferroelectric capacitor instead of an inductor will enable substantial savings in the footprint of the circuit, and as will be discussed in Section 4.4, the proposed oscillator can achieve a much higher tuning range compared to that of an LC oscillator.

Compared to the existing works thus far, the oscillator proposed in this work will utilize the characteristics of a standalone ferroelectric layer rather than one integrated with a FET, which will have the advantage of having more relaxed fabrication constraints compared to the NCFET oscillator proposed in [117], or any FeFET oscillator that aims to integrate a ferroelectric into a FET without any metal layer between the ferroelectric and the dielectric. Furthermore, the oscillator proposed here will be aimed at higher frequency operation of up to 10 GHz and will in principle have a much higher amplitude due to the differential nature of the design.

Throughout the rest of the chapter, the operating principles of this oscillator will be thoroughly explored and basic performance comparisons against a traditional digitally controlled LC oscillator (LC-DCO) will be presented. Overall, the results of this work will be an important step in further motivating the exploration of ferroelectrics as BEOL elements by carefully showing their potential in novel and advantageous circuit designs.

This chapter is organized into four sections. Section 4.2 will describe the topology and basic results of the FE-DCO, Section 4.3 will analyze operating principles of the ferroelectric oscillator and provide insights into design considerations, Section 4.4 will benchmark the ferroelectric oscillator with a standard LC oscillator, and the conclusions will be summarized in Section 4.5.

4.2 FE-DCO Topology and Basic Results

The topology of the proposed FE-DCO follows that of a standard LC oscillator, with a ferroelectric that exhibits negative capacitance as a part of its behavior *directly* replacing the inductor that is usually present in a standard LC-DCO. Typically, a standard LC-DCO consists of an inductor-capacitor resonator that generates oscillation, along with an active circuit in parallel with the resonator exhibiting negative resistance to counteract parasitic losses within the resonator, such that sustained oscillations can be achieved [66, Ch. 8]. To tune the frequency, the capacitive component of the resonator is usually realized with one or more capacitor banks, where the effective capacitance can be modulated by turning on or off switches within the bank [118], [119].

Following an identical topology as a standard CMOS cross-coupled LC oscillator [66, p. 531], the circuit diagram of the proposed FE-DCO can be found in Fig. 4.1(a). In this circuit, the ferroelectric is placed in parallel with a tuning bank of capacitors, between the gate terminals of two cross-coupled transistor pairs that exhibit an effective negative resistance. Much like an LC-DCO, the tuning capacitor bank is used to control the oscillation frequency of the output voltage V_{osc} in the FE-DCO.

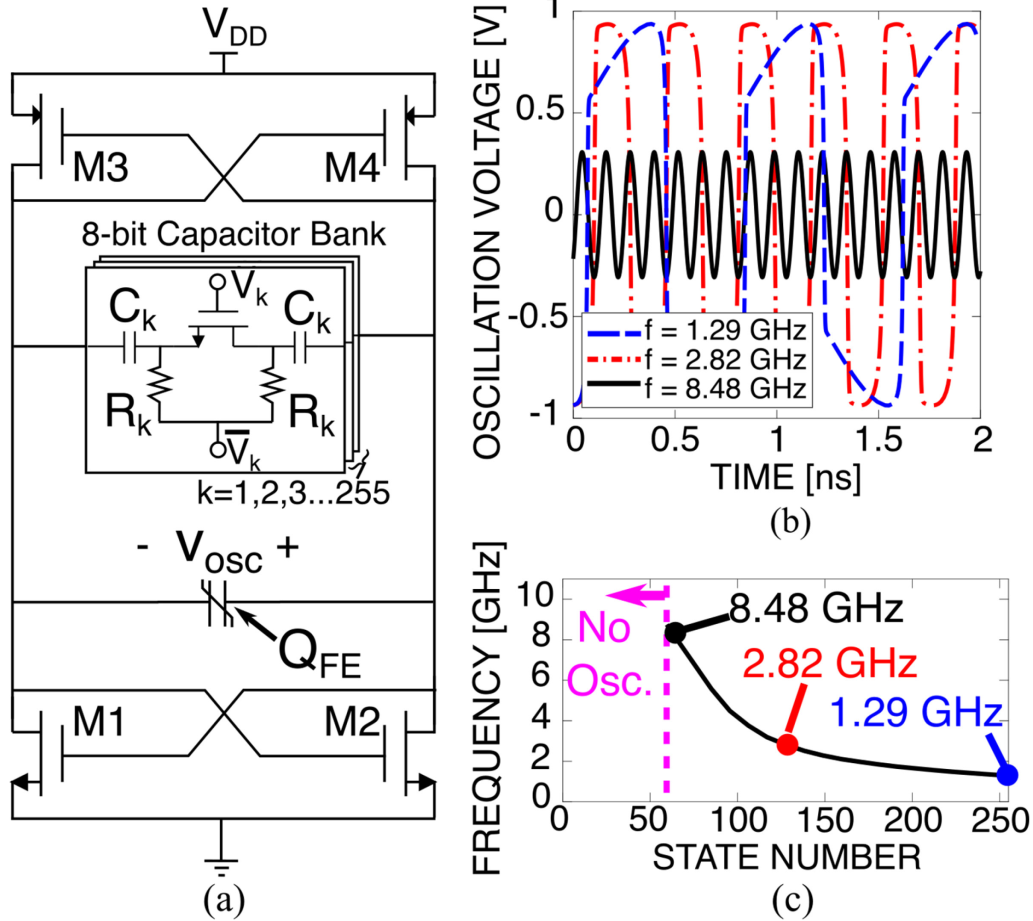


Fig. 4.1 (a) Schematic diagram of the FE-DCO circuit, where the ferroelectric is labeled as a non-linear charge storage device Q_{FE}. (b) Oscillation waveforms at the maximum achievable frequency, minimum achievable frequency, and at the mid-code frequency of 2.82 GHz. (c) Oscillation frequency as a function of the switches turned on, showing oscillation amplitude quickly decays and ceases if less than 61 switches are turned on. The occurrences of the waveforms in (b) are labeled on the tuning curve in (c).

The tuning bank in this work is a standard, 8-bit, thermometer-coded, digitally controlled bank, where all capacitors are controlled via an NMOS transistor acting as a switch, similar to the tuning bank used in [118]. To explore basic characteristics of the FE-DCO in the simplest adequate way, we have considered the voltage sources in this work to be ideal. Furthermore, while only a single tuning bank is considered to demonstrate the basic tuning capabilities of the FE-DCO, more tuning banks can be added to improve the control of the oscillation frequency [119]. All non-ferroelectric components in the circuit are modeled via the Global Foundries 65-nm process development kit (PDK), and important parameters for the circuit can be found in Table 4.1.

Parameter	Value	Parameter	Value
NMOS Gate Length	60 nm	Ferroelectric Thickness t_{FE}	37.7 nm
NMOS Total Gate Width	24 μm	Ferroelectric Area A_{FE}	35.0 $\mu\mathrm{m}^2$
PMOS Gate Length	60 nm	Bank Capacitor C_k	20.2 fF
PMOS Total Gate Width	60 μm	Bank Resistor R_k	36.6 kΩ
LK Parameter α	$-3.6 * 10^8\ \frac{\mathrm{Vm}}{\mathrm{C}}$	Bank NMOS Gate Length	60 nm
LK Parameter β	$2.25 * 10^{10}\ \frac{\mathrm{Vm}^5}{\mathrm{C}^3}$	Bank NMOS Gate Width	18 μm
LK Parameter γ	$1.6 * 10^9\ \frac{\mathrm{Vm}^9}{\mathrm{C}^5}$	Fitting Capacitor C_{tune}	1.82 pF
LK Parameter ρ	1.8 mΩ · m	Fitting Resistor R_N	$-183\ \Omega$

Table 4.1 Circuit parameters.

For the ferroelectric Q_{FE}, a single-domain LK model is utilized [14], as done in [43]. As discussed in Section 4.1, achieving aggregate behavior equivalent to single-domain LK dynamics under low- and high-frequency conditions is an active field of research, but this assumption allows us to explore the potential of ferroelectrics as BEOL elements and motivate further work toward this goal. All parameters associated with the ferroelectric can also be found in Table 4.1, with static LK parameters extracted from [9], and the loss parameter ρ picked according to [55]. Throughout this work, we will also assume that the ferroelectric is initialized in the negative-capacitance region; practically, this can be achieved using an approach similar to that in [43].

Basic oscillation waveforms of the circuit shown in Fig. 4.1(a) can be seen in Fig. 4.1(b). Here, the frequency of the FE-DCO is controlled by changing the number of switches turned on in the capacitor bank, with more switches turned on yielding a lower frequency [Fig. 4.1(c)], much like a traditional LC-DCO. The oscillations shown in Fig. 4.1(b) correspond to the maximum achieved frequency with appreciable amplitude, the mid-code frequency, and the lowest achieved frequency. Here, the mid-code frequency corresponds to the frequency when half the switches in the capacitor bank are turned on. The occurrences of these waveforms are also labeled on the tuning curve in Fig. 4.1(c).

While there are many superficial similarities between the proposed FE-DCO and a standard LC-DCO, it is important to note that there are many intricacies within these basic results that are not expected for a standard LC-DCO. For example, the amplitude changes as frequency changes, and the oscillation stops if too many switches are turned off, as shown in Fig. 4.1(b) and 4.1(c). These phenomena originate from the fact that the ferroelectric is a non-linear capacitor that exhibits negative capacitance as a part of its behavior, which is very different from an inductor. As a result, the underlying oscillation mechanisms of the FE-DCO are very different from an LC-DCO, as the FE-DCO is not a resonator circuit.

Therefore, before comparing the performance of the FE-DCO against an LC-DCO, systematic and careful analysis of the FE-DCO must be conducted to unveil its basic operating principles.

4.3 FE-DCO Analysis

4.3.1 Operating Principles and Oscillation Criteria

4.3.1-A. Basic Oscillator Element

To analyze the FE-DCO in Fig. 4.1(a), the circuit must first be simplified to a basic oscillation element that exhibits the same output waveforms, such as the simplified circuit shown in Fig. 4.2(a), where the tuning capacitor bank and MOSFET gate capacitances are simplified into one ideal capacitor C_{tune}, and the cross-coupled transistor pairs are simplified to a negative resistor R_N, appropriately picked to account for both the transconductance of the transistors and the voltage swing [66, Ch. 8]. In addition, the ferroelectric is broken into a resistive component $R_\rho = \rho t_{\text{FE}}/A_{\text{FE}}$, representing loss within the ferroelectric, and a non-linear ferroelectric capacitor with a stored charge Q_{FE} predicted by lossless Landau theory.

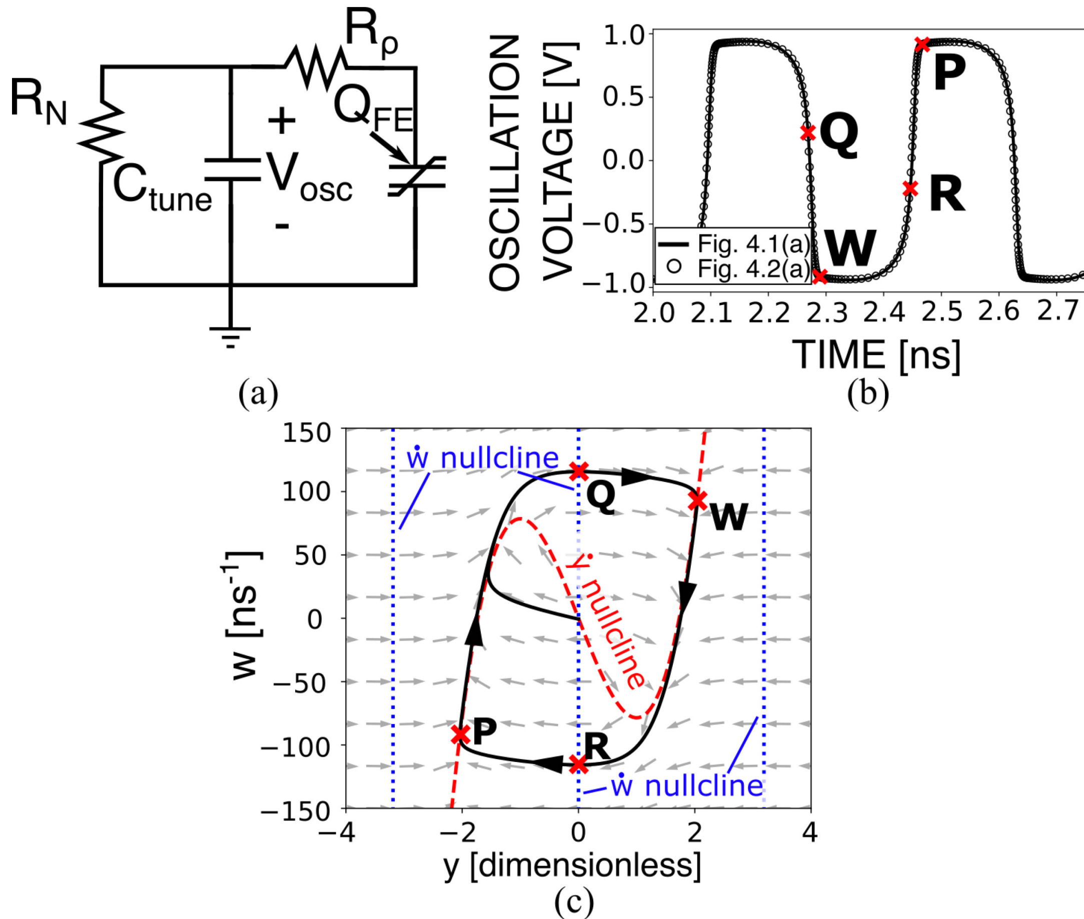


Fig. 4.2 (a) Simplified circuit used to conduct analysis on the FE-DCO. (b) Calibration of the simplified circuit in Fig. 4.2(a) to the FE-DCO circuit in Fig. 4.1(a) for the mid-code oscillation frequency of 2.82 GHz. (c) Phase-space plot for the FE-DCO circuit at 2.82 GHz. The solid black curve shows the phase-space trajectory of the circuit, with the labeled points on the cycle corresponding to the points labeled in (b). Gray arrows illustrate the direction of the phase-velocity field, and the $\dot{y}$ and $\dot{w}$ nullclines are shown with the red dashed and blue dotted lines, respectively.

This simplified circuit can create the same oscillation waveform as the full FE-DCO circuit for a given frequency, as long as the value of the fitting elements C_{tune} and R_N are appropriately selected. For example, a replication of the FE-DCO waveform at mid-code can be seen in Fig. 4.2(b), with the required values of C_{tune} and R_N to match the behavior provided in Table 4.1. In the following subsections, this simplified circuit will be used to establish understanding for the operating principles of the FE-DCO.

4.3.1-B. Phase Space Approach

To analyze the FE-DCO via the simplified circuit in Fig. 4.2(a), we begin by obtaining the differential equations that govern its behavior, which we then analyze using tools from the

field of non-linear dynamics [65]. This approach is necessary since the oscillations of the FE-DCO stem from the highly non-linear nature of the ferroelectric.

The dynamics of the charges Q_{tune} and Q_{FE} can be described by the following equations obtained via elementary circuit analysis:

$$\dot{Q}_{\mathrm{tune}} = -\left(\frac{R_N+R_\rho}{R_N R_\rho C_{\mathrm{tune}}}\right) Q_{\mathrm{tune}} + \frac{2\alpha t_{\mathrm{FE}}}{A_{\mathrm{FE}} R_\rho} Q_{\mathrm{FE}} + \frac{4\beta t_{\mathrm{FE}}}{A_{\mathrm{FE}}^3 R_\rho} Q_{\mathrm{FE}}^3 \tag{4.1}$$

$$\dot{Q}_{\mathrm{FE}} = \frac{1}{R_\rho C_{\mathrm{tune}}} Q_{\mathrm{tune}} - \frac{2\alpha t_{\mathrm{FE}}}{A_{\mathrm{FE}} R_\rho} Q_{\mathrm{FE}} - \frac{4\beta t_{\mathrm{FE}}}{A_{\mathrm{FE}}^3 R_\rho} Q_{\mathrm{FE}}^3 \tag{4.2}$$

where the dots above the variables on the left of (4.1) and (4.2) are used to denote time derivatives. All the other variables have been defined in Table 4.1 and in the circuit diagram in Fig. 4.2(a).

In deriving (4.1) and (4.2), the term quintic in Q_{FE} from the LK model, as well as any non-linearity within the negative resistor R_N, has been neglected. The quintic term from the LK equation does not appreciably change the behavior of the circuit. The non-linearity in R_N will have important higher order effects, which will be discussed in Section 4.3.2-A 4).

To develop further understanding of (4.1) and (4.2), we perform algebraic manipulation and a change of variables. This process yields the following pair of differential equations, written in terms of a pair of abstract variables y and w, which are linearly related to the charges on the ferroelectric and tuning capacitor:

$$\dot{w} = -k^2 b y + b y^3 \tag{4.3}$$

$$\dot{y} = w + a y - \frac{1}{3} a y^3 \tag{4.4}$$

where

$$w = 2\sqrt{\frac{3\beta t_{\mathrm{FE}}}{A_{\mathrm{FE}}^3 R_\rho^3 C_{\mathrm{tune}}^2 a}} \left[Q_{\mathrm{tune}} + \left(\frac{R_N+R_\rho}{R_N}\right) Q_{\mathrm{FE}}\right] \tag{4.5}$$

$$y = \left(2\sqrt{\frac{3\beta t_{\mathrm{FE}}}{A_{\mathrm{FE}}^3 R_\rho a}}\right) Q_{\mathrm{FE}} \tag{4.6}$$

$$a = \frac{1}{\tau_{\text{FE}}} - \frac{1}{\tau_{\text{tune}}} \tag{4.7}$$

$$b = -\frac{a}{3R_N C_{\text{tune}}} \tag{4.8}$$

$$k = \sqrt{\frac{3}{\tau_{\text{FE}} a}} \tag{4.9}$$

and where τ_{FE} and τ_{tune} are time constants introduced solely to simplify the equations, given by

$$\tau_{\text{FE}} = R_\rho \frac{A_{\text{FE}}}{2|\alpha| t_{\text{FE}}} = R_\rho |C_{\text{N}}| \tag{4.10}$$

$$\tau_{\text{tune}} = \left(\frac{R_N R_\rho}{R_N + R_\rho}\right) C_{\text{tune}} \tag{4.11}$$

In (4.10) and (4.11), $C_{\text{N}} = A_{\text{FE}}/2\alpha t_{\text{FE}}$ represents the magnitude of the linear negative capacitance of the ferroelectric near the center of the S-shaped curve predicted by the Landau theory. It can be shown that (4.3) and (4.4) are the equations of an unforced van der Pol (VdP) Duffing oscillator [120].

To analyze the basic oscillating element of the FE-DCO using these equations, we consider a y-w plane, which we call phase space [65, Ch. 6], and plot values of y and w within this space. Since a pair of Q_{FE} and Q_{tune} corresponds to a unique pair of y and w, a point in phase space corresponds to a particular state of the oscillator circuit. As such, the time evolution of $Q_{\text{FE}}(t)$ and $Q_{\text{tune}}(t)$, the latter of which is directly proportional to the time evolution of the output voltage, traces out a parametric curve of $y(t)$ and $w(t)$, hereafter called a trajectory, in phase space. The phase-space trajectory corresponding to the voltage waveform shown in Fig. 4.2(b) can be found in Fig. 4.2(c), with reference points of the cycle marked on both figures.

To further guide our understanding of the dynamics of the system, we also plot on Fig. 4.2(c) the normalized time derivatives of y and w, *i.e.*, $\dot{y}(y, w)$ and $\dot{w}(y, w)$, as a vector field called the phase velocity. This phase velocity is represented by the gray arrows in Fig. 4.2(c) and will aid the analysis because the phase-space trajectory, and correspondingly the evolution of Q_{FE} and Q_{tune}, is dictated by the phase velocity.

Finally, to help obtain a set of oscillation criteria, we also plot the curves corresponding to $\dot{y} = 0$ or $\dot{w} = 0$, known as nullclines, which are the red dashed and blue dotted lines in Fig. 4.2(c). These nullclines show where the w or y phase velocity is zero, and act as boundaries where the components of the phase velocity change direction. In the next two subsections, the $\dot{y}$ and $\dot{w}$ nullclines will be discussed, and the oscillation criteria of the FE-DCO will be derived using these nullclines.

4.3.1-C. $\dot{y}$ Nullcline and First Oscillation Criterion

We begin by observing the $\dot{y}$ nullcline by setting the left side of (4.4) to zero, obtaining

$$w = -ay + \frac{1}{3}ay^3 \quad (4.12)$$

which is a cubic curve that splits phase space into two regions and is shown by the red dashed line in Fig. 4.2(c). For w values lying above the $\dot{y}$ nullcline the phase velocity will have a positive y-component, and the opposite is true for w values lying below the $\dot{y}$ nullcline.

It can be shown using (4.12), and it is well known within the literature on van der Pol oscillators [65, Ch. 7], that the coefficient a must be positive for autonomous oscillation to occur. Then, recalling that $R_N < 0$, and noting we expect $|R_N| \gg R_\rho$ given the cross-coupled pair is expected to introduce a relatively small amount of positive feedback, the latter equivalent to a large $|R_N|$, we conclude using (4.11) that $\tau_{\text{tune}} > 0$. Finally, using $a > 0$, $\tau_{\text{tune}} > 0$, and (4.7), one obtains the following criterion that needs to be satisfied for oscillations to occur in the FE-DCO:

$$\frac{\tau_{\text{FE}}}{\tau_{\text{tune}}} < 1 \quad (4.13)$$

or, equivalently, $C_{\text{N}} + C_{\text{tune}} > 0$. By examining the circuit in Fig. 4.2(a) in the context of large $|R_N|$ and small R_ρ, this condition is equivalent to stating that the resulting RC time constant $R_\rho[C_N C_{\text{tune}}/(C_N + C_{\text{tune}})]$ of the circuit must be negative, *i.e.*, the circuit must not be linearly stable. Therefore, (4.13) is akin to the classical oscillator startup condition, known as Barkhausen's criterion, where oscillations can only occur within unstable feedback systems that have sufficient gain [66, Ch. 8].

4.3.1-D. $\dot{w}$ Nullclines and Second Oscillation Criterion

4.3.1-D 1) Location of nullclines:

We next consider the $\dot{w}$ nullclines, obtained via setting the left side of (4.3) to zero:

$$y = 0, \pm k \tag{4.14}$$

which are lines that separate phase space into four regions, *e.g.*, as illustrated (using values from Table 4.1) by the blue dotted lines in Fig. 4.2(c). Furthermore, when $a > 0$, the polarity of $\dot{w}$ throughout phase space around these nullclines is as follows:

$$\{y < -k \text{ or } 0 < y < k\} \Rightarrow \dot{w} < 0 \tag{4.15}$$

$$\{y > k \text{ or } -k < y < 0\} \Rightarrow \dot{w} > 0 \tag{4.16}$$

which we will use further below in conjunction with Fig. 4.3.

4.3.1-D 2) Approach:

Using information regarding the polarity of $\dot{w}$ from (4.15) and (4.16), along with information regarding the polarity of $\dot{y}$ discussed in the previous subsection, a second criterion for oscillation can be obtained by examining whether a cyclic phase-space trajectory, known as a limit cycle [65, Ch. 7], exists for a given placement of the $\dot{w}$ nullclines, with that placement determined by the value of the parameter k according to (4.14). The existence of a limit cycle would correspond to oscillatory behavior, as the phase-space trajectory corresponds to a cyclic trajectory of charge states ($Q_{\mathrm{FE}}, Q_{\mathrm{tune}}$) in the system, as discussed Section 4.3.1-B.

4.3.1-D 3) Analysis in the limit of large C_{tune}:

We will first consider the limit of large C_{tune}, corresponding to many switches turned on in the capacitor bank, which can be shown via (4.7) – (4.11) to correspond to a limit of $a \gg b, k$. In this case, the phase-space trajectory can be easily predicted.

When $a \gg b, k$, by subtraction of (4.3) and (4.4), we can conclude that $\dot{w} \ll \dot{y}$ for all $\dot{y} \neq 0$, *i.e.*, the w (vertical) component of the phase velocity is negligible in comparison to the y (horizontal) component for all points that do not lie directly on the $\dot{y}$ nullcline. The resulting velocity vectors are illustrated by the gray arrows shown in both parts of Fig. 4.3. While

negligible in comparison to $\dot{y}$, both parts of Fig. 4.3 also indicate (via blue bolded arrows) the *polarity* of $\dot{w}$ between the $\dot{w}$ nullclines as indicated by (4.15) and (4.16).

We now consider two cases based on the value of the parameter k in (4.9), where $k = 2$ serves as a key delineation point irrespective of circuit parameters when $a \gg b, k$.

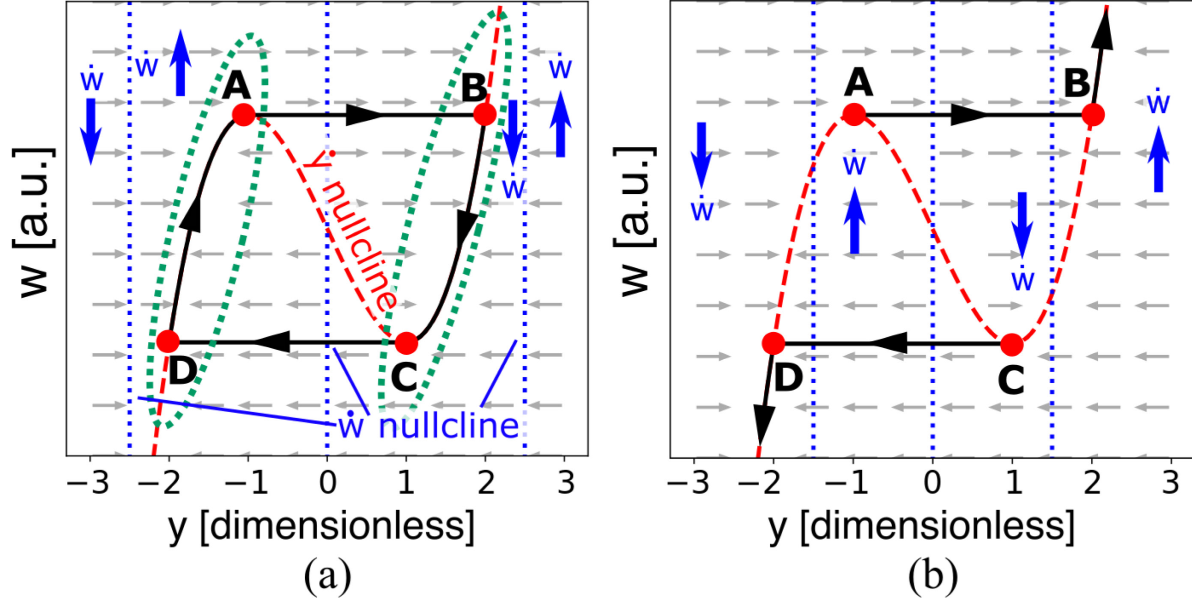


Fig. 4.3 Phase-space plot for the theoretical $a \gg b, k$ limit for two different scenarios: (a) $k > 2$, a limit cycle ABCD is observed, and oscillation occurs. (b) $k < 2$, no limit cycle is observed and the system diverges.

For $k > 2$, we obtain Fig. 4.3(a), with the $\dot{w}$ nullclines situated at $y = 0$ and outside the region $-2 < y < 2$, as stipulated by (4.14). In this case, the system has a stable limit cycle between points A, B, C, and D. Between D and A, or between B and C, the trajectory evolves qualitatively up or down, respectively, directly on the $\dot{y}$ nullcline; intuitively, this occurs because the phase velocity arrows converge directly on the $\dot{y}$ nullcline, as indicated within the circled regions of Fig. 4.3(a). Whenever the trajectory reaches A or C, the phase velocity will induce a transition horizontally in phase space, directly to B or D, respectively, as shown by the vectors in Fig. 4.3(a).

For $k < 2$, we obtain the situation in Fig. 4.3(b), with the $\dot{w}$ nullclines situated at $y = 0$ and to the *inside* of $-2 < y < 2$, according to (4.14). In this case, the system does not have a stable limit cycle, and instead will diverge to infinity along the $\dot{y}$ nullcline once it reaches point B or point D, as shown in Fig. 4.3(b). Using B as an example, the divergence occurs because

B now lies in a region where $\dot{w} > 0$, causing evolution upward along the $\dot{y}$ nullcline, instead of downward toward C; a similar situation exists at D.

4.3.1-D 4) Oscillation criterion in the limit of large C_{tune}:

We hence conclude that for large C_{tune}, *i.e.*, when $a \gg b, k$, the system must satisfy $k > 2$ for stable oscillations to occur. Using $k > 2$ in conjunction with (4.7) and (4.9), we obtain the following inequality, which is a lower bound on $\tau_{\mathrm{FE}}/\tau_{\mathrm{tune}}$:

$$\frac{\tau_{\mathrm{FE}}}{\tau_{\mathrm{tune}}} > \frac{1}{4} \tag{4.17}$$

4.3.1-D 5) Generalization:

When the value of C_{tune} is small, the system will not be within the $a \gg b, k$ limit, in which case it may not exhibit oscillations even if (4.17) is satisfied. This situation occurs because the phase velocity in the w direction can be non-negligible, as seen in Fig. 4.2(c), in contrast to the velocities in Fig. 4.3. This means the simple analysis using Fig. 4.3 and leading to (4.17) must be modified. Numerically, we have found that the requirement $k > 2$ for oscillation must be slightly modified to $k > 2.236 \approx \sqrt{5}$ to be valid for any value of $a > 0$, and is a sufficient condition for a general limit cycle. Such a cycle is shown in Fig. 4.2(c), which retains many of the qualitative features of that shown in Fig. 4.3(a). Using $k > \sqrt{5}$ with (4.7) and (4.9), the result (4.17) can then be generalized to read

$$\frac{\tau_{\mathrm{FE}}}{\tau_{\mathrm{tune}}} > \frac{2}{5} \tag{4.18}$$

4.3.1-E. Overall Oscillation Criterion

Combining (4.18) with the earlier condition (4.13) yields the overall oscillation criterion:

$$\frac{2}{5} < \left|\frac{\tau_{\mathrm{FE}}}{\tau_{\mathrm{tune}}}\right| < 1 \tag{4.19}$$

The upper bound in (4.19) signifies that circuit parameters must be chosen such that the system is linearly unstable, as discussed in conjunction with (4.13), and the lower bound signifies that the circuit parameters must be chosen such that the voltage can be *bounded* and

turned around, leading to *oscillatory behavior*, instead of *divergent behavior*, *i.e.*, to a limit cycle as discussed leading to (4.18).

4.3.1-F. Start-up Considerations

It is worth clarifying startup conditions in relation to (4.19). It was mentioned while introducing Fig. 4.1(a) in Section 4.2 that a startup circuit similar to that in [43] can be used to put the ferroelectric into its negative-capacitance region, *e.g.*, with $Q_{\mathrm{FE}} = 0$; it is sufficient to also have $Q_{\mathrm{tune}} = 0$, starting the system at the origin of phase space to achieve oscillation. This type of trajectory is shown in Fig. 4.2(c) and the same startup is also applicable to the trajectory shown in Fig. 4.3(a). When (4.19) is not satisfied, it can be shown that oscillation will not occur irrespective of the startup location in phase space.

4.3.2 Oscillation Design Considerations

4.3.2-A. Amplitude Control

4.3.2-A 1) Expression for amplitude:

From Fig. 4.2(a), the oscillation voltage is $V_{\mathrm{osc}}(t) = Q_{\mathrm{tune}}(t)/C_{\mathrm{tune}}$, which with (4.5) and (4.6) is

$$V_{\mathrm{osc}}(t) = \frac{1}{2}\rho t_{\mathrm{FE}}\sqrt{\frac{\rho a}{3\beta}}\left[w(t) - \frac{y(t)}{R_\rho C_{\mathrm{tune}}}\right] \tag{4.20}$$

The amplitude of oscillation can be found by maximizing (4.20) over one cycle. This maximum can be found by setting the time derivative of $w(t) - y(t)/R_\rho C_{\mathrm{tune}}$ to zero, which in turn yields a required slope in phase space, $dw/dy = 1/R_\rho C_{\mathrm{tune}}$.

4.3.2-A 2) Saturated amplitude:

Empirically, we observe that as C_{tune} increases, the frequency steadily decreases but the amplitude quickly saturates, and remains constant for a large range of C_{tune}. Given this behavior, an expression for this saturated amplitude will be developed in the limiting case of large C_{tune}, *i.e.*, low frequency.

In the case of large C_{tune}, the trajectory in phase space is exactly as shown in Fig. 4.3(a). Notably, the only regions with a non-zero dw/dy occur between points A and D, and between points B and C; the trajectory in these regions is expressed via (4.12). By finding the values of w and y in (4.12) where $dw/dy = 1/R_\rho C_{\text{tune}}$ and substituting them into (4.20), the saturated amplitude of oscillation is found as

$$V_{\max} = E_C t_{\text{FE}} = V_c \tag{4.21}$$

where we have applied (4.7), (4.10), and (4.11), along with $E_c = 4/3 \times \sqrt{-\alpha^3/6\beta}$, which is the coercive field of the ferroelectric [106], to simplify the final expression. V_c is the coercive voltage of the ferroelectric.

Utilizing values in Table 4.1, (4.21) yields the $V_{\max}$ to be 0.93 V, which is exactly the value observed in the 2.82 GHz and 1.29 GHz case in Fig. 4.1(b), showing that (4.21) is accurate. The amplitude decay observed for the 8.75 GHz case will be discussed in the subsequent section.

Intuitively, the simplified result in (4.21) is not unexpected, as the ferroelectric is the only non-linear element in the circuit shown in Fig. 4.2(a), and V_c is directly related to how this non-linearity would transition from a negative to positive capacitance according to the Landau theory; this is much like how non-linear behavior of the FETs limits the amplitude of a classical LC oscillator [66, Ch. 8].

In practice, (4.21) means that by increasing the coercive voltage of the ferroelectric, which can be done by either increasing the coercive field or increasing the thickness of the ferroelectric, a higher oscillation amplitude can be achieved. While increasing the thickness t_{FE} would be the easiest way, it must be done carefully so as not to violate the oscillation criteria set out by (4.19); one way is to simply increase the area and thickness by the same factor, which will ensure that (4.19) remains satisfied while thickness is increased.

4.3.2-A 3) Amplitude decay at high frequency:

In addition to the simple relationship in (4.21), one further important observation is the decay of amplitude as frequency increases. This decay can be seen by comparing the amplitude

of the 1.29 GHz case in Fig. 4.1(b), which is near 1 V, to the 8.48 GHz case in the same figure, which is only around 300 mV. As will be discussed below, this phenomenon can be explained via (4.20).

To relate frequency to (4.20), we first relate frequency and the abstract variable a, which is in turn related to C_{tune}. As seen from Fig. 4.1(c), the frequency of oscillation increases as C_{tune} decreases. However, as C_{tune} decreases, τ_{tune} decreases according to (4.11), causing the second term in (4.7) to increase, which causes a to decrease.

Given that $V_{\text{osc}}(t)$ in (4.20) is proportional to $\sqrt{a}$, the analysis thus far shows that as frequency increases, oscillation amplitude will approach zero if the term in the square brackets of (4.20) is bounded.

Results from the non-linear dynamics literature [120, eq. 5] show that $y(t)$ will approach a bounded sinusoid in the case of a approaching zero, which corresponds to $w(t)$ also being bounded via algebraic manipulation of (4.4). Since both $y(t)$ and $w(t)$ are bounded, (4.20) approaches zero as a approaches zero, which explains the decrease in amplitude as frequency increases.

From a design perspective, the qualitative observations above mean that the amplitude decay could be alleviated if other parameters in the leading factor of (4.20) can be picked to offset the effects of vanishing a. To not violate the oscillation criteria of (4.19) while doing so, the most effective way is to pick a ferroelectric material with lower β, since (4.20) is proportional to $1/\sqrt{\beta}$, while not changing the other ferroelectric parameters. Since β is proportional to E_c/P_r^3, whereas a specified by (4.7), (4.10), and (4.11) depends on the ferroelectric parameter α and hence E_c/P_r [106], this requirement can be achieved by picking a ferroelectric with simultaneously higher coercive field E_c and remnant polarization P_r.

4.3.2-A 4) Effect of non-linear R_N:

Thus far, the discussion of amplitude has been based on the simplified circuit shown in Fig. 4.2(a), where the negative resistance generated by the cross-coupled MOSFETs is assumed to be linear. In practice, as voltage swing increases, the MOSFETs could enter the triode region,

where the generated negative resistance becomes non-linear. The analysis with non-linear R_N is involved, and we note only that it serves as an additional limiter for amplitude and will cause oscillations to cease by disrupting the phase-space trajectory if the amplitude becomes too high.

4.3.2-B. Frequency Control

4.3.2-B 1) Expression for frequency:

In general, the exact frequency behavior of the FE-DCO as a function of the circuit parameters is difficult to predict analytically, because it would require an analytical solution to the coupled differential equations (4.1) and (4.2). However, for purposes related to the design of the FE-DCO, the analysis of frequency can be simplified, and a few important predictions can be made.

Through simulations, we have observed that as C_{tune} increases, the frequency of oscillation decreases, and the output waveform changes from near-harmonic oscillation to an extremely anharmonic oscillation, as shown in Fig. 4.1(b). Intuitively, the general trend of frequency decreasing when capacitance is increased is not surprising, as an increase of C_{tune} will increase the effective time constant of the circuit in Fig. 4.2(a), making $V_{\text{osc}}(t)$ slower to respond.

While quantitative prediction of the oscillation frequency as a function of C_{tune} in general is difficult, techniques from the literature on non-linear dynamics can be applied to predict the frequency as a function of C_{tune} for small C_{tune}, and equivalently, corresponding to the high-frequency limit [120]. By performing algebraic manipulation of [120, eq. 6(a)], it can be shown that the frequency in this limit is

$$2\pi f = \frac{1}{|R_{\text{N0}}|C_{\text{tune}}}\sqrt{\left|\frac{R_{\text{N0}}+R_\rho}{R_\rho}\right|} \tag{4.22}$$

where

$$\frac{1}{R_{\text{N0}}} = -\left(\frac{g_{\text{m,n}}}{2}+\frac{g_{\text{m,p}}}{2}\right) \tag{4.23}$$

is the value of R_N to be used this limit and is the well-known equivalent resistance of the cross-coupled pair when the amplitude of oscillation is small [66, Ch. 8]. In (4.23), $g_{\text{m,n}}$ and $g_{\text{m,p}}$ are the transconductances of the NMOS and PMOS transistors at the dc bias point, respectively.

4.3.2-B 2) Maximum frequency:

Using (4.22), the maximum frequency of oscillation for the FE-DCO can be derived. First, note that a maximum frequency exists because oscillation stops below a minimum value of C_{tune} as dictated by the upper bound of (4.19). The maximum frequency of oscillation $f_{\max}$ can then be found by substituting an expression for this minimum C_{tune} found from the upper bound of (4.19), into (4.22):

$$2\pi f_{\max} = \sqrt{\frac{1}{|(R_{N0}+R_\rho)R_\rho C_{\text{N}}^2|}} \tag{4.24}$$

Here, it is important to point out that even though (4.24) represents the theoretical maximum frequency of oscillation, the amplitude at $f_{\max}$ will be zero due to the abstract variable a, which affects amplitude as previously discussed, vanishing in this limit. As such, the maximum frequency achieved with appreciable amplitude will be lower than that of $f_{\max}$. The accuracy of (4.24) will be examined in more detail in the next section.

Beyond the amplitude concerns which occur at high frequencies, which were discussed in the previous section, one additional design challenge in tuning the frequency of the FE-DCO is that the frequency will be very sensitive near $f_{\max}$, which arises from the reciprocal relationship between frequency and C_{tune}, as shown in (4.22). This sensitivity means that it will be more difficult to precisely tune the FE-DCO frequency near $f_{\max}$ compared to a lower frequency. To mitigate this sensitivity, fine-tuning capacitor banks, like those used in traditional LC-DCOs, could be utilized to improve the precision of C_{tune} [119].

4.4 FE-DCO Benchmark

4.4.1 Benchmark LC-DCO Design

To benchmark the FE-DCO described in the previous sections, an equivalent traditional LC-DCO is constructed with an identical circuit topology and capacitor bank. In the LC-DCO, the ferroelectric in Fig. 4.1(a) is replaced by an inductor, and the FET width of the LC-DCO is increased by 1.6 × compared to values in Table 4.1 such that similar power consumption is achieved at the mid-code frequency of 2.8 GHz. The inductor used is a two-turn inductor with a line width of 10 µm, and outer diameter of 250 µm, and an inductance of 1.67 nH. At the

mid-code frequency, the average power consumption of the FE-DCO and the LC-DCO is 6.5 mW and 6.7 mW, respectively. At this oscillation frequency, the FE-DCO has comparable amplitude to the LC-DCO, and a comparison of oscillation waveforms can be found in Fig. 4.4(a).

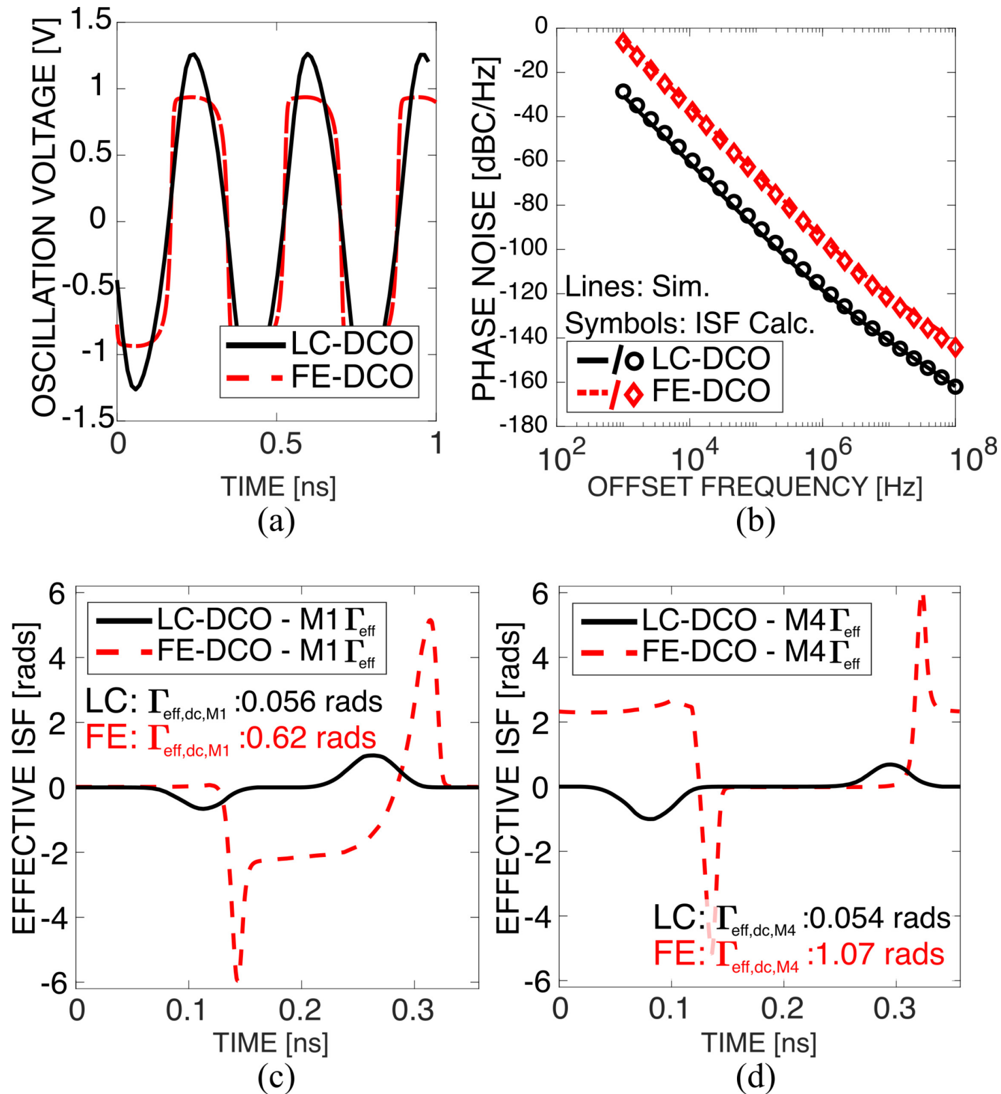


Fig. 4.4 Benchmark of the FE-DCO vs. a traditional LC-DCO. (a) Time-domain results for an oscillation frequency of 2.8 GHz. (b) Phase noise results for an oscillation frequency of 2.8 GHz, where the solid lines represent simulated results, and the symbols represents calculated results from the ISF method. Parts (c) and (d) show the effective impulse sensitivity function Γ_{eff} for the (c) NMOS (M1) and (d) PMOS (M4) of the FE-DCO and LC-DCO.

4.4.2 Comparison With LC Oscillator

4.4.2-A. Phase Noise

In modern RF applications, one important performance criterion for oscillators is phase noise. In Fig. 4.4(b), the phase noise of the FE-DCO vs. the LC-DCO can be seen for the mid-code frequency of 2.8 GHz.

As seen from Fig. 4.4(b), the phase noise of the FE-DCO is around 20–25 dB worse than that of the LC-DCO, consistent across a large range of offset frequencies from the oscillation frequency. This result is consistent with the widely accepted result that relaxation oscillators, such as the one proposed here, generally have worse noise performance compared to LC oscillators [121]–[123].

To further confirm this observation, the well-known impulse sensitivity function (ISF) approach, detailed in [122], [124], is used to estimate the phase noise of the FE-DCO and the LC-DCO. The calculated noise found using this approach is within 2 dB of the simulated noise, as seen from the symbols in Fig. 4.4(b).

In the ISF approach, the flicker noise contribution from the MOSFETs to the overall phase noise, which is most of the observed phase noise, is characterized by a quantity known as the effective ISF, Γ_{eff}. This quantity characterizes how sensitive a particular oscillator topology is to noise, with the phase noise proportional to $\Gamma_{\mathrm{eff,dc}}^2$, which is the dc component of Γ_{eff} [124].

The calculated values of Γ_{eff} for the NMOS transistor M1 and PMOS transistor M4 for both the FE-DCO and LC-DCO are shown in Fig. 4.4(c) and (d), respectively. As seen from the figure, the Γ_{eff} for both the NMOS and PMOS transistors are higher in the FE-DCO compared to that of the LC-DCO, showing that the FE-DCO should indeed be more sensitive to noise.

Overall, while the FE-DCO exhibits worse phase noise performance compared to that of the LC-DCO, its significantly smaller footprint, evident by comparing the area of the spiral inductor, which is estimated to be 49087 $\mu\mathrm{m}^2$ using its diameter, to the area of the ferroelectric used, which is only 35.0 $\mu\mathrm{m}^2$, could give it significant advantages in applications where the phase noise requirement is less stringent. For applications where phase noise is critical, further work will be required to optimize the FE-DCO to improve the phase noise.

4.4.2-B. Tuning Range

In addition to noise, another important performance criterion for oscillators in modern applications is tuning range. A tuning curve comparison of multiple FE-DCOs, each with a different ferroelectric area, and the LC-DCO can be seen in Fig. 4.5(a), with oscillation frequency plotted as a function of the bits turned on in the capacitor bank. The exact design shown in Fig. 4.1(a), with parameters listed in Table 4.1 and labeled as 1 × area, will first be compared against the LC-DCO. Observation relating to other area multipliers will be discussed later.

4.4.2-B 1) Comparison of tuning range:

As seen from Fig. 4.5(a), the LC-DCO has a tuning range of 50%, consistent with a similar single-inductor design presented in [118]. On the other hand, the FE-DCO has a tuning range of up to 149%, from 1.29 to 8.75 GHz. Compared to more complex, multi-inductor LC oscillators such as the one presented in [63], the FE-DCO can cover a much higher range of oscillation frequencies.

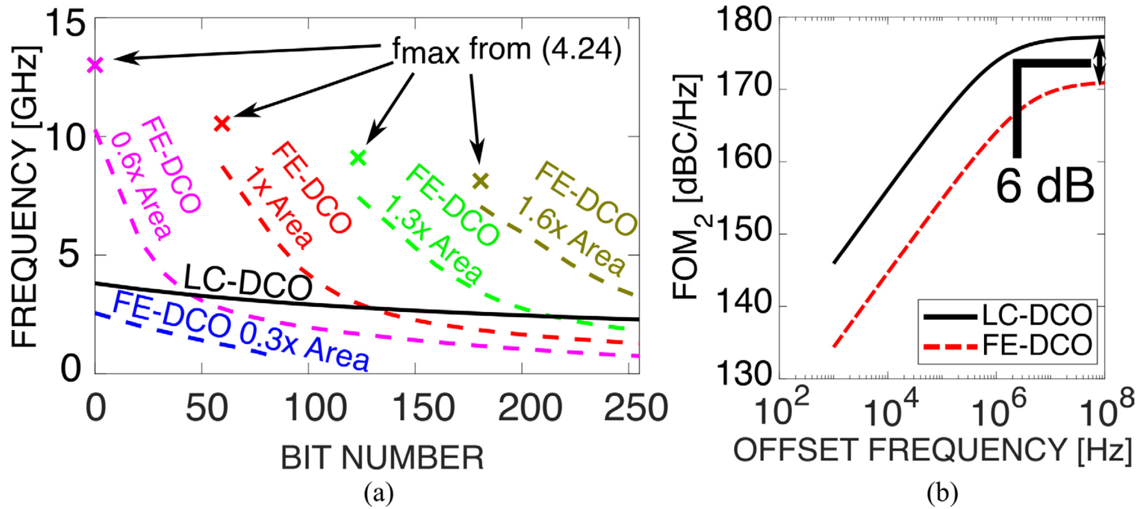


Fig. 4.5 (a) Tuning range the FE-DCO with various ferroelectric areas and the LC-DCO as a function of capacitor bank bit number. Curves are cut off if the system does not oscillate. The 1 × area line is the same line as Fig. 4.1(c). The symbols mark the $f_{\max}$ estimated from (4.24). (b) FOM_2 of the FE-DCO and LC-DCO for an oscillation frequency of 2.8 GHz.

Given this result, the extremely wide tuning range gives the FE-DCO a distinct advantage over traditional LC-DCOs for applications that require a broad range of frequencies, at the cost of worse phase noise. To evaluate this trade-off in more detail, we have calculated the figure

of merit FOM_2, for the LC-DCO and FE-DCO at the mid-code frequency of 2.8 GHz. This figure of merit is calculated as

$$\text{FOM}_2 = \frac{(\text{Oscillation Frequency})^2}{\text{Power [mW]}\times\text{Phase Noise}\times\text{Offset Frequency}} \times \left[\frac{\text{Max Frequency}-\text{Min Frequency}}{\text{Oscillation Frequency}}\right]^2 \quad (4.25)$$

and considers the noise, power, and tuning range of an oscillator together for an overall evaluation of oscillator performance [66, Ch. 8]. The results are plotted in Fig. 4.5(b), and the FOM_2 of the FE-DCO and LC-DCO are only about 6 dB apart, which indicates that they have similar overall performance. This similarity makes the FE-DCO design proposed here an attractive alternative for traditional LC-DCOs, especially considering the vastly smaller area of the FE-DCO achieved via an inductor-less design.

4.4.2-B 2) Tuning behavior with different A_{FE}:

In Fig. 4.5(a), the tuning curves of FE-DCO designs with different ferroelectric areas are shown. For each design, all parameters are identical to Table 4.1 except for the ferroelectric area A_{FE}, which is modified as indicated in the figure. As seen from Fig. 4.5(a), the tuning curve is shifted when the ferroelectric area is changed, with each tuning curve cutting off at different numbers of bits due to a violation of (4.19). The f_{max} estimated using (4.24) is also plotted in Fig. 4.5(a) and is around 25% higher than the maximum frequencies achieved in simulations, showing that (4.24) provides a reasonable first estimate of the upper frequency bound.

When multiple ferroelectrics with different areas are used, the total tuning range increases, as each oscillator can cover a different range of frequencies, as shown in Fig. 4.5(a). In this case, a total tuning range of 174%, from 0.7 – 10.3 GHz can be achieved. Furthermore, we have observed that the tuning curve becomes flatter when a ferroelectric with a larger area is used, which could point to a way to alleviate the potential high sensitivity of the oscillation frequency to capacitance. Overall, this result suggests that further performance improvements can be attained if multiple FE-DCOs are to be built and utilized for a given circuit, much like how multiple LC oscillators can be utilized in standard circuits [62]. This application avenue is especially attractive as the area consumed by multiple FE-DCOs is still considerably smaller compared to even a single LC-DCO.

4.5 Conclusions

In this work, we proposed and investigated a novel negative-capacitance ferroelectric oscillator (FE-DCO) design that utilizes the single-domain dynamics predicted by the Landau theory. Through detailed simulations and analysis, the following conclusions can be made:

1. Tuned oscillations can be achieved with a ferroelectric using the circuit shown in Fig. 4.1(a). The frequency can be tuned by tuning the capacitors in the bank, much like a traditional LC-DCO, as shown in Fig. 4.1(b).

2. The operating principles of the FE-DCO can be described using a simplified circuit and the phase-space approach. A criterion for oscillation is provided by (4.19).

3. Control of the amplitude and frequency of the FE-DCO is investigated analytically. It was found that amplitude can be directly controlled by the ferroelectric coercive voltage, per (4.21). Frequency control is also analyzed and an expression for maximum oscillation frequency is in (4.24). Both formulas are useful in estimating the performance of the FE-DCO.

4. The FE-DCO exhibits an extremely high tuning range of 149% vs. 50% for the LC-DCO, as shown in Fig. 4.5(a). Even though the phase noise performance of the FE-DCO is worse, when the overall performance is considered using a single metric FOM_2 [66, Ch. 8], the FE-DCO shows similar performance to that of the LC-DCO, as shown in Fig. 4.5(b).

Combined with the advantage of a vastly smaller area, the FE-DCO proposed in this work is hence shown to be a promising alternative to the traditional LC-DCO. Even though further studies in the broader field of ferroelectric negative capacitance are required to ensure that the proposed design can be reliably implemented in experiment, including work probing the high-frequency behavior of ferroelectric domains and identifying materials that can provide aggregate single-domain dynamics under high-speed switching, this work shows the strong potential of exploiting negative capacitance from ferroelectrics as BEOL elements, as recently suggested [111], and thus provides continuing motivation for their ongoing exploration beyond NCFETs in future circuits and systems.

Chapter 5

Conclusions and Future Work

5.1 Summary of Contributions

In this chapter, the specific conclusions from each stage of the Ph.D. research are presented, with work leading up to these conclusions detailed in the previous chapters and summarized in Chapter 1.

5.1.1 Stage 1 (Chapter 2)

The specific contributions from this stage, "RF Performance Projections of Negative-Capacitance FETs: f_T, $f_{\max}$, and $g_m f_T/I_D$," are as follows:

1. The f_T, $f_{\max}$, and $g_m f_T/I_D$ performance of NCFETs with the MFIS structure, which is the more practical structure for RF applications, have been investigated, providing a previously unavailable baseline for future studies into the RF performance of NCFETs.

2. Utilizing a combination of physics-based device simulation and small-signal circuits, the f_T of MFIS NCFETs was found to be similar compared to a baseline MOSFET device for a given technology.

3. The $f_{\max}$ of NCFETs was found to be negatively impacted by the ferroelectric damping constant. However, it was also found that similar $f_{\max}$ versus a baseline MOSFET device can be achieved if the damping constant is sufficiently low.

4. The $g_m f_T/I_D$, a metric that can simultaneously capture the dc power consumption and RF performance, has been investigated for MFIS NCFETs. The value of $g_m f_T/I_D$ for MFIS NCFETs was found to be much higher compared to that of a baseline device, showing promise for next-generation RF applications with NCFETs.

Utilizing an experimentally calibrated baseline MOSFET model, basic RF performance metrics of the NCFET were successfully predicted in this stage, providing the field with a previously unavailable performance prediction for the application of NCFETs in RF applications. By highlighting the pros and cons of the NCFET structure, the predictions made through this stage are extremely important starting points for future detailed evaluations of NCFETs in the domain of RF electronics.

5.1.2 Stage 2 (Chapter 3)

The specific contributions from this stage, "Potential Enhancement of f_T and $g_m f_T / I_D$ via the Use of NCFETs to Mitigate the Impact of Extrinsic Parasitics," are as follows:

1. Extending from the general benchmarks of the first stage, the potential for NCFETs to improve the *extrinsic* unity-current-gain cut-off frequency $f_{\mathrm{T,e}}$ by mitigating the effects of extrinsic parasitic capacitances via a higher intrinsic gate capacitance C_{gg} have been investigated.

2. Using this basic idea and numerical simulations, the $f_{\mathrm{T,e}}$ and $g_m f_T / I_D$, the latter calculated using extrinsic quantities, of the NCFET was found to be up to 20% higher for $f_{\mathrm{T,e}}$ and up to 80% higher for $g_m f_T / I_D$. This increase in $f_{\mathrm{T,e}}$ is comparable to improvements seen between technology nodes.

3. The increases of $f_{\mathrm{T,e}}$ and $g_m f_T / I_D$ in NCFETs are accompanied by an undesirable decrease of the *intrinsic* unity-current-gain cut-off frequency $f_{\mathrm{T,i}}$, which is the unity-current-gain cut-off frequency of the core transistor structure. This decrease is a result of the ferroelectric electrostatics near the drain effectively increasing the electrical channel length of NCFETs. Two ways of alleviating the undesirable decrease of $f_{\mathrm{T,i}}$, via channel-length scaling and adjustments to V_{th} and V_{DD} of the NCFET, were proposed and examined.

4. It was found that the performance gain of NCFETs is decreased as extrinsic parasitic resistance increases. This trend emphasizes the importance of keeping

parasitic resistances as low as possible to maximize performance gains from NCFETs.

5. It was found that as parasitic capacitance increases, the performance gain in NCFETs is more pronounced. Hence, the benefits of using an NCFET is expected to increase as scaling continues, demonstrating the promise of NCFETs for use in next-generation RF applications.

Building upon the results of stage 1, this stage further examined the RF performance potential of NCFETs by examining the potential for this architecture to mitigate parasitic capacitances and improve $f_{\mathrm{T,e}}$ as well as $g_m f_T / I_D$. Through this investigation, we have illuminated a specific potential advantage of NCFETs towards future RF applications, and have outlined important design considerations for NCFETs to maximize the potential, such as the need to minimize parasitic resistances.

5.1.3 Stage 3 (Chapter 4)

The specific contributions of this stage, "Toward a BEOL GHz-Frequency Ferroelectric Negative-Capacitance Oscillator with a Wide Tuning Range," are as follows:

1. Utilizing expertise gained with respect to negative capacitance devices developed in the previous two stages, the potential for single-domain ferroelectric dynamics to be exploited for use in a tuned oscillator is explored. It was found that tuned oscillation can be achieved by replacing the inductor in a traditional LC oscillator with a ferroelectric.

2. The operating principles of the proposed ferroelectric oscillator were analyzed using techniques applicable in non-linear dynamics, and a sufficient criterion for oscillation has been found analytically.

3. The amplitude of oscillation was found to be proportional to the coercive field of the ferroelectric. In addition, an expression for maximum frequency of oscillation has also been derived. Both results can be used by designers in designing the proposed ferroelectric oscillator that can meet required performance metrics.

4. The performance of the oscillator was compared to an equivalent traditional LC oscillator. It was found that the tuning range can be vastly higher at the cost of worse phase noise. If both tuning range and phase noise are considered, the overall performance of the two oscillators are shown to be similar, meaning that the proposed ferroelectric oscillator can be an attractive alternative to the traditional LC oscillator as it has a much smaller footprint from its inductor-less design.

Building upon the expertise obtained in the previous two stages regarding negative capacitance, this stage explores the possibility of using negative capacitance as a standalone element. Through our investigations, we have proposed an oscillator that utilizes the ferroelectric negative capacitance that could be a suitable candidate to address challenges with the existing LC oscillator design.

5.2 Future Work – RF Linearity Performance Projection of Negative-Capacitance FETs

In stage 1 and stage 2 of this work, the RF performance of NCFETs has been evaluated in terms of important figures of merit including f_T, $f_{\max}$, and $g_m f_T / I_D$. In addition to these figures of merit, another essential step in further unveiling the RF performance potential of these novel transistors is to examine their RF linearity. While this performance metric has been considered superficially by previous studies [94], [125], and shows promise over standard MOSFETs, these studies were restricted to basic calculations using derivatives of static characteristics. Crucially, the impact of non-linear capacitance has not been examined in the context of NCFET linearity, which has been shown in previous studies [126], [127] to have profound impacts on the linearity of graphene and carbon nanotube FETs.

While the ferroelectric ideally acts as linear negative capacitor with a constant capacitance, this approximation is only valid for the center of the previously discussed S-shaped curve, which is repeated here as Fig. 5.1(a). If the entire ferroelectric behavior is examined, this ideal, constant negative capacitance transitions from a negative capacitance to a positive capacitance in an extremely non-linear fashion away from the center of the S-shaped curve, as depicted in Fig. 5.1(b).

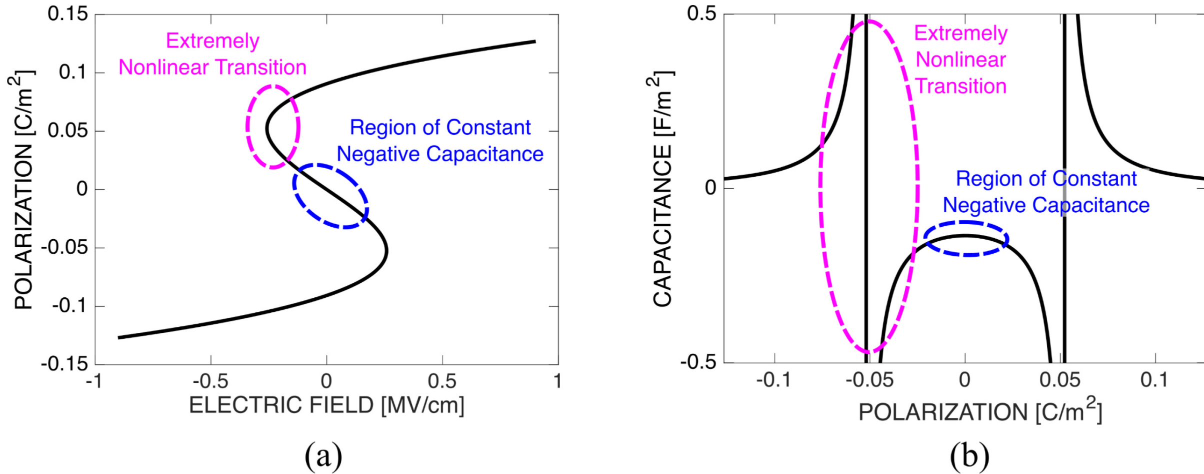


Fig. 5.1(a) The S-shaped polarization-electric field curve of the ferroelectric. (b) The corresponding capacitance -polarization curve obtained by taking the first derivative of polarization vs. electric field. The colored circles show the same regions of constant negative capacitance and the extremely non-linear transitions for each plot.

Thus far, it has been shown that depending on device design, parts of the ferroelectric could be in the positive capacitance region, while other parts would be in the negative capacitance region in an NCFET [36], which could correspond to an extremely non-linear capacitance due to the sharp transition region illustrated in Fig. 5.1(a) and (b). Furthermore, it has also been shown that in stacked ferroelectric-dielectric structures, which can serve as simplified models of the NCFET gate stack, the time-dependent trajectory of ferroelectric polarization and electric field is also extremely non-linear [128], which also corresponds to a time-dependent non-linear capacitance, since capacitance is directly related to the polarization-electric-field behavior as discussed in Chapter 1. Given these observations, it is important to carefully examine the RF linearity behavior of NCFETs beyond the superficial work done thus far [94], [125].

Building upon the extensive knowledge on ferroelectric negative capacitance, NCFETs, and the simulation framework established in stages 1 and 2 of this work, the linearity of NCFETs can be examined using a non-linear equivalent circuit approach, combining linear RF performance evaluations in stages 1 and 2, and previous work from our research group evaluating the non-linear RF performance of FETs [126], [127].

To conduct this study, a “core” or “intrinsic” device structure will be modeled in a similar manner as the first two stages of this work, exploiting our existing model that couples

ferroelectric electrostatics with modified drift-diffusion transport. Beyond the existing model, this study will also aim to further improve the existing multidomain ferroelectric model beyond the already-modeled polarization gradient effects, by including additional important effects discussed in literature such as the inclusion of dielectric grains [129]. Similar to the previous stages, an extrinsic model capturing effects of the contacts beyond the immediate vicinity of the transistor will also be constructed in a similar manner, and both the intrinsic and the extrinsic model will be used to construct a non-linear equivalent circuit model, as done in [127]. Finally, the linearity performance of NCFETs will be explored via circuit simulations of the non-linear equivalent circuit model, which will provide further insights into the RF performance potential of these devices.

5.3 Conclusion

In conclusion, the first two stages of this work (Chapter 2 and Chapter 3) provide important first steps in exploring the potential of NCFETs for use in future RF applications, and the third stage of this work (Chapter 4) illustrates the potential benefits of ferroelectrics negative capacitance for use in RF circuits beyond the NCFET configuration. Further, the work proposed in Section 5.2 outlines yet another unexplored facet for NCFETs in terms of RF performance. Combining all the three completed stages along with the proposed future work, this thesis thus provides concrete contributions towards the on-going effort of improving the performance of nanoscale electronic devices to meet the continually increasing demands of performance and power in modern applications.

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