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A THREE MODE FREQUENCY FEEDBACK CONTROLLER

BY

L. R. SCHNEIDER

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE

DEGREE OF MASTER OF SCIENCE

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FACULTY OF GRADUATE STUDIES

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled, " A Three Mode Frequency Controller ", submitted by L. R. Schneider in partial fulfilment of the requirements for the degree of Master of Science.

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Supervisor

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Date.....

ABSTRACT

Digital control algorithms have existed for some time in direct digital control installations, however, the expense of high resolution analog to digital and digital to analog converters makes these positional algorithms uneconomic for single loop control. Using frequency as a feedback medium, rather than direct A/D and D/A conversion, can result in an economical single loop digital controller. Employing this concept the traditional position algorithm is replaced with a velocity one, in which a voltage controlled oscillator and stepper motor replace the A/D and D/A converters respectively. Test results from a controller using a PID velocity algorithm indicate that frequency feedback can produce a controller with performance characteristics similar to those of the conventional three mode analog device.

ACKNOWLEDGEMENTS

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I wish to thank my supervisor, Dr. J. F. Vaneldik, for his review, comments and assistance and Dr. K. A. Stromsmoe for his guidance throughout the project. I would also like to acknowledge the help given by the University of Regina to allow my project to be completed there. A special thanks to my wife who offered encouragement during the difficult days.

The financial help given by the National Research Council, Calgary Power Limited, and the University of Alberta was greatly appreciated.

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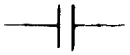
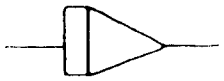
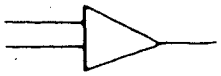
LIST OF SYMBOLS

Symbol	Explanation
$c(t)$	Feedback Variable
$\theta(t)$	Stepper Motor Output
$f_o(t)$	Frequency Input to Stepper Motor
f_s	Sample Frequency
f_c	Highest Frequency Component in Sampled Signal
f_{vco}	Voltage Controlled Oscillator Output Frequency
t_{sa}	Sample Period
T	Aperture time
	Time Delay Between Sucessive c(t) Evaluations
x	Deflection of c(t)
a	Acceleration
K	Analog Proportional Gain Setting
K^*	Digital Proportional Gain Setting
K_s	Stepper Motor Gain
K_{vco}	Voltage Controlled Oscillator Gain
G_i	Digital Integral Gain
T_i	Analog Reset Time in sec/repeat
β	Digital Derivative Gain
T_d	Analog Rate Time in sec
◯	Potentiometer
A	Relay

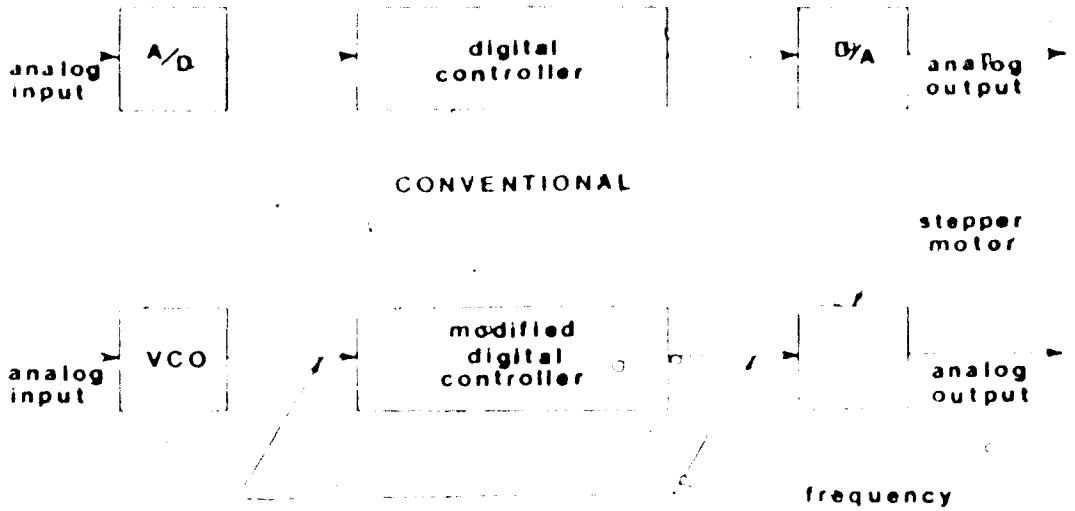
Symbol	Explanation
	Normally Open Relay Contact
	Normally Closed Relay Contact
	Integrator
	Summer
	Inverter

Chapter 1

INTRODUCTION

Between the extremes of the single loop analog controller on the one hand and computer control of many loops on the other, lies a field of application for an economical single loop digital controller.

The single loop digital controller could be expected to replace the analog device, resulting in better control resolution and drift free output.[3] Because the digital controller interfaces easily with a digital computer, it would provide an excellent back up for a computer operating in the direct digital control environment, or as an end device for a supervisory computer system employing setpoint control. These obvious advantages of digital control have been apparent for some time,[3] however, the relatively high cost of using analog to digital and digital to analog converters with sufficient resolution to yield meaningful results has made single loop digital controllers uneconomic. An alternate approach in the development of the digital controller has been the use of frequency as an intermediate medium between the analog and digital states as shown in figure 1.



CONTROLLER CONFIGURATION

FIGURE 1

Use of the voltage controlled oscillator and the stepper motor as analog to frequency and frequency to analog converters respectively have eliminated the need for the conventional analog to digital and digital to analog devices.

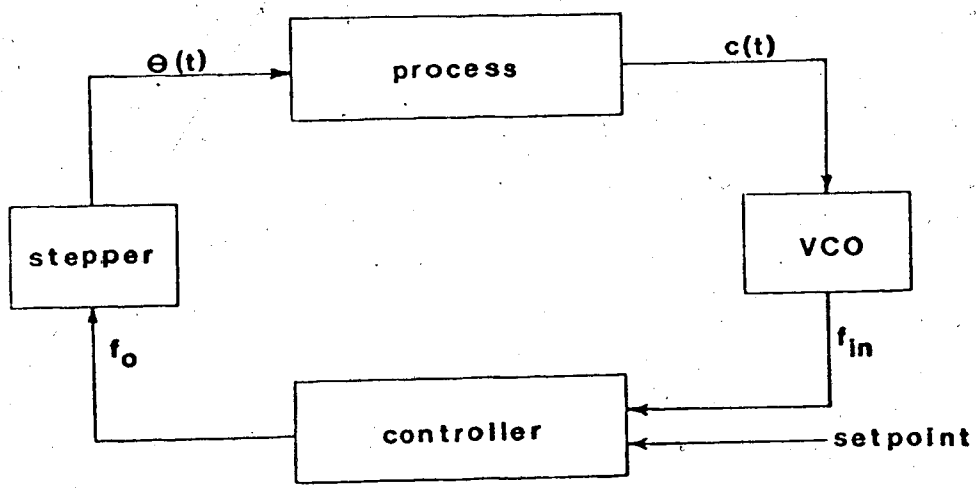
Problems encountered with transmission of analog signals over relatively long distances in a noisy environment can largely be eliminated by using frequency feedback. Converting to frequency at the end device and using it as the feedback medium provides immunity to analog noise and removes the need for extensive filtering to produce a " clean " signal.

Using the frequency feedback approach Montgomerie et al[1] produced a workable PI temperature controller in 1968. The purpose of this research was to extend the scope to include a derivative term, hence developing the digital equivalent of the conventional analog three mode controller. Several other features were added to enhance the controller performance. Instead of providing a control output for each of the terms, as was previously done, the components were added to produce a composite control signal for each sample period. To provide added controller flexibility a sampling rate adjustment has been added to allow tuning of the controller sampling rate to the process response time.

Chapter 2

THEORY OF OPERATION

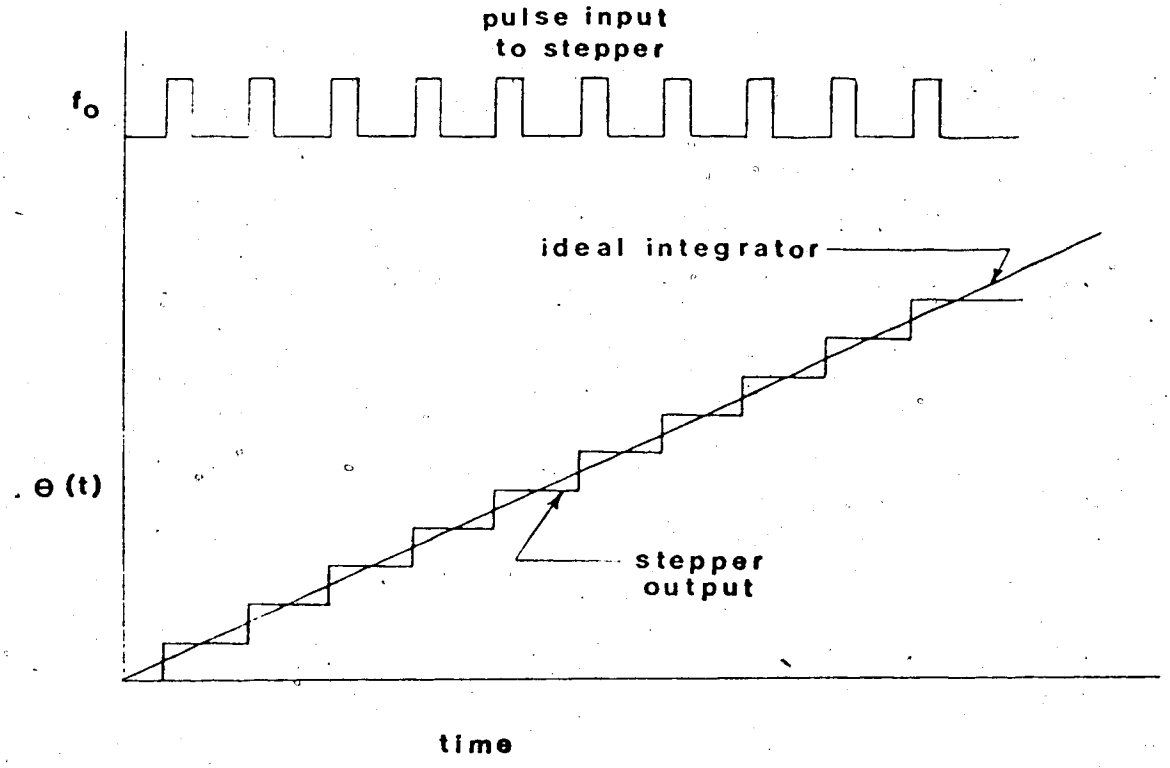
The aim of this project was to implement the digital equivalent to the existing analog three mode controller using the frequency feedback concept shown in figure 2.



FREQUENCY FEEDBACK CONTROLLER

FIGURE 2

Consider the stepper motor output shown in figure 3.



STEPPER MOTOR CHARACTERISTICS

FIGURE 3

Providing the step size is sufficiently small* the stepper motor may be considered an integrator with the following transfer function.

* The difference in stepper output and an ideal integrator is shown in figure 3. The difference is due to the stepper quantization error.

$$\theta(t) = K_o \int f_o(t)dt \tag{2.1}$$

$\theta(t)$ = Stepper output

$f_o(t)$ = frequency input to stepper motor

To produce an output proportional to the measured error the stepper motor input frequency must be of the form.

$$f_{01}(t) = K_1 \, d \, \frac{e(t)}{dt} \qquad e(t) = \text{error} \tag{2.2}$$

Extending this reasoning, the term corresponding to the integral of the error is obtained.

$$f_{02}(t) = K_2 \, e(t) \tag{2.3}$$

The derivative term is obtained in a similar fashion.

$$f_{03}(t) = K_3 \, d^2 \, \frac{e(t)}{dt^2} \tag{2.4}$$

Combining the three terms

$$f_0(t) = K_1 \, d \, \frac{e(t)}{dt} + K_2 \, e(t) + K_3 \, d^2 \, \frac{e(t)}{dt^2} \tag{2.5}$$

Using this frequency as the stepper motor input

$$\theta(t) = K_o K_1 e(t) + K_o K_2 \int e(t)dt + K_o K_3 d \frac{e(t)}{dt} \qquad (2.6)$$

which is the transfer function of a conventional PID controller.

Simplifying

$$\theta(t) = K \left[e(t) + \frac{1}{T_i} \int e(t)dt + T_d d \frac{e(t)}{dt} \right] \qquad (2.7)$$

$$K = K_o K_1$$

$$T_i = \frac{K}{K_o K_2}$$

$$T_d = \frac{K_o K_3}{K}$$

Since the digital controller is a discrete device, consider the discretized equivalent at time $t = t_{s-1}$.

$$\theta_{s-1} = K \left[e_{s-1} + \frac{1}{T_i} \sum_{j=o}^{s-1} e_j \Delta t + T_d \frac{\Delta e_{s-1}}{\Delta t} \right] \qquad (2.8)$$

At time $t = s$

$$\theta_s = K \left[e_s + \frac{1}{T_i} \sum_{j=o}^{s} e_j \Delta t + T_d \frac{\Delta e_s}{\Delta t} \right] \qquad (2.9)$$

$$\theta_s = K \left[e_s + \frac{1}{T_i} \sum_{j=o}^{s-1} e_j \Delta t + \frac{1}{T_i} e_s \Delta t + T_d \frac{\Delta e_s}{\Delta t} \right] \qquad (2.10)$$

Subtracting

$$\theta_s - \theta_{s-1} = K \left[e_s - e_{s-1} + \frac{1}{T_i} e_s \Delta t + T_d \frac{\Delta e_s - \Delta e_{s-1}}{\Delta t} \right] \tag{2.11}$$

Now

$$e_s = r_s - c_s \tag{2.12}$$

r_s = setpoint

c_s = feedback variable

$$\theta_s - \theta_{s-1} = K \left[(r_s - c_s - r_{s-1} + c_{s-1}) + \frac{\Delta t}{T_i} (r_s - c_s) + \frac{T_d}{\Delta t} (\Delta (r_s - c_s) - \Delta (r_{s-1} - c_{s-1}) \right] \tag{2.13}$$

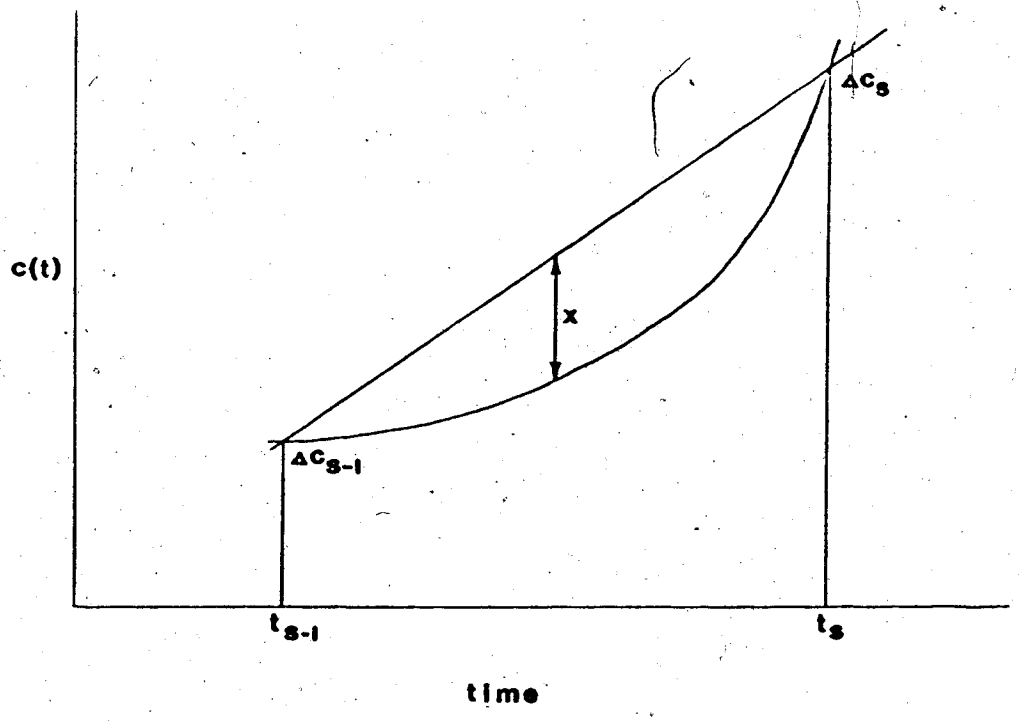
Assuming no setpoint changes

$$\theta_s - \theta_{s-1} = K \left[(c_{s-1} - c_s) + \frac{\Delta t}{T_i} (r_s - c_s) + \frac{T_d}{\Delta t} (\Delta c_{s-1} - \Delta c_s) \right] \tag{2.14}$$

$\theta_s - \theta_{s-1}$	$(c_{s-1} - c_s)$	$\frac{\Delta t}{T_i} (r_s - c_s)$	$\frac{T_d}{\Delta t} (\Delta c_{s-1} - \Delta c_s)$
required correction	proportional term	integral term	derivative term

The integral and proportional terms can be obtained by a straightforward evaluation of the difference between the setpoint and feedback signal and between two successive feedback signals respectively. Direct evaluation of the derivative term $(\Delta c_{s-1} - \Delta c_s)$ is difficult; however, it can be evaluated indirectly. It is shown in Appendices A and D that the derivative term can be evaluated in

both sign and magnitude by measuring the amount of deflection " x " in the feedback variable c(t) as indicated below.



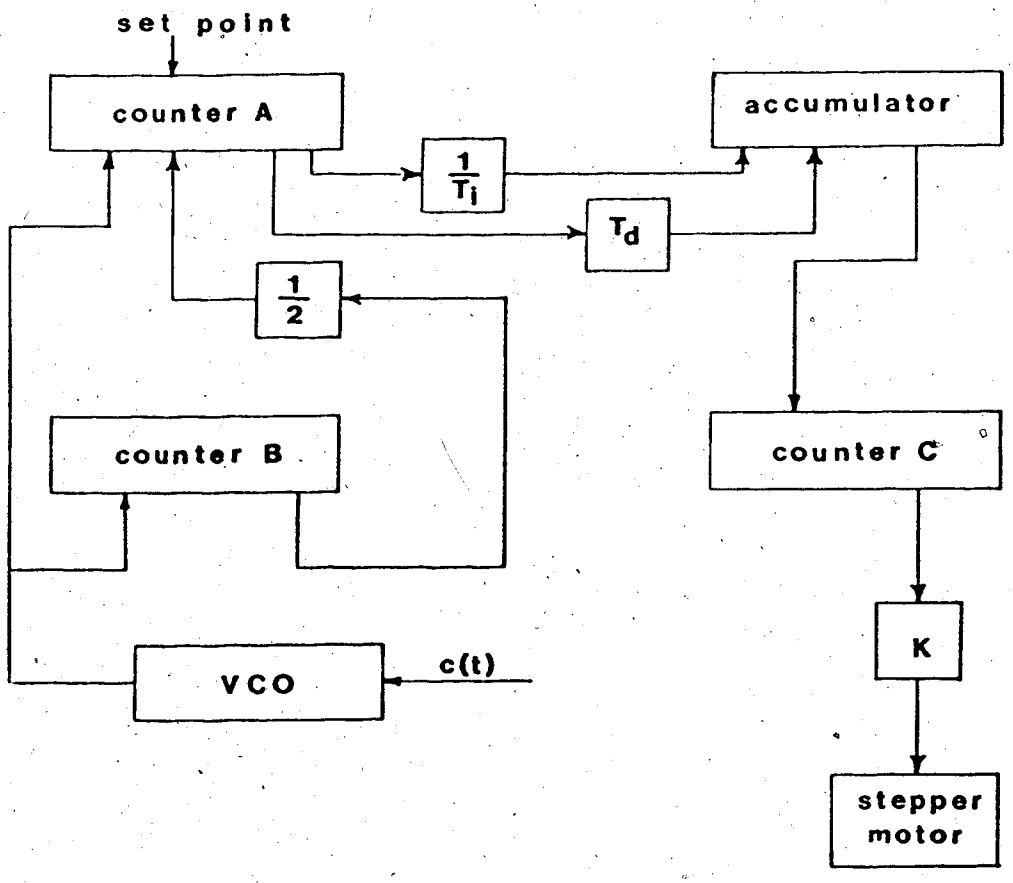
DEFLECTION MEASUREMENT

FIGURE 4

Chapter 3

IMPLEMENTATION

To minimize the sampling time, a scheme using four counters as shown below was implemented.



COUNTER CONFIGURATION

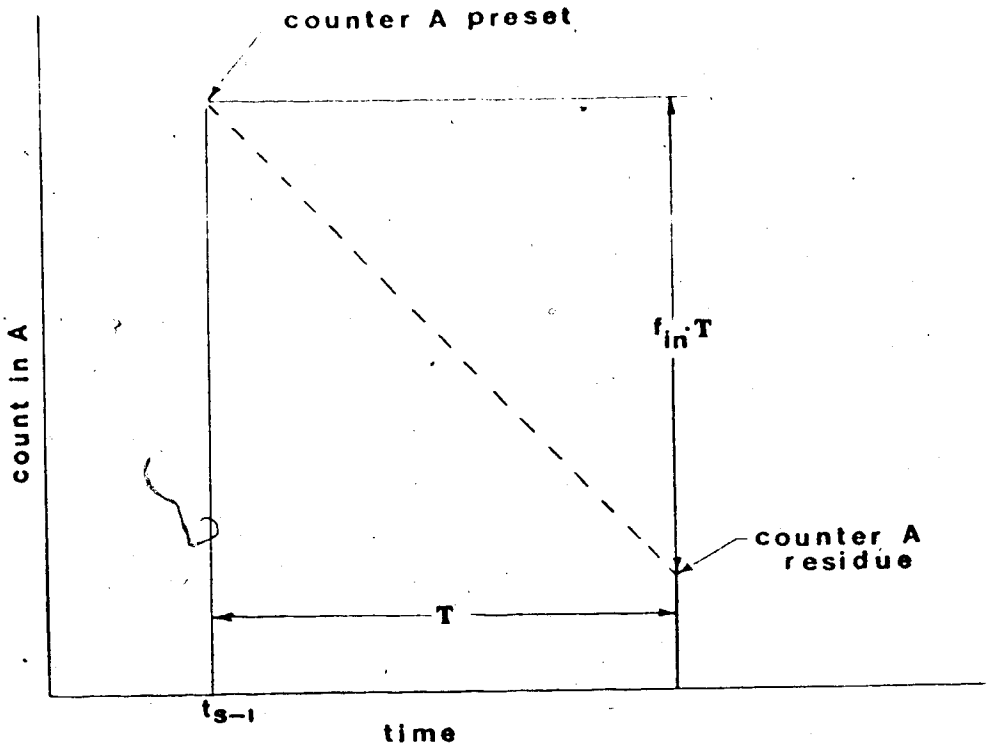
FIGURE 5

Each of the three terms is evaluated individually as follows.

1 Integral term $(r_s - c_s)^*$

The set point r_{s-1} is preset into counter A. The voltage controlled oscillator, with c(t) as voltage input, is enabled to counter A for a period T. Setting counter A in the count down mode produces a residue proportional to $(r_{s-1} - c_{s-1})$ as shown in figure 6. The residue in counter A is multiplied by the appropriate gain and placed in the accumulator as the integral term.

* In the interest of minimizing the sampling time, the term $(r_{s-1} - c_{s-1})$ will be evaluated instead of $(r_s - c_s)$. The reason will become apparent later.

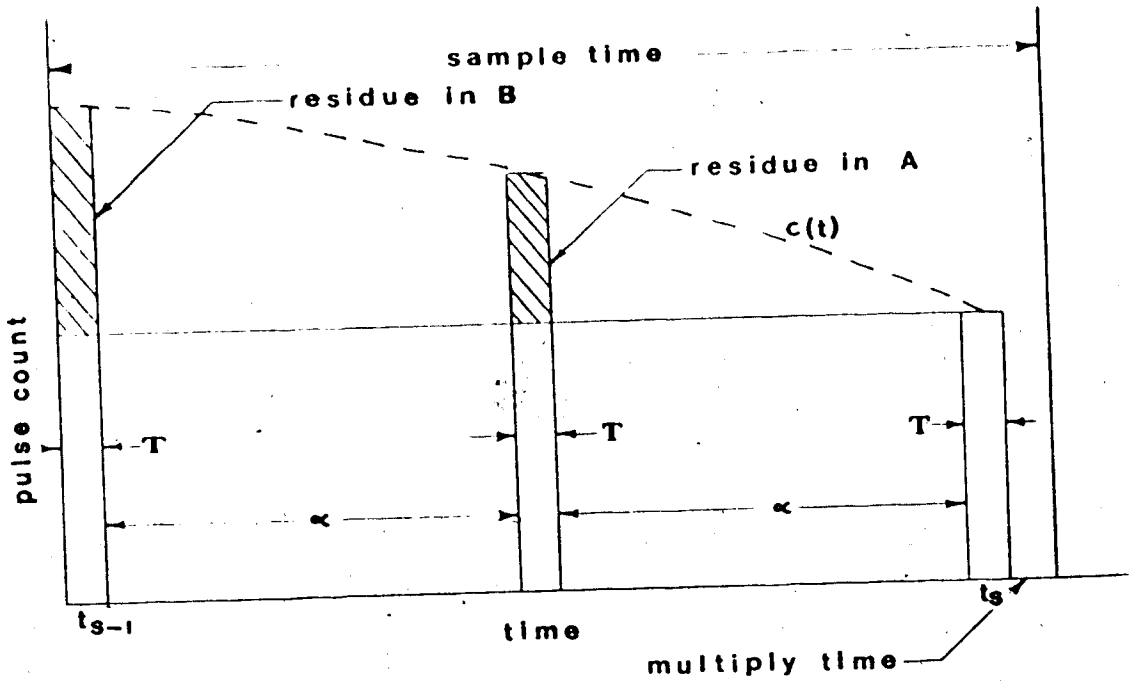


INTEGRAL EVALUATION

FIGURE 6

2 Proportional term $(c_{s-1} - c_s)$

At time $t = t_{s-1}$ the voltage controlled oscillator with c(t) as input is counted up in the initially zeroed counter B for time T.



PROPORTIONAL EVALUATION

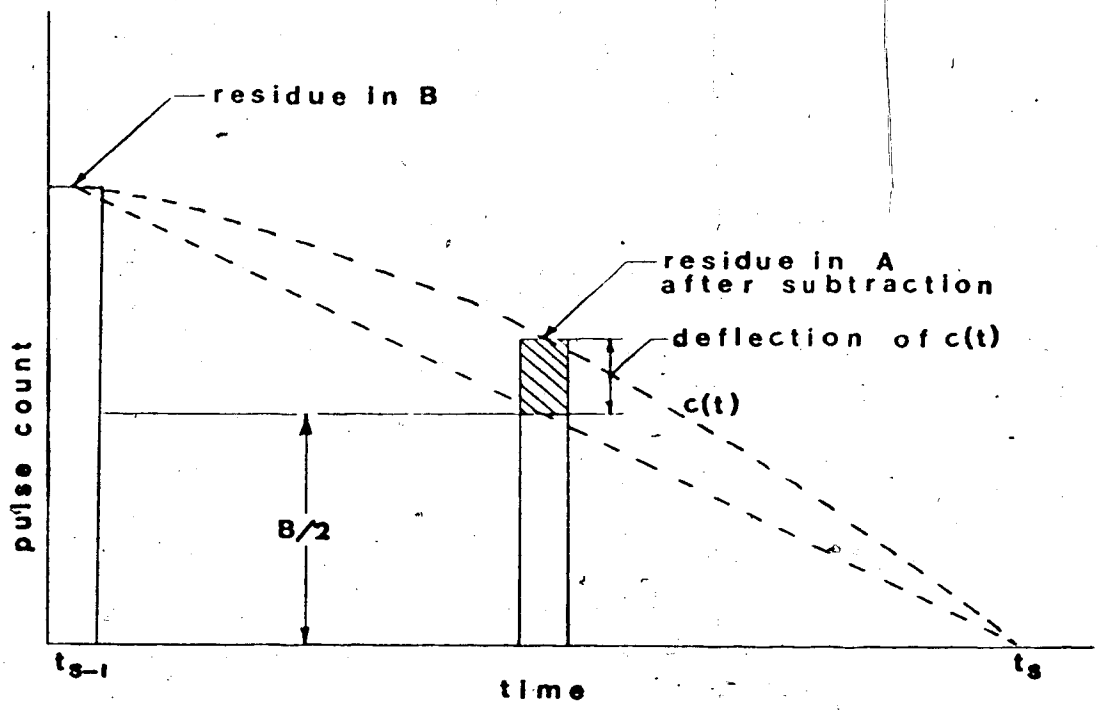
FIGURE 7

After the appropriate delay α^* the voltage controlled oscillator is counted up in the initially zeroed counter A for period T. Again after a delay of α (at time $t = t_s$) the voltage controlled oscillator is counted down in both counters A and B to yield the residues shown in figure 7. The residue in counter B, which is proportional to $(c_{s-1} - c_s)$, is added to the accumulator as the proportional term.

* The appropriate choice of α, like T, is dependent on the time constant of the controlled system. For added flexibility the terms α and T will be variable to allow "tuning" of the controller.

3 Derivative term $(\Delta c_{s-1} - \Delta c_s)$

Subtracting one half of the residue in counter B from the residue in counter A (see figure 7a), leaves a residue in counter A proportional to the magnitude of the deflection of c(t) and hence, as shown in Appendix D, proportional to the term $(\Delta c_{s-1} - \Delta c_s)$.



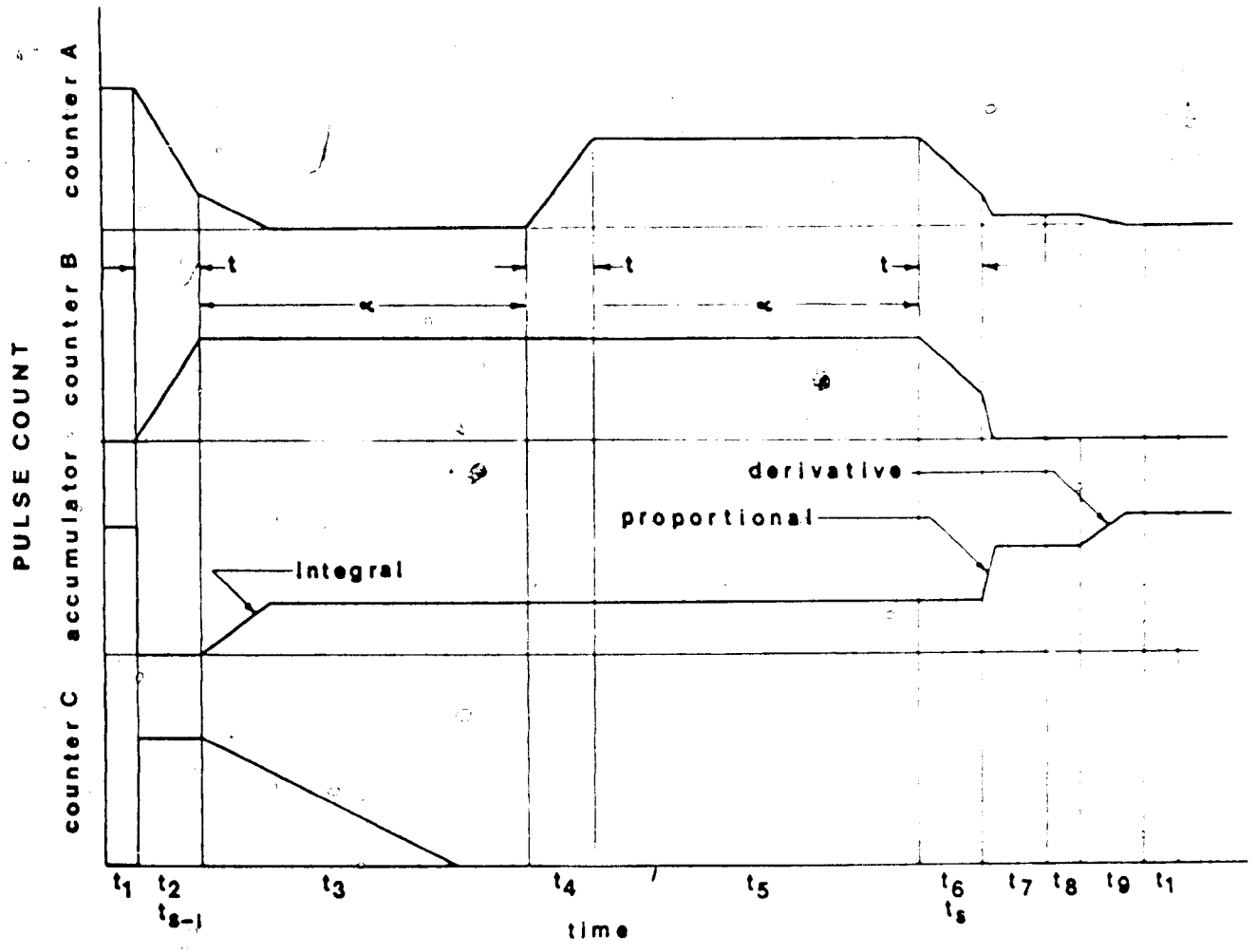
DIFFERENTIAL EVALUATION

FIGURE 7a

The counter A residue remaining after subtraction is multiplied by the appropriate gain and added to the accumulator as the derivative term. Although only one particular case (velocity and acceleration negative) is shown here, Appendix A demonstrates the consistent relationship between the sign of the A residue and $(\Delta c_{s-1} - \Delta c_s)$ for

all possible combinations of velocity and acceleration for c(t).

To minimize time the sum of the three control terms stored in the accumulator is strobed in parallel into counter C. The evaluation of the next sample is started while the contents of counter C is clocked to the stepper motor with a proportional gain. Sequence timing for a typical sample period is shown in figure 8.



CONTROLLER TIMING DIAGRAM

FIGURE 8

Chapter 4

CONSTRUCTION

Because most of the construction is a straightforward implementation of digital logic, the majority of the hardware will not be discussed but rather only shown on the schematic drawings in Appendix C. Only those elements which have a unique construction or which directly affect the controller performance will be discussed in detail.

Many design factors interact to affect the controller performance. Preliminary considerations suggested that performance would be altered by such factors as system time constant, sampling rate, quantization and gain to name a few. Since this interaction between factors is quite complex, mathematical analysis to determine the controller settings for the best response is difficult. Therefore, the design philosophy used in this thesis was to mathematically determine the maximum and minimum constraints on the parameters, build the controller, then further specify the parameters by evaluating preliminary performance tests.

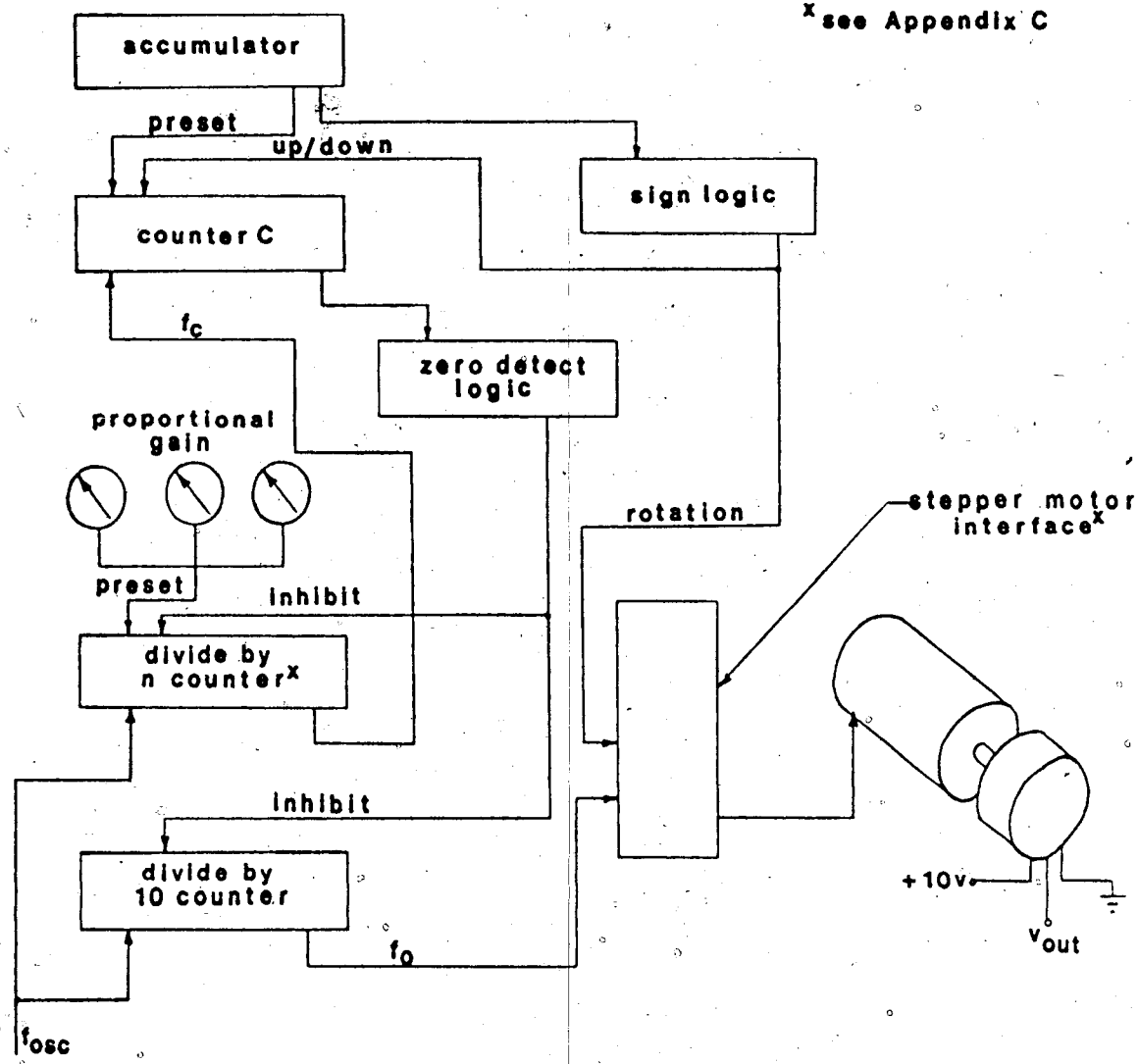
Several significant components and concepts will now be discussed.

1 Stepper Motor

Use of the stepper motor as a frequency to voltage transducer can be accomplished by coupling the motor output shaft to a potentiometer. To enable connection to a standard analog computer for

testing purposes, the analog voltage range for both the feedback signal into the voltage controlled oscillator and the control voltage from the potentiometer attached to the stepper motor was set at 0 to + 10v. Connecting counter C to the stepper motor as shown in figure 9 results in a digital to analog converter with adjustable gain.

Counter C is preset from the accumulator at the end of each sample period. The up/down control line for counter C and stepper rotation are determined by the sign of the accumulator. Simultaneous with the evaluation of the next control signal, f_{osc} is enabled to both the stepper and counter C and is inhibited when counter C reaches zero. The amount of stepper movement ΔV_{out} is proportional to $\frac{n}{10}$ times the original residue in counter C. The stepper used was a 1.8°/step coupled to a one turn potentiometer which produces a quantization error of $\frac{1}{200}$ or $\pm$ 0.05v. Obviously this error can be reduced by employing a smaller step size or a multiturn potentiometer. Performance of this unit will also depend on the stepper input frequency (f_{osc}), which will affect the rate of output voltage change. Testing the stepper motor capability disclosed a maximum skip free input frequency of approximately 300 pulses per second. In the interest of prolonged stepper life it was desired to reduce this frequency, therefore, f_{osc} was adjusted during preliminary tests. Adequate response speed was obtained for f_{osc} = 50 pulses per second.



[x] see Appendix C

OUTPUT CONFIGURATION

FIGURE 9

2 Voltage Controlled Oscillator

Performance of the voltage controlled oscillator is an important factor in the performance of the controller. The oscillator frequency is counted up in a counter for a specified aperture time T to produce a digital result. The amount of resolution, and hence the quantization error in this count, is dependent on two factors, namely: the oscillator frequency and the aperture time T. Ideally, an infinitely high oscillator would produce a good resolution count with a very short aperture time. Practically, the linearity of a voltage controlled oscillator deteriorates rapidly as the frequency range is increased.[13] As a compromise, and for reasons of availability, a voltage controlled oscillator[14] with 10 to 10k hertz output was chosen (A schematic is shown in Appendix C). The nonlinearity was found to be within 0.1%. Having chosen the voltage controlled oscillator, two factors remain to be resolved, namely: the aperture and sample times.

Aperture time

As shown previously, the discrete nature of the stepper motor produces a voltage uncertainty of ± 0.05v. Because the complete control signal consists of three independent components, each component must contribute a maximum error of ± 0.0167v to preserve the output accuracy. The errors introduced in each case result from the analog to digital conversion and subsequent multiplication. The A/D conversion is performed by counting the voltage controlled oscillator frequency, therefore, the counter enable time will dictate the quantization error. It can be shown (Appendix B) that an aperture time of 0.08 seconds

will produce a quantization error of $\pm$ 0.0125v for each component, yielding a worst case composite error of $\pm$ 0.0375v.

Sample time

From the Nyquist criterion the minimum sample rate is defined as

$$f_s = 2f_c \tag{4.1}$$

where f_c is the highest frequency component in the sampled signal. An accurate evaluation of f_c is difficult to obtain, but since f_c is required only to set a minimum bound on f_s, a rough approximation can be made. Because typical response curves are approximately sinusoidal,[15] we can consider the sampled curve to be of the form

$$c(t) = 2 \sin \omega_c t \tag{4.2}$$

$$d\,\frac{c(t)}{dt} = 2\omega_c \cos \omega_c t \tag{4.3}$$

$$d\,\frac{c(t)}{dt}_{max} = 2\omega_c \tag{4.4}$$

Using the response curve for an analog system with a ten second time constant $d\,\frac{c(t)}{dt}_{max}$ was found (figure A-1).

$$d\,\frac{c(t)}{dt}_{max} = 0.237\text{v/sec} = 2\omega_c \tag{4.5}$$

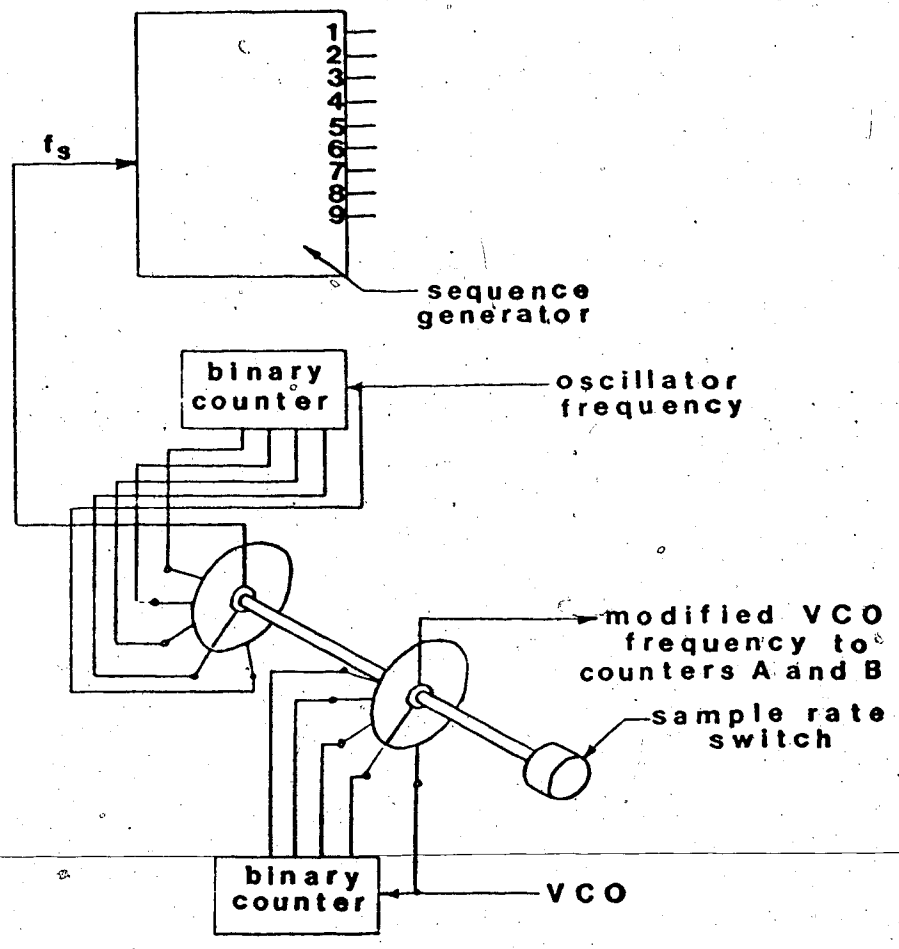
$$\omega_c = 0.118 \text{ rad/sec} \tag{4.6}$$

$$f_c = \frac{\omega_c}{2\pi} = 0.019 \text{ hertz} \tag{4.7}$$

$$f_s \geq 0.038 \text{ hertz} \qquad t_{sa} \leq 26 \text{ sec} \tag{4.8}$$

To allow for the rough approximation used, a sample time of approximately two seconds was chosen.

Making the sample and aperture times variable results in a more flexible controller. By accompanying each aperture time increase with a corresponding voltage controlled oscillator frequency decrease, the final count and hence the resolution, will remain unchanged. This feature will allow tuning the controller to a wide range of process time constants. The implementation is shown in figure 10.



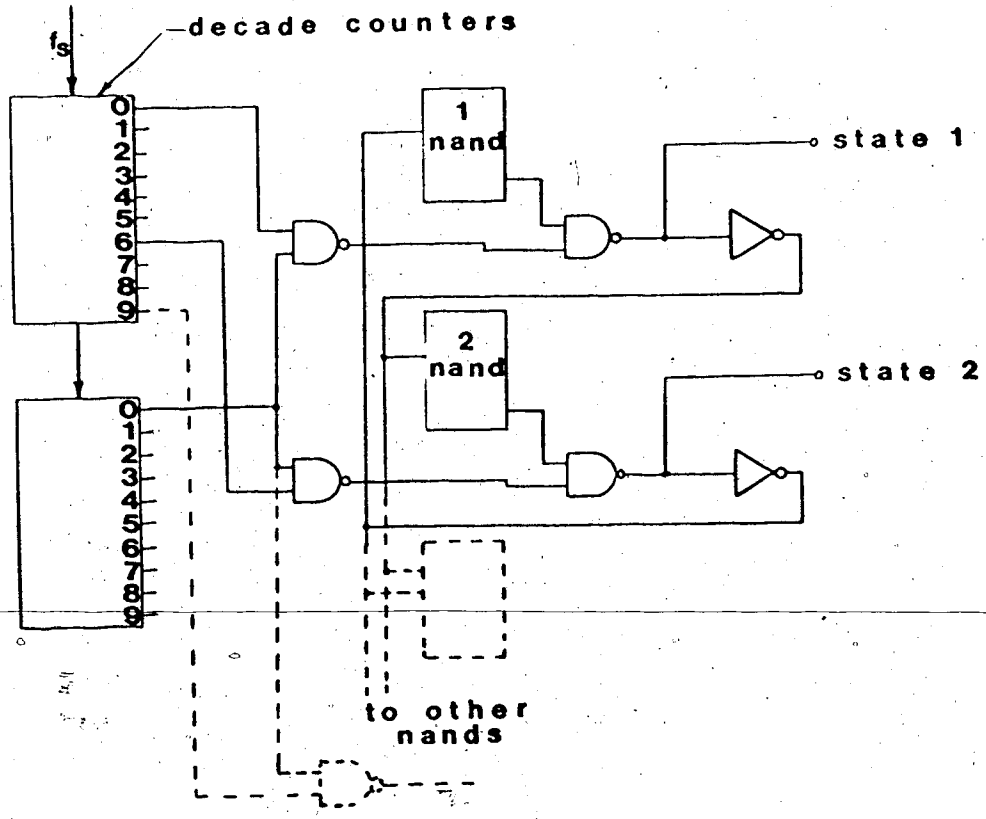
SAMPLE RATE SCHEMATIC

FIGURE 10

3 Sequence Generator

The implementation of the timing diagram shown in figure 8 required a sequence generator with nine stable states. Because several of the interval times resulted from rough approximations, the chances of possible alteration, governed by preliminary test results, were fairly high. For this reason, an easily adjusted sequence generator

was desired. By expanding and modifying the n-flop developed by Goldberg,[16] a sequencer meeting the above criteria was developed. To explain the operation, a partial schematic is shown in figure 11 (A complete schematic is shown in Appendix C).



SEQUENCE GENERATOR SCHEMATIC

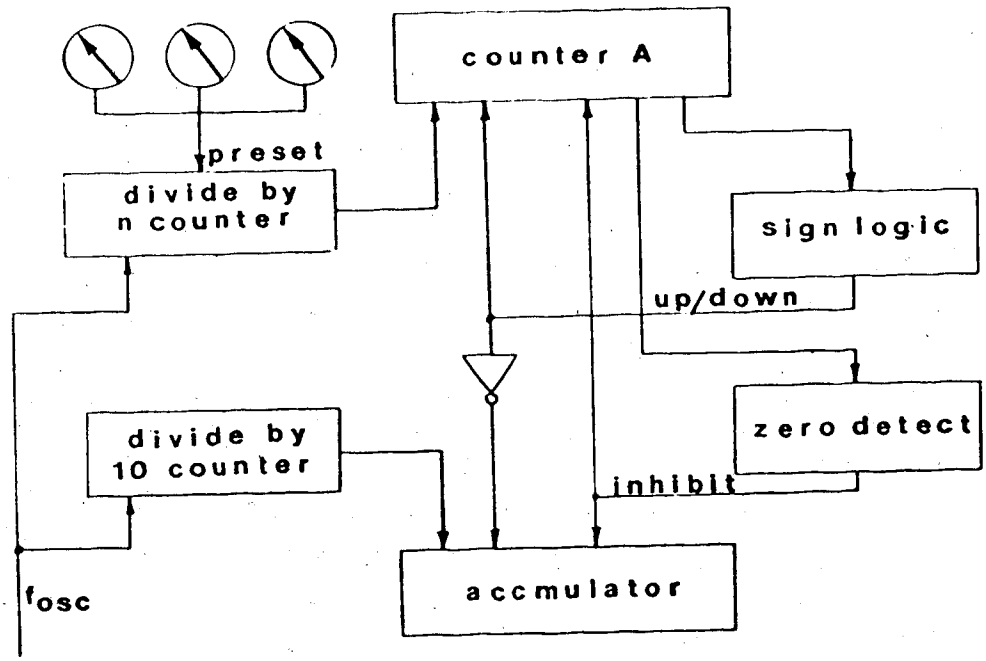
FIGURE 11

Assu is high, feedback through the inverter to all NAND i other states are zero. The remaining states (other an 1) are inverted and used as inputs for the #1 NAND. A zero output from the #1 NAND holds state 1 high. State 2 goes high when the

counter reaches 06. Feedback from state 2 through the inverter forces all other states (other than 2) to zero. This is a stable state and will remain until the next desired count is reached. Time duration changes are easily made by changing the counter connections to the two input NAND gates. Although the generator is extremely flexible, it is obvious that in operation one state is always high, therefore, in some cases a "dummy" state may be required to produce the desired intervals. Another feature is the overlap between intervals. Because the next state goes high before the present state goes low, care must be exercised when using this sequencer.

4 Multiplication

From previous calculations the sample time was chosen as approximately two seconds. This slow sample rate allows the required multiplications to be carried out serially with very little addition to the sample time (see figure 8) and large hardware component savings. The programmable divide by n counter[12] is used extensively to implement the serial multiplier. A typical configuration is shown in figure 12.



MULTIPLIER SCHEMATIC

FIGURE 12

The value to be multiplied is stored in counter A. The up/down count for both the accumulator and counter A is determined by the sign of counter A. For example, a positive initial value in counter A will set the A counter in a count down mode and the accumulator in a count up mode. A zero condition in counter A inhibits both counters completing the multiplication. The accumulator count can be shown to be $\frac{n}{10}$ times the original count in A. Similar configurations are used for each of the three terms in the control equation. Theoretical gain calculations for each term are given in Appendix D.

5 Sign Convention

The binary coded decimal number system was used to facilitate interfacing to the setpoint input. Positive numbers are represented by counting up in the counters yielding the traditional BCD form. Negative numbers are obtained by counting down yielding a 1000-x (counters are three decade) complement of the original number. A sign bit, which is appropriately set by zero transitions, is associated with each counter. Each sign is associated with a particular stepper motor rotation (positive = clockwise). A negative number in counter C is recomplemented on output by counting up to zero with the appropriate rotation. The sign convention can be clarified best by an example.

Case 1 Positive 20

Counter C

sign bit = 1 (positive)

value = 20

- sign bit sets the up/down count to down and stepper rotation to clockwise.
- counter C will count down until zero detect. Using a gain of 1, stepper will rotate 20 steps clockwise.

Case 2 Negative 20

Counter C

sign bit = 0 (negative)

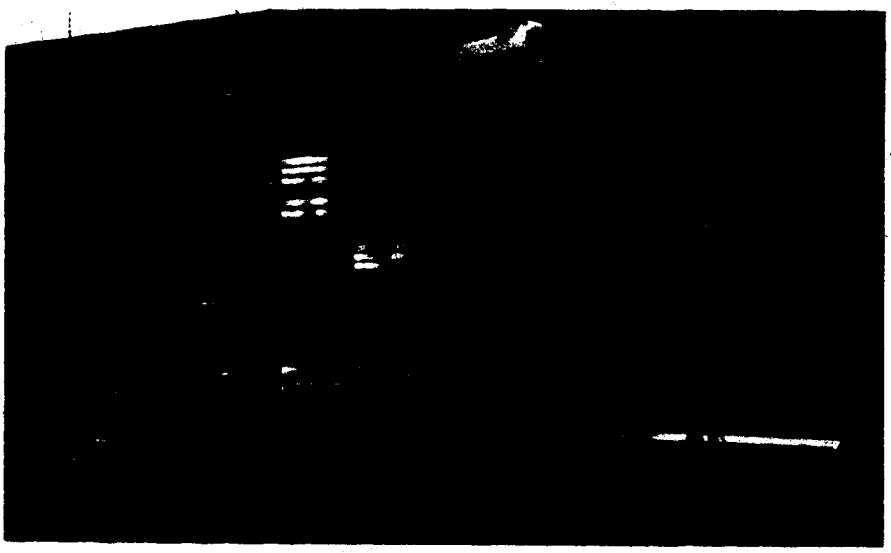
value = 980 (1000-20)

- sign bit sets the up/down count to up and stepper motor rotation to counterclockwise.
- counter C will count up until zero detect. Using a gain of 1, stepper motor will rotate 20 steps counterclockwise.

Chapter 5

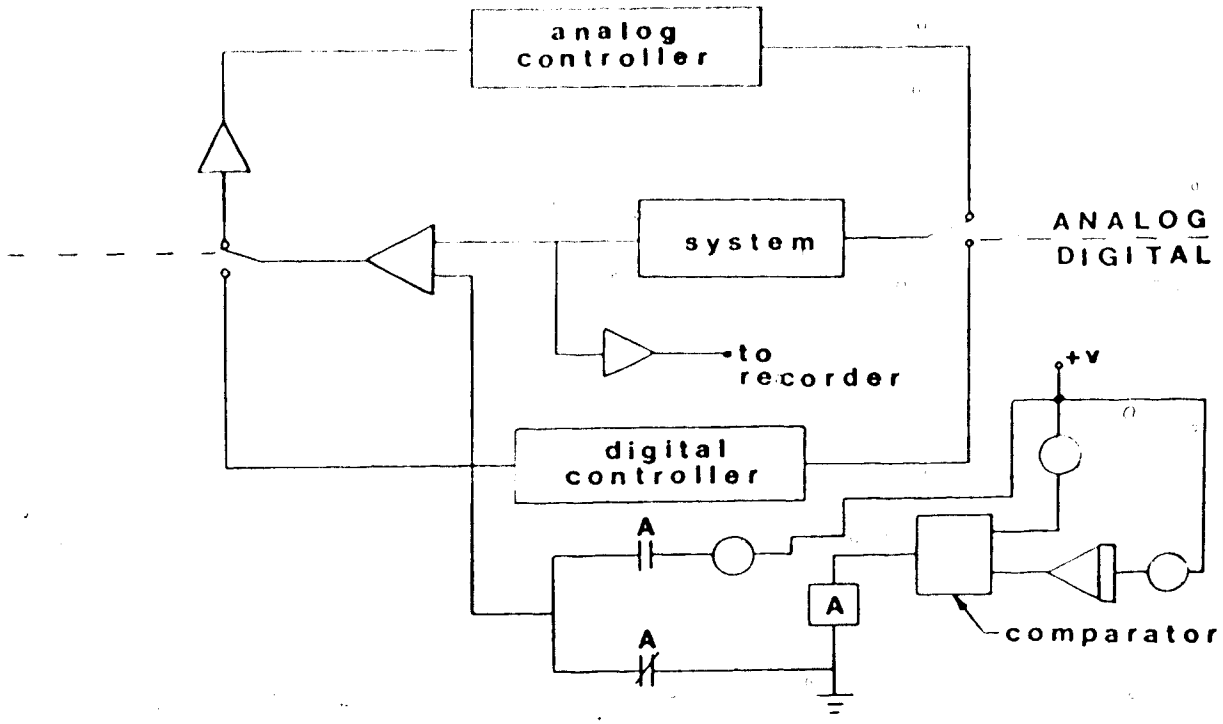
TESTING

The prime objective of the test series was to evaluate the performance of the digital controller in typical control applications. Performance was measured by recording the system response to a step disturbance in the feedback loop. First and second order lag approximations to a process control valve, simulated on the analog computer, were used as the controlled systems (see Appendix A). A system time constant of ten seconds was chosen as a typical representation of the physical system. The test configuration is shown physically in figure 13 and schematically in figure 14.



PHYSICAL TEST CONFIGURATION

FIGURE 13



TEST SCHEMATIC

FIGURE 14

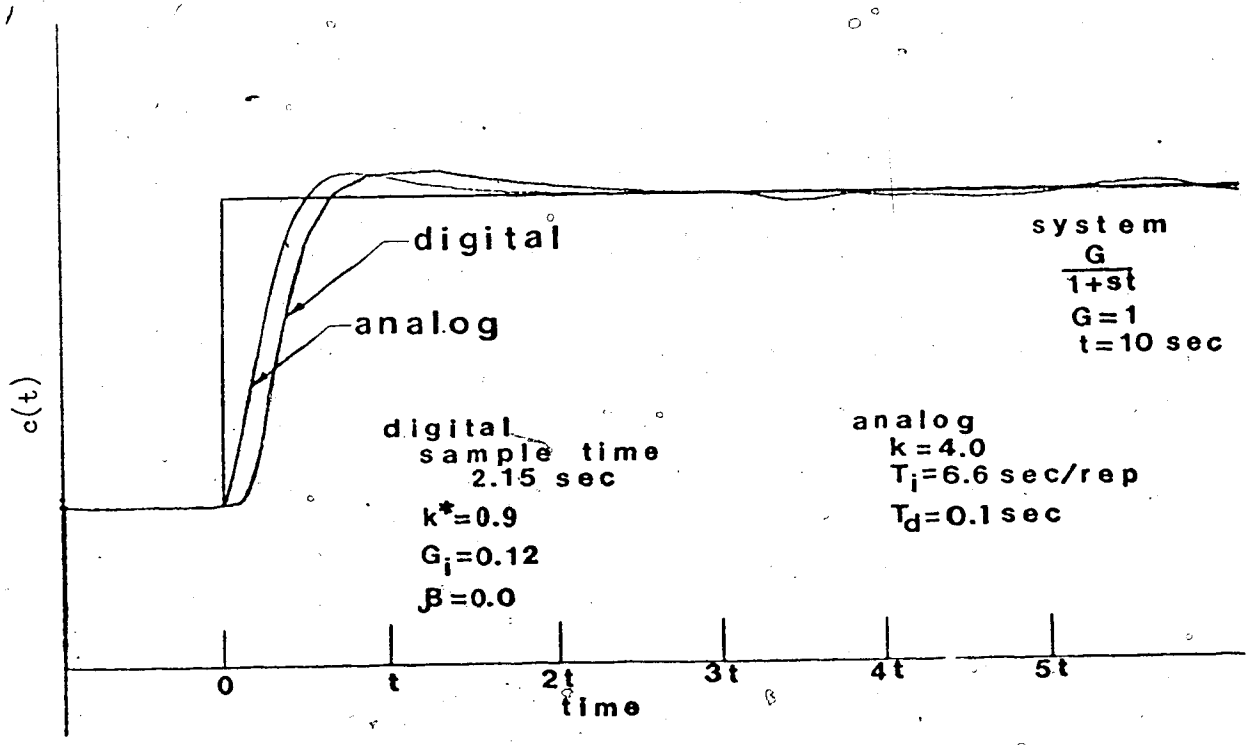
Three series of tests, as described below, were conducted to evaluate the effect of various parameters.

Series A (comparison test)

Using the first order process control valve approximation (Appendix E) as the controlled system, the optimized* response curves for the digital controller were obtained. These curves were compared

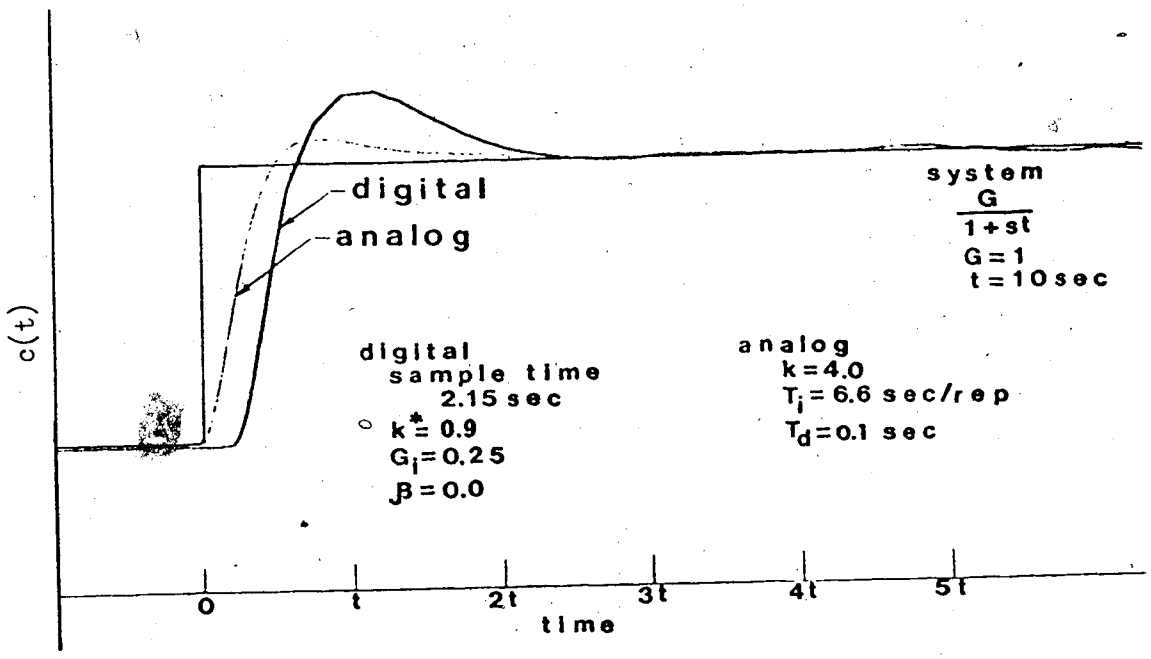
* Optimum response, used in the context of this thesis, refers to a response that exhibits the best combination of fast rise time and minimum overshoot.

to the optimized analog controller response for the same system. The analog controller used was an analog computer simulation of a three mode controller (Appendix E). The results appear in figures 15 - 17.



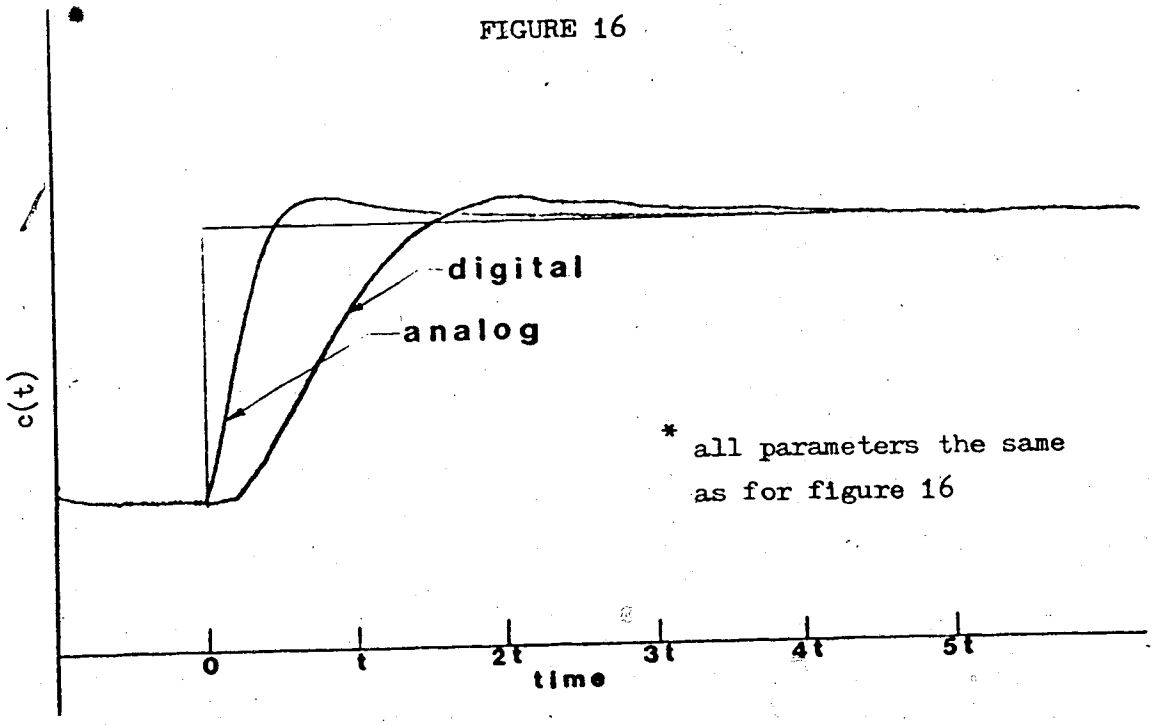
SYSTEM RESPONSE TO A UNIT STEP INPUT

FIGURE 15



SYSTEM RESPONSE TO A UNIT STEP INPUT

FIGURE 16

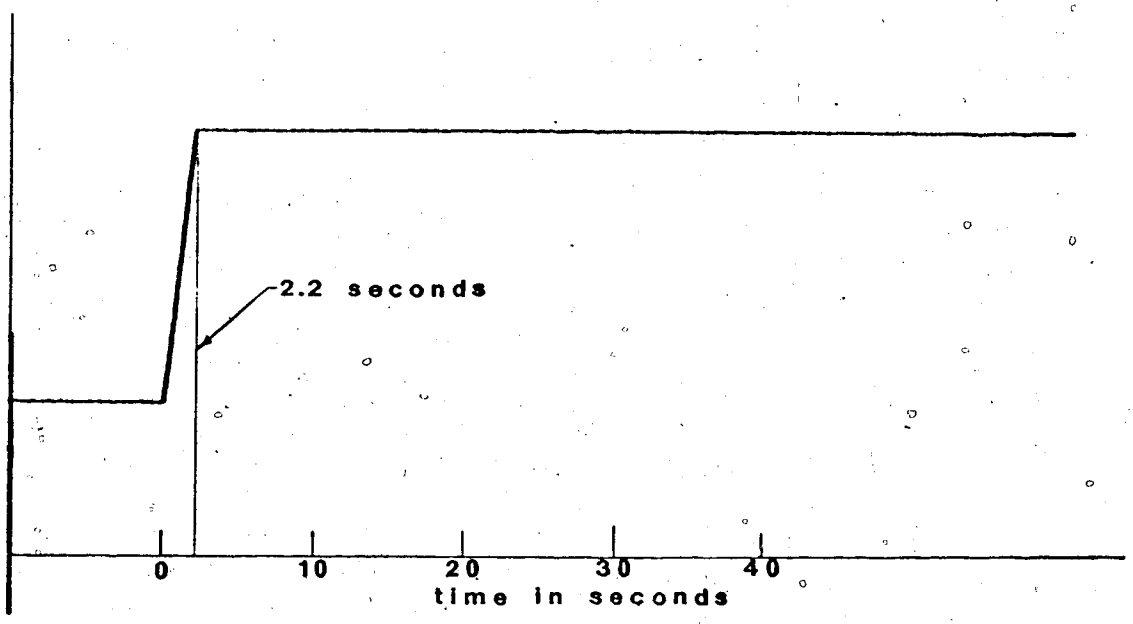


SYSTEM RESPONSE TO A SETPOINT CHANGE

FIGURE 17

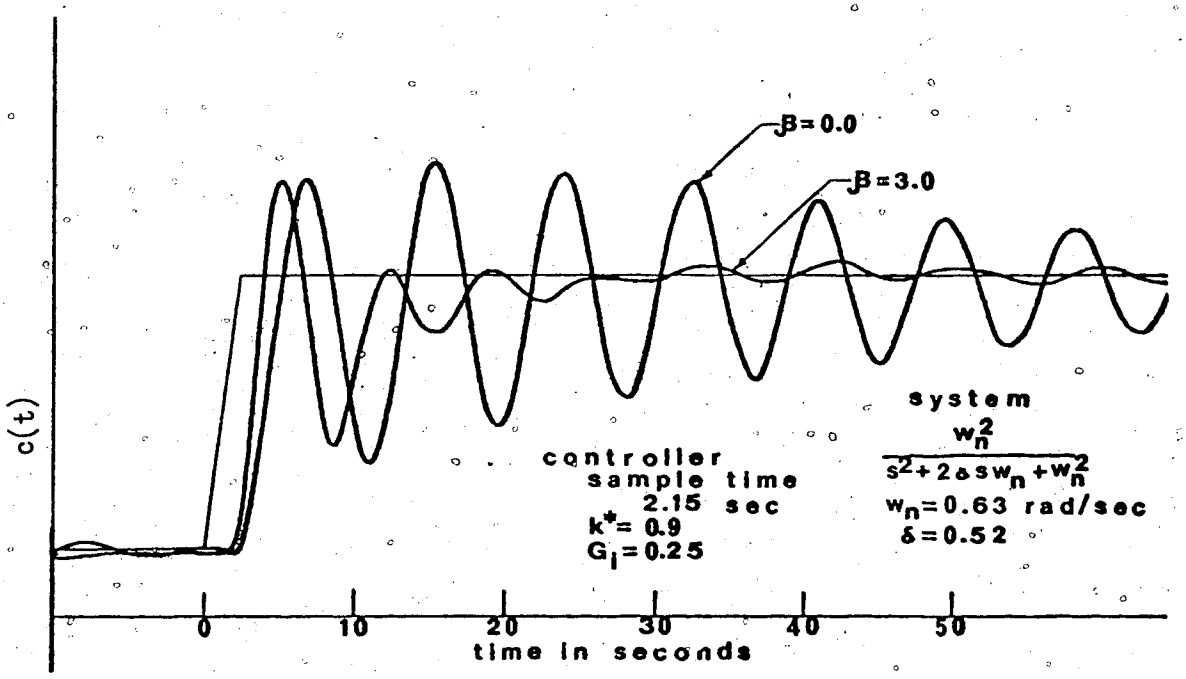
Series B (derivative term)

The PI control algorithm is optimal for first order systems[19] as proven by the series A set of tests (derivative times were approximately zero). To evaluate the effect of the derivative component, a second order approximation to a process control valve was used (Appendix E). Because of the nature of the controller another modification must be made. All calculations regarding the derivative component were done assuming a fast enough sample rate to ensure that the feedback variable had a monotonic slope with no inflection points (Appendix A). Using a step function as an input it is obvious that this criterion is no longer met, thereby invalidating all previous derivative calculations. Monotonicity can be restored by expanding the step over the entire sample period (figure 18). Using this modified step function as an input, the effect of derivative gain on the system response was recorded in figure 19.



MODIFIED UNIT STEP INPUT

FIGURE 18

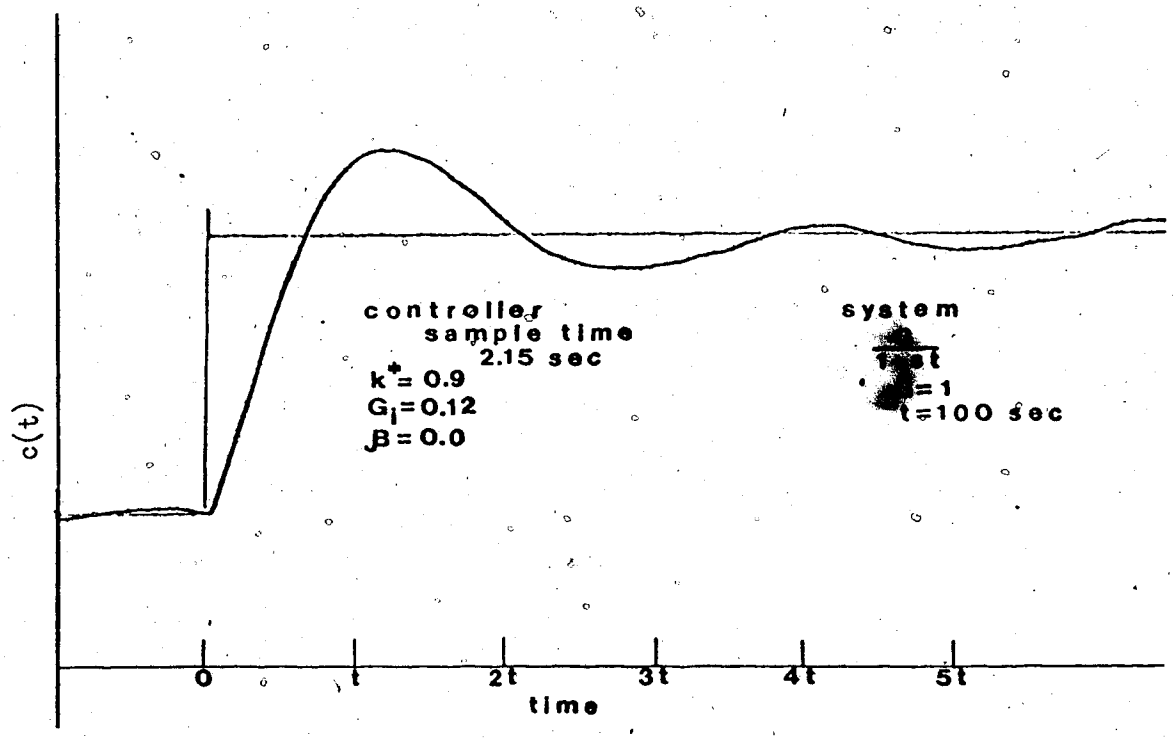


EFFECT OF THE DERIVATIVE TERM

FIGURE 19

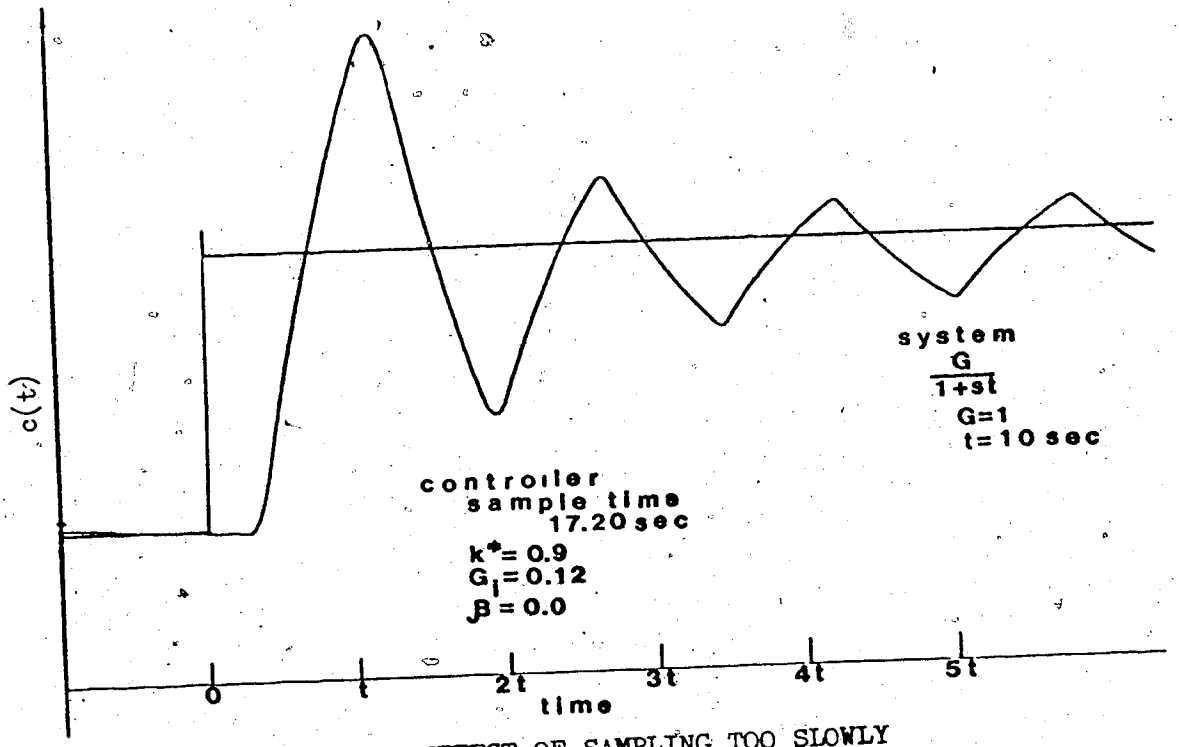
Series C (sample time)

This series of tests demonstrates the well documented results[1] obtained by varying the sample time. The results are shown in figures 21 - 24.



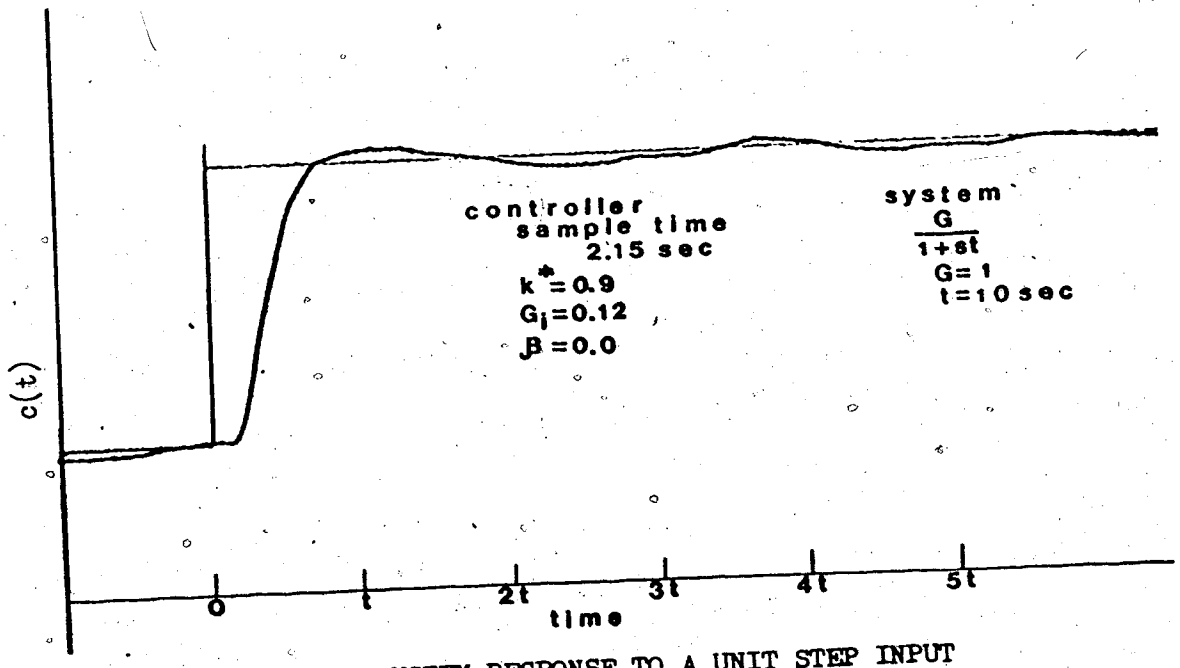
EFFECT OF SAMPLING TOO FAST

FIGURE 21



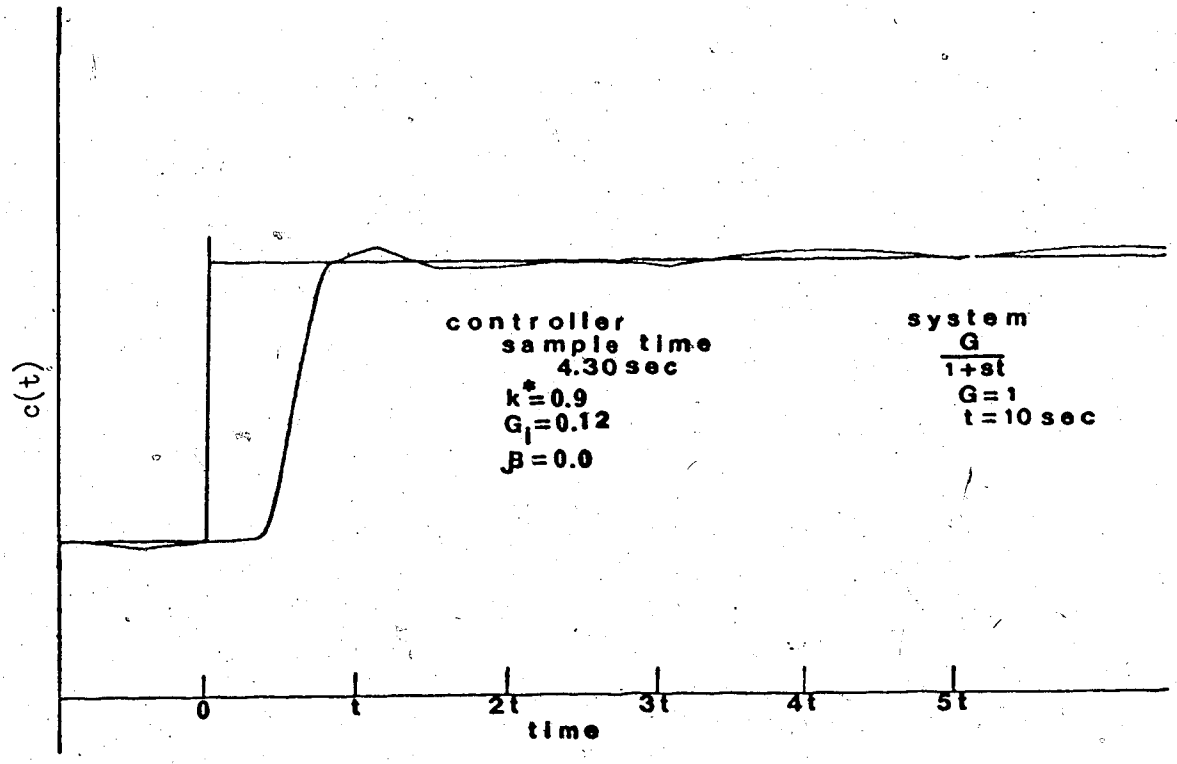
EFFECT OF SAMPLING TOO SLOWLY

FIGURE 22



SYSTEM RESPONSE TO A UNIT STEP INPUT

FIGURE 23



SYSTEM RESPONSE TO A STEP INPUT

FIGURE 24

Chapter 6

DISCUSSION

Series A

Figure 15 is a comparison of the optimum digital and analog controller responses to a unit step disturbance. There are two obvious differences, namely: the response delay and the steady state quantization error of the digital controller, both of which were anticipated. Since the curves are virtually identical except for the delay, it is interesting to compare the digital and analog gains for the components.

Proportional Gain

for the digital controller

$$K^* = 0.9 \tag{6.1}$$

from Appendix D

$$K = 4K^* \qquad K = 3.6 \tag{6.2}$$

for the analog controller

$$K = 4.0 \tag{6.3}$$

Integral Gain

for the digital controller

$$G_i = 0.12 \tag{6.4}$$

from Appendix D

$$\frac{G_i}{t} = \frac{1}{T_i} = \frac{0.12}{2.15} = 0.056 \text{ rep/sec} \tag{6.5}$$

for the analog controller

$$\frac{1}{T_i} = \frac{1}{6.6} = 0.151 \text{ rep/sec} \tag{6.6}$$

Derivative Gain

for the digital controller

$$\beta = 0.0 \tag{6.7}$$

from Appendix D

$$T_d = \beta/\beta^* = 0.0 \text{ sec} \tag{6.8}$$

for the analog controller

$$T_d = 0.1 \text{ sec} \tag{6.9}$$

Theoretically $T_d = 0.0$ seconds for optimal control of a first order lag process, however, due to the configuration of the analog simulation (Appendix E) this was impossible to achieve (required infinite gain). Typical analog derivative times range from 0.6 to 1500 seconds, therefore, $T_d = 0.1$ seconds may be considered zero derivative gain.

The apparently large discrepencies in the proportional and integral terms are easily explained by considering the operation of the digital controller. The control equation was shown to be

$$\Theta_s - \Theta_{s-1} = K\left[(c_{s-1} - c_s) + \frac{\Delta t}{T_i}(r_s - c_s) + \frac{T_d}{\Delta t}(\Delta c_{s-1} - \Delta c_s)\right] \tag{6.10}$$

which gives an output correction dependent on gains of the various

components. However, using a sample rate several times faster than the system response time causes further corrections to be made before the system can respond fully to the original. This results in a pseudo gain being obtained from the sampling rate. Therefore, the gains recorded for the digital controller are somewhat lower than the corresponding analog gain as expected. This pseudo gain is a function of both the sample time and the system time constant and is difficult to compute analytically. Further verification is obtained by considering figure 21. The response curve obtained from an excessive sampling rate is identical to the response curve which would be obtained from an analog controller with significantly higher gains.

Recall from Appendix D, that to maintain the steady state deviation within the desired error bounds, the minimum integral gain was limited to $G_i = 0.25$. The integral gain was increased to this value and the unit step response recorded (figure 16). We note that the transient response shows some deterioration, however, it is now ensured that the steady state quantization error is within the limits calculated earlier ($\pm$ 0.05v). An added advantage of using the higher integral gain is the improved setpoint response as described below.

Another important aspect of the controller operation can be demonstrated by considering the control equation.

$$\theta_s - \theta_{s-1} = K \left[(c_{s-1} - c_s) + \frac{\Delta t}{T_i} (r_s - c_s) + \frac{T_d}{\Delta t} (\Delta c_{s-1} - \Delta c_s) \right] \qquad (6.11)$$

If a setpoint change, rather than a change in the feedback variable is produced, this equation reduces to

$$\theta_s - \theta_{s-1} = K\left[\frac{\Delta t}{T_i}(r_s - c_s)\right] \qquad (6.12)$$

This equation results in a response that is less than optimum as shown in figure 17. If the response to a setpoint change is critical the algorithm must be changed to compensate for this. Mergler et al[5] have developed such an algorithm for a two mode controller. The development of an equivalent three mode modified algorithm is beyond the scope of this thesis. From the controller timing diagram (figure 8) we note that a step disturbance occurring in the t_7 to t_1 time period will also result in the modified control equation (equation 6.12) being implemented. Because the occurrence of the disturbance is random, the ratio of the t_7 to t_1 period to the total period limits the possibility of a miss to 12%. Since the controller will be in a physical environment with time constants in the order of seconds, a disturbance with a rise time of 0.26 seconds (required to cause a miss) will be extremely rare. However, if a miss does occur the results will not be catastrophic, merely a response that is less than optimum.

Series B

The effect of the derivative term on the control of a second order system can be readily evaluated from figure 19, which shows the response with no derivative term compared with the response for $T_d = 0.8$ seconds (β=3.0). Because the derivative term obtains its effect from the curvature of the sampled signal, the linear input

(modified step) during the first sample period results in no improvement during this time. However, from the second sample period onward the effect of the derivative term is obvious. Note that the addition of the derivative term causes an oscillatory steady state which was not present in the first order system. Since the oscillation lies within the expected quantization error discussed previously ($\pm$ 0.05v), this characteristic is not serious. Because of the nature of the controller, the derivative term will be effective for disturbances with rise times in the order of seconds or longer. For disturbances with faster rise times it can be shown, by considering the controller operation, that the derivative term will add a proportional gain resulting in a response that is less than optimum. Since the controller would be expected to operate in a process environment where short rise time disturbances are rare or nonexistent, the controller performance will not be affected.

Series C

This series of graphs demonstrates the effect of sampling rate on controller performance. Figure 21 and 22 show the results of sampling too fast and too slowly respectively. Figures 23 and 24 show the changes in response by decreasing the sample time by a factor of 2.

The curves are almost self explanatory. A fast sample rate tends to over correct for each error because the system does not have time to respond to the previous correction before the next sample is taken. This produces an oscillatory effect much the same as produced by a high gain controller (This pseudo gain is a result of the sample rate as

discussed earlier.). Slow sampling allows the system to deviate a large amount before a correction is made, yielding much the same type of oscillatory result.

The slower sample rate of figure 24 compared to figure 23, results in more delay but still yields an acceptable response.

Chapter 7

CONCLUSION

As mentioned in the introduction the main objectives of this thesis were three-fold: combine the three control signals into a composite control signal; provide added flexibility by employing a variable sample rate and probably the most important, verify the curve deflection measurement as a derivative control term. From the test results it can be concluded that these objectives were achieved with a degree of success.

Throughout the tests, any response deterioration was attributable to either the steady state quantization error or the sample rate. Because these factors are the common denominator in performance limitations, it is beneficial to examine them in more detail. Recall that the output quantization error was shown to depend on both the step size and the potentiometer used on the output. Therefore, either reducing the step size or changing the potentiometer from a single to a multi-turn will reduce the error. Changing the potentiometer with corresponding changes in gain and stepper input frequency will provide the easiest method to improve the steady state error.

Although the recorded tests were made using a system time constant of ten seconds as a typical value, fairly acceptable response was obtained for time constants down to four seconds. Operation in environments with time constants below this value would have to be accomplished by a reduction in the controller sample time. Since it was shown that the sample time is a function of the voltage controlled

oscillator range, an increase in the output range of the oscillator will reduce the sample time. An excellent voltage controlled oscillator replacement candidate is the Hybrid Systems Model 610, which would replace the original 10k hertz range with a range of up to 100k hertz.

Making the above modifications coupled with some hardware logic simplifications, would produce a cheap high performance digital three mode controller for process control applications.

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Appendix A

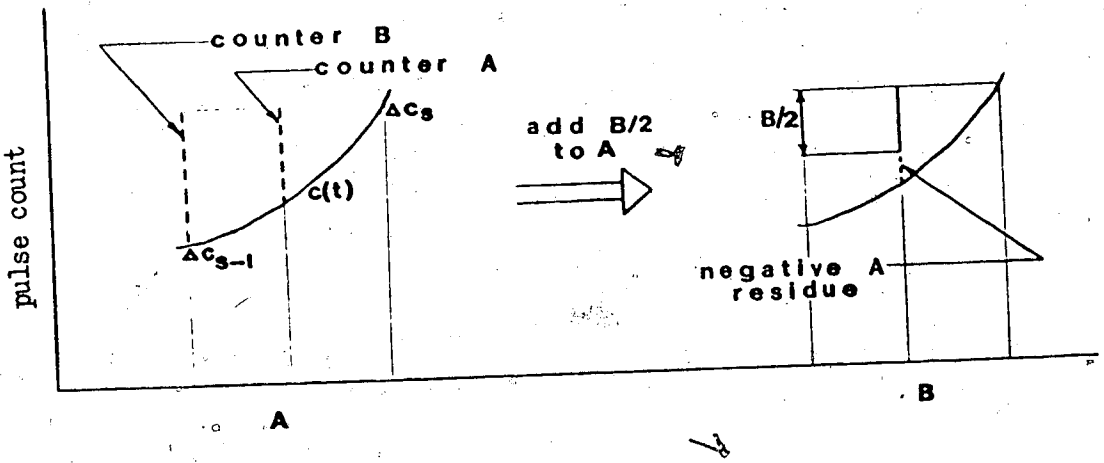
ACCELERATION TERM JUSTIFICATION

As mentioned in the theoretical portion of the paper, a unique relationship exists between the residues of counters A and B and the magnitude and direction of the acceleration term. This can be confirmed by considering all possible combinations of velocity and acceleration as shown in figures A-1 and A-2.

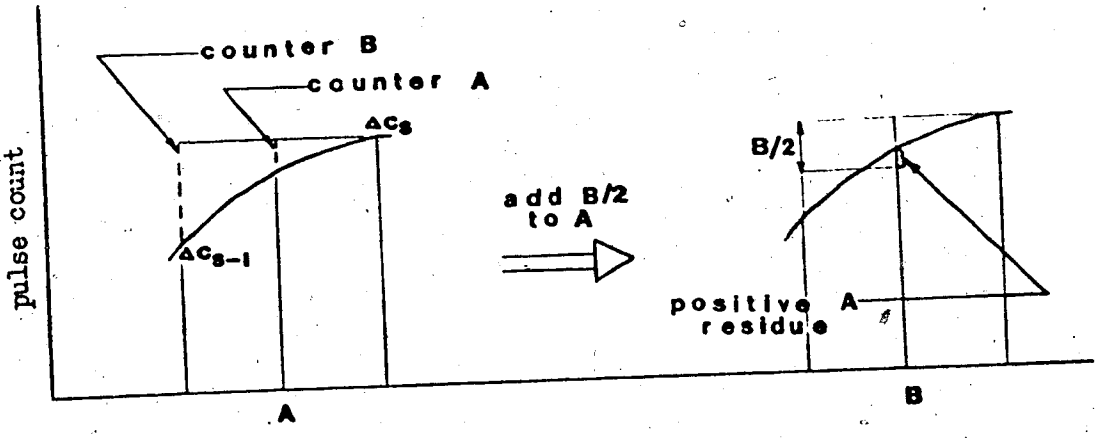
* Note on figures A-1 and A-2.

- dashed lines represent negative counter residues
- figure A in each case shows counter residues after time period # 6
- figure B in each case shows counter A residue after time period # 7

CASE 1 Velocity positive $(\Delta C_{s-1} - \Delta C_s)$ negative



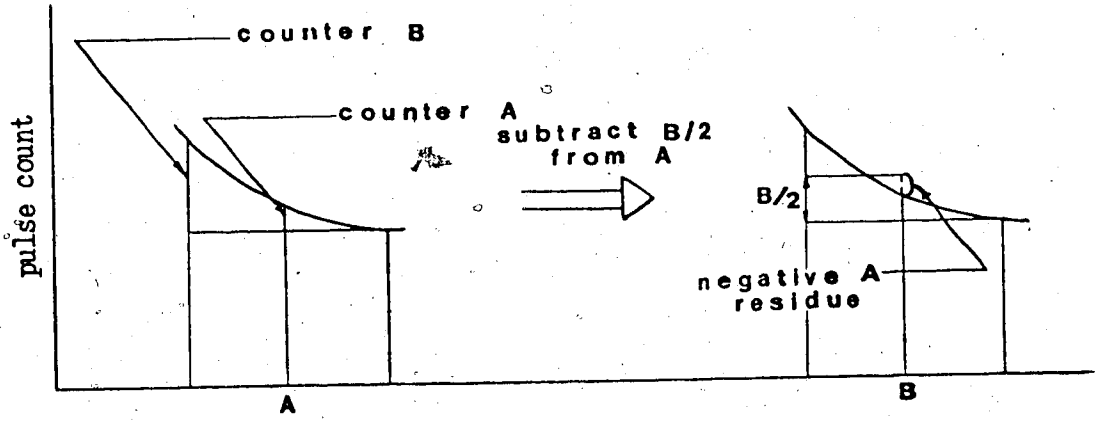
CASE 2 Velocity positive $(\Delta C_{s-1} - \Delta C_s)$ positive



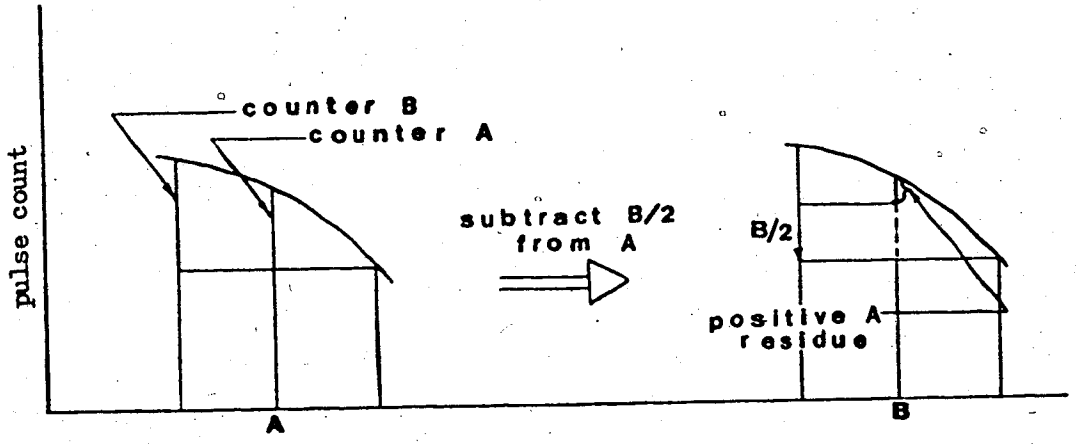
ACCELERATION TERM JUSTIFICATION

FIGURE A-1

CASE 3 Velocity negative $(\Delta C_{s-i} - \Delta C_s)$ negative



CASE 4 Velocity negative $(\Delta C_{s-i} - \Delta C_s)$ positive



ACCELERATION TERM JUSTIFICATION

FIGURE A-2

Summary (Figures A-1 and A-2)

- add B/2 to A for negative residue in counter A

- subtract B/2 from A for positive residue in counter A

Then the sign of the residue remaining in counter A is identical to the sign of the term $(\Delta c_{s-1} - \Delta c_s)$.

Appendix B

CALCULATION OF INPUT QUANTIZATION ERROR

The analog to digital conversion is accomplished by counting the voltage controlled oscillator frequency for a specified time.

$$\text{count} = f_{vco} \cdot T \tag{B.1}$$

The counter resolution determines the quantization error as a result of converting. Using a voltage controlled oscillator with 10 to 10k hertz output for a 0 to 10v input, consider an aperture time of 0.01 seconds.

$$\text{minimum count} = 1 \tag{B.2}$$

$$1 = f_{vco} \cdot 0.01 \text{ sec} \tag{B.3}$$

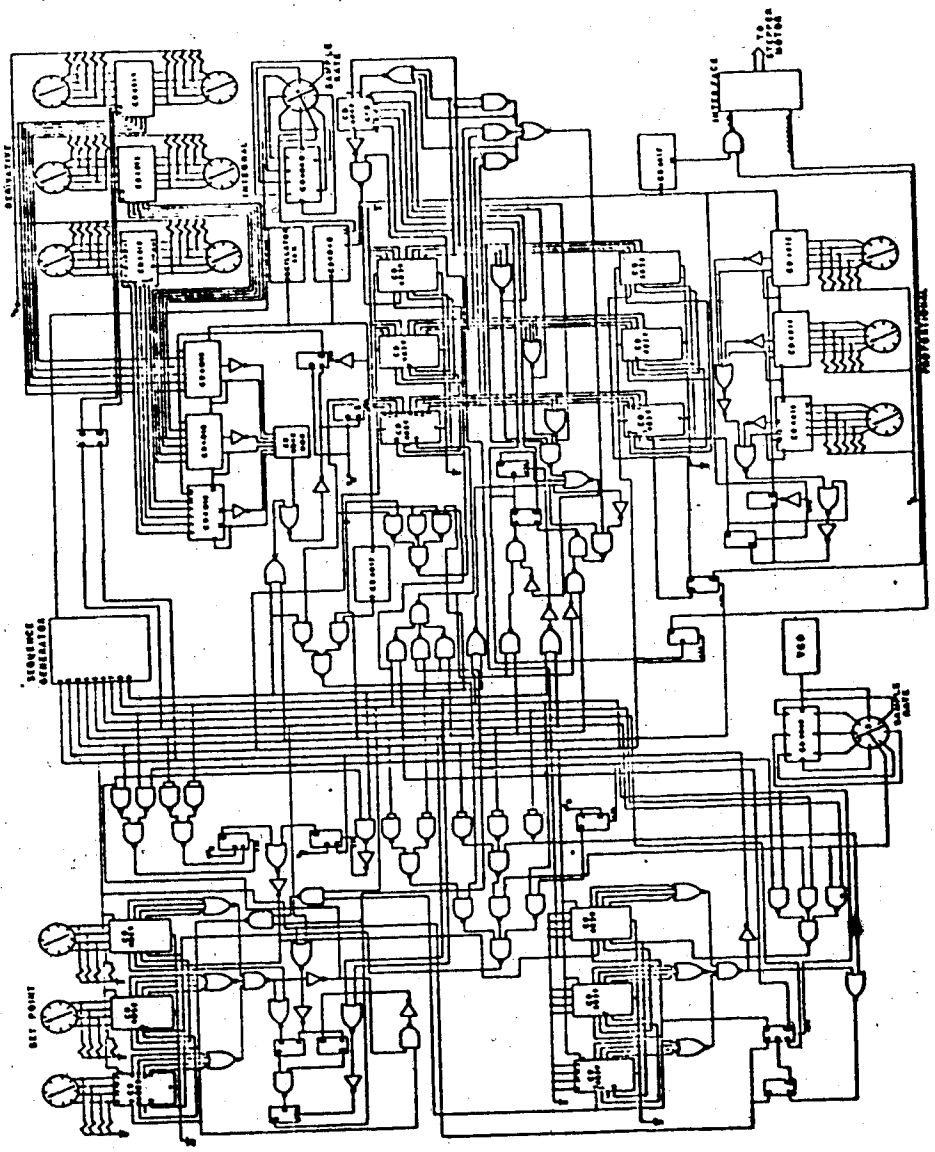
$$f_{vco} = 100 \text{ hertz} \tag{B.4}$$

Therefore a frequency variation of less than 100 hertz will go undetected. This corresponds to an input excursion of 0.1v. Extending the above, it is obvious that an aperture time of 0.08 seconds yields an input uncertainty of 0.0125v. Because up/down counters are used the possibility of either count occurring exists. Therefore, the input uncertainty limit for an aperture time of 0.08 seconds is extended to $\pm$ 0.0125v.

Appendix C

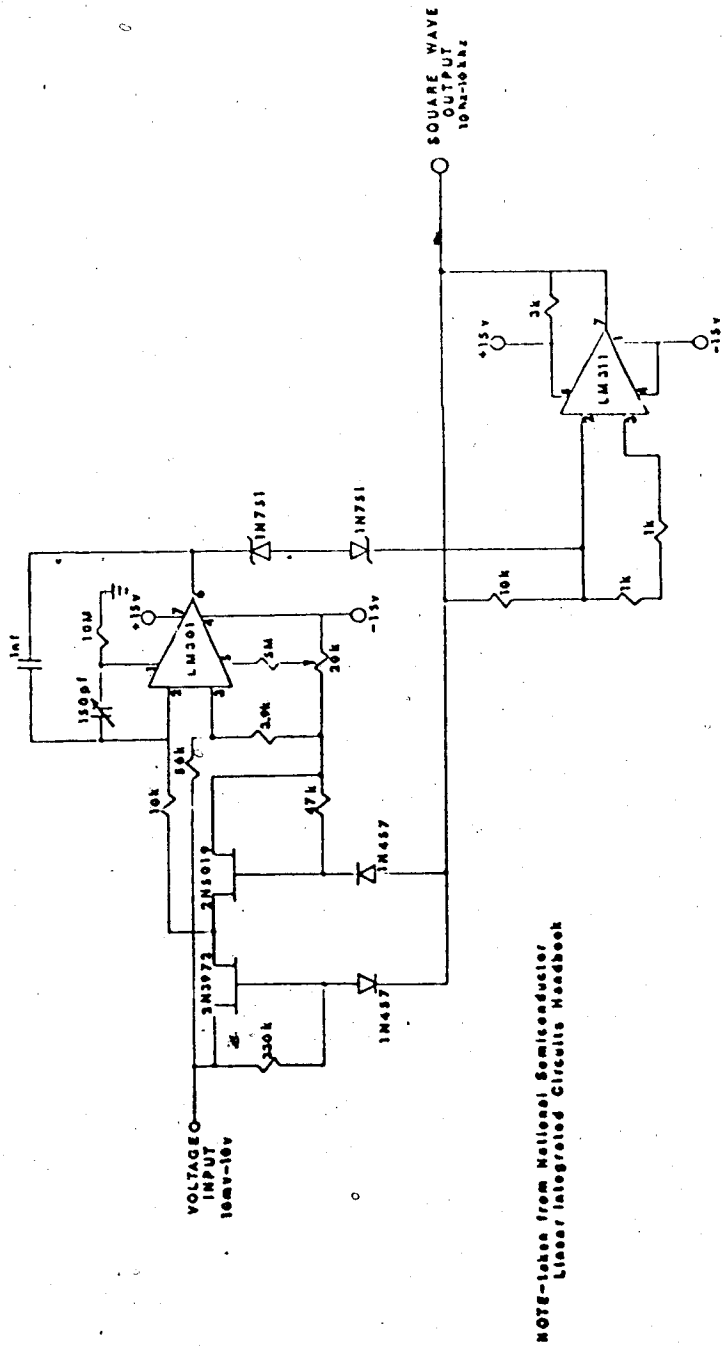
SCHEMATIC DRAWINGS

The following four figures are the complete schematic drawings of the components used in the controller construction.



CONTROLLER SCHEMATIC

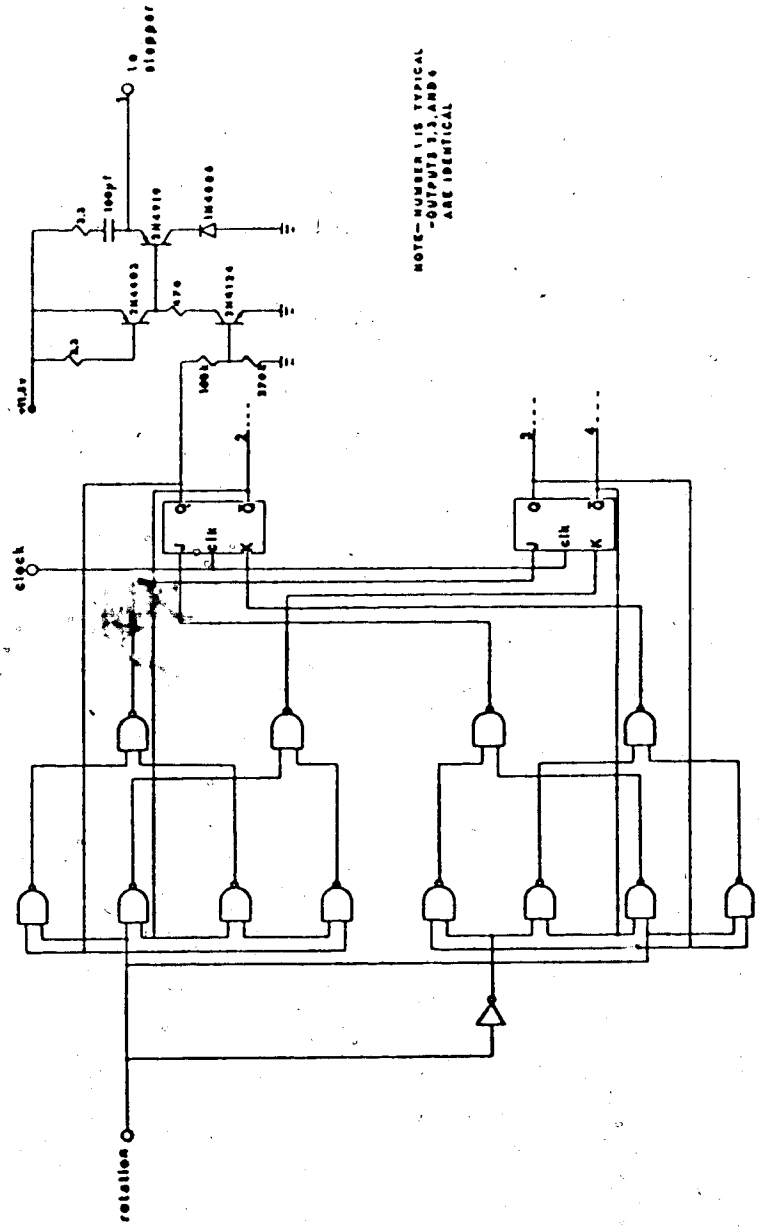
FIGURE C-1



VOLTAGE CONTROLLED

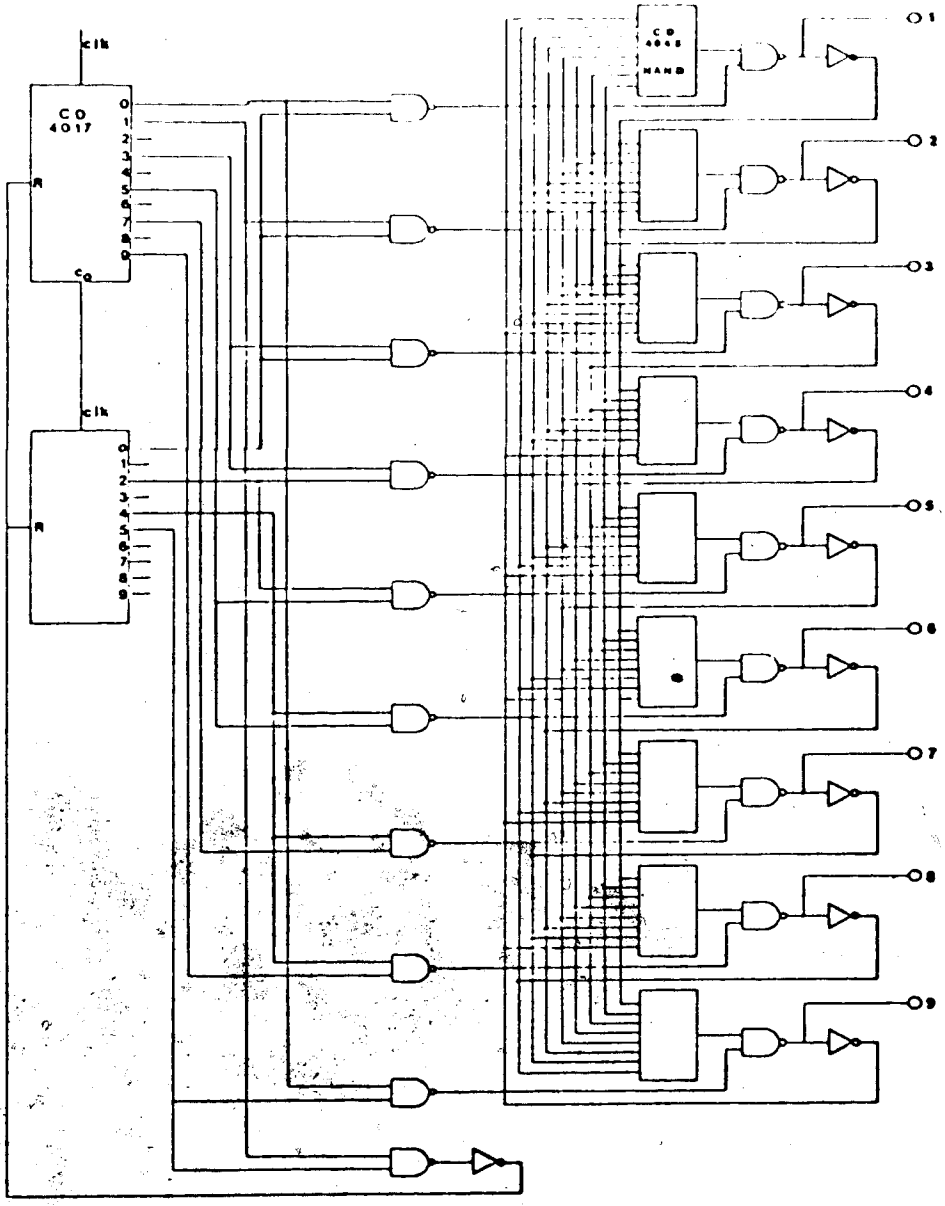
OSCILLATOR SCHEMATIC

FIGURE C-2



STEPPER MOTOR INTERFACE SCHEMATIC

FIGURE C-3



SEQUENCE GENERATOR SCHEMATIC

FIGURE C-4

Appendix D

CALCULATION OF

THEORETICAL GAINS

From the theoretical section, the control equation was obtained.

$$\theta_s - \theta_{s-1} = K\left[(c_{s-1} - c_s) + \frac{\Delta t}{T_i}(r_s - c_s) + \frac{T_d}{\Delta t}(\Delta c_{s-1} - \Delta c_s)\right] \quad (D.1)$$

Proportional Gain K

The total proportional gain consists of the fixed gains from the voltage controlled oscillator and stepper motor and an adjustable gain K^* to allow adjustment of K.

$$K = K^* K_s K_{vco} \quad (D.2)$$

K_s = stepper gain

K_{vco} = VCO gain

Using a 1.8^o /pulse stepper coupled to a one turn potentiometer, one pulse yields $\frac{1}{200}$ or 0.05v.

$$K_s = 0.05\text{v/pulse} \quad (D.3)$$

Considering the voltage controlled oscillator with an aperture time of 0.08 seconds.

$$K_{vco} = 1000 \frac{\text{pulse}}{\text{volt sec}} \cdot 0.08 \text{ sec} \quad (D.4)$$

$$K_{vco} = 80 \text{ pulse/volt} \quad (D.5)$$

$$K = 0.05 \text{ volt/pulse} \bullet 80 \text{ pulse/volt} \bullet K^* \tag{D.6}$$

$$K = 4K^* \tag{D.7}$$

From typical analog data

$$K_{min} = 0.3 \tag{D.8}$$

$$K_{max} = 50.0 \tag{D.9}$$

Yielding

$$K^*_{min} = 0.07 \tag{D.10}$$

$$K^*_{max} = 12.5 \tag{D.11}$$

To improve the resolution $10K^*$ was used as the input switch setting (see multiplier construction).

Integral Gain

From equation (D.1) the required integral gain is $\frac{\Delta t}{T_i}$. From previous calculations (see chapter 4) a sample time of approximately two seconds was indicated. For convenience in the sequence generator construction, a sample time of 2.15 seconds was used.

From typical analog controller data

$$T_{i\ max} = 1500 \text{ sec/repeat} \tag{D.12}$$

$$T_{i\ min} = 0.6 \text{ sec/repeat} \tag{D.13}$$

These values yield the following gains

$$G_{i\ min} = \frac{\Delta t}{T_{i\ max}} = \frac{2.15}{1500} = 1^{\circ}.43 \cdot 10^{-3} \qquad (D.14)$$

$$G_{i\ max} = \frac{\Delta t}{T_{i\ min}} = \frac{2.15}{0.6} = 3.6 \qquad (D.15)$$

As shown in the implementation section, the setpoint deviation is determined as part of the integral term. Obviously reducing the integral term to a near zero value will allow wide deviations from the setpoint to occur. Consistent with the expected output accuracy, detection and subsequent corrective action for setpoint deviations as small as 0.05v is desired. Using an aperture time of 0.08 seconds, this deviation yields a counter residue of 4. Since the minimum detectable count after multiplication is 1, the minimum gain is limited to 0.25. Therefore, the modified gain limits are

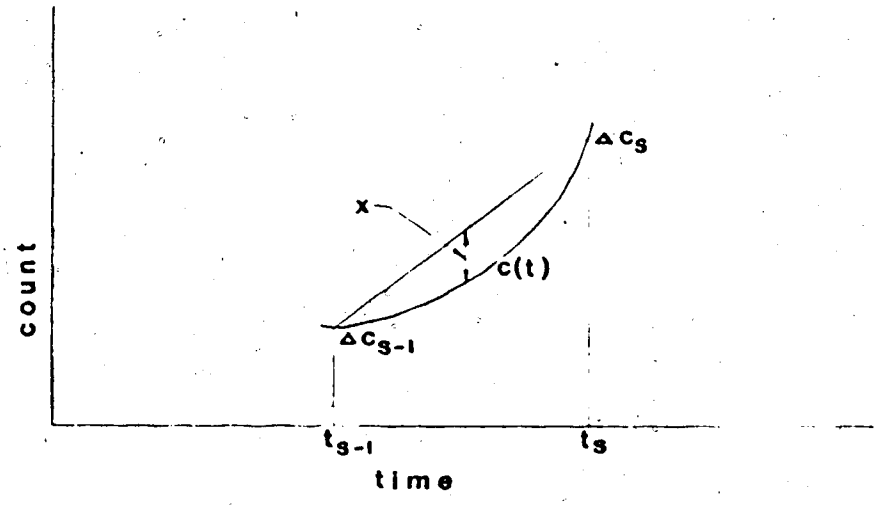
$$G_{i\ min} = 0.25 \qquad (D.16)$$

$$G_{i\ max} = 3.6 \qquad (D.17)$$

To increase resolution, 10 G_i was used as the input switch setting (see multiplier construction).

Derivative Gain

From equation (D.1) the derivative term is $\frac{T_d}{\Delta t}(\Delta c_{s-1} - \Delta c_s)$. As mentioned in the theoretical section, this term would not be evaluated directly but rather the value "x" shown below would be used.



DEFLECTION MEASUREMENT

FIGURE D-1

Appendix A showed the sign relationship between "x" and $(\Delta c_{s-1} - \Delta c_s)$. The magnitude relationship remains to be found.

$$\beta \left| x \right| = \frac{T_d}{\Delta t} \left| \Delta c_{s-1} - \Delta c_s \right| \qquad (D.18)$$

where β is to be determined

For convenience in evaluation set $T_d = 1$ second

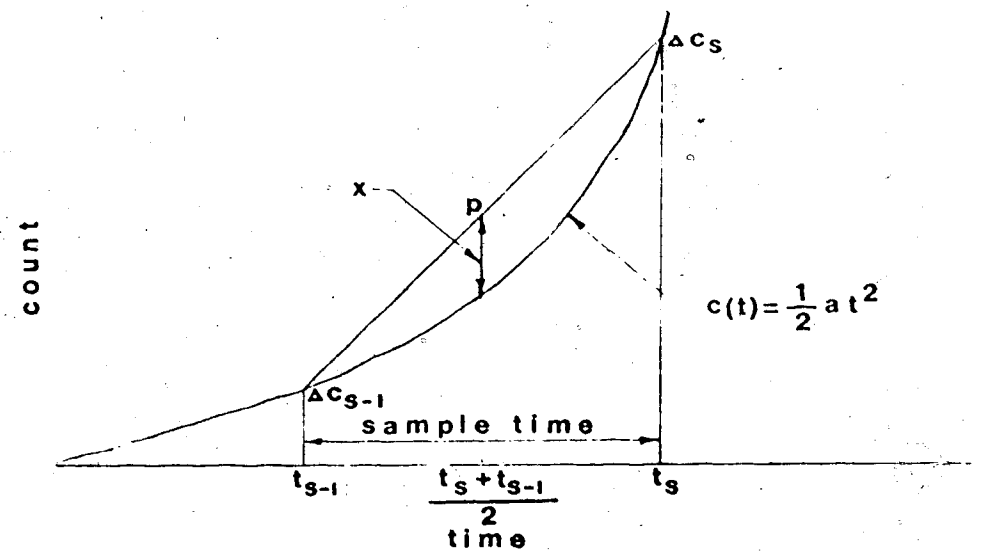
then

$$\beta^* \left| x \right| = \left| \frac{\Delta c_{s-1} - \Delta c_s}{\Delta t} \right| \qquad (D.19)$$

$$\beta = T_d \cdot \beta^* \qquad (D.20)$$

Consider a constant acceleration curve of the form

$$c(t) = \frac{1}{2} a t^2 \qquad (D.21)$$



DERIVATIVE TERM EVALUATION

FIGURE D-2

Determine the difference in slopes.

$$\left| \frac{\Delta c_{s-1} - \Delta c_s}{\Delta t} \right| = \left| d \left. \frac{c(t)}{dt} \right|_{t=s-1} - d \left. \frac{c(t)}{dt} \right|_{t=s} \right| \qquad (D.22)$$

From (D.21)

$$d \frac{c(t)}{dt} = at \qquad (D.23)$$

$$\left| \frac{\Delta c_{s-1} - \Delta c_s}{\Delta t} \right| = \left| a(t_{s-1} - t_s) \right| \qquad (D.24)$$

Determine $|x|$

$$|x| = \left| p - c(t) \Big|_{t = \frac{t_s + t_{s-1}}{2}} \right| \tag{D.25}$$

$$|x| = \left| \frac{c(t)\Big|_{t=s} + c(t)\Big|_{t=s-1}}{2} - c(t)\Big|_{t = \frac{t_s + t_{s-1}}{2}} \right| \tag{D.26}$$

$$|x| = \left| \frac{\frac{1}{2} a t_s^2 + \frac{1}{2} a t_{s-1}^2}{2} - \frac{1}{2} a \left(\frac{t_s + t_{s-1}}{2} \right)^2 \right| \tag{D.27}$$

$$|x| = \left| \frac{1}{4} a \left(t_s^2 + t_{s-1}^2 \right) - \frac{1}{8} a \left(t_s + t_{s-1} \right)^2 \right| \tag{D.28}$$

$$|x| = \left| \frac{a}{8} (t_{s-1} - t_s)^2 \right| \tag{D.29}$$

Substituting equations (D.24) and (D.29) into (D.19)

$$\beta^* \left| \frac{a}{8} (t_{s-1} - t_s)^2 \right| = \left| a(t_{s-1} - t_s) \right| \tag{D.30}$$

$$\beta^* = \frac{8}{|t_{s-1} - t_s|} = \frac{8}{t_s - t_{s-1}} \tag{D.31}$$

Using a sample time of 2.15 seconds

$$\beta^* = 3.72 \tag{D.32}$$

From typical analog controller data

$$T_{d\ max} = 1500 \text{ seconds} \tag{D.33}$$

$$T_{d\ min} = 0.6 \text{ seconds} \tag{D.34}$$

From equation (D.20)

$$\beta = T_d \cdot \beta^*$$

$$\beta_{max} = 1500 \quad 3.72 = 5580 \tag{D.35}$$

$$\beta_{min} = 0.6 \quad 3.72 = 2.23 \tag{D.36}$$

Appendix E

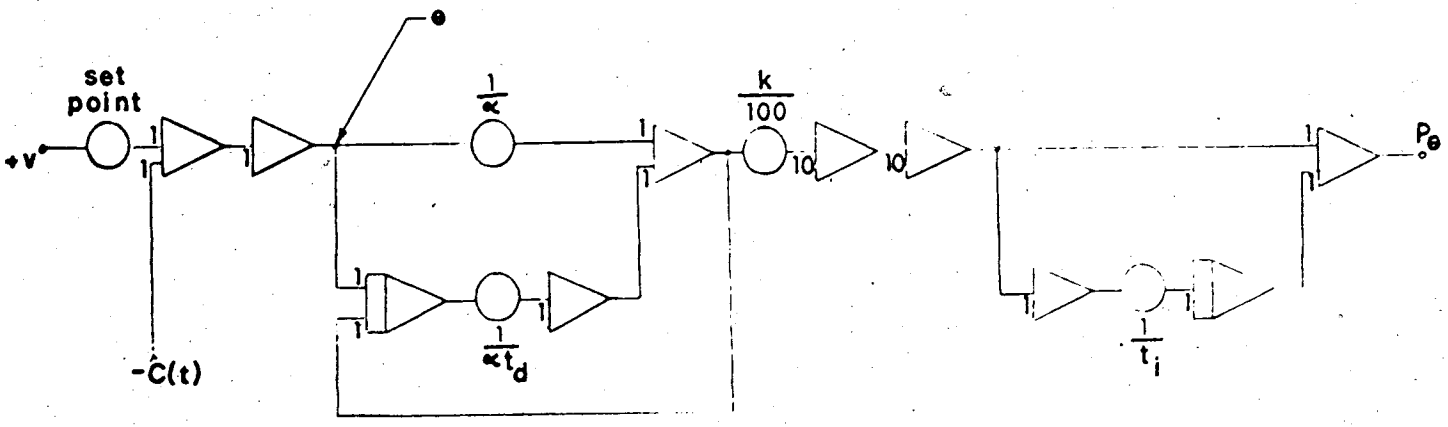
ANALOG COMPUTER DIAGRAMS

The following two figures represent the analog computer simulations for both the analog controller and the system (control valve) used in this thesis.

ANALOG CONTROLLER*

$$\frac{P_\theta}{\theta} = k\left(1 + \frac{t_d}{t_i}\right) + \frac{k}{t_i s} + k t_d s$$

$\alpha = 10$



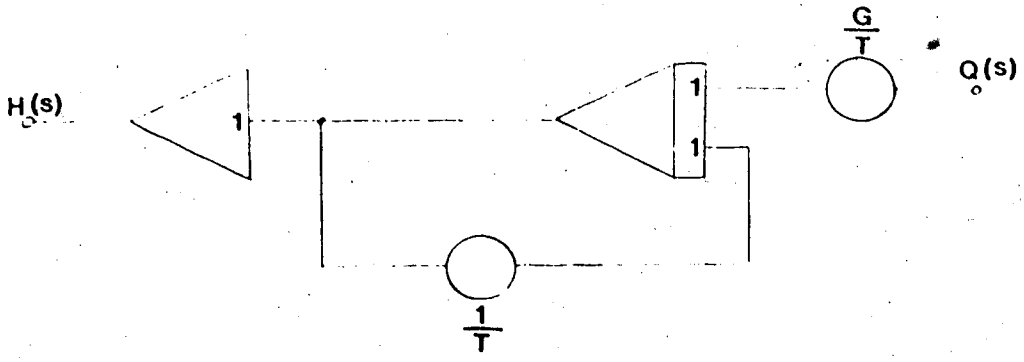
* taken from Analog Computation in Engineering Design[17]

ANALOG CONTROLLER SIMULATION

FIGURE E-1

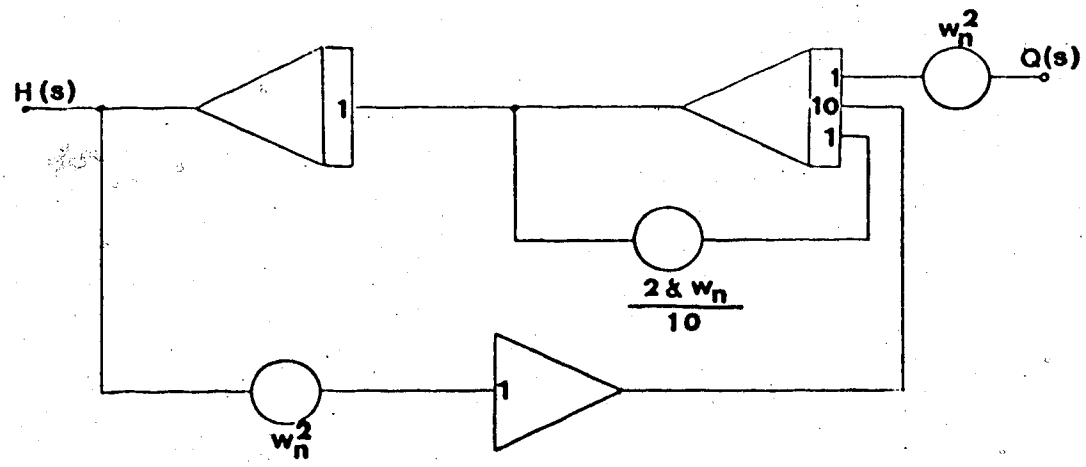
SERIES A - FIRST ORDER LAG

$$\frac{H(s)}{Q(s)} = \frac{G}{1 + Ts}$$



SERIES B - SECOND ORDER LAG

$$\frac{H(s)}{Q(s)} = \frac{w_n^2}{s^2 + 2\&sw_n + w_n^2}$$



CONTROL VALVE SIMULATIONS

FIGURE E-2