Real-Time Electromagnetic Transient Hardware Emulation of Multi-Terminal
High Voltage DC Grid

by

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Abstract

New high voltage DC (HVDC) transmission projects are being increasingly operated globally, which can be developed into multi-terminal DC (MTDC) grid interconnecting the conventional AC grid and the off-shore renewable energy power plants. Among various power converter topologies, modular multi-level converter (MMC) has the features of providing very low harmonics and low switching frequency, which is specifically focused on in this work. Real-time electromagnetic transient (EMT) simulation is a powerful tool for the transient study and analysis of the DC grid, and for the design and verification of the control and protection systems. Field Programmable Gate Arrays (FPGAs) and Multi-Processor System-on-Chip (MPSoC) devices, which have highly parallel hardware architectures, are used for the real-time emulation systems developed in this work.

This thesis focuses on the off-line and real-time simulation of the multi-terminal high voltage DC grid, and contributes on the aspects of EMT simulation technique, MMC modeling scheme, DC grid modeling scheme, and hardware implementation method. Variable time-stepping schemes combined with nonlinear element solution schemes have been applied to FPGA-based real-time simulation of power electronics circuit and power system circuit for the first time. This work proposes the datasheet based device-level electrothermal model for the MMC containing half-bridge sub-module (HBSM) and clamp double sub-module (CDSM). Such a model can increase the simulation accuracy and provide the detailed device-level thermal data and switching transient waveforms for the efficiency and safety evaluation of the control and protection scheme during normal operation and contingency. The comprehensive simulation of the AC/DC grid, which is composed of CIGRÉ DC grid test system, IEEE 39-bus AC system and the wind farms is presented with hybrid modeling scheme. Finally, the thesis develops and presents the detailed implementation of real-time emulation of the CIGRÉ DC grid test system for the hardware-in-the-loop (HIL) test on MPSoC-FPGA platform.

Preface

The material presented in this thesis is based on original work by Zhuoxuan Shen. As detailed in the following, material from some chapters of this thesis has been published in conference proceedings and as journal articles under the supervision of Dr. Venkata Dinavahi in concept formation and by providing comments and corrections to the article manuscript.

Chapter 3 includes the results from the following paper:

- Z. Shen and V. Dinavahi, "Dynamic variable time-stepping schemes for real-time FPGA-based nonlinear electromagnetic transient emulation," *IEEE Trans. Ind. Electron.,* vol. 64, no. 5, pp. 4006-4016, May 2017.

Chapter 4 includes the results from the following paper:

- Z. Shen and V. Dinavahi, "Real-time device-level transient electrothermal model for modular multilevel converter on FPGA," *IEEE Trans. Power Electron.,* vol. 31, no. 9, pp. 6155-6168, Sept. 2016.

Chapter 5 includes the results from the following paper:

- Z. Shen and V. Dinavahi, "Real-time MPSoC-based transient simulation of fault tolerant MMC topology" *Submitted to IEEE Trans. Power Delivery*, pp. 1-8, Feb. 2018, (TPWRD-00183-2018).

Chapter 6 includes the results from the following papers:

- Z. Shen and V. Dinavahi, "Comprehensive electromagnetic transient simulation of AC/DC grid with multiple converter topologies and hybrid modeling schemes," *IEEE Power Energy Technology Syst. J.,* vol. 4, no. 3, pp. 40-50, Sept. 2017.

- Z. Shen, N. Lin and V. Dinavahi, "Electromagnetic transient simulation of CIGR DC grid test system with hybrid converter topologies," *IEEE Power & Energy Society General Meeting,* Chicago, IL, Jul. 2017, pp. 1-5.

Chapter 7 includes the results from the following paper:

- Z. Shen, T. Duan and V. Dinavahi, "Design and implementation of real-time MPSoC-FPGA based electromagnetic transient emulator of CIGRÉ DC grid for HIL application," *Submitted to IEEE Power Energy Technology Syst. J.,* pp. 1-10, May 2018, (PETSJ-00033-2018).

To my parents and my fiancée,
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List of Acronyms

AC   Alternating Current
APU   Application Processing Unit
ASIC   Application Specific Integrated Circuit
ATP   Alternative Transients Program
AVM   Average Value Model
AXI   Advanced eXtensible Interface
BLM   Bergeron Line Model
BRAM   Block Random Access Memory
CDSM   Clamp Double Sub-Module
CLB   Configurable Logic Blocks
CPU   Central Processing Unit
DAC   Digital to Analog Converter
DDR4   Double Data Rate Fourth-generation
DSP   Digital Signal Processing (Processor)
DUT   Device-Under-Test
EMT   Electro-Magnetic Transient
FACTS   Flexible Alternating Current Transmission System
FBSM   Full-Bridge Sub-Module
FF   Flip-Flop
FFT   Fast Fourier Transform
FIFO   First-In First-Out
FMC   FPGA Mezzanine Card
FPGA   Field-Programmable Gate Array
FPU   Floating Point Unit
FSM   Finite State Machine
GPIO   General Purpose IO
GPU   Graphical Processing Unit
GT   Gigabit Transceiver
HBSM   Half-Bridge Sub-Module
HIL   Hardware-In-the-Loop
HLS   High-Level Synthesis
HVDC   High Voltage Direct Current
I/O   Input/Output
IGBT   Insulated Gate Bipolar Transistor
JTAG   Joint Test Action Group
LTE   Local Truncation Error
LUT   Look-up Table
MMC   Modular Multi-Level Converter

MPSoC	Multi-Processor System-on-Chip
MTDC	Multi-Terminal DC
NLC	Nearest Level Control
NPC	Neutral-Point-Clamped
N-R	Newton-Raphson
PD	Phase-Disposition
PL	Programmable Logic, Piecewise Linearization
PLL	Phase Locked Loop
PNR	Piecewise Newton-Raphson
PS	Processing System
PSC	Phase-Shifted Carrier
PSM	Programmable Switch Matrix
PWM	Pulse Width Modulation
QSFP	Quad Small Form-Factor Pluggable
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RPU	Real-Time Processing Unit
RTL	Register-Transfer Level
SDK	Software Development Kit
SFP	Small Form-Factor Pluggable
SM	Sub-Module
SPWM	Sinusoidal Pulse Width Modulation
ULM	Universal Line Model
USB	Universal Serial Bus
VHDL	Very High-Speed Integrated Circuit Hardware Description Language

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Introduction

HVDC transmission has the advantage of low energy loss, low overall investment, greater controllability, high capacity long distance power transmission capability for the future power grid upgrading [1–10]. Many multi-terminal HVDC projects can be further connected either by DC/DC converters or AC systems creating a meshed DC grid. The DC transmission system offers an efficient solution to transfer the energy from the remote off-shore renewable sources to the conventional AC grid, which composes the modern AC/DC grid. The complexity of the large-scale AC/DC system makes the control and protection a significant challenge to ensure the steady-state and safe operation under different contingencies, such as DC and AC faults. Detailed electromagnetic transient (EMT) simulation is necessary to study and analyze the transient phenomena of the AC/DC system [11–17]. During last decades, various AC-DC converter topologies have been developed. Among them, the modular multi-level converter (MMC) has raised great attention and has been used in HVDC projects due to its low harmonics, low switching frequency, and good scalability [18–26]. The complex topology of MMC, which contains numerous sub-modules (SMs) with various structures, imposes the challenges for the efficient and accurate modeling and simulation.

Real-time electromagnetic transient simulation is a powerful tool for the hardware-in-the-loop (HIL) test of the corresponding control and protection systems and has strict requirements for computation capability. This thesis is focused on the development of the detailed and efficient modeling schemes for the MMC and conducting the real-time simulation of the multi-terminal high voltage DC containing MMCs. Field programmable gate arrays (FPGAs) containing substantial reconfigurable logic resources, can provide high parallel computing capability [27–29]. Multi-processor system-on-chip (MPSoC) integrates the FPGA resources and multi-core CPU in the same chip providing the fast sequential

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computing and high parallelism simultaneously [30]. Both FPGA and MPSoC are utilized for realizing the proposed modeling and simulation schemes and developing the real-time emulator for the DC grid.

In this thesis, the variable time-stepping schemes are explored for off-line and real-time simulation, and the device-level datasheet based electrothermal model for the half-bridge sub-module (HBSM) and the clamp double sub-module (CDSM) of MMC for real-time simulation are developed. This work conducts the off-line simulation of a complex AC/DC grid with hybrid modeling scheme, and develops the MPSoC-FPGA based real-time emulator for CIGRÉ DC grid test system. In this work, the term emulation is used for the design implemented on the hardware platform such as the FPGA or the MPSoC, which requires the digital circuit reconfiguration, while simulation is used as a general term regardless of the implementation platform. The following sections present the background information, literature review, motivations, objectives, and outlines of this work.

1.1 Background

1.1.1 Real-time Electromagnetic Transient Simulation

Electromagnetic transient simulation originating from Dr. H. W. Dommel's work is often used by power system engineers to study the electromagnetic transient phenomena, which are caused by switching event, short-circuit, lightning strike, etc [11, 31]. During the last few decades, more accurate and efficient models for power system equipment and power electronics devices have been developed, and the numerical solution schemes have been improved, which extend the functions and scopes of EMT-type simulation. For instance, the simulation can be used to verify the control and protection algorithm under the circumstance of communication failure or cyber attack. The simulated system can vary from conventional AC power system, HVDC and flexible alternating current transmission system (FACTS), microgrid system, power electronics circuits, etc. The simulation of the mechanical system, the thermal network and the magnetic field can potentially be either combined or interacted with the conventional EMT-type simulation. Such improvements and applications make EMT-type simulation not only useful for power system industry, but also for other industry sectors, such as automotive, aerospace, power electronics, etc.

Thanks to the rapid development of integrated circuit technology and computing science, the digital real-time EMT simulators have experienced fast development, which can be used in the HIL test. Such test is flexible, reliable and cost-effective before employing the equipment to the grid. Besides HIL test, real-time simulator is often used for academic research and operator training due to its fast and reliable performance. The usage of power electronics devices requires smaller time-step due to the high switching frequency and the high sampling frequency for HIL test. The complex topologies of MMC and the need for simulating large-scale AC/DC grid demand higher computing capability of the real-time

simulator. Therefore, extending the parallelism of the numerical algorithm and exploring feasible computing devices for high parallelism are critical for the development of the real-time simulators.

1.1.2 Modular Multi-Level Converter

The modular multi-level converter has various advantages over other conventional converter topologies, such as low harmonics, low switching frequency, high modularity, and good scalability [18–26]. It has been applied in medium and high voltage rating applications, including the HVDC system, industrial drive system, etc.

Fig. 1.1 presents the circuit topology of the MMC. The MMC contains 6 inverter arms, where each arm is composed by n identical sub-modules and an arm inductor L_m in series. There are various sub-module topologies existed, such as half-bridge SM, full-bridge SM, clamp double SM. The SM can seem as a switchable capacitor, which can be either bypassed, or inserted into the converter arm in series. Once inserted, the the capacitor voltage of the SM is contributed to the total DC voltage at the left side of Fig. 1.1. Assuming that the SM capacitor voltages are maintained around the rated value. The total number of the inserted SMs in a converter leg, which is composed of two converter arms in the same leg, is kept around n to maintain the relative steady DC side voltage. By using different combinations of the inserted SMs in the upper and lower arm of a phase, multiple voltage levels can be presented at the AC side of the converter. If the total inserted SM number in a phase is controlled exactly as n, then the AC side can present up to $n+1$ levels. One major challenge for the operation and control of MMC is to keep all capacitor voltages close to the rated value. Multiple modulation and control strategies are developed for the MMC, including space-vector pulse width modulation [18], phase-disposition sinusoidal pulse width modulation (PD-SPWM) [21], phase-shifted carrier pulse width modulation (PSC-PWM) [32], staircase modulation based on nearest level control (NLC) [22], etc. Due to the imperfect balance of the SM capacitor voltages among different phases, circulating current exists among different phase, which can be limited by the arm inductor L_m. Compared with other conventional converters, such as two-level converter and three-level neutral-point-clamped (3L-NPC) converters, MMC has the most complex topologies, which make it the most challenging for modeling and simulation.

1.1.3 CIGRÉ DC Grid Test System

The CIGRÉ working group has proposed a high voltage DC grid test system, which is composed of 3 DC sub-systems connecting the off-shore renewable resource power plants and the on-shore AC system as shown in Fig. 1.2 [2,33,34]. The DC grid test system contains in total 11 AC-DC converters and 2 DC-DC converters and covers three major DC transmission configurations, which are two-terminal HVDC system, non-meshed multi-terminal DC (MTDC) system, meshed multi-terminal DC system.
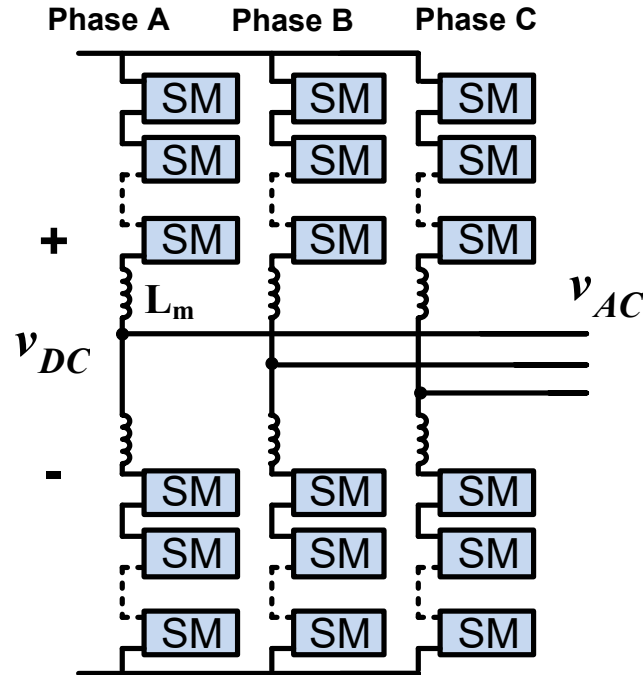
Figure 1.1: MMC topology.

The three DC systems are either connected indirectly through AC buses at the converter station or connected directly through DC/DC converters. The complex DC grid test system provides comprehensive and abundant testing scenarios, which also increases the difficulties for efficient and accurate simulation. Although the CIGRÉ DC grid test system or similar system has not been practically implemented, no insurmountable barrier exists for the future development of such system.

In [2], all the converters are MMCs using the average value model. Alternatively, the complete CIGRÉ DC test system can also contain two-level converters, three-level neutral-point-clamped converters, MMCs, and four-quadrant (4Q) DC-DC converters. The reasons for using hybrid converter topologies are the followings:

1. The establishment of a DC grid can be accomplished by connecting existing HVDC projects step-by-step. MMC provides many advantages over other converter topologies, such as extremely low harmonics, low switching frequency, high modularity, etc.; however, due to the practical constraints of cost, reliability, maturity, etc., other HVDC converter topologies would still be constructed and operated, and can be a significant portion of the DC grid.

2. The usage of hybrid converter topologies complicate the entire system to a great extent, which creates higher demand of upper-level control and protection of the system. The challenges prove to be an advantage for control and protection algorithm testing and verification purpose.
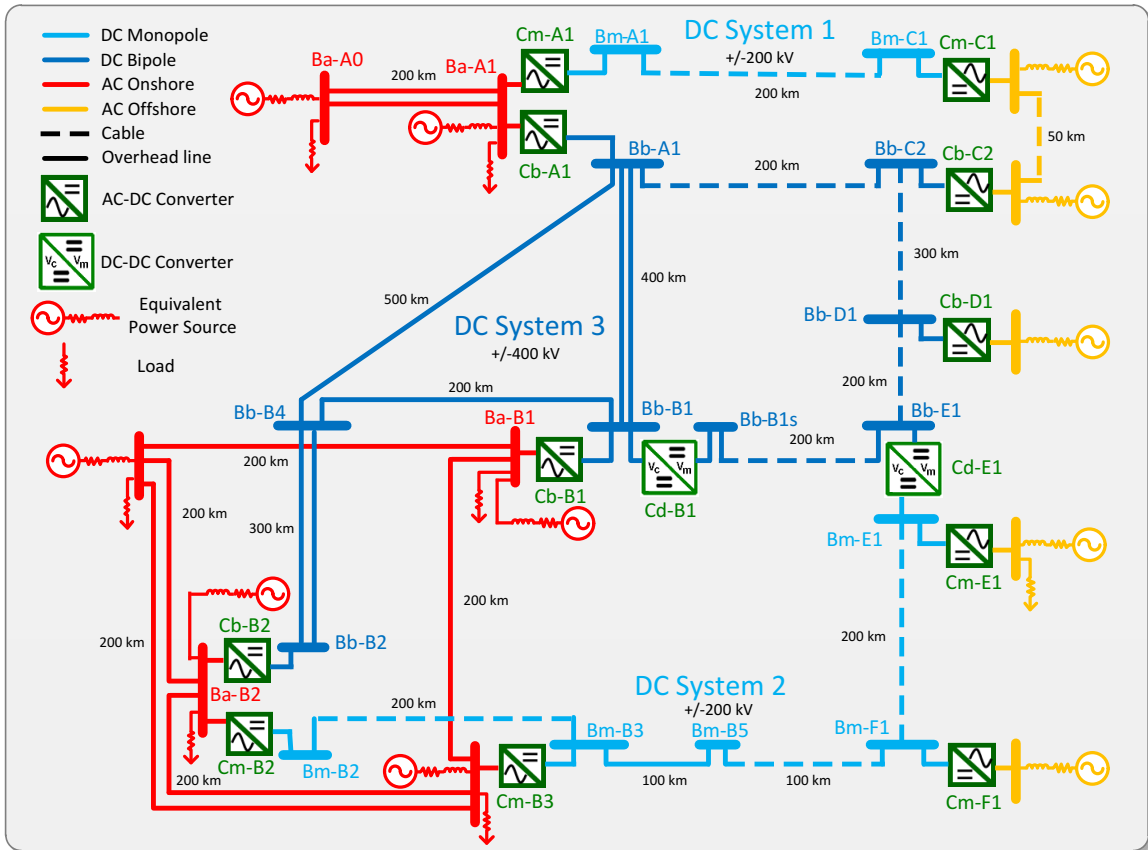
Figure 1.2: The CIGRÉ DC grid test system.

Although the DC grid has the benefits of high controllability, low power losses, and relatively low capital investment for long-distance bulk-power transmission, low impedance of DC transmission lines, which is the merit for normal operation, can cause severe short circuit currents during contingencies. It is critical to develop accurate and efficient modeling schemes and implementation platforms for off-line and the real-time EMT simulation to conduct in-depth studies of such systems, and to design and validate the solutions, control algorithms, and equipment by HIL testing.

1.2 Literature Review

This section provides the literature review of the nonlinear element solution schemes, dynamic time-stepping methods, and the conventional modeling methods of MMC for real-time simulation, which is beneficial for the understanding of the proposed variable time-stepping schemes and the device-level electrothermal model of MMC for real-time simulation.

1.2.1 Nonlinear Element Solution Schemes and Dynamic Time-Stepping Methods

In this sub-section, several widely-used nonlinear element solution methods and time-stepping schemes are introduced [11, 35–45], which are the foundation for the exploration of applying variable time-stepping to real-time simulation.

1.2.1.1 Nonlinear Element Solution Methods

1. **Newton-Raphson Method:** Applying N-R method to solve a general nonlinear circuit using nodal analysis, the matrix equation is giving by:

$$\mathbf{G}(\mathbf{v}^k)\mathbf{v}^{k+1} = \mathbf{I}_{eq}(\mathbf{v}^k), \tag{1.1}$$

where $\mathbf{v}$ is the unknown node voltage vector; $\mathbf{I}_{eq}$ is the equivalent current source vector; k is the iteration number; $\mathbf{G}$ is the Jacobian matrix for conductances, given by:

$$\mathbf{G}(\mathbf{v}^k) = \begin{pmatrix} \frac{\partial i_1}{\partial v_1}\big|_{\mathbf{v}^k} & \frac{\partial i_1}{\partial v_2}\big|_{\mathbf{v}^k} & \cdots & \frac{\partial i_1}{\partial v_n}\big|_{\mathbf{v}^k} \\ \vdots & \vdots & & \vdots \\ \frac{\partial i_n}{\partial v_1}\big|_{\mathbf{v}^k} & \frac{\partial i_n}{\partial v_2}\big|_{\mathbf{v}^k} & \cdots & \frac{\partial i_n}{\partial v_n}\big|_{\mathbf{v}^k} \end{pmatrix}. \tag{1.2}$$

   The computation effort of N-R method is relatively large, because of the iteration process, which often involves the matrix re-factorization. The complex process of N-R method, on the other hand, provides various convergence information, such as iteration counts and local truncation errors, which can be used as the criteria for time-stepping schemes.

2. **Piecewise Linearization (PL) Method:** This method, also known as pseudo-nonlinear method, uses piecewise linearized segments to fit the nonlinear curve. The segment is determined at the beginning of each time-step based on the node voltages of previous time instance, which may cause the problem of overshoot. This method is less accurate however faster compared with other iteration methods, which is often used by conventional real-time simulators.

3. **Piecewise N-R (PNR) Method:** N-R method uses continuous functions to describe the nonlinear elements, while PNR method instead uses piecewise linearized functions, which simplifies the nonlinear function resolving process and lowers the convergence criteria. PNR can also be seen as the iterative version of PL method. During fast transients, iteration is necessary to locate the correct piecewise segment without delay, which significantly increases the result accuracy.

1.2.1.2 Dynamic Time-Stepping Schemes

1. **Local Truncation Error (LTE) Method:** LTE is generated locally from the last time t_{n-1} to the current time t_n due to the approximation of discrete integration schemes

for dynamic elements, which can be estimated by Taylor series, given as:

$$LTE = C(\Delta t)^{p+1} x^{(p+1)}(t_n) + 0((\Delta t)^{p+2}), \tag{1.3}$$

where C is the coefficient determined by Taylor series; Δt is the time-step; p is the order of the integration method. In simulation software, predictor-corrector method is often used to estimate the LTE. Various predictor methods are available such as using interpolation polynomial estimate, given as:

$$x_{n+1}^0 = x_n + \sum_{k=1}^{p} (\prod_{j=0}^{k-1}(t_{n+1} - t_{n-j})) x[t_n, ... t_{n-k}], \tag{1.4}$$

where,

$$x[t_n, ..., t_{n-k}] = \frac{x[t_n, ..., t_{n-k+1}] - x[t_{n-1}, ..., t_{n-k}]}{t_n - t_{n-k}}, \tag{1.5}$$

$$x[t_n] = x_n. \tag{1.6}$$

The predictor results are good initial guesses for the N-R iteration with order p or larger integration method. The error of the predictor and the final corrector result obtained by using N-R iteration is used to estimate the LTE, which then determines the time-step of next time instance. The scheme can be applied for general m dimension nonlinear system by simply using the norm or maximum LTE of all variables.

2. **Iteration Count Method:** This method simply records the iteration count for each time instance. If many iterations are required to obtain the convergent results, the time-step will decrease for future time instances.

3. **DVDT or DIDT Method:** DVDT and DIDT are the derivatives of the node voltages and branch currents detecting the large changing rates. When a sudden large voltage or current surge appears in the circuit, small time-steps are used to capture the transients more clearly and accurately.

1.2.2   Modeling Schemes of MMC for Real-Time Simulation

Real-time performance of the MMC system simulation using FPGAs has been demonstrated well in the literature [46–48]. The computation time for MMC system in conventional circuit simulation program increases almost quadratically as a function of the sub-module number, since the size of the nodal matrix expands [23]. In the literature, the following MMC modeling methods are used in the real-time simulation for simplification:

1. Thévenin equivalence method using two-state resistor model for the IGBT module [46],

2. equivalent circuit method [47];

3. surrogate network method [48];

4. virtual phase module method [49]; and

5. digital-analog hybrid simulation method [50].

The first method uses a two-state resistor to model the IGBT module with very small resistance for turn-on state and very large resistance for turn-off state. The equivalent circuit method, the surrogate network method and virtual phase module method are similar, in that they both classify the SMs into three models based on the SM modes: on-state, off-state and blocked. In the surrogate network method, a discharge resistor is connected in parallel with the capacitor to simulate the fault condition of SM. The first three methods all use Thévenin equivalence method simplifying the SM in order to reduce the matrix nodes for the entire MMC system. In the fourth method, the converter is simulated by scaled down analog circuit components which are inflexible to reconfigure, and the simulation accuracy is highly dependent on the quality of the analog components. Even with the usage of these methods, current commercial real-time simulator can only simulate the multi-terminal DC grid with few converters.

1.3   Motivation and Objectives

The motivation of this thesis is consistent with the general development trend of real-time electromagnetic transient simulation, which is to generate more accurate and detailed results for larger power systems. The emerging technologies of power electronics devices, converter and grid topologies also require the corresponding developments of the modeling and simulation techniques. Such challenges come from the higher demand of simulation quality and the complexity of the modern AC/DC grid, which requires the solutions from both the algorithm and the hardware implementation platform.

The specific research objectives and the corresponding motivations are listed as follows:

- **Variable Time-Stepping Schemes for Real-Time EMT Simulation**
  Electromagnetic transient simulation of nonlinear elements in power systems is a particular challenge due to the requirements of accurate representation and efficient solution. Electromagnetic transients can happen in very short time-period, which requires small time-step for accurate simulation. However, it is not necessary to use such small time-step for normal steady-state operation conditions. Therefore, variable time-stepping schemes can be used to obtain accurate and efficient off-line and real-time simulation. Variable time-stepping schemes are conventionally used for device-level electronics and power electronics circuits combined with nonlinear solution methods. It has seldom been used for off-line electromagnetic transient power system simulation, and has not been used for real-time simulation. The objective

is to explore various variable time-stepping schemes which are applicable for EMT type simulation, and determine the restrictions and solutions for real-time simulation. The feasible variable time-stepping schemes and corresponding nonlinear elements methods are implemented on hardware.

- **Device-Level Datasheet-Based Electrothermal Model for MMC**
  The functionality of the EMT simulation can be extended by considering the phenomenon from other physical domains. The characteristics of power electronics devices, such as insulated gate bipolar transistor (IGBT), are highly influenced by the junction temperatures. The calculation of the power losses and the thermal network can be combined to the modeling of IGBT and diodes in MMC. The task of this work is to determine the efficient modeling schemes with easily accessible parameters from manufacturer's datasheet. Various SM topologies shall be considered and appropriate interfaces shall be developed to combine the device-level model to the system circuit ensuring real-time performance.

- **Off-Line and Real-Time AC/DC Grid Simulation**
  There is a large number of converters existed in CIGRÉ DC grid test system, which can be further expanded by connecting the renewable energy power plants and conventional AC grid. The study of the large AC/DC grid is necessary for the comprehensive and accurate analysis to minimizing the potential risks during both planning and operation stages. With limited computation capability, hybrid modeling schemes can be applied to the modeling of the converters to maintain the accuracy of the zone of interest and the size of the complete system at the same time. The criteria of partitioning the zones for different accuracies are studied in this work. The development of the converter control system, the modeling of the converters and other components are all required for the simulation of the AC/DC grid.

- **MPSoC-FPGA Platform Development and Design Methodologies**
  With more detailed converter models and more complex grid topologies, the computation requirement is substantially increased, which can be met by using the interconnected computing devices with high parallelism. The proposed algorithms and modeling schemes are either implemented and verified on FPGA or MPSoC device. The MPSoC-FPGA platform is developed for the real-time emulation of the CIGRÉ DC grid, which uses the small form-factor pluggable (SFP) for board-level communication. The complexity of the emulation system has been substantially increased, which naturally requires much higher design effort. To address this issue, high-level synthesis (HLS) is explored and applied to the design process.

1.4   Summary of Contributions

The major contributions of this work are summarized as follows:

- **Variable Time-Stepping Schemes for EMT Simulation**
  Variable time-stepping scheme for real-time EMT application has been implemented on FPGA. With the same computation resource, the transient results with higher accuracy can be obtained by using the scheme. The variable time-stepping scheme is also feasible for off-line EMT simulation with fewer restrictions.

- **Datasheet-Based Device-Level Electrothermal Model for MMC**
  Datasheet-based device-level electrothermal model for MMC has been proposed for real-time simulation. The detailed algorithm and hardware implementation has been presented. The device-level thermal data can be used to evaluate the efficiency and the security of the converter.

- **Hybrid Modeling Scheme and Grid Partition Schemes**
  The hybrid modeling scheme for converters and other elements is proposed to obtain the accurate and detailed result for the components of interest, and reduce the total computation resources for the complete system. The grid partition schemes based on the distance, the node number and the network coupling are proposed to determine the different zones, which use different modeling complexity.

- **CIGRÉ DC Grid and AC/DC Grid Modeling**
  The AC/DC grid composed of the CIGRÉ DC gird, the IEEE 39-bus AC grid, and the off-shore wind farm has been detailed modeled in PSCAD/EMTDC®. The modeling algorithm of various components in the CIGRÉ DC gird has been developed, which is applied for the design of the real-time emulator.

- **MPSoC-FPGA Platform Development**
  The MPSoC-FPGA platform has been developed to provide sufficient logic resources with high parallelism. QSFP/SPF cable and Aurora IP core are used for the communication of between the MPSoC board and the FPGA board.

- **Hardware Implementation for Real-Time Emulator**
  The design and implementation on FPGA and MPSoC devices for various proposed modeling schemes and circuit topologies have been presented in detail.

1.5   Thesis Outline

This thesis consists of eight chapters. The other chapters are outlined as follows:

- **Chapter 2**

  The background information of the FPGA and MPSoC devices used for the implementation of the real-time emulator in this work is described in this chapter. The architectures and the characteristics of the FPGA and MPSoC are introduced. The advantages and restrictions of using high-level synthesis are presented. The communication approach used in this work is introduced.

- **Chapter 3**

  This chapter proposes the detailed methodologies for applying variable time-stepping to real-time electromagnetic transient simulation to improve the simulation accuracy and efficiency. The challenges, the feasible solutions, and corresponding restrictions of applying various variable time-stepping schemes along with nonlinear element solution methods in real-time are discussed. The off-line simulation and real-time hardware emulation of two case studies, full-bridge diode circuit and power transmission system, are presented. The case studies were implemented on the FPGA device (Xilinx® Virtex-7 XC7VX485T) in real-time using high-level synthesis tool to achieve a parallelized and pipelined hardware design with minimum coding effort. The real-time emulation results captured by oscilloscope are validated against the off-line simulation on SaberRD® and PSCAD/EMTDC® software tools.

- **Chapter 4**

  A novel datasheet-based device-level electro-thermal model for MMC implemented on FPGA is presented in this chapter for real-time hardware emulation. Conduction and switching power losses, junction temperatures, temperature dependent electrical parameters, and linearized switching transient waveforms of IGBT modules are adequately captured in the proposed model. Simultaneously the system-level behavior of the MMC is accurately modeled. 5-level and 9-level MMC systems are emulated in the hardware with the time-step of $10\mu s$ and $10ns$ for system-level and device-level computations, respectively. The paralleled and pipelined hardware design using IEEE 32-bit floating point number precision runs on Xilinx® Virtex-7 XC7VX485T device with the real-time results validated by SaberRD®.

- **Chapter 5**

  This chapter applies the device-level electrothermal model to CDSM topology for the real-time EMT simulation.Among different MMC SM topologies, CDSM has the capability of DC fault current limiting and utilizes a relatively small number of switching devices. Since CDSM has a more complex circuit structure than half-bridge or full-bridge SM, it is a significant challenge for the real-time EMT simulation for MTDC system containing CDSM MMC. The electrical parameters of the IGBTs and the diodes are temperature-dependent, which increases the simulation accuracy. To ensure the real-time performance of the proposed model, the equivalent circuit model

is combined with the device-level model. The system-level and device-level waveforms during normal operation and DC fault transient for a 3-terminal DC system are both presented and compared with PSCAD/EMTDC® and SaberRD®. The emulation system was implemented on the Xilinx® Zynq UltraScale+ ZCU102 platform using CPU/FPGA multi-processor system-on-chip.

- **Chapter 6**
  This chapter focuses on the comprehensive EMT simulation of an AC/DC grid, which is composed of CIGRÉ DC grid test system, IEEE 39-bus AC system, and wind farms. The AC-DC converters are composed of different topologies of voltage source converters, including modular multi-level converters, 3-level neutral-point-clamped converters, and 2-level converters. Piecewise polynomial curve fitting is proposed for the IGBT modules in the MMC. Hybrid modeling schemes are proposed with different levels of complexity on the AC/DC grid to obtain accurate and efficient EMT simulation on PSCAD/EMTDC®. Three zone partition schemes based on distance, node number, and network coupling are also proposed and compared. The performance of the proposed schemes is presented and verified with a DC fault case study.

- **Chapter 7**
  This chapter presents the efficient solution of the DC grid real-time emulator providing accurate and detailed results. The design and implementation of the CIGRÉ DC grid is carried out on a hybrid MPSoC-FPGA platform realizing the synergy between the Xilinx® Vitrex UltraScale+ FPGA device containing a large number of logic resources and Xilinx® Zynq UltraScale+ MPSoC device containing the ARM® multi-core processing system and FPGA resources on a single chip. Hybrid modeling methodology using device-level electrothermal model, equivalent circuit model, and average value model for the converters is employed to present the detailed device-level results of local equipment and the accurate system-level results of global interactions of the DC grid. The detailed design partitioning and implementation methods are presented, and the real-time results are captured and validated with PSCAD/EMTDC® and SaberRD®.

- **Chapter 8**
  This chapter summarizes the contributions of this research and discusses the future work for the EMT simulation and DC grid study.

2

Architecture, Design Methodology and Communication of FPGA and MPSoC

Various computing devices exist for implementing certain functions or algorithms, such as the general-purpose processors, field programmable logic arrays, and application specific integrated circuits (ASICs). The processor has high clock frequency for sequential calculation and is easier for algorithm realization with high-level software programming languages and corresponding mature compiling tools. While its generality is sometimes not necessary for a specific task, which is periodically and exclusively executed. Processors cannot change its hardware architecture to optimize for the specific application. ASIC is specifically designed and manufactured for a certain application, which can be optimized to a very high level for both parallel and sequential computing. However, once designed, the ASIC system can only be used for the specific task and cannot be modified. In general, such a device is very expensive, unless massive production required. FPGA is essentially a reconfigurable digital integrated circuit, accomplished by the programmable connection and configuration of the switch matrices and the configurable logic blocks (CLBs). The hardware can be reconfigured to accommodate highly paralleled algorithms by using hardware programming language. The MPSoC device combines the FPGA and multi-core processing system on the same chip acquiring the advantages of both architectures.

For the application of the real-time simulator, ASIC is not applicable due to the relatively low quantity demand and high requirement of flexibility. Conventionally, real-time EMT simulators are implemented on the multi-core processing systems, where the simulators and the user interfaces can be designed with relatively smaller design effort using software programming languages. Although multi-core processing system can provide parallelism to some extent, the total core number is limited and the latency cannot be neglected for the inter-core communication. With the substantial increase of the computation
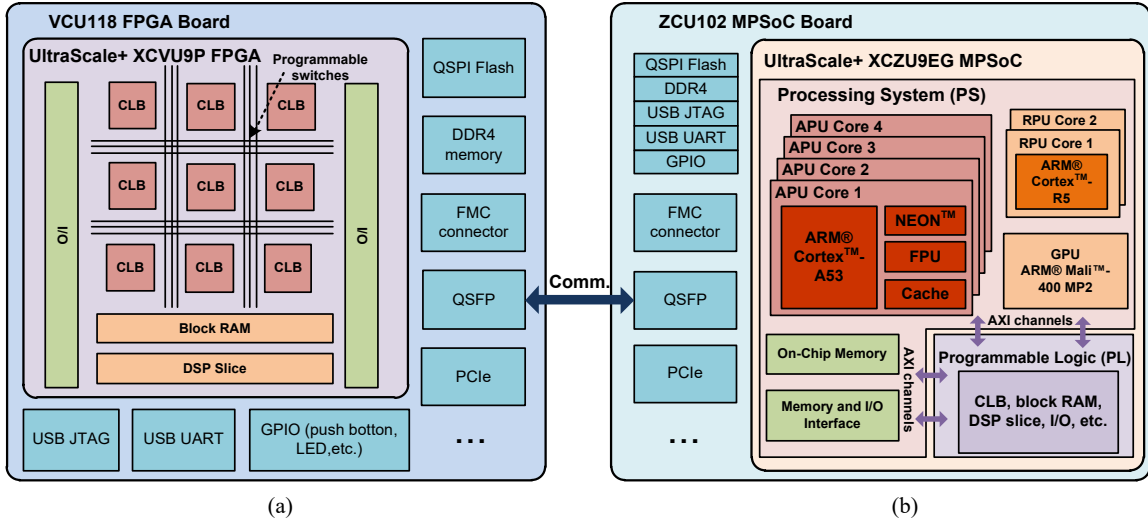
Figure 2.1: FPGA and MPSoC hybrid architecture used in this thesis: (a) Xilinx® VCU118 FPGA board and UltraScale+ XCVU9P device, (b) Xilinx® ZCU102 MPSoC board and UltraScale+ XCZU9EG device.

requirement due to the complexity of the component models and the grid topology, high parallelism is necessary for the computing device to realize the real-time performance. When power electronics devices are included, the simulator often uses smaller time-step, which again raises the requirement of computing performance. To significantly improve the parallelism, FPGA and MPSoC devices are used as the implementation platform for the real-time emulator in this research. The architecture, design methodologies, and the communication are described in the following sections with details.

2.1 FPGA Architecture

FPGA is a configurable integrated digital circuit, which contains all the basic design blocks to implement various digital circuit system. In effect, the multi-processor system can also be designed using the resources on FPGA, although it is not an efficient way to implement due to the existence of additional logic resources used to realize the reconfiguration capability. The major configuration and architecture of Xilinx® VCU118 FPGA board and the corresponding Virtex UltraScale+ XCVU9P device are shown in Fig. 2.1 (a) [29]. The other FPGA board used in this thesis is Xilinx® VC707 board containing Virtex 7 XC7VX485T device, which shares similar basic structures as Virtex UltraScale+ devices with the differences mostly on the manufacturing technologies and the quantity of the contained logic resources. FPGA contains various logic resources and structures, such as CLBs, programmable switch matrices (PSMs), block random-access memories (BRAMs), digital signal processing (DSP) slices, input/output (I/O) resource, described as follows [51–53]:

- **Configurable Logic Block**

  The basic elements of a digital system are the cascaded combinational logics and sequential logics, which are realized by the CLBs on FPGA. The combinational logics, such as inverter, NAND, NOR operators, are the major basic elements to realize certain logic functions, which can further construct the mathematical operation. The sequential logics along with the clock signals can be used to synchronize the digital system ensuring the proper function for a complex design. The sequential logics can also be used as the distributed memory. CLB is composed of the look-up-table (LUT), the FFs, and the multiplexers. LUT is the combinational logic resource to implement arbitrary logic function with a certain amount of inputs. Flip-flop (FF) is a typical sequential element which receives the data from the combinational logic and updates the values only at the clock edges. The multiplexer is used for the signal routing inside the CLB to configure the LUT and FF resources in a design. The behavior of the LUT and multiplexer can be flexibly programmed.

- **DSP Slices and Block RAMs**

  As previously explained, CLBs can provide the highest flexibility to configure arbitrary digital logic functions, which also have relatively high cost regarding the power consumption and operation speed. DSP slices and BRAMs are added to address this issue for frequently used functions or modules. DSP slice is composed of multi-bit adder, multiplier, accumulator, and multiplexer. Such optimized structure can be used to further compose complex arithmetic operations. Similarly, BRAMs provide a more efficient way for memory access. Each BRAM can be either configured to two independent 18Kb RAM or one 36Kb RAM.

- **Programmable Switch Matrices, I/Os and Other Elements**

  PSMs and the interconnected wires are the key structures to realize the configuration capability and consumes a large amount of space on FPGA. The PSM connects various elements, such as the CLBs, BRAMs, DSP slices, I/Os, etc., based on the configuration file downloaded from the host system or the storage on the board. There is a large number of I/Os which can be routed to various internal blocks and connected to the other external resources or ports on the board. FPGA also contains other necessary elements, such as buffers, mixed-mode clock manager module, etc., to fulfill the complete functions.

FPGA is currently adopted in many applications [54–62], including real-time electromagnetic transient simulation [12–14, 46, 63–77].

2.2 MPSoC Architecture and Design Process

Due to the complex routing and additional combinational and sequential logics inferred for reconfiguration on FPGA, the clock frequency of such device is lower than processing system (PS). It is critical to analyze the characteristics of the algorithm before determining the implementation platform. The EMT program contains the one-time initialization stage and periodic calculation stage for every time-step. Since the parallelism exists in both stages, FPGA may work faster with optimized design. The usage rate of FPGA resources can be low if the implemented functions are not frequently used. The resources can be a major limitation for the simulation of complex and large-scale systems on FPGA. Therefore, it is more efficient to use CPU for the infrequent tasks such as the system initialization, and complex sequential tasks, such as control algorithm. According to the above discussion, using the combination of CPU and FPGA is a more efficient and cost-effective solution for real-time transient emulation. The MPSoC architecture used in Xilinx® UltraScale+ XCZU9ZG integrates the FPGA resources and multi-processing system, including ARM® Cortex-A53 quad-core application processing units (APUs), ARM® Cortex-R5 dual-core real-time processing units (RPUs), and ARM® Mali-400 MP2 graphical processing unit (GPU) on a single chip shown in Fig. 2.1 (b) [30]. Within each APU, various components available to accelerate the computation speed, such as NEON (an advanced single instruction multiple data architecture), floating point unit (FPU), etc.

The processing system communicates with programmable logic (PL) using high bandwidth and low-latency Advanced eXtensible Interface (AXI) channels. Such architecture provides high flexibility to merge the advantages of the fast sequential calculation and the paramount parallelism to meet the requirements of high-performance computing. However, the logic resources of MPSoC are much lower than the FPGA with the same manufacture technology. A summary of the main resources of the devices used in this work are shown in Table 2.1.

Table 2.1: Programmable Logic Resource Comparison

Device	XC7VX485T FPGA	XCVU9P FPGA	XCZU9EG MPSoC
LUT	303600	1,182,240	274,080
FF	607200	2,364,480	548,160
DSP Slice	2800	6,840	2,520
Memory (Mb)	37.08	345.9	32.1
I/O	700	832	328

Xilinx® provides the Software Development Kit (SDK) tools for the software design of the MPSoC device. SDK imports the hardware design from Xilinx® Vivado tool and provide the board support package which includes various fundamental drivers for the resources of both PS and PL. Various operating systems, such as real-time operating sys-

tem, Linux, are available for a generalized system. In this work, the operating system is not utilized, therefore higher computing performance can be achieved.

2.3 High-Level Synthesis

Traditionally, FPGA programmers need to work on both designing the algorithm of specific tasks and the complex digital circuits in register-transfer level (RTL) structure using hardware description language (HDL), which is time-consuming and error-prone. High-level synthesis, provided by Xilinx®, translates C/C++ language to HDL with highly paralleled hardware structure [78]. HLS supports the arbitrary data precision, and provides abundant directives for optimization, such as loop unroll, array partition, pipelining, etc. Since C/C++ language has much higher abstraction than HDL, the coding effort is substantially reduced. A major feature of the HLS provided by Xilinx is the powerful and flexible automatic optimization.

   With a given algorithm in C/C++, HLS can automatically parallelize the algorithm to a maximum level during the synthesis process. While for the hardware design, the latency and hardware resource requirements generally cannot be met simultaneously. Appropriate directives shall be added to emphasize that which aspect is the priority of the optimization. For example, if "unroll" directive is added for a "for" loop, the calculation for all independent iterations will be unrolled to full parallelism. However, it consumes more resources, since multiplexing for hardware is unavailable for the loop. Another example is the dimension of I/O arrays and internal arrays. If the array is fully partitioned by the "array_partition" directive, the throughput capacity will be significantly increased and the latency can be reduced. "Pipeline", "loop_merge", etc, are all useful directives for optimization. It is noted that, even without adding directives, the optimization can been automatically done. However such optimization may not exactly meet the programmer's need. For small case studies, minimizing latency is the priority of the optimization, while for the DC grid emulator, the hardware resource is the major limitation. The effectiveness of the optimization for parallelism can be verified by the analysis chart and the synthesis report. A natural doubt for HLS could be that it cannot have the same optimization level of a good handwritten VHDL code. However, to write such VHDL code requires every detailed delay and resource information for all basic circuit structures based on the technology of the devices. The uncertainty and invariance of the delay also needs be considered. This professional work is indeed required for the ASIC circuit design. However, this information is generally unavailable or may be too trivial for complex FPGA application programmers, who are more focused on algorithms with high abstraction. It is very likely that the programmer may consider a design with a larger safe margin for delay, which makes the design less optimized. However, with HLS, all the delay information is considered with constant safe margin, which made the design may be even better optimized than the handwritten VHDL codes. The HLS generates the hardware, which

Figure 2.2: Communication process: (a) block diagram and (b) digital signal waveforms.

includes the operators, registers, FSM, etc. Except the I/Os defined in C functions, clock signal ("ap_clk"), reset signal ("ap_rst") and other handshake signals, such as "ap_start", "ap_done", "ap_idle", "ap_ready" will be added as the I/Os of the exported IP cores during the synthesis process. The synthesized HLS code will be packaged as the user-defined IP core, which is an RTL-level component.

However, the HLS does have limitations compared with conventional VHDL programming. The clock signal and other handshake signals cannot be precisely defined in C/C++ codes, which make it not possible to generate controllable timing for the modules. Therefore, real-time counter and the real-time I/O control module are written directly with VHDL in this work. The structure of multiplexer and FSM are also written in VHDL due to the straightforward implementation. However, the modules containing relatively complex mathematic equations can be synthesized by HLS obtaining optimized latency which is equivalent as using VHDL. Therefore, the mix usage of both VHDL and HLS is more efficient obtaining a high level of optimization with smaller coding effort.

2.4   Communication

Both Xilinx® VCU118 and ZCU102 boards have plenty of components and interfaces, such as double data rate fourth-generation (DDR4) memory, quad serial peripheral interface (QSPI) flash, general purpose IO (GPIO), FPGA mezzanine card (FMC), small form-factor pluggable. The CIGRÉ DC grid emulator described in Chapter 7 uses the SFP interface of ZCU102 and quad SFP (QSFP) interface of VCU118 combined with the Xilinx® Aurora IP cores to accomplish the communication between the two boards as shown in Fig. 2.2 (a). The Aurora 64B/66B core is a scalable, lightweight, high data rate, link-layer protocol for high-speed serial communication, supporting bi-directional transfer of data between devices using consecutive bonded gigabit transceiver Y (GTY) on VCU118 board and gigabit transceiver H (GTH) on ZCU118 board [79]. This work uses a total of four transceivers located in ZCU102 SFP and VCU118 QSFP interface to construct four lanes with 64-bit AXI-4 user data stream transmitting in each lane, which can achieve a throughput from 500 Mb/s to over 254 Gb/s. Fig. 2.2 (b) shows the waveforms of major signals during the communication process. When CHANNEL_UP signal is asserted, the Aurora cores have initialized and established 4 channel lanes for user applications to pass frames of data. User data are loaded on AXI4_TDATA[0:255] bus (64b×4 lanes) at each edge of USER_CLK when AXI_TREADY is asserted. Then user data are transferred into encoded differential serial data (RXP/N[0:3] and TXP/N[0:3]) and transmitted through the four GTH or GTY transceivers and the QSFP/SFP cable.

3

Variable Time-Stepping Schemes for Off-Line and Real-Time Simulation

3.1 Introduction

Electromagnetic transients occur frequently in power systems due to various reasons such as lightning strikes, switching surges, or power frequency overvoltages, that threaten the safety and reliability of power system equipment. The frequency range of such transients can vary from low frequency oscillations ($\sim$0.1Hz), to switching overvoltages (50Hz-20kHz), to very fast surges as in lightning and current breaker restrike transients (10kHz-50MHz) [80]. EMT simulation is essential to study the impact of their phenomena, and to design adequate insulation and protection strategies for the host power system, which often contains nonlinear elements such as surge arresters, magnetic saturation, hysteresis, switches and power electronic devices [11].

Since the transients can happen in just few tens of microseconds and the overvoltages or overcurrents can be multiple times the corresponding ratings, small time-steps are required for the EMT simulation to accurately capture the transient behavior. However, for the simulation of normal steady-state operation, a small time-step is not necessary for observation and can be a great computational burden for optimum simulation speed. Currently existing off-line EMT simulation tools such as ATP, PSCAD/EMTDC®, EMTP-RV®, etc., all employ fixed user-defined simulation time-step [35–37]. The concept of variable time-step, which is not new, has been traditionally used in many device-level power electronics circuit simulation tools such as PSpice®, HSPICE®, SaberRD® [38–40]. Such simulation tools often use iterative methods, like Newton-Raphson (N-R) combined with various dynamic time-stepping schemes to solve the nonlinear circuit system. It is noted that some EMT-type software tools have already used iterative schemes with fixed

time-step, such as EMTP-RV$^{®}$.

However, in the context of real-time simulation, which is a powerful tool for hardware-in-the-loop testing, fixed time-step is exclusively used in commercial EMT-type simulators due to the following main reasons:

1. The real-time simulators are often required to interface with external device-under-test (DUT) such as a control system or protection system. The sampling process of the interface signals, such as assigned instantaneous voltage and current values collected by control and protection system, or the gating signals of switching devices received by the simulator, is inherently required at fixed time intervals.

2. Computation efforts are large and are unable to be predicted precisely for iterative and variable time-stepping schemes. The iterative methods used in device-level circuit simulation tools often have less stability, and the solution may not converge under certain circumstances.

Nevertheless, imperfectness exists in the interface process between the real-world power system and the control and protection system, which includes communication delay, analog-to-digital conversion delay, drive circuit delay, the reaction and process time of execution devices, etc. These inherent delays are considered in the design of control systems. A small amount of delay for the real-time simulator is tolerable depending on the system type and control purpose, varying from tens of microseconds to a few milliseconds. Based on this fact, variable time-stepping schemes are implementable within a fixed longer sampling period for real-time simulation.

In many academic research projects, the real-time simulator often works in standalone mode where the control algorithm is built inside the simulator along with the host system model. In some industrial training applications, the real-time simulator is used to train and test the response of the operators under certain circumstances. For such applications, reliable and accurate results and overall real-time performance are required over the simulation duration, however it is not necessary to ensure the real-time performance for all time instances.

At this point, the concept of *hard* real-time, *firm* real-time, and *soft* real-time, which originally comes from the area of general real-time computing, is discussed within the scope of power systems real-time simulation [81]. The hard real-time applications refer to those where real-time constraint must be met in every simulation time-step, therefore fixed time-step must be used. The firm real-time applications refer to those where the interface sampling period is significantly larger than the minimum simulation time-step; however, it is still less than a certain value, such as one millisecond, where a variable simulation time-step can be used restrictedly. The soft real-time applications refer to those which do not require hardware interfacing or have a very large interface sampling period, where variable time-stepping schemes can be used fully or with minimum restriction. The usage

of firm and soft real-time does not necessarily mean the degradation of the simulation results, but the emphasis on the different functions and purposes. As later demonstrated in this chapter, with the same computation capability, fast transients can be better presented if a variable time-stepping scheme is applied.

This work proposes methodologies for using the variable time-stepping to real-time electromagnetic transient simulation. Various combinations of nonlinear solution methods and dynamic time-stepping schemes are explored in detail revealing the challenges and corresponding characteristics. This chapter discusses the restrictions applied for the appropriate time-step range, changing criteria, and the measurements to make variable time-stepping more efficient in real-time simulation. The improved accuracy and efficiency for using variable time-step are demonstrated with two case studies: a diode full-bridge circuit employing physics-based diode model showing reverse recovery phenomenon and a three-phase power transmission system with nonlinear surge arresters.

In this work, FPGA is chosen as the platform using both HDL and HLS for designing. The case studies were emulated on the Xilinx® Virtex-7 XC7VX485T FPGA device using the proposed time-stepping schemes. This chapter discusses some major nonlinear element solution methods, variable time-stepping schemes, the feasible combinations, and the restrictions and corresponding measurements for real-time simulation. The circuit structure, major element models, and off-line simulation results of two case studies are presented. This chapter introduces real-time emulation applications on FPGA and then presents the FPGA implementation and the real-time emulation results of the case studies.

3.2 Combinations and Measurements for Applying Variable Time Stepping Schemes to Real-Time Simulation

The selection of time-stepping scheme is related to the nonlinear element solution method, which provides certain variables for the time-step control algorithm. Therefore, the combinations can be various, but not arbitrary. The challenges of applying variable time-stepping for real-time simulation and the mitigation solutions are then elaborated. The three time-stepping schemes mentioned in the literature review of Chapter 1 have the major focus on the LTE induced by dynamic element modeling, the degree of convergence for nonlinear elements, and the observations needed for accurate large-amplitude high-frequency transients, respectively. The circuit type, modeling method, and the simulation purpose all affect the selection of time-stepping scheme and the corresponding threshold parameters. Another issue is the choice of the time-step changing rate, and multiple methods exist in the literature [43–45]. This work uses multiplying or dividing by 2 as the changing rate for time-step, which is straightforward and has been adopted by SaberRD® software [40, 41].

3.2.1   Combinations

Various combinations of nonlinear element solution methods and dynamic time-stepping schemes are feasible for real-time simulation. DVDT or DIDT method can be used with all three above-mentioned nonlinear solution methods with or without iterations. It is noted that the combination of PL method and DVDT/DIDT method is compatible with off-line EMT-type software engine. Therefore, this combination could be helpful for boosting the off-line simulation for some applications. Although PNR method does require iterations for some time instances, however in other circumstances the nonlinear segment does not change and the results can be solved without iteration, which is the same as PL method. Therefore, iteration count scheme is not available for PNR and PL method. LTE scheme is normally used with N-R like method, where highly nonlinear functions exist. Under such circumstances, the numerical stability is relied on the appropriate choice of time-steps. Since PNR and PL methods generally have good numerical stability, the LTE scheme is not necessary though the predictor-corrector procedures may still be applicable for some applications.

Since the computation effort for N-R method is higher, the simulated circuit scale is smaller than those using other simpler methods. The smaller circuit using N-R method can be cooperated with other larger linear circuit by using various circuit separation schemes such as introducing delays, using transmission line model for connection. The connected larger circuit can use fixed time-step with the interface similar to the one used for the external control system.

3.2.2   Restrictions and Measurements for Real-Time Simulation

The relatively large computation effort for iterative schemes and the requirement of a fixed interface sampling rate are major challenges for applying variable time-stepping schemes. Some restrictions and measurements are applied to mitigate the issues, listed as follows.

3.2.2.1   Limit the Range of Time-Steps

The smaller range, especially limiting the maximum time-step, can improve the convergence property of the iteration schemes, and reduce the chance of rejecting solutions since large LTE or iteration counts are often caused by using large time-steps. To maximize the usage of the computation capability, the variable time-steps shall be changed around the maximum fixed time-step, which ensures the real-time performance. The maximum time-step can not exceed the interface sampling period, while the minimum time-step is restricted by the computation capability.

3.2.2.2 Apply Conservative Time-Step Changing Criteria and Avoid Frequent Time-Step Changing

The time-step changing criteria is referred to the threshold values of LTE, iteration counts, or DVDT. The conservative threshold criteria chooses smaller time-steps, which may increase the total time instances. However, because of the smaller time-steps, the total iteration counts tend to be smaller, and the chance of solution rejection is smaller. Combined with the limited time-step range, the computational effort is relatively stabler and easier to predict during the simulation.

3.2.2.3 Use Smaller Maximum Iteration Count Number

The purpose of this restriction is to limit the computation burden for a time instance. It is particular useful for PNR method with numerical stable applications, where solution rejection is not necessary since limiting iterations just affects the result accuracy. For such applications, the extreme case of applying this restriction is the same as using PL method.

3.2.2.4 Calculate the Constants for Different Time-Steps in Advance

When applying smaller range of time-steps and using constant changing rate for time-step, there are only several determined time-steps during the simulation. Before the simulation begins, the constants and the conductance matrices for all these time-steps are calculated and partially-decomposed. When the time-step is changed, these pre-calculated constants are loaded to the solver directly without re-calculation. The loading process can be extremely fast for FPGA with merely one clock cycle delay.

3.2.2.5 Use the Foreknown Transient Information

Some test conditions, such as faults and surges, are often pre-set to the simulator and triggered at a determined time instance. This knowledge can let the simulator set the time-step to a minimum value just before the condition happens, since high frequency transients may occur. This measurement will not affect testing results, since the device under test, which can be a controller, is not aware of any test conditions in advance.

3.3 Off-Line Simulation of Two Case Studies

Two case studies, diode full-bridge circuit (Case 1) and power transmission system (Case 2), are presented in this section, using different time-stepping schemes. The parameters of the case studies are listed in Appendix. The off-line circuit simulation programs for the case studies are written in Matlab® script, where the restrictions and measurements for real-time simulation are considered. The result accuracy is verified by comparing with SaberRD® or PSCAD/EMTDC® software. The solution combinations with the best performance are then implemented on FPGA and run in real-time.

3.3.1 Diode Full-Bridge Circuit

3.3.1.1 Diode Model Description

The topology of diode bridge circuit is shown in Fig. 3.1, where a physics-based nonlinear p-i-n diode model including accurate reverse recovery phenomenon is used [82], given as:

$$i(t) = \frac{q_E(t) - q_M(t)}{T_M}, \tag{3.1}$$

$$0 = \frac{dq_M(t)}{dt} + \frac{q_M(t)}{\tau} - \frac{q_E(t) - q_M(t)}{T_M}, \tag{3.2}$$

$$q_E(t) = I_S\tau[e^{\frac{v(t)}{nV_T}} - 1], \tag{3.3}$$

where $q_E(t)$ is the junction charge variable; $q_M(t)$ is the charge in the middle of intrinsic region; $i(t)$ and $v(t)$ is the current and voltage across the diode; T_M is the diffusion transit time; τ is the carrier lifetime; I_S is the diode saturation current constant; V_T is the thermal voltage; n is 2 for high level injection. Fig. 3.1 presents the equivalent circuit model of p-i-n diode and the reverse recovery phenomenon from T_0 to T_2 with the peak value I_{RM} at T_1. Since the diodes are modeled by highly nonlinear and relatively complex functions, N-R method is chosen to obtain the results accurately. The Trapezoidal rule is applied to discretize and linearize the differential equation (3.2), given as:

$$q_M(t) = \frac{\Delta t}{2T_M(1 + k_1)} \cdot q_E(t) + \frac{q_{hist}(t - \Delta t)}{1 + k_1}, \tag{3.4}$$

where,

$$q_{hist}(t - \Delta t) = q_M(t - \Delta t) \cdot (1 - k_1) + \frac{\Delta t}{2T_M} \cdot q_E(t - \Delta t), \tag{3.5}$$

$$k_1 = \frac{\Delta t}{2}(\frac{1}{\tau} + \frac{1}{T_M}). \tag{3.6}$$

The time-step Δt for the calculation of $q_M(t)$ and $q_{hist}(t - \Delta t)$ can be different when applying dynamic time-stepping schemes. Using N-R method, the equivalent conductance g_R and the current source i_{Req} are given as:

$$g_R = \frac{\partial i_R}{\partial v(t)} = k_2 I_S\tau \cdot \frac{1}{nV_T} \cdot e^{\frac{v(t)}{nV_T}}, \tag{3.7}$$

$$i_{Req} = k_2 I_S\tau[e^{\frac{v(t)}{nV_T}} - 1] - k_3 q_{hist}(t - \Delta t) - g_R \cdot v(t), \tag{3.8}$$

where,

$$k_2 = \frac{1}{T_M} - \frac{\Delta t}{2T_M^2(1 + k_1)}, \tag{3.9}$$

$$k_3 = \frac{1}{T_M(1 + k_1)}. \tag{3.10}$$
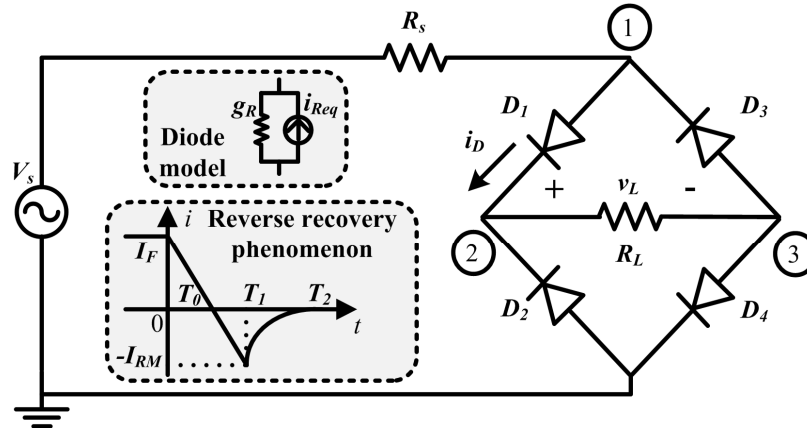
Figure 3.1: The circuit topology, diode model, and reverse recovery phenomenon for diode full-bridge circuit case study.

3.3.1.2 Off-Line Simulation Results

The off-line circuit simulation results for the diode bridge circuit using LTE and iteration count schemes based-on N-R method are shown in Fig. 3.2 (b)-(c). Since the voltage and current waveforms do not change abruptly, DVDT and DIDT methods are not effective for this application. The off-line simulation results, including the diode current i_D for D_1 and load voltage v_L, are compared with SaberRD$^®$ (Fig. 3.2 (a)), where the power diode model is employed. All the current and voltage waveforms have sufficient accuracy clearly showing the diode reverse recovery phenomenon. The time-steps for both LTE and iteration count schemes are limited within the range of 1.25μs to 5μs, while the minimum time-step is not limited for Saber$^®$ result. By limiting the range, the calculated points are reduced, while accuracy is preserved. Using a fixed small time-step to limit the LTE for all points ensuring sufficient accuracy can be computational very inefficient. Compared with the iteration count scheme, LTE scheme utilizes less total iteration counts, therefore it is chosen to be implemented on the FPGA.

3.3.2 Power Transmission System

3.3.2.1 Circuit Structure

The three-phase power transmission system shown in Fig. 3.3, is simulated to observe the transients of the lightning strike, occurring in the middle of a transmission line. On the generator side, an equivalent voltage source V_s in series with a resistor R_s is connected to a Y-Y connected transformer T. Series connected inductor L_L and resistor R_L are used to represent the load, connected through a 100km transmission line using Bergeron line model (distributed parameter traveling wave model). To determine the history current value $i(t - \tau)$ for Bergeron line model with variable time-stepping scheme, the exact time of the history current value is required to be stored. The $i(t - \tau)$ can be obtained by linear
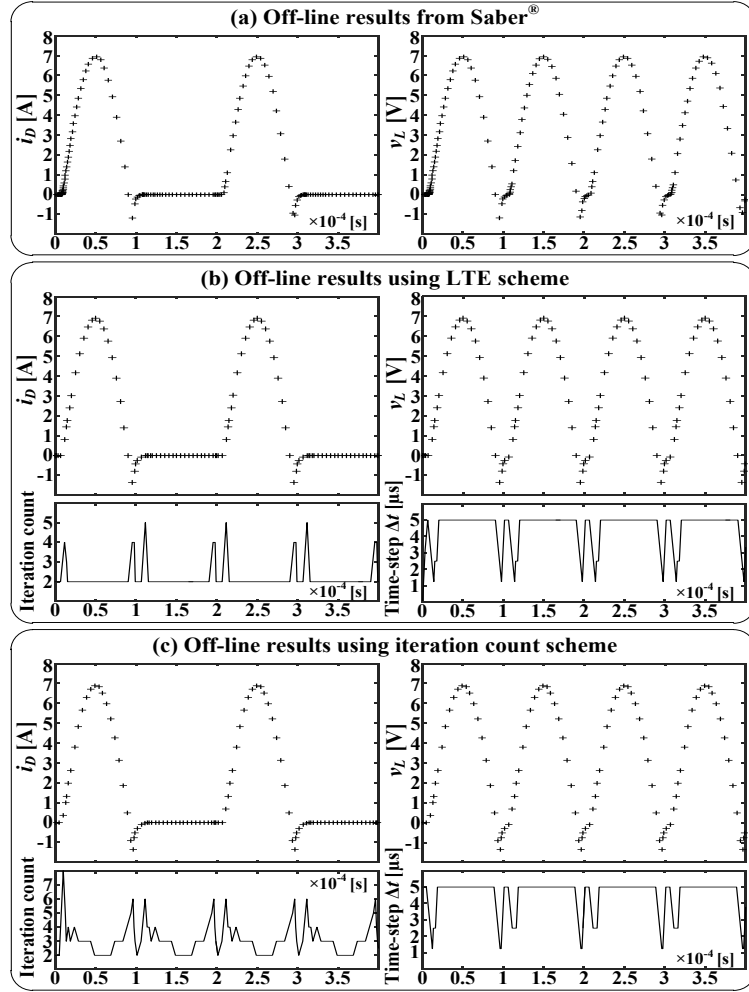
Figure 3.2: Off-line results of diode current i_D for D_1, load voltage v_L, iteration count, and time-step Δt: (a) SaberRD$^{\circledR}$, (b) LTE scheme based on N-R method, and (c) iteration count scheme based on N-R method.

interpolation of the two history current values between $t - \tau$. The six gap-less surge arresters SA_{1-6} are connected to the both sides of the transmission line, which is separated into two segments L_1 and L_2 with the lightning directly hitting phase C represented by a current source I_{LS}.

3.3.2.2   Surge Arrester Model and Lightening Surge Waveform

Metal-oxide surge arrester is commonly used to suppress the overvoltage caused by lightning, switching, faults, etc [83]. Piecewise linearization method is applied to model the surge arrester, consuming less computation effort than using a continuous nonlinear function. The segment data for surge arresters are presented in Appendix.

The standard $8/20\mu s$ current surge testing waveform is used in this work, given as [84]:

$$I_{LS}(t) = AI_p t^k exp(-t/\tau), \tag{3.11}$$
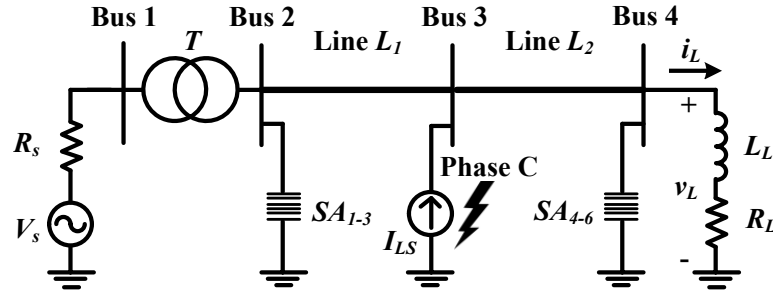
Figure 3.3: Single-line diagram for power transmission system case study.

where $A = 0.01243(\mu s)^{-3}$; $k = 3$; $\tau = 3.911\mu s$; I_p, the maximum value of the surge current, is 5000A.

3.3.2.3 Off-Line Simulation Results

PNR and PL methods combined with DVDT scheme are utilized for the off-line power transmission system. The lightning current surge starts from exactly $10ms$ of the simulation. The results are compared with PSCAD/EMTDC® using fixed time-steps, shown in Fig. 3.4. By changing the time-step value from 5μs to 10μs in PSCAD/EMTDC®, the result accuracy is significantly reduced, which can be observed by comparing the maximum values of overvoltages and overcurrents. When using PNR with various time-steps between 5μs and 20μs, the results are very close to the one from PSCAD/EMTDC® with 5μs as the time-step. If PL scheme is used, the results from variable time-stepping are no longer accurate, however, they are still better than the PSCAD/EMTDC® results with 10μs. Since the transient frequency is very high, the change of time-steps can pose great impact on the result accuracy. In this application, by using dynamic time-stepping, the computation effort is similar to the one using 10μs as fixed time-step, while results with PNR method are more accurate which are close to the PSCAD/EMTDC® results using 5μs as the fixed time-step. Admittedly, the small-amplitude high-frequency transients are somewhat diminished, which is due to the DVDT algorithm used for the application. For hardware implementation, PNR method is chosen for its better accuracy.

3.4 FPGA Implementation and the Real-Time Emulation Results

3.4.1 FPGA Implementation

The hardware implementation and data flow of the two case studies are presented in Fig. 3.5. The cells in dashed-line boxes are implemented for the diode full-bridge case study and the power transmission system case study, respectively. For other parts, the two case studies share the same hardware structure.

The finite state machine (FSM) of the real-time emulator controls the overall emula-
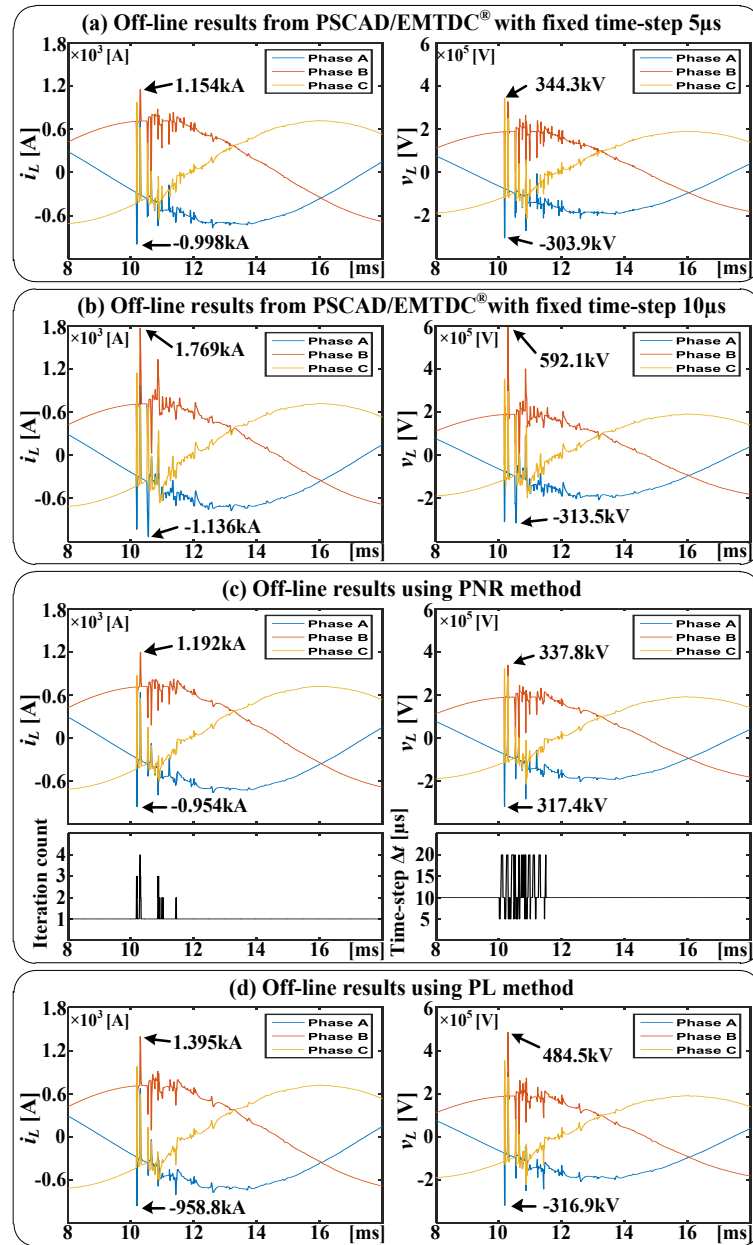
Figure 3.4: Off-line results of load current i_L, load voltage v_L, iteration count, and time-step Δt: (a) PSCAD/EMTDC® with fixed time-step 5μs, (b) PSCAD/EMTDC® with fixed time-step 10μs, (c) DVDT scheme based on PNR method, and (d) DVDT scheme based on PL method.

tion flow by interfacing with other modules through control signals, and the state chart is shown in Fig. 3.6. It receives the exact time t_{real} from real-time counter, and communicates with another internal FSM in real-time I/O control module, which manages the I/O data transfer between the emulator and the external devices. When the reset signal is detected, the state changes from S_0 to S_1, starting the initialization module, which calculates the constants for all time-steps. These constants are processed from user defined circuit
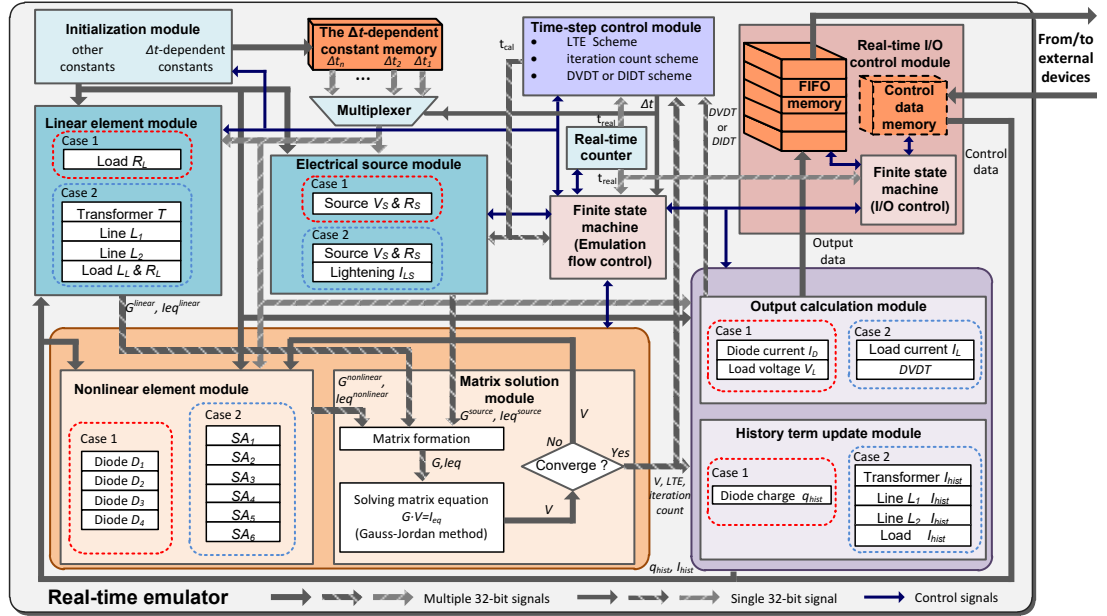
Figure 3.5: Hardware implementation and data flow of the real-time emulator for the case studies.
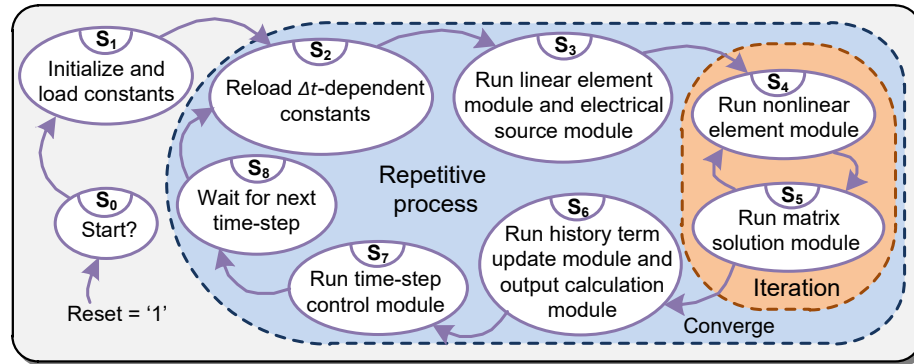
Figure 3.6: The state chart for real-time emulation flow control.

parameters to avoid unnecessary repetitive calculations, and some of them can be applied directly to the conductance matrix entries, such as the conductance of linear resistor. Taking the example of the nonlinear diode, the expression $k_2 I_s \tau$ is a typical Δt-dependent constant, while $1/nV_T$ is a pre-calculated constant without such dependence in (3.7) and (3.8). The time-step Δt dependent constants are stored in the Δt-dependent constant memory connecting to a multiplexer, while others are transferred to the corresponding modules directly.

After the initialization and loading process, the FSM then enters to the repetitive processes from S_2 to S_8, which marks the start of the real-time emulation enabling t_{real}. In S_2, the Δt-dependent constants are reloaded to the electrical source module, linear element module, and nonlinear element module through the multiplexer with Δt as the selection

signal.

Once S_2 is done, all the cells in the linear element module and the electrical source module start simultaneously in S_3, which execute only once for one time-step. These cells calculate the conductance entries and the current terms of various elements, similar to the g_R and i_{Req} in (3.7) and (3.8), but for other sources and linear elements, such as the transformer and the transmission lines, using Trapezoidal rule for discretization. Then in S_4, the equivalent conductances and current terms for nonlinear elements are calculated, which are exactly the g_R and i_{Req} of the diodes for Case 1. For nonlinear elements, iterations between S_4 and S_5 may be required, and g_R and i_{Req} need to be recalculated several times until the results converge.

The matrix solution module running in S_5, is composed of three sequential processes: matrix formation, matrix solution, and convergence judgment. Matrix formation is applied adding the conductances and current terms of multiple elements connecting to the same node, and forming the matrix $\mathbf{G}$ and vector $\mathbf{I}_{eq}$, which are then solved by Gauss-Jordan method. For the matrix solver, LU factorization, conventional Gauss elimination and Gauss-Jordan method, etc., could all be the candidates for the real-time emulator [85]. LU factorization is very useful when conductance matrix G does not change over time. However when nonlinear elements contained, the factorization may need to be re-applied if any element of G changes. In such case, LU factorization is less efficient than simply using Gauss elimination, since LU method requires two sequential substitution processes (forward and backward substitutions). Both Gauss elimination and Gauss-Jordan methods include the forward elimination and backward substitution processes. The Gauss-Jordan method can effectively parallel the two processes, which always run completely for every solution calculation, though the total sequential computation effort is slightly higher. For the purpose of achieving highest parallelism and lowest latency, Gauss-Jordan method is applied for the FPGA-based implementation. Then the matrix solution module conduct the convergence judgment by comparing the node voltages or the segments of surge arresters of the last two sets of results in Case 1 and Case 2, respectively.

Once the converged results are obtained, the history term update module and the output calculation module runs simultaneously in S_6. The history term update module calculates some variables which will be used for future calculations for dynamic elements, such as the q_{hist} in (3.5) for diode. Various outputs, such as the currents of the diodes in Case 1, require further calculation, which is accomplished by the output calculation module. In S_7, the next Δt is calculated in the time-step control module.

When the next time instance comes, the state changes from S_8 to S_2, and the computation for next time-step begins. Due to the usage of variable time-stepping, S_8 may go through without actual waiting, when the delay time t_{delay}, the difference between t_{real} and the time for the current calculated solution t_{cal}, is positive.

The algorithms of the time-step control module for the case studies are shown in Fig. 3.7

```
                if   LTE > LTE_th1
                   Δt ← Δt / 2
                   if   Δt < Δt_min
                      Δt ← Δt_min
                else
                   if   LTE < LTE_th2
                      Δt ← Δt × 2
                      if   Δt > Δt_max
                         Δt ← Δt_max
             t_cal ← t_cal + Δt
             (LTE_th1 > LTE_th2)
                                        (a) Case 1
```

```
             t_delay ← t_real - t_cal
                if   lightening surge starts
                   Δt ← Δt_1
                else
                   if   DVDT > DVDT_th
                      Δt ← Δt_1
                   else
                      if   t_delay > t_delay,th
                         Δt ← Δt_3
                      else
                         Δt ← Δt_2
             t_cal ← t_cal + Δt
             (Δt_1 < Δt_2 < Δt_3)
                                        (b) Case 2
```
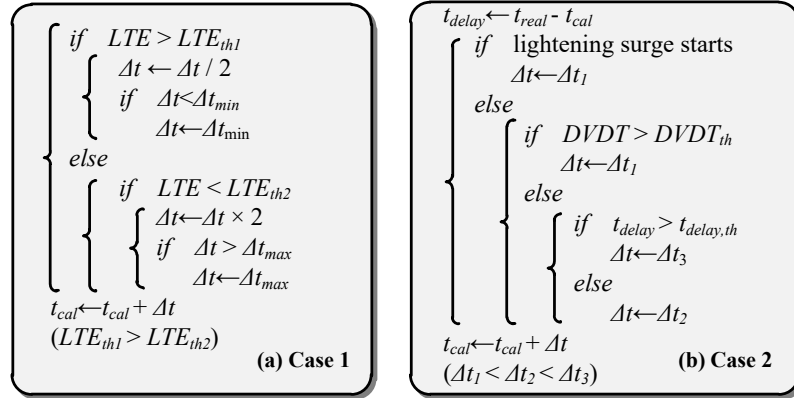
Figure 3.7: Pseudo-code for time-step control module: (a) diode full-bridge circuit and (b) power transmission system.

in the form of pseudo-code. The time-steps can be either limited to a range between the maximum value Δt_{max} and the minimum value Δt_{min} or predetermined with several choices. For diode full-bridge circuit, the LTE is compared with the threshold value LTE_{th1} and LTE_{th2} to determine the next time-step. While for power transmission system, the time-step is not only decided by $DVDT$ and the threshold value $DVDT_{th}$, but also the delay time t_{delay} and the threshold value $t_{delay,th}$. When the computation time exceeds the minimum time-step, a large time-step will be applied to balance the overall computation time ensuring real-time performance. Due to numerical stability consideration, this strategy is not applied for the diode full-bridge case study. For the diode full-bridge case study, the results can be calculated slightly ahead of real-time, when interfacing is not required (soft real-time condition). In other words, t_{delay} can be negative, while the results are sent out in exact real-time.

The Real-time I/O control module synchronizes and exchanges data between the emulation system and external devices, such as monitors, control and protection systems. For the case studies in this chapter, the external device is a 4-channel oscilloscope connected by a 16-bit digital-to-analog converter (DAC). The first-in first-out (FIFO) memory receives the results, and sends them out during the next interfacing period. The data of several time instances will be available during one interfacing period, and the external devices can receive the data of either one time instance or all time instances with the delay maximum of up to one interfacing period based on the setting in the internal FSM. A control data memory can be added to the emulator, which is not implemented for the two case studies. When the control data arrives, it will be first registered and remain the same for the interfacing period. It will then be loaded to other modules when the calculation for the next time-step starts in S_2. For the case studies, the FSM for the I/O control module only has two states: idle state and real-time output data sending state, which can be expanded for controller interface or other user defined features. Once the results of output calculation module are ready, they are sent to the FIFO memory, which is not controlled by the FSM

of real-time I/O control module.

The initialization module, the linear element module, the electrical source module, the nonlinear element module, the matrix solution module, the history term update module, and the output calculation module, shown in Fig. 3.5, are synthesized by HLS, and then packaged as user designed IP cores, respectively. These modules generally include relatively complex algorithm, and the design effort can be much lowered by C programming. The real-time counter, and the real-time I/O control module are designed by VHDL code for their strict timing requirement. The finite state machine (emulation flow control), the Δt-dependent constant memory, and the multiplexer have their own fixed or classic hardware structures, and can be designed by VHDL code very efficiently and easily. IEEE 32-bit floating-point number precision is applied for the hardware design. All these modules and structures are assembled with VHDL coding, and then implemented generating the configuration bit stream.

Table 3.1: Hardware Resource Utilization for Diode Full-Bridge Circuit and Power Transmission System Case Studies

Resource	Diode full-bridge circuit	Power transmission system
LUT	51043 (16.81%)	62495 (20.58%)
LUTRAM	903 (0.69%)	539 (0.41%)
FF	32678 (5.38%)	63804 (10.51%)
BRAM	7 (0.68 %)	102 (9.90%)
DSP	344 (12.29%)	327 (11.68%)

3.4.2 Hardware Setup, Resource Utilization, and Latency

The hardware setup for the case studies are presented in Fig. 3.8. The bit stream was downloaded to the Xilinx® VC707 board using the Virtex-7 XC7VX485T FPGA, through the JTAG adapter. The case studies were emulated on the Xilinx® Virtex-7 XC7VX485T FPGA at 100MHz clock frequency, which contains 303600 LUTs, 130800 LUTRAMs, 607200 Flip Flops, 1030 block RAMs, 2800 DSP slices, etc. The hardware resource consumption for the case studies are presented in Table 4.7. The outputs from the FPGA board were converted to analog signals by Texas Instrument® DAC34H8 DAC board [86], which requires basic configuration setting. The Tektronix® DPO 7054 oscilloscope was used to capture and present the analog signals from the DAC board.

The latencies of various states and the total latency for the two case studies are presented in Table 3.2. The latencies for adder/subtracter, multiplier and divider are 4, 4, and 9 clock cycles respectively for the case studies with 10ns as the clock period. The latencies may vary for different modules, due to the module scale, and are also influenced by the FPGA device, and the uncertainty of the clock period. Since S_1 only executes once before the repetitive process, and is therefore not taken account into the total latency. For both S_3
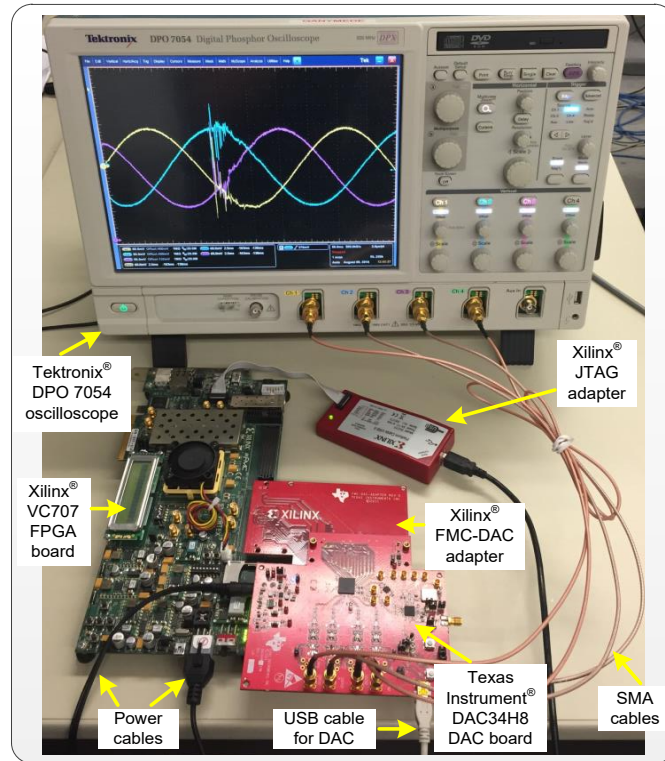
Figure 3.8: Hardware setup for the FPGA-based real-time emulation.

and S_6, two modules runs concurrently, and the maximum latency of the modules is used as the latency of the corresponding state. The latency of linear element module in Case 2 is relatively long, because it requires multiple comparisons for transmission line model to find the correct history term and then conduct the linear interpolation. The maximum iteration number is four for the both case studies, with the given parameters and test conditions. For the case studies, the average allocated computation times for one time-step are 5μs and 10μs for the two case studies. In such setting, the maximum delays due to the use of variable time-stepping and iterative method are 9.1μs and 75μs, respectively. The minimum average computation times for a time-step could be 3.9μs and 8.2μs, measured from the time scopes of 0.15-0.65 ms and 7-17 ms, for two case studies. However the maximum delay could be much larger, if using the minimum average computation time as the allocated value with no redundancy.

The CPU-based computation times for the case studies are also presented in Table 3.2 for the two case studies. The C program complied by Visual Studio 2012 was running on Intel® Xeon E5-2609 CPU at 2.40 GHZ with Windows 7 operation system. With the same computer system, SaberRD® took 0.172s computation time for the simulation of 0.4ms, which is 430 times slower than real-time for Case 1, and PSCAD/EMTDC® took 0.561s computation time for the simulation of 0.02s, which is 28 times slower than real-time for Case 2.
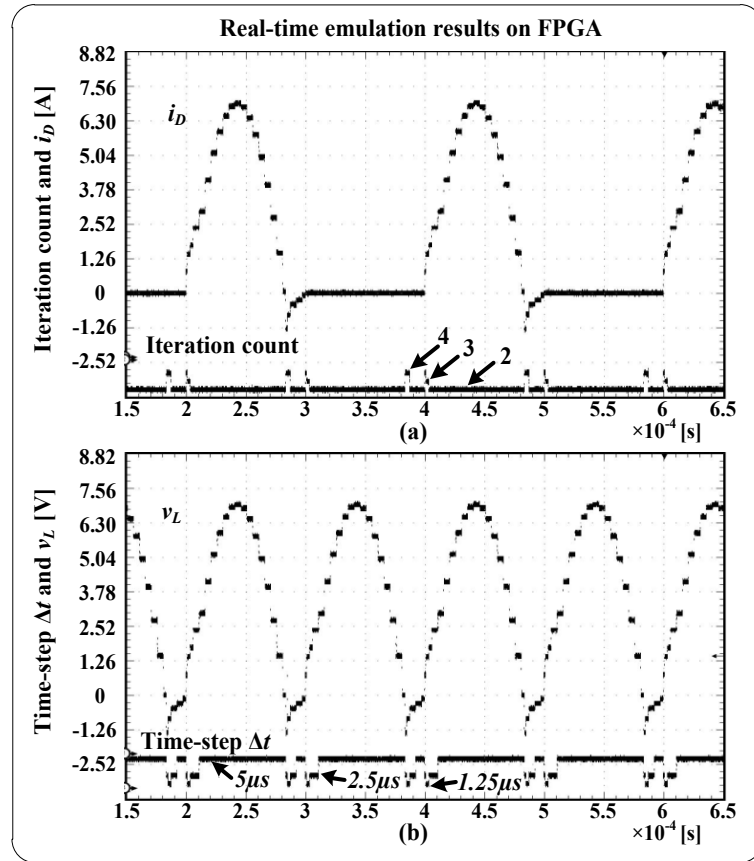
Figure 3.9: Real-time emulation results on FPGA captured by oscilloscope for diode full-bridge circuit case study: (a) diode current i_D for D_1 and iteration count and (b) load voltage v_L and time-step Δt.

3.4.3 Real-Time Emulation Results

Real-time emulation results for the case studies obtained from the oscilloscope are shown in Fig. 3.9 and Fig. 3.10, with the same parameters and test condition as the off-line simulations. All calculated data points were captured and sent to the oscilloscope. Since the matrix solver and data precision of the real-time emulator are different from the ones from Matlab®, the results are slightly different from the off-line simulation. For both case studies, the real-time emulator used the iteration counts maximum up to 4 times for any time-instances, and did not reject any solutions. The results from hardware emulation have good accuracy compared with the off-line SaberRD® and PSCAD/EMTDC®, respectively.

3.4.4 Scalability

Scalability is composed of two major parts, the increase of sequential calculation, and the parallelism capability and corresponding cost of larger system.

During periodic calculation, the two major steps are matrix element update (S_3, S_4,

Table 3.2: State Latency for Diode Full-Bridge Circuit and Power Transmission System Case Studies

State	Module	Case 1	Case 2
S_1	Initialization module	$0.36\mu s$	$1.54\mu s$
S_2	Δt-dependent constant memory and multiplexer	$0.01\mu s$	$0.01\mu s$
S_3	Linear element module	$0.01\mu s$	$2.27\mu s$
	Electrical source module	$0.16\mu s$	$0.43\mu s$
S_4	Nonlinear element module	$0.29\mu s$	$0.05\mu s$
S_5	Matrix solution module	$0.81\mu s$	$2.8\mu s$
S_6	History term update module	$0.4\mu s$	$0.86\mu s$
	Output calculation module	$0.4\mu s$	$0.19\mu s$
S_7	Time-step control module	$0.16\mu s$	$0.28\mu s$
	Total Min. latency	$2.93\mu s$	$6.27\mu s$
	(iteration number)	(two)	(one)
	Total Max. latency	$5.13\mu s$	$14.82\mu s$
	(iteration number)	(four)	(four)
	Total CPU-based Min. latency	$10.86\mu s$	$24.34\mu s$
	(iteration number)	(two)	(one)
	Total CPU-based Max. latency	$17.38\mu s$	$68.47\mu s$
	(iteration number)	(four)	(four)

and S_6) and matrix solution (S_5). The longest latency for matrix element update is only dependent on the most complex single element, not the element number. For EMT-type power system real-time simulation, the matrix is sparse and can be naturally decomposed to multiple smaller matrices through existing transmission line model by properly numbering the nodes, which is typically used in commercial real-time simulators. The latency of matrix solution is therefore decided by the size of largest sub-matrix.

The iteration number is mostly affected by the nonlinearity of the element, modeling schemes and the time-stepping schemes. The system size may also have an effect, since more nonlinear elements are involved. It can affect the stability for N-R method, while only affect the result accuracy for PNR method with a certain maximum iteration number.

FPGA provides very high parallelism capability and data transfer bandwidth. The resource can be a major limitation for hardware implementation of large circuit system using the proposed variable time-stepping schemes, however it can be resolved by using an advanced FPGA device, such as UltraSCALE+ XCVU440 containing 3,780k logic cells and 12,288 DSP slices, or by using multiple interconnected FPGA boards [87].
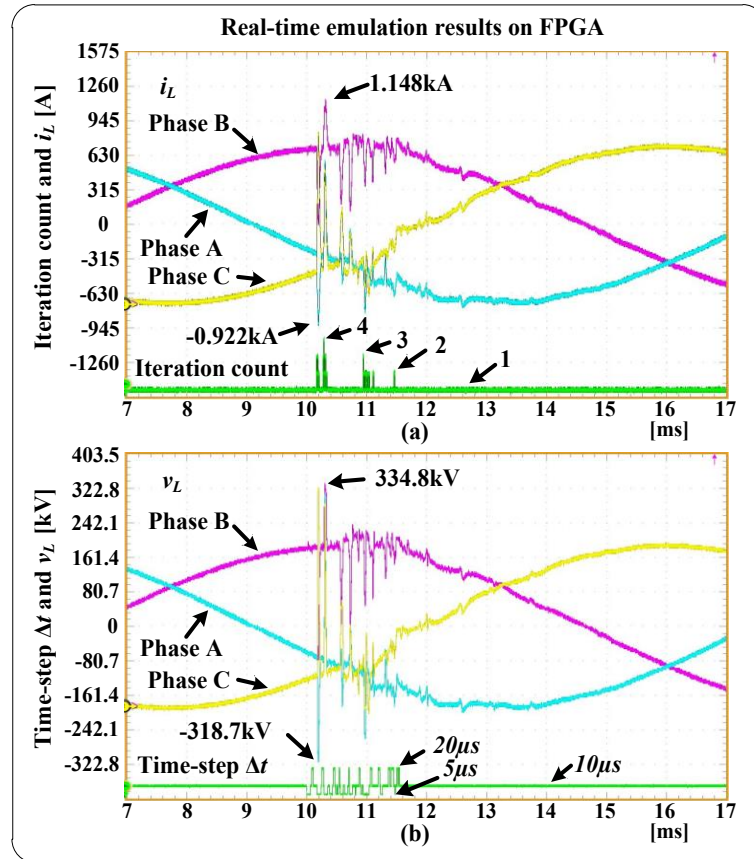
Figure 3.10: Real-time emulation results on FPGA captured by oscilloscope for power transmission system case study: (a) load current i_L and iteration count and (b) load voltage v_L and time-step Δt.

3.5 Summary

Real-time emulation of nonlinear transients in power systems can be greatly enhanced in both accuracy and efficiency by adopting variable time-steps. This chapter presented multiple dynamic variable time-stepping schemes coupled with nonlinear element solution methods, and discussed the strengths and limitations for real-time emulation in detail. Two case studies are presented to illustrate the performance of the proposed variable time-stepping schemes and their efficiency in capturing nonlinear transients in both off-line and real-time. For optimum realization of paralleled hardware implementation and smaller coding effort, the FPGA and high level synthesis are chosen to emulate the proposed schemes on hardware. As verified, using variable time-stepping in both off-line simulation and real-time emulation can have better accuracy with the same amount of computation effort especially during the transients.

4

Device-Level Electrothermal Model for Half-Bridge Sub-Module MMC

4.1 Introduction

The complicated circuit topology and control system of MMC impose a challenge for system stability and reliability, especially in abnormal operation conditions, which makes electromagnetic transient simulation of MMC system critical. Real-time digital simulators are widely used in closed-loop testing for external hardwares such as controllers and protection relays, and are powerful tools for power system simulation and industrial training. They are expected to provide accurate and abundant information, such as voltage and current waveforms in assigned branches, and transferred power.

Admittedly, by using the conventional MMC modeling methods introduced in the literature review in Chapter 1, the real-time simulators can show the system-level waveforms and the capacitor voltages with sufficient accuracy. However, the dynamic behavior of IGBT modules in SMs, such as the power losses and junction temperatures, are not available and presented. There is growing emphasis on power efficiency in modern power system, which is one of the reasons to construct HVDC systems using MMC-based power electronics converters [88, 89]. This chapter presents a real-time datasheet-driven device-level electro-thermal model for the MMC system hardware emulation on the FPGA, which contains the non-ideal IGBT module characteristics. Abundant detailed information of each SM is available in this model including conduction and switching power losses, junction temperatures, and linearized switching transient waveforms of IGBT modules. These are important indicators which can be used for among other benefits:

1. evaluating the power converter efficiency of various control methods;

2. tuning control parameters such as switching frequency based on converter efficiency and thermal requirements;

3. choosing appropriate current rating for IGBT modules and design qualified heatsink based on thermal requirements;

4. obtaining a more accurate fast Fourier transform (FFT) analysis for MMC voltage and current waveforms when considering non-ideal switching characteristics.

The proposed model utilizes readily available IGBT module parameters from the manufacturer's datasheet. This model uses junction temperature dependent series-connected voltage source and resistor representing the threshold voltage and slope resistance to piecewise linearize the output characteristic of IGBTs and diodes, which is compatible with the Thévenin equivalence method. The conduction losses and switching losses are calculated and then fed into the thermal network to compute the junction temperatures, which in turn affect the electrical parameters. The device-level transient waveform modules generate the linearized switching transient waveforms based on system-level results and temperature dependent device rise-time and fall-time from the datasheet.

The 5-level and 9-level MMC hardware emulations with paralleled and pipelined design in VHDL are targeted to a medium-size FPGA board, Xilinx® Virtex-7 XC7VX485T device [90]. This design uses IEEE 32-bit floating-point number precision, and uses a time-step of $10\mu s$ and $10ns$ for the MMC system-level computation and the device-level waveform generation, respectively, based on the clock frequency of 100MHz. All SMs of MMC system have their corresponding calculation hardware units on the FPGA, which run in parallel to ensure real-time performance.

This chapter explains the modeling method and hardware emulation of the SM and presents the model for the entire MMC system and the hardware emulation. The real-time emulation results of the case study MMC systems and the verification by off-line simulation on SaberRD® software are presented.

4.2 Datasheet-Based Device-Level Electro-Thermal Model for the Sub-Module and Hardware Emulation

Fig. 4.1 (a), shows the SM structure of a 2-level half bridge topology consisting of an upper IGBT $\mathbf{S}_1$, an upper diode $\mathbf{D}_1$, a lower IGBT $\mathbf{S}_2$, a lower diode $\mathbf{D}_2$, and an energy-storing capacitor $\mathbf{C}$. With different combinations of gate signals $g_1(t)$ and $g_2(t)$, the SM has on-state, off-state, blocking, and short circuit operation modes. In off-state, current goes through either $\mathbf{S}_2$ or $\mathbf{D}_2$ without affecting the capacitor voltage, while in on-state the capacitor is charging or discharging according to the direction of the SM current $i_{sm}(t)$. Blocking mode appears in dead-time period when the SM switches between on-state and off-state or in some special control modes. Short-circuit is not allowed in normal operation, which
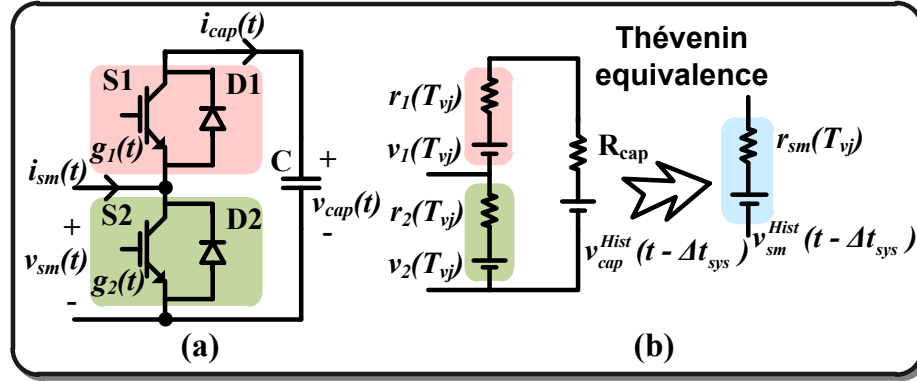
Figure 4.1: The sub-module : (a) 2-level half bridge topology, (b) temperature dependent modeling and Thévenin equivalence.

may damage the devices and even the entire MMC system. Table 4.1 lists the conduction devices and capacitor charging conditions for all operation cases classified by the combination of the gate signals and the SM current direction.

This section describes the detailed modeling method and hardware emulation for the SM. In Sub-section A, parameters from manufacturer's IGBT module datasheet are listed, part of which are employed in the modeling process. Sub-sections B to E explain the main computation procedures for the proposed model, which are electrical model calculation, power loss calculation, thermal network calculation and device-level waveform generation. In Sub-section F, all the procedures are emulated by the parallel hardware units on the FPGA.

Table 4.1: Conduction Devices and Capacitor Charging Conditions in all SM Operation Cases

Mode	(g_1, g_2, i_{sm})	Conduction device	Capacitor condition
On-State	$(1, 0, >0)$	$\mathbf{D}_1$	Charging
	$(1, 0, <0)$	$\mathbf{S}_1$	Discharging
Off-State	$(0, 1, >0)$	$\mathbf{S}_2$	No change
	$(0, 1, <0)$	$\mathbf{D}_2$	No change
Blocking	$(0, 0, >0)$	$\mathbf{D}_1$	Charging
	$(0, 0, <0)$	$\mathbf{D}_2$	Discharging
Short circuit	$(1, 1, >0)$	$\mathbf{S}_1$ and $\mathbf{S}_2$	Short circuit
	$(1, 1, <0)$	$\mathbf{S}_1$ and $\mathbf{S}_2$	Short circuit

For g_1 and g_2, 1 means turn-on, 0 means turn-off.

4.2.1 Datasheet Information Utilization for the IGBT Module

The datasheet of the IGBT module, which can be easily accessed from the device manufacturer, provides major parameters of IGBTs and diodes. This work uses the Infineon's

single IGBT module FZ400R33KL2C_B5 in construction and hardware emulation of the MMC system. Some major characteristics of the single IGBT module, which are a subset of all information in the manufacturer's datasheet, are listed as follows [91].

The IGBT module data presented in *tables* includes:

1. maximum rated values for IGBT: collector-emitter voltage V_{CES}, DC collector current I_C^{max}, peak collector current I_{CRM}, junction temperature T_{vj}^{max}, gate-emitter peak voltage V_{GES}, etc;

2. characteristic values for IGBT: collector-emitter saturation voltage V_{CEsat}, gate threshold voltage V_{GEth}, input capacitance C_{ies}, reverse transfer capacitance C_{res}, collector-emitter cut-off current I_{CES}, turn-on delay time $t_{d,on}$, rise time t_r, turn-off delay time $t_{d,off}$, fall time t_f, etc;

3. maximum rated values for diode: repetitive peak reverse voltage V_{RRM}, DC forward current I_F^{max}, peak forward current I_{FRM}, minimum turn-on time t_{on}^{min}, etc;

4. characteristic values for diode: forward voltage V_F, peak reverse recovery current I_{RM}, recovered charge Q_r, etc;

5. characteristics for module: isolation test voltage V_{ISOL}, storage temperature T_{stg}, weight G, etc.

The IGBT module data presented in *graphs* includes:

1. output characteristic of IGBT (i_C-v_{CE}) and forward characteristic of Diode (i_F-v_F);

2. turn-on loss (E_{on}^{IGBT}-i_C) and turn-off loss (E_{off}^{IGBT}-i_C) for IGBT, and reverse recovery loss for diode (E_{rr}^{Diode}-i_F);

3. transient thermal impedance from junction to case for IGBT (Z_{thjc}^{IGBT}-t) and (Z_{thjc}^{Diode}-t) diode;

4. safe operation area for IGBT (I_C^{max}-V_{CE}^{max}) and diode (I_F^{max}-V_F^{max}), etc.

Table 4.2: Utilization of Datasheet Parameters in the Modeling Procedures for the SM

Modeling procedure	Datasheet parameters
Electrical model calculation	i_C-v_{CE} and i_F-v_F plots
Power loss calculation	E_{on}^{IGBT}-i_C, E_{off}^{IGBT}-i_C, and E_{rr}^{Diode}-i_F plots; i_C-v_{CE} and i_F-v_F plots
Thermal network calculation	Z_{thjc}^{IGBT}-t and Z_{thjc}^{Diode}-t plots
Device-level waveform generation	$t_{d,on}, t_r, t_{d,off}, t_f$, and I_{RM}

Datasheets from various manufacturers may give slightly different parameters and present them in different formats; nevertheless the aforementioned data can be most commonly found. Some of the data listed above is given at two test temperatures T_1 and T_2, which are typically 25°C and 125°C. Linear interpolation can be used to estimate the parameters at other temperatures. For the purpose of SM modeling, the characteristic values of IGBT and diodes are of particular interest. Table 4.2 shows the datasheet parameters utilization in all major modeling procedures described below.

4.2.2 Electrical Model for the SM

Instead of using the simple two-state resistors, this model utilizes junction temperature dependent resistors ($r_1(T_{vj})$ and $r_2(T_{vj})$) and voltage sources ($v_1(T_{vj})$ and $v_2(T_{vj})$) to represent the IGBT modules, which are shown in Fig. 4.1 (b). Table 4.3 shows the values selected for $r_1(T_{vj})$ and $v_1(T_{vj})$ (same for $r_2(T_{vj})$ and $v_2(T_{vj})$) determined by the device conduction conditions, which are listed in Table 4.1 for all SM operation cases. The slope resistance $r_{on}(T_{vj})$ and threshold voltage $v_{on}(T_{vj})$ for the IGBT and the diode are obtained from the I_C-V_{CE} and the I_F-V_F curves by piecewise linearization. R_{off} is the off-state resistance which can be estimated by I_{CES}. Fig. 4.2 shows the output and forward characteristic curves for the IGBT and the diode at T_1=25°C and T_2=125°C from the datasheet [91]. Linear interpolation is used to estimate $r_{on}(T_{vj})$ and $v_{on}(T_{vj})$ at any junction temperatures T_{vj} for either IGBT or diode, when values in T_1 and T_2 are known, given as:

$$r_{on}(T_{vj}) = \frac{T_{vj}-T_2}{T_2-T_1}(r_{on}^{T_2} - r_{on}^{T_1}) + r_{on}^{T_2}, \tag{4.1}$$

$$v_{on}(T_{vj}) = \frac{T_{vj}-T_2}{T_2-T_1}(v_{on}^{T_2} - v_{on}^{T_1}) + v_{on}^{T_2}. \tag{4.2}$$

Table 4.3: $r_1(T_{vj})$ and $v_1(T_{vj})$ in Three IGBT Module States

IGBT module state	$r_1(T_{vj})$	$v_1(T_{vj})$
S1 conduction	$r_{on}^{S1}(T_{vj}^{S1})$	$v_{on}^{S1}(T_{vj}^{S1})$
D1 conduction	$r_{on}^{D1}(T_{vj}^{D1})$	$v_{on}^{D1}(T_{vj}^{D1})$
No conduction	R_{off}	0

The capacitor voltage $v_{cap}(t)$ of the SM is derived using Trapezoidal numerical integration with history value $v_{cap}^{Hist}(t - \Delta t_{sys})$ expressed as:

$$v_{cap}(t) = (2 - \alpha)R_{cap}i_{cap}(t) + v_{cap}^{Hist}(t - \Delta t_{sys}), \tag{4.3}$$

where

$$R_{cap} = \frac{\Delta t_{sys}}{2C}, \text{and} \tag{4.4}$$

$$v_{cap}^{Hist}(t - \Delta t_{sys}) = \alpha R_{cap}i_{cap}(t - \Delta t_{sys}) + v_{cap}(t - \Delta t_{sys}), \tag{4.5}$$
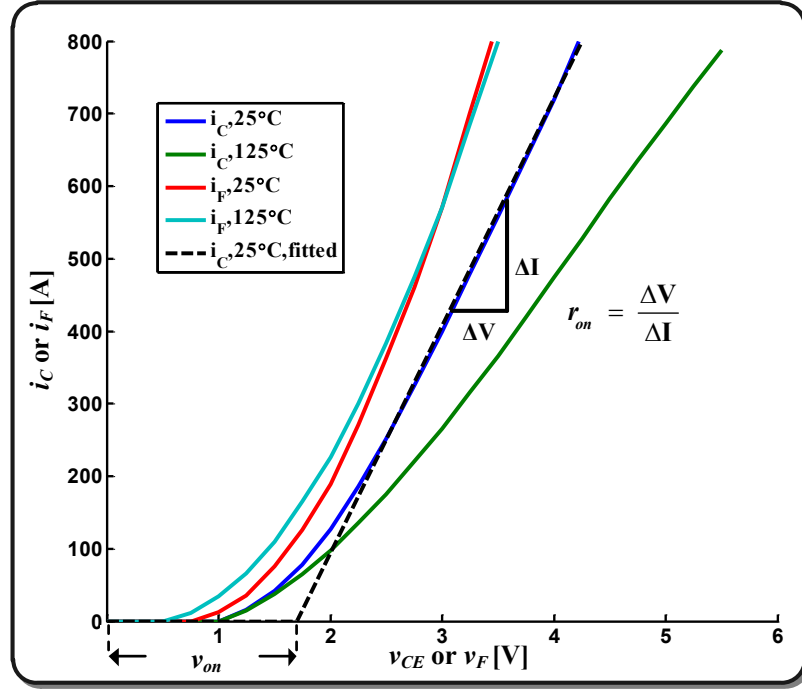
Figure 4.2: Output characteristics for IGBT and diode at T_1=25°C and T_2=125°C.

$$\alpha = 2(\frac{t_{gate} - t_{comm} - (t - \Delta t_{sys})}{\Delta t_{sys}}), (0 \leq \alpha \leq 2). \tag{4.6}$$

C is the capacitance of the SM capacitor; $i_{cap}(t)$ is the current through the capacitor; Δt_{sys} is the system-level time-step; t_{gate} is the exact time when the emulator receives the updated gate signals; t_{comm} is the communication delay of gate signals from the controller to the real-time emulator. The coefficient α is introduced for the purpose of reducing the capacitor voltage error when gate signals are changing, while, for the rest of the time, α shall be 1 for the Trapezoidal integration rule. This coefficient is only necessary when gate signal sampling time-step is significantly smaller than the system-level time-step and the communication delay cannot be neglected. In the demonstration design described in Section III, the controller and the emulator were designed on the same FPGA board, and the communication delay can be neglected since it is only one clock cycle or $10ns$. Moreover the sampling time-step of gate signals is the same as the system-level time-step, therefore α is always set as 1 in the demonstration design.

Using Thévenin equivalence, the circuit model for the SM is represented by $r_{sm}(T_{vj})$ and $v_{sm}^{Hist}(t - \Delta t_{sys})$ in series, and the SM output voltage $v_{sm}(t)$ is given as:

$$v_{sm}(t) = r_{sm}(T_{vj})i_{sm}(t) + v_{sm}^{Hist}(t - \Delta t_{sys}), \tag{4.7}$$

where

$$r_{sm}(T_{vj}) = \frac{r_2(T_{vj})(r_1(T_{vj}) + R_{cap})}{r_1(T_{vj}) + r_2(T_{vj}) + R_{cap}}, \text{and} \tag{4.8}$$

$$v_{sm}^{Hist}(t - \Delta t_{sys}) = \frac{r_1(T_{vj}) + R_{cap}}{r_1(T_{vj}) + r_2(T_{vj}) + R_{cap}} v_2(T_{vj}) +$$
$$\frac{r_2(T_{vj})}{r_1(T_{vj}) + r_2(T_{vj}) + R_{cap}} (v_{cap}^{Hist}(t - \Delta t_{sys}) - v_1(T_{vj})). \tag{4.9}$$

Similarly, Thévenin equivalence for all SMs of the MMC are processed in parallel on the FPGA. $r_{arm}(T_{vj})$ and $v_{arm}^{Hist}(t - \Delta t_{sys})$ representing all SMs in one converter arm are the interface circuit elements to the system-level calculation, which are given as:

$$r_{arm}(T_{vj}) = \sum_{k=1}^{n} r_{sm}^{k}(T_{vj}), \tag{4.10}$$

$$v_{arm}^{Hist}(t - \Delta t_{sys}) = \sum_{k=1}^{n} v_{sm}^{k,Hist}(t - \Delta t_{sys}), \tag{4.11}$$

where, n is the number of SMs in one converter arm. The dynamics of the other linear passive elements can also be discretized by Trapezoidal rule. After solving the nodal equations for the circuit of entire MMC system, $i_{sm}(t)$, which is the same as $i_{arm}(t)$, is known. $i_{cap}(t)$ for each SM capacitor is updated as follows:

$$i_{cap}(t) = \frac{r_2(T_{vj})i_{sm}(t) + v_1(T_{vj}) + v_2(T_{vj}) - v_{cap}^{Hist}(t - \Delta t_{sys})}{r_1(T_{vj}) + r_2(T_{vj}) + R_{cap}}. \tag{4.12}$$

Finally, a recursive equation is applied for the calculation of v_{cap}^{Hist}, given as:

$$v_{cap}^{Hist}(t) = 2R_{cap}i_{cap}(t) + v_{cap}^{Hist}(t - \Delta t_{sys}). \tag{4.13}$$

(4.13) is applicable when the coefficient α for capacitor voltage error correction is 1, otherwise (4.3) - (4.6) are used to update $v_{cap}^{Hist}(t)$. At this point, a set of electrical circuit solution ((4.1) - (4.13)) for the SM is established.

4.2.3 Power Loss Calculation

After the system-level calculation and the update of capacitor voltages, the power losses of the IGBTs and the diodes in the SMs can be calculated for each system-level time-step. The power losses calculation method used in this chapter is the same in [92], [93]. Power losses for IGBT $P_{loss}^{IGBT}(t)$ are mainly composed of conduction power losses $P_{cond}^{IGBT}(t)$, turn-on power losses $P_{on}^{IGBT}(t)$, and turn-off power losses $P_{off}^{IGBT}(t)$, while the power losses for diode $P_{loss}^{Diode}(t)$ are mainly from conduction power losses $P_{cond}^{Diode}(t)$ and reverse recovery power losses $P_{rr}^{Diode}(t)$.

The equations of conduction power losses for the IGBT and the diode during one system-level time-step Δt_{sys} are given as:

$$P_{cond}^{IGBT}(t) = (r_{on}^{IGBT}(T_{vj})i_C(t) + v_{on}^{IGBT}(T_{vj}))i_C(t), \tag{4.14}$$

$$P_{cond}^{Diode}(t) = (r_{on}^{Diode}(T_{vj})i_F(t) + v_{on}^{Diode}(T_{vj}))i_F(t), \tag{4.15}$$

where $i_C(t)$ is the collector current in IGBT and $i_F(t)$ is the forward current in diode, which can be determined based on $i_{sm}(t)$ and switching condition. $r_{on}^{IGBT}(T_{vj})$, $v_{on}^{IGBT}(T_{vj})$, $r_{on}^{Diode}(T_{vj})$, and $v_{on}^{Diode}(T_{vj})$ are slope resistances and threshold voltages of either upper or lower IGBT and diode pair. Reference [91] provides the IGBT switch-on energy E_{on}^{IGBT}, switch off energy E_{off}^{IGBT}, and the diode reverse recovery energy E_{rr}^{IGBT} as functions of the current $i_C(t)$ or $i_F(t)$, when junction temperature T_{vj} is 125°C and the voltage across the switch in off-state is the rated value v_{rated} (1800V). Second order polynomials are adopted here to fit these curves with the T_{vj} of 125°C (T_2), given as:

$$E_{sw}^{T_2}(i(t), v(t)) = (a \cdot i^2(t) + b \cdot i(t) + c) \cdot \frac{v(t)}{v_{rated}}, \tag{4.16}$$

where $E_{sw}^{T_2}$ represents E_{on}^{IGBT,T_2}, E_{off}^{IGBT,T_2} or E_{rr}^{Diode,T_2}, $i(t)$ represents $i_C(t)$ or $i_F(t)$, $v(t)$ represents the voltage across the switch in off-state.

Table 4.4: Extracted a, b, and c for Switching Energy Curve Fitting

$E_{sw}^{T_2}(T_2 = 125°C)$	a	b	c
E_{on}^{IGBT,T_2}	0.002575	1.478	179.7
E_{off}^{IGBT,T_2}	0.0003982	1.209	58.23
E_{rr}^{Diode,T_2}	-0.00068631	1.075	177.2

Based on the data from [91], the fitting parameters are presented in Table 4.4, and the comparison between fitting curves and original curves from datasheet is shown in Fig. 4.3. However, besides the loss curves at 125°C, [91] only provides the switching energy losses when current is at the rated value (400A) at 25°C. Based on the assumption that all points with different currents in the switching loss curves at 25°C (T_1) follow the proportional relationship of the rated current case, and the curves at other junction temperature are linearly distributed, the energy estimation equations can be derived as:

$$E_{sw}(T_{vj}, i(t), v(t)) = \frac{T_2 - T_{vj}}{T_2 - T_1}(E_{sw}^{T_1}(i(t), v(t)) - E_{sw}^{T_2}(i(t), v(t))) + E_{sw}^{T_2}(i(t), v(t)), \tag{4.17}$$

where

$$E_{sw}^{T_1}(i(t), v(t)) = \frac{E_{sw}^{T_1,rated}}{E_{sw}^{T_2,rated}}E_{sw}^{T_2}(i(t), v(t)). \tag{4.18}$$

$E_{sw}^{T_1,rated}$ and $E_{sw}^{T_2,rated}$ are the energy losses at rated test condition at T_1 and T_2. The averaged switching power loss in one system-level time-step is given as:

$$P_{sw}(T_{vj}, i(t), v(t)) = \frac{E_{sw}(T_{vj}, i(t), v(t))}{\Delta t_{sys}}. \tag{4.19}$$
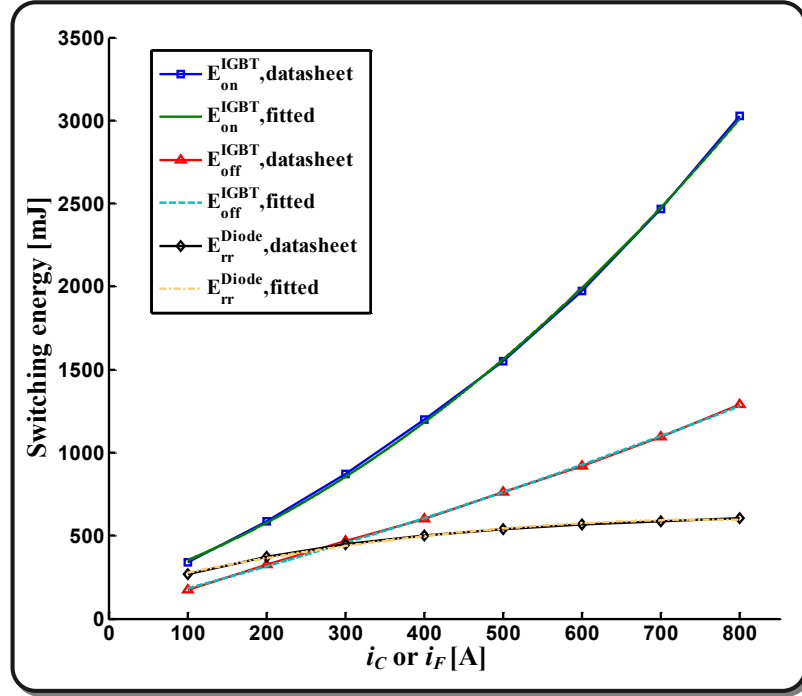
Figure 4.3: Switching energy losses at the T_{vj} of 125°C from fitted equations and datasheet.

4.2.4 Thermal Network Calculation

The calculated power losses now become the input of the thermal network to compute the junction temperatures for all IGBTs and diodes in the SM. Partial fraction thermal circuit model composed of multiple levels of thermal resistor and capacitor pairs are employed to compute the junction temperature, as shown in Fig. 5.5. The junction temperature $T_{vj}(t)$ can be calculated as:

$$T_{vj}(t) = P_{loss}(t) \cdot (Z_{thjc} + Z_{thch}) + P_{total}(t) \cdot Z_{thha}$$
$$+ T_{amb}, \tag{4.20}$$

where $P_{loss}(t)$ is the power loss for single IGBT or diode; $P_{total}(t)$ is the power loss for all devices mounted on the same heatsink; T_{amb} is the ambient temperature which is fixed in the emulation; Z_{thjc}, Z_{thch}, and Z_{thha} are the thermal impedances from junction to case, case to heatsink, and heatsink to ambient, respectively. In this work we consider that two IGBT modules are mounted on the same 10K/kW water-cooled heatsink. The thermal impedance Z_{thjc} and thermal resistor R_{thch} from case to heatsink are given by the datasheet. All the thermal impedance parameters for this work is shown in Table 5.3 in the form of thermal resistances and time constants [91].

Applying Trapezoidal rule, the numerical equation to solve for the junction tempera-
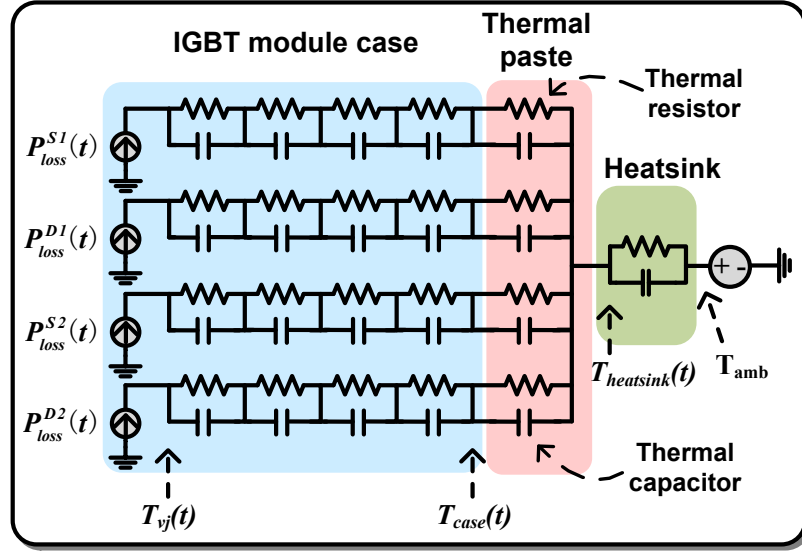
Figure 4.4: Thermal circuit structure.

Table 4.5: Thermal Impedances for Thermal Network

Thermal impedance	Z_{thjc}				Z_{thch}	Z_{thha}
	$i=1$	$i=2$	$i=3$	$i=4$	$i=5$	$i=6$
$R_{th}^{i,IGBT}[K/kw]$	11.475	6.375	1.53	6.12	24	10
$\tau_{th}^{i,IGBT}[s]$	0.03	0.1	0.3	1	3	45
$R_{th}^{i,Diode}[K/kw]$	22.95	12.75	3.06	12.24	48	10
$\tau_{th}^{i,Diode}[s]$	0.03	0.1	0.3	1	3	45

ture for either the IGBT or the diode is given as:

$$
\begin{aligned}
T_{vj}(t) &= \sum_{i=1}^{6} \Delta T_{th}^{i}(t) + T_{amb} \\
&= \sum_{i=1}^{5} (\alpha_i(P_{loss}(t) + P_{loss}(t - \Delta t_{thm})) + \\
&\quad \beta_i \Delta T_{th}^{i}(t - \Delta t_{thm})) + \alpha_6(P_{total}(t) + P_{total}(t - \Delta t_{thm})) + \\
&\quad \beta_6 \Delta T_{th}^{6}(t - \Delta t_{thm}) + T_{amb},
\end{aligned}
\tag{4.21}
$$

where

$$
\alpha_i = \frac{R_{th}^{i} \cdot \Delta t_{thm}}{2\tau_{th}^{i} + \Delta t_{thm}}, \text{ and}
\tag{4.22}
$$

$$
\beta_i = \frac{2\tau_{th}^{i} - \Delta t_{thm}}{2\tau_{th}^{i} + \Delta t_{thm}}, \ i = 1, 2, ...6.
\tag{4.23}
$$

Δt_{thm} is the thermal time-step, which has the same value as Δt_{sys} in this work. Considering the fact that thermal time constant is much longer than the time-step of MMC
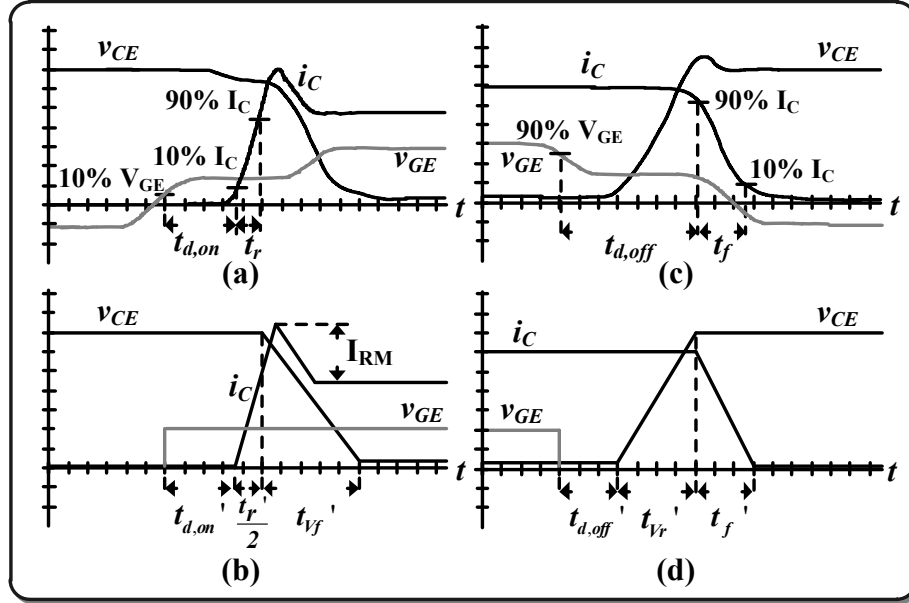
Figure 4.5: Device-level transient waveforms for IGBT module: (a) actual waveforms during turn-on transition, (b) linearized waveforms during turn-on transition, (c) actual waveforms during turn-off transition, and (d) linearized waveforms during turn-off transition.

system emulation, the time-step for thermal network can be longer without significant affect in accuracy.

4.2.5 Device-Level Transient Waveforms

The device-level waveform hardware unit generates linearized transient waveforms for IGBT modules in real-time, based on the solution from system-level emulation and the transient time information from datasheet. Rise time t_r^{rated}, fall time t_f^{rated}, turn-on delay $t_{d,on}^{rated}$, and turn-off delay $t_{d,off}^{rated}$ at T_1=25°C and T_2=125°C in standard test conditions, with rated current i_{rated} and rated voltage v_{rated} through and across IGBT module, are provided by the datasheet. The actual and linearized voltage and current waveforms in turn-on and turn-off transients are shown in Fig. 4.5. During the turn-on transition of the linearized waveform, after turn-on delay time, the IGBT collector current rises from the bottom to the steady-state conduction value; after the exact point of the current reaching the steady-state value, the voltage across the IGBT starts to drop. The turn-off transition is similar except that voltage rises first, and then the current drops.

The revised rise time $t_r'(T_{vj}, i(t))$ and fall time $t_f'(T_{vj}, i(t))$ of current waveform as a function of junction temperature T_{vj} and conduction current through IGBT module $i(t)$
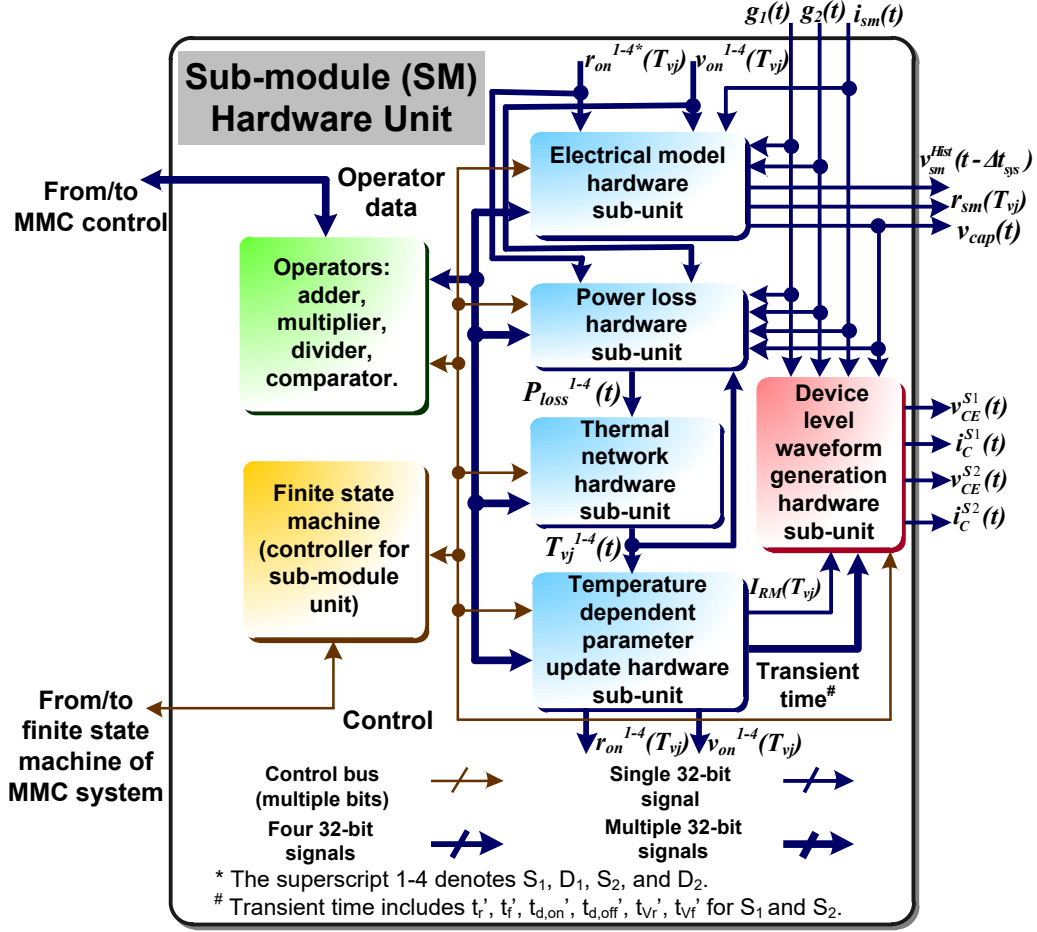
Figure 4.6: Sub-module hardware unit emulation on FPGA.

are estimated as follows:

$$t_r'(T_{vj}, i(t)) = \frac{i(t)}{i_{rated}} \cdot \frac{1}{0.8}(\frac{T_{vj} - T_2}{T_2 - T_1}(t_r^{T_2,rated} - t_r^{T_1,rated})+ \\ t_r^{T_2,rated}), \tag{4.24}$$

$$t_f'(T_{vj}, i(t)) = \frac{i(t)}{i_{rated}} \cdot \frac{1}{0.8}(\frac{T_{vj} - T_2}{T_2 - T_1}(t_f^{T_2,rated} - t_f^{T_1,rated})+ \\ t_f^{T_2,rated}). \tag{4.25}$$

In (4.24) and (4.25), the current changing rates are assumed to be constant for different conduction currents, and the coefficient 0.8 is used simply to expand the transient time range of current changing from 80% to 100%, since the provided current rise and fall time in [91] are between 10% and 90%.

The rise time $t_{Vr}'(T_{vj}, i(t), v(t))$ and fall time $t_{Vf}'(T_{vj}, i(t), v(t))$ for voltage waveforms
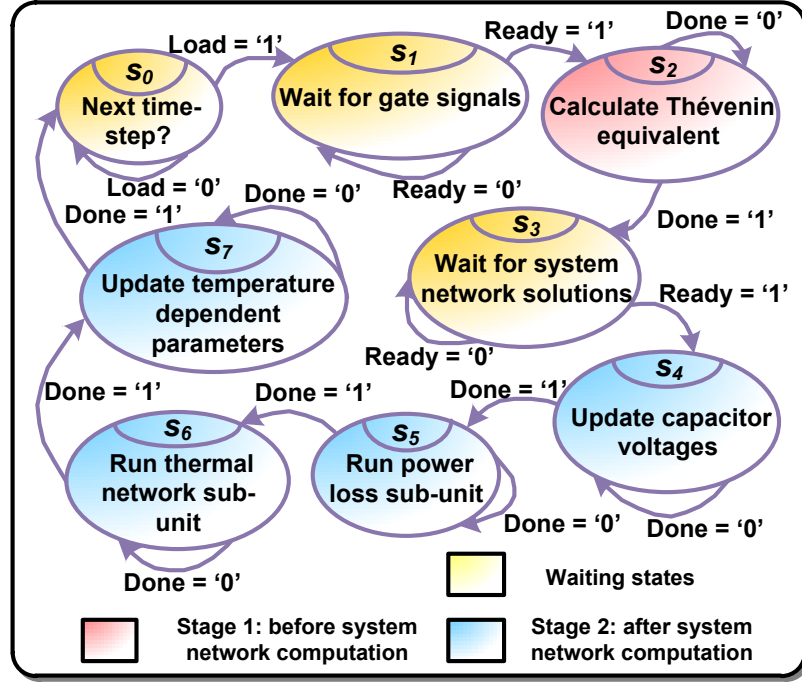
Figure 4.7: State chart for SM hardware unit.

are not provided by datasheet, which can be estimated as follows:

$$
t'_{Vr}(T_{vj}, i(t), v(t)) = \frac{2E_{off}^{IGBT}(T_{vj}, i(t), v(t))}{v(t) \cdot i(t)} - \\
t'_f(T_{vj}, i(t)),
$$
(4.26)

$$
t'_{Vf}(T_{vj}, i(t), v(t)) = \frac{2E_{on}^{IGBT}(T_{vj}, i(t), v(t))}{v(t) \cdot i(t)} - \\
t'_r(T_{vj}, i(t)).
$$
(4.27)

Finally, the revised turn-on delay $t'_{d,on}(T_{vj}, i(t))$ and turn-off delay $t'_{d,off}(T_{vj}, i(t), v(t))$ are given as:

$$
t'_{d,on}(T_{vj}, i(t)) = \frac{T_{vj} - T_2}{T_2 - T_1}(t_{d,on}^{T_2,rated} - t_{d,on}^{T_1,rated}) + t_{d,on}^{T_2,rated} \\
- \frac{1}{10}t'_r(T_{vj}, i(t)),
$$
(4.28)

$$
t'_{d,off}(T_{vj}, i(t), v(t)) = \frac{T_{vj} - T_2}{T_2 - T_1}(t_{d,off}^{T_2,rated} - t_{d,off}^{T_1,rated}) + \\
t_{d,off}^{T_2,rated} - t'_{Vr}(T_{vj}, i(t), v(t)) - \frac{1}{10}t'_f(T_{vj}, i(t), v(t)).
$$
(4.29)

When the IGBT modules are configured in half-bridge circuit topology, the diode reverse recovery current will add to the IGBT current during turn-on transient. This over current cannot be ignored, since the reverse recovery current can be even larger than the steady-state current of on-state. To present this phenomenon, the exact amount of maximum

diode reverse recovery current I_{RM}, which is temperature dependent and proportional to the steady-state current, is added to the current waveform. This addition happens when the IGBT current begins to rise as shown in Fig. 4.5 (b). By doing so the current rise slope is doubled, which means the exact rise time of the hardware emulation is only half of the result calculated in (4.24).

Admittedly, the linearized transient waveforms are not obtained from accurate differential equation solution for the IGBT module, and therefore cannot reflect the exact detailed physical phenomenon of the IGBT modules. Nevertheless, they provide a fairly accurate estimate of the switching transients in the real-time emulation for MMC system based on the limited information available from the datasheet.

4.2.6 Hardware Emulation of SM Model on FPGA

For each SM in the MMC system, a dedicated SM hardware unit (Fig. 4.6) is emulated on the FPGA, consisting of operators, finite state machine and 5 hardware sub-units: the electrical model hardware sub-unit, the power loss hardware sub-unit, the thermal network hardware sub-unit, the temperature dependent parameter update hardware sub-unit, and the device-level waveform generation hardware sub-unit. All SM hardware units run simultaneously, which means the computation time for SM hardware units of the MMC will not increase with the number of SMs.

In Fig. 4.6, the signal connections and the execution of hardware sub-units follow the algorithm described in the previous sub-sections. For instance, the power loss hardware sub-unit requires the gate signals $g_1(t)$, $g_2(t)$ and the direction of SM current $i_{sm}(t)$ from the MMC controller and the system network solution to figure out the SM operation mode, listed in Table 4.1, which determines the conditions of all switching devices (switch-on, switch-off, conduction or off). Then, $r_{on}(T_{vj})$, $v_{on}(T_{vj})$, $T_{vj}(t)$ of the corresponding devices, $v_{cap}(t)$, $i_{sm}(t)$ and other constants are substituted to (4.14)-(4.19), completing the power loss calculation.

The finite state machine controls the execution sequence for other hardware sub-units in the SM hardware unit, and receives the control signals from the finite state machine of the entire MMC emulation hardware. Fig. 4.7 shows the periodic state chart for the SM hardware unit, which begins from s_1, the start of a new emulation time-step. After the gate signals are received, the stage 1 of the SM hardware unit is activated by first calculating $v_{sm}^{Hist}(t - \Delta t_{sys})$ and $r_{sm}(T_{vj})$, which are then used for system network calculation. After $i_{sm}(t)$ is received from the system network solution, the stage 2 starts from s_4 to s_7, corresponding to the four hardware sub-units in blue shown in Fig. 4.6: electrical model, power loss, thermal network, temperature dependent parameter update hardware sub-units. When all the calculations are finished, the finite state machine goes into s_0, waiting for the next time-step.

Because of the sequential relation among the hardware sub-units except for the device-

level waveform generation hardware sub-unit, they share the same set of floating-point operators with pipelined structure and multiplexed input registers in this design, including one adder (3 clocks), one multiplier (3 clocks), one divider (9 clocks) and one comparator (2 clocks). The calculation times for the sub-units with one set of operators and the percentage of total computation time for the SM hardware unit are listed in Table 4.6. Since the FPGA runs at the clock frequency of 100MHz, and system-level time-step is $10\mu s$; thus, there are 1000 clock cycles available for a complete computation for one system-level time-step. Using more operators can decrease the delay significantly due to the parallelism existing in those hardware sub-units, which requires more FPGA resources.

The device-level waveform generation hardware sub-unit generates the voltage and current waveforms of the upper and lower IGBTs, $v_{CE}^{S1}(t)$, $i_C^{S1}(t)$, $v_{CE}^{S2}(t)$ and $i_C^{S2}(t)$, with linearized transients continuously at the time-step of $10ns$, which means the output waveforms will update at each FPGA clock cycle. The received voltage and current will be first converted into fixed-point format, since fixed-point adders are much faster than those of floating-point. The fixed-point operators will add or substrate a specific value to the voltage and current during a specific time period determined by temperature dependent transient times.

Table 4.6: Latencies of Various Sub-units in the SM Hardware Unit

Sub-unit	Total computation time with one set of operators [clock cycles]
Electrical model in stage 1	27
Electrical model in stage 2	18
Power loss	38
Thermal network	72
Temperature dependent parameter update	18
Total clock cycles used in SM hardware unit	173
Percentage in 1000 clock cycles	17.3%

4.3 MMC System Model and Hardware Emulation

4.3.1 MMC System Model and Control Scheme

Fig. 4.8 presents the three-phase MMC system circuit used as the test case in this work. The left side is connected to DC voltage source V_{DC} with a ground connection in the middle,
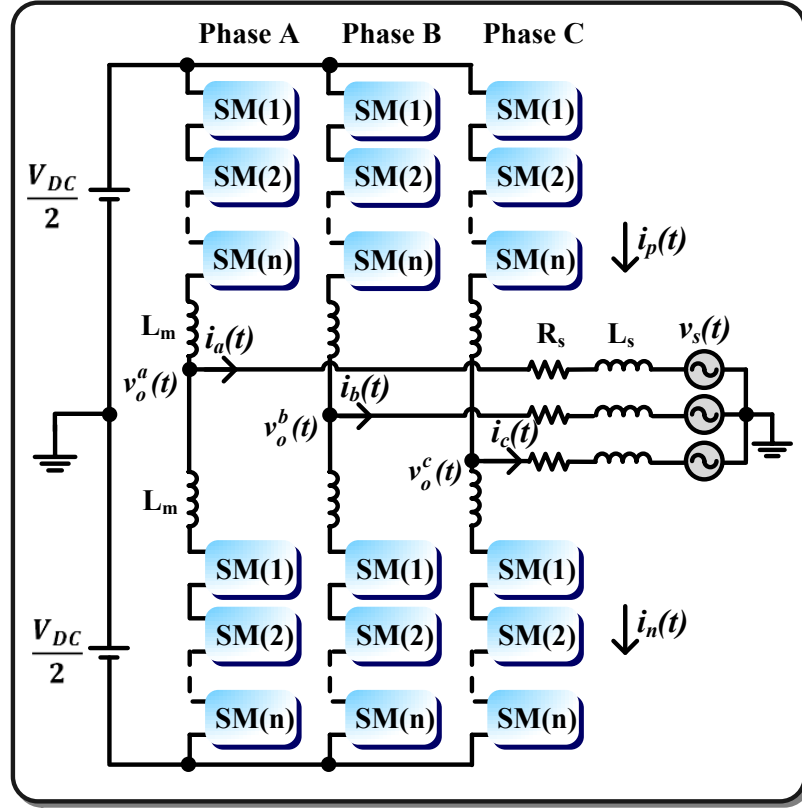
Figure 4.8: MMC system circuit.

while the right side is connected to series-connected resistors R_s, inductors L_s and three-phase AC voltage sources $v_s(t)$.

This work adopts the PSC-PWM method, which is one of the experimentally-verified modulation method. This method naturally ensures the even usage of all SMs, which is beneficial for the long-term operation of MMC. One disadvantage is the requirement of individual PI controllers for all SMs, which increases the computation effort significantly along with the growth of SM numbers. Fortunately, the control scheme for each SMs can be arranged in parallel on FPGA to minimize the time delay for the computation in controller. PSC-PWM method has the operation modes of providing $n + 1$ and $2n + 1$ voltage levels. To be consistent with other control methods and to minimize circulating current, the operation mode of providing $n + 1$ levels is chosen in this work.

Fig. 4.9 shows the entire control process of MMC used in this work. The control purpose is to track reference active power P_{ref} and reactive power Q_{ref}. The errors between reference powers and actual powers of the last time-step are fed into the proportional-integral controllers. The phase angle $\theta(t)$ is obtained from the three-phase voltage sources $v_s^{a,b,c}(t)$ through phase locked loop (PLL). In direct voltage control, the amplitude of modulation signals $M(t)$ determines the reactive power flow, and the phase shift of modulation signals $\phi(t)$ determines the real power flow, when R_s is very small. The three-phase mod-
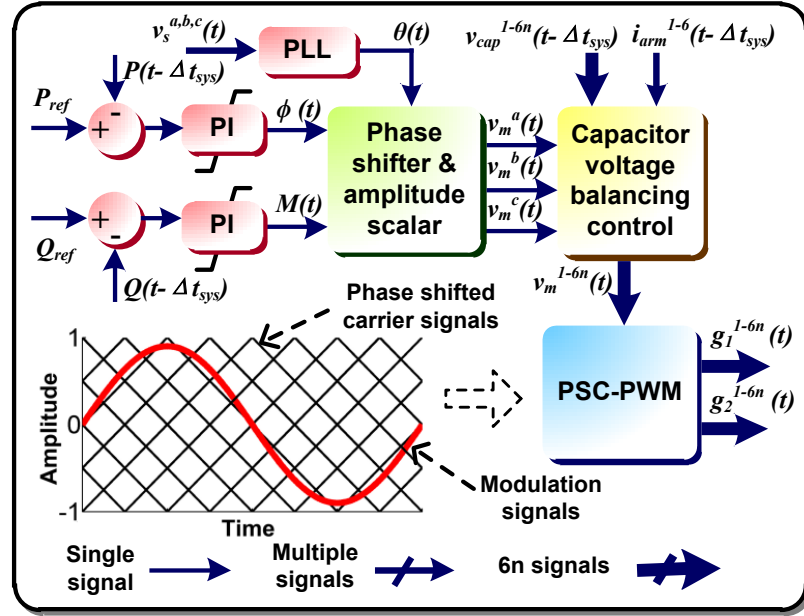
Figure 4.9: Control system for the MMC.

ulation signals $v_m^a(t)$, $v_m^b(t)$, and $v_m^c(t)$ then enter the capacitor voltage balancing control module, which is composed of averaging control and balancing control [32]. The justified modulation signals $v_m^{1-6n}(t)$ for all $6n$ SMs will compare with the corresponding phase-shifted carrier signals to generate the gate signals $g_1^{1-6n}(t)$ and $g_2^{1-6n}(t)$ in PSC-PWM module.

4.3.2 MMC System Hardware Emulation

The MMC system hardware emulation and state chart on FPGA are shown in Fig. 4.10 and Fig. 4.11, respectively. The finite state machine controls the entire emulation flow by interacting with the state machines of other hardware units through the control bus. It activates different hardware units according to the sequence shown in the state chart. After the reset button has been activated, the FPGA-based emulator goes into the initialization state s_1 through s_0. The initialization step calculates some constants which will be periodically used in later computation, such as α_i in (4.23). The matrix simplification requested by system network solution is also done in the initialization. Then the time-step counter starts to work, providing the exact time t of the real-time emulation to the finite state machine, which is used to determine the arrival moment of next time-step in s_2.

In s_3, the MMC control unit receives the active and reactive commands from the control commands unit as well as the data from the SM hardware units and the system network solution unit, and then generates the gate signals to SM hardware units. In practice, the MMC control unit and the control commands unit are the devices under test during the real-time emulation. In this work, they are integrated onto the FPGA board in the demon-
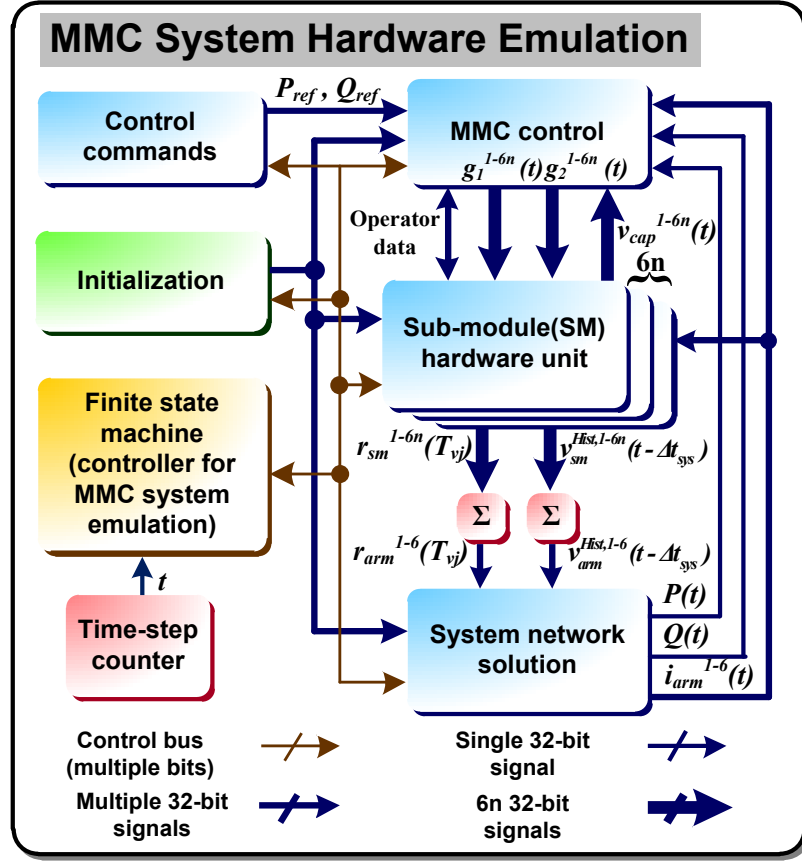
Figure 4.10: MMC system hardware emulation on FPGA.

stration design. Since the PSC-PWM control method generates control signals for each SM, therefore the process requires $6n$ sets of operators to ensure full parallelism. In this design, the MMC control unit and the SM hardware units share the same sets of operators, indicated by the bi-directional operator data bus. The detailed internal structure and algorithm of MMC control unit and SM hardware units are presented in the previous sections. State s_4 involves the stage 1 of SM hardware units and the summation for $r_{sm}^{1-6n}(T_{vj})$ and $v_{sm}^{Hist,1-6n}(t - \Delta t_{sys})$. For clarity, two summation units are drawn in Fig. 4.10. However, they are multiplexed in the actual design to save resources without affecting the speed, since the calculation of $v_{sm}^{Hist,1-6n}(t - \Delta t_{sys})$ involves more steps, and are completed later than $r_{sm}^{1-6n}(T_{vj})$. The system network solution unit receives the interface components $r_{arm}(T_{vj})$ and $v_{arm}^{Hist}(t - \Delta t_{sys})$ for the 6 arms from stage 1 of SM hardware units and then solves the nodal equations for the entire circuit topology in s_5. The outcome $i_{arm}^{1-6}(t)$ are then used to complete the stage 2 of the SM hardware units in s_6, including the power loss and thermal network calculation. When the moment of next time-step arrives, the finite state machine changes from s_7 to s_2, starting a new emulation cycle.
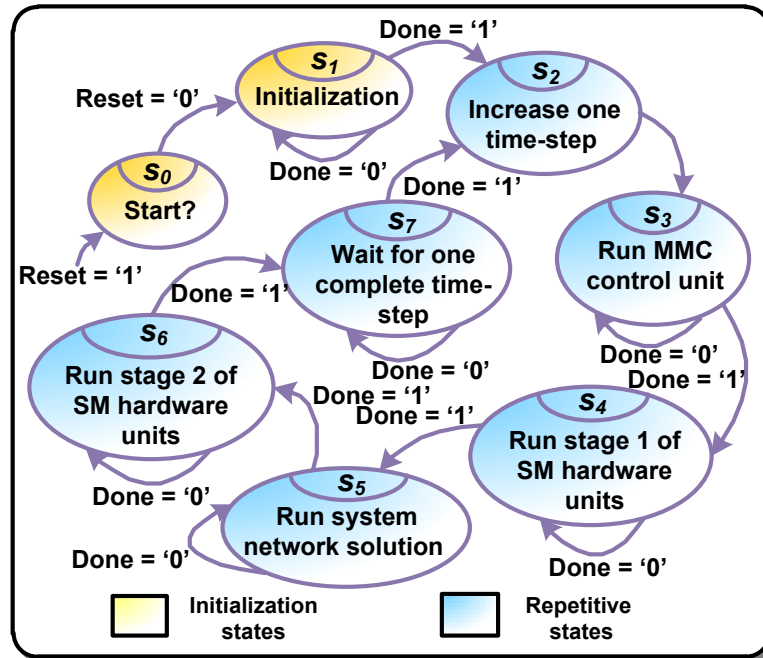
Figure 4.11: State chart for the MMC system.

4.4 Real-Time Emulation Results and Discussion

4.4.1 Test Circuit and Hardware Resource Utilization

Two case studies for MMC systems: a single-phase 5-level MMC and a three-phase 9-level MMC, were emulated on the Xilinx® Virtex-7 XC7VX485T FPGA at the clock frequency of 100MHz to validate both system-level and device-level results. The three-phase test case has the same topology of Fig. 4.8, while the single-phase test case is connected to a passive load instead of the grid. Table A.3 in the Appendix shows the circuit parameters for the two cases. The emulation results were captured by a 4-channel oscilloscope connected to the 16-bit 4-channel digital-to-analog converter, which received the data from the FPGA. The major resource utilization summary is presented in Table 4.7, and the percentage data are indicated for Virtex-7 XC7VX485T and XC7V2000T boards respectively. Since the designs only use distributed registers as memory units, the BRAM utilization is 0. The 17-level and 25-level MMCs were synthesized on the Xilinx® Virtex-7 XC7V2000T FPGA, which has more logic resources than the FPGA board used for demonstration. Fig. 4.12 shows the exact number of operators, including adders, multipliers, and dividers, utilized for MMC emulation hardware with different levels. The FPGA designs which only contain SM hardware units and summation units by the proposed electro-thermal model and the Thévenin equivalence method with two-state resistor model for IGBT modules were synthesized on XC7V2000T for resource comparison purpose. The same FPGA design methodology was applied for both cases, which is using one set of operators for each SM.

When using two-state resistor model for IGBT modules, only one adder and one multiplier are required for each SM. Sharing the same set of operators among multiple SM hardware units reduces the resource consumption, however can increase the time delay, which is not adopted in this work. The maximum SM number accommodated on XC7V2000T device for the electro-thermal model and two-state resistor model are 276 and 1104, respectively. Under normal operation, the power losses and junction temperatures are in the same level for different SMs, verified by Table 4.9, therefore emulating all SMs by the electro-thermal model is not necessary with limited FPGA resources. A combination of using the above two methods can greatly reduce the resource consumption. With these optimization and simplification schemes, the FPGA design can be very flexible to meet the resource usage and time delay requirements.

Moreover, according to Table 4.7 and Fig. 4.12, the resource usage and the operator numbers for the proposed electro-thermal model increase almost linearly with the number of MMC levels, which indicates that with more advanced FPGA devices, such as the Xilinx® UltraScale series, or using multiple FPGA boards, MMCs with larger number of levels can be configured and emulated quite efficiently.

The off-line simulation tool SaberRD® was used to validate the real-time emulated results for the single-phase 5-level MMC test case. Electro-thermal behavioral IGBT and power diode model with parameters extracted from the datasheet were employed in the SaberRD® model with a variable time-step strategy.
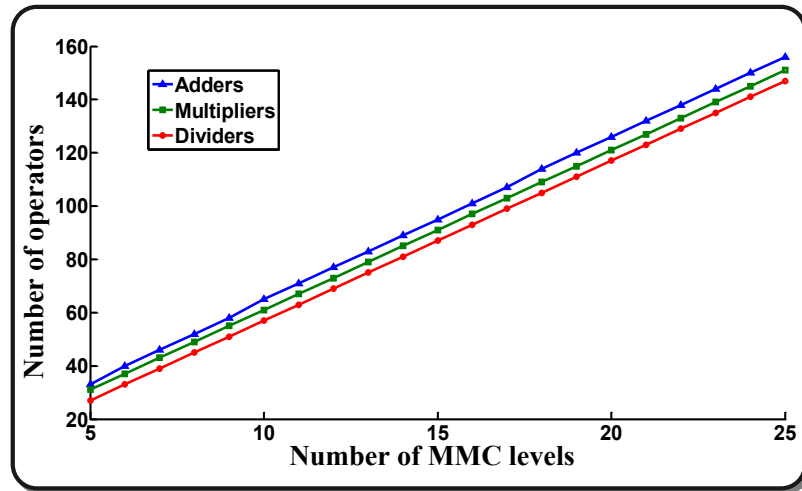
Figure 4.12: The operator count for the MMC system with increasing number of levels.
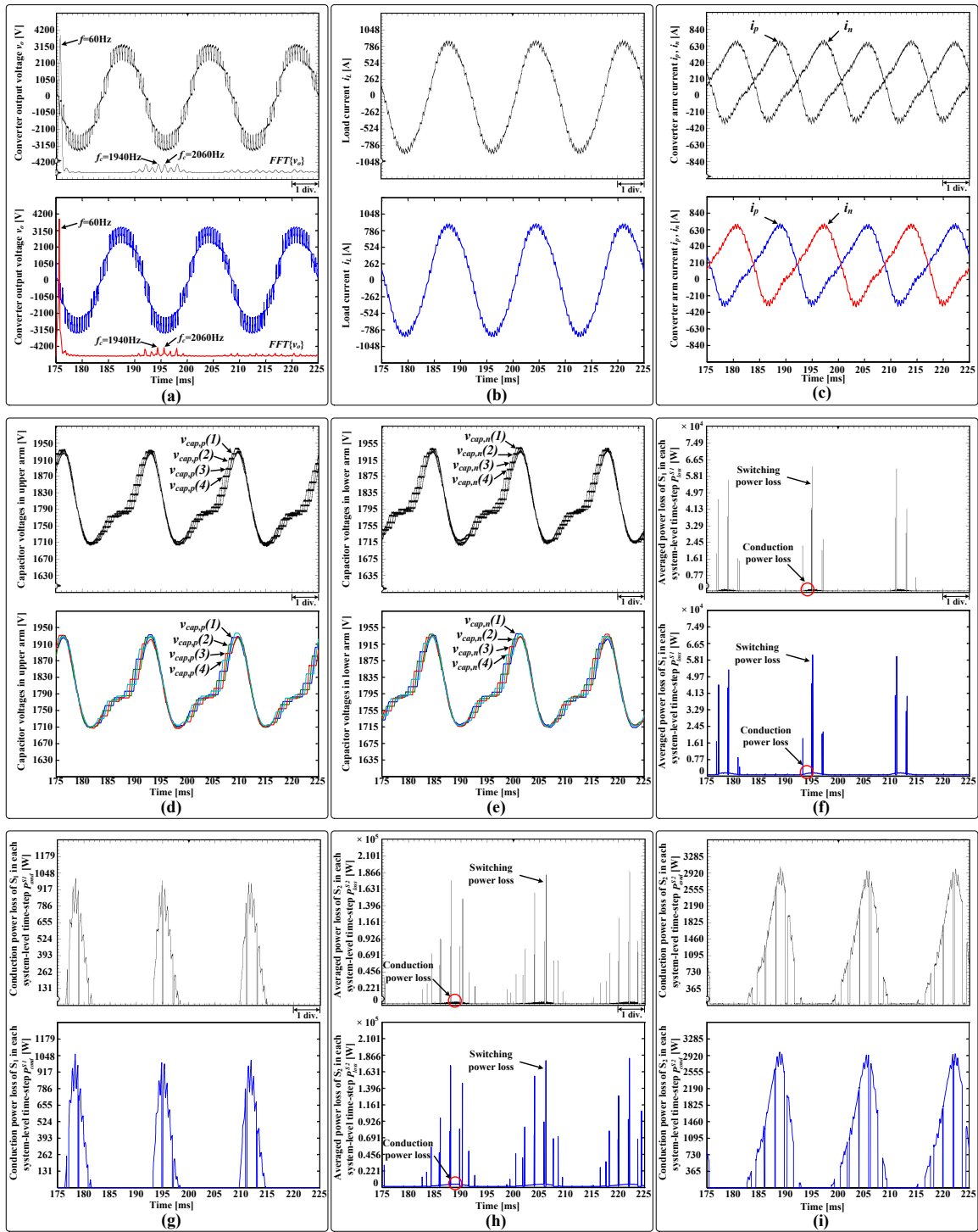
Figure 4.13: System-level and device-level power loss results for single-phase 5-level MMC system from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure) at 500Hz switching frequency. Scale: (a)-(i) x-axis: $5.0ms/$div.

Table 4.7: Hardware Resource Utilization for Three Phase MMC

Device	Levels	SM numbers	Registers	LUTs	DSP slices
XC7VX485T	5	24	180447(28%)	157735(51%)	130(4%)
	9	48	315931(52%)	294554(97%)	236(8%)
XC7V2000T	17	96	686767(28%)	639887(52%)	420(19%)
	25	144	1020845(41%)	991004(81%)	612(28%)
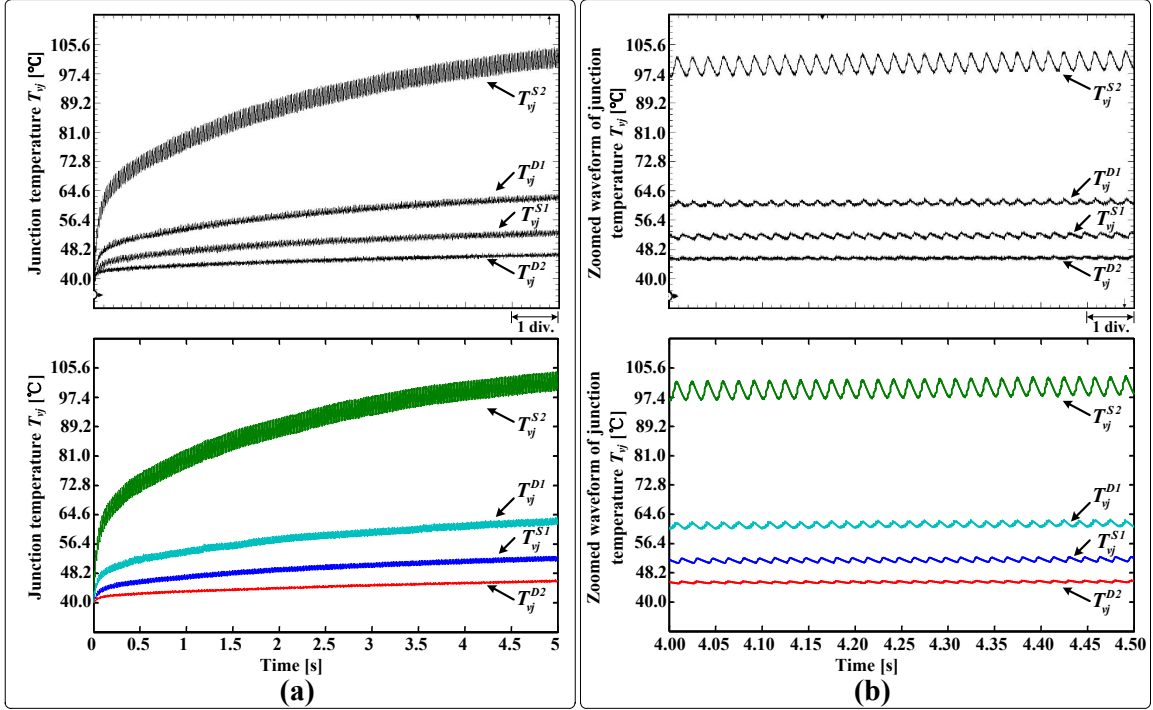
Figure 4.14: Junction temperature for single-phase 5-level MMC system from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure). Scale: (a) x-axis: $0.5s$/div, (b) x-axis: $0.05s$/div.

4.4.2 Results and Comparison for Single-Phase 5-Level MMC

Fig. 4.13 (a)-(e) present the system-level results including the converter output voltage v_o, the load current i_L, the converter arm current i_p and i_n, and the capacitor voltage of all SMs in positive and negative converter arm $v_{cap,p}$ and $v_{cap,n}$. The FFT analysis was applied to v_o. Despite the line frequency, harmonics around 2kHz are notable in both hardware emulation and SaberRD® results. It is expected, since the switching frequency is 500Hz and each converter arm has 4 SMs. Fig. 4.13 (f)-(i), Fig. 4.14, and Fig. 4.15 present the device-level results for the IGBTs and diodes in the first SM of the positive converter arm. Fig. 4.13 (f) and (h) show the averaged power losses of $\mathbf{S}_1$ and $\mathbf{S}_2$ in each system-level time-step (P_{loss}^{S1} and P_{loss}^{S2}). The conduction power losses P_{cond}^{S1} and P_{cond}^{S2} are particular shown in Fig. 4.13 (g) and (i), where switching power losses are removed for clarity. The junction
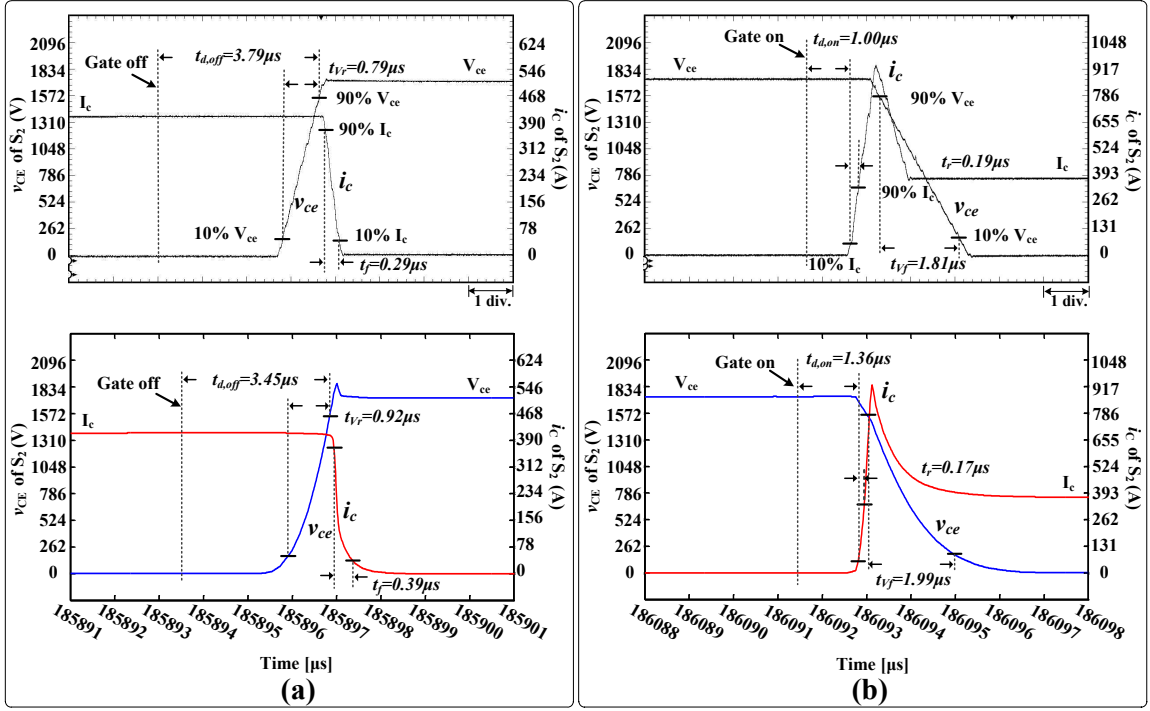
Figure 4.15: Device-level switching waveforms for IGBTs in single-phase 5-level MMC system from real-time hardware emulation (top sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure). Scale: (a)-(b) x-axis: $1\mu s$/div.

temperature of $\mathbf{S}_1$, $\mathbf{S}_2$, $\mathbf{D}_1$, and $\mathbf{D}_2$ (T_{vj}^{S1}, T_{vj}^{D1}, T_{vj}^{S2} and T_{vj}^{D2}) in first $5s$ and the zoomed waveforms during $0.5s$ are shown in Fig. 4.14 (a) and (b), respectively. Fig. 4.15 (a) and (b) show the switching transients of $\mathbf{S}_2$ during IGBT turn-off and turn-on (v_{CE} and i_C). Table 4.8 shows the averaged switching and conduction power losses between $0.175s$ and $0.225s$ from SaberRD® and FPGA hardware emulation. The apparent errors exist for device-level results, since the solver and IGBT module model used in the proposed model and SaberRD® are very different. The datasheet does not provide adequate data for switching power losses when the current through the IGBT module is low. The switching power losses from curve fitting in hardware emulation are higher than those from the off-line simulation results from SaberRD®, which can be observed from Fig. 4.13 (e) and (f). This explains the largest power loss error occurs in the reverse recovery loss of $\mathbf{D}_2$ in Table 4.8, where the smallest current goes through. The IGBT switching transient parameters are extracted based on the power losses and the current rise and fall time under rated cases. The linear interpolation scheme used to estimate the non-linear curves for other non-rated cases induced the errors. From the perspective of power loss matching, the transient time of non-linear SaberRD® waveforms are slightly longer than the linear curves from hardware emulation. The diode reverse recovery process greatly expedites the turn-on process of the IGBT, therefore t_r of IGBT from both the real-time and off-line simulation shown in Fig. 4.15 (b) is almost half the value in the datasheet, which is $0.4\mu s$. Since the

datasheet does not provide the detailed information for the drive circuit, they are simply modeled as the ideal voltage sources in series with the gate resistors in SaberRD®'s model, which caused the differences for turn-on and turn-off delay times. Despite all of the above, the hardware emulation and SaberRD® results are quite close.

Table 4.9 shows the average power dissipation and junction temperature of IGBTs and diodes for all SMs under steady-state operation. These data are collected from the real-time emulation after $369s$, which is more than 8 times longer than the largest thermal time constant ($45s$). The power losses and junction temperatures of the corresponding devices in different SMs are very close to each other, which verifies the advantage of even usage of SMs for PSC-PWM control scheme.

Table 4.8: Comparison of Power Dissipations of IGBTs and Diodes between SaberRD® and Real-Time Emulation on FPGA

Power Dissipation	SaberRD®	FPGA	Error
P_{on}^{S1}	60.6W	61.2W	1.0%
P_{off}^{S1}	41.7W	42.2W	1.2%
P_{cond}^{S1}	137.3W	134.4W	2.1%
P_{rr}^{D1}	72.2W	74.3W	2.9%
P_{cond}^{D1}	136.3W	130.3W	4.4%
P_{on}^{S2}	293.7W	280.1W	4.6%
P_{off}^{S2}	168.1W	163.6W	2.7%
P_{cond}^{S2}	722.0W	723.5W	0.2%
P_{rr}^{D2}	24.7W	26.8W	8.5%
P_{cond}^{D2}	13.5W	14.0W	3.7%

Table 4.9: Average Power Dissipation and Junction Temperature of IGBTs and Diodes in Steady-State Operation

| Arm	Sub module	S1		D1		S2		D2	
		P_{loss}	T_{vj}	P_{loss}	T_{vj}	P_{loss}	T_{vj}	P_{loss}	T_{vj}
Pos. arm	SM(1)	256.3W	72.44°C	243.2W	83.83°C	1425.1W	130.28°C	51.1W	64.81°C
	SM(2)	255.9W	72.40°C	242.9W	83.78°C	1424.2W	130.23°C	50.1W	64.68°C
	SM(3)	255.1W	72.31°C	239.5W	83.39°C	1424.3W	130.19°C	49.1W	64.53°C
	SM(4)	257.0W	72.48°C	242.3W	83.75°C	1425.8W	130.33°C	51.5W	64.86°C
Neg. arm	SM(1)	255.4W	72.31°C	239.6W	83.39°C	1424.7W	130.20°C	49.1W	64.54°C
	SM(2)	257.1W	72.49°C	242.7W	83.75°C	1426.3W	130.33°C	51.5W	64.86°C
	SM(3)	256.3W	72.44°C	243.3W	83.83°C	1425.0W	130.30°C	51.1W	64.81°C
	SM(4)	256.3W	72.41°C	243.0W	83.78°C	1424.3W	130.24°C	50.3W	64.70°C
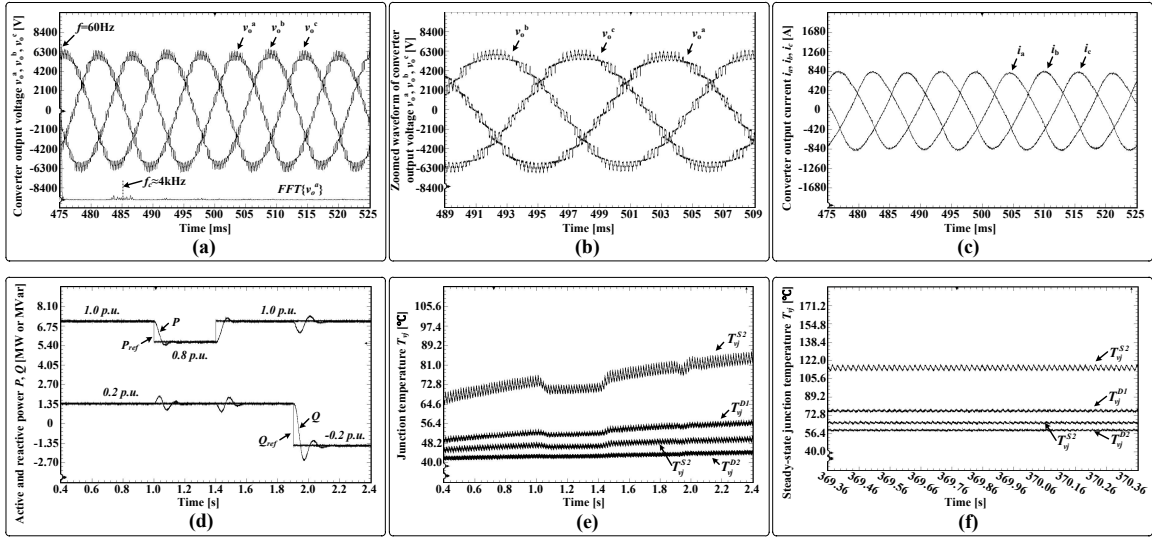
Figure 4.16: System-level and device-level results for three-phase 9-level MMC system from real-time hardware emulation (oscilloscope) at 500Hz switching frequency. Scale: (a) x-axis: $5.0ms$/div, (b) x-axis: $2.0ms$/div, (c) x-axis: $5.0ms$/div, (d)-(e) x-axis: $0.2s$/div, (f) x-axis: $0.1s$/div.

4.4.3   Results for Three-Phase 9-Level MMC

The emulated three-phase 9-level MMC is the largest circuit which can be configured in the Virtex-7 XC7VX485T FPGA board. Fig. 4.16 (a) and (b) show the converter output phase voltages (v_o^a, v_o^b, and v_o^c) during $50ms$ and the zoomed waveforms during $20ms$, while Fig. 4.16 (c) shows the output line current (i_a, i_b, and i_c). Fig. 4.16 (d) shows the active and reactive power tracking performance, with the rated power of 7 MW, and Fig. 4.16 (e) shows the junction temperature transients of the switching devices in the first positive arm SM of phase A during the same time period. Fig. 4.16 (f) shows the steady-state junction temperatures with 1.0p.u. active power and -0.2p.u. reactive power after $369s$.

4.5   Summary

This chapter proposed and demonstrated a device-level electro-thermal model for IGBT modules with the complex MMC system and its hardware emulation in real-time. The power losses and junction temperatures of IGBT modules can be used to determine the efficiency of the converter, which expands the function of real-time emulation. The modularity is not only inherent in the MMC sub-modules but also in the emulation hardware, which is presented as the independent calculation hardware units for all SMs. The proposed model is fully paralleled on the FPGA to be both latency and resource efficient. Therefore, the additional time delay cost for the electro-thermal model is very little. The resource utilization problem for larger MMC system can be solved by using multiple

advanced FPGA boards with larger capacities or combining the proposed device-level electro-thermal model and other simpler IGBT module models, such as two-state resistor model. The comparison with SaberRD® proves that the proposed model has sufficient accuracy. The small amount of error for device-level results are expected, since the transients are not generated by solving differentiation equations but from the manufacturer's datasheet. The more complete and accurate datasheet can further improve the accuracy of the transient results. However, for the purpose of tuning control parameters when running the real-time emulation, the accuracy for the power losses and junction temperatures is adequate.

5

MPSoC-Based Real-Time Emulation of Clamp Double Sub-Module MMC

5.1 Introduction

A major challenge of implementing MTDC or DC grid is the strict demand of safe operation under contingencies, especially the DC side fault, which can lead to a complete malfunction of the MTDC system and cause severe damage to the converter stations [1, 34]. One method of limiting DC fault current is the development of an effective DC circuit breaker, which also uses IGBT switches and can be expensive and have significant power losses [94,95]. Besides the DC breaker, the control of the converter station may provide the short-circuit current reduction with specific sub-module topologies. The half-bridge SM has the most simple topology; however, it cannot effectively block the DC fault current. This work focuses on the clamp double SM topology, which has the following characteristics among the fault tolerant topologies [19,96,97]:

1. providing the fault current limiting capability;

2. using smaller number of additional switching devices;

3. generating fewer power losses;

4. using simple control of IGBT switches for fault protection strategy.

These features make the CDSM topology a competitive candidate for MMC design and development.

Real-time electromagnetic transient simulation is commonly utilized HIL test for power system equipment, such as the control and protection systems [11,12,98,99]. An accurate

and efficient electromagnetic transient simulation is critical for the comprehensive and rigorous validation and analysis of MTDC systems. Therefore the modeling and hardware emulation of CDSM MMC in an MTDC system is the subject of this chapter. The CDSM also has the most complex structure compared with half-bridge and full-bridge SMs, which makes the modeling process the most challenging.

   The MMC circuit is composed of numerous SMs, that provide many voltage levels at the AC side of the converter station. Simplified or equivalent circuit schemes are used for the off-line and the real-time simulation of the MMC station, such as Thévenin equivalence method, surrogate network method, and equivalent circuit method [23, 48, 100]. The Thévenin equivalence method is suitable for a simple SM topology because the calculation of the SM can grow cubically with the increase of the internal nodes in the SM topology, which makes this method unsuitable for real-time simulation of CDSM MMC. Both surrogate network and equivalent circuit methods use multiple circuit topologies for finite combinations of IGBT gate signals and arm current direction, which are employed by RTDS® and OPAL-RT® real-time simulators, respectively. These methods calculate the capacitor voltages of individual SMs and can include some of the static electrical characteristics of the switching devices; however, these methods do not consider and present detailed temperature-dependent static and dynamic characteristics. In a realistic environment, multiple factors, especially junction temperatures, can have great influence on the performance of power electronics devices, and are determined by the operation of the electrical system. Considering multi-physics domains, which are the electromagnetic and thermal networks in this case, can effectively reflect the interactive phenomenon and increase the overall simulation accuracy.

   With complex converter topologies, control and protection schemes applied in the modern power system, using analytical calculation to estimate the power losses and the thermal information is difficult and inaccurate, especially during system contingencies. It is necessary to use accurate electromagnetic transient waveform considering the electrothermal dynamics to calculate the detailed device-level data, which are of great value for the system designers and operators. This work proposes a device-level electrothermal model of CDSM MMC for real-time emulation, which utilizes temperature-dependent electrical parameters, and presents the power losses, the junction temperatures, and the switching transients of the individual IGBTs and diodes during normal operation and fault conditions. The IGBT and diode characteristics are based on the piece-wise polynomial scheme. Compared with the conventional modeling scheme for CDSM MMC, the proposed modeling scheme has the following advantages:

1. increasing the accuracy of the system-level and device-level simulation;

2. providing the thermal data during fault condition, which is the critical information to evaluate protection schemes and parameters;

3. providing significant indicators for system designer to evaluate the thermal performance, which can be useful for IGBT module selection, heat sinker design, etc.;

4. helpful for converter control system designer to evaluate the overall energy efficiency and balance the thermal performance of all individual IGBT modules, and to adjust valve-level control scheme and control parameters.

For the real-time implementation of the CDSM MMC system, the Xilinx® ZCU102 board using XCZU9EG CPU/FPGA multi-processor system-on-chip device is chosen as the platform due to its high parallelism, high flexibility, and relative low design cost [30]. A three-terminal MTDC system composed of one CDSM MMC and two HBSM MMCs is used as the case study with $20\mu s$ as the system simulation time-step. The system is decomposed into three subsystems, and each contains one converter station. This chapter explains the parallelism from both algorithm and hardware implementation perspectives of the device-level, the converter-level, and the system-level. The 32-bit floating point precision is used for the emulation system, except for the switching transient waveform generation, which uses fixed-point data and can update the values on every FPGA clock cycle (10ns). PSCAD/EMTDC® and SaberRD® are employed to validate both system-level and device-level emulation results captured on the oscilloscope for steady-state operation and DC fault transient. This chapter describes the operation principles of CDSM and briefly explains the device-level electrothermal model and the interface for CDSM. The detailed partitioning, implementation of the MTDC system case study on the MPSoC platform are described, and the emulation results and their validation are presented.

5.2   Operation Principles of CDSM

The MMC is composed of multiple SMs in each converter arm as shown in Fig. 5.1 (a). The capacitors in submodules can be either inserted or bypassed by controlling the gate signals of IGBTs. Therefore multiple voltage levels can be generated forming the low-harmonic sinusoidal waveforms at the AC side. Inductors are connected in series with the SMs to suppress the circulating current.

Breaking DC over-current is a major challenge for the HVDC transmission system. If the capacitor voltage in the SM can be negatively inserted into the converter arm, the DC fault current can be decreased and limited rapidly due to the reversed DC side voltage at the converter. Multiple submodule topologies exist in literature and in practical projects [19, 34, 96]. Among them, the half-bridge SM, the full-bridge SM (FBSM), and the clamp double SM are the most popular ones shown in Fig. 5.1 (b)-(d). The half-bridge topology is the simplest one, although it can not reverse the polarity of the inserted capacitor voltage. The full-bridge submodule has the fault-tolerant capability with the cost of doubling the power electronics switches. In addition, the full-bridge SM provides the
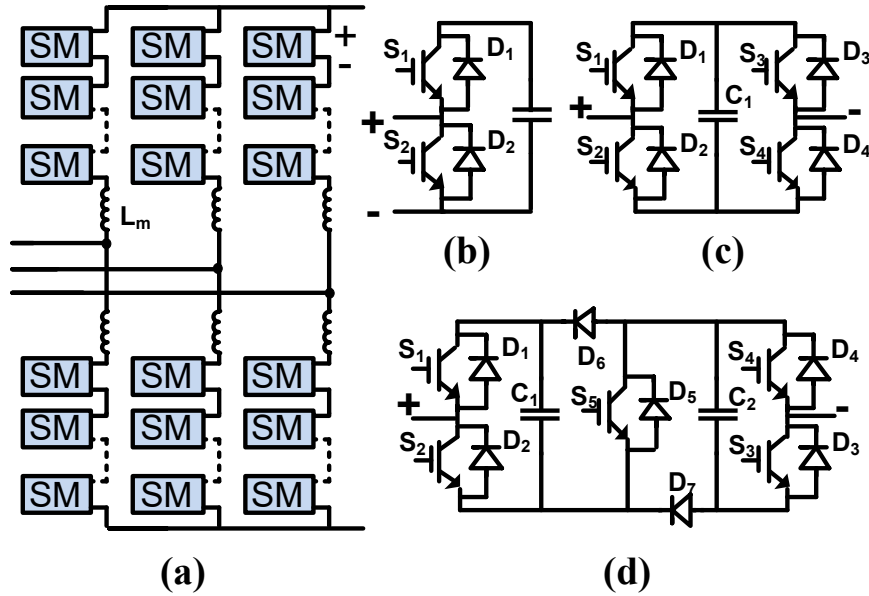
Figure 5.1: MMC and SM topologies: (a) modular multi-level converter, (b) half-bridge submodule, (c) full-bridge submodule, and (d) clamp double submodule.

capability of eventually changing the DC voltage rating and polarity, although it is normally not required for an HVDC system. As the name indicates, the CDSM contains two half-bridge SMs and a clamping circuit composed of two additional diodes and one IGBT module. One CDSM is equivalent to two FBSM providing the same voltage rating and levels; therefore the CDSM MMC utilizes fewer switches than FBSM MMC.

Fig. 5.2 presents some cases of the normal operation mode and the protection mode during faults. In normal operation, the IGBT gate signal of $\mathbf{S}_5$ is always on as shown in Fig. 5.2 (a)-(b). The existence of Diodes $\mathbf{D}_6$ and $\mathbf{D}_7$ can clamp the capacitor voltage to positive values and can prevent internal loop current. Thus, the two half-bridge structures are connected in series, and can be controlled independently. The IGBT modules of the half-bridge structures are numbered in such a way that if the odd number switches are turned on, the corresponding capacitor is inserted in the converter arm. By doing so, the control scheme of HBSM MMC is compatible to the CDSM MMC during normal operation. When a fault is detected, $\mathbf{S}_5$ and other gate signals will be turned off. The capacitor voltages are inserted into the arm limiting the fault current with opposing polarity. In Fig. 5.2 (c), current flows from the negative side to the positive side with $-Vc$ inserted, which will go through capacitors C_1, C_2 or both in parallel based on the comparison of the capacitor voltages. In Fig. 5.2 (d), current flows from the positive side to the negative side with $+2Vc$ inserted. Table 5.1 lists the operation modes of each half-bridge structure for Case I when $\mathbf{S}_5$ is on combined with any SM current direction and Case II when $\mathbf{S}_5$ is off combined with positive SM current, while Table 5.2 lists the modes of CDSM for Case III when $\mathbf{S}_5$ is off combined with negative SM current.
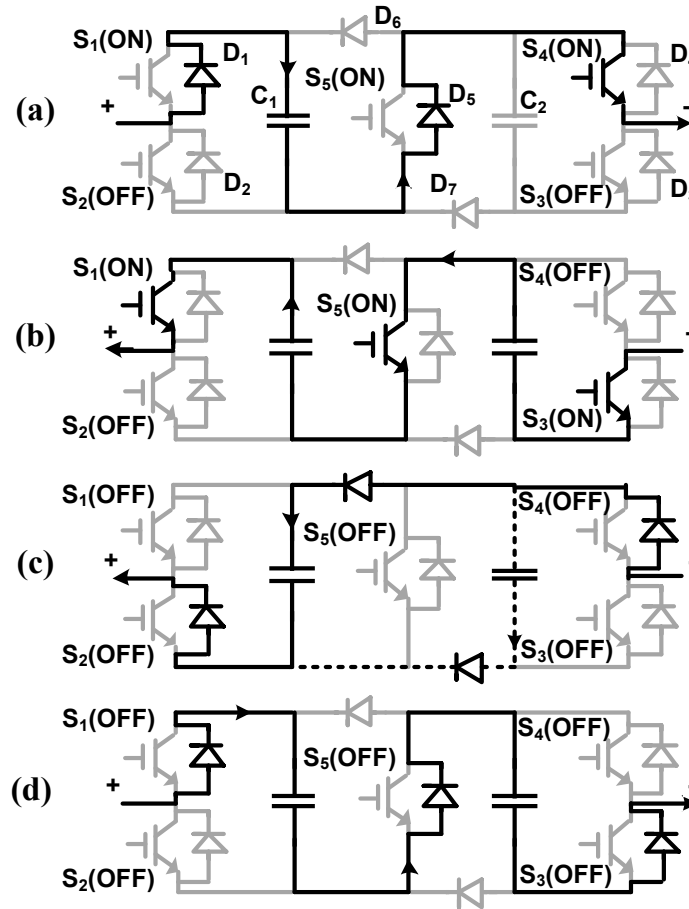
Figure 5.2: CDSM operation demonstration: (a) normal operation with positive arm current, (b) normal operation with negative arm current, (c) protection mode with negative arm current, and (d) protection mode with positive arm current.

Table 5.1: Operation Mode of Each Half-Bridge Structure: Case I (S_5 Turned-On Combined with any SM Current Direction) and Case II (S_5 Turned-Off Combined with Positive SM Current)

Mode	S_1/S_3	S_2/S_4	Current direction	Inserted voltage
Insert	1	0	+/-	$+Vc_1/+Vc_2$
Bypass	0	1	+/-	0
Block	0	0	+	$+Vc_1/+Vc_2$
	0	0	-	0
Fault	1	1	+/-	0

1 (0) means turned-on (turned-off), and + (-) means current flows from SM positive side to negative side (negative side to positive side).

Table 5.2: Operation Mode of CDSM: Case III (S_5 Turned-Off Combined with Negative SM Current)

Mode	S_1	S_2	S_3	S_4	$Vc_1 vs Vc_2$	Inserted voltage
Positive Insert	1	0	1	0	$Vc_1 < Vc_2$	$+Vc_1$
					$Vc_1 = Vc_2$	$+Vc_1/+Vc_2$
					$Vc_1 < Vc_2$	$+Vc_2$
Negative Insert	0	1/0	0	1/0	$Vc_1 < Vc_2$	$-Vc_2$
					$Vc_1 = Vc_2$	$-Vc_1/-Vc_2$
					$Vc_1 < Vc_2$	$-Vc_1$
Bypass	1	0	0	1/0	Any	0
	0	1/0	1	0		
Fault	1	1	1/0	1/0	Any	0 or Vc_2
	1/0	1/0	1	1		0 or Vc_1

5.3 Device-Level Electrothermal Model of CDSM

This section proposes the device-level electrothermal model of CDSM, which can accurately simulate the thermal conditions of the IGBT modules. It describes the proposed modeling schemes and explains the parallelism from algorithm perspective, which includes device-level, SM-level, and converter-level modeling schemes.

5.3.1 Device-Level Modeling Scheme

Device-level modeling refers to the generation of the circuit model of individual IGBT modules and diodes, which are the voltage source v_{sw} (subscript sw indicates the IGBT module or diode) in series with the resistor r_{sw} as shown in Fig. 5.3 (a). In this work, the detailed device-level electrothermal model of the IGBT modules for CDSM MMC is built using the information obtained from the manufacture's datasheet for the Infineon® FZ400R33KL2C_B5 IGBT module [91]. The algorithm contains the temperature-dependent electrical interface parameter calculation, the power loss calculation, the thermal network calculation, and the device-level linearized transient waveform calculation.

5.3.1.1 Temperature-Dependent Electrical Interface Parameter Calculation

The electrical interface of the IGBT or diode is composed of the voltage source v_{sw} in series with a resistance r_{sw}. The temperature-dependent IGBT and diode output characteristics can be obtained from the datasheet, as shown in Fig. 5.4 (a). The piece-wise polynomial
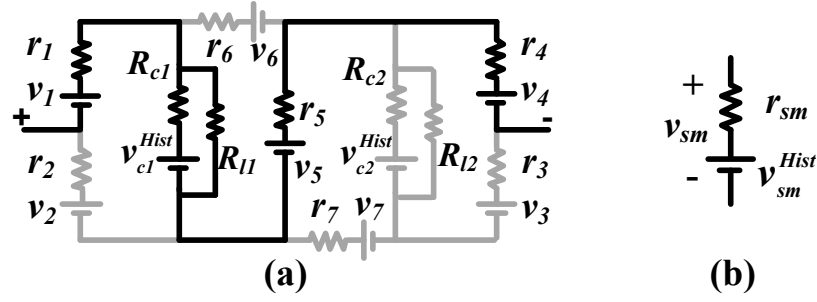
Figure 5.3: CDSM models: (a) complete circuit model with active route and (b) simplified SM interface model.
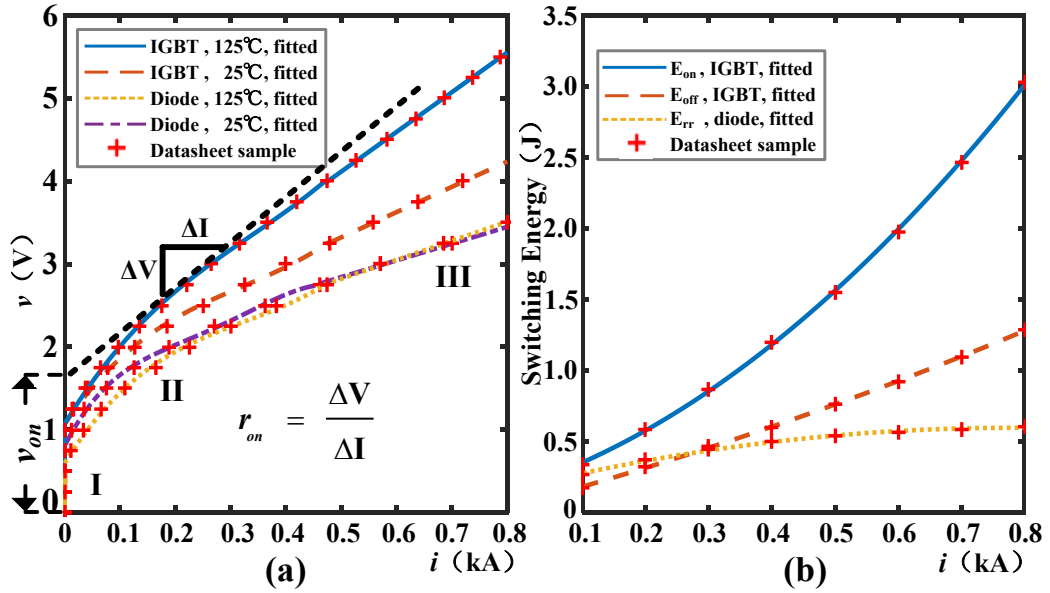
Figure 5.4: Datasheet sample and fitted curves of the Infineon® FZ400R33KL2C_B5 IGBT and diode characteristics: (a) output characteristics of IGBT and diode at $125°C$ and $25°C$ and (b) switching energy losses of IGBT turn-on, IGBT turn-off and diode reverse recovery processes at $125°C$.

curve fitting scheme is applied, with the following equations:

$$v(i) = \sum_{i=0}^{n} a_n i^n, \ r_{sw} = \frac{\mathbf{d}v}{\mathbf{d}i} = \sum_{i=0}^{n-1} b_n i^n, \ v_{sw} = v(i) - r_{sw}i, \tag{5.1}$$

where v and i are the voltage and current across the device; a_n and b_n are the correspondent polynomial coefficients. In this work, the curve is divided into three sections: the threshold section, the nonlinear section, and the linear section. In the threshold section, since the current is very small and has negligible influence on the electrical and thermal performance, the device is simply modeled as a large fixed resistor. In the nonlinear section, a third- or a fourth-order polynomial function is used, while the first-order fitting is applied when current is large in the linear section or section III as shown in Fig. 5.4 (a).
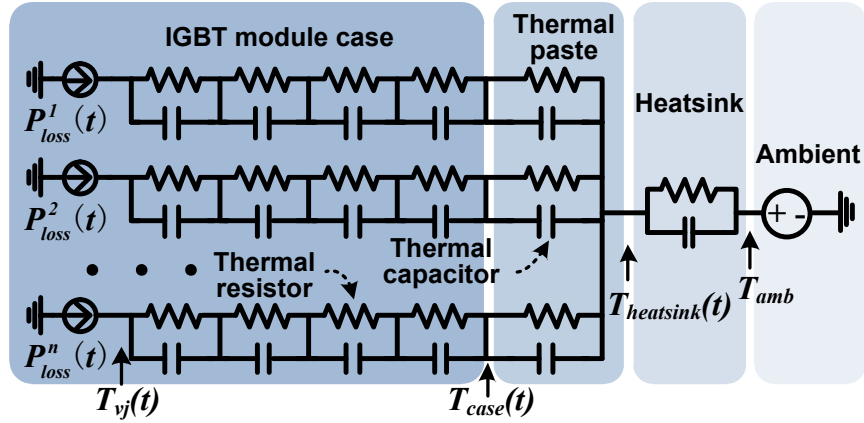
Figure 5.5: Equivalent circuit for IGBT module thermal network.

Since the datasheet only provides the characteristics at $T_1 = 25°C$ and $T_2 = 125°C$, linear interpolation is applied to calculate the values at arbitrary temperatures, which can also be used for other temperature-dependent variables given in datasheet, such as switching energy, IGBT current rise, fall time, etc. Taking the example of r_{sw}, the interpolation equation is given as:

$$r_{sw}(T_{vj}) = \frac{T_{vj} - T_2}{T_2 - T_1}(r_{sw}^{T_2} - r_{sw}^{T_1}) + r_{sw}^{T_2}, \tag{5.2}$$

where T_{vj} is the junction temperature of the corresponding device.

When using equivalent circuit method for SM-level modeling, only a portion of the devices are turned on in a certain operation case. Therefore, not all device-level model parameters are required for the calculation of SM interface. However, if the thermal performances of all power electronic devices in the SM are required to be monitored, the conditions and variables for all devices shall be calculated and stored.

5.3.1.2 Power Loss Calculation

After solving the system circuit matrix, the arm current is obtained, and the SM capacitor voltage can be updated. This data along with the IGBT gate signals can be used to calculate the power losses of the individual IGBTs and diodes. The power losses of the power electronic switches are mostly composed of the conduction power losses and the switching power losses. The conduction power loss P_{cond} is given as:

$$P_{cond}(t) = (r_{sw}(T_{vj})i(t) + v_{sw}(T_{vj}))i(t). \tag{5.3}$$

The switching energy at $125°C$ is given by the datasheet as shown in Fig. 5.4 (b). The switching energy E_{switch} is assumed to be proportional to the voltage between the device when turned off. The fitting equation using second-order polynomial function is given as:

$$E_{switch}(i(t), v(t)) = (\sum_{i=0}^{2} a_n i^n)\frac{v(t)}{v_{rated}}, \tag{5.4}$$

where v_{rated} is 1800V in this work. The switching energy at $25°C$ is also given at the rated test condition, where current is 400A when IGBT/diode turned on. The complete energy curve at $25°C$ can be estimated following the proportional relation of the rated condition. The switching energy at an arbitrary temperature can then be estimated using linear interpolation similar to (5.2). The total power losses is calculated as:

$$P_{loss}(T_{vj}) = P_{cond}(T_{vj}) + \frac{E_{sw}(T_{vj})}{\Delta t}, \tag{5.5}$$

where Δt is the simulation time-step.

5.3.1.3   Thermal Network Calculation

The obtained power losses of the individual switches are the inputs to the thermal network as shown in Fig. 5.5. The thermal network contains 6 stages of thermal impedances from the semi-conductor junction to the case, the thermal paste, the heatsink, and the ambient. Each thermal impedance is composed of a thermal resistor and a thermal capacitor, and multiple devices can be mounted on the same heatsink. Table 5.3 presents the impedances in the form of resistances and time constants, where Z_{thjc}, Z_{thch}, and Z_{thha} represent the impedances from the junction to the case, the case to the heatsink, and the heatsink to the ambient environment, respectively. In this work, multiple IGBT modules are connected in parallel and in series to provide sufficient current and voltage rating for the MMC system. It is assumed that the paralleled IGBT modules are mounted on the same heatsink. The junction temperature is calculated using the Trapezoidal integration rule as follows:

$$\begin{aligned}
T_{vj}(t) = \sum_{i=1}^{5}(\frac{R_{th}^i \cdot \Delta t}{2\tau_{th}^i + \Delta t}(P_{loss}(t) + P_{loss}(t - \Delta t)) + \frac{2\tau_{th}^i - \Delta t}{2\tau_{th}^i + \Delta t}\Delta T_{th}^i(t - \Delta t)) + \\
\frac{R_{th}^6 \cdot \Delta t}{2\tau_{th}^6 + \Delta t}(P_{total}(t) + P_{total}(t - \Delta t)) + \frac{2\tau_{th}^6 - \Delta t}{2\tau_{th}^6 + \Delta t}\Delta T_{th}^6(t - \Delta t) + T_{amb},
\end{aligned} \tag{5.6}$$

where P_{loss} and P_{total} is the power loss of the device and the total power losses of the devices in the same heatsink; T_{amb} is the ambient temperature; $\Delta T_{th}^i(t - \Delta t)$ is the history temperature across impedance Z_{th}^i. The calculated junction temperatures are then used to update the temperature-dependent parameters.

5.3.1.4   Device-Level Linearized Transient Waveform Calculation

This work uses linearized waveforms for the IGBT transients in [12, 14]. The rise time and fall time of the IGBT are obtained from the datasheet, which are temperature dependent.

Table 5.3: Thermal Impedances of the Thermal Network

Device	Parameter	$i=1$	$i=2$	$i=3$	$i=4$	$i=5$	$i=6$
IGBT	$R_{th}^i[K/kw]$	11.475	6.375	1.53	6.12	12	5
	$\tau_{th}^i[s]$	0.03	0.1	0.3	1	3	45
Diode	$R_{th}^i[K/kw]$	22.95	12.75	3.06	12.24	24	5
	$\tau_{th}^i[s]$	0.03	0.1	0.3	1	3	45
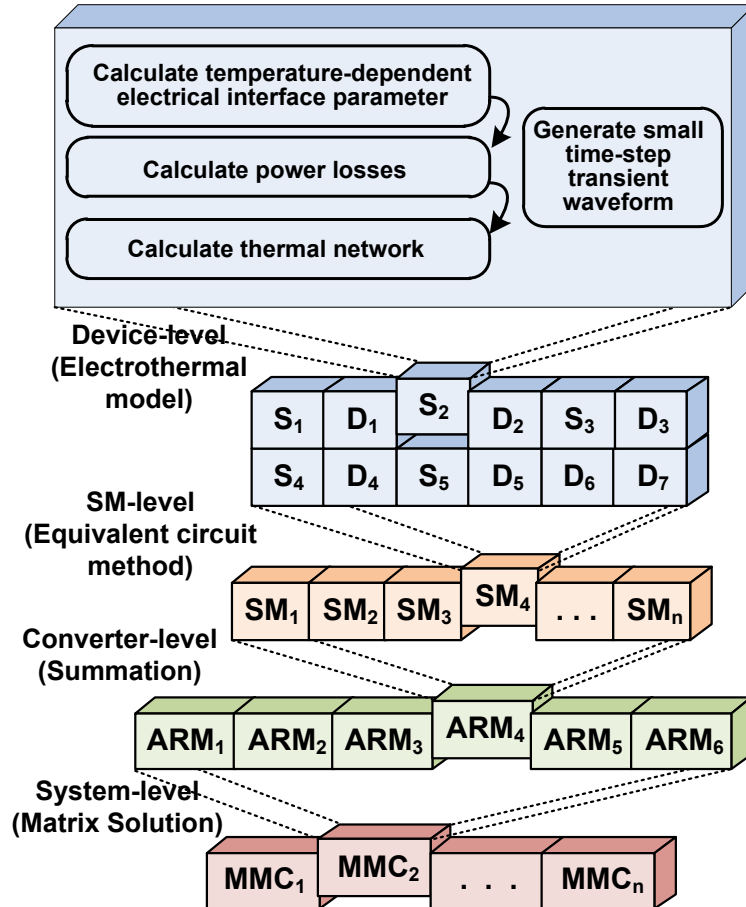
Figure 5.6: Hierarchical illustration of MMC modeling algorithm.

The slope of the transient is assumed to remain constant, therefore the rise time and fall time of the current and voltage waveform are proportional to the values of the turn-on current and turn-off voltage of the device, respectively. Since the datasheet only provides the rise time and fall time of the current waveform, the corresponding fall time and rise time of the voltage waveform are estimated by the switching energy losses.

5.3.2 SM-Level Modeling Scheme

The task of SM-level modeling is to obtain the simplified SM model composed of the voltage source and resistor. Multiple simplification schemes were developed in the literature

such as Thévenin equivalence method, surrogate network method, and equivalent circuit method [23, 48, 100]. The SM-level modeling schemes can be significantly different among the above-mentioned schemes. The computation effort of determining Thévenin equivalent is similar to solving the matrix equation of the SM circuit model. The number of effective nodes is calculated as the total nodes of the circuit topology minus one, which is assumed to be the ground node. The HBSM only contains two effective nodes, while the CDSM topology contains 5 effective nodes. The computation effort increases cubically with the matrix size to be solved, which is the same as the number of effective nodes. Therefore it can be computationally expensive to use Thévenin equivalence method to calculate for all the CDSMs.

This work uses multiple equivalent circuits for different switching combinations, which is essentially the same as the surrogate network method, and the equivalent circuit method. With a certain switching combination, current flows into some determined branches. The leakage current of the IGBT module can be as small as several milliamperes, and is therefore neglected. Under most operating conditions, there is only one current path between the terminal nodes. Fig. 5.3 (a) shows the CDSM circuit model, and the black path indicates the active current route, when S_1 and S_4 are turned on. The capacitor is modeled as the impedance R_c in series with the history voltage source v_c^{Hist} using Trapezoidal rule, and a leakage resistance R_l is also included.

The SM-level model can be obtained by summing the circuit model elements of the devices in the active path to a voltage source in series with a resistor, as shown in Fig. 5.3 (b). The determination of the circuit topology is based on the gate signals of the IGBTs, the current direction and the relation between the two capacitor voltages as listed in Table 5.1 and 5.2. Occasionally, symmetrical current paths may happen, which can be easily combined by adding the conductances of the two paths.

5.3.3 Converter-Level Modeling Scheme

The MMC has a large number of switching devices and relatively complex circuit topology, which is a major challenge for its modeling and simulation. To accelerate the computation speed, the size of the system matrix shall be minimized. In this work, equivalent voltage sources and impedances are used for all SMs. Using the arm current of the last time-step, the simplified SM model can be summed to a single voltage source to interface with the external circuit. Therefore, the nodes of the interface elements for the converter arms are substantially decreased, and all SMs can be calculated in parallel.

Fig. 5.6 illustrates the major algorithm of the proposed electrothermal CDSM MMC model. The complete electromagnetic transient simulation of MMC system is composed of device-level, SM-level, converter-level, and system-level calculation. The sequential relation exists between different levels, which means only when the interface elements of the fundamental level are obtained, the results of the next level can be accomplished. The

(a)

(b)
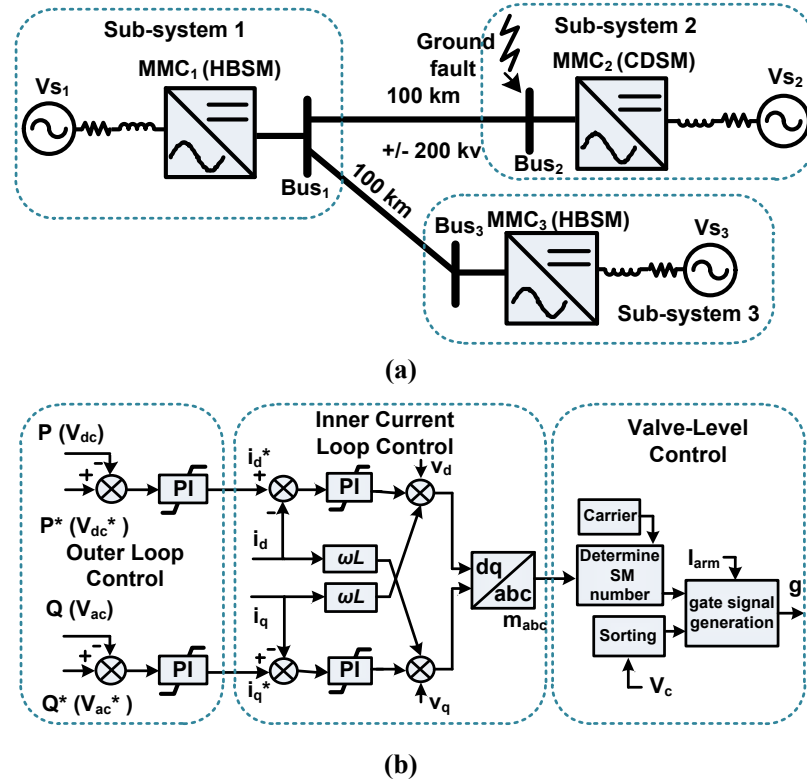
Figure 5.7: (a) Circuit topology of MMC-based three-terminal MTDC system and (b) control diagram of MMC. (The signals with the superscript * are reference signals.)

calculation among the units of the same level can be parallelized well. When expanding each level, the amount of the paralleled device-level units is substantial and requires large computation capability. The parallelism also exists in each calculation step of the device-level modeling scheme.

5.4   Case Study and Hardware Implementation

A three-terminal DC system is used as the case study as shown in Fig. 5.7 (a) to illustrate the effectiveness of the proposed modeling schemes. The MTDC system is composed of two HBSM MMC stations and one CDSM MMC station connected by two 100km +/-200kV DC transmission lines. The major parameters of the case study are listed in Appendix. A ground fault of both poles at **Bus**$_2$ is applied to the test condition. Since this work is focused on the modeling of CDSM MMC, the electrothermal model is only used for **MMC**$_2$, while **MMC**$_1$ and **MMC**$_3$ are using equivalent circuit models. All MMCs have 17 levels, which means that each MMC arm has 16 HBSMs or 8 CDSMs. To provide sufficient current rating and voltage rating, four FZ400R33KL2C_B5 IGBT modules or diode are connected in parallel, and 14 such paralleled structures are connected in series [91]. The transmission lines are modeled using distributed line or Bergeron model.
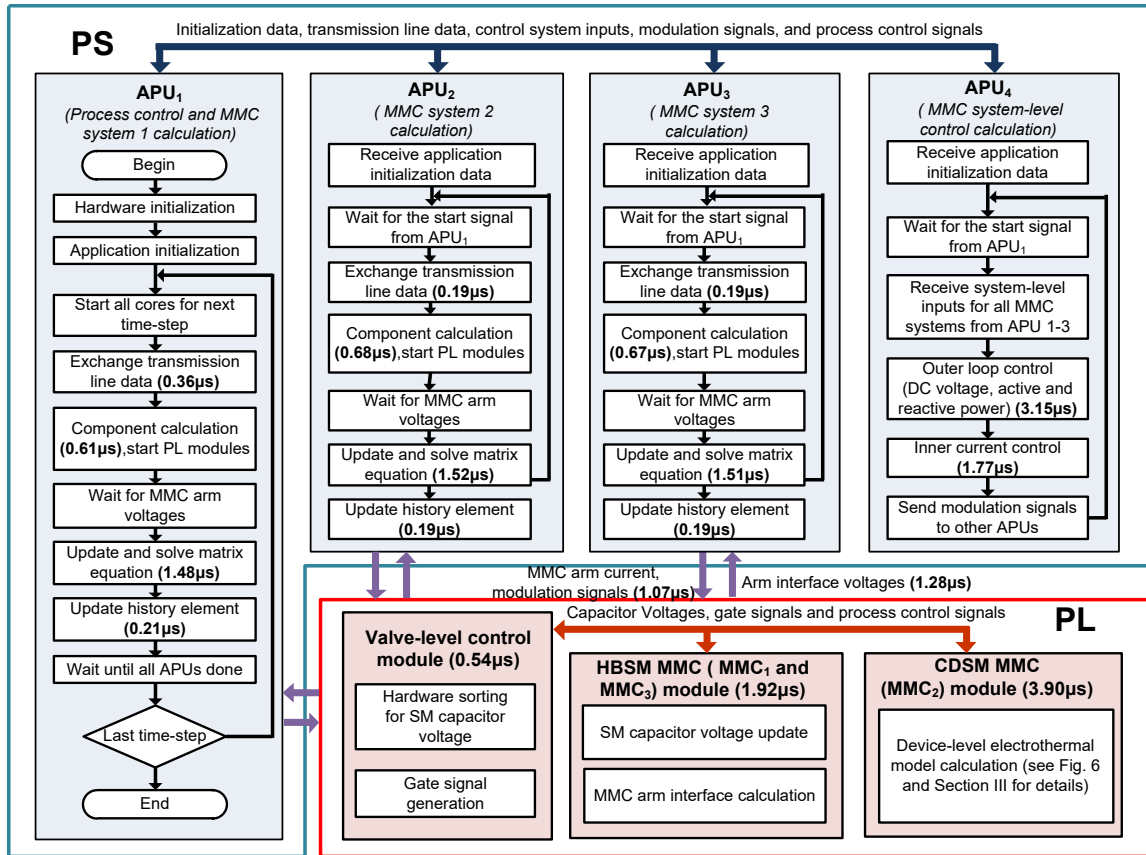
Figure 5.8: The design of the MTDC emulation system.

5.4.1 Design Partition

The computation of the MTDC system is allocated to the four APU cores and programmable logic resources of the Zynq UltraScale+ MPSoC system. The major challenge of the partition process is to minimize the communication latency between different computation units. In other words, the exchanged data between different units shall be minimized. As discussed in the last section, programmable logic is more suited for highly paralleled tasks, which are the MMC SMs related computation in this work. To save the PL resource, other computations are located in PS part, though some of them could be accelerated in PL.

With the above consideration, the system design is first partitioned into the three sub-systems separated by the distributed line model. Besides the process control signals for synchronizing purpose, the exchanged data during periodic calculation is only the history current of the transmission line model. The system matrix can also be divided into three smaller sub-matrices. One APU core is responsible for the calculation of each sub-system, and the fourth core is used for the system-level control calculation which generates the modulation signals for valve-level control. The valve-level control requires the SM capacitor voltage sorting process and generates gate signals for all SMs, which needs a large

amount of data exchange from the SM calculation units. Therefore the valve-level control is located in PL section to avoid the long latency between PS-PL communication.

Fig. 5.8 shows the major computation processes of all applied units in Zynq UltraScale+ MPSoC. APU 1 is the master core which controls the simulation processes. At the beginning, it executes the hardware initialization, which includes waking up other cores, setting system counter, and initializing the PL module. Then it begins the initialization of the application, which are the calculation of the circuit element parameters, and the variable initialization. The initialized data is sent to other cores during the receiving process.

Then the periodic calculation begins, APU 1-3 can execute simultaneously for the correspondent sub-systems. They first exchange the transmission line data, and then calculate the variables for other components, such as the transmission lines, arm inductances, voltage sources, etc. In the meantime, the valve-level control, HBSM MMC, CDSM MMC modules of the sub-systems on PL will start their respective calculations. With all variables calculated, the system matrix equations are calculated and the history data of the transmission lines and the inductances are then updated. APU 1 will first wait for the accomplishment of other cores and then wait until the next time-step comes in real-time before entering to the next loop. The system-level control can have its independent time-step, and can transfer its system-level control data with a fixed delay. It uses classical dq-axis decomposition and PI controllers for the DC voltage and power outer loop control and the inner current loop control as shown in Fig. 5.7 (b) [5, 21]. In this work, the control on APU 4 uses the same time-step as the simulation time-step, and transfers its control variables during the component calculation process of other cores.

On the PL, the valve-level control module generates the gate signals for the HBSM MMC and CDSM MMC module using capacitor voltage sorting based control scheme [21]. Hardware sorting of n capacitor voltages in one converter arm is implemented with full $\frac{n(n-1)}{2}$ times comparison, which can be conducted in parallel. By adding the corresponding one-bit comparison results, the sequence is generated. Compared with sequential software sorting, hardware sorting is substantially faster, which uses two FPGA clock cycles (20ns) for the SMs in one arm. It is noted that software sorting can also use $\frac{n(n-1)}{2}$ times comparison in the worst case scenario, which must be considered for real-time application. In HBSM MMC module, the major tasks are the SM capacitor voltage update and MMC arm interface calculation. The interface calculation for SMs in one arm is conducted in parallel. The interface voltage sources of SMs are summed to generate the arm interface, and then sent back to corresponding APU cores. The general process of CDSM MMC is similar to the more complex process of the SM interface generation, where the device-level electrothermal model is applied as described in Section III.
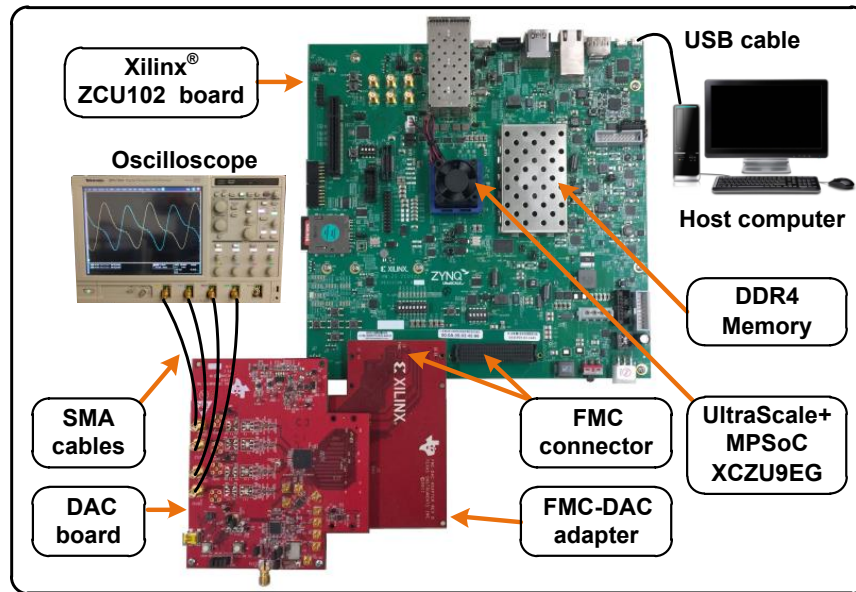
Figure 5.9: Hardware setup of the emulation system on the MPSoC.

Table 5.4: Resource Consumption of Modules on PL

Module	LUT	FF	DSP
Valve-level control module	24635 (9.0%)	8234 (1.5%)	0 (0%)
HBSM MMC module	13896 (5.1%)	12390 (2.3%)	135 (5.4%)
CDSM MMC module	213104 (77.7%)	160800 (29.3%)	970 (38.5%)
Available	274080 (100%)	548160 (100%)	2520 (100%)

5.4.2   Latency and Resource Consumption

The latencies of the major processes during the periodic calculation are shown in Fig. 5.8. For instance, the calculation time for the component calculation takes 0.61μs and the calculation of the matrix equation takes 1.48μs on APU 1. The calculation time on different APU cores has slight variance due to the minor difference of the included components. For instance, MMC system 2 contains the two-state resistance connecting to the ground for short circuit test purpose, and MMC system 1 contains two outgoing transmission lines. Although the computation can be fully paralleled on FPGA resources as long as the algorithm allows, it may not be necessary and can consume much hardware resource. Multiplexing and pipelining are used for the resource optimization. The valve-level control module for one arm takes 30ns, and it takes 540ns for 18 arms in 3 MMCs by multiplexing.
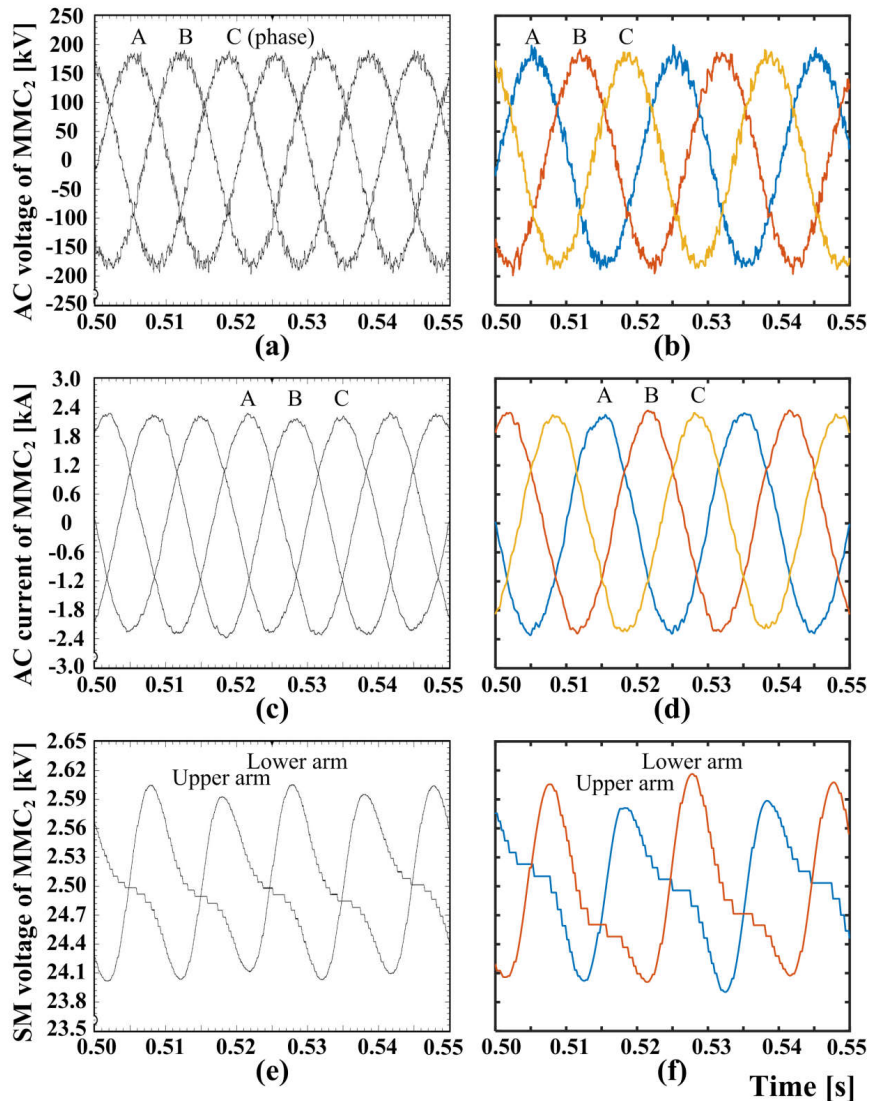
Figure 5.10: Steady state results: (a) (b) AC voltages, (c) (d) AC currents, and (e) (f) SM voltages. (The left sub-figures are real-time results, and the right sub-figures are offline PSCAD/EMTDC® results.)

The HBSM MMC module includes three sets of the paralleled arm calculation units, and the CDSM MMC module has two sets of arm calculation units. The resource consumption for the modules are listed in Table 5.4, which is relevant to the allocation of corresponding arm-level units. In other words, the resource consumption can be lower with a higher cost of the latency by using fewer paralleled units. Another strategy to reduce the resource consumption and increase the MMC level number is applying hybrid modeling scheme by using both electrothermal model and simple equivalent circuit model in the same MMC, which will be developed in future work.
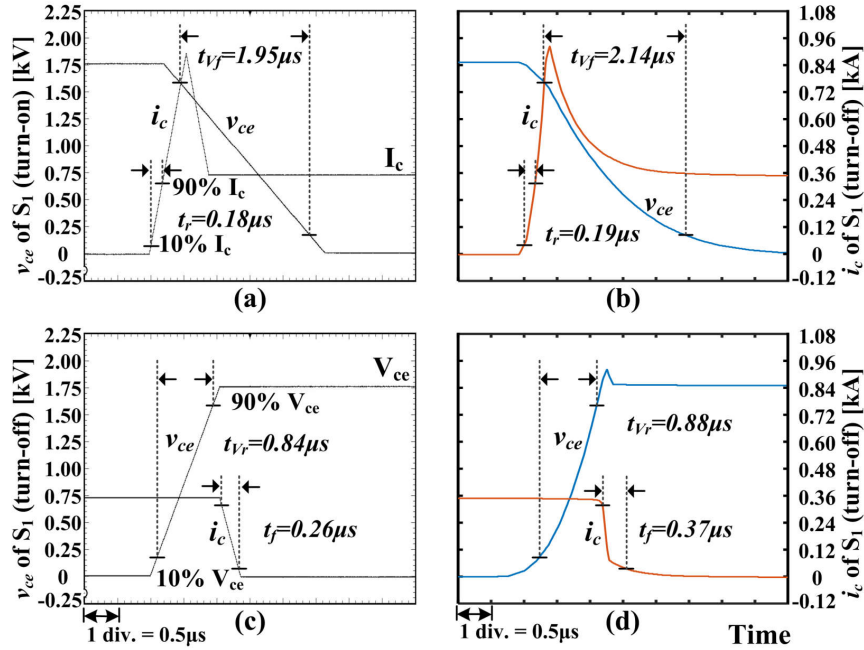
Figure 5.11: Voltage and current switching transient waveforms of $\mathbf{S}_1$: (a) (b) turn-on process and (c) (d) turn-off process. (The left sub-figures are real-time results, and the right sub-figures are offline SaberRD® results.)

5.5   Real-Time Emulation Results and Analysis

Fig. 5.9 presents the hardware setup of the emulation system. A host computer downloads the programming files including the bitstream to the Xilinx® ZCU102 MPSoC board through the USB cable and the on-board JTAG chip. The Zynq board contains the UltraScale+ MPSoC XCZU9EG device, DDR4 memory and various I/O devices, etc. On the Zynq device, the CPU cores are running at 1.2GHz, while the FPGA is running at 100MHz. The real-time results are transferred to the digital-to-analog converter through the FMC connector and the FMC-DAC adapter. The analog results are then collected on the oscilloscope through SMA cables.

5.5.1   Steady-State Results

Fig. 5.10 presents the CDSM MMC AC voltages, AC currents, and the first SM capacitor voltages of the upper and lower arm in phase-A. The left-side oscilloscope results are compared with the right-side PSCAD/EMTDC® results. The small control error can be accumulated and can lead to different conditions of SMs, especially for the voltage sorting based algorithm. Therefore the switching patterns for individual SMs cannot exactly match between the real-time results and PSCAD/EMTDC® results, which explains that the overall performance matches quite well, however the harmonics can have small differences. Fig. 5.11 presents the turn-on and turn-off switching transients of $\mathbf{S}_1$. The results
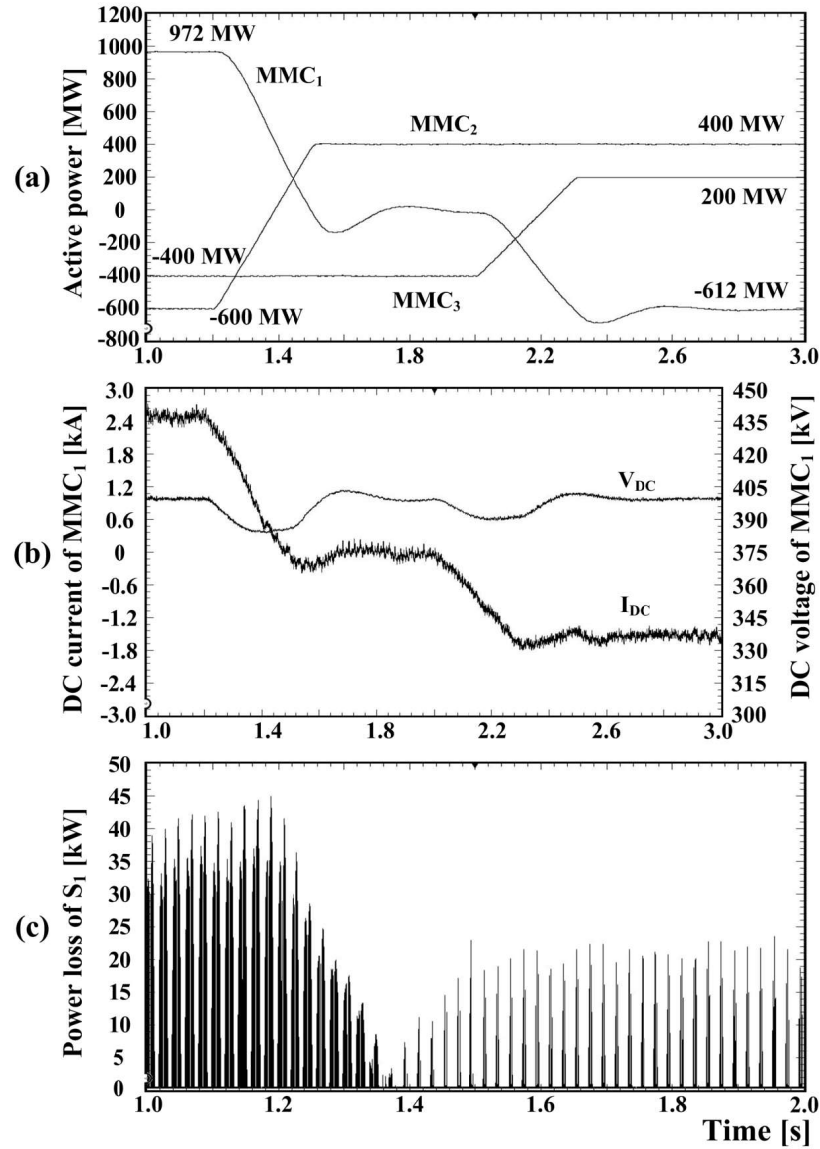
Figure 5.12: (a) Active power of **MMC$_1$**, **MMC$_2$** and **MMC$_3$**, (b) DC current and DC voltage of **MMC$_1$**, and (c) power loss of **S$_1$**.

are compared with SaberRD®, which uses detailed datasheet-based device-level behavior model for IGBT and diode. The current rise time t_r, current fall time t_f, voltage rise time t_{Vr}, voltage fall time t_{Vf} are measured, with the definition of 10% to 90% change of the steady-state I_c and V_{ce} as shown in Fig. 5.11. The overshoot current during the turn-on process is generated due to the reverse-recovery current of the turn-off of D_2. The linearized waveforms can give a good estimation of the switching transients based on the datasheet.
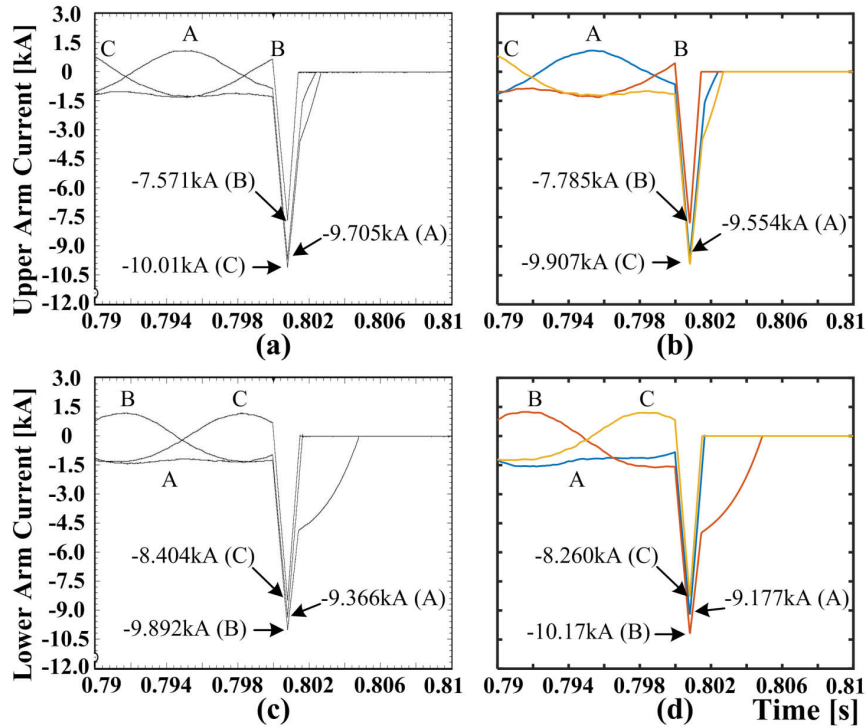
Figure 5.13: Arm current transients: (a) (b) upper arm currents, (c) (d) lower arm currents. (The left sub-figures are real-time results, and the right sub-figures are offline PSCAD/EMTDC® results.)

5.5.2   DC Power Flow Control

This subsection presents the test results of the power flow control of the MTDC system as shown in Fig. 5.12. Among the three MMC stations, **MMC**$_1$ maintains the DC voltage of the MTDC grid, while **MMC**$_2$ and **MMC**$_3$ control the power flow. All the MMCs can adjust the reactive power of the corresponding AC systems independently. The reference active power of **MMC**$_2$ changes from -600MW to 400MW from 1.2s to 1.5s of the simulation run, and the reference active power of **MMC**$_3$ changes from -400MW to 200MW from 2.0s to 2.3s of the simulation run. The positive direction of the active power is defined as the direction from the DC side to the AC side of the converter. The reactive power of the converter is all controlled to be 0MVar. As shown in Fig. 5.12 (a), the reference power tracking performances of **MMC**$_2$ and **MMC**$_3$ is satisfactory, and the power flow of **MMC**$_1$ can eventually reach steady-state with the disturbance due to the regulation of DC voltage. Fig. 5.12 (b) shows the change and variation of DC current and DC voltage of **MMC**$_1$. Fig. 5.12 (c) shows the power loss of **S**$_1$ (**MMC**$_2$), which first decreases to almost 0kW and then rises to a steady condition during the power flow reverse.
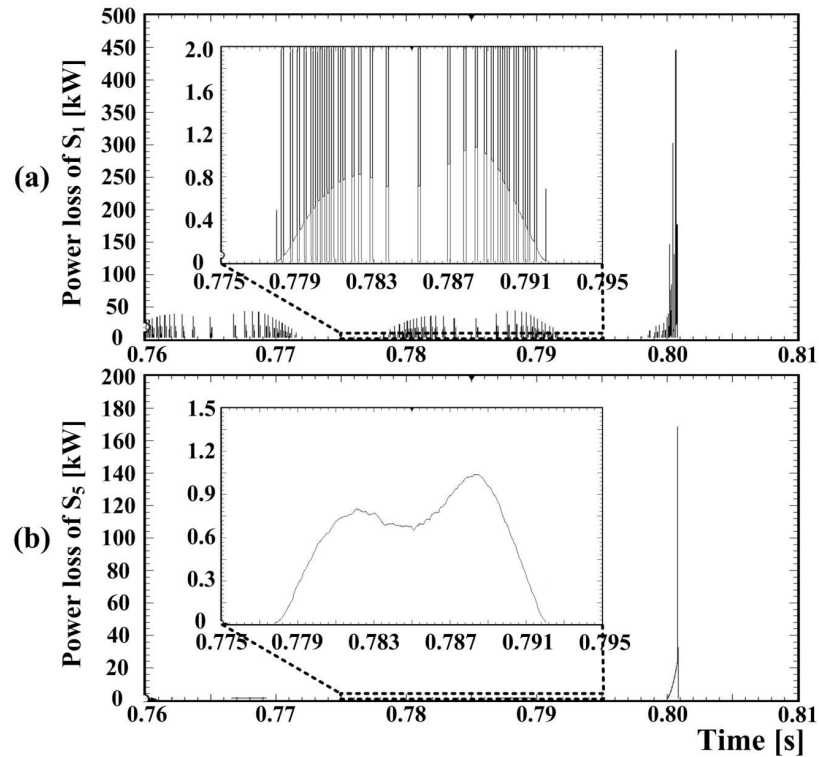
Figure 5.14: Power losses on oscilloscope: (a) power loss of $\mathbf{S}_1$ and (b) power loss of $\mathbf{S}_5$.

5.5.3   DC Fault Transient Results

A DC ground fault is applied to the case study system at 0.8s of the simulation run. Once the instantaneous over-current is detected which is +/-10kA in this work, the protection mode is activated and $\mathbf{S}_5$ is turned off. The capacitor voltages are then inserted into the arm with the reversed polarity to suppress the fault current. Once the arm current reaches 0, the breaker in the converter arm is then opened. Fig. 5.13 shows the comparison of the arm current fault transients of the upper and lower arms between the real-time results on the oscilloscope and the PSCAD/EMTDC® results. It is observed that the rate changes during the decrease of the current. It happens because when the other arm current in the same converter leg reaches 0, the effective circuit topology is changed. Fig. 5.14 presents the power losses of $\mathbf{S}_1$ and $\mathbf{S}_5$ in the first CDSM of phase-A upper arm. The conduction power losses of the switches are zoomed between 0.775s and 0.795s. The switching power is not exactly instantaneous power, but the average power during every simulation time-step. The power losses during the fault transient are substantially larger than the losses during steady-state operation. The composition of the power losses between $\mathbf{S}_1$ and $\mathbf{S}_5$ is very different due to the different switching pattern of the devices. $\mathbf{S}_5$ is always turned on unless the protection mode is active. Therefore, during normal operation, there are only conduction power losses. Fig. 5.15 shows the junction temperatures of all devices in the first CDSM in phase-A upper arm, which are compared with SaberRD® results.
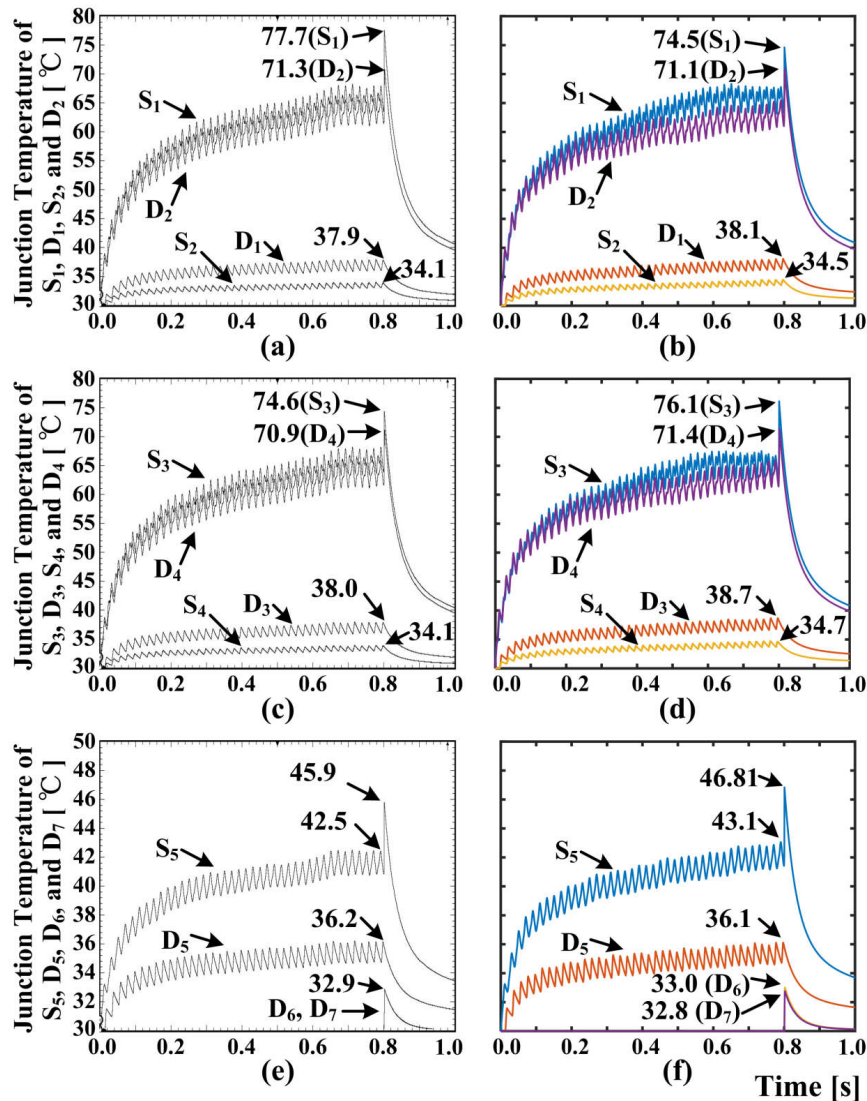
Figure 5.15: Junction temperatures: (a) (b) S_1, D_1, S_2, and D_2, (c) (d) S_3, D_3, S_4, and D_4, and (e) (f) S_5, D_5, S_6, and D_7. (The left sub-figures are real-time results, and the right sub-figures are offline SaberRD® results.)

Due to the difference of the switching pattern, the existence of the MMC loop current, the junction temperatures can be quite different for the devices though they may have same electrothermal characteristics. When the fault happens, the junction temperatures of the active devices first rise sharply due to the abnormally high power losses, then decrease to a lower value since the converter is shut down. Due to the assumption that the paralleled devices are mounted on the same heatsink, the junction temperatures of D_6 and D_7 are not influenced by other devices and do not change until the fault mode is active. When S_5 is turned off, the two capacitor voltages are balanced very quickly, and D_6 and D_7 evenly share the current as long as they have same characteristics. The proposed method assumes that the voltages will be instantaneously balanced, otherwise numerical oscillation may

occur with EMT type algorithm. It explains that the junction temperatures of $\mathbf{D}_6$ and $\mathbf{D}_7$ are exactly same in oscilloscope results, while there is a minor difference in the SaberRD® results. Due to the difference of the modeling schemes and solution methods between the proposed method and SaberRD®, a small amount of error is expected.

5.6 Summary

This chapter proposed the device-level electrothermal model for CDSM MMC for the real-time simulation of MTDC system on an MPSoC. The design and partition of the emulation system are described in detail. The system-level waveforms, device-level waveforms, power losses, and junction temperatures of individual switches were collected and validated with PSCAD/EMTDC® and SaberRD®. The detailed device-level results can be further used to evaluate the switch condition under normal operation and contingency for a specific control and protection scheme. Such a comprehensive real-time emulation is necessary for the safe operation of the MTDC system.

6

Off-Line Simulation of the AC/DC Grid

6.1 Introduction

This chapter is focused on the efficient and accurate electromagnetic transient simulation of a complex AC/DC transmission system on PSCAD/EMTDC®. The proposed AC/DC grid integrates the CIGRÉ DC grid test system, IEEE 39-bus system, and wind farms, as shown in Fig. 6.1 [2, 101]. The DC grid is specifically focused on in this work, which employs various converter topologies including modular multi-level converter, 3-level neutral-point-clamped converter, 2-level converter, and four-quadrant DC/DC converter.

Among the different converter topologies, the MMC has the advantages of low switching frequency, low harmonics, and high modularity, which is also challenging for electromagnetic transient simulation due to the complex circuit topology [12, 18, 19]. Thévenin equivalence scheme is often used for MMC modeling to reduce the number of electrical nodes [23]. Instead of using the two-state resistor for IGBT module modeling, this work proposes the piecewise polynomial curve fitting modeling method for the IGBT module in the MMC sub-modules to increase the simulation accuracy.

The computation effort for EMT simulation can increase significantly with the scale of the AC/DC grid. Model reduction or model equivalence is often adopted to decrease the calculation time for a large system. For instance, average value model and switching function model can be used to model AC-DC converters instead of using discrete switching devices [2, 20].

In this work, a *hybrid modeling scheme* is applied to the system, which is defined as utilizing multiple model complexities of the converters and other elements at different locations in the EMT-type simulation for the purpose of obtaining optimal performance of both accuracy and simulation speed. The most detailed model is used for the most in-
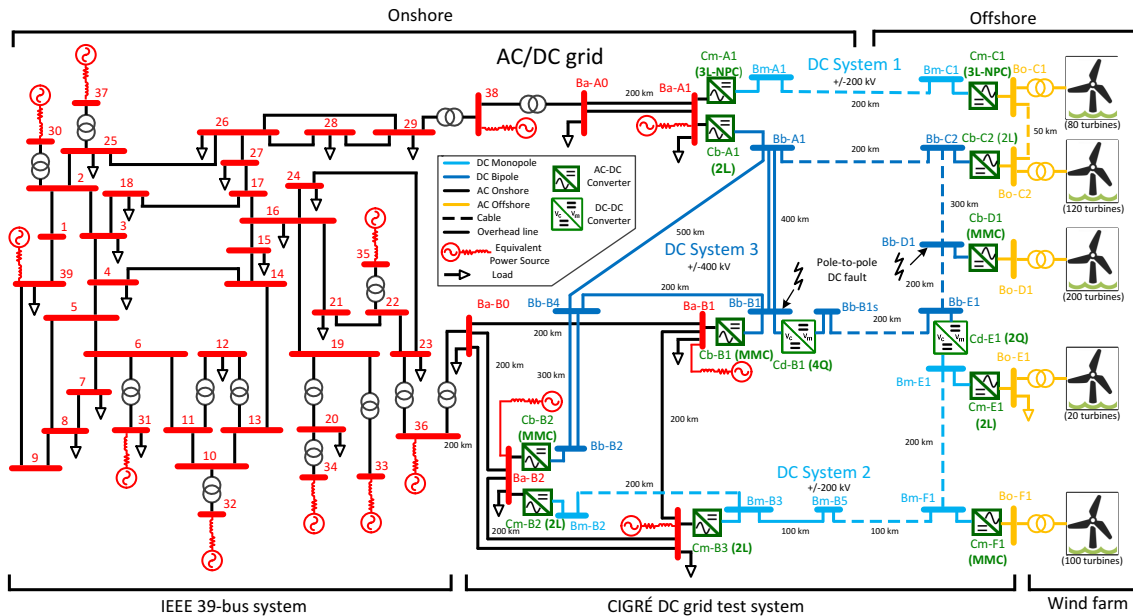
Figure 6.1: Topology of the AC/DC grid.

teresting component or area. Two criteria of zone division are defined. The system can be partitioned into study zone and external zone based on the simulation purpose. The study zone contains the nodes and components where the transient event happens or detailed observation is required, and the external zone contains the rest of the components. The system can also be partitioned into a detailed zone, accurate zone, and averaged zone based on the model complexity. For a specific circuit and simulation purpose, the study zone is given, for instance, the fault location, the location of the controller and protection relay requiring parameter tuning. It can be challenging to determine the zones of different model complexity to achieve optimal performance of efficiency and accuracy. This work proposes three zone partition schemes based on distance, node number, and network coupling with result comparison. The circuit topology reduction is not applied in this work to ensure the flexibility of changing the study zone. By changing the model complexity, the components at any location can be included in the study zone.

The major contribution of this work is the proposed MMC modeling method, the detailed electromagnetic simulation of the complex AC/DC grid, and the zone partition schemes using different converter model complexities. A matrix mapping scheme is proposed in this work to illustrate the zone partitioning. This chapter describes the AC/DC grid, the modeling schemes for various components, and the zone partition schemes. The case studies and the simulation results are described and presented.
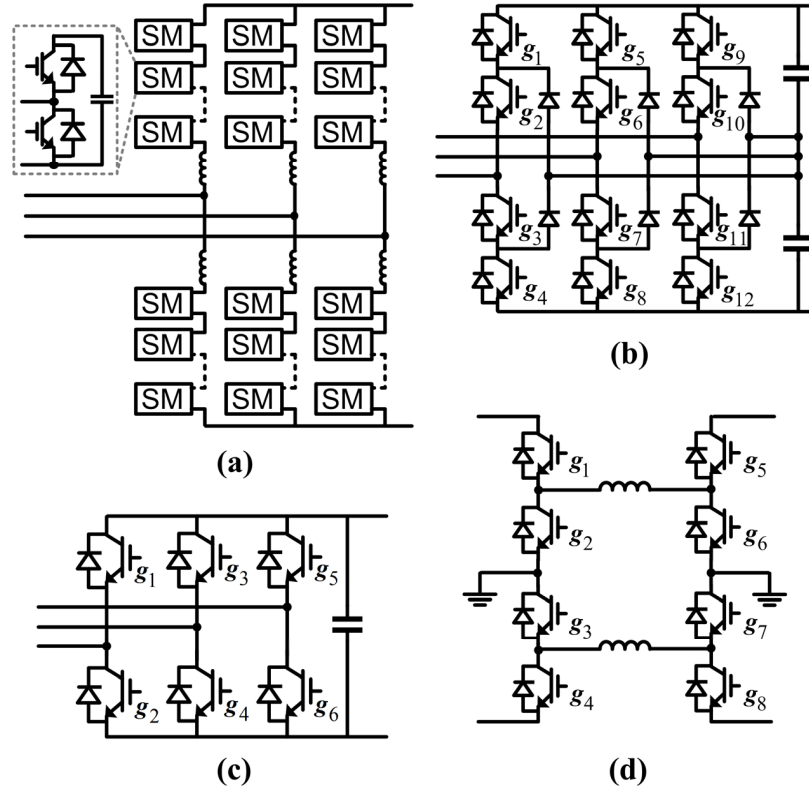
Figure 6.2: Topologies of converter: (a) modular multi-level converter, (b) three-level neutral-point-clamped converters, (c) two-level converter, and (d) four-quadrant DC/DC converter.

6.2 AC/DC Grid Description and Hybrid Modeling

As shown in Fig. 6.1, the AC/DC grid is composed of onshore IEEE 39-bus system, the offshore wind farms and the CIGRÉ DC grid test system, which emulates a modern transmission system efficiently integrating renewable energy sources. The CIGRÉ DC grid, which contains 3 DC transmission systems, was designed by CIGRÉ working groups as a common reference for DC grid study [2]. In the original report, MMCs are used for all the AC-DC converters with averaged model [2]. In this work, hybrid converter topologies, including MMC, 3L-NPC converter, and 2L converter, are adopted with the topologies shown in Fig. 6.2 (a)-(c), for the purpose of presenting a more variant and realistic test scenario. Four-quadrant DC/DC converter is applied for Station Cd-B1 (Fig. 6.2 (d)), while two-quadrant DC/DC converter is used for Station Cd-E1 (right side or left side of Fig. 6.2 (d)). For convenience, 60 Hz is used for all the AC transmission systems, although the AC system frequency connecting the wind farms can be different. The control diagram of the AC-DC converter is shown in Fig. 7.2, which is composed of outer loop control, inner current loop control, and the pulse width modulation (PWM) generator. The voltage droop control is added to regulate the DC voltage for power sharing. For MMC, phase dis-
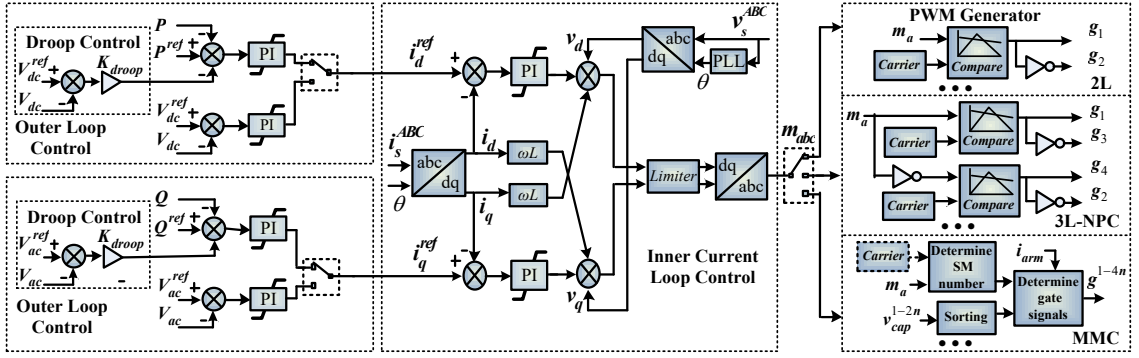
Figure 6.3: AC-DC converter control scheme.

position method is used for capacitor voltage balancing, which is equivalent as staircase modulation for high-level MMC [21].

The electromagnetic transient simulation is conducted for the proposed AC/DC grid with hybrid modeling complexity. Among various components, the converters, especially the MMCs, in the DC grid are specifically focused on for accurate modeling in this work. The proposed piecewise polynomial curve fitting method for MMC modeling is described in detail, while different types of models for converters and other elements are briefly reviewed.

6.2.1 Proposed Modeling Scheme for MMC

The topology and the circuit model of a half-bridge MMC SM are shown in Fig. 6.4 (a) and (b). Each IGBT module, containing an IGBT and an anti-parallel connected diode, is modeled by series connected nonlinear resistor and voltage source representing the slope resistance r_{on} and the threshold voltage v_{on} in this work to increase the modeling accuracy compared with the two-state resistor model conventionally applied for Thévenin equivalence based MMC model. The leakage resistance R_{leak} is added in parallel with the capacitor, modeled with series connected equivalent resistor R_c and history term v_c^{Hist}. Fig. 6.4 (d) shows the output characteristics of the IGBT and diode from the manufacturer's datasheet [91].

This chapter proposes the scheme of applying multiple polynomial functions to fit the highly nonlinear characteristics, as the following equations:

$$v(i) = \sum_{i=0}^{n} a_n i^n, \tag{6.1}$$

$$r_{on} = \frac{\mathbf{d}v}{\mathbf{d}i}, \qquad v_{on} = v(i) - r_{on}i. \tag{6.2}$$

The entire v-i curve is divided into three sections. Section I is the region where current is very small and grows exponentially with the increase of the voltage. The current
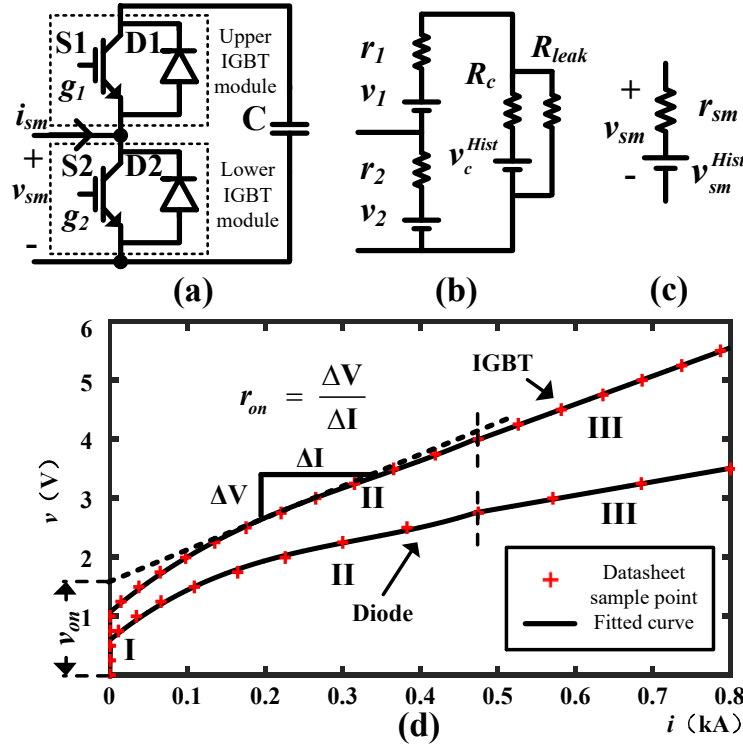
Figure 6.4: SM modeling scheme: (a) half-bridge structure, (b) circuit model, (c) Thévenin equivalence model, and (d) output and forward characteristics of IGBT and diode.

in Section I has little impact on the system simulation and is normally not presented in the datasheet. Therefore a large constant resistance is used to model this region. Section II is modeled with a third order polynomial function for the nonlinear characteristics. Higher orders can obtain extra accuracy, however, with the cost of extra computation burden. When the current increases, the resistive relation dominates; therefore, Section III is modeled with a first-order equation. More sections can also be applied to improve the fitting accuracy and can ease the issue of discontinuity of the section boundaries. Since the SM current is the same in one arm, the additional calculation time for the nonlinear resistance and voltage sources is small and does not increase with the SM numbers. The fitted parameters of polynomial functions for the IGBT and diode characteristics and their corresponding fitting errors are listed in Table 6.1.

The exact resistances and voltage source values of the upper and lower IGBT modules (r_1, v_1, r_2, and v_2) are determined based on the gating signals and the direction of the SM current i_{sm}. Thévenin equivalence is then applied for node elimination, given as follows:

$$v_{sm}(t) = r_{sm}i_{sm}(t) + v_{sm}^{Hist}(t - \Delta t), \tag{6.3}$$

where

$$r_{sm} = \frac{((R_c + R_{leak})r_1 + R_c R_{leak})r_2}{(R_c + R_{leak})(r_1 + r_2) + R_c R_{leak}}, \text{and} \tag{6.4}$$

Table 6.1: Fitted Parameters of Polynomial Functions for IGBT and Diode Characteristics

Device	Section II					Section III		
	a_3	a_2	a_1	a_0	error	a_1	a_0	error
IGBT	19.332	-19.501	11.118	1.069	1.50%	4.787	1.720	0.16%
Diode	25.950	-25.319	10.743	0.598	2.48%	2.292	1.675	0.36%

The voltage and current are in the units of V and kA, correspondingly.

$$v_{sm}^{Hist}(t - \Delta t) = \frac{(v_c^{Hist}(t - \Delta t) - v_1 - v_2)(R_{leak} + R_c)r_2}{(R_c + R_{leak})(r_1 + r_2) + R_c R_{leak}} + v_2. \tag{6.5}$$

Then the SM equivalent resistor r_{sm} and history term v_{sm}^{Hist} of the same arm are summed to form the interface for the system-level circuit. With the proposed model, the detailed waveforms of both the capacitors and individual IGBT modules can be presented accurately as well as the conduction power losses of switches. Because the datasheet only provides the current range of normal operation, the curve fitting may not be accurate if an extreme large current goes through the device. In this work, the proposed model is realized by designing user-defined module with Fortran code in PSCAD/EMTDC®.

6.2.2 Two-State Resistor Model

The two-state resistor model uses a resistor with two distinct values to present the switching state, which are a small value for on-state and a large value for off-state. This model is a simple type of discrete switch model, while it cannot represent the detailed and accurate characteristics of IGBT modules.

6.2.3 Switching Function Model

The switching function model uses the voltage sources at AC side and the current source at DC side, with the waveforms controlled by the IGBT gate pulses, DC side voltage and AC currents. The circuit topology is similar for various converter types, except for the additional arm inductors in MMC. For the MMC, the switching function model can not be used to verify the capacitor voltage balancing algorithm, since the voltages are assumed to be the same. Since the value of the equivalent voltage source and the current source is based on the data of last time-step, errors and even oscillation may occur, which can also happen for the average value model.

6.2.4 Average Value Model

The average value model uses similar topology as the switching function model, except using the fundamental frequency waveform instead of switching function waveforms. For different converter topologies, the harmonics induced by switched waveform are ignored.

Therefore, this model cannot effectively differentiate multiple converter topologies and can not be used to analyze the converter harmonics. For the MMC, especially with high levels, the system-level waveforms will not seem very different compared with the other detailed modeling schemes during steady-state operation. When using averaged model, the PWM control is not necessary and can be neglected, which saves the computation effort for controllers.

6.2.5 Wind Farm

The wind farm by itself can be a complex system, which may involve hundreds of generation units. The fixed-speed wind generator is used in this work, composed of the wind turbine, drive train, induction machine, pitch angle controller, compensating capacitor, and step-up transformer [101]. A controlled current source is connected in parallel with the single wind turbine modeled in detail, which has the value of n-1 (n is the number of the wind generators in a wind farm) times the current going through the single unit. In this way, the wind farm can be represented by the duplication of a single generation unit. If the wind farm is not the object of interest, it can be simplified to be a single induction machine or even an equivalent voltage source in series with impedance. Alternately, more detailed and complex wind turbine models, such as variable-speed wind generator based on doubly-fed induction machine and the corresponding converters, can also be included.

6.2.6 Transmission Line/Cable and Other Elements

The major transmission line and cable models include frequency dependent model, Bergeron model (traveling wave model), and PI section model (at fundamental frequency), etc. The first two types are distributed model, while the third one is a lumped model. The distributed model presents the delay property of traveling waves, which can be used to effectively and conveniently decompose the entire circuit topology into multiple sub-systems. The PI section model has a straightforward topology with few data input; however, it cannot decompose the system topology, and can consume longer computation time for a large system. For DC transmission line, high frequency harmonics induced by converter switching can be significant instead of the fundamental frequency of AC system. Therefore, the Bergeron model is not sufficient and accurate for DC transmission line system even under steady-state operation. The system also contains other elements, such as transformers, synchronous generators, etc. The AC system model can be made more complex by including the nonlinearities, such as the saturation and hysteresis of transformers.

   The judgment of the accuracy and efficiency of a certain model is highly dependent on the application. The major focus of this work is the AC-DC converter modeling with multiple topologies and different modeling complexity. In this work, other elements are considered as control variables, and use fixed and feasible modeling schemes. Since this work adopts relatively simple topology of DC/DC converters, the DC/DC converters use

discrete switches for modeling without further simplification. In the IEEE 39-bus system, the Bergeron model is used for AC transmission lines, since only the impedance of system frequency is provided, and the voltage source in series with impedance is used to represent the generators. Frequency dependent modeling is applied to the DC transmission lines and cables.

6.3   Grid Partition Schemes

To optimize the accuracy and efficiency of the electromagnetic simulation of large AC/DC grid, the converter modeling of multiple complexities is applied for different zones. This section describes three partition schemes based on distance, node number, and network coupling. In addition to the application in this work, the circuit partitioning schemes has wide applications, such as the hybrid simulation of transient stability and electromagnetic transient simulation, and node tearing for parallel calculation.

6.3.1   Distance

The modeling scheme can be simpler if the distance is far from the center of the study zone, which can be a single node or multiple nodes. The scheme is based on the assumption that the longer distance of transmission lines can have larger impedance and need longer latencies for the traveling waves, and the components at remote locations can have minor and delayed effect on the electromagnetic transients. This scheme is straightforward, and has most clear and certain criteria for partitioning. It is particularly useful when the circuit topology is similar to the tree structure without forming loops at remote end as shown in Fig. 6.5 (a), which is common for a distribution network. A case disobeying this scenario could be the existence of a remote electrical bus which has multiple paths connecting to the study zone as shown in Fig. 6.5 (b), which is common in a transmission network. This remote bus will be partitioned into the accurate or averaged zone by the scheme based on distance; however, it has significant influence to the study zone. This drawback can also happen on the node number based scheme.

6.3.2   Node number

The electrical nodes between the converter location and the center of study zone can be another significant indicator for zone partition. Simpler models can be used for the converters when the electrical node number is large. Actually, the node number shall refer to the one existing in the matrix equation instead of the circuit topology. The determination of exact node numbers can be challenging, which requires detailed knowledge of modeling scheme and solution algorithm of a specific EMT software. The node elimination scheme for a certain element or a group of elements can be different for various programs. For simplicity and certainty, the electrical nodes in this work refer to the ones existing in the circuit
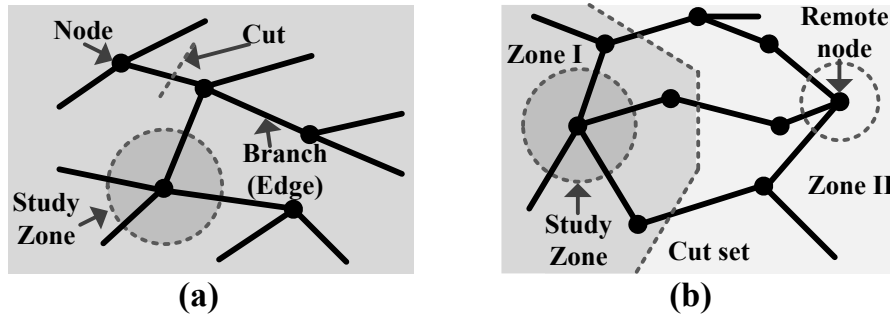
Figure 6.5: Circuit topology: (a) tree structure, (b) mesh structure.
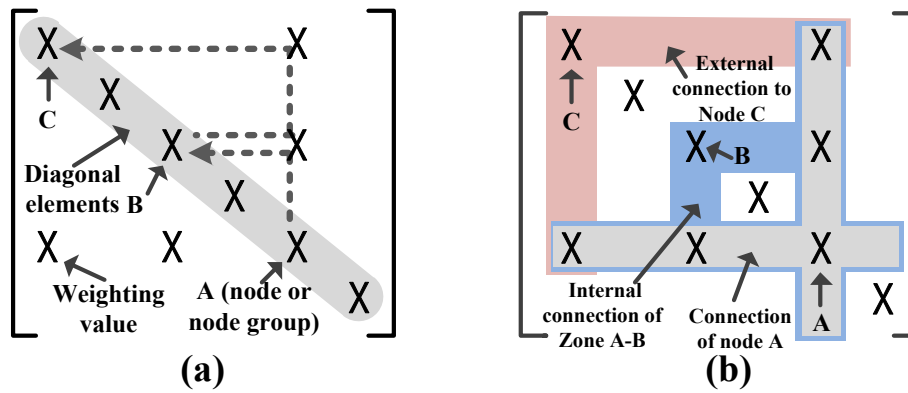
Figure 6.6: Matrix mapping scheme: (a) node number illustration, (b) connection layer illustration.

topology, which are the AC and DC buses in the case study. A matrix mapping method is proposed to illustrate the concept of node number partitioning, which is similar to the procedure of constructing the conductance matrix. The diagonal element, which is a cross, stands for the circuit node or bus in the circuit topology. Whenever a connection exists between two nodes, crosses are symmetrically placed at the intersection of corresponding rows and columns of the two nodes. The dashed line, which must go through the off-diagonal cross, as shown in Fig. 6.6, is a connection between the two buses. The node number is the minimum off-diagonal crosses for all possible routes between two nodes. For example, the node number between Node A and Node B is 1, while the node number between Node B and Node C is 2. The node number can be determined from either the circuit topology or the proposed matrix mapping. The elements in a conductance matrix stand for the conductances connecting to a node, while the cross in the matrix mapping may represent a group of nodes or elements for the purpose of presenting the connectivity or coupling relation of a circuit topology. The off-diagonal elements can be later replaced by other meaningful values to represent the connectivity.

6.3.3   Network coupling

Network coupling refers to the coupling strength between components or sub-networks. If multiple paths exist between two components, they are considered strongly coupled. In many cases, the coupling of the electromagnetic field is much weaker than direct galvanic connection. Galvanic isolation can be a criterion for zone partition. Especially under contingency conditions, the fault may have a significant impact on the area without galvanic isolation though far from the study zone. The nominal power flow and short circuit capacity is another factor. With large power flows between two networks, the coupling strength is considered strong. The partition process is to apply a cut set for the circuit topology. A weighting function can be applied for each branch, considering the above aspects, including galvanic isolation, power flow, etc. In addition, the size of each zone can be applied as the constraint to determine the cut set. More future research work is needed to determine the appropriate weighting function and the corresponding coefficients. The process can also be interpreted as the matrix mapping scheme. As shown in the Fig. 6.6 (b), the top layer, which covers the row and column of Node A, indicates the connections of Node A; the middle layer indicates the internal connections of the zone composed of Nodes A and B; the bottom layer indicates the external connections of Zone A-B. The weighting value can replace the off-diagonal crosses. Finding minimum total coupling strength is equivalent to finding the zone with the minimum sum of the weighting values located in the bottom layer. It is noted that the matrix mapping does not necessarily give a more intuitive solution than the circuit topology graph, while it offers a different perspective to observe the circuit.

In this work, the DC grid is composed of three DC systems. There are limited connections between the DC systems, and the DC/DC station does not provide galvanic isolation. Therefore the coupling between DC Systems 3 and 2 is deemed stronger than the coupling between DC Systems 3 and 1. This work uses the naturally existed partitioning of the three DC systems in the CIGRÉ DC grid, while the above-mentioned schemes can be developed for a more general circuit in future work.

6.4   Case Studies and Simulation Results

This section presents the simulation results of various tests and case studies, to verify the proposed MMC modeling scheme, compare the converter modeling of different complexities, and illustrate the hybrid modeling schemes, in the following three sub-sections, respectively. The CIGRÉ DC grid test system is used for the first two sub-sections, while, for the third sub-section, the complete AC/DC grid is utilized. For the MMCs in DC System 1 and 3, there are 200 sub-modules in each arm; for the MMCs in DC System 2, there are 400 sub-modules in each arm. The converter types used for different converter stations are listed in Table 6.2.
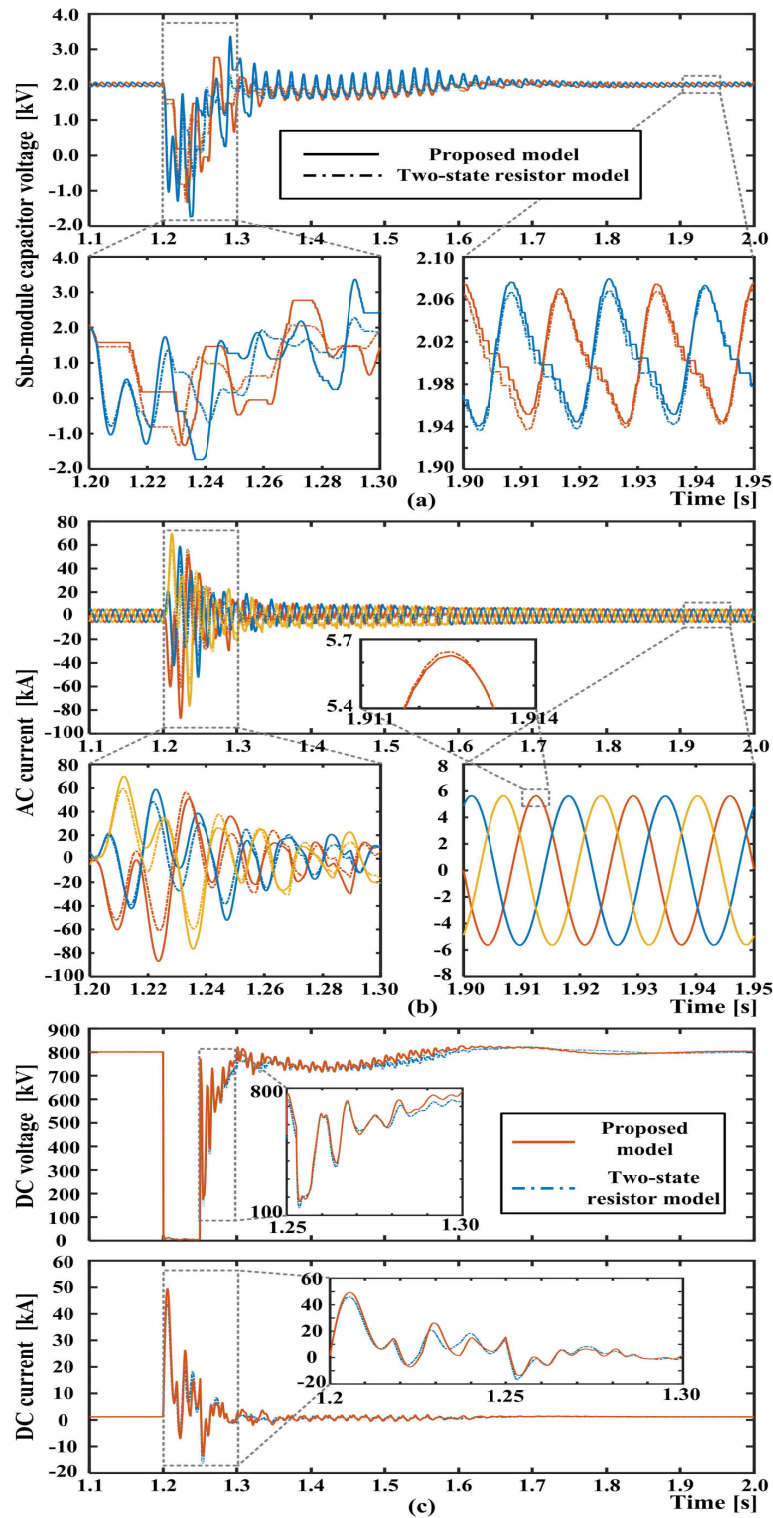
Figure 6.7: Comparative results between the proposed model and the two-state resistor model of MMC at Station Cb-D1: (a) capacitor voltages of the first SM in the upper and lower arms of phase-a, (b) AC current, and (c) DC voltage and DC current.

Table 6.2: Converter Types Utilized for Different Converter Stations

Converter type	Converter station
MMC	Cb-B1, Cb-D1, Cb-B2, Cm-F1
3L-NPC	Cm-A1, Cm-C1
2L	Cb-A1, Cb-C2, Cm-B2, Cm-B3, Cm-E1
4Q DC/DC	Cd-B1
2Q DC/DC	Cd-E1
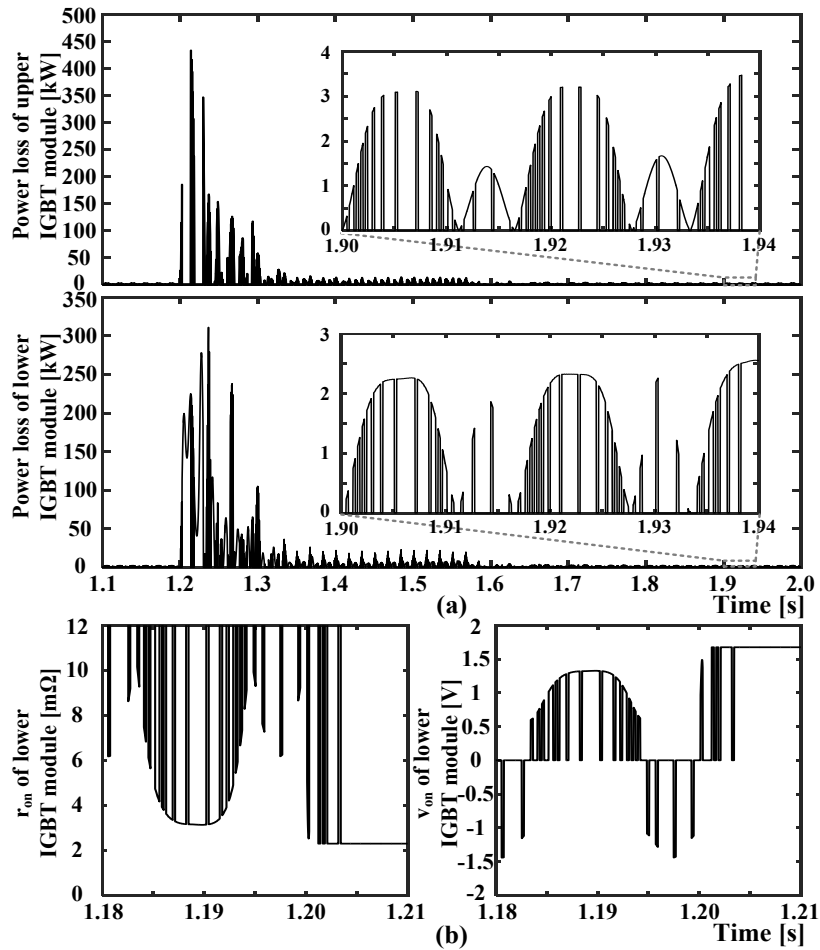
Figure 6.8: Switching device level waveforms in the first sub-module of upper arm of phase-a: (a) power losses of upper and lower IGBT modules (b) r_{on} and v_{on} of lower IGBT module.

6.4.1 Verification of Proposed MMC Modeling Scheme

Fig. 6.7 compares the simulation results between the proposed piecewise polynomial curve fitting scheme and the two-state resistor model for MMC. Pole-to-pole DC fault with the fault resistance of 0.1Ω occurs at the DC bus Bd-D1 from 1.2s lasting for 0.05s, and the

MMC Station Cb-D1 is chosen for observation. Except for the difference of MMC modeling schemes, the remainder converter topologies all use discrete switches. It is observed that the differences of capacitor voltages and AC currents of the two models are significant at the beginning of the fault and then become smaller after few hundreds of milliseconds, as shown in Fig. 6.7 (a) and (b). The differences of DC current and DC voltage are much smaller compared with capacitor voltages. In other words, the steady-state results are very close to each other for the two models, while the transient waveforms can be different. This is due to the difference of IGBT module parameters, including the slope resistance and threshold voltage. The two-state resistor model does not consider the threshold voltage and uses idealized resistances for IGBT modules, which are very large value for turn-off state and very small value for turn-on state. In contrast, the proposed model uses accurate curve fitting for the IGBT and diode characteristics from the manufacturer's datasheet. When the DC fault occurs, the current can be multiples of the steady-state value, which makes the IGBT module characteristics more significant for simulation accuracy. The parameter influence is larger for the waveforms of a single device or sub-module, compared with converter-level or system-level waveforms.

Both models have sufficient accuracy for system-level study and can monitor the submodule capacitor voltage, while the proposed model can provide switching device level waveforms, such as the conduction losses, dynamically changing r_{on} and v_{on} for the IGBT modules as shown in Fig. 6.8. The power losses during the fault transient and steady-state are presented. During the fault, the instantaneous power losses can reach up to around 450 kW, which may damage the devices. Note that the performance of the protection devices, such as breakers, by-pass switches, are not included in the simulation, which can limit the over current and protect the devices effectively. Fig. 6.8 (b) shows the dynamic change of r_{on} and v_{on} according to the gate pulses and the SM current. When the IGBT module is turned off, the resistor value is 1MΩ, which can not fit in Fig. 6.8 (b). When the fault happens, the current is located in Section III of Fig. 6.4 (d), which makes the r_{on} and v_{on} unchanged for the corresponding period.

6.4.2 Comparison of Various Converter Modeling Complexities

In this sub-section, the proposed model (discrete switches applied for 2L and 3L-NPC converter modeling), two-state resistor model (discrete switches applied for 2L and 3L-NPC converter modeling), switching function model, and average value model are used for the converters in CIGRÉ DC grid test system. The test condition is the same as in the previous sub-section, which is the pole-to-pole DC fault at Bus Bb-D1 from 1.2s. The comparison of results of DC voltage and DC current at multiple converter stations are presented in Fig. 6.9, and the following phenomena can be observed.

1. At Station Cb-D1, which is the DC fault location, both the DC voltage and current waveforms using switching function model and average value model have severe
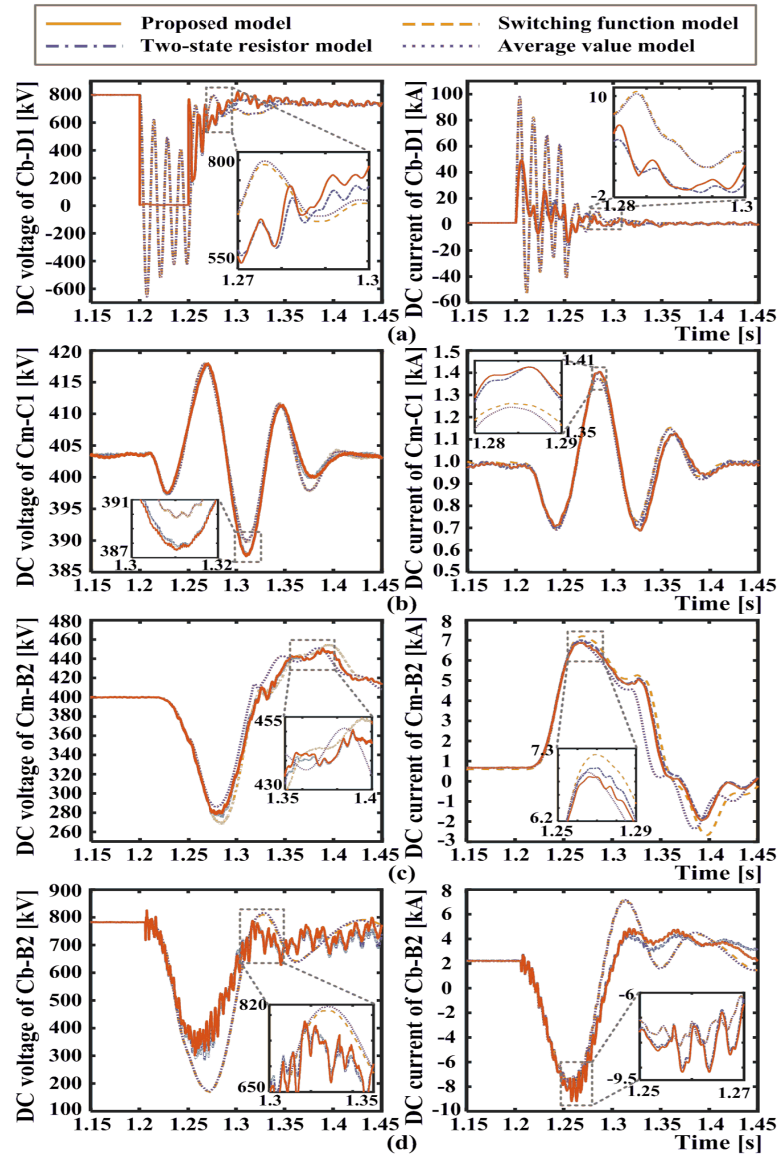
Figure 6.9: Comparative results of using different model complexities: (a) DC voltage and DC current at Station Cb-D1, (b) DC voltage and DC current at Station Cm-C1, (c) DC voltage and DC current at Station Cm-B2, (d) DC voltage and DC current at Station Cb-B2.

numerical oscillations, which leads to the spurious results. After few hundred milliseconds, oscillations subside and the waveforms reach steady-state. This happens mainly because the model interface uses delayed voltage and current information, which can cause the numerical issues when abrupt change occurs. Applying iterations between the AC and DC side may solve the issue; however, this is not supported by PSCAD/EMTDC®, and can consume longer calculation time.

2. At the station far away from the fault location, the switching function model and the

average value model do not have numerical issues. However, the error is relatively large compared with more detailed models.

3. For the MMC modeling, SM capacitor balancing is not considered for the switching function model and the average value model, which can have a significant impact on the transient behavior and lead to a larger error during transients compared with the scenarios for 2L and 3L-NPC converters. Since the voltages of MMC with high levels are almost perfect sinusoidal waveforms, therefore the system-level waveforms of the switching function model and average value model are almost identical. For 2L and 3L-NPC converters, the waveforms can be quite different for the switching function model and average value model, especially at the AC side of the converters.

4. Among the Stations of Cm-C1, Cm-B2, and Cb-B2, Station Cm-B2 has the largest disturbances, which is located in the same DC System 2 of the fault location, while Station Cm-C1 has the smallest disturbance, located in the DC System 1 which has the weakest coupling with DC System 2. This observation is consistent with the network coupling discussion in Section III.

In summary, the switching function model and the average value model can be used in stations far away from the fault location with certain accuracy; however, they are not appropriate for use exactly at the fault location. Table 6.3 presents the execution time for a 5s run using different modeling schemes. The simulation is conducted on the PC using Intel® Xeon CPU E5-2609 at 2.4GHz, 32 GB RAM, and Window 7 operating system. The additional execution time of the proposed method is small (while providing greater details) compared with the one using two-state resistor model, and the execution times of switching function model and average value model are close to each other and are much smaller compared with the Thévenin equivalence based methods.

Table 6.3: Execution Time Comparison of CIGRÉ DC Grid Test System

Model	Execution time (for a 5s run)
Proposed model	501s
Two-state resistor model	423s
Switching function model	119s
Average value model	107s

6.4.3 Case Study of Hybrid Modeling Scheme

In this section, the complete AC/DC grid is used for the case study including the wind farms and IEEE 39-bus AC system. The DC fault lasting 0.05s from 5s of the simulation
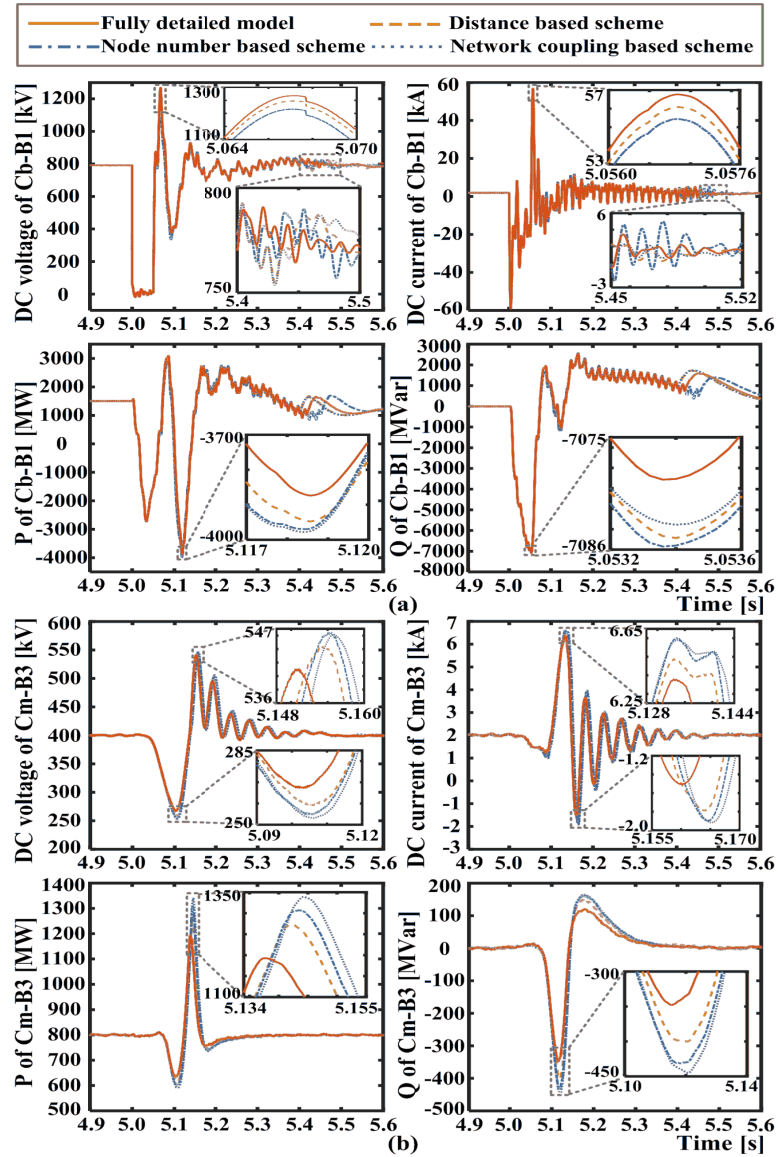
Figure 6.10: Comparative results of converter stations using different partition schemes: (a) DC voltage, DC current, AC-side active power, and reactive power at Station Cb-B1, (b) DC voltage, DC current, AC-side active power, and reactive power at Station Cm-B3

occurs at the DC Bus Bb-B1, which is close to the center of the test system. In the case study, the fault location and the converter stations around it are assumed as the study zone. Three zone partition schemes are applied based on distance, node number, and network coupling to divide the complete system into the detailed zone, accurate zone, and averaged zone. The modeling schemes for different zones are shown in the upper part of Table 6.4. Since the switching function model and the average value model have almost identical accuracy for MMC modeling, the two-state resistor model is applied for the accurate zone to differentiate it from the averaged zone.

For distance based scheme, the detailed zone contains the converters within 300km,
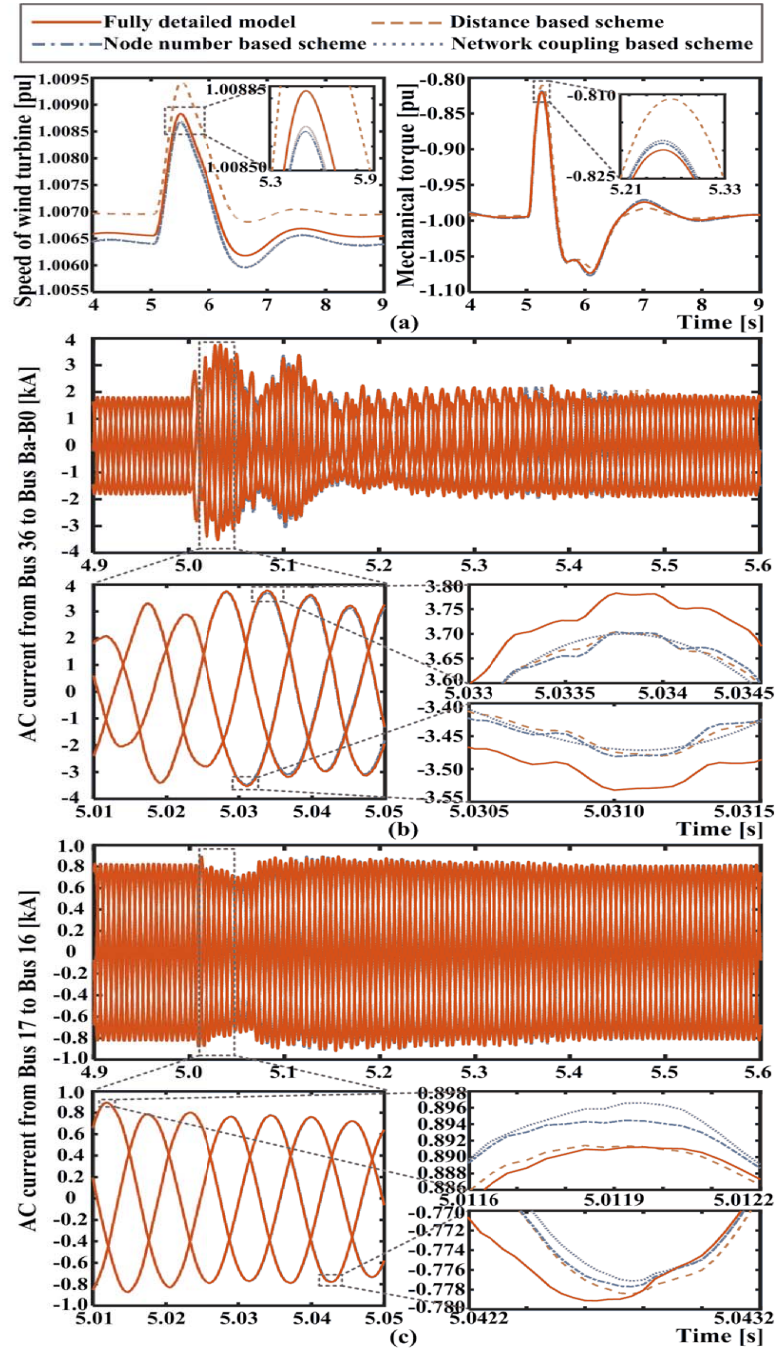
Figure 6.11: Comparative results of wind farms and AC systems using different partition schemes: (a) shaft speed and mechanical torque of the wind turbine connecting to Station Cb-D1, (b) AC current form Bus 36 to Bus Ba-B0, and (c) AC current form Bus 17 to Bus 16

while the accurate zone contains the ones within 500km. For node number based partitioning scheme, the detailed zone contains the converters with the node number of 1 or 0 to the node of fault location, the accurate zone contains the converters that have the node number of 2 to the node of fault location. For the network coupling based scheme, the

detailed zone only contains the Station Cb-B1, while all the Stations in DC system 3 are in accurate zone. The rest converters in corresponding schemes are located in averaged zone. The lower part of Table 6.4 presents the allocations of converter stations in the three zones for different partition schemes.

Fig. 6.10 and Fig. 6.11 present comparative results of converter stations, wind farm and AC system using different zone partition schemes as well as the case using all detailed models. By using the hybrid modeling scheme, the simulation accuracy is maintained for the transient analysis, though a certain amount of error exists. For Station Cb-B1, since all the schemes use the detailed model, the results using different partition schemes are quite consistent with each other, especially at the beginning of the transients. However, the waveforms notably differ from each other after around 400 milliseconds of the fault. This is because the converters using simplified modeling schemes are generally far from the fault location. The traveling wave latency of transmission lines delays the waveform discrepancy. When the steady-steady is reached, the waveforms are become consistent eventually. The errors for different schemes are relatively large at Station Cb-B1 at the beginning of the transients due to the modeling difference at the Station Cb-B1 and other nearby stations. Although the partitioning is based on different criteria, the zones overlap with each other to some extent. The similarity of AC/DC grid modeling between the fully detailed model case and other cases using hybrid modeling is not as much as the similarity among the different partition schemes, which is presented in Table 6.4. It explains the phenomenon that the waveforms of detailed model is slightly different from the waveforms of the cases using hybrid modeling, while the waveforms between different partition schemes are close to each other, which can be observed, especially in Fig. 6.10 (b) and Fig. 6.11 (b). In Fig. 6.11 (a), the shaft speed and the mechanical torque of the case using node number based scheme have notable error compared with other cases. Because the MMC Station Cb-D1 uses average value model for node number case, while other cases use at least the two-state resistor model. The control dynamics can affect simulation accuracy, which is neglected in the case using node number based scheme. In the on-shore AC system, it is clearly observed that the disturbance is much smaller for the location far away from the fault location.

If another location different from the fault location is desired, the partition schemes can be applied independently, which is equivalent to applying the superposition theorem. The modeling method of a certain station adopts the most detailed one, if the two partition results are not consistent.

The execution time of a 5s run is listed in Table 6.4. Using hybrid modeling schemes can reduce around 40% of the execution time compared with the case using fully detailed model. The speed-up can be more significant for a larger system, where the averaged zone can cover more converters. Although the case using distance based scheme consumes longer computation time, the case using node number based scheme obtains higher accu-

racy except for the waveform at the wind turbine connecting to Station Cb-D1 in Fig. 6.10 and Fig. 6.11. However, it is difficult to generally evaluate the performance of the three partition schemes, since it is affected by the circuit topology and simulation purpose.

Table 6.4: Modeling Scheme, Converter Station Allocation, and Execution Time for the AC/DC Grid Case Study

Converter/Partition scheme	Modeling method/Converter station allocation			Execution time (for a 5s run)
	Detailed zone	Accurate zone	Averaged zone	
MMC	Proposed model	Two-state resistor model	Average value model	NA
2L & 3L-NPC	Discrete switches	Switching function model	Average value model	NA
Full detailed model	All Stations	None	None	738s
Distance based scheme	Cb-B1,Cm-E1,Cm-B3	Cm-F1,Cm-A1,Cb-B2, Cm-B2,Cb-D1,Cb-A1	Cm-C1,Cb-C2	499s
Node number based scheme	Cb-B1,Cb-A1	Cb-B2, Cm-B3, Cb-C2, Cm-A1	Cm-B2,Cm-F1,Cm-E1, Cb-D1,Cm-C1	445s
Network coupling based scheme	Cb-B1	Cb-A1,Cb-C2, Cb-D1,Cb-B2	Cm-b2,Cm-B3,Cm-F1, Cm-E1, Cm-A1, Cm-C1	432s

6.5 Summary

This chapter proposed the piecewise polynomial curve fitting scheme for MMC modeling, and presented the simulation results of a complete AC/DC grid using fully detailed model and hybrid modeling schemes. The hybrid modeling scheme can effectively balance the accuracy and the simulation speed. Although this work used PSCAD/EMTDC® as the implementation platform, the proposed model and the simulation of the AC/DC grid can be accomplished in other EMT tools, such as EMTP-RV®. The purpose of this work is to provide comprehensive electromagnetic modeling schemes and guidelines to develop the complex AC/DC grid system. Insights and accelerate gained through such simulation can greatly enhance the control and protection studies of the AC/DC grid system.

7

Real-Time Emulation of CIGRÉ DC Grid on MPSoC-FPGA Platform

7.1 Introduction

In this chapter, a hybrid MPSoC-FPGA platform using Xilinx® Zynq Ultrascale+ XCZU9EG and Virtex Ultrascale+ XCVU9P devices is established for the realization of CIGRÉ DC grid real-time emulator. For the purpose of providing both the accurate and detailed results of the components in the local study zone, and the global interactive results of other components in the DC grid with relatively low hardware resource and design cost, a feasible hybrid modeling scheme is utilized for representing various MMCs in the DC grid. Device-level electrothermal model, equivalent circuit model, and the average value model are used for representing different components and zones in the emulated system [12, 20, 23, 48, 100]. The complete system is fully decomposed to 20 sub-systems to achieve high parallelism and modularity.

The contribution of this chapter is the development and detailed presentation of the algorithm decomposition, hardware design partitioning and implementation methodologies for the CIGRÉ DC grid emulator. It is the first time that the emulator of such complex DC grid which includes the device-level models are developed and operated in real-time whether on the conventional simulator or the proposed hybrid digital hardware platform. The system-level and the device-level emulation results captured in real-time on the oscilloscope are compared with commercial EMT tools PSCAD/EMTDC® and SaberRD®, respectively. The developed emulation system can significantly enhance the accuracy and efficiency of HIL test for the control and protection schemes in the DC grid.

This chapter briefly presents the topology and control scheme of the CIGRÉ DC grid test system and the hybrid modeling scheme of the MMCs and other devices particularly
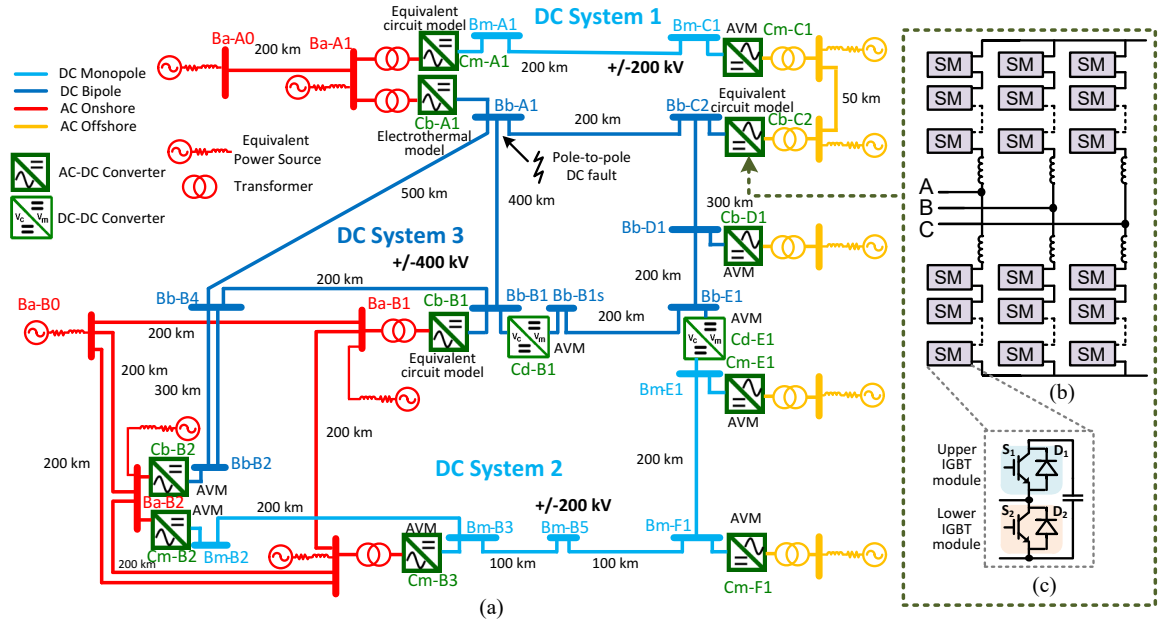
Figure 7.1: Topology of the: (a) CIGRÉ DC grid test system, (b) modular multi-level converter, and (c) half-bridge sub-module.

applied in this work. The detailed partitioning and design implementation methodologies of the emulation system are described. The captured real-time system-level and device-level results during normal operation, power flow control, and DC fault conditions with the validation are presented.

7.2 CIGRÉ DC Grid Network Topology, Control Scheme, and Hybrid Modeling Methodology

7.2.1 Network Topology

The CIGRÉ DC grid test system emulated in this chapter is shown in Fig. 7.1 (a), with the parameters from [2]. The DC System 3 uses the meshed topology with the DC-DC converter Cd-B1 to provide an extra degree of freedom for controlling the loop power flow. DC System 1 and DC System 3 are connected through AC system, while DC System 2 and DC System 3 are connected directly by the DC-DC converter Cd-E1. The circuit topology of MMC, which is used for all the AC-DC converters, is shown in Fig. 7.1 (b). The MMC contains 6 arms, and each arm is composed of the series connected sub-modules and arm inductor L_m. Half-bridge SM topology is utilized for all the MMCs containing the upper IGBT module (IGBT S_1 and Diode D_1), the lower IGBT module (IGBT S_2 and Diode D_2), and the SM capacitor as shown in Fig. 7.1 (c).
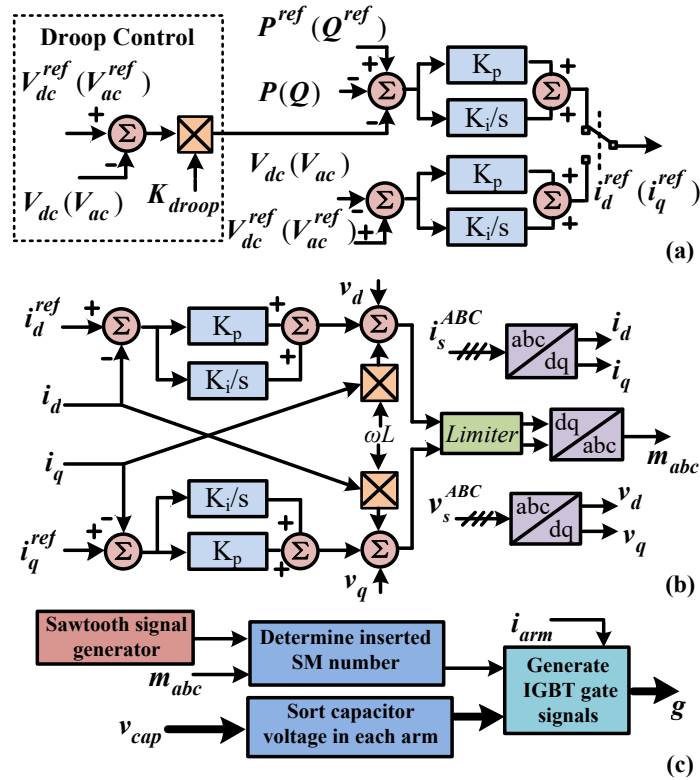
Figure 7.2: Control diagram of MMC: (a) outer loop control for power and DC voltage, (b) inner current loop control (c) MMC valve-level control.

7.2.2 Control Scheme

The control diagram of the MMC is shown in Fig. 7.2, which is composed of the outer loop control, inner current loop control, and valve-level control. The controlled variables are determined by the converter function and the type of the AC system. In this chapter, Converters Cm-A1, Cb-A1, Cm-B2 connecting to the relatively strong on-shore AC system are utilized for DC voltage regulation, while the other AC-DC converters primarily control the active power flow. The reactive power flow can be regulated independently for all converters. Capacitor-sorting based control scheme is used for the valve-level control of MMC [5, 21]. It is noted that the computation effort of valve-level control is dependent on the SM number in an arm, and can be significantly larger than the system-level control including the outer and inner loop controls.

7.2.3 Hybrid Modeling Methodology of MMC

The major challenge and the focus of this chapter are the modeling and implementation of all the converters in the DC grid for real-time EMT simulation with limited hardware resources. Although the FPGA board can provide high parallelism, the realization of all converters using detailed models can consume a huge amount of resources, which ex-

ceeds the capacity of a single board. Hybrid modeling strategy is applied to reduce the resource consumption and maintain the accuracy of the study zone and the size of the complete system. Among various modeling methods, device-level electrothermal model, equivalent circuit model, and average value model, which cover a wide range of modeling complexity, are adopted for various locations in the DC grid [12, 20, 23, 48, 100]. The detailed modeling scheme is used at the local element or zone which is of most interest and can be the closest converter to the fault location for transient analysis; the equivalent circuit modeling scheme is applied for the converters surrounding the local element; the average value model is used for the converters in remote locations. In Fig. 7.1, the modeling schemes adopted for various converters are annotated. Such strategy is also applicable for other elements, such as the transmission lines, etc.

7.2.3.1 Device-Level Electrothermal Model

Device-level electrothermal model is the most complex method adopted in this chapter, which can provide the power losses, the junction temperatures and device-level switching transients of any single IGBT or diode. The parameters of the electrical model interface obtained from manufacture's datasheet [91] are dependent on the values of the junction temperature, which matches the actual physical phenomena of power electronic devices. Using such a modeling scheme in the real-time simulation can provide the comprehensive on-line evaluation of the power converter for efficiency and security under normal condition and fault transients with direct thermal indicators.

The major processes of the electrothermal model are illustrated in Fig. 7.3. During each system-level time-step, the system-level results, such as current waveforms and switching signals, from the electromagnetic transient simulation are used to calculate the conduction and switching power losses. Then the power losses of individual switches are imported as equivalent current sources into a thermal network, which is composed of multiple series-connected thermal impedance of various devices in the same heatsink. The calculated junction temperatures are used to update the electrical parameters of the interface, which is used for the next time-step calculation. The device-level calculation requires the temperature-dependent parameters, such as the rise-time and fall-time of the voltage and current waveforms, and the system-level results. When implemented on hardware, the device-level waveform generation module can update at each FPGA clock frequency, which is 100MHz in this work.

7.2.3.2 Equivalent Circuit Model

Since an MMC with high level number contains many SMs, which can generate a large number of system matrix nodes, the conventional EMT simulation can be extremely time-consuming and is not able to execute in real-time. Equivalent or surrogate circuit is commonly used for the simplification of a sub-module model shown in Fig. 7.4 (b). The sim-
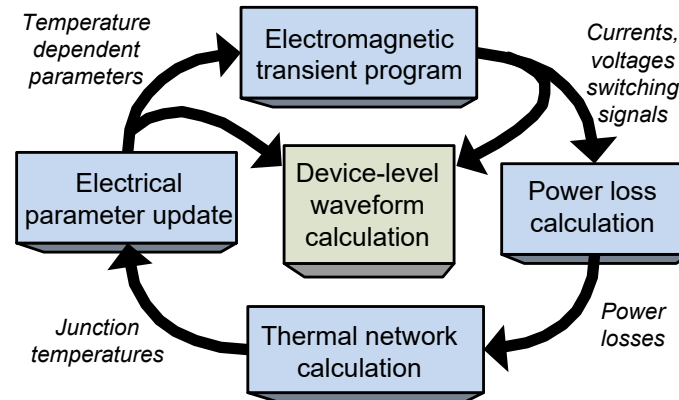
Figure 7.3: Major procedures of device-level electrothermal model.

plified SM model shown in Fig. 7.4 (c) can be further summed generating the interface of a converter arm, which decreases the electrical nodes substantially. The equivalent circuit modeling scheme accurately calculates the SM capacitor voltages and verify the fundamental function of the complete control algorithm. The equivalent circuit model is also applied to combine the device-level electrothermal model of IGBT modules to the interface of MMC model ensuring the real-time performance. Taking the example of upper IGBT module, the resistor r_1 and voltage source v_1 are calculated using piecewise polynomial functions based on the temperature dependent characteristics of IGBT module shown in Fig. 7.4 (a) and the operating conditions determined by the gate signal and the arm current direction. For conventional equivalent circuit modeling scheme, r_1 and v_1 only have two fixed values to represent the on-state and off-state, respectively.

7.2.3.3 Average Value Model (AVM)

The average value model is the simplest modeling scheme for an MMC converter applied in this work. The voltage waveform with fundamental frequency is generated at the AC side of a converter, and the DC side current is generated conserving the transferred power. The valve-level control cannot be verified with this model, since all the SM capacitor voltages are assumed to be balanced at all time. The average value model uses the controlled voltage and current sources with one time-step latency, which provides the matrix separation capability between the AC and DC side. Such a feature is beneficial for the system decomposition of reducing the matrix size, while may also bring numerical consequences during faults.

7.2.3.4 Transmission Line Model

A hybrid modeling methodology is also applied to the transmission line model by using both universal line model (ULM) and Bergeron line model (BLM) [11, 102]. The ULM fully considers the frequency-dependent characteristics of the transmission lines, while the
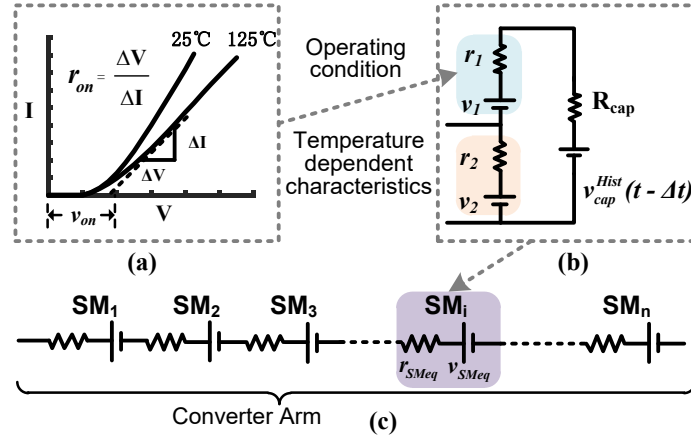
Figure 7.4: (a) Temperature-dependent IGBT module output characteristics (b) circuit model of half-bridge SM, and (c) simplified SM model.

time-domain convolution required for such model consumes relatively larger computation and memory resources. On the other hand, BLM is simpler and less accurate considering only the fundamental frequency. ULM is applied to the lines in the study zone connecting the interested local elements, while BLM is used for short lines or remote locations in AC system. The PI section model is avoided in this work due to its inaccuracy and the absence of latency feature for decomposing the DC grid.

In this work, the Converter Cb-A1 is chosen as the component of interest; and the detailed electrothermal model is applied to all the IGBT modules of this converter. The nearby three Converters Cb-B1, Cb-C2, and Cm-A1 utilize the equivalent circuit model. The modeling schemes used for various converters in this work are presented in Table 7.1 . Each of the above four converters has 65 levels or 384 modules. Multiple IGBT modules are connected in parallel and in series, which are 10 and 7 in this work respectively, to provide sufficient voltage and current rating for the converter. The transmission lines connecting between these converters utilize the ULM. The rest of the converters and transmission lines use AVM and BLM, respectively. A uniform modeling scheme is used for the power sources and transformers in the grid. In future work, hybrid modeling schemes could also be used for these elements, such as connecting a detailed wind power plant on the off-shore side.

Table 7.1: Modeling Scheme for Converter Stations

Modeling scheme	Converter station
Electrothermal model	Cb-A1
Equivalent circuit model	Cb-B1, Cb-C2, Cm-A1
Average value model	Cb-D1, Cb-B2, Cm-B2, Cm-B3, Cm-C1, Cm-E1, Cm-F1, Cd-B1, Cd-E1

7.3 Design and Implementation of Real-Time MPSoC-FPGA Based DC Grid Emulator

7.3.1 System Decomposition Method

Besides the rapid development of IC technology, the feasibility of conducting real-time electromagnetic transient simulation for large-scale power systems relies on the appropriate decomposition or relaxation of the system, which is to divide the complete system to multiple smaller sub-systems. Therefore, the large system matrix is decomposed into multiple sub-matrices, which can be calculated in parallel. The delay property is required for the decomposition scheme which was realized by following means applied in this work:

1. using distributed line models, such as ULM and BLM, for the widely existing transmission lines in the DC grid;

2. using the delay property of the average value model of the converters.

When using disturbed line models, the line length must be sufficiently long, which makes the traveling time at least longer than the system simulation time-step, which is 20μs in this work. The traveling time of some specific transmission lines shall also be longer than the communication latencies between various hardware computing units. Such requirements can be generally met for a transmission network, while may be an issue for a smaller system, such as a microgrid. It can be solved by inserting short distributed line models for decomposition. As previously explained, average value model of MMC can also provide the system decomposition with the sacrifice of accuracy and numerical stability.

During the periodical calculation for each time-step, the EMT simulation includes three major steps, which are the electrical and control element calculation, the data exchange between sub-systems, and the matrix equation formation and solution as shown in Fig. 7.5 (a). Except for the exchange of history values of transmission line models and the voltage and current values of MMC average value model, the calculations among the sub-systems are independent and can be parallelized.

7.3.2 Hardware Resource Allocation and Task Partitioning

The multi-core CPU is often used for the real-time EMT simulation. Admittedly, the communication latencies among the CPU cores are small, but frequent and large-amount of data exchange between cores is a heavy burden and is seldom recommended. For such reason, the complete calculation of a sub-system often resides in a single thread or core illustrated in Fig. 7.5 (a). Since a CPU core is a sequential calculation device, the compute capability is limiting the number of sub-systems which can be contained in a single core.
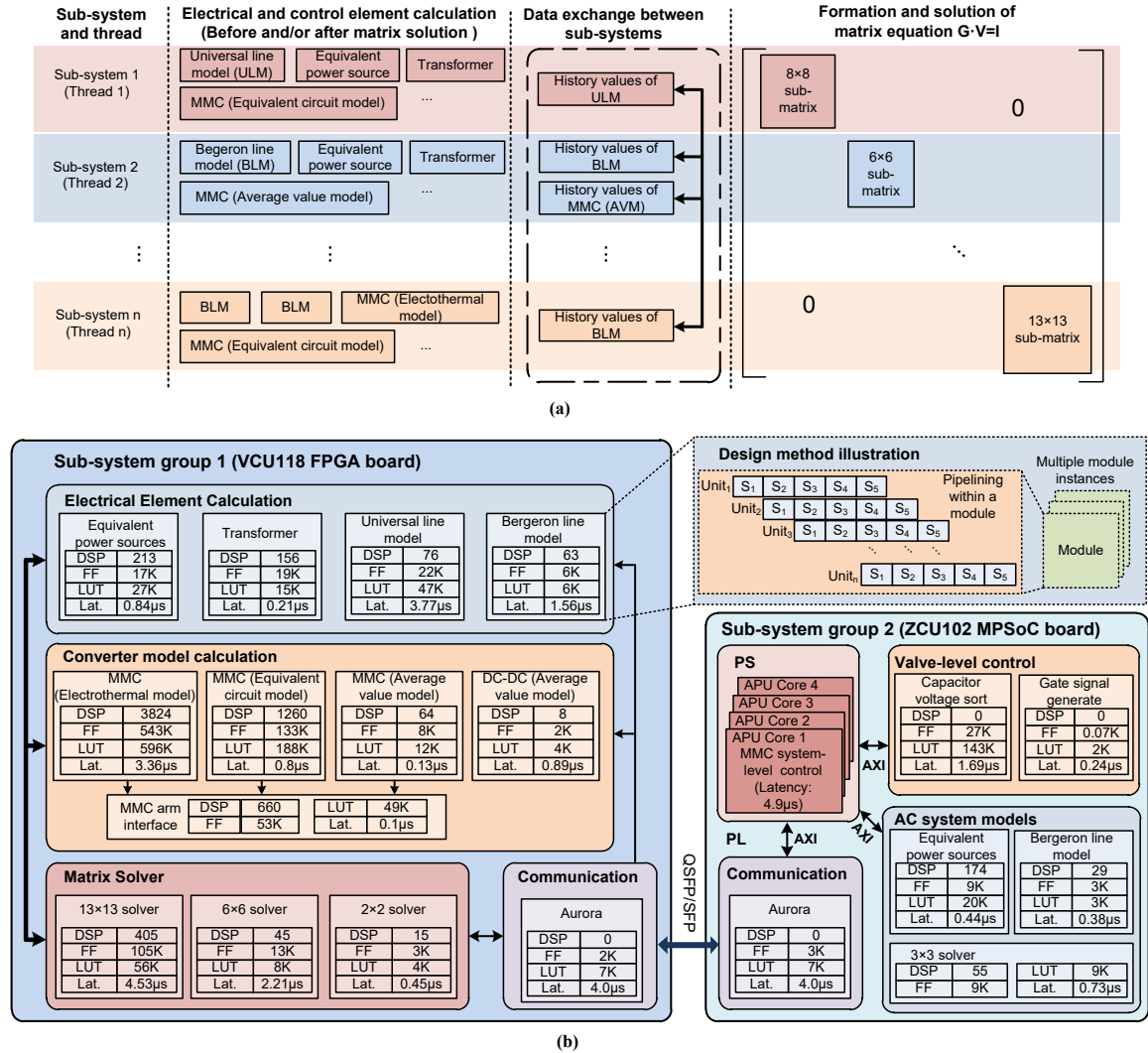
Figure 7.5: (a) System decomposition and conventional processor-based partition scheme, (b) MPSoC-FPGA based partition and implementation details.

When complex topologies and components exist, it is necessary to use multiple cores increasing the parallelism to some extent for the calculation of the sub-system ensuring the real-time performance, which in effect increases the inter-core communication burden.

The utilization of FPGA resources can effectively eliminate the above dilemma, since various modules are connected directly by appropriate routing design without the complex mechanism for generalized communication. In effect, the module-level connections have no fundamental differences from the internal connections for various logic resources within an FPGA module. Instead of partitioning the system by sub-systems used in the conventional CPU-based simulator, this work partitions the system by different functions. The internal design of the modules uses pipelined structures to optimize the resource utilization. One or multiple module instances are applied to different components based on the timing requirements. Such processes are automatically done by HLS tools with the

input of C code and directives enforcing specific resource and latency requirements. Generally, resource and latency optimization cannot be achieved simultaneously, which may require multiple design iterations to achieve the balance for a specific design.

The resources on one FPGA or MPSoC board may not be sufficient for the emulator of a large and detailed system. Multiple boards can be interconnected providing enormous computation capability. The board-level partition scheme is similar to the sub-system based partition, due to the relatively high communication cost. A sub-system group containing a large number of sub-systems is assigned to a board. In order to present the versatility of the proposed CIGRÉ DC grid emulator, which can conduct control device HIL test, power equipment HIL test and the multi-board expansion, the MMC control of all 11 converters and the calculation of two AC buses Ba-A0 and Ba-B0 alone with the corresponding equivalent power source and solver modules reside in the MPSoC board.

7.3.3 Design and Implementation

Fig. 7.5 (b) shows the hardware implementation of the CIGRÉ DC grid emulator on MPSoC-FPGA platform. The resource consumption and the latency of major components or functions are also presented. When the emulator starts, the initialized coefficients and variables are loaded to all the modules. Then all the modules of the electrical element calculation and converter model calculation begin simultaneously. When all the values of the matrix equations are updated, the solver modules run simultaneously. The communication modules exchange the data between the FPGA board and the MPSoC board through Aurora IP core, which handles the data conversion for serial transceivers. The transferred data includes the emulation control signals, MMC control input and output data, transmission line data, and chosen emulation results for observation. The MPSoC board follows the control signals from the FPGA board for synchronization and accomplishes the tasks of MMC control and the calculation of two AC buses. When the exact time of the next time-step reaches, the periodical calculation starts again.

There are 20 sub-matrices existing in the DC grid emulator with sizes varying from 2×2 to 13×13. Four types of solvers are implemented calculating different size range to achieve the optimized resource and latency performance as shown in Fig. 7.5 (b). For example, a 9×9 matrix equation can be solved by a 13×13 solver; while the matrix equation with smaller size such as 6×6 can use another smaller matrix solver.

The implementation of the MMC controller takes the advantages of MPSoC devices. The relatively complex and sequential calculations of the system-level control of the 11 MMC converters are completed in the four APU cores. The system-level control schemes and parameters can also be conveniently modified in the APU cores for HIL test. The valve-level control required by Converters Cb-A1, Cb-B1, Cb-C2, and Cm-A1, includes the sorting of all the SM capacitors in an arm and the gate signal generation of all IGBT modules, which is computationally demanding assigned on PL for acceleration.
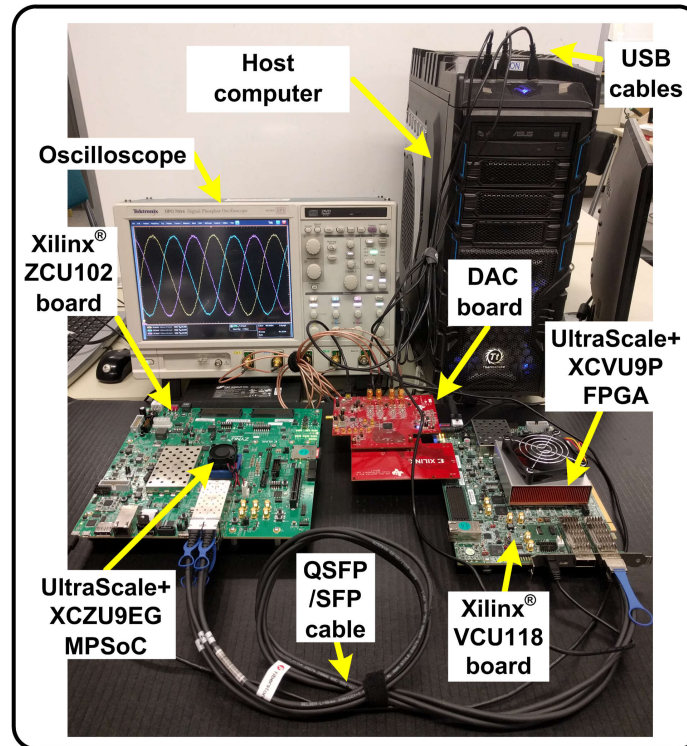
Figure 7.6: Hybrid platform configuration of the DC grid emulator.

There are various design flexibilities regarding the latency and resource consumption, when using the same devices or other devices, such as Xilinx® XCVU13P, which has 46% more logic blocks and 80% more DSP slices compared with Xilinx® XCVU9P used in this work. In this work, the calculation modules for converters on the FPGA board wait for the MMC control signals from the MPSoC board within the same time-step. Sometimes there could be a delay for the MMC control signals, and the converter calculation modules can use the control signals of the previous time-step. In this way, the simulation time-step can be further reduced. In terms of resource consumption, the number of SMs using electrothermal model within an MMC model, the number of MMC converters using electrothermal model or equivalent circuit model, and the MMC level numbers can be adjusted based on the available resources and emulation requirements.

7.3.4 MPSoC-FPGA Hybrid Hardware Configuration

Fig. 7.6 shows the hybrid platform configuration of the emulator. The VCU118 FPGA board is connected to the ZCU102 board through QSFP to 4×SFP cable. The programmable logics of both boards are running at 100MHz. The USB-JTAG cables of the two boards are connected to the host computer for downloading the configuration files. A digital-analog converter board is used to connect the FPGA mezzanine card of the VCU118 board and the oscilloscope to capture the real-time results from the emulator.
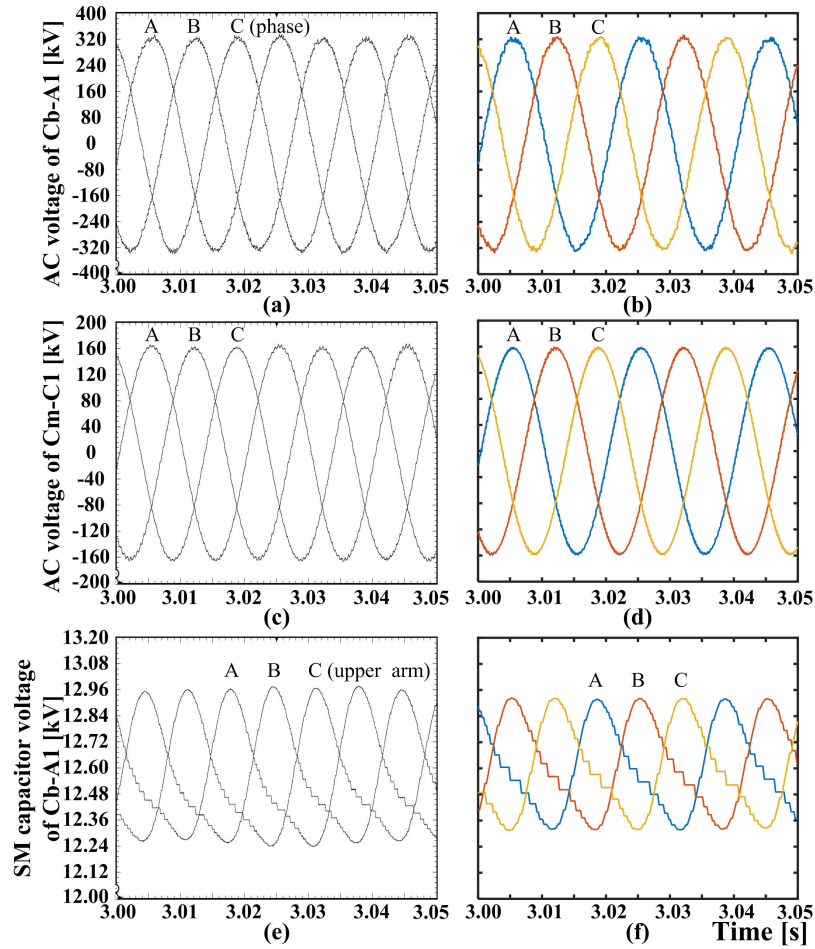
Figure 7.7: System-level steady-state results: (a) (b) AC voltages of Converter Cb-A1, (c) (d) AC voltages of Converter Cm-C1, and (e) (f) the first upper arm SM capacitor voltages of Converter Cb-A1. ((a) (c) (e) are the real-time results; (b) (d) (f) are the offline PSCAD/EMTDC® results.)

7.4 Real-Time Emulation Results, Validation, and Discussion

Various studies and tests along with substantial results can be accomplished with the proposed real-time CIGRÉ DC grid emulator. The emulator uses $20\mu s$ as the time-step for the system-level calculation and $10ns$ as the time-step for the device-level transient waveform update. This section presents some of the system-level and device-level real-time results under both normal operation and DC fault transient validated with commercial software PSCAD/EMTDC® and SaberRD® respectively. The complete CIGRÉ DC grid is modeled in PSCAD/EMTDC® with the same hybrid modeling scheme as the real-time emulator, except that the electrothermal model is not used. However, the complete DC grid could not be implemented in SaberRD® due to the numerical stability and convergence issue for the complex DC grid system, and the external system-level waveforms are imported to the precisely modeled sub-module for device-level results verification.
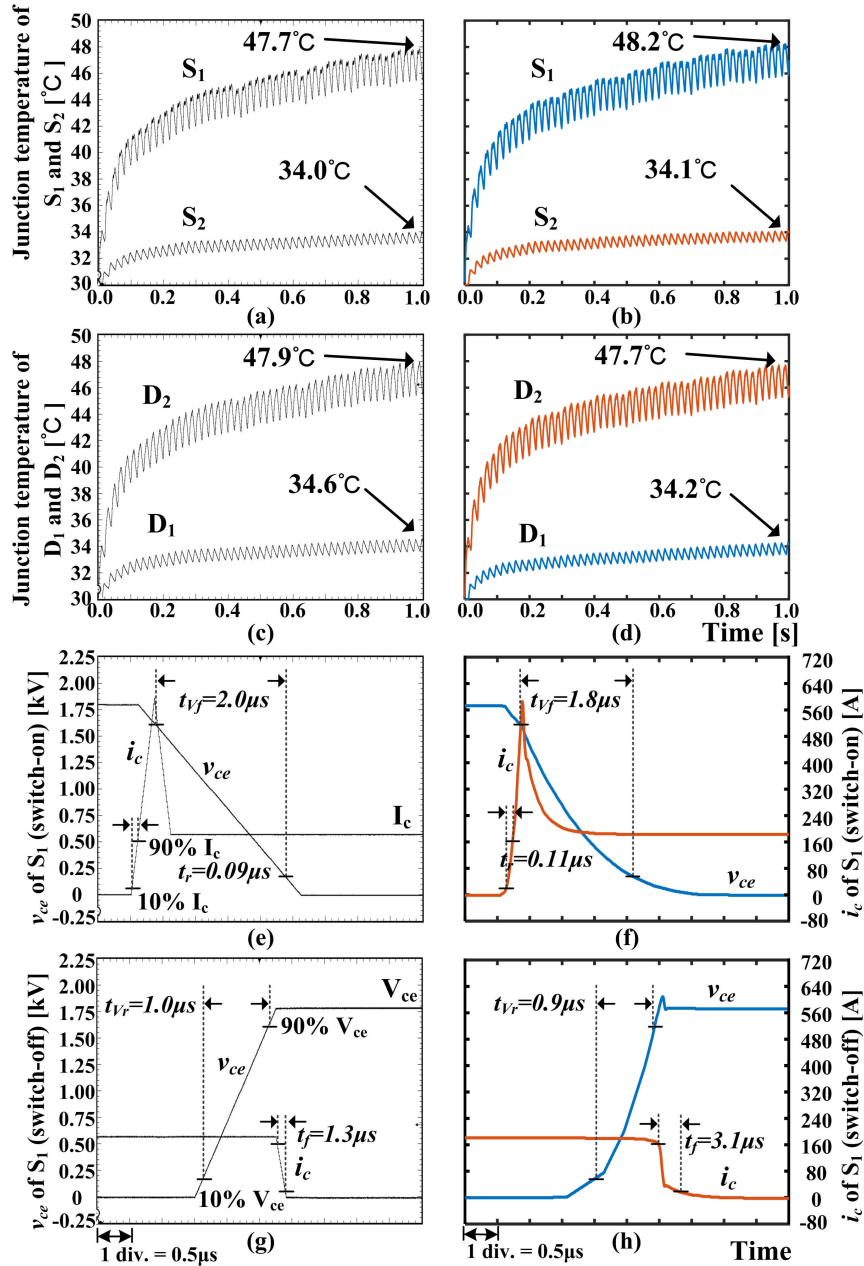
Figure 7.8: Device-level steady-state results of the first SM in Converter Cb-A1 upper arm Phase A: (a) (b) junction temperatures of IGBTs S_1 and S_2, (c) (d) junction temperatures of Diodes D_1 and D_2, (e) (f) voltage v_{ce} and current i_c of S_1 during switching-on transient, (g) (h) voltage v_{ce} and current i_c of S_1 during switching-off transient, ((a) (c) (e) (g) are the real-time results; (b) (d) (f) (h) are the offline SaberRD$^{®}$ results.)

7.4.1 Steady-State Operation Results

Fig. 7.7 shows the system-level steady-state operation results including the AC voltages of Converters Cb-A1 and Cm-C1, and the SM capacitor voltages of the first upper arm SM of Converter Cb-A1, which are compared with PSCAD/EMTDC$^{®}$. Since the MMCs
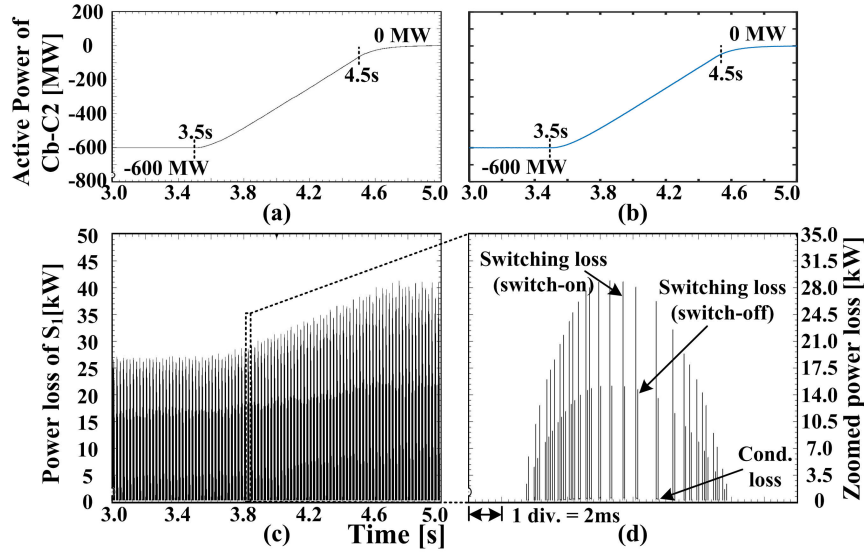
Figure 7.9: Results during power flow command change: (a) (b) active power of Converter Cb-C2, (c) power loss of IGBT S_1 from the first SM in Converter Cb-A1 upper arm Phase A, and (d) zoomed power loss. ((a) (c) (d) are the real-time results; (b) is the offline PSCAD/EMTDC® result.)

modeled in this work have 65 levels, the AC voltage of the Converter Cb-A1 is close to sinusoidal waveforms with few harmonics. Such harmonics can also be observed for Converter Cm-C1 modeled with average value model since the other converter Cm-A1 uses the equivalent circuit model and can affect the waveforms of Converter Cm-C1, which are in the same DC system. The SM capacitor voltages of the real-time results and the PSCAD/EMTDC® results have some differences, due to the different modeling schemes. The IGBT model used in PSCAD/EMTDC® simulation is the two-state resistor model with a small resistance representing on-state and a large resistance representing the off-state. While the electrothermal model used for Converter Cb-A1 is based on the detailed and accurate temperature-dependent nonlinear output characteristics of the IGBT module obtained from the manufacturer's datasheet for FZ400R33KL2C_B5 IGBT module [91].

The device-level results of IGBTs and diodes are presented in Fig. 7.8 with the steady-state initial condition. SaberRD® is utilized for the verification, which uses dynamic thermal IGBT transistor model and dynamic thermal power diode model. The final values and dynamical changing patterns of the junction temperatures for S_1, S_2, D_1, and D_2 are consistent between the real-time results and SaberRD® results shown in Fig. 7.8 (a)-(d). The linearized voltage and current waveforms can give a good estimation for the switching transients with small amount of additional computation effort shown in Fig. 7.8 (e)-(h).
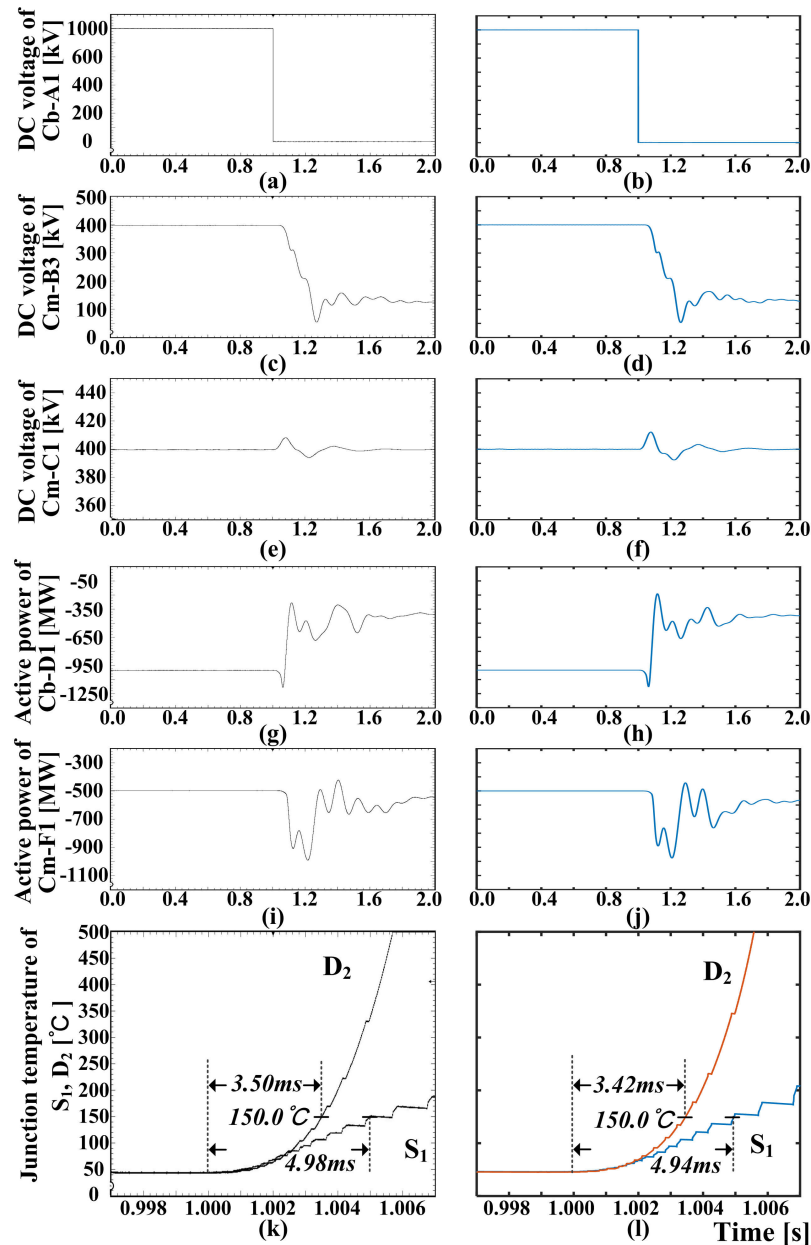
Figure 7.10: Results during DC fault: (a) (b) DC voltage of Converter CB-A1, (c) (d) DC voltage of Converter Cm-B3, (e) (f) DC voltage of Converter Cm-C1, (g) (h) active power of Converter Cb-D1, (i) (j) active power of Converter Cm-F1, and (k) (l) junction temperatures of S_1 and D_2. ((a) (c) (e) (g) (i) (k) are the real-time results; (b) (d) (f) (h) (j) are the offline PSCAD/EMTDC® results; (l) is the offline SaberRD® result.)

7.4.2   Results during Power Flow Command Change

Fig. 7.9 shows the results during power flow command change. The power generation from Converter Cb-C2 changes from 600MW to 0MW from 3.5s to 4.5s of the simulation run representing the scenario of cutting-off an off-shore power plant. Fig. 7.9 (a)-(b) shows

the active power tracking performance of Converter Cb-C2. Since Converter Cb-A1 is responsible for DC voltage regulation, the power flow increases responding to the power flow change of Converter Cb-C2, which influences the corresponding power losses of the IGBT as shown in Fig. 7.9 (c)-(d).

7.4.3   Results during DC Fault

A DC ground fault of both poles is applied to the Bus Bb-A1 at 1.0s of the simulation run with the steady-state initial condition. The DC voltages of Converter Cb-A1, Cm-B3, and Cm-C1 are shown in Fig. 7.10 (a)-(f), which are located in DC System 3, DC System 2, and DC System 1. The real-time results are accurate compared with PSCAD/EMTDC®. Although Converter Cm-B3 is far away from the fault location, the DC voltage is seriously affected by the fault. It is because the DC System 3 and DC System 2 are directly connected by the DC-DC converter without galvanic isolation. On the other hand, the fault effect is small for DC System 1 due to the galvanic isolation and the support from the relatively strong AC system. Fig. 7.10 (g)-(j) presents active powers of Converters Cb-D1 and Cm-F1 during the DC fault. Fig. 7.10 (k)-(l) shows the junction temperatures of S_1 and D_2, where the fault current flows through. The characteristics and parameters of high temperatures and high currents are estimated from the normal operation data from the datasheet and the IGBT and diode parameter fitting tools provided by SaberRD®. It is observed that the temperatures increase significantly within few milliseconds. The times for the devices reaching $150°C$ since the begin of the fault are measured and compared with SaberRD®. When temperatures exceed $150°C$, the devices are no longer safe for operation. It is noted that such results may not be accurate with extreme high temperatures, where the devices could be damaged and the characteristics are fundamentally changed in practical situation. The electrothermal model can still give a rough estimation of the junction temperatures during the faults to evaluate the potential damage to the devices and to verifies the control and protection algorithms for the devices.

7.5   Summary

This chapter presented the design and implementation of a hybrid real-time DC grid emulator on MPSoC-FPGA platform. Hybrid modeling scheme and detailed hardware implementation of the real-time EMT emulation system of the complete CIGRÉ DC grid test system are presented, which are flexible and extensible respectively. PSCAD/EMTDC® and SaberRD® were used to validate the results of system-level and device-level hardware emulation results. The improvement of the modeling schemes and implementation techniques can enlarge the functionality and the scope of the EMT study and provide comprehensive analyses of the AC/DC grid.

8

Conclusions and Future Work

During recent years, more advanced power electronics devices, novel sub-module and converter topologies have been developed and applied to practical projects. With more HVDC and MTDC systems in construction and operation, the large-scale AC/DC grid is also realizable in the near future. All these emerging technologies require the development of modeling, simulation, and implementation methodologies for off-line and real-time electromagnetic transient simulation. The simulation in the multi-physics domain can substantially increase the accuracy, since more realistic and detailed physical phenomena are taken into account. The advancements in IC technology and computing science can benefit the development of the real-time simulator, which has been examined in this work and requires further exploration.

In this thesis, variable time-stepping schemes for real-time simulation, device-level datasheet-based electrothermal model for HBSM and CDSM MMC have been proposed. The AC/DC grid has been simulated using hybrid modeling schemes and corresponding partition schemes in PSCAD/EMTDC®. The CIGRÉ DC grid has been modeled and emulated in real-time on MPSoC-FPGA platform. The proposed methodologies in this thesis address some perspectives of the above discussion; however, substantially more work is required to be conducted in the future driven by the continuous progress on the system to be simulated and the platform simulated on. The specific and detailed contributions of this thesis, corresponding applications, and the directions of future work are described in this chapter.

8.1   Contributions of This Thesis

The main contributions of this thesis are summarized as follows:

- **Variable Time-Stepping Schemes for Real-Time EMT Simulation**
  For the first time, variable time-stepping schemes have been applied to real-time EMT simulation for optimal utilization of computation capability and higher accuracy of high-frequency transients. The restrictions and the corresponding mitigating measurements are presented in detail. The hardware implementation especially for the modules related to the realization of the variable time-stepping schemes are described.

- **Datasheet-Based Device-Level Electrothermal Model for MMC**
  Datasheet-based device-level electrothermal model has been proposed. Such a modeling scheme uses the parameters and plots which can be obtained from manufacturer's datasheet. The calculated power losses and the junction temperatures dynamically affect the electrical model parameters of IGBT and diode. The electrothermal model not only improves the calculation accuracy, but also provides the direct indicators to evaluate the converter efficiency and operation security. This work also develops the appropriate interface schemes for both HBSM and CDSM to combine the electrothermal model to the MMC model. Equivalent circuit modeling scheme is applied to simplify the complex circuit model of CDSM ensuring the real-time performance.

- **Hybrid Modeling Scheme and Grid Partition Schemes**
  The hybrid modeling scheme for converters and other elements is proposed to conduct the detailed and accurate simulation for the zone of interest and maintain the scale of a large grid. Such a scheme is applied to the off-line simulation of the AC/DC grid and the real-time emulation of the CIGRÉ DC grid. The grid partition schemes based on the distance, the node number, and the network coupling are proposed to decompose the gird to the detailed zone, the accurate zone, and the averaged zone.

- **CIGRÉ DC Grid and AC/DC Grid Modeling**
  The AC/DC grid composed of the complete CIGRÉ DC gird, 39-bus AC grid, and the wind farm has been detailed modeled in PSCAD/EMTDC®. The algorithm of the solver and the components existing in CIGRÉ DC grid, such as MMC, transformer, frequency dependent transmission lines, are developed for further real-time hardware implementation and emulation.

- **MPSoC-FPGA Platform Development**
  This work explores the use of the MPSoC device and develops the hybrid MPSoC-FPGA platform to provide more logic resources and more flexible computing architecture. The communication between the FPGA board and the MPSoC board has been established through QSFP/SPF cable and Aurora IP core.

- **Hardware Implementation for Real-Time Emulator**

FPGA boards, MPSoC board, and the MPSoC-FPGA platform are all utilized to implement the real-time emulator realizing and verifying the proposed methodologies. The detailed hardware design of various case studies are developed and presented in detail in the corresponding chapters.

8.2 Applications

This section describes the applications of applying the detailed electrothermal model for off-line and real-time simulation of AC/DC grid. Such applications exist in the design, testing, and operation stages of the power converter and power system, which are summarized as follows:

- In the design stage, the detailed device-level data provided by the electrothermal model can be used to evaluate the model selection of IGBT modules, control algorithm, and the heatsink design from thermal perspective. In this stage, real-time simulation is not required, however, it can substantially increase the efficiency for design iterations.

- Once the control and power equipment are designed, they are often required to conduct HIL test before installing. The operator may require a comprehensive verification of the product from the manufacturer, which includes the basic functionality, security, and economy. The thermal data is useful for the verification of economic efficiency during the normal operation and the security during the fault transients. Such simulation must be conducted in real-time.

- In the operation stage, the operators need to run a large power system with sophisticated control and protection schemes. The real-time simulator can be used to train the operator for different scenarios. The detailed modeling scheme can present a high-fidelity simulation environment representing the real power system.

- It is envisioned that the real-time simulation of the power system can be very accurate in the future. The real-time simulation and the real system operate using the same control data and they respond in a very similar fashion. If the monitored electrical parameters and waveforms from the real system are very different from the simulation results, the real-time simulator can be used to detect the fault of the real system in the life cycle. It is believed that the electrothermal and other physical phenomena must be considered to achieve the high accuracy of the real-time simulation.

8.3 Directions for Future Work

The following topics are proposed for future work:

- The variable time-stepping schemes can be developed for larger power system and power electronics system. The modeling schemes and solution schemes for various components, such as converters, electrical machines, need to be developed.

- The electrothermal modeling scheme can be further improved, especially for the power losses and electrical parameter fitting. Higher order equations can be applied instead of linearized interpolation, which also requires more inputs from a detailed datasheet or field experiments.

- Transient stability simulation can be applied to the AC/DC grid. It can also work with EMT simulation to compose a co-simulation strategy.

- More FPGA and MPSoC boards can be interconnected to provide significantly more logic resources and higher computing performance. More communication channels can be established.

- The host computer system and graphical processing unit for general-purpose computing can be integrated with the FPGA-MPSoC platform to form a more powerful computing system, which provides more flexibility and computing capability for various tasks.

- With the accurately modeled AC/DC grid on PSCAD/EMTDC$^{\circledR}$ and the real-time DC grid emulator, more tests and researches can be conducted to study the interactive phenomena of the AC and DC grid. Novel supervisory control and protection strategy can be verified with the simulation system.

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A
Parameters for Case Studies

A.1 Parameters of Case 1 in Chapter 3

Table A.1: Parameters of Case 1

Circuit parameter	Value
Vs (peak-peak)	10V
Vs frequency	5kHz
R_s	1mΩ
R_L	1Ω
I_s	10^{-12}A
τ	10μs
T_m	5μs
V_T	25.9mV
n	2

A.2 Parameters of Case 2 in Chapter 3

V-I characteristics for surge arresters: [(0kV, 0kA), (263.82kV, 0.001kA), (317.19kV, 0.1kA), (362.42kV, 2.8kA), (429.89kV, 200kA)].

A.3 Parameters for Case Study in Chapter 4

Table A.2: Parameters of Case 2

Circuit parameter	Value
Base power	200MW
Base frequency	60Hz
$Vs(L-L)$	120kV
Rs	1Ω
Transformer voltage	115kV/230kV
Transformer leakage inductance	0.16pu
Transformer copper loss	0.004pu
Line segment L_1 length	50km
Line segment L_2 length	50km
Line inductance: mode +	0.9337mH/km
Line inductance: mode 0	4.1264mH/km
Line capacitance: mode +	12.74nF/km
Line capacitance: mode 0	7.751nF/km
L_L	2mH
R_L	265Ω

Table A.3: Circuit Parameters for two MMC test cases

Circuit parameter	Single-phase 5-level	Three-phase 9-level
SMs in one phase	8	16
V_{DC}	7200V	14400V
L_m	2mH	5mH
C (for each SM)	4000μF	4000μF
R_s	3.6Ω	7.4mΩ
L_s	1mH	2.5mH
V_s (L-L)	n/a	7200V

A.4   Parameters for Case Study in Chapter 5

Table A.4: Parameters of Case Study

Circuit parameter	Value
Vs amplitude (RMS)	220kV
Vs frequency	50Hz
R_s	0.6Ω
L_s	30mH
Arm inductor L_m	18.9mH
SM capacitance	2mF
Transmission line voltage	+/-200kV
Transmission line distance	100km
Transmission line surge impedance	394Ω

A.5 Parameters of CIGRÉ DC grid test system

This section presents some major parameters of the CIGRÉ DC grid test system [2].

Table A.5: System Data

System	Voltage[kV]
AC Onshore	380
AC Offshore	145
DC Sym. Monopole	+/- 200
DC Bipole	+/- 400

Table A.6: AC Bus Data

Bus	Bus Type	Generation [MW]	Load [MW]
Ba-A0	Slack Bus	-	-
Ba-A1	PQ	-2000	1000
Ba-B0	Slack Bus	-	-
Ba-B1	PQ	-1000	2200
Ba-B2	PQ	-1000	2300
Ba-B3	PQ	-1000	1900
Ba-C1	PQ	-500	0
Ba-C2	PQ	-500	0
Ba-D1	PQ	-1000	0
Ba-E1	PQ	0	100
Ba-F1	PQ	-500	0

Table A.7: Converter Station Data

AC-DC Converter Station	Power Rating [MVA]
Cm-A1	800
Cm-C1	800
Cm-B2	800
Cm-B3	1200
Cm-E1	200
Cm-F1	800
Cb-A1	2*1200
Cb-B1	2*1200
Cb-B2	2*1200
Cb-C2	2*400
Cb-D1	2*800