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Grid Phase and Harmonic Detection Using
Cascaded Delayed Signal Cancellation Technique

by

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Abstract

Power converters are indispensable in modern energy conversion and utilization systems. For their control, there are two interesting topics: one is grid phase detection for their grid-tied operation; the other is harmonic detection for power quality improvement. Both problems involve sequence separation and signal detection, which is always challenged by voltage unbalance, harmonics and other disturbances.

It is revealed in this thesis that the solution to the two problems can be rooted in the same technique, namely cascaded delayed signal cancellation (CDSC), which can isolate the positive-sequence fundamental signal from arbitrary harmonic patterns. It can be further renovated to extract any harmonic. Based on it, an advanced phase-locked loop system can be built for rapid, accurate and frequency adaptive grid phase and harmonic detection. For the practical implementation of the system, an effective discretization error reduction method is also developed. All system performances are verified by experiments.

Acknowledgment

I would like to express my deepest gratitude to my supervisor, Dr. Yunwei (Ryan) Li. His broad knowledge and insightful guidance are the keywords of this fruitful and rewarding research project. Without his support, I would not be able to step onto this new journey towards a higher standard of excellence.

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Finally, I am immensely indebted to my dear family—my father Xijian Wang, who is the first teacher in my life, and my soulmate Shijing (Crystal) Yang, who has been patiently accompanying me all the way through.

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List of Symbols

a	Unit-length rotating factor $a = \mathrm{e}^{\mathrm{j}120^\circ}$
a_1, a_2	Interpolation coefficients
$\vec{A}^{\,h^+}$	Adjustment factor on harmonic h^+
A^{h^+}	Modulus of $\vec{A}^{\,h^+}$
α	Parameter of the discrete PI controller
α^{h^+}	Phase angle of $\vec{A}^{\,h^+}$
b, β, b_1, b_2	Parameters to calculate the harmonic gain of the discrete DSC with interpolation
b', β', b_1', b_2'	Parameters to calculate the harmonic gain of the discrete DSC with interpolation when the original gain is set at zero
δ	Phase error
ΔT_r	Absolute delay time error
e	Euler's number $\mathrm{e} = 2.71828\,18284\ldots$
$\varepsilon_\mathrm{r}, \varepsilon_\mathrm{f}, \varepsilon_\mathrm{c}$	Relative delay error: general, round-down and round-up
f	Grid fundamental frequency (Hz)
f_s	Digital system sampling frequency (kHz)
$F(s)$	Transfer function of filters
φ	Initial phase angle of voltage signal
$G(s)$	Closed-loop transfer function of control systems
$G_0(s)$	Open-loop transfer function of control systems

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$\vec{G}_n^{\,h}$	Harmonic gain of the continuous DSC with delay factor n at harmonic h
G_n^h	Modulus of $\vec{G}_n^{\,h}$
ϕ_n^h	Phase angle of $\vec{G}_n^{\,h}$
$\vec{G}_{n\mathrm{r}}^{\,h}$	Harmonic gain of the discrete DSC with delay factor n at harmonic h
$\vec{G}_{n\mathrm{i}}^{\,h}$	Harmonic gain of the discrete DSC with interpolation
$\vec{G}_{n,m}^{\,h}$	Cascaded harmonic gain of the continuous CDSC with delay factors n and m at harmonic h
$\vec{G}_{n,m\mathrm{r}}^{\,h}$	Cascaded harmonic gain of the discrete CDSC
$\gamma_\mathrm{r}, \gamma_\mathrm{f}, \gamma_\mathrm{c}, \gamma_\mathrm{i}$	Harmonic gain error of the discrete DSC: general, round-down, round-up and interpolation
h	Harmonic order
h^*	Targeted harmonic order of DSC
h^+	Harmonic to extract by DSC/CDSC
h^-	Harmonic to eliminate by DSC/CDSC
$H, -H$	Upper and lower limits of existing harmonic order
$\boldsymbol{i}_{abc}$	Stationary *abc*-frame current signal
$\boldsymbol{i}_{dq}$	Synchronous *dq*-frame current signal
$\boldsymbol{i}_{dq}^*$	Reference value for the synchronous *dq*-frame current signal
i_dc	Dc current drawn by APF to charge the energy storage element
i_F	Filter current in APF system
i_L	Load current in APF system
$i_\mathrm{L,fund}$	Fundamental component of the load current in APF system
$i_\mathrm{L,harm}$	Harmonic content of the load current in APF system
$\boldsymbol{i}_\mathrm{L,harm}$	Detected load harmonics in APF system
i_S	Supply current in APF system
j	Imaginary unit $\mathrm{j} = \sqrt{-1}$
k	Integer index
K_i	Integral coefficient of PI controller
K_p	Proportional coefficient of PI controller

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n, m	Delay factors
N	Number of sample points in a fundamental period
N_h	Number of harmonics to detect
N_n	Ideal number of sample points in delay time T/n
$N_{n\mathrm{r}}, N_{n\mathrm{f}}, N_{n\mathrm{c}}$	Rounded results of N_n: general, round-down and round-up
ω	Grid fundamental angular frequency (rad/s)
ω_b	Bandwidth frequency of control systems (rad/s)
ω_f	Cut-off frequency of filters (rad/s)
ω_ff	Feedforward frequency in dqPLL (rad/s)
ω_n	Undamped natural oscillation frequency of control systems (rad/s)
π	Mathematical constant $\pi = 3.14159\,26535\ldots$
s, z	Complex numbers used in Laplace and Z-transforms
$\int$	Integrator
t	Time (s)
T	Grid fundamental period (ms)
T_s	Digital system sampling period (ms)
θ	Phase angle of the grid voltage space vector (rad)
ϑ	Phase different between the d- and the α-axes of the synchronous dq- and the stationary $\alpha\beta$-frames (rad)
θ_n	Delayed angle in the renovated DSC (rad)
θ_r	Rotation angle in the renovated DSC (rad)
Θ	Laplace transform of the phase angle of the grid voltage space vector
u, u'	General denotation for the voltage/current signals processed by SDFT
v	Voltage signal (V, p.u.)
$\boldsymbol{v}_{abc}, v_a, v_b, v_c$	Time-domain stationary abc-frame voltage signal and its components (V, p.u.)
$\boldsymbol{v}^*_{abc}$	Reference value for the voltage signal (V, p.u.)
$\vec{v}_{abc}$	Stationary abc-frame voltage space vector
$\boldsymbol{v}_{\alpha\beta}, v_\alpha, v_\beta$	Time-domain stationary $\alpha\beta$-frame voltage signal and its components (V, p.u.)
$\vec{v}_{\alpha\beta}$	Stationary $\alpha\beta$-frame voltage space vector

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$\boldsymbol{v}_{dq}, v_d, v_q$	Time-domain synchronous dq-frame voltage signal and its components (V, p.u.)
$\vec{v}_{dq}$	Synchronous dq-frame voltage space vector
v_{dc}	Dc link voltage in DG system (V, p.u.)
$\boldsymbol{v}_{\mathrm{ref}}$	PWM reference voltage in APF system (V, p.u.)
V	Peak value of voltage signal (V, p.u.)
V_a, V_b, V_c	Peak values of phase a, b, c voltage signals (V, p.u.)
ζ	Damping ratio of control systems

List of Abbreviations

A/D	Analog-to-Digital
ac	Alternating Current
ANF	Adaptive Notch Filter(ing)
ANN	Artificial Neural Network
APF	Active Power Filter
ASD	Adjustable Speed Drive
ASRF-PLL	Autoadjustable Synchronous Reference Frame Phase-Locked Loop
BPF	Band-Pass Filter(ing)
CDSC	Cascaded Delayed Signal Cancellation
CDSC-PLL	Cascaded Delayed Signal Cancellation Phase-Locked Loop
D/A	Digital-to-Analog
dc	Direct Current
DDSRF-PLL	Decoupled Double Synchronous Reference Frame Phase-Locked Loop
DFT	Discrete Fourier Transform
DG	Distributed Generation
*dq*PLL	Synchronous *dq*-Frame Phase-Locked Loop
DSC	Delayed Signal Cancellation
DSC-PLL	Delayed Signal Cancellation Phase-Locked Loop
DSP	Digital Signal Processor/Processing
EDSC-PLL	Enhanced Delayed Signal Cancellation Phase-Locked Loop

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EPLL	Enhanced Phase-Locked Loop
FC	Fuel Cell
FFL	Frequency Feedback Loop
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
GDSC-PLL	Generalized Delayed Signal Cancellation Phase-Locked Loop
HPF	High-Pass Filter(ing)
I/O	Input/Output
LF	Loop Filter
LPF	Low-Pass Filter(ing)
MA-PLL	Moving Average Phase-Locked Loop
MCCF-PLL	Multiple Complex-Coefficient-Filter Phase-Locked Loop
MSOGI	Multiple Second-Order Generalized Integrators
PD	Phase Detection
PF	Passive Filter
PI	Proportional-Integral
PLL	Phase-Locked Loop
*pq*PLL	Instantaneous *pq* Power Phase-Locked Loop
PV	Photovoltaic
PWM	Pulse-Width Modulation
QPLL	Quadrature Phase-Locked Loop
RDFT	Recursive Discrete Fourier Transform
RES	Renewable Energy Source
RMS	Root-Mean-Square
RTI	Real-Time Interface
SDFT	Sliding Discrete Fourier Transform
SOGI	Second-Order Generalized Integrator
SOGI-PLL	Second-Order Generalized Integrator Phase-Locked Loop
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop

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SSI	Sinusoidal Signal Integrator
SV-DFT	Space Vector Discrete Fourier Transform
SVF	Space Vector Filtering
THD	Total Harmonic Distortion
UPQC	United Power Quality Conditioner
V2G	Vehicle-to-Grid
VCO	Voltage-Controlled Oscillator
VOC	Vector-Oriented Control
WLSE	Weighted Least Square Estimation
WMV	Weighted Mean Value
WT	Wind Turbine
ZCD	Zero-Crossings Detection

Chapter 1

Introduction

In the pursuit of smarter, cleaner, more flexible and more sustainable energy systems, power electronics have proven to be a key one of the enabling technologies, and have gained widespread applications in all the stages of the generation, delivery, storage and utilization of electric power.

During the operation of power electronic systems, the controllers must obtain pertinent information from the operating environment, so as to properly generate reference signals for the converters, and produce required outcomes in terms of the power flow and the power quality [1, 2].

A representative example is the control of the grid-tied converters in distributed generation (DG) units and the grid-connected chargers in electric-vehicle-to-grid (V2G) operations, where the phase angle of the power source must be detected—such information is required to synchronize the output current of the power converters with the sources, and so achieve proper active and reactive power exchange between them [3–6].

Another example lies in power quality compensation devices, such as active power filters (APFs), unified power quality conditioners (UPQCs), etc. During the operation of these devices, system power harmonics and the other power quality disturbances [7] must be promptly and accurately detected, so they can be responsively counterbalanced, and the rest parts of the power system can be refrained from those disturbances.

For the control schemes of both examples, rapid, accurate and robust sequence separation and signal detection play a critical role. However, the detection process is always challenged by various signal disturbances, such as three-phase unbalance, harmonics, jitters and so forth. The change of working conditions, such as grid frequency variation, can have a side-effect on the detection process, too.

In response to such challenges, the author has been motivated in this research program to develop a superior signal detection technique, namely the cascaded delayed signal cancellation (CDSC) operation. An advanced signal detection phase-locked loop (PLL), namely CDSC-PLL, is also built around the CDSC operation and is implemented and verified. In this thesis, the proposed technique is formulated to address the representative problems of grid phase detection and selective harmonic detection, but it can also be adapted to a wider range of applications.

The following sections elaborate the background and the state of the art regarding the studied problems, introduce the motivation and the contributions of this research project, and outline the structure of this thesis.

1.1 The Problem of Grid Phase Detection

1.1.1 Problem Background

Distributed generation systems are generally based on renewable energy sources (RESs) and micro-sources, such as photovoltaic (PV) units, wind turbines (WTs), fuel cells (FCs) and microturbines, etc. For these energy sources, power converters are required to interface with the main grid. As demonstrated by the example DG system in Figure 1.1, when the DG unit is operated in the grid-connected mode, the controller must detect grid phase angle θ from the grid voltage signal $\boldsymbol{v}_{abc}$ to generate the synchronized reference signal $\boldsymbol{v}^*_{abc}$, which is required by the pulse-width modulation (PWM) process of the grid interfacing converter.

Ideally, θ can be mathematically calculated from the sensed values of $\boldsymbol{v}_{abc}$. In practice, however, $\boldsymbol{v}_{abc}$ is contaminated by everlasting power quality disturbances and sensing noises. Therefore, the detection of θ usually requires certain signal processing procedures, rendering more complex detection schemes necessary.

Despite the concrete formulation of the grid phase detection schemes, their basic objectives are

1. Accurately isolate the positive-sequence fundamental component of $\boldsymbol{v}_{abc}$ from the contaminating contents (voltage unbalance, harmonics, etc)

2. Promptly track θ of this component through various short-term disturbances (phase jumps, frequency variations, voltage sags and swells, etc), and

3. Stably adapt to varied working conditions (grid voltage and frequency shifts, etc).

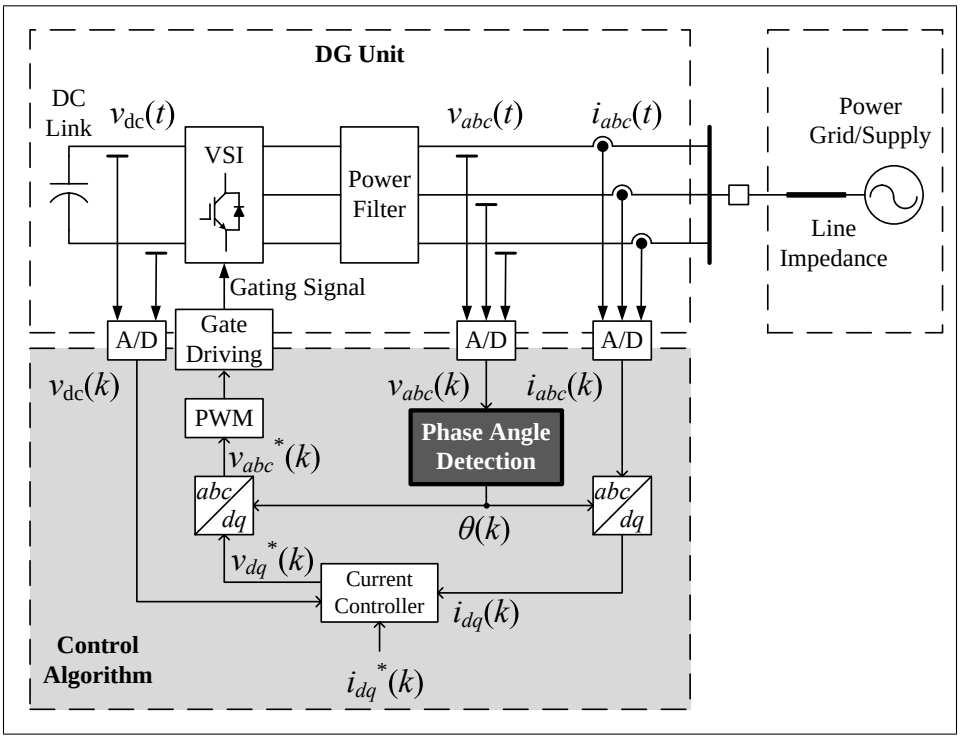


Figure 1.1: Diagram of a grid-connected DG system and its control algorithm that shows the location and function of the grid phase angle detection block.

Besides the basic objectives, numerous other design and implementation factors should also be taken into account, such as the computational complexity, the storage overhead, the robustness in varying working conditions, etc.

These requirements are often conflicted in nature, and hence a variety of grid phase detection schemes have been developed by weighting different aspects against their benefits and making certain trade-offs. They are depicted in the following subsection.

1.1.2 State of the Art

As illustrated by the tree diagram in Figure 1.2, common grid phase detection methods can be generally classified into the frequency-domain methods and the time-domain ones.

The most renowned frequency-domain detection methods are discrete Fourier transform (DFT) and fast Fourier transform (FFT) [8, 9]. DFT transforms the discrete time-domain signal into the frequency domain, and determines the magnitude and the phase angle of all harmonic components up to the Nyquist frequency, including the fundamental one as well. FFT improves DFT by significantly reducing

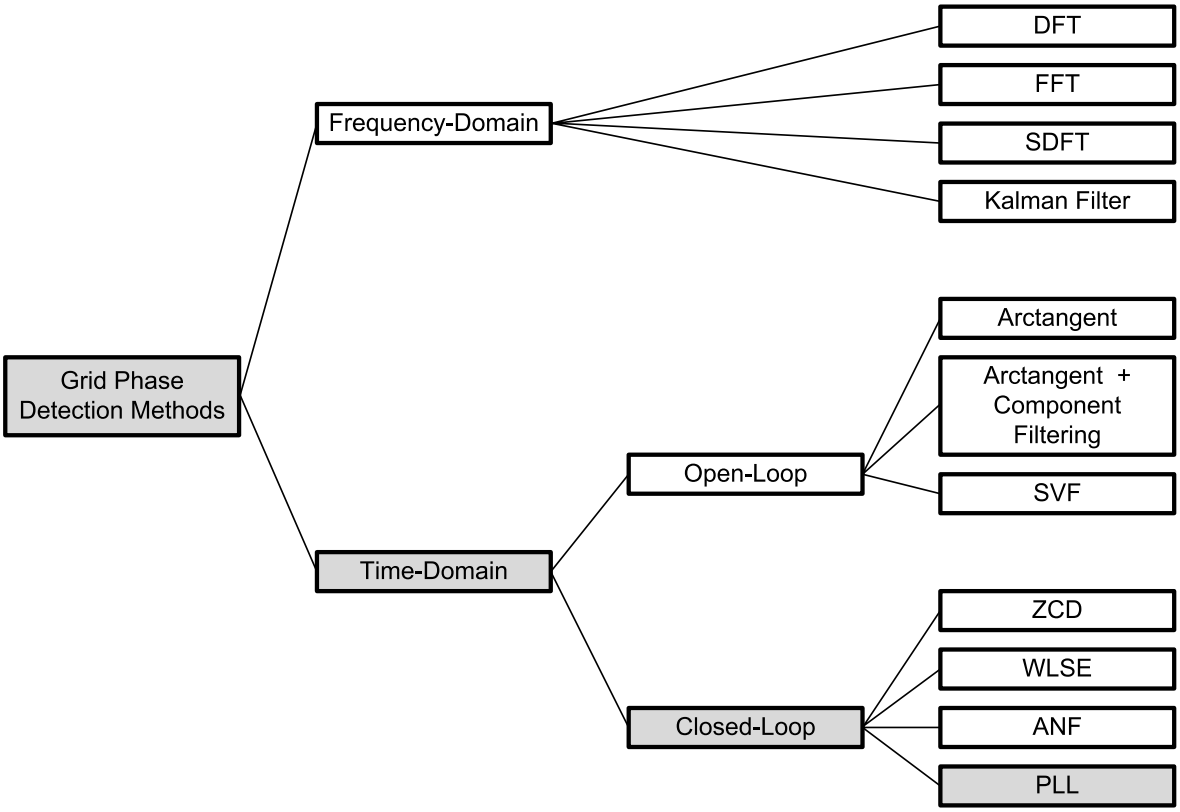


Figure 1.2: Hierarchical classification of the common grid phase detection methods.

- DFT = Discrete Fourier Transform
- FFT = Fast Fourier Transform
- SDFT = Sliding Discrete Fourier Transform
- SVF = Space Vector Filtering
- ZCD = Zero-Crossings Detection
- WLSE = Weighted Least Square Estimation
- ANF = Adaptive Notch Filtering
- PLL = Phase-Locked Loop

the number of calculations when certain criteria can be met.

In real-time control systems, the input signal is repetitively sampled and updated through A/D conversion. Therefore, DFT is modified into the sliding DFT (SDFT), also known as the recursive DFT (RDFT), for this situation [10,11]. As illustrated by Figure 1.3, SDFT has a "sliding window" of N signal samples, which are sensed at T_s interval (the sliding window length $N \cdot T_s$ must be an integer multiple of the fundamental signal period T). After applying DFT to all the signal samples $u(k), u(k-1), \ldots u(k-N)$ in the sliding window, the window shifts forward by one signal sample, and the DFT is recalculated on $u'(k), u'(k-1), \ldots u'(k-N)$ in the new window. Some intermediate results from the previous DFT can be used to reduce the number of calculations needed in this round.

Besides DFT, FFT and SDFT, there are also other frequency-domain methods based on non-Fourier

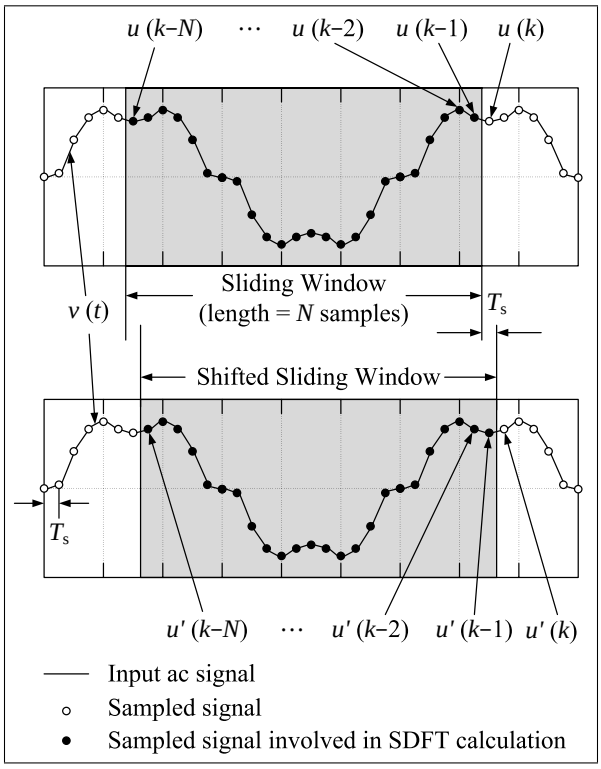


Figure 1.3: Illustration of the operation of sliding discrete Fourier transform (SDFT) for grid phase detection.

transforms, such as Kalman fitering and discrete cosine transform [12, 13].

Evaluation of these methods with a standardized experimental setup [14, 15] indicates that the frequency-domain methods have at least one cycle settling time, and require more data storage and computational resources, hence are generally more suitable for harmonic monitoring and metering. On the other hand, time-domain methods function better for the purpose of real-time control.

Depending on the construction form of the detection scheme, time-domain methods can be subdivided into two general types: the open-loop and the closed-loop ones. The open-loop methods include the arctangent method, the improved arctangent method with component filtering, and the space vector filtering (SVF) method [16, 17]. The closed-loop methods include the zero-crossings detection (ZCD), the weighted least square estimation (WLSE), the adaptive notch filtering (ANF), and the phase-locked loop (PLL) techniques [18, 19].

The simplest open-loop method is based on four-quadrant arctangent calculation. This method transforms the *abc*-frame grid voltage signal $\boldsymbol{v}_{abc}$ into the $\alpha\beta$-frame by Clarke transformation, and the

resulted $\boldsymbol{v}_{\alpha\beta}$ can then be used to calculate the phase angle θ:

$$\theta = \arctan\left(\frac{v_\beta}{v_\alpha}\right) + \begin{cases} 0, & \text{if } v_\alpha \geq 0 \\ \pi, & \text{if } v_\alpha < 0. \end{cases} \tag{1.1}$$

Obviously, all the harmonics and other disturbances in $\boldsymbol{v}_{\alpha\beta}$ will be simultaneously reflected in the calculated θ, and so [16] suggests to filter the $\alpha\beta$-components with low-pass or band pass filters before doing the arctangent calculation. However, such filters cannot deal with the very common voltage unbalance, because the unbalanced signal can be decomposed into the positive- and the negative-sequence components, which are at the same fundamental frequency.

SVF method [17] maintains a local estimated signal $\hat{\boldsymbol{v}}_{\alpha\beta}$. The detected $\boldsymbol{v}_{\alpha\beta}$ is continuously "blended" into $\hat{\boldsymbol{v}}_{\alpha\beta}$ with a weighting factor, while θ is calculated with (1.1) from the blended result. Such a technique can "cushion" abrupt signal variations, but has no efficacy with steady-state disturbances, such as harmonics.

Comparatively speaking, the closed-loop methods contain one or multiple control loops, and so can achieve more accuracy and better controllability. The simplest one among them may be ZCD, which repetitively resets θ once a zero-crossing point in the voltage signal is detected [18], or employs the so-called lead-lag comparison and adjusts θ according to the zero crossings [19]. ZCD is usually quite sluggish as the algorithm only updates every half cycle; it is also prone to noises and jitters [20].

The basic idea of WLSE methods [21, 22] is to estimate all the harmonic components existing in the input signal and compare their composite result with the actual input. The error is then used to update the estimates by evaluating a covariance matrix. A recent progress of WLSE is published in [23], which adds a PLL to the scheme to obtain information on the real-time grid frequency. For all of these schemes, the covariance matrix expands squarely as the number of the harmonics to estimate increases, and therefore it would be really challenging for the computing platform when a wide range of harmonics are present.

ANF-based methods, as the name suggests, use a cluster of notch filters to isolate the fundamental and the harmonic components. Among them, the one to isolate the fundamental component (called the "master ANF block" so as to distinguish from the "slave ANF blocks" that isolate the rest harmonic components) also outputs an estimated fundamental frequency, which is used to adjust the filter parameters in all the ANF blocks. Such an adaption process is inevitably slow, and so the response of ANF

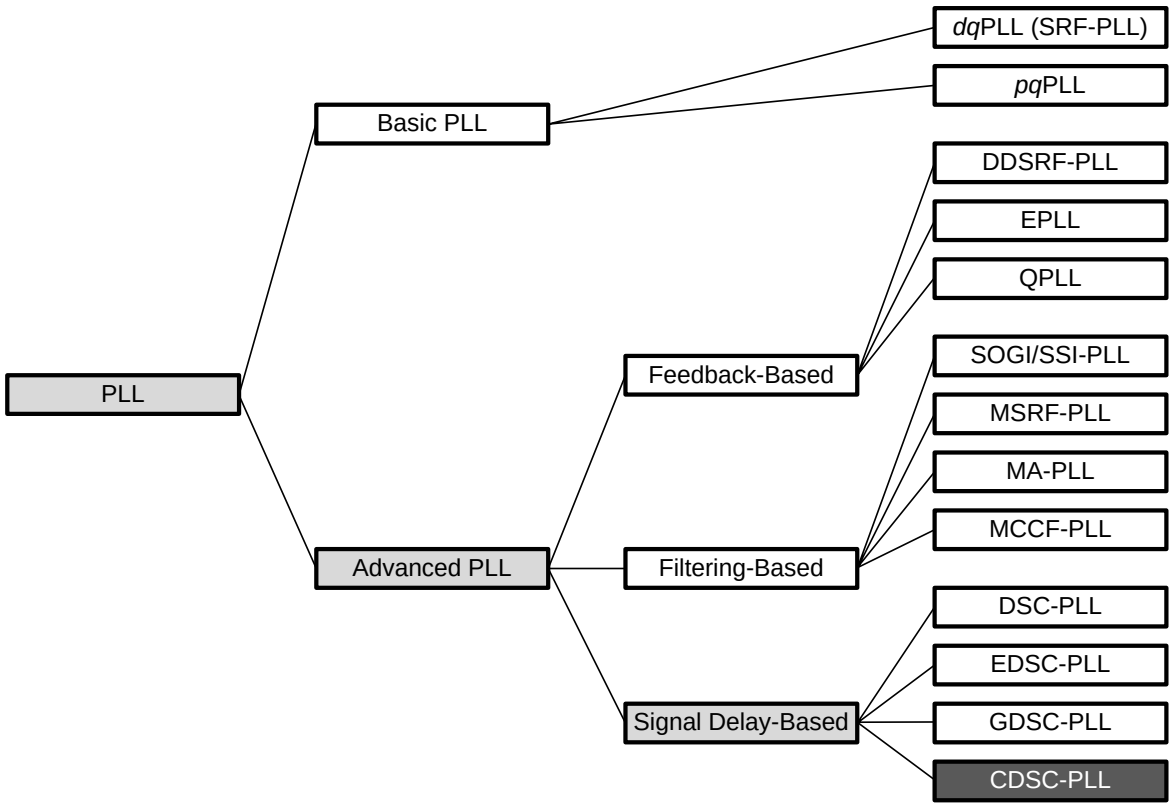


Figure 1.4: Hierarchical classification of the common grid phase detection PLLs.

- SRF-PLL = Synchronous Reference Frame PLL
- DDSRF-PLL = Decoupled Double Synchronous Reference Frames PLL
- EPLL = Enhanced PLL
- QPLL = Quadrature PLL
- SOGI/SSI-PLL = Second-Order Generalized Integrator / Sinusoidal Signal Integrator PLL
- MSRF-PLL = Modified Synchronous Reference Frame PLL
- MA-PLL = Moving Average PLL
- MCCF-PLL = Multiple Complex-Coefficient-Filter PLL
- DSC-PLL = Delayed Signal Cancellation PLL
- EDSC-PLL = Enhanced Delayed Signal Cancellation PLL
- GDSC-PLL = Generalized Delayed Signal Cancellation PLL
- CDSC-PLL = Cascaded Delayed Signal Cancellation PLL

systems to a load change often reaches a few cycles [24–26].

PLL has a long history in ac signal tracking [27, 28]. It has also been long recognized for grid phase (and other information) detection due to its simple structure and high flexibility for different problem backgrounds [18]. Therefore, a big family of PLL schemes have been formed, which can be categorized as the basic PLLs and the advanced ones, as illustrated by Figure 1.4.

The basic three-phase PLL can be constructed either with the tool of the synchronous reference frame (*dq*-frame) or with the concept of the instantaneous power (*pq* power); the resulted *dq*PLL (also known as SRF-PLL) [29, 30] and *pq*PLL [31, 32] schemes are mathematically equivalent to each other. Take only the *dq*PLL as an example, it receives the three-phase voltage/current signal as the input, and gives estimates of the magnitude, the frequency and the phase angle of the signal as the output. While

the internal details are discussed later in Chapter 2, here it can be simply described as a second-order control system with a certain bandwidth. A higher bandwidth improves system transient response at the cost of deteriorated harmonic immunity; a lower bandwidth has the opposite effect [30, 33], and the actual PLL bandwidth must be selected by the trade-off between the two aspects. As a result, a big difficulty is brought upfront to PLL tuning when the input signal is unbalanced—the negative-sequence component appears to be a second harmonic in the dq-frame; it requires a very low bandwidth to cut it off, which leads to extremely slow system dynamics.

Therefore, a natural thought is to introduce certain harmonic suppressing mechanism into PLL structure and avoid the abovementioned compromise. This thought has inspired various advanced PLL schemes, which can be roughly classified as the feedback-based, the filtering-based and the signal delay-based ones.

Among the feedback-based PLLs, decoupled double synchronous reference frame PLL (DDSRF-PLL) [34–36] transforms the input into two sets of oppositely rotating dq-frames, and use their respective outputs in multiple feedback loops to separate the positive- and negative-sequence components. This design, however, gives no consideration to input harmonics. Enhanced-PLL (EPLL) [37–39] and quadrature PLL (QPLL) [40] make use of the output estimates together with the input in a complex phase detector (PD) block to determine the estimating error and do adjustment accordingly. The two schemes (EPLL for three-phase signal and QPLL for single-phase signal) have transient response time from 30 ms to over 60 ms, which are generally longer than the filter- and the signal delay-based PLL schemes.

For the filtering-based advanced PLLs, the delicately designed filters (usually between the first to the fourth order) can be applied either to the $\alpha\beta$-or the dq-frame signal. Examples of dq-frame filtering include moving average PLL (MA-PLL) [41, 42], modified synchronous reference frame PLL (MSRF-PLL), and autoadjustable synchronous reference frame PLL (ASRF-PLL) [43]. Their common challenge is, the dq-frame filters are located within the PLL control loop, which affects system stability when the loop gain is high. Examples of $\alpha\beta$-frame filtering include multiple complex-coefficient-filter PLL (MCCF-PLL) [44] and second-order generalized integrator PLL (SOGI-PLL) [45, 46]. SOGI is also known as sinusoidal signal integrator (SSI) [47, 48]. Both MCCF and SOGI essentially perform resonant filtering (at the fundamental and/or the harmonic frequencies). They are known to have a few drawbacks, such as the incomplete harmonic rejection, as well as the sensitivity in the magnitude and the phase responses around the resonant points.

Signal delay-based PLL schemes are among the most recently emerged advanced PLLs. Their common idea is to construct operators that associate the input signal and its delayed versions. In terms of signal processing, the signal delay-based operators can be regarded as finite impulse response (FIR) filters of higher-order, which are capable of more flexible harmonic suppressing. Examples in this category include delayed signal cancellation PLL (DSC-PLL) [49, 50], enhanced delayed signal cancellation PLL (EDSC-PLL) [51], generalized delayed signal cancellation PLL (GDSC-PLL)[1] [53–55], as well as the CDSC-PLL [56–58] presented in this research project.

1.2 The Problem of Selective Harmonic Detection

1.2.1 Problem Background

The fast proliferating power electronics in today's energy systems are accompanied by increasing power quality problems, especially power system harmonics. In response to this challenge, researchers have been actively involved with the topic of harmonic compensation. Whether the task is accomplished by APFs that have a long history of practical use [14, 15], or is shouldered by DG units as recently emerged [1, 59, 60], harmonic detection always plays a critical role in their control.

A representative example of harmonic compensation system is the three-phase shunt APF [15] in Figure 1.5. The APF outputs current i_{F} to dynamically counterbalance the harmonic content in the distorted load current i_{L}, therefore the grid/supply current i_{S} is refrained from harmonic injection. To achieve this target, the harmonic detection block in the control algorithm must be able to process the sensed load current i_{L} and extract the harmonic content $\boldsymbol{i}_{\mathrm{L,harm}}$, which is then used by the voltage/current controller to generate PWM reference signal v_{ref} for the APF.

Besides the shown example of harmonic current detection in a shunt APF, harmonic voltage detection is also required in some occasions, e.g. series/hybrid APFs [61] and DG for distributed system power quality improvement [1,59,60]. For both harmonic current detection and voltage detection, the detection function can be implemented in an independent control block [14, 15], as demonstrated by the example APF control algorithm in Figure 1.5. It can be embedded in the controller [62, 63] as part of the control scheme, too.

The harmonic detection scheme has two types in terms of the expression of the extracted harmonic signal $\boldsymbol{i}_{\mathrm{L,harm}}$ [64, 65]:

[1] This technique is also known as space vector DFT (SV-DFT) [52].

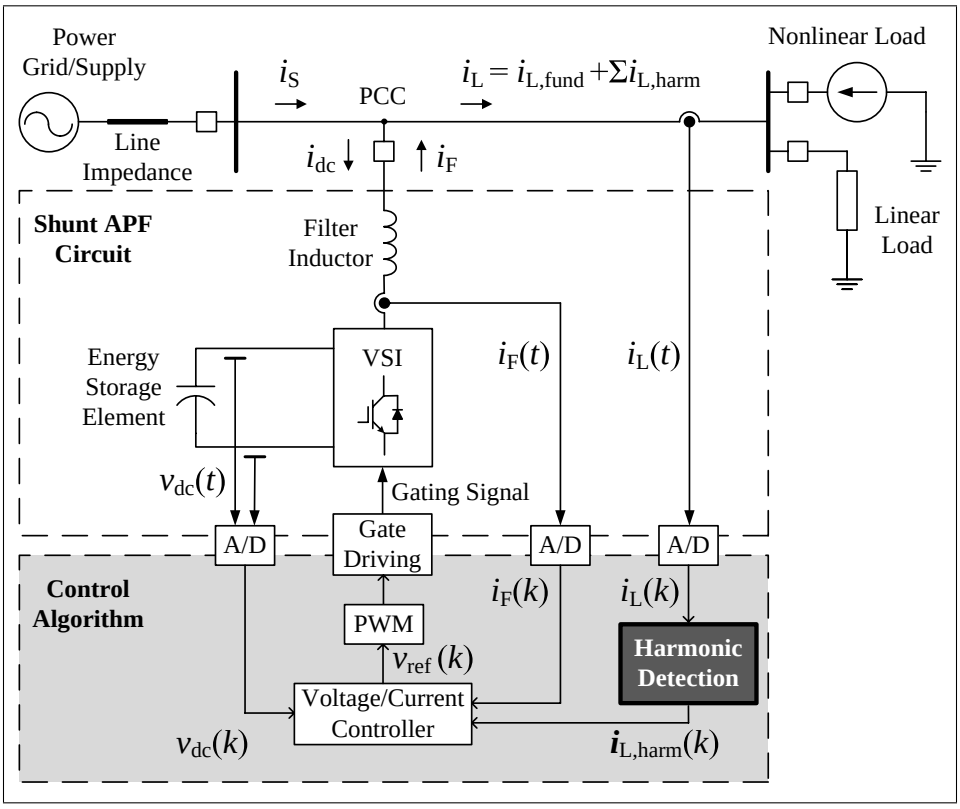


Figure 1.5: Diagram of a APF system and its control algorithm that shows the location and function of the load harmonic detection block.

1. *Overall harmonic detection*, which only eliminates the fundamental component in i_L and outputs the rest harmonic content as one signal.

2. *Selective harmonic detection*, which isolates individual harmonics and delivers them in the output as a set of signals.

Compare with overall harmonic detection, selective harmonic detection can offer some advantages and flexibilities in many harmonic control applications. For example,

1. The compensation system can be tuned to address the most problematic harmonics, avoiding unnecessary investment on excessive control bandwidth and converter ratings.

2. The compensation system has inherent sampling/actuation delay time, and the same delay time corresponds to substantially different delay angles for different harmonics. Selective harmonic compensation allows individual correction, as each harmonic reference can be adjusted by a unique compensation angle that correspondingly counterbalances the delay angle.

3. Sometimes a shunt APF is installed together with a passive filter (PF) to make a hybrid compensation system—the APF for the lower harmonic orders and the PF for the higher ones [61]. This is because PFs are bulky and uneconomic at low frequencies, while at high frequencies APFs are often restricted by their limited operating frequency. Besides, APFs can also suffer from the high switching $\mathrm{d}v/\mathrm{d}t$ that results in electromagnetic interference and insulation stress. For the case of hybrid compensation, selective harmonic detection must be employed to accordingly generate reference signal for the APF.

Due to the function in the whole control algorithm, a harmonic detection scheme must be able to detect the harmonic signals as accurately and fast as possible, so as to enable the compensation device to promptly respond to the frequent variations of the harmonic load current. As explained above, the capability of selective harmonic detection is also a must in some occasions. To address these requirements, many harmonic detection schemes have been proposed, and they are reviewed in the next subsection.

1.2.2 State of the Art

Similar to the problem of grid phase detection, harmonic detection schemes can also be formulated in the frequency or the time domain. As shown in Figure 1.6, the frequency-domain schemes include DFT, FFT, SDFT and Kalman filter, which are basically the same as the techniques used for grid phase detection. Just like the case of grid phase detection, their inherent one-cycle transient time and intensive calculations make them better candidates for use in metering and monitoring, rather than in real-time control systems.

The time-domain schemes are significantly different in terms of the operating principle and structure. They can be subdivided according to the theories and the operations they rely on, such as stationary reference frame filtering (or $\alpha\beta$-frame filtering), synchronous reference frame filtering (or dq-frame filtering), hybrid reference frame filtering, instantaneous power theory (or pq power theory), artificial neural network (ANN) theories and so on. While the abundant literature on this topic is reviewed in [15] and [61], a brief summary and some additional references are provided here.

Among the stationary reference frame ($\alpha\beta$-frame) schemes, the simplest one uses a notch filter at the fundamental frequency, and hence is called fundamental notch filtering method. It deeply attenuates the fundamental-frequency component, and outputs the a signal that contains the rest harmonic spectra.

A more complex stationary reference scheme is based on SOGI (also known as SSI). The operators

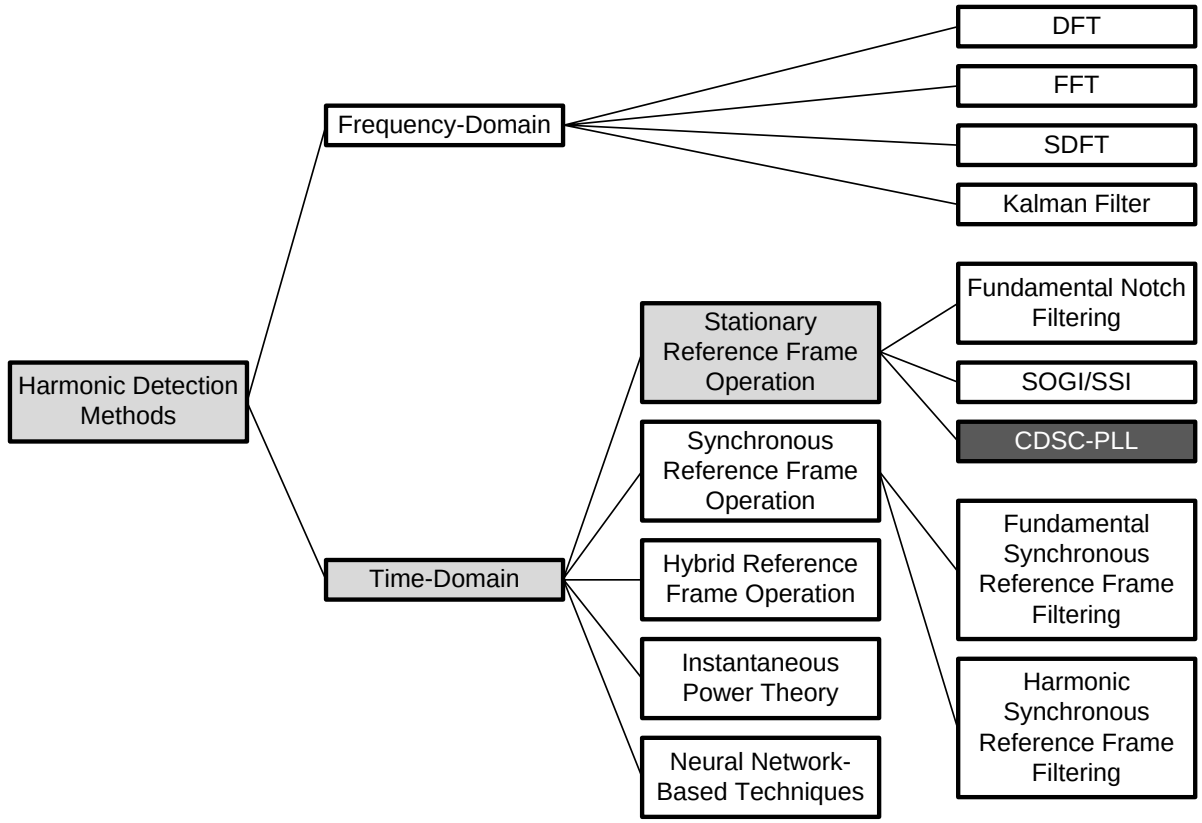


Figure 1.6: Hierarchical classification of the common harmonic detection methods.

- DFT = Discrete Fourier Transform
- FFT = Fast Fourier Transform
- SDFT = Sliding Discrete Fourier Transform
- SOGI = Second-Order Generalized Integrator
- SSI = Sinusoidal Signal Integrator
- CDSC-PLL = Cascaded Delayed Signal Cancellation PLL

are tuned to have multiple resonant points at some specified harmonic frequencies, usually ones with significant magnitude that require targeted compensation (such as the 5th, the 7th, etc). Therefore, the output signal only contains these problematic harmonics; the other harmonics, interharmonics and high frequency noises that are less concerned will not show up in the output.

As an improvement to the SOGI method, the multiple second-order generalized integrators (MSOGI) method [66] arranges multiple SOGI subsystems in parallel to extract individual harmonics. The extracted harmonics are then fedback and used by the SOGI subsystems: if one SOGI subsystem aims to extract a certain harmonic, then the other harmonics obtained through feedback are subtracted from the input signal for this SOGI subsystem, so as to minimize the interference from the irrelevant harmonics.

Among the synchronous reference frame (dq-frame) schemes, the simplest one is the fundamental synchronous reference frame filtering (or fundamental dq-frame filtering). It first transforms the input

signal into the dq-frame, where the positive-sequence fundamental component becomes a dc signal. Then the dc signal is rejected by a high pass filter (HPF), and the remaining signal that contains the complete harmonic spectra is transformed back into the $\alpha\beta$-frame as the output. For this method, sometimes the HPF mechanism is implemented by a LPF: the LPF extracts the dc component, which is fedback and subtracted from the original signal to obtain the harmonic content.

The fundamental dq-frame filtering is essentially equivalent to the $\alpha\beta$-frame notch filtering. Similarly, the MSOGI scheme has an equivalence in the dq-frame, which is called harmonic synchronous reference frame filtering (or harmonic dq-frame filtering). It utilizes multiple dq-frames, each rotating at a harmonic frequency of interest. Because a harmonic becomes a dc signal in its corresponding dq-frame, it can be easily isolated by a LPF. The obtained dq-frame harmonics are also transformed back into the $\alpha\beta$-frame as the output.

There also exist some more complex schemes, which are developed based on hybrid reference frame filtering [48], instantaneous power theory (or pq power theory), neural network theories [67–69], etc. The study of them is still undergoing.

Among the introduced popular schemes, MSOGI and harmonic dq-frame filtering are capable of selective harmonic detection. Although they have been successfully applied in harmonic compensation systems, their performance is also undermined by a few defects. The MSOGI method demands the number of SOGI subsystems be the same as the number of the significant harmonics. Therefore, when there are many significant harmonics, but only some of them need to be detected, there is a redundancy in the use of SOGI subsystems. Also, SOGI has drastic variation in the magnitude and phase response around the harmonic frequencies, and hence is prone to signal frequency fluctuation [59, 60]. On the other hand, the harmonic dq-frame filtering method has a low cut-off frequency and slow transient when dealing with unbalanced input signal. Both MSOGI and harmonic dq-frame filtering methods cannot achieve zero steady-state error, because the fundamental signal usually has much bigger magnitude than the harmonics, and can hardly be completely filtered out [70].

Through certain configuration process, the CDSC-PLL system in this research project can also be used to accomplish highly flexible and efficient selective harmonic detection. Perceived in a mathematical point of view, the CDSC operation it uses falls within the scope of stationary reference frame filtering. However, CDSC-PLL has compensated for the known defects of the peer schemes in this category.

The following section gives the reasons that have motivated the researcher to the development of CDSC-PLL, and highlights to the readers about the major contributions.

1.3 Motivation and Contributions of the Project

1.3.1 Motivation of the Research Project

Although the problems of grid phase detection and selective harmonic detection emerge from different practical backgrounds, they are both associated with the separation and detection of harmonic signals in real-time control systems: grid phase detection requires to isolate the positive-sequence fundamental component from the distorted grid voltage signal, and selective harmonic detection asks to individually extract harmonics from the distorted load current/voltage signal. Such inherent connection renders it possible to develop an technique that can be applied to tackle both problems.

This technique can be developed from signal delay operation. The reason is: time-domain harmonic signals can be represented by space vectors, which are rotated in the chosen reference frame at different harmonic frequencies. By delaying the space vectors for the same portion of time, the vectors can be shifted apart in the reference frame. Then by using certain trigonometric manipulation, different harmonic space vectors can be separated from each other. The reasoning is also true with the fundamental component, if it is seen as a wide-sense harmonic.

Originated from this general idea, the researcher first developed a kind of generalized delayed signal cancellation (DSC) operator, and then arranges it into the more advanced cascaded delayed signal cancellation (CDSC) operator. The DSC and CDSC operators are used as the cardinal building blocks of an advanced PLL system, namely CDSC-PLL. Through certain reconfiguration and renovation, the system can fulfill both the tasks of grid phase detection and selective harmonic detection in different circumstances, as unfolded in Chapters 2, 3 and 4.

1.3.2 Contributions of the Research Project

Major contributions of the research project include

- Derived the generalized DSC and CDSC operators in the dq- and the $\alpha\beta$-frames for fundamental signal extraction.
- Renovated the generalized DSC and CDSC operators for arbitrary harmonic extraction.
- Proposed the concept of harmonic gain of DSC and CDSC operators, and used the concept to create a convenient and systematical approach for parameters design. With this approach, the

CDSC operator can extract the fundamental signal from any harmonic scenarios; the renovated CDSC operator can further extract arbitrary harmonic from any harmonic scenarios.

- Designed the CDSC-PLL system, whose variants can deal with the problems of grid phase detection and selective harmonic detection in different circumstances. The presented CDSC-PLL has zero steady-state detection error, very fast transient response and robust frequency adaptability. It also features small memory overhead and light computational burden. Unlike some other schemes that require parameters retuning to address different tasks, the different aspects of the good performances of CDSC-PLL are achieved under the same system parameters.

- Investigated the discretization issues of the DSC/CDSC operators, which arise in their practical implementation with digital controllers. An efficient discretization error reduction method is developed, and the method can also benefit all the other delay-based signal detection techniques.

1.4 Thesis Structure

This thesis is organized as the follows:

Chapter 1 introduces the research background of the problems of grid phase detection and selective harmonic detection, the state of art of their solutions, the motivation and contributions of this research project, and the structure of this thesis.

Chapter 2 discusses the derivation of DSC/CDSC operators and the development of CDSC-PLL system used to deal with the problems of grid phase detection.

Chapter 3 renovates the proposed DSC/CDSC operators, as well as the related CDSC-PLL system, for the problem of selective harmonic detection.

Chapter 4 addresses the issues related to system discretization for the use in practical digital controllers, and formulates the discretization error reduction method for both of the two problems.

Chapter 5 describes the experimental platform and the numerous test cases designed to evaluate the performances of the grid phase detection CDSC-PLL, the selective harmonic detection CDSC-PLL, and the discretized DSC/CDSC operators. Comprehensive experimental results are reported and analyzed.

Chapter 6 concludes the thesis. It also makes a few recommendations for possible future research.

Besides the main body, this thesis also includes the lists of tables, figures, symbols, abbreviations, author's publications and references, as well as an index for readers' convenience.

Chapter 2

CDSC-PLL for Grid Phase Detection

2.1 Introduction

During the grid synchronization of DG units, PLL is well accepted as an efficient approach to detect grid phase angle. Conventional PLL schemes have to compromise between steady-state accuracy and transient dynamics when the grid voltage signal is polluted by voltage unbalance and/or harmonics, as explained in Section 1.1. Therefore, numerous advanced PLL schemes have been proposed. Among them, CDSC-PLL proves to be superior in terms of harmonic elimination ability, transient response, frequency adaptability and engineering efforts in implementation.

As suggested by the name, CDSC-PLL is formed as a PLL system augmented by the CDSC operator. The CDSC operator processes the input voltage signal and eliminates the harmonics it contains, leaving a "clean" signal to the PLL system. As a result, the PLL bandwidth can be set to a very high value to achieve excellent system dynamics, while no steady-state detection error arises due to the impact of the input harmonics.

Naturally, the CDSC operator is the key part of CDSC-PLL and must be carefully designed. The study in this chapter shows that it can be arranged as multiple DSC operators connected in series. Each DSC is configured to eliminate certain harmonics, and the CDSC collectively eliminates all undesired harmonics resting in the input. Through such a "sieving" process, only the positive-sequence fundamental signal is left as the input for the subsequent PLL block.

It should be pointed out that every DSC introduces certain time delay to the signal processing procedure, and the delay of the entire CDSC operator is an accumulated result. Therefore, DSC parameters

must be delicately selected to minimize the overall delay and prevent prolonged transient response.

An easy and straightforward approach has been formulated for optimal DSC parameters selection. The approach is based on the concept of harmonic gain—zero gain of a DSC on a harmonic means the DSC can eliminate the harmonic, while unity gain means the harmonic can pass through without attenuation. The overall harmonic gain of a CDSC is derived to be the product of the individual gains of all DSC blocks. That means a CDSC operator with properly chosen DSC blocks can eliminate all undesired harmonics step by step.

The calculation of harmonic gain and the construction of DSC are first done in the dq-frame, because the dq-frame has a feature that the original positive-sequence fundamental voltage is dc here, and that makes the derivation of DSC much easier and more intuitive. Then the dq-frame DSC is transferred into the $\alpha\beta$-frame with equivalent functionality. This is to avoid dq-frame DSC bringing time delay into the PLL loop and complicating system stability. It is mathematically proven that the $\alpha\beta$-frame DSC has identical harmonic gain as the dq-frame one, but it no longer has side-effect on system stability, as the time delay it involves is now located outside PLL loop. For the case of CDSC, one just needs to design the constituent DSC blocks in the dq-frame, then transfer the resulted CDSC configuration into the $\alpha\beta$-frame for practical implementation.

This chapter is unfolded from Section 2.2 that defines the representation of harmonic signals. Then Section 2.3 explains the structure and the operating principles of the basic PLL system. Section 2.4 elaborates DSC operator in the dq-frame as well as how to design their parameters with the tool of harmonic gain. Section 2.5 extends to dq-frame CDSC that contains multiple DSC blocks for a wider range of harmonic elimination. This section also presents the complete CDSC-PLL system. Section 2.6 and Section 2.7 show the process to transfer dq-frame DSC and CDSC into the $\alpha\beta$-frame, as well as how to construct CDSC-PLL based on the $\alpha\beta$-frame CDSC operator. Section 2.8 discusses the influence of grid frequency variation on CDSC-PLL performance; it also provides a robust solution based on a frequency feedback loop (FFL). Section 2.9 summarizes this chapter.

2.2 Representation of Harmonic Signals

For three-phase power systems, grid voltage can be described by either the rotating space vector or time-domain signals, whose mutual relationship is described by Table 2.1.

In the table, a is a unit-length rotating factor defined as $a = \mathrm{e}^{\mathrm{j}120^\circ} = -\frac{1}{2} + \mathrm{j}\frac{\sqrt{3}}{2}$, hence $a^2 = \mathrm{e}^{\mathrm{j}240^\circ} =$

Table 2.1: Mathematical representation of grid voltage quantities.

Space vectors	Stationary Reference frames		Synchronous Reference frame
	abc-frame	$\alpha\beta$-frame	*dq*-frame
	$\vec{v}_{abc} = \frac{2}{3}(v_a + av_b + a^2 v_c)$	$\vec{v}_{\alpha\beta} = v_\alpha + \mathrm{j}v_\beta$	$\vec{v}_{dq} = v_d + \mathrm{j}v_q$
Time-domain signals	$\boldsymbol{v}_{abc} = [v_a, v_b, v_c]^{\mathrm{T}} = \begin{bmatrix} V\cos\theta \\ V\cos(\theta - 120^\circ) \\ V\cos(\theta + 120^\circ) \end{bmatrix}$	$\boldsymbol{v}_{\alpha\beta} = [v_\alpha, v_\beta]^{\mathrm{T}} = \begin{bmatrix} V\cos\theta \\ V\sin\theta \end{bmatrix}$	$\boldsymbol{v}_{dq} = [v_d, v_q]^{\mathrm{T}} = \begin{bmatrix} V\cos\delta \\ V\sin\delta \end{bmatrix}$

$\mathrm{e}^{-\mathrm{j}120^\circ} = -\frac{1}{2} - \mathrm{j}\frac{\sqrt{3}}{2}$. Grid voltage space vector $\vec{v}$ can be coordinated in either the *stationary reference frame* (i.e. the *abc*- or the $\alpha\beta$-frame) or the *synchronous reference frame* (i.e. the *dq*-frame). In the former case, $\vec{v}$ is denoted as $\vec{v}_{abc}$ or $\vec{v}_{\alpha\beta}$. In the latter case, $\vec{v}$ is denoted as $\vec{v}_{dq}$. Its magnitude keeps the same in all the three frames; it can be denoted as V, which is equal to the peak value of grid phase voltage. The phase angle of $\vec{v}$ in the *abc*- and the $\alpha\beta$-frame is θ. In the *dq*-frame, however, the phase angle becomes $\delta = \theta - \vartheta$, where ϑ is the angle difference between the *d*-axis and the α-axis (the same as the *a*-axis). For simplicity, ϑ is usually chosen to be the same as θ, i.e. the *d*-axis is aligned along $\vec{v}$, so as to keep $\delta = 0, v_q = 0$, $v_d = V$. This is known as the voltage-oriented control (VOC) method for power electronic converters.

Use Table 2.1 to expand the vectors and compare their individual components on the two sides, it is easy to obtain the transformation of time-domain signals from the *abc*- to the $\alpha\beta$- and the *dq*-frames[1]:

$$\boldsymbol{v}_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \boldsymbol{T}_{\alpha\beta} \cdot \boldsymbol{v}_{abc} \tag{2.1a}$$

$$\boldsymbol{v}_{dq} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\vartheta & \sin\vartheta \\ -\sin\vartheta & \cos\vartheta \end{bmatrix} \cdot \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \boldsymbol{T}_{dq} \cdot \boldsymbol{v}_{\alpha\beta}. \tag{2.1b}$$

When the grid voltage is ideal, vector $\vec{v}_{\alpha\beta}$ is rotating at a constant frequency $\omega = \mathrm{d}\theta/\,\mathrm{d}t$, hence v_α and v_β in (2.1a) are all sinusoidal signals. However, the grid voltage is usually unbalanced and distorted,

[1]These formulae are also well known as Clarke and Park transformations.

and v_α and v_β are therefore comprised of a series of harmonic signals:

$$\begin{aligned}\vec{v}_{\alpha\beta} &= v_\alpha + \mathrm{j}v_\beta = \sum_{h=-H}^{H} v_\alpha^h + \mathrm{j}\cdot\sum_{h=-H}^{H} v_\beta^h \\ &= \sum_{h=-H}^{H} V^h\cos\theta^h + \mathrm{j}\cdot\sum_{h=-H}^{H} V^h\sin\theta^h \\ &= \sum_{h=-H}^{H} V^h\Big(\cos\theta^h + \mathrm{j}\sin\theta^h\Big) = \sum_{h=-H}^{H} V^h\mathrm{e}^{\mathrm{j}\theta^h} = \sum_{h=-H}^{H}\vec{v}_{\alpha\beta}^{\,h}\end{aligned} \tag{2.2}$$

where ω is the fundamental angular frequency and is equal to $2\pi f$. The instantaneous phase angle of each harmonic space vector $\theta^h = h\omega t + \varphi^h$. φ^h is the initial phase angle. Harmonic order $h = 0, \pm1, \pm2, \pm3, \ldots, \pm H$. The harmonic order h (in wide sense) ranges from the order of dc component to the possible maximum values H. A positive value of h indicates a positive-sequence harmonic, while a negative value indicates a negative-sequence one.

In other words, the harmonic distortion of time-domain voltage signals can be translated as: the space vector $\vec{v}_{\alpha\beta}$ is no longer a single vector, but the vectorial sum of a series of harmonic vectors, respectively rotating at harmonic frequencies $h\omega$. In this paper, h can be positive or negative, indicating harmonics are in positive- or negative-sequence regarding the fundamental component. In the stationary *abc*- and $\alpha\beta$-reference frames, positive-sequence harmonic vectors are rotating counterclockwise, while negative-sequence ones are rotating clockwise. Zero-sequence harmonics are disregarded, as they are usually blocked either in line-to-line voltage measurement or the *abc*–$\alpha\beta$ transformation.

Similarly, in the *dq*-frame

$$\begin{aligned}\vec{v}_{dq} &= v_d + \mathrm{j}v_q = \sum_{h=-H}^{H} v_d^h + \mathrm{j}\cdot\sum_{h=-H}^{H} v_q^h \\ &= \sum_{h=-H}^{H} V^h\cos\delta^h + \mathrm{j}\cdot\sum_{h=-H}^{H} V^h\sin\delta^h \\ &= \sum_{h=-H}^{H} V^h\Big(\cos\delta^h + \mathrm{j}\sin\delta^h\Big) = \sum_{h=-H}^{H} V^h\mathrm{e}^{\mathrm{j}\delta^h} = \sum_{h=-H}^{H}\vec{v}_{dq}^{\,h}\end{aligned} \tag{2.3}$$

where the instantaneous phase angle $\delta^h = h\omega t + \varphi^h$. h is the harmonic order in the *dq*-frame.

It should be noted that the *dq*-frame vector $\vec{v}_{dq}^{\,h}$ comes from $\alpha\beta$-frame vector $\vec{v}_{\alpha\beta}^{\,h+1}$, as the *dq*-frame itself is rotating counterclockwise at ω. For example, the positive-sequence fundamental vector $\vec{v}_{\alpha\beta}^{\,+1}$ becomes a dc signal $\vec{v}_{dq}^{\,0}$ in the *dq*-frame. On the other hand, the negative-sequence vector $\vec{v}_{\alpha\beta}^{\,-1}$, which

comes from unbalanced fundamental voltage, becomes a second harmonic $\vec{v}_{dq}^{-2}$ in the dq-frame.

Typically, power system harmonics (such as those injected by line-commutated diode rectifiers) possess orders of $h = -5, +7, -11, +13, \ldots$ Besides them, even-order harmonics can also be produced by loads operating in an aperiodic or a half-wave asymmetrical way, such as ac electric arc furnaces [7]. If distorted three-phase voltage signals are symmetrical, then the 1st harmonic (i.e. the fundamental component) should be in positive-sequence, the 2nd in negative-sequence, the 3rd in zero-sequence, and the subsequent harmonics repeat the pattern. However, nonlinear loads often operate in a three-phase asymmetrical manner [71]. Further considering the presence of single-phase nonlinear loads, it is very possible that the three-phase harmonics are asymmetrical. In this case, positive-, negative- and zero-sequence components at all harmonic orders can exist, and they can be mathematically resolved by the method of harmonic symmetrical components [72, 73].

For example, when the three-phase signal waveforms of a 5th harmonic voltage are symmetrical with the same magnitude $V_a^5 = V_b^5 = V_c^5 = 0.1$ p.u., only negative-sequence $V^{-5} = 0.1$ p.u. can be resolved, and it can be named as a "symmetrical harmonic". On the other hand, if $V_a^5 = 0.2$ p.u., $V_b^5 = V_c^5 = 0.1$ p.u., then besides $V^{-5} = 0.1$ p.u., one more $V^{+5} = 0.1$ p.u. can be resolved, and it is named as an "asymmetrical harmonic" in this thesis. By this definition, the commonly found negative-sequence fundamental voltage is also an asymmetrical harmonic.

In order to investigate the process of harmonic elimination in a general scope, even-order and asymmetrical harmonics are all taken into account in this thesis.

2.3 Structure and Principles of the Basic PLL

As an effective ac signal detection method, PLL has gained a widespread application in telecommunication, signal processing and automatic control. Its general principle is to find the phase error between the input and its estimated signals, and adjust the estimate accordingly until the two signals overlap with zero phase difference. At this time, the phase angle (and other information such as the frequency) can be readily obtained from the estimated signal.

In practice, PLL was first implemented by circuits with discrete components. Later, analog and digital integrated circuits were made available for PLL. Due to the popularity of digital controllers now, today's PLL systems are generally implemented by software [27].

For the grid phase detection in power converter control, it is common to use the basic PLL system

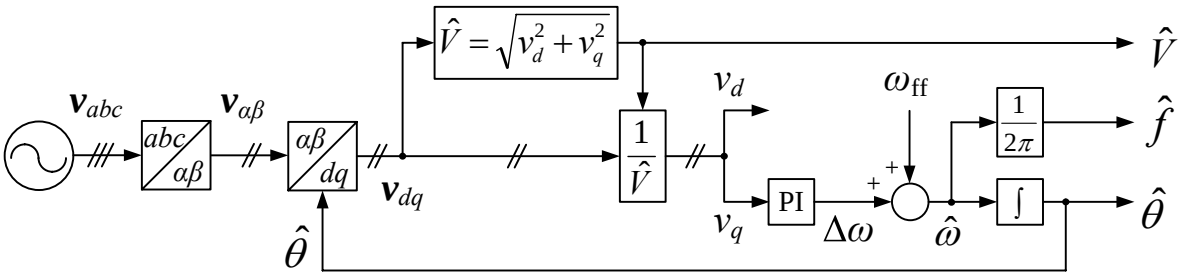


Figure 2.1: Structure diagram of a basic dqPLL for three-phase ac signal detection.

- $\boldsymbol{v}_{abc}$: stationary abc-frame ac signal
- $\boldsymbol{v}_{\alpha\beta}$: stationary $\alpha\beta$-frame ac signal
- $\boldsymbol{v}_{dq}$: synchronous dq-frame ac signal
- v_d: direct component of $\boldsymbol{v}_{dq}$
- v_q: quadrature component of $\boldsymbol{v}_{dq}$
- PI: proportional-integral controller
- $\int$: integrator
- $\Delta\omega$: angular frequency error
- ω_{ff}: feedforward angular frequency
- $\hat{\omega}$: estimated angular frequency
- $\hat{\theta}$: estimated phase angle
- $\hat{f}$: estimated frequency
- $\hat{V}$: estimated magnitude Integrator

shown in Figure 2.1. This is a dqPLL system that takes the three-phase abc-frame voltage signal $\boldsymbol{v}_{abc}$ as the input, and gives the estimated magnitude $\hat{V}$, frequency $\hat{f}$ and phase angle $\hat{\theta}$ as the output. In this system, $\boldsymbol{v}_{abc}$ is first transformed into the stationary $\alpha\beta$-frame as $\boldsymbol{v}_{\alpha\beta}$. Then $\boldsymbol{v}_{\alpha\beta}$ is further transformed into the synchronous dq-frame as $\boldsymbol{v}_{dq}$. Since the angular position of the d-axis is set equal to $\hat{\theta}$, the transformations, as defined by (2.1), results in

$$\boldsymbol{v}_{dq} = V[\cos\delta, \sin\delta]^{\mathrm{T}} \tag{2.4}$$

where dq-frame phase angle $\delta = \theta - \hat{\theta}$ is equal to the phase error between the original and the estimated signals.

In order not to be affected by the voltage magnitude, the dq-frame signal is normalized by the estimated magnitude $\hat{V} = \sqrt{v_d^2 + v_q^2}$. Now the q-axis component v_q, which is usually small, becomes $\sin\delta \approx \delta = \theta - \hat{\theta}$.

When the original $\boldsymbol{v}_{abc}$ is ideally sinusoidal, $\boldsymbol{v}_{dq}$ is a pure dc signal, and the phase error $\delta = \theta - \hat{\theta}$ is dc, too. Therefore, it can be controlled to zero by using a proportional-integral (PI) controller, which has infinite gain at dc frequency. As a result, the estimated phase angle in steady state $\hat{\theta} = \theta$.

By-products of the system include the estimated magnitude $\hat{V}$ and the estimated frequency $\hat{f}$. Note that a feedforward frequency ω_{ff} is added to the control loop to shorten the initialization transients.

The control block diagram of the dqPLL system in Figure 2.1 can be drawn with some simplification as shown in Figure 2.2. It is comprised of three parts—the phase detector (PD), the loop filter (LF) and

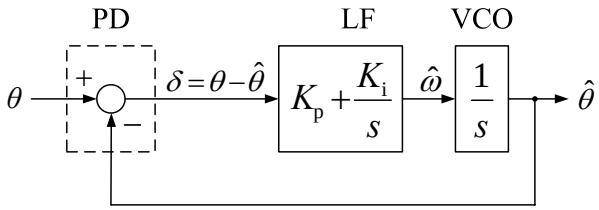


Figure 2.2: Block diagram of the simplified PLL control loop.

- PD: phase detection
- LF: loop filter
- VCO: voltage controlled oscillator
- θ: original phase angle
- $\hat{\theta}$: estimated phase angle
- δ: phase error
- K_p: proportional coefficient
- K_i: integral coefficient
- $\hat{\omega}$: estimated frequency

the so-called voltage-controlled oscillator (VCO). The PD part corresponds to the lump of the abc–$\alpha\beta$ transformation, the $\alpha\beta$–dq transformation and the normalization blocks. The LF part is simply the PI controller, which is essentially a 1st-order LPF. The VCO part was originally implemented by crystal oscillator or LC-tank oscillator in hardware PLL; it has the function of varying the output frequency according to the input dc voltage. For today's software PLL, however, the VCO part is generally implemented as an integrator $1/s$.

Block diagram analysis indicates that the PLL is a 2nd-order system with open-loop transfer function

$$G_0(s) = F(s) \cdot \frac{1}{s} \tag{2.5}$$

where the loop filter $F(s) = K_\mathrm{p} + K_\mathrm{i}/s$ has proportional coefficient K_p and integral coefficient K_i. The closed-loop transfer function

$$G(s) = \frac{\hat{\Theta}(s)}{\Theta(s)} = \frac{G_0(s)}{1 + G_0(s)} = \frac{K_\mathrm{p}s + K_\mathrm{i}}{s^2 + K_\mathrm{p}s + K_\mathrm{i}}. \tag{2.6}$$

Compare it with the general form of the 2nd-order system transfer function

$$G(s) = \frac{2\zeta\omega_\mathrm{n}s + \omega_\mathrm{n}^2}{s^2 + 2\zeta\omega_\mathrm{n}s + \omega_\mathrm{n}^2} \tag{2.7}$$

and it can be derived that $K_\mathrm{i} = \omega_\mathrm{n}^2$, $K_\mathrm{p} = 2\zeta\omega_\mathrm{n}$, where ω_n is the (undamped) natural oscillation frequency, ζ is the damping ratio.

In [33] and [30], it is recommended to use $\zeta = 1/\sqrt{2}$ for best system damping. On the other hand, the

selection of ω_n is associated with the bandwidth frequency ω_b[2]. It usually depends on the requirement on the harmonic attenuation ability of a certain PLL scheme, and its relationship with ω_n can be determined according to the definition of ω_b.

Let $\left|G(\mathrm{j}\omega_\mathrm{b})\right| = 1/\sqrt{2}$ in (2.7), it can be solved that

$$\omega_\mathrm{b} = \omega_\mathrm{n}\sqrt{1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}}. \tag{2.8}$$

Therefore, for $\zeta = 1/\sqrt{2}$, $\omega_\mathrm{b} = \omega_\mathrm{n}\sqrt{2+\sqrt{5}} \approx 2.1\omega_\mathrm{n}$, or $\omega_\mathrm{n} \approx \omega_\mathrm{b}/2.1$. It is a linear relationship once ζ is chosen.

Consider that the 2nd-order system has a settling time around $4/(\zeta\omega_\mathrm{n})$ and $5/(\zeta\omega_\mathrm{n})$, it can be perceived that a higher bandwidth ω_b leads to faster dynamics in ideal situation. On the other hand, however, when the input $\boldsymbol{v}_{abc}$ is nonideal and $\boldsymbol{v}_{dq}$ contains harmonic ripples, ω_b must be lowered to deeper attenuate the harmonics for less steady-state error in the output $\hat{\theta}$. Doing so has a cost of slower PLL dynamics.

In this thesis, the solution to avoid this compromise is to eliminate the harmonics by DSC operation, which is formulated in the dq-frame at first.

2.4 dq-Frame DSC Operation

As already mentioned, when $\boldsymbol{v}_{abc}$ is unbalanced and/or distorted, grid synchronization PLL aims to track its positive-sequence fundamental component $\boldsymbol{v}_{abc}^{+1}$, which is a dc signal $\boldsymbol{v}_{dq}^{0}$ in the dq-frame. Any other component (including the dc offset and the negative-sequence fundamental component) will appear to be a harmonic signal. Moreover, the component originally with order $h+1$ in the abc- and the $\alpha\beta$-frames will become an h-th harmonic $\boldsymbol{v}_{dq}^{h}$ in the dq-frame. Now consider the half-wave symmetry of a sinusoidal harmonic signal, it is possible to eliminate it by summing it with its half-cycle delayed version. If the result is further divided by 2, then such operation does not affect the dc signal $\boldsymbol{v}_{dq}^{0}$ at all.

Inspired by this idea, a time-domain DSC operator can be defined in the dq-frame, which manipulates a voltage signal $v(t)$ as

$$dq\mathrm{DSC}_n\big[v(t)\big] = \frac{1}{2}\big[v(t) + v(t - T/n)\big]. \tag{2.9}$$

Here T is grid fundamental period, n is the "delay factor" and T/n is the "delay time". As long as

[2]Also known as the cut-off frequency.

T is known, n can be calculated to ensure T/n equal to one-half cycle of the harmonic to eliminate. The calculation formula is derived as shown in the sequal.

The application of DSC operator in (2.9) to the d-axis harmonic component $v_d^h(t)$, as expressed in (2.3), yields

$$\begin{aligned} dq\mathrm{DSC}_n\big[v_d^h(t)\big] &= \frac{1}{2}\big[v_d^h(t) + v_d^h(t-T/n)\big] \\ &= \frac{1}{2}\Big[V^h\cos\big(h\omega t+\varphi^h\big) + V^h\cos\big(h\omega(t-T/n)+\varphi^h\big)\Big] \\ &= \frac{V^h}{2}\Big[\cos\big(h\omega t+\varphi^h\big) + \cos\big(h\omega t - h\cdot 2\pi/n+\varphi^h\big)\Big] \\ &= V^h\cos\big(h\omega t+\varphi^h-h\pi/n\big)\cdot\cos(h\pi/n). \end{aligned} \tag{2.10}$$

Similarly, the application to the q-axis component $v_q^h(t)$ yields

$$\begin{aligned} dq\mathrm{DSC}_n\big[v_q^h(t)\big] &= \frac{1}{2}\big[v_q^h(t) + v_q^h\big(t-T/n\big)\big] \\ &= \frac{1}{2}\Big[V^h\sin\big(h\omega t+\varphi^h\big) + V^h\sin\big(h\omega(t-T/n)+\varphi^h\big)\Big] \\ &= \frac{V^h}{2}\Big[\sin\big(h\omega t+\varphi^h\big) + \sin\big(h\omega t - h\cdot 2\pi/n+\varphi^h\big)\Big] \\ &= V^h\sin\big(h\omega t+\varphi^h-h\pi/n\big)\cdot\cos(h\pi/n). \end{aligned} \tag{2.11}$$

Therefore, if define a space vector DSC operator as simultaneous application of the time-domain DSC to both the d- and the q-axis components of space vector $\vec{v}_{dq}^{\,h}(t)$, then such operation yields

$$\begin{aligned} &dq\mathrm{DSC}_n\big[\vec{v}_{dq}^{\,h}(t)\big] = dq\mathrm{DSC}_n\big[v_d^h(t) + \mathrm{j}\,v_q^h(t)\big] \\ &= dq\mathrm{DSC}_n\big[v_d^h(t)\big] + \mathrm{j}\,dq\mathrm{DSC}_n\big[v_q^h(t)\big] \\ &= V^h\Big[\cos\big(h\omega t+\varphi^h-h\pi/n\big) + \mathrm{j}\sin\big(h\omega t+\varphi^h-h\pi/n\big)\Big]\cdot\cos(h\pi/n) \\ &= V^h\mathrm{e}^{\mathrm{j}(h\omega t+\varphi^h-h\pi/n)}\cdot\cos(h\pi/n) = V^h\mathrm{e}^{\mathrm{j}(h\omega t+\varphi^h)}\cdot\cos(h\pi/n)\,\mathrm{e}^{-\mathrm{j}h\pi/n} \\ &= \vec{v}_{dq}^{\,h}(t)\cdot\vec{G}_n^{\,h} \end{aligned} \tag{2.12}$$

where $\vec{G}_n^{\,h}$ is named as the "harmonic gain" of $dq\mathrm{DSC}_n$ operator upon harmonic space vector $\vec{v}_{dq}^{\,h}(t)$. It is a complex number with modulus

$$G_n^h = \big|\vec{G}_n^{\,h}\big| = \cos(h\pi/n) \tag{2.13}$$

and phase angle

$$\phi_n^h = \angle \vec{G}_n^{\,h} = -h\pi/n. \tag{2.14}$$

The two quantities have certain meanings: the time-domain DSC operation scales the magnitude of signal $\boldsymbol{v}_{dq}^h(t)$ by G_n^h, and shifts its phase angle by ϕ_n^h along the ωt-axis, or in other words delays the signal by ϕ_n^h/ω along the t-axis.

It is easy to verify that the gains for positive- and negative-sequence harmonics with the same order are conjugates: $\vec{G}_n^{\,h} = \left[\vec{G}_n^{\,-h}\right]^*$. However, when studying the harmonic elimination ability of DSC, one only needs to consider G_n^h, the modulus of the gain, which is always the same for both harmonics.

From (2.13) it can be seen that the value of G_n^h ranges from 0 to 1. While zero gain corresponds to the situation that the DSC completely eliminates the harmonic, unity gain corresponds to that the harmonic is not scaled. For all the other values between 0 and 1, the harmonic is attenuated yet not eliminated.

Therefore, in order to determine DSC parameters for the elimination of a certain harmonic, let $G_n^h = 0$, and it can be solved from (2.13) that

$$n = \left|\frac{h}{2k \pm 1/2}\right|, \quad k = 1, 2, 3, \ldots \quad h = 0, \pm 1, \pm 2, \ldots, \pm H \tag{2.15}$$

where k is an integer, h is the dq-frame harmonic order. It means that a DSC operator with the solved delay factor n can eliminate the corresponding harmonic signal $\boldsymbol{v}_{dq}^h$.

For example, the abc-frame negative-sequence fundamental component $\boldsymbol{v}_{abc}^{-1}$ becomes a second harmonic $\boldsymbol{v}_{dq}^{2^-}$ in the dq-frame. A solution to (2.15) for $h = -2$ is $n = 4$. Intuitively, $T/4$ is one-half period for this harmonic, and a delay of one-half period followed by summation with the original signal should annihilate it. Such a process is graphically demonstrated by Figure 2.3 (only v_q^{-2} is drawn in the figure, as the illustration for v_d^{-2} is similar).

2.5 Grid Phase Detection CDSC-PLL based on the dq-Frame CDSC Operation

When a single DSC operator is applied to $\boldsymbol{v}_{dq}$ that contains more than one harmonic, all those with h satisfying (2.15) will be eliminated. Other ones will also be attenuated or at least left unchanged, noting

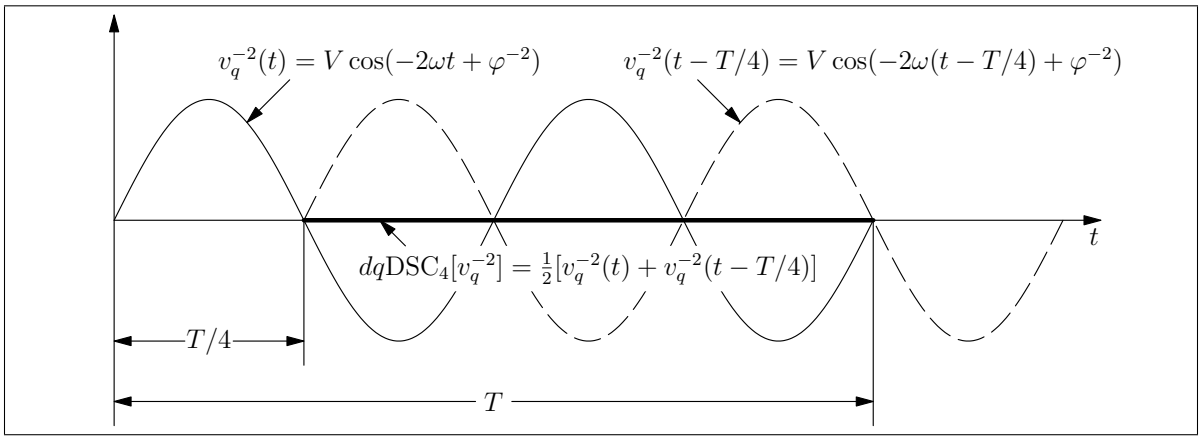


Figure 2.3: Demonstration of the principle that the dq-frame DSC eliminates a selected harmonic in the time domain

that $G_n^h \leq 1$ holds for any h.

Although one DSC operator cannot eliminate every harmonic, it does not alter the frequency of those remaining harmonics. That gives the possibility that the rest harmonics can be further eliminated by other DSC operators. In other words, multiple DSC operators do not interfere with one another during harmonic elimination process, so they can be cascaded (in an arbitrary sequence) to form a cascaded delayed signal cancellation (CDSC) operator [56], which can then be applied to the input signal and eliminate all undesired harmonics step by step.

In analogy to the DSC operator, the harmonic elimination ability of CDSC operator can be characterized by its harmonic gain. For the purpose of generality, assume two DSC operators $dq\text{DSC}_n[\,\cdot\,]$ and $dq\text{DSC}_m[\,\cdot\,]$ are used to construct a CDSC operator $dq\text{CDSC}_{n,m}[\,\cdot\,] = dq\text{DSC}_m\big[dq\text{DSC}_n[\,\cdot\,]\big]$. Its gain can be derived from[3]

$$\begin{aligned} dq\text{CDSC}_{n,m}\big[\vec{v}_{dq}^{\,h}\big] &= dq\text{DSC}_m\Big[dq\text{DSC}_n\big[\vec{v}_{dq}^{\,h}\big]\Big] = dq\text{DSC}_m\big[\vec{v}_{dq}^{\,h}\cdot\vec{G}_n^{\,h}\big] \\ &= dq\text{DSC}_m\big[\vec{v}_{dq}^{\,h}\big]\cdot\vec{G}_n^{\,h} = \vec{v}_{dq}^{\,h}\cdot\vec{G}_m^{\,h}\cdot\vec{G}_n^{\,h} = \vec{v}_{dq}^{\,h}\cdot\vec{G}_{n,m}^{\,h}. \end{aligned} \tag{2.16}$$

Therefore, the "cascaded harmonic gain" $\vec{G}_{n,m}^{\,h} = \vec{G}_m^{\,h}\cdot\vec{G}_n^{\,h}$, i.e. the cascaded gain is the product of the individual gains of the two DSC operators forming the CDSC operator. This conclusion can be easily extended through the same procedure to the case of more than two DSC operators.

In order to systematically find out the required values of the delay factor n to eliminate different harmonics, (2.15) can be iteratively solved for n with $h = \pm1, \pm2, \pm3, \ldots$ and $k = 0, 1, 2, \ldots$ and the

[3]Note that DSC operator has linearity, which can be proven through a process that resembles the derivation of (2.12).

Table 2.2: Selection of dq-frame CDSC parameters to eliminate different harmonics.

n		k											
		0	0	1	1	2	2	3	3	4	4	5	5
$\|h\|$	1	2	2	2/5	2/3	2/9	2/7	2/13	2/11	2/17	2/15	2/21	2/19
	2	4	4	4/5	1 1/3	4/9	4/7	4/13	4/11	4/17	4/15	4/21	4/19
	3	6	6	1 1/5	2	2/3	6/7	6/13	6/11	6/17	2/5	2/7	6/19
	4	8	8	1 3/5	2 2/3	8/9	1 1/7	8/13	8/11	8/17	8/15	8/21	8/19
	5	10	10	2	3 1/3	1 1/9	1 3/7	10/13	10/11	10/17	2/3	10/21	10/19
	6	12	12	2 2/5	4	1 1/3	1 5/7	12/13	1 1/11	12/17	4/5	4/7	12/19
	7	14	14	2 4/5	4 2/3	1 5/9	2	1 1/13	1 3/11	14/17	14/15	2/3	14/19
	8	16	16	3 1/5	5 1/3	1 7/9	2 2/7	1 3/13	1 5/11	16/17	1 1/15	16/21	16/19
	9	18	18	3 3/5	6	2	2 4/7	1 5/13	1 7/11	1 1/17	1 1/5	6/7	18/19
	10	20	20	4	6 2/3	2 2/9	2 6/7	1 7/13	1 9/11	1 3/17	1 1/3	20/21	1 1/19
	11	22	22	4 2/5	7 1/3	2 4/9	3 1/7	1 9/13	2	1 5/17	1 7/15	1 1/21	1 3/19
	12	24	24	4 4/5	8	2 2/3	3 3/7	1 11/13	2 2/11	1 7/17	1 3/5	1 1/7	1 5/19
	13	26	26	5 1/5	8 2/3	2 8/9	3 5/7	2	2 4/11	1 9/17	1 11/15	1 5/21	1 7/19
	14	28	28	5 3/5	9 1/3	3 1/9	4	2 2/13	2 6/11	1 11/17	1 13/15	1 1/3	1 9/19
	15	30	30	6	10	3 1/3	4 2/7	2 4/13	2 8/11	1 13/17	2	1 3/7	1 11/19
	16	32	32	6 2/5	10 2/3	3 5/9	4 4/7	2 6/13	2 10/11	1 15/17	2 2/15	1 11/21	1 13/19
	17	34	34	6 4/5	11 1/3	3 7/9	4 6/7	2 8/13	3 1/11	2	2 4/15	1 13/21	1 15/19
	18	36	36	7 1/5	12	4	5 1/7	2 10/13	3 3/11	2 2/17	2 2/5	1 5/7	1 17/19
	19	38	38	7 3/5	12 2/3	4 2/9	5 3/7	2 12/13	3 5/11	2 4/17	2 8/15	1 17/21	2
	20	40	40	8	13 1/3	4 4/9	5 5/7	3 1/13	3 7/11	2 6/17	2 2/3	1 19/21	2 2/19

solved results are tabulated in Table 2.2. Note that for the same k, the left column corresponds to the values of n with $n = h/(2k + 1/2)$, while the right column corresponds to $n = h/(2k - 1/2)$.

Based on the solved results, three kinds of DSC and CDSC operators (generally referred to as DSC/CDSC operators) are considered here:

1. $dq\text{DSC}_4$. This DSC operator with delay factor $n = 4$ can eliminate all harmonics with $h = \pm 2, \pm 6, \pm 10, \pm 14, \pm 18, \ldots$ in the dq-frame, i.e. $h = -1, +3, -5, +7, -9, +11, -13, +15, -17, +19, \ldots$ in the $\alpha\beta$-frame. In other words, it covers the negative-sequence fundamental component and some odd-order harmonics.

2. $dq\text{CDSC}_{4,6,24}$. This CDSC operator has 3 DSC blocks with delay factors $n = 4, 6, 24$, respectively (the entries in Table 2.2 with light gray background). It can eliminate all harmonics with $h = -1, -2, +4, -5, +7, -8, +10, -11, +13, -14, +16, -17, +19, -20, +22, \ldots$ in the $\alpha\beta$-frame, i.e. all symmetrical harmonics no higher than $h = 22$.

3. $dq\text{CDSC}_{2,4,8,16,32}$. This CDSC operator has 5 DSC blocks with delay factors $n = 2, 4, 8, 16, 32$, respectively (the entries in Table 2.2 with white text). It can eliminate all harmonics with $h = 0, -1, \pm 2, \pm 3, \pm 4, \ldots, \pm 30, \ldots$ in the $\alpha\beta$-frame, i.e. the DC offset, all symmetrical and asymmetrical harmonics up to $h = 30$, and some of the higher-order harmonics. It should be noted the $dq\text{DSC}_{32}$

block can often be omitted and only $dq\text{CDSC}_{2,4,8,16}$ is used. This is to avoid unnecessary detection delay when some high-order harmonics are known to be absent.

To illustrate the harmonic elimination ability of $dq\text{CDSC}_{4,6,24}$ and $dq\text{CDSC}_{2,4,8,16}$ operators in a more intuitive manner, the absolute values of their gains on harmonics from $h = \pm 1$ to $h = \pm 30$ are visualized in Figure 2.4. CDSC gains on symmetrical harmonics are plot in the upper half-plane, while gains on asymmetrical harmonics are plot in the lower half-plane. The visualized results also confirm that $dq\text{CDSC}_{4,6,24}$ can eliminate all the symmetrical harmonics up to $h = 22$, while $dq\text{CDSC}_{2,4,8,16}$ can eliminate most symmetrical as well as asymmetrical harmonics in the plot range.

Although interharmonics are not a major concern in this design, actually they are also attenuated by the two CDSC operators, as their gains are quite small for most non-integer values of h. Besides, if an interharmonic is known to be prominent and is concerned, then an extra DSC operator can be designed in turn to eliminate this interharmonic.

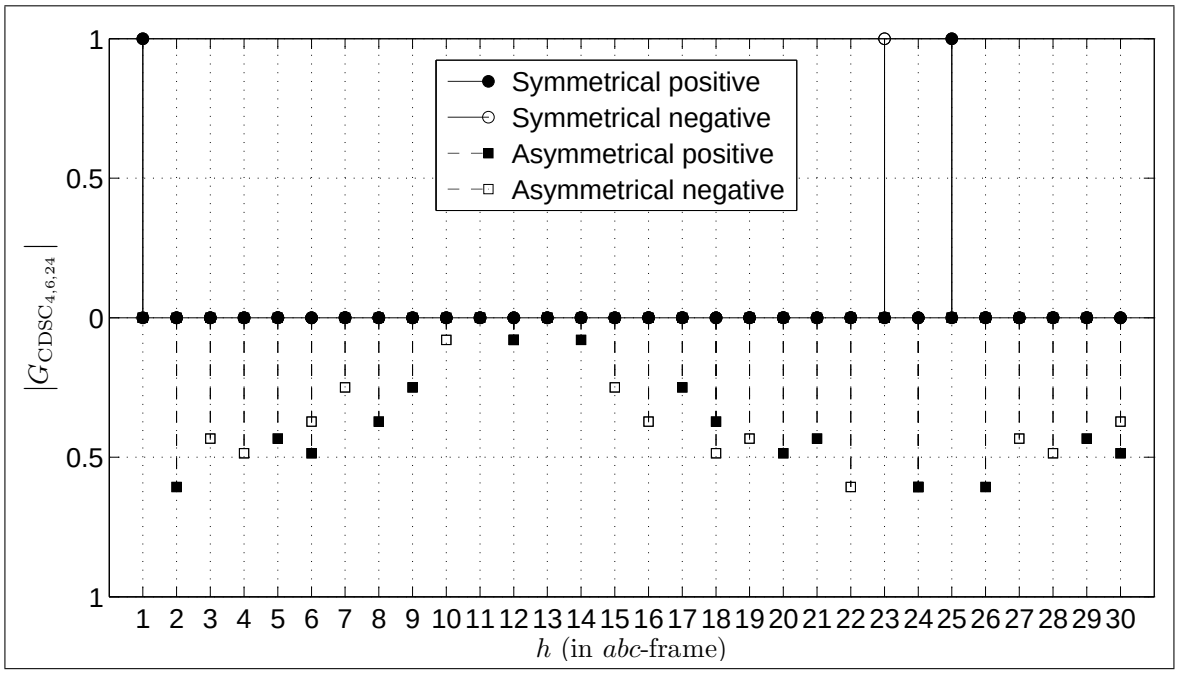
The selection of CDSC operators basically depends on the anticipated harmonic input. Firstly, if the grid voltage is unbalanced yet not distorted, then only the negative-sequence fundamental component exists and $dq\text{DSC}_4$ is good enough to eliminate it. Secondly, if the grid voltage is distorted in a symmetrical manner, then only symmetrical harmonics are present and $dq\text{CDSC}_{4,6,24}$ would be preferrable. Finally, if the distortion pattern is asymmetrical, then $dq\text{CDSC}_{2,4,8,16,32}$ should be used.

The combination of these CDSC operators and the basic PLL system in Figure 2.1 yields the CDSC-PLL system shown in Figure 2.5. In this system, each DSC block performs the operation defined by (2.10) and (2.11). The overall dq-frame CDSC operator eliminates the harmonics contained in the polluted $\boldsymbol{v}_{dq}$ and outputs the "clean" signal for the PLL loop. The number and the parameters of the DSC blocks are problem specific, and hence are generally denoted as $dq\text{DSC}_n$, $dq\text{DSC}_m, \ldots$ in the diagram.

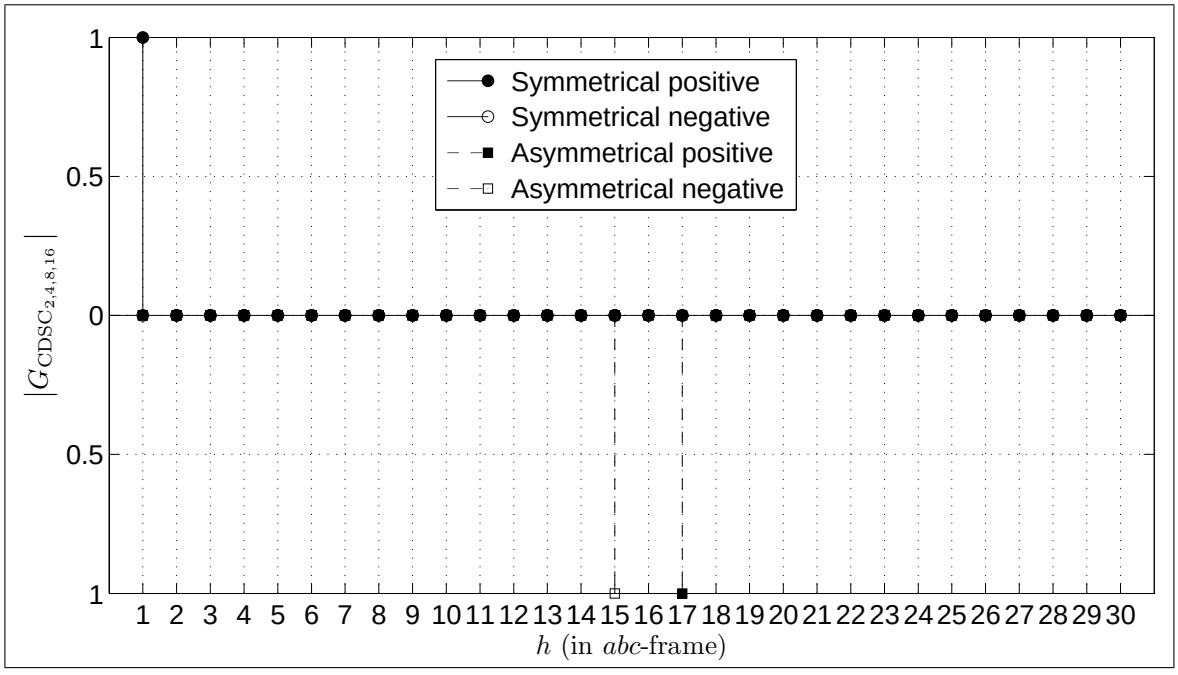
It should be explained that the shown model is an idealized one with all signals, delay buffers and controllers assumed to be continuous. The issues arising from digital discretization in practical implementation of the proposed PLL will be addressed later in Chapter 4.

2.6 $\alpha\beta$-Frame DSC Operation

Ideally, with all undesired harmonics eliminated, the PLL loop bandwidth can be set at a very high value for good system dynamics. As a matter of fact, however, the DSC/CDSC operators in the dq-frame introduce time delay into the control loop, and will complicate PLL tuning [56]. Specifically,



(a)



(b)

Figure 2.4: Gains of two example CDSC operators on symmetrical/asymmetrical and positive-/negative-sequence harmonics. (a) $dq\mathrm{CDSC}_{4,6,24}$ operator. (b) $dq\mathrm{CDSC}_{2,4,8,16}$ operator.

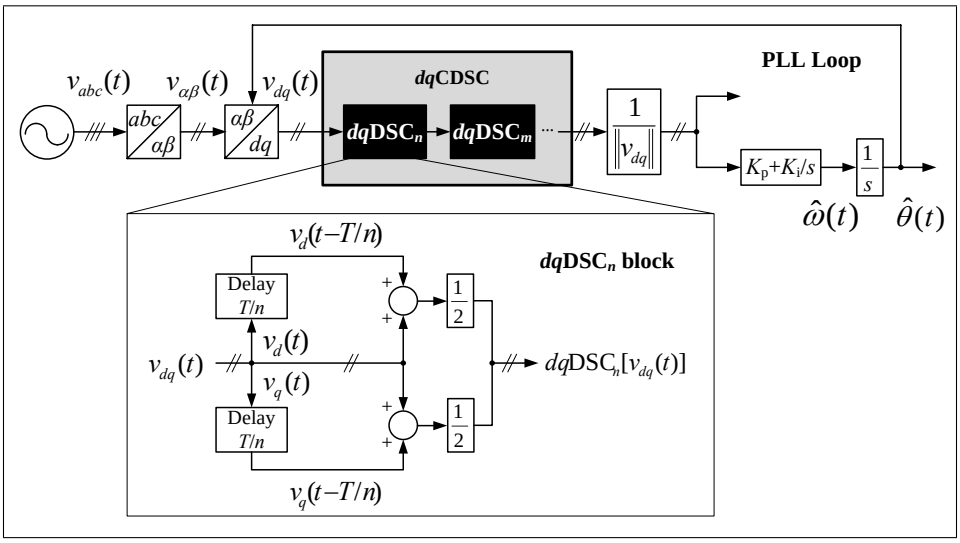


Figure 2.5: Block diagram of the dq-frame DSC/CDSC-PLL system

$dq\text{DSC}_4$ introduces $T/4 = 0.25\ T$ delay. $dq\text{CDSC}_{4,6,24}$ introduces $T/4+T/6+T/24 = 11T/24 \approx 0.46\ T$ delay. $dq\text{CDSC}_{2,4,8,16,32}$ introduces $T/2+T/4+T/8+T/16+T/32 = 31T/32 \approx 0.97\ T$ delay. As shown in Figure 2.5, these delays are located within the PLL loop, so they will adversely affect PLL dynamic performance. This is because the entire control system must take a period much longer than the in-loop delay to stabilize.

This reasoning is confirmed by some simulation results obtained by the researcher: CDSC-PLL system based on $dq\text{CDSC}_{4,6,24}$ uses at least 1.6 T to lock in in response to a phase jump, while CDSC-PLL based on $dq\text{CDSC}_{2,4,8,16}$ uses at least 4.9 T. Any higher loop gain will make the PLL unstable. Similar problems also exist in other PLL systems that involve dq-frame time delay, such as the one in [51] as identified in [54, 55].

Therefore, the DSC/CDSC block must be relocated outside of the loop to ensure PLL stability with high gain. This section presents an avenue for such relocation—the basic idea is to mathematically map the DSC/CDSC operators from the dq-frame into the $\alpha\beta$-frame while the same functionality is maintained.

Naturally, the first step to do so is mapping a single $dq\text{DSC}$ operator into the $\alpha\beta$-frame. As illustrated by Figure 2.6, the polar coordidates of dq-frame harmonic space vector $\vec{v}_{dq}^{\,h}(t)$ can be associated with the corresponding $\alpha\beta$-frame vector $\vec{v}_{\alpha\beta}^{\,h+1}(t)$ through ϑ, the angle difference between the d- and the α-axis. The delayed $\vec{v}_{dq}^{\,h}(t-T/n)$ can also be associated with $\vec{v}_{\alpha\beta}^{\,h+1}(t-T/n)$ through $\vartheta - 2\pi/n$, noting that the

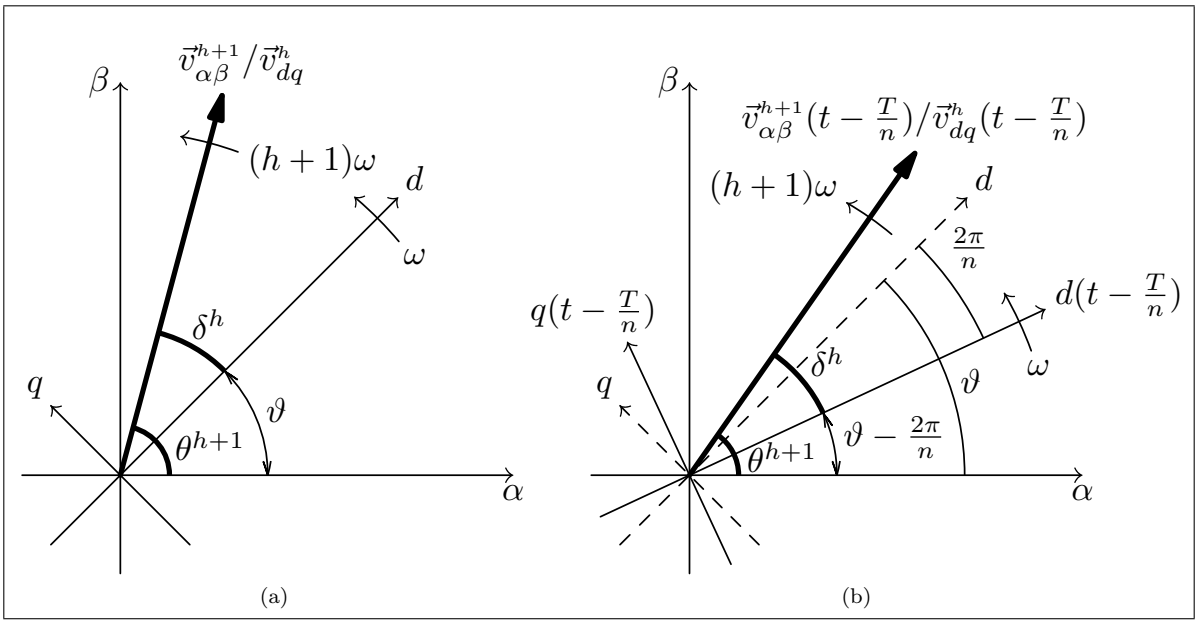


Figure 2.6: Phase relationship between the original and the delayed harmonic space vectors used in the DSC operation. (a) The original vector in the $\alpha\beta$- and dq-frames. (b) The delayed vector in the $\alpha\beta$- and dq-frames.

dq-frame rotates over $2\pi/n$ angle in T/n time:

$$\vec{v}^{\,h}_{dq}(t) = V\mathrm{e}^{\mathrm{j}\delta^h} = V\mathrm{e}^{\mathrm{j}(\theta^{h+1}-\vartheta)} = \mathrm{e}^{-\mathrm{j}\vartheta}\cdot V\mathrm{e}^{\mathrm{j}\theta^{h+1}} = \mathrm{e}^{-\mathrm{j}\vartheta}\cdot\vec{v}^{\,h+1}_{\alpha\beta}(t) \tag{2.17a}$$

$$\vec{v}^{\,h}_{dq}(t-T/n) = \mathrm{e}^{-\mathrm{j}(\vartheta-2\pi/n)}\cdot\vec{v}^{\,h+1}_{\alpha\beta}(t-T/n). \tag{2.17b}$$

Suppose an $\alpha\beta$-frame DSC operator (denoted as $\alpha\beta\mathrm{DSC}_n$) has the same effect on $\alpha\beta$-frame vectors as the aformentioned dq-frame operator $dq\mathrm{DSC}_n$ on the corresponding dq-frame vectors, and consider the fact that a dq-frame vector after dqDSC is still a dq-frame vector, while an $\alpha\beta$-frame vector after $\alpha\beta$DSC is still an $\alpha\beta$-frame vector, there should be

$$dq\mathrm{DSC}_n\big[\vec{v}^{\,h}_{dq}(t)\big] = \mathrm{e}^{-\mathrm{j}\vartheta}\cdot\alpha\beta\mathrm{DSC}_n\big[\vec{v}^{\,h+1}_{\alpha\beta}(t)\big] \tag{2.18a}$$

$$dq\mathrm{DSC}_n\big[\vec{v}^{\,h}_{dq}(t-T/n)\big] = \mathrm{e}^{-\mathrm{j}(\vartheta-2\pi/n)}\cdot\alpha\beta\mathrm{DSC}_n\big[\vec{v}^{\,h+1}_{\alpha\beta}(t-T/n)\big]. \tag{2.18b}$$

Moreover, original time-domain dq-frame DSC operation (2.10) and (2.11) corresponds to space vector

operation (using the expression of dq-frame space vector in Table 2.1)

$$dq\text{DSC}_n\big[\vec{v}_{dq}^{\,h}(t)\big] = \frac{1}{2}\big[\vec{v}_{dq}^{\,h}(t) + \vec{v}_{dq}^{\,h}(t - T/n)\big]. \tag{2.19}$$

Substituting (2.17) and (2.18) into (2.19) yields

$$\alpha\beta\text{DSC}_n\big[\vec{v}_{\alpha\beta}^{\,h+1}(t)\big] = \frac{1}{2}\big[\vec{v}_{\alpha\beta}^{\,h+1}(t) + \mathrm{e}^{\mathrm{j}2\pi/n}\cdot\vec{v}_{\alpha\beta}^{\,h+1}(t - T/n)\big]. \tag{2.20}$$

Or equivalently,

$$\alpha\beta\text{DSC}_n\big[\vec{v}_{\alpha\beta}^{\,h}(t)\big] = \frac{1}{2}\big[\vec{v}_{\alpha\beta}^{\,h}(t) + \mathrm{e}^{\mathrm{j}2\pi/n}\cdot\vec{v}_{\alpha\beta}^{\,h}(t - T/n)\big] \tag{2.21}$$

whose corresponding time-domain operation can be obtained as (using Euler's formula and the expression of $\alpha\beta$-frame space vector in Table 2.1)

$$\alpha\beta\text{DSC}_n\big[\boldsymbol{v}_{\alpha\beta}^{h}(t)\big] = \frac{1}{2}\begin{bmatrix} v_\alpha^h(t) + \cos\left(\frac{2\pi}{n}\right) v_\alpha^h\big(t - T/n\big) - \sin\left(\frac{2\pi}{n}\right) v_\beta^h\big(t - T/n\big) \\ v_\beta^h(t) + \cos\left(\frac{2\pi}{n}\right) v_\beta^h\big(t - T/n\big) + \sin\left(\frac{2\pi}{n}\right) v_\alpha^h\big(t - T/n\big) \end{bmatrix}. \tag{2.22}$$

The derived (2.21) and (2.22) define the general $\alpha\beta$-frame DSC operations for $\alpha\beta$-frame space vectors and time-domain signals, and their harmonic elimination ability can also be characterized by the concept of harmonic gain. With (2.12), (2.17a) and (2.18a), it can be proven that

$$\alpha\beta\text{DSC}_n\big[\vec{v}_{\alpha\beta}^{\,h+1}\big] = \mathrm{e}^{\mathrm{j}\vartheta}\cdot dq\text{DSC}_n\big[\vec{v}_{dq}^{\,h}\big] = \mathrm{e}^{\mathrm{j}\vartheta}\cdot\vec{v}_{dq}^{\,h}\cdot\vec{G}_n^{\,h} = \vec{v}_{\alpha\beta}^{\,h+1}\cdot\vec{G}_n^{\,h}. \tag{2.23}$$

Or equivalently,

$$\alpha\beta\text{DSC}_n\big[\vec{v}_{\alpha\beta}^{\,h}\big] = \vec{v}_{\alpha\beta}^{\,h}\cdot\vec{G}_n^{\,h-1}. \tag{2.24}$$

This can be understood as: the gain that a dq-frame DSC operator has on a dq-frame harmonic signal is the same as the gain the corresponding $\alpha\beta$-frame DSC operator has on the corresponding $\alpha\beta$-frame signal. For example, dq-frame signal $\boldsymbol{v}_{dq}^{-2}$ can be eliminated by $dq\text{DSC}_4$, whose gain is $G_4^{-2} = \cos(-2\pi/4) = 0$. The corresponding $\alpha\beta$-frame signal is $\boldsymbol{v}_{\alpha\beta}^{-1}$, so the corresponding $\alpha\beta\text{DSC}_4$ operator must have the same gain $G_4^{-2} = 0$ upon $\boldsymbol{v}_{\alpha\beta}^{-1}$, and can equally eliminate it in the $\alpha\beta$-frame.

2.7 Grid Phase Detection CDSC-PLL based on the $\alpha\beta$-Frame CDSC Operation

Now that the $\alpha\beta$-frame DSC operator is derived and proven to be funtionally equivalent to the dq-frame DSC, it can also be cascaded to achieve wider harmonic coverage. With (2.16) and (2.24), there should be

$$\alpha\beta\text{CDSC}_{n,m}\left[\vec{v}^{\,h}_{\alpha\beta}\right] = \alpha\beta\text{DSC}_m\left[\alpha\beta\text{DSC}_n\left[\vec{v}^{\,h}_{\alpha\beta}\right]\right] = \vec{v}^{\,h}_{\alpha\beta}\cdot\vec{G}^{\,h-1}_{n,m} \tag{2.25}$$

which suggests that the cascaded harmonic gain of $\alpha\beta$-frame CDSC is also the product of the individual gains of the two $\alpha\beta$-frame DSC operators. Similar to the case of dq-frame CDSC, the conclusion of (2.25) can also be extended to cases with more than two $\alpha\beta$-frame DSC operators.

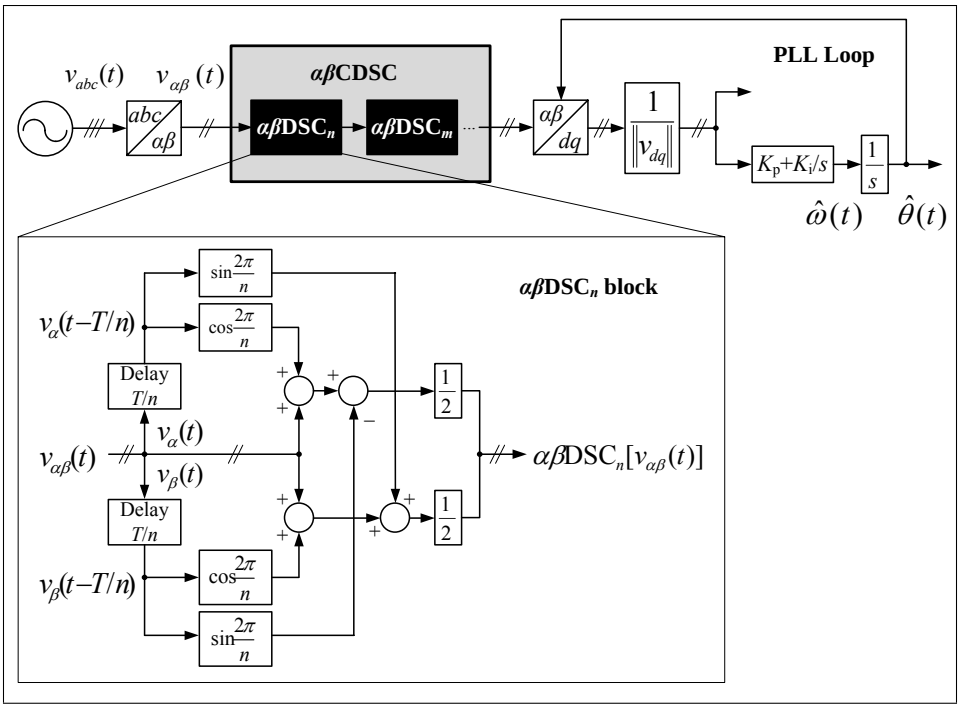


Figure 2.7: Block diagram of the $\alpha\beta$-frame DSC/CDSC-PLL system

Therefore, the $dq\text{DSC}_4$, $dq\text{DSC}_{4,6,24}$ and $dq\text{DSC}_{2,4,8,16,32}$ operators discussed in Section 2.5 can be equivalently replaced by the corresponding $\alpha\beta\text{DSC}_4$, $\alpha\beta\text{DSC}_{4,6,24}$ and $\alpha\beta\text{DSC}_{2,4,8,16,32}$ operators, as defined by (2.22) and (2.25). The DSC/CDSC-PLL system in Figure 2.5 can also be redesigned as the one in Figure 2.7, which has exactly the same harmonic elimination ability. The in-loop delay, however, is no longer present, and so the control loop can maintain stable at very high gain.

2.8 Frequency Adaptability Realized by the Frequency Feedback Loop

Besides harmonic distortion, grid voltage may also experience various frequency variations. In this case, it is no longer accurate to use a constant $T = 1/f$ s in the CDSC block to calculate the delay times. In order to equip the PLL system with frequency adaptability, T must be obtained in real time from the output frequency $\hat{\omega}$. A new control loop—the frequency feedback loop (FFL), is added to the CDSC-PLL system to fulfill such requirement. The modified system is shown in Figure 2.8.

In the diagram, the estimated angular frequency $\hat{\omega}$ is passed through a 1st-order low-pass filter (LPF)

$$F(s) = \frac{\omega_{\mathrm{f}}}{s + \omega_{\mathrm{f}}} \tag{2.26}$$

and divided by 2π to generate the estimated frequency $\hat{f}$. The reciprocal of $\hat{f}$ is the estimated period $\hat{T}$, which is then fedback to the CDSC block to calculate their delay intervals.

Now with the FFL, the PLL comprises two loops with feedback variables as $\hat{\theta}$ and $\hat{T}$. The outer loop of $\hat{T}$ must work slower than the inner loop of $\hat{\theta}$ to maintain stability. This is realized by the LPF placed in the FFL. However, by properly tuning the LPF cut-off frequency ω_{f}, the dynamics of the inner and the outer loops can be optimally matched, as experimentally verified in the test cases in Chapeter 5.

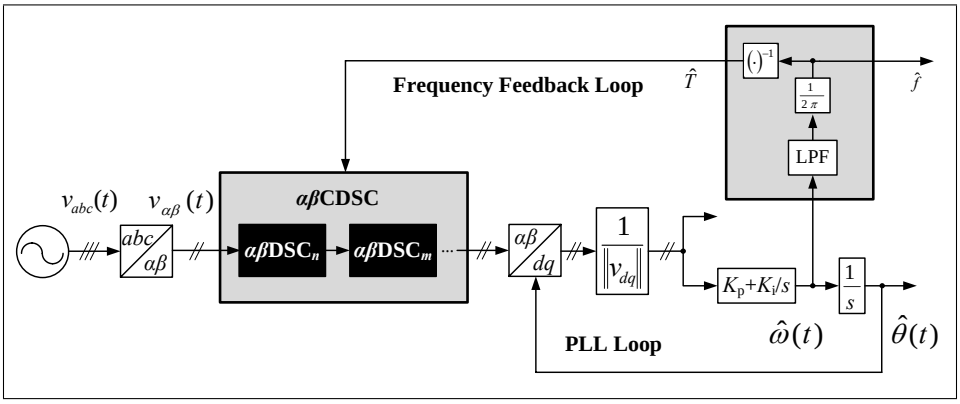


Figure 2.8: Block diagram of the $\alpha\beta$-frame DSC/CDSC-PLL system equipped with FFL for frequency adaptive grid phase detection.

2.9 Summary

This chapter systematically introduces the CDSC-PLL system for grid phase detection. It begins from the representation of grid voltage harmonic signal and the structure and the operating principles of basic PLL system. Through the rigorous and quantitative description, the readers can learn how the grid phase angle is detected through the basic PLL and why its performance is challenged by input harmonics.

To address this challenge, the generalized DSC operator is defined, first in the dq-frame. The operator can be specified to eliminate any harmonic, while the dc signal, i.e. the original positive-sequence fundamental component in the input signal, is intact in DSC process. For the purpose of DSC parameters design, a mathematical tool, namely the harmonic gain, is also established. The dq-frame DSC operator is then extended to the CDSC operator, which contains multiple DSC blocks to cover a wider range of harmonics. Several CDSC configurations are provided; they are also depicted by the tool of cascaded harmonic gain and other visualized approaches.

In order to avoid DSC bringing delay into the PLL loop and complicating system stability, the dq-frame DSC and CDSC operators are then relocated into the $\alpha\beta$-frame through mathematical mapping. The ensuing operators are functionally equivalent in terms of harmonic elimination ability, but their delay times are located outside the PLL loop. Since this limiting factor is removed, the loop can have a very high gain and very short transients while PLL stability is still maintained.

Considerations are also given to frequency variations, which may cause inaccurate DSC operation. A FFL mechanism is design to update the delay intervals in CDSC operator, and so the CDSC-PLL system incorporating the FFL is equipped with frequency adaptability.

Chapter 3

CDSC-PLL for Selective Harmonic Detection

3.1 Introduction

A fast and accurate selective harmonic detection scheme provides the vital information needed by many harmonic compensation systems. This chapter proposes a superior three-phase selective harmonic detection scheme, which is based on the variant of the CDSC-PLL system. However, in order to deal with the more complex task of selective harmonic detection, the PLL system discussed in this chapter has two major renovations.

Firstly, the DSC and CDSC operators are directly derived in the $\alpha\beta$-frame; they are also modified to have more generalized forms. Therefore, they are named as the "renovated" DSC and CDSC operators to distinguish from the "original" ones introduced in Chapter 2. To the contrary, the original DSC and CDSC operators are first derived in the dq-frame and then mapped into the $\alpha\beta$-frame. Such a derivation process guarantees that the original DSC and CDSC operators only eliminate the undesired harmonics and always have unity gain on the positive-sequence fundamental signal. The renovated DSC and CDSC operators, however, can eliminate the positive-sequence fundamental signal as well. Otherwise, the target of harmonic detection can not be achieved. The operators may not have unity gain on the harmonic to detect, either. This proves to be necessary to minimize the computational resources required by the operators, which becomes a major limiting factor when many harmonics are to be detected.

Secondly, while the grid phase detection CDSC-PLL system has only one CDSC operator and one PLL loop, the selective harmonic detection CDSC-PLL system is usually constructed with multiple CDSC operators, multiple PLL loops and some other auxiliary function blocks. The more complex

structure is also at the service of the more demanding task of multiple harmonic detection[1].

The selective harmonic detection CDSC-PLL system has many advantages, such as the very short transient time (settling time less than 0.3 cycles for typical harmonic circumstance) and the small memory overhead (0.67 cycles of signal samples to detect up to the 13th harmonic). The system can achieve zero steady-state error with the undesired harmonics, as well as the fundamental signal, totally eliminated. Besides, the system is insensitive to small frequency variation, and can be designed to handle considerable frequency shift by virtue of the FFL mechanism.

The chapter is organized as follows: Section 3.2 introduces the renovated $\alpha\beta$-frame DSC operator and its effect on harmonic signals. Section 3.3 extends the renovated $\alpha\beta$-frame DSC operator to its cascaded form—the renovated $\alpha\beta$-frame CDSC operator. The section also presents three different approaches to design CDSC parameters. Section 3.4 elaborates the construction of CDSC-PLL system for selective harmonic detection, its computational complexity, and how the system can be tailored for different applications. Section 3.5 discusses the CDSC-PLL system can be equipped with FFL to address the frequency variation problem. Section 3.6 summarizes this chapter.

3.2 Renovated $\alpha\beta$-Frame DSC Operation

Although the proposed detection method can be equally applied to harmonic voltage and current signals, the harmonics analyzed in this chapter are all denoted as voltage signals for simplicity of expression.

Assume a set of three-phase power harmonic signal $\boldsymbol{v}_{abc}$ is fed to the selective harmonic detection block. The signal can be transformed into the $\alpha\beta$-frame with (2.1a). When $\boldsymbol{v}_{abc}$ is unbalanced and/or distorted, the resulted time-domain signal $\boldsymbol{v}_{\alpha\beta}$ is the sum of harmonics: $\boldsymbol{v}_{\alpha\beta} = \sum \boldsymbol{v}^h_{\alpha\beta}$, where h is the harmonic order. Each $\alpha\beta$-frame harmonic signal $\boldsymbol{v}^h_{\alpha\beta}$ can be represented by a space vector $\vec{v}^{\,h}_{\alpha\beta} = V\mathrm{e}^{h\omega t+\varphi}$, where V is the magnitude, ω is fundamental angular frequency, and φ is the initial phase angle. The harmonic space vector rotates at $h\omega$ frequency in the $\alpha\beta$-frame—positive-sequence harmonics ($h > 0$) are rotating counterclockwise, while negative-sequence ($h < 0$) are rotating clockwise.

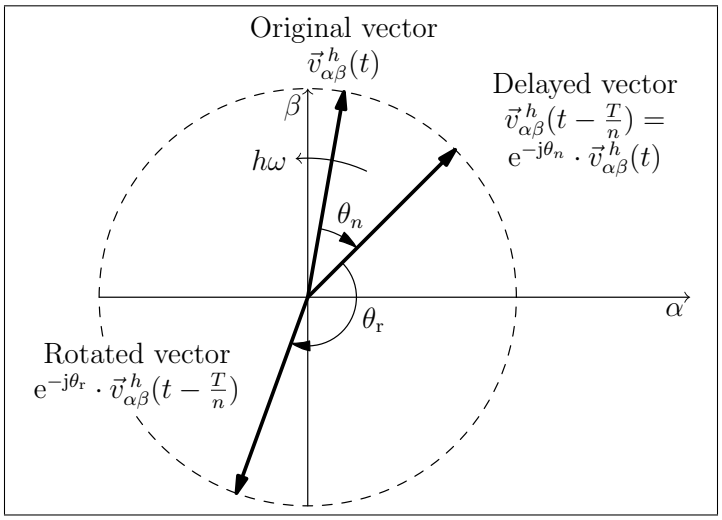


Figure 3.1: Illustration of the harmonic space vectors used by the renovated $\alpha\beta$-frame DSC operation.

3.2.1 Derivation of the renovated $\alpha\beta$-frame DSC operator

Due to the their different rotating frequencies, different harmonic space vectors rotate over different angles in the same portion of time. That is why it is feasible to distinguish them through delay operation. Suppose T/n is the delay time, where T is the fundamental period and n is the delay factor, then $\vec{v}^{\,h}_{\alpha\beta}(t-T/n)$, the h-th harmonic vector delayed by T/n, is lagging the original vector $\vec{v}^{\,h}_{\alpha\beta}(t)$ by angle

$$\theta_n = h\omega \cdot \frac{T}{n} = \frac{2\pi h}{n}. \tag{3.1}$$

Rotating the "delayed vector" with a chosen rotation angle θ_r results in the "rotated vector", as shown in Figure 3.1, and it can now be used together with the "original vector" to construct the renovated $\alpha\beta$-frame space vector DSC operator:

$$\begin{aligned}
\mathrm{DSC}_n\big[\vec{v}^{\,h}_{\alpha\beta}(t)\big] &= \frac{1}{2}\Bigg[\overbrace{\vec{v}^{\,h}_{\alpha\beta}}^{\text{Original vector}} + \underbrace{\mathrm{e}^{-\mathrm{j}\theta_\mathrm{r}} \cdot \overbrace{\vec{v}^{\,h}_{\alpha\beta}\,(t-T/n)}^{\text{Delayed vector}}}_{\text{Rotated vector}}\Bigg] \\
&= \frac{1}{2}\left[\vec{v}^{\,h}_{\alpha\beta} + \mathrm{e}^{-\mathrm{j}\theta_\mathrm{r}} \cdot \mathrm{e}^{-\mathrm{j}\theta_n} \cdot \vec{v}^{\,h}_{\alpha\beta}(t)\right] \\
&= \vec{v}^{\,h}_{\alpha\beta}(t) \cdot \frac{1 + \mathrm{e}^{-\mathrm{j}(\theta_\mathrm{r}+\theta_n)}}{2} \\
&= \vec{v}^{\,h}_{\alpha\beta}(t) \cdot \vec{G}\,.
\end{aligned} \tag{3.2}$$

[1]It should be noted that when many harmonics are present in the input, the number of CDSC operators only needs to match the number of harmonics to detect, and so the design is still more compact than the MSOGI method [66] that requires the number of MSOGI to match the total number of harmonics that exist.

Here the harmonic gain $\vec{G} = \left[1 + \mathrm{e}^{-\mathrm{j}(\theta_\mathrm{r}+\theta_n)}\right]/2 = G \cdot \mathrm{e}^{\mathrm{j}\phi}$ is a complex number with modulus G and phase angle ϕ:

$$\begin{cases} G &= \left|\cos[(\theta_\mathrm{r} + \theta_n)/2]\right| \\ \phi &= -(\theta_\mathrm{r} + \theta_n)/2. \end{cases} \tag{3.3}$$

It is easy to solve that $\theta_\mathrm{r} = -\theta_n$ leads to $G = 1$, while $\theta_\mathrm{r} = \pi - \theta_n$ leads to $G = 0$. Intuitively, the former case implies that the rotated vector is in phase with the original vector, while the latter case implies that they have opposite phase.

3.2.2 Effect of the renovated $\alpha\beta$-frame DSC on harmonic signals

When the renovated DSC operator is applied to input signal $\vec{v}_{\alpha\beta}$ that contains different harmonics, the operator has different effects on them. The delay operation has a uniform delay time T/n, but it causes each harmonic vector to be delayed by a distinctive angle $\theta_n = 2\pi h/n$. Meanwhile, the rotation operation simply rotates all vectors by the same angle θ_r, whose particular value is totally subject to the designer's choice. For example, it can be set as $\theta_\mathrm{r} = -2\pi h^*/n$, where h^* is the "targeted harmonic order". The overall effect of DSC on harmonics can be characterized by its magnitude response (how DSC scales each harmonic magnitude) and phase response (how DSC shifts each harmonic phase angle), as shown in Figure 3.2.

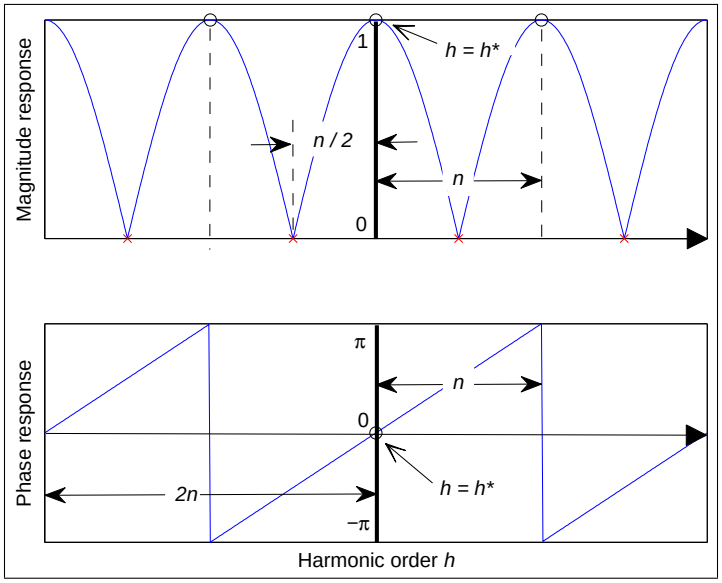


Figure 3.2: Magnitude and phase response of a renovated $\alpha\beta$-frame DSC operator. h^* is the targeted harmonic order. n is the delay factor.

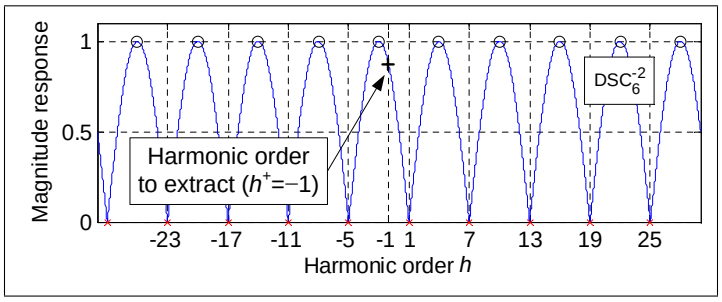


Figure 3.3: Magnitude response of an example renovated DSC operator (DSC_6^{-2}) used to extract the negative-sequence fundamental component. The targeted harmonic order is set at $h^* = -2$ to properly eliminate all typical harmonics and the fundamental component, while the signal to extract ($h^+ = -1$) will be slightly attenuated.

Obviously, DSC has unity gain and zero phase shift at the targeted order $h = h^*$, and zero gain for harmonics $h = h^* - (k + 1/2)n, k = 0, \pm 1, \pm 2, \ldots$ and so eliminate them when they are processed by DSC. All the rest harmonics between the unity gain points and the zero gain points are attenuated but not eliminated. Therefore, by properly selecting parameters h^* and n, a DSC operator can be configured to eliminate, attenuate, or retain an arbitrarily given harmonic.

For example, if the given input signal contains some typical harmonics $h = +1, -1, -5, +7, -11, +13, -17, +19, \ldots$, then in order to extract the negative-sequence fundamental signal $\boldsymbol{v}_{\alpha\beta}^{-1}$, the DSC operator can be designed with parameters $h^* = -2, n = 6$. Denoted as DSC_6^{-2}, this operator has such magnitude response (Figure 3.3) that all harmonics and the positive-sequence fundamental component can be eliminated. Meanwhile, the obtained $\boldsymbol{v}_{\alpha\beta}^{-1}$ signal, which is named as the "harmonic to extract" and its order is denoted as $h^+ = -1$, is scaled by a factor around 0.866, and shifted by a certain angle. Nonetheless, it can be easily corrected later, as detailed in Section 3.4.

The space vector definition in (3.2) can be rewritten into the corresponding time-domain form:

$$\mathrm{DSC}_n\big[\boldsymbol{v}_{\alpha\beta}(t)\big] = \frac{1}{2}\big[\boldsymbol{v}_{\alpha\beta}(t) + \boldsymbol{R}(\theta_\mathrm{r}) \cdot \boldsymbol{v}_{\alpha\beta}\,(t - T/n)\big] \tag{3.4}$$

where the rotation matrix

$$\boldsymbol{R}(\theta_\mathrm{r}) = \begin{bmatrix} \cos\theta_\mathrm{r} & \sin\theta_\mathrm{r} \\ -\sin\theta_\mathrm{r} & \cos\theta_\mathrm{r} \end{bmatrix} \tag{3.5}$$

and the rotation angle

$$\theta_\mathrm{r} = -\frac{2\pi h^*}{n}. \tag{3.6}$$

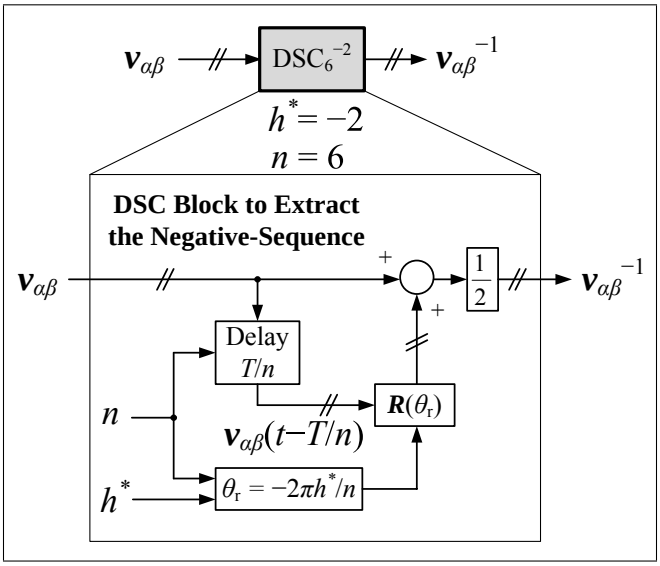


Figure 3.4: Structure diagram of a renovated DSC operator (DSC_6^{-2}) configured to extract the negative-sequence fundamental component.

Now with (3.4), it is easy to obtain the structure diagram of the time-domain renovated DSC operator, as shown in Figure 3.4. For the example of DSC_6^{-2}, the parameters in the figure should be set as $h^* = -2, n = 6$, and therefore θ_r is calculated to be $2\pi/3$. Once the parameters are determined, the whole DSC block only involves signal buffering and arithmetic operations, and no trigonometric functions need to be called.

It is worth mentioning that similar delay-based operators are also studied under the name of the extended DSC [51], the generalized DSC [55], the space vector DFT [52], etc. In the field of digital signal processing, however, the operators are better known as the comb filters [74], which essentially perform finite-impulse response (FIR) filtering on space vectors. The most distinguishing feature of this sort of filters is that they have multiple equiripple lobes in the frequency response, where the maxima (peaks) and the minima (notches) appear periodically.

3.3 Renovated $\alpha\beta$-Frame CDSC Operation

As revealed by Figure 3.2, a single renovated DSC operator cannot eliminate all the harmonics but the one of interest. However, it can be used as a building block, and multiple DSC operators connected in the cascaded form (namely the "renovated CDSC operator") can eliminate all the undesired harmonics step by step, leaving only the harmonic component meant to extract.

With this general idea in mind, the renovated CDSC can be designed through the following three different approaches.

3.3.1 CDSC operator design Approach I

When the input signal contains N_h harmonics, The most straightforward idea of CDSC design is to use $N_\mathrm{h}-1$ DSC blocks to eliminate $N_\mathrm{h}-1$ harmonics and reserve only one harmonic. Name this harmonic as the "harmonic to extract" and denote it as h^+, and name any rest harmonic as a "harmonic to eliminate" and denote it as h^-. Naturally, all DSC blocks should have unity gain at h^+, while each should have zero gain at a unique h^-. Therefore, according to Figure 3.2, the targeted harmonic order and the delay factor of each DSC block should satisfy

$$\begin{cases} h^* &= h^+ \\ n/2 &= |h^+ - h^-|. \end{cases} \tag{3.7}$$

Substitute (3.1) and (3.6) into (3.7) and (3.3), it can be verified that the ensuing DSC has gain

$$\begin{cases} G = \left|\cos[(\theta_\mathrm{r} + \theta_n)/2]\right| = 1 & \text{for } h = h^+ \\ G = \left|\cos[(\theta_\mathrm{r} + \theta_n)/2]\right| = 0 & \text{for } h = h^- \end{cases} \tag{3.8}$$

which meets the expectation from performing the analysis.

When the designed DSC operators are used to build a CDSC operator, the gain of the CDSC operator is the product of the gains of all individual DSC operators, and hence the overall gain must be one at h^+ and zero at any h^-.

3.3.2 CDSC operator design Approach II

The main drawback of design Approach I is the overuse of DSC blocks—every DSC has multiple zero gain points, hence $N_\mathrm{h}-1$ harmonics can actually be eliminated by less than $N-1$ DSC blocks, providing their parameters are properly designed.

Look at Figure 3.2 again: the zero gain points appear periodically and are symmetrically located around h^* point. Therefore, by configuring all DSC blocks with parameters $h^* = h^+$ and $n/2 = 1, 2, 4, 8, \ldots$ a CDSC operator can be ensured to have unity gain at h^+ and zero gain at every other

harmonic order (up to a certain value limited by the number of DSC blocks).

An example resulted from this approach is given in Figure 3.5, where $h^+ = +7$ and five DSC blocks (respectively configured with $h^* = h^+ = +7$ and $n = 2, 4, 8, 16, 32$) can be used to extract it. Denote the formed CDSC operator as CDSC^{+7}, its magnitude response can be determined through (3.3), and it is plot in Figure 3.6. The result confirms that the designed CDSC can eliminate almost all the rest harmonics in the range of $h = -30$ to $+30$ (only except $h = -25$, which is a high-order asymmetrical harmonic and is usually negligible). It also provides very good attenuation to the possible interharmonics and sensing noises.

The defect of this design approach lies in the overall delay time. In the example above, although the number of the DSC blocks used is small, their accumulated delay time reaches $31/32 \approx 0.97$ cycle, which has no obvious advantage over the conventional SDFT method.

However, consider the fact that only some harmonics are likely to be present in power systems, and only a few of them tend to have significant magnitude, the CDSC design approach can be further improved with greatly shortened delay time.

3.3.3 CDSC operator design Approach III

In this approach, multiple DSC blocks are designed to show zero gain only for those undesired harmonics with significant magnitude, and the DSC blocks need not maintain unity gain at h^+—of course, the gain should not be too small. Otherwise, a large amplification factor must be used later to correct the shrunk magnitude of h^+, which in turn would amplify the remained untypical harmonics, interharmonics and noises.

For example, in a typical harmonic scenario $h = +1, -1, -5, +7, -11, +13, -17, +19, \ldots$, if $h^+ = +7$ is to be extracted, then the CDSC only needs to eliminate $h = +1, -1, -5, -11, +13, -17, +19, \ldots$ Solving (3.3) for these harmonic orders yields multiple solutions, and one of them is to use four DSC blocks, respectively configured with parameters $h^* = +7, +7, +7, +23$ and $n = 12, 24, 48, 48$, as demonstrated in Figure 3.7. Its magnitude response (Figure 3.8) indicates that the CDSC can eliminate all the undesired components and greatly attenuate the untypical harmonics, interharmonics and noises, if there are any. This time, however, the total delay is reduced to $1/6 \approx 0.17$ cycle, only one sixth of that of SDFT.

With the new design approach, the harmonic gain of CDSC^{+7} for $h^+ = +7$ becomes around 0.5; the phase shift is no longer zero, either. But both can be corrected easily in the CDSC-PLL system, as detailed in Section 3.4.

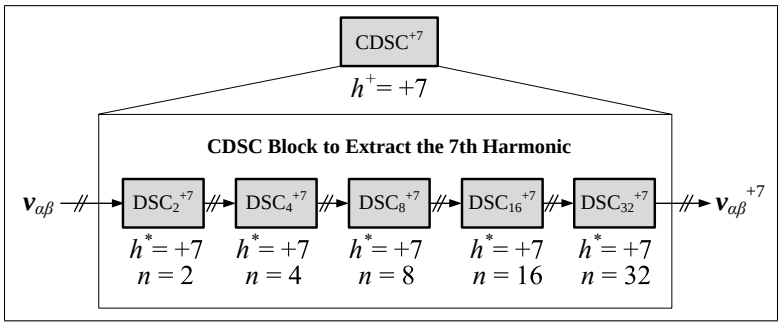


Figure 3.5: Structure diagram of the renovated CDSC operator designed through Approach II.

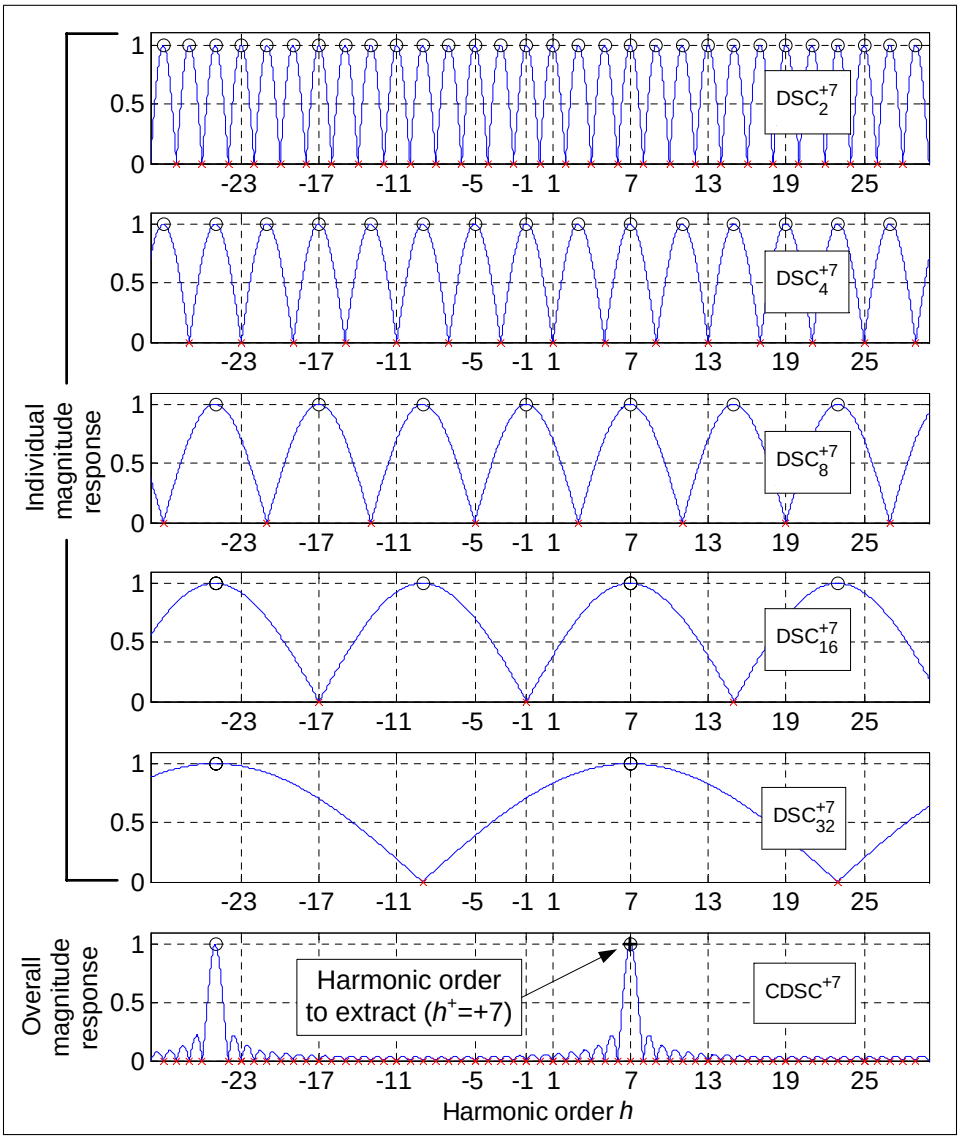


Figure 3.6: Individual and overall magnitude response of the renovated CDSC operator designed through Approach II. Unity gain points are marked by "o". Zero gain points are marked by "x".

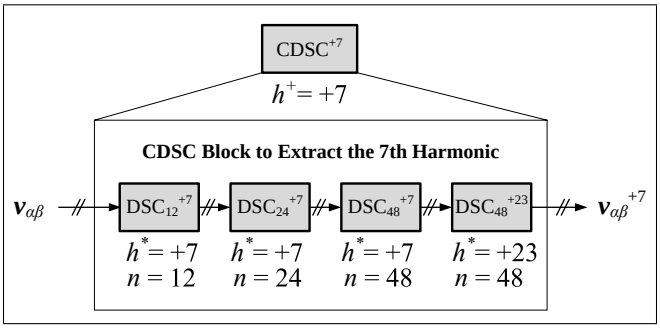


Figure 3.7: Structure diagram of the renovated CDSC operator designed through Approach III.

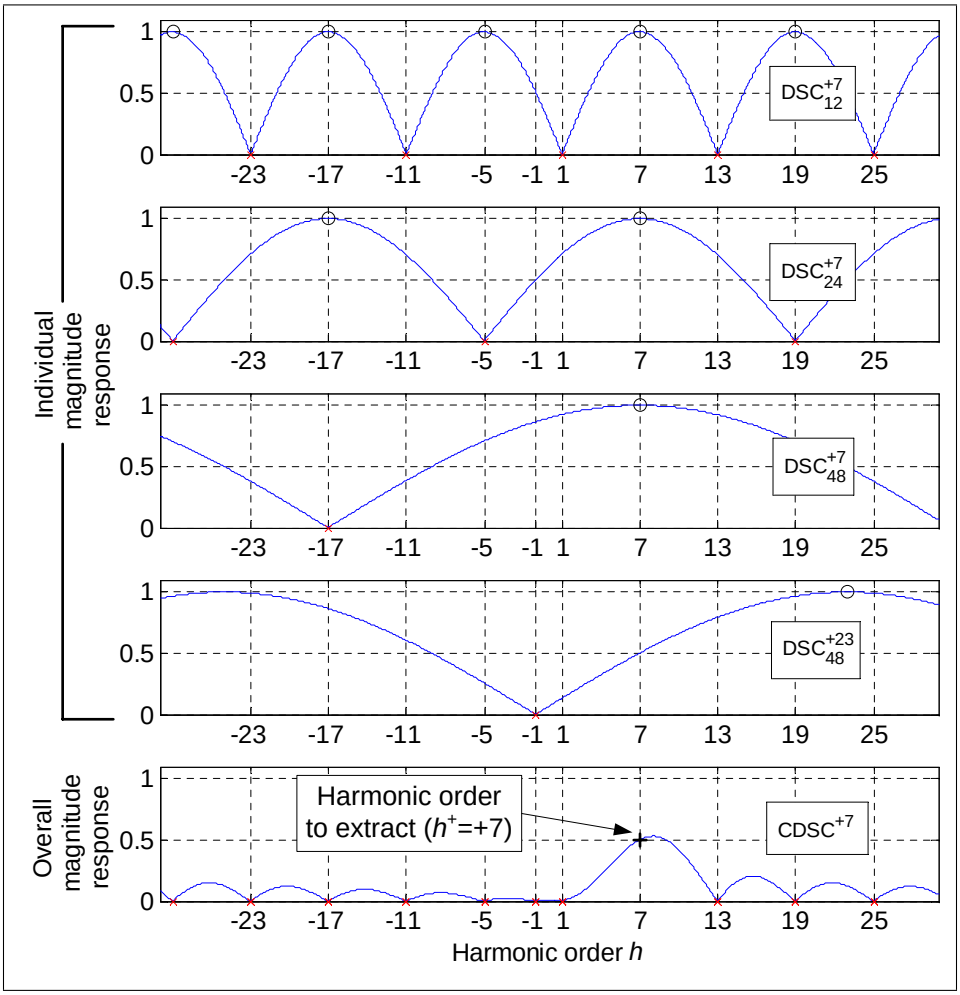


Figure 3.8: Individual and overall magnitude response of the renovated CDSC operator designed through Approach III. Unity gain points are marked by "o". Zero gain points are marked by "x".

3.4 Selective Harmonic Detection CDSC-PLL System based on the Renovated CDSC Operation

The selective harmonic detection CDSC-PLL system is built around the renovated CDSC operator with some peripheral function blocks, such as the *dq*PLL and the Magnitude and Phase Correction block. There are detailed in the following subsections.

3.4.1 Correction of the magnitude and the phase angle

In order to correct the harmonic magnitude and the phase angle scaled and shifted by the CDSC operator, the overall effect of the CDSC operator on the harmonics must be quantified first. Denote the harmonic gain of one DSC operator (with targeted harmonic order h^*) upon harmonic h^+ as $\vec{G}^{\,h^*h^+}$, and denote the overall gain of the CDSC operator upon h^+ as $\vec{G}^{\,h^+}$. Since it is proven in Section 2.7 that the overall gain of CDSC is the product of the individual gains of all constituent DSC blocks, there is

$$\begin{aligned}\vec{G}^{\,h^+} &= \prod_{\text{for all } h^*} \vec{G}^{\,h^*h^+} = \prod_{\text{for all } h^*} G^{h^*h^+} \cdot \mathrm{e}^{\mathrm{j}\phi^{h^*h^+}} \\ &= \prod_{\text{for all } h^*} G^{h^*h^+} \cdot \exp\left(\mathrm{j} \cdot \sum_{\text{for all } h^*} \phi^{h^*h^+}\right) \\ &= G^{h^+} \cdot \mathrm{e}^{\mathrm{j}\phi^{h^+}}.\end{aligned} \tag{3.9}$$

Therefore, the directly detected harmonic space vector $\vec{v}_{\alpha\beta}^{\,h^+}$ should be corrected by such an adjustment factor

$$\vec{A}^{\,h^+} = A^{h^+} \cdot \mathrm{e}^{\mathrm{j}\alpha^{h^+}} = 1/\left(\vec{G}^{\,h^+}\right) \tag{3.10}$$

whose modulus

$$A^{h^+} = 1/\prod_{\text{for all } h^*} G^{h^*h^+} \tag{3.11}$$

and phase angle

$$\alpha^{h^+} = -\sum_{\text{for all } h^*} \phi^{h^*h^+}. \tag{3.12}$$

After harmonic signal $\vec{v}_{\alpha\beta}^{\,h^+}$ is extracted and its magnitude (denoted as $\hat{V}^{h^+}$) and phase angle (denoted as $\hat{\theta}^{h^+}$) are determined, A^{h^+} should be used to multiply $\hat{V}^{h^+}$ to get the correct estimate V^{h^+}, and α^{h^+} should be added to $\hat{\theta}^{h^+}$ to get the correct estimate θ^{h^+}. Such algebraic operation involves neither mass

storage of data nor time delay, and so it is very efficient.

It should be highlighted here that the phase angle of the adjustment factor α^{h^+} can be further modified to account for other phase delays identified in the harmonic compensation system, such as the sampling delay in A/D conversion, the actuation delay of the power converter, etc [65]. That is why the proposed method has the potential of greatly improving the accuracy and flexibility of selective harmonic compensation systems.

3.4.2 Structure of the selective harmonic detection CDSC-PLL

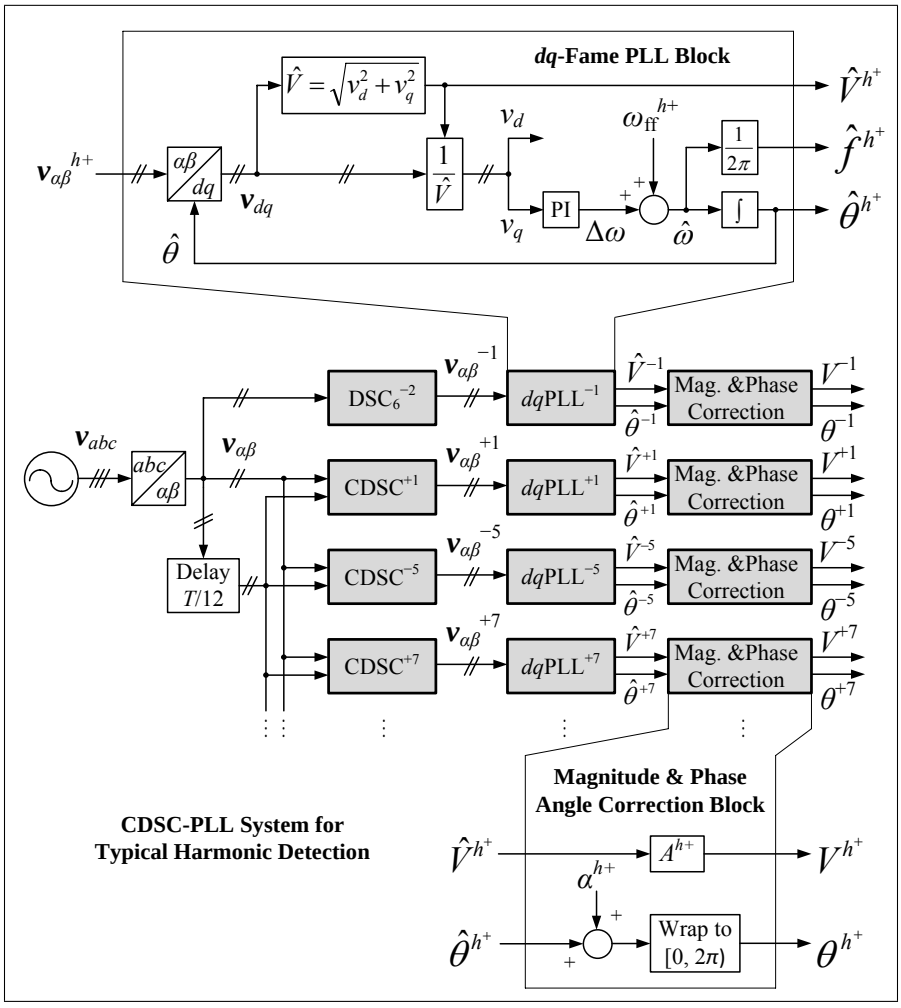


Figure 3.9: Structure diagram of the renovated CDSC operator-based CDSC-PLL system for typical harmonic detection.

Extended from the renovated CDSC operator, a complete selective harmonic detection system CDSC-

PLL system can be created, as illustrated in Figure 3.9. This system takes the sensed three-phase harmonic signal as the input, and gives fundamental and individual harmonic magnitude and phase angle as the output. The system contains several detection subsystems: each subsystem is configured for the detection of one harmonic, and is comprised of three blocks. Their functions are elaborated as follows:

1. DSC/CDSC block. This block "sieves" the input $\alpha\beta$-frame signal, letting through a single component (probably with certain magnitude scaling and phase shift). Moreover, the DSC_6^{-2} block, whose magnitude response is plot in Figure 3.3, extracts the negative-sequence fundamental component. Other CDSC blocks have magnitude responses similar to the one shown in Figure 3.8, though each one has its h^+ set at $+1, -5, +7, \ldots$ instead. Because all CDSC blocks have the same DSC sequence ($\mathrm{DSC}_{12}^{h^+}$, $\mathrm{DSC}_{24}^{h^+}$, $\mathrm{DSC}_{48}^{h^+}$ and DSC_{48}^{+23}), the longest delay buffer of $T/12$ (resting in the $\mathrm{DSC}_{12}^{h^+}$ block) is shared by all the CDSC operators to reduce the overall memory usage.

2. *dq*PLL block. This block detects the magnitude and the phase angle of each extracted harmonic signal. The PI parameters can be designed according to [33, 57]. Since the input signal is not distorted, the bandwidth can be set very high for short transient [30]. The *dq*-frame signal is normalized before feeding into the PI. This is to guarantee the *dq*PLL dynamics are independent from input signal magnitude and are consistent in different working conditions. This also guarantees that all *dq*PLL have the same PI parameters, so the whole system design is much simplified. Each *dq*PLL block's feedforward frequency $\omega_{\mathrm{ff}}^{h^+}$, however, should be set at the corresponding harmonic frequency $h^+\omega$, so as to speed up the initial lock-in process and alleviate the startup transient.

3. Magnitude & Phase Correction block. This block simply corrects the magnitude scaling and the phase shift introduced in DSC/CDSC as explained in Subsection 3.4.1. Detailed values of the adjustment factor can be easily calculated by (3.11) and (3.12), and they are tabulated in Table 3.1 for the example system in Figure 3.9.

3.4.3 Computational complexity of selective harmonic detection CDSC-PLL system

The computational complexity of the presented CDSC-PLL system can be estimated as follows: If the system is designed to detect N_{h} harmonics from the representative scenario $h = +1, -1, -5, +7, -11, +13,$

Table 3.1: Values of the adjustment factor used in the CDSC-PLL system.

Harmonic Order to Extract h^+	Magnitude Adjustment Factor A^{h^+}	Phase Adjustment Factor α^{h^+}
$+1$	7.6613	$82.5°$
-1	1.1547	$-30.0°$
-5	3.8637	$105.0°$
$+7$	2.0000	$60.0°$
-11	1.6427	$127.5°$
$+13$	1.2605	$37.5°$
-17	1.1547	$150.0°$
$+19$	1.0353	$15.0°$

$-17, +19, \ldots$ then the system needs N_h detection subsystems. The overall delay caused by DSC/CDSC blocks is still $T/6$ because of their parallel connection. The overall memory usage of the delay buffers is equal to $(N_\mathrm{h} + 2)/12$ cycle of signal samples, i.e. $T/3$ for detection of $h = +1, -1$, $T/2$ for $h = +1, -1, -5, +7$, $2T/3$ for $h = +1, -1, -5, +7, -11, +13$, etc.

In order to provide a more general reference on the computational complexity of the CDSC-PLL system, the number of algebraic calculations and function calls are counted for the basic DSC block in Figure 3.4, the CDSC block with response in Figure 3.8, and the typical CDSC-PLL system in Figure 3.9 (with 4 detection subsystems). The results are:

1. The basic DSC uses 8 multiplications/divisions and 4 additions/subtractions in every sampling period, plus 2 trigonometric function calls in program initialization.

2. The CDSC has 4 DSC blocks, and hence involves 32 multiplications/divisions and 16 additions/subtractions in every sampling period, plus 8 trigonometric function calls in program initialization.

3. Further considering the *dq*PLL and the Magnitude & Phase Correction blocks, the entire CDSC-PLL system requires 134 multiplications/divisions, 70 additions/subtractions, 2 trigonometric function calls and 1 square root operation in every sampling period. The number of the trigonometric function calls in program initialization is 26.

With such a general reference at hand, the number of computer instructions can be estimated for the execution of the CDSC-PLL system on a specific platform by consulting the hardware manual. It should be pointed out that the CDSC-PLL system is highly scalable, and can often be simplified for a specific application. For example, the number of the detection subsystems can vary according to the harmonics needed to compensate. The DSC/CDSC blocks can be altered to achieve most suitable

harmonic response a certain harmonic pattern anticipated. If no high-order harmonics ($h > 30$) or noises would be encountered, the *dq*PLL block can be replaced by the simple four-quadrant arctangent operation. Finally, if the DSC/CDSC blocks in one detection subsystem has unity gain and zero phase shift on its harmonic to extract, then the associated Magnitude & Phase Correction block can be entirely dropped.

3.5 Frequency Adaptability Realized by the Frequency Feedback Loop

Harmonic distortion may be superposed by grid or supply frequency disturbances, and that threats the normal operation of the harmonic detection CDSC-PLL. Differing from all the resonant filtering-based methods, the renovated DSC/CDSC operators are insensitive to small frequency variations. This can be clearly observed from Figure 3.3, 3.6 and 3.8: in the vicinity of the unity gain points, the gain is still quite close to one, while in the vicinity of the zero gain points, the gain is still close to zero. Since the magnitude response has no abrupt transitions, slight frequency excursion can be tolerated, and fairly accurate harmonic elimination result can be obtained, as verified later by the experiments in Chapter 5.

In the case of a considerable frequency shift, however, it is no longer accurate to assume a constant $T = 1/f$ a priori and use it to calculate the delay times for the DSC/CDSC delay buffers. Instead, T must be estimated in real time.

For this purpose, the FFL proposed in Section 2.8 can be applied again. The new CDSC-PLL system with the FFL is named as CDSC-FFL-PLL in this chapter. Its structure is depicted in Figure 3.10, where the *dq*PLL block with the fundamental input also provides the estimated fundamental frequency $\hat{f}^{+1}$. The FFL conditions this signal with LPF and saturation to get the "detected frequency" f_{det}. Its reciprocal T_{det}, the "detected period", is finally used by all the delay buffers in the DSC/CDSC blocks.

In the FFL subsystem, the saturation block is meant to avoid "division by zero" error during the startup transient of the control loop. It also helps increase system robustness while various disturbances occur. The LPF in the FFL is inserted to properly regulate the control loop dynamics, and here it is also implemented as a 1st-order LPF defined by (2.26).

For the CDSC-PLL system, the stability solely depends on the *dq*PLL, because the DSC/CDSC blocks and the Magnitude & Phase Correction blocks only contain open-loop operations. Furthermore, as analyzed in [33], the stability of *dq*PLL can be guaranteed by properly choosing the PI parameters.

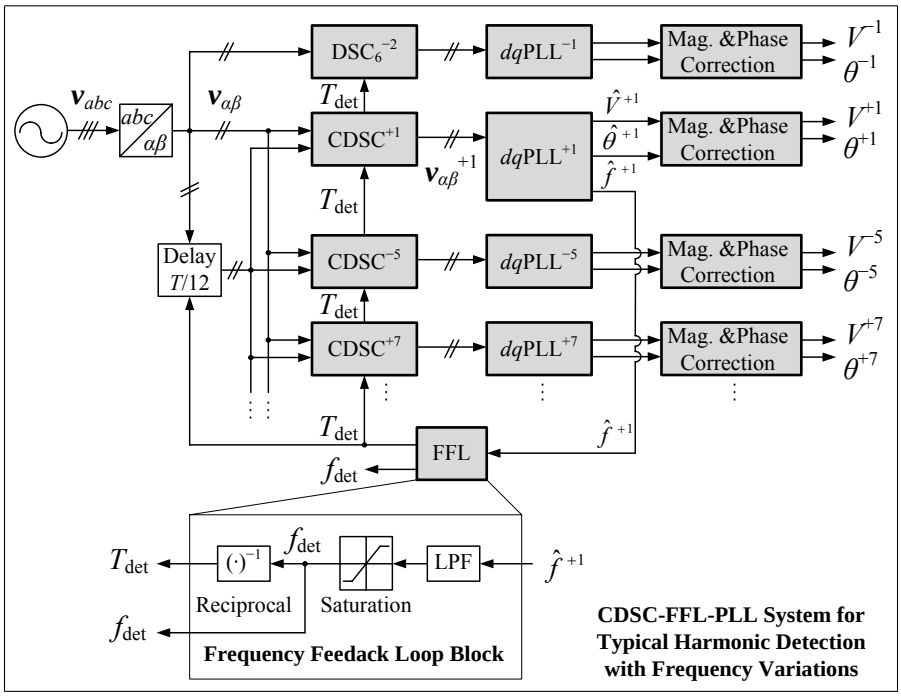


Figure 3.10: Block diagram of the CDSC-FFL-PLL system for frequency adaptive harmonic detection.

In the CDSC-FFL-PLL system, however, the FFL is a highly nonlinear loop, and the LPF cut-off frequency ω_{f} must be carefully chosen to guarantee system stability. While more accurate results can be obtained by studying its averaged dynamics [66], ω_{f} can also be tuned through simulations. The basic principle is to make sure that the outer FFL has slower dynamics than the inner blocks, considering both the signal delay caused by the CDSC blocks and the dqPLL transients. For the CDSC-FFL-PLL system introduced in this chapter, ω_{f} is tuned to around $\omega/3$ for best dynamic performance.

3.6 Summary

This chapter presents a powerful harmonic detection scheme based on the CDSC-PLL system. Different from the CDSC-PLL introduced in Chapter 2, the DSC operators used now have some major renovations: they are completely derived and designed in the $\alpha\beta$-frame. They are also designed to have one more parameter—the targeted harmonic order h^*, in addition to the delay factor n, and so the ensuing renovated DSC/CDSC operators have greater flexibility in terms of their harmonic elimination ability.

The overall structure of the CDSC-PLL system also becomes more complex to address the more demanding task of selective harmonic detection. Multiple detection subsystems are arranged in parallel

to simultaneously detect different harmonics. Each subsystem is designed to have a DSC/CDSC block to extract a harmonic, a dqPLL block to estimate the harmonic magnitude and phase angle, and a Magnitude & Phase Correction block to correct the biases in the estimated quantities.

In spite of the complex structure, the CDSC-PLL system still has very short transient time and small memory overhead. Besides, the system is insensitive to small frequency variations, and can be further equipped with the FFL to address considerable frequency shifts.

Similar to Chapter 2, the CDSC-PLL system in this chapter is also derived in the continuous domain. The discretization process of CDSC-PLL for practical implementation and the associated issues are next discussed in Chapter 4.

Chapter 4

Digital Implementation of the CDSC-PLL System

4.1 Introduction

Chapter 2 and Chapter 3 have discussed the various aspects of grid phase detection and selective harmonic detection CDSC-PLL systems. So far all the discussions are limited to the continuous domain: the input, output and intermediate signals are all assumed to be continuous functions of time. The delay buffers are assumed to be ideal and can be assigned arbitrary delay intervals. And, all the control blocks are described by their s-domain transfer functions.

In practice, however, the CDSC-PLL systems must be discretized for implementation with digital controllers, which are popular in the control of today's power converters. Due to the non-ideal system sampling frequency (and sometimes grid frequency variations), the discretization process is often non-ideal. As a result, the DSC/CDSC operators may subject to discretization error, which subsequently leads to residual distortions in the output.

This chapter provides a thorough analysis on the discretization issues of the CDSC-PLL systems. It is organized as follows: Section 4.2 talks about the discretization of the basic PLL loop. Section 4.3 talks about the discretization of the the original dq-frame DSC and CDSC operators, and proposes a new tool named harmonic gain error to characterize the discretization error of the operators. It also presents an effective error reduction method, which is developed from the linear interpolation theory. Section 4.4

extends the analysis about the original dq-frame DSC and CDSC operators to the $\alpha\beta$-frame, and shows that the error reduction method is also applicable. Section 4.5 deals with the discretization error of the renovated DSC operator, and reformulates the error reduction method for use with it. Section 4.6 summarizes the chapter.

4.2 Discretization of the PLL Loop

The first step is the discretization of the basic PLL illustrated by Figure 2.1. Assume the sampling frequency of the digital system is f_s, and so the sampling period $T_\mathrm{s} = 1/f_\mathrm{s}$. Therefore, the input, output and intermediate signals are sampled and updated at T_s interval during the execution of the control program. To reflect this fact, all the signal denotations in the continuous domain should be modified. For example, the three-phase input voltage signal $\boldsymbol{v}_{abc}$ is no longer a continous function of time $\boldsymbol{v}_{abc}(t)$, but a discrete series of samples $\boldsymbol{v}_{abc}(kT_\mathrm{s})$, where T_s is often dropped and $\boldsymbol{v}_{abc}(k)$ is used for simplicity. Such denotation applies to all the other discrete signals mentioned in this chapter.

The PI block of the PLL is originally implemented as one with continuous transfer function

$$\mathrm{PI}(s) = K_\mathrm{p} + \frac{K_\mathrm{i}}{s}. \tag{4.1}$$

And now the transfer function needs to be transformed into a discrete one. There are different approaches to do this, such Euler's method, the trapezoidal rule, the bilinear transform, the zero-pole matching method, etc [75]. Here the forward Euler's method is simply used to obtain

$$\mathrm{PI}(z) = K_\mathrm{p}\frac{z-\alpha}{z-1} \tag{4.2}$$

where parameter $\alpha = 1 - (K_\mathrm{i}/K_\mathrm{p}) \cdot T_\mathrm{s}$.

Similarly, the original 1st-order integrator $1/s$ in the continuous domain can be discretized through the forward Euler's method as $T_\mathrm{s}/(z-1)$; such discretization results are generally satisfactory for commonly used T_s [75].

The z-domain transfer functions of the PI block and the integrator can now be easily rewritten as difference equations, which can be coded into computer program for the practical execution.

4.3 Discretization Error of the dq-Frame DSC/CDSC Operators and the Error Reduction Method

For the DSC and CDSC operators, the discretization process becomes more complicated, and so the study of the issues must begin from the simplest case—the original dq-frame DSC.

Assume the grid fundamental frequency is f, the fundamental cycle is T, and T contains $N = f_\mathrm{s}/f = T/T_\mathrm{s}$ signal samples. Theoretically, the signal delay of time T/n involved in DSC operation should be realized by buffering $N_n = N/n$ samples in the memory of the digital controller. And in ideal situation, f_s can be chosen to ensure N and N_n are integers.

In practice, however, f_s is usually selected based on many considerations, such as power converter switching loss, the PWM scheme, etc. On the other hand, the grid frequency f may also vary from its nominal value [76], and so deviate f_s/f from the original value. Due to the two reasons, N_n is not an integer in most cases, and is inevitably rounded in the control program, which results in imperfect harmonic elimination process and small residual error in the output of the DSC/CDSC operators [50].

In the following subsections, the rounding operation and the raised discretization error are first analyzed for the dq-frame DSC and CDSC operators. An efficient error reduction method is then developed based on the linear interpolation theory. The improvement brought by the reduction method is finally quantified.

4.3.1 Discretization error during the digital implementation of the dq-frame DSC/CDSC operators

Define the round-down result of N_n as $N_\mathrm{nf} = \mathrm{floor}(N_n)$, and the round-up result as $N_\mathrm{nc} = \mathrm{ceil}(N_n)$. Obviously, $N_\mathrm{nc} - N_\mathrm{nf} = 1$. To avoid repeated expression, use N_nr to represent either N_nf or N_nc, where 'r' refers to "rounded". With this denotation, (2.19) can be discretized into

$$dq\mathrm{DSC}_{n\mathrm{r}}\big[\vec{v}^{\,h}_{dq}(k)\big] = \frac{1}{2}\Big[\vec{v}^{\,h}_{dq}(k) + \vec{v}^{\,h}_{dq}\big(k - N_\mathrm{nr}\big)\Big] \tag{4.3}$$

It corresponds to discrete time-domain operation

$$dq\mathrm{DSC}_{n\mathrm{r}}\big[\boldsymbol{v}^{h}_{dq}(k)\big] = \frac{1}{2}\begin{bmatrix} v^{h}_{d}(k) + v^{h}_{d}\big(k - N_\mathrm{nr}\big) \\ v^{h}_{q}(k) + v^{h}_{q}\big(k - N_\mathrm{nr}\big) \end{bmatrix} \tag{4.4}$$

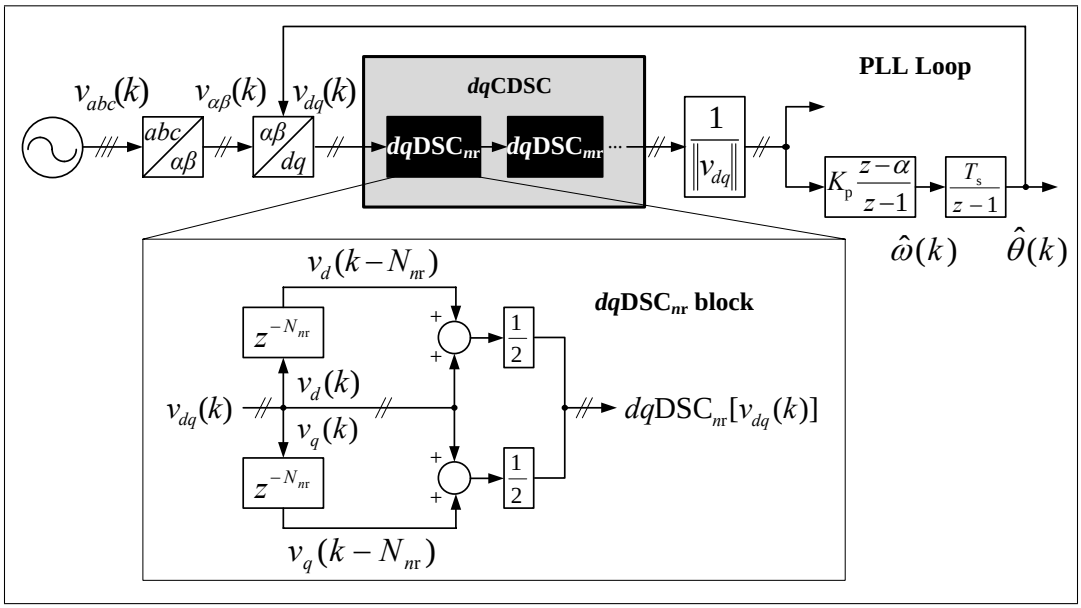


Figure 4.1: Block diagram of the discretized dq-frame DSC/CDSC-PLL system

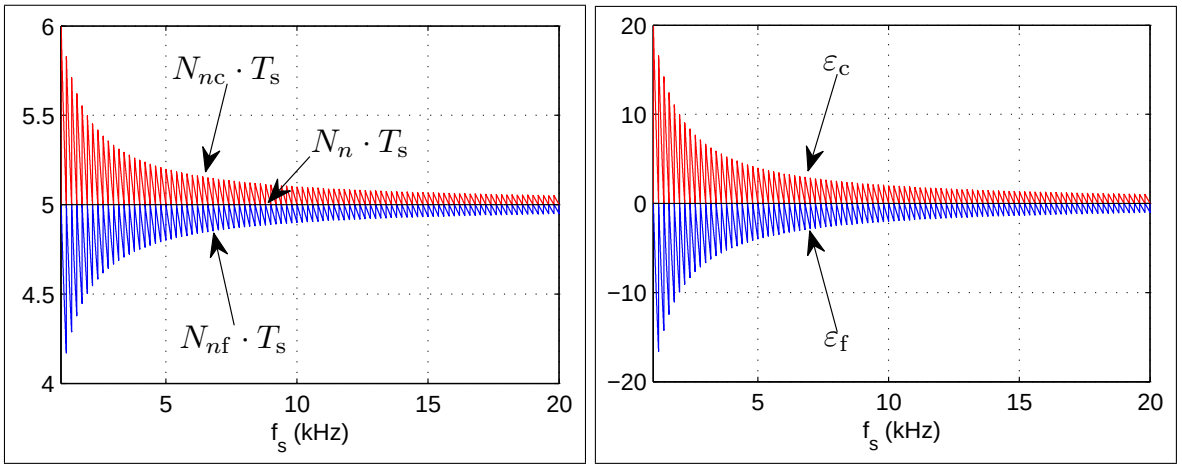
where

$$\boldsymbol{v}_{dq}^{h}(k)=\begin{bmatrix}v_d^h(k)\\ v_q^h(k)\end{bmatrix}=\begin{bmatrix}V\cos\big(h\omega\cdot kT_{\rm s}+\varphi^h\big)\\ V\sin\big(h\omega\cdot kT_{\rm s}+\varphi^h\big)\end{bmatrix}.$$

Based on this discretized dq-frame DSC operator, the dqDSC/CDSC-PLL system in Figure 2.5 can be reformulated as the one in Figure 4.1 for digital implementation.

It can be foreseen in $dq\text{DSC}_{n\text{r}}$, the discretized dq-frame DSC block, that the rounding of N_n causes the practical delay time $N_{n\text{r}}\cdot T_{\rm s}$ to deviate from its ideal value $T/n=NT_{\rm s}/n=(N/n)\cdot T_{\rm s}=N_n\cdot T_{\rm s}$. The extent of deviation can be characterized either by the absolute delay time error $\Delta T_{\rm r}=N_{n\text{r}}\cdot T_{\rm s}-N_n\cdot T_{\rm s}=(N_{n\text{r}}-N_n)\cdot T_{\rm s}$, or by the relative delay error, defined as $\varepsilon_{\rm r}=\Delta T_{\rm r}/(N_n\cdot T_{\rm s})=(N_{n\text{r}}-N_n)/N_n$, i.e. round-down error $\varepsilon_{\rm f}=(N_{n\text{f}}-N_n)/N_n$, round-up error $\varepsilon_{\rm c}=(N_{n\text{c}}-N_n)/N_n$. With this definition, the rounded number of delay samples can be generally written as $N_{n\text{r}}=N_n(1+\varepsilon_{\rm r})$.

To outline the relationship between the absolute and the relative delay time error, they are calculated for such an example: $f=50$ Hz, $T=20$ ms, $n=4$, $T/n=N_n\cdot T_{\rm s}=5$ ms, $f_{\rm s}$ increases from 1 kHz to 20 kHz. The visualized results in Figure 4.2 show that the absolute delay time error is rigorously proportional to the relative error. Nonetheless, the relative error is a better index for general analysis, as it is independent from the actual grid frequency. Therefore, the relative error is adopted in this chapter to make the conclusions applicable to both 50 and 60 Hz power systems.



(a) (b)

Figure 4.2: Illustration of the delay time error and the relative delay error in discretized DSC operation. (a) Ideal and practical delay time (ms). $N_n \cdot T_\mathrm{s}$: ideal delay time. $N_{n\mathrm{f}} \cdot T_\mathrm{s}$ and $N_{n\mathrm{c}} \cdot T_\mathrm{s}$: practical delay time in round-down and round-up at different sampling frequency. (b) Relative delay error (%). ε_f and ε_c: relative delay error calculated for round-down and round-up at different sampling frequency.

Figure 4.2 also shows that the relative delay error ε_r is zero only at some discontinuous f_s points, where f_s happens to make N_n an integer. For other intervals of f_s that are encountered much more frequently than those discontinuous points, the error remains considerable even when f_s is high.

In order to quantify the effect of the discretization error on the harmonic elimination of DSC/CDSC operators, redo the trigonometric manipulation in (2.10), (2.11) and (2.12) for (4.4) and derive (using the definition of $N_{n\mathrm{r}}$ and ε_r)

$$\begin{aligned} dq\mathrm{DSC}_{n\mathrm{r}}\left[\vec{v}_{dq}^{\,h}(k)\right] &= dq\mathrm{DSC}_{n\mathrm{r}}\left[v_d^h(k) + \mathrm{j}\, v_q^h(k)\right] \\ &= dq\mathrm{DSC}_{n\mathrm{r}}\left[v_d^h(k)\right] + \mathrm{j}\, dq\mathrm{DSC}_{n\mathrm{r}}\left[v_q^h(k)\right] \\ &= \vec{v}_{dq}^{\,h}(k) \cdot \cos\left[\frac{h\pi}{n}(1+\varepsilon_\mathrm{r})\right] \mathrm{e}^{-\mathrm{j}\frac{h\pi}{n}(1+\varepsilon_\mathrm{r})} = \vec{v}_{dq}^{\,h}(k) \cdot \vec{G}_{n\mathrm{r}}^{\,h} \end{aligned} \tag{4.5}$$

where $\vec{G}_{n\mathrm{r}}^{\,h} = G_{n\mathrm{r}}^h \cdot \mathrm{e}^{\mathrm{j}\phi_{n\mathrm{r}}^h}$ is the "harmonic gain of the discretized dq-frame DSC operator".

In the original design, the modulus of the harmonic gain of the continuous DSC operator $G_n^h = \cos(h\pi/n)$ must be set at zero for harmonic elimination. So now the modulus of the harmonic gain of the discrete DSC operator $G_{n\mathrm{r}}^h$ becomes

$$G_{n\mathrm{r}}^h = -\sin\left(\frac{h\pi}{n}\varepsilon_\mathrm{r}\right) = \gamma_\mathrm{r}. \tag{4.6}$$

It is no longer equal to zero, and so the harmonic initially intended to be eliminated by this DSC operator will now pass through it, scaled by factor γ_{r}. This factor is named as the "harmonic gain error" in this thesis. For the two cases of round-up and round-down, there is $\gamma_{\mathrm{c}} < 0 < \gamma_{\mathrm{f}}$.

The same analysis can also be extended to the discrete CDSC operator. For generality, it is denoted as $dq\mathrm{CDSC}_{n,m\mathrm{r}}$ in this section. It is easy to derive that the cascaded harmonic gain will become $\vec{G}^{\,h}_{n,m\mathrm{r}} = \vec{G}^{\,h}_{n\mathrm{r}} \cdot \vec{G}^{\,h}_{m\mathrm{r}}$. Its modulus is $G^h_{n,m\mathrm{r}} = G^h_{n\mathrm{r}} \cdot G^h_{m\mathrm{r}}$, and all the terms originally equal to zero are not zero now. Therefore, the overall product is not zero, either. The harmonic originally meant to be eliminated is now only scaled by this small scaling factor, and so certain approach must be utilized to compensate for this effect.

4.3.2 Error reduction by linear interpolation in the dq-frame

Viewed at the time point kT_{s}, if the exact value of signal $\boldsymbol{v}^h_{dq}$ before $N_n \cdot T_{\mathrm{s}}$ time interval, denoted as $\boldsymbol{v}^h_{dq}(k - N_n)$, is available, then (4.4) can be updated into

$$dq\mathrm{DSC}_{n\mathrm{i}}\big[\boldsymbol{v}^h_{dq}(k)\big] = \frac{1}{2}\begin{bmatrix} v^h_d(k) + v^h_d(k - N_n) \\ v^h_q(k) + v^h_q(k - N_n) \end{bmatrix} \tag{4.7}$$

to achieve proper harmonic elimination with the correct harmonic gain. In practice, however, only the signal value before $N_{n\mathrm{f}} \cdot T_{\mathrm{s}}$ and $N_{n\mathrm{c}} \cdot T_{\mathrm{s}}$ delay time, i.e. $\boldsymbol{v}^h_{dq}(k - N_{n\mathrm{f}})$ and $\boldsymbol{v}^h_{dq}(k - N_{n\mathrm{c}})$, are available from the buffered samples. Considering th fact that the time between number $k - N_{n\mathrm{f}}$ and $k - N_{n\mathrm{c}}$ sample points is equal to T_{s}, and is a very short interval, $\boldsymbol{v}^h_{dq}$ within it can be treated as linear to time. Therefore, the values of $\boldsymbol{v}^h_{dq}(k - N_{n\mathrm{f}})$ and $\boldsymbol{v}^h_{dq}(k - N_{n\mathrm{c}})$ can be used to estimate $\boldsymbol{v}^h_{dq}(k - N_n)$ according to the linear interpolation theory:

$$\boldsymbol{v}^h_{dq}(k - N_n) = a_1\, \boldsymbol{v}^h_{dq}(k - N_{n\mathrm{f}}) + a_2\, \boldsymbol{v}^h_{dq}(k - N_{n\mathrm{c}}) \tag{4.8}$$

where the interpolation coefficients

$$\begin{cases} a_1 = (N_{n\mathrm{c}} - N_n)/(N_{n\mathrm{c}} - N_{n\mathrm{f}}) = \varepsilon_{\mathrm{c}} N_n \\ a_2 = 1 - a_1 = -\varepsilon_{\mathrm{f}} N_n \end{cases} \tag{4.9}$$

For this formula, $0 \le a_1, a_2 \le 1$ always holds. In the special case that N_n is an integer, $N_{n\mathrm{f}} = N_n =$

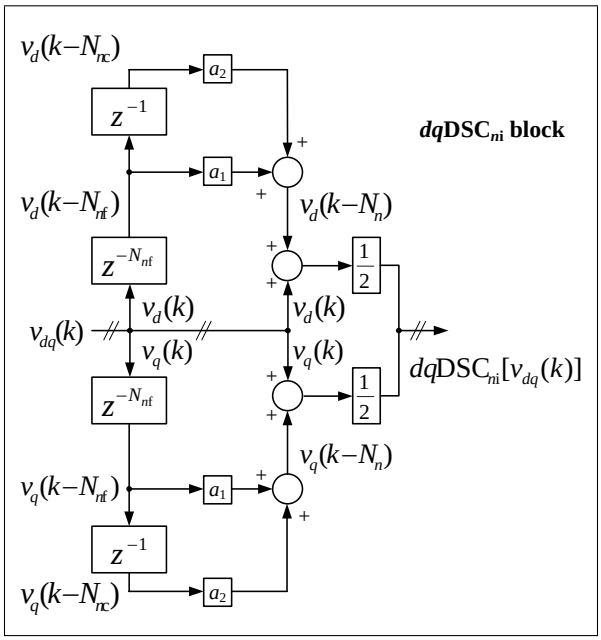


Figure 4.3: Block diagram of the discretized dq-frame DSC operator that incorporates the linear interpolation method

$N_{nc} - 1$, so $a_1 = 1$, $a_2 = 0$, and (4.7) regresses to (4.4).

(4.7), (4.8) and (4.9) defines a new dq-frame DSC operator that incorporates the interpolation method, whose structure is shown in Figure 4.3. It can be denoted as $dq\text{DSC}_{ni}$, where the subscript 'i' refers to "interpolation". If it is substituted for the $dq\text{DSC}_{nr}$ block illustrated in Figure 4.1, then the discretized DSC/CDSC-PLL system is compensated by the interpolation method.

The derived interpolation formula is actually the same as the one in the 2nd-order Lagrange polynomial interpolation. A natural thought is, if more sample points are used for higher-order interpolation, then closer approximation can be achieved. Nonetheless, consider the fact that $T_\text{s} \ll T$, further improvement will be very limited, and cannot counterbalance the increased computational overhead.

The best way to describe the improvement brought by this linear interpolation method is to quantify and visualize it. Rewrite (4.7) into its space vector form, and use (4.8) and (4.9) to obtain

$$dq\text{DSC}_{ni}\big[\vec{v}^{\,h}_{dq}(k)\big] = \frac{1}{2}\Big[\vec{v}^{\,h}_{dq}(k) + \vec{v}^{\,h}_{dq}\big(k - N_n\big)\Big] = \vec{v}^{\,h}_{dq}(k) \cdot \vec{G}^{\,h}_{ni} \tag{4.10}$$

where $\vec{G}^{\,h}_{ni} = G^h_{ni} \cdot \mathrm{e}^{\mathrm{j}\phi^h_{ni}}$ is the harmonic gain of the discrete DSC operator with interpolation. It has

modulus and phase angle

$$G_{ni}^{h} = \frac{1}{2}\sqrt{b^2 + 2b\cos\beta + 1} \tag{4.11a}$$

$$\phi_{ni}^{h} = -\arctan\left(\frac{b\sin\beta}{1 + b\cos\beta}\right) \tag{4.11b}$$

where parameters

$$\begin{cases} b &= \sqrt{b_1^2 + b_2^2} \\ \beta &= \arctan\left(\frac{b_1}{b_2}\right) + \begin{cases} 0, & \text{if } b_2 > 0 \\ \pi, & \text{if } b_2 < 0 \end{cases} \\ b_1 &= a_1 \sin\Big[\frac{2h\pi}{n}\big(1+\varepsilon_{\mathrm{f}}\big)\Big] + a_2 \sin\Big[\frac{2h\pi}{n}\big(1+\varepsilon_{\mathrm{c}}\big)\Big] \\ b_2 &= a_1 \cos\Big[\frac{2h\pi}{n}\big(1+\varepsilon_{\mathrm{f}}\big)\Big] + a_2 \cos\Big[\frac{2h\pi}{n}\big(1+\varepsilon_{\mathrm{c}}\big)\Big]. \end{cases} \tag{4.12}$$

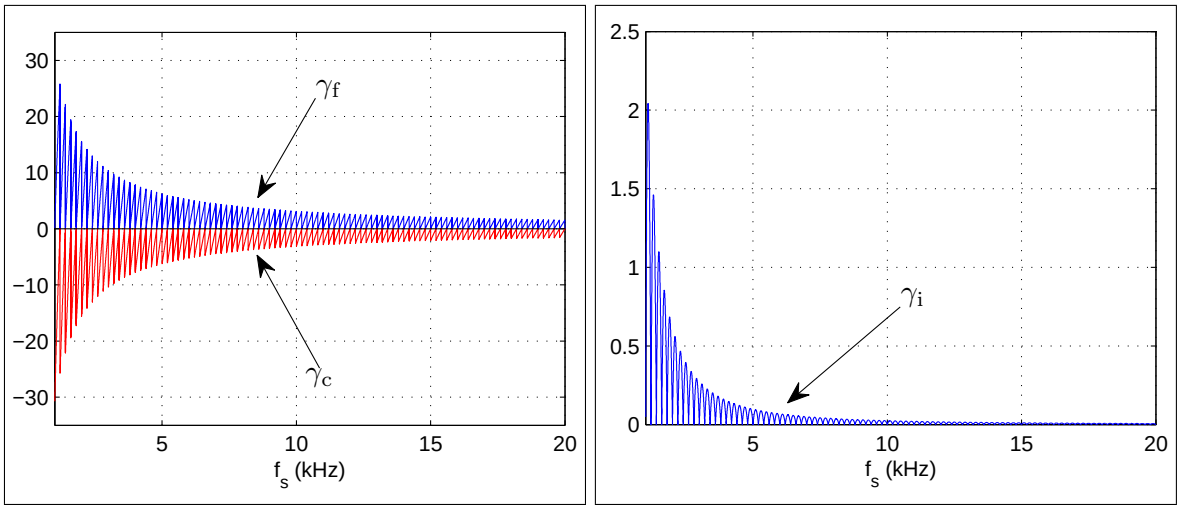
Again, since $G_n^h = \cos(h\pi/n)$ is kept at zero for harmonic elimination in the original design of the continuous DSC, the modulus in (4.11a) will actually be equal to

$$G_{ni}^{h} = \frac{1}{2}\sqrt{b'^2 + 2b'\cos\beta' + 1} = \gamma_{\mathrm{i}} \tag{4.13}$$

where parameters

$$\begin{cases} b' &= \sqrt{b_1'^2 + b_2'^2} \\ \beta' &= \arctan\left(\frac{b_1'}{b_2'}\right) + \begin{cases} 0, & \text{if } b_2' > 0 \\ \pi, & \text{if } b_2' < 0 \end{cases} \\ b_1' &= -a_1 \sin\Big(\frac{2h\pi}{n}\varepsilon_{\mathrm{f}}\Big) - a_2 \sin\Big(\frac{2h\pi}{n}\varepsilon_{\mathrm{c}}\Big) \\ b_2' &= -a_1 \cos\Big(\frac{2h\pi}{n}\varepsilon_{\mathrm{f}}\Big) - a_2 \cos\Big(\frac{2h\pi}{n}\varepsilon_{\mathrm{c}}\Big). \end{cases} \tag{4.14}$$

γ_{i} derived in (4.13) and (4.14) describes the "harmonic gain error" for the discretized DSC operator with interpolation. It can be compared with the original gain error γ_{r} in (4.6) with the aforementioned example: $f = 50$ Hz, $T = 20$ ms, $n = 4$, f_{s} increases from 1 kHz to 20 kHz. The visualized results in Figure 4.4 show that the original gain error, either γ_{f} in round-down or γ_{c} in round-up settings (Figure 4.4a), is nearly proportional to the relative delay error ε_{r} (Figure 4.2b). It is equal to zero only at some discontinuous points of f_{s}, and remains considerable even when f_{s} is high. To the contrary, γ_{i} in Figure 4.4b drastically reduces as f_{s} increases, and quickly falls to less than 0.1% for $f_{\mathrm{s}} > 5$ kHz.



(a) (b)

Figure 4.4: Harmonic gain error in discretized DSC operations with and without interpolation. (a) Error in DSC without interpolation (%). γ_{f} and γ_{c}: error in DSC with round-down and round-up settings. (b) Error in DSC with interpolation (%). γ_{i}: error in DSC with interpolation setting). *Note that the two subplots are in different scales.*

4.4 Discretization Error of the $\alpha\beta$-Frame DSC/CDSC Operators and the Error Reduction Method

In the following subsections, it will be demonstrated how the discrete form of the $\alpha\beta$-frame DSC/CDSC operators can be derived, and how the raised discretization error can be suppressed by the interpolation method likewise, i.e. using the two neighboring signal samples to approximate the accurate sample value.

4.4.1 Discretization error during the digital implementation of the $\alpha\beta$-frame DSC/CDSC operators

Similar to the situation of the dq-frame DSC operator, the discrete $\alpha\beta$-frame operator can be obtained by discretizing (2.22). However, it should be noted that the term $2\pi/n$ (equal to $\omega T/n$) in (2.22) is the angle that the d-axis rotates over in time $T/n = N_n \cdot T_{\mathrm{s}}$, as demonstrated by Figure 2.6b. In VOC, the PLL always aligns the d-axis along the voltage space vector. However, since the voltage signal is discretely sampled, the calculated angular position of the d-axis is also discrete. As a result, the calculated angle that the d-axis rotates over can only be an integer multiple of ωT_{s}. For $N_{n\mathrm{r}}$ delay

samples in this problem, the angle is equal to

$$\omega T_{\mathrm{s}} \cdot N_{n\mathrm{r}} = \omega T_{\mathrm{s}} \cdot N_n(1+\varepsilon_{\mathrm{r}}) = \frac{\omega T_{\mathrm{s}} \cdot N}{n}(1+\varepsilon_{\mathrm{r}}) = \frac{\omega T}{n}(1+\varepsilon_{\mathrm{r}}) = \frac{2\pi}{n}(1+\varepsilon_{\mathrm{r}}). \tag{4.15}$$

Subsequently, after the discretization process (2.21) turns out to be

$$\alpha\beta\mathrm{DSC}_{n\mathrm{r}}\big[\vec{v}^{\,h}_{\alpha\beta}(k)\big] = \frac{1}{2}\Big[\vec{v}^{\,h}_{\alpha\beta}(k) + \mathrm{e}^{\mathrm{j}\frac{2\pi}{n}(1+\varepsilon_{\mathrm{r}})} \cdot \vec{v}^{\,h}_{\alpha\beta}\big(k - N_{n\mathrm{r}}\big)\Big] \tag{4.16}$$

which corresponds to discrete time-domain operation

$$\alpha\beta\mathrm{DSC}_{n\mathrm{r}}\big[\boldsymbol{v}^{h}_{\alpha\beta}(k)\big] = \frac{1}{2}\begin{bmatrix} v^h_\alpha(k) + \cos\left[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{r}})\right] v^h_\alpha\big(k-N_{n\mathrm{r}}\big) - \sin\left[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{r}})\right] v^h_\beta\big(k-N_{n\mathrm{r}}\big) \\ v^h_\beta(k) + \cos\left[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{r}})\right] v^h_\beta\big(k-N_{n\mathrm{r}}\big) + \sin\left[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{r}})\right] v^h_\alpha\big(k-N_{n\mathrm{r}}\big) \end{bmatrix}. \tag{4.17}$$

Based on this discrete $\alpha\beta$-frame DSC operator, the $\alpha\beta$DSC/CDSC-PLL system in Figure 2.7 can be discretized into the one in Figure 4.5 for digital implementation.

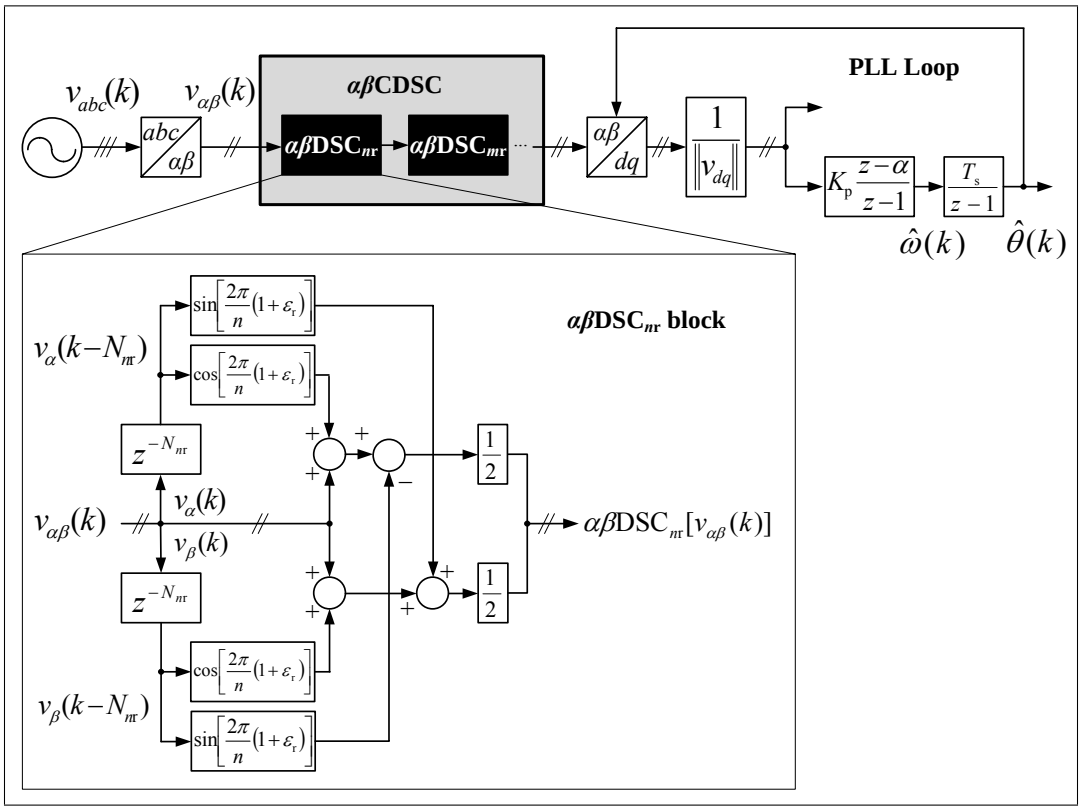


Figure 4.5: Block diagram of the discretized $\alpha\beta$-frame DSC/CDSC-PLL system

4.4.2 Error reduction by linear interpolation in the $\alpha\beta$-frame

Using the similar approach that produces (4.5), it can be obtained from (4.16) that

$$\alpha\beta\mathrm{DSC}_{n\mathrm{r}}\big[\vec{v}^{\,h}_{\alpha\beta}(k)\big] = \vec{v}^{\,h}_{\alpha\beta}(k)\cdot\cos\left[\frac{(h-1)\pi}{n}(1+\varepsilon_{\mathrm{r}})\right]\mathrm{e}^{-\mathrm{j}\frac{(h-1)\pi}{n}(1+\varepsilon_{\mathrm{r}})} = \vec{v}^{\,h}_{\alpha\beta}(k)\cdot\vec{G}^{\,h-1}_{n\mathrm{r}}. \tag{4.18}$$

Again, for the discrete cascaded operator $\alpha\beta\mathrm{CDSC}_{n,m\mathrm{r}}$, the cascaded harmonic gain is $\vec{G}^{\,h-1}_{n,m\mathrm{r}} = \vec{G}^{\,h-1}_{n\mathrm{r}}\cdot\vec{G}^{\,h-1}_{m\mathrm{r}}$. The conclusion about its harmonic elimination ability is the same as that about the dq-frame one $dq\mathrm{CDSC}_{n,m\mathrm{r}}$.

(4.18) and (2.24) can be understood as: the dq- and the corresponding $\alpha\beta$-frame operators have the same gain on a dq- and the corresponding $\alpha\beta$-frame harmonic signal. This is true in both the continuous and the discrete systems. Therefore, they also have the same harmonic gain error γ_{r}.

This conclusion can greatly simplify the derivation of the error reduction method in the $\alpha\beta$-frame, because it implies that the interpolation method proposed for dq-frame DSC operation can be applied to $\alpha\beta$-frame DSC in a similar manner and achieve similar improvement.

The proposed $\alpha\beta$-frame DSC operation in space vector form is (subscript 'i' refers to "interpolation")

$$\alpha\beta\mathrm{DSC}_{n\mathrm{i}}\big[\vec{v}^{\,h}_{\alpha\beta}(k)\big] = \frac{1}{2}\big[\vec{v}^{\,h}_{\alpha\beta}(k) + \mathrm{e}^{\mathrm{j}\frac{2\pi}{n}}\cdot\vec{v}^{\,h}_{\alpha\beta}(k-N_n)\big] \tag{4.19}$$

where the value of signal $\boldsymbol{v}^{h}_{\alpha\beta}$ before $N_n\cdot T_{\mathrm{s}}$ time interval is estimated by linear interpolation

$$\vec{v}^{\,h}_{\alpha\beta}(k-N_n) = a_1\,\mathrm{e}^{\mathrm{j}\frac{2\pi}{n}\varepsilon_{\mathrm{f}}}\cdot\vec{v}^{\,h}_{\alpha\beta}(k-N_{n\mathrm{f}}) + a_2\,\mathrm{e}^{\mathrm{j}\frac{2\pi}{n}\varepsilon_{\mathrm{c}}}\cdot\vec{v}^{\,h}_{\alpha\beta}(k-N_{n\mathrm{c}}). \tag{4.20}$$

The interpolation coefficients a_1 and a_2 are the same as given by (4.9).

By substituting (4.20) and (4.9) into (4.19), the discrete time-domain $\alpha\beta$-frame DSC operation with interpolation can be obtained as

$$\begin{aligned}\alpha\beta\mathrm{DSC}_{n\mathrm{i}}\big[\boldsymbol{v}^{h}_{\alpha\beta}(k)\big] = \frac{1}{2}&\begin{bmatrix} v^{h}_{\alpha}(k) + a_1\cos\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{f}})\big]\cdot v^{h}_{\alpha}\big(k-N_{n\mathrm{f}}\big) + a_2\cos\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{c}})\big]\cdot v^{h}_{\alpha}\big(k-N_{n\mathrm{c}}\big) \\ v^{h}_{\beta}(k) + a_1\cos\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{f}})\big]\cdot v^{h}_{\beta}\big(k-N_{n\mathrm{f}}\big) + a_2\cos\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{c}})\big]\cdot v^{h}_{\beta}\big(k-N_{n\mathrm{c}}\big)\end{bmatrix} \\ +&\begin{bmatrix} a_1\sin\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{f}})\big]\cdot v^{h}_{\beta}\big(k-N_{n\mathrm{f}}\big) - a_2\sin\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{c}})\big]\cdot v^{h}_{\beta}\big(k-N_{n\mathrm{c}}\big) \\ a_1\sin\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{f}})\big]\cdot v^{h}_{\alpha}\big(k-N_{n\mathrm{f}}\big) + a_2\sin\big[\frac{2\pi}{n}(1+\varepsilon_{\mathrm{c}})\big]\cdot v^{h}_{\alpha}\big(k-N_{n\mathrm{c}}\big)\end{bmatrix}.\end{aligned} \tag{4.21}$$

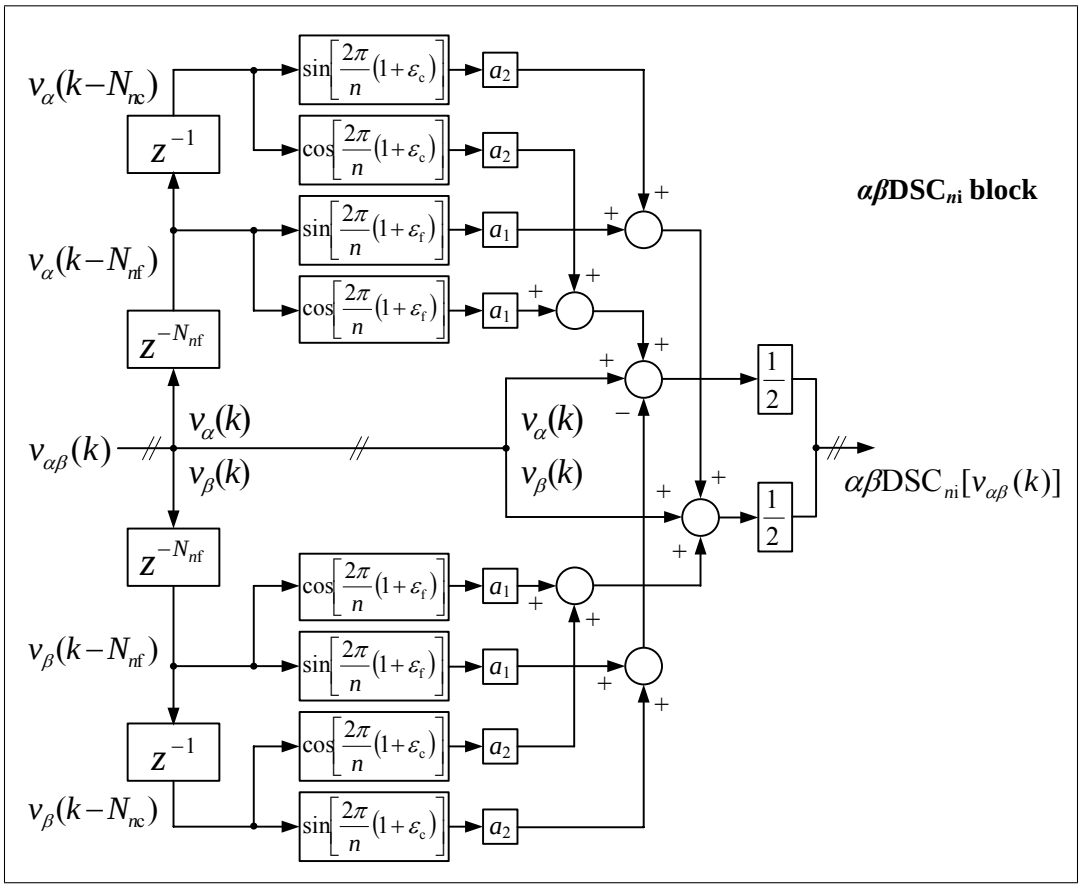


Figure 4.6: Block diagram of the discretized $\alpha\beta$-frame DSC operator that incorporates the linear interpolation method

Based on this formula, the discrete $\alpha\beta$-frame DSC block with interpolation $\alpha\beta\mathrm{DSC}_{n\mathrm{i}}$ can be constructed as shown in Figure 4.6. By substituting it for the $\alpha\beta\mathrm{DSC}_{n\mathrm{r}}$ block in Figure 4.5, the discretized DSC/CDSC-PLL system is equivalently compensated for the discretization error. The improvement can also be quantified by the harmonic gain:

$$\alpha\beta\mathrm{DSC}_{n\mathrm{i}}\left[\vec{v}^{\,h}_{\alpha\beta}(k)\right] = \vec{v}^{\,h}_{\alpha\beta}(k)\cdot\vec{G}^{\,h-1}_{n\mathrm{i}} \tag{4.22}$$

where the gain $\vec{G}^{\,h-1}_{n\mathrm{i}}$, as verified through the same mathematical derivation in (4.10), is exactly the same as given by (4.11) and (4.12).

It should be mentioned that once f_s is decided, all the coefficients in the system in Figure 4.6 are constants and can be coded in the design stage. No sine/cosine functions need to be called during the execution of the DSC/CDSC-PLL program, and so the scheme is very computationally efficient.

Note that the developed error reduction method based on linear interpolation gives formulae similar to the weighted mean value (WMV) method in [50, 76]. However, the method in this work needs less computations, as it requires only one DSC operation for each compensated DSC block, compared to WMV method that requires two (with round-down and round-up settings, respectively). Besides, the derivation by directly interpolating the discrete voltage signal is also more straightforward.

4.5 Discretization Error of the Renovated $\alpha\beta$-Frame DSC Operator and the Error Reduction Method

The selective harmonic detection CDSC-PLL and CDSC-FFL-PLL systems, as introduced in Chapter 3, are also described in the context of continuous systems. When they are practically implemented with digital controllers, they must be discretized as well. The discretization of the PI controllers, the integrators and the LPFs can be easily done with good precision through the approaches mentioned in Section 4.2. On the other hand, the discretization of the renovated DSC/CDSC operatos can also incur certain discretization error and requires compensation for more accurate operation.

Since a detailed explanation has been provided in the previous sections regarding the origin of the discretization error, the descriptive tool of harmonic gain error and the background of the interpolation method, this section simply provides the discrete form of the renovated DSC operator, as well as the derived linear interpolation formula.

Rewritten the expression of the renovated DSC operator in (3.4) into the ideal discrete form:

$$\mathrm{DSC}_n\big[\boldsymbol{v}_{\alpha\beta}(k)\big] = \frac{1}{2}\big[\boldsymbol{v}_{\alpha\beta}(k) + \boldsymbol{R}(\theta_\mathrm{r})\cdot\boldsymbol{v}_{\alpha\beta}(k-N_n)\big] \tag{4.23}$$

where $\boldsymbol{v}_{\alpha\beta}(k)$ is the current signal sample, $\boldsymbol{v}_{\alpha\beta}(k-N_n)$ is the sample delayed by N_n points.

Because N_n is not an integer, it must be either rounded down into $N_{n\mathrm{f}} = \mathrm{floor}(N_n)$, or rounded up into $N_{n\mathrm{c}} = \mathrm{ceil}(N_n)$, and only the sample delayed by $N_{n\mathrm{f}}$ or $N_{n\mathrm{c}}$ points is available from the controller memory. However, the linear interpolation method can be used again, and (4.23) can thus be approximated by

$$\mathrm{DSC}_n\big[\boldsymbol{v}_{\alpha\beta}(k)\big] = \frac{1}{2}\Big[\boldsymbol{v}_{\alpha\beta}(k) + a_1\boldsymbol{R}\big(\theta_\mathrm{r}(1+\varepsilon_\mathrm{f})\big)\cdot\boldsymbol{v}_{\alpha\beta}\big(k-N_{n\mathrm{f}}\big) + a_2\boldsymbol{R}\big(\theta_\mathrm{r}(1+\varepsilon_\mathrm{c})\big)\cdot\boldsymbol{v}_{\alpha\beta}\big(k-N_{n\mathrm{c}}\big)\Big] \tag{4.24}$$

where the relative delay error are same defined as

$$\varepsilon_{\mathrm{f}} = (N_{n\mathrm{f}} - N_n)/N_n, \quad \varepsilon_{\mathrm{c}} = (N_{n\mathrm{c}} - N_n)/N_n \tag{4.25}$$

and the interpolation coefficients are same calculated as

$$a_1 = \varepsilon_{\mathrm{c}} N_n, \quad a_2 = -\varepsilon_{\mathrm{f}} N_n = 1 - a_1. \tag{4.26}$$

This formula looks quite similar to (4.21), but the readers should pay attention to one of its parameters, the rotation angle θ_{r}, as defined in (3.6)—it is different from the $2\pi/n$ used in (4.21).

(4.24) can now be used instead of (3.4) to construct the discrete DSC operators. Based on them, the discrete CDSC operators can be further formed for the implementation of the complete selective harmonic detection CDSC-PLL and CDSC-FFL-PLL systems.

4.6 Summary

The CDSC-PLL systems proposed for grid phase detection and selective harmonic detection must be discretized for digital implementation. This chapter is dedicated to the study of this topic, and it mainly examines the following three aspects:

1. The discretization process and the discrete forms of the function blocks in CDSC-PLL systems. While this job is easier for the control blocks due to the existing control theory, delicate handling is needed in the discretization of the DSC/CDSC delay buffers.

2. The rounding operation required by the discretized DSC/CDSC operators and how it incurs certain discretization error and inaccurate harmonic elimination. The tool of harmonic gain error is used to characterize this effect. The visualized results of an example makes it apparent that the error exists for most sampling frequencies, and simply increasing the sampling frequency only brings very limited improvement.

3. An error reduction method developed from the linear interpolation theory is used in the discretized dq-frame DSC, $\alpha\beta$-frame DSC and the renovated DSC operators. The method is mathematically simple and can efficiently suppress the discretization error, as confirmed by the visualized results.

Chapter 5

Experimental Results

In order to verify the performance of the CDSC-PLL systems used for grid phase detection and selective harmonic detection, many experiments have been conducted across this research program. Experiments have also been conducted to study the rounding effects in the discretized DSC/CDSC operators and the effectiveness of the error reduction method.

The exploratory experiments were initially done on an eZdsp experimental platform, while all of the subsequent experiments transited to a newly available dSPACE platform due to its many advantages in fast control system prototyping and experimental data acquisition. On this experimental platform, both the grid phase detection and the selective harmonic detection CDSC-PLL systems were modeled, and the models were tailored to account for the different CDSC-PLL configurations. An additional model was also built for the discretized $\alpha\beta$- and dq-frame DSC/CDSC operators; it has incorporated round-down, round-up and interpolation settings. For each experimental model, several test cases were designed for different model configurations and working conditions. Abundant results were obtained from them and thoroughly analyzed. The results have confirmed that the proposed CDSC-PLL systems have met the goals of the research project.

This chapter is dedicated to these experiments-related topics: Section 5.1 introduces the dSPACE experimental platform and the detailed workflow with it during the experiments. Section 5.2 depicts the models used in the experiments. Section 5.3–5.5 details the test cases applied to the models, as well as the results obtained from them. The analysis of the experimental results is also dispersed in this section. Section 5.6 summarizes this chapter.

5.1 Experimental Platform

dSPACE refer to a series of model-based control design systems[1]. The dSPACE experimental platform used in this research project is established around a dSPACE DS1103 product. Its hardware setup is shown in Figure 5.1.

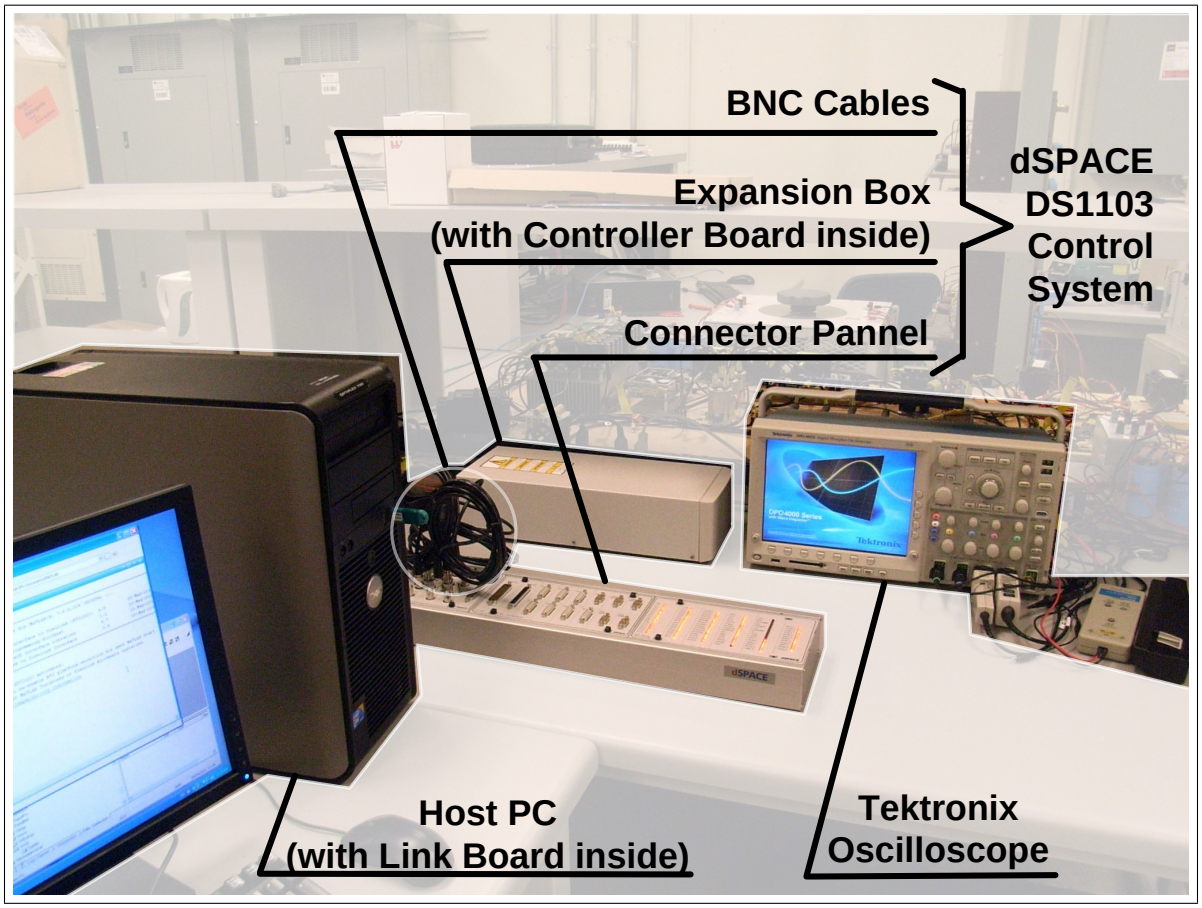


Figure 5.1: Photo of the dSPACE experimental platform, where the different components of the hardware setup are labeled and highlighted from the background.

The hardware in the photo is comprised of the Expansion Box, the Connector Panel, the Link Board[2] and some cables. The Expansion Box hosts the Controller Board—the core of the system, which has an IBM PowerPC 750GX Master DSP, a TI TMS320F240 Slave DSP, some memory devices, I/O chips and other peripheral components mounted on it. The Controller Board is invisible in the figure, but its block diagram is reproduced in Figure 5.2 for illustration purpose.

[1]dSPACE is a registered trademark of dSPACE GmbH, Paderborn, Germany.
[2]The Link Board is installed in the host PC and so is invisible in the figure.

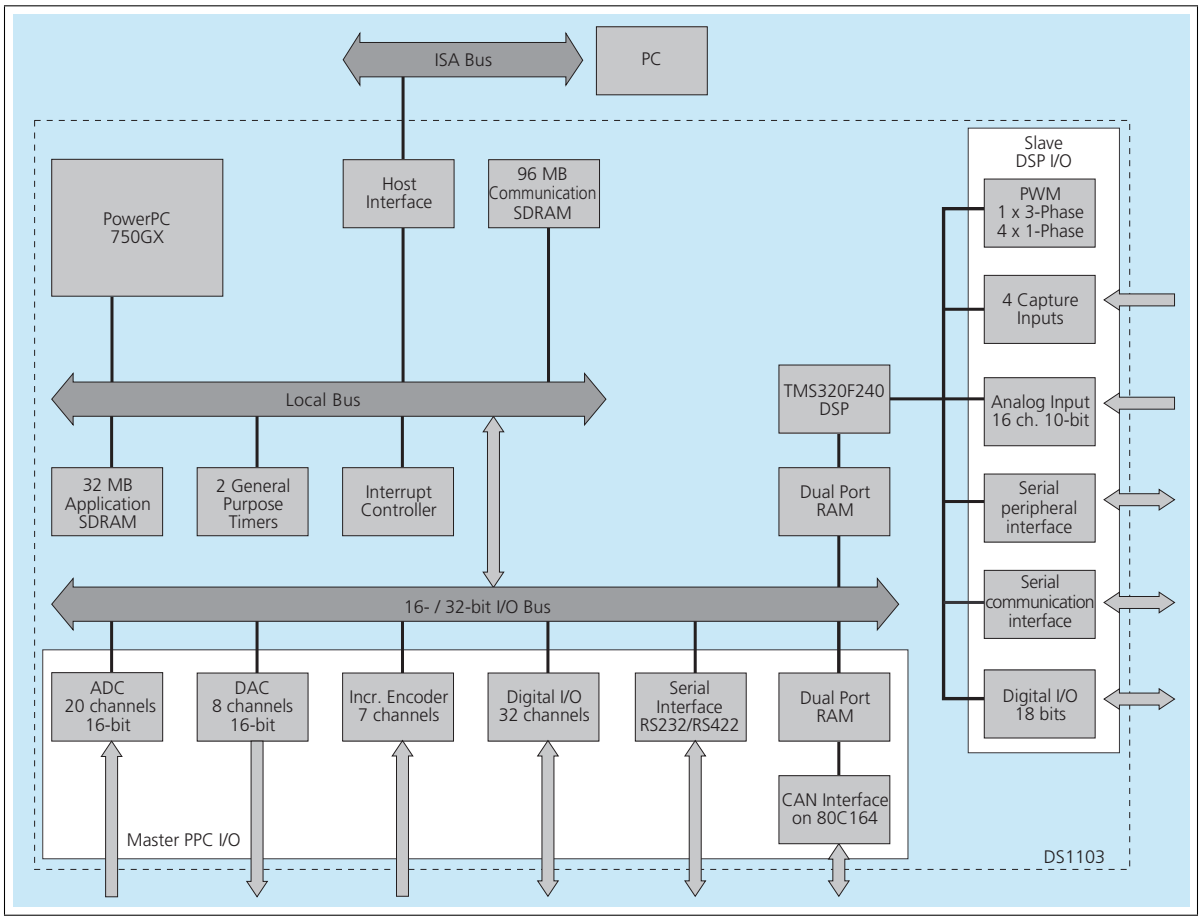


Figure 5.2: Block diagram of dSPACE DS1103 Controller Board (source: *DS1103 PPC Controller Board Product Information*).

Among the other hardware components, the Connector Panel provides I/O ports for external access (such as by the oscilloscope). It also provides LED signals to indicate the internal status. The Link Board serves as the interface between the control system and the host PC. It is installed onto the PC motherboard through an ISA slot and connected to the Expansion Box through an optical fiber cable.

The workflow with the dSPACE experimental platform is closely combined with the model building and the simulation processes in MATLAB/Simulink development environment[3]. It can be divided into the following major steps:

1. Build the MATLAB/Simulink model (`.mdl` file) representing the whole or a part of the CDSC-PLL system from the theoretically derived block diagram.

2. Initialize the operating parameters using a MATLAB M-file (`.m` file). There are multiple groups

[3]MATLAB and Simulink are registered trademarks of Mathworks Inc., Natick, MA, United States.

of parameters to be enabled or disabled, corresponding to different test cases and model settings.

3. Run offline simulation. Test, debug and fine-tune the model until it meets the design prospects.

4. Modify the model for hardware experiment, such as insert dSPACE Real-Time Interface (RTI) blocks to make signals externally accessible, adjust the sampling frequency to match the hardware capability, change the run time from a fixed length to infinite for continuous execution, etc.

5. Compile the model into the executables. The compilation process actually has two steps: a) translate the Simulink model description file (`.mdl` file) and the supporting M-file (`.m` file) into C/C++ language program files (`.c`/`.cpp` and `.h` files), and b) compile and link them into the processor-specific executables (`.sdf`, `.ppc`, `.trc` and `.map` files). However, the whole process is handled by dSPACE TargetLink tool and does not need human interference.

6. Open dSPACE ControlDesk, the software for the centralized management of model execution, data acquisition and the other related tasks. Create an experiment file (`.cdx` file) to accommodate the executables, and create in it one or multiple layer files (`.lay` files) with visual controls for the observation and manipulation of the experimental models.

7. Load the executables into the Controller Board and assign an execution processor[4]. Acquire experimental data through the Capture Settings tool, and save them into MATLAB format data files (`.mat` files) for further use.

The introduced workflow of dSPACE experiments greatly shortens the development cycle, reduces the workload between model building to the practical execution, and eases the observation and acquisition of the experimental data. That is why the dSPACE platform is favored in most of the CDSC-PLL experiments.

Another prominent advantage of dSPACE experiments is that the three-phase grid voltage signal can be generated by a stand-alone Simulink model, which is also running on the Controller Board. The signal is converted into an analog one through the D/A unit in the Connector Panel. Then it is transferred through BNC cables (as highlighted in Figure 5.1) to the A/D unit and sensed as the input for the CDSC-PLL model. This design provides a highly flexible "virtual programmable power supply", which can be used to emulate various input disturbances and offer the most degrees of freedom in experiments. It can also provide internal information (such as the instantaneous fundamental phase

[4]The Master DSP is always used in the presented experiments.

angle) for comparison with the theoretical results. This is a feature that the ordinary ac power supply can never provide.

With this dSPACE experimental platform, numerous models are prototyped and experimented. They are described in Section 5.2.

5.2 Experimental Models

Models have been built for both the virtual programmable power supply and the CDSC-PLL systems. Some of the peer researchers' grid phase detection and selective harmonic detection schemes have also been modeled for comparison. In the research program, a total number of 73 Simulink models and 90 supporting M-files were created, and the following subsections depict the finalized versions of them that are used in the experiments.

5.2.1 Model of the Virtual Programmable Power Supply

The model of the virtual programmable power supply has three-phase output with variable magnitude and frequency. It initially outputs an ideal voltage waveform with nominal magnitude and frequency. Then it is switched to a waveform with certain disturbances, and finally it is switched back to the ideal waveform. The duration of each waveform can be arbitrarily specified. The disturbances that can be imposed onto the waveform include voltage unbalance, voltage sags/swells with phase jump, harmonics and frequency variation, etc.

During the "programming" process of the virtual programmable power supply, all the specifications, including those for the disturbances, are initialized by running a MATLAB M-file. For example, different harmonic patterns are saved in form of the sequence components at each harmonic order (up to the 20th). In the initialization process, they are loaded and converted into three-phase components before assigned to the model. There is also a tool developed to visualize and verify the harmonic pattern. The screenshot in Figure 5.3 shows the objects involved in this workflow: the model, the M-file and the visualization tool. Such a workflow ensures that the setting of the harmonic patterns is convenient and intuitive.

During the dSPACE experiments, the three-phase output of the virtual programmable power supply is connected to three RTI D/A blocks to drive the physical D/A unit in the Controller Board and produce analog output signals.

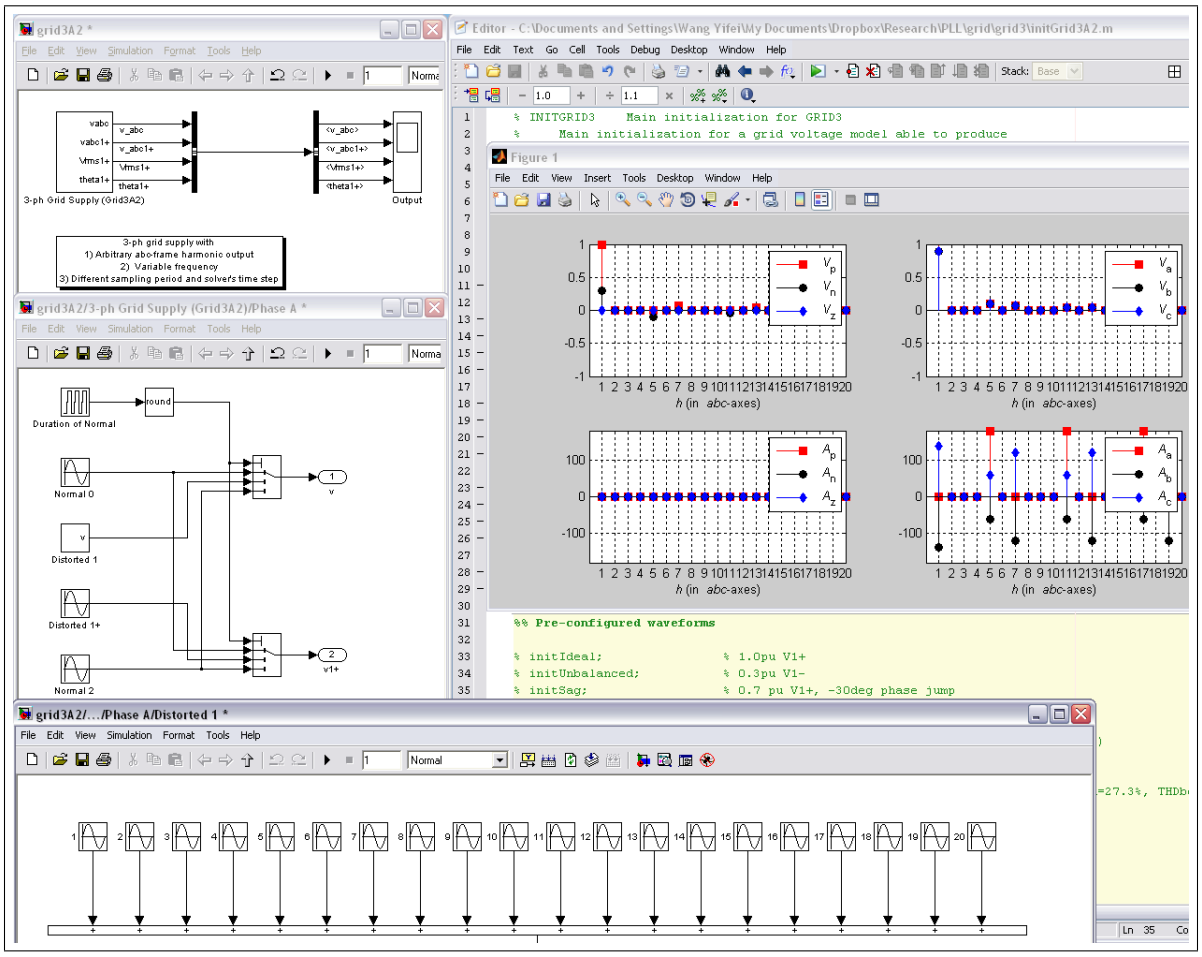


Figure 5.3: Screenshot that shows the objects involved in the "programming" process of the virtual programmable power supply: the Simulink model, the M-file to pre-specifiy the supply waveform, and the tool to visualize the harmonic pattern.

5.2.2 Models of the CDSC-PLLs

Three models have been built for the experiments with the grid phase detection CDSC-PLL, the selective harmonic detection PLL, and the discretized DSC/CDSC operators. They are introduced as follows:

1. *Model for the grid phase detection CDSC-PLL*

   This model is generally built according to the block diagram in 2.8. The $\alpha\beta$-frame CDSC operator used in it can be configured as $\alpha\beta\text{CDSC}_{4,6,24}$ or $\alpha\beta\text{CDSC}_{2,4,8,16}$, whose harmonic responses are the same as the one plot in Figure 2.4(a) and Figure 2.4(b), respectively. One of the two CDSC operators can be enabled in experiments simply by modifying a flag variable in the initialization M-file. For distinguishment purpose, the CDSC-PLL with the $\alpha\beta\text{CDSC}_{4,6,24}$ operator enabled is

named as CDSC-PLL1 in this chapter, while the one with $\alpha\beta\text{CDSC}_{2,4,8,16}$ is named as CDSC-PLL2.

Similarly , there are two options to obtain the fundamental period T used by the CDSC operators: use a constant value, or enable the FFL and use its estimated result. One of the two options is picked up in the initialization stage, too.

2. *Model for the selective harmonic detection CDSC-PLL*

   This model is generally built according to the block diagram drawn in Figure 3.9. When frequency adaptability is needed, the FFL is added to the model to make a CDSC-FFL-PLL system, whose block diagram is just like the one drawn in Figure 3.10. Both of the CDSC-PLL and CDSC-FFL-PLL models have six detection subsystems, respectively to detect harmonics $h = +1, -1, -5, +7, -11, +13$. All the subsystems share the same CDSC configuration that has the harmonic response in Figure 3.8. The only exception occurs when the input harmonics are asymmetrical, and the CDSC block must be configured to have the harmonic response in Figure 3.6.

3. *Model for the discretized DSC/CDSC operators*

   In this model, the three-phase grid voltage signal is transformed into the $\alpha\beta$-frame and the dq-frame. The $\alpha\beta$-frame signal is simultaneously provided to the $\alpha\beta\text{DSC}_4$, $\alpha\beta\text{DSC}_{4,6,24}$ and $\alpha\beta\text{DSC}_{2,4,8,16}$ operators, each of which is respectively discretized with round-down, round-up and interpolation settings (nine $\alpha\beta$-frame DSC/CDSC operators in total). Round-down is set by using $\alpha\beta\text{DSC}_{n\text{f}}$ for the $\alpha\beta\text{DSC}_{n\text{r}}$ block in Figure 4.5, i.e. let delay block $z^{-N_{n\text{r}}} = z^{-N_{n\text{f}}}$ and relative delay error $\varepsilon_{\text{r}} = \varepsilon_{\text{f}}$. Similarly, round-up is set by using $\alpha\beta\text{DSC}_{nc}$ for the $\alpha\beta\text{DSC}_{n\text{r}}$ block, i.e. let $z^{-N_{n\text{r}}} = z^{-N_{nc}}$, $\varepsilon_{\text{r}} = \varepsilon_{\text{c}}$. Finally, interpolation is implemented by entirely replacing the $\alpha\beta\text{DSC}_{n\text{r}}$ block by the $\alpha\beta\text{DSC}_{n\text{i}}$ block in Figure 4.6.

   On the other hand, the dq-frame signal is simultaneously provided to the dq-frame versions of the abovementioned DSC/CDSC operators, which also have round-down, round-up and interpolation settings (nine dq-frame DSC/CDSC operators in total). Therefore, this model allows the experimenter to systematically investigate and compare the effects of rounding and interpolation in different DSC/CDSC configurations.

5.3 Test Cases and Experimental Results for the Grid Phase Detection CDSC-PLL

For the models of CDSC-PLL1 and CDSC-PLL2, four test cases are designed, where the grid voltage input is contaminated by the mixture of different disturbances. The settings are detailed as follows:

1. For CDSC-PLL1

   (a) *Test Case 1* (unbalanced voltage sag): the peak value of the positive-sequence fundamental component V^{+1} is reduced to 0.7 p.u., accompanied by a $-30°$ phase jump. Meanwhile, a 0.3 p.u. negative-sequence component V^{-1} is added.

   (b) *Test Case 2* (symmetrical harmonics): $V^h = 1.0/2h$ p.u. for odd harmonics $h = -5, +7, -11, +13, -17, +19$, and $V^h = 1.0/2h/4$ p.u. for even harmonics $h = -2, 4, -8, 10, -14, 16, -20$. The total harmonic distortion (THD) is calculated to be 16.0% for this case.

   (c) *Test Case 3* (frequency variation with unbalanced voltage sag): grid frequency f jumps from the nominal value of 60 Hz to 55 Hz, lasts for 10 cycles (166.7 ms), and then returns to 60 Hz. The unbalanced voltage sag (with the phase jump) in Test Case 1 is also triggered in the beginning of the frequency variation.

   (d) *Test Case 4* (frequency variation with voltage harmonics): grid frequency f jumps from the nominal value of 60 Hz to 55 Hz, lasts for 10 cycles (166.7 ms), and then returns to 60 Hz. The symmetrical harmonics in Test Case 2 is also added throughout the frequency variation.

2. For CDSC-PLL2

   (a) *Test Case 1* (unbalanced voltage sag): the same as Test Case 1 for CDSC-PLL1.

   (b) *Test Case 2* (symmetrical and asymmetrical harmonics): $V^h = 1.0/2h$ p.u. for $h = \pm 5, \pm 7, \pm 11, \pm 13$, which can be translated into $V_a^5 = 0.2$ p.u., $V_b^5 = V_c^5 = 0.1$ p.u., $V_a^7 = 0.142$ p.u., $V_b^7 = V_c^7 = 0.071$ p.u., etc. In this test case, phase A voltage is less sinusoidal (THD = 27.3%) than phase B and C (THD = 16.7%).

   (c) *Test Case 3* (frequency variation with unbalanced voltage sag): the same as Test Case 3 for CDSC-PLL1.

   (d) *Test Case 4* (frequency variation with voltage harmonics): grid frequency f jumps from the nominal 60 Hz to 55 Hz, lasts for 10 cycles (166.7 ms), and then returns to 60 Hz.

The symmetrical and asymmetrical harmonics in Test Case 2 are also added throughout the frequency variation.

The test cases are designed in such a way that CDSC-PLL1 is subject to symmetrical harmonics, while CDSC-PLL2 is subject to both symmetrical and asymmetrical harmonics. This is because the two PLL schemes are intentionally configured for these two different scenarios. CDSC-PLL1 cannot operate satisfactorily under asymmetrical harmonics. Contrarily, CDSC-PLL2 can readily handle all symmetrical harmonics, but it is not as time efficient as CDSC-PLL1.

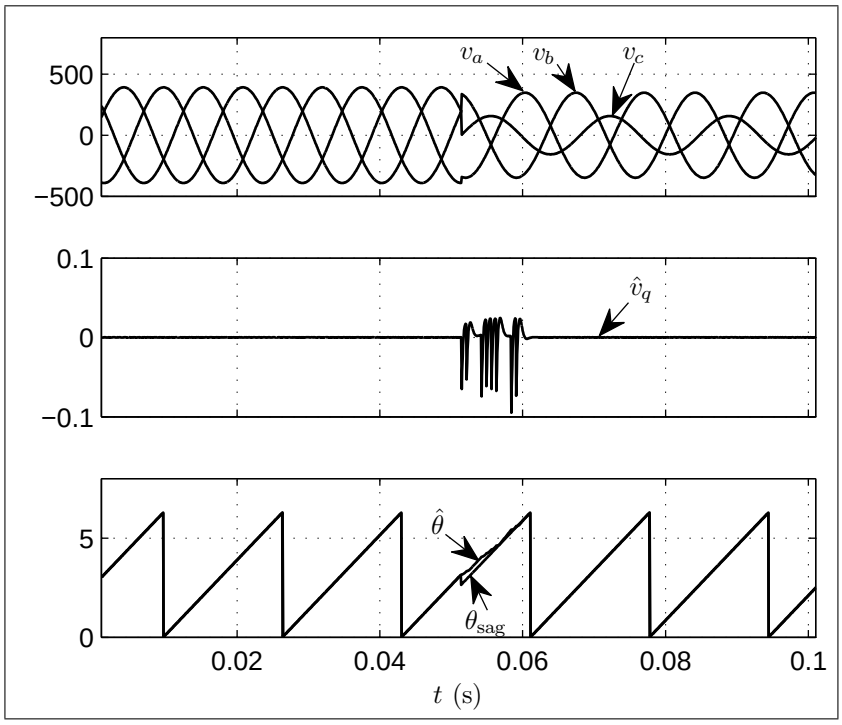
All experiments are set with nominal frequency $f = 60$ Hz and nominal phase voltage (peak value) $V^{+1} = 392$ V $= 1.0$ p.u. System sampling frequency f_s is selected as 14.4 kHz to make sure that every delay interval in CDSC-PLL1 and CDSC-PLL2 corresponds to an integer number of signal samples. The experimental results are reported in Figure 5.4–5.7.

Figure 5.4 shows the performance of the two PLL schemes in Test Case 1. The ideal grid phase angle θ_{sag} is also captured from the virtual programmable power supply and plot to compare with the estimated phase angle $\hat{\theta}$. To quantify the duration of the transient, the waveform of $\hat{v}_q$ is zoomed in for better observation—as mentioned in Section 2.3, this signal $\hat{v}_q = \sin\delta \approx \delta$ marks the phase error. The 30° phase jump corresponds to an initial phase error $\delta = 0.52$ rad. When $\hat{v}_q < 1\% \times \sin(0.52) = 0.005$ p.u., the transient can be considered over. With this criterion, it can be read from Figure 5.4(a) and 5.4(b) that CDSC-PLL1 undergoes a transient of 0.6 T (10 ms), while CDSC-PLL2 undergoes a longer time—1.0 T (17 ms) due to more DSC blocks used. Both results agree with the analysis in Section 2.5. The disturbance of $\hat{v}_q$ displays a chopped pattern, which is produced by summation of v_q with its cascaded delayed versions. Compared with the 2.0 T settling time in [51], the performance of CDSC-PLL1 and CDSC-PLL2 are obviously more superior. After the transients are over, both PLL schemes maintain ripple-free $\hat{v}_q$, implying that their output, the estimated phase $\hat{\theta}$, is unaffected by voltage unbalance.

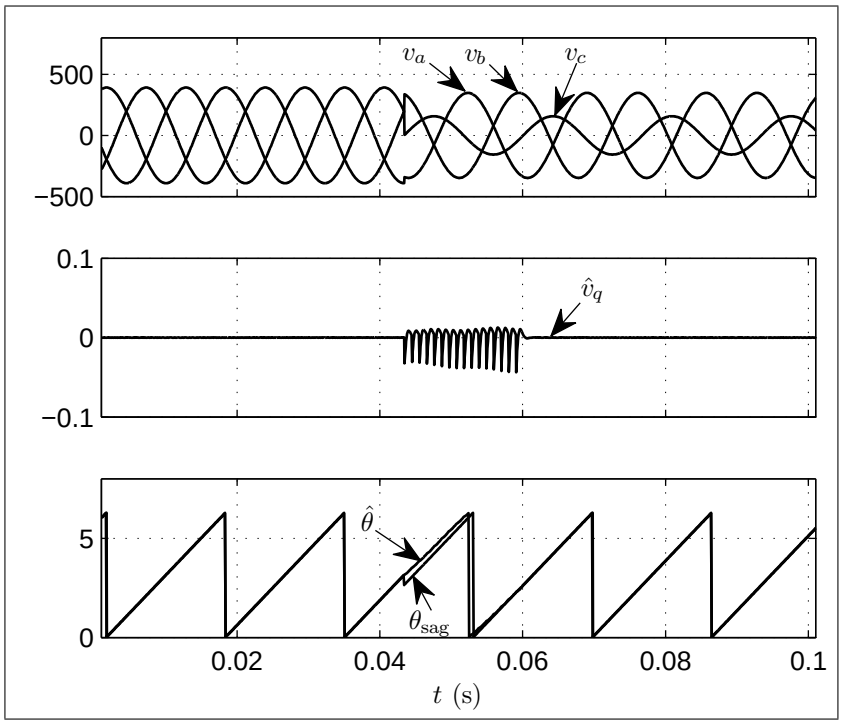
In Test Case 2 for CDSC-PLL1 (Figure 5.5(a)), $\boldsymbol{v}_{abc}$ is severely distorted with symmetrical (odd- and even-order) harmonics, hence the waveform is not half-wave symmetrical. Ripple-free $\hat{v}_d$ and $\hat{v}_q$ indicate that CDSC-PLL1 completely cancels out all harmonics, as expected for the CDSC operator. Meanwhile, Figure 5.5(b) demonstrates the satisfactory performance of CDSC-PLL2 under asymmetrically distorted three-phase harmonics, and confirms that the PLL cancels out all positive- and negative-sequence harmonics.

Figure 5.6(a) and 5.6(b) show how CDSC-PLL1 and CDSC-PLL2 equipped with the FFL track the grid phase and frequency in Test Case 3, where a ± 5 Hz frequency variation takes place. To more comprehensively evaluate the robust performance of the FFL, the same unbalanced voltage sag (with a -30° phase jump) in Test Case 1 is also triggered in the beginning of the frequency variation. It can be measured from the plot that for both CDSC-PLL1 and CDSC-PLL2, zero frequency and phase angle tracking errors are achieved within approximately 40 to 48 ms, i.e. 2.4 to 2.9 T in 60 Hz power system, after the frequency shift is triggered. CDSC-PLL2 has a longer transient, as its CDSC operator introduces longer delay into the FFL loop. Compared with the situation without the FFL, both CDSC-PLL has increased transient duration. This is in agreement with the theoretical analysis that the slower FFL dominates the entire PLL loop dynamics.

Finally, Test Case 4 is used to verify the performance of CDSC-PLL with FFL under frequency variation accompanied by voltage distortion. Besides the same ± 5 Hz frequency variation, the same harmonics as in Test Case 2 are also added to the grid voltage (CDSC-PLL1: only symmetrical harmonics. CDSC-PLL2: both symmetrical and asymmetrical harmonics). Results in Figure 5.7(a) and 5.7(b) make it evident that it also takes approximately 2.4 to 2.9 T for the two systems to achieve zero frequency and phase angle tracking errors. Moreover, both CDSC-PLL schemes can completely eliminate their targeted harmonics at the new 55 Hz frequency. This proves that the delay time in each DSC block is accurately calculated with the shifted frequency—frequency adaptability is successfully realized for CDSC-PLL.

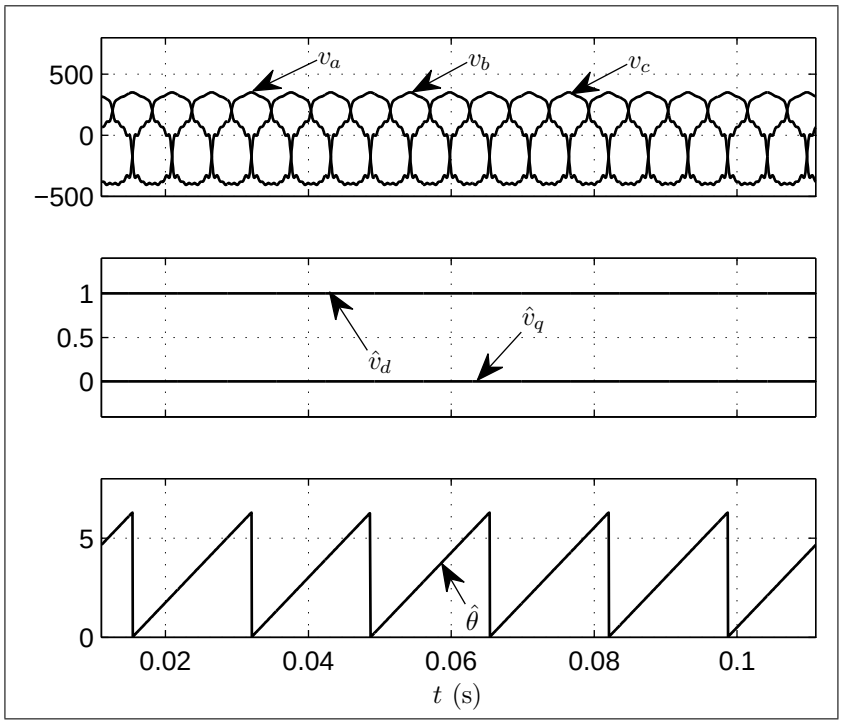


(a)

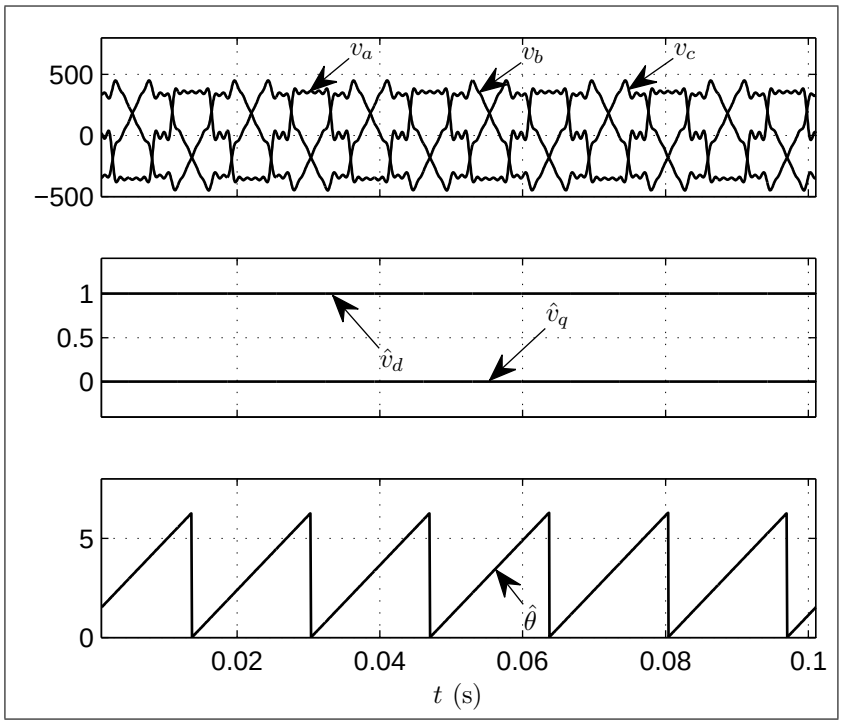


(b)

Figure 5.4: Experimental results of CDSC-PLL in Test Case 1. (a) Response of CDSC-PLL1. (b) Response of CDSC-PLL2. $\boldsymbol{v}_{abc}$ (V): three-phase grid voltage. $\hat{v}_q$ (p.u.): estimated q-component of grid voltage. θ_{sag} (rad): calculated ideal grid phase angle during the sag. $\hat{\theta}$ (rad): estimated phase angle.

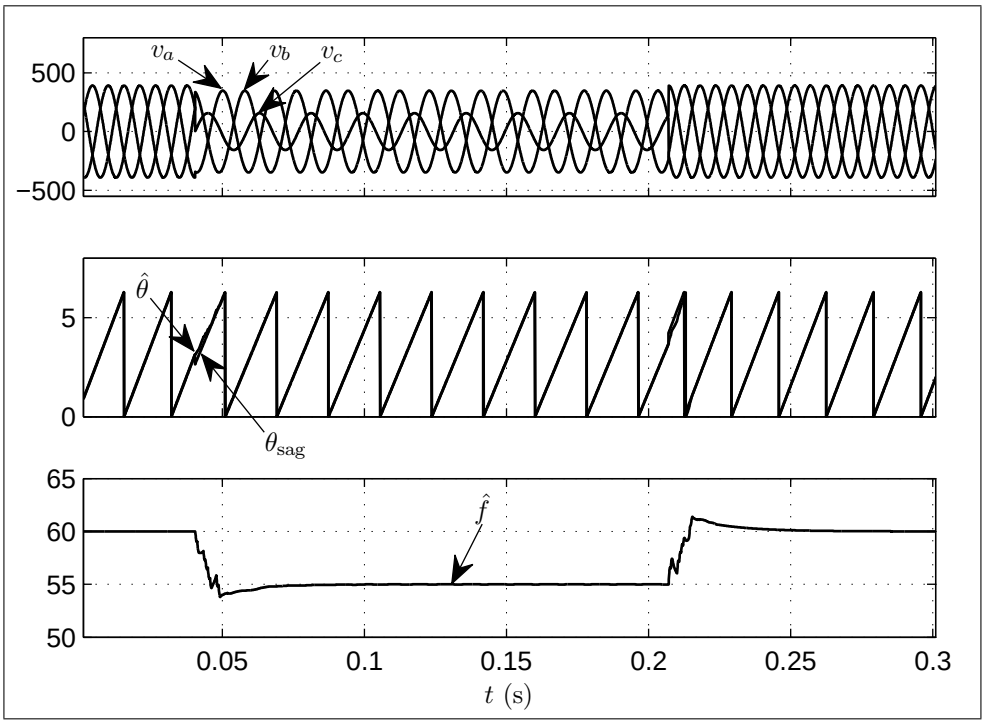


(a)

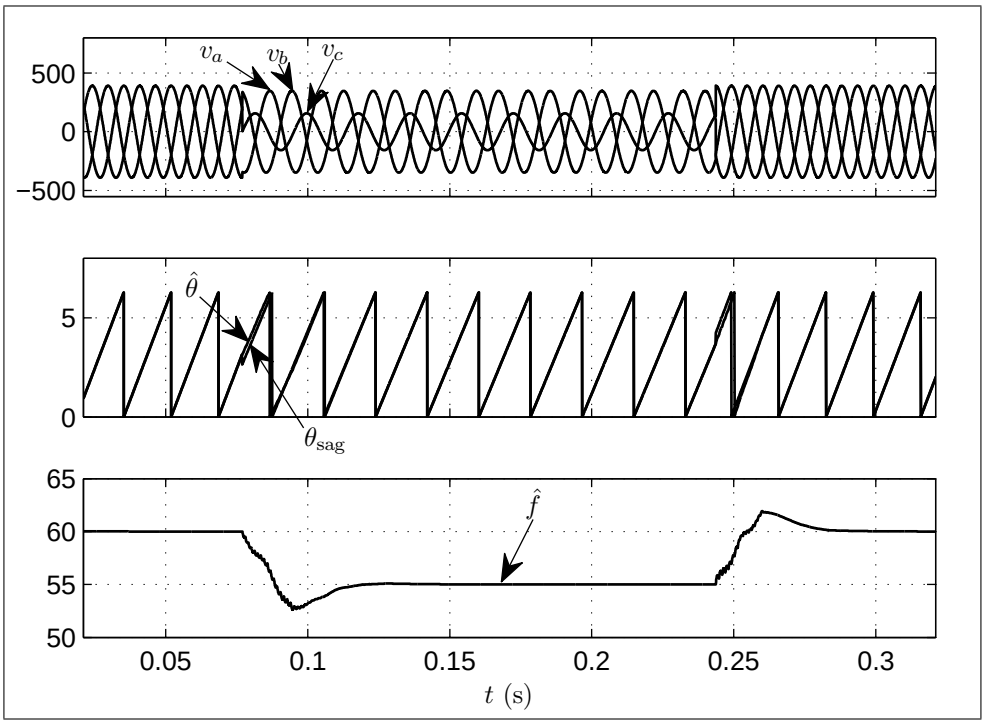


(b)

Figure 5.5: Experimental results of CDSC-PLL in Test Case 2. (a) Response of CDSC-PLL1. (b) Response of CDSC-PLL2. $\boldsymbol{v}_{abc}$ (V): three-phase grid voltage. $\hat{\boldsymbol{v}}_{dq}$ (p.u.): estimated dq-components of grid voltage. $\hat{\theta}$ (rad): estimated phase angle.

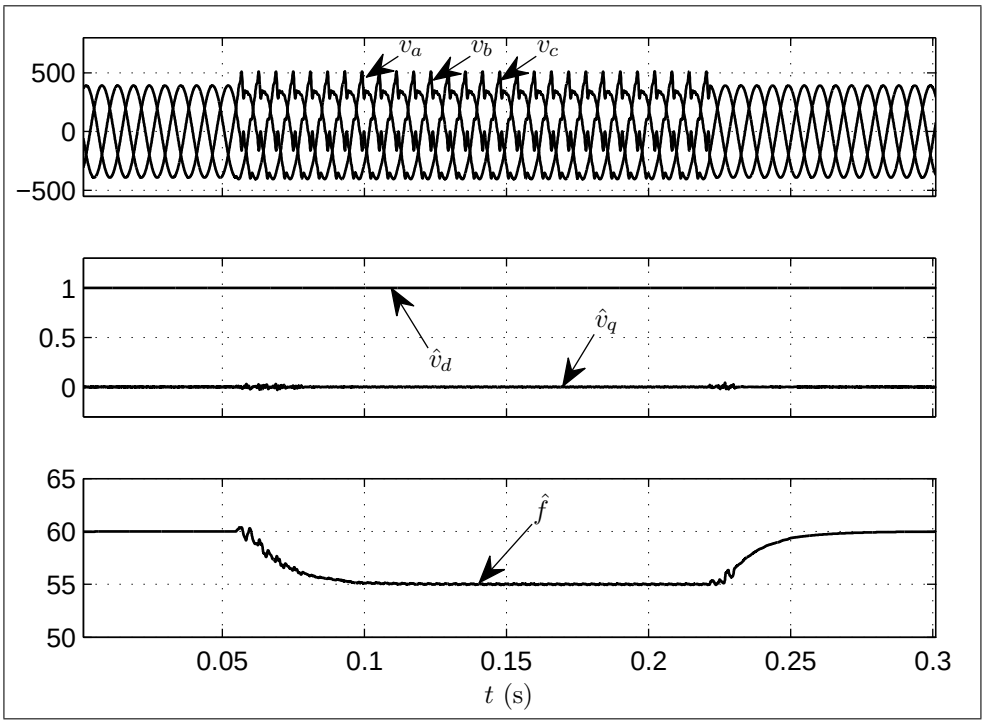


(a)

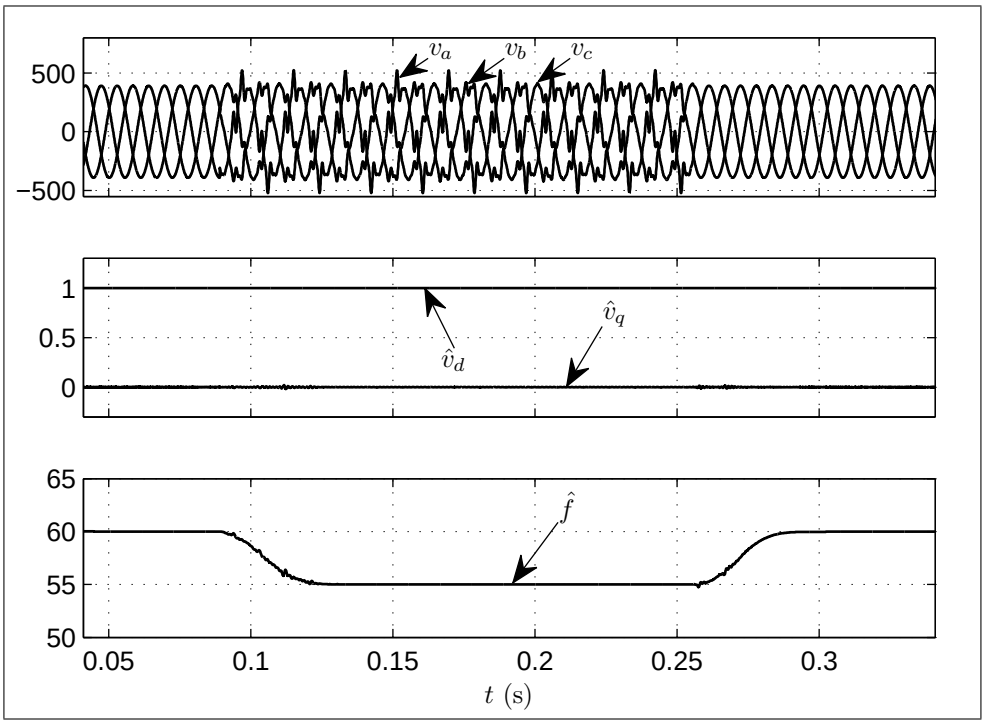


(b)

Figure 5.6: Experimental results of CDSC-PLL in Test Case 3. (a) Response of CDSC-PLL1. (b) Response of CDSC-PLL2. $\boldsymbol{v}_{abc}$ (V): three-phase grid voltage. θ_{sag} (rad): calculated ideal grid phase angle during the sag. $\hat{\theta}$ (rad): estimated phase angle. $\hat{f}$ (Hz): estimated frequency.



(a)



(b)

Figure 5.7: Experimental results of CDSC-PLL in Test Case 4. (a) Response of CDSC-PLL1. (b) Response of CDSC-PLL2. $\boldsymbol{v}_{abc}$ (V): three-phase grid voltage. $\hat{\boldsymbol{v}}_{dq}$ (p.u.): estimated dq-components of grid voltage. $\hat{f}$ (Hz): estimated frequency.

5.4 Test Cases and Experimental Results for the Selective Harmonic Detection CDSC-PLL

Four test cases are designed to verify the performance of the selective harmonic detection CDSC-PLL and CDSC-FFL-PLL systems under different conditions:

1. *Test Case 1*: the CDSC-PLL is used to detect typical harmonics with constant grid frequency (50 Hz).

2. *Test Case 2*: the CDSC-PLL is used to detect typical harmonics with slightly changed grid frequency (from 50 Hz to 49.9 Hz). The harmonics are introduced simultaneously as the frequency change is triggered.

3. *Test Case 3*: the CDSC-FFL-PLL is used to detect typical harmonics with considerably shifted grid frequency (from 50 Hz to 45 Hz). The harmonics and the frequency shift are also imposed simultaneously.

4. *Test Case 4*: the CDSC-PLL is used to detect asymmetrical harmonics generated by a diode rectifier.

Table 5.1: Harmonic specification of the power supply for the selective harmonic detection experiments.

Harmonic Order h	Magnitude V^h (p.u.)	Harmonic Order h	Magnitude V^h (p.u.)
$+1$	1.000	-11	0.046
-1	0.300	$+13$	0.039
-5	0.100	-17	0.029
$+7$	0.071	$+19$	0.026

Experiments are conducted for these test cases on the dSPACE platform at 7.2 kHz sampling frequency. For Test Cases 1–3, the input harmonics (with a spectrum specified in Table 5.1) are generated by the virtual programmable power supply, so as to easily incorporate the different frequency variations. Test Case 4 uses harmonics generated by a three-phase diode rectifier to evaluate the PLL system in a more realistic environment. The rectifier is supplied by a 50 Hz 104 V (line-to-line RMS value) voltage source through 5 mH line impedance. The load is a 940 μF capacitor and a resistor box connected in parallel. The ac side three-phase voltage waveforms are sensed as voltage input; they are also cap-

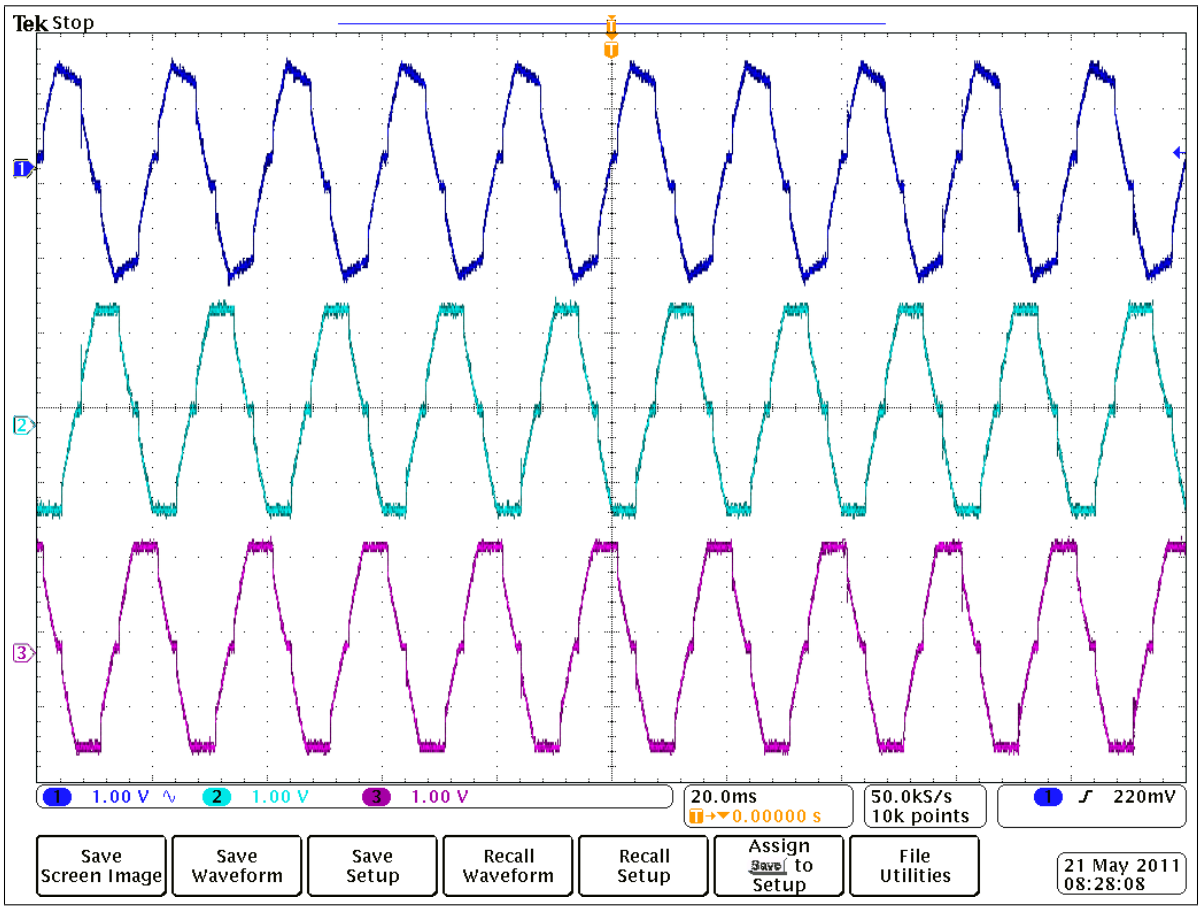


Figure 5.8: Three-phase asymmetrical voltage waveforms captured from a diode rectifier that is used to evaluate the performance of the selective harmonic detection CDSC-PLL system.

tured by a Tektronix DPO4034 oscilloscope with ×100 potential probes. The waveforms, as shown in Figure 5.8, are slightly asymmetrical due to the line impedance unbalance.

The experimental results of Test Cases 1–4 are plot in Figs. 5.9–5.20, respectively. Note that the magnitude waveforms of the fundamental components and the harmonics are plot in different scale, as the harmonics are relatively small. The phase angle waveforms of the fundamental components and the harmonics are also plot in different time scale, as the harmonics have much shorter periods.

It can be seen in Figure 5.9–5.11 that once the harmonics in Test Case 1 are superposed onto the input signal, the CDSC-PLL system can identify all of them after around 0.2–0.3 cycle (0.17 cycle from the DSC/CDSC operations and the rest from the *dq*PLL). The ripple-free magnitude waveforms implies that each detection subsystem can properly eliminate all the other harmonic components. Comparison of the detected magnitudes V^{h^+} with the preset value V^h in Table 5.1 shows agreement, verifying that

the magnitude correction mechanism functions as expected.

In Figure 5.12–5.14 (Test Case 2), although the harmonics are superposed in the same time when the grid frequency is reduced to 49.9 Hz, the CDSC-PLL system appears to be insensitive to this frequency variation, and can still accurately detect all the components. The transient duration does not change significantly, either.

Figure 5.15–5.17 presents the results of Test Case 3. This time the CDSC-FFL-PLL system undergoes a longer transient after the 5 Hz frequency shift is triggered. This is because the FFL must have slower dynamics than the inner detection subsystem, so as to maintain the overall system stability. Comparison of the detected frequency f_{det} and the programmed grid frequency f makes it clear that the FFL takes around one cycle (20 ms) to converge to the actual frequency. After that the DSC/CDSC blocks are working with accurate delay times, and the whole system can give precise estimate of the harmonic signals at the new frequency.

Finally, the results of Test Case 4 are provided in Figure 5.18–5.20, which demonstrates that the proposed CDSC-PLL system can work well with harmonics coming from a very realistic and typical application case. And, by properly configuring the structure of the CDSC block, CDSC-PLL system can handle complex harmonic inputs, such as asymmetrical harmonics.

It must be explained here that the non-ideal plotting of the high-frequency harmonics (e.g. the 11th and the 13th ones) in Figure 5.9–5.20 is due to the sampling frequency (7.2 kHz) of the experimental platform, which limits the data resolution.

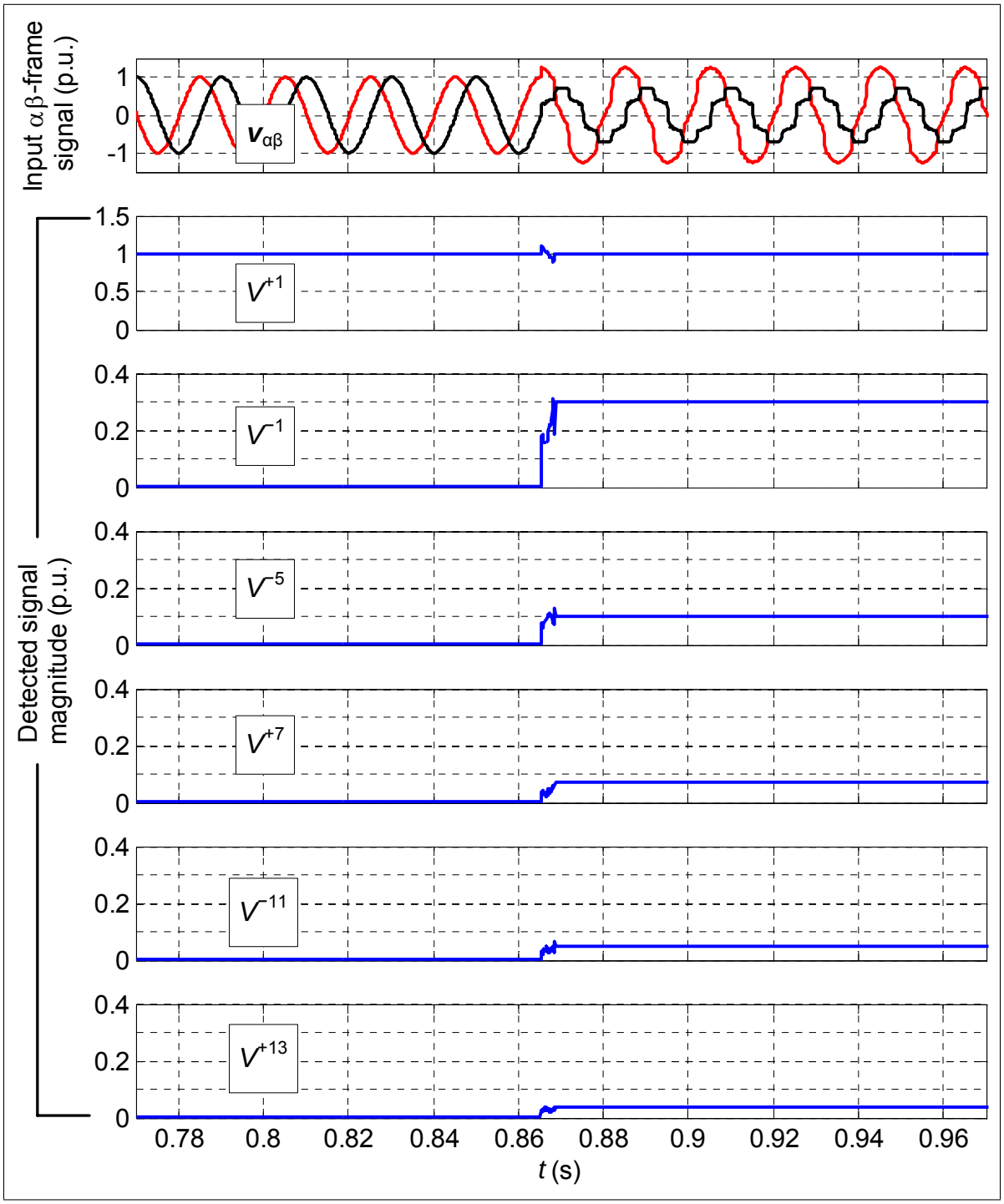


Figure 5.9: Experimental results of selective harmonic detection CDSC-PLL in Test Case 1: Input signal and detected signal magnitude.

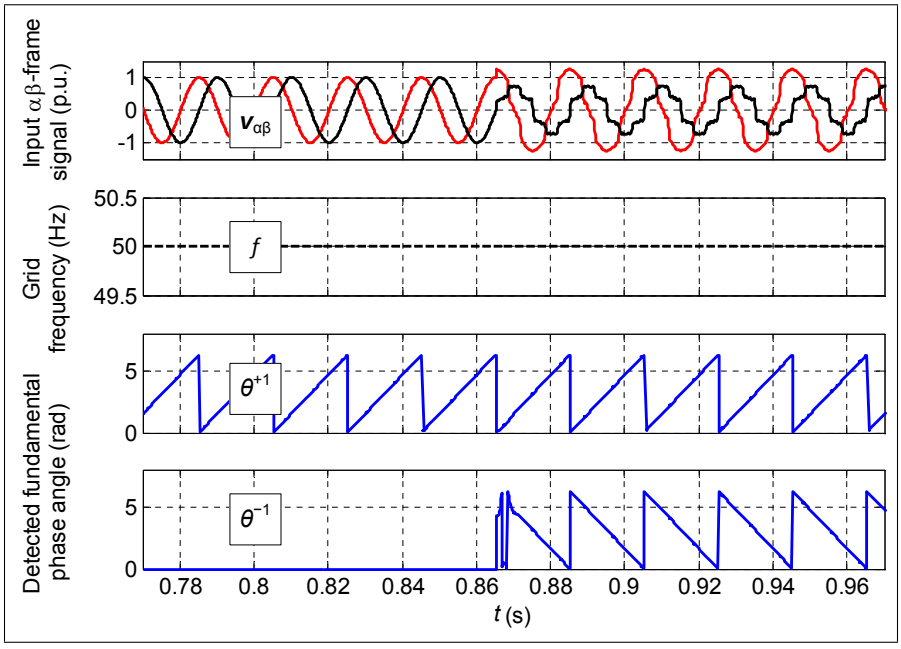


Figure 5.10: Experimental results of selective harmonic detection CDSC-PLL in Test Case 1: Input signal, grid frequency and detected fundamental phase angle.

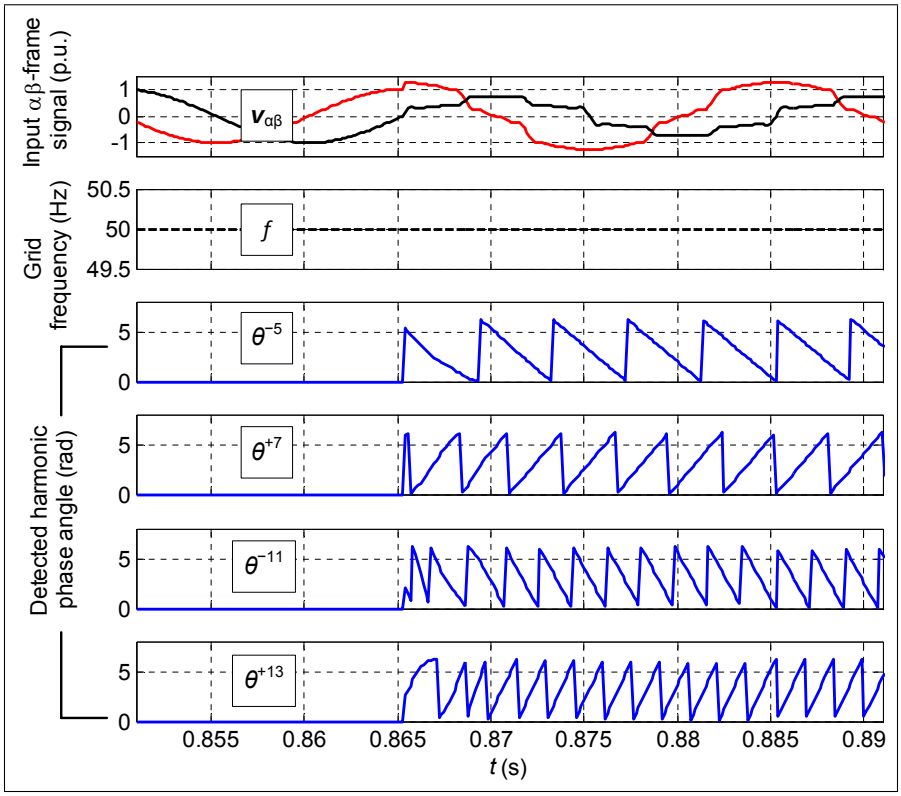


Figure 5.11: Experimental results of selective harmonic detection CDSC-PLL in Test Case 1: Input signal, grid frequency and detected harmonic phase angle.

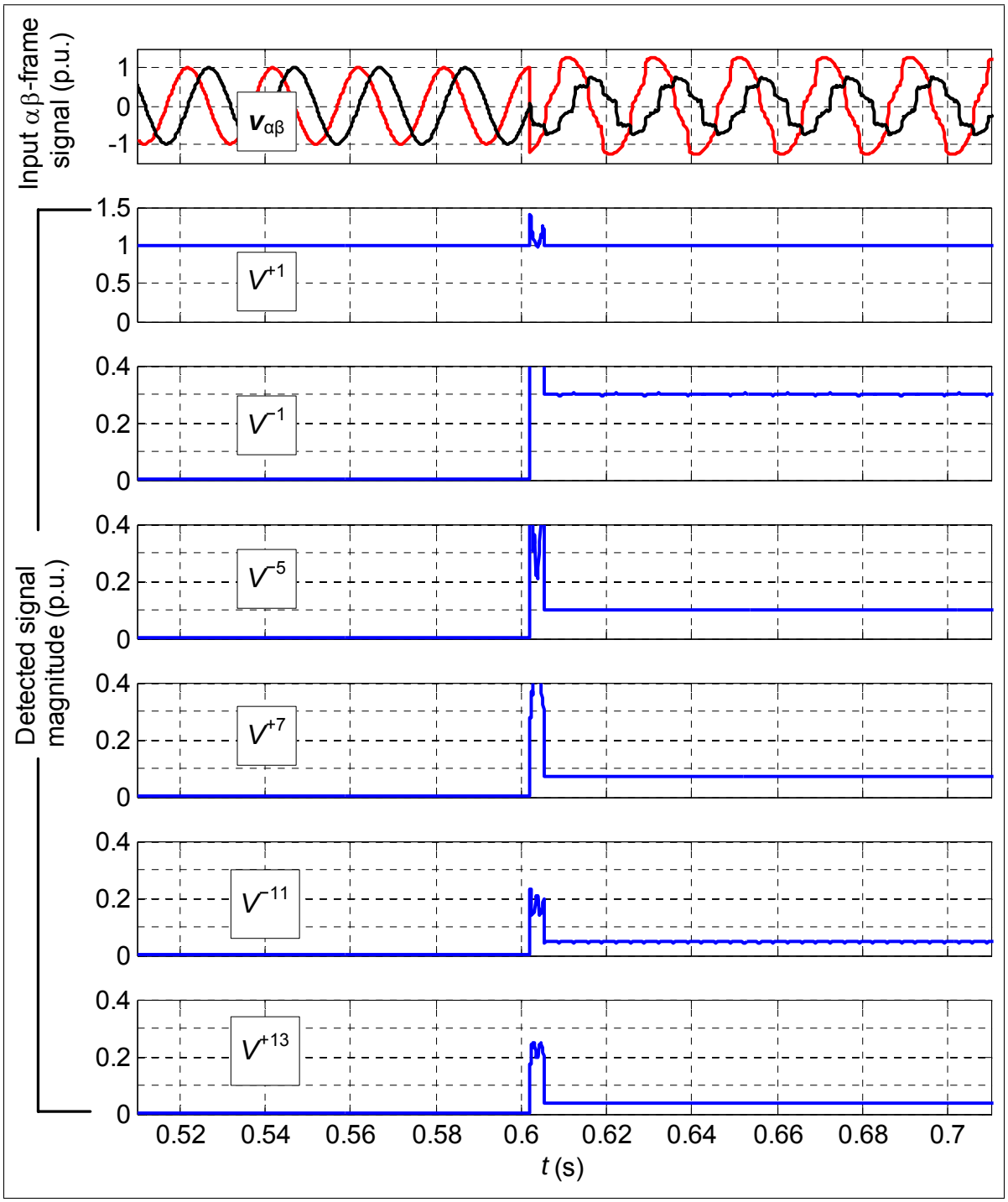


Figure 5.12: Experimental results of selective harmonic detection CDSC-PLL in Test Case 2: Input signal and detected signal magnitude.

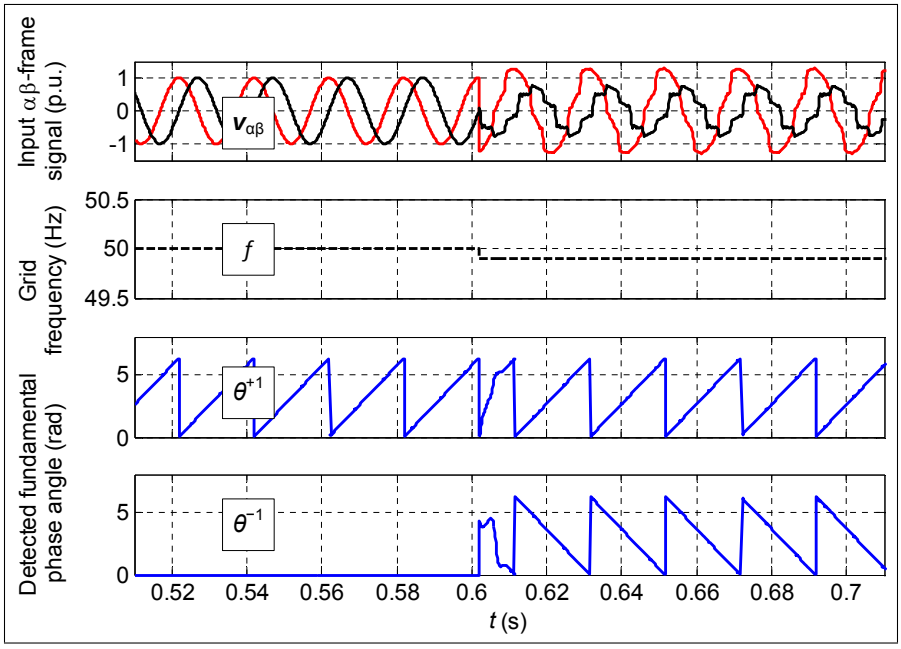


Figure 5.13: Experimental results of selective harmonic detection CDSC-PLL in Test Case 2: Input signal, grid frequency and detected fundamental phase angle.

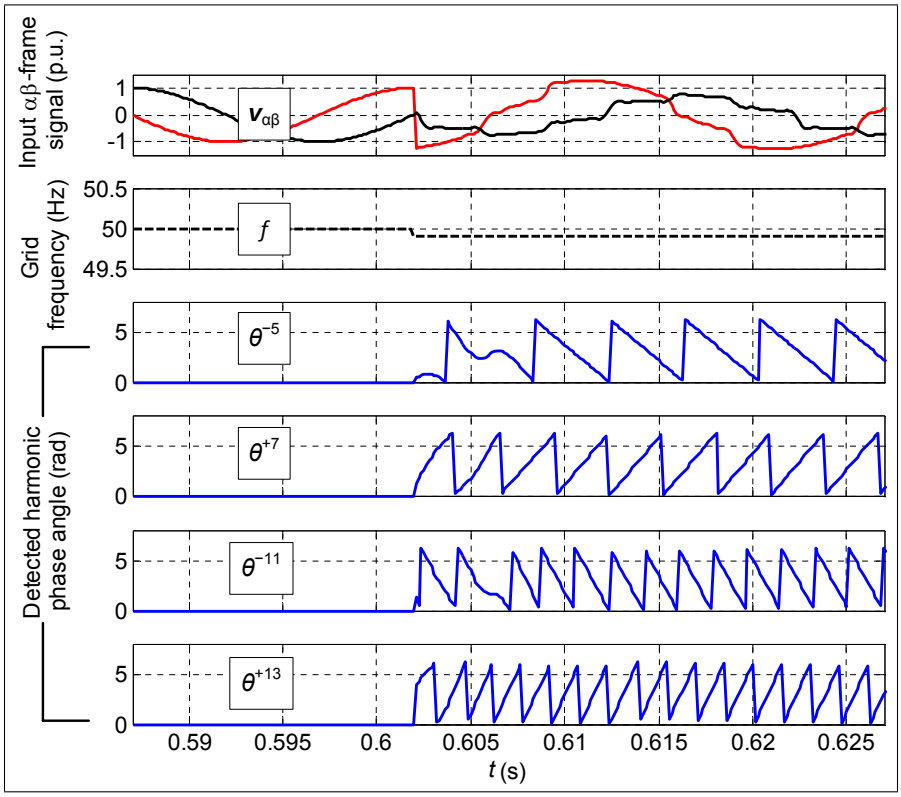


Figure 5.14: Experimental results of selective harmonic detection CDSC-PLL in Test Case 2: Input signal, grid frequency and detected harmonic phase angle.

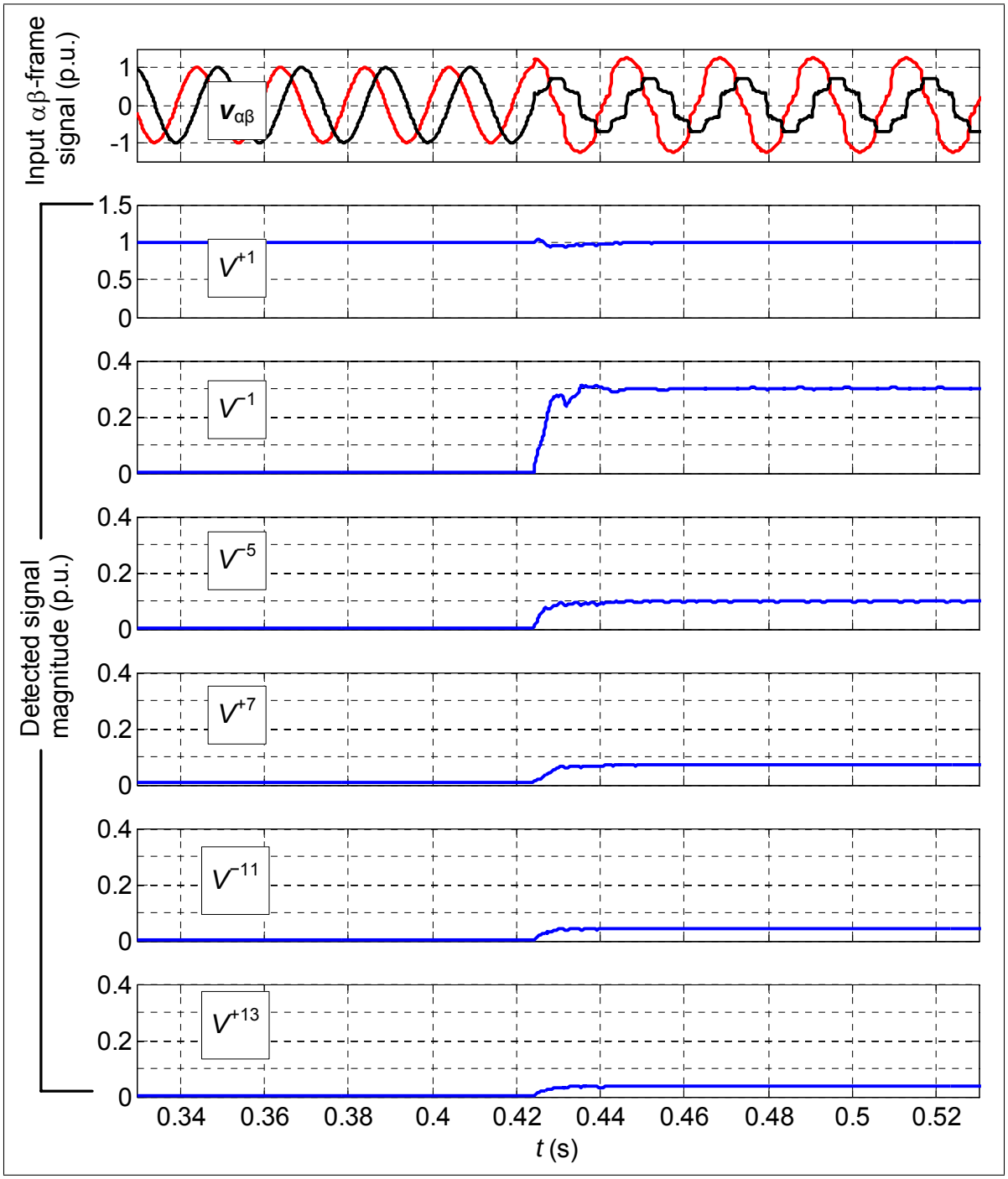


Figure 5.15: Experimental results of selective harmonic detection CDSC-FFL-PLL in Test Case 3: Input signal and detected signal magnitude.

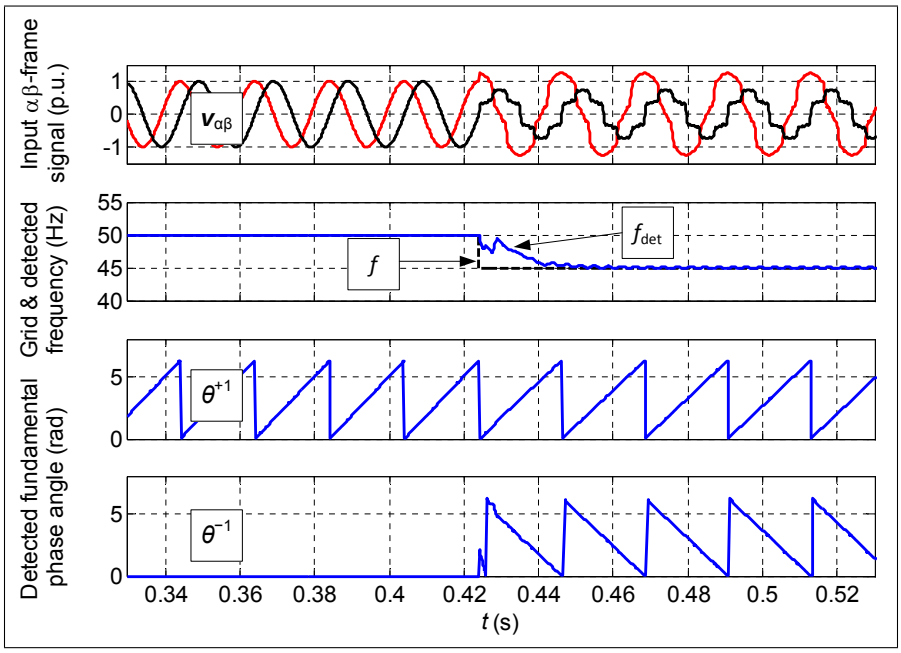


Figure 5.16: Experimental results of selective harmonic detection CDSC-FFL-PLL in Test Case 3: Input signal, grid & detected frequency and detected fundamental phase angle.

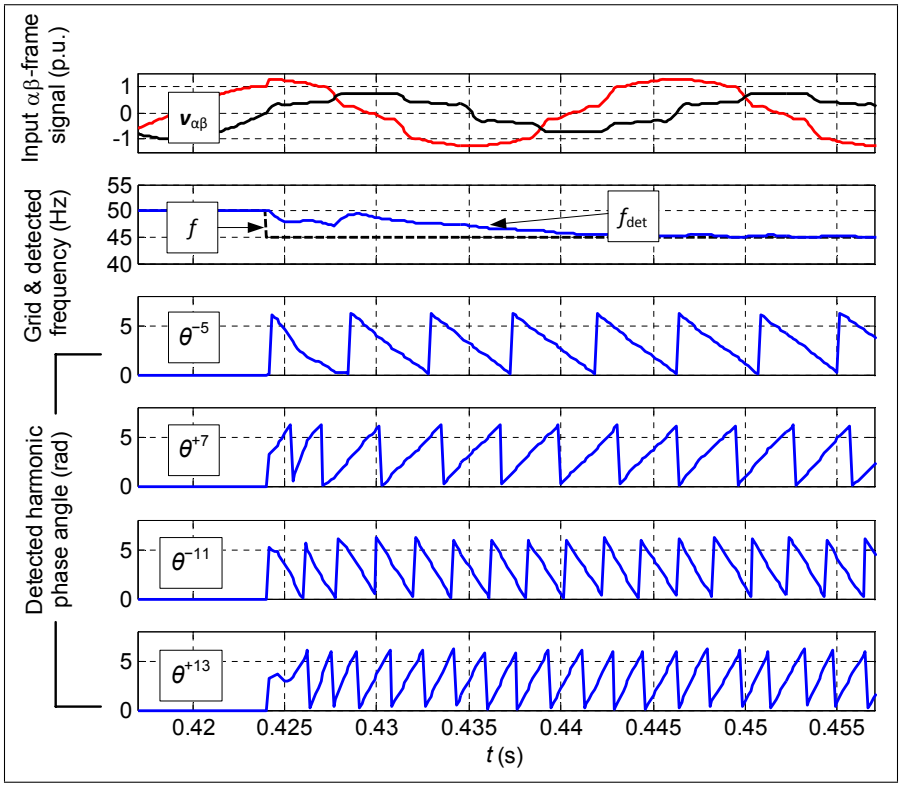


Figure 5.17: Experimental results of selective harmonic detection CDSC-FFL-PLL in Test Case 3: Input signal, grid & detected frequency and detected harmonic phase angle.

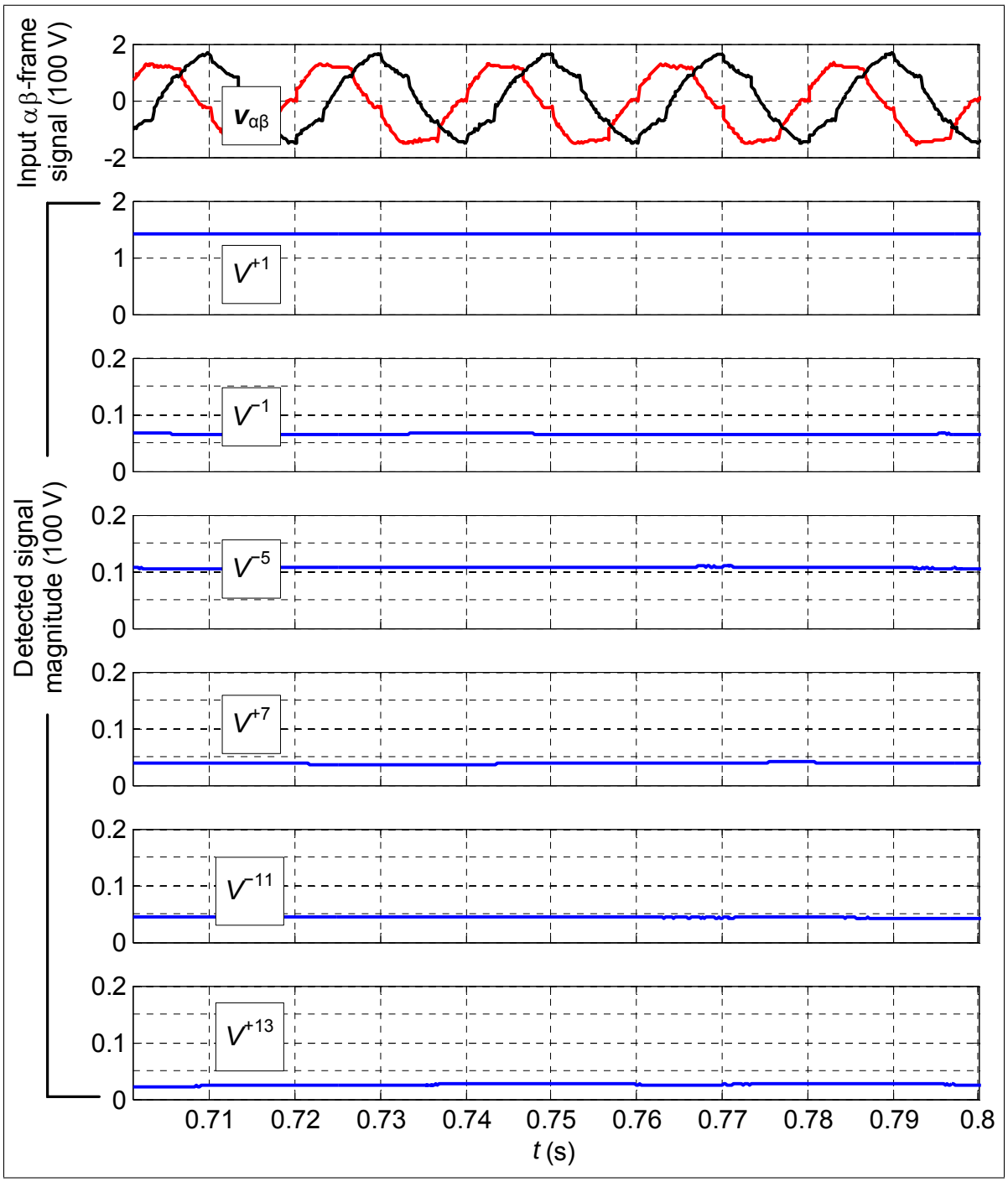


Figure 5.18: Experimental results of selective harmonic detection CDSC-PLL in Test Case 4: Input signal and detected signal magnitude.

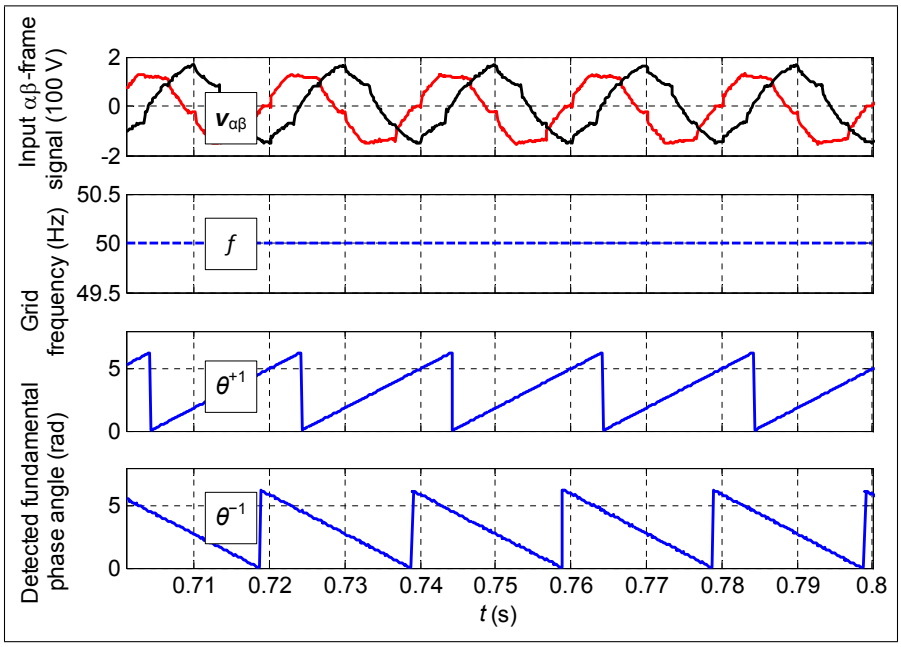


Figure 5.19: Experimental results of selective harmonic detection CDSC-PLL in Test Case 4: Input signal, grid frequency and detected fundamental phase angle.

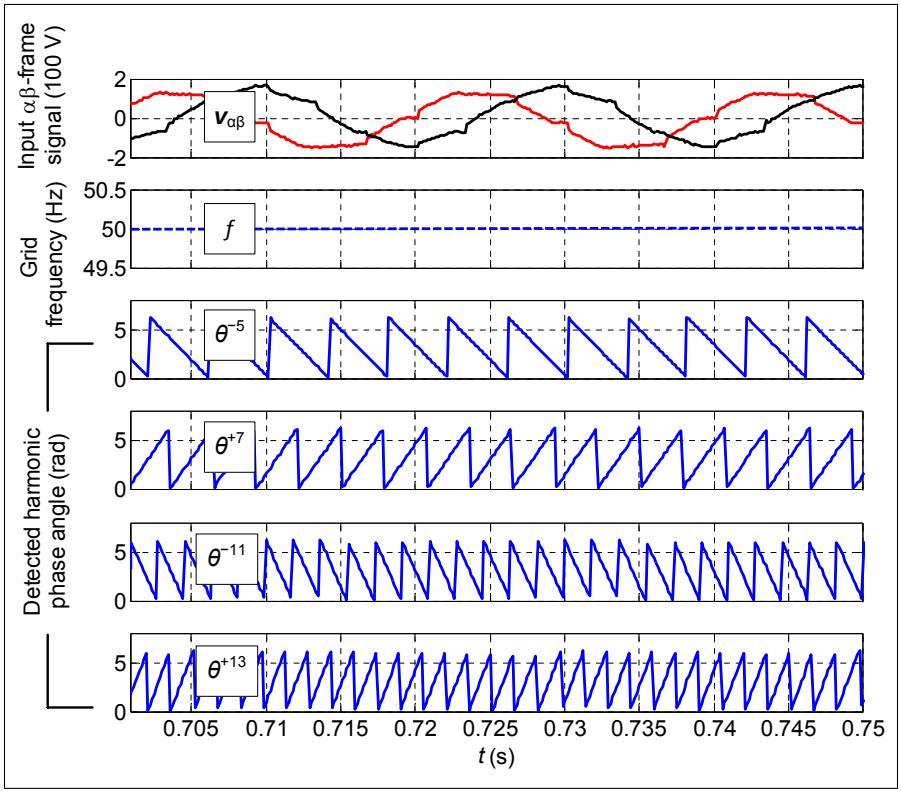


Figure 5.20: Experimental results of selective harmonic detection CDSC-PLL in Test Case 4: Input signal, grid frequency and detected harmonic phase angle.

5.5 Test Cases and Experimental Results for the Discretized DSC/CDSC Operators

Three test cases are designed to examine the effect of round-down, round-up and interpolation on the performance of the discretized $\alpha\beta$- and dq-frame DSC and CDSC operators. These test cases are:

1. *Test Case 1* (negative-sequence fundamental component vs. $\alpha\beta\text{DSC}_4$ and $dq\text{DSC}_4$): only a 0.3 p.u. negative-sequence harmonic is injected, while the $\alpha\beta\text{DSC}_4$ and $dq\text{DSC}_4$ operators are used to eliminate it.

2. *Test Case 2* (symmetrical harmonics vs. $\alpha\beta\text{CDSC}_{4,6,24}$ and $dq\text{CDSC}_{4,6,24}$): symmetrical harmonics ($h = -2, +4, -5, +7$[5]) are programmed in the grid supply with magnitude $V^h = 1.0/2h$ p.u. for odd harmonics $h = -5, +7, -11, +13, -17, +19$, and $V^h = 1.0/2h/4$ p.u. for even harmonics $h = -2, 4, -8, 10, -14, 16, -20$. The $\alpha\beta\text{CDSC}_{4,6,24}$ and $dq\text{CDSC}_{4,6,24}$ operators are used to eliminate these harmonics.

3. *Test Case 3* (symmetrical and asymmetrical harmonics vs. $\alpha\beta\text{CDSC}_{2,4,8,16}$ and $dq\text{CDSC}_{2,4,8,16}$): symmetrical ($h = -5, +7$) and asymmetrical harmonics ($h = +5, -7$) are programmed with magnitude $V^h = 1.0/(2h)$ p.u.. The $\alpha\beta\text{CDSC}_{2,4,8,16}$ and $dq\text{CDSC}_{2,4,8,16}$ operators are used to eliminate these harmonics.

In all the test cases, the nominal grid phase voltage (peak value) V^{+1} is equal to 392 V = 1.0 p.u. The grid frequency f is kept constant at 50 Hz, and the sampling frequency is set as $f_s = 10.15$ kHz.

For verification purpose, theoretical results are firstly calculated for the three test cases to determine the expected harmonic magnitude after the DSC/CDSC operations. The calculation is done by multiplying the harmonic magnitude before the DSC/CDSC operations by the harmonic gain derived in (4.5) and (4.11), and the results are visualized in Figure 5.21. It should be pointed out that every harmonic magnitude before DSC/CDSC operation is scaled by 1/10, otherwise the value is too much greater than the values after DSC/CDSC operation, making it very hard to compare them in the same plots.

The theoretical results in Figure 5.21 can be interpreted as

1. Grid harmonics can be greatly suppressed by the properly selected DSC/CDSC operators. Due to the high flexibility in the selection of DSC and CDSC operators, an arbitrary combination of harmonics can virtually be handled by the DSC/CDSC operation.

[5] All the harmonic orders in this section are in the $\alpha\beta$-frame.

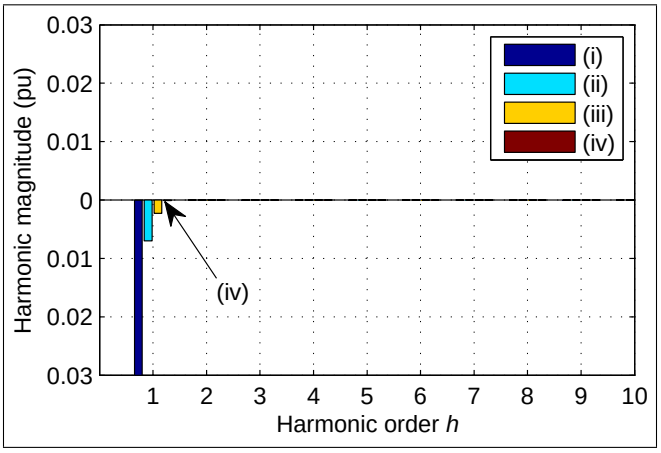
2. Small discretization errors arise from rounding when the harmonics are processed by discretized DSC/CDSC operators. In Figure 5.21, the shown magnitude of the round-down error is higher than that of the round-up error. This is because the truncation error is higher for round-down in this particular example.

3. The discretization error can be suppressed by the interpolation method, which performs stably for all the test cases and is insensitive to f_{s}.

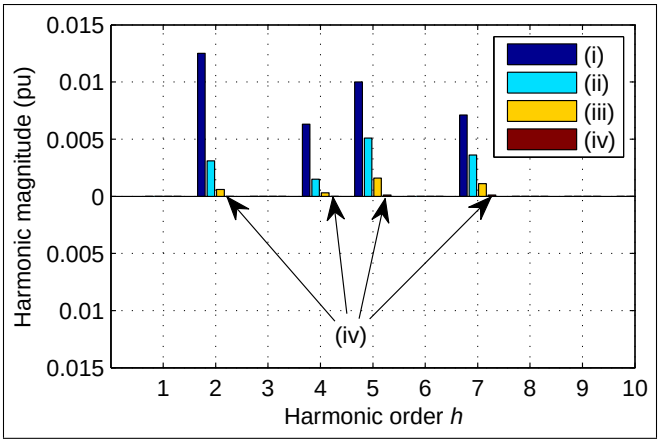
After the theoretical results are obtained, the three test cases are applied to the model on the dSPACE platform. The results are reported in Figure 5.22–5.24, where the theoretical results calculated above are also used to plot theoretical waveforms and compared with the experimental ones.

Figure 5.22 displays the experimental voltage waveforms of Test Case 1. In the plot, the left, the middle and the right columns of subplots show waveforms in the $\alpha\beta$-frame, waveforms in the dq-frame, and zoomed-in waveforms in the dq-frame, respectively. Among them, the original $\alpha\beta$-frame signal $\boldsymbol{v}_{\alpha\beta}$ is unbalanced, because it is the sum of the positive-sequence component $\boldsymbol{v}_{\alpha\beta}^{+1}$ (with 1.0 p.u. magnitude) and the negative-sequence one $\boldsymbol{v}_{\alpha\beta}^{-1}$ (with 0.3 p.u. magnitude). After simultaneously passed through $\alpha\beta$-frame DSC blocks $\alpha\beta\mathrm{DSC}_{4\mathrm{f}}$, $\alpha\beta\mathrm{DSC}_{4\mathrm{c}}$ and $\alpha\beta\mathrm{DSC}_{4\mathrm{i}}$ (respectively configured with round-down, round-up and interpolation settings), the negative-sequence component is removed as verified by the left column of subplots ($\alpha\beta\mathrm{DSC}_{4\mathrm{f}}[\boldsymbol{v}_{\alpha\beta}]$, $\alpha\beta\mathrm{DSC}_{4\mathrm{c}}[\boldsymbol{v}_{\alpha\beta}]$ and $\alpha\beta\mathrm{DSC}_{4\mathrm{i}}[\boldsymbol{v}_{\alpha\beta}]$). To better expose the performance improvement brought by interpolation, the original input signal $\boldsymbol{v}_{\alpha\beta}$ is also transformed into the dq-frame. The resulted $\boldsymbol{v}_{dq}$ is simultaneously passed through dq-frame DSC operators $dq\mathrm{DSC}_{4\mathrm{f}}$, $dq\mathrm{DSC}_{4\mathrm{c}}$ and $dq\mathrm{DSC}_{4\mathrm{i}}$. The output dq-frame signal waveforms are captured and zoomed-in in the right column. The subplots immediately make it apparent that the signals after dq-frame DSC operators with round-up and round-down settings ($dq\mathrm{DSC}_{4\mathrm{f}}$ and $dq\mathrm{DSC}_{4\mathrm{c}}$) do not completely eliminate the 100 Hz oscillation (corresponding to the negative-sequence component), but leave ripples with around 0.007 and 0.002 p.u. magnitude, respectively. To the contrary, $dq\mathrm{DSC}_{4\mathrm{i}}$, the operator with interpolation, completely suppresses the ripples. It confirms that the discretization error exists for the DSC operator, and can be successfully removed with the proposed interpolation method.

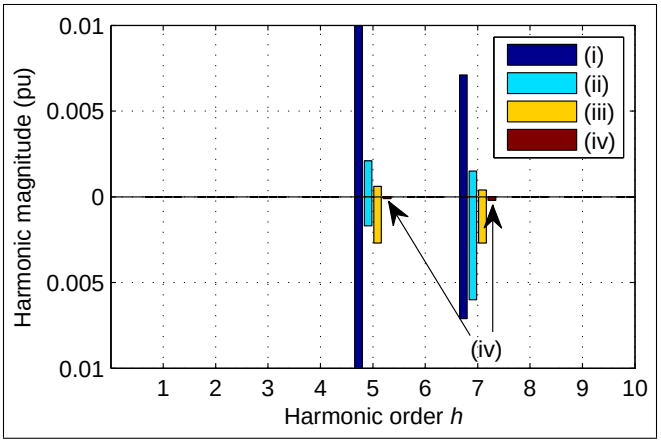
Besides the captured experimental waveforms, some theoretical results (the calculated harmonic magnitude before and after DSC operations, as shown in Figure 5.21a) are also used to plot theoretical waveforms in the right column of Figure 5.22. They overlap with the experimental ones very well, and so the correctness of the harmonic gain error formulae (4.5) and (4.11) is confirmed.



(a)



(b)



(c)

Figure 5.21: Theoretical harmonic magnitude before and after DSC/CDSC operations in the three test cases. (a) Test Case 1. (b) Test Case 2. (c) Test Case 3. (i) Original harmonic magnitude (*scaled by* 1/10). (ii) Magnitude after DSC/CDSC with round-down setting. (iii) Magnitude after DSC/CDSC with round-up setting. (iv) Magnitude after DSC/CDSC with interpolation.

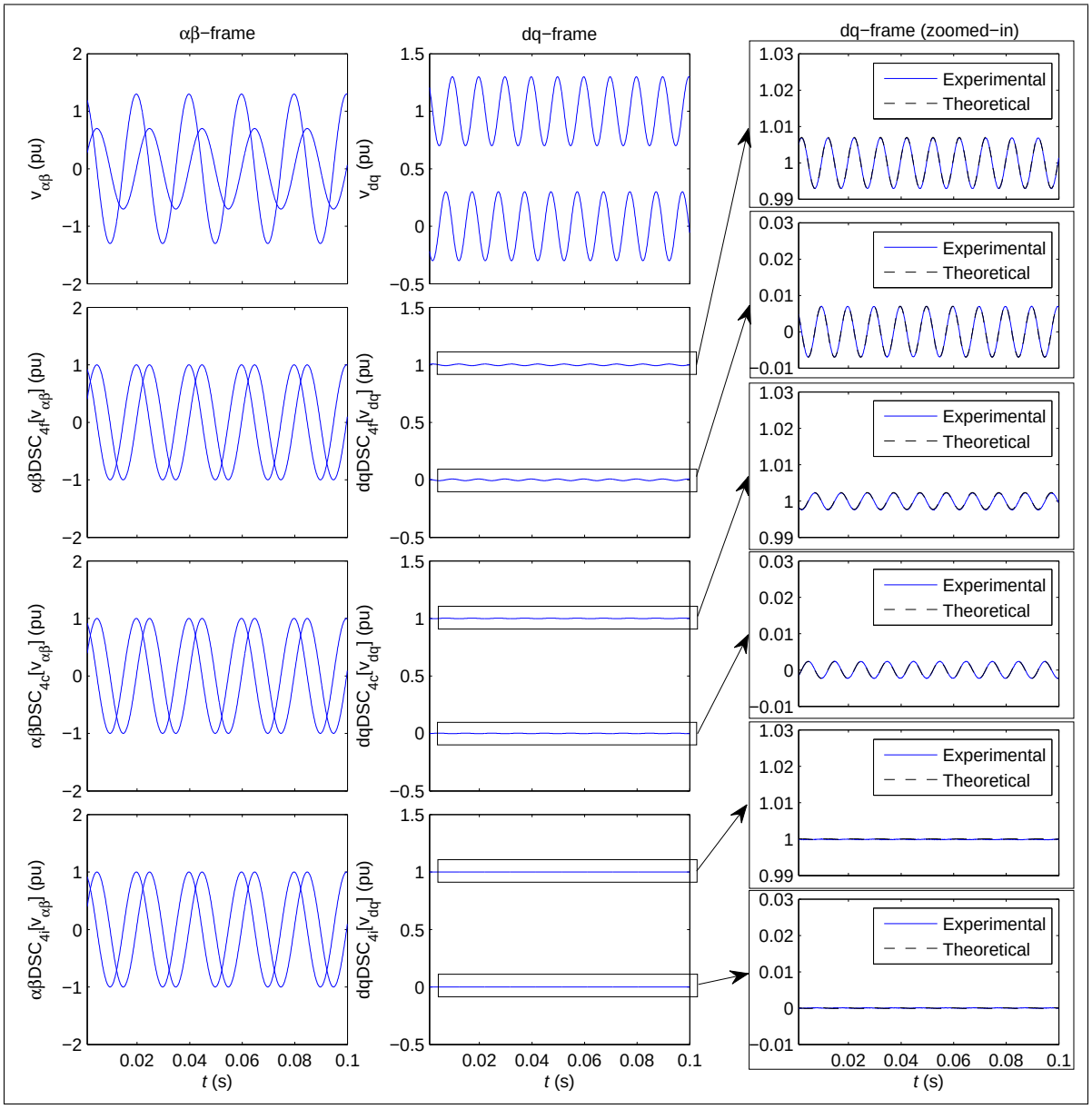


Figure 5.22: Theoretical and experimental voltage waveforms of the discretized DSC/CDSC operators in Test Case 1 (negative-sequence fundamental component vs. $\alpha\beta$DSC$_4$ and dqDSC$_4$). Subscripts 'f', 'c' and 'i' respectively refer to DSC/CDSC operation with round-down, round-up and interpolation settings.

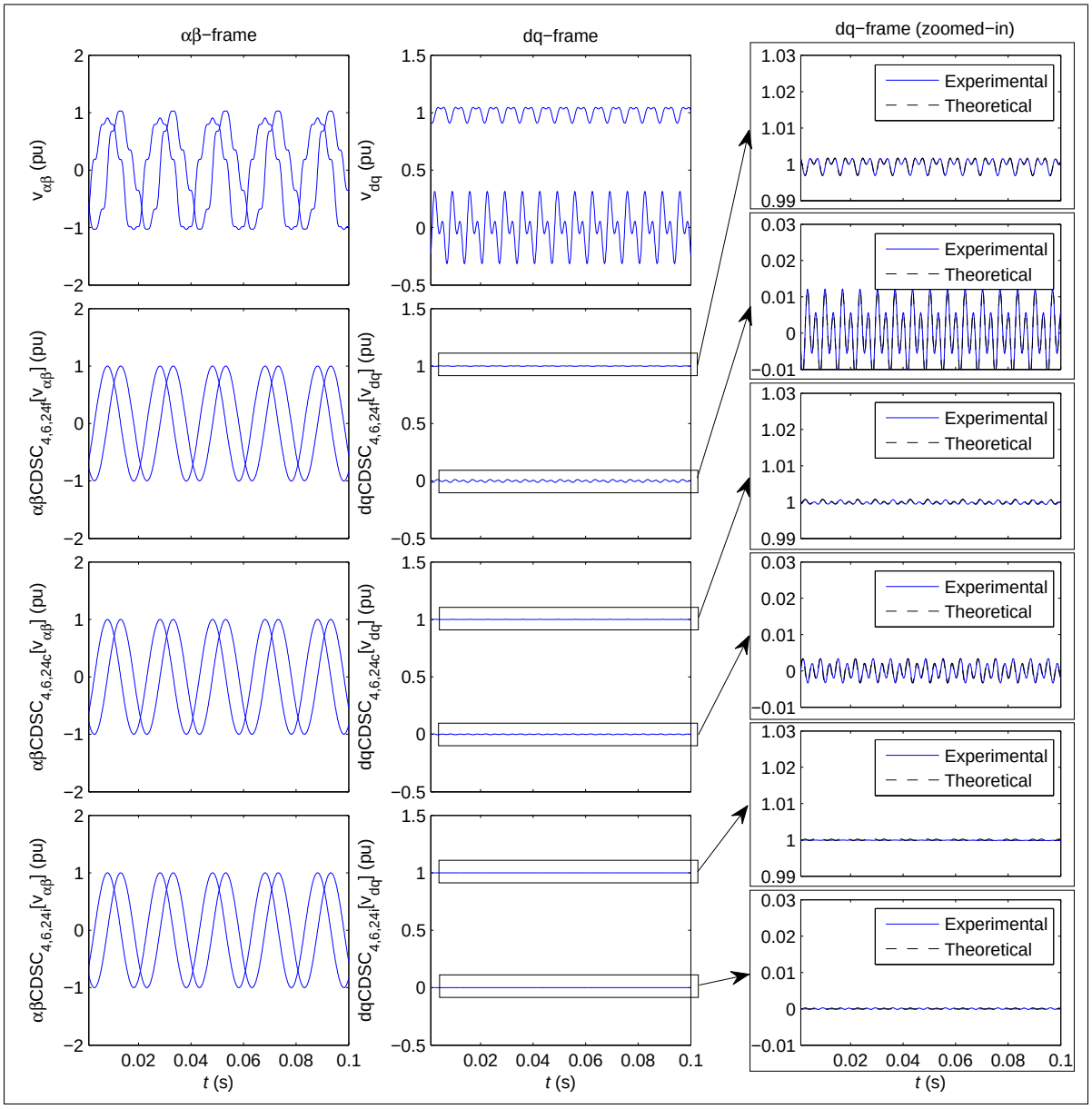


Figure 5.23: Theoretical and experimental voltage waveforms of the discretized DSC/CDSC operators in Test Case 1 (symmetrical harmonics vs. $\alpha\beta\text{CDSC}_{4,6,24}$ and $dq\text{CDSC}_{4,6,24}$). Subscripts 'f', 'c' and 'i' respectively refer to DSC/CDSC operation with round-down, round-up and interpolation settings.

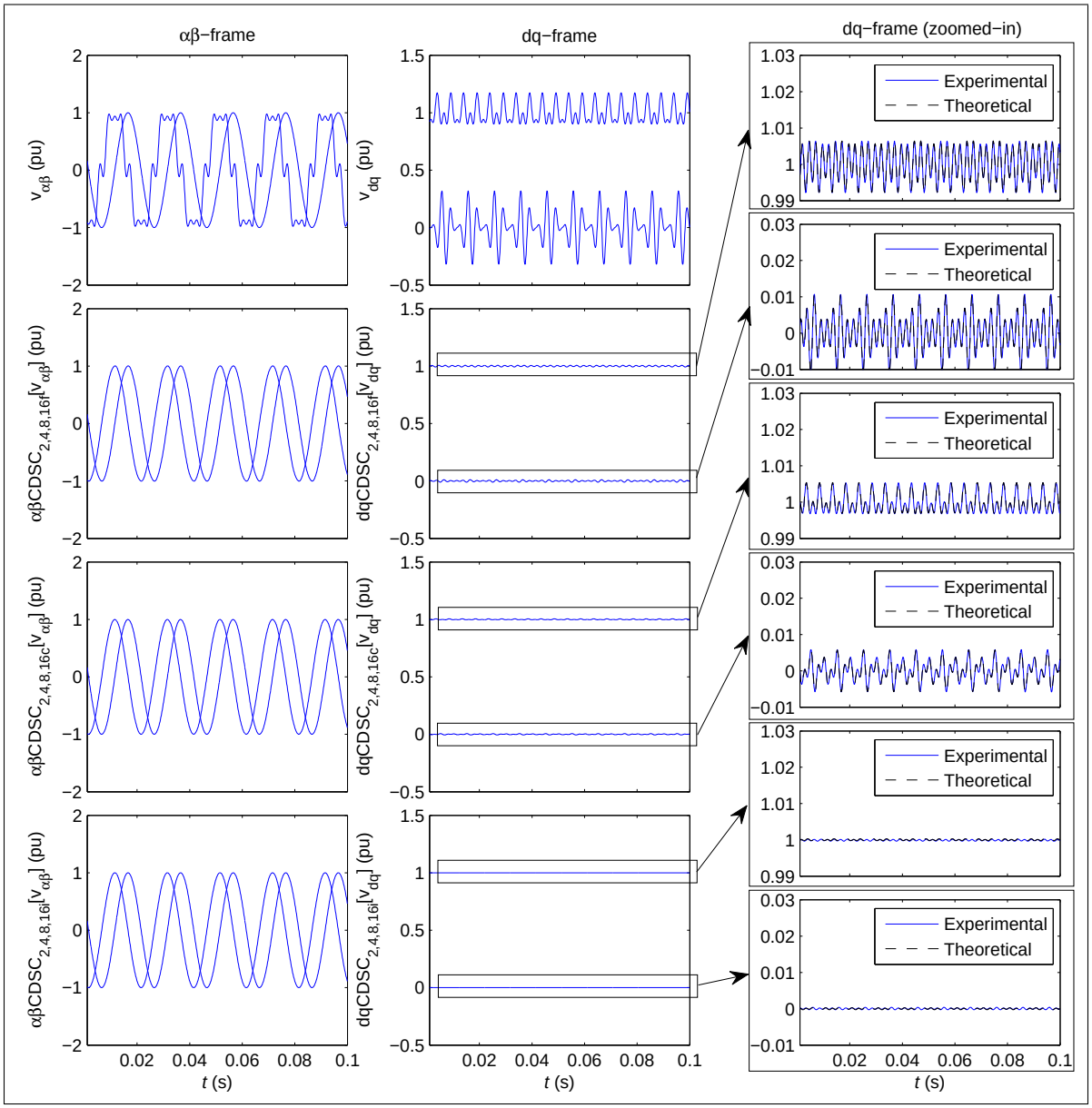


Figure 5.24: Theoretical and experimental voltage waveforms of the discretized DSC/CDSC operators in Test Case 1 (symmetrical and asymmetrical harmonics vs. $\alpha\beta\text{CDSC}_{2,4,8,16}$ and $dq\text{CDSC}_{2,4,8,16}$). Subscripts 'f', 'c' and 'i' respectively refer to DSC/CDSC operation with round-down, round-up and interpolation settings.

Figure 5.23 and 5.24 in turn present the results from Test Case 2 and 3. In the figures, $\alpha\beta$-frame waveforms in the left columns verifies that the selected $\alpha\beta$-frame CDSC operators can remove the corresponding symmetrical and asymmetrical harmonics, producing undistorted $\alpha\beta$-frame signals. At the same time, the zoomed-in dq-frame waveforms also confirm the effectiveness of the interpolation method. Furthermore, the consistency of the experimental results and the theoretical results proves the accuracy of the harmonic gain error analysis in this work.

5.6 Summary

This chapter first introduces the experimental platforms, especially the dSPACE platform, used in the research project. Details are provided on the composition of the platforms and the workflow to do experiments with them.

Subsequently, a section is dedicated to describe the structure and the features of the experimental models, including the model that serves as the virtual programmable power supply, and the models for the grid phase detecton CDSC-PLL, the selective harmonic detection CDSC-PLL, and the discretized $\alpha\beta$- and dq-frame DSC/CDSC operators.

For each model used in the experiments, several test cases are designed to subject the model to different disturbances, such as voltage unbalance and sags, harmonics, frequency variations, etc. Some test cases are the mixtures of them. The comprehensive experimental results obtained from these test cases are presented and analyzed, and they confirm that the proposed CDSC-PLL systems have met their respective design prospects.

Chapter 6

Conclusions and Recommendations for Future Research

This thesis investigates two problems of great significance in the control of power converters: the grid phase detection in the grid-connected operation of DG systems, and the harmonic detection in the control of harmonic compensation systems. The two problems are in fact associated with each other, as they are both related to the separation and detection of harmonic components in polluted voltage/current signals. Therefore, the solution to the two problems could be rooted in the same methodology, as confirmed by the outcomes of this research project.

In this chapter, Section 6.1 draws conclusions about the research project, and Section 6.2 makes a few recommendations for the future research.

6.1 Conclusions

This research project has lead to the development of the cascaded delayed signal cancellation phase-locked loop (CDSC-PLL) system, whose variants can satisfactorily address the two problems mentioned above. Besides that, there are also several other achievements, and they can be recaped here:

1. The grid phase detection CDSC-PLL system has been developed in form of the basic dq PLL system augmented by the proposed CDSC operator.

   (a) The CDSC operator, comprised of multiple delayed signal cancellation (DSC) operators con-

nected in series, can be configured to eliminate arbitrary harmonics. The extracted positive-sequence fundamental signal can then be used in the PLL loop for very fast grid phase detection with zero steady-state error. Compared with the many conventional PLL schemes, there is no need to compromise between the transient response and the steady-state accuracy.

(b) Both the dq-frame and the $\alpha\beta$-frame DSC and CDSC operators are developed and their relationships are fully studied. The derivation of the dq-frame operators is more straightforward, and hence provides a more convenient approach for parameters design. The obtained parameters can then be used to construct the $\alpha\beta$-frame operators, which has equivalent harmonic elimination ability, but avoids the in-loop delay issue.

(c) The CDSC operator can be flexibly configured using the parameters design approach to deal with different harmonic patterns. Two representative configurations are presented: one can eliminate a wide range of symmetrical harmonics, and the other can futher eliminate asymmetrical harmonics.

(d) Unlike the reviewed DDSRF-PLL and the DSC-PLL that uses quarter-cycle delay, the CDSC-PLL system considers both voltage unbalance and harmonics, and gives a unified solution to eliminate them.

(e) The CDSC operator does not utilize the estimated output as does the feedback-based PLL schemes, and so system stability is unconditionally guaranteed. The settling time can also be much shorter.

(f) The filtering-based PLL schemes usually employ 1st- or 2nd-order low-pass or band-pass filters. Compared with them, the CDSC operator is actually a high-order comb filter; that is why it has better harmonic elimination ability.

2. The selective harmonic detection CDSC-PLL system has been developed in form of multiple detection subsystems connected in parallel. The core of each subsystem is the renovated $\alpha\beta$-frame DSC/CDSC operator.

(a) The renovated $\alpha\beta$-frame DSC has more generality than the original DSC, and so it can elminate harmonics as well as the the fundamental signal.

(b) Compared with the conventional selective harmonic detection schemes (such as SDFT), the CDSC-PLL has much shorter settling time and smaller memory overhead.

(c) Differing from the synchronous reference frame filtering or hybrid reference frame filtering schemes, CDSC-PLL does not need the grid phase angle as an extra input.

3. A frequency adaptation mechanism, namely frequency feedback loop (FFL), is designed to use with the grid phase detection and the selective harmonic detection CDSC-PLLs. With this additional control loop, the delay intervals in the CDSC operators can be updated in real time, and so accurate harmonic elimination can be achieved even when considerable frequency variations take place.

4. The issues about the practical implementation of the proposed CDSC-PLL systems are also fully investigated. It is demonstrated how the control blocks and the CDSC operators can be discretized. The rounding effect is quantified with the concept of harmonic gain error, and an effective discretization error reduction method is developed from the linear interpolation theory. The method can benefit all signal delay-based PLL schemes.

5. Comprehensive experiments have been conducted to verity the performance of the CDSC-PLL systems with different configurations and under different working conditions. The developed virtual programmable power supply can produce very flexible three-phase voltage waveforms, and can be reused in many other harmonic study projects.

6.2 Recommendations for Future Research

The outcomes of this research project has also inspired some ideas for potential future research:

1. The presented CDSC-PLL system is currently limited to three-phase applications. However, grid phase detection and selective harmonic detection schemes are also in need for single-phase systems, such as single-phase DG and single-phase harmonic compensation systems [77]. Some existing single-phase PLL schemes delays the input signal by a quarter cycle using delay buffer [78], filters [79] or other transformations [78,80], and take the original and the delayed signal as the α- and the β-components as input for the basic dqPLL. Such an arrangement is valid when the single-phase input signal is ideally sinusoidal, but is often problematic when the signal is distorted. Other schemes consider to construct more advanced single-phase PLL schemes based on certain feedback loops [38, 39, 81–84], but they often encounter difficulty in terms of stability and efficiency when multiple harmonics exisit [85].

The CDSC-PLL can deal with single-phase signal, if the original distorted signal is used as the α-component, and a constant zero signal is used as the β-component. The resulted $\alpha\beta$-frame space vector can be seen as the vectorial sum of multiple conjugate harmonic vectors, whose β-components always cancel each other and hence keep to be zero. With a redesigned CDSC operator, all the undesired harmonics can be eliminated, and so the fundamental component (or any harmonic of interest) can be isolated.

2. A control model for the FFL is yet to developed. It is found that the derivation of a rigorous model is difficult, due to the high nonlinearity of the loop including CDSC blocks. [66] has proposed an approach to develop an approximate model by studying the averaged dynamics. In light of this technique, an approximate FFL model could be developed, which is meaningful to tune the FFL more accurately and gain better system dynamics.

3. The selective harmonic detection CDSC-PLL already features a very short transient time, but it could be further reduced. Currently, all the DSC operators are connected in series in the CDSC operator. Attempts have been made to rearrange the topology into a parallel structure, which is unsuccessful. It could be worthwhile to investigate a third option—a lattice-like topology, in which a row of the input signal and its different delayed versions are used in operations with a column of such signals. It can be inferred that, while all the harmonics can be detected respectively, the optimized arrangement of the operations could result in an even shorter overall delay. More research is needed on this hypothesis.

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Author's Publications

Several parts of the work and ideas presented in this thesis have been published by the author during the course of the research work. These publications are listed as follows.

IEEE Transactions

1. **Y. F. Wang** and Y. W. Li, "Three-phase cascaded delayed signal cancellation PLL for fast selective harmonic detection," *IEEE Transaction on Industrial Electronics*, 2011 (*In Press*).

2. **Y. F. Wang** and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Transaction on Power Electronics*, 2011 (*In Press*).

3. **Y. F. Wang** and Y. W. Li, "Analysis and digital implementation of cascaded delayed signal cancellation," *IEEE Transaction on Power Electronics*, 2011.

IEEE Conference Proceedings

4. **Y. F. Wang** and Y. W. Li, "Fast selective harmonic detection based on cascaded delayed signal cancellation PLL," to be presented at *2011 IEEE Energy Conversion Congress and Exposition*, Phoenix AZ, Sept. 17–22, 2011.

5. **Y. F. Wang** and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," presented at *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta GA, Sept. 12–16, 2010.

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