Increasing Organic Photovoltaic Device Efficiency Through Microstructuring Techniques

by

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Abstract

Organic photovoltaics offer the tantalizing possibility of inexpensive renewable energy generation. However, there are many issues that need to be solved before organic photovoltaics can see widespread use. One main issues that needs to be resolved is the relatively low efficiency of organic photovoltaics, which increases the cost per watt for the cells. Increasing efficiency of organic photovoltaics would therefore offer a possible avenue for their commercial adoption. This thesis explores the hypothesis that decoupling electrical carrier collection and light absorption in organic photovoltaics would allow for increased photoconversion efficiency. A model was created to test the feasibility of this concept. The model informed the fabrication of a prototype device using microfabrication techniques to test the hypothesis. Numerous fabrication steps were optimized, including mask design, photolithography, etching, thermal oxidation, glancing angle deposition, and polymer spinning. Severe issues were resolved in the photolithography, glancing angle deposition, and polymer spinning processing steps. The highest performing device achieved a 0.6% photoconversion efficiency and a fill factor of 0.25, with a carrier collection distance of 1.0 μm and a light absorption distance of 2.2 μm. For these device characteristics, the model predicted an efficiency of 0.63%, demonstrating good agreement between the model and the prototype device. The thesis concludes by suggesting additional processing steps and methods to further test the hypothesis.

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List of Symbols

A	Cross sectional area of an electric short
A_λ	Optical density
α	Deposition angle
$\alpha(\lambda)$	Absorption coefficient
β	Inclination angle of thin film posts
EQE	External quantum efficiency
FF	Fill factor
φ	Rotational angle of substrate during deposition
$\varphi(\lambda)$	Spectra of the incident light in units of photons s^{-1} cm^{-2} nm^{-1}
IQE	Internal quantum efficiency
IQE(w)	Charge extraction distance dependant internal quantum efficiency
I_{sc}	Short circuit current
I_0	Incident irradiance
I(z)	Transmitted irradiance through material thickness z
J_{sc}	Short circuit current density
L	Light absorption length OR Length of electrical short
η	Photoconversion efficiency
η_{CC}	Charge capture efficiency
$\eta_{CT}(w)$	Charge extraction distance dependent charge transfer efficiency

η_{ED}	Exciton dissociation efficiency
λ	Light wavelength
P	Power
q	Elementary charge
R	Reflectance OR Resistance
$r(\lambda)$	wavelength dependent reflection coefficient
ρ	Resistivity
T	Transmittance
t	Charge extraction distance
V_{oc}	Open circuit voltage
z	Material thickness

Chapter 1: Introduction

1.1 The Need for Clean Energy

The reduction of greenhouse gas emissions is seen as one of the major hurdles humanity faces in the coming century. The continued release of these gases will accelerate and add to the overall amount of climate change that the world will experience. Greenhouse gases are emitted primarily from three main sources: gasoline and diesel combustion for transportation (16%), the combustion of a wide variety of fuel sources for manufacturing and industrial processes (20%), and the combustion of natural gas and coal for electrical power generation (38%) [1]. In light of this problem, a large amount of work is being done to develop solutions that solve the greenhouse gas emission issue at its source. For example, to eliminate vehicular greenhouse gas emissions, electric and hybrid vehicles are starting to be developed by many car manufacturers. Many major car manufactures have electric vehicles on the market or under development such as Tesla Motors, General Motors, Nissan, and Ford [2].

Unfortunately, switching to all electric vehicles does not completely solve the issue of greenhouse gases when it comes to vehicles. As long as fossil fuels are burned to produce electricity, all electric vehicles will emit greenhouse gases through their operation. Therefore, it is especially important for electricity generation to become entirely fossil fuel free, not only because it is the largest producer of greenhouse gases, but also because it will allow for the elimination of greenhouse gas emission in road transportation. Fortunately, there are many renewable power generation sources under development or currently in large-scale use.

Wind power's use is currently small but is experiencing strong growth and is starting to penetrate the power generation market in significant levels in certain areas [3]. Hydroelectric power is the only renewable energy source with large market penetration, taking up roughly 18% of the worldwide generation as of 2012 [4]. Geothermal power has a very small market share, mostly due to the fact that it is currently limited to areas that have thermal hot springs [3,4].

Solar energy generation involves generating electricity directly from sunlight, the fundamental power source for the whole planet. Theoretically, it offers great potential as a partial solution to the renewable power generation dilemma. There are two main categories of solar

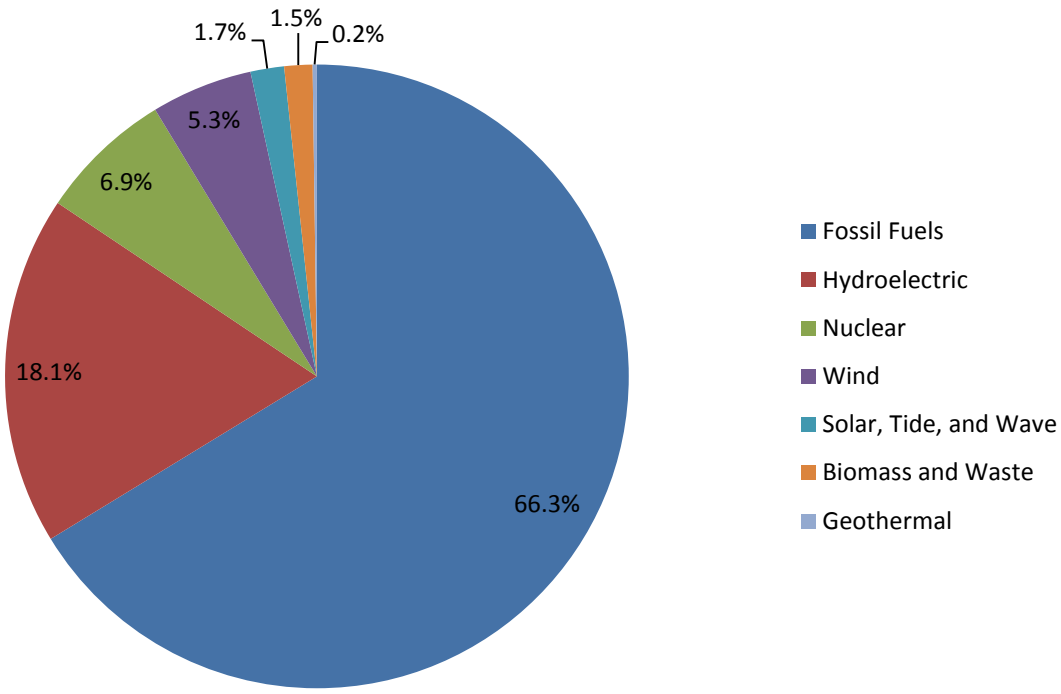


Fig 1.1 – Worldwide power generation by source in 2012 [4]

power generation: solar photovoltaic and solar thermal. Solar thermal in most instances involves using sunlight to heat a working fluid to spin a turbine connected to a generator. Solar photovoltaic (PV) on the other hand directly converts light into electrical energy. Solar PV has a much lower overall cost [5] than solar thermal and is more likely to achieve large market penetration in the near term.

Solar PV has so far not achieved a very large market share [6]. This is due to a variety of technical, social, and institutional issues that have historically plagued the solar industry such as cost, power intermittency, lack of standards and installers, subsidies, and aesthetics. Of course the most important issue to solve out of all these issues is cost. If there is no economic incentive to use solar power, it will not be used except for those who are motivated from an entirely environmental point of view.

Currently the use of photovoltaic power on a transmission scale is not yet economically feasible without significant government subsidies due to the high cost of photovoltaic modules [4]. The cost of a residential solar PV installation is viable in certain locations in the world, but on a global basis is still not fully realizable without subsidies. Thus, there is a great deal of effort and focus to reduce the costs of a full solar PV installation. There are three main methods being explored to reduce the cost: reducing the overall material costs of the modules themselves,

increasing the efficiency of the cells to produce more power per panel, and reducing the so-called balance of system costs of the installation, such as the cost of grid connection and labour.

The most cost effective source of solar power is currently the crystalline silicon technology system. This system has, without a doubt, the lowest cost on a dollar per watt basis is the best metric at evaluating the performance of a solar generation method [7]. This is due to its combination of relatively high efficiency at ~20% and, in some cases, a long operating lifetime, up to 25 years [8]. The fundamental limit to the cost of this technology system is the cost of the purified crystalline silicon and the amount required for the cells. Although the price of solar grade polysilicon has decreased in recent years, driving a reduction in panel price, the process to make solar-grade silicon is still highly energy intensive and relatively expensive [9].

The high temperatures required for purification of the silicon is the main driving force of solar-grade polysilicon cost. The Siemens process, which is the state-of-the-art solar-grade polysilicon manufacturing process, requires temperatures reaching 900 °C and a cold wall furnace, multiple distillations of trichlorosilane, and pre-existing silicon rods for the gas to deposit on [10]. The high energy requirements and technical challenges of the Siemens process put a limit on the fundamental cost of polycrystalline silicon solar panels, which could limit the use of solar energy generation in areas where subsidies do not exist.

Given the possibility that silicon based systems may never be competitively viable in the certain energy generation marketplaces, different material systems are being considered for solar energy generation to reduce overall cost, such as thin-film technologies like CdTe [11], perovskite-based solar cells [12], and organic-based photovoltaics [13].

1.2 The Potential of Organic Photovoltaics

Organic photovoltaic (OPV) devices offer a plethora of potential advantages for reducing the cost of solar energy generation. These devices use a mixture of various organic polymers and/or small organic molecules as their active absorbing layer, which is the main source of the potential advantages. These organic active layers are, first of all, much cheaper to produce than solar-grade polysilicon, or any other materials system for that matter [14], due to the fact that they are made from readily available elements like carbon, oxygen, nitrogen, hydrogen and

sulfur. They can be made using batch chemistry and are readily available from chemical suppliers [14]. Not only is the material less expensive, the organic layers are strongly light absorbing over a large portion of the visible spectrum and require only a very thin layer to absorb most incoming light. The exact thickness required depends on the polymers and molecules being used, but it is usually on the order of one hundred to two hundred nanometers, thousands of times smaller than the thickness of a typical silicon solar panel [14]. The combination of the inexpensive raw materials and the thin layers enables the extremely low material cost of OPVs.

The general malleability of polymers, along with the thin nature of the absorbing layers, also provides another advantage for OPVs, namely that they can be deposited onto thin, flexible, lightweight substrates [14]. This allows for OPVs to be used in a variety of orientations and shapes that are not attainable by rigid crystalline solar panels, such as silicon based systems. The more flexible forms allow for more favourable coverage of nonrectangular architectural features, ensuring that south facing portions of nearly any structure can be made photovoltaic. This is very important for solar energy generation as the south facing portions of a structure receive the most solar insulation in the northern hemisphere. The lightweight nature of the substrates also reduces the cost of installation as they require less structural support and less heavy lifting to install onto surfaces. Transportation costs are also lower due to the fuel savings of a lower weight cargo. The thinner sheets allow for better cargo packing as well. In addition, this tight packing enables lower storage costs as they take up less warehouse space than traditional silicon solar panels.

The fact that the cells can be made on flexible substrates allows for great cost savings during cell production. The cells can be made in a roll-to-roll production method, a method that allows continual plant operation [15]. The cells can be fabricated by continual deposition of the layers that make up the cell as the substrate moves through the production line. Even the active absorbing layers can be deposited in a roll to roll method, as the organic nature of the absorbing layers allows them to be solvated and sprayed onto the substrate [16]. All of the layer deposition techniques are relatively low temperature (~100 °C) and thus the production line requires much less energy to produce the cells compared to crystalline based systems, a significant cost saving [15]. These coating techniques have the added benefit of reducing the amount of wasted layer materials as roll-to-roll coating systems can be set up to primarily deposit only on the substrate. The roll-to-roll production method, as well as the flexible substrates, allows for extremely easy

sizing and resizing of the cells so that the length and width of the installation can be taken into account at a production level. This allows solar installation designers greater flexibility for optimizing energy production.

Numerous possible polymers and organic molecules that could be used for organic photovoltaics offers the potential for distinct advantages for adaptable solar energy generation [14]. The active materials of the cells can be optimised for particular lighting and environmental conditions in different parts of the world. A cell that performs well in dry, hot conditions and under direct sunlight could be made for places like southern California or northern Africa, while a cell that performs better under indirect illumination and more temperate climates, such as the United Kingdom, could also be developed. This flexibility allows for the possibility of maximum achievable cost per watt to be obtained for every area of the globe. The variety of potential active layers will also enable new architectural features to be included into building designs [17]. Cells can be made to be semi-transparent with different colouring tints to cover windows and give rooms and spaces various aesthetic touches.

1.3 Project Motivation

Given the number of potential cost advantages OPVs have over the status quo of silicon-based systems there must be obvious downsides that reduce their economic viability. As stated earlier, silicon-based systems offer the best dollar per watt power generation out of any materials system. There are two large cost inducing problems with OPVs, both of which are areas of significant research. The first issue is that OPVs tend to degrade very rapidly compared to silicon and other crystalline solar cells [18]. While a silicon solar panel can have a useful lifetime of up to 30 years, the vast majority of OPV systems can last at most 2.5 years [18]. This requires OPV installations to be replaced much more often, adding significant labour costs for long-term installations.

The cause of this degradation comes from two major sources, both of which are largely ubiquitous and, therefore, a significant engineering and design challenge. Firstly, molecular water vapour and oxygen in the air can diffuse through many standard layers in an OPV device [19]. The sensitive active layer and interfacial layers will be degraded by the presence of these molecules, throwing off the careful electrical balance of the layers over a relatively small amount

of time, on the order of days for most polymer systems [19]. This will drop the efficiency of the cells below 80% of their original value, the standard definition for the lifetime of solar cells. The solution used so far for this problem is to add a final transparent encapsulation layer around the cells to reduce the diffusion of molecular oxygen and water vapour into the cell [19]. This extra layer adds material and production costs to the OPV cells. Because the cells are so sensitive to these gasses, this also calls for anaerobic and dry conditions during production, incurring a significant cost to the fabrication of the cells.

The second cause of degradation is from UV light in the solar spectrum [20]. UV light will cause photochemical bleaching in many OPV material systems, reducing the absorbance of the polymers and organic molecules to all incoming visible light [20]. Since the cell's active layer can absorb less light as exposure to UV light continues, the cell's efficiency will naturally degrade over time until the cell is no longer a useful energy source. Adding protective layers to the cell to block or reflect the UV light can help increase lifetime, and is an area of active research. Again these extra layers add production costs and a cost-benefit analysis must be done to ensure the cost of adding the extra layer is offset by the improved lifetime of the cell.

The other main cost inducing problem is the relative lack of efficiency of OPVs. The current world record for efficiency for an OPV device is 12%, held by Heliatek [21]. Compare this with the world record silicon solar cell, held by Panasonic, of 25.6%, more than double the efficiency [22]. Not only is there a large efficiency difference, the silicon cell world record was achieved over an area two orders of magnitude larger, as the silicon cell was 143 cm^2 while the Heliatek OPV cell had an area of 1.1 cm^2 [21,22]. The large difference in areas shows that the high efficiency silicon cell is can be produced easier on a commercial scale compared to the OPV cell. The OPV cell requires significantly more scale up to cover large areas.

Increasing the efficiency of cells has a strong effect on decreasing the dollar per watt of cells, as it directly increases the amount of watts produced by the cell during its operation. It is therefore no surprise that increasing the efficiency of OPVs is one of the largest areas of study for this burgeoning field [23]. A variety of methods are being examined for increasing efficiency including developing new active layer materials, new interfacial layers to increase charge extraction and other electrical properties, and entirely new device architectures. The latter approach has been shown to bear great fruit recently, as the record setting device made by

Heliatek is a non-standard design [21]. Given that new architectures could offer increased efficiency, and therefore lower dollars per watt for OPVs, this avenue of research begs for greater attention.

1.4 Project Scope

Changes in architecture could potentially increase efficiency for OPV devices because different device architectures can overcome a fundamental issue with the standard OPV cell design. Normally, the absorbing layer of a cell is sandwiched between two electrical contacts, one of which is transparent to let incoming light reach the organic absorbing layer [24]. If the absorbing layer is made maximally thick to absorb as much light as possible, the electrical carriers have to navigate a larger distance to get to the contacts. Electrical carriers have very short mean lifetime in the organic absorbing materials before they recombine, producing heat [25]. Therefore, there is a classic engineering trade off with standard cells. Making the absorbing layer very thin to increase carrier collection will lower the amount of light absorbed and thus lower efficiency, while making the absorbing layer very thick will increase light absorption but lower carrier collection and thus also lower efficiency. New architectures could solve this problem by decoupling the light absorption thickness and the carrier extraction distance. To do this would require that charge collection occurs orthogonally to light absorption, instead of parallel to light absorption as in the current standard design.

There are many possible designs that could do this, but the simplest device that would test the achievability of this concept is a rectangular trench based design in which metal contacts are placed onto either side of a thin microfabricated, insulating trench, that is then filled with the absorbing layer. This can be seen in figure 1.2 on the next page. The light absorption could be increased by increasing the depth of the trench, while the carrier collection could be increased by making the trench thinner. By changing these two variables the viability of charge collection and light absorption decoupling can be tested to determine if it is a valid approach to increasing the efficiency of OPV cells. This thesis will explore the modelling, fabrication, and characterization of such devices.

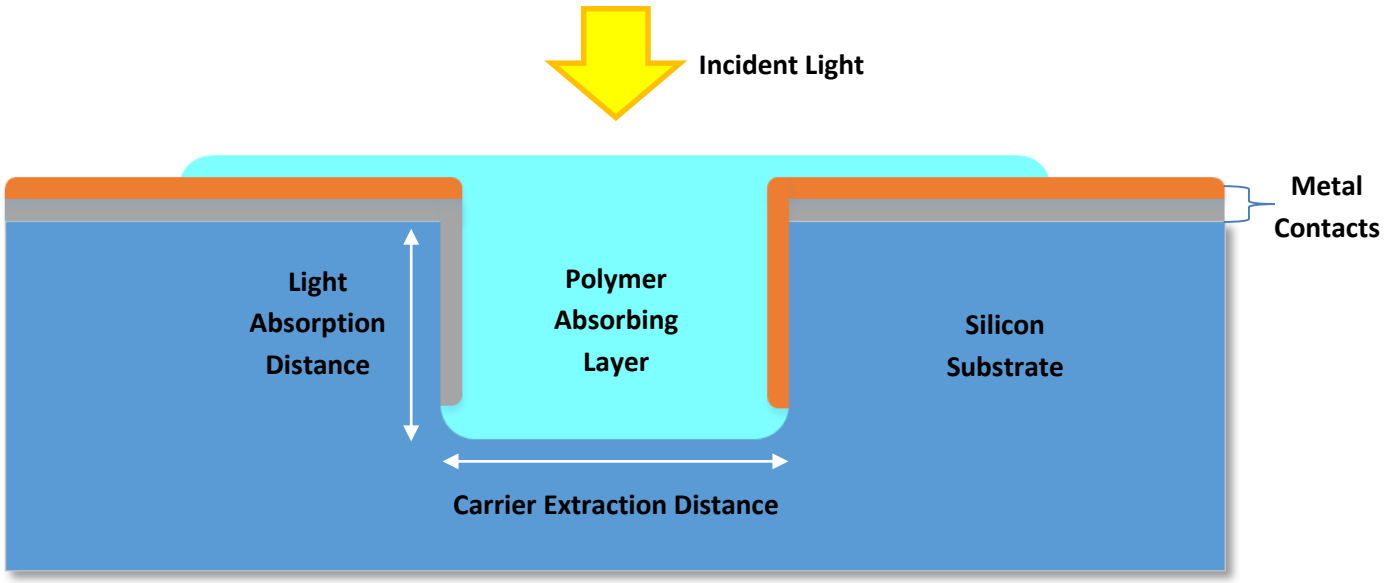


Fig 1.2 – Cartoon image of proof of concept OPV device.

Chapter 2: Background

2.1 Basic Principles of Photovoltaic Cells and Figures of Merit

The vast majority of photovoltaic systems are made from semiconducting materials to exploit their unique electrical properties [26]. In semiconductors, incoming photons of sufficiently high energy, will be absorbed by an atom through a change in one of its electron's energy levels. In the process of photon absorption the electron moves into a higher unoccupied energy state. This higher energy state allows the electron to move around the material instead of being locked down to an atom, thus allowing it take part in conduction processes. The energy state that was previously occupied by the electron becomes a 'hole,' which acts as a positive charge carrier. The hole is also mobile because electrons will tunnel from a similar energy state into the empty state, 'moving' the hole to where the tunneling electron was previously. This process is analogous to a bubble moving in a liquid, where the bubble (the hole) moves because the liquid (the surrounding electrons) moves into its location. Holes and electrons have a finite lifetime in the semiconductor if not acted upon by outside forces; they will annihilate each other in a process called recombination. When an electron and hole meet, the electron will 'fall' back into the lower energy state of the hole. The energy gained by absorbing the photon will be released as thermal energy, wasting the photon's potential to generate useful electrical current.

Thus, for a semiconducting-based photovoltaic device to successfully turn light into electrical current, it must separate the electrons and holes before they recombine. It must not only limit recombination but also ensure that the two device contacts only receive primarily one carrier type, hole or electron. Otherwise there will be no net current flow and, thus, no power generation. The primary way of doing this is to use two different semiconducting systems together in the same device [27]. At the interface between the two semiconductors, holes and electrons are separated so that electrons are the majority carrier in one of the semiconductors and holes are the majority carrier in the other. To ensure a net current flow, each semiconductor is connected to its own separate contact. The way the hole and electron separate at the interface depends on the semiconducting system used, as will be seen later when comparing organic and inorganic photovoltaics.

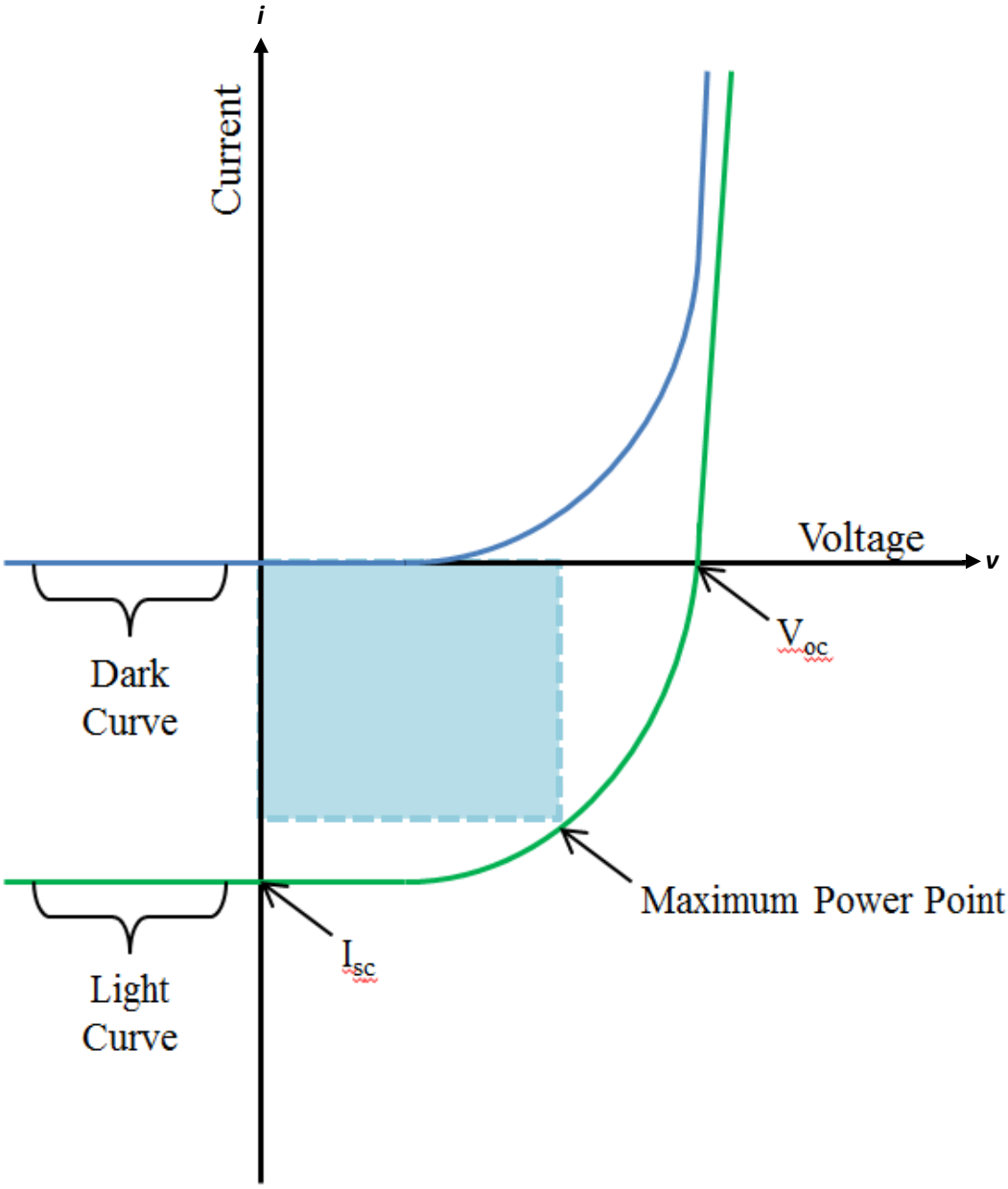


Fig 2.1- Current vs. voltage characteristics of a typical solar cell

The best performing photovoltaic devices have an exponential *i-v* behavior [28]. Since the power generated by a cell is a product of its current and voltage, the maximum power point on the exponential curve lies near the 'knee' of the curve as seen in figure 2.1. The exponential behavior of these cells allows the photoconversion efficiency of a cell to be described by the following formula:

$$\eta = \frac{V_{OC} I_{sc} FF}{P} \qquad (1)$$

Voc is called the open-circuit voltage and is the voltage generated between the contacts when no electrical load is placed on the cell. I_{sc} is called the short circuit current and is the current measured when the two contacts of the device are connected via a strong conductor. P is the total power of all incoming light incident on the cell. FF stands for fill factor and is the ratio of the power generated at the maximum power point and the product of V_{oc} and I_{sc}. The fill factor is represented visually in figure 2.1 by the ratio of the shaded rectangle to the not-shown rectangle defined by V_{oc} on one corner I_{sc} diagonally adjacent to it. The product of V_{oc} and I_{sc} is the ideal maximum power point corresponding to an infinitely sharp exponential curve. The higher the fill factor, the more ideal the cell behavior. V_{oc}, I_{sc}, and FF are commonly used figures of merit when comparing the performance of different cells.

Another common figure of merit used when discussing solar cells is the quantum efficiency, which is defined as the average number of electrons generated for each incident photon on the cell [29]. The quantum efficiency can be separated into two different concepts, the internal quantum efficiency (IQE) and external quantum efficiency (EQE). The product of all the efficiencies of processes that occur inside the cell defines the internal quantum efficiency and is a measure of the number of electrons generated for each photon that reaches the absorption layer of the cell. The number of steps and their efficiency depends on the material system and cell structure. Typical efficiencies include absorption efficiency, efficiency of carriers reaching the semiconducting interface before recombination, efficiency of carrier separation at the interface, and efficiency of reaching the contacts after separation. The external quantum efficiency additionally takes into account reflective and transmissive losses of the cell and is defined as follows:

$$EQE = IQE(1 - R - T) \qquad (2)$$

Where R is the reflectance and T is the transmittance of the cell. External and internal quantum efficiency are best understood when looked at spectrally, as they can vary greatly depending on the wavelength of incoming light.

2.2 Inorganic photovoltaics

Inorganic photovoltaics are primarily made from crystalline semiconducting systems such as silicon and gallium arsenide [30]. The crystalline nature of these semiconductors gives

rise to a valence band, a band of energy states where the vast majority of immobile electrons reside. It also creates a conduction band, a sparsely populated band of energy states, higher in energy than the valence band, where electrons are free to move around the crystal. The valence band and conduction band are separated by a band of forbidden energy states. The difference in energy between the most energetic state of the valence band and the least energetic state of the conduction band is what is called the band gap. Incident photons of energy greater than or equal to the band gap on the semiconductor will be absorbed by valence band electrons to jump them to the conduction band, leaving a hole in the valence band. This photon absorption process completely dissociates the hole and electron, which are now free to move around the crystal.

Inorganic crystalline semiconductors have a very useful property in that their conduction can be controlled greatly by the addition of impurities called dopants [31]. P-type dopants create an excess number of holes in the semiconductor while n type dopants create an excess number of conduction electrons in the semiconductor. What impurities coincide with n-type or p-type depends on the semiconductor being used. Creating a junction where n-type and p-type semiconductors meet is the basis for inorganic photovoltaics, and forms the meeting of the two semiconducting systems mentioned in section 2.1 [32]. The p-n junction, as it is known, creates a depletion region where few free carriers exist, which sets up a built-in electric field across the depletion region. This electric field, corresponding to a built-in voltage, is generated by the proximity of fixed dopants of opposite charge on either side of the junction that are no longer offset by free carriers. This electric field is the key to separating the electrons and holes in inorganic photovoltaics.

When a photon creates an electron and hole on either side of the junction, minority carriers diffuse through random thermal motion towards the depletion region [32]. The average distance a minority carrier will travel in the semiconductor before recombination occurs is called the diffusion length. Carriers that are not generated within a diffusion length of the junction will not be collected by the cell. Once minority carriers reach the junction, they are swept across the depletion region by the built-in electric field. Then, they are free to diffuse toward the contacts that are connected to either side of the pn-junction to perform useful electrical work.

Silicon is the most widely used inorganic semiconductor for photovoltaic applications due to its electrical and optical properties, and its wide availability, making it the most cost

efficient photovoltaic system. However, some of these properties are not ideal for making a solar cell [33]. It is the semiconductor most easily made with high purity and crystallinity, lowering the defect density that can enhance recombination [34]. It is also easily doped to form p-n junctions through processes developed in the fabrication of microelectronics. Common n-type dopants for silicon are phosphorus and arsenic, while the most common p-type dopant is boron. Aluminum is used in some cases as a p-type dopant as well [31]. The main property of silicon that makes it non-ideal in forming solar cells is that it is an indirect band gap semiconductor [32]. For an electron to be promoted from the valence band to the conduction band it must not only change its energy, but also change its momentum. Therefore, when an electron absorbs a photon to change its energy, it must nearly simultaneously absorb a phonon, a quantum of lattice vibration, to change its momentum. If phonon absorption does not occur, the photon is re-emitted. This makes the creation of a valence band electron a three-particle process, greatly reducing the likelihood of photon absorption occurring compared to a two-particle process. Hence, to absorb all the light incident on the cell, the silicon layer needs to be on the order of 100 μm thick, increasing the distance that electrons and holes need to travel to reach the junction.

2.3 Organic photovoltaics

Organic photovoltaics (OPVs) are also based on semiconducting systems; however the semiconductors are organic and, thus, have different properties. Unlike inorganic systems, the absorption of light does not create a freely conductive electron and hole. The electron and hole are attracted to each other through coulombic attraction and, therefore, are tightly bound to each other to form a quasiparticle called an exciton [35]. The exciton will diffuse through the organic semiconductor and recombine after an extremely short period of time.

The semiconductor interface that seperates the electrons from the holes in OPVs is fundamentally different from that of inorganic photovoltaics. Instead of having a single semiconductor doped with different impurities to form a p-n junction, two entirely different organic semiconductors are used [36]. The interface between these two different materials is called a heterojunction. Each organic semiconductor has its own bandgap but, instead of a valence band and conduction band, the band gap exists between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). For the organic

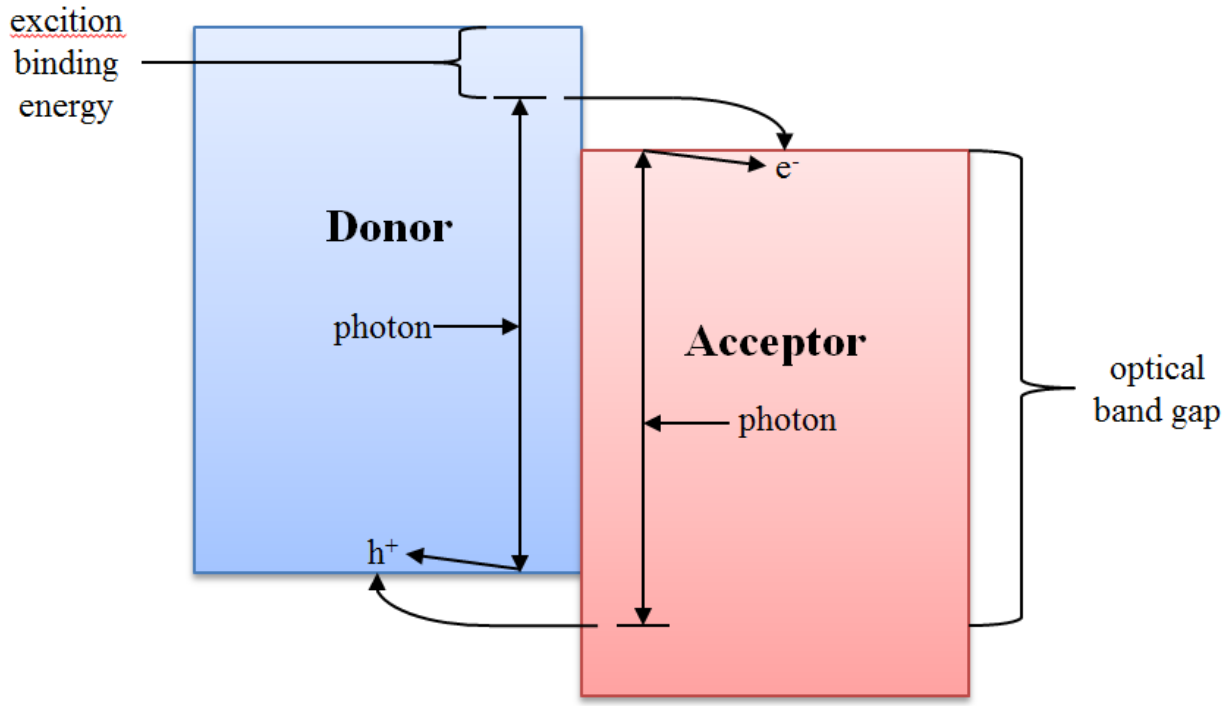


Fig 2.2- Band structure of a basic organic photovoltaic device

heterojunction to successfully form a photovoltaic cell, a difference in energy levels between each semiconductor's LUMO and HOMO must exist. The difference between these energies must be larger than the exciton binding energy otherwise the exciton will fail to dissociate at the interface. The organic semiconductor with the lower energy HOMO and LUMO has a higher electron affinity. It is energetically favourable for electrons to be swept into this semiconductor, defining it as the electron acceptor, or 'acceptor' in short. The other semiconductor is the opposite; holes will preferentially be swept into it, and, thus, is known as the electron donor, or 'donor' for short.

In their simplest form, OPVs consist of a bilayer of distinct organic semiconductors with a flat interface parallel to the contacts [36,37]. Excitons generated in either layer will diffuse toward the interface for dissociation. The problem with this design is that the exciton diffusion length in many semiconducting polymers is extremely small, on the order of 10 nm [38]. This limits the thickness of the cell absorbing layer to the same order to obtain the highest efficiency. A cell with an absorbing layer so thin will reflect or transmit a large amount of the incident light, greatly reducing the cells efficiency.

While the exciton diffusion length is very small in organic semiconductors, the free carrier diffusion lengths are often an order of magnitude higher [39]. This allows the design for a bulk heterojunction OPV. A bulk heterojunction is where the electron donor and acceptor are mixed together into a polymer blend where domains of the donor and acceptor spread randomly around the mixture. The domain size is controlled through an annealing step after the polymer

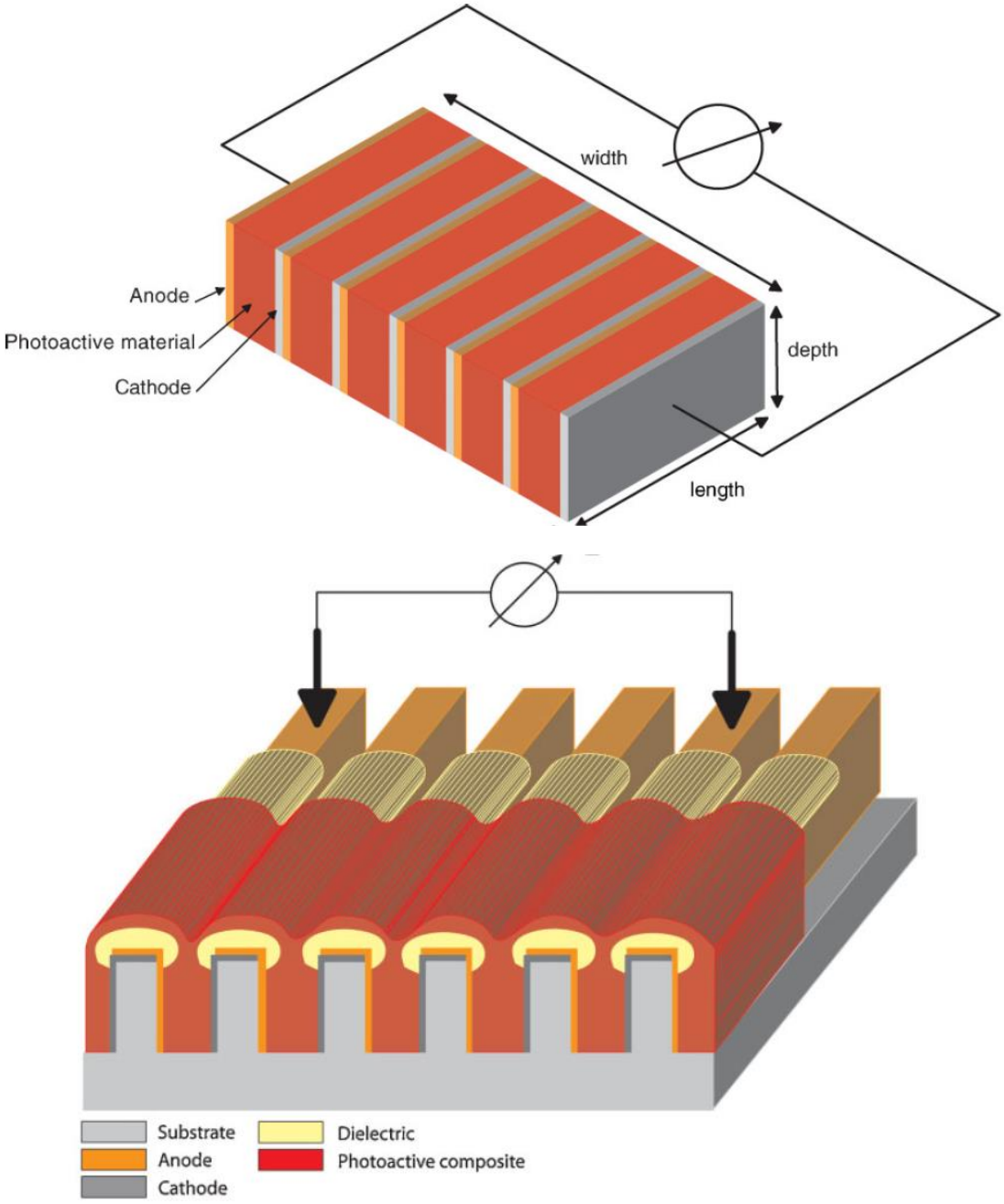


Fig 2.3- Cartoon image of series connected multicell OPV device from Niggeman et al. [40]

deposition. If the domain size is smaller on average than the excition diffusion length, most excitons generated in the absorbing layer will dissociate as they are always very close to the donor-acceptor interface. The now-free electron and hole can then diffuse toward the contacts for collection. This allows the absorbing layer thickness not to be limited by the exciton diffusion length, but by the free carrier diffusion lengths. Hence, the absorbing layer can be made an order of magnitude thicker for a bulk heterojunction cell compared to a simple bilayer cell. The greatly increased thickness of the absorbing layer allows for the majority of light across the visible spectrum to be absorbed.

2.4 Light Absorption and Carrier Collection Decoupling

The standard OPV cell has the carrier collection distance and light absorption distance coupled. Decoupling these two variables by using contacts perpendicular to light absorption could allow for efficiency gains, as discussed further in the next chapter. The use of vertical contacts to decouple light absorption and carrier collection in organic photovoltaics has been previously studied in the literature by Niggemann et al. [40-41]. The most recent use of vertical contacts for OPVs came in 2008 when a multiple trench-based OPV device was used to generate extremely high photovoltages [40]. This device consisted of thousands of OPV cells connected in series, with 1390 cells per mm. Interference lithography defined trench widths of 400 nm with a period between trenches of 720 nm in photoresist. This structured photoresist was then electroplated with nickel to create a nickel stamp. This stamp served as a master to form copies of the nanostructure in a UV curable photopolymer and had a trench depth of 400 nm. The depth of the trench was increased to 1 μm in the polymer copies by covering the tops of the fins in 8 nm of chrome and 30 nm of gold via glancing angle deposition (GLAD) at $\alpha = 80°$ to form an etch resist and followed by an argon sputter etching. The anode (Ti) and cathode (MoO_3) were then deposited by GLAD to coat opposite sides of the trenches and the tops of the fins to form the series connection between cells. LiF caps were added to the tops of the fins also via GLAD to help prevent recombination of carriers occurring between the cells. Poly(3-hexylthiophene-2,5-diyl):Phenyl-C61-butyric acid methyl ester (P3HT:PCBM) was then spun into the trenches at 400 rpm using tetraline as the solvent. The polymers were then annealed at 110°C for 10 min. The device achieved an extremely high V_{oc} of 880V, an I_{sc} of 19.9 nA, a FF of 0.25 and an extremely low η of 0.008%.

Another multiple-trench device was fabricated earlier by Niggemann in 2005 using the same nickel stamp [41]. This again resulted in a nanostructured polymer substrate with 400 nm wide and 400 nm deep trenches with a period of 720 nm. Instead of forming a series connection between individual cells within the trenches, the contacts were deposited in such a way to form an interdigitated electrode system. LiF was deposited at $\alpha = 80°$ using GLAD to form a lift-off layer on top of the fins. Gold and titanium were then deposited using GLAD to coat either side of the trenches to form the contacts, while shadow masking was used to create the contact pads. The lift-off layer was then removed through repeated adhesive exfoliation. P3HT:PCBM was then finally spun into the trenches to form the cell. This cell had V_{oc} 380mV, J_{sc} 0.05mA/cm^2, FF 0.25, and efficiency 0.05%.

These devices are ground-breaking realizations of the concept of decoupling light absorption and carrier collection, but the devices could be improved upon in several ways. First, there has been no modelling done of this kind of structure to estimate what kind of device architecture would result in the highest efficiencies. Without this modelling to inform the design of the device, it is unknown whether the efforts to increase trench depth and lower trench width will result in significantly enhanced efficiencies. Second, these devices' absorbing layer is actually relatively thin. In the series-based device the depth of the trench is 1 μm but the absorbing layer filling the trench is approximately 150 nm thick. For the interdigitated electrode device, the depth of the trenches is only 400 nm. A bigger issue with the interdigitated electrode is that the aspect ratio of the trenches is unity, meaning there is no advantage in having the trenches at all when looking at it from an electrical performance perspective. Finally, the efficiencies of these devices are extremely low due to a combination of factors, leaving a great deal of room for improvement.

Chapter 3: Modeling and Device Process Flow

3.1 Modeling Carrier Collection and Light Absorption Decoupling*

Most organic semiconductors used for OPVs are optimized to absorb in the 400 nm to 600 nm part of the solar spectrum, as making fully broadband absorption is difficult with organic polymers [42]. This optimization is made because this wavelength range is the most intense part of the solar spectrum, as can be seen in figure 3.1. The data for this figure was obtained from the ASTM standard G-173-03 and was plotted by the author. Since conventional OPVs have a very thin active layer there is little power gained in wavelength ranges that are not strongly absorbing, specifically the red and infrared parts of the spectrum. There is still significant solar power present in these wavelength ranges and thus neglecting them leads to a significant power production loss. Heavily increasing the light absorption distance can therefore greatly increase the absorption of red and infrared wavelengths. This is the method in which decoupling carrier extraction and light absorption can increase the efficiency of OPVs.

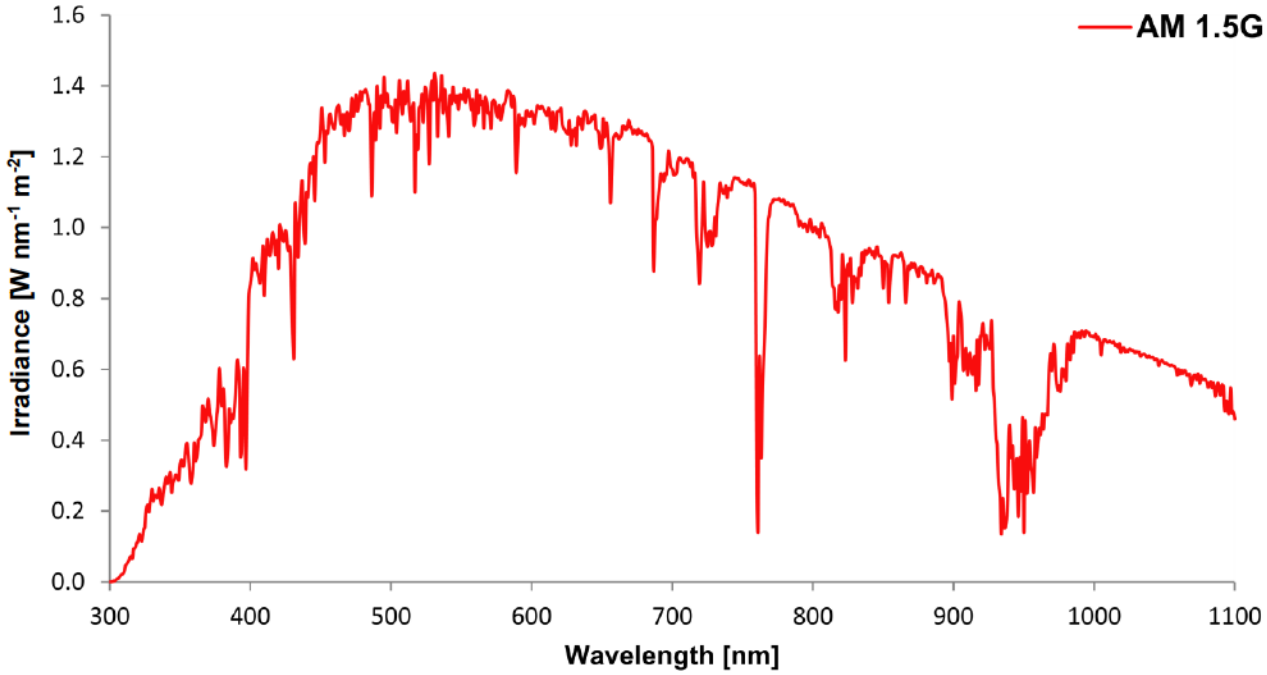


Fig 3.1 – AM 1.5 G: spectrum of solar irradiance at sea level. Data was obtained from ASTM standard G-173-03 and plotted by the author.

*The author would like to sincerely thank Mike Taschuk for his guidance and large contribution in the development of this model, such as providing starting formula and data.

To gain understanding into how much efficiency could be increased with the fabrication of vertical contacts, a mathematical model was generated to predict how the variation of carrier collection distance and absorption length will affect efficiency. The model starts with the following formula for short-circuit current density [43]:

$$J_{SC} = \int d\lambda \; q \; \varphi(\lambda)\,[1 - r(\lambda)]\left[1 - e^{-\alpha(\lambda)L}\right]\eta_{CC}\eta_{CT}(w)\eta_{ED} \qquad (3a)$$

In this formula q represents the elementary charge, $\varphi(\lambda)$ represents the spectra of the incident light in units of photons s^{-1} cm^{-2} nm^{-1}, $r(\lambda)$ represents the wavelength-dependent reflection coefficient and $\alpha(\lambda)$ represents the wavelength-dependent absorption coefficient. L is the absorption length of the light and is also the depth of the trench assuming perfect polymer filling of the trench, while w is the carrier collection distance and hence the width of the trench after contact deposition. The various efficiencies of charge extraction are represented by η, with η_{CC} representing charge capture efficiency, $\eta_{CT}(w)$ representing charge transfer efficiency, which is a function of the carrier collection distance, and η_{ED} representing the exciton dissociation efficiency. The product of all these efficiencies is the IQE of the cell, which due to $\eta_{CT}(w)$ makes the IQE a function of the carrier collection distance as well: $IQE(w)$. This allows formula 3a to be represented more easily as:

$$J_{SC} = \int d\lambda \; q \; \varphi(\lambda)\,[1 - r(\lambda)]\left[1 - e^{-\alpha(\lambda)L}\right]IQE(w) \qquad (3b)$$

To help simplify the model to aid in the solution of the integral the reflection coefficient will be assumed to be zero, due to the following reasons. First of all, $r(\lambda)$ is entirely dependent on the encapsulation layer in a completed cell. Since the prototype cells that will be tested will not have an encapsulation layer, the inclusion of the average encapsulation layer reflectivity would not make sense. Secondly the reflectivities of the encapsulation layers are nearly constant over the visible spectrum, and have a low value, normally in the 10% to 15% range [44,45]. Since this model is going to be used to obtain an order of magnitude value for the required trench dimensions, including this slight variation is not worthwhile computationally.

To solve this simplified integral $IQE(w)$, $\varphi(\lambda)$, and $\alpha(\lambda)$ must be known. The incident photon spectra is extremely well documented in the ASTM standard, as seen in figure 3.1, and

all that is required is a simple multiplication to get the spectra into the correct units for the model. The absorption coefficient will depend on the polymer system used for the cell, and needed to be obtained from literature. For the prototype cell the P3HT:PCBM polymer system was used, and the thus the absorption coefficient for that system needed to be obtained. Lee et al. [46] reports the optical density of the P3HT:PCBM system as seen in figure 3.2a). To obtain the absorption coefficient from the optical density data a formulaic relationship between the two had to be derived. The formulae for the optical density, A_λ, and the absorption coefficient can be seen below.

$$A_\lambda = \log_{10} \frac{I_0}{I(z)} \qquad (4)$$

$$I(z) = I_0 e^{-\alpha z} \qquad (5)$$

Where I_0 is the incident irradiance, $I(z)$ is the transmitted irradiance through the material thickness z. Equating the ratio of I_0 to $I(z)$ yields the relationship between optical density and absorption coefficient:

$$\alpha = \frac{\ln 10^{A_\lambda}}{z} \qquad (6)$$

Using this relationship the absorption coefficient can be calculated from the optical density data from Lee et al. [46]. The optical density data was first extracted from the plot using plot digitizing software to obtain a data point roughly every nanometer at the steep part of the curve below 400 nm, and roughly every five nanometers for the rest of the curve. Using the thickness of the film, 520 nm, it was then possible to plot $\alpha(\lambda)$, as seen in figure 3.2b). Lee reports an absorption coefficient of 10^5 at $\lambda = 510$ nm, and from the extracted data a value of 0.8 x 10^5 was obtained, showing fairly good agreement. The extracted $\alpha(\lambda)$ data was then linearly interpolated creating a value for $\alpha(\lambda)$ for every integer value of wavelength. This interpolation allowed for the numerical integration to solve for *Jsc,* as the data points for $\varphi(\lambda)$ are at the same wavelength values in the ASTM standard.

Direct values of *IQE(w)* were not able to be found in literature and hence a different approach was required compared to the direct data conversion that could be done to find $\alpha(\lambda)$. Since *IQE(w)* is not a function of wavelength, it is able to be taken out of the integral in formula

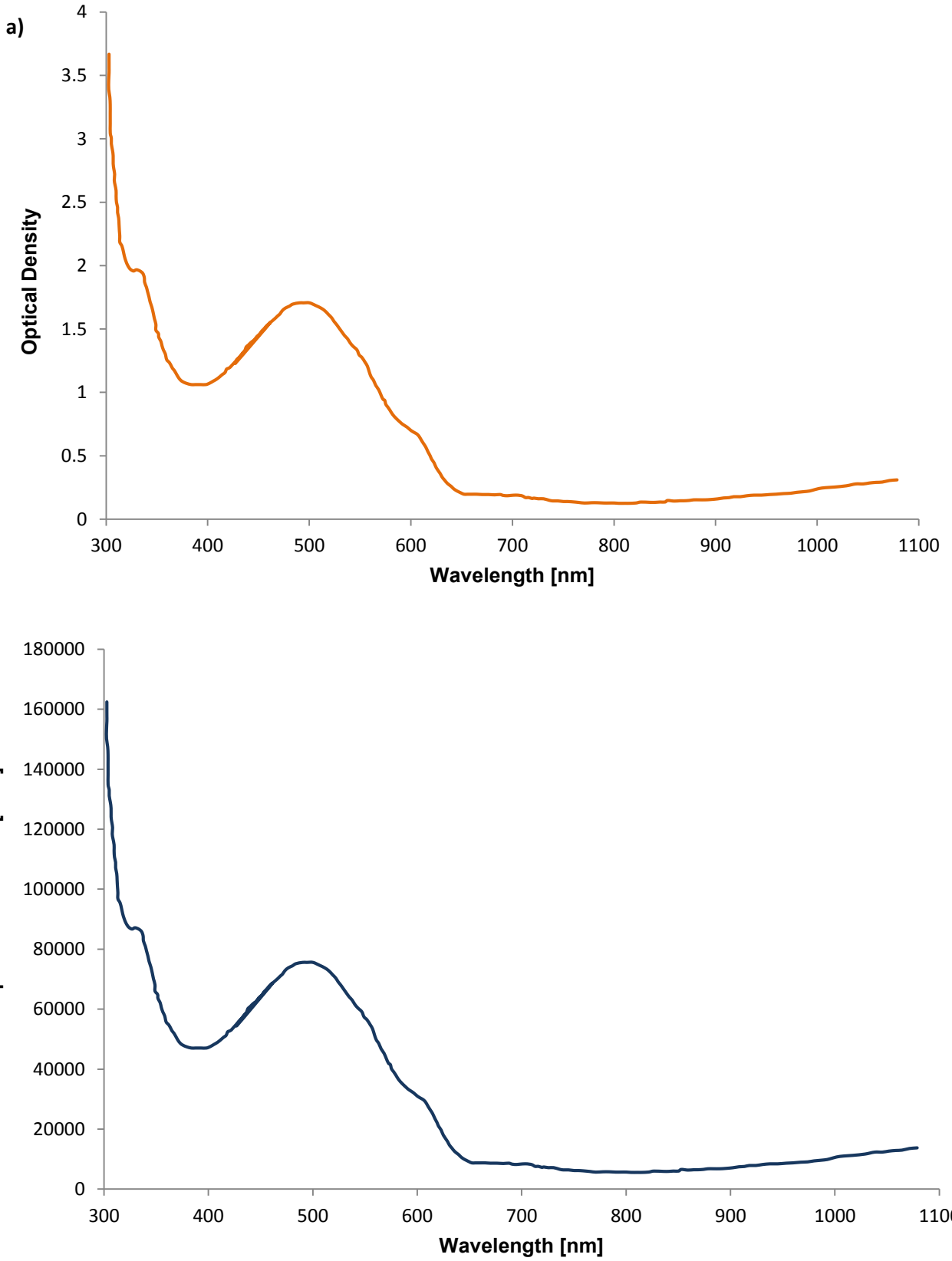


Fig 3.2 a) – Optical density data of a 520 nm P3HT:PCBM layer captured from Lee et al. [46]. **b)** Absorption coefficient of P3HT:PCBM calculated from optical density data.

(3). This fact, along with the assumption of no reflectivity, allows formula 3 to be rearranged to the following:

$$IQE(w) = \frac{J_{SC}}{\int q\varphi(\lambda)[1 - e^{-\alpha(\lambda)L}]d\lambda} \qquad (7)$$

This rearrangement allows for the possibility of generating a model for *IQE(w)* by using known values of J_{SC} and calculating the denominator integral in formula 7 from the device thickness L and the calculated values of $\alpha(\lambda)$. Calculating is possible because in a standard cell architecture seen throughout literature the charge extraction distance, t, and the light absorption thickness, L, are the same value as they are not decoupled. Values of J_{SC} and t were obtained from Dennler et al. and Lee et al.[46,47] and were used to calculate data points for a plot of IQE vs. charge extraction distance, as seen in figure 3.3, using formula 7. A linear least-squares fitting was generated to model *IQE(w)*. The fitting had a R^2 value of 0.92 showing a good agreement to the data. With this model of *IQE(w)*in hand J_{SC} could then be calculated for an arbitrary charge extraction distance and light absorption length. By using formula 1 from chapter

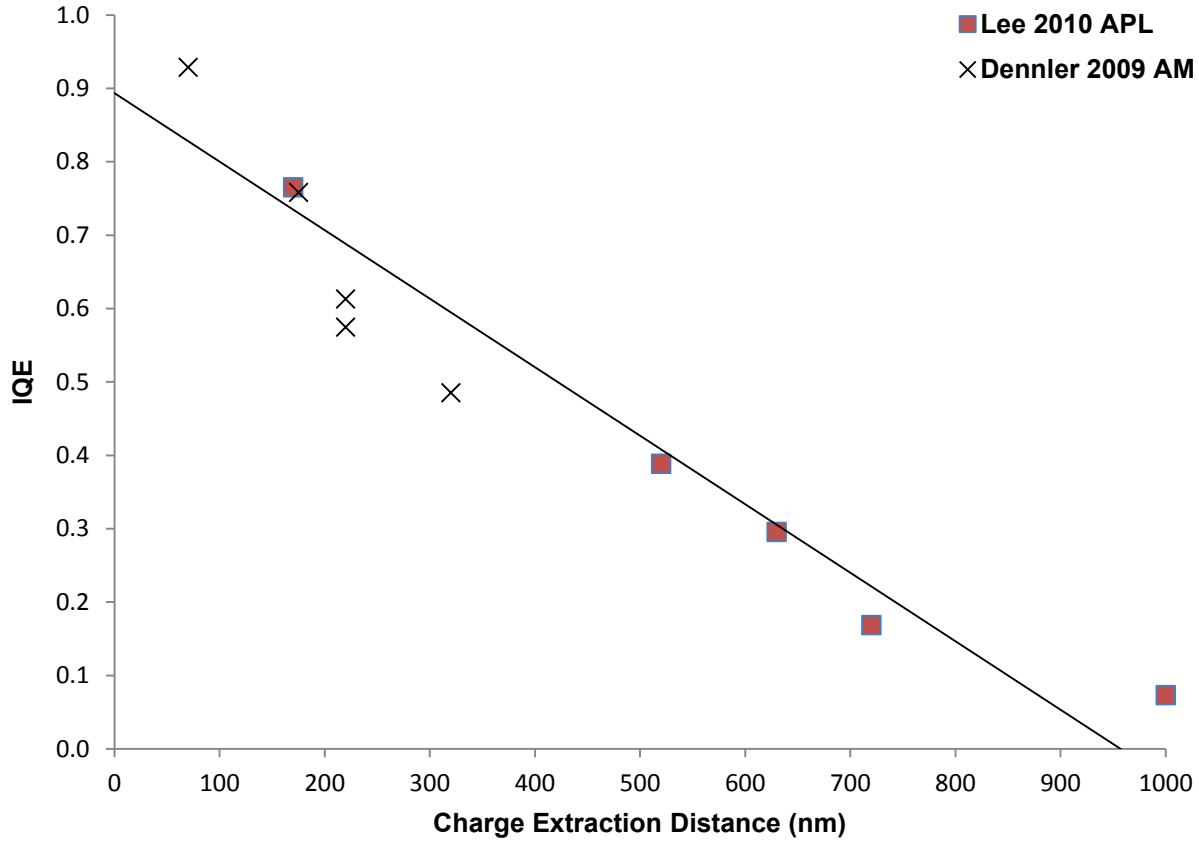


Fig 3.3 – Linear fitting of IQE vs charge extraction distance giving IQE(w). R^2= 0.92.

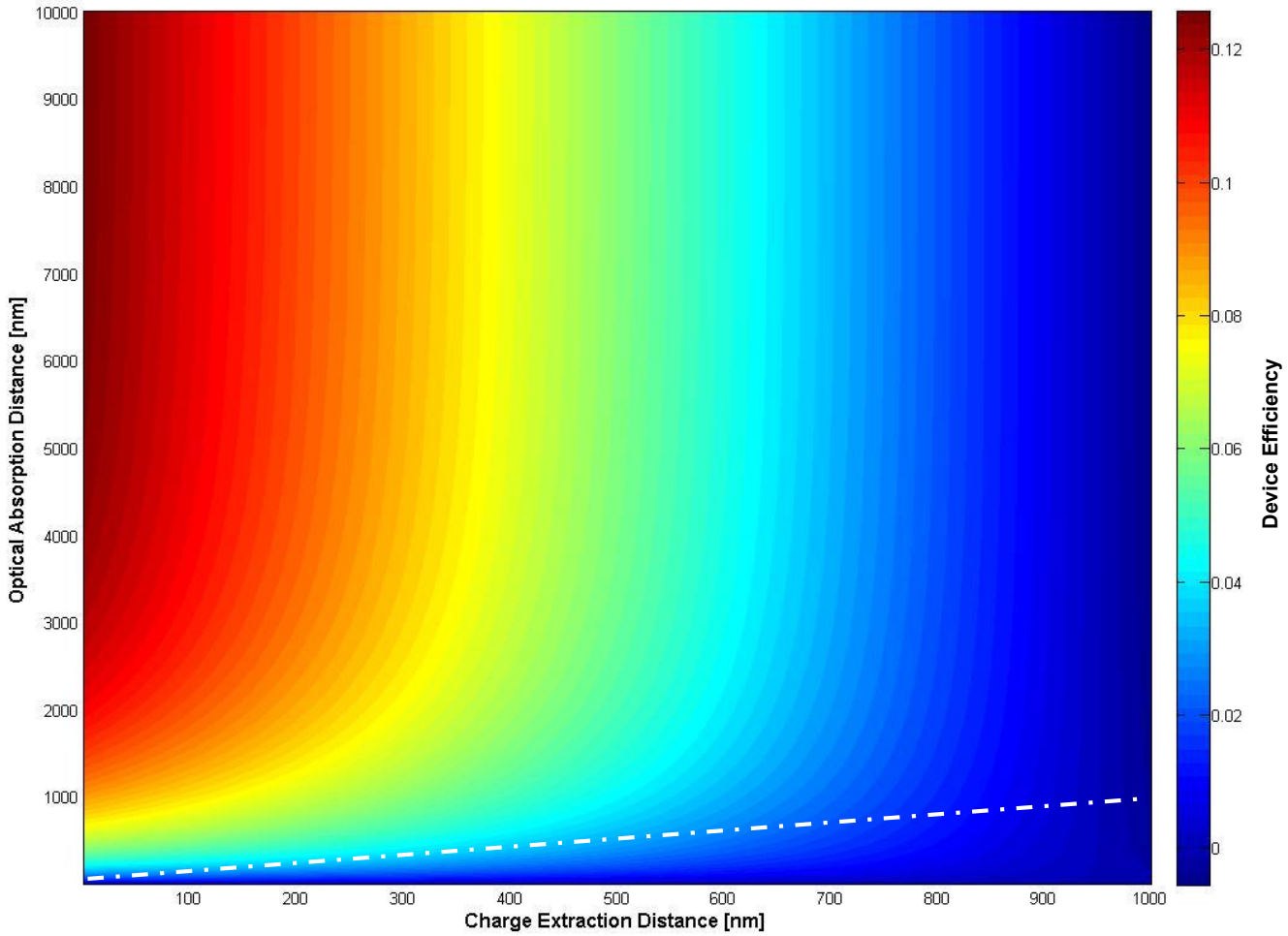


Fig 3.4 – Heat map modelling the efficiencies of devices with decoupled optical absorption length and charge extraction distance.

2, as well as assuming values for fill factor and open circuit voltage commonly obtained in literature (0.6 and 0.6 V respectively) [48], a heat map of photoconversion efficiency was obtained and can be seen in figure 3.4.

The dashed white line in figure 3.4 shows the efficiencies that standard cell architecture is constrained to, as by definition in a standard cell t is equal to L. The model shows that for a standard cell design the average maximum photoconversion efficiency capable of being generated for the P3HT:PCBM polymer system is approximately 4% with a thickness of 200-300nm, which matches extremely well with literature [47]. The reproduction of common efficiency values from literature suggest that the model can successfully estimate the gains obtainable from decoupling charge extraction distance and optical absorption length.

According to the model, extremely high efficiency gains can be made through the use of vertical contacts. By setting the charge extraction distance anywhere between 100-200 nm it can be seen that efficiencies of 10% or more can be achieved by increasing the optical absorption distance to approximately 2-3 μm. Vertical contacts in OPV devices with dimensions in that range have not been demonstrated before, to the best of this author's knowledge. Indeed, the model suggests that the pioneering devices of Niggeman et al. did not have dimensions required to properly see the effect of decoupling carrier extraction and light absorption, and likely contributed to the devices' poor efficiencies [40-41].

Structures of this size and aspect ratio can be created using common lithographical and etching techniques that are used in the microfabrication industry [49]. Given the current ability to fabricate structures of this size as well as the large potential gains in efficiency that could be achieved by creating such a device, a microfabrication process flow was developed to create a prototype device that would test the predictions of the model.

3.2 Prototype Device Fabrication and Testing Process Flow

Initially many complex large area device designs were considered to test the model, some of which can be seen in chapter 9. Under further examination, it was decided that the device should be made as simply as possible to more easily test the model. Therefore, small-area device designs that implement as many standard microfabrication processes as possible were examined for use.

Firstly, the material system used to form the structure of the device needed to be chosen. The most well understood materials system to use for microfabrication by far is single crystal silicon wafers, due to their long standing use in integrated circuits [50]. There are many industry standard processes for fabricating structures on the order of hundreds of nanometers in silicon, such as photolithography and anisotropic plasma etching [49]. Multiple photolithography steps add complexity to the fabrication and therefore increases the failure rate of devices. Therefore, it was decided that a single photolithography and plasma etching step would be used to create a single small trench in the silicon substrate. The trench sidewalls could then be used to form the vertical electrical contacts required for decoupling carrier extraction and light absorption.

Ideally, the vertical electrical contacts used in the device would be made from metals due to their high conductivity and their ability to match energy levels in the device. One issue that needed to be solved was the fact that metal electrical contacts often form Schottky diodes when in contact with silicon due to the fact that silicon is a semiconductor and not an insulator [51]. Thus the silicon needed to be oxidized after forming the trench to form a thick layer of SiO_2, a very stable insulator. Since there are no other layers that had been added, only structured silicon, a wet thermal oxidation process was decided as the ideal process to form this oxidation layer. With this protective insulating layer lining the entirety of the trench, metal layers could be deposited without worrying about conduction through the silicon wafer.

To form the device, metal layers have to be deposited on the sidewalls of the trenches without overlapping on the bottom of the trench. To do this, the metals must therefore be deposited at an angle, with a collimated deposition source. This requirement lends itself directly to glancing angle deposition (GLAD), where the substrate can be angled arbitrarily with respect to the deposition source and deposition occurs through evaporation, which provides a very collimated deposition plume [52]. By tilting the structured substrate, a metal deposition can be performed that only covers one sidewall of the trench, which allows for two different metal layers to be used as the contacts to the cell. This is ideal for OPVs as the two metals can be chosen so that their work functions allow preferentially for holes or electrons to be swept out of the cell, which increases efficiency. The angled deposition also forms metal layers on the top of the substrate, creating large electrical contact pad for easy connection to testing equipment.

Once the metal contacts have been deposited the polymer system needs to be introduced into the trench. Spin coating is an ideal method for this as it allows for the coverage of highly structured substrates in a uniform fashion [53]. The polymer mixture can be solvated using appropriate organic solvents and then spun onto the substrate, naturally forming a solid bulk heterojunction layer once the solvent evaporates. The spin speed can be optimized to easily provide proper filling of the trench, to form the cell. Excess polymer can then be wiped off the contact pads to allow for clip connection to I-V testing equipment.

I-V testing is done under illumination of a solar simulator to characterize the cell. The applied voltage is swept across a range and the current is measured to obtain the I-V curve of the cell, allowing for the efficiency of the cell to be determined. Once this is complete the device can

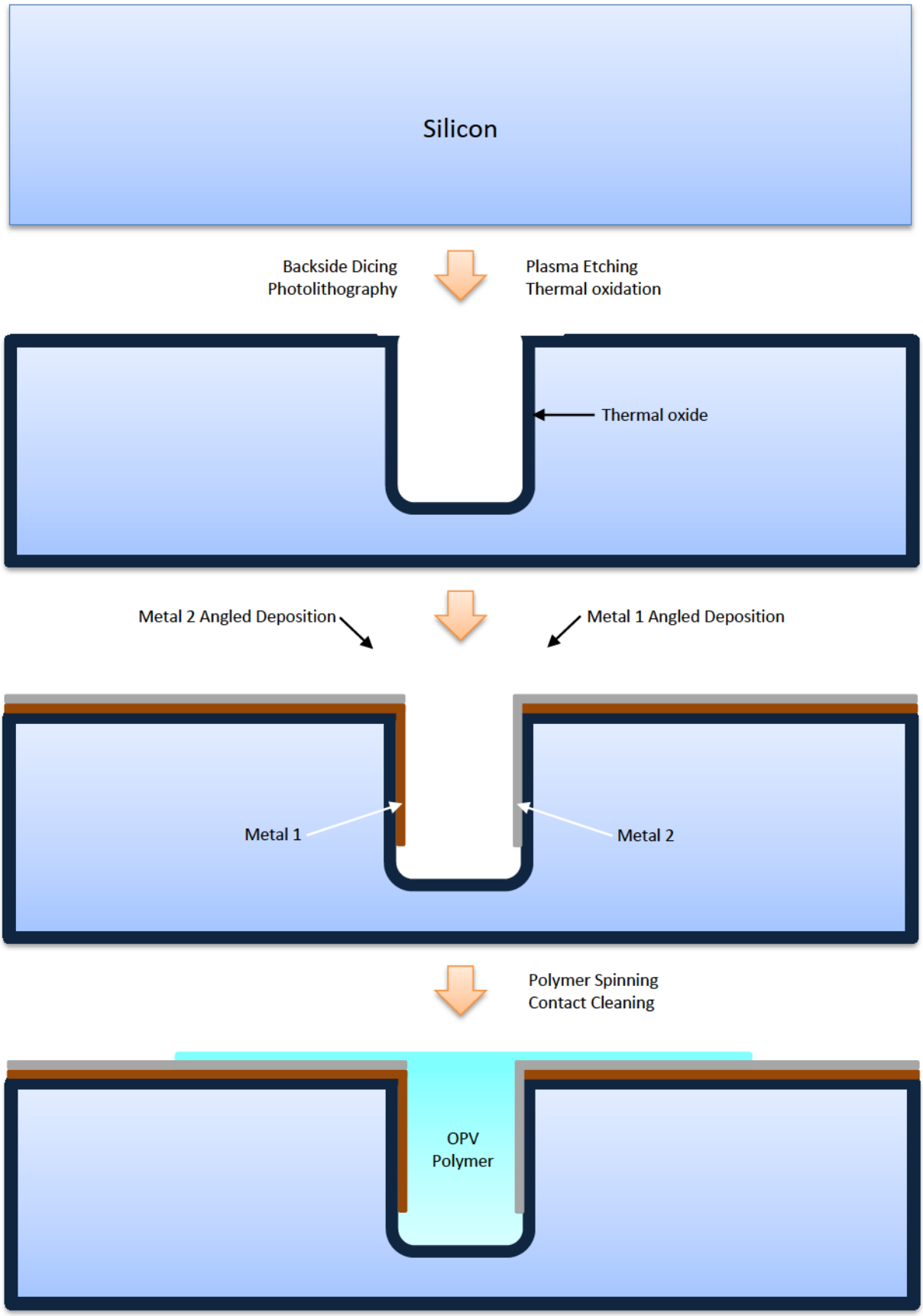


Fig 3.5 – Process flow to create prototype single trench OPV device

be imaged with SEM to determine the trench dimensions, thus allowing the device to be compared with the model. The entirety of this process flow is shown in figure 3.5 on the page above.

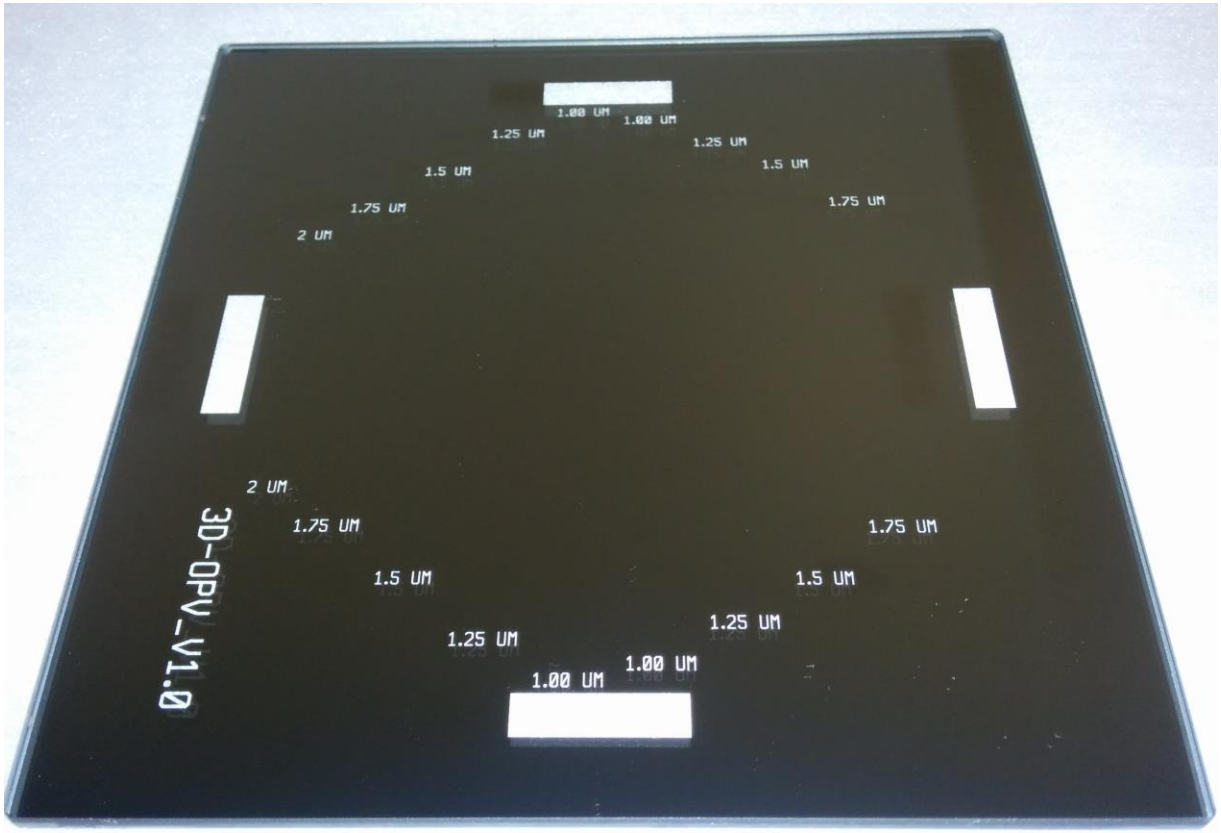
Chapter 4: Mask Design and Backside Dicing Optimization

4.1 Photolithography Mask Design

Before any device fabrication could be done, the shadow mask for the photolithography process step needed to be designed. To fully test the model, a wide variety of trench depths and widths needed to be fabricated to compare to different parts of the model's heatmap. It was therefore ideal for the mask to generate trenches of different widths in one exposure to reduce processing time and effort. The photolithography equipment used for fabricating the devices were contact lithography mask aligners, which have a one micron size limit on the patterns they can successfully generate. This is just on the edge of testing the model, but a processing method described in chapter 6 allows the reduction of the trench size after it has been etched. It was therefore decided to design the mask to have etched trenches ranging from 1-2 micrometres wide, separated by 250 nm increments, yielding five different trench sizes.

To successfully separate the trenches by cleaving the wafer, as well as provide reasonably sized electrical contact pads for I-V testing, it was decided that the trenches would be separated by one centimeter. Using this spacing, the 100 mm diameter silicon wafers that were used for processing allow for nine trenches. Trenches patterned closer to the middle of the wafer could be much longer than to those more offset from the wafer center. The device yield for lithographical processes is often highest in the center of the wafer, with yield decreasing closer to the edge. In light of these facts the choice for where to place the different size trenches on the wafer, and thus the mask, can be made. Smaller lithographical features have a higher defect density and thus lower yield. Therefore, the pattern for the smallest trenches, one micron in width, were placed in the center of the mask to help increase their yield. The pattern for the next smallest trench, one and a quarter micron in width, was placed on either side the one micron trench pattern. This trend was continued until the patterns for all the different sizes trenches were placed onto the mask, with the two micron trench being the only one that does not repeat. Following these rules led to the mask design seen below in figure 4.1 and figure 4.2.

a)



b)

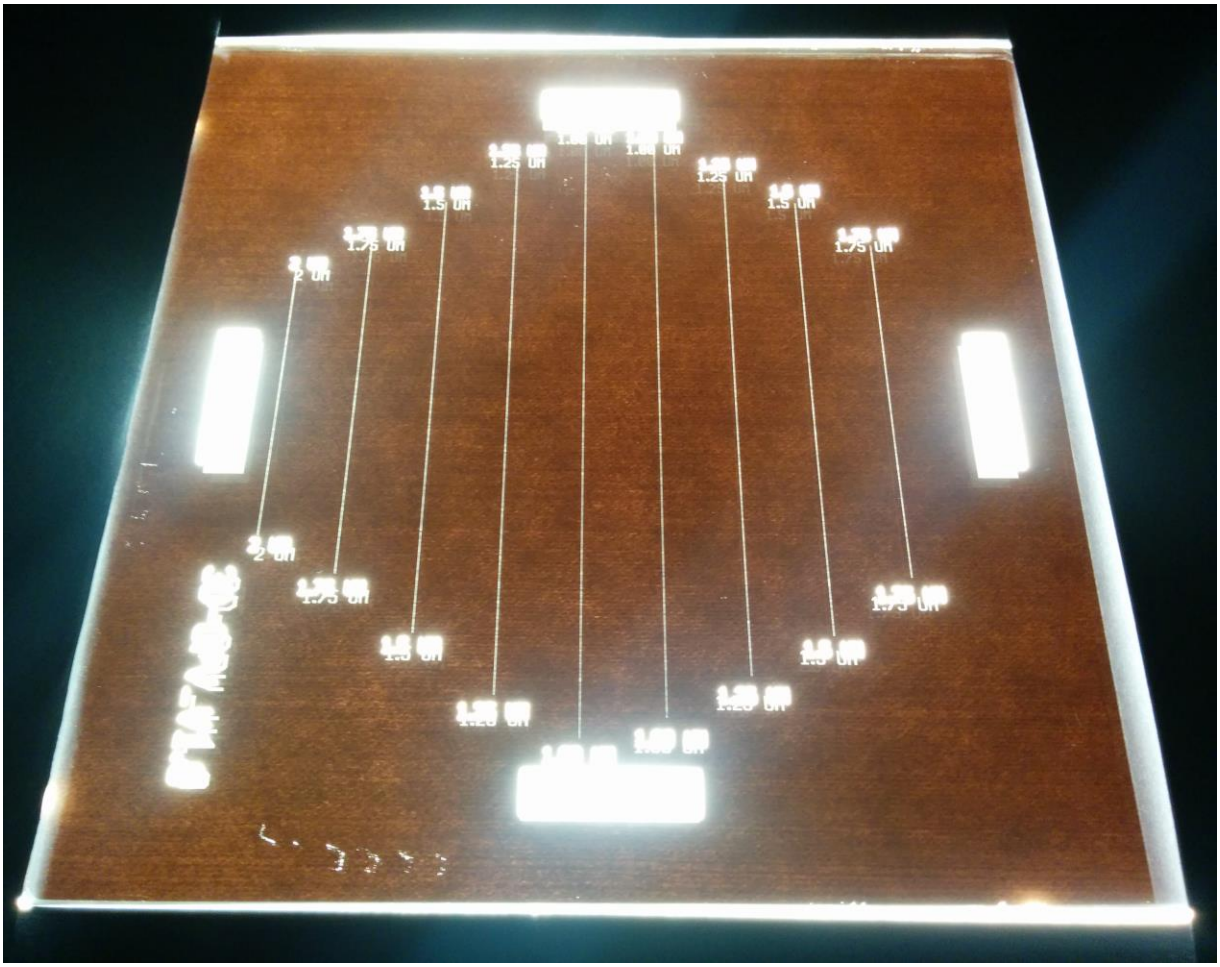


Fig 4.1 a) Photo of mask without backlighting showing the pattern labeling and alignment windows **b)** Photo of mask with backlighting showing the placement of the trenches on the mask

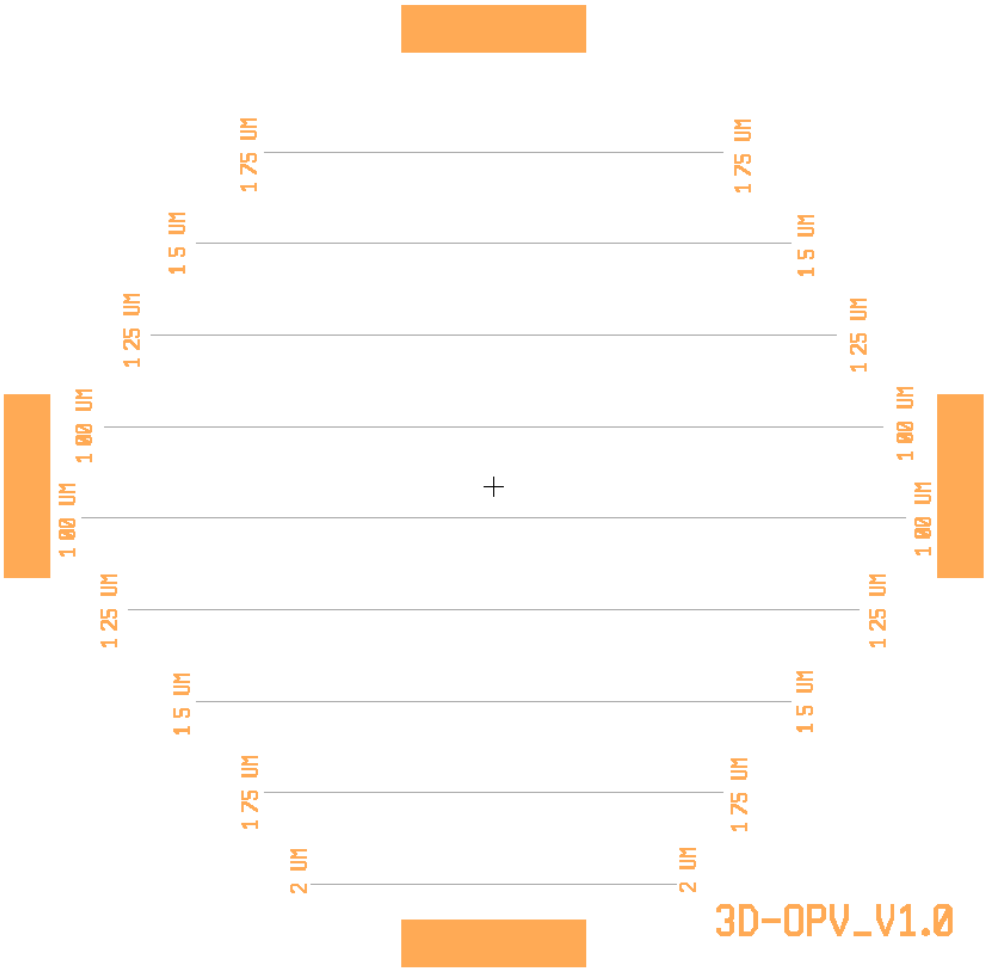


Fig 4.2 – Mask profile in mask designing software L-edit

4.2 Backside Dicing Optimization

As seen in figure 4.1 the trenches end up nearly crossing the entirety of the wafer, parallel with the wafer flat. If each full length trench was made into a single device, one killer defect anywhere on the trench would yield a defective device. Thus it makes the most sense to split the trenches up into as small as physically manageable pieces to minimize the effect of killer defects. By patterning a silicon wafer and manually cleaving up the wafer, it was determined that a 3 mm device length was the best balance of small trench length and ease of physical handling. This trench length conveniently was the minimum size required for polymer spinning. Since the trenches are patterned one centimeter apart on the wafer this yields a die size of three millimeters by ten millimeters for the devices.

To manually cleave up the whole wafer into such die sizes would be extremely time consuming as well as lead to a large variance in sizes between the different devices, making

direct comparison between devices difficult. The normal solution to such a problem is to use a dicing saw to reliably separate the dies from each other after all the processing is finished. This works because most devices are designed to be fully contained within the die so the dicing saw does not cut through any working portion of the device. In these device however, the trench spans the length of the device and therefore the dicing saw would need to cut through the trench itself. This would likely lead to much lower yield as the rough cut of the dicing saw could easily cause short circuits by connecting either side of the trench by a particle simply bridging the gap. Cleaving leads to a much smoother divide on the micro and nanometer scale that would likely cause lower defect rates.

A possible solution to this issue was to dice partially through the unpolished side of the wafer, henceforth referred to as the backside, before any other processing was done. After backside dicing, the wafer would be taken through the full fabrication processes before polymer spinning and would ideally be easily cleavable along the preset lines defined by the backside dicing. This method could then increase the speed and accuracy of the cleaving, quickly yielding devices of comparable size and shape, ideal for both OPV polymer spinning consistency and for device to device comparison. This backside dicing method needed to be tested and optimized to determine if it was possible to backside dice the wafer with shallow enough cuts that it would fully survive the rest of the fabrication processing, but be deep enough to provide cleaving without the need for a diamond scribe to start every cleave.

Normally when dicing a wafer, flexible blue microfabrication tape is adhered to the unpolished backside of the wafer by using a heated raising table. Once the raising table presses the wafer up into the blue tape a hand held roller is used to remove any bubbles present to ensure a the wafer lies flat on the chuck for the wafer dicer. The wafer is then diced with the polished device side facing up. In the backside dicing process, the polished device side needed to be adhered with blue tape. The polished side was much more likely to trap air bubbles and the bubbles were nearly impossible to remove once the wafer was fully adhered to the blue tape for two reasons. Firstly, the blue tape adhered much more strongly to polished side of the wafer due to the extremely flat surface it had. Secondly there is essentially no roughness on the polished side which constricts the movement of the bubbles when pressed with the roller. The roughness of the unpolished backside helps the bubbles to move as the air can more easily transfer through

the micro-valleys where the tape has not fully adhered. Thus when the roller was pressed down after the tape adhered all it served to do was to compress the air in the bubbles, making the bubbles smaller but much less compressible. These bubbles would cause the wafer to not sit level enough in the chuck of the dicing machine, leading to irregularities in the dicing depth, a critically important factor when not trying to dice all the way through the wafer as in the case with the backside dicing process.

Initially, an ad hoc solution was found by poking a small hole in each bubble with a pin or exacto-knife before rolling to allow the air to escape when pressure was applied. The hole had to be placed such that it was farthest away from the rolling direction to fully allow the air to escape. As there were normally hundreds of small bubbles when adhering to the polished side and due to the fact that each bubble had to be popped by hand, this was a very time consuming process. A better method for reducing the amount of bubbles when adhering to the device side of the wafer was discovered by accident due to user impatience. Since popping the bubbles took an inordinate amount of time and because many wafers had to be tested for the backside dicing depth optimization the rest of the process was implemented as fast as possible by the user. This resulted into trying to use the roller as soon as the table had finished raising the wafer. In one of these bouts of haste, the roller was used as the table was being raised. The roller bent the flexible blue tape enough so as the wafer was coming upwards the tape would only adhere to where roller was applying pressure. If timed correctly the entirety of the wafer could be adhered before the table had fully raised. This method naturally presses the air to where the tape had not yet adhered and thus drastically cut down on bubbles. The number of bubbles created dropped from the order of hundreds to roughly ten, which could be removed quickly with a pin and another application of the roller. Once practiced, this method of blue tape adhering became a standard part of the backside dicing process.

With this problem removed, a variety of depths could then be tested to discover if the backside dicing method could be used in the process flow. The wafers used for the project were approximately 500 μm thick, which the dicing saw was designed to cleanly cut through, yet not cut the blue tape. The blade could be offset by different amounts to allow for wafers with a variety of thicknesses to be used. Defining zero offset to be the depth normally used to cut through the whole 500 μm thick wafer, blade offsets of 100 μm, 150 μm, 200 μm, 300 μm, and

400 μm were tested, with four wafers of each offset being diced and used for testing. These wafers where then placed through the steps in the fabrication process that would be the most physically demanding to determine if they would break. Once this was done the wafers were then tested to see how easily they cleaved without using a diamond scribe.

The 100 μm offset diced wafers were extremely fragile. Two of the four wafers fractured by simply removing the wafers from the chuck of the dicing machine, while the other two fractured when removing the blue tape. The 150 μm offset devices were more robust but not by a great deal. All four wafers survived the removal from the chuck, but two of the wafers fractured with the removal of the blue tape. The other two wafers fractured and explosively broke apart during the 4000 rpm spin speed test, the speed used to apply the photoresist for the photolithography process. The 200 μm offset again followed the trend of being more physically robust, as was expected. Removal from the chuck and removal of the blue tape was successful for all four wafers. During the spin speed testing only one of the four wafers broke apart, which was considered an acceptable amount of yield if the 200 μm offset wafers cleaved well and none of the higher offset wafers did. The 200 μm offset also stood up fairly well to piranha cleaning with only one slightly fracturing in the hot solution, which was again considered an acceptable amount of yield if necessary. One of the 200 μm wafers was put into the spin rinse dryer after piranha cleaning and explosively fractured within a handful of seconds, while the other was dried using a nitrogen gun and remained intact. It was therefore determined that if this was the only offset that was cleavable without a diamond scribe that the wafers would be dried by hand using the nitrogen gun. The 300 μm offset wafers held up very well for the most part. They fully survived removal from the chuck, blue tape removal, 4000 rpm spin speed testing, and piranha cleaning. One of the wafers did end up fracturing in the spin rinse drying after piranha cleaning, so again it was determined that hand drying with the nitrogen gun would be the method of drying if this blade offset was the scribelessly cleavable. The 400 μm offset wafers were extremely robust, holding up to all physical processes mentioned above.

Since it was only the 200 μm, 300 μm, and 400 μm offset wafers that survived the entirety of tested physical processes it was only these wafers that were tested for ease of cleavability. The 200 μm offset wafers were extremely easy to cleave into large sections without a diamond scribe, allowing each trench size to be cleaved out of the wafer without much effort.

This was ideal for the metal deposition step as each trench size had to be deposited on its own due to differences in geometry, as is further discussed in chapter 7. When cleaving the individual device sized pieces the 200 μm offset was often slightly too fragile. Trying to break off one individual device-sized piece from the larger chunk, as would be done after metal deposition, would often result into three or more pieces breaking off which would fly off in random directions. It was found that if the large piece was held very close to the table that the small pieces that would break off would land right side up the majority of the time, however this was not an ideal solution. The 300 μm offset wafers had the opposite problem of the 200 μm offset diced wafers. Large pieces could not be reliably cleaved without the use of a diamond scribe as the wafer would fracture in odd rectangular patterns when attempting to break apart without scribing, forming jagged lined pieces. Once cleaved into pieces that only would contain a single trench however, the device sized pieces would easily cleave off one at a time without the need for a diamond scribe, the ideal scenario for after the metal deposition step. The 400 μm offset diced wafers would not cleave at all without diamond scribing, showing that this offset depth was not effective as a backside dicing depth. A visual summary of the cleaving test can be seen in figure 4.3 on the next page. Comparing the 200 μm and 300 μm offset diced wafer results it was determined that the 300 μm offset depth was ideal due to its physical robustness during the processing steps, only fracturing during the optional spin rinse drying step, and also the ease at which single device sized pieces could be reliably cleaved. Having to use a diamond scribe to break up the wafer into the pieces containing a single sized trench was very manageable as this would only result in nine to ten cleaves per wafer.

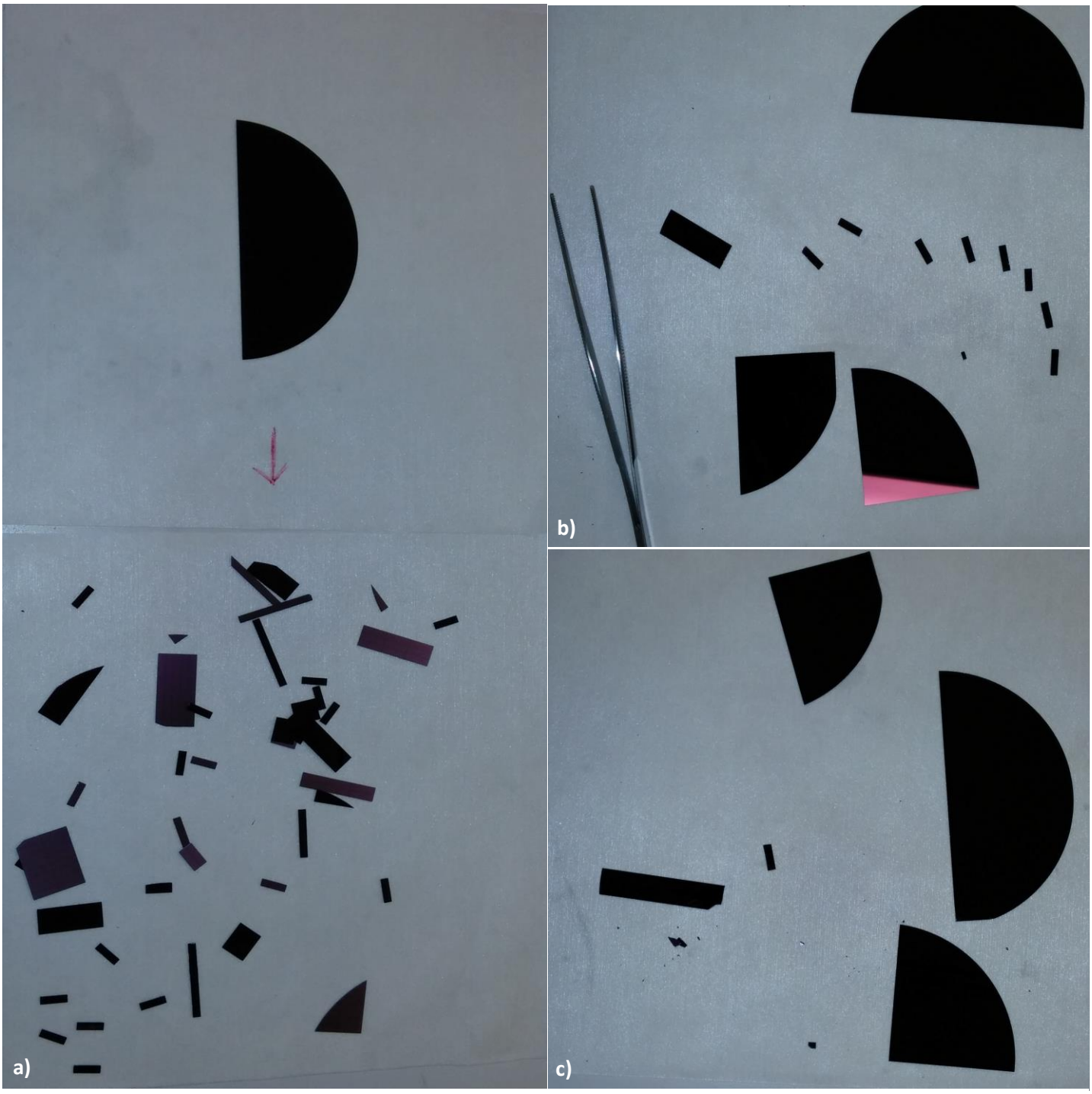


Fig 4.3 a) Result of 200 µm offset diced wafer cleaving test: cleaving could not be reliably controlled **b)** Result of 300 µm offset diced wafer cleaving test: cleaving reliably controllable **c)** Result of 400 µm offset diced wafer cleaving: pieces not cleavable without diamond scribe

Chapter 5: Photolithography Optimization

5.1 Initial Photolithography Experimental Procedure

The starting point for the optimization of the lithographic process used to define the trenches followed the standard procedure for basic lithographic processes at the University of Alberta nanoFAB. The backside diced wafers are first cleaned of organic and metallic contaminants using a piranha clean. The piranha cleaning solution is first made by mixing 96% sulfuric acid and 30% hydrogen peroxide in a ratio of 3 parts sulfuric acid to one part hydrogen peroxide. The mixture of these two chemical causes an exothermic reaction which heats the solution to near-boiling temperatures. The backside diced wafers are then placed into the hot piranha for 15 minutes using a Teflon wafer boat. Once the time expires, the wafers are taken out of the piranha and rinsed five times with de-ionized water in a dump rinser. The wafers are then dried by hand using a clean dry nitrogen air gun to remove the excess water.

The piranha-cleaned wafers are then coated in hexamethyldisilizane (HMDS), using a Yield Engineering Systems (YES) HMDS oven. HMDS is used to promote strong adhesion between a bare silicon surface and photoresists by the formation of a hydrophobic organic layer on the silicon surface. Ammonia is produced during the process and thus the coating must take place in a sealed vacuum oven, such as the YES HMDS oven. The oven reduces the pressure over the wafers and applies heat in a proprietary process to remove water from the wafer, which would interfere with the HMDS application. HMDS is then introduced into the vacuum oven in vapour form at 150 °C to coat the wafers. The total cycle of water removal and HMDS coating takes roughly 17 minutes. Once the application of HMDS is complete, the wafers are ready to be coated in photoresist.

The photoresist used for the process is HPR 504, a very well characterized positive photoresist used a great deal by the University of Alberta nanoFAB. The wafers were placed on a Solitec spinner and 5-10 mL of HPR 504 resist was poured over the center of the wafer. The wafer was then spun at 500 RPM for 10 s to evenly coat the wafer with the resist and then spun

at 4000 rpm for 40 s to thin the resist layer down to approximately 1.25 μm. The wafer is then placed onto a hot plate at 115 °C for 90 s to perform what is referred to as a soft bake of the resist. The soft bake reduces the solvent content of the resist, which promotes increased resist adhesion, bubbling of N_2 during exposure and etching, as well as reducing mask adhesion [54]. After soft baking, the wafers were rested for 15 min to re-hydrate the resist, which is critically important for consistent results when exposing and developing the resist.

Once re-hydration is complete, the wafers were exposed using an ABM mask aligner. The wafers were put into hard vacuum contact with the mask after being aligned. They were then exposed for 3 s using 405 and 365 nm light. Once exposure was complete, the wafers were removed from the mask aligner and developed using 354 Developer. The wafers were developed for approximately 20 s by immersing the wafer in the developer and agitating the fluid by hand. After rinsing the developer off with de-ionized water and drying off with clean dry nitrogen, the wafer was ready for etching to fabricate the trenches. The initial exposure and development time were chosen to keep the trench dimensions as accurate as possible to the mask.

5.2 Patterned Wafer and Mask Analysis

One of the easiest ways of characterizing a lithographical process is to look at the substrate after etching. Initial analysis of the etched trenches fabricated using the standard procedure mentioned above seemed very promising. As seen in figure 5.1, the etched trenches had the required shape for the OPV device and a quick scan top down showed trenches that were straight and had little deviation over 100 μm distances. The devices created from these trenches led to extremely low

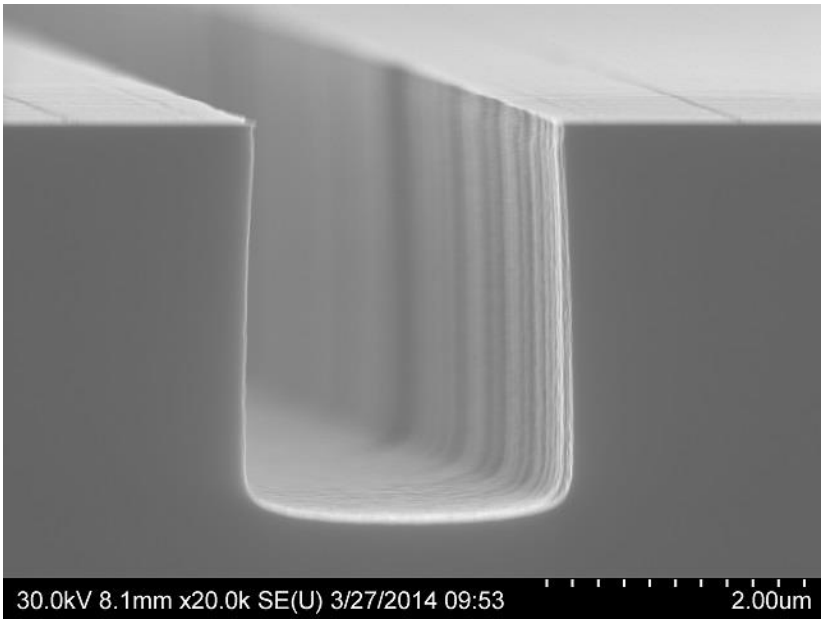


Fig 5.1 – Etched silicon trench

resistance short circuits however, on the order of a few ohms. Even after solving a metal deposition issue that will be discussed in chapter 7, the devices made from these trenches still showed this low-resistance short-circuit behavior. Seeking the cause of these shorts much larger top-down SEM scans were taken of the trenches after metal deposition, which is explained more in detail in chapter 7. High-resolution images could much more easily be obtained due to the conducting nature of the metallic films. During these scans a large amount of errors were found along the trenches that could be the cause of the shorts as can be seen in figure 5.2.

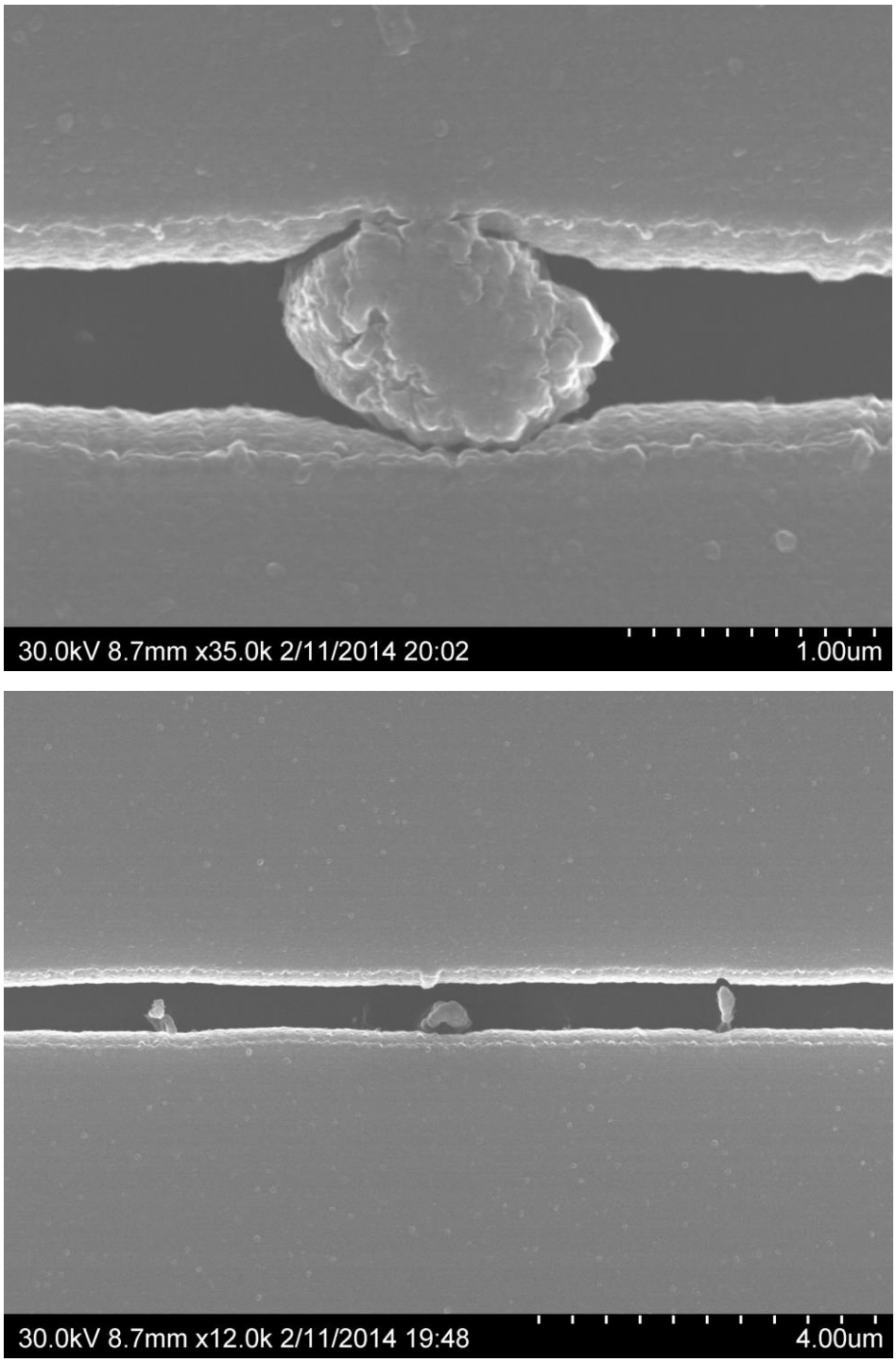


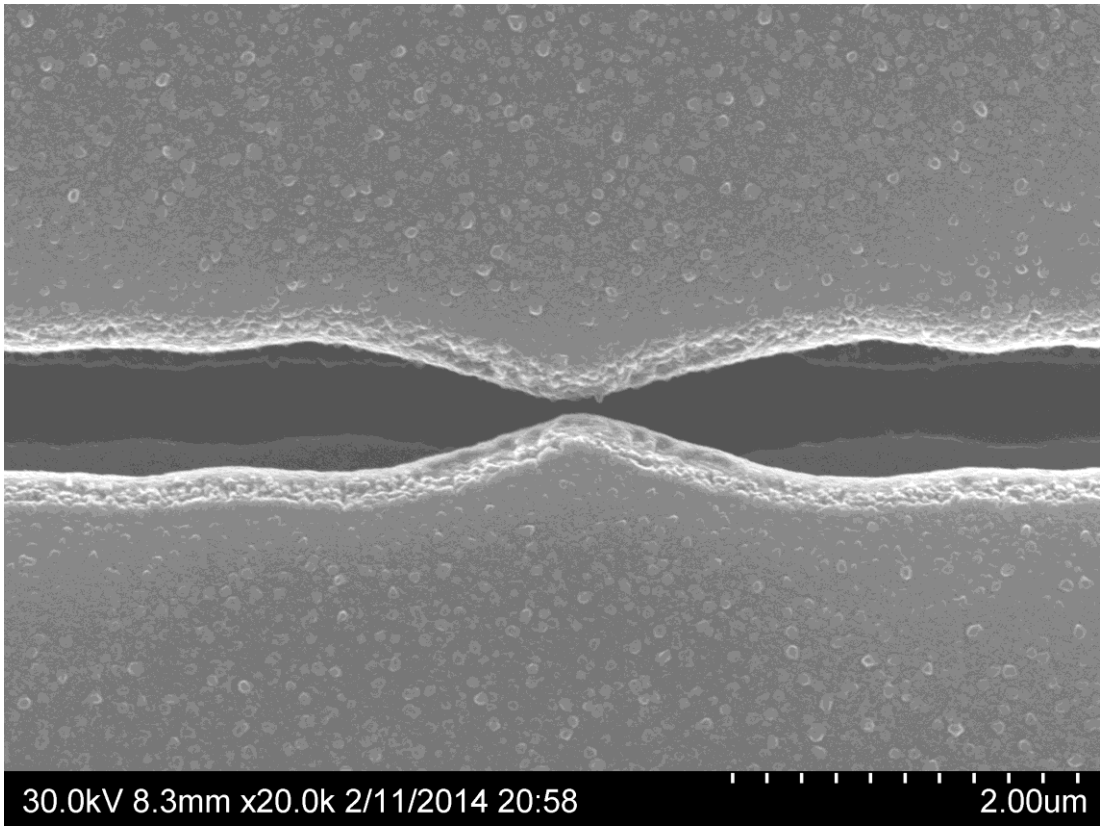
Fig 5.2 – Occlusion errors in trenches with particles (above) and pillars (below)

There were two main types of errors spotted in this scan. The first type looked to consist of a particle that seemed to have crossed the trench before the metal deposition, bridging the two sides of the metal contact causing the short. An example of this error can be seen in figure 5.2a. The other type of error found were column like structures that protruded out from the trench. These errors were likely caused by a small particle inside the trench itself. The metal deposition could build up to form a column as metal was being deposited on either side of the trench walls. These errors can be seen in figure 5.2b, and are less likely to cause a short but are still a large concern.

Since both these errors were likely caused by particles being deposited onto the wafers during processing, it was decided that photolithography and etching would be performed at night when there were far fewer users, and the particle count in the clean room would be far lower. To help further reduce the particle count the mask was cleaned before every exposure as well. The trenches made from this lithography test were checked for shorts after the metal deposition step and it was found that the number of extremely low-resistance shorts (those on the order of ohms) had been reduced from roughly 90% of potential devices to roughly 40% of potential devices. The other devices had shorts on the order of tens to hundreds of kilohms. This suggested that performing lithography in the evenings did reduce the number of errors due to particles, but did not fully reduce it, or might not be the only issue to cause the low-resistance shorts. These lower error rate trenches were then scanned with the SEM to determine the errors that were causing shorts. Errors like those found in figure 5.2 were found, but at a far reduced rate, particularly the particle bridging errors seen in figure 5.2a.

During these scans, the whole device length of 3 mm was scanned for multiple trenches, an extremely time consuming process, which led to the discovery of two other kinds of errors: trench pinching and trench breaking. These errors can be seen in figure 5.3 on the next page. In the pinch error the sides of the trench pinch in towards each other but are not quite touching. These errors would not lead to a short under the low voltage used for the resistance measurement, but could pose a significant issue in the actual device itself due to higher operating voltages as well as direct conduction through the organic polymer over such a small distance. The limit of the pinch error results in the break error, in which the etch failed entirely at one part of the trench. This error results in the two metal layers overlapping and thus creating a very low

resistance short. As seen in figure 5.3 the metal film does not bulge up or down in these errors, suggesting that a particle was not to blame for these and that the photolithography pattern itself



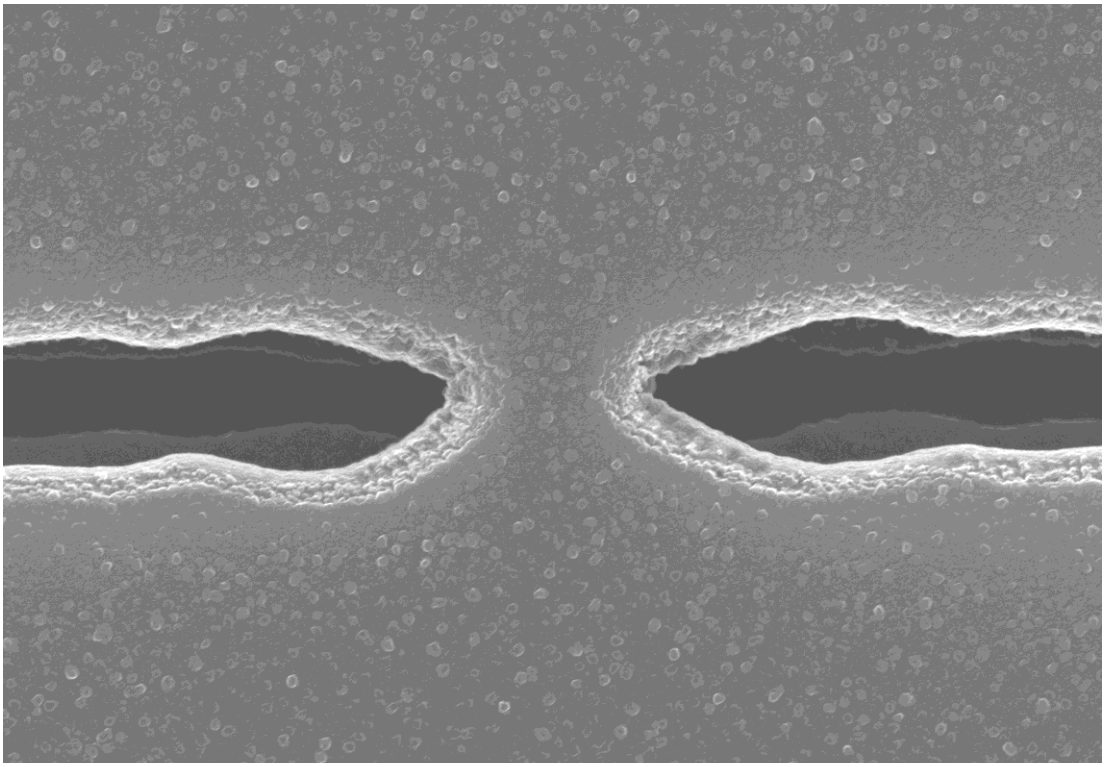
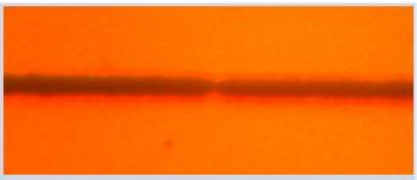
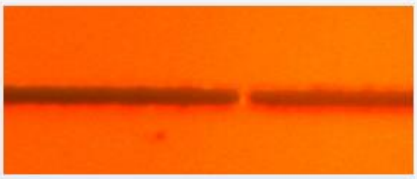
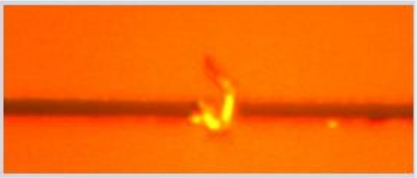
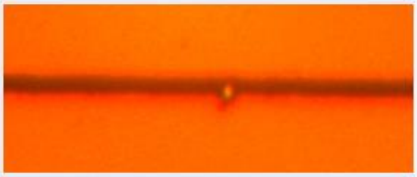


Fig 5.3 – Pinch error (above) and break error (below) occurring in metal deposited over the trench

was to blame. The discovery of these errors sparked an investigation of the mask itself to determine its accuracy.

The mask was put under a Leica INM-100 Optical Microscope equipped with a digital SLR camera attachment after being cleaned twice using a specialized mask cleaning solution proprietary to the nanoFAB. The lines with the highest error rates were likely to be the narrowest ones, so the one micron and one and a quarter micron lines were investigated for errors along their whole length. These mask lines showed nearly the exact same kind of errors seen in the trenches themselves, also with very high error rates for the pinch and break errors as seen in Table 1. Another type of error which consisted of a piece of debris or an occlusion within the line itself was also discovered and could be a likely cause of the errors seen in figure 5.2. This error type, called debris type II, also had a significant error rate that could a short in a sizable percentage of devices. Since the devices themselves were cleaved to be three millimeters wide

Table 1

Error Type	Image of Error	Rate
Pinch		• 1 µm line: ~2.9 errors/mm (258 times on longest 1 µm line) • 1.25 µm line: ~1.4 errors/mm (104 times on 1.25 µm line)
Break		• 1 µm: ~0.16 errors/mm (14 times on shortest 1 µm line) • Only once on 1.25 µm line
Debris Type I (debris over line)		• Rare, only three instances observed
Debris Type II (debris in line)		• 1 µm line: ~0.25 errors/mm (22 times on longest 1 µm line) • 1.25 µm line: ~0.13 errors/mm (10 times on 1.25 µm line)

the likelihood of obtaining a device that was not affected by the break errors or the debris type II errors was quite low, and it would be nearly impossible to obtain a device that was not affected with the pinch errors.

To reduce the effect of these errors, it was therefore required to overdevelop and overexpose the photoresist during fabrication. Overexposing the resist would help expose the resist that is shadowed by the errors to the point were enough diffracted light would cause the resist to react to the developer. The overdeveloping would further reduce the effect of the errors as areas of unexposed resist with high surface area are affected by the developer more strongly than smaller surface area features. It was found that increasing the exposure time to the UV light to four seconds and increasing the development time to 30 s nearly eliminated the effect of the mask errors on the lines formed in the resist. Having to overexpose and overdevelop to correct for the mask errors did result in wider trenches, with the smallest obtainable resist trench width being roughly 1.75 μm. This width is of course not ideal for testing the model. A feature of oxidation discussed in the next chapter allowed the device trench width to be made much smaller, bringing the devices to the edge of testability within the model.

Chapter 6: Trench Etching and Oxidation

6.1 Reactive Ion Etching

There is a plethora of ways to etch silicon [55], and the best method available had to be chosen to create the ideal rectangular cross section for the design. Since the cross section ideally would be as close to rectangular as possible, the etching method used would need to be an anisotropic one. Also, to fully test the model, the rectangular trenches needed to have fairly high aspect ratios, possibly as high as 10:1. To meet these needs, it was decided that a form of reactive ion etching (RIE), a highly anisotropic method of plasma etching, would be used. There were three suitable reactive ion etches available at the University of Alberta nanoFAB at the time of fabrication: a Bosch process etching method, an unswitched precision etching method, and a cryo etching method.

Each of these etching methods have various strengths and weaknesses. The cryo etching method cools the wafer, usually below -100 °C [56], to inhibit the chemical reactions that occur to create isotropic etching. The ion bombardment from the plasma then etches very anisitropically, creating a smooth-walled etch. Cryo etching can often result in resist cracking due to the thermal expansion mismatch, as well as redeposition of etched materials onto the cold substrate [56], creating possible issues with using the technique.

The Bosch process involves quickly switching back and forth between an isotropic etching step and wall passivation step [57]. The ion bombardment during the isotropic etch step preferentially removes the passivation layer from the bottom of the trench to allow a small etch to occur there, without affecting the side walls, while the next passivation step convers the newly formed sidewalls with a passivation layer, preventing them from being etched during the following etch step. The successive isotropic etches produce scalloped sidewalls, which may not be ideal for deposition of the metal contact layers. Both the Bosch process, and cryo etching method can etch very deeply, on the order of hundreds of microns, to produce very high aspect ratio structures, and are thus known as deep reactive ion etching (DRIE) methods.

The unswitched precision etching method uses the same passivating and etching gasses as the Bosch process, but instead of switching back and forth between the passivating gas and etching gas, it creates a plasma with both gases. This etch produces a smooth walled anisotropic etch at standard etch temperatures, a key advantage of the method. The main downside to this method is that it can only create anisotropic etch profiles on the order of ten microns. Since the etch depth required for the devices to explore the model is approximately five microns or less it was decided that the unswitched precision etching method would be used for etching the trenches.

Similar to the methodology used for the photolithography process development, the etching processing step was based upon the standard unswitched precision etching process of the University of Alberta nanoFAB. The equipment used for etching the wafers was a Surface Technology Systems (STS) inductively coupled plasma (ICP) RIE system. The STS ICP RIE was first conditioned before etching by performing 25 cycles of the nanoFAB's standard Bosch process etching on a bare silicon wafer. Next, the patterned resist-covered wafers were loaded into the system and the pressure in the chamber was reduced to a base pressure of 1.0 mTorr over 20 s with a 10 s stabilization check. A helium leak check was performed to ensure the wafer was in firm contact with the wafer platen by introducing helium underneath the wafer and measuring the change in pressure of the cavity between the wafer platen and the wafer over a 1 min period. If the leak rate was below 30 mTorr/min it was deemed the wafer was in proper contact with the wafer platen and etching was allowed to proceed. Otherwise, the wafer was unloaded and the back of the wafer was inspected to ensure cleanliness and was reloaded into the chamber to try to pass the leak test again.

Once the leak test was passed, the etching and passivating gasses were introduced to the chamber and a plasma was lit to start the etching process. The flow rate of the passivating gas, C_4F_8, was held at 60 sccm and the flow rate of the etching gas, SF_6, was held at 80 sccm throughout the entire etching step. The operating pressure of the chamber during etching was held at 20 mTorr ± 5%. The coil power used to create the inductively coupled plasma was 750 W at frequency 13.56 MHz. The total amount of etching time was varied to obtain trenches of different depths, with four different etch times being explored. The different etch times used were 1 min, 1.5 min, 2 min, and 2.5 min. An Alphastep 200 thin-film profilometer was used to

measure the trench depth formed by the various etch times after the resist was removed and depths of 1.1 μm, 2.0 μm, 2.5 μm, and 3.2 μm were found respectively.

After the etching of the trenches was complete, the resist was removed using a Branson 3000 Barrel Etcher using the standard plasma ashing process at the University of Alberta nanoFAB. Once the wafers were loaded into the chamber, the chamber was pumped down to a pressure of <200 mTorr. First, a nitrogen plasma is lit using at an operating pressure of 1 Torr for 3 min, with an RF power of 500 W to condition and warm the chamber to the operating temperature of 80ºC. After this, oxygen gas is introduced to the chamber at a pressure of 1.4 Torr and a plasma is lit at 600 W RF power for twenty minutes to remove the resist. The wafers are then cleaned with piranha using the process described in section 5.1 to prepare them for oxidation.

6.2 Thermal Oxidation

Thermal oxidation is a required step in the device fabrication process as it provides an insulating layer to prevent the deposited metal layers from contacting the silicon and forming an electrical path in parallel to the device (a short). Forming a thick oxide allows for the added benefit of increasing the aspect ratio of the trench. This is due to the fact that when forming a thermal oxide on silicon, 55% of the thickness of the formed oxide layer protrudes out from the original position of the silicon surface. Therefore the depth of the trench will not change as the bottom of the trench and the top surface of the wafer both have their normal vectors pointing in the same direction, but the trench will get thinner as the trench walls have their normal vectors pointing towards each other. Therefore the trench will thin by twice the distance the oxide grows above the surface, or $1.1t$, where t is the thickness of the grown oxide. This fact helps to make up for the overdeveloping and overexposing that had to be done for the photolithography step to work.

It was decided that growing approximately 500 nm of oxide was a good initial test to determine how thick of an oxide could be grown successfully in the trenches. Initially the smaller sized trenches were used as the issues with the photolithography process step had not yet been discovered. The standard thermal oxidation procedure for the University of Alberta nanoFAB was followed to produce the oxide. The wafers were placed in a wheeled quartz boat and rolled

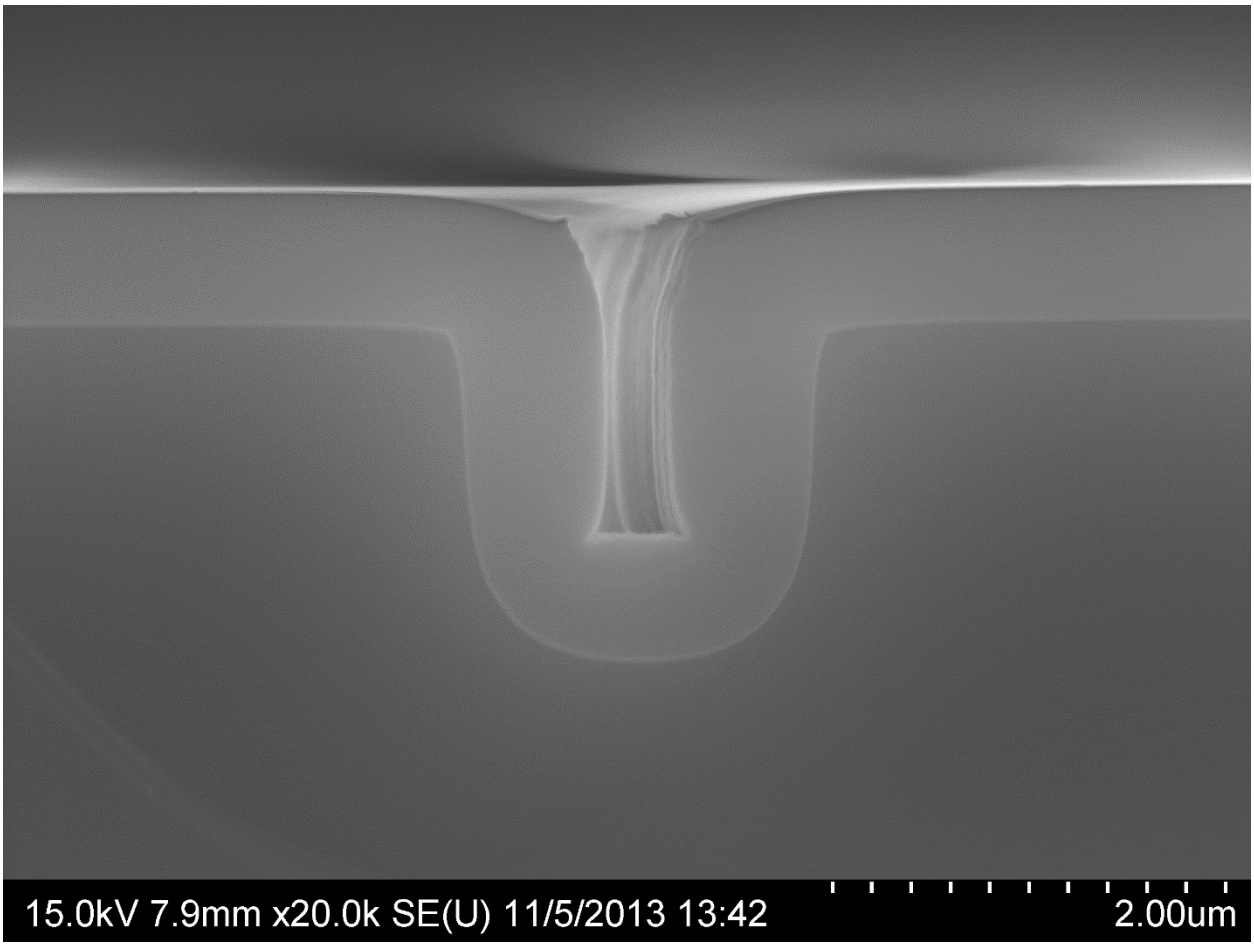


Fig 6.1 – SEM image of a 2.5 µm deep trench. Width of oxidized trench is 357 nm.

into the center a Thermco Mini Brute quartz-tube furnace. Nitrogen was bubbled through de-ionized water held at 94 °C at a flow rate of 40 sccm to generate the flow of oxidizing water vapour in the tube furnace. The tube furnace was ramped up to 1000 °C over the course of 45 min and was held at that temperature for 1.5 hr. The flow of gas was then stopped and the wafers were left to cool to 200 °C over a 4 hr period before they were removed from the furnace.

As seen in figure 6.1 very small trench widths could be obtained with this method when photolithography was performed without overexposing and overdeveloping. The trench shown has a width 357 nm with a depth of 1.86 µm, giving an aspect ratio of approximately 5.2. With initially narrow trenches, oxidation can actually completely close the trench off and fill it in as seen in figure 6.2 on the next page. The trenches also display the well-known effects of oxidation of non-planar silicon surfaces, as the sharp initial corners of the trench become rounded out over the course of oxide growth [58]. Silicon surfaces with curvature undergo less oxide growth than

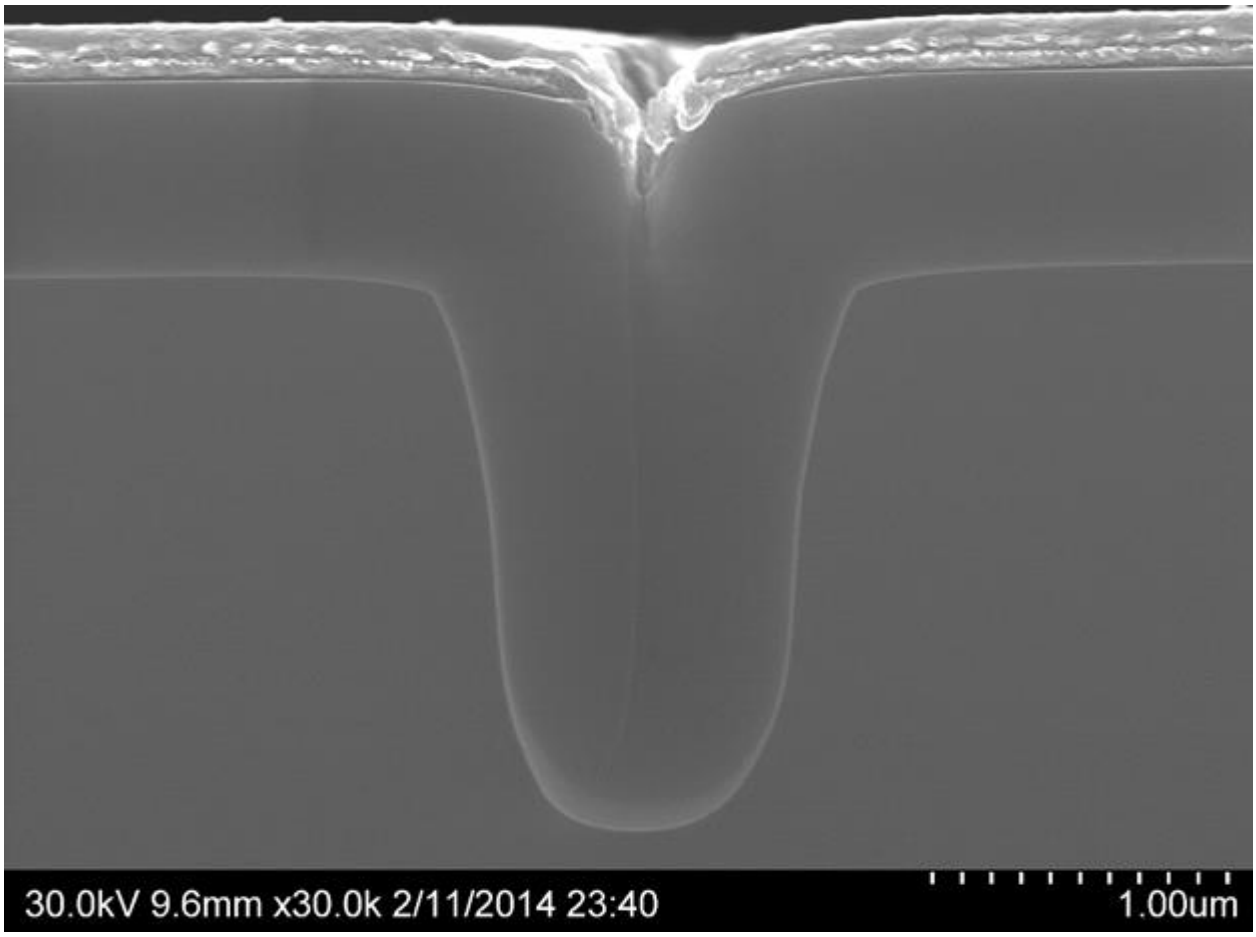


Fig 6.2 – SEM image of a completely closed off trench with metal layers deposited on top, to be discussed in chapter 7.

planar surfaces when exposed to the same oxidation environment [58]. The smaller the radius of curvature of the silicon surface the slower the growth rate, with convex curvature oxidizing faster than concave curvature. This fact naturally leads to the rounding out of corners as is demonstrated in figure 6.3 on the next page. Corners are areas of extremely high curvature and thus grow slowly. Thermal oxide growth also involves viscous deformation of the previously grown oxide by the newly formed oxide [59]. This flow then combines with the slow growth of highly curvature silicon to round out the corner for the convex case at the top of the trench and pinch in the corner for the concave case.

The source of the reduced growth rates for curved silicon surfaces is the increased stress formed in the oxide when growing in a non-planar fashion. For both the convex and the concave curvature, a compressive stress is generated in the radial direction (the direction normal to the silicon surface) [59]. Newly forming oxide at the silicon-silicon oxide interface must overcome

this increased energy barrier to formation. Therefore the reaction rate constant at curved interfaces is reduced due to the higher energy of formation. The reason that convex and concave surfaces have different reaction rates is that the circumferential stresses for both cases are different [59]. In the convex curvature case, the circumferential stress is tensional, which allows for increased diffusion through the oxide by the water or oxygen which in turn allows for a higher concentration of oxidants at the silicon surface, helping to increase the reaction rate. In the concave case the circumferential stress is compressive, which has the opposite effect of decreasing the diffusivity of oxidants in the oxide, and in turn the concentration of oxidants at the silicon-silicon oxide interface, reducing the overall reaction rate.

When the issues with photolithography came to light, it was decided that a longer oxidation would be used to make up for the further increase of size of the trenches. The same procedure was followed as above, but instead of 1.5 hours of exposure to oxidants in the quartz tube furnace the wafers were exposed for 4 hours. Oxidizing for this long, however, introduced extreme stresses onto the trenches, as continued oxide growth produces more and more stress in the oxide layer as the thickness increases [59]. This often led to heaving in the oxide layer, where the oxide at the bottom of the trench protruded out, completely destroying the profile of the trench as seen in figure 6.4 on the next page. Not only that, but the oxide thickness would not increase much past the 500 nm in the 1.5 hour oxidation. Thus it was decided that increasing the oxidation time would not completely solve the problem that the photolithography issues would introduce and the 1.5 hour oxidation time was kept as the standard oxidation process, which

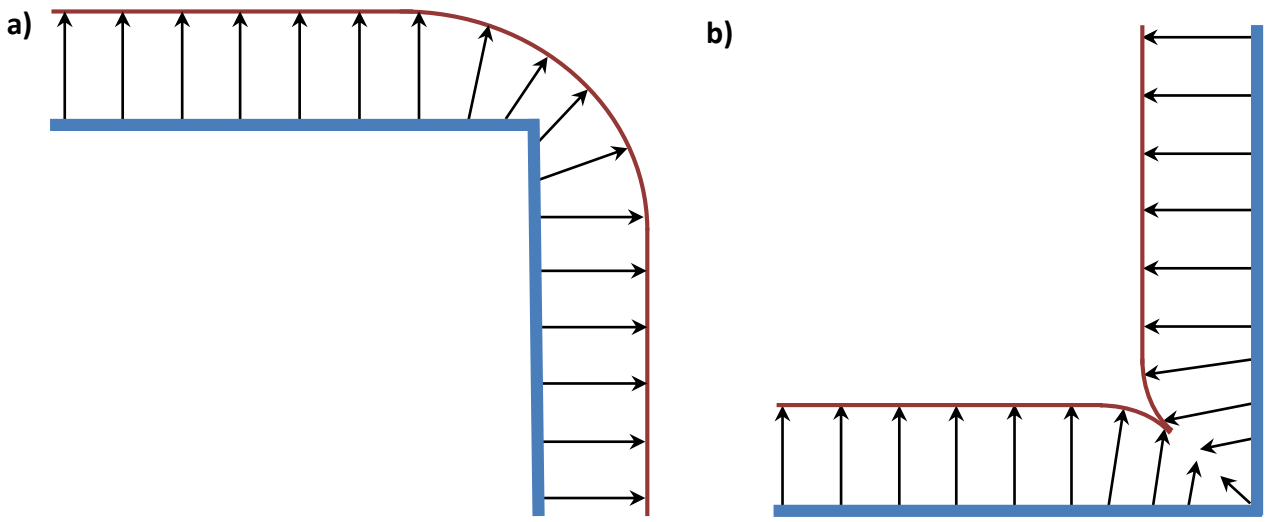


Fig 6.3 - Formation of curved oxide surface (red) from when starting from a) convex and b) concave corners in the original Si surface (blue). The black arrows show the direction and speed of oxide growth

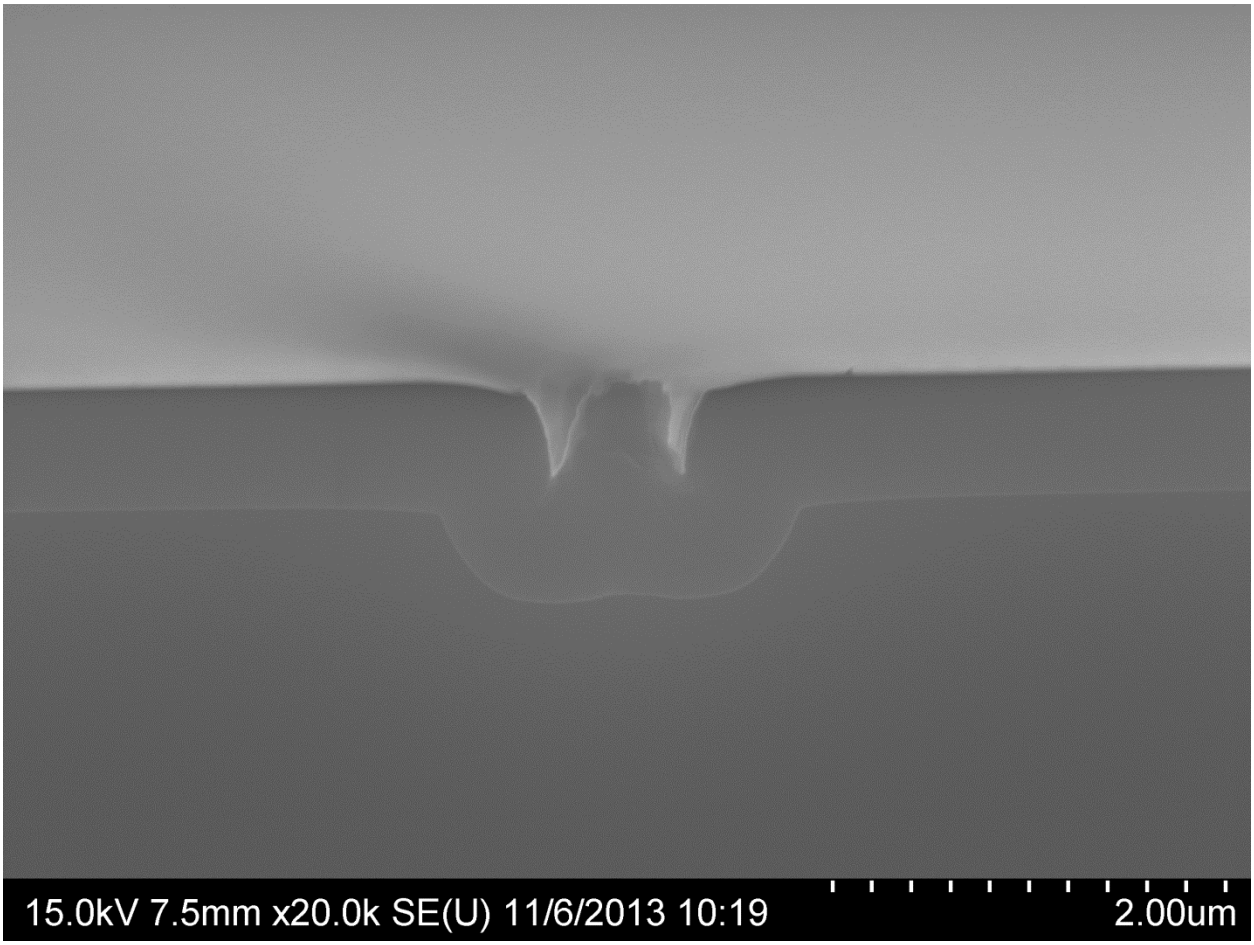


Fig 6.4– SEM of heaved oxide after 4 hours of oxidation at 1000°C

limits the minimum trench width to one micron.

Chapter 7: Metal Layer Formation Through Glancing Angle Deposition

7.1 Choice of Metal Layers

As discussed in chapter 2, the work functions of the contacts need to be at the proper value with respect to the LUMO of the electron acceptor and the HOMO of the electron donor. In the case of the electron-accepting contact, the work function ideally would be a higher value than the LUMO of the electron acceptor while the work function of the electron-donating contact ideally would be a lower value than the electron donor. In the P3HT-PCBM absorbing system PCBM is the electron acceptor, with a LUMO of 4.0 eV, and P3HT is the electron donor, with a HOMO of 5.0 eV. In a standard P3HT-PCBM cell, the electron-accepting contact is aluminum, with a work function of 4.2 eV and the electron-donating contact is transparent indium tin oxide (ITO), with a work function of 4.7 eV [60]. Since a transparent conductor is not required for the vertical contacts a different contact can be used in the place of ITO, one of the benefits of the device design as discussed in chapter 2. Another benefit of this design is that both electrodes are reflective, causing light to bounce between the contacts which increases absorption.

The work functions of metal films can vary depending on the depositions conditions and the film crystallinity [61]. Even purely crystalline metal layers will have different work functions depending on which crystal plane is exposed to vacuum [61]. To avoid the issues caused by the variation of metal work functions, it was decided to use a metal that had a small range that was close to 5 eV, while still being amenable to vacuum deposition. The metal that best fit this description was nickel, as it has a work function range of 5.04 eV to 5.35 eV and deposits well using e-beam deposition, the method of choice for this project [61]. The reason e-beam deposition was a requirement is discussed in the next section. The work function range of nickel is not exactly ideal for an electron-donating contact as the value of it is not lower than 5.0 eV. It is still the most ideal metal found for this project however, as the range is such that it will not ever switch between being higher or lower than 5.0 eV depending on deposition conditions,

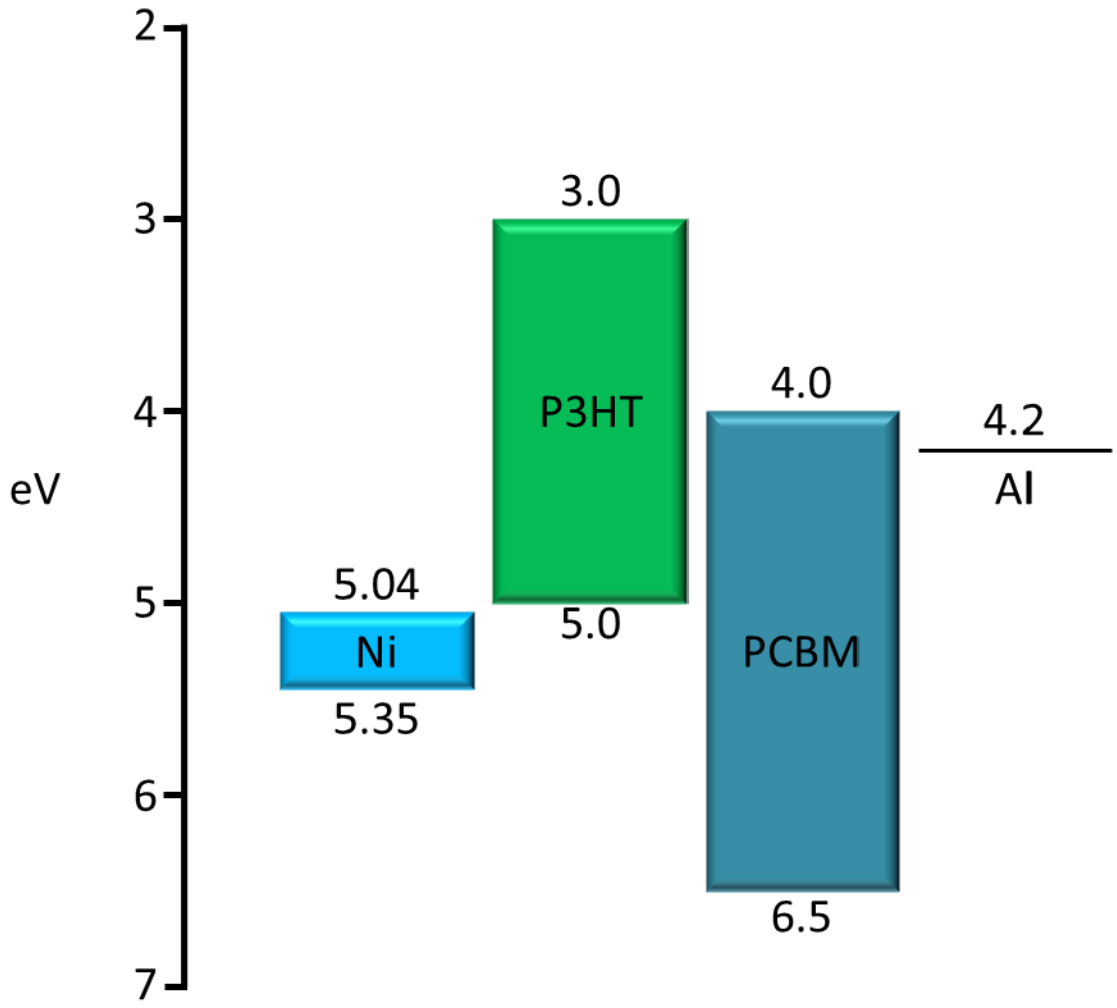


Fig 7.1 – Band diagram of prototype device

yielding more consistent electrical behavior, and the range is the smallest out of all the elemental metals with work functions close to 5.0 eV [61].

7.2 Initial Deposition Method

To controllably deposit the aluminum and nickel films onto the sidewalls of the trenches, a highly directional and collimated source needed to be used for deposition of both metals. This collimated source allows the film to be deposited at a controllable angle to ensure the bottom of the trench remains metal-free, and therefore ensuring no shorting between the metal layers. In addition, the metal layers needed to be deposited onto opposite sidewalls to form the cell. The ideal method to deposit the two metal films in this way is glancing angle deposition (GLAD).

In GLAD [52], a highly collimated vapour flux is required and is typically generated by high vacuum e-beam deposition of a source material held far enough away from the substrate to approximate a point source [62,63]. The substrate is held at a variable glancing angle α with respect to the vapour flux, where α is defined to be 0° when the substrate is orthogonal to the vapour flux, as seen in figure 7.2a. The substrate can then also rotate about the substrate normal, by an angle φ. This technique is typically used to generate various types of columnar nanostructures by depositing at high enough α angles so that the early film nucleation sites shadow the rest of the substrate. Typically $\alpha > 80°$ [62,63]. This substrate shadowing makes it so that only the early nuclei receive any vapour flux and are thus the only growth points of film, as seen in figure 7.2b. The film growth being constrained to the early film nuclei is what drives the growth of the columnar structures, demonstrated in figure 7.2c. Film growth is constrained to the nuclei only if adatom diffusion is sufficiently low. If φ is held constant, the film will grow as a series of columns with an inclination angle of β, which is measured with respect to the substrate normal [62,63]. To generate other types of columnar nanostructures, such as vertical posts, chevrons, helices, tilted columns, or any combination thereof, φ is varied while the film is growing to change the azimuthal direction of the incoming flux from the perspective of the substrate.

How GLAD was used to deposit metal onto the trench sidewalls in a continuous film is described below. The oxidized wafers were first cleaved utilizing the backside dicing method described in chapter 4 to obtain long 1 cm wide substrates with a single size of trench in the middle. The substrates were then adhered onto a six-inch circular aluminum deposition chuck using vacuum tape such that the trench was in line with the diameter of the circular chuck. The chuck was then mounted in a custom Kurt J. Lesker AXXIS e-beam deposition system outfitted for GLAD depositions. The φ angle was then adjusted, which in the AXXIS system rotates the circular chuck, so that the trench line will always be orthogonal to α. This orthogonality allows one of the trench sidewalls to shadow the bottom of the trench when α is set to the correct value, as seen in figure 7.3. With the φ angle set at the correct value the vacuum chamber was closed and was pumped down below 2.5 μTorr. Initially α was kept at 100° to

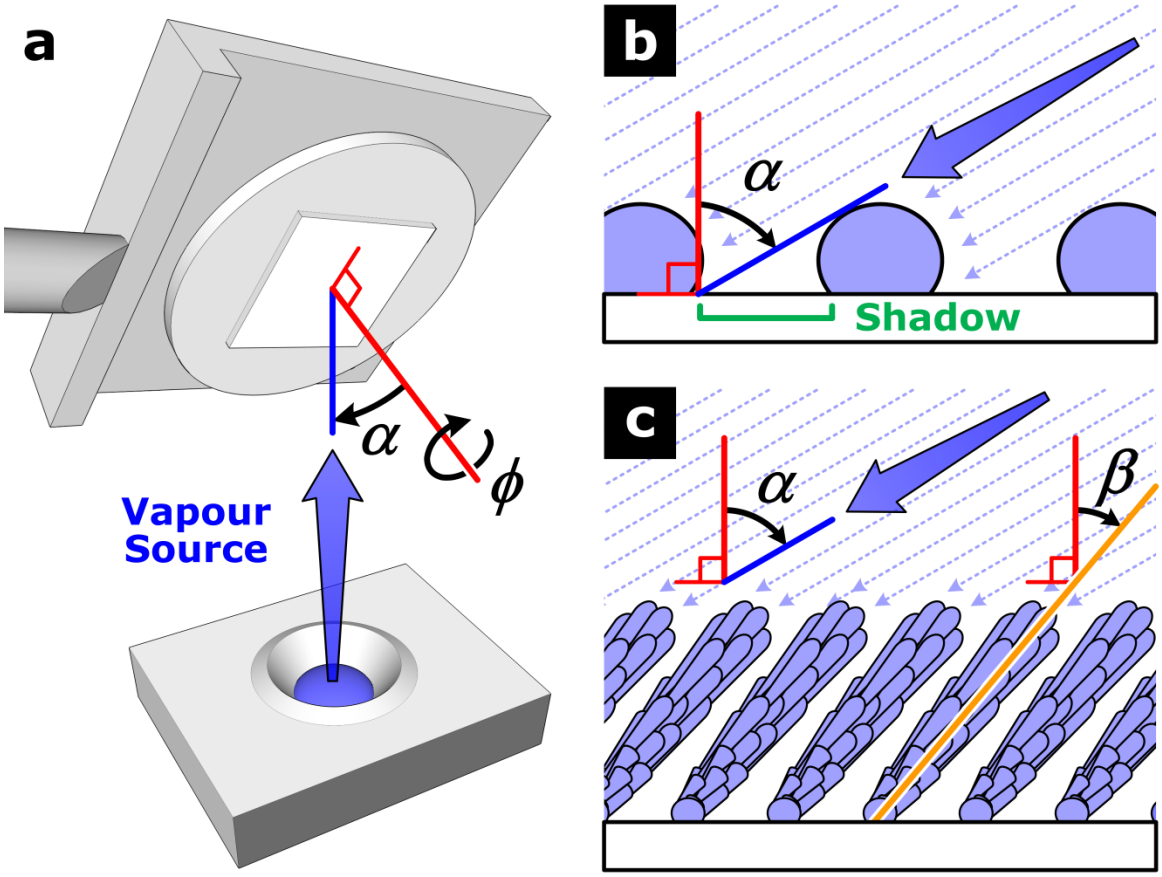


Fig 7.2 – a) Geometry of chuck, wafer and source in a GLAD system b) shadowing of the substrate by initial film nucleation c) GLAD post formation from initial film nucleation. From S. Jim and M.J. Brett [63]

allow the metal deposition source to be conditioned without depositing onto the substrate.

The nickel film was the first film to be deposited using a 6.3 kV electron beam moving in a spiral pattern using 99.995% pure source material. The beam pattern used during the nickel deposition was a spiral pattern and during conditioning the pattern covered the entirety of the source material. Since the melting temperature of nickel is much higher than that of aluminum (1455 °C vs 660 °C), a much higher current was needed, and thus a longer conditioning time was required when compared to the aluminum. The beam current was increased in increments of 10 mA approximately every minute until it reached a value of 270 mA, bringing initial conditioning time to roughly 24 min. At this point, the nickel would melt and the current would then be increased in increments of 5 mA every minute, while also decreasing the radius of the spiral pattern down by 20% of the original radius on every current increase. This was continued until a

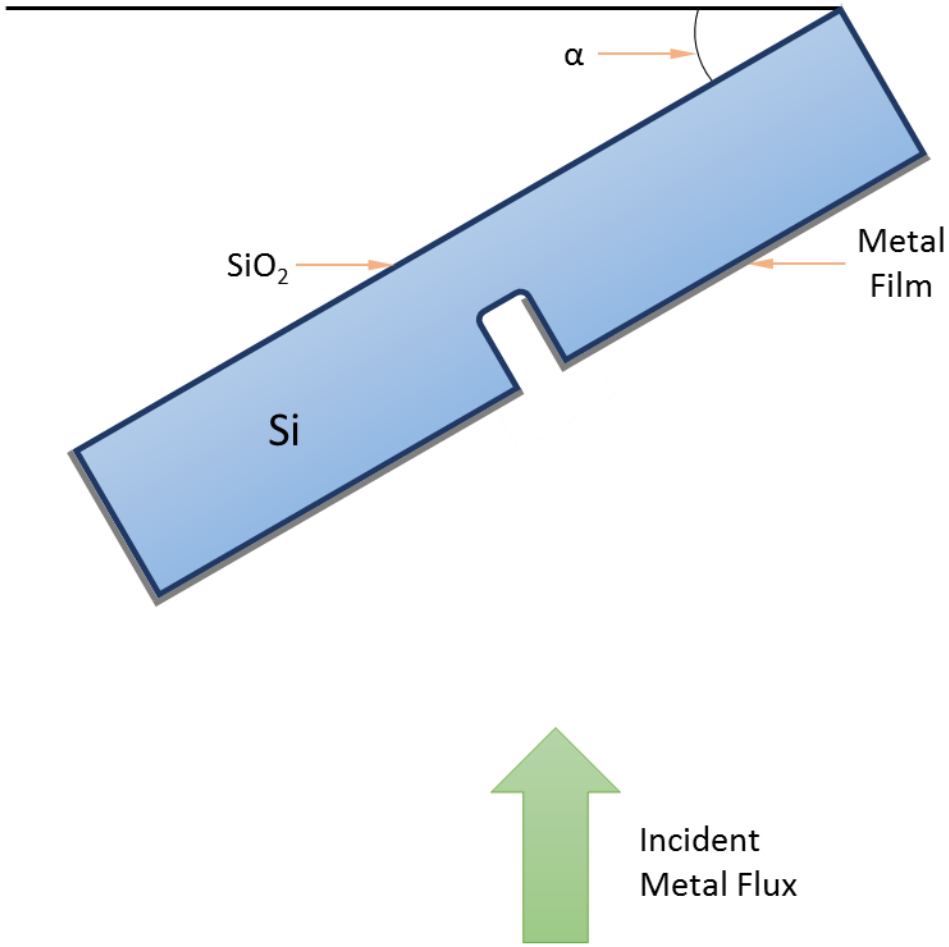


Fig 7.3 – Using GLAD to coat sidewalls of the trench. Substrate held at an angle so bottom of the trench is shadowed from the collimated flux.

current of 290 mA was achieved and the beam pattern radius was 20% of the original value. The beam current was then increased in increments of 5 mA until a deposition rate of 10-11 Å/s was achieved as measured by a quartz crystal thickness monitor. The range of beam current in which this deposition rate would occur was 290-340 mA. Such a high deposition rate was chosen so that the film would have a low amount of impurities to ensure the film had consistent electrical properties. With the proper deposition rate achieved, the source material was shuttered and the substrate was moved into the appropriate α angle. How the correct α was determined is discussed further in depth below. Once the substrate was in position, the shutter was opened for 100 s to deposit nominally 100-110 nm of nickel onto the substrate. Once the deposition was completed, the source was shuttered and the substrate was moved to $\alpha = 180°$ to prepare for substrate removal. The beam current was slowly ramped to zero over the course of one to two minutes to help prevent rapid cooling from cracking the crucible.

Once the system had cooled a sufficient amount, the nickel-containing crucible could be removed. The system was vented and the crucible was exchanged for one containing 99.99% pure aluminum source material. The angle φ was then increased by 180° to deposit the aluminum onto the other trench sidewall. The chamber was then closed and again pumped down below 2.5 μTorr. Once this base pressure was achieved the 6.3kV e-beam was started at 30 mA. The aluminum source material was conditioned for approximately 15 min by starting the electron beam current at 30 mA and increasing the current by 5 mA roughly every minute up to 100 mA. During this initial conditioning step the spiral e-beam pattern was sized to cover the entirety of the source material. Once the beam current had reached 100 mA, the source material melted. During this time, the current was again raised by 5 mA approximately every minute but also the spiral pattern radius would be reduced by 20% of its original size every time the current was increased. This was continued until the radius of the spiral overall was 20% of the original size of the pattern and the current was raised to 120 mA. At this point, the current was adjusted, again in increments of 5 mA approximately every minute, so that a deposition rate of 10-11 Å/s was achieved as measured by a quartz crystal thickness monitor. The current range in which this deposition rate would occur was 120 mA to 150 mA.

Once the proper deposition rate was achieved the source was shuttered and the substrate was moved into the correct α position so that the vapour was only deposited at the correct angle. With the substrate in the correct position and orientation the shutter covering the source material was opened for 100 s to allow the aluminum to deposit onto the substrate to give a film that was nominally 100-110 nm thick. The shutter was closed after 100 s and the substrate was moved back to α = 100°. The e-beam current was slowly ramped down to zero over the course of one to two minutes to help prevent crucible cracking and the system was left to cool for approximately one hour. The system was then vented so that the substrate could be removed. The substrate was then cleaved into the small 1 cm by 3 mm pieces that were defined by the backside dicing and a resistance measurement was performed using a hand held digital multimeter to ensure the trench was open circuit before polymer infill.

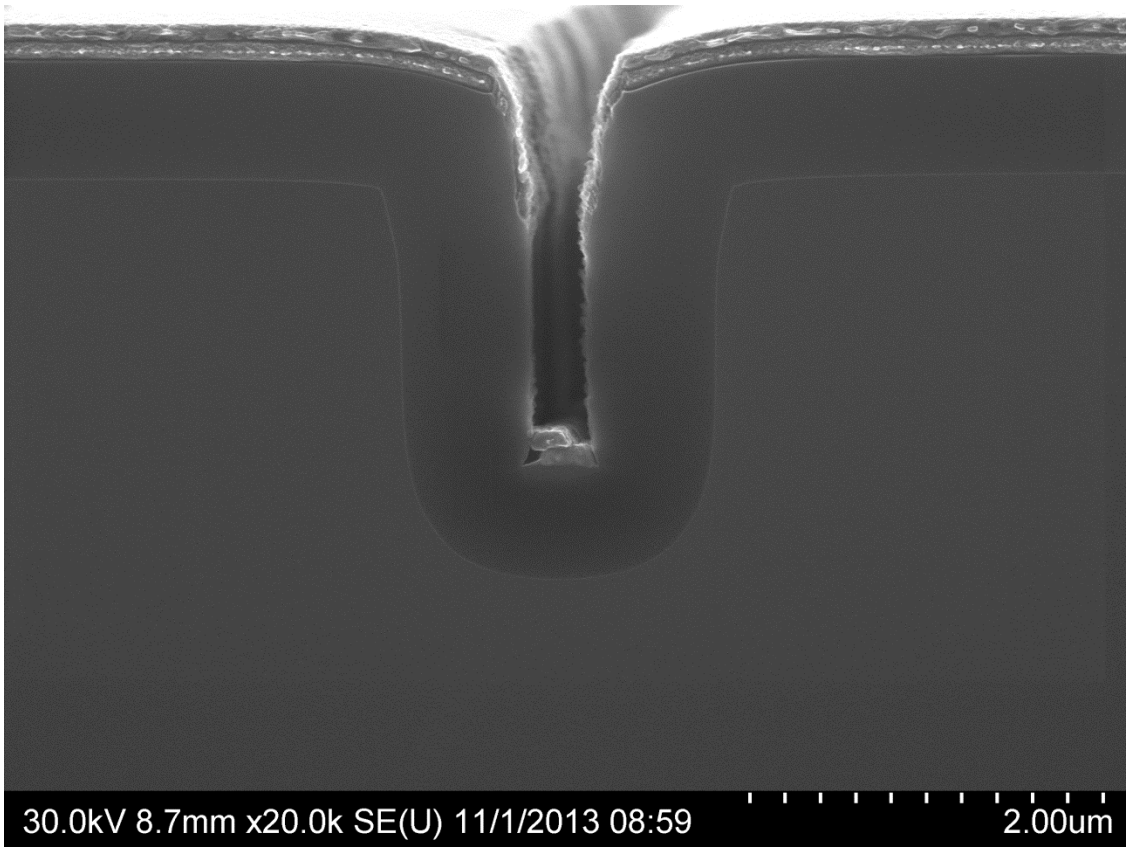


Fig 7.4 – Trench with metal deposited at too shallow of an angle so bottom of trench was not shadowed from flux.

To ascertain the value of α that would cover the whole sidewall but not the bottom of the trench, a geometric calculation was initially done. The depth of the etch after oxidation was measured by using an Alpha Step 200 Profilometer on some of the etched lettering on the wafer. The oxidation layer thickness was then measured with a Filmetrics Resist and Dielectric Thickness Mapping System. Using both of these measurements as well as the initial trench width as defined by mask line widths the geometry of the oxidized trench was estimated. This was done by using the fact that during silicon planar oxidation, 55% of the new oxide layer grows above the original silicon surface [64]. The depth of the trench was estimated to be the same as before oxidation as the oxide growth direction of the bottom of the trench and the top surface layer are parallel. On the other hand, the width of the trench was estimated to become thinner by a factor of 1.1 of the oxide thickness as the trench sidewalls' oxide growth direction is antiparallel and each side will grow by 0.55 of the oxide thickness toward each other. With the trench geometry after oxidation estimated finding α was a simple act of trigonometry. Unfortunately, using this simple geometry-based estimation led to severely low resistance shorts, with resistances on the order of tens of ohms. When these devices were characterized with an

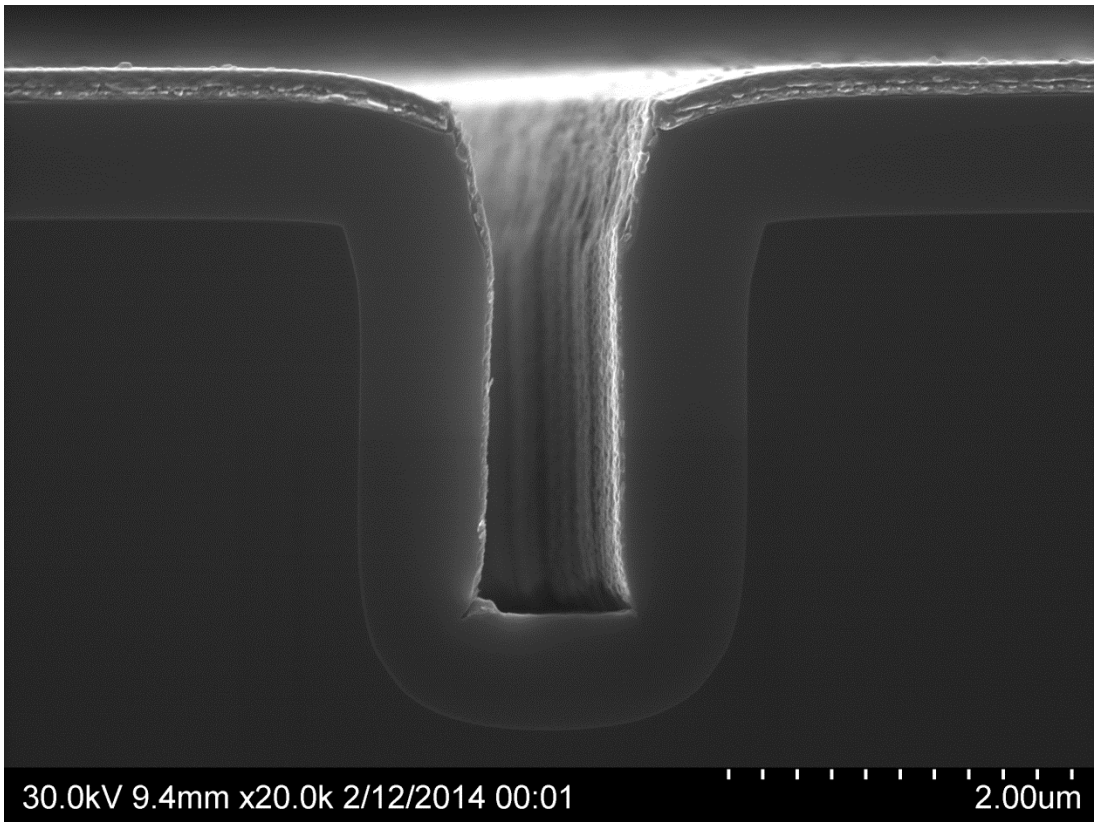


Fig 7.5 – Trench with metal coated sidewalls with bottom of trench metal-free.

SEM, it was discovered that the metal films were overlapping at the bottom of the trench, as seen in figure 7.4. This overlap showed that the α angle derived from the geometry approximation was in error. It was discovered that there were two main sources of error in the approximation. The first error was the fact that the corners of the trench oxidize at a much lower rate than planar oxide, as discussed in chapter 6, which rounds out the corners. This rounding increases the angle of acceptance for film growth in the trench, and thus increased the α angle required to deposit only onto the sidewalls and not the bottom of the trench. The next issue was the fact that the photolithography development was done by hand, which lead to large enough deviations in the trench width that it could not be accurately ascertained to the level required for the geometric approximation. Therefore it was decided that before metal film deposition the geometry of the trench would be characterized using SEM and thus an accurate value for α could be obtained. As seen in figure 7.5, this method was much more successful in obtaining the proper α angle. The exact α required varied with the exact geometry of the device, but normally fell within the range of 20º ± 2º. As seen in figure 7.5 the metal films were rough, and dense enough to form a contiguous coating.

7.3 Burnout Testing

Once the metal overlap issue caused by the usage of incorrect α angles was resolved, the low ohmic device shorts were reduced but not entirely eliminated. Further investigation into the trenches through SEM characterization led to the discovery of the photolithography issues discussed in Chapter 5. With those issues resolved, the rate of devices that suffered from low ohmic shorts was reduced to less than 10%. Devices that did not suffer from this low resistance issue still showed a measurable resistance value however, typically in the range of 100 kΩ to 5 MΩ. A small amount of devices, approximately 10%, had resistance values on the order of 10 kΩ as well. In an effort to obtain open circuit devices, a burn out test was attempted on multiple high ohmic devices. The idea behind the burnout method is to expose the device to a high enough voltage that the resulting current that is running though the device will heat the small metal overlaps or dust molecules that are causing the short within the trench. When a sufficient temperature is reached it will ablate the metal overlap or destroy the particle causing the short, and hence 'burn out' the short resulting in an open circuit device.

As it was unknown for each device what exactly was causing the short, a general method was developed so as to not unnecessarily expose a device to high voltages and cause damage to it. First, the device would have its resistance measured and recorded. During these resistance measurements, it was noted that the high-resistance devices had a different resistance depending on which side of the contacts the DMM leads were attached, showing diode-like behavior. This suggested that the short in the trench was not a simple metal overlap, and was like some kind of semiconducting particle. One possible source of this was particles created during the substrate cleaving finding their way into the trench. For completeness, both resistance measurements for the device were recorded.

With the resistance measurements recorded, the devices were connected to a voltage supply in series with DMM in ammeter mode. The supplied voltage was initially held at one volt for one minute and the current was monitored to see if it ever dropped to zero. If the current did not drop to zero after one minute the voltage was increased to 2 V over five seconds and then again held there for a minute to see if the current would drop to zero. This pattern was repeated with the following voltage steps: 1V, 2 V, 5 V, 7 V, 10 V, 15 V, 20 V, 25 V, 30 V, 35 V, and finally 40 V. None of the 13 devices tested ever had their current drop to zero with this process.

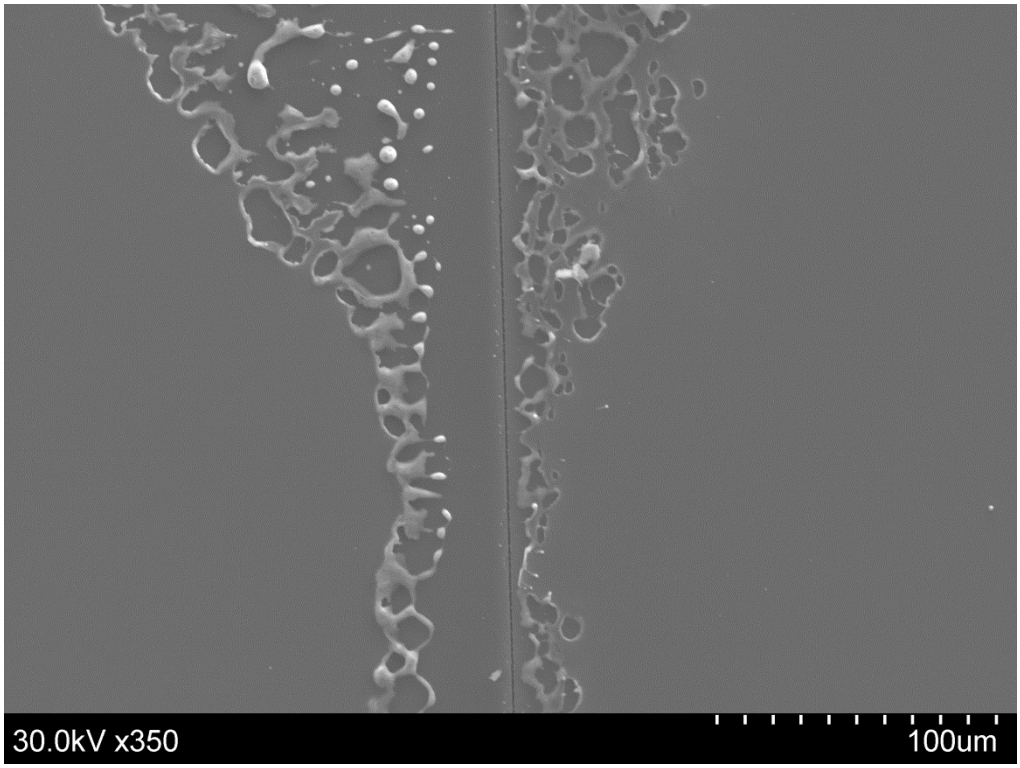


Fig 7.6 – Melted metal films from metal burnout process

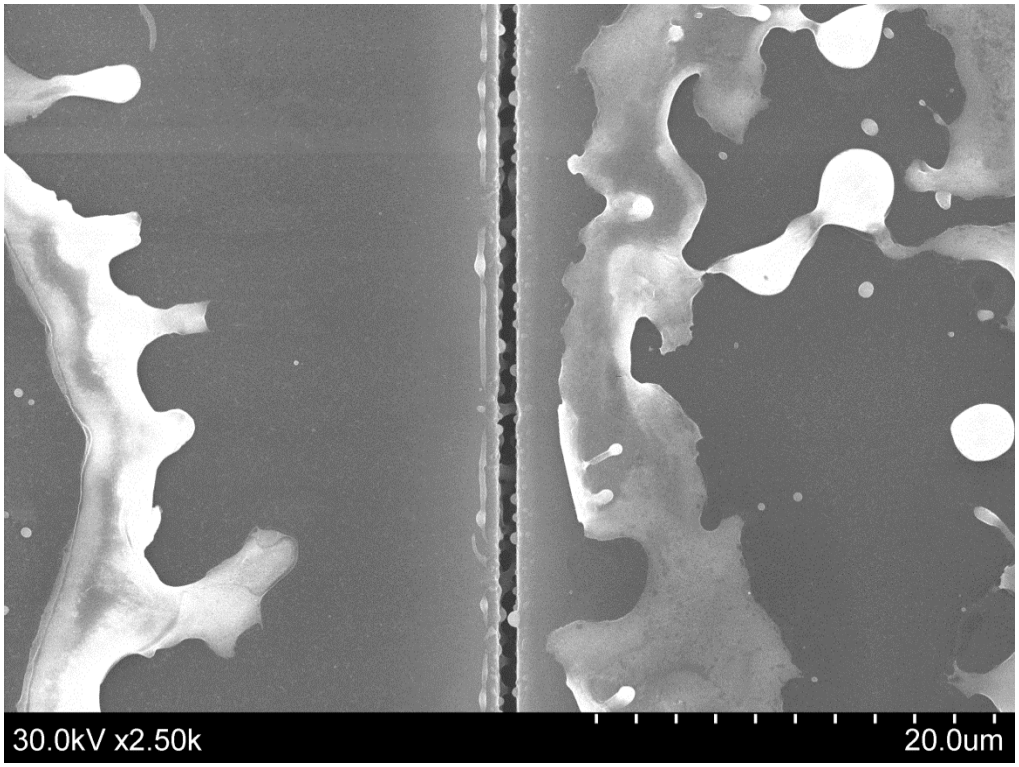


Fig 7.7 – Close up of melted films from burnout process. Film in the trench has formed solidified droplets that bridge the trench.

The devices displayed one of two patterns of behavior when exposed to this burnout process. Six of the devices would have the current stay the same or slightly drop during the increasing voltage, particularly after the 30 V mark. After burnout they would have roughly double the resistance that they started with. The other devices would follow the same kind of behavior but at the higher voltages an audible snap would be heard and the current would dramatically increase. Inspecting the trench by eye it looked much larger, likely meaning large-scale damage to the device. Looking at the damaged trenches under SEM confirmed this fact as the films appeared to have melted near the trench, as seen in figure 7.6 and 7.7.

This burnout film melting was likely caused by the following mechanism. The breakdown voltage of pure air is 3 MV/m, or 3 V/μm [65]. The trench width is on the order of a micron wide and therefore any voltage over 3 V will cause sparking from one side of the trench to the other. This fact is also likely why no device was successfully burned out. The contact overlaps in the trench were likely not greatly heated by a potential difference of 3 V or less. As soon as the voltage was increased to over 3 V sparks would carry current from one contact to other through the air, instead of more current flowing through the short. This sparking would cause very localized heating in the trench for a brief period after the spark, as well as serve to heat the whole film itself over time. As the voltage was increased the electrostatic forces attracting the two sides of the film would obviously increase, as well as increase the amount of sparking and therefore the overall film heating. As the film heats up, it becomes more and more pliable and loses adhesion to the oxide layer. Eventually if the film locally becomes hot enough due to a spark, the electrostatic forces between the two films on either side of the trench will overcome the adhesive forces and jump across the trench. As the film is continuous, this causes a chain reaction all along the length of the trench akin to peeling off a sticker. This leads to the audible snap and mass film destruction.

Since the burnout method could not successfully remove the metal film overlaps, another method needed to be investigated to remove them.

7.4 Focused Ion Beam Device Correction

With the failure of the burnout method at removing the device short it was then decided that focused ion beam milling would be performed to spot remove any errors seen in the trench

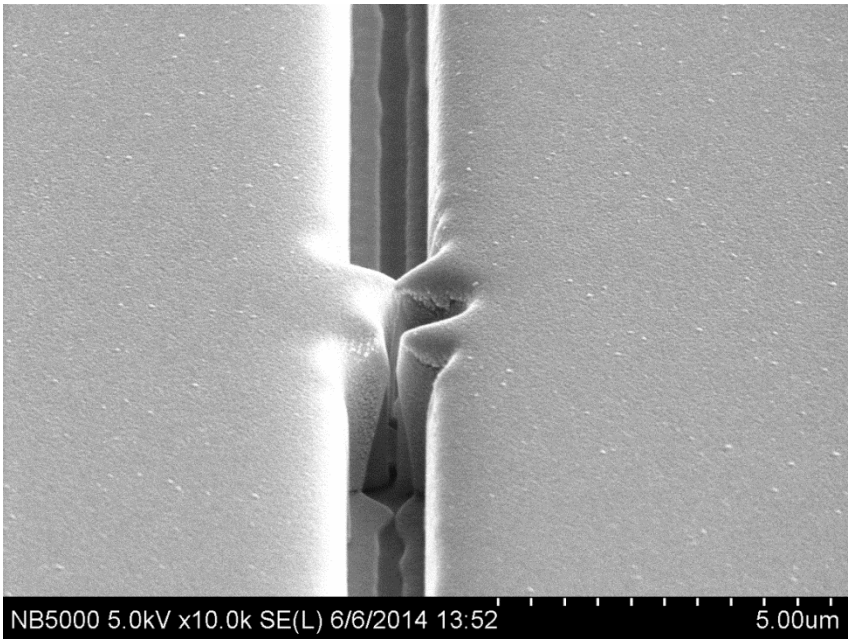


Fig 7.8 – Large error in trench geometry

along a whole device length. A handful of high-resistance devices were brought to the National Institute for Nanotechnology for ion beam milling. A Hitachi NB-5000 Dual (Focused Ion/Electron) Beam Microscope was operated by Martin Kupsta to locate any large errors in the trench with the scanning electron microscope function of the NB-5000. If an error was found it was blasted away with a directed burst of gallium ions. A pre and post-ion beam exposure of a trench error can be seen in figure 7.8 and 7.9. This was done along the entire length of the trench for three devices, removing any possible large-scale overlap. All the devices had their resistance change, but no device became open circuit after the ion beam treatment. Two devices had their resistance roughly double while the other one stayed approximately the same. For the device that stayed the same, it was noted that even though there were deviations in trench shape, it never appeared as though there were any metal overlaps over the whole trench and there was no large particulate bridging the trench. This led to the idea that perhaps the trench itself was not the source of the short, but the

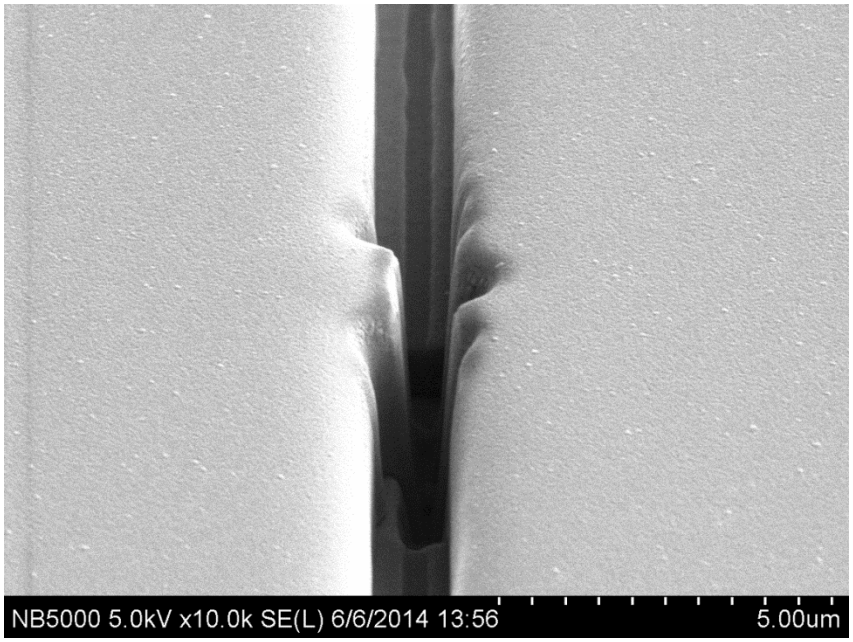


Fig 7.9 – Same error from figure 7.8 after FIB treatment

edges of device were. To test this theory, the focused ion beam (FIB) was used to remove material in a rectangular pattern, separating the middle of the trench and metal films from the edges. When this was done the resistance value of the device tested actually decreased by a great deal, by roughly a factor of ten. It is hypothesized that since the ions used to remove the material are conductive gallium, the ions that are being embedded into the device are actually forming another conduction path and so the device is not truly separated from the edge when this is done.

7.5 Thin Metal Sheet Resistance Modeling and Resistance Measurement Sweeps

To further explore the idea that the conduction pathway in the high resistance devices is forming at the edge of the device instead of the trench, a simple model was used to examine the possible dimensions of a metal short that occurs within the device trench. The model uses the basic formula for resistivity:

$$R = \frac{\rho L}{A} \qquad (8)$$

Where R is the resistance, L is the length of short, ρ is the resistivity and A is the cross-sectional area of the metal short. In the model a resistance of 100 kΩ is used, a very representative value of resistance for the measured devices, while for L a value of a micron is used as it is also an average value for the trench width. Both a purely nickel and purely aluminum short were tested in the model and therefore ρ values of 69.3 nΩm and 26.5 nΩm were used respectively [66]. For the cross-sectional area, a rectangular cross-section was assumed with the height of the short only being a monolayer thick. This thickness was chosen as it would give the limit in how wide the metal short could be in the trench. The height used in the model was therefore the diameter of nickel and aluminum atoms in a metallic bonding environment, 248 pm and 286 pm respectively [67,68]. Solving for the width of the short for both the nickel and aluminum cases values of ~3 nm and ~ 1 nm were obtained. Shorts of these dimensions, with a one micron long 1-3 nm wide strip and monolayer thickness, seem highly unlikely. When higher resistance shorts (some devices showed megaohms of resistance) are taken into account the width of a monolayer short required would be much thinner than an atom, which of course makes no physical sense. In light of this, it could be concluded that the high resistance shorts were not caused by metal overlap in the trench.

To inquire further about the nature of the high resistance shorts an IV sweep was done on two different high resistance devices. If the short was a metal to silicon contact a diode like IV curve would be expected due to the formation of a Schottky diode [51]. One of the devices was measured to be 2.2 MΩ / 1.6 MΩ using a DMM while the other was measured to be 548 kΩ / 99.7 kΩ. The two resistance values were obtained by measuring the device in both the forward and reverse direction with the DMM probes. The devices were swept from -1.0 V to 1.0 V in 0.1 V increments and the subsequent current was measured using a Keithley model 6482 dual channel picoammeter / voltage source. The result of the current sweeps can be seen below in figures 7.10 and 7.11. Both sweeps show obvious diode-like behavior and the higher resistance device shows a turn on voltage near 0.6 V, which is characteristic of a silicon diode. This suggested that for the very high resistance devices, in the MΩ range, the conduction path was somehow occurring though the silicon body. This motivated a review of the total device processing to discover where this metal to silicon contact could be occurring.

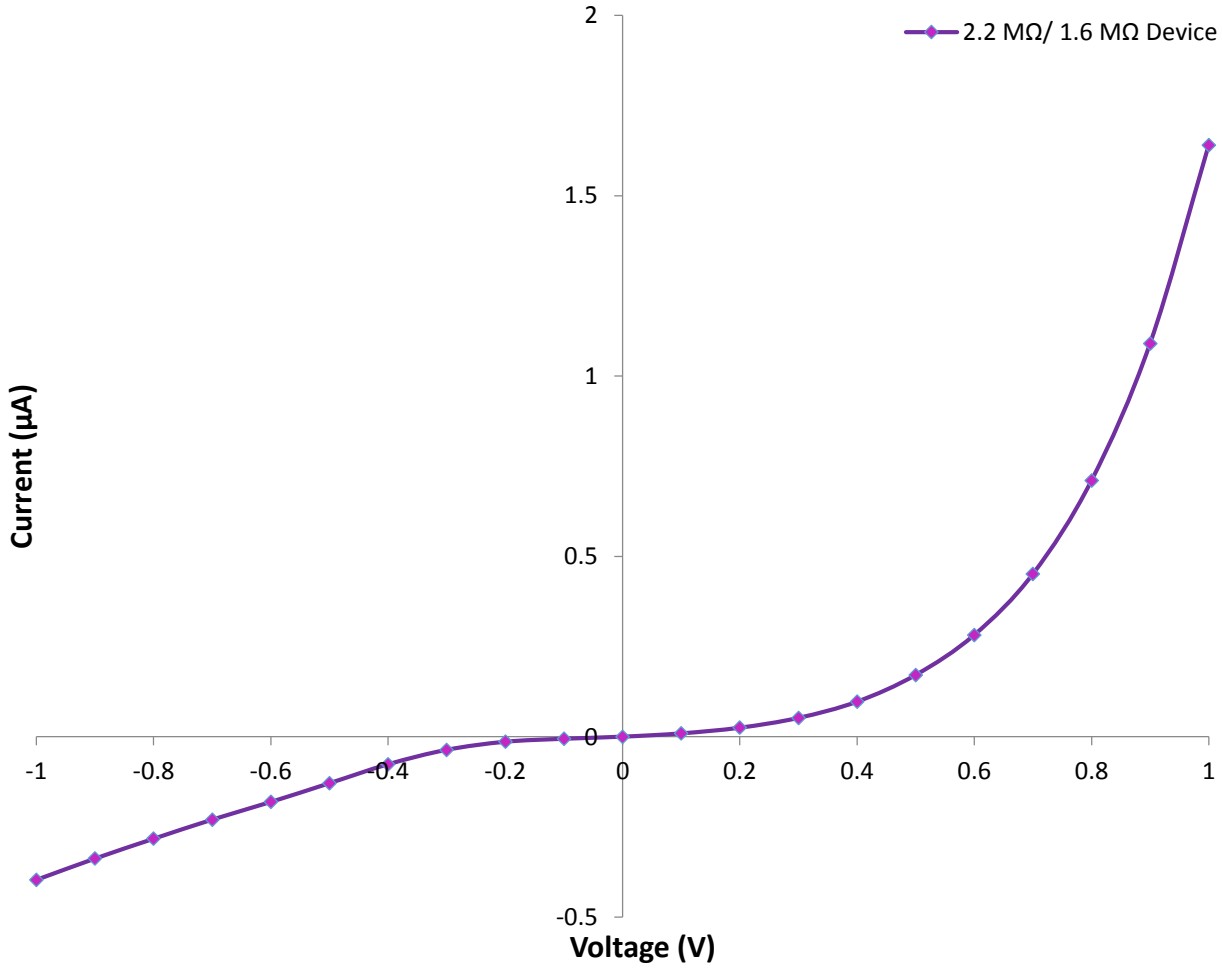


Fig 7.10 – IV curve of a high resistance shorted device

It was discovered during this review that the way the metal deposition was being performed resulted in metal coming directly into contact with the silicon body at the edge. The wafer was cleaved after oxidation to separate the trenches of different sizes, as the trenches of various dimensions had different optimal α angles. Cleaving the wafer after oxidation of course exposed the silicon body to possible metal contact. This in itself is not a problem so long and the entirety of the edges for each wafer piece were covered during the metal deposition. The standard method for substrates when being deposited in the AXXIS system was to use as little katpon tape (tape safe for high vacuum deposition) as possible and so only the corners of the wafer piece were taped down. This issue was corrected by taping down all the edges during deposition and resulted in the first open circuit devices with roughly a 10 % yield. With the issue solved the devices could finally be filled with P3HT:PCBM polymer blend and characterized under light and dark conditions.

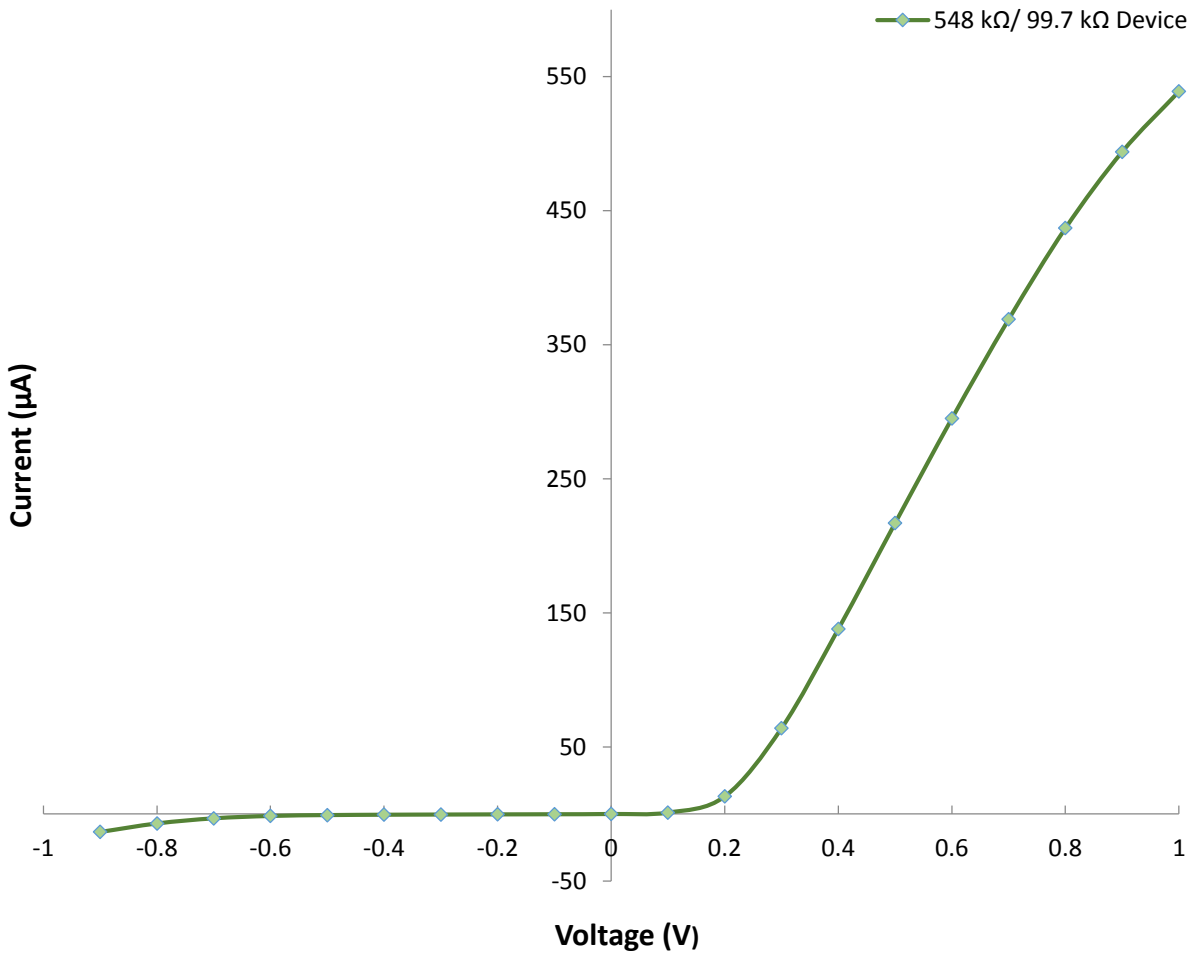


Fig 7.11 – IV curve of a mid resistance shorted device

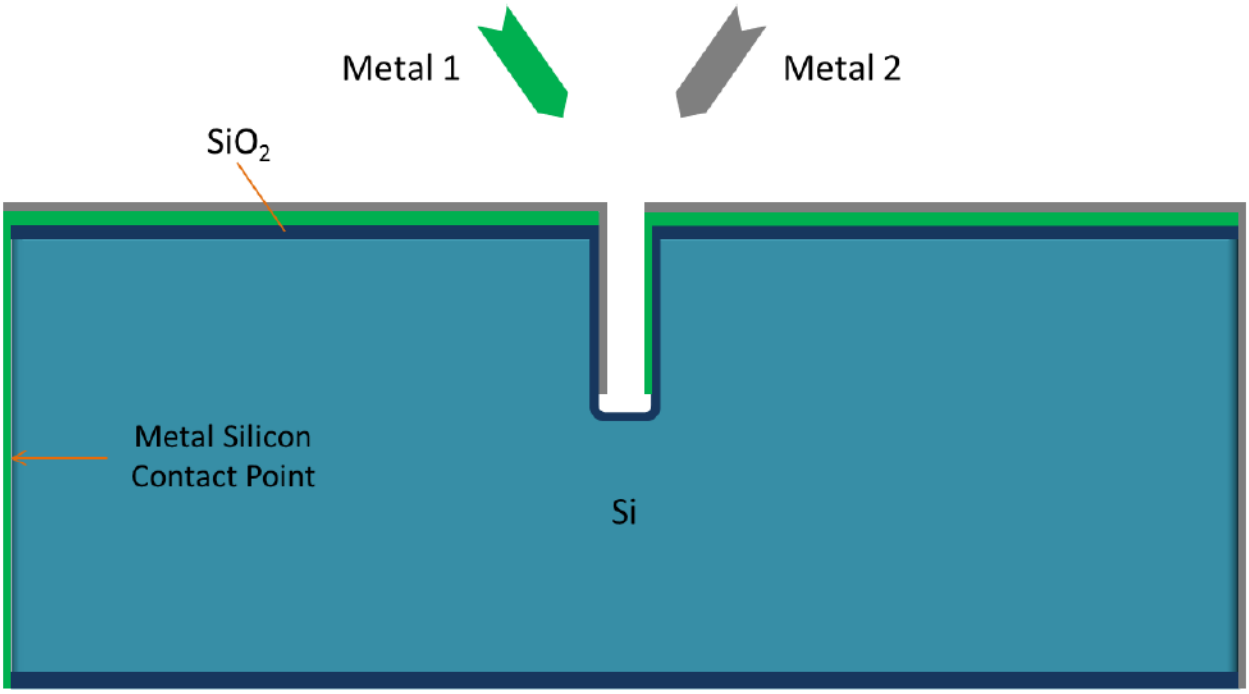


Fig 7.12 – Cartoon image illustrating the shorting point that occurred due to improper set up

Chapter 8: Device Filling and Characterization

8.1 Polymer Preparation

With the previous processing steps developed, the optimization of the polymer filling could be performed to maximize the power output of the devices. As mentioned many times before, the polymer system used for the device is the well characterized P3HT:PCBM polymer/small molecule mixture. The mixture was made using the standard recipe of the Buriak Lab at the University of Alberta, which is outlined below. All but the last steps of this process take place in a glovebox under inert argon atmosphere, due to both P3HT and PCBM being very sensitive to oxygen and water vapour [24,44].

First, 25 mg of P3HT is added to a Teflon capped vial with a magnetic stir bar. This process is repeated with 25 mg of PCBM into a seperate vial. 500 µL of ortho-dichlorobenzene is added to each vial using a 1000 µL micropipette. The vials are then left on a hot plate held at 75 ºC overnight to stir for at least 12 hours. After mixing overnight the PCBM solution is added to the P3HT solution and left to stir on the hotplate for an hour. The 1:1 (by weight) mixture of P3HT:PCBM is then taken out of the glovebox to be spun onto the devices. Before spinning takes place the solution is filtered through a 0.45 µm Teflon filter to remove any solid particles of P3HT or PCBM that have failed to dissolve. With the solution mixed and filtered spin speed optimization could take place.

8.2 Spin Speed Optimization

The spin speed and time required to fully fill the channel with minamal overburden is an important point of optimization. The reason is due to how strongly absorbing P3HT:PCBM is below a wavelength of 600 nm, as seen in figure 3.2b. If there is a large overburden of polymer, the vast majority of the photon energy absorbed will occur far away from the contacts that are within the trench. Thus any significant (>50 nm) amount of overburden will greatly reduce the efficiency of the device. The revolution speed used for the standard cells made in the Buriak Lab is 600 rpm for one minute and the polymer is spun onto planar indium tin oxide. This spin speed

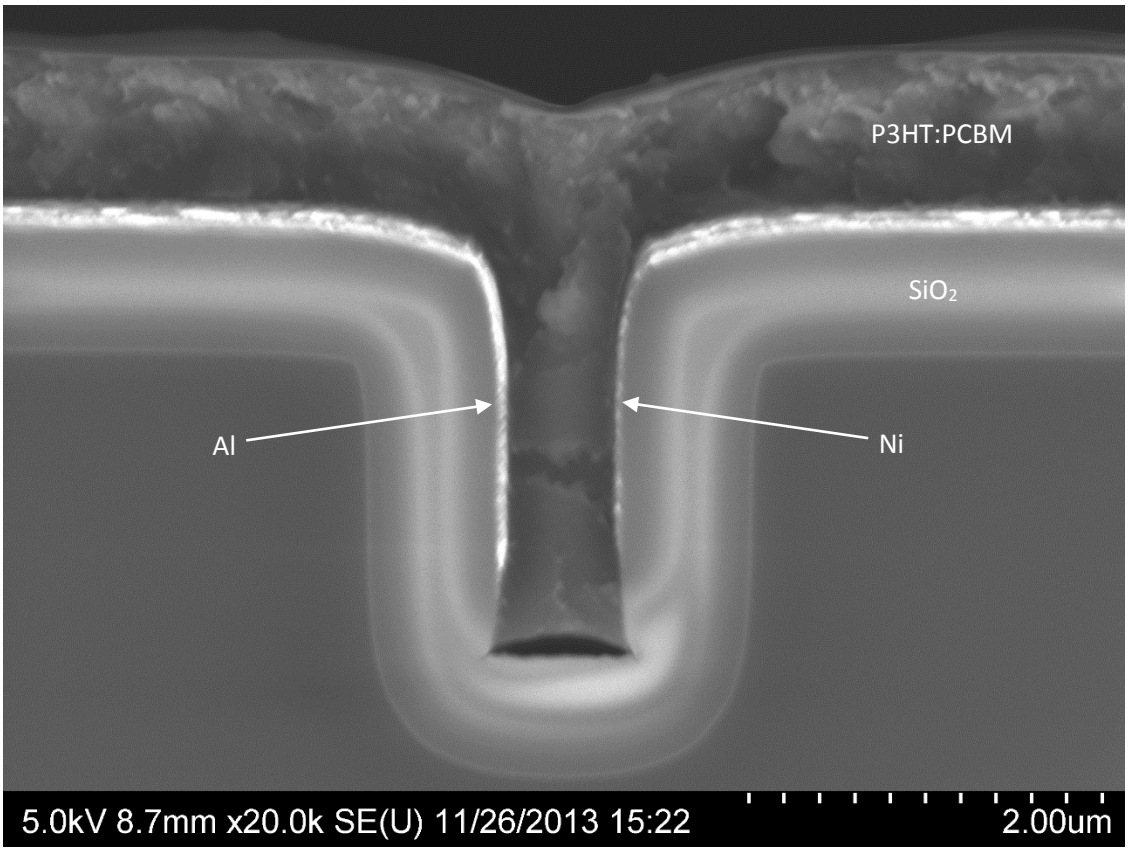


Fig 8.1 – Polymer fill of device that was spun at 600 rpm for one minute. Large overburden of polymer seen at this spin speed.

and time as a starting point for the device's polymer filling optimization. Due to the small size of the devices, it was also decided to use a 10 µL micropipette to place 5 µL of the polymer mixture on the center of the device before spinning. Once the spin took place, the ends of the devices were cleaned of polymer with a cotton swab that had been dipped in dichlorobenzene and the devices were left in a one-inch petri dish that had been covered in aluminum foil for the polymer to dry in the dark. Drying took place over the course of a half an hour. This initial spin speed and time led to full filling of the channel but with an extremely large overburden as seen in figure 8.1. To reduce this overburden, the spin time was increased to two minutes. This did not resolve the issue however as nearly the exact same results were seen when characterized via SEM. It was discovered that a 600 rpm spin speed was not high enough to cause the polymer mixture to wick off the exposed aluminum film, meaning that any increase in spin time would actually do nothing to reduce the overburden layer. Instead, a higher spin speed needed to be used.

Subsequent trials used a spin speed of 2000 rpm and tested varying spin times to see if the polymer layer could fill the trench with less overburden. Using 5 µL was also found to be an unnecessarily large amount of fluid to coat the small 10 mm by 3 mm devices and so the amount

was reduced to 2 μL. To further help the polymer wick off the device during spinning, it was held on a hot plate at 75 ºC for ten minutes after filtering took place. The polymer was then pipetted onto the device and spinning started within ten seconds to maintain the higher temperature during spinning. Again, the device was dried in a foil covered petri dish after spinning. The spin times used for the test were 60 s, 30 s, 10 s, and 5 s and the cross-sectional SEM images of the test samples can be seen in figures 8.2-8.5 respectively. The 60 s spin time can be seen to be far too long as the polymer has only filled halfway up the trench and alarmingly the polymer has delaminated from the sidewalls of the trench. This delamination completely removes the polymer to metal contact and would cause severe performance issues in functional devices due to the limited carrier extraction it would lead to. The 30 s spin time led to a much better trench filling, with more than three quarters of the trench being filled with polymer. There was some slight delamination of the polymer on one side of the trench but it is unknown if this is an issue along the entirety of the device or simply a localized effect of cleaving the device for SEM. The 10 s spin time also led to a roughly three quarter filling of the channel, very similar to the 30 s spin time. Both spin times also led to the same polymer surface profile and the same delamination could be seen occurring in the 10 s spin time, albeit on the bottom of the trench instead of the sidewall. This type of delamination is obviously much less damaging to potential device as the entirety of the metal films are in contact with the polymer, and it is also unknown if this type of delamination is localized to the cleave point or if it along the entirety of the trench. The 5 s spin time lead to a fully filled trench, with the meniscus of the polymer nearly level with the top of the trench. Due to the shape of the trench this type of filling is actually not ideal as most of the optical absorption would occur where the metal contacts are furthest apart.

The reason for both the 30 s and 10 s spin times producing the same profile is believed to be due to the difference in the shape and size of the channels themselves. The trench used in the 30 s spin time is 0.53 μm at its thinnest and bows in on either side due to the oxidative stress discussed in chapter 6. The device spun for 10 s is wider, at 0.70 μm, and has straighter, more vertical sidewalls. Comparing the results of the two spins shows the sensitivity of the spinning process to the geometry of the device, as a difference of less than 200 nm can lead to widely varying polymer filling behavior. The width of the channel is fundamentally

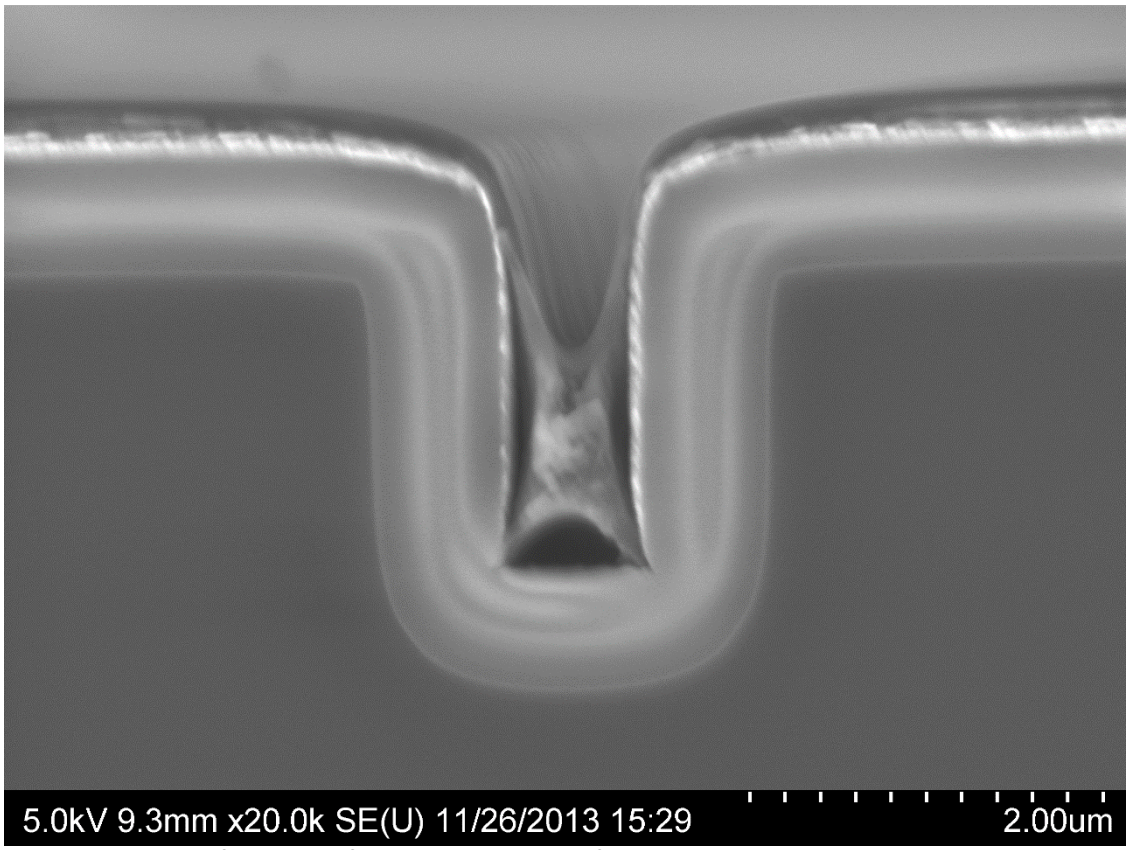


Fig 8.2 – Polymer fill test performed at 2000 rpm for 60 s

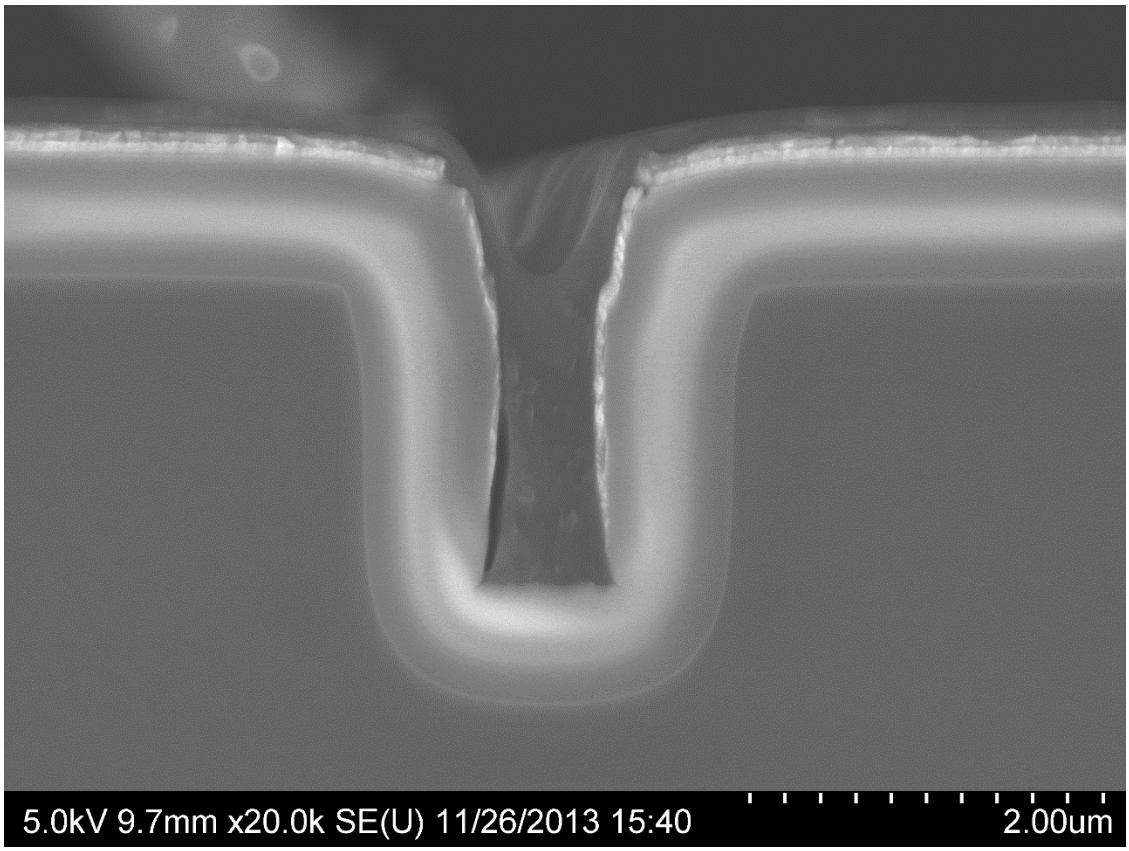


Fig 8.3 – Polymer fill test performed at 2000 rpm for 30 s

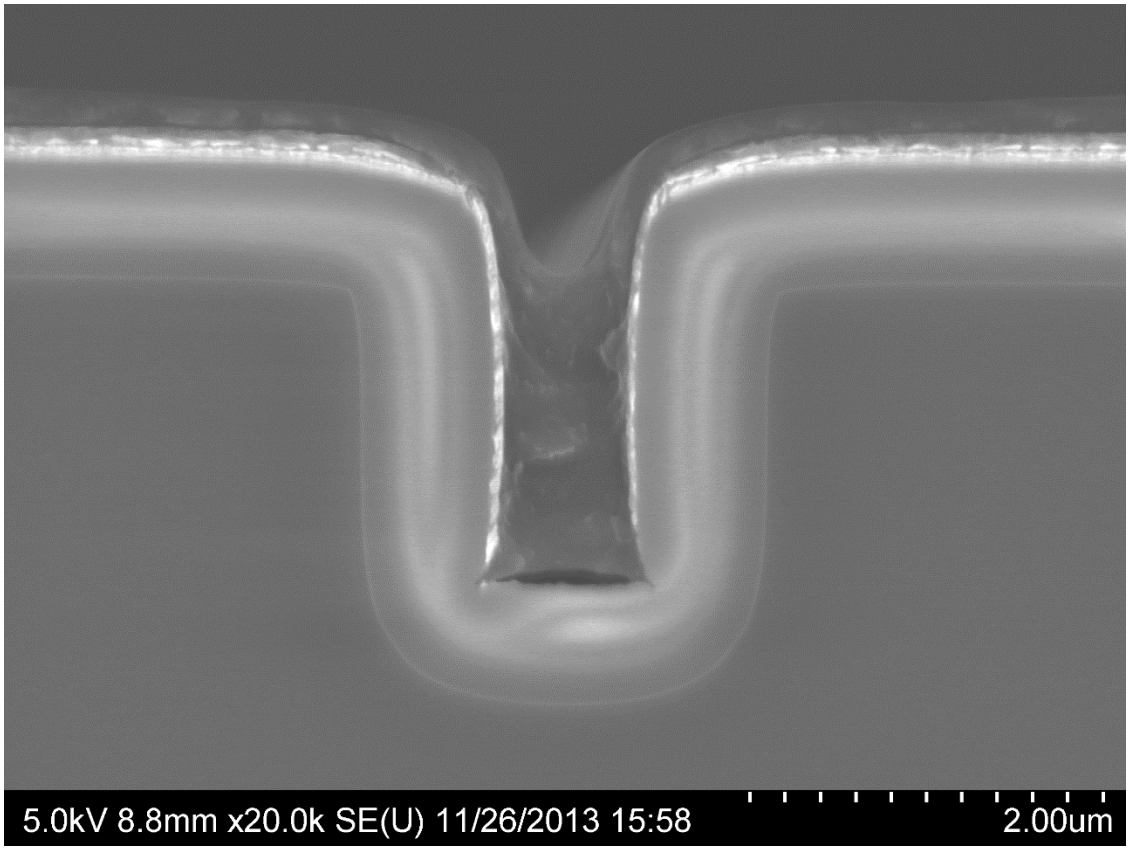


Fig 8.4 – Polymer fill test performed at 2000 rpm for 10 s

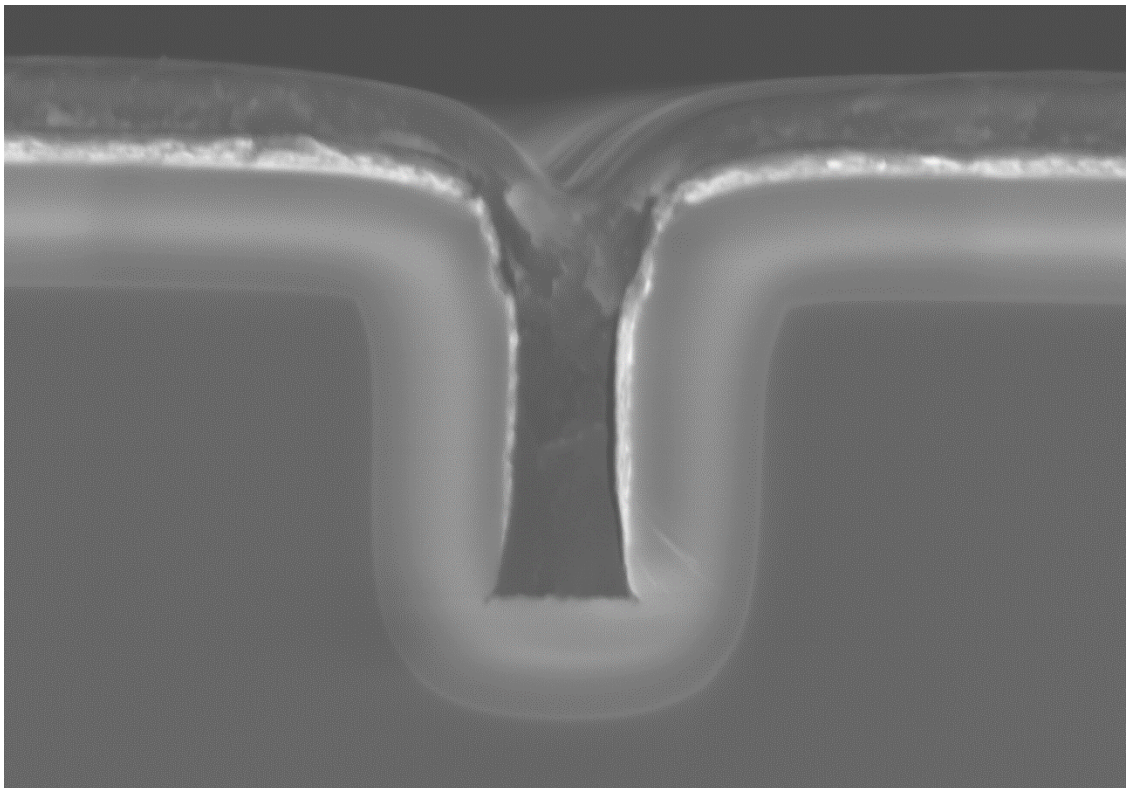


Fig 8.5 – Polymer fill test performed at 2000 rpm for 5 s

defined during the photolithography stage of the process, which has the most variability due to the manual resist development required in the University of Alberta nanoFAB. Due to this fact, the trench width can vary by ±100 nm after all trench processing is complete when comparing trenches across the wafer. Mixing this with the additional variability of batch-to-batch polymer variation (as the polymer mixing is the other manual step in processing) leads to the polymer trench filling process being difficult to optimize. There is simply no way of knowing the size of the trench before spinning to the required accuracy for high-yield polymer filling due to the large decrease in device yield and increased processing time that imaging would entail. Put simply, mounting each and every device to be spun on an SEM stub with silver paint, imaging it and then removing the device from the stub without damaging would slow down processing to an untenable degree. Not only that, but the stub removal process would likely have a low to medium yield itself, completely negating the benefits of the higher-yield polymer filling that would result. Because of these yield issues, it was decided to simply fill open circuit trenches with polymer using a standardized polymer filling process until a device showed good polymer filling due to the variation in trench sizes.

Since yield was such a large issue for the polymer filling process, it was also decided to spin the polymer at room temperature instead of heating the polymer to 75 ºC, as it would reduce the variability in the cooling of the polymer when spinning. To ensure wicking when spinning the spin rate was further increased to 3000 rpm and spin times of 3 s, 5 s, 7 s, and 15 s were tested. It was found that a 7s spin time at 3000 rpm offered a 80% fill rate in a 0.51 µm wide vertically walled trench, and therefore 7s spin time at 3000 rpm was chosen as the finalized polymer filling process.

8.3 Electrical Characterization

To characterize the filled devices two major pieces of equipment were used: an OAI TriSOL AAA 300 W solar simulator, and a Keithley 6482 dual channel picoammeter. The solar simulator was left on for a minimum of half an hour before testing to stabilize the light output. The power of the simulator was then adjusted to a level of 100 ± 2 mW/cm^2 to match the power output of the ASTM E927 standard using a standardized silicon cell. Once this was complete, the device under test (DUT) was held in place on an acrylic mount with copper clips. The clips firmly held down the DUT and also served as the electrical contacts to the device. The

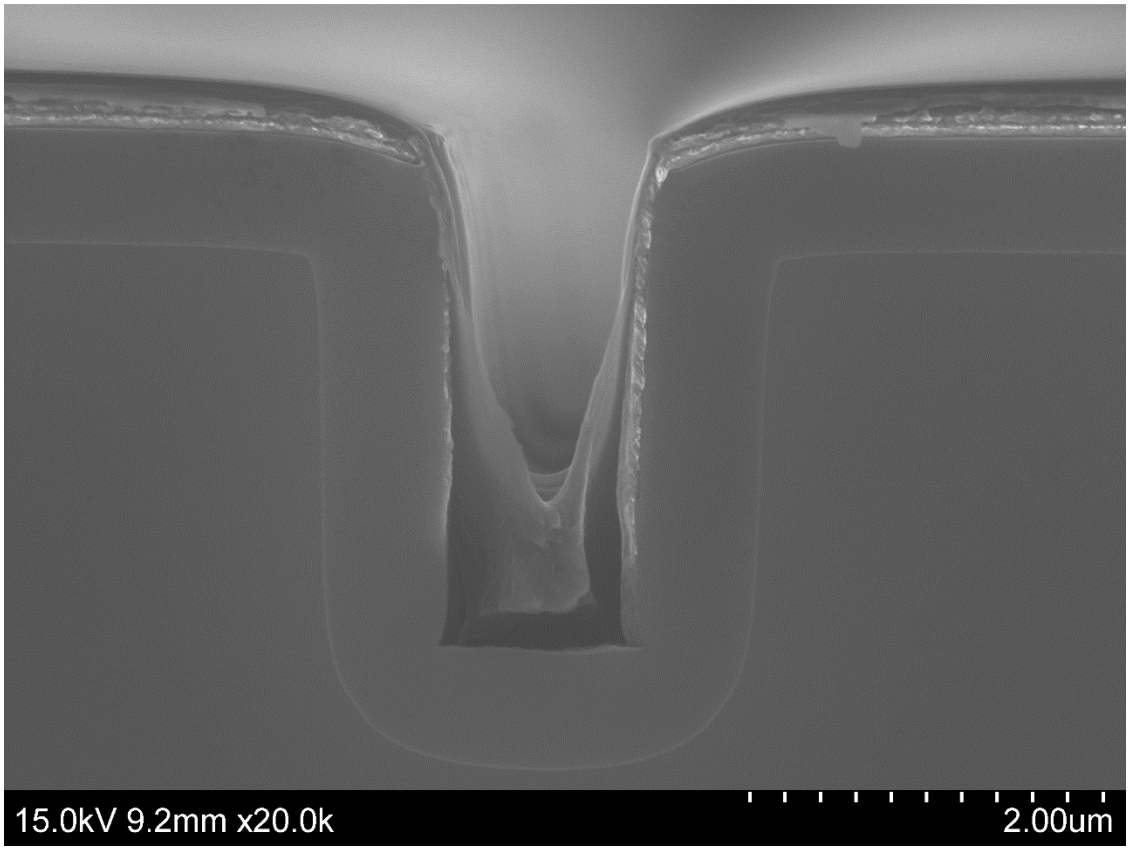


Fig 8.6 – Polymer filling seen in one of first devices tested

picoammeter was then connected to the clips and the acrylic mount was placed into the center of the solar simulator light output at the same height as the power meter to ensure the device was exposed to the proper power output. The devices were then swept from -0.6 V to 0.6 V in 0.05 V increments in both light and dark conditions and the resulting current was measured. This electrical characterization was done within a minimum of one hour after the devices were spun, to reduce the effect of oxygen-induced polymer aging.

The first round of devices tested had very poor filling, as seen in figure 8.6 and therefore had extremely poor electrical characteristics. The IV curve for the device shown in figure 8.6 can be seen in figure 8.7 and shows very little electrical power generation. The overall efficiency of the device was less than 0.05%, which is representative of the other devices tested in the first round. The current response in the low-fill device can be seen to be fairly symmetrical across the positive and negative voltages, particularly for the light curve. This is likely due to the lack of electron or hole blocking layers in the device, which would block charge carriers from being captured by the wrong contacts. The only pressure for carriers to move to one contact over

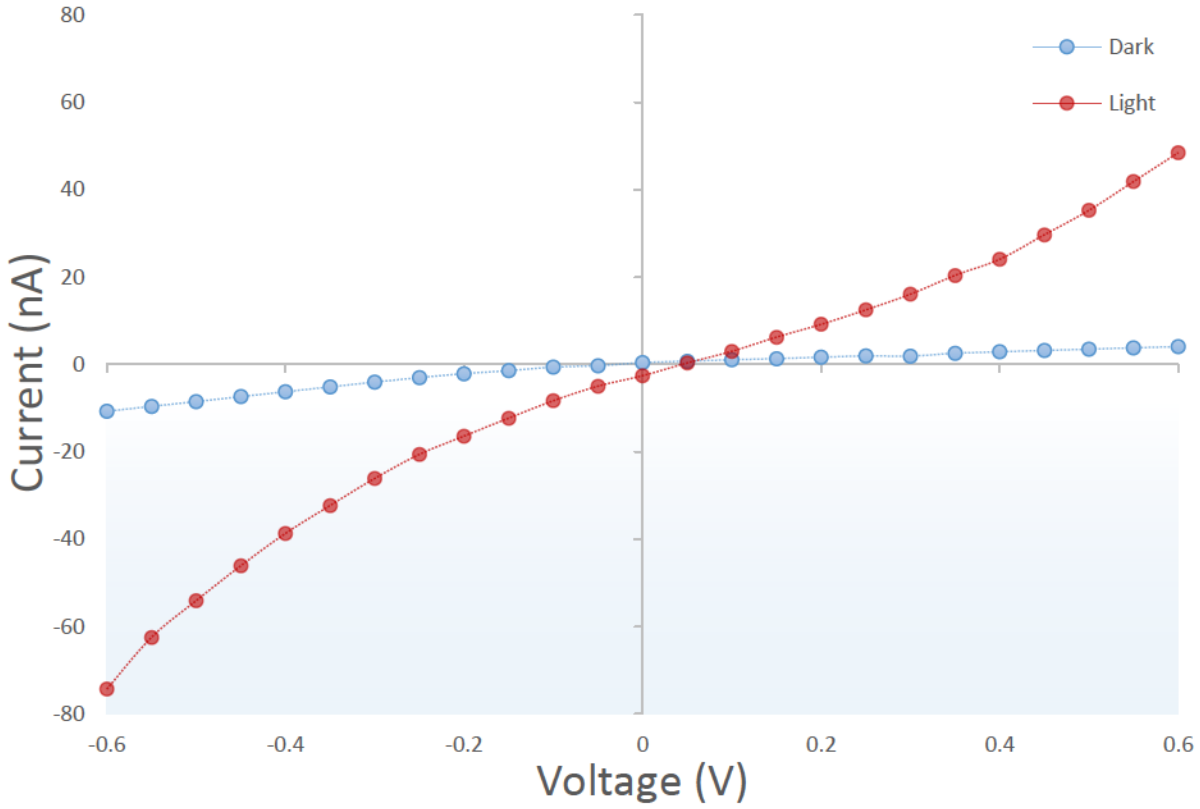


Fig 8.7 – IV curve of one of the initial devices. Very low I_{sc} and highly ohmic response can be seen.

another is the difference in the work functions between the two contacts. This difference in work function is enough to form diode like characteristics in the dark case, but under illumination the carriers are generated within the polymer itself, instead of being injected only from the contacts, leading to non-ideal ohmic behavior. This is discussed more in chapter 9, especially with regard to the band diagram explanation of carrier blocking layers.

The next round of devices tested were mostly similar to the ones in the first round in terms of their electrical response and their trench filling. One device however did have nearly perfect filling as seen in figure 8.8, with the only downside to the filling being that it is a fairly bumpy, non-uniform polymer surface. This device had a trench width of 1.0 μm, a trench depth of 2.80 μm and the metal contacts reached 2.15 μm down into the trench. The IV curve obtained from the device can be seen in figure 8.9 and shows the expected electrical response. The dark curve shows diode-like behavior indicating that the polymer mixture formed a semi-conducting system within the trench. The light curve shows a more ohmic response due to the lack of blocking layers, as explained above. The more ohmic response lead to a relatively poor fill factor

of 0.25 with the short circuit current at 52.7 nA and the open circuit voltage at 0.178 V. The length of the trench was measured with calipers and found to be 3.85 mm. Using these values the total device efficiency can be found using formula 1 introduced in chapter 2:

$$\eta = \frac{V_{OC} J_{sc} FF}{P}$$

$$\eta = \frac{0.178\,V * 52.7 * 10^{-9}\,A * 0.25}{0.1\frac{W}{cm^2} * 3.85 * 10^{-5}\,cm^2} * 100\%$$

$$\eta = 0.6\%$$

This efficiency, although quite low in an absolute sense, actually matches up very well to the model in chapter 3 when the fill factor of 0.25 and width of the trench is taken into account. The model shows for a 0.6 fill factor, a charge extraction distance of 1.0 μm, and an optical absorption distance of 2.2 μm the expected efficiency is 1.5%. If the model is re-calculated using

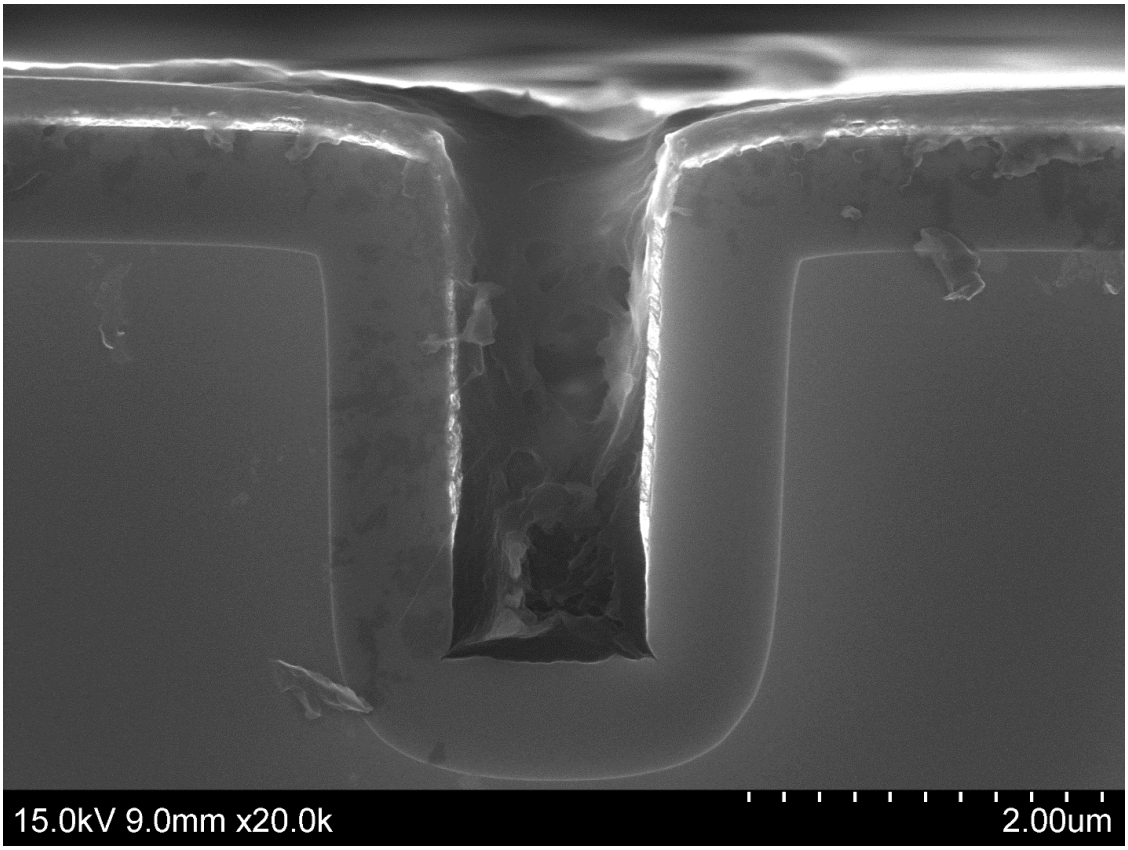


Fig 8.8 – Polymer filling seen in champion device

the actual fill factor of 0.25 the resulting expected efficiency is 0.63%, providing good agreement with experiment.

Note that this working device was 1 of approximately 50 devices fabricated during this research, and was chosen to be the endpoint of the work due to low yield and the time and difficulty required to reach this point. With the agreement of measured efficiency to predicted efficiency from the model of chapter 3, a preliminary proof of concept device has been demonstrated, and a preliminary validation of the model for long charge extraction distances has been provided. It is hopeful that this model will also be able to guide design for shorter charge extraction distances in future work. Methods to further test the model, as well as other future work are discussed in chapter 9.

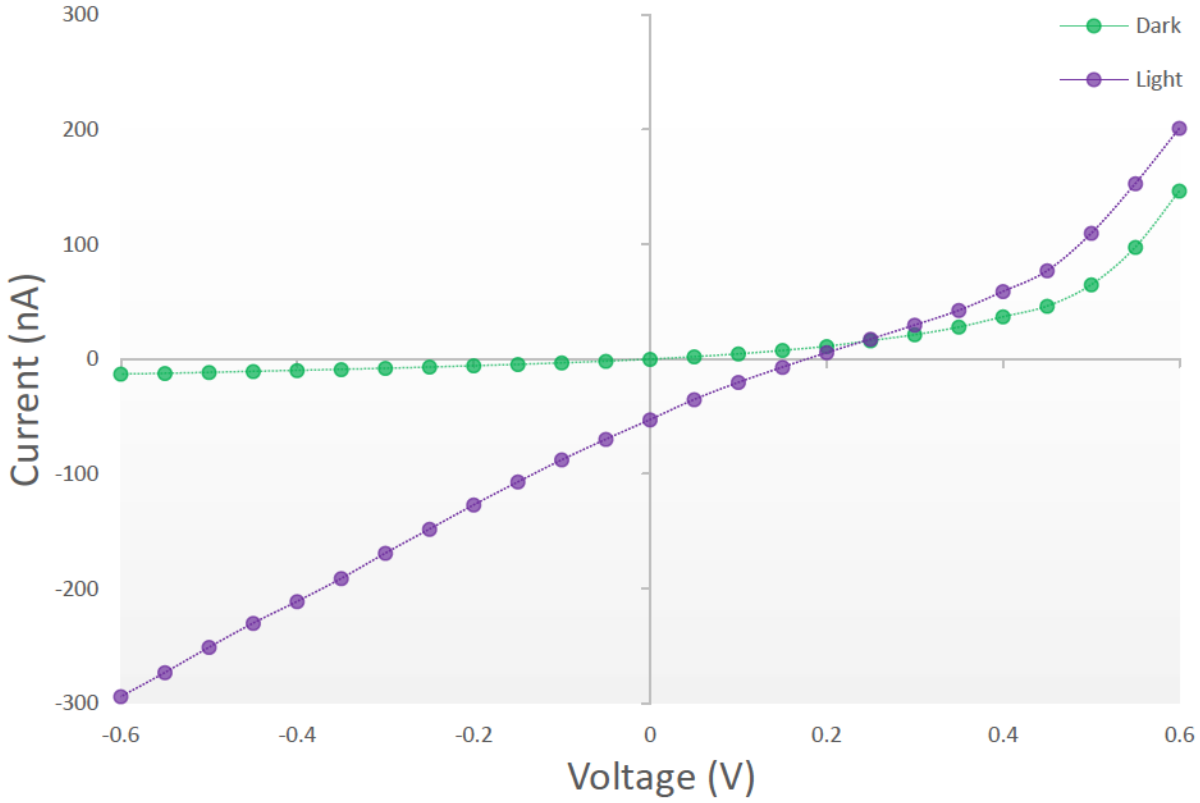


Fig 8.9– IV response of champion device. Higher diode like behavior, with ohmic response in the light curve

Chapter 9: Future Work and Conclusions

9.1 Further Process Optimization

Although the processing work that was done for this thesis did confirm the accuracy of the low aspect ratio part of the model, much more work could be done to further explore the concept of charge extraction and photon absorption decoupling. The first set of future work that could be attempted would be to explore the more extreme ends of the carrier collection and photon absorption decoupling model through further process optimization or using higher fidelity processing techniques. Specifically, carrier collection distances of 750 nm and below still need to be examined.

The most obvious constraint that was encountered in processing was the one micron limit of the photolithography used at the University of Alberta nanoFAB. Not only was the limit right on the edge of the model, necessitating the use of the heavy oxidation layer growth to decrease the trench width, the high error rate of the one micron photolithography over large distances made device formation at such sizes practically impossible. The high error rate was actually due to errors in the mask itself, requiring larger trench sizes and heavy oxidation just to get into the edge of the model range. Recently the nanoFAB has upgraded the Heidleberg pattern generator, which produces the chrome photomasks, to have a higher accuracy below two microns. A new mask could therefore be made using this upgraded equipment which may reduce the error rate enough that smaller trenches could be fabricated without changing any of the processes presented in this thesis. Another plan of attack would be to simply use another facility's lithographic capabilities to generate smaller width lines, likely using a non-contact photolithographical technique, such as a stepper system or interference lithography [69,70]. Using these methods would likely allow exploration of carrier collection distances on the order of 500 nm.

A low-throughput method that could be used to test the model very thoroughly would be to use electron beam (e-beam) lithography to generate the trench lines, as this method can easily

create linewidths below 50 nm in size [71]. Since e-beam lithography is a direct write method, each exposure can take many hours [71], which limits the amount of devices that can be produced. Therefore, this method would likely be useful for examining carrier collection distances on the order of 100 nm, as wider trenches would likely take many hours, possibly even days, to write, which could allow beam drift to become a significant issue [71].

The other processing step that had large consistency issues was the polymer spinning process. The consistency of this processing step was hindered mainly from the variation in trench sizes, which can be solved using the methods mentioned above, and from issues in centering the small 3 mm by 10 mm devices onto the chuck of the spinner. One way this issue could be solved would be to run the whole wafer through all processing steps. The current process involves breaking up the wafer into the different sized trench widths before depositing the metal layers, as the different trench widths can require extremely different deposition angles. A new mask could be made with all the same trench widths across the wafer and varying the trench widths could be controlled by varying the oxidation time. Therefore the whole wafer could be metal deposited at the same time, increasing throughput as well as enabling the entire wafer to be spun with polymer. The full size wafer would be much easier to center before spinning, improving the consistency of this processing step. The wafer would then be cleaved into small pieces after spinning to be electrically characterized.

Another way of solving the polymer deposition issue would be to spray on the polymer instead of spinning it, removing the centering issues altogether. This process itself would have to be optimized, but the possible gains in consistency are well worth further exploration. Spray coating also lends itself to mass production, and so development of this processing step could enable manufacture of cells in the future.

9.2 Additional Processing Steps

There are two additional processing steps that are consistently done to standard P3HT:PCBM cells to increase their efficiency that could be added to this process flow [72,73]. The first additional step would be to anneal the polymer mixture after drying at temperatures of 120ºC or higher for a small period of time (approximately a half an hour or less) [72]. This annealing process increases the crystallinity and ordering of the P3HT which increases the hole

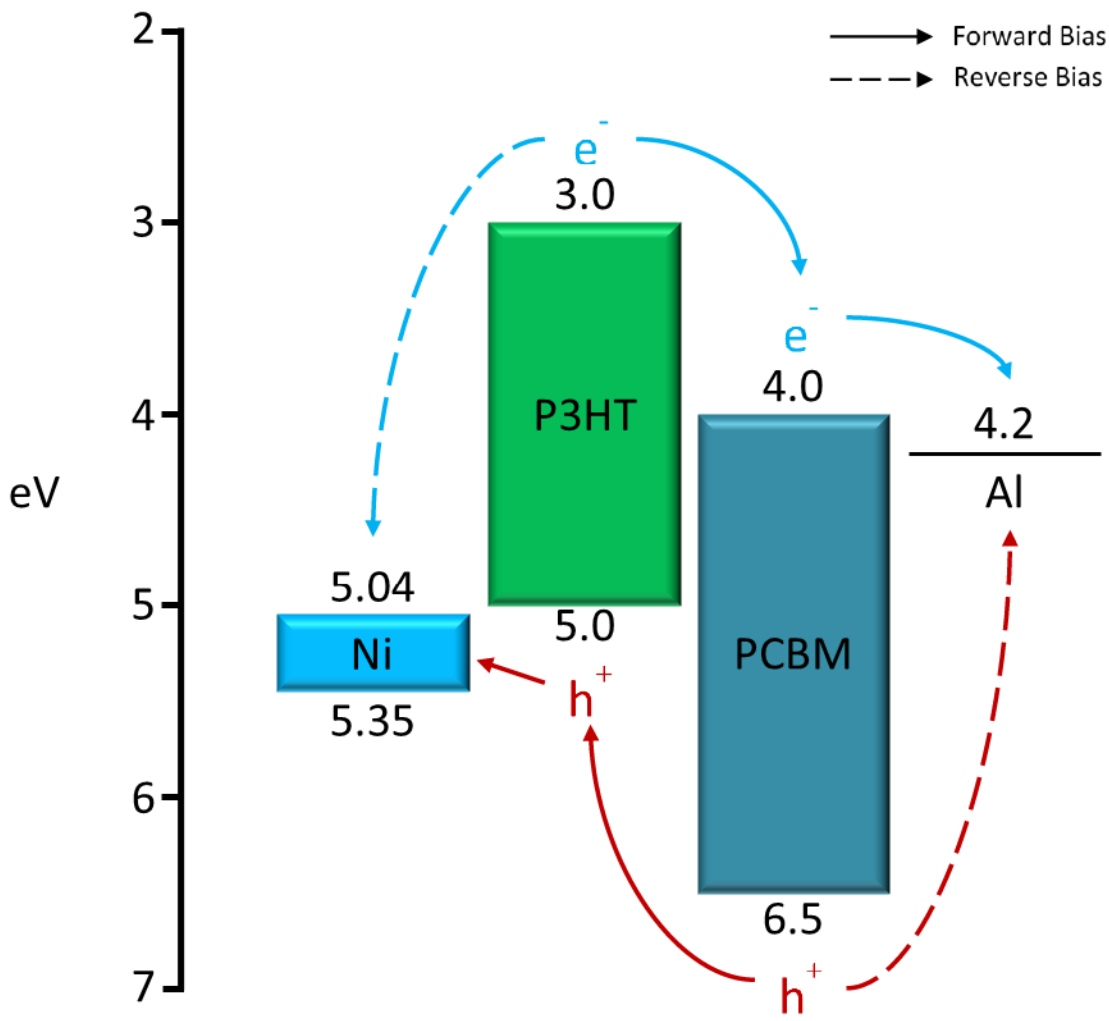


Fig 9.1 – Band diagram of device showing conduction path in forward and reverse bias

mobility in the polymer blend [72]. This increased mobility obviously helps to increase the efficiency of the device as more carriers are collected the higher their mobility.

The second additional step that would help to increase the efficiency of the device would be to add an electron or hole blocking layer over one of the contacts as mentioned in chapter 8. Without an electron or hole blocking layer electrons and holes are energetically driven towards the wrong contacts when the device is under reverse bias, as can be seen in the band diagram figure 9.1. The conduction path in the reverse bias case is completed by the excess holes in P3HT and the excess electrons in the PCBM recombining. Since this reverse pathway exists the device responds quite ohmically in reverse bias as discussed in the previous chapter, which greatly lowers the fill factor of the device. A carrier blocking layer stops either electrons or holes

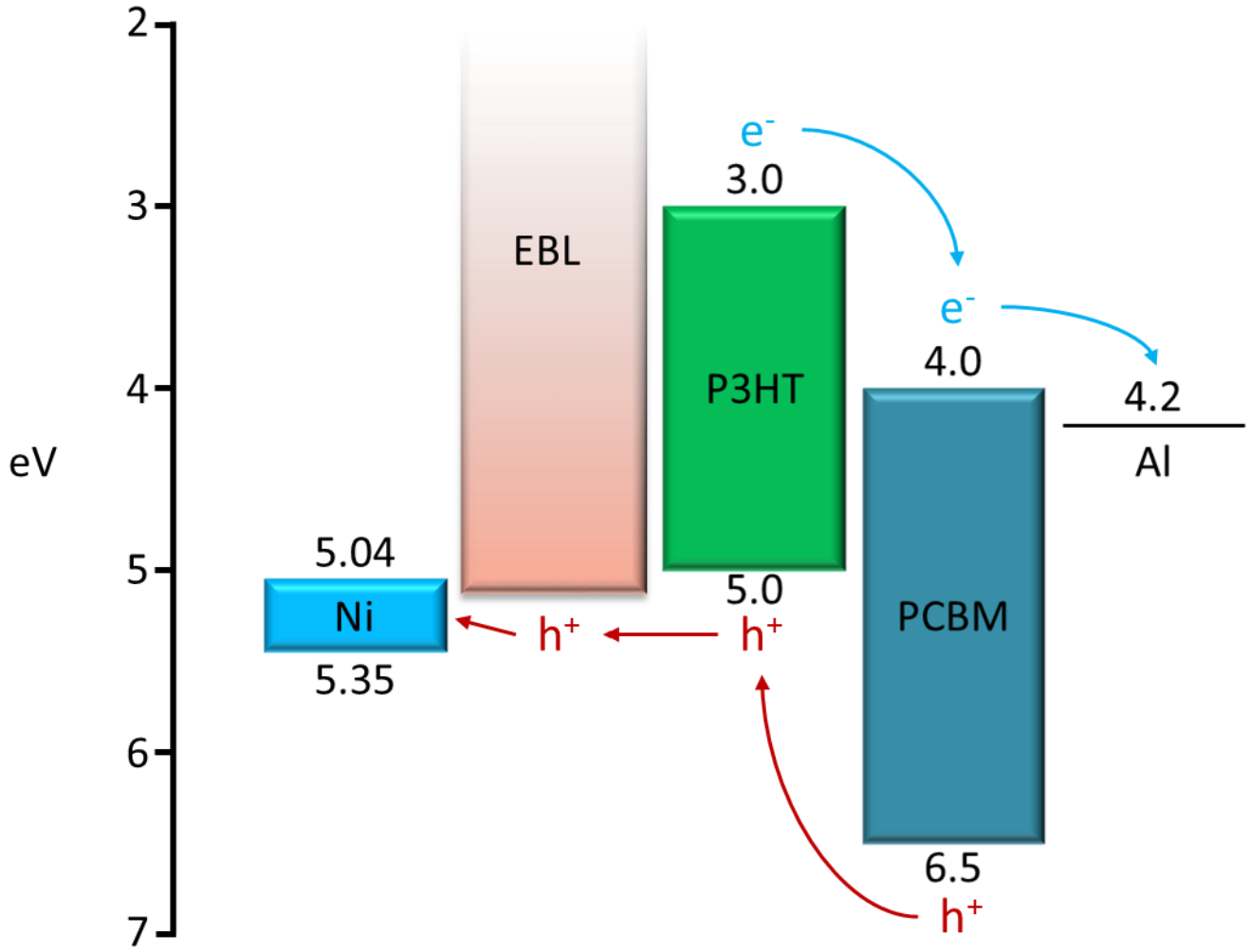


Fig 9.2 – Hypothetical band diagram of our device with electron blocking layer added

from energetically favoring the transition to the wrong contact by creating a large energy barrier and therefore blocks off the reverse bias conduction pathway. This can be seen in figure 9.2 with the addition of an electron blocking layer to the band structure.

The most commonly used carrier blocking layer in the P3HT:PCBM polymer system is PEDOT:PSS, a polymer electron blocking layer [73]. The problem with using a polymer for a blocking layer in this device architecture is that there is no easy way of depositing a polymer onto only one of the contacts since polymers are typically deposited by spin-on or spray-on techniques. Therefore to add a blocking layer requires the source material to be e-beam evaporated just like the metal contacts. Luckily there are many possible materials that fit this criteria, such as WO_3, NiO, Nb_2O_5, and ZnO [73]. The most promising of such materials is likely

NiO which is an electron blocking layer. The way NiO could be added would be to slow down the deposition of Ni and add a small amount of oxygen to the deposition environment to create a NiO film over top of the Ni film. This allows for a single deposition step to deposit both the hole contact as well as the electron blocking layer.

9.3 Parallelization of Structure

Once the model has been more thoroughly tested and if it continues to show promising results, the exploration of large area device can be performed. Scaling up in area is not a trivial problem to solve and it will need an entirely new process flow to achieve. The main issue with scaling up the area is that vertical contacts will inherently take up area that would be used for absorbing material. This requires that the scaffolding that holds up the contacts should be as thin as possible. There are a huge variety of possible process flows that could solve this issue. Two possible solutions to the area scale up problem are presented in process flows seen in figure 9.3 and 9.4. The first solution involves using the polymer itself as the scaffolding to have the lowest possible efficiency losses due to contact area. This process flow involves depositing the polymer absorbing layer first, followed by a nanoimprinting step, which would need to be optimized very heavily to find out if it is a feasible step to perform. The next steps involve depositing thin layers of metal onto the polymer and then removing the excess metals deposited on the top of the polymer layer through angled ion milling. The ion milling is another step would need to be thoroughly investigated to determine its feasibility. Redeposition of metal onto the device once it has been milled is a likely issue with this step. Subsequently, another layer of the absorbing polymer layer would be deposited followed likely by an encapsulation step.

The second process flow that could create a wide-area device involves making interdigitated cylindrical electrodes through a series of metal deposition and the use of a sacrificial layer, as seen in figure 9.4. This process flow would lead to more area loss due to larger area contacts but would likely be far more robust. The first step involves depositing a thick sacrificial layer, likely made up of silicon dioxide. From there cylindrical holes could be etched into the sacrificial layer and metal deposited into them, likely through an initial atomic layer deposition step followed by an electroplating step. Another set of holes would then be etched through the first metal and into the sacrificial layer. An insulating layer would then be deposited at an angle to prevent the next metal deposition from contacting the first one, while

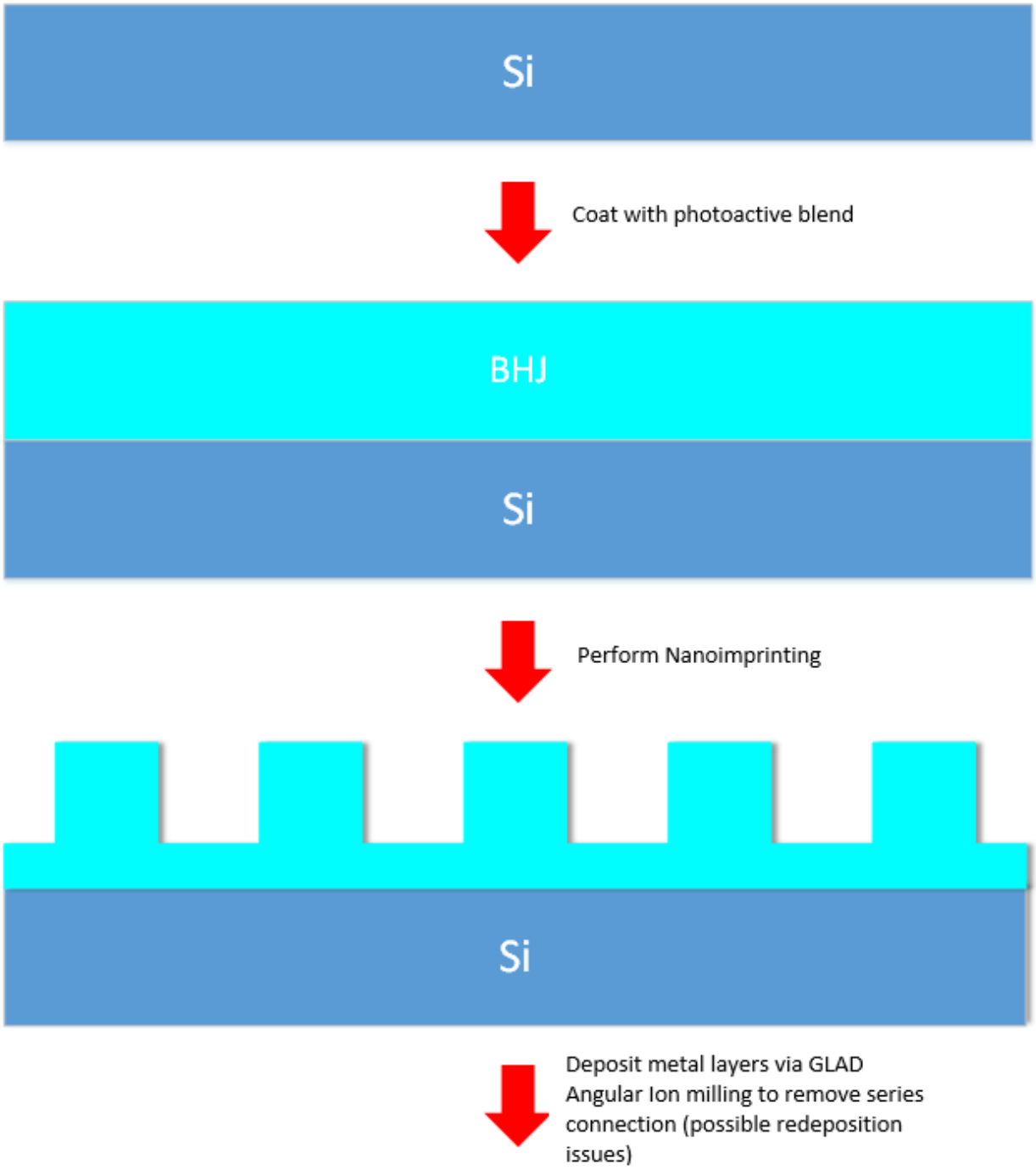


Fig 9.3a) – Formation of trenches in polymer system through nanoimprinting

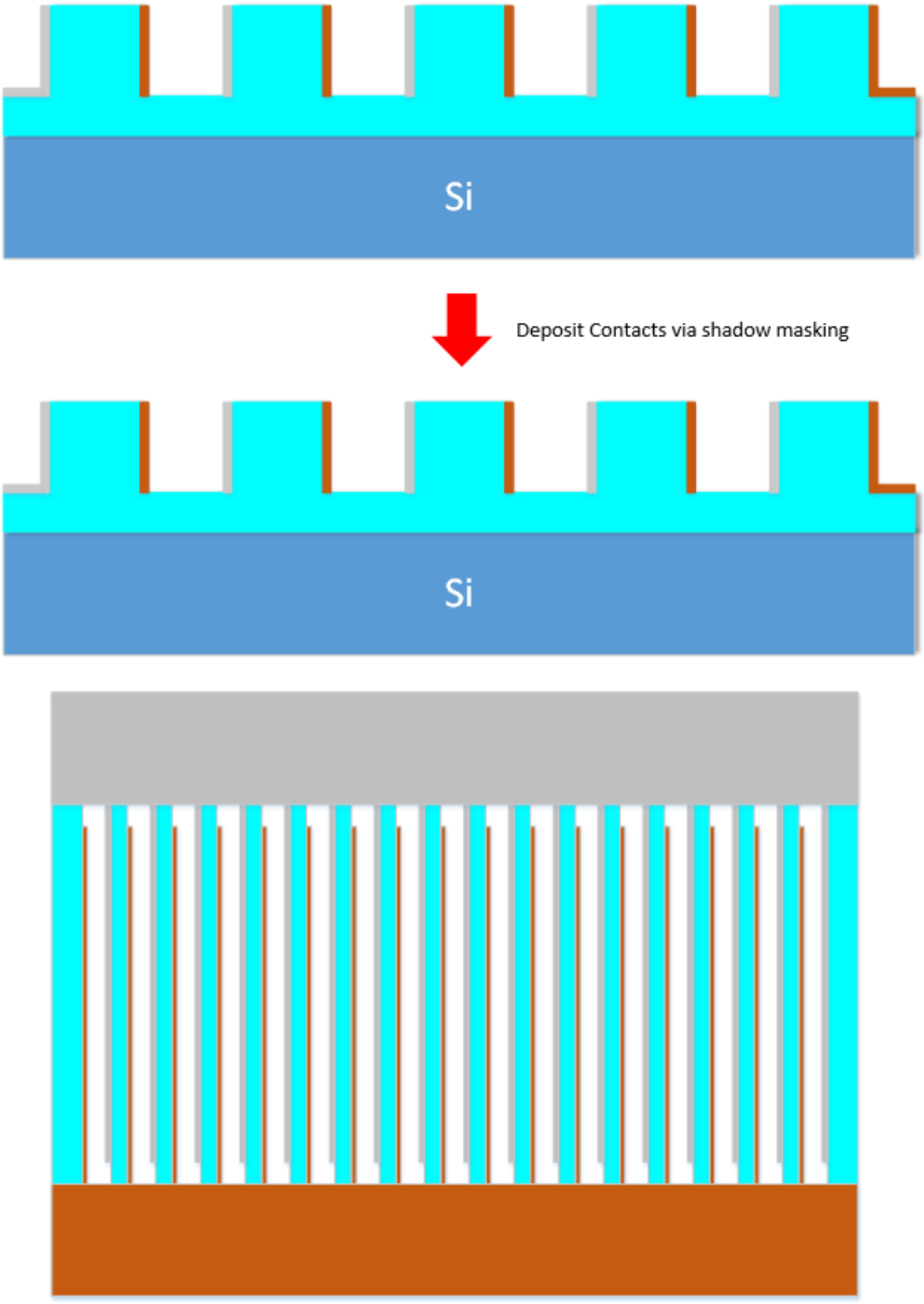


Fig 9.3b) – Depositing of metal contacts onto imprinted polymer system

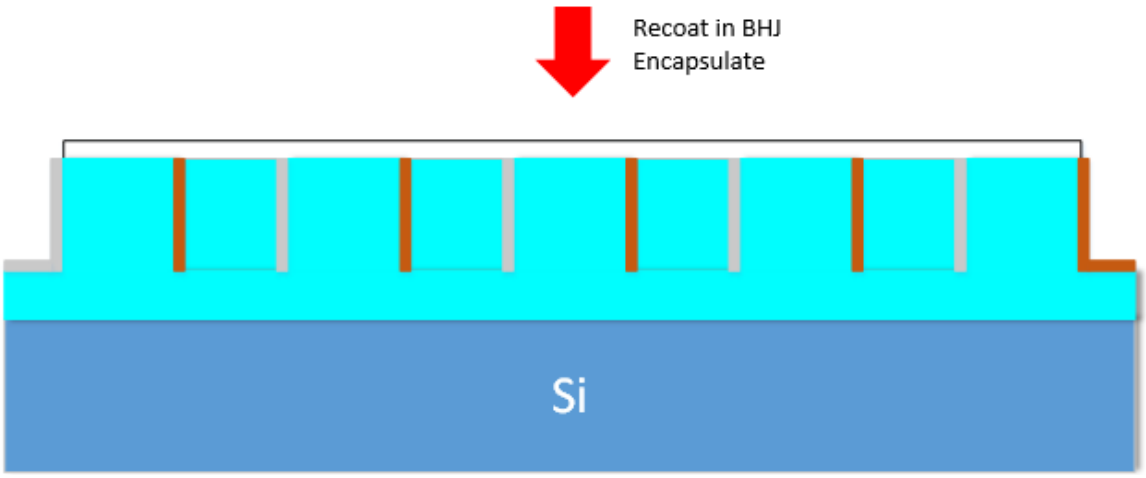


Fig 9.3c) – recoating in bulk hetero junction and encapsulating

simultaneously not clogging the holes. The second metal would then be deposited and a wafer bonding procedure would bond the second metal to a new substrate. The sacrificial layer could then be released to expose the electrodes and then filled with the polymer absorbing layer and encapsulated.

9.4 Final Remarks

The hypothesis that decoupling charge extraction from carrier collection in organic photovoltaics still needs to be explored further. The model developed for this thesis work shows the possibility of large efficiency gains through high aspect ratio structures with a small carrier collection distance. A series of prototype devices were fabricated using silicon microstructuring techniques. Each fabrication process to create the devices were optimized to the best of the author's ability. Issues with the photolithography step resulted in minimum device widths of one micron. Similarly, problems with the polymer spinning process resulted in the proper filling of only the 2.5 μm deep trench. The efficiency of the prototype device matched up very well with the model, although it had a low fill factor and efficiency due to the lack of carrier blocking layers and the large dimensions of the device. More work could be performed to fully test the smaller carrier collection distances of the model.

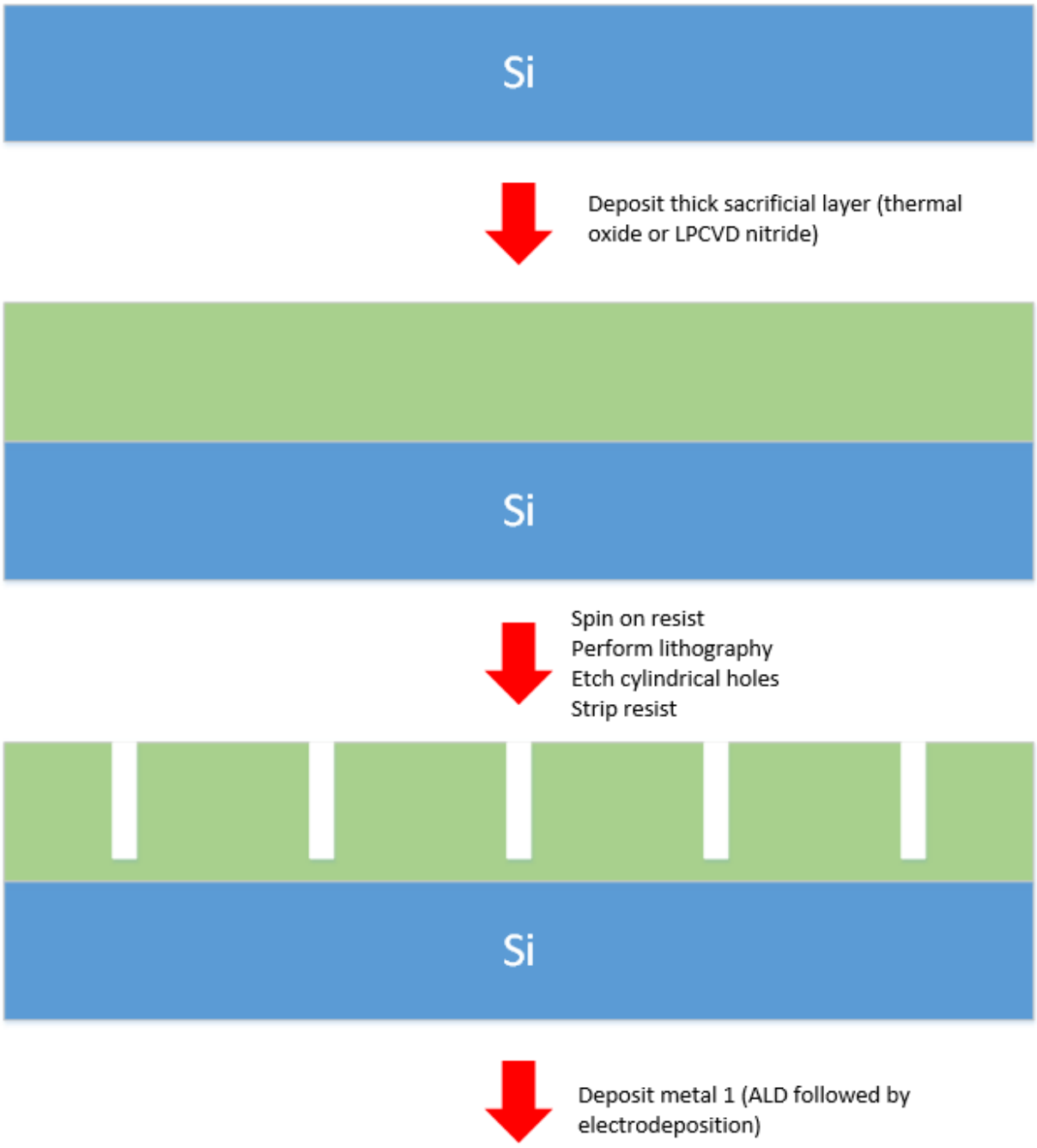


Fig 9.4a) – Forming cylindrical holes in sacrificial layer

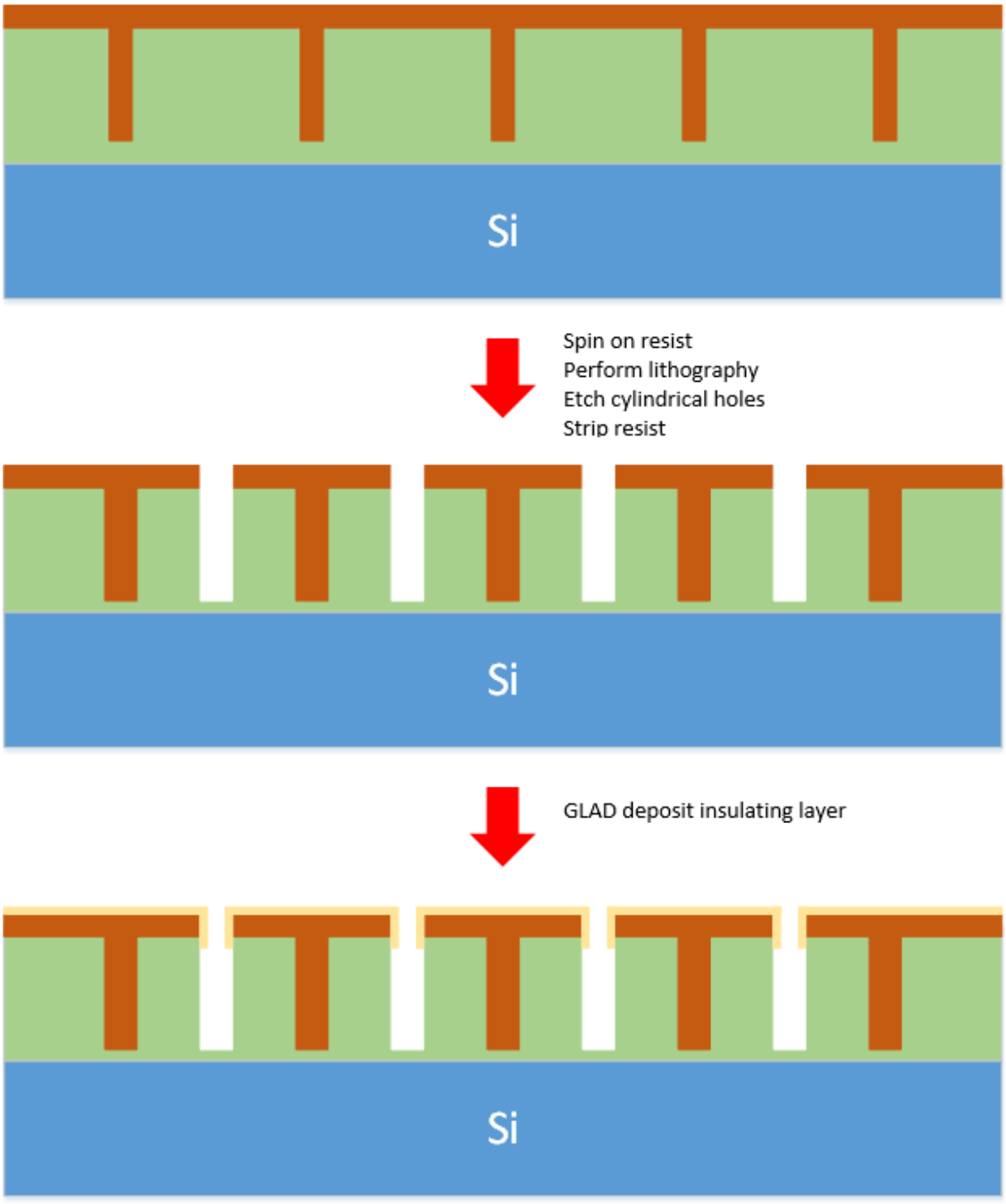


Fig 9.4b) – Depositing metal and etching a new set of cylindrical holes. Insulating layer deposited to ensure no shorting between contacts.

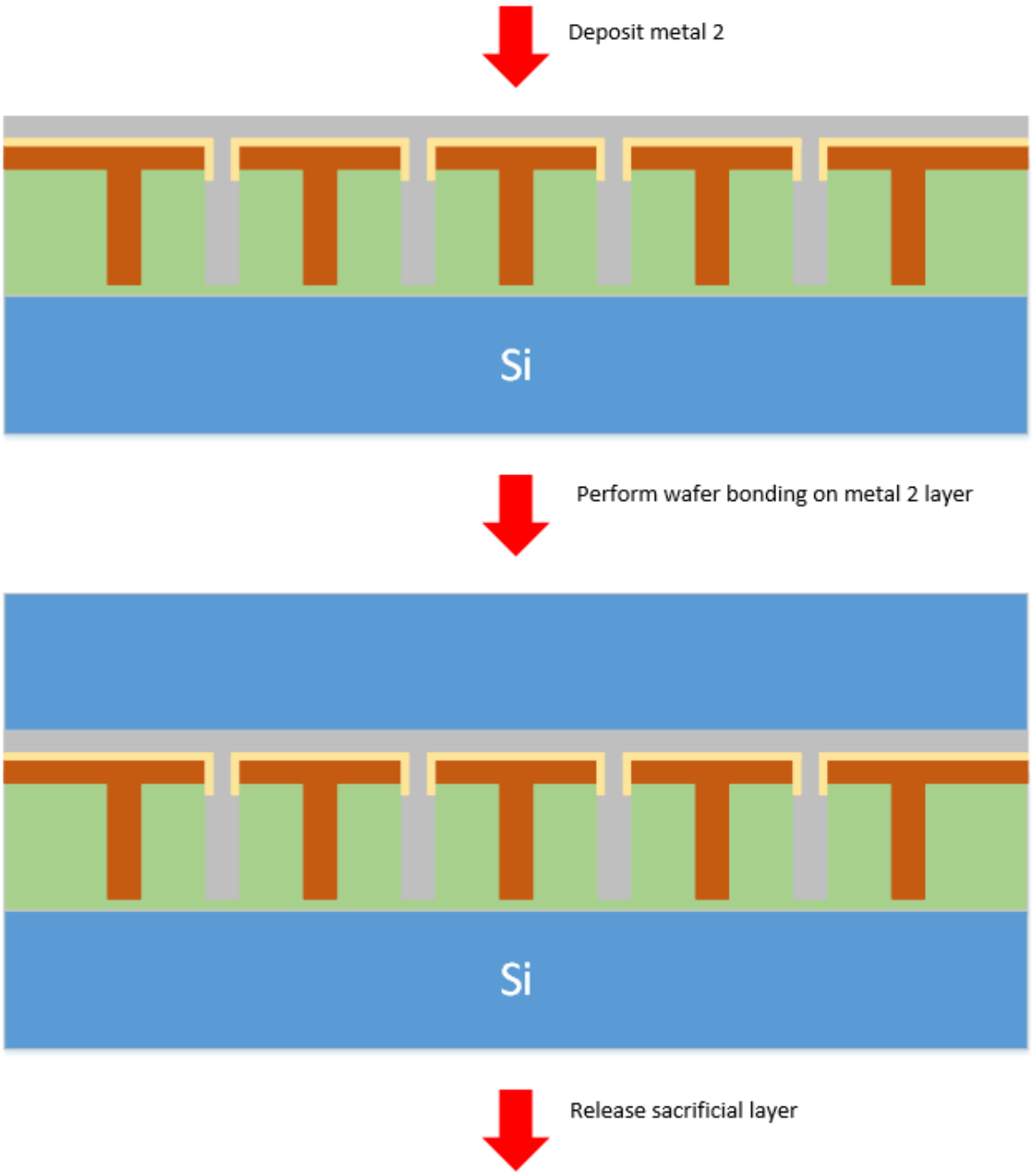


Fig 9.4c) – Depositing second metal layer and wafer bonding.

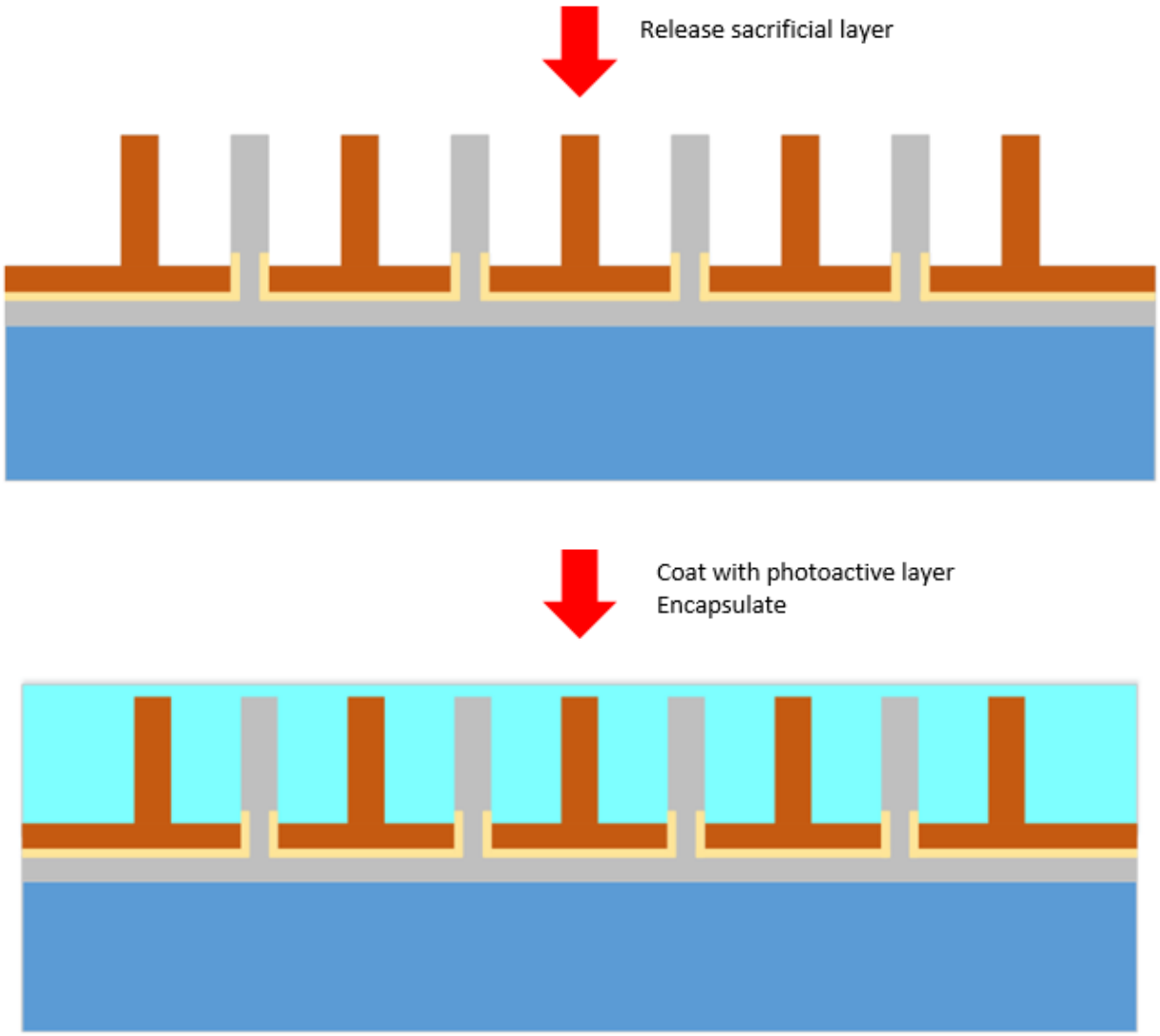


Fig 9.4d) – Release of sacrificial layer and coating with polymer system. Finally, device is encapsulated

References

[1] United States Environmental Protection Agency. *Greenhouse Gas Emissions*, [Online]. Available: http://www.epa.gov/climatechange/ghgemissions/gases/co2.html

[2] Hybrid Cars, *Electric,* [Online]. Available: http://www.hybridcars.com/electric-car

[3] World Wind Energy Report 2013. (2014, Apr 8). *WWEC2014: Key Statistics of World Wind Energy Report Published* [Online]. Available: http://www.wwindea.org/wwec2014-key-statistics-of-world-wind-energy-report-published/

[4] The Shift Project. (2014). *Breakdown of Energy Generation by Sourc,* [Online]. Available: http://www.tsp-data-portal.org/Breakdown-of-Electricity-Generation-by-Energy-Source#tspQvChart

[5] U.S. Energy Information Administration, *Levelized Cost of New Generation Resources in the Annual Energy Outlook 2012*, [Online]. Available: http://www.eia.gov/forecasts/aeo/electricity_generation.cfm

[6] A. Sharma *et al.,* "Top Solar Power Industry Trends for 2015," IHS, Douglas County, CO, 2015

[7] G. Carr. (2012, Nov 21). *Sunny Uplands* [Online]. Available: http://www.economist.com/news/21566414-alternative-energy-will-no-longer-be-alternative-sunny-uplands

[8] R. Frischknecht, *et al.*, "Life cycle assessment of future photovoltaic electricity production from residential-scale systems operated in Europe", Subtask 2.0 "LCA", IEA-PVPS Task 12, 2014

[9] S. Mufson. (2013, July 23). *Chinese tariffs may hurt U.S. makers of solar cells' raw material* [Online]. Available: http://www.washingtonpost.com/business/economy/chinese-tariffs-may-hurt-us-makers-of-solar-cells-raw-material/2013/07/23/01ac60a4-f3d9-11e2-aa2e-4088616498b4_story.html

[10] Green Rhino Energy. (2013). *PV Manufacturing* [Online]. Available: http://www.greenrhinoenergy.com/solar/technologies/pv_manufacturing.php

[11] J. Britt and C. Ferekides, "Thin-film CdS/CdTe solar cell with 15.8% efficiency," *Appl. Phys. Lett*, vol. 63*,* no. 22*,* pp. 2851-2852*,* May 1993

[12] M. Liu, *et al.*, "Efficient planar heterojunction perovkite solar cells by vapour deposition," *Nat. Let.*, vol. 501*,* pp. 395-398*,* Sept. 2013

[13] M. Hiramoto *et al.,* "Three -layered organic solar cell with a photoactive interlayer of codeposited pigments," *Appl. Phys. Lett,* vol. 58, no. 10, pp. 1062-1064, Mar. 1991

[14] A.M. Bagher, "Comparison of organic solar cells and inorganic solar cells," *Int. J. of Ren. Sus. Energy,* vol. 3, no. 3, pp. 53-58, May 2014

[15] R. Sondergaard, *et al.,* "Roll-to-roll fabrication of polymer solar cells," *Mat. Today,* vol. 14, no. 1-2, pp. 36-49, Feb. 2012

[16] F.C. Krebs, "Fabrication and processing of polymer solar cells: A review of printing and coating techniques," *Sol. Ener. Mat. Sol. Cells,* vol. 93, no. 4, pp. 394-412, Apr. 2009

[17] M. Pagliaro, *et al.*, "Flexible Solar Cells," *ChemSusChem,* vol. 1, no. 11, pp. 880-891, Nov. 2008

[18] A. Hellemans. (2014, Oct 17). *Can Organic Solar Cells Reach Old Age?* [Online]. Available: http://spectrum.ieee.org/energywise/green-tech/solar/can-organic-solar-cells-reach-old-age1

[19] K. Norrman, *et al.,* "Lifetimes of organic photovoltaics: Combining chemical and physical characterisation techniques to study degradation mechanisms," *Sol. Ener. Mat. Sol. Cells,* vol. 90, no. 17, pp. 2793-2814, Nov. 2006

[20] A. Rivaton, *et al.,* "Light-induced degradation of the active layer of polymer-based solar cells," *Pol. Deg. Stab.,* vol. 95, no. 3, pp. 278-284, Mar. 2010

[21] Heliatek. (2013, Jan 16). *Heliatek consolidates its technology leadership by establishing a new world record for organic solar technology with a cell efficiency of 12%* [Online]. Available: http://www.heliatek.com/en/press/press-releases/details/heliatek-consolidates-its-technology-leadership-by-establishing-a-new-world-record-for-organic-solar-technology-with-a-cell-effi

[22] Panasonic. (2014, Apr 10). *Panasonic HIT® Solar Cell Achieves World's Highest Energy Conversion Efficiency of 25.6%*2 at Research Level* [Online]. Available: http://news.panasonic.com/press/news/official.data/data.dir/2014/04/en140410-4/en140410-4.html

[23] I. Etxebarria, *et al.*, "Solution-processable polymeric solar cells: A review on materials, strategies and ecell architecture to overcome 10%," *Org. Elec.*, vol. 19, pp. 34-60, Apr. 2015

[24] M. Glatthaar, *et al.*, "Organic solar cells using inverted layer sequence," *Thin Solid Films,* vol. 491, no. 1-2, pp. 298-300, Nov. 2005

[25] G. Garcia-Belmonte, *et al.*, "Simultaneous determination of carrier lifetime and electron density-of-states in P3HT:PCBM organic solar cells under illumination by impedance spectroscopy," *Sol. Ener. Mat. Sol. Cells,* vol. 94, no. 2, pp. 366-375, Feb. 2010

[26] *SOLAR CELLS – From Basics to Advanced Systems*, McGraw-Hill Book Co., New York, NY, 1983, pp. 6

[27] *SOLAR CELLS – From Basics to Advanced Systems*, McGraw-Hill Book Co., New York, NY, 1983, pp. 7

[28] M.A. Green, "Solar cell fill factors: general graph and empirical expressions," *Solid-State Elec.*, vol. 24, no. 8, pp. 788-789, Aug. 1981

[29] U.S. Department of Energy. (2013, Aug 20). *Photovoltaic Cell Quantum Efficiency Basics* [Online]. Available: http://energy.gov/eere/energybasics/articles/photovoltaic-cell-quantum-efficiency-basics

[30] R. W. Miles, *et al.*, "Inorganic photovoltaic cells," *Mat. Today*, vol. 10, no. 11, pp. 20-27, Nov. 2007

[31] *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, Upper Saddle River, NJ, 2010, pp. 5-8

[32] *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, Upper Saddle River, NJ, 2010, pp. 117-124
[33] *SOLAR CELLS – From Basics to Advanced Systems*, McGraw-Hill Book Co., New York, NY, 1983, pp. 40-67
[34] K. Yasuda, *et al.*, "Production of Solar-grade Silicon by Halidothermic Reduction of Silicon Tetrachloride," *Met. Mat. Trans. B*, vol. 42, no. 1, pp. 37-49
[35] H. Wang, *et al.*, "Exciton diffusion and charge transfer dynamics in nano phase-separated P3HT/PCBM blend films," *Nanoscale*, vol. 3, pp. 2280-2285, Mar. 2011
[36] H. Hoppe and N.S. Sariciftci, "Organic solar cells: An overview," *J. Mat. Res.*, vol. 19. no. 7, pp. 1924-1945, Mar. 2011
[37] P. Peumans, *et al.*, "Small molecular weight organic thin-film photodetectors and solar cells," *J. Appl. Phys.*, vol. 93, pp 3693, Mar. 2003
[38] D.R. Kozub, *et al.,* "Direct measurements of exciton diffusion length limitations on organic solar cell performance," *Chem. Commun.*, vol. 48, pp. 5859-5861, Apr. 2012
[39] G. Garcia-Belmonte, *et al.*, "Charge carrier mobility and lifetime of organic bulk heterojunctions analyzed by impedance spectroscopy," *Org. Elec.*, vol. 9, no. 5, pp. 847-851, Oct. 2008
[40] M. Niggemann, *et al.,* "Realization of ultrahigh photovoltages with organic photovoltaic nanomodules," *Adv. Mat.,* vol. 20, no. 21, pp. 4055-4060, Nov. 2008
[41] M. Niggemann, "Fundamental investigations on periodic nano- and microstructured organic solar cells, Ph.D. dissertation, Albert-Ludwigs-Universitaet Freiburg im Breisgau, Germany, 2005
[42] S. Günes, *et al.*, "Conjugated polymer-based organic solar cells," *Chem. Rev.,* vol. 107, no. 4, pp. 1324-1338, Apr. 2007
[43] M. Padilla, *et al.,* "Short-circuit current density mapping for solar cells," *Sol. En. Mat. Sol. Cells,* vol. 120, pp. 282-288, Oct. 2013
[44] G. Dennler, *et al.,* "Flexible, conjugated polymer-fullerene-based bulk-heterojunction solar cells: Basics, encapsulation, and integration," *J. Mater. Res.,* vol. 20, no. 12. Dec. 2005
[45] J. Du, *et al.,* "Reflectivity and absorption of a borosilicate glass during ^{60}Co-γ irradiation calculated from data measured by an integrating sphere," *Rad. Eff. Def. in Sol.*, vol. 167, no. 1, Aug. 2011
[46] S. Lee, *et al.,* "Organic solar cells with submicron-thick polymer:fullerene bulk heterojunction films," *App. Phys. Let.,* vol. 97, no. 10, pp. 103503, Sept. 2010
[47] G. Dennler, *et al.,* "Polymer-fullerene bulk-heterojunction solar cells," *Adv. Mat.,* vol. 21, no. 13, pp. 1323-1338, Apr. 2009
[48] S.S. van Bavel, *et al.,* "P3HT/PCBM Bulk Heterojunction Solar Cells: Impact of Blend Composition and 3D Morphology on Device Performance," *Adv. Fun. Mat.,* vol. 20, no. 9, pp. 1458-1463, May 2010
[49] *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, Upper Saddle River, NJ, 2010, pp. 59-84

[50] R. N. Noyce, "Semiconductor circuit complex having isolation means," U.S. Patent 3150299, Sept. 22, 1964
[51] *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, Upper Saddle River, NJ, 2010, pp. 133-137
[52] K. Robbie and M.J. Brett, "Sculptured thin films and glancing angle deposition: Growth mechanics and applications," *J. Vac. Sci. Technol.,* vol. 15, no. 3, pp. 1460-1465, Mar. 1997
[53] D.B. Hall, *et al.,* "Spin coating of thin and ultrathin polymer films," *Pol. Eng. and Sci.,* vol. 38, no. 12, pp. 2039-2045, Dec. 1998
[54] Microchemicals (2013, Nov 7), *Baking Steps in Photoresist Processing,* [Online]. Available: www.microchemicals.eu/technical_information/photoresist_baking.pdf
[55] K.R. Williams, *et al.,* "Etch rates for micromachining processing-part II," *J. of Microelectromech. Sys.,* vol. 12, no. 6, pp. 761-778, Dec. 2013
[56] J.K. Bhardwaj, *et al.,* "Advanced silicon etching using high-density plasmas," *Micromach. and Microfab.,* vol. 2639, pp. 224-233, Sept. 1995
[57] L. Franz and A. Schilp, "Method of anisitropically etching silicon," U.S. Patent 5501893, Mar. 3, 1996
[58] R. Marcus and T. Sheng, "The oxidation of shaped silicon surfaces," *J. Electrochem. Soc.,* vol. 129, no. 6, pp. 1278-1282, Oct. 1982
[59] D. Kao, *et al.,* "Two-dimensional thermal oxidation of silicon. II. Modeling stress effects in wet oxides," *IEEE Trans. Electron Devices,* vol. 35, no. 1, pp. 25-37, Jan. 1988
[60] M.D. Irwin, *et al.,* "p-Type semiconducting nickel oxide as an efficiency-enhancing anode interfacial layer in polymer bulk-heterojunction solar cells," *Proc. Nat. Aca. Sci.*, vol. 105, no. 8, pp. 2783-2787, Feb. 2008
[61] *Handbook of Chemistry and Physics,* 95th ed., CRC Press, Boca Raton, FL, 2015, pp. **12**-124
[62] *Handbook of Deposition Technologies for Films and Coatings*, (3rd ed.) William Andrew Publishing, Norwich, NY, 2009, pp. 623-629
[63] *Instrumental Thin-Layer Chromatography,* Elsevier, Amsterdam, Netherlands, pp. 61
[64] J.W. Sun, "Method for removing poly silicon," U.S. Patent 20080299682 A1, Dec. 4, 2008
[65] P.B. Sankar, "Measurement of air breakdown voltage and electric field using standard sphere gap method," M.S. thesis, Dept. Elec. Eng., Nat. Inst. Tech., Rourkela, India, 2011
[66] *Handbook of Chemistry and Physics,* 95th ed., CRC Press, Boca Raton, FL, 2015, pp. **12**-41 – **12**-42
[67] *Chemistry of the Elements,*2nd ed., Elsevier, Amsterdam, Netherlands, pp. 222
[68] *Chemistry of the Elements,*2nd ed., Elsevier, Amsterdam, Netherlands, pp. 1148
[69] ASML, *Twinscan NXT:1980Di,* [Online]. Available: https://www.asml.com/asml/show.do?lang=EN&ctx=46772&dfp_product_id=10567
[70] *Lithography: Principles, Processes and Materials*, Nova Science Publishers, Hauppage, NY, 2011, pp. 133-148
[71] *Nanofabrication Techniques and Principles*, Springer, Berlin, Germany, pp. 11-41
[72] T.M. Clarke, *et al.,* "Free energy control of charge photogeneration in polythiophene/fullerene solar cells: the influence of thermal annealing on P3HT/PCBM blends," *Adv. Fun. Mat.,* vol. 18, no. 24, pp. 4029-4035, Dec. 2008

[73] S. Lattante, “Electron and hole transport layers: their use in inverted bulk heterojunction polymer solar cells,” *Electronics,* vol. 3, no. 1, pp. 132-164, Mar. 2014