Design of Constant Transconductance Reference Circuits for Ultra-Low Power Applications

by

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Abstract

The semiconductor industry strives to develop ultra-low power circuits and systems because of the ever-increasing consumer demand for more functionality and longer battery life for portable electronic devices. Subthreshold operation brings both reduced power consumption through lower voltage operation and increased power efficiency since the ratio of a transistor's transconductance to its biasing current (g_m/I_{ds}) is maximized in the subthreshold region. A major challenge of operating in subthreshold is the magnified effect of process, voltage and temperature (PVT) variations because of the exponential current-voltage relationship of the transistors. Under PVT variations, a constant transconductance is needed to limit changes to main circuit parameters, such as gain, frequency response and input matching, to ensure devices operate within specifications.

The conventional method of maintaining a constant transconductance is by using a beta-multiplier. The effects of channel length modulation cause its transconductance to vary significantly with temperature and voltage. The use of cascode current mirrors reduces the channel length modulation effect at the cost of a higher minimum operating voltage, while using operational amplifiers (op-amp) to equalize the drain voltages, does not entirely eliminate the channel length modulation effect because of the temperature-dependent difference in the source voltages. Other existing works proposed to further minimize the issues of channel length modulation by equalizing the drain source voltage or by cancelling out the effects of channel length modulation by using differential signaling. These methods have the drawbacks of increased reliance on external references

and precise components or have limited applications while still requiring the use of cascode and op-amps.

This thesis presents a constant transconductance reference circuit for subthreshold operation that creates a constant transconductance by subtracting two independent transconductance references. By taking the difference between the output currents of the two independent transconductance references, variations over process, voltage and temperature are reduced by minimizing the effects of channel length modulation without relying on op-amps to regulate the drain voltage. The proposed constant transconductance reference is self-contained and developed to work in place of conventional reference circuits, without influencing the characteristics of the core device. The proposed reference is implemented in TSMC's 65 nm process, and can provide a constant transconductance over a temperature range of -30°C to 120°C, and a supply voltage range of 0.5 to 1.5 V. A maximum variation of $\pm 0.197\%$ transconductance over temperature and $\pm 1.82\%$ transconductance over the supply voltage can be obtained. Through the subtraction, the proposed circuit also shows less process variation against the conventional constant transconductance reference. The proposed constant transconductance reference posts the highest power efficiency (transconductance over power consumption) amongst the reported constant transconductance references up to the date of this writing. At 0.5 V, the constant transconductance reference produces a transconductance of 21.95 μS while consuming 2.06 μW.

Preface

This thesis is an original work by Martin Lee. Parts of this thesis has been submitted for initial review as M. Lee and K. Moez, "A 0.5-1.5V Highly Efficient and PVT-Invariant Constant Transconductance Reference in CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, 2020.

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Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation for Subthreshold Operation

The demand for ultra-low power (ULP) design is continuing to increase as the semiconductor industry strives to increase the functionality and battery life of portable electronic devices. This is particularly essential for many Internet of Things (IoT) devices, which are often battery powered. IoT devices are expected to operate reliably and be deployed anywhere and everywhere, but these expectations are constrained by current battery technology. While improvements are continuously made to increase the energy density of batteries, advancements in energy storage have been outpaced by advancements in electronics [1]. The predominant method to supply power for portable electronics is with lithium-ion (Li-ion) batteries, which were first commercialized in 1991. For IoT devices to operate constantly, these Li-ion batteries require regular maintenance. As the number of IoT devices are scaled up, the required maintenance also scales up, increasing the financial and operational cost for deploying an IoT infrastructure. In extreme cases, maintenance may not be feasible if IoT devices are located in remote or inaccessible environments. For these cases, harvesting ambient energy may be the only option to increase the autonomy of these devices, but there are limitations to the amount of energy that can be harvested [2]. Whether energy harvesting or battery operation is used, there are strict constraints in available energy. It is imperative to improve both power consumption

and efficiency; to maximize the use of the limited available energy for operation, rather than depending on relying on improvements to energy capacities. Operating in the subthreshold region is one of the main ways of addressing this challenge, as it can provide lower power consumption coupled with higher power efficiency. These advantages come not only at a cost of performance degradation, but also magnified process, voltage and temperature (PVT) variations. These variations will severely compromise the robustness and operation of the device [3]. These PVT variations will need to be controlled to ensure subthreshold devices operate as intended. This thesis will be focused on controlling the PVT variations associated with operating in the subthreshold region.

1.2 Subthreshold Operation

One of the main techniques to achieve low power operation is to operate circuits in the subthreshold region for CMOS circuits [3]. The subthreshold region is defined by operating MOSFETs under the threshold voltage. Ideally, transistors operate as switches that stop conducting when they are turned off, with an input voltage less than the threshold voltage. However in practice, transistors do not immediately stop conducting when the input voltage falls below the threshold voltage: a small drain current still flows, resulting in subthreshold operation. In the subthreshold region, the applied gate voltage is not high enough to create an inversion channel to support a flow of majority carriers. Therefore, the current is not dominated by drift current but by diffusion current, similar to BJTs, and has an exponential relationship to the input voltage defined by the following I-V equation [3]:

$$I_{ds} = I_0 exp\Big(\frac{V_{gs} - V_{th}}{nV_T}\Big)\Big(1 - exp\Big(\frac{-V_{ds}}{V_T}\Big)\Big)(1 + \lambda V_{ds}), \tag{1.1}$$

where V_{gs} is the gate source voltage, V_{th} is the threshold voltage, V_{ds} is the drain source voltage, $V_T = k_B T/q$ is the thermal voltage, n is the subthreshold slope factor, λ is the

channel length modulation coefficient and the characteristic current, I_0, is defined as:

$$I_0 = \mu C_{ox} \frac{W}{L} (n-1) V_T^2, \tag{1.2}$$

where μ is the charge mobility, C_{ox} is the gate oxide capacitance and W/L represent the dimensions of the MOSFET. As shown in (1.1), the overdrive voltage, $(V_{gs} - V_{th})$, is exponentially related to the subthreshold current. When V_{ds} is large enough in subthreshold, the drain current saturates and (1.1) simplifies to:

$$I_{ds} = I_0 exp\Big(\frac{V_{gs} - V_{th}}{nV_T}\Big)(1 + \lambda V_{ds}), \tag{1.3}$$

The advantage of operating in subthreshold comes from the lower required supply voltage. To operate in saturation, as defined by the square law equation, V_{gs} needs to be larger than V_{th}, and V_{ds} needs to be larger than the overdrive voltage, $V_{gs} - V_{th}$. This leads to constraints on the minimum supply voltage to place MOSFETs into saturation. These constraints are not present when operating in subthreshold. Subthreshold does not require V_{gs} to be above V_{th}. Furthermore, as shown in (1.1), the third term of the subthreshold current saturates when V_{ds} is larger than 3 to 5 V_T, this means that V_{ds} saturates around 75 mV to 125 mV, which is significantly lower than the overdrive voltage. Reducing the required voltage can lead to significant power savings because the power scales linearly with voltage if the current draw remains the same. Additionally, the g_m efficiency, transconductance-to-current ratio, that dictates the power efficiency of many analog circuits is maximized in the subthreshold operation. By deriving the subthreshold g_m as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{I_{ds}}{nV_T}, \tag{1.4}$$

the g_m efficiency can be expressed as follows:

$$\frac{g_m}{I_{ds}} = \frac{1}{nV_T}. \tag{1.5}$$

In comparison to the g_m efficiency of operating MOSFETs in saturation, using the squared-law model we obtain:

$$\frac{g_m}{I_{ds}} = \frac{2}{V_{gs} - V_{th}}, \tag{1.6}$$

and the g_m efficiency of operating MOSFETs in the linear region is given by:

$$\frac{g_m}{I_{ds}} = \frac{1}{V_{gs} - V_{th} - \frac{V_{ds}}{2}}. \tag{1.7}$$

Since the thermal voltage, V_T, is approximately 25 mV at nominal temperature, g_m efficiency is maximized in the subthreshold region. Plotting g_m/I_{ds} while sweeping V_{gs} and keeping V_{ds} constant demonstrates the efficiency by operating in subthreshold compared to saturation. This is represented in Fig. 1.1. As shown, as the MOSFET transitions from operating in subthreshold to saturation, g_m rises, however g_m/I_{ds} falls. This aligns with the g_m/I_{ds} equations formulated above for subthreshold and saturation operation. Subthreshold operation can simultaneously reduce power consumption and improve efficiency for CMOS circuits. However, speed and performance in subthreshold is sacrificed for lower power consumption and power efficiency. In some energy constrained applications, low speed may not be an issue, this can make subthreshold operation desirable.

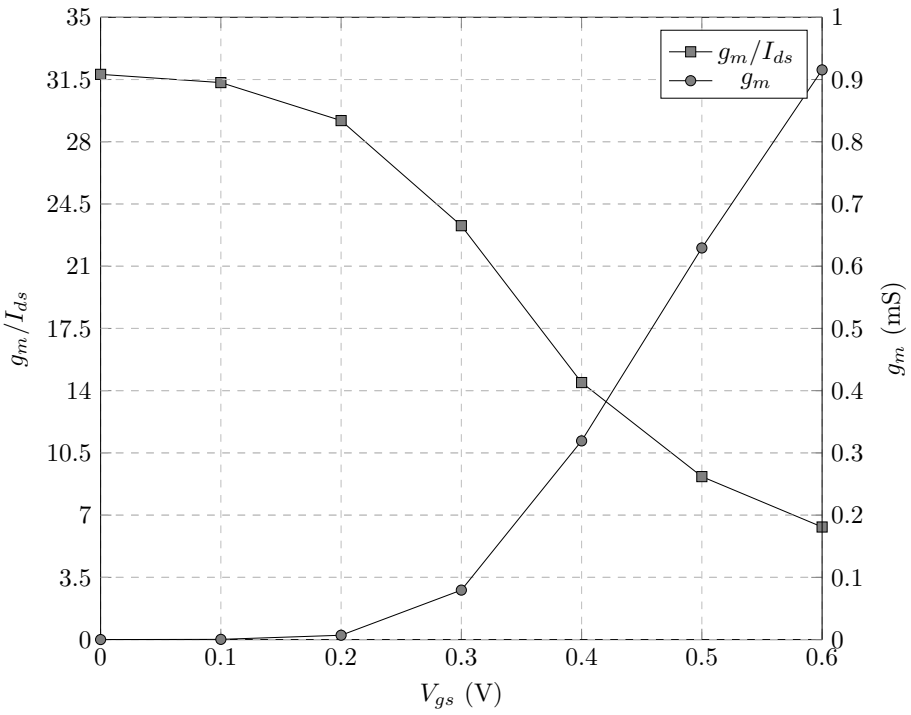


Figure 1.1: g_m/I_{ds} and g_m from operating in subthreshold to saturation

1.3 PVT Variations of Subthreshold MOSFETs

The advantages of subthreshold operation come at the expense of increased sensitivity to process, voltage and temperature (PVT) variations. This sensitivity is due to the exponential relationship between PVT variations and the output current, which will translate to relatively large variations in the device transconductance (g_m), which often determines main circuit parameters. For instance, the gain, frequency response and impedance matching of a low-noise amplifier (LNA) are strongly dependent on the transistor's g_m. Therefore, it is critical to keep g_m as constant as possible for all operation conditions so that the performance of the circuit remains consistent. This sensitivity of subthreshold MOSFETs to PVT variations can be explained by its I-V characteristic derived in (1.1). Voltage variations directly affect V_{gs} and V_{ds}, resulting in changes along the exponential I-V curve through V_{gs}. Process variations affect the dimensions of the MOSFET, such as the channel width, channel length and oxide thickness, which translates

to changes to the characteristic current and threshold voltage. While temperature variations affect the thermal voltage, carrier mobility, threshold voltage and subthreshold slope factor. The relationship of carrier mobility and threshold voltage with temperature are not obvious from (1.1), but their variations with temperature can be shown through the following relationships [4]:

$$V_{th}(T) = V_{th}(T_0) - A(T - T_0), \tag{1.8}$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha}, \tag{1.9}$$

where T_0 is the reference temperature, α is the mobility temperature parameter and A is the threshold voltage coefficient. This describes the threshold voltage as having a linear

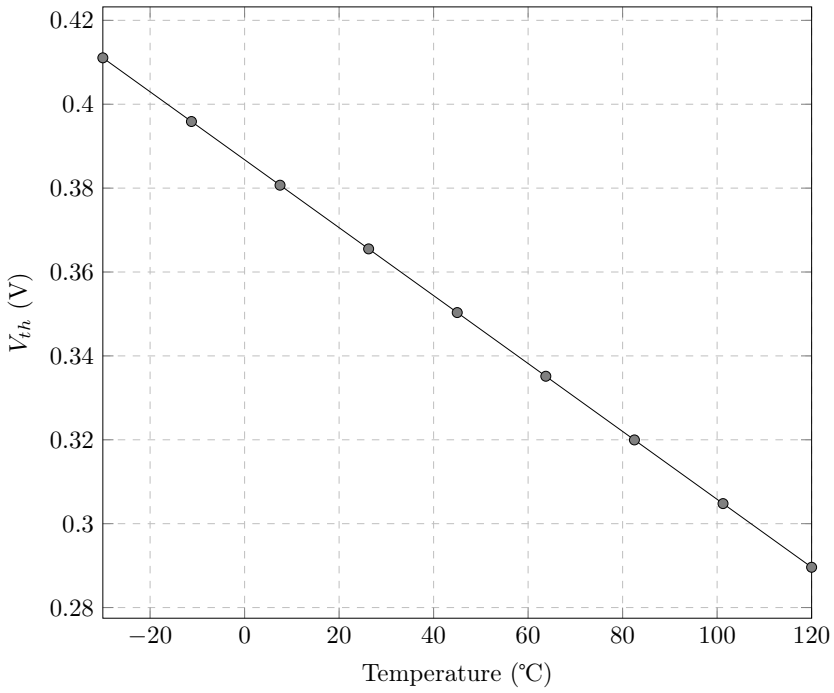


Figure 1.2: Threshold voltage vs. temperature

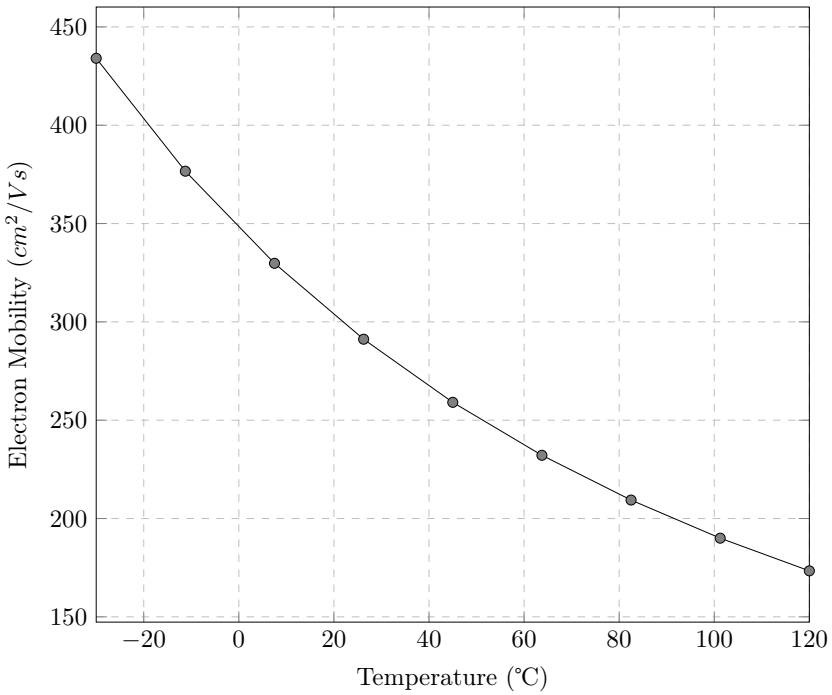


Figure 1.3: Electron mobility vs. temperature

relationship with temperature through the linear coefficient, A, whereas, mobility adopts a power law relationship with temperature. While both parameters decrease with temperature, the decrease in threshold voltage causes the current to rise, while the decrease in carrier mobility causes the current to fall, as shown in (1.1). These variations are verified through simulation as shown in Fig. 1.2 and 1.3. In addition to the carrier mobility and threshold voltage, it is important to evaluate the temperature dependency of the subthreshold slope factor since g_m varies inversely with n. To derive its temperature dependency, we first define n by the following equation:

$$n = 1 + \frac{C_{dep}}{C_{ox}}, \tag{1.10}$$

where C_{dep} is the depletion capacitance per unit area and C_{ox} is the oxide capacitance per unit area. Equation (1.10) shows that n will increase with temperature. As temperature increases, the depletion layer width decreases due to the increase in carrier density. The

smaller depletion width will cause C_{dep} to increase. As a result, n should increase with temperature. To verify its temperature dependency, n can be linked to the subthreshold swing, SS. It is defined by how much V_{gs} needs to increase to increase the subthreshold current by an order of magnitude as the MOSFET turns on [3]:

$$\begin{aligned} SS &= \left[\frac{\partial log(I_{ds})}{\partial V_{gs}}\right]^{-1}, \\ SS &= nV_T ln(10). \end{aligned} \tag{1.11}$$

n can be extracted from the subthreshold swing shown in Fig. 1.4a. As temperature increases, the slope of $log(I_{ds})$ decreases, therefore SS increases. Fig. 1.4b verifies the positive temperature dependency of n. The combination of the thermal voltage in the characteristic current, and the threshold voltage in the exponential will cause the subthreshold to increase overall with temperature.

As shown, the PVT variations have a significant impact on the characteristic current

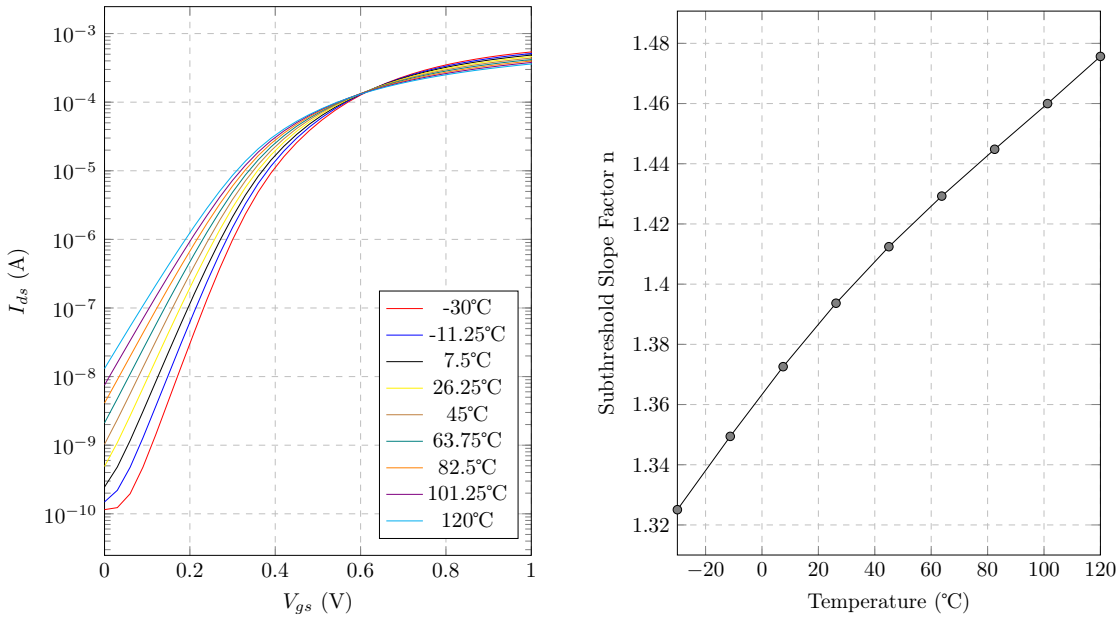
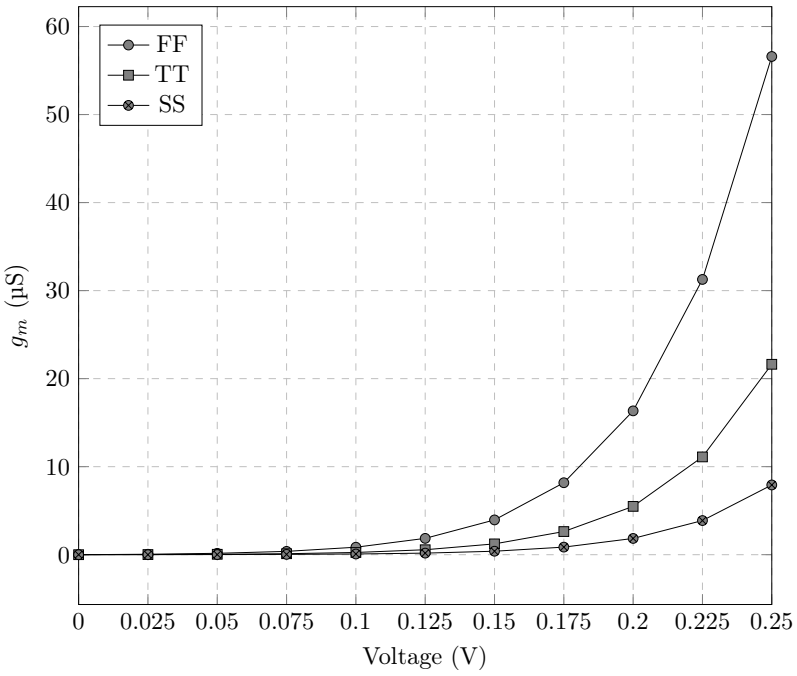
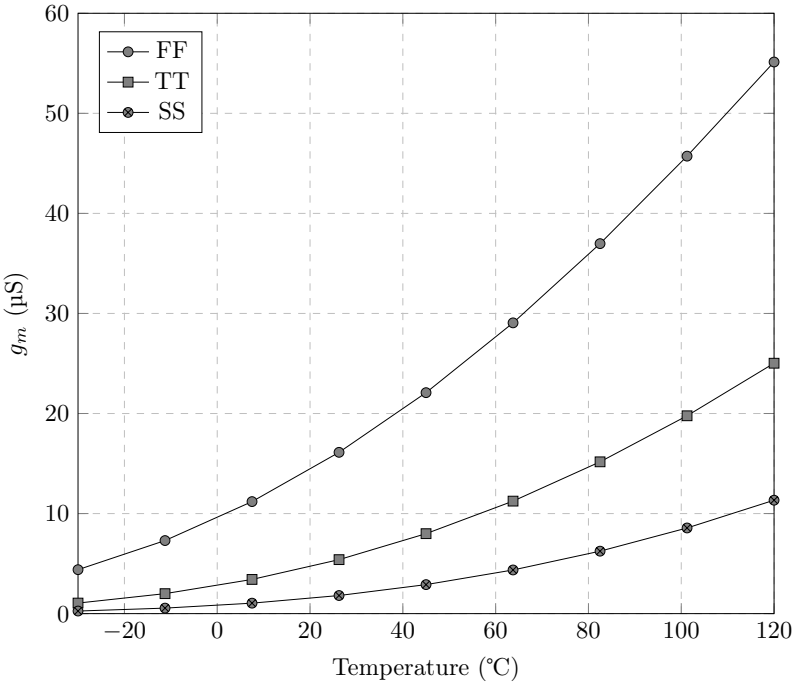


Figure 1.4: Determining subthreshold slope factor (a) $log(I_{ds})$ vs. V_{gs} (b) subthreshold slope factor vs. temperature at V_{gs} = 0.25 V



(a)



(b)

Figure 1.5: g_m over PVT variations

and the overdrive voltage that resides inside the exponential term. The variations inside the exponential will create a larger impact on the drain current under subthreshold

operation compared to operating in saturation. Subsequently, these variations to the drain current will translate to variations in g_m since g_m is proportional to I_{ds}, as shown in (1.4). The PVT dependency in subthreshold operation is illustrated in the simulation of g_m for a diode-connected MOSFET over voltage and temperature for the fast-fast (FF), typical-typical (TT) and slow-slow (SS) process corners in Fig. 1.5. This demonstrates that g_m changes considerably due to PVT variations. For circuits that depend on a constant g_m, these PVT variations will need to be controlled.

1.4 Thesis Overview

This thesis is organized into five chapters. Chapter 1 presents the motivation behind operating in the subthreshold region. This includes the advantages from lower power consumption, and the disadvantages of higher PVT variability under subthreshold operation. PVT variations can significantly modify g_m; therefore, they need to be controlled to benefit from the low power draw and improved efficiency of operating below the threshold voltage.

Chapter 2 presents the conventional method of producing a constant g_m. This details the requirement, principles and design of a constant g_m reference circuit, with further exploration into the issues of the conventional constant g_m reference circuit that causes it to be susceptible to PVT variations.

In Chapter 3, existing works that propose solutions to the issues of the conventional constant g_m reference are presented. This addresses issues such as the potentially high PVT variations of resistors, and second-order effects of MOSFETs in the conventional constant g_m reference. This chapter provides understanding for the proposed constant g_m reference circuit.

Chapter 4 presents the proposed constant g_m reference that reduces the effects of channel length modulation. By subtracting the output currents of two independent g_m

reference circuits, the sensitivity of the resulting current of the proposed g_m reference circuit to temperature, voltage, and process is significantly reduced. The principles, design and results of the proposed circuit will be detailed. This demonstrates the flexibility of the design for general-purpose use.

The thesis concludes in Chapter 5, summarizing the contribution and discussing further improvements to the proposed constant g_m reference circuit.

Chapter 2

Conventional Constant Transconductance Reference

In Chapter 1, the mathematical model for subthreshold operation was presented. It was concluded that the efficiency of g_m is maximized in the subthreshold region at the cost of increased PVT variations. Here, we present how subthreshold g_m can be made insensitive to PVT variations, and describe the conventional method of creating a constant g_m reference.

2.1 Creating Constant g_m

An interesting result can be found in (1.4). Since the thermal voltage varies proportionally with temperature, if the subthreshold current can be controlled to have an approximately proportional relationship with temperature, then g_m can become insensitive to both temperature and supply voltage variations. This suggests that the reference circuit must output a proportional-to-absolute-temperature (PTAT) current, which can be used to bias a transistor to maintain a constant g_m. This forms the basis for g_m reference circuits.

2.2 Beta-Multiplier

The conventional method of producing the PTAT current described above to maintain a constant g_m across PVT variations using MOSFETs as shown in Fig. 2.1, known as the beta-multiplier, was proposed in [5]. Conventionally, the beta-multiplier is biased into

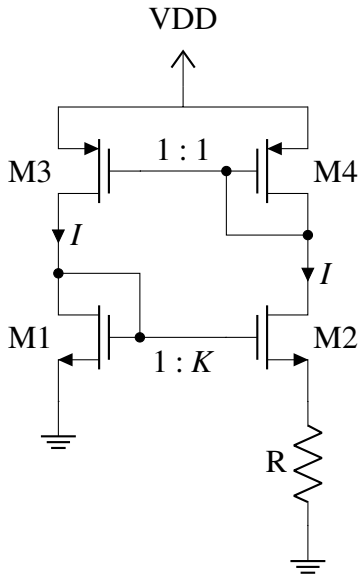


Figure 2.1: Conventional beta-multiplier

saturation to generate a constant g_m; however, constant g_m biasing can also be achieved in subthreshold [5, 6]. To demonstrate how the ideal beta-multiplier can produce the required PTAT current to create a constant g_m operating in the subthreshold saturation region, it is helpful to first ignore second-order effects. Equation (1.3) simplifies to (2.1), and V_{gs} can be defined with respect to the subthreshold current as shown:

$$I_{ds} = I_0 exp\Big(\frac{V_{gs} - V_{th}}{nV_T}\Big), \tag{2.1}$$

$$V_{gs} = nV_T ln\Big(\frac{I_{ds}}{I_0}\Big) + V_{th}. \tag{2.2}$$

The beta-multiplier should be self-biased to achieve independence from the supply voltage, which means that the reference current must be derived from its output and vice versa. This is done by bootstrapping the current in either of the two branches of the beta-multiplier to each other using a combination of NMOS and PMOS current mirrors [7]. To create the PTAT current, M2 is sized K times larger than M1, while M2 is source degenerated with a resistor, R, to create a difference in V_{gs}. Using (2.2), the PTAT current

can be mathematically derived by solving for the current through R, noting that the difference in V_{gs} between M1 and M2 will drop over R:

$$\begin{aligned} IR &= V_{gs1} - V_{gs2}, \\ &= \left[nV_T ln\left(\frac{I_{ds}}{I_0}\right) + V_{th}\right] - \left[nV_T ln\left(\frac{I_{ds}}{KI_0}\right) + V_{th}\right], \\ &= nV_T \left[ln\left(\frac{I_{ds}}{I_0}\right) - ln\left(\frac{I_{ds}}{KI_0}\right)\right], \end{aligned} \tag{2.3}$$

$$I = \frac{nV_T ln(K)}{R}. \tag{2.4}$$

Substituting this current into (1.4) gives the g_m produced by the ideal beta-multiplier:

$$g_m = \frac{ln(K)}{R}. \tag{2.5}$$

The resulting g_m of the beta-multiplier is only a function of the size difference, K, between M1 and M2 and the resistor, R. Provided that R is PVT-invariant, (2.5) shows that g_m is independent of both temperature and voltage, while having a low dependency to process variations because of K. The current of the beta-multiplier can be mirrored to provide a constant g_m bias for the desired circuit.

2.2.1 Stability

The beta-multiplier uses positive feedback, through two current mirrors with their inputs and outputs connected, which may cause instability in the circuit. It is important to analyze the feedback loop of the circuit to prevent instability. The closed loop gain of a positive feedback loop is defined by the following:

$$G = \frac{A}{1 - A\beta}, \tag{2.6}$$

where G is the closed loop gain, A is the open loop gain, and $A\beta$ is the loop gain. In a positive feedback system, the loop gain must be less than one to ensure stability. Calculating the loop gain is done by breaking the loop at either the gate of the NMOS or PMOS transistors and finding the gain, which is equivalent to the combined gain of the NMOS and PMOS current mirror. Noting that the g_m of all four transistors are equal under subthreshold conditions, and g_m is defined by (2.5):

$$\begin{aligned} A\beta &= \left[\frac{g_{m2}\frac{1}{g_{m4}}}{1 + g_{m2}R}\right]\left[\frac{g_{m3}}{g_{m1}}\right], \\ A\beta &= \frac{1}{1 + g_{m2}R}, \\ A\beta &= \frac{1}{1 + ln(K)}. \end{aligned} \tag{2.7}$$

The stability of the beta-multiplier is achieved by source degenerating M2. If K>1 then the loop gain is less than one; therefore, the beta-multiplier can be made stable. One concern is the shunt capacitance at the source of M2. If this capacitance is large, this can cause the beta-multiplier to oscillate which may occur if the resistor is implemented off-chip [6].

2.2.2 Effects of Substrate Bias

In Section 2.2, the current of the beta-multiplier is derived by neglecting the body effect of M2, as a result of shorting the source and substrate of M2. However, it is important to consider the impact of a non-zero source-substrate bias on the operation of the beta-multiplier. When the substrate bias of M2 is present, this modifies the threshold voltage of M2 through the body effect, causing a mismatch in the threshold voltage between M1 and M2. [5] extends the derivation of (2.1) by including an additional term to

model the body effect. The subthreshold current and V_{gs} becomes:

$$I_{ds} = I_0 exp\Big(\frac{V_{gs} - V_{th}}{nV_T}\Big) exp\Big(\frac{-(n-1)V_{sb}}{nV_T}\Big), \tag{2.8}$$

$$V_{gs} = nV_T ln\Big(\frac{I_{ds}}{I_0}\Big) + V_{th} + (n-1)V_{sb}. \tag{2.9}$$

Undergoing a similar derivation, the current then becomes:

$$I = \frac{V_T ln(K)}{R}. \tag{2.10}$$

When a non-zero source-substrate voltage is present, an exact PTAT current without the subthreshold slope factor that is present in (2.4) is produced by an ideal beta-multiplier, assuming a PVT-invariant resistor. This is beneficial for a temperature sensor or a bandgap reference that uses a PTAT and complementary to absolute temperature (CTAT) current, but is undesirable for a constant g_m reference because the subthreshold g_m is proportional to $1/nV_T$. Therefore, a zero source-substrate voltage is required to produce a constant g_m that can be accomplished by shorting the substrate and source of M2.

2.3 PVT Dependency of Beta-Multiplier

The two main issues of the beta-multiplier are the PVT variations of the resistor and the effects of channel length modulation. As shown in (2.5), g_m is a function of the size ratio between M2 and M1 and the resistor, R, allowing g_m to be independent of the supply voltage and temperature. If R is process-independent, this translates also to low process variations in the beta-multiplier. In practice, the PVT sensitivity of R, and channel length modulation can significantly alter the ability of the beta-multiplier to produce a constant g_m. Since g_m is proportional to $1/R$, any PVT variations of the resistor will significantly affect

g_m. This PVT sensitivity will depend on the implementation of the resistor [8]. This will be significant if the resistor is proportional to temperature, causing the beta-multiplier to output an approximately constant current rather than the PTAT current needed for a constant g_m. In addition, large resistors are needed to operate the beta-multiplier at very low current and power. On-chip resistors typically have low sheet resistances, requiring a large area to implement high resistances. Fabrication will affect the absolute resistance attainable. The limited size, precision and high PVT variations of integrated resistors makes it difficult to develop a fully integrated solution. Therefore, these resistors are often implemented off-chip, which increases the size, complexity and cost of the circuit.

The effects of channel length modulation arise because of the mismatch in V_{ds} in simple current mirrors. Channel length modulation increases as the channel length shortens, a result of reduced output impedance, causing poor tracking performance in the current mirror. The effects of channel length modulation can significantly influence the PVT sensitivity of the beta-multiplier. We can mathematically determine the impact of channel length modulation on the PMOS and NMOS current mirrors. Differences in V_{ds} between M1 and M2, and M3 and M4 modify (2.4) to:

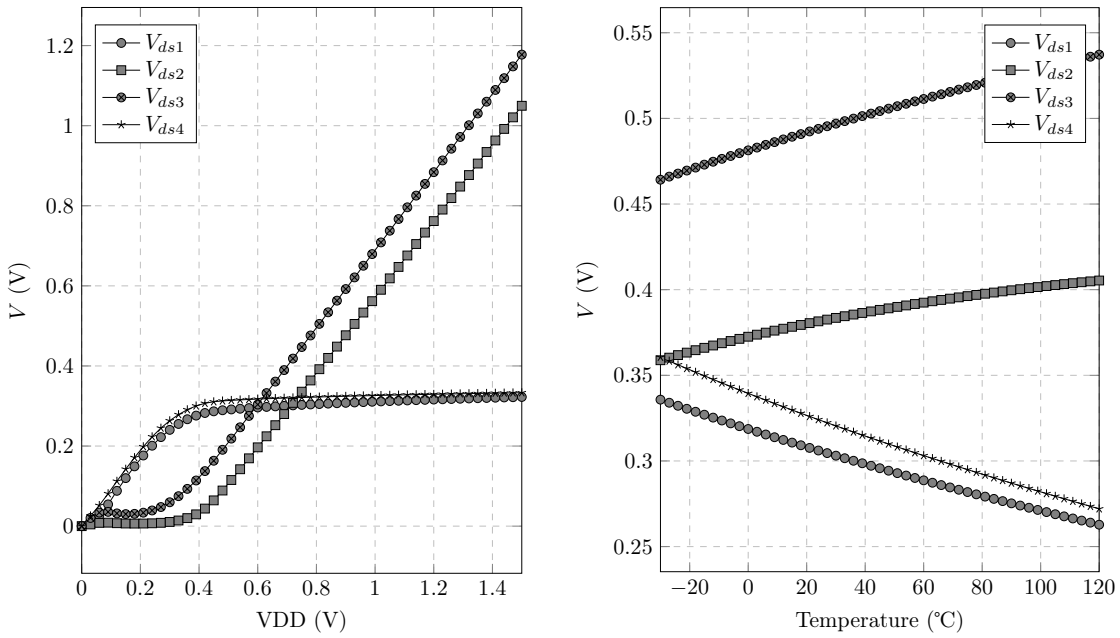
$$I = \frac{nV_T}{R}\Big[ln(K) + ln\Big(\frac{(1+\lambda V_{ds2})}{(1+\lambda V_{ds1})}\Big) + ln\Big(\frac{(1+\lambda |V_{ds3}|)}{(1+\lambda |V_{ds4}|)}\Big)\Big]. \tag{2.11}$$

The suffix appended to V_{ds} in (2.11) indicates the V_{ds} of the respective transistors in Fig. 2.1. The V_{ds} mismatch between the NMOS and PMOS transistors causes the second and third logarithmic terms to appear in the PTAT current, respectively. The issue is how V_{ds} of the four transistors evolve over temperature. If the V_{ds} of the PMOS and NMOS pair of transistors has the similar relationship to temperature, this means that the second and third logarithmic terms remain constant. Therefore, despite the mismatch between V_{ds}, channel length modulation should not modify the PTAT current. It is when V_{ds} of the PMOS and

NMOS pair of transistors evolve differently over temperature that the logarithmic terms cause a temperature dependency, which results in variations in the PTAT current. The temperature dependency of V_{ds} for the four transistors can be determined by deriving the V_{ds} of the diode-connected MOSFETs, M1 and M4. There are several assumptions made to simplify the derivation for the temperature dependency of V_{ds}. Second-order effects are neglected, and the beta-multiplier is assumed to operate ideally. The subthreshold slope factor, n, is assumed to be temperature-independent, although n does increase with temperature. Since M1 is diode-connected, the V_{ds} of M1 is equal to (2.2). The temperature dependence shown previously in Chapter 1 can be substituted into the equation along with the PTAT current in (2.4). All the temperature-independent terms in the natural logarithm are grouped into a term C. This results in the following equation:

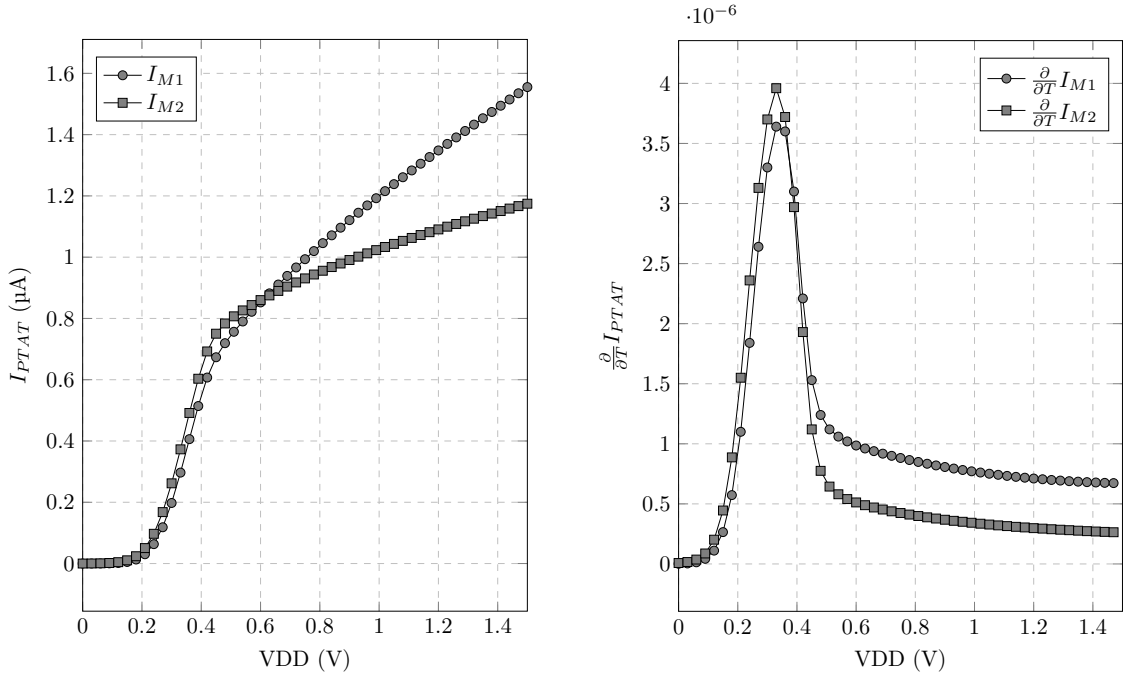
$$\begin{aligned} V_{ds1} &= nV_T ln\Big(\frac{C}{T^{\alpha+1}}\Big) + V_{th}(T_0) - A(T - T_0), \\ &= V_{th}(T_0) + AT_0 + \Big(\frac{nk_B ln(C)}{q} - A\Big)T - \frac{nk_B(\alpha+1)}{q} T ln(T). \end{aligned} \tag{2.12}$$

If the currents through both branches of the beta-multiplier are equal, V_{ds4} will have the same relationship to temperature shown in (2.12), aside from the differences between PMOS and NMOS transistors. There are few things to note from (2.12). A is a positive coefficient, while α is a negative parameter, and the most frequent figures used are -2 mV/°C and -1.5, respectively [4]. C is found to be positive but is less than 1; therefore, $nk_B ln(C)/q$ is a negative coefficient. Equation (2.12) shows that as temperature increases, the third term will cause V_{ds} of M1 and M4 to fall. Although the fourth term of (2.12) increases with temperature, its coefficient is much smaller than A; therefore, V_{ds1} will decrease with temperature overall. As V_{ds1} decreases, the rest of the supply voltage will need to be absorbed by M3 since V_{ds3} is simply the difference between VDD and V_{ds1}. Similarly for the right branch of the beta-multiplier, V_{ds4} will decrease, and the rest of the supply voltage will drop over M2 and R. The voltage across R is determined by the PTAT



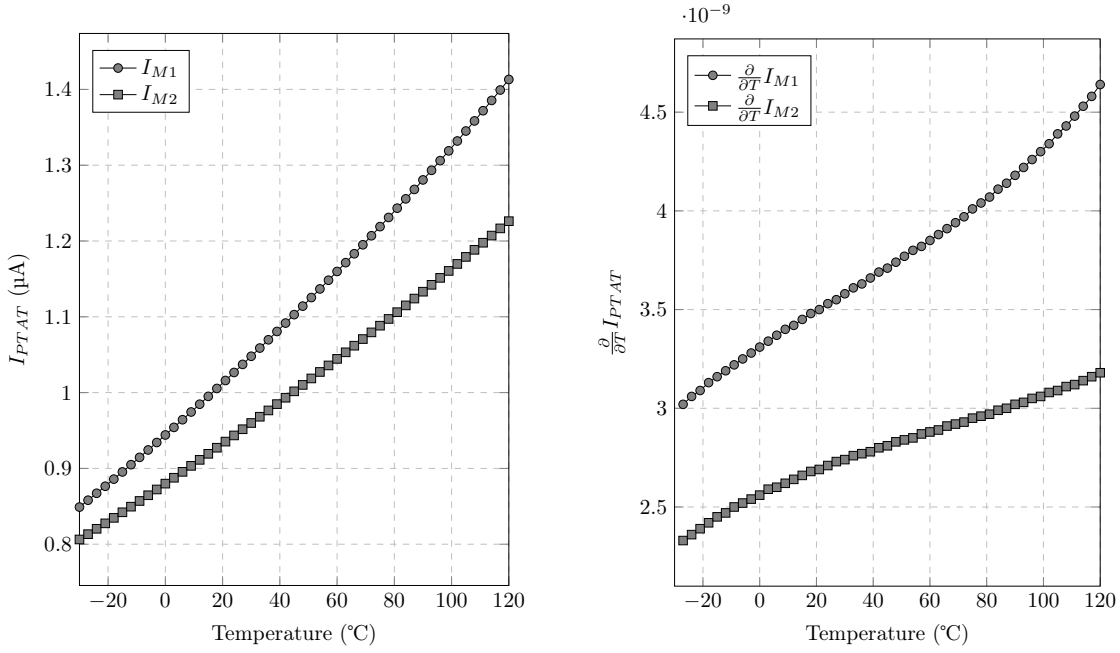
(a) (b)

Figure 2.2: Variation of V_{ds} of conventional beta-multiplier over (a) temperature and (b) supply voltage



(a) (b)

Figure 2.3: I_{PTAT} of conventional beta-multiplier vs. VDD and its derivative



(a) (b)

Figure 2.4: I_{PTAT} of conventional beta-multiplier vs. temperature and its derivative

current, $nV_T ln(K)$, so it will rise proportionally to temperature. The rest of the voltage must be absorbed by M2. The result is that V_{ds} of M1 and M4 will decrease, while the V_{ds} of M2 and M3 will increase with temperature. The variations of V_{ds} vs. temperature aligns with the results in Fig. 2.2. The variations of V_{ds} vs. voltage are explained by the output impedance of each of the MOSFETs. As a result, the effects of channel length modulation deviations will cause the PTAT current, needed for constant g_m, to become PVT-dependent as shown in Fig. 2.3 and 2.4.

2.4 Summary

In this chapter, the idea and conventional method of producing a constant g_m is presented in the form of the beta-multiplier. A brief stability and substrate bias analysis was performed. Ideally, the beta-multiplier can produce a g_m that is only a function of the size difference between M1 and M2, and a resistor, R, resulting in a g_m that is PVT-invariant. However, the PVT variations of the resistor and second-order effects of the

MOSFET can significantly affect the output g_m. These effects are undesirable for producing a g_m reference that aims to be PVT-independent.

Chapter 3

Literature Review

As highlighted in Chapter 2, the beta-multiplier deviates from its ideal behaviour because of the effects of channel length modulation of the transistor causing both supply voltage and temperature dependence and the PVT variations in the resistors. Recent works on constant g_m references have focused on mitigating these undesirable effects to improve upon the PVT independence of the beta-multiplier.

3.1 Resistorless Reference Circuits

One major issue highlighted above with the beta-multiplier is the need for a resistor to generate a PTAT current. The dependence on the resistor to generate a constant g_m causes the reference circuit to be highly process variant. This resistor needs to be precise and exhibit minimal variation over temperature. One solution to this issue is to use on off-chip resistor; another solution is to use post-fabrication trimming [6, 9–11]. While these solution may resolve the PVT variations of the resistor, they adds cost and complexity to the fabrication process. Replacing the resistor with an equivalent resistance will reduce PVT variations and improve the ability of the beta-multiplier to produce a PVT-invariant g_m without increasing fabrication complexity.

One of the methods to replace the resistor is to use capacitors. On-chip capacitors have less temperature dependence with higher precision and less variations during fabrication

compared to resistors. A capacitor in combination with an external clock reference can be used to create a switched capacitor resistor (SCR) [7, 12, 13]. The equivalent resistance from the SCR is:

$$R_{eq} = \frac{1}{fC}, \tag{3.1}$$

where f is the clock frequency and C is the capacitance. A simple replacement of the resistor using a SCR is shown in Fig. 3.1. Unfortunately, these SCR schemes can cause the beta-multiplier to be susceptible to ripple [14]. This requires the addition of a low-pass filter to remove the ripple. The SCR can be used in other methods, as shown in Fig. 3.11 and 3.22 that will be discussed later in this chapter.

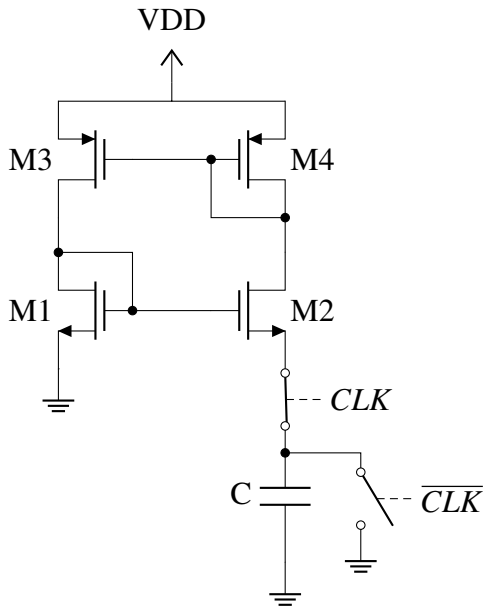


Figure 3.1: Conventional beta-multiplier with switched capacitor resistor [7]

Another method is to replace the resistor with a MOSFET equivalent. The MOSFET equivalent resistor will result in less process variation and silicon area when compared to on-chip resistors at the expense of increased power to produce the equivalent resistor. From (2.4), we can see that the voltage drop over the resistor is proportional to temperature. If

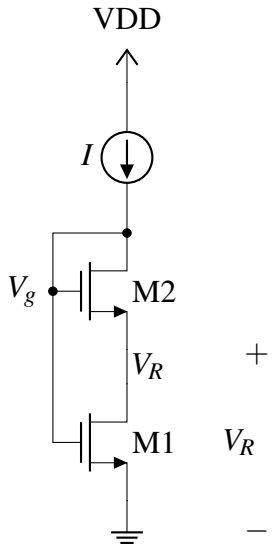


Figure 3.2: PTAT voltage source in [15]

a MOSFET can create a PTAT voltage at the source of M2, then this will be equivalent to source degenerating M2 with a resistor.

One of the methods the PTAT voltage can be realized is proposed by [15]. This PTAT voltage source is created by using a self-cascode transistor, which consists of two transistors connected in series with their gates shorted in a diode-connected fashion, as shown in Fig. 3.2. When both M1 and M2 operate in subthreshold saturation, V_R can be found to be proportional to temperature. Considering the current through M1 and M2 is modelled using the idealized subthreshold saturation current of (2.1), V_R can be determined by equating the currents of M1 and M2:

$$\begin{aligned} I_1 &= I_2, \\ S_1 I_0 exp\Big(\frac{V_{gs1}-V_{th}}{nV_T}\Big) &= S_2 I_0 exp\Big(\frac{V_{gs2}-V_{th}}{nV_T}\Big), \\ S_1 I_0 exp\Big(\frac{V_g-V_{th}}{nV_T}\Big) &= S_2 I_0 exp\Big(\frac{V_g-V_r-V_{th}}{nV_T}\Big), \\ exp\Big(\frac{V_r}{nV_T}\Big) &= \frac{S_2}{S_1}, \\ V_r &= nV_T ln\Big(\frac{S_2}{S_1}\Big). \end{aligned} \tag{3.2}$$

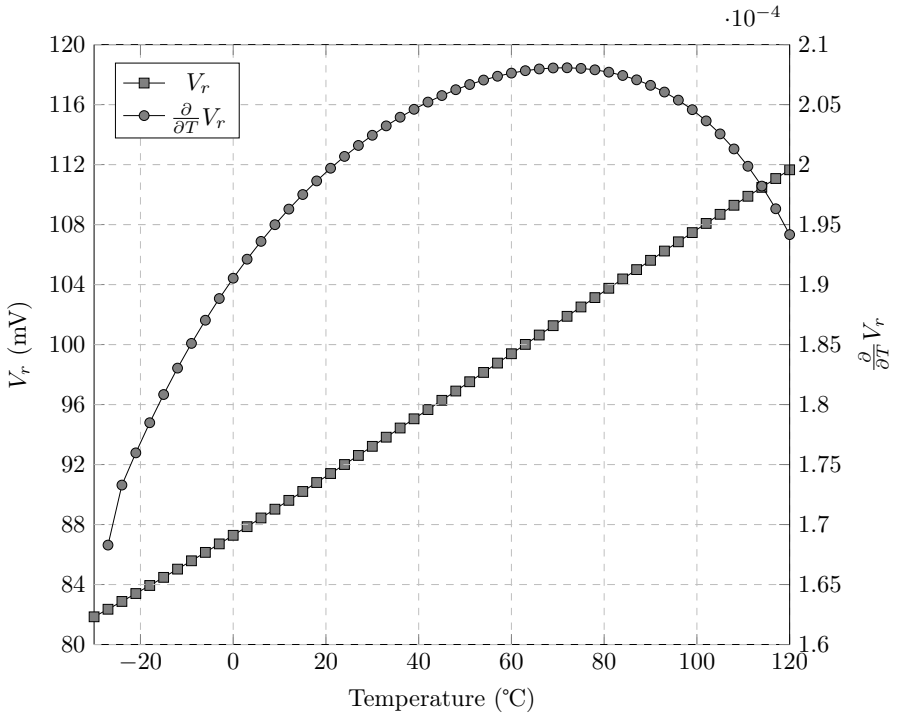


Figure 3.3: PTAT voltage, V_r, and its derivative

This shows that V_R is proportional to temperature and depends on the ratio of M1 and M2, shown as S1 and S2 respectively, while being independent of the current flowing through the transistors. This is verified by the simulating the PTAT voltage source, as shown in Fig. 3.3. The simulation is performed while biasing the voltage source using a PTAT current and making $S_2/S_1 = 10$. The PTAT voltage realized in (3.2) is equivalent to the voltage drop of the resistor required in (2.4); therefore, the PTAT voltage source can be used to replace the resistor. A number of works on resistorless constant g_m reference circuits utilize a version of this circuit to replace the resistor. [16] and [17] directly replaces the resistor using the PTAT voltage source shown in Fig. 3.4 and 3.5, respectively. [16] also modifies the conventional beta-multiplier by using an operational amplifier (op-amp) to improve tracking of the current mirror, while [17] improves the current mirror of the beta-multiplier by cascoding the current mirror. Both the use of the op-amp and cascode will be discussed in Section 3.3. When the PTAT voltage source is used in this manner, (3.2) is modified into the following due to the difference in current between M1 and M2:

$$V_r = nV_T ln\Big(\frac{S_2}{S_1}\frac{I_1}{I_2}\Big). \tag{3.3}$$

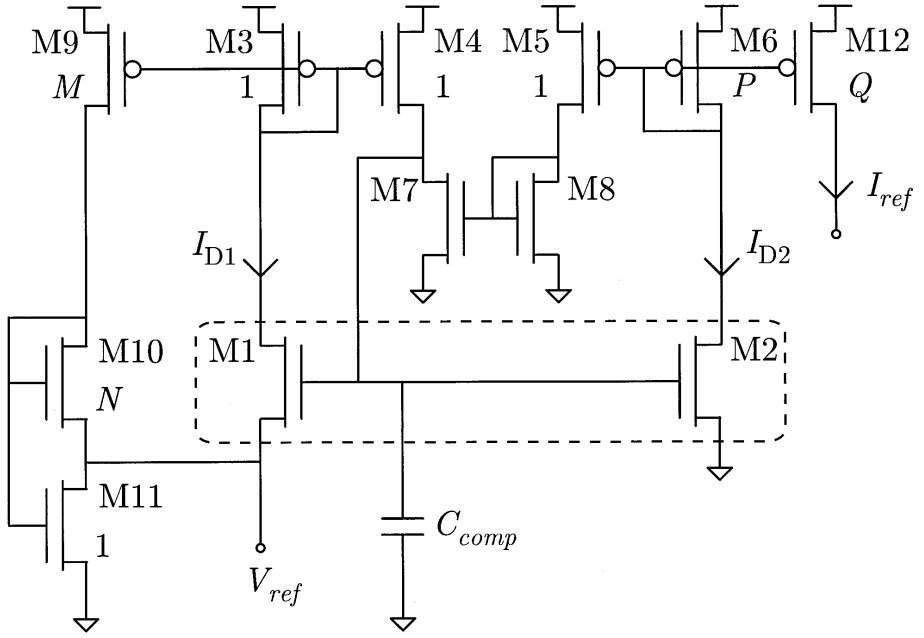


Figure 3.4: Resistorless PTAT current reference using PTAT voltage source in [16] © 2003 IEEE

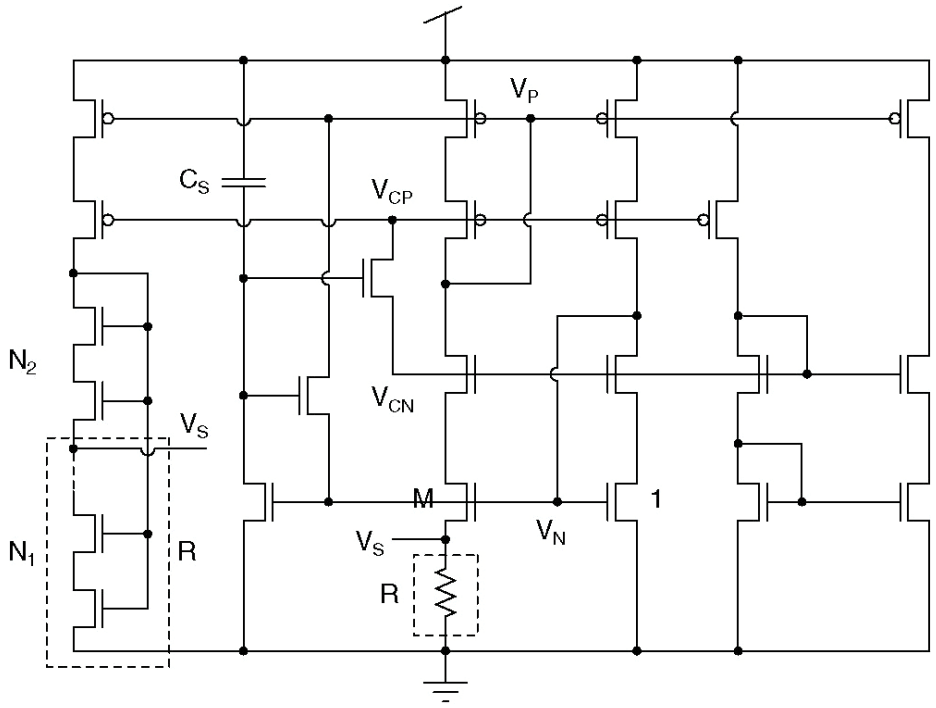


Figure 3.5: Another resistorless PTAT current reference using PTAT voltage source in [17] © 2006 IEEE

[18] uses the PTAT voltage source to extract the characteristic current, called the specific current in this work, to create a PTAT current reference. To extract the characteristic current, the PTAT voltage implemented by the self-cascode transistor biased in weak inversion is transferred, using the beta-multiplier, to the V_x node of the self-cascode transistor biased in moderate inversion, M1 is in the linear region and M2 is the saturation region. When a PTAT voltage is applied to the self-cascode transistor biased in moderate inversion, it generates a current that is proportional to the characteristic current. To achieve a PTAT current from the characteristic current of the MOSFET, [18] assumes the mobility temperature parameter is equal to -1 in the given fabrication process. This assumption is difficult to maintain. The mobility temperature parameter, α, is

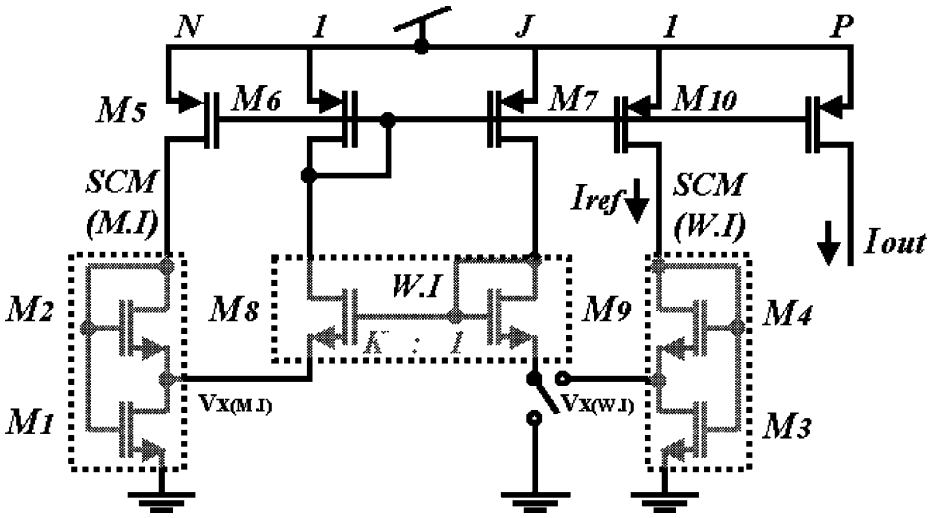


Figure 3.6: Resistorless PTAT current reference proportional to characteristic current in [18] © 2005 IEEE

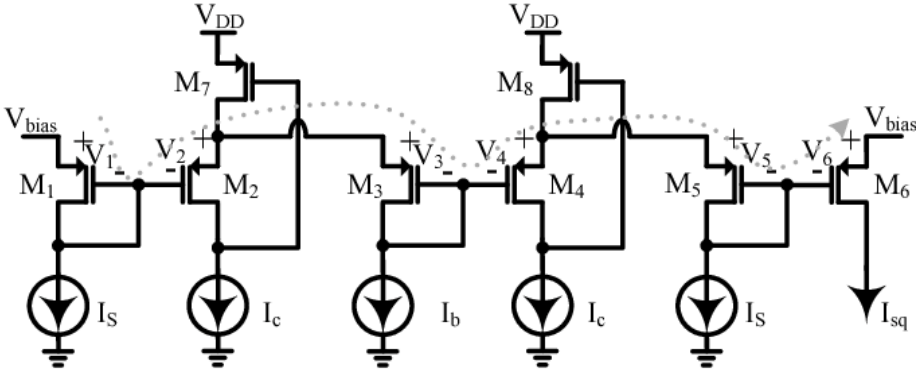


Figure 3.7: Squaring circuit in [19] © 2017 IEEE

typically thought to be equal to -1.5 since the theoretical value of acoustic phonon interaction is proportional to $T^{-3/2}$ [4]. However, other scattering mechanisms modify α, and the mobility temperature parameter can be found to vary with temperature [4, 20]. If $\alpha = -1.5$, [19] uses a squaring circuit to obtain a PTAT current from the characteristic current, with the help from multiple constant current sources, as shown in Fig. 3.7. An additional constant voltage reference is needed for fine tuning the value of the mobility temperature parameter, which adds complexity to the reference circuit. These works show that developing a reference circuit that is dependent on α makes it difficult to develop a general-purpose reference applicable to different fabrication processes, especially when α varies with temperature.

The PTAT voltage source in Fig. 3.2 represents an effective method of to generate a PTAT voltage with low complexity and area. However, it suffers from effects of channel length modulation, similar to the beta-multiplier, that modifies (3.2) to become PVT-dependent:

$$V_r = nV_T \left[ln\Big(\frac{S_2}{S_1}\Big) + ln\Big(\frac{(1+\lambda V_{ds2})}{(1+\lambda V_{ds1})}\Big)\right]. \tag{3.4}$$

The deviation over temperature can be explained when considering a PTAT current flowing through the PTAT voltage source, and evaluating the response of V_{ds}. When temperature increases, V_g decreases to maintain a PTAT current, as it compensates for the approximately exponential relationship between the drain current and temperature. V_r increases with temperature; therefore, V_{ds1} increases while V_{ds2} decreases with temperature, modifying the response of the PTAT voltage source, as shown in Fig. 3.3. The response of V_{ds} is clearly represented in Fig. 3.8, and aligns with (3.4). When V_{ds2} is larger than V_{ds1}, the PTAT voltage shows a positive and increasing derivative, the derivative stops increasing when V_{ds2} approaches V_{ds1}. The derivative of the PTAT voltage

also increases at lower temperatures due to the subthreshold slope factor, since it increases with temperature.

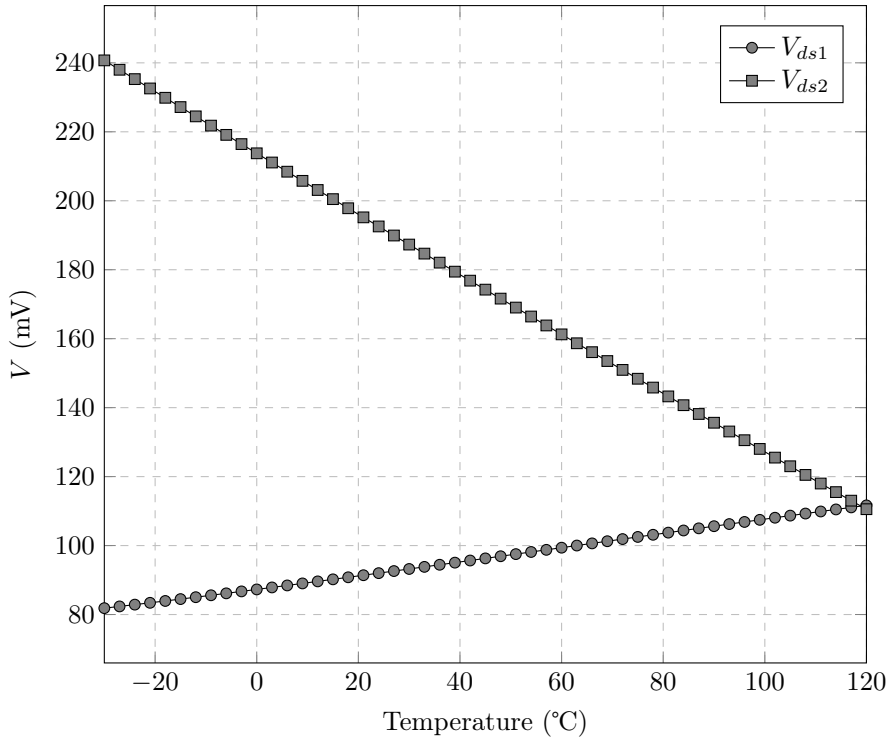


Figure 3.8: V_{ds1} and V_{ds2} of PTAT voltage source

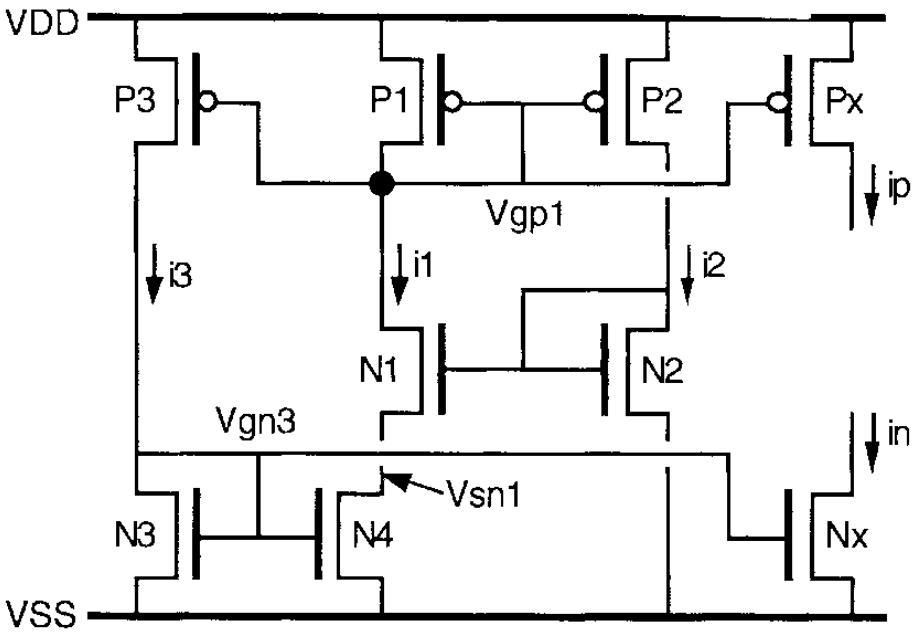


Figure 3.9: Resistorless constant current reference in [21] © 1997 IEEE

A MOSFET operating in the linear region can also be used to replace the resistor in (2.1), instead of directly using the PTAT voltage source in Fig. 3.2. There are a number of methods that can be used to bias this MOSFET in the linear region. [21] demonstrates the use of a MOSFET equivalent resistor operating in the linear region biased using additional transistors P3 and N3, as shown in Fig. 3.9. Although the circuit proposed in [21] produces a constant current reference rather than a PTAT current reference, it

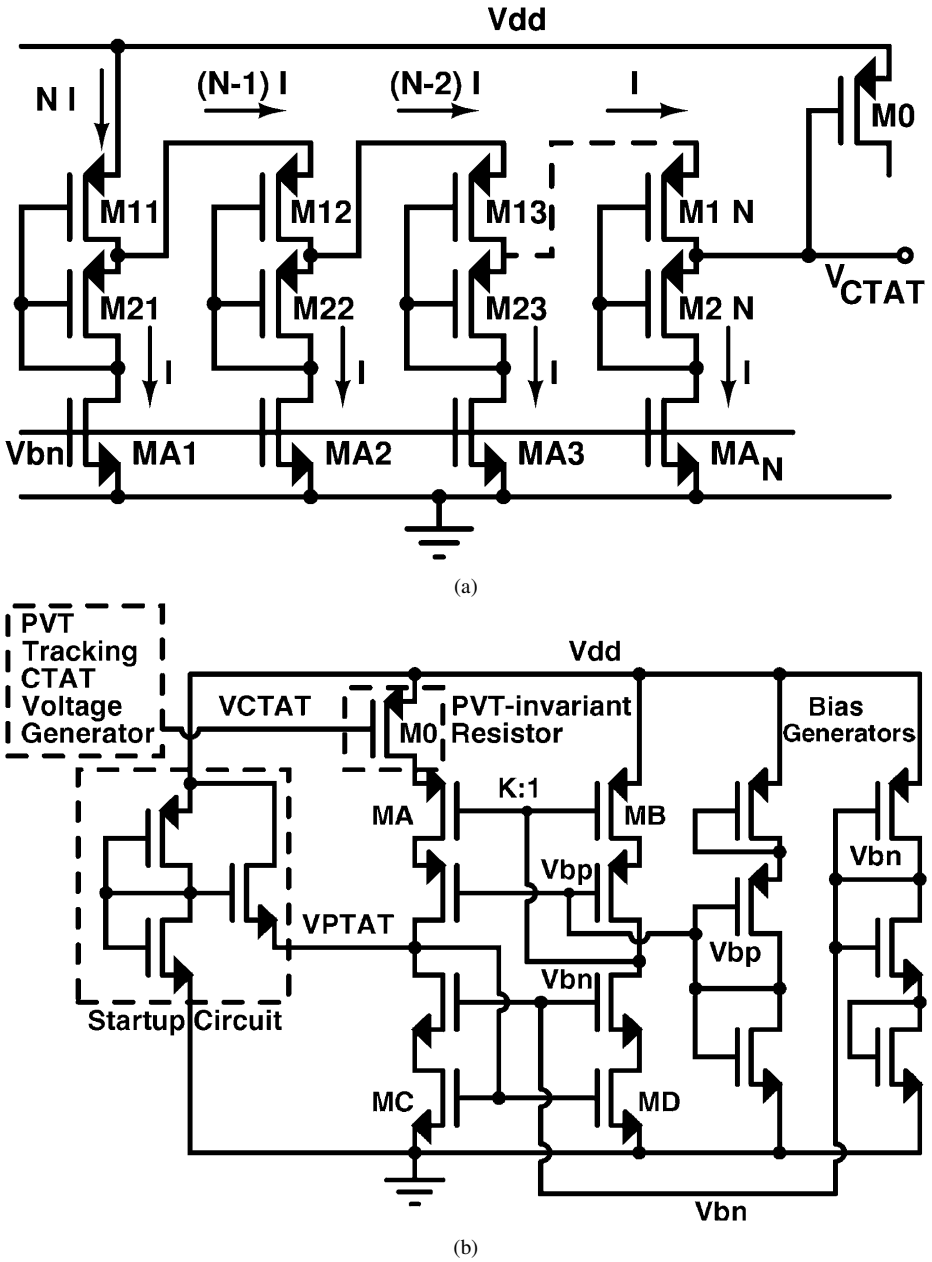


Figure 3.10: Resistorless PTAT current reference with linear MOSFET in [22] © 2013 IEEE

demonstrates the viability of using a MOSFET in the linear region to replace the resistor. The difficult is in generating the correct bias to ensure a PTAT current.

This method is shown in [22]. To provide the bias to a MOSFET in the linear region, [22] makes use of the PTAT voltage source in Fig. 3.2. A PMOS version of the PTAT voltage source is used to generate a CTAT voltage. In this circuit, the voltage source is not directly connected to the source of M2 in the beta-multiplier, but is connected to the gate of the transistor in the linear region. [22] determined that for a MOSFET in the linear region, a CTAT gate voltage is needed to compensate for the effects of temperature. A stack of CTAT voltage sources is used increase the CTAT voltage to supply the proper gate bias. The proposed circuit of [22] is shown in Fig. 3.10.

Another example of a circuit that using a MOSFET in the linear region is demonstrated in [23]. The bias is provided using a switched capacitor resistor scheme as part of a master-slave tuning approach. As mentioned above, a SCR can be used to represent an equivalent resistance. The resistance of a MOSFET in the linear region is matched to the equivalent resistance of the switched capacitor resistor in the master tuning block. The master tuning block consists of two branches: one branch with the replica resistor implemented using a MOSFET, and the other branch with the SCR. The negative feedback applies a bias to the MOSFET to equalizes its resistance to the SCR. The same bias to the MOSFET in the master tuning block is provided to the MOSFET equivalent resistor in the beta-multiplier, thereby matching the resistance to the MOSFET in the master. A couple of low-pass filters are used to suppress the ripples that originate from the SCR mentioned above. This proposed circuit is shown in Fig. 3.11.

The use of switched capacitors or transistors as equivalent resistors can significantly reduce the PVT variations, and the size and precision limitations that would be present with a on-chip resistor. However, the direct replacement of the resistor described in the above does not resolve the issue of channel length modulation in the beta-multiplier.

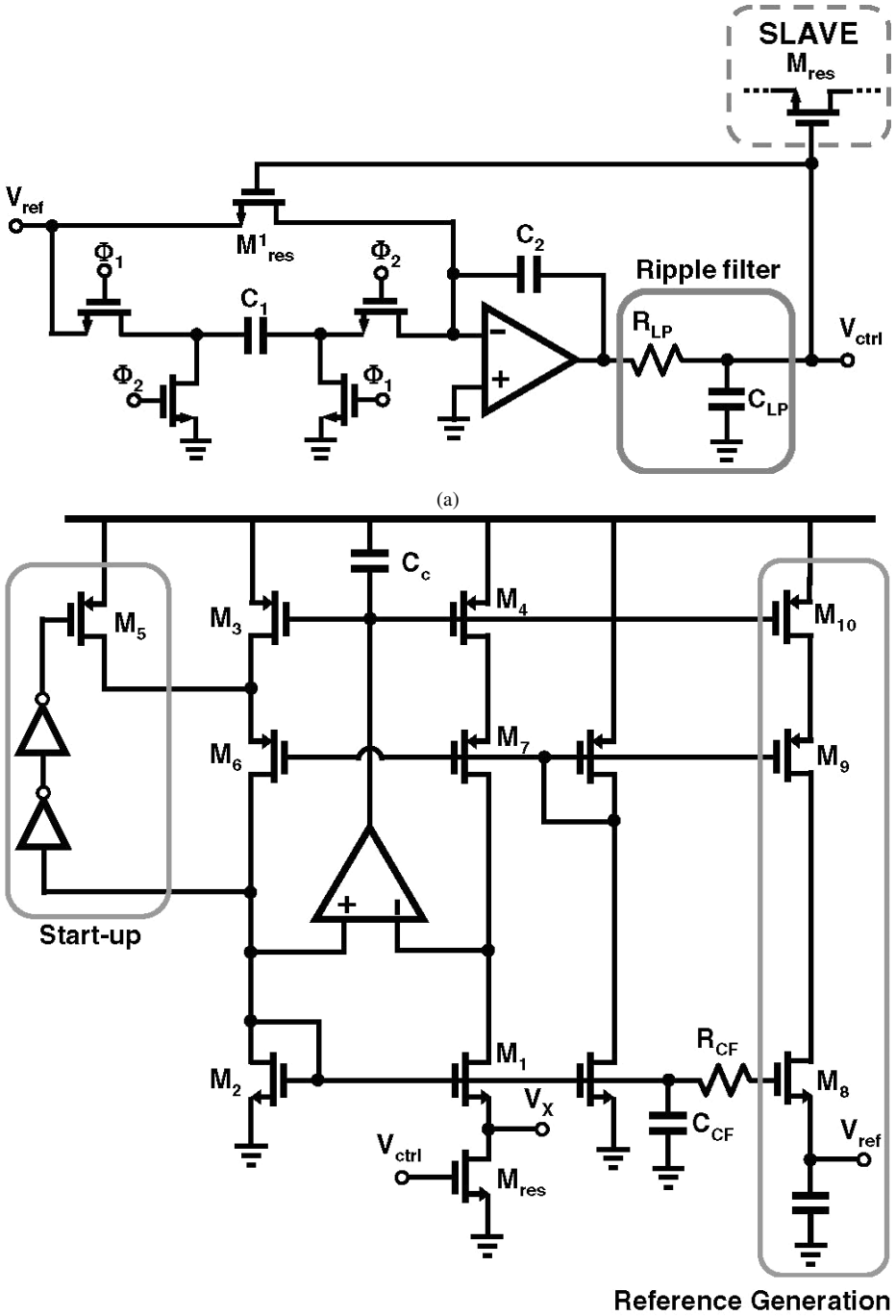


Figure 3.11: Constant g_m reference in [23] (a) master tuning block (b) beta-multiplier with slave variable resistor © 2006 IEEE

3.2 Constant Transconductance Reference with Feedback from Biased Device

The above works described in the previous section are references that have been designed to be independent of the circuit that they intend to bias. They do not monitor the state of the device that the biasing circuit is biasing, but rather try to produce a reliable bias that can be ensured over PVT variations. There are some works monitor the state of the core device that reference circuit is biasing through feedback to produce a bias to keep g_m constant, rather than providing an independent g_m reference.

[24] uses feedback to provide a constant g_m for a g_m controlled oscillator (GCO) by using MOSFETs in the linear region described in Section 2.1. By connecting the output of the GCO to the phase-locked loop (PLL), the frequency of the GCO is matched to the frequency of an external clock signal by adjusting the tunable resistor using feedback through adjusting three different control signals for different levels of adjustment. Each bit of the control signal connects to a MOSFET biased in the linear region. A bank of these linear MOSFET and a resistor replaces the resistor in Fig. 2.1. Fig. 3.12 shows the

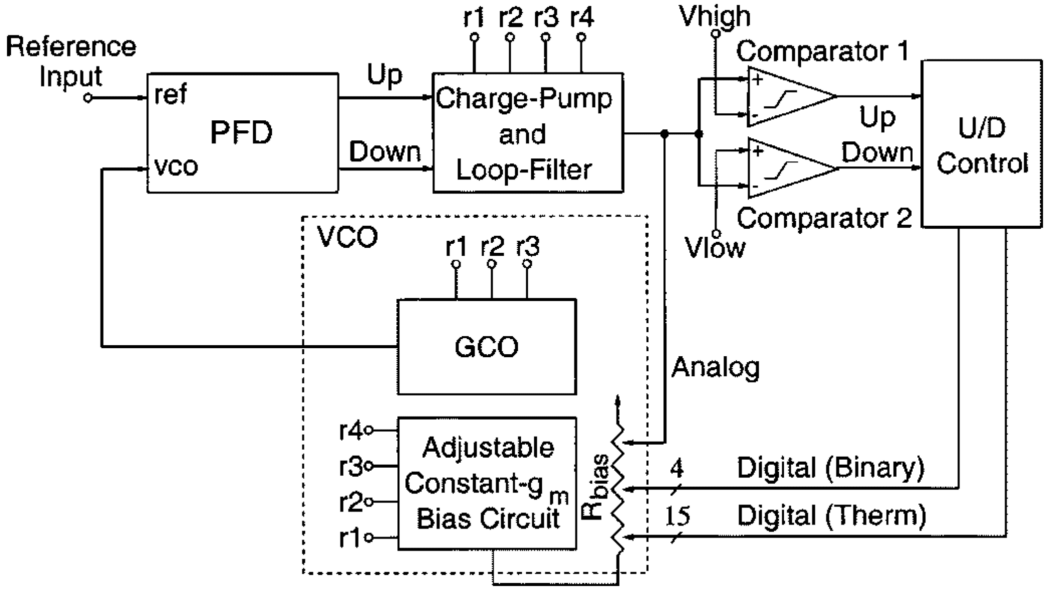


Figure 3.12: Block diagram of constant g_m reference with an adaptive tunable resistor proposed in [24] © 2001 IEEE

block diagram of the constant g_m reference circuit of [24]. While the beta-multiplier in the adjustable constant g_m bias circuit is used to provide the g_m for the GCO the beta-multiplier does not serve the role of creating a constant g_m, but rather the constant g_m is provided by the feedback through the PLL used to trim the resistor, similar to the master slave approach presented in [23]. This tunable resistor is an adaptive method of resistor trimming without physically trimming. Despite incorporating a resistor in the tunable

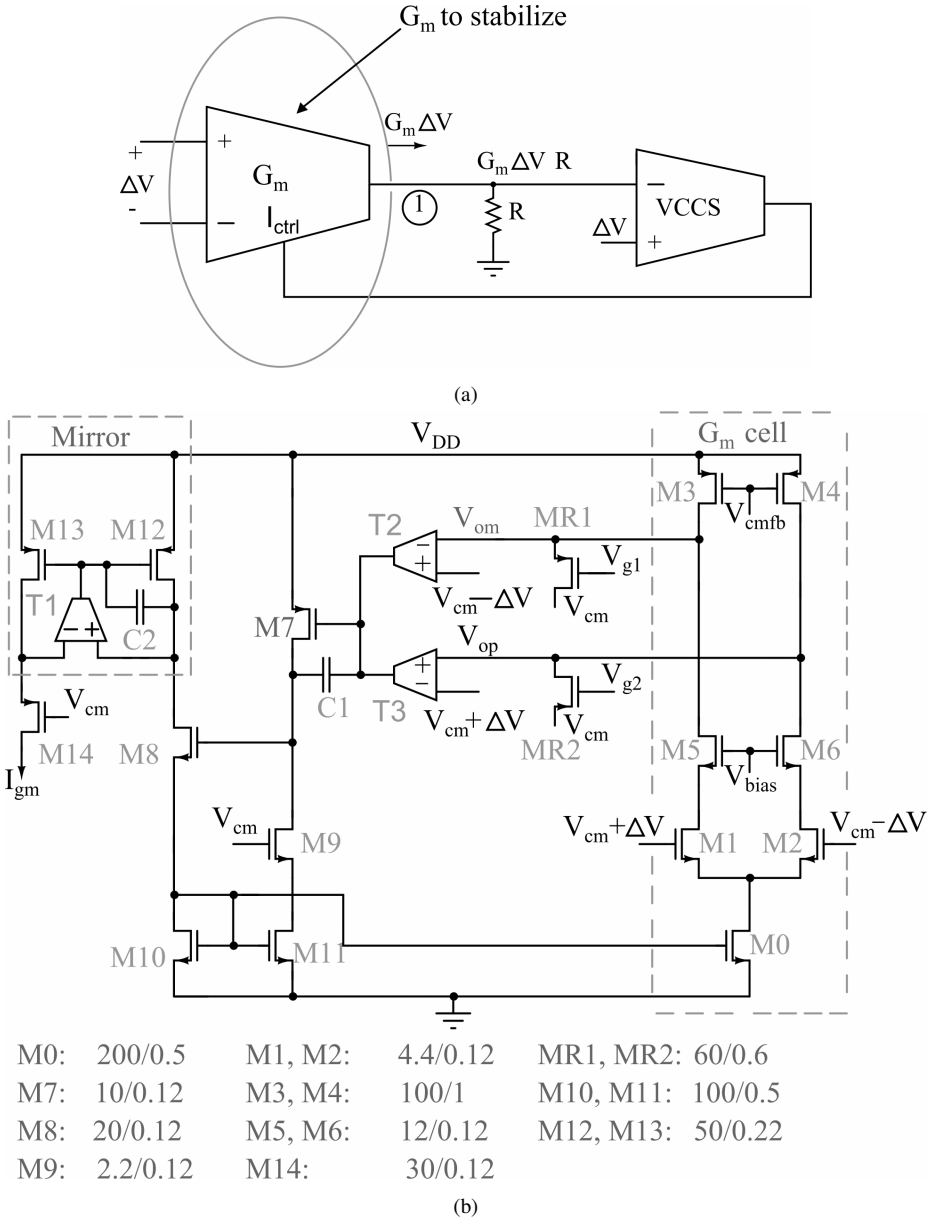


Figure 3.13: Constant g_m reference using feedback with transconductor in [25] (a) block diagram (b) schematic © 2015 IEEE

resistor, the PVT variations of the resistor have a limited effect on g_m since the PVT variations are tuned out through the feedback loop. The insensitivity of g_m depends on how precise adjustments can be made to trim the resistor. This proposed reference still requires an on-chip resistor, which still has disadvantages in the form of area and size of resistance. Since g_m is matched to an input frequency, it has the advantages and disadvantages similar to SCR implementations because it adjusts the g_m to an external clock signal. By this method, the g_m can be changed through an adjustment in frequency, and is not fixed according to the sizing of the transistors or resistors, at the cost of requiring an external clock signal.

[25] presents a constant g_m reference that stabilizes the g_m of a transconductor. Fig 3.13a shows the block diagram representing the operation of the constant g_m reference of [25], and is implemented using the circuit in Fig. 3.13b, where the resistor is replaced with a MOSFET equivalent driven with an op-amp to provide V_{g1} and V_{g2}. The output current of the transconductance, which is proportional to g_m, is converted into a voltage through a resistor. This voltage is compared to an applied voltage using an op-amp, and its output adjusts the bias current of the transconductor through negative feedback. If the g_m of the transconductor is high, this drives the gate of M7 high and lowers the current of M10 and subsequent M0, causing g_m to drop back down. This stabilizes the output voltage of the transconductor to the applied voltage.

In another example, [26] demonstrates a way to use feedback to minimize PVT variations, as shown in Fig. 3.14. In this proposed circuit, feedback is used with a replica circuit, so that the biasing circuit can remain distinct from the device, to stabilize g_m. A constant current source is developed from a PTAT reference circuit with a series of diode-connected MOSFETs to extract the PTAT current leaving behind a constant current, as shown in Fig. 3.14a. Some process compensation is incorporated in this current source through feedback to the substrate. They may be used to control the body of the MOSFET

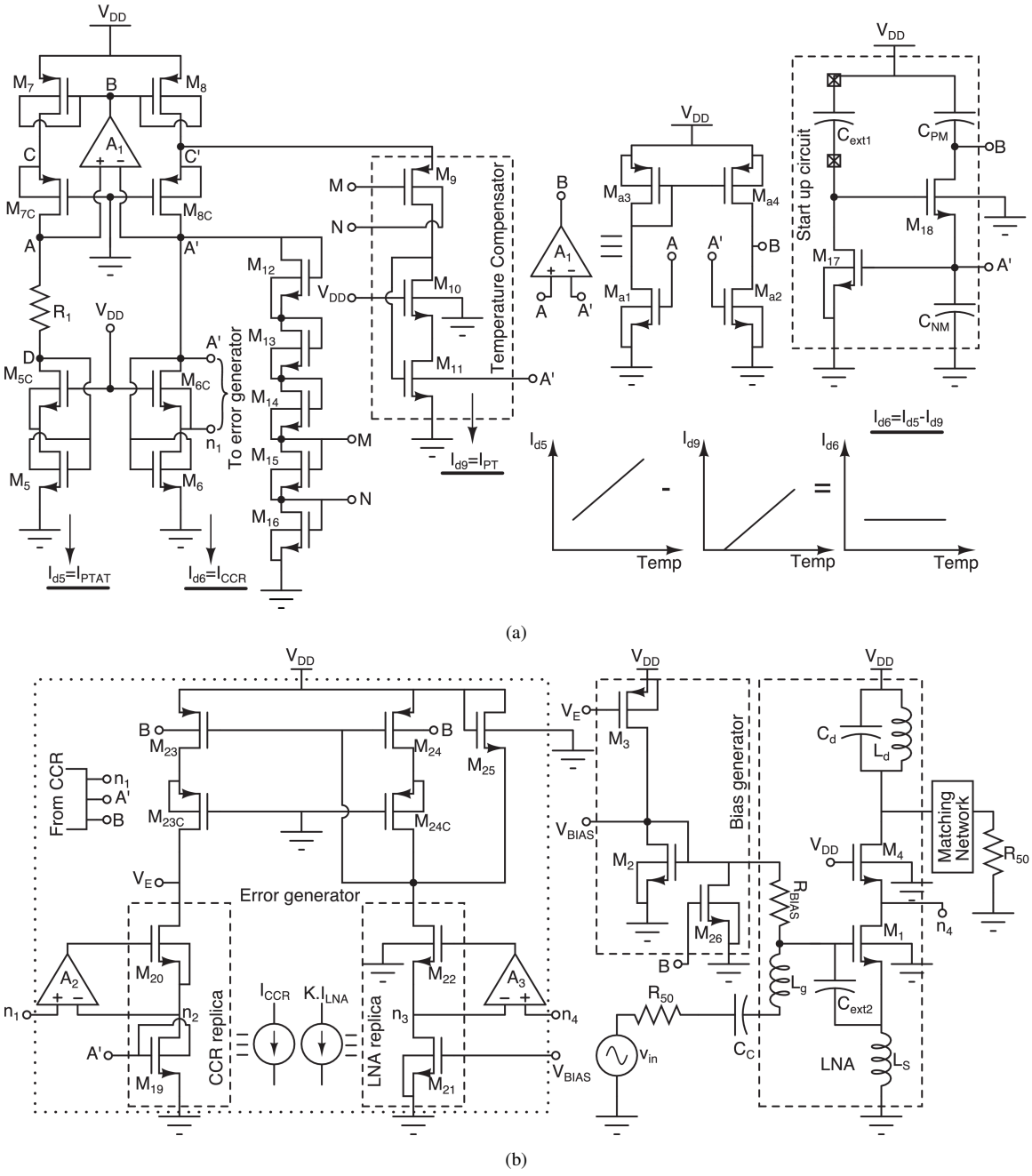


Figure 3.14: Constant g_m reference using feedback with LNA replica in [26] (a) constant current reference (b) circuit of compensated LNA and its biasing scheme © 2015 IEEE

to compensate for changes to the threshold voltage in different process corners. The use of body biasing to adjust has been found to be able to compensation for process calibration by adjusting the substrate bias [27, 28]. This constant current reference is compared to the current in the replica, which generates a CTAT voltage to correct the current in the actual

device. By using a replica circuit, this requires the replica circuit to have the same response as the original under PVT variations, and requires intra-die variations to be minimal. While this works states that feedback with the biased device is necessary to maintain constant g_m in all conditions, the feedback mechanism has the drawback of adding additional complexity and power consumption.

The commonality between all these feedback mechanisms with the biased device is the high complexity. [24] requires an entire PLL to control g_m, while [25] and [26] requires several op-amps and large number of transistor to implement the feedback mechanism. The increase in complexity leads to worse efficiency. It is seen in above works in Section 2.1, that feedback mechanisms with the biased device are not necessary to control voltage or temperature variations. If an accurate PTAT current can be generated, then the feedback mechanism with a replica or the core device will only add unnecessary complexity and power overhead. In the case of process variations, feedback mechanisms with the core device may be useful since the beta-multiplier is not able to control differences in threshold voltage or process variations of the resistor. Overall, to minimize temperature and supply variations, feedback by sensing the device or its replica is not necessary to develop a constant g_m reference.

3.3 Minimizing Channel Length Modulation

The effects of channel length modulation in most reference circuits are conventionally minimized with the use of cascode or feedback drain-regulated current mirrors [6, 7, 16, 17, 22–24, 26, 29–32]. The beta-multiplier of Fig. 2.1 can provide a roughly constant g_m in long channel designs. As the channel is reduced, the output resistance decreases, leading to more pronounced effects of channel length modulation. With the increased significance of channel length modulation, cascode devices are adopted to increase the output resistance to equalize V_{ds}, as demonstrated in one the early papers to develop a PTAT current [33]. This can be applied to the beta-multiplier, as shown in Fig. 3.15.

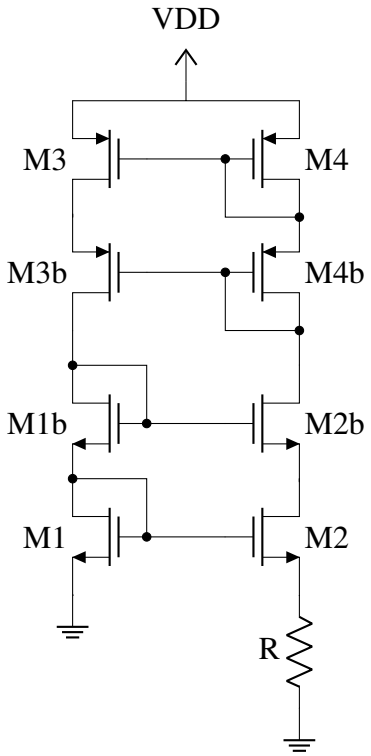
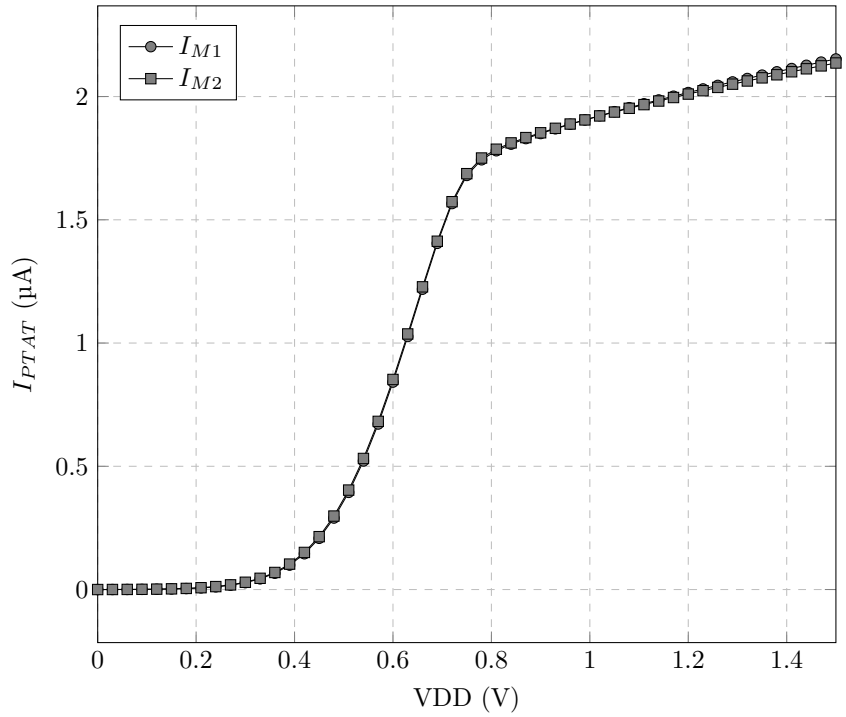


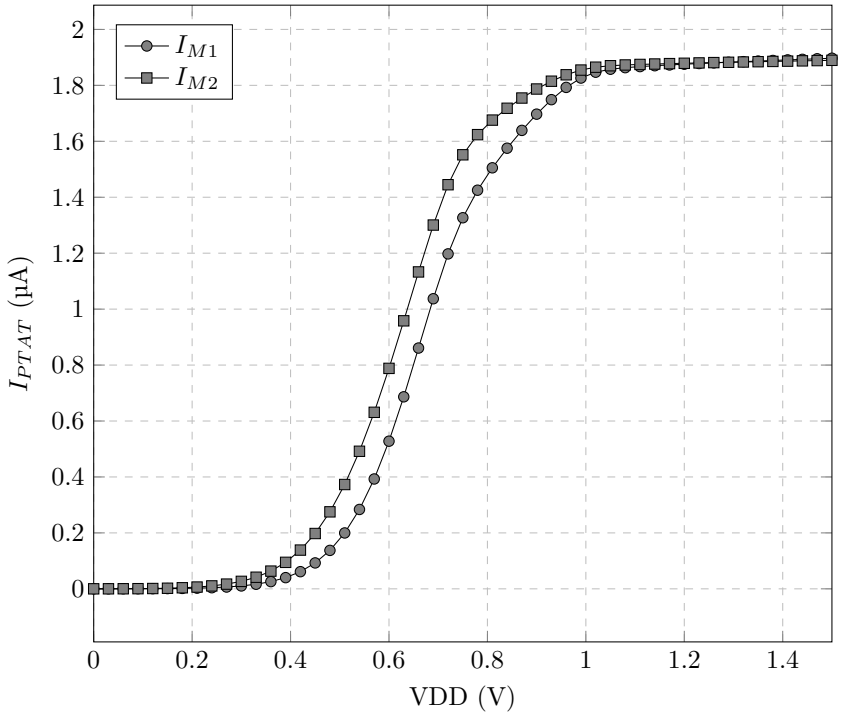
Figure 3.15: Conventional beta-multiplier with cascode current mirrors for both NMOS and PMOS current mirrors [6]

Both current mirrors need to adopt a cascode configuration to effectively reduce the effects of channel length modulation [6]. If only the PMOS current mirror is cascoded, the currents in both branch are made equal. However, the V_{ds} of the NMOS current mirror still varies; therefore, the current still varies with VDD, as shown in Fig. 3.16a. On the other hand, if only the NMOS current mirror is cascoded, the current in each branch will not be equal, and the current will still vary with VDD, albeit with less variation. The result of cascoding both current mirrors reduces variations at the cost of increasing the minimum operating voltage depicted in Fig. 3.16b, which is detrimental for ULP applications.

[29] proposes the use of negative feedback, such as with an op-amp, to regulate the drain voltage of the beta-multiplier, as shown in Fig. 3.17. This forces equal currents in both branches while increasing the output resistance of M1 and M2 without increasing the minimum operating voltage, with its performance depending on the gain and offset voltage of the op-amp. Some circuits use a combination of an op-amp and cascode current mirrors



(a)



(b)

Figure 3.16: I_{PTAT} vs. supply voltage for beta-multiplier with (a) cascode for PMOS current mirror only and (b) cascode for both current mirrors

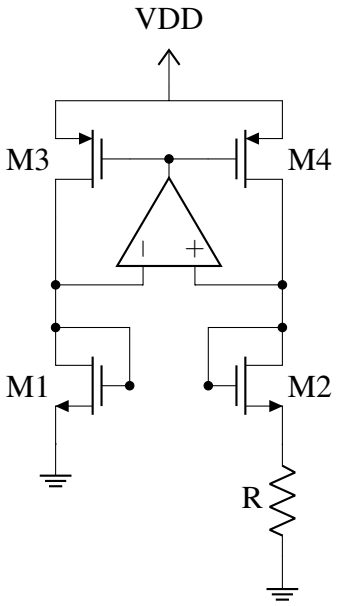


Figure 3.17: Conventional beta-multiplier with feedback drain-regulated current mirror [29]

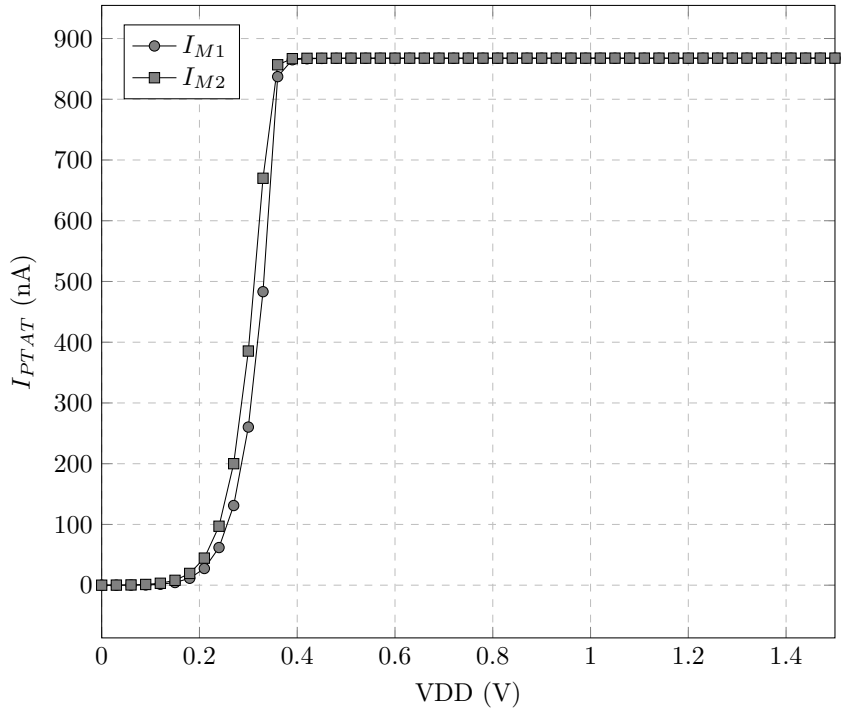
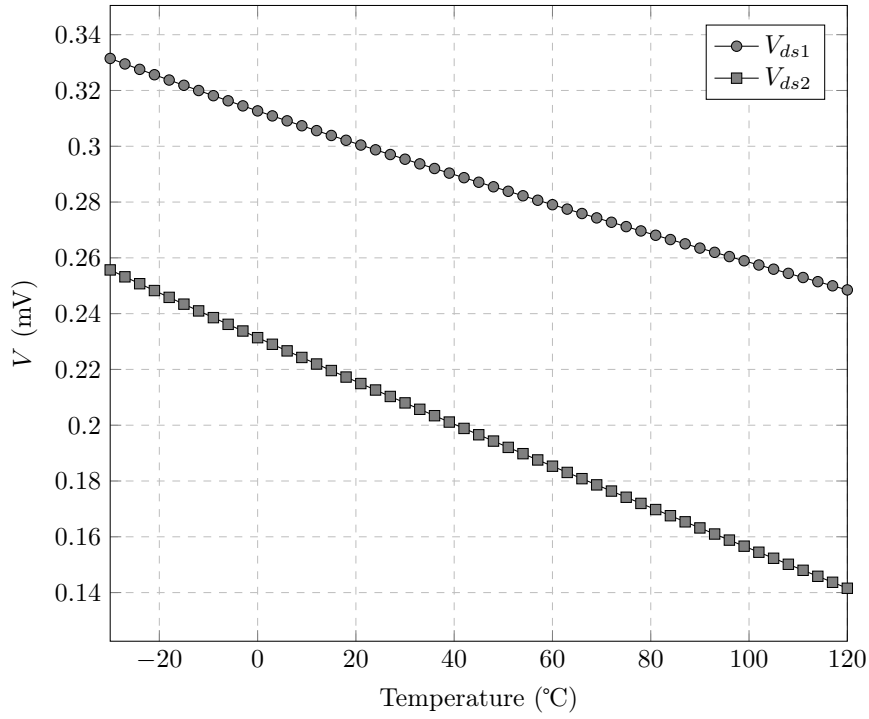
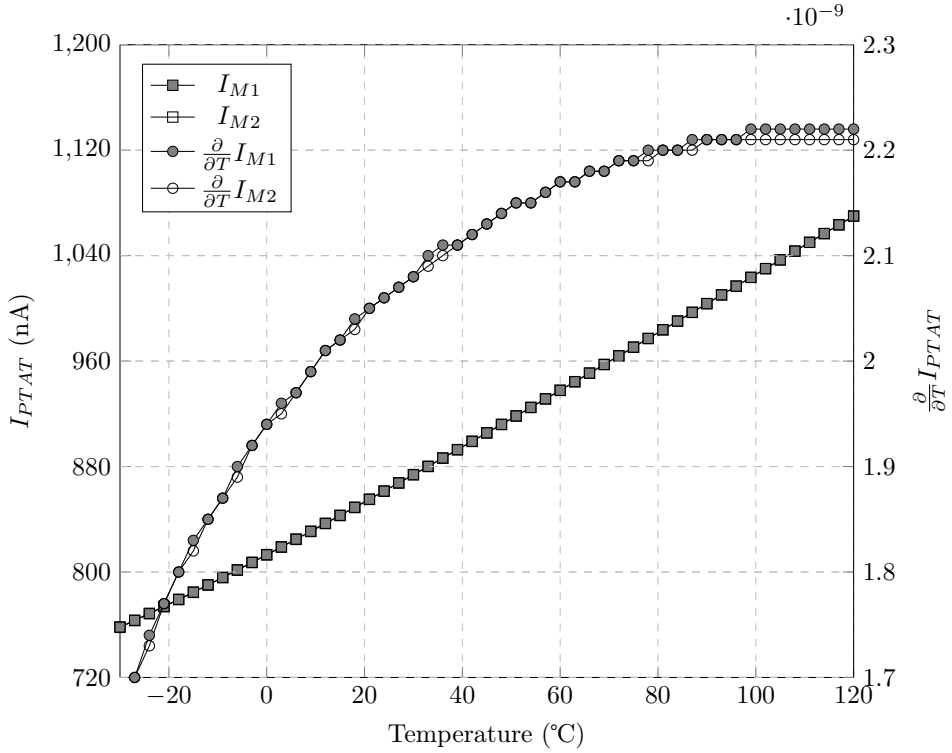


Figure 3.18: I_{PTAT} vs. supply voltage for feedback drain-regulated current mirror

to keep drain voltages equal and to improve external tracking. While regulating the drain voltage is effective for VDD variations, as shown in Fig. 3.18, this is not completely true for temperature variations because of the PTAT voltage drop across the resistor. While



(a)



(b)

Figure 3.19: Feedback drain-regulated beta-multiplier (a) V_{ds} vs. temperature (b) I_{PTAT} vs. temperature

the drain voltages of M1 and M2 are equal, the source voltage are unequal because of the PTAT voltage over the resistor. The source voltage of M2 increases with temperature, which means the V_{ds} of M1 and M2 vary differently over temperature. The increased difference in V_{ds} with temperature is shown in the simulation of V_{ds} in Fig. 3.19a and is reflected in the PTAT current vs. temperature in Fig. 3.19b. The increase in ΔV_{ds} causes the derivative of the PTAT current to fall at higher temperatures.

Further improvements to channel length modulation aim to eliminate the difference in V_{ds}, by creating the difference in V_{gs} at the gate rather than the source of M2 as suggested

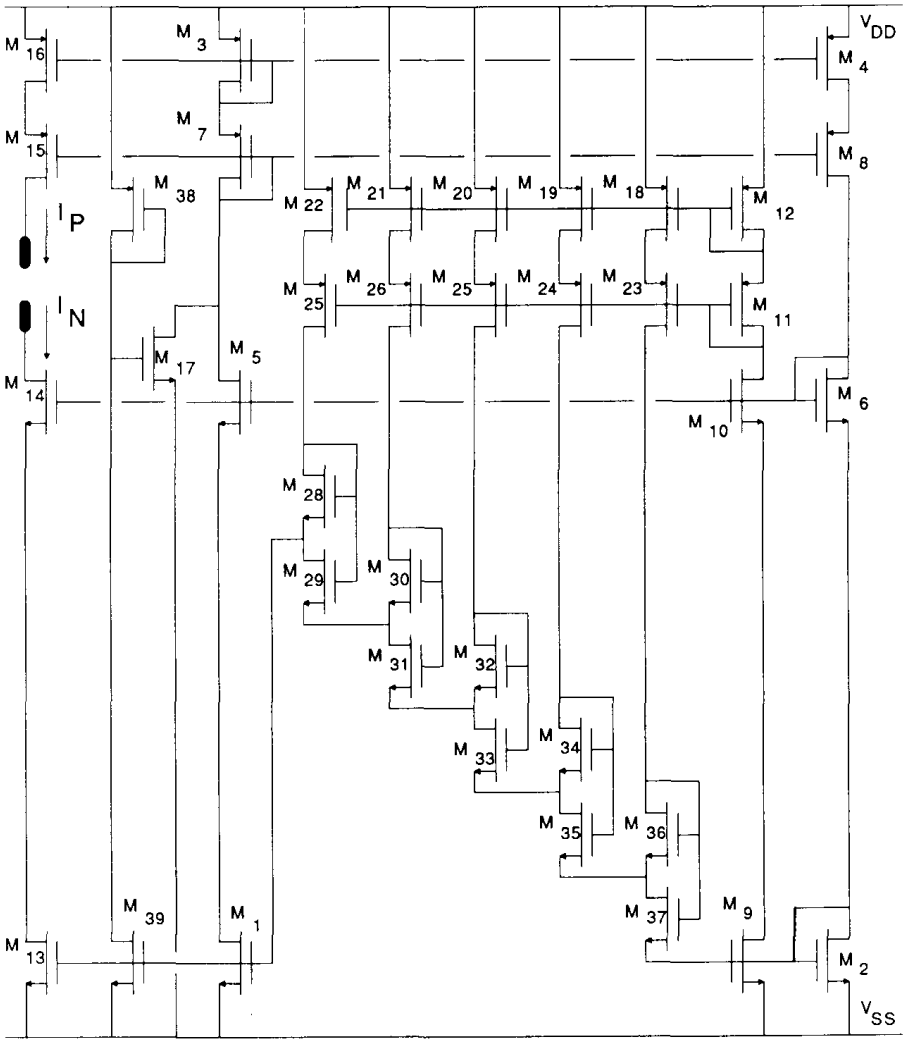


Figure 3.20: Current reference with ΔV_{gs} defined at gate of M2 in [34] © 1988 IEEE

in several papers. [34] develops a PTAT voltage drop between the gate of M1 and M2, by using a long stack of self-cascode transistors to eliminates differences in the source voltage of M1 and M2. This eliminates the inherent difference in V_{ds} between the four transistors of Fig. 2.1, but still requires the use of a cascode current mirror due to the unbalanced impedance in each branch of the beta-multiplier. Eliminating the inherent difference in V_{ds} comes at the expense of introducing effects of channel length modulation in developing the difference in gate voltage using the PTAT voltage source in Fig. 3.2 as mentioned in Section 3.1.

The difference in V_{ds} is addressed in [31] by modelling the beta-multiplier as an analog computer. The generation of the voltage drop (ΔV) across R sets the proper gate bias to be applied to the M2 to create a constant g_m. Instead of using the current in the beta-multiplier to generate ΔV, it is generated by an external current reference to define the gate bias for M2. In this situation, R is no longer in series with M2, therefore V_{ds1} and V_{ds2} can be

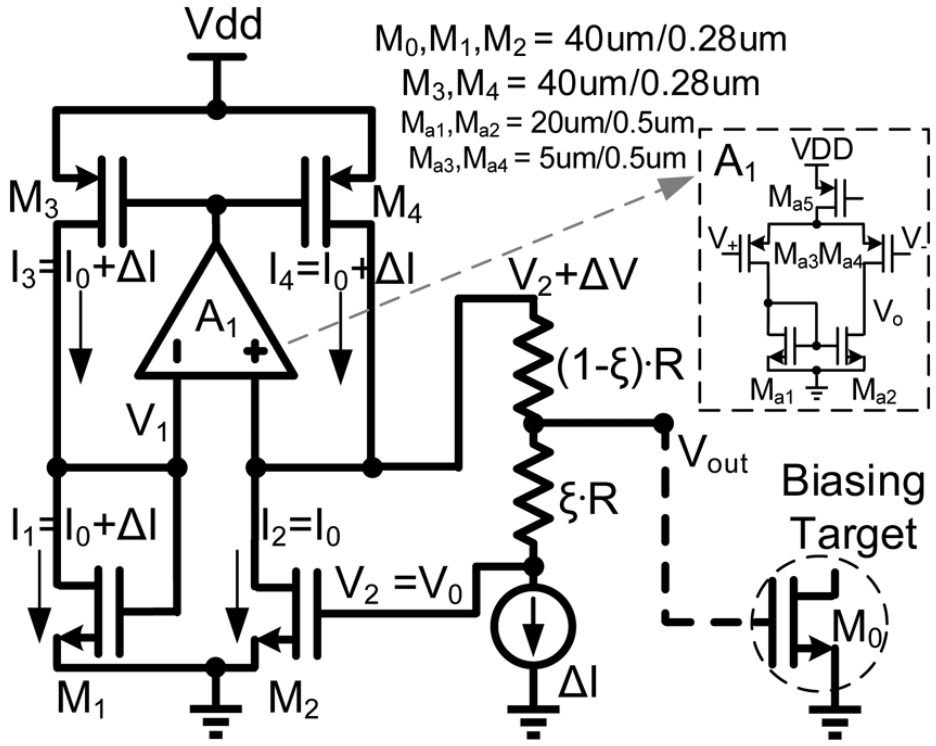


Figure 3.21: Constant g_m reference modelled as an analog computer in [31] © 2014 IEEE

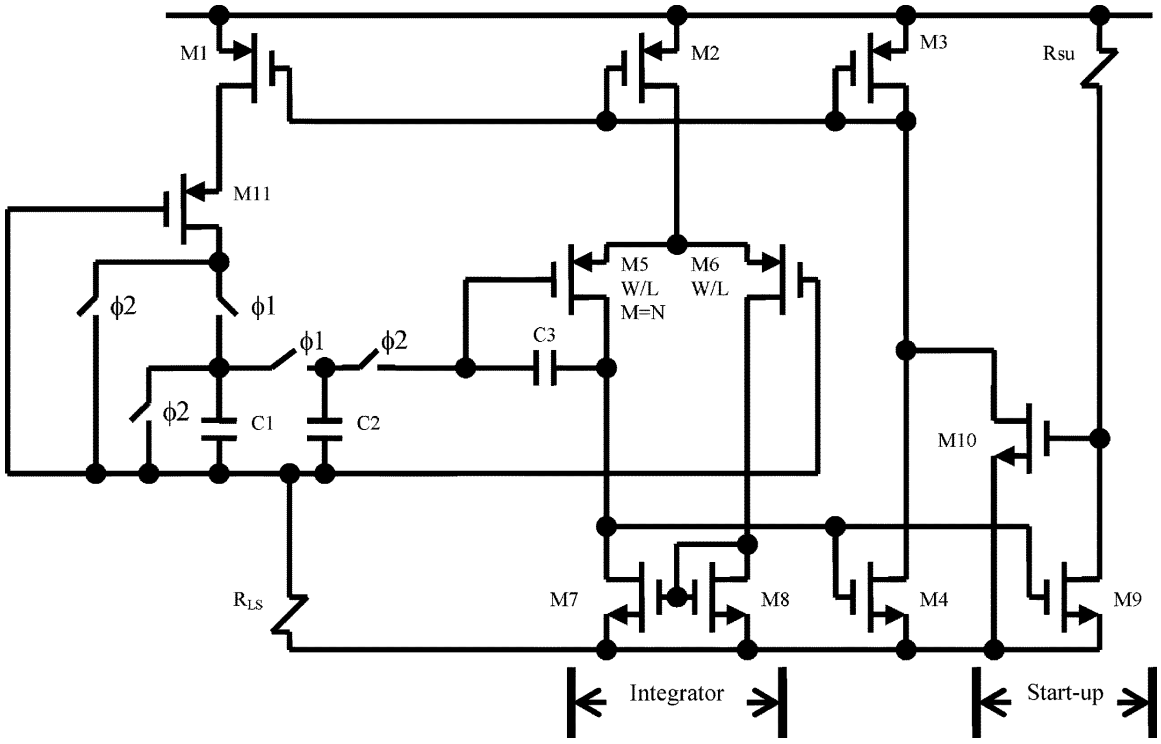


Figure 3.22: Constant g_m switched capacitor current source in [14] © 2007 IEEE

made equal. This eliminates the effects of channel length modulation. However, now g_m is defined by the external current reference and a series of resistors, which both need to be precise. Not to mention, the above works still require the use of cascode or drain-regulated currents mirrors to keep V_{ds} of the current mirrors equal, similar to [34].

Similarly, [14] equalizes V_{ds}, and defines the gate biases externally using switched capacitors. The circuit proposed is different than the beta-multiplier. It uses an op-amp with unequal sized input transistors to create a voltage difference at the gate of the input transistors. This voltage difference is equivalent to the PTAT voltage drop across the resistor in the beta-multiplier, and is proportional to the output reference current. While using switched capacitors in this circuit alleviates the concerns of using resistors, the circuit depends on the availability of a clock signal. For the considerations of a general-purpose constant g_m reference, this becomes an issue since it develops a reliance on an external clock signal, an issue with all switched capacitor resistor schemes.

The effects of V_{ds} are addressed in [30] by connecting two constant gm biasing blocks with opposite polarities to minimize the effects of differences in V_{ds}. Connecting two constant g_m blocks in this manner can reduce the effects of channel length modulation and produce a PTAT current with higher accuracy, but the circuit presented in [30] has a number of drawbacks. First, a differential amplifier and signaling is required. Second, the core device that needs to be biased needs to be part of the biasing circuit [26]. To cancel out the difference in V_{ds}, differential input and outputs are required to connect the gm

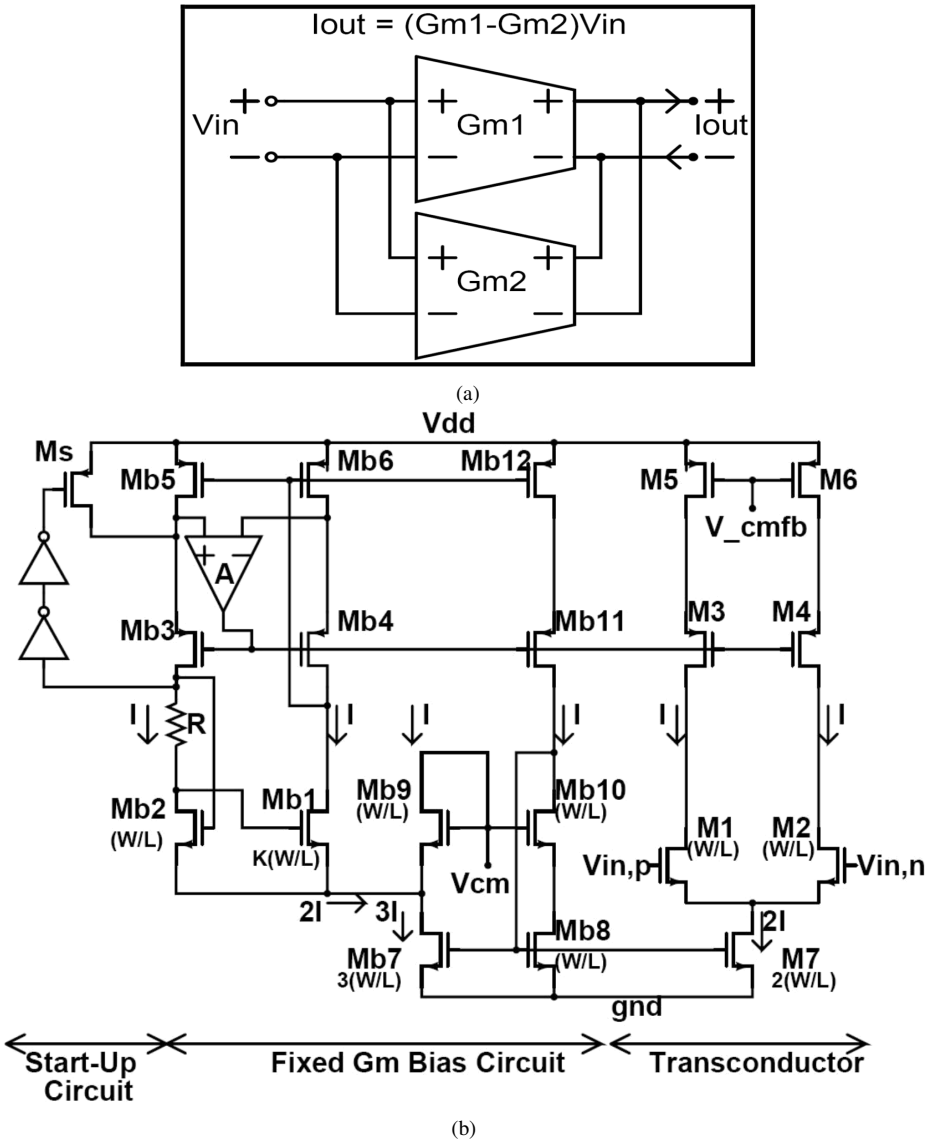


Figure 3.23: Constant g_m reference using differential signaling in [30] (a) block diagram using two g_m biasing blocks to produce constant g_m (b) schematic of a g_m biasing block © 2008 IEEE

blocks in opposite polarities. This requires a differential amplifier to be part of the constant g_m biasing circuit. [30] uses this biasing circuit for a g_m-C filter, where it may be advantageous to have the differential amplifier, transconductor, built into the biasing circuit for optimal area. However, building the biasing circuit as part of the transconductor will limit its application to other circuits, especially with single-ended circuits such as LNAs and PAs. Keeping the biasing circuit distinct from the core device will also minimize the effects of the biasing circuit on input and output matching characteristics that are required in RF applications. This will allow for existing circuits to remain constant, with only the biasing circuit needed to be modified to keep subthreshold circuits PVT insensitive.

Furthermore, in this circuit, [30] suggests that the source voltages of the input transistor in the transconductor and their equivalent transistor represented as M1 in Fig. 2.1 must be equal to minimize the body effect. When the transconductor is controlled by a tail current using a MOSFET, this sets the source voltage of the input transistors of the transconductor to be above ground. To have the input transistor of the transconductor and the M1 equivalent of that circuit at the same source voltage, the circuit in [30] uses a replica circuit in each g_m block. This adds further complexity to the design.

3.4 Summary

In this chapter, a literature review was done on works and circuits that tries to minimize the PVT dependence of the conventional g_m reference circuit. Chapter 2 concluded that the PVT variations of the resistor and the effects of channel length modulation can be reduced. To mitigate the PVT variations of the resistors, existing works that develop resistorless g_m references are detailed. These works replace the resistor with a MOSFET or SCR equivalent, where MOSFET equivalent resistors are done by creating a PTAT voltage, or by placing a MOSFET in the linear region. A direct replacement of the resistor reduces the PVT variations of the resistor, but does not reduce the effects of channel length modulation.

To control the effects of channel length modulation, most works cascode the current mirrors or use an op-amp to regulate the drain voltage. Some existing works further reduce the effects of channel length modulation by equalizing V_{ds} of M1 and M2, or by cancelling out the effects of channel length modulation by connecting two g_m blocks with opposite polarities. These methods require an external reference and precise components while still requiring the use of cascode and op-amps or have limited applications. Some g_m references opt to use negative feedback with the biased or core device to control PVT variations, but these references tend to be highly complexity, which reduces its efficiency. There is a need to develop a reliable, general-purpose g_m reference circuit that can minimize the effects of channel length modulation to produce a more constant g_m over PVT variations. This will be the focus of Chapter 4.

Chapter 4

Proposed Constant Transconductance Reference

4.1 Technique of Proposed Constant Transconductance Reference

The proposed circuit utilizes two independent g_m references with different K values but are otherwise identical, as shown in Fig. 4.1, by taking the difference between the currents produced by the two beta-multipliers, less variation over voltage and temperature can be achieved. The principle of the circuit is that second-order effects that affect both

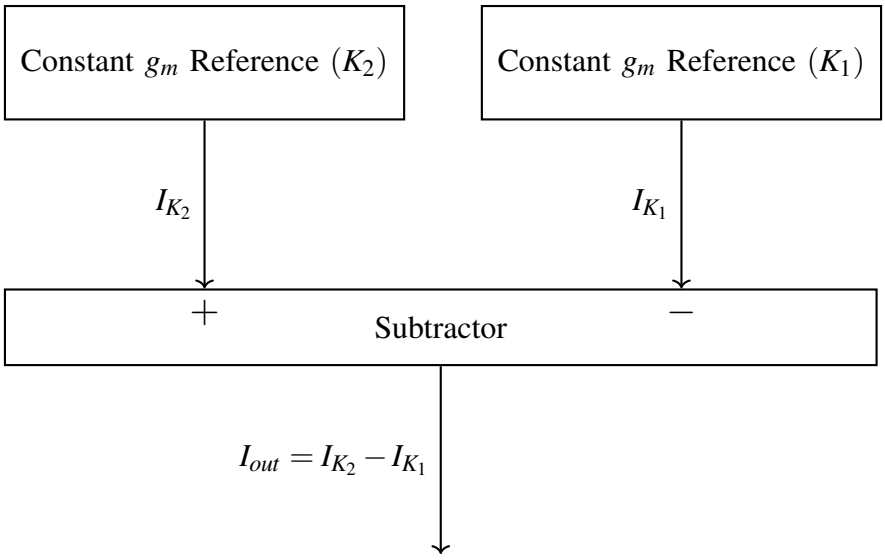


Figure 4.1: Block diagram of proposed circuit

beta-multipliers will cancel out, not only reducing the variations with voltage and temperature, but also with process. The circuit was developed with the intention that it can work with conventional biasing techniques, by replacing existing conventional reference circuits, without influencing the characteristics of the device that it is biasing. The proposed g_m reference is a standalone circuit, without requiring external current references, clock signals and op-amps. By subtracting the currents from the two beta-multipliers with K values of K_1 and K_2, where $K_2 > K_1$, we can ideally cancel the effects of channel length modulation, resulting in the following stable current, similar to the derivation presented in [30]:

$$I = \frac{nV_T ln\left(\frac{K_2}{K_1}\right)}{R}. \tag{4.1}$$

This gives the following g_m:

$$g_m = \frac{ln\left(\frac{K_2}{K_1}\right)}{R}. \tag{4.2}$$

These equations are formed under the assumption that the V_{ds} of the MOSFETs across both beta-multipliers are identical, which is not true due to different currents in each beta-multiplier with different K values. The proposed g_m reference does not attempt to equalize V_{ds} across two beta-multipliers, but rather reduces the effects of channel length modulation by making the variations in V_{ds} of the same transistor across two beta-multipliers evolve similarly over VDD and temperature. The general equation, considering all the effects of V_{ds} is as follows:

$$I_{out} = \frac{nV_T}{R}\left[ln\left(\frac{K_2}{K_1}\right) + ln\left(\frac{(1+\lambda V_{ds2r})}{(1+\lambda V_{ds2})}\frac{(1+\lambda V_{ds1})}{(1+\lambda V_{ds1r})}\right) + ln\left(\frac{(1+\lambda |V_{ds3r}|)}{(1+\lambda |V_{ds3}|)}\frac{(1+\lambda |V_{ds4r}|)}{(1+\lambda |V_{ds4}|)}\right)\right]. \tag{4.3}$$

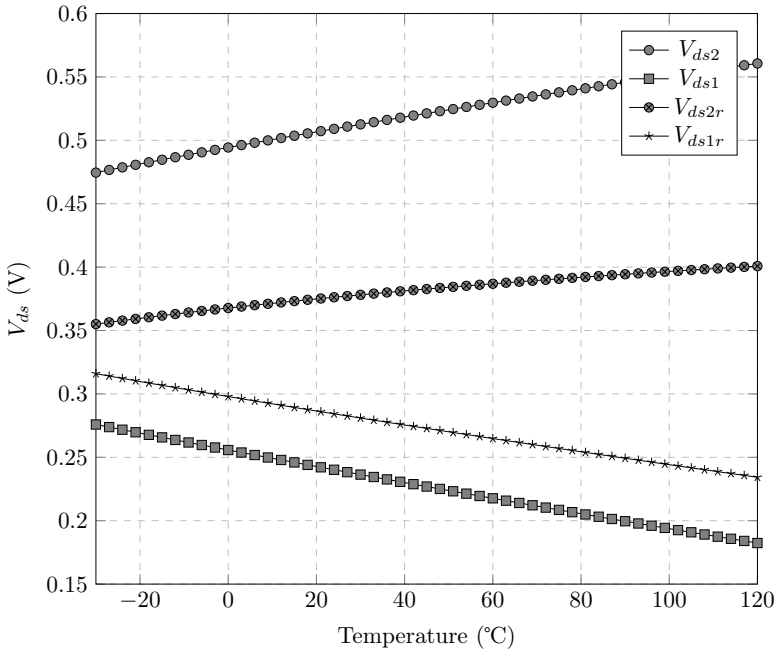
Variations of V_{ds} across VDD can be evaluated in part by determining the output impedance of the MOSFETs in the beta-multiplier. The output impedance of the diode-connected MOSFETs, M1 and M4, are equal to $1/g_m$, while the output impedance of M3 is r_o. Since M2 is a source-degenerated MOSFET, it has the equivalent output resistance of $r_o + g_m r_o R + R$. M2 and M3 are high impedance; therefore, as VDD increases the majority of VDD will fall across M2 and M3. Since M2 and M3 are diode-connected, their V_{ds} cannot change freely since they determine the current flow, and this limits changes to V_{ds} to M2 and M3. If K value of the beta-multiplier increases, the V_{ds} of M1 and M4 also increases to support the increased current, while the V_{ds} of M2 and M3 will decrease correspondingly.

Variations of V_{ds} across temperature are as described in Chapter 2. The V_{ds} of M1 and M4 will decrease as a result of the third term in (2.12), while M2 and M3 will increase with temperature correspondingly. For variations across different K values, (2.12) can be modified to account for variations in K, where C' is equivalent to C of (2.12) with K extracted out:

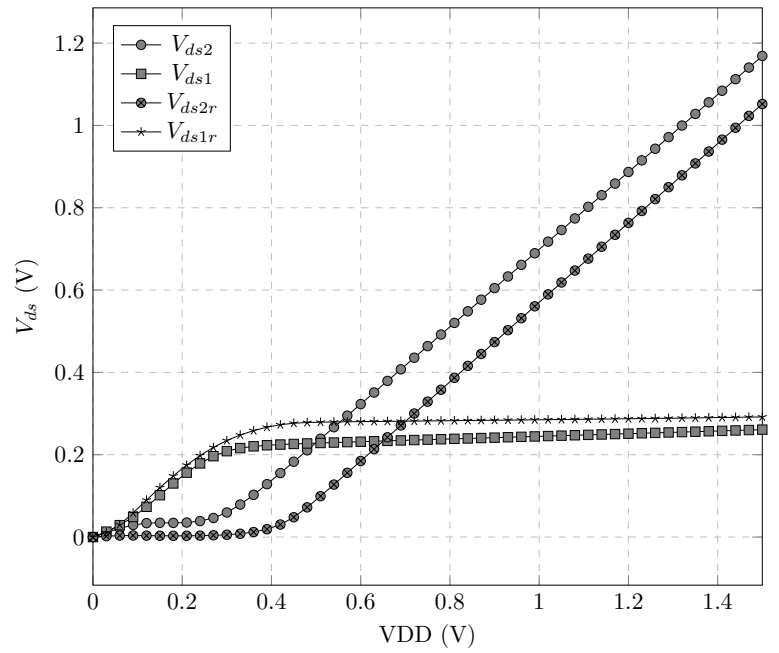
$$\begin{aligned} V_{ds1} &= nV_T ln\Big(\frac{C' ln(K)}{T^{\alpha+1}}\Big) + V_{th}(T_0) - A(T - T_0), \\ &= V_{th}(T_0) + AT_0 + \Big(\frac{nk_B ln(C' ln(K))}{q} - A\Big)T - \frac{nk_B(\alpha+1)}{q} T ln(T). \end{aligned} \tag{4.4}$$

This suggests that larger K values increases the third term of (4.4), making it less negative, which results in V_{ds} of M1 and M4 to increase with K, and corresponds to V_{ds} of M2 and M3 decreasing with K. The above analysis across VDD and temperature is confirmed by the simulation results in Fig. 4.2, where the number in the subscript indicates the corresponding MOSFET in Fig. 2.1 and the subscript r represents the beta-multiplier designed with a K value of K_2. The main significance of the above analysis is that while changing the K value will increase or decrease the V_{ds} of the transistors, it does not

significantly affect their relationship to VDD and temperature variations. Within a single beta-multiplier, the V_{ds} of the PMOS and NMOS transistor pairs diverge, causing the



(a)



(b)

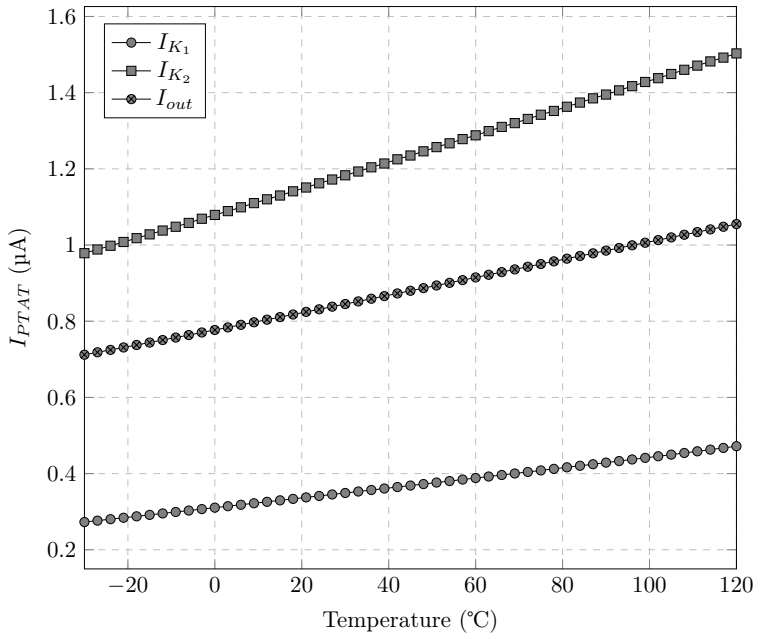
Figure 4.2: Variation of V_{ds} of proposed reference vs. (a) temperature and (b) supply voltage for $K_1 = 2$ and $K_2 = 18$

effects of channel length modulation to appear. When comparing the V_{ds} of the same transistor across two beta-multipliers with different K values, they are found in both the analysis and Fig. 4.2 to vary under a similar relationship across VDD and temperature. Consequently, the logarithmic terms of (4.3) are relatively constant, and this reduces the effects of channel length modulation. While Fig. 4.2b only shows variations for V_{ds1} and V_{ds2} across both beta-multipliers, this result is also applicable for V_{ds3} and V_{ds4}.

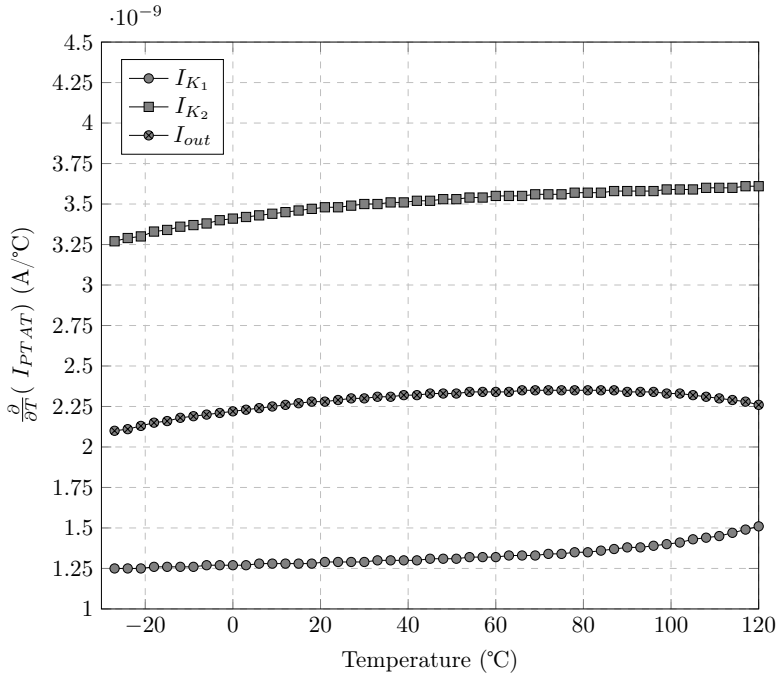
Fig. 4.3 and 4.4 demonstrate the improvements of the PTAT current dependence to temperature and VDD using the proposed constant g_m reference circuit that implements a current subtraction. The currents through the two beta-multipliers, used to generate the bias current, shown as I_{K_1} and I_{K_2}, show significant effects of channel length modulation. By taking the difference between the currents in the two beta-multiplier, a relatively flat response over VDD is obtained. I_{out}, the output current of the proposed reference, can be found to change by 4.2%/V, from 0.5 to 1.5 V. Most of the variation is attributed to operating from 0.5 to 0.6 V. If the voltage range is redefined between 0.6 to 1.5 V, there is a supply variation of 2.07%/V. This result is reflected by taking the derivative in Fig. 4.4b. In comparison, I_{K_1} and I_{K_2} changes by 99.1% and 25.4% over 0.5 to 1.5 V range, respectively.

As for the dependence of I_{out} to temperature, by taking the difference between I_{K_1} and I_{K_2}, a PTAT current vs. temperature with less variations due to channel length modulation is obtained. The divergence of V_{ds} of the PMOS and MMOS transistor pairs in (2.11) causes the currents of each of the beta-multipliers to increase more with temperature, as shown in its derivative. By taking the difference in current, the slope of I_{out} is reduced, and therefore, the effects of channel length modulation is minimized. I_{out} still exhibits a positive and increasing derivative since the subthreshold slope factor, n, increases with temperature.

Process variations are also likewise reduced as process variations affect both of the beta-multipliers similarly, therefore the difference between the two beta-multipliers will



(a)

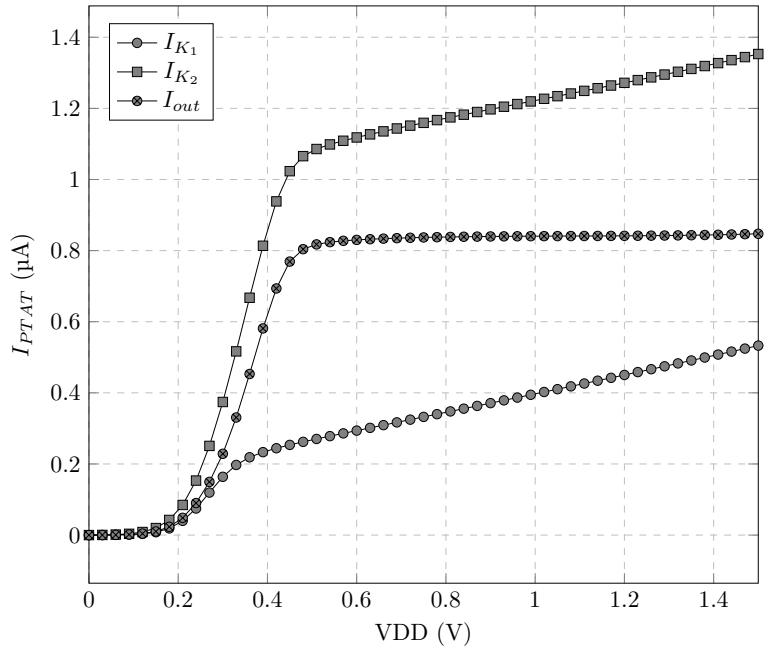


(b)

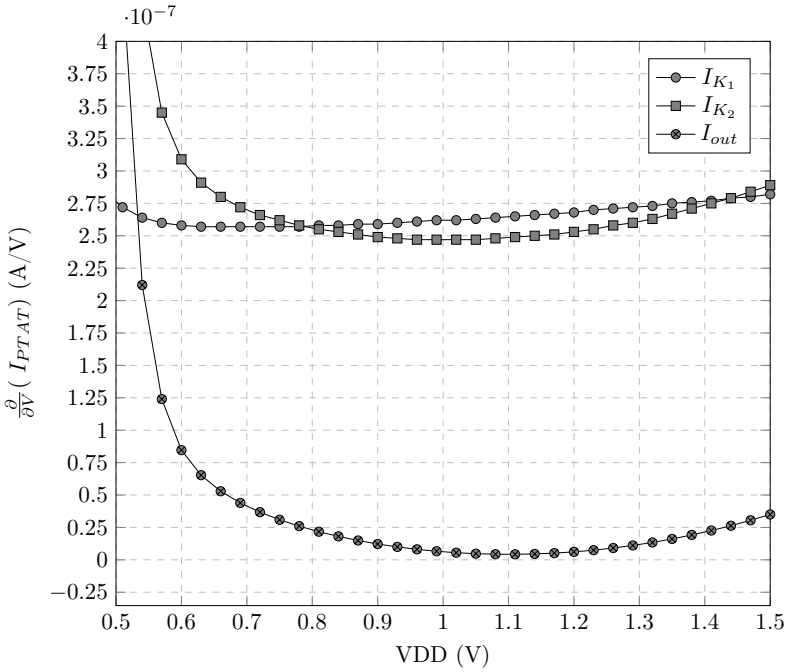
Figure 4.3: I_{PTAT} vs. temperature and its derivative

be relatively constant through process variations. Fig. 4.5 demonstrates process variations of the beta-multiplier without including process variations of the resistor. It can be seen that the grouping of the curves over the process corners is tighter for the output current of

the proposed constant g_m reference compared to the curves for the two beta-multipliers that form the proposed circuit. Closer analysis reveals that at nominal temperature, I_{out}

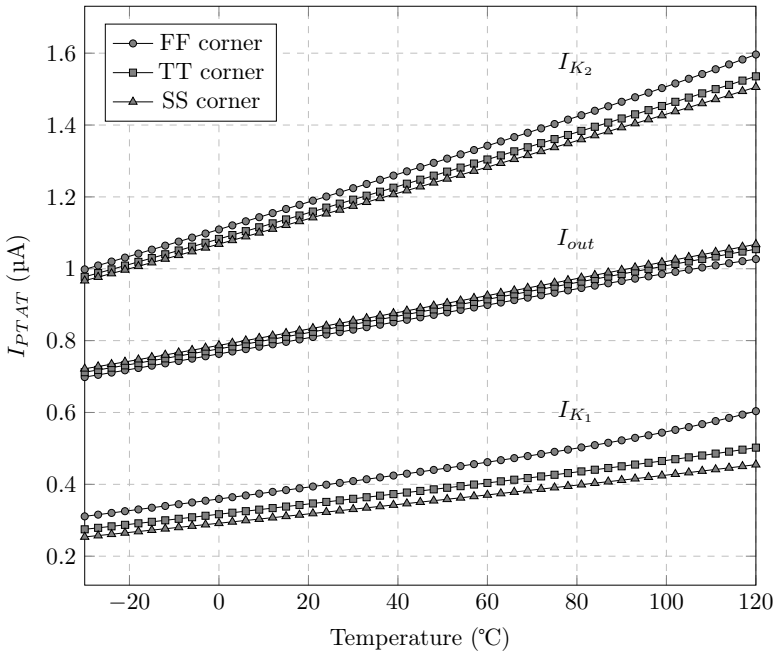


(a)

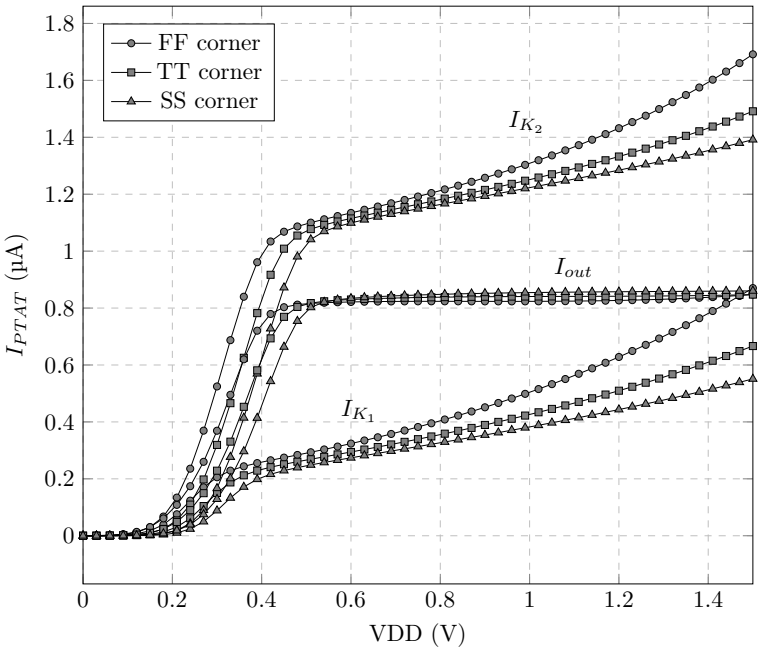


(b)

Figure 4.4: I_{PTAT} vs. supply voltage and its derivative



(a)



(b)

Figure 4.5: I_{PTAT} over process corners without resistor variation vs. (a) supply voltage and (b) temperature

varies by ±1.47% over the process corners, while I_{K_1} and I_{K_2} varies by ±10.57% and ±2.05% over the process corners, respectively. At 0.8 V supply voltage, I_{out} varies by ±1.49% over the process corners, while I_{K_1} and I_{K_2} varies by ±10.7% and ±2.1% over the

process corners, respectively. At higher temperatures and voltages, the current of the two beta-multipliers show greater deviations, while deviations of I_{out} are kept relatively constant across temperature and voltage.

4.2 Design of Proposed Constant Transconductance Reference

4.2.1 Composite/Self Cascode Transistor

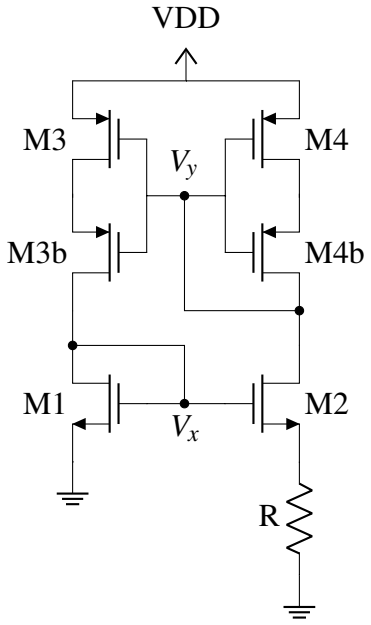


Figure 4.6: Beta-multiplier with self-cascode PMOS current mirror

In a short channel transistor design, the effects of channel length modulation can severely affect the tracking accuracy of current mirrors. The accuracy of the current mirror is critical in the beta-multiplier since the PTAT current is derived, in this case, under the assumption that the current is equal in each branch of the beta-multiplier. The PMOS current mirror is used to ensure that this assumption is maintained. Nevertheless, simple current mirrors cannot adequately maintain equal current in the two branches because of the low output impedance present in short channel MOSFETs. Using a cascode configuration or an op-amp to equalize the currents in both branches may not be desirable due to a higher minimum required voltage and lower power efficiency, respectively.

Therefore, those configurations are excluded to prevent further power consumption in the design. Similarly, a low voltage cascode configuration is excluded to prevent further power consumption required to generate the bias for the cascode transistors.

A configuration that can be employed in this situation is the self-cascode transistor, otherwise called a composite transistor, where two transistors are connected in series with a shared gate connection. The use of the self-cascode transistor was first demonstrated in [35]. By sizing the top transistor to be m times wider than the bottom transistor, a high output impedance can be obtained, while enabling low voltage operation. The larger the m value, the higher the output impedance that can be obtained. The self-cascode transistor behaves as a single long-channel transistor, while using short-channel transistors.

Originally, the self-cascode transistor was demonstrated to work in superthreshold by biasing the top transistor into saturation, while the bottom transistor can operate either in the saturation or linear region [35–38]. However, it has been shown to work in the subthreshold region as well [39–42]. Therefore this configuration works in applications with low current draw. This configuration is adopted for the top PMOS current mirror to improve current tracking in the beta-multiplier, as shown in Fig. 4.6.

4.2.2 PTAT Current Subtractor

The outputs of two beta-multipliers with different K values, but are otherwise identical, can be subtracted to reduce effects of channel length modulation. To facilitate the subtraction operation, current mirrors can be used to perform the subtraction [43]. The two PTAT current will be mirrored by the top PMOS current mirror. An additional current mirror is used to mirror one of the PTAT currents into the same branch of the other PTAT current. This allows one of the beta-multiplier to source the current and the other to sink the current. The difference between the two PTAT currents will be passed through a load transistor, Mbias, that can be used to bias the core device in similar fashion to conventional biasing methods. Depending on the configuration of the subtractor, whether

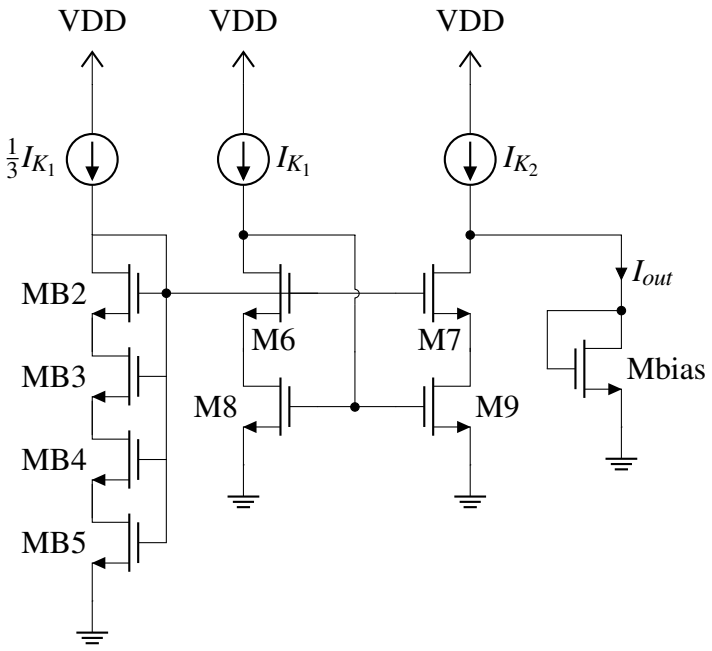


Figure 4.7: PTAT current subtractor

the beta-multiplier with the larger K value is used to source or sink the current, the load transistor can either be a PMOS or NMOS transistor. In this design, the difference in current is passed through an NMOS transistor.

The current mirror for the subtraction operation is implemented using a low voltage cascode current mirror due to the low voltage requirement and the high output impedance associated with the cascode design. The bias voltage for the top transistors in the low voltage cascode is provided by using a fraction of the PTAT current provided by the beta-multiplier with the lower K value, by sizing the PMOS transistors to be $1/3$ of the original. A series of four transistors with all their gates connected is used to set the bias voltage. The resulting PTAT current subtractor is shown in Fig. 4.7.

4.2.3 Start-up Circuit

A start-up circuit is necessary to prevent the beta-multipliers in this design from remaining in its degenerate operating point as the supply voltage ramps up from zero [7]. This degenerate operating point occurs when the gate voltage of the PMOS and NMOS

mirrors remain at the supply voltage and ground, respectively, and no current flows in either branch of the beta-multiplier. While this degenerate operating point is metastable [17], a start-up circuit is necessary to guarantee that the circuit operates at the desired bias point when the beta multiplier is initialized.

A number of start-up circuits have been proposed in reference circuits. A simple start-up shown in [7], is a diode-connected MOSFET connected between the gates of the PMOS and

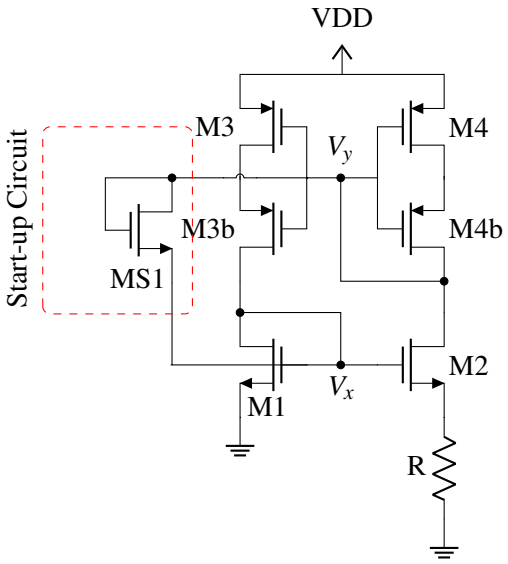


Figure 4.8: Start-up circuit shown in [7]

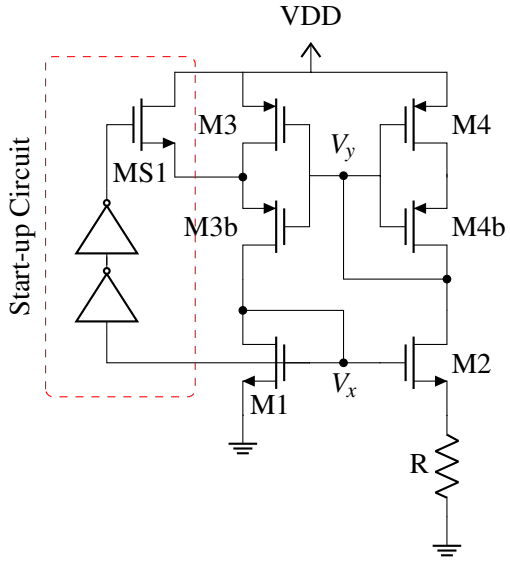


Figure 4.9: Start-up circuit shown in [23] and [30]

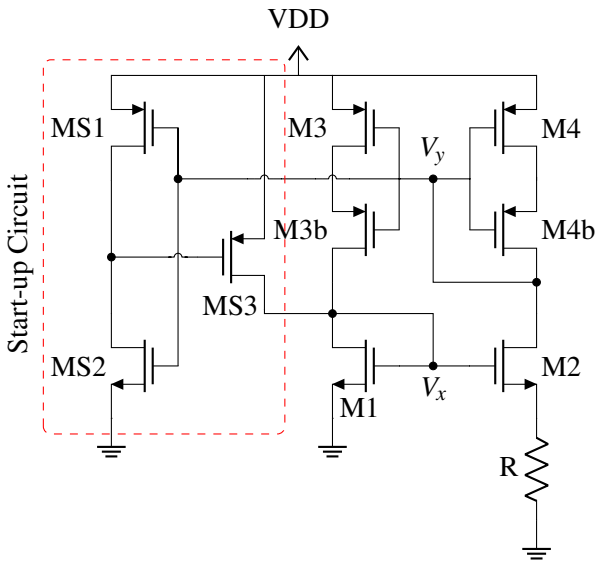


Figure 4.10: Start-up circuit shown in [44]

NMOS current mirror. This allows current to follow between the two gate nodes, pulling the gate of the PMOS transistors down, while pulling the NMOS transistors up.

One of the start-up circuits is shown in [23] and [30], which consists of two inverters and a MOSFET, as shown in Fig. 4.9. Using this start-up circuit, when no current flows, the gate voltage of the NMOS transistors are at ground; this pulls the gate voltage of the start-up MOSFET down. This in turn injects current into the beta-multiplier. The gate voltage of the NMOS transistors rises, causing the gate voltage of the start-up MOSFET to rise as well, turning the start-up MOSFET off.

Another start-up circuit that uses an inverter is shown in Fig. 4.10. The gate voltage of the PMOS inverter, MS1 and MS2, is pulled high when no current flows, causing the gate voltage of MS3 to be pulled low. This injects current into the beta-multiplier. The gate of MS3 is pulled up during steady state operation.

The issue with the simple start-up of Fig. 4.8 is the leakage current during steady state operation. At steady state, the diode-connected MOSFET will be biased into the subthreshold region, and will not completely turn off. This results in a leakage path between the gates of the NMOS and PMOS mirror. This leakage current is not defined by

the beta-multiplier and will prevent a proper PTAT current. Therefore, it is important for the start-up circuit to draw little static power and to minimally affect the beta-multiplier during operation. The start-up circuits that involve inverters may also create a sufficient leakage current that affects operation of the beta-multiplier. This may be adjusted by the optimizing the size of the inverter, but having an inverter connected to either the PMOS or NMOS gate will causes the input of the inverter to float between ground and VDD. This will keep the MOSFET connected to the output of the inverter to operate in the subthreshold region, resulting in a relatively large leakage current in the start-up circuit.

To completely reduce the leakage current, the MOSFET used to inject current into the beta-multiplier must be fully turned off. A start-up circuit that uses a capacitor can accomplish this. The start-up circuit proposed in [17] is shown in Fig. 4.11, and is composed of two transistors and a capacitor. The capacitor in the start-up circuit acts as a short circuit as the supply voltage ramps up, this causes V_s to rise with the supply voltage. The transistor connected between the gates of the PMOS and NMOS mirror turns on as a result of the applied gate bias. Current flows between V_x and V_y, pulling V_x and V_y up and

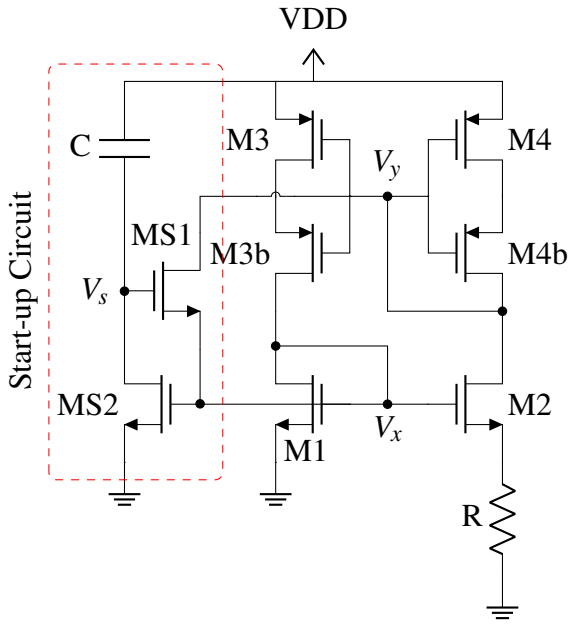
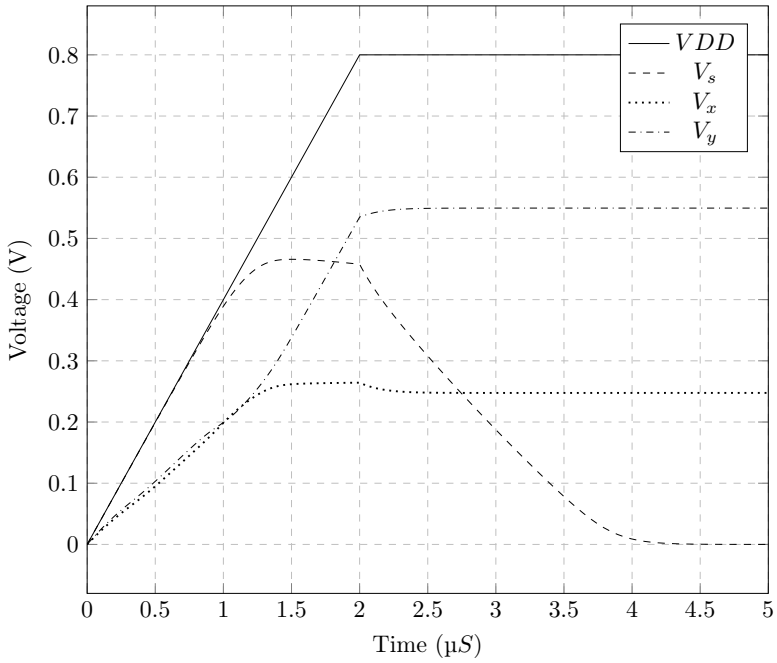
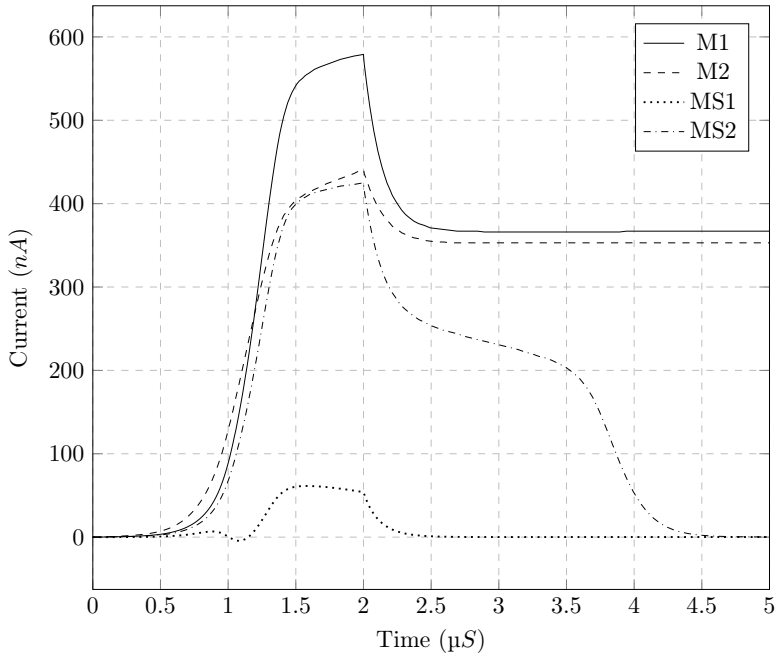


Figure 4.11: Beta-multiplier with self-cascode PMOS current mirror and start-up circuit

down respectively. This causes the transistors to turn on, allowing the beta-multiplier to leave its degenerate operating point. During steady state, the capacitor acts as an open circuit, and the bottom start-up transistor is turned on. V_s is discharged to ground, causing



(a)



(b)

Figure 4.12: Transient simulation of beta-multiplier during start-up

the transistor connected between the gates of the PMOS and NMOS mirror to turn off, preventing the gate of MS1 from floating between ground and VDD. This isolates the start-up circuit from the beta-multiplier during steady state operation, and the capacitor prevents the start-up circuit from drawing power. The capacitor may be replaced with a large resistor, as shown in Fig. 3.22, but the open circuit of the capacitor at DC presents a far higher impedance. The start-up circuit proposed in [17] will be used in this proposed constant g_m reference circuit.

A transient simulation of the beta-multiplier with the start-up circuit, shown in Fig. 4.11, was performed over 5 µS. The voltage supply is ramped up from ground to VDD. As shown in Fig. 4.12a, V_s rises with the supply voltage, but due to the slow ramp up, V_s flattens midway through. As the supply voltage reaches VDD, V_s falls towards 0 V. V_x and V_y rises and falls, respectively, as expected from the above analysis. The current through M1 and M2 sees a slight jump during start-up because of the current injected by MS1. The beta-multiplier achieves steady-state operation approximately 4 µS after powered on. At steady state, the current through MS1 and MS2 are found to be 124 pA and 210 pA, respectively. This indicates a low leakage current during operation that will have negligible effect on the PTAT current.

4.2.4 Resistor Selection

Many papers that utilize a beta-multiplier as a basis for achieving constant g_m reference, which develops a g_m that is proportional to $1/R$, indicate the use of a PVT-invariant resistor to obtain its results. However, this assumption is not practical in evaluating the PVT dependence of a constant g_m reference since even a precise external resistor will have a slight temperature and voltage dependence. As for the use of integrated resistors, large resistors occupy a significant amount of silicon area, and the resistance of these resistors are highly process dependent, which affects their temperature coefficient (TC) and voltage coefficient (VC) as well [45].

Nevertheless, by using a combination of different types of integrated resistors, an approximately zero-TC equivalent resistor can be obtained [8]. In TSMC's 65 nm process, this can be implemented by using a series of unsalicided p+ poly and n+ poly resistor. The p+ poly resistor has a negative first-order TC, whereas the n+ poly resistor adopts a positive first-order TC. With proper sizing, a zero TC resistor can be achieved on the first order. Since the positive TC of the n+ poly resistor is much lower than the negative TC of the p+ poly resistor, the n+ poly resistor is sized larger to cancel out the TC. The variations of the equivalent resistor are plotted over temperature and voltage in Fig 4.14. The equivalent resistor has a slightly concave response over temperature due to the positive second-order TC of both resistor types. Since the resistors are sized to achieve a zero-TC, the negative VC of the p+ poly resistor is not larger enough to offset the positive VC of the n+ poly resistor, so the resistance will rise slightly as voltage increases.

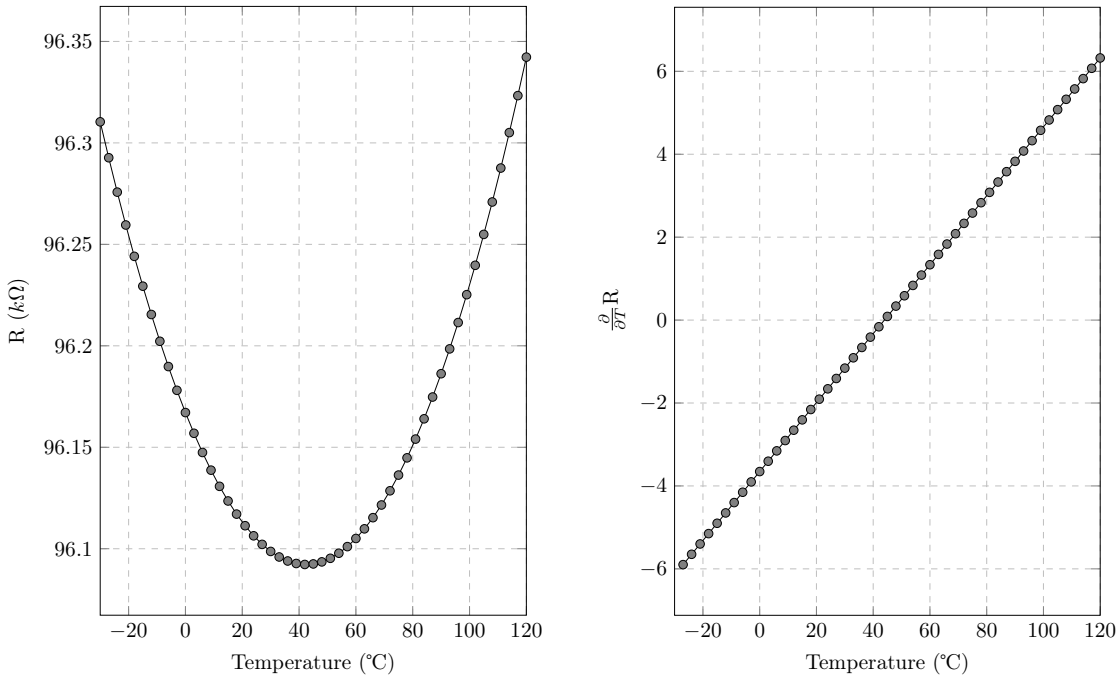
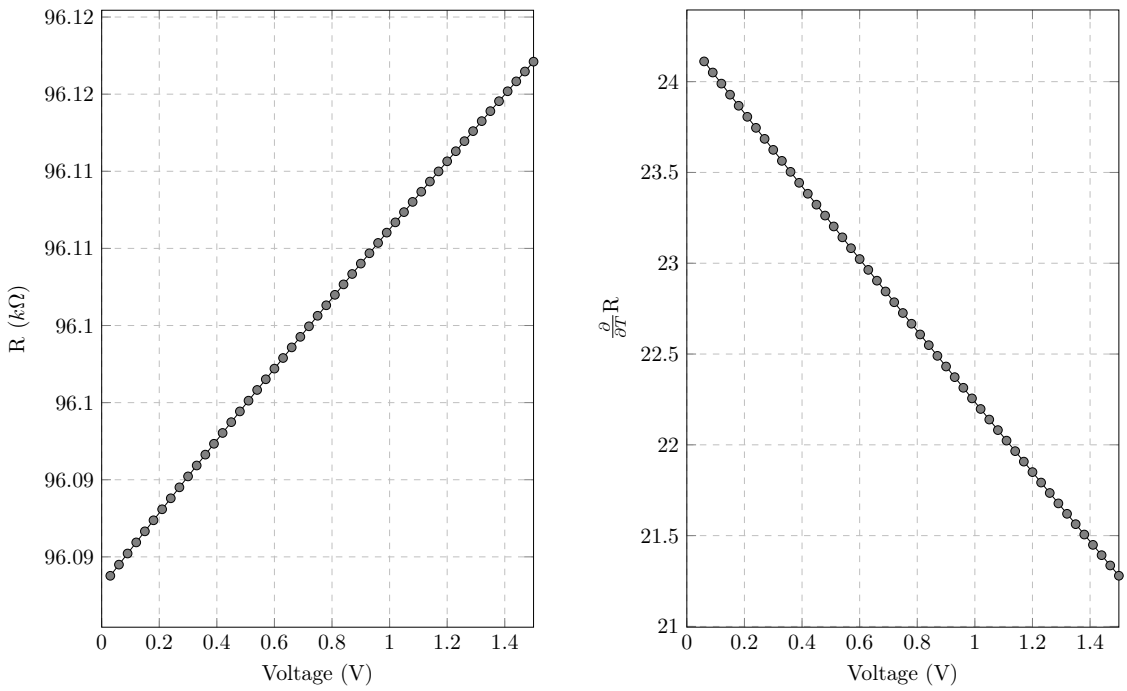


Figure 4.13: Plot of resistance of *R* over temperature and its derivative



(a) (b)

Figure 4.14: Plot of resistance of R over voltage and its derivative

4.2.5 Complete Design of Proposed Constant Transconductance Reference

The complete design of the proposed constant g_m reference that involves the design considerations discussed in Section 4.2.1 to Section 4.2.4 is shown in Fig. 4.15. Two independent beta-multipliers are shown at the left and right of Fig. 4.15, while the PTAT current subtractor is shown in the middle. The output current and g_m is taken from Mbias, which can be used to bias intended circuits.

4.3 Results

The complete proposed constant g_m reference circuit, shown in Fig. 4.15, is implemented using TSMC's 65 nm process. For the final design, K values of 18 and 2 are selected. Since integrated resistors are used in this paper. There is a balance between the available area and the size of resistance that can be obtained. Larger resistances can be

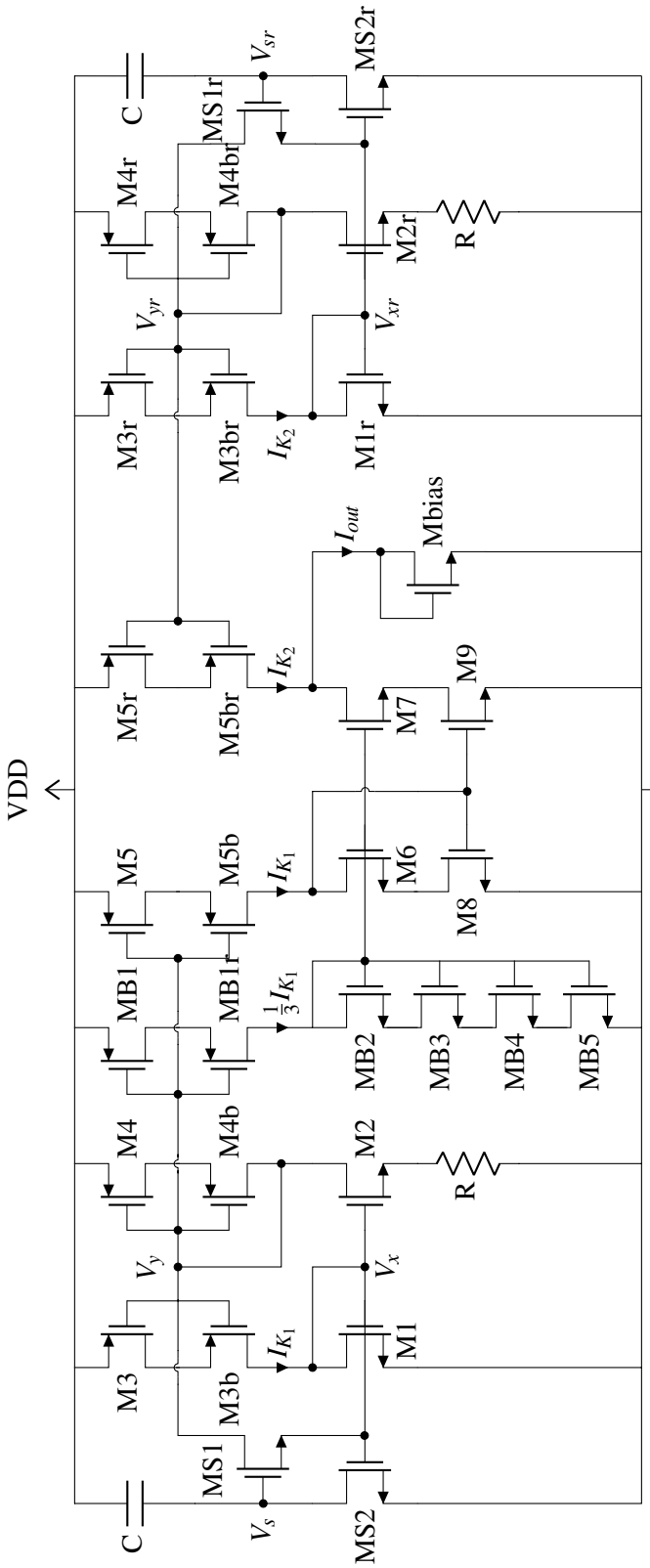


Figure 4.15: Proposed constant g_m reference circuit

obtained by reducing the width of the resistor, however this will lead to larger process variations due to under-etching non-uniformity [45]. Since the resistance value is determined by balancing the TC of the resistors, the die area available, and minimizing process variations, a total equivalent resistance represented by R in Fig. 4.15 is selected to be approximately 95 kΩ. Since the output PTAT current is proportional to $ln(K_2/K_1)/R$. If R is fixed, the ratio of K values will determine the output current. If a low K_2/K_1 value is selected, then the total power consumption of the circuit will be reduced at the expense of worse power efficiency. The opposite is true if a high K_2/K_1 value is chosen. As a result, to balance the total power consumption with power efficiency, $K_1 = 2$ and $K_2 = 18$ were chosen for the final design. While $K_1 = 2$ and $K_2 = 18$ were selected for implementation, it should be noted that this design can work at various K values.

In this design, all transistors are sized to have a length of 240 nm. Minimum lengths are avoided in the core design to decrease process variations and improve output resistance. This is important to improve the tracking of the current mirrors of this design. This also helps to minimize any leakage from MS1 and MS1r, which could influence the results if the leakage is significant. The widths of the transistors in Fig. 4.15 are listed in Table. 4.1.

As noted in [41], to maintain both PMOS transistors in the self-cascode current mirror in subthreshold saturation, the top transistors of the self-cascode MOSFETs are sized to be 20 times larger than the bottom transistors. Aside from the K value, the sizes for M1/M1r and M2/M2r are adjusted to optimize the response. The size of Mbias is sized small to allow for large replication of the output PTAT current.

The minimum widths for the self-cascode current mirror as well as the subtractor were found to produce the optimum results. However, the current through the branch with the MB1 and MB1r transistors should be reduced to improve power efficiency. Therefore, the self-cascode PMOS current mirrors are sized three times larger the minimum width, to allow MB1 and MB1r to be sized three times smaller to reduce the current in the bias

Table 4.1: Width of transistors in Fig. 4.15

Component	Value
M1, M1r	1.25 µm
M2	2.5 µm
M2r	22.5 µm
M3-M5, M3r-M5r	1.8 µm
M3b-M5b,M3br-M5br	36 µm
M6-M9	600 nm
MB1-MB5	600 nm
MB1r	12 µm
MS1, MS2, MS1r, MS2r	600 nm
Mbias	2 µm

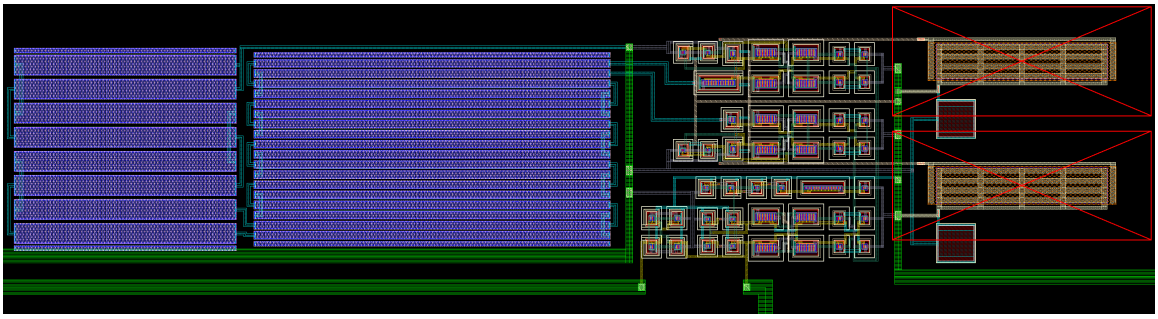


Figure 4.16: Layout of proposed g_m reference

branch. A series of four NMOS transistors, shown as MB2 to MB5, is used to generate the bias to keep M6 to M9 in subthreshold.

Since this design relies on the operation of several current mirrors and utilizes two beta-multipliers having different K values with identical resistors, it is important to minimize the effects of mismatch during fabrication. The use of multifinger transistors with dummy gates in a common-centroid arrangement is used to reduce mismatch in current mirror pairs [7]. It is also necessary to use an interdigitized layout with dummy resistors to improve the matching of the resistors [45]. Although process variations will

affect the absolute value of resistance and its TC, this variation can be slightly minimized by maximizing the perimeter to area ratio of the resistors to reduce the effects of under-etching and process gradients. The layout of the circuit is shown in Fig. 4.16 with an area of 315 µm x 64 µm. The core of the beta-multiplier, not including the resistors and the capacitor of the start-up circuit, occupies an area of 69 µm x 64 µm, which is only 1/5 of the total area. The passive components take up most of the silicon area.

To properly compare the results of the proposed constant g_m circuit to the conventional beta-multiplier, the conventional beta-multiplier is simulated with an K value of 9 to produce a similar output. The beta-multiplier shown in Fig. 4.6 is used to bias a transistor that is equivalent to the transistor Mbias of the proposed circuit in Fig. 4.15. The voltage and temperature variations of the proposed circuit are evaluated over a VDD range of 0.5 to 1.5 V, and over a temperature range of -30 °C to 120 °C. Fig. 4.17 shows the family of

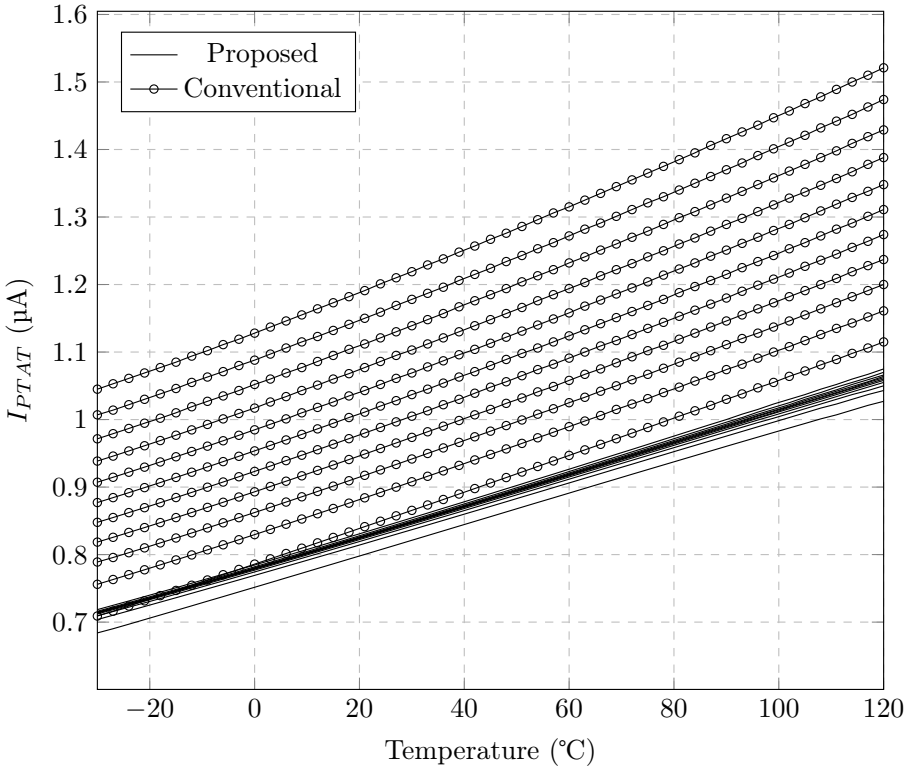
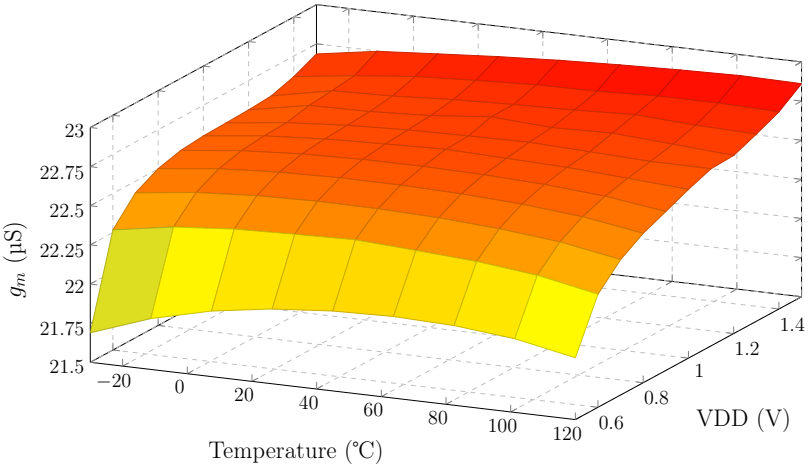


Figure 4.17: Comparison of family of I_{PTAT} over temperature between proposed and conventional circuit by sweeping supply voltage from 0.5 to 1.5 V



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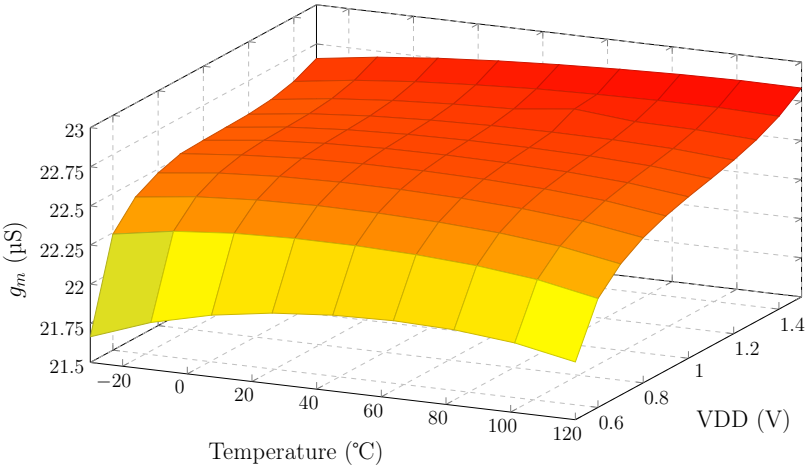

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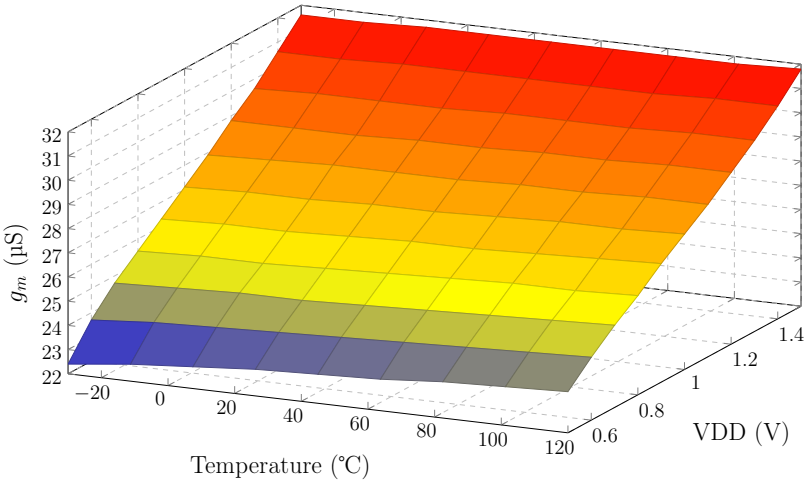
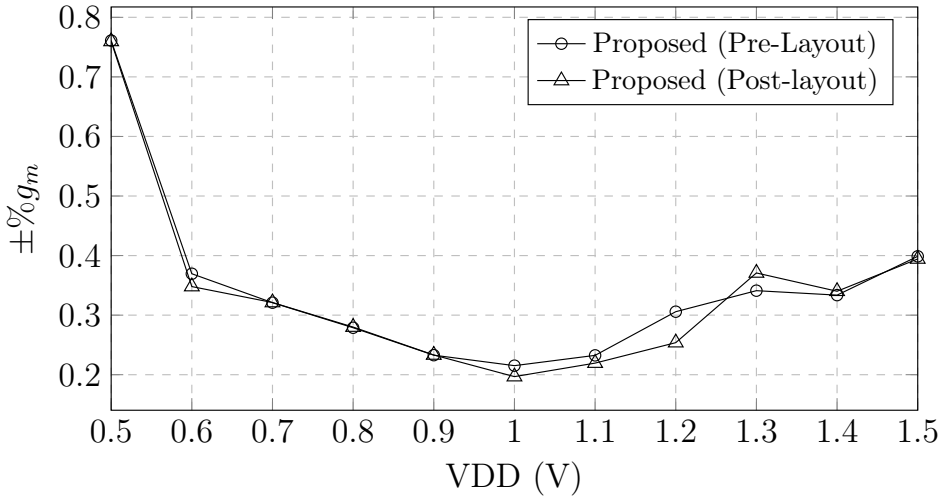


(c)

Figure 4.18: Surface plot of g_m over temperature and VDD (a) pre-layout (b) post-layout (c) conventional

PTAT currents over temperature for both the conventional beta-multiplier and the proposed reference circuit by sweeping over the tested supply voltage range. The PTAT currents of the proposed circuit shows significantly less deviation over VDD, compared to a beta-multiplier with a K value of 9, indicated by the smaller spread of PTAT currents as VDD is varied, which reflects the results shown in Fig. 4.4.

The g_m of the transistor Mbias will be considered the output g_m of the entire proposed constant g_m reference circuit, which is extracted from its operating point. To measure the



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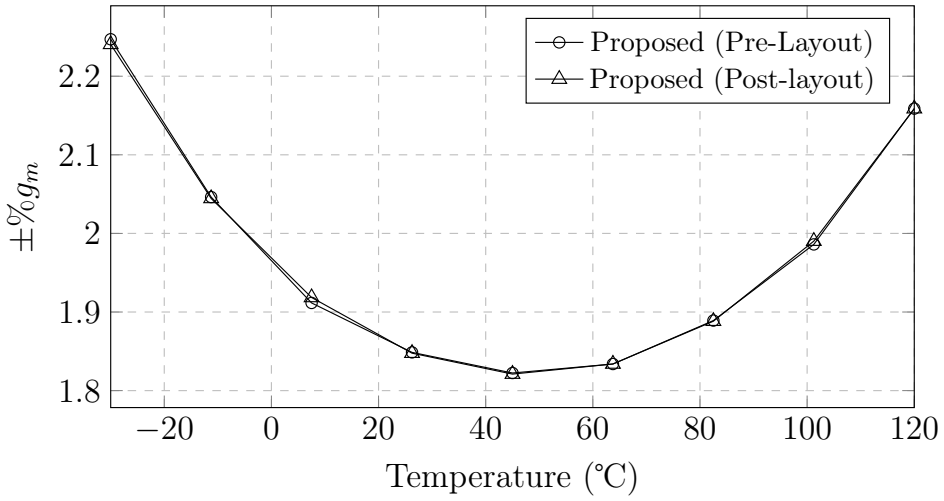

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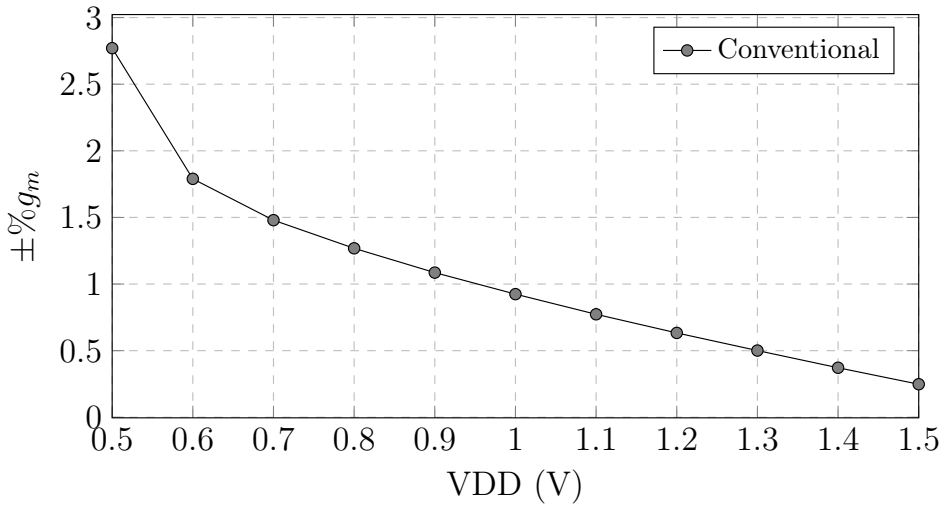
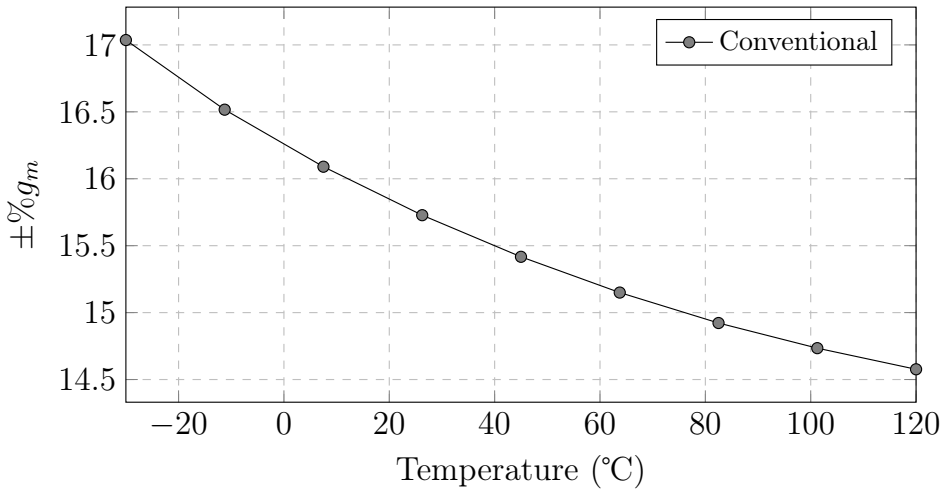
Figure 4.19: g_m dependence over (a) temperature for a given VDD and (b) VDD for a given temperature



(a)



(b)

Figure 4.20: g_m dependence over (a) temperature for a given VDD and (b) VDD for a given temperature

temperature and voltage dependence of the proposed circuit, the variations in g_m will be calculated using the maximum positive/negative variation ($\pm\%$) with respect to the mean. Fig. 4.18 shows surface plots of g_m over both voltage and temperature. Fig. 4.19 and 4.20 shows the $\pm\%$ error over VDD and temperature for the proposed and conventional circuits, respectively. For the proposed reference, g_m shows a minimum variation of $\pm 0.197\%$ over temperature at a supply voltage of 1 V, and a minimum variation of $\pm 1.82\%$ over VDD at a temperature of 45 °C. Across the entire tested VDD range, the variations of g_m vs.

temperature do not exceed $\pm 0.76\%$. While across the entire tested temperature range, the variations of g_m vs. VDD do not exceed $\pm 2.25\%$. The post-layout simulations show negligible difference to the pre-layout simulation results. While the conventional circuit was able to achieve a minimum variation of $\pm 0.25\%$ over temperature at a supply voltage of 1.5 V, it shows significant degradation over the entire VDD range, with a maximum variation of $\pm 2.77\%$ over temperature at a supply voltage of 0.5 V. Variations over VDD is significantly worse with a minimum variation of $\pm 14.58\%$ over VDD.

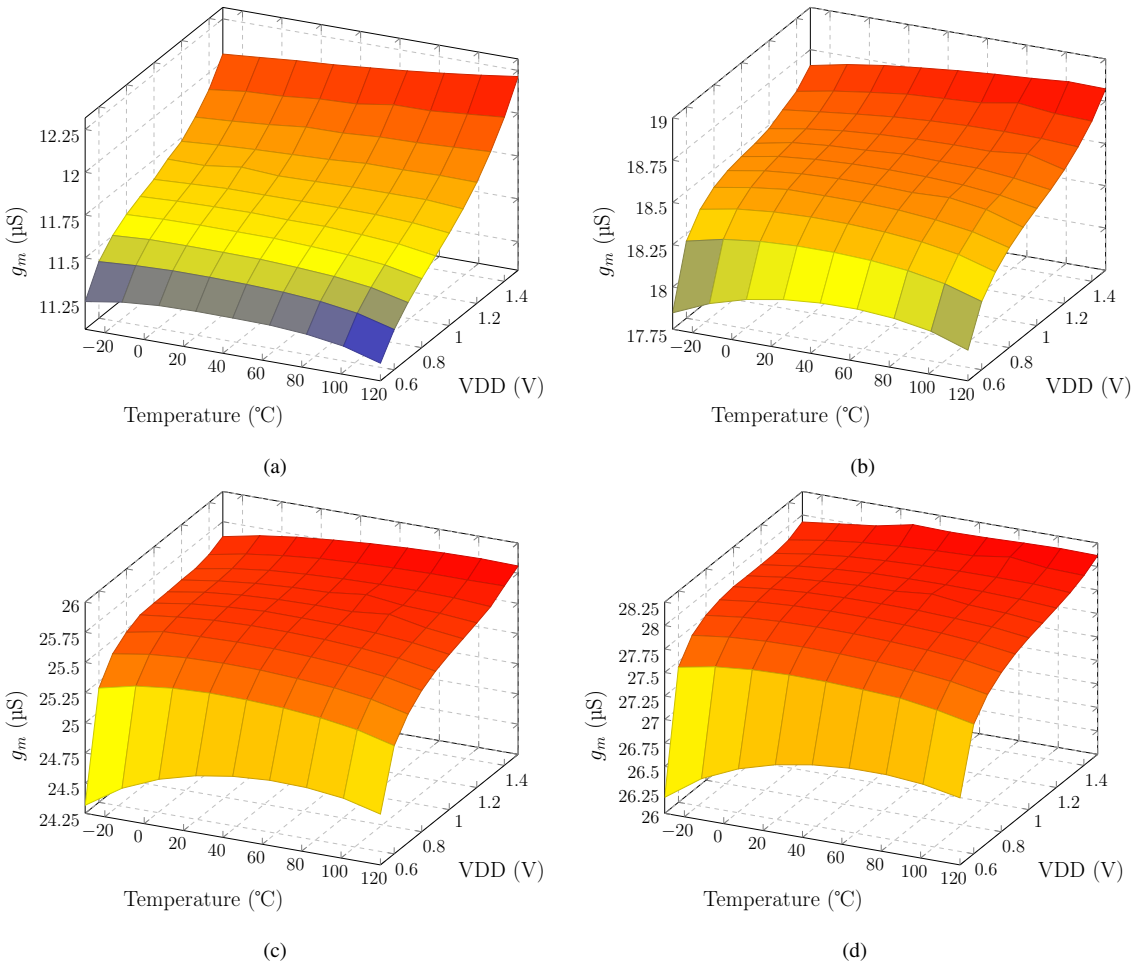
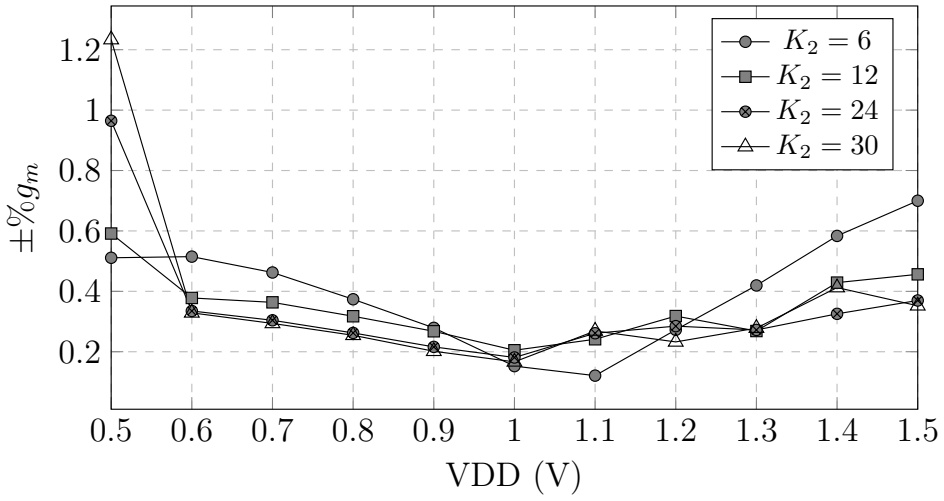


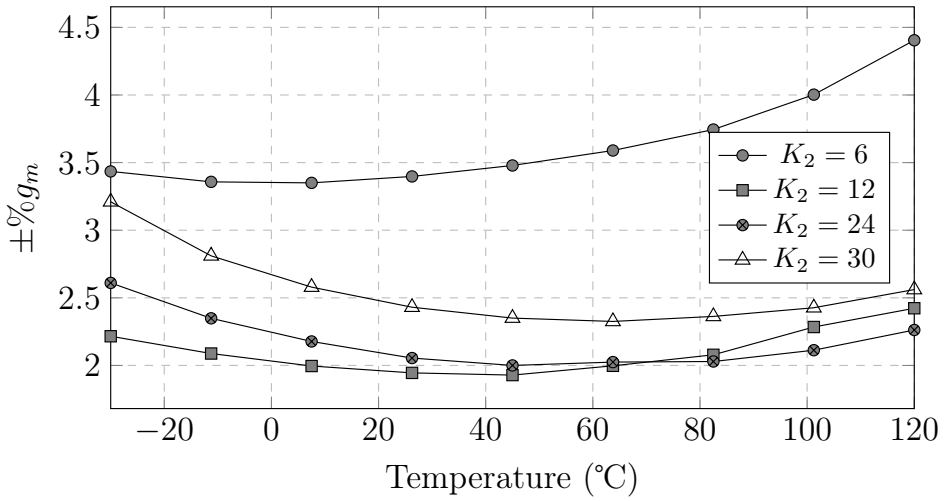
Figure 4.21: Surface plot of g_m over temperature and VDD for $K_1 = 2$ and (a) $K_2 = 6$ (b) $K_2 = 12$ (c) $K_2 = 24$ (d) $K_2 = 30$

4.3.1 Results over Different K values

As noted above, although the proposed circuit was implemented with $K_1 = 2$ and $K_2 = 18$, various K_2 values can be chosen. To show the dependence of the reference as a function of K_2 to K_1, the circuit is simulated with K_2 values of 6, 12, 24 and 30 while maintaining a K_1 of 2. The surface plots of g_m vs. temperature and VDD for different K_2 values are depicted in Fig. 4.21. The temperature and voltage variations at these K_2 values is



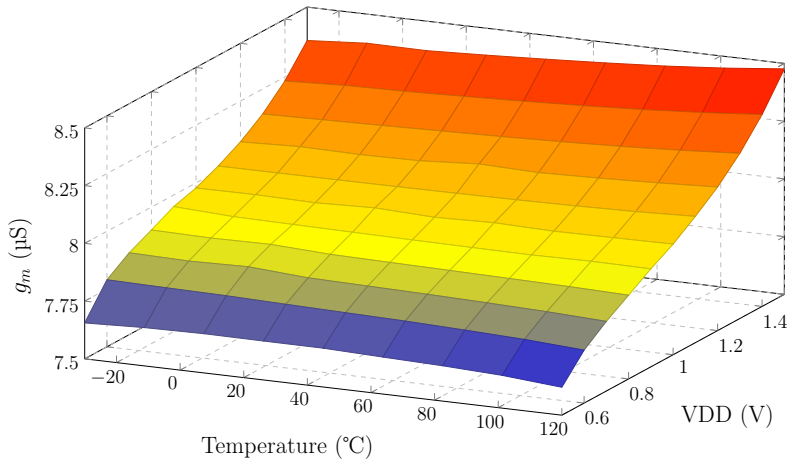
(a)



(b)

Figure 4.22: g_m dependence over (a) temperature for a given VDD and (b) VDD for a given temperature for different K_2 values

comparable to $K_2 = 18$, as shown in Fig. 4.22. It should be noted that for higher K_2 values, variations at a lower VDD are larger due to the higher minimum operating voltage to supply the required current. Fig. 4.21 and 4.22 demonstrate that using various K values is viable in the proposed design, and its selection is dependent on whether a low power consumption or high g_m efficiency is desired. Increasing K_2, while keeping K_1 constant will increase the usable current, and therefore g_m efficiency, at the expense of higher power consumption from the beta-multiplier with the K_2 value.



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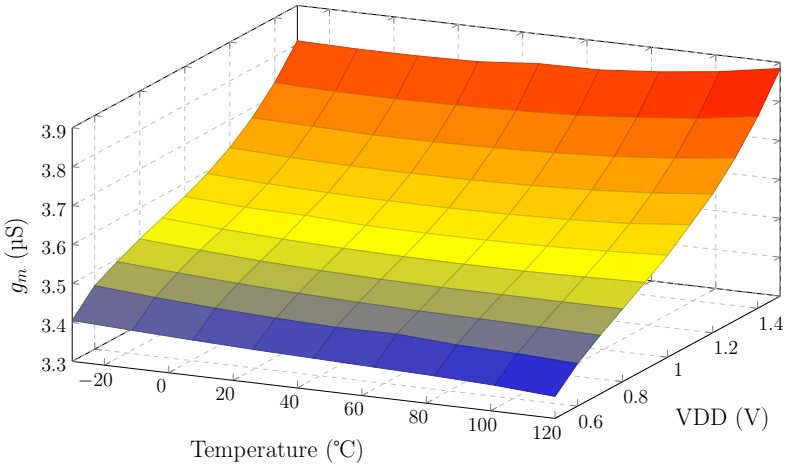
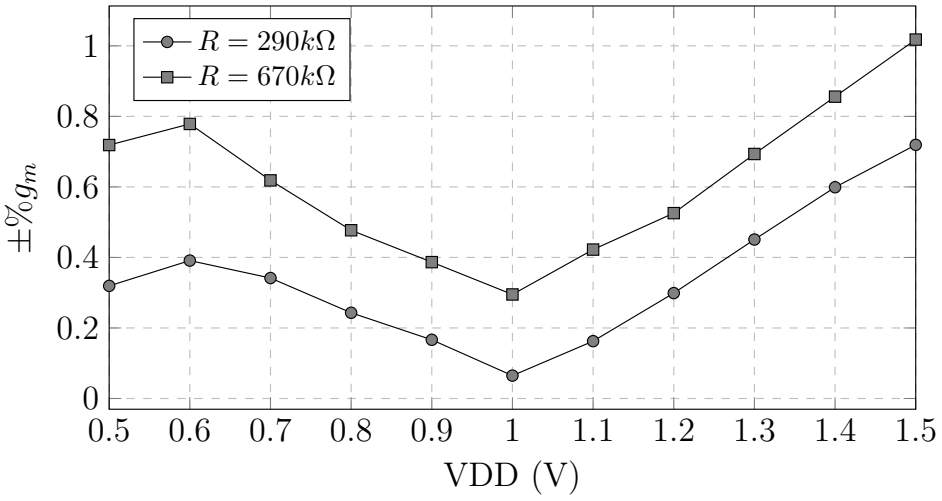


(b)

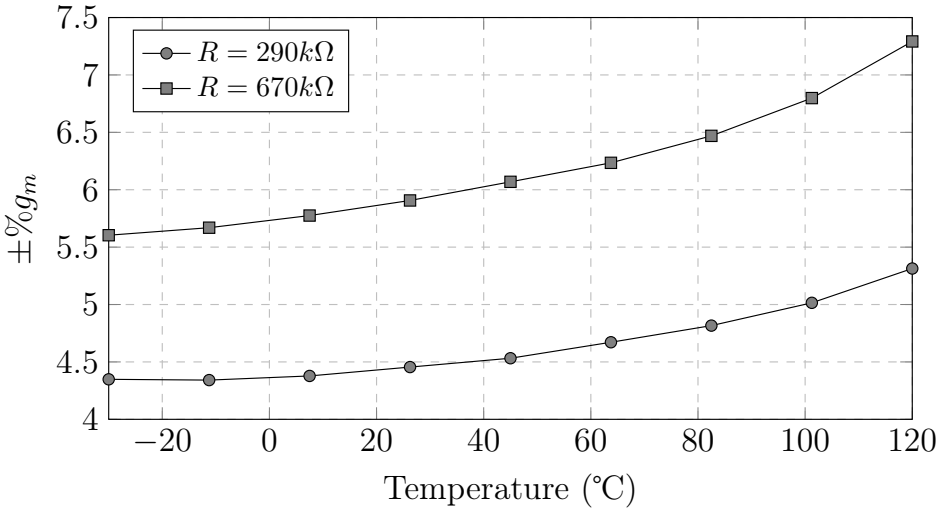
Figure 4.23: Surface plot of g_m over temperature and VDD for (a) R = 290 kΩ (b) R =670 kΩ

4.3.2 Results over Different R values

Similarly, various R values can also be selected. Surface plots of g_m for $R \approx 290$ kΩ and 670 kΩ are shown in Fig. 4.23. Their voltage and temperature dependence is likewise indicated in Fig. 4.24a and 4.24b for variations across temperature for a specific VDD and variations across VDD for a specific temperature, respectively. Although a larger R can be chosen, their dependence as measured by the $\pm\%$ variations, indicate that voltage and



(a)



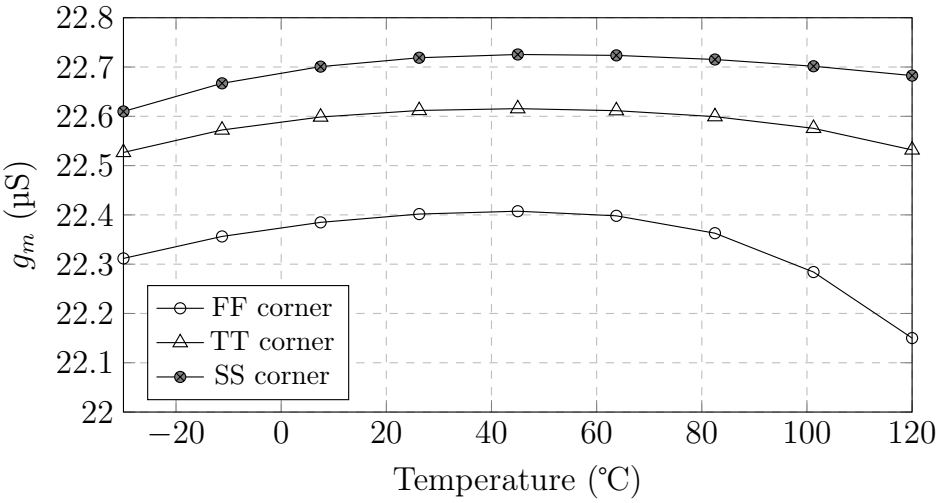
(b)

Figure 4.24: g_m dependence over (a) temperature for a given VDD and (b) VDD for a given temperature for different resistors

temperature variations increases with R. For $R \approx 290$ kΩ, while g_m performs well across temperature, it shows larger variations over voltage, as shown in Fig. 4.24b. For $R \approx 670$ kΩ, voltage and temperature variations increases, showing larger variations in g_m.

4.3.3 Results over Process Variations

In Section 4.1, the method for reducing process variations in the proposed constant g_m reference was described. Here we evaluate and compare the process dependence of the



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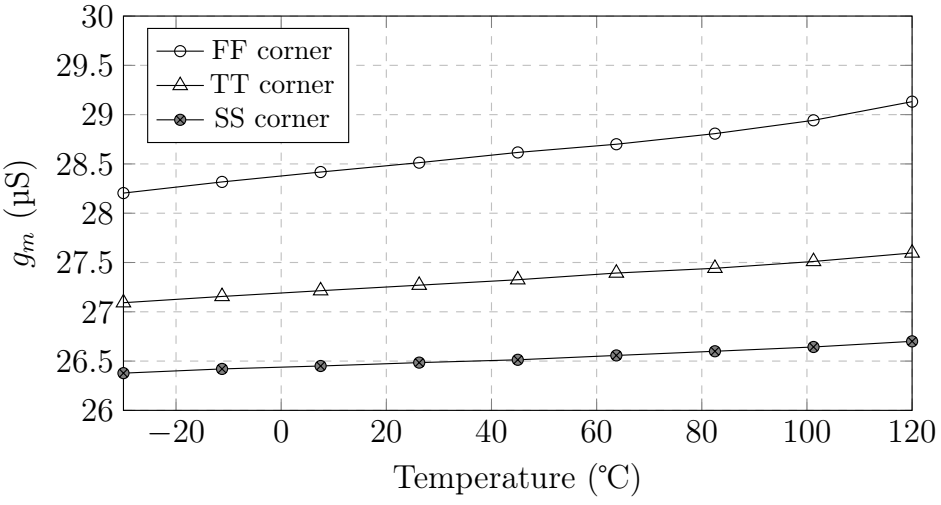
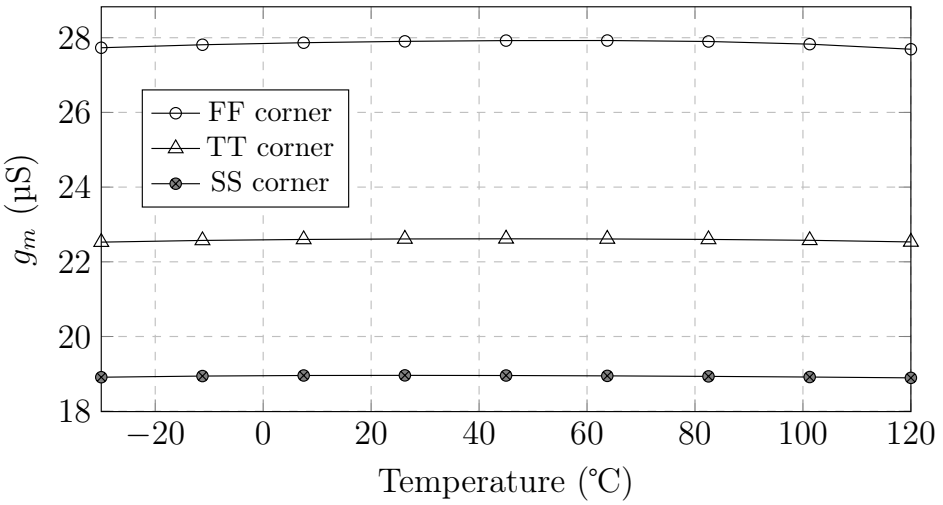
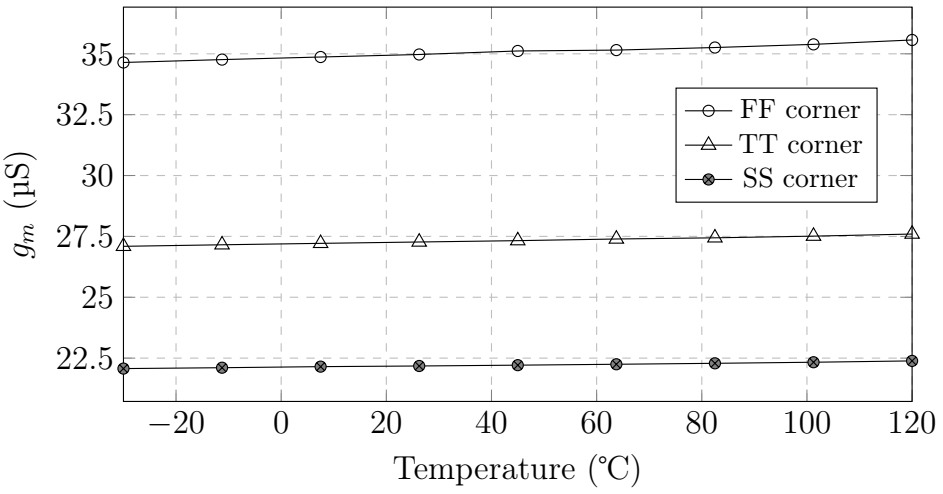


(b)

Figure 4.25: g_m vs. temperature across process corners without process variations of resistor for (a) proposed post-layout and (b) conventional



(a)

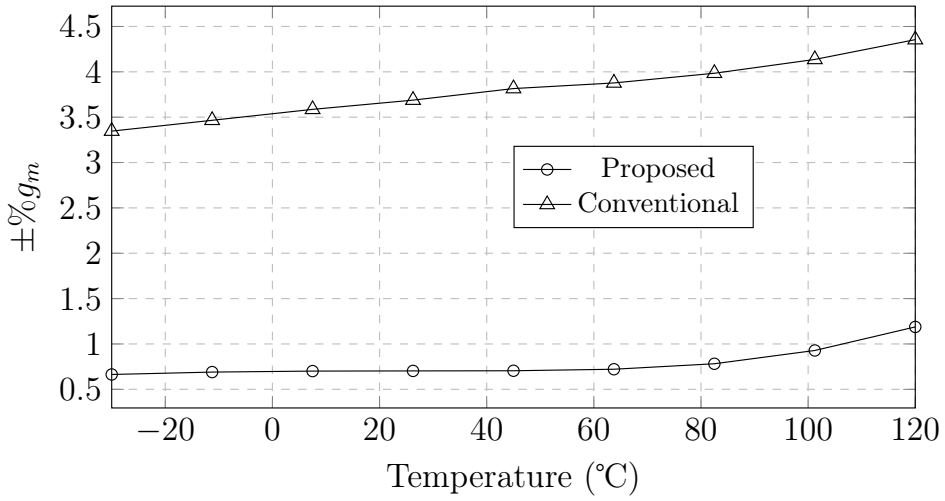


(b)

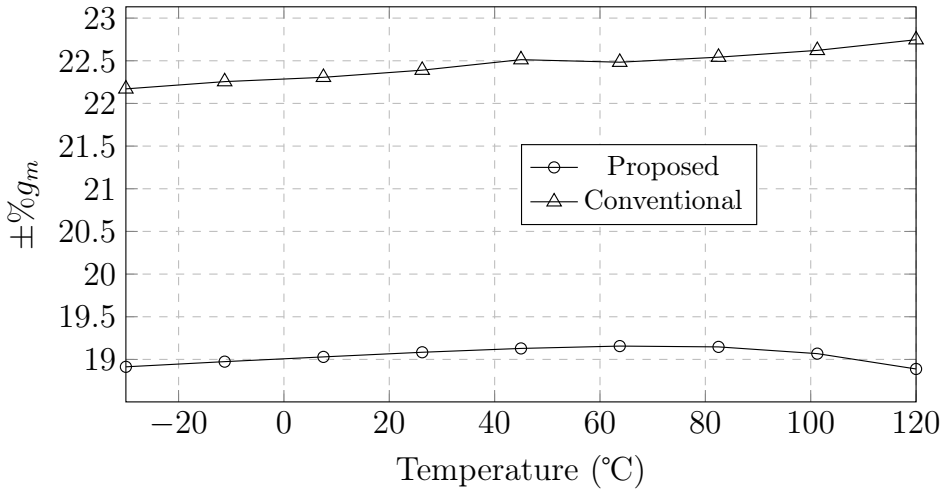
Figure 4.26: g_m vs. temperature across process corners with process variations of resistor for (a) proposed post-layout and (b) conventional

proposed circuit to the conventional circuit. To evaluate the process dependence of the references, g_m will be plotted vs. temperature at a supply voltage of 1 V for the SS, TT and FF corners. Fig. 4.25 shows the g_m vs. temperature curves over process corners without considering process variations of the resistor. g_m of the beta-multiplier should ideally only depend on the difference in transistor size and R. If the resistor is process invariant, then the constant g_m reference should display less variations with process. The non-idealities of the conventional beta-multiplier causes it to show some process variation as reflected

in the Fig. 4.25b. At nominal temperature, the conventional reference shows variations of $\pm 3.69\%$ over process corners. The proposed circuit is able to further reduce this process sensitivity due to second-order effects to provide a more constant g_m over process corners, as shown in Fig. 4.25a, resulting in variations of $\pm 0.7\%$ at nominal temperature. The g_m for the FF corner is found to be lower, while g_m for the SS corner is higher than the typical corner. This result is due to process variations affecting the beta-multiplier with the smaller K value more than the beta-multiplier with the larger K value.



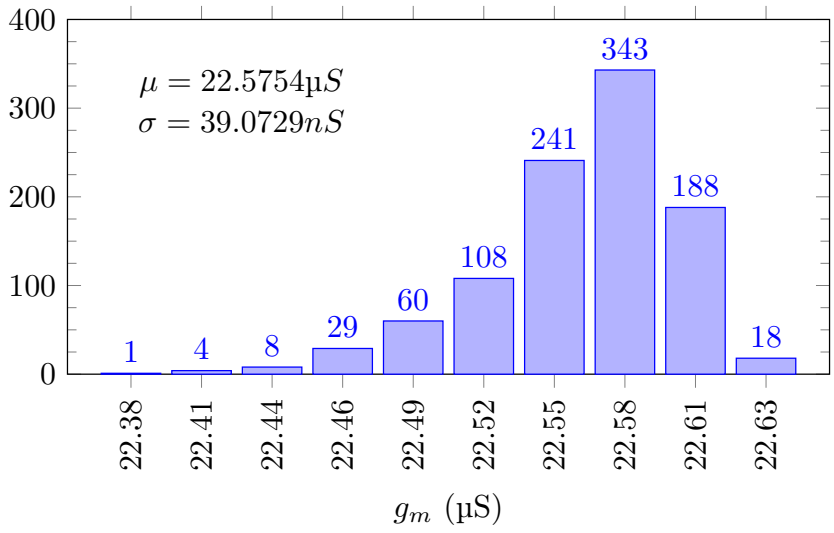
(a)



(b)

Figure 4.27: g_m dependence over process variations for a given temperature at 1 V (a) without resistor variations (b) with resistor variations

When process variations of the resistor are considered, both the proposed and conventional references see a significant increase of dependence to process variations shown in Fig. 4.26. Process variations rise to $\pm 22.4\%$ and $\pm 19.1\%$ for the conventional and proposed reference, respectively. The proposed constant g_m reference displays a similar improvement in percentage with or without considering process variations of the resistor. The insensitivity to process variations of both the proposed and conventional g_m



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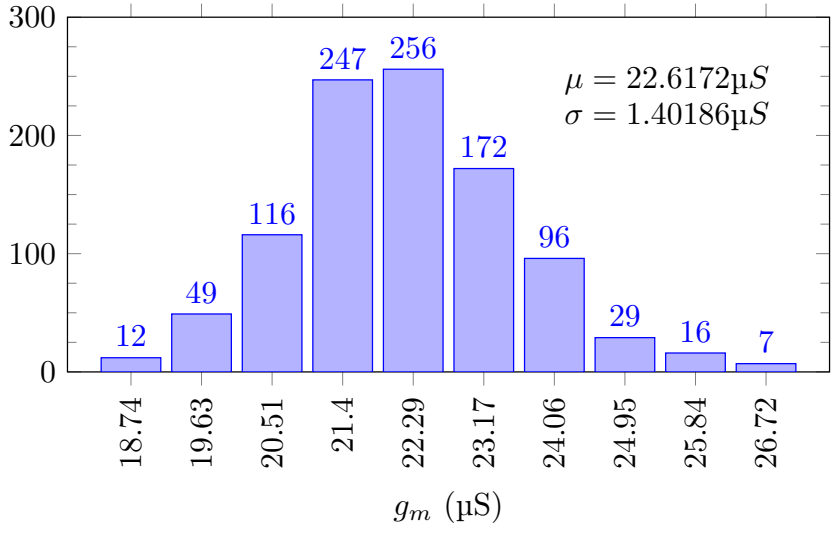
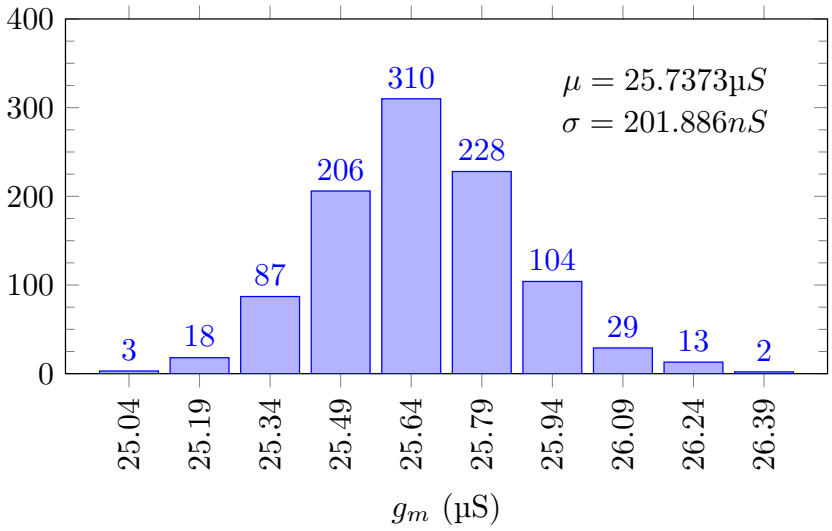


(b)

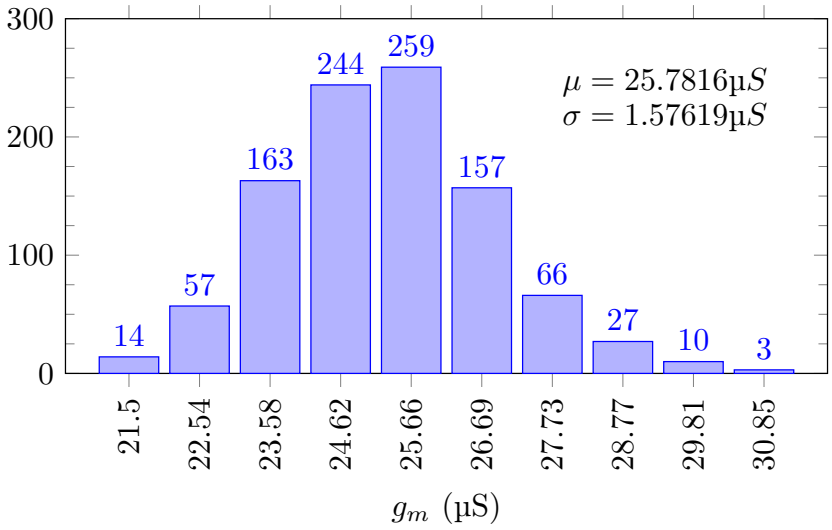
Figure 4.28: Monte Carlo process analysis of proposed g_m reference (a) without resistor process variation and (b) with resistor process variation

reference is limited by the process variations of the resistor. This is to be expected since g_m of both references are proportional to $1/R$. The $\pm\%$ variations over the process corner across the entire temperature range is shown in Fig. 4.27. The proposed g_m reference is less process dependent, regardless of temperature.

Process variations for the proposed circuit and conventional circuit are also evaluated



(a)



(b)

Figure 4.29: Monte Carlo process analysis of conventional g_m reference (a) without resistor process variation and (b) with resistor process variation

using Monte Carlo simulations over 1000 samples. Fig. 4.28 shows the Monte Carlo process analysis of the proposed circuit, while Fig. 4.29 shows the Monte Carlo process analysis for the conventional circuit. The Monte Carlo simulations reflect the results obtained over the process corners. The Monte Carlo simulation of the proposed constant g_m reference has a standard deviation of 1.40 µS and only 39.1 nS, with and without accounting for process variations in the resistor, respectively. This improves upon the conventional circuit, which has a standard deviation of 1.58 µS and 200 nS, with and without accounting for process variations in the resistor, respectively.

4.3.4 Comparison with Previous Works

Table 4.2 compares this proposed g_m reference to other prior works. The results of the proposed circuit in Table 4.2 are shown when operating nominally at 0.5 and 1 V. Supply variations of the proposed circuit shows higher $\pm\%g_m$ variations compared to other works; however the proposed circuit was evaluated over a larger voltage range than most works, and most of the variation is attributed to operating from 0.5 to 0.6 V. If the voltage range is redefined to lie between 0.6 to 1.5 V, there is a g_m variation of $\pm 0.951\%$. The proposed g_m reference shows the least variations over temperature when operating at 1V, while again maintaining a larger temperature range than most works. Variations of g_m over temperature at 0.5 V is in line with other works. Most notable is the efficiency in generating the output transconductance compared to other works at both operating voltages; the output g_m produce for the given power is significantly higher than other reported g_m references.

Table 4.2: Comparison to other works

Reference	Process	Temp. Range (°C)	Voltage Range (V)	$\pm\%g_m$ over VDD	Nominal g_m	$\pm\%g_m$ over Temp.	Power	g_m/Power Ratio
This Work	65 nm	-30 to 120	0.5 to 1.5	1.85 (0.951†)	21.95 µS*	0.760*	2.06 µW*	10.67*
					22.61 µS**	0.197**	5.12 µW**	4.42**
[23]	180 nm	20 to 80	1.2 to 1.8	1	-	1.5	1.275 mW	-
[22]	180 nm	25 to 100	1.8	-	1.41 µS	1.4	1.44 µW	0.98
[24]	0.35 µm	20 to 80	2.7 to 3.3	1.3	284 µS	1.1	-	-
[26]	65 nm	-20 to 110	0.4 to 1.2	6.15‡	10.5 mS	2.6‡‡	56 mW	0.19
[30]	0.5 µm	-30 to 110	1.1 to 1.7	-	69.2 nS	0.76	110.6 nW	0.63
[31]	65 nm	-60 to 130	2.5	-	5.002 mS	0.22	2 mA	1
[32]	180 nm	-25 to 125	1.0 to 2.0	-	83.5 µS	∼1.02	486 µW	0.17
[19]	150 nm	-40 to 125	1.52 to 1.68	0.8	860 pS	0.63	9 nW	0.096

* Results from operating at 0.5 V and nominal temperature

** Results operating at 1 V and nominal temperature

† Calculated for voltage range from 0.6 to 1.5 V

‡ Maximum $\pm\%g_m$ vs. VDD and process for voltage range of 0.54 to 0.66 V. No process variation for resistors.

‡‡ Maximum $\pm\%g_m$ vs. temperature and process. No process variation for resistors.

4.4 Summary

The proposed constant g_m reference, which creates a constant transconductance by subtracting two independent transconductance references is presented in this chapter. Second-order effects that are common to both beta-multipliers are minimized, which reduces all PVT variations. The proposed g_m reference does not rely on the use of op-amps or external references, and is developed to work as a general-purpose reference to replace conventional current biasing techniques. The technique, design and results of the proposed g_m are explored. The proposed circuit was implemented with a a $K_2/K_1 = 9$ and $R \approx 96$ kΩ but was also demonstrated to work with different K and R values. To evaluate the PVT dependence of the proposed circuit, its response over a temperature range of -30°C to 120°C, and a supply voltage range of 0.5 to 1.5 V was demonstrated. To evaluate the effects of process variations, the proposed circuit was simulated over SS, TT and FF corners, and by using Monte Carlo simulations. The proposed circuit was compared to the conventional beta-multiplier with composite transistors for the PMOS current mirror for all PVT variations, and was found to be more PVT invariant than the conventional circuit. The transconductance of the proposed reference has a maximum variation of $\pm 0.197\%$ over temperature at 1 V, lower than all compared circuits, and a maximum variation of $\pm 1.82\%$ over the supply voltage at 45°C. The proposed constant transconductance reference has the highest power efficiency (transconductance over power consumption) amongst the reported constant transconductance references. At 0.5 V and nominal temperature, the constant transconductance reference produces a transconductance of 21.95 µS, while consuming 2.06 µW.

Chapter 5

Conclusions and Future Research

5.1 Conclusions

Subthreshold operation offers ultra-low power consumption combined with high g_m efficiency but comes with increased sensitivity to PVT variations that modify g_m, which determines key circuit parameters such as gain, frequency response and impedance matching. To produce reliable circuits that operate in the subthreshold region, it is critical to keep g_m constant to ensure that operation of the biased circuit remains consistent for all operating conditions. This is conventionally done by using the beta-multiplier. However, second-order effects, such as channel length modulation, will cause the constant g_m reference to vary considerably. The use of cascodes or operational amplifiers reduces the effects of channel length modulation at the expense of limiting the operating voltage range (higher minimum voltage) and increased power consumption. Other existing works have tried to minimize the effects of channel length modulation but they come with drawbacks of limited application and the need for external references or sources, while still relying on operational amplifiers. This thesis addresses the effects of channel length modulation and proposes a general-purpose self-contained g_m reference that reduces PVT variations by taking the difference between two references.

In Chapter 1, the fundamentals of subthreshold operation, and its advantages and

disadvantages are detailed. Chapter 2 focuses on the conventional method of creating a constant g_m, and the challenges and issues of the conventional circuit, coming from the PVT variations of the resistor and channel length modulation. Chapter 3 reviews existing works that minimizes these issues, which leads to the conclusion that there needs to be more work done to create a general-purpose, self-contained constant g_m reference that reduces the effects of channel length modulation with high efficiency.

Chapter 4 presents the proposed constant g_m reference circuit to minimize second order-effects, by taking the difference between two currents generated by two independent beta-multipliers. The proposed circuit reduces all PVT variations compared to the conventional g_m reference. The resulting g_m reference circuit was able to operate over a VDD range of 0.5 to 1.5V, which is larger than most g_m reference circuits, and over a temperature range of -30°C to 120°C. From 0.5 to 1.5V, the current varies by 4.2%/V. The proposed reference has a maximum variation of only $\pm 0.197\%$ g_m with respect to temperature at 1V, the smallest variation found compared to other g_m references, and a maximum variation of $\pm 1.82\%$ g_m over the entire tested voltage supply at 45°C. The proposed constant g_m reference posts the highest efficiency amongst the reported constant g_m references. At 0.5V, the constant g_m reference produces a g_m of 21.95 µS, while consuming 2.06 µW.

5.2 Future Work

The notable deficiency in the proposed reference circuit design is the use of a resistor. As indicated in Chapter 3, a number of papers have proposed replacing the resistor with a MOSFET or capacitor equivalent due to the impracticalities associated with implementing a on-chip or external resistor. While the TC of the resistor can be managed at the onset as shown in Section 4.2.4, the resistor remains highly process dependent. This will not only affect the absolute value of resistance but also the TC of the resistor as well, since the TC depends on the sizing of the resistor. Therefore, a MOSFET or capacitor equivalent

resistor needs to be developed in future work to avoid issues with using on-chip or off-chip resistors.

5.3 Related Publication

From the results of the research presented in this thesis, the following journal article has been submitted for publication:

M. Lee and K. Moez, "A 0.5-1.5V Highly Efficient and PVT-Invariant Constant Transconductance Reference in CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, 2020. (Submitted for Initial Review)

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