Published in IET Power Electronics
Received on 16th March 2011
Revised on 14th July 2011
doi: 10.1049/iet-pel.2011.0105

ISSN 1755-4535

Comparison of insulated gate bipolar transistor models for FPGA-based real-time simulation of electric drives and application guideline

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Abstract: In this study, a comparison of various insulated gate bipolar transistor (IGBT) models for field-programmable gate array (FPGA)-based real-time simulation of power electronic devices is presented. System-level behavioural models include ideal, switching function and averaged models, and the detailed device-level model includes both linear behavioural and non-linear look-up table-based models of IGBT. A three-level 12-pulse voltage source converter system driving a squirrel-cage induction motor has been chosen as the test case system. The entire system including the controller and pulse width modulation (PWM) is implemented on a single FPGA using very high-speed description language in real-time at a fixed time-step of 12.5 ns. The Altera Startix III FPGA is the device used for real-time simulation. Results obtained through all five models are compared and as expected, it has been found that the behaviour-mode simulation is fast but comes with a sacrifice of accuracy and details. A guideline is provided for the users with suggestions, so that the right kind of model can be selected for a particular study.

1 Introduction

The insulated gate bipolar transistor (IGBT) has become the device of choice for many power applications because of its promising performance, low on-state and switching loss, switching speed and ease of use. Prior to the development of any new application employing an IGBT, a rigorous study of the dynamic performance of the system is essential. Accurate modelling of the device along with the proper simulation platform can guarantee the true reflection of device behaviour. However, owing to the limitations imposed by the modelling complexity and specific hardware used, it is sometimes necessary to compromise in both arenas. Though off-line simulations tools such as SABER, SPICE, etc. are available with detailed models [1], these models take excessive time for a small amount of simulation time. In addition, owing to the differences in the system parameter values with the actual measured values, the designed control system may not operate as desired in the real world. Hence, the results produced through the off-line simulation may not reflect the true system behaviour. Real-time simulation or to be precise, hardware-in-the-loop simulation has come forward to help avoid such a compromise and thus produces realistic results with the help of state-of-the-art hardware and software [2–21].

Most of the commercial real-time simulators employ either general purpose processors or digital signal processor (DSP) to perform the real-time simulation. Although parallel processing techniques are applied by these simulators to perform fast computation, their main drawback still lies in their inability to perform a real-time simulation using a time-step in the range of sub-micro seconds, which is a requirement for producing the dynamic behaviour of an IGBT using a detailed device-level model. In this regard, field-programmable gate arrays (FPGAs) are gaining momentum as the computation engine either independently or embedded with other fast processors. This digital processor can be used for implementing computationally intensive algorithms in real-time because of its high-speed inherent parallel hardwired architecture and flexible memory allocation. As this device works as a reconfigurable hardware (as opposed to processors where a task is performed through software programs), the simulation is performed through the realignment of hardware logic gates and digital signals (voltages) are passed through them. As a result the simulation is very fast and is performed with a time-step of a few nano-seconds. This provides the opportunity to accurately model the turn-on and turn-off non-linear characteristics of the IGBT.

Over the years, owing to the high volume of interest in the IGBT for power electronic applications, many models of this device have been proposed and used in the simulation industry. These models of IGBTs can be categorised broadly as [22–25] physics based models, device-level models and behavioural models. Other types of classifications such as mathematical model, semi-mathematical model, behavioural model, semi-numerical model are also used in the literature. Irrespective of the

classification used, these models were developed using different methods and have different objectives, aspects and performance. In this paper, a comparison of five different kinds of IGBT models is given for a complete real-time simulation of the power electronic motor drive on a single FPGA. The results are compared and a guideline for the users has been provided so that proper model of the IGBT can be chosen for intended study.

2 Overview of IGBT modelling for transient simulation

IGBT-based power electronic apparatus can be modelled using two types of off-line [1] simulation tools: (1) system-level, and (2) device-level. System-level modelling is fairly fast, however, it cannot show the device characteristics accurately. All electromagnetic transient (EMT)-type software and general mathematical modelling packages such as PSCAD/EMTDC, EMTP-RV and MATLAB/SIMULINK belong to this category. These tools utilise nodal analysis or state-space solution of linear ordinary differential equations discretised using numerical integration rules such as the Trapezoidal Rule. For system-level study, power electronic devices are often modelled in these tools using three types of behavioural [24] models: (i) ideal model, (ii) switching function model and (iii) averaged model. All of these models have also been used for off-time simulation.

In the 'ideal model', the detailed device non-linear characteristics are replaced by an ideal characteristics where external characteristics related to switching transients, diode reverse recovery, snubber circuits and stray components are omitted. In this modelling category, each IGBT is represented as a two-valued resistor for its 'on' and 'off' states. A change of switch status, however, results in a change of circuit topology which, in turn, requires the re-calculation of the system admittance matrix. Generally, in real-time simulation, these matrices are pre-computed and stored to minimise simulation time.

In the 'switching function' model, a switching converter circuit is replaced by a circuit consisting of only controlled voltage and current sources. The simulation is much faster using the switching-function model with almost the same results as those of the ideal model, that is, high-frequency effect is included. However, since individual switches no longer exist, it is not possible to monitor the voltage/current or conduction of individual switches.

The 'averaged model' can be obtained directly from the switching functions by including the low-frequency components of the switching functions while ignoring all the high-frequency components. Averaged models have been used in controller design and small-signal analysis of the switching converters.

In the second category of device-level modelling, the phenomena of interest are the switching transients, power losses and thermal characteristics of the device. SABER and the family of SPICE software are examples of these types of tools, which employ simultaneous non-linear system solution using numerical methods such as the Newton–Raphson or the Katzenelson method [26]. Device-level modelling is very accurate; however, for motor drives simulation it can be very time-consuming. There are three types of device-level models [22] available in the literature: (i) analytical models, (ii) behavioural models and (iii) numerical models. These device models have yet not been employed for real-time simulation mainly because of their computational complexity. The analytical models are based on semiconductor physics describing the carrier dynamics in the device. In this category, the two most popular models are the Hefner model [23] and the Kraus model [25] which have been implemented in SABER as well as SPICE.

In the behavioural models, IGBT characteristics are fitted using different methods, and the resultant switching functions are then used in an off-line simulator. This approach [27] has been used in an off-line system-level simulation tool (EMTP) to model the device accurately. However, this model still requires very small time-steps to be practically implemented in a real-time simulator based on conventional general purpose processors or DSPs. In [28], the non-linear Hammerstein-like model was proposed and the model parameters are derived from semiconductor physics, but the model is still too complex to implement in the real-time simulation. A device-level real-time model implemented in an FPGA, for an IGBT-based VSC drive was proposed in [9], which takes into account the precise switching times albeit based on linearised device characteristics.

The 'linearised device-level behavioural model' is obtained through the linearisation of the detailed model [9] and its hardware realisation is explained in Section 5. As the characteristics of the IGBT are expressed through a linear function, the reverse recovery, tailing current and other non-linearities at turn-on and turn-off are ignored; however, switching losses and on-state-losses are considered. The 'non-linear device-level look-up table (LUT)-based model' [10, 11] can be constructed from the measured switching characteristics of the IGBT as explained later in Section 4 and its hardware realisation is explained in Section 5. The numerical models utilise finite-element methods to model the carrier diffusion in the device resulting in a very accurate although computationally expensive model.

In this paper, five IGBTs models are implemented on the FPGA for the complete simulation of three-level voltage source converter (VSC)-based induction machine drive: three system-level models (ideal model, switching function model and averaged model) and two device-level models (linearised behavioural model and non-linear LUT-based model).

3 IGBT based test system: three-level 12-pulse drive

3.1 System description

The three-level 12-pulse VSC drive including the closed-loop field-oriented control (FOC) with the squirrel-cage induction motor (SCIM) has been modelled, simulated in real-time and compared using all aforementioned IGBT modelling techniques. The system consists of four main parts: the SCIM, the fast responsive direct field oriented controller, sine-wave pulse width modulation (SPWM) and the VSC. As shown in Fig. 1*a*, we use the two DC power supplies instead of using the capacitors to obtain the stable DC voltage for the system. The motor is modelled using the fifth-order Park's machine model with rotor reference frame. The three-phase currents, rotor speeds and the rotor flux are the feedback signals to the FOC including the reference speed and reference rotor flux. Through the FOC control, the pulse width modulation (PWM) will generate the 12-gating signals for the VSC. The motor and the FOC control have been implemented using the Altera's DSP Blockset and very high-speed description language (VHDL)

doi: 10.1049/iet-pel.2011.0105

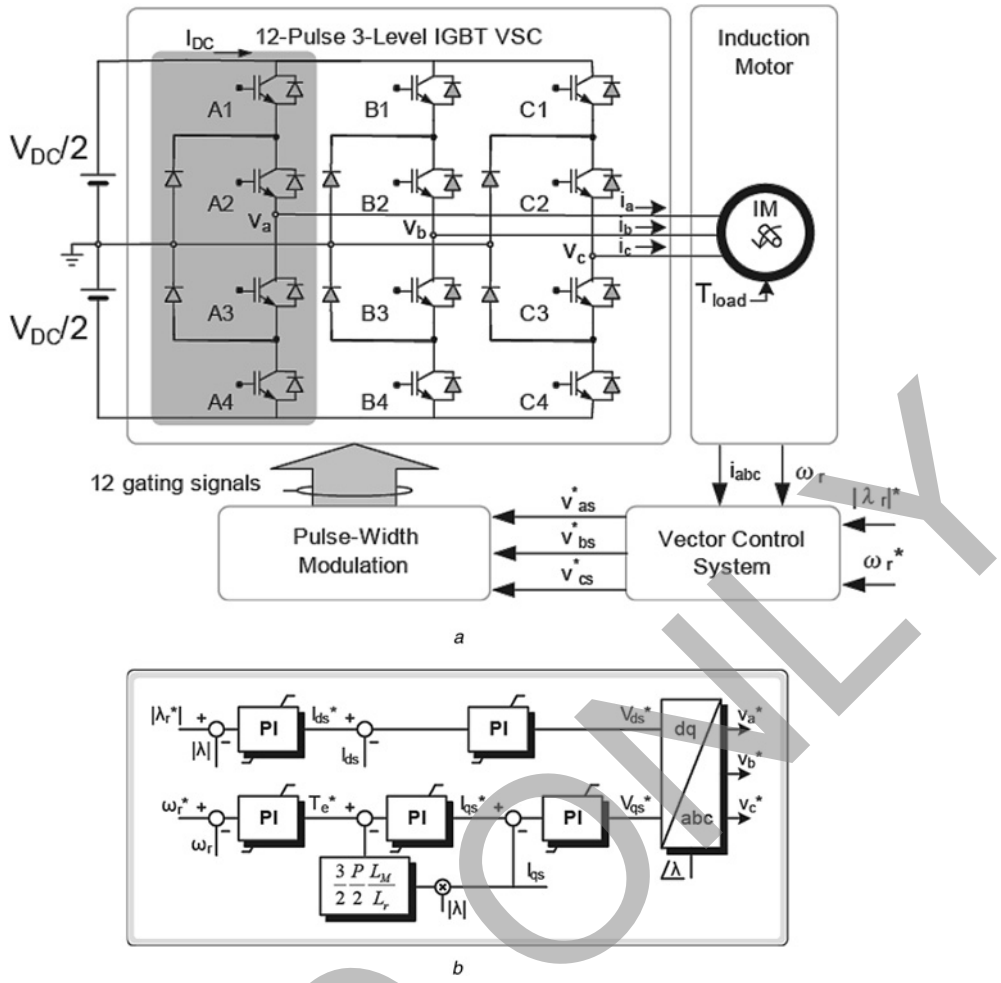

Fig. 1 *Schematics of IGBT based test system*

a 12-pulse three-level VSC induction motor drive (shaded box: one VSC leg)
b FOC for motor drives

codes are generated. The other parts were directly written in VHDL source code.

3.2 Control algorithm

The block diagram of the FOC is shown in Fig. 1*b*. The FOC control is considered in the *dq* reference frame where each axis is 90^0 apart. As a machine output, the speed (ω_r), the rotor flux (λ_r) and currents (i_a, i_b and i_c) are measured. The speed reference (ω_r^*) and flux reference (λ_r^*) are used as the inputs in the controller. From the speed reference (ω_r^*), the torque (T^*) and the stator current (I_{qs}^*) can be calculated. The electrical torque and rotor flux reference signal are obtained from the following equations

$$T_e = \frac{3}{2}\frac{P}{2}\frac{L_M}{L_r}\lambda_r i_{qs} \tag{1}$$

$$\lambda_r = L_M i_{ds} \tag{2}$$

where L_M, λ_r and P are the mutual inductance, the rotor flux and the number of pairs of poles. A proportional-integral (PI) control is implemented for the speed control loop to produce the electrical torque T_e^* and another PI produces the I_{qs}^*. The current controllers of I_{ds}^* and I_{qs}^* can generate the necessary control references of V_{ds}^* and V_{qs}^*. The required control signals, v_a^*, v_b^* and v_c^*, for the SPWM can be obtained from the stationary reference voltages V_{ds}^* and V_{qs}^*. The hardware realisation of the detail control system implementation can be seen in [9].

4 Modelling of IGBT based test system

4.1 System-level models

4.1.1 Ideal model of IGBT: Fig. 2*a* shows the ideal characteristics of IGBT. In the ideal model, the on/off transients of IGBT switching and reverse recovery of diode are neglected (Fig. 2*a*) and the IGBT is considered as an ideal switch. The on-stage and off-stage resistances are replaced by 1 mΩ and 1 MΩ, respectively (Fig. 2*b*). Furthermore, the stray components of IGBTs are not considered. The set of non-linear equations for the IGBT characteristics is replaced by a set of linear equations, which reduce the simulation time greatly for real-time and off-line simulation. The ideal model is the most commonly used approach in system-level simulation.

4.1.2 Switching function model of IGBT: In this approach, the IGBT is replaced by a circuit consisting of only the controlled voltage and current sources that describe the external behaviour of IGBT output voltage v_{ce} and current i_c. The switching function equivalent circuit and its representation for a three-level converter is shown in

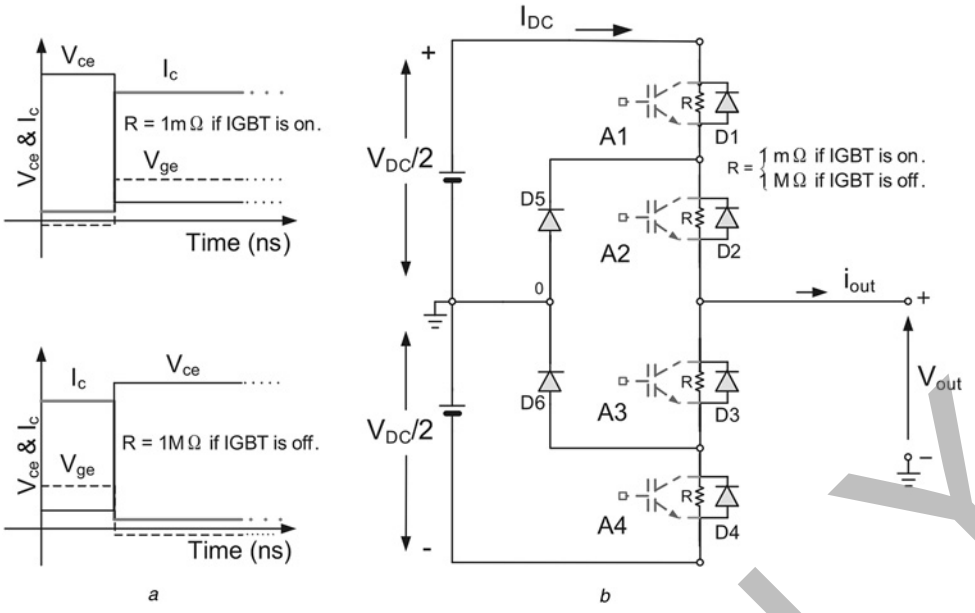

Fig. 2 *Ideal characteristics of IGBT*

a Idealised timing characteristics of an IGBT during turn-on and turn-off switching
b One leg of the three-level converter with ideal models for the IGBTs

Figs. 3*a* and *c*. The relationship between the input and output quantities of each IGBT can be expressed as

$$v_o(t) = f(t) \cdot v_{in}(t) \tag{3}$$

$$i_{in}(t) = g(t) \cdot i_o(t) \tag{4}$$

In the above equations, $f(t)$ and $g(t)$ are the switching functions. In many cases, $f(t)$ and $g(t)$ are related, and one can be derived from the other. From (3) and (4), the equivalent models of the three-level converter circuit in Fig. 1 can be expressed as in Fig. 3. The switching function $f(t)$ in this case is the same as the gating signal for IGBT switch. The relationship between the input voltage, switching function and output voltage can be seen in Fig. 3*b*. Using the switching-function representation, the converter circuit in Fig. 1 can be replaced by the equivalent circuit in Fig. 3*c*. Usually, the switching functions can be

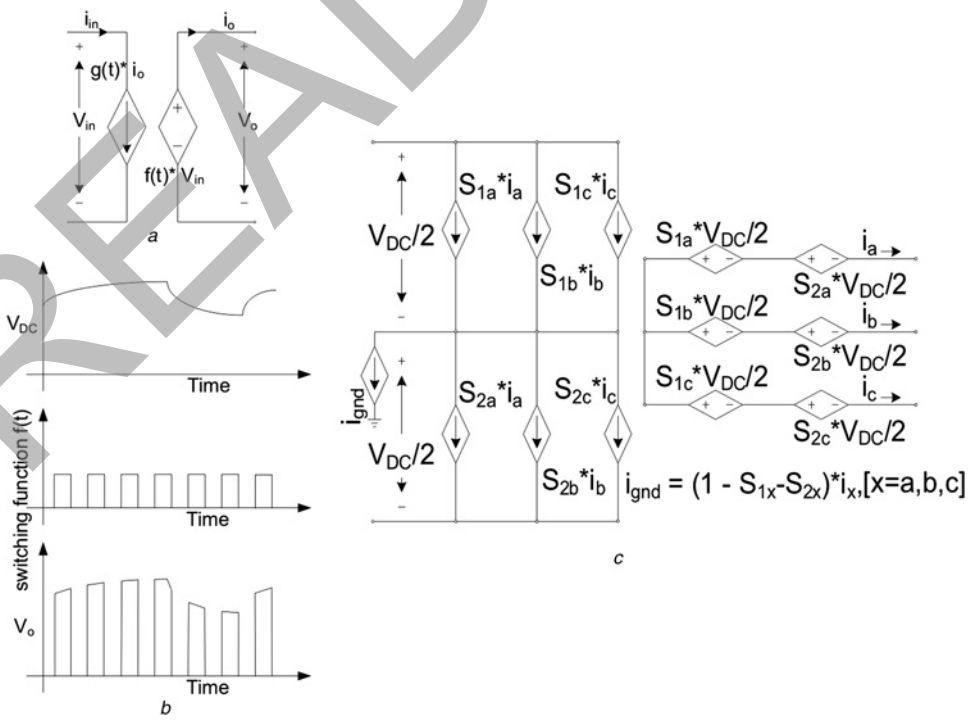

Fig. 3 *Switching function based behavioural model of IGBT converter*

a Equivalent circuit model of switching function for IGBT
b Input voltage, switching function and output voltage
c Switching function model representation for three-level converter

doi: 10.1049/iet-pel.2011.0105

obtained by directly inspecting the converter circuit. The simulation is much faster using the switching-function models. Also, the switching-function approach gives the same results as the ideal-model approach, that is, high-frequency effect is preserved.

4.1.3 Averaged model of IGBT: To develop an averaged model of the converter, the switching function is averaged over one switching period, T_s. Thus, the switching behaviour and harmonic components are excluded. The averaged model operator can be expressed as

$$m_{ij}(\tau) = \frac{1}{T_{PWM}} \int_{\tau}^{\tau+T_{PMW}} h_{ij}(t) \cdot \mathrm{d}t \tag{5}$$

where $i = 1, 0, -1$ and $j = a, b, c$.

In both the ideal-model approach and switching function approach, the high-frequency switchings of the circuits are considered, whereas only the low-frequency components are considered in the averaged model. As an example, in the average-model approach, the switching function $f(t)$ in Fig. 3*a* becomes a DC value (assuming the duty cycle to be 0.5 in this case) and the output voltage v_o has no switching harmonics. The averaged model can be obtained directly by replacing all the switching functions by their averaged counterparts. Since there is no switching and the circuit topology is invariant, the simulation speed can be very fast for this type of modelling.

4.2 Device level models

4.2.1 Linearised device-level behavioural model of IGBT: For the linear model of IGBTs in drive application, the IGBTs are used only in the switched mode. Furthermore, the largest possible value of the gate-to-emitter voltage V_{ge} is used to minimise the conduction loss in this region. In this case, the forward characteristics of the IGBT can be represented by a linear substitute characteristic (Fig. 4*b*), which is given as follows

$$v_{ce,sat}(t) = v_{ce}(t_0) + r_{ce} \cdot i_c(t) \tag{6}$$

where $v_{ce}(t_0)$ $v_{ce}(t_0)$ is the collector–emitter threshold voltage, r_{ce} is the device on-state resistance.

The linearised characteristics of the implemented IGBT model are based on the CM50DU-24F IGBT from Powerex (Table 1) with the timing diagrams shown in Figs. 4*b* and *c*. These data are available from the IGBT manufacturer's data-sheet.

4.2.2 Detailed non-linear LUT-based device-level model of IGBT: Using the measured IGBT characteristics (Figs. 4*d* and *e*), a non-linear device-level model was developed using per-unit scaling and LUT in the FPGA. From the experimental data obtained, it was observed that the rise and fall times for the current and voltage are constant and are proportional to the amplitude of the final value. Therefore the turn-on and turn-off waveforms can be obtained by scaling a per-unit device-level switching function stored in a LUT by the final amplitudes.

Under normal operation of the three-level converter there are five valid switching states for four IGBTs ($A1$, $A2$, $A3$ and $A4$) in each converter leg [11]. For each of these combinations, at every time-step (12.5 ns) of the real-time simulation, the value of the load current i_{out} is used to determine whether the current will flow through the IGBTs or the clamping diodes or the antiparallel diodes.

For example, considering the single converter leg (Fig. 1) assume that at time $t = t_1$, the gating signals for $A1$, $A2$, $A3$ and $A4$ are changed to 1, 1, 0 and 0, respectively. If i_{out} is positive, it will flow through the diodes D3 and D4 for $t < t_1$, and the steady-state output voltage would be $V_{out} = V_{DC2} - 2V_{d(sat)}$, where $V_{d(sat)}$ is the voltage drop across the diode. After $t = t_1 + t_{d(on)}$, $A1$ and $A2$ will start to conduct and i_{out} will flow through the IGBTs to reach its steady-state value of I_c. The output voltage will also rise until it reaches its steady-state value of $V_{out} = V_{DC1} - 2V_{ce(sat)}$.

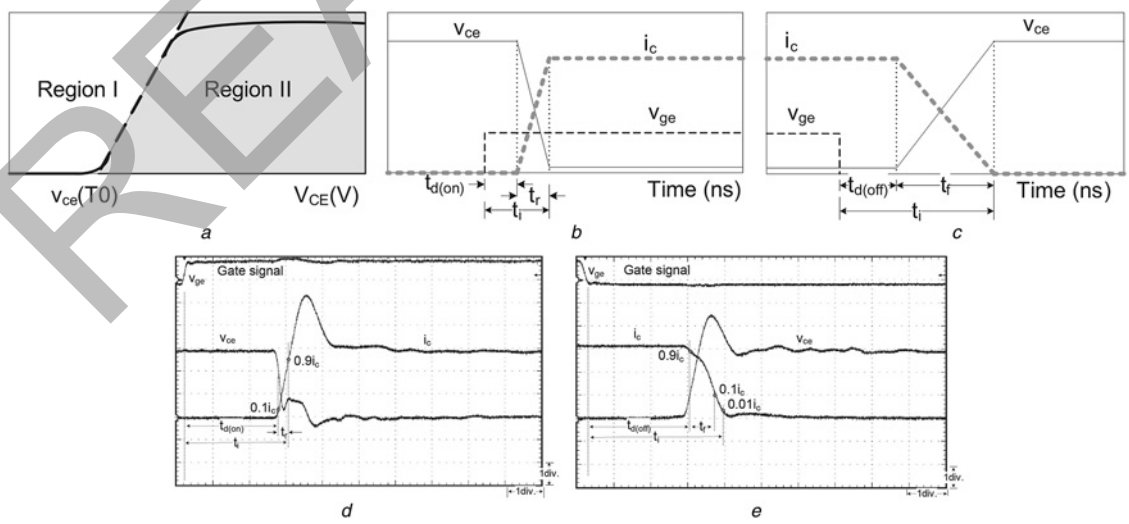

Fig. 4 *Linear behavioural and detailed non-linear model of IGBT*

a VCE-IC curve of a generic IGBT for a specific value of VGE
b Linearised timing characteristics of IGBT during turn-on
c Linearised timing characteristics of IGBT during turn off
d Measured IGBT hard-switching transient waveforms: turn-on
e Measured IGBT hard-switching transient waveforms: turn-off

Table 1 Implemented data for CM100DU-24F IGBT unit from Powerex®

$t_{d(on)}$	100 ns
t_r	50 ns
$t_{d(off)}$	400 ns
t_f	300 ns
$V_{CE_{sat}}$	1.8 V
$V_{d_{sat}}$	1.25 V

During dead-time1 the gating signals for $A1$, $A2$, $A3$ and $A4$ will change to 0, 1, 0 and 0, respectively, and v_{out} would remain the same as before. After the time $t_{d(off)}$ for $A1$, v_{ce} will increase and collector current i_c decreases until it reaches 90% of I_c. Thereafter, i_c falls quickly to reach 10% of I_c which causes the overshoot in v_{ce}. Within the tailing region, i_c falls slowly becoming almost zero, and then gets replaced by the current of clamping diode D5 flowing through $A2$. For the gating pattern 0, 1, 1, 0, the positive current will continue to follow through D5 and $A2$ and $v_{out} = V_{d(sat)} + V_{ce(sat)}$. During dead-time2 for the gating pattern 0, 0, 1, 0, the current will flow through the antiparallel diodes D3 and D4, and $v_{out} = -V_{DC2} - 2V_{d(sat)}$. When the gating pattern changes to 0, 0, 1, 1, the positive current will continue to flow through D3 and D4, when the steady-state output voltage will be $v_{out} = -V_{DC2} - 2V_{d(sat)}$.

On the other hand, if i_{out} is negative, and assuming that the gating signals for $A1$, $A2$, $A3$ and $A4$ were equal to 1, 1, 0, 0 at time $t = t_1$, the current would flow through the diodes D1 and D2 for $t < t_1$, and at $t = t_1$, it would continue flowing through the same diodes resulting in $v_{out} = -V_{DC1} + 2V_{d(sat)}$. During dead-time1 with the gating pattern 0, 1, 0, 0, v_{out} will be same as before. For 0, 1, 1, 0, the negative i_{out} will flow through $A3$ and D6 resulting in $v_{out} = V_{ce(sat)} + V_{d(sat)}$. During dead-time2, v_{out} will remain the same as before. Finally, when the gating pattern 0, 0, 1, 1 occurs, i_{out} will go through A3 and A4 with $v_{out} = -V_{DC2} + 2V_{ce(sat)}$.

When i_{out} is equal to zero, the steady-state value for the output voltage will be V_{DC1}, 0, or $-V_{DC2}$ depending on the gating pattern.

5 FPGA implementation of models

The hardware realisation of the system model has been the straightforward implementation on an FPGA chip. It is divided into four parts that include the three-level VSC, the induction motor, the direct-field oriented controller and SPWM.

5.1 Three-level VSC hardware realisation

This section describes the hardware implementation of the system-level IGBT models and the device-level IGBT models for three-level VSC. The implementation was done entirely in VHDL.

5.1.1 System-level model hardware realisation: The overall hardware realisation (Fig. 5*a*) of the VSC using the three system-level IGBT models (ideal, switching function and averaged) is basically the same except for the IGBT model itself. The DTC1 and DTC2 are counters to include dead-time for $A1$ and $A2$ switch. The three-level VSC model was then constructed by duplicating this design for the single leg.

5.1.2 Linearised device-level model hardware realisation: The FPGA realisation of the single leg of the three-level VSC using a linearised device-level IGBT model is shown in Fig. 5*b*. Instead of receiving the four gating signals, the model receives only the two gate signal for the switches $A1$ and $A2$. These gating signals go through a block that adds the dead-time and then generates the four gate signals for $A1$, $A2$, $A3$ and $A4$. This approach was chosen to simulate the presence of the IGBT gate drivers, which add the dead-time after the PWM generation. With the gating signals, V_{DC1}, V_{DC2} and I_{out} as inputs, the model then implements a state machine with eight states, one for each possible combination of the switches. In each state, the output current value of the leg is verified in order to determine the path of current flow. The state machine interacts with the counters responsible for modelling the time turn-on delays $t_{d(on)}$, turn-off delay $t_{d(off)}$, rise time t_r and fall time t_f, generating control signals that drive these counters. The counter outputs are used to determine the output voltage with respect to the ground terminal of dc bus. The model also outputs the current I_{DC} through $A1$, $A2$ or D1, D2, which could be used to determine the output current of the DC link.

The single leg model was duplicated to make the three-phase three-level VSC model. The inputs to the VSC model are the three phase currents, two DC voltages and six gating signals with their complements. The outputs of the model are the three-phase voltages V_a, V_b and V_c, and the current I_{DC}. All model variables are chosen as signed fixed point numbers except for the gate signals, which are single bits. The number format for all model voltages and currents in the FPGA implementation was 19.5, that is, 19 bits are used to represent the integer part, and five bits are used to represent the fractional part.

5.1.3 Non-linear LUT-based device-level model hardware realisation: The FPGA realisation of one-leg of the three-level VSC using a non-linear device-level IGBT model is shown in Fig. 5*c*. For the non-linear model, the measured per-unit IGBT switching characteristics were implemented at a resolution of 12.5 ns in a LUT of the ROM on the FPGA board and then the behaviour model was generated. 'Altsyncrams' from the mega-function library of ALTERA are used with one read port in the ROM mode. To obtain the non-linear IGBT characteristics, ROM is used to implement a combinational logic circuit, which converts a 7-bit number to the corresponding non-linear characteristic signal. At each time-step, the appropriate IGBT characteristic is read from the LUT based on the gating signals. Depending on the address and clock frequency, the accurate per-unit IGBT characteristic can be read and converted to the outputs of $v_{ce}(t)$ and $i_c(t)$, and then changed to the instantaneous output voltage v_{out} and current I_{DC} exactly depending on the inputs I_{out}. Therefore the output result values are the instantaneous current and voltage (within the nanoseconds range) that are shown accurately.

For this model of the IGBT, there are four LUTs to implement the IGBT characteristics of $V_{ce(on)}$, $V_{ce(off)}$, $I_{c(on)}$ and $I_{c(off)}$. From those characteristics of IGBT, the instantaneous V_{ce} and I_c can be calculated. For example, when the gating signal is on, the IGBT characteristics of $V_{ce(on)}$ and $I_{c(on)}$ are read. The ROM can be initialised using a Memory Initialisation File (.mif), which can be created using a simple text editor.

doi: 10.1049/iet-pel.2011.0105

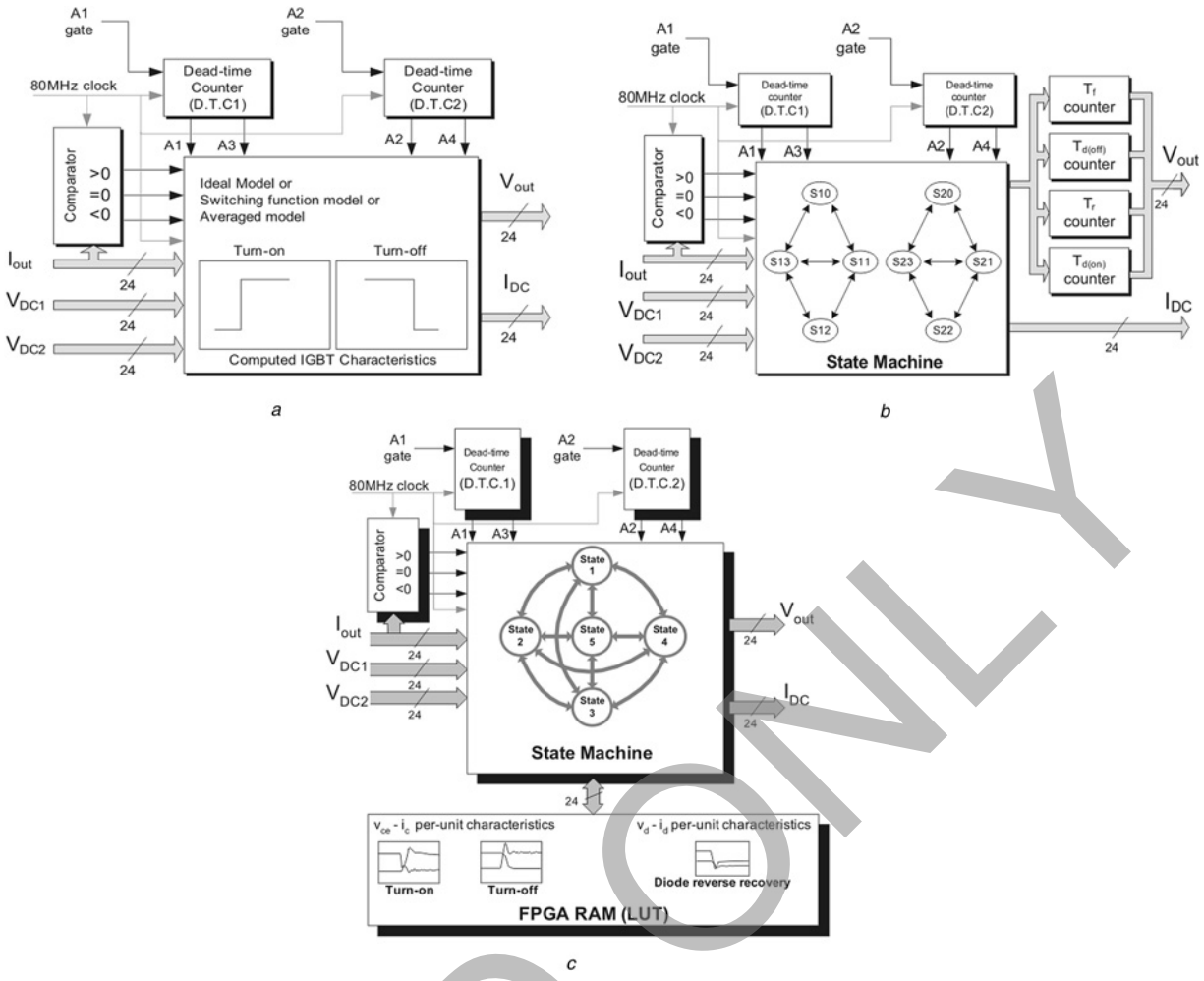

Fig. 5 *Functional block diagram of the hardware realisation of one leg of three-level VSC using*

a System-level models
b Linearised device-level IGBT model
c Non-linear device-level LUT-based model

After the model of one leg of the converter was built, it was duplicated to build the other two legs to implement the three-phase VSC. The overall VSC model requires as inputs, the three-phase currents, the DC voltage and the six gating signals. The outputs of model are the three voltages V_a, V_b and V_c with respect to the ground bus and the current I_{DC}. All the variables are considered as being signed fixed point numbers except the gate signals which are single bits. The number format for the input and output variables are that 19 bits are used to represent the integer part of the number and 5 bits are used to represent the fraction part.

The internal variables of the model usually have more fractional bits than the input/output variables in order to preserve the resolution of the simulation calculations. The developed model considers that in one simulation time-step there is no change in the current signal. This is a valid assumption since the time-step chosen for the VSC model was 12.5 ns.

5.2 Induction machine hardware realisation

The fifth-order Park's machine model has been used to represent the induction machine [29]. This model was implemented using the Altera's DSP Blockset that generated the VHDL source code. The sample time for the motor is 10 μs. In the induction motor, the torque T^* and the three phase voltages are inputs, and the currents, speed and electrical torque are outputs. The machine model was discretised for the hardware realisation by using the 'Trapezoidal' rule. The non-linear model of motor was implemented by using the arithmetic function DSP blocks such as subtractors, adders and multipliers, etc.

The complete FPGA hardware implementation of this machine model is described in [9]. In addition to the stator and rotor current components, the model also outputs the rotor flux magnitude and position, which are used to implement the FOC in the next section.

5.3 Direct field oriented controller and SPWM hardware realisation

For the direct field oriented controller, the three-phase currents, the rotor flux and the speeds of motor are considered as inputs. Speed and rotor flux are the two references in the system. By using the PI controller, FOC generates the controlled signals v_a^*, v_b^* and v_c^*. These control signals go to the STPWM.

The fraction and integer parts of results are 5-bits and 19-bits wide, and are used in order to calculate the adequate accuracy for the output voltages and currents. The internal variables have more fractional bits than inputs and outputs to obtain more precision results.

In the SPWM hardware implementation, the carrier frequency for the PWM is 8 kHz (125 μs), while the controller sampling frequency is 16 kHz (62.5 μs). Two synchronised triangle carriers are compared with the control signals (v_a^*, v_b^*, v_c^*) to generate the necessary switching signals.

Once the control signals values are sampled, they are transformed to the three-phase system v_a^*, v_b^* and v_c^*. The comparison with control signals and the carrier waves will generate the six gating signals with respect to the two channels for each phase. The carrier waveforms are generated at a resolution of 12.5 ns in the FPGA with the 16-bit up-down counters. The 'Sync' signal is used to synchronise the carrier waveform to the control waveform. The 'reset' signal resets the counters at the top and bottom limits of the carrier signal. The gating signals coming from the SPWM need to include the dead-time. Each gating signal passes through the dead-time (2 μs in this case) to avoid the DC short circuit and to reduce the IGBT stress and generate its complementary signal. Therefore the total of 12 gating signals are obtained for three VSC legs.

6 FPGA resources

In this paper, the Stratix III EP3SL150 FPGA development board from Altera was used to implement the system components. It includes adaptive logic modules (ALMs) and high performance, flexible memory and DSP blocks to meet system's most demanding requirements. The I/O banks and external memory interfaces make design process easier, and security features keep the designs secure. The main features of this FPGA are; 57 000 ALMs, 142 500 logic elements (LEs), 355 M9 K memory blocks, 16 M144 K memory blocks, 5499 embedded memory (Kbits), 1775 MLAB (Kbits), 384 18 × 18 Multipliers, 8PLLs and 736 maximum user I/O pins.

A digital-to-analogue board, THDB ADA card from Terasic was interfaced with the Stratix III board. On-board dual seven-segment display can be used to show the completion of the downloadable SRAM object file (SOF). By using the ByteBlaster II cable, the SOF file can be downloaded to the board for real-time simulation. One eight-pin (DIP) switch and three user-definable sliding button switches are used as the interface of human and machine. For the system reset, one of three user-definable sliding button switches (SW0) is used. The others are set to reverse and increase/decrease the speed of the motor. The DIP switches are used for two D/A outputs management, and the load T_L applied to the induction motor.

The FPGA logic resources utilised in the Stratix III device for the entire system implementation are shown in Table 2. Note that there are five IGBT models with different usages of LEs and memory bits. The linear model consumes the most LEs because it is a direct function of the IGBT gating signals, whereas the other models use the ALMs. The non-linear IGBT model has the largest usage of memory bits for storing the IGBT switching characteristics in the ROM. The induction machine model uses more than half of the LEs of the whole system.

7 Results and discussion

In this section, results are presented from the real-time simulation and compared with off-line simulation of the three-level VSC variable speed AC drive for validation purpose.

7.1 Off-line validation for real-time simulation

The off-line simulation, using two well-known simulation programs, SABER and SIMULINK, was carried out with an objective of validating the real-time simulation of the variable speed AC drive. A co-simulation environment was set up by interfacing the three-level converter and PWM modelled in SABER with the rest of the system (machine and controller) modelled in MATLAB/SIMULINK. A non-linear model of the IGBT1 and diode was used in SABER to model the three-level VSC.

For modelling the VSC in SABER, igbt1 model was used. This is a non-linear behavioural computational model [26]. The steady-state and transient results were recorded and then compared. The comparison reveals high degree of similarity among the results obtained through both simulation environments with minor discrepancies. The SABER simulation runs at 12.5 ns, whereas the interfaced MATLAB/SIMULINK simulation runs at 10 μs.

7.2 IGBT switching characteristics

The IGBT switching characteristics for the system-level and device-level models are shown in Fig. 6. The characteristics for all system-level models are the same except for the averaged model. As shown in Figs. 6*a* and *b* for the switching function model, the IGBT transients only include simple on and off without any time delays or non-linear transients. It can be clearly seen that there is no turn-on delay $t_{d(on)}$, or turn-off delay $t_{d(off)}$ and there is a straight forward relationship with the gating signals.

Table 2 EP3SL150 FPGA resources used by the system components

Component	ALMs	LEs	DSPs	PLLs	Memory bits
VSC (ideal)	7616	0	60	0	0
VSC (switching function)	6595	0	0	0	0
VSC (average)	6745	0	60	0	0
VSC (linear device-level)	1716	10 790	0	0	0
VSC (non-linear LUT)	1098	0	60	0	17 920
induction machine	2733	12 314	130	0	0
controller	564	3095	69	0	0
STPWM	102	552	0	0	0
measurement system	31	150	8	0	0
D/A interface	52	255	0	0	0
total usage	27 252	26 627	259	1	17 920

doi: 10.1049/iet-pel.2011.0105

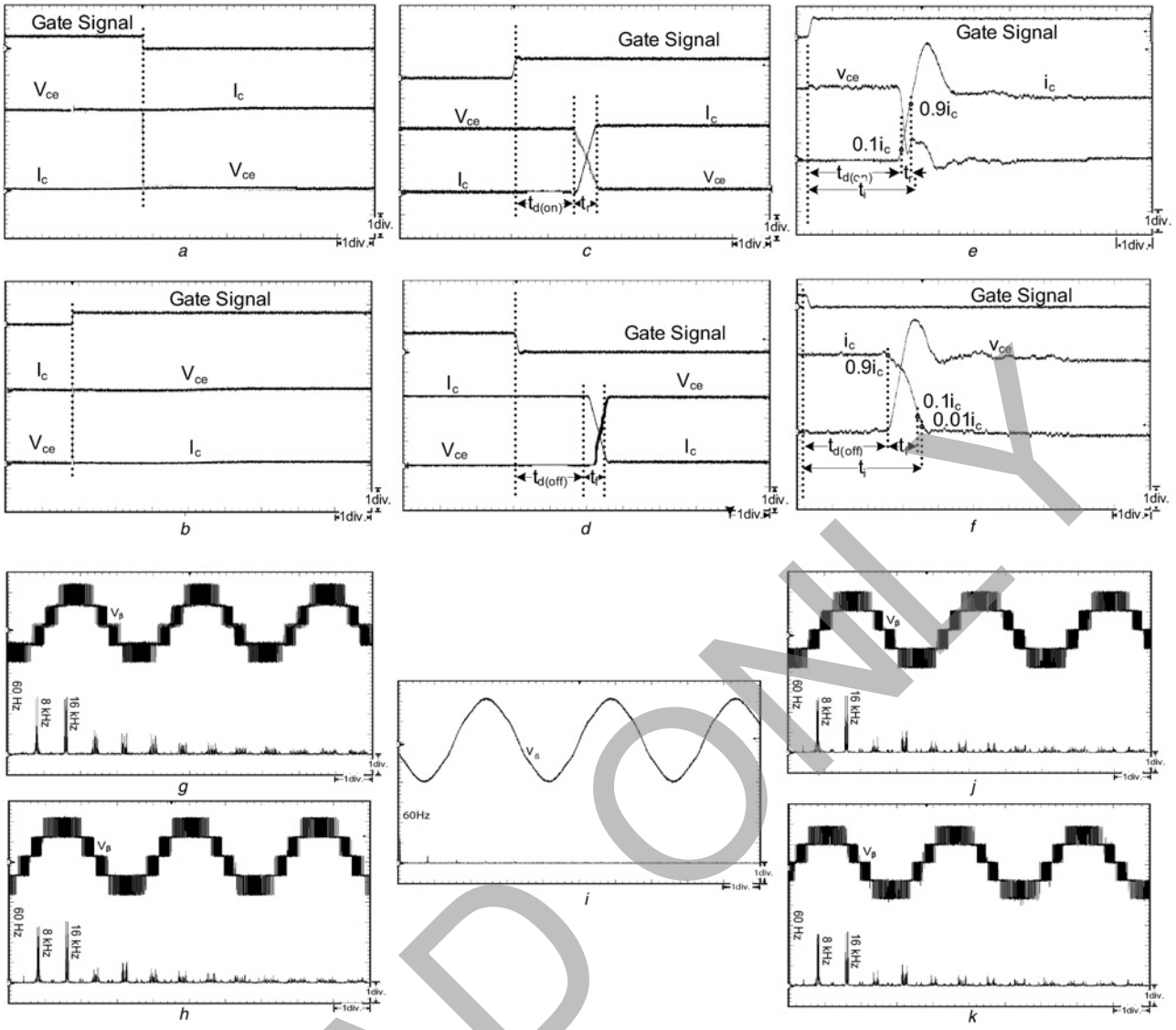

Fig. 6 *Real-time simulation results of various IGBT models*

a and *b* Idealised system-level models
c and *d* Linearised device-level model
e and *f* Non-linear LUT-based model
g Output voltage waveform of three-level VSC: ideal IGBT model
h Output voltage waveform of three-level VSC: switching function model
i Output voltage waveform of three-level VSC: averaged model
j Output voltage waveform of three-level VSC: linearised device-level model
k Output voltage waveform of three-level VSC: non-linear LUT-based model

For the linearised device-level IGBT model simulation, we can notice in Figs. 6*c* and *d* that there are turn-on $t_{d(on)}$ and turn-off delay $t_{d(off)}$, and the rise time t_r and fall time t_f of IGBT. In Figs. 6*e* and *f*, we can see the non-linear characteristics of IGBT obtained from the non-linear LUT-based device-level model.

7.3 Steady-state results

For steady-state analysis, the system has been simulated for a few seconds; however, the results are shown for shorter periods because of the larger amount of data as well as the clarity of the figures. There were some initial transients that subsided very fast and the system reached steady state thereafter.

Figs. 6*g*–*k* show the steady-state waveforms of the v_β voltages and the harmonics spectrum of the voltages at the inverter frequency of 60 Hz. As expected, all voltages are very similar in all cases and the differences only appear in the averaged model. For the averaged model, the FFT calculation result of switching frequency components is very small compared with other models.

All figures show the output voltages of VSC after the induction machine reaches its steady state with $\omega_r^* = 377$ rad/s. In these figures, it is possible to observe that the typical three-level voltages are present in the converter phase voltage. The FFT calculated by the oscilloscope shows a fundamental frequency component at $f = 60$ Hz. Other significant components are the sidebands centred at $f_c = 8$ kHz and $f_c = 16$ kHz, since the PWM frequency is equal to 8 kHz. The line voltage magnitudes for various IGBT models are given in Table 3.

A comparison of steady-state results from the real-time simulation and the off-line simulation is shown in Figs. 7*a*

Table 3 Line voltage magnitudes for various IGBT models

IGBT model	V_{ll}(peak) V	60 Hz, %	8 kHz, %	16 kHz, %
ideal	750	100	16	16
switching function	750	100	17	20
averaged	750	100	5	3
linear	750	100	14	16
non-linear LUT	750	100	12	13

and *b*, respectively. These two figures show the inverter line voltage, the machine line current, and the FFT of the line voltage. Both sets of results are quite comparable. The current distortion in off-line simulation and jitter of the waveform is attributed to the use of higher time-step used for modelling the machine and control system. One the other hand, the line current found from real-time simulation is quite smooth and sinusoidal because of the very small time-step used in FPGA-based simulation.

7.4 Transient results

The transient results are shown in Figs. 7*c* and *d* from the real-time simulation and the off-line simulation, respectively. The transient results are the same regardless of the IGBT models used in VSC because they are system level. Results are shown for the machine speed ω_r, the speed reference ω_r^*, and the currents i_α and i_β when the machine is subjected to the following transients:

1. the startup of machine with speed set-point of 150 rad/s at t_1,
2. the speed set-point variation to 377 rad/s at t_2,
3. the application of 100 N.m load at t_3 and removal of the load at t_4, and
4. the speed reverse to −377 rad/s at t_5.

As can be observed from the machine torque and speed, the controller has a stable and fast performance during the transients and no perturbation can be seen in the speed during the application or removal of the load. As the machine was modelled by ignoring the mechanical losses, and the machine resistances are quite small, during the transients, the converter must supply or absorb the power consumed or generated by the machine as a function of the controller action. It is also possible to observe that the frequency variation of the currents and voltages during the applied load, speed-up and speed reversal.

8 Application guideline

The key to a successful simulation is to identify the need for simulation and then choose the right model and simulation platform (off-line or real-time). There are many modelling and simulation tools for modelling and simulation of power electronics circuits. Some software tools employ detailed model (SPICE, SABER, etc.), and are suitable for monitoring individual device characteristics; on the other hand, some are for evaluating system-level performance. Since the detailed models are constructed to represent the actual physics as close as possible and they represent the most accurate analysis of switching characteristics and IGBT power losses, they can be used for low-rated power electronics circuits. Because it is a computationally exhaustive modelling and simulation approach, its application cannot be justified for high power and large circuits. However, a detailed model of IGBT may provide

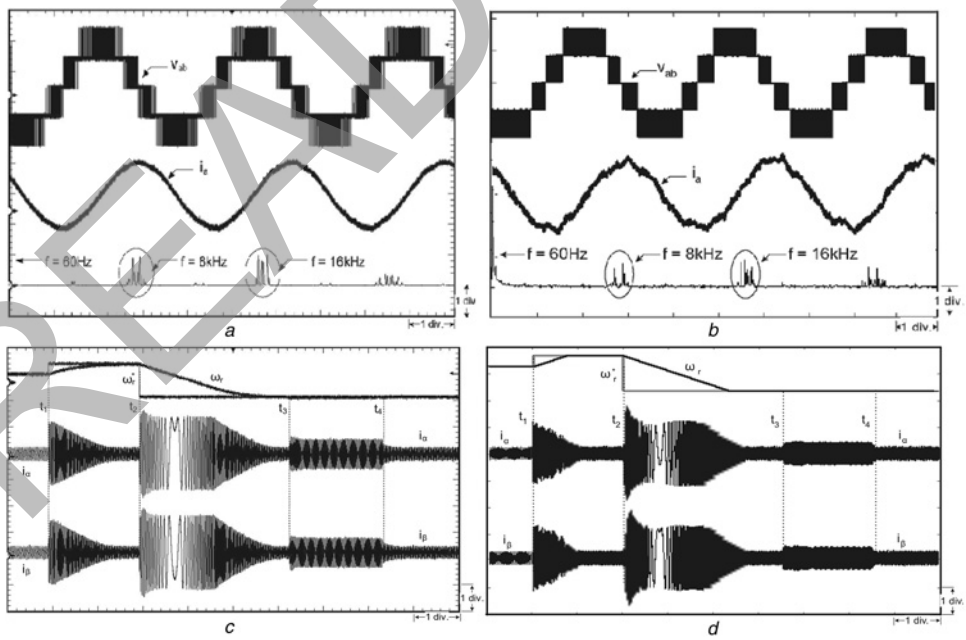

Fig. 7 *Comparison of steady-state results for the line voltage v_{ab} and line current i_a applied to the machine and harmonic spectrum of v_{ab} (scale, v_{ab}: 350 V/div.; i_a, 20 A/div.; time, 5 ms/div.)*

a Real-time simulation oscilloscope trace, and
b Off-line SABER/SIMULINK simulation
Comparison of transient results of reference speed ω_r^*, machine speed ω_r and currents i_α, i_β for: machine running at 150 rad/s and speed set-point variation to 377 rad/s at t_1, speed reversal to −377 rad/s at t_2, application and removal of load at t_3 and t_4, respectively. (scale, ω_r^*; ω_r, 630 rad/s/div.; i_α and i_β, 150 A/div.; time, 1 s/div.)
c Real-time simulation oscilloscope trace
d Off-line SABER/SIMULINK simulation

doi: 10.1049/iet-pel.2011.0105

the most accurate results; it may be redundant for some studies. For example, an IGBT used in the VSC-HVDC and FACTS controllers does not require a detailed modelling, where the objective of the study is to understand the system-level dynamics. Similarly, when it comes to low-voltage and low-power switching applications, a detailed modelling of the device may be a prerequisite where study of the switching transients, power losses and thermal characteristics of the device is a major issue. In special cases where thermal stress is of great concern (such as in an electric ship), study using detailed model may be necessary for high-power devices and circuits as well.

System-level simulation uses the behavioural modelling employing idealised and simplified characteristics. The behaviour mode simulation only gives a good prediction of the circuit performance. Hence, it is not possible to estimate the losses of the devices. It is suitable for concept verification, sensitivity analysis, control-loop design, component rating calculation and other system-level studies. In this category, the issues of interest are the network behaviour of the power electronic apparatus and its impact on the power system, such as injected voltage and current harmonics, machine dynamics and controller performance, etc. A good simulation strategy is to use the behaviour mode simulation at the beginning of the design stage or for the over all system analysis and then use the detailed mode simulation at a later stage or for the detailed analysis of individual devices or for a small portion of the circuit.

9 Conclusions

This paper compares the FPGA implementation of five different IGBT models applied in the modelling and simulation of a three-level, 12-pulse drives system. Both system-level and device-level modelling techniques were implemented in the exercise. System-level model employs ideal, switching and averaged model, whereas detailed model use both linear and non-linear models of the IGBT. The IGBT switching characteristics for linear model was obtained from the IGBT catalogue, whereas for non-linear model, the characteristics were obtained through experimental measurements. The complete drive system including its control was modelled in a fast FPGA (Startix III) using VHDL code and was simulated in real time. The real-time results were validated against SABER and MATLAB/SIMULINK software.

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