makes jitter measurement and analytical analysis difficult [18]. Only some basic guidelines to jitter reduction will be offered.

Jitter results from noise modulating the effective threshold level. One approach to jitter reduction is to reduce the circuit noise using traditional low noise design techniques [34,26]. These techniques rely on the reduction of the noise sources. Another approach to the problem is from a topological point of view. Due to the nonlinear nature of the multivibrator, V_C, the capacitor voltage only affects the threshold circuit when it is near a threshold level. Therefore, by increasing the rate at which the capacitor voltage approaches the threshold, less time is spent in the region where it is vulnerable to corruption by noise and jitter is reduced. This is the technique used by Wakayama [12] to achieve a jitter of < 100ppm. For a given frequency, the slope of the capacitor voltage can be increased by increasing V_{HYST}. For low jitter CCOs both techniques should be applied.

Another source of frequency jitter is from rapid variations in the supply voltage due to noise on the supply lines or poor regulation. To the first order, the Piskarev multivibrator is immune to power supply variations since the hysteresis voltage in independent of V_{CC}. But second order effects such as the finite output impedance of the current sources and mirrors, plus the resistive divider formed by R_1, R_2 allow supply variations to enter the circuit and contribute extra noise to the circuit. The most effective means of reducing the effects of supply variations is external to the circuit and involves ensuring adequate decoupling of supply lines, separation of digital

and analog supplies, and providing good supply regulation.

4.6 Choice of Hysteresis Voltage

The choice of the hysteresis voltage, V_{HYST}, is a compromise between minimizing switching delays and improving stability. For a given frequency, jitter can be reduced by increasing V_{HYST} so that the rate at which V_C approaches the threshold is increased, this requires that V_{HYST} be made as large as possible. Switching delays depend largely on the amount of voltage the parasitic nodal capacitance must be charged/discharged through (plus the amount of charging current available). Reduced delays dictate that small signal swings be used throughout the circuit, therefore V_{HYST} should be kept small. The optimal balance of stability and speed will be determined by the intended application of the CCO.

4.7 Modifications

Applications of CCOs are many and varied; each places different emphasis of the various criteria such as linearity, range, stability, and size; no one CCO design is, therefore, the best for all applications. Some modifications to the basic Piskarev multivibrator will now be presented that allow it to be fine-tuned for its intended use.

4.7.1 Buffer Stage

An important modification to the basic Piskarev multivibrator is addition of a buffer stage to the threshold circuit to reduce the output on this critical stage. A simple buffer which

makes full use of the circuit topology is shown in Fig. 4.5 and consists of M13 to M17. If additional drive capability is required, the output of this stage can be used to drive further inverter stages until the desired drive capability is achieved. By proper design of the inverters' *W/L* ratios, i.e. the ratio should grow by a factor of e (≈ 2.7) between stages, increased drive capability can be achieved with minimum delay [27].

The addition of the buffer stage increases the capacitive loading at the drain of M2 resulting in increased switching delays for the threshold circuit. To reduce the capacitive loading, M16 should be kept relatively small compared to M3 and any additional drive required for the ouput should be obtained through additional inverter stages.

The output of the buffer stage swings from rail to rail, but since it is not in the signal path of the threshold/charge circuit, the increased switching delays due to the large swings will not be detrimental to the circuit's performance (maximum output frequency is, however, limited by the buffer delays).

4.7.2 Using Buffer Output to Control Charge Circuit

In the basic Piskarev multivibrator the maximum charge current is limited by the requirement that (from 4.19)

$$I_C \leq I_T \frac{\beta_{nC}}{\beta_{nT}} \qquad (4.25)$$

This condition must be met to ensure that the switching voltage across the threshold differential pair is adequate to completely switch the charge circuit differential pair.

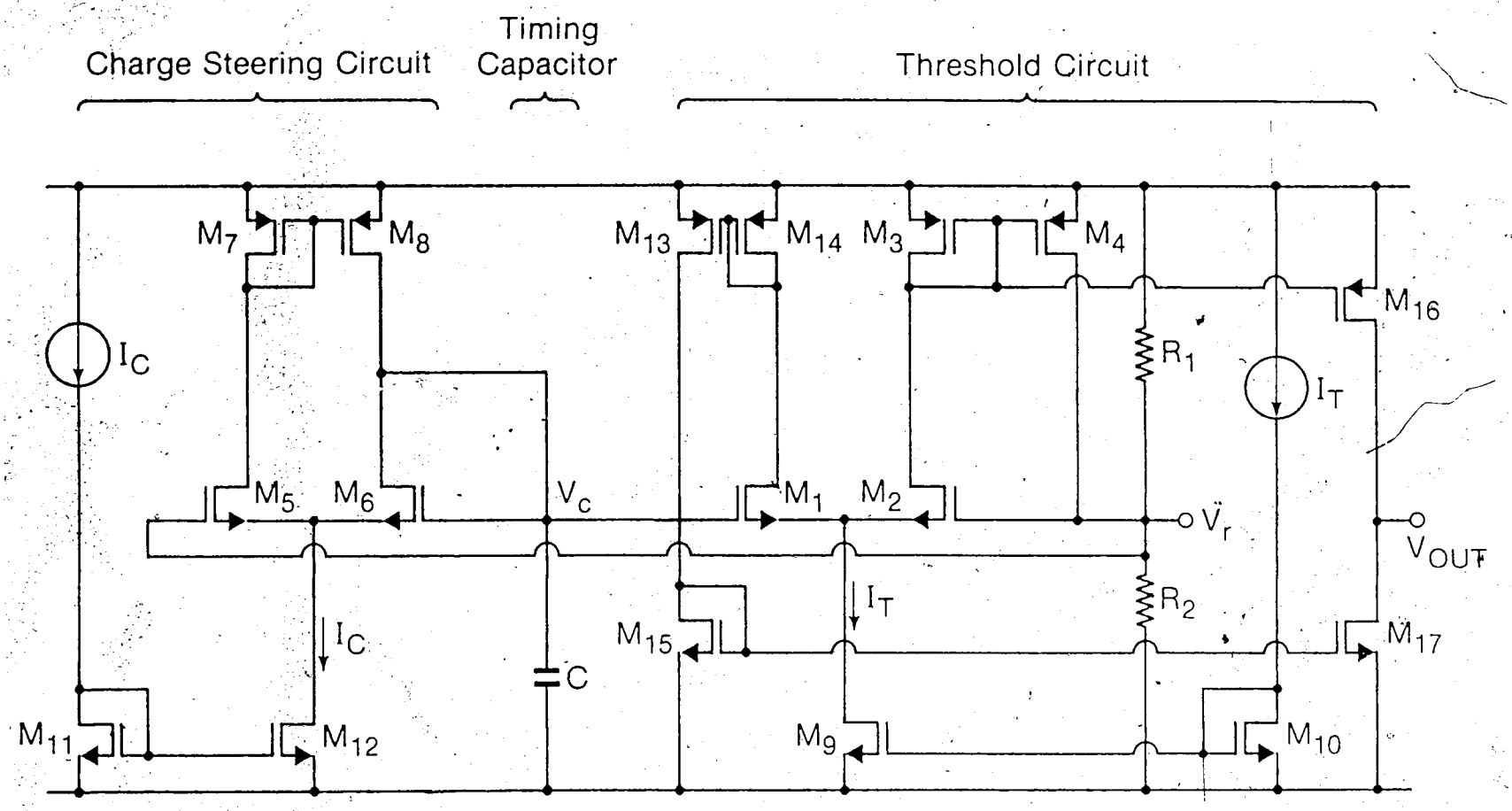

Figure 4.5 Piskarev Multivibrator with Buffer Stage

Increased range for the charge current can be obtained by moving the gate of M5 from M2 to the output of the buffer stage (drain of M17) as shown in Fig. 4.6. This provides a greater voltage swing with which to switch the charge circuit differential pair. Now, the entire charging current can be switched if the following expression is satisfied:

$$\beta_{nC} (V_{GND} + V_{TH,LOW})^2 \geq I_C \leq \beta_{nC} (V_{CC} - V_{TH,HIGH})^2 \quad (4.26)$$

A further increase in the charge current range can be obtained by using a buffer stage, which inverts the output signal, and using this to drive the gate of M5, while the gate of M6 is driven by the capacitor voltage. The condition for full switching of the charge differential pair now becomes:

$$\beta_{nC} (V_{GND} + V_{TH,HIGH})^2 \geq I_C \leq \beta_{nC} (V_{CC} - V_{TH,LOW})^2 \quad (4.27)$$

It should always be checked that the circuits are still operating in pinchoff at the desired current level.

The use of the buffer output to drive the charge differential pair introduces additional switching delays which will degrade the high frequency performance. The current control range, however, will be increased.

4.7.3 Single Supply / Split Supply Operation

The Piskarev multivibrator can be operated with either a single or split supply. The choice is often determined by the availability of split supplies in the intended application. If split supplies are

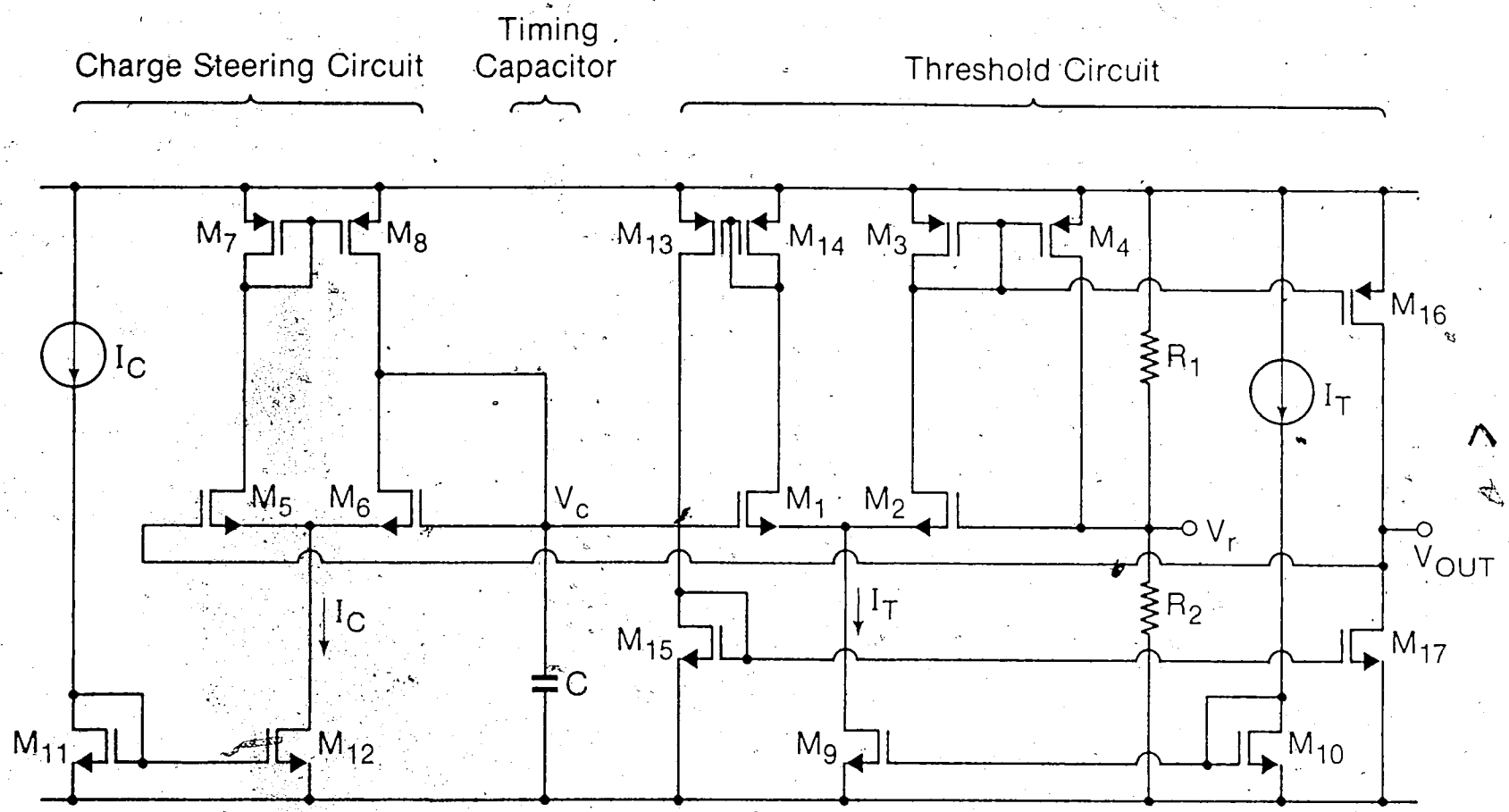

Figure 4.6 Piskarev Multivibrator with Buffer Stage Controlling Charge Steering Circuit

available, then the chip area required to implement the threshold resistors can be reduced.

The only modification to the basic Piskarev multivibrator for split supply operation is the replacement of the resistive divider network formed by R_1, R_2 with a single resistor of value $R_{SS} = R_{eq}$ connected to *GND* (Fig. 4.7). Maintaining the same signal swing at V_r, and assuming constant I_T, the total resistance required by the split supply circuit will be reduced by a factor of four compared to the single supply version. A four fold decrease in the chip area required for fabricating the required resistors is achieved by using of split supplies. The savings in area can be significant. Consider fabricating a 1kΩ resistor using 50Ω/square diffusion [25], this would require 20 squares or an area of 200x10 μ^2 if 10μ squares are used.

If the total area consumed in fabricating the resistors is held constant, then for the same V_r swing, the threshold bias current, I_T, can be reduced by a factor of four. Such a measure reduces power consumption and increases the hysteresis voltage (for the same V_r swing) which, in turn, helps reduce jitter.

4.7.4 Current Mirror Gain

Small switching delays dictate that the swing of V_r be kept small, whereas low jitter requires V_{HYST} to be large. In the basic Piskarev multivibrator the hysteresis voltage is given approximately by

$$V_{HYST} \approx R_{eq} I_T - 2\sqrt{\frac{I_T}{\beta_{nT}}} \qquad (4.28)$$

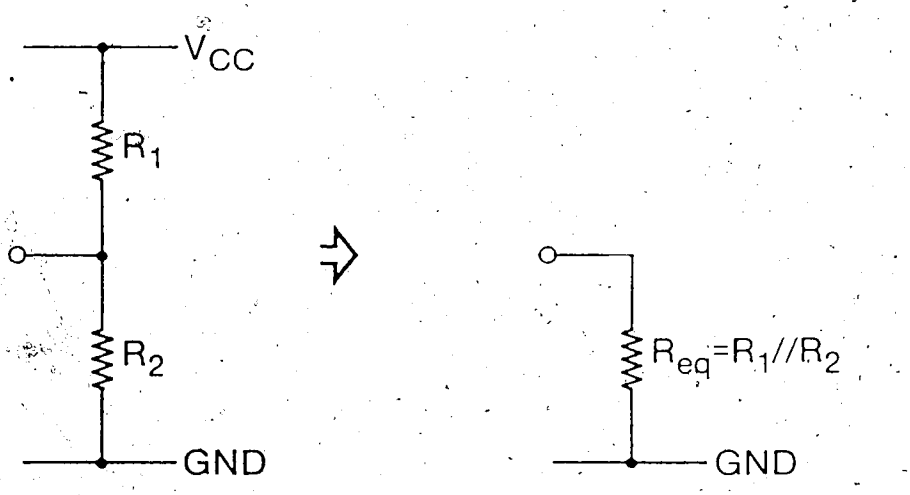

Figure 4.7 Threshold Setting Resistor(s) Configurations for Single & Split Supply Operation

and the swing of V_r is given by

$$V_{r,swing} = R_{eq} I_T \tag{4.29}$$

In order to increase the hysteresis voltage without increasing the swing of V_r the gain coefficient β_{nT} of the threshold differential pair could be increased, which means increased device size for M1 and M2. Alternatively, the threshold current, I_T, can be reduced while increasing R_{eq}. This increases the area required for fabricating the resistors.

An alternate method is to provide current gain in the current mirror formed by M3 and M4. Let

$$\left(\frac{W}{L} \right)_4 = A \left(\frac{W}{L} \right)_3 \tag{4.30}$$

where A is the current gain. Now, the effective threshold current through the differential pair can be reduced by a factor of A thereby increasing the hysteresis voltage without affecting the swing at V_r. Since the size of only one device is changed, the area increase will typically be less than that required to increase the β of M1 and M2, or the size of the resistors. The decrease in I_T will reduce the control range, unless the charge differential pair is driven by the buffer output as discussed previously.

Increasing the size of M4 will increase the capacitive loading on the drain of M2 and so some increase in switching delay is expected. The benefit of decreased jitter should outweigh the increased delay for most applications.

4.7.5 Voltage Gain at Input to Threshold Circuit

Another method for increasing the hysteresis voltage without increasing the swing at V_r is to provide voltage gain between the timing capacitor and the input to the threshold circuit. This is illustrated in Fig. 4.8 using a comparator. The hysteresis voltage will be given by

$$V_{HYST} \approx R_{eq} I_T - \frac{2\sqrt{I_T / \beta_{nT}}}{A_v} \approx R_{eq} I_T \qquad (4.31)$$

if A_v (the voltage gain of the comparator) is large. The hysteresis voltage is equal to the swing of V_r. Unfortunately, the addition of the comparator in the threshold signal path introduces an additional switching delay due to its large signal swings and the whole point of using reduced signal swings to improve frequency performance is defeated.

4.8 Experimental Verification

The basic Piskarev multivibrator was breadboarded using the MC415 CMOS transistor arrays from Ferranti Interdesign [14]. First, the threshold circuit was separated from the rest of the multivibrator and the hysteresis voltage was measured as a function of R_{eq}. Then the entire circuit was reconnected and the frequency as a function of current was measured. This provided experimental verification of the basic theory and concepts of the Piskarev multivibrator. All measurements were carried out at low frequencies to minimize the

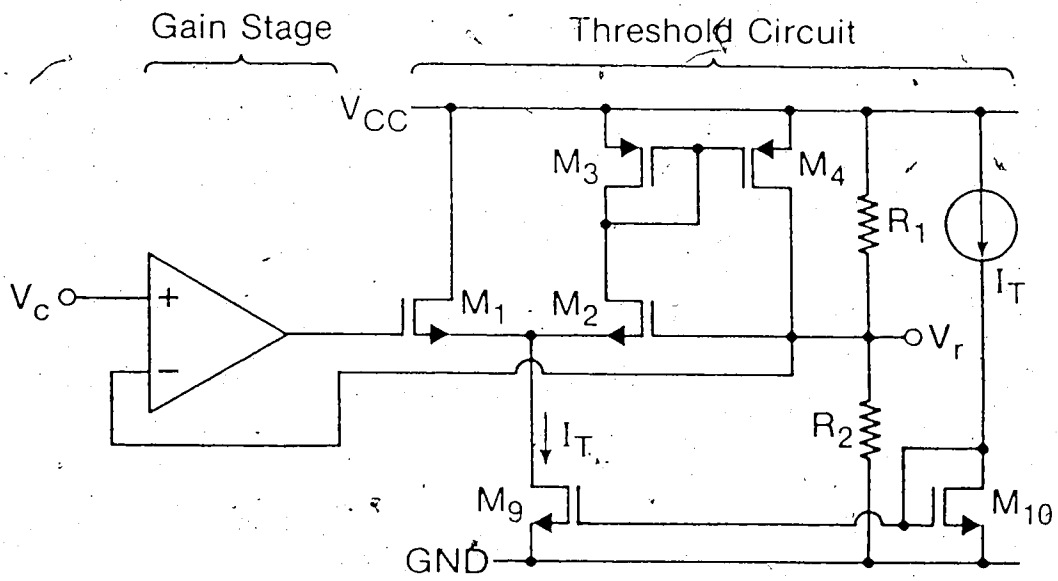

Figure 4.8 Gain Stage at Input of Threshold Circuit

effect of switching delays.

Breadboarding with discrete devices does not provide a true representation of the capabilities of a wholly integrated Piskarev multivibrator. The use of discrete devices and the plug-in type breadboard results in excessive parastic capacitances which degrade the frequency performance. To provide a clearer picture of the obtainable performance, SPICE [28] simulations were used to evaluate high frequency operation. Two areas of interest were investigated: (1) the influence on high frequency performance of using the buffer stage to control the charge circuit, and (2) the range of frequency control that is possible with this configuration.

The Piskarev multivibrator is intended for integrated circuit applications and verification of its performance in this form would be desirable. CMOS fabrication facilities are available to the student through the Canadian Microelectronics Corporation (CMC). With this in mind, the core of the multivibrator, consisting of the threshold and charge circuits (see appendix 2) but not including the bias generation circuits nor the R's and C, has been designed, layed out, and submitted for fabrication in the CMOS1B [29] process available through the CMC. The SPICE simulations are based upon these designs and this should provide a check of the simulation accuracy. Unfortunately, due to time constraints, these devices will not be available for testing in time for inclusion in this work.

4.8.1 Breadboard Verification: Experiments 4.1, 4.2a, 4.2b

The most important portion of the theory deals with the prediction of the hysteresis voltage. To test the accuracy of the

predicted hysteresis voltage the threshold circuit of the basic Piskarev multivibrator (Fig. 4.9) was constructed using the CMOS transitors array available from Ferranti Interdesign. Discrete resistors and capacitors were used to allow increased flexibilty in the experimental conditions. The device parameters for the experimental circuit are found in Table 4.1.

The threshold parameter m_{th} (4.11) has a strong influence on the hysteresis voltage and can be varied through R_{eq}. The hysteresis voltage was measured (Exp. 4.1) for a range of R_{eq} = 18 → 30kΩ (with I_T and β_{nT} held constant) and compared with the values predicted by (4.21). This range of R_{eq} corresponds to a variation of $m_{th} \approx 1/2 \rightarrow 0$ (the entire valid range for m_{th}). Good oincidence between the experimental and theoretical results is obtained over the entire range (Fig. 4.10). For oscillations to occur, the hysteresis voltage must be greater then zero, or $m_{th} < 1/2$ (see 4.11) so the minimum value for R_{eq} is set by the requirement

$$R_{eq} \geq \sqrt{\frac{2}{I_T \beta_{nT}}} \tag{4.32}$$

or more generally

$$R_{eq}^2 I_T \beta_{nT} \geq 2 \tag{4.33}$$

For the test circuit $R_{eq,min} \approx 14$ kΩ, which corresponds roughly with the x axis intercept (≈15 kΩ) of the hysteresis voltage versus R_{eq} graph in Fig. 4.10. Accurate prediction of the hysteresis voltage is possible over the entire range of m_{th}, indicating that the operation

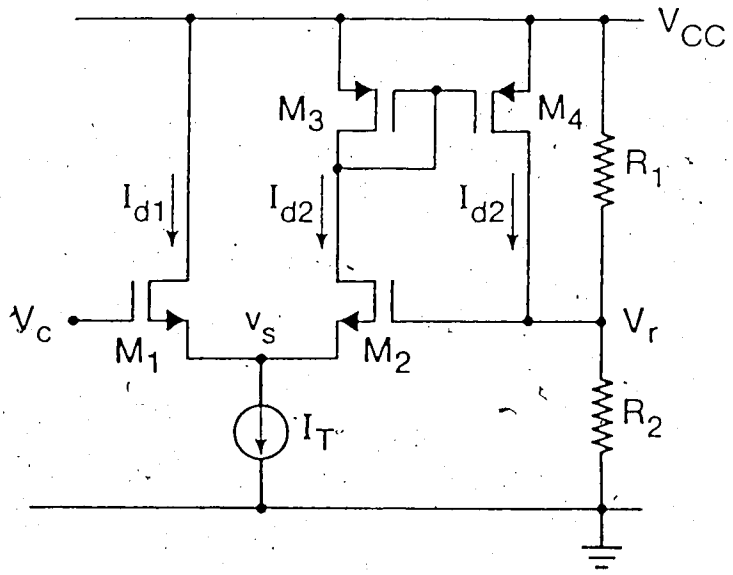

Figure 4.9 Threshold Circuit

	NMOS	PMOS
W/L	310/24	580/24
β^* ($\mu A/V^2$)	110	110
V_t (V)	1.25	0.9
γ ($V^{1/2}$)	1.8	-
ϕ_f (V)	0.3	0.3

* Measured at $|I_D| \approx 50\ \mu A$ and $|V_{SB}| \approx 0$

\- see [25] for method of determining device parameters

TABLE 4.1. TYPICAL TRANSISTOR PARAMETERS FOR EXP. 4.1, 4.2A, AND 4.2B

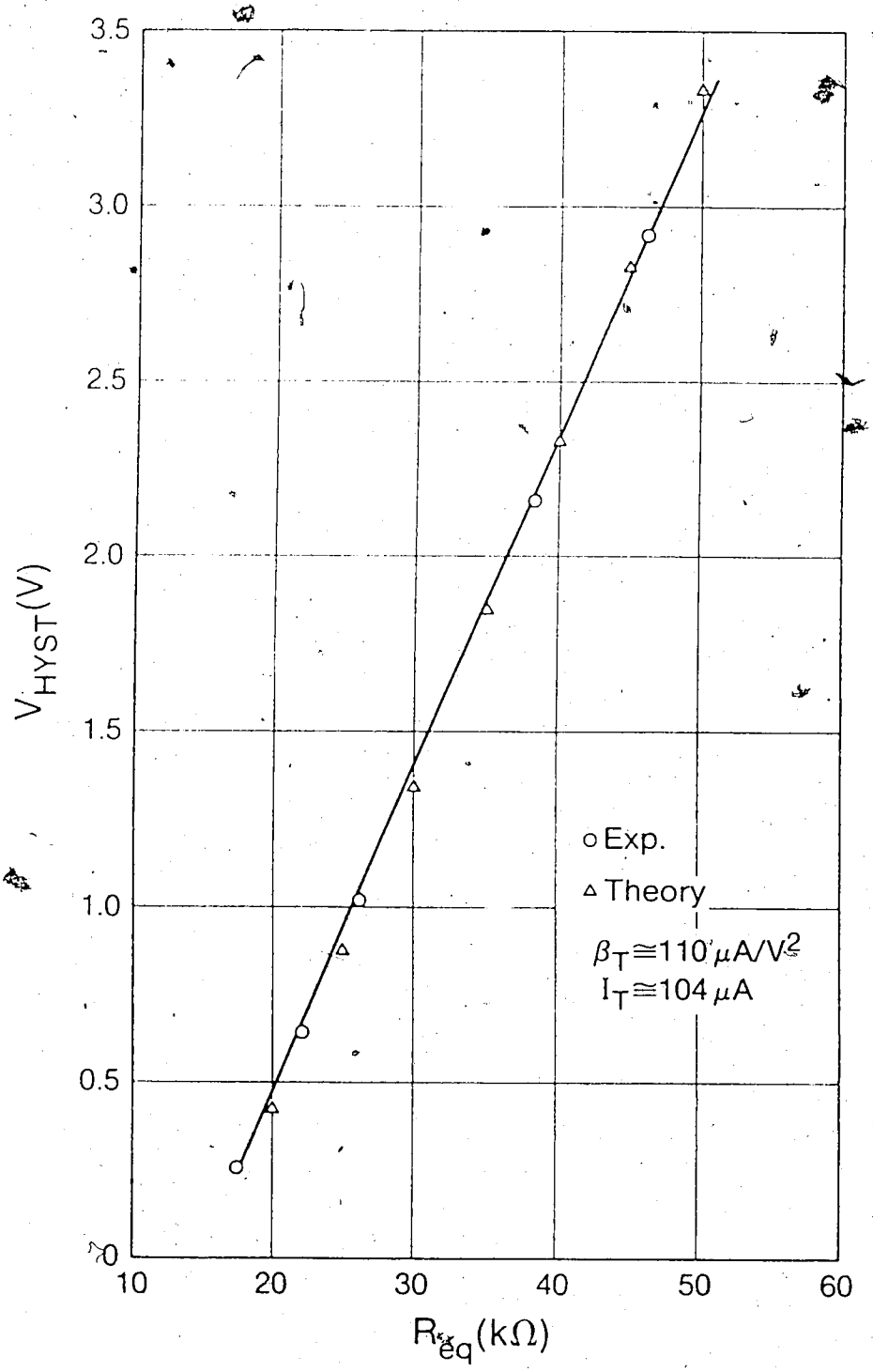

Figure 4.10 Hysteresis Voltage vs. Threshold Setting Resistance

of the threshold circuit is understood.

The entire multivibrator was now constructed (Fig. 4.1 and Table 4.2) and the frequency was measured as a function of current I_C, with I_C varied from 10 to 100 μA (one decade). The lower limit for the current is set by the level which could be accurately measured using the available test equipment (about 10μA), and the upper limit by (from 4.19)

$$I_C \leq I_T \frac{\beta_{nC}}{\beta_{nT}} \tag{4.34}$$

which limits I_C to about 100 μA maximum since $\beta_{nC} \approx \beta_{nT}$ and $I_T \approx 104$ μA. Two values of timing capacitor C were used: 220 nF (Exp. 4.2a) and 8.2nF (Exp. 4.2b).

The frequency versus I_C characteristic with the large (220 nF) timing capacitor is shown in Fig. 4.11 along with the predicted values (from 4.21). Within reasonable error the theoretical and experimental results correspond and show a linear relationship between frequency and current, as expected. If the experiment is repeated with the smaller timing capacitor (8.2 nF) and therefore a higher overall frequency range, the frequency versus current characteristic becomes nonlinear (Fig.4.11). Since only the capacitor was changed, the nonlinearity must be a result of switching delays (see 3.1). The total switching delay of the circuit was measured to be about 30 μS. Subtracting this delay from the frequency characteristic shown in Fig. 4.11 returns it to a straight line.

When the switching delays are insignificant, as for the case of

	EXP. # 4.2a	EXP. #-4.2b
R_1 (kΩ)	47	47
R_2 (kΩ)	47	47
V_{CC}	10	10
C (nF)	220	8.2

TABLE 4.2 CIRCUIT PARAMETERS FOR EXP. 4.2A, 4.3B

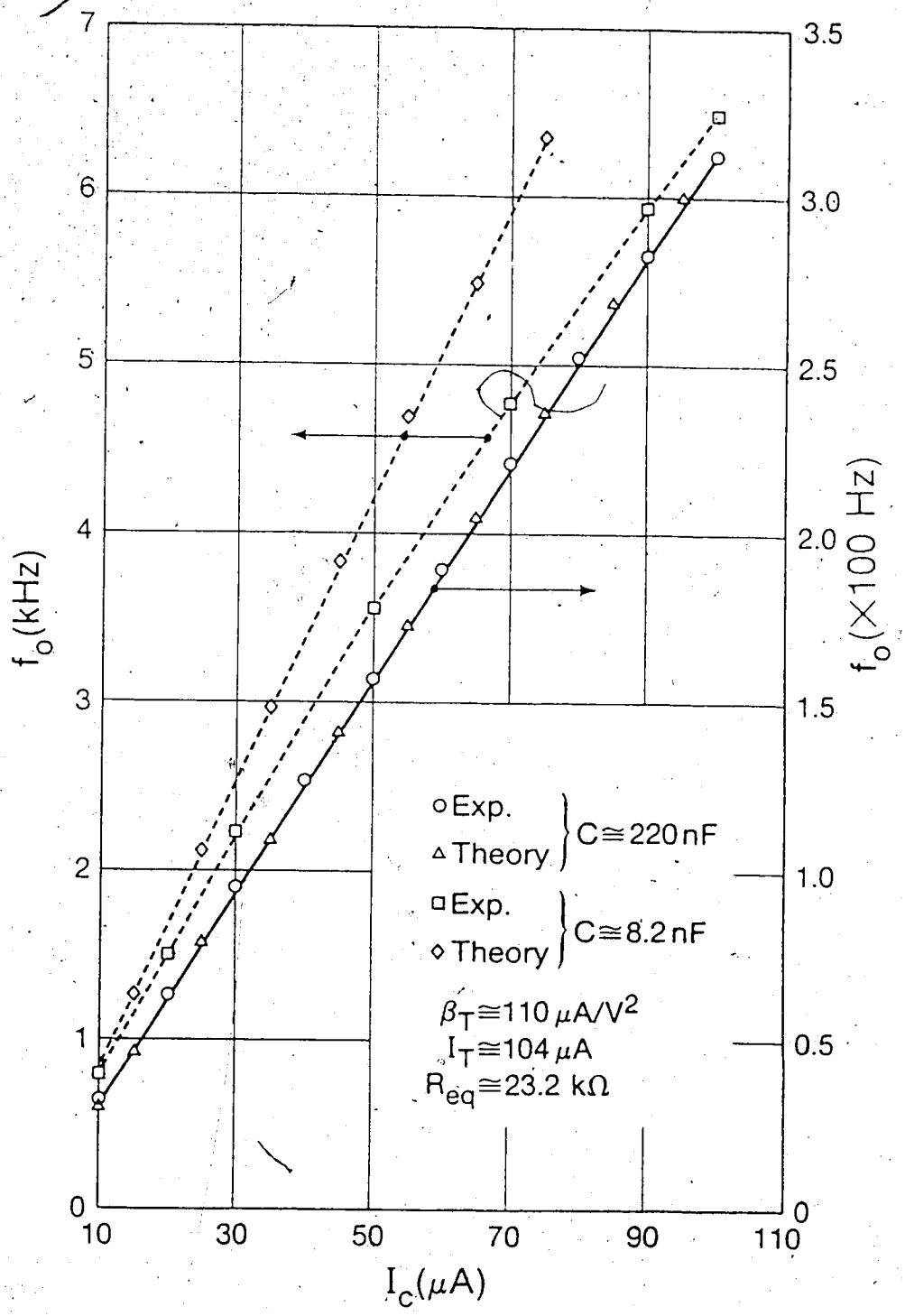

Figure 4.11 Frequency vs. Control Current for Basic Piskarev Multivibrator

C = 220 nF, the frequency characteristic can be accurately predicted. Once switching delays become significant compared to the period, the frequency characteristic becomes nonlinear. Integrating the multivibrator should reduce the parasitic capacitances and, therefore the switching delays, considerably.

4.8.2 SPICE Simulation: Experiments 4.3a, 4.3b, 4.4

Breadboarding is a suitable investigative tool only at low frequencies. To investigate the Piskarev multivibrator at higher frequencies the circuit's operation was simulated using SPICE [28]. SPICE simulation provides a window on the performance that can expected once the circuit is integrated.

In the basic Piskarev multivibrator the range of frequency control is limited by I_T and β_{nT} of the threshold circuit. As discussed in Section 4.7.2 an increased range of frequency control can be obtained by using a buffer stage to drive the charge steering differential pair. Additional switching delays are expected due to the addition of the buffer stage in the signal path. SPICE simulation will be used to investigate the significance of this delay.

The circuit under investigation consists of the basic multivibrator with the addition of a buffer stage (Fig. 4.5). Two connections for the charge steering differential pair will be studied: (1) the gate of M5 is connected to the gate of M2, which is the standard configuration (Fig. 4.5) and will be used as a benchmark (Exp. 4.3a), and (2) the gate of M5 is connected to the output of the buffer (drain of M17) (Exp. 4.3b) to provide additional frequency control range (Fig. 4.6). The input file for SPICE for these

simulations are found in appendix 1.

The two configurations were simulated a current range of I_c from 10 to 100 μA. The range of control current was set by the limitations (see Sect. 4.4) of the benchmark configuration; the behaviour of the other configuration over a larger current range will be addressed later. For these simulations the timing capacitor was set to 10 pF, a value which is suitable for realization in intergrated form. The results, Fig. 4.12, indicate that the use of the buffer stage to drive the charge steering circuit increases the nonlinearity of the frequency versus current characteristic, due to the increased switching delays. The benchmark configuration had a frequency range of about 0.7 → 3.4 MHz, while the buffered configuration had a range of about 0.7 → 2.5 MHz. Both versions have nonlinear frequency characteristics due to switching delays, but what is significant is that the maximum frequency of the buffered configuration has been reduced by about 25 % due to the additional delays of the buffer stage. At the low end of the frequency characteristic the two configurations are approximately equal. Therefore, the use of the buffer to extend the frequency control range degrades the frequency characteristic near the upper limits, but the penalty at lower frequencies is not as significant. For example, for this set of circuit parameters, if the maximum frequency is kept below ≈ 1 MHz the use of the buffer to increase the control range does not introduce a significant delay penalty.

The above results indicate that for frequencies below approximately 1 MHz the use of the buffer stage to drive the current

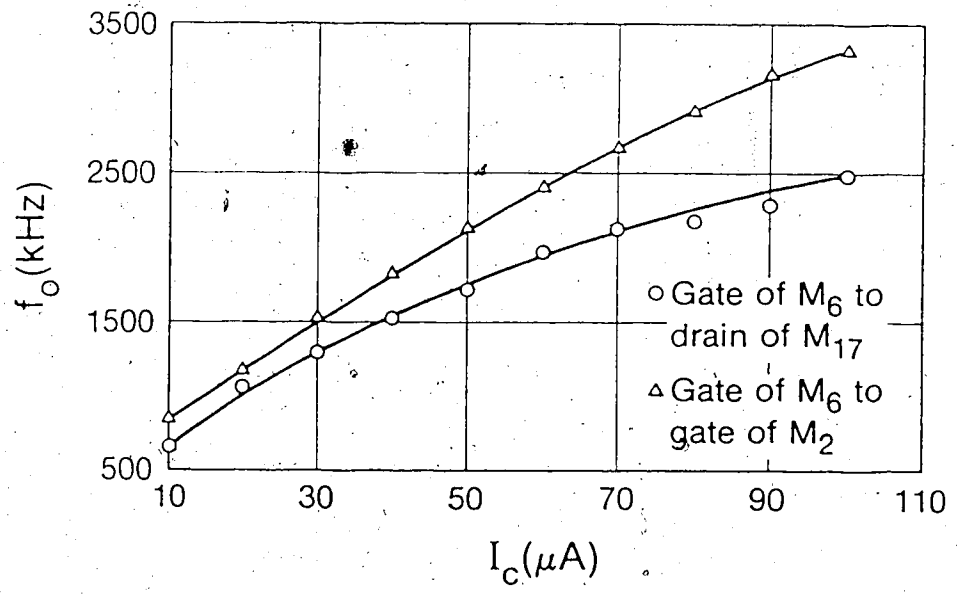

Figure 4.12 Effect of Using Buffer Stage to Control the Charge Steering Circuit

steering stage does not introduce significant additional delays. Using the same extended control range configuration (Fig. 4.6) as before, but with a larger timing capacitor (1 nF) to decrease to maximum frequency, the frequency was measured over a current range of I_C from 3 to 1000 μA (Exp. 4.4). At current levels much below $\approx$ 3 μA the charge/discharge currents become asymmetric and the oscillator loses its 50% duty cycle. The results (Fig. 4.13) indicate that frequency control is obtained over the entire range, but switching delays are still significant resulting in a nonlinear frequency characteristic.

4.9 Discussion

At low frequencies where the switching delays constitute only a small part of the total period, the hysteresis voltage (4:12) and frequency of oscillation (4.21) can be predicted with good accuracy. As the portion of the period consumed by the switching delay increases, the effective hysteresis voltage grows (due to overshoot) and the frequency versus charge current characteristic becomes nonlinear. At high frequencies, the assumption that at the threshold point the charge current's direction is instantaneously changed, is no longer valid. The delay between the time the capacitor voltage reaches the threshold point and time at which the direction of the charge current is reversed causes the voltage of the capacitor to overshoot the threshold voltage by an amount proportional to the delay. This results in an increase in the effective hysteresis voltage and the subsequent decrease in the oscillation frequency.

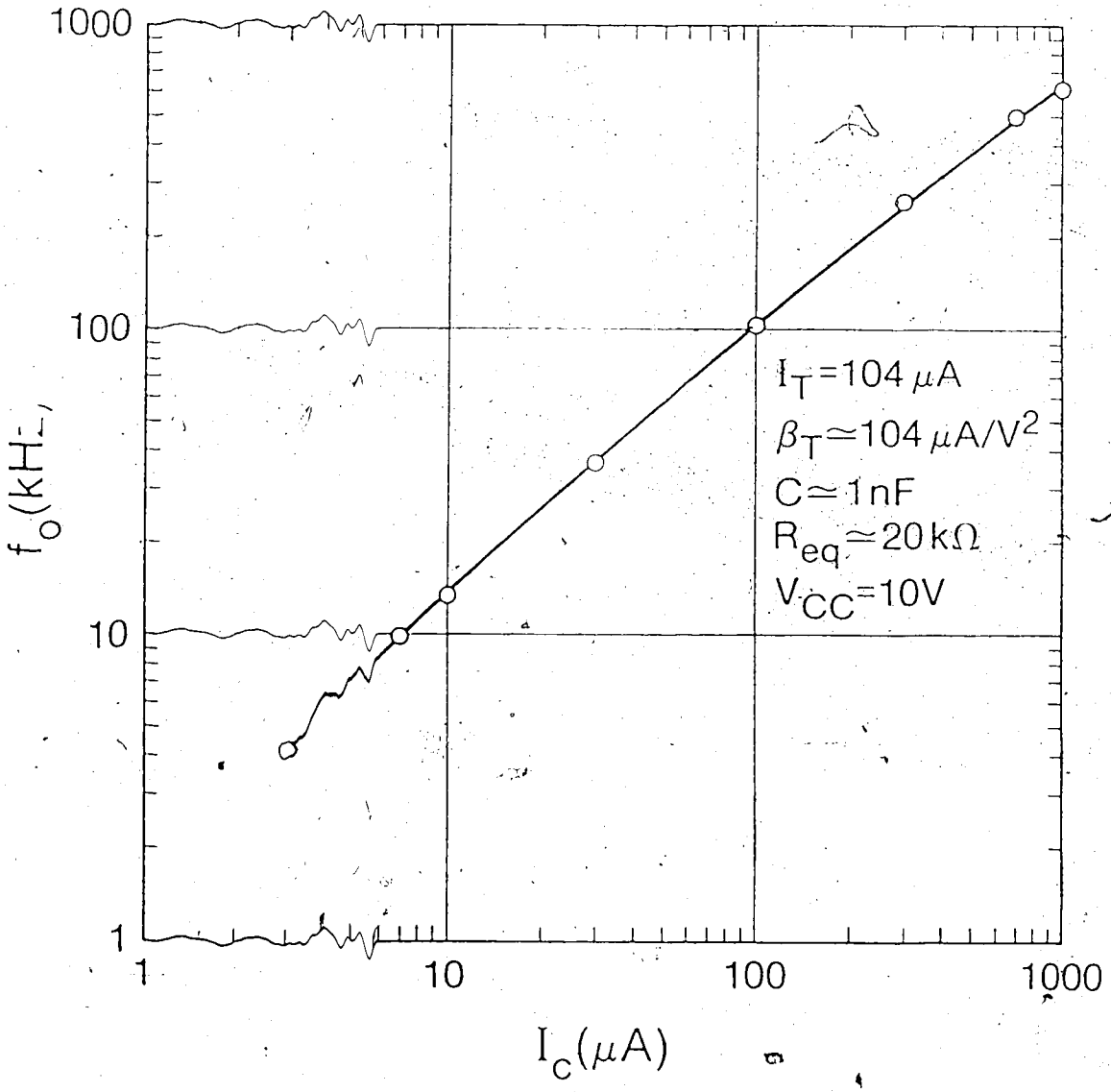

Figure 4.14 Frequency Characteristic with Extended Control Range

A wider range of frequency control can be obtained by using the extended control range configuration (Fig. 4.6) as compared to the basic configuration (Fig. 4,5), but the maximum frequency of oscillation will be decreased due to the additional switching delays introduced by the buffer stage. Therefore a tradeoff of the range of control with maximum frequency must be made in choosing between the extended control range and basic configurations.

To reduce the susceptibility of the hysteresis voltage to process and temperature variation the contribution of the term I_T / β_{nT} to the overall hysteresis voltage (4.12) should be minimized. This can be accomplished by reducing I_T (limited by the stability of the bias circuitry) and increasing β_{nT} (limited by chip area), while maintaining a constant swing at V_r (Fig. 4.1). To maintain a constant swing at V_r the reduction in I_T can be countered by the combination of increasing R_{eq} and the use of current mirror gain (Sect 4.7.4). Ideally the voltage swing at V_r should be large to minimize the influence of β_{nT} on the hysteresis voltage and to reduce jitter. The maximum level for V_r is set by either the requirement that M4 remains in pinch off operation (i.e. $V_{CC} - V_{r,high} \geq |V_{GS,M4} - V_{tp}|$) or speed limitations imposed by the increased delay of large swings. The latter limitation is best tested via SPICE simulations.

Once the term I_T / β_{nT} is minimized as described above, further improvements in thermal and process stability of the hysteresis voltage can be made by generating the threshold current in the

appropriate manner. Consider, for example, that:

$$I_T = V_{REF} / R_{bias} \tag{4.35}$$

where

$$R_{bias} = \frac{1}{N} R_{eq} \tag{4.36}$$

and V_{REF} is generated from a thermally stable voltage reference such as a bandgap voltage reference [34]. Now, if $I_T / \beta_{nT} \ll I_T R_{eq}$ and $m_{th} \ll 1$ then the effective hystersis voltage becomes

$$V_{HYST} \approx N V_{REF} \tag{4.32}$$

which is independent to the first order of R_{eq}, β_{nT}, and I_T and only dependent on the thermal and process sensitivity of the reference voltage. For the basic Piskarev multivibrator, the frequency control range is proportional to I_T/β_{nT} (4.21); therefore, the reduction of this term in order to decrease the sensitivity of the hysteresis voltage to temperature and process variations occurs at the cost of reduced control range. If a large control range is required and the cost of a reduced maximum frequency is acceptable, the use of the buffer stage to drive the current steering circuit can be used to increase the control range. The buffer stage should be used in most applications, whether or not it is used to drive the current steering stage, to provide conditioning and load driving capability for the output signal.

4.10 Conclusion

At low frequencies the operation of the Piskarev multivibrator is well understood and it shows good promise as a simple CCO with good linearity and range of control. A variety of modifications are suggested that allow fine tuning of the circuit's performance for specific applications. As the frequency increases, switching delays cause the frequency control characteristic to become nonlinear. A better understanding of the sources of the switching delays is required. It is uncertain at this point whether the poor performance of the Piskarev multivibrator in terms of switching delays is inherent in its structure and therefore a fundamental limitation, or whether appropriate choice of the transistor dimensions etc., will lead to improved high frequency performance.

5.0 Review of Results

5.1 Summary of Results

The source coupled and Piskarev multivibrators have not performed as well as was hoped, especially in terms of the frequency control characteristic linearity. The multivibrators, do however, perform as predicted by theory. The behaviour of the multivibrators is understood and the cause of the nonlinearity is known. For the source coupled multivibrator the nonlinearity of the frequency characteristic results from mismatches of the load and threshold device β's. This is a fundamental flaw resulting from the structure. The nonlinearity in the frequency characteristic of the Piskarev multivibrator is caused by switching delays. The exact source of the delays is unknown and requires further research, until which point it cannot be ascertained whether or not the delays are fundamental to the structure or can be reduced via careful design.

The primary achievement of this thesis lies not in the performance of the source coupled and Piskarev multivibrators but in the ability to understand and accurately predict their behaviour. An important part of the work is the approach used to find the hystersis voltage of the threshold circuit. The accurate determination of the switching points of the threshold circuit is crucial to accurate frequency calculation. The general approach taken is to use small signal analysis to find the currents in the threshold circuit at the onset of regenerative switching, then use large signal analysis to find the threshold voltage. A variety of other approaches have been proposed [30,31,32,33] for the determination of the hysteresis voltage

of a simple Schmitt trigger (which is what the threshold circuit is). The method proposed here, however, provides a simple and intuitive method which is widely applicable as evidenced by its successful application to the rather different topologies of the source coupled and Piskarev multivibrators.

For CCO applications where linearity is not of prime importance both the source coupled and Piskarev multivibrators are worthy of consideration. The principal advantage of the source coupled multivibrator is its extremely simple and thus compact structure. The Piskarev multivibrator is capable of operating over a wide range of frequencies (almost three decades in the SPICE simulation) and has the advantage of separate charge steering and threshold circuits which is benefical both in terms of linearity and ease of control, at the cost of a slight increase in circuit complexity.

5.2 Further Research

The nonlinearity of the Piskarev multivibrator is a result of the switching delays, the source of these delays is uncertain and needs further investigation. It is unknown whether the large delays are fundamental to the structure or can be be reduced through careful design. The major source of the delay is suspected to be parasitic capacitance located at the gate of M2. This capacitance has limited charge/discharge currents, so significant delays may still result even though careful attention was paid to minimizing the voltage swings at this point. The delay at this point is critical since it affects the speed with which the circuit undergoes regenerative switching. Due to

the highly nonlinear nature of the threshold circuit, analysis of the switching delays is a nontrivial problem.

The use of NMOS transitors for both the load and threshold devices of the source coupled multivibrator should be investigated. This will require the circuit to be fabricated in a p-well CMOS technology to allow the NMOS devices to be placed in separate wells so that the body effect can be removed. This is important since any body effect will result in mismatch of the β's. By using all NMOS devices the multivibrator should be capable of increased frequency performance (since no slow PMOS devices are used) as well as improved linearity of frequency control due to better matching of the β's.

References

[1] F.M. Gardner, *Phaselock Techniques*, 2nd ed. New York: John Wiley, 1979.

[2] H.P. Baltes and R.S. Popovic', "Intergrated semiconductor magnetic field sensors," *Proc. IEEE*, vol. 74, no. 8, pp. 1107-1132, Aug. 1986.

[3] S. Middelhoek, P.J. French, J.H. Huising, and W.J. Lian, "Sensors with digital frequency output," *Proc. 4th Int. Conf. Solid-State Sensors and Actuators*,1987, pp. 17-24.

[4] K.D. Wise, "Integrated sensors: key to future VLSI systems," *Proc. 6th Sensor Symp.*, , 1986, pp.1-9.

[5] A.F. Arbel, *Analog Signal Processing and Instrumentation*, Cambridge, Cambridge University Press, 1980.

[6] E. Habekotte, B. Hoefflinger, H.W. Klien, and M.A. Beunder, "State of the art in anlaog CMOS circuit design," *Proc. IEEE*, vol. 75, no. 6, pp. 816-828, Jun. 1987.

[7] J. Mavor, M.A. Jack, and P.B. Denyer, *Introduction to MOS LSI Design*, London: Addision-Wesley, 1983.

[8] Y. Tsividis and P. Antognetti, editors, *Design of MOS VLSI Circuits for Telecommunications*, New Jersey: Prentice Hall, 1985.

[9] A.B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, New Jersey: John Wiley,1984.

[10] R.R. Cordel and G. Garrett, "A highly stable VCO for application in monolithic phase-locked loops," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 480-485, Dec. 1975.

[11] J.F. Kukielka and R.G. Meyer, "A high frequency temperature stable monolithic VCO," *IEEE J. Solid-State Circuits*, vol. SC-16, no. 6, pp. 639-647, Dec. 1981.

[12] M.H Wakayama and A.A. Abidi, "A 30 MHz low-jitter high-linearity CMOS voltage controlled oscillator," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp. 1074-1081, Dec. 1987.

[13] A. Nathan, I.A. McKay, I.M. Filanovsky, and H.P. Baltes, "Design of a CMOS oscillator with magnetic-field frequency modulation," *IEEE. J. Solid-State Circuits*, vol. SC-21, pp. 230-232, Apr. 1987.

[14] *Analog CMOS Integrated Circuit Design Manual*, Ferranti Interdesign Inc., Scotts Valley, Ca.,1983.

[15] I.M. Filanovsky and I.G. Finvers, "A simple nonsaturated CMOS multivibrator," *IEEE J. Solid-State Circuits*, vol SC-23, no. 1, Feb. 1988.

[16] B. Gilbert, "A versatile monolithic voltage to frequency converter," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 6, pp. 852-864, Dec. 1976.

[17] F.V.J. Sleeckx and W.M.C. Sansen, "A wide-band current controlled oscillator using bipolar-JFET technology," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 5, pp. 875-881, Oct. 1980.

[18] A.A. Abidi and R.G. Meyer, "Noise in relaxation oscillators," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 494-496, Jun. 1987.

[19] A.A. Abidi, "Linearization of voltage controlled oscillators using switched capacitor feedback," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 3, pp. 494-496, Jun. 1987.

[20] RCA CMOS Integrated Circuits Data Book (SSD-250C), 1983.

[21] R.S. Muller and T.I. Kamins, *Device Electronics for Integrated Circuits*, 1st ed. New York: John Wiley, 1977.

[22] C.J.M. Verhoeven, "A new model for regenerative circuits," *Proc. 30th Midwest Symp. Circuits and Systems*, pp. 631-634, Aug. 1987.

[23] Y.P. Tsvidis, *Operation and modeling of the MOS transistor*, New York: McGraw-Hill, 1987.

[24] I.M. Filanovsky and V.A. Piskarev, "A simple nonsaturated multivibrator for low voltage power supply," *Int. J. Electronics*, vol. 6[illegible], no. 5, pp. 757-765, 1987.

[25] P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, New York: Holt, Rinehart and Winston, 1987.

[26] A. Ambrozy, *Electronic Noise*, New York: McGraw-Hill, 1982.

[27] C. Mead and L. Conway, *Introduction to VLSI systems*, Reading, Massachusetts: Addision-Wesley, 1980.

[28] L.W. Nagel and D.O. Pederson, "Simulation program with integrated circuit emphasis," *Proc. 16th Midwest Symp. Circuit Theory*, April 12, 1973.

[29] *Guide to the integrated circuit implementation services of the Canadian Microelectronics Corporation*, Carruthers Hall, Queen's University, Kingston, Canada, Jan. 1987.

[30] C.J.F. Ridders, "Accurate determination of threshold voltage levels of a Schmitt Trigger," *IEEE Trans. Circuits Syst.*, vol. CAS-32, no. 9, pp. 969-970, Sept. 1985.

[31] S.C.D. Roy, "Comment of accurate determination of threshold voltage levels of a Schmitt Trigger," *IEEE Trans. Circuits Syst.*, Vol. CAS-33, no. 7, pp. 734-73 , ul. 1986.

[32] H.V. Lauer, "Comment on accurate determination of voltage levels of a Schmitt Trigger," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 10, pp. 1252-1253, Oct. 1987.

[33] M.J.S. Smith, "On the circuit analysis of the Schmitt Trigger," *IEEE J. Solid-State Circuits*, vol SC-23, no. 1, Feb. 1988.

[34] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. New York: John Wiley, 1984.

List of Related Papers by Author

I.G. Finvers and I.M. Filanovsky, "Analysis of a source coupled CMOS multibrator," *IEEE Trans. Circuits Syst.*, accepted for publication.

I.M. Filanovsky and I.G. Finvers, "Analysis of a source coupled MOS multivibrator with resistive drain loads," *Int. J. Electronics*, accepted for publication.

I.M. Filanovsky and I.G. Finvers, "A simple nonsaturated CMOS multivibrator," *IEEE J. Solid-State Cicuits*, vol. SC-23, no. 1, Feb. 1988.

Conference Papers

I.M. Filanovsky, I.G. Finvers, L. Ristic, and H.P. Baltes, "Multivibrators with frequency control for application in integrated sensors," 1*st*, *Int. Forum ASIC and Transducer Technology*, Feb. 7-10, 1983.

Appendix 1 SPICE Input Files

```
Experiment 4.3(a) Piskarev Multivibrator
*    Basic Piskarev Multivibrator with buffer stage, control
*    of current steering stage provided by gate of M2 (see Fig.4.5)
*
.WIDTH  IN=80 OUT=80
.OPTIONS  ABSTOL=1P VNTOL=1U CPTIME=3000 NUMGET=4
+LIMPTS=2000 ITL5=10000
*
*    TRANSISTOR MODELS (FROM [29])
*
.MODEL NTNMOS (LEVEL=2 VTO=1.0
+KP=30.5E-6 GAMMA=1.4 CGSO=4.0E-12
+CGDO=4.0E-12 CGBO=2.0E-12 RSH=15.0
+CJ=4.0E-8 MJ=2.0 CJSW=8.0E-12
+MJSW=2 JS=1E-10 TOX=8.5--10
+NSUB=1E16 XJ=1E-6 LD=.7E-6
+UO=750 UCRIT=5E4 UEXP=0.14
+VMAX=5E6)
*
.MODEL NTPMOS (LEVEL=2 VTO=-1.0
+KP=10.2E-6 GAMMA=0.635 CGSO=4.0E-12
+CGDO=4.0E-12 CGBO=2.0E-12 RSH=75.0
+CJ=1.8E-8 MJ=2.0 CJSW=6.0E-12
+MJSW=2 JS=1E-10 TOX=8.5--10
+NSUB=2E15 XJ=0.9E-6 LD=.6E-6
+UO=250 UCRIT=1E4 UEXP=0.03
+VMAX=3E6)
*
*
*    CIRCUIT DESCRIPTION (REFER TO FIG. 4.5)
*
*
M1 12 3 5 5 NTNMOS W=100U L=10U AS=1900P AD=1200P
M2 6 4 5 5 NTNMOS W=100U L=10U AS=1900P AD=1200P
M3 6 6 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M4 4 6 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M5 3 3 2 0 NTNMOS W=150U L=10U AS=2850P AD=1800P
M6 9 11 2 0 NTNMOS W=150U L=10U AS=2850P AD=1800P
M7 3 9 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M8 9 9 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M9 5 7 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M10 7 7 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M11 2 8 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M12 8 8 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M13 12 12 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M14 10 12 1 1 NTPMOS W=100U L=10U AS=5700P AD=3600P
M15 10 10 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M16 11 6 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M17 11 10 0 NTNMOS W=100U L=10U AS=1900P AD-1200P
```

```
*
*
*    THRESHOLD SETTING RESISTORS
*
R1 1 4 40K
R2 4 0 40K
*
*
*    TIMING CAPACITOR
*
C 3 0 10P
*
*
*    CHARGE CURRENT
*
IC 1 8 (CONTROL CURRENT)
*
*
*    THRESHOLD CURRENT
*
IT 1 7 (THRESHOLD CURRNENT)
*
*
*    POWER SUPPLY VOLTAGE
*
VCC 1 0 DC 10
*
*
*    TRANSCIENT ANALYSIS
*
*    SET INITIAL CONDITIONS ON CAPACITOR
*
.IC V(3)=0
*
*    PERFORM TRANSCIENT ANALYSIS
*
.TRAN STEP STOP START UIC
*
*    PLOT THE RESULTS
*    WHERE V(3) IS THE VOLTAGE ON THE TIMING CAPACITOR
*    AND V(11) IS THE OUTPUT OF THE BUFFER STAGE
*
.PLOT TRAN V(3) V(11)
*
.END
```

```
Experiment 4.3(b) Piskarev Multivibrator
*     Basic Piskarev Multivibrator with buffer stage, control
*     of current steering stage (gate of M6) is provided by
*     output of buffer stage (drain of M17) see Fig. 4.6

*
.WIDTH  IN=80 OUT=80
.OPTIONS  ABSTOL=1P VNTOL=1U CPTIME=3000 NUMGET=4
+LIMPTS=2000 ITL5=10000
*
*     TRANSISTOR MODELS (FROM [29])
*
.MODEL NTNMOS (LEVEL=2 VTO=1.0
+KP=30.5E-6 GAMMA=1.4 CGSO=4.0E-12
+CGDO=4.0E-12 CGBO=2.0E-12 RSH=15.0
+CJ=4.0E-8 MJ=2.0 CJSW=8.0E-12
+MJSW=2 JS=1E-10 TOX=8.5=-10
+NSUB=1E16 XJ=1E-6 LD=.7E-6
+UO=750 UCRIT=5E4 UEXP=0.14
+VMAX=5E6)
*
.MODEL NTPMOS (LEVEL=2 VTO=-1.0
+KP=10.2E-6 GAMMA=0.635 CGSO=4.0E-12
+CGDO=4.0E-12 CGBO=2.0E-12 RSH=75.0
+CJ=1.8E-8 MJ=2.0 CJSW=6.0E-12
+MJSW=2 JS=1E-10 TOX=8.5=-10
+NSUB=2E15 XJ=0.9E-6 LD=.6E-6
+UO=250 UCRIT=1E4 UEXP=0.03
+VMAX=3E6)
*
*
*     CIRCUIT DESCRIPTION (REFER TO FIG. 4.5)
*
*
M1  12  3  5  5 NTNMOS W=100U L=10U AS=1900P AD=1200P
M2  6  11  5  5 NTNMOS W=100U L=10U AS=1900P AD=1200P
M3  6  6  1  1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M4  4  6  1  1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M5  3  3  2  0 NTNMOS W=150U L=10U AS=2850P AD=1800P
M6  9  11  2  0 NTNMOS W=150U L=10U AS=2850P AD=1800P
M7  3  9  1  1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M8  9  9  1  1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M9  5  7  0  0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M10  7  7  0  0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M11  2  8  0  0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M12  8  8  0  0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M13  12  12  1  1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M14  10  12  1  1 NTPMOS W=100U L=10U AS=5700P AD=3600P
M15  10  10  0  0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M16  11  6  1  1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M17  11  10  0 NTNMOS W=100U L=10U AS=1900P AD=1200P
*
```

```
*
*    THRESHOLD SETTING RESISTORS
*
R1 1 4 40K
R2 4 0 40K
*
*
*    TIMING CAPACITOR
*
C 3 0 10P
*
*
*    CHARGE CURRENT
*
IC 1 8 (CONTROL CURRENT)
*
*
*    THRESHOLD CURRENT
*
IT 1 7 (THRESHOLD CURRNENT)
*
*
*    POWER SUPPLY VOLTAGE
*
VCC 1 0 DC 10
*
*
*    TRANSCIENT ANALYSIS
*
*    SET INITIAL CONDITIONS ON CAPACITOR
*
.IC V(3)=0
*
*    PERFORM TRANSCIENT ANALYSIS
*
.TRAN STEP STOP START UIC
*
*    PLOT THE RESULTS
*    WHERE V(3) IS THE VOLTAGE ON THE TIMING CAPACITOR
*    AND V(11) IS THE OUTPUT OF THE BUFFER STAGE
*
.PLOT TRAN V(3) V(11)
*
.END
```

```
Experiment 4.4 Piskarev Multivibrator
*    Basic Piskarev Multivibrator with buffer stage, control
*    of current steering stage (gate of M6) is provided by
*    output of buffer stage (drain of M17) see Fig. 4.6
*    Extended control range i.e. I_C is varied from 3 to 1000 μA
*    and C is increased to 10nF
*
.WIDTH  IN=80 OUT=80
.OPTIONS  ABSTOL=1P VNTOL=1U CPTIME=3000 NUMGET=4
+LIMPTS=2000 ITL5=10000
*
*    TRANSISTOR MODELS (FROM [29])
*
.MODEL NTNMOS (LEVEL=2 VTO=1.0
+KP=30.5E-6 GAMMA=1.4 CGSO=4.0E-12
+CGDO=4.0E-12 CGBO=2.0E-12 RSH=15.0
+CJ=4.0E-8 MJ=2.0 CJSW=8.0E-12
+MJSW=2 JS=1E-10 TOX=8.5--10
+NSUB=1E16 XJ=1E-6 LD=.7E-6
+UO=750 UCRIT=5E4 UEXP=0.14
+VMAX=5E6)
*
.MODEL NTPMOS (LEVEL=2 VTO=-1.0
+KP=10.2E-6 GAMMA=0.635 CGSO=4.0E-12
+CGDO=4.0E-12 CGBO=2.0E-12 RSH=75.0
+CJ=1.8E-8 MJ=2.0 CJSW=6.0E-12
+MJSW=2 JS=1E-10 TOX=8.5--10
+NSUB=2E15 XJ=0.9E-6 LD=.6E-6
+UO=250 UCRIT=1E4 UEXP=0.03
+VMAX=3E6)
*
*
*    CIRCUIT DESCRIPTION (REFER TO FIC. 4.6)
*
*
M1 12 3 5 5 NTNMOS W=100U L=10U AS=1900P AD=1200P
M2 6 11 5 5 NTNMOS W=100U L=10U AS=1900P AD=1200P
M3 6 6 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M4 4 6 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M5 3 3 2 0 NTNMOS W=150U L=10U AS=2850P AD=1800P
M6 9 11 2 0 NTNMOS W=150U L=10U AS=2850P AD=1800P
M7 3 9 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M8 9 9 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M9 5 7 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M10 7 7 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M11 2 8 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M12 8 8 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M13 12 12 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
M14 10 12 1 1 NTPMOS W=100U L=10U AS=5700P AD=3600P
M15 10 10 0 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
M16 11 6 1 1 NTPMOS W=300U L=10U AS=5700P AD=3600P
```

```
M17 11 10 0 NTNMOS W=100U L=10U AS=1900P AD=1200P
*
*
*    THRESHOLD SETTING RESISTORS
*
R1 1 4 40K
R2 4 0 40K
*
*
*    TIMING CAPACITOR
*
C 3 0 10N
*
*
*    CHARGE CURRENT
*
IC 1 8 (CONTROL CURRENT)
*
*
*    THRESHOLD CURRENT
*
IT 1 7 (THRESHOLD CURRNENT)
*
*
*    POWER SUPPLY VOLTAGE
*
VCC 1 0 DC 10
*
*
*    TRANSCIENT ANALYSIS
*
*    SET INITIAL CONDITIONS ON CAPACITOR
*
.IC V(3)=0
*
*    PERFORM TRANSCIENT ANALYSIS
*
.TRAN STEP STOP START UIC
*
*    PLOT THE RESULTS
*    WHERE V(3) IS THE VOLTAGE ON THE TIMING CAPACITOR
*    AND V(11) IS THE OUTPUT OF THE BUFFER STAGE
*
.PLOT TRAN V(3) V(11)
*
.END
```

Appendix 2

Circuits Submitted to CMC for Fabrication

Circuit # 1 Basic Paskarev: see figure 4.1(a)

DEVICE (REFER TO FIG. 4.1)	W/L
1,2,9,10	100/10
5,6,11,12	200/10
3,4	300/10
7,8	600/10

TABLE A.1 DEVICE SIZES FOR CMC.1

NOTE:
(1) R_1,R_2,C are external
(2) M1, M2 have no body effect
(3) M5, M6 have body effect
(4) I_T,I_C set externally

Circuit # 2 : Basic Piskarev with current mirror gain (3)

DEVICE (REFER TO FIG. 4.1)	W/L
1,2,9,10	100/10
5,6,11,12	200/10
3	300/10
4	900/10
7,8	600/10

TABLE A.2 DEVICE SIZES FOR CMC.2

NOTE: (1) R_1,R_2,C are external
(2) M1, M2 have no body effect
(3) M5, M6 have body effect
(4) I_T,I_C set externally

Circuit # 3 Piskarev Multivibrator with Buffer Stage (see fig. 4.5)

DEVICE (REFER TO FIG. 4.6)	W/L
1,2,9,10	100/10
5,6,11,12	200/10
3,4	300/10
7,8	600/10
13,14	300/10
15	100/10
16	600/10
17	200/10

TABLE A.3 DEVICE SIZES FOR CMC.3

NOTE: (1) R_1, R_2, C are external
(2) M1, M2 have no body effect
(3) M5, M6 have body effect
(4) I_T, I_C set externally