University of Alberta

Virtual Impedance Based Selective Harmonic Compensation (VI-SHC) PWM

by

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of

> Master of Science in Power Engineering and Power Electronics

Electrical and Computer Engineering

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Abstract

A low-switching PWM scheme is presented for a high power current source rectifier (CSR) system to actively compensate the grid background harmonics and improve the line current harmonic performance.

The PWM scheme described above is placed in context with the existing techniques review of the traditional selective harmonic elimination (SHE) and the recently developed selective harmonic compensation (SHC) PWM. The switching angles calculation method based on the global optimization approach is designed to develop a user-friendly software tool for the SHE and SHC PWM switching angles calculation.

A novel virtual impedance based selective harmonic compensation (VI-SHC) PWM scheme is described in the thesis with a view to overcoming the disadvantages of the SHE and SHC PWM methods existing in the implementation. The VI-SHC PWM does not require to measure the grid voltage harmonics, does not rely on an accurate CSR system model, and therefore is very robust for practical implementation.

Acknowledgement

I should like to express my gratitude to a number of people for their invaluable assistance in helping me accomplish my Master of Science (Msc.) thesis at the Department of Electrical and Computer Engineering of the University of Alberta. First, I shall be eternally grateful to Dr. Yunwei (Ryan) Li, my Msc. supervisor, for his pivotal role, guidance, constant support, patience and encouragement throughout the whole research work. I am also thankful to Dr. Navid Zargari, Dr. George Cheng from Rockwell Automation Canada, who supported this research work by providing insightful suggestions and feedback. I would like to give my truly thanks to my colleagues in Dr. Li's group, especially Jinwei He, Hua Zhou, Eric Zhang and Jian Shang who offered advices and helps during the experimental verification phase of this work. Last but not least, I must express my immense gratitude to my father and mother, my relatives and my dear friends for their great encouragement and support.

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List of Abbreviations

PWM	Pulse width modulation
CSC	Current source converter
CSR	Current source rectifier
CSI	Current source inverter
VSC	Voltage source converter
VSI	Voltage source inverter
GTO	Gate turn off thyristor
GCT	Gate commutated thyristor
IGCT	Integrated gate commutated thyristor
IGBT	Insulated gate bipolar transistors
TPWM	Trapezoidal pulse width modulation
SVPWM	Space vector pulse width modulation
m_a	Modulation index
SHE	Selective harmonic elimination
w_h	Weighting factor
THD	Total harmonic distortion
SHC	Selective harmonic compensation
GUI	Graphical user interface
SDFT	Sliding discrete Fourier transformation
N_A	Number of free angles
N_P	PWM pulse number in half fundamental cycle
VI-SHC	Virtual impedance based selective harmonic compensation
k	Coefficient designed for the emulation of a virtual impedance
A	The real part of k when k is a complex number
В	The imaginary part of k when k is an imaginary or a complex
	number

Chapter 1

Introduction

An introduction and background information of the thesis work are given in this chapter. The main objective of the research in this thesis is to develop a pulse width modulation (PWM) scheme for a three-phase current source rectifier (CSR) system to mitigate the line current harmonic distortions. The features of a PWM current source converter (CSC) are first introduced and discussed in this chapter followed by a review of the traditional PWM control schemes of a CSC. Afterwards, the challenge of line current harmonics mitigation in a CSR system is presented. The objectives of the research work, as well as the thesis outline are provided in the end.

1.1 Background

1.1.1 PWM current source converter (CSC)

Increasing interest and efforts on the development of high power converters and medium-voltage (MV) (2.3kV- 13.8kV) drives started since the mid-1980s when the 4500V gate turn off (GTO) thyristors became commercially available. These high power MV drives have been commissioned worldwide in the industrial applications, such as pipeline pumps, fans in the cement industry, traction applications in transportation, etc. [1-2]. In the late 1990s, the advent of high-power insulated gate bipolar transistors (IGBT), gate commutated thyristors (GCT) and especially the integrated gate commutated thyristors (IGCT), has dramatically changed the dominant position of the GTO in the high power MV drives [1-3].



Figure 1.1 A MV high power current source drive

The converters used in MV drives can be generally classified into voltage source converters (VSC) and current source converters (CSC). The voltage source converter outputs a defined three-phase PWM voltage while the current source converter produces a defined three-phase PWM current for the load. There are mainly two types of CSC used in the MV drives: PWM converters and load-commutated converters. The load-commutated converter, which utilizes SCR thyristors whose commutation is assisted by the load with a leading power factor, is very suitable for very large synchronous motor drives with a power rating up to 100 MW [1]. With the advent of GCT and IGCT switches, the PWM CSC is increasingly used in current source fed MV (2.3kV-6.9kV) high power applications. Its characteristics are described as follows [1-2] [4-10]:

- Simple converter topology: Figure 1.1 shows a typical medium voltage high power drive topology with a PWM current source rectifier (CSR) and a PWM current source inverter (CSI). The CSR or the CSI only needs 6 symmetrical GCT or IGCT switches (without anti-parallel freewheeling diodes).
- Motor friendly waveforms: The CSI outputs a three-phase PWM current instead of PWM voltage as in the voltage source inverter (VSI). With the filter capacitors installed at the CSI output, the load current and voltage wave-forms are close to sinusoidal. Thus the issue of high *dv/dt* in the VSI does not exist in the CSI.
- Reliable short circuit protection: On the DC side of the CSR, there is a DC choke inductor which is required to mitigate the ripples in the DC current to

an acceptable level (<15%). The size of this DC inductor is rather large, normally in the range of 0.5p.u. to 0.8p.u. Therefore, with a short-circuit fault in the terminals of CSR or CSI, the rate of rise of the DC current is limited by the large DC choke.

- Improved power factor: The current source drive using the PWM CSR as a front end has a minimum input power factor of 98% over a wide speed range [1]. With relevant power factor control schemes, the CSR can operate at the unity power factor or the highest achievable power factor over the full operating range.
- Reduced line current harmonic distortion: As can be seen from Figure 1.1, the input of the CSR requires a three-phase capacitor, to assist the commutation of the switches, and to help filter out the current harmonics. Moreover, with the relevant PWM control schemes, the harmonic performance of the line current of the CSC can be very good. However, this three-phase capacitor together with the line impedance would raise the issue of LC resonances.
- Four-quadrant operation and regenerative braking capability: The power flow in the CSI drive is bidirectional. No additional components are required for four-quadrant operation and dynamic braking.

1.1.2 Traditional PWM control schemes of the CSC

For a CSC, the PWM design is restrained by two conditions: the DC current should be continuous and the PWM current should be defined [1-2]. Thus, at any time instant, there should be only two switches conducting, one in the upper half of the bridge while the other in the lower half.

Various PWM techniques have been developed for the CSC. Among them, three methods are most frequently employed for a high power CSC with a switching frequency of a few hundred hertz: trapezoidal pulse width modulation (TPWM), space vector pulse width modulation (SVPWM), and selective harmonic modulation (SHE) [1] [11].

A. Trapezoidal pulse width modulation (TPWM)



Figure 1.2 Trapezoidal pulse-width modulation

The TPWM is a carrier based PWM scheme. As can be observed from Figure 1.2, v_m is the trapezoidal modulation wave, while v_c is the triangular carrier signal. The resultant PWM current i_{wa} is produced by comparing the trapezoidal modulating reference waveform v_m with the triangular waveform v_c . It can be observed that there is no triangular pulse in the center 60° interval of the positive (and negative) half fundamental cycle to avoid switching in this region. The modulation index m_a is set as:

$$m_a = \frac{V_m}{V_c} \tag{1.1}$$

where V_m and V_c are the peak-peak values of the modulating reference and carrier waves, respectively.

The switching frequency f_{sw} can be calculated as:

$$f_{sw} = f_1 \bullet N_p \tag{1.2}$$

where f_I is the PWM fundamental frequency and N_p is the pulse number per half fundamental cycle.

In terms of the THD performance of the TPWM, the generated PWM does not contain any even order harmonics since the PWM pattern is half-wave symmetrical. However, it has two pairs of dominant harmonics at harmonic order



Figure 1.3 space vector diagram for a CSC

 $h = 3(N_p - 1) \pm 1$ and $h = 3(N_p - 1) \pm 5$, thus this modulation scheme is usually used in the condition in which the fundamental frequency is rather low (N_p is rather large), e.g. in the CSI fed induction motor drives when the motor is operating at low speeds, since the filter of the drive usually cannot filter out low order harmonics. The TPWM is commonly employed in the case N_p is no less than 7 [1] [11-13].

B. Space vector pulse width modulation (SVPWM)

In consideration of the constraint of the CSC switching, the overall switching states of the CSC can be obtained and divided into two types: zero and active switching states. The active and zero switching states can be represented by active and zero space vectors, respectively. As is shown in Figure 1.3, $\overline{I_1}$ to $\overline{I_6}$ are the active vectors and $\overline{I_7}$ to $\overline{I_9}$ are the zero vectors.

The balanced three-phase instant PWM current i_{wa} , i_{wb} , and i_{wc} can be transformed into two-phase currents in the α - β plane, which would then be used to express the current space vectors, as is given in (1.3):

$$\overline{I_k} = \frac{2}{\sqrt{3}} I_d e^{j\left((k-1)\frac{\pi}{3} - \frac{\pi}{6}\right)}$$
(1.3)

where *k*=1, 2, ..., 6.

The SVPWM is actually using the stationary space vectors to synthesize the rotating current reference vector $\overline{I_{ref}}$. For a given $\overline{I_{ref}}$, it can be synthesized by two adjacent active vectors and a zero vector when it passes through each sector. For example, when the reference current is in the first sector, equation (1.4) can be established according to the current-second balancing:

$$\overline{T_{ref}}T_s = \overline{T_1}T_1 + \overline{T_2}T_2 + \overline{T_0}T_0$$

$$T_s = T_1 + T_2 + T_0$$
(1.4)

where T_1 , T_2 and T_0 are the dwell times for $\overline{I_1}$, $\overline{I_2}$ and $\overline{I_0}$, and T_s is the sampling period.

Substituting the expression of the relevant stationary space vectors (1.3) into equation (1.4) will lead to the expression of the dwelling times [1]:

$$T_{1} = m_{a} \sin\left(\frac{\pi}{6} - \theta_{sec}\right) T_{s}$$

$$T_{2} = m_{a} \sin\left(\frac{\pi}{6} + \theta_{sec}\right) T_{s}$$

$$T_{0} = T_{s} - T_{1} - T_{2}$$

$$\theta_{sec} = \theta - (k - 1)\frac{\pi}{3}$$
(1.5)

where m_a is the modulation index, defined as $m_a = \frac{I_{ref}}{I_d}$, which ranges from 0 to 1;

 θ is the angular displacement between $\overline{I_{ref}}$ and the α axis, as is illustrated in Figure 1.4; θ_{sec} is the reference vector angle in a space sector which is in the range of $\left(-\frac{\pi}{6}, \frac{\pi}{6}\right)$; and k = 1, 2, ..., 6 for sectors 1, 2, ..., 6, respectively.

In addition, the specific switching sequence is also required for the synthesis of $\overline{I_{ref}}$. Generally, in order to minimize the number of device switching for a given PWM period, only two switches are allowed during the transition from one switching state to another, three zero vectors are therefore arranged in each sector, as shown in Figure 1.3.



Figure 1.4 Various space vector sequences for CSC [55]

Various space vector sequences have been employed in the literatures for the modulation of CSC [52-55]. Figure 1.4 lists a few sequences, where the sequence (e) is more popular in industry [55].

The main feature of the SVM scheme is fast dynamic response. The modulation index (m_a) can be adjusted within a sampling period T_s , to control the PWM current i_w . Therefore, the SVM scheme is suitable for applications where a fast dynamic response is required. However, the SVM scheme has the lowest DC current utilization due to its bypass operation. And its THD performance is less



Figure 1.5 Traditional SHE PWM pattern

satisfactory than TPWM and SHE under the same switching frequency [1] [11-13].

C. Selective harmonic elimination (SHE)

The SHE scheme is an optimal off-line modulation scheme which is employed to enable the elimination of a number of unwanted harmonics in the CSC PWM current. It provides a superior harmonic performance with a low switching frequency [1] [15] [16]. For this modulation scheme, the desired PWM current patterns (which don't contain the selected undesired harmonics) are first calculated off-line, and then the SHE PWM is typically implemented by using a look-up table. To obtain balanced, well-defined three-phase PWM currents without any triplen or even order harmonics, the following constraints need to be satisfied for the PWM pattern design [16]:

- No PWM is permitted in the center 60° width of each half-cycle;
- The waveform should have quarter-wave and half-wave symmetry;
- For 30° on either side of the 30° and 150° positions, the pulse pattern must be an inverse mirror image.

It is worth noting that the first constraint is to avoid the shoot through state and restrain the modulation index (m_a) to be its maximum value. This constraint can be released for CSR using m_a control. However, for the CSR using the delay-angle control for DC current regulation, the first constraint should also be maintained [15-16]. Figure 1.5 illustrates a typical half-cycle waveform of the CSC PWM current pattern which satisfies the above constraints.

Due to the pattern design constraints given above, for a waveform with N_p (N_p is always odd) pulse number in half fundamental cycle, the number of unknown switching angles (or free angles) that determine the complete PWM pattern is $N_A = (N_p - 1)/2$ and all the free angles are bound in between 0° and 30° [16]. Given the free angles, all the other switching angles of the pattern can be calculated. For the waveform shown as an example in Figure 1.5, there are five current pulses per half fundamental cycle with two independent switching angles θ_1 , and θ_2 , the rest of the switching angles can be obtained through the equation (1.6) as follows:

$$\theta_{i} = \frac{\pi}{3} - \theta_{5-i}, \quad i = 3, 4$$

$$\alpha_{j} = \frac{2\pi}{3} + \theta_{j}, \quad j = 1, 2, ..., 4$$
(1.6)

The Fourier analysis of the PWM current with N_p pulses per half cycle can be expressed as [16]:

$$i_a = \sum I_{ah} \sin wt \tag{1.7}$$

where I_{ah} is the magnitude of i_a ,

$$I_{ah} = \left(\frac{4I_d}{h\pi}\right) \cos\left(\frac{h\pi}{6} \left[\left(-1\right)^{N_T} + 2\sum_{i}^{N_T} \left(-1\right)^{i+1} \cos\left[h(\theta_i - \frac{\pi}{6})\right] \right] \right)$$
(1.8)

where *h* is the harmonic order, h=1, $6m\pm 1$, m=1, 2, ...; N_A is the number of free angles, and I_{ah} is the Fourier coefficient. Note that the Fourier coefficient I_{bh} is zero due to the quarter-wave symmetry. Therefore, in order to eliminate *k* harmonics, *k* equations of (1.8) are needed to be solved simultaneously (assign the relevant I_{ah} to be zero) so as to obtain *k* free angles. Thus, the relationship between the number of the harmonics which need to be eliminated (*k*) and the number of the free angles (N_A) can be obtained as in (1.9).

$$k = N_A = \frac{(N_p - 1)}{2} \tag{1.9}$$

Additionally, the minimum pulse width (r) requirement should be satisfied for the feasibility of implementation. Therefore the free angles should meet the constraints listed in (1.10) [16].

$$\begin{aligned} \theta_2 &-\theta_1 \ge r \\ \theta_3 &-\theta_2 \ge r \\ \vdots \\ \theta_k &-\theta_{k-1} \ge r \\ \frac{\pi}{6} &-\theta_k \ge r \end{aligned} \tag{1.10}$$

In the real applications, the free angles of a PWM pattern are also selected to optimize various performance criteria [15-16]. The optimization process demands off-line computation of the free angles, targeting the minimization of the appropriate performance index (objective function), which commonly is a nonlinear function possessing several variables (free angles) with fixed bounds and inequality constraints, as stated in (1.10). For example, one probable objective function (also called cost function) is the minimization of the square of each harmonic, with weighting factor imposed on each harmonic, as given in equation (1.11).

$$C(\theta_1, \theta_2, \dots, \theta_k) = \sum w_h I_{ah}^2(\theta_1, \theta_2, \dots, \theta_k)$$
(1.11)

where k is the number of the free angles; I_{an} is the magnitude of the h^{th} harmonic current which is expressed as in (1.8); and w_h is the weighting factor for the h^{th} harmonic current. The higher the weighting factor, the higher priority is put on the minimization of the relevant harmonic. For the normalized PWM current of the CSC, this cost function is actually equal to the THD² since the fundamental current is approximately 1 p.u.

The SHE scheme usually provides the CSC superior waveform performance with a relatively low switching frequency, since the low order harmonics are usually eliminated and the higher order harmonics can be mitigated by the filter of the converter. This scheme has been widely used in CSI-fed motor drives to provide grid-friendly and motor-friendly waveforms [1] [13] [15-16].

1.1.3 Line current harmonics mitigation

In recent years, the problems caused by the harmonic currents in electric power systems have become more serious due to the proliferation of power electronic devices and non-linear loads [17]. Typical non-linear loads include office and

home applications (such as computers, air-conditioners, photostat machines, refrigerators, etc.) as well as large industrial power electronic systems (such as high power motor drives). The nonlinear loads draw non-sinusoidal current from the grid. This nonlinear current leads to non-sinusoidal voltage drops on transformers and power lines, thereby distorting the voltage at the point of common coupling (PCC), where other equipment and loads are connected [18-19]. The excessive harmonic effects can cause many problems such as faster overheat of the equipments, malfunction of the power electronic devices, wiring failure, poor power factor, etc. Non-linear devices are the main source of power quality deterioration [20].

To limit the nonlinear current flowing through the system, the load current is strictly regulated by IEEE 519 [56]. In a high power drive system, due to the low PWM switching frequency for loss reduction, a grid side (front end) rectifier usually uses SHE PWM to eliminate certain low order harmonics in the PWM pattern to improve the line current harmonic performance. However, the grid background harmonics are not considered in this case. In a CSR system, due to the use of an input LC filter (see Figure 1.1), the grid background voltage harmonics (such as 5th or 7th order harmonics) could be amplified by the filter, which results in a high distortion of the line current, although the grid voltage harmonics are low.

To actively compensate the grid background harmonics and to avoid the amplification of certain harmonics in the line current, the concept of active harmonic compensation has been proposed for grid-interfacing converter systems [27-29]. For active harmonic compensation, the grid-interfacing converter operates as an active power filter at the harmonic frequencies. However, this harmonic compensation requires a relatively high converter switching frequency of at least a few thousands hertz [24-25] [27-29]. This is not feasible in a high power medium voltage CSR system, where the converter usually operates at a few hundred hertz switching frequency to reduce the losses. None of the existing CSC PWM techniques reviewed earlier in this chapter can provide the active harmonic compensation with such a low switching frequency.

In order to actively compensate the grid background harmonics, and at the same time operate the current source drive system at a low switching frequency, new PWM techniques are required for the CSR.

1.2 Thesis objectives

The main objective to be realized in this thesis is the minimization of line current harmonic distortions in a high power CSR system. More specifically, the thesis is aimed at developing a PWM scheme that can be used to actively compensate the grid background harmonics and improve the line current harmonic performance. The PWM scheme developed should be able to accurately compensate the grid background harmonic effects, while with a very low switching frequency that is suitable for a high power CSR system. It should also be robust to system model parameter (such as line impedance) variations. Note that although the PWM scheme in this thesis is focused on a CSR system, the ideas and techniques related should be able to be extended to the field of voltage source grid-interfacing converters as well.

To achieve that goal, first of all, the traditional SHE PWM and the recently proposed selective harmonic compensation (SHC) PWM [33] need to be reviewed thoroughly, as these PWM methods can shape the PWM current harmonic spectrum and offer excellent potential for achieving the principal objective set in the thesis. The techniques for the switching angles calculation for the SHE and SHC also need to be investigated, as they are directly related to how the PWM current harmonic spectrum can be shaped. In addition, a user-friendly software tool, which can be used to conveniently design the independent switching angles by using the global optimization algorithm, is required to facilitate the switching angles calculation.

In consideration of the disadvantages of the SHE and SHC PWM for line current harmonics control in practice, a new PWM scheme is required to minimize the line current distortion. Unlike the SHC PWM, the new PWM method should be made to avoid the measurement of grid voltage harmonics, which is usually not very high. Moreover, the new PWM scheme should not rely on an exact CSR system model for harmonic compensation, as the model parameters might not be obtained precisely (e.g. the source impedance can vary). Therefore, the second step of the thesis work is to develop a PWM control scheme for the high power CSR system, which can accurately compensate the grid background harmonics, with the benefit of doing away with the defects in the previous SHC scheme.

1.3 Thesis outline

This thesis contains 6 chapters. In the first chapter an introduction is made to the PWM CSC and three relevant PWM control schemes, namely TPWM, SVPWM, and SHE. The challenge of the CSR line current harmonics minimization is presented. The objectives of the thesis are also given in this chapter.

The second chapter is prepared to provide a detailed review of the recently proposed SHC PWM scheme. The SHC PWM can actively compensate the grid background harmonics in a CSR system with a switching frequency of a few hundred hertz. Then the optimization based switching angles calculation methods for the traditional SHE and SHC schemes are presented. A SHE and SHC PWM switching angles calculation software tool developed with a user-friendly interface is also shown in this chapter.

To overcome the disadvantage of the SHC scheme under low grid voltage harmonics or system model parameter variations, a more robust virtual impedance based selective harmonic compensation (VI-SHC) PWM for the CSR is proposed in the third chapter. In this chapter details are provided to elaborate on this active harmonic compensation scheme, including the modeling of the CSR with virtual impedance, design of the virtual impedance, and the on-line implementation scheme.

Chapters 4 and 5 present the Matlab/Simulink simulation results and the realtime experimental verification of the proposed VI-SHC scheme on a 10kVA/208V CSR hardware prototype. The steady-state performance comparisons of the proposed VI-SHC PWM with the traditional SHE PWM and the SHC PWM are conducted. Different transient simulations and experiments are also carried out. The simulation results and the experimental ones are consistent and verify the superior performance of the proposed VI-SHC PWM scheme.

Finally, the conclusion of the thesis work and some suggestions for future research are given in the sixth chapter.

Chapter 2

Selective Harmonic Compensation (SHC) Scheme

High power converters have been commissioned worldwide in the industrial applications, such as pipeline pumps, fans in the cement industry, traction applications in transportation, etc. As has been introduced in Chapter 1, the selective harmonic elimination (SHE) is widely utilized on high power converters for its superior harmonic performance with a low switching frequency.

On the other hand, to actively compensate the grid background harmonics and to avoid the amplification of certain harmonics in the line current, the concept of active harmonic compensation has been proposed for grid-interfacing converter systems [27-29]. For active harmonic compensation, the grid-interfacing converters work like an active power filter at the harmonic frequencies. However, this harmonic compensation requires a relatively high switching frequency of the converter of at least a few thousands hertz [24-25] [27-29]. This is not feasible in high power medium voltage converters, where the power semiconductors are operated with a few hundred hertz switching frequency to reduce the switching losses. Furthermore, the traditional SHE modulation, while being able to eliminate certain harmonics in the PWM current, is not able to actively control the line current harmonics.

A newly developed method for accomplishing this is the selective harmonic compensation (SHC) PWM [33]. It has been shown that based on the transfer functions derived from the CSR system equivalent circuit, the obtained source voltage harmonics information can be used to generate the relevant harmonic reference current in the PWM process, which would in turn improve the line

current. Nevertheless, this PWM scheme is not without drawbacks. In a practical system, it is hard to determine the exact CSR circuit transfer functions because of the possible variation of system parameters (e.g. source impedance). Moreover, the grid voltage distortion is usually not significant, which makes it difficult to measure.

In this chapter, the SHC PWM will firstly be reviewed. The method for independent switching angles (free angles) calculation of both SHE and SHC schemes will then be presented. An optimization tool developed based on Matlab/GUI (graphical user interface) for the SHE and SHC switching angles calculation (with global optimization) will also be presented.

2.1 Review of the SHC PWM scheme

2.1.1 The principles of the SHC scheme

In a CSR system, the grid source voltage v_s and PWM current i_w can be treated as two independent sources, as is shown in Figure 2.1. Here the PWM current i_w can be represented as a controlled current source which is determined by the PWM switching pattern and DC current:

$$\overline{I_w} = \overline{S_p} \times I_{dc} \tag{2.1}$$

where $\overline{S_p}$ is the PWM switching pattern.

Based on the superposition principle, the equivalent circuit in Figure 2.1 can be split into two individual parts as illustrated in Figure 2.2 (a) and (b). Then the transfer function from the voltage source v_s to the line current i_{s1} , and the transfer function from the current source i_w to the line current i_{s2} can be obtained respectively, as given in (2.2) and (2.3):

$$TF_{is1_vs}(s) = \frac{i_{s1}(s)}{v_s(s)} = \frac{sC_f}{s^2 L_f C_f + sR_s C_f + 1}$$
(2.2)

$$TF_{is2_iw}(s) = \frac{i_{s2}(s)}{i_{w}(s)} = \frac{1}{s^{2}L_{f}C_{f} + sR_{s}C_{f} + 1}$$
(2.3)

Note here $i_s = i_{s1} + i_{s2}$.



Figure 2.2 Separation of two excitations in the CSR system

As is described in [33], the SHC scheme utilizes the PWM switching harmonic effect i_{sh2} to compensate the grid background harmonic effect i_{sh1} according to the transfer functions (2.2) and (2.3). For a complete grid background harmonic compensation, i_{sh2} should have the same amplitude and 180° phase angle difference compared to i_{sh1} , as is described in (2.4) and (2.5).

$$I_{sh2} = I_{sh1} \tag{2.4}$$

$$\varphi_{i_{sh2}} = \varphi_{i_{sh1}} \pm \pi \tag{2.5}$$

where I_{sh1} , I_{sh2} , $\varphi_{i_{sh1}}$ and $\varphi_{i_{sh2}}$ are the magnitudes and phase angles of i_{sh1} and



Figure 2.3 Principles of the SHC scheme



Figure 2.4 A demonstrated 7-pulse SHC PWM pattern

 i_{sh2} , respectively. The overall compensation process is shown in Figure 2.3.

2.1.2 SHC PWM switching pattern

The SHC switching pattern in [33] is designed based on the traditional SHE scheme. The major difference lies in the removal of a constraint on quarter-wave symmetry of the PWM waveform in the SHC scheme (one constraint of the traditional SHE switching pattern is that the pattern must be an inverse mirror image on either side of the 30° and 150° positions [15-16], which guarantee the quarter-wave symmetry). This is necessary as both the magnitude and phase angle of the harmonics need to be controlled in the SHC PWM [33-35] (note that the half wave symmetry is still maintained).

An example 7-pulse SHC PWM pattern is shown in Figure 2.4. It can be observed that the 7-pulse PWM waveform has seven free angles: θ_1 , θ_2 , θ_3 , θ_4 , θ_5 , θ_6 and θ_7 . (Note that the traditional 7-pulse SHE pattern only has three free angles). This pattern still maintains the half-wave symmetry, and guarantees that there will be only two switches conducting anytime while the zero state is not used. The rest of the switching angles α_j can be calculated in the same way as equation (1.6). The relationship between the involved harmonic component and the free angles can be derived from Fourier analysis:

$$I_{ah} = \frac{4I_d}{h\pi} \sin\left(\frac{h\pi}{3}\right) \left(\sum_{i=1}^{7} (-1)^{i+1} \sin\left[h\left(\theta_i + \frac{\pi}{3}\right)\right]\right)$$
(2.6)

$$I_{bh} = \frac{4I_d}{h\pi} \sin\left(\frac{h\pi}{3}\right) \left(\sum_{i=1}^{7} (-1)^{i+1} \cos\left[h\left(\theta_i + \frac{\pi}{3}\right)\right]\right)$$
(2.7)

h=1, 5, 7, 11, 17...

The expression of h^{th} harmonic of the PWM switching pattern signal, denoted as i_{wh}^* , can be obtained as given in (2.8).

$$i_{wh}^{*} = \frac{i_{wh}}{I_d} = f_{iw-\theta}(\theta_1, \theta_2, \theta_3, ..., \theta_{N_A})|_h = \frac{\sqrt{I_{ah}^2 + I_{bh}^2}}{I_d} \sin\left(hw_1 t + \tan^{-1}\left[\frac{I_{bh}}{I_{ah}}\right]\right)$$
(2.8)

h=1, 5, 7, 11, 17...

where *h* is the order of the involved harmonic; N_A is the number of independent PWM pattern angles and I_{ah} and I_{bh} are the Fourier coefficients.

The PWM signal s_{p_i} can also be expressed as the sum of a series of harmonic components as shown in (2.9):

$$s_p(wt) = C_0 + \sum_{h=1}^{\infty} \left[M_h \sin\left(hwt + \varphi_h\right) \right]$$
(2.9)

where C_0 is the DC component of the signal which is zero here; M_h is the magnitude of the h^{th} harmonic component and φ_h is the phase angle of the h^{th} harmonic component, as are expressed in (2.10) and (2.11):

$$M_{h} = \frac{\sqrt{I_{ah}^{2} + I_{bh}^{2}}}{I_{d}}$$
(2.10)

$$\varphi_h = \tan^{-1} \left(\frac{I_{bh}}{I_{ah}} \right) \tag{2.11}$$

Due to the constraint of the quarter-wave symmetry, the traditional SHE PWM pattern has: $I_{bh} = 0$, $|i_{wh}^*| = M_h = \frac{I_{ah}}{I_d}$, $\varphi_h = 0$. Therefore, it is unable to control the phase angles of the PWM pattern harmonic component. However, with the SHC PWM pattern, by modifying the free angles, both I_{ah} and I_{bh} can be controlled to regulate the h^{th} harmonic of the PWM pattern. With this capability, the SHC PWM can be utilized to actively generate harmonics in the PWM current and compensate the system background harmonics.

2.1.3 On-line implementation of the SHC scheme

According to the SHC compensation principles illustrated in Figure 2.3, the reference of the h^{th} PWM current harmonic i_{wh_ref} can be obtained as equation (2.12) and (2.13):

$$I_{wh_ref} = I_{sh2} \bullet \frac{1}{M_{TF_i_{s2}_i_{w}}} = V_{sh} \bullet \frac{M_{TF_i_{s1}_v_{s}}}{M_{TF_i_{s2}_i_{w}}}$$
(2.12)

$$\varphi_{i_{wh}_ref} = \varphi_{i_{sh2}} - \varphi_{TF_i_{s2}_i_{wh}} = \varphi_{vs} + \varphi_{TF_i_{s1}_v_{sh}} - \varphi_{TF_i_{s2}_i_{wh}} \pm \pi$$
(2.13)

where I_{wh_ref} and $\varphi_{i_{wh_ref}}$ are the magnitude and phase angle of i_{wh_ref} ; I_{sh2} and $\varphi_{i_{sh2}}$ are the magnitude and phase angle of the PWM current harmonic effect i_{sh2} shown in Figure 2.3. V_{sh} and φ_{vs} are the magnitude and phase angle of the background voltage harmonic v_{sh} ; $M_{TF_i_{s1_}v_{sh}}$ and $\varphi_{TF_i_{s1_}v_{sh}}$ are the magnitude and phase angle of the transfer function of (2.2) at the h^{th} harmonic frequency; $M_{TF_i_{s2_}i_{wh}}$ and $\varphi_{TF_i_{s2_}i_{wh}}$ are the magnitude and phase angle of the transfer function of (2.3) at the h^{th} harmonic frequency.

Thus, the reference of the h^{th} harmonic of the PWM pattern signal can be obtained as (2.14) and (2.15):

$$S_{Ph_ref} = \frac{I_{wh_ref}}{I_d}$$
(2.14)

$$\varphi_{s_{Ph_ref}} = \varphi_{i_{wh_ref}} \tag{2.15}$$

where S_{Ph_ref} and $\varphi_{s_{Ph_ref}}$ are the magnitude and phase angle of the h^{th} harmonic reference of the pattern signal. The h^{th} PWM current harmonic reference normalized to the DC current can then be expressed in the form of vector as given in (2.16):

$$\overline{S_{Ph_ref}} = S_{Ph_ref} e^{j\varphi_{SPh_ref}}$$
(2.16)

Equation (2.16) can be substituted into the cost function (1.11) for the calculation of the free angles, which lead to the PWM pattern that contains h^{th}

harmonic with the normalized magnitude of $S_{Ph ref}$ and the phase angle of

 $\varphi_{s_{Ph_ref}}$.

For the free angles calculation, targeting the minimization of the cost function, the optimization algorithms (solvers) incorporated in the Optimization Toolbox of the Matlab are most commonly used. These algorithms are capable of solving linear, quadratic, and nonlinear optimization problems with and without constraints [36-37]. However, all these algorithms cannot be used for on-line computation due to the large number of iterations they need to obtain the result. A compromising way to solve this problem is to use a look-up table to store the pre-calculated switching angles as described in [33]. By measuring the grid background harmonics using Sliding DFT (SDFT) technique [38-39], which is very suitable for real-time implementation, the desired PWM harmonics reference can be produced as discussed earlier and the associated switching angles can be obtained through the look-up table.

To obtain such a table, the nominal PWM pattern reference $\overline{S_{Ph_ref}}$ needs to be determined first. The range of $\overline{S_{Ph_ref}}$ should be defined according to the



Figure 2.5 SHC on-line implementation diagram

compensation capability, e.g. from 0% to 8% for the magnitude (p.u. value normalized to DC current reference) and from -180° to 180° for the phase angle range (relative to the h^{th} phase). As a result, a two-dimension table with respect to the magnitude and phase angle can be obtained for the pre-determined range of the magnitude and angle with certain resolution, such as 0.2% for the magnitude and 5° for the angle.

The on-line implementation diagram is shown in Figure 2.5, where the DC current is adjusted by a delay angle control loop so that the modulation index (m_a) can be maintained at its maximum value. With the measurement of h^{th} background harmonic in the source voltage, the reference PWM pattern can then be determined, and the magnitude and phase angle of the h^{th} PWM pattern harmonic reference which can be on-line calculated using (2.12) and (2.13). Then by using the pre-determined look-up table, the desired PWM switching angles can be indexed by the magnitude and phase angle of the h^{th} PWM pattern harmonic reference.

It is worth noting that this two-dimension look-up table based method can only compensate one harmonic (e.g. 5thor 7th only). If more harmonics are to be considered, the look-up table becomes multi-dimensional and may consume considerable memory. However, if the switching angles in the table do not change abruptly, interpolation techniques can be adopted and a smaller size table could be used as will be discussed later.

2.2 SHE and SHC free angles calculation

For either off-line PWM or on-line implementation using the look-up table, the PWM switching angles need to be calculated accurately for harmonic elimination or compensation. This section describes the PWM angle calculation method for the SHE and SHC schemes.

2.2.1 The optimization approach for SHE and SHC switching angles calculation

According to the SHE algorithm which has been reviewed in Chapter 1, in order to eliminate k harmonics, k equations of (1.8) are needed to be solved

simultaneously (assign the relevant I_{ah} to be zero) so as to obtain k free angles. For example, to eliminate 5th, 7th, and 11th in the PWM current i_w , the following three equations need to be satisfied:

$$I_{a5} = \left(\frac{4I_d}{5\pi}\right) \cos\left(\frac{5\pi}{6} \left[-1 + 2\sum_{i}^{3} \left(-1\right)^{i+1} \cos\left(5(\theta_i - \frac{\pi}{6})\right)\right]\right] = 0$$

$$I_{a7} = \left(\frac{4I_d}{7\pi}\right) \cos\left(\frac{7\pi}{6} \left[-1 + 2\sum_{i}^{3} \left(-1\right)^{i+1} \cos\left(7(\theta_i - \frac{\pi}{6})\right)\right]\right] = 0 \quad (2.17)$$

$$I_{a11} = \left(\frac{4I_d}{11\pi}\right) \cos\left(\frac{11\pi}{6} \left[-1 + 2\sum_{i}^{3} \left(-1\right)^{i+1} \cos\left(11(\theta_i - \frac{\pi}{6})\right)\right]\right] = 0$$

The nonlinear and transcendental equations in (2.17) can be solved by a number of numerical methods. However, it does not always have solutions for these transcendental equations. Therefore, in order to achieve best harmonic elimination or compensation results, the optimization approach is usually used [16].



Figure 2.6 Optimum design process [36]

The optimum design is an iterative process of finding the solution which can to the largest extent minimize the output of the objective function. A typical optimization process is illustrated as Figure 2.6. The main feature of the optimum design process is that it requires the designer to identify explicitly a set of design variables, an objective function to be optimized, and the constraint functions for the system.

The optimization of the SHE and SHC free angles can be classified as a typical constrained optimum design problem. In terms of the SHE angle design, the free angles are the design variables; the objective (cost) function is given as (1.11) (which can be related to the PWM or line current THD with adjustable weighting factors on the harmonics of interest); and the constraints on the design variables are listed as (1.10). For the SHC free angles design, the objective function and the free angles constraints need to be revised.

Since the SHC PWM pattern needs to generate harmonic for background harmonic compensation, the relevant harmonic reference is needed to be incorporated into the objective function:

$$C = w_H \bullet \left| S_{PH_ref} e^{j\varphi_{SPH_ref}} - M_H e^{j\varphi_H} \right|^2 + \sum_{h=5}^{103} w_h \bullet \left| M_h e^{j\varphi_h} \right|^2$$
(2.18)

where *H* is the order of harmonic which needs to be generated for the relevant harmonic compensation; h=5, 7, 11, 13, 17, ..., 103, excluding *H*; $S_{PH_ref}e^{j\varphi_{spH_ref}}$ is the *H*th harmonic vector reference which has been given in (2.16); $M_h e^{j\varphi_h}$ is the *h*th harmonic vector of the SHC PWM pattern, its magnitude M_h and phase angle φ_h can be obtained through equation (2.6), (2.7), (2.10) and (2.11); w_h is the weighting factor for the *h*th harmonic. It can be found from (2.18) that all the harmonic references except the *H*th harmonic are set to zero. By doing this, the *H*th harmonic will be generated according to its reference for selective harmonic cancellation, while all other harmonics are minimized towards zero.

With regards to the constraints for the free angles, N_A (free angles number) equals N_P (PWM pulse number in half fundamental cycle) for the SHC scheme now.

Additionally, it is worth noting that the delay angle control is implemented for DC link current reference I_{d_ref} tracking. Therefore, the fundamental phase angle φ_1 must be kept as a constant so that the control of DC link current will not be affected. This is not an issue in the traditional SHE scheme since the Fourier coefficient of the SHE PWM pattern I_{bh} is zero, meaning that the h^{th} PWM current

harmonic's phase angle $\varphi_h = \tan^{-1} \left(\frac{I_{bh}}{I_{ah}} \right)$ is always zero. However, in the case of

SHC scheme, φ_h is not a constant and the PWM fundamental current phase angle φ_1 could change after updating the PWM patterns. Therefore, the constraint $\varphi_1=0$ should be added to make sure that φ_1 is kept at zero when updating the SHC PWM switching angles. In the optimum design program, the inequality constraint

$$|\varphi_1| = \left| \tan^{-1} \left(\frac{I_{b1}}{I_{a1}} \right) \right| < e$$
 is used, where *e* is a very small value. Thus the constraints

for the SHC free angles can be obtained as (2.19):

$$\begin{aligned} \theta_{2} - \theta_{1} &\geq r \\ \theta_{3} - \theta_{2} &\geq r \\ \vdots \\ \theta_{k} - \theta_{k-1} &\geq r \\ \frac{\pi}{3} - \theta_{k} &\geq r \\ |\varphi_{1}| &= \left| \tan^{-1} \left(\frac{I_{b1}}{I_{a1}} \right) \right| < e \end{aligned}$$

$$(2.19)$$

where θ_k is the free angle, *r* is the minimum pulse width and *e* is the limitation value for φ_1 .

In this work, the Matlab Optimization Toolbox is utilized to accomplish the optimum design of the SHE and SHC switching angles. Table 2.1 summarizes the solvers in the Optimization Toolbox for some typical minimization problems [37]. The syntax of invoking an optimization function is generally of the form given in (2.20). The optimization parameters can be modified through the "options" command available as can be observed in (2.20).

[x, FunValue, ExitFlag, Output] = fminX ('ObjFun', . . ., options) (2.20)
Туре	Formulation	Solver
Scalar minimization	Find x to minimize $f(x)$	fminbnd
	subject to $x_l < x < x_u$ (x is a scalar)	
Unconstrained minimization	Find x to minimize $f(\mathbf{x})$ (x is a vector)	fminunc, fminsearch
Constrained minimization	Find x to minimize $f(\mathbf{x})$	fmincon
	Subject to $\mathbf{A} \cdot \mathbf{x} \leq \mathbf{b}$, $\mathbf{A} \cdot \mathbf{q} \cdot \mathbf{x} = \mathbf{b} \cdot \mathbf{q}$.	
	$c(\mathbf{x}) \le 0, ceq(\mathbf{x}) = 0,$ $x_{il} \le x_i \le x_{iu}, i=1 \text{ to m.}$	
	$x_{il} \le x_i \le x_{iu}$, $i=1$ to m.	
Linear programming	Find x to minimize $f(\mathbf{x}) = \mathbf{c}^T \mathbf{x}$	linprog
	Subject to $\mathbf{A} \cdot \mathbf{x} \leq \mathbf{b}$, $\mathbf{A} \cdot \mathbf{q} \cdot \mathbf{x} = \mathbf{b} \cdot \mathbf{q}$.	
Quadratic programming	Find x to minimize $f(\mathbf{x}) = \mathbf{c}^T \mathbf{x} + \frac{1}{2} \mathbf{x}^T H \mathbf{x}$	quadprog
	Subject to $\mathbf{A} \cdot \mathbf{x} \leq \mathbf{b}$, $\mathbf{A} \cdot \mathbf{q} \cdot \mathbf{x} = \mathbf{b} \cdot \mathbf{q}$.	

Table 2.1 Traditional Matlab solvers for minimization problems [37]

In (2.20), the left side of the statement represents the quantities returned by the *"function"*. On the right side, *"fminX"* represents one of the functions presented in Table 2.1. There can be several arguments for the function *fminX*; e.g., starting values for the variables; upper and lower bounds for the variables; M-file names containing objective functions and their gradients ('ObjFun'); optimization algorithm related data, etc [37].

2.2.2 SHE and SHC angles calculation using Matlab global optimization

As is described above, the optimum design of the SHE and SHC free angles is a process of finding the solution which can minimize the output of the objective function. The solutions are called minima, which have two types: local minimum and global minimum. As is illustrated in Figure 2.7, a local minimum of a function is a point where the function value is smaller than or equal to the value at nearby points, but possibly greater than a distant point. A global minimum is a



Figure 2.7 Global minimum and local minimum

point where the function value is the smallest [40].

Generally, traditional Optimization Toolbox solvers in Matlab (e.g. *fmincon*) can only find a local minimum. These solvers work well enough for the cases where there are not many variables. Since in these cases, there are not many combinations of the variables, and thereby not many solutions (local minima) can be found for the same cost function. As a result, the global minima can be easily obtained by comparing the local minimums. However, due to the substantial variations of the SHE free angles of the PWM pattern with very large pulse number (e.g. in the case a CSI is driving a low speed motor with a low fundamental frequency, the PWM pattern pulse number could be very high), thousands of different local minima could be found for the minimization of the same objective function. In this case, finding the global minimum using the

Solver	Convergence	Characteristics
GlobalSearch	Fast convergence to local	Deterministic iterates
(Global Search)	optima for smooth	Gradient-based
	problems.	Automatic stochastic start points
		Removes many start points
		heuristically
MutiStart	Fast convergence to local	Deterministic iterates
	optima for smooth	Can run in parallel
	problems.	Gradient-based
		Stochastic or deterministic start points,
		or combination of both
		Automatic stochastic start points
		Runs all start points
		Choice of local solver: fmincon,
		fminunc, lsqcurvefit, or lsqnonlin
patternsearch	Proven convergence to	Deterministic iterates
(Pattern Search)	local optimum, slower	Can run in parallel
	than gradient-based	No gradients
	solvers.	User-supplied start point
ga	No convergence proof.	Stochastic iterates
(Genetic Algorithm)		Can run in parallel
		Population-based
		No gradients
		Automatic start population, or user
		supplied population, or combination of
		both
simulannealbnd	Proven to converge to	Stochastic iterates
(Simulated Annealing)	global optimum for	No gradients
	bounded problems with	User-supplied start point
	very slow cooling	Only bound constraints
	schedule.	

Table 2.2 Characteristics of the global optimization solvers in Matlab 2010a [40]

traditional optimization solvers could be very challenging [36] [41]. The same problem exists in the SHC free angles computation. To solve this issue, a proper global optimization algorithm needs to be integrated into the optimum design [40]. A summary of the global optimization algorithms is given in the Appendix of this thesis.

Since version 2010a, Matlab starts to be integrated with global optimization tool box which can be utilized to efficiently tackle global optimization problems. This tool box includes Global Search (GS), Multistart (MS), Pattern Search (PS), Genetic Algorithm (GA), and Simulated Annealing (SA) solvers. While, the basic description and discussion of the aforementioned solvers is presented in the Appendix, the characteristics of each solver are shown in Table 2.2. The general recommendations for choosing the suitable global solver are also given, as is shown in Table 2.3 [40].

According to [40], solver GS features faster convergence speed to local optima compared with the other solvers. It is also very efficacious in most optimization cases. GS is thereby selected as the global optimization algorithm for the SHE and SHC free angles calculation.

2.3 A developed free angles calculation tool

A user-friendly SHE angles calculation tool has been built using Matlab 2010a/GUI (graphical user interface) for convenient and efficient optimization designs of the SHE free angles. Specifically, this GUI features the function of designing the globally optimal switching angles of the SHE with PWM pattern pulse number up to 71. The maximum pulse number can be easily increased. Therefore, the tool can be used for a CSI system driving the motor at low speed

Desired Solution	Smooth Objective and	Nonsmooth Objective or
	Constraints	Constraints
Single global solution	GlobalSearch, MultiStart,	patternsearch, ga,
	patternsearch, ga,	simulannealbnd
	simulannealbnd	
Multiple local solutions	MultiStart	
using parallel processing		
Single global solution	MultiStart	patternsearch, ga
using parallel processing		

Table 2.3 Recommendations for choosing a global optimization solver [40]



Figure 2.8 GUI of the developed SHE angles computation software tool

(with a low fundamental frequency). For the SHE PWM, only quarter-wave symmetrical SHE is considered. For the SHC scheme, the embedded algorithm should be changed for quarter-wave asymmetrical SHE (as has been introduced in Section 2.1.2 and 2.2.1). The GUI of this the SHE angles calculation tool is shown in Figure 2.8.

2.3.1 Description of the switching angles computation tool

As is displayed in Figure 2.8, this interface is mainly composed of 6 parts: Symmetrical SHE Parameters Settings panel, Command Buttons, Result Display panel, Faults Information display panel, Optimization Process Status Display panel, and Simulated PWM Pattern Waveform display panel. The following text gives a brief description of each component.

A. Symmetrical SHE Parameters Settings

This panel is used for SHE parameters settings. The panes are editable and are used for relevant parameters entry. Specifically,

• "Number of Pulses"

This item controls the number of the pulses of the PWM pattern needs to be designed. As is mentioned above, the highest number of pulses is 71 (can be easily increased if higher number is needed).

• "Number of Free Angles"

Once the N_P is typed in, the corresponding N_A will be generated automatically.

• "Weighting Factors for Harmonics Minimization"

Each editable pane in this panel controls the weight of each harmonic needs to be minimized, i.e., the greater the weight, the higher priority the relevant harmonic will gain for harmonic minimization. The objective function of the embedded SHE algorithm is actually THD^2 including individual harmonic weighting factor, as shown in (1.11). The highest harmonic order considered here is 103^{rd} .

B. Global Optimization Parameters Setting

This control panel contains editable panes for global options required by the Global Search algorithm in Matlab 2010a. The functions as well as the setting of each parameter are briefly introduced in the Appendix.

C. Command Buttons

As can be seen from Figure 2.8, there are four buttons on the interface: "Initialization", "Start Optimization Computation", "Reset Weighting Factor for each Harmonic" and "Reset Global Options". These functions are used to facilitate the optimum design progress.

D. Results display panel

This panel output the results of the optimization. It contains the optimal free angles obtained, the spectrum of the relevant PWM pattern and its THD.

E. Faults Information display panel

This panel reminds the errors made in entering the parameters value.

F. Optimization Process Status

This window displays the current status of the optimization procedure.

G. Simulated PWM pattern waveform

Once the optimal free angles are obtained, they will be transferred into the corresponding Simulink model to simulate the PWM pattern waveform and the generated waveform will be illustrated in this window.

An example of a 5-pulse PWM with 5th and 7th harmonic elimination is used to illustrate the use of this developed tool, and the results are shown in Figure 2.8. It can be seen that the number of pulses is set to 5, and the weighting factors for H5 and H7 (5th and 7th harmonics) are set to a relatively high value (10000). The result shows the optimal free angles obtained through optimization process, spectrum of the designed PWM pattern (where the magnitudes of 5th and 7th harmonics are almost zero). Additionally, the simulated SHE PWM pattern is also displayed on the GUI.

2.3.2 Using the software tool for the SHC angles calculation

As has been stated earlier, this developed free angles computation tool can be modified for the quarter-wave asymmetrical SHE pattern free angles calculation by removing the constraint on quarter-wave symmetry (as is described in Section 2.1.2). Moreover, this tool can be further modified for SHC free angles calculation, simply by including the reference harmonics into the cost function and revising the constraints according to Section 2.2.1.

Further modifying the program for automatic calculation of switching angles in a pre-defined range with the PWM harmonic reference, the SHC switching angle look-up table can be obtained. The graphics of the calculated independent switching angles (θ_1 to θ_7) of the 7-pulse SHC PWM pattern associated with the 5th PWM harmonic reference ($\overline{S_{P5_ref}}$) are shown in Figure 2.9. In this case, the normalized reference magnitude range and phase angle range are 0% to 8% and -180° to 180°, respectively. It can be seen from the plots that the PWM switching angles have relatively smooth trends with the variation of the magnitude and phase angle of $\overline{S_{P5_ref}}$. Therefore, the size of the look-up table does not need to be very large, as interpolation techniques can be used in a considerable range of the table.



Figure 2.9 Look-up tables of the 7-pulse SHC PWM pattern free angles regarding $\overline{S_{P5_ref}}$

2.4 Summary

This chapter reviews a recently developed harmonic compensation scheme (SHC), which can be used in high power converters with a very low switching frequency. Then the SHE and SHC free angles calculation techniques are presented. To accurately obtain the free angles for both the SHE and SHC schemes, a global optimization based method is developed with THD² as the objective function. Adjustable weighting factors in the method can flexibly realize different harmonics optimization purpose. A software tool based on Matlab Global Optimization Toolbox is also developed to carry out the switching angle calculation task with a convenient user interface.

Note that although the thesis work is focused on the grid side CSR system, the developed user-friendly switching angle calculation tool can be equally used for a CSI. For a CSI-drive at low speed, the SHE or SHC PWM with high number of pulses (at low fundamental frequency) can be easily obtained with the developed software tool.

Chapter 3

Virtual Impedance Based Selective Harmonic Compensation (VI-SHC) PWM

The SHC PWM scheme and its on-line implementation scheme are presented. The SHE or SHC switching angle calculation approach and the developed software tool are also discussed. While effective for grid background harmonics compensation, the SHC PWM is based on measuring the grid harmonic current and an assumption of the system model transfer function, which may not be very practical in real applications. In this chapter, a virtual impedance based SHC (VI-SHC) PWM method is proposed to address the implementation disadvantages of the traditional SHC method. The virtual impedance design and relevant analyses of the VI-SHC are presented in this chapter. The simulation and experimental verification, as well as the performance comparison of the proposed VI-SHC PWM with the traditional SHE and the recently proposed SHC schemes are provided in Chapters 4 and 5.

3.1 Implementation disadvantages of the SHC scheme

The SHC PWM is suitable for high power application as it uses a very low switching frequency (comparable to the traditional SHE PWM) for the grid background harmonic compensation. For implementation on a CSR system, the SHC scheme requires a very detailed and precise model of the converter system, including the source impedance, filter inductance and capacitance. This CSR model is then used to determine the equivalent circuit transfer functions for reference PWM harmonics generation. However, determining the exact CSR system parameters is difficult in practice due to the possible variation of the source impedance [33].

Moreover, the SHC scheme requires the measurement of grid voltage harmonics in the reference PWM current generation process. The voltage harmonics are usually very subtle at the medium voltage level, which makes it difficult to measure accurately. Combining the voltage harmonics measurement error and the CSR model inaccuracy, the compensation effects are not as good as desired, especially when the grid voltage harmonics are not very high (note that the grid line current distortion can still be significant even when the grid voltage harmonics are small, as the CSR input filter may amplify certain harmonics [42-43]).

To well overcome the aforementioned implementation drawbacks, a selective harmonic compensation scheme using the virtual impedance concept (VI-SHC) can be used. This method compensates for the pre-existing grid background harmonics using only the line current measurement, and provides superior line current harmonic performance.

3.2 Virtual impedance based SHC PWM

The virtual impedance concept has been increasingly used in power converters or active damping of the converter filter circuit [43-45], converter output power flow control [46-48], system harmonics compensation [43] [49], etc. In different applications, virtual resistance, virtual inductance, virtual capacitance or combination of them has been used [46-49]. Generally, the virtual impedance is realized through the control of a power converter and it does not involve the physical loss as in a real impedance.

Combining the virtual impedance concept with the recently proposed SHC PWM scheme, an improved SHC scheme can be developed, and is called virtual impedance SHC (VI-SHC) scheme. In the proposed VI-SHC scheme, only the line current is measured as the feedback, and the extracted harmonic in the line current is used to realize a virtual impedance at the harmonic frequency. Figure 3.1 (a) shows the basic idea of the VI-SHC scheme. As can be seen, the h^{th} line



(b) Reference harmonic generation in SHC scheme Figure 3.1 Comparison of the VI-SHC and the SHC schemes

current harmonic to be compensated ($\overline{I_{sh}}$) is acquired using the SDFT method on the measured line current. $\overline{I_{sh}}$ is then used to realize the virtual impedance control by multiplying a coefficient k. As will be discussed later in this chapter, different k (real number, imaginary number or complex number) will be related to different types of virtual impedance. The virtual impedance block output is the h^{th} PWM current harmonic reference $\overline{I_{wh_ref}}$, which is next used for PWM generation. In comparison with the SHC scheme implementation shown in Figure 3.1 (b), the virtual impedance features two advantages:

- The proposed VI-SHC scheme compensates the system background harmonics using the line current measurement instead of the source voltage in the SHC scheme. Therefore the VI-SHC PWM is more practical in the real applications, since the voltage distortion is usually too subtle for accurate measurement.
- As the PWM output in a CSR system is directly related to the line current, the VI-SHC method is essentially a closed-loop compensation scheme by feeding back the line current harmonics. Therefore, it does not require the detailed and precise system parameters for the derivation of the system transfer functions.

To further prove that the virtual impedance based SHC can effectively reduce the line current harmonics, the CSR system equivalent circuit, shown in Figure



Figure 3.2 CSR equivalent circuit



Figure 3.3 CSR equivalent circuit with virtual impedance

3.2 (a), is transformed to Figure 3.2 (b) according to Thevenin's theorem. In Figure 3.2 (b), $\overline{V_{Th}}$ and Z_{Th} are the Thevenin equivalent voltage and Thevenin equivalent impedance respectively, and are expressed as equation (3.1) and (3.2).

$$\overline{V_{Th}} = -\frac{\overline{I_{wh}}}{jw_h C_f}$$
(3.1)

$$Z_{Th} = \frac{1}{jw_h C_f} \tag{3.2}$$

where h is the harmonic order.

To properly emulate a virtual impedance in the Thevenin equivalent circuit, the line current is fed back and is multiplied by a gain *k* to generate the PWM current reference harmonic $\overline{I_{wh}}$ in the VI-SHC scheme, as given in (3.3):

$$\overline{I_{wh}} = k \bullet \overline{I_{sh}} \tag{3.3}$$

Subsequently, it can be obtained that:

$$\overline{V_{Th}} = \overline{I_{sh}} \cdot \frac{-k}{jw_h C_f}$$
(3.4)

Finally, Figure 3.2 (b) can then be represented by Figure 3.3, where Z_{vh} is the virtual impedance and it is represented as in (3.5):

$$Z_{vh} = \frac{-k}{jw_h C_f} \tag{3.5}$$

Comparing Figure 3.2 (b) with Figure 3.3, it can be found that the virtual impedance Z_{vh} is utilized to represent the Thevenin equivalent voltage $\overline{V_{Th}}$, and Z_{vh} is related to the coefficient k. The expression of line current harmonic $\overline{I_{sh}}$ can then be derived as in (3.6):

$$\overline{I_{sh}} = \frac{\overline{V_{sh}}}{R_s + jw_h L_f + Z_{Th} + Z_{vh}}$$
(3.6)

Obviously, the virtual impedance can help to reduce the harmonics in the line current by properly shaping the system equivalent model. Further considering that k can be selected as a real number, an imaginary number or a complex number, different types of virtual impedance (resistive, inductive, capacitive or combination of them) can be realized. More detailed analysis and design of the virtual impedance will be presented in the next section.

3.3 Design of the virtual impedance

As is described above in Section 3.2, k can be taken as a real number, an imaginary number or a complex number. Different k has different physical meanings for the virtual impedance. In this section, the analysis of the impacts of k on the compensation effects and system stability is presented, which leads to the optimal design of the virtual impedance.

3.3.1 CSR system model

To facilitate the design of virtual impedance in the proposed PWM scheme, the CSR system model is first derived. The CSR system model can be built in the format of block diagram (at the h^{th} harmonic frequency) based on Figure 3.2 (a), as is shown in Figure 3.4, where $TF_{i_{s1}-v_s}$ is the transfer functions from the voltage source v_s to the line current i_{s1} while $TF_{i_{s2}-i_w}$ is the transfer function from the current source i_w to the line current i_{s2} , as given in equation (2.2) and (2.3), and are



Figure 3.4 Block diagram of CSR system using VI-SHC scheme at the h^{th} harmonic frequency



Figure 3.5 Bode plot of SDFT transfer function

again listed here in (3.7) and (3.8); i_{sh1} is the line current harmonic induced by the background voltage harmonic distortion v_{sh} ; i_{sh2} is the line current harmonic effect of the PWM current harmonic which is intentionally generated through VI-SHC scheme.

$$TF_{i_{s1} v_s}(s) = \frac{i_{s1}(s)}{v_s(s)} = \frac{sC_f}{s^2 L_f C_f + sR_s C_f + 1}$$
(3.7)

$$TF_{i_{s2}}(s) = \frac{i_{s2}(s)}{i_{w}(s)} = \frac{1}{s^{2}L_{f}C_{f} + sR_{s}C_{f} + 1}$$
(3.8)

In the CSR control system, the h^{th} line current harmonic i_{sh} is extracted using the Sliding DFT (SDFT) [38-39]. The *z*-domain SDFT transfer function for the h^{th} harmonic is given as:

$$TF_{SDFT}(z) = \frac{1}{N} \cdot \frac{(1 - z^{-N})e^{j2\pi h/N}}{1 - e^{j2\pi h/N} \cdot z^{-1}}$$
(3.9)

where h is the harmonic order of interest, N is the number of sampling points in one fundamental cycle.



Figure 3.6 Overall block diagram of CSR system with SDFT and one fundamental cycle delay

Figure 3.5 shows the bode plot of the SDFT for the 5thharmonic extraction, with the fundamental frequency of 60Hz and sampling frequency of 2.4 kHz. As can be seen from Figure 3.5, it has unity gain at the harmonic which is to be extracted, while the gains at other harmonics are rather small so as to filter out undesired frequency components. However, it can be seen from Figure 3.5 that the stop band of the SDFT is not excellent which could possibly lead to spectral leakage if inter-harmonics are present [38-39] [50].

The PWM current generation of this control scheme, similar to the SHE PWM pattern, is only updated once in each fundamental cycle. This means in the worst case, there would be one fundamental cycle delay in the PWM current update. Thus, a delay block is added to simulate this effect. Therefore, Figure 3.4 can be further modified to the block diagram shown in Figure 3.6.

Since the CSR system is a discrete system, and for the convenience of analysis, each transfer function in *s*-domain in Figure 3.6 is discretized with the same sampling rate as that of the SDFT: 2.4 kHz. Harmonic order (*h*) is set to 5 since the 5th harmonic is the one which is mostly concerned here. This is because for the CSR system considered in this thesis work, the input LC filter will amplify the 5th harmonic from the grid. Therefore, the transfer functions of the CSR system using the proposed VI-SHC scheme can be obtained as in (3.10) and (3.11).

$$TF_{sys_{-}i_{s}-v_{s}} = \frac{i_{s}(z)}{v_{s}(z)}$$
(3.10)

$$TF_{sys_{-}i_{s}_{-}i_{w}} = \frac{i_{s}(z)}{i_{w}(z)}$$
(3.11)

The system transfer function $TF_{sys_i_s_v_s}$ can be used to analyze the line current harmonic compensation performance under the grid background harmonics. The transfer function $TF_{sys_i_s_i_w}$ can be used to analyze the impacts from the PWM current harmonics with different virtual impedance settings, as the PWM current i_w also contains the inter-harmonics produced by the interaction of DC current ripples and PWM pattern. More detailed analyses will be given in the following sections.

3.3.2 *k* as a real number (virtual inductor)

When k is selected as a real number, the magnitude of the h^{th} line current harmonic can be yielded from (3.6) as:

$$\left|\overline{I_{sh}}\right| = \frac{\left|\overline{V_{sh}}\right| w_h C_f}{\sqrt{(w_h^2 L_f C_f + k - 1)^2 + (R_s w_h C_f)^2}}$$
(3.12)

From equation (3.12), it can be found that the magnitude of k can affect the magnitude of $\overline{I_{sh}}$. Theoretically, from (3.12), if the magnitude of k is high enough, $|\overline{I_{sh}}|$ would be very low regardless of what the sign of k is.

A. System stability analysis

The CSR system transfer functions in *z*-domain are obtained as in (3.10) and (3.11). The system zero-pole map ((3.10) and (3.11) have exactly the same poles) regarding different *k* values is shown in Figure 3.7, where (a) is the zero-pole map when *k* is positive, (b) is the zoomed in view of (a), and (c) is the zoomed in zero-pole map when *k* is negative.

The three circles of poles (denoted using blue, green and red color respectively) in Figure 3.7 (a) represent the system poles when k equals 0.01, 1, and 1.2 respectively. As can be observed in Figure 3.7 (b), the inner circle of poles (blue)



Figure 3.7 Zero-pole map of CSR system transfer function with different k values

is when k is set to a very small value (0.01), and all the poles are inside of the unit circle. The middle circle (green) represents poles while k is set to 1. It can be found that there is one pole on the unit circle, which means k=1 is probably the critical condition in terms of system stability. The outer circle (red) represents poles when k is set to 1.2. It can be observed that there is one pole existing outside of the unit circle, which means the system is no longer stable in this condition. To sum up, according to the zero-pole map analysis, the circle of system poles moves from the inner side towards the outer side as k increases. And the system is in critical state while k is around 1. Therefore it can be concluded that when k is selected as a positive real number, its value cannot exceed 1 to maintain system's stability. Similar conclusion can be drawn from Figure 3.7 (c) that the approximate critical value of k is -0.6 when k is negative. Considering the system in simulation and real-time experiment, with parameters shown in Table 4.1 in Chapter 4 ($L_{s p.u.}=0.15$, $C_{f p.u.}=0.4$ and h=5), it can be obtained that:

$$|w_h^2 L_f C_f + k - 1| = |0.5 + k|$$
 (3.13)

Substituting (3.13) into (3.12), one would find that with the range of k being from -0.6 to 1, setting k as a positive real number will achieve better compensation result. In this way, as can be seen from (3.5), when k is a positive real number the virtual impedance actually is a capacitor with negative capacitance, which is essentially an inductor at the concerned harmonic frequency.

B. Bode plot analysis

The bode diagrams of CSR system transfer functions (3.10) and (3.11) regarding different *k* values are shown in Figure 3.8, where *k* varies from 0 to 1.

It can be found from Figure 3.8 (a) that the magnitude of the bode plot of $TF_{sys_i_s_v_s}$ at 5th harmonic (300Hz) decreases as k increases, which is consistent with the discussion above that a k with higher magnitude would further lower the magnitude of 5th line current harmonic. However, it also can be observed from Figure 3.8 (b) that the bode plot of $TF_{sys_i_s_i_w}$ becomes more drastically distorted as k rises. It has several spikes and the peak value of each spike (e.g. the gain at f=288Hz) increases as k increases. It means the inter-harmonics in the PWM current (caused by DC ripples and PWM pattern) would be amplified with the



Figure 3.8 Bode diagrams of the CSR system transfer function regarding different k values

increase of the k value.

3.3.3 *k* as an imaginary number (virtual resistor)

When k is selected as an imaginary number, assuming k=Bj, equation (3.12) can be revised to:

$$\left|\overline{I_{sh}}\right| = \frac{\left|\overline{V_{sh}}\right| w_h C_f}{\sqrt{(w_h^2 L_f C_f - 1)^2 + (R_s w_h C_f - B)^2}}$$
(3.14)

It can be deduced from (3.14) that a *B* with high magnitude can also reduce $\left|\overline{I_{sh}}\right|$.

A. System stability analysis

With the CSR system transfer function obtained in Section 3.3.1, the zero-pole map of CSR system transfer function regarding different *B* values is shown as Figure 3.9. The 3 groups of poles in Figure 3.9 (a) represent the system poles when *B* equals -0.01 (blue), -1 (green) and -1.2 (red) respectively. According to the zero-pole map analysis, the group of system poles moves from the inner side towards the outer side as the magnitude of *B* increases. And it can be observed that the system is in critical state while B=-1. Similar analysis can be done from Figure 3.9 (b) that the approximate critical value of *B* is 0.65 when *B* is positive. With the system parameters shown in Table 4.1, it can be yielded from (3.14) that:

$$\left| R_{s} w_{h} C_{f} - B \right| = \left| 0.3 - B \right| \tag{3.15}$$



Figure 3.9 Zero-pole map of CSR system transfer function with different B values

where *B* ranges from 0 to 0.65 when it is positive, and from 0 to -1 when it is negative. The highest value of equation (3.15) is 0.35 when *B* is positive, while it is 1.3 when *B* is negative. Thus setting *B* as a negative number would have better compensation effects. Therefore, only negative *B* value is considered here. From equation (3.5), it can be concluded that when *B* is negative the virtual impedance acts as a resistor at the harmonic frequency of concern:

$$Z_{vh} = \frac{-B}{w_h C_f} \tag{3.16}$$

where $B \in [0, -1]$.

B. Bode plot analysis

The bode diagrams of CSR system transfer functions (3.10) and (3.11) regarding different *B* values are illustrated as Figure 3.10, where *B* varies from 0 to -1. It can be found from Figure 3.10 (a) that the magnitude of the bode plot of $TF_{sys_is_vs}$ at 5th harmonic (300Hz) decreases as *B* decreases. On the other hand, it also can be observed from Figure 3.10 (b) that the bode plot of $TF_{sys_is_is_iw}$ becomes more dramatically distorted as *B* drops. The curve has several spikes and the peak value of each spike (e.g. the gains at *f*=277Hz) increases dramatically as *B* decreases. It indicates the other inter-harmonics in the PWM current (caused by DC ripples and PWM pattern) would be augmented with the descent of the *B* value within the limit.





3.3.4 k as a complex number (virtual R-L impedance)

In this case, it is assumed that k=A+Bj. Thus equation (3.12) can be revised to:

$$\left|\overline{I_{sh}}\right| = \frac{\left|\overline{V_{sh}}\right| w_h C_f}{\sqrt{(w_h^2 L_f C_f + A - 1)^2 + (R_s w_h C_f - B)^2}}$$
(3.17)

Similar to the analysis above, a higher *A* and *B* value can also help to minimize $|\overline{I_{sh}}|$. According to the discussions in Sections 3.3.2 and 3.3.3, *A* should be set as a positive number while *B* should be selected as a negative number. In this way, equation (3.5) can be revised to:

$$Z_{vh} = \frac{-A}{jw_h C_f} + \frac{-B}{w_h C_f}$$
(3.18)

It can be found from (3.18) that this virtual impedance is a combination of an inductor and a resistor at the harmonic frequency of concern.



Figure 3.11 Zero-pole map of CSR system transfer function with different A and B values



Figure 3.12 Bode diagrams of the CSR system transfer function regarding different k values

A. System stability analysis

The zero-pole maps of CSR system transfer function regarding different *A* and *B* combinations are shown as Figure 3.11. As is indicated in Figure 3.11 (a), the 3 groups of system poles are corresponding to *k* equals 0.01-*j*0.01 (blue), 0.7-*j*0.7 (green) and 1-*j*1 (red) respectively. Figure 3.11 (b) shows the comparison between the set of poles when k=0.7-*j*0.7 (green) and the set of poles when k=1-*j*0.7 (red). Figure 3.11 (c) illustrates the set of poles when k=0.7-*j*0.7 (green) in comparison with the set of poles when k=0.7-*j*1 (red). Figure 3.11 implies that the magnitude of either *A* or *B* cannot be too large considering the CSR system stability.

B. Bode plot analysis

The bode diagrams of CSR system transfer functions (3.10) and (3.11) regarding different *A* and *B* combinations are illustrated as Figure 3.12, where *A* varies from 0 to 0.7 and *B* varies from 0 to -0.7. It can be observed from Figure 3.12 (a) that with the increase of *A* and decrease of *B*, the gain of the 5th (300Hz) harmonic drops. It is, nevertheless, obvious that the bode plot of $TF_{sys_is_iw}$ is more drastically warped as *A* and *B* varies, as is illustrated in Figure 3.12 (b). Moreover the peak value of each spike (e.g. the gains at around *f*=283Hz) rises with the increase of *A* and descent of *B*, which indicates the other inter-harmonics in the PWM current (caused by DC ripples and PWM pattern) would be augmented with the rise of the *A* and *B* magnitude.

3.3.5 The analytical region of k

In order to obtain the region of k especially when it is set as a complex number, thorough zero-pole map analyses are taken. The border of k value according to the analyses is shown in Figure 3.13. The square-dots in Figure 3.13 represent various critical k values obtained from zero-pole analyses. Combing them together, the square-dotted-curve (black) constitutes the approximate border of the region of k value. It can be observed that the analytical region of k value is like a sector with a radius of around 1.

The region of k values defined from simulation is also given, as is illustrated in Figure 3.13 as the red star-dotted-curve. The red star-dots represent the points where the system is still stable, but starts to have relatively high inter-harmonics. It can be found in Figure 3.13 the boundary defined by simulation is not exactly the same as that from analyses. There are two reasons for this. Firstly, there is one fundamental cycle delay considered in the system model, which is used to simulate the delay caused by SHE PWM current update for the worst case. As this is only a worst case scenario, the k can be set with higher magnitude in the



Figure 3.13 The region of k value defined by both analyses and simulations



Figure 3.14 Vector diagram of the virtual impedance

simulation without causing significant problems most of the time. Secondly, considering the possible amplification of the inter-harmonics in such a system, the virtual impedance would have more damping effects on the inter-harmonics when it acts like a resistor. Therefore when k is an imaginary number, the magnitude of inter-harmonics is lower than the case when k is a real number. This can explain that in the simulation the highest real value of k is around 0.85 while the highest imaginary value of k is around -1.1j.

3.3.6 The optimization of the k value

It is obvious that when k is set as a real or an imaginary number, the critical value of k will provide the best line current harmonic reduction effects. For the case that k is set as a complex number, considering the range of k is limited within an area with a fix radius, the most efficient way is to set the virtual impedance Z_{vh} to have the same impedance angle as the original equivalent circuit impedance Z_{eh} , as is shown in Figure 3.14. By doing this, the vector sum of two impedance can be maximized.

Therefore, the virtual impedance angle can be derived from Figure 3.3 and is expressed in equation (3.19).

$$Ang_{Zvh} = Ang_{Zeh} = \tan^{-1} \left(\frac{w_h L_f - 1/(w_h C_f)}{R_s} \right)$$
(3.19)

where Ang_{Zvh} is the angle of the virtual impedance and Ang_{Zeh} is the angle of the original equivalent circuit impedance.

Regarding the system considered in simulation and real-time experiment, with parameters shown in Table 4.1, the coefficient k can be designed as: 0.83-0.55j.

It appears that the highest virtual R-L impedance obtained from the above analysis should have the best attenuation effects on the line current harmonics. However, in terms of the damping effects of a virtual resistor on the system interharmonics, and the requirement of knowledge of existing equivalent model impedance angle for a R-L impedance, using the virtual impedance as a virtual resistor could be a more practical choice. To further compare the effects of using different types of impedance, Figure 3.15 illustrates the comparison of bode plots of the system transfer functions $TF_{sys_is_vs}$ and $TF_{sys_is_iw}$ while k is set to 0, 1 (maximum real number), -1j (maximum imaginary number) and 0.83-0.55j (analytically designed complex number). It can be seen from Figure 3.15 (a) that the gain of curve d at the 5th harmonic (300Hz) is much lower than curve a and b, but only slightly lower than curve c. Moreover, the peak value of curve c in Figure 3.15 (b) is lower than curve b and d. This comparison shows that the compensation performance of setting k as an imaginary number is very close to that of setting k as a complex number. Therefore, considering the convenience of k value adjustment, and the damping effects from a virtual resistor, setting k as an imaginary number (a virtual resistor) is more practical, and is recommended in this work.

3.4 On-line implementation of the VI-SHC scheme

The on-line implementation of the VI-SHC scheme is based on the look-up table method used in the SHC scheme, as has been introduced in Section 2.1.3. With the pre-determined look-up table, the desired PWM angles can be indexed on-line by the magnitude and phase angle of the on-line calculated h^{th} PWM current harmonic reference $\overline{I^*_{wh_ref}}$, which is generated by multiplying the measured line current harmonic $\overline{i_{sh}}$ by a designed coefficient *k* and normalized to



Figure 3.15 Comparison of bode plots of the CSR system transfer function regarding different *k* values



Figure 3.16 On-line implementation of the proposed VI-SHC scheme

DC current reference $I_{d ref}$ as is shown in Figure 3.16.

Note that this on-line method can effectively compensate one harmonic (e.g. 5^{th} or 7^{th}) using a two-dimensional look-up table. Further considering that the grid voltage are mostly polluted with certain low order harmonics, and at middle voltage level the CSR input LC filter may not be able to mitigate the 5^{th} harmonic, the compensation of the 5^{th} line current harmonic thereby has the highest priority.

If more harmonics are to be considered, the look-up table becomes multidimensional and would consume considerable memory. However, as discussed in the previous chapter, interpolation techniques can be adopted for the table to reduce the memory size, since the obtained switching angle plots (illustrated in Figure 2.9) are continuous and have a relatively linear shape in a considerable region.

3.5 Summary

The principle of the proposed VI-SHC PWM scheme is presented in this chapter for CSR line current harmonics elimination. Compared to the SHC PWM, the proposed VI-SHC scheme compensates pre-existing grid background current harmonic using only the line current measurement and does not need an accurate system model during the compensation process. It is therefore more robust and suitable for practical implementations.

The detailed virtual impedance design procedure is also discussed in this chapter. Three types of virtual impedance are selected based on the analysis: virtual inductor (k is a positive real number), virtual resistor (k is a negative imaginary number) and virtual R-L impedance (k is a complex number). Different types of virtual impedance in the VI-SHC scheme are thoroughly analyzed in terms of CSR system stability and compensation effects. Optimal design of the virtual impedance to achieve the best line current harmonic attenuation is presented. It is found the harmonic performance of a virtual R-L impedance is the best in theory. However, it is very close to the virtual resistor's performance. In consideration of the convenience of k value adjustment and the damping effects on the inter-harmonics associated with a virtual resistor, setting k as an imaginary number (adding a virtual resistor) is more practical and thereby is recommended from this work.

Chapter 4

Simulation Results

Simulations are carried out in Matlab/Simulink to verify the theory and algorithms of the proposed VI-SHC scheme presented in Chapter 3. A CSR system is used in the simulations to test the proposed PWM scheme. The system parameters are given in Table 4.1.

In the simulations, a 0.6% 5th voltage harmonic is added into the background voltage to simulate the scenario that the grid voltage is slightly polluted with 5th harmonic. Note that the simulation parameters are selected to be the same as for the lab CSR prototype in Chapter 5. Also the LC filter at the CSR input is tuned with a resonant frequency of 4.08 p.u. so that the 5th harmonics in the grid will be amplified. In the simulations, four cases are tested:

- Case 1: Steady-state performance of the proposed VI-SHC PWM. It is also compared with the traditional SHE and SHC PWM schemes.
- Case 2: Transient performance of the VI-SHC with grid voltage harmonic variations.

Parameter	Value	
Rated power	10 kVA	
Rated voltage (line-line)	208 V	
DC current	10A	
Fundamental frequency	60 Hz	
DC link inductance L_d	2 p.u.	
DC load resistance R_d	1.46 p.u.	
Line inductance L_s	0.15 p.u.	
Filter capacitance C_f	0.4 p.u.	
Line resistance R_s	0.15 p.u.	
PWM switching frequency	420 Hz (7-pulse)	

Table 4.1 Parameters for simulations and experiments

• Case 3: Transient performance of the VI-SHC with DC current variations.



• Case 4: The VI-SHC scheme with different virtual impedance.

Figure 4.1 Steady-state line current (i_s) , PWM current (i_w) and DC current (I_{dc}) waveforms

4.1 Case 1: Steady-state performance of the VI-SHC scheme

In this case, the steady-state performance of the VI-SHC is compared with the traditional SHE and the SHC schemes. The line current, PWM current and DC link current waveforms of the system using the traditional SHE PWM, the SHC PWM and the proposed VI-SHC PWM are shown in Figure 4.1 (a) to (c) respectively. Obviously, the traditional SHE has the worst line current as it cannot





compensate the source background harmonic (although it is only 0.6% 5th harmonic).

It can be seen from the line current spectra comparison in Figure 4.2 (a), (c) and (e) that the 5th line current harmonic is mitigated from 8.7% (when using SHE) to 3% and 3.5% while the SHC and VI-SHC (with k=-1.1j) schemes are implemented respectively. From the comparison of the PWM current (i_w) spectra illustrated in Figure 4.2 (b), (d) and (f), it is obvious that both SHC and VI-SHC schemes actively generate the 5th PWM current harmonic for the 5th line current harmonic compensation.

It can be concluded from the simulation results that the proposed VI-SHC has very similar harmonic compensation performance as the SHC scheme, and is





Figure 4.3 Steady-state waveforms with inaccurate parameters

much better than the traditional SHE scheme in the case where there is harmonic distortion pre-existing in the background voltage.

It can also be observed from the simulation results that in the ideal situations (i.e., the converter system parameters obtained are accurate) the SHC scheme has better performance than the proposed VI-SHC scheme. This is because SHC scheme use the system model which is very precise in the simulations to compensate the grid harmonics.

However, determining the precise CSR system parameters is difficult in practice due to the possible variation of the source impedance. To emulate effects of system parameter inaccuracy in SHC, the actual system line inductance (L_s) is changed slightly from 0.15 p.u. to 0.1 p.u. while the L_s =0.15 p.u. is still used in the SHC PWM scheme. The waveforms and spectral analyses of the line current and PWM current using the SHC scheme and the proposed VI-SHC scheme are shown in Figure 4.3 and Figure 4.4, respectively.

While the improvement using the VI-SHC under parameter variation is not



(c) Line current spectrum (VI-SHC) (d) PWM current spectrum (VI-SHC) Figure 4.4 Spectral information of the line current and PWM current with inaccurate parameters

very obvious in the time domain waveforms comparison shown in Figure 4.3, the advantages of VI-SHC can be clearly seen in the spectra analysis in Figure 4.4. It can be observed from Figure 4.4 (b) that the PWM current of SHC scheme has similar spectrum as Figure 4.2 (d), as the same system model parameters are used here for the PWM reference current generation. However, as the actual line inductance has been changed, the compensation is not very accurate, leading to the significant 5th harmonic existing in the line current as shown in Figure 4.4 (a).

On the contrary, for the proposed VI-SHC method, the line current 5th harmonic and THD shown in Figure 4.4 (c) are smaller compared to the SHC scheme. This is due to the robustness of the proposed VI-SHC under system parameter variations.

Moreover, the challenge regarding the harmonic measurement is not applicable here, as in the simulation, the 5th harmonic (although very small) of the background voltage can be accurately measured. However this effect will be very obvious in the experimental part, as is discussed in Chapter 5.

4.2 Case 2: Grid voltage harmonic transient

In this test, the 5th harmonic in the background grid voltage is controlled with a step change from 0% to 0.6%. The performance of the line current (i_s) , PWM waveform (i_w) , as well as the DC current (I_{dc}) using the proposed VI-SHC under



Figure 4.5 Grid voltage harmonic transient



Figure 4.6 DC current transient

this transient are shown in Figure 4.5. The line current waveform would reach the steady state in about 2-3 fundamental cycles. This is due to two factors: i) the one fundamental delay of the SDFT harmonic detection algorithm; and ii) the proposed VI-SHC scheme is actually a closed-loop compensation process.

It also can be found that the DC current is not affected during this transient, which indicates that the power flow control part is completely decoupled from the harmonic compensation part in the proposed VI-SHC scheme.

4.3 Case 3: DC current transient

To test the CSR system DC current transient performance with the proposed VI-SHC scheme, the DC current reference is set to step changed from 10A to 20A in this case. There is still a 0.6% 5th harmonic pre-existing in the background voltage. The simulated transient waveforms are given in Figure 4.6.

It can be observed that the proposed VI-SHC scheme does not affect the DC current transient performance, the DC current shows a very smooth and quick transition from 10A to 20A, which again illustrates that the power flow control part and the harmonic compensation part of the VI-SHC scheme are decoupled. This is due to the last constraint for the SHC free angles optimization, as is given in (2.19).



4.4 Case 4: VI-SHC scheme with different virtual impedance

4.4.1 k is a positive real number (virtual inductor)

Figure 4.7 shows the spectra of the steady-state line current when k is set to 0 (traditional SHE), 0.5, 0.85 and 1 respectively. It can be found from the comparison of Figure 4.7 (a), (b), (c) and (d) that the 5th harmonic drops as k increases. The low order inter-harmonics do not have much difference when k is lower than 0.85. However, once k reaches 1, although the 5th harmonic is further lowered, the magnitude of inter-harmonics especially the ones around f = 280Hz become relatively high as is shown in Figure 4.7 (d). This indicates the low order inter-harmonics, which are mainly caused by the interaction of DC current ripples and PWM pattern, would be drastically augmented with the rise of k magnitude. This may even cause system stability problems. These simulation results are consistent with the analysis in Chapter 3 (see Figure 3.8).



Figure 4.8 Spectra of line current when k is an imaginary number

4.4.2 k is an imaginary number (virtual resistor)

Figure 4.8 shows the spectra of the steady-state line current when k is set to 0, - 0.5*j*, -1.1*j* and -1.27*j* respectively. It can be observed from the comparison of Figure 4.8 (a), (b), and (c) that the 5th harmonic drops as the magnitude of the imaginary part of k increases. The low order inter-harmonics do not have much difference as the magnitude increases under the critical point (k=-1.1*j*). However, once k reaches -1.27*j*, although the 5th harmonic is further lowered, the magnitude of inter-harmonics especially the ones around *f*=270Hz become relatively high. This is shown in Figure 4.8 (d). These amplified inter-harmonics will cause the system to be unstable (when B is set too high). The results are also consistent with the analysis in Chapter 3 (see Figure 3.10).

4.4.3 k is a complex number (virtual R-L impedance)

Figure 4.9 illustrates the simulation spectra of the steady-state line current when k is set to 0, 0.83-0.55j and 0.9-0.6j. It is obvious that once the magnitude of the real part and imaginary part of k is set too high, the inter-harmonics especially


Figure 4.9 Spectra of line current when k is a complex number

the ones at around f=276Hz would be greatly amplified, as is shown in Figure 4.9 (c). This phenomenon coincides with the bode plot analysis given in Figure 3.12. Additionally, it can be observed from the comparison between Figure 4.8 (c) and Figure 4.9 (b) that the performance of setting k to -1.1j is pretty much the same as setting k to the optimal complex value of 0.83-0.55j. This is due to the damping effects provided by the virtual resistor as discussed in Chapter 3.

4.5 Summary

In this chapter, the simulation results of the proposed VI-SHC scheme are given with the following scenarios to verify the foregoing analyses:

• The steady-state performance of the VI-SHC is compared with the traditional SHE and the SHC schemes. In this case both SHC and VI-SHC schemes are effective of mitigating the line current harmonic induced by the background grid voltage distortion. However, when a system parameter (line inductance) variation is introduced in the simulation, the advantage of the proposed VI-SHC compared to the SHC scheme is clearly shown.

- The good performance of the VI-SHC method under a grid voltage harmonic transient (the 5th harmonic component is programmed with a step change from 0% to 0.6%) is illustrated.
- With a DC current reference step change from 10A to 20A, the good system transient performance using the VI-SHC is also verified.
- The VI-SHC scheme with different types of virtual impedance is tested in the simulation as well. The results are consistent with the theoretical analysis in Chapter 3, where it shows using a virtual resistor is a good choice due to the better damping effects and easiness of parameter tuning.

Chapter 5

Experimental Verifications

To experimentally verify the proposed VI-SHC PWM scheme, plenty of realtime experiments have been carried out on a on a 10kVA/208V CSR prototype. The parameters of the hardware CSR system prototype are exactly the same as the simulation model and are shown in Table 4.1. In this chapter, after the introduction of the CSR prototype and control system, the experimental tests under five different cases are provided:

- Case 1: Steady-state performance of the proposed VI-SHC PWM, which is also compared with the traditional SHE and SHC PWM schemes.
- Case 2: PWM scheme transition from the traditional SHE PWM to the proposed VI-SHC PWM.
- Case 3: Transient performance of the VI-SHC with grid voltage harmonic variations.
- Case 4: Transient performance of the VI-SHC with DC current variations.
- Case 5: The VI-SHC scheme with different virtual impedance.

Compared to the simulation testing in Chapter 4, Case 2 here is new. This case is used to emulate the situation that the SHE is originally adopted, while an increase of grid voltage harmonic necessitates the use of the proposed VI-SHC PWM to improve the line current harmonic performance.



Figure 5.1 CSR prototype system setup

5.1 Setup of the CSR prototype and the control system

The CSR prototype system used in the real-time experiments is illustrated in Figure 5.1. The CSR main power converter bridge is composed of six IGCTs produced by ABB, with a rated voltage of 6000V and a rated current of 800A. These high power IGCTs are donated from Rockwell Automation Canada. The IGCTs are installed into a switch cage suitable for press pack mounting, where a heat sink is placed between every two switches. Note that one switch cage with six IGCTs are supposed to be used for a single phase leg in a high power CSR system, where three IGCTs are actually connected in series to provide higher voltage ratings. However, in the low voltage and low power testing at the University of Alberta, two isolation boards are inserted among the six press-packed IGCTs so that a single cage can be used as a three-phase CSR system. Six independent linear power supplies are applied to provide 20V voltage required by the IGCT devices.



Figure 5.2 dSPACE-CPLD control system [51]

The CSR control platform is designed based on a dSPACE (DS1103) system and a CPLD (Complex Programmable Logic Device). Details of this control platform are shown in Figure 5.2. The DS1103 PPC controller board of the dSPACE system is a single-board system with real-time processor and comprehensive I/O. It is designed to meet the requirements of modern rapid control prototyping and is highly suitable for applications such as automotive controllers and induction motor control. In the control system developed for the experiments, the DS1103 PPC controller generates the control signals according to the designed Simulink model in Matlab. To handle the control algorithms of the closed-loop current regulation in a CSR and the fine step size requirement for accurate PWM signal generation, multiple rate control is adopted in the dSPACE system, where the main CSR control, including PLL (phase locking loop), delay angle control, harmonic current/voltage detection, software over current/voltage protection etc., are running at 2.4kHz, while the PWM generation block is running at 120kHz to ensure fine step size for accurate PWM gating signals [51].

The CPLD (XILINX XCR3064XL) soldered on a CPLD interface board is used to convert the electrical signals from the DS1103 to the optic signals for driving IGCTs. Moreover, the CPLD interface board provides hardware protections to the CSR system, including gating logic protection and relay control [51].

The measurements of the CSR system include the three-phase CSR line currents, the three-phase CSR PWM currents, the three-phase source voltages and the DC link current. A sensor board installed with LA 25-P voltage sensors and LA 55-P current sensors are used for this prototype. These signals are measured and sent back to the dSPACE control system for DC current control and the VI-SHC PWM scheme implementation.

In order to simulate the grid voltage with pre-existing background voltage harmonics, a three-phase programmable voltage source (Lx4500) from California Instruments is used as the grid with controllable background harmonics.

5.2 Experimental results of the proposed VI-SHC scheme

5.2.1 Case 1: Steady-state performance of the proposed VI-SHC scheme

In this case, the background grid voltage is programmed with a $0.6\% 5^{\text{th}}$ harmonic. The coefficient *k* is set as the critical imaginary value (-1.1*j*), which is equivalent to a virtual resistor as discussed in Chapter 3.

The steady-state line currents and CSR PWM currents are obtained using the traditional SHE PWM and the proposed VI-SHC scheme, respectively. The results are shown in Figure 5.3. From the comparison between Figure 5.3 (a) and (b), significant improvement can be noticed in the line current waveform when







Figure 5.4 Spectra of the steady-state current harmonics

the proposed VI-SHC scheme is implemented. This improvement is further proven by the spectra comparison illustrated in Figure 5.4 (a) and (b), where the 5^{th} harmonic in the line current is reduced from 9% to less than 2% when the proposed VI-SHC PWM is used. It can be seen from the comparison of Figure 5.4 (c) and (d) that the 5^{th} PWM current harmonic is generated by the VI-SHC



using the SHC scheme

scheme in order to compensate the 5th background voltage harmonic. Note there is 3rd harmonic (3%) existing in the line current, this is due to the minor asymmetry of the CSR system components (mainly the line inductors) used in the experiments.

The SHC scheme is based on the grid voltage harmonic measurement and system model transfer functions. The selected harmonic (e.g. 5th harmonic) can be well minimized under the assumption that the background voltage harmonic component is relatively high for precise measurement (higher than 1% of fundamental) and the system model parameters are obtained accurately. However, when the voltage harmonic component is lower than 1%, the performance of the proposed SHC scheme is less satisfactory, due to the harmonic measurement error and the fact that the CSR system parameters may not be obtained super accurately in the experiments. The line current and PWM current waveforms and the line current harmonics spectrum obtained using the SHC PWM with a 0.6% 5th harmonic in the grid voltage are shown in Figure 5.5 and Figure 5.6. It can be seen that the compensation of the 5th harmonic is not effective in this case (compared to the proposed VI-SHC scheme). Therefore, the SHC scheme presented in [33] is not as practical as the VI-SHC scheme, especially when the magnitude of the background voltage harmonic component is not very high and the system parameters are not known exactly.



Figure 5.7 Transient from SHE to VI-SHC. i_s : 5A/div., i_w , I_{dc} : 10A/div., time: 10ms/div.



 $i_s: 5A/div., i_w, I_{dc}: 10A/div., time: 20ms/div.$

5.2.2 Case 2: PWM scheme transition (from SHE to VI-SHC)

This experiment is to study the transient when the PWM scheme is switched from the SHE to the proposed VI-SHC. This can emulate the situation that the SHE PWM is initially used for the system, while an increase of grid harmonics requires the use of the proposed VI-SHC scheme. As is shown in Figure 5.7, the transition is very smooth and the closed-loop control of the DC current is not affected.

5.2.3 Case 3: Grid voltage harmonic transient

In this case, the 5th harmonic in the grid voltage is programmed with a step change from 0% to 0.6%. The performance of the line current, PWM waveforms, as well as the DC current using the proposed VI-SHC under this transient are shown in Figure 5.8. It can be observed that with the proposed VI-SHC scheme, the line current waveform would reach the steady state in about 2-3 fundamental cycles. As explained earlier in Chapter 4, this is due to the one fundamental delay of the SDFT harmonic detection block and the closed-loop compensation nature of the VI-SHC scheme. Moreover, it can be seen that the DC current is not affected during this transient, which indicates that the power flow control is completely decoupled from the harmonic compensation part in the proposed VI-SHC scheme.



Figure 5.9 DC current transient performance. i_s : 10A/div., i_w : 20A/div., I_{dc} : 5A/div., time: 100ms/div.

5.2.4 Case 4: DC current transient

For this experiment, the DC current reference is set with a step change from 10A to 15A to test the DC current control response of the CSR system when using the proposed VI-SHC scheme. In this test, the background grid voltage is injected with 0.6% 5th harmonic. The experimental transient waveforms are shown in Figure 5.9. It can be seen that the proposed VI-SHC scheme does not affect the



Figure 5.10 Steady-state line current and PWM current waveforms when k is a real number. $i_s: 5A/div., i_w: 10A/div., time: 10ms/div.$

DC current transient performance, which again illustrates that the power flow control part and the harmonic compensation part of the VI-SHC scheme are decoupled.

5.2.5 Case 5: VI-SHC scheme with different virtual impedance

As is discussed in Chapter 3, k can be selected as a real number, an imaginary number or a complex number. Different definition of k has different physical meanings for the virtual impedance. Different values of k will also affect the performance of the VI-SHC compensation scheme. Similar to the simulations in Chapter 4, several real-time experiments are carried out to verify the theoretical analyses made in Section 3.3. Again, the background grid voltage is injected with 0.6% 5th harmonic in this case.

A. Experimental results of a virtual inductor

Figure 5.10 shows the steady-state line current and CSR PWM current



Figure 5.11 Spectra of the line current harmonics when k is a positive real number

waveforms when k is set to 0, 0.5, 0.85 and 1.05 respectively. The respective line current harmonics spectra are illustrated in Figure 5.11. It can be found from the comparison of Figure 5.11 (a), (b) and (c) that the 5th harmonic drops as k increases. The low order inter-harmonics do not have much difference as long as k is lower than the critical point (k=0.85). However, once k reaches 1.05, the magnitude of inter-harmonics, especially the ones at around f=220Hz and f=280Hz, become relatively high as is shown in Figure 5.11 (d). These results are consistent with the analysis and simulation results shown in Section 3.3.2 and Section 4.4.1 respectively.

B. Experimental results of a virtual resistor

The steady-state line current waveforms as well as CSR PWM current waveforms, while k is set to different negative imaginary numbers, are also obtained in the experiments and shown in Figure 5.12. Their respective line current harmonics spectra are illustrated in Figure 5.13. It can be observed from the comparison of Figure 5.13 (a), (b) and (c) that the 5th harmonic drops as the magnitude of the imaginary part of k increases. The low order inter-harmonics do



Figure 5.12 Steady-state line current and PWM current waveforms when k is an imaginary number. $i_s: 5A/div., i_w: 10A/div., time: 10ms/div.$



Figure 5.13 Spectra of the line current harmonics when k is an imaginary number

not have much change when the magnitude is lower than the critical point (k=-1.1j). However, once k reaches -1.3j, as is shown in Figure 5.13 (d), the magnitude of inter-harmonics, especially the ones at around f=200Hz, f=260Hz and f=320Hz, become relatively high. However, due to the damping effects of the applied virtual resistor, the inter-harmonics are much lower than the ones shown in Figure 5.11 (d). These results are consistent with those of the analysis and simulations results given in Section 3.3.3 and Section 4.4.2 respectively.

C. Experimental results of a virtual R-L impedance

Figure 5.14 illustrates the current waveforms when k is set to 0, 0.4-1j and 0.5-1.1j. While the relevant line current harmonics spectra are obtained and shown in Figure 5.15. Note that considering the relatively high parasitic resistors existing in the line inductors, the optimal complex value of k is obtained as 0.4-1j in the experiments using the same method described in Section 3.3.6.



Figure 5.14 Steady-state line current and PWM current waveforms when k is a complex number i_s : 5A/div., i_w : 10A/div., time: 10ms/div.

It can be observed from the FFT analyses of the line current, as shown in Figure 5.15 that once the magnitude of k is set too high, the inter-harmonics especially the ones at around f=210Hz and f=270Hz would be worsened. These results are consistent with the analysis and simulation results obtained in Section 3.3.4 and Section 4.4.3 respectively.

Additionally, from the comparison of Figure 5.11 (c), Figure 5.13 (c) and Figure 5.15 (b), it can be concluded that the harmonic performance of setting k as an optimal complex number excels that of setting k to the critical real number. However, it does not have obvious improvement compared with setting k to the critical imaginary number. Therefore, considering the convenience of k value adjustment as well as the damping effects from a virtual resistor, setting k as an imaginary number (a virtual resistor) is recommended.

5.3 Summary

In this chapter, experiments are carried out on a 10kVA/208V CSR prototype with a control platform using the dSPACE (DS1103) system and CPLD. The real-



Figure 5.15 Spectra of the line current harmonics when k is a complex number

time experimental results of five testing cases are presented to verify the effectiveness of the proposed VI-SHC PWM scheme in both transient and steady-state situations.

From the comparisons and observations of the experimental results, it shows that the proposed VI-SHC scheme can greatly mitigate the CSR line current harmonic caused by the background voltage distortion with only line current measurement. The proposed PWM scheme also has excellent transient performance in the cases of PWM scheme transition, grid voltage harmonic variations, and the DC link current changes. Moreover, the real-time experimental results of Case 5 (different types of virtual impedance) are consistent with the theoretical analyses as well as the simulation results given in Section 3.3 and Section 4.4. Similarly, considering the damping effects and the easiness of k value tuning, the virtual resistor is recommended in this work.

Chapter 6

Conclusion and Future Work

This thesis presents a new PWM scheme to improve the line current harmonic performance in a high power CSR system, especially when the grid background harmonics exist. This is important as the input LC filter of a CSR system may amplify certain low order harmonics from the grid, and therefore the traditional SHE PWM scheme, which is aimed at the PWM current harmonics elimination, does not provide satisfactory performance in this situation. In consideration of the high power CSR applications, the PWM scheme described uses very low switching frequencies (f_{sw} =420Hz).

As the traditional SHE PWM and selective harmonic compensation (SHC) PWM as proposed recently [33] have the ability to shape the PWM current harmonics, a thorough review of these two methods are conducted first in the thesis. The techniques for the switching angle calculations for both SHE and SHC are investigated, and the optimization technique using the THD² as the cost function and with weighting factors imposed on each harmonic is selected due to its flexibility of harmonic pattern shaping for both SHE and SHC PWM. To further facilitate the PWM switching angle calculations, a user-friendly software tool based on the Matlab Global Optimization Toolbox is described.

For the recently proposed SHC PWM, the grid background harmonic compensation is based on the measurement of grid voltage harmonics and the use of CSR system model transfer functions. This model based approach is quite sensitive to the system parameter variations and measurement inaccuracies. Moreover, the harmonics in the grid voltage are usually not high enough at

medium voltage level for precise measurement. To overcome the disadvantages of the SHC PWM in implementation, a virtual impedance based selective harmonic compensation (VI-SHC) PWM scheme is proposed. The detailed information about analyses, designs and implementation for the proposed VI-SHC scheme is presented in the thesis. Both simulations and experiments on a CSR system are carried out to verify the performance of the proposed VI-SHC PWM scheme.

The main contributions made in the research work are summarized as follows.

6.1 Contributions

The contributions made in the thesis mainly involve two aspects: i) the development of a software tool that can be used to calculate the switching angles of the SHE and SHC PWM conveniently, and ii) the development of a VI-SHC PWM that can overcome the implementation disadvantages of the recently proposed SHC PWM.

For the first aspect, a switching angle calculation tool has been developed by using Matlab 2010a/GUI (graphical user interface) with an efficient global optimization algorithm integrated. The user-friendly software tool as developed can be used to flexibly calculate the SHE switching angles for PWM pattern of up to 71 pulses per half cycle. The maximum pulse number can be increased easily to an even higher value, so that the tool can also be used for the CSI for low speed (low fundamental frequency) operation in a drive system. Moreover, with minor modifications of the program, quarter-wave asymmetrical PWM waveform can be produced for SHC PWM as well. The optimization program as developed has the ability to automatically calculate the SHC switching angles with the PWM harmonic reference in a pre-defined range, so as to obtain the SHC look-up table for real-time application of the SHC PWM.

For the second aspect, a VI-SHC scheme is proposed to deal with the implementation defects related to the SHC scheme. More specifically, the proposed VI-SHC scheme has two main advantages over the SHC scheme:

• It compensates the system background current harmonics by using the line current measurement instead of the source voltage. Therefore the VI-SHC

PWM is more practical in the real applications, since the voltage distortion at medium voltage level is usually very subtle for accurate measurement.

 As the PWM output in a CSR system is directly related to the line current, the VI-SHC method is essentially a closed-loop compensation scheme by feeding back the line current harmonics. Therefore, it does not require the detailed and precise system parameters for the derivation of the system transfer functions. As a result, the VI-SHC is more robust to system model parameter uncertainties.

The detailed virtual impedance design procedure is also developed. Different types of virtual impedance (virtual inductor, virtual resistor and virtual R-L impedance) are analyzed on the basis of the developed CSR system model. A presentation is given to the optimal design of the virtual impedance to achieve the best line current harmonic attenuation. It is found that the harmonic performance of a virtual R-L impedance is the best in theory. However, in consideration of the damping effects and easiness of parameter tuning, the virtual resistor is recommended in this work.

The proposed VI-SHC scheme has been implemented on a Matlab/Simulink CSR simulation model as well as a 10kVA/208V hardware CSR prototype in the real-time experiments. The detailed simulation and experimental results show that the proposed VI-SHC PWM scheme proves efficacious in mitigating the CSR line current harmonics induced by the background voltage harmonic distortion while overcoming the disadvantages associated with the SHC scheme.

6.2 Future work

It is suggested in the thesis that future research be conducted into the multiple background harmonics compensation. It has been mentioned in Chapters 2 and 3 that both SHC and VI-SHC PWM schemes can easily compensate one harmonic (e.g. 5th or 7th harmonic) by using a two-dimensional look-up table. If more harmonics are to be considered, the look-up table will become multi-dimensional and may consume considerable memory. However, it can be observed from Figure 2.10 that, instead of changing abruptly, the PWM switching angles have

relatively smooth trends with the variation of the magnitude and phase angle of the PWM harmonic reference in a considerable region. As a result, interpolation techniques can be adopted to reduce the size of the look-up table.

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Appendix A:

Global Optimization Algorithms for SHE and SHC Switching Angles Calculations

A.1 Review of typical global optimization algorithms

In this section, several global optimization methods are investigated and some of their advantages and defects are listed respectively.

A.1.1 Multistart (MS) Methods

MS has plenty of sample points and each sample point is used as a starting point for the local minimization procedure. The best local minimum point found is a candidate for the global minimum x_G^* . Each sample point is usually randomly generated from a uniform distribution over the set of bound constraints S_b .

- Advantages:
- i) This type of methods is reliable, a particular local minimum may be reached several times starting from different points.
- Defects:
- i) The method is not efficient since many sample points will lead to the same local minimum.

A.1.2 Clustering Methods

Clustering methods remove the inefficiency of the MS methods by trying to use the local search procedure only once for each local minimum point. In clustering methods, random sample points are linked into groups to form clusters. Each cluster is considered to represent one region of attraction for a local minimum point. Each local minimum point has a region of attraction such that a



Figure A.1 Clusters of points with the same local minima [36], where the star * indicate local minima

search initiated from any point in the region converges to the same local minimum point, as is displayed in Figure A.1. During the procedure, a cluster is started with a local minimum point as a seed and then expanded in stages by increasing its critical radius. All points within the new radius are added to the cluster, the best un-clustered point is used in a local search procedure to find a local minimum point. If the local minimum found is new, then it is taken as the seed for a new cluster; otherwise that minimum point is the seed for an already existing cluster that needs to be expanded. This is continued until all the sample points are clustered.

- Advantages:
- This method removes the inefficiency of the MS method by reducing the probability that many local searches converge to the same local minimum point.
- Defects:
- i) Their performance depends heavily on the dimension of the problem, i.e. the number of design variables.

A.1.3 Acceptance-Rejection (A-R) Methods

The acceptance-rejection (A-R) methods are modifications of the MS algorithm to improve its efficiency by using ideas from statistical mechanics. Instead of using local minimization started from each randomly generated point, in A-R methods, the local minimization is started from a point only if it has the probability given by:

$$P(x) = \exp\left(\frac{\left[f(x) - \overline{f}\right]_{+}}{-F}\right)$$
(A.1)

where \overline{f} is an estimate of the upper bound of the global minimum, F is a target value for the global minimum, and $[h]_{+} = \max(0, h)$. The initial value of F is usually provided by the user, or it may be estimated using a few random points. \overline{f} is adjusted at each iteration as the best approximation to the global minimum value.

- Advantages:
- This type of methods improves the efficiency compared with the MS methods by avoiding doing lots of local searches which actually converge to the same local minima.
- Defects:
- i) The approximation of \overline{f} and F is not clear.

A.1.4 Domain Elimination (DE) Methods

The basic idea of this algorithm is to explore the entire feasible domain for the problem in a systematic way for the global minimum. During the procedure, each local search is attempted from a point that is likely to lead to a new local minimum point. The general stages are described as is shown in Figure A.2. The algorithm starts with the selection of a random point from a uniform distribution over the constraint set S_b (Block 2). Test is applied to determine whether this new point is accepted based on some criteria (Block 3); if the point is accepted, then a search for a local minimum \mathbf{x}^* (vector) is initiated from there (Block 5); if it is rejected, then it is added to the set of rejected points (Block 4) and a new random point would be generated. If the point is accepted and a minimum \mathbf{x}^* is obtained, this \mathbf{x}^* is checked to see whether it is a new local minimum (Block 6). If it is, \mathbf{x}^* would then be added to the set of local minima. If it is not, the algorithm would check the stop criteria to see whether should continue a new iteration or stop. Note in order to accept or reject a random point, records for the following three types of points are kept: previous starting points for local minimization, local



Figure A.2 Flow chart of Domain Elimination method

minimum points, and rejected points. A random point is rejected if it is within a critical distance to one of the foregoing sets. Additionally, if the point is accepted, a search is initiated for a new local minimum point. The local search process would also be monitored, and if the search is going toward a known local minimum point, it is terminated.

- Advantages:
- According to the statistics in [36], the global iteration number is relatively small compared with other major global algorithms, since when the process approaches the end, most of the sample points would converge to the same minimum. Therefore, this method is efficient.
- ii) From the statistics in [36], the chance that this method finds the real global minima is very high, 9 in 10 cases.
- Defects:
- i) The adjustment of the stopping criteria and the interval tolerance is critical in this type of methods.

 ii) Since the rejection criteria heavily depend on checking the distance between the new point and the records of foregoing points sets, the checking procedure would take a long time when dealing with problems with lots of design variables.

A.1.5 Stochastic Zooming (ZOOM) Methods

This type of methods uses a target value for the global minimum of the cost function. Once the target is achieved, it is reduced further to "zoom-in" on the global minimum. The method combines a local minimization method with successive truncation of the feasible set S (initial points) to eliminate regions of local minima to zoom-in on the global solution. It initiates the search for a local minimum from any point. Once a local minimum point has been found, the problem is redefined in such a way that the current solution is eliminated from any further search by adding the following constraint to the problem:

$$f(\mathbf{x}) < \gamma \cdot f(\mathbf{x}^*) \tag{A.2}$$

where $f(\mathbf{x})$ is the cost function value at the current minimum point and $0 < \gamma < 1$ if $f(\mathbf{x}^*) > 0$; and $\gamma > 1$ if $f(\mathbf{x}^*) < 0$. The re-defined problem is solved again and the process continues until no more minimum points can be found.

The major difference between ZOOM and DE is the addition of the zooming constraint (2.18). They share similar advantages and defects. Additionally, the reliability of this kind of methods largely depends on whether sufficient initial points are searched.

A.2 Global optimization tool box in Matlab [40]

From version 2010a, Matlab starts to include global optimization tool box which can be utilized to efficiently tackle global optimization problems. This tool box includes Global Search (GS), Multistart (MS), Pattern Search (PS), Genetic Algorithm (GA), and Simulated Annealing (SA) solvers. These solvers can be used to solve optimization problems where the objective or constraint function is continuous, discontinuous, stochastic, does not possess derivatives, or includes simulations or black-box functions with undefined values for some parameter settings. Here the basic description of the above mentioned solvers is given as follows except MS (which has already been described before).

A.2.1 Global Search (GS)

Similar to MS, GS also starts a local minima search from multiple trial start points which are generated using scatter search (The detailed introduction of scatter search can be found in [41]). The distinct part of this method compared with MS is that it utilizes the basin of attraction to avoid doing lots of repeated iterations which converge to the same local minima. Generally, initial values $\mathbf{x}(\mathbf{0})$ (vector) that are close to each other give steepest descent paths that tend to the same minimum point. The basin of attraction for steepest descent is the set of initial values leading to the same local minimum, as can be seen in Figure A.3. In GS, it is assumed that the basins of attraction are spherical, and are centered at local minima points. The initial radius of each sphere is the distance from the initial point to its solution point (local minimum point). These estimated basins can overlap. During the procedure, the trial start points whose distance to either center of basin is within the radius of that basin are regarded as inside of a basin of attraction, and therefore stop continuing the local search. The trial points which are outside of each basin would be calculated (to find a local minimum point), if the local search from one trial point converges to an existing center of basin, the radius of that basin would be increased to the distance between that trial point and the center of that basin; if the search finds a new local minimum, a new basin would be built. This procedure continues until all the generated trial points are included into the basins of attractions. From the description of the algorithm, it can be found GS is actually very close to Clustering methods introduced above.



Figure A.3 Basins of attraction

- Advantages:
- This method has fast convergence to local minima for smooth problem. The building of basins of attraction could avoid lots of iterations which actually have the same minima.
- Defects:
- i) The setting of the parameters and criteria is vital to the optimization results.

A.2.2 Pattern Search (PS) methods

PS methods belong to direct search methods which do not require any information about the gradient of the objective function. The Matlab Global Optimization Toolbox functions include three pattern search algorithms called the generalized pattern search (GPS) algorithm, the generating set search (GSS) algorithm, and the mesh adaptive search (MADS) algorithm.

PS algorithms compute a sequence of points that approach an optimal point. At each step, the algorithm searches a set of points, called a mesh, around the current point: the point computed at the previous step of the algorithm. The mesh is formed by adding the current point to a scalar multiple of a set of vectors called a pattern. If the pattern search algorithm finds a point in the mesh that improves the objective function at the current point, the new point becomes the current point at the next step of the algorithm. This procedure continues until the optimal point is found or certain stop criteria is met.

- Advantages:
- i) This type of algorithm can be used to solve problems where the objective function is not differentiable, or is not even continuous.
- Defects:
- The convergence procedure would take longer time compared with GS and MS, especially when the scalar multiple is very small and with large number of design variables.

A.2.3 Genetic Algorithm (GA)

The genetic algorithm is a method for solving both constrained and unconstrained optimization problems that is based on natural selection. To better understand the principles of this algorithm, several terms are explained as follows:

- i) Fitness function: the function you want to optimize, similar as objective function.
- ii) Individuals: an individual is any point to which the fitness function can be applied.
- iii) Population: a population is an array of individuals.
- iv) Generation: at each iteration the GA performs a series of computations on the current population to produce a new population. Each successive population is called a new generation.
- v) Parents and children: to create the next generation, the genetic algorithm selects certain individuals in the current population, called parents, and uses them to create individuals in the next generation, called children. Typically, the algorithm is more likely to select parents that have better fitness function values.

The genetic algorithm repeatedly modifies a population of individual solutions. At each step, the genetic algorithm selects individuals at random from the current population to be parents and uses them to produce the children for the next generation. Over successive generations, the population "evolves" toward an optimal solution. GA uses three main types of rules at each step to create the next generation from the current population:

- i) Selection rules select the individuals, called parents, which contribute to the population at the next generation.
- ii) Crossover rules combine two parents to form children for the next generation.
- iii) Mutation rules apply random changes to individual parents to form children.
- Advantages:
- i) This type of method can be applied to solve a variety of optimization problems that are not well suited for standard optimization algorithms,

including problems in which the objective function is discontinuous, nondifferentiable, stochastic, or highly nonlinear.

- Defects:
- This method is highly stochastic. When with lots of variables, the possible forms of the stochastic mutations and crossover would be substantial. Therefore, the computation may take longer time compared with GS and MS.
- ii) The setting of the parameters and criteria is critical.

A.2.4 Simulated Annealing (SA)

Simulated Annealing models the physical process of heating a material and then slowly lowering the temperature to decrease defects. At each iteration of the SA algorithm, a new point is randomly generated. The distance of the new point from the current point, or the extent of the search, is based on a probability distribution with a scale proportional to the temperature. The algorithm accepts all new points that lower the objective function value, but also, with a certain probability, points that raise the objective function value. By accepting points that raise the objective, the algorithm avoids being trapped in local minima, and is able to explore globally for more possible solutions. The temperature decreases as the algorithm proceeds. As the temperature decreases, the algorithm reduces the region of its search to converge to a minimum. The temperature is a parameter in SA that affects two aspects of the algorithm: the distance of a trial point from the current point and the probability of accepting a trial point with higher objective function value.

- Advantages
- i) This type of algorithms can be used to solve discrete problems.
- ii) It is proven that this method can converge to global minima for bounded problems with very slow cooling schedule.
- Defects:
- i) This type of algorithm cannot solve problems with non-linear constraints.
- ii) The cooling schedule may take very long time for searching a global convergence.
- iii) The setting of each parameter is not easy and clear.

A.3 Conclusion

Some of the major global optimization algorithms and the ones integrated in the Matlab tool box have been introduced above. Their advantages and defects are also given. Here, one or more methods need to be selected for the SHE and SHC angles optimization.

The PWM patterns need to be designed could have large number of pulses per half cycle so as to minimize harmonics up to a very high harmonic order (when the fundamental frequency is very low). This means there would be a large number of different combinations of the free angles. Therefore, GA and PS are not very suitable, since it may take them a long time to finish scanning the feasible initial points. And according to [37] and [40], non-gradient-based methods are less efficient than gradient-based ones. From the aspect of the constraints, in this case, the constraints are none linear, thus the SA would be excluded. Additionally, since the adjustment of parameters in A-R is not clear, this type of methods is not considered either. Thus, the remaining suitable algorithms are MS, Clustering methods, DE, ZOOM and GS.

According to the statistics in [36], DE has got a very satisfactory performance compared with other major algorithms. ZOOM is very similar as DE, but since the setting of γ is not clear in this case, ZOOM is excluded. Clustering methods and the solver GS are actually the same, thus the selected methods are MS, DE and GS.

It is mentioned above that both DE and GS improves the efficiency of MS. However, in Matlab 2010a, the MS can run in parallel, which may reduce its searching time. With regards to the performance of DE in this case, it is found the setting of the critical distance which is used for determining the distance of a new point from the foregoing point sets is not easy and may need change depending on the number of the free angles of the PWM pattern. According to the simulation results of GS, it is found it gets similar optimization results as DE, and it is very fast (According to [40], GS is the fastest compared with the other 4 solvers). Additionally, in Matlab 2010a, the searching process of the global optimization solver can be well observed, which is very useful for results checking. GS is thereby selected as the global optimization algorithm for the SHE and SHC free angles calculation. However, the parameters and criteria in GS are vital in finding the true global optimal points, and thus need to be well defined.

Appendix B:

Global Optimization Parameters Setting of the Developed Switching Angles Calculation Tool

As has been introduced in Section 2.3, the developed SHE angles computation tool can obtain globally optimum results using Global Search algorithm (GlobalSearch solver). And as has been stated in Appendix A, the parameters and criteria related to this solver are vital in finding the true global optimal points, and thus need to be well defined. The control panel illustrated in Figure 2.8 contains editable panes for global options required by the global search algorithm in Matlab 2010a. The following part gives a brief introduction to each parameter; the default values for each option for most cases are presented as well.

"Number of Trial Points"

Number of potential start points to examine from the problem structure. Global Search runs only those potential start points that pass several tests, i.e., this item controls the number of uniformly distributed sample points which are considered as the start points of the iteration algorithm. A greater number of trial points will get better chance in finding the global optima.

Default: 1000 (Must be a positive integer)

• "Maximum Wait Cycles"

This item controls the searching speed and the extent of searching. The smaller the value, the more slowly it searches, but in return it searches more thoroughly.

Default: 5 (Must be a positive integer)

• "Basin Radius Factor"

A basin radius decreases after Maximum Wait Cycles consecutive start points are within the basin. The basin radius decreases by a factor of (1-Basin Radius Factor). This item also controls the searching speed and the carefulness of searching.

Default: 0.2 (Must be a value between 0 and 1)

• "Distance Threshold Factor"

A multiplier for determining whether a trial point is in an existing basin of attraction. This factor controls the region of search. The smaller it is, the more carefully it searches.

Defaults: 0.5 (Must be a value between 0 and 1)

• "Penalty Threshold Factor"

This item determines increase in penalty threshold. It impacts the threshold value of start points testing criteria.

Default: 0.2 (Must be positive)

• "TolX" and "TolFun"

These two properties describe how close two solution points must be for solvers to consider them identical. Solvers consider two solutions identical if they are within TolX distance of each other and have objective function values within TolFun of each other.

Default:

- i) TolX: 0.1*pi/180 (Must be 0 or positive)
- ii) TolFun: 0.01. (Must be 0 or positive)
- "Maximum Wait Time"

This item determines the maximum calculation time permitted, with the unit of second.

Default: 2000 (s)

• "Display"

This popup menu has three options which can be used for results display:

- i) "iter": summary results to command line after each local solver run.
- ii) "final": summary results to command line after last solver run.
- iii) "off": no output to Matlab command line.

Default: 'iter'

The aforementioned items are the parameters which impact the effect of Global Search solver utilized for global optimization. The detailed description of this solver has been given in [40]. According to the experiments, most of the predefined parameters (default values) are of no necessity to change, their respective default values have already been adjusted and are good enough for most cases except "Number of Trial Points", "Maximum Wait Time" and "Display" which need to be changed regarding different preferences. Increasing the number of trial points would get higher possibility in finding the global optima. However, as a tradeoff, it will take longer time for the switching angles calculation.