Investigation of Potential Platforms for Low Frequency MEMS-based Piezoelectric Energy Harvesting

by

Mehdi Rezaeisaray

A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Department of Mechanical Engineering
University of Alberta

Abstract

MEMS based energy harvesters have recently been investigated for scavenging, otherwise useless, ambient vibration energy. Piezoelectric materials are fabricated on micro-devices to convert the mechanical vibration energy into electrical energy. The main focus for these harvesters is low frequency (under 500 Hz) ambient vibration which is the source of a fundamental challenge with MEMS oscillators. The smaller the oscillator is, the higher its natural frequencies will become. Various techniques have been proposed to decrease the natural frequency of micro-energy harvesters such as increasing the length of the devices or assembling extra proof mass to the fabricated devices which could potentially affect the mass production of the MEMS devices. Another challenge is that most of the reported piezoelectric energy harvesters in the literature have cantilever designs. These structures have a high mechanical quality factor providing a sharp peak at their resonant frequency. Since microfabricating resonators with a resonant frequency exactly matching their designed value is very challenging, linear cantilever designs seem to be less practical for real applications where excitation frequency could change. Therefore, some techniques in vibration have been adapted to widen the frequency bandwidth of the harvesters. One of the most effective methods to broaden the frequency bandwidth is taking advantage of large deflection effect of oscillators. However, some of the proposed designs such as a fixed-fixed beam design have high resonant frequencies (≥1 kHz), whereas the focus for energy harvesters is low frequency range.

In this work, a silicon based structure has been designed and fabricated to carry an electronic chip and potentially provide in-situ supplementary power for it. This design provides capability of harvesting at three different frequencies because the resonant frequencies of this structure at its first three mode shapes are within the low ambient vibration frequency range. The widening frequency bandwidth has been investigated for this design. Natural frequencies as low as 71.8, 84.5, and 188.4 Hz have been measured using a laser vibrometer. A frequency bandwidth of ~10 Hz has been obtained for the 2^{nd} mode shape of the structure under the base excitation of 0.2g. A maximum open circuit voltage of ~1V and maximum power output of 136nW have been obtained using this harvester.

In addition, as opposed to the conventional silicon-based harvesters, polymeric materials have been investigated as the main structural material for energy harvesters. Due to the much lower stiffness of polymers compared to silicon, the resonant frequency of the harvesters could be reduced. To prove the concept, a SU-8 (E_{SU-8}=5GPa vs. E_{Si}=160GPa) membrane has been designed and fabricated with Aluminum Nitride harvesting elements. The membrane configuration provides the capability to widen the harvester's frequency bandwidth. Testing results reveal a linear resonant frequency of 381 Hz, frequency bandwidth of 146Hz, maximum output power of 1.37μW, and power density of 3.81 $\mu W/cm^2$ at the base excitation of 4g with this design. The much lower resonant frequency of polymeric structures compared to the similar silicon-based structures (more than 5 times lower) makes them a strong candidate for the future harvesters.

The objective of this thesis is to develop a platform using silicon-based and polymer-based energy harvesters to improve the performance of the energy harvesters by reducing the resonant frequencies and widening the frequency bandwidth. Throughout this research, all stages including design, fabrication, packaging, testing, and characterization of both silicon- and polymer-based harvesters have been developed or adapted for the purpose of this work. Finite element simulations have been conducted to examine the mechanical response of the structures as well as their electrical output at the design stage. A scalable microfabrication process flow has been developed in this work to fabricate piezoelectric layers on SU-8 micro-structures. An improved approach for cleaving fabricated devices from the silicon substrate has been developed to overcome challenges of the dicing process. Various 3-D micro-assembly techniques have been adapted to package the fabricated harvesters. In addition, 3-D printed parts were used to enhance the yield of the packaging and testing stages. This technique could potentially be used for bio-compatible packaging, as well. In conclusion, the polymer-based and wideband energy harvesters seem promising for real applications at low ambient vibration frequencies. This research introduces opportunities to further improve the performance of the harvesters by decreasing their resonant frequencies.

Preface

Some sections of this thesis have been published or submitted to refereed journals under supervision of Dr. Don Raboud and Dr. Walied Moussa. I also consulted Dr. Dan Sameoto to conduct the research work and in most of the publications. In the following, the publications and my responsibilities for each one are elaborated.

Both Chapter 3 and Chapter 6 include various sections of two articles we have submitted as 1.Mehdi Rezaeisaray, Mohamed El Gowini, Dan Sameoto, Don Raboud, Walied Moussa, "Wide-Bandwidth Piezoelectric Energy Harvester with Polymeric Structure", accepted, *Journal of Micromechanics and Microengineering* and 2.Mehdi Rezaeisaray, Mohamed El Gowini, Dan Sameoto, Don Raboud, Walied Moussa, "Low Frequency Piezoelectric Energy Harvesting at Multi Vibration Mode Shapes", in review, *Sensors and Actuators: A*. Mohammad El Gowini provided me with his recipe for depositing AlN thin films. Other than that, I was responsible for designing the energy harvesters, analyses, developing a full fabrication process flow with 7 masks, and writing the whole paper.

The first part of Chapter 5 has been published as Mehdi Rezaei, Jonathan Lueke, Dan Sameoto, Don Raboud and Walied Moussa, "A New Approach to Cleave MEMS Devices from Silicon Substrates", *Journal of Mechanics Engineering and Automation*, 3 (2013) 731–738. I proposed the main idea of this publication based on a cleaving method that Jonathan Lueke adapted from a recipe developed by Norcada Inc. in UofA NanoFab and also a paper previously published by Dr. Sameoto on patterning photoresists. I was responsible for process development, fabrication, data collection, and writing the full paper.

The second part of Chapter 6 has some sections of our publication as Rezaeisaray M, Lueke J, El Gowini M, Yue S, Raboud D, Moussa W, "Overcoming Some of the Challenges in 3D Micro-Assembly Techniques to Package MEMS Devices", *Austin Journal of Nanomedicine and*

Nanotechnology, Vol.2, Issue 6, 2014. I was responsible for writing the whole paper. The other co-authors (Lueke J, El Gowini M, and Yue S) had contribution in terms of providing images of their research work related to the publication objectives. Only the parts I had developed for that paper are included in this thesis.

We have published another paper as Mehdi Rezaei, Jonathan Lueke, Don Raboud, Walied Moussa, "Challenges in Fabrication and Testing Piezoelectric MEMS with Particular Focus on Energy Harvesters", *Microsystem Technologies*, (2013) 19: 1195–1219. This paper was used in Chapter 2 and Appendices to cite similar researches in the energy harvesting field. For this publication, Jonathan Lueke collaborated in editing the article, providing some images and introducing some references which were cited in this article.

The adapted and developed PZT microfabrication process was used in an article as Jonathan Lueke, Mehdi Rezaei, Walied A. Moussa, "Investigation of Folded Spring Structures for Vibration-based Piezoelectric Energy Harvesting", Accepted, *Journal of Micromechanics and Microengineering*. My contribution to this publication was developing and providing the recipe for J. Lueke on both deposition and patterning stages of the PZT thin film.

Acknowledgement

Thanks God who displays the Sun after dark nights, grows the blooms after dead cold winters, and plants hope in hopeless hearts. Thanks to God who helps to forget, to forgive, and to move on.

I would like to appreciate the knowledge, the patience and the support of my supervisor Dr. Don Raboud. He has been a good listener and very motivated to help at all levels. Also, I would like to express my gratitude to my co-supervisor Dr. Walied Moussa for providing resources, equipment, and research requirements. He has been always with the research group understanding the problems and trying to assist. In addition, my deeply thanks are due to Dr. Dan Sameoto, my supervisory committee member, for his new ideas, for his quick responses, and for his technical advices.

This research work could not be done without the financial supports. Great thanks to National Science and Engineering Research Council (NSERC), Alberta Innovates Technology Futures (AITF), and CMC Microsystems.

I would like to appreciate all my colleagues who provided a friendly space to study. Thanks to my former colleagues Hossam Gharib, Jonathan Lueke, Ryan Saunders, and David Benfield who at some stages guided me through equipment in the lab. Thanks to Mohamed El Gowini, my great friend and colleague, who were always there to listen and provide friendly advices in very stressful situations during my PhD program.

I also thank the Faculty of Engineering professors who dedicated their valuable knowledge in the courses I took or audited in University of Alberta: Dr. Ben Nadler, Dr. Bob Koch, Dr. Steve Dew, Dr. Saeed Behzadipour, Dr. Don Raboud, Dr. Walied Moussa, and Dr. Dan Sameoto.

I would like to appreciate knowledgeable former NanoFab director Dr. Ken Westra for listening to my ideas and patiently explaining the issues I might face. I also thank current NanoFab director Dr. Eric Flaim who helped me to understand the fabrication challenges and pave a road to approach and finally

solve them. I have been grateful for the support that all NanoFab staffs, including Keith Franklin, Stephanie Bozic, Scott Munro, and Les Schowalter, provided for my research work through the long course of fabrication stage. In addition, I always felt the supportive attitude from machine shop staff especially Dave Waege, Bernie Faulkner, Rick Conrad, and Tuula Hilvo. Last but not least, I appreciate all IT Technicians especially David Dubyk and administrative team especially Gail Dowler, Richard Groulx, Teresa Gray, and Donna Waring at the Department of Mechanical Engineering who have been very friendly and always helpful.

Eventually, my endless thanks to my dearest father and mother who always make me speechless describing their warm support to build my enthusiasm for success. Great appreciation to my beloved wife, Nahid, whose understanding and support during these years was the key to pass through difficult situations. No words would be able to express my heartfelt gratitude to her. Thanks for late nights and early mornings. Thanks for being my strength and hope when I needed the most. In one sentence, you just made me owe you.

Table of Contents

List of Tables

List of Figures

List of Symbols, Abbreviations, and Nomenclature

A	Amplitude of the base excitation acceleration
AC	Alternative current
AlN	Aluminum Nitride
Ar	Argon
BOE	Buffered Oxide Etch
C	Equivalent of a similar linear system
C_{eq}	All damping forces of the system
$C_{11}, C_{12}, C_{13}, C_{33}, C_{44}$	Nonlinear Elastic Constants
CMUT	Capacitive micro-machined ultrasonic transducer
C_p	Capacitance of the piezoelectric elements
Cr	Chromium
C_s	Structural damping
Cu	Copper
d_{31}	Representing the 3-1 mode of piezoelectricity where induced stain and generated voltage are at two different axes with 90˚ angle.
d_{33}	Representing the 3-3 mode of piezoelectricity where induced stain and generated voltage are at the same axis.
DC	Direct current
DCA	direct chip attach
DI	deionized
DRIE	Deep Reactive Ion Etching
e_{31}, e_{33}, e_{15}	Piezoelectric Constants
FEM	Finite element method
FFT	Fast Fourier transform
FPCB	Flexible PCB
HCl	Hydrochloric Acid
HF	Hydrofluoric Acid
ICPRIE	Inductively Coupled Plasma Reactive Ion Etching
IPA	Isopropyl Alcohol

k_l	Linear stiffness
k_n	Cubic stiffness
L_b	Beam length
LDV	Laser Doppler Vibrometer
l_e	Length of the electrodes
LIGA	Stands for German words Lithographie Galvanoformung Abformtechnik
L_m	Mass length
M	Proof mass
MEMS	Micro Electro Mechanical Systems
PAG	Photoacid generator
PCB	Printed circuit board
PDMS	Polydimethylsiloxane
PGMEA	Propylene Glycol Monomethyl Ether Acetate
P_{max}	Maximum power
PMMA	Polymethylmethacrylate (Acrilic)
PR	Photoresist
Pt	Platinum
PZT	Lead zirconate titanate ($Pb(Zr_x,Ti_{1-x})O_3$)
Q	Quality factor
Q_i	Electrical quality factor
RF	Radio Frequency
RIE	Reactive Ion Etch
R_{opt}	Optimum load resistance
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
SOI	silicon on insulator
SSHI	Synchronized switch harvesting on inductor
T_b	Beam thickness
Ti	Titanium
T_m	Mass thickness
t_p	thickness of the piezoelectric layer

TSV	Through silicon via
U_M	Mass deflection
$V_{o.c.}$	Open circuit voltage
V_{pk}	Peak Voltage
$V_{pk\text{-}pk}$	Peak to peak amplitude of AC voltage output
V_{rms}	RMS voltage
W_b	Beam width
W_e	Width of the electrodes
W_m	Mass width, length, thickness
XeF_2	Xenon Difluoride
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
ZnO	Zinc Oxide
δ	Displacement of the proof mass
ε_r	relative permittivity
ε_0	Vacuum permittivity
$\varepsilon_{11}, \varepsilon_{33}$	Piezoelectric Dielectric Constants
$\varepsilon_{bending}$	Bending Strain
$\varepsilon_{stretching}$	Stretching Strain
ε_{total}	Total Strain
ζ	damping ratio
ρ	Density
ω	Base excitation frequency
ω_n	natural frequency ($\omega_n = 2\pi f_n$)

Chapter 1 - Introduction

Energy harvesting is defined as scavenging ambient, otherwise useless, energy from a device's surroundings and converting it to electrical energy. One step up could be converting any sort of energy into another as long as the produced form of energy is useful for an application. One step down in detail is converting ambient vibrational energy into electrical power. The idea is taking advantage of useless energy out of human activities or vibrations of the environment such as vehicles and structures and converting it to electrical power to be saved for later use. Three main vibration driven energy harvesting methods are: Piezoelectric, Electromagnetic, and Electrostatic techniques. The piezoelectric energy harvesting provides the highest energy density over the other methods [1]. Therefore in this research, the improvements in the piezoelectric energy harvesting are investigated.

1.1 Motivation

There are many vibration sources around us that are potential sources of useful energy through their vibration. Using energy harvesters, these otherwise useless energies could be scavenged and saved for other usage. Devices which require electrical power sources in bio-medical, automotive, aerospace, and industry applications are potential hosts for energy harvesters. In addition, energy harvesters could potentially be used for wristwatches, bicycle lights, and portable consumer electronics (such as laptops, mobile phones, calculators, toys, etc.). The need of energy generation for wireless sensor networks and the idea of running devices without batteries are the main motivations for fast growing energy harvesting technology all around the world. Using energy harvesting has benefits including long operation time, elimination of chemical disposal, saving

in costs, eliminating or lengthening charging period, etc. EE Times[1] in 2007 reported that, "The importance of energy harvesting has motivated the German federal government to include the topic in its €500 million (about $685 million) research support program". Also, the Energy Harvesting Journal on Jan.14th, 2009 has reported a forecast which represents the global market for energy harvesting devices used for small electronic and electrical equipment[2]. Based on this report the numbers of energy harvesting devices which are/will be sold globally are ~500M in 2009, ~2,000M in 2014 and 10,000M in 2019. To meet the requirements of the market, the performance of energy harvesters should be improved over their current levels. There are also a number of reports which predict the growing performance of the energy harvesters in future[3].

One of the main potential applications for micro energy harvesters is providing electrical energy for bio-medical implantable devices. Since energy harvesters could produce electrical energy out of vibration of human walking and activities, energy harvesters instead of rechargeable batteries could be integrated with implantable devices to be placed inside the human body without worrying about recharging or replacing their batteries. Obviously, these energy harvesters' size needs to be very small for those applications. However, the existing energy harvesters in the market are not small enough and their fabrication technique is not scalable.

Interestingly, micro energy harvesters are capable of extending the operation life-time of rechargeable batteries [2]. This effect can be used for lengthening the usable time of portable electronics such as cell phone, MP3 Player, iPhone, etc. In the fast growing consumer electronics market, an energy harvester which is capable of extending the life-time of any rechargeable batteries is potentially commercially important.

[1] Source: http://www.eetimes.com/electronics-news/4189761/Race-is-on-to-develop-energy-harvest-ICs
[2] Source: http://www.energyharvestingjournal.com/articles/paybacks-from-energy-harvesting-00001201.asp
[3] Source: IDTechEx, "Energy Harvesting and Storage 2009-2019," Cambridge 2009.

1.2 Proposed Approach

The idea of using energy harvesting for wireless sensor networks and consumer electronics requires developing devices in very tiny sizes. Micro Electro Mechanical Systems (MEMS) technology provides the capability of manufacturing sub-millimeter devices. Microfabrication techniques have been used to produce the energy harvesters in MEMS scale. One of the main challenges of using micro-energy harvesters is their high natural frequencies due to their small sizes. Assuming a cantilever as an oscillator, the shorter the length of the device, the higher its natural frequency would be. Considering the fact that most of the reported micro-energy harvesters have silicon based cantilever structure, new structural configurations need to be developed and tested to decrease the natural frequency of the energy harvesters within the same size ranges. The other challenge is that most conventional energy harvesters are linear resonators which usually provide a single sharp peak (with a high quality factor) at their resonant frequency. Figure 1.1 shows the electrical power output of a fabricated cantilever based energy harvester in the frequency domain. The resonant frequency is 343.6 Hz and the frequency bandwidth is ~1 Hz. It is clear that any excitation vibration happening at the frequencies shown by dash lines 1 and 2 could not be harvested efficiently by that cantilever design. Therefore, the resonant frequency of the harvester must be designed to be very close to the excitation vibration frequency to obtain the most efficient performance out of the harvester. However, fabricating resonators with a resonant frequency exactly matching its designed value seems unrealistic. This issue causes the linear oscillators to become less practical for real applications.

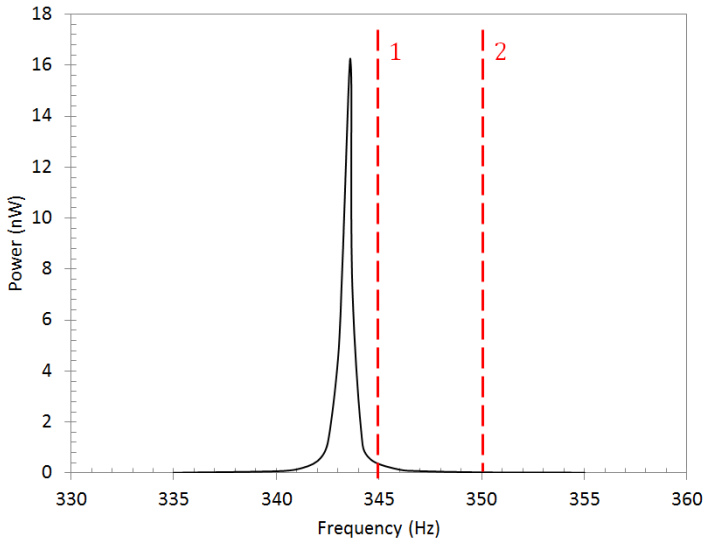


Figure 1.1 – Linear oscillators provide a sharp peak. Any excitations slightly different from their resonant frequency could not be harvested.

In this research, a different configuration of silicon-based micro-energy harvesters is designed aiming to decrease the natural frequency of the MEMS device. This structure is design such that it can carry an electronic chip and potentially provide supplementary power for it. As shown in Figure 1.2, the beams of this design are placed next to proof mass instead of extending away from the proof mass, similar to regular fixed-fixed beams. Therefore, the beams could be chosen longer, which results in lower natural frequency, while the device is almost the same size. Moreover, this configuration allow taking advantage of more than one vibration mode shape for energy harvesting which is elaborated in Chapter 3. In addition, the capability of using a polymeric structure for energy harvesters is investigated in this research aiming to reduce the natural frequency of the target energy harvester. A polymeric structure would have a lower natural frequency in comparison to a similar silicon-based structure due to much smaller stiffness of the polymer than silicon. A schematic of the polymeric energy harvester is demonstrated in Figure 1.3. In this research, a SU-8 membrane is designed, fabricated, and characterized to investigate the capability of using polymers as main structural material for the energy harvesters. This approach is elaborated in detail in Chapter 3.

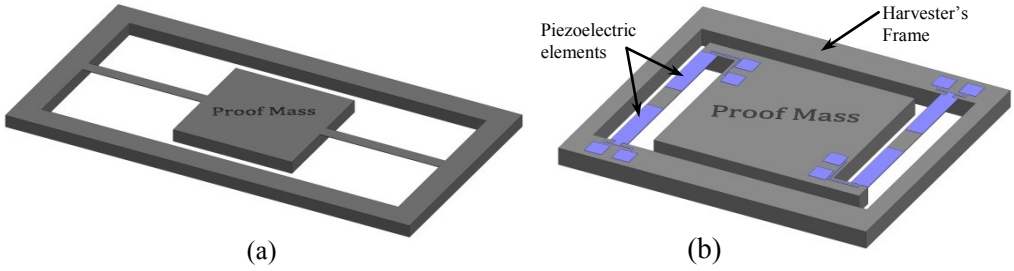


Figure 1.2 – (a) Schematic of a regular fixed-fixed beam, (b) The proposed silicon-based energy harvester.

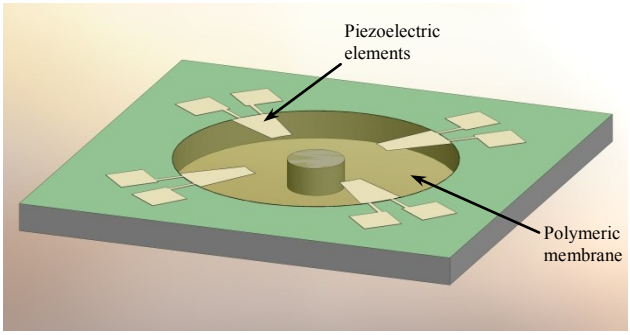


Figure 1.3 – Schematic of the polymer-based energy harvester.

1.3 Research Objectives

The thesis objectives in summary include investigating new configurations of silicon-based designs aiming to decrease the natural frequency of the harvesters and also investigating the capability of using softer structural materials for piezoelectric micro-energy harvesters. All the steps from design to fabrication and characterization of the silicon-based and polymeric micro-energy harvesters need to be carried out to obtain a device. The research objectives are explained in the following:

- Investigate different structural designs for silicon-based energy harvesters to reduce the natural frequency for devices in MEMS scales.
- Integrate SU-8 thin films as a structural material for micro-energy harvesters. Silicon-based devices have conventionally been used for energy harvesting. However for a given design, a SU-8 structure could

have a lower natural frequency due to its softer stiffness than a silicon structure.

- Develop a scalable microfabrication process to build energy harvesters with polymeric structures. The piezoelectric energy harvesters' fabrication process includes several high temperature process and various stages of soaking the substrate into acetone, HF acid and other solutions. These processes can damage or delaminate SU-8 thin films. So, the fabrication process must be designed such that the SU-8 thin film is fabricated along with other harsh fabrication steps.
- Investigate the capability of widening the harvestable frequency bandwidth. Due to the fact that the frequency of the ambient vibrations is not a fixed exact number, a linear oscillator which provides a sharp peak with a narrow bandwidth at its resonant frequency could not probably be used very efficiently for real applications. Therefore, a harvester with broader frequency bandwidth would be more practical for real applications.

In addition, some secondary objectives are necessary to be addressed to be able to achieve above objectives. The secondary objectives of this research are listed in the following:

- Finite element analysis to estimate the mechanical and electrical behavior of the energy harvesters. The characterization of the fabrication limitations and including them in the simulation settings provides more reasonable results comparing to experimental measurements. The simulation helps to estimate the behavior of the new designs before fabricating them.
- Develop a technique to separate the fabricated devices from the silicon substrates. The traditional method is using a dicing machine. However, this machine can damage the fragile and overhanging devices. A different method must be used to safely separate an individual device without dramatically increasing the fabrication cost.

- Develop improved packaging techniques or adapt previously reported techniques to mechanically and electrically package the fabricated energy harvesters. Packaging is known as one of the most challenging stages of the prototyping MEMS devices. Therefore, a reliable and repeatable packaging technique is required to package various devices.
- Test and characterize the packaged energy harvesters. The vibration driven energy harvesters need two main testing schemes. Mechanical tests to determine the response of the device in the frequency spectrum. Also, a set of electrical tests must be conducted to measure the electrical output of the energy harvesters.

1.4 Thesis Overview

This thesis provides a detailed description of the design, microfabrication, and testing of a number of piezoelectric energy harvesters. The thesis is divided in seven chapters which are described briefly in the following.

Chapter 1 contains the introduction to the presented research and underlines the motivations behind this research and explains the methodology pursued in throughout this work.

The background of vibration driven energy harvesting and related researches to the objectives of this work are reviewed in Chapter 2. Various devices which have previously been designed for piezoelectric energy harvesting are provided in this chapter. Also, a number of techniques reported in the literature to broaden the frequency bandwidth of the energy harvesters are summarized in this chapter. In addition, the previously reported devices in which SU-8 is used as structural material are represented.

In Chapter 3, the designed configurations are introduced and also analyzed in terms of mechanical and electrical responses. Finite Element Analyses, which is used for modal and coupled field studies, are also presented in this chapter.

The developed microfabrication process for the energy harvesters is provided in Chapter 4. All fabrication steps are described in details and the characterization of various processes are also explained.

Chapter 5 discusses the packaging stage of making the energy harvesters. The challenges and steps taken to overcome those challenges are elaborated. The new approach for cleaving silicon substrate and mechanical and electrical packaging techniques exploited for this research are given in this chapter.

Chapter 6 illustrates both mechanical and electrical testing and characterization methods. The testing apparatus and the procedures are demonstrated in detail. In addition, the experimental results obtained out of testing various configurations of the energy harvesters are provided in this chapter.

Chapter 7 presents the main contributions of this research and also some recommendations to continue this research and to advance in this field.

An alternative piezoelectric thin film was also considered for this research and a number of processes were developed that are provided in the Appendix A.

Finally, the mask layouts and some of the ANSYS codes of this work are provided in the Appendices.

Chapter 2 - Literature Review

2.1 Overview

In this chapter, an overview of vibration driven micro-energy harvesting and in particular piezoelectric energy harvesters is introduced. The reported energy harvesters are reviewed. Optimization of the electrical output of the harvesters is examined. The main practical challenges of using conventional linear energy harvesters and the reported solutions to overcome the issue are presented. The recent literature is reviewed on using the nonlinear vibrating structures as one of the effective techniques to widen the frequency bandwidth of the energy harvesting. In addition, the reported works in using SU-8 as the main structural material in MEMS are investigated. Finally, the focus of this thesis which is provided in details in the following chapters is presented.

2.2 Vibration Driven Piezoelectric Energy Harvesters

Energy harvesting is defined as scavenging ambient, otherwise useless, energy from a device's surroundings and convert it to electrical energy. The "First Draft of Standard on Vibration Energy Harvesting", which was provided at the 2nd annual energy harvesting workshop held on January 30–31, 2007 at FortWorth, TX [3], indicates the energy sources in the surrounding which are/can be trapped for generating electricity (Table 2.1). No matter at what frequency or acceleration, any vibrating object around us is losing some energy. The energy of these vibrations could be converted into electrical power and saved in a capacitor or a rechargeable battery to be used later. In addition, the generated electrical energy could be exploited as a supplementary power source for wireless devices such as RFIDs, cellphones, MP3 players, etc.

Table 2.1–Energy sources for generating electricity [3].

Human body	Vehicles	Structures	Industrial	Environment
Breathing, Blood pressure, exhalation, body heat.	Aircraft, UAV, helicopter, automobiles, trains.	Bridges, roads, tunnels, farm house structures.	Motors, compressors, chillers, pumps, fans.	Wind
Walking, arm motion, finger motion, jogging, swimming, eating, talking.	Tires, tracks, peddles, brakes, shock absorbers, turbines.	Control-switch, HVAC systems, ducts, cleaners, etc.	Conveyors, cutting and dicing, vibrating mach.	Ocean currents, acoustic waves.

Roundy et al [4] have provided a list of some ambient vibration sources (on which energy harvesters could be used) along with their acceleration magnitudes and their frequencies when they are at their peak (Table 2.2). In the case of each particular environmental energy source, knowing this information is critical to design an energy harvester to match those conditions so that the harvester has the best performance.

Table 2.2 –Acceleration and frequency of a number of ambient vibration sources [4].

Vibration Source	$a\ (m/s^2)$	$f_{peak}(Hz)$
Car engine compartment	12	200
Base of 3-axis machine tool	10	70
Blender casing	6.4	121
Clothes dryer	3.5	121
Person nervously tapping their heel	3	1
Car instrument panel	3	13
Door frame just after door closes	3	125
Small microwave oven	2.5	121
HVAC vents in office building	0.2–1.5	60
Windows next to a busy road	0.7	100
CD on notebook computer	0.6	75
Second story floor of busy office	0.2	100

Vibration-driven piezoelectric energy harvesting has broadly been examined in literature such that in a short period (2004–2008), several review papers were

published. In 2004, Sodano et al [5] published a review article to highlight the previous literature on piezoelectric harvesting. Also, Roundy et al [1] presented an article to discuss the modeling, design, and optimization of piezoelectric generators. They also provided a set of design intuitions such as the removed electrical energy looks like damping to the mechanical system. In 2006, Beeby et al. [6] provided a review of previous works on piezoelectric, electrostatic, and electromagnetic harvesting for micro-scale applications. In 2007, Priya [7] published an article overviewing piezoelectric vibration harvesters, and Anton et al [8] presented a review of piezoelectric energy harvesting from 2003-2006 as an update to the previous work by Sodano et al [5]. In 2008, Cook-Chennault et al. [9] reviewed various energy harvesting sources for MEMS applications such as solar harvesting, thermal harvesting, and all three kinds of vibration harvesting devices. In addition in 2011, Kim et al [10] reviewed the performances of vibration devices, piezoelectric materials, and mathematical modelings of the harvesters. In 2013, Rezaei et al [11] overviewed the challenges of fabrication, packaging, and testing of piezoelectric energy harvesters.

Roundy et al [4] presented a comparison of vibration-driven energy harvesters based on their available examples (Table 2.3). Piezoelectric energy harvesters provide the highest electrical output without requiring a voltage source.

Table 2.3 –Comparing three different vibration-driven energy harvesting [4].

Mechanism	Advantages	Disadvantages
Piezoelectric	No voltage source needed Output voltage is 3–8 V	More difficult to integrate in microsystems
Electrostatic	Easier to integrate in microsystems	Separate voltage source needed Practical difficulties
Electromagnetic	No voltage source needed	Output voltage is 0.1–0.2 V

2.2.1 Piezoelectricity

The piezoelectric effect was discovered by Jacques and Pierre Curie in 1880 [12]. "The piezoelectric effect is understood as the linear electromechanical interaction between the mechanical and the electrical state in crystalline materials with no inversion symmetry" [2]. In simple words, if piezoelectric materials are pushed or pulled, electrical voltage will be generated and conversely by applying voltage to piezoelectric materials, the structure will mechanically be deflected. These effects have been exploited to produce sensors and actuators, respectively.

Several piezoelectric materials exist but the main materials which have been reported in microfabrication of thin films are Lead Zirconate Titanate ($Pb(Zr_x,Ti_{1-x})O_3$ known as PZT), Aluminum Nitride (AlN) and Zinc Oxide (ZnO). Additionally, polymeric piezoelectric materials such as polyvinylidene fluoride (PVDF) have also been investigated because of their unique capabilities in terms of microfabrication. Table 2.4 compares the piezoelectric coefficients of these materials [13-16]. The bigger the piezoelectric coefficient/constant is, the better the electrical output will be. However, there are some limitations in fabrication which sometimes eliminates using a material and it has to be replaced. For instance, depostion of PZT thin films involves various challenges and also it can contaminate the fabrication tools [11].

Table 2.4 – Comparing the properties* of the thin film piezoelectric materials [17].

Piezoelectric Materials	ZnO	AlN	PVDF	PZT
d_{31} (pC/N)	-2.3 – -4.7	-2	-8	-40 – -94
k_{31} (CV/Nm)	0.19	-	0.12	0.22 – 0.31
d_{33} (pC/N)	7.5 – 12.4	3.4 – 5.1	30 – 33	90 – 223
k_{33} (CV/Nm)	0.28 – 0.41	0.21	0.16	0.49 – 0.67

* d represents piezoectric coefficient and k represents the piezoelectric coupling.

2.2.2 Various Designs for Energy Harvesters

Energy harvesters, in general, have been investigated by researchers to provide a power supply for wireless sensors. In the case of MEMS energy harvesters, the size of the harvester limits the output power of the device. However, if an energy harvester could not instantaneously provide enough power for a wireless sensor it can still be useful as a supplementary power source to extend the battery life of that device.

One of the early piezoelectric energy harvesters was developed in 2001 by Glynne-Jones et al where they used thick-film piezoelectric technologies to deposit PZT layers on both sides of a triangular Steel cantilever [18]. Beam length was 23 mm and had a width of 23 mm at root. In 2003, Roundy et al provided a broad review of potential power harvesting technologies [4]. They studied the vibration-based harvesters as a viable power source and showed that the potential power density obtained from the piezoelectric conversion is significantly higher than other vibration-driven energy scavenging. In 2004, Roundy et al presented PZT bimorph on various beam configurations [1]. They prototyped PZT beams which had ~1.75 cm length with Tungsten proof mass. Demir et al. have investigated the behavior of a 1.3μm thick silicon membrane with 1μm PZT film at high deflections and strains for use as generators. They also examined the residual stress, pressure–deflection relationships, and the electrical output of the device [19]. Lu et al provided a model to analyze the piezoelectric power generators in MEMS applications [20]. They showed that there is an optimal external resistance that gives the maximum power output. In 2005, Jeon et al used thin film PZT technology to make d_{33}[4] mode piezoelectric power generators with natural frequency of 13.9 kHz [21]. They showed that a piezoelectric cantilever with d_{33} mode could potentially generate an open circuit voltage of ~20 times higher than a same size d_{31} mode piezoelectric cantilever. They have also presented a technique to control the curling which happens in

[4] d_{33} and d_{31} are two modes of piezoelectric effect elaborated in [20] Lu F, Lee HP, Lim SP. Modeling and analysis of micro piezoelectric power generators for micro-electromechanical-systems applications. Smart Mater Struct. 2004;13:57-63.

released micro-beams due to their residual stress. In 2006, Fang et al installed a Nickel mass on a 2000×600 μm^2 silicon cantilever to lower the natural frequency to 608 Hz [22]. They exploited UV-LIGA SU-8 technique to fabricate Nickel proof masses of 600×500 μm^2 (length×width). In 2007, Marzencki et al developed a CMOS compatible fabrication process to make a silicon cantilever with a built-in silicon proof mass and a thin film of AlN to capture frequencies of the range of 1 kHz [23]. In 2008, Shen et al reported fabricating a $4.56 \times 0.4\, mm^2$ piezoelectric beam with an integrated $1.36 \times 0.94\, mm^2$ silicon proof mass with a resonant frequency of 461.15 Hz [24]. They used 4 masks in their fabrication process and exploited d_{31} mode of PZT thin film to generate power. In 2009, the same group considered utilizing SOI wafers to fabricate a similar design where they could decrease the resonant frequency to 183.8 Hz. Lee et al fabricated both d_{31} and d_{33} modes on the same size cantilevers to compare their electrical outputs [25]. They reported 2.6 $V_{pk\text{-}pk}$ using d_{31} mode versus 4.1 $V_{pk\text{-}pk}$ using d_{33} mode of PZT on a $3 \times 1.5\, mm^2$ silicon cantilever. Elfrink et al. reported generating maximum output power of 60 µW exploiting a silicon cantilever with a large proof mass under base excitation of 572 Hz frequency and 2g acceleration [26]. They showed AlN as a viable piezoelectric thin film for vibration driven energy harvesters. In 2011, Alper Erturk and Daniel Inman wrote a book called “Piezoelectric Energy Harvesting” and reviewed the literature and also collected most of the reported analytical modeling, experimental results, and challenges of the reported cantilever based energy harvesters in one place [27]. Newer techniques have recently been considered for piezoelectric energy harvesters to enhance scavenging the ambient energy including optimizing the performance of the electrical circuitry connected to the harvester, using an array of cantilevers, natural frequency tuning, and wide-band oscillators.

2.2.3 Electrical Ouput Optimization

The output signal is in the form of alternating current (AC). However, most of the electronics targeted to benefit from harvesters require direct current (DC)

power supplies. Therefore, the generated energy from harvesters could not be directly used to power electronics unless appropriate circuitry is added to condition the harvester's output to a usable form. Basic conditioning circuits (also known as standard interface) includes a full bridge rectifier and a capacitor to conduct the AC/DC conversion. Since the immediate energy generated by a piezoelectric harvester is not usually sufficient to power electronics, a capacitor or a rechargeable battery is used to temporarily store the harvested energy to be used later on.

The ouput power of a piezoelectric energy harvester depends on the terminal load resistance and the impedance of the circuitry. The load resistance must match with the internal resistance of the harvester. The internal resistance is a function of the internal capacitance which is elaborated more in detail in Chpater 6. Figure 2.1 shows that there is an optimum resistance for each harvester in which the maximum power is transferred. In addition, at each excitation frequency, there exists an optimum reisistance. Researchers have been seeking optimization methods to enhance the output power of energy harvesters [28-31]. Considering the size of the MEMS energy harvesters, the output energy of these devices would be low. Therefore, maximizing the efficiency seems more important in this case. Various electrical circuitries have been reported in literature to improve the output power of the vibration driven energy harvesters which are illustrated in Chapter 6.

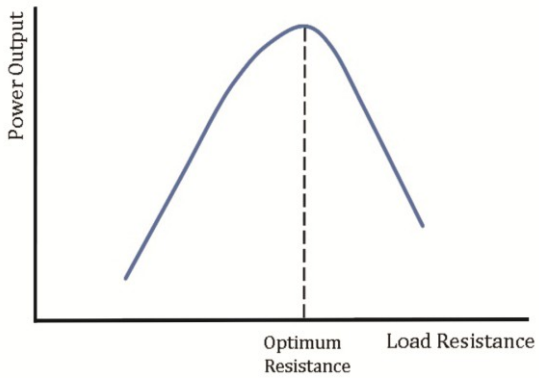


Figure 2.1–Power output of piezoelectric harvesters significantly depends on the load resistance [11].

2.3 Broad Band Energy Harvesters

One of the challenges of using micro-energy harvesters is their low electrical output due to their tiny sizes. Another main challenge for conventional energy harvesters to be used in real life applications is their narrow frequency bandwidth. In the following, various reported approaches are investigated to overcome these challenges.

2.3.1 Arrays of Cantilevers

The very small size of micro-energy harvesters limits their maximum extractable power output. However, their small size allows stacking many of them together aiming to generate sufficient amount of electrical power. S.M. Shahruz [32] has reported a theoretical approach to design a mechanical band-pass filter using an array of cantilevers. In this approach a systematic procedure is proposed to maximize the frequency band of the filter by properly choosing the size of the beams and the proof masses. He has also investigated the limitations of the performance of the filter [33]. Xue et al [34] reported a different theoretical approach to design broadband piezoelectric harvesters by integrating multiple piezoelectric bimorphs. Their numerical results show that the operating frequency bandwidth of the device could be adjusted by connecting patterns of bimorphs in parallel or in series. Ferrari et al [35] presented an array of three cantilevers in macro-scale. The resonant frequencies were 113, 183, and 281 Hz and the voltage output of the cantilevers were rectified and charged in individual capacitors before adding them up. Liu et al [36] were the first group who microfabricated an array of cantilevers. They micro-assembled Nickel proof masses to decrease the natural frequency of their cantilevers. Natural frequencies of the cantilevers were 226, 229, and 234 Hz. The output voltages were rectified individually and then charged in one capacitor. They have reported 3.98 μW effective electrical power and 3.93V DC output voltage. Sari et al [37] used an array of parylene cantilevers with planar gold coils on them. This array takes advantage of electromagnetic effect instead of piezoelectricity. A maximum voltage and a maximum power of 0.67 mV and 56 pW are reported out of one

cantilever. Lien et al [38] have analytically investigated the electrical behavior of an array of piezoelectric cantilevers with various interfacing circuits. They have shown that the electrical performance of an array with SSHI (synchronized switch harvesting on inductor)[5] system has both benefits of power boosting and bandwidth improvement.

2.3.2 Natural Frequency Tuning

The narrow frequency bandwidth of the linear cantilever based energy harvesters potentially limits them from being used in real applications. In fact, the ambient vibration is not controllable and can vary by a few Hertz, whereas, the linear vibrating energy harvesters deliver their best efficiency at their resonant frequencies. Deviating from resonant frequency, the output power of the harvesters would be close to zero. Researchers have examined using passive and active tuning of the resonant frequency for the oscillators to match their resonant frequency with the ambient vibration frequency.

Tuning methods generally fall into two major categories: Intermittent and Continuous. In intermittent tuning, power is consumed periodically to tune the device, whereas, in continuous tuning, the tuning mechanism is continuously powered. In other words, continuous method is an active tuning, while, intermittent method is a passive technique. They also can be classified in two major groups: 1.Mechanical and 2.Electrical Tuning Methods. In general, electrical methods are easier to implement, less efficient and usually suitable for in-situ tuning, while mechanical methods are more efficient and sometimes not suitable for in-situ tuning. A number of review papers have been published studying various reported tuning techniques [39, 40]. A few examples of tuning techniques are illustrated in the following.

2.3.2.1 Passive Tuning

Wu et al [41] proposed a mechanical tuning technique. Figure 2.2 demonstrates their device and the tuning strategy. In this method, a moveable screw is used to

[5] The SSHI interface has recently been used to improve the electrical output of the energy harvesters. This interface has been exploited in Chapter 6 in this work's simulations as well.

change the position of the center of gravity in the proof mass. They have reported changing the natural frequency of the cantilever from 180Hz to 130Hz.

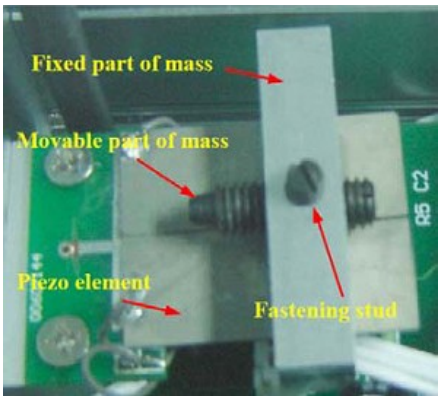
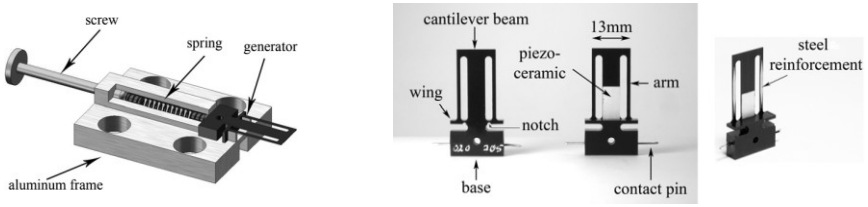


Figure 2.2 – A mechanical passive frequency tuning technique for a cantilever [41].

Leland et al [42] investigated the frequency tuning by straining the vibrating structure. In this method, a simply supported (on both sides) piezoelectric bimorph is axially compressed to lower its resonant frequency. They have reported adjusting the resonant frequency of the loaded beam up to 24% below its unloaded resonant frequency. Remtema et al [43] and Syms [44] took advantage of applying thermal stress to tune the natural frequency of resonators. Eichhorn et al [45] designed a cantilever beam with two thin arms (along the length of the beam) to apply mechanical stress to the tip of the beam. The compressive or tensile pre-stress which is applied to the beam through the arms (by an external screw shown in Figure 2.3(a)) could shift the natural frequency of the beam. They have also improved the tuning performance by adding notches to the spaces between the beam and the arms (Figure 2.3(b)). They have reported for a beam with 20mm length, 5mm width and 0.44mm thickness, they could shift its natural frequency about 22% by applying compressive pre-stress, whereas, tensile pre-stress shift the natural frequency up to 4%.



(a) (b)

Figure 2.3 – Schematic diagram of the test device [45].

2.3.2.2 Active Tuning

Mukherjee [46] proposed an idea of tuning the natural frequency of a cantilever beam by applying axial electrostatic force. The design includes two sets of comb-like structures as shown in Figure 2.4. One set of combs is used for sensing and the other set which is closer to the tip of the cantilever is used for tuning. The frequency tuning is conducted by applying a voltage difference between the fixed electrodes and the free end of the cantilever. Therefore, an axial tensile or compressive load can be applied to the cantilever. A range of -0.6% to 3.3% frequency shifts from untuned frequency was reported for this design.

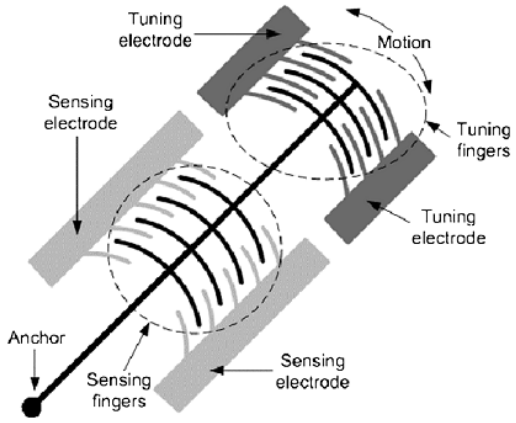


Figure 2.4 – Active frequency tuning by applying axial electrostatic force [40].

Zhu et al [47] designed a closed loop frequency tuning mechanism for an electromagnetic vibration based energy harvester. They use an axial tensile magnetic force to shift the natural frequency of the micro-generator. Figure 2.5 demonstrates a schematic diagram of the mechanism. One magnet is fixed at the free end of a cantilever and one another is connected to a linear actuator which is located axially in line with the cantilever. The opposite poles of the magnets are facing each other and the magnets faces are curved to maintain equal gap while cantilever is vibrating. The tuning is performed by varying the distance between the two magnets using the actuator. Therefore, the axial load on the cantilever and consequently, the resonant frequency can be adjusted.

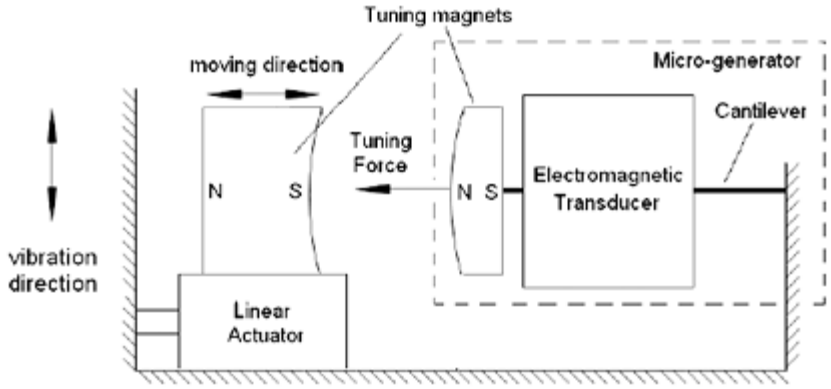


Figure 2.5 – Schematic of an electromagnetic frequency tuning mechanism [47].

Table 2.5 provides a comparison for the reported frequency tuning techniques. It seems that the mechanical tuning procedures are the most efficient methods. However, implementing the mechanical techniques in micro-scales is very difficult. On the other hand, the electrical frequency tuning techniques are easy to be implemented for MEMS devices to actively tune the oscillator in-situ. However, these techniques suffer from low efficiency.

Table 2.5 – Comparing different frequency tuning techniques (Modified from [40]).

Strategies	Advantages	Disadvantages
Mechanical tuning	• High efficiency	• Extra system and energy are required • Responds to only one frequency at a time • Slow response to a change in a vibration frequency
• Change dimension	• Does not affect damping	• Difficult to implement • Not suitable for tuning in-situ
• Change center of gravity	• Does not affect damping	• Not suitable for tuning in-situ
• Change spring stiffness continuously	• Suitable for in-situ tuning	• Consumes energy when generators work at resonance
• Apply axial load (intermittently)	• Easy to implement • Suitable for in-situ tuning • No energy is required when generators work at resonance • Damping is not affected when the tensile load is applied	• Increased damping when the compressive load is applied

Electrical tuning	• Easy to implement • No energy is required when generators work at resonance • Suitable for in-situ tuning	• Low tuning efficiency

Some of the reported frequency tuning techniques (such as [46]) have not been designed for energy harvesters. Their focus does not take the efficiency of the tuning procedure into account. Some others have been designed for bulk sizes (such as [41]) and in most of the cases, their fabrication in MEMS scale is almost impossible. Designing an in-situ tuning procedure to be applicable for MEMS structures still seems very challenging. The main problem in this case is the efficiency of the tuning procedure where the generated power must be higher than the energy used for tuning.

2.3.3 Widen the Frequency Bandwidth

The conventional vibration driven energy harvesters are designed as linear resonators as discussed in Section 2.2.2. The main issue of using these designs is their narrow frequency bandwidth [48, 49]. They operate efficiently only if the base excitation frequency very closely matches their resonant frequency. In addition, fabricating a device to have a natural frequency exactly matching its designed value does not seem to be realistic due to various challenges in fabrication. Therefore, researchers are seeking new approaches to make wideband energy harvesters to overcome this issue [39, 40, 50]. A mechanical stopper was used close to the proof mass of the beam to widen the frequency bandwidth of a piezoelectric cantilever. Liu et al [51] designed a cantilever based energy harvester to widen the harvestable frequency bandwidth exploiting a second cantilever as a stopper to limit the amplitude of the main harvester and change its frequency. An operating bandwidth of 18 Hz is reported using that technique [51]. Widening the frequency bandwidth could also be done by taking advantage of the vibrating devices with nonlinear stiffness. The nonlinear stiffness of the oscillator could result in Duffing effect. As opposed to the oscillators with linear stiffness which represent a sharp peak at frequency

spectrum (Figure 2.6(a)), the oscillators whose spring stiffness is not linear will have a skewed peak as shown in Figure 2.6(b) and (c) representing the Duffing effect. Three common nonlinearities of oscillations which have been lately explored to widen the harvestable bandwidth are: hardening, softening, and bistability. In addition, multi degree of freedom oscillators are designed to broaden the electrical output peak of harvesters. In the following, the reported widening techniques are reviewed.

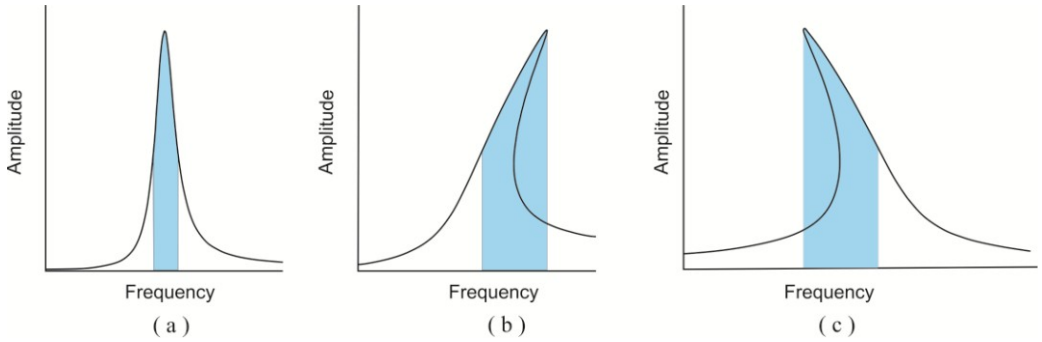


Figure 2.6 –The bandwidth of a (a) linear oscillator's peak is compared to the bandwidth of a resulted peak due to (b) hardening and (c) softening Duffing effect at frequency spectrum.

2.3.3.1 Bistable Oscillators

A category of nonlinear vibrating structures is called bistable oscillators. These oscillators have two stable states and their transition from one stable state to another is nonlinear. Bistable oscillators have been designed based on magnetic interaction and buckled beams in macro- and micro-scales aiming to increase the harvestable bandwidth. In 2009, Erturk et al proposed a piezomagnetoelastic power generator with piezoelectric layers deposited on the beam and two magnets installed close to the tip of the beam at its maximum deflection such that beam had to vibrate between the magnets [52]. In their case, the beam was made of steel with PZT films on both sides and was 145 mm long, 26 mm wide, and 0.26 mm thick. In this case, the resonant frequencies before and after adding magnets are reported 7.4 Hz and 10.6 Hz, respectively. In 2010, Arrieta et al used a bistable composite plate without using magnets [53] and Ferrari et al

presented a piezoelectric beam with a magnetic proof mass and another permanent magnet fixed in a short distance from the cantilever tip [54]. In 2013, Liu et al presented a novel spring-mass configuration (Figure 2.7) which included a proof mass, some hinges, and two piezoelectric components [55]. The structure was 33mm long and was fixed in one side and adjustable on the other side to tune the frequency range of the structure within its bistability effect. Nguyen et al proposed an energy harvester in micro-scale with curved springs which provided an extremely wide bandwidth of 715 Hz from a linear resonant frequency of 1149 Hz [56]. The chip area was $1 \times 1\ cm^2$ including 1725 μm long curved springs which were fixed in one side and adjustable on the other side. The structure used the buckling effect to tune the frequency range of the harvester through bistable effect.

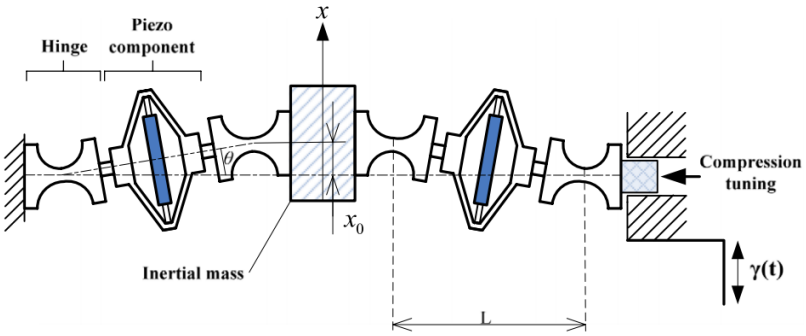


Figure 2.7 – Schematic of a bistable mechanism which uses the buckling effect [55].

2.3.3.2 Softening Stiffness

The softening effect results in skewing the resonant frequency peak toward the lower frequencies at higher amplitudes. On the other hand, the hardening effect results in skewing the resonant frequency peak toward the higher frequencies. In either case, the harvestable frequency bandwidth is broadened comparing to the narrow band linear oscillators.

In 2009, Stanton et al presented a new design which provides both softening and hardening effect [57]. Figure 2.8 shows their proposed design. The design consists of a cantilever with a permanent magnet as proof mass and two other permanent magnets installed on the sides. The length of the cantilever was 26

mm. By adjusting the distance of the magnets to the proof mass (d in Figure 2.8), they could tune the frequency response of the harvester from 12 Hz, in case of no magnets, to 14.4 Hz in case of locating magnets at d=4.7 mm. In 2010, Nguyen et al fabricated a MEMS electrostatic energy harvester with a die size of $9.5 \times 9.5\, mm^2$ which utilizes four nonlinear springs [58]. The springs were arranged to achieve the softening effect of suspension and consequently broadening the frequency bandwidth of the harvester. Some comb shaped electrodes were contrived on the proof mass and the fixed frame. Therefore, the excitation vibration energy was converted to electrical voltage through the electrostatic effect between the fixed and moveable electrodes. In 2013, the same group expanded their work by improving their results. They reported widening the frequency bandwidth up to 50 Hz and generating an average power of 1μW [48].

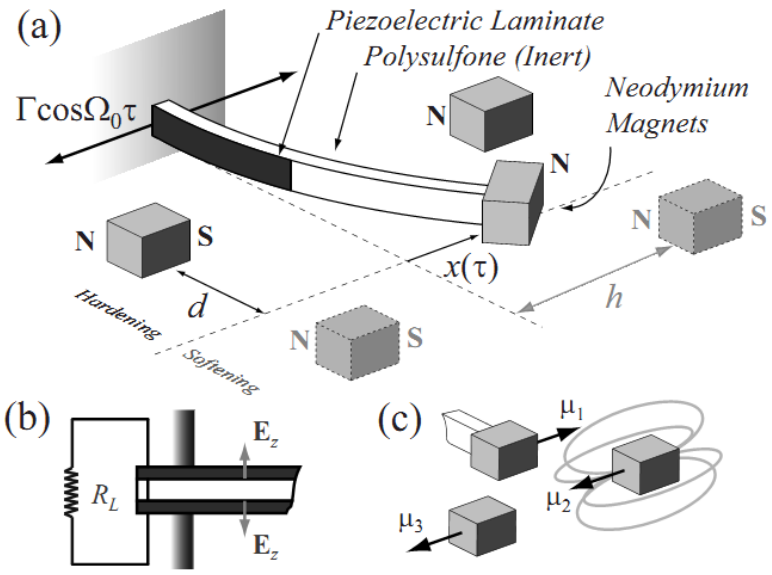


Figure 2.8 – Schematic of a nonlinear energy harvester using both softening and hardening effects [57].

2.3.3.3 Hardening Stiffness

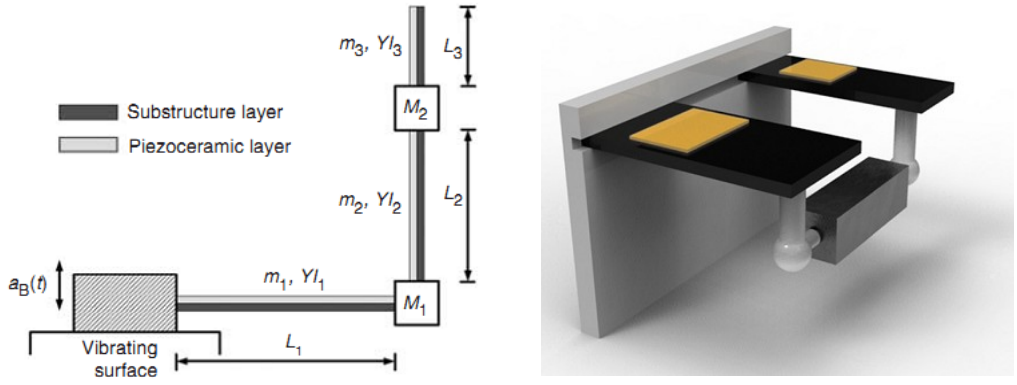
The increasing stiffness effect has been mostly reported by utilizing stoppers with the oscillators. In addition, using permanent magnets and the Duffing effect

have been reported in the literature. In the following, some examples are described.

In 2009, Soliman et al developed wideband electromagnetic micro-generators using the nonlinearity of the oscillators [59]. A mechanical stopper is used within the stroke of the vibration of the cantilever. When the amplitude of the cantilever increases, the adjustable stopper repositions the anchor of the cantilever from the root to the location of the stopper. Therefore, the stiffness of the cantilever increases due to decreasing the length of the beam. A magnet is used as proof mass and a copper coil is affixed with a small gap from the tip of the beam. They could widen the bandwidth by ~10 Hz from ~94 Hz natural frequency without using the stopper. In 2011, Liu et al presented a silicon cantilever with a large proof mass ($5 \times 5 \times 0.4\, mm^3$) and 10 parallel piezoelectric elements on a supporting silicon layer with a size of $3 \times 5 \times 0.4\, mm^3$ [60]. Some of the piezoelectric elements were used as actuators by applying AC voltage which results in vibrating the cantilever and the rest of the elements generate voltage due to the produced vibration. They have limited the vibration amplitude of the cantilever by adjusting the gap between the proof mass and the carrier base. A frequency bandwidth of ~17 Hz is reported around the low resonant frequency of ~36Hz. In addition, Hajati et al proposed utilizing a doubly clamped beam with a proof mass in the middle [49]. This design takes advantage of the stretching strain as a negative feedback which provides a nonlinear stiffness and results in a Duffing effect at resonance. They have fabricated four fixed-fixed beams with a size of $5 \times 4\, mm^2$ next to one another and installed a large mass on them to reduce their natural frequency to around 1kHz. In 2012, Le et al reported prototype of a wideband electrostatic energy harvester with a built-in stoppers [61]. They presented an end-stop model with a linear stiffness which can fit to the nonlinear stiffness model within limited vibration amplitudes.

2.3.3.4 Multi Degree of Freedom Harvesters

Some designs have been proposed in the literature that takes advantage of multiple beams [62] or more than one resonant frequency per device [63] to scavenge the ambient vibration energy. In 2008, Erturk et al presented a L-shaped beam and mass structure as a piezoelectric energy harvester [64]. They designed a 50 mm long structure such that its first two natural frequencies are close to one another and could potentially widen the harvestable bandwidth. As shown in Figure 2.9(a), two beams and two masses were used in their design. The second beam starts from the middle of the first proof mass and is oriented in 90˚ from the first beam. The whole structure vibrates due to the applied vertical vibration at the base. As the first mass moves up, the second mass can independently move to the right or to the left. Therefore, the structure represents two mode shapes with close resonant frequencies. In 2011, Kim et al introduced a two-degree-of-freedom structure (Figure 2.9(b)) which consisted of two beams and a mass utilizing both translational and rotational motions of the proof mass [65]. The structure had a size of $50 \times 40\, mm^2$. In both designs, two peaks appear at the frequency spectrum which results in widening the frequency bandwidth of the harvester. It seems that most of the reported multi-degree-of-freedom harvesters are in macro-scales, whereas, implementing shown configurations in Figure 2.9 is not as feasible to be made with microfabrication techniques.



(a) (b)

Figure 2.9 – Two examples of multi-degree-of-freedom energy harvesters. ((a) and (b) are taken from [64] and [65], respectively)

2.4 Using Polymers as Main Structural Material in MEMS

Polymer micromachining is a relatively new, but fast-growing, field in fabrication of MEMS devices. Although microfabricating polymers involves various challenges, their unique properties such as flexibility, biocompatibility, and transparency provide vast range of fabrication possibilities to meet micro-applications which sometimes are not practically feasible with conventional methods. In addition, comparing the expensive conventional microfabrication processes, polymer microfabrication costs are cheaper [66]. In a review paper, Becker et al [67] have collected polymeric materials which have been used in microfabrication and compared their properties. In that article, the advantages of SU-8 are listed as high mechanical, thermal, and chemical stability which makes it a strong candidate (compared to the other polymeric materials) for the purpose of this research.

2.4.1 SU-8 as structural material in MEMS

SU-8 is an epoxy based photoresist composed of a Bisphenol A Novolak epoxy oligomer and a photoacid generator (PAG) in the form of triarylsulfonium hexafluroantimonate salt [68]. SU-8 was originally introduced by IBM[6] as a

[6] International Business Machines (IBM) Corporation.

negative tone photoresist in 1989. They also used it to make scanning force microscopy probes [69]. This material was also used in LIGA[7] processes to decrease its costs and it is called poor man's LIGA [70]. However recently, SU-8 is used to make MEMS devices. Fabrication of microfluidics channels is one of the applications for SU-8 which is mainly done by soft-lithography and nano-imprinting lithography. SU-8 has recently been used as the main structure for a number of micro-devices in various applications such as micro-valve [71], micro-beam [72], self-assembled structures [73], micro-channels [74], micro-lens [75], optical accelerometer [76], micro-resonator [77], electrostatic micro-actuator [78], micro-gripper with integrated thermal actuator [79], micro-pump [80], optical ammonia gas sensor [81], and integrated force sensor [82].

A general fabrication process was reported [73] which can be exploited to build various SU-8 based micro-structures such as self-assembled structures and micro-cantilevers. For this process, a sacrificial layer (surface micromachining) was used to release the final structures. The sacrificial layer is polystyrene and since it has a good adhesion to gold, chrome/gold is sputtered as the first layer on a silicon substrate. Figure 2.10 shows SU-8 cantilevers fabricated using this technique. The exposure time was adjusted to control the curvature of the cantilevers such that by 35 seconds exposure, all cantilevers had a negative curvature, whereas, by 90 seconds exposure cantilevers were managed to be straight.

[7] LIGA stands for German words Lithographie Galvanoformung Abformtechnik. This process is used for molding tall structures with sometime high aspect ratios.

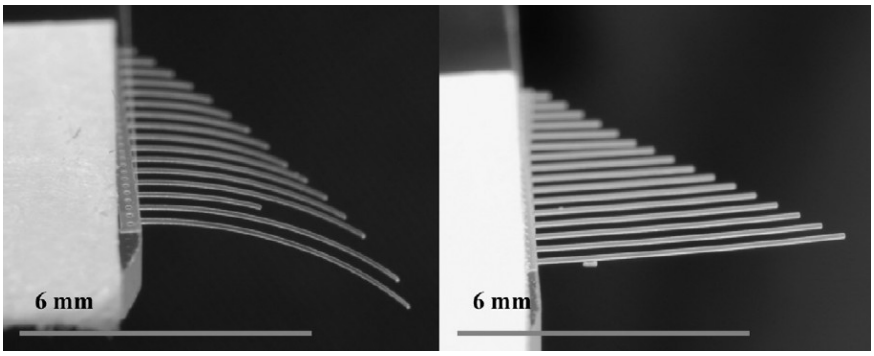


Figure 2.10–The exposure time has been varied to control the curvature of SU-8 cantilevers in a surface micromachining process [73].

To develop a microfabrication technique for polymer-based energy harvesters, various polymer microfabrication techniques were studied in terms of their compatibility with different fabrication techniques such as deep silicon etching. Two examples are illustrated in the following.

Using only 2 masks, a micro-gripper was fabricated using SU-8 (Figure 2.11) [83]. Polysilicon was used as sacrificial layer to be removed by xenon difluoride (XeF_2) afterwards. An interesting stage in this fabrication is that a blind cut was done using dicing machine to remove the silicon substrate underneath the gripper and release the functioning structure. One another interesting stage in this fabrication process is that wafer was diced into chips and then each individual chip was hard-baked at 120ºC for 15 min once before and once after releasing the structure by XeF_2.

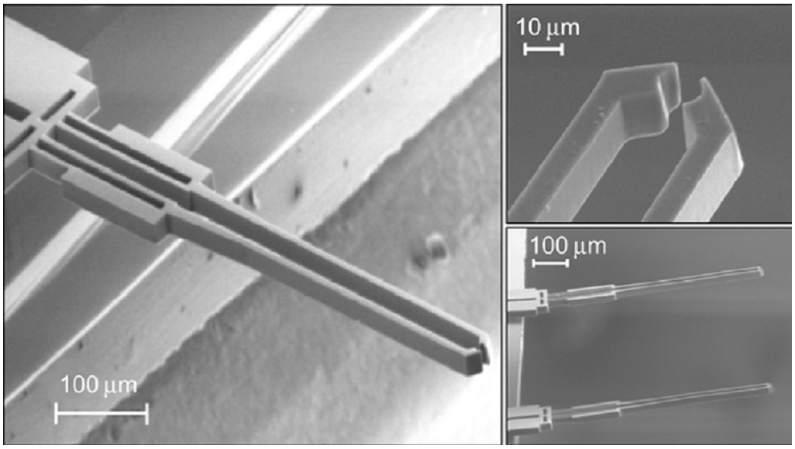


Figure 2.11 – A micro-gripper made of SU-8 [83].

An optical waveguide was made of SU-8 to be used for endoscopy purposes (Figure 2.12) [84]. Both surface and bulk micromachining techniques were exploited to build this structure. The waveguide was made in four steps: oxidation, backside and front side SU-8 patterning and backside etching (Figure 2.12). A 85 μm SU-8 film was coated on 300nm oxide layer which was deposited on a single side polished silicon wafer. Then, a 50 μm SU-8 layer was deposited on the backside of the wafer to mask the silicon etching. After processing the SU-8 layers, the substrate was etched from the backside all the way up to the SU-8 layer on front side using reactive ion etch (RIE). The reported waveguide has 2.1 mm length, 100 μm width and 85 μm thickness.

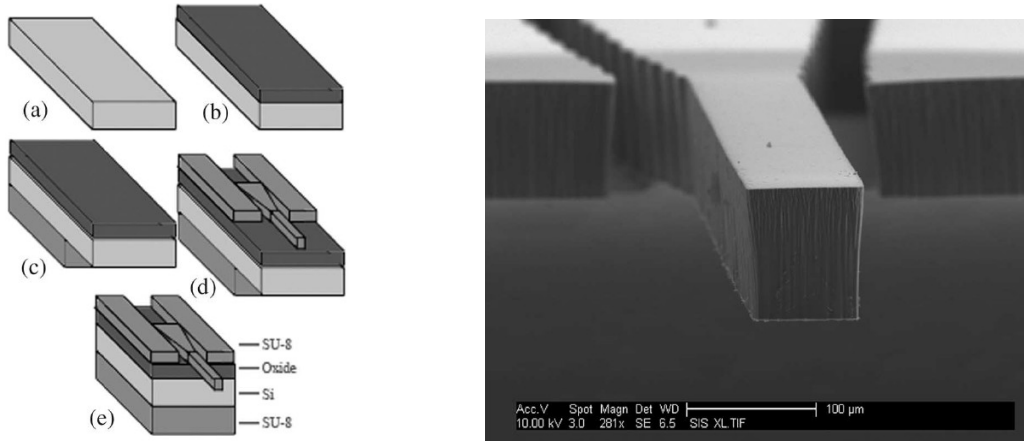


Figure 2.12 – Fabrication process flow and SEM image of a waveguide made of SU-8 [84].

2.4.2 Polymeric structures for energy harvesting

In terms of using polymers for energy harvesters, Mathers et al. [85] have made a cantilever-based energy harvester using PMN-PT (as piezoelectric material) as shown in Figure 2.13. They made a beam with PMN-PT and gold electrodes were deposited and patterned on both sides of the beam. Then, it was dipped into PDMS to coat it with a PDMS layer. The PMNPT/PDMS cantilever was then heated to a temperature 100^{o}C for 15 minutes. To add a proof mass, they only dipped the cantilever's tip into PDMS. They've reported a maximum output voltage of 10 V (0.3 mW power) under a vibration excitation with peak-to-peak amplitude of 1 mm at a frequency of 1.3 kHz. The reported size for this harvester

is 7.4mm × 2mm × 110µm. The fabrication process seems neither scalable nor precise to fabricate MEMS devices. In addition, the natural frequency of the device is higher than low ambient vibration frequency range (<500Hz) which is usually considered for vibration based energy harvesting.

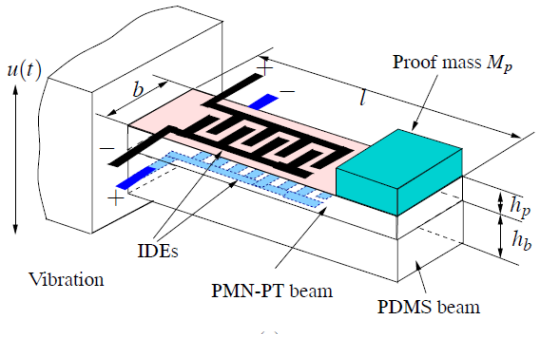


Figure 2.13 – Polymer-based energy harvester [85].

Prashanthi et al [86] have integrated ZnO nanoparticles into SU-8 to make low cost MEMS structures. They have fabricated 250×50×4.5 μm^3 cantilevers with natural frequency of 4.2 kHz. The maximum output power is reported 25 nW across load resistance of 100 kΩ. Considering the fact that the energy harvesters are usually used to harvest the low ambient vibration energy, the reported natural frequency seems very high for energy harvesting applications but could be useful for sensor applications.

Rho et al [87] have reported a technique to fabricate PZT capacitors on a silicon substrate and then transfer them to a thin plastic substrate using an elastomeric stamp. Although the idea is interesting, applying this technique for the microfabricated energy harvesters seems very challenging due to the difficulty of the aligning lifted PZT capacitors to their destination position and also will affect the scalability and batch fabrication capability in fabrication.

Using polymeric structure for the oscillating purposes results in some concerns about their fatigue strength. Hopcroft et al [88] have done micromechanical testing on SU-8 cantilevers and reported that the Young modulus of SU-8 is under 5 GPa. Some other works has been done to address the reliability of SU-8

as a structural material [89, 90]. They have performed cyclic loading on dog-bone SU-8 specimen and showed that the fatigue strength at 100,000 cycles is 98 MPa which is equal to the tensile strength [89]. It is also shown that the fatigue strength is susceptible to stress level [89]. In Chapter 6, it is shown that the maximum mass displacement for the membrane design is 143 μm. Finite element simulation shows that if the maximum displacement is applied to the membrane, the maximum stress in SU-8 layer is 19 MPa. Assuming that the device is not running at maximum displacement during most of the usage time, a long cyclic life is expected for this device. However, it seems that the fatigue strength of the polymer-based energy harvesters should be examined for each specific application.

2.5 Summary

The piezoelectric micro energy harvesting has recently been developed and various advantages and also challenges have been presented in the literature. In this chapter, a number of vibration sources which potentially could be employed for energy harvesting are presented. The piezoelectric effect is explained along with introducing the most common thin film piezoelectric films used for microfabricating micro-energy harvesters. Targeting the low ambient vibration energy, the main concern about MEMS energy harvesters is their high natural frequency due to their tiny sizes. In the following chapters, the focus is on designing micro-energy harvesters with low (<500 Hz) natural frequencies using a different approach than conventional energy harvesters. The possibility of using a softer material as structural material for energy harvesters is investigated in this research aiming to decrease the natural frequency of the MEMS energy harvesters.

Another challenge of the conventional piezoelectric energy harvesters is their narrow frequency bandwidth which could limit their practical applications due to non-constant real ambient vibration frequencies. Some techniques have been reported lately to broaden the frequency bandwidth of the energy harvesters including arrays of cantilevers, resonant frequency tuning, bistable vibrators,

taking advantage of hardening and softening effects, and the multi-degree of freedom oscillators. In this research, the stiffness hardening effect is adapted for the developed energy harvesters to widen their frequency bandwidth to be more useful for real applications.

The next chapter presents the design and methodology of developed energy harvesters in this research. In continue, the microfabrication techniques used to build the devices and also their packaging procedures are demonstrated. Next, the test and characterization stage along with the results are provided. Finally, the conclusion and a few suggestions to improve this research are presented.

Chapter 3 - Design and Analysis

3.1 Overview

The vibration-driven micro-energy harvesting is mostly considered for scavenging the low frequency ambient vibration energy. Therefore, a micro-energy harvester has to have a low resonant frequency. However, the small size of the micro-devices makes them have high resonant frequencies. Some design considerations must be taken into account to decrease the resonant frequency of these devices. In this work, a low frequency silicon-based structure is designed at the size of an electronic chip. This design allows having longer beams which decrease the overall stiffness and consequently decrease the resonant frequency of the structure. The designed structure is capable of harvesting vibration energy in three different frequencies. In addition, the polymeric materials have been investigated, in this work, as the main structural material for vibration driven energy harvesters to decrease the natural frequency of the devices. A polymer-based circular plate has been designed and analyzed as proof-of-concept to be used as a vibration-based energy harvester. A wide bandwidth energy harvester will be more admissible for practical applications. The Duffing effect has been investigated for both of above designs to widen the frequency bandwidth of the energy harvesting. The nonlinear stiffness causing the Duffing effect is modeled using finite element analysis. The results are used in an analytical model to simulate the nonlinear behavior of the structures. In addition, the electrical output of the piezoelectric energy harvesters is modeled using coupled field analyses in ANSYS. The modeling of mechanical and electrical responses of an energy harvester helps to understand the behavior of a device in various situations without making them. The details of the simulations are presented in

this chapter and the results are compared to the experimental measurements in chapter 6.

3.2 Silicon-based MicroChip Design

A fixed-fixed beam design instead of a cantilever design could be exploited for energy harvesting purposes to take advantage of the nonlinear stiffness to widen the harvestable frequency range [49, 91]. However, there are some challenges in designing and fabrication of these structures for micro-energy harvesting. In the case of fixed-fixed beams, the beams must be very thin and/or long to have low resonant frequency. A new design is proposed in this work to employ fixed-fixed beams while keeping the resonant frequency low for small structural sizes. In addition, this structure allows energy harvesting at three different frequencies. Some designs have been proposed in the literature that have more than one harvesting frequency [64, 65], however, making a multi-degree of freedom vibrating structure in MEMS scale seems to have more limitations. A scalable microfabrication process has been exploited in this work to fabricate the proposed energy harvester. One of the motivations behind this work is that a microelectronic chip could be flip-chipped on the proof mass of the above design. Therefore, the resonant frequency of the harvester could be decreased further and also potentially provide in-situ supplementary power for the chip to be used in remote applications.

3.2.1 Multi Degree of Freedom Structure

The designed microstructure is shown in Figure 1.2.b. In this design, the proof mass of the structure is suspended by two beams which are fixed to the device frame. There are four (2 on each beam) piezoelectric elements on the beams to harvest environmental vibration energy. One advantage of the presented design over a regular fixed-fixed beam [92] (Figure 1.2(a)) is that longer beams (equal to the length of the proof mass) could be exploited without changing the overall size of the device. The longer the beam length is, the lower the resonant frequency would be.

Another advantage of this structure is that its first three vibration mode shapes deflects the beams such that their piezoelectric elements are under strain. Designing the resonant frequencies of those mode shapes to be within the low ambient vibration frequency range [92] allow using this design for energy harvesting in multiple vibration mode shapes. Figure 3.1 shows a frequency spectrum of the vibration velocity of an energy harvester measured by a Polytec laser Doppler vibrometer. Within the shown frequency range, there are three peaks representing the resonance at three mode shapes of the structure. The mode shape images taken from a finite element modal analysis are also shown for each particular peak. Table 3.1 provides the specifications of two energy harvesters which were fabricated in this work. The larger harvester (CEH-2) has lower resonant frequencies and smaller gaps between the three peaks.

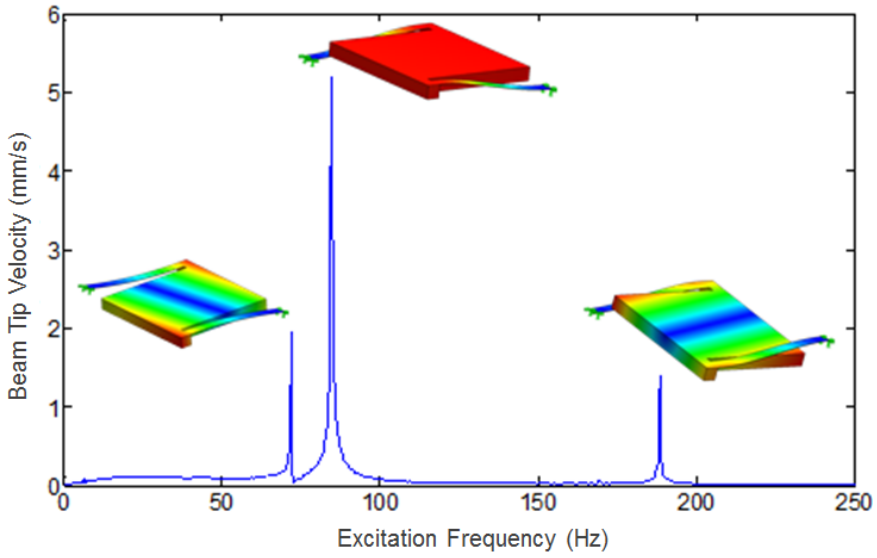


Figure 3.1–The presented design (CEH-2) peaks at three low resonant frequencies. The graph is from the laser based vibrometer measurement and figures from FEM modal analyses.

Table 3.1–Sizes and resonant frequencies of the fabricated Micro-Chip designs.

Device	Mass size (mm^2)	Beam width (mm)	Beam Thickness (µm)	Resonant frequencies (Hz)		
CEH-1	3×3	0.3	18	205.5	288.8	662.7
CEH-2	6×6	0.5	20	71.8	84.5	188.4

3.2.2 Wide Harvestable Frequency Bandwidth

To estimate the deflection of a vibrating structure under a given base excitation, the stiffness of the structure must be found. In this work, the load–deflection relation of the device is obtained using a finite element simulation in ANSYS. The second mode, which represents the highest nonlinearity in the proposed device, is examined to determine the stiffness values. Figure 3.2 demonstrates the boundary conditions and the applied load for the second mode shape. Both beams are fully clamped from the side which is connected to the harvester frame. A known point load is applied to the center of the proof mass and the resulted deflection is calculated by running a static analysis. The FEM result points are shown in Figure 3.3. Each point in this graph represents a static analysis. These points are connected by curve fitting. The load-deflection equation [92, 93] is used to fit a curve to these result points:

$$F(x) = k_l x + k_n x^3 \tag{3.1}$$

where k_l and k_n are the linear and cubic stiffness parameters. The stiffness coefficients were extracted from the fitted curve as $k_l = 12.32\ \mathrm{N/m}$ and $k_n = 6.38\mathrm{e}6\ \mathrm{N/m^3}$, respectively.

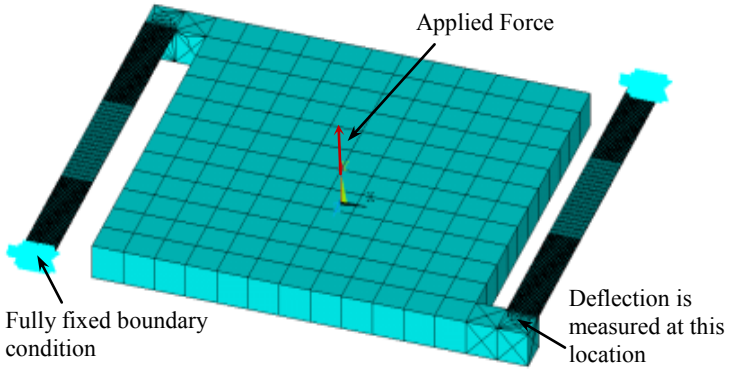


Figure 3.2–Static finite element simulations to calculate the load-deflection relation for second vibration mode shape.

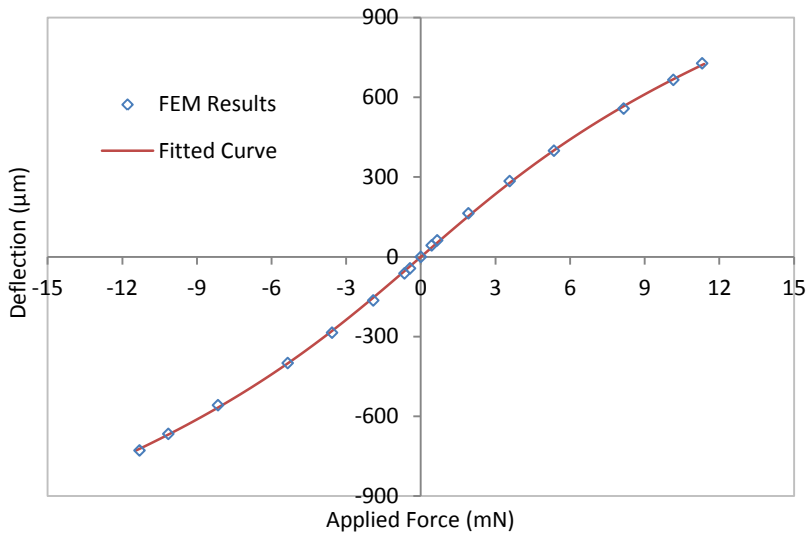


Figure 3.3–Finite element simulation results and the fitted curve for 2nd mode shape of CEH-2.

The total strain induced by the membrane deflection consists of both bending and stretching strains ($\varepsilon_{total} = \varepsilon_{bending} + \varepsilon_{stretching}$). In the larger deflections, the stretching strain dominates and results in the Duffing effect [94, 95]. The differential equation of motion of the system could be written as [96]:

$$M\ddot{\delta} + C_{eq}\dot{\delta} + k_l\delta + k_n\delta^3 = -MAsin\omega t \tag{3.2}$$

where δ is the deflection of the proof mass, M is the proof mass, and A and ω are base excitation acceleration and frequency, respectfully. C_{eq} represents all damping forces of the system. Due to the nonlinearity in the system, the equivalent damping is calculated as [97],

$$C_{eq} = C + \frac{3}{4}\delta^2 c_s \frac{k_n}{k_l} \tag{3.3}$$

where C is the equivalent of a similar linear system which includes all damping effective on the device and it can be calculated using the quality factor [98] and c_s is the structural damping which is assumed to be half of C in this case.

$$C = \frac{\sqrt{k_l M}}{Q} \tag{3.4}$$

Finding C from equation (3.4) and substituting equation (3.3) into equation (3.2) results in a cubic equation with respect to δ^2, where δ is the displacement of the proof mass:

$$\frac{9k_n^2}{16}\left(1+\frac{c_s^2}{k_l^2}\omega^2\right)\delta^6+\frac{3k_n}{2}\left(k_l+\frac{c_sC}{k_l}\omega^2-M\omega^2\right)\delta^4 + (C^2\omega^2+(k_l-M\omega^2)^2)\delta^2-M^2A^2=0 \quad (3.5)$$

Figure 3.4 shows the mass displacement versus excitation frequency which is drawn by solving equation (3.5) for different quality factors. As opposed to the frequency response of a linear system which is a sharp peak with a narrow bandwidth, the frequency response of the second mode shape of CEH-2 represents the Duffing effect [99]. For instance in the case of Q=250, the frequency bandwidth reaches ~12Hz. The frequency bandwidths in this work are all reported based on 3-dB-bandwidth definition as elaborated in [100].

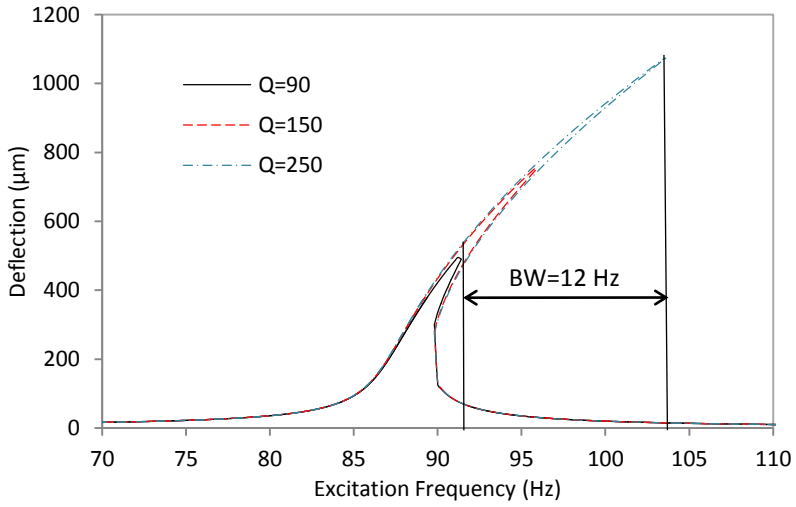


Figure 3.4 – Simulated mass displacement versus frequency for second mode shape of CEH-2.

3.3 Polymer-based Micro Energy Harvester

A polymeric membrane is designed to support piezoelectric energy harvesters. A membrane structure provides the capability of widening the harvestable frequency bandwidth through increasing the stiffness with increasing displacement. Due to the lower Young modulus of SU-8 (~5 GPa [101, 102]) compared to silicon (~160 GPa), a membrane structure with SU-8 could have lower natural frequency to be closer to the low ambient vibration frequencies. Besides, a membrane configuration has been exploited in various applications such as micro-pumps [103], speakers and capacitive micro-machined ultrasonic transducers (CMUTs) [104]. Using a polymeric membrane with piezoelectric elements for the above applications enables in-situ power generation in those systems. Additionally beyond the energy harvesting, some piezoelectric microphones, which were developed mostly for audio applications, use a circular plate configuration [105-108], and a circular diaphragm could be used as actuators [109, 110] and MEMS-based acoustic energy harvesters [111-114]. Therefore, a polymer-based MEMS piezoelectric harvester could be exploited to harvest acoustic energy at low frequency range.

3.3.1 Structural Design

The membrane is made of SU-8 with a proof mass of silicon. Figure 3.5 demonstrates how piezoelectric elements are distributed on the membrane to harvest maximum extractable power out of the membrane vibration. The induced stress on the membrane is maximized around the edges. A longer piezoelectric element would pick up the generated negative voltage which could cancel out a part of the generated positive voltage. This happens due to the deflection form of a circular plate [95]. Table 3.2 presents the dimensions of the designed SU-8 membrane. Four different materials are simulated in ANSYS for a simple membrane with a silicon proof mass and no piezoelectric pads to compare their resonant frequencies. Table 3.3 shows the results of the analyses. The same dimensions as given in Table 3.2 were used for all materials. The membranes in this case are fully fixed around the edge and the modal analysis was performed

identically for all materials. Table 3.3 reveals that comparing a SU-8 and a silicon-based membrane with identical geometries, the SU-8 based membrane has ~5.7 times lower resonant frequency than the silicon-based membrane. Based on the simulation results, the thickness of a silicon membrane must be <0.5µm to have a resonant frequency in the range of a polymeric membrane. Apart from being fragile, such a silicon membrane would be very difficult to fabricate. Therefore, implementing SU-8 as the main structural material for the energy harvesting is beneficial in terms of decreasing the natural frequency of the structure. In this work, the capability of developing a SU-8 based energy harvester is investigated. The fabrication process and challenges are illustrated in Chapter 4 and the results of fabricated devices are provided in Chapter 6.

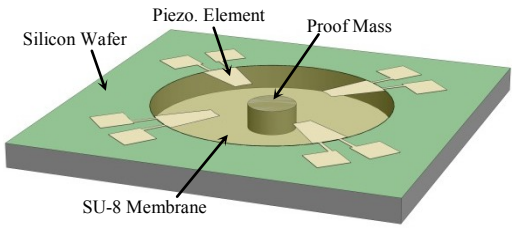


Figure 3.5 – A schematic of arrays of energy harvesting elements on a SU-8 membrane.

Table 3.2 – Energy harvester's specifications.

Membrane Thickness	AlN Thickness	Membrane Radius	Mass Radius	# Piezo. Elements
5µm	1.2µm	3mm	1mm	4

Table 3.3 – Comparing resonant frequency of membranes made in the same size but of different materials from FEA.

Membrane Material	Silicon	Silicon Dioxide	Silicon Nitride	SU-8
Resonant Frequency(Hz)	702.3	448.1	969.8	122.6

3.3.2 Wide Harvestable Frequency Bandwidth

This section examines the nonlinear behavior of the structure. The approach is to simulate the stiffness of the structure by finite element method (FEM) and use those results in a theoretical model to estimate the deflection of the structure based on the excitation frequency spectrum.

A finite element model of the membrane including the piezoelectric elements was prepared in ANSYS. The overall dimensions of the model are the same as Table 3.2. The inner radius of the piezoelectric elements is 2 mm. Each piezoelectric element covers 30 degree of the allocated membrane surface area. In addition, the microfabrication defects are taken into consideration for the simulation such as the silicon dioxide layer at the bottom of the membrane and the undercut which inevitably occurred in XeF_2 etching. The fabrication defects are elaborated in detail in Chapter 4. Considering the defects, an extra proof mass was added by flip-chipping technique to lower the natural frequency of the fabricated device. The total proof mass including the built-in silicon mass and the added extra silicon mass is ~112.8µg. A number of static analyses were run to calculate the deflection of the membrane under a vertical load applied to the proof mass. Figure 3.6 shows the FEM model results. The load-deflection behavior of a membrane follows the form shown in equation (3.1). Therefore, MATLAB was employed to fit a specific curve using equation (3.1) to the FEM result points (Figure 3.6). Consequently, the linear and cubic stiffness coefficients were extracted from the fitted curve. The resulted stiffness values are $k_l = 713.78\ N/m$ and $k_n = 5.5e10\ N/m^3$, respectively.

Figure 3.7 shows the mass displacement versus excitation frequency obtained by solving equation (3.5) for different quality factors. As opposed to the frequency response of a cantilever which is a sharp peak with narrow bandwidth (~1 Hz) as shown in Figure 1.1, the frequency response of the membrane is skewed to the right representing the Duffing effect [99]. Figure 3.7 shows that the frequency bandwidth of the nonlinear harvester is much wider (for instance 290 Hz in the

case of Q=90) than linear oscillators. The quality factor is a function of damping. Therefore as shown in Figure 3.7, by controlling the damping of the vibrating structure, the bandwidth of the vibration could be adjusted.

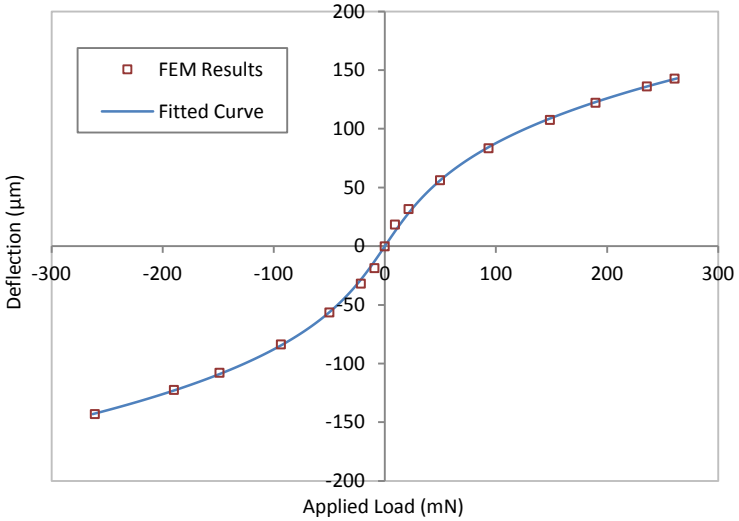


Figure 3.6–Stiffness calculation using ANSYS and fitted curve to extract linear and cubic stiffness coefficients.

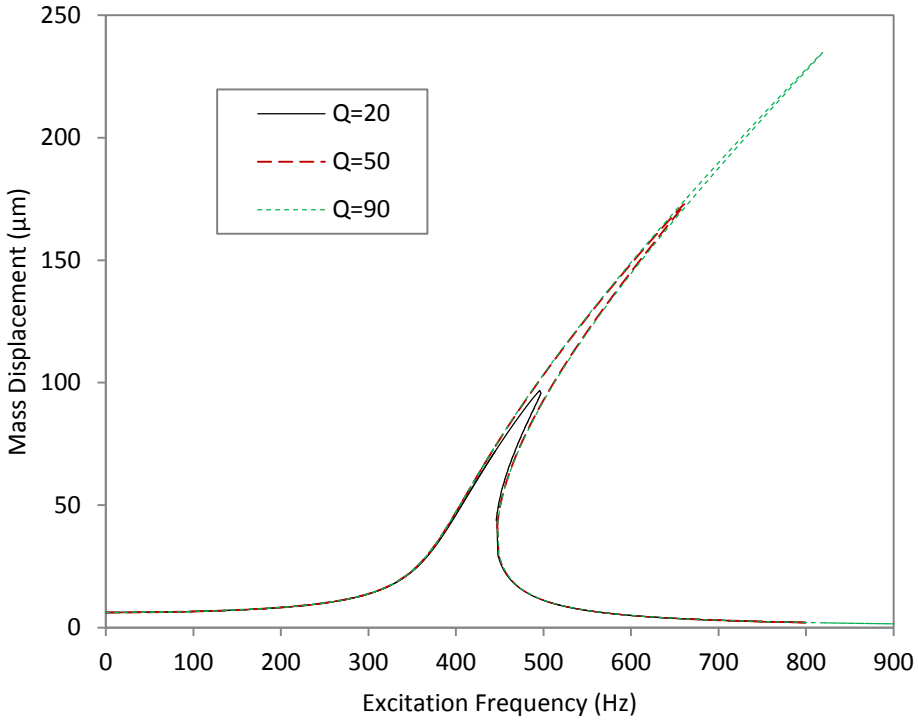


Figure 3.7–Theoretical mass displacement versus frequency.

3.4 Finite Element Simulation

Finite element simulations in ANSYS have been used to model the designed energy harvesters and estimate the mechanical behavior or electrical outputs. Modal analysis is used to estimate the natural frequencies of the designed structures and examine their mode shapes. Coupled field analysis is used to determine an estimation of the electrical outputs of the energy harvesters. For both above designs in which nonlinear stiffness plays an important role, the large deflection effect must be considered in the static analysis. In addition to the above designs, some cantilever designs were fabricated to characterize the fabrication steps and also the simulation process. These designs have been examined in the following sections and their experimental results are provided in Chapter 6.

3.4.1 Frequency Characterization

In the modal analyses of this work, the top and bottom electrodes are not modeled due to their very thin thickness. The silicon, SU-8, and piezoelectric layers are modeled. In the fabrication masks a number of cantilever designs were included as well. These designs were used to characterize the fabrication steps and also the simulation process. Figure 3.8 shows three configurations of the designed and fabricated cantilever-based energy harvesters. These configurations were used for characterizing both mechanical and electrical responses of the energy harvesters. In the modal analysis, the microfabrication defects such as etching undercuts were taken into consideration to more accurately simulate the geometry of the structure for the analysis. The details about each configuration design are provided in Section 6.3.3. In addition, the results of the finite element analysis for various configurations are compared to experimental results.

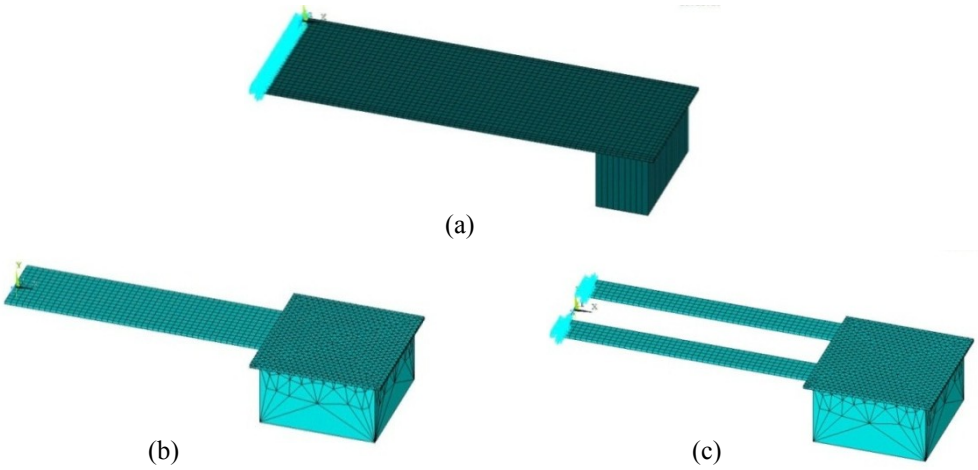
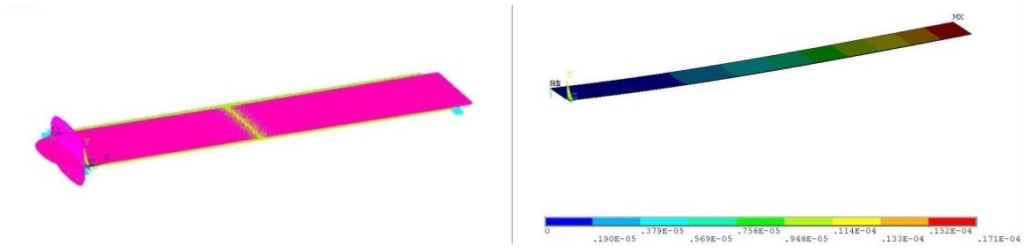


Figure 3.8 – The designed cantilever configurations are simulated in ANSYS.

3.4.2 Electrical Output Characterization

A set of coupled field finite element analyses is conducted in ANSYS to simulate the electrical output of the piezoelectric elements of the various configurations of the energy harvesters with respect to the deflection of the structure. Figure 3.9(a) illustrates the boundary condition set for a cantilever with piezoelectric layer as an example. The left side of the cantilever is fully fixed and a displacement load is applied to the right side of the cantilever. The bottom electrode is defined as ground (voltage is set to zero) and the top electrode shows the generated voltage due to the bending of the cantilever. Figure 3.9(b) represents the deflection of the beam which is 17.1μm at the tip. This is the same displacement applied to the tip as input loading. Figure 3.10 demonstrates the electrical potential gradient induced in the thickness of the piezoelectric layer. The top and bottom surfaces of the beam are defined as top and bottom electrodes. Therefore, those surfaces are unicolor and the gradient starts from blue which is zero volt (defined to be ground) to red which is 71.5mV in this particular case. The properties of the piezoelectric layer are extracted from literature [115] and provided in Table 3.4. The results of the finite element analysis in comparison to the experimental measurements are given in Section 6.3.3.



(a) (b)

Figure 3.9 – (a) The boundary condition set for finite element analysis, (b) the deflection of the cantilever tip due to displacement applied to the tip.

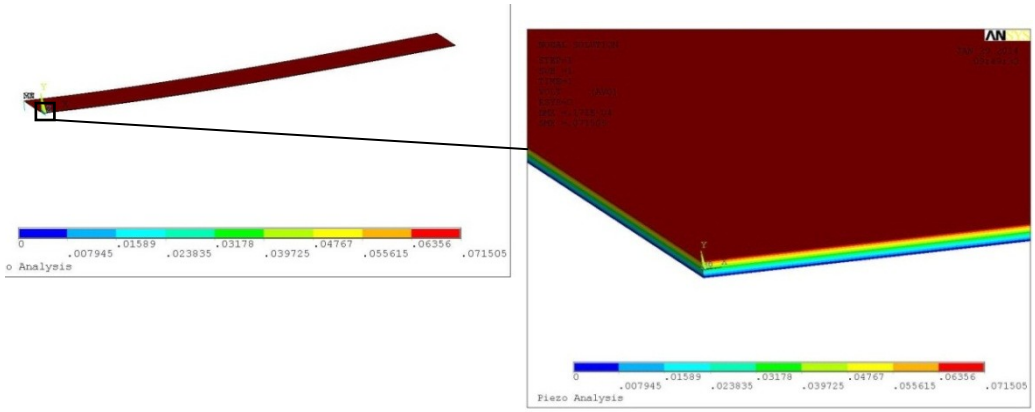


Figure 3.10 – The electrical potential gradient in the thickness of the piezoelectric layer.

Table 3.4 – Material properties of AlN used in the simulation.

Piezoelectric Constants (C/m^2)			Dielectric Constants		Density (kg/m^3)	Elastic Constants (GPa)				
e_{33}	e_{31}	e_{15}	$\varepsilon_{11}/\varepsilon_0$	$\varepsilon_{33}/\varepsilon_0$	ρ	C_{11}	C_{12}	C_{13}	C_{33}	C_{44}
1.39	-0.57	-0.29	8.5	8.5	3260	345	125	120	395	118

Chapter 4 - Microfabrication of the Energy Harvesters

4.1 Overview

Various configurations of energy harvesters were prototyped using silicon and polymer as their structural material. Aluminum Nitride (AlN) thin films were deposited as piezoelectric material to convert the mechanical vibration energy to electrical power. In fact, fabricating energy harvesters with different structural materials (silicon or polymer) requires different fabrication process flows. All of these process flows were developed in University of Alberta Micro and Nanofabrication Facility (NanoFab). In this chapter various designs and a number of fabrication processes are presented in details. First, the silicon-based energy harvesters with AlN as their piezoelectric material are illustrated. Then, the polymer-based energy harvesters with AlN are described. At the end, the challenges faced in the course of fabricating aforementioned energy harvesters are explored.

4.2 Microfabrication of Silicon-Based Devices

4.2.1 Design

All of energy harvesters were designed based on d_{31} piezoelectric mode. A schematic of a simple cantilever-based energy harvester is demonstrated in Figure 4.1. There are two metallic layers, one under and another one above piezoelectric layer working as bottom and top electrodes. The metallic layers have been chosen to be Platinum due to its preferable properties in terms of low resistivity, resistance to oxidation, and resistance to high temperature. In this document, a set of bottom electrode, piezoelectric layer, and top electrode is called *harvesting element*. There are two pads which are connected to the two

metallic layers. The pads are used for electrical connections between the harvesting element and the conditioning circuit at the packaging stage. In addition, a silicon oxide (Oxide) layer is required to electrically isolate the energy harvesting elements from the silicon wafer. All energy harvesting structures, in this work, have a built-in silicon proof mass which is fabricated using bulk micromachining of silicon substrate. The backing silicon is the main structural material defining the overall shape of each structural configuration. The thickness and length of the backing silicon are the main parameters which determine the natural frequency of the resulted energy harvester.

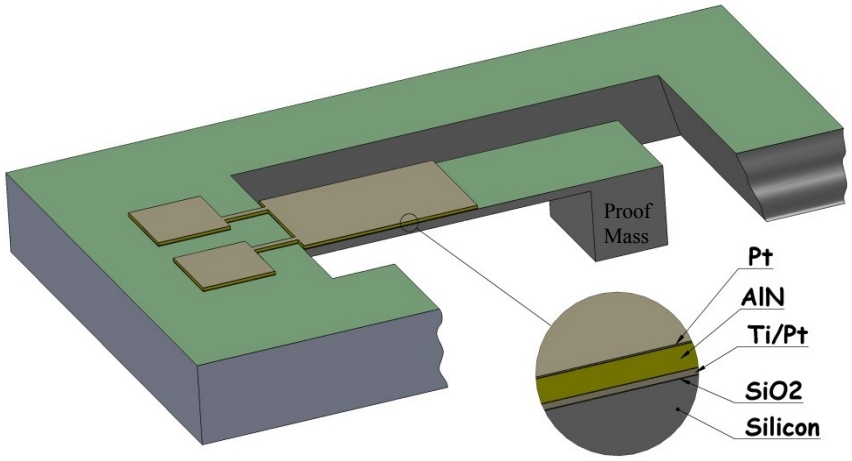


Figure 4.1 – Schematic of a silicon-based energy harvester with d_{31} piezoelectric mode.

Various structural configurations of silicon-based energy harvesters were designed and fabricated in this work. All of these designs were fitted in a set of 5"×5" masks aimed for 4" silicon wafers using L-Edit. A number of cantilever-based energy harvesters along with two special structural configurations (Microchip and Membrane designs) have been designed and fabricated. In the following the schematic process flow figures are shown for the Microchip and Membrane designs. However, all silicon-based configurations have the same fabrication processes. As well, all polymer-based energy harvesters were fabricated using the same processes.

4.2.2 Process Flow

The developed fabrication process flow for the Microchip design (same for all silicon-based energy harvesters) is shown in Figure 4.2. In this process, 5 masks were used: two for patterning backside and front side of the silicon substrate and the other three for pattering bottom electrode, piezoelectric layer, and top electrode.

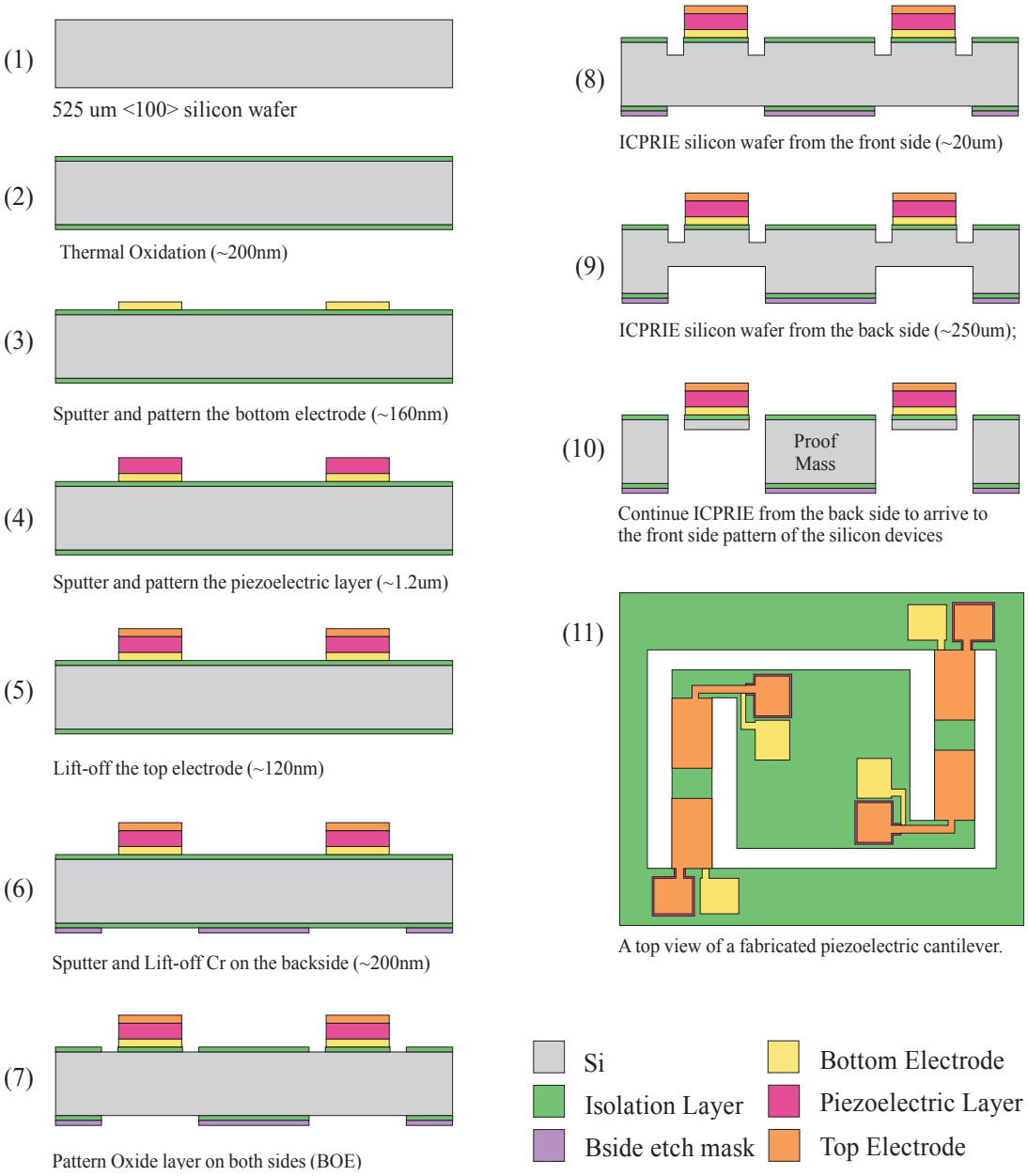


Figure 4.2 – The process flow developed to fabricate silicon-based energy harvesters.

Each fabrication step is explained in details in the following. Each section is numbered such that the number matches each step's assigned number in Figure 4.2.

(1) *Silicon Wafer* – The process starts with a 4" p-type <100> silicon wafer. It has been experienced that any other orientation or doping type of silicon wafer could be used without affecting the general process flow apart from RIE etch rate. The thickness of the wafer was chosen to be 525±10μm due to consistency in fabrication process of one wafer over another. One of the main concerns about choosing proper silicon wafers for this process flow was that, the silicon wafers must be transparent to infrared. Otherwise, the backside aligning would be impossible. Therefore, transparency of all the wafers was tested prior to start any fabrication processes on them. The wafer is cleaned by Piranha cleaning (soaked in 3 H_2SO_4:1 H_2O_2 solution) for 15 minutes, dried and prepared for the next step.

(2) *Wet Thermal Oxidation* – A silicon dioxide (SiO_2) layer is required to isolate the harvesting elements from the silicon substrate. Minibrute Top Furnace in NanoFab was used at 950ºC for one hour and 45 minutes with wet vapor inlet from a bubbler set at 95°C and a nitrogen flow set at 40 liter/min. A thickness of ~250nm oxide layer was grown on both sides of the silicon wafer.

(3) *Sputter and Pattern Bottom Electrode* – In this step thin layers of Titanium (Ti) and Platinum (Pt) were deposited and patterned by lift-off process:

   a. First Mask was used in an optical photolithography process to pattern a photoresist layer. Since lift-off was required to pattern the Pt layer, AZ 5214E was chosen at this stage because it leaves negative sidewalls after patterning and also it quickly dissolves in Acetone. For this step, the negative tone of the photoresist[8] was used to accommodate the available Mask. AZ 5214E was spread at 500 RPM for 10 seconds and spun at 2000 RPM for 30 seconds. This followed

[8] AZ 5214E photoresist could be used for both positive and negative pattern transfers.

by a soft-bake at 90ºC for 90 seconds. The wafer was left to cool down and rehydrate for around 15min before exposing. The photoresist was exposed to ultraviolate (UV) light under the first mask with exposure energy of 514 mJ/cm^2. A post exposure bake is required at 110ºC for 2 minutes[9] followed by a flood exposure (without a mask) for 60 seconds. This step is necessary to convert the pattern of the Mask. Finally, the photoresist was developed in MF CD 319 for 35 seconds. This process provides ~2.25μm thick AZ 5214E patterns on the wafer. At this stage, the backside of the wafer is also covered with a photoresist (without patterns) to protect the silicon surface in the following steps from dust and scratches. As this protecting photoresist layer would be removed at different stages (e.g. lift-off), a new protection photoresist layer is spin-coated after each removal.

b. Next step is sputtering the bottom metallic layer on the patterned photoresist. Sputtering System #1 (BOB) in NanoFab is used for this step. Titanium (Ti) is used as an adhesion layer between Pt and Oxide layers. ~20nm of Ti and ~200nm of Pt are deposited at 7 mTorr deposition pressure. The required base pressure is $\leq 1.6\times10^{-6}$ Torr which takes about 1 hour to pump down before carrying on the sputtering.

c. Finally, ultrasonic Acetone bath is used to lift-off the sputtered layer and leave a pattern of Ti/Pt on the wafer based on Mask #1 pattern. Since AZ 5214E photoresist quickly dissolves in Acetone, the lift-off process takes no more than 10 minutes. It has been experienced that if the wafer is soaked vertically in acetone, the lift-off process would be accelerated. Eventually, Acetone, Isopropyl Alcohol (IPA) and

[9] The temperature of the post exposure bake is critical. In fact, high post exposure bake temperatures would cause longer development stage and may result in no photoresist removal in the patterns. A special attention must be paid to characterize this particular temperature beside other parameters of this photography step. This issue was solved by some research in the product data sheet, literature and several experimental tests in NanoFab.

deionized (DI) water rinses, followed by nitrogen drying, cleans the wafer and prepares the wafer for the next step.

(4) *Deposition and Pattern of the Piezoelectric Layer* – An Aluminum Nitride (AlN) thin film is deposited as piezoelectric layer for various structural configurations of energy harvesters. Mask #2 was used in this step to pattern the piezoelectric layer. The deposition step of the AlN film is one of the most critical steps in the fabrication process because the orientation of the film affects its piezoelectric properties. The desired crystallographic orientation of AlN layer is (002). Lead Zirconate Titanate (PZT) was also considered in this research. The deposition and etching progresses were developed. However, some tool problems in NanoFab prevented further progress with PZT thin films. The detailed steps taken for PZT process are presented in Appendix A.

a. Deposition[10]: The AlN film is deposited in a DC magnetron sputtering system in an $Ar+N_2$ atmosphere. The base pressure in the chamber is reduced to remove any contaminants that could affect the orientation of the AlN film. Sputtering System #2 (Doug) in NanoFab is used at this stage. The sputtering system utilizes two pulsed DC power supplies and hence two 3" diameters by 0.25" thickness, high purity (99.9995%) Aluminum targets from Kurt J. Lesker Canada Inc. The applied power is set at 300W. The average deposition rate is 6nm/min. The thickness of the AlN film deposited in these conditions is 1.1μm ±50nm. The crystalline orientation of the AlN film is examined via X-Ray Diffraction (XRD) using mono-chromatized Cu Kα radiation. Figure 4.3 demonstrates the XRD result where ~1.1 μm is deposited on ~160nm Platinum /20nm Titanium/~250nm silicon oxide/silicon. In addition, Figure 4.4 shows a cross section of the AlN layer which has a vertical orientation from the wafer surface.

[10] The sputtering recipe of AlN layer has been adapted from Mr. Mohamed El Gowini's work for his PhD program.

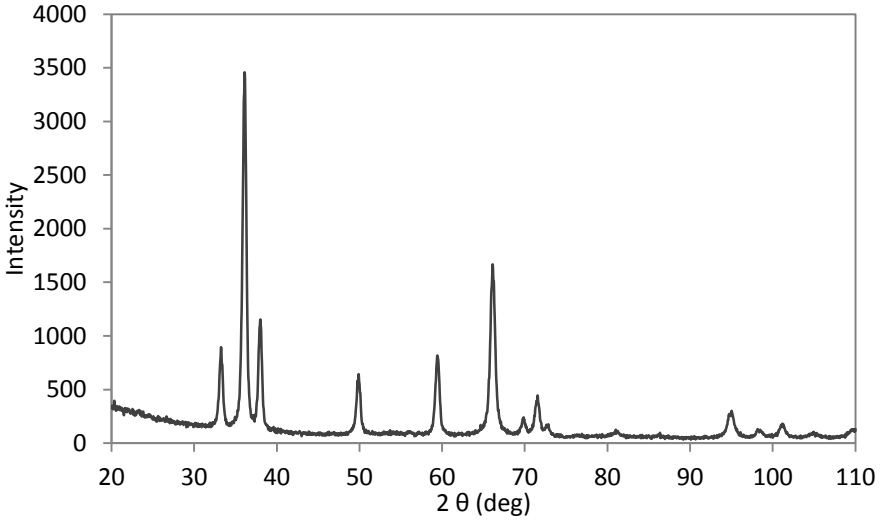


Figure 4.3 – X-ray diffraction patterns for AlN deposited on platinum layer.

b. Pattern-1: Mask #2 was used to pattern the piezoelectric layer. Both lift-off and etching processes were used to pattern the AlN layer. The advantage of lift-off process is that for thin AlN layers (≤500nm), both AlN layer and top electrode could be patterned by only one set of lithography and sonication steps. Two layers of HPR 506 photoresist were spun on the wafer with 500RPM for 10 seconds and 2000RPM for 30 seconds. Each spin follows by a soft-bake at 115ºC for 90 seconds. The wafer is left for ~15 minutes to cool down and rehydrate. This provides ~7µm thickness of photoresist. Mask #2 is used to pattern the photoresist. The photoresist was exposed to ultraviolet (UV) light with exposure energy of 195 mJ/cm^2. Finally, the photoresist was developed in MICROPOSIT 354 developer (an aqueous alkaline solution) for 60 seconds. Then, the wafer is rinsed with DI water and dried by nitrogen gun. Then, an AlN layer is deposited using Doug sputtering system and then a ~120nm Pt layer is deposited by Bob sputtering system and finally an Acetone soak and sonication (same as section 3.c) completes the piezoelectric and top electrode patterning stage.

c. Pattern-2: In case of thicker AlN layers, the lift-off process was not exploited. The thicker AlN layer requires longer sputtering time

which causes the photoresist to crack. These cracks cause unclean patterns of AlN after lift-off. In addition, if the top electrode is deposited on the cracked photoresist and AlN, it would easily cause short circuit between the top and bottom electrodes. With respect to etching, AZ 400K solution which is known as photoresist developer was used to etch AlN layer. It seems that existing KOH in AZ 400K solution is the main reason of etching AlN. Since AZ 400K is used for etching, a photoresist from AZ group (AZ 4620) is used for this step. In addition, the photoresist should not be exposed to the environmental light and the etching process has to be done in the lithography room to protect the photoresist patterns. This etchant has no effect on Pt layer, whereas, if Al bottom electrode was used, it could be etched by AlN etchant. Since color distinction is not possible between AlN and Pt, it would be difficult to recognize the end of the etching process. Therefore, Alpha Step IQ surface profiler is used to ensure fully removal of AlN from the surface of Pt bottom electrode.

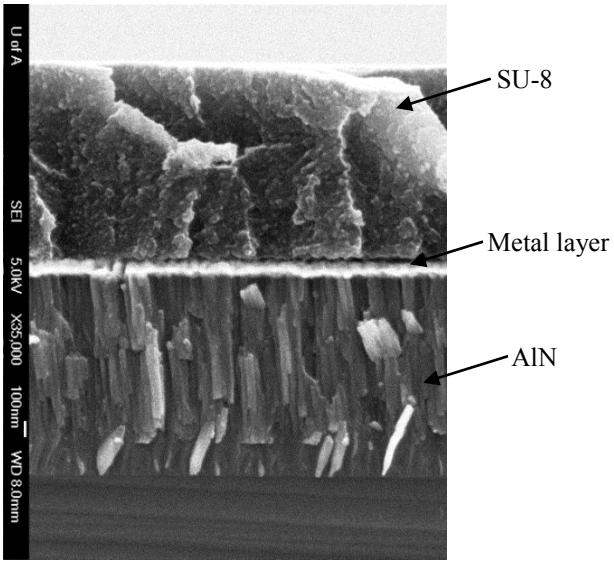


Figure 4.4 – The orientation of AlN layer is at 90˚ from the surface of the wafer[11].

[11] This image is taken by Mr. El Gowini and is included here with his permission.

(5) *Pattern Top Electrode* – Lift-off process was used again to pattern Pt top electrode.

a. First, Mask #3 was used in photolithography to pattern a photoresist layer. HPR 506 photoresist was chosen for this step as it provides thick layer to make the lift-off process easier. The reason is that the sputtering is directional and the taller the sidewall (and the thinner the sputtered layer) is, the bigger gap would be formed between the main metal pattern and the metal on the photoresist. At this step, two layers of HPR 506 were deposited with spread/spin speeds of 500/3000RPM for 10/30 seconds and soft-baked at 115ºC for 90 seconds in a vacuum hotplate. The photoresist was exposed under 195 mJ/cm^2 exposure energy and then developed in MICROPOSIT 354 developer for around 1 minute. This process provides ~7μm thick HPR 506 patterns on the wafer. A hard-bake was also done in a vacuum hotplate at 100ºC for 5–10 minutes.

b. BOB sputtering system was used to deposit ~120nm of Pt on the piezoelectric layer.

c. Finally, ultrasonic bath was used to complete the lift-off process and leave Pt top electrode patterns on the piezoelectric layer. This process took around 12 minutes and then Acetone, IPA and DI water rinses and nitrogen drying would clean the wafer.

(6) *Backside Patterning* – A lift-off process was used to pattern a thin layer of Chromium (Cr) on the backside of the silicon wafer.

a. The photolithography in this step is slightly different as the mask for the backside pattern must be aligned to the front side bottom electrode pattern. This is done by Mask Aligner Station 2 (Ernie) in NanoFab. Clean wafers at this stage and well-designed alignment marks are crucial to properly align the mask with the pattern on the front side of the wafer. AZ 5214E photoresist was also used at this stage. The spinning, exposure and developing parameters were the

same as Step (3)–a, except using Mask #4 for this step. Note that, the front side of the wafer is covered at this stage with HPR 506 photoresist to protect the previously fabricated front side patterns. Spread/spin speeds for HPR 506 photoresist were 500/2000 RPM for 10/30 seconds and baking temperature was 115ºC for 90 seconds.

b. Floyd sputtering system in NanoFab is used to deposit ~200nm of Cr on the backside of the wafer.

c. Finally, an ultrasonic bath is used to perform the lift-off and leave a pattern of Cr layer which will work as a mask for the backside silicon etching. This process is quick and takes about 5 minutes. Acetone soak dissolves the photoresists on both sides of the wafer. Therefore, both sides of the wafer must be carefully and patiently cleaned by Acetone, IPA and DI water rinses and nitrogen drying. The cleaning at this stage is critical for the success of the following steps (Figure 4.5). Since both sides of the wafer need to be cleaned, handling the wafer for rinsing acetone and IPA requires some experience. Any metallic particles resulted from lift-off could cause short-circuit between the top and bottom electrodes and any defects of the photoresist on either side of the wafer could cause uneven deep backside silicon etching or result in defective released structures.

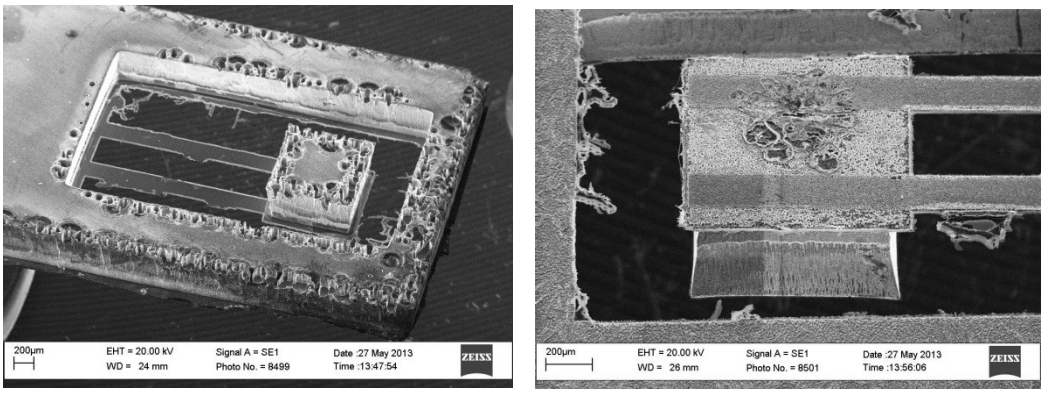


Figure 4.5 – Improperly cleaning both sides of the wafer causes defective released devices.

(7) *Oxide Patterning* – The oxide layer which was grown on both sides of the wafer at Step (2) is patterned at this stage. This pattern reveals the boundary of the devices by etching oxide layer. This step exposes silicon on both front and back sides of the wafer to be etched at Steps (8) – (9).

   a. Mask #5 was used to pattern one layer of HPR 506 photoresist on front side of the wafer. Spread and spin speeds were 500 and 2000 RPM for 10 and 30 seconds, respectively. The photoresist was exposed under 195 mJ/cm^2 exposure energy and then patterned in MICROPOSIT 354 developer for maximum 36 seconds. This photoresist is used as an etch mask to pattern oxide layer on the front side of the wafer. The back side of the wafer is left as it is with Chromium patterns at this stage.

   b. Buffered Oxide Etch (BOE) is used to pattern oxide layer on both sides of the wafer at the same time. Masking layer on front side is the photoresist and on the backside is the Chromium layer. Since both oxide layers have the same thickness (grown at Step (2)), there would not be any issues such as over-etching one side while the other side is under-etched. The etch rate is regularly ~55 nm/min, however, this rate can change based on using fresh or used BOE solution and the number of re-using BOE solution.

(8) *Front Side Silicon Etch* – It has been experienced in the back side etching of the silicon substrate, estimation of the remaining thickness of the silicon wafer is difficult. Considering the fact that the etch rate of the deep RIE process in NanoFab facility could change from time to time, the determined thickness of silicon structure, using SEM images, may not work for the DRIE at next time[12]. Therefore, the silicon etching step is ordered such that the required thickness of the silicon for devices is etched from the front side and then the back side silicon etching releases the structure. The front side

[12] Due to numerous users and various processes done using the same equipment, the o-ring could be contaminated and cause some pressure leak or isotropic etching which eventually result in different etch rates.

provides a great sign to stop the back side silicon etching with a better understanding of the final thickness of the devices.

a. Lithography – After BOE process, the front side photoresist is not stripped. Therefore, the same pattern of the photoresist (Section 7.a) is used to mask the front side silicon etching. The backside of the wafer could be either covered by a thin layer of photoresist or a carrier wafer which could be employed to protect the backside of the wafer from dust or scratches.

b. ICPRIE– Inductively Coupled Plasma Reactive Ion Etching (ICPRIE) is performed on the front side of the wafer using an etcher tool from Surface Technology Systems (STS) in NanoFab. The recipe used in this equipment for this step is called "Standard Etch" and the etch rate is usually ~0.49μm/cycle. The etch rate is subjected to change based on the available amount of silicon to be etched by the tool. ~17μm of silicon is etched from the front side defining an estimation of the final device's thickness[13]. The "Standard Etch" recipe provides quicker etching/passivation steps and less helium leakage rate which leads to less photoresist removal.

(9) *Back Side Silicon Etching* – Backside silicon etching is used to remove the majority of the thickness of the silicon substrate on the devices' patterns and provide the required thickness of silicon as the main structure of the energy harvesters. In addition, backside etching[14] provides sufficient space for an energy harvester to vibrate. Whereas, Surface Micromachining could not be used since it requires depositing a thick sacrificial layer at first stage and keep it until the end of the fabrication process. Because piezoelectric energy harvesters' fabrication process involves experiencing high temperatures (e.g. 700ºC), soaking in several acids and developers, it is very challenging to find

[13] SOI (Silicon on Insulator) wafers could also be exploited to obtain almost the same thickness all across the wafer. However, a SOI wafer is ≥4 times more expensive than a regular prime wafer.

[14] Etching through the thickness of a silicon substrate to build a micro-structure is categorized as Bulk Micromachining process.

a material as sacrificial layer which could go through all these harsh fabricating processes, stay the same condition as it was at first stage and could finally be removed easily. Therefore, Bulk Micromachining was used for this step.

a. Same as Section 8.b an ICPRIE process was performed on the backside of the wafer using an STS etcher in NanoFab. At this stage, the recipe used in this equipment is called "Deep Etch" and the etch rate for our mask is ~1.2μm/cycle. However, the deeper the etched trench, the slower the etch rate become. Around 200 cycles of "Deep Etch" provided ~240μm depth through the backside patterns.

(10) *Back Side Silicon Etching (w/ Carrier Wafer)* – Because of etching the cleaving trenches (see packaging section in Chapter 5), etching further than ~240 μm results in breaking the wafer inside the etching chamber due to the wafer holding mechanism of the STS etcher (Figure 4.6). Therefore, a carrier wafer is used to support the main wafer and continue the same process as Section 9.a from the backside.

a. A carrier silicon wafer which has a thin layer (~200μm) of Chromium on its front side was used as carrier wafer at this step. The Cr layer is used for two reasons: 1-provide better heat transfer across the surface of the wafer; 2-avoid etching the carrier wafer when the backside etching reaches to the carrier wafer. The front side of the main wafer is placed on the front side of the carrier wafer and tiny pieces of Kapton tape were used to fix the two wafers together (Figure 4.7). Backside etch continues with STS etcher using the same "Deep Etch" recipe. The back side etching has a proper etch stop point which is the front side silicon pattern. However, special inspection is needed to determine the required parameters to set on the STS tool at the final stages of the etching. Sometimes, the etching cycles are set to 1 or 2 cycles to save the wafer from over-etch or damage. Alpha Step IQ is used in the NanoFab to inspect the depth of

the trenches, uniformity across the wafer surface, etc. in different stages of the back side etching process. Especially when the back side is close to the end, the inspection is very crucial. Because the thickness of the wafers has a tolerance of ±10μm and the silicon etch rate changes faster in deeper trenches, predicting the depth of etching and hence the remaining thickness of silicon is difficult. Therefore, at the final stages of the back side etch, few cycles are set on the tool and inspection is performed after that[15].

b. Despite taking all possible techniques into consideration to provide a uniform etch, some of the devices cannot be fully released when the back side silicon etch is complete. One of the main reasons is the carrier wafer which causes some non-uniformity in backside cooling of the main wafer. Therefore, the etch rate on different spots of the wafer are different. This non-uniformity result in half released or even unreleased devices when the back side etch has fully released a number of the devices. To release the rest of the devices on the wafer, the main wafer could be flipped so that its front side is up and the backside is placed on the front side of the carrier wafer. A few cycles of "Standard Etch" recipe would fully release most of the remaining devices. The remaining photoresist on the front side (same photoresist from Section 7.a) works as an etch mask in this case as well. The ICPRIE process from the front side cannot be continued for a long time as it becomes an isotropic etch and over etch the fully released devices [48]. In the case of remaining more devices unreleased, individual devices after cleaving (see Chapter 5) could be released using XeF_2 etching technique[16]. This isotropic dry silicon

[15] Despite being expensive, using SOI wafers is a great help at this stage as the buried Oxide layer works as an etch-stopper and the thickness of the device wafer is known and also is uniform all across the wafer.

[16] The associated tool for XeF_2 in NanoFab has a small chamber and any sizes of silicon pieces could be manually loaded inside the chamber, whereas, the ICPRIE tool has a load lock and requires a full 4" wafer. However if possible, ICPRIE is always preferred because it provides anisotropic silicon etching while the XeF_2 isotropically etches silicon and in this case removes some part of proof mass which affects the natural frequency of the device.

etching technique is highly selective to any material other than silicon. Therefore, either the same photoresist from Section 7.a or even oxide and electrodes layers work as mask for XeF_2 etch.

c. Cleaning with RIE-O_2 –Once the back and front side ICPRIE are finished and before cleaving, the full wafer is placed in the μEtch system in NanoFab. This equipment provides a plasma containing Oxygen which is used to oxidize (ash) the photoresist and facilitate its removal. Therefore, the photoresist (which is sometime burned in the ICPRIE process) is removed from the electrodes and the devices leaving a clean wafer. The Pt layers are unaffected in this step, while, Aluminum or other metallic layers could be affected and oxidized.

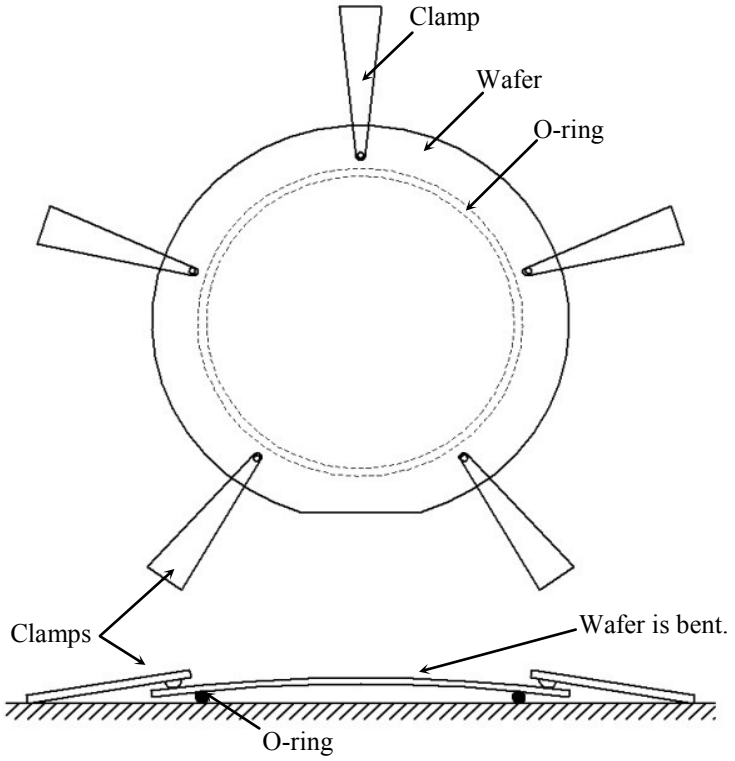


Figure 4.6 – Wafer holding configuration inside the chamber can break the wafer.

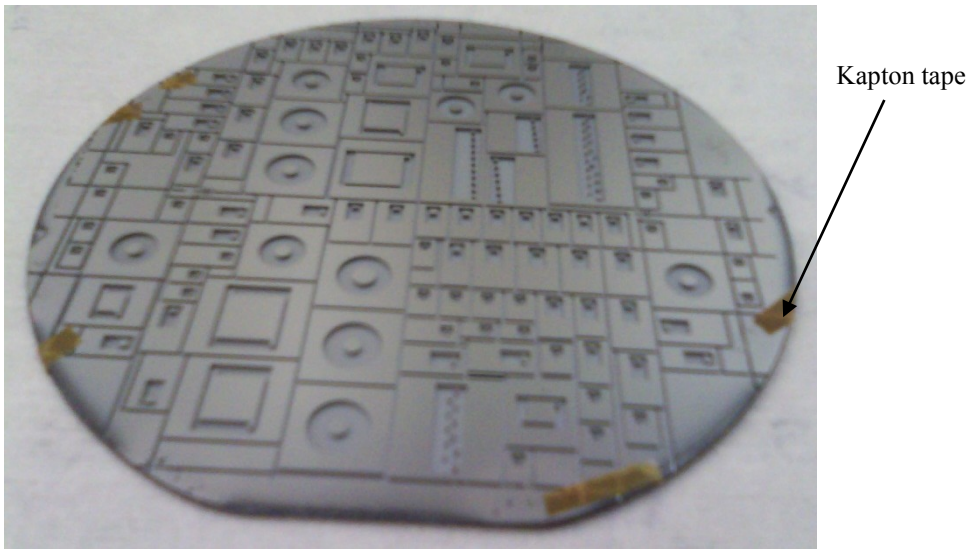


Figure 4.7 –Pieces of Kapton tape are used to fix the main wafer to the carrier wafer.

Instead of using the above technique with Kapton tape to mount a device wafer on a carrier wafer, gluing with a layer of photoresist in between, Crystal Bond glue, double sided blue tapes, etc. could also be exploited. However, due to fragility of the released devices and difficulties in separating the main and carrier wafers after backside etching, the Kapton tape was preferred among all above techniques after many try and error processes. For instance, Figure 4.8 demonstrates the result of using double sided tape to mount a piece of a device wafer on a carrier wafer. Some of the released devices could not be separated from the tape and therefore, break and adhere to the tape.

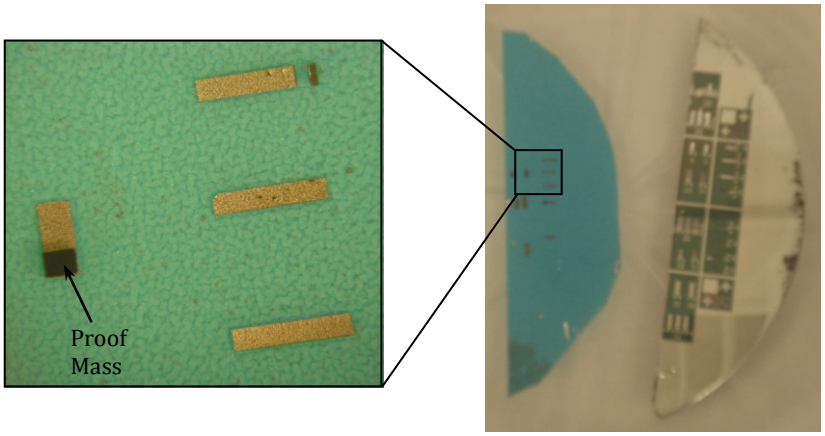


Figure 4.8 – Some of the released devices could break and stay on the tape.

Figure 4.9 shows the front and back side of a full silicon wafer before the final releasing step. Also, Figure 4.10 demonstrates the full wafer with most of the devices fully released. Due to some non-uniformity in the RIE process, when the DRIE process is finished, some devices still need more etching. Continue etching the whole wafer causes over etching previously released devices. Therefore, the devices are cleaved first and RIE or XeF_2 etching is used to fully release the under etched devices. Since XeF_2 has a very selective etch, it only etches silicon and therefore, no photoresist is required at this stage. Silicon oxide layer and the electrodes layers work as masks to finish releasing process. Figure 4.11 shows two devices from the top before the patterning the front side oxide layer. It is shown that how clean are device even after several layers of fabrication.

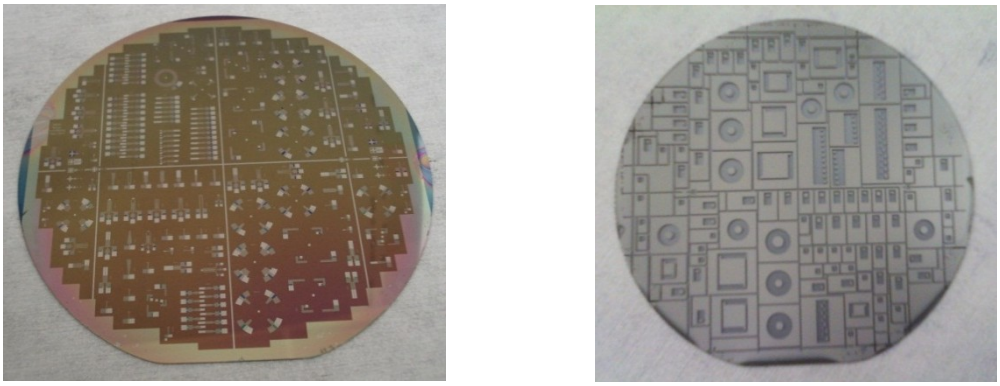


Figure 4.9 – Front and back side of the wafer just before final releasing step.

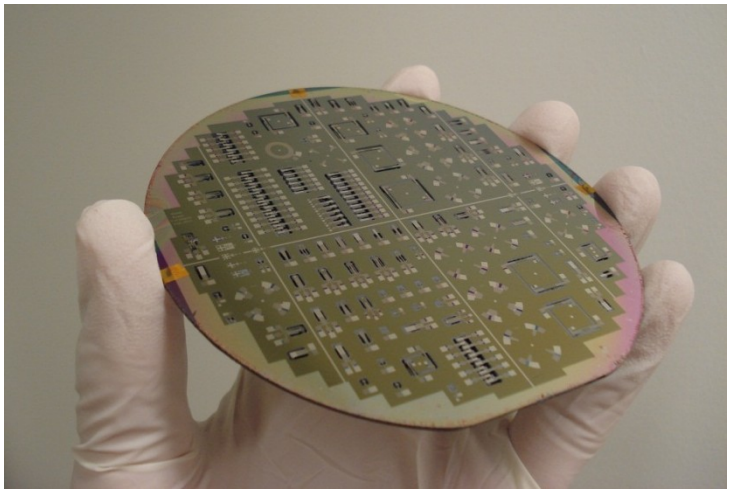


Figure 4.10 – The full wafer after released process and before cleaving.

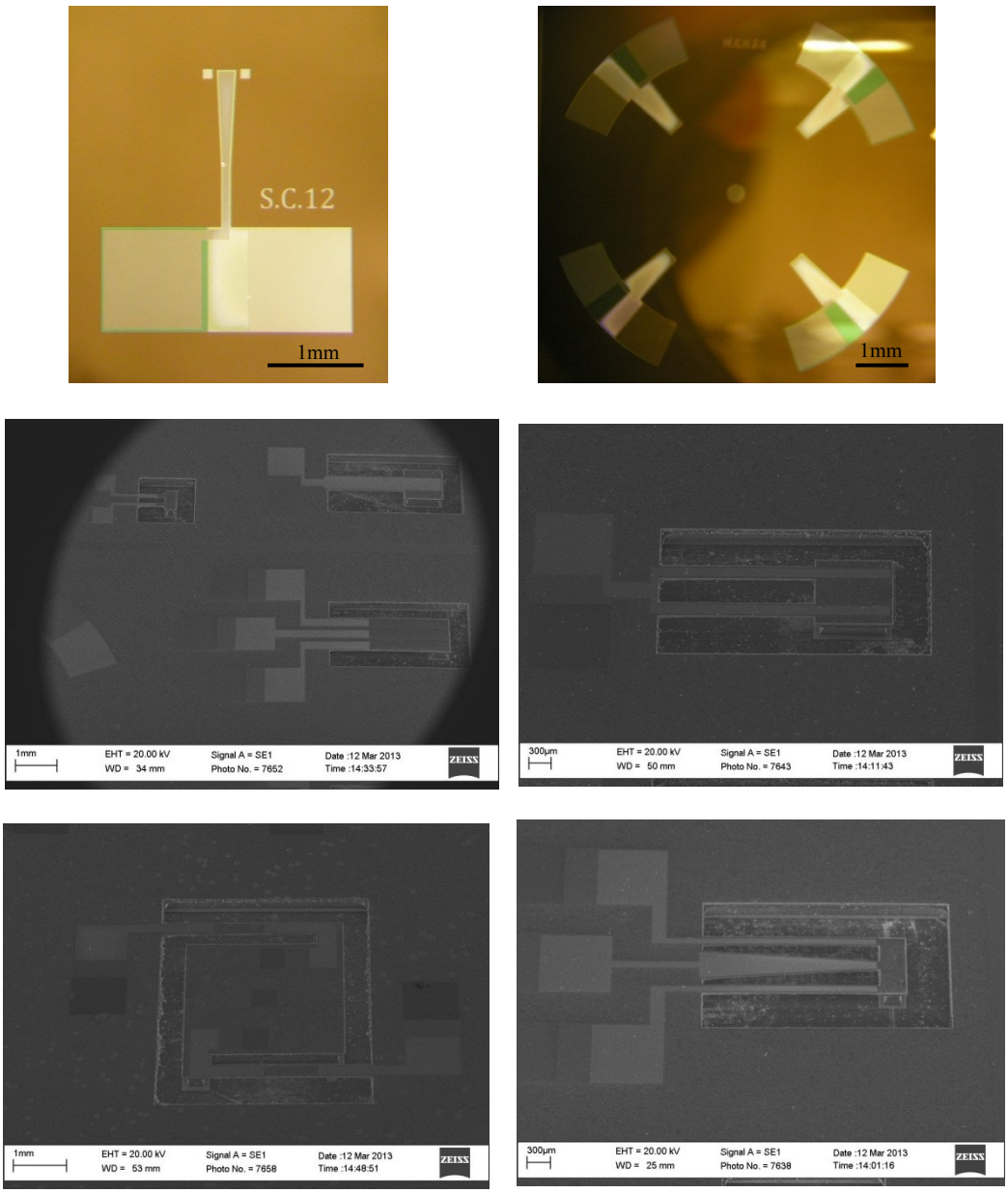


Figure 4.11 – Cleanness of the process is shown before patterning the oxide layer by microscopic images and after releasing by SEM images.

4.3 Microfabrication of Polymer-Based Devices

4.3.1 Design

The process flow for polymer-based energy harvesters was designed such that depositing the SU-8 was one of the last steps in the fabrication. The main reason is that the conditions and the materials used over the course of the fabrication

steps, such as high temperatures in thermal oxidation step and soaking the wafer in various solutions (e.g. Acetone and HF acid), could damage the SU-8 layer. Therefore, the SU-8 deposition was kept to be done before the final releasing step. Except the Micro-Chip design, all the other structural configurations of silicon-based energy harvesters could potentially be used for polymer-based energy harvesters as well. In addition, a circular array of energy harvesters was designed to take advantage of a SU-8 membrane with a silicon proof mass to generate electrical power. Figure 4.12 illustrates two examples of fabricated membranes one shown from the top and the other one shown from the bottom.

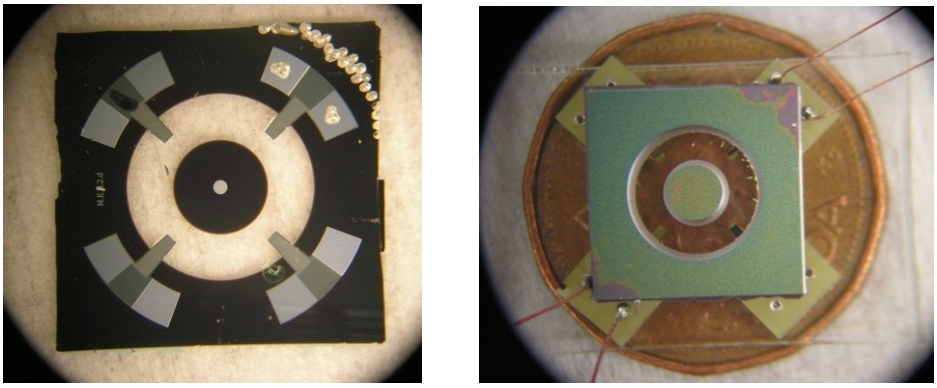


Figure 4.12 – A circular array of energy harvesters on a SU-8 membrane with a silicon proof mass.

4.3.2 Process Flow

The fabrication process flow for making polymer-based energy harvesters is the same as the process flow explained in Section 4.2.2. The only difference is the SU-8 deposition and final releasing stages (Figure 4.13). In total, six masks were used in this process: the same five masks previously used for silicon-based devices plus one more mask to pattern SU-8 layer.

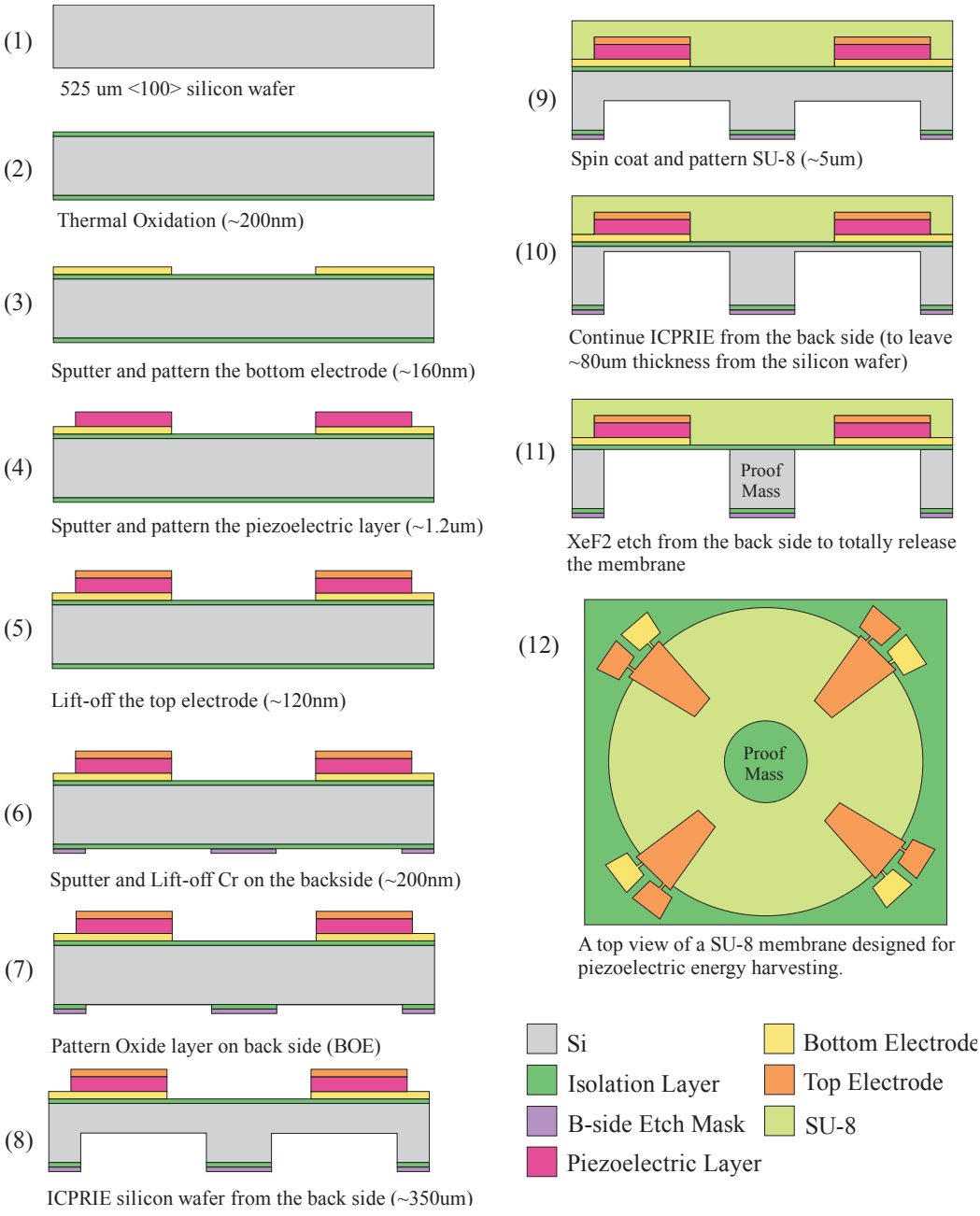


Figure 4.13 – Fabrication Process Flow of Polymer-based Energy Harvesters.

The different fabrication steps are explained in details in the following. Each section is numbered such that the number matches with the number in Figure 4.13.

(1) – (7) These steps are the same as fabrication steps of silicon-based energy harvesters explained in Section 4.2.2.

(8) *Backside Silicon Etching* – This step is the same as Step (9) in Section 4.2.2. The front side of the wafer is covered with HPR 506 photoresist to protect the surface from dust and scratches. In this case, a carrier wafer must be used from the beginning to protect the main wafer due to a deeper back side etch which needs to be done before adding the SU-8 layer on the front side of the wafer. "Deep Etch" recipe is used in the ICPRIE/STS tool in NanoFab to make ~350μm etch from the backside of the wafer. This depth can even be deeper. We have experienced having only ~100μm left from the thickness of the silicon wafer in trenches. The deeper the trenches are at this stage, the better the sidewalls could eventually be obtained, however, the more difficult the handling of the wafer would be. Therefore, there is a tradeoff between the depth of the trenches and the ease of handling in the following steps. Once the backside etching at this stage is complete, the main wafer needs to be separated from the carrier wafer and cleaned for the next step. The photoresist on the front side of the wafer could be removed in two ways: Plasma-O_2 and Acetone rinse. If the trenches are too deep, the plasma-O_2 (same as Section 10.c explained for silicon-based structures) is used to avoid any possible handling issues with rinsing.

(9) *SU-8 Deposition* – SU-8 was originally used as a photoresist and, therefore, the deposition and patterning of a SU-8 thin layer is very similar to spin-coating a common photoresist. However, characterizing the SU-8 deposition parameters with respect to the environment in which it is deposited, needs some trials to figure out the proper parameters. As SU-8 2005 was not available in place, SU-8 2010 and SU-8 2002 were mixed with the ratio of 1.5:1 to obtain SU-8 2005 and it was used in all SU-8 deposition processes:

a. ~5 mL of the resulted solution was spread/spun at 500/3000 RPM for 5/30 seconds. Because there are trenches on the back side of the wafer, the vacuum between the chuck and the wafer does not occur. Therefore, a carrier wafer is required to keep the main wafer on the chuck. This carrier wafer must be removed before baking. Otherwise, it will stick to the main wafer all around its edge making it very difficult to separate.

b. A two-step soft-bake was performed at 65°C and 95°C for 3 and 5 minutes, respectively.

c. The SU-8 layer was exposed under the 6^{th} mask at 357 mJ/min exposure energy.

d. A two-step post exposure bake was performed at 65°C and 95°C for 2 and 5 minutes, respectively.

e. The resulted layer was developed in SU-8 developer (Propylene Glycol Monomethyl Ether Acetate (PGMEA)) for 3 minutes followed by 1 minute IPA soak and spray and finally nitrogen flow to dry off the wafer.

f. Finally, a hard-bake performed in a vacuum hotplate at 150°C for 20 minutes. The hotplate was set to room temperature, then was ramped up to 150°C, was held at that temperature for 20 minutes and finally ramped down to room temperature again. The ramping up and down for this step is critical to control the residual stress of the SU-8 layer.

(10) *Back Side Silicon Etching* – Using a carrier wafer, the backside silicon etch was continued similar to Step (8). This etching continues to leave ~80um from the thickness of the silicon wafer in trenches.

(11) *Back Side XeF_2 Etch* – Since SU-8 would be etched under RIE and the chamber condition can affect the membranes, ICPRIE process must be stopped before it reaches the membrane. The remaining thickness of the silicon wafer in trenches, are removed by XeF2 etch. The XeF_2 etch was continued to remove all silicon underneath the devices to have only SU-8 as structural material. The associated tool for XeF_2 etching in NanoFab has a small chamber with a glass top which allows inspecting the etching progress step by step. Figure 4.14 shows the size of the XeF_2 chamber which is in the process of etching a few individual devices. The process could be stopped at any time even in the middle of etching or expansion. Therefore, the stop point for etching is decided visually. The downside of using XeF_2 is that because this etching is isotropic, it over-etches

the proof mass from its side wall and leaves residues at the edges of the membrane and the proof mass. Both of these side-effects increase the natural frequency of the device.

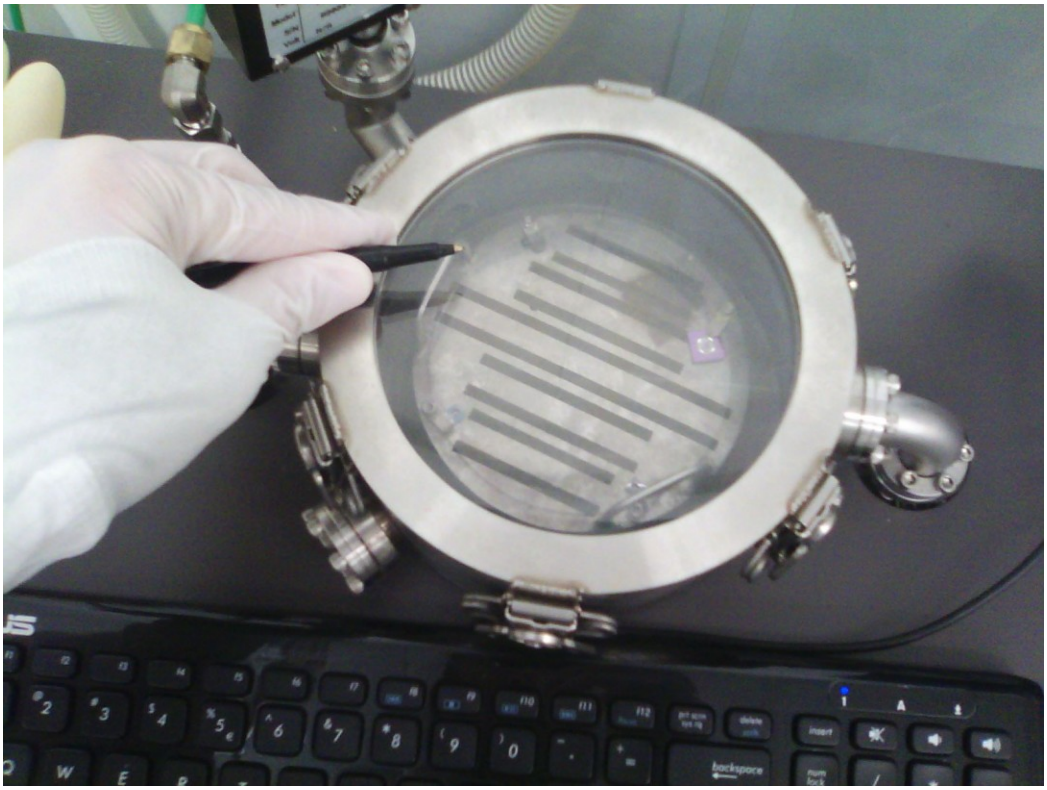


Figure 4.14 – The XeF2 etching chamber allows mounting a full 4" silicon wafer or individual devices.

The final releasing step is very critical and took a long time in this research to find a proper way to do it. Various methods were tried. One of the techniques was using a KOH etching technique. This technique was chosen over DRIE because it only requires soaking the wafer in the KOH solution. So, no hot temperature or harsh etching condition was involved. However, the effect of soaking a wafer with a SU-8 layer on it resulted in delamination of the whole SU-8 layer. Figure 4.15 shows one of the wafers which was soaked in KOH solution for a long time. Although the SU-8 layer is not affected by the KOH solution, the whole layer is delaminated removing some of the electrodes layers with it as well.

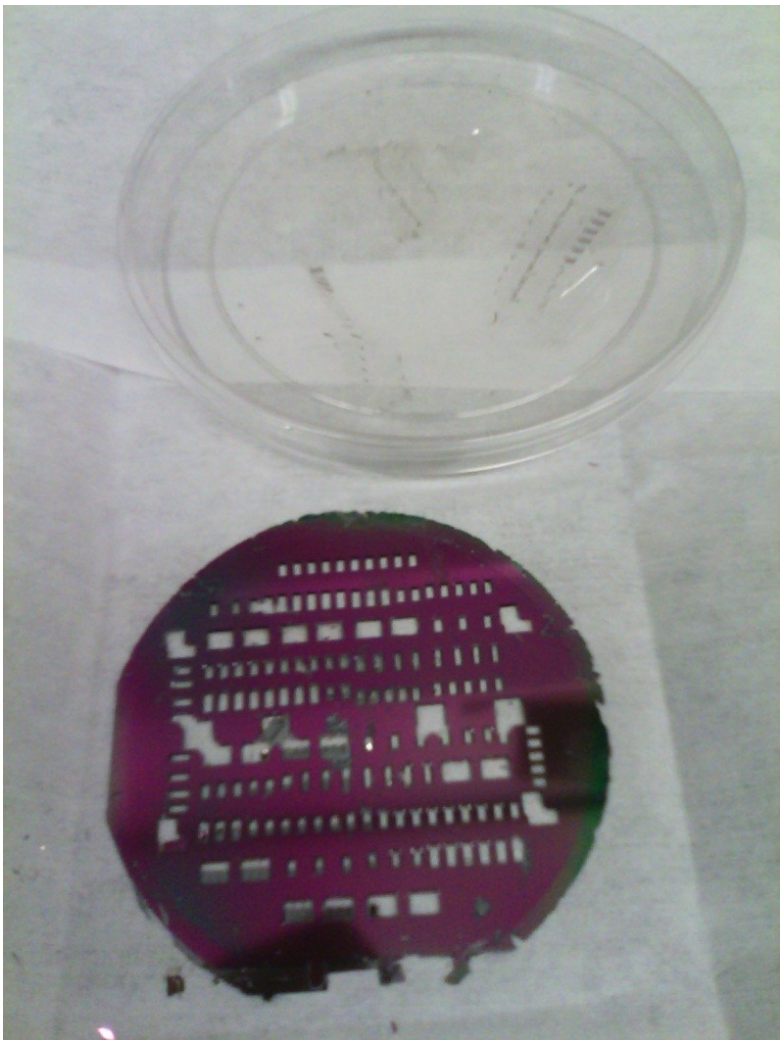


Figure 4.15 – Releasing the polymer based devices with KOH etch.

4.3.3 Aluminum Nitride (AlN) Thin Films

4.3.3.1 AlN Deposition

Various techniques could be used to deposit Aluminum Nitride (AlN) layers including reactive sputtering [116-123], chemical vapor deposition [124], molecular beam epitaxy [125], and pulsed laser deposition [126]. In this research, a reactive sputtering technique was used to deposit AlN[17]. A co-sputtering process of two Aluminum targets in presence of Nitrogen (N_2) flow was used to deposit a thin layer of AlN. Power is set to 300W, deposition

[17] The deposition recipe was adapted from Mr. Mohamed El Gowini's PhD research.

pressure was 4×10^{-7} Torr, deposition rate is ~6.67 nm/min. The main challenge in the AlN deposition for this research was the long sputtering process. The sputtering equipment in UofA NanoFab had to be booked from noon to mid-night. The overall deposition time depended on the condition of the sputtering equipment. The pump down process in some cases took more than 8 hours. Adding the preparation and real sputtering times, the whole deposition stage took very long time to complete.

4.3.3.2 AlN Patterning

Both lift-off and etching was successfully performed to pattern the AlN layer.

a. *Lift-off* – Photolithography was used to pattern two layers of HPR 506 photoresist with the same parameters as Step (5)-a at Section 4.2.2. Then, AlN layer was sputtered and finally an ultrasonic acetone bath was used to complete the lift-off process. Note that in the case of using lift-off process for AlN patterning, the top Pt electrode was sputtered after depositing AlN. Then, both AlN and top electrode layers were lifted-off together. This process was tested in a number of iterations and no short-circuiting between top and bottom electrodes was experienced.

b. *Etching* – Apart from a dry etching method, various wet etching solutions have been reported in the literature as given in Table 4.1 to pattern AlN thin films. Some of the etching acids need to be heated to properly etch AlN layers. Heating acids require special considerations. However in this research, AZ400K developer was used in room temperature and the etch rate was ~5.7 nm/sec. AZ400K is usually exploited as a trivial developer for exposed photoresists. Therefore, it was an easy solution to work with.

Table 4.1 – Etching alternatives for AlN thin layers.

No.	Source	Etching Methods for AlN	Etch Rate (nm/min)
1	[127]	Cl_2-based Reactive Ion Etching	~150
2	[128]	BCl_3/Cl_2/Ar Inductively Coupled-Plasmas	> 400
3	[129]	NaOH	50 at (75ºC)
4	[129]	H_3PO_4	2265
5	[129]	Reported of using HF/H_2O, HF/HNO_3 and NaOH	Not Given
6	[130]	H_3PO_4 (at 160ºC)	Not Given
7	[131]	Pure AZ400K @ 23ºC	~450
8	[131]	$5H_2O$:1AZ400K @ 23ºC	~142.5
9	[132]	KOH Solution	18 for <002> 75 for <100>

Chapter 5 - Packaging the Energy Harvesters

5.1 Overview

The prototyping process of an energy harvester includes design, microfabrication, packaging, and test and characterization stages. In this work, once the fabrication process is complete, the released devices are separated from the substrate using a cleaving technique. Then, each individual device is packaged and tested separately. Separating released devices, which are very fragile, from the substrate is a challenging stage. In addition, having polymers as structural material adds more difficulties to the preparation steps of the cleaving. In this research, an improved cleaving method is developed to avoid conventional dicing and reduce the challenges of gluing the main substrate to a carrier wafer within the fabrication process. Also, a different approach was proposed to package an energy harvester together with a PCB using a conductive adhesive epoxy. In this chapter, the new cleaving technique is presented. Then, the packaging approach is demonstrated along with the required apparatus which were developed in the course of this research work. Finally, the vacuum chamber is presented and some vibration results are shown to demonstrate the effect of using the vacuum chamber.

5.2 Cleaving Technique

Each individual vibration driven energy harvester must be packaged and tested separately. The reason is: 1-to run electrical tests, a device must be packaged with a PCB and this is not feasible on wafer level; 2-each individual device has to be vibrated at a specific frequency which could be different from another device located beside it on the wafer. In addition, the devices must be installed such that they are ~2mm away from the ground to accommodate their deflection

amplitude. Hence, once the microfabrication is finished, the devices need to be separated from the wafer. This is regularly done by dicing. However in terms of fragile and overhanging devices, the cutting process in a dicing machine can easily damage the structures [133]. Some techniques such as wafer bonding [134] and stacking devices [135] have been used to overcome this problem but dicing continues to be a challenge. Although the reliability of dicing has been improved [136, 137], researchers are still seeking dicing-free techniques [138, 139] to alleviate this issue. Laser-based dicing or scribing [140, 141] is an alternative, however, it adds more fabrication steps and increase the fabrication cost.

In some cases, a diamond scriber [142-144] was used to cleave individual devices, however, it is not sufficiently accurate to separate dense devices. Alternatively, DRIE (deep reactive ion etching) which is one of the main etching techniques for releasing MEMS structures [145], has widely been used to enhance the cleaving process [146, 147]. As etching too deep causes breaking of the wafer, usually wafers are mounted on a carrier wafer [148, 149]. This mounting causes other challenges such as damaging fragile devices while removing them from the adhesive [135, 150].

In some cases, DRIE has been used on SOI (silicon on insulator) wafers to eliminate the supporting wafer [151, 152]. Apart from SOI wafers' cost, this technique works well only for limited types of materials. The long hydrofluoric acid (HF) immersion which is required for final separation, in this approach, could result in damaging or delaminating some previously fabricated layers. Another cleaving technique is a one-step backside DRIE process which was used to cleave individual devices while the boundary of the device was previously etched from the front side by a specific aspect ratio [153]. It uses different etch areas to achieve a through-hole and partial thickness "cracks". As novel as this approach is, it appears to be too specific to be used for general MEMS devices.

The modified cleaving technique used in this work is based on a single differential depth DRIE using a soft photoresist mask. This technique can be

used with any silicon wafer type including single-side-polished wafers. The technique is based on an atypical method of PR (photoresist) patterning [73]. The PR layer is exposed in two steps, both with separate masks and exposure times. This achieves two different depths of developed PR. The PR which is used to mask the etching process, would be etched under the DRIE process at a slower etch rate depending on the etch selectivity. Typically, the removal of masking PR is an unwanted byproduct of the DRIE process. In this case, this phenomenon is used to produce secondary etch windows to obtain two separate etch depths in a single etch step.

A schematic of the wafer's backside is shown in Figure 5.1. The dashed lines represent the main devices (SU-8 cantilevers in this case) on the front side of the wafer. Several widths of cleaving trenches have been examined that would help determine the optimal width and depth to provide a clean cleave and exploit minimum extra wafer area around the individual devices.

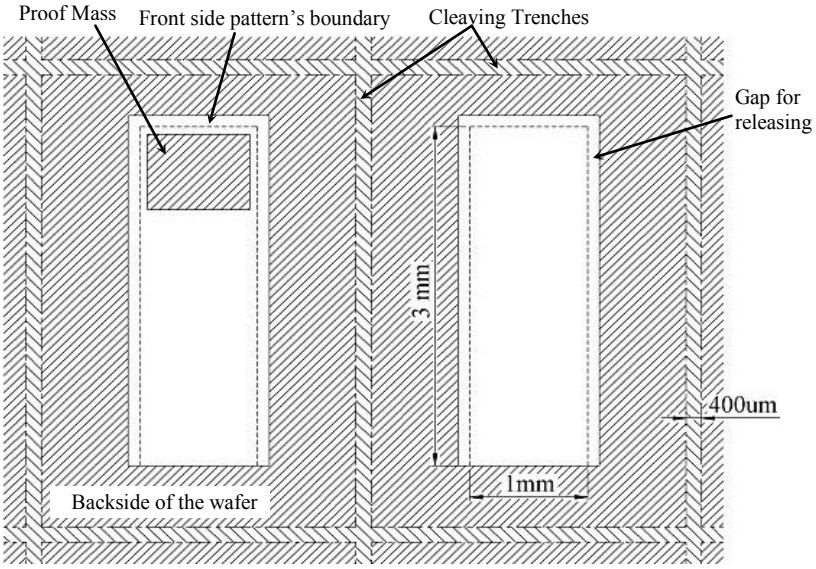


Figure 5.1 – Schematic of the backside of the wafer with cleaving trenches [154].

In the case of using a supporting wafer (also known as carrier wafer), the cleaving trenches could be designed on the same mask as the back side silicon etch. In these cases, the front side of the main wafer is glued to another bare silicon wafer until the back side silicon etch is over. Then, the two wafers are

separated. However mostly, the separation results in damaging the fabricated or released devices. The two wafers have to be glued to prevent the main wafer from cracking during the ICPRIE process due to the load applied by the wafer holding mechanism inside the etching chamber. On the other hand, the supporting wafer could be eliminated to avoid the wafer separation challenges. Figure 5.2 demonstrates a cleaving technique in which the cleaving trenches are designed on a different mask than the devices mask for back side silicon etching. This etching process is called "carrier-wafer-free DRIE" in this work.

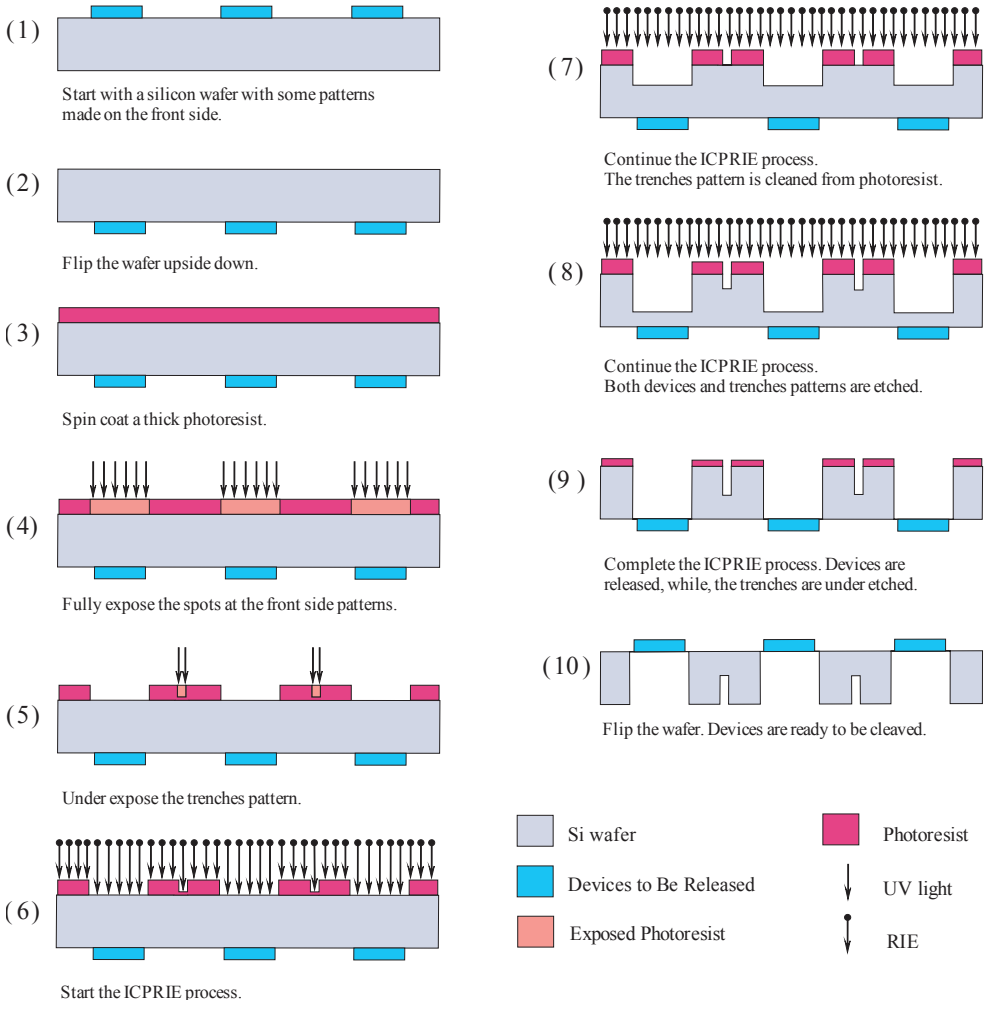


Figure 5.2 – The cleaving technique to separate individual dies while the wafer remains in one piece by the end of the fabrication process.

In the following the processes are elaborated such that the step numbers matches with the numbers in the figure.

(1) The process flow begins with a silicon wafer with previously fabricated devices (SU-8 based structures in this case) on the front side of the wafer.

(2) The front side of the wafer is covered with a photoresist and then the wafer is flipped to run processes at the back side. This helps protecting the front side features from scratches or damage.

(3) A thick layer of PR is spun-coated on the backside of the wafer. In this work, two layers of AZ4620 (providing a thickness of 24.71 μm), which is known as a thick PR, is used to mask the backside etch. The PR spin parameters are 500 rpm spread for 10 seconds and 2,000 rpm spin for 25 seconds. The wafer was then baked using a non-contact hotplate at 100°C for 90 seconds and a contact hotplate for 60 seconds. The deposited PR needs to be dehydrated for at least 2 h before the exposure.

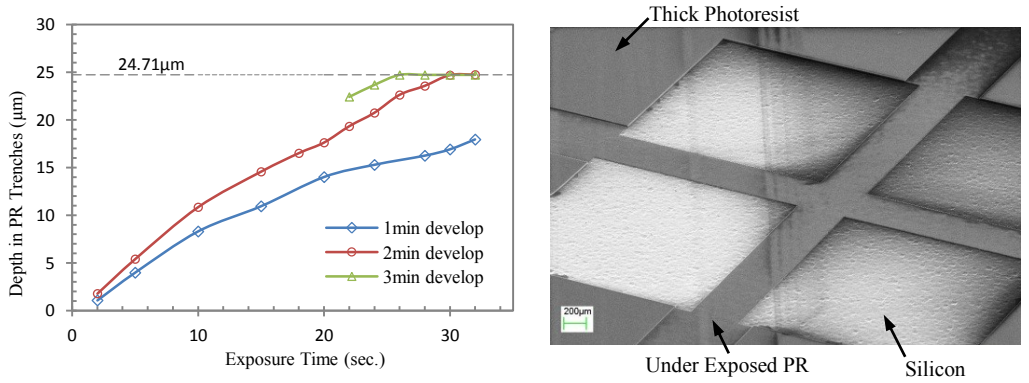
(4) The PR is then fully exposed using the first mask to open areas underneath the front side cantilevers.

(5) A second mask, containing the patterns of the cleaving trenches, is then used to partially expose the PR. Figure 5.3(a) shows the patterns depth obtained by applying different exposures (under UV exposure intensity of 11.2 mW/cm^2 at 365 nm light) and developing times. Exposure times were varied from 2 seconds to 32 seconds with the samples developed in AZ400K for 1, 2 and 3 minutes. In two cases after PR development, there were PR residues left in the trenches pattern: 30 seconds expose/2 minutes develop and 26 seconds expose/3 minutes develop. Since PR residue in etch areas may result in non-uniform silicon etching, over-exposure and over-development are recommended to ensure consistent etch in the device regions. Figure 5.3(b) shows a SEM image of an alignment mark after developing the PR on the backside of the wafer.

(6) – (8) The remaining thickness of the PR in the trenches pattern will create the desired etch delay in the next step when the wafer is etched with DRIE.

(9) The depth of the cleaving trenches depends on the thickness of the remaining PR and the selectivity of PR:Si in the DRIE process. This ensures that once the devices are totally released, the silicon wafer is still strong enough to stay as one piece (not breaking inside the RIE chamber).

(10) Once the process is complete, the photoresist is removed and the wafer is flipped. At this stage, the wafer has the required cleaving lines through which the devices could be precisely cleaved and separated from the substrate.

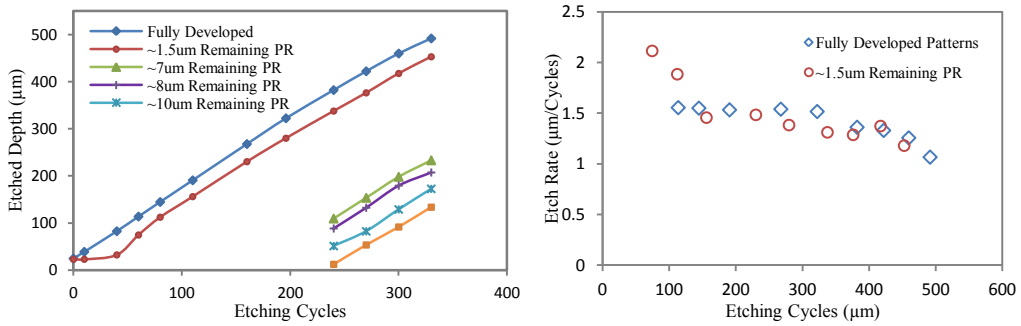


(a) (b)

Figure 5.3 – (a) Trench depth on PR vs. exposure time for different exposure times; (b) Depth differences in the PR pattern shown by an alignment mark [154].

To characterize the etching process, the photoresist on the back side of a 4" wafer was exposed under the trenches mask with various exposure and development times. The same trench sizes were compared in terms of delaying in DRIE. Figure 5.4(a) demonstrates the etched depth of fully developed trenches in comparison to the trenches with 1.5 µm-12 µm remaining PR. This graph clearly shows that by picking only one size for trenches and adjusting the thickness of the remaining PR, a proper final trench depth after DRIE could be designed for various scenarios. Figure 5.4(b) compares the etch rates of fully and partially developed trenches. It is illustrated that the etch rate decreases by going deeper in the trenches. This behavior is due to the etch rate dependency on the

pattern's aspect ratio and the depth of the etched regions. This effect is described in detail in [153, 155].



(a) (b)

Figure 5.4 – (a) Comparing trenches' depths in DRIE for fully and partially exposed/developed PR; (b) Comparison of etch rate in fully and partially developed trenches [154].

Figure 5.5 shows the cleaving steps and the capability of handling the wafer while the cleaving trenches are incorporated. Figure 5.6 demonstrates applying the cleaving technique on a 4" wafer right before cleaving. The individual devices are separated while the wafer is still in one piece and possible to be handled. Figure 5.7 shows some SEM images of the cleaved devices. It is shown that very fragile devices are separated safely. Each device has a small extra space around it as a frame which represents the minimum usage of the wafer area. Therefore, the cleaving technique allows high density mask designs which results in fabricating more devices on a single wafer. Although the cutting frame for the devices shown in Figure 5.7 is rectangular, the other configurations could be cleaved with the same technique.

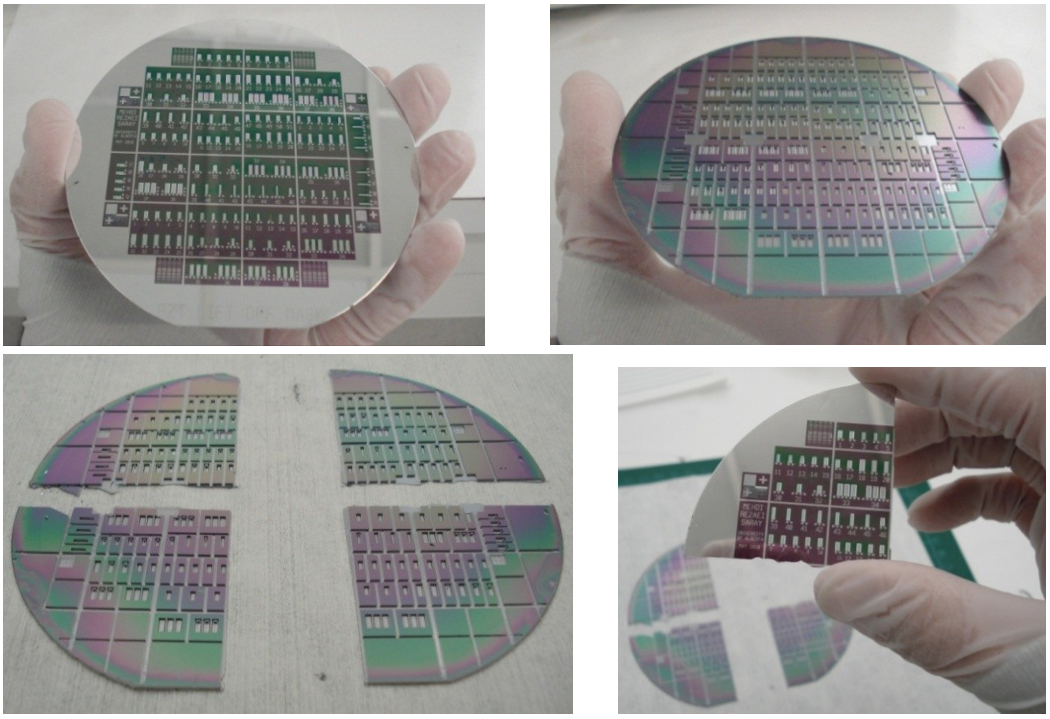


Figure 5.5 – Cleaving stages of a full wafer.

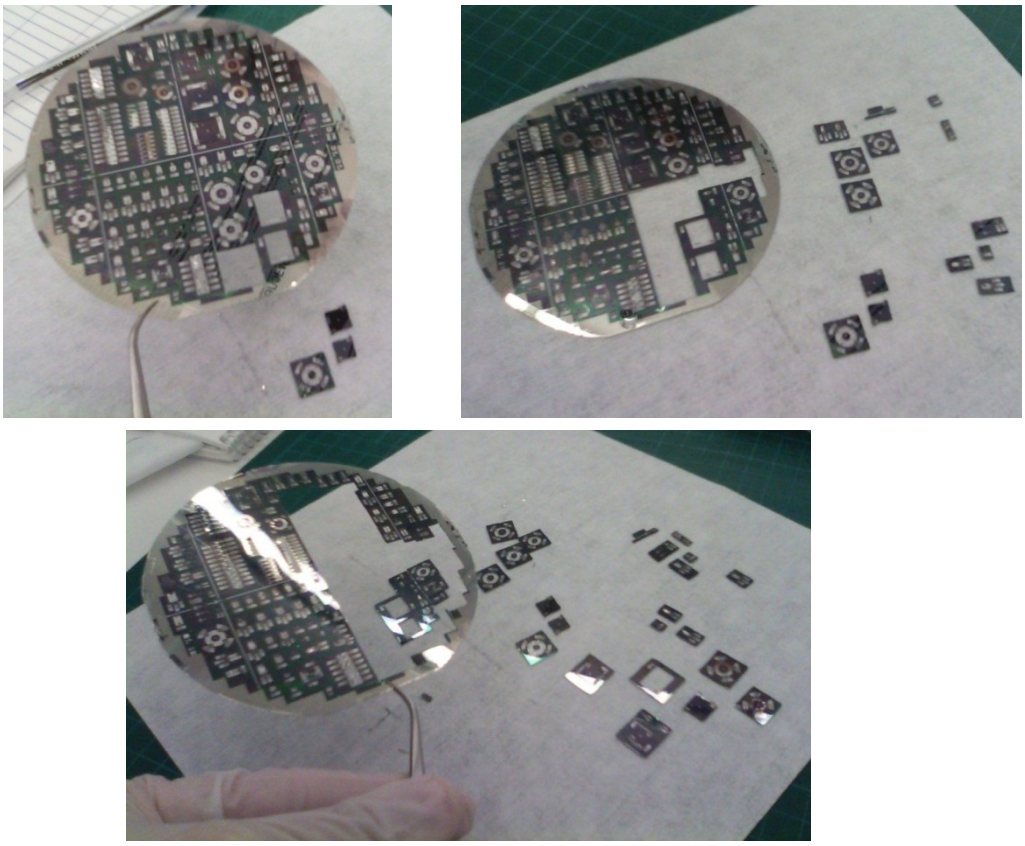


Figure 5.6 – Cleaving individual devices while the wafer is still in one piece [154].

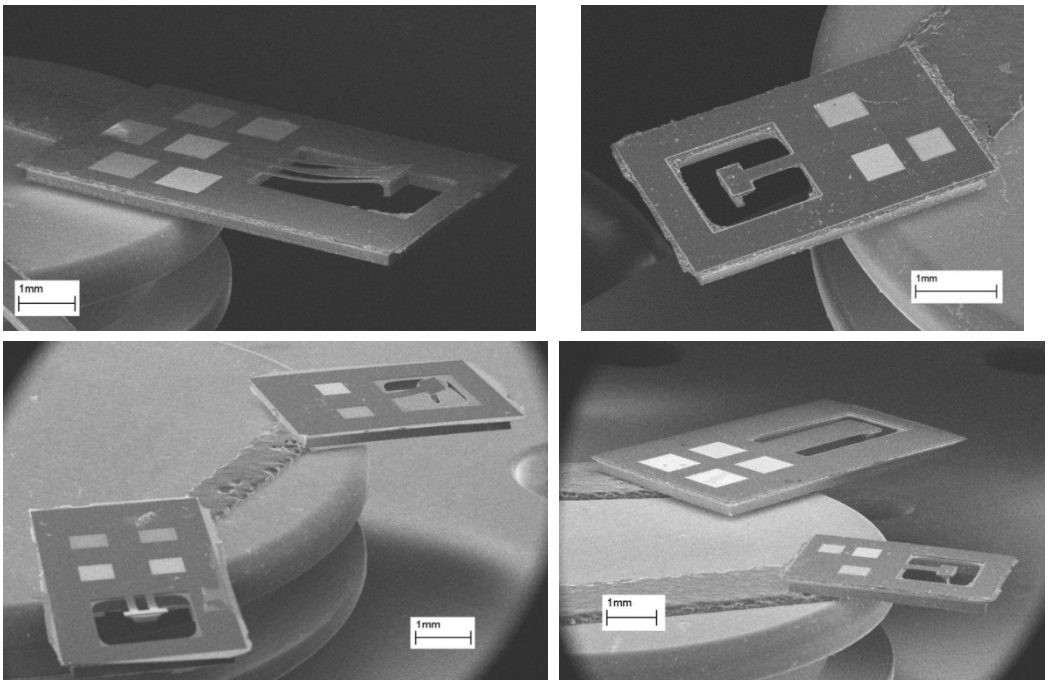


Figure 5.7 – SEM images of cleaved devices.

5.3 Packaging Approach

The packaging is considered as a vital bridge between semiconductors and printed circuit boards (PCBs) [156]. Packaging in general terms is categorized in various subsections such as biological micro-electromechanical systems (bioMEMS) packaging [157, 158], packaging of optoelectronics [159] and radio frequency (RF) devices package [160]. However, the package must satisfy multiple functions including: protection (from the surrounding environment); connectivity (electrical, material transport, radiant energy, external force); compatibility (chip-to-package, package to PCB); routing (electrical, materials); mechanical stress control; thermal management; assembly simplification; testability; and reworkability [156]. Although the packaging, testing and calibration cost (70% of the manufacturing cost [70]) is more than the microfabrication, it has gained less consideration in literature. It is known that the packaging belongs to industrial and commercial fields [92].

Packaging of micro-sensors and micro-actuators is different than general microelectronic devices [92]. In the case of microelectronics, a particular

package type can be used for various chips. The size and number of wire-bonds might change but the shape could be the same. However for MEMS devices, the package design crucially depends on the function of the device [92]. Therefore, the MEMS device and its package must be considered simultaneously to take into account each design's limitations for designing the other. Individual MEMS devices must be diced and then mounted on a package and attached to a metallic, ceramic or plastic platform. A numbers of dicing and die-attach [161] techniques have been reported. Wiring and electrical interconnections are usually the next process in packaging. Various packaging techniques have been developed based on the specific device's requirements. Microfluidic interconnections are needed for microfluidic devices such as micropumps and microvalves. Ceramic packaging, which is one of the main techniques of electrical packaging, has been extended to the MEMS packaging. Many commercial micromachined sensors use ceramic packaging which is expensive compared to other techniques [162]. However, the high reliability, interesting material properties such as electrical insulation and hermetic sealing and easy shaping keeps ceramic packaging one the main techniques in electronic packaging. Metal packaging, molded plastic packaging and multichip modules are some other MEMS packaging methods [163]. Integrated MEMS devices merge microstructures and microelectronics on a single substrate to reduce overall size, electrical noise, and system power requirements. However, there are some challenges in terms of materials and process incompatibilities and high cost [164-166]. As an alternative, hybrid packaging which has separate processes for the MEMS device and the electronics could be exploited [167].

Figure 5.8 demonstrates the path is followed in MEMS manufacturing and Figure 5.9 presents the steps taken to package the energy harvesters in this research. In each packaging, the devices are electrically checked at the first and the last steps. The probing is done before cleaving to make sure the device is electrically functional. Once the packaging is complete, due to possible defects of wire-bonding and adhesives, the functionality of the device is again checked

by a quick short-circuit test. The other stages are elaborated in the following sections.

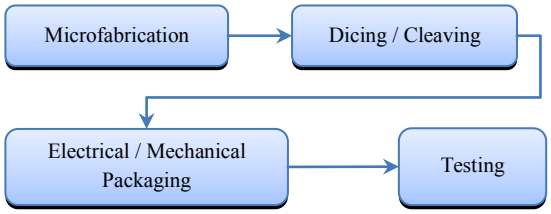


Figure 5.8– Manufacturing process steps for MEMS devices.

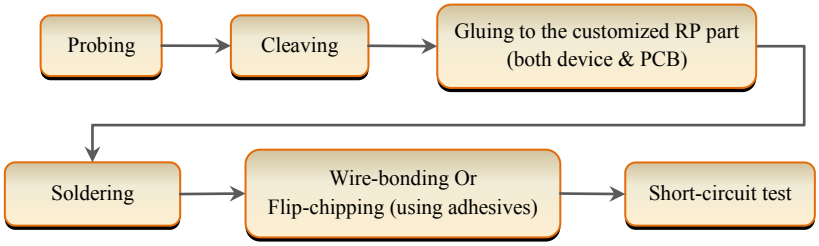


Figure 5.9 – Packaging steps for energy harvesters in this work.

5.3.1 Wire-bonding

Wire-bonding for MEMS is a fairly standard packaging technique. It is known as the most widely used interconnection technique to electrically connect a MEMS die to the package. Typically, gold and aluminum wires are used in wire-bonding but silver and copper wires are also reported [168]. Bonding of gold wire seems to be easier than bonding aluminum wires. However, it is difficult to find gold wires above 50µm diameter, whereas, aluminum wires are available up to 560µm in diameter which makes them the only solution for high current applications [163]. In addition, wire-bonding seems to be problematic for RF applications. The resistance of thin wires and bonds could result in significant losses and, depending on the wires' lengths, some parasitic inductance might be added to the system [169]. Soft platforms for the die is a source of challenge for wire-bonding and typically needs coupling of ultrasonic energy of the capillary into the bonding region [92]. Reliable wire-bonds are essential for the electrical functionality of the package. In operational point of view, achieving a reliable

bond is challenging. Purity and contamination-free wire, optimizing capillary feed, clean operation, optimized process parameters such as temperature, pressure, and ultrasonic energy must be considered to achieve a reliable bond [168].

In some cases, especially for resonators, the MEMS device(s) and PCBs have to be mounted on a structure [26, 36, 170-172]. The structure could be as simple as Figure 5.10 where two PMMA[18] sheets are cut by laser and glued such that there is enough space for the cantilever's proof mass to vibrate. However due to mass production and reliability issues, a more robust method must be chosen. In this work, 3D printing is proposed as an alternative.

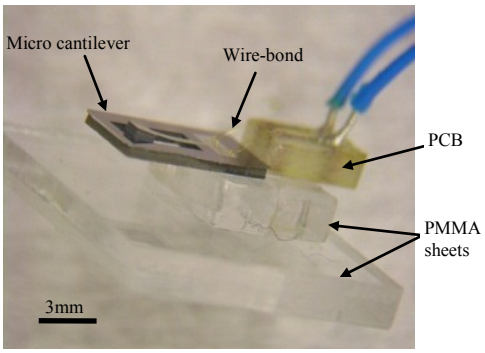


Figure 5.10 – A simple structure to hold the device and PCB and provide some space for cantilever's oscillation.

Lately, MEMS inertial sensors are in transition from fully hermetic ceramic to plastic packaging that helps meet their price margins [156]. Therefore, the plastic packaging could be considered as an alternative for MEMS devices. 3D printing is used in this work to package both micro energy harvester and the PCB as one structure. 3D printing is a cheap and quick manufacturing technique to build such tiny structures and customize them for special shapes and designs. In addition, researchers have recently developed, and are still working on, developing biocompatible materials to be used for 3D printing machineries [173-177]. These materials could also be exploited to make packaging structures for covering energy harvesters from its environment for use with biological systems.

[18] Polymethylmethacrylate (Acrilic)

3D printing could also be used for the prototyping stage to keep the costs down. Figure 5.11 demonstrates customizing a structure design to mechanically support both a MEMS device and a tiny PCB. Wire-bonding and soldering was used to make electrical connections. The 3D printed part was designed such that it could be clamped to a shaker table (Figure 5.12). To make the 3D printing parts, an Eden 350V from Object was used with high resolution layers of 16µm in Z axis, accuracy of 0.1–0.3 mm and with glossy quality.

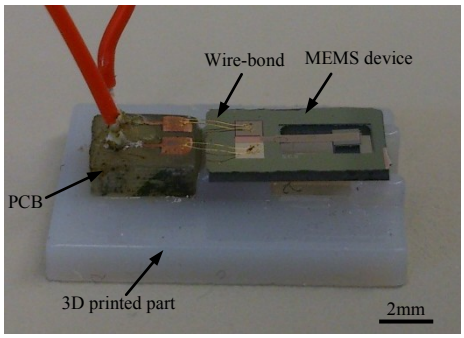


Figure 5.11–3D printed part is customized as a mechanical support for a resonator.

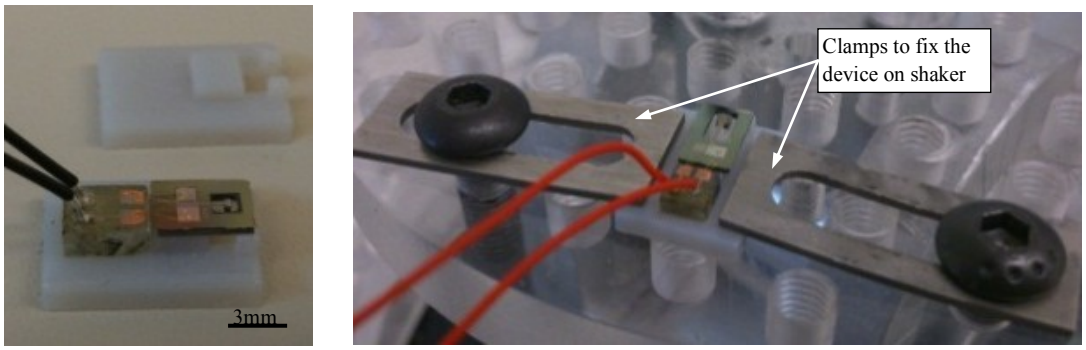
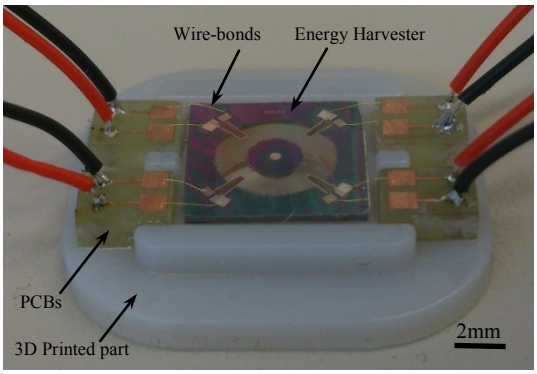
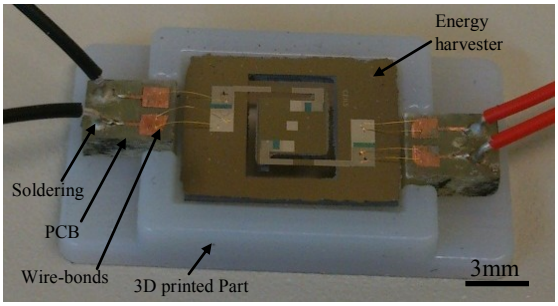


Figure 5.12–An example of 3D printed part for a 1mm long cantilever. All packaging structures are designed to be clamped to a shaker table.

Figure 5.13 shows the packaging for the two main energy harvesters considered for this research. Due to having multiple harvesting elements for these devices, multiple PCBs are placed around the device. All PCBs are designed at the same size and shape to match with all structural configurations of the designed energy harvesters. The PCBs were ordered in large sizes and then cut into $2 \times 3mm^2$ size.



(a)



(b)

Figure 5.13 – (a) A fully packaged membrane energy harvester, (b) a fully packaged MicroChip energy harvester.

3D printing could also be considered for sealed box packages to completely protect the device from its environment (Figure 5.14). Various adhesives or laser sealing which are used to seal plastic packages [156] could be exploited to seal the lid to the bottom of a 3D printed structure. MEMS ink-jet chip packaging, capping process and thermoplastic injection molding are some of the other methods to build a structure to protect the chip from its environment. However, none of them is as fast, cheap and customizable as the 3D printing process.

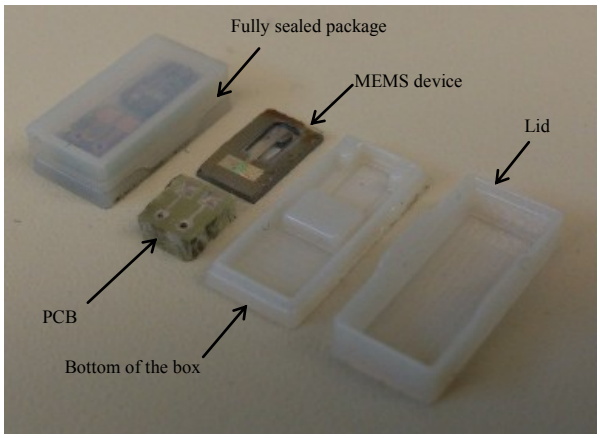


Figure 5.14 – A sealed box was manufactured by 3D printing.

5.3.2 Conductive Adhesive Technique

Adhesives could be used for various purposes such as thermal conduction, electrical conduction, reduce parasitic capacitance between traces and leads, underfill process for flip-chip, and gluing and encapsulating chip on board [178]. In this section, the focus is on dispensing electrically conductive adhesives. Through silicon via (TSV) is a vertical interconnection through the thickness of a silicon substrate enabling electrical conductivity between components on top and bottom of the substrate. A variety of TSV designs has been reported [179-183]. All designs consist of a through hole in the substrate, an insulating layer which prevents current leakage to bulk silicon, metal layers on both sides for the traces or pads, and conductive materials filled in the void. A number of materials have been investigated as conductive fillings such as electroplated copper [184], polysilicon [185, 186], conductive adhesive [187, 188], tungsten [189], and even wire-bonds to lower the capacitance of the coupling [190]. However in this work, the conductive adhesives have been exploited to provide electrical connection between a device's pad and a PCB's pad. In this case, the device is flip-chipped on a PCB while adhesives are previously dispensed on one of their pads.

5.3.2.1 Using syringes setup

There are a variety of automatic dispensing tools. For instance, Finetech GmbH & Co. provides submicron die positioning and also offers dispensing of various materials such as optical, thermal, isotropic, and anisotropic conductive adhesives. They also provide rework services for preassembled dies by removing and re-dispensing solder paste. However, automatic dispensing equipment is costly and possibly not available for all researchers to use. Alternatively, manual dispensers are used. The main challenge with manual dispensers is accuracy in positioning due to shaking of the hand. In this work, an adapter was designed to hold a dispensing syringe and be installable on a micropositioner which is capable of positioning in three axes within one micrometer accuracy. A micropositioner from Quarter Research and Development (Model XYZ 500 TIS) and a dispensing system from Nordson EFD (Ultimus II) were used in this case. Figure 5.15 demonstrates the adaptor. Figure 5.16 shows the orientation of the needle and also the ability to place adhesive dots in the middle of tiny pads. The tip of the syringe needs to be oriented in the same orientation as the hole to enhance the filling of the TSV. But, using a straight needle as syringe's tip blocks the microscope view. Therefore, instead of straight needles, angled ones (45°) were used and the 3D printed adaptor was designed such that the syringe was oriented 45° to the surface. Consequently, the tip of the needle is perpendicular to the surface and neither syringe nor the adaptor blocks the user's view.

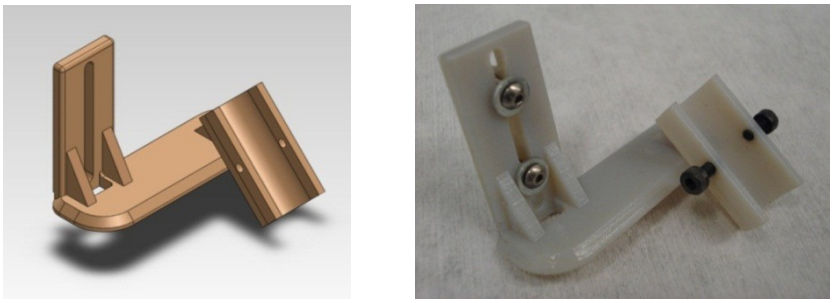


Figure 5.15 – The designed and manufactured adaptor for a micro-positioner.

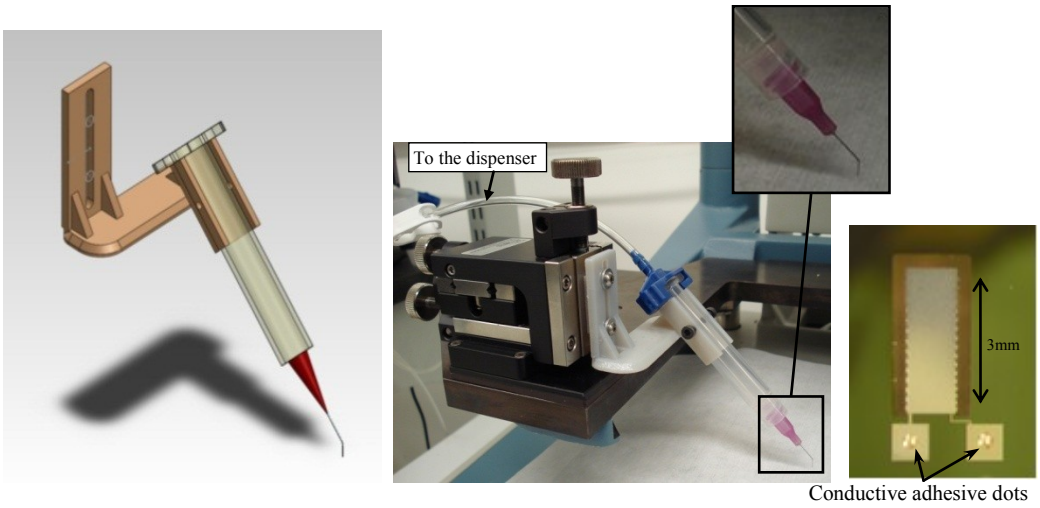


Figure 5.16 – The designed and implemented syringe holding mechanism for precise adhesive dispensing developed to replace manual dispensing.

5.3.2.2 Flip-Chip Bonding

Flip-chip or direct chip attach (DCA) is a low volume, 3D vertical integration scheme that allows for direct connection between PCB and the die (top-face-down). Capped devices could easily be made by a flip-chipper. DCA provides a number of joining systems from conventional metallic solders to low-temperature conductive polymers. DCA has four subdivisions: device, bumps, joining material, and under-fill [156]. There is usually a relatively small gap (50–200μm) between the die and the packaging substrate [163]. Therefore, the parasitic inductance and capacitance for each interconnection is minimized due to minimum transmission line length which makes flip-chipping a better packaging technique than wire-bonding for RF applications [169]. In addition, unlike wire-bonding which requires bond pads away from die to prevent wires from crossing, flip-chip involves placing bond pads on top of the die resulting in significant increase in input/output connection density [163]. Flip-chip is attractive for MEMS industry due to providing the capability of packaging a number of dies in a single package substrate with multi-level electrical traces (hybrid packaging). Wire-bonding could also be used to build a similar system, however, not only will its area usage not be as efficient, but also its reliability

will be doubtful due to too many wires in the package. One of the disadvantages of flip-chipping is that it is not compatible with released microstructures. For instance, a MEMS device with a thin diaphragm could be damaged during the flip-chip process [163].

Figure 5.17 demonstrates packaging resonators to flexible PCBs with the flip-chip technique. Conductive adhesive dots are placed on the device's pads (using the technique shown in Figure 5.16) and then the flexible or conventional PCB's pads are flip-chipped on them. Figure 5.18 shows a membrane energy harvester flip-chipped on four solid PCBs and also two cantilevers are shown which are flip-chipped on the solid PCBs. Flexible PCBs (FPCBs) are soft and could be cut by scissors. Pads and traces could be designed very close (3µm width, 5µm gap). However, the process is expensive for prototyping. In comparison although solid PCBs are much cheaper, they need a tool to be diced and do not have as high resolution as FPCBs.

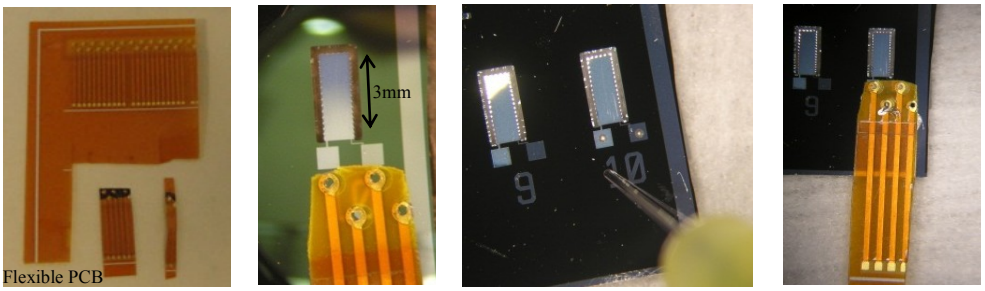
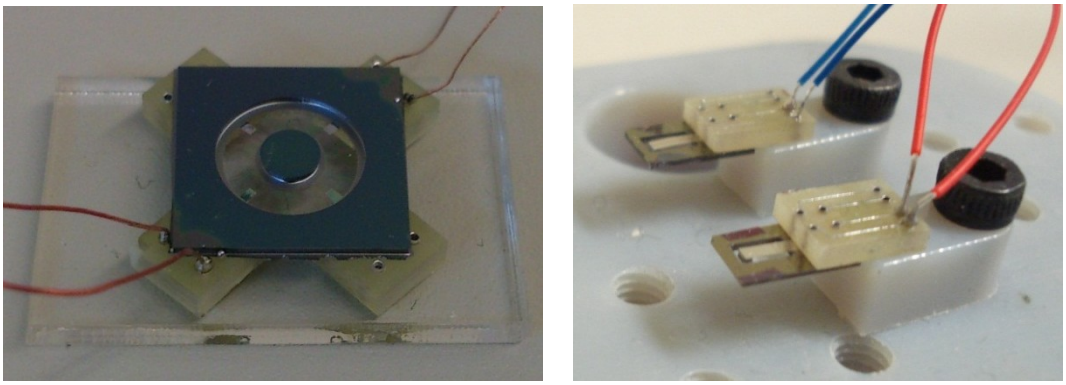


Figure 5.17 – Using flexible PCBs to flip-chip on conductive adhesives.



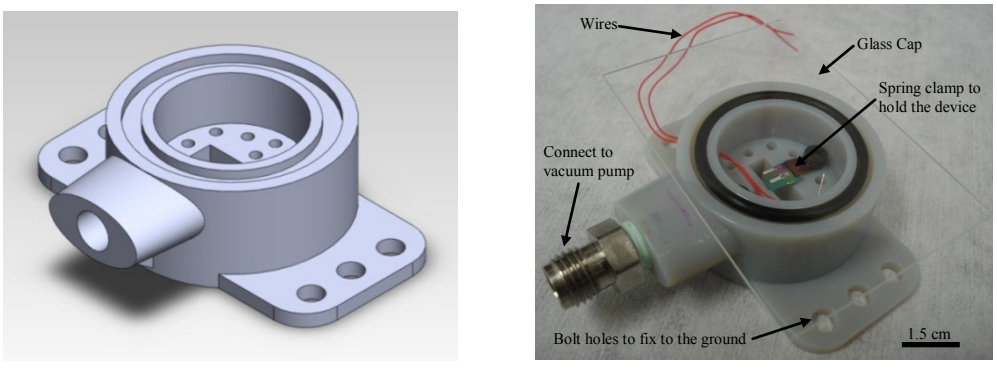
(a) (b)

Figure 5.18 – Flip-chipping is used to package resonators to the conventional PCBs.

5.4 Vacuum Chamber

Testing under vacuum would decrease the air damping effect and consequently increase the quality factor of a resonator. In the case of an energy harvester, a device under vacuum would have higher vibration amplitudes which in turn causes higher output energy for a given excitation amplitude. Researchers would always prefer to package their devices under vacuum to improve the output results [191-194]. Various techniques have been developed for chip-level and wafer-level vacuum packaging of MEMS devices [195-201]. However, before pursuing a vacuum packaging process, one would like to test and characterize the fabricated MEMS device under vacuum. Considering the low yield of any packaging technique in general, it would be beneficial to test a device under vacuum before it is fully packaged.

Figure 5.19 shows the small vacuum chamber which was designed using SolidWorks and then was built in the Department of Mechanical Engineering machine-shop (Meceshop) using the rapid prototyping (3D printing) technique. The chamber includes a glass slide to allow laser go through and be focused on the energy harvester, an o-ring to seal the chamber from the top, a tube fitting to connect the chamber to a vacuum pump, two wires to provide electrical connection between inside and outside of the chamber, and a few clamps to fix the devices inside the chamber. In addition, some holders were designed to easily install and remove the devices inside the vacuum chamber (Figure 5.20).



(a) (b)

Figure 5.19 – Vacuum Chamber: (a) was designed in SolidWorks and (b) as built using the 3D printing technique.

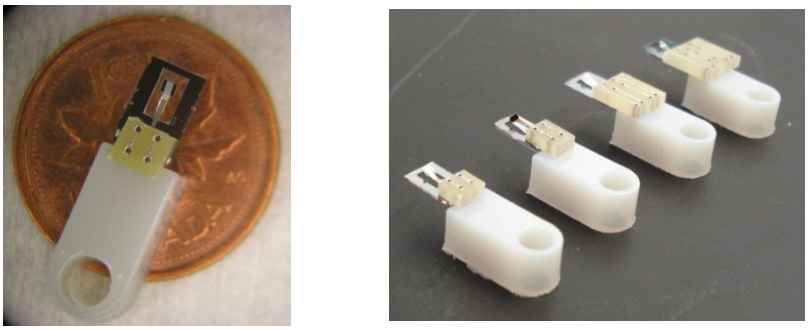


Figure 5.20 – A sample holder was designed to fix the packaged devices inside the vacuum chamber.

The vacuum pump (from Fisher Scientific) was able to provide a pressure of 1×10-4 Torr. Testing under vacuum caused decreasing the air friction and consequently increasing the amplitude of the vibrating devices. Figure 5.21 demonstrates the effect of using vacuum to minimize the air friction on vibrating devices. Red graph shows the amplitude of a cantilever under vacuum and the blue line is the amplitude of the same device in air.

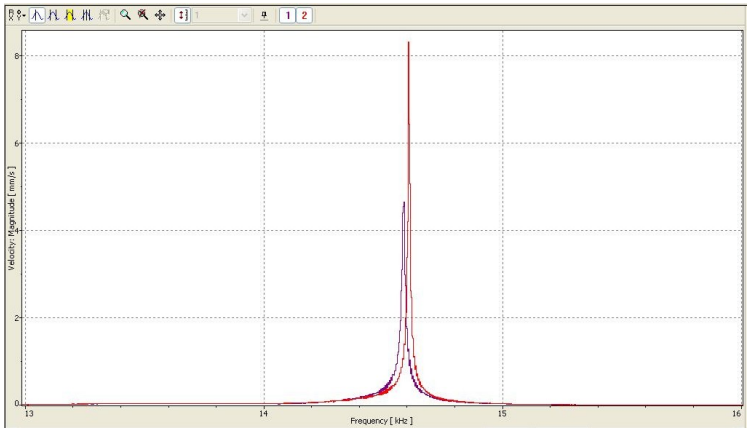


Figure 5.21 – Effect of minimizing air friction on the amplitude of the vibration.

5.5 Summary

In this chapter, various packaging techniques presented which were developed over the course of this research work. In this section, the main packaging methods are summarized. The carrier-wafer-free cleaving technique (elaborated in Section 5.2) and a carrier-wafer-based (without gluing) technique (explained

in Section 4.2.2, Step (10)) are the two main cleaving techniques exploited for cleaving devices. The wire-bonding (shown in Figure 5.13) and flip-chipping (shown in Figure 5.18) techniques are the two main electrical interconnection methods used between devices and tiny solid PCBs. Finally, 3D printing is exploited to build customized packaging structures to mount devices and PCBs on them.

In terms of industrial mass production, the scalability of the fabrication process flow presented in Chapter 4 and the packaging procedure presented in Chapter 5 could be examined in two ways. On one side, characterization of each fabrication stage could be easier due to using a specific machine with known parameters to produce a particular device, whereas in the university lab, one must use publically available tools which are used by numerous people for various processes each of which could contaminate the tool and change the previous parameters. However on the other side, the yield of the fabrication and more importantly the packaging must be investigated for mass production. Each step in this research was developed aiming to improve the overall yield of the process. Various alternatives in fabrication stage were investigated such that in final fabrication runs, all devices were successfully released except one or two devices on the edges of the wafer. In terms of packaging, the developed cleaving technique helped to eliminate damages due to using dicing or other forms of cleaving. Finally, the 3D printing structures to secure the devices, significantly improved the overall yield such that after using this technique there was no device loss in testing stage. With regard to the scalability, similar concepts could be used with some modifications or they can be replaced by industrially available techniques.

Chapter 6 - Testing and Results

6.1 Overview

In this chapter, two testing procedures are demonstrated: Vibration Tests and Electrical Output Measurements. The objective of the vibration test is to determine the natural frequency of a fabricated energy harvester. Once the electrical interconnection packaging is performed between an energy harvester and a PCB, the electrical test could be conducted. The electrical test is required to determine the output voltage and power of a fabricated energy harvester. In this chapter, the adopted testing approaches are presented in detail including exploited apparatus. The final results for the designs presented in Chapter 3 are depicted in terms of frequency spectrum, open circuit voltage, internal impedance, output power.

6.2 Testing approaches

6.2.1 Vibration Tests

The output power of an energy harvester directly depends on the amplitude of the vibrations because the larger amplitudes in vibration cause larger strains on piezoelectric layer. The largest vibration amplitude happens at resonant frequency. Therefore, determining the natural frequency/frequencies of an energy harvester is critical.

A Polytec Laser Doppler Vibrometer (LDV) was used to measure the vibration amplitude of the energy harvesters and provide a frequency spectrum by taking Fast Fourier Transform (FFT) of the data. Peaks in FFT graph represent the resonant frequency of each device. Each fabricated and packaged energy harvester needs to be fixed on a shaker table which is mounted under the LDV's

laser head. The laser must be focused on a proper spot of the device (e.g. on the proof mass in case of having a cantilever), before starting the test. Figure 6.1 demonstrates a schematic of the LDV, shaker and a device which is mounted on the shaker table. Conceptually, LDV works based on Doppler effect. The incident signal from the laser head reflects from the vibrating surface and the velocity measurement could be performed. The built-in software in the LDV allows measuring displacement and acceleration as wee. Figure 6.1 demonstrates a sample sinusoidal signal which is applied to the shaker. The amplitude of the input signal is fixed, but its frequency sweeps within a range. The LDV measurements allow comparing the amplitude of the vibration in a frequency spectrum. Therefore, peaks represent the natural frequencies of the vibrating energy harvester. A sample output signals in both time and frequency domains are also shown in Figure 6.1.

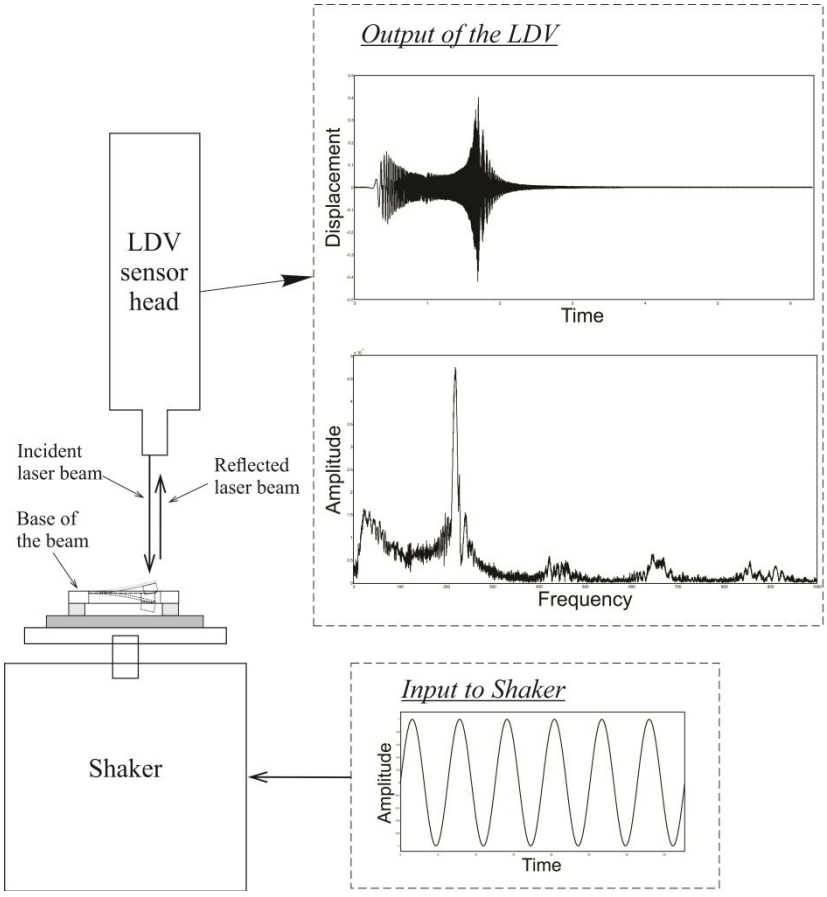


Figure 6.1 – A schematic of the vibration test using LDV. Examples of input and output signals are also presented.

For each device, at least two vibration tests must be conducted to find the right location of the peaks in the frequency spectrum. In the first test, the laser is shined to a spot on the vibrating device where its amplitude is needed. For the second test, the laser is shined to a fixed spot on the device or to the shaker table. Filtering the first signal from the second signal eliminates the base excitation signal and some of the noises involved in both signals. Figure 6.2 shows the signals of the base and tip of a cantilever. It is shown that the base excitation has an effect on the amplitude of the cantilever tip. Therefore, the base excitation signal must be filtered out of the tip signal.

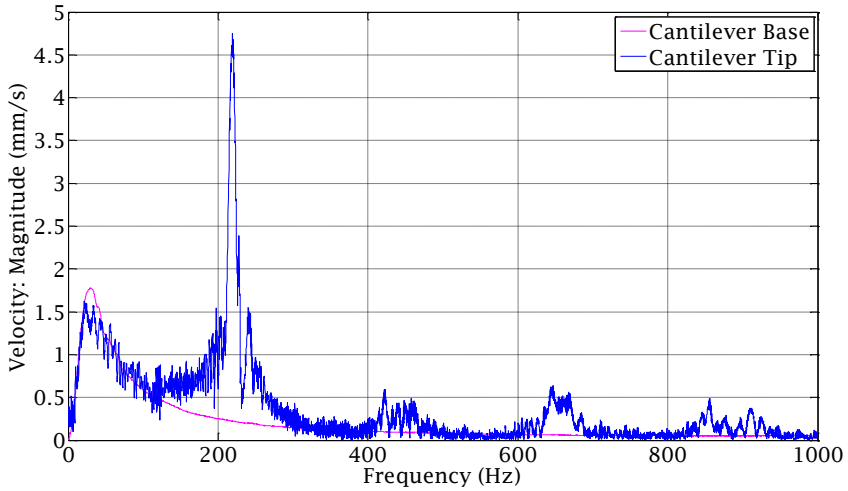


Figure 6.2–A sample LDV results in frequency domain. The base excitation signal must be filtered out of the tip signal.

The built-in software in LDV allows measuring the Q-factor of the vibrating devices. Once the frequency spectrum is obtained and the base excitation vibration is filtered out, Q-factor can be measured out of the main peak as shown in Figure 6.3. The tool is using the following equation as given in [202]:

$$Q = \frac{\omega_n}{\omega_2 - \omega_1} \tag{6.1}$$

where ω_n is the natural frequency and ω_1 and ω_2 are the two frequencies equally located on both sides of ω_n and -3dB lower than the peak. Now that the Q-factor is obtained, the damping ratio can be estimated using equation (6.2).

$$\zeta = \frac{1}{2Q} \tag{6.2}$$

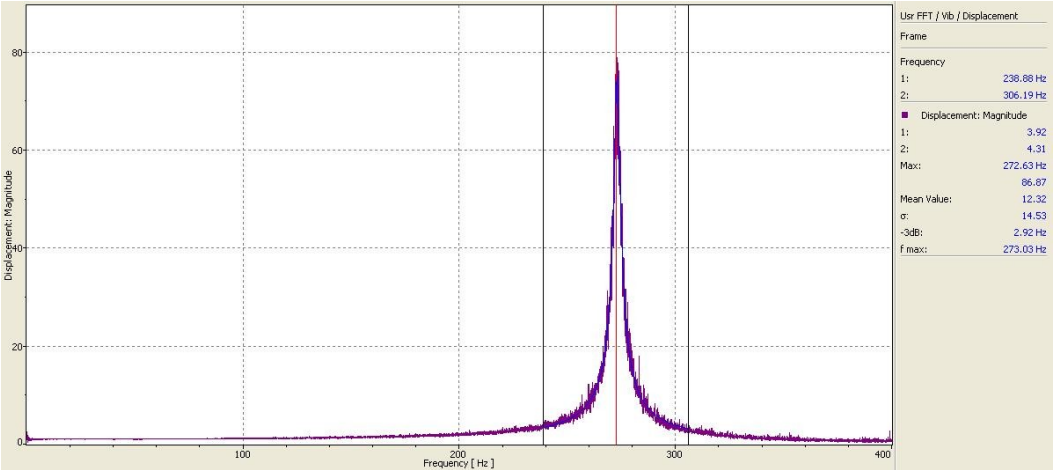


Figure 6.3 – Determining the maximum frequency of the peak and the value of -3dB lower than the peak using LDV software to estimate the Q-factor.

6.2.2 Electrical Output Measurements

One of the characteristics of linear vibration based energy harvesters is that their output voltage is maximum at their resonant frequency and if the base excitation frequency is not close to the device's resonant frequency, the output voltages drops dramatically to some value close to zero. Since the output voltage of the energy harvester is directly proportional to the amplitude of the excitation signal, special attention must be paid to adjusting the excitation amplitude. A very small excitation amplitude will result in very low output voltage and a very large excitation amplitude can break the energy harvester's structure because the structure is vibrating at its resonant frequency.

The excitation signal is generated by an Agilent Signal Generator and using an Agilent Power amplifier the signal is amplified and then fed into a Bruel & Kjaer Type 4809 shaker table (Figure 6.4). A packaged energy harvester has two wires one end of each is connected to the devices pads. The other end of these two wires is connected to an Agilent Oscilloscope to measure the output voltage of the energy harvester. This will show the open circuit voltage ($V_{o.c.}$) of the energy

harvester. However, to measure the output power of each energy harvester, a proper resistance must be added in the loop. A decade box is connected in parallel to energy harvester and oscilloscope. Therefore, one can vary the resistance quite easily and measure the voltage on two ends of the resistor. In future as a final prototype, a printed circuit board (PCB) could be used to place the electrical components next to the energy harvester.

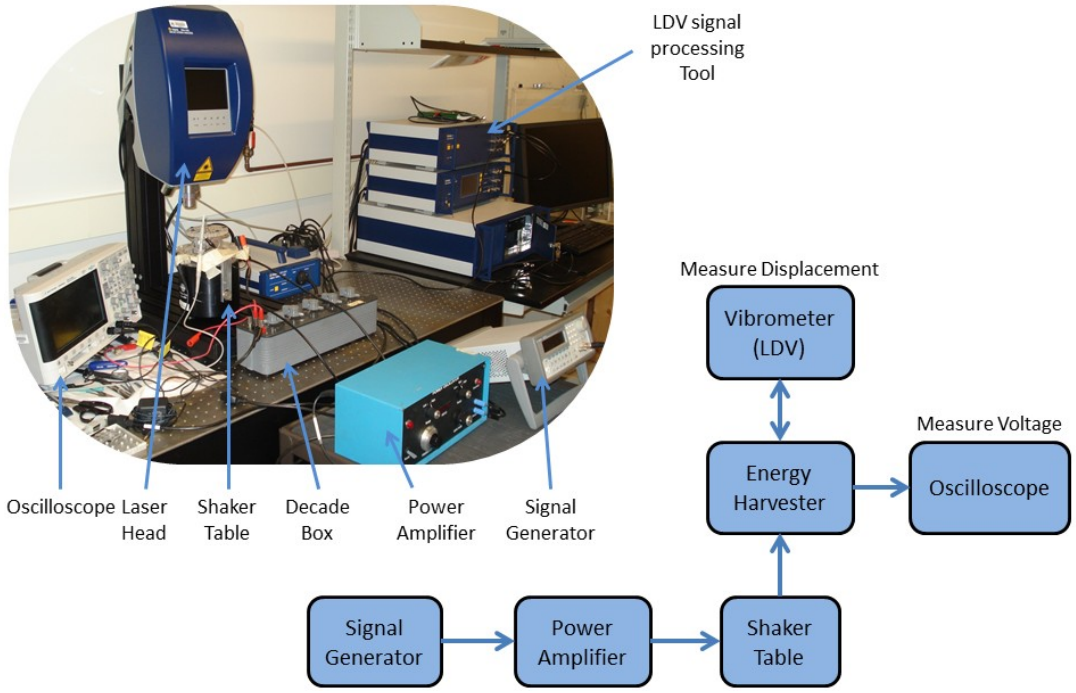


Figure 6.4 – Electrical and Mechanical Tests Setup.

The output power of the energy harvester depends of the terminal load resistance. As shown in Figure 2.1, the output power increases by increasing the load resistance until it reaches its maximum value where the power starts to decline by further increasing load resistance. The corresponding load resistance value is called optimum load. The optimum load resistance can be calculated as following [26]:

$$R_{opt} = \frac{1}{2\pi f_n C} \tag{6.3}$$

where f_n is the natural frequency in Hertz and C is the internal capacitance of the energy harvester. C can be either found from equation (6.4) or measured directly from the harvester using a regular multimeter.

$$C = \frac{\varepsilon_0 \varepsilon_r w_e l_e}{t_p} \tag{6.4}$$

where ε_0 and ε_r are vacuum and relative permittivity, w_e, l_e are width and length of the electrodes, and t_p is the thickness of the piezoelectric layer. To calculate the maximum output power, $V_{rms} = V_{pk} / \sqrt{2}$ is needed to be measured and used in:

$$P_{\max} = \frac{V_{rms}^2}{R_{opt}} \tag{6.5}$$

where V_{rms} and V_{pk} are the RMS and peak voltage measured at the load terminal, respectively. As shown in Figure 6.4, it is also possible to measure the deflection amplitude of the harvester at the same time the electrical measurement is taking place. For this reading using the LDV, it is recommended to use a velocity decoder and capture the signal in FFT mode. Based on Polytec recommendations, the "flat top" window in the built-in software must be exploited for such sinusoidal signals to obtain the most accurate results.

6.3 Results and Discussion

As elaborated previously, various structural configurations of energy harvesters have been designed and fabricated in this research. These configurations are either silicon-based or polymer-based. This section presents and discusses the results of each structural configuration.

6.3.1 Verification and Validation

The masks layout is presented in Figure A.16 (Appendix-B). It is shown that various cantilever configurations were fabricated along with the membrane and micro-chip designs. The simple cantilever designs allowed characterizing the

fabrication steps and also validate the results of the fabricated devices with the simulation. In the following the frequency and electrical output characterization on the cantilever designs are elaborated.

6.3.1.1 Frequency Response Characterization

One of the main concerns of fabricating a number of a particular harvester on a wafer is controlling their natural frequencies. The non-uniformity of the backside deep silicon etching results in obtaining different thicknesses for the cantilevers across the wafer. It is usually difficult to control the etching depth across the wafer, therefore, one cantilever would be over-etched while the other one is under-etched. Different thicknesses for two identical geometry cantilevers results in different resonant frequencies. Various reasons could cause this defect such as helium leak, cleanliness issues inside the chamber and sealing, non-uniformity of cooling the wafer. Properly clamping the wafer in the RIE etching chamber to reduce the helium leak would decrease the etching non-uniformity. However, it seems that imperfect uniformity of the deep etch due to its long process is inevitable. Slight thickness differences of two similar devices located at two different spots of the wafer results in two different natural frequencies.

A silicon-on-insulator (SOI) wafer with 20µm device wafer, 1µm oxide layer, and 500µm handle wafer is used to control the thickness of the devices over the wafer and characterize the microfabrication defects. The defects of the backside silicon etching are the major ones which were investigated and considered in the simulations. Figure 6.5 shows the scanning electron microscopy (SEM) images of the backside of the fabricated micro-cantilevers. The undercut in the proof masses is clear in all the images. One might also notice the negative sidewalls on the proof masses and smaller area of the masses than their base which reveal the undercut due to backside etching. The undercut reduces the mass and consequently increases the natural frequency of a cantilever away from its designed value. As shown in Figure 6.5, the undercut at the base of the proof masses is larger than the other sides. The reason is the wider opening of the base than the sides of the mass for the backside etching. Three different

configurations of cantilevers with different size proof masses have been depicted to show the etching defects. The etching residues due to any cleanliness issues at the previous stages such as lithography and wet etching as well as handling issues during RIE process or non-cleanliness of the RIE chamber are shown. These residues could potentially affect the performance of the devices. For instance, the residue at the clamped end of the cantilever shown in below-right corner of Figure 6.5 could effect on the oscillation of the cantilever.

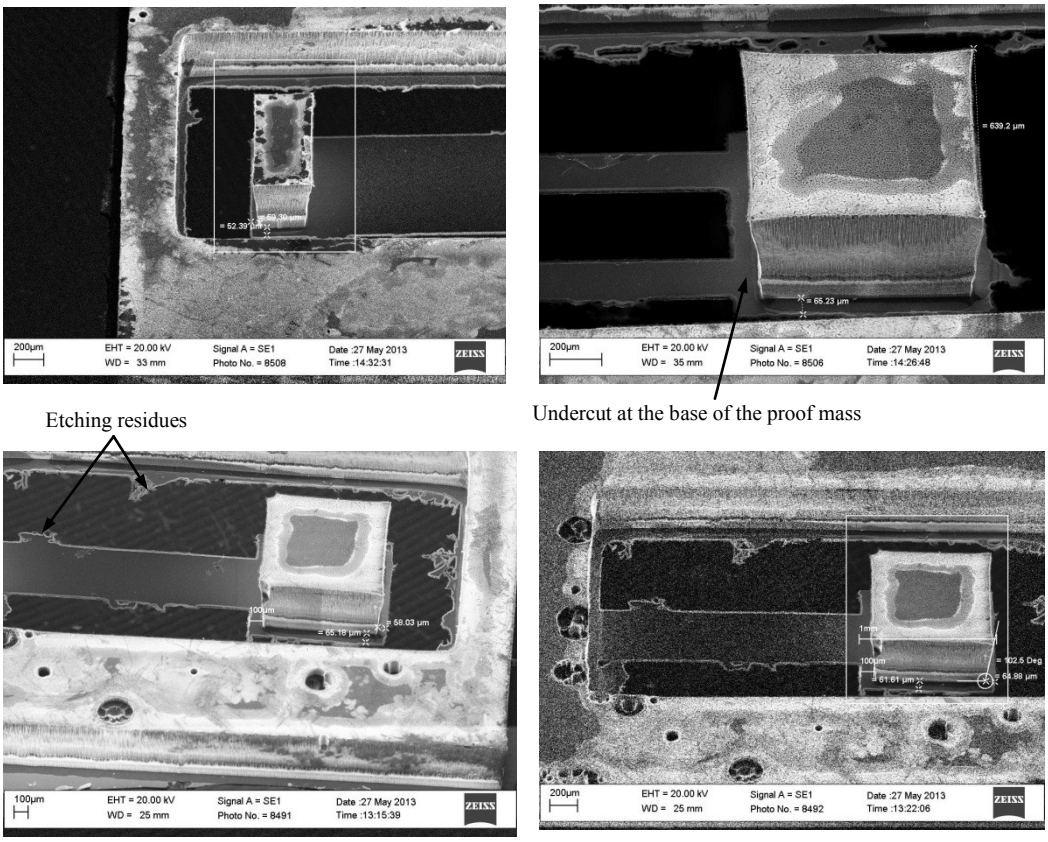


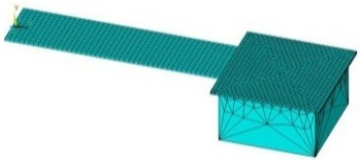
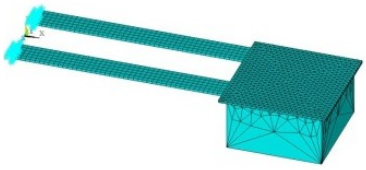
Figure 6.5 – SEM images of the backside of the fabricated cantilevers.

A set of modal analyses is performed using ANSYS for three different cantilever configurations. The undercuts are measured in SEM images and an average of the undercuts is applied to the FEM models. A uniform undercut of 60µm all around the proof mass is considered for the first set of simulations. In addition, it was noticed that in most of the devices, the base of the proof mass has more undercut due to a bigger open area to be etched from the backside. ~100µm of undercut was measured at that base of the proof masses. Both of these settings

were used in the simulations which are tabulated in Table 6.1. The first configuration is a $3 \times 1\, mm^2$ which includes a $0.5 \times 0.5\, mm^2$ of proof mass. Ten of this size cantilevers existed on the fabricated wafer and the natural frequencies were measure by a laser based vibrometer. The values are 908.8, 950, 953.8, 956.3, 967.5, 975, 981.9, 1025.6, 1062.5, 1083.8 Hz. The average is 986.52 Hz. The second configuration is a $2 \times 0.5\, mm^2$ plus a $1 \times 1\, mm^2$ proof mass in the length. Three of this size of cantilever existed on the fabricated wafer and the natural frequencies are 541.3, 543.8, 560 Hz. The average is 548.37 Hz. Finally, the third configuration is two $2 \times 0.2\, mm^2$ beams plus a $1 \times 1\, mm^2$ proof mass. Five of this size of cantilever existed on the fabricated wafer and the natural frequencies are 490.6, 497.5, 498.1, 508.1, 537.5 Hz. The average is 506.36 Hz. In the case of the second and third designs, the uniform undercut was not able to predict the resonant frequency as good as considering larger undercut at the base. Whereas in the case of the first design, the uniform undercut assumption worked better. The reason could be the larger proof mass at the last two designs which makes the proof mass more susceptible for the undercut and alteration to the resonant frequency. The larger the proof mass, the larger the area to be cut around it, and the bigger the error could happen in considering experimental defects for the simulation.

Table 6.1 – Experimentally measured and simulation results of the natural frequency of the various cantilever configurations.

No.	Cantilever Configuration	Experiment (average)	Simulation (uniform undercut)	Simulation (more undercut in base)
1		986.52 Hz	988.37 Hz	1026.3 Hz

2		548.37 Hz	543.04 Hz	549.04 Hz
3		506.36 Hz	497.33 Hz	502.99 Hz

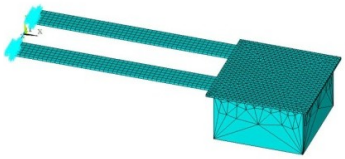
6.3.1.2 Voltage Output Characterization

The first and third configurations of the cantilevers which are representing uniform and split beams are considered for a comparison between the experimental measurements and simulation results of the electrical output of the harvesters. The finite element simulation settings are provided in Section 3.4.2 for coupled field analyses. Table 6.2 and Table 6.3 presents the comparison. In both cases, the Aluminum Nitride layer completely covers the top surface of the beams. The experimental displacement values were measured using a laser based vibrometer while the laser point is shined to the tip of the cantilever. The experimental open circuit voltage values were measured using an oscilloscope. In the case of simulation, the applied load is a static displacement of the tip of the cantilever and the voltage output is calculated through a coupled field analysis. Both tables show that by increasing the tip displacement the voltage output increases. The simulation prediction on the uniform beam seems slightly better than the split beam especially at larger amplitudes. The reason could be due to some tilting in the split beam which is not considered in the simulation.

Table 6.2 – Comparing the experimental and FEM results for a simple cantilever.

Cantilever Configuration	Tip Disp. (µm)	V_{pk} (mV)	
		Simulation	Experiment
	33.15	77.83	80.7
	64.61	151.74	158.6
	91.61	215.16	224.5
	113.32	266.11	279.4
	132.54	311.23	323.8

Table 6.3 – Comparing the experimental and FEM results for a split cantilever.

Cantilever Configuration	Tip Disp. (µm)	V_{pk} (mV)	
		Simulation	Experiment
	33.42	59.69	68.6
	49.74	88.31	101.1
	65.37	116.75	132.3
	80.32	143.44	164.3
	94.57	168.89	191.0
	108.25	193.33	220.9
	118.22	211.13	274.2

6.3.1.3 Voltage Output vs. Power Output

A $3 \times 1\ mm^2$ silicon cantilever with a silicon proof mass is considered in the following to provide an example of the data collected in an electrical output measurement. The natural frequency of the beam was measured 1447.3 Hz and internal capacitance of 0.243 nF. Therefore, the internal impedance was calculated 452.77 kΩ using equation (6.6). Figure 6.6 demonstrates how the voltage and power output of the energy harvester change by increasing the load resistance. The voltage output increases by increasing the external load resistance and approaches a plateau, whereas, the power output reaches a maximum value and then decreases by increasing the external resistance. Figure 6.7 and Figure 6.8 show how the output voltage and power changes versus

external load resistance by increasing the base excitation acceleration at resonant frequency. The optimum load resistance in which the maximum power output occurs is the same value for various base excitations. The predicted optimum load value by equation (6.6) is 452.77 kΩ. However, the internal impedance of the oscilloscope (10MΩ) which was connected in parallel to the external load resistance must be considered as well. Considering the internal impedance of the oscilloscope, the value of 474.24 kΩ for added load was calculated which is closer to the measured values shown in Figure 6.8.

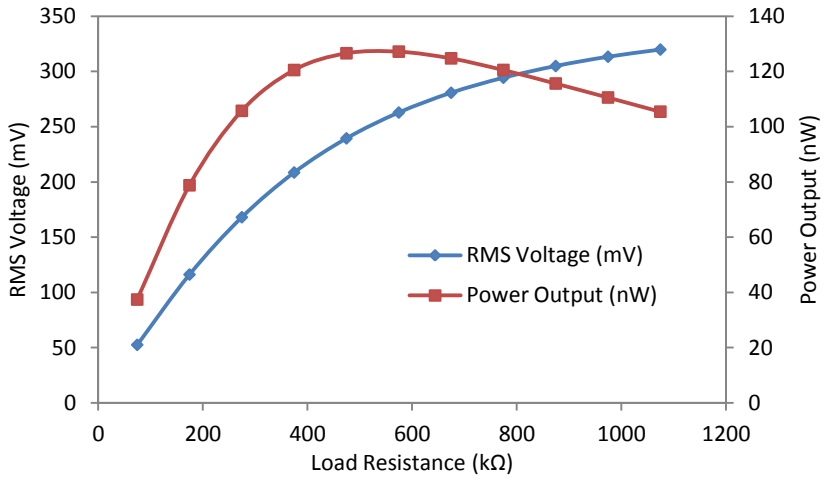


Figure 6.6 – Voltage output and power output versus external load resistance at base acceleration of 0.25g.

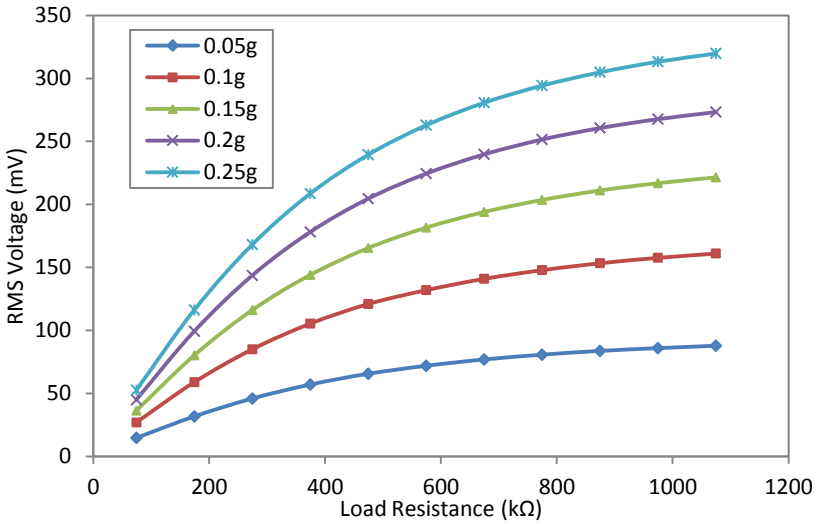


Figure 6.7 – RMS voltage versus external load at various base excitation acceleration.

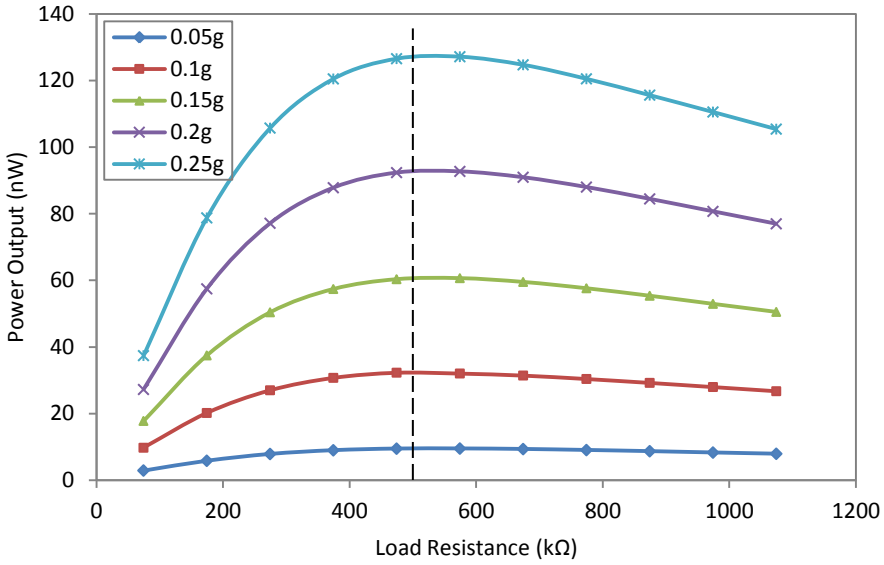


Figure 6.8 – Power output versus external load at various excitation acceleration.

Another set of data was collected to characterize the natural frequency based on the electrical output. Figure 6.9 demonstrate the power output of the harvester versus base excitation frequency under various excitation accelerations. This graph is shown in logarithmic scale to show the result clearer.

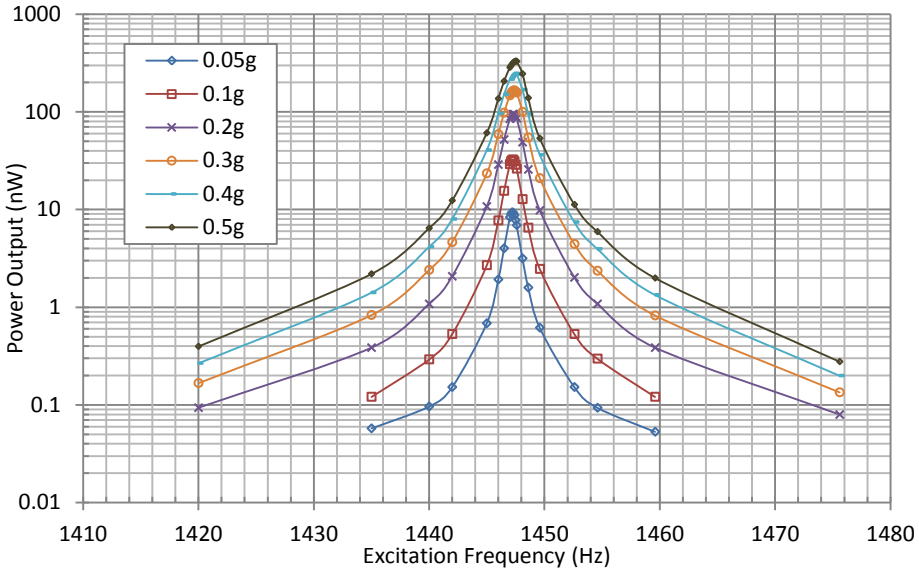


Figure 6.9 – Power output versus excitation frequency at various excitation acceleration (in logarithmic scale).

Figure 6.10 shows the peak voltage output versus the tip displacement of the cantilever. As expected, there is a linear relation between these two. Figure 6.11 demonstrates the correlation of the power output and tip displacement of the cantilever. As power output has a direct relation to square of voltage output ($P = \frac{V^2}{R_L}$), it is shown in Figure 6.11 that power output has also a direct relation to the square of the tip displacement. In both figures, the experimentally measured points are connected using curve fitting to better visualize the correlations.

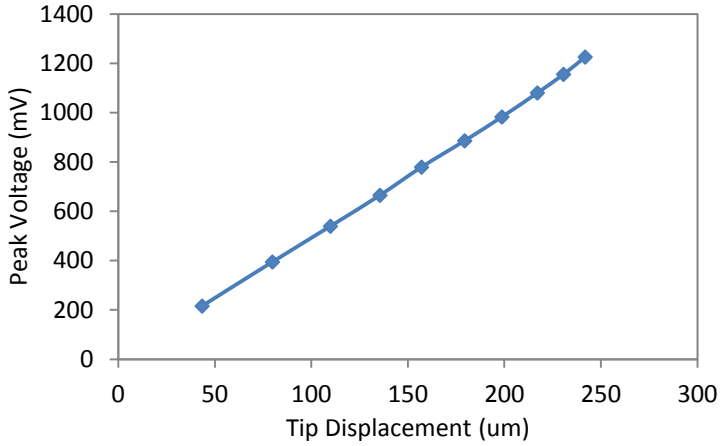


Figure 6.10 – The generated voltage has a linear correlation with tip displacement of the cantilever.

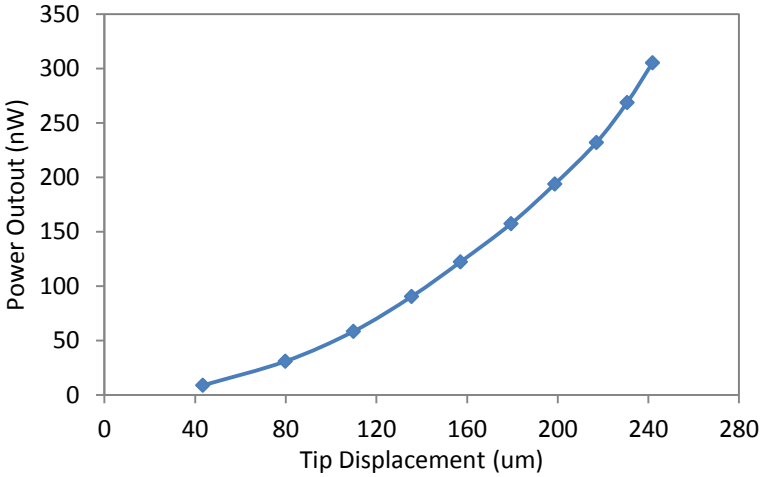


Figure 6.11 – The generated power has a direct correlation with the square of the tip displacement of the cantilever.

6.3.1.4 Array of Cantilevers

Figure 6.12 demonstrates a fabricated array of silicon based energy harvesters. Looking from the top, the length of the beams and their proof masses are purposely designed such that their natural frequency values are slightly different from one another. The thickness of all beams and the thickness of all proof masses have to be equal. The reason is that the thickness of the beams is defined by the backside deep silicon etching and the thickness of the proof masses is the same thickness as the silicon wafer. Since all members of the array are located close to each other and in one small section of the substrate, their thicknesses will be almost the same after deep silicon etching. The thickness of the beams could be adjusted to cover a lower or higher range of frequencies using the same array design. The same packaging scheme as explained in Section 5.3.1 was used for this device as well.

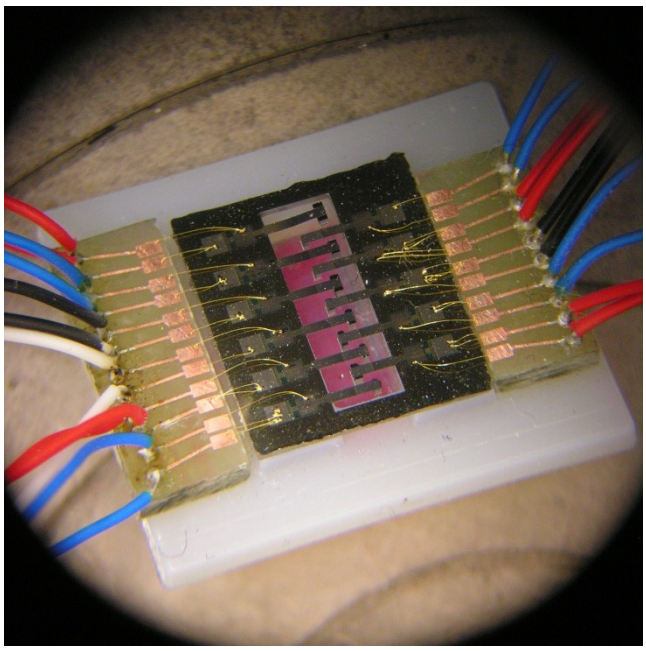


Figure 6.12 – An array of eleven silicon cantilevers is fabricated and packaged along with two PCBs on a customized 3D printed structure.

Table 6.4 provides the dimensions of all the cantilevers and their proof masses along with the measured natural frequencies. The sizes are selected based on the following analysis: For the cantilevers, the same width of 0.5 mm was used, but

the length was altered between three values of 2, 2.5, and 3 mm; For the proof masses, the width was altered from 0.5 to 1 mm with an increment of 0.1 mm and the length was varied from 0.3 to 0.5 mm with a gap of 50 μm. Among all possible combinations of sizes, the provided sizes in Table 6.4 were chosen to provide a wideband of the resonant frequencies for the array. The idea is where one peak goes close to zero (i.e. no harvesting), the other peak begins to harvest the ambient vibration at that frequency.

Table 6.4 – Silicon beam sizes and measured frequency responses.

No.	Beam Size (mm^3) ($W_b \times L_b \times T_b$)*	Mass Size (mm^3) ($W_m \times L_m \times T_m$)*	Measured Resonant Frequency. (Hz)
1	0.5×3×0.032	1×0.5×0.5	1520.3
2	0.5×3×0.032	0.7×0.45×0.5	1523.5
3	0.5×2.5×0.032	0.9×0.45×0.5	1528.1
4	0.5×2.5×0.032	0.8×0.35×0.5	1532.4
5	0.5×2.5×0.032	0.7×0.3×0.5	1537.4
6	0.5×2.5×0.032	0.5×0.35×0.5	1538.2
7	0.5×2×0.032	0.8×0.4×0.5	1548.4
8	0.5×2×0.032	0.8×0.3×0.5	1561.3
9	0.5×2×0.032	0.6×0.35×0.5	1572.1
10	0.5×2×0.032	0.5×0.35×0.5	1579.4
11	0.5×2×0.032	0.5×0.3×0.5	1595.6

* W, L, and T are the width, length, and thickness of the beam and mass.

Figure 6.13 and Figure 6.14 demonstrate the measured tip displacement and output voltage of all harvesters at their resonant frequencies. The sizes of the cantilevers could be selected such that the resulted resonant frequencies occur very close to one another (same as the first 5 harvesters) or provide slightly bigger gaps between the peaks (same as the last 6 harvesters). Due to the narrow bandwidth of each harvester, it seems that designing the array same as the first 5

harvesters would work better in terms of accommodating all ambient frequencies happening within a defined range.

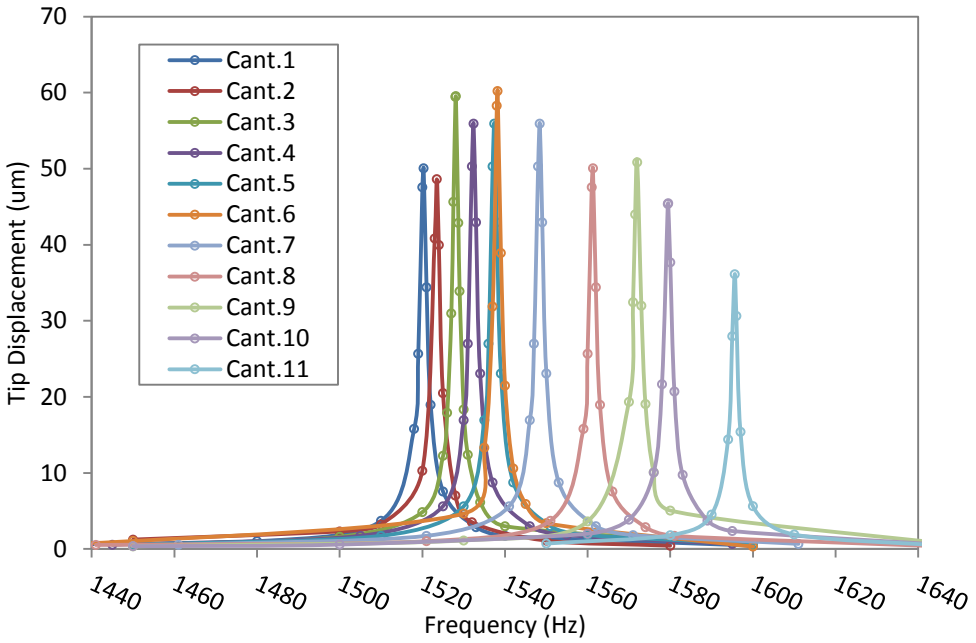


Figure 6.13 – The measured deflections of all harvesters at their resonant frequencies.

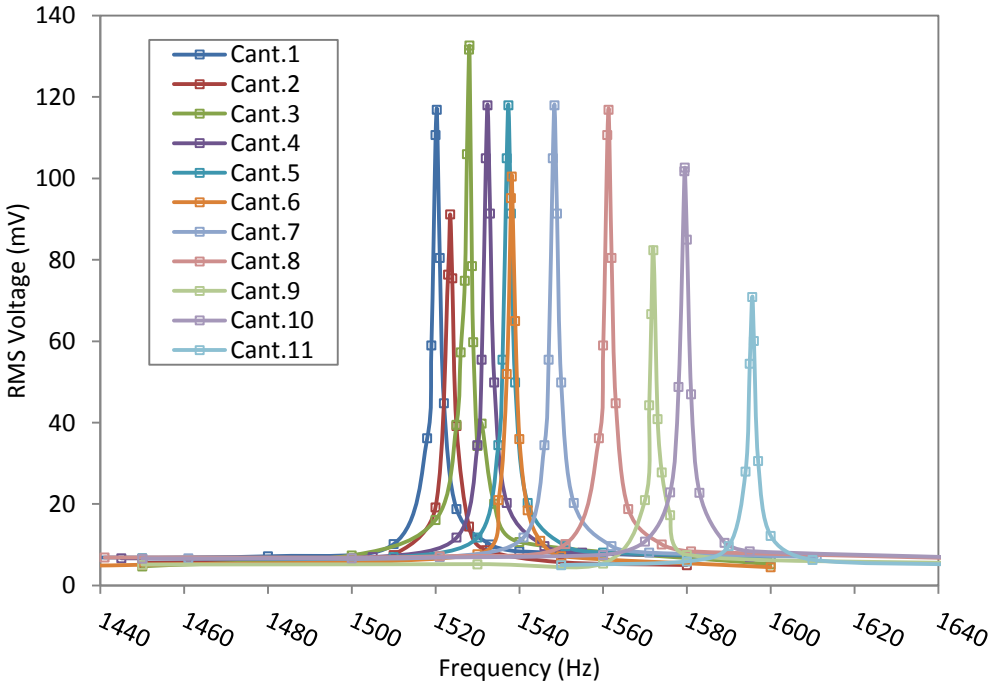


Figure 6.14 – The measured output voltage of all harvesters at their resonant frequencies.

As opposed to the conventional cantilever array designs which targeted higher power, above design could be implemented aiming to widen the frequency bandwidth of the energy harvesting. The piezoelectric thin film technology is growing which would provide the capability of using a single energy harvester to power a micro-device. Therefore, the presented array design would be more practical where each member covers a portion of the frequency spectrum to tactile the narrow bandwidth issue of linear vibration-driven energy harvesters.

6.3.2 Micro-Chip Energy Harvester

The micro-chip energy harvesters were designed for two different electronic chip sizes. The structural sizes and the vibrational measurements of the fabricated devices are presented in Table 3.1. The reported resonant frequencies in this table are measured values from the laser vibrometer. The mass displacement amplitude and electrical output of both energy harvesters are presented in the following sections.

6.3.2.1 CEH-1, Designed for 3×3 mm^2 Chip-size

The smaller energy harvester has higher resonant frequencies. Figure 6.15 presents the deflection of the energy harvester over a frequency spectrum for the first and second mode shapes under excitation acceleration of 0.15g. For this design, individual resonant frequencies are away from one another. For instance, there is approximately 70 Hz gap between the two peaks shown in Figure 6.15. At the first and second mode shapes, the induced stretching strain due to the large deflections of the beams results in the Duffing effect. This effect causes a wider frequency bandwidth at each natural frequency. However, the deflection at the third mode is smaller (Figure 6.16). Therefore, the backward frequency sweep graph overlaps with the forward frequency sweep graph similar to linear vibrating devices.

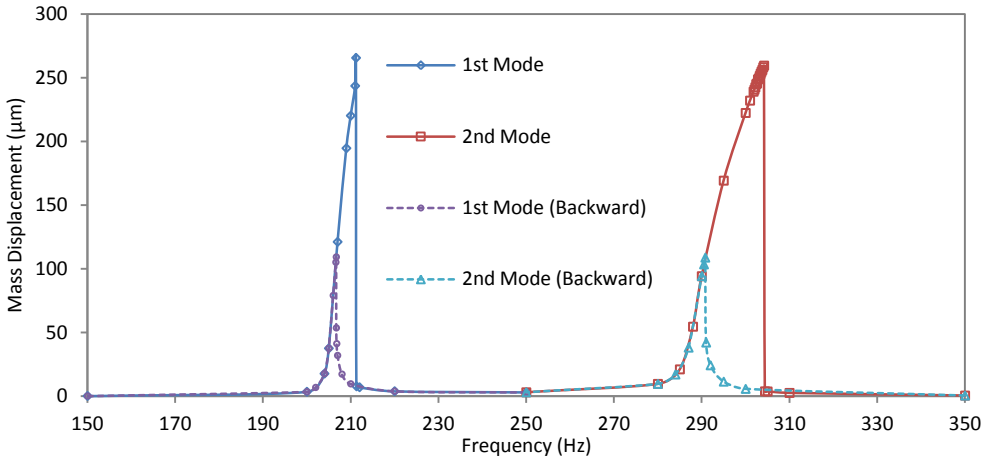


Figure 6.15–Mass displacement vs. base excitation frequency for 1st and 2nd modes of CEH-1 at 0.15g.

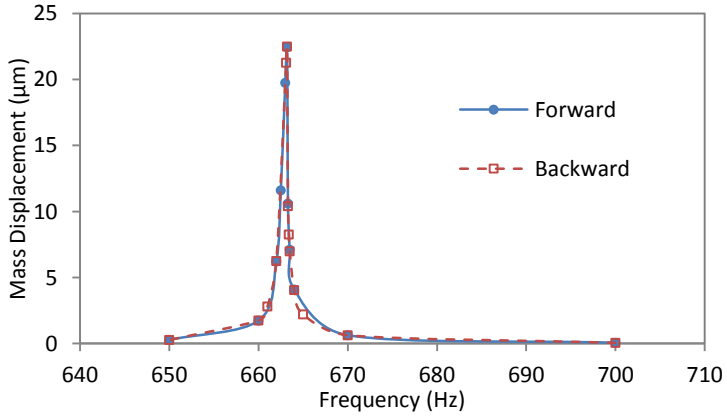


Figure 6.16–In 3rd mode under 0.15g, CEH-1 harvester acts similar to linear oscillators.

A set of coupled field static finite element analyses was conducted in ANSYS to simulate the electrical output of the piezoelectric elements of the CEH-1 energy harvester with respect to the deflection of the structure for each vibration mode. The same sizes as listed in Table 3.1 were used in this simulation. The properties of the piezoelectric layer were extracted from literature [115] and provided in Table 3.4. The boundary conditions were defined similar to Figure 3.2. The only difference is that a displacement was used for external loading in ANSYS instead of a force. Figure 6.17 shows the simulation results for all three mode shapes of the CEH-1 energy harvester. These results are also compared with the experimental measurements under the base excitation acceleration of 0.15g. The

second mode shape represents the highest nonlinearity and the third mode shape shows a linear behavior due to the small deflections at that mode. The third mode in Figure 6.17 is shown as a straight line representing a linear behavior which agrees with the results shown in Figure 6.16 where the results of the forward and backward frequency sweep overlap. As well, the nonlinearity shown in Figure 6.15 agrees with the electrical results shown in Figure 6.17. The reported voltages are the output of all four harvesting elements in series. For each point in the graph, a coupled-field static analysis has been done. The input load in the simulation is defined as the displacement of the same point used for the experimental measurements (Figure 3.2).

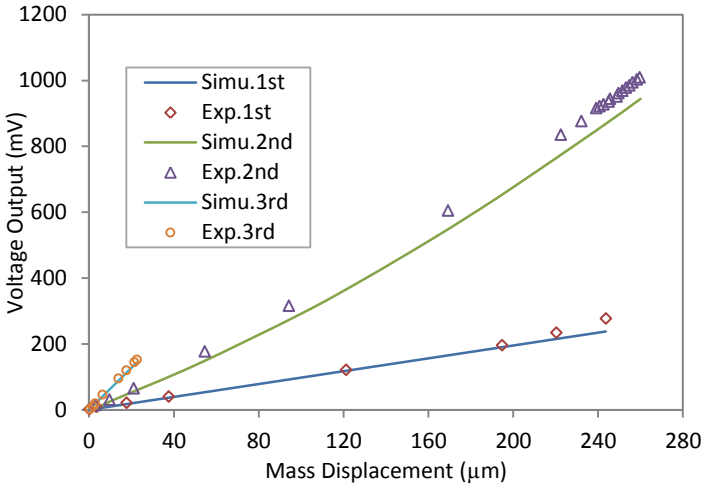


Figure 6.17–Comparing simulation and experimental voltage output results versus deflection for all three vibration mode shapes of CEH-1.

6.3.2.2 CEH-2, Designed for 6×6 mm^2 Chip-size

The larger energy harvester (CEH-2) has lower resonant frequencies, and the resonant frequencies are closer than in the CEH-1. Figure 6.18 shows the experimentally measured deflection of the proof mass over the forward and backward frequency sweep. The wider bandwidth at the first and second mode shapes makes the two mode shapes located next to one another on the frequency spectrum. As opposed to CEH-1, in the CEH-2 design, large deflection happens

in the third resonant frequency and causes a slightly wider bandwidth at this mode shape.

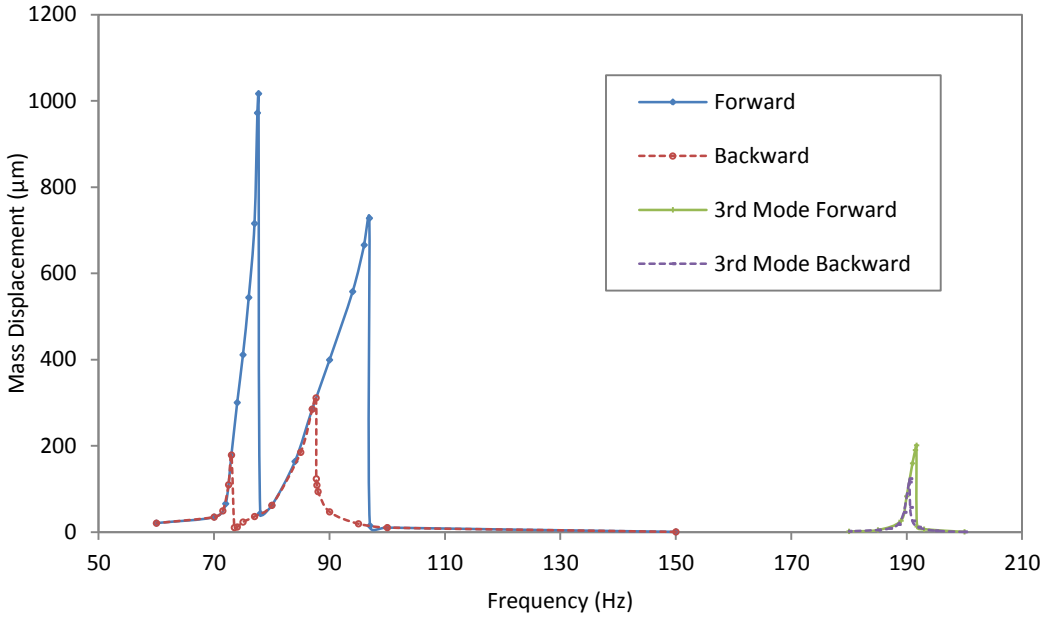


Figure 6.18 – Mass displacement versus the excitation frequency for CEH-2.

The experimental measurement of the second mode shape which shows the widest bandwidth is compared with the model presented in Section 3.3 (Figure 6.19). A quality factor of 150 was estimated for the model. Each point at the experimental graph represents a reading from the LDV. At a constant excitation acceleration, the excitation frequency was swept forward (from low to high frequencies) and backward (from high to low frequencies). Based on results, it seems that the simulation could be further exploited to model other cases at the designing stage before fabricating them.

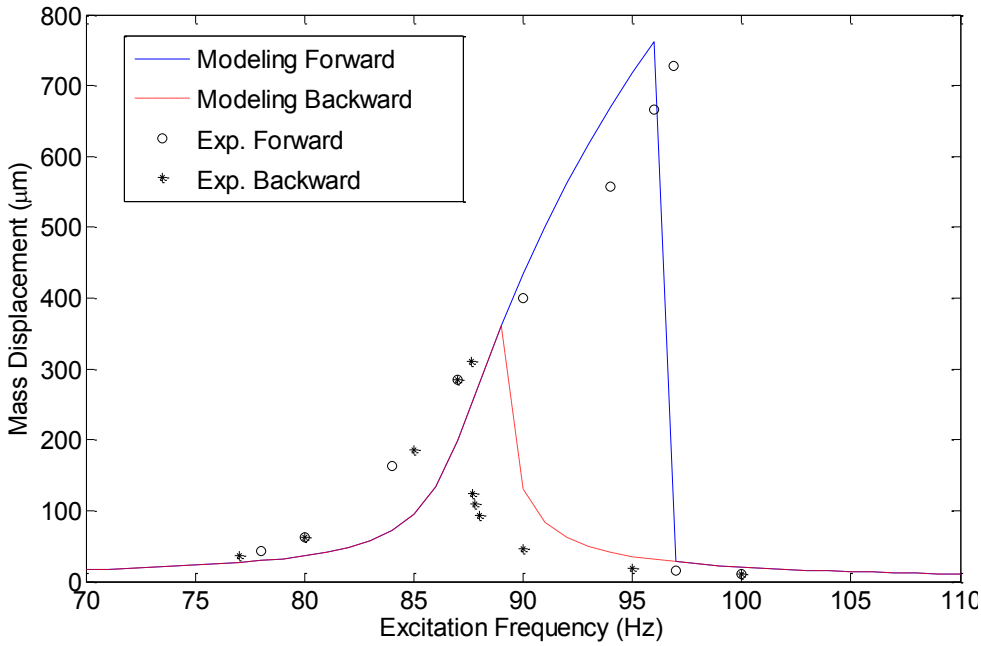


Figure 6.19–Comparing the simulated (Q=150) and experimentally measured mass displacement versus the excitation frequency of second mode of CEH-2 at 0.2g.

Figure 6.20 demonstrates the experimentally measured effect of different base excitation accelerations on the electrical response of the structure at the first two mode shapes. Also, Figure 6.21 compares the voltage output of the harvester at all three mode shapes under 0.2g base acceleration. One might note that the amplitude of the displacement in the first mode is higher than in the second mode (Figure 6.18), however, the maximum voltage at first mode is less than the maximum voltage at second mode (Figure 6.21). The reason is that, in second mode all four piezoelectric elements are under the same strain, while only two piezoelectric elements experience maximum strain in the first mode vibration. Figure 6.21 also shows that at higher accelerations, the first and second modes could overlap and make a wider frequency bandwidth including both mode shapes.

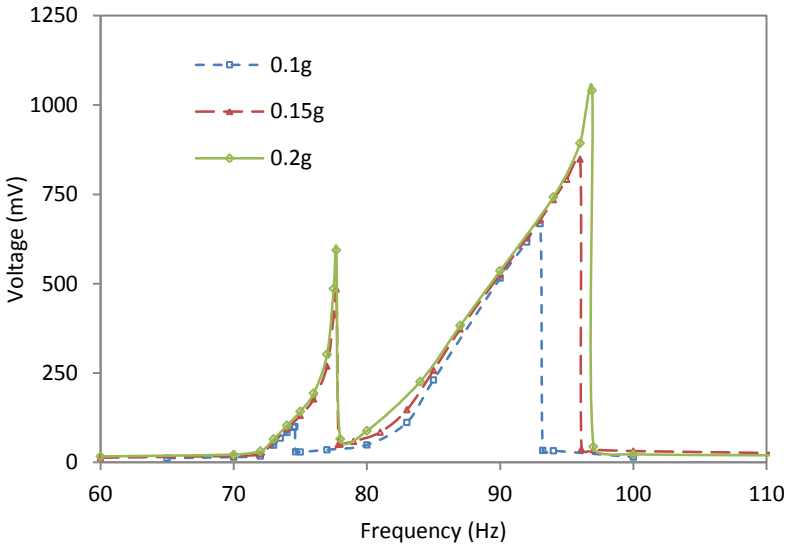


Figure 6.20–Voltage output versus frequency for first two modes of CEH-2 at different excitation accelerations.

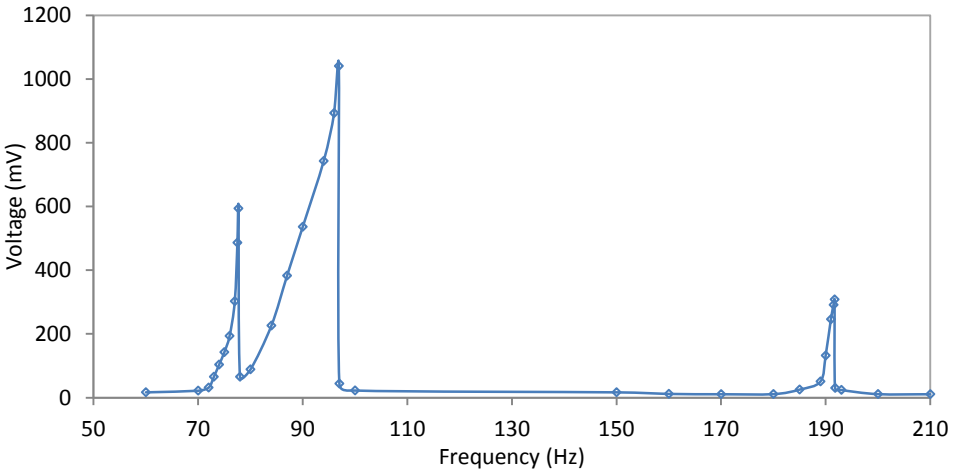


Figure 6.21–Voltage output of all three modes of CEH-2 versus the excitation frequency at 0.2g.

Figure 6.22 presents the output voltage versus the mass displacement of the harvester. Both the first and second modes follow a cubic nonlinear path. As opposed to a simple fixed-fixed beam, the presented design undertakes higher bending strains and after certain points the nonlinear effect appears. This helps to increase the amplitude of the vibration and consequently increase the output voltage and also provide a reasonably wide bandwidth to allow use for practical

applications. Maximum power output of 20nW was measured across an optimal load resistance of 4.8MΩ at first mode, 136nW across 2MΩ at second mode, and 26nW across 0.9MΩ at third mode for the CEH-2 harvester.

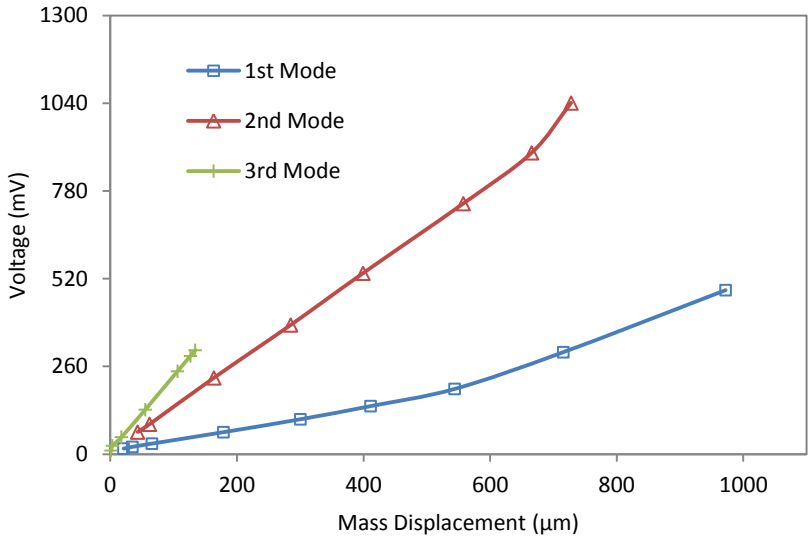


Figure 6.22–Comparing the experimental voltage output versus the mass displacement for the three modes of CEH-2 at 0.2g.

6.3.3 Membrane Energy Harvester

The packaged device was clamped on a Brüel & Kjær type 4809 shaker table. A sinusoidal signal was applied to the shaker through a signal generator and a power amplifier. The vertical displacement of the base and the proof mass was measured using a Polytec Laser Doppler Vibrometer (LDV). Subtracting the Fast Fourier Transform (FFT) of the base signal from the mass signal provides the relative displacement signal in the frequency domain.

Figure 6.23 presents a comparison of the theoretically estimated (using Q=35) and the experimentally measured proof mass displacement in forward and backward frequency sweep at an acceleration of 4g of the shaker table. For the experimental test, the frequency of the input signal to the shaker table was set to a low value and then, it is increased. For each excitation frequency, a point is shown in Figure 6.23. An inverse trend was used for backward frequency sweep. The frequency bandwidth at this excitation is calculated of 146 Hz. Figure 6.24

compares the bending and stretching strains of the structure in forward and backward frequency sweep at 4g. The same technique as [92, 95] is used to calculate the bending and stretching strains. Figure 6.24 shows that the stretching strain occurs in higher frequencies where the mass displacement is larger. Also, this figure illustrates much lower bending strain in comparison to the stretching strain. The electrical output results are discussed in the following section.

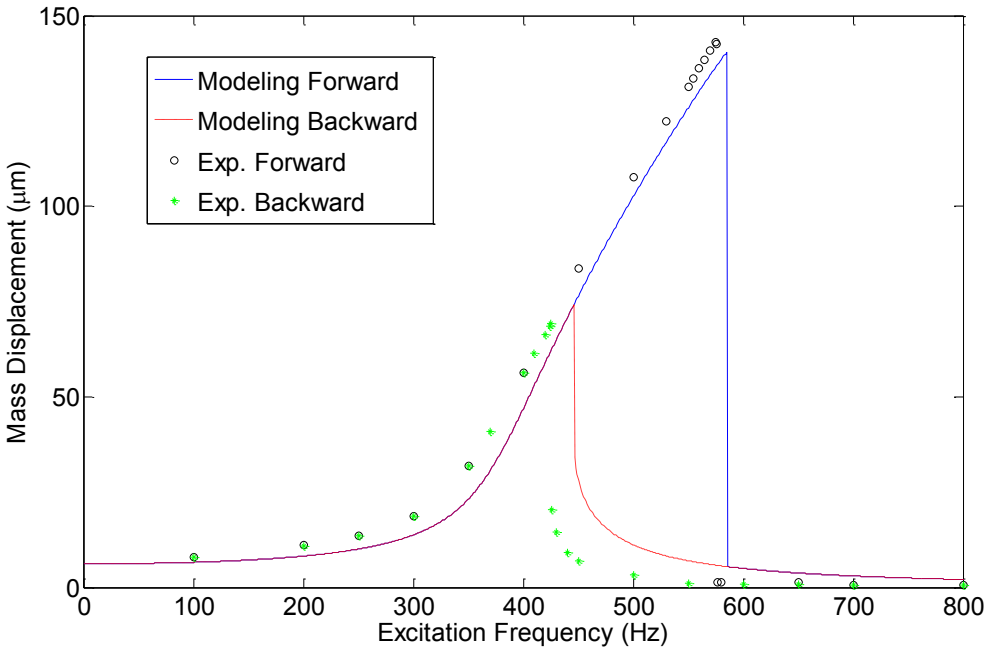
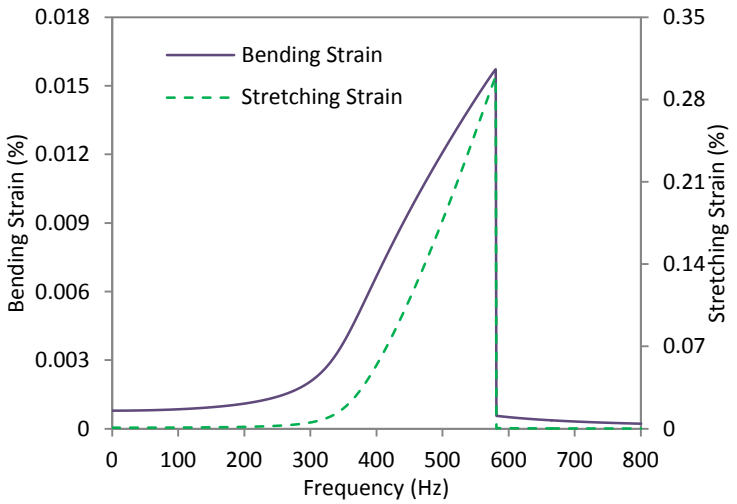
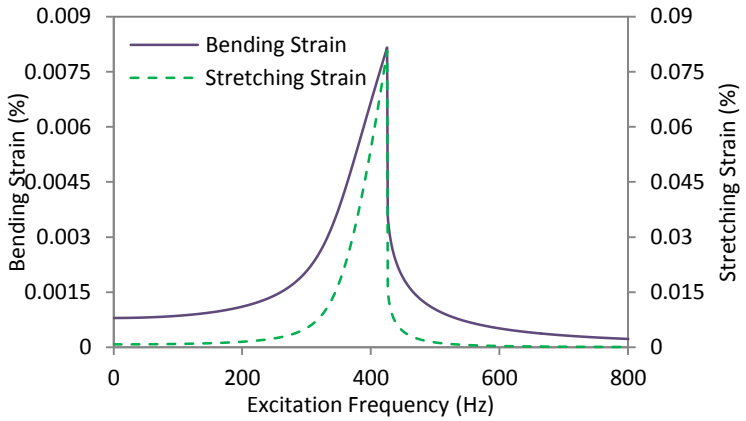


Figure 6.23–Comparing the experimental and theoretical results (Q = 35) of mass displacement versus base excitation frequency.



(a)



(b)

Figure 6.24–Comparing bending and stretching strains in a forward (a) and backward (b) excitation frequency sweep at 4g.

6.3.3.1 Electrical output measurement

The packaged devices were connected to an oscilloscope to monitor their output voltage while they were excited by a shaker table. Figure 6.25 demonstrates the generated open circuit voltage at 4g base excitation. The excitation frequency was swept from low to high frequencies and vice versa and the voltage was measured at each frequency. The reported voltage is the output of four harvesting elements in series.

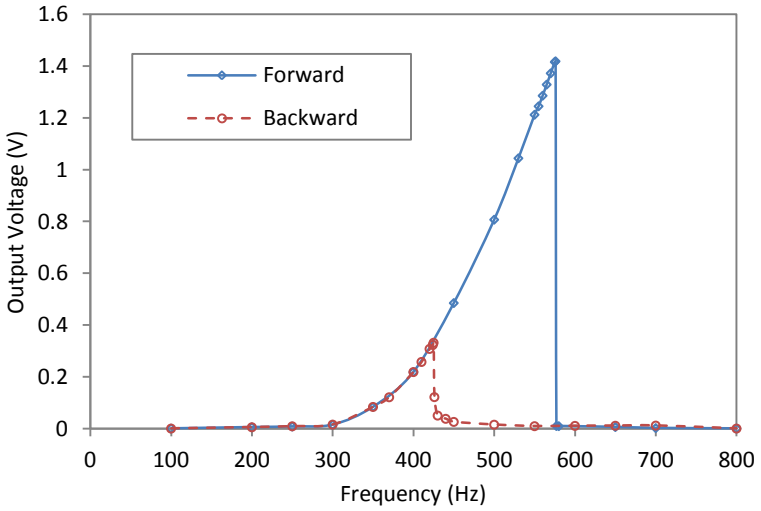


Figure 6.25–Output voltage under forward and backward excitation frequency sweep at 4g base acceleration.

Figure 6.26 demonstrates the nonlinear relation between the deflection amplitude of the proof mass and the output open circuit voltage in forward frequency sweep just before jumping down. In the case of a linear vibrating system such as a cantilever with small deflections, there would be a linear correlation between the tip deflection and the output voltage. Figure 6.27 compares the frequency bandwidth of the membrane deflection and the output voltage. It is shown that the frequency bandwidth of the voltage graph (Figure 6.27) is much closer to the stretching strain graph than the bending strain graph (Figure 6.24.a). Therefore the stretching strain, as opposed to the bending strain, plays a more important role in generating electrical output in the SU-8 membrane.

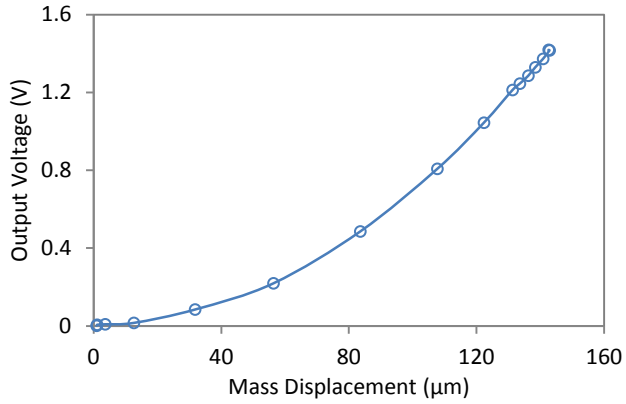


Figure 6.26–The mass deflection and the output voltage have a nonlinear relation.

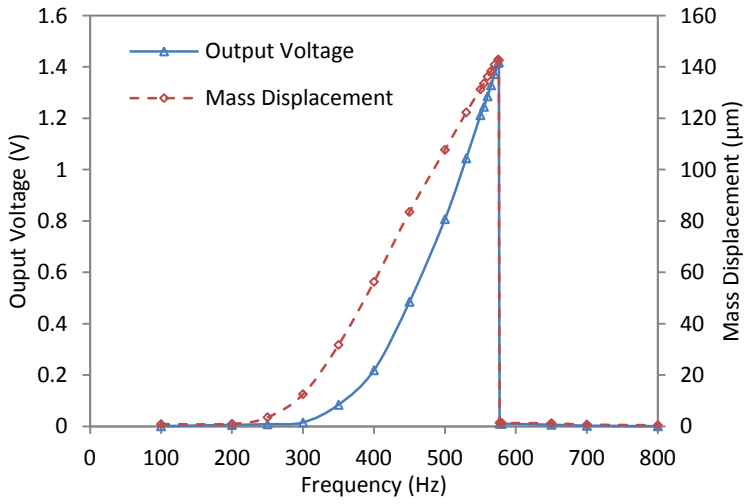


Figure 6.27– Output voltage and membrane deflection over a range of excitation frequencies.

To find the maximum power output, the optimal load resistance needs to be determined using equation (6.6),

$$R_L = \frac{1}{2\pi C_p f_n} \tag{6.6}$$

$$P = \frac{V_{rms}^2}{R_L} \tag{6.7}$$

where C_p is the capacitance of the piezoelectric elements and f_n is the resonant frequency of the membrane [26]. For the power calculations (equation (6.7)) in this work, the resonant frequency is considered constant and subsequently, the load resistance is calculated as a constant (equation (6.6)). However by changing the load resistance, both power output and the bandwidth could be enhanced [49]. The load resistance is connected in parallel to the harvester and as well to the oscilloscope. The output power is calculated using equation (6.7) where V_{rms} is the RMS output voltage. The internal capacitance of the harvester was measured as 1.17 nF. Using a natural frequency of 380.8 Hz, the load resistance was calculated 357.4 kΩ. The constant natural frequency value used here is the same value found by frequency test under LDV. Figure 6.28 demonstrates the output power under three different base excitation accelerations while excitation frequency was swept forward. The higher excitation acceleration results in higher stretching strain values. Therefore, the generated electrical power would become higher and consequently for a required power generation, a wider frequency bandwidth can be obtained.

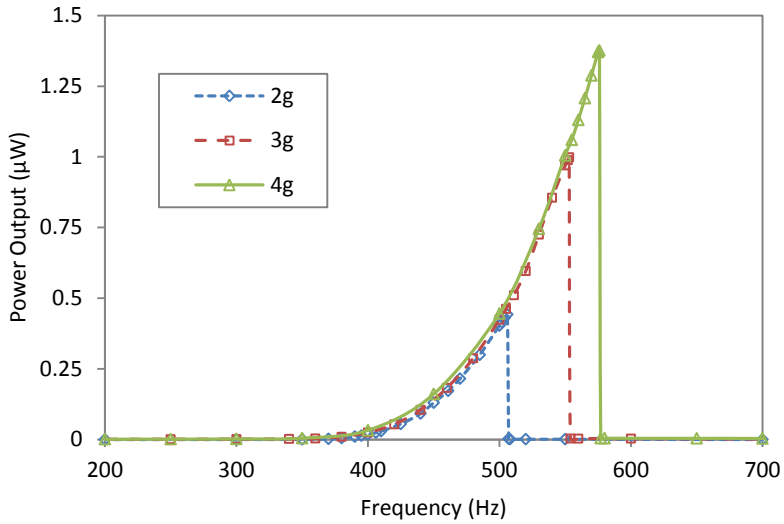


Figure 6.28– Output power under forward frequency excitation at various accelerations.

6.3.3.2 Increasing the Power Output

This work demonstrates the capability of using a polymeric membrane for energy harvesting purposes. The reported electrical outputs in the previous sections could be enhanced by various methods. For instance, replacing the AlN layer with a Lead Zirconate Titanate (PZT) layer would increase the maximum output power due to higher piezoelectric coefficients of PZT versus AlN [203]. In addition, a d_{33} mode piezoelectric configuration would respond better than d_{31} mode to the stretching strain and is shown to have higher power output for the same structural configuration [204]. In addition, a different electrical interface and testing under vacuum could increase the electrical output as explained in the following.

A. SSHI vs Classic electrical interface

An optimum piezoelectric energy harvester requires both mechanical structure to convert the maximum available environmental vibration energy to electrical energy and an electrical interface to transmit the optimum output energy to the electrical load. As an alternative for the classic interface, various electrical interfaces were developed to improve the output power of the piezoelectric energy harvesters. Some of those interface circuits are: voltage doubler, synchronous charge extraction, parallel-synchronized switch harvesting on

inductor (SSHI) and series-SSHI interfaces [205-208]. In the following, the parallel-SSHI interface is used to estimate the extractable power and compare it with the results of the classic interface. In comparison to a standard interface, a parallel SSHI interface has an extra switching device, which consists of a switch and an inductor, connected in parallel to the piezoelectric element. The switch is always open until maximum displacement occurs. Then, the switch is closed for a very short period where the voltage on the piezoelectric element is reversed. While switch is closed, the inductor and the capacitance of the piezoelectric element form a LC oscillating electrical circuit. As a result, (a) the voltage amplitude increases; (b) the voltage and velocity become in-phase [209]. These effects provide a significant improvement in the output power. The output power of the energy harvester using standard (classic) and SSHI interfaces can be calculated by equation (6.8) and (6.9), respectively [206, 207],

$$P_{Std} = \frac{R_L \alpha^2 \omega^2 U_M^2}{(R_L C_p \omega + \frac{\pi}{2})^2} \tag{6.8}$$

$$P_{SSHI} = \frac{4R_L \alpha^2 \omega^2 U_M^2}{(R_L C_p \omega (1 - e^{-\pi/2Q_i}) + \pi)^2} \tag{6.9}$$

where α is force factor, U_M is mass deflection and Q_i is the electrical quality factor. Figure 6.29 compares the calculated power output using the classic electrical interface and the estimated power output using parallel-SSHI interface with three different electrical quality factors (Q_i=2, 3, 5). The electrical quality factor depends on the losses of the electrical components and could go up to 20 [49, 206]. The higher Q_i results in the higher power output, however, there are some limitations due to the losses of the electrical components [206]. As shown in Figure 6.29, the generated 1.37μW using the classic interface could be enhanced to 10.1μW using the parallel-SSHI interface. It is worth to note that the maximum power output experimentally measured at 4g (Figure 6.28) is close to the theoretical power output calculated for standard electrical interface (Figure 6.29). In conclusion, this section shows that, comparing to the conventional

harvesters, by exploiting a proper electrical interface and optimizing its parameters to reduce the losses (i.e. increasing the electrical quality factor) a higher power output could be extracted from a given vibration-based energy harvester.

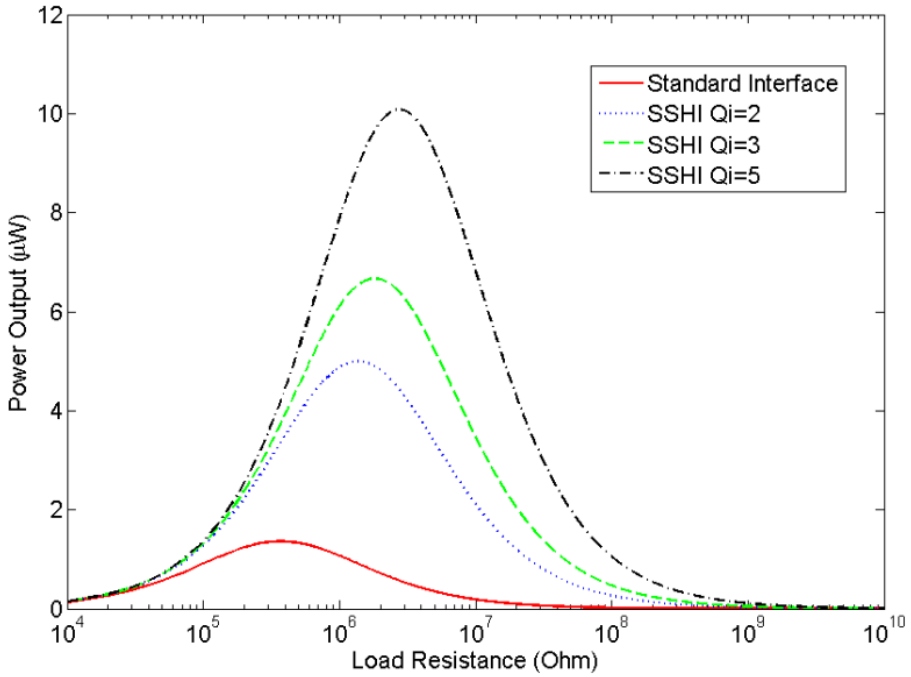


Figure 6.29–Estimating the maximum power output at 4g base excitation using the classic and SSHI interfaces with Q_i=2, 3, and 5.

B. *Testing under Vacuum*

The air damping effect on MEMS devices could decrease the amplitude of the vibration. The wide surface of a membrane makes the device affected by the air damping more than the devices with smaller surface area such as cantilevers. Therefore, it seems packaging a micro-membrane under vacuum could increase the vibration amplitude. In this work, a small vacuum chamber was prepared. The chamber was connected to a vacuum pump capable of providing 1×10-4 Torr vacuum pressure. A membrane with slightly different natural frequency was placed in the vacuum chamber under base excitation of 2.5g applied by a B&K shaker table. The vibration amplitude was improved by ~10% (Figure 6.30). In addition, the harvestable frequency bandwidth was improved by ~7%. The

resonant frequency would shift in different air pressures [210, 211]. One could clearly see this effect in Figure 6.30, but in comparison to silicon based designs, the improvement in amplitude is relatively small, indicating internal damping is much more important.

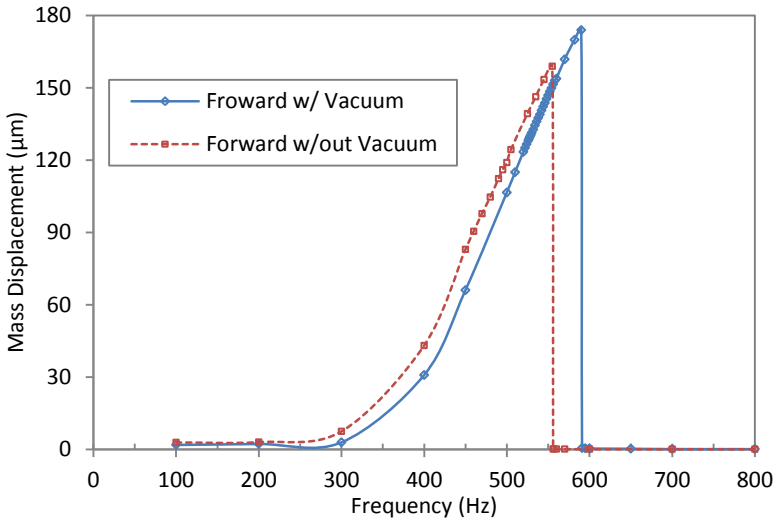


Figure 6.30–Packaging a membrane under vacuum enhances both the vibration amplitude and the harvestable frequency bandwidth.

C. *Scaling Effect on Polymeric Membrane with PZT Layer*

As mentioned previously, a circular diaphragm could be used for various applications such as sensors, actuators, miniaturized microphones, and acoustic energy harvesters. An investigation of the scaling effect to characterize the performance of the device will provide a better understanding of this design. It is shown in previous sections that simulation could reasonably predict what could happen in real applications. In this section, the polymeric membrane is investigated using the Lumped Element Modeling which is introduced in [112, 212] for composite diaphragm. The Lumped Element Model, which was validated by experimental results, has been reported as a directly applicable model for investigating scaling effects and designing piezoelectric composite diaphragms [112, 212]. Figure 6.31 demonstrates the schematic of a polymeric diaphragm which could be used for energy harvesting. In this device, R_2 is the radius of the diaphragm and also the outside diameter of the piezoelectric ring

and R_1 is the inside radius of the piezoelectric ring. The piezoelectric layer in this case assumed to be distributed around the edge of the membrane in the shape of a ring which deviates from the design shown in Figure 3.5, but would still provide qualitative comparisons for performance. As previously mentioned, using a PZT layer could improve the piezoelectric effect comparing to an AlN layer. Therefore, PZT layer is considered for characterization in this section.

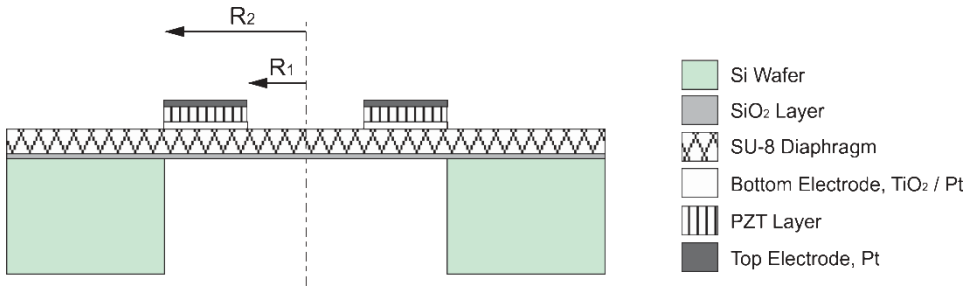


Figure 6.31 – Schematic of a piezoelectric diaphragm.

Three parameters are examined for various geometries of the device to characterize the scaling effect of the polymeric energy harvester: resonant frequency, deflection, and coupling coefficient (k). Figure 6.32 shows the effect of varying R_1/R_2 ratios on the above three parameters. The PZT and SU-8 thicknesses are 1.2μm and 5μm, respectively. Figure 6.32 suggests that a larger R_1 results in a lower natural frequency and a higher deflection which is due to the much lower stiffness of SU-8 comparing to PZT. Figure 6.32 (c) demonstrates that the smaller the device is the higher the coupling coefficient will be. In addition, it is seen that increasing R_1 enhances the coupling coefficient of the energy harvester. In the case of R_1/R_2=0.95, by decreasing the size of the membrane by a factor of 2 (from R_2=4mm to 2mm), the resonant frequency of the diaphragm increases by a factor of ~4 (from 546.6Hz to 2172Hz), the deflection decreases by a factor of ~15.5 (from 6.9 μm to 0.44μm), and the coupling coefficient increases by a factor of ~2 (from 0.0022 to 0.0043). Almost same effect has been seen when decreasing the membrane size from R_2=2mm to 1mm.

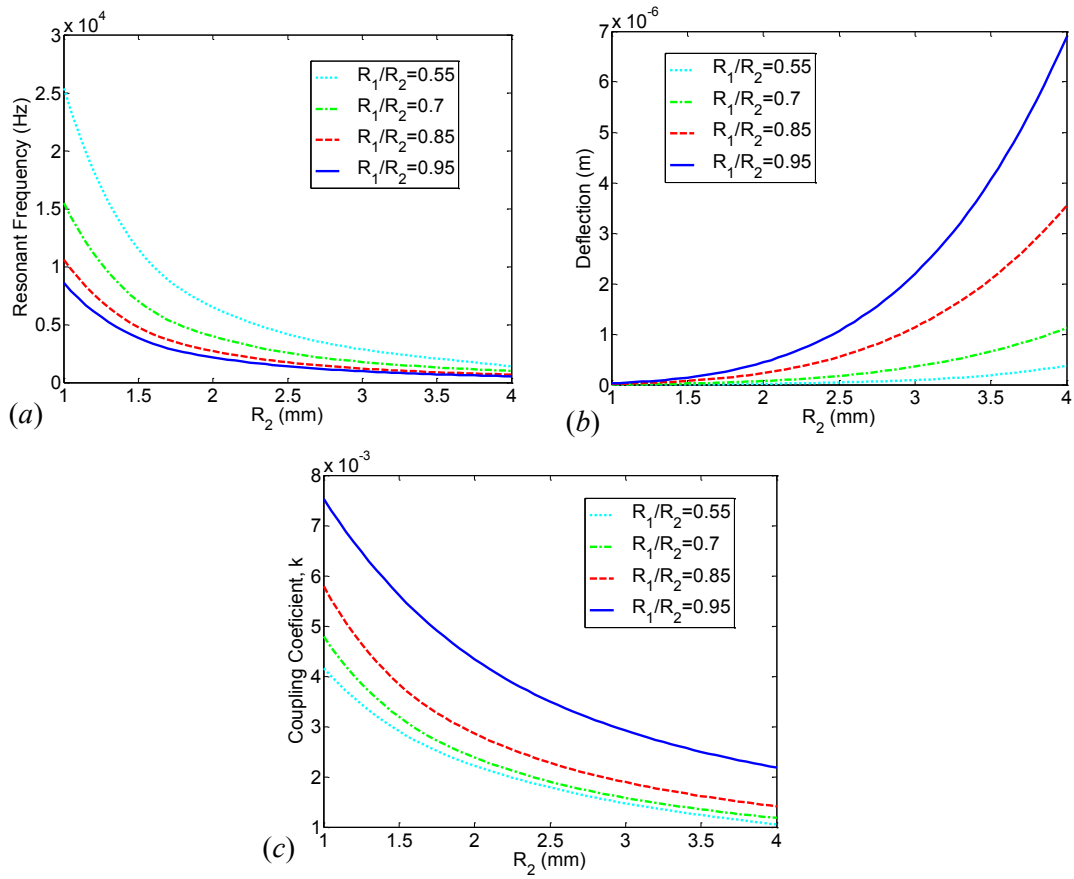


Figure 6.32 – The effect of changing the R_1/R_2 ratio on (a) resonant frequency, (b) deflection, and (c) coupling coefficient are investigated while the radius of the diaphragm is altered. PZT thickness is 1.2µm and SU-8 thickness is 5µm.

The effect of varying the SU-8 diaphragm's thickness on different device sizes is investigated in Figure 6.33. The graphs show that a thinner diaphragm results in lower resonant frequency, higher deflection, and lower coupling coefficient. The thickness of the diaphragm could be adjusted for different applications such as a low frequency energy harvester or an actuator with large deflections. The effect of thickness variation does not change by altering the size of the diaphragm. For instance in the case of R_2=3mm, same as other sizes, increasing the thickness of the diaphragm by a factor of 2 (for instance from 4µm to 8µm), the resonant frequency increases by a factor of ~1.8, deflection decreases by a factor of ~6.5, and the coupling coefficient increases by a factor of ~2.7.

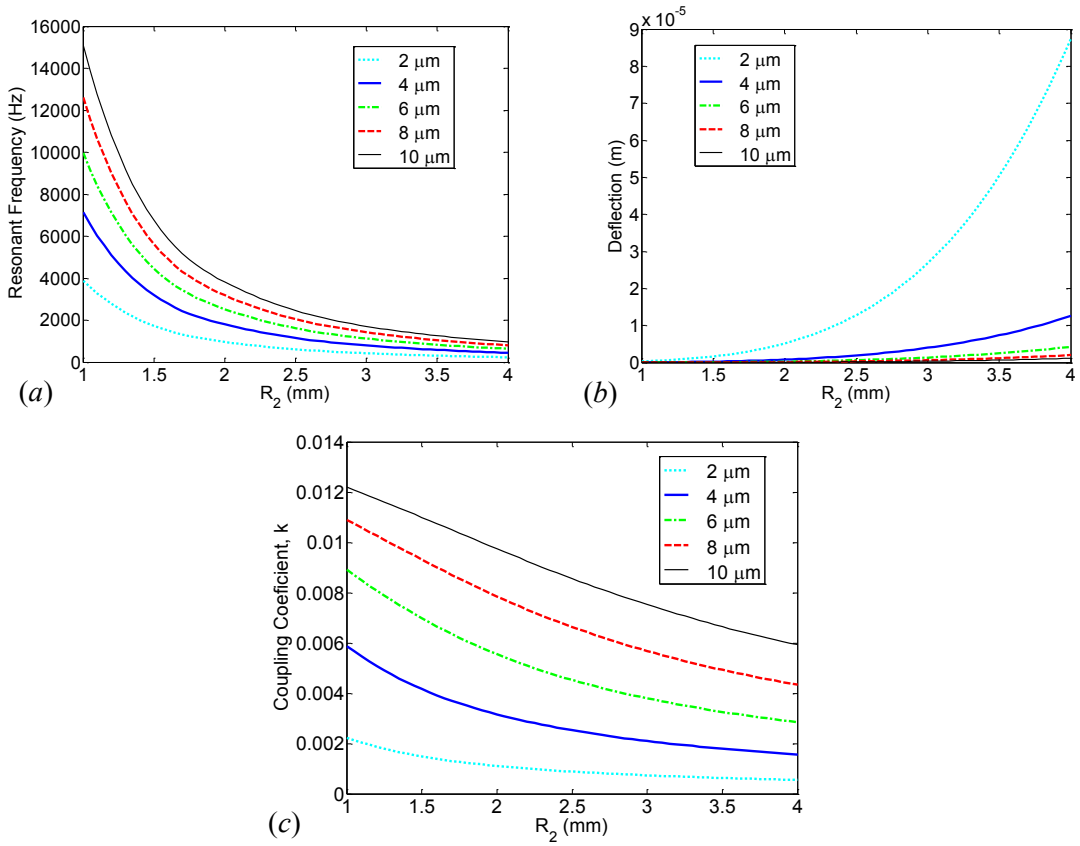


Figure 6.33 – The effect of changing the SU-8 diaphragm thickness on (a) resonant frequency, (b) deflection, (c) coupling coefficient are investigated for various radiuses of the diaphragm. R_1/R_2=0.95 and PZT thickness is 1.2μm.

The effect of residual stress in the TiO_2 and PZT layers are investigated on the coupling coefficient for various sizes of the diaphragm. Figure 6.34 demonstrates the results. Residual stresses of PZT and TiO_2 thin films have been examined in [213] and [214], respectively. Depending on the thickness of the thin films and their processing parameters and conditions, the residual stress of the resulted layers could dramatically change. Figure 6.34 shows that, in general, the higher the residual stress in different layers of a composite diaphragm is, the lower the coupling coefficient will be. For instance as shown in Figure 6.34(a) for a PZT layer with a residual stress of 1000 MPa, decreasing the size of the diaphragm by a factor of 2 (from R_2= 4mm to 2mm) results in increasing the coupling coefficient by a factor ~2 (from 0.000925 to 0.00186). In the case of

decreasing the diaphragm size from R_2= 2mm to 1mm, the coupling coefficient increment gradually declines from a factor of ~2 to a factor of ~1.5 for 1000 MPa and 10 MPa residual stresses, respectfully. This effect shows that the performance of a piezoelectric layer with a smaller residual stress is slightly less affected by the scaling.

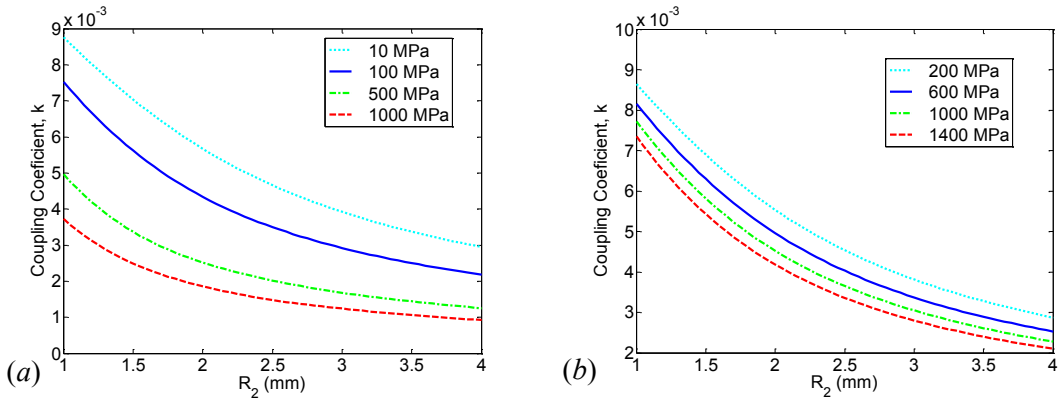


Figure 6.34 – The effect of variation in the residual stress of (a) PZT layer and (b) TiO_2 layer on coupling coefficient is investigated while the residual stress of the TiO_2 layer is 1200 MPa for (a) and the residual stress of the PZT layer is 100 MPa for (b). R_2=3mm, R_1/R_2=0.95, PZT thickness is 1.2µm, and SU-8 thickness is 5µm.

Finally, the effect of using a polymer-based diaphragm is compared with an identical geometry silicon-based diaphragm in Figure 6.35. A SU-8 based energy harvester provides a lower resonant frequency, larger deflections, and lower coupling coefficient. Therefore, the material of the diaphragm has a significant effect on the performance of the device. A proper material must be chosen for different applications. The characterization of the scaling effect provides a proper platform at the design stage.

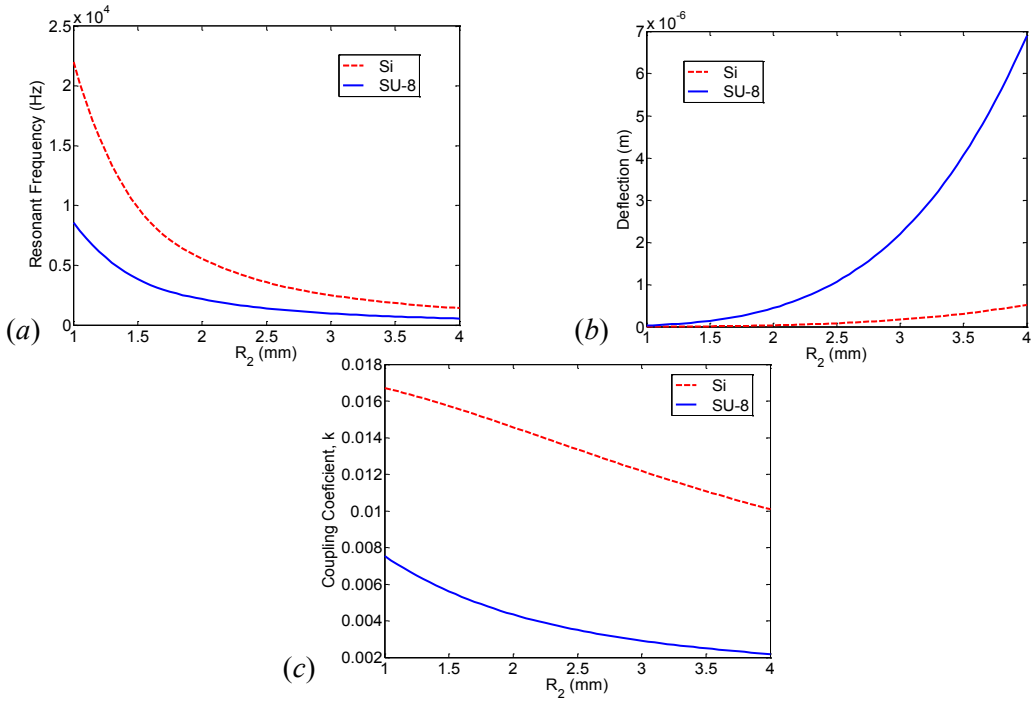


Figure 6.35 – Comparing the performance of a silicon diaphragm versus a SU-8 diaphragm with an identical geometry. (a) Resonant frequency, (b) deflection, and (c) coupling coefficient are investigated versus various diaphragm radiuses. R_1/R_2=0.95, PZT thickness is 1.2µm, and the diaphragm's thickness is 5µm.

Chapter 7 - Conclusion and Future Work

7.1 Thesis Summary

In this thesis the vibration-driven piezoelectric energy harvesting was considered to harvest ambient vibration energy. The main challenges in this field are the requirement for oscillators with low resonant frequencies (<500Hz) and wide frequency bandwidth. Due to tiny sizes of the MEMS harvesters, their resonance frequency is high. In this research, two platforms were investigated to decrease the natural frequency of MEMS devices. In addition, most of the conventional energy harvesters reported in the literature are linear oscillators providing very narrow frequency bandwidth. Therefore in this thesis, widening the frequency bandwidth by increasing the stiffness of the structure was considered for both designs. With regard to the silicon-based design, a wideband frequency spectrum was obtained in addition to the capability of harvesting in three different ambient frequencies. With regard to the polymer-based design, a much wider frequency bandwidth was obtained promising the capability of polymeric structures to be used as energy harvesters. The measured experimental results were compared to the simulation results. The potential methods to improve the electrical outputs were investigated and simulation results show promising strategies to enhance the performance of the proposed energy harvesters. In addition, the capability of microfabricating polymer-based structures with piezoelectric elements was illustrated. The microfabrication of piezoelectric energy harvesters involves various processes such as high temperature oxidation, soaking in acids and acetone, and long RIE which could damage the polymers. In this research, a microfabrication process flow was developed to accommodate building polymeric structures along with above processes. The packaging of the fabricated devices was also a concern in this research. Various packaging

techniques were developed in-house or adapted from reported methods in the literature. In the following, the contributions of this work and also a few suggestions to continue this research are provided.

7.2 Research Contribution

The objective of this research was to develop platforms for broad bandwidth energy harvesting with low resonant frequency and also to develop a complete prototyping path including all steps starting from the design to the testing. A silicon based configuration was designed and analyzed with low resonant frequency. Also, Polymeric materials were investigated to be used as structural material to decrease the resonant frequency of the energy harvesters. In the following, above items are listed with more details.

1. A structural design with multi degrees of freedom was investigated to harvest low frequency ambient vibrations energy. This structure has been fabricated with MEMS techniques which provide the capability of scaling and mass production. The resonant frequencies of the presented design are less than 200Hz for its first three mode shapes and less than 100Hz for its first two mode shapes. The first two mode shapes occur very close to one another representing two close peaks at the frequency spectrum demonstrating a wide frequency bandwidth. The first and third modes shapes involve with torsion, while the second mode shape represent a directional deformation. The presented design considering its second mode shape could be compared with a conventional doubly clamped beam where this work's design has a smaller size. A maximum open circuit voltage of 1V and maximum power of 136nW were measured at 0.2g base excitation acceleration using the microchip design. (This design is presented in a paper which is under review at Sensors and Actuators: A)
2. A polymer based structure was used to build energy harvesters in order to reduce the natural frequency of the harvesters. SU-8 was the polymeric material which was used to build a circular membrane as the main structure

for the energy harvester. Piezoelectric elements were fabricated on the edges around the membrane to obtain the maximum generated power. This design was also fabricated using the MEMS thin film techniques which is capable to be mass produced or scaled. The simulation results show that the resonant frequency of a SU-8 membrane is more than 5 times lower comparing to a similar geometry silicon membrane. Testing results show a linear resonant frequency of 381Hz and a maximum power output of 1.37μW at the base excitation of 4g using the polymeric membrane. (This design has been presented in a paper which is accepted at Journal of Micromechanics and Microengineering, 2014)

3. Both micro-chip and SU-8 membrane designs provide a broad frequency bandwidth due to the Duffing effect. In the case of the micro-chip design, the structure shows 10 Hz frequency bandwidth at its second mode which is wider than its bandwidth at the first and third modes. In the case of the polymeric membrane device, the frequency bandwidth was measured as high as 146Hz. This demonstrates that the polymeric devices not only can be exploited to make low resonant frequency devices, but also can provide wide frequency bandwidth. Comparing with the conventional linear energy harvesters, above designs are more practical for real applications due to their wider harvesting bandwidth.

The above objectives were pending development of the required microfabrication and packaging methods. A fabrication process flow was developed to accommodate the polymeric material in the energy harvesting fabrication. In addition, 3D packaging techniques were adapted to package the fabricated devices. These items are elaborated in the following.

a) A scalable fabrication process flow was developed to properly fabricate piezoelectric layers on SU-8 thin films. The main challenge was that the piezoelectric energy harvesters' fabrication process involves several high temperature steps and soaking substrate in various acids which all could damage the polymeric layer. The proposed process flow allows fabricating

the polymeric layer at one of the last stages. Therefore, the polymeric layer is subjected to the minimal defects caused by the other fabrication processes.

b) A modified approach to separate fabricated devices from the silicon substrate was developed. The dicing is the common technique for this purpose. However, dicing overhanging and fully released devices involves a high risk of damaging those devices. In this research, a modified approach was developed to cleave the silicon substrate such that the wafer stays as one piece until the end of the fabrication run and once the fabrication is over, the individual devices could be separated through the cleaving trenches. A few similar techniques were reported in literature but they mostly suffer from either being expensive or having handling issues. (This concept has been published at Journal of Mechanics Engineering and Automation, 3 (2013) 731-738)

c) Various 3D packaging techniques were adapted to improve the yield of the packaging and testing stages. A fabricated individual harvester is very susceptible to break. 3D printing technique was employed to make structures to hold the devices for handling and also testing purposes. Based on literature, this technique could also be used for bio-compatible packaging by taking advantage of bio-compatible materials as raw material for the printer. (These packaging techniques have been presented in a publication at Austin Journal of Nanomedicine and Nanotechnology, Volume 2, Issue 6, 2014)

7.3 Future Work

The presented research in this thesis considered various areas of improving the micro-energy harvesters in terms of design, fabrication, and packaging. In the following, there are some recommendations which could enhance the development of the current research approach.

7.3.1 Flip-chip an electronic chip on the Microchip design

The Microchip configuration in this research is designed for the size of an electronic chip. Designing a PCB with all required electrical components could

be a future work for the current research. This PCB can be flip-chipped on the Microchip harvester (Figure 7.1) using conductive adhesives between the pads (Section 5.3.2). Also, through silicon via holes (TSV) could be used to electrically connect the front and back side of the chip. This assembly provides a proof of concept prototype for real life piezoelectric micro-energy harvesters.

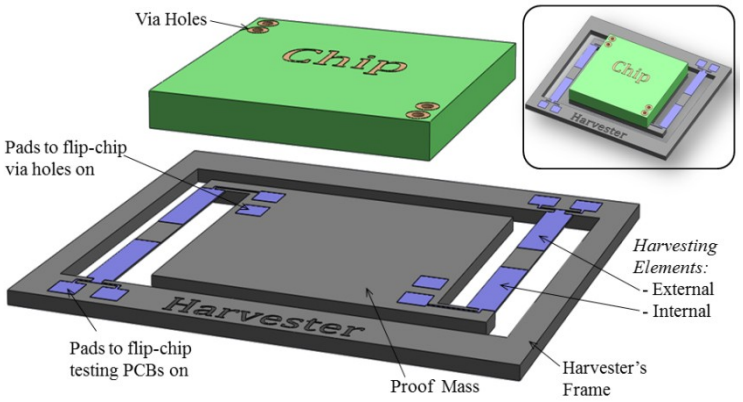


Figure 7.1 – An electronic chip could be installed on the Microchip energy harvester to provide in-situ power supply for the chip.

7.3.2 Multi-degree of freedom micro energy harvesters

Figure 7.2 shows a frequency spectrum of an example multi-degree of freedom energy harvester. If the structural configuration is designed such that the resonant frequency peaks locate close to one another, the resultant energy harvester will be able to harvest in a broader frequency bandwidth.

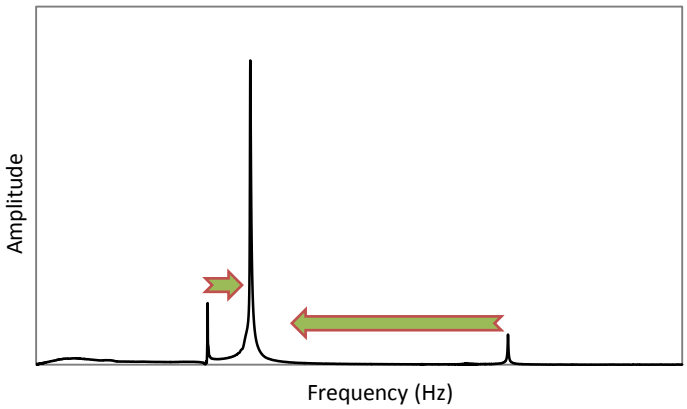


Figure 7.2 – If the resonant frequencies of different mode shapes of a multi degree of freedom structure become closer, a wide band energy harvester could be obtained.

7.3.3 Improving the power output

Based on the literature and the simulation results, the electrical output of the presented energy harvesters could be improved by (a) using PZT film instead of AlN layer and (b) designing a conditioning circuit with the synchronized switch harvesting on inductor (SSHI) concept. Implementing these suggestions and experimentally testing the devices would be a next step to significantly enhance the performance of this work's energy harvesters.

7.3.4 Fine-tuning polymeric membranes with Hydrogel

As presented in Chapter 2, one of the techniques to broaden the frequency bandwidth of the energy harvesters is in-situ tuning. However, the efficiency of the implemented tuning technique in MEMS is the main limitation in this field. A new concept of in-situ tuning technique has been developed, in this work, using the polymeric structures and Hydrogel. Figure 7.3 demonstrates the concept of this resonant frequency tuning method. Polydimethylsiloxane (PDMS) membranes with and without silicon proof masses are fabricated by spin coating on a silicon wafer. ICPRIE process is used to etch through the wafer and reach the bottom of the PDMS layer. This process provides the PDMS membranes. Besides, the required caps and micro-channels are molded in one piece out of PDMS. Eventually, the caps are aligned and bonded on top of the membranes (Figure 7.4). Both caps and membranes are chosen to be PDMS to obtain a strong bond in this case. The Hydrogel solutions with different KOH concentrations are injected through the inlet on the caps. The preliminary vibration test results reveal a clear difference in frequency responses of the devices with two different KOH concentrations (Figure 7.5). It seems that there is a possibility to implement this technique for in-situ passive natural frequency tuning to fine-tune the fabricated oscillators. In addition, the membrane vibration could be actively tuned by fabricating some electrodes on the membrane and apply voltage through the electrodes to the Hydrogel and actuate them. However, the feasibility of these designs needs to be investigated.

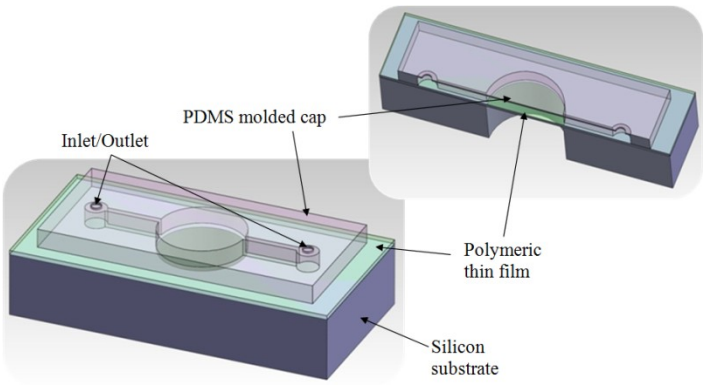


Figure 7.3 – A schematic of the proposed in-situ natural frequency tuning technique.

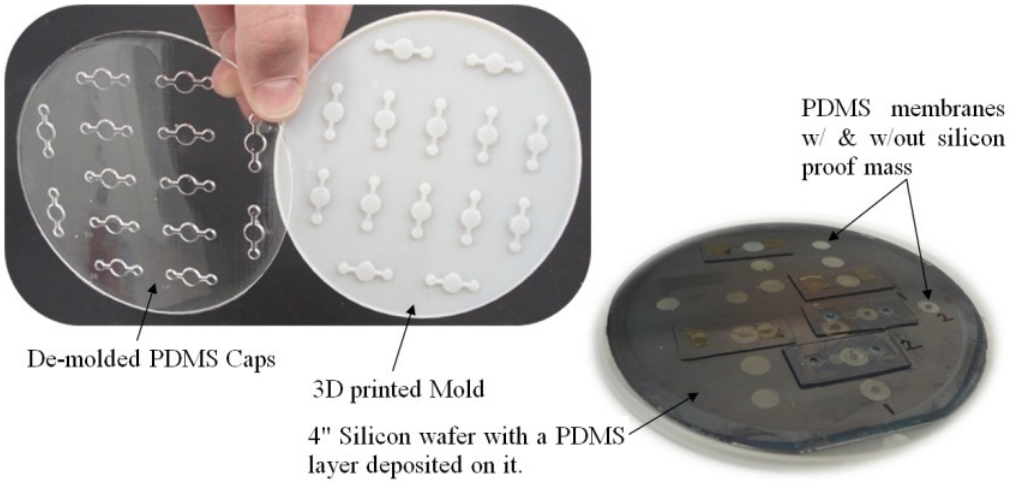


Figure 7.4 – The PDMS caps are molded and then bonded on top of the membranes.

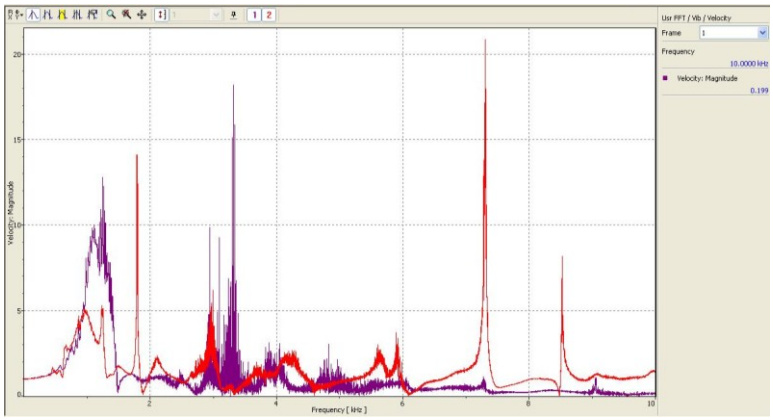


Figure 7.5 – Different concentrations of KOH in the injected solutions caused variation in the frequency outputs.

7.3.5 Alternative methods for XeF_2 etch to eliminate undercut

The XeF_2 etching process is very helpful in terms of being highly selective on silicon. In addition, this process is very desirable comparing to the harsh RIE processes. Even individual devices could be placed in the XeF_2 chamber. However since the process is isotropic, the etching results in large undercuts. In terms of energy harvesters, the size of the proof mass is critical in determining the natural frequency, while, the XeF_2 process etches the side walls of the proof masses reducing their size and weight. One of the main reasons of using XeF_2 in this research was the non-uniformity of ICPRIE process which ended up with some released devices while some others still need to be etched. Here are two recommendations that would help to alleviate the non-uniformity of the silicon etching process.

7.3.5.1 UV released blue tapes

One of the non-uniformity sources in deep RIE is the use of carrier wafer. The carrier wafer is used to hold the main wafer in one piece during the etching process. However, the carrier wafer prevents the backside cooling to be performed properly on the main wafer. Double-sided tapes and crystal bond glue would potentially damage the released devices in the stage of separating the main and carrier wafers. Some kinds of dicing tapes are sensitive to UV light. They provide strong adhesion but release easily under UV exposure[19]. These tapes could be tried instead of carrier wafer to hold the wafer in one piece and finally separate easily without damaging the released devices.

7.3.5.2 Uniform wafer holding mechanism for RIE process

Another source of non-uniformity in deep RIE process is the mechanism of the etching equipment to hold the wafer in the chamber. The available equipment for this research work was a STS[20] silicon etcher which had an o-ring under the wafer and some clamps held the wafer from the edge. The issue of this mechanism is that the wafer is bent due to the pressure applied to the edges

[19] Source: http://dicing-blades.com/dicing-materials/dicing-tapes/
[20] Surface Technology Systems

(Figure 4.6). Therefore, the wafer could be broken if cleaving trenches is used. However, there are other silicon etchers which hold the wafer uniformly around the edge. Therefore if those etchers are used, the wafer will be secured during the etch process.

APPENDICES

A. Fabrication of Lead Zirconate Titanate (PZT) Thin Films

Two piezoelectric layers were exploited in this research: AlN and PZT. Since neither material had pre-developed processes in the NanoFab facility, a long time was spent to develop and adapt both deposition and patterning processes for the two piezoelectric materials. The details about the AlN layer are presented in Chapter 4. However in terms of PZT, some technical difficulties were faced which effected the repeatability of the overall microfabrication process. In the following, the literature is reviewed and also the developed processes for the deposition and patterning of the PZT thin films are elaborated. The repeatability problem is described and also some of the steps taken to alleviate the issue are provided. In this research, PZT (15% PbZrTi (115/52/48)) sol-gel from Mitsubishi Materials Co., Sanda, Japan was used to spin-coat a thin layer of piezoelectric layer on Pt bottom electrodes. The deposition and patterning of PZT have been adapted for this research purposes at the UofA NanoFab.

A.1. PZT Deposition

There are various methods to deposit PZT including Sputtering, Sol-gel, and Metal Organic Chemical Vapor Deposition (MOCVD) techniques. Each of these techniques was reported in literature with a different set of parameters. Therefore, proper parameters need to be developed for a particular condition. Table A.1 summarizes the deposition techniques, their general specifications and the literature in which the techniques are presented. In this research, a sol-gel technique was adapted to deposit PZT layers. The deposition method includes a successive process of spin-coating, bake (paralyzing) and annealing. For spin-

coating and paralyzing bake, Fumehood Aisle 1 was used and for annealing Muffle Furnace was used in NanoFab.

a. Spin-coat PZT sol-gel at 500/3000 RPM spread/spin speed for 5/30 seconds;
b. Bake on hotplate at 350ºC for 1 minute;
c. Repeat steps a and b three times;
d. Anneal in a furnace at 700ºC for 15 minutes;
e. Repeat steps a to d, 5 times to obtain 1.2 µm thick PZT layer.

Table A.1 – Comparing the reported PZT deposition techniques [11].

Deposition Technique	Specifications	Used in literature
Sputtering	• Good for thin layers (usually ≤1µm); • Process requires heat treatment at 475–745℃; • Potential cross contamination risk.	[215, 216]
MOCVD	• Suitable step coverage for 3D applications; • Used to deposit thicknesses of <0.3µm; • Processing temperature at 260–650℃; • Not very commonly used in literature.	[217, 218]
Sol-gel	• Thicker films (≥1µm) are achievable; • Process requires annealing at 450–700℃; • Low risk of contamination.	[219-224]

A.2. PZT Patterning

Based on literature [225, 226], the best approach to etch PZT is dry etch using RIE. However, due to cross contamination issues which might happen in the RIE chambers in the NanoFab, it was not allowed to run RIE for etching PZT layers. Lift-off is another method to pattern PZT thin layers. However, due to the high

annealing temperature required for PZT process and because most of the photoresists would not survive at 700ºC, the lift-off is not a wise choice. The last alternative to pattern a PZT layer is wet etch. Table A.2 shows the wet etching solutions which were reported in literature for PZT patterning. The main etchant is Hydroflouric Acid (HF), however, this solution alone would cause huge undercut (~10:1). Therefore instead of HF, Buffered HF has usually been mixed with Hydrochloric Acid (HCl).

Table A.2 – Reported wet etching process for PZT layers.

No.	Source	Wet etching recipes for PZT	Etch rate	Undercut
1	[227]	1BHF:2HCl:4NH_4Cl:4H_2O	0.016 µm/s	(1.5:1)
2	[227]	1BHF:2HCl:4H_2O	0.013 µm/s	(5.5:1)
3	[228]	17.5 g EDTA tri-sodium 44 g NH_4Cl 800 ml H_2O 62 ml acetic acid (CH_3COOH) 62 ml nitric acid (70% $HN0_3$) 62 ml hydrochloric acid (38% HCl) 6.5 ml BHF (7:l NH_4F : HF)	0.25 µm/min	(1.2: 1)
4	[229]	{1 ml (BOE(6:1)) + 6ml (CH_3COOH) + 6ml (HNO_3(65%)) + 6ml (HCl (35%)) + 4g (NH_4Cl) + 2g ($C_{10}H_{18}N_2O_{10}Na_2$ (EDTA))} in 75ml H_2O	0.2 µm/min	(1.5:1)
5	[230]	1BHF:2HCl:3H_2O	0.01 µm/min	–
6	[231]	$NH_4F + H_2O + HNO_3$	–	–
7	[231]	$NH_4F + H_2O$ + HCl	–	–
8	[225]	Dry Etching by Reactive Ion Etching	$(2–7)\times10^{-3}$ µm/min	–
9	[226]	Deep Reactive Ion Etching using SF_6	0.3 µm/min	–
10	[232]	Dry etching using Inductively Super Magnetron (ISM) plasma source	0.19 µm/min	–

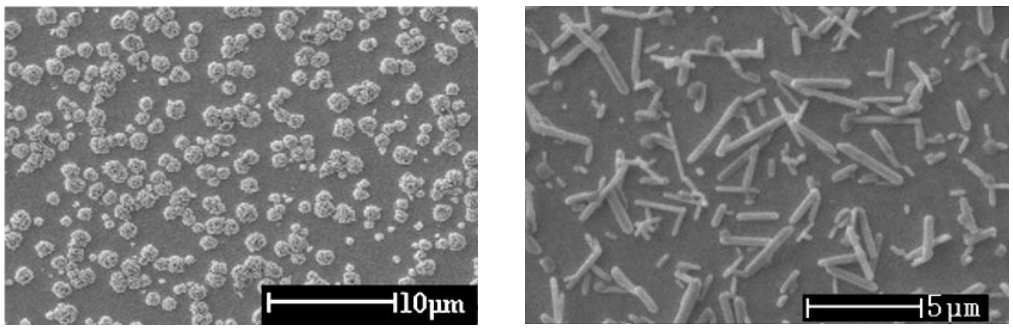
In this research, the first etchant (1BHF:2HCl:4NH_4Cl:4H_2O) presented in Table A.2 is used. The etching recipe is:

a. soak in 1BHF:2HCl:4NH_4Cl:4H_2O solution (the etch rate is 16nm/s);
b. Dry with nitrogen flow;
c. 15 seconds soak in 2HNO_3:1H_2O;
d. Soak and rinse with DI water.

Note that this recipe works the best to etch PZT on Pt layers. The recipe is adapted from [227]. First, soaking in etchant solution results in etching PZT by leaving PbClF on the Pt patterns (Reaction A.1). Then, soaking in HNO_3 changes PbClF to $PbCl_2$ (Reaction A.1.a) which would completely dissolve in DI water at the last step. Figure A.1 demonstrates PbClF on Pt layer after soaking the wafer in the 1BHF:2HCl:4H_2O solution. Figure A.1.b demonstrates $PbCl_2$ on Pt layer after soaking in 2HNO_3:1H_2O solution.

$$Pb(Ti,Zr)O_3 + H^+ + F^- + Cl^- \rightarrow [TiF_6]^{2-} + [ZrF_6]^{2-} + [PbCl_4]^{2-} + PbClF\downarrow + H_2O \quad \text{Reaction A.0.1}$$

$$PbClF + HNO_3 \rightarrow PbCl_2 + Pb^{2+} + NO_3^- + HF \quad \text{Reaction A.0.2}$$



(a) (b)

Figure A.1 – (a) SEM image of the residues on Pt bottom electrode after etching in 1BHF:2HCl:4H_2O solution; (b) SEM image of the reaction product after dipping in 2HNO_3:1H_2O [227].

The resulted patterns of PZT are shown in Figure A.2. Also, the surface quality of the PZT layer is shown by a Zygo image of a top electrode in Figure A.3. Since PZT layer is not reflective, the PZT layer is not shown in Zygo image. The quality of this PZT surface is appreciated when it is compared to a lifted-off PZT

surface (Figure A.4). In addition, Figure A.5 demonstrates a full 4" silicon wafer with one layer of PZT layer (3 spin-coatings) deposited and patterned on Pt film.

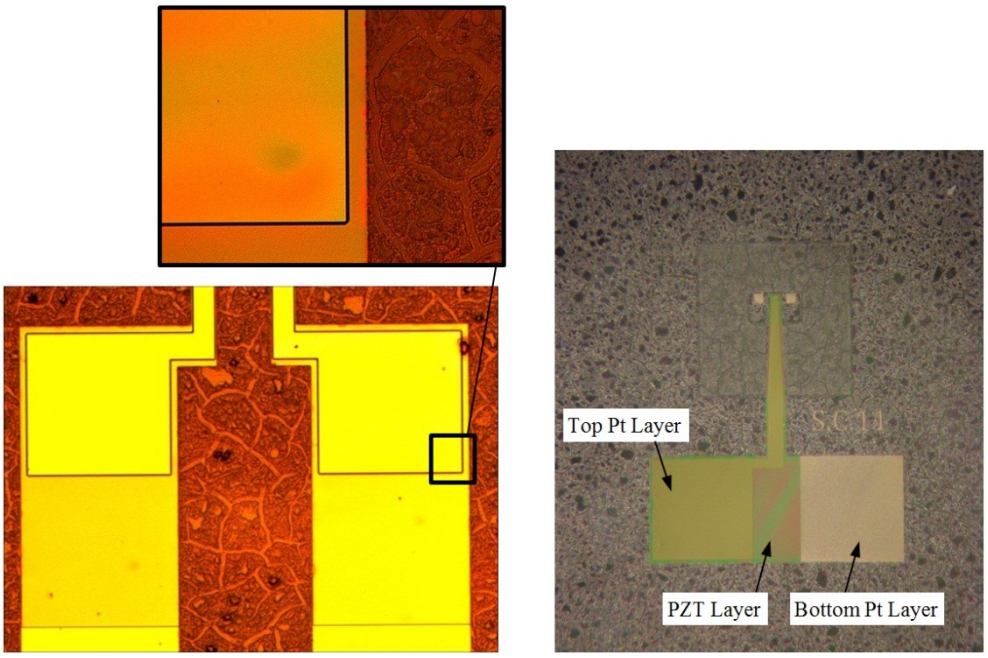


Figure A.2 – Photoresist patterned on PZT layer for top electrode lift-off (Left); An example cantilever before DRIE process.

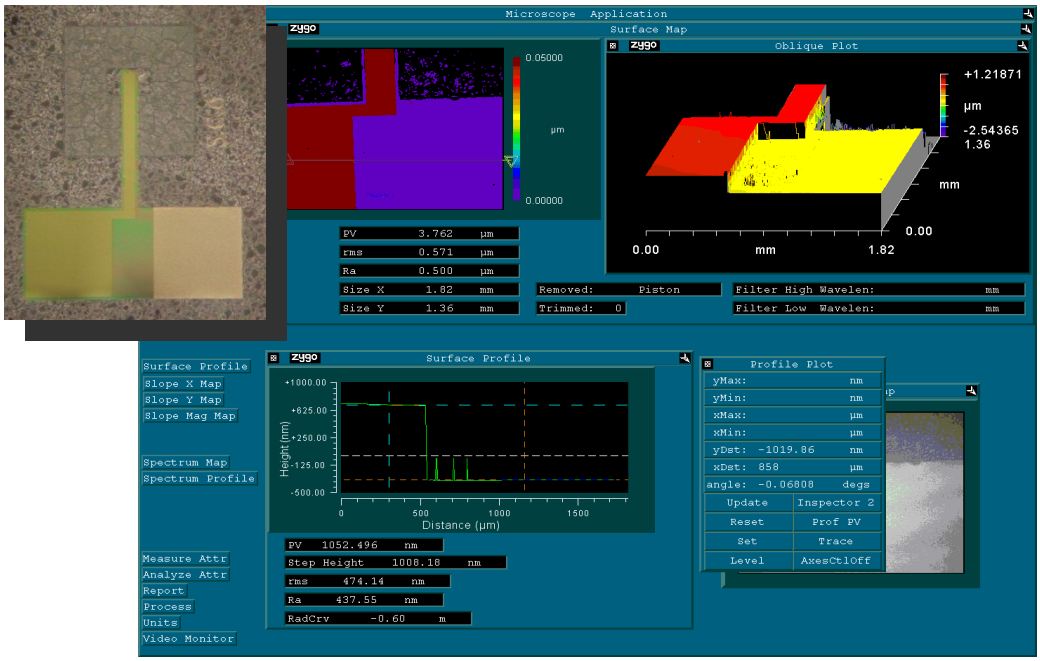


Figure A.3 – Zygo image of a cantilever pads with top and bottom Pt layers and PZT layer. PZT is wet-etched in this case.

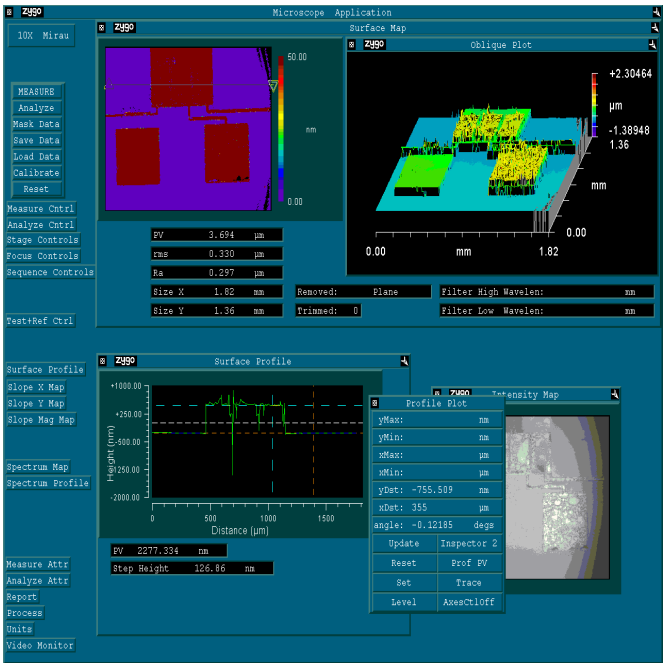


Figure A.4 – Zygo image of a cantilever pads. PZT is lifted off in this case.

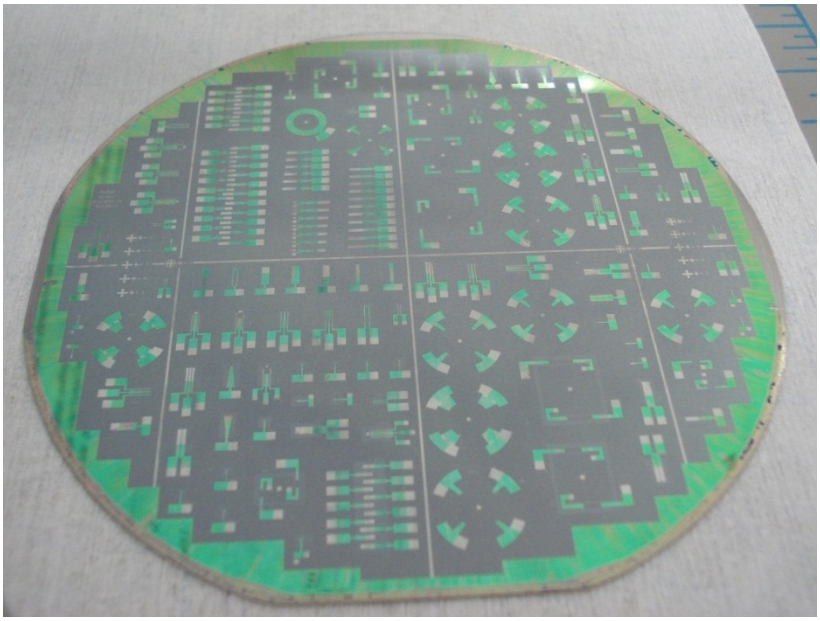


Figure A.5–A silicon wafer with one PZT layer deposited and patterned on Pt thin film.

X-ray diffraction (XRD) is used to characterize the deposited PZT layer. Figure A.6 shows the XRD result for a PZT layer with ~240nm thickness on a Pt thin film. The incident beam could be adjusted to shallow (0.5˚) or deep (4˚) angle. The XRD measured at 0.5˚ reveals that the orientation of the PZT thin film is

(110) due to peak at 2θ angle of ~31.2˚. A 4˚ XRD measurement shows the orientation of Pt layer underneath the PZT which is at 2θ=~40˚ (Figure A.7).

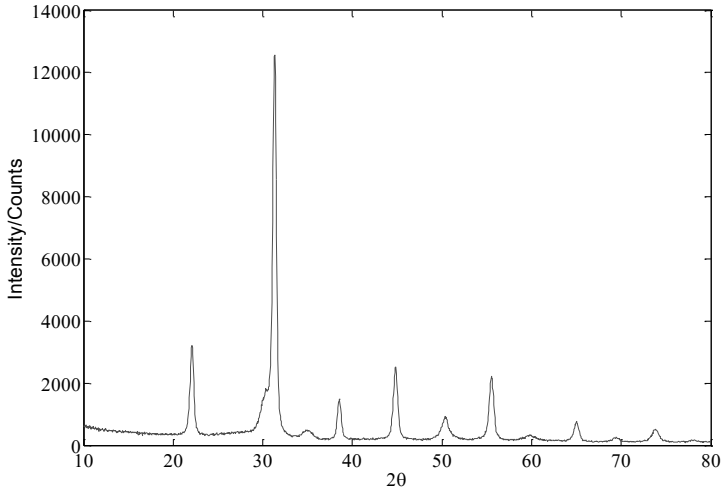


Figure A.6 – Thin film (at 0.5˚) XRD measurement of the deposited PZT thin film.

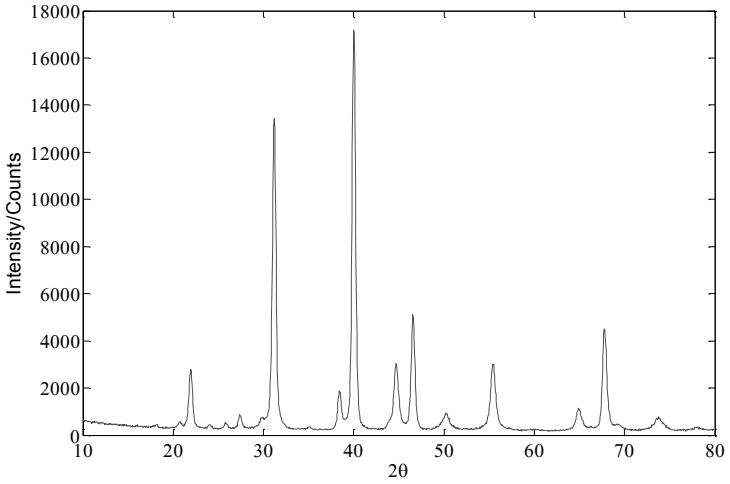


Figure A.7 – Deep (at 4˚) XRD measurement of the deposited PZT thin film.

A.3. PZT Deposition Challenges

During the development run of the energy harvesters, it was noticed that the deposition step of the PZT layer is not consistent. After a certain point, the PZT deposition step failed in most of the microfabrication runs. Therefore, an investigation was performed to figure out the reason for this issue. Usually, the surface of the PZT layer is not clean after annealing stage. X-ray photoelectron spectroscopy (XPS) measurement is performed to find out the reason. Figure A.8 demonstrates the unclean surface of the PZT layer with a SEM image. It seems

that something from the bottom pushes the PZT layer up. In some cases it cracks the surface such as point 1 in Figure A.8. The XPS test results reveal the presence of Chromium at the surface of the PZT layer (Figure A.9). Apparently, the reason of peeling is the migration of Titanium or Chromium molecules (which is used as adhesion layer) from underneath Pt bottom electrode layer.

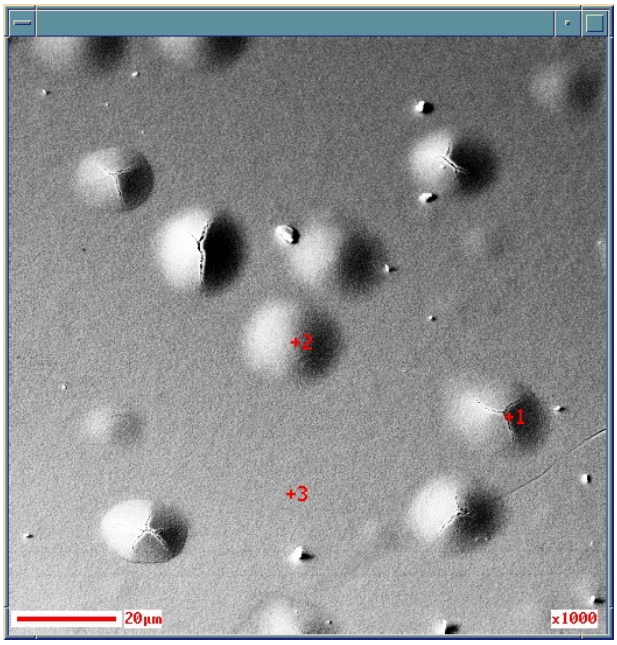


Figure A.8– A SEM image from the top surface of the PZT layer.

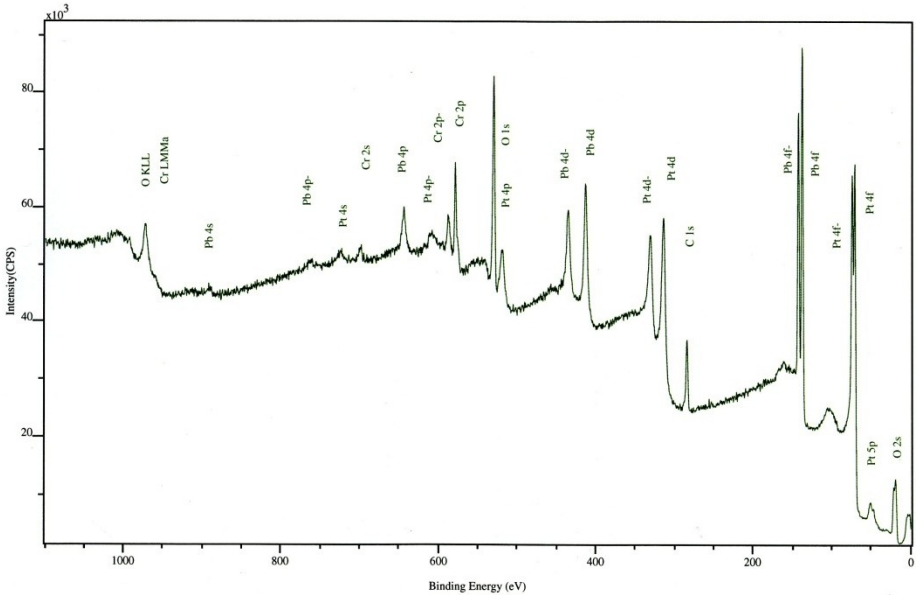


Figure A.9 – XPS test results from Point 1 shown in Figure A.8. The results reveal the presence of Chromium at the surface of the PZT layer.

In some cases, the PZT layer and the bottom electrode were peeled off (Figure A.10). To investigate this issue, a sample of the peeled layer is taken from the middle of the wafer and XPS measurements were done on the bottom surface of peeled layer and also the top surface of the wafer at that location. Results showed no sign of Titanium (or Chromium) which is used as adhesion layer between Pt and silicon oxide layers. Apparently, the reason of peeling is migration of Titanium or Chromium molecules from underneath of Pt layer.

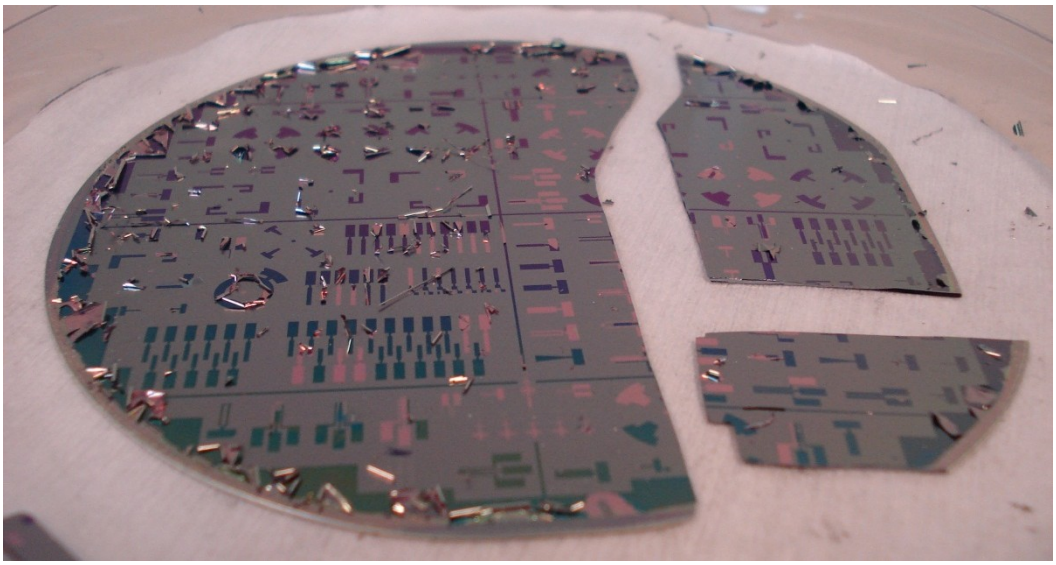


Figure A.10 – In some cases, the PZT layer is peeled off along with the Pt bottom electrode layer at the paralyzing or annealing stage.

Figure A.11 presents an SEM image of the section view of a sample of PZT/Pt/Ti/SiO2/Si layers and also the results of Auger analysis. It seems that the Titanium adhesion layer is not presence at its location which must be right before Pt peak.

Figure A.12 represents a sample of PZT layers deposited on Pt/Ti layer at four consecutive annealing stages (12 spin-coating and paralyzing steps in total). Four sections of the same silicon wafer are used to ensure similar conditions for all samples. Depositing the first layer (3 spin-coatings) had no defects. However, next layers had serious issues.

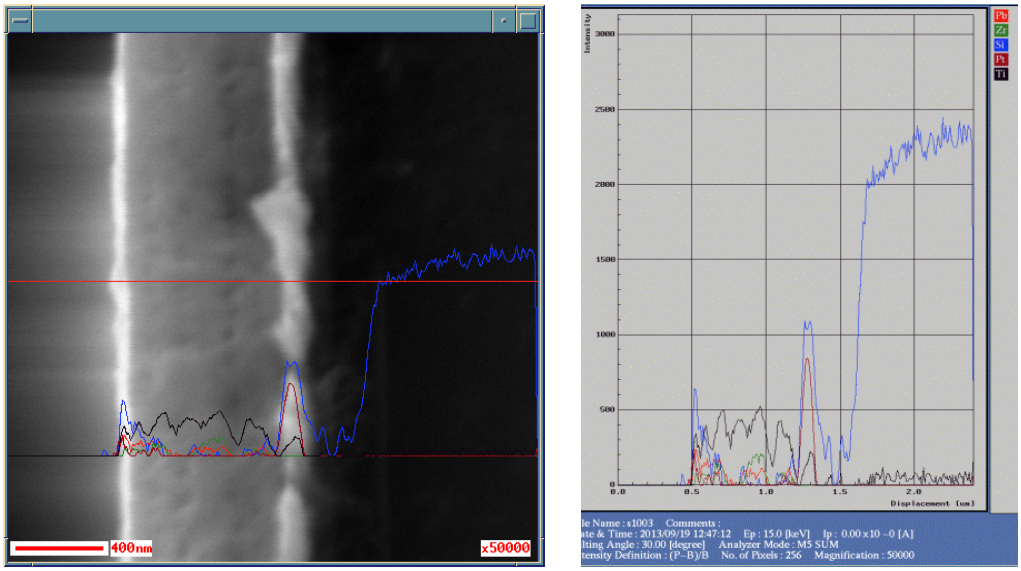


Figure A.11 – SEM image and results of an Auger analysis. The Auger analysis was conducted on a sample of PZT/Pt/Ti/SiO_2/Si layers.

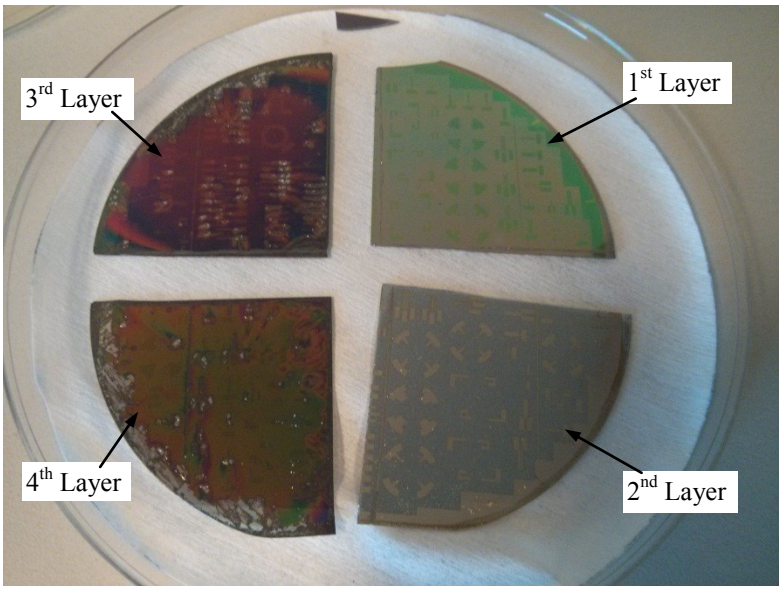


Figure A.12 – PZT deposition had serious issues for more than one layer.

Further research revealed that TiO_2 has actually been used as adhesion layer not Titanium due to the high annealing temperature required for PZT deposition. It seems that the reason why the deposition had no problem at first point was the defect in Nanofab sputtering equipment where it had oxygen leak inside the chamber during the Ti/Pt deposition stage. Once the maintenance was performed

for this equipment the leakage problems is solved and consequently the PZT deposition stopped working due to depositing Ti instead of TiO_2 as adhesion layer. At this point, it was tried to use TiO_2 as adhesion layer fore Pt thin film. Sputtering TiO2 is not a regular process in NanoFab. Therefore, a procedure must have been adapted included purchasing new TiO_2 sputtering targets. Alternatively, the evaporation of TiO_2 and sputtering Ti and then anneal it to obtain TiO_2 were used. In addition, TiW, which is usually used in MEMS industry as adhesion layer instead of Ti, is exploited. Figure A.13 shows one of the peeled regions of PZT on Pt with an adhesion layer of TiO_2 which is deposited by evaporation. Figure A.14 shows the XPS test results done on both PZT and peeled spots. It seems that in the peeled spot there is a mixture of Pt and PZT components. Figure A.15 demonstrates cracking and peeling of PZT when the adhesion layer of Pt was annealed Ti and sputtered TiW. Using Rapid Thermal Annealing (RTA) machine is recommended in literature and PZT supplier to decrease the annealing time from 15 minutes to 1 minute. Therefore, RTA could be replaced instead a box furnace. However, one of the main challenges known in literature regarding the PZT deposition is cracks and pin-holes. One of the methods to prevent cracking in later steps of PZT deposition is sputtering bottom electrode in a high temperature (600ºC) [223]. It seems that more research must be done to characterize the PZT deposition technique based on the existed condition in Nanofab and develop a repeatable process.

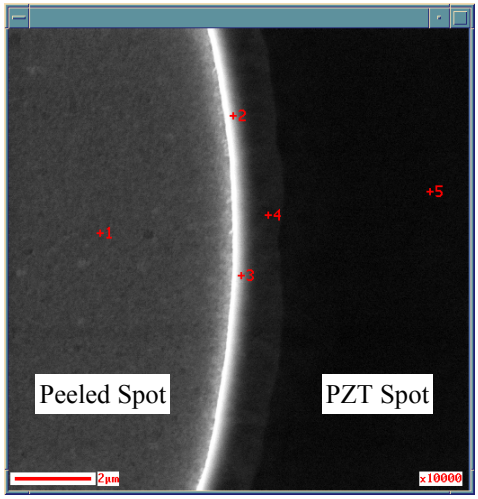
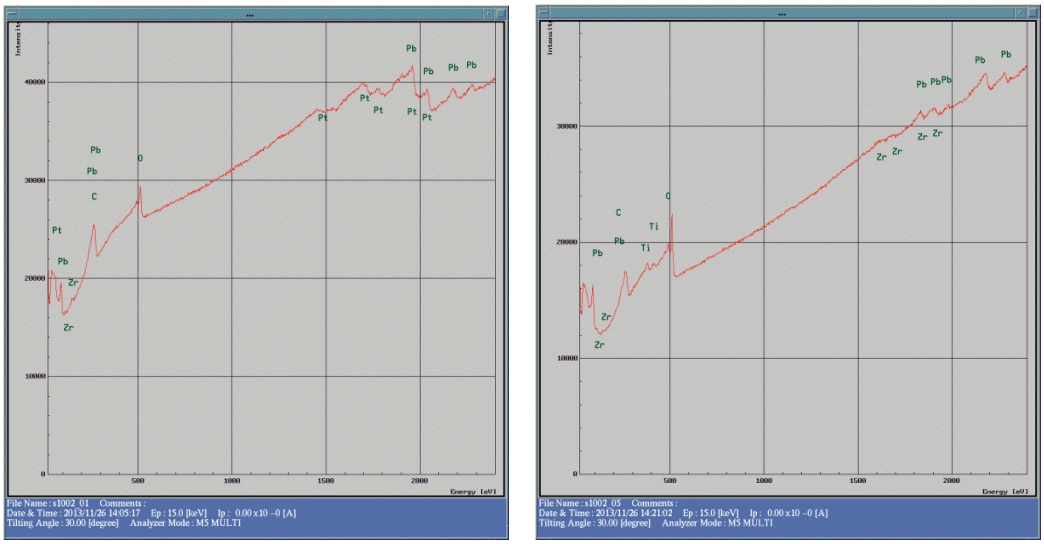
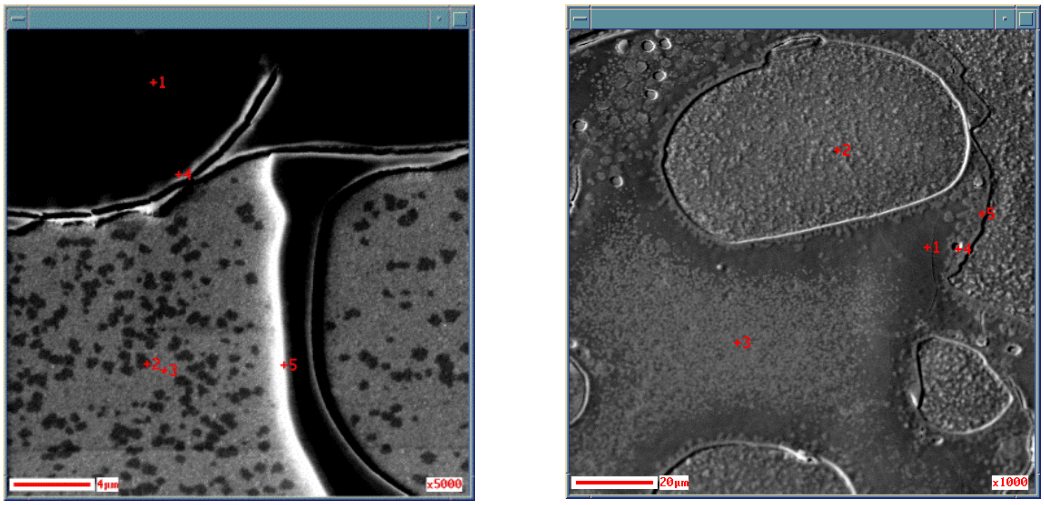


Figure A.13– A SEM image of the peeled sample showing both peeled and PZT spots.



(a) (b)

Figure A.14 – XPS results from the peeled and PZT spots; Point 1 (a) and point 5 (b) shown in Figure A.13.



(a) (b)

Figure A.15 – PZT cracks or peels off when Pt adhesion layer is (a) Ti which is sputtered and then annealed at 600˚C and (b) TiW which is regularly sputtered.

A.4. Summary

It seems that Ti as adhesion layer is not stable at high temperatures tending to migrate through the other layers and, therefore, could not be used for PZT sol gel deposition. However, TiO_2 which is very stable material in high temperatures

must be used as adhesion layer for Pt bottom electrode of PZT layer. Deposition of TiO_2 has multiple methods such as sputtering direct TiO_2, evaporation of TiO_2, and sputtering Ti and then oxidizing by annealing in high temperatures by rapid thermal annealing (RTA) or in a furnace. Apparently, sputtering direct TiO_2 would be the best option eliminating any possible contaminations. With regard to annealing the PZT sol-gel, RTA seems to be a better choice due to much lower annealing time of RTA (1min) comparing to furnace (15min). However, using furnace could lead to acceptable results as well by characterizing all the steps properly. With regard to etching PZT, dry etching using RIE is the most recommended technique. However, limited researchers use dry etching due to contamination issues for the etching chamber. One of the reported wet etching techniques has been successfully adapted in UofA NanoFab. This etching process results in a clean patterns and clean wafer and provides minimal undercut compared to similar techniques.

B. Microfabrication Masks Layout

Figure A.16 shows an image of the general layout of the 5"×5" masks designed using LEdit and exploited for this research microfabrication. An overlap of Masks #1 (Bottom Electrode), #3 (Top Electrode), and #5 (Backside ICPRIE) are shown in Figure A.16. Also, all 7 microfabrication Masks including SU-8 Mask are overlapped and shown in Figure A.17.

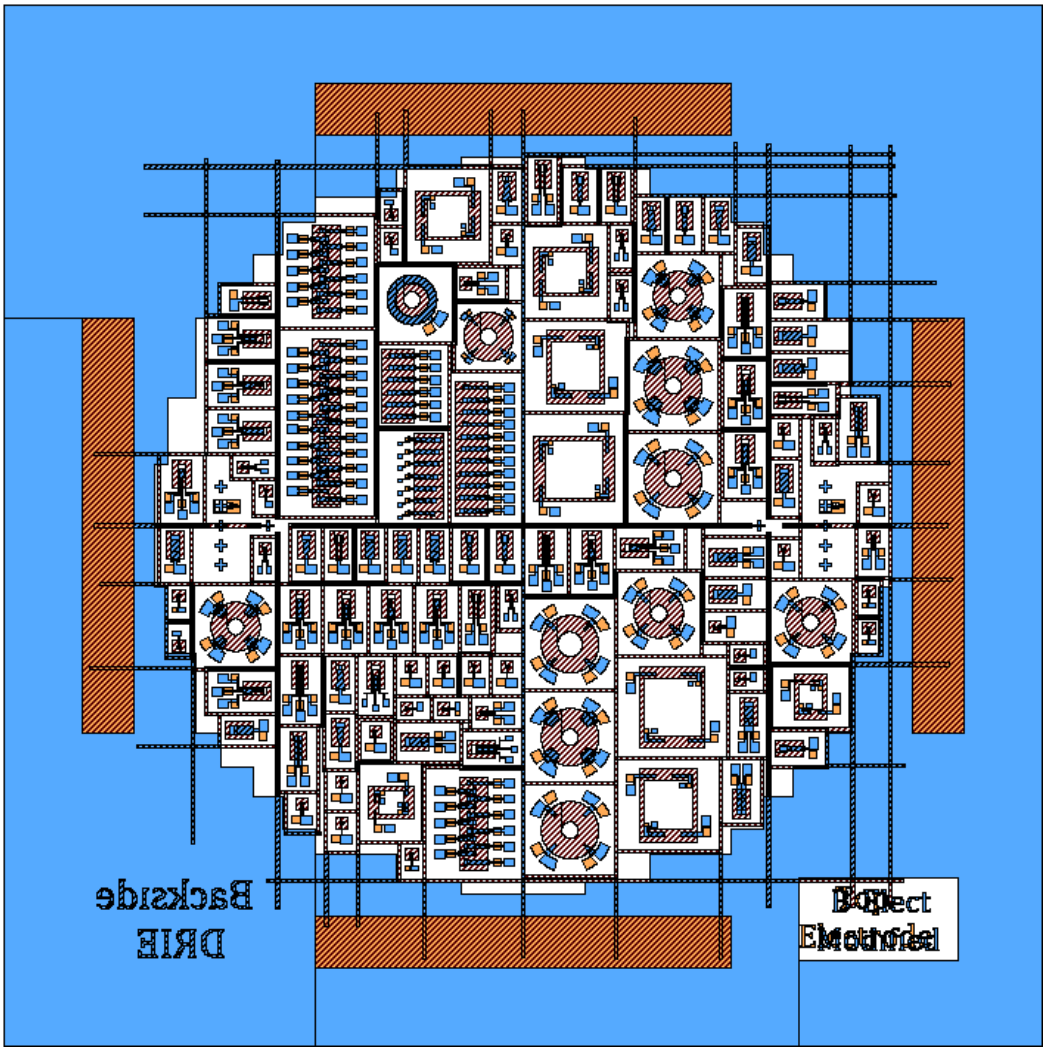


Figure A.16 – An image of the overlapped microfabrication Masks #1,3, and 5.

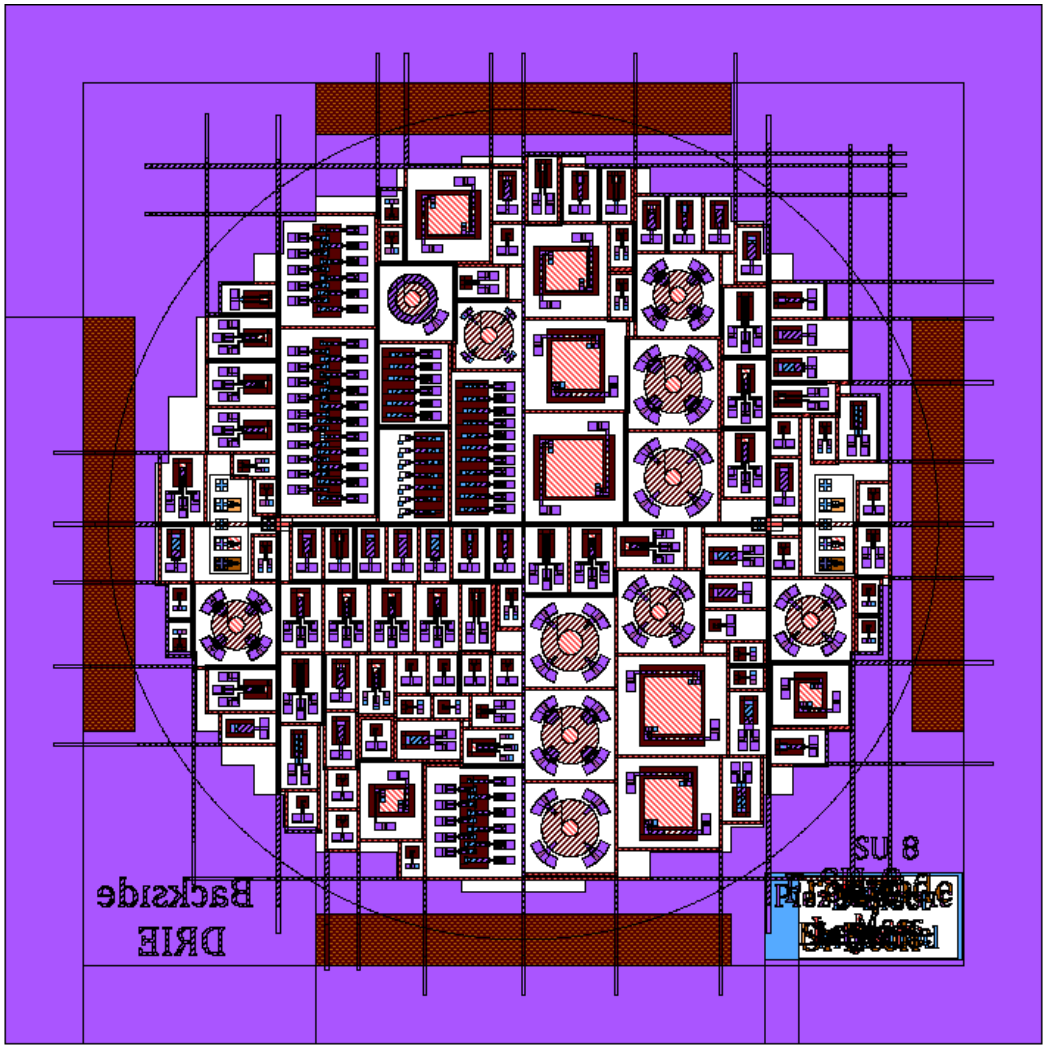


Figure A.17 – An image of overlapped all microfabrication Masks including the SU-8 mask.

C. ANSYS Code for Large Deflection Static Analysis for a MicroChip Energy Harvester

```
Finish
/CLEAR

/TITLE, MicroChip Piezo Harvester - Large Deflection
/PREP7
! ============================
! - Define Element Types
!et,1,SOLID226,1001,,0
et,2,solid186
! ============================
! - Geometry
L=6000e-6                ! Length of Chip
H=500e-6                 ! Thickness of the Mass
h1=22e-6                 ! Thickness of the Beams
h2=1.5e-6                ! Thickness of AlN+2xPt layers
Lpzt=L/3                 ! Length of PZT layer on Sensing/Harvesting region
S=500e-6                 ! Space between the mass and the beams
Stip=500e-6              ! Space from the tip of the beam to the edge of the mass
W=500e-6                 ! Width of the Beam
! ============================
! - Loading values
Fy=10e-3          ! Applied Force, N
! ============================
! Material properties for AlN
MP, DENS, 1, 3260
! Defining the Dielectric (Permittivity) Constants at Constant Strain (Dimensionless)
TB, DPER,1,,0
TBDATA,1, 8.5, 8.5, 8.5, 0, 0, 0

! Defining the Piezoelectric Stress Matrix at Constant Strain (C/m^2)
TB,PIEZ,1,,0
TBDATA,1, 0, 0, -0.57, 0, 0, -0.57
TBDATA,7, 0, 0, 1.39, 0, 0, 0
TBDATA,13, 0, -0.29, 0, -0.29, 0, 0

! Defining the Elasticity matrix in Stiffness Form (N/m^2)
TB,ANEL,1,,0
TBDATA,1, 3.45E11, 1.25E11, 1.20E11, 0, 0, 0
TBDATA,7, 3.45E11, 1.20E11, 0, 0, 0, 3.95E11
TBDATA,13, 0, 0, 0, 1.10E11, 0, 0
TBDATA,19, 1.18E11,0, 1.18E11

tblist,all
! ============================
!  - Material Properties
MP,EX,2,160e9                    ! Young's modulus of beam (Si)
MP,PRXY,2,0.27                   ! Poisson's ratio
MP,DENS,2,2328                   ! Density
! ============================
! Blocks Modeling
BLOCK,-(L/2+S+W),(L/2+S+W),,H,-L/2-Stip,L/2+Stip      ! Create volume for main beam with arms
BLOCK,-(L/2+S),-L/2,,H,-L/2+Stip,L/2+Stip,            ! Create volume for cutting the spacing parts
BLOCK,L/2,(L/2+S),,H,-L/2-Stip,L/2-Stip,              ! Create volume for cutting the spacing parts
VSBV, 1, 2                                            ! Subtracting
VSBV, 4, 3                                            ! Subtracting

BLOCK,-(L/2),(L/2+S+W),,H,L/2,L/2+Stip,               ! Create volume for cutting the extra mass
BLOCK,-(L/2+S+W),(L/2),,H,-(L/2+Stip),-L/2,           ! Create volume for cutting the extra mass
VSBV, 1, 2                                            ! Subtracting
VSBV, 4, 3                                            ! Subtracting
```

```
BLOCK,-(L/2+S+W),-(L/2+S),,H-h1,-L/2+Stip,L/2+Stip,   ! Create volume for cutting underneath the beams
BLOCK,(L/2+S),(L/2+S+W),,H-h1,-(L/2+Stip),L/2-Stip,   ! Create volume for cutting underneath the beams
VSBV, 1, 2                                                  ! Subtracting
VSBV, 4, 3                                                  ! Subtracting

BLOCK,-(L/2+S+W),-(L/2+S),H,H+h2,L/2-Lpzt+Stip,L/2+Stip,     ! Create volume for Harvesting AlN
BLOCK,-(L/2+S+W),-(L/2+S),H,H+h2,-L/2+Stip,-L/2+Stip+L/3,   ! Create volume for Harvesting AlN
BLOCK,(L/2+S),(L/2+S+W),H,H+h2,L/2-Stip,L/2-Stip-Lpzt,      ! Create volume for Harvesting AlN
BLOCK,(L/2+S),(L/2+S+W),H,H+h2,-L/2-Stip+Lpzt,-L/2-Stip,    ! Create volume for Harvesting AlN
!-------------
/VIEW,1,1,2,3
/ANG,1
/REP,FAST
!-------------
WPLANE,-1,-L/2-S,H,0,-L/2-S,H,L/2,-L/2-S,H+h2,0
VSBW, all
WPLANE,-1,L/2+S,H,0,L/2+S,H,L/2,L/2+S,H+h2,0
VSBW, all                                                   ! Cut to separate Beams from Mass

WPLANE,-1,-L/2,H,0,-L/2,H,L/2,-L/2,H+h2,0
VSBW, all
WPLANE,-1,L/2,H,0,L/2,H,L/2,L/2,H+h2,0
VSBW, all                                                   ! Cut to separate small sections from Mass

WPLANE,-1,-(L/2+S+W),H,-L/2+Stip,L/2,H,-L/2+Stip,-(L/2+S+W),H+h2,-L/2+Stip
VSBW, all
WPLANE,-1,(L/2+S+W),H,L/2-Stip,-L/2,H,L/2-Stip,(L/2+S+W),H+h2,L/2-Stip
VSBW, all                                                   ! Cut to separate Tip of Beams from Mass

WPLANE,-1,(L/2+S+W),H,-L/2-Stip+Lpzt,-L/2,H,-L/2-Stip+Lpzt,(L/2+S+W),H+h2,-L/2-Stip+Lpzt
VSBW, all
WPLANE,-1,(L/2+S+W),H,-L/2+Lpzt+Stip,-L/2,H,-L/2+Lpzt+Stip,(L/2+S+W),H+h2,-L/2+Lpzt+Stip
VSBW, all
WPLANE,-1,-(L/2+S+W),H,L/2-Lpzt-Stip,L/2,H,L/2-Lpzt-Stip,-(L/2+S+W),H+h2,L/2-Lpzt-Stip
VSBW, all
WPLANE,-1,-(L/2+S+W),H,L/2+Stip-Lpzt,L/2,H,L/2+Stip-Lpzt,-(L/2+S+W),H+h2,L/2+Stip-Lpzt
VSBW, all                                                   ! Cut to separate PZT layer from the beam

vglue,all                                                   ! Glue layers and mass
!----------------
/VIEW,1,1,2,3
/ANG,1
/REP,FAST
/AUTO,1
/REP,FAST
!----------------
! ====================================

hptcreate,area,149,1001,coord,0,0,0         ! hard point for 2nd Mode
! ============================
!  - Meshing
mat,1
type,2
esize,15*h2
vmesh,1 !$ esys,11                ! Generate mesh within the PZT layers
vmesh,5 !$ esys,11
vmesh,2 !$ esys,11
vmesh,11 !$ esys,11
vmesh,37 !$ esys,11
vmesh,28 !$ esys,11
vmesh,3 !$ esys,11
vmesh,40 !$ esys,11

mat,2                             ! Generate mesh within beams
type,2
esize,5*15*h2
```

```
vmesh,4
vmesh,9
vmesh,24
vmesh,25
vmesh,36
vmesh,38
vmesh,39
vmesh,41
vmesh,42
vmesh,43
vmesh,44
vmesh,45

esize,H                 ! Generate mesh within the proof mass
vmesh,14
vmesh,22
vmesh,27
vmesh,31
vmesh,34
mshape,1,3D
vmesh,10
vmesh,29
vmesh,8
vmesh,46
vmesh,47
vmesh,48
! ========================
!  - Loading
asel,s,,,11
asel,a,,,179
nsla,r,1
d,all,Ux,0,,,,Uy,Uz
nsel,all

asel,s,,,2
asel,a,,,182
nsla,r,1
d,all,Ux,0,,,,Uy,Uz
nsel,all

finish
! ====================================
/SOLU                   ! Static Large Deflection Simulation
ANTYPE,static
nlgeom,on               ! Turn on non-linear geometry analysis
autots,on               ! Auto time stepping
nsubst,5,1000,1         ! Size of first substep=1/5 of the total load, max # substeps=1000, min #
substeps=1
outres,all,all          ! Save results of all iterations

nsel,s,loc,Y,0          ! Loading for 2nd Mode
nsel,r,loc,X,0
nsel,r,loc,Z,0
F,all,FY,Fy
allsel,all

solve

FINISH
/POST1
/DSCALE,ALL,AUTO
/EFACET,1
PLNSOL, U,Y, 0,1.0
```

D. ANSYS Code for Coupled Field Analysis for Piezoelectric Elements

```
finish
/CLEAR

/TITLE, Piezo Analysis
/PREP7
! ============================
! - Define Element Types
et,1,SOLID226,1001,,0
et,2,solid45
! ============================
! - Geometry
L=2000e-6
W=520e-6
h1=10e-6
h2=1.1e-6
! ============================
! - Loading values
Uy=17e-6              ! Tip displacement, m
! ============================
! Material properties for AlN
MP, DENS, 1, 3260
! DEFINING THE DIELECTRIC (PERMITTIVITY) CONSTANTS AT CONSTANT STRAIN (Dimensionless)
TB, DPER,1,,0
TBDATA,1, 8.5, 8.5,8.5, 0, 0, 0

! DEFINING THE PIEZOELECTRIC STRESS MATRIX AT CONSTANT STRAIN (C/m^2)
TB,PIEZ,1,,0
TBDATA,1, 0, 0, -0.57, 0, 0, -0.57
TBDATA,7, 0, 0, 1.39, 0, 0, 0
TBDATA,13, 0, -0.29, 0, -0.29, 0, 0

! DEFINING THE ELASTICITY MATRIX IN STIFFNESS FORM (N/m^2)
TB,ANEL,1,,0
TBDATA,1, 3.45E11, 1.25E11, 1.20E11, 0, 0, 0
TBDATA,7, 3.45E11, 1.20E11, 0, 0, 0, 3.95E11
TBDATA,13, 0, 0, 0, 1.10E11, 0, 0
TBDATA,19, 1.18E11, 0, 1.18E11

tblist,all
! ============================
!  - Material Properties
MP,EX,2,160e9                    ! Young's modulus of beam (Si)
MP,PRXY,2,0.27                   ! Poisson's ratio
MP,DENS,2,2328                   ! Density
! ============================
! Blocks Modeling
BLOCK,0,L,-h2,0,-W,0,        ! create volume for Lower AlN  => V1
BLOCK,0,L,0,h2,-W,0,         ! create volume for upper AlN  => V3

vglue,all                ! Glue layers and mass

K,101,0,0,0
K,102,L,0,0
K,103,0,0,-W
K,104,L,0,-W
```

```
CSKP,30,0,101,102,103
CSYS, 0
CSKP,31,0,103,104,101
CSYS, 0
! ============================
!  - Meshing
mat,1
type,1
esize,12*h2
VATT,1,,1,31
vmesh,1                  ! Generate mesh within lower AlN layer

mat,1
type,1
esize,12*h2
VATT,1,,1,30
vmesh,3                  ! Generate mesh within upper AlN layer
! ============================
! - Define Electrodes
nsel,s,loc,x,L
*get,ntip,node,0,num,min    ! Get master node at beam tip
!
nelec = 1                ! Number of electrodes on top surface
*dim,ntop,array,nelec
l1 = 0                   ! Initialize electrode locations
l2 = L/nelec
i=1
nsel,s,loc,y,h2
nsel,r,loc,x,l1,l2
cp,i,volt,all
*get,ntop(i),node,0,num,min  ! Get master node on top electrode
! ============================
!  - Loading
nsel,s,loc,y,-h2          ! Define bottom electrode of upper PZT layer
d,all,volt,0              ! Ground bottom electrode

nsel,s,loc,x,0            ! Clamp left end of bimorph
d,all,Ux,0,,,,Uy,Uz
nsel,all

finish
! ============================
! - Solution
/SOLU
antype,static

ASEL,S,LOC,X,L
NSLA,R,1
NSEL,R,LOC,Y,-h2
D,All, ,Uy, , , ,UY, , , , ,
allsel,all

solve
fini

/POST1
/com,
/com, Sensor mode results:
/com, - Electrode %i%  Voltage = %volt(ntop(i))% (Volt)
```

Bibliography

[1] Roundy S, Wright PK. A piezoelectric vibration based generator for wireless electronics. Smart Mater Struct. 2004;13:1131-42.

[2] Gautschi G. Piezoelectric Sensorics: Force Strain Pressure Acceleration and Acoustic Emission Sensors Materials and Amplifiers: Springer; 2011.

[3] Priya S, Inman DJ. Energy harvesting technologies: Springer; 2009.

[4] Roundy S, Wright PK, Rabaey J. A study of low level vibrations as a power source for wireless sensor nodes. Comput Commun. 2003;26:1131-44.

[5] Sodano HA, Inman, D. J., and Park, G. A review of power harvesting from vibration using piezoelectric materials. Shock and Vibration Digest 2004;36:197–205.

[6] Beeby SP, Tudor MJ, White NM. Energy harvesting vibration sources for microsystems applications. Meas Sci Technol. 2006;17:R175-R95.

[7] Priya S. Advances in energy harvesting using low profile piezoelectric transducers. J Electroceram. 2007;19:167-84.

[8] Anton SR, Sodano HA. A review of power harvesting using piezoelectric materials (2003-2006). Smart Mater Struct. 2007;16:R1-R21.

[9] Cook-Chennault KA, Thambi N, Sastry AM. Powering MEMS portable devices - a review of non-regenerative and regenerative power supply systems with special emphasis on piezoelectric energy harvesting systems. Smart Materials and Structures. 2008;17.

[10] Kim HS, Kim JH, Kim J. A Review of Piezoelectric Energy Harvesting Based on Vibration. Int J Precis Eng Man. 2011;12:1129-41.

[11] Rezaei M, Lueke J, Raboud D, Moussa W. Challenges in fabrication and testing of piezoelectric MEMS with a particular focus on energy harvesters. Microsyst Technol. 2013;19:1195-219.

[12] Jaffe B, Cook WR, Jaffe HL. Piezoelectric ceramics: Academic Press; 1971.

[13] Shen D, Choe SY, Kim DJ. Analysis of piezoelectric materials for energy harvesting devices under high-g vibrations. Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers. 2007;46:6755-60.

[14] Muralt P. PZT thin films for microsensors and actuators: Where do we stand? Ieee T Ultrason Ferr. 2000;47:903-15.

[15] Wu X, Vanderbilt D, Hamann DR. Systematic treatment of displacements, strains, and electric fields in density-functional perturbation theory. Phys Rev B. 2005;72.

[16] Roundy SJ. Energy Scavenging for Wireless Sensor Nodes with a Focus on Vibration to Electricity Conversion [PhD Dissertation]. Mechanical Engineering: University of California, Berkeley; 2003.

[17] Park J-h. Development of MEMS Piezoelectric Energy Harvesters [PhD Dissertation]. ProQuest LLC.: Materials Engineering, Auburn University; 2010.

[18] Glynne-Jones P, Beeby SP, White NM. Towards a piezoelectric vibration-powered microgenerator. Iee P-Sci Meas Tech. 2001;148:68-72.

[19] Demir I, Olson AL, Skinner JL, Richards CD, Richards RF, Bahr DF. High strain behavior of composite thin film piezoelectric membranes. Microelectron Eng. 2004;75:12-23.

[20] Lu F, Lee HP, Lim SP. Modeling and analysis of micro piezoelectric power generators for micro-electromechanical-systems applications. Smart Mater Struct. 2004;13:57-63.

[21] Jeon YB, Sood R, Jeong JH, Kim SG. MEMS power generator with transverse mode thin film PZT. Sensor Actuat a-Phys. 2005;122:16-22.

[22] Fang HB, Liu JQ, Xu ZY, Dong L, Wang L, Chen D, et al. Fabrication and performance of MEMS-based piezoelectric power generator for vibration energy harvesting. Microelectron J. 2006;37:1280-4.

[23] Marzencki M, Ammar Y, Basrour S. Design, Fabrication and Characterization of a Piezoelectric Microgenerator Including a Power Management Circuit. DTIP of MEMS & MOEMS 2007. Stresa, Italy2007.

[24] Shen D, Park JH, Ajitsaria J, Choe SY, Wikle HC, Kim DJ. The design, fabrication and evaluation of a MEMS PZT cantilever with an integrated Si proof mass for vibration energy harvesting. J Micromech Microeng. 2008;18.

[25] Lee BS, Lin SC, Wu WJ, Wang XY, Chang PZ, Lee CK. Piezoelectric MEMS generators fabricated with an aerosol deposition PZT thin film. J Micromech Microeng. 2009;19.

[26] Elfrink R, Kamel TM, Goedbloed M, Matova S, Hohlfeld D, van Andel Y, et al. Vibration energy harvesting with aluminum nitride-based piezoelectric devices. J Micromech Microeng. 2009;19.

[27] Erturk A, Inman DJ. Piezoelectric Energy Harvesting: Wiley; 2011.

[28] Ottman GK, Hofmann HF, Bhatt AC, Lesieutre GA. Adaptive piezoelectric energy harvesting circuit for wireless remote power supply. Ieee T Power Electr. 2002;17:669-76.

[29] Lefeuvre E, Badel A, Richard C, Guyomar D. Piezoelectric energy harvesting device optimization by synchronous electric charge extraction. J Intel Mat Syst Str. 2005;16:865-76.

[30] Kong N, Ha DS, Erturk A, Inman DJ. Resistive Impedance Matching Circuit for Piezoelectric Energy Harvesting. J Intel Mat Syst Str. 2010;21:1293-302.

[31] Lallart M, Anton SR, Inman DJ. Frequency Self-tuning Scheme for Broadband Vibration Energy Harvesting. J Intel Mat Syst Str. 2010;21:897-906.

[32] Shahruz SM. Design of mechanical band-pass filters for energy scavenging. J Sound Vib. 2006;292:987-98.

[33] Shahruz SM. Limits of performance of mechanical band-pass filters used in energy scavenging. J Sound Vib. 2006;293:449-61.

[34] Xue HA, Hu YT, Wang QM. Broadband piezoelectric energy harvesting devices using multiple bimorphs with different operating frequencies. Ieee T Ultrason Ferr. 2008;55:2104-8.

[35] Ferrari M, Ferrari V, Guizzetti M, Marioli D, Taroni A. Piezoelectric multifrequency energy converter for power harvesting in autonomous microsystems. Sensor Actuat a-Phys. 2008;142:329-35.

[36] Liu JQ, Fang HB, Xu ZY, Mao XH, Shen XC, Chen D, et al. A MEMS-based piezoelectric power generator array for vibration energy harvesting. Microelectron J. 2008;39:802-6.

[37] Sari I, Balkan T, Kulah H. An electromagnetic micro energy harvester based on an array of parylene cantilevers. J Micromech Microeng. 2009;19.

[38] Lien IC, Shu YC. Array of Piezoelectric Energy Harvesters. Active and Passive Smart Structures and Integrated Systems 2011. 2011;7977.

[39] Tang LH, Yang YW, Soh CK. Toward Broadband Vibration-based Energy Harvesting. J Intel Mat Syst Str. 2010;21:1867-97.

[40] Zhu DB, Tudor MJ, Beeby SP. Strategies for increasing the operating frequency range of vibration energy harvesters: a review. Meas Sci Technol. 2010;21.

[41] Wu X, Lin J, Kato S, Zhang K, Ren T, Liu L. A frequency adjustable vibration energy harvester. Proceedings of PowerMEMS. 2008:245-8.

[42] Leland ES, Wright PK. Resonance tuning of piezoelectric vibration energy scavenging generators using compressive axial preload. Smart Mater Struct. 2006;15:1413-20.

[43] Remtema T, Lin LW. Active frequency tuning for micro resonators by localized thermal stressing effects. Sensor Actuat a-Phys. 2001;91:326-32.

[44] Syms RRA. Electrothermal frequency tuning of folded and coupled vibrating micromechanical resonators. J Microelectromech S. 1998;7:164-71.

[45] Eichhorn C, Goldschmidtboeing F, Woias P. Bidirectional frequency tuning of a piezoelectric energy converter based on a cantilever beam. J Micromech Microeng. 2009;19:094006.

[46] Mukherjee R. MEMS resonator using frequency tuning. Google Patents; 2007.

[47] Zhu D, Roberts S, Tudor J, Beeby S. Closed loop frequency tuning of a vibration-based micro-generator. PowerMEMS 2008. Sendai, Japan: PowerMEMS 2008+ microEMS2008; 2008. p. 229-32.

[48] Nguyen SD, Halvorsen E, Jensen GU. Wideband MEMS Energy Harvester Driven by Colored Noise. J Microelectromech S. 2013;22:892-900.

[49] Hajati A, Kim SG. Ultra-wide bandwidth piezoelectric energy harvesting. Appl Phys Lett. 2011;99.

[50] Eichhorn C, Tchagsim R, Wilhelm N, Woias P. A smart and self-sufficient frequency tunable vibration energy harvester. J Micromech Microeng. 2011;21.

[51] Liu HC, Lee CK, Kobayashi T, Tay CJ, Quan CG. Investigation of a MEMS piezoelectric energy harvester system with a frequency-widened-bandwidth mechanism introduced by mechanical stoppers. Smart Materials and Structures. 2012;21.

[52] Erturk A, Hoffmann J, Inman DJ. A piezomagnetoelastic structure for broadband vibration energy harvesting. Appl Phys Lett. 2009;94.

[53] Arrieta AF, Hagedorn P, Erturk A, Inman DJ. A piezoelectric bistable plate for nonlinear broadband energy harvesting. Appl Phys Lett. 2010;97.

[54] Ferrari M, Ferrari V, Guizzetti M, Ando B, Baglio S, Trigona C. Improved energy harvesting from wideband vibrations by nonlinear piezoelectric converters. Sensor Actuat a-Phys. 2010;162:425-31.

[55] Liu WQ, Badel A, Formosa F, Wu YP, Agbossou A. Novel piezoelectric bistable oscillator architecture for wideband vibration energy harvesting. Smart Materials and Structures. 2013;22.

[56] Nguyen SD, Halvorsen E, Paprotny I. Bistable springs for wideband microelectromechanical energy harvesters. Appl Phys Lett. 2013;102.

[57] Stanton SC, McGehee CC, Mann BP. Reversible hysteresis for broadband magnetopiezoelastic energy harvesting. Appl Phys Lett. 2009;95.

[58] Nguyen DS, Halvorsen E, Jensen GU, Vogl A. Fabrication and characterization of a wideband MEMS energy harvester utilizing nonlinear springs. J Micromech Microeng. 2010;20.

[59] Soliman MSM, Abdel-Rahman EM, El-Saadany EF, Mansour RR. A Design Procedure for Wideband Micropower Generators. J Microelectromech S. 2009;18:1288-99.

[60] Liu HC, Tay CJ, Quan CG, Kobayashi T, Lee C. Piezoelectric MEMS Energy Harvester for Low-Frequency Vibrations With Wideband Operation Range and Steadily Increased Output Power. J Microelectromech S. 2011;20:1131-42.

[61] Le CP, Halvorsen E. MEMS electrostatic energy harvesters with end-stop effects. J Micromech Microeng. 2012;22.

[62] Kim JE, Kim YY. Power enhancing by reversing mode sequence in tuned mass-spring unit attached vibration energy harvester. Aip Adv. 2013;3.

[63] Abdelkefi A, Najar F, Nayfeh AH, Ben Ayed S. An energy harvester using piezoelectric cantilever beams undergoing coupled bending-torsion vibrations. Smart Mater Struct. 2011;20.

[64] Erturk A, Renno JM, Inman DJ. Modeling of Piezoelectric Energy Harvesting from an L-shaped Beam-mass Structure with an Application to UAVs. J Intel Mat Syst Str. 2009;20:529-44.

[65] Kim IH, Jung HJ, Lee BM, Jang SJ. Broadband energy-harvesting using a two degree-of-freedom vibrating body. Appl Phys Lett. 2011;98.

[66] Forrest SR. The path to ubiquitous and low-cost organic electronic appliances on plastic. Nature. 2004;428:911-8.

[67] Becker H, Gartner C. Polymer microfabrication technologies for microfluidic systems. Anal Bioanal Chem. 2008;390:89-111.

[68] Aktary M, Jensen MO, Westra KL, Brett MJ, Freeman MR. High-resolution pattern generation using the epoxy novolak SU-8 2000 resist by electron beam lithography. J Vac Sci Technol B. 2003;21:L5-L7.

[69] Genolet G, Brugger J, Despont M, Drechsler U, Vettiger P, de Rooij NF, et al. Soft, entirely photoplastic probes for scanning force microscopy. Rev Sci Instrum. 1999;70:2398-401.

[70] Madou MJ. Fundamentals of Microfabrication: The Science of Miniaturization, Second Edition: Taylor & Francis; 2002.

[71] Seidemann V, Butefisch S, Buttgenbach S. Fabrication and investigation of in-plane compliant SU8 structures for MEMS and their application to micro valves and micro grippers. Sensor Actuat a-Phys. 2002;97-8:457-61.

[72] Schmid S, Wagli P, Hierold C. Biosensor based on All-Polymer Resonant Microbeams. Micro Electro Mechanical Systems, 2009 MEMS 2009 IEEE 22nd International Conference on2009. p. 300-3.

[73] Sameoto D, Tsang SH, Parameswaran M. Polymer MEMS processing for multi-user applications. Sensor Actuat a-Phys. 2007;134:457-64.

[74] Guerin LJ, Bossel M, Demierre M, Calmes S, Renaud P. Simple and low cost fabrication of embedded microchannels by using a new thick-film photoplastic. Transducers 97 - 1997 International Conference on Solid-State Sensors and Actuators, Digest of Technical Papers, Vols 1 and 2. 1997:1419-22.

[75] Yang R, Wang WJ. Out-of-plane polymer refractive microlens fabricated based on direct lithography of SU-8. Sensor Actuat a-Phys. 2004;113:71-7.

[76] Llobera A, Seidemann V, Plaza JA, Cadarso VJ, Buttgenbach S. SU-8 optical accelerometers. J Microelectromech S. 2007;16:111-21.

[77] Schmid S, Wendlandt M, Junker D, Hierold C. Nonconductive polymer microresonators actuated by the Kelvin polarization force. Appl Phys Lett. 2006;89.

[78] Dai W, Lian K, Wang WJ. Design and fabrication of a SU-8 based electrostatic microactuator. Microsyst Technol. 2007;13:271-7.

[79] Nguyen NT, Ho SS, Low CLN. A polymeric microgripper with integrated thermal actuators. J Micromech Microeng. 2004;14:969-74.

[80] Truong TQ, Nguyen NT. A polymeric piezoelectric micropump based on lamination technology. J Micromech Microeng. 2004;14:632-8.

[81] Airoudj A, Debarnot D, Beche B, Poncin-Epaillard F. Development of an optical ammonia sensor based on polyaniline/epoxy resin (SU-8) composite. Talanta. 2009;77:1590-6.

[82] Duc TC, Lau GK, Creemer JF, Sarro PM. Electrothermal Microgripper With Large Jaw Displacement and Integrated Force Sensors. J Microelectromech S. 2008;17:1546-55.

[83] Chronis N, Lee LP. Electrothermally activated SU-8 microgripper for single cell manipulation in solution. J Microelectromech S. 2005;14:857-63.

[84] Panergo R, Huang CS, Liu CS, Reinhall PG, Wang WC. Resonant polymeric waveguide cantilever integrated for optical scanning. J Lightwave Technol. 2007;25:850-60.

[85] Mathers A, Moon KS, Yi JG. A Vibration-Based PMN-PT Energy Harvester. Ieee Sens J. 2009;9:731-9.

[86] Prashanthi K, Naresh M, Seena V, Thundat T, Rao VR. A Novel Photoplastic Piezoelectric Nanocomposite for MEMS Applications. J Microelectromech S. 2012;21:259-61.

[87] Rho J, Kim SJ, Heo W, Lee NE, Lee HS, Ahn JH. PbZrxTi1-xO3 Ferroelectric Thin-Film Capacitors for Flexible Nonvolatile Memory Applications. Ieee Electr Device L. 2010;31:1017-9.

[88] Hopcroft M, Kramer T, Kim G, Takashima K, Higo Y, Moore D, et al. Micromechanical testing of SU-8 cantilevers. Fatigue Fract Eng M. 2005;28:735-42.

[89] Park J-H, An J-H, Kim Y-J, Lee H-J, Roh HY, Kim S-H. Reliability Assessment of MEMS Structure of Su-8 Thin Film. 2007 First International Conference on Integration and Commercialization of Micro and Nanosystems: American Society of Mechanical Engineers; 2007. p. 495-500.

[90] Park SB, Chung SW, Makhar S, Ackler H, Lin PY. Structural reliability of Su-8 material for MEMS application. Electronic and Photonic Packaging, Integration and Packaging of MICRO/NANO/Electronic Systems. 2005:251-8.

[91] Tvedt LGW, Nguyen DS, Halvorsen E. Nonlinear Behavior of an Electrostatic Energy Harvester Under Wide- and Narrowband Excitation. J Microelectromech S. 2010;19:305-16.

[92] Senturia SD. Microsystem Design: Springer; 2000.

[93] Zhang WH, Baskaran R, Tumer KL. Effect of cubic nonlinearity on auto-parametrically amplified resonant MEMS mass sensor. Sensor Actuat a-Phys. 2002;102:139-50.

[94] Hajati A, Kim S. Wide-bandwidth MEMS-scale piezoelectric energy harvester. PowerMEMS'09. 2009.

[95] Hajati A, Kim SG. Rectifier-less piezoelectric micro power generator - art. no. 69281T. Active and Passive Smart Structures and Integrated Systems 2008. 2008;6928:T9281-T.

[96] Dai XH, Miao XD, Sui LH, Zhou HL, Zhao XL, Ding GF. Tuning of nonlinear vibration via topology variation and its application in energy harvesting. Appl Phys Lett. 2012;100.

[97] Hajati A. Ultra wide-bandwidth micro energy harvester [PhD Dissertation]. Massachusetts Institute of Technology: Massachusetts Institute of Technology.; 2011.

[98] Thomson W. Theory of Vibration with Applications: Taylor & Francis; 1996.

[99] Nayfeh AH, Mook DT. Nonlinear Oscillations: Wiley; 2008.

[100] Cammarano A, Neild SA, Burrow SG, Inman DJ. The bandwidth of optimized nonlinear vibration-based energy harvesters. Smart Materials and Structures. 2014;23.

[101] Lorenz H, Despont M, Fahrni N, LaBianca N, Renaud P, Vettiger P. SU-8: a low-cost negative resist for MEMS. J Micromech Microeng. 1997;7:121-4.

[102] Al-Halhouji AT, Kampen I, Krah T, Buettgenbach S. Nanoindentation testing of SU-8 photoresist mechanical properties. Microelectron Eng. 2008;85:942-4.

[103] Kamper KP, Dopper J, Ehrfeld W, Oberbeck S. A self-filling low-cost membrane micropump. Micro Electro Mechanical Systems - Ieee Eleventh Annual International Workshop Proceedings. 1998:432-7.

[104] Chang MMW, Deng MTM, Gwo JTJ, Mai JD, Hsu E. Polymer-based capacitive micromachined ultrasonic transducers (CMUT) for micro surgical Imaging applications. 2006 1st IEEE International Conference on Nano/Micro Engineered and Molecular Systems, Vols 1-3. 2006:61-5.

[105] Royer M, Holmen J, Wurm M, Aadland O, Glenn M. ZnO on Si integrated acoustic sensor. Sensors and Actuators. 1983;4:357-62.

[106] Kim E, Kim J, Muller R. Improved IC-compatible piezoelectric microphone and CMOS process. Solid-State Sensors and Actuators, 1991 Digest of Technical Papers, TRANSDUCERS'91, 1991 International Conference on: IEEE; 1991. p. 270-3.

[107] Horowitz S, Nishida T, Cattafesta L, Sheplak M. Development of a micromachined piezoelectric microphone for aeroacoustics applications. The Journal of the Acoustical Society of America. 2007;122:3428-36.

[108] Williams MD, Griffin BA, Reagan TN, Underbrink JR, Sheplak M. An AlN MEMS piezoelectric microphone for aeroacoustic applications. Microelectromechanical Systems, Journal of. 2012;21:270-83.

[109] Griffin BA, Williams MD, Coffman CS, Sheplak M. Aluminum Nitride Ultrasonic Air-Coupled Actuator. J Microelectromech S. 2011;20:476-86.

[110] Papila M, Sheplak M, Cattafesta LN. Optimization of clamped circular piezoelectric composite actuators. Sensor Actuat a-Phys. 2008;147:310-23.

[111] Shinoda S, Tai T, Itoh H, Sugou T, Ichioka H, Kimura S, et al. Lead Zirconate Titanate Acoustic Energy Harvester Proposed for Microelectromechanical System/IC Integrated Systems. Jpn J Appl Phys. 2010;49.

[112] Horowitz SB, Sheplak M, Cattafesta LN, Nishida T. A MEMS acoustic energy harvester. J Micromech Microeng. 2006;16:S174-S81.

[113] Yang AC, Li P, Wen YM, Lu CJ, Peng X, Zhang JT, et al. Enhanced Acoustic Energy Harvesting Using Coupled Resonance Structure of Sonic Crystal and Helmholtz Resonator. Appl Phys Express. 2013;6.

[114] Iizumi S, Kimura S, Tomioka S, Tsujimoto K, Uchida Y, Tomii K, et al. Lead Zirconate Titanate Acoustic Energy Harvesters Utilizing Different Polarizations on Diaphragm. Procedia Engineer. 2011;25.

[115] Bu G, Ciplys D, Shur M, Schowalter LJ, Schujman S, Gaska R. Surface acoustic wave velocity in single-crystal AlN substrates. Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on. 2006;53:251-4.

[116] Assouar MB, Elmazria O, Le Brizoual L, Alnot P. Reactive DC magnetron sputtering of aluminum nitride films for surface acoustic wave devices. Diam Relat Mater. 2002;11:413-7.

[117] Lee HC, Lee JY, Ahn HJ. Effect of the Substrate Bias Voltage on the Crystallographic Orientation of Reactively Sputtered Aln Thin-Films. Thin Solid Films. 1994;251:136-40.

[118] Khanna A, Bhat DG. Effects of deposition parameters on the structure of AlN coatings grown by reactive magnetron sputtering. J Vac Sci Technol A. 2007;25:557-65.

[119] Duquenne C, Tessier PY, Besland MP, Angleraud B, Jouan PY, Aubry R, et al. Impact of magnetron configuration on plasma and film properties of sputtered aluminum nitride thin films. J Appl Phys. 2008;104.

[120] Okano H, Takahashi Y, Tanaka T, Shibata K, Nakano S. Preparation of C-Axis Oriented Aln Thin-Films by Low-Temperature Reactive Sputtering. Jpn J Appl Phys 1. 1992;31:3446-51.

[121] Xu XH, Wu HS, Zhang CJ, Jin ZH. Morphological properties of AIN piezoelectric thin films deposited by DC reactive magnetron sputtering. Thin Solid Films. 2001;388:62-7.

[122] Kar JP, Bose G, Tuli S. Influence of nitrogen concentration on grain growth, structural and electrical properties of sputtered aluminum nitride films. Scripta Mater. 2006;54:1755-9.

[123] Cheng H, Sun Y, Hing P. The influence of deposition conditions on structure and morphology of aluminum nitride films deposited by radio frequency reactive sputtering. Thin Solid Films. 2003;434:112-20.

[124] Aspar B, Rodriguezclemente R, Figueras A, Armas B, Combescure C. Influence of the Experimental Conditions on the Morphology of Cvd A1n Films. J Cryst Growth. 1993;129:56-66.

[125] Miyauchi M, Ishikawa Y, Shibata N. Growth of Aluminum Nitride Films on Silicon by Electron-Cyclotron-Resonance-Assisted Molecular-Beam Epitaxy. Jpn J Appl Phys 2. 1992;31:L1714-L7.

[126] Vispute RD, Wu H, Narayan J. High-Quality Epitaxial Aluminum Nitride Layers on Sapphire by Pulsed-Laser Deposition. Appl Phys Lett. 1995;67:1549-51.

[127] Cleland AN, Pophristic M, Ferguson I. Single-crystal aluminum nitride nanomechanical resonators. Appl Phys Lett. 2001;79:2070-2.

[128] Khan FA, Zhou L, Kumar V, Adesida I, Okojie R. High rate etching of AlN using BCl3/Cl-2/Ar inductively coupled plasma. Mat Sci Eng B-Solid. 2002;95:51-4.

[129] Zhuang D, Edgar JH. Wet etching of GaN, AIN, and SiC: a review. Mat Sci Eng R. 2005;48:1-46.

[130] Piazza G, Stephanou PJ, Pisano AP. Piezoelectric aluminum nitride vibrating contour-mode MEMS resonators. J Microelectromech S. 2006;15:1406-18.

[131] Mileham JR, Pearton SJ, Abernathy CR, Mackenzie JD, Shul RJ, Kilcoyne SP. Wet Chemical Etching of Aln. Appl Phys Lett. 1995;67:1119-21.

[132] Chen D, Xu D, Wang JJ, Zhang YF. Investigation of chemical etching of AlN film with different textures by x-ray photoelectron spectroscopy. J Phys D Appl Phys. 2008;41.

[133] Ganesh VP, Lee C. Overview and emerging challenges in mechanical dicing of silicon wafers. El Packag Tech Conf. 2006:15-21.

[134] Awatani Y, Matsumoto Y, Kato K. Damage free dicing method for MEMS devices. Optical MEMs, 2002 Conference Digest 2002 IEEE/LEOS International Conference on2002. p. 137-8.

[135] Hoheisel D, Cvetkovic S, Kurniawan W, Obermeier E, Gatzen HH. System Integration Challenges for a Slider With an Integrated Microactuator. Ieee T Magn. 2010;46:2163-6.

[136] Landesberger C, Klink G, Schwinn G, Aschenbrenner R. New dicing and thinning concept improves mechanical reliability of ultra thin silicon. International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, Proceedings. 2001:92-7.

[137] Agarwal A, Mohanraj S, Premachandran CS, Singh J. Process technique for singulating fragile devices. Proceedings of the 7th Electronics Packaging Technology Conference, Vols 1 and 2. 2005:716-9.

[138] Enikov ET, Nelson BJ. Three-dimensional microfabrication for a multi-degree-of-freedom capacitive force sensor using fibre-chip coupling. J Micromech Microeng. 2000;10:492-7.

[139] Gradin H, Braun S, Stemme G, van der Wijngaart W. Localized removal of the Au-Si eutectic bonding layer for the selective release of microstructures. J Micromech Microeng. 2009;19.

[140] Tseng S, Xiao F, Juang Y, Chiu C, Cheng M. Solutions for dicing released CMOS-MEMS multi-project wafer. Proc Design, Test, Integration and Packaging (DTIP) of MEMS/MOEMS Conf(Montreux, Switzerland, 12–14 May)2004. p. 55-9.

[141] Cooke M. Scribe and dice. III-Vs Review. 2006;19:20-4.

[142] Misra A, Fininie I. On the scribing and subsequent fracturing of silicon semiconductor wafers. Journal of Materials Science. 1979;14:2567-74.

[143] Oliver AD, Wallner TA, Tandon R, Nieman K, Bergstrom PL. Diamond scribing and breaking of silicon for MEMS die separation. J Micromech Microeng. 2008;18.

[144] Ogorodnikov AI, Ogorodnikova OM, Tikhonov IN. Simulation of defect zones in scribed silicon wafers. Iop Conf Ser-Mat Sci. 2010;15.

[145] Sokmen U, Stranz A, Fundling S, Wehmann HH, Bandalo V, Bora A, et al. Capabilities of ICP-RIE cryogenic dry etching of silicon: review of exemplary microstructures. J Micromech Microeng. 2009;19.

[146] Sari I, Zeimpekis I, Kraft M. A Full Wafer Dicing Free Dry Release Process for MEMS Devices. Procedia Engineer. 2010;5:850-3.

[147] Porter DA, Berfield TA. Die separation and rupture strength for deep reactive ion etched silicon wafers. J Micromech Microeng. 2013;23.

[148] Pau S, Taylor JA, Pai CS. Nonorthogonal wafer dicing for waveguide, microelectromechanical systems, and nanotechnology applications. J Vac Sci Technol B. 2004;22:L15-L6.

[149] Qu HW, Xie HK. Process development for CMOS-MEMS sensors with robust electrically isolated bulk silicon microstructures. J Microelectromech S. 2007;16:1152-61.

[150] Cvetkovic S, Saalfeld H, Gatzen H. Dicing process for the device separation of a slider with an integrated microactuator (SLIM). Proceedings of ASPE 23rd annual meeting and 12th ICPE2008. p. 380-3.

[151] Overstolz T, Clerc PA, Noell W, Zickar M, de Rooij NF. A clean wafer-scale chip-release process without dicing based on vapor phase etching. Mems 2004: 17th Ieee International Conference on Micro Electro Mechanical Systems, Technical Digest. 2004:717-20.

[152] Sari I, Zeimpekis L, Kraft M. A dicing free SOI process for MEMS devices. Microelectron Eng. 2012;95:121-9.

[153] Heriban D, Agnus J, Petrini V, Gauthier M. A mechanical de-tethering technique for silicon MEMS etched with a DRIE process. J Micromech Microeng. 2009;19.

[154] Rezaei M, Lueke J, Sameoto D, Raboud D, Moussa W. A New Approach to Cleave MEMS Devices from Silicon Substrates. Journal of Mechanics Engineering and Automation. 2013;3:731 - 8

[155] Yeom J, Wu Y, Shannon MA. Critical aspect ratio dependence in deep reactive ion etching of silicon. Boston Transducers'03: Digest of Technical Papers, Vols 1 and 2. 2003:1631-4.

[156] Gilleo K. MEMS/MOEM Packaging : Concepts, Designs, Materials and Processes: Concepts, Designs, Materials, and Processes: McGraw-Hill Professional Publishing; 2005.

[157] John H. Lau CL, C. S. Premachandran, Yu Aibin. Bio-MEMS Packaging: McGraw-Hill Professional, 2010; 2010.

[158] Wong CP, Moon KS, Li Y. Nano-Bio- Electronic, Photonic and MEMS Packaging: Springer; 2009.

[159] Tekin T. Review of Packaging of Optoelectronic, Photonic, and MEMS Components. Ieee J Sel Top Quant. 2011;17:704-19.

[160] Lucyszyn S. Review of radio frequency microelectromechanical systems technology. Iee P-Sci Meas Tech. 2004;151:93-103.

[161] Shoji S, Kikuchi H, Torigoe H. Low-temperature anodic bonding using lithium aluminosilicate-beta-quartz glass ceramic. Sensor Actuat a-Phys. 1998;64:95-100.

[162] Maluf N, Williams K. Introduction to Microelectromechanical Systems Engineering: Artech House; 2004.

[163] Ramesham R, Ghaffarian R. Challenges in interconnection and packaging of microelectromechanical systems (MEMS). P Electr C. 2000:666-75.

[164] Morrissey A, Kelly G, Alderman J. Selection of materials for reduced stress packaging of a microsystem. Sensor Actuat a-Phys. 1999;74:178-81.

[165] Butler JT, Bright VM, Comtois JH. Multichip module packaging of microelectromechanical systems. Sensor Actuat a-Phys. 1998;70:15-22.

[166] Bustillo J, Fedder G, Nguyen CC, Howe R. Process technology for the modular integration of CMOS and polysilicon microstructures. Microsystem Technologies. 1994;1:30-41.

[167] Tilmans HAC, De Raedt W, Beyne E. MEMS for wireless communications: 'from RF-MEMS components to RF-MEMS-SiP'. J Micromech Microeng. 2003;13:S139-S63.

[168] Viswanadham P. Essentials of Electronic Packaging: A Multidisciplinary Approach: American Society of Mechanical Engineers; 2011.

[169] Hsu TR. Mems Packaging: Institution of Engineering and Technology; 2004.

[170] Wang PH, Tanaka K, Sugiyama S, Dai XH, Zhao XL, Liu JQ. A micro electromagnetic low level vibration energy harvester based on MEMS technology. Microsyst Technol. 2009;15:941-51.

[171] Miao P, Mitcheson PD, Holmes AS, Yeatman EM, Green TC, Stark BH. Mems inertial power generators for biomedical applications. Microsyst Technol. 2006;12:1079-83.

[172] Aktakka EE, Peterson RL, Najafi K. A Self-Supplied Inertial Piezoelectric Energy Harvester with Power-Management IC. In: IEEE, editor. 2011 IEEE International Solid-State Circuits Conference. Beijing, China2011. p. 120-1.

[173] Khalyfa A, Vogt S, Weisser J, Grimm G, Rechtenbach A, Meyer W, et al. Development of a new calcium phosphate powder-binder system for the 3D printing of patient specific implants. J Mater Sci-Mater M. 2007;18:909-16.

[174] Warnke PH, Seitz H, Warnke F, Becker ST, Sivananthan S, Sherry E, et al. Ceramic scaffolds produced by computer-assisted 3D printing and sintering: characterization and biocompatibility investigations. J Biomed Mater Res B. 2010;93B:212-7.

[175] Peltola SM, Melchels FPW, Grijpma DW, Kellomaki M. A review of rapid prototyping techniques for tissue engineering purposes. Ann Med. 2008;40:268-80.

[176] Seitz H, Rieder W, Irsen S, Leukers B, Tille C. Three-dimensional printing of porous ceramic scaffolds for bone tissue engineering. J Biomed Mater Res B. 2005;74B:782-8.

[177] Pfister A, Landers R, Laib A, Hubner U, Schmelzeisen R, Mulhaupt R. Biofunctional rapid prototyping for tissue-engineering applications: 3D bioplotting versus 3D printing. J Polym Sci Pol Chem. 2004;42:624-38.

[178] Blackwell GR. The Electronic Packaging Handbook: Taylor & Francis; 1999.

[179] Cao YH, Ning WG, Luo L. Wafer-Level Package With Simultaneous TSV Connection and Cavity Hermetic Sealing by Solder Bonding for MEMS Device. Ieee T Electron Pack. 2009;32:125-32.

[180] Dixit P, Salonen J, Pohjonen H, Monnoyer P. The application of dry photoresists in fabricating cost-effective tapered through-silicon vias and redistribution lines in a single step. J Micromech Microeng. 2011;21.

[181] Jackson N, Muthuswamy J. Flexible Chip-Scale Package and Interconnect for Implantable MEMS Movable Microelectrodes for the Brain. J Microelectromech S. 2009;18:396-404.

[182] Joung YH, Allen MG. A micromachined chip-to-board interconnect system using electroplating bonding technology. Ieee T Adv Packaging. 2008;31:357-66.

[183] Jozwiak J, Southwick RG, Johnson VN, Knowlton WB, Moll AJ. Integrating through-wafer interconnects with active devices and circuits. Ieee T Adv Packaging. 2008;31:4-13.

[184] Tian J, Sosin S, Lannacci J, Gaddi R, Bartek M. RF-MEMS wafer-level packaging using through-wafer interconnect. Sensor Actuat a-Phys. 2008;142:442-51.

[185] Ji F, Leppadvuori E, Luusua I, Hentfinen K, Eranen S, Hietanen H, et al. Fabrication of silicon based through-wafer interconnects for advanced chip scale packaging. Sensor Actuat a-Phys. 2008;142:405-12.

[186] Chow EM, Chandrasekaran V, Partridge A, Nishida T, Sheplak M, Quate CF, et al. Process compatible polysilicon-based electrical through-wafer interconnects in silicon substrates. J Microelectromech S. 2002;11:631-40.

[187] Ham YH, Kim DP, Park KS, Jeong YS, Yun HJ, Baek KH, et al. Dual etch processes of via and metal paste filling for through silicon via process. Thin Solid Films. 2011;519:6727-31.

[188] Lee SWR, Hon R, Zhang SXD, Wong CK. 3D stacked flip chip packaging with through silicon vias and copper plating or conductive adhesive filling. Elec Comp C. 2005:795-801.

[189] Kikuchi H, Yamada Y, Ali AM, Liang J, Fukushima T, Tanaka T, et al. Tungsten through-silicon via technology for three-dimensional LSIs. Jpn J Appl Phys. 2008;47:2801-6.

[190] Fischer AC, Grange M, Roxhed N, Weerasekera R, Pamunuwa D, Stemme G, et al. Wire-bonded through-silicon vias with low capacitive substrate coupling. J Micromech Microeng. 2011;21.

[191] Yang B, Lee C, Kotlanka RK, Xie J, Lim SP. A MEMS rotary comb mechanism for harvesting the kinetic energy of planar vibrations. J Micromech Microeng. 2010;20.

[192] Elfrink R, Renaud M, Kamel TM, de Nooijer C, Jambunathan M, Goedbloed M, et al. Vacuum-packaged piezoelectric vibration energy harvesters: damping contributions and autonomy for a wireless sensor system. J Micromech Microeng. 2010;20.

[193] Williams CB, Shearwood C, Harradine MA, Mellor PH, Birch TS, Yates RB. Development of an electromagnetic micro-generator. Circuits, Devices and Systems, IEE Proceedings -. 2001;148:337-42.

[194] Lee C, Lima YM, Yang B, Kotlanka RK, Heng CH, He JH, et al. Theoretical comparison of the energy harvesting capability among various electrostatic mechanisms from structure aspect. Sensor Actuat a-Phys. 2009;156:208-16.

[195] Gooch R, Schimert T. Low-Cost Wafer-Level Vacuum Packaging for MEMS. MRS Bulletin. 2003;28:55-9.

[196] Topalli ES, Topalli K, Alper SE, Serin T, Akin T. Pirani Vacuum Gauges Using Silicon-on-Glass and Dissolved-Wafer Processes for the Characterization of MEMS Vacuum Packaging. Ieee Sens J. 2009;9:263-70.

[197] Chae J, Giachino JM, Najafi K. Fabrication and characterization of a wafer-level MEMS vacuum package with vertical feedthroughs. J Microelectromech S. 2008;17:193-200.

[198] Sparks DR, Massoud-Ansari S, Najafi N. Chip-level vacuum packaging of micromachines using NanoGetters. Ieee T Adv Packaging. 2003;26:277-82.

[199] Cheng YT, Hsu WT, Najafi K, Nguyen CTC, Lin LW. Vacuum packaging technology using localized aluminum/silicon-to-glass bonding. J Microelectromech S. 2002;11:556-65.

[200] Lee B, Seok S, Chun K. A study on wafer level vacuum packaging for MEMS devices. J Micromech Microeng. 2003;13:663-9.

[201] Welch WC, Najafi K. Gold-indium transient liquid phase (TLP) wafer bonding for MEMS vacuum packaging. Mems 2008: 21st Ieee International Conference on Micro Electro Mechanical Systems, Technical Digest. 2008:806-9.

[202] Rao SS. Mechanical Vibrations Addison-Wesley Publishing Company; 1984.

[203] Trolier-McKinstry S, Muralt P. Thin film piezoelectrics for MEMS. J Electroceram. 2004;12:7-17.

[204] Kim SB, Park H, Kim SH, Wikle HC, Park JH, Kim DJ. Comparison of MEMS PZT Cantilevers Based on d(31) and d(33) Modes for Vibration Energy Harvesting. J Microelectromech S. 2013;22:26-33.

[205] Ramadass YK, Chandrakasan AP. An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor. Ieee J Solid-St Circ. 2010;45:189-204.

[206] Lefeuvre E, Badel A, Richard C, Petit L, Guyomar D. A comparison between several vibration-powered piezoelectric generators for standalone systems. Sensor Actuat a-Phys. 2006;126:405-16.

[207] Guyomar D, Badel A, Lefeuvre E, Richard C. Toward energy harvesting using active materials and conversion improvement by nonlinear processing. Ieee T Ultrason Ferr. 2005;52:584-95.

[208] Shu YC, Lien IC, Wu WJ. An improved analysis of the SSHI interface in piezoelectric energy harvesting. Smart Materials & Structures. 2007;16:2253-64.

[209] Vasic D, Chen YY, Costa F. Design of self-powering part of SSHI interface for piezoelectric energy harvesting. Electron Lett. 2013;49:288-90.

[210] Prak A, Blom FR, Elwenspoek M, Lammerink TSJ. Q-Factor and Frequency-Shift of Resonating Silicon Diaphragms in Air. Sensor Actuat a-Phys. 1991;27:691-8.

[211] Weigert S, Dreier M, Hegner M. Frequency shifts of cantilevers vibrating in various media. Appl Phys Lett. 1996;69:2834-6.

[212] Horowitz SB. Development of a MEMS-based Acoustic Energy Harvester [PhD Dissertation]. University of Florida University of Florida 2005.

[213] Ong RJ, Payne DA, Sottos NR. Processing effects for integrated PZT: Residual stress, thickness, and dielectric properties. J Am Ceram Soc. 2005;88:2839-47.

[214] Al-Homoudi IA, Zhang LF, Georgiev DG, Naik R, Naik VM, Rimai L, et al. Residual stresses in TiO2 anatase thin films deposited on glass, sapphire and Si substrates. Mater Res Soc Symp P. 2005;875:363-8.

[215] Inoue N, Nakura T, Hayashi Y. Low thermal-budget process of sputtered-PZT capacitor over multilevel metallization. Ieee T Electron Dev. 2003;50:2081-7.

[216] Takita R, Tsuchiya K, Uetsuji Y. Research on the Surface in Au-Pt Buffer Layer for the High Piezoelectric PZT. 2012 International Symposium on Micro-Nanomechatronics and Human Science (Mhs). 2012:201-6.

[217] Funakubo H, Nagai A, Minamidate J, Koo JM, Kim SP, Park Y. Trial for making three dimensional PZT capacitor for high density ferroelectric random access memory. Integr Ferroelectr. 2006;81:219-26.

[218] Li TK, Zawadzki P, Stall RA. Microstructure and properties of PbZr1-xTixO3 thin films made by one and two step metalorganic chemical vapor deposition. Integr Ferroelectr. 1997;18:155-69.

[219] Uchida T, Kikuchi T, Murakami T, Kawashima N, Takeuchi S. Effect of Surface Modification of Titanium Substrate by Anodic Oxidation on Hydrothermally Synthesized PZT Poly-crystalline Film. Ultrason. 2008:2122-5.

[220] Bathurst SP, Kim SG. Designing direct printing process for improved piezoelectric micro-devices. Cirp Ann-Manuf Techn. 2009;58:193-6.

[221] Wang D, Edirisinghe MJ, Dorey RA. Formation of PZT crack-free thick films by electrohydrodynamic atomization deposition. J Eur Ceram Soc. 2008;28:2739-45.

[222] Dauchy F, Dorey RA. Patterned crack-free PZT thick films for micro-electromechanical system applications. Int J Adv Manuf Tech. 2007;33:86-94.

[223] Kanda K, Kanno I, Kotera H, Wasa K. Simple Fabrication of Metal-Based Piezoelectric MEMS by Direct Deposition of Pb(Zr, Ti)O-3 Thin Films on Titanium Substrates. J Microelectromech S. 2009;18:610-5.

[224] Okamura S, Shiosaki T. Properties of micropatterned ferroelectric thin films fabricated by electron beam exposed chemical solution deposition process. Ferroelectrics. 1999;232:895-904.

[225] Tang TA, Chen Z, Li N, Zou SX. Reactive ion etching of sol-gel derived PZT thin film and Pt/Ti bottom electrode for FRAM. Ferroelectrics. 1999;232:927-32.

[226] Wang SA, Li XH, Wakabayashi K, Esashi M. Deep reactive ion etching of lead zirconate titanate using sulfur hexafluoride gas. J Am Ceram Soc. 1999;82:1339-41.

[227] Zheng K, Lu J, Chu J. A novel wet etching process of Pb(Zr,Ti)O-3 thin films for applications in microelectromechanical system. Jpn J Appl Phys 1. 2004;43:3934-7.

[228] Miller RA, Bernstein JJ. A novel wet etch for patterning lead zirconate-titanate (PZT) thin-films. Integr Ferroelectr. 2000;29:225-31.

[229] Ezhilvalavan S, Zhang ZL, Loh J, Ying JY. Microfabrication of PZT force sensors for minimally invasive surgical tools. J Phys Conf Ser. 2006;34:979-84.

[230] Mancha S. Chemical Etching of Thin-Film Plzt. Ferroelectrics. 1992;135:131-7.

[231] Yeh TH, Suresh MB, Shen JN, Yu JC, Chou CC. Chemical Reactions During Wet-Etching Process of LSMO/PZT/LSMO-Structured Device Fabrication. Ferroelectrics. 2009;380:97-101.

[232] Kokaze Y, Kimura I, Endo M, Ueda M, Kikuchi S, Nishioka Y, et al. Dry etching process for Pb(Zr,Ti)O-3 thin-film actuators. Japanese Journal of Applied Physics. 2007;46:280-2.