Behavioral Device-Level Modeling of Modular Multilevel Converters in Real Time for Variable-Speed Drive Applications

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***Abstract*— This paper presents the real-time hardware-in-the-loop (HIL) emulation of an induction machine (IM) driven by a modular multilevel converter (MMC) on the field-programmable gate array (FPGA). The insulated gate bipolar transistors and antiparallel diodes of the MMC are modeled with nonlinear static and dynamic characteristics to provide not only accurate system-level performance of the converter but also insight into the power losses under different operation conditions. Due to the large network size of the MMC, its solution in conjunction with the IM fifth-order model proved to be a significant computational challenge. Therefore, circuit partitioning based on the transmission line modeling is proposed, which introduced an interface to the electrical network for the IM as well as split the multiloop MMC into several smaller subcircuits in terms of matrix size, and consequently enabled a fully parallel implementation on the FPGA. Control strategies for the MMC and IM are also emulated in hardware, and due to the large latency difference between subcircuits and controllers, the overall system hardware design is divided into several layers, each having an independent time step ranging from 500 ns to 4 μs so as to attain the goal of real-time execution. A comparison of transient and steady-state results from the HIL emulation and offline simulation tools shows high accuracy of the modeling approach as well as the efficacy of proposed multiple time steps in achieving real time.**

***Index Terms*— Field-programmable gate array (FPGA), induction machine (IM), modular multilevel converter (MMC), parallel processing, partitioning algorithms, real-time systems.**

NOMENCLATURE

R_{ON}, R_{OFF}	ON- and OFF-state resistances of a two-state switch.
$V_{g1,2}$	Gate voltages of two insulated gate bipolar transistors (IGBTs) in a submodule.
$i_{u,d}$	MMC upper or lower arm current.
n	Subscript for time step index.
$Z_{Lu,d}$	Arm inductor characteristic impedance.
v^i_{Lu}, v^i_{Ld}	Arm inductor incident pulses.
v_s, i_s	Single-phase stator voltage and current.
v^i_{mj}, v^i_{kj}	Incident pulses of jth transmission line modeling (TLM) link.
abc	Three-phase indexes.
r_1, r_2	Resistances of two IGBTs in a submodule.
v_{Cj}, v^i_{Cj}	jth submodule capacitor voltage and incident pulse.
$i_{C1,2}$	IGBT/diode current in a submodule.

I. INTRODUCTION

The modular multilevel converter (MMC) has received tremendous attention in recent years with wide industrial applications in medium- and high-power occasions, such as static synchronous compensator [1]–[3], renewable energy grid connection [4]–[6], medium-power drives [7], [8], and high-voltage direct current (HVdc) transmission projects [9], [10], where this voltage source converter (VSC) has been gaining momentum and is expected to overtake traditional thyristor-based line-commutated converters as the main vehicle for electrical energy conversion due to its advantages such as resilience to commutation failure and capacity of regulating reactive power. Meanwhile, it also has merits over traditional two-level or other multilevel converters such as high-power quality quasi-sinusoidal output waveforms, obviating the need for bulky filtering equipment and scalability, which allows the number of submodules to be flexibly changed to adjust to different voltage stresses or to produce the demanded voltage levels.

The simulation of MMC by electromagnetic transient (EMT) programs is significant in terms of providing a platform for testing and validating control and protection strategies as well as giving specific information about the power system's performance when a certain fault occurs and is detected. However, unlike other VSCs where the number of switches is limited, modularity of the MMC indicates that there could be dozens or even hundreds of nonlinear switches. From a circuit solution point of view, the nodes or meshes in the MMC outnumber those of other converter topologies, which means it takes a longer execution time for a CPU to calculate the results when the output voltage level rises [11]–[16]. This negative impact can be remarkably minimized using field-programmable gate arrays (FPGAs), which are excellent in hardwired parallelism and by conducting several calculations simultaneously. The computational time for MMC models is greatly shortened and it is possible for hardware-in-the-loop (HIL) emulation to achieve real-time execution, which made it attractive alternative. Therefore, FPGAs have successfully been utilized

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for accurate real-time modeling of various power systems and power electronic equipment components in both industrial applications and academic study [17]–[22] by significantly increasing the modeling complexity and reducing latencies for HIL applications.

Nevertheless, the large quantity of switches still poses a challenge to attaining real time for HIL emulation or fast simulation for other EMT simulation tools by forcing the adoption of simpler modeling strategies for the MMC switches or arms. Finding an appropriate model for the MMC that can provide switch-level details while being computationally efficient is crucial. A variety of models have so far been proposed for MMC modeling, which largely fall into the following categories: device-level model, detailed equivalent model (DEM), and average value model (AVM). The switches in device-level model can either be detailed physics-based models of IGBT and diode, which are accurate but rather complicated, or equivalent models that combines an ideal switch with classical nonlinear diodes, enabling engineers to estimate conduction loss [23]. While such detailed models are useful and actually needed for being able to offer greater accuracy [24], new MMC model construction as well as validation [25], and converter design to achieve higher efficiency [26], [27], they are computationally burdensome and may not be suitable for real-time HIL emulation or system-level simulation. DEM ignores specific features of the IGBT/diode pair, which is replaced by a bidirectional two-state switch with R_{ON} and R_{OFF} commanded by the driving pulses, allowing the submodule to be represented by its Thévénin equivalent circuit and the subsequent merging of all submodules in the same arm [11], [12], [28], [29]. In this way, the node number is significantly reduced and the computational speed is fast. AVM is carried out under the assumption that all internal variables, including dc capacitor voltages of submodules, are well controlled and balanced. Switching effects are not explicitly shown and submodules are modeled as equivalent voltage and current sources, which are also merged to replace all submodules [30]–[32]. For DEM and AVM, which are currently the predominant models for MMC, the accuracy is sufficient for system-level power system studies; however, both models lose some specificities, for example, the possibilities of observing switching transients and assessing converter power losses are excluded, and even the capacitor charging process is not observable for the latter. Although AVM variants are proposed to show the dc capacitor voltage ripples [33] or to enable converter power loss calculation [34], the focus is still on system-level performance and the individuality of the switches cannot be shown; meanwhile, the power loss based on the DEM is merely a rough estimation as it is carried out under the assumption that the IGBT and diode have equal ON-state resistance and are set constant.

In this paper, a new device-level behavioral MMC model suitable for real-time HIL emulation is proposed in the context of a variable-speed induction machine (IM) drive application. The main features of the IGBT/diode pair, such as the static nonlinear V–I characteristics, turn-ON/OFF, and reverse recovery process, are preserved in order to provide more accurate details of the converter within the capability of the real-time system for evaluation of an MMC design or a new type of model. Apart from previous works where the simulation time steps were generally in the range of tens of microseconds to enable real-time execution while omitting nanosecond-scale phenomena, the time step should be much smaller for the IGBT/diode pair so as to capture the switching transients. Meanwhile, calculation of the MMC and the IM controllers requires a much larger time step, and therefore, high parallelism between MMC parts and a multiple time step algorithm are essential. In contrast with DEM and AVM that merge all submodules in an arm to eliminate nodes, we propose a TLM [35]–[37] based link model that enables effective partitioning of the submodules from the arm and decomposes the large matrix for the overall circuit into corresponding submatrices with smaller sizes, which are then calculated in parallel to improve computational efficiency. Furthermore, strategies for MMC inner and IM outer control are implemented and based on the latencies of various parts of the MMC–IM system, and multiple time steps are applied to ensure the calculation of each part to achieve real-time execution.

This paper is organized as follows. Section II presents the modeling details of the IM and the IGBT/diode pair. Section III discusses the TLM-based circuit partitioning method. Details of hardware design of the MMC–IM system are presented in Section IV. Section V shows the results of real-time HIL emulation, and in Section VI, conclusions are drawn.

II. Models for MMC–IM Components

Fig. 1 shows the circuit configuration of an $(N + 1)$-level MMC, where N is the number of submodules in an arm, and each submodule adopts the half-bridge topology with one dc capacitor and two switches, denoted by S_1 in the upper position and S_2 for the lower one. The wires are idealized, and consequently, stray inductance caused by them is not considered in MMC modeling. The behavior of the IGBT/diode pair can be rather complex and simply considering it as a two-state resistor falls short of providing insight such as IGBT turn-ON/OFF and diode reverse recovery; therefore, the behavior of the switches is studied and depending on working state, it is modeled accordingly. As for the IM, the fifth-order model [38] based on stationary reference frame is utilized and the corresponding discrete-time model can be obtained using the trapezoidal rule of integration [39] or Euler's first-order approximation [40] for simulating the performance. Moreover, the machine model can be split from the converter and constitute an independent part when the input voltages are preknown [39]. As our main objective is the device-level modeling of MMC and its real-time emulation, the power loss of the IM is not included in this paper. However, other more complex models, such as the finite-element model or the magnetic equivalent circuit model [41], can also be interfaced with the MMC to provide detailed information of the machine.

A. Induction Machine

The model for the IM is based on a combination of two sets of equations that represent its electrical and mechanical

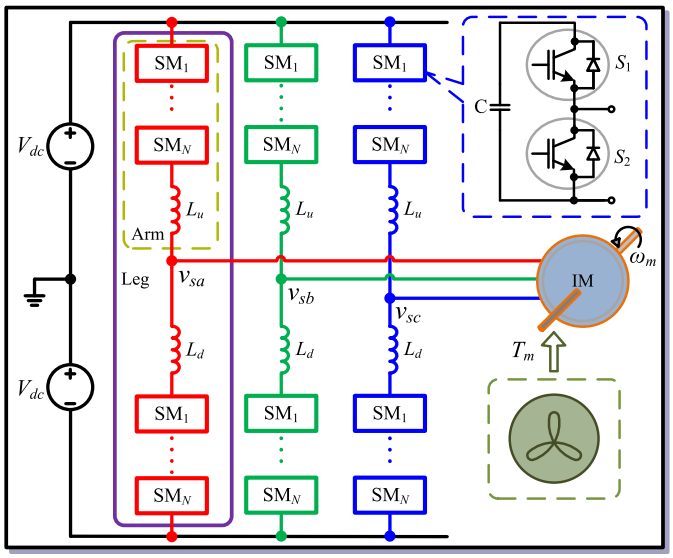


Fig. 1. Configuration of a three-phase $(N+1)$-level MMC driving the IM.

characteristics. The former is described by

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{1}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) \tag{2}$$

where the state, input, and output vectors take the form of

$$\mathbf{x} = [\lambda_{\alpha s}(t) \quad \lambda_{\beta s}(t) \quad \lambda_{\alpha r}(t) \quad \lambda_{\beta r}(t)]^T$$

$$\mathbf{u} = [V_{\alpha s}(t) \quad V_{\beta s}(t)]^T$$

$$\mathbf{y} = \left[i_{\alpha s}(t) \quad i_{\beta s}(t) \quad i_{\alpha r}(t) \quad i_{\beta r}(t)\right]^T$$

in α–β frame and their corresponding matrices are

$$\mathbf{A} = \begin{bmatrix} -c_3 R_s & 0 & c_1 R_s & 0 \\ 0 & -c_3 R_s & 0 & c_1 R_s \\ c_1 R_r & 0 & -c_2 R_r & -\omega_r \\ 0 & c_1 R_r & \omega_r & -c_2 R_r \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}^T$$

$$\mathbf{C} = \begin{bmatrix} c_3 & 0 & -c_1 & 0 \\ 0 & c_3 & 0 & -c_1 \\ -c_1 & 0 & c_2 & 0 \\ 0 & -c_1 & 0 & c_2 \end{bmatrix}$$

where $V_{\alpha s}(t)$ and $V_{\beta s}(t)$ are input voltages and $\lambda_{\alpha s}(t)$, $\lambda_{\beta s}(t)$, $\lambda_{\alpha r}(t)$, and $\lambda_{\beta r}(t)$ represent the fluxes of stator and rotor, whose currents are denoted by $i_{\alpha s}(t)$, $i_{\beta s}(t)$, $i_{\alpha r}(t)$, and $i_{\beta r}(t)$, respectively. R_s and R_r are stator and rotor resistances, and c_1, c_2, and c_3 are obtained by

$$c_1 = \frac{L_m}{L_s L_r - L_m^2}, \quad c_2 = \frac{L_s}{L_s L_r - L_m^2}, \quad c_3 = \frac{L_r}{L_s L_r - L_m^2} \tag{3}$$

where L_m, L_s, and L_r are the magnetizing, stator, and rotor inductances, respectively.

The other equation set describes the mechanical dynamics as

$$\frac{d\omega_r(t)}{dt} = \frac{P}{2J} \cdot (T_e(t) - T_m(t)) \tag{4}$$

which is linked to the electrical domain by

$$T_e(t) = \frac{3}{2}\frac{P}{2} \cdot (i_{\beta s}(t)\lambda_{\alpha s}(t) - i_{\alpha s}(t)\lambda_{\beta s}(t)) \tag{5}$$

where $T_e(t)$ and $T_m(t)$ represent the electromagnetic and load torques, respectively, P denotes the number of poles, J is the combined rotor and load inertia, and ω_r is the electrical angular velocity, whose relation with ω_m, the mechanical angular velocity, is given as $\omega_r = (P/2)\omega_m$.

For digital computation, the above equations are discretized using the trapezoidal rule. Equations (2) and (5) are similar to their time-domain expressions, while for (1) and (4), which contain derivatives, the discretized equations are

$$\mathbf{x}(k) = (\mathbf{I} - \frac{\mathbf{A}\Delta t_1}{2})^{-1} \cdot \left[\left(\mathbf{I} + \frac{\mathbf{A}\Delta t_1}{2}\right)\mathbf{x}(k-1) + \frac{\mathbf{B}\Delta t_1}{2}(\mathbf{u}(k) + \mathbf{u}(k-1))\right] \tag{6}$$

$$\omega_r(k) = \omega_r(k-1) + \frac{P\Delta t_1}{4J} \times (T_e(k) - T_m(k) + T_e(k-1) - T_m(k-1)) \tag{7}$$

where $\mathbf{I}$ is a 4×4 diagonal matrix and Δt_1 denotes time increment and consequently sets as time step for the IM.

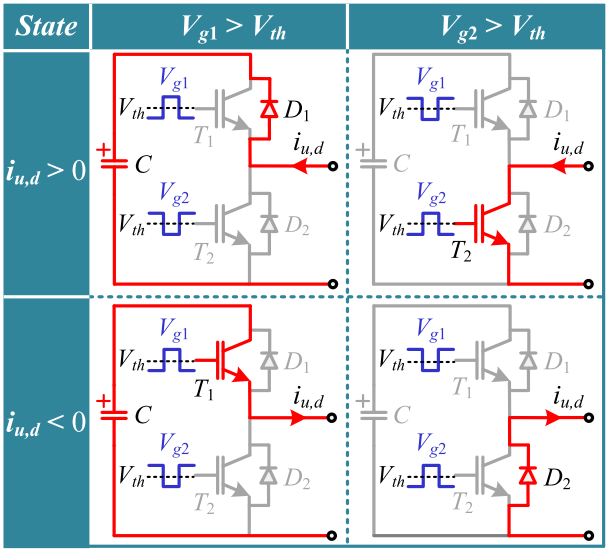
B. IGBT/Diode Pair

IGBT is one of the most popular semiconductor switches in large power applications. It is a fully controllable device with fast response, when the gate voltage V_g exceeds the threshold voltage V_{th}, a current begins to go through from collector to emitter after a short period of turn-ON delay, while if V_g vanishes or goes below zero, the device is forced to turn-OFF. On the other hand, it is a unidirectional device, i.e., the conduction path goes from collector to emitter, and it will not provide a path in reverse direction for current even though the gate driving pulse is high enough. The diode is another fundamental device that is a building block of a power converter, and it is essential in ensuring the normal operation of MMC as a charging path is needed to maintain the dc voltage of each submodule at the desired level.

Table I gives the four states that a normally operated submodule undergoes. It indicates that each IGBT and diode is unique and it is easy to pin down which of them is operating at any given time. For example, positive arm current implies that either the upper diode or lower IGBT is conducting, and combined with the value of V_g, a final judgment can be correctly made. Based on that principle, since a considerable number of modern-day IGBT modules are a combination of both, modeling them as one switch and showing the corresponding features according to gate voltage and arm current direction would reduce the number of meshes in the submodule and consequently shorten the MMC model calculation time.

To establish an accurate model, both the nonlinear static and dynamic characteristics are required and most of the information is readily available in the device datasheet, whose parameters are extracted from the experimental setup, meaning factors such as stray inductance caused by the IGBT are also counted and reflected by the data. The static characteristic of

TABLE I
MMC SUBMODULE OPERATION STATES



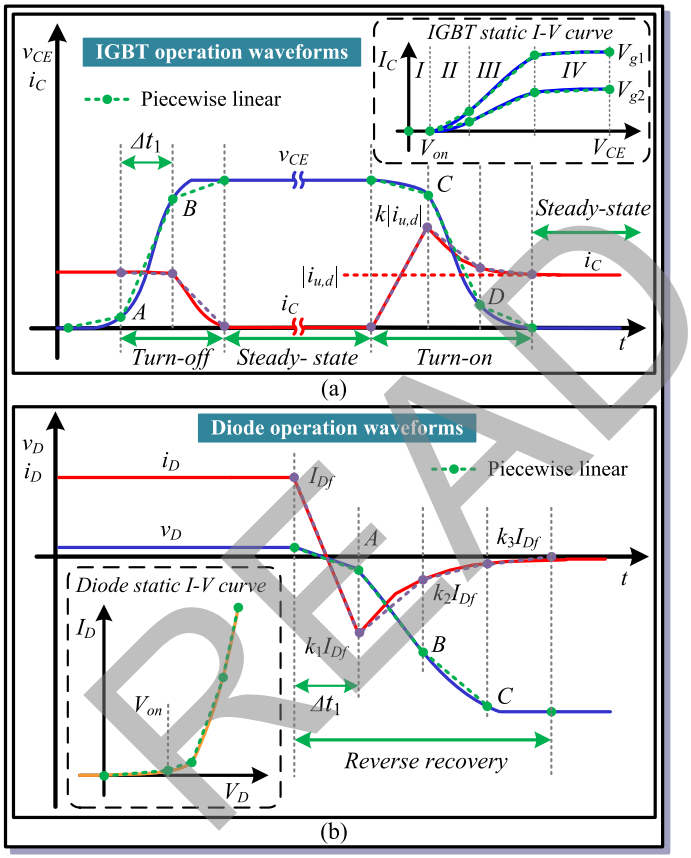


Fig. 2. Behavior of IGBT and diode. (a) IGBT static I–V characteristics and switching transient waveforms. (b) Diode static I–V characteristics and reverse recovery process.

IGBT is shown in Fig. 2(a), from which its voltage drop under steady state can be acquired according to gate voltage and collector current, and therefore, the power consumption can be calculated. However, the $I_C - V_{CE}$ curves are nonlinear and representing them by nonlinear or polynominal functions would lead to a long hardware latency in the FPGA implementation. Considering that it is not necessary to obtain the $I_C - V_{CE}$ values as precisely as they are, the nonlinear curve is divided into several segments and each is treated as a straight line, so that the collector–emitter voltage in a certain segment takes the form of

$$V_{CE} = r_0 \cdot I_C + v_{ceo} \tag{8}$$

where the constants r_0 and v_{ceo} are deduced by linearization and their values at different segments differ from each other. Equation (8) reflects a linear resistance in a segment. Hence, a piecewise linear resistor that consists of all the linear resistances can be used to replace the IGBT. Thus, a general expression for the resistance of any segment can be written as

$$r = \frac{V_{CE}}{I_C} = r_0 + \frac{v_{ceo}}{I_C}. \tag{9}$$

The typical terminal voltage and current waveforms of the IGBT is also shown in Fig. 2(a), which can be obtained from SaberRD simulation of a circuit with a similar topology as that of the MMC submodule. It is proved by SaberRD that the shapes of v_{CE} and i_C are virtually the same in different levels of MMC. Therefore, curve fitting is used and these shapes are applied to IGBTs in the MMC, meaning the proportions of the IGBT terminal voltage and current at turn-OFF and turn-ON stages accounting for the steady-state values are known. The v_{CE} value at OFF-state can be deemed as equal to the submodule capacitor voltage V_C, and therefore, the transient voltage values can be calculated instantly. With regard to the current, the turn-OFF curve can be easily obtained, because its trend is certain, dropping from steady-state current to the final value of zero with a known rate. Nevertheless, the final value of the turn-ON stage is unavailable unless the IGBT enters steady state; therefore, it is difficult to determine the current surge during the turn-ON stage. The MMC arm current provides a solution, noting that its absolute value can be deemed as equal to the IGBT current under steady state. Then the voltage and current during the transient stage take the form of

$$v_{CE}(t + \Delta t_1) = x\% \cdot V_C \tag{10}$$

$$i_C(t + \Delta t_1) = k(t + \Delta t_1) \cdot |i_{u,d}| \tag{11}$$

where Δt_1 is the time step used to mark the transient process and $x\%$ and $k(t + \Delta t_1)$ are coefficients that decided by the shapes of v_{CE} and i_C, respectively. Obviously, the smaller the Δt_1, the more precise the model would be, as the transient stage for the IGBT and diode usually only lasts from several hundred nanoseconds to a few microseconds. It should be pointed out that the gate driver resistance affects the static and dynamic characteristics of the IGBT. However, usually its value is chosen from a small range within which the impact of gate resistance variation is little, and the typical value of 10 Ω is normally chosen since a larger resistor leads to a longer dynamic process.

Fig. 2(b) shows nonlinear static and dynamic characteristics of the antiparallel diode. Forward conduction and reverse recovery are the important phenomena since they account for the majority of power loss. The exponential static curve of

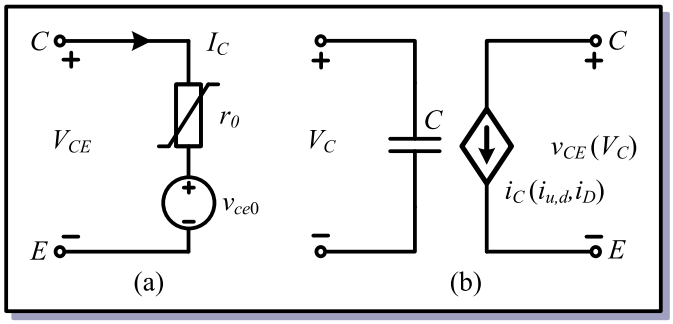


Fig. 3. Unified IGBT/diode pair behavioral model for (a) static characteristics and (b) dynamic features.

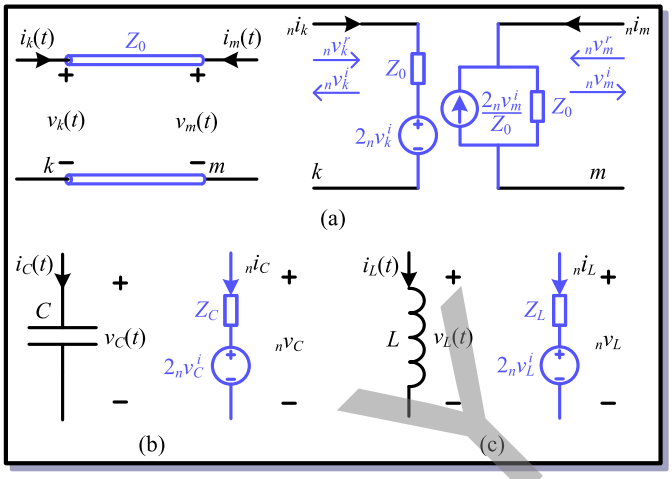


Fig. 4. TLM and the discrete-time equivalent circuit of (a) link, (b) capacitor, and (c) inductor.

diode is linearized in a similar fashion as the IGBT. Hence, it has the same form to (9) and is shown in Fig. 3(a). The nodes are denoted by those of the IGBT since the diode shares its terminals with it. During the diode reverse recovery process, the terminal voltage is still deemed as a controlled voltage source, whereas the current is a time-dependent current source, which is proportional to the static current. For example, the peak value of the reverse current is set as large as the value just prior to the process, and the sequence of coefficients k_1, k_2, and k_3 is in decline to represent the tailing current. Therefore, the transient model for IGBT and diode can be unified as a combination of the current-controlled current source and the voltage-controlled voltage source, as shown in Fig. 3(b).

III. MMC–IM System Equivalent Model

In the MMC, unlike other converters, the input vector **u** for the IM or its time-domain three-phase voltages cannot be instantly determined from the ON/OFF states of the switches due mainly to the existence of two arm inductors L_u and L_d. In addition, the IM state-space model (1)–(5) is not directly compatible with the MMC circuit network. Hence, an interface is introduced in which the machine is treated as a current source, whose values are fed to the MMC whose terminal voltages are in turn calculated and returned [42]. As with the large MMC network, solving directly its corresponding matrix equation established using either the mesh current or nodal voltage method would significantly slow down computational speed. Thus, a simplification of the circuit that could reduce the size of matrices is needed. In this paper, a mixed partitioning–merging approach is adopted: all submodules are separated from the MMC arms by TLM links to constitute individual subcircuits and the remaining parts in the arms are then merged. The benefits are twofold, details of each submodule and switch are retained, and solution of these subcircuits is much faster and easier due to the enabled parallelism so that real time is attained even though the time step is very small.

A. TLM Link and Stub

TLM has been utilized in large circuit simulations due to its capability to replace reactive components while maintaining high precision [35]–[37], [43], [44]. There are mainly two types of lossless transmission line models seen in the literature: link and stub. For the former, it is a two-port model of transmission line that has typically been used to decouple a large circuit into small subcircuits, leading to a reduction in sizes of the impedance and admittance matrices as well as a saving of calculation time. It is shown in Fig. 4(a), where $v_k(t)$, $i_k(t)$, $v_m(t)$, and $i_m(t)$ are the time-domain voltages and currents at terminals k and m, and Z_0 represents the line characteristic impedance defined by $\sqrt{L/C}$ Ω.

According to transmission line theory, the terminal voltage can be divided into two components: the incident pulse denoted by the superscript i and reflected pulse with the superscript r, as shown on the right-hand side of Fig. 4(a), where the discretized hybrid Thévénin–Norton equivalent circuit, rather than its Thévénin model, is adopted for the convenience of circuit calculation. In digital simulation, the two discretized pulses are linked by the present time step n and the next time step $n+1$, that is, ${}_{n+1}v_k^i = {}_n v_m^r$ and ${}_{n+1}v_m^i = {}_n v_k^r$, assuming that it takes one time step for pulses to travel from one terminal to the other, and then the following two equations are valid at both terminals:

$$ {}_n v_{(k,m)} = {}_n i_{(k,m)} \cdot Z_0 + 2_n v_{(k,m)}^i \tag{12} $$

$$ {}_n v_{(k,m)}^r = {}_n v_{(k,m)} - {}_n v_{(k,m)}^i. \tag{13} $$

Therefore, with discretization of the link, a circuit can be divided into two parts, meaning in digital simulation, these two subcircuits are independent when solving their respective matrix equations, the only connection between them being the update of incident pulses on both sides that takes place after the reflected pulses are obtained at the end of one time step.

The TLM stub is also a commonly seen modeling method being used to replace linear and nonlinear reactive elements in a circuit to solve complex lumped networks. Different from its link counterpart that is modeled into two separate parts, TLM stub is often treated as one element regardless of linearity [43], [44], as shown in Fig. 4(b) and (c), where their characteristic impedance take the form of $Z_L = 2L/\Delta t_1$ and $Z_C = \Delta t_1/2C$, respectively, and Δt_1 is the time step. It should be noted that the form discretized link and stub

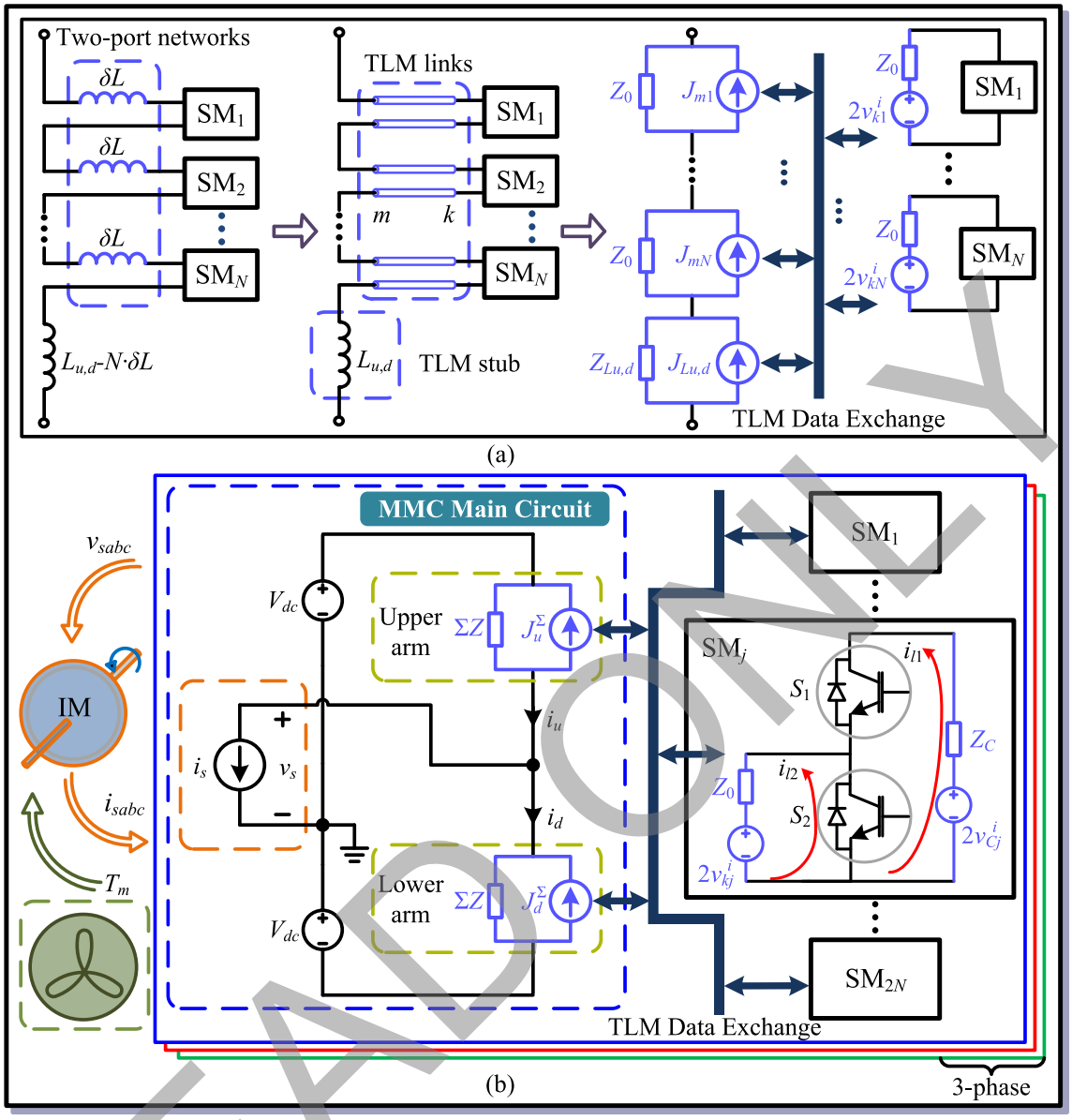


Fig. 5. TLM-based model for $(N+1)$-level MMC with IM interface. (a) MMC partitioning approach. (b) Discretized schematic for the overall system.

models take can convert validly between the Thévénin and Norton equivalent circuit models. Instead of other one-step integration approximations such as the trapezoidal rule and backward Euler, the stubs are used in this paper to replace arm inductors as well as dc capacitors in the MMC to constitute a unified TLM-based network.

B. Circuit Partitioning

As the three-phase MMC is symmetrical, it is reasonable to carry out analysis based on one phase. Fig. 5(a) shows the process of splitting the large MMC network consisting of a considerable number of nodes and meshes into several structurally independent, electrically related subcircuits. The arm inductor is first divided into $(N+1)$ parts, which are redistributed so that a new inductor δL is connected in series with each submodule to constitute a two-port network, and consequently, the remaining inductance for the arm inductor is $L_{u,d}$-$N \cdot \delta L$. Then, these new inductors are replaced by TLM links, discretization of which leads to the separation of submodules from the rest of the converter (MMC main circuit), enabling the replacement of the originally large impedance or admittance matrix by a number of submatrices with smaller dimensions, which if processed in parallel on the FPGA would be much more time and resource efficient.

The selection of the value of δL, which decides the characteristic impedance Z_0 and vice versa, plays a significant role on the emulation results. The principle is an appropriate value of δL that should lead to a tiny current change in the inductor within each time step [37]. Thus, the optimum value can be picked from its range by running MATLAB simulation of the MMC and comparing the current changes. It shows that the final value of δL is negligible compared with the arm inductance so that the latter can still be deemed as $L_{u,d}$.

TABLE II
HARDWARE UTILIZATION OF THE MMC–IM SYSTEM

FPGA Part	System	LUT	LUTRAM	FF	BRAM	DSP	f_{max} (MHz)
XC7VX485T	MMC5 ($3ph$)	232983 (76.74%)	1101 (0.84%)	134064 (22.08%)	55.50 (5.40%)	966 (34.50%)	116
	MMC7 ($1ph$)	113839 (37.50%)	496 (0.38%)	64175 (10.57%)	19.50 (1.89%)	490 (17.50%)	115
	MMC11 ($1ph$)	168122 (55.38%)	828 (0.63%)	109480 (18.03%)	21.50 (2.09%)	901 (32.18%)	116
	MMC5-IM	249123 (82.06%)	1343 (1.03%)	143411 (23.62%)	7 (0.68%)	1155 (41.25%)	115
XC7V2000T	MMC5 ($3ph$)	233238 (19.08%)	1113 (0.33%)	134064 (5.49%)	55.50 (4.29%)	966 (44.73%)	125
	MMC7 ($3ph$)	350245 (28.67%)	1485 (0.43%)	194071 (7.94%)	58.50 (4.53%)	1530 (70.83%)	121
	MMC11 ($1ph$)	168530 (13.80%)	825 (0.24%)	110760 (4.53%)	21.50 (1.66%)	901 (41.71%)	121
	MMC5-IM	250567 (20.51%)	1344 (0.39%)	143411 (5.87%)	7 (0.54%)	1155 (53.47%)	125

For the MMC main circuit where the Norton equivalent circuit part of TLM link's hybrid model locates, by merging all the Norton circuits in the upper and lower arms, respectively, there is actually only one node since the potentials at all other three nodes are known, as shown in Fig. 5(b), the overall schematic for the MMC–IM system. Then, the nodal voltage equation at nth time step can be derived by applying Kirchhoff's current law

$$ {}_n\mathbf{V}_s = \mathbf{G}^{-1} \cdot {}_n\mathbf{J} \tag{14} $$

where these 1×1 matrices are

$$ \begin{aligned} \mathbf{G} &= \left[\frac{2}{N\cdot Z_0 + Z_{Lu,d}}\right] \\ {}_n\mathbf{J} &= \left[\frac{{}_nJ_u^{\Sigma} - {}_nJ_d^{\Sigma}}{\Sigma Z} - {}_ni_s\right] \\ &= \left[2\cdot\frac{\sum_{j=N+1}^{2N} {}_n\upsilon_{mj}^i + {}_n\upsilon_{Ld}^i - \left(\sum_{j=1}^{N} {}_n\upsilon_{mj}^i + {}_n\upsilon_{Lu}^i\right)}{N\cdot Z_0 + Z_{Lu,d}} - {}_ni_s\right]. \end{aligned} \tag{15} $$

In (15), ΣZ and ${}_nJ_u^{\Sigma}$ and ${}_nJ_d^{\Sigma}$ are the impedance and current sources of the Norton equivalent circuit of an arm, respectively. The one-element voltage vector ${}_n\mathbf{V}_s$ is numerically equal to the stator voltage ${}_n\upsilon_s$. Also, it should be pointed out that all variables keep constant for a whole time step. Prior to calculating reflected pulses for the next time step using (12) and (13), the upper and lower arm currents should be updated based on the obtained nodal voltages, as briefly expressed by

$$ \begin{bmatrix} {}_ni_u \\ {}_ni_d \end{bmatrix} = \begin{bmatrix} \frac{1}{\Sigma Z} & \frac{-1}{\Sigma Z} \\ \frac{1}{\Sigma Z} & \frac{1}{\Sigma Z} \end{bmatrix} \begin{bmatrix} V_{\mathrm{dc}} \\ {}_n\upsilon_s \end{bmatrix} + \begin{bmatrix} -{}_nJ_u^{\Sigma} \\ -{}_nJ_d^{\Sigma} \end{bmatrix}. \tag{16} $$

The $2N$ subcircuits containing the Thévénin equivalent circuit part of the TLM link are identical, all with two meshes, so according to Kirchhoff's voltage law, the mesh current equations under steady state can be written uniformly as

$$ \begin{bmatrix} {}_ni_{l1} \\ {}_ni_{l2} \end{bmatrix} = \begin{bmatrix} Z_C + r_1 + r_2 & -r_2 \\ -r_2 & r_2 + Z_0 \end{bmatrix}^{-1} \begin{bmatrix} 2\cdot {}_n\upsilon_{Cj}^i \\ -2\cdot {}_n\upsilon_{kj}^i \end{bmatrix} \tag{17} $$

where ${}_ni_{l1}$ and ${}_ni_{l2}$ are mesh currents and Z_C is the characteristic impedance of dc capacitor. On the other hand, when the transient stage takes place, discretization of (11) leads to

$$ {}_ni_{C1,2} = {}_nk\cdot|{}_ni_{u,d}| \tag{18} $$

from which it is convenient to calculate the mesh currents by

$$ {}_ni_{l1} = {}_ni_{C1} \tag{19} $$

$$ {}_ni_{l2} = {}_ni_{C1} - {}_ni_{C2}. \tag{20} $$

Then, the voltage across each Thévénin equivalent circuit, regardless of the stage, can be calculated by

$$ \begin{bmatrix} {}_n\upsilon_{Cj} \\ {}_n\upsilon_{kj} \end{bmatrix} = \begin{bmatrix} -Z_C & 0 \\ 0 & Z_0 \end{bmatrix} \begin{bmatrix} {}_ni_{l1} \\ {}_ni_{l2} \end{bmatrix} + \begin{bmatrix} 2{}_n\upsilon_{Cj}^i \\ 2{}_n\upsilon_{kj}^i \end{bmatrix}. \tag{21} $$

Thus, calculation of reflected pulses can be carried out by substituting the acquired terminal voltages into (13), and the time step ends with updating the incident pulses.

IV. REAL-TIME HARDWARE EMULATION ON FPGA

A. Hardware Platform

The hardware design of the MMC–IM system was carried out on the Xilinx XC7VX485T-2FFG1761CES FPGA, which includes 303 600 lookup tables (LUTs), 607 200 flip-flops, 2800 DSPs, and 2060 block RAMs. Table II lists an estimation of hardware utilization when different levels of MMCs are implemented on two types of FPGA devices, and the maximum operational frequency $f_{\max}$ of each design is also shown. A higher operational frequency gives a larger speed margin for a certain time step, but the chip power dissipation increases along with it; on the contrary, a lower frequency leads to less power dissipation, but the design may fail to attain real-time execution. Therefore a tradeoff is made and the operational frequency of 100 MHz is chosen, with the corresponding clock period of the FPGA T_{clk} as 10 ns.

The hardware resources of XC7VX485T are sufficient for running a single-phase 11-level MMC but fall short of driving the IM with even a seven-level MMC due to a lack of LUTs. As can be seen from Table II, the demand for one phase accounts for 37.50% and will exceed the total available resources if the size triples. This can be avoided if the design is deployed to another FPGA device with abundant LUTs like the XC7V2000T, although it has fewer DSPs for implementing the three-phase 11-level MMC, as shown in Table II.

B. Controller Emulation

For the MMC–IM system, the control section is twofold, referred to as the MMC inner control and IM outer control, respectively. The former is in charge of the dc capacitor

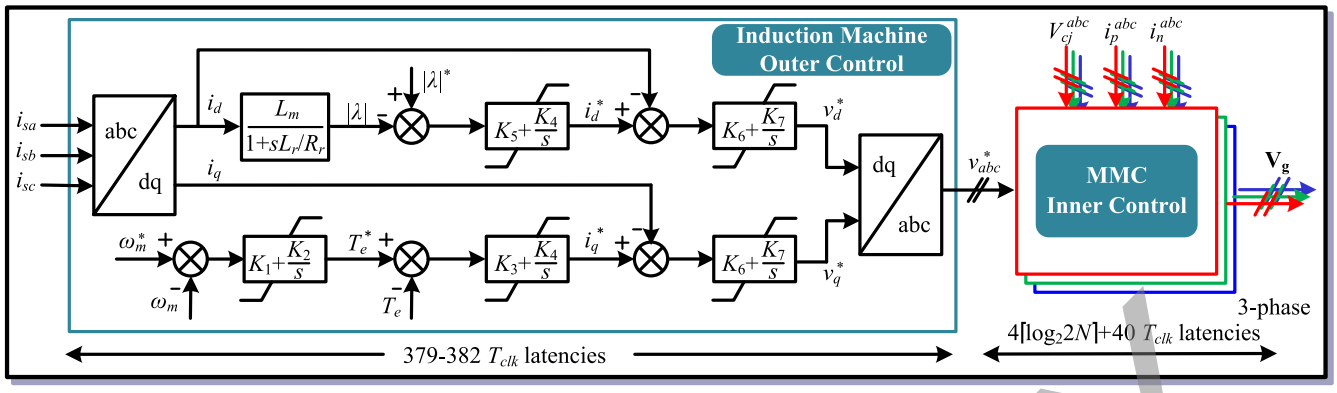


Fig. 6. Control algorithm for the MMC–IM system.

voltages of submodules and the latter regulates the IM's angular velocity. Detailed control algorithms for MMC and the IM have been separately developed [45]–[48], and their relations in HIL emulation are shown in Fig. 6. Three-phase stator currents i_{sa}, i_{sb}, and i_{sc} as well as ω_m and its reference ω_m^* are the inputs for the outer controller, which produces three-phase modulation signals v_{abc}^* and sends them to the inner controller as its inputs. Then the three-phase MMC inner controller generates driving pulses to control the switches.

As can be seen, regardless of what the conditions of surrounding devices such as the IM are, the hardware latency of the outer controller is restricted in a small range between 379 and 382 T_{clk}, while the latency of the inner controller is a logarithmic function of the number of submodules in a leg due to the averaging of dc capacitor voltages, and the hardware delay is

$$L_{\text{inner}} = (T_{\text{adder}} \cdot \lceil \log_2(2N) \rceil + 40) \cdot T_{\text{clk}} \tag{22}$$

where T_{adder} is the latency of the adder, which takes four clock cycles for single precision numbers, and the rounding function is equivalent to setting N to its nearest even number times of 4. Hence, for the five-level MMC that has eight submodules, the controller latency is 52 T_{clk}, or a 520-ns time delay, slightly over the time step of 500 ns for the MMC circuit, and for the seven-level MMC, this delay increases to 560 ns, so using the same time step would hinder achieving real time. The solution is to utilize multiple time steps for the subsystems: 1 μs for the MMC inner controller and 4 μs for the IM outer controller are applied. Theoretically, with this time step setting, the inner controller is able to deal with MMCs with thousands of levels for real-time HIL emulation purpose, but in reality, the number of voltage levels is restricted by hardware resources.

C. MMC Emulation on FPGA

Table III is a summary of the latencies of each hardware module in the five-level MMC–IM system and the emulation time steps for these subsystems. Based on the update frequency of variables, the whole system is dispatched to three layers, each satisfying the following criterion that ensures real time:

$$T_{\text{clk}} \cdot \max\left\{L_1^i, L_2^i, \ldots L_n^i\right\} \leq \Delta t_i \tag{23}$$

TABLE III
LATENCIES OF DIFFERENT HARDWARE MODULES IN THE FIVE-LEVEL MMC–IM SYSTEM

Hardware Module	Maximum Latency	Time-step	Layer
MMC main circuit	37 T_{clk}		
Induction machine	41 T_{clk}	Δt_1=0.5 μs	*Layer 1*
Submodule	37 T_{clk}		
MMC controller	52 T_{clk}	Δt_2=1.0 μs	*Layer 2*
IM controller	382 T_{clk}	Δt_3=4.0 μs	*Layer 3*

where $L_1^i, L_2^i, \ldots, L_n^i$ are the latencies of hardware modules that the ith layer with the time step Δt_i contains.

In order to run the five-level MMC HIL emulation in real time, the time step for *Layer 1* should be close to 370 ns, if the IM is not taken into account. According to the device datasheet, this minimum time step is approximately the rise/fall time of the selected Infineon IGBT FZ400R33KL2C_B5 (V_{CES} = 3300 V, I_C = 400 A) when its gate resistor is 10 Ω. This means that under these circumstances, a maximum of two values can be caught during rise/fall process and that section of the switching curve is straightened. On the other hand, the transient process is not limited to the aforementioned region and there are other sections of the curves that distribute beyond it; thus, the time step can be set a little larger to 500 ns and the voltage and current waveforms can be represented by piecewise linearized lines, one of which contains the rise/fall process.

Table III also shows that the IM has the largest latency in *Layer 1*. However, when the number of submodules increases, as the only part whose latency is affected, the MMC main circuit latency begins to overtake the IM as the dominant factor to determine real-time operation. The latency incremental for $(M+1)$-level MMC main circuit can be deduced from its $(N+1)$-level counterpart by

$$\Delta t_{N\to M} = \left(T_{\text{adder}} \cdot \left\lceil \log_2 \frac{M+1}{2^{\lceil \log_2(N+1) \rceil}} \right\rceil\right) \cdot T_{\text{clk}}. \tag{24}$$

Thus, the maximum number of levels that can achieve for real-time HIL emulation with a 500-ns time step is 64, when the latency of the MMC main circuit reaches 49 T_{clk}.

The hardware structure and signal flow routes for the MMC–IM system are drawn in Fig. 7, where jth submodule

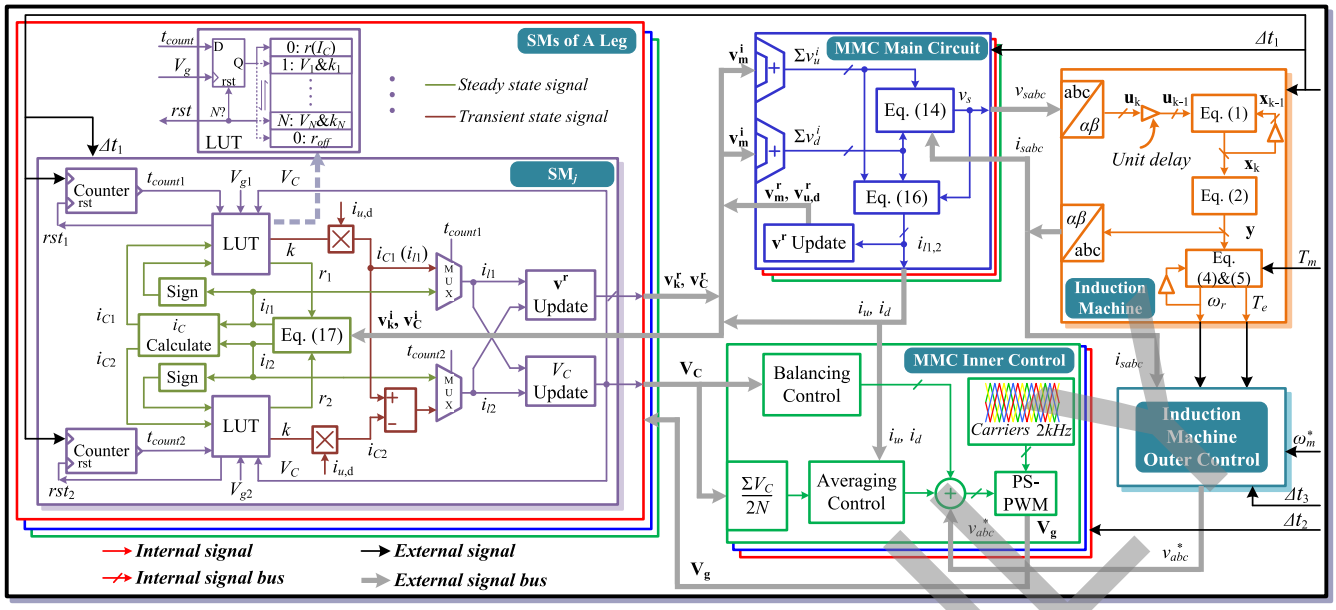


Fig. 7. Hardware structure and signal flow diagram for the FPGA emulation of the MMC–IM system.

structure can be seen out of the total $2N$ submodules. There are two levels of parallelism in the design: layers with different time steps run simultaneously, and all hardware modules within a certain layer are also in parallel. In *Layer 1*, after each time step Δt_1, the MMC main circuit exchanges TLM link information with the submodules and updates the three-phase voltages for the IM, from which stator currents are received. Then there are information exchanges between the layers. Data going to the IM outer controller will not take effect unless an entire time step Δt_3 ends and produces the three-phase modulation waves for the inner one. For *Layer 2*, since Δt_2 is between two other time steps, the values of modulation waves are kept constant for $(\Delta t_3/\Delta t_2)$ cycles and the dc capacitor voltages $\mathbf{V_C}$ and arm currents from *Layer 1* can participate in the control only when a new time step begins. One of the benefits with such a hardware design is that all external and internal signals as well as the hardware other than LUTs in the submodules will not change if a new piecewise linear switch model is established to replace the original one. Even if a more complex switch model such as physics-based model is introduced, the only alteration occurs within submodules and thus there is no necessity to redesign the hardware for other parts.

With regard to the specific structure of each hardware module, Xilinx Vivado HLS helps to shorten the design process by providing a platform with which users are enabled to code by C/C++. In this hardware design, there are totally five types of function blocks: the IM, the MMC main circuit and submodules, as well as the two controllers. Each is coded as an independent function in a separate program, whose inputs and outputs include all external signals of that block. Meanwhile, detailed mathematical as well as logic operations within a function block, such as those in Fig. 7, are represented by the programming language in a pipelined fashion. Although Xilinx Vivado HLS also has a pipeline directive option, which could further increase the maximum

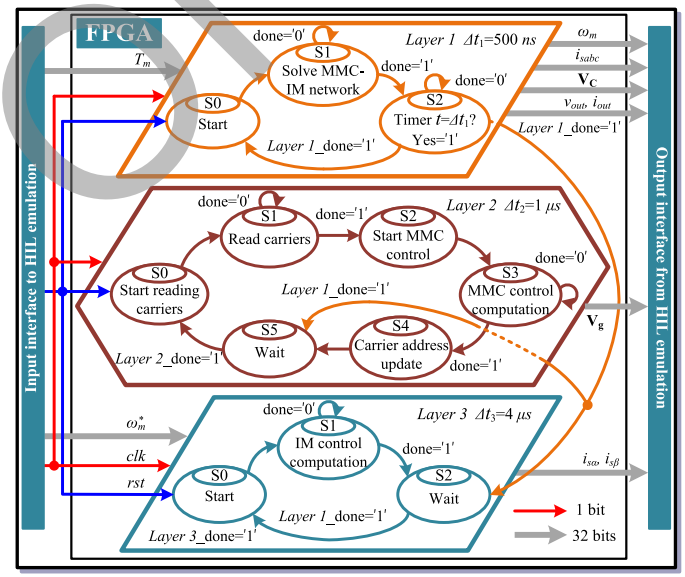


Fig. 8. FSM of the overall MMC–IM system for hardware emulation.

operational frequency of the designs, it was not used because the frequency improvement is at the cost of more hardware resource utilization and 100 MHz was deemed sufficient to ensure real-time execution. By running C synthesis of the completed code and the exporting RTL operation that follows, an IP core, the hardware module corresponding to the function block, is generated. However, these modules are yet to be linked with each other. This is realized by VHDL coding in the form of signal exchange that takes place at the end of every time step, and so is the finite state machine (FSM) that achieves the multilayer design and decides the time sequence of each module.

Fig. 8 shows the relationship between different layers and how they cooperate to execute the entire MMC–IM system by FSM. It should be pointed out that the maximum latency in each layer is smaller than corresponding time step, meaning

TABLE IV
PARAMETERS OF MMC–IM SYSTEM

(N+1)-level MMC parameters		
Arm inductance	$L_{u,d}$	$1mH$
MMC test load	$R-L$	5Ω-$2mH$
Submodule capacitance	C_{1-2N}	$6mF$
Submodule DC voltage	$V_{C_{1-2N}}$	$\frac{2V_{dc}}{N}$
Induction machine parameters		
Stator inductance	L_s	$35.5mH$
Rotor inductance	L_r	$35.5mH$
Magnetizing inductance	L_m	$34.7mH$
Stator resistance	R_s	0.087Ω
Rotor resistance	R_r	0.228Ω
Inertia	J	$1.662Kg \cdot m^2$
Number of poles	P	4

that the MMC–IM system will proceed *faster* than real time. Therefore, a timer is introduced in *Layer 1* to achieve exact real time; when it counts to Δt_1, that value is reset and the calculation for the next time step begins. The command is also sent to the other two layers to enable their respective FSMs to enter a new stage, if they are already waiting. In *Layer 2*, the values of carriers are needed before the control starts, and near the end of each time step, the carrier addresses are updated so that in the next time step new values can be referred to. For the last layer, the operation is similar to the first layer, other than the fact that shifting to state *S*0 is controlled by the command from the latter. When the reset order is issued, the states in all three layers begin to circulate and the HIL emulation of the MMC–IM system is ongoing. Thus, by giving proper speed and torque orders through the input interface, the status of the overall system can be observed via the output interface.

V. REAL-TIME EMULATION RESULTS

A. MMC

In this section, functions of different levels of MMCs are tested with *R–L* load. In the test, the dc line voltage is maintained at $2V_{\rm dc} = 900$ V, meaning that when the number of levels increases, the dc capacitor voltages will decline accordingly. However, the values of other circuit components such as the arm inductance will not be changed, as shown in Table IV, and the switching frequency is 2000 Hz. To validate the results from HIL emulation, SaberRD simulations are also carried out with a maximum time step 500 ns to ensure transient processes are recorded. The IGBT and diode models employed in simulations are *igbt1_3* and *dp1*, respectively.

In Fig. 9, specific system-level performances of the five-level MMC and its seven-level counterpart are shown. Fig. 9(a) and (d) shows the 60-Hz single-phase output voltages of the five-level and seven-level converters, respectively. As can be observed, the voltage waveform in the latter has two more levels than the former, but their peak values are virtually the same, both close to 430 V, and high symmetry is also observed. Moreover, voltage spectral analysis is carried out by the oscilloscope, which demonstrates that for the five-level MMC, its output voltage harmonics mainly distribute around 8 kHz, four times higher than the switching frequency, while for the seven-level converter, the major harmonics center around 12 kHz. This phenomenon agrees with the theory that for $(N+1)$-level MMC, the effective switching frequency is *N* times higher. The results are verified by SaberRD simulations as they give identical waveforms. Fig. 9(b) demonstrates the upper and lower arm currents of the five-level converter, and the results from oscilloscope and simulation agree with each other quite well in both waveshape and values. Fig. 9(c) shows the dc voltage ripples of the submodules in upper and lower arms for the five-level converter. These values fluctuate around the reference of 225 V, indicating that the inner controller is working properly. The peak valley difference is estimated to be around 13.3 V from the oscilloscope and simulation. In Fig. 9(e) and (f), some dc capacitor voltages of seven-level MMC are shown and compared. The former indicates that for submodules in the same arm, the rising/declining trends of dc voltage ripples are same, while the latter shows the trend in the opposite arm is totally in contrary. The average values of these dc voltages, as can be read from Fig. 9(e) and (f), are about 150 V since the number of submodules in an arm increases to six while dc line voltage is kept constant.

Fig. 10 gives the switching process and power losses in the five-level MMC and the shape of these waveforms in seven-level MMC are almost the same and are therefore not shown. Fig. 10(a) and (b) shows the transient IGBT voltage and current waveforms during the turning ON and OFF processes. After exerting a positive driving pulse on the gate and a period of turn-ON delay lasting for 1 μs, the voltage begins to drop and a current surge can be observed from both HIL emulation and SaberRD simulation. Then the current gradually stabilizes and the voltage finally remains slightly above zero due to the conduction resistance. The rise time is defined as the time interval between 10% and 90% of collector current under steady state, which is around 0.33 μs, slightly below 0.4 μs provided in the datasheet. When the driving pulse disappears, the turning OFF process takes place after a turn-OFF delay of approximately 4 μs; it is an opposite process during which $v_{\rm CE}$ rises to dc capacitor voltage and collector current goes to zero, but the fall time has a similar definition to rise time and its value is near 0.42 μs, a little larger than the datasheet value of 0.35 μs. In Fig. 10(c), diode reverse recovery process is shown. As can be seen after plunging to peak value, which virtually has the same amplitude as the steady-state current, the reverse current begins to decay to zero and voltage over the diode climbs to dc capacitor voltage. It is observable that the current tail in the SaberRD simulation is a little longer, but since the value of the final stage is extremely small, it is forced to zero in the diode model and that will not cause a significant error when calculating power loss. Meanwhile, the forward voltage of diode is also nonzero attributing to the exponential static *I–V* characteristics. The power loss corresponding to each process is also shown, and a high degree of consistency between HIL emulation and SaberRD simulation is observed.

To validate the effectiveness and convenience of the proposed circuit partitioning method in achieving real time, the 7-level MMC is expanded to 11-level and emulated execution on the FPGA. Fig. 11(a) shows the 11-level output voltage and

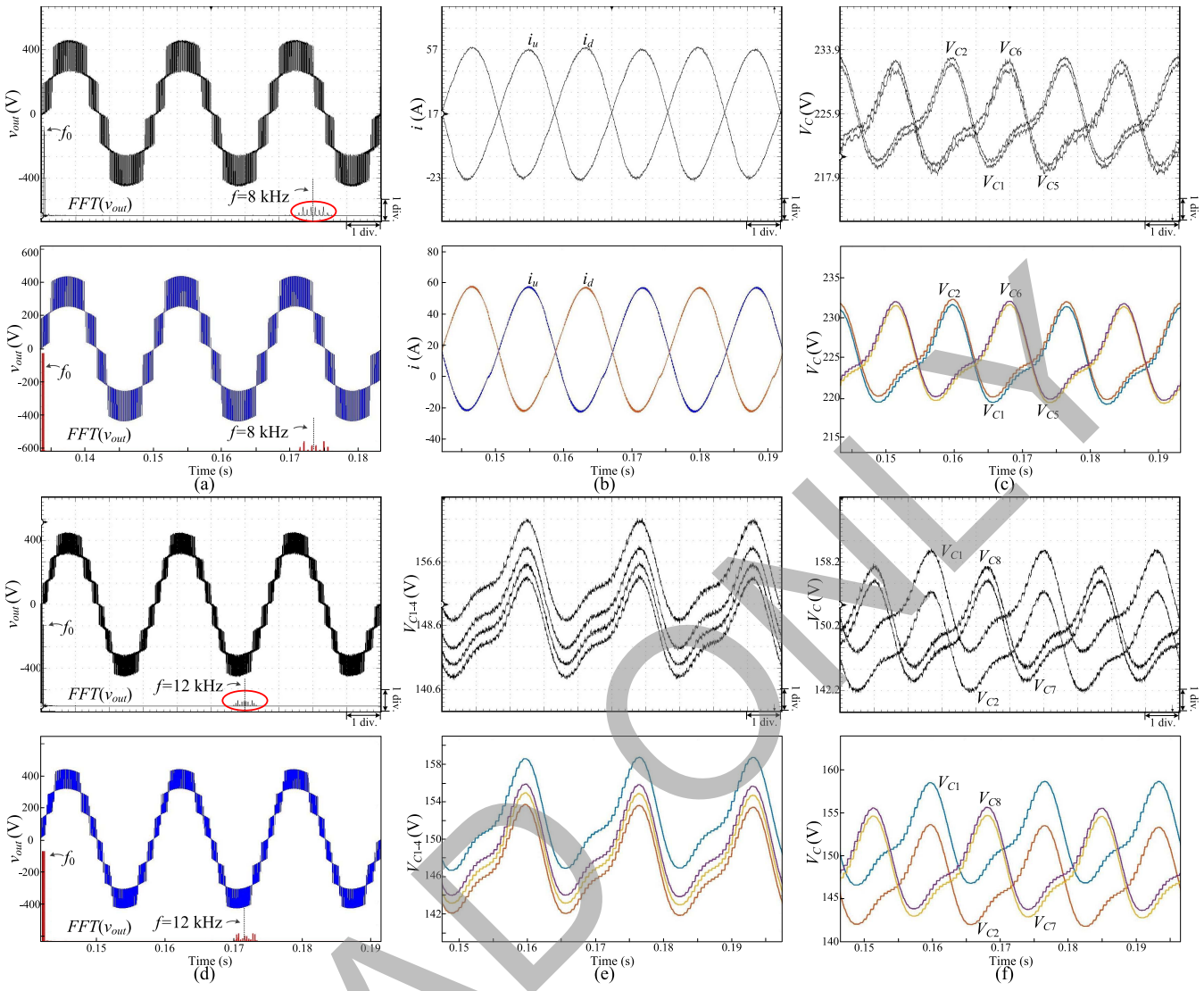


Fig. 9. Comparison of performances of five-level and seven-level MMC between real-time HIL emulation (top) and SaberRD (bottom). (a)–(c) Five-level MMC output voltage, arm currents, and dc voltage ripples of submodules in upper and lower arms. (d)–(f) Seven-level MMC output voltage and dc voltage ripples of submodules. Oscilloscope axis settings are (a) and (d) x-axis 5 ms/div, y-axis 133.34 V/div (v_{out}) and 66.67 V/div (FFT); (b) x-axis 5 ms/div, y-axis 13.333 A/div; and (c), (e), and (f) x-axis 5 ms/div, y-axis 2.667 V/div.

the load current from HIL emulation, compared with those of five- and seven-level MMCs. The voltage quality is higher and as anticipated that the voltage spectral analysis yields an array of harmonics around 20 kHz, but they are almost negligible. The root-mean-square value of fundamental component is the same as those of other two, all about 280 V. The output current, due to filtering effect of inductors, is sinusoidal and it reaches a peak value of 80 A, and agrees with its theoretical value. The results from SaberRD are also shown in Fig. 11(b) for comparison, which indicates that the hardware implementation of MMC is correct.

Table V lists the time each switching process takes. The IGBT turn-ON delay from HIL emulation is exactly what was provided in the datasheet, while its turn-OFF delay and diode reverse recovery time are both rounded to integers because the HIL emulation time step is 500 ns. The errors for IGBT rise and fall time are relatively large, because their values are smaller than the time step, and consequently, both processes are located on straightened lines and affected by the slopes.

TABLE V
SWITCHING TIMES OF IGBT AND DIODE

Time	Description	HIL	Datasheet/SaberRD®
$t_{IGBT}^{d,on}$	Turn-on delay	1.00 μs	1.00 μs
t_{IGBT}^{r}	Rise time	0.33 μs	0.40 μs
$t_{IGBT}^{d,off}$	Turn-off delay	4.00 μs	3.90 μs
t_{IGBT}^{f}	Fall time	0.42 μs	0.35 μs
t_{diode}^{rr}	Reverse recovery time	5.00 μs	4.80 μs

For the upper switch in a submodule, the maximum current flows through the antiparallel diode, while for the lower switch, the maximum current emerges in the IGBT; thus, their power losses are important. Table VI shows the maximum

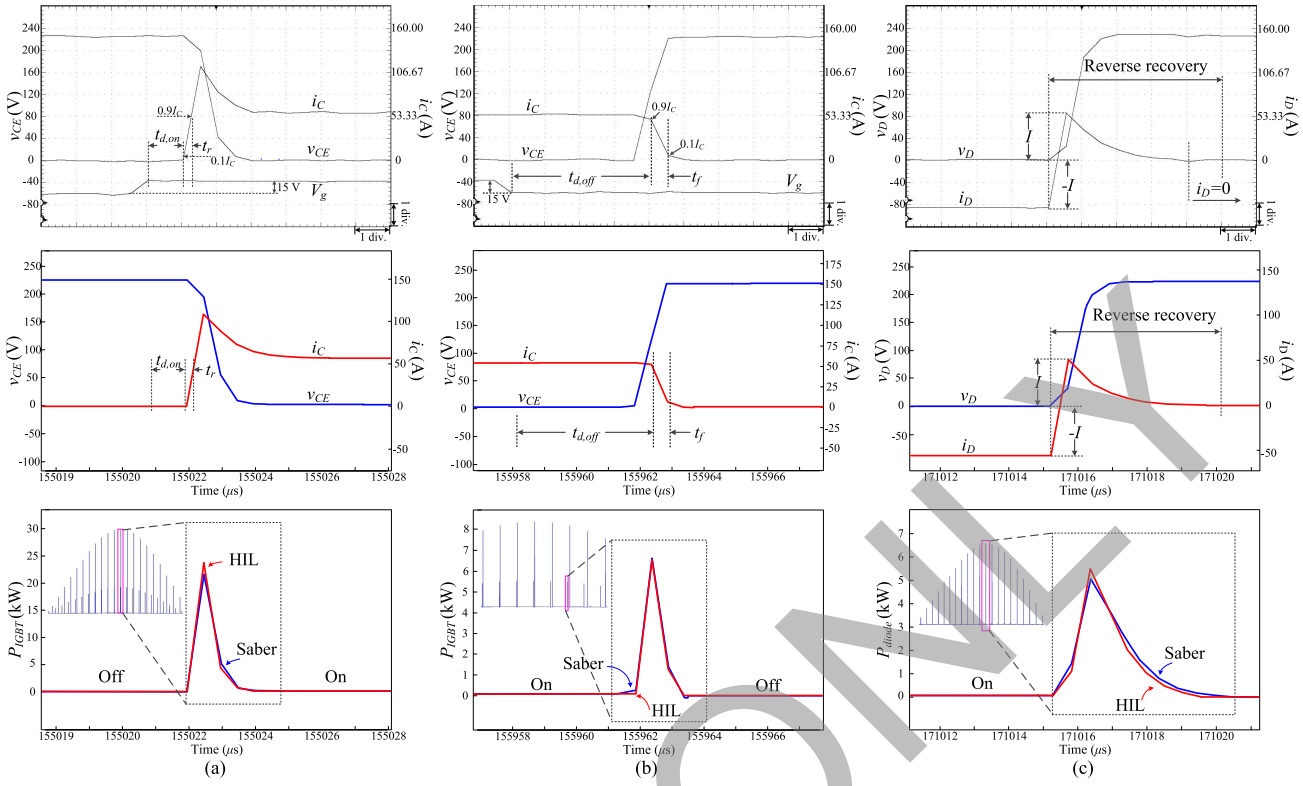


Fig. 10. Details of switching processes and power losses of IGBT or diode from HIL emulation (top) and SaberRD simulation (bottom). (a) IGBT turning ON, (b) IGBT turning OFF, and (c) diode reverse recovery. Oscilloscope axis settings: x-axis 1 μs/div, y-axis 40 V/div and 26.67 A/div.

TABLE VI
MAXIMUM POWER LOSS OF IGBT AND DIODE

MMC	5L-MMC		7L-MMC	
Power (W)	HIL/SaberRD®	Error	HIL/SaberRD®	Error
P_{IGBT}^{on}	7005.2/6713.3	4.35%	3961.5/4164.5	4.87%
P_{IGBT}^{off}	3751.3/3983.7	5.83%	3181.0/3195.9	0.47%
$P_{IGBT}^{conduct}$	103.4/102.9	0.49%	96.16/95.47	0.72%
P_{diode}^{rr}	1856.3/1911.8	2.90%	937.3/1006.2	6.84%
$P_{diode}^{conduct}$	70.05/70.20	0.21%	67.65/65.51	3.27%

power loss of IGBT and diode during the transient process and steady state in five- and seven-level MMCs, where the errors are in their absolute forms to avoid negative values. As can be seen from Fig. 10, the maximum steady-state current for both IGBT/diode pairs is about 60 A.

The steady-state power losses are quite accurate because the static V–I characteristics are provided in the datasheet, whereas the transient waveforms are obtained by curve fitting, and therefore, the error is a bit larger, but still they are precise and can be referred to when designing the MMC as well as the cooling system. Moreover, with the increase of output voltage level, the power consumed by switches decreases along with voltage and current stresses. Generally, the proposed HIL system is able to offer accurate power losses of both steady-state and transient stages in the MMC despite the variation of its voltage level and the load. It is more convenient compared with measuring power losses by setting up an experimental MMC prototype whose excitations as well as the loads should be adjusted repeatedly in order to provide the switches with the same electromagnetic environment. In addition, although knowing the steady-state current from simulation of conventional MMC models with ideal switches enables direct acquisition of steady-state power loss from the device datasheet, estimating the transient portion based on the turn-ON and turn-OFF energy losses provided by datasheet is less accurate, since they were obtained in an experimental setup with distinct testing conditions.

B. Induction Machine Driven by Five-Level MMC

The speed of the IM can only be regulated by the five-level MMC when the emulation was done on the XC7VX485T FPGA. As shown in Table II, the LUT is not enough for the other two MMCs to extend to three phases.

Fig. 12(a) shows the regulation of the mechanical angular velocity by real-time HIL emulation. The initial speed reference is 160 rad/s, so the machine starts and the velocity goes up to the reference value in about 1 s. Meanwhile, a large stator current can be observed in all three phases and only phase A is shown since they are symmetrical. After 1 s, the actual speed is very close to the reference and the machine operates under steady state with stator currents reducing significantly to around 20 A in amplitude. Then at $t_1 = 3$ s, ω_m^* plummets to -160 rad/s, meaning that the rotation direction is reversed, so that the positive speed slows

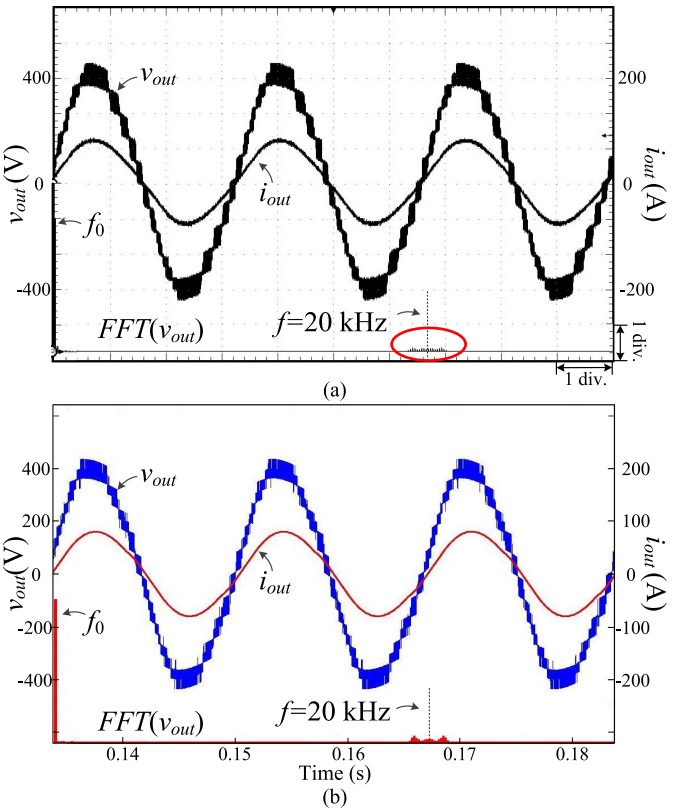


Fig. 11. System-level behavior of 11-level MMC. (a) Real-time oscilloscope results. (b) SaberRD simulation results. Oscilloscope axis settings: x-axis 5 ms/div, y-axis 133.34 V/div (v_{out}), 66.67 V/div (FFT), and 66.67 A/div.

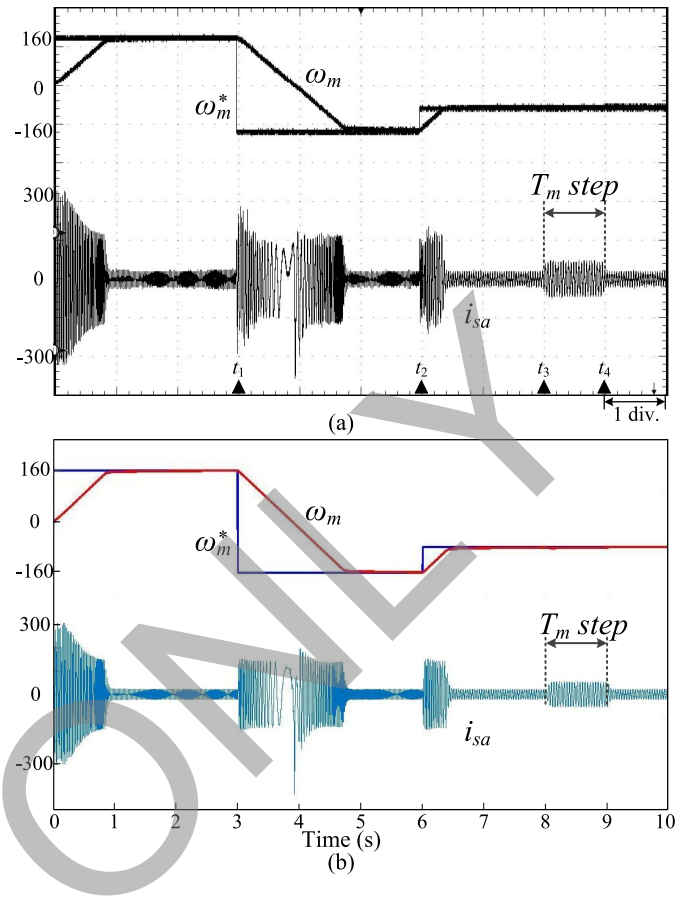


Fig. 12. Regulation of IM speed by the five-level MMC. (a) Real-time oscilloscope results. (b) Offline simulation results. Oscilloscope x-axis: 1 s/div.

down to zero and later increases in the opposite direction until it reaches the reference value, which sees a slight increase at $t_2 = 6$ s to -80 rad/s. Consequently, the real speed follows and the machine quickly enters steady state. Between $t_3 = 8$ s and $t_4 = 9$ s, a pulse of 100 N·m is applied to the torque; following this change is a temporary rise of stator current, but the impact it has on the angular velocity is negligible. As can be seen throughout the whole period, a large angular velocity leads to a higher current frequency demonstrated by the density of the waveform. For comparison, MATLAB/Simulink simulation is carried out, and corresponding system-level performance is shown in Fig. 12(b), which proves that both controllers are functioning normally and the design theory is correct.

The starting of the IM with different values of torques was also tested. In Fig. 13(a), the loci of stator currents in α–β frame are drawn for the starting period when the mechanical angular velocity climbs up from 0 to 160 rad/s without any load. A momentary current surge at the vertical axis is observed immediately after starting, indicated by curve A. Then, as can be seen from curve B, the current steadily reduces from 300 to 150 A, and following a sudden decline shown by curve C, the current finally stabilizes around the region D.

The loci of stator currents for three torques under steady state are shown in Fig. 13(b). As expected, it shows that a larger torque yields a circle with greater radius. Other information such as the relation between the duration of transient process and torque is also available. When $\omega_m^* = 160$ rad/s,

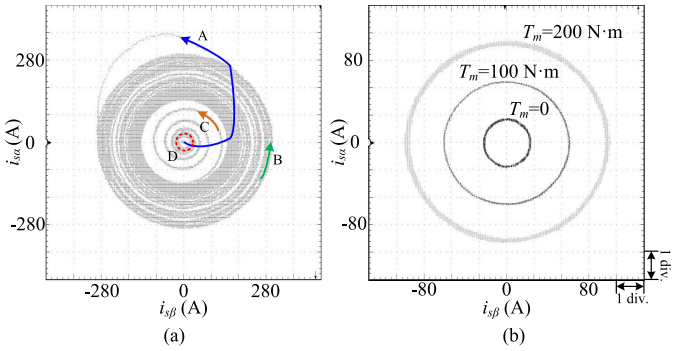


Fig. 13. Real-time oscilloscope results of stator current in α–β frame under (a) starting period and (b) steady-state with $T_m = 0$, 100 and 200 N·m, respectively. Oscilloscope x- and y-axis settings. (a) 93.34 A/div. (b) 26.67 A/div.

it takes 0.52, 0.65, 0.86, 1.31, and 2.68 s for the machine to reach 95% of ω_m^* when the torques are -200, -100, 0, 100, and 200 N·m, respectively, indicating that a larger torque leads to a longer time to approach steady state, while the reverse is true for $\omega_m^* = -160$ rad/s.

VI. Conclusion

This paper has demonstrated real-time hardware emulation of a TLM-based MMC structure with a detailed behavioral IGBT/diode model for variable-speed drive applications. From

a mathematical point of view, using TLM links to partition the MMC circuit achieved the decomposition of a large matrix equation corresponding to the integral circuit by a set of smaller equations, which when solved in parallel, significantly accelerated computational speed even though the emulation time step was small. Meanwhile, it offered a new perspective for hardware design in which the overall system is represented by several hardware modules and any change specific to one of them has no impact on others; thus, scalability and modularity are attained, just as in a real MMC system. Moreover, the computational speed is entirely independent of the number of output voltage levels of the converter. The only impact is on the utilization of hardware resources, as several hardware designs have shown in the results, which helped to determine the appropriate voltage level according to the capacity of the FPGA device. MMCs of different levels were implemented, where the behavioral IGBT/diode model enables HIL emulation to provide accurate system-level performance as well as device-level information such as turn-ON/-OFF time and power losses. Implementation of the MMC inner controller and IM outer controller was also carried out. Multiple time steps are particularly useful when there is a remarkable latency disparity between different hardware modules. A comparison of waveforms of MMCs and the IM between HIL emulation and offline simulation tools indicates that the hardware implementation of the MMC–IM system gives accurate results and can therefore be referred to when designing a real MMC system. Future work will focus on improving the proposed switch models to make them more adaptive to various electromagnetic environments, and more complex nonlinear IGBT and diode models readily available in literature will also be implemented in HIL emulation of the MMC as well as other power electronic systems.

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