UNIVERSITY OF ALBERTA

TEMPERATURE-STABLE VOLTAGE TO FREQUENCY CONVERTERS

BY

SEAN SIDONG CAI ©

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND

RESEARCH IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING, 1995

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Name of Author: SEAN SIDONG CAI

Title of Thesis: TEMPERATURE-STABLE VOLTAGE TO FREQUENCY CONVERTERS

Degree: MASTER OF SCIENCE

Year this Degree Granted: 1995

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled **Temperature-Stable Voltage to Frequency Converters** submitted by **Sean Sidong Cai** in partial fulfillment of the requirements for the degree of **Master of Science**.

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ABSTRACT

An overview of voltage to frequency converters (VFCs) is given in this thesis. Comparing with charge-balance VFCs, multivibrator VFCs are more widely used in monolithic analog integrated circuit design. The two different multivibrator VFCs, one with floating and the other with grounded timing capacitor, are compared for further studies. A flexible voltage to frequency converter topology is presented. Based on this topology, the design technique is developed. The threshold voltage V_H - V_L is very critical and can be realized with good temperature stability in a VFC design. This is proved in the design of a modified multivibrator circuit which is simple but has high performance specifications. The circuit can be used as a general VFC building block.

The approach was also used to design a bipolar high precision voltage to frequency converter. The circuit consists of Zener diode voltage reference circuit, voltage to current converter and current-controlled multivibrator. The multivibrator includes a window comparator with a limiter for the output voltage swing. The window comparator allows the upper and lower thresholds to be precisely set. The thresholds can be applied to the comparator respectively. The circuit simulation shows that the converter provides an accuracy better than 2% in 100 Hz to 100 kHz frequency range and exhibits good temperature stability. The breadboarded circuit was finally tested in the temperature range from -25°C to 75°C and provided a temperature coefficient of the output frequency less than 60 ppm/°C. The converter can be fabricated using ASIC process and is suitable for many applications in data-acquisition systems.

The components of dielectric isolation and junction isolation processes for optimum high-temperature performance are analyzed and characterized over the temperature range 25°C to 300°C. High-temperature parameters which pose special design problems are noted and methods for overcoming the problems are described. The research shows that the voltage to frequency converter topology has more flexibility and is suitable for different environmental conditions.

ACKNOWLEDGEMENTS

The author would like to express his deep gratitude to his supervisor Dr. I. M. Filanovsky for his guidance and encouragement throughout the whole graduate program.

The financial support for this research provided by the Alberta Microelectronic Centre and the University of Alberta is greatly appreciated.

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LIST OF ABBREVIATIONS AND SYMBOLS

ADC	analogue to digital converter
A_{OL}	open loop gain
ASIC	application specific integrated circuit
BiCMOS	bipolar complementary metal oxide semiconductor
C	capacitor
CCO	current controlled oscillator
CMOS	complementary metal oxide semiconductor
C_T	timing capacitor
DA	dielectric absorption
DI	dielectric isolation
ECL	emitter-coupled logic
ECM	emitter coupled multivibrator
EXT	external
f	oscillation frequency
FET	field-effect transistor
FPLD	field-programmable logic device
FVC	frequency to voltage converter
GaAs	gallium arsenide
g_m	transistor transconductance
g_{mTOT}	total differential pair transconductance
I	current
JI	junction isolated
PLL	phase-locked loop
PTAT	proportional to absolute temperature
Q(#)	transistor number

R_L	load resistor
R_T	external timing resistor
R_{TH}	threshold resistor
SHA	sample-and-hold amplifier
SPICE	circuit simulation program
TC	temperature coefficient
V_C	voltage across the timing capacitor
V_{CC}	positive supply voltage
VCC	voltage to current converter
VCO	voltage controlled oscillator
VFC	voltage to frequency converter
V_H	upper threshold voltage
V_L	lower threshold voltage
V_{ref}	reference voltage
V_T	thermal voltage (kT/q)
V_{TH}	threshold voltage
δV	hysteresis voltage
ΔV	voltage swing across the timing capacitor

1 INTRODUCTION

1.1 Applications of VFCs

A voltage to frequency converter (VFC) is a device which accepts at its input an analog voltage or current signal and provides at its output a train of pulses or square waves at a frequency which is proportional to the input value. A VFC is a useful and versatile electronic building block. It can be used as a voltage controlled oscillators (VCO) for generation of clock signals for timing applications, and for generation of carrier signals which can be modulated in amplitude and frequency to facilitate the transmission of information. More complex systems such as frequency synthesizers, tone decoders, and phase lock loops (PLLs) also use the VCO as a key element. A PLL is an extremely useful device: among its many applications are AM and FM demodulation, clock recovery, carrier synchronization, and signal conditioning. VFCs have also found application in the area of integrated silicon sensors, providing conversion of the sensor's output signal (typically a voltage) into a frequency signal, to improve noise immunity during transmission and to allow the multiplexing of many sensor outputs onto a single transmission line. One can conclude that a VFC is rarely used as a single block; usually it is only one element of a larger system. However, the performance of the overall system is often strongly influenced by the characteristics of the VFC. Consider, for example, the PLL. The VCO is the critical block in a PLL, determining the stability of the center frequency, distortion in FM demodulation applications, high frequency capability and, possibly, the tracking range.

In many telemetry, remote control, and remote data gathering applications it is advantageous to convert the analog information into a frequency, which can be transmitted and measured, or recorded, more accurately than an analog voltage or current signal. This is particularly true if the signal transmission path is quite long and noisy.

One can convert the signal into frequency using a voltage-to-frequency converter

(VFC), a circuit whose output is a frequency proportional to its input. It is relatively easy to send a frequency signal without interference over a long transmission path, via optical isolators, optical fibre links, twisted-pair or co-axial lines, or radio links. An example of such system is shown in Figure 1.1.

The receiving frequency is reconverted to analog voltage by a "frequency-to-voltage converter" (FVC). This is generally a VFC configured to perform its inverse function, often using a phase-locked loop. If the transmitted data must be digital, the receiver will include a frequency counter, easily implemented in a single-chip microcomputer.

1.2 VFC Performance Parameters

Voltage-to-frequency (V/F) converters are a class of circuits designed to produce an output frequency directly proportional to an analog voltage input signal. These circuits are basically encoder circuits, whose function is to encode an analog signal into a stable frequency, which can then be transmitted over long distances or measured and recorded by digital means. Compared to the ordinary voltage-controlled oscillator circuits, V/F converters have some very stringent performance requirements depending on the dynamic range, precision, and resolution requirements of the analog data. Some of the performance requirements commonly encountered in most data encoding applications are:

1. Dynamic Range. A V/F converter is required to have at least 60 dB (i.e., 1000:1) dynamic range in terms of its input voltage range.

2. Frequency Range. This defines the range of output frequencies corresponding to the analog input dynamic range. For a 60 dB dynamic range, the output frequency is typically in the range of 10Hz to 10 kHz or 100 Hz to 100 kHZ.

3. Linearity. The V/F conversion characteristics are required to be extremely linear, with a nonlinearity error less than 1% of full scale. In precision designs, these linearity errors must be kept to < 0.1%.

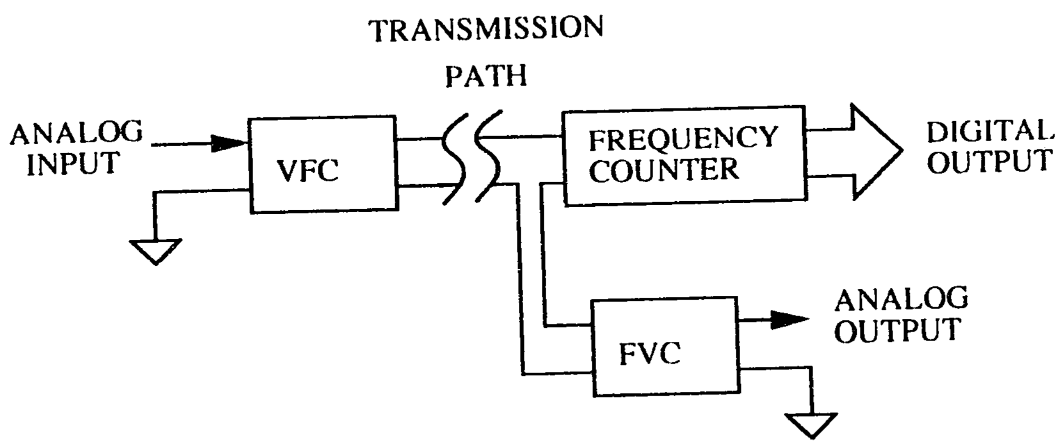


Figure 1.1 Data transmission system based on VFC

4. Scale-Factor Accuracy. Normally, the scale factor or gain is externally adjusted for a given conversion gain setting.

5. Scale-Factor Stability. At any given gain setting, the scale factor (and the output frequency) must be stable with temperature and power supply changes. Typical stability requirements are on the order of ≤ 100 ppm/°C drift with temperature and ≤ 0.1%/V change with power supply.

6. Output Waveform. The output waveform of V/F converter is, in general, not a critical factor as long as its levels are compatible with logic signals. Most V/F converters produce constant-width output pulses whose repetition ate, that is, frequency, is proportional to an input voltage.

1.3 High Temperature VFCs

The design of a high temperature precision VFC is driven by the instrumentation needs of the oil and gas well testing industry. A common form of well testing is to lower a probe into a well to measure the reservoir temperature and pressure. In deep wells, the probe electronics may be required to operate in temperatures as high as 200°C. Therefore to avoid signal degradation, an analogue to digital converter (ADC) or a VFC is used to convert the pressure transducer output voltage into a more robust digital format.

Precision high temperature VFCs are also required in areas such as industrial process control and automotive engine monitoring. Whenever a sensor must be placed in a hot environment, the ability to also place some signal processing circuitry in site with the sensor opens up the possibility of using a less sophisticated and therefore less expensive sensor.

The maximum temperature rating for commercial semiconductor devices with military specifications is usually 125°C. Only a few specialized components are available with higher temperature rating. As a result, many high temperature instrumentation systems are constructed by screening standard components at the desired operating temperature and selecting those that meet the required specification.

A temperature-stable monolithic VCO can be a very important building block for such data-acquisition systems. The development of a VCO with low temperature coefficient is the goal of this work.

1.4 ASIC Design

Application-specific integrated circuits (ASICs) are integrated circuits designed for a specific purpose, containing all the functional elements for the task on a single chip. An ASIC is dedicated to a single function, or limited range of functions, and is generally fabricated in batches of ten to ten thousand units, such as in a compact disc player or a telecommunications system. ASICs stand in sharp contrast to standard IC products such as memories or microprocessors which are typically designed for use in a wide range of applications. In addition to being a class of IC products, ASICs also define a design style or methodology which is based on the extensive use of circuit libraries with computer-aided design (CAD) tools and systems. ASICs are typically designed, at least in part, by someone other than the semiconductor vendor's personnel. Most often, the designer is the customer. This fact, coupled with differences in design objectives such as performance, area, and time to market, further differentiates ASICs from other types of IC designs. ASICs have driven an expansion of the semiconductor industry, have fundamentally altered the IC business, and have resulted in a significant increase in the number of IC designs and designers. The rapid growth of ASICs has required advances in a number of different areas of semiconductor technology including design, process, manufacturing, test, packaging, and CAD.

ASICs can be grouped into four broad categories: (1) full-custom, (2) semi-custom, (3) field-programmable logic devices (FPLDs), and (4) linear arrays.

1.5 ASIC Technology

There are several different approaches to ASIC design and implementation. These range from custom, to standard cells, to gate array implementations. Thus, a potential ASIC user has four implementation approaches available: full custom, standard cells, gate arrays and programmable logic arrays. The full custom approach yields a chip that is optimized for both silicon area and performance; with the other end of the spectrum being the programmable logic array, which has a set number of I/Os and logic equations available. A semicustom chip, such as gate arrays and standard cells, does not achieve the density of a full custom chip; in fact a 50-60% density comparison is good.

These four implementation approaches are based on three semiconductor technologies; specifically: complementary metal oxide semiconductor (CMOS) integrated circuits, bipolar integrated circuits, and gallium arsenide (GaAs) integrated circuits. The predominant technology for ASIC designs has been and will continue to be CMOS. Both bipolar and GaAs technology find particular application in the higher performance, less cost-sensitive system applications.

1.5.1 Complementary metal oxide semiconductor

When the term "ASIC' or "VLSI" is mentioned, the circuit technology referred to as CMOS, complementary metal oxide semiconductor, is the first technology mentioned. CMOS is the choice for virtually all cost-driven applications and can be both cost- and performance-effective in many applications. The lower speed of CMOS, in comparison to bipolar and GaAs, is often more than offset by its higher level of integration.

The predominant characteristic of CMOS that lends itself to high levels of functional integration is the potential for less power dissipation than required for its bipolar or GaAs counterparts. If a comparison of intrinsic gate delay is drawn between comparable-sized components, then GaAs will be the fastest, followed by bipolar technology, with CMOS being the slowest. In spite of this, short-channel CMOS devices can achieve, with minimal loads, switching delays of less than 0.5 ns. A shortcoming, however, of CMOS structure is that transconductance (ability to charge/discharge capacitance) is lower than a comparably sized bipolar device. As a result the delay per unit of capacitance is more, thus reducing the performance at the system level when compared to a bipolar implementation.

Scaling, the proportional reduction of the device or circuit parameters, will impact all three implementation technologies. CMOS, however, is the easier of the three structures in terms of determining the impact of scaling. This results from the fact that MOS structures are primarily surface devices and thus simpler than bipolar in terms of electrical modeling. CMOS circuits will dissipate more power as the operating frequency is increased. A 1-μm CMOS gate switching at 150 MHz will dissipate 3.75 mW, which is comparable to a bipolar Emitter-Coupled Logic (ECL) circuit switching at the same speed. The point, of course, is that most CMOS ASIC implementations are limited to less than 25% of their gates switching simultaneously, in which case the power dissipation is reduced significantly. All CMOS ASIC designs must be carefully evaluated for maximum power dissipation.

1.5.2 Bipolar

Bipolar integrated circuits were the predominant choice through the 1960s and into the 1970s. The use of TTL and ECL were commonplace throughout most of the industry. While CMOS has displaced the bulk of the bipolar families (DTL, TTL, I^2L, etc.) the high speed of ECL has ensured the survival of this technology.

The primary attribute of the bipolar technologies and, in particular, ECL is their high performance. In contrast to CMOS, ECL circuitry dissipates a relatively constant amount of power as the switching rate is moved from static to its maximum rate. As a result the power dissipation is typically much higher as compared to a CMOS implementation.

Since it is apparent that bipolar technology, in the form of ECL, provides the highest performance with highest power dissipation, and CMOS provides good performance with low power dissipation and the highest gate density, the merging of these two technologies in the same chip could result in a winning combination. This, of course, has happened, with the combination referred to as BiCMOS (bipolar complementary metal oxide semiconductor).

BiCMOS ASICs have had considerable attention but slower than expected introduction and acceptance rate. BiCMOS arrays in excess of 20,000 gates are being introduced. This is a technology of the future, which may substantially impact the growth of both the ECL and GaAs ASIC marketplace; it can be expected that these two technologies will be limited to applications that require only the highest speed performance implementation. The combination of CMOS process technology, multilayers of interconnect (up to four), and an excellent speed-times-power product at the chip level makes BiCMOS a logical choice for future system implementation. For analog circuits, however, bipolar technology is often more suitable due to the superior performance of bipolar transistors in terms of input noise, offset, voltage gain, output drive, and maximum frequency in comparison to the MOSFET.

Bipolar ASIC technology was chosen in this VFC circuit design because it was available at the Alberta Microelectronic Centre, and bipolar version VFCs are often preferred in high performance design [7].

1.5.3 Gallium arsenide

Gallium arsenide is an evolving technology that is just beginning to be accepted as an ASIC implementation technology. Unfortunately, while these ASICs offer very short intrinsic delays, the impact of interconnect cause the total path delay to increase significantly. As a result, GaAs chips are providing comparable speeds to an ECL implementation with reduced power and lower integration levels. While the mobility of electrons in GaAs is significantly higher than in silicon, the hole mobility is actually less than in silicon. This effectively precludes a complementary GaAs structure, thus limiting the technology based on its power dissipation characteristics.

1.6 Thesis Content

This thesis mainly investigates voltage to frequency converters based on grounded capacitor type multivibrators. Yet, both types (floating and grounded timing capacitor) multivibrators are reviewed, and the advantages and disadvantages of these multivibrators are also discussed. The first multivibrator with grounded timing capacitor is considered (Kukielka multivibrator), which uses separate threshold and current steering circuits, but very complicated circuitry is required just to compensate the temperature dependency of the threshold voltage. Based on using a nonhysteresis comparator, an alternative topology is presented which does not require such complicated circuitry. The new topology has more flexibilities for different design purposes. Finally a precision voltage to frequency converter is proposed and discussed with simulations.

The applications of voltage to frequency converters were introduced here in Chapter 1. High temperature voltage to frequency converters, especially over 200°C, have wide applications in industry. The VFC performance parameters which are commonly encountered in most data encoding applications were also given in this chapter, and ASIC technologies of bipolar, CMOS, BiCMOS and GaAs designs were reviewed.

Two common types of VFCs, multivibrator and charge-balance VFCs, are reviewed and two most popular multivibrators, floating timing capacitor and grounded capacitor multivibrators are investigated and discussed in Chapter 2. The grounded capacitor type multivibrator has a better structure for high temperature VFC design.

Chapter 3 introduces the improved topology for the grounded capacitor multivibrators. Each circuit building block is discussed separately. The chapter starts from a simple multivibrator and discusses possible circuit modifications. The underling idea of the discussion is that a multivibrator performance can be improved by redesigning each building block to meet nigher specifications. The modified multivibrator design confirms this point. Finally a precision voltage to frequency converter is proposed with a clear and easily understood circuit structure, good linearity and temperature stability.

High temperature integrated circuit design is very different from circuits designed for the industrial range of temperatures. Leakage currents are the major problem in high temperature IC design, the temperature compensation techniques are the core of high-temperature stable VFC design. The two most popular bipolar processes, junction-isolated bipolar transistors and dielectrically isolated vertical bipolar transistors, are introduced in Chapter 4. Theses methods can be applied to the high temperature VFC circuit design.

In Chapter 5, analog ASIC design and simulation are introduced. It discusses specifics of the design due to the limitations of the technology. SPICE and breadboarding simulations are very important for most analog IC design.

Finally in Chapter 6, the important circuit measurements are given, and results are summarized. The conclusion is presented in Chapter 7.

2 AN OVERVIEW OF VOLTAGE TO FREQUENCY CONVERTERS

2.1 Two Common Types of VFCs

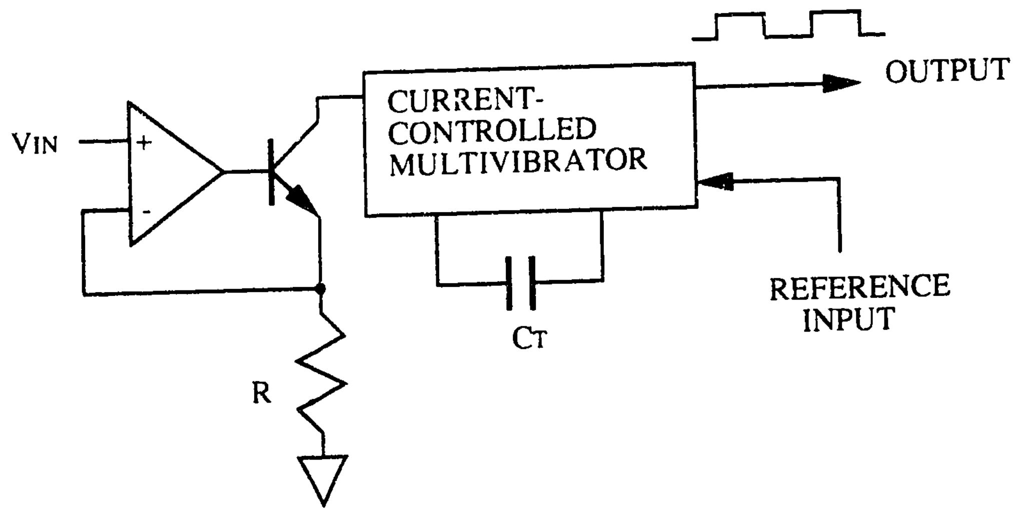
There are a number of advantages to using a VFC in an analog to digital conversion scheme. First, unlike converters based on binary-weighted networks, monotonicity is inherent under all supply and temperature conditions. Second, the fact that the signal is converted to an easily-transmitted serial bit stream allows the analog circuitry (the VFC and analog signal conditioning circuits) to be located elsewhere.

There are two common types of VFCs: multivibrator- and charge-balance VFCs [11,5].

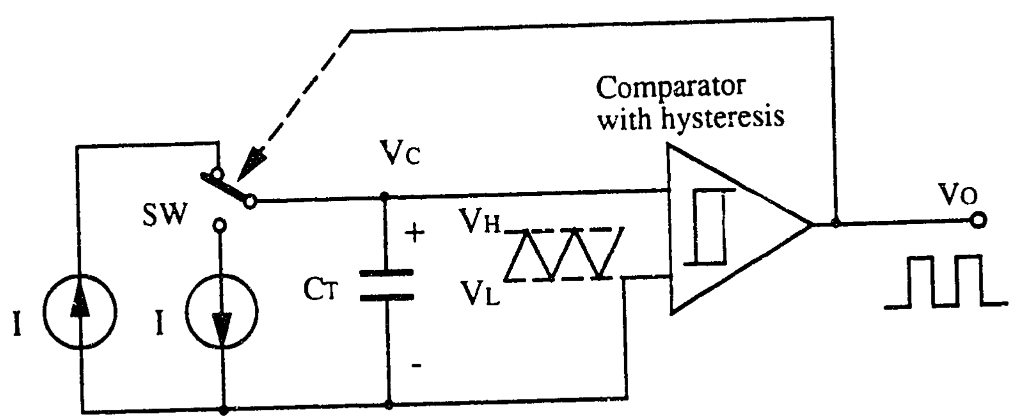
In the *multivibrator* type as shown in Figure 2.1a, the input voltage is converted to [illegible] which charges and discharges a capacitor. The switching thresholds are set by a stable reference, and the output, which has unity mark to space ratio, is a rectangular signal with frequency proportional to the input. Figure 2.1b illustrates a current controlled multivibrator. The timing capacitor is charged/discharged by a constant current which results in a linear waveform (triangular) for the voltage across the capacitor. The output frequency is determined by the current I and the threshold voltage $V_H - V_L$.

The *charge-balance* VFC includes an integrator, a comparator and a precision charge source as shown in Figure 2.2. The input is applied to the integrator, which charges. When the integrator output reaches the comparator threshold, the charge source is triggered and a fixed charge is removed from the integrator. The rate at which charge is removed must balance the rate at which it is being supplied, so the frequency at which the charge source is triggered will be proportional to the input to the integrator.

The multivibrator type VFC is simple and cheap, demands little power, and has unity mark to space (M-S) output which is very convenient with some transmission media. But it is less accurate than the charge-balance type VFC and cannot response to negative



a) Multivibrator architecture



b) Current controlled multivibrator

Figure 2.1 Multivibrator type VFC

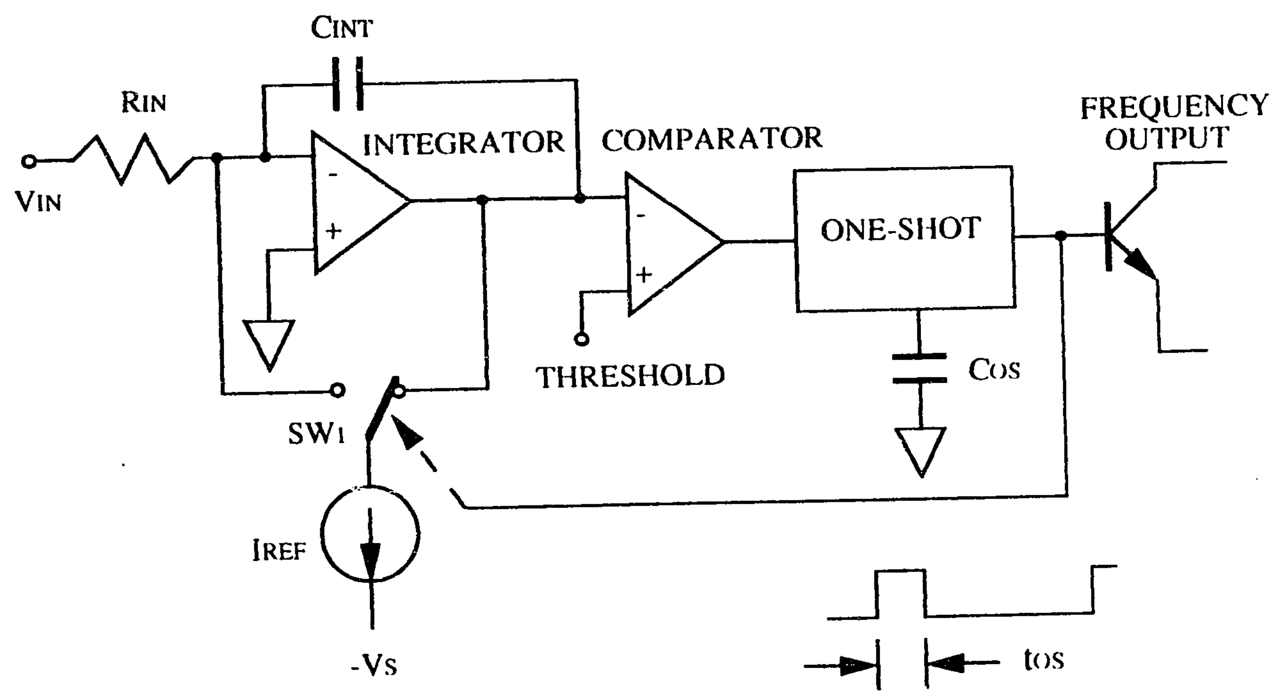


Figure 2.2 Charge-balance VFC architecture

input transients.

The charge-balance type is more accurate, and negative input transients are integrated to contribute to the output. It has more demanding supply requirements and a lower input impedance, and its output is a pulse train, not a unity M-S square wave.

2.2 Multivibrators

The most important portion of a multivibrator is the threshold control circuit. This circuitry senses when the voltage across the capacitor has reached a threshold point and then causes the capacitor charging current to reverse. The performance parameters of the multivibrator such as the linearity, range, and stability of operation are directly dependent upon the performance of the threshold control circuitry.

As shown in Figure 2.1 the hysteresis comparator (or a nónhysteresis comparator together with a threshold circuit) works as a threshold control circuit which is bistable in form. Assume that, initially, the capacitor is discharged and the output of the comparator is low. The current source is connected to the capacitor and charges it linearly with a constant current towards the upper threshold. Once the threshold point is reached the comparator undergoes regenerative switching and the output goes high. The current sink is now connected to the capacitor and it discharges linearly towards the lower threshold, at which point the comparator undergoes regenerative switching forcing the output low. The charge/discharge cycle repeats and the circuit enters astable operation. The time required for the capacitor to charge between the two thresholds is given by

$$\frac{T}{2} = \frac{\left(V_H - V_L\right) C_T}{I} = \frac{V_{TH} C_T}{I} \tag{2.1}$$

where V_H = upper threshold

V_L = lower threshold

$V_{TH} = V_H - V_L$ = hysteresis voltage

I = charge/discharge current

C_T = timing capacitor

T = period of oscillation

Linear control of the frequency can be achieved by the variation of the charge/discharge current I. The frequency can also controlled by voltage variation through a voltage-to-current converter, $I = V_{in} / R_T$ (where V_{in} is input voltage and R_T is external timing resistor). The overall frequency of oscillation is given by

$$f_o = \frac{1}{T} = \frac{I}{2\,C_T\,V_{TH}} = \frac{V_{in}}{2\,C_T\,R_T\,V_{TH}} \tag{2.2}$$

Topologically, there are two major types of relaxation multivibrators. These use either floating or grounded timing capacitors and are now discussed in detail.

2.2.1 Floating capacitor multivibrator

This type of multivibrator is most commonly implemented as the emitter-coupled multivibrator [5,12,7], where transistors Q_1-Q_4 form the positive feedback gain stage (Figure 2.3). Its operation can be briefly explained as follows.

At any given time, either Q_1 and D_1 or Q_2 and D_2 are conducting , such that the capacitor C_T is alternately charged and discharged by the voltage controlled current sources I_1 and I_2. Normally I_1 and I_2 are chosen to be equal, say I. The circuit provides a symmetric square wave output across D_1 and D_2, with a peak-to-peak amplitude of $2V_{BE}$, where V_{BE} is the transistor base-emitter voltage drop. The output V_{E1} is constant when Q_1 is on, and becomes a linear ramp with a slope equal to (I/C_T) when Q_1 is off. The output

... Both of these waveforms have peak-to-peak amplitudes of $2V_{BE}$. The frequency of oscillation f_0 can be expressed as

$$f_o = \frac{I}{4\,V_{BE}\,C_T} \tag{2.3}$$

The ramp output voltages V_{E1} and V_{E2} can be subtracted from each other to give a linear triangular waveform. This can be done by using a simple differential amplifier stage.

Transistors Q_3 and Q_4 prevent Q_1 and Q_2 from saturating. The circuit is simple, composed of *npn* transistors, is nonsaturating, and hence offers high-frequency capability. However, the temperature coefficient of the output frequency depends on the V_{BE} of the transistors. The temperature coefficient of the base emitter voltage is approximately -2 mV/°C which causes the frequency to have a temperature coefficient of approximately

$$TC = \frac{1}{f_o}\frac{\partial f_0}{\partial T} = -\frac{1}{V_{BE}}\frac{\partial V_{BE}}{\partial T} = \frac{1}{0.65\ V}(-2\ \text{mV/°C}) \approx 3300\ \text{ppm/°C} \tag{2.4}$$

Various methods of stabilizing the TC of frequency have been taken to reduce this large temperature coefficient. Some circuits [13] [14], for example by Cordell, yield TC values as low as 20 ppm/°C below 100kHz. However, as the frequency of oscillation increases, the temperature coefficient deteriorates rapidly due to the effect of parasitic capacitance at the emitters of Q_1 and Q_2, which undergo large common-mode voltage swings as shown in Figure 2.3.

The emitter coupled multivibrator's all-*npn* construction, nonsaturated operation, and small signal swings combine to produce a VFC capable of high frequency operation with good linearity over a wide range. But the emitter-coupled multivibrator presents parasitic capacitances at both ends of the floating capacitor, introducing a voltage divider effect at high frequencies and thus limiting performance. Temperature compensation

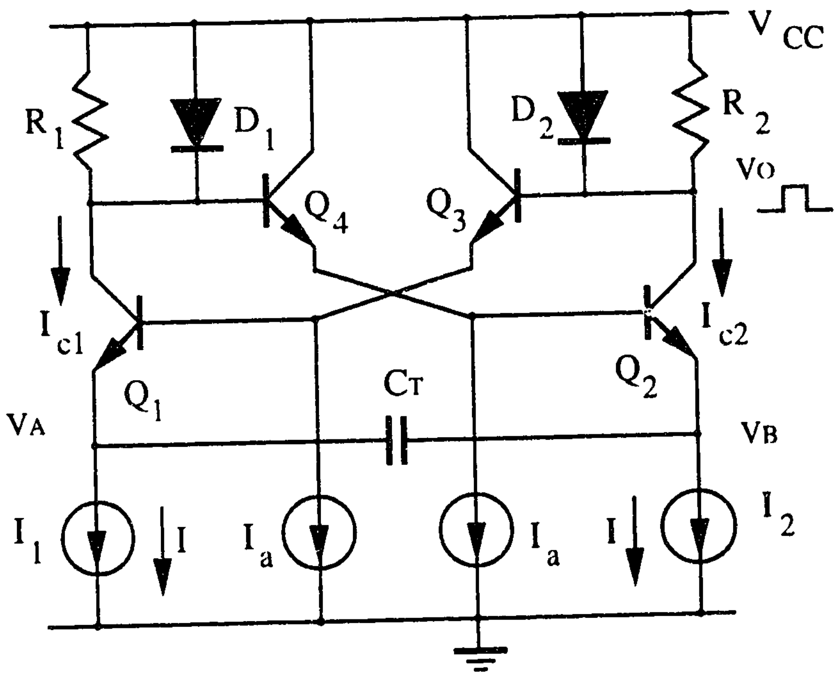


Figure 2.3 Emitter-coupled multivibrator

circuitry is required, though, to improve the inherently poor temperature stability of the basic emitter-couple multivibrator. For high temperature environment, emitter-coupled multivibrators are aimost impossible to use because V_{BE} changes dramatically with different currents and temperatures. The circuits suffer from very poor linearity and temperature-stability.

2.2.2 Grounded capacitor multivibrator

This type of relaxation multivibrator [15,7,8], which is shown in Figure 2.4, has not received as much attention as the emitter-coupled multivibrator. The timing capacitor C_T is grounded at one end, making any parasitic capacitances at the other end appear in parallel. C_T is alternately charged and discharged by either of the current sources. The comparator senses the voltage level V_C across C_T and controls the switching to initiate the charge and discharge cycles. The currents of the two sources, charging and discharging the timing capacitor, form an integrator that produces a triangular wave. A square wave is available at the output of the comparator.

The frequency of the oscillation can be expressed as

$$f_0 = \frac{I}{2\,C_T\,(V_H - V_L)} \tag{2.5}$$

where V_H and V_L are the higher and lower threshold voltages which are also the switching points of the comparator, and I is the current charging/discharging the capacitor.

Computer simulations showed the grounded capacitor VFC to be inherently superior for high-frequency temperature stable design, and this topology was chosen for IC realization. The widespread belief that the emitter-coupled multivibrator is superior for high-frequency operation probably dates back to discrete-component circuits where loop delays in the grounded-capacitor circuit were a severe limitation. However, both computer

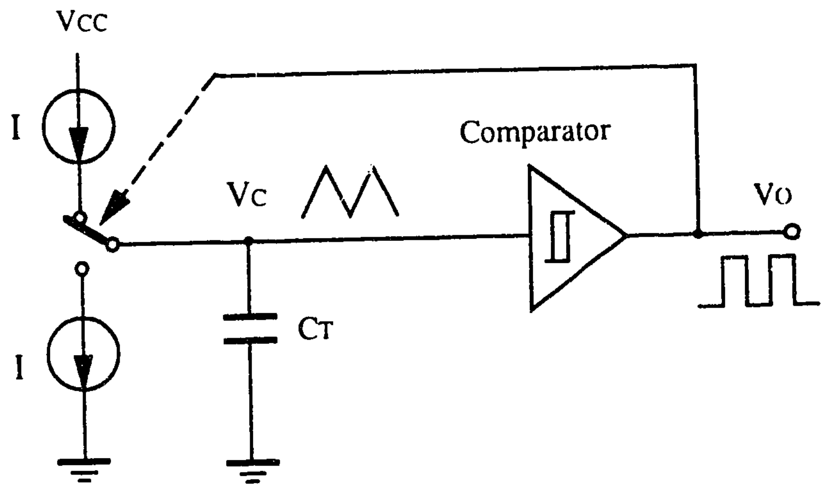


Figure 2.4 Grounded-capacitor multivibrator top!ogy

simulation and circuit measurements show that with careful design of the comparator and current switches using monolithic technology, the high-frequency temperature stability of the grounded-capacitor circuit is superior to that of the emitter coupled circuit.

2.3 Improved Grounded Capacitor Multivibrator

2.3.1 Kukielka multivibrator

The circuit uses a grounded external timing capacitor C_T with charging and discharging via current sources controlled by fast switches. A fast Schmitt trigger senses the voltage on the timing capacitor and operates the current switch. The input voltage passes through a V-I converter and varies the frequency by varying the current sources. The multiplier and the V_T generator are part of the temperature compensation scheme, and their function will become clearer when the scheme is detailed later in this section.

The circuit operation can be seen from the simplified schematic of Figure 2.5. In order to achieve maximum operating speed, the Schmitt trigger is as simple as possible: Q_1 and Q_2 form a differential pair, and the emitter follower Q_3 is connected to give unity gain positive feedback. The current switch is composed of Q_4 and Q_5, whose bases are connected to the output of the Schmitt trigger that alternately turns them on and off. Devices Q_6 and Q_7 are level shifters, and D_1, D_2, and D_3 are diode connected transistors to avoid saturation of Q_1 and Q_2 at high temperatures. When Q_5 is on and Q_4 is off, the external timing capacitor C_T is charged with a current I. When the voltage across C_T reaches the switching point of the Schmitt trigger, Q_1 and Q_2 change state, driving Q_4 on and Q_5 off, and C_T is discharged with an effective current I. The frequency of oscillation is given by

$$f_o = \frac{I}{2\, C_T\, \Delta V_C} \qquad (2.6)$$

where ΔV_C is the voltage swing across the capacitor C_T. ΔV_C is obtained by subtracting

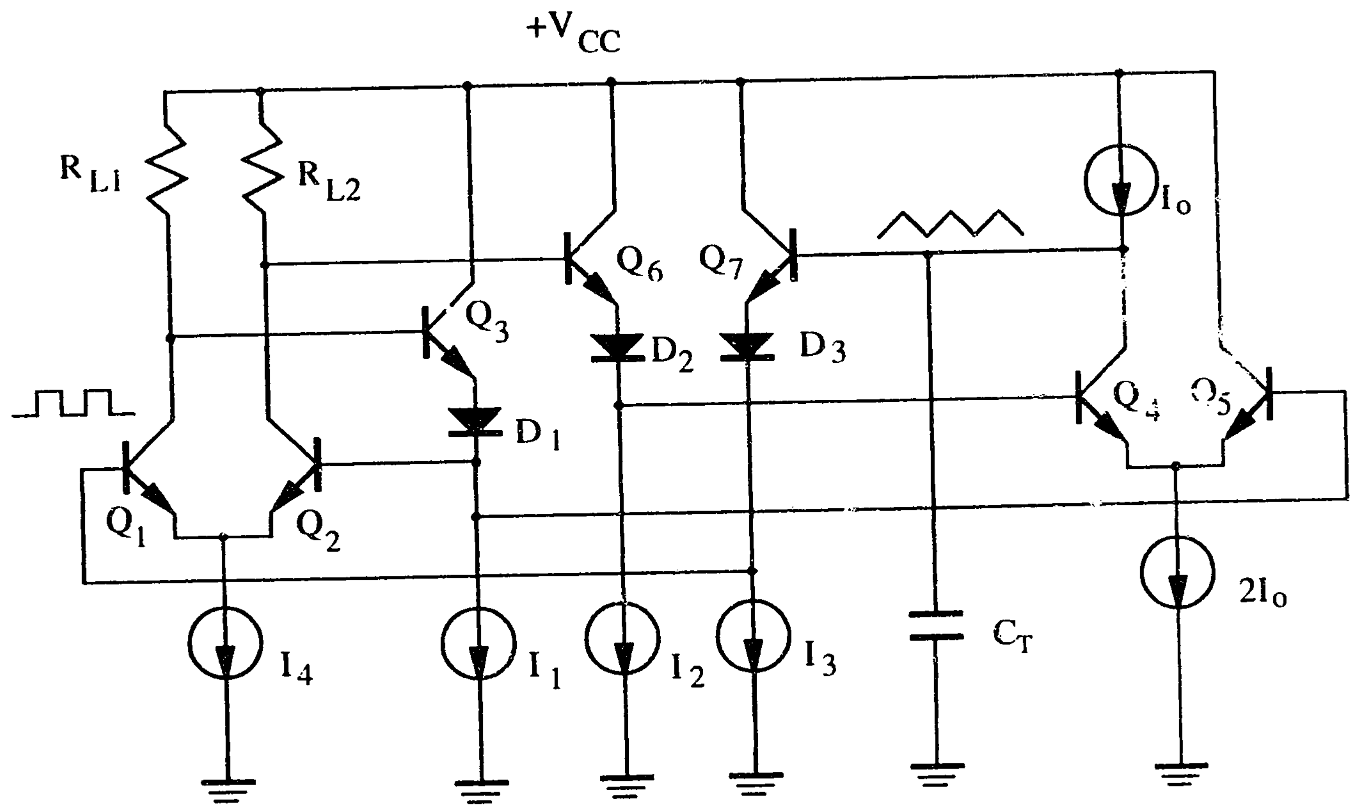


Figure 2.5 Kukielka multivibrator

from the total collector voltage swing (I_4R_{L1}) an amount equal to twice the Schmitt trigger hysteresis (since there are two switching points, an upper one and a lower one) plus an extra voltage drop due to the small current flowing in the transistor that is turning on at the switching instant. ΔV_C can be expressed as

$$\Delta V_C = I_4 R_{L1} - 2I'_C R_{L1} - 2\delta V \tag{2.7}$$

where δV is the hysteresis (or voltage difference) between the input and output of the comparator and $I'_C R_{L1}$ is the voltage drop due to the current through the transistor which is turning on at the moment of switching.

Since the Schmitt trigger has unity gain positive feedback, δV is obtained by equating the open loop gain A_{0L} of the comparator to 1 and solving for δV.

Neglecting base current and ohmic resistance in the transistors and assuming perfectly matched devices, the open loop gain is given by

$$A_{0L} = g_{mTOT} R_{L1} \tag{2.8}$$

where

$$g_{mTOT} = \left(\frac{1}{g_{mQ1}} + \frac{1}{g_{mQ2}}\right)^{-1} = \frac{g_{mQ1} g_{mQ2}}{g_{mQ1} + g_{mQ2}} \tag{2.9}$$

and

$$g_m = \frac{I_C}{V_T}, \quad V_T = \frac{kT}{q}. \tag{2.10}$$

Also,

$$I_{CQ1} = \frac{I_4}{1 + \exp\left(-\frac{\delta V}{V_T}\right)}, \quad I_{CQ2} = \frac{I_4}{1 + \exp\left(\frac{\delta V}{V_T}\right)}. \tag{2.11}$$

From (2.9), (2.10), and (2.11), (2.8) becomes

$$A_{0L} = \frac{I_4 R_{L1}}{2V_T\left(1 + \cosh \frac{\delta V}{V_T}\right)} \tag{2.12}$$

Equating A_{0L} to unity, solving for δV and using the relation

$$\cosh^{-1} = \ln\left(x + \sqrt{x^2 - 1}\right), \tag{2.13}$$

we have

$$\delta V = V_T \ln\left[\left(\frac{I_4 R_{L1}}{2V_T}\right) - 1 + \sqrt{\left(\frac{I_4 R_{L1}}{2V_T} - 1\right)^2 - 1}\right]. \tag{2.14}$$

If I_4 = 2mA, R_{L1} = 350 Ω then δV=83 mV at room temperature. The square wave amplitude will be $I_4 R_{L1}$ = 0.7 V and the triangle wave amplitude ΔV_C = 479 mV.

Using (2.14), (2.11), and (2.7), the frequency of oscillation given in (2.6) becomes

$$f_0 = \frac{I_0}{2C_T\left\{I_4 R_{L1} - \dfrac{2I_4 R_{L1}}{\dfrac{I_4 R_{L1}}{2V_T} + \sqrt{\left(\dfrac{I_4 R_{L1}}{2V_T} - 1\right)^2 - 1}} - 2V_T \ln\left[\left(\dfrac{I_4 R_{L1}}{2V_T} - 1\right) + \sqrt{\left(\dfrac{I_4 R_{L1}}{2V_T} - 1\right)^2 - 1}\right]\right\}} \tag{2.15}$$

(assuming $R_{L1} = R_{L2}$). From this result, it can be seen that temperature compensation can be achieved by making

$$I_4 R_{L1} = k_1 V_T \tag{2.16}$$

and

$$I_0 = k_3 V_T \tag{2.17}$$

where k_1 and k_3 are constants, then

$$f_0 = \frac{k_3}{2\, C_T\, k_4} \tag{2.18}$$

with

$$k_4 = k_1 - \frac{2k_1}{\frac{k_1}{2} + \sqrt{\left[\frac{k_1}{2} - 1\right]^2 - 1}} - 2\ln\left\{\frac{k_1}{2} - 1 + \sqrt{\left[\frac{k_1}{2} - 1\right]^2 - 1} \quad -1\right\} \tag{2.19}$$

which is to the first order independent of frequency.

In Kukielka multivibrator design, the Schmitt trigger switching exhibits a strong temperature dependence through V_T, which is compensated by very complicated circuitry[7], but not over a wide range of temperatures. The multivibrator only works well around room temperature from 0 to 75°C and can achieve a temperature coefficient of less than 60 ppm/°C at frequencies up to 20 MHz and a nonlinearity of less than 3%. Since the thresholds and input currents are dependent on temperature it is difficult to calculate the actual output frequency.

2.3.2 Multivibrator with temperature-stable thresholds

To avoid using a temperature-dependent Schmitt trigger, we suggest a new multivibrator, using separate comparator and threshold circuits. The thresholds are independent of temperature. The simplified schematic is shown in Figure 2.6. The difference in this multivibrator from the Kukielka multivibrator is that it uses a nonhysteresis, non-saturating, high speed comparator: Q_6 and Q_7 form a differential pair, it senses the voltage on the timing capacitor C_T and alternate turns Q_3 and Q_8 on and off through the current mirror; The threshold circuit is composed of Q_4, Q_5, R_{TH} and E_2, whose output $R_{TH}I_{TH}$ is temperature independent as long as I_{TH} is temperature stable. When Q_1 is on and Q_2 is off, the external timing capacitor C_T is charged with a current I_{IN}. When the voltage across C_T reaches the threshold circuit output, Q_6 and Q_7 change state, Q_6 turns on and Q_7 turns off, Q_3 is driven on by the bottom current source and Q_8 turns off, which causes Q_1 and Q_2 to

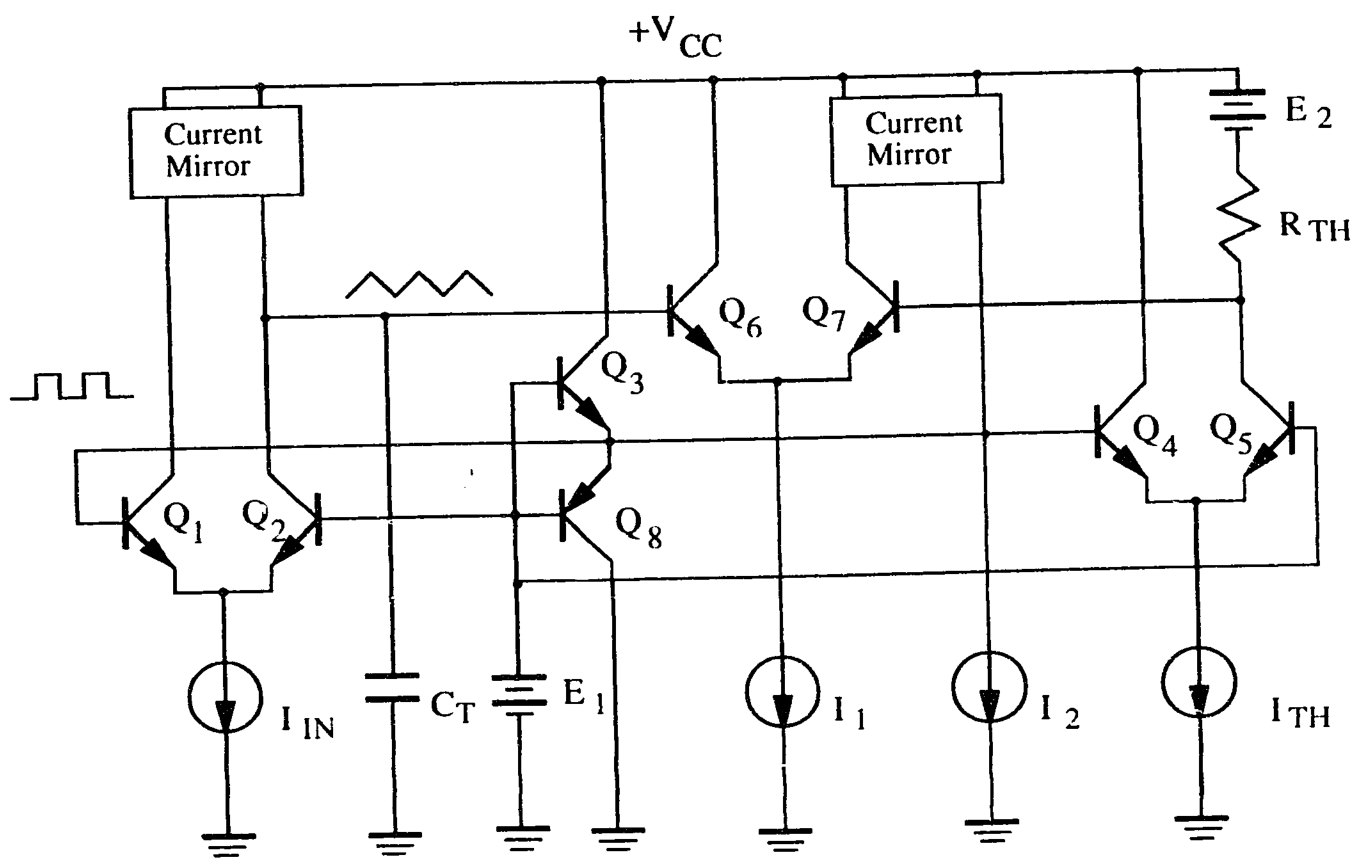


Figure 2.6 Temperature stable multivibrator

change state, and C_T is discharged with current I_{IN}. The output frequency of the multivibrator is

$$f = \frac{I_{IN}}{2\, C_T\, R_{TH}\, I_{TH}} \tag{2.20}$$

From (2.20) we know, as long as the threshold voltage $R_{TH}I_{TH}$ is temperature stable, the frequency of the oscillation is independent of temperature, and can be easily calculated. $R_{TH}I_{TH}$ can be achieved by a voltage reference.

PTAT (proportional to absolute temperature) and V_T generator circuits are eliminated in the design. The circuit structure is much simpler than that of Kukielka VFC. More detailed implementation and discussion will be presented in the next chapter.

2.4 Choice of Capacitors

Apart from the usual precautions necessary with any precision analog circuitry (grounding, decoupling, current routing, isolation of noise, etc., a subject for a book, not a paragraph) the main precautions necessary when using a VFC are the choice of capacitor and separation of the input and output.

The critical capacitors in a precision VFC (the multivibrator's timing capacitors, and the monostable timing capacitor in a charge-balance type) must be stable with temperature variation. Furthermore, if they suffer from dielectric absorption, the VFC will be nonlinear and may have poor settling time.

If a capacitor is charged, discharged and then open-circuited it may recover some charge. This effect, known as dielectric absorption (DA), can reduce the precision of VFCs or sample-hold amplifiers using such capacitors. VFCs and sample-hold amplifiers (SHAs) should therefore use teflon, polypropylene, or zero-temperature-coefficient (NP0, Coupling between output and input of a VFC can also affect its linearity. To prevent problems, decoupling practices and the usual layout precautions should be observed. This is critically important with opto couplers, which require high current drive (10-30 mA).

2.5 Conclusion

The emitter coupled multivibrator is based on a floating capacitor structure and provides a simple and compact circuit capable of high frequency operation with wide range and good linearity of frequency control. Of the grounded capacitor topologies, the bipolar multivibrator developed by Kukielka has shown good performance in terms of linearity, range of frequency control, high frequency capacity and has a low temperature coefficient even at high frequencies.

The precision threshold multivibrator we proposed is much simpler comparing with Kukielka multivibrator, and it can operate over wide range of temperature with low temperature coefficient and has high linearity, it is ideal for most VFC building block design. So we can easily see that grounded capacitor multivibrators have the potential for good performance in high temperatures. The idea of separating switching, comparator and threshold circuits design will be very important for designing a temperature stable VFC. If we can design each of the functional circuit block temperature independent, then the whole circuit will be temperature independent. The new architecture provides the circuit with higher linearity, accuracy and temperature stability, which has good potential for high temperature multivibrator design. So far, a multivibrator which can work over 200°C can not yet be found in the market. Developing a high temperature multivibrator will be a very interesting goal and highly demanded in the industries. It is of interest therefore to investigate new grounded capacitor structures which higher frequency range and lower temperature coefficient.

3 GROUNDED CAPACITOR VFC DESIGN AND IMPLEMENTATION

3.1 Introduction

The main problem of the emitter coupled based multivibrator is its high temperature stability. As mentioned before, the poor high frequency TC is primarily caused by parasitic and junction capacitances (with strong temperature coefficients) that appear at both of the emitters connected to the timing capacitor. For grounded capacitor multivibrator, the timing capacitor is grounded, any parasitic capacitances appear to be in parallel and relatively smaller. The grounded capacitor multivibrator shows structural advantages of high frequency and high temperature performance.

Different from most other grounded capacitor VFCs [7,8], the converters proposed in this thesis are structurally divided into four independent subcircuits: voltage-to-current converter, capacitor charge-discharge circuit, non-hysteresis comparator and threshold circuit. The structure diagram in Figure 3.1 shows the connection between these functional building blocks. Subcircuit blocks could be very different in various designs, and will be investigated and discussed in this chapter. This makes the design more flexible and provides an abundance of circuits adapted for different design conditions. Circuits designed using this idea will be presented later.

3.2 Voltage-to-Current Converters

Since a charge-discharge circuit is usually current-controlled, a voltage-to-current converter (VCC) is needed to interface it with an input voltage. Voltage-to-current converters can achieve high performance with integrated circuit design techniques. For this reason, they constitute powerful building blocks in integrated circuits, especially in VCO's, waveform generators, and VFCs. A voltage-to-current converter has to be carefully designed in order [illegible] stability of the whole VFC circuit.

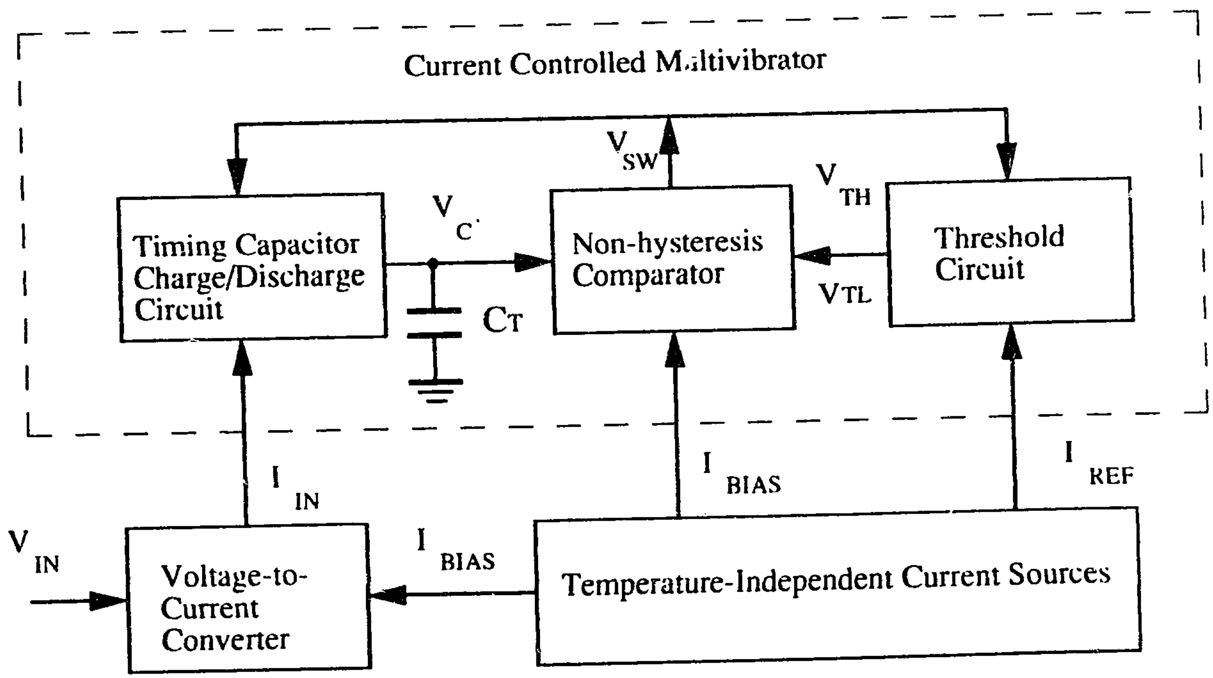


Figure 3.1 VFC architecture diagram

3.2.1 Basic voltage-to-current converter

A basic voltage to current converter consists of a simple differential amplifier with 100% feedback (Figure 3.2). Q_1 and Q_2 form a differential amplifier with an active load, Q_{101} and Q_{102}. Feedback is provided by Q_3 so that the voltage across the external current setting resistor is identical to the input voltage. The current is then picked up at the collector Q_3.

The main error source in this circuit is the base current of Q_3. However, if R_1 is set at one-half the value of the external resistor, then the base current drawn by Q_2 cancels this effect. The minimum input voltage for the circuit shown is 0.7V. If R_1 is replaced by a current source connected to a more negative voltage, then the current will operate with an input voltage down to ground level. Alternately, R_1 can be increased in value and connected to a negative supply voltage. The temperature coefficient is 10 to 100ppm/°C. The supply voltage must be 4V minimum and can be as high as the breakdown limit of the integrated circuit [8].

3.2.2 High accuracy voltage-to-current converter

As shown in Figure 3.3, Q_1, Q_2, Q_{101} and Q_{102} form a differential amplifier, V_{B1} and V_{B2} are the input, V_{B4} is the output. The output feeds back to the V_{B2} through Q_4 and Q_3 to ensure that $V_{B2} = V_{B1}$. If the voltage drop across the external current setting resistor is less than the input voltage, Q_2 and Q_{102} will draw more current than Q_1 and Q_{101}, turning on Q_4 harder, which increases the current through Q_3 and through the external resistor, thus increasing its voltage drop.

This feedback circuit requires very little input current (a maximum of 0.015% of input current): thus its error is very small and the temperature coefficient is less than 10ppm/°C. Q_5 provides a start-up current; thus the input voltage must be 1.5V minimum initially [8]. Compensation for the feedback loop is provided by C_c. The circuit is good

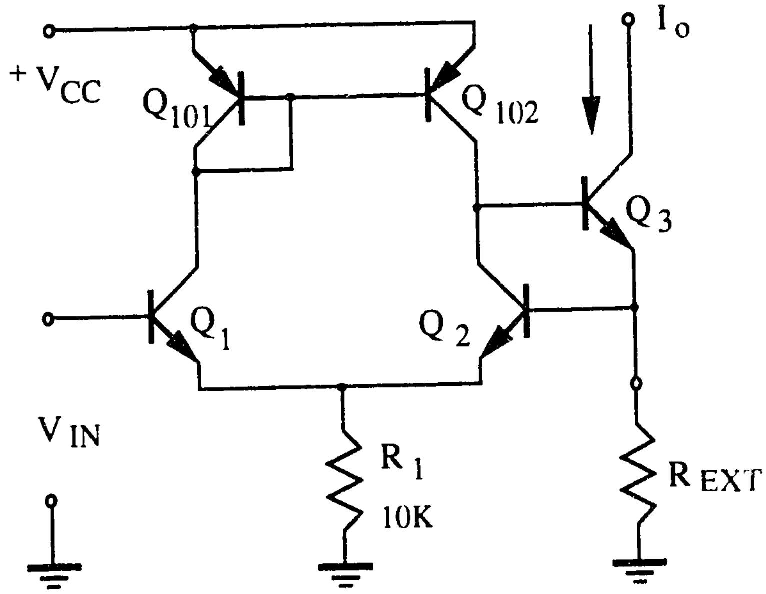


Figure 3.2 Simple voltage to current converter

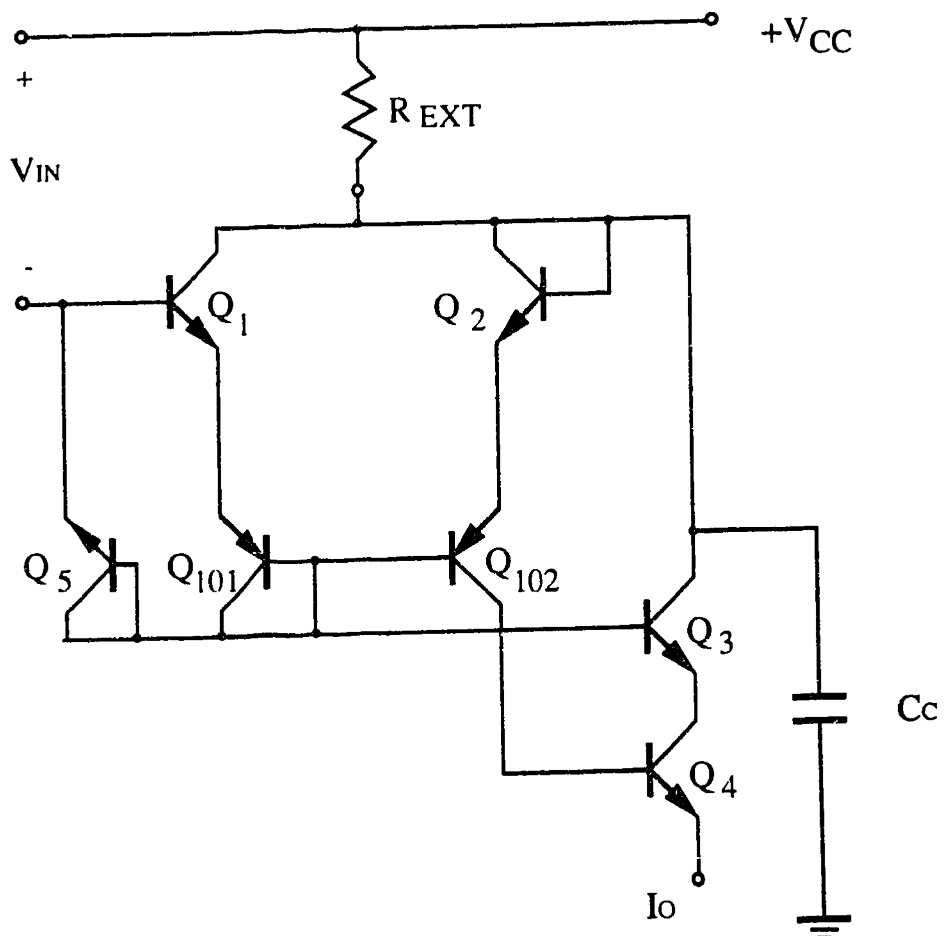


Figure 3.3 High accuracy voltage to current converter

for commercial temperature range, but not for high temperature environment. Q_{101} is connected as a diode, V_{BE101} will be lot higher than V_{BE102}, and the currents of Q_1, Q_2, Q_{101} and Q_{102} are very small which are comparable to leakage currents at high temperatures. The linearity and temperature coefficient will degrade dramatically because of that.

3.2.3 Voltage to current converter used in VFC circuits

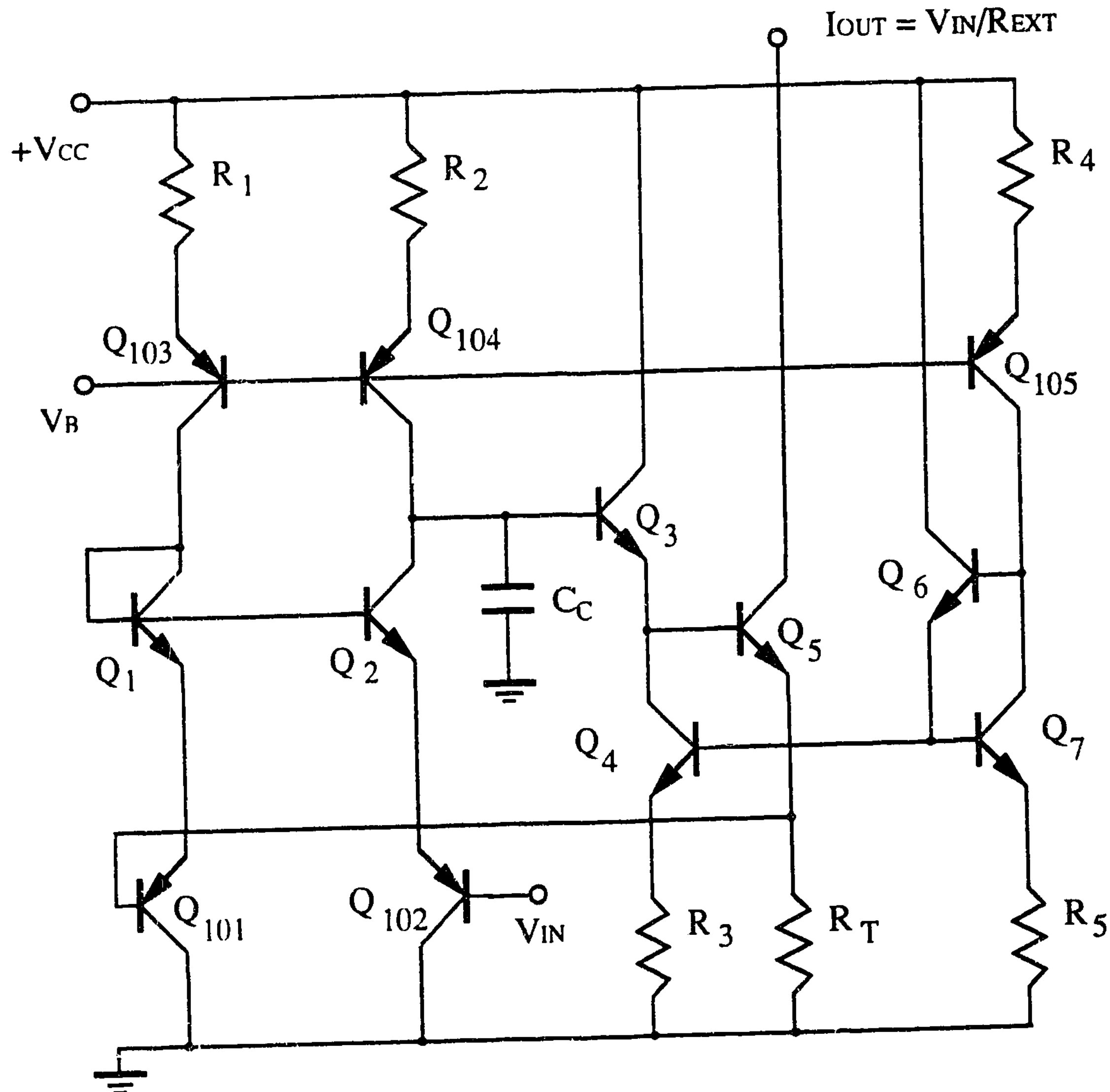
The voltage-controlled input current can be easily obtained by a simple op amp with negative feedback around an external resistor as shown in Figure 3.4. The collector current of transistor Q_5 can be shown to be

$$I_{C5} = \frac{V_{IN}}{R_T} \tag{3.1}$$

The practical implementation of the op amp circuit shown in Figure 3.4 is a simplification of a circuit presented in [13] in which a detailed description is given.

The input devices Q_{101} and Q_{102} are vertical *pnp* transistors that allow the input voltage to be taken close to ground potential. The beta of these transistors is only slightly temperature dependent (typically -0.15 percent/°C) [13].

Q_1-Q_2 and Q_{101}-Q_{102} are arranged in a thermally-symmetric quad to minimize the effect of temperature gradients. All of the voltage gain is provided by Q_2 with Q_{104} load. To maintain a low temperature drift after nulling, the ratio of the bias currents for Q_1 and Q_2 must be temperature independent and the bias for Q_3 must be equal to the sum of these, and Q_4 has twice the area of Q_1 and Q_2 to preserve base-current cancellation. R_T is the external resistor that programs the gain of the V-I converter. High-frequency compensation is provided by C_c.



Figurer 3.4 Low temperature coefficient voltage-to-current converter

3.3 Timing Capacitor Charge and Discharge Circuits

Capacitor charge-discharge circuits control the charge and discharge of the timing capacitor so that it is alternately charged and discharged by a current to reach certain threshold voltages. The cycle of the operations is inversely proportional to the current. Generally speaking, there are three different types of charging and discharging circuits [5].

In the first type of these circuits (Figure 3.5 a), the timing capacitor is charged by the current source I^+ from the top. When the voltage v_c attains the value of V_H, the comparator opens the switch SW^+ and turns off the current source I^+, closes the switch SW^-, turns on the complementary current source I^-. Now the timing capacitor is discharged and when v_c attains the value of V_L, the comparator turns off the current source I^- and the switching operations are repeated in the inverse order.

In the second type (Figure 3.5 b) the current source I^+ permanently charges the timing capacitor from the top and the comparator redirects the current source $2I^-$. During the timing capacitor discharge both current sources are connected to the timing capacitor and it is discharged by the difference of two currents.

Finally, in the third type (Figure 3.5 c) has only one current source, which is redirected by the comparator output, operating the two complementary switches. When the switch SW^+ is on, the current is directed into current mirror and charges the timing capacitor from the top; when the switch SW^- is on, the current source is directly connected to the capacitor and discharges it.

The oscillation frequency is

$$f_0 = \frac{I}{2C\left(V_{cH} - V_{cL}\right)} \tag{3.2}$$

for all three types of circuits.

In the circuits of the first type, the switching and trigger subcircuits are operating in

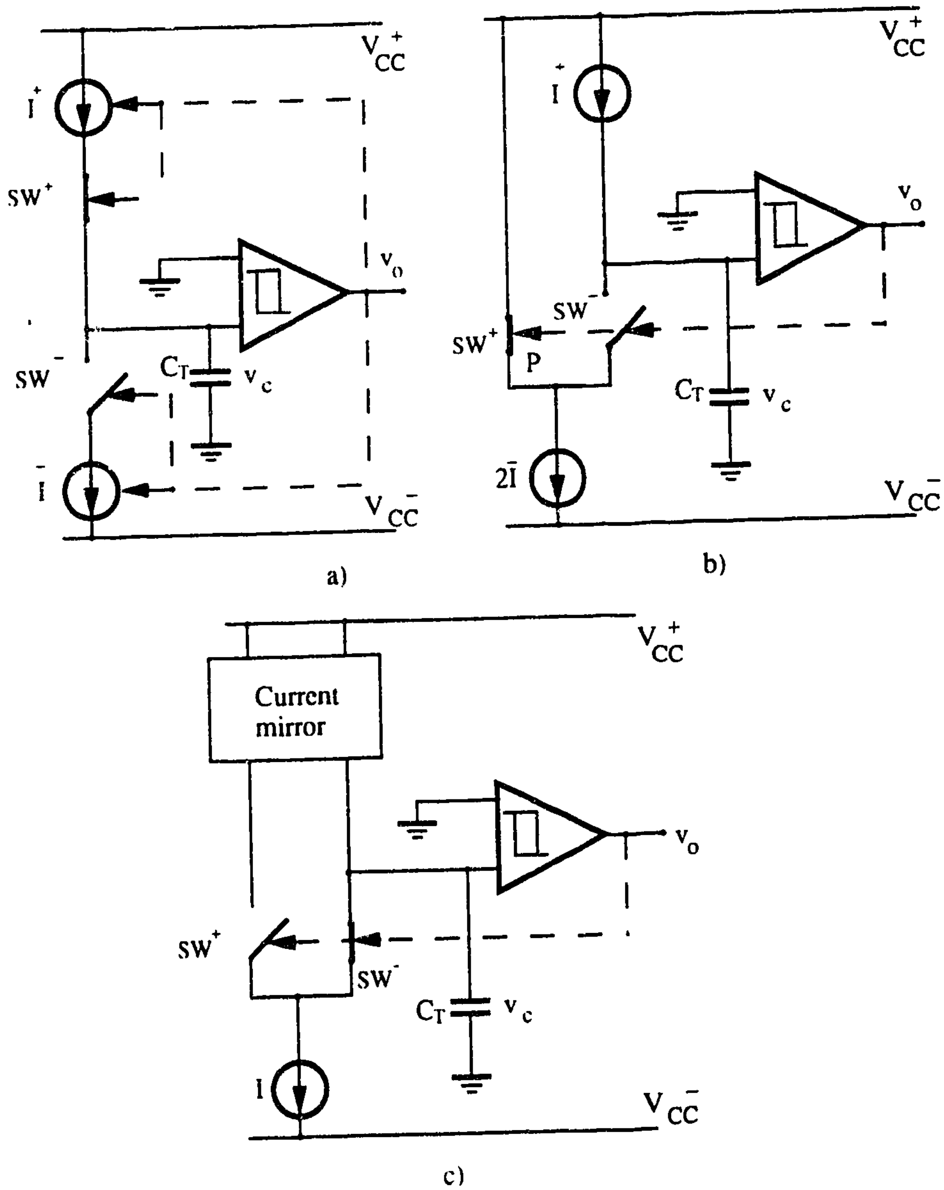


Figure 3.5 Timing capacitor charge/discharge circuits: (a) complementary current sources; (b) I and 2I sources; (c) I and a current mirror.

series. These circuits are suitable for applications in sensors measuring slowly changing variables (temperature, static fields) [16,17]. The trigger can be realized using a comparator and two-resistor positive feedback. The relative frequency error for these converters can be estimated

$$\frac{\delta f}{f_0} \approx -2 f_0 T_S \tag{3.3}$$

where T_S is the combined delay introduced by the comparator and the switch.

In the second and third types the switching and trigger subcircuits are driven in parallel. This results in faster circuits capable to operate at higher frequencies [7,8]. In addition, these circuit structure makes the design more flexible and provides abundance of circuits adapted for different design conditions. The charge-discharge circuit includes two complementary switches which only redirect the current (2I or I). Nearly all designs are using a differential pair, which is able to provide fast switching of its tail current. The comparator subcircuit can be realized using an operational amplifier in this case as well. The fast converters rely on more simple structures of the comparator circuit block also based on switching a differential pair. The whole circuit becomes a nonsaturated multivibrator. The circuits corresponding to the second group allow the widest range of the control current because they can be realized (in bipolar technology) using *npn* transistors only. The circuits of the third group are slower (the bipolar *pnp* integrated transistors have inferior frequency properties), but their bipolar design can be topologically transferred into CMOS technology (the additional limitations are minor).

3.4 Comparator Circuits

Comparators are very similar to op amps except they have no compensation capacitor and a specialized output stage. Comparator circuits are designed to provide a digital output that indicates the relative amplitudes of its inputs. A comparator is basically a high-gain, open-loop amplifier that can amplify a very small voltage difference between its inputs enough to drive its output to its high or low limit. Common-mode range is important in comparators and must include the range of voltages to be compared.

Comparators can have significant problems with signals that are very close together. Noise on the signals or within the comparator's input stage may cause the comparator to oscillate between states under these conditions. This situation usually occurs when the signal is changing slowly through the transition region. The latter case occurs when the comparator is sensing a slowly charging capacitor. One method to overcome this problem is the use of hysteresis. Hysteresis constitutes positive feedback that reinforces the comparator's decision to switch. The circuit can be realized by connecting a non-hysteresis comparator with a threshold circuit which provides the hysteresis threshold voltages. A comparator with precise adjustable hysteresis could be a good building block of a VFC.

3.4.1 Basic comparator

Figure 3.6 illustrates one of the most simple comparators which can be realized as an integrated circuit. Q_1 and Q_2 act as a differential pair. Q_{101} senses the output of the amplifier through R_1 to force output HIGH or LOW. When the base of Q_1 is at a higher potential than Q_2, all the current provided by R_2 is diverted through Q_1, turning on Q_{101}, forcing output to HIGH; When the base of Q_1 is at lower potential than Q_2, all the current is diverted to Q_2, no current flow through R_1, Q_{101} is off, output voltage goes LOW. Propagation delay of the circuit is about 120 nsec.

3.4.2 Nonsaturated comparator

The circuit presented in Figure 3.7 is a very simple but nonsaturated bipolar comparator [43]. The output stage includes two transistors Q_5 and Q_6 which clamp the swing at the

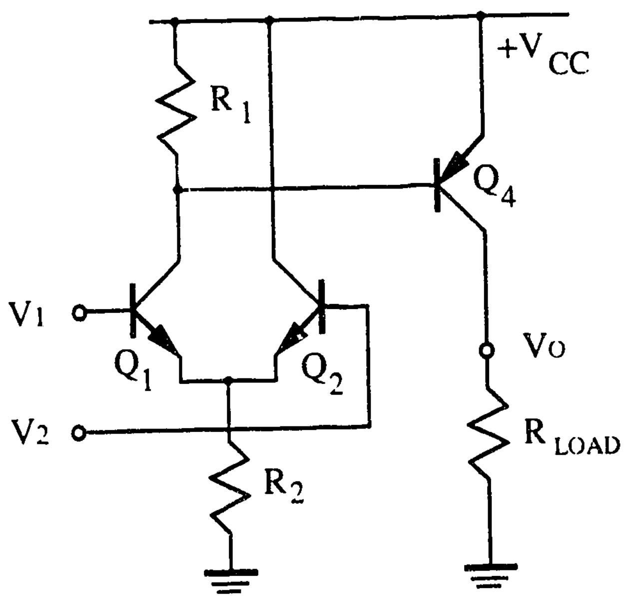


Figure 3.6 A basic comparator

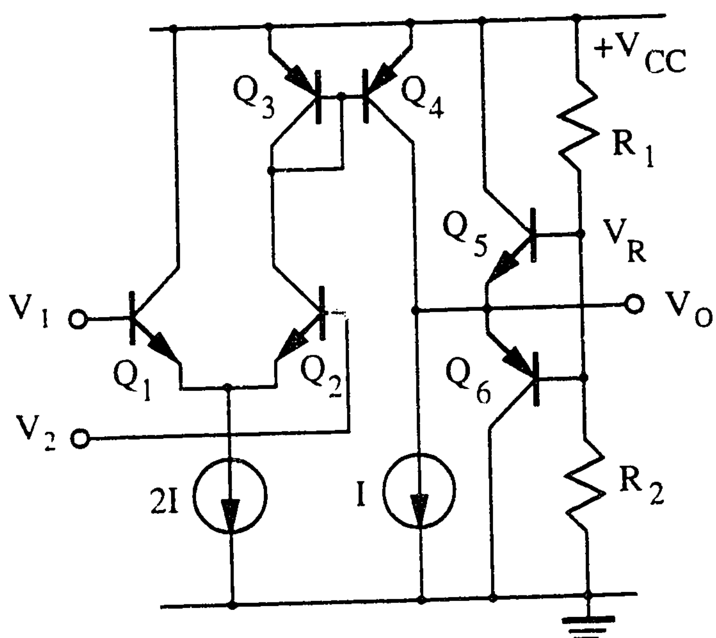


Figure 3.7 Nonsaturated comparator

output to ± 1 V_{BE}, preventing any transistors from saturating. The main difference from the Schmitt trigger used by Kukielka multivibrator [7] is that this comparator has zero hysteresis, the switching point of this comparator is exactly at the moment when inputs are equal. Q_1 and Q_2 are the input differential pair. Q_3 and Q_4 are connected as a current mirror. When $V_2 > V_1$, most the current from current source 2I will be diverted through Q_2 into Q_3 and duplicated by Q_4, turning on Q_6. If $V_2 < V_1$, Q_5 will be turned on by current source I. If Q_3 and Q_4 are vertical transistors, the circuit will work at much higher speed. The output can be directly used as input signal of another differential amplifier or comparator.

3.5 Current Source and Threshold Circuits

Most circuitry of VFC functions by modulating, steering, or switching currents. Bipolar transistors are, fundamentally, current-operated devices (as opposed to FETs, which are voltage operated). Depending on their desired usage, currents can be fixed, controlled by signals, or absolute temperature. In the VFC design, it is necessary to establish a temperature-independent bias reference within the circuit. This stable bias reference can be either a current or a voltage. A threshold circuit can operate after the bias reference is established, by switching the reference current to a resistor to provide V_{TH}. In other words, the threshold circuit design is nothing special but a reference current circuit design.

To realize current sources, very close matching, ratioing, and thermal tracking of transistors are necessary. *Pnp* transistors usually have lower current capacity, lower beta, and lower output impedance than *npn* transistors. This implies that significant errors can be associated with *pnp* current sources.

In full custom designs, the geometry of transistors can be scaled to yield different

... geometries are fixed, either integer ratios must be used or emitter ballast resistors must be added to fine-tune the ratio. Figure 3.8a shows a current mirror, in which output current is equal to input current. Figure 3.8b demonstrates how output current can be increased and Figure 3.8c demonstrates how output current can be decreased with respect to the reference current using emitter ballast resistors. Emitter ballast resistors serve two functions in current sources. First, they allow current ratios to be adjusted in other than integer increments. Second, they provide negative feedback to prevent extra current through one transistor on a bias string.

Next, the relationship used to calculate the emitter ballast resistor value will be developed. Recall that the current through a diode can be described as

$$I = I_s \exp\left(\frac{q\,V_{BE}}{k\,T}\right) \tag{3.4}$$

In Figure 3.8c, the ratio of two currents can be expressed as

$$\frac{I_1}{I_2} = \frac{I_s \exp\left(\frac{q\,V_{BE1}}{k\,T}\right)}{I_s \exp\left(\frac{q\,V_{BE2}}{k\,T}\right)} \tag{3.5}$$

Canceling out I_s, taking the natural log of both sides and rearranging yields

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{k\,T}{q} \ln\left(\frac{I_1}{I_2}\right) \tag{3.6}$$

This equation expresses the necessary difference in V_{BE} required for two identical transistors at the same temperature to produce a current mirror with the ratio I_1/I_2.

"Current hogging" occurs when several transistors are biased by one diode (or voltage reference) and one or more of the current source transistors are mismatched due to small differences in transistor geometry or temperature. Temperature differences can readily occur due to voltage differences on the collectors (local heating of a transistor due to its

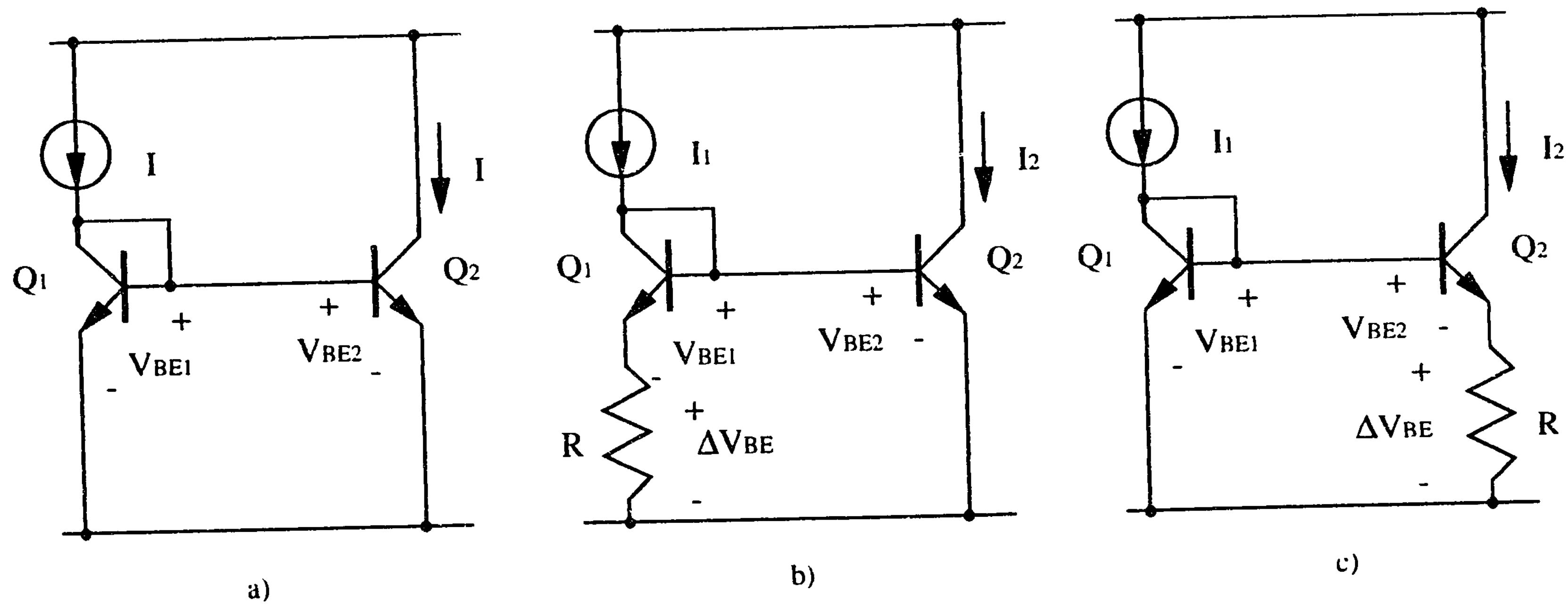


Figure 3.8 Current sources: (a) equal, (b) increased or (c) decreased output current mirrors

own power dissipation) or by one transistor's proximity to another power dissipation device. The result is that the hotter transistor has a lower V_{BE} than the others on the common bias string for a same current. The hotter transistor will take (hog) a disproportionate base current from the bias string, thus disrupting the ratios of the currents. A cure for this undesirable action is to use emitter ballast resistors in the emitters of all transistors on the bias string. A rule of thumb is to drop approximately 100 mV across the emitter resistor. The emitter resistor provides negative feedback that counteracts the current hogging action of a warmer transistor. As the V_{BE} becomes smaller due to heating, the increased current through the transistor develops a larger voltage across the emitter resistor, thus tending to turn off the transistor. The use of these ballast resistors is most important on long bias lines where transistors may be physically far apart on a die or where one or more of the transistors are relatively closer to a power-dissipating device such as an output transistor; it is also critical in high temperature circuit design. A negative impact of these resistors is that they reduce the voltage compliance of the current source by the amount of voltage drop on the resistor. On the other hand, emitter ballast resistors increase the output impedance of the current source.

3.5.1 Voltage reference threshold circuit

A voltage reference can be used for many different purposes in a circuit. It can be a rock steady reference with a known absolute value and a very low temperature coefficient used as a reference for voltage to frequency conversion or for biasing of the circuitry on a chip. A voltage reference can be created with a known temperature coefficient or resistor value dependence to cancel another effect. When operating on battery power, it is frequently desirable for circuit bias voltages to be proportional to the battery voltage to prolong the usable battery life. For example, VFC circuits can be designed to be biased such that the [illegible] power supply. This way, as the battery discharges, the frequency of the VFC remains the same. Although the power consumption of the whole circuit may decrease as the battery discharges.

There are many different implementations of voltage references. Although many are closely related, they can be roughly broken into four major groups; resistive dividers, diode, band gap, and Zener.

Resistive dividers can use current sources and transistors as well as resistors. Resistor dividers are the simplest and most widely used to provide reference voltages proportional to other voltages. The other three types of voltage references provide some measure of regulation and tend to output a constant voltage even if the supply voltage changes [1,18].

Diode references depend on the voltage of a forward-biased base-emitter junction. Normally the output current can be calculated as follow

$$I_{out} \approx \frac{V_{BE}}{R} \tag{3.7}$$

A typical value for a V_{BE} is 0.65V. This voltage depends on semiconductor process, temperature, and current. A typical V_{BE} has a temperature coefficient of approximately -2.2 mV/°C, which is of the order of -3000 ppm/°C, and a voltage coefficient of approximately +60 mV/decade increase in current. If the resistor R is a base-diffused resistor, it would introduce an additional temperature coefficient of ≈ +2000 ppm/°C into the denominator of Eq. (3.7) which would result in a total temperature coefficient of I_{out} on the order of -5000 ppm/°C. This would result in proximately 50% reduction in the value of I_{out} over a 100°C temperature change.

Band-gap reference circuit operates on the principle of compensating the negative temperature drift of V_{BE} with the positive temperature coefficient of the thermal voltage V_T. It can be expressed as

$$V_{out} = V_{BE} + K\ V_T \tag{3.8}$$

where K is a temperature-independent scal(:actor and thermal voltage $V_T = kT/q$. A more detailed circuit will be given in Chapter 4. Practical voltage reference circuits with temperature coefficients in the range of 5 to 60 ppm/°C can be obtained over -55 to +125°C [20]. A bandgap reference circuit would be a good threshold circuit for a VFC design working over the military temperature range.

The temperature coefficient of the monolithic resistors (with the exception of thin-film resistors) is too high and too nonlinear to be used for any predictable temperature compensation. However, the resistor ratios show excellent tracking over temperature, with the temperature coefficient of the resistor ratio being on the order of ±5 to ±20 ppm/°C for well-matched resistors. Thus, monolithic resistors are suitable for generating temperature-insensitive scale factors, when used in a ratio rather than in an absolute-value form.

Typical emitter base breakdown voltages are approximately 6.3V and have a temperature coefficient of approximately +2.5 mV/°C. Both the Zener voltage and its temperature coefficient depend somewhat on the semiconductor process and bias current. Figure 3.9 shows a simple voltage reference circuit which makes use of the opposite-polarity drift between the Zener voltage V_Z and the forward diode voltage V_{BE}. The supply-independent constant current I_{DZ} is generated internally by means of the current mirrors Q_2 and Q_3, it provides V_Z a positive temperature coefficient (typically ≈ +3mV/°C). The temperature dependence of the V_{BE} drop across Q_1 and D_1 result in a temperature coefficient of about +7mV at the cathode of D_1. Similarly, the thermal variation of the voltage drop across D_2 creates a temperature coefficient of ≈ -2mV/°C at the anode of D_2. Thus, a voltage reference $V_{TH} = V_{TH+} - V_{TH-}$ can be made to have a nominally zero temperature coefficient. The voltage level of V_{TH} is given as

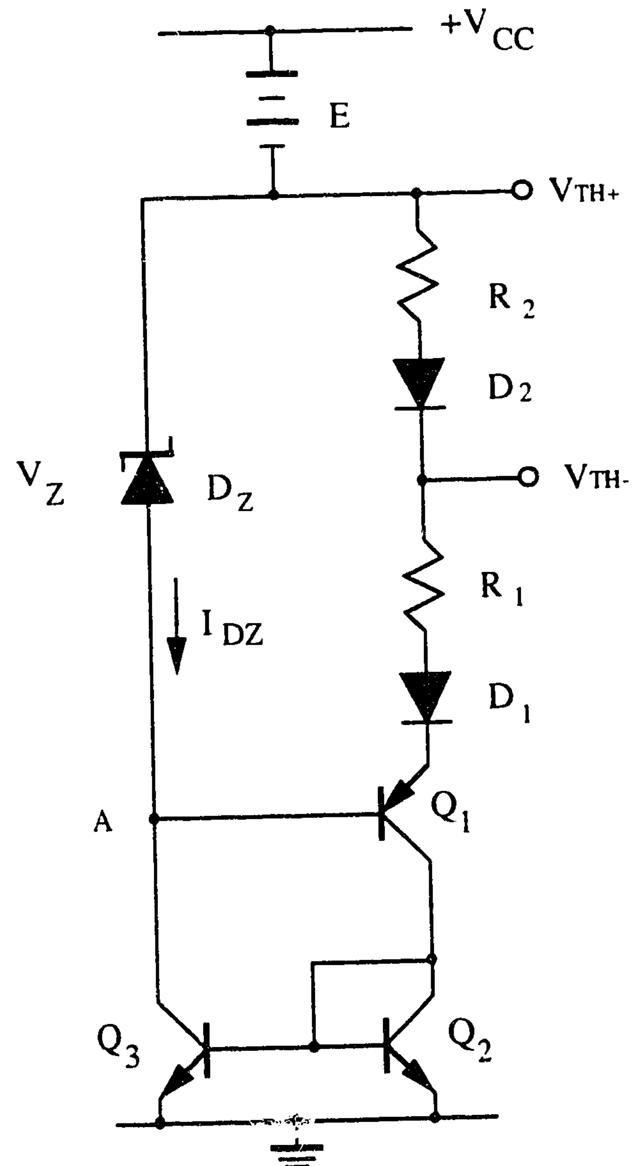


Figure 3.9 Voltage reference threshold circuit

$$V_{TH} = \frac{R_2 V_Z + V_{BE}(R_1 - 2R_2)}{R_1 + R_2} \tag{3.9}$$

The temperature coefficient of V_{TH} can be nominally set to zero by setting the resistor ratio as

$$\frac{R_1 - 2R_2}{R_2} = -\frac{\partial V_Z / \partial T}{\partial V_{BE} / \partial T} \tag{3.10}$$

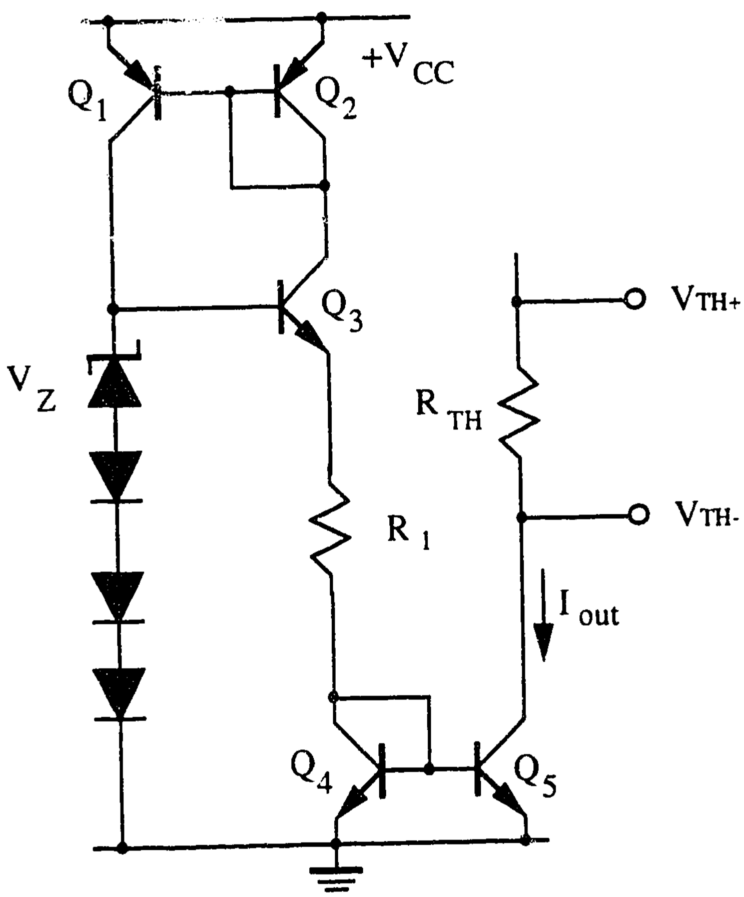
The temperature coefficient of the circuit that can be achieved is on the order of ± 30 to ±50ppm/°C. The basic disadvantage of the Zener-reference bias circuits are that they require a relatively high value of power supply (typically ≥ 10V) and introduce substantial noise into the circuit, due to the avalanche breakdown within the diode, as well as exhibiting some long-term drift of the Zener voltage V_Z. However, in the more recent designs, the long-term drift and noise problems have been largely eliminated by using buried-Zener structures [18, 20].

3.5.2 Current reference threshold circuit

When voltage reference is established, a constant current can be established by a resistor

$$I_{ref} = \frac{V_{ref}}{R} \tag{3.11}$$

The reference current in one branch of the circuit can be accurately reproduced or reflected in a second branch, relatively independent of the absolute value of the device parameters, using a current source. As long as a temperature-stable current source I_{ref} is established, the reference voltage can be easily given by connecting it with a resistor, similar to the circuit shown in Figure 3.10a. Futhermore, if using I_{out} as a differential pair biasing, the circuit can be used as multivibrator threshold circuit shown in Figure 3.10b. It has dynamic V_{TH+} and V_{TH-} voltage output simply by turning the switches (Q_1 and Q_2) on and off



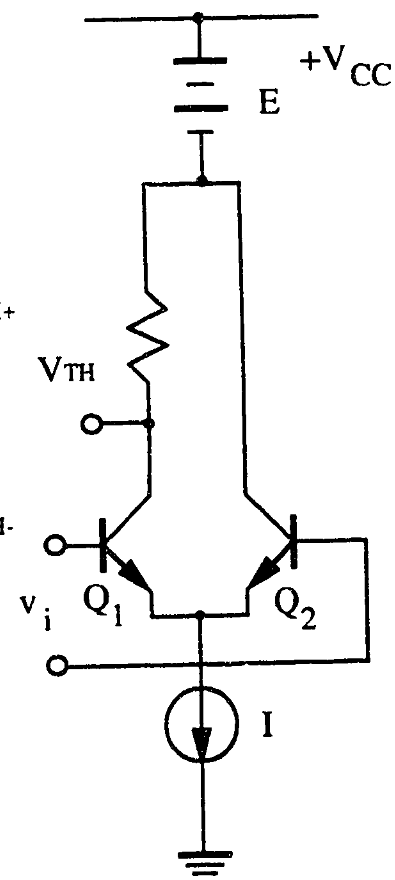


Figure 3.10 Current reference threshold circuit

alternatively. The TC of the threshold voltage is small, which is independent of the TCs of resistors due to the cancellation. The ratios of resistors are temperature-insensitive.

3.6 VFC Circuits

As introduced above, each function block can be designed independently, but how to put them together as a complete voltage to frequency converter circuit is very important. The basic constraints and limitations of monolithic circuit technology often pose a difficult challenge. This is particularly true with regard to many of the conventional techniques that cannot be directly applied to monolithic VFC designs because of the following limitations of IC components: poor absolute-value tolerances (resistor, capacitor), poor temperature coefficients (resistor, V_{BE}, beta, etc), limitations on component values (resistor, slow *pnp* transistor and low beta, small capacitor, etc), lack of coupling capacitors, limited choice of compatible active devices (depend on different IC technologies).

On the other hand, IC fabrication methods offer a number of unique and powerful advantages to the circuit designer: availability of a large number of active devices, good matching and tracking of component values, close thermal coupling, control of device layout and geometry.

Fortunately, over the years a number of VFC circuit configurations, or subcircuits, have been developed, which make efficient use of the advantages of monolithic technology, while avoiding most of its shortcomings [5,7,8].

3.6.1 Simple VFC

The circuit shown in Figure 3.11 provides an output square wave whose frequency is directly proportional to an input control voltage [8]. The circuit is comprised of a V-I converter (Q_1-Q_8), a current switch (Q_9- Q_{13}) for charging and discharging the timing

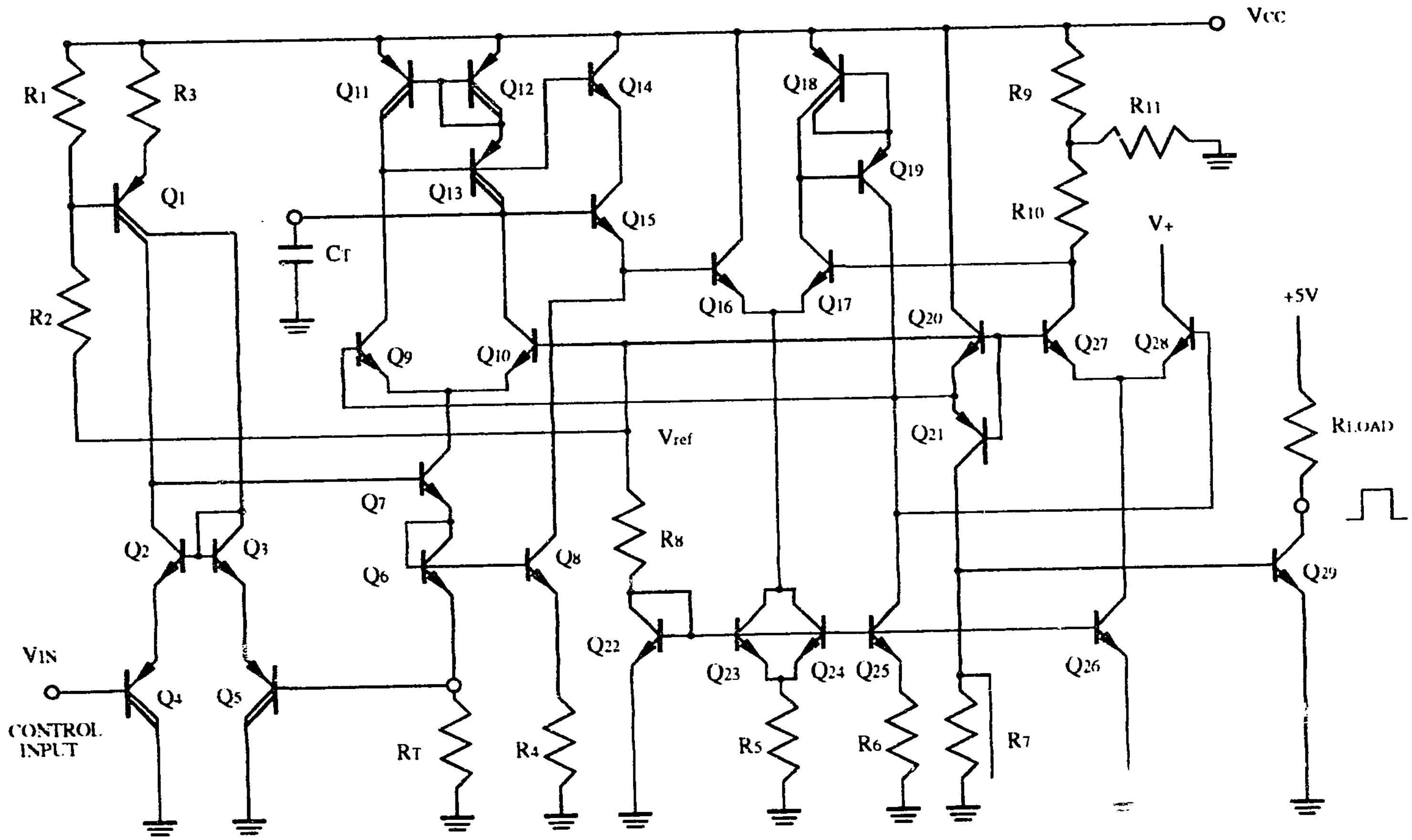


Figure 3.11 Basic VFC

capacitor, C_T, a buffer (Q_{14}, Q_{15}), and a non-saturating, high speed comparator (Q_{16}-Q_{29}). The input control voltage may range from 0 to 2 volts, producing a frequency

$$f_o = \frac{V_{IN}}{2\,V_{TH} R_T C_T} \tag{3.12}$$

where

$$V_{TH} = \left(\frac{R_9 R_{11}}{R_9 + R_{11}} + R_{10} \right) I_{C26} \tag{3.13}$$

and

$$I_{C26} = \frac{V_{CC} - V_{BE22}}{R_1 + R_2 + R_8} \tag{3.14}$$

The V-I converter operates by keeping the voltage across R_T equal to V_{IN}, thus generating a current in Q_7 equal to V_{IN}/R_T. This current alternately charges and discharges C_T by means of the current switch. The triangle wave is buffered with Q_{15}, along with Q_{14} providing base current cancellation. The buffer is also operated at a current proportional to the control current (from Q_8) to reduce the effects of its base current and to speed up the response of the buffer at higher frequencies. The output of the buffer is compared with Q_{16}-Q_{17} to the switching thresholds which are switched between V_H and V_L with Q_{27}-Q_{28}. Q_{20} and Q_{21} clamp the swing on Q_{27}-Q_{28} and prevent saturation of any transistors in the loop. Q_{21} also drives Q_{29}, which provides a TTL compatible output. This VFC provides an accuracy better than 1% in the range of 10 Hz to 10 kHz and exhibits a temperature stability of around 200ppm/°C. The circuit is power supply dependent.

3.6.2 Modified VFC

The circuit described above in 3.6.1 can be modified structurally to achieve better performance. The modified circuit is shown in Figure 3.12. In the original circuit, shown in Figure 3.11, the current through Q_7 could be large comparing with the current through Q_2, therefore, I_{B7} could be taking too much from I_{C2} (about 50 μA). So Q_6 and Q_7 are reconnected as Darlington configuration; the difference between the threshold voltages is dependent on the power supply, a voltage reference circuit (D_Z, Q_{30}-Q_{36}) is used to get rid of the dependency. Unlike (3.14) I_{C26} is temperature stable

$$I_{C26} = I_{C35} = \frac{V_{DZ} + V_{BE30}}{R_{12}} \tag{3.15}$$

Q_{35} and Q_{36} form a current mirror, so that the current through D_Z and Q_{30} is equal to constant current I_{C35}. $V_{DZ} + V_{BE30}$ has TC close to 0. After all these modifications, the new circuit is able to operate with a much better performance (improved linearity and temperature stability).

3.6.3 Modified Schmitt trigger's threshold independent of V_T

The threshold voltages of a nonsaturated bipolar Schmitt trigger include a term that depends on the V_T. But V_T is proportional to temperature (V_T = 26 mV at room temperature), and compensating for variations complicates the circuit in cases where the trigger is used in voltage-to-frequency converters. Schmitt triggers based on transconductance amplifiers, however, can be easily modified to obtain thresholds independent of V_T.

Consider the typical circuit shown in Figure 3.13a. Input voltage v_i switches the current source, I. The output voltage, v_r, can be one of two values, namely, $V_L = V_{CC}R_2/(R_1+R_2)$, when the current I is intercepted by the transistor Q_1; or $V_H = V_{CC}R_2/(R_1+R_2) + I(R_1R_2)/(R_1+R_2)$, when I is intercepted by Q_2 and is presented to current mirror Q_3-Q_4. The output changes state when the input voltage has threshold values of

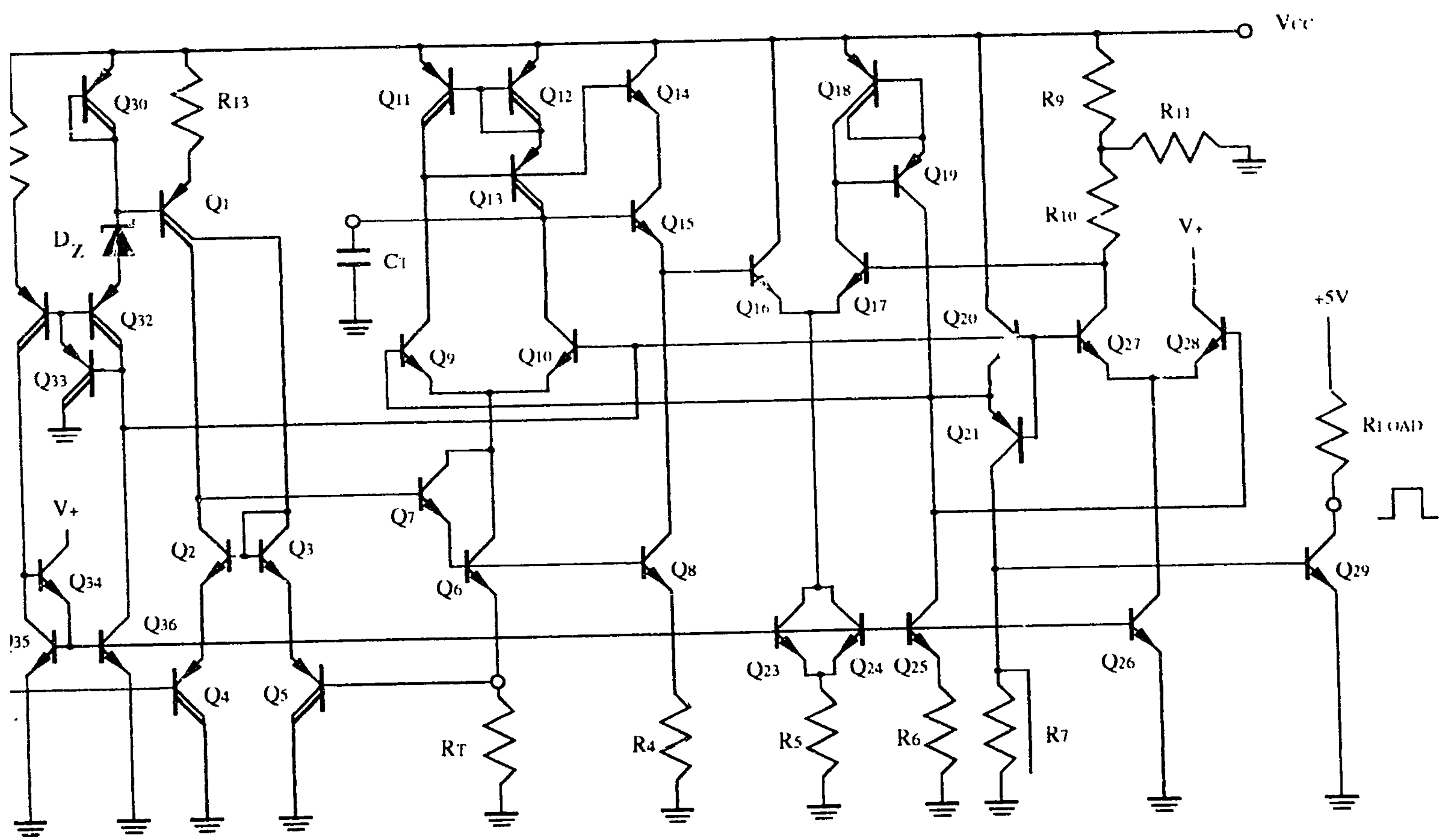


Figure 3.12 Modified VFC

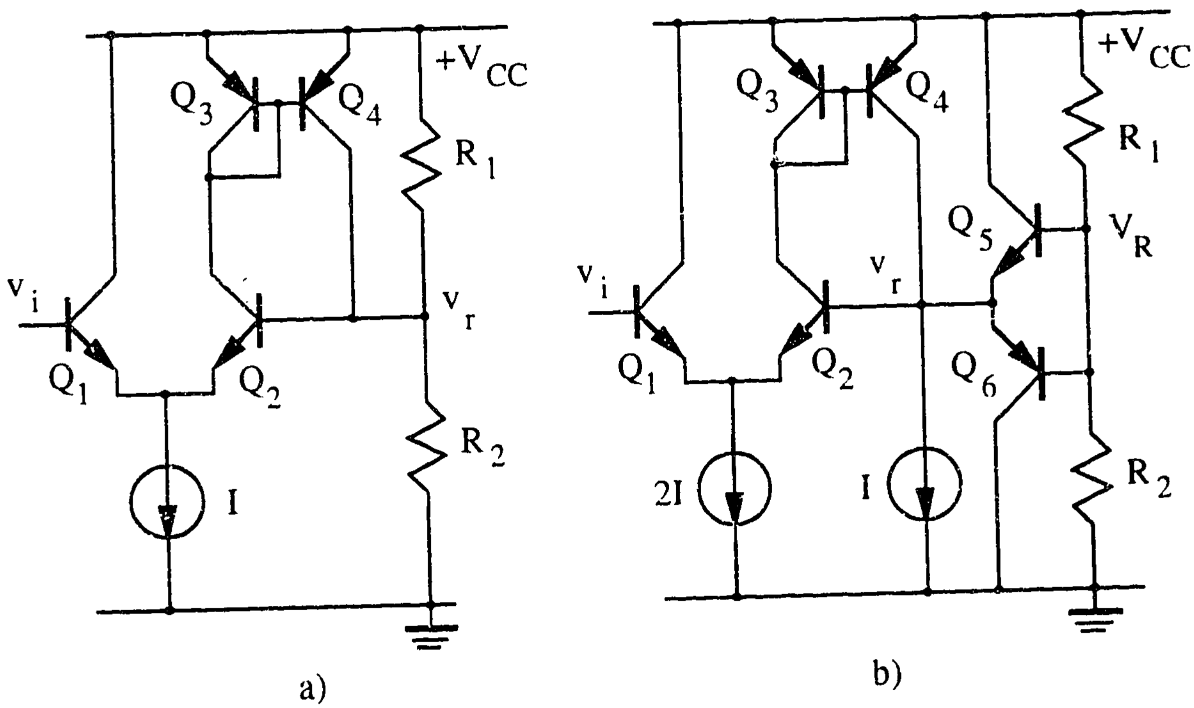


Figure 3.13 Schmitt trigger circuits

$V_{iL} \approx V_{rL} + 2V_T$ and $V_{iH} \approx V_{rH} - 2V_T$. When the differential voltage, $v_d = v_i - v_r$ is inside the interval $\pm 2V_T$, both Q_1 and Q_2 are active, and the transconductance is considered constant, equal to $I/2V_T$. For v_d outside of this interval the transconductance is zero. A change of state occurs when all transistors are active in the positive feedback loop that includes the transistors Q_1-Q_4 and resistors R_1 and R_2. Then, the change of state occurs immediately when $v_d \approx \pm 2V_T$.

To eliminate the terms $\pm 2V_T$, we increase the tail current to 2I as shown in Figure 3.13b, add a current source, I, and add limiting transistors Q_5 and Q_6. In this circuit, v_r has the values $V_{rL} = V_R - V_{BE(ON)}$ when the current 2I is intercepted by Q_1, and current I becomes the emitter current for Q_5; $V_{rH} = V_R + V_{BE(ON)}$, when current 2I is intercepted by Q_2, reflected by the current mirror, and I becomes the Q_6's emitter current.

Here, $V_R = V_{CC}R_2/(R_1+R_2)$. The transition from one state to another takes place when Q_4's collector supplies the current I, i.e., when Q_1 and Q_2 carry equal currents. Hence, the circuit is characterized by threshold voltage $V_{iL} = V_{rL}$ and $V_{iH} = V_{rH}$.

Readers may point out that the voltage $V_{BE(ON)}$, is also dependent on temperature and d is unstable. However, the reference voltage V_R and the voltage v_r can now be used for switching an exact current, which creates an exact voltage drop.

The reworked (final) circuit is shown in Figure 3.14. Here, v_r switches the current I_0, and this switching takes place when the current supplied by Q_4 equals I. But this happens when v_i and v_o are equal. Hence, the switching thresholds of the circuit are $V_{iL} = V_{oL} = V_{CC} - E - I_0R_{TH}$ and $V_{iH} = V_{oH} = V_{CC} - E$. The voltage E can be created by a thermo-compensated Zener diode. Well-known circuitry reference to obtain a constant and stable voltage drop, I_0R_{TH}, can also be applied. Moreover, in many Schmitt trigger

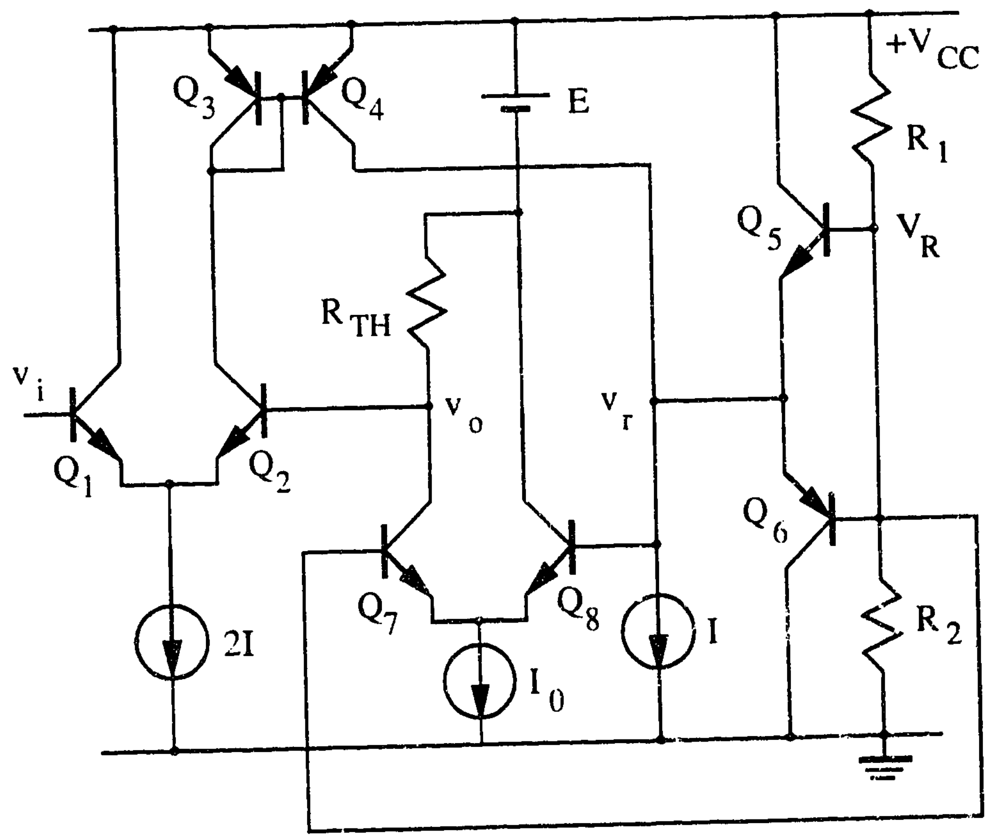


Figure 3.14 Modified trigger circuit

$V_{iL}=I_0R_{TH}$.

3.7 High Precision Voltage-to-Frequency Converter

3.7.1 Overview

A lot of work has been done to develop the design methods of the circuits where the oscillation parameters (amplitude, frequency, phase, and, in multivibrators, duty cycle) provide information on the values of passive (usually resistors and capacitors) or active (current and voltage sources) external sensor elements. These values are usually functions of some other factors (mechanical force, electric or magnetic field, temperature, etc.) and the modification of oscillation parameters gives the information about these factors.

Many integrated sensors can be used as the above mentioned elements [5] and the oscillating circuits driven from such sensors became important interface circuits. The oscillating circuits with linearly controlled frequency are usually required. The frequency output being noise immune satisfies the current trend in realization of integrated sensors, namely, the demand for communication with a microprocessor. The preference is given to multivibrator circuits because the rectangular multivibrator output is easier convertible in the final digital form. Besides the multivibrators do not require an amplitude stabilization circuit, the amplitude and frequency transients are very short (their duration is about one oscillation period) and a wide frequency control can be achieved by modification of the current which is charging the timing capacitor [6]. If a multivibrator is preceded by a transconductance amplifier (i.e a voltage-to-current converter) the multivibrator becomes a voltage-to-frequency converter which can be used with wide variety of sensors.

The voltage-to-frequency converters described in this work also include a voltage-to-current conversion stage and a modified current-controlled oscillator proposed in [7].

final forms to use a window comparator which includes two separate input stages and a common output stage. This output stage drives the switch of the current source discharging the timing capacitor and, simultaneously, drives a switch of the bias current for the window comparator input stages. The voltage swing of the output stage is limited which allows to keep the comparator out of saturation. This solution creates two positive feedback loops with separate switching operation near the comparator thresholds. As a result of such approach the voltage swing on the timing capacitor is nearly equal to the voltage difference between the comparator thresholds. Thus, the capacitor voltage swing, in our case, does not include a small thermo-dependent term distorting the converter voltage-to-frequency characteristic. The stability of the voltage difference between the thresholds was provided by a separate current source included in the circuit.

Other measures improving the linearity of the converter characteristic and its thermal behavior included introduction of the input current compensation in the window comparator and very careful design of the follower in the voltage-to-current converter feedback.

3.7.2 Circuit operation

A block diagram of the converter is shown in Figure 3.15. The input signal is applied between $+V_{CC}$ power supply line and the operational amplifier input. The operational amplifier feedback is closed via an emitter follower. If the amplifier gain is high one can write that:

$$I_T = \frac{V_{in}}{R_T} \tag{3.16}$$

If it is possible to neglect the feedback transistor base current (this is achieved using a compound transistor: the detailed description is given below) then the current supplied to

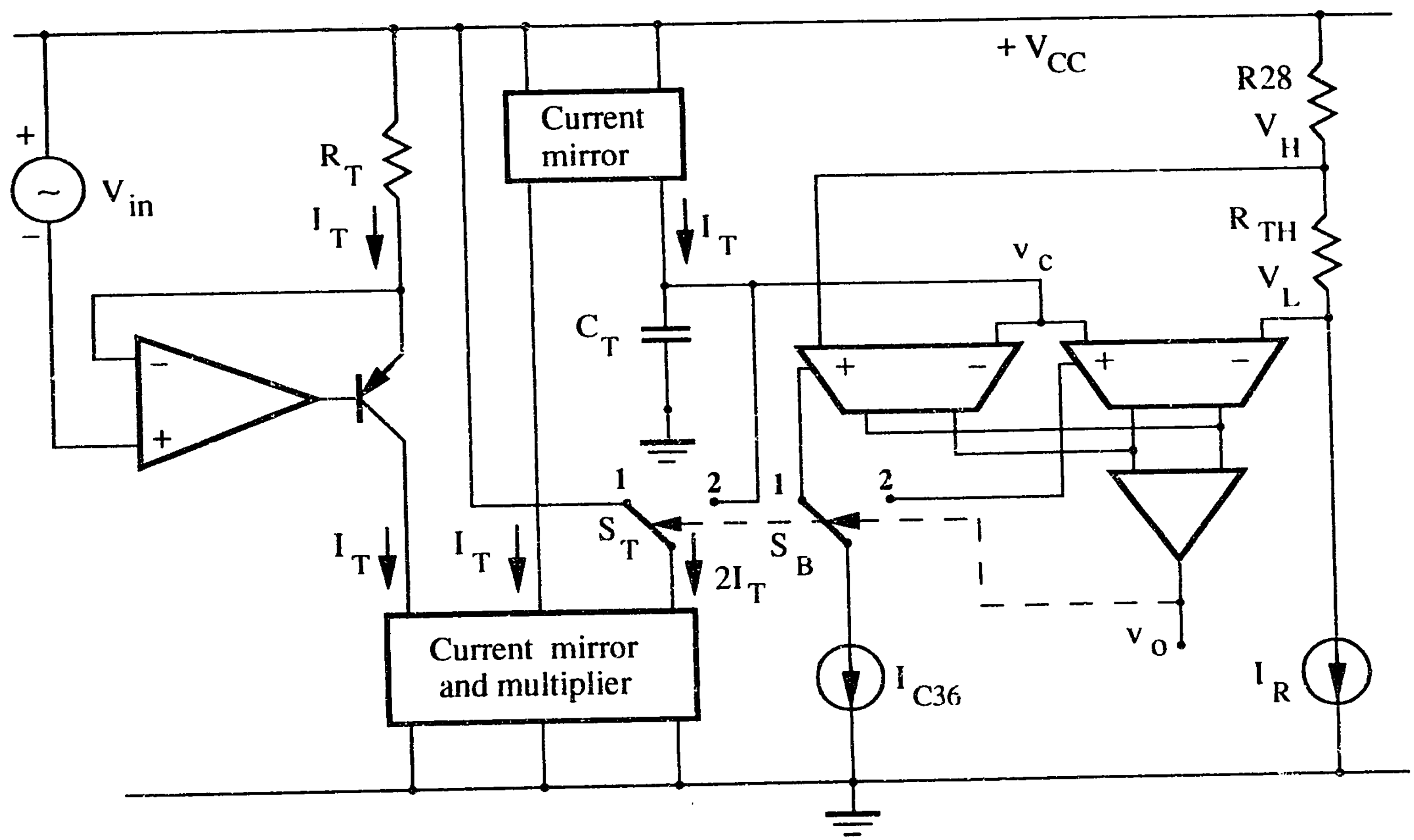


Figure 3.15 Block diagram of the voltage to frequency converter

the bottom current mirror will be equal to I_T. This current mirror supplies two currents. The first current, I_T, is mirrored by the top current mirror, and is supplied to the timing capacitor C_T. The direction of the second current, $2I_T$, is controlled by the switch S_T. During the first half of oscillation period the switch S_T in the position 1 (as shown in the Figure 3.15) and the timing capacitor is charged by the current I_T from the top current mirror. During the second half of oscillation period the switch S_T is in the position 2 and the current $2I_T$ is sourced from C_T. The capacitor C_T is, hence, discharged by the current $I_T = 2I_T - I_T$. The position of the switch S_T is controlled by the window comparator output voltage V_0.

This window comparator includes two input stages and a common output stage. The timing capacitor voltage v_c is applied to the common point of the input stages. A stable reference current I_R creates the voltage drop $\Delta V_{TH} = V_H - V_L = I_R R_{TH}$. The second input of the left input stage has the potential V_H, the second input of the right input stage has the potential V_L. The voltage v_c swing is practically equal to ΔV_{TH}. The charge balance, thus , gives the oscillation frequency

$$f_0 = \frac{I_T}{2C_T \Delta V_{TH}} \tag{3.17}$$

Substituting (3.16) into (3.17) one obtains the equation of the voltage-to-frequency converter characteristic

$$f_0 = \frac{V_{in}}{2C_T R_T \Delta V_{TH}} \tag{3.18}$$

The switching operation is following. When v_c is increasing and heading toward V_H the switch S_B which is also controlled by the output voltage v_0 is in the position 1 providing the bias current I_{C36} to the left input stage. When the voltage v_c is equal to V_H the output voltage v_0 changes state (in reality, this happens when v_c is slightly less than V_H). Now the switch S_T is connected to the timing capacitor and the switch S_B is in the position 2 providing the bias current to the right input stage of the window comparator. This switching of bias only is faster than switching of bias combined with switching of thresholds [8]. The bias provided to the right input stage confirms the new position of switches and the timing capacitor starts to discharge. When the voltage v_c becomes equal to V_L the output voltage changes state again, the switches S_T and S_B return to the position shown in Figure 3.15, and the timing capacitor starts to charge again.

3.7.3 The circuit implementation

Implementation of the above described voltage-to-frequency converter circuit includes the following blocks.

3.7.3(a) Input voltage-to-current converter

The circuit of the input voltage-to-current conversion stage is shown in Figure 3.16. It is a one-stage operational amplifier with external feedback via transistors Q_9 to Q_{13}. The amplifier gain is high and in the steady-state condition the base potentials of Q_1 and Q_2 are equal and the current I_T is determined by (3.16). Transistors Q_{11} and Q_{13} are connected as a combination transistor [9] which has the properties of *pnp* transistor and has high current gain. This avoids an excessive base current (which is especially important at high I_T currents, when the current gain of *pnp* transistors is low). As a result the current entering the bottom current mirror (transistors Q_{17}, Q_{18}) is nearly equal to I_T. The Darlington circuit Q_{14}, Q_{15} allows to avoid the base current losses and to repeat the current I_T at the collector of Q_{18}. The current $2I_T$ at the collector of Q_{19} is obtained by proper design of the emitter

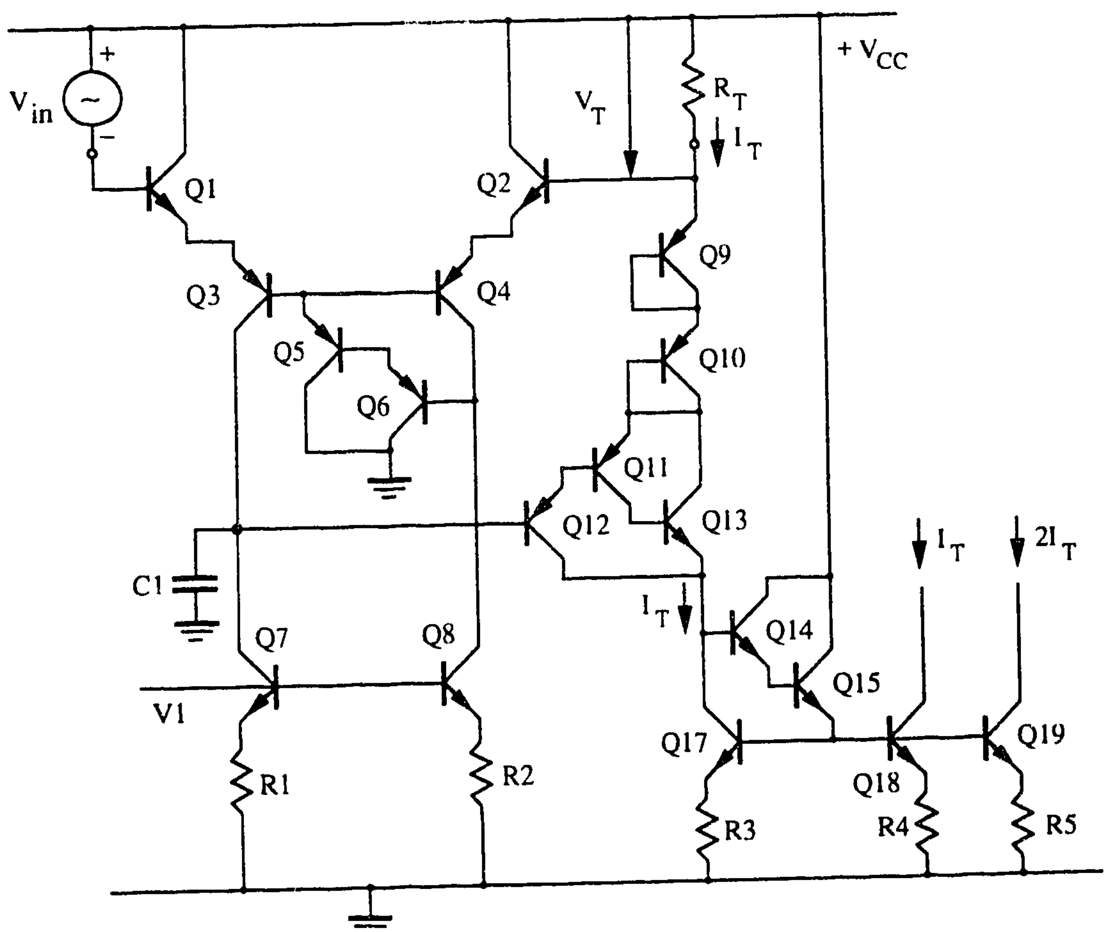


Figure 3.16 Input voltage to current converter

resistance R_5. The voltage V_1 is taken from the reference voltage circuit. Capacitor C_1 is used for the operational amplifier frequency compensation.

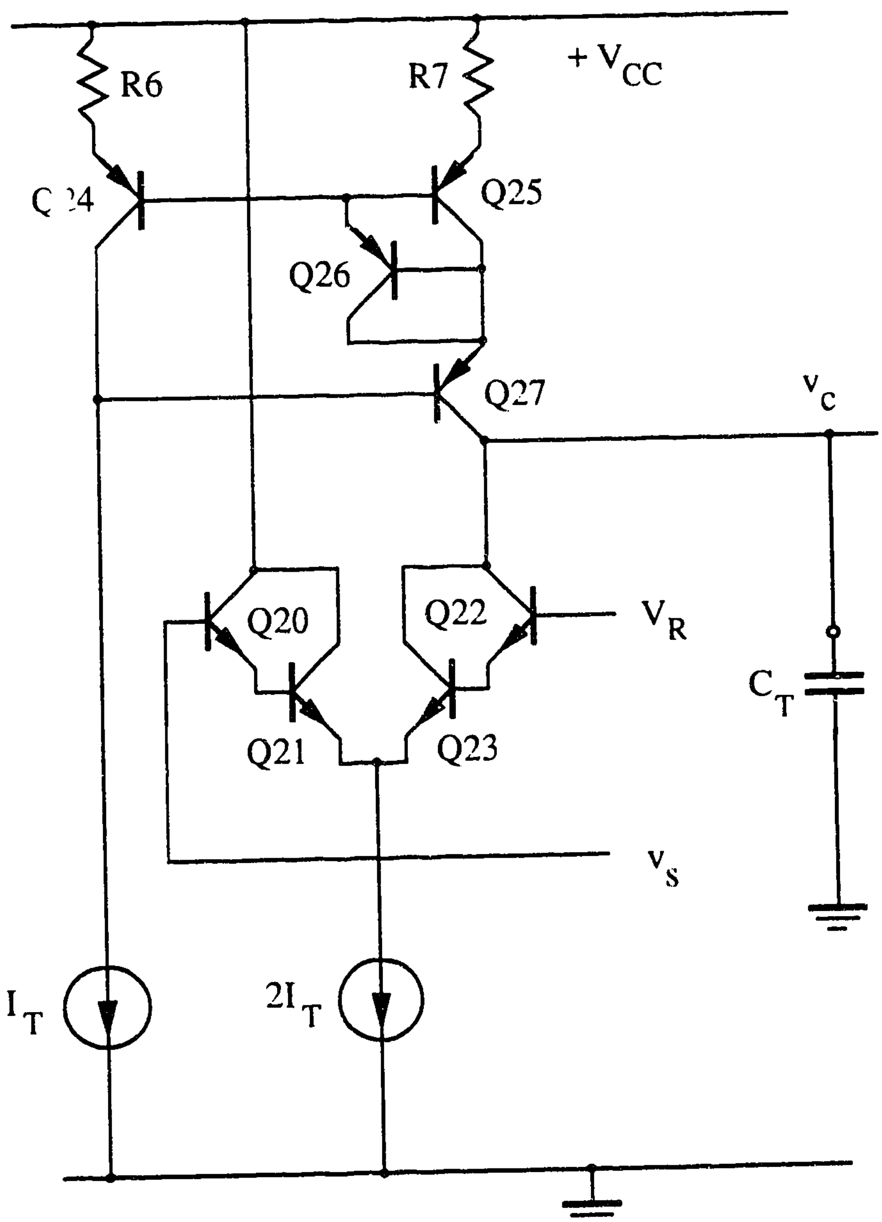
3.7.3(b) Timing capacitor charge and discharge circuit

The circuit which is used to charge the timing capacitor C_T is shown in Figure 3.17. It includes a current mirror (transistors Q_{24} to Q_{27}) which is sinking the current I_T into C_T, and a transconductance amplifier (transistors Q_{20} to Q_{23}) which is used as a switch for the tail current $2I_T$ (both currents are supplied from the input voltage-to-current converter stage). The base of Q_{20} is driven by the voltage v_s, the base of Q_{22} has the potential V_R. Both are provided from the window comparator circuit described below.

When the voltage v_s is HIGH, transistors Q_{22} and Q_{23} are OFF, transistors Q_{20} and Q_{21} are ON and the current $2I_T$ is sourced from the $+V_{CC}$ line. The current I_T is mirrored by the current mirror and appears in the collector of Q_{27}. The collector current of Q_{27} is charging the timing capacitor. When v_s is switched to LOW, transistors Q_{22} and Q_{23} are ON, transistors Q_{20} and Q_{21} are OFF. The tail current $2I_T$ is now intercepted by Q_{22} and Q_{23} and the timing capacitor is discharged by the difference of the tail current and the collector current of Q_{27}. Thus, the timing capacitor is discharged by the current of the same value as the charge current.

3.7.3(c) Window comparator circuit

The voltage v_s driving the switching transconductance amplifier described in the previous section is obtained in the window comparator circuit (Figure 3.18). This circuit includes two input transconductance stages (transistors Q_{50} to Q_{60}). The outputs of the input transconductance stages are connected in parallel and then connected to the window



Figue 3.17 Timing capacitor charge and discharge circuit

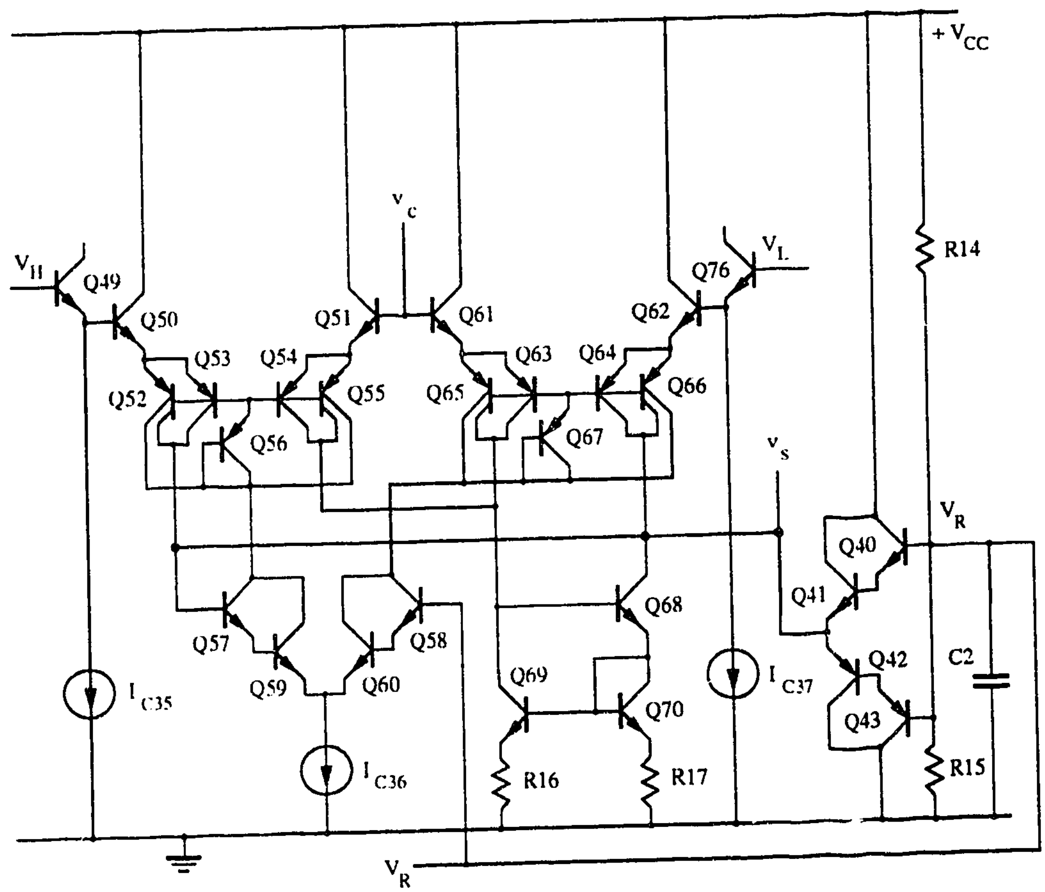


Figure 3.18 Window comparator circuit

comparator output stage (transistors Q_{68} to Q_{70}). The timing capacitor voltage v_c is applied to the common point of the input transconductance stages. Left input of the left input stage is connected to the reference voltage V_H via a emitter follower Q_{49}, right input of the right stage is connected to the reference voltage V_L via a follower Q_{76}. The bias currents I_{C35}, I_{C36}, and I_{C37} for the comparator and followers are referring to the collectors of the corresponding transistors in the full converter circuit.

In addition, the circuit includes a limiting clamper (transistors Q_{40} to Q_{43}) which clamps the switching voltage v_s to a constant voltage V_R and limits the swing of v_s by $V_R \pm 2V_{BE(ON)}$.

Assume that the timing capacitor is charging. Then the voltage v_s should be HIGH. If it is then the current I_{C36} is intercepted by the transistors Q_{57}, Q_{59} and supplied to the window comparator left input stage. The voltage v_c is less than V_H and the current I_{C36} will be supplied to the transistor Q_{52} and [illegible]. The transistor Q_{53} will develop a current which will be sinked by the transistors Q_{42}, Q_{43} of the clamped limiter and the HIGH state of the voltage v_s will be confirmed (in other words, positive feedback which is necessary for the correct operation of the timing capacitor charge and discharge circuit is provided).

When the voltage v_c approaches the value of V_H the collector current of Q_{57}, Q_{59} will be diverted into Q_{55} and Q_{51}. The current in Q_{53} will disappear. The collector current in the transistor Q_{54} will emerge and will enter into the window comparator output stage. The voltage v_s becomes LOW and the collector current of the output stage will be sinked by Q_{41} and Q_{40}.

When the voltage v_s is LOW the current I_{C36} is supplied to the right input stage of the window comparator. The voltage v_c is higher than V_L and, hence, this current will enter Q_{62} and will force to operate the transistor Q_{63}. The current to the output stage will be provided. At the same time Q_{64} will be without current and the LOW state of v_s will be confirmed.

This change of state results in the timing capacitor discharge. The voltage v_c is decreasing now . When v_c approaches the value of V_L the collector current of Q_{58}, Q_{60} will be directed into Q_{65} and Q_{67}. The current in Q_{63} will disappear. The collector current in the transistor Q_{64} will emerge, the voltage v_s becomes HIGH again and all the processes will be repeated.

3.7.3(d) Reference voltage circuit

The reference voltage circuit (Figure 3.19) includes a temperature compensated Zener diode (transistors Q_{84} and Q_{85}) with the current determined by resistor R_{19} and series connected diodes Q_{79} to Q_{83}. Transistors Q_{86} to Q_{100} represent two current mirrors: one is providing the mirroring of the current developed in the resistor R_{19} to Zener diode, another is providing a stable current I_{TH} (the design details can be found in [9]) in the resistor R_{TH}. Hence, a stable voltage difference $\Delta V_{TH} = V_H - V_L$ is created.

If one substitutes $\Delta V_{TH} = I_{C100} R_{TH}$ in (3.18) and obtains

$$f_0 = \frac{V_{in}}{2 C_T R_T I_{C100} R_{TH}} \tag{3.19}$$

then this results allows to estimate the stability of the oscillation frequency. The current I_{C100} is approximately inversely proportional to R_{19}, then as it follows from (3.19), if the resistors R_{19} and at R_{TH} are located in the geometric vicinity on the chip the design will provide good temperature stability if the oscillation frequency (assuming that the time constant $C_T R_T$ due to the external elements C_T and R_T have low temperature coefficient).

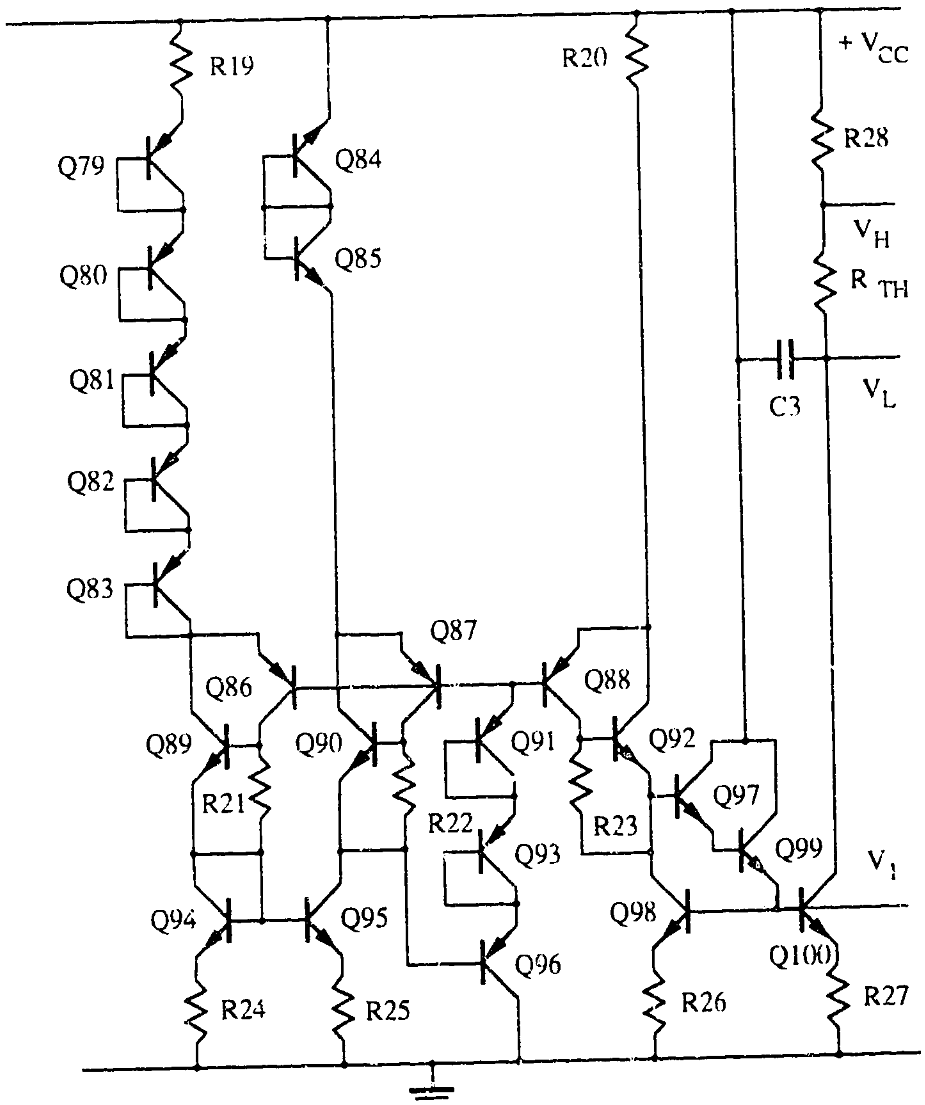


Figure 3.19 Reference voltage circuit

3.7.3(e) The voltage-to-frequency converter circuit

To verify experimentally the feasibility of the temperature compensation technique developed before in this chapter. The whole circuit of the voltage-to-frequency converter is shown in Figure 3.20. In addition to the previously described subcircuits it includes an emitter follower with bias cancellation (transistors Q_{29} to Q_{34}) between the timing capacitor and the window comparator. The voltages V_H and V_L are applied via similar followers as well. Q_{29} - Q_{34}, Q_{44} - Q_{49} and Q_{71} - Q_{76} are emitter followers together with base-current compensation circuits, where the bases currents are measured internally and fed back to the input terminals of the amplifiers, as shown in Figure 3.20. This way, base currents of Q_{49} and Q_{76} will not cause additional voltage drops across R_{28} and R_{TH}, the threshold circuit becomes temperature independent. When the window comparator senses the the voltage across the timing capacitor, the base-current compensation circuit also do a good job without taking extra current from C_T, increasing output frequency temperature stability. C_1 - C_3 are junction capacitors which are formed by the buried layer diffusion and the isolation diffusion reaching into the buried layer. They are used as high frequency compensation capacitors. Since the *pnp* transistor has very low beta, Q_{11} and Q_{13} are connected as a combination transistor, together with Q_{12}, which has very high beta value $\beta = \beta_{11}\ \beta_{13}\ \beta_{12}$. Q_{100} and Q_{98}, R_{26} and R_{27} should be transistor and resistor pair physically layouted together, so that when the temperature changes, they came be heated up or cooled down at the same time, providing identical output current to R_{TH} to generate constant threshold voltage V_{TH}. The output voltage is taken from the Darlington follower Q_{77}, Q_{78}.

The circuit design was done assuming realization by Semicustom Analog Array developed by Ferranti Interdesign [10]. The *npn* transistors Q_{19}, Q_{98}, Q_{100} should be double sized (or two transistors connected together). The beta value of large current *pnp*

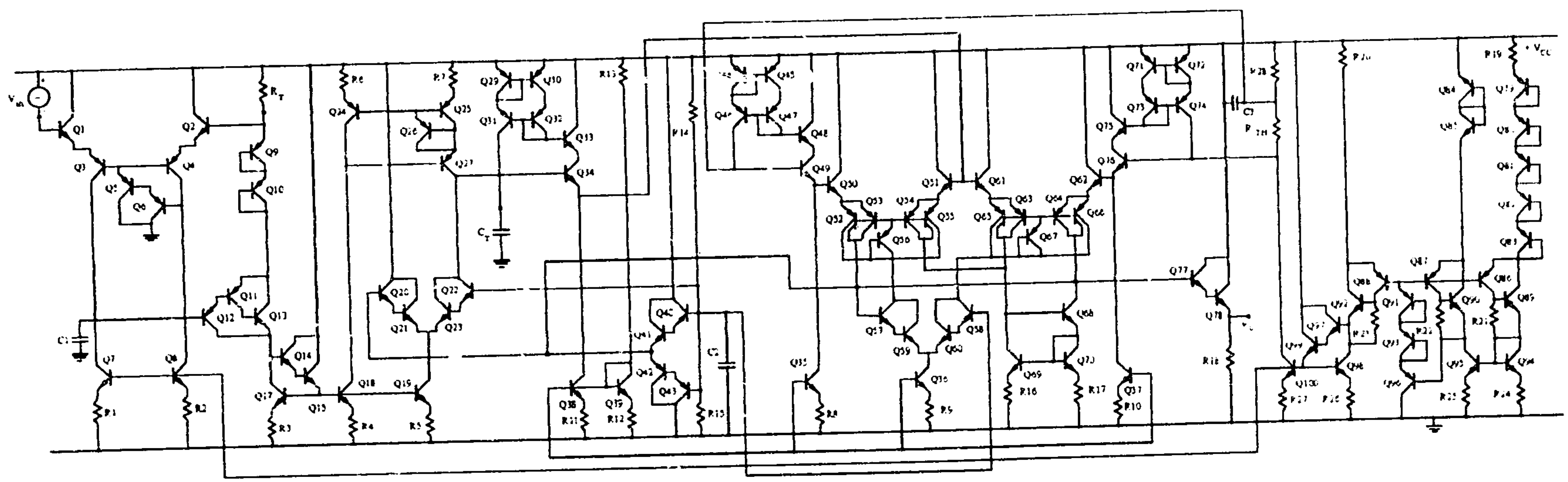


Figure 3.20 The voltage to frequency converter circuit

transistor is very small, *pnp* transistors Q_{24}, Q_{25}, Q_{27} are also used double sized transistors (or two lateral transistors together) so that the current mirror can handle large currents. The circuit has potential to operate at high temperature environments with the temperature compensation techniques introduced in Chapter 4.

3.7.4 Conclusion

Using a window cooperator with an output voltage swing limiter in the triggering circuit of a current-controlled multivibrator allows to be made the voltage swing on the timing capacitor equal to the difference between threshold voltages. This difference can be made very stable applying the well known design methods for reference current sources and voltage references. The approach gives the oscillation frequency a low temperature coefficient. For this reason, we chose the window comparator circuit. This results in a high operation speed of the triggering circuit.

4 TEMPERATURE COMPENSATION METHODS FOR BIPOLAR ANALOG INTEGRATED CIRCUITS

4.1 Introduction

During the last three decades, interest in the development of high-temperature electronics has attracted researchers from industry and universities. The applications considered were quite different. Certain common device and circuit requirements have emerged from their efforts which now constitute the "unwritten" rules of a successful high-temperature technology. A very rough but succinct quantitative summary of these requirements is that for most applications, packaged devices and circuits must be able to operate reliably "in the field" for at least one thousand hours at junction temperatures up to 300°C and withstand shock, vibration and wide atmospheric pressure ranges. The applications are such as oil, gas and geothermal well logging, jet engine control, under-hood automotive engine monitoring and industrial process control [23-28,33].

The traditional maximum ambient temperature for operation of integrated circuits has been 125°C defined primarily by the requirements of many military systems. Conceptually, the design of a high-temperature circuit is very different from a similar design for the commercial or military temperature ranges. Several component characteristics change so much that most conventional circuits fail to work at high temperature (>200°C). Bipolar circuits with either junction or dielectric isolation degrade due to changes in device operating points and high leakage currents.

To compensate for variation in characteristics due to temperature, the Si device has been found to be the most useful at this time in realizing high-temperature ICs. For this, it is necessary not only to develop such a high-temperature device technology in durability and reliability, but also to compensate the fluctuation in characteristics by improving circuit construction. In particular, it is important for circuit design to stabilize the dc bias in the high-temperature range because integrated circuits become nonfunctional due largely to such fluctuation.

4.2 Characteristics of Silicon Devices at High Temperature

A question of current relevance among workers in need of severe-environment electronics is that of the choice of technology for the near future. The question is not a simple one because the required operating temperature range is a key consideration. Moreover, the issue of metallization reliability is, at the present time, the single outstanding problem in need of a solution, regardless of the nature of the semiconductor material used to build the circuits. Indeed, workers who monitor failures of parts operating "in the field" for extended periods of time (hundreds of hours), invariably find that bonds, wires and other packaging-related items are the overwhelming culprits. Failures within the semiconductor materials are relatively rare under typical operating requirements.

Silicon has clearly been shown to perform well in digital and analog applications up to about 250°C [29-32]. Other materials such as compound semiconductors (e.g. GaAs, GaP, SiC) seem to show promise for the range 200-500°C, it seems therefore, that the technology of choice is silicon, not only because currently standard and mutually compatible processes, metallization and packaging techniques exist which will provide satisfactory products.

For applications beyond this temperature, new process and/or circuit techniques will have to be developed and other materials may be required since junction leakages are large enough in most commercial bipolar and CMOS process to disrupt many digital and most analog silicon IC functions.

Under a high-temperature environment, the characteristics of silicon devices vary depending on temperature which has an effect on circuit operation. In Table 4.1, the effects of high-temperature on the main classes of silicon devices and circuits are summarized.

DEVICE CLASS	OBSERVED EFFECTS
PN junctions	• Forward-bias voltage desreases by ≈ 2mV/°C (constant current) • Carrier mobility decreases • Reverse-bias small-signal conductances increase exponentially
BJTs	• V_{BE} decreases by ≈ 2mV/°C at constant I_C • Mobility decreases cause increases in base and collector resistances • Current gain (beta) increases as T^y, $1<y<2$
Analog	• Gain-bandwdth product decrease • Input offset current increases
JFETs (n channel)	• Mobility decreases as T^{-n}, $1<n<2$ • Channel-turnoff voltage magnitude increases
MOSFETs	• Mobility decreases as ≈ $T^{-1.5}$ • Threshold voltage magnitude decreases as p_0T, $p_0 \approx$ -2mV/°C • Zero-temperature-coefficient bias points • Junction leakage currents increase exponentially
CMOS circuits	• Input protection (diodes') leakage currents increase exponentially
(junction isolated)	• Latchup holding and trigger currents decrease as T^{-x}, $3.3<x<4.1$ • Bulk resistivity increases as ≈ $T^{2.3}$
Analog	• Amplifier gain-bandwidth products decrease • Amplifier input-offset votages increase • Leaky switches impose minimum sampling rate in switched-capactor applications

TABLE 4.1 High-temperature effects and limitations of various classes of silicon devices and circuits (25- 300°C)

Material	Energy bandgap E_g at 0 K (eV)	Technology	Temperature (°C) (demonstrated)	References
Si	1.21	BJT MOSFET	325 380	[34] [35]
GaAs	1.52	BJT	400	[36]
$GaP/Al_xGa_{1-x}P$		BJT	550	[37]
GaP	2.34	BJT MESFET	450 295	[38] [39]
SiC	2.39 to 3.33	MOSFET	600	[40,41]
Diamond	5.45	MESFET	1000	[42]

TABLE 4.2 Semiconductor material with high-temperature electronics potential

Table 4.2 lists the highest temperatures at which integrated devices and circuits built with semiconductors other than silicon have been reported to remain functional.

In bipolar transistors, all currents bear an exponential dependence on absolute temperature. The widely-used rule of thumb that junction currents "double approximately for every 10°C increase", corresponds to the fact that in most conventional IC processes, including junction-isolated and dielectric-isolation integrated technologies, both forward and reverse junction currents are widely observed to vary as $n_i(T)$ near room temperature where e they are dominated by generation-recombination processes. Since no ZTC (zero-temperature-coefficient) bias point exist for bipolar transistors (not like MOS transistors), circuit techniques must be used for purposes of current stabilization. These characteristics will be discussed in the following.

4.3 Leakage Current and Compensation

Important silicon material-related changes at high temperature are p-n junction leakage current increases, carrier mobility decreases, and changes in Fermi level both in the bulk and at the surface.

Both bulk and surface carrier mobility are known to decrease with temperature. For bipolar devices, mobility decreases lead to second-order device effects, such as increase of parasitic base and collector resistance.

The tendency of the Fermi level toward midgap with increasing temperature has first-order parametric effects for MOSFET's and JFET's, but is less important for bipolar transistor devices.

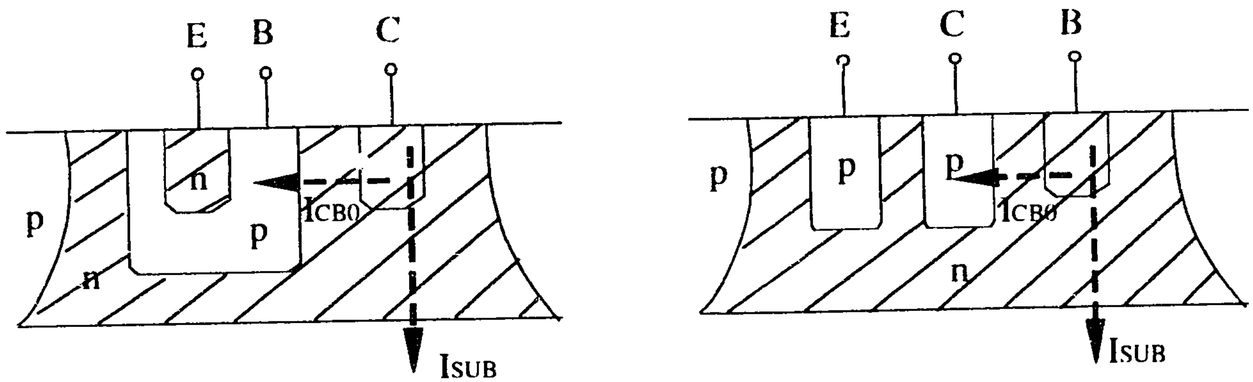
Bipolar circuits with either junction or dielectric isolation degrade due to changes in device operating point and high leakage currents. Increases of junction leakage currents and decreases of base-emitter forward voltage are the most obvious operating parameter effects for bipolar devices. Leakage current has an exponential temperature dependence and is the parameter which most obviously requires attention at high temperatures, and leakage current compensation techniques become particularly important in high temperature bipolar circuit design.

4.3.1 Junction-isolated bipolar transistor

Junction-isolated (JI) bipolar transistors are the most commonly used bipolar transistors. The device cross sections of *npn* transistor and lateral *pnp* transistor are shown in Figure 4.1. For *npn*, the substrate current I_{SUB} passes from the collector to the substrate; and for *pnp*, it leaks from the base to the substrate. As shown in Figure 4.1, I_{CBO} is the leakage current between collector and base junction. The measurement results of leakage currents I_{SUB} and I_{CBO} for standard geometry *npn* transistor are shown in Figure 4.2. Thus, substrate current I_{SUB} cannot be ignored over 200°C because it becomes more than a few micro amps; I_{CBO} is also a concern if the operating current level is low.

It is possible to cancel the effect of the substrate leakage current by using a bypassing diode. The concept is shown in Figure 4.3 for the case of the *npn* transistor. This compensation is done by connecting the diode (whose reverse-biased leakage current is equal to the substrate current of the compensated transistor) at the collector of the compensated transistor. Consequently, the substrate current is bypassed and is not added to the collector current of the compensated transistor I_C. Also, since the leakage current of the bypassing diode depends little on reverse-bias voltage, it is sufficient for the compensation diode to be made similarly to the *pn* junction between the collector and the substrate.

I_{CBO} is the leakage current which appears at the base-collector junction and flows in the direction opposite normal base current. It mainly causes difficulty on the side of the base whose current level is relatively low. When the I_{CBO} becomes larger than the transistor intrinsic base current I_B, an additional current is required to compensate for the reversal in



npn transistor

pnp transistor

Figure 4.1. Structure of *npn* transistor and *pnp* transistor.

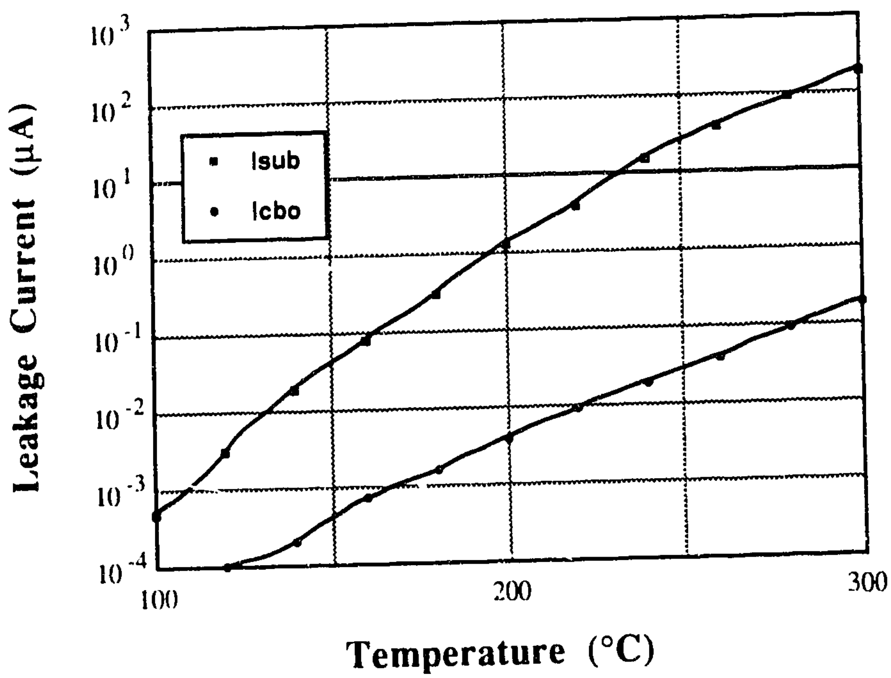


Figure 4.2. Isub and Icbo vs. temperature

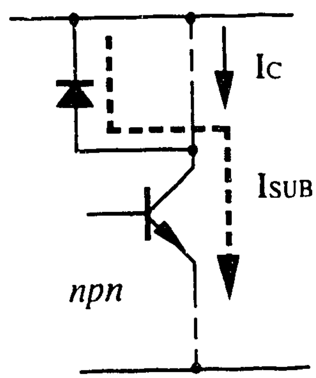


Figure 4.3. Bypassing collector-substrate leakage compensation

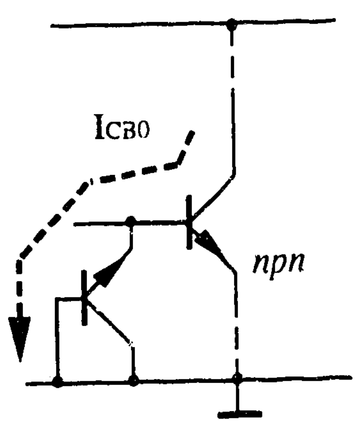


Figure 4.4. Bypassing ICBO from the base

the direction of base current flow. For this, a reverse-biased diode bypassing I_{CBO} is applied to the base of the compensated transistor. Generally, the base-collector junction can be used for this purpose. However, it is overcompensated for the junction-isolated IC because substrate current I_{SUB} (which is much large than I_{CBO}) appears from the collector. Accordingly, I_{CBO} can be compensated by the emitter-base junction as shown in Figure 4.4. While the leakage current of the reverse-based base-emitter junction is not directly a match for I_{CBO} in this case, it is possible to match the forementioned currents by scaling the emitter area.

4.3.2 Dielectrically isolated complementary vertical bipolar transistor

Dielectrically isolated devices have superior electrical isolation which is obtained by surrounding each *n*- type pocket or tub not with a reverse-biased *p-n* junction, but with a dielectric layer. Normally, thermally grown SiO_2 is used as the dielectric material.

Dielectric isolation (DI) eliminates isolation leakage and the possibility of latch-up (four layer *pnpn* parasitic transistor action), two of the major high temperature sources of circuit failure which are present in junction isolated processes. The complementary vertical *pnp* offers superior AC and DC characteristics compared to a lateral *pnp* allowing simpler stabilization methods. The junctions are relatively deep (>3μ) to minimize sensitivity to interconnect pitting [3,18]. Device cross sections are shown in Figure 4.5.

Characterization of the *npn* and *pnp* show them to be quite suitable for use up to 300°C, however certain parameters change drastically over the temperature range and require special consideration in a high temperature design. I_{CES} is the leakage current between collector and emitter junction. Leakage currents increase to micro amps as shown in Figure 4.6 [3]. An important point illustrated in the figure is the fact that I_{CES} is several times larger than I_{CBO}. Significant, but not shown on the figure, is the fact that the leakage

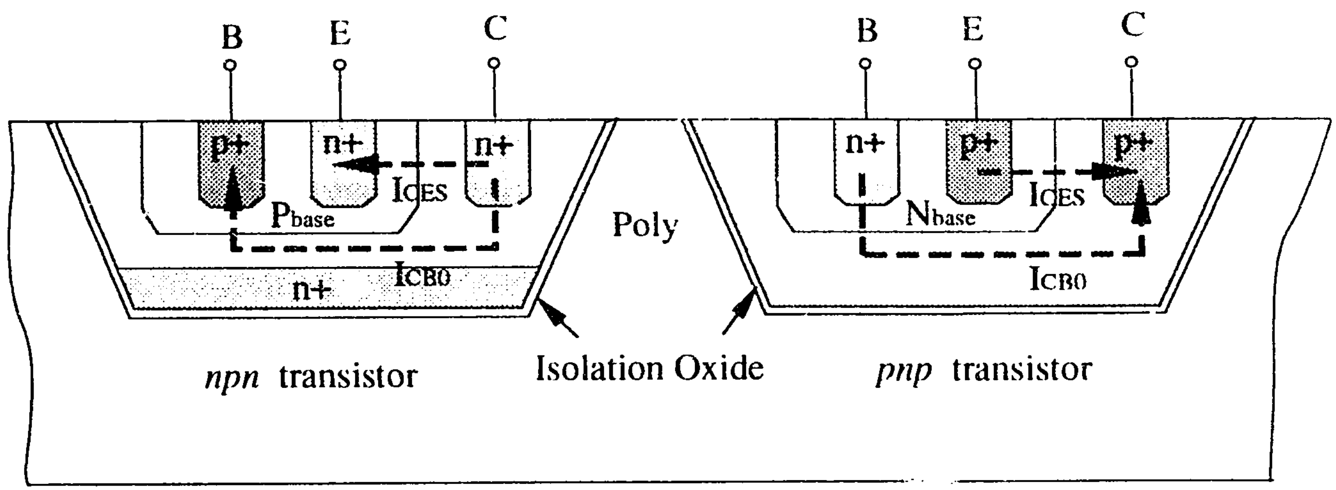


Figure 4.5. Cross sections of *npn* transistor and *pnp* transistor.

page 84 has been removed due to copyright restrictions. The information removed was Figure 4.6 Leakage current vs. temperature [3].

currents for the matched devices on the same chip typically match to 10%. These characteristics are exploited in the circuit design.

Another potential source of failure, parasitic MOS formation, is eliminated by isolation of each device in its own dielectrically isolated island. This eliminates the isolation diffusion which can act as drain for parasitic pMOS in junction isolated circuits.

As shown in Figure 4.7, I_{CB0} can be compensated by connecting another transistor to bypass the current from the base, which is very sensitive to leakage current. In Figure 4.7a, R_1 and R_2 provide most of the collector base voltage for Q_1 and Q_2 whose I_{CB0}'s cancel those of Q_3 and Q_4 to within the limits of their match. In high-temperature bias circuits, I_{CB0}s are often compensated by the source of I_{CES} which seems to be a minimum of three times I_{CB0} at 300°C. The leakage current compensation networks are shown in Figure 4.7b, in which the bottom current source is set by Q_1 and R_1. Emitter follower Q_4 supplies the base drive requirements of Q_1, Q_2 and Q_3 until the base currents reverse at high temperature. Then they are supplied by Q_5's I_{CES} whose excess is then supplied by the emitter follower. This excess flowing through R_4 and Q_4 provides some collector to base voltage for Q_1. The same considerations apply to the top line current source which is set up by *pnp* transistors.

4.4 Compensation for V_{BE} and V_Z

Most designers are familiar with the -2mV/°C temperature coefficient of the base-emitter voltage V_{BE} of a transistor biased into an active region. The exact value also depends on I_E and V_{CB}, but it is very reproducible for a given device. The dependence of V_{BE} on temperature is shown in Figure 4.8. At 300°C, V_{BE} at typical current densities is only 50 to 100mV. A compensation resistor is usually connected to a transistor's emitter to

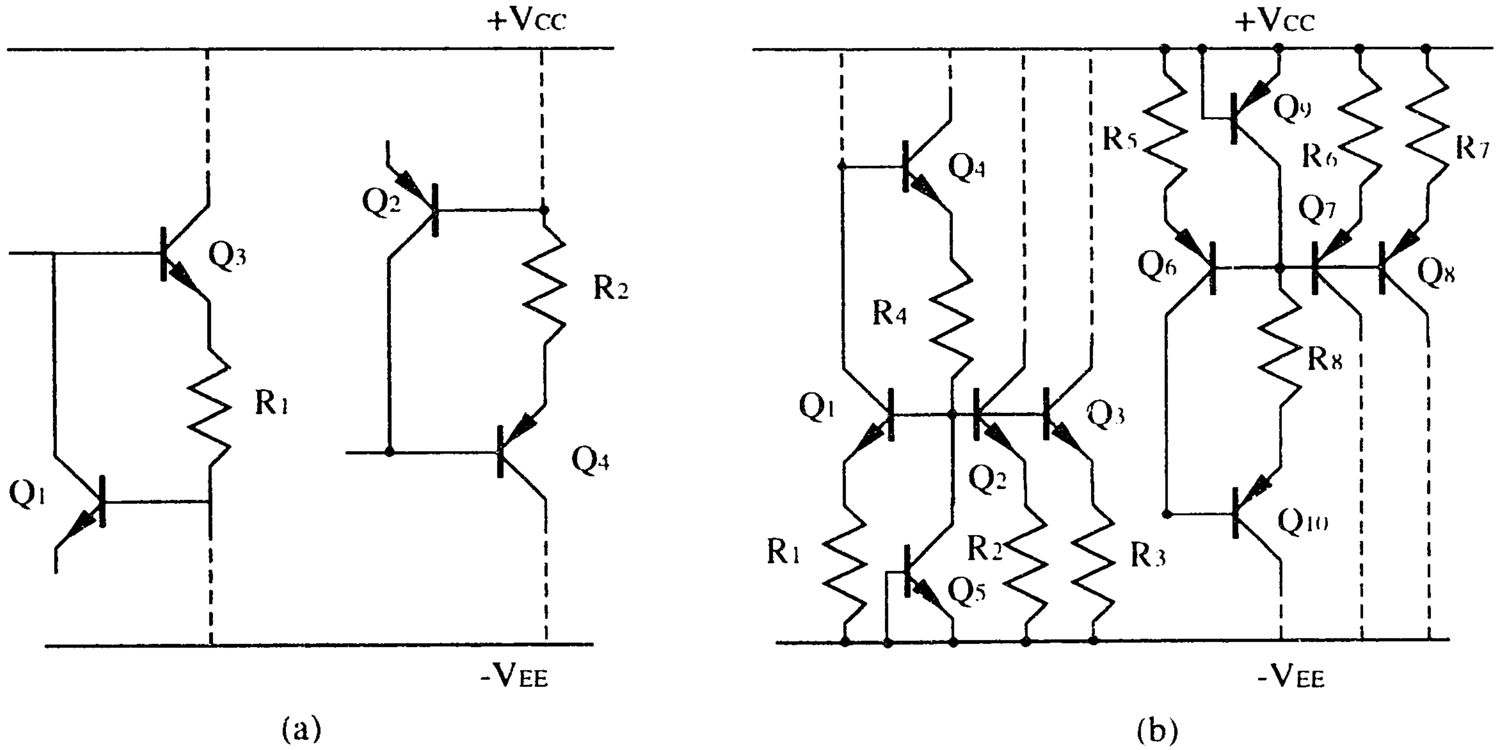


Figure 4.7. Leakage current compensation networks

page 87 has been removed due to copyright restrictions. The information removed was Figure 4.8 Temperature dependence of V_{BE} [3].

compensate the voltage drop of V_{BE}. The connections can be seen in Figure 4.7b, which ensure that the voltage across Q_5's base and emitter won't be too low at high temperature.

The Zener diode voltage V_Z increases at the rate of about 2.5 mV/°C where an emitter-base junction which has a Zener voltage of about 6V is used. Often, V_Z and V_{BE} are used as reference voltage in analog IC; and in this case, the temperature dependence is a problem. A Zener diode is usually connected with a diode to compensate its positive temperature coefficient.

4.5 Current Gain h_{FE} and Saturation Voltage V_{CE}

The favored type of bipolar transistor for ICs is the *npn* transistor, for two basic reasons: 1) The electron mobility in silicon is about 2.5 times higher than the hole mobility, so the base transit time will generally be shorter in *npn* transistors than in *pnp* transistors. This will lead to a somewhat higher current gain and to improved high-frequency performance for the *npn* transistors. 2) As a result of the higher solubility of the donor dopants, phosphorous and arsenic, compared to boron, a more efficient emitter-base structure can be obtained in the case of an *npn* transistor than in the *pnp* case, thus leading to a higher current gain.

For many applications, however, *pnp* transistors are needed at various places in the circuit. The large base width of the *pnp* transistor results in a long emitter-to-collector transit time for the holes traveling across the base region, which in turn produces a low value for the current gain and a poor high-frequency response with f_T values in the range compared to the *npn* transistor. Table 4.3 summarizes the characteristics of IC *npn* and *pnp* transistors. It is possible to produce IC *pnp* transistors with characteristics that are comparable to those of *npn* transistors. These higher-performance *pnp* transistors will, however, require extra processing steps beyond those required for *npn* transistors, and so

Transistor type	Current gain, ß	f_T (MHz)	BV_{EBO} (V)	BV_{CBO}(V)
npn	~ 50 - 200	~ 500	~ 6 - 8	~ 50
Vertical *pnp*	~ 5 - 30	~ 10 - 30	~ 50	~ 50
Lateral *pnp*	~ 5 - 20	~ 1 - 10	~ 50	~ 50

Table 4.3 Typical IC bipolar transistoı parameter values

add to cost of the IC.

Unfortunately most of these characteristics are temperature dependent, especially for *pnp* transistors which have low current gain and inherently slow (low f_T), the effects to the high-temperature circuits would be very significant. The DC current gain h_{FE} changes nonlinearly over wide range of temperatures, and also depends on the collector current, I_C. The typical saturation voltage increases at the rate about 0.3 %/°C. Figure 4.9 shows the characteristics of lateral *pnp* transistors (Ferranti Interdesign, Inc.) over -55°C to 125°C.

4.6 Variation in Characteristics of Diffused Resistor

A diffused resistor structure is formed by the bulk resistance of a diffused semiconductor region. In forming a monolithic resistor, either of the two basic diffusion cycles, that is, the base or the emitter diffusion, can be utilized. The *p*- type diffused resistor obtained using the base diffusion cycle of the *npn* transistor, is the most commonly used resistor structure.

The resistance of a diffused resistor increases linearly with temperature, and at 300°C it becomes about two times larger than at room temperature. Hence, the leakage current of the diffused resistor must be taken into account. Leakage currents in Figure 4.10 are classified according to the following:

I_{NSUB} : *n* -type region to substrate; and

I_{NP} : *n* -type region to resistor (*p* -type diffused base).

The magnitude of leakage current is inversely proportional to impurity concentration and proportional to junction area. In general, impurity concentration of a *p* -type diffused base region is slightly greater than that of a substrate, and the junction area between the substrate and the *n* -type region is larger than that of the *p* -type diffused base and the n-type region by a few times or a few tens of times.

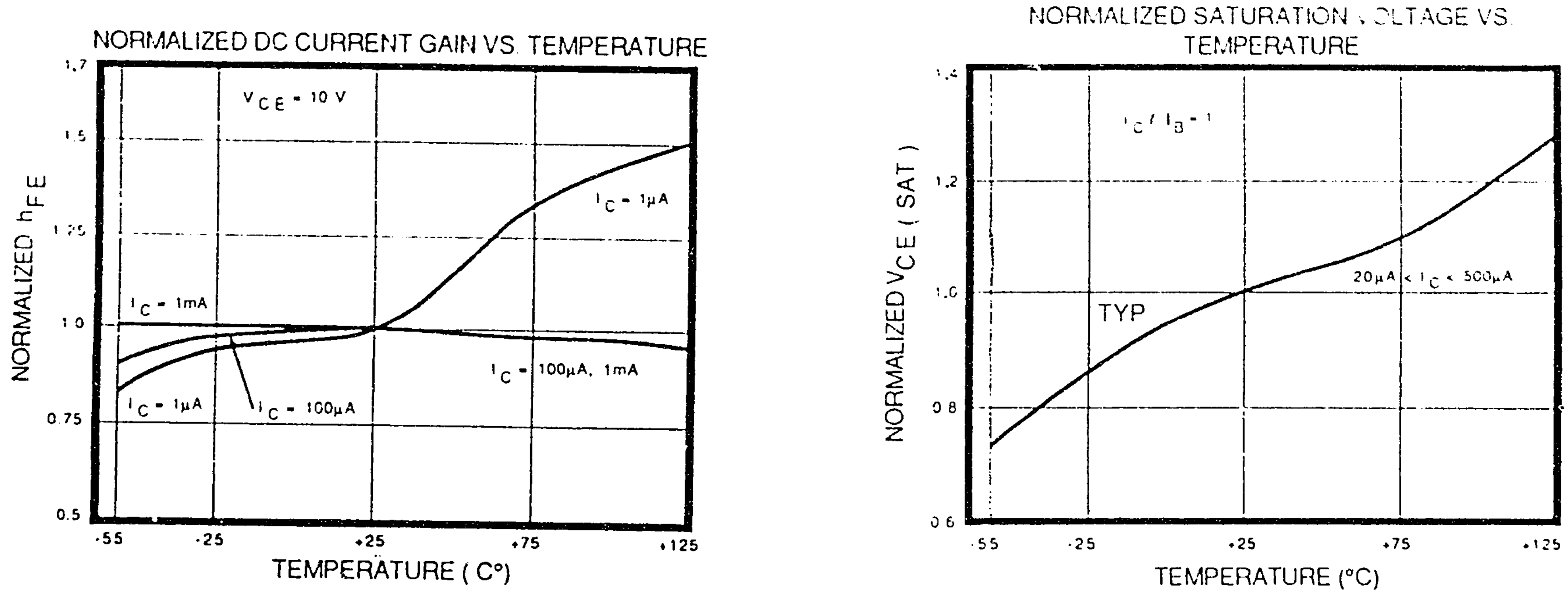


Figure 4.9 Temperature versus h_{FE} and V_{CE}

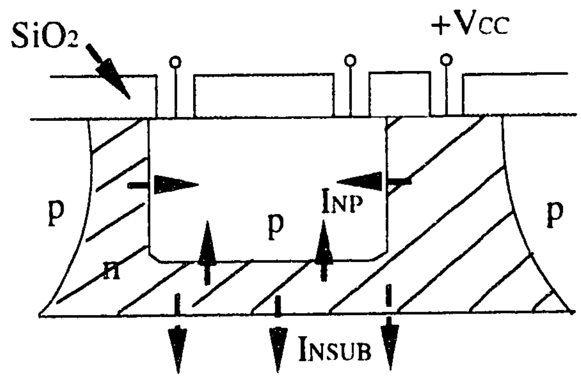


Figure 4.10. Leakage currents of diffused resistor

Thus, compared with I_{NSUB}, I_{NP} takes a very small value and can be ignored. As for I_{NSUB}, if the resistor structure is as shown in Figure 4.10, there is no problem concerning utility. This is because, in this case, I_{NSUB} passes from positive supply V_{CC} to the substrate and it has no effect on the current passing through the resistor. (However, when the resistor has a structure whereby the *n* -type (surrounding the resistor) is not connected to V_{CC}, I_{NSUB} is isolated from the *p* -type diffused base itself, thereby causing a problem).Then I_{NP} is almost equivalent to I_{CBO} and the effect is negligible in that, in general, only a few tens of micro amps current is used. Therefore, the problem of the resistor concerns only the temperature dependence of resistance. Figure 4.11 shows the normalized diffused base resistor temperature dependence. Its linearity over the full operating temperature range and positive temperature coefficient are exploited in several areas of the circuit design.

4.7 Compensation of Biasing Current Source

In chapter 4.3.2, circuit compensation techniques based on dielectrically isolated devices has been introduced (Figure 4.7). Here, more about circuit compensation of junction isolated transistors will be discussed as well.

4.7.1 Problems of biasing current source

Figure 4.12a is a basic current mirror using two JI transistor in this circuit, there is a problem in that the output current increase at high temperature. This is considered to be due to the following.

(1) On the side of the output the emitter current increase by the discrepancy in the I_C-V_{BE} characteristic with temperature caused by the difference of V_{BC} between the input transistor and the output transistor .

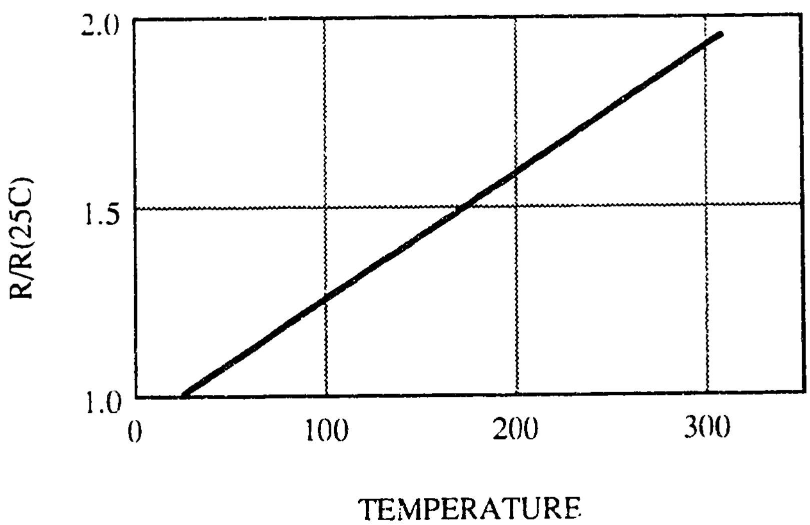
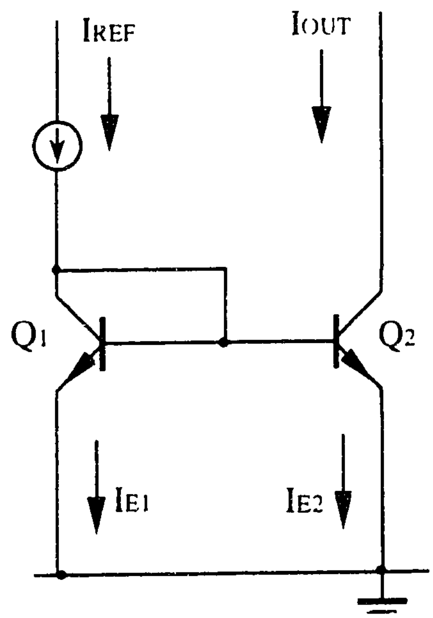
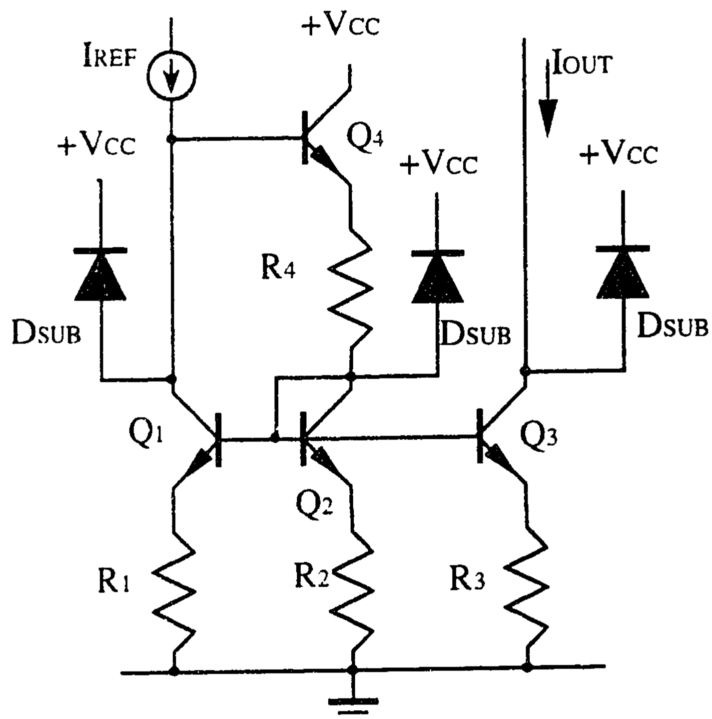


Figure 4.11. Normalized base resistor temperature dependence.



(a) Normal current mirror circuit



(b) Current mirror which works at high temperature

Figure 4.12. Current mirror circuits

(2) Substrate current is added to the collector current of the output transistor. At high temperature there is a great difference in the emitter current according to such conditions even if V_{BE} is identical.

4.7.2 High temperature current mirror circuit

Figure 12b shows the proposed current mirror of JI transistors able to operate at high temperature. It is based on Wilson's current mirror.

First, to cope with the forementioned problem (1), this circuit is constructed so that the base-collector junction of input transistor Q_1 as well as the output side Q_3 is reverse-biased.

Second, the problem (2) uses the compensation method for substrate current (b). It is the diode D_{SUB} that is bypassing the substrate current in Figure 4.12b. As for resistors R_1 to R_4, the accuracy of the absolute value is not important (but in R_1 to R_3, it is required that R_1=R_2=R_3). Thus the temperature dependence of these resistors is not taken into consideration.

4.8 Voltage references

There are two common types of voltage reference: bandgap and buried zener. Both make good stable references, and each has particular strengths and weaknesses which are compared as following:

Bandgap:	•Low Reference Voltage	•Low Quiescent Power
Buried Zener:	•Low Noise	•Good Long-Term Stability

Bandgap references make use of the bandgap voltage of silicon: 1.205V. Properly designed bandgap references compensate PTAT and CTAT ("Proportional to Absolute Temperature" and "Complimentary to Absolute Temperature") voltages to obtain a stable output near this value. Other voltages may be obtained by using this as the input to a precision amplifier with suitable gain.

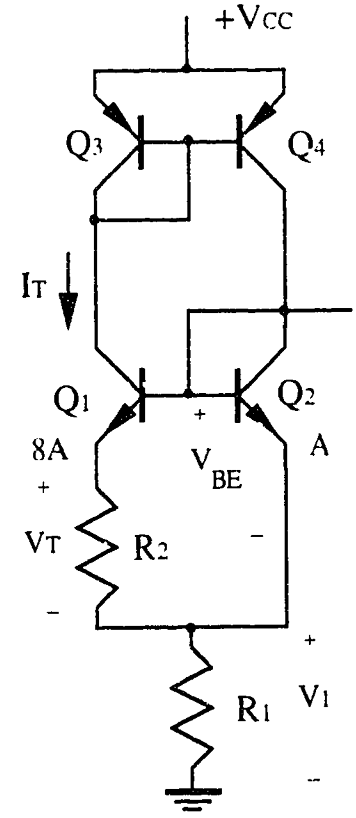
Buried zener diodes are zener diodes fabricated beneath the surface of a chip is prone to contamination and lattice dislocations and zener diodes at the surface are more noisy and less stable than "buried" ones. Buried zener diodes may be made with a range of voltages, they all have good low noise performance (better than bandgap references) but ones which, in combination with their temperature compensating diodes, have a breakdown voltage just below 7V have the best temperature performance, with high initial accuracy and low drift.

4.8.1 Bandgap-reference regulator

If the emitter current is made proportional to temperature, the V_{BE} temperature coefficient is nearly constant over a relatively wide temperature range (-55°C to +150°C) [17,18]. If V_{BE} for several devices were plotted as a function of temperature and extrapolated towards absolute zero (-273°C), the straight lines would have differing slopes but would intersect at the same value of voltage: 1.205V, the "bandgap voltage of silicon, extrapolated to zero", which can be generated as constant voltage by compensating V_{BE}'s decreasing, as shown in the circuits of Figure 4.13. The difference between the V_{BE}'s of two identical transistors, operating at a constant collector-current ratio, r, is PTAT (proportional to absolute temperature), since

$$V_T = \frac{KT}{q} \ln \left(\frac{r\,I}{I_{ceo}}\right) - \frac{KT}{q} \ln \left(\frac{I}{I_{ceo}}\right) = \frac{KT}{q} \ln r \qquad (4.1)$$

where k/q (the ratio of Boltzmann's constant to the charge of an electron) is about 86.2μV/K, I_{ceo} is the same for both transistors, and T is the absolute temperature of both transistors.



$$V_{out} = V_{BE} + V_1$$

$$= V_{BE} + 2\frac{R_1}{R_2}V_T$$

$$= V_{BE} + 2\frac{R_1}{R_2}\frac{KT}{q}\ln r$$

$$= 1.205\ \mathrm{V}$$

Figure 4.13. Basic bandgap-reference regulator circuit

In the circuit of Figure 4.13, Q_2 is made up of eight transistors that are identical to Q_1, connected in parallel. Therefore, the current density in Q_1 is 8 times that of Q_2, so we know that r=8 for this circuit. I_T is equal to the current across R_2, which is V_T/R_2. The total current flowing through R_1 is twice the current through R, since the currents in the two branches are equal. Therefore,

$$V_{out} = V_{BE} + V_1 = V_{BE} + 2\frac{R_1}{R_2}V_T = V_{BE} + 2\frac{R_1}{R_2}\frac{KT}{q}\ln 8 \qquad (4.2)$$

The ratio, R_1/R_2, is the value necessary for V_{out} = 1.205V. This voltage is very stable around room temperature but not at high temperature (>200°C) due to V_{BE}'s nonlinearity.

4.8.2 Voltage reference circuit works at high temperature

One circuit frequently used as a source of temperature stabilized bias current is shown in Figure 4.14a. The output current is given by:

$$I_{out} = \frac{V_{ZEN} + (n_1 - n_2 - 2)V_D}{R} \qquad (4.3)$$

where V_{ZEN} is the Zener diode voltage, and V_D is the diode voltage drop. Using Eq.4.3 and minimizing the temperature coefficient $\partial I_{out}/\partial T$ of I_{out}, we find the required numbers n_1 and n_2 of the diodes, and the value of the resistor, R. Eq 4.3 assumes that the collector currents of Q_4 and Q_5 are equal. Yet, due to the deference between the collector-base voltages of Q_4 and Q_5, their collector currents are different. At low and moderately elevated temperatures, this difference is small. At high temperatures, however (above 200°C), this difference becomes very large. It can be reduced by increasing the collector-base voltage of Q_4. However, the circuit of Figure 4.14a does not allow the designer to introduce the required modification.

This drawback is eliminated using the circuit of Figure 4.14b. The output current

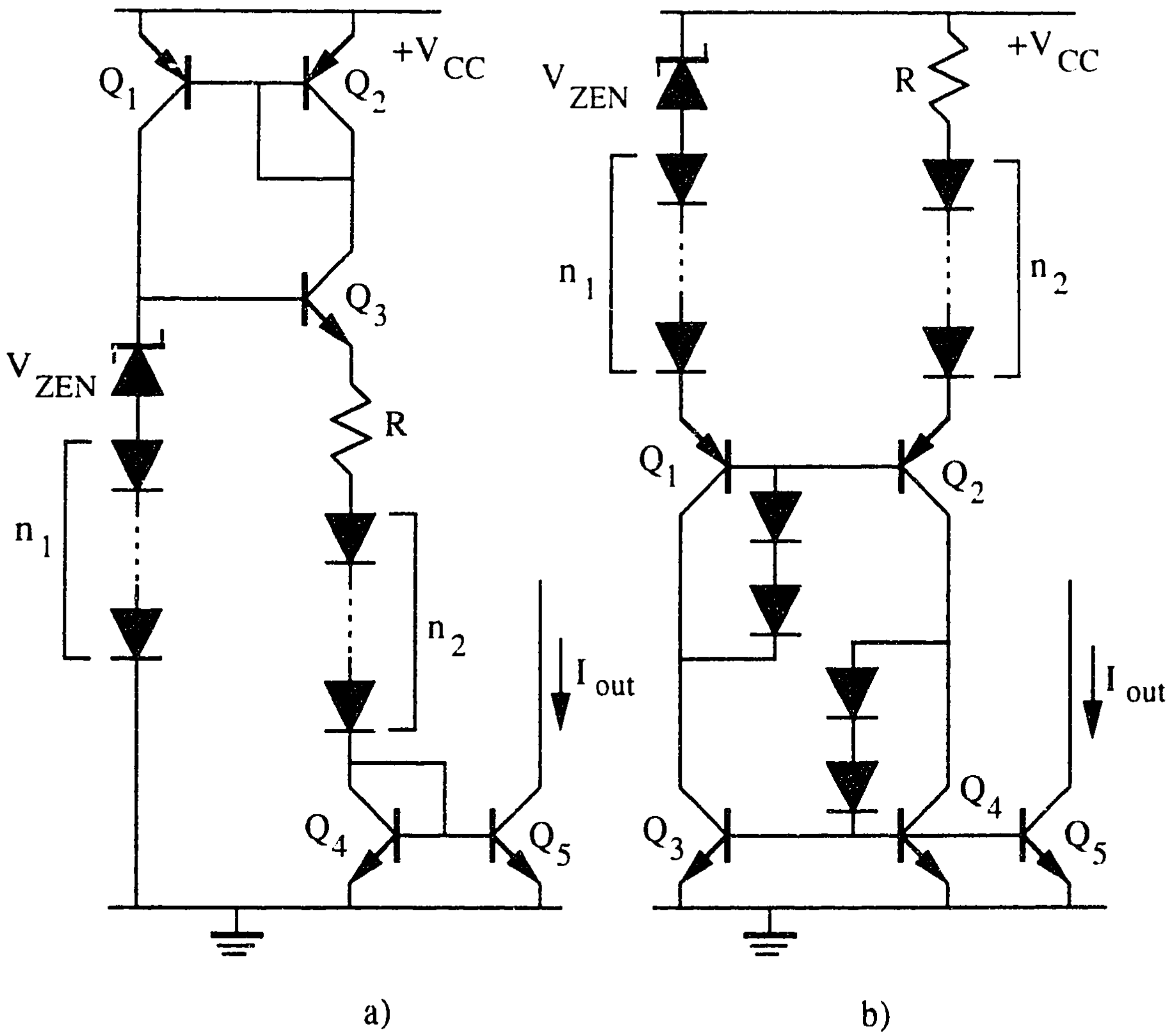


Figure 4.14 High temperature voltage reference circuit

is given by:

$$I_{out}=\frac{V_{ZEN}+(n_1-n_2)V_D}{R} \tag{4.4}$$

which is very similar to Eq.4.3. variables n_1, n_2, and R can be chosen in the same way as in the circuit of Figure 4.14a. Yet , the circuit of Figure 4.14b has one essential advantage: Q_4's collector-base potential can be increased with a two diode circuit, as shown. This simple modification drastically decreases the difference between Q_4 and Q_5's collector currents at high temperatures. Appropriate diodes are also added to increase the base-collector voltage of Q_1 to ensure the circuit operates under high temperature condition.

4.9 Conclusion

To realize a VFC for use at high ambient temperature, compensation methods considering the problems of the devices are very critical. It is proved that the analog integrated circuits using dielectrically isolated or junction-isolated silicon bipolar process can extent the functional temperature range significantly if the compensation techniques are applied properly.

Future problems include applying these compensation methods to the VFC circuit design and implementing all the building blocks into a single chip. Further study on the influence on VFC parameters by compensation will be very important for high temperature VFC design as well.

5 ANALOG ASIC DESIGN AND SIMULATION

5.1 Analog ASIC technologies

An analog ASIC can take on many different forms. There are component arrays, tile arrays, standard cells, and fully custom ICs. The last three forms are for large production volumes (at least more than 1000 units), the development cycles are long, and relatively high initial development cost. Component arrays are suggested for a small circuitry design and development.

Component arrays are the original analog semicustom ICs. They are prefabricated arrays of transistors, resistors, and in some cases capacitors and other specialized components. These components are arranged and spaced on the IC to facilitate the routing of metal interconnections and the implementation of integrated circuitry. Many of the older arrays have a more or less random placement of components and a single layer of metal that can make the layout of high-performance differential circuitry difficult. The more up-to-date component arrays have component groupings which are more amenable to modern design techniques. The amount of circuitry that can be integrated on the chip is limited by the number of components on the chip and the achievable layout efficiency for the circuitry being integrated. The amount of circuitry that can be integrated per unit of die area will typically be lower on this type of array than any other. The major disadvantages of this implementation are the relatively low level of achievable integration and the relatively high unit price.

Major analog ASIC vendors are as fellows: AT&T Microelectronics, Cherry Semiconductor, CLASIC (National Semiconductor), Extra Corporation, GENNUM Corporation, Plessey, Micro Linear and Raytheon.

Table 5.1 lists many of the component arrays offerings from major analog ASIC vendors. It is important to realize that new products are continuously being developed and

Vendor	Product	Process (V)	Total *npn*	Large *npn*	Lateral *pnp*	Vertical *pnp*	JFET	Bonding pads
Cherry								
	3600	20	123	6	52			25
	4000M	20	153	8	52	4		28
	7600	15	142	4	26			25
Exar								
	M-100	20	149	12	52	4		28
	W-100	36	212	4	60	14	8	40
GENNUM								
	LA251	20	152	4	49			40
	LA252	20	116	4	34			32
Plessey								
	MOM	20	149	12	52	4		28
	MON	20	182	12	64	6		40
Raytheon								
	RLA120	32	39	4	16			24
	RLA160	32	43	4	10			44

Table 5.1 Component arrays

many not be reflected in this table. This information is just a reference for the majority of the available component arrays offered by each vendor.

5.2 Analog IC CAD Tools

The CAD tools for Digital Gate Arrays have been available in many forms for many years. It is only recently that effective, user friendly CAD support has been developed that is suitable for Analog products. The availability of these new design tools in part contributed to the concept of Analog Semi-Custom Arrays utilizing the Macrocell concept.

As circuit integration increases, building hardware breadboards for circuit simulation is becoming less and less representative of final performance. This situation has led engineers to use simulation programs to create software breadboards allowing them to perform various circuits analysis.

Also, with the widespread use of workstations such as IBM PC, MENTOR, ANALOG WORKBENCH etc..., system designers have the opportunity to easily design analog ICs with a library of predesigned circuit blocks available such as Op-amps, regulators, comparators...

Taking advantage of the repeated cell structure common to all arrays and using the fully characterized library of micros and macros , the CAD tools provide schematic capture and simulation capabilities and are a substantial help for the designer. Computer analysis can be used to optimize performances and improve the yield. It can also spot subtle mistakes and effects that might remain unnoticed an a breadboard and all the way to integration.

A library of computer models of all active components on the gridded arrays, including the effects of the parasitic elements inherent in monolithic ICs, has been developed at Ferranti Integration.

5.3 CAD Support

There are three major ways in which the Macrochip gridded arrays are supported in the area of schematic capture, circuit simulation, and graphic displays. All are based on the use of Berkeley SPICE for simulation and coupled with a variety of pre- and post-processing to improve user interface capability. The three areas which are supported include:

•Main-frame capture and simulation for either time share or in house system (SPICE-HSPICE on the VAX).

• Analog Workbench on Sun, Apollo, or IBM/PC Computer Systems.

• IBM XT/AT with Futurenet and PSPICE.

All active components on the Macrochip gridded arrays are described by Basic and Full device models and symbols which represent the process and device geometries available. All micros and macros are fully supported by a library containing the schematic capture and instrument packages allowing the end user to run his own circuit simulation and develop customized designs.

5.4 Software

As we have already mentioned, all circuit simulations are based on the use of SPICE (AWB, VAX) and its derivatives PSPICE (IBM XT/AT) and HSPICE (VAX).

SPICE (from UC Berkeley) is a general purpose simulation program designed to perform various analysis of circuit containing independent sources, linear and non-linear devices.

5.5 The Analog Work Bench

The circuits were simulated on Analog Work Bench. Analog Work Bench as an integrated CAD tool provides extremely flexible analysis capability for the library of micro and macro circuits available on the gridded array Macrochips. This library includes complete device symbols, SPICE parameters, micro and macro schematics, function generator and instrument set-ups to allow the user to quickly capture, simulate, modify, interconnect, or generate new IC functions. Some of the analysis features provided by the total software package include:

- Time domain analysis using Waveform Generator and Oscilloscope
- Frequency domain analysis using Frequency Sweeper and Network Analyzer
- Parametric plots with two variables
- Analysis of effects of component tolerances, temperature, etc.
- Statistical analysis, distributions, Monte Carlo analysis
- Generation of sub-circuit blocks
- Spectrum analysis using F.F.T.

5.6 Models

A library of symbols is provided for the analog gridded arrays for specific utilization with the Analog Workbench. These symbols correspond to integrated components, and every active device in the family is provided with a substrate connection. There are two different models for the active devices:

•The basic models are simple first level models which provide a fairly good description of the devices electronic behavior under standard conditions. It is recommended that they not be used in the saturation region.

•The full models are more sophisticated and use subcircuits in order to model all the parasitic effects describing the electronic behavior of the active devices. They should be used for any accurate study of a circuit.

Here the library of SPICE models provided by Ferranti Interdesign:

TYPE:	NAME:
Basic 1X NPN	MM01NB
Full 1X NPN	MM01NF

Basic 2X NPN	MM02NB
Full 2X NPN	MM02NF
Basic PNP	MM02PB
Full PNP	MM02PF

The basic and full models are shown in Figure 5.1. Macrochip transistor performances can be found in Appendix A.

5.7 Analog IC Design Hints

Integrated design approaches are strongly influenced by the following facts:

- Active components are less expensive than passive components.
- Components that match or ratio are readily available.
- Components have wide absolute value tolerances.
- Manufacturing technologies are not easily intermixed.
- Design changes are expensive and time-consuming.
- Inductors and large-value capacitors are not available.
- Large currents and high power dissipation are hard to deal with.

Integrated design focusses on current-source biasing, component ratios, and matching. Multiple technologies, inductors, and large-value capacitors are impractical on a single chip. Power dissipation is a problem and is kept to a minimum. Component substitution and "tweaking" are impractical in an integrated design. Every possible effect must be made to ensure first-time design success. Integrated design makes heavy use of circuit simulation wi[illegible]s and breadboards. It is important to realize the circuit in a way that maximizes th[illegible] integrated design and downplays its limitations.

- Use a modularized ap[illegible]e design. This is especially true on more complex circuits. Common circuit blo[illegible] minimize design and simulation efforts and improve the chances of first-time success.

page 108 has been removed due to copyright restrictions. The information removed was Figure 5.1 Basic and full transistor models [10].

• Minimise the use of passive components. One of the major strengths of integrated design is the availability of large number of active devices.

• Avoid dependence on absolute values. The absolute values of integrated resistors found on semicustom arrays vary by a significant amount. Matching, ratioing, and thermal tracking are inherent strengths of integrated design. Reliance on absolute values can be disastrous.

• Avoid using *pnp* transistors as switches. *Pnp* transistors are inherently slow. For high-speed circuits, *npn* transistors are better switches than *pnp* transistors.

5.8 Breadboarding Hints

A carefully and thoughtfully constructed breadboard can produce a true representation of the circuit for evaluation. It can confirm a design's integrity or reveal faults in part of the design. To facilitate breadboarding effort and ensure accurate results of a breadboard, here some hints:

• All substrate pins on the device kit parts must be tied to the most negative potential on the breadboard.

• Measure a breadboard's substrate current value and make sure it is not large enough to cause parasitic conduction.

• For debugging purpose, it is easier to evaluate individual circuit blocks first before evaluating the combined system performance.

• Keep in mind that the result will vary due to the normal process variations.

• For high frequency or high speed circuits, one should beware of stray capacitance effects associated with the breadboard.

6 MEASUREMENT

6.1 Experimental Verification

The most important portion of the theory deals with improvement of the frequency range, linearity and temperature stability of VFC circuits. How well are the current-source biasing, component ratios, matching, and etc. The test results presented in this chapter focus on the characteristics of linearity and temperature stability due to the change of circuit structures. The behavior, with temperature, of maximum frequency and waveforms are primary interest. Of course, the general characteristics of the VFC, such as the power dissipation, are also measured, but these aspects are not emphasized. The precision VFC was breadboarded using the MM macrochips transistor arrays from Ferranti Interdesign [10], and SPICE simulation was run on Analog Work Bench.

6.2 Breadboard Verification

First, the basic multivibrator shown in Figure 3.11 was breadboarded and the voltage-to-current converter, current switches delay, actual threshold voltage of the circuit were test and measured. Table 6.1 shows the device values used in the circuit. The circuit supply has to be exactly 12V. When the frequency goes up more than 10KHz, the output waveform starts to distort and linearity degrades dramatically. The circuit provides nonlinearity less than 1% from 10-10kHz and exhibits a temperature stability of around 200ppm/°C. The output frequency is power supply dependent, because the thresholds was set by the resistors and reference current source, which varies when changing power supply voltage.

The modified circuit shown in Figure 3.12 was breadboarded after that, and much higher performance specifications are achieved due to the changes. The modified circuit is still very simple but with much better linearity and temperature stability, which is a very good circuit as a voltage-to-frequency converter building block. The parameters of the

R3	900 Ω	R2	6.7 KΩ
R3	3.6 KΩ	R4	3.6 KΩ
R5	300 Ω	R6	600 Ω
R7	30 KΩ	R8	8.1 KΩ
R9	2.7 KΩ	R10	2.7 KΩ
R_T	2 KΩ	C_T	10 nF

Table 6.1 Circuit parameters for the basic multivibrator

devices are listed in Table 6.2. The circuit is designed to be power supply independent, it can operate with $V_{CC} \geq 12V$. The linearity of the circuit is improved, the conversion error is about 0.5%. But the temperature stability was not tested through the oven but the SPICE simulation. The temperature coefficient is less than 100 ppm/°C.

To test the accuracy and temperature performance of the precision VFC, the more complicated circuit was constructed using MM macrochips transistor arrays available from Ferranti Interdesign. Discrete resistors and capacitors were used to allow increased flexibility in the experimental conditions. The device parameters for the experiment circuit (shown in Figure 3.20) are found in Table 6.3. The circuit is designed to operate with $V_{CC} \geq 15V$. $\Delta V_{TH} = 2V$. The circuit has very stable performance, but parasitic capacitance is introduced from the breadboard, which degrades the output linearity and temperature stability. The circuit board was tested over -25°C to 75°C temperature range. The test show that the temperature coefficient of the output frequency is less than 60 ppm/°C.

6.3 SPICE Simulation on Analog Work Bench

Breadboarding is a suitable investigative tool only at low frequencies and temperatures. The use of discrete devices and the plug-in type breadboard results in excessive parasitic capacitances which degrade the frequency performance. To provide a clearer picture of the obtainable performance, SPICE simulations on Analog Work Bench were used to evaluate high frequency operation.

The circuit design was verified using SPICE simulation program. The simulation results for $C_T = 5nF$ and $R_T = 3k\Omega$ are shown in Figure 6.1. They are compared with the calculated results obtained from Eq.3.18 using $C_T = 5$ nF, R_T $3k\Omega$ and $\Delta V_{TH} = 2V$.

The converter should provide an output square wave whose frequency is directly proportional to an input control voltage. The simulation shows that the converter operates

R11	300 Ω	R4	3.6 KΩ
R5	300 Ω	R6	600 Ω
R7	30 KΩ	R8	8.1 KΩ
R9	2.7 KΩ	R10	2.7 KΩ
R12	6.8 KΩ	R_T	1 KΩ
R_{LOAD}	2.7 KΩ	C_T	2 nF

Table 6.2 Circuit parameter for the modified multivibrator

R1	2 KΩ	R2	2 KΩ
R3	400 Ω	R4	400 Ω
R5	200 Ω	R6	200 Ω
R7	200 Ω	R8	200 Ω
R9	200 Ω	R10	200 Ω
R11	200 Ω	R12	200 Ω
R13	44 KΩ	R14	8.5 KΩ
R15	3.5 KΩ	R16	200 Ω
R17	200 Ω	R18	6 KΩ
R19	3 KΩ	R20	6.3 Ω
R21	10 KΩ	R22	10 KΩ

Table 6.3 The circuit devices of precision VFC (continued on next page)

R23	10 KΩ	R24	200 Ω
R25	200 Ω	R26	200 Ω
R27	200 Ω	R28	3 KΩ
R_{TH}	2 KΩ	C1	47 pF
C2	47 pF	C3	47 pF
C_T	5 nF	R_T	3 KΩ

Table 6.3 The circuit devices of precision VFC (continued from last page)

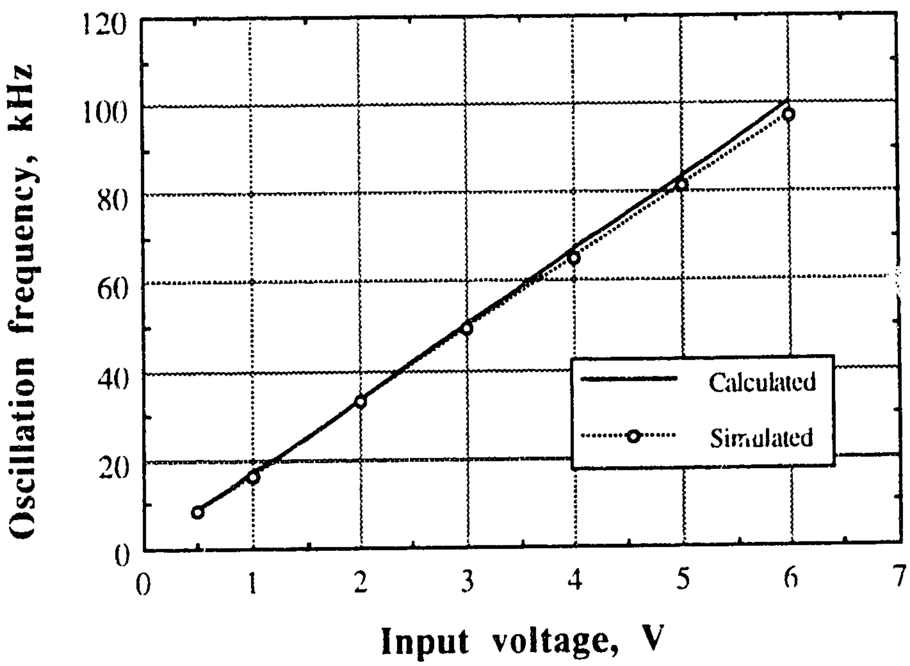


Figure 6.1 SPICE simulated converter characteristic

in the range 100Hz - 100kHz with the deflection from the proportionality law not more than 2% (taking into consideration that all simulation results are below the calculated line).

7 CONCLUSION

The new VFC structure can be adapted for different design purposes. It can be realized as a simple circuit (like the modified multivibrator in Figure 3.12) or a more complicate circuit (the precision voltage to frequency converter in Figure 3.20), in both cases, it shows their high performances. The simplified VFC circuit with modified multivibrator is very suitable for use as a circuit building block in most general data-acquisition systems. The precision VFC is a more complicated and carefully designed circuit, which has the potential to work at high temperature by introducing the high-temperature leakage current compensation.

Using a window comparator with an output voltage swing limiter in the triggering circuit of a current-controlled multivibrator allows the voltage swing on the timing capacitor to equal the difference between threshold voltages. This difference can be done very stable applying the well known design methods for reference current sources and voltage references. The approach gives a low temperature coefficient of the oscillation frequency. Besides, this solution forces to use the window comparator bias switching. This results in a high operation speed of the triggering circuit.

The nonlinearity of the precision multivibrator is a result of the switching delays, the source of these delays is mainly due to the inherent slowness of *pnp* transistors used in the circuits.

The primary achievement of this thesis lies not only in the performance of the two voltage to frequency converters but in the ability to understand the design of various VFC circuits according to the introduced topology. High temperature bipolar circuit design techniques are also introduced in this thesis, which is important for future high-temperature voltage to frequency converter design. The temperature stable bias circuit is the most critical and also most difficult part for high temperature design. The accurate design of the switching point of the threshold circuit is crucial to accurate frequency output. Also, matching components instead of exact-valued components are used in the designs, which will be suitable for semicustom analog ASIC design.

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Appendix 1 Transistor Performance

Transistor Performance

Parameter	Small NPN, 1X, 2X	Medium NPN, 10X	Lateral PNP
Useful Current Range	10nA — 10mA	100nA — 100mA	10nA — 1mA
Current Gain, h_{FE}	80 — 350	80 — 350	30 — 100
Matching of h_{FE}	± 10%	± 10%	± 10%
Offset Voltage	± 5mV maximum	± 4mV maximum	± 5mV maximum
Collector Breakdown Voltage, LV_{CEO}	20V minimum	20V minimum	30V minimum
Collector-Base Leakage	0.1nA maximum	1nA maximum	
Base-Emitter Breakdown, BV_{EBO}	6.65V typical	6.5V typical	
Cutoff Frequency, f_T	400MHz typical	350MHz typical	3MHz typical
Saturation Resistance	10 — 30 ohms	3 — 10 ohms	300 — 900 ohms

Appendix 2 Diffused Rsistor Performance

Diffused Resistor Performance

P Base Diffused Resistor

Resistor Values .... 260 ohms
.... 600 ohms
.... 1.2 Kohms
Resistor Tolerance .... ± 25%
Temperature Coefficient .... + 0.1 %/°C typ.
Matching
Equal (1:1) Ratio .... ± 2%
Non-equal Ratio .... ± 6%

N + Emitter Diffused Resistors

Resistor Values .... 25, 15 ohms
Resistor Tolerance .... ± 25%
Temperature Coefficient .... + 0.08 %/°C typ.

Base Pinch Resistor Performance

Resistor Values . . . . 80K ohms typ.
Resistor Tolerance . . . . +100, −50% max.
Temperature Coefficient . . . . +0.5%/°C typ.
Resistor Breakdown Voltage, End to End . . . . 6.1 — 7.1V
Breakdown Voltage to Substrate . . . . 20V min.

Diode Performance

Forward Voltage . . . . 0.7V typ.
Forward Voltage Matching . . . . ±5mV max.
Temperature Coefficient, Forward . . . . −2mV/°C typ.
Reverse Breakdown Voltage
  Emitter-Base (NPN) . . . . 6.1 — 7.1V
  Emitter-Base (PNP) . . . . 20V min.
Temperature Coefficient, Reverse . . . . +2.3mV/°C typ.