Investigation and Reduction of the Common-Mode Voltage Effects in Transformerless Solar PV Inverters

by

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Abstract

Facing the trend of rapid-growing solar PV capacity, there is an increasing demand for achieving efficient and reliable energy conversion between distributed PV plants and the utility power grid. Varieties of the three-phase transformerless solar PV inverters have been developed to enhance the system's efficiency, reliability, and power density. In such systems, common-mode (CM) leakage current can be produced due to varying common-mode voltage (CMV), which usually requires a CM filter to suppress. Extensive studies have been conducted on reducing the size of CM filters. In particular, the zero CMV (ZCMV) PWM and interleaved PWM are two popular approaches.

The ZCMV PWM is proposed to eliminate the CMV in a multilevel inverter. Despite the reduced linear modulation range, this method has been a popular approach in the literature for PV inverters in both 1000V and 1500V systems. The AC voltage can be low. As such, the reduced linear modulation range is not a big limiting factor for the ZCMV PWM in PV inverter application. However, the CMV cannot be completely eliminated due to the inevitable dead-time. As a result, passive CM filter is still required in a PV inverter. Moreover, the ZCMV PWM results in larger harmonics in the output current. As a result, the practical value of the ZCMV PWM for PV inverter application remains unknown.

On the other hand, modular parallel PV inverter system has been widely employed in practical applications to enhance system lifetime and efficiency. With interleaved PWM, the overall CMV of the system can be further reduced, thus results in smaller CM filters. The key challenge to implement the parallel interleaved inverters is the control of low-frequency (LF)

zero-sequence circulating current (ZSCC) which can be induced by unavoidable hardware parameters mismatch and output power mismatch.

This thesis focuses on addressing the key issues of employing ZCMV PWM and interleaved PWM to reduce the CMV effects in different types of the grid-connected PV inverters. A comprehensive evaluation of the ZCMV PWM is conducted on the transformerless T-type 3L-NPC string PV inverters. In this study, two aspects are explored including dead-time effect and resultant filter volume. Impact of dead-time is thoroughly investigated first, which indicates CMV spikes caused by dead-time are inevitable to ZCMV PWMs. To mitigate the dead-time effects, a cost-effective dead-time mitigation strategy has been proposed by using NP-LCL filters. The analysis indicates NP-LCL has better CM performance than conventional LCL filter, which can be applied to mitigate the dead-time effect without introducing extra passive filtering elements. In order to investigate the actual impact of ZCMV PWM on the total output filter volume, a comparative study has been conducted between the conventional PD PWM and ZCMV PWM methods. The study indicates size of the CM filter can be reduced with ZCMV PWM, but at the cost of two times larger of the DM filter and 1.5 times larger of the total filter volume. Considering the dead-time effect and larger DM filter requirements, ZCMV is less applicable than PD in such applications.

Interleaved PWM, on the other hand, can be applied to reduce the CMV effects in central or multistring PV inverters where modular parallel VSIs are employed. This thesis proposed an MPC-based centralized control scheme to achieve interleaved PWM and elimination of LF-ZSCC. Carriers are adopted to realize interleaving, where the benefits of MPC and interleaved PWM are combined to further enhance the system performances. A generalized ZSCC model is derived, which allows the proposed method to be applied to any number of modular parallel

VSIs. With LF-ZSCC eliminated, the proposed method enables interleaved PWM to be implemented in N paralleled inverter modules for CMV reduction. Compared to the existing MPC-based ZS control schemes, proposed method is more applicable and more flexible, which can be implemented either in a dedicate central controller or in each converter's local controllers. Effectiveness of the proposed method has been verified by MATLAB simulations and lab-scale experiments using paralleled two-level VSI as an example.

Preface

This research was carried out under the supervision of Professor Yunwei (Ryan) Li from the Department of Electrical and Computer Engineering at University of Alberta. Parts of this thesis have been published as IEEE conference and journal publications.

Part of Chapter 2 of this thesis has been published in ECCE2018.

- C. Jiang, Z. Quan and Y. Li, "Passive Filter Design to Mitigate Dead-Time Effects in Three-Level T-Type NPC Transformerless PV Inverters Modulated with Zero CMV PWM," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 6275-6282.

Chapter 3 of this thesis has been presented in ECCE2019 and accepted for publication as a journal paper in IEEE Transaction of Industrial Electronics.

- C. Jiang, Z. Quan, D. Zhou and Y. Li, "Carrier-Based MPC for Interleaved 2L-VSIs with Reduced Low-order Zero-Sequence Circulating Current," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 1474-1481.
- C. Jiang, Z. Quan, D. Zhou, and Y. Li, "A Centralized CB-MPC to Suppress Low-Frequency ZSCC in Modular Parallel Converters," in *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2020.2982111, accepted on Mar 05, 2020.

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List of Abbreviations

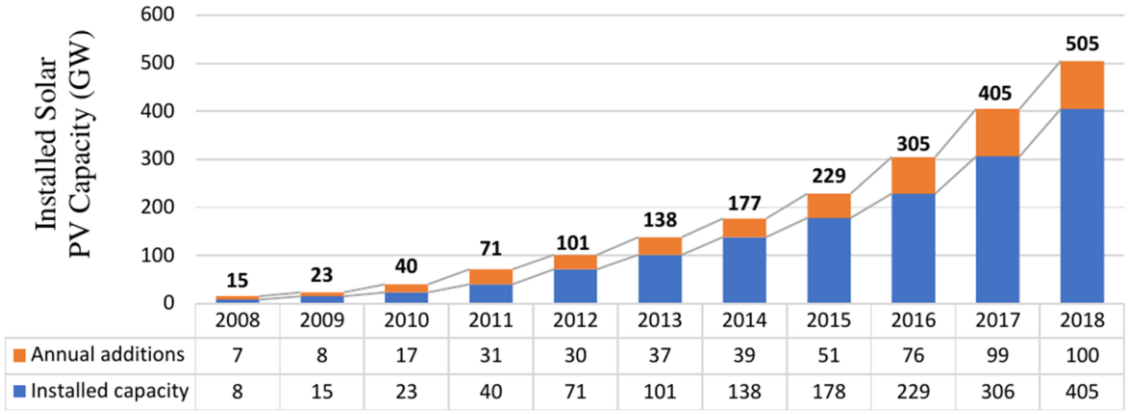
2L-VSI	Two-level voltage source inverter
3L-NPC	Three-level neutral-point clamped inverter
CB PWM	Carrier-based pulse-width modulation
CB-MPC	Carrier-based model predictive control
CM	Common-mode
CMV	Common-mode voltage
DM	Differential-mode
GaN	Gallium Nitride
HF-ZSCC	High-frequency zero-sequence circulating current
IEC	International Electrotechnical Commission
IGBTs	Insulated-gate bipolar transistors
LF-ZSCC	Low-frequency zero-sequence circulating current
MIMO	Multi-input-multi-output
MPC	Model predictive control
MPPT	Maximum power point tracking
NPC	Neutral-point clamped inverter
NP-LCL	Neutral-point connected LCL filter
PD	Phase-disposition
PI	Proportional integral
PV	Photovoltaic
PWM	Pulse-width modulation
SVM	Space-vector modulation
SiC	Silicon Carbide
VSI (VSC)	Voltage source inverter (Voltage source converter)
WBG	Wide-band-gap
ZCMV PWM	Zero common-mode voltage pulse-width modulation
ZSCC	Zero-sequence circulating current

Chapter 1 Introduction

Rapid growing solar photovoltaic (PV) generation becomes one of the major sources of renewable electricity to meet the worldwide increasing energy demand. According to the latest Renewables 2019 Global Status Report [1], the newly installed PV generation capacity has increased by 199 GW in the past two years as shown in Fig. 1.1, which leads renewable capacity growth and accounts for 55% of the global total renewable addition. The Global Market Outlook for Solar Power [2] reveals the prospective global PV market will double its size from 505.1 GW to over 1TW by 2022. Behind the fast growing PV market, one driving force is the massive production capacity of the silicon-based PV module, which facilitated over 90% price drop of the PV module in the past 20 years [3, 4]. The other reason is development of the solid state PV inverters, which enables integration of distributed solar plants into utility power grid [5-7]. Meanwhile, the rapid expanding PV capacity imposes greater challenges on the efficiency, reliability, and power density of the grid-interfacing PV inverters [5-11].

In the solar-to-grid energy conversion process, the grid-connected PV inverters play a key role in converting the direct current (DC) from PV power to the grid-frequency alternating current (AC) power. On the one hand, yield of PV system is dependent on efficiency of the PV inverters. On the other hand, reliability of the PV inverters has been identified as the major constrain for solar production. According to the statistics, the average lifespan of commercialized PV inverters is around 5-10 years, while the PV modules can last for over 25 years [12]. PV inverter is among the most vulnerable components in PV systems, which can affect the yield of the solar farms in a significant way [13]. Beside efficiency and reliability, inverter's power density is another important aspect to be considered during the design. For the emerging utility-

scale PV projects, number of the PV inverters can easily reach up to several thousands, which requires considerable manpower for installation and maintenance. Size and weight of PV inverters can make significant difference in inverter-related labour cost [14]. Thus, it is highly desirable to improve the PV inverter's power density.



	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
Annual additions	7	8	17	31	30	37	39	51	76	99	100
Installed capacity	8	15	23	40	71	101	138	178	229	306	405

Fig. 1.1. Cumulative installed global solar PV capacity between year 2008 to 2018 as reported in the Renewable 2019 Global Status Report [1].

1.1. Voltage source inverters in solar PV applications

Varieties of the PV inverter topologies have been developed to enhance the system efficiency, reliability, and power density [8-11]. Due to the advances in semiconductor devices, voltage source inverter (VSI) have been widely applied in the grid-connected PV inverters. In general, the grid-connected VSI-based PV inverters can be classified into three categories as shown in Fig. 1.2, which includes 1) central PV inverters, 2) string or multistring PV inverters, 3) AC module PV inverters [5, 15, 16]. Central inverters are developed for the utility-scale PV installations, while string or multistring PV inverters can be found in all types of the PV

installations. AC module PV inverter finds more of its application in residential-scale or commercial-scale PV installations. This thesis focuses on the first two types of the PV inverters.

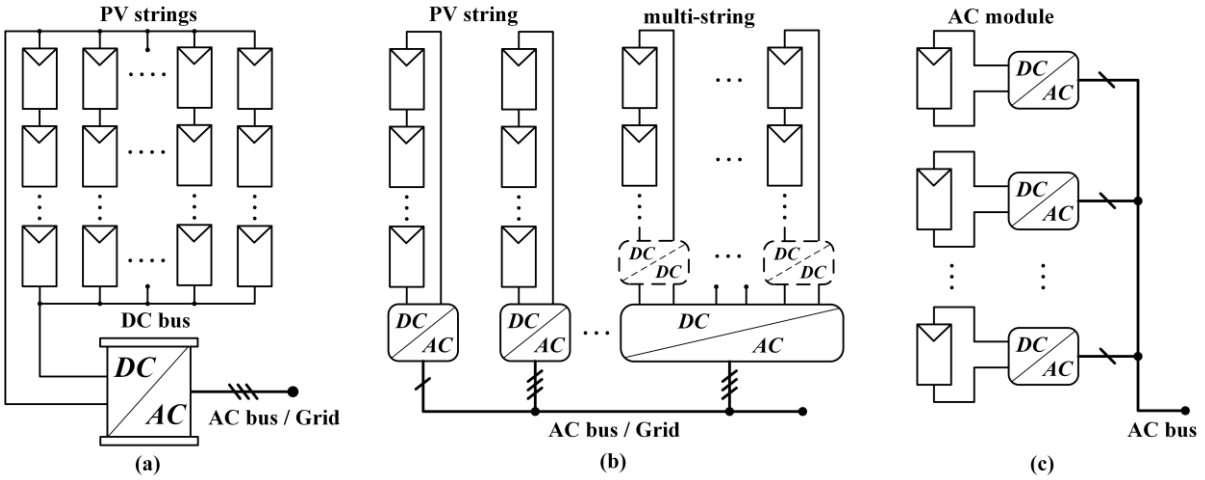


Fig. 1.2. Different types of the grid-connected VSI-based PV inverters: (a) three-phase central PV inverter, (b) one-phase/three-phase string and multistring PV inverters, (c) AC module PV inverters.

1.1.1. Grid-connected central PV inverters

Central PV inverters are more suitable for large utility-scale PV installations because of higher capacity, fewer components, and lower maintenance cost. As shown in Fig. 1.2, PV panels are series-parallel connected to common central PV inverter through the DC combiner box. The entire PV farm runs and relies on one central inverter, which imposes more challenges on the inverter's reliability. Also, the power loss can be higher due to the common maximum power point tracking (MPPT) strategies and module output mismatch [17]. Even though, it is still the proven inverter technology that widely applied in the large-scale PV generations.

The rapid expanding PV market has imposed increasing demand for the central inverter with higher capacity. Nowadays, the commercial central PV inverters can reach up to multi-megawatts in capacity, e.g., SMA offers a 4.7 MW central inverter for solar PV [18], and ABB's

central PV inverters have a power capability of 5 MW [19]. In such high-power PV inverters, modular paralleled multi-VSI systems can be employed to extend the inverter's capacity beyond the switching device's current limit without harming the system's efficiency and reliability [20, 21].

1.1.2. Grid-connected string or multistring PV inverters

String or multistring PV inverters can replace the central inverters in small utility-scale PV installations (below 1 MW). Higher yield can be achieved by implementing the MPPT individually for each PV string. Each PV string is individually controlled by a single inverter (string inverters) or by DC-DC converters (optional in multistring inverters) to realize individual MPPT. Beside efficiency, these designs offer better flexibility compared to central PV inverters, which allows easy "plug-and-play" and simplifies system expansion [5].

Both the single-phase and three-phase VSI topologies can be applied to string or multistring PV inverters. Particularly, single-phase VSIs are more suitable for PV systems rated below 10 kW. Three-phase VSIs are more favorable for larger PV installations where single-phase VSIs may cause the grid unbalance [16]. Facing the trend of expanding PV capacity, the study focuses on the most popular three-phase string or multistring PV inverters which have better grid interfacing capability. Power ratings of these inverters range from one kilowatt to a few hundred kilowatts. The market trend of such type PV inverter is towards higher power densities [14]. Taking the state-of-the-art commercial product for instance, SMA recently released a 75kW three-phase multistring PV inverter with a power density of 0.58 kW/L for volume or 0.97kW/kg for weight [22].

Multilevel VSI topologies are adopted to improve the output quality and power density. Compared to the conventional two-level VSIs, multilevel VSIs have better performance because

of lower switching stress, less harmonic distortions, and higher efficiency [9-11]. The performance can be further leveraged by employing the wide-band-gap (WBG) devices like 1200 kV Silicon Carbide (SiC) or 600V Gallium Nitride (GaN) [23]. Compared to the conventional silicon-based switching devices such as insulated-gate bipolar transistors (IGBTs), these WBG devices have higher switching frequencies (above 10 kHz) and much lower switching losses. Increasing application of those WBG devices are found in string or multistring PV inverters [24, 25].

1.2. CM voltage effects in transformerless PV inverters

In addition to the cost and performance, safety has always been a priority for grid-connected PV inverters, where common-mode voltage (CMV) could cause major safety concerns. In a balanced three-phase PV system, CMV is the average of phase-to-neutral output voltages v_{an}, v_{bn}, v_{cn}, which can be derived in (1.1). CM leakage current will be produced if there exists a circulating path, e.g., in grid-tied transformerless PV inverter systems. The leakage current i_{CM} is expressed in (1.2), where Z_{CM} denotes the CM equivalent impedance across the system.

$$v_{CM} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn}) \tag{1.1}$$

$$|i_{CM}| = \frac{|v_{CM}|}{|Z_{CM}|} \tag{1.2}$$

Traditionally, a high-frequency DC transformer or a line-frequency AC transformer is implemented in PV inverters to enhance the safety performance, which can provide galvanic isolation between the PV source and utility grid. However, these heavy and bulky transformers increase the PV inverter's size, weight, and cost while lowering the efficiency and power density [26-28]. To address those challenges, transformerless PV inverters are developed and adopted in

the grid-connected PV applications [5, 8-11]. Without the transformers, inverter's power density and efficiency can be significantly improved [29, 30]. However, in transformerless PV inverters, common-mode (CM) leakage current can be produced due to change of CMV. Without the galvanic isolation, grounding path forms between the PV panels and utility grid, which allows the flow of the CM leakage currents. As shown in Fig. 1.3, circulation path for CM leakage current is plotted in red, where the C_g denotes the parasitic capacitance of the PV arrays in range of 50–150 nF/kW [16]. For the utility-scale PV installations, PV panels become dangerous to touch where the leakage current can flow through human body to cause electrical shock or safety hazards. Beyond the safety concerns, major issues such as output waveform distortion, extra power loss, and electromagnetic interference will arise if the CM harmonics are not properly eliminated [31, 32].

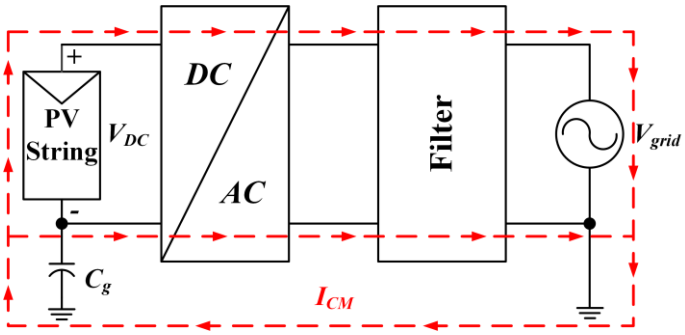


Fig. 1.3. CM leakage current circulation path (as plotted in red) in transformerless PV systems.

There are several widely accepted industrial standards specifying the limit for CM harmonics. For instance, IEC-62109 defines the CM leakage current limit of 300mA in RMS [33]. In practice, transformerless PV inverters usually require large CM chokes to suppress the CM current in order to comply with the grid code. The size of the CM choke depends on the peak value of the high-frequency CM harmonics. To scale down the costly and bulky CM

chokes, improved inverter topologies [32, 34, 35] and pulse-width modulation (PWM) schemes [36-45] are developed for different types of the PV inverters. For instance, zero CMV (ZCMV) PWMs are mainly proposed for sting/multistring PV inverters employing the multilevel topologies [38-42], while the interleaved PWM technique can be applied to high-power central PV inverters when modular parallel VSIs are adopted [43-45]. This thesis focuses on addressing the key issue of employing ZCMV PWMs and interleaved PWM technique to reduce CMV effects in different types of grid-connected transformerless PV inverters.

1.3. CM harmonics elimination with ZCMV PWM

For the string or multistring PV inverters, a widely applied T-type three-level neutral-point-clamp (T-type 3L-NPC) inverter topology has been selected for investigation [46]. The topology can be found in Fig. 1.4. On the one hand, it has fewer components, lower switching loss, and simplified current commutation loop compared to conventional 3L-NPC topologies [46, 47]. On the other hand, this topology offers three output levels, which makes it easier to comply with grid codes such as IEEE519 or IEEE1547. Compared to the conventional two-level VSI, output harmonics are pushed to higher orders with lower magnitudes [48], which can be converted to less CM harmonics or lower leakage current. However, the reduction is insufficient especially in string or multistring PV inverters, because large CM choke or isolation transformer are still required in order to eliminate the CM leakage current to below 300mA according to IEC-62109 [33]. To achieve transformerless power conversion without using a large CM choke, zero common-mode voltage (ZCMV) PWMs have been proposed as an attractive solution for multilevel PV inverters [38-41].

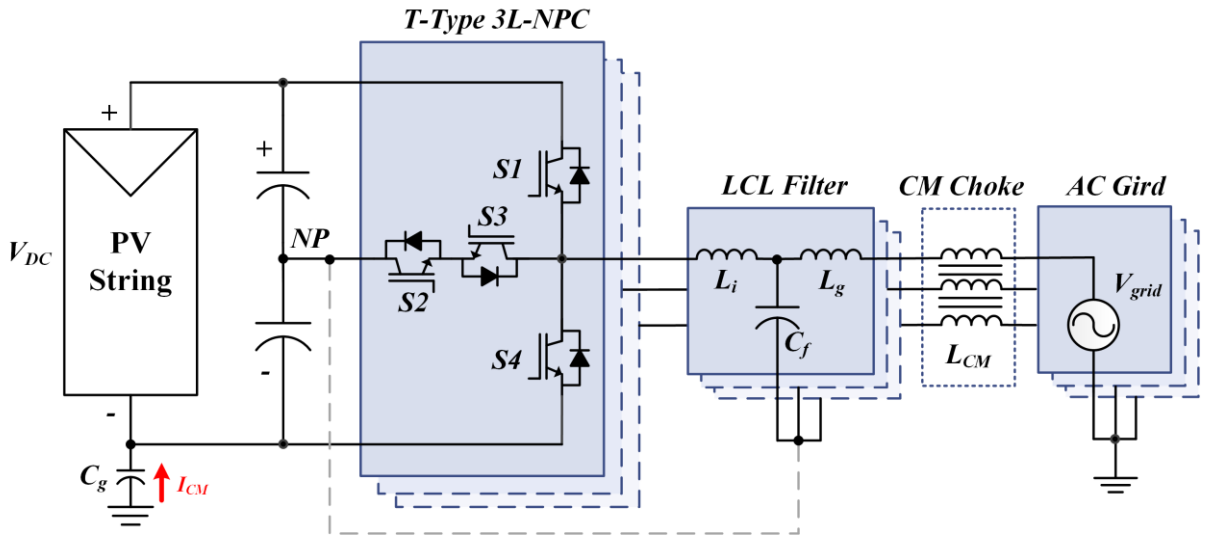


Fig. 1.4. Topology of three-phase T-type 3L-NPC in transformerless string or multistring PV inverters

In T-type 3L-NPC PV inverters, the output voltage/current are actively controlled by adjusting the firing angles of IGBTs. Each phase has three possible outputs $+V_{dc}/2$ [P], 0 [O], and $-V_{dc}/2$ [N]. Considering all three phases, there are 27 switching states and 18 switching vectors. As summarized in Table 1.1, switching actions of the IGBTs will generate different levels of CMV on the neutral terminal. For conventional PWM methods such as phase-disposition (PD) or space vector modulation (SVM), significant amount of the high-order CM harmonics will be produced due to selection of the switching states with different CMV. Aiming at transformerless power conversion and smaller CM filters, modified PWM methods have been proposed by only selecting switching states producing zero CMV. ZCMV PWMs can be realized with either SVM [38, 39] or carrier-based PWM [40, 41]. Taking SVM-based ZCMV PWM for instance, only the medium vectors [NPO], [NOP], [PON], [PNO], [OPN], [ONP] and zero vector [OOO] are selected during modulation. High-order CM harmonics can be reduced if all the switching states produce zero CMV. More details about SVM-based ZMCV studied in the thesis can be found in Fig. 1.5. It should be noted that ZCMV PWMs has a major drawback, which is inverter's DC

voltage utilization rate. With ZCMV PWMs, DC voltage utilization rate is 13.4% lower compared to the conventional PWM methods. Despite of the lower DC voltage utilization rate, ZCMV PWMs are still widely applied in string PV inverters and electrical motor drives where leakage current is a major concern.

Table 1. 1. Common-Mode Voltages of Three-Phase T-type 3L-NPC Inverter with 27 Switching States

Switching states	CMV (V_{CM})
PPP	$+V_{dc}/2$
PPO, POP, OPP	$+V_{dc}/3$
PNP, PPN, NPP, OOP, POO, OPO	$+V_{dc}/6$
OOO, NPO, NOP, PON, PNO, OPN, ONP	**0**
NPN, NNP, PNN, OON, NOO, ONO	$-V_{dc}/6$
NON, ONN, NNO	$-V_{dc}/3$
NNN	$-V_{dc}/2$

Beside DC voltage utilization rate, there are other factors such as dead-time effect, and resultant total filter volume, which can affect the applicability of ZCMV PWMs in the transformerless PV inverters. Theoretically, CMV can be 100% eliminated with ZCMV PWMs thus no CM filter is required. In practice, CMV spikes with a magnitude of $V_{dc}/6$ can be observed due to the inevitable dead-time effect, which still requires a CM choke. On the other hand, considering the ZCMV modulation will undermine the output current quality which may lead to size increase of differential-mode (DM) filters, the impact of ZCMV on the total filter volume remains unknown, which also requires further investigation.

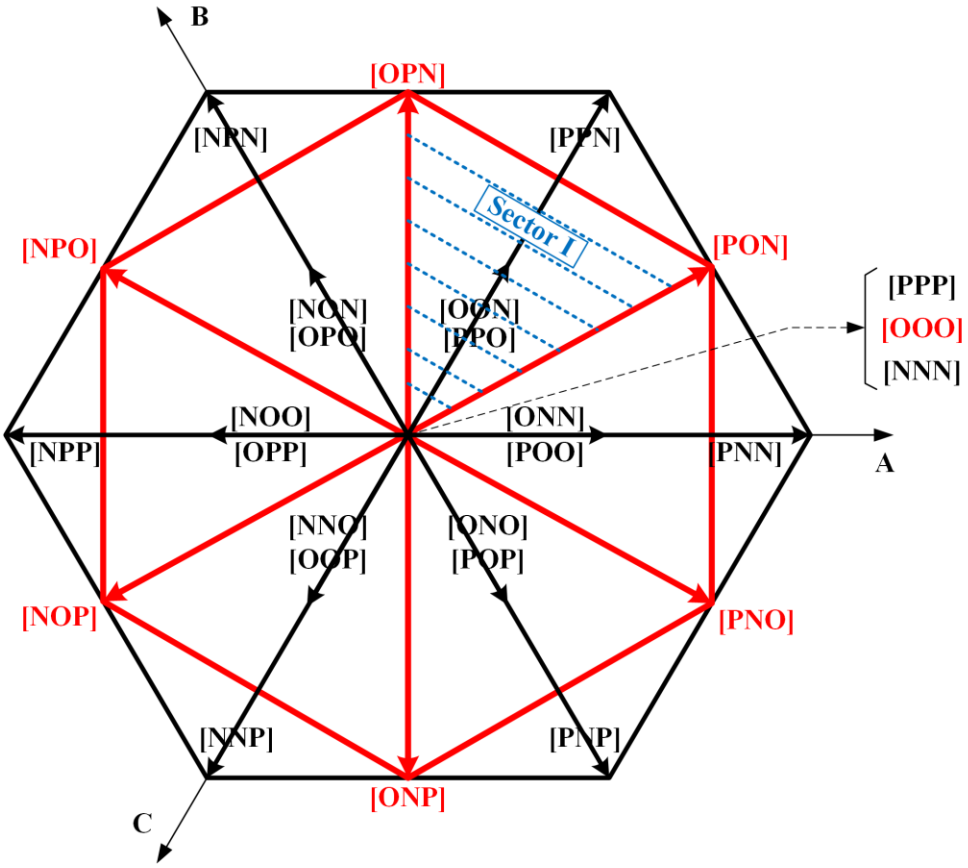


Fig. 1.5. Summary of voltage vectors for the three-phase T-type 3L-NPC inverter. In the conventional SVM-based ZCMV PWM scheme, only the six medium vectors [PON] [OPN] [NPO] [NOP] [ONP] [PNO] and a zero vector [OOO] are select for modulation (as highlighted by red in this figure).

1.4. CM harmonics reduction with interleaved PWM

Employing modularity becomes the trend of modern power electronics, where parallel operation of three-phase VSIs is commonly found in high-power multistring or central PV inverters [49]. Higher power ratings can be easily achieved along with better scalability, reliability, and fault tolerant capability [50-51]. In this work, modular parallel two-level VSI (2L-VSI) system has been selected for illustration. As shown in Fig. 1.6, multiple 2L-VSI modules

are sharing a common DC-link, and parallel-connected to the AC grid. Each inverter module shares partial of the total load during DC-to-AC power conversion.

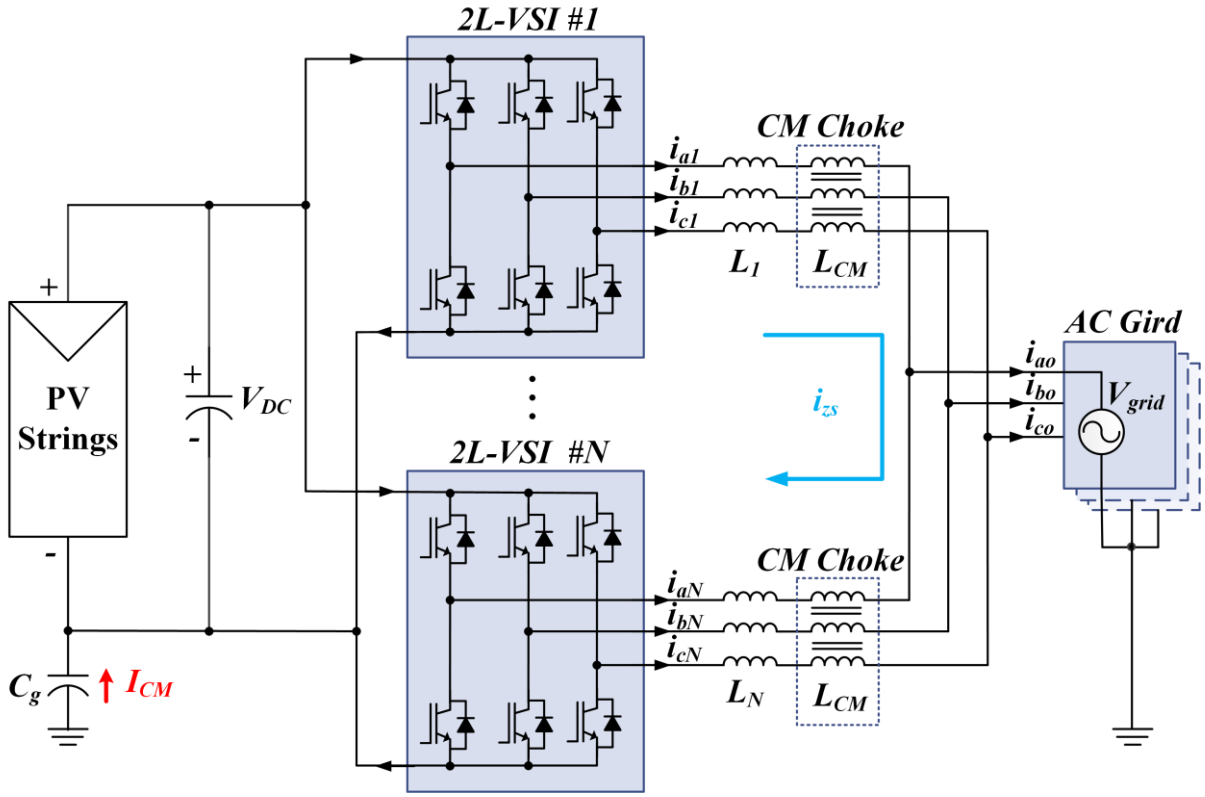


Fig. 1.6. Topology of N modular paralleled 2L-VSIs in multistring or central PV inverters.

Facing the challenge of CMV effects, interleaved PWM techniques [43-45] can be employed in paralleled multi-VSIs for reduction of the CMV effects or leakage current. If the PWM carriers for each inverter are phase-shifted by $2\pi/N$ radians, the dominant CM harmonics will be pushed from the carrier frequency of f_{cr} to higher orders. More specifically, frequency-domain analysis in Fig. 1.7 indicates that the dominant CM harmonics of N interleaved 2L-VSIs appears at N times of the carrier frequency. Larger the module number N, higher the order of dominant CM harmonics, which will result in a smaller CM filter. Additional benefits of the interleaved PWM include multiple output voltage levels, reduced PWM voltage ripple, cancellation of low-

order DM harmonics, and size reduction of the passive filtering components. According to the study in [75], the most used LCL filters can be replaced with smaller L filters to satisfy the grid code, when a certain number of converters are interleaved. With smaller DM filters adopted in each module, system power density can be further improved.

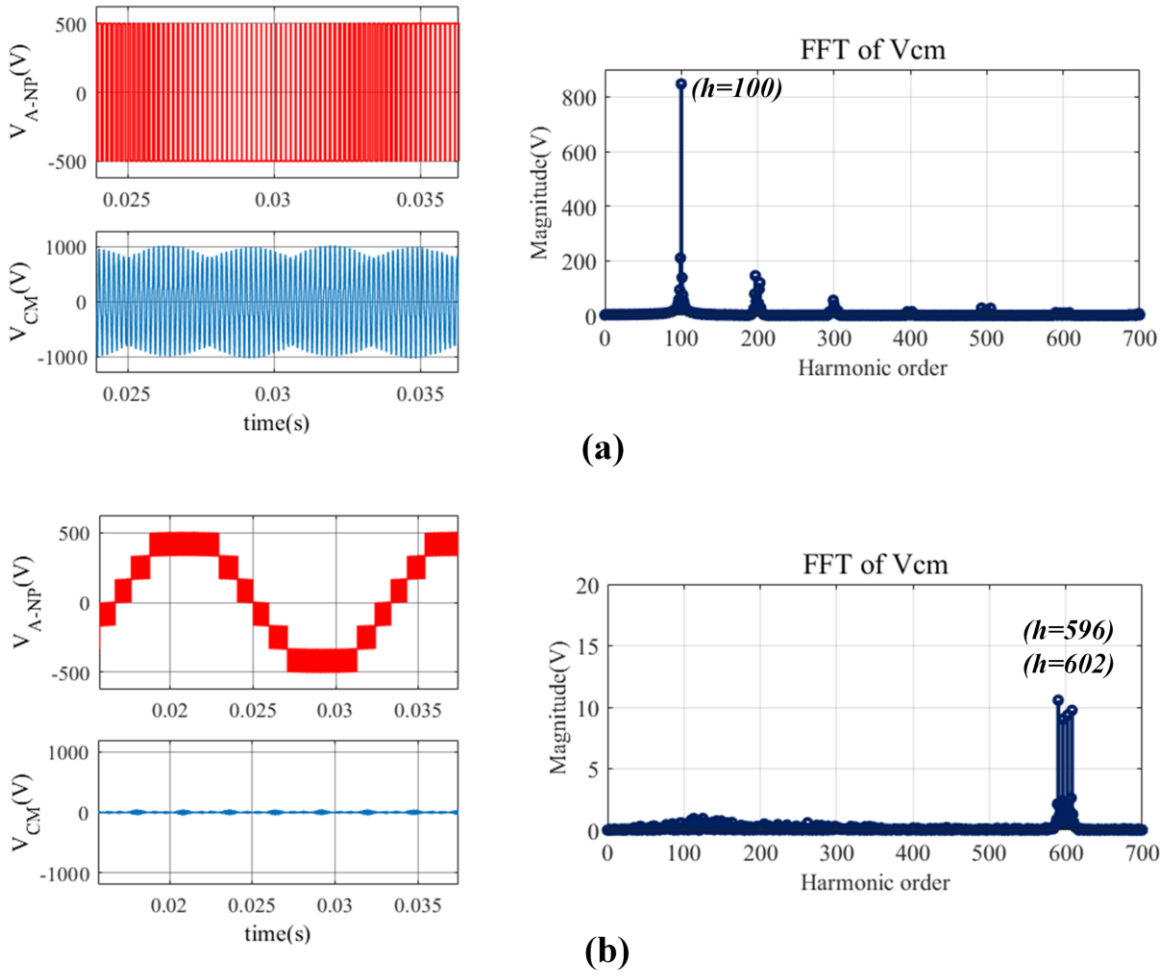


Fig. 1. 7. CM harmonics distribution of six paralleled 2L-VSIs modulated with (a) synchronized (non-interleaved) PWM (b) interleaved PWM technique. Waveforms of phase A to neutral-point voltage $V_{A\text{-}NP}$, common-mode voltage (CMV) V_{CM}, and frequency domain FFT analysis of V_{CM}. where the fundamental frequency is 60Hz; carrier frequency is 6kHz (or h=100); DC-link voltage is 1000V.

However, zero-sequence circulating current (ZSCC) i_{zs} becomes the major concern when adopting interleaved PWM in modular parallel VSIs. ZSCC can be decomposed into the high-frequency (HF) components and low-frequency (LF) components. HF-ZSCC is the side-effect of

interleaving as the terminal voltages are different among the paralleled inverters. CM choke is required to be implemented in each inverter to eliminate the HF-ZSCC. LF-ZSCC can be generated due to the inevitable hardware parameters mismatch and/or unequal power sharing among the paralleled inverter modules. If not properly eliminated, such LF-ZSCC may saturate the CM choke, increase device power loss, and even damage the entire system. In the central or multistring PV inverters that adopting paralleled multi-VSIs, CMV effects can be mitigated with interleaved PWM if and only if LF-ZSCC has been completely eliminated.

To regulate LF-ZSCC in the interleaved multi-VSI systems, zero-sequence (ZS) controllers can be applied in different control schemes. References [50, 51] propose some simple ZS current controllers. Those controllers are to be implemented in a distributed manner at each inverter, where communications among the modules are prohibited. However, these communication-less ZS controllers are not effective when the inverter modules have different output powers. Such condition is commonly seen when unit-shading strategy is applied to improve the light-load efficiency. Facing those challenges, centralized control methods [52-62] are proposed where communications are implemented among ZS controllers to achieve complete elimination of LF-ZSCC. In such design, paralleled inverter modules are usually integrated into one housing, where data exchange are made through the interconnected fiber-optic cables. Different ZS control methods sharing the similar control architecture can be found in literature which including proportional integral (PI) control based method [52], feed-forward control based methods [53, 54], deadbeat control based methods [55, 56], and model predictive control (MPC) based methods [57-62]. In these methods, each inverter needs to exchange data with all other modules, which requires significant amount of the communication cables. Beside higher cost, complex communications will impose more challenges on installation and maintenance. In addition, most

of the existing LF-ZSCC control schemes, especially those adopting MPC, are only applicable to two paralleled inverters. Without a generalized ZSCC model, methods like [57-62] cannot be applied to multiparalleled VSI systems with more than two modules. Therefore, it is highly desirable to develop a generalized LF-ZSCC control scheme which has lower cost and better applicability to *N* modular parallel VSIs.

1.5. Thesis contributions and organization

This thesis focuses on addressing the key issues of employing ZCMV PWM and interleaved PWM to reduce the CMV effects in different types of the grid-connected transformerless PV inverters. Multilevel VSI and modular paralleled VSIs are both considered in this study. Major contributions of this thesis are outlined in below.

- For string or multistring PV inverters with multilevel VSIs, CMV cannot be completely eliminated with ZCMV PWM methods due to the inevitable dead-time effect. In Chapter 2, a thorough investigation of the dead-time effect is conducted on T-type 3L-NPC inverters when modulated with ZCMV PWMs. A cost-effective dead-time mitigation strategy of using DC neutral-point connected LCL (NP-LCL) filter has been proposed, which does not introduce any additional passive filtering elements into the system. However, considering the undermined output quality, ZCMV PWMs still require larger DM filters compared to conventional PWM methods. The actual impact of ZCMV PWMs on the total output filter volume remains unknown. This thesis first explores the actual impact of ZCMV on the total output filter volume. Comparative studies are conducted between ZCMV and conventional PD PWM methods. Volumes of the

resultant CM and DM filters are fairly compared under the same filter parameters design framework. More details about the design and comparison are presented in Chapter 2.

- For multistring or central PV inverters with modular parallel VSIs, interleaved PWM can be employed to reduce the CMV effects, but LF-ZSCC issue must be addressed in the first place. In Chapter 3, a novel centralized carrier-based model predictive control (CB-MPC) scheme has been proposed to achieve interleaving and full elimination of LF-ZSCC in N modular paralleled VSIs. Power can be individually controlled for each inverter module, where LF-ZSCCs caused by unavoidable hardware parameters mismatch and/or unequal module output power are completely eliminated. A generalized ZSCC model has been derived to leverage the employment of modulated MPC. Carriers are adopted to achieve interleaving. Benefits of MPC and interleaved PWM are combined to yield further improvement of the performance. In this thesis, 2L-VSI has been selected for illustration. The proposed method is applicable to N modular parallel multilevel VSIs as well for LF-ZSCC elimination. Compared to the exiting MPC-based LF-ZSCC control methods, the proposed centralized control scheme has better applicability and flexibility, which can be implemented either in a dedicate central controller or in converter's master controllers. More details about the design, implementation, and performance of the centralized CB-MPC are presented in Chapter 3. Conclusions and prospects for future work are summarized in Chapter 4.

Chapter 2 Evaluation of ZCMV PWM in Transformerless T-type 3L-NPC Inverter

In this chapter, a comprehensive evaluation of ZCMV PWM methods is conducted on transformerless T-type 3L-NPC PV inverters. Effectiveness of ZCMV PWMs on eliminating CMV has been studied first, where dead-time effect is thoroughly investigated. The analysis indicates CMV cannot be completely suppressed with ZCMV PWMs due to the inevitable dead-time effect. The resultant CMV spikes will induce leakage current, which still requires a CM choke to suppress. In this work, an empirical evaluation approach has been proposed to quantitively analyze the dead-time effect on ZCMV PWMs. An alternative dead-time mitigation strategy is developed by using DC neutral-point connected LCL (NP-LCL) filter. Since there always exists a differential-mode (DM) LCL filter in such PV inverters, the proposed method does not introduce any additional passive filtering elements into the system. Compared to the conventional LCL filters, NP-LCL provides better attenuation to high-order CM harmonics thus can mitigate the dead-time effect. Effectiveness of the proposed method is verified by experimental results.

However, considering ZCMV will undermine the current quality which could result in larger DM filters, the impact of ZCMV on the overall filter size remains unknown. To investigate the actual size of the resultant CM and DM filters, a comparative study is carried out between ZCMV and the conventional PD PWM methods. Two different filter types, LCL and NP-LCL, are considered in this comparison, which leads to four combinations, i.e. 1) PD with LCL, 2) PD with NP-LCL, 3) ZCMV with LCL, and 4) ZCMV with NP-LCL. Both the DM and CM filters

are considered, upon which the total filter volumes are compared. To ensure a fair comparison, filter parameters are designed under the same framework that in compliance with grid codes IEC-62109 and IEEE1547. Design and analysis have been verified in MATLAB simulation.

2.1. Analysis of dead-time effect in T-type 3L-NPC inverter

The original goal for ZCMV modulation is to achieve net "zero" CMV and to avoid the use of CM chokes. For three-phase T-type 3L-NPC inverters, as summarized in Table 1.1, there exist 27 switching states which can produce different levels of CMV. Only the seven switching states that producing zero CMV, [NPO], [NOP], [PON], [PNO], [OPN], [ONP], [OOO] are selected for modulation. Theoretically, the CMV can be fully eliminated with ZCMV PWM. Fig. 2.1(a) and Fig. 2.1(b) show the measured CMV of the conventional PD and SVM-based ZCMV PWM methods. Zero CMV is observed for ZCMV in Fig. 2.1(b), when the dead-time has not been implemented. However, that is not the case in the real application where dead-time must be implemented in order to prevent the "shoot-through" phenomena. As shown in Fig. 2.1(c), repeating CMV spikes with a magnitude of $V_{dc}/6$ can be observed when dead-time is implemented in ZCMV. To better understanding CMV generated during the dead-time, an in-depth investigation has been conducted in this section. More details about the studied SVM-based ZCMV PWM method can be found in Fig. 1.5.

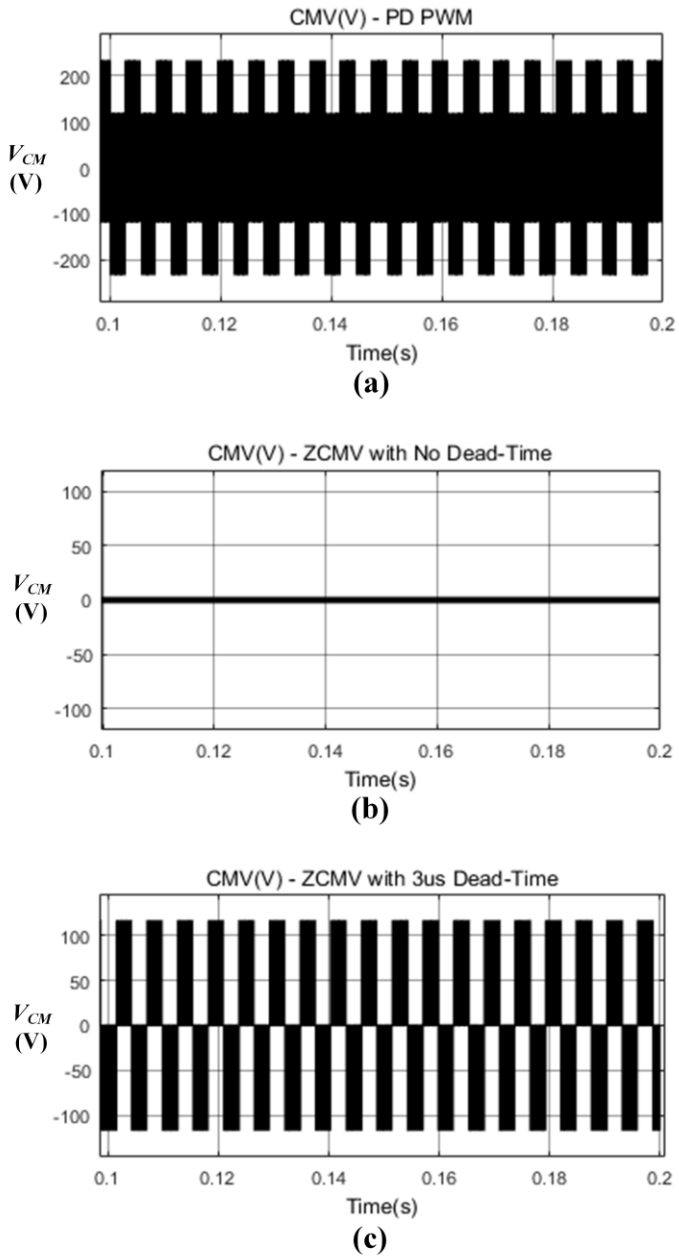


Fig. 2.1. Simulation results of CMV measured from 10kW/400Vrms/60Hz T-type 3L-NPC inverter sampled at 9kHz, when modulated with (a) conventional PD PWM (b) SVM-based ZCMV PWM applied with 0 μs dead-time (c) SVM-based ZCMV PWM applied with 3 μs dead-time.

2.1.1. Current commutation analysis

Dead-time is a very short time period to be implemented in the most PWM schemes including ZCMV. The time delay is implemented between the operation of different switching

devices to avoid the "shoot-through" phenomena. Length of the dead-time T_{DT} depends on the device switching cycle T_s or the switching frequency f_{sw}. Different phase output voltage can be produced during the dead-time, whose magnitude depends on the current flow direction. For example, if one phase is switching from state [O] to state [P], zero output voltage will be produced during the current commutation when the terminal current goes outbound as indicated by blue in Fig. 2.2(a). For the same switching action, if current flows inbound as plotted by red in Fig. 2.2(a), the output voltage will be $V_{dc}/2$ during the dead-time. Current commutation of all the other switching actions can be analyzed in the same way as shown in Fig. 2.2(b) to Fig. 2.2(d).

Most importantly, CMV spikes will be produced during the dead-time, which is known as the dead-time effect. In three-phase T-type 3L-NPC inverters, CMV spikes will be produced when the two phases with opposite current-flow are switched. Taking one switching cycle from sector I for example (Fig. 1.5), the output voltage is synthesised by three vectors [PON] [OPN] and [OOO]. CMV spikes will be produced when the actual output state changes from [OOO] to [PON], [PON] to [OPN], or [OPN] to [OOO]. As shown in Fig. 2.3, there will be exactly one CMV pulse generated in each switching cycle, whose polarity depends on the current flow direction. The pulse duration equals to the length of the dead-time T_{DT}. The amplitude equals to the average of the three-phase output voltage, whose magnitude is $V_{dc}/6$ according to (1.1). As shown in Fig. 2.1(c), CMV spikes are measured to be 116V which equals to one-sixth of the DC-link voltage of 700V.

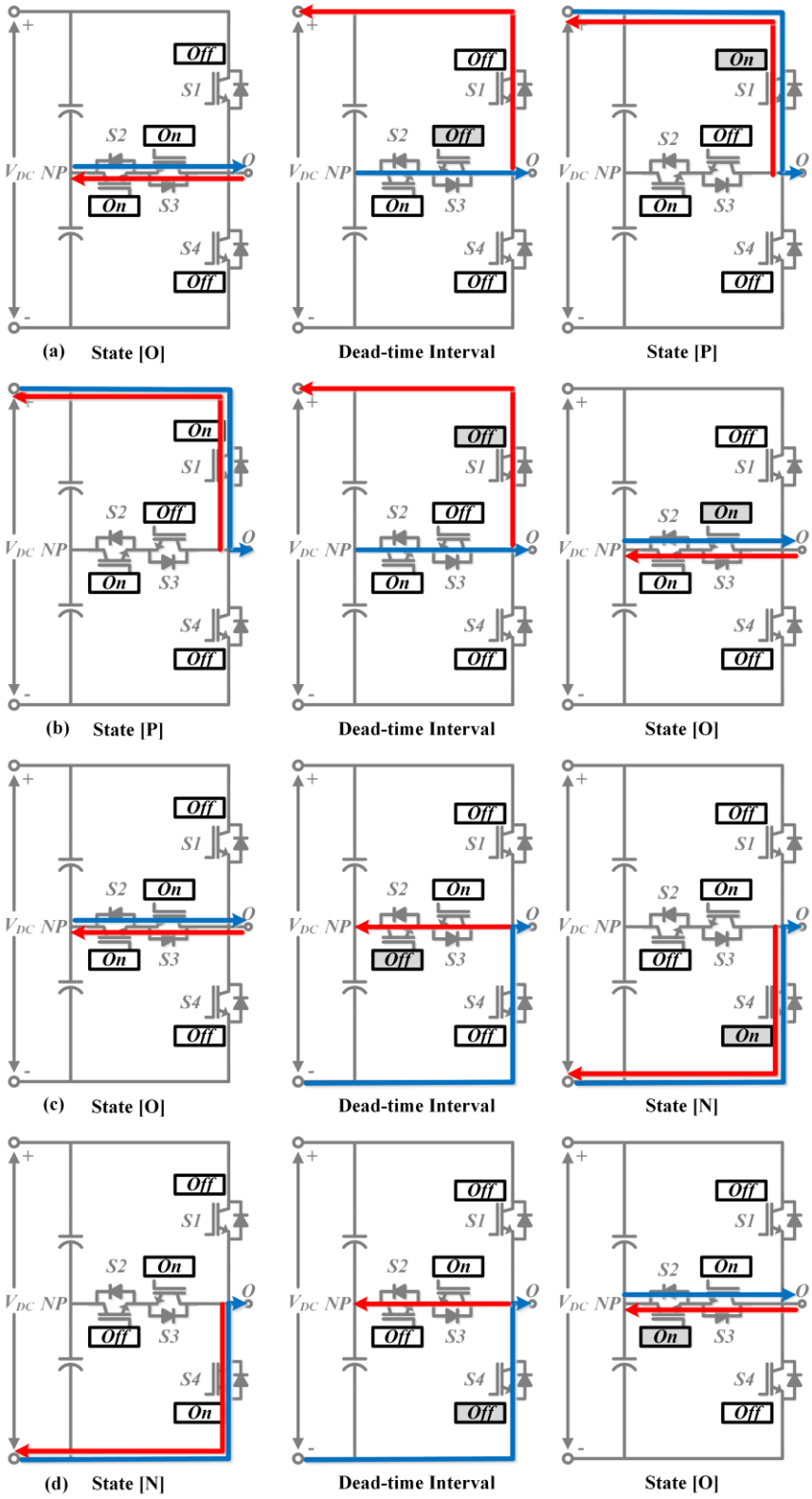


Fig. 2.2. Current commutation for one phase during switching state transition from (a) [P] to [O], (b) [O] to [P], (c) [O] to [N], (d) [N] to [O]. Inbound current flow is plotted in red. Outbound current flow is plotted in blue.

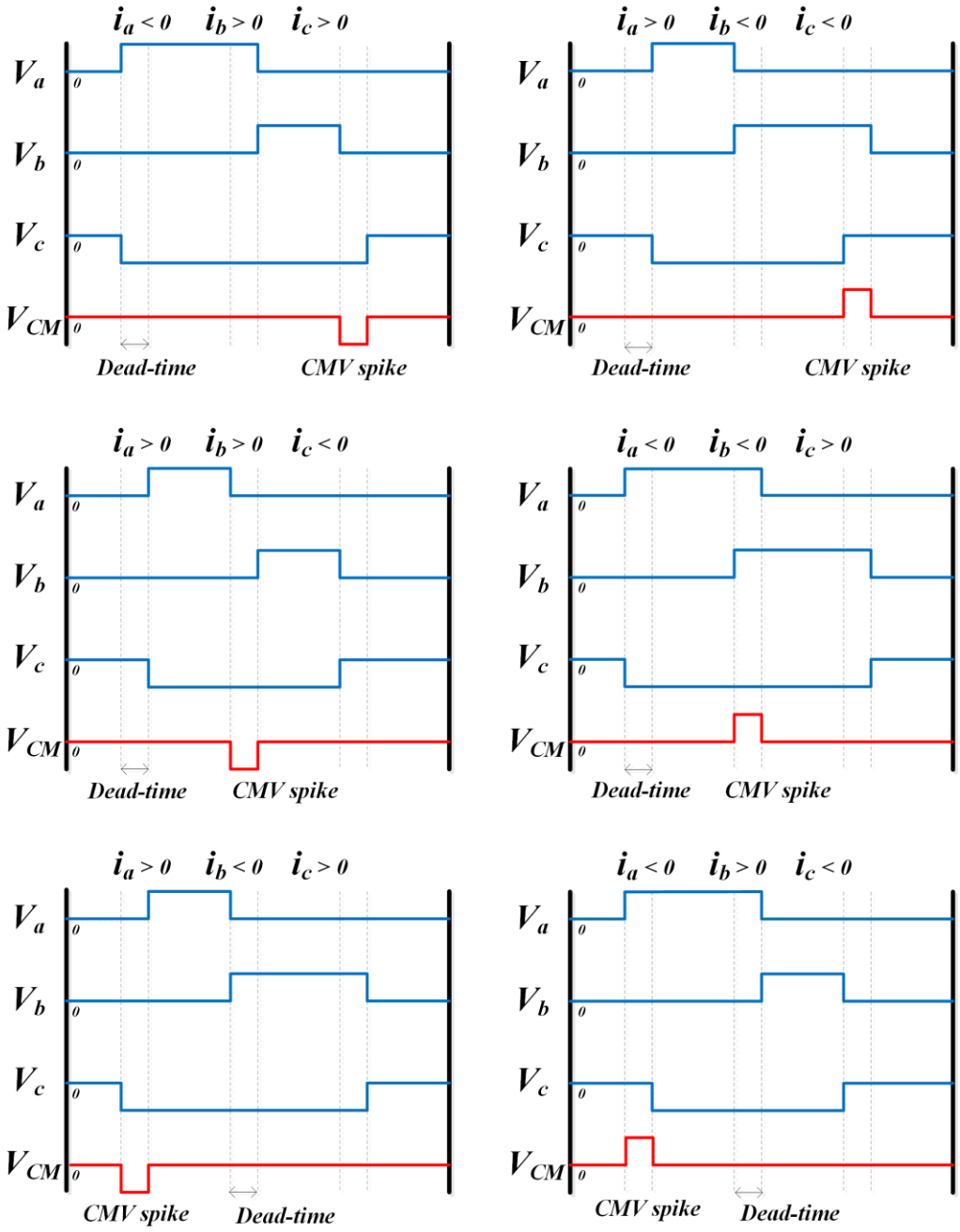


Fig. 2.3. CMV spikes caused by dead-time in one switching cycle (from Sector I) when modulated with SVM-based ZCMV PWM.

2.1.2. Fourier analysis

Fourier analysis has been conducted to further investigate the dead-time effect on ZCMV PWMs. As shown in Fig. 2.4, CMV spikes can be approximated by multiplication of two

periodic square waves. Since there is only one CMV spike generated in each switching cycle, the CMV pulse wave can be first approximated by a periodic square wave $f_1(t)$ without considering its polarity. The first wave $f_1(t)$ reveals the frequency and amplitude of CMV spikes (frequency f_{cr} = 9kHz, amplitude =$V_{dc}/6$). Pulse duration equals to the length of dead-time T_{DT}. The second wave $f_2(t)$ indicates the polarity of CMV spikes, which has 50% duty cycle repeating at three times of the fundamental frequency f_g (180Hz in this case).

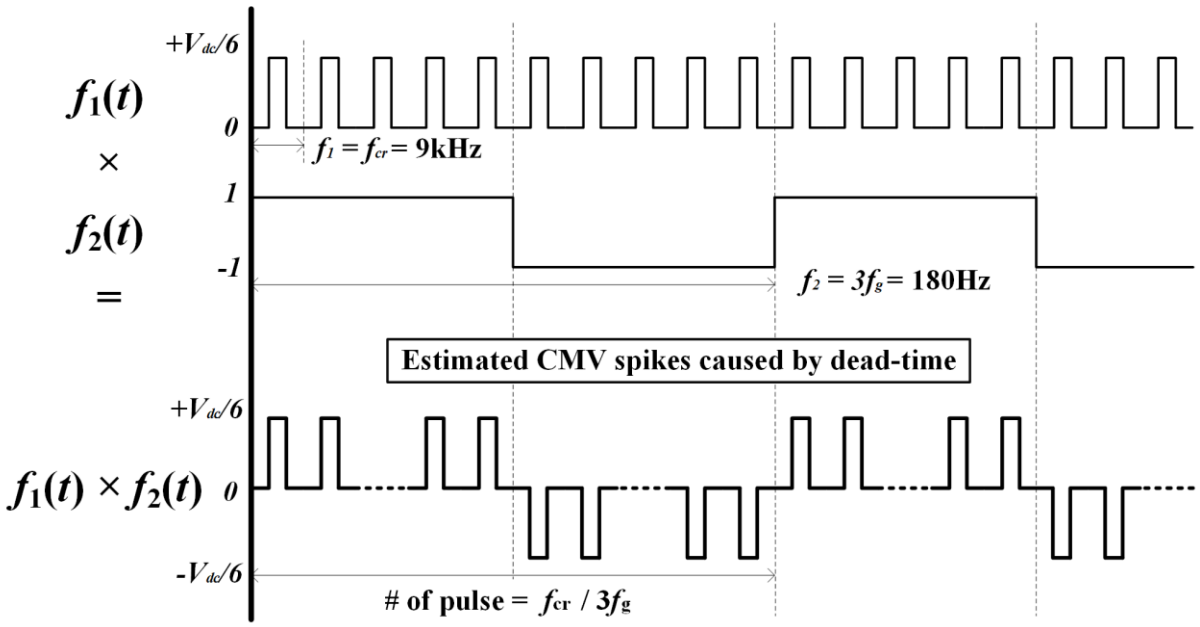


Fig. 2.4. Estimation of the waveform of CMV spikes caused by dead-time: $V_{CM}(t) \approx f_1(t) \times f_2(t)$.

According to the convolution theorem, multiplication in time domain is equivalent to convolution in frequency domain. Since $V_{CM}(t)$ equals to the product of $f_1(t)$ and $f_2(t)$, frequency domain Fourier expression of $V_{CM}(h)$ can be obtained in (2.1) by performing convolution multiplication of $F_1(n)$ and $F_2(m)$, where * denote the convolution operation; m denotes the harmonic order of f_1 at the fundamental of f_{cr}; n denotes harmonic orders of f_2 with a fundamental frequency of $3f_g$; h denotes harmonic order of V_{CM} based on f_g.

$$V_{CM}(h) = \mathrm{F}[f_1(t)f_2(t)] = F_1(n) * F_2(m) \tag{2.1}$$

Accordingly, the magnitude of $V_{\mathrm{CM\_ZCMV}}$ at different harmonic order h can be derived in (2.2).

$$V_{CM\_ZCMV}(h) = \frac{2V_{dc}T_{DT}f_{cr}}{3\pi h}\sin\left(\frac{\pi h}{2}\right) + \sum_{\substack{\tau=-\infty \\ \tau\neq 0 \\ \tau\neq f_g h/f_{cr}}}^{+\infty} \frac{2V_{dc}f_g \sin(3\pi f_{cr}T_{DT}\tau)}{3\pi^2\tau(f_g h - \tau f_{cr})}\sin\left[\frac{(f_g h - \tau f_{cr})\pi}{2f_g}\right] \tag{2.2}$$

From the above derivation, dead-time effect on ZCMV PWMs become quantitatively analyzable. Based on the magnitude of dominant CM harmonics estimated, the minimal CM inductance required to satisfy IEC-62109 can be determined when designing the CM filter.

CMV spectrums of a 10kW/380Vrms/60Hz T-type 3L-NPC inverter modulated with ZCMV PWM are shown in Fig. 2.5. The carrier frequency is 9kHz. Dead-time applied is 1% or 1.1μs. One can see the dominant CM harmonics caused by dead-time appear at the multiple of carrier frequency f_{cr} plus or minus three times of the fundamental frequency f_{g}. The dominant sidebands appear at the order of $150k\pm3$ where k=1,2,3…. The amplitude of CM components is estimated by (2.2) accordingly. Simulation results are also provided for verification. By comparing the analytical results with the practical results presented in Fig. 2.5(a), discrepancies are observed at the odd multiple of the carrier frequency (150^{th}, 450^{th}…). In the simulation results, low-order sidebands at odd multiples (147^{th}, 447^{th}…) are transferred to high-order (153^{rd}, 453^{rd}…) causing the amplitude of high-order sidebands increased to 163%. Such discrepancy between the analytical results and the practical results is caused by location variation of the CMV spikes. In previous analysis, it was assumed periodic CMV pulses repeating at each sampling cycle T_{s}. In fact, as shown in Fig. 2.3, there are three possible CMV pulse locations in each switching cycle, which leads to the dominant odd sidebands shifting from low-order side to the high-order side (e.g. from h=147 to h=153). Also note that the percentage discrepancy between the practical and

analytical results are always less than 70% for all m_a. Thus, 200% calculated V_{CM_ZCMV} should be selected for a conservative design of CM filters.

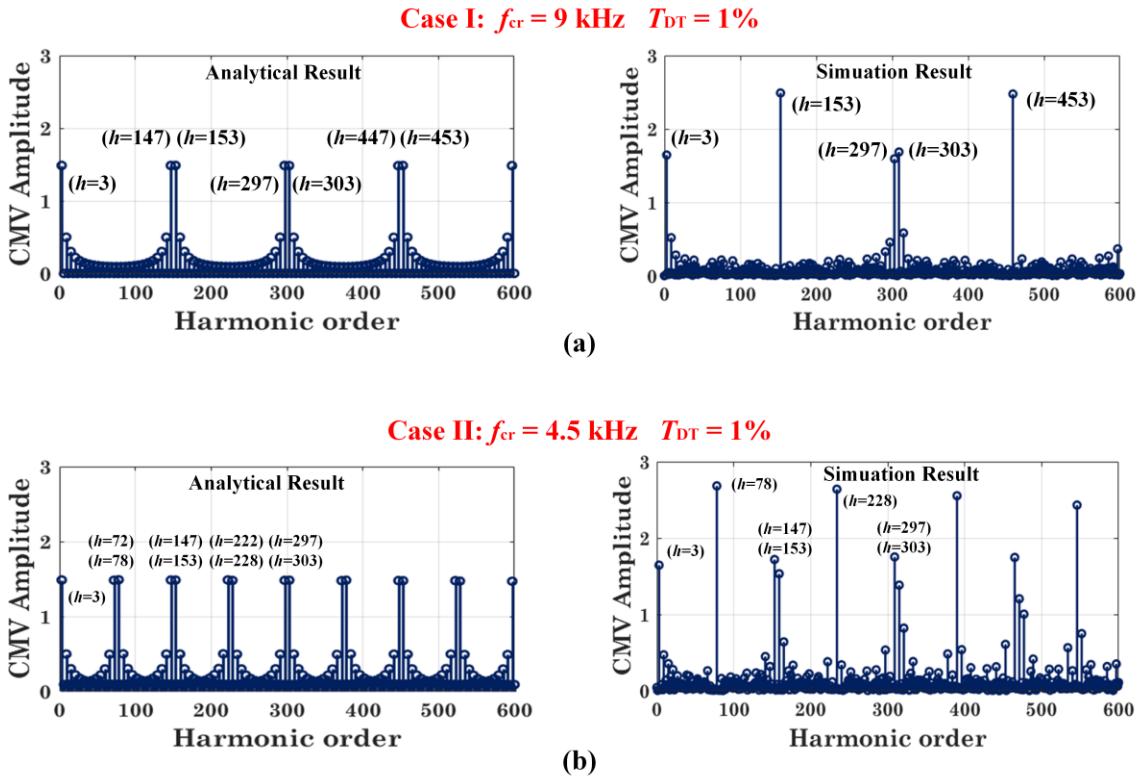


Fig. 2.5. Harmonics spectrums of CMV caused by dead-time when modulated with ZCMV PWM at (a) f_{cr} = 9kHz, T_{DT}=1%T_s; (b) f_{cr} = 4.5kHz, T_{DT}=1%T_s. For each case, analytical result is on the left, simulation result is on the right.

Above analysis and estimation are applicable to three-level inverter systems with different carrier frequencies. By observing (2.2), the amplitude of CMV spike caused by dead-time are proportional to T_{DT}/T_s. In other words, if T_{DT} always equals 1% of T_s, amplitude of CMV caused by dead-time will be irrelevant to the carrier frequency. Back to previous study, if the carrier frequency changes from 9kHz to 4.5kHz with 1% (or 2.2μs) dead-time applied, the amplitude of dominant CMV components will not change. As shown in Fig. 2.5(b), dominant CM harmonics appears at 75k±3 where k=1,2,3…, whose magnitudes are identical to the case of f_{cr} = 9kHz. In

this study, it has also been found that the magnitude of CMV caused by dead-time is irrelevant to the power factor.

2.2. Mitigation of the dead-time effect with NP-LCL filter

It has been shown that dead-time effect is inevitable for ZCMV PWMs. In transformerless T-type 3L-NPC PV inverters, CMV spikes generated at dead-time can cause danger leakage currents, output waveform distortions, and fundamental voltage losses [63, 64]. To compensate the dead-time effect, a modified PWM switching sequence has been proposed in [27]. However, the switching loss is found 50% higher than conventional ones which makes this method undesirable, especially for PV inverters with efficiency as a key consideration. Therefore, passive CM filters are still necessary for ZCMV PWMs. Rather than applying a full-size CM filter, dead-time effect can be eliminated by other passive filtering options. In this section, an alternative solution has been proposed by using DC neutral-point connected LCL (NP-LCL) filters for dead-time mitigation [67]. With NP-LCL, CM harmonics caused by dead-time can be eliminated without introducing extra passive filtering elements. Design and implementation of the NP-LCL are detailed first, where the performance of NP-LCL has been compared to conventional LCL considering both DM and CM performances. Efficacy of the proposed method is verified by experimental results obtained from a lab-scale DSP-based 3L-NPC platform.

2.2.1. Conventional LCL vs. NP-LCL filters

As the most preferable passive DM filtering solutions, conventional LCL filter can be found in most of the three-phase string PV inverters [65, 66]. For inverters adopted conventional LCL filters, CM chokes are usually required to suppress the leakage currents caused by dead-time. It

is found in studies that NP-LCL filter is another DM filtering option, which can provide extra leakage current suppression capability at no extra cost. NP-LCL can be implemented by connecting filter capacitors' neutral-point to the inverter's DC midpoint.

To compare these two filtering solutions, DM performance is considered first since the primary goal of these filters is to eliminate the high-frequency DM harmonics. As shown in Fig. 2.6, NP-LCL shares the same DM equivalent circuit with conventional LCL. The DM harmonics attenuation rate Att_{DM} can be derived accordingly in (2.3), where L_i denotes the inverter-side filter inductance; L_g denotes the grid-side filter inductance; C_f denotes the filter capacitance.

$$Att_{DM} = \frac{1}{(C_f L_i L_g)s^3 + (L_{i+} L_g)s} \tag{2.3}$$

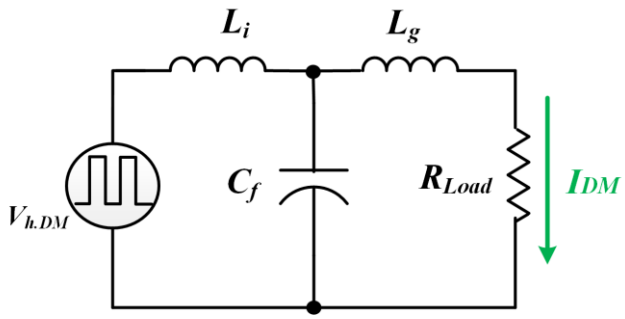


Fig. 2.6. DM equivalent circuit of the conventional LCL or NP-LCL filters

Considering CM on the other hand, only one-third of the DM filter inductance appears in the CM loop. CM equivalent circuit of LCL and NP-LCL filter can be found in Fig. 2.7(a) and Fig. 2.7(b). Compared to the conventional LCL, NP-LCL has better CM harmonics suppression capability because majority of the leakage current I_{NC} will be bypassed through the neutral-point connected capacitor. The leakage current division ratio $I_{NC} : I_{CM}$ depends on the CM impedance ratio of $Z_{3Cf} : Z_{Lg/3+Cg}$. High-frequency CM harmonics will see lower impedance of Z_{3Cf} at the shunt capacitive branch, thus get by-passed from the output path. As will be shown, effectiveness

of the NP-LCL on suppressing leakage current has been verified by simulation and experimental results.

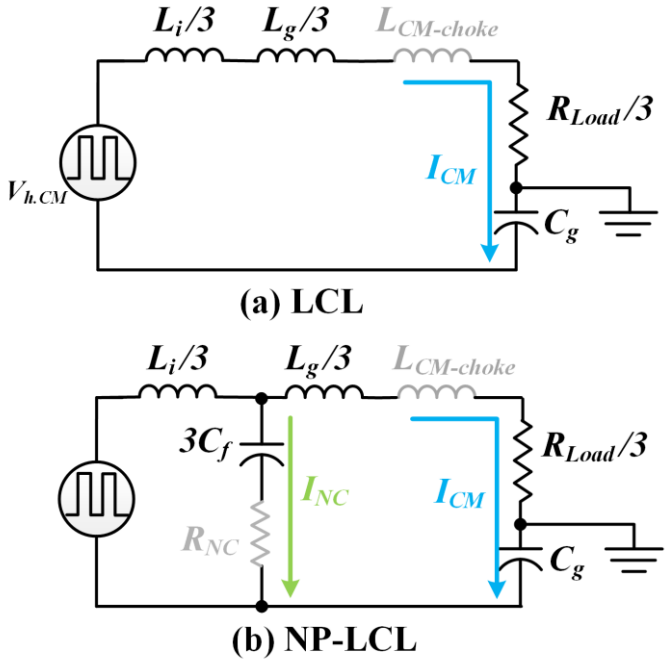


Fig. 2.7. CM equivalent circuit of (a) conventional LCL filter (b) NP-LCL filter.

In addition, it is better to insert CM chokes to grid side as long as the uncoupled DM inductors are adopted in NP-LCL. As shown in Fig. 1.4, such design has been widely adopted in multi-stage output filters [68] because the size of CM choke can be further reduced when moved from inverter side to the grid side. To prevent the potential oscillations between two neutral points, CM choke should be designed to ensure that resonance frequency is different from the triplet multiples of fundamental frequency. A damping resistor R_{NC} can be inserted in between the inverter midpoint and filter neutral point to provide necessary damping [69]. CM attenuation rate of conventional LCL $Att_{CM(LCL)}$ and NP-LCL filter $Att_{CM(NP\text{-}LCL)}$ are derived in (2.4) and (2.5) respectively, where the optional CM choke and R_{NC} are not included in the derivation.

$$Att_{CM(LCL)} = \frac{3C_g s}{(L_i+L_g)C_g s^2+R_l C_g s+3} \tag{2.4}$$

$$Att_{CM(NP-LCL)} = \frac{3C_g s}{L_i L_g C_f C_g s^4+LiR_l C_f C_g s^3+(3L_i C_f+L_i C_g+L_g C_g)s^2+ R_l C_g s+3} \tag{2.5}$$

To evaluate the CM performance of NP-LCL filters, simulations are performed with LCL and NP-LCL filters that sharing the same filter parameters of 2.5mH/5μF/2.5m. Frequency domain responses of LCL and NP-LCL are plotted in Fig. 2.8. One can see, NP-LCL can provide better attenuation to high-order CM harmonics than conventional LCL with the same filter parameters. For example, if the carrier frequency is 9 kHz, NP-LCL can provided 145.6 dB larger attenuation to dominant CM harmonic than with conventional LCL filter.

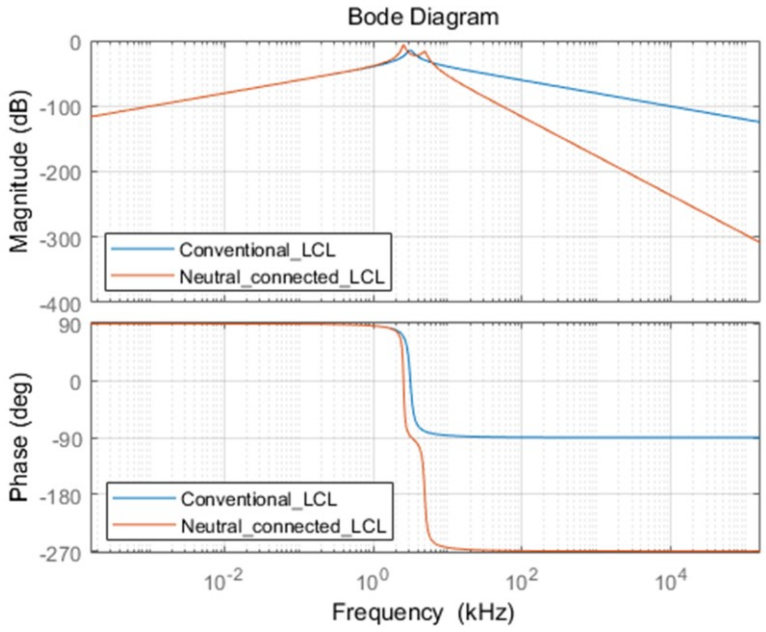


Fig. 2.8. Common-mode frequency domain response of the conventional LCL filter (orange) and NP-LCL filter (blue) with the same filter paramters of 2.5mH/5μF/2.5mH.

From above analysis, one can see NP-LCL has better CM performance than conventional LCL, which can be applied to eliminate dead-time effect on ZCMV PWMs. The size of CM

choke can be reduced in an effectively way since the dominant high-order CM harmonics get well attenuated. Experimental results will be presented in the next subsection for verification. As will be shown later, no CM choke is required if ZCMV PWM is combined with an optimal designed NP-LCL filter to comply with IEEE1547 and IEC-62109. With the proposed dead-time mitigation strategy, system power density is improved at no extra cost while the system reliability gets enhanced.

2.2.2. Experimental verification

To verify the effectiveness of the proposed dead-time mitigation strategy, 1kW experiments have been performed on a lab-scale grid-connected 3L-NPC platform. The experimental prototype can be found in Fig. 2.9. In this design, power from a 140V DC supply is injected into $80V_{rms}$ AC grid through the inverter. Power controllers and ZCMV PWM strategy are implemented in DSP TMS320F28335. The sampling frequency is 9kHz with 3us dead-time implemented for both methods. A 0.15uF grounding capacitor is inserted in between AC grounding point and inverter DC neutral-point, which representing the worst-case scenario with the largest leakage current. Two filtering options, conventional LCL and NP-LCL, are considered in this design with the same filter parameters adopted: 0.8mH (L_i) / 15μF (C_f) / 0.8mH (L_g). With uncoupled inductors applied, one-third of the filter inductance is naturally applied in the CM loop. Thus, no extra CM choke has been applied in this setup.

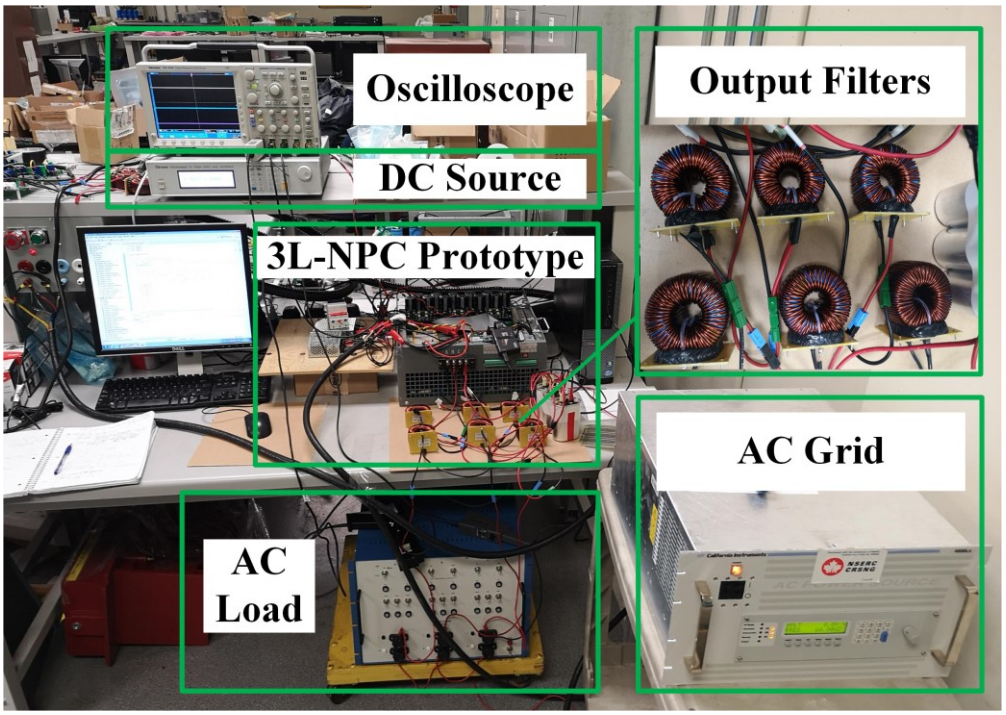


Fig. 2.9. Experiment setup and hardware prototype.

Fig. 2.10 shows the experimental results of ZCMV PWM with a conventional LCL filter adopted. With 3μs dead-time applied, CMV spikes with a peak of 23.3 V are observed which causes 63.3 mA leakage current in RMS. Frequency domain analysis indicates the dominant CM harmonic appears at 153rd order with a magnitude of 0.13A. Considering DM sidebands, only 0.22% DM harmonics appear at 151st order. The magnitude is less than the maximum grid code allowance of 0.3% as specified in IEEE1547. With the NP-LCL design adopted, the dominant CM harmonics at 153rd order get well attenuated to below 0.01%. As shown in Fig. 2.11, clean output current waveforms are observed when the leakage current is reduced down to 12.9 mA in RMS. As will be shown in the next section, IEC-62019 can be satisfied without requiring extra CM choke when NP-LCL is combined with ZCMV. The experimental results agree with the analysis, which indicate NP-LCL filter can provide the desirable DM performance and a better

CM performance in the transformerless T-type 3L-NPC string PV inverters. Effectiveness of the proposed dead-time mitigation strategy is verified.

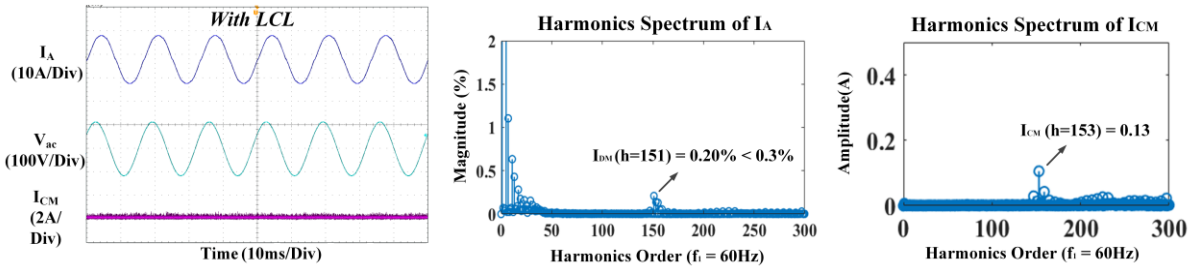


Fig. 2.10. Experimental waveforms of ZCMV PWM with conventional LCL: phase A output current I_A (10A/div), phase A grid voltage V_{ac} (100V/div), CM current I_{CM} (5A/div). Harmonic spectrum of output current I_A (% of rated) and measured CM current I_{CM}(A).

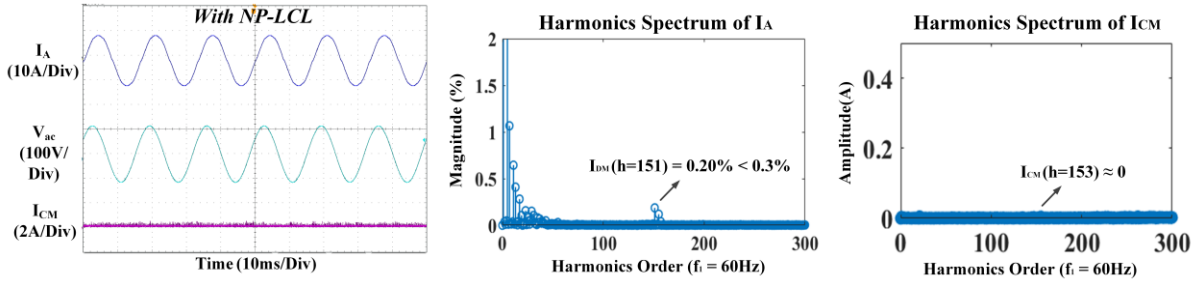


Fig. 2.11. Experimental waveforms of ZCMV PWM with NP-LCL: phase A output current I_A (10A/div), phase A grid voltage V_{ac} (100V/div), CM current I_{CM} (5A/div). Harmonic spectrum of output current I_A (% of rated) and measured CM current I_{CM}(A).

2.3. Impact of ZCMV PWM on output filter volume

As shown in the previous analysis, passive output filters are essential to transformerless string or multistring PV inverters. DM output filters are designed to mitigate DM harmonics, while CM filters are implemented to deal with CM harmonics. The filter parameters need to be carefully designed to satisfy the grid codes IEEE1547 and IEC-62109. On the other hand, ZCMV PWM is proposed to reduce the CMV effects and to scale-down the size of CM filters. With the

proposed dead-time mitigation strategy applied, size of CM filters can be further reduced. However, the DM output quality is undermined which will result in larger DM filters. As most of the existing/ongoing research focused on how to reduce the CMV effects or the size of CM filters, the real impact of the ZCMV PWM on the total output filter volume (DM + CM) has not yet been investigated in the transformerless PV inverters.

In order to evaluate the resultant filter volume of ZCMV PWM, a comparative study has been carried out between the conventional PD and ZCMV PWM methods. For either modulation methods, two DM filtering options can be selected, i.e. the conventional LCL and neutral-point connected LCL (NP-LCL) filter, which results in four designs: 1) PD with LCL, 2) PD with NP-LCL, 3) ZCMV with LCL, and 4) ZCMV with NP-LCL. In this work, different power ratings are considered where studies are conducted on a 10kW and a 100kW three-phase T-type 3L-NPC inverter systems for analysis. An applicable filter parameter design procedure has been developed, which makes it possible to fairly compare the resultant filter size of different cases. With output filter parameters properly designed under the same framework for all the cases, volume of the resultant filters is estimated and compared accordingly. The study indicates DM filter dominants the total filter volume in the studied PV inverter systems. Size of the CM choke can be minimized with ZCMV PWM but at the cost of significant larger DM filters. The total filter volume for ZCMV PWM is at least 1.5 times larger than PD which reveals the PV inverter's power density cannot be improved with ZCMV PWM. All the designs and analysis are verified by MATLAB simulation, which will be presented in this section.

2.3.1. Filter parameters design procedure

In this study, two filtering options, LCL and NP-LCL, are considered when modulated with PD and ZCMV PWM methods. To fairly compare the resultant filter size of two PWM methods,

a common filter parameter design framework has been developed, which takes both the CM and DM performances into consideration.

1) Inverter-side filter inductance

The inverter-side inductance L_i can be determined first based on the maximum output current ripple allowance. Commonly, the peak-to-peak current ripple should fall in the range between 20% to 50% of its rated value. For T-type 3L-NPC inverters modulated with PD PWM, the minimum inverter-side inductance can be calculated by (2.6), where ΔI_{pk} denotes the peak value of maximum allowable ripple. The derivation is based on the volt-seconds balance law presented in [70].

$$L_i = \frac{V_{dc}}{12\Delta I_{pk} f_{cr}} \tag{2.6}$$

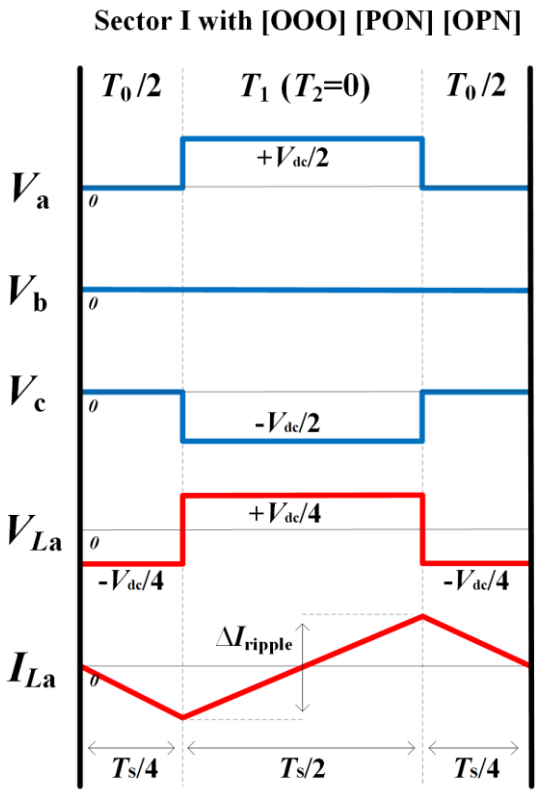


Fig. 2.12. Inductor voltage V_{La} and current I_{La} waveforms (phase A) of 3L-NPC inverter with ZCMV PWM.

For T-type 3L-NPC modulated with ZCMV PWM, inverter-side inductance can also be derived from its maximum volt-second. As shown in Fig. 2.12, largest ripple current will be produced in phase A if dwell-time T_2 of [OPN] is zero. At the monument, T_0 and T_1 equal to $T_s/2$, where the average capacitor voltage equals $V_{dc}/4$. From there, the minimum inverter-side inductance L_i for ZCMV method can be derived in (2.7).

$$L_i = \frac{V_{dc}}{8\Delta I_{ripple} f_{cr}} \tag{2.7}$$

2) Filter capacitance

In this design, relatively large filter capacitance is preferable in NP-LCL filter because larger capacitance can create a CM loop with lower impedance to bypass the leakage current and to reduce the size of CM choke. Therefore, maximum allowable filter capacitance should be selected in this design. To avoid low power factor and over 5% of reactive power loss, filter capacitance should be less than the boundary value specified in (2.8).

$$C_f \leq \frac{5\%\, P_n}{V_{grid}^2 \omega_{grid}} \tag{2.8}$$

Note that there is a trade-off between filter inductance and capacitance. When filter capacitance is selected at its upper boundary, minimum inductance is required to achieve desired attenuation to DM harmonics.

3) Grid-side filter inductance

To comply with grid code of IEEE1547, specific amount of DM filter inductance is required to achieve certain attenuation to DM harmonics. In this design, the worst-case scenario specified in Table 2.1 has been considered where the high-order harmonics (above 35^{th} order) should be eliminated to below 0.3% of its rated. Since the largest DM harmonics

appear near carrier frequency f_{cr} and its multiples, harmonics above 35th order can be eliminated as long as the dominant sideband at f_h get properly attenuated [68].

Table 2. 1. Current Harmonic Limits Specified by IEEE1547

Maximum odd harmonics current in percentage of rated output current						
Individual odd order harmonics	**h≤11**	**11<h≤17**	**17<h≤23**	**23<h≤35**	**35≤h**	**THD with h≤50**
%	4.0	2.0	1.5	0.6	0.3	5.0

Desired DM attenuation rate Att_{DM_req} can be calculated in (2.9), where $I_{IEEE1547}$ denotes the high-order harmonics target which is 0.3% of base current; V_h denotes the magnitude of the DM harmonic voltage at lower sideband.

$$Att_{DM\_req} = \frac{I_{IEEE1547}}{V_h(f_h)} \tag{2.9}$$

With L_i and C_f determined from previous steps, the grid-side inductance L_g can be obtained by solving (2.3) at frequency f_h. Since LCL or NP-LCL filters provides 60 dB/dec attenuation to high-order DM harmonics, the value of L_g can be approximated with (2.10) by ignoring the low-order terms.

$$L_g \approx \left| \frac{1}{C_f L_i (2\pi f_h)^3 Att_{DM}} \right| \tag{2.10}$$

Damping might be required to deal with potential resonance. Oscillations caused by LCL or NP-LCL filters can be prevented with various damping techniques such as passive damping methods [70] or active damping methods [71, 72].

From above three-step design procedure, DM filter parameters for different scenarios can be determined, while the impact of different modulation methods on filter volume can be fairly compared. Desired DM performance can be achieved which satisfying IEEE1547. The output current ripple will be within the allowance. In additions, leakage current can be well suppressed

with NP-LCL which can lead to a smaller CM choke. From there, a fair comparison of the resultant filter volume can be performed between PD and ZCMV PWM methods.

2.3.2. Comparison of the resultant filter volume

To investigate the impact of ZCMV PWM on total filter volume, comparative study is carried out between the convention PD and ZCMV PWM methods. Two filtering options are considered which leads to four designs: 1) PD with LCL, 2) PD with NP-LCL, 3) ZCMV with LCL, and 4) ZCMV with NP-LCL. The resultant filter volume of PD and ZCMV are estimated and compared. Since the focus of this study is on practical string or multistring PV inverters rated below 100kW, two sets of the comparison are performed on 10kW and 100kW cases. The system parameters are specified in Table 2.2.

Table 2. 2. Electrical Specifications of a Grid-Tied Three-Phase T-Type 3L-NPC PV Inverter System

Symbol	Electrical Parameter	Design Value
V_{grid}	Line-to-line main RMS voltage	380 V_{rms} ($\pm$10%)
V_{dc}	Nominal DC-link voltage	700 V ($\pm$10%)
f_{cr}	Carrier frequency	9 kHz
f_{grid}	Grid fundamental frequency	60 Hz
P_n	Rated active power from DC to AC	10 kW / 100 kW
I_{rated}	Rated output current in RMS	15.2 A_{rms} / 151.9 A_{rms}
C_g	Ground capacitance of a PV system	1.5 μF / 15.0 μF

Output filters are designed based on the same filter parameter design criteria. Filter parameters are determined through the procedure developed in Section 2.3.1. To fairly compare the resultant filter size of two PWMs, maximum of 20% output current ripples are allowed in all the designs. DM filter parameters are summarized in Table 2.3. To better suppress the leakage current, relatively large filter capacitance (5% of based capacitance) is chosen for both modulation schemes. For filter inductance, ZCMV requires larger DM inductance because

portion of the CM harmonics are transferred into DM causing larger DM distortion. To achieve the desired DM attenuation with ZCMV, filter inductance required in case 3) and 4) is 1.7 times larger than with PD in case 1) and 2). Effectiveness of the output filters designed for this comparative study has been verified by MATLAB simulation, which is detailed in the next subsection.

Table 2. 3. Parameters Selection for LCL & NP-LCL Filters

Designed for a 10 kW PV Inverter			
Symbol	**Electrical Parameter**	**PD PWM (case 1, case 2)**	**ZCMV PWM (case 3, case 4)**
L_i	Inverter-side inductance	1.5 mH	2.3 mH
L_g	Grid-side inductance	0.6 mH	1.2 mH
C_f	Filter capacitance	9.2 μF	9.2 μF
Designed for a 100 kW PV Inverter			
Symbol	**Electrical Parameter**	**PD PWM (case 1, case 2)**	**ZCMV PWM (case 3, case 4)**
L_i	Inverter-side inductance	0.15 mH	0.23 mH
L_g	Grid-side inductance	0.06 mH	0.12 mH
C_f	Filter capacitance	91.8 μF	91.8 μF

To better analyze the size difference of filter inductors, it is necessary to study the relationship between DM filter inductances and their core volumes. Note that inductor volume can be estimated with the box volume of its magnetic core. In this study, widely applied C-type core is selected for study. Area product A_p (in cm^4) is an important factor in design of the DM inductors, where A_p is the product of the available window area W_a (in cm^2) and the effective cross-section area A_c (in cm^2). According to its definition, A_p is proportional to the fourth power of core linear dimension l (in cm). Since the core box volume Vol (in cm^3) is proportional to l^3, relationship between core volume and area product can be obtained as

$$Vol \propto l^3 \propto {A_p}^{0.75} \tag{2.11}$$

At the same time, core volume is determined by how much energy it can handle. According to [73], energy handling capability of a core is related to its area product A_p. This relationship can

be described by (2.12), where B_m is the flux density in Tesla; K_u denotes window utilization factor (which is 0.4 in most cases); K_j denotes the current density efficiency.

$$A_p = \left(\frac{2E_L \times 10^4}{B_m K_u K_j}\right)^{1.14} \quad where \;\; E_L = \frac{1}{2} L I_m^2 \tag{2.12}$$

Core energy is represented by E_L (in J), where I_m is the peak current through inductor; L is the desired inductance in H. Assume I_m is constant, there is a positive correlation between DM inductance and core volume as described in (2.13)

$$Vol \propto L^{0.855} \tag{2.13}$$

Back to the previous comparative study, ZCMV requires 1.7 times larger DM inductance than PD method at 10kW or 100kW, which will result in 1.6 times larger core volume according to (2.13). In other words, ZCMV will lead to significantly larger DM filters in string PV inverters, which can potentially increase the total passive filter volume.

Although DM filter is the dominant factor, CM choke should also be considered when comparing the total filter volume. CM inductance can be designed based on the CM equivalent circuit derived in Fig. 2.7. To eliminate the leakage current to below 300mA (as specified in IEC-62109), CM inductance required can be calculated with the amplitude of dominant high-order CMV components estimated in Section 2.12. CM inductances selected for each case are presented in Table 2.4. Since majority of the leakage current can be supressed with NP-LCL filter, size of the CM choke can be significantly reduced in case 2) and 4). Considering the resultant output filter volume, CM choke becomes less comparable with DM filter. Although size of CM choke can be further reduced with ZCMV PWM (as in case 4), at least 1.6 times larger DM inductors will be required than PD, which will result in a larger total filter volume. Among all the designs, total filter volume can be minimized with PD and NP-LCL in case 2), because PD requires smaller DM filter while NP-LCL leads to a smaller CM choke.

To further investigate the impact of ZCMV PWM on filter volume, total filter volumes (DM+CM) are estimated and compared based on the magnetic core selections. In this comparison, only inductive filters are considered because capacitor volumes are identical at certain power ratings. Different cores are selected to achieve the desired CM and DM inductance. The total inductor volumes are estimated by the sum of the cores' box volume for each case. In this study, a widely applied industrial Core Design and Select Tool developed by Hitachi [74] is referred when making the core selection. Toroidal core made with nanocrystalline material is selected for CM inductor while iron-based amorphous C-type core is chosen for DM inductors. Total core volume (CM+DM) can be easily estimated according to the core selections. Core selections and volume estimation for all studied cases are summarized in Table 2.4. In case 2) and 4), NP-LCL filter results in a smaller CM choke compared to cases with conventional LCL filter. CM inductor can be further reduced with ZCMV PWM in case 4), however results in larger total filter volume. Taking cases 2) and 4) at 10 kW for example, size of the CM filter is reduced from 6.2 cm^3 to zero by applying ZCMV PWM; however, the core size of DM inductors increase from 822.9 cm^3 to 1277.7 cm^3 causing the total inductor volume increased from 829.1 cm^3 to 1277.7 cm^3.

According to above core-volume analysis, DM filter dominates the total filter volume for the studied string PV inverters. At 10 kW, ZCMV method results in 1.54 times larger output filter than with PD, which shows good accordance with analytical results of 1.6 times. Similar conclusions can be drawn from 100 kW designs, where the total core volume of ZCMV method is about twice larger than PD. Above comparative study indicates ZCMV PWM can minimize the size of CM choke but at the cost of a larger DM filter, which will cause the overall filter volume to increase.

Table 2. 4. Core Selections and Volume Comparison of the Inductive CM & DM Filters

Power Rating = 10kW		**DM Inductor Core Design**			**CM Inductor Core Design**			**Total Core Volume for 10kW Design (cm^3)**
#	PWM Methods & Filter Types	L_i & L_g (mH)	Core Type	Core Box Volume (cm^3)	L_{CM} (mH)	Core Type	Core Box Volume (cm^3)	
1)	PD+LCL	L_i = 1.5	AMCC80	212.2	6.0	F1AH0048	10.4	833.3
2)	PD+NP-LCL	L_g = 0.6	AMCC26S	62.1	0.5	F1AH0047	6.2	829.1
3)	ZCMV+LCL	L_i = 2.3	AMCC125	266.8	0.1	F1AH0047	6.2	1283.9
4)	ZCMV+NP-LCL	L_g = 1.2	AMCC63	159.1	0.0	NA	NA	1277.7
Power Rating = 100kW		**DM Inductor Core Design**			**CM Inductor Core Design**			**Total Core Volume for 100kW Design (cm^3)**
#	PWM Methods & Filter Types	L_i & L_g (mH)	Core Type	Core Box Volume (cm^3)	L_{CM} (mH)	Core Type	Core Box Volume (cm^3)	
1)	PD+LCL	L_i = 0.15	AMCC800B	1317.5	7.0	F1AH0023	725.8	5996.2
2)	PD+NP-LCL	L_g = 0.06	AMCC367S	439.3	1.8	F1AH0052	270.4	5540.8
3)	ZCMV+LCL	L_i = 0.23	AMCC664	2468.7	0.6	F1AH0019	102.4	11461.0
4)	ZCMV+NP-LCL	L_g = 0.12	AMCC800B	1317.5	0.0	NA	NA	11358.6

***** Core selection criteria [74]: fundamental frequency 60Hz (DM inductors) / 9 kHz (CM inductors), nominal RMS current 15.2A and 151.8A, ambient temperature 55°C, maximum operation temperature 130°C, maximum flux 1 Tesla, window fill factor 0.4, current density factor 800A/cm^2.

2.3.3. Simulation verification

To verify the filter design and previous analysis, simulations have been performed on the four cases studied, i.e. 1) PD with LCL, 2) PD with NP-LCL, 3) ZCMV with LCL, and 4) ZCMV with NP-LCL. The grid-tied transformerless T-type 3L-NPC string PV inverter system in Fig. 1.4 is modeled in MATLAB Simulink. Simulation parameters are specified in Table 2.2. In this design, active power is transferred from DC-link to AC grid through the studied T-type 3L-NPC inverter. Simulation tests are conducted on PV inverter systems rated at 10 kW and 100 kW respectively. To make fair comparisons, 3 μs dead-times are applied to all cases. The worst-case scenario is simulated by selecting the PV leakage capacitance C_g (50 – 150 nF/kW) at its upper boundary [35], which will result in the largest leakage currents. A proportional zero-sequence current controller is implemented to eliminate the low-order CM harmonics, while CM filters are designed to attenuate the high-order CM harmonics in order to comply with IEC-62019. DM

filters are designed to eliminate the inverter-side current ripple to below 20% and to comply with IEEE1547. Filter parameters are adopted from the comparative study detailed in Table 2.3.

At power rating of 10kW, desired DM performances have been achieved in all the four designs. Frequency domain analysis indicates the dominant high-order DM harmonics are less than 0.3%, which comply with IEEE1547. Fig. 2.13 and Fig. 2.14 are simulation results of case 1) and case 2) respectively when modulated with PD PWM. Three-phase output currents and CM harmonics are measured. Dominant CM harmonic is observed at 150th order whose magnitude depends on the type of output filter. With conventional LCL filter, 3.51 A leakage current is measured, which requires a 6 mH CM choke to eliminate it to below 300 mA to comply with IEC-62109. With NP-LCL filter, only 0.5 mH CM choke is required to achieve the same CM performance. Fig. 2.15 and Fig. 2.16 provide the simulation results of case 3) and case 4) where SVM-based ZCMV method is adopted. Considering the impact of dead-time, 0.1mH CM choke is required for case 3) when conventional LCL filter is adopted. With NP-LCL filter, CM choke can be eliminated since the leakage current is only 52 mA (< 300 mA) in RMS. With ZCMV

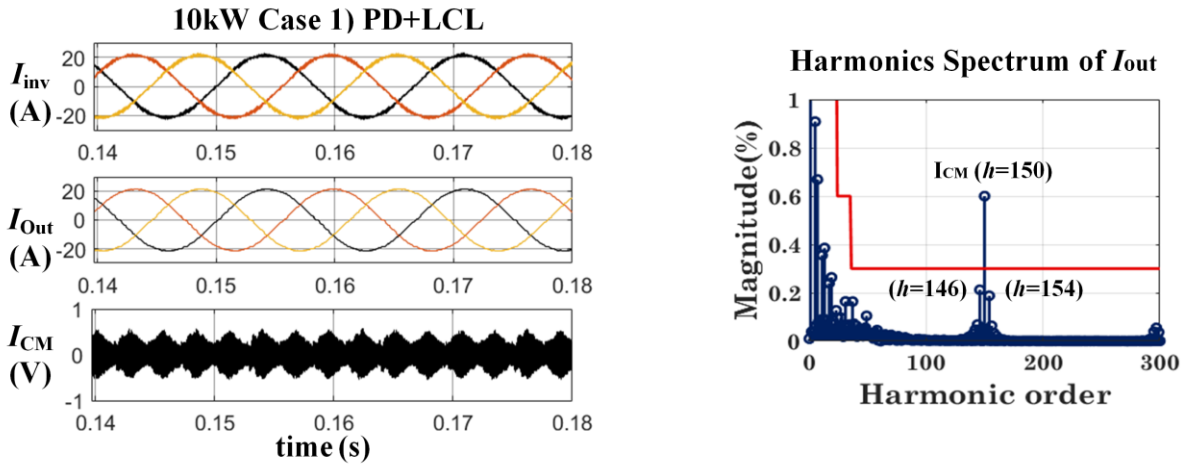


Fig. 2.13. Simulation results of case 1) at 10kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A output current and IEEE1547 standard (red).

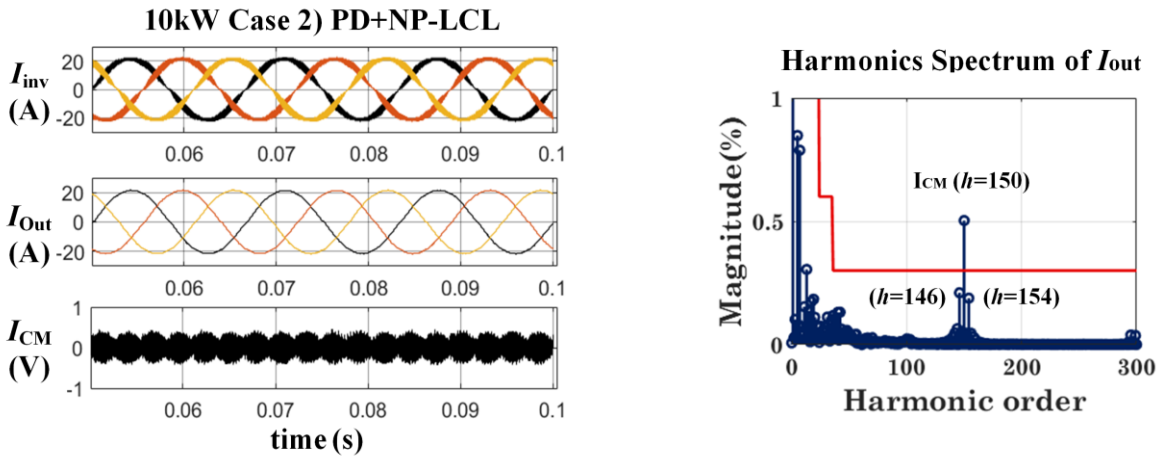


Fig. 2.14. Simulation results of case 2) at 10kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A output current and IEEE1547 standard (red).

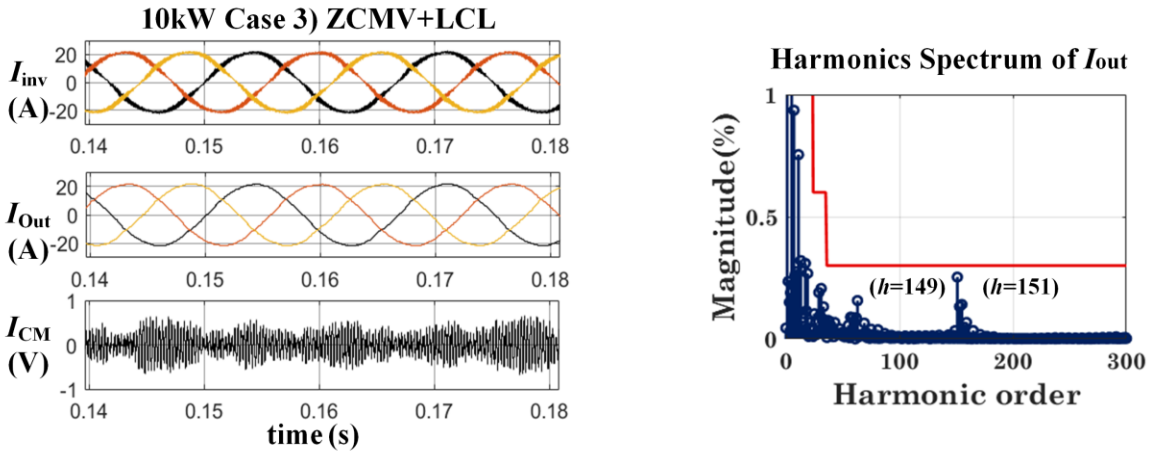


Fig. 2.15. Simulation results of case 3) at 10kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A output current and IEEE1547 standard (red).

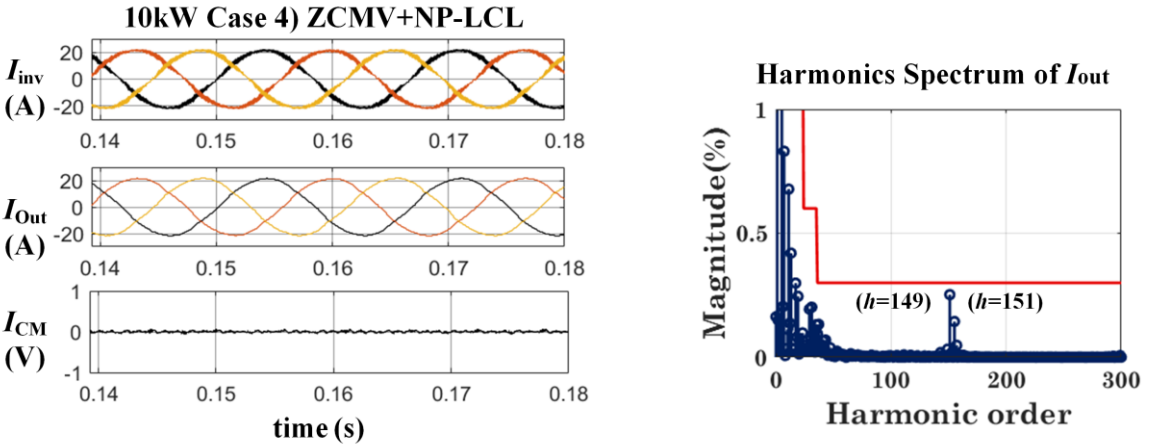


Fig. 2.16. Simulation results of case 4) at 10kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A output current and IEEE1547 standard (red).

modulation, size of CM choke is significantly reduced but at the cost of 1.6 times larger DM inductors which is undesirable.

To better investigate the performance of difference designs at higher power ratings, identical studies are conducted on string PV inverter rated at 100kW. With DM filters and CM chokes redesigned, similar simulation results are obtained in Fig. 2.17 to Fig. 2.20. IEEE1547 is satisfied in all cases since high-order DM harmonics are less than 0.3%. CM chokes are properly designed to comply with IEC-62109. It has been found that larger leakage currents are produced at 100 kW, which result in slightly larger CM filters than the 10 kW cases. In addition, ten times smaller DM inductances are required at higher power ratings according to the design. Comparing the four 100kW cases, ZCMV with NP-LCL filter provides the best leakage current suppression, which requires the smallest CM choke but with a larger DM filter. Filter design are validated by simulation results, which indicates ZCMV modulation can lead to larger output filter than PD PWM in transformerless string PV inverters.

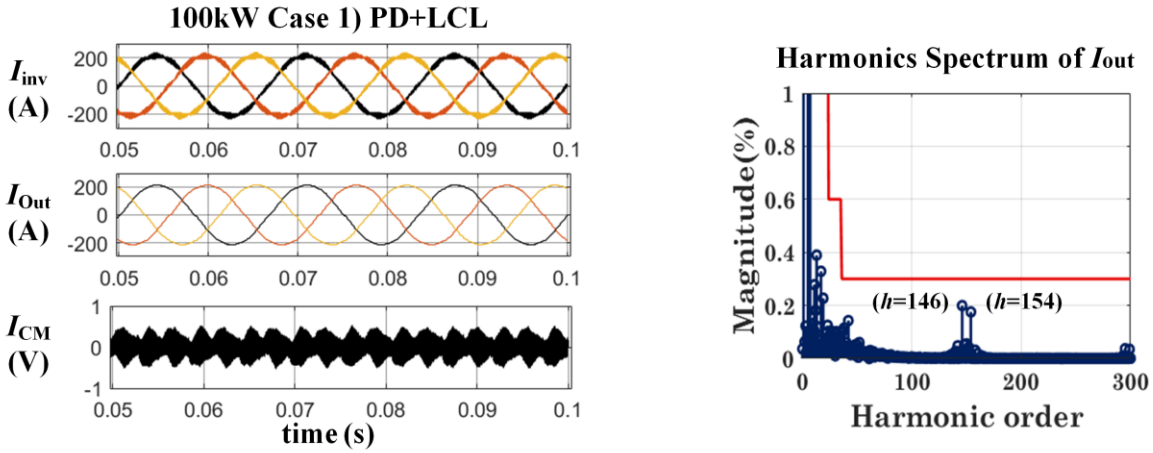


Fig. 2.17. Simulation results of case 1) at 100kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A current and IEEE1547 standard (red).

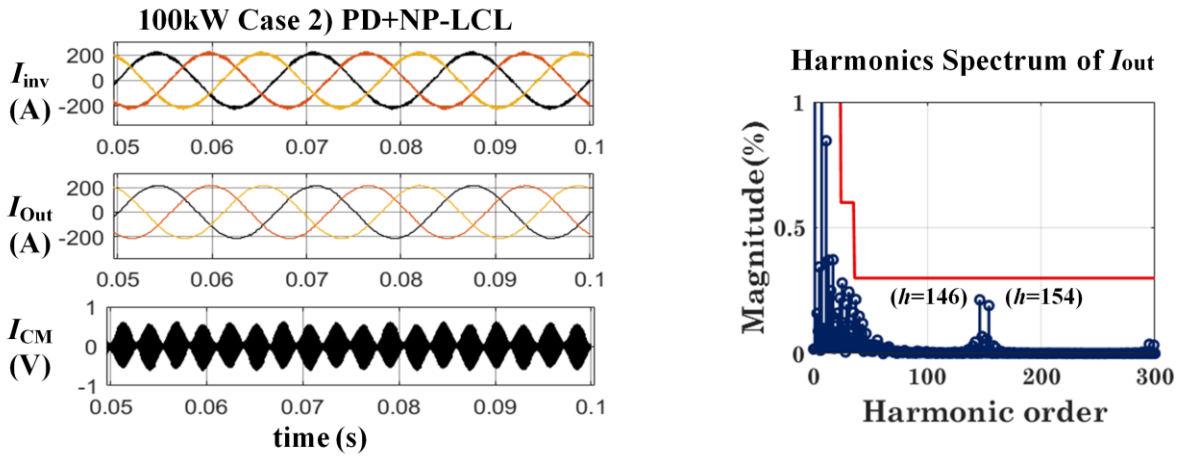


Fig. 2.18. Simulation results of case 2) at 100kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A current and IEEE1547 standard (red).

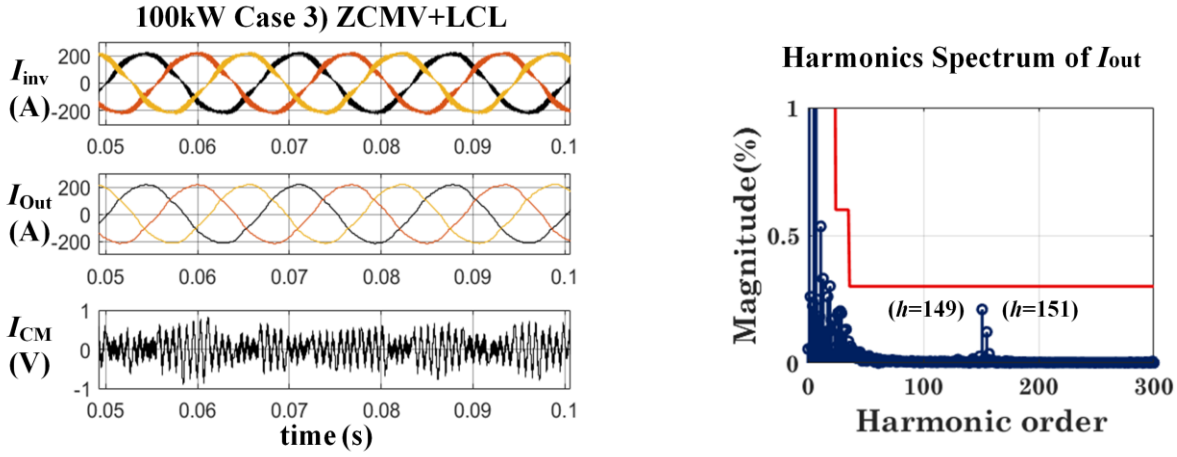


Fig. 2.19. Simulation results of case 3) at 100kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A current and IEEE1547 standard (red).

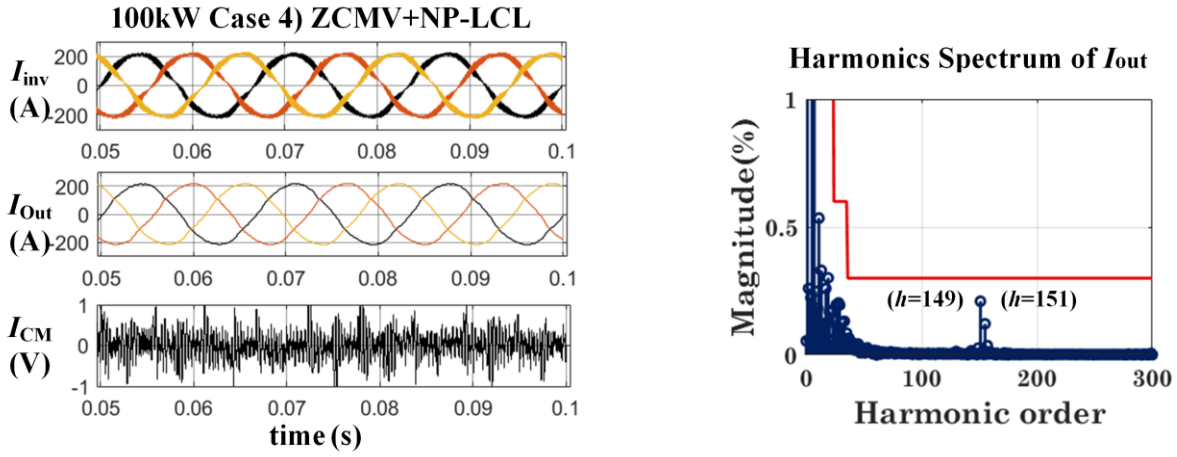


Fig. 2.20. Simulation results of case 4) at 100kW: inverter-side current I_{inv}, grid-side output current I_{Out}, and leakage current I_{CM}. Harmonic spectrum of phase A current and IEEE1547 standard (red).

2.4. Summary

This chapter presents a comprehensive evaluation of ZCMV modulation in transformerless T-type 3L-NPC PV inverters. The study focuses on two aspects, i.e. dead-time effect and resultant filter volume. Impact of dead-time has been thoroughly investigated first, which indicates CMV spikes caused by dead-time are inevitable to ZCMV PWMs. CM filter will be required to mitigate the dead-time effect when modulated with ZCMV PWMs. An alternative dead-time mitigation strategy has been proposed by using DC neutral-point connected LCL (NP-LCL) filter. The analysis indicates NP-LCL has better CM performance than conventional LCL filter, which can be applied to mitigate the dead-time effect. The proposed method is easy to implement in PV inverters without introducing extra passive filtering elements.

To investigate the actual impact of ZCMV PWM on the total output filter volume, comparative studies are conducted on four designs i.e. 1) PD with LCL, 2) PD with NP-LCL, 3) ZCMV with LCL, and 4) ZCMV with NP-LCL. The resultant filter volumes have been fairly compared, which indicates the total filter volume of ZCMV is larger than PD. Size of CM choke can be reduced with ZCMV but at the cost of larger DM filter. In the studied cases, ZCMV results in at least 1.5 times larger total filter volume than PD. On the other hand, leakage currents are well controlled by NP-LCL filters at various power ratings when combined with either PWM methods. Considering dead-time effect and larger DM filter requirement, ZCMV PWM method becomes less applicable in transformerless string or multistring PV inverters rated from 10kW to 100kW, where DM inductor dominants the overall filter volume. Design and analysis of the proposed study have been verified by simulation and experimental results.

Chapter 3 Interleaved Carrier-Based MPC for Modular Parallel VSIs

As discussed in the last Chapter, CMV effects can be reduced with ZCMV PWMs but at the cost of larger DM filters. In fact, CM filters are still required for ZCMV due to the inevitable dead-time effect. Even with an optimal designed NP-LCL filter, the total filter volume of ZCMV is still significantly larger than the conventional PWM method, which makes ZCMV PWM methods less applicable. Alternatives are explored, among which, the interleaved PWM has been found as an effective way to reduce CMV effects in central or multistring PV inverters with multiparalleled VSIs. However, as introduced in Chapter 1, low-frequency (LF) zero-sequence circulating current (ZSCC) is identified as the major challenge for such systems, which requires to be properly addressed.

In this chapter, a centralized carrier-based model predictive control scheme (CB-MPC) has been proposed to achieve full elimination of LF-ZSCC in modular parallel VSIs. The proposed method is a centralized MPC scheme that adopting carriers to realize interleaved PWM. Compared to the existing MPC-based ZS control schemes [57-62], CB-MPC is more applicable and more flexible, which can be implemented either in a dedicate central controller or in each converter's local controllers. In this study, 2L-VSI has been selected for illustration, where the proposed method is also applicable to modular parallel multilevel VSIs for LF-ZSCC control. A generalized ZSCC model has been derived, which allows the proposed method to be applied to N modular parallel VSIs. Output power can be individually controlled for each inverter module. LF-ZSCC caused by hardware parameters mismatch and unequal power sharing are fully eliminated, which enables the interleaved PWM to be implemented to reduce the CMV effects.

Design and implementation of the proposed method are detailed in this chapter. Simulation and experimental results are provided for verification of the proposed method.

3.1. Modeling of *N* modular paralleled 2L-VSIs

As MPC requires an accurate system model, this section presents an average output current model for induvial VSI module, followed by a generalized ZSCC model derived for the whole system. 2L-VSI has been selected as an example for illustration. Topology of the studied *N*-paralleled 2L-VSI system can be found in Fig. 1.6. The inverter modules are attached to a common DC-link and directly paralleled at AC side. Since this is a simplified illustration of the modular parallel VSI systems, line resistance is ignored where the filter inductance is considered as the dominant factor for modeling.

3.1.1. Average output current model

Continuous-time current model of the j^{th} inverter (j=1,2…N) has been derived in (3.1), where L_j denotes the filter inductance; v_{aj}, v_{bj}, v_{cj} denote inverter output voltage under three-phase stationary coordinate; i_{aj}, i_{bj}, i_{cj} denote the inverter output current; v_{AO}, v_{BO}, and v_{CO} denote the AC grid voltage; v_{NP} is the neutral-point voltage of the AC grid. The negative pole of DC-link has been taken as the reference point for this derivation.

$$\frac{d}{dt}\begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{cj} \end{bmatrix} = \frac{1}{L_j}\begin{bmatrix} v_{aj} \\ v_{bj} \\ v_{cj} \end{bmatrix} - \frac{1}{L_j}\begin{bmatrix} v_{AO} - v_{NP} \\ v_{BO} - v_{NP} \\ v_{CO} - v_{NP} \end{bmatrix} \tag{3.1}$$

Clark transformation is applied to transfer the average model from the three-phase stationary frame into two-phase synchronous stationary coordinate. The mathematic model of the j^{th} 2L-VSI module has been derived as

$$\frac{d}{dt}\begin{bmatrix} i_{\alpha j} \\ i_{\beta j} \end{bmatrix} = \frac{1}{L_j}\begin{bmatrix} v_{\alpha j} \\ v_{\beta j} \end{bmatrix} - \frac{1}{L_j}\begin{bmatrix} v_{\alpha O} \\ v_{\beta O} \end{bmatrix} \tag{3.2}$$

3.1.2. Generalized zero-sequence circulating current model

In multiparallel inverter systems, ZSCC can be produced due to uneven zero-sequence voltages generated at each module. Research in [53-56] indicates either circuit parameters mismatch or module power output mismatch can cause the inverter modules to produce difference levels of zero-sequence voltage, thus results in LF-ZSCC. In this section, a generalized ZSCC model has been derived to model ZSCC among *N* paralleled inverters.

System in Fig. 1.6 can be simplified by only considering zero-sequence components. Equivalent zero-sequence circuit diagram can be found in Fig. 3.1, where v_{zsj} denotes the zero-sequence voltage generated by the j^{th} inverter module; i_{zsj} denotes ZSCC of the j^{th} module; u_{cmj} denotes the CM harmonics injection on the j^{th} module which is implemented to improve the DC voltage utilization rate by 15%. Phase and amplitude of the CM harmonics injection mainly depend on the original modulation signals for each inverter module.

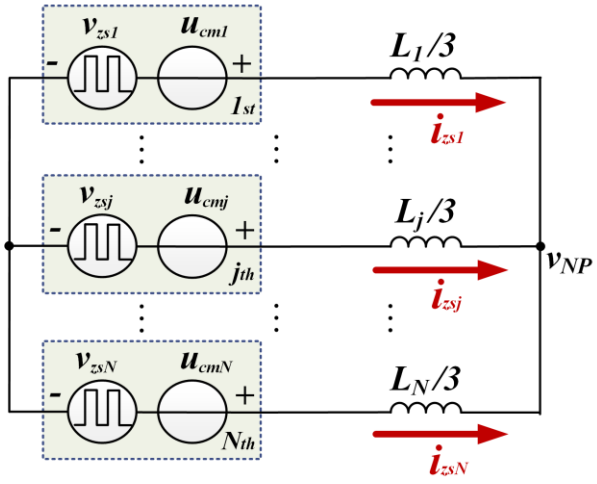


Fig. 3.1. Equivalent zero-sequence circuit diagram of *N* paralleled 2L-VSI modules.

Superposition Theorem indicates ZSCC measured from one module, e.g. i_{zsj}, always equals to the sum of N components produced from all the ZS source. As shown in Fig. 3.2, ZSCC circuit diagram of the j^{th} module can be decomposed into N independent circuits. Total circulating current seen by the j^{th} module can be represented by (3.3).

$$i_{zsj} = \sum_{x=1}^{N} i_{zsxj} \tag{3.3}$$

From the KCL, ZSCC components i_{zsxj} contributed from the module x can be derived in (3.4), where x=1, 2…N. Filter inductances L are assumed to be identical for convenience of analysis. The total equivalent inductance L_t equals $\frac{L}{3} + \frac{L}{3(N-1)}$.

$$i_{zsxj} = \begin{cases} \frac{v_{zsj}+u_{cmj}}{sL_t} & \text{if x = j} \\ -\frac{v_{zsj}+u_{cmj}}{sL_t(N-1)} & \text{if x} \neq \text{j} \end{cases} \tag{3.4}$$

By substituting (3.4) into (3.3), ZSCC model of N paralleled inverters can be derived as

$$L_t \frac{di_{zsj}}{dt} = \frac{N}{N-1}(v_{zsj} + u_{cmj}) - \sum_{x=1}^{N} \frac{v_{zsx}+u_{cmx}}{N-1} \tag{3.5}$$

The above derivation indicates the magnitude of ZSCC is determined by DC-link voltage, filter inductance, CM harmonics injection, and ZS compensations of all modules. The proposed generalized ZSCC module is validated by simulation as detailed in the next subsection.

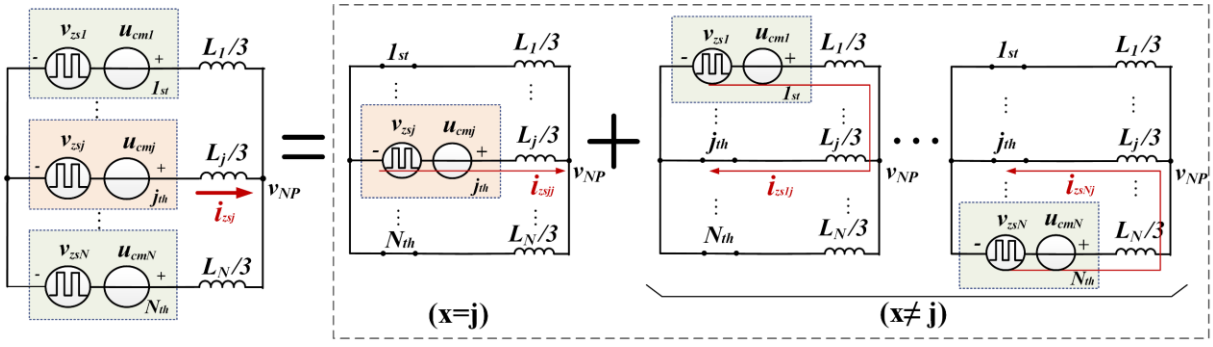


Fig. 3.2. Analysis of ZSCC on the j^{th} inverter module using Superposition Theorem.

3.1.3. Validation of the ZSCC model

To validate the generalized ZSCC model derived in Section 3.1.2, simulation tests are conducted on different multiparallel 2L-VSI systems. ZSCC is first estimated by using the model derived in (3.5), and then compared with the simulation results. The system in Fig. 1.6 is simulated in MATLAB Simulink for different operating conditions, i.e. with even or uneven power sharing, and using different module numbers, i.e. N=3 or N=6.

In the first test, six inverter modules (N=6) are parallel connected at DC side. Each module produces a rated output power of 20kW in the first 0.02s. Inverter #1 is shutdown at t=0.02s, causing 100% power mismatch. During the test, ZSCC has not been controlled. As shown in Fig. 3.3, only HF-ZSCC are measured before t=0.02s. LF-ZSCC can be observed after inverter #1 is switched off. Serious LF-ZSCC is measured from the inverter #1 with an amplitude of 16A. To validate the proposed ZSCC model, the measured value of ZSCC i_{zs_m} is compared with their estimated value i_{zs_est} by using the proposed model. From the zoomed waveforms in Fig. 3.3, one can see the estimated values of ZSCC closely match with their practical values under both even

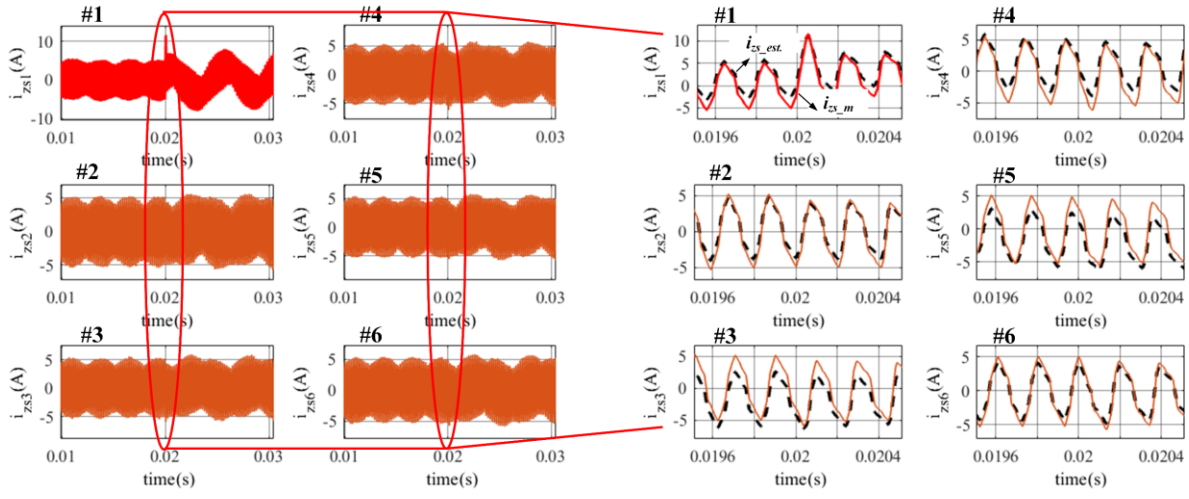


Fig. 3.3. Validation of the generalized ZSCC model in six paralleled 2L-VSIs: measured ZSCC i_{zs_m} (plotted with red/orange solid lines) vs. estimated ZSCC using the proposed ZSCC model $i_{zs\_est.}$ (plotted with black dashed lines). The plot is zoomed at t=0.02s when inverter #1 shutdown.

(t = 0.01s - 0.02s) and uneven even (t = 0.01s - 0.02s) power sharing conditions.

In the second test, three inverter modules (N=3) are parallel connected with rated output of 20kW. Again, module #1 is shutdown at t=0.02s causing 100% power mismatch. During the second test, LF-ZSCC on module #1 and #3 have not been controlled. To better validate the proposed ZSCC model, inverter #2 is controlled to generate a 10A LF-ZSCC with an order of zero. According to the simulation results in Fig. 3.4, zero-order ZSCC on inverter #2 are well regulated to 10A during the test. Third-order ZSCC can be observed on inverter #1 and #3 after t=0.02s due to uneven power sharing. From zoomed Fig. 3.4, the estimated value of ZSCC $i_{zs\_est.}$ using the proposed model matches the practical measurements i_{zs_m} under all operating conditions. The discrepancies caused by negligible loss and sampling delay are minor and within acceptance.

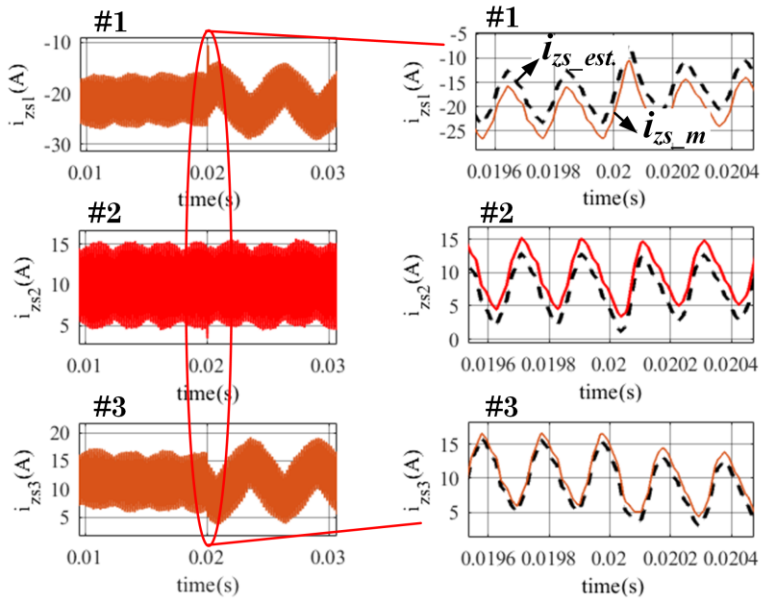


Fig. 3.4. Validation of the generalized ZSCC model in three paralleled 2L-VSIs: measured ZSCC from three inverter modules i_{zs_m} (plotted with red/orange solid lines) vs. estimated ZSCC using the proposed ZSCC model $i_{zs\_est.}$ (plotted with black dashed lines). The plot is zoomed at t=0.02s when inverter #1 is shutdown.

According to above analysis, the generalized ZSCC derived in this section is validated under different operation conditions and with different module numbers. This mathematical model can be applied to design of the model-based LF-ZSCC controllers.

3.2. Interleaved CB-MPC for LF-ZSCC elimination

To achieve interleaving and CMV reduction in multiparallel VSI systems, this section proposed a novel centralized control scheme which can suppress LF-ZSCC at any operating conditions. Named as carrier-based model predictive control (CB-MPC), carriers and module predictive controller are employed in the proposed method. Benefits of MPC (e.g. multi-objective control and fast dynamic response) and interleaving (e.g. filter size reduction and possible resonant-free design) can be combined to yield further performance improvements. Leveraged with the generalized ZSCC model derived in Section 3.12, proposed method can be applied to multiparalleled inverter systems with any number of inverter module.

Details of the proposed control scheme can be found in Fig. 3.5. In CB-MPC, there are two control layers. The outer layer is a centralized model predictive controller, which takes all the current/voltage measurements and generates the optimal modulation signals $m_{abc,j}$ for each module. Fast dynamic response can be achieved with modulated MPC [76]. Detailed design steps include current prediction, cost function establish, and cost function optimization, which will be presented in this section. The inner layer features the localized carrier-based PWM (CB-PWM) for gating control. Desired interleaving angle of $(j\text{-}1)/N*360^{o}$ can be realized in the same way as in synchronizing, where phase-shift is set for each carrier through either DPS or FPGA. With such design, the devices switching frequencies can be fixed at carrier frequency, while higher sampling frequency can be selected for better control performance [77].

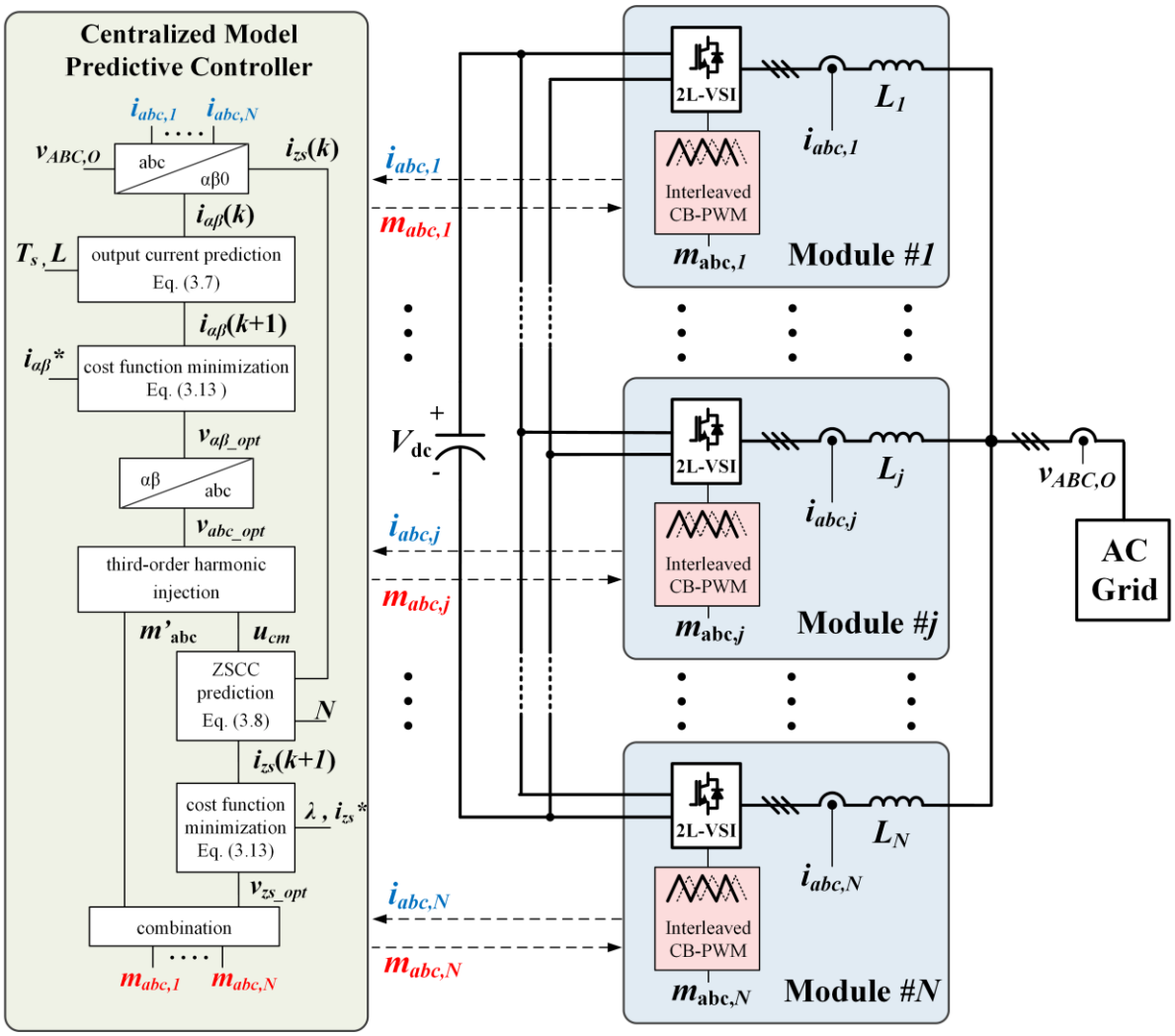


Fig. 3.5. Control scheme of the proposed centralized CB-MPC implemented in the centralized control architecture.

3.2.1. Current modeling & prediction

The first step of designing a centralized CB-MPC controller is to predict the output currents and ZSCC for each inverter module. From the Euler's Forward Approximation theorem, inverter current at the next sampling instant $i_j(k+1)$ can be predicted from the current measurements $i_j(k)$, assuming the sampling period T_s is sufficiently small. In this design, one-step prediction is

implemented to compensate the sampling delay. DM output current can be predicted with the average output current model derived from the last section.

$$\frac{di_j}{dt} = \frac{i_j(k+1)-i_j(k)}{T_s} \tag{3.6}$$

Based on Euler's forward approximation and the average output current model derived in (3.2), one-step prediction of the inverter output current of the j^{th} module can be obtained in (3.7).

$$\begin{bmatrix} i_{\alpha j}(k+1) \\ i_{\beta j}(k+1) \end{bmatrix} = \frac{T_s}{L_j}\begin{bmatrix} v_{\alpha j}(k)-v_{\alpha O}(k) \\ v_{\beta j}(k)-v_{\beta O}(k) \end{bmatrix} + \begin{bmatrix} i_{\alpha j}(k) \\ i_{\beta j}(k) \end{bmatrix} \tag{3.7}$$

Based on Euler's forward approximation and the generalized ZSCC model derived in (3.5), one-step prediction of ZSCC for the j^{th} module can be obtained in (3.8).

$$i_{zsj}(k+1) = \frac{T_s}{L_t}\frac{N}{N-1}(v_{zsj} + u_{cmj}) - \frac{T_s}{L_t}\sum_{x=1}^{N}\frac{v_{zsx}+u_{cmx}}{N-1} + i_{zsj}(k) \tag{3.8}$$

3.2.2. Cost function design

The second step is to establish a cost function that representing all the control objectives. For the centralized CB-MPC, there are two major control objectives: 1) current reference tracking, 2) LF-ZSCC elimination. The output current/power should be individually controlled for each module, which can be achieved by evaluating the performance of all possible switching states and selecting the optimal one to minimize the cost function. On the other hand, global optimization is required to eliminate LF-ZSCC caused by hardware parameters mismatch and/or different module power outputs. Since the fundamental output tracking is not affected by ZS components, two control objectives can be achieved simultaneously under the synchronous stationary coordinate. Cost function for the j^{th} inverter module $g_j(v_{\alpha j}, v_{\beta j}, v_{zs1}...v_{zsN})$ is established in (3.9), where the first two terms evaluate the performance of fundamental output states on tracking the current/power reference. The third term represents the impact of ZS voltage on LF-

ZSCC control. i_j^*(k+1) denotes output current reference for the j^{th} inverter under αβ-frame, where i_k^*(k+1) ≈ i_k^*(k) for a short sampling period; i_{zs}^*(k+1) denotes ZSCC reference for all modules which is designed to be zero; λ denotes the weighting factor of ZSCC control, which is selected as one for optimal LF-ZSCC control performance.

$$g_j(v_{\alpha j}, v_{\beta j}, v_{zs1} \cdots v_{zsN}) = \left|i_{\alpha j}(k+1) - i_{\alpha j}^*(k+1)\right|^2 + \left|i_{\beta j}(k+1) - i_{\beta j}^*(k+1)\right|^2 + \lambda \sum_{x=1}^{N} |i_{zsx}(k+1) - i_{zsx}^*(k+1)|^2 \tag{3.9}$$

3.2.3. Cost function optimization

The last step is to select the optimal switching states which can achieve the best overall control performance. CB-MPC adopts the same idea of cost function minimization as in conventional MPC algorithms but requires fewer steps of online computation. In conventional MPCs, the impact of all eight possible switching states [000], [001], [010], [011], [100], [101], [110], [111] needs to be evaluated one by one in each sampling period, which leads to high amount of computation steps. The computation burden will be significant for system with more than two modules. Inspired by [76], this optimization procedure in MPC can be simplified by avoiding the time-consuming iteration steps. To minimize cost function g_j, the optimal solutions must satisfy the minimum value conditions defined in (3.10). The optimal output states can be obtained by solving (3.10) so that the time-consuming iteration steps can be avoided.

$$\begin{cases} \frac{dg_j(v_{\alpha j}, v_{\beta j}, v_{zs1} \cdots v_{zsN})}{dv_{\alpha j}} = 0 \\ \frac{dg_j(v_{\alpha j}, v_{\beta j}, v_{zs1} \cdots v_{zsN})}{dv_{\beta j}} = 0 \\ \frac{dg_j(v_{\alpha j}, v_{\beta j}, v_{zs1} \cdots v_{zsN})}{dv_{zsj}} = 0 \end{cases} \tag{3.10}$$

The optimal fundamental output of the j^{th} module $v_{\alpha j\_opt}$ and $v_{\beta j\_opt}$ is derived in (3.13). Since the fundamental output of one module is independent from all other N-1 modules, the optimal solution for each module can be obtained by solving the first two equations of (3.10). ZSCC, on

the other hand, depends on the ZS output of all modules $v_{zs1}...v_{zsN}$. Global optimization is required in order to obtain the optimal ZS outputs for all N modules. To solve the third equation of (3.10) for N modules all at once, a multi-input-multi-output (MIMO) system can be established as

$$\begin{cases} \frac{dg_1(v_{zs1}\cdots v_{zsN})}{dv_{zs1}} = \frac{d}{dv_{zs1}}\lambda \sum_{x=1}^{N}|i_{zsx}(k+1) - i_{zsx}^*(k+1)|^2 = 0 \\ \vdots \\ \frac{dg_j(v_{zs1}\cdots v_{zsN})}{dv_{zsj}} = \frac{d}{dv_{zsj}}\lambda \sum_{x=1}^{N}|i_{zsx}(k+1) - i_{zsx}^*(k+1)|^2 = 0 \\ \vdots \\ \frac{dg_N(v_{zs1}\cdots v_{zsN})}{dv_{zsN}} = \frac{d}{dv_{zsN}}\lambda \sum_{x=1}^{N}|i_{zsx}(k+1) - i_{zsx}^*(k+1)|^2 = 0 \end{cases} \tag{3.11}$$

By substituting the predicted ZSCC (3.8) into (3.11), the optimal solution of ZS output v_{zsj_opt} for all N modules can be obtained in (3.12). The i^{th} model is defined as the ZS reference for the rest N-1 modules, where i can be any number between 1 to N. LF-ZSCC of the i^{th} module can always be eliminated by controlling ZS outputs of the rest N-1 modules.

$$\begin{cases} v_{zs1\_opt} = \frac{N}{2N-3}[i_{zsi}(k) - i_{zs1}(k)]\frac{L}{3T_s} + (u_{cmi} - u_{cm1}) \\ \vdots \\ v_{zsj\_opt} = \frac{N}{2N-3}[i_{zsi}(k) - i_{zsj}(k)]\frac{L}{3T_s} + (u_{cmi} - u_{cmj}) \\ \vdots \\ v_{zsN\_opt} = \frac{N}{2N-3}[i_{zsi}(k) - i_{zsN}(k)]\frac{L}{3T_s} + (u_{cmi} - u_{cmN}) \end{cases} \tag{3.12}$$

From above steps, the optimal output states of the j^{th} module [$v_{\alpha j\_opt}$, $v_{\beta j\_op}$, v_{zsj_opt}] can be easily obtained through one-step computation of (3.13), instead of going through those time-consuming iteration steps. In this design, the N^{th} module is selected as the ZS reference. Filter inductances L are assumed to be identical where line resistances are ignored.

$$\begin{cases} v_{\alpha j\_opt} = -\frac{L}{T_s}i_{\alpha j}(k) + v_{\alpha O}(k) + \frac{L}{T_s}i_{\alpha j}^*(k) \\ v_{\beta j\_opt} = -\frac{L}{T_s}i_{\beta j}(k) + v_{\beta O}(k) + \frac{L}{T_s}i_{\beta j}^*(k) \\ v_{zsj\_opt} = \frac{N}{2N-3}[i_{zsN}(k) - i_{zsj}(k)]\frac{L}{3T_s} + (u_{cmN} - u_{cmj}) \end{cases} \tag{3.13}$$

With the proposed centralized CB-MPC, two control objectives, i.e., current/power reference tracking and LF-ZSCC elimination, can be achieved simultaneously for N paralleled inverters. Most importantly, interleaved PWM can be achieved with CB-MPC, which can reduce the CMV effects and improve system output quality. Implementation of the proposed method will be detailed in the following subsection.

3.2.4. Implementation of CB-MPC

The communication-based LF-ZSCC control can be implemented in two types of the control architectures i.e. master-slave or centralized design. Different number of the communication channels will be required, which lead to different cost for implementation. The system complexity and reliability will also be different for the two designs.

The conventional design is known as the master-slave control structure which can be found in Figure 3.6 (a). Master controller is capable to communicate with all other slave controllers located in each inverter modules. Typically, LF-ZSCC control will be implemented in a master controller powered by the master inverter. The master inverter cannot be shut down in order to maintain system operation. However, in practical applications, any inverter module should be allowed to shut down because unit shading is usually required to improve light-load efficiency and to extend module lifetime. To ensure constant operation and suppression of LF-ZSCC, every inverter module should be able to operate as the master inverter. Therefore, each inverter module needs to communicate with the rest of the system, which can result in high amount of the communication channels. Although it is a highly reliable design where every single distributed controller can serve as the master controller when required, implementation can be extremely challenging especially for systems with a large number of modules.

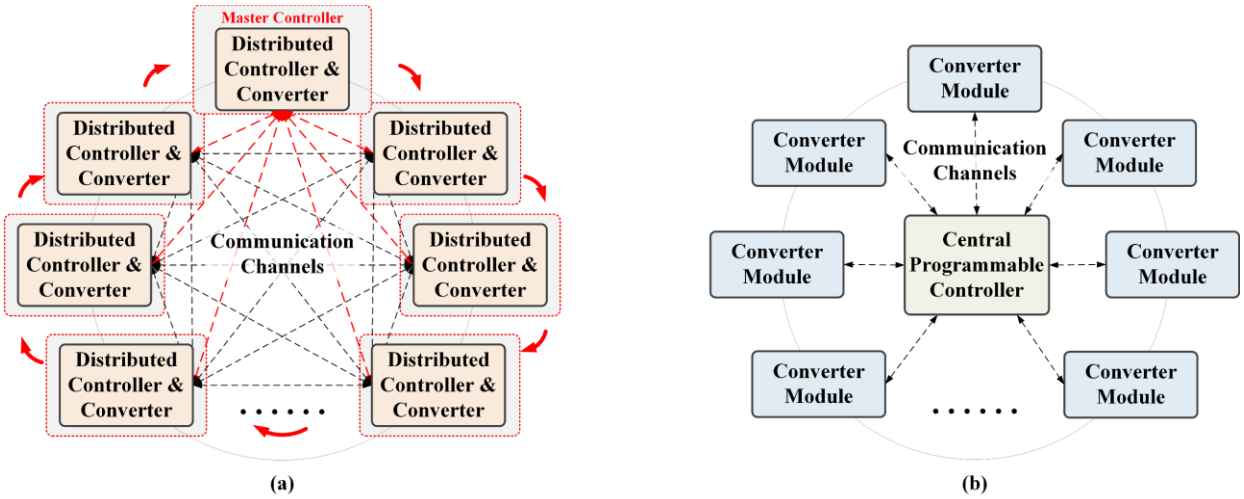


Fig. 3.6. (a) conventional master-slave control architecture (b) centralized control architecture for modular parallel inverters.

Alternatively, centralized control architecture can be adopted if the LF-ZSCC control is designed in a centralized manner. As shown in Figure 3.6 (b), a standalone central controller is employed to exchanged control information with the whole system. Communication lines can be saved since the inverters only need to exchange information with the central controller. Compared to the master-slave design, less communication cables are required which can reduce the system cost and system complexity. As shown in Figure 3.7, number of the required communication channels N_{cc} is lower in the centralized design, when the module number N is greater than three. Moreover, employing a central controller will not harm the system's modularity and reliability. In practical applications, central controllers are commonly found in multiparallel converter systems to synchronize the PWM carriers and/or to regulate the module power sharing [78-80]. Reliability of those commercial off-the-shelf programmable central controllers have been proven in diverse industrial applications, which makes it an alternative solution to implement LF-ZSCC control in modular parallel VSI systems.

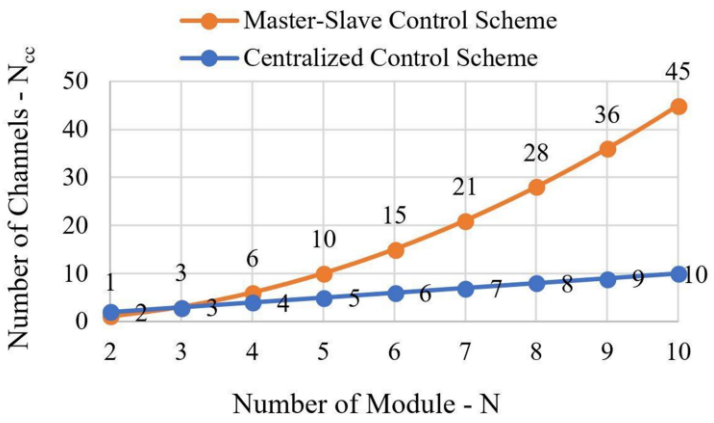


Fig. 3.7. Number of the modules N vs. Number of communication channels N_{cc} required in master-slave control scheme (orange) and centralized control architecture (blue).

Different from the existing LF-ZSCC control methods [52-56] that used to be implemented in a master-slave manner, the proposed centralized CB-MPC can be implemented in either control architectures. Depending on the applications, the proposed ZS control scheme is highly flexible, which can be implemented either in a dedicate central controller or in master converter's controllers. In the studied utility-scale PV inverter systems, large amount of the 2L-VSI modules may exist in a multi-megawatts central PV inverter, which can result in high amount of the communication channels in the master-slave design. In addition, considering the processor's limit, controllers in each module may not be powerful enough to work as a master controller. Therefore, centralized control scheme become a preferable solution for such application. Demonstration of the proposed method implemented in the centralized control architecture can be found in Fig. 3.5. Performance of the proposed method has been evaluated in both simulations and experiments, which will be detailed in the following sections.

3.3. Simulation verification

To evaluate the performance of the proposed control scheme, simulations are conducted on the grid-connected PV inverter system shown in Fig. 1.6. A scenario with six modular paralleled 2L-VSIs (*N*=6) has been simulated in MATLAB Simulink. System parameters are defined in Table 3.1. In normal operation, active output power of 120kW is transferred from DC link to AC grid through six paralleled inverter modules. Unit shading strategy is implemented because individual inverter module will be shut down during low-power conditions. The proposed CB-MPC has been implemented in a central controller, which can communicate with all six inverter modules for output power regulation and LF-ZSCC elimination.

Table 3.1. Electrical Specifications of Grid-Connected PV System with Six Modular Paralleled 2L-VSI Modules

Electrical Parameter	Design Values	Electrical Parameters	Design Values
Nominal AC grid voltage	600 V_{rms}	Number of modules	6
Nominal DC-link voltage	1000 V	Rated power / module	20 kW
Grid fundamental frequency	60 Hz	Rated current / module	19 A_{rms}
Carrier frequency	5 kHz	Rated filter inductance	1 mH
Sampling frequency	10 kHz	Ground capacitance	18 μF

Output characteristics have been evaluated first. Waveforms of module individual output currents and total output current can be found in Fig. 3.8. All six modules are operating at rated conditions with CB-MPC applied. One can see the total output quality has been significantly improved as the THD reduced from an average of 21.0% down to 1.7% after interleaving. Frequency domain analysis indicates low-order DM harmonics induced at each module are canceled out, while the dominant sidebands shift from switching frequency (h =83) to six times of it (h = 500). Interleaved AC output voltage can be found in Fig. 3.9. For six paralleled 2L-

VSIs, seven voltage levels are observed which verifies the effectiveness of interleaving. System CMV is measured and provided in Fig. 3.9. FFT analysis indicates the dominant sidebands of CMV have also been pushed from the switching frequency to six times of it with interleaved CB-MPC applied. CMV effects are reduced in a significant way. Less leakage current is induced thus requires a smaller CM filter to fulfill the grid code requirements. In practical applications, the system's overall power density can also be improved with CB-MPC.

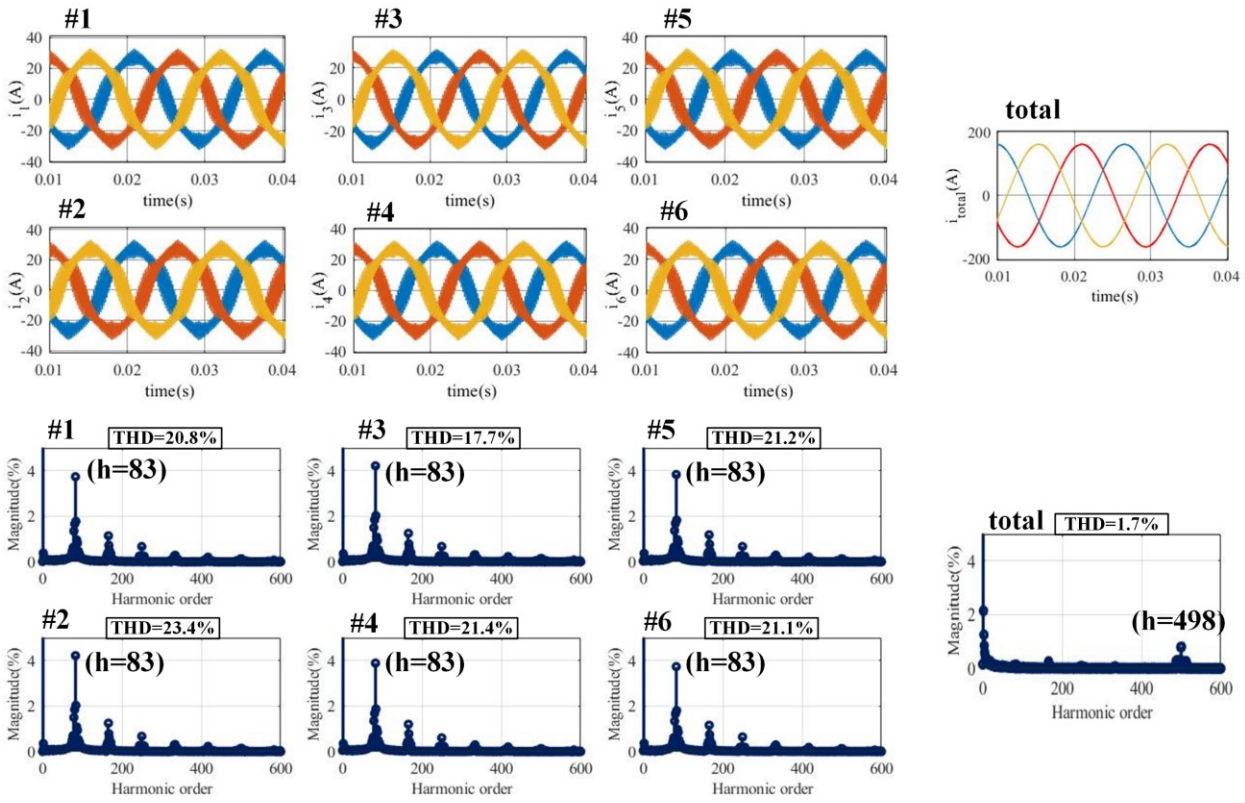


Fig. 3.8. Simulation result of six paralleled 2L-VSIs with CB-MPC: inverter individual output currents i_1 to i_6 (left); total interleaved output current i_{total} (right); and corresponding frequency domain FFT analysis.

Dynamic performance of the proposed method is evaluated on the same system. All six modules are operating at full load producing 20 kW/ 0 var, when step change is applied to inverter #1 for reducing the power reference to zero at t=0.15s. Current waveforms of each inverter module can be found in Fig. 3.10. The output power for inverter #1 is reduced from 20

kW to 0 kW, while the whole system's total output power reduces from 120kW to 100kW after at t=0.15s. One can see output currents precisely follow the reference signals before and after the step-change is applied. Zoomed Fig. 3.10 indicates module output current coverages to their αβ references with a minor transient time period since t_{trans} is less than 1ms. Both steady-state and transient-state results show that module output current/powers can be individually controlled with the proposed CB-MPC. Benefits of MPC and interleaving are combined in CB-MPC, which results in superior overall performance for grid-tied solar PV inverters with modular parallel VSIs.

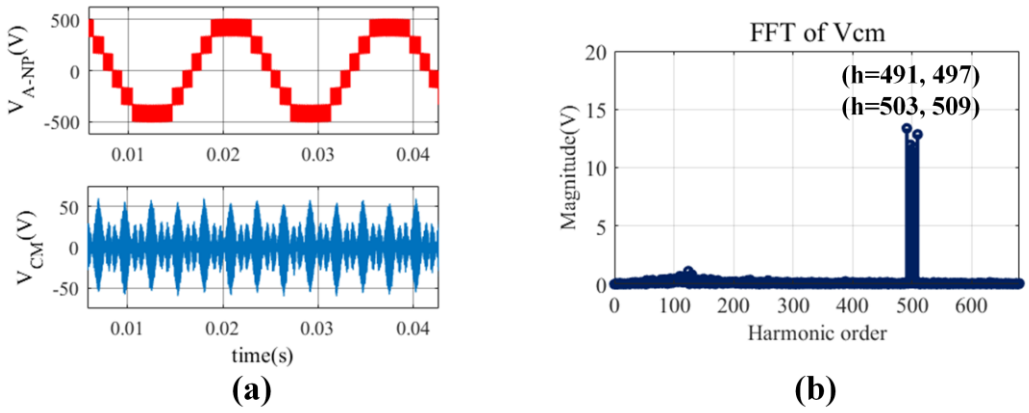


Fig. 3.9. Simulation result of six paralleled 2L-VSIs with CB-MPC: measured total phase-to-neutral output voltage v_{A-NP}(V); measured CM voltage v_{CM}; and frequency domain FFT analysis.

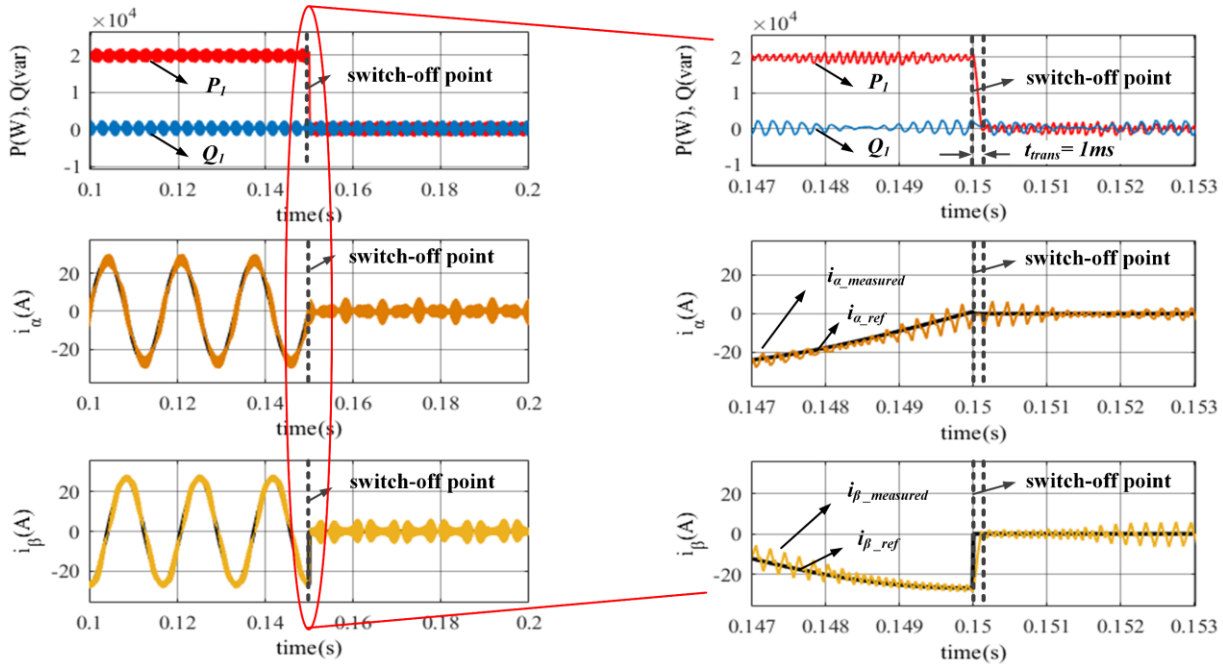


Fig. 3.10. Dynamic performance of the CB-MPC when inverter #1 shutdown at t=0.15s: variation of output power P_1(W) and Q_1(var); output current reference i_{α_ref}, i_{β_ref} (shown in dark); and measured output current i_{α}, i_{β} (shown in color). The figure is zoomed at t=0.15s when inverter #1 is shutdown.

To verify the effectiveness of the proposed centralized CB-MPC on eliminating LF-ZSCC while realizing interleaved PWM, two operating conditions are simulated including both filter parameters mismatch and module output mismatch cases. The first scenario is when the inverter modules share the same load but with unequal filter inductances. LF-ZSCC can be produced due to the filter parameter mismatch. The second scenario is when one of the inverters is shutdown while the others are still operating at full-load. In that case, significant LF-ZSCC will be produced due to imbalanced module outputs and filter parameter mismatch. Effectiveness of the proposed CB-MPC on eliminating LF-ZSCC will be evaluated under above operating conditions.

Simulation results of above two scenarios can be found in Fig. 3.11 to Fig. 3.13. The first 0.05s (t=0.10s-0.15s) represents the first scenario with equal module output powers. As shown in Fig. 3.11, total output power of 120 kW is evenly distributed among six 2L-VSI modules. Filter inductance for inverter module #2 is 10% less than the rated value. Filter inductance for module

#3 is 20% larger. LF-ZSCC can be observed in Fig. 3.12. Frequency domain analysis indicates majority of the LF-ZSCC appears at inverter #2 and inverter #3. The dominant sidebands of HF-ZSCC appear at the switching frequency of 5kHz or h=83, which can be eliminated with CM chokes. The second 0.05s (t=0.15s-0.20s) represents the scenario when the inverter modules have different output powers. Inverter #1 is shutdown at t=0.15s causing 100% power mismatch. Filter parameters remain unchanged leading to more serious LF-ZSCC. As shown in Fig. 3.11, total output power reduces from 120 kW to 100kW after inverter #1 switched off. Significant LF-ZSCC has been observed due to power mismatch. Magnitude of the HF-ZSCC also increases due to the incomplete harmonic cancellation during the interleaving. As shown in Fig. 3.13, majority of the LF-ZSCC appears at inverter #1 with order of h = 3, 9, 15. The dominant LF-ZSCC sideband have the magnitude of 32A, which is significantly larger than the first case. Without proper LF-ZSCC control in place, interleaved PWM cannot be implemented for CMV reduction. Furthermore, CM chokes' magnetic core will be saturated, which could lead to serious power quality issues and safety concerns.

Simulation results of the proposed centralized CB-MPC can be found in Fig. 3.14. LF-ZSCC components are regulated to zero in either scenarios, when the inverter modules have different output powers and unequal filter inductances. From above analysis, effectiveness of the proposed centralized CB-MPC on eliminating LF-ZSCC, realizing interleaved PWM, and regulating module output powers are verified. In summary, the proposed CB-MPC features several advantages over the existing MPC methods, which makes it a practical solution for central/multistring solar PV inverters with modular paralleled 2L-VSIs adopted. Efficient DC to AC power conversion can be achieved with less CMV or leakage current produced, which can improve the system efficiency, power density, and reliability.

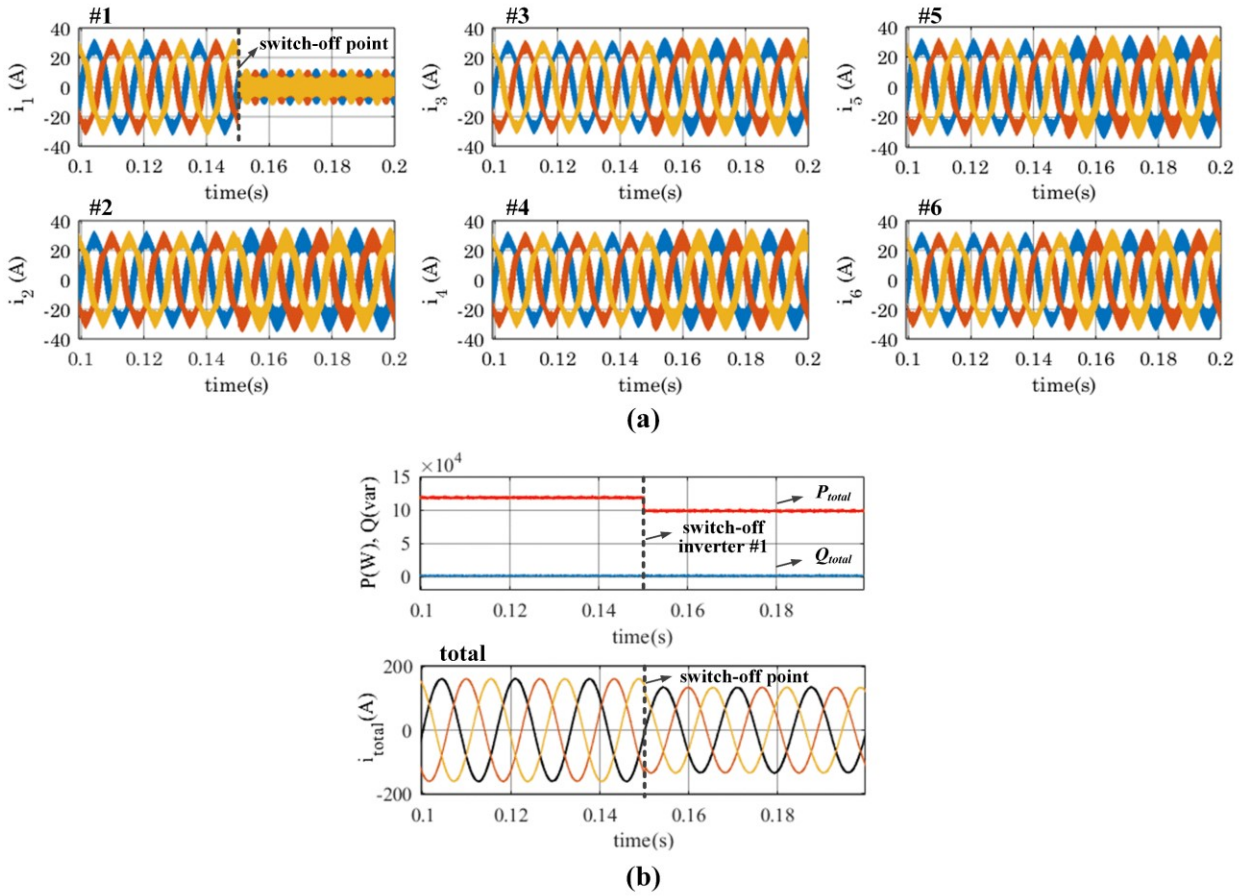


Fig. 3.11. Simulation results the proposed CB-MPC on six paralleled 2L-VSIs, when inverter #1 shutdown at t=0.15s: (a) module individual three-phase output currents i_1 (A) to i_6 (A); (b) total output power P_t (W) & Q_t (var), and total output current i_{total} (A).

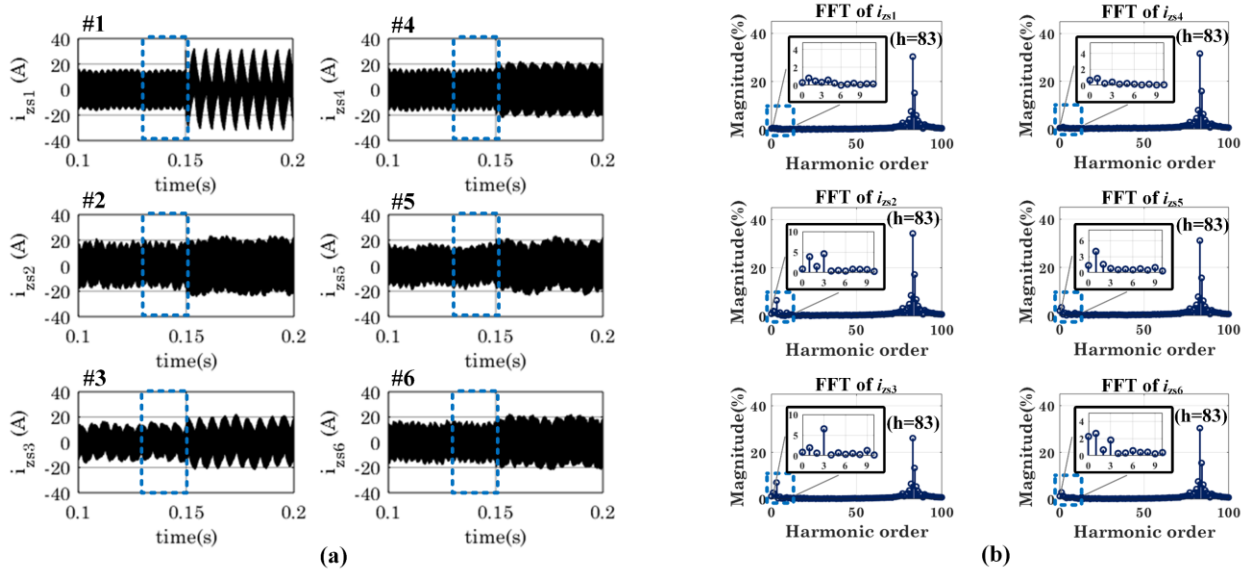


Fig. 3.12. LF-ZSCC caused by hardware parameter mismatch (L_2=90%, L_3=120%) in six paralleled 2L-VSIs: (a) waveforms of six inverter's individual ZSCCs i_{zs1}(A) to i_{zs6}(A); (b) frequency-domain FFT analysis of ZSCC at t=0.10s – 0.15s.

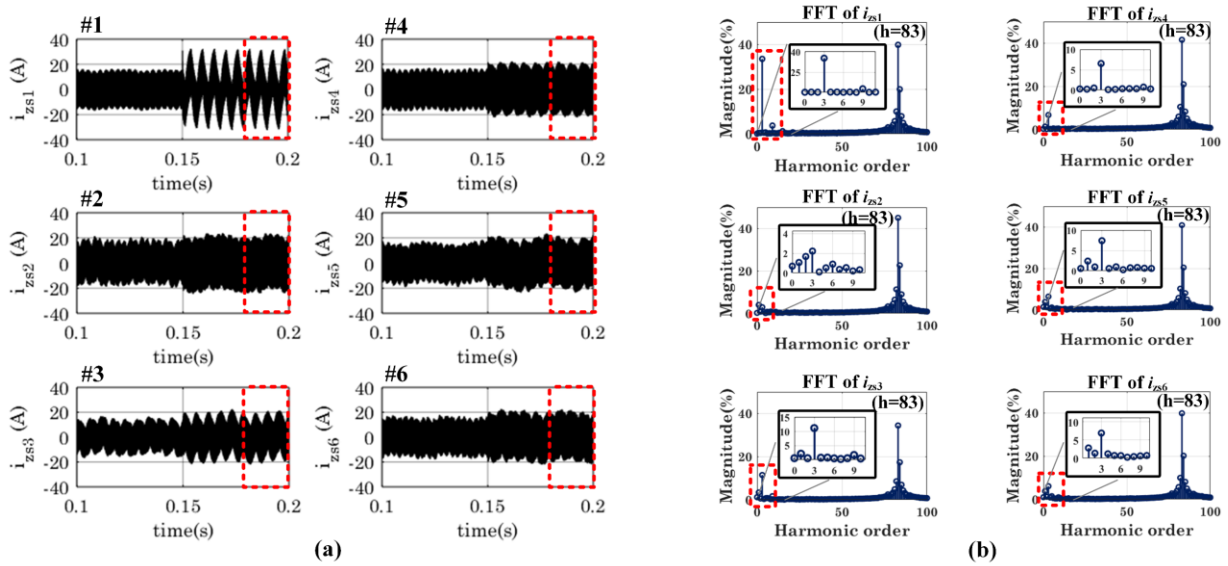


Fig. 3.13. LF-ZSCC caused by unequal output powers (P_1=0W, P_2 to P_6 = 20kW) & hardware parameter mismatch (L_2=90%, L_3=120%) in six paralleled 2L-VSIs: (a) waveforms of inverter's individual ZSCC i_{zs1} (A) to i_{zs6} (A); (b) frequency-domain FFT analysis of ZSCC at t=0.15s – 0.20s.

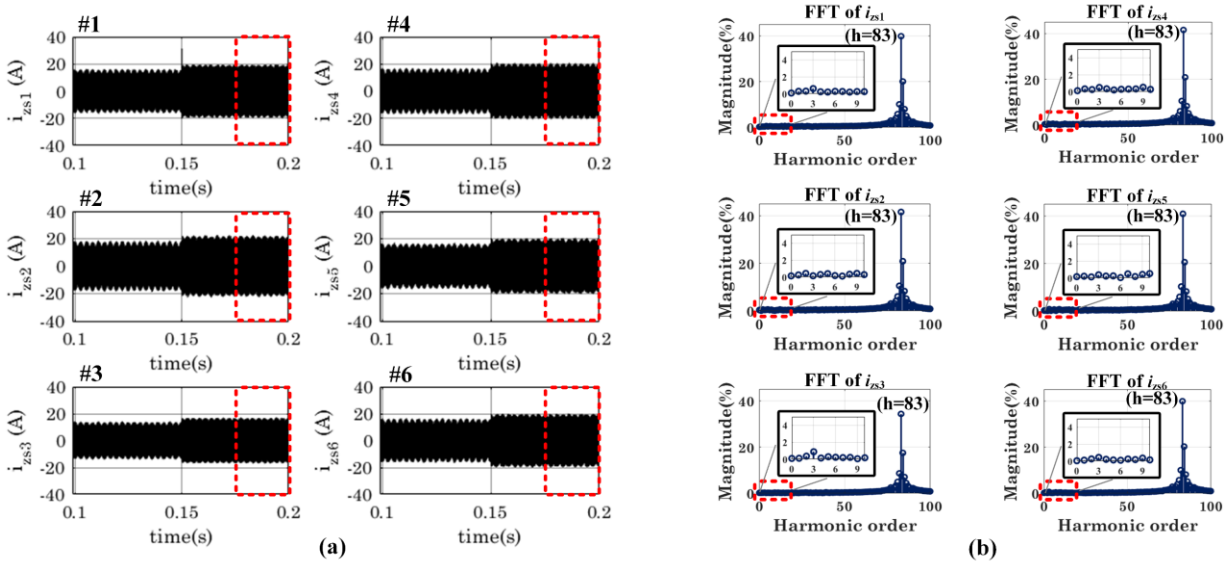


Fig. 3.14. Simulation results of the proposed CB-MPC with LF-ZSCC elimination in six paralleled 2L-VSIs: (a) waveforms of individual ZSCC i_{zs1} (A) to i_{zs6} (A) measured from six paralleled 2L-VSIs; (b) frequency-domain FFT analysis of ZSCC at t=0.15s – 0.20s.

3.4. Experimental validation

To evaluate the performance of the proposed centralized CB-MPC, a two-module 2L-VSI prototype has been established as shown in Fig. 3.15. Two isolated 2L-VSI modules are parallel-connected to a common DC-link. Voltage of the DC-link is maintained at 120V with a PV simulator and a DC source. The proposed control strategy is implemented in a centralized manner on the dSPACE DS1202 platform. Communication between VSI modules and the central controller are realized through fiber-optic cables. Both the sampling and switching frequency is set to be 5kHz. The system's AC output frequency is 60Hz.

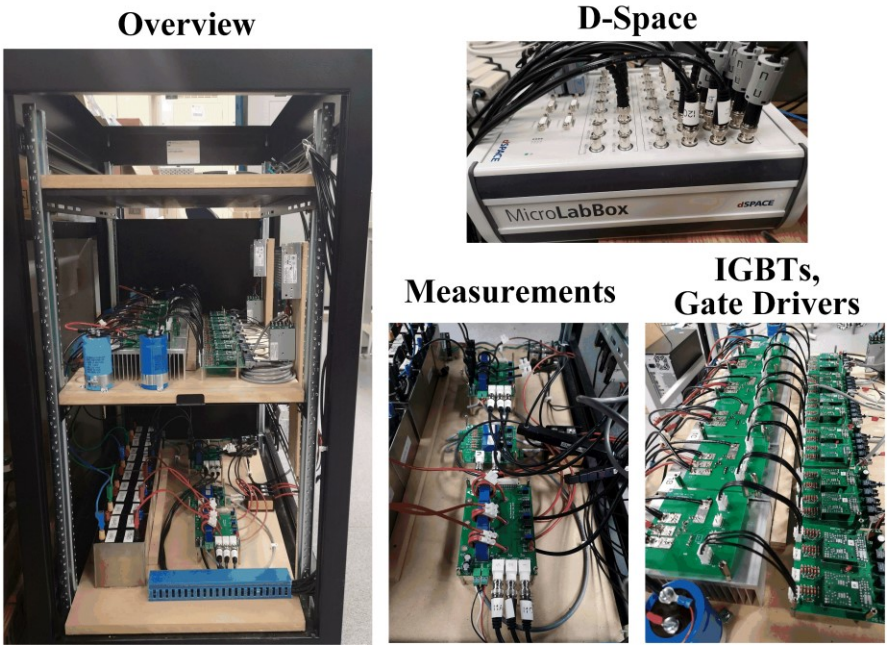


Fig. 3.15. Experimental prototype of two paralleled 2L-VSIs with dSPACE DS1202.

The circulating current among the two modules has been studied first. Both even and uneven power sharing conditions are considered. Over 10% filter parameter mismatch is implemented, namely, L_1 = 0.8 mH and L_2 = 0.9 mH. Experimental results of two modules sharing the same load can be found in Fig. 3.16. Relatively low LF-ZSCC is observed. The dominant HF-ZSCC

appears at switching frequency of 5 kHz or h = 83, which can be eliminated with CM filters. Experimental results of the two modules with unequal power output can be found in Fig. 3.17. As the worst case scenario, the second module is shut down causing 100% power mismatch. Significant amount of LF-ZSCC is observed with order h = 3, 9, 15, which will saturate the magnetic core of the CM filters and cause safety concerns. Even with all the IGBTs switched off on the second module, ZSCC can still circulate through the anti-parallel diodes to cause issues during the operation.

Experimental results of the proposed centralized CB-MPC are presented in Fig. 3.18 and Fig. 3.19. The steady-state performance is examined first. Taking the same filter inductances under 100% power mismatch, CB-MPC is applied to achieve interleaving and elimination of LF-ZSCC. According to the observation, output quality is significantly improved with the interleaved CB-MPC. The frequency domain analysis in Fig. 3.18 indicates dominant sidebands of each module appear at switching frequency of 5 kHz or h=83 for both i_1 and i_2. At the AC side, low-order DM harmonics are cancelled out while the dominant sideband of i_{total} is pushed to two times of the switching frequency with h=166. For individual modules, THD is 40% and 43% respectively for module #1 and module #2. THD of the interleaved output is reduced down to 13%. Effectiveness of the proposed method on realizing interleaving PWM has been verified. For circulating currents, LF-ZSCC is effectively reduced with CB-MPC. Magnitude of LF-ZSCC components are significantly lower than the uncontrolled case in Fig. 3.17. The remained LF-ZSCC components are minor and acceptable, which will not saturate the core of CM filters. Transient response of the proposed CB-MPC controller is provided in Fig. 3.19. One can see output currents can follow the reference signals precisely when step-change is applied. Frequency domain analysis also indicates low-frequency ZSCC components are eliminated

before and after inverter #1 switched off. The steady-state and transient-state performance of the proposed CB-MPC are verified. Two major control objectives are achieved, i.e. module output power control and LF-ZSCC regulation, which allows interleaved PWM to be implemented in grid-connected multiparallel VSI systems for CMV reduction.

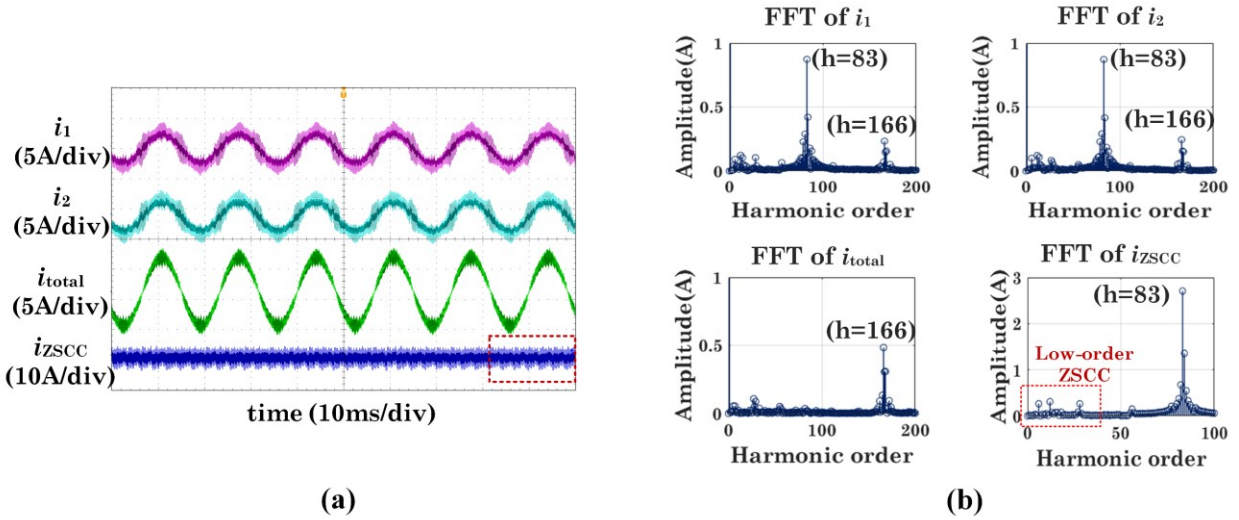


Fig. 3.16. Experimental results of two paralleled 2L-VSIs under equal power sharing condition: (a) phase A module individual output currents, total output currents, and measured ZSCC; (b) frequency domain FFT analysis of the last fundamental cycle.

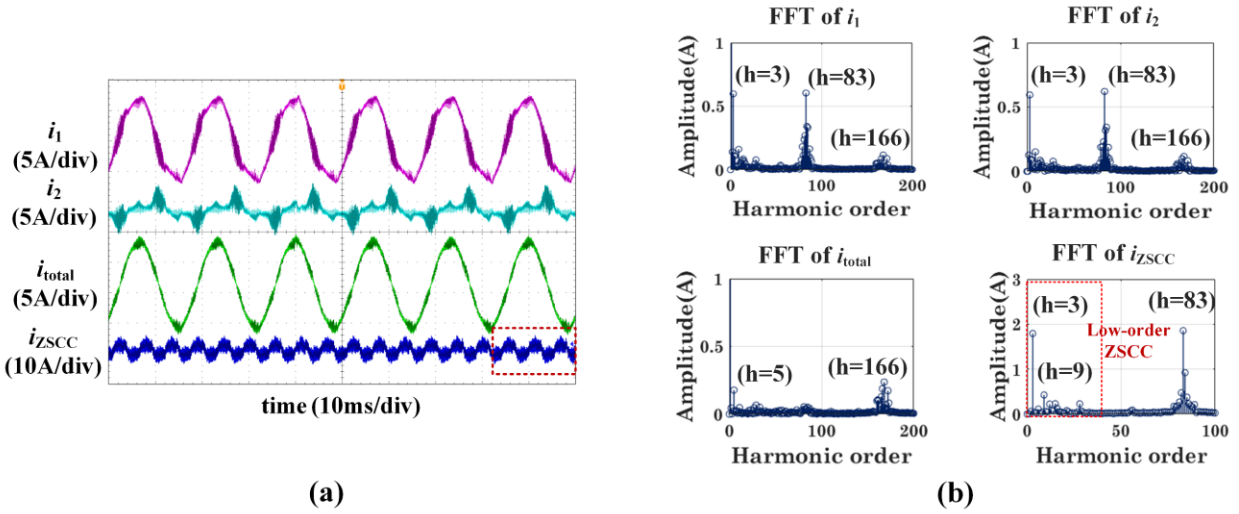


Fig. 3.17. Experimental results of two paralleled 2L-VSIs without LF-ZSCC control: (a) phase A module individual output currents, total output currents, and measured ZSCC; (b) frequency domain FFT analysis of the last fundamental cycle.

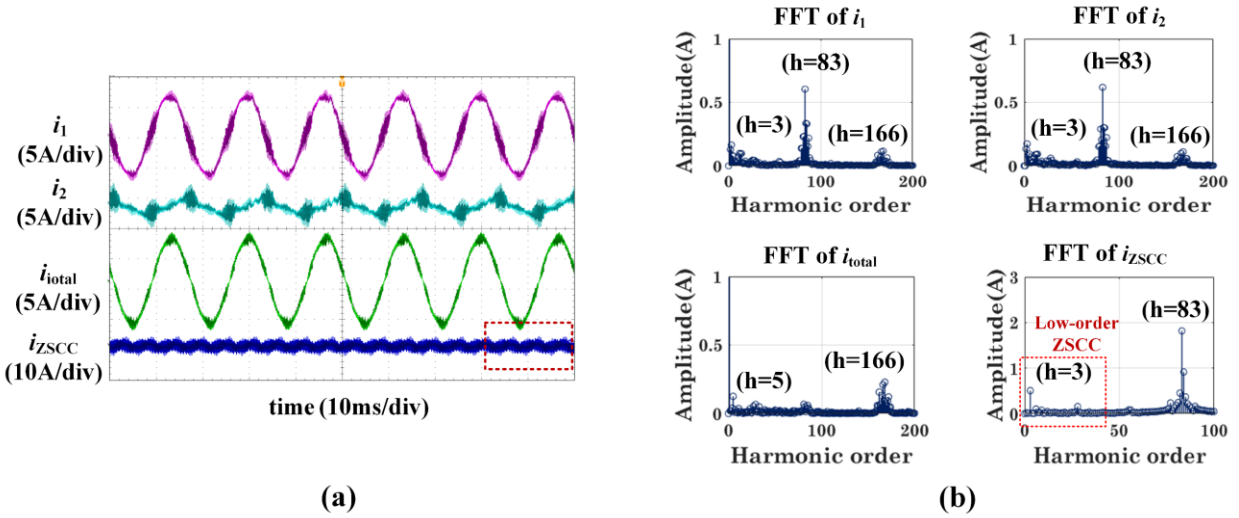


Fig. 3.18. Experimental results of the proposed centralized CB-MPC with LF-ZSCC elimination: (a) phase A module individual output currents, total output currents, and measured ZSCC; (b) frequency domain FFT analysis of the last fundamental cycle.

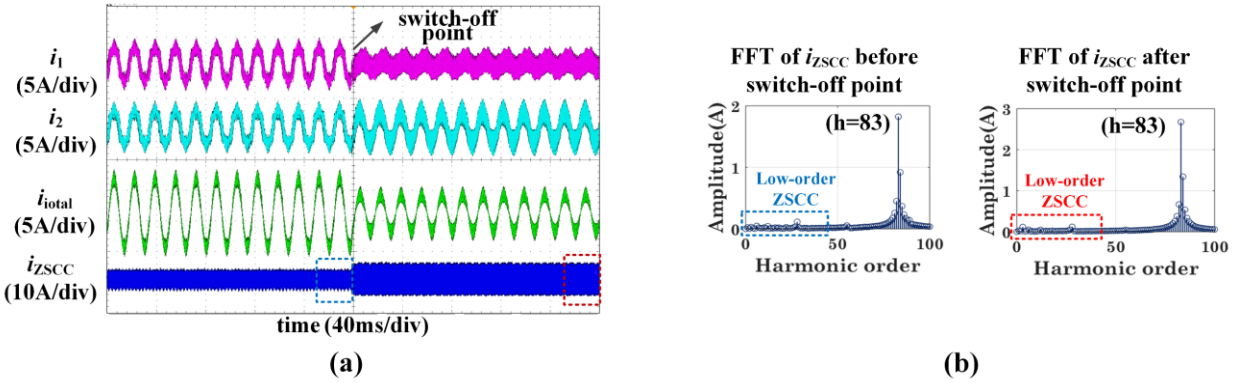


Fig. 3.19. Experimental results of the proposed centralized CB-MPC with LF-ZSCC elimination: (a) phase A module individual output currents, total output currents, and measured ZSCC; (b) frequency domain FFT analysis of ZSCC before (blue) & after (red) inverter #1 switched off.

3.5. Summary

It has been proved that interleaved PWM technique can be employed to reduce the CMV effects in multistring or central PV inverters with modular parallel 2L-VSIs adopted. However, LF-ZSCC needs to be addressed in the first place to prevent saturation of the CM filters and to

ensure safe operation. In this chapter, a centralized CB-MPC scheme has been proposed to achieve full elimination of LF-ZSCC in modular parallel VSIs. Carriers are adopted to realize interleaving. A generalized ZSCC model has been derived to leverage the employment of modulated MPC, which allows the proposed method to be applied to systems with N paralleled VSIs. Benefits of interleave and MPC are combined to yield further improvements in performance. This centralized CB-MPC control scheme can be implemented either in a dedicate central controller or in each converter's master controller. With the proposed method, power can be individually controlled for each inverter module. LF-ZSCC caused by inevitable hardware parameters mismatch and unequal power sharing are completely eliminated, which enables the interleaved PWM to be implemented in multistring or central PV inverters for CMV reduction.

Chapter 4 Conclusions & Future work

4.1. Thesis conclusions

This thesis focuses on addressing the key issues of employing ZCMV PWM and interleaved PWM to reduce CMV effects in different types of the grid-connected PV inverters. For transformerless sting or multistring PV inverters adopting multilevel VSIs, ZCMV PWM methods are explored first as a way to suppress CMV and leakage current without using large passive filtering elements. However, analysis indicates CMV cannot be completely eliminated with ZCMV PWMs because of the inevitable dead-time effect. To mitigate the dead-time effect, passive CM filters are still required which will increase the system size and cost. Upon thorough investigation of the dead-time effect in T-type 3L-NPC inverters, this thesis proposes an alternative dead-time mitigation strategy by using DC neutral-point connected LCL (NP-LCL) filter. Since there always exists a differential-mode (DM) LCL filter, the proposed method does not introduce any additional passive filtering elements into the system. Analysis in Chapter 2 indicates NP-LCL has better CM performance than the conventional LCL filter, which can be applied to mitigate the dead-time effect. Effectiveness of the proposed dead-time mitigation strategy has been verified in a lab-scale experimental platform of 3L-NPC inverter.

However, considering ZCMV will undermine the fundamental output quality which could result in larger DM filters, the actual impact of ZCMV on the total filter volume remains unknown. In Chapter 2, a comparative study is carried out to investigate the actual impact of ZCMV on total output filter volume. The following four designs are considered for comparison: 1) PD with LCL, 2) PD with NP-LCL, 3) ZCMV with LCL, and 4) ZCMV with NP-LCL. The

resultant filter volumes are fairly compared under the same filter parameter design framework. The study indicates the size of CM choke can be reduced with ZCMV but at the cost of a larger DM filter. Total filter volume of ZCMV is at least 1.5 times larger than the conventional PD PWM, because DM inductor dominates the overall filter volume. Considering the dead-time effect and larger DM filters, ZCMV PWM method becomes less applicable in T-type 3L-NPC PV inverters rated from 10kW to 100kW. On the other hand, conventional PD PWM is recommended since the total output filter volume can be minimized if combined with the NP-LCL. All the design, analysis, and conclusion have been verified in MATLAB simulation.

Beside the transformerless T-type 3L-NPC, research extends to central and multistring PV inverters adopting modular parallel VSIs, where the interleaved PWM can be employed to reduce the CMV effects. However, LF-ZSCC is identified as the major challenge which can be produced due to inevitable hardware parameters mismatch and module output power mismatch. In Chapter 3, a centralized carrier-based model predictive control scheme (CB-MPC) is proposed to achieve full elimination LF-ZSCC in module parallel VSIs. A novel generalized ZSCC model is derived, which allows the proposed method to be applied in N paralleled VSIs. Compared to the existing MPC-based ZS control schemes, CB-MPC is more applicable and more flexible, which can be implemented either in a dedicate central controller or in each converter's local controllers. Effectiveness of the proposed method has been verified by both simulation and experimental results. With full elimination of LF-ZSCC, the proposed method allows interleaved PWM to be implemented in multistring or central PV inverters for CMV reduction. Beside solar PV inverters, the proposed method can be beneficial to various other applications such as low-voltage motor drive or electrical power system for aircraft, where modular parallel VSIs are employed.

4.2. Future work

This work provides the foundation for future work in the following areas:

1. Experimental validation of the actual impact of ZCMV PWM on the total filter volume in a 10kW full-scale T-type 3L-NPC inverter platform. Comparative study proposed in Chapter 2 can be verified with customized DM and CM filters for each case.
2. Development of an effective active damping methods for transformerless T-type 3L-NPC PV inverter with NP-LCL filter in order to eliminate resonance in between the inverter midpoint and filter neutral point and to avoid using of passive damping elements.
3. Experimental validation of the proposed CB-MPC in solar PV inverters with more than two paralleled 2L-VSI modules or paralleled multilevel VSI modules, e.g., multi-paralleled 3L-VSIs.
4. Exploration of the proposed centralized CB-MPC control scheme in other applications with higher fundamental frequency such as the power system in aircraft, where both the interleaved PWM and centralized LF-ZSCC control are required to ensure sound and reliable operation.

References

[1] REN21 Secretariat, REN21. Renewables 2019 Global Status Report, Paris, France, 2019, ISBN 978-3-9818911-7-1. Available online: http://www.ren21.net/gsr-2019, Accessed 2019-11-23.

[2] Solar Power Europe, “Global Market Outlook for Solar Power / 2018 - 2022,” Available online: http://www.solarpowereurope.org/global-market-outlook-2018-2022, Accessed 2019-12-01.

[3] B. Azzopardi, J. Mutale and D. Kirschen, "Cost boundaries for future PV solar cell modules," 2008 IEEE International Conference on Sustainable Energy Technologies, Singapore, 2008, pp. 589-594.

[4] P. Mints and Z. J. Yu, "Photovoltaic Module Manufacturing Costs, Average Prices and Industry Balance 2006–2016," 2017 IEEE 44th Photovoltaic Specialist Conference (PVSC), Washington, DC, 2017, pp. 2039-204.

[5] S. B. Kjaer, J. K. Pedersen and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," in IEEE Transactions on Industry Applications, vol. 41, no. 5, pp. 1292-1306, Sept.-Oct. 2005.

[6] I. C. Rath and A. Shukla, "Review of Three Phase Transformer-less PV Converters," 2019 IEEE International Conference on Sustainable Energy Technologies and Systems (ICSETS), Bhubaneswar, India, 2019, pp. 063-068.

[7] R. Mechouma, B. Azoui and M. Chaabane, "Three-phase grid connected inverter for photovoltaic systems, a review," 2012 First International Conference on Renewable Energies and Vehicular Technology, Hammamet, 2012, pp. 37-42.

[8] W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," in IEEE Transactions on Industrial Electronics, vol. 62, no. 7, pp. 4537-4551, July 2015.

[9] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes and F. Blaabjerg, "Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 805-835, March 2020.

[10] D. Barater, E. Lorenzani, C. Concari, G. Franceschini and G. Buticchi, "Recent advances in single-phase transformerless photovoltaic inverters," in IET Renewable Power Generation, vol. 10, no. 2, pp. 260-273, 2 2016.

[11] D. Meneses, F. Blaabjerg, Ó. García and J. A. Cobos, "Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2649-2663, June 2013.

[12] P. Zhang, Y. Wang, W. Xiao and W. Li, "Reliability Evaluation of Grid-Connected Photovoltaic Power Systems," in IEEE Transactions on Sustainable Energy, vol. 3, no. 3, pp. 379-389, July 2012.

[13] J. Flicker and S. Gonzalez, "Performance and reliability of PV inverter component and systems due to advanced inverter functionality," 2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC), New Orleans, LA, 2015, pp. 1-5.

[14] Y. Xue, K. C. Divya, G. Griepentrog, M. Liviu, S. Suresh and M. Manjrekar, "Towards next generation photovoltaic inverters," 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, 2011, pp. 2467-2474.

[15] F. Bradaschia *et al.*, "Modulation for three-phase transformerless Z-source inverter to reduce leakage currents in photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5385–5395, Dec. 2011.

[16] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 435–443, Jan. 2012.

[17] M. C. Cavalcanti et al., "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 4, pp. 1360–1368, Apr. 2010.

[18] W. Kleinkauf, G. Cramer, and M. Ibrahim; "PV Systems Technology - State of the art developments and trends in remote electrification"; SMA Technologies AG, Dec. 01, 2005.

[19] M. Kazanbas, C. Nöding, H. Can, T. Kleeb and P. Zacharias, "A new single phase transformerless photovoltaic inverter topology with coupled inductor," 6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012), Bristol, 2012, pp. 1-6.

[20] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez and E. Aldabas, "A New High-Efficiency Single-Phase Transformerless PV Inverter Topology," in IEEE Transactions on Industrial Electronics, vol. 58, no. 1, pp. 184-191, Jan. 2011.

[21] B. Yang, W. Li, Y. Gu, W. Cui and X. He, "Improved Transformerless Inverter with Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 752-762, Feb. 2012.

[22] T. K. S. Freddy, N. A. Rahim, W. Hew and H. S. Che, "Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters," in IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5358-5369, Oct. 2014.

[23] L. Wang, Y. Shi, Y. Shi, R. Xie and H. Li, "Ground Leakage Current Analysis and Suppression in a 60-kW 5-Level T-Type Transformerless SiC PV Inverter," in IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 1271-1283, Feb. 2018.

[24] J. Lee and K. Lee, "New Modulation Techniques for a Leakage Current Reduction and a Neutral-Point Voltage Balance in Transformerless Photovoltaic Systems Using a Three-Level Inverter," in IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 1720-1732, April 2014.

[25] C. Hou, C. Shih, P. Cheng and A. M. Hava, "Common-Mode Voltage Reduction Pulse-width Modulation Techniques for Three-Phase Grid-Connected Converters," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1971-1979, April 2013.

[26] J. Rodriguez, J. Pontt, P. Correa, P. Cortes, and C. Silva, “A new modulation method to reduce common-mode voltages in multilevel inverters,” IEEE Trans. Ind. Electron., vol. 51, no. 4, pp. 834–839, Aug. 2004.

[27] X. Zhang, R. Burgos, D. Boroyevich, P. Mattavelli and F. Wang, "Improved Common-Mode Voltage Elimination Modulation with Dead-Time Compensation for Three-Level Neutral-Point-Clamped Three-Phase Inverters," Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, pp. 4240-4246, Denver, CO, 2013

[28] H. Zhang, A. V. Jouanne, S. Dai, A. K. Wallace and F., "Multilevel Inverter Modulation Schemes to Eliminate Common-Mode Voltages", IEEE Trans. Industry Applications, vol. 36, pp. 1645-1653, Nov/Dec. 2000.

[29] X. Guo; M. C. Cavalcanti, “Single-Carrier Modulation for Neutral-Point-Clamped Inverters in Three-Phase Transformerless Photovoltaic Systems,” IEEE Transactions on Power Electronics, 28(6), no.6, June 2013

[30] X. Guo, J. Zhou, R. He, X. Jia and C. A. Rojas, "Leakage Current Attenuation of a Three-Phase Cascaded Inverter for Transformerless Grid-Connected PV Systems," in IEEE Transactions on Industrial Electronics, vol. 65, no. 1, pp. 676-686, Jan. 2018.

[31] D. Zhang, F. Fred Wang, R. Burgos and D. Boroyevich, "Common-Mode Circulating Current Control of Paralleled Interleaved Three-Phase Two-Level Voltage-Source Converters with Discontinuous Space-Vector Modulation," in IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3925-3935, Dec. 2011.

[32] S. K. T. Miller, T. Beechner and J. Sun, "A Comprehensive Study of Harmonic Cancellation Effects in Interleaved Three-Phase VSCs," 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, 2007, pp. 29-35.

[33] Z. Quan and Y. W. Li, "Impact of PWM Schemes on the Common-Mode Voltage of Interleaved Three-Phase Two-Level Voltage Source Converters," in IEEE Transactions on Industrial Electronics, vol. 66, no. 2, pp. 852-864, Feb. 2019.

[34] J. M. Carrasco et al., "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," in IEEE Transactions on Industrial Electronics, vol. 53, no. 4, pp. 1002-1016, June 2006.

[35] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner and M. Sumner, "Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies," in IEEE Transactions on Power Electronics, vol. 24, no. 9, pp. 2202-2211, Sept. 2009.

[36] G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary and M. Vitelli, "Reliability Issues in Photovoltaic Power Processing Systems," in IEEE Transactions on Industrial Electronics, vol. 55, no. 7, pp. 2569-2580, July 2008.

[37] SMA PV central inverter datasheet, "SUNNY CENTRAL UP", Available online: https://files.sma.de/dl/32926/SC4xxxUP-DS-en-23.pdf, Accessed 2020-02-01.

[38] ABB central PV inverter datasheet, "PVS980-58 – 4348 to 5000 kVA", Available online: http://search.abb.com/library/Download.aspx?DocumentID=9AKK107492A3104&LanguageCode=en&DocumentPartId=&Action=Launch, Accessed 2020-02-01.

[39] Xiao Sun, Yim-Shu Lee and Dehong Xu, "Modeling, analysis, and implementation of parallel multi-inverter systems with instantaneous average-current-sharing scheme," in IEEE Transactions on Power Electronics, vol. 18, no. 3, pp. 844-856, May 2003.

[40] T. Chen, C. Lee and S. Y. R. Hui, "A General Design Procedure for Multi-Parallel Modular Grid-Tied Inverters System to Prevent Common and Interactive Instability," in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6025-6030, July 2019.

[41] SMA multistring PV inverter datasheet, "*Sunny Highpower PEAK1*", Available online: https://files.sma.de/dl/30188/SHP75-10-DEN1744-V23web.pdf, Accessed 2020-03-02.

[42] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014.

[43] E. Gurpinar, F. Iannuzzo, Y. Yang, A. Castellazzi and F. Blaabjerg, "Design of Low-Inductance Switching Power Cell for GaN HEMT Based Inverter," in IEEE Transactions on Industry Applications, vol. 54, no. 2, pp. 1592-1601, March-April 2018.

[44] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath and C. A. Teixeira, "The Benefits of SiC mosfets in a T-Type Inverter for Grid-Tie Applications," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2808-2821, April 2017.

[45] International Electrotechnical Commission (IEC), “IEC 62109-2 -Safety for power converters for use in photovoltaic power systems,”Part 2: Particular requirements for inverters, ed: IEC, 2011.

[46] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," in IEEE Transactions on Industry Applications, vol. IA-17, no. 5, pp. 518-523, Sept. 1981.

[47] Kerekes T, Teodorescu R, and Borup U, “Transformerless photovoltaic inverters connected to the grid,” IEEE Applied Power Electronics Conference., Anaheim, pp. 1733-1737, Feb. 2007.

[48] M. Schweizer, and J. W. Kolar, “Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications,” IEEE Transactions on Power Electronics, Vol. 28, No. 2, Feb. 2013

[49] J. L. Agorreta, M. Borrega, J. López and L. Marroyo, "Modeling and Control of N-Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants," in *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 770-785, March 2011.

[50] T. -. Chen, "Circulating zero-sequence current control of parallel three-phase inverters," in IEE Proceedings - Electric Power Applications, vol. 153, no. 2, pp. 282-288, 2 March 2006.

[51] Z. Ye, D. Boroyevich, J.-Y. Choi and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," in *IEEE Trans. on Power Electronics*, vol. 17, no. 5, pp. 609-615, Sept. 2002.

[52] K. Sun, X. Lin, Y. Li, Y. Gao and L. Zhang, "Improved Modulation Mechanism of Parallel-Operated T-Type Three-Level PWM Rectifiers for Neutral-Point Potential Balancing and Circulating Current Suppression," in *IEEE Trans. Power Electron*., vol. 33, no. 9, pp.7466-7479, Sept. 2018.

[53] Z. Xueguang, C. Jiaming, M. Yan, W. Yijie and X. Dianguo, "Bandwidth Expansion Method for Circulating Current Control in Parallel Three-phase PWM Converter Connection System," in *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6847-6856, Dec. 2014.

[54] X. Zhang, T. Wang, X. Wang, G. Wang, Z. Chen and D. Xu, "A Coordinate Control Strategy for Circulating Current Suppression in Multiparalleled Three-Phase Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 838-847, Jan. 2017.

[55] Z. Xueguang, Z. Wenjie, C. Jiaming and X. Dianguo, "Deadbeat Control Strategy of Circulating Currents in Parallel Connection System of Three-Phase PWM Converter," in *IEEE Transactions on Energy Conversion*, vol. 29, no. 2, pp. 406-417, June 2014.

[56] X. Xing, C. Zhang, A. Chen, H. Geng and C. Qin, "Deadbeat Control Strategy for Circulating Current Suppression in Multiparalleled Three-Level Inverters," in IEEE Transactions on Industrial Electronics, vol. 65, no. 8, pp. 6239-6249, Aug. 2018.

[57] X. Wang, J. Zou, Y. Peng, C. Xie, K. Li and J. M. Guerrero Zapata, "Elimination of zero sequence circulating currents in paralleled three-level T-type inverters with a model predictive control strategy," in *IET Power Electronics*, vol. 11, no. 15, pp. 2573-2581, Dec. 2018.

[58] X. Xing, C. Zhang, J. He, A. Chen and Z. Zhang, "Model predictive control for parallel three-level T-type grid-connected inverters in renewable power generations," in *IET Renewable Power Generation*, vol. 11, no. 11, pp. 1353-1363, Sep. 2017

[59] X. Wang *et al*., "A Novel Model Predictive Control Strategy to Eliminate Zero-Sequence Circulating Current in Paralleled Three-Level Inverters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 309-320, March 2019.

[60] F. Wang, Z. Li, X. Tong and L. Chen, "Modeling, Analysis and Evaluation of Modified Model Predictive Control Method for Parallel Three-Level Simplified Neutral Point Clamped Inverters," in *IEEE Access*, vol. 7, pp. 185349-185359, 2019.

[61] S. Bella *et al*., "FCS-MPC Current Control of Parallel Photovoltaic Grid Connected Inverter with Common AC and DC Buses," *2019 6th International Conference on Control, Decision and Information Technologies (CoDIT)*, Paris, France, 2019, pp. 1138-1143.

[62] Z. Zhang, A. Chen, X. Xing and C. Zhang, "A novel model predictive control algorithm to suppress the zero-sequence circulating currents for parallel three-phase voltage source inverters," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 3465-3470.

[63] L. Chen and F. Z. Peng, “Dead-Time Elimination for Voltage Source Inverters,” IEEE Transactions on Power Electronics, Vol. 23, No. 2, March 2008.

[64] Y. Lai and F. Shyu, “Optimal common-mode Voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development,” IEEE Trans. Ind. Appl., vol. 40, no. 6, pp. 1605–1612, Nov.–Dec. 2004.

[65] J. C. Giacomini, L. Michels, L. Schuch, H. Pinheiro, C. Rech, "Design of a LCL Filter for Leakage Current Reduction in Transformerless PV Grid-connected Three-Level Inverter", Proc. of APEC, pp. 239-245, 2015.

[66] M. Liserre, F. Blaabjerg, S. Hansen, “Design and Control of an LCL-Filter-Based Three-Phase Active Rectifier,” IEEE Transactions on Industry Applications, Vol. 41, No. 5, Sep/Oct 2005.

[67] C. Jiang, Z. Quan and Y. Li, "Passive Filter Design to Mitigate Dead-Time Effects in Three-Level T-Type NPC Transformerless PV Inverters Modulated with Zero CMV PWM," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 6275-6282.

[68] K.B Park, F. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, "Weight Minimization of LCL Filters for High-Power Converters: Impact of PWM Method on Power Loss and Power Density," IEEE Transactions on Industry Applications, Vol. 53, No. 3, May/June 2017

[69] Z. Cheng, M. Pande, Y. Xiao, and N. Zargari, "Power conversion system and method for active damping of common-mode resonance," U.S. Patent 7 990 097, Aug. 2, 2011

[70] A. A. Rockhill, M. Liserre, R. Teodorescu and P. Rodriguez, "Grid-Filter Design for a Multimegawatt Medium-Voltage Voltage-Source Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1205-1217, April 2011.

[71] J. He, Y. W. Li, F. Blaabjerg and X. Wang, "Active Harmonic Filtering Using Current-Controlled, Grid-Connected DG Units with Closed-Loop Power Control," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 642-653, Feb. 2014.

[72] Y. W. Li, "Control and Resonance Damping of Voltage Source and Current Source Converters with LC Filters," IEEE Transactions on Industrial Electronics, vol. 56, pp. 1511-1521, May 2009.

[73] W. T Mclyman, "Simplifier cut core inductor design," Jet Propulsion Lab. (NASA), California Inst. of Tech.; Pasadena, CA, United States, Tech. Rep. NASA-CR-149241, JPL-TM-33-697-REV-1, Nov. 1976.

[74] Hitachi Metals America Ltd., "Amorphous and Nanocrystalline Core Design and Selection Tool", [Online]. Available: https://www.hitachimetals.com/materials-products/amorphous-nanocrystalline/design-tools-core-selection.php

[75] Z. Quan, Y. W. Li and C. Jiang, "Design of Interleaved Converters with Minimum Filtering Requirement," *2019 IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Anaheim, CA, USA, 2019

[76] F. Sebaaly, H. Vahedi, H. Y. Kanaan and K. Al-Haddad, "Novel Current Controller Based on MPC with Fixed Switching Frequency Operation for a Grid-Tied Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6198-6205, Aug. 2018.

[77] P. Karamanakos and T. Geyer, "Guidelines for the Design of Finite Control Set Model Predictive Controllers," in IEEE Transactions on Power Electronics

[78] Rockwell Automation, "Programmable Controller Products," [online] Available: https://ab.rockwellautomation.com/programmable-controllers

[79] S. Brüske, S. Pugliese, S. Flacke and M. Liserre, "High-Frequency Grid Current Control of Parallel Inverters," *44th Annual Conference of the IEEE Industrial Electronics Society*, Washington, DC, 2018

[80] Huawei Technologies Co. Ltd, "Power Line Communicated Central Controller PLC CCO01A," Product User Manual," [online] Available: http://support.huawei.com/enterprise/en/doc/EDOC1-10003349210.