Design, Analysis and Implementation of New Durable Streetlighting LED Driver Topology

by

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Abstract

Light Emitting Diode (LED) fixtures are widely used in streetlighting owing to their durability, high luminous efficacy, and low power consumption. LED drivers which are ac/dc converters are required as an interface between the LEDs and the grid voltage. There are certain requirements mandated by standards for the safe operation and requirements relevant to the performance of streetlighting LED drivers. Most important ones include a Power Factor Correction (PFC) circuit that is essential for every high power streetlighting LED driver to achieve high Power Factor (PF), and low Total Harmonic Distortion (THD), and output light flickers of a streetlighting fixture that must be maintained under a certain limit to create a healthy lighting environment.

This thesis presents a high PF, flicker-free LED driver consisting of a novel buck-boost typed PFC circuit integrated with an asymmetric half-bridge LLC resonant converter. The proposed buck-boost PFC unit operates in Discontinuous Conduction Mode (DCM), and achieves almost unity PF and acceptable THD. The proposed topology limits the dc bus voltage to nearly the peak value of input sinusoidal voltage reducing the voltage stress of MOSFETs.

The control system of the LED driver is designed such that the output light flickers are mitigated without using any electrolytic capacitors in the circuit. Furthermore, the proposed LED driver achieves high efficiency throughout a wide operating range owing to the Zero Voltage Switching (ZVS) obtained in LLC switches, and optimal magnetic designs. Simulation and experimental results based on a 200 W laboratory prototype are presented to verify the effectiveness of the design and control systems. The laboratory prototype provides the maximum efficiency of 94.6%, power factor greater than 0.98 at full-load, and below 15% output current ripples.

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Abbreviations

ZVS	**Z**ero **V**oltage **S**witching
PFC	**P**ower **F**actor **C**orrection
PF	**P**ower **F**actor
THD	**T**otal **H**armonic **D**istortion
DCM	**D**iscontinuous **C**onduction **M**ode
SSL	**S**olid **S**tate **L**ighting
PV	**P**hoto **V**oltaic
HPS	**H**igh **P**ressure **S**odium
PC	**P**ower **C**onversion
LED	**L**ight **E**mitting **D**iode
CRI	**C**olor **R**endering **I**ndex
RCC	**R**ipple **C**ancellation **C**onverter
EMC	**E**lectro **M**agnetic **C**ompatibility
EMI	**E**lectro **M**agnetic **I**nterference
PFM	**P**ulse **F**requency **M**odulation
PWM	**P**ulse **W**idth **M**odulation
RMS	**R**oot **M**ean **S**quare
KCL	**K**irchoff's **C**urrent **L**aw
KVL	**K**irchoff's **V**oltage **L**aw

List of Symbols

α_i	copper loss allocation coefficient	[−]
ΔE_{C1}	energy change of C_1 during $\frac{T_l}{4}$	[J]
Δt_d	conduction time of D_a	[s]
ΔV_{bus}	double-frequency voltage ripple of C_1	[V]
Δv_{C2}	switching frequency voltage ripple of C_2	[V]
δ	skin depth	[m]
η	converter efficiency	[−]
$\hat{B}$	maximum flux density	[T]
$\hat{i}_S$	maximum current of S_{1-2} during T_{sw}	[A]
$\hat{i}_{C2}$	maximum of i_{C2} during T_{sw}	[A]
$\hat{i}_{in}$	maximum of i_{in} during T_{sw}	[A]
$\hat{p}_{in}$	maximum input power during T_{sw}	[W]
κ	inductor parameter	[−]
λ	ferrite core exponent	[−]
$\lvert v_g \rvert$	rectified input voltage	[V]
$\mathcal{P}$	number of strands of a Litz wire	[−]
$\mathcal{R}$	magnetic reluctance	[H^{-1}]
$\mathcal{V}_e$	magnetic volume	[m^3]
μ_0	air permeability	[$\mathrm{H\,m}^{-1}$]
ω_l	angular line frequency	[$\mathrm{rad\,s}^{-1}$]
ω_r	angular resonance frequency	[$\mathrm{rad\,s}^{-1}$]
ω_s	angular switching frequency	[$\mathrm{rad\,s}^{-1}$]
Φ	magnetic flux	[Wb]
Ψ	magnetic flux linkage	[Wb]
ρ	copper resistivity	[$\Omega\,\mathrm{m}$]
θ_s	voltage lag angle of LLC resonant tank	[rad]
A_e	magnetic area of middle leg	[m^2]
A_f	ferrite coefficient	[−]
a_{ch}	largest dimension of ferrite core	[m]

A_{eo}	magnetic area of outer legs	[m^2]
D	duty cycle	[−]
d	wire diameter	[m]
d_{wg}	winding distance from ferrite core	[m]
F	normalized switching frequency	[−]
f_{eq}	equivalent frequency of a winding	[Hz]
f_l	line frequency	[Hz]
f_p	pole frequency	[Hz]
f_{rp}	peak resonance frequency	[Hz]
f_r	resonance frequency	[Hz]
f_{sw}	switching frequency	[Hz]
g	airgap	[m]
$i_{C2,0}$	value of i_{C2} at turn-on of S_1	[A]
$i_{C2,1}$	value of i_{C2} at turn-on of S_2	[A]
$I_{C2,rms}$	rms of i_{C2}	[A]
i_{C2}	current of secondary winding of T_a	[A]
$I_{Da,max}$	maximum of i_{Da}	[A]
i_{Da}	current of D_a	[A]
$I_{Dr,max}$	maximum current of D_{1-2}	[A]
$I_{g,rms}$	rms of input current	[A]
i_g	input current	[A]
$i_{in,ave}$	average of i_{in} over T_{sw}	[A]
$I_{in,max}$	maximum of i_{in}	[A]
$I_{in,rms}$	rms of i_{in}	[A]
i_{in}	current of primary winding of T_a	[A]
$I_{La,max}$	maximum of i_{La}	[A]
$i_{La,pp}$	peak-to-peak current of L_a	[A]
$I_{La,rms}$	rms of i_{La}	[A]
i_{La}	current of L_a	[A]
$I_{Lr,max}$	maximum of i_{Lr}	[A]
i_{Lr}	resonant current	[A]
i_{nr2}	current of secondary winding of T_r	[A]
i_o	output current	[A]
I_{ref}	reference output current	[A]
$I_{rms,S1-2}$	rms current of S_{1-2}	[A]
$I_{S,max}$	maximum current of S_{1-2}	[A]
i_{S1-2}	current of S_{1-2}	[A]

J	current density	$[\mathrm{A\,m^{-2}}]$
k_e	core loss constant	$[-]$
K_{sy}	symmetry factor	$[-]$
k_{cp}	coupling factor	$[-]$
k_f	inductor factor	$[-]$
k_{tf}	transformer factor	$[-]$
l_e	magnetic length	[m]
l_T	mean-length-per-turn	[m]
L_{llc}	L_{mr} to L_r ratio	$[-]$
m	number of layers of a winding	$[-]$
M_g	voltage gain of LLC resonant tank	$[-]$
m_E	effective number of layers of a winding	$[-]$
$M_{g,DC}$	dc voltage gain of LLC resonant tank	$[-]$
N_i	number of turns of a winding	$[-]$
$n_{(r)}$	transformer turns ratio	$[-]$
P_h	heat dissipation capability of a core	[W]
P_{ac}	ac loss of a winding	[W]
p_{ave}	instantaneous input power	[W]
$P_{cond,S1-2}$	conduction loss of S_{1-2}	[W]
P_{cu}	copper loss	[W]
P_{Da}	loss of D_a	[W]
P_{Db}	loss of each diode used in diode bridge	[W]
P_{dc}	dc loss of a winding	[W]
P_{Dr}	loss of D_{1-2}	[W]
$P_{fe,max}$	maximum core loss	[W]
$P_{fe,sp}$	core loss per volume	$[\mathrm{W\,m^{-3}}]$
P_{fe}	core loss	[W]
$P_{h,cu}$	copper loss budget	[W]
$P_{h,fe}$	core loss budget	[W]
P_{in}	average input power	[W]
P_{loss}	total converter loss	[W]
P_{out}	output power	[W]
P_{S1-2}	total loss of S_{1-2}	[W]
P_{Ta+La}	total loss of L_a and T_a combined	[W]
P_{Tr}	total loss of T_r	[W]
Q	quality factor	$[-]$
Q_{C2}	charge stored in C_2 during T_{sw}	[C]

R_{ac}	ac resistance of a winding	[Ω]
R_{dc}	dc resistance of a winding	[Ω]
$r_{DS,on}$	ON resistance of MOSFETs	[Ω]
S_{tot}	total volt-amp rating	[V A]
t_{w}	winding thickness	[m]
T_l	line period	[s]
t_{rr}	diode reverse recovery time	[s]
T_{sw}	switching period	[s]
V_F	diode forward voltage	[V]
V_m	peak value of input sinusoidal voltage	[V]
$V_{bus,max}$	maximum of V_{bus}	[V]
V_{bus}	average dc bus voltage	[V]
v_{bus}	dc bus voltage	[V]
v_{C2}	voltage of C_2	[V]
v_{Cr}	voltage of C_r	[V]
v_{D2}	voltage of D_2	[V]
$V_{Da,max}$	maximum voltage of D_a	[V]
v_{Da}	voltage of D_a	[V]
$V_{Dr,max}$	maximum voltage of D_{1-2}	[V]
$V_{g,rms}$	rms of input voltage	[V]
v_g	input (grid) voltage	[V]
$V_{La,rms}$	rms of v_{La}	[V]
v_{La}	voltage of L_a	[V]
$V_{Lma,rms}$	rms of v_{Lma}	[V]
v_{Lma}	voltage across secondary winding of T_a	[V]
v_{Lmr}	output voltage of resonant tank	[V]
$V_{M,rms}$	rms of v_M	[V]
v_M	voltage across primary winding of T_a	[V]
v_{nr2}	voltage across secondary winding of T_r	[V]
V_o	output voltage	[V]
$V_{rect,max}$	maximum voltage of input diode bridge	[V]
v_{rect}	output voltage of diode bridge	[V]
$V_{S,max}$	maximum voltage of S_{1-2}	[V]
v_{S1-2}	drain-source voltage of S_{1-2}	[V]
v_{tank}	input voltage of resonant tank	[V]
w	winding width	[m]
z	wire diameter to skin depth ratio	[−]

Chapter 1

Introduction

LED fixtures have become more popular in Solid State Lighting (SSL) because of their long lifespan, ultra low power consumption, good Color Rendering Index (CRI), and high luminous efficacy [1–4]. Due to their reliability, flexibility, and low maintenance costs, LEDs are widely used in both residential and commercial applications, and in a variety of lighting fixtures ranging from indoor lighting bulbs and background lighting of display panels, to decorative lighting fixtures, automotive lighting modules, and streetlighting [5–10].

The LED fixtures used in streetlighting have a variety of advantages over traditional High Pressure Sodium (HPS) lamps, such as higher luminous efficacy, longer lifespan, and higher quality output light [8]. Ongoing reduction in the price of LEDs along with environmental awareness and increasing energy costs make them a viable and promising option for streetlighting.

LEDs are inherently dc loads. Therefore, an LED driver which is an ac/dc converter is required as an interface between them and the grid voltage. Based on their application, LED drivers are implemented using different topologies, and in a vast range of power from 3 W to more than 500 W. The safe operation of LED drivers is very important that several regulatory standards have been created by industry to ensure they meet certain requirements.

1.1 LED Driver Topologies

Considering their topology, LED drivers are divided into three categories as follows:

1. Single-stage LED drivers
2. Two-stage LED drivers
3. Integrated single-stage LED drivers

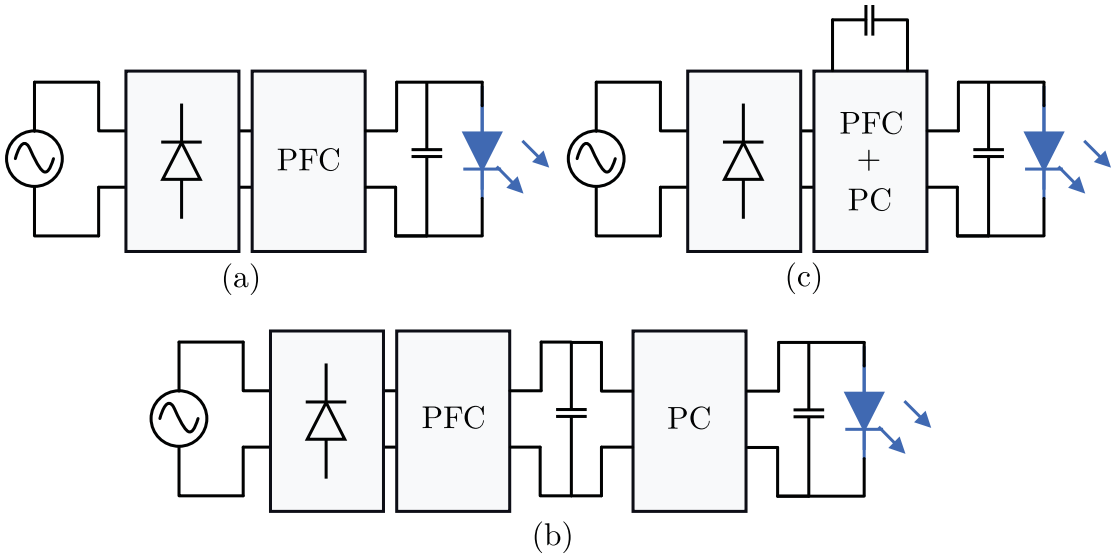


Figure 1.1: Different LED driver topologies

1.1.1 Single-Stage LED Drivers

The typical configuration of a single-stage LED driver which is an ac/dc converter with PFC capability is shown in Fig. 1.1(a). Several LED drivers based on this topology have been proposed in literature [11–15]. Single-stage LED drivers are very compact and highly efficient, but they have relatively large output current ripples that cause the LEDs to flicker. The output light flickers make the lighting environment unhealthy, and cause side effects such as fatigue and vision impairment over time [16, 17]. To limit the light flickers, the output current ripples must be reduced which is not cost effective using this configuration, especially for high power applications. Therefore, this type of LED drivers is not suitable for streetlighting. To address this problem, the PFC stage of an LED driver must be followed by a Power Conversion (PC) stage whose task is to eliminate the output current ripples.

1.1.2 Two-Stage LED Drivers

In a two-stage LED driver as shown in Fig. 1.1(b), the PC stage which is a dc/dc converter is cascaded with the PFC stage to remove the output ripples. Various two-stage LED drivers have been proposed in literature [18–22]. Despite their advantages, they have certain drawbacks, such as high component count, extra costs, and an additional control system.

1.1.3 Integrated Single-Stage LED Drivers

The configuration of an integrated single-stage LED driver is shown in Fig. 1.1(c), where the PFC and PC stages are integrated to form a single unit. To overcome the shortcomings of single-stage and two-stage LED drivers, a variety of integrated single-stage LED drivers have been proposed in literature [23–34]. This type of LED drivers is designed to achieve high PF, low THD, and reduced output light flickers with relatively lower component count, simpler control system, and lower cost. As a conclusion, this topology is the most promising choice for streetlighting.

1.2 LED Driver Requirements

Depending on the application, different requirements must be satisfied for LED drivers. Power decoupling, current balancing, and input power quality are among the most important ones that are discussed in this thesis. There are also other requirements, such as complying with Electro Magnetic Compatibility (EMC) standards, providing galvanic isolation, dimming capability, limited output voltage range, e.g. $V_o < 70$ V, IP rating, over current/voltage protections, etc.

1.2.1 Power Decoupling in LED Drivers

The instantaneous input power of an LED driver contains double-frequency oscillations, while the output power is ideally constant. The input/output power difference must be processed in the LED driver that is defined as power decoupling. As a result of poor power decoupling, double-frequency ripples appear on the output causing light flickers. As mentioned earlier, excessive light flickers in a lighting environment give rise to several possible health issues over time, and it is recommended that they be restricted as much as possible [16, 17].

Electrolytic capacitors are among the most straightforward options for power decoupling because they are compact and cost-effective. High-capacitance film capacitors on the other hand are bulky and relatively more expensive. The downside of electrolytic capacitors is the short lifetime in the range of $15,000 - 25,000$ hours, whereas film capacitors can last up to more than $50,000$ hours, at least twice as that of electrolytic ones. Reliability and long lifetime play an integral role in streetlighting LED drivers as the maintenance costs associated with replacing broken fixtures at high altitudes are prohibitive. LED modules themselves benefit from a long lifetime in the range of at least $50,000$ hours which this is one of the reasons they have dominated the market. Therefore, it is important that the lifetime of LED drivers matches

that of LED modules. Utilizing electrolytic capacitors in an LED driver reduces its durability and the reliability of the whole fixture. Thus, many researchers have been seeking for alternative solutions of power decoupling to remove electrolytic capacitors.

Various approaches have been developed to eliminate electrolytic capacitors, such as pulsating driving current [35], and input current shaping techniques [36,37] that focus on manipulating the output or input current respectively to decrease the input/output power difference. These techniques might yield satisfactory results, but at the expense of additional complexity in control and aggravated quality of either the output or input of the LED driver. The use of a magnetic element has been proposed in [18] in which by using a coupled inductor, the more optimized power flow path has been provided. In this technique, a portion of the input power reaches the load directly through the coupled inductor and without being processed twice. The problem of magnetic elements compared with capacitors is their large size and increased losses. Among all power decoupling approaches, active energy storage techniques [38–47], and control techniques [48–54] have received more attention because they yield more satisfactory reults.

1.2.1.1 Active Energy Storage Techniques

An active energy storage technique is when an auxiliary circuit is added to a regular LED driver to process the input/output power difference, or when the LED driver is modified in such a way that power processing becomes more efficient. Either way, it requires additional control systems or extra components.

A non-cascaded topology has been proposed in [43] to eliminate electrolytic capacitors by designing an energy buffer unit added to a flyback converter. Whenever the instantaneous input power is lower than the output power, additional energy is supplied from the buffer capacitor, and whenever the instantaneous power is greater than the output power, the surplus energy is stored in the buffer capacitor. In the LED driver proposed in [42], a bidirectional buck-boost converter has been connected in parallel with the output of PFC stage. The bidirectional buck-boost circuit absorbs the double-frequency current ripples existing at the output of PFC stage allowing the dc power to be delivered to LEDs. In the LED driver proposed in [44], a buck converter has been utilized on the tertiary winding of a flyback circuit as the Ripple Cancellation Converter (RCC). The LED driver is controlled such that the dc power is delivered to the load via the flyback circuit through one stage of power conversion, and the ac power is processed through both the flyback and buck stage. Another usage of the flyback topology has been proposed in [45] where a bidirectional buck

ripple-cancellation unit has been added to the tertiary winding of a flyback converter. The converter proposed in [46] is a manipulation of a single-switch flyback-forward converter in which a buck circuit has been placed between the forward converter and load to make the power processing more efficient. The objective is to improve the efficiency by making an improved 1.5-stage forward-flyback converter. The control strategy is devised such that most of the power is delivered to the load directly via the flyback stage, and the rest is delivered through the forward converter and cascaded buck stage. A non-cascaded integrated LED driver has been proposed in [47] which consists of a buck-boost stage to deliver the dc power to the load, and a boost stage for low frequency ripple cancellation. Due to the opposite polarity between the output voltage of each stage, the double-frequency voltage ripples of the boost circuit is subtracted from those of the buck-boost circuit resulting in reduced output ripples.

Some of the most notable drawbacks of active energy storage converters is their poor efficiency, complicated control systems for low-frequency ripple cancellation, and the need for extra high voltage rating MOSFETs that increase the total cost of the LED driver.

1.2.1.2 Control Techniques

The major storage elements used in an LED driver is the dc bus capacitor at the output of PFC stage and the output capacitors across LEDs. An interesting way to remove the output double-frequency ripples is by transferring them to dc bus where by accepting high voltage ripples, a small film capacitor can be chosen as dc bus capacitor. In addition, since the low frequency ripples are removed from the output, low-capacitance film capacitors can be selected as output capacitors as well.

This method was first applied to converters of Photo Voltaic (PV) solar systems [48, 52, 53], and then to LED drivers [49, 54]. In the LED driver proposed in [49], a feed-forward controller is designed for the asymmetric half-bridge stage. The Feed-Forward controller is quite effective in low-frequency ripple cancellation. However, the optimal design is challenging, and it requires a complicated digital control system that increases the hardware cost.

In the proposed LED driver, similar to [54], a control system much simpler than feed-forward controller is designed. The proposed control system removes the output double-frequency ripples and place them on the dc bus capacitor where by accepting high voltage ripples, a small durable film capacitor is selected. Finally, a 200 W electrolytic-capacitor-free LED driver is achieved. The advantage of this method is that it does not require any additional circuits or complexity in control.

1.2.2 Current Balancing in LED Strings

For a higher reliability and performance, multiple LED strings are usually paralleled with each other at the output of lighting fixtures. However, because of the non-linear I-V characteristic of LEDs, current imbalance might happen between different LED strings in parallel resulting in inconsistent output light, and reduced lifetime of the lighting fixture.

Different active and passive techniques have been proposed to address this problem, such as active balancing techniques based on either linear current regulators [55, 56] or switching-mode current regulators [57]. Active current balancing techniques fall short in comparison with passive techniques as they suffer from increased cost and component count, as well as complex control and reduced efficiency. On the other hand, passive current balancing methods use generally simple structures based on passive elements to address the current balancing issue.

Passive techniques are divided into resistive, inductive, and capacitive approaches. Resistive schemes [58] are used to linearize LED loads with the help of series resistors. Their main shortcoming is the extra power dissipation in resistors making this method impractical for high power LED drivers. Inductive schemes use magnetic components like inductors and transformers [59]. They improve the converter in terms of thermal capability and lifetime, but they reduce the power density. In addition, they suffer from extra winding and core losses that worsen the overall efficiency. Finally, capacitive schemes seem to be the most promising solution for current balancing as not only are they almost lossless, but they also improve the overall lifetime and power density of the LED driver.

Various capacitive current balancing schemes have been proposed [15,23,60–63] which most of them rely on the charge-balance property of capacitors. Current balancing is discussed in Appendix.

1.2.3 Input Power Quality

Based on Energy Star program for commercial lighting, streetlighting LED drivers must have a PF greater than 0.9, [64]. In addition, IEC 61000-3-2 Class C requirements set certain limits for input current harmonics [65]. These two obligations make it imperative to utilize a PFC circuit for streetlighting LED drivers.

In integrated single-stage LED drivers, the PFC circuit is usually designed to operate in DCM, and the PC stage is responsible for regulating the output. Based on the topology of PFC circuit, integrated single-stage LED drivers are divided into three main categories as stated below:

1. Buck PFC LED drivers [23].
2. Boost PFC LED drivers [24–26, 28, 29, 50, 66].
3. Buck-boost PFC LED drivers [27, 30–34].

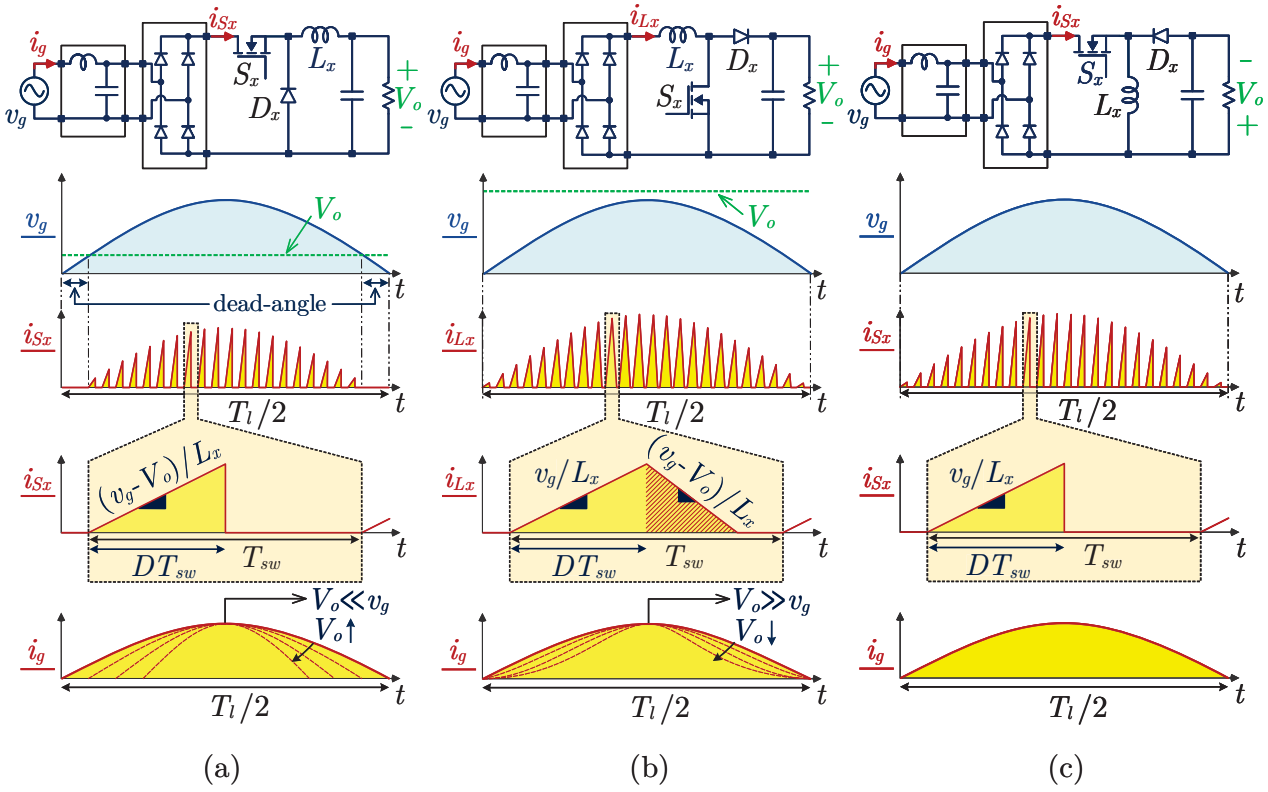


Figure 1.2: Different types of PFC circuits operating in DCM

1.2.3.1 Buck PFC

Consider the buck PFC circuit shown in Fig. 1.2(a). In this circuit, the average of input rectified current denoted as i_{Sx} is a function of both input voltage (v_g) and output voltage (V_o). When V_o is much smaller than v_g, the dependency of i_g on V_o becomes weaker, and it nearly becomes a linear function of only v_g which this results in acceptable PF and THD.

Although lowering the output voltage of buck PFC cicuit helps in improving the input power quality, the efficiency is compromised due to increased conduction losses of the buck inductor and diode. In addition, as illustrated in Fig. 1.2(a), the dead angle appearing on the input current waveform is another problem associated with DCM buck PFC circuits that might cause the LED driver not to meet the required PF and THD regulatory standards.

An LED driver with a hybrid switched-inductor buck PFC circuit instead of a conventional one has been proposed in [13] to lower conduction losses. An inverted buck LED driver achieving a small dead angle has been proposed in [12], and a buck PFC circuit integrated with a resonant dc-dc unit has been proposed in [23].

1.2.3.2 Boost PFC

Consider the boost PFC circuit shown in Fig. 1.2(b). Because of the hatched area on i_{Lx} waveform during a switching period (T_{sw}), the average of input rectified current denoted as i_{Lx} is a function of both v_g and V_o. When V_o is much greater than v_g, the dependency of input current (i_g) on V_o becomes weaker, and it nearly becomes a linear function of only v_g resulting in acceptable PF and THD.

Several integrated single-stage LED drivers based on DCM boost PFC circuit have been proposed in literature, such as the integrated boost-flyback converter proposed in [25], the LED drivers integrating a boost-typed PFC circuit with a half-bridge converter proposed in [29, 50], and the integrated bridgeless boost PFC half-bridge LED drivers proposed in [24, 26, 28, 66].

The downside of boost PFC circuits is that to get acceptable PF, the output voltage must be at least twice the input voltage. This in turn increases the voltage stress of components, and the total cost of the LED driver. This issue is more severe when the LED driver is designed for the universal input voltage range, or input voltage range of $(185 - 265)$ V_{rms} adopted by European and some other countries. As a result, DCM boost PFC circuits are not normally utilized in integrated single-stage LED drivers that are designed for this input voltage range.

1.2.3.3 Buck-Boost PFC

Consider the buck-boost PFC circuit shown in Fig. 1.2(c). Unlike the other two types of PFC circuits, in a buck-boost PFC circuit, the average of input rectified current denoted as i_{Sx} is a linear function of only v_g which this results in unity PF and zero THD in theory.

Several integrated single-stage LED drivers based on DCM buck-boost PFC circuit have been proposed in literature. Buck-boost PFC circuits are commonly integrated with flyback, class E, or half-bridge resonant converters. A buck-boost PFC circuit integrated with a flyback converter has been proposed in [34]. Albeit this structure is very compact, the power switch suffers from hard-switching which has decreased the efficiency to below 90%. The integration of buck-boost PFC circuit with an isolated dc/dc converter with voltage doubler rectifier has been proposed in [30] in which below 90% efficiency has been achieved for a 120 W prototype due to hard-switching losses. An integration of a buck-boost PFC circuit with a class E resonant converter has been proposed in [32] in which an almost unity PF, 5% THD, and around 91% efficiency have been achieved for a 100 W prototype.

Owing to the soft-switching capability of half-bridge resonant converters and their simpler structure compared with class E resonant converters, the integration of a buck-boost PFC circuit with a half-bridge resonant converter yields the highest efficiency, and is the best possible configuration for streetlighting LED drivers. However, it has certain problems that are addressed in the LED driver proposed in this thesis.

A single-stage LED driver by integrating a buck-boost PFC circuit with a half-bridge LLC resonant converter has been proposed in [33] where to ensure the proper operation of the buck-boost PFC circuit, extra diodes have been added that not only increase the costs, but also decrease the converter efficiency. A buck-boost typed PFC circuit integrated with a half-bridge CLCL resonant converter has been proposed in [27] where even though this LED driver is bridgeless, it still contains four extra diodes. Finally, [31] has proposed a SEPIC PFC circuit integrated with a half-bridge LLC resonant converter where again additional diodes have been utilized to ensure the buck-boost typed PFC operation.

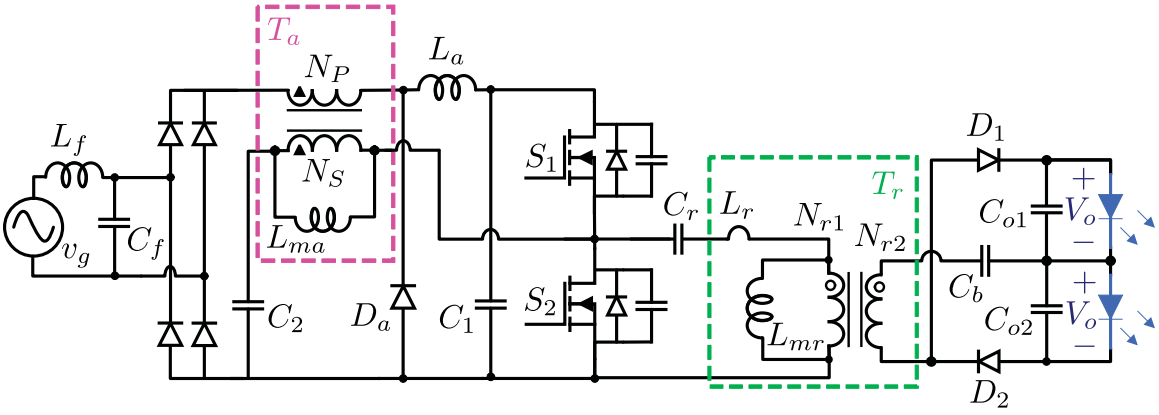


Figure 1.3: The proposed LED driver

1.3 Description of the Proposed LED Driver

The proposed LED driver in thesis shown in Fig. 1.3, is composed of a buck-boost typed PFC circuit integrated with a half-bridge LLC resonant converter in which transformer T_a acts like the buck-boost switch. Therefore, the extra diodes used in previous buck-boost half-bridge converters [27, 31, 33] are eliminated. With a fixed duty cycle, switching frequency is used as the control variable. Therefore, Pulse Frequency Modulation (PFM) is used to regulate the converter. Since high PF and low THD are achieved with the DCM operation of input current, S_1 and S_2 are utilized to regulate the output current and make a flicker-free LED driver. Owing to the proposed control system [48,52–54], output current ripples are attenuated without using any low-lifetime electrolytic capacitors. The LLC resonant circuit is designed such that the ZVS of S_1 and S_2 is ensured for a wide operating range. On the LED side, a passive current balancing scheme is adopted which is not depicted in Fig. 1.3, but will be discussed in the "Current Balancing" chapter in Appendix.

The transformer and inductor of PFC circuit are integrated on the same core to improve the efficiency and power density. In addition, the average dc bus voltage denoted as V_{bus} is limited to approximately the peak value of input sinusoidal voltage which helps in lowering the voltage stress of S_1 and S_2. The circuit is implemented and for a wide input voltage and power range, the peak efficiency of 94.6 % is measured.

1.4 Thesis Objectives

The main objectives of this thesis are summarized as follows:

1. To design an integrated single-stage LED driver suitable for input voltage range of $(185 - 265)\mathrm{V}_{rms}$ with high PF, low THD, and low output ripples.

2. To design a buck-boost typed PFC circuit that results in unity PF and zero THD in theory with minimum component count.

3. To design an LED driver with very limited dc bus voltage to lower the voltage stress of MOSFETs.

4. To design a robust controller that eliminates output ripples, and makes it possible to remove electrolytic capacitors.

5. To design an optimal magnetic integration to minimize corresponding losses and increase the total efficiency.

6. To verify the design through an experimental prototype.

1.5 Thesis Outline

This thesis is organized as follows:

Chapter 2 explains briefly about PF and THD requirements of streetlighting LED drivers. The proposed PFC topology is presented, and the topology and principles of operation are comprehensively investigated. In addition, theoretical PF and THD of the proposed LED driver are calculated. Finally, simulation and experimental results are presented to verify the performance of PFC circuit. Moreover, by using a Tektronix power analyzer model PA4000, the harmonic content of the input current is measured for three different input voltage.

Chapter 3 begins by explaining briefly about LLC resonant converters, and ZVS as one of the benefits. The design parameters of the LLC resonant circuit are also obtained. Subsequently, the formula of average dc bus voltage is obtained in terms of circuit parameters to verify the limited dc bus voltage range. The control system of the proposed LED driver is also presented that helps in eliminating electrolytic capacitors. At the end, simulation and experimental results are provided to validate the effectiveness of the LLC resonant circuit, limited dc bus voltage, and proposed control sytem.

Chapter 4 thoroughly investigates the optimum design of PFC integrated transformer and inductor. This chapter discusses the design steps essential for every magnetic design in details, and verifies the proposed magnetic design by calculating the maximum flux density, core loss, and copper loss including both dc ohmic and high frequency ac losses. It also gives insight into the importance of Litz wires in high frequency applications, skin effect and proximity effect concepts, and the importance of good winding arrangements to minimize corresponding losses. In addition, the magnetic integration of resonant inductor and transformer is briefly discussed. At the end, the experimental prototypes of both magnetic integrations are presented.

Chapter 5 discusses the design steps of different components. Loss and stress analyses of all component are also carried out to determine their restrictions, and expected losses. Based on stress analysis, the best possible components are selected for the experimental prototype, and based on loss analysis, the lowest efficiency of the converter at full-load is calculated. At the end, by using a Tektronix 5 series Mixed Signal Oscilloscope model MS058, the efficiency of the experimental prototype is measured and presented for several operating points.

Chapter 6 summarizes the contributions, and provides suggestions for further improvement of the design.

Ultimately in Appendix, the importance of current balancing in LED drivers is briefly discussed, and the adopted current balancing scheme and the modes of operation are analyzed. At the end, simulation and experimental results of the four outputs are presented to verify the current balancing performance.

Chapter 2

Power Factor Correction

Power Factor (PF) is an index determining the quality of power utilization. The lower the PF of a certain electrical device, the higher the current drawn from the grid for the same amount of power. This increased current that can also be accompanied by different orders of harmonics, creates excessive power loss in power system. Lighting applications account for about 19 % of total electrical energy consumption in the world [34]. Therefore, they play an integral role in reducing the total electrical power consumption. This has given rise to increasing share and popularity of LED lighting products because of their low power consumption. Nevertheless, LEDs are inherently non-linear loads with an adverse effect on power utilization. Certain standards, such as IEC 61000-3-2 Class C [65], and U.S. Energy Star program [64] have set certain requirements for PF and input current harmonics of LED lighting products. According to Energy Star standard, the PF of high-power commercial LED lighting products must be greater than 0.9. In addition, regarding IEC standard, the input current harmonics must be within the IEC 61000-3-2 Class C standard limits shown in Table. 2.1.

Table 2.1: IEC 61000-3-2 Class C standard limits

Harmonic order	Harmonic current/Input current (%)
2	2
3	≈ 30
5	10
7	7
9	5
11	3
13	3
15	3

To comply with these requirements, high power LED drivers like the ones used in streetlighting must utilize a PFC circuit to ensure meeting the aforementioned standards.

In this chapter, a novel DCM buck-boost typed PFC circuit is firstly proposed. Then the converter and operating principles are analyzed, and the theoretical PF and THD are calculated as well. Finally, simulation and experimental results are provided to verify the performance of PFC operation.

2.1 The Proposed PFC Topology

The 200 W streetlighting LED driver proposed in this thesis is a single-stage, soft-switching, high PF converter with no electrolytic capacitors that is composed of a buck-boost typed PFC rectifier integrated with an asymmetric half-bridge LLC resonant converter as shown in Fig. 2.1.

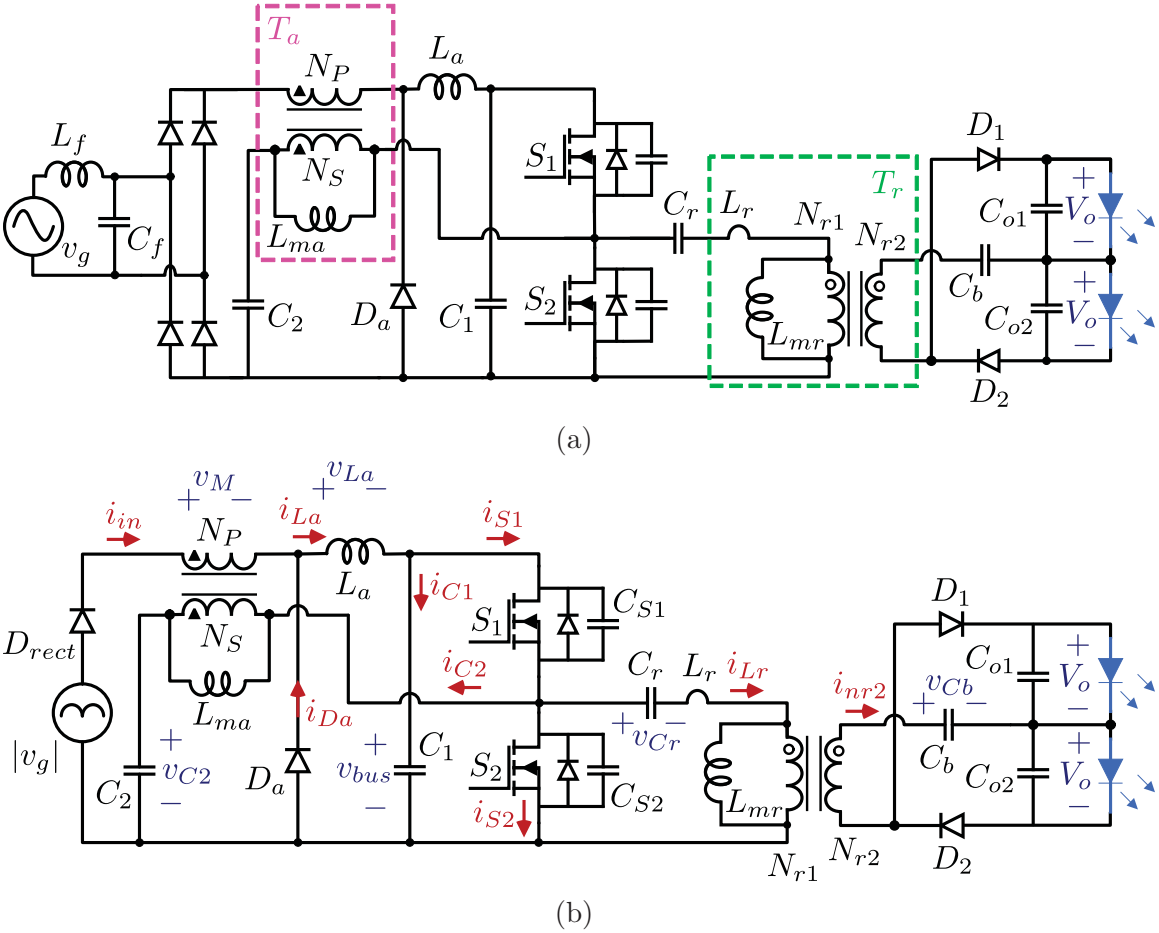


Figure 2.1: (a) Equivalent circuit of the proposed LED driver, and (b) the simplified circuit

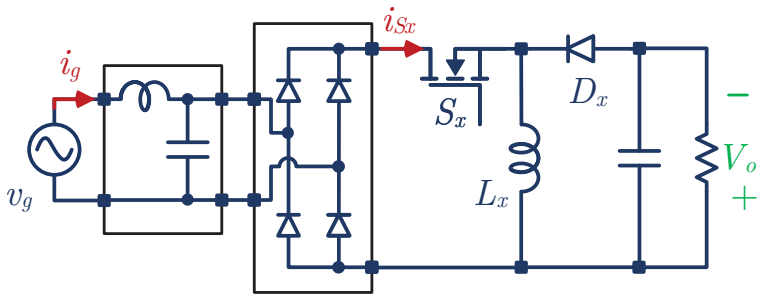


Figure 2.2: Buck-boost circuit

In the proposed LED driver, T_a acts like the buck-boost switch. Therefore, the extra diodes utilized in previous integrated buck-boost half-bridge LED drivers are removed. This results in lower component count, higher power density, and higher efficiency. Corresponding to the buck-boost circuit shown in Fig. 2.2, T_a acts like S_x, D_a acts like D_x, and L_a acts like L_x. The proposed PFC circuit might seem like a buck converter, but as shown in (2.4), if $n = \dfrac{N_P}{N_S} = 2$ is selected, in the first half of switching period, the voltage across L_a denoted as v_{La} becomes a function of only v_g and independent of v_{bus}. By mimicking the PFC behavior of a DCM buck-boost converter, the best possible PF and THD are obtained without designing any control system for input current shaping.

2.2 Principles of Operation

Depending on the ON/OFF state of switches, seven operating intervals are conceivable for the proposed LED driver. To simplify the analysis, following assumptions are made:

1. The MOSFETs and diodes are ideal which means their ON-state voltage equals zero, and they resemble an infinity resistor in OFF-state.

2. The current balancing scheme of the LED driver is different from what is presented here, and will be analyzed in Appendix. In addition, the LED driver is composed of four outputs. Since neither of these two affects the converter analysis, for simplicity they are not considered.

The key waveforms of the converter are illustrated in Fig. 2.3.

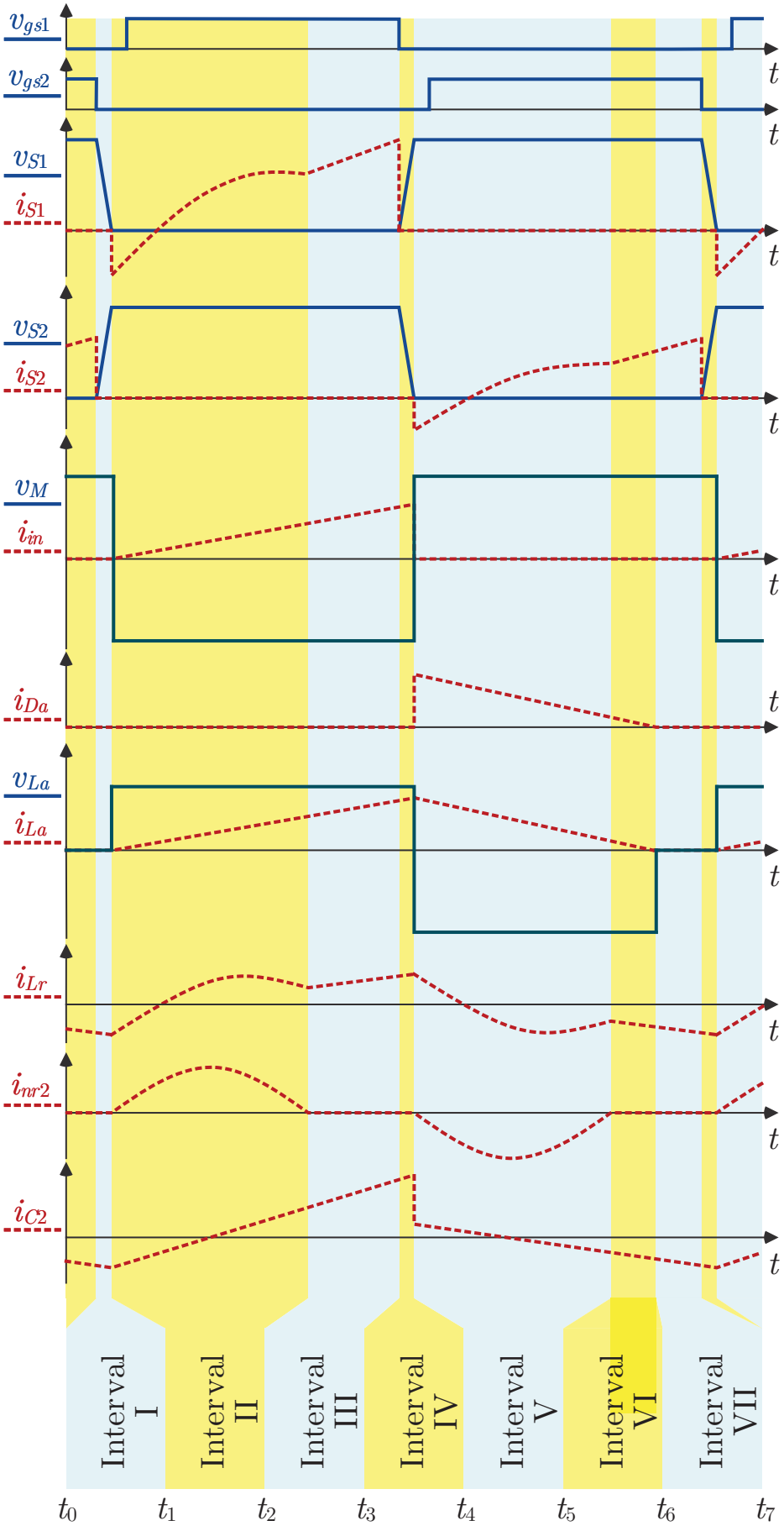


Figure 2.3: Theoretical key waveforms of the proposed LED driver

2.2.1 Interval I, $[t_0 - t_1]$

Before this interval, S_2 was ON having discharged C_{S2}. When S_2 turns OFF and before S_1 turns ON, C_{S1} discharges completely. Input and output rectifying diodes are OFF in this interval.

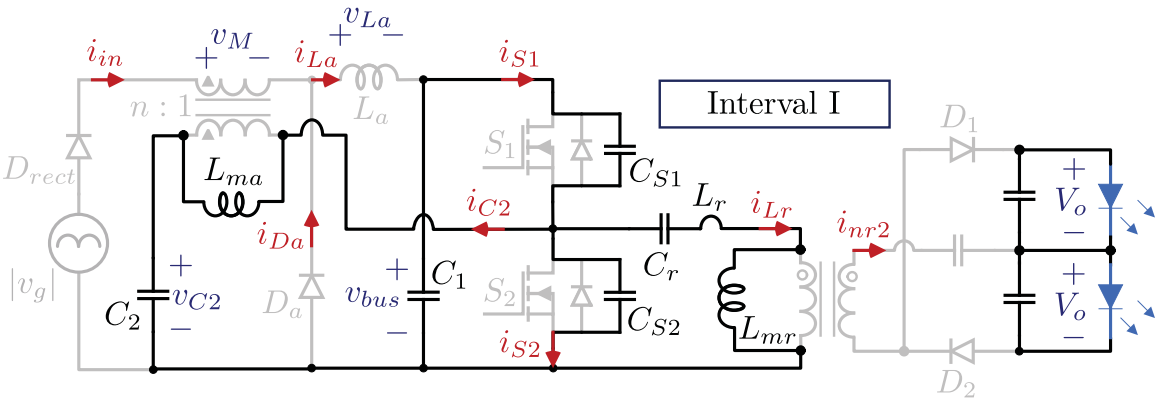


Figure 2.4: Interval I of the converter operation

2.2.2 Interval II, $[t_1 - t_2]$

At the beginning of this interval, the body diode of S_1 begins to conduct to ensure the ZVS of switch before the MOSFET of S_1 turns ON.

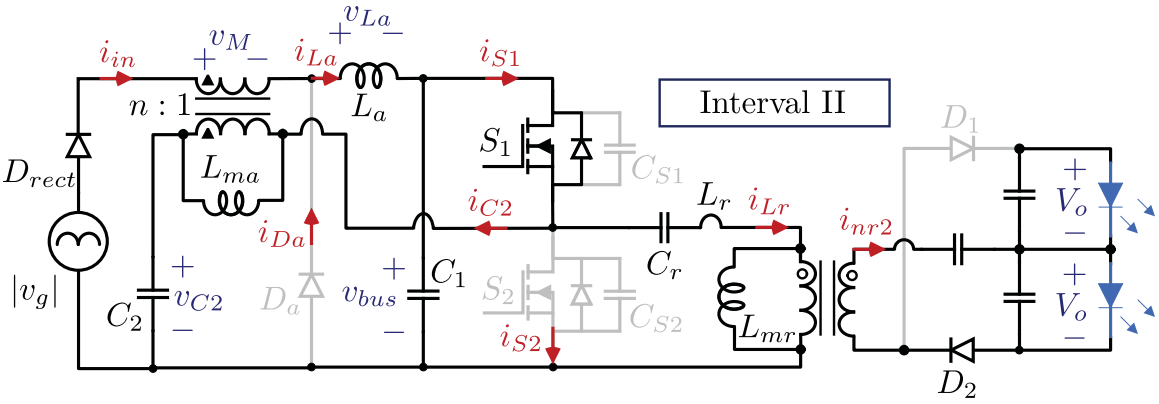


Figure 2.5: Interval II of the converter operation

By writing a KVL, it is obtained that:

$$v_M(t) = n(v_{C2} - v_{bus}). \tag{2.1}$$

For an asymmetric half bridge converter assuming $D = 0.5$, it can be written that:

$$v_{C2} = \frac{v_{bus}}{2}. \tag{2.2}$$

Then (2.1) can be rewritten as:

$$v_M(t) = n(v_{C2} - v_{bus}) = -\frac{n}{2}v_{bus}. \tag{2.3}$$

By writing another KVL, it is obtained that:

$$v_{La}(t) = |v_g| - v_M(t) - v_{bus} = |v_g| + (\frac{n}{2} - 1)v_{bus}. \tag{2.4}$$

To get unity PF, v_{La} in (2.4) must be independent of v_{bus}. Therefore, $n = 2$ must be selected as the primary to secondary turns ratio of PFC transformer. Then, the last two equations are changed as follows:

$$v_{La}(t) = |v_g|, \tag{2.5}$$

and

$$v_M(t) = -v_{bus}. \tag{2.6}$$

In this interval, the current of L_a denoted as i_{La} starts to increase linearly from zero. The current of the secondary winding of LLC transformer denoted as i_{nr2} is positive, and thus D_2 conducts. This interval continues until i_{nr2} becomes zero.

2.2.3 Interval III, $[t_2 - t_3]$

At this interval, because i_{nr2} becomes zero, D_2 stops conducting. MOSFET of S_1 is still ON, and the rest of components operate the same as previous interval.

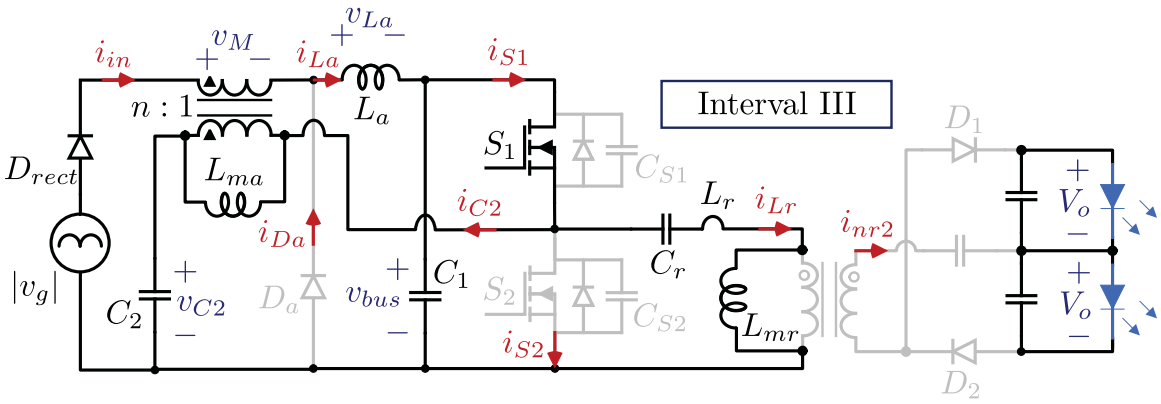


Figure 2.6: Interval III of the converter operation

2.2.4 Interval IV, $[t_3 - t_4]$

Before this interval, S_1 was ON having discharged C_{S1}. When S_1 turns OFF and before S_2 turns ON, C_{S2} discharges completely. Because i_{in} is still positive, D_{rect} continues to conduct, and since i_{nr2} is still zero, D_1 and D_2 do not conduct.

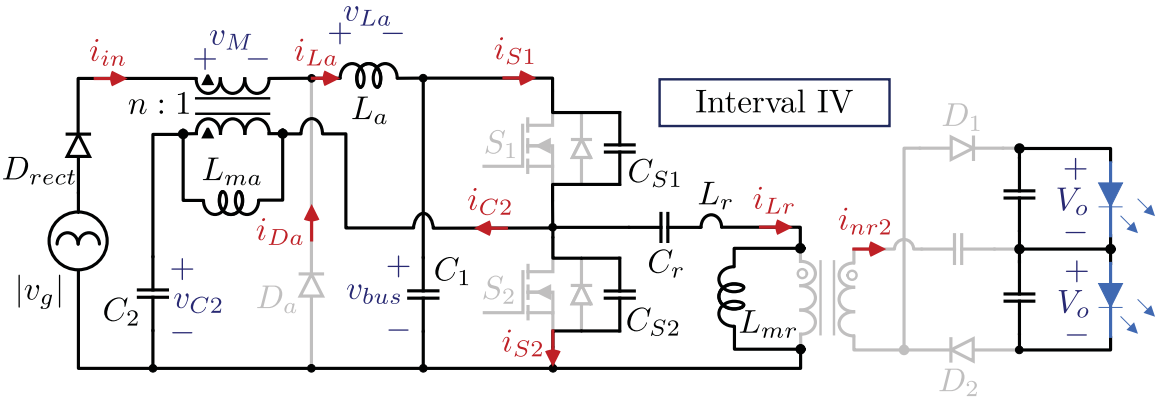


Figure 2.7: Interval IV of the converter operation

2.2.5 Interval V, $[t_4 - t_5]$

At the beginning of this interval, the body diode of S_2 begins to conduct to ensure the ZVS of switch before the MOSFET of S_2 turns ON.

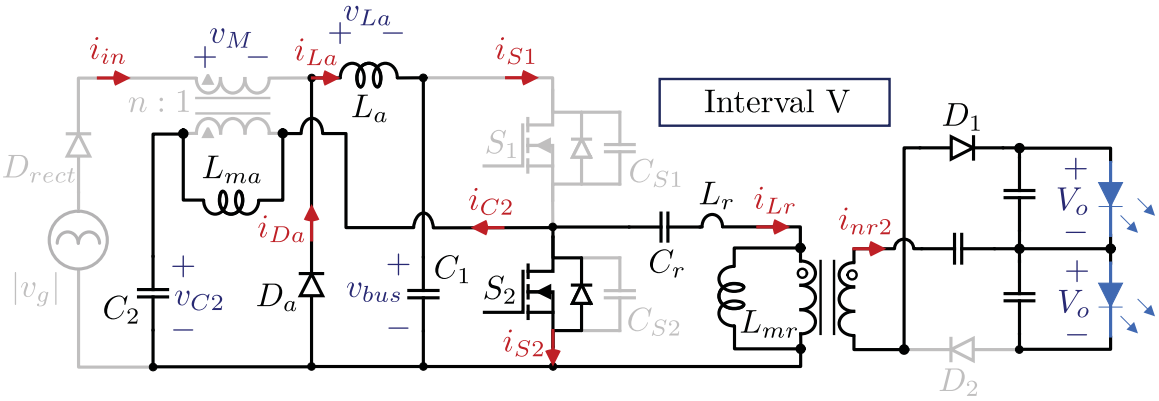


Figure 2.8: Interval V of the converter operation

By writing a KVL, and since $n = 2$, it is obtained that:

$$\frac{v_M(t)}{2} = v_{C2} \tag{2.7}$$

which can be stated as:

$$v_M(t) = 2v_{C2} = v_{bus} > 0. \tag{2.8}$$

With the change of voltage polarity across the primary winding of T_a, input current i_{in} becomes zero causing D_{rect} to stop conducting. In this interval, the voltage across L_a is determined as:

$$v_{La}(t) = -v_{bus}. \tag{2.9}$$

This causes D_a to start conducting. Moreover, since i_{nr2} is negative, D_1 conducts. This interval continues until i_{nr2} becomes zero.

2.2.6 Interval VI, $[t_5 - t_6]$

At this interval, because i_{nr2} becomes zero, D_1 stops conducting. MOSFET of S_2 is still ON, and the rest of components operate the same as previous interval.

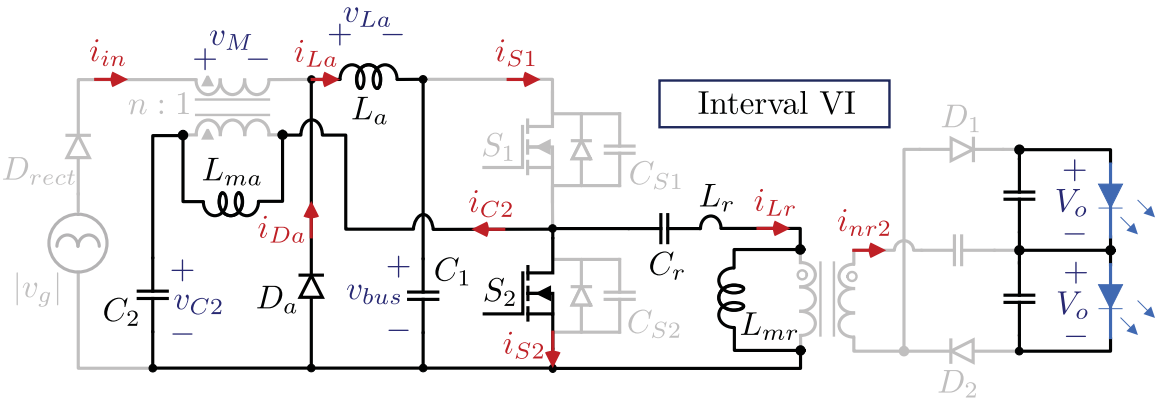


Figure 2.9: Interval VI of the converter operation

2.2.7 Interval VII, $[t_6 - t_7]$

At this interval, and since both i_{La} and i_{in} are zero, D_a stops conducting.

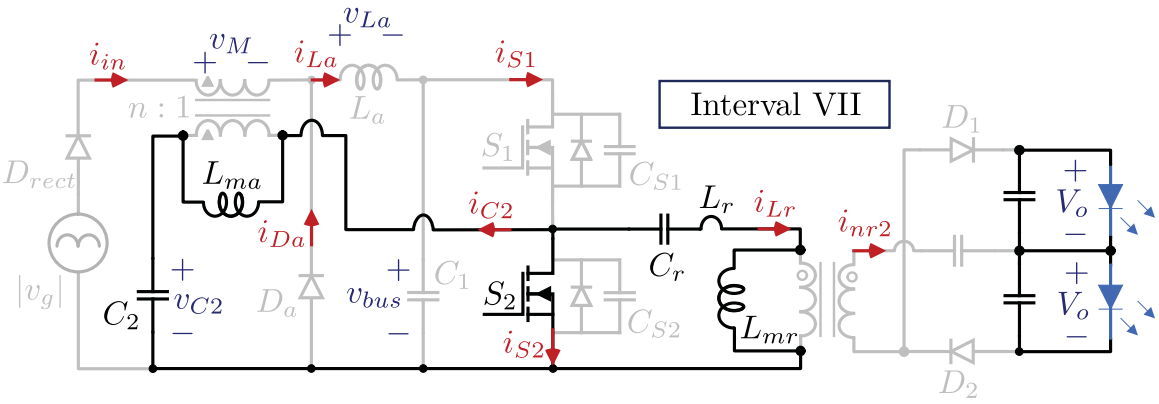


Figure 2.10: Interval VII of the converter operation

During $t_1 < t < t_4$, and according to (2.5), v_{La} is obtained as:

$$v_{La}(t) = |v_g|, \tag{2.10}$$

during $t_4 < t < t_6$, and according to (2.9), v_{La} is obtained as:

$$v_{La}(t) = -v_{bus}, \tag{2.11}$$

and during $t_6 < t < t_7$, it is obtained as:

$$v_{La}(t) = 0. \tag{2.12}$$

According to the volt-second balance of L_a, the time duration $\Delta t_d = t_6 - t_4$ when D_a conducts is determined as:

$$\Delta t_d = \frac{|v_g|}{2 f_{sw} v_{bus}} = \frac{V_m}{2 f_{sw} v_{bus}} |\sin \omega_l t|, \tag{2.13}$$

where V_m is the peak value of input sinusoidal voltage, and ω_l is angular line frequency. Moreover, in this interval, because i_{nr2} is still zero, D_1 and D_2 do not conduct. This interval continues until S_2 turns OFF.

2.3 Theoretical Calculation of PF and THD

By considering Fig. 2.3, the maximum of i_{in} during a switching period which is denoted as $\hat{i}_{in}$ is calculated. During $t_1 < t < t_4$, since D_a does not conduct, it can be written that:

$$i_{in}(t) = i_{La}(t), \tag{2.14}$$

and according to (2.5), v_{La} can be written as:

$$v_{La}(t) = |v_g| = V_m |\sin \omega_l t|. \tag{2.15}$$

Then by writing the voltage-current relationship of L_a, it is obtained that:

$$|v_g| = L_a \frac{\hat{i}_{in}}{(t_4 - t_1)}, \tag{2.16}$$

where

$$t_4 - t_1 = \frac{T_{sw}}{2}. \tag{2.17}$$

Then, $\hat{i}_{in}$ is obtained as:

$$\hat{i}_{in} = \frac{|v_g|}{2f_{sw}L_a} = \frac{V_m|\sin\omega_l t|}{2f_{sw}L_a}, \tag{2.18}$$

where f_{sw} is switching frequency.

The PFC section of the proposed LED driver is shown in Fig. 2.11. To calculate the PF, first the average of i_{in} over a switching period which is denoted as $i_{in,ave}$ is determined based on its waveform shown in Fig. 2.3 as:

$$i_{in,ave} = \frac{\hat{i}_{in}\dfrac{T_{sw}}{2}}{2T_{sw}} \overset{(2.18)}{=} \frac{V_m|\sin\omega_l t|}{8f_{sw}L_a}. \tag{2.19}$$

Then, the Root Mean Square (RMS) of input current (i_g) is calculated as:

$$i_g = \frac{V_m \sin\omega_l t}{8f_{sw}L_a} \implies I_{g,rms} = \frac{V_m}{8\sqrt{2}L_a f_{sw}}. \tag{2.20}$$

Finally, the theoretical PF of the proposed converter is determined according to the formula of P_{in} obtained in (5.5) as:

$$PF = \frac{P}{S} = \frac{P_{in}}{V_{g,rms} \times I_{g,rms}} = \frac{\dfrac{V_m^2}{16f_{sw}L_a}}{\dfrac{V_m}{\sqrt{2}} \times \dfrac{V_m}{8\sqrt{2}L_a f_{sw}}} = 1. \tag{2.21}$$

Consequently, theoretical $THD = 0\%$ is inferred.

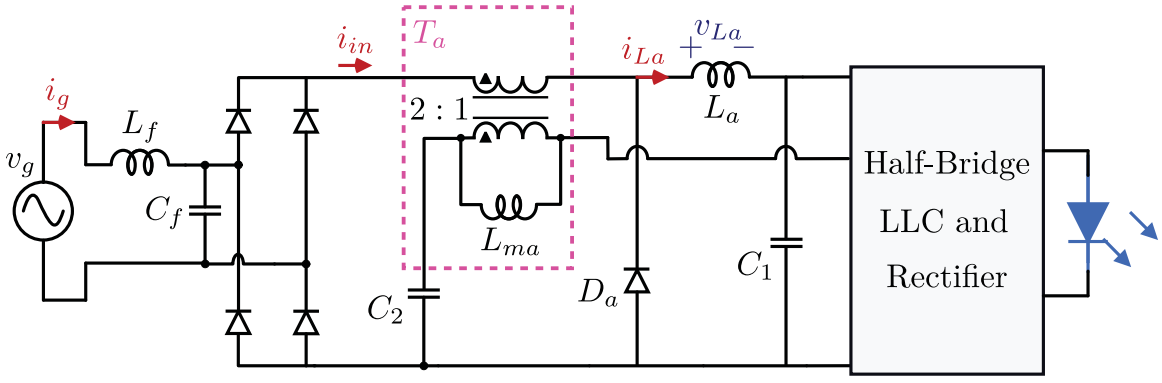
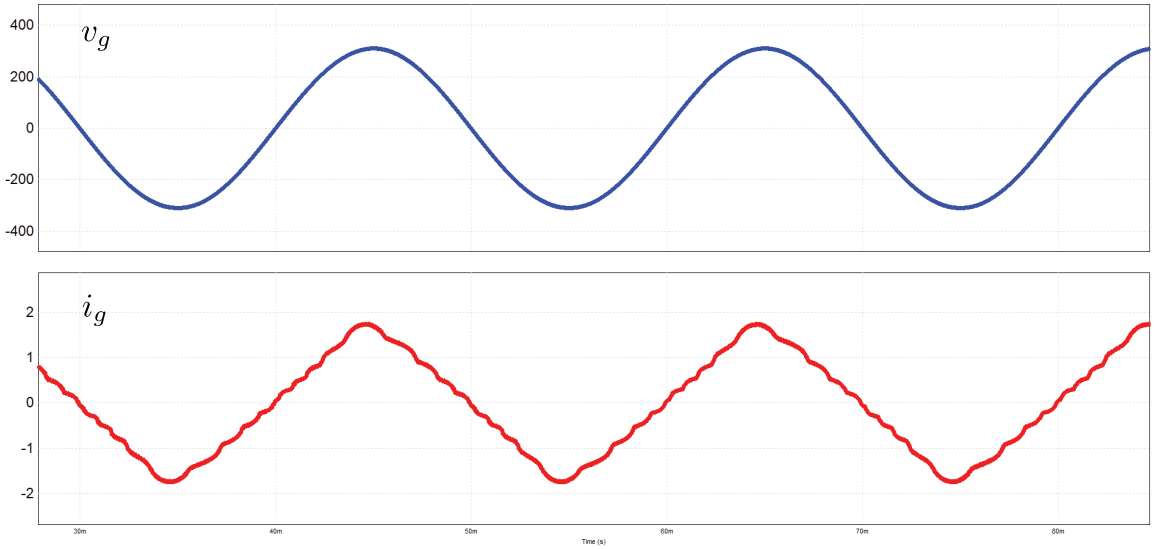


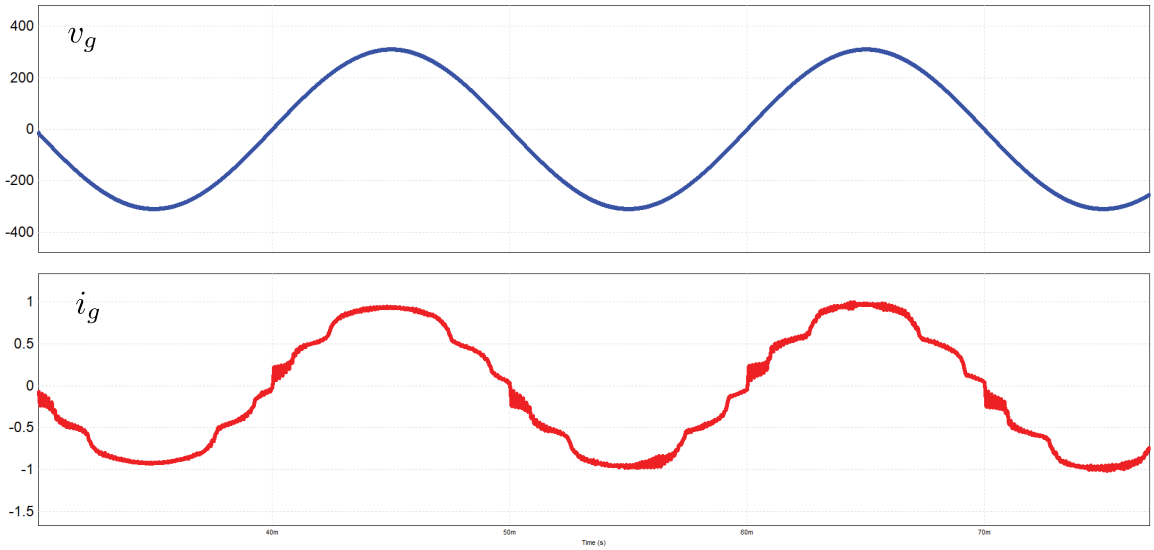
Figure 2.11: PFC section of the proposed converter

2.4 Simulation and Experimental Results

The simulation results of the PFC circuit are shown in Fig. 2.12 and Fig. 2.13 for different operating points in which the parasitic elements of the converter are considered.

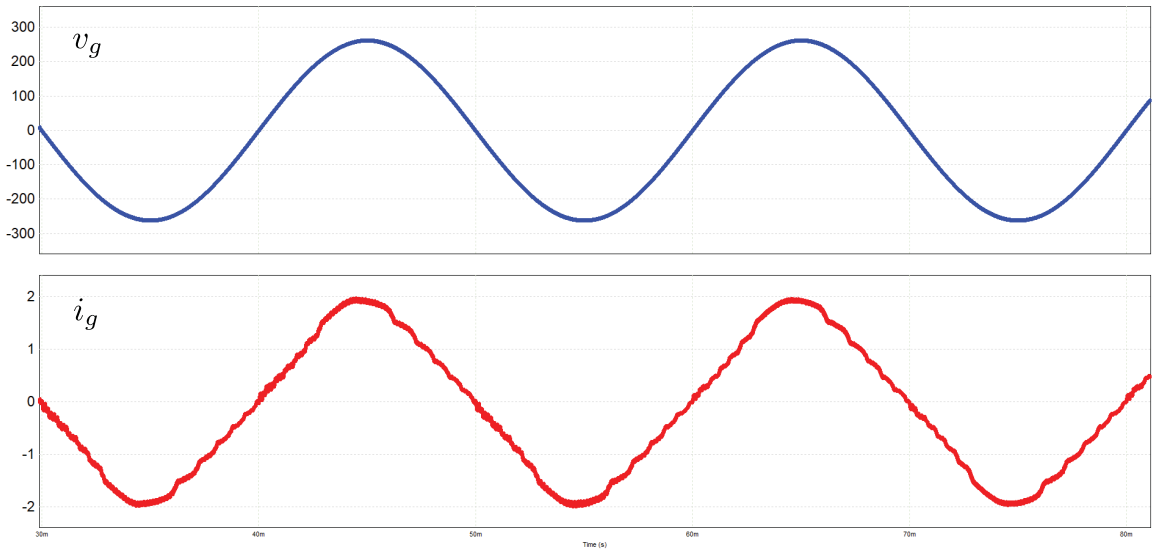


(a)

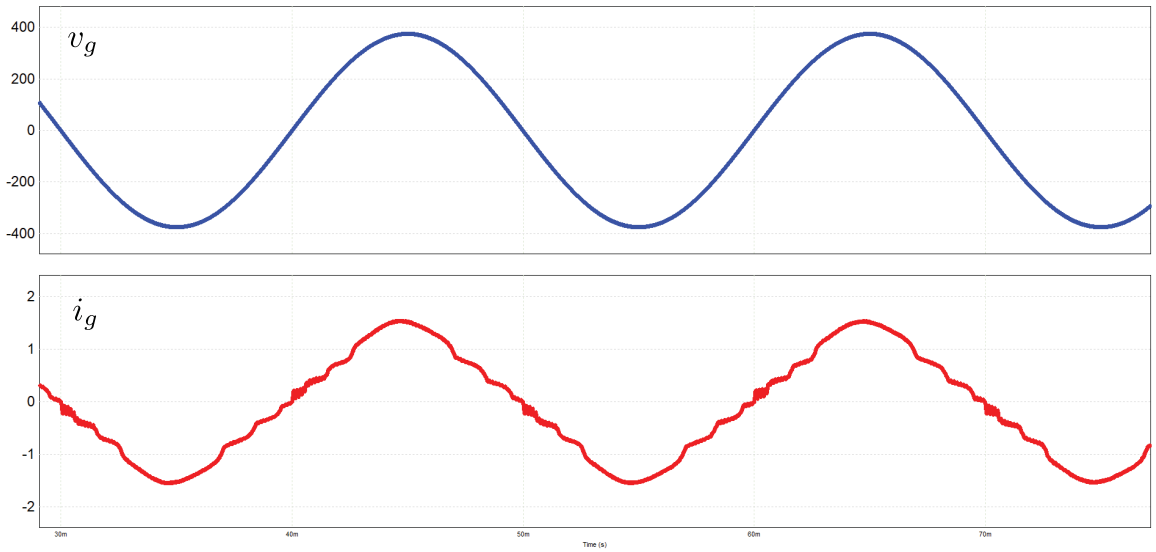


(b)

Figure 2.12: Input voltage and current waveforms at nominal input voltage at (a) full-load, (b) light-load



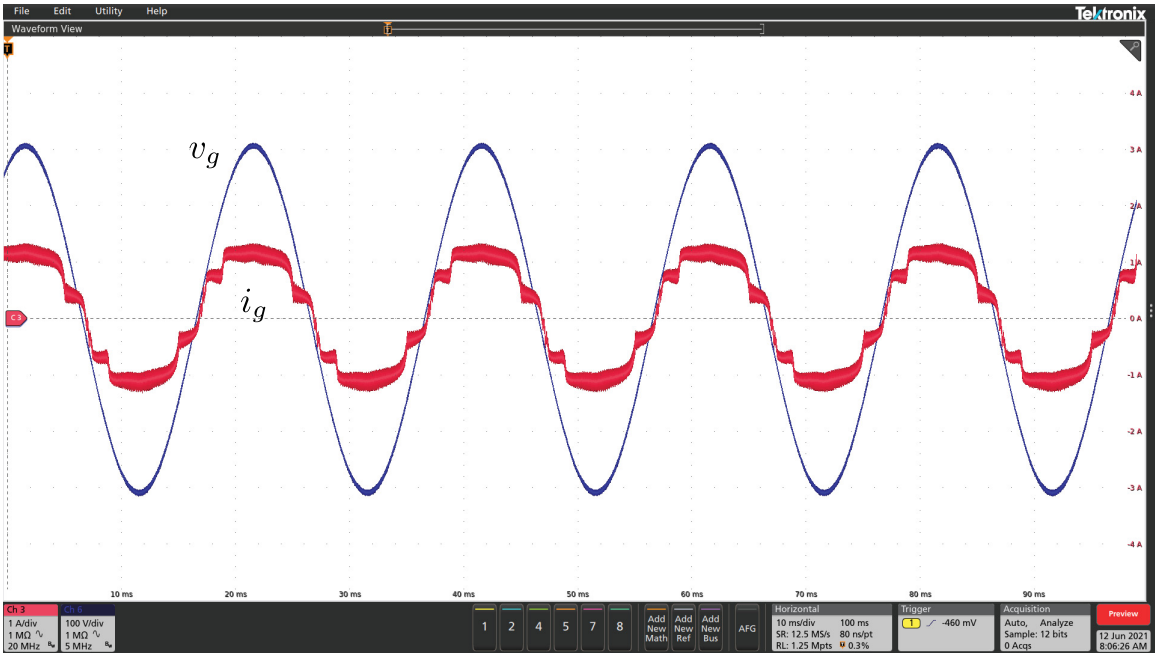
(a)



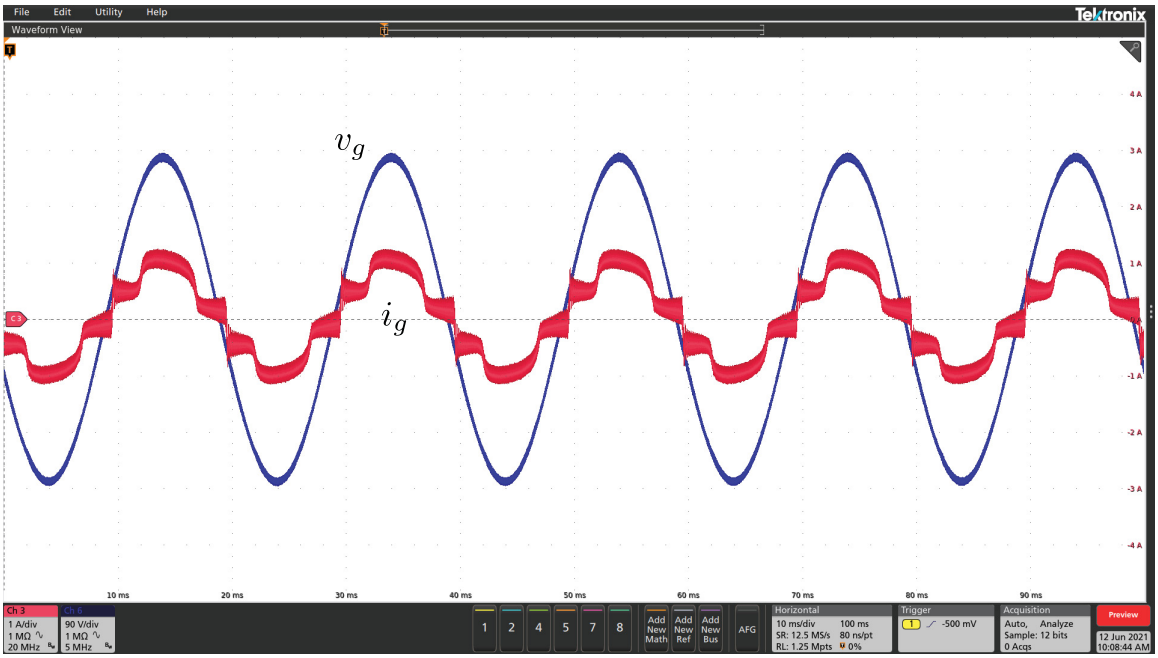
(b)

Figure 2.13: Input voltage and current waveforms at rated power at (a) minimum input voltage, (b) maximum input voltage

The experimental results are shown in Fig. 2.14 and Fig. 2.15 for different operating points.

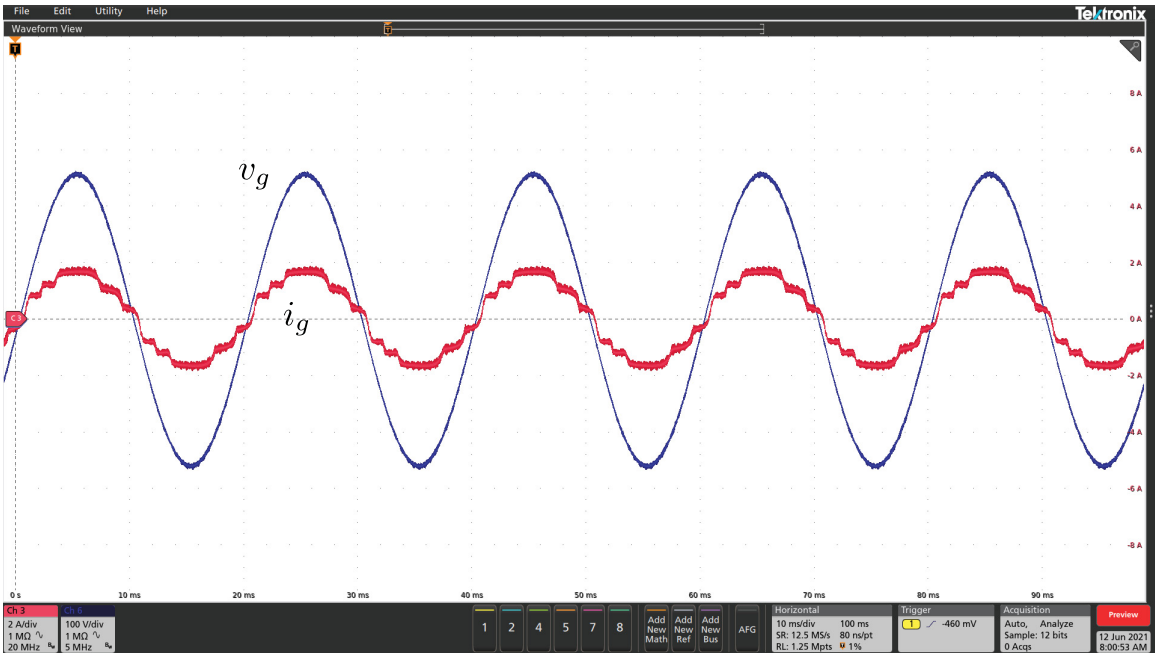


(a)

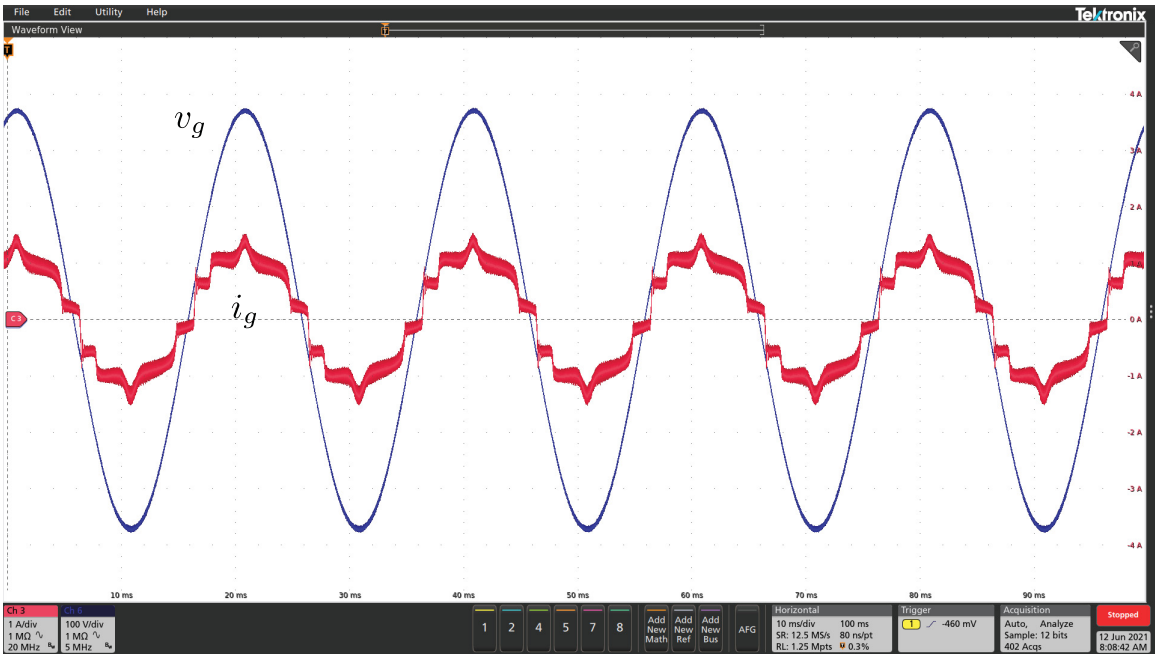


(b)

Figure 2.14: Input voltage and current waveforms at (a) full-load, (b) light-load



(a)

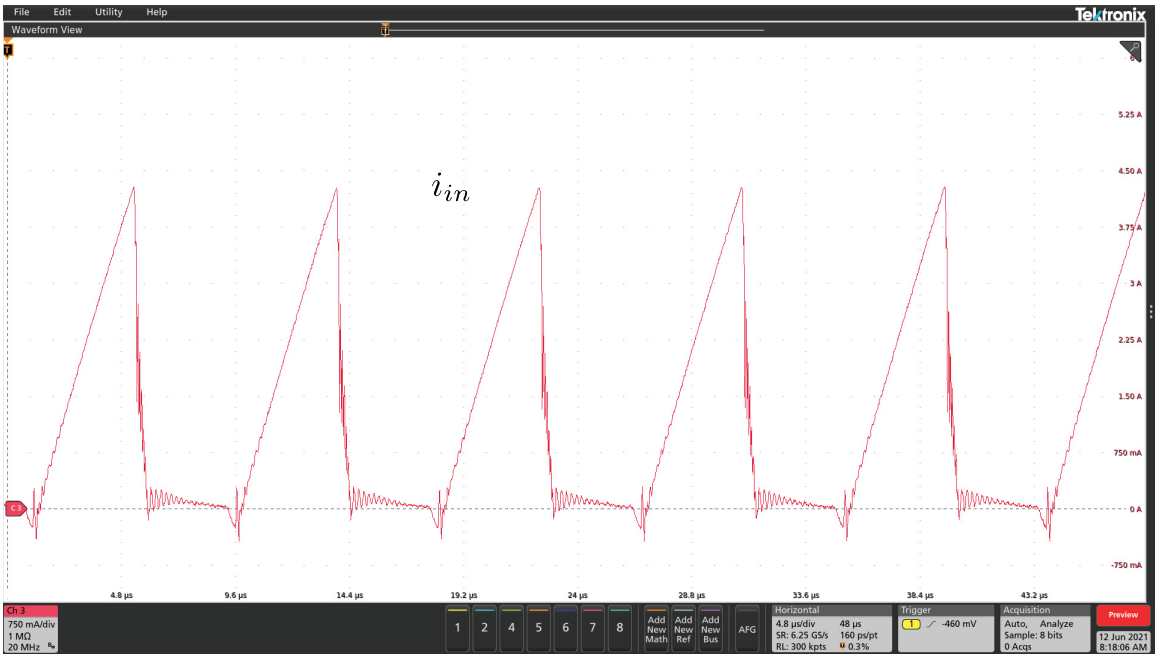


(b)

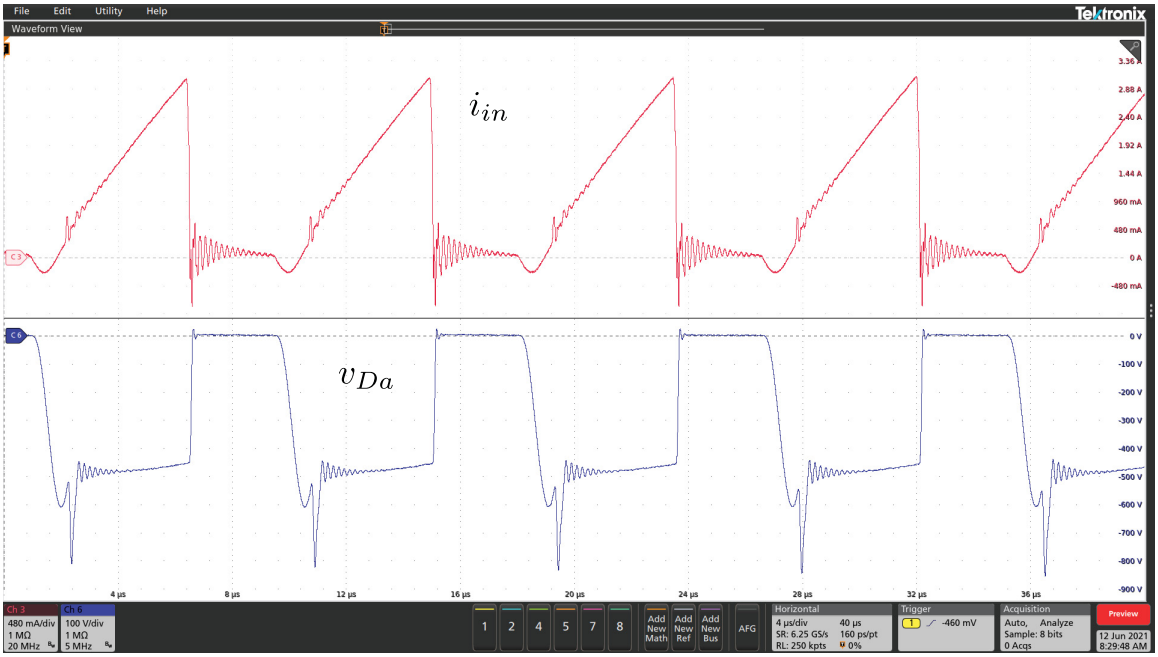
Figure 2.15: Input voltage and current waveforms at rated power at (a) minimum input voltage, (b) maximum input voltage

The current of the primary winding of T_a denoted as i_{in}, and the voltage across D_a denoted as v_{Da} are shown in Fig. 2.16. The current behaves like the input current of a DCM buck-boost PFC circuit, and D_a switches as expected according to the converter operating principles. However, the leakage inductance of T_a, delays the falling time

of i_{in} slightly in each switching period as shown in Fig. 2.16(a). In addition, the resonance between this inductance and the parasitic capacitance of D_a appears on i_{in} as shown in Fig. 2.16(b). These two factors result in imperfect PF and THD different from (2.21).



(a)



(b)

Figure 2.16: (a) Current of the primary winding of T_a, and (b) interaction between D_a and T_a during switching periods

Using a Tektronix power analyzer model PA4000, input current harmonics of the prototype have been measured, and compared with IEC61000-3-2 class C requirements as shown in Fig. 2.17. The experimental setup can pass the required standards. Nevertheless, designing a transformer with a lower leakage inductance, and a snubber circuit for D_a will help in further decreasing the harmonics.

2.5 Summary

This chapter gives an insight into the importance of PFC circuits for LED drivers to comply with required PF and THD standards. Subsequently, the novelty and advantages of the proposed PFC topology which is a DCM buck-boost typed circuit over other integrated buck-boost half-bridge LED drivers are explained. The key waveforms and operating principles of the converter are discussed, and the theoretical PF and THD are also calculated. At the end, simulation and experimental results at different operating points are presented to verify the feasibility of the proposed PFC circuit. Furthermore, by using a power analyzer, the PF and THD of the experimental prototype are measured, and the compliance with regulatory standards is verified.

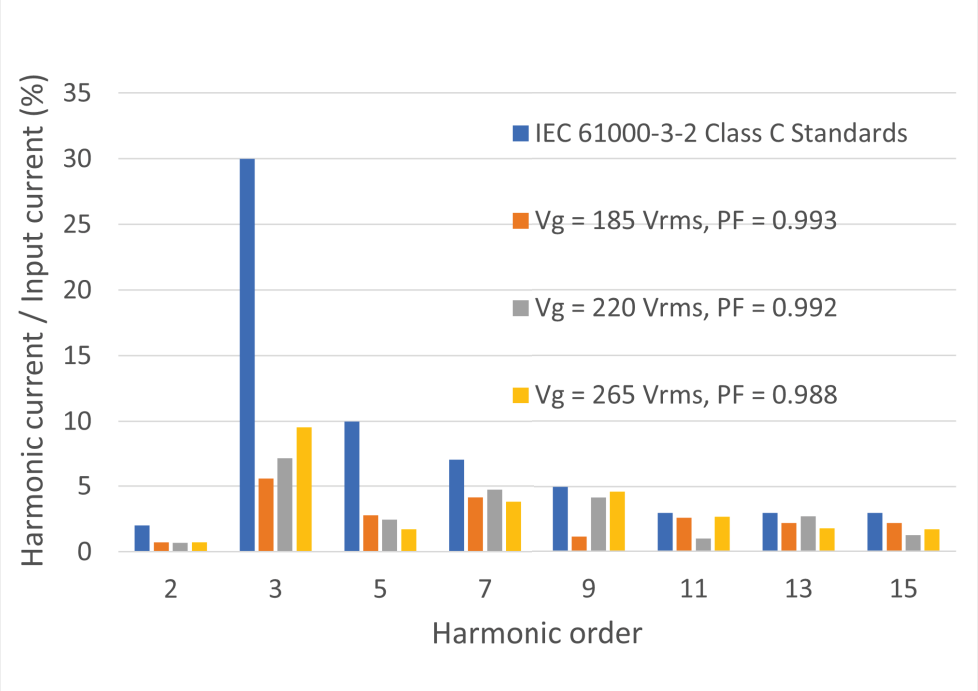


Figure 2.17: Measured input current harmonics of the experimental prototype at rated power at three different input (grid) voltage

Chapter 3

LLC Resonant Converter and Control System

Resonant converters in power electronics have gained more popularity in recent years owing to their higher efficiency and power density. The LLC resonant converter presents many extra benefits over other types of resonant converters, such as the ability to operate in near no-load condition with a reasonable switching frequency, and the ability to regulate the output throughout a wide operating range with relatively a small change in switching frequency. In addition, if designed properly, LLC resonant converters can achieve ZVS for the entire operating range [67].

Consider the Fig. 3.1(a) showing a typical half-bridge LLC resonant converter. The followings can be observed:

1. The LLC switches, S_1 and S_2 are utilized to produce a unipolar square-wave voltage on the input terminal of resonant tank which is denoted as v_{tank}. A certain amount of deadtime must be considered during the commutation of switches to ensure ZVS.

2. The resonant tank consists of a series capacitor denoted as C_r, a series inductor denoted as L_r, and a transformer with magnetizing inductance of L_{mr}. The voltage across the primary winding of transformer denoted as v_{Lmr} is a bipolar square-wave voltage. The transformer provides both galvanic isolation and turns ratio which is a variable in design.

3. On the secondary side of transformer, a rectifier network is provided for delivering dc power to the load.

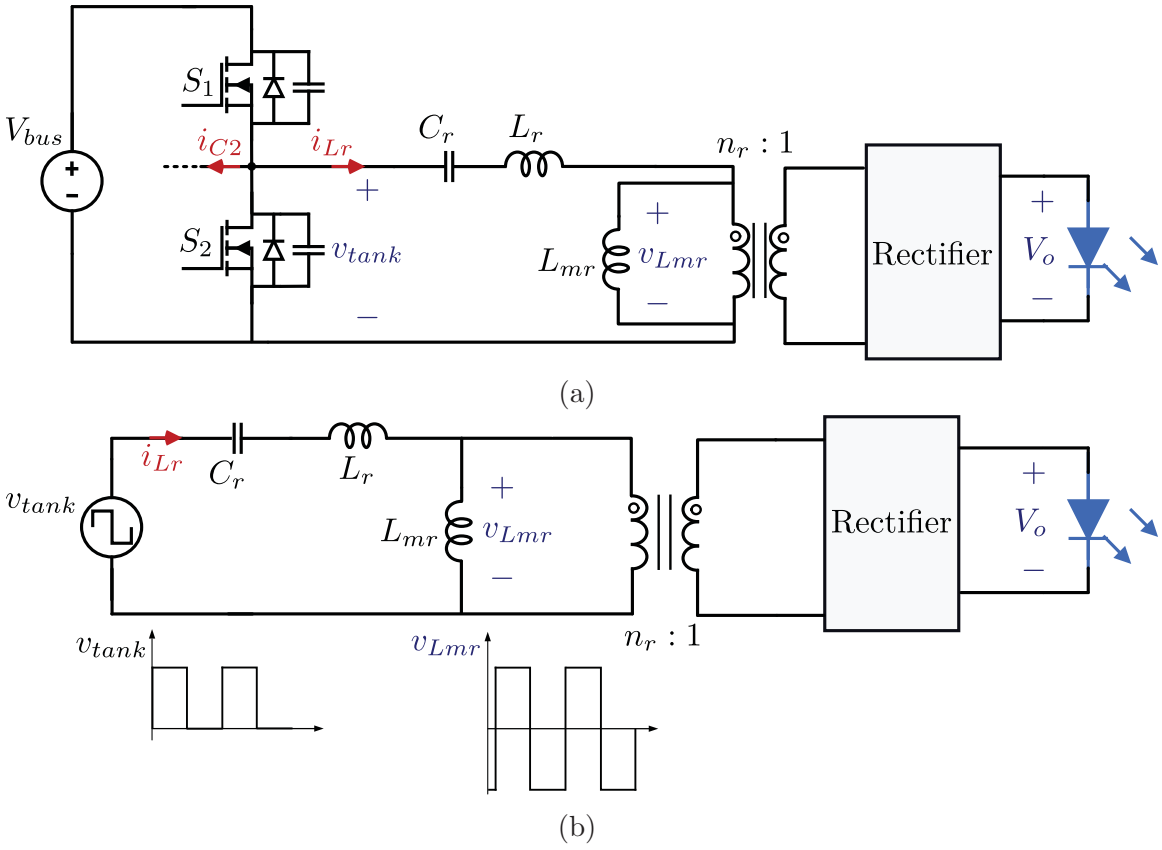


Figure 3.1: (a) Half-bridge LLC resonant converter, and (b) the simplified circuit

In this chapter, the LLC resonant converter and its advantages are briefly discussed, and the design parameters of the utilized half-bridge LLC resonant circuit are obtained. One of the advantages of the proposed LED driver is the limited dc bus voltage which is formulated in this chapter as a function of converter parameters. In addition, the proposed control system is discussed which effectively mitigates the output current ripples. At the end, simulation and experimental results are provided to verify the ZVS of LLC switches, limited range of dc bus voltage, and effectiveness of the proposed control system.

3.1 LLC Overview

The simplified circuit of a half-bridge LLC resonant converter is shown in Fig. 3.1(b) where the input voltage of LLC resonant tank denoted as v_{tank} is a square-wave signal. The impedance of LLC resonant tank consisting of C_r, L_r, and L_{mr} varies by changing the switching frequency, and this adjusts the amount of current/power delivered to the load. The fact that the amount of delivered power is controlled by changing the switching frequency makes that a viable option for control system.

The peak resonance frequency of a resonant converter denoted as f_{rp} is defined as the switching frequency that minimizes the resonant tank impedance, or in other words maximizes the amount of power delivered to the load [67]. For a series-resonant converter which is an LLC circuit without the parallel inductance L_{mr}, peak resonance frequency is the same as resonance frequency (f_r), and is independent of load as described below:

$$f_{rp} = f_r = \frac{1}{2\pi\sqrt{C_r L_r}}. \tag{3.1}$$

However, in an LLC resonant converter, and because of L_{mr}, f_{rp} becomes a function of load as follows:

$$f_p = \frac{1}{2\pi\sqrt{C_r(L_r + L_m)}} < f_{rp} < f_r = \frac{1}{2\pi\sqrt{C_r L_r}}, \tag{3.2}$$

where f_p is defined as pole frequency [67].

At no load condition, f_{rp} is the same as f_p, and by increasing the load, it becomes larger moving towards f_r, and finally at short-circuit condition where the LLC resonant converter is like a series-resonant converter, f_{rp} becomes nearly equal to f_r. These three frequencies have been shown on Fig. 3.2.

3.1.1 Voltage Gain of Resonant Tank

The voltage gain of resonant tank is defined as:

$$M_g = \frac{V_{Lmr}}{V_{tank}}, \tag{3.3}$$

where V_{Lmr} is the RMS of v_{Lmr}, and V_{tank} is the RMS of v_{tank}.

Two important variables used in the analysis of LLC resonant converters are normalized switching frequency denoted as F, and quality factor denoted as Q that are defined as follows:

$$F = \frac{f_{sw}}{f_r}, \tag{3.4}$$

and

$$Q = \frac{\omega_r L_r}{R_{eq}^2} = \frac{2\pi f_r L_r}{(\frac{V_o^2}{P_{out}})(\frac{8n_r^2}{\pi^2})} = (\frac{\pi^2}{8n_r^2})(\frac{P_{out}}{V_o^2})\sqrt{\frac{L_r}{C_r}}. \tag{3.5}$$

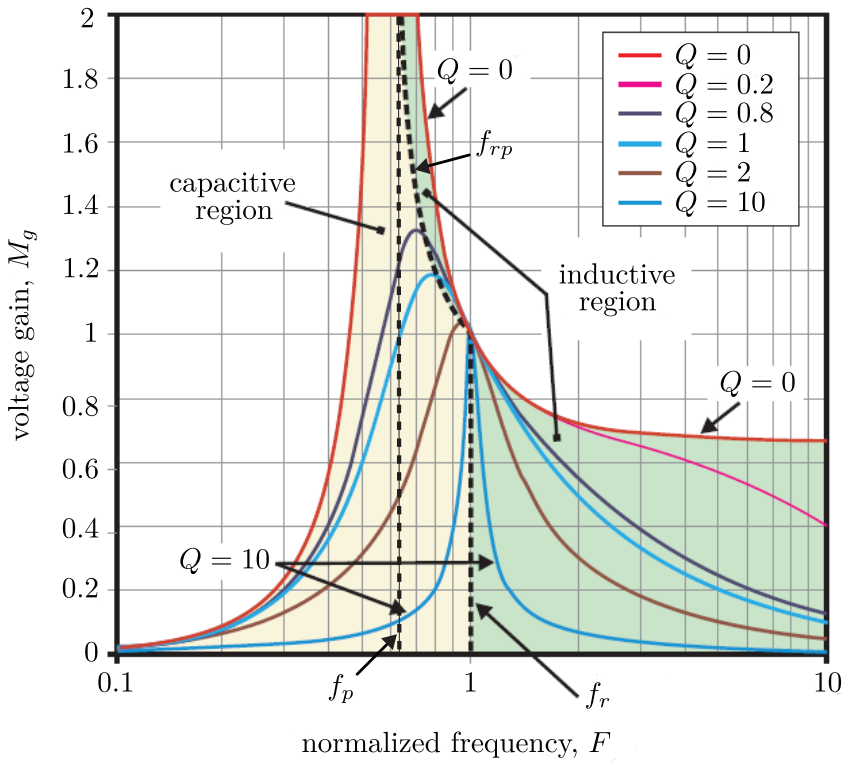


Figure 3.2: The curves of LLC resonant converter depending on different quality factors; Picture courtesy of [67]

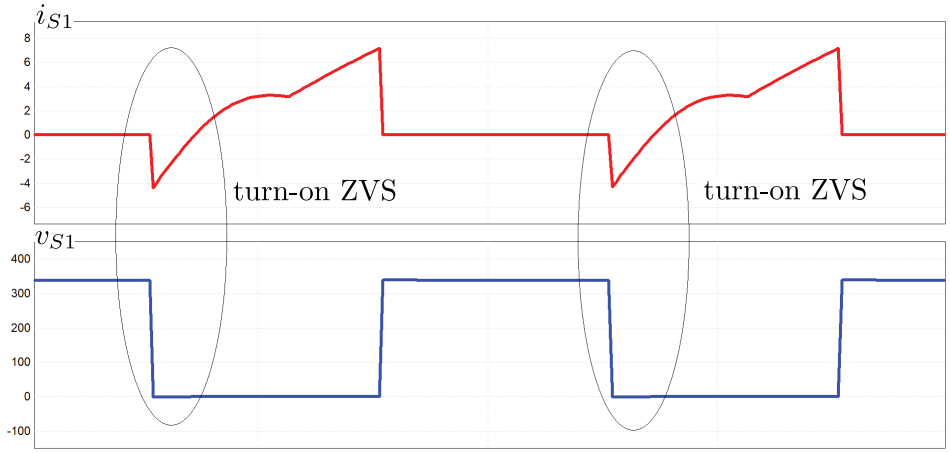
There is a family of curves as shown in Fig. 3.2 associated with an LLC resonant converter depending on different loads or equivalently different quality factors according to (3.5). In addition, the voltage gain of resonant tank defined in (3.3) varies by changing the switching frequency for every specific load.

3.1.2 Zero Voltage Switching

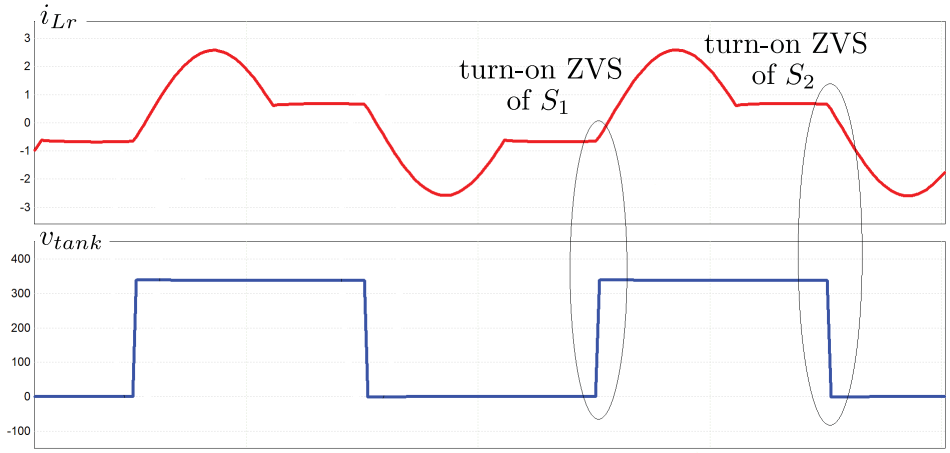
One benefit of the LLC resonant converter is the ability to achieve ZVS provided that it is designed to operate in the inductive region shown in Fig. 3.2. By achieving ZVS, the turn-on switching loss of MOSFETs becomes close to zero.

ZVS is achieved when the MOSFET turns ON after its drain-source voltage is clamped to zero. In the LLC resonant converter when ZVS is achieved, at the turn-on, before the gate-source voltage is applied, the LLC circuit forces the reversal of current to flow through the MOSFET's body diode as illustrated in Fig. 3.3(a).

When the LLC resonant converter is designed to operate in inductive region, the resonant current denoted as i_{Lr} lags v_{tank}. In other words, i_{Lr} will have a negative (positive) value on the rising (falling) edge of v_{tank} that ensures turn-on ZVS for $S_1(S_2)$ as illustrated in Fig. 3.3(b). It is worth mentioning that turn-off ZVS is achieved by adding large enough parallel capacitors on switches.



(a)



(b)

Figure 3.3: ZVS shown in (a) S_1, and (b) LLC resonant tank

3.2 Design of the LLC resonant circuit

The half-bridge LLC resonant circuit of the proposed LED driver is shown in Fig. 3.4 which is designed for dc bus voltage range of $(265 - 425)$ V, output voltage of 50 V, and output power range of $(20 - 200)$ W. The other constraint is that ZVS must be obtained for both S_1 and S_2. Because achieving ZVS is mandatory, the LLC resonant circuit must operate in inductive region throughout the whole operating range.

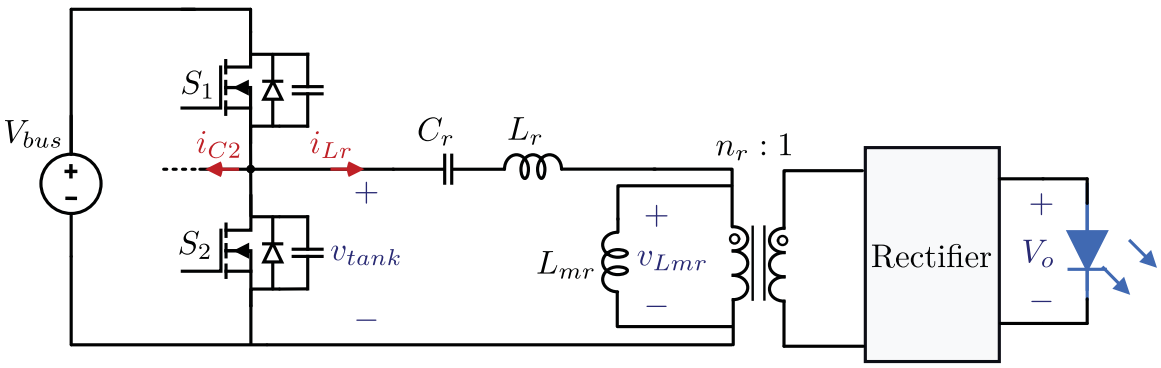


Figure 3.4: Half-bridge LLC resonant section of the proposed LED driver

According to Fig. 3.2, when the LLC resonant circuit operates in inductive region, the voltage gain of resonant tank decreases by increasing the switching frequency for a given Q. In addition, for a given dc bus voltage, and since the output voltage is constant, Q and accordingly the output power decreases by increasing the switching frequency. As a result, not only the resonance frequency but also the range of switching frequency are design variables. The other design variables are the transformer turns ratio denoted as n_r, and resonant tank variables including C_r, L_r, and L_{mr}. It is worth mentioning that i_{C2} helps in achieving ZVS, therefore, designing the LLC variables is easier compared with a regular LLC resonant circuit. The value of i_{C2} at the turn-on of S_1 and S_2 is respectively obtained in (5.23) and (5.24).

The resonance frequency is set to:

$$f_r = 132 \text{ kHz}. \tag{3.6}$$

The dc voltage gain of resonant tank is defined as [67]:

$$M_{g,DC} = \frac{V_{Lmr}^{+}}{\frac{V_{bus}}{2}} = \frac{n_r V_o}{\frac{V_{bus}}{2}} = \frac{2n_r V_o}{V_{bus}}, \tag{3.7}$$

where V_{Lmr}^{+} is the positive value of v_{Lmr} in half a switching period.

The dc voltage gain of resonant tank at resonance frequency is equal to 1. In addition, the LLC converter is designed to operate at resonance frequency when the dc bus voltage is around 380 V to make sure the highest efficiency is achieved near the nominal input (grid) voltage. The turns ratio of LLC transformer is obtained as follows:

$$\frac{2n_r V_o}{380} = 1 \implies \frac{1}{n_r} \approx 0.26. \tag{3.8}$$

The LLC transformer turns ratio is selected as $n_r = \frac{N_{r1}}{N_{r2}} = \frac{27}{7}$.

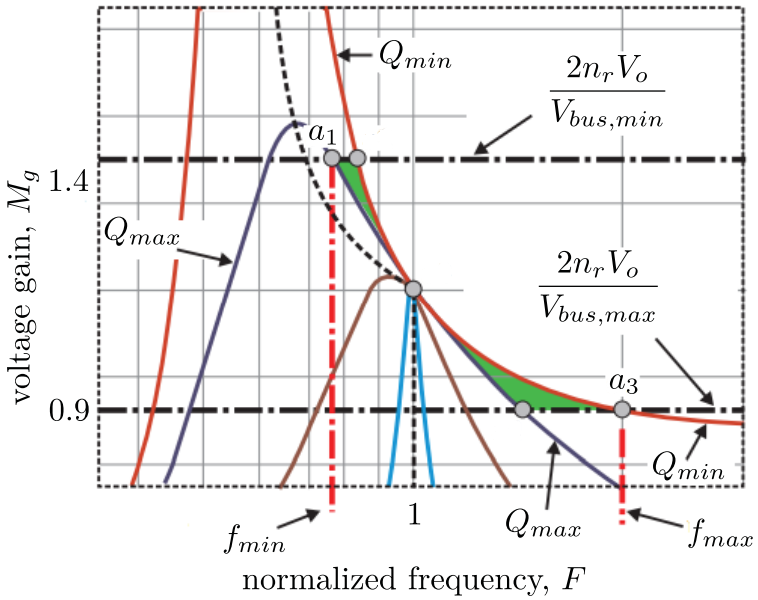


Figure 3.5: LLC curves; Picture courtesy of [67]

The magnetizing to series inductance ratio of resonant tank is selected as:

$$L_{llc} = \frac{L_{mr}}{L_r} = 7.5, \tag{3.9}$$

to minimize circulating currents, and facilitate the integration of LLC transformer and inductor.

The LLC curves are shown in Fig. 3.5. a_1 and a_3 are two critical points of the design. First, the minimum switching frequency happens at minimum dc bus voltage equal to 265 V, and maximum output power which is 200 W (point a_1). Second, the maximum switching frequency happens at maximum dc bus voltage equal to 425 V, and minimum output power which is 20 W (point a_3).

The optimal point for a_1 is near and at the right side of the curve to minimize conduction losses. For this purpose, $Q_{max} = 0.44$ is selected resulting in $f_{min} =$ 80 kHz. In addition, according to (3.5), (3.6) and (3.8), C_r and L_r will be determined, and consequently according to (3.9), L_{mr} will be also obtained. The resonant tank variables are designed as follows:

$$\begin{cases} C_r = 18.1 \text{ nF} \\ L_r = 80 \ \mu\text{H} \\ L_{mr} = 600 \ \mu\text{H}. \end{cases} \tag{3.10}$$

Then $Q_{min} = 0.044$ is obtained resulting in $f_{max} = 150$ kHz. Thus, the range of switching frequency is set as:

$$80 \text{ kHz} \leq f_{sw} \leq 150 \text{ kHz}. \tag{3.11}$$

3.3 Limited DC Bus Voltage

The output voltage is constant because the LEDs are assumed to be ideal. Furthermore, the output current is assumed to be dc based on the proper control system. As a result, the input power absorbed by the LLC and sent to the output will be dc, and consequently the double frequency oscillations can be ignored.

The voltage range of V_{bus} is important since it determines the voltage stress of S_1 and S_2. Given the peak value of input sinusoidal voltage that can be as high as 375 V, it is critical that V_{bus} have a reasonable range to lower the voltage stress of components. To determine V_{bus} in terms of the converter parameters, the voltage gain of half-bridge LLC resonant converter is obtained based on the Fourier series of v_{Lmr} and v_{tank}, and is used to relate P_{out} to V_{bus} as follows:

$$\frac{V_o}{V_{bus}} = \frac{4n_r F}{\pi^2 Q} \sum_{k=odd} \frac{\sin k\theta_s}{k((kF)^2 - 1)}, \tag{3.12}$$

where θ_s is the lag angle between v_{tank} and v_{Lmr}. In addition according to (3.4),(3.6), and (3.11), the range of F_2 is obtained as:

$$0.36 < F^2 < 1.3. \tag{3.13}$$

The series in (3.12) can be expanded as follows:

$$\sum_{k=odd} \frac{\sin k\theta_s}{k(k^2F^2 - 1)} = \frac{\sin \theta_s}{F^2 - 1} + \frac{\sin 3\theta_s}{3(9F^2 - 1)} + \frac{\sin 5\theta_s}{5(25F^2 - 1)} + \dots . \tag{3.14}$$

According to (3.13),

$$\begin{aligned}
|\frac{\sin 3\theta_s}{3(9F^2 - 1)}| &< \frac{1}{4}|\frac{\sin \theta_s}{F^2 - 1}|, \\
|\frac{\sin 5\theta_s}{5(25F^2 - 1)}| &< \frac{1}{18}|\frac{\sin \theta_s}{F^2 - 1}|, \\
&\vdots \\
|\frac{\sin k\theta_s}{k((kF)^2 - 1)}| &<< |\frac{\sin \theta_s}{F^2 - 1}| \quad for \quad k > 5 .
\end{aligned} \tag{3.15}$$

Considering (3.15), and to simplify the formula of V_{bus}, only the first term of (3.14) is considered, and (3.12) can be rewritten as:

$$\frac{V_o}{V_{bus}} = (\frac{4n_rF}{\pi^2Q})(\frac{\sin\theta_s}{F^2-1}), \tag{3.16}$$

where $\sin\theta_s$ depends on the variables of LLC resonant converter, and since i_{Lr} is in phase with v_{Lmr}, and according to (5.47) is obtained by solving the following equation:

$$i_{Lr}(t=\theta_s) = 0 \implies$$
$$(\frac{8n_r^2F}{\pi^2Q})(\sum_{k=odd}\frac{\sin k\theta_s}{k(k^2F^2-1)})(\sum_{k=odd}\frac{(1+L_{llc})k^2F^2-1}{L_{llc}k^2F^2(k^2F^2-1)}) - \sum_{k=odd}\frac{\cos k\theta_s}{k^2F^2-1} = 0. \tag{3.17}$$

For simplicity, only the first terms of Fourier series of (3.17) are considered, and (3.17) can be rewritten as:

$$(\frac{8n_r^2F}{\pi^2Q})(\frac{\sin\theta_s}{F^2-1})(\frac{(1+L_{llc})F^2-1}{L_{llc}F^2(F^2-1)}) = \frac{\cos\theta_s}{F^2-1}. \tag{3.18}$$

By using (3.18), it can be written that:

$$\tan\theta_s = \frac{1}{A_1B_1}, \tag{3.19}$$

where

$$\begin{cases} A_1 = \dfrac{8n_r^2F}{\pi^2Q} \\ \\ B_1 = \dfrac{(1+L_{llc})F^2-1}{L_{llc}F^2(F^2-1)}. \end{cases} \tag{3.20}$$

Finally, $\sin\theta_s$ is obtained in terms of A_1 and B_1 as:

$$\sin\theta_s = \frac{1}{\sqrt{1+(A_1B_1)^2}} \approx \frac{1}{A_1B_1}. \tag{3.21}$$

By replacing (3.21) into (3.16), and according to (3.20), V_{bus} is obtained as follows:

$$V_{bus} = \frac{2n_rV_o}{L_{llc}}(1+L_{llc}-\frac{1}{F^2}), \tag{3.22}$$

where

$$\begin{cases} F = \dfrac{f_{sw}}{f_r} \\ f_r = \dfrac{1}{2\pi\sqrt{L_rC_r}} \end{cases} \implies F^2 = 4\pi^2L_rC_rf_{sw}^2. \tag{3.23}$$

Assuming a lossless converter, and according to the input power formula obtained in (5.5), it can be written that:

$$f_{sw} = \frac{V_m^2}{16 P_{out} L_a} \implies F^2 = (\frac{\pi V_m^2}{8 P_{out} L_a})^2 L_r C_r. \tag{3.24}$$

Then, (3.22) is related to the peak value of input sinsusoidal voltage (V_m) and output power as follows:

$$V_{bus} = \frac{2 n_r V_o}{L_{llc}} (1 + L_{llc} - \frac{1}{(\frac{\pi V_m^2}{8 P_{out} L_a})^2 L_r C_r}). \tag{3.25}$$

By replacing the known parameters, the formula of V_{bus} is obtained as:

$$V_{bus} = 51.43\ (8.5 - \frac{P_{out}^2}{V_m^4 \times 2.566 \times 10^{-6}}). \tag{3.26}$$

The maximum of (3.26) happens at $V_m = 375$ V, and $P_{out} = 20$ W, and is equal to:

$$V_{bus,max} = 436.74 \text{ V}. \tag{3.27}$$

The variation of V_{bus} with respect to V_m and P_{out} is depicted in Fig. 3.6.

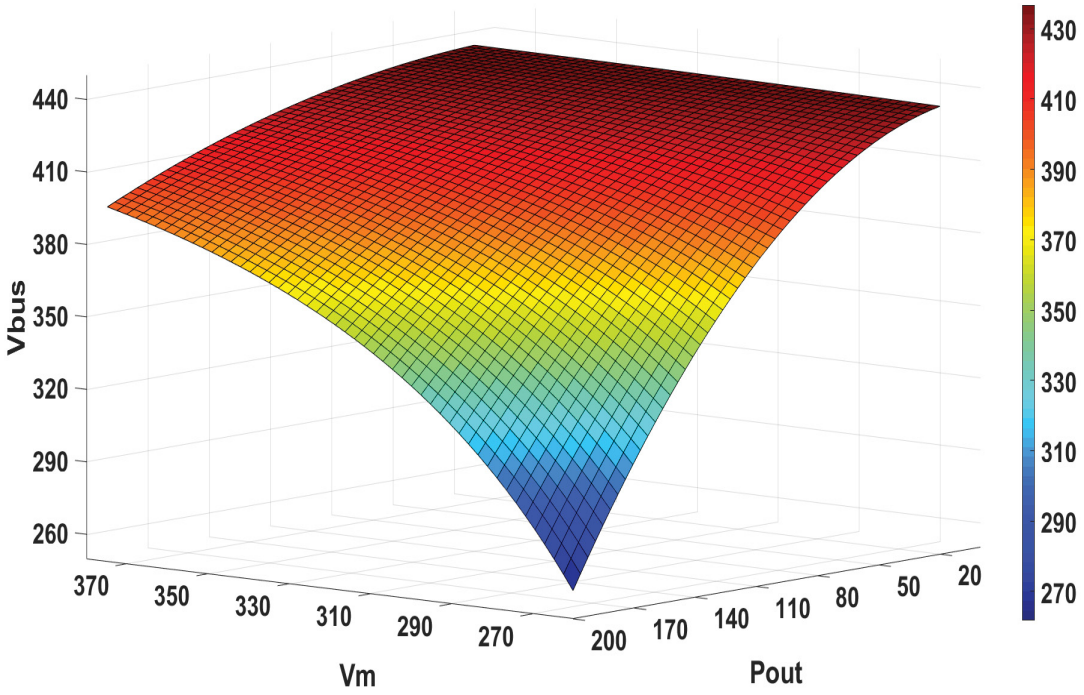


Figure 3.6: The variation of V_{bus} with respect to V_m and P_{out}

3.4 Control System

The input power of an LED driver has double-frequency oscillations, whereas the output power is ideally constant. The LED driver is responsible for decoupling these two powers. As a result of imperfect power decoupling, double-frequency ripples appear on the output causing light flickers. To comply with safety regulations, the output current ripples of the LED driver must be minimized.

As discussed in [48, 52, 53], one way to remove the output double-frequency ripples is by accepting them on the output of PFC stage and controling the LLC to produce constant dc current at the output. As a result, a low-capacitance highly durable film capacitor can be chosen as dc bus capacitor. Moreover, since the ripples are removed from the output, film capacitors can be also chosen as output capacitors.

In proposed LED driver in this thesis, similar to the proposed control system of [48] for microinverters of PV solar systems, a very fast PI controller is designed to remove the output double-frequency ripples, and place them on the dc bus capacitor. The advantage of this power decoupling method over other techniques is that it does not require any additional circuits, or complexity in control.

The control system of the proposed LED driver is depicted in Fig. 3.7.

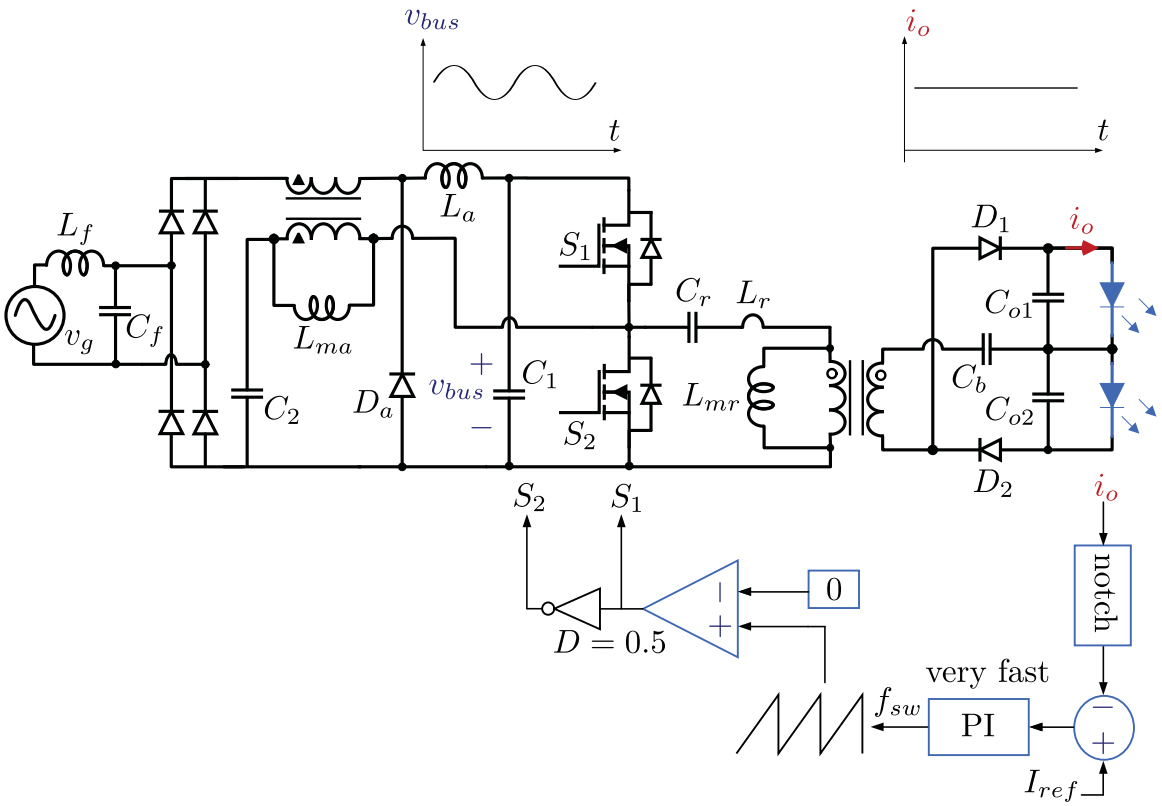
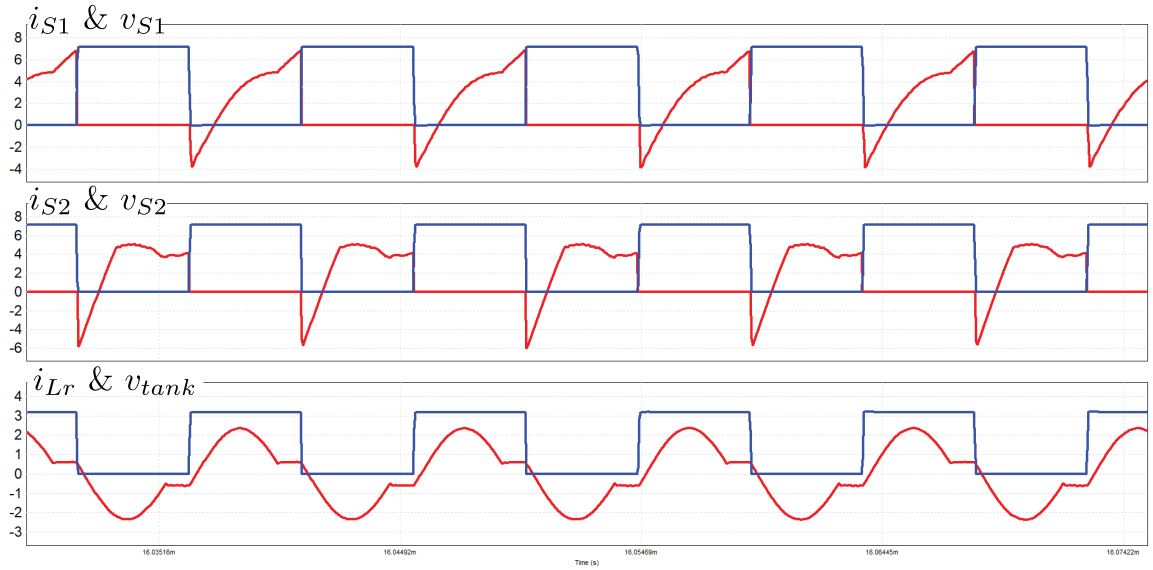


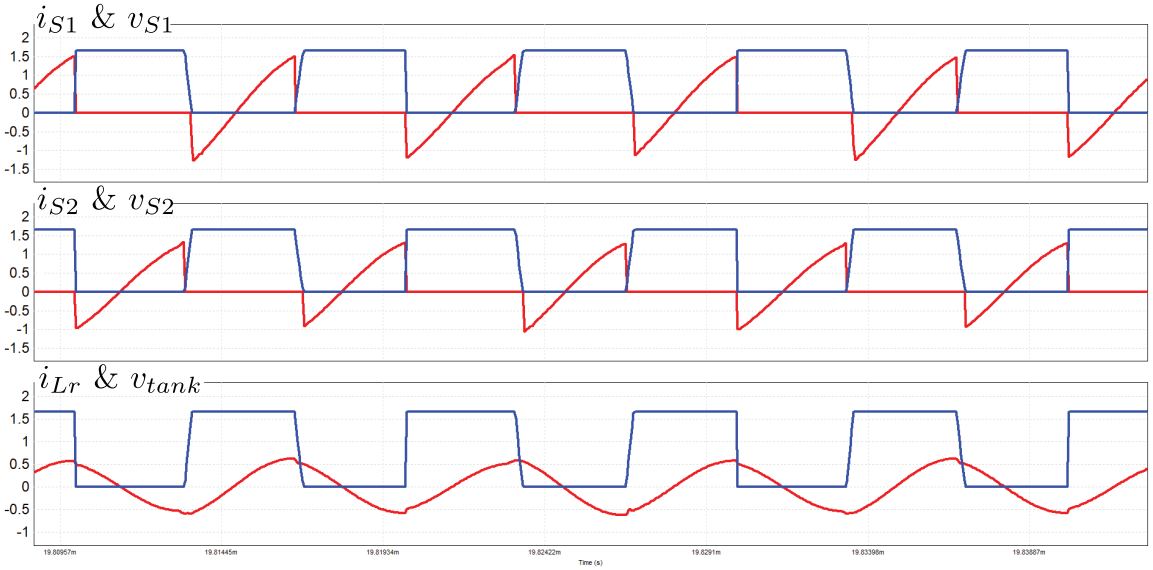
Figure 3.7: Control system of the proposed LED driver

3.5 Simulation and Experimental Results

The simulation results of the half bridge LLC resonant circuit are shown in Fig. 3.8 and Fig. 3.9 displaying the current and scaled drain-source voltage waveforms of both switches, as well as the resonant current (i_{Lr}) and v_{tank} waveforms.

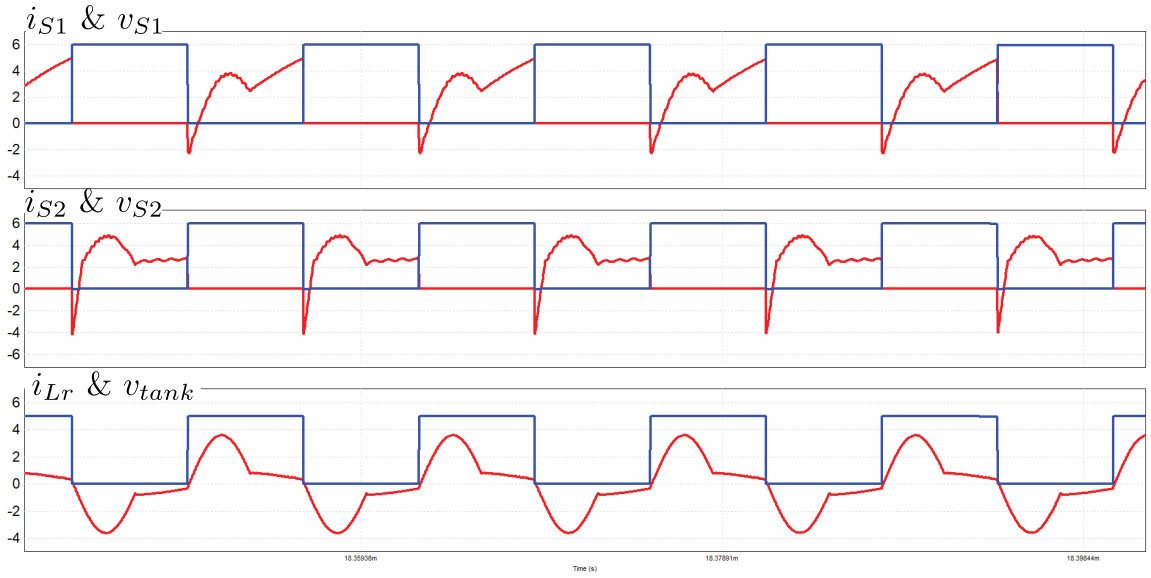


(a)

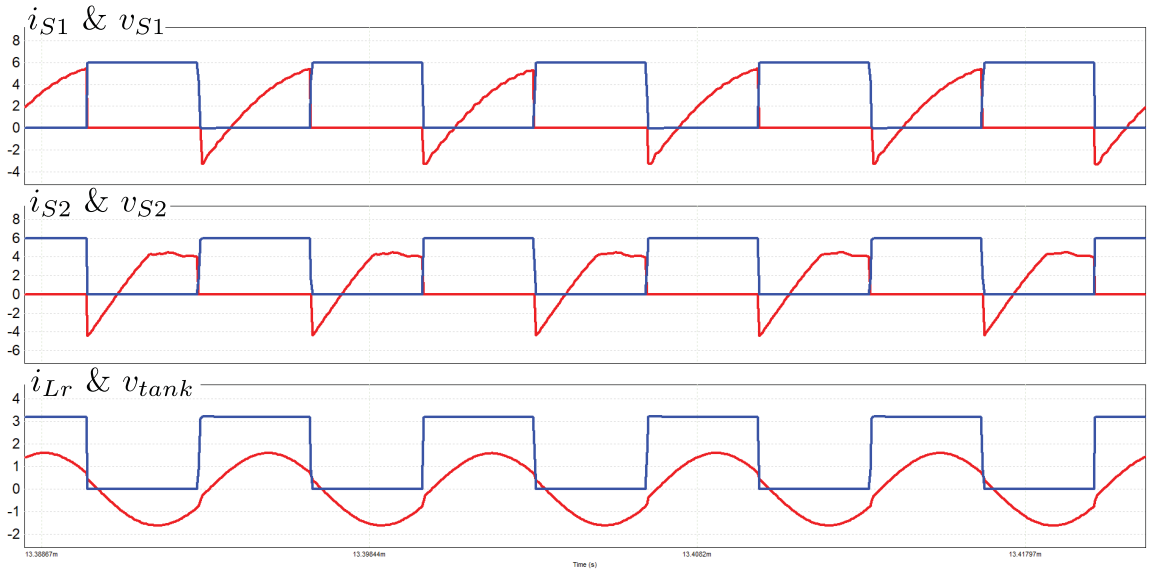


(b)

Figure 3.8: Simulation result showing ZVS at nominal input (grid) voltage at (a) full-load, (b) light-load



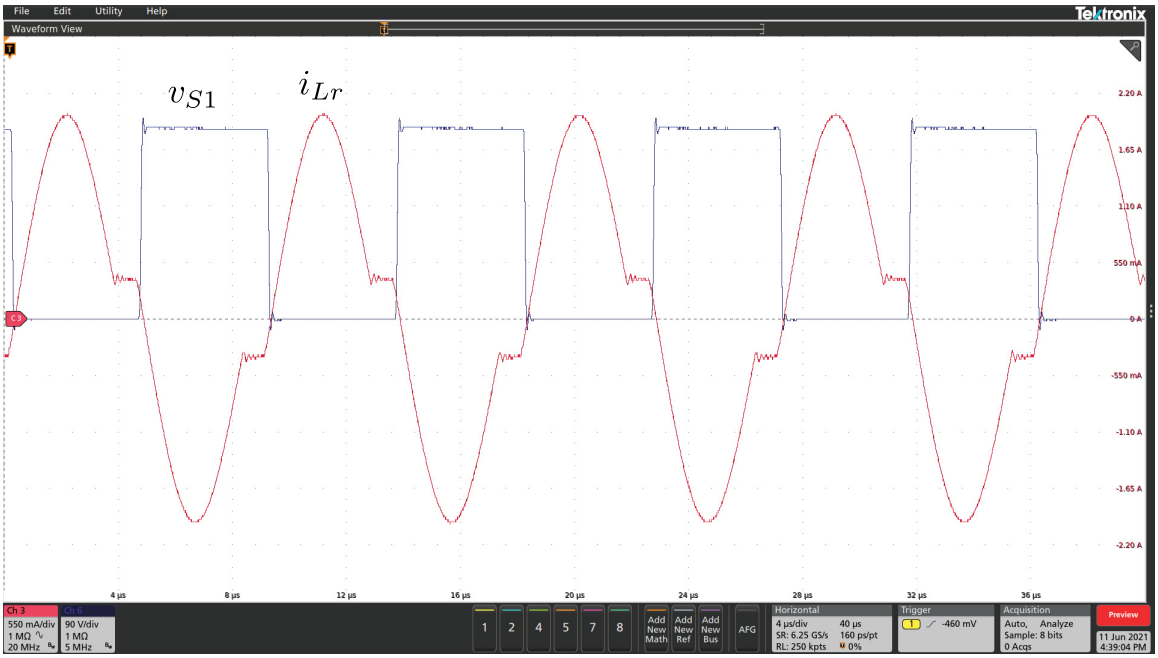
(a)



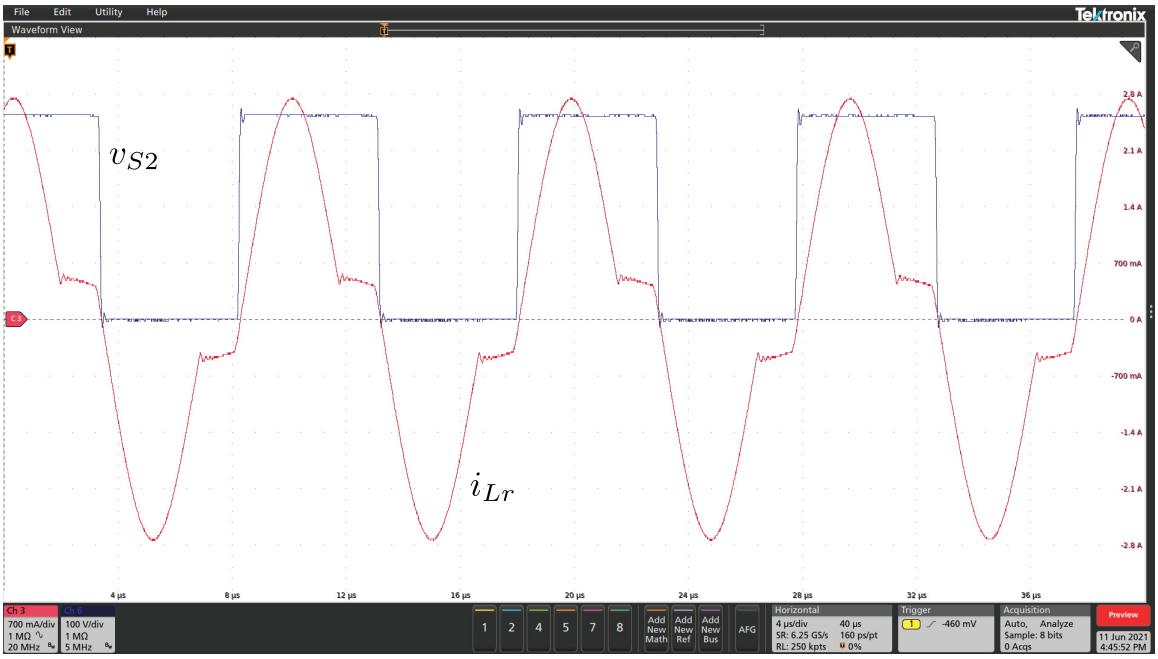
(b)

Figure 3.9: Simulation result showing ZVS at rated power at (a) minimum input (grid) voltage, (b) maximum input (grid) voltage

The experimental results are also shown in Fig. 3.10 and Fig. 3.11.

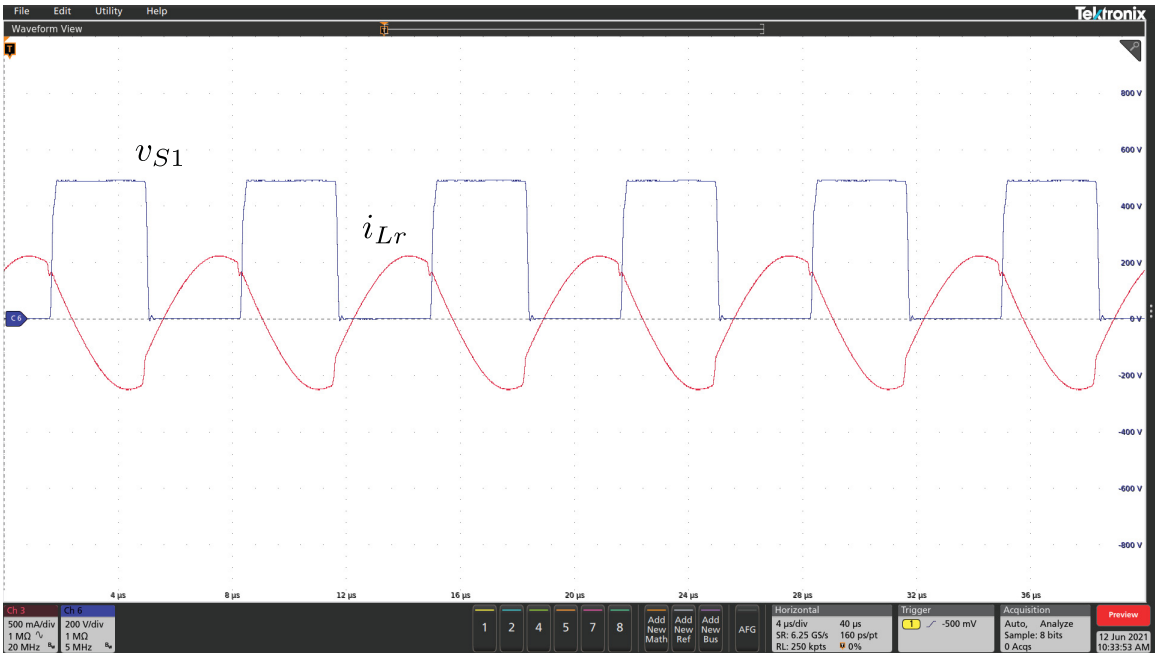


(a)

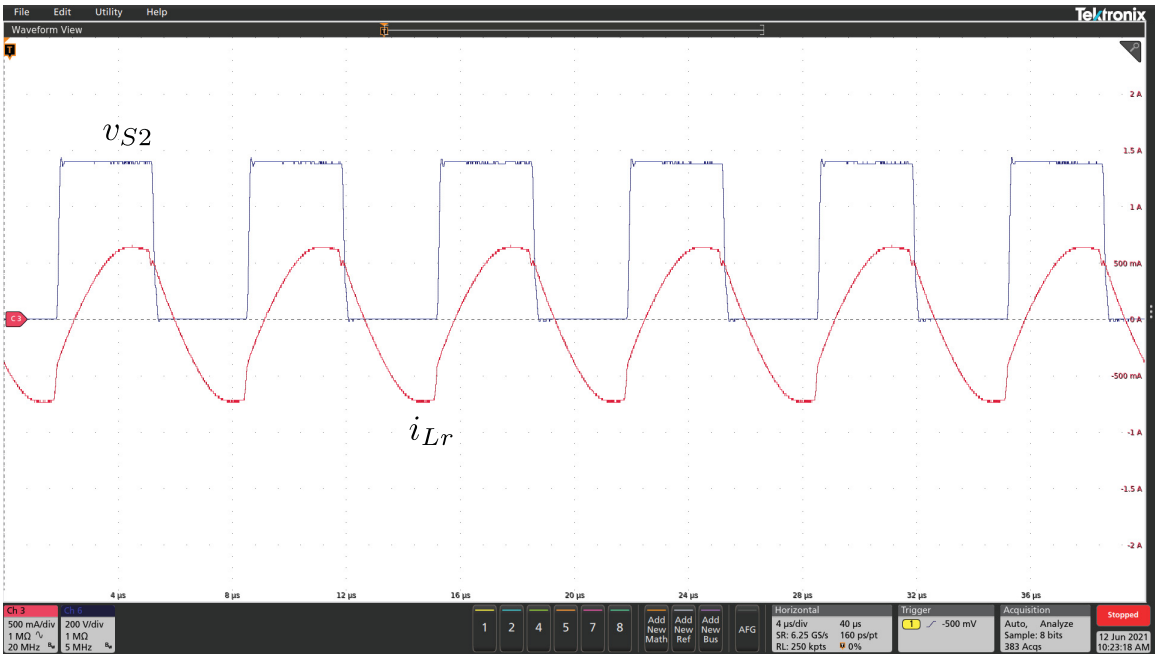


(b)

Figure 3.10: Experimental result showing ZVS at full-load for (a) S_1, and (b) S_2



(a)



(b)

Figure 3.11: Experimental result showing ZVS at light-load for (a) S_1, and (b) S_2

The current and voltage waveforms of the resonant capacitor are shown in Fig. 3.12.

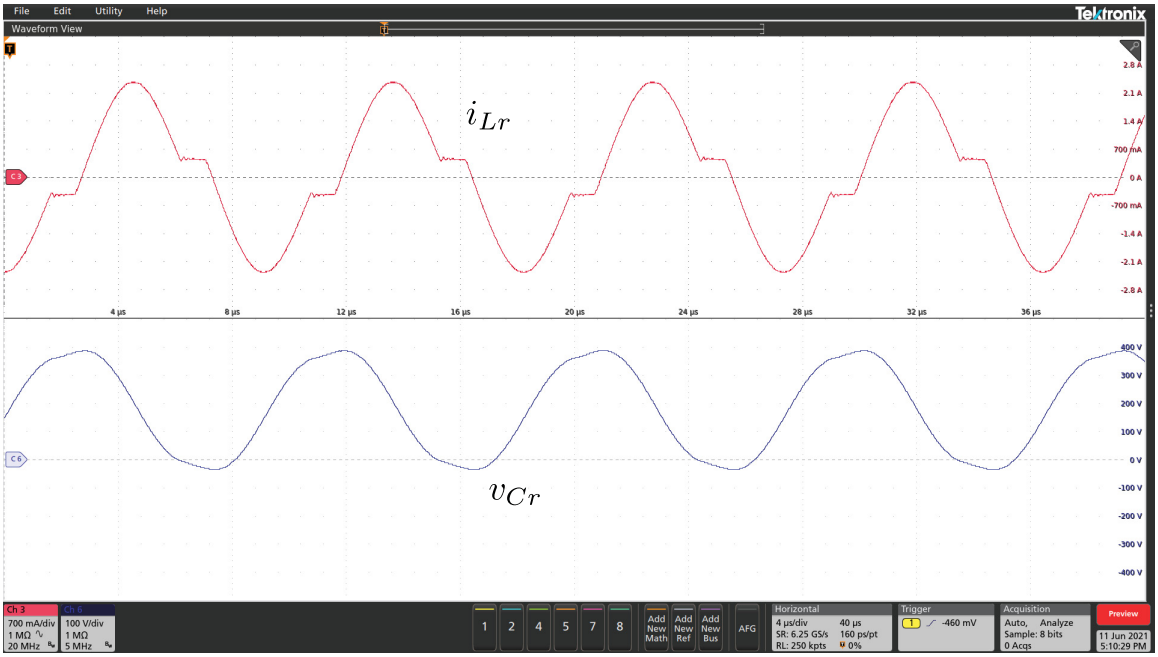


Figure 3.12: Current and voltage waveforms of C_r

The dc bus voltage waveform is shown in Fig. 3.13 which at rated power and maximum input voltage ($V_{g,rms} = 265$ V), the average is only 387.1 V. In addition, the variation of V_{bus} at rated power with respect to the rms of input voltage ($V_{g,rms}$) is depicted in Fig. 3.14.

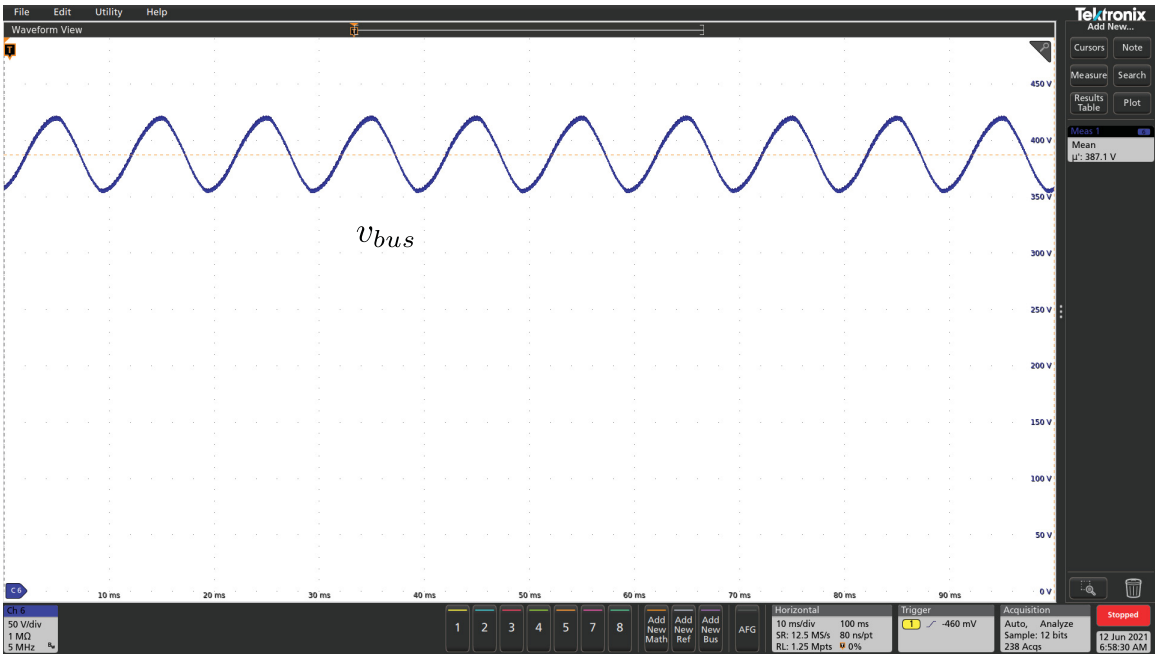


Figure 3.13: DC bus voltage at full load at maximum input voltage

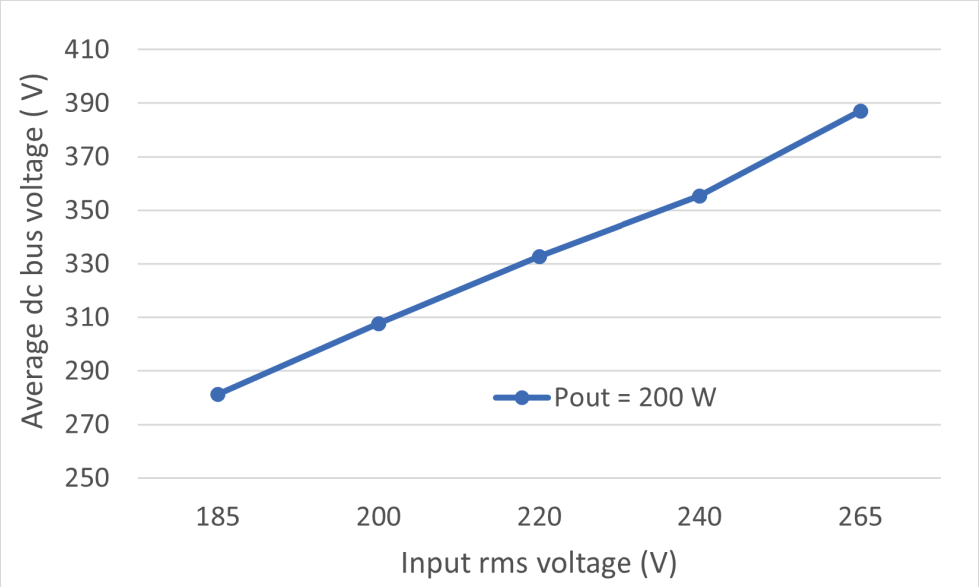


Figure 3.14: Average dc bus voltage with respect to $V_{g,rms}$ at rated power

Finally, the proposed control system is implemented using the Texas Instrument TMS320F28335 microcontroller. One of the output currents is shown in Fig. 3.15. As explained, by accepting high voltage ripples across the dc bus capacitor, the output current ripples can be reduced which for the experimental prototype could be restricted as to below 15%.

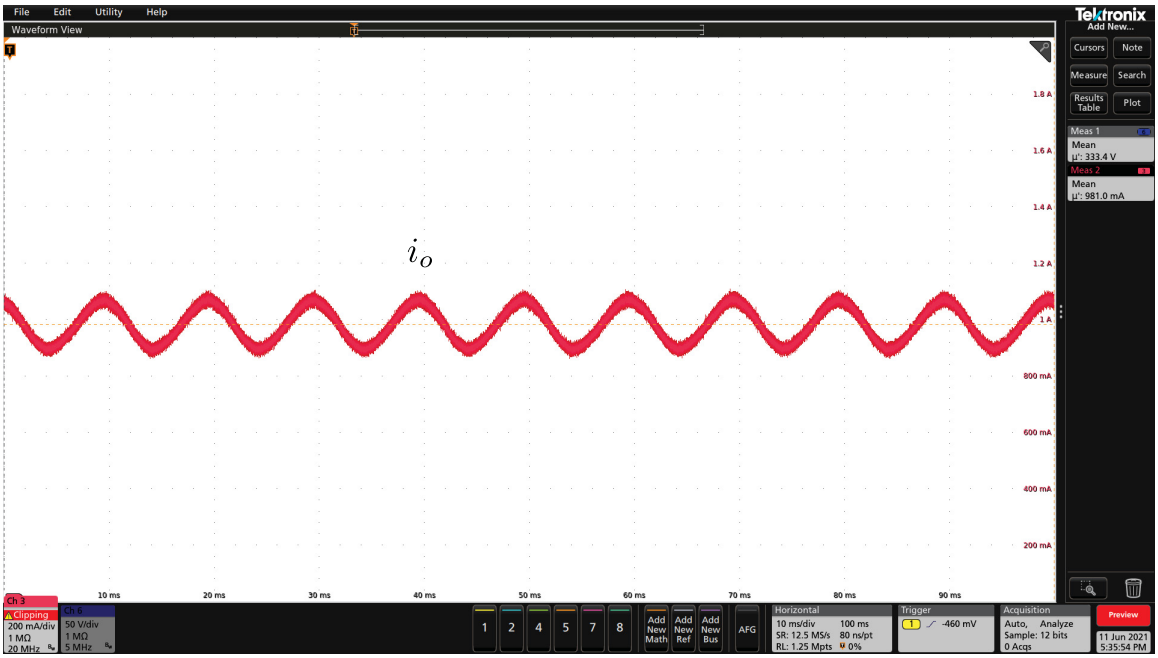


Figure 3.15: Output current at nominal input voltage ($V_{g,rms} = 220$ V) at rated power ($P_{out} = 200$ W)

3.6 Summary

This chapter starts by explaining briefly about LLC resonant converters, and their advantages over other types of resonant converters. The voltage gain function of LLC resonant tank, the LLC curves, and ZVS concept are explained, and finally the design parameters of the LLC resonant stage are obtained based on which the ZVS of both switches is guaranteed throughout the whole operating range.

In addition, the formula of average dc bus voltage is obtained in terms of the converter parameters. It is shown that V_{bus} is not higher than 436.74 V during the whole operating range. This is a great advantage of the proposed LED driver since low-voltage rating power MOSFETs can be selected.

Subsequently, the control system of the design is discussed where by designing a very fast controller, the output current ripples are minimized, and electrolytic capacitors are removed.

At the end, simulation and experimental results are provided to verify the ZVS of both switches, limited range of dc bus voltage, and effectiveness of the proposed control system which could restrict the output current ripples to below 15%.

Chapter 4

Magnetic Design

Magnetic design plays a pivotal role in power electronics due to their effect on the overall efficiency and power density of power electronic converters. There are four magnetic components in the proposed LED driver, the inductor and transformer of the PFC circuit, as well as the inductor and transformer of the LLC resonant circuit. Each inductor and transformer pair will be integrated on the same core. Therefore, there will be only two magnetic designs.

There are three general magnetic design categories as discussed in [68] as follows:

1. Saturated thermally limited design,
2. Non-saturated thermally limited design,
3. Signal quality limited design.

The choice of magnetic design is critical, and depending on the design measurements like RMS and peak value of winding currents, insulation requirements, and maximum flux density, one of the aforementioned design categories must be selected [68]. Non-saturated thermally limited design is chosen for the magnetic components of the proposed LED driver because of high frequency and large ac components of winding currents. The flowchart of non-saturated thermally limited design is depicted in Fig. 4.1.

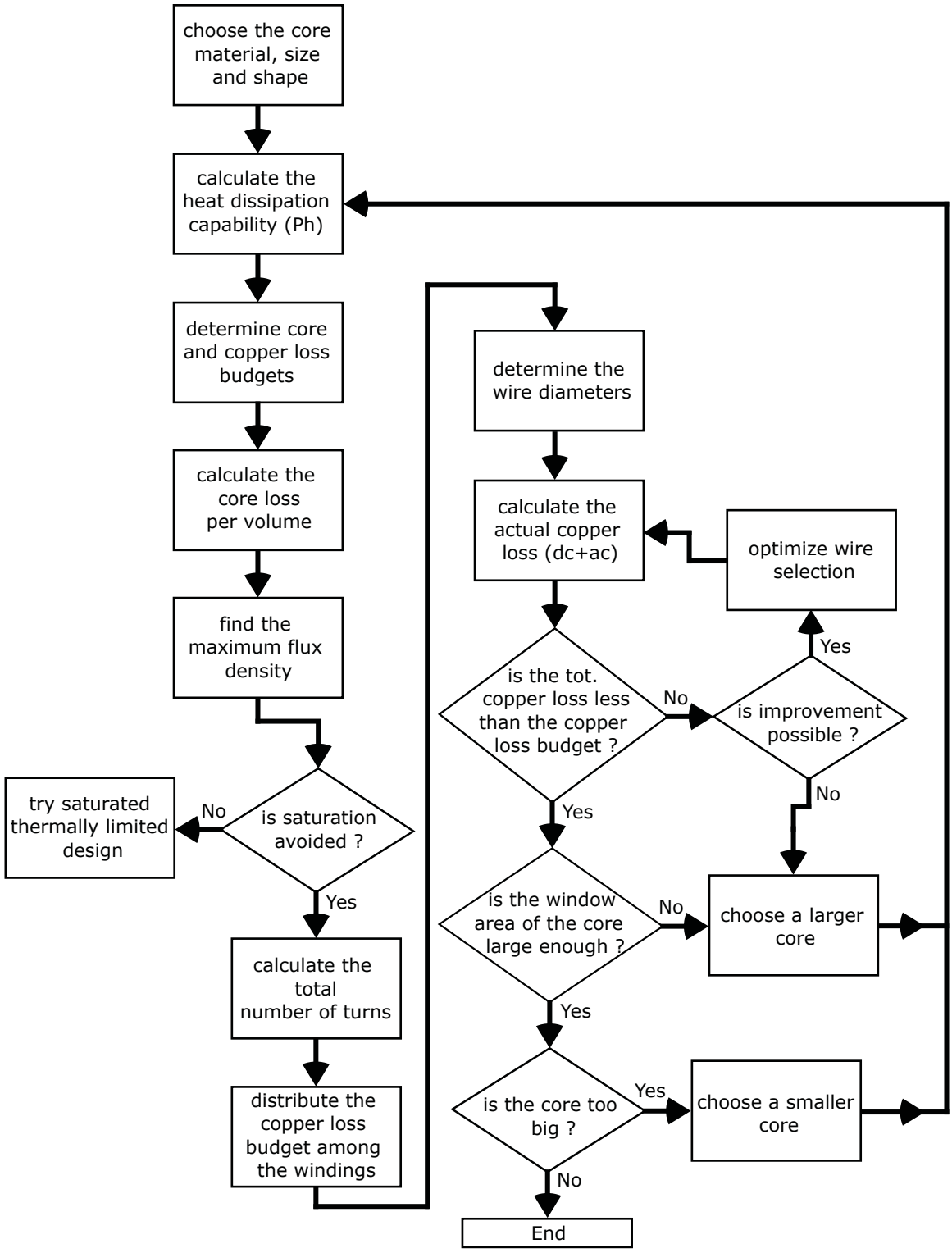


Figure 4.1: Flowchart of non-saturated thermally limited magnetic design

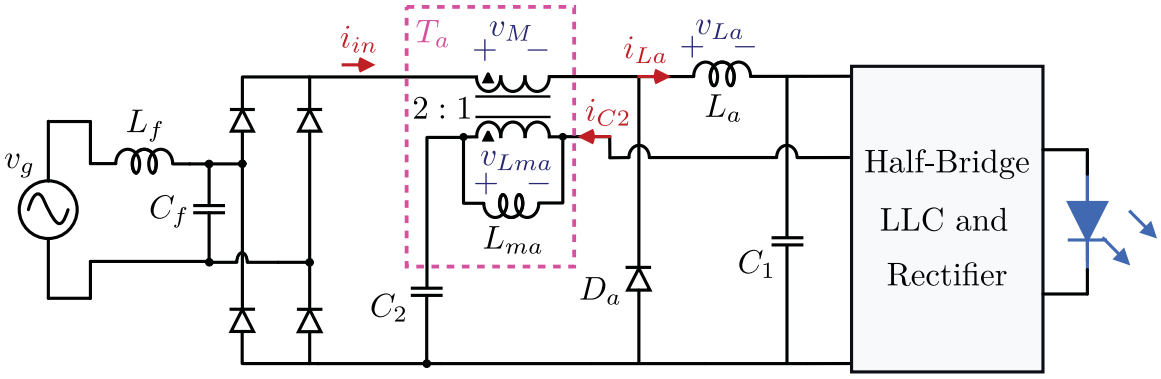


Figure 4.2: PFC section of the proposed LED driver

4.1 Magnetic Integration of T_a and L_a

The PFC section of the proposed LED driver is shown in Fig. 4.2. To achieve a higher power density and efficiency, the PFC transformer (T_a) and inductor (L_a) are integrated on the same core as shown in Fig. 4.3(a).

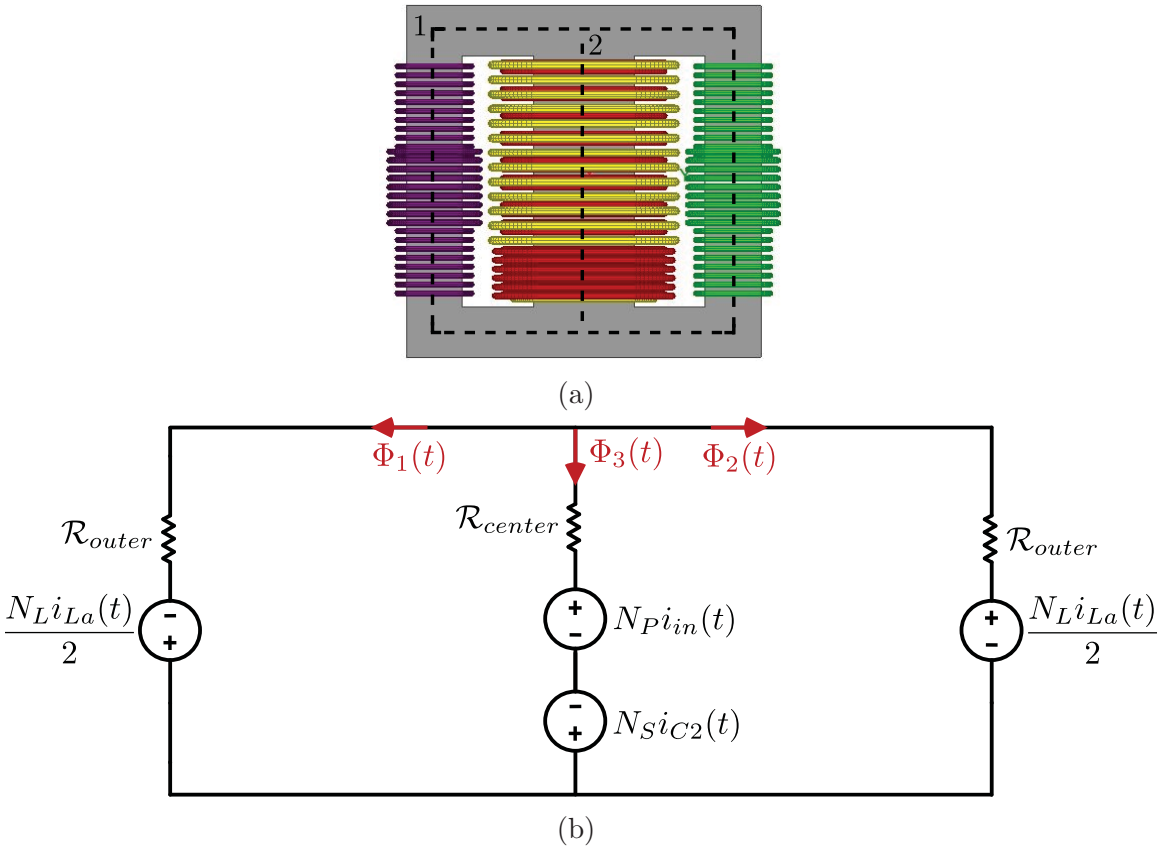


Figure 4.3: (a) The 3D model in Ansys Maxwell and (b) equivalent magnetic circuit of the magnetic integration of L_a and T_a

4.1.1 Core Material

The first step of magnetic design is to choose the core material. Material 3C94 is chosen due to its high permeability, high saturation limit, and suitability for the selected operating frequency range.

4.1.2 Core Size

The core size is determined using the following equation comparing the component total volt-amp rating with core dimensions to assess the core capacity for withstanding expected losses [68]

$$S_{tot} = \sum V_{i,rms} I_{i,rms} = A_f a_{ch}^{\lambda} \implies a_{ch} = (\frac{S_{tot}}{A_f})^{\frac{1}{\lambda}}, \tag{4.1}$$

where A_f is the ferrite coefficient in the range of $(5-25)\times 10^6$ if a_{ch} is in [m] which for high frequency designs, $A_f = (20-25)\times 10^6$ is normally selected, a_{ch} is the largest dimension of magnetic core, S_{tot} is the component volt-amp rating, and λ is an exponent characterizing the material, and shape of the core, $\lambda = 3$.

Based on the rms voltage and current of the windings at rated power, the maximum dimension of core is determined as follows:

$$\begin{cases} V_{M,rms} = 347.1 \text{ V} \\ I_{in,rms} = 1.45 \text{ A} \\ V_{Lma,rms} = 188 \text{ V} \\ I_{C2,rms} = 2.58 \text{ A} \\ V_{La,rms} = 231.28 \text{ V} \\ I_{La,rms} = 1.59 \text{ A} \end{cases} \overset{A_f = 20\times 10^6}{\Longrightarrow} \begin{cases} S_{tot} = 1356.9 \text{ V} \\ a_{ch} = 40.79 \text{ mm} . \end{cases} \tag{4.2}$$

As the largest dimension of core is calculated as $a_{ch} = 40.79$ mm, the ferrite core EE 42/20 which is made of two E 42/21/20 cores placed on each other is selected for the PFC integrated magnetic component.

4.1.3 Structure of the Magnetic Design

As illustrated in Fig. 4.3(a), the transformer windings are wrapped around the middle leg, and the inductor winding is wrapped around the outer legs of the core that will be identically designed in terms of air gap, and number of winding turns. The equivalent magnetic circuit of the proposed structure is shown in Fig. 4.3(b).

Using two KVLs, and one KCL, it can be written that:

$$\begin{cases} -\frac{N_L}{2} i_{La}(t) + \mathcal{R}_{outer}\Phi_1(t) - \mathcal{R}_{center}\Phi_3(t) - N_P i_{in}(t) + N_S i_{C2}(t) = 0 \\ N_P i_{in}(t) - N_S i_{C2}(t) + \mathcal{R}_{center}\Phi_3(t) - \mathcal{R}_{outer}\Phi_2(t) - \frac{N_L}{2} i_{La}(t) = 0 \\ \Phi_3(t) = -\Phi_1(t) - \Phi_2(t), \end{cases} \tag{4.3}$$

and consequently the magnetic fluxes shown on Fig. 4.3(b) are obtained as follows:

$$\begin{cases} \Phi_1(t) = -\frac{\Phi_3(t)}{2} + \frac{N_L i_{La}(t)}{2\mathcal{R}_{outer}} \\ \\ \Phi_2(t) = -\frac{\Phi_3(t)}{2} - \frac{N_L i_{La}(t)}{2\mathcal{R}_{outer}} \end{cases} \tag{4.4}$$

where $\Phi_3(t)$ is the flux created by T_a, and according to (4.3) and (4.4) can be calculated as:

$$\Phi_3(t) = \frac{N_S i_{C2}(t) - N_P i_{in}(t)}{\frac{\mathcal{R}_{outer}}{2} + \mathcal{R}_{center}}. \tag{4.5}$$

The results shown in (4.4) and (4.5) indicate that the flux created by L_a ($\frac{N_L i_{La}(t)}{2\mathcal{R}_{outer}}$) does not pass through the middle leg. In addition, half of the flux created by T_a ($\frac{\Phi_3(t)}{2}$) existing in each outer leg is in the opposite direction, and the voltage created by them will be cancelled with each other not affecting L_a. In conclusion, there is no interaction between L_a and T_a in this structure. Therefore, they can be independently designed.

4.1.4 Heat Dissipation Capability and Total Loss Budget

Calculating the operating temperature of a magnetic component is essential for every power electronic device as there is a heat dissipation capability for every wire, and the ferrite core that must be considered. The heat dissipation capability of a magnetic component denoted as P_h is defined as [68]:

$$P_h = k_A ab, \tag{4.6}$$

where P_h is the allowable loss budget that guarantees the temperature rise under 50°C in W, k_A is a coefficient, a typical value is 2500 $\mathrm{W\,m^{-2}}$, and a and b are the two largest dimensions of magnetic core in [m].

For the chosen EE 42 core,

$$P_h = 2500 \times 0.042 \times 0.042 = 4.41 \text{ W}. \tag{4.7}$$

4.1.5 Optimal Core/Copper Loss Ratio

The total loss of every magnetic component consists of core loss which is related to core characteristics such as dimension, material, etc., and copper loss which is the ohmic loss dissipated in windings. For every magnetic design, there is a trade-off between these two losses.
It is proven that the maximum efficiency of any magnetic design happens when the core loss and copper loss are nearly the same [69]. Therefore, to achieve the optimal design, it is assumed that

$$P_{h,fe} = P_{h,cu} = \frac{P_h}{2}, \tag{4.8}$$

where $P_{h,fe}$ is the core loss budget, and $P_{h,cu}$ is the copper loss budget of the design.

For the selected core, it can be written that:

$$P_{h,fe} = P_{h,cu} = \frac{4.41}{2} = 2.205 \text{ W}. \tag{4.9}$$

Since this magnetic component consists of an inductor and a transformer, the core and copper loss budgets must be divided between L_a and T_a.

4.1.6 Allocation of Core Loss Budget

The core loss of a certain magnetic component denoted as P_{fe} is proportional to its magnetic volume denoted as $\mathcal{V}_e$, and is determined by Stienmetz equation as:

$$P_{fe} = k_e f_{sw}^{\gamma} \hat{B}^{\beta} \mathcal{V}_e, \tag{4.10}$$

where k_e is a constant, γ and β are exponents, and $\hat{B}$ is maximum flux density.

According to (4.10), and assuming that the maximum flux density of L_a and T_a is nearly the same, the core loss budget obtained in (4.9) is divided between inductor and transformer according to their corresponding magnetic volumes.

As illustrated in Fig. 4.3(a), the flux created by L_a only passes through the outer legs (path 1) while the flux created by T_a passes through all three legs (both path 1 and path 2).

The total magnetic volume of a certain core is defined as:

$$\mathcal{V}_e = A_e \times l_e, \tag{4.11}$$

where A_e is the magnetic area of middle leg, and l_e is the total magnetic length of the core.

Both A_e and l_e can be found in the ferrite core datasheet, or by simple calculations based on different measures of the core given in the datasheet.

As for the EE 42 core [70], the magnetic volume of inductor magnetic path (path 1) and middle leg (path 2) shown in Fig. 4.3(a) are calculated respectively as follows:

$$\mathcal{V}_{e1} = 18152 \text{ mm}^3. \tag{4.12}$$

$$\mathcal{V}_{e2} = 8784 \text{ mm}^3. \tag{4.13}$$

The total magnetic volume of the EE 42 core is obtained as:

$$\mathcal{V}_e = \mathcal{V}_{e1} + \mathcal{V}_{e2} = 26936 \text{ mm}^3. \tag{4.14}$$

In this design for simplicity, the core loss budget associated with middle leg (path 2) is not involved in calculations. Then, assuming that the maximum flux density of L_a and T_a is nearly the same, the core loss budget associated with inductor magnetic path (path 1) is divided between inductor and transformer equally, and the core loss budget of each of them is determined as follows:

$$\frac{\mathcal{V}_{e1}}{\mathcal{V}_e} = 67.3\% \quad \overset{(4.10)}{\Longrightarrow} \quad P_{h,fe,L} = P_{h,fe,T} = \frac{0.673}{2} P_{h,fe} = 0.743 \text{ W}, \tag{4.15}$$

where $P_{h,fe,L}$ is the core loss budget of L_a, and $P_{h,fe,T}$ is the core loss budget of T_a.

4.1.7 Core Loss per Volume

The core loss per volume denoted as $P_{fe,sp}$ is defined as [68]:

$$P_{fe,sp} = \frac{P_{h,fe}}{1000 \times \mathcal{V}_e} \text{ [kW m}^{-3}\text{]}. \tag{4.16}$$

According to (4.12) and (4.15), the core loss per volume of L_a is obtained as:

$$P_{fe,sp,L} = \frac{0.743}{1000 \times 18152 \times 10^{-9}} = 40.93 \text{ kW m}^{-3}, \tag{4.17}$$

and according to (4.14) and (4.15), the core loss per volume of T_a is obtained as:

$$P_{fe,sp,T} = \frac{0.743}{1000 \times 26936 \times 10^{-9}} = 27.58 \text{ kW m}^{-3}. \tag{4.18}$$

4.1.8 Maximum Flux Density

In the datasheet of ferrite materials, the graphical dependency of $P_{fe,sp}$ is shown versus maximum flux density, and frequency as shown in Fig. 4.4 which is the datasheet of 3C94 material [71]. Based on this graph, for a given frequency, one can find the maximum flux density, and thus that of L_a and T_a are calculated respectively as follows:

$$\hat{B}_L = 93.12 \text{ mT}, \tag{4.19}$$

and

$$\hat{B}_T = 80.9 \text{ mT}. \tag{4.20}$$

The assumption made earlier that $\hat{B}_L$ and $\hat{B}_T$ were considered almost the same is justified.

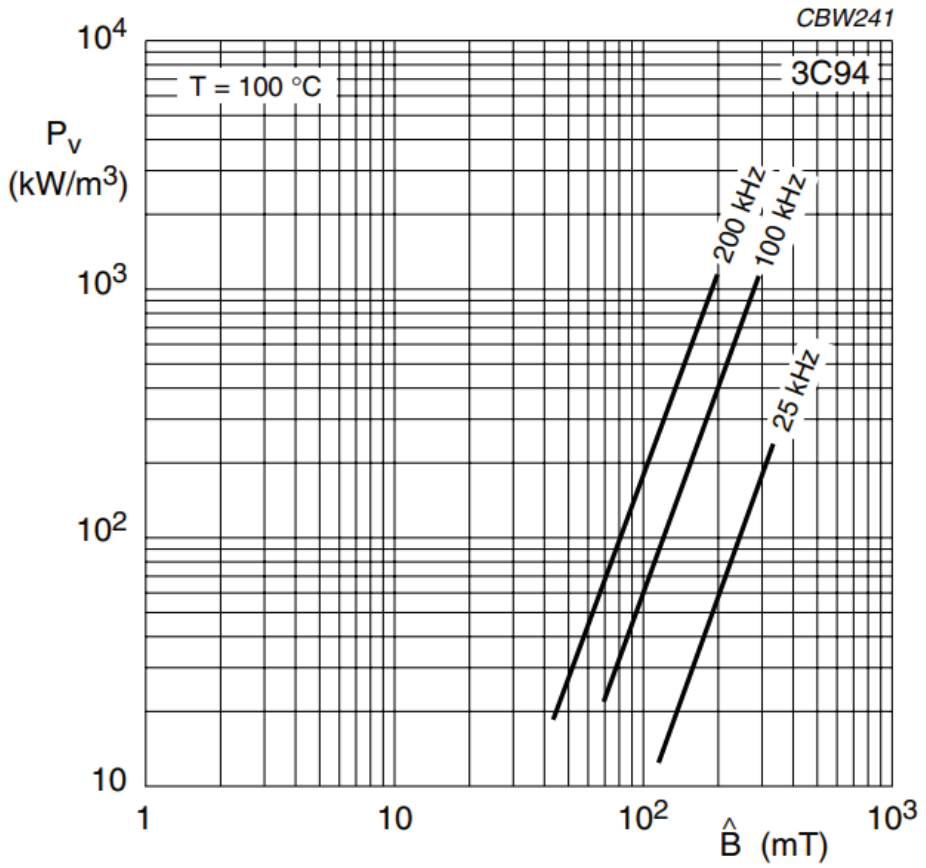


Figure 4.4: Core loss per volume versus maximum flux density and frequency [71]

4.1.9 Number of Turns

Calculating the number of turns of transformer and inductor windings is slightly different, yet both are calculated according to their maximum flux density.

4.1.9.1 Number of Turns of T_a Windings

The number of turns of the primary winding denoted as N_P is defined as [68]:

$$N_P = \frac{\Psi_{pp,T}}{\Phi_{pp,T}}, \tag{4.21}$$

where $\Psi_{pp,T}$ is the magnetic flux linkage of T_a defined as the area under the voltage waveform of the primary winding for half a switching period, and $\Phi_{pp,T}$ is the peak-to-peak magnetic flux of T_a.

The peak-to-peak magnetic flux linkage of T_a is obtained as:

$$\Psi_{pp,T} = \int_0^{\frac{T_{sw}}{2}} v_M(t)\, d\tau = v_{bus} \times \frac{T_{sw}}{2}. \tag{4.22}$$

This integrated magnetic is designed at full-load, and minimum switching frequency which results in the highest magnetic field to ensure saturation is avoided for the whole operating range.

For this operating point, the average dc bus voltage is calculated according to (3.26) as:

$$V_{bus} = 266.05 \text{ V}. \tag{4.23}$$

The approximation used in (3.21) to determine (3.26) is fairly accurate, but for the selected operating point, the actual value of V_{bus} is slightly higher. Therefore, a 10% increase is regarded for (4.23). Furthermore, considering the worst case scenario, the double-frequency voltage ripples (40% peak-to peak is allowed across C_1) are considered, and the switching interval when the peak value of v_{bus} happens is evaluated. Then, $\Psi_{pp,T}$ is calculated as:

$$\Psi_{pp,T} = 1.1 \times 1.2 \times V_{bus} \times \frac{T_{sw}}{2} = 0.002195 \text{ Wb}. \tag{4.24}$$

The peak-to-peak magnetic flux of T_a is also calculated as:

$$\Phi_{pp,T} = 2 \times \hat{B}_T \times A_e = 3.78 \times 10^{-5} \text{ Wb}. \tag{4.25}$$

Using (4.21), the number of turns of the primary winding is calculated as:

$$N_P = 58.1. \tag{4.26}$$

Since according to $V = 4N\Phi f$ equation for transformers, higher number of turns helps in avoiding saturation, the primary number of turns is rounded up to $N_P = 60$, and then the number of turns of the secondary winding is determined as:

$$N_S = \frac{N_P}{2} = 30. \tag{4.27}$$

4.1.9.2 Number of Turns of L_a Winding

The number of turns of L_a winding denoted as N_L is defined as [68]:

$$N_L = \frac{\Psi_{pp,L}}{\Phi_{pp,L}}, \tag{4.28}$$

where $\Psi_{pp,L}$ is the peak-to-peak magnetic flux linkage of L_a, and $\Phi_{pp,L}$ is the peak-to-peak magnetic flux of L_a.

The peak-to-peak magnetic flux linkage of L_a is obtained as:

$$\Psi_{pp,L} = L_a \times i_{La,pp}, \tag{4.29}$$

where $i_{La,pp}$ is the peak-to-peak current of L_a.

According to (5.6) and (5.7), for the chosen operating point, $L_a = 267\ \mu$H, and $i_{La,pp}$ is determined as:

$$i_{La,pp} = \hat{i}_{in} \overset{(2.18)}{=} \frac{V_m|\sin\omega_l t|}{2f_{sw}L_a}. \tag{4.30}$$

The switching time instant when $|\sin\omega_l t| = 1$ is considered. Then for the chosen operating point, it can be written that:

$$I_{La,max} = \frac{V_m}{2f_{sw}L_a} = 6.12\ \text{A}, \tag{4.31}$$

where $I_{La,max}$ is the maximum current of L_a and is equal to its peak-to-peak current since it operates in DCM. Then, $\Psi_{pp,L}$ is calculated as:

$$\Psi_{pp,L} = L_a \times I_{La,max} = 0.00163\ \text{Wb}. \tag{4.32}$$

Similar to transformer, $\Phi_{pp,L}$ is calculated as:

$$\Phi_{pp,L} = 2 \times \hat{B}_L \times A_{eo} = 2.33 \times 10^{-5}\ \text{Wb}, \tag{4.33}$$

where $A_{eo} \approx \frac{A_e}{2}$, and is the magnetic area of outer legs around which L_a is wrapped.

Finally, according to (4.28), the number of turns of L_a winding is calculated as:

$$N_L = 69.96. \tag{4.34}$$

For L_a, a certain amount of airgap denoted as g must be considered to avoid saturation that is obtained as:

$$g = \frac{\mu_0 A_{eo} N_L^2}{L_a} = 2.88 \text{ mm}. \tag{4.35}$$

The airgap $g_1 = g_2 = 1.4$ mm is then chosen on each outer leg.

The inductor (L_a) is composed of two identical sub-inductors on each outer leg that are in series with each other. According to the arrangement of these two sub-inductors shown in Fig. 4.3(a) in which their fluxes are in the same direction, the total inductance is calculated as:

$$L_a = L_{a1} + L_{a2} + 2M_a, \tag{4.36}$$

where L_{ai} is the self inductance of each sub-inductor, $M_a = k_{cp}\sqrt{L_{a1}L_{a2}}$, is the mutual inductance between the sub-inductors, and k_{cp} is their coupling factor.

Perfect coupling happens when all the flux passing through L_{a1} passes through L_{a2} as well resulting in $k_{cp} = 1$. However, the coupling of sub-inductors in this configuration is not perfect. According to (4.36), constructing the inductor with $N_L = 70$ obtained in (4.34) will result in an inductance higher than the inductance range of (5.7) which is not desired. Based on simulation in Ansys Maxwell, and through verifying in practice, $N_L = 62$ is selected. The measured inductance ($L_a = L_{a1} + L_{a2} + 2M_a$) of the laboratory prototype is 295 μH which satisfies the inductance range of (5.7). While on the subject, fewer number of turns helps in decreasing the flux density according to the $Ni = \mathcal{R}\Phi$ equation for inductors which in turn reduces the core loss, and there will be more window area in the core for all three windings as well.

4.1.10 Magnetizing Inductance L_{ma}

Considering Fig. 4.3(b), the magnetizing inductance of T_a denoted as L_{ma} is calculated as follows:

$$\begin{cases} L_{ma} = \dfrac{N_P^2}{\mathcal{R}_{center} + \dfrac{\mathcal{R}_{outer}}{2}} \\ \mathcal{R}_{outer} = \dfrac{g_1}{\mu_0 A_{eo}} = 8.9 \times 10^6 \\ \mathcal{R}_{center} = \dfrac{g_1}{\mu_0 A_e} = 4.56 \times 10^6 \\ N_P = 60 \end{cases} \implies L_{ma} = 399\ \mu\text{H}. \tag{4.37}$$

4.1.11 Flux Calculation

The maximum flux density of T_a and L_a calculated in (4.20) and (4.19) respectively are based on the number of turns obtained in (4.26), (4.27), and (4.34). For transformers, according to $V = 4N\Phi f$ which is for a square-shaped excitation, N and $\hat{B}$ are inversely related, while for inductors, according to $Ni = \mathcal{R}\Phi$, N and $\hat{B}$ are proportionally related. Therefore, based on the chosen number of turns for T_a and L_a in practice, the maximum flux density of T_a and L_a is changed respectively as follows:

$$\hat{B}_T = 80.9\ \text{mT} \times \frac{58.1}{60} = 78.34\ \text{mT}. \tag{4.38}$$

$$\hat{B}_L = 93.12\ \text{mT} \times \frac{62}{69.96} = 82.52\ \text{mT}. \tag{4.39}$$

One of the challenges of magnetic integration is the saturation problem that might occur in the core. According to (4.4), (4.38), and (4.39), the maximum flux passing through the core denoted as $\hat{\Phi}_{tot}$ happens in outer legs, and is the summation of the flux created by L_a and half of the flux created by T_a which is obtained as:

$$\hat{\Phi}_{tot} = \hat{B}_L \times A_{eo} + \frac{\hat{B}_T \times A_e}{2} = 1.987 \times 10^{-5}\ \text{Wb}. \tag{4.40}$$

Then, the maximum flux density of the design denoted as $\hat{B}_{tot}$ is obtained as:

$$\hat{B}_{tot} = \frac{\hat{\Phi}_{tot}}{A_{eo}} = 159\ \text{mT}. \tag{4.41}$$

The other way to calculate $\hat{B}_{tot}$ is by obtaining the formula of $\hat{\Phi}_{tot}$. According to (4.4) and (4.5), and the waveforms of i_{C2}, i_{in}, and i_{La} during a switching period shown in Fig. 2.3, it can be inferred that the maximum flux passing through the core denoted as $\hat{\Phi}_{tot}$ happens in outer legs, and according to (4.4), (4.5),(5.22),(5.53),(5.55), and by considering $|\sin\omega_l t| = 1$, and neglecting the bus voltage ripples, can be obtained as:

$$\hat{\Phi}_{tot} = (|\frac{N_S(\frac{V_{bus}}{L_{ma}} + \frac{3V_m}{L_a}) - N_P\frac{2V_m}{L_a}}{\mathcal{R}_{outer} + 2\mathcal{R}_{center}}| + \frac{N_L V_m}{\mathcal{R}_{outer} L_a})\frac{T_{sw}}{4}, \tag{4.42}$$

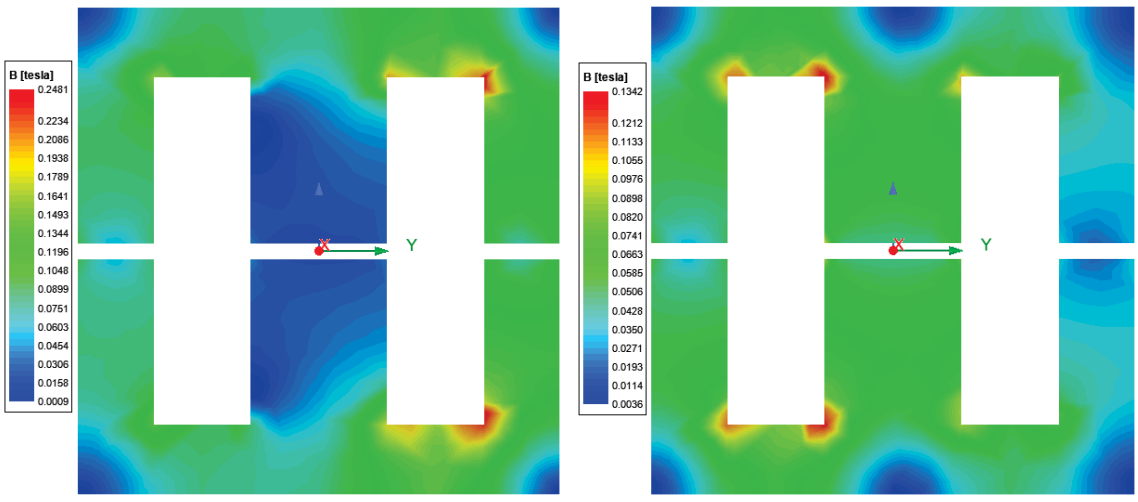
which for the chosen operating point is calculated as:

$$\hat{\Phi}_{tot} \approx 2.05 \times 10^{-5} \text{ Wb}, \tag{4.43}$$

and $\hat{B}_{tot}$ is obtained as:

$$\hat{B}_{tot} = \frac{\hat{\Phi}_{tot}}{A_{eo}} = 164 \text{ mT}. \tag{4.44}$$

The value of $\hat{B}_{tot}$ obtained in (4.41) and (4.44) is nearly the same and lower than the saturation flux density of 3C94 ferrite material at 80 kHz which is 300 mT. Therefore, working in the linear region of the core is guaranteed. To verify this, the simulation of the design in Ansys Maxwell is conducted and shown in Fig. 4.5 which is compatible with calculations. The maximum flux density of the middle leg and outer legs does not happen at the same time.



(a) (b)

Figure 4.5: Maximum flux density of (a) outer legs, and (b) middle leg shown in Ansys Maxwell

4.1.12 Core Loss

Using the $P_{fe,sp} - \hat{B} - f$ graph of 3C94 ferrite material shown in Fig. 4.4, the core loss per volume of the design denoted as $P_{fe,sp,tot}$ at $\hat{B}_{tot} = 159$ mT, and $f_{sw} = 80$ kHz is obtained as:

$$P_{fe,sp,tot} \approx 120 \text{ kW m}^{-3}, \tag{4.45}$$

and the maximum core loss of the design is calculated as:

$$P_{fe,max} = P_{fe,sp,tot} \times \mathcal{V}_e = 3.2 \text{ W}. \tag{4.46}$$

This means if the design steps of the flowchart shown in Fig. 4.1 are followed, the core loss will be less than 3.2 W.

4.1.13 Allocation of Copper Loss Budget

The copper loss budget of the design is 2.205 W according to (4.9). Extra caution should be considered for selecting the wires as choosing inappropriately causes the copper loss to exceed the budget which in turn invalidates the whole design. The copper loss budget ($P_{h,cu}$) must be distributed between the three windings;

1. The primary winding of T_a with 60 turns.
2. The secondary winding of T_a with 30 turns.
3. The winding of L_a with 62 turns.

The copper loss allocation coefficient denoted as α_i which determines the allocated copper loss budget to the i_{th} winding is defined as [68]:

$$\alpha_i = \frac{N_i I_{rms,i}}{\sum N_i I_{rms,i}}, \tag{4.47}$$

where N_i is the number of turns and $I_{rms,i}$ is the rms current of the i_{th} winding.

Then, $P_{h,cu,i}$ which is the copper loss budget of the i_{th} winding is obtained as:

$$P_{h,cu,i} = \alpha_i P_{h,cu}. \tag{4.48}$$

4.1.14 Wire Diameters

After determining the copper loss budget of all three windings, their minimum wire diameter is obtained according to the power equation, as follows:

$$\begin{cases} P_{h,cu,i} = R_{dc,i} \times I_{rms,i}^2 \\ R_{dc,i} = \dfrac{\rho\ l_{Ti} N_i}{\dfrac{\pi d_i^2}{4}} \end{cases} \implies d_i \geq \frac{2}{\sqrt{\pi}} I_{rms,i} \sqrt{\frac{\rho\ l_{Ti} N_i}{P_{h,cu,i}}}, \tag{4.49}$$

where $R_{dc,i}$ is the dc resistance of the i_{th} winding, l_{Ti} is the mean-length-per-turn of the i_{th} winding, and ρ is copper resistivity equal to $\rho = 1.68 \times 10^{-8}$.

To determine the minimum wire diameter of each winding, first of all, according to (4.47), α_L, α_P, and α_S are calculated as the copper loss allocation coefficient of L_a winding, primary and secondary windings of T_a respectively, as follows:

$$\begin{cases} \alpha_L = \dfrac{N_L I_{La,rms}}{N_P I_{in,rms} + N_L I_{La,rms} + N_S I_{C2,rms}} \overset{(4.2)}{=} 0.375 \\ \alpha_P = \ \ldots\ = 0.33 \\ \alpha_S = \ \ldots\ = 0.295. \end{cases} \tag{4.50}$$

Then according to (4.48), the copper loss budget of L_a winding is obtained as:

$$P_{h,cu,L} = 0.83 \text{ W}, \tag{4.51}$$

and the copper loss budget of T_a primary winding is calculated as:

$$P_{h,cu,P} = 0.73 \text{ W}, \tag{4.52}$$

and the copper loss budget of T_a secondary winding is calculated as:

$$P_{h,cu,S} = 0.65 \text{ W}. \tag{4.53}$$

By determining the copper loss budget of each winding, according to (4.49), the wire diameter of L_a winding is calculated as:

$$d_L \geq \frac{2}{\sqrt{\pi}} I_{La,rms} \sqrt{\frac{\rho\ l_{TL} N_L}{P_{h,cu,L}}} = 0.52 \text{ mm}, \tag{4.54}$$

the wire diameter of T_a primary winding is obtained as:

$$d_P \geq 0.58 \text{ mm}, \tag{4.55}$$

and the wire diameter of T_a secondary winding is obtained as:

$$d_S \geq 0.832 \text{ mm}. \tag{4.56}$$

In (4.49), only the dc loss of wires is considered, whereas due to high frequency content of currents, ac loss associated with skin effect and proximity effect also exists in windings as illustrated in Fig. 4.6.

In practice, the diameter of wires is selected much larger than the obtained value from (4.49) to reduce the total loss. However, there are some restrictions associated with larger wire diameters as listed below:

1. The wires can be selected as thick as possible as long as the window area of the chosen core has enough space for them.

2. By enlarging the wire diameters, although the dc ohmic loss decreases, the ac loss associated with skin effect will increase significantly if single wires are used due to the increase of $z = \dfrac{d}{\delta}$ ratio of wires where δ is defined as skin depth.

3. Another challenge regarding the magnetic design is proximity effect. Normally, when a winding is wrapped in several layers, the ac loss associated with proximity effect becomes too large. A good practice is to enlarge the wire diameter as long as the winding will not become more than three layers.

Therefore, there is a trade-off between dc ohmic and ac losses. Extra caution must be considered for selecting appropriate wires.

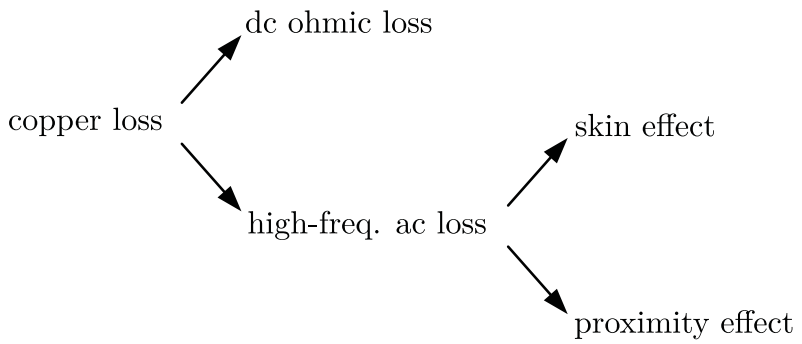


Figure 4.6: Copper loss in a wire

4.1.15 Skin and Proximity Effects

4.1.15.1 Skin Effect

The area near the wire surface where most of the ac current flows is called skin depth (δ) which for copper at $100°C$, is calculated as:

$$\delta \approx \frac{7.5 \text{ cm}}{\sqrt{f_{sw}}}. \tag{4.57}$$

For this magnetic design, it can be obtained that:

$$80 \text{ kHz} \leq f_{sw} \leq 150 \text{ kHz} \implies$$

$$0.194 \text{ mm} \leq \delta \leq 0.265 \text{ mm}. \tag{4.58}$$

As a rule of thumb, selecting wires with diameter to skin depth ratio of greater than 1.6 results in higher ac loss [68]. Therefore, for this magnetic design, the diameter of wires denoted as d should be selected as:

$$z = \frac{d}{\delta} < 1.6 \implies d < 1.6\delta < 0.31 \text{ mm}. \tag{4.59}$$

By noticing the conflict between (4.54),(4.55),(4.56) that consider the dc ohmic loss, and (4.59) which considers the high frequency ac loss, it can be inferred that using single wires for this design is not appropriate because the combined dc ohmic and high frequency ac losses will exceed the copper loss budget. Therefore, Litz wires that their strands satisfy the $z = \frac{d_{strand}}{\delta} < 1.6$ constraint should be chosen.

4.1.15.2 Proximity Effect

The proximity effect results in the poor utilization of the wire cross section area even if a good Litz wire is chosen. This in turn increases the ac loss significantly.

The proximity effect happens not only between adjacent wires but also between the wire and ferrite core. A similar increase in losses appears when wires are tightly wrapped around the core legs and very close to them. This issue becomes more severe near the airgap area because of the fringing effect.

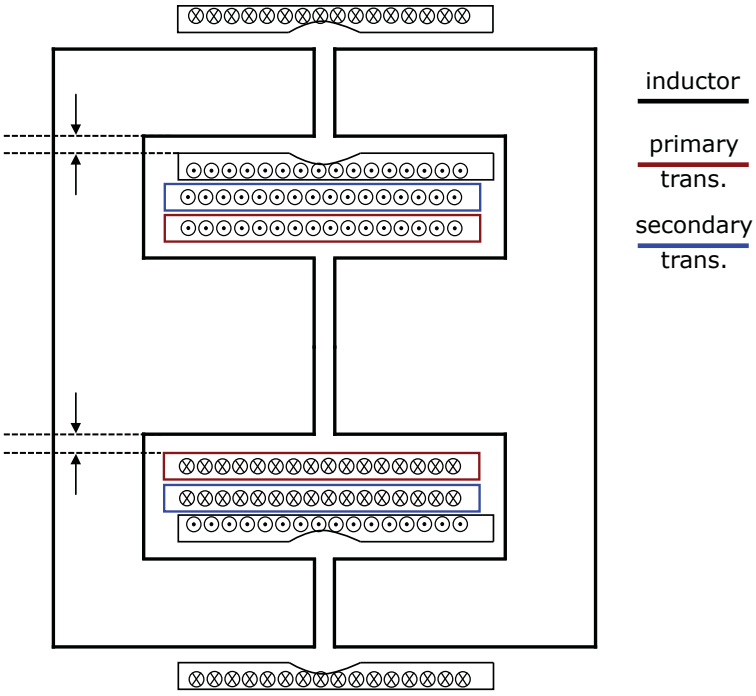


Figure 4.7: Arrangement of T_a and L_a windings

4.1.16 Arrangement of Wires

In this design, and to tackle the proximity effect related to the windings of T_a, the transformer wires are selected such that the windings will not become more than three layers by utilizing the full length of the middle leg. In addition and to avoid the proximity effect between the windings and ferrite core, a certain distance is provided between the primary winding and middle leg.

The inductor winding is wrapped around the outer legs. To address the proximity effect caused by L_a, the inductor wire is chosen with the purpose that firstly the winding will not become more than two layers, and secondly there will be enough window area in the core for providing a distance between the winding and core legs which becomes larger closer to the airgap area.

The arrangement of the windings is shown in Fig. 4.7.

4.1.17 Selected Wires

According to the available wires, and by considering (4.59) for the strands, and (4.54),(4.55), and (4.56) for the whole wire, the Litz wire with 7 strands of AWG30 (7/30) is chosen for the primary winding of T_a and L_a winding, and the Litz wire with 360 strands of AWG44 (360/44) is chosen for the secondary winding of T_a.

The rule of thumb in selecting the wires is to calculate their current density which is denoted as J [$\mathrm{A\,m^{-2}}$]. A good design will result in a current density of:

$$3\ \mathrm{A\,m^{-2}} < J < 5\ \mathrm{A\,m^{-2}}. \tag{4.60}$$

The current density of a wire is defined as:

$$J = \frac{I_{rms,i}}{\mathcal{P} \times A_{single}}, \tag{4.61}$$

where $\mathcal{P}$ is the number of strands, and A_{single} is the cross sectional area of each strand.

The wire current density of L_a winding is calculated as:

$$J_L = \frac{I_{La,rms}}{7 \times A_{\mathrm{AWG30}}} = 4.47\ \mathrm{A\,m^{-2}}, \tag{4.62}$$

and the wire current density of the primary winding of T_a is obtained as:

$$J_P = \frac{I_{in,rms}}{7 \times A_{\mathrm{AWG30}}} = 4.07\ \mathrm{A\,m^{-2}}, \tag{4.63}$$

and the wire current density of the secondary winding of T_a is obtained as:

$$J_S = \frac{I_{C2,rms}}{360 \times A_{\mathrm{AWG44}}} = 3.58\ \mathrm{A\,m^{-2}}. \tag{4.64}$$

4.1.18 Copper Loss

The copper loss of the design includes dc ohmic and high frequency ac losses.

4.1.18.1 DC Ohmic Loss

The dc resistance of a winding with Litz wire is obtained as [68]:

$$R_{dc} = \frac{\rho\ l_T N}{\frac{\pi}{4} d_{single}^2 \mathcal{P}}, \tag{4.65}$$

where d_{single} is the diameter of each strand.

Using this formula, the dc resistance of the three windings are obtained as follows:

$$R_{L,dc} = 0.162\ \mathrm{m\Omega}. \tag{4.66}$$

$$R_{P,dc} = 0.197\ \mathrm{m\Omega}. \tag{4.67}$$

$$R_{S,dc} = 0.056\ \mathrm{m\Omega}. \tag{4.68}$$

Then, the dc ohmic loss corresponding to these three windings are obtained as follows:

$$P_{L,dc} = R_{L,dc} \times I_{La,rms}^2 = 0.41 \text{ W}. \tag{4.69}$$

$$P_{P,dc} = R_{P,dc} \times I_{in,rms}^2 = 0.414 \text{ W}. \tag{4.70}$$

$$P_{S,dc} = R_{S,dc} \times I_{C2,rms}^2 = 0.372 \text{ W}. \tag{4.71}$$

4.1.18.2 High Frequency AC Loss

The high frequency ac loss of the design is divided between the transformer windings and inductor winding.

4.1.18.2.1 AC Loss of T_a To determine the ac copper loss of T_a, the ac resistance of its windings will be obtained.

The equivalent frequency of transformer windings is defined as [68]:

$$f_{eq} = f_{sw}(\frac{d_{single}}{0.5 \text{ mm}})^2, \tag{4.72}$$

which is used to determine the ac loss of windings.

Using (4.72) and by considering $f_{sw} = 80$ kHz, the equivalent frequency of the primary winding of T_a for which AWG30 is selected is calculated as:

$$f_{eq,P} = 80 \text{ kHz } (\frac{d_{\text{AWG30}}}{0.5 \text{ mm}})^2 = 20.74 \text{ kHz}, \tag{4.73}$$

and the equivalent frequency of the secondary winding for which AWG44 is selected is obtained as:

$$f_{eq,S} = 80 \text{ kHz } (\frac{d_{\text{AWG44}}}{0.5 \text{ mm}})^2 = 0.8 \text{ kHz}. \tag{4.74}$$

The ac to dc resistance ratio of transformer windings is obtained as follows [68]:

$$\frac{R_{ac}}{R_{dc}} = m_E^2 k_{tf} = \mathcal{P} m^2 k_{tf}, \tag{4.75}$$

where m_E is the winding's effective number of layers, m is the winding's actual number of layers, and k_{tf} is the transformer factor obtained from the graph shown in Fig. 4.8.

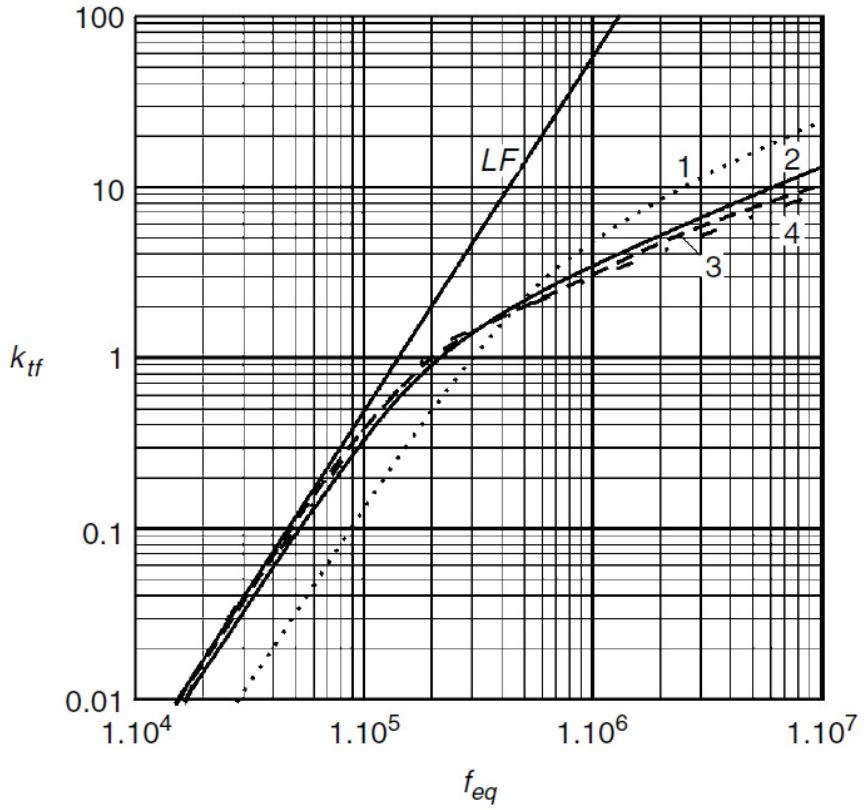


Figure 4.8: Transformer factor k_{tf}, [68]; (1) and dotted line for $m_E = 0.5$, (2) and solid line for $m_E = 1$, (3) and dashed for $m_E = 2$, (4) and dash-dot for $m_E > 2$, LF = low frequency approximation.

For this design, the actual number of layers of the primary winding is $m_P = 3$, and that of the secondary winding is $m_S = 2$. Then according to (4.73) and (4.74), and using Fig. 4.8, k_{tf} of both windings will be determined.

After obtaining all the required parameters and according to (4.75), the ac resistance of the primary winding of T_a is calculated as:

$$\frac{R_{P,ac}}{R_{P,dc}} \approx 0.78 \quad \overset{(4.67)}{\Longrightarrow} \quad R_{P,ac} = 0.153 \text{ m}\Omega, \tag{4.76}$$

and the ac resistance of the secondary winding is calculated as:

$$\frac{R_{S,ac}}{R_{S,dc}} \approx 0.55 \quad \overset{(4.68)}{\Longrightarrow} \quad R_{S,ac} = 0.03 \text{ m}\Omega. \tag{4.77}$$

Finally, the ac loss of the primary winding is calculated as:

$$P_{P,ac} = R_{P,ac} \times I_{in,rms}^2 = 0.32 \text{ W}, \tag{4.78}$$

and the ac loss of the secondary winding is determined as:

$$P_{S,ac} = R_{S,ac} \times I_{C2,rms}^2 = 0.2 \text{ W}. \tag{4.79}$$

4.1.18.2.2 AC Loss of L_a The ac to dc resistance ratio of inductor windings is obtained as follows [68]:

$$\frac{R_{ac}}{R_{dc}} = (\frac{z^4}{16})(\frac{N^2\mathcal{P}^2 d_{single}^2}{3w^2})(\frac{\pi^2}{4})(\frac{k_f}{\sqrt{1+\frac{(z+0.37)^6}{1024}}}), \tag{4.80}$$

where w is the winding width, and k_f is the inductor factor defined as:

$$k_f = \frac{3.5(0.5-\kappa)^2 + 0.69}{\kappa}, \tag{4.81}$$

where

$$\kappa = \frac{d_{\text{wg}} + \frac{t_{\text{w}}}{3}}{\frac{w}{K_{\text{sy}}}}, \tag{4.82}$$

in which d_{wg} is the distance between the winding and core leg, t_{w} is the winding thickness, and K_{sy} is the symmetry factor. $K_{\text{sy}} = 2$ for a center-gapped inductor.

The importance of the distance between the winding and ferrite core previously discussed in "Proximity Effect" section is validated because according to (4.80),(4.81) and (4.82), by increasing d_{wg}, the ac resistance of the winding decreases.

The approximate arrangement of L_a winding is shown in Fig. 4.9.

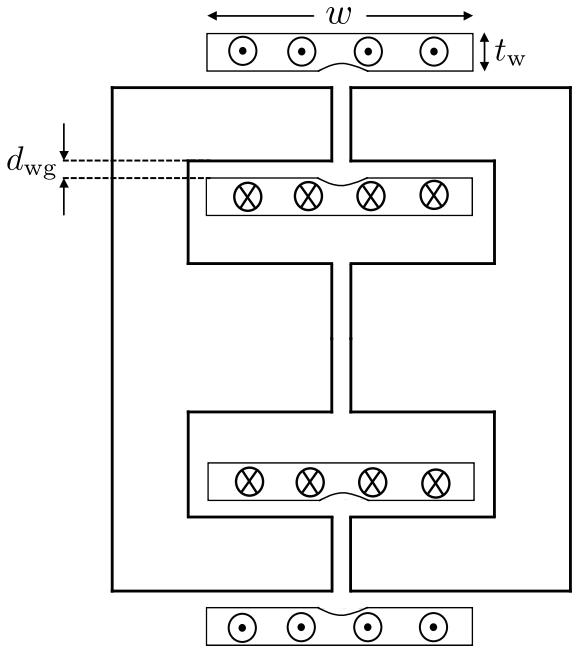


Figure 4.9: Arrangement of L_a winding

The optimum value of κ is around 0.6 or more that could not be achieved for this integrated magnetic because of the limited window area. For the constructed inductor (L_a), $\kappa \approx 0.2$ is calculated by using (4.82). Then according to (4.81), the inductor factor is calculated as:

$$k_f = 5.025. \tag{4.83}$$

Finally, according to (4.80), and because AWG30 strands are selected with $z = 0.96$, at $f_{sw} = 80\ kHz$, the ac resistance of L_a winding is calculated as:

$$\frac{R_{L,ac}}{R_{L,dc}} = (\frac{z^4}{16})(\frac{N_L^2 \mathcal{P}^2 d_{\mathrm{AWG30}}^2}{3w^2})(\frac{\pi^2}{4})(\frac{k_f}{\sqrt{1+\frac{(z+0.37)^6}{1024}}}) = 1.068 \quad \overset{(4.66)}{\Longrightarrow} \quad R_{L,ac} = 0.173\ \mathrm{m\Omega}, \tag{4.84}$$

and the ac copper loss of L_a is calculated as:

$$P_{L,ac} = R_{L,ac} \times I_{La,rms}^2 = 0.438\ \mathrm{W}. \tag{4.85}$$

4.1.19 Total Calculated Loss

The copper loss of a winding is the summation of dc ohmic and ac losses. According to (4.70), (4.71), (4.78), and (4.79), the copper loss of the primary and secondary windings of T_a is calculated respectively as follows:

$$P_{P,cu} = P_{P,dc} + P_{P,ac} = 0.41 + 0.32 = 0.73 \text{ W} \leq P_{h,cu,P} = 0.73 \text{ W}. \tag{4.86}$$

$$P_{S,cu} = P_{S,dc} + P_{S,ac} = 0.372 + 0.2 = 0.572 \text{ W} < P_{h,cu,S} = 0.65 \text{ W}. \tag{4.87}$$

The calculated copper loss is less than the copper loss budgets calculated in (4.52) and (4.53). Therefore, the design is acceptable.

Similarly, according to (4.85), and (4.69), the copper loss of L_a winding is calculated as:

$$P_{L,cu} = P_{L,dc} + P_{L,ac} = 0.41 + 0.438 = 0.848 \text{ W} \approx P_{h,cu,L} = 0.83 \text{ W}. \tag{4.88}$$

The calculated copper loss is almost equal to the copper loss budget calculated in (4.51). Therefore, the design is acceptable.

The total copper loss of the design is then calculated as:

$$P_{cu} = P_{L,cu} + P_{P,cu} + P_{S,cu} = 0.848 + 0.73 + 0.572 = 2.15 \text{ W}. \tag{4.89}$$

Finally, according to (4.46), and (4.89), the total estimated loss of the design including copper and core losses is calculated as:

$$P_{Ta+La} = P_{fe,max} + P_{cu} = 3.2 + 2.15 = 5.35 \; W. \tag{4.90}$$

4.1.20 Experimental Prototype

The magnetic design is then constructed as displayed in Fig. 4.10, and the measured parameters are shown in Table. 4.1.

Table 4.1: Experimental prototype parameters

Parameter	Value
L_a	295 μH
L_{ma}	415 μH

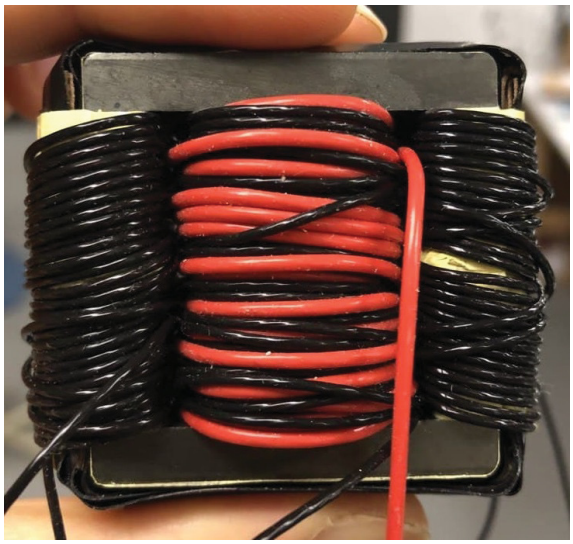


Figure 4.10: The constructed prototype of PFC integrated magnetic ($T_a + L_a$)

4.2 Magnetic Integration of T_r

To achieve a higher power density, the LLC transformer and inductor are also integrated. The design of this integrated magnetic is similar to the previous one. Ferrite material 3C94, and magnetic core EE30 which is comprised of two E30/15/7 cores placed on each other are selected.

The number of turns of the primary winding of T_r is chosen as $N_{r1} = 27$, and using the transformer turns ratio obtained in (3.8), $N_{r2} = 7$ is selected. Furthermore, based on the available Litz wires, the Litz wire with 360 strands of AWG44 (360/44) is chosen for the primary winding of T_r, and the Litz wire with 1000 strands of AWG46 (1000/46) is chosen for the secondary winding of T_r.

The estimated total loss of the design including core and copper losses is obtained as:

$$P_{Tr} = P_{fe,max,llc} + P_{cu,llc} \approx 1.125 + 0.85 = 1.975 \text{ W}. \tag{4.91}$$

The main difference of this design is that the leakage inductance of T_r is utilized as L_r. Therefore, it must be as large as 80 μH according to (3.10). To achieve this, the primary and secondary windings are separated from each other using a magnetic ferrite sheet. The primary winding is wrapped around the upper part of the middle leg, while the secondary winding is wrapped at the bottom, with a ferrite sheet placed between them. The thickness of the ferrite sheet is selected such that the desired leakage inductance is obtained.

The prototype of this magnetic design is constructed as shown in Fig. 4.11, and the measured parameters are shown in Table. 4.2.

Table 4.2: Leakage and magnetizing inductance of the experimental prototype

Parameter	Value
L_r	80 μH
L_{mr}	600 μH

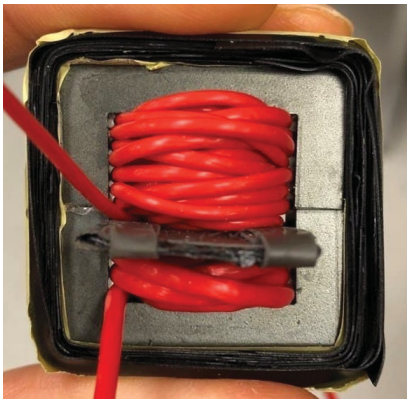


Figure 4.11: The constructed prototype of LLC integrated magnetic (T_r)

4.3 Summary

This chapter provides optimal magnetic designs for the proposed LED driver. The magnetic integration of T_a and L_a based on the structure according to which they share the same core without any flux interaction, is investigated. The design flowchart of a magnetic design is followed, and accordingly appropriate core material, core size, number of turns and wires for windings are selected. Finally, the total loss of the design is calculated, and the prototype based on design calculations is constructed and verified in practice.

Following the same design steps, the magnetic integration of T_r is also carried out. The primary and secondary windings of T_r are separated using a magnetic ferrite sheet to utilize the leakage inductance as L_r. Finally, the total loss of the design is calculated, and the prototype based on design calculations is constructed and verified in practice.

Chapter 5

Design and Analysis

Design and thorough analysis of every power electronics converter is essential to achieve proper performance and avoid iterations in design process and over-design of converters leading to high cost of products.

The PFC inductance (L_a) is designed using the power equation, and the capacitances are designed by allowing 40% peak-to-peak voltage ripples across them, and using either the amount of power they need to process or their charge balance property. During the design of C_2, the formula of i_{C2} and its important values are obtained illustrating why it helps both S_1 and S_2 in achieving turn-on ZVS.

The stress and loss analyses of components are also carried out. Based on stress analysis, the voltage and current limits of components are determined, and based on loss analysis, the lowest efficiency of the converter at full-load is calculated. Finally, the efficiency of laboratory prototype in different operating points is measured which is compatible with the calculated expected efficiency.

5.1 Design of L_a

The proposed PFC circuit is shown in Fig. 5.1(a). The inductance of PFC circuit denoted as L_a is designed for nominal output power equal to 200 W, and input voltage range of $(185 - 265)$ V_{rms}. The value of L_a is determined assuming $\eta = 1$, where η is the converter efficiency.

The input power waveform during a switching period is depicted in Fig. 5.1(b). During the second half of switching period when S_2 is ON, the input power is zero because i_{in} is zero, and during the first half when S_1 is ON, by neglecting the fundamental voltage ripples during a switching period, the shape of input power is similar to the waveform of i_{in} shown in Fig. 2.3.

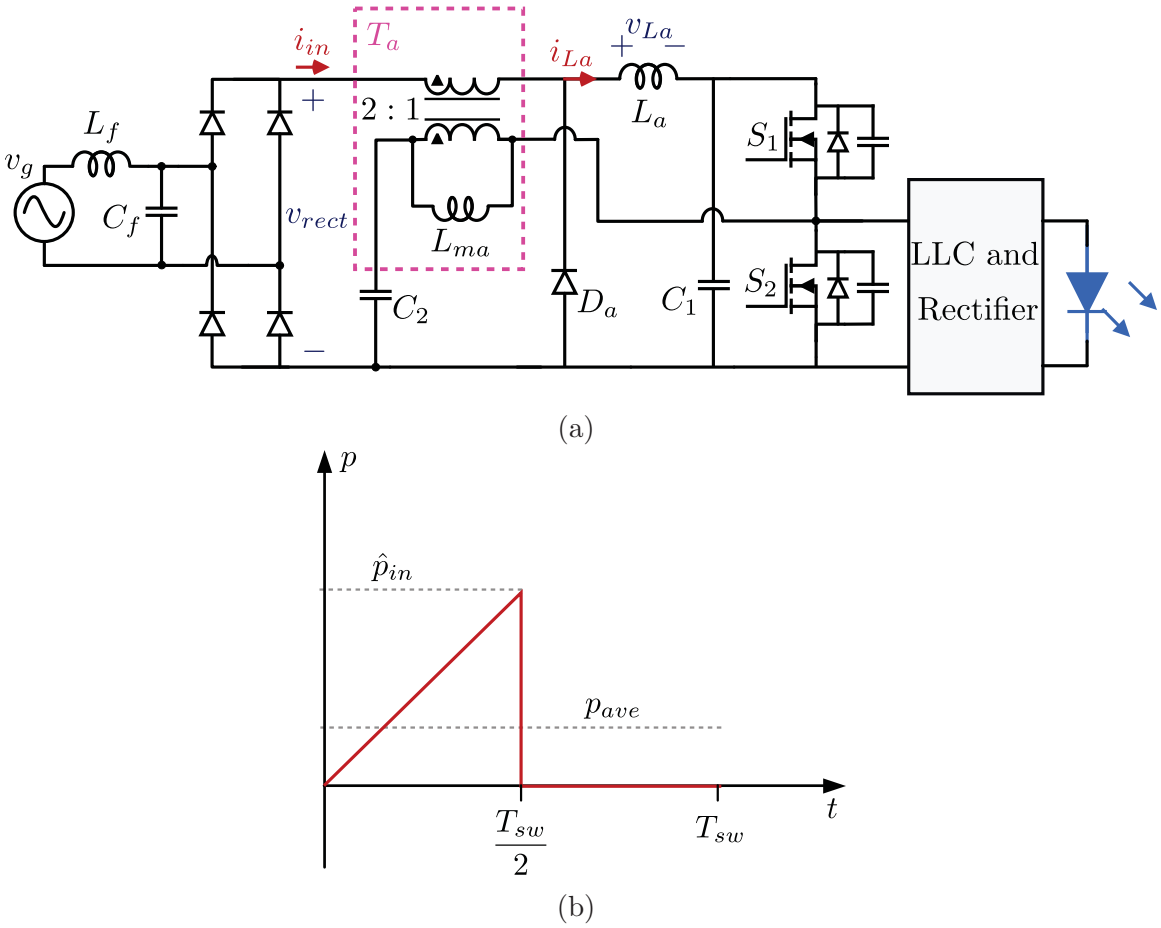


Figure 5.1: (a) PFC circuit of the proposed converter, and (b) input power waveform during a switching period

To obtain the average input power denoted as P_{in}, the instantaneous input power denoted as p_{ave} must be determined which is the average of input power over T_{sw}.

During $0 < t < \dfrac{T_{sw}}{2}$ when S_1 is ON, it can be written that:

$$v_{rect}(t) = |v_g| = V_m|\sin \omega_l t|. \tag{5.1}$$

Then, the maximum of input power during a switching period denoted as $\hat{p}_{in}$ is determined as:

$$\hat{p}_{in} = v_{rect} \times \hat{i}_{in}, \tag{5.2}$$

where $\hat{i}_{in}$ is the maximum of input current previously calculated in (2.18).

According to (5.1), (5.2) and (2.18), $\hat{p}_{in}$ is determined as:

$$\hat{p}_{in} = \frac{V_m^2 \sin^2 \omega_l t}{2 f_{sw} L_a}, \tag{5.3}$$

and the instantaneous input power is obtained as:

$$p_{ave} = \frac{\hat{p}_{in} \dfrac{T_{sw}}{2}}{2T_{sw}} \overset{(5.3)}{=} \frac{V_m^2 \sin \omega_l t^2}{8 f_{sw} L_a} = \frac{V_m^2}{16 f_{sw} L_a}(1 - \cos 2\omega_l t). \tag{5.4}$$

The average input power is the average of (5.4) over line period (T_l), and is obtained as:

$$P_{in} = \frac{\displaystyle\int_0^{T_l} \frac{V_m^2}{16 f_{sw} L_a}(1 - \cos 2\omega_l t)\, dt}{T_l} = \frac{V_m^2}{16 f_{sw} L_a} = P_{out} \tag{5.5}$$

Finally, from (5.5), L_a is obtained in terms of the known parameters as:

$$L_a = \frac{V_m^2}{16 P_{out} f_{sw}}, \tag{5.6}$$

where since L_a is designed for rated power, $P_{out} = 200$ W is considered, and f_{sw} is ranging from 80 kHz to 150 kHz.

Based on (5.6), the PFC inductance range is obtained as:

$$\frac{1 \times (\sqrt{2} \cdot 185)^2}{16 \times 200 \times 80\text{k}} < L_a = \frac{\eta V_m^2}{16 P_{out} f_{sw}} < \frac{1 \times (\sqrt{2} \cdot 265)^2}{16 \times 200 \times 150\text{k}}$$

$$\implies 267\ \mu\text{H} < L_a < 293\ \mu\text{H}. \tag{5.7}$$

The inductance of the experimental prototype is measured as 295 μH.

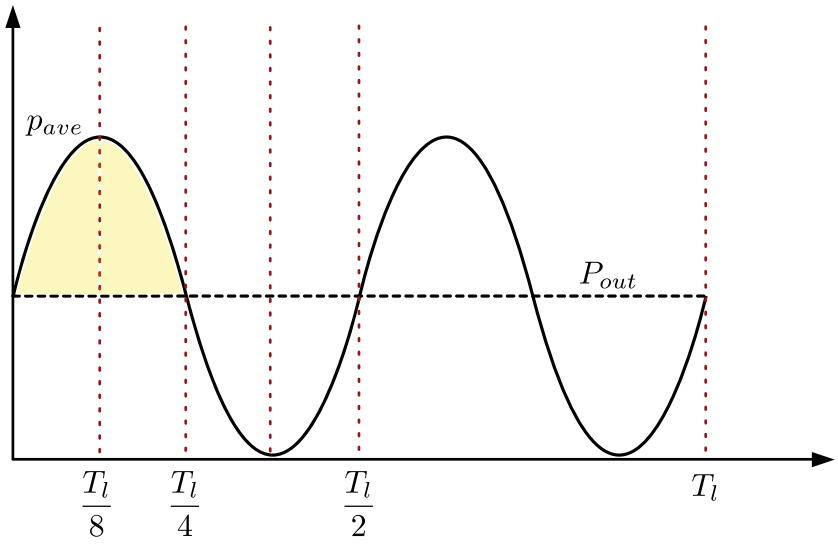


Figure 5.2: Input and output power in one line period

5.2 Design of C_1

The input/output power difference during $[0, \frac{T_l}{4}]$ shown in Fig. 5.2 is the energy change of C_1 denoted as ΔE_{C1} which is calculated as:

$$\Delta E_{C1} = \int_0^{\frac{T_l}{4}} (p_{ave}(t) - P_{out})\, dt = 2\int_0^{\frac{T_l}{8}} (p_{ave}(t) - P_{out})\, dt$$
$$= \frac{1}{2}C_1(V_{bus} + \frac{\Delta V_{bus}}{2})^2 - \frac{1}{2}C_1(V_{bus} - \frac{\Delta V_{bus}}{2})^2, \tag{5.8}$$

where ΔV_{bus} is the peak-to-peak voltage ripple of C_1.

Based on (5.4), and (5.5), equation (5.8) can be rewritten as:

$$2\int_0^{\frac{T_l}{8}} (\frac{V_m^2}{16 f_{sw} L_a} \cos 2\omega_l t)\, dt = C_1 V_{bus} \Delta V_{bus}, \tag{5.9}$$

and ΔV_{bus} can be calculated in terms of circuit parameters including C_1 as:

$$\Delta V_{bus} = \frac{{V_m}^2}{16 L_a f_{sw} \omega_l C_1 V_{bus}}. \tag{5.10}$$

By accepting peak-to-peak voltage ripples up to 40% of V_{bus}, it can be written that:

$$\Delta V_{bus} \leq 0.4\ V_{bus} \implies \frac{{V_m}^2}{16 L_a f_{sw} \omega_l C_1 V_{bus}} \leq 0.4\ V_{bus}, \tag{5.11}$$

and the minimum value of C_1 is obtained as:

$$C_1 \geq \frac{1}{640\pi L_a f_{sw}} (\frac{V_m}{V_{bus}})^2. \tag{5.12}$$

According to the V_{bus} formula obtained in (3.26),

$$\frac{V_m}{V_{bus}} \leq 1. \tag{5.13}$$

Then, (5.12) is rewritten as:

$$C_1 \geq \frac{1}{640\pi L_a f_{sw}}, \tag{5.14}$$

based on which the value of C_1 is decided.

For this converter, $L_a = 295$ μH is selected, and 80 kHz $\leq f_{sw} \leq$ 150 kHz. Therefore, C_1 is calculated as:

$$C_1 \geq 21.074 \ \mu\text{F} \tag{5.15}$$

A 30 μF polyester film capacitor is selected as C_1.

5.3 Design of C_o

Due to the design of a fast controller, low frequency ripples will not appear on LEDs. Therefore, four 4.7 μF polyester film capacitors are chosen as output capacitors.

5.4 Design of C_2

The converter circuit is shown in Fig. 5.3(a) where each winding of T_a is modelled with an inductor in series with a dependent source, v_{C2} contains relatively large switching frequency ripples due to the current shape of this capacitor denoted as i_{C2} shown in Fig. 5.3(b) during a switching period.

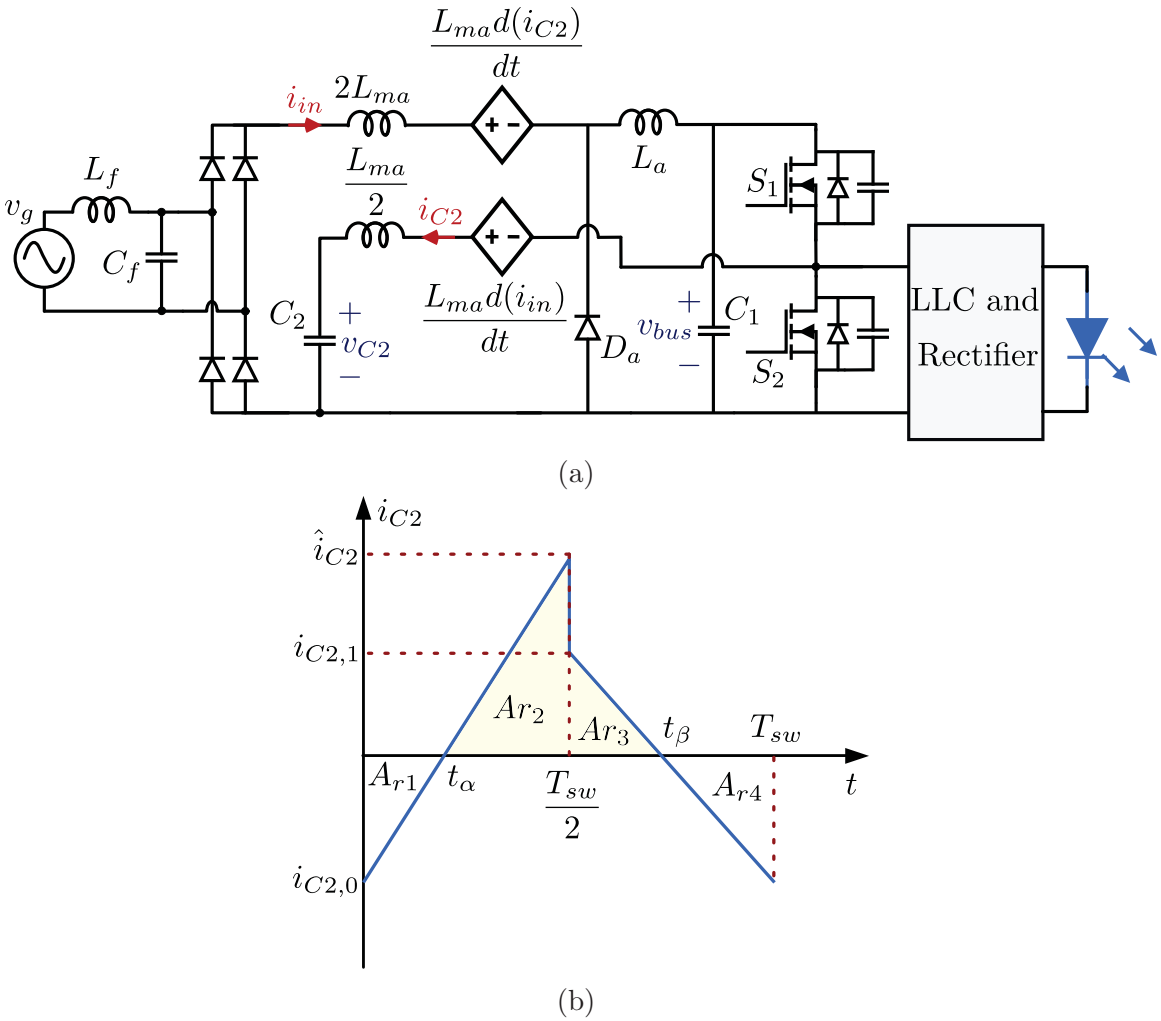


Figure 5.3: (a) The proposed converter with equivalent circuit of T_a, and (b) waveform of i_{C2} during a switching period

During the first half of switching period when S_1 is ON, by writing a KVL, and according to the waveform of i_{in} shown in Fig. 2.3, (2.18) and (2.2), it can be written that:

$$v_{C2} + \frac{L_{ma}}{T_{sw}}(\hat{i}_{C2} - i_{C2,0}) - \frac{L_{ma}}{L_a}V_m|\sin\omega_l t| - v_{bus} = 0$$

$$\implies \hat{i}_{C2} - i_{C2,0} = \frac{v_{bus}}{2f_{sw}L_{ma}} + \frac{V_m|\sin\omega_l t|}{f_{sw}L_a}, \tag{5.16}$$

based on which the slope of i_{C2} during the first half of switching period is obtained as:

$$m_1 = \frac{v_{bus}}{L_{ma}} + \frac{2V_m|\sin\omega_l t|}{L_a}. \tag{5.17}$$

During the second half of switching period when S_2 is ON, i_{in} is clamped to zero. By writing a KVL, and according to (2.2), it can be written that:

$$v_{C2} + \frac{L_{ma}}{T_{sw}}(i_{C2,0} - i_{C2,1}) = 0 \implies i_{C2,0} - i_{C2,1} = \frac{-v_{bus}}{2f_{sw}L_{ma}}, \tag{5.18}$$

based on which the slope of i_{C2} during the second half of switching period is obtained as:

$$m_2 = \frac{-v_{bus}}{L_{ma}}. \tag{5.19}$$

Considering Fig. 5.3(b), the following equations can be written:

$$\begin{cases} \dfrac{\frac{T_{sw}}{2} - t_\alpha}{t_\alpha} = \dfrac{\hat{i}_{C2}}{-i_{C2,0}} \\ \\ \dfrac{t_\beta - \frac{T_{sw}}{2}}{T_{sw} - t_\beta} = \dfrac{i_{C2,1}}{-i_{C2,0}}, \end{cases} \tag{5.20}$$

based on which t_α and t_β are determined in terms of T_{sw}, $\hat{i}_{C2}$, $i_{C2,0}$, and $i_{C2,1}$.

Then according to charge balance property of C_2, it can be written that:

$$A_{r1} + A_{r2} + A_{r3} + A_{r4} = 0, \tag{5.21}$$

which by solving and using (5.20), $\hat{i}_{C2}$, $i_{C2,0}$, and $i_{C2,1}$ are calculated respectively as follows:

$$\hat{i}_{C2} = (\frac{v_{bus}}{L_{ma}} + \frac{3V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4}. \tag{5.22}$$

$$i_{C2,0} = -(\frac{v_{bus}}{L_{ma}} + \frac{V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4}. \tag{5.23}$$

$$i_{C2,1} = (\frac{v_{bus}}{L_{ma}} - \frac{V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4}. \tag{5.24}$$

It is worth mentioning that $i_{C2,0}$ helps in achieving turn-on ZVS for $S1$, and $i_{C2,1}$ helps in achieving turn-on ZVS for S_2.

The formula of i_{C2} during the first half of switching period according to (5.22) and (5.23), is obtained as:

$$i_{C2}(t) = (\frac{v_{bus}}{L_{ma}} + \frac{2V_m|\sin\omega_l t|}{L_a})t - (\frac{v_{bus}}{L_{ma}} + \frac{V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4}, \tag{5.25}$$

and during the second half of switching period according to (5.24) and (5.23), is obtained as:

$$i_{C2}(t) = \frac{-v_{bus}}{L_{ma}}(t - \frac{T_{sw}}{2}) + (\frac{v_{bus}}{L_{ma}} - \frac{V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4}. \tag{5.26}$$

The area $Ar_2 + Ar_3$ shown on Fig. 5.3 is the total charge stored in C_2 during a switching period which is calculated as:

$$Q_{C2} = Ar_2 + Ar_3 = (\frac{T_{sw}}{8})^2 \frac{(\frac{v_{bus}}{L_{ma}} + \frac{V_m|\sin\omega_l t|}{L_a})^3}{(\frac{v_{bus}}{2L_{ma}} + \frac{V_m|\sin\omega_l t|}{L_a})(\frac{v_{bus}}{2L_{ma}})} = C_2\Delta v_{C2}. \tag{5.27}$$

If similar to the design of C_1, $\Delta v_{C2} < 0.4\ v_{C2}$ is assumed, then according to (2.2),

$$\Delta v_{C2} < 0.2\ v_{bus}, \tag{5.28}$$

and using (5.27), the minimum value of C_2 is obtained as:

$$C_2 > \frac{T_{sw}^2}{6.4\ k_{C2}^2} \frac{L_{ma}(\frac{k_{C2}}{L_{ma}} + \frac{1}{L_a})^3}{\frac{1}{L_a} + \frac{k_{C2}}{2L_{ma}}}, \tag{5.29}$$

where

$$k_{C2} = \frac{v_{bus}}{V_m|\sin\omega_l t|}. \tag{5.30}$$

Since $k_{C2} > 1$ and the right term of (5.29) decreases by increasing k_{C2}, the worst case scenario is considered assuming $k_{C2} = 1$, and (5.29) can be rewritten as:

$$C_2 > \frac{T_{sw}^2}{6.4} \frac{L_{ma}(\frac{1}{L_{ma}} + \frac{1}{L_a})^3}{\frac{1}{L_a} + \frac{1}{2L_{ma}}}. \tag{5.31}$$

According to the value of L_{ma} and L_a obtained in (4.37) and (5.7) respectively, and by considering $f_{sw} = 80$ kHz, the minimum capacitance of C_2 is calculated as:

$$C_2 > 430\ \text{nF}. \tag{5.32}$$

To further decrease the ripples, and since the price difference of film capacitors is negligible for below 1 μF capacitors, a 1 μF polypropylene film capacitor is selected as C_2.

5.5 Stress Analysis

5.5.1 Voltage Stress of S_1 and S_2

The maximum voltage of either S_1 or S_2 can be written as:

$$V_{S,max} = V_{bus} + \frac{\Delta V_{bus}}{2}, \tag{5.33}$$

and since $\Delta V_{bus} \leq 0.4\ V_{bus}$ is assumed, it can be written that:

$$V_{S,max} \leq 1.2\ V_{bus}. \tag{5.34}$$

According to (3.27), the voltage stress of switches is calculated as:

$$V_{S,max} \leq 1.2\ V_{bus,max} \leq 525\ \text{V}. \tag{5.35}$$

This is the maximum voltage that S_1 and S_2 must withstand for the safe operation. For a similar boost-typed PFC converter operating in DCM with acceptable PF and THD, the voltage stress of switches exceeds 900 V. This is a significant advantage of the proposed LED driver that 600 V rating power MOSFETs can be chosen which are more cost effective than the higher voltage rating ones.

5.5.2 Voltage Stress of Input Diode Bridge and D_a

The maximum voltage of input diode bridge during a switching period happens at Interval VII that is depicted in Fig. 5.4(a). Since $v_{La}(t) = 0$ during this interval, and by writing two KVLs, the output voltage of input diode bridge denoted as v_{rect} is determined as follows:

$$v_{C2} - \frac{v_M(t)}{2} = 0 \implies v_M(t) = v_{bus}, \quad \text{(Interval VII)} \tag{5.36}$$

$$v_{rect}(t) = v_M(t) + v_{bus} \overset{(5.36)}{=} 2v_{bus}. \quad \text{(Interval VII)} \tag{5.37}$$

The maximum voltage of D_a during a switching period happens at Interval III shown in Fig. 5.4(b). By writing two KVLs, the voltage of D_a at this interval is determined as follows:

$$v_{C2} - \frac{v_M(t)}{2} - v_{bus} = 0 \implies v_M(t) = -v_{bus}, \quad \text{(Interval III)} \tag{5.38}$$

$$v_{Da}(t) = v_{rect}(t) - v_M(t) \overset{(5.38)\text{and}(5.1)}{=} V_m|\sin\omega_l t| + v_{bus}. \quad \text{(Interval III)} \tag{5.39}$$

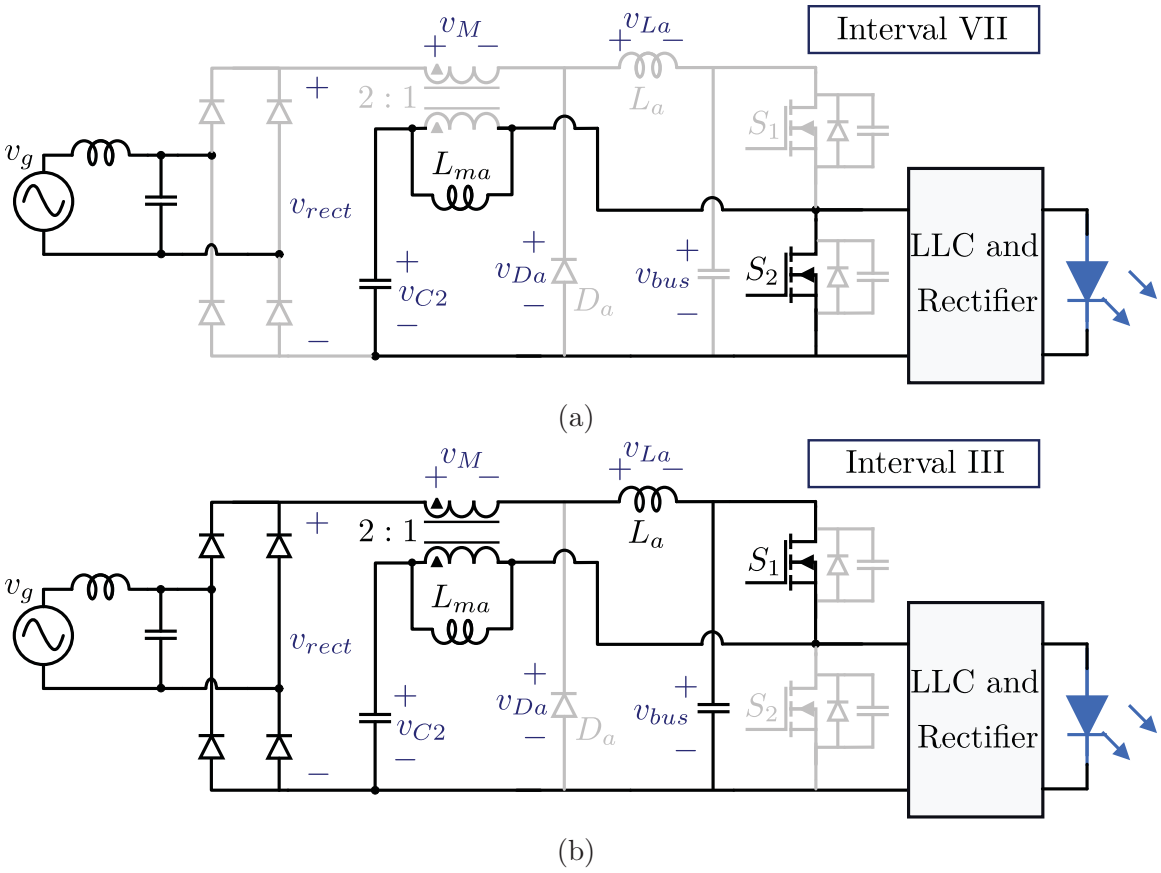


Figure 5.4: (a) Interval VII, and (b) Interval III of the converter operation

Given the peak-to-peak dc bus voltage ripples that are below 40%, and according to (5.37), the voltage stress of input diode bridge can be obtained as:

$$V_{rect,max} \leq 1.2 \times 2V_{bus} = 2.4V_{bus}, \tag{5.40}$$

which according to (3.27), is calculated as:

$$V_{rect,max} \leq 1 \text{ kV}. \tag{5.41}$$

Similarly, according to (5.39), and since $|\sin \omega_l t| \leq 1$, the voltage stress of D_a is calculated as:

$$V_{Da,max} \leq 1.2V_{bus} + V_m < 900 \text{ V}. \tag{5.42}$$

5.5.3 Voltage Stress of Output Rectifying Diodes

By writing a KVL, the voltage of each output rectifying diode when it does not conduct can be obtained as:

$$V_{Dr} = -2V_o = -100 \text{ V}. \tag{5.43}$$

5.5.4 Current Stress of S_1 and S_2

The current of switches can be written as follows:

$$i_{S1}(t) = \begin{cases} i_{C2}(t) + i_{Lr}(t) & 0 < t < \dfrac{T_{sw}}{2} \\ 0 & \dfrac{T_{sw}}{2} < t < T_{sw}. \end{cases} \tag{5.44}$$

$$i_{S2}(t) = \begin{cases} 0 & 0 < t < \dfrac{T_{sw}}{2} \\ -i_{C2}(t) - i_{Lr}(t) & \dfrac{T_{sw}}{2} < t < T_{sw}. \end{cases} \tag{5.45}$$

The maximum of $|i_{C2}(t) + i_{\mathrm{Lr}}(t)|$ happens at $t = \dfrac{T_{sw}}{2}$.

According to (5.25) and (5.22), the value of i_{C2} at $t = \dfrac{T_{sw}}{2}$ is determined as:

$$i_{C2}(t = \frac{T_{sw}}{2}) = \hat{i}_{C2} = (\frac{v_{bus}}{L_{ma}} + \frac{3V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4}. \tag{5.46}$$

In addition, by ignoring the dc bus voltage ripples, the Fourier series formula of i_{Lr} is obtained as:

$$i_{Lr}(t) = \frac{4n_r V_o\ \omega_s\ C_r}{\pi} \sum_{\substack{k=1 \\ odd}}^{\infty} \frac{\cos\left(k\omega_s t - k\theta_s\right)}{(kF)^2 - 1} - \frac{2V_{bus}\ \omega_s\ C_r}{\pi} \sum_{\substack{k=1 \\ odd}}^{\infty} \frac{\cos k\omega_s t}{(kF)^2 - 1}. \tag{5.47}$$

For simplicity, the two series are approximated with their first terms, and (5.47) is simplified as follows:

$$i_{Lr}(t) \approx \frac{8n_r f_{sw} C_r V_o}{F^2 - 1} \cos\left(\omega_s t - \theta_s\right) - \frac{4V_{bus} f_{sw} C_r}{F^2 - 1} \cos\omega_s t$$

$$= \frac{8n_r f_{sw} C_r V_o \cos\theta_s - 4V_{bus} f_{sw} C_r}{F^2 - 1} \cos\omega_s t + \frac{8n_r f_{sw} C_r V_o \sin\theta_s}{F^2 - 1} \sin\omega_s t, \tag{5.48}$$

and its value at $t = \dfrac{T_{sw}}{2}$ is calculated as:

$$i_{Lr}(t = \frac{T_{sw}}{2}) = \frac{4f_{sw} C_r (V_{bus} - 2n_r V_o \cos\theta_s)}{F^2 - 1}. \tag{5.49}$$

According to (5.44), (5.45), (5.22), (5.49), and if a perfect switching with no deadtime is considered, the maximum current of either S_1 or S_2 during a switching period is obtained as:

$$\hat{i}_S = |\hat{i}_{S1}| = |\hat{i}_{S2}| =$$

$$|(\frac{v_{bus}}{L_{ma}} + \frac{3V_m|\sin\omega_l t|}{L_a})\frac{T_{sw}}{4} + \frac{4f_{\rm sw}C_{\rm r}(V_{\rm bus} - 2n_rV_o\cos\theta_s)}{F^2-1}|. \tag{5.50}$$

Finally, if for simplicity, the dc bus voltage ripples are neglected, and $|\sin\omega_l t| = 1$ is considered, the maximum current of either S_1 or S_2 will be obtained as:

$$I_{S,max} = |(\frac{V_{bus}}{L_{ma}} + \frac{3V_m}{L_a})\frac{T_{sw}}{4} + \frac{4f_{sw}C_r(V_{bus} - 2n_rV_o\cos\theta_s)}{F^2-1}|. \tag{5.51}$$

For the worst case scenario in which $f_{sw} = 80$ kHz, $V_m = 262$ V, and $P_{out} = 200$ W, and by calculating V_{bus} from (3.26), and $\cos\theta_s$ from (3.20) and (3.21), the current stress of each switch is calculated as:

$$I_{S,max} \approx 9.8 \text{ A} \tag{5.52}$$

5.5.5 Current Stress of Input Diode Bridge

The output current of input diode bridge is denoted as i_{in} which its maximum during a switching period denoted as $\hat{i}_{in}$ was previously calculated in (2.18). By considering $|\sin\omega_l t| = 1$, the current stress of input diode bridge is determined as:

$$I_{in,max} = \frac{V_m}{2f_{sw}L_a}. \tag{5.53}$$

This current at $V_m = 262$ V, $f_{sw} = 80$ kHz, and $P_{out} = 200$ W, is calculated as:

$$I_{in,max} = 5.55 \text{ A}. \tag{5.54}$$

5.5.6 Current Stress of D_a

The current stress of D_a is similar to input diode bridge, and it can be written that:

$$I_{Da,max} = I_{L_a,max} = I_{in,max}. \tag{5.55}$$

For the worst case scenario, the current stress of D_a is calculated as:

$$I_{D,max} = 5.55 \text{ A}. \tag{5.56}$$

5.5.7 Current Stress of Output Rectifying Diodes

The maximum current of each output rectifying diode can be written as:

$$I_{Dr,max} = |\frac{n_r I_{Lr,max}}{2}|, \tag{5.57}$$

which using (5.48), is obtained as:

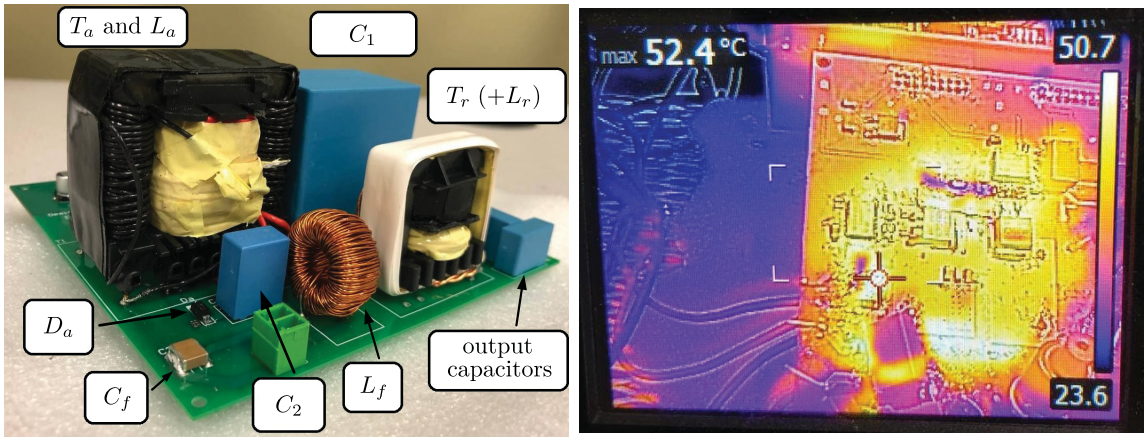
$$I_{Lr,max} = \frac{4 f_{sw} C_r}{F^2 - 1}\sqrt{V_{bus}^2 + (2 n_r V_o)^2} \overset{(5.57)}{\Longrightarrow} I_{Dr,max} = |\frac{2 n_r f_{sw} C_r}{F^2 - 1}|\sqrt{V_{bus}^2 + (2 n_r V_o)^2}, \tag{5.58}$$

and at $V_m = 262$ V, $f_{sw} = 80$ kHz, and $P_{out} = 200$ W, is calculated as:

$$I_{Dr,max} = 7.94 \text{ A}. \tag{5.59}$$

5.6 Loss Analysis

To verify the feasibility of the converter, the prototype of the proposed LED driver is built as shown in Fig.5.5, and the selected components are listed in Table. 5.1.



(a) (b)

Figure 5.5: (a) The experimental prototype, and (b) operating temperature after half an hour

Table 5.1: System parameters

Input End		
Line Frequency	f_l	50 Hz
Input Voltage (rms)	$V_{g,rms}$	185 V to 265 V
Input Filter		
Capacitance	C_f	470 nF
Inductance	L_f	$L_f = 1$ mH
PFC Circuit		
Inductance	L_a	295 μH
Transformer	T_a	$L_{ma} = 415$ μH
Bus Capacitance	C_1	30 μF
Half-bridge LLC Resonant Circuit		
Switching Frequency	f_{sw}	80 kHz to 150 kHz
Resonant Capacitance	C_r	18.1 nF
Half-bridge Capacitance	C_2	1 μF
Transformer	T_r	$L_{mr} = 600$ μH and $L_r = 80$ μH
Rest of the Circuit		
Balancing Capacitance	C_{b1}-C_{b3}	4.7 μF
Output Capacitance	C_{o1}-C_{o4}	4.7 μF
Output End		
Nominal Power	P_{out}	200 W
Output Voltage	V_o	50 V
Output Current	I_o	0.1 A to 1 A

The loss analysis is carried out at $V_m = 262$ V, and $P_{out} = 200$ W which corresponds to $f_{sw} = 80$ kHz. This operating point is expected to yield the lowest efficiency at rated power since the conduction losses at this operating pont are relatively higher.

5.6.1 Loss of S_1 and S_2

Owing to the design of half-bridge LLC resonant circuit, ZVS is obtained for both S_1 and S_2. Therefore, the switching loss of both MOSFETs is negligible. The conduction loss of S_1 and S_2 is calculated as follows:

$$P_{S1} = r_{DS,on} I^2_{rms,S1}, \tag{5.60}$$

$$P_{S2} = r_{DS,on} I^2_{rms,S2}, \tag{5.61}$$

where $r_{DS,on}$ is the ON resistance of MOSFETs.

The rms current of S_1 is obtained as:

$$I_{rms,S1} = \frac{1}{2}\sqrt{2\sum_{k=odd}(1+\cos\xi_k)J_k^2 - \sum_{k=even} H_k^2}, \tag{5.62}$$

where

$$\begin{cases} H_k = \dfrac{V_{bus}}{k\pi f_{sw} L_{ma}} + \dfrac{2V_m}{k\pi f_{sw} L_a}, \\ J_k = \dfrac{V_m}{k\pi f_{sw} L_a}, \\ \cos\xi_k = \dfrac{2n_r V_o \sin k\theta_s}{\sqrt{(2n_r V_o \cos k\theta_s - V_{bus})^2 + (2n_r V_o \sin k\theta_s)^2}}. \end{cases} \tag{5.63}$$

By replacing V_{bus} from (3.22), $\cos\xi_k$ can be rewritten as:

$$\cos\xi_k = \frac{\sin k\theta_s}{\sqrt{(\cos k\theta_s - \dfrac{8.5 - \dfrac{1}{F^2}}{7.5}))^2 + (\sin k\theta_s)^2}}. \tag{5.64}$$

By considering the selected operating point, $\theta_s = 33^\circ$ from (3.18), and $F = 0.6$ are obtained, and it can be approximated that:

$$2\sum_{k=odd}(1+\cos\xi_k)J_k^2 \approx 4\sum_{k=odd} J_k^2. \tag{5.65}$$

Finally, by calculating the series of (5.62), the rms current of S_1 is determined as:

$$I_{rms,S1} \approx \frac{1}{4\sqrt{6}f_{sw}}\sqrt{12(\frac{V_m}{L_a})^2 - (\frac{2V_m}{L_a} + \frac{V_{bus}}{L_{ma}})^2}. \tag{5.66}$$

Similarly, and by writing the Fourier series of $I_{rms,S2}$, the rms current of S_2 is obtained as:

$$I_{rms,S2} \approx \frac{1}{4\sqrt{6}f_{sw}}\sqrt{12(\frac{V_m}{L_a})^2 - (\frac{V_{bus}}{L_{ma}})^2}. \tag{5.67}$$

For the considered operating point, the rms currents are calculated as:

$$I_{rms,S1} \approx 2.3 \text{ A}. \tag{5.68}$$

$$I_{rms,S2} \approx 3.8 \text{ A}. \tag{5.69}$$

UJ3C065030B3 power MOSFETs are used for this converter with $r_{DS,on} = 35$ mΩ. Using (5.60), and (5.61), the conduction loss of S_1 is determined as:

$$P_{S1} \approx 0.185 \text{ W}, \tag{5.70}$$

and the conduction loss of S_2 is calculated as:

$$P_{S2} \approx 0.5 \text{ W}. \tag{5.71}$$

5.6.2 Loss of Input Diode Bridge

Due to the existence of switching harmonics at input of the converter, four individual fast recovery diodes with $t_{rr} = 75\ ns$, and $V_F = 1.2$ V are utilized as diode bridge.

The current of each diode is the half-wave rectified of input current. By assuming that the resistance of diodes are negligible, the power loss of each of them is obtained as:

$$P_{Db} \approx \frac{2P_{out}V_F}{\pi\eta V_m}, \tag{5.72}$$

which for the considered operating point, and assuming $\eta = 0.95$, is calculated as:

$$P_{Db} \approx 0.61 \text{ W}. \tag{5.73}$$

5.6.3 Loss of D_a

The same diode as input bridge is selected as D_a with $V_F = 1.2$ V.

According to (2.13), and by neglecting the dc bus voltage ripples, the duration that D_a conducts is determined as:

$$\Delta t_d = t_6 - t_4 = \frac{V_m}{2 f_{sw} V_{bus}} |\sin \omega_l t|. \tag{5.74}$$

In addition, according to (5.74), (5.55), and (2.18), the average current of D_a is obtained. Finally, by assuming that the diode resistance is negligible, the loss of D_a is determined as:

$$P_{Da} \approx \frac{V_m^2 V_F}{16 f_{sw} L_a V_{bus}}, \tag{5.75}$$

which for the considered operating point, is calculated as:

$$P_{Da} \approx 0.76 \text{ W}. \tag{5.76}$$

5.6.4 Loss of Output Rectifying Diodes

Four fast recovery diodes with $t_{rr} = 25\ ns$, and $V_F = 0.64$ V are chosen as output rectifying diodes to avoid reverse recovery losses. As a result, the power loss of each diode is determined as:

$$P_{Dr} \approx I_o V_F = \frac{P_{out} V_F}{4 V_o}, \tag{5.77}$$

which for the considered operating point, is calculated as:

$$P_{Dr} \approx 0.64 \text{ W}. \tag{5.78}$$

5.6.5 The Lowest Efficiency at Full-Load

The total loss of the converter can be written as:

$$P_{loss} = P_{S1} + P_{S2} + 4P_{Db} + P_{Da} + 4P_{Dr} + P_{Ta+La} + P_{Tr}, \tag{5.79}$$

where the loss of PFC integrated magnetic calculated in (4.90) is denoted as P_{Ta+La}, and P_{Tr} is the loss of LLC integrated magnetic calculated in (4.91).

The efficiency of the converter can be written as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}, \tag{5.80}$$

which for the considered operating, is calculated as:

$$\eta = 93.56\ \%. \tag{5.81}$$

This is the lowest efficiency at full-load. The measured efficiency of the experimental prototype at this operating point is lower than expected, but at rated power and nominal input voltage, $\eta = 93.3\ \%$.

5.7 Experimental Results

Using a Tektronix 5 series Mixed Signal Oscilloscope model MS058, the efficiency of the converter for different operating points have been measured as illustrated in Fig.5.6 and Fig.5.7 . Since the converter has four output channels, it was not possible to measure the efficiency using a two-channel power analyzer.

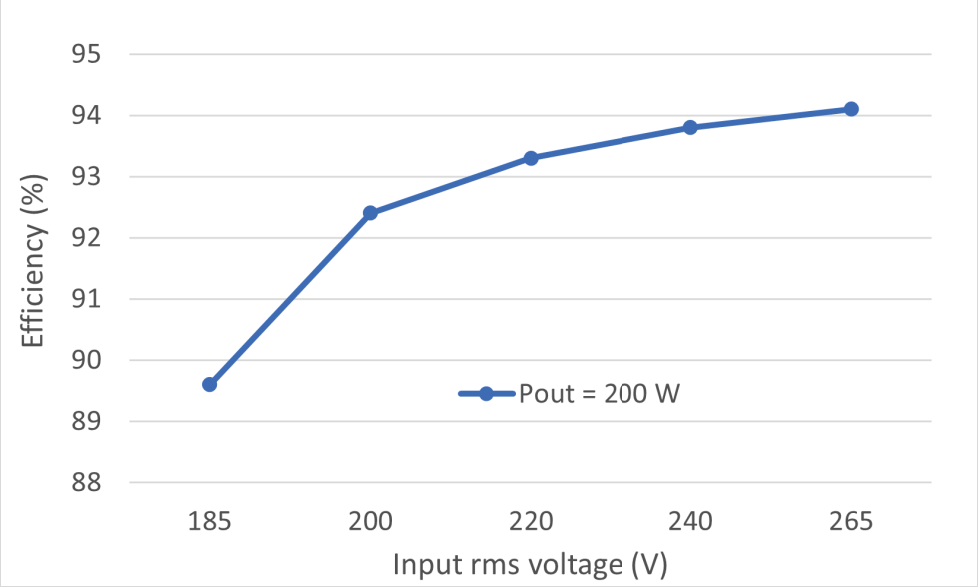


Figure 5.6: Efficiency of the prototype with respect to input voltage

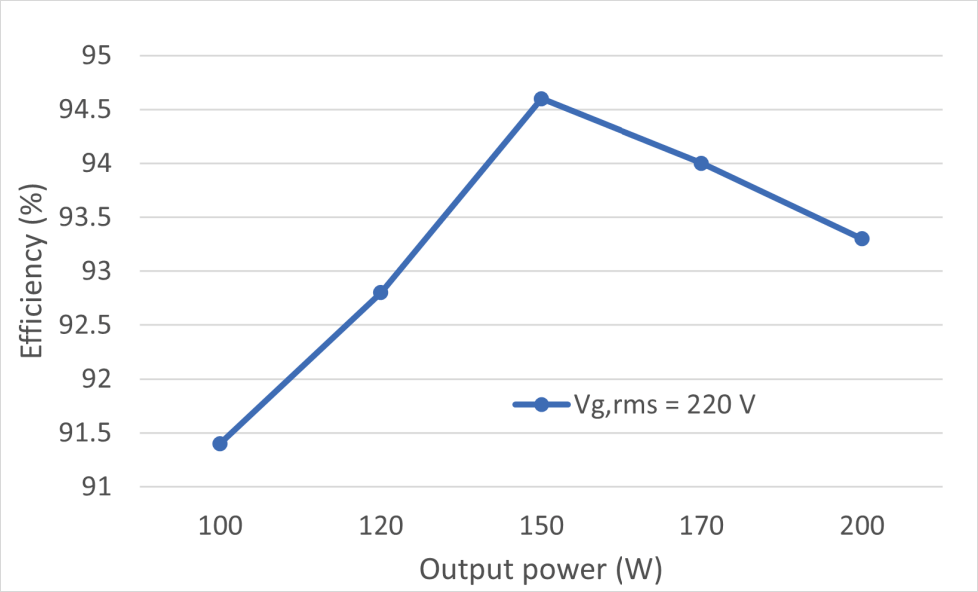


Figure 5.7: Efficiency of the prototype with respect to output power

5.8 Summary

This chapter performs design calculations to obtain the PFC inductance value, and capacitance values. The formula of i_{C2} is also obtained which helps in achieving ZVS more comfortably. In addition, a comprehensive stress analysis is carried out to obtain the maximum current and voltage of every component. This helps in choosing appropriate components for the LED driver that can tolerate the expected voltage and current levels. The loss analysis is also provided that calculates the expected loss of MOSFETs and diodes. Based on the calculated losses, the lowest efficiency of the converter at full-load is then calculated. At the end, by using a Tektronix 5 series Mixed Signal Oscilloscope model MS058, the efficiency of the experimental prototype at different operating points is measured and presented.

Chapter 6

Summary and Future Work

6.1 Summary of Contributions

In this thesis, the analysis and design of a 200 W streetlighting LED driver are carried out, and different challenges associated with streetlighting LED drivers are addressed. Furthermore, the simulation and experimental results of the design are provided. The main contributions of the proposed LED driver are listed below:

1. An integrated single-stage LED driver is proposed which is suitable for input voltage range of $(185 - 265)$ V_{rms} with low THD, high PF, low output ripples, and limited dc bus voltage that lowers the voltage stress of MOSFETs.

2. A novel buck-boost typed PFC circuit is proposed in which the transformer of PFC circuit acts like the buck-boost switch, and the problem associated with other DCM buck-boost PFC circuits is resolved.

3. The control system of the proposed converter is designed such that low frequency ripples are removed from the output. As a result, electrolytic capacitors are eliminated which improves the lifespan of the LED driver.

4. The inductor and transformer of PFC circuit are integrated on the same core where the inductor winding is wrapped around the outer legs to achieve high efficiency.

6.2 Suggested Improvements

The proposed LED driver can be still improved in some areas that are presented as follows:

1. The actual PF and THD of the experimental prototype can pass the required standards, but they can be furthered improved. The leakage inductance of PFC transformer is largely responsible for not achieving the best PF and THD as not only does it affect the falling time of input current in each switching period, but it also resonates with the parasitic capacitance of D_a that appears on input current. The problem can be addressed by interleaving the transformer windings more effectively to decrease the leakage inductance, and by designing an optimized snubber circuit for the diode.

2. Because of high frequency content of diode currents, and due to using SiC MOSFETs with low rising and falling times, Electro Magnetic Interference (EMI) noises exist in the circuit that must be filtered to comply with EMC requirements. Therefore, designing an appropriate EMI filter is recommended.

3. In the proposed LED driver, PFM is used to regulate the output. However, variable switching frequency operation makes it challenging to design the EMI filter. As an improvement, the Pulse Width Modulation (PWM) technique can be used to regulate the output by keeping the switching frequency constant.

4. It was shown in "Stress Analysis" section of Chapter 5 that the voltage stress of input diode bridge, and D_a is nearly twice the dc bus voltage. Other alternative topologies or circuit modifications can be derived to reduce this voltage stress.

5. The obtained efficiency of the converter is relatively high. However, a bridgeless topology can improve the efficiency by removing some of the input diodes.

6. The power density of the converter is relatively high. However, further improvement is possible by increasing the switching frequency. This is less challenging for the proposed circuit because owing to the current of the secondary winding of PFC transformer, ZVS is achieved more comfortably in the proposed converter than in a regular LLC resonant converter.

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Appendix A

Current Balancing

Since the output light of an LED is directly related to its forward current, the luminance uniformity of an LED fixture with several LEDs is guaranteed only if the LEDs have the same amount of current. To have a high standard lighting environment, equalizing or balancing the current of different LEDs is crucial for streetlighting fixtures. Current balancing is guaranteed for a string of LEDs connected in series. However, connecting LEDs in series, especially for high power streetlighting applications where hundreds of LEDs are required, increases the output voltage of driver. This will cause the LED driver not to comply with required safety standards. In addition, with this arrangement, if one of the LEDs breaks, the whole LED string turns OFF which this causes a significant reduction in reliability, and lifetime of the fixture.

Multiple LED strings connected in parallel with an acceptable output voltage is the best possible configuration for LED streetlighting fixtures. Due to the manufacturing process of LEDs, the forward voltage, and equivalent series impedance of LEDs are different that results in current imbalance even if the terminal voltage of each LED string is the same. This leads to unacceptable inconsistency in output light, as well as reduction in life expectancy of LEDs. Therefore, using a current balancing scheme is essential.

Different methods have been proposed in literature for current balancing among which devising a scheme based on the charge balance property of capacitors yields the best result because capacitive configurations are almost lossless, and not very complicated.

A.1 The Adopted Current Balancing Scheme

The current balancing scheme of the proposed LED driver is adopted from [63] that has two LED strings. Therefore, its current balancing scheme is extended to accommodate a four-output LED driver as depicted in Fig. A.1.

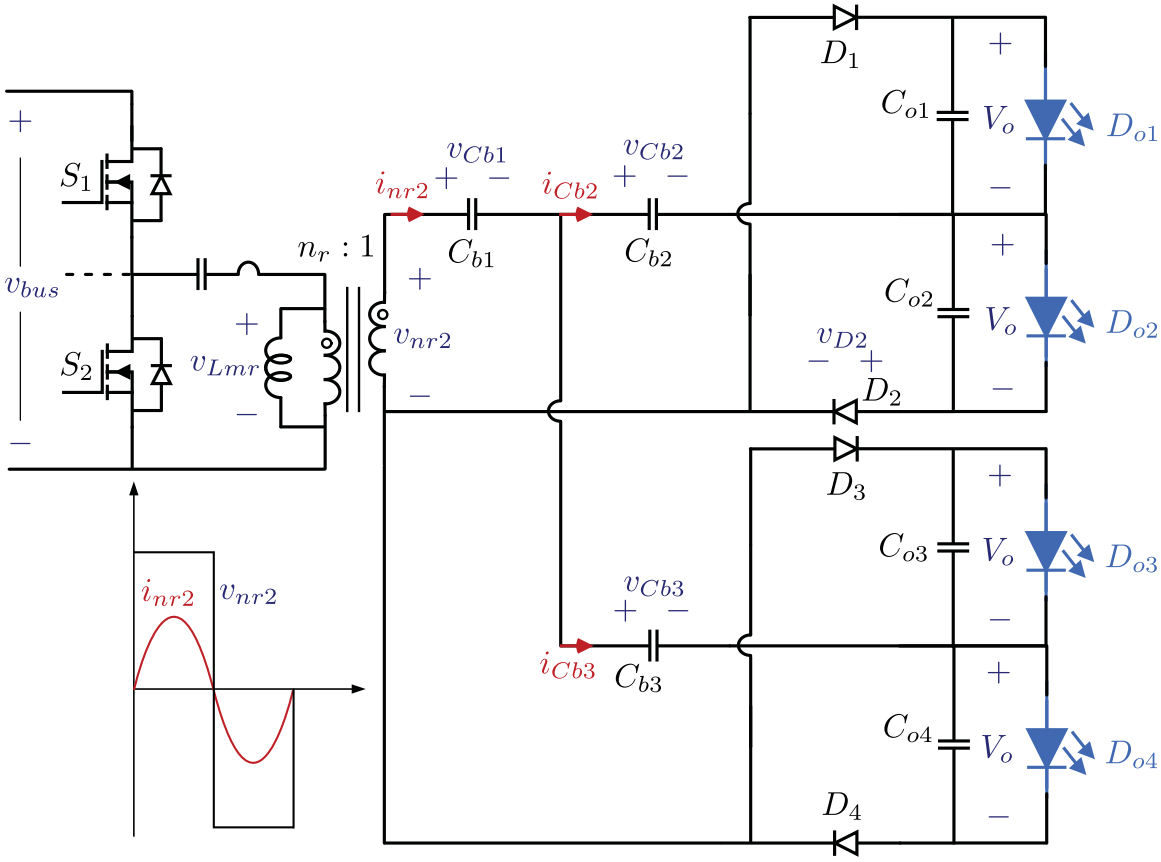

Figure A.1: The adopted current balancing circuit [63]

Four output rectifying diodes, and three balancing capacitors are used in this structure with no additional inductors. Due to the charge-balance property of balancing capacitors (C_{b1}, C_{b2}, and C_{b3}), the complete current balancing of LED pair D_{o1} and D_{o2}, as well as LED pair D_{o3} and D_{o4} is achieved. This technique does not guarantee the complete current balancing between either of the LEDs at top (D_{o1} or D_{o2}) with the LEDs at bottom (D_{o3} or D_{o4}). However, their current imbalance is negligible.

A.2 Modes of Operation

(For this part, and for the waveforms depicted on Fig. A.1, one of the operating points in which the LLC resonant converter operates in above resonance ($f_{sw} > f_r$) is considered)

Depending on the ON/OFF state of MOSFETs, two operating modes are conceivable.

A.2.1 Mode I

When S_1 is ON, and according to (3.7), the secondary voltage of LLC transformer is determined as follows:

$$v_{Lmr}(t) = V_{Lmr}^{+} = n_r V_o \implies v_{nr2}(t) = \frac{1}{n_r} \times n_r V_o = V_o. \tag{A.1}$$

Since $v_{nr2}(t)$ is positive, D_2 and D_4 conduct, whereas D_1 and D_3 are OFF.

A.2.2 Mode II

When S_2 is ON, the secondary voltage of LLC transformer is determined as follows:

$$v_{Lmr}(t) = -n_r V_o \implies v_{nr2}(t) = \frac{1}{n_r} \times (-n_r V_o) = -V_o. \tag{A.2}$$

Since $v_{nr2}(t)$ is negative, D_1 and D_3 conduct, whereas D_2 and D_4 are OFF.

A.3 Voltage of Balancing Capacitors

For this design, equal capacitances ($C_{b1} = C_{b2} = C_{b3}$) is considered. By writing a KCL, and considering the symmetry of circuit, it can be written that:

$$i_{nr2}(t) = i_{Cb2}(t) + i_{Cb3}(t) \quad \overset{C_{b1}=C_{b2}=C_{b3}}{\Longrightarrow} v_{Cb1}(t) = 2v_{Cb2}(t) = 2v_{Cb3}(t). \tag{A.3}$$

In addition, a KVL can be written as follows:

$$v_{nr2}(t) - v_{Cb1}(t) - v_{Cb2}(t) - V_o - v_{D2}(t) = 0, \tag{A.4}$$

where $v_{nr2}(t)$ is a square wave signal with the positive value of V_o during the first half of switching period, and the negative value of $-V_o$ during the second half, and $v_{D2}(t)$ is a square wave signal with zero value at the first half of switching period, and the negative value of $-2V_o$ during the second half.

By writing the Fourier series of v_{nr2}, and v_{D2} which for simplicity only their first terms are considered, and according to (A.3), and (A.4), the voltage of balancing capacitors is obtained as follows:

$$\frac{4V_o}{\pi}\sin\omega_s t - 3v_{Cb2}(t) - V_o - (\frac{4V_o}{\pi}\sin\omega_s t - V_o) = 0$$

$$\implies v_{Cb2}(t) = v_{Cb3}(t) = v_{Cb1}(t) = 0. \tag{A.5}$$

In practice, the non idealities of diodes, leakage inductance of secondary winding, and resistance of PCB traces result in a non-zero, yet small ac voltage across the three capacitors.

A.4 Simulation and Experimental Results

Fig. A.2 shows the simulation result of the current balancing circuit in which a moderate difference is considered in the characteristics of four LEDs. As one can see, the current balancing between the two LEDs at top, and the two LEDs at bottom is obtained. However, current balancing is not achieved between any of the LEDs at top with any of the LEDs at bottom, but the amount of their current imbalance is negligible.

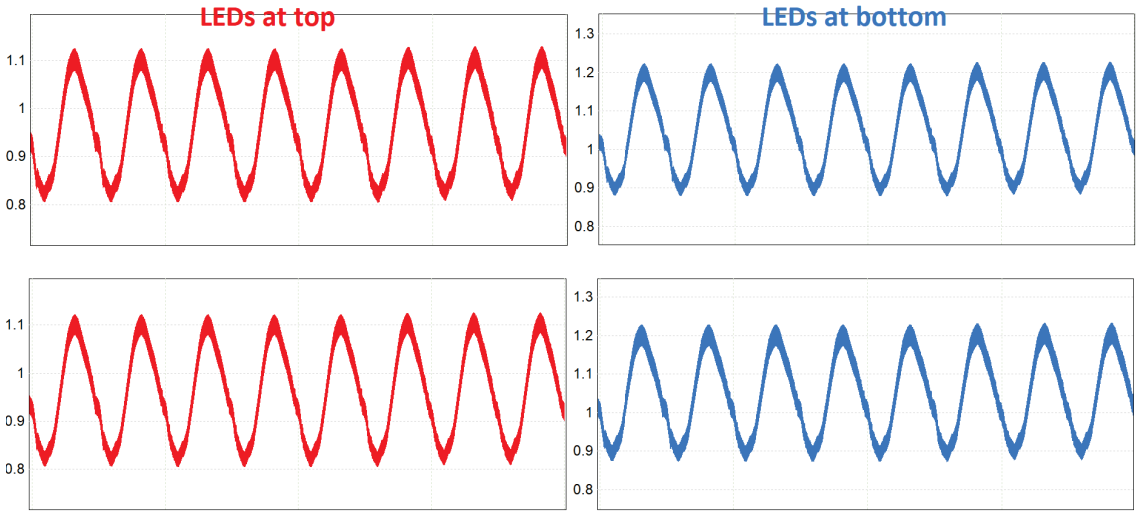

Figure A.2: Simulation result showing the output currents

The output currents of the experimental prototype are shown in Fig.A.3 where the average of each output current is measured. The current balancing between the four outputs is satisfactory.

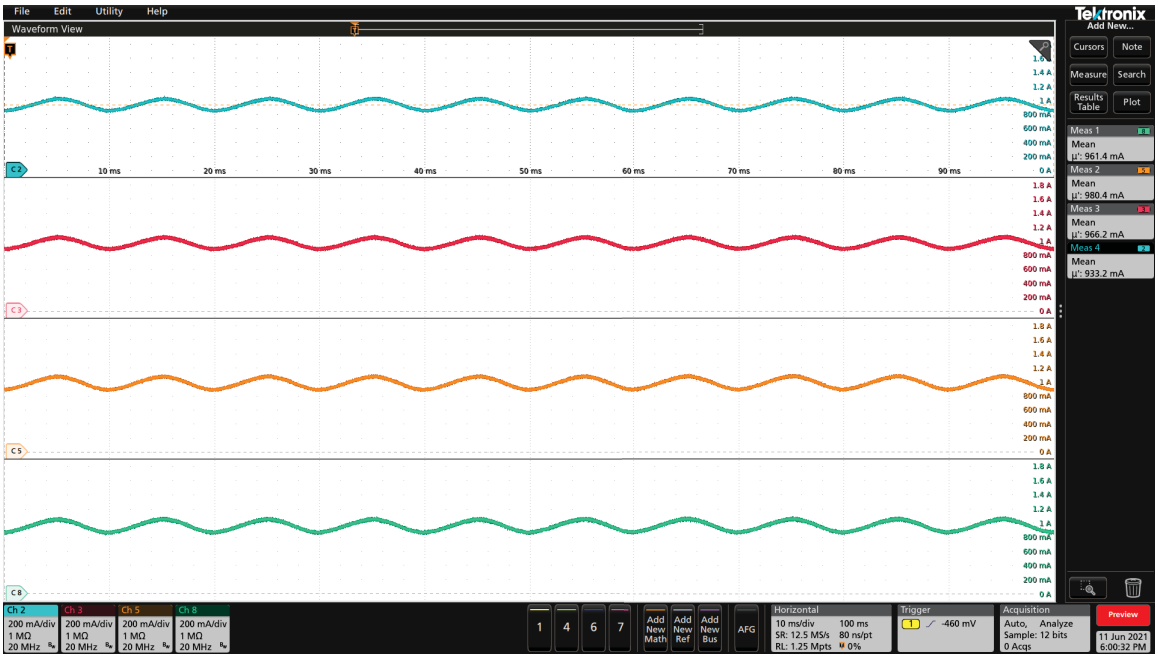

Figure A.3: Experimental result showing the output currents

A.5 Summary

This chapter gives insight into the importance of current balancing in LED drivers, and why it is essential to devise a current balancing scheme for multiple LED strings connected in parallel. The adopted current balancing scheme is introduced, and the modes of operation are discussed. Finally, simulation and experimental results of the four outputs are provided showing an acceptable and below 10% difference between the four output currents.