Real-Time HIL Emulation of Faulted Electric Machines Based on Nonlinear MEC Model

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***Abstract*—In electric machine drive systems, hardware-in-the-loop (HIL) emulation provides accurate testing of actual control system prototypes and protection devices interfaced with the electric machine model on a real-time simulator in a non-destructive environment particularly when faults are studied. A compromise between the model accuracy and computational burden makes the magnetic equivalent circuit (MEC) model ideal for real-time simulation of electric machines. However, satisfying the timing constraints of real-time simulation to accommodate internal machine faults is still challenging due to the nonlinearity and rotation of electric machines. In this paper, the transmission line modeling (TLM) method is utilized to keep the MEC coefficient matrix unchanged during nonlinear iterations. Afterward, for the first time, the entire potential of the TLM method for pre-calculation is exploited by proposing an efficient matrix re-ordering combined with the left-looking Gilbert–Peierls algorithm to minimize the computational burden of the sparse MEC matrix LU decomposition required in each time-step due to rotation. Furthermore, the massive hardware architecture of the field programmable gate array is used as the platform for implementation to fully exploit parallelism. With the proposed MEC-based real-time TLM method, the minimum time-step as low as 500 μs can be achieved and the results validation with two-dimensional finite element model (FEM) of the commercial Jmag-Designer software shows the accuracy and efficiency of the proposed methodology.**

***Index Terms*—Fault analysis, field programmable gate array, hardware-in-the-loop emulation, induction motor, magnetic equivalent circuit, nonlinearity, parallel processing, real-time systems, transmission line modeling.**

NOMENCLATURE

Z_0/Y_0	TLM characteristic impedance/admittance
N_{ss}	Number of stator slots
N_{rs}	Number of rotor slots
μ	Magnetic permeability
μ_0	Air permeability
μ_{tlm}	TLM permeability
P	Permeance
L	Length of the permeance elemental area
S	Area of the permeance elemental area
A	Magnetic vector potential
N	Number of turns
i	Current
λ	Flux linkage
W	Winding function
L	Inductance
T_e	Electromagnetic torque
T_L	Load torque
J	Inertia
B	Friction coefficient
ω	Angular speed
P	Number of poles

superscripts/subscripts

sb	Stator base
st	Stator tooth
rb	Rotor base
rt	Rotor tooth
$stst$	Stator tooth to stator tooth
$rtrt$	Rotor tooth to rotor tooth
$strt$	Stator tooth to rotor tooth
n	Time-step number
k	TLM iteration number
$inc.$	Incident wave
$ref.$	Reflected wave
l	Leakage
r	Rotor
b	Rotor bar
be	Rotor back end ring
fe	Rotor front end ring

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I. INTRODUCTION

FEILD programmable gate array (FPGA) based hardware-in-the-loop (HIL) emulation provides an accurate testing platform by real-time data transfer of the actual device under test, including control system prototypes and protection devices, interfaced with the interacted systems, involving electric machines, on real-time simulator [1]–[4]. In the domain of FPGA-based real-time simulation of electric machine drives, numerous studies have been conducted with lumped q-d vector model [5], [6]. In [7], a lumped parameter coupled circuit model in phase domain is used for single and three phase fault analysis. However, internal machine faults were not investigated. The proposed model struggles with considering saturation, exact winding function, and defining an effective air gap, which is dependent on experimental measurement for calculation of

lumped inductances in offline. In some other studies, the nonlinearity of the iron core is taken into account in the lumped q-d vector model through FEM-based off-line pre-calculation of nonlinear inductance matrix as a function of rotor position and stator currents [8], [9]. The pre-calculated data are stored in a look-up table and are used during lumped q-d based real-time simulation depending on the operating condition. However, creating the look-up tables to cover a dense grid of the variables range is very time consuming, memory inefficient, and causes incorrect transient behavior due to jump discontinuities. With the lumped q-d model, time-steps in the range of hundreds of nanoseconds to a few microseconds have been achieved. Since the HIL platform is safe and non-destructive, the scenario is particularly beneficial when electric machine faults are studied on the real-time simulator. The lumped q-d model is unable to accommodate electric machine internal faults. Thus, physics-based models, i.e., magnetic equivalent circuit (MEC) and finite element method (FEM) models, should be employed. FPGA-based hardware acceleration of FEM computation for a linear induction motor was investigated in [10], where an acceleration rate of 9.7 is achieved in comparison with commercial FEM software on CPU. In [11], for the first time, a 2 ms time-step real-time TLM (RT-TLM) is proposed for FEM computation of one pole pitch of a linear induction motor on FPGA employing finite pre-calculation of LU decompositions. The computational intensity of FEM makes it inappropriate for real-time simulation of faults since the entire electric machine domain needs to be modeled [12]. The ability of magnetic equivalent circuit (MEC) to consider magnetic nonlinearity of the iron core, spatial harmonics and machine faults with medium computational burden make it promising for real-time simulation [13]–[21].

The solution of MEC system of nonlinear equations requires LU decomposition of the entire coefficient matrix in each Newton-Raphson (N-R) iteration and time-step due to the nonlinearity of iron core and rotation, respectively. Furthermore, fault studies require high bandwidth simulation of a non-periodic boundary problem, which challenges the timing constraints of the real-time simulation. The transmission line modeling (TLM) method decouples nonlinear elements from a coupled linear network using lossless time-delayed transmission lines to keep the coefficient matrix unchanged during nonlinear iterations [22], [23].

The MEC model has the lowest computational burden with the ability of electric machine internal fault modeling. In [24], a new transmission line modeling (TLM) algorithm for the MEC-based solution of induction machines is proposed to decouple the nonlinear magnetic equations. A look-up table is used to solve the decoupled nonlinear elements, where an acceleration rate of 8.7 times is achieved in comparison to the conventional MEC method. Later in [25], MEC-based real-time simulation of one pole pitch of the induction machine with the time-step of 150 μs has achieved on multi-core CPU-based real-time simulator. In [26], the FPGA-based real-time simulation of a switched reluctance motor (SRM) using the MEC model is performed on FPGA. However, due to the salient magnetic structure of this type of machine, the MEC system of equations size is small and cannot be generalized for other electric machines including induction motors. In [27], the MEC model of an induction motor is used for real-time simulation on FPGA using massively paralleled and deeply pipelined Gauss-Jordan elimination solver and the minimum time-step of 400 μs is achieved. However, the proposed hardware prototype is not able to accommodate internal machine faults since the study domain is reduced to one pole pitch of an induction motor under anti-periodicity boundary condition.

In this paper, for the first time, real-time HIL emulation of faulted electric machines on FPGA is proposed, which further struggles with larger problem size of the entire study domain due to asymmetric properties of faults, and smaller time-step requirement to capture higher order of harmonics in the stator winding current under fault condition. To overcome the computational intensity, the TLM method is utilized as the basis to keep the MEC coefficient matrix unchanged during the nonlinear iterations, and two novel ideas are proposed for the real-time TLM (RT-TLM) method as follows: (1) A special combination of matrix re-ordering and left-looking Gilbert-Peierls algorithm for sparse LU decomposition to keep the majority of the decomposed matrix unchanged through the entire simulation, which minimizes the real-time simulation computational burden, and (2) FPGA hardware implementation is used to fully exploit the parallelism of the TLM algorithm and the reduced-order sparse solver.

The main purpose in HIL emulation of an electric machine drive system is for testing actual control and protection devices interfaced with the electric machine model on the real-time simulator. Thus, this work focuses on development of real-time electric machine model to be utilized for HIL testing. The paper is organized to first present the MEC-based TLM formulation and the proposed RT-TLM ideas in Section II. The massively parallel and deeply pipelined hardware design architecture and implementation on Xilinx Virtex UltraScale+ XCVU9P FPGA board are discussed in Section III. Then, the real-time simulation results of the transient start-up and steady-state under healthy and various kind of faulty conditions are presented, including winding inter-turn faults, broken rotor bar, broken end ring, as well as power system disturbances including voltage unbalance and power supply harmonics followed by 2-D FEM results validation in Section IV. Finally, in Section V the conclusions are provided.

II. Novel MEC-Based RT-TLM Emulation

A. Transmission Line Modeling (TLM) Method

TLM is a discretization method in time-domain, which proposes decoupling of nonlinear and reactive elements of an electrical circuit through lossless and time-delayed transmission lines with arbitrarily chosen characteristic impedance [22], [23]. Based on the TLM method, a nonlinear network is made equivalent to a linear network and decoupled nonlinear and reactive elements. The TLM procedure is based on traveling incident waves through the transmission lines and calculating the reflected waves at the linear network (sending end) and the decoupled elements (receiving end) due to mismatch of the traveling wave characteristic impedance. The calculation of the reflected waves at the sending end requires solution of a linear system of equations corresponding to the linear network

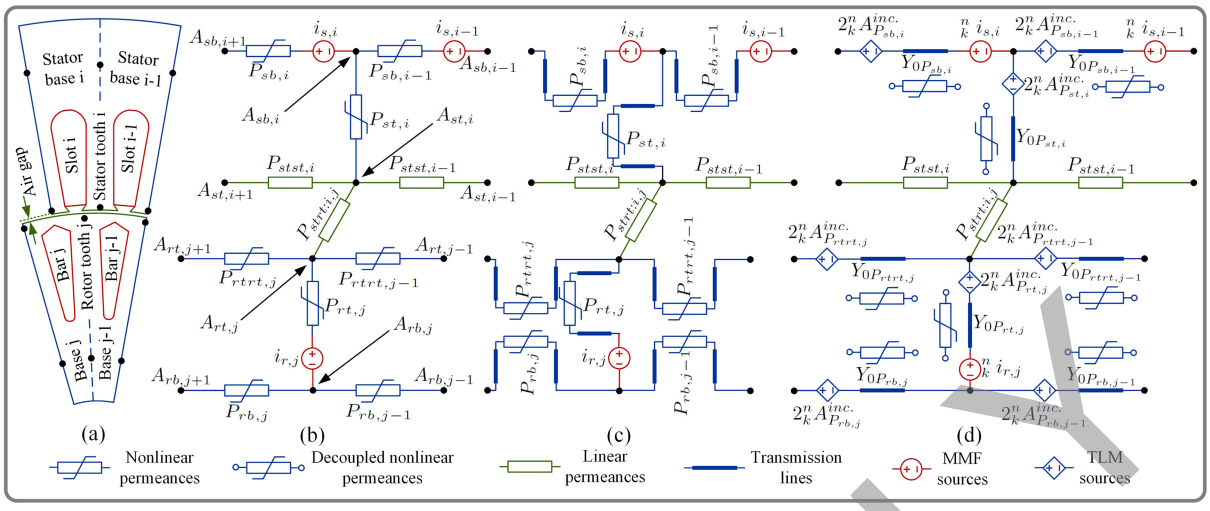


Fig. 1. The TLM application procedure on MEC. (a) One tooth of the stator and rotor of an induction motor. (b) MEC model. (c) Transmission line decoupling. (d) MEC-based TLM network and the decoupled nonlinear permeances.

including transmission lines. At the receiving end, the calculation of the reflected waves requires solution of decoupled individual nonlinear elements, where parallelism can be exploited. In comparison with the conventional method, where a linear system of equations needs to be solved in every nonlinear iteration and time-step, the TLM method requires only one LU decomposition per time-step followed by a number of forward elimination and backward substitutions equal to the number of TLM iterations.

B. TLM-Based MEC Modeling

Assuming an induction machine with N_{ss} number of stator slots and N_{rs} number of rotor slots, the ith stator tooth and the j*th* rotor tooth followed by their MEC models are shown in Fig. 1 (a) and (b), respectively. Due to the dependence of μ on magnetic flux density, the permeances of stator base (P_{sb}), stator tooth (P_{st}), rotor tooth-tooth (P_{rtrt}), rotor tooth (P_{rt}) and rotor base (P_{rb}) are nonlinear. However, the permeances of stator-tooth-to-rotor-tooth (P_{strt}) and the stator tooth-tooth (P_{stst}) are considered linear due to the dominance of constant permeability of air (μ_0).

Conventionally, MEC model requires the solution of a system of equations in every iteration and time-step due to the nonlinearity of permeances and rotation, respectively. The TLM method uses lossless time-delayed transmission lines to decouple nonlinear permeances from a coupled linear network as shown in Fig. 1 (c) to keep the MEC matrix unchanged within each time-step. The corresponding transmission line characteristic admittances (Y_{0P}) can be determined by substituting the nonlinear permeability of the permeances (μ) with arbitrarily chosen permeability (μ_{tlm}) as follows:

$$P = \left(\int_0^L \frac{dl}{\mu S(l)}\right)^{-1}, Y_{0P} = \left(\int_0^L \frac{dl}{\mu_{tlm} S(l)}\right)^{-1}. \quad (1)$$

The nonlinear permeances are substituted by their Thevenin equivalent circuits of the transmission lines shown in Fig. 1(d) [24].

The TLM iterative procedure begins with traveling incident potentials through transmission lines and calculation of the reflected potentials from the linear network (sending end) using the nodal magnetic vector potentials. Considering the k*th* TLM iteration of the k*th* simulation time-step, the magnetic vector potentials (${}^n_k\mathbf{A}$) can be found by the solution of MEC-based TLM linear system of equations.

In Fig. 1(d), the Kirchhoff's current law (KCL) for the stator base and tooth nodes are respectively as follows:

$$\begin{aligned} &Y_{0P_{st,i}}({}^n_k A_{sb,i} - {}^n_k A_{st,i} - 2\times {}^n_k A^{inc.}_{P_{st,i}}) + Y_{0P_{sb,i-1}}({}^n_k A_{sb,i} \\ &- {}^n_k A_{sb,i-1} - \mathbf{N}^T_{qd0,i-1}\,{}^n_k\mathbf{i}_{qd0} - 2\times {}^n_k A^{inc.}_{P_{sb,i-1}}) + Y_{0P_{sb,i}} \\ &({}^n_k A_{sb,i} - {}^n_k A_{sb,i+1} + \mathbf{N}^T_{qd0,i}\,{}^n_k\mathbf{i}_{qd0} + 2\times {}^n_k A^{inc.}_{P_{sb,i}}) = 0, \quad (2) \\ &Y_{0P_{st,i}}({}^n_k A_{st,i} - {}^n_k A_{sb,i} + 2\times {}^n_k A^{inc.}_{P_{st,i}}) + P_{stst,i-1} \\ &({}^n_k A_{st,i} - {}^n_k A_{st,i-1}) + P_{stst,i}({}^n_k A_{st,i} - {}^n_k A_{st,i+1}) \\ &+ \sum_{j=1}^{N_{rs}} P_{strt:i,j}({}^n_k A_{st,i} - {}^n_k A_{rt,j}) = 0, \quad (3) \end{aligned}$$

where ${}^n_k A^{inc.}_{P_{sb,i}}$ and ${}^n_k A^{inc.}_{P_{st,i}}$ are the incident magnetic vector potentials, while ${}^n_k A_{sb,i}$ and ${}^n_k A_{st,i}$ are the nodal magnetic vector potentials of the ith stator base and tooth, respectively. The ${}^n_k i_{s,i} = \mathbf{N}^T_{qd0,i}\,{}^n_k\mathbf{i}_{qd0}$ represents the stator magnetic motive force (MMF) of the ith stator slot, where $\mathbf{N}^T_{qd0,i}$ is the ith slot turn function and ${}^n_k\mathbf{i}_{qd0}$ is the stator winding current in $qd0$ frame.

Similarly, for the rotor tooth and base nodes, the KCL can be presented as:

$$\begin{aligned} &Y_{0P_{rt,j}}({}^n_k A_{rt,j} - {}^n_k A_{rb,j} - {}^n_k i_{r,j} - 2\times {}^n_k A^{inc.}_{P_{rt,j}}) + Y_{0P_{rtrt,j-1}} \\ &({}^n_k A_{rt,j} - {}^n_k A_{rt,j-1} - 2\times {}^n_k A^{inc.}_{P_{rtrt,j-1}}) + Y_{0P_{rtrt,j}}({}^n_k A_{rt,j} - \\ &{}^n_k A_{rt,j+1} + 2\times {}^n_k A^{inc.}_{P_{rtrt,j}}) + \sum_{i=1}^{N_{ss}} P_{strt}({}^n_k A_{rt,j} - {}^n_k A_{st,i}) = 0, \\ &\quad (4) \end{aligned}$$

$$Y_{0P_{rt,j}}({}^n_k A_{rb,j} - {}^n_k A_{rt,j} + {}^n_k i_{r,j} + 2 \times {}^n_k A^{inc.}_{P_{rt,j}}) + Y_{0P_{rb,j}}({}^n_k A_{rb,j} - {}^n_k A_{rb,j+1} + 2 \times {}^n_k A^{inc.}_{P_{rb,j}}) + Y_{0P_{rb,j-1}}({}^n_k A_{rb,j} - {}^n_k A_{rb,j-1} - 2 \times {}^n_k A^{inc.}_{P_{rb,j-1}}) = 0, \quad (5)$$

where ${}^n_k i_{r,j}$ is the j*th* rotor bar current of the k*th* TLM iteration of the k*th* simulation time-step.

The stator winding linkage flux ($\boldsymbol{\lambda}_{qd0}$) can be represented in terms of the magnetizing and leakage fluxes as follows:

$$\boldsymbol{\lambda}_{qd0} = \sum_{i=1}^{Nss} \mathbf{W}_{qd0,i} Y_{0P_{st,i}}({}^n_k A_{st,i} - {}^n_k A_{sb,i} + 2 \times {}^n_k A^{inc.}_{P_{st,j}}) + \mathbf{L}_l {}^n_k \mathbf{i}_{qd0}, \quad (6)$$

where $\mathbf{W}_{qd0,i}$ is the winding function of the *i*th stator slot in $qd0$ frame, and $\mathbf{L}_l$ is the stator winding leakage inductance, both extensively discussed in [17]. The j*th* rotor loop and end ring linkage flux can be represented as:

$$\hat{\lambda}_{r,j} = Y_{0P_{rt,j}}({}^n_k A_{rb,j} - {}^n_k A_{rt,j} + 2 \times {}^n_k A^{inc.}_{P_{rt,j}} + {}^n_k i_{r,j}) - P_{b,j-1} {}^n_k i_{r,j-1} + (P_{b,j} + P_{b,j-1} + P_{fe,j} + P_{be,j}) {}^n_k i_{r,j} - P_{b,j} {}^n_k i_{r,j+1} - \frac{P_{fe,j}}{P_{fe}} \sum_{j_1=1}^{N_{rs}} P_{fe,j_1} {}^n_k i_{r,j_1} \quad (7)$$

where $P_{b,j}$, $P_{fe,j}$ and $P_{be,j}$ are the linear permeances of the rotor bar, front end ring, and back end ring, respectively.

The MEC-based TLM equations of (2)–(7) can be reorganized into a system of equations of ${}^n_k \mathbf{M} {}^n_k \mathbf{x} = {}^n_k \mathbf{b}$, where the MEC matrix ($\mathbf{M}$) is dependent on the transmission line admittances. $\mathbf{M}$, ${}^n_k \mathbf{x}$, and ${}^n_k \mathbf{b}$ are ordered as follows due to an advantage discussed in *Subsection B*.:

$$\begin{pmatrix} \mathbf{M_{sb-sb}} & \mathbf{0} & \mathbf{M}_{sb-si} & \mathbf{0} & \mathbf{M}_{sb-st} & \mathbf{0} \\ \mathbf{0} & \mathbf{M}_{rb-rb} & \mathbf{0} & \mathbf{M}_{rb-ri} & \mathbf{0} & \mathbf{M}_{rb-rt} \\ \mathbf{M}_{s\lambda-sb} & \mathbf{0} & \mathbf{L}_l & \mathbf{0} & \mathbf{M}_{s\lambda-st} & \mathbf{0} \\ \mathbf{0} & \mathbf{M}_{r\lambda-rb} & \mathbf{0} & \mathbf{M}_{r\lambda-ri} & \mathbf{0} & \mathbf{M}_{r\lambda-rt} \\ \mathbf{M}_{st-sb} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{M}_{st-st} & \mathbf{M}_{st-rt} \\ \mathbf{0} & \mathbf{M}_{rt-rb} & \mathbf{0} & \mathbf{M}_{rt-ri} & \mathbf{M}_{rt-st} & \mathbf{M}_{rt-rt} \end{pmatrix} \quad (8)$$

$${}^n_k \mathbf{x} = \begin{pmatrix} {}^n_k \mathbf{A}_{sb} & {}^n_k \mathbf{A}_{rb} & {}^n_k \mathbf{i}_{qd0} & {}^n_k \mathbf{i}_r & {}^n_k \mathbf{A}_{st} & {}^n_k \mathbf{A}_{rt} \end{pmatrix}^T \quad (9)$$

$${}^n_k \mathbf{b} = \begin{pmatrix} {}^n_k \mathbf{b}_{sb} & {}^n_k \mathbf{b}_{rb} & \lambda_{qd0} + {}^n_k \mathbf{b}_{s\lambda} & \hat{\lambda}_r + {}^n_k \mathbf{b}_{r\lambda} & {}^n_k \mathbf{b}_{st} & {}^n_k \mathbf{b}_{rt} \end{pmatrix}^T \quad (10)$$

where ${}^n_k \mathbf{b}_{sb}$, ${}^n_k \mathbf{b}_{rb}$, ${}^n_k \mathbf{b}_{s\lambda}$, ${}^n_k \mathbf{b}_{r\lambda}$, ${}^n_k \mathbf{b}_{st}$ and ${}^n_k \mathbf{b}_{rt}$ are the TLM sources dependent on the incident potentials of the sending end that change in each TLM iteration. Since the MEC-based TLM matrix remains unchanged within each time-step, the solution requires only one LU decomposition per time-step. Meanwhile, the ${}^n_k \mathbf{b}$ matrix changes, where only sparse forward elimination and backward substitution need to be carried out per TLM iteration.

The TLM procedure continues with the calculation of reflected magnetic vector potentials at the sending end of each permeance (${}^n_k \mathbf{A}^{ref.}_P$) as follows:

$${}^n_k \mathbf{A}^{ref.}_P = {}^n_k \mathbf{A}_P - {}^n_k \mathbf{A}^{inc.}_P, \quad (11)$$

where ${}^n_k \mathbf{A}_P$ is a vector of the potential difference across each permeance (P). The reflected potentials of the sending end travel through the transmission lines and become the incident potentials of the decoupled nonlinear permeances (receiving end) without any change since the transmission lines are lossless. The mismatch of the transmission line admittances and the nonlinear permeances results in reflecting potentials at the receiving end, which travel toward the sending end and become the next incident potentials of the sending end and can be obtained by nonlinear solution of the decoupled nonlinear permeances as follows:

$$Y_{0P}({}^n_k A^{ref.}_P - {}^n_{k+1} A^{inc.}_P) = P({}^n_k A_P)({}^n_k A^{ref.}_P + {}^n_{k+1} A^{inc.}_P), \quad (12)$$

where $P({}^n_k A_P)$ represents the magnetic permeance as a function of magnetic vector potential difference across each nonlinear permeance.

As the N-R solution of (12) converges for all nonlinear permeances, the incident magnetic vector potentials at the sending end of the transmission lines unconditionally converge and the output variables including stator and rotor currents are obtained.

The time derivative of the state variables, including the stator flux ($\boldsymbol{\lambda}_{qd0}$), the rotor linkage flux of the j*th* rotor loop ($\lambda_{r,j}$), and the front end ring linkage flux (λ_{fe}) can be calculated from the electrical circuit of the stator and rotor, respectively as follows:

$$\frac{d}{dt}\boldsymbol{\lambda}_{qd0} = \mathbf{v}_{qd0} - r_s \mathbf{i}_{qd0}, \frac{d}{dt}\lambda_{fe} = -\sum_{j=1}^{N_{rs}} r_{fe,j}(i_{fe} - i_{r,j})$$

$$\frac{d}{dt}\lambda_{r,j} = -r_{b,j}(i_{r,j} - i_{r,j+1}) - r_{be,j} i_{r,j} - r_{b,j-1}(i_{r,j} - i_{r,j-1}) - r_{fe,j}(i_{r,j} - i_{fe}), \quad (13)$$

where $\mathbf{v}_{qd0}$ and r_s are the stator voltage and winding resistance. $r_{b,j}$, $r_{be,j}$, and $r_{fe,j}$ are the bar, back end ring and front end ring of the j*th* rotor loop, respectively. The time-stepping procedure continues to the next time-step with forward Euler discretization of (13).

The rotational speed can be found through the equation of motion as follows:

$$T_e - T_L = J\dot{\omega} + B\omega, \quad (14)$$

where

$$T_e = \frac{P}{2}(\lambda_d i_q - \lambda_q i_d). \quad (15)$$

C. Matrix Re-Ordering, Partially Pre-Calculated LU Decomposition and Reduced Order Sparse Solver

Conventional randomly organized MEC-based TLM system of equations requires one LU decomposition of the MEC matrix with the size of $2N_{ss} + 3N_{rs} + 3$ per time-step. However, only the $\mathbf{M}_{st-rt}$, $\mathbf{M}_{rt-st}$, $\mathbf{M}_{st-st}$ and $\mathbf{M}_{rt-rt}$ sub-matrices change during simulation due to rotation through the change of $Y_{0P_{strt,j}}$. The idea behind ordering the MEC-based TLM system

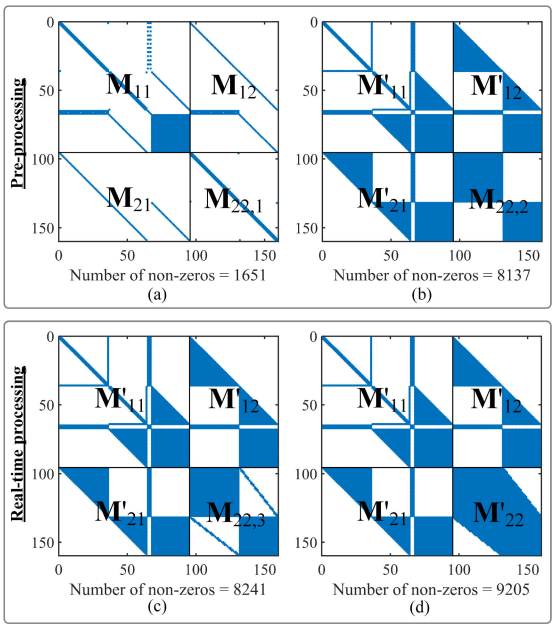


Fig. 2. Proposed RT-TLM MEC matrix LU decomposition procedure.

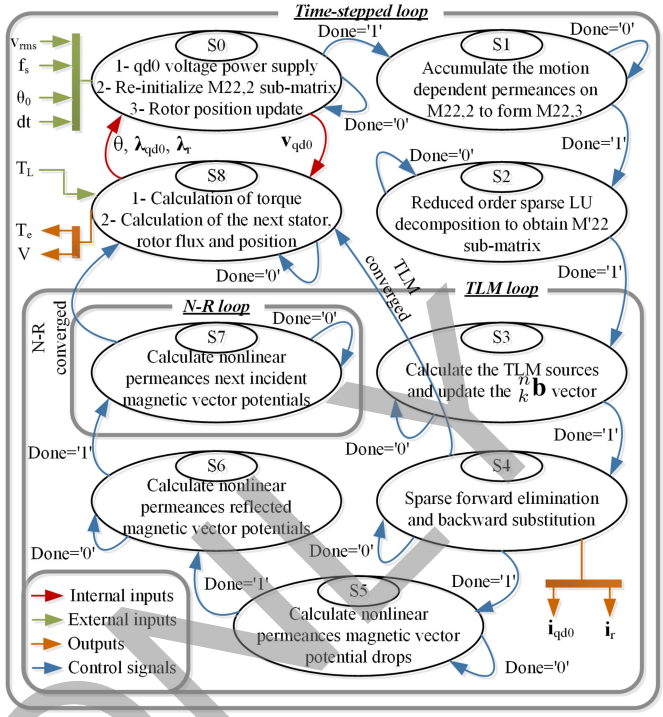


Fig. 3. Proposed MEC-based RT-TLM FPGA implementation state diagram.

of equations is shown in (8) to keep the majority of the matrix unchanged during rotation. In column by column approach of the left-looking Gilbert-Peierls algorithm for sparse LU decomposition, each element $M'(r_i, c_i)$ on the decomposed matrix is only dependent on the already computed elements in the decomposed sub-matrix of $\mathbf{M}'(1:r_i, 1:c_i)$, where r_i and c_i are the row and column indices respectively. Taking the advantage of the algorithm, the LU decomposition of the majority of the matrix remains unchanged during the time-stepped procedure and make it amenable for partial pre-calculation to satisfy the real-time simulation timing constraints.

Fig. 2 shows the non-zero pattern of the MEC coefficient matrix (M) during LU decomposition procedure broken into the two stages of pre-processing and real-time processing. The re-ordered non-zero pattern of matrix $\mathbf{M}$ is shown in Fig. 2(a), where the sub-matrices of $\mathbf{M}_{11}, \mathbf{M}_{12}, \mathbf{M}_{21}$ are fixed through the entire simulation and $\mathbf{M}_{22,1}$ contains the elements of $\mathbf{M}_{st-st}$ and $\mathbf{M}_{rt-rt}$, which are motion independent. Fig. 2(b) shows the non-zero pattern of the partially pre-calculated LU decomposition of matrix $\mathbf{M}$, where the sub-matrices of $\mathbf{M}'_{11}, \mathbf{M}'_{12}, \mathbf{M}'_{21}$ are calculated independent of $\mathbf{M}_{22,1}$ based on the left-looking Gilbert-Peierls algorithm. The pre-calculated sub-matrix of $\mathbf{M}_{22,2}$ is part of the motion dependent sub-matrix of $\mathbf{M}_{22,3}$, which is dependent on already decomposed fixed sub-matrices of $\mathbf{M}'_{11}, \mathbf{M}'_{12}, \mathbf{M}'_{21}$ to maximize the benefit of pre-calculation. In the real-time process of Fig. 2(c), the motion dependent terms of $\mathbf{M}_{st-rt}$, $\mathbf{M}_{rt-st}$, $\mathbf{M}_{st-st}$ and $\mathbf{M}_{rt-rt}$ sub-matrices are accumulated on the pre-calculated $\mathbf{M}_{22,2}$, while the rest of sub-matrices are unchanged. Finally, only the sparse LU decomposition of the $\mathbf{M}_{22,3}$ needs to be carried out to obtain $\mathbf{M}'_{22}$. As a result, the LU decomposition computation burden of a matrix dimension of $2N_{ss} + 3N_{rs} + 3$ is considerably reduced to $N_{ss} + N_{rs}$.

To maximize the solver efficiency in the pre-processing stage, the sparsity pattern of the partially pre-calculated LU decomposition of the MEC-based TLM matrix (Fig. 2(b)) is stored through 6 six auxiliary matrices, where SNZL/SNZU addresses the first nonzero number in each column of the lower/upper triangular, NNZL/NNZU addresses the number of nonzeros in each column of the lower/upper triangular, NZRL/NZRU addresses the nonzeros row index of the lower/upper triangular. Afterward, the six auxiliary matrices are partially updated during the real-time processing of reduced-order sparse LU decomposition to be readily used in the sparse forward elimination and backward substitution.

D. Parallelism Exploitation

One source of parallelism can be found in the column-by-column approach of the left-looking Gilbert-Peierls algorithm for sparse LU decomposition with respect to rows when the column is being updated by fill-ins calculation. Similarly, for the sparse forward elimination and backward substitution, computations are independent with respect to rows.

Owing to the TLM algorithm, another source of parallelism can be found in the nonlinear solution of (12) to find the next incident potentials of the sending end from decoupled nonlinear permeances at the receiving end, which makes the TLM method highly effective on parallel processors rather than sequential ones. FPGAs as the massively paralleled hardware can be utilized to take the benefit of parallel processing to achieve real-time simulation. The parallelism exploitation is extensively discussed in Section III.

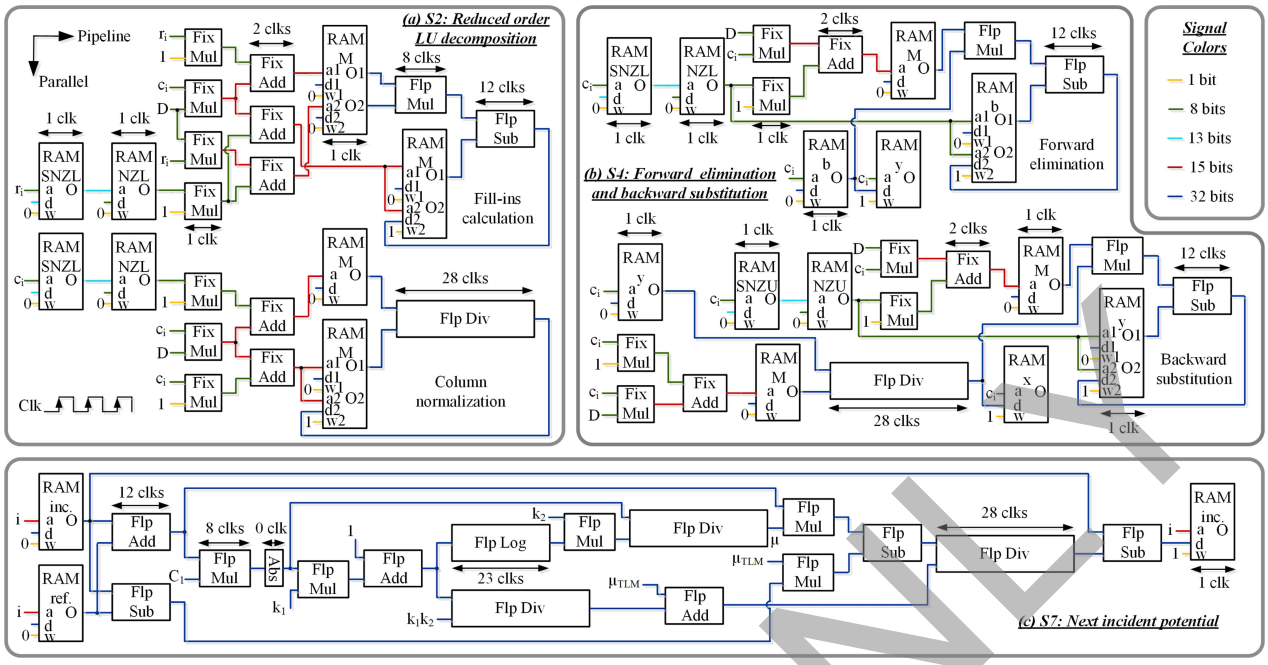


Fig. 4. Massively paralleled and deeply pipelined FPGA hardware architecture. (a) S2: Reduced-order sparse LU decomposition. (b) S4: Sparse forward elimination and backward substitution. (c) S7: Next incident magnetic vector potentials.

III. MEC-Based RT-TLM Hardware Implementation

When the case study machine changes, the pre-processing stage includes defining the machine geometry and material properties, calculation of the electrical parameters, calculation of the linear, TLM and motion independent permeances, the formation of motion independent MEC-based TLM matrix of Fig. 2(a), and finally performing the partial LU decomposition to calculate the matrix of Fig. 2(b). The pre-processing stage can be performed on either the same hardware platform or another CPU-based processor and loaded into the hardware, where both are followed by the same real-time processing stage. The latter strategy is used in this work for simplicity.

The proposed MEC-based RT-TLM methodology state diagram is shown in Fig. 3. The diagram includes three cascaded loops, i.e., the time-step, the TLM, and the N-R loop. It can be seen that with the proposed methodology, taking the advantage of TLM method, the reduced-order sparse LU decomposition in State S2, which has the most computational burden, needs to be carried out only once per time-step. However, the sparse forward elimination and backward substitution in State S4 should be calculated for the TLM number of iterations (N_{TLM}) per time-step. In addition, massive parallelism can be implemented for State S7 as the most inner loop with highest number of iterations ($N_{TLM} \times N_{N-R}$) per time-step, which is the calculation of the next incident magnetic vector potential for decoupled nonlinear permeances of P_{sb}, P_{st}, P_{rtrt}, P_{rt} and P_{rb} through the N-R method. The numbered items in states indicate the component level parallelism, while the state-to-state transition is sequential. The external inputs and outputs are connected to the FPGA board input and output pins (I/O pins) for HIL emulation.

Fig. 4 shows the hardware implementation, where paralleled and pipelined implementation are shown for the most critical designed states of Fig. 3 in terms of execution time per iteration and the number of iterations per time-step, i.e., S2: reduced-order sparse LU decomposition, S4: sparse forward elimination and backward substitution, and S7: calculation of nonlinear permeances next incident magnetic vector potentials. The parallelism in the algorithm-level and operation-level is fully exploited through parallelism and pipelining schemes, where parallelism is simultaneous operations through parallel hardware and pipelining is a chain of independent operations in each clock through the same hardware due to the involvement of RAMs with a limited number of ports (dual port). The data is pipelined from the component input to the output by changing the row and column indices of r_i and c_i, respectively.

The maximum latency is considered for each floating point operation IP core to achieve the highest drivable FPGA clock frequency and total reduction in time-step size, which is 28 clocks for floating point divisions (Flp Div), 23 clocks for the logarithm (Flp Log), 12 clocks for additions/subtractions (Flp Add/Sub), 8 clocks for multiplications (Flp Mul), 2 clocks for 16 bits fixed point addition (Fix Add), 1 clock for 8 bits fixed point multiplication (Fix Mul), and 1 clock for RAMs read/write. The register IP blocks used for signal timing coordination in the pipelining scheme is not shown in the Fig. 4 to improve readability. A compromise between the result accuracy, hardware resource, and achievable frequency make the standard 32-bit single precision number representation for floating point operations ideal.

The hardware is designed by 10,000 lines of handwritten VHDL code in Xilinx Vivado software and the bit stream is generated after the behavioral simulation, synthesis, design

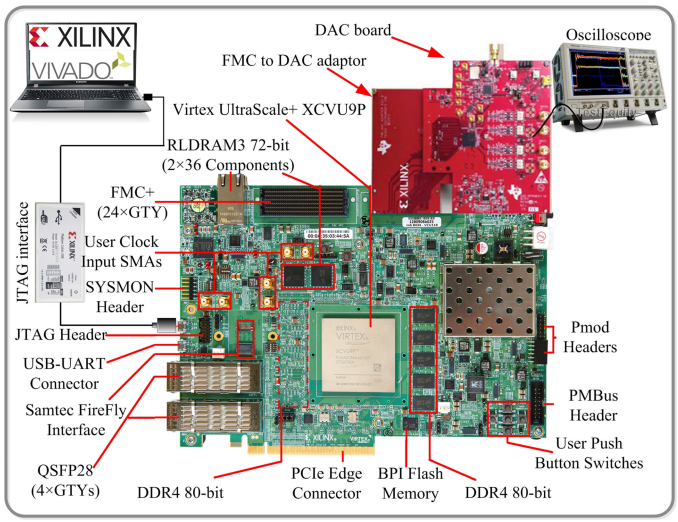


Fig. 5. Real-time simulator hardware set up.

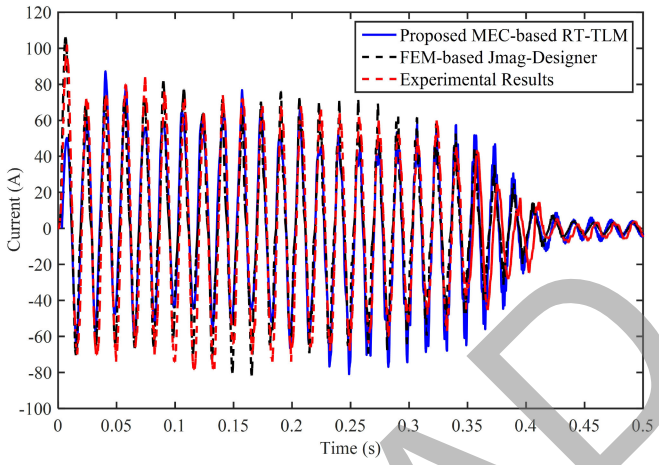


Fig. 6. Stator winding phase current transients during no load start-up.

initialization, optimization and placing the design, respectively. The bit-stream is implemented using JTAG interface on the Xilinx Virtex UltraScale+ XCVU9P FPGA board shown in Fig. 5. The digital outputs of the FPGA board on FMC port are converted to analog using DAC board to be shown on the oscilloscope.

IV. Real-Time Simulation Results

In this section, the fidelity of the proposed MEC-based RT-TLM method under transient start-up and steady-state operation of a wye-connected, 3-hp and 4-pole squirrel-cage induction motor with closed rotor slots is evaluated with the 2-D FEM model on the commercial Jmag-Designer software.

A. Transient Start-Up

Figs. 6 and 7 show the induction motor real-time stator phase current and rotor speed transients validated by FEM and experimental results when the induction motor is directly line-fed from a 208 V three-phase 60 Hz power supply. During the start-up period of t = 0 s to t = 0.4 s, a high (42 A_{rms}) no load

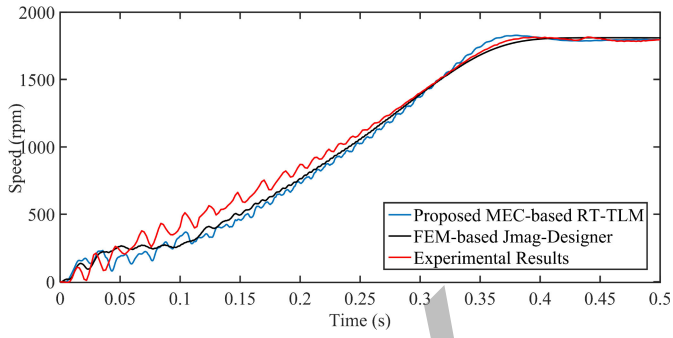


Fig. 7. Rotor speed transients during no load start-up.

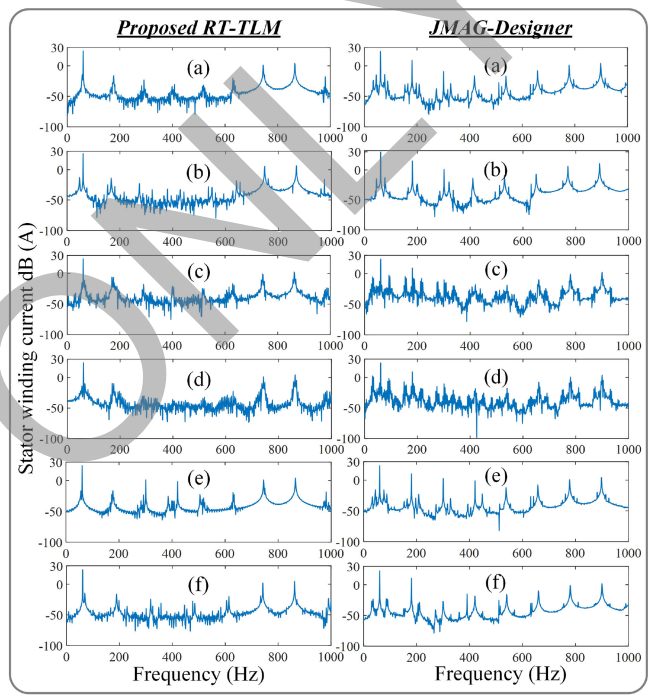


Fig. 8. Steady-state stator current result validation. (a) Case 1: Healthy. (b) Case 2: Stator winding inter-turn short circuit fault. (c) Case 3: Rotor broken bar fault. (d) Case 4: Rotor broken end ring fault. (e) Case 5: Supply 5th and 7th harmonics. (f) Case 6: Unbalanced supply.

inrush current passes through the winding to rotate the rotor to the asynchronous speed of 1792 rpm. Afterward, during the time period of t = 0.4 s to t = 0.5 s, the winding current settles down to the steady-state no load current (2.8 A_{rms}).

It is shown that the time-domain transient current wave shape of the proposed real-time method is in a good agreement with FEM and experimental results.

B. Steady-State

In this part, the induction motor under ideal steady-state operation is compared with abnormal operating conditions under various types of machine faults and supply disturbances, which do not initially and necessarily lead the machine operation to fail. The stator winding current harmonic spectrum is shown for 6 cases in Fig. 8 with a line-fed 208 V three-phase 60 Hz power supply and full load torque of 13 Nm at the speed of 1746 rpm.

1) Case 1. Healthy: In practice, under a healthy condition, the air-gap MMF and flux are not purely sinusoidal and contain spatial harmonics as a result of winding distribution and slotting effect. The harmonic spectrum of the stator winding current using the Discrete Fourier Transform (DFT) of Fig. 8(a) shows those odd harmonic contents.

2) Case 2. Stator Winding Inter-Turn Short Circuit Fault: The 4-pole induction motor is equipped with 2 parallel coils per phase with 40 turns per coil. The inter-turn short-circuit fault is modeled by reducing the number of turns of one coil of *phase-a* to 30. Fig. 8(b) shows the current amplitude of phase-a is increased from 15 A (23 dB) to 20 A (26 dB) as a result of the partial short-circuit of the stator winding. In addition, sub-harmonics, side band harmonics of the main and spatial harmonics are manifested in the winding current DFT as expected due to change of the non-sinusoidal winding distribution function.

3) Case 3. Rotor Broken Bar Fault: The induction motor case study contains 28 rotor bars. The broken rotor bar is modeled through a 10 $m\Omega$ resistance in the electrical circuit instead of the 48.72 $\mu\Omega$ of the healthy bar, since in most cases the bar is cracked rather than entirely disconnected. From Fig. 8(c), it can be seen the fault increases the harmonic spectrum in the current waveform as a result of facing the broken bar to the stator winding MMF.

4) Case 4. Rotor Broken End Ring Fault: Similar to the broken bar, the cracked end ring is modeled by substituting a 100 $\mu\Omega$ resistance instead of the healthy end ring resistance of 1.38 $\mu\Omega$. The broken end ring interferes with the rotor bar current flow, and for the same reason as the broken bar, it results in increasing the harmonic content as shown in Fig. 8(d).

5) Case 5. Supply 5th and 7th Harmonics: In the case of direct grid connected induction motors, the supply voltage is not purely sinusoidal. Harmonics 5th and 7th are the dominant time harmonics in the power system due to the presence of power electronic devices. In this case, 10% harmonics of 5th and 7th are considered in the voltage supply to evaluate the ability of the model in capturing those harmonics with the real-time sampling period. Since the 5th and 7th harmonics are already present in the motor current even for purely sinusoidal supply voltage, due to the spatial harmonics, higher than normal 5th and 7th harmonics are injected in the supply voltage to distinguish the spatial harmonics and the supply voltage harmonics with better visibility. Fig. 8(e) shows that the harmonics are effectively captured in the DFT of the winding current.

6) Case 6. Unbalanced Supply: Finally, The DFT of the stator current with 10% voltage drop in *phase-a* is shown in Fig. 8(f).

Fig. 9 shows the steady-state torque and current versus speed to validate the proposed RT-TLM results with FEM.

The comparison of the MEC-based real-time and 2-D FEM results shows the validity and efficiency of the proposed RT-TLM method in estimating the stator winding phase current harmonic contents. The discrepancy of the results is mainly due to the fact that MEC model is only a crude distributed approximation of the major flux paths whereas FEM is an extremely accurate distributed model. Since the MEC is a lumped

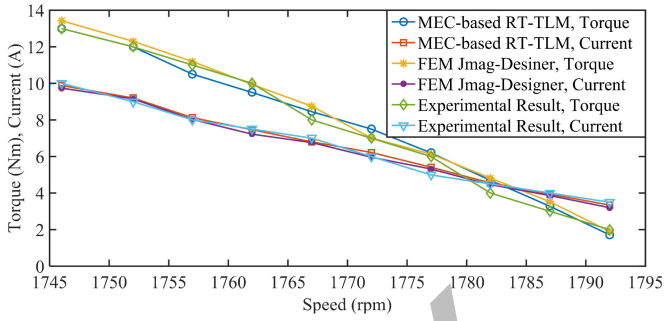


Fig. 9. Steady-state torque and current vs. speed from no load to full load.

parameter model, it is generally expected to display a somewhat different (less accurate) harmonic content in comparison to FEM. For instance, the spatial harmonics in the airgap cannot be modeled accurately due to the lumped modeling of the stator tooth to rotor tooth permeances. On the hardware side, utilization of the 32-bit single precision floating point number of the MEC-based real-time model in comparison to the 64-bit double precision floating point number of the FEM model in Jmag-Designer can results in some deviations by the accumulation of the round-off errors through the computation process. Considering that the high order harmonic amplitudes are negligible in comparison with the main frequency, the DFTs in Fig. 8 are plotted based on decibels ($20\log_{10} x$) to make the harmonics visible. This representation visually highlights the MEC-based real-time and 2-D FEM result discrepancies. Nevertheless, the harmonic content verification of Fig. 8 still shows the proposed MEC-based RT-TLM approach is able to represent a sufficiently accurate signature of spatial and fault harmonics. A more detailed MEC model with a smaller time-step could be proposed to accurately capture higher order harmonics, however, the real-time simulation timing and hardware resource constraints will be violated. Although the MEC model itself is sensitive to the machine parameter uncertainties, the proposed RT-TLM computational procedure is not sensitive to the machine parameter uncertainties. Fig. 10 shows the FEM magnetic field and current density distribution analyzed by Jmag-Designer for healthy and broken bar conditions. It is shown that the rotor broken bar prevents the normal distribution of the magnetic field surrounding the broken bar as well as the stator winding facing that bar. The asymmetric magnetic field distribution as the result of rotor broken bar causes non-sinusoidal MMF in the air gap, which causes the additional harmonic contents in the stator current of Fig. 8(c).

C. Hardware Resource

The implementation of the proposed RT-TLM method is performed on Xilinx Virtex UltraScale+ XCVU9P FPGA board, which is among the highest speed and largest FPGAs available on the market. The concern behind selecting the device is more to achieve the highest clock frequency rather than hardware resource. Table I shows the hardware resource utilization. Since the design is deeply pipelined, just a small portion of the device is used.

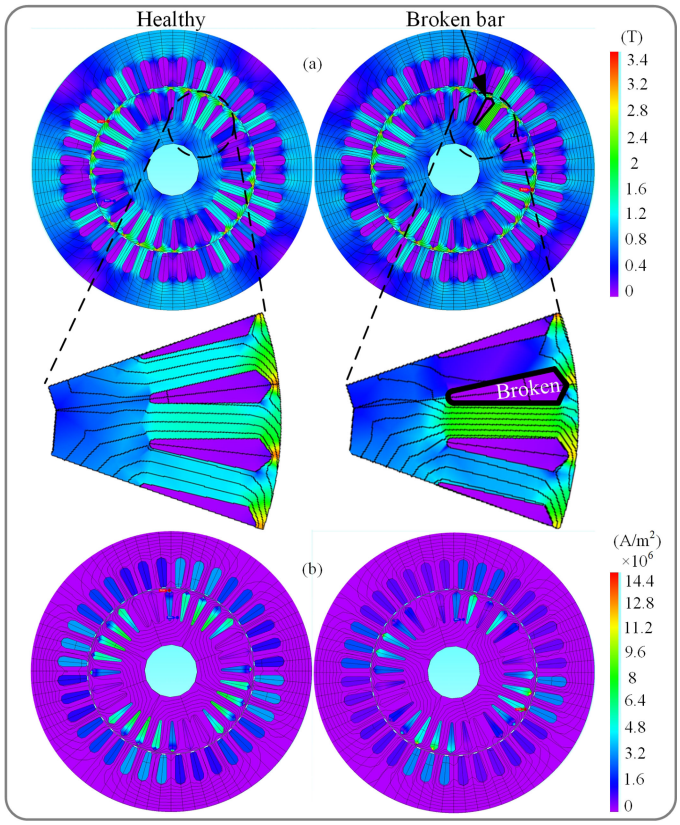


Fig. 10. FEM results of Jmag-Designer for healthy and broken rotor bar. (a) Magnetic flux density. (b) Current density.

TABLE I
HARDWARE RESOURCE UTILIZATION

Resource	Utilization	Available	Percentage
Look-up table (LUT)	63,421	1,182,240	5.36
LUT-RAM	4,343	591,840	0.73
Flip flop (FF)	96,163	2,364,480	4.07
Block RAM (BRAM)	53.50	2,160	2.48
Input/output (IO) port	78	832	9.38
Global buffer (BUFG)	2	1,800	0.11

D. Timing Analysis

Table II shows the latencies of the real-time processing states of Fig. 3. The MEC-based RT-TLM solution timing is reported based on the required number of 3 N-R and 4 TLM iterations with the convergence tolerance of 10^{-3} for both iterative loops when the $\mu_{TLM} = 1000\ \mu_0$ is chosen.

The designed hardware on the targeted FPGA is derivable with the maximum clock frequency of 300 MHz. Consequently, considering the number of clock latencies of Table II and an idle time of 6.04 μs, the minimum time-step of 500 μs is achieved. The 500 μs time-step can be considered small enough to efficiently model the transients of the induction motor since it delivers 33 data points on each cycle of the 60 Hz. Based on Nyquist theorem, a signal can be reproduced with at least two data points per cycle of the highest frequency content of a periodic waveform. Accordingly, the achieved time-step can reproduce the waveform up to the 16th harmonic, i.e., 960 Hz.

TABLE II
LATENCIES OF EACH STATE IN REAL-TIME PROCESSING

State No.	No. of clocks per iteration	No. of iterations per time-step	No. of clocks per time-step	Execution time (μs)
S0	2,498	1	2,498	8.32
S1	4,081	1	4,081	13.6
S2	95,128	1	95,128	317.1
S3	153	N_{TLM}	612	2.04
S4	9,582	N_{TLM}	38,328	127.76
S5	138	N_{TLM}	552	1.84
S6	115	N_{TLM}	460	1.53
S7	534	$N_{TLM} \times N_{N-R}$	6,408	21.36
S8	120	1	120	0.4
Total	-	-	**148,187**	**493.96**

The 500 μs electric machine model can be interfaced with a few μs fast switching power converter model in an electric machine drive system through digital integration of the converter output PWM voltage over the PWM period to supply the electric machine in a variable frequency drive system [29]. The proposed methodology is efficient and can be extended not only to MEC of other types of electric machines but also to FEM computation of any other small to medium size magnetodynamic problem with moving structures subject to availability of the hardware resource and satisfying the real-time constraint.

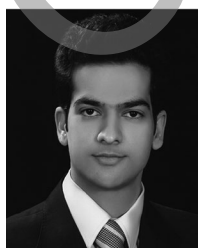
V. CONCLUSION

For the first time, the paper proposes a real-time TLM (RT-TLM) emulation of faulted induction machines, facing the timing constraint challenges with high band width and non-periodic boundary condition of fault studies. The paper applied the TLM method to the MEC model in order to keep the coefficient matrix unchanged during each time-step, requiring only one LU decomposition per time-step due to rotation. The MEC-based TLM matrix is re-ordered efficiently to keep the majority of the matrix unchanged during the entire simulation to facilitate partial pre-calculation of LU decomposition through the left looking Gilbert-Peierls algorithm. Taking the advantage of FPGAs in parallel processing of the algorithm, the minimum time-step of 500 μs with the FPGA clock frequency of 300 MHz is achieved for real-time fault study of electric machines. The results show the accuracy of the proposed method of obtaining the harmonics in the stator winding currents validated by the Jmag-Designer commercial FEM software. The proposed model can be used for testing actual condition monitoring devices to detect and distinguish various types of faults through motor current signature analysis (MCSA); however, it requires complex signal processing and filtering stages, which is left for future work.

REFERENCES

[1] I. Munteanu, A. I. Bratcu, S. Bacha, D. Roye, and J. Guiraud, "Hardware-in-the-loop-based simulator for a class of variable-speed wind energy conversion systems: Design and performance assessment," *IEEE Trans. Energy Convers.*, vol. 25, no. 2, pp. 564–576, Jun. 2010.
[2] F. Gao, B. Blunier, M. G. Simoes, and A. Miraoui, "PEM fuel cell stack modeling for real-time emulation in hardware-in-the-loop applications," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 184–194, Mar. 2011.

[3] O. Vodyakho, M. Steurer, C. S. Edrington, and F. Fleming, "An induction machine emulator for high-power applications utilizing advanced simulation tools with graphical user interfaces," *IEEE Trans. Energy Convers.*, vol. 27, no. 1, pp. 160–172, Mar. 2012.
[4] S. Mojlish, N. Erdogan, D. Levine, and A. Davoudi, "Review of hardware platforms for real-time simulation of electric machines," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 1, pp. 130–146, Mar. 2017.
[5] N. R. Tavana and V. Dinavahi, "A general framework for FPGA-based real-time emulation of electrical machines for HIL applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2041–2053, Apr. 2015.
[6] B. Jandaghi and V. Dinavahi, "Hardware-in-the-loop emulation of linear induction motor drive for maglev application," *IEEE Trans. Plasma Sci.*, vol. 44, no. 4, pp. 679–686, Apr. 2016.
[7] A. B. Dehkordi, P. Neti, A. M. Gole, and T. L. Maguire, "Development and validation of a comprehensive synchronous machine model for a real-time environment," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 34–48, Mar. 2010.
[8] Z. Liu, O. A. Mohammed, and S. Liu, "Equivalent hardware representation of PM synchronous motors from the physics-based phase variable model obtained through FE computation," *IEEE Trans. Magn.*, vol. 45, no. 3, pp. 1450–1453, Mar. 2009.
[9] A. Sarikhani and O. A. Mohammed, "HIL-based finite-element design optimization process for the computational prototyping of electric motor drives," *IEEE Trans. Energy Convers.*, vol. 27, no. 3, pp. 737–746, Sep. 2012.
[10] B. Jandaghi and V. Dinavahi, "Prototyping of nonlinear time-stepped finite element simulation for linear induction machines on parallel reconfigurable hardware," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7711–7720, Oct. 2017.
[11] B. Jandaghi and V. Dinavahi, "Real-time FEM computation of nonlinear magnetodynamics of moving structures on FPGA for HIL emulation," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7709–7718, Oct. 2018.
[12] T. Garbiec, "Fast computation of performance characteristics for solid-rotor induction motors with electrically inhomogeneous rotors," *IEEE Trans. Energy Convers.*, vol. 31, no. 4, pp. 1688–1696, Dec. 2016.
[13] M. L. Bash, J. M. Williams, and S. D. Pekarek, "Incorporating motion in mesh-based magnetic equivalent circuits," *IEEE Trans. Energy Convers.*, vol. 25, no. 2, pp. 329–338, Jun. 2010.
[14] M. Amrhein and P. T. Krein, "Induction machine modeling approach based on 3-D magnetic equivalent circuit framework," *IEEE Trans. Energy Convers.*, vol. 25, no. 2, pp. 339–347, Jun. 2010.
[15] H. Gorginpour, H. Oraee, and R. A. McMahon, "A novel modeling approach for design studies of brushless doubly fed induction generator based on magnetic equivalent circuit," *IEEE Trans. Energy Convers.*, vol. 28, no. 4, pp. 902–912, Dec. 2013.
[16] S. D. Sudhoff, G. M. Shane, and H. Suryanarayana, "Magnetic equivalent circuit-based scaling laws for low-frequency magnetic devices," *IEEE Trans. Energy Convers.*, vol. 28, no. 3, pp. 746–755, Sep. 2013.
[17] S. D. Sudhoff, B. T. Kuhn, K. A. Corzine, and B. T. Branecky, "Magnetic equivalent circuit modeling of induction motors," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 259–270, Jun. 2007.
[18] G. Y. Sizov, A. Sayed-Ahmed, Y. Chia-Chou, and N. A. O. Demerdash, "Analysis and diagnostics of adjacent and nonadjacent broken-rotor-bar faults in squirrel-cage induction machines," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4627–4641, Nov. 2009.
[19] A. Gandhi, T. Corrigan, and L. Parsa, "Recent advances in modeling and online detection of stator interturn faults in electrical motors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1564–1575, May 2011.
[20] J. Faiz, S. M. M. Moosavi, M. B. Abadi, and S. M. A. Cruz, "Magnetic equivalent circuit modeling of doubly-fed induction generator with assessment of rotor inter-turn short-circuit fault indices," *IET Renew. Power Gener.*, vol. 10, no. 9, pp. 1431–1440, Oct. 2016.
[21] P. Naderi and A. Shiri, "Rotor/stator inter-turn short circuit fault detection for saturable wound-rotor induction machine by modified magnetic equivalent circuit approach," *IEEE Trans. Magn.*, vol. 53, no. 7, Jul. 2017, Art. no. 8107013, doi: 10.1109/TMAG.2017.2672924.
[22] O. Deblecker, J. Lobry, and C. Broche, "Use of the transmission line modeling method in FEM for solution of nonlinear eddy-current problems," *Proc. IEE, Sci. Meas. Technol.*, vol. 145, no. 1, pp. 31–38, Jan. 1998.
[23] A. M. Knight, "Time-stepped eddy-current analysis of induction machines with transmission line modeling and domain decomposition," *IEEE Trans. Magn.*, vol. 39, no. 4, pp. 2030–2035, Jul. 2003.
[24] B. Asghari and V. Dinavahi, "Novel transmission line modeling method for nonlinear permeance network based simulation of induction machines," *IEEE Trans. Magn.*, vol. 47, no. 8, pp. 2100–2108, Aug. 2011.
[25] B. Asghari and V. Dinavahi, "Experimental validation of a geometrical nonlinear permeance network based real-time induction machine model," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4049–4062, Nov. 2012.
[26] F. Fleming and C. Edrington, "Real-time emulation of switched reluctance machines via magnetic equivalent circuits," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3366–3376, Jun. 2016.
[27] N. R. Tavana and V. Dinavahi, "Real-time nonlinear magnetic equivalent circuit model of induction machine on FPGA for hardware-in-the-loop simulation," *IEEE Trans. Energy Convers.*, vol. 31, no. 2, pp. 520–530, Jun. 2016.
[28] P. C. Krause, O. Wasynczuk, and S. Sudhoff, *Analysis of Electric Machinery and Drive Systems*. Piscataway, NJ, USA: IEEE Press, 1994.
[29] G. G. Parma and V. Dinavahi, "Real-time digital hardware simulation of power electronics and drives," *IEEE Trans. Power Del.*, vol. 22, no. 2, pp. 1235–1246, Apr. 2007.



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