University of Alberta

Modeling, Analysis and Stabilization of Converter-Dominated Power Distribution Grids

by

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Abstract

The energy sector is moving towards extensive use of power electronic (PE) converters to interface distributed generation (DG) units and modern converter-interfaced loads (CILs). Therefore, the conventional distribution-grid is gradually transformed into a multi-stage PE converter-dominated network. However, interaction dynamics among equivalent source and load converters may adversely influence the overall stability even if each converter stage is inherently functional and stable.

In multi-cascaded PE stages, the equivalent load/source admittance ratio should satisfy the Nyquist stability criterion to ensure stable operation. Moreover, tightly-regulated PE converters induce negative input admittance in the small-signal sense, which reduces overall stability margins.

This thesis addresses interaction dynamics in emerging PE distribution systems by using small-signal linearization to derive equivalent input/output admittance models of typical PE converters. Active compensators are designed to maintain the system stability. Theoretical analysis and extensive simulation results are presented to validate the developed models and the proposed active compensators.

Acknowledgements

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I would like to express my thanks to the examiners committee for their valued time and interests in my thesis.

My sincere thanks go to my mother, brother and all my family for their continuous encouragements and support. This work is also dedicated to the memory of my father who is really missed in these moments.

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Acronyms

AC: Alternating Current

BP: Band-Pass

CCM: Continuous-Conduction Mode
CIL: Converter-Interfaced Load
CP: Constant Power
CPL: Constant Power Load
CSC: Current Source Converter

DC: Direct Current
DER: Distributed Energy Resource
DG: Distributed Generation
d-: Direct-
d-*q*: Direct and Quadrature

HFC: High-Frequency Compensator
HP: High-Pass
HVDC: High Voltage DC

IGBT: Insulated-Gate Bipolar Transistor

LC: Inductive-Capacitive
LPF: Low Pass Filter
LSC: Load-Side Compensator

MFC: Mid-Frequency Compensator
MPP: Maximum Power Point

p.u: Per-Unit

PCC: Point of Common Coupling

PE: Power Electronic

Pf: Power Factor

PHEV: Plug-in Hybrid Electric Vehicle

PI: Proportional Plus Integral

PLL: Phase-Looked Loop

PMSM: Permanent Magnet Synchronous Motor

PV: Photovoltaic

PWM: Pulse-Width Modulation

q-: quadrature-

RES: Renewable Energy Source

RHS: Right Hand Side

RIC: Reference-Inverter-Current

RIV: Reference-Inverter-Voltage

RLC: Resistive-Inductive-Capacitive

RLV: Reference-Load-Voltage

rms: Root-Mean Square

SW: Static Switch

SSC: Source-Side Compensator

STATCOM: Static Synchronous Compensator

UPS: Uninterrupted Power Supply

VSC: Voltage Source Converter

VSI: Voltage Source Inverter

VSR: Voltage Source Rectifier

WTG: Wind Turbine Generator

Chapter 1

Introduction

1.1 Background

Driven by environmental and technical reasons, the interest in distributed energy resources (DERs) and micro-grids is gaining high momentum in the smart grid environment [1]. Most DERs are interfaced to the grid/load via high efficiency tightly-regulated power electronic (PE) converters. Micro-grids can be classified as alternating current (ac), direct current (dc) or hybrid ac/dc types.

Ac micro-grids have an advantage of utilizing the existing ac power grid infrastructure but they require quite complicated control strategies for the synchronization process and preserving the system stability [2], [3].

Dc micro-grids offer several attractive features. From the generating side, most of the renewable energy resources are inherently dc, such as photovoltaic (PV) cells, fuel cells and storage units. From the load-side, modern electronic loads such as computers, data centers, communication & technology facilities and, more importantly, most of motor drives can be directly supplied with dc. Dc power lines provide better current carrying capacity than ac lines due to the absence of the skin effect in dc transmission. Moreover, dc micro-grids have better short circuit protection and transformer-less voltage levels, which significantly improve the efficiency, size and cost of the distribution network [4]–[7].

As the penetration level of both ac/dc loads to micro-grids systems increases, hybrid high-stream networks that combine down-stream ac/dc micro-grids via multiple bi-directional converters are created [8], [9]. Hybrid grids help to reduce successive multi-conversions between ac and dc using PE converters to improve system reliability and efficiency.

Future micro-grids may be combined with smart meters, communication facilities and remote control of both generation units and loads to move-forward to smart grids era. Decentralized control topologies with maximized reliability and real-time energy management with data acquisition systems are the main featuring characteristics of

smart grids [10]. The conventional distribution system is transformed to active distribution system with distributed intelligence capabilities.

With the variety of these topological structures, the conventional utility-grid with the thermo- and electro-mechanical distribution systems is gradually transformed to multi-stage PE converter-dominated system, in which interaction dynamics and stability can be a major issue.

1.2 Research Motivation

In multi-converter distributed generation (DG) applications, interaction dynamics among converters can adversely influence the overall stability even if each PE converter is inherently functional and stable [11] – [13]. If the system is initially stable, additional loading or changed generation conditions may influence the dynamic performance and lead to instabilities.

For PE converters that are integrated to converter-dominated power grids, the following conditions should be fulfilled to ensure the achievement of plug-and-play features and averts possibility of destabilizing interaction dynamics:

- Meeting the admittance ratio or "Nyquist" criterion especially with multi-cascading of PE stages [13] – [19]. For voltage source PE systems, with equivalent load (input) and source (output) admittance around a common point of investigation, the overall system stability is guaranteed if the equivalent load admittance is less than the equivalent source admittance. With current source converters, this criterion is reversed [19].
- Compensating the side effects of tightly-regulated control objectives in advanced PE interfaces to effectively meet load or generation requirements. Tightly-regulated control topologies induce the PE stage to incrementally appear as a negative admittance, which reduces overall stability margin. Equivalently, this behavior is represented by a constant power (CP) operation which inherently has negative damping characteristics [13], [20] and [21].

Throughout the thesis Chapters, the aforementioned stability conditions are evaluated in different topologies of converter-dominated power grids. Moreover, proposed active techniques are employed to satisfy these conditions and maintain the system stability.

1.3 Research Objectives

This research aims to assess interaction dynamics in power distribution grids with high penetration of converter interfaced loads (CILs), and develop efficient active damping solutions to mitigate undesirable interaction dynamics. The key objectives are summarized as follows:

- Developing small-signal admittance models for key PE converters in different DG applications such as dc, ac and hybrid micro-grids.
- Conducting stability analysis based on the Nyquist admittance ratio criterion around common points of interconnections in DG systems.
- Designing linear active compensators either from the source- or load-sides to actively satisfy the stability conditions. Linear analysis tools such as root-locus and Bode plots are utilized in the design phase and dynamics studies [22].

1.4 Thesis Layout

The remainder of the thesis is organized as follows:

Chapter 2 presents the state-of-art and literature survey of converter modeling for stability studies, and converter-dominated power grids including dc, ac and hybrid systems with their structure and operation.

Chapter 3 presents the dc micro-grid as an example of converter-dominated networks. The voltage-source rectifier (VSR) as a dc micro-grid interface is subjected to severe instabilities if it is highly penetrated by CILs. Analytical studies, stability investigation and proposed stabilization solutions applied to the VSR side are provided. Evaluation results obtained from a complete dc micro-grid model built under Matlab/Simulink® platform [23] are presented.

Chapter 4 presents stability analysis and active damping solutions of ac micro-grids under high penetration of tightly-regulated CIL. This Chapter provides multi-solutions for interaction dynamics problems with typical scenarios that can be applied in ac micro-grid applications. Firstly, interaction dynamics between the equivalent source-side that is represented by a voltage-source inverter (VSI)-based ac micro-grid and a VSR-based common load is provided. Load-side compensator (LSC) is proposed to successfully integrate the VSR interfaced load to the ac micro-grid. Secondly, generic model for augmented CILs is considered when supplied from an ac micro-grid

interface. As a result, a load-independent design approach for a proposed source-side compensator (SSC) from the VSI is presented to actively satisfy the Nyquist admittance ratio criterion.

Chapter 5 presents a recently emerged scenario in DG applications, which is a hybrid ac/dc grid. Destabilizing interaction dynamics are studied analytically and demonstrated through a complete hybrid network model. In this scenario, the CILs are represented by a VSI and augmented model of a dc micro-grid; these entities are connected to a dc DG park. Active compensation technique is proposed at the VSI sides to relocate the overall lightly-damped modes of the hybrid network to more damped ones. The influence of the operating mode of the DG park with dispatchable or non-dispatchable DER on the ac micro-grid or grid-connected inverters are investigated as well.

Chapter 6 presents the thesis summary, conclusions, and suggestions for future work.

Chapter 2

Background and Literature Survey

2.1 Introduction

This Chapter introduces background and literature survey of the core topics in the thesis. The Nyquist admittance ratio criterion with the destabilizing effect of tightly-regulated PE converters will be addressed. A general background on different modeling approaches for equivalent load or source admittance of tightly-regulated PE stages in converter-dominated grids is also provided. These methods include the *d-q* transformation method, phasor-based modeling and harmonic linearization technique. It is shown that PE interfaces became key building element for different applications in the power system. As result, converter-dominated grids such as; dc micro-grids, ac micro-grids and hybrid grids are formed with challenging interaction dynamics problems and stability issues.

2.2 Interaction Dynamics and Instabilities in Converter-Dominated Grids

2.2.1 Nyquist Admittance Ratio Criterion

In multi-converter systems, the ratio between the source output admittance and the load input admittance around an interconnection point must satisfy the Nyquist stability criterion to ensure the overall stability of the integrated system [14] – [19].

Figure 2.1 shows equivalent impedance representation of a voltage source and load subsystems integrated at interconnection point *ab*. The source subsystem is represented by a Thevenin equivalent circuit with a voltage source (V_s) and a source impedance $\left(Z_s(s)\right)$ while $Z_l(s)$ is the equivalent load impedance; s is the Laplace operator. Applying voltage division on the linear circuit in Figure 2.1 yields:

$$V_l = V_s \frac{Z_l(s)}{Z_l(s)+Z_s(s)} = V_s \frac{1}{1+\frac{Z_s(s)}{Z_l(s)}} \tag{2.1}$$

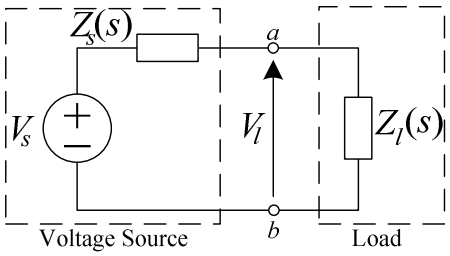

Figure 2.1: Impedance representation of integrated voltage source-load system.

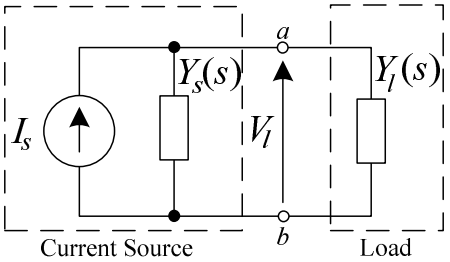

Figure 2.2: Impedance representation of integrated current source-load system.

The source voltage is assumed to be stable, so the stability of the integrated systems is maintained if the ratio $(1 + Z_s(s)/Z_l(s))^{-1}$ is stable. This ratio represents a closed loop system with a unity forward gain and negative feedback of the ratio $Z_s(s)/Z_l(s)$. Thus, the system is stable if $Z_s(s)/Z_l(s)$ satisfies the Nyquist stability criterion. In other words, this ratio $(Z_s(s)/Z_l(s))$ mustn't encircle the (-1 ,0) point on Nyquist plots which means that $Z_s(s)$ should be less than $Z_l(s)$ in the whole frequency domain range. The stability condition in (2.1) is applied to voltage source converters (VSC) where the source impedance $\left(Z_s(s)\right)$ is required to be low.

For grid-connected converters, current control topology is employed [19]. As result, stability criterion in (2.1) has to be modified. Figure 2.2 shows impedance representation of integrated load and current source system. The current source subsystem is represented by a Norton equivalent with a current source (I_s) in parallel with source admittance $\left(Y_s(s)\right)$ while the load is represented by equivalent load admittance $\left(Y_l(s)\right)$. The load voltage (V_l) is given by:

$$V_l = I_s \frac{1}{Y_l(s)+Y_s(s)} = \left(\frac{I_s}{Y_l(s)}\right)\frac{1}{1+\frac{Y_s(s)}{Y_l(s)}} \tag{2.2}$$

Assuming a stable current source (I_s) and load $\big(Y_l(s)\big)$, the overall system stability is maintained if the ratio $(1 + Y_s(s)/Y_l(s))^{-1}$ is stable. Therefore, the stability criterion with current source converters (CSC) is that the ratio $Y_s(s)/Y_l(s)$ must satisfy the Nyquist criterion ($Y_s(s) < Y_l(s)$ in the whole frequency domain range).

Comparing (2.1) and (2.2), it can be concluded that the stability requirements for VSC is opposite to that for CSC. Both results meet the ideal requirements in which the voltage source impedance $\big(Z_s(s)\big)$ is ideally zero and the source impedance $\big(1/Y_s\,(s)\big)$ of a current source is ideally infinity.

Note that PE converter systems are highly nonlinear. The load or source impedances in multi-stages PE converter systems are obtained by averaging and linearization methods as shown throughout the thesis Chapters. So, both $Z_s(s)$ and $Z_l(s)$ (or $Y_s(s)$ and $Y_l(s)$) can be obtained and represented by small-signal linearization analysis. They can be represented by a transfer function that depends on the control and physical parameters of the associated PE converter.

From the stability conditions in (2.1) and (2.2), the system can be re-stabilized by modifying or "reshaping" the source- or load-side impedance (admittance) to avoid undesirable interactions on the whole frequency domain. The reshaping can be done by using passive elements or active compensators to modify the load- or source-side characteristics and achieve load/source admittance matching (i.e. avoid interactions).

2.2.2 Tight Regulation Effect of Power Electronic Converters

In multi-converter applications, interaction dynamics among individual converters may adversely influence the overall stability. Even if each individual converter is inherently functional and stable in standalone operation, possible destabilizing interactions may exist once sub-systems are integrated [20]. With standalone PE converter, the source impedance is usually small and the converter itself may drive a passive load. Thus, the system stability is probably maintained. With the current advances in PE technology with associated cost reduction, multi-stage PE systems are created. As a result, interaction dynamics arise and become more complicated as the simple passive-load/low-source impedance combination is no longer applied.

According to the nature of the PE converter, there exist closed loop control functions to tightly regulate certain parameter such as speed in motor drives applications or output voltage in a VSR. Consequently, and based on the controller parameters, the PE converter tends to appear as a constant power load (CPL). As a result, incremental negative input admittance of the overall converter appears within the bandwidth of the converter control loop. Any reduction of the input voltage to the PE converter causes an increase in the drawn current due to the negative slope of the input admittance. As result, the input voltage decreases further. Similarly, with any step increase of the input voltage, successive increases with instabilities are yielded [21].

Interaction dynamics problems in multi-stage PE converter grids, especially dc type, were considered earlier in self-contained electric distribution systems in aircrafts to move towards the more electric aircraft (MEA) and fly-on-wire (FOW) concept [24]. Hydraulic drives and pneumatic transmission systems are replaced by PE interfacing converters to reduce the weight, cost and maintenance and increase the reliability and efficiency of the overall system [25].

In the following subsections, it will be shown that cascaded PE converters became the main building element in DG systems. Therefore, interaction dynamic problems that might violate the Nyquist admittance ratio criterion with the equivalent CP mode of operation appear with severe degradation in system stability.

2.3 Power Converters Modeling for Interaction Dynamics Studies

Power converter modeling is classified into time-domain methods such as state-space modeling or frequency-domain methods such as admittance-based modeling. State-space modeling is mainly adopted in large power systems where the effect of individual loads or sub-distribution systems is insignificant to the overall system dynamics due to their relatively small capacity. In power electronics distribution systems, this assumption is not valid because the individual loads should be accurately considered to assess the overall distribution system dynamics. Therefore, with load variations, which occur frequently in distribution systems, the system model have to be reconfigured. This technique is not preferred in distribution systems and, more importantly, in DG applications where high uncertainties exist at the load-side.

On the other hand, admittance-based analysis is advantageous due to:

- Its compatibility with the Nyquist admittance ratio criterion that depends on obtaining the equivalent load and source admittances to investigate the system stability around an interconnection point.
- Each equivalent load or source admittance can be analytically obtained using small-signal linearization methods.
- If the load or source admittance is not available analytically, they can be developed numerically or experimentally with the aid of system identification techniques [26] – [29].
- Multi-converter networks can be modeled by cascaded load/source admittances to provide flexibility in adding or removing a load or source without major influences on the overall model characteristics.

Developing source or load admittance for PE converters requires small-signal linearization tools to overcome the nonlinearities associated with the switching devices of the converters modules. Some modeling techniques are discussed to figure out the most appropriate method by which small-signal analysis and hence admittance-based technique can be developed and applied [30].

2.3.1 DQ-Coordinates System Modeling

In switch-mode dc power converters, the averaging method is usually adopted to overcome the discontinuity and switching behavior of PE converters [31], [32]. Small-signal linearization can be applied to approximate nonlinearities in the resultant average-model around certain operating points. In ac distribution systems, average-method can be also applied [33]. However, the resultant nonlinear model is time-varying that makes it impossible to be linearized by small-signal linearization tools. Alternatively, nonlinear analysis tools can be directly applied to the resultant nonlinear and time-varying average model but on the expense of the modeling complexity. On the other hand, the most popular analytical tool for the time-varying systems is to use rotating frame coordination system [34]. The time-varying quantities are transformed to direct and quadrature (*d-q*) axis components in a two dimensional rotating frame that rotates synchronously with the angular speed of the three phase quantities. In this transformation, there exists a zero-axis component which is dropped in case of three-

phase balanced systems or systems with floating neutral as the zero-axis current is trapped. As result, both *d-q* components equivalently appear as dc quantities in steady state conditions so that they can be linearized using small-signal analysis tools.

The main features of the *d-q* transformation method are:

- It is very compatible with machine analysis and control in power systems. A widely used approach is to employ the field orientation control in three-phase machines using synchronous-frame proportional plus integral (PI) current controllers [35]. This technique allows the machine to achieve similar torque control performance to a separately excited dc motor, where torque and flux can be controlled separately.
- In the resultant *d-q* coordination system, cross coupling terms appears. Compensating these terms can be accomplished by including decoupling terms in the control loops.
- This method is only applicable for three-phase, balanced systems. It is not applied for single-phase systems. With unbalanced systems, periodically and time-varying zero-axis component appears, and makes the linearization impossible. However, the maximum voltage unbalance level is 3% or less [36] in typical distribution systems. Therefore, accepted and accurate models under the current low leveled unbalanced conditions can be obtained.
- This method is not applicable to involve harmonic studies as they have multi-frequencies which make it difficult to specify the orientation angular velocity. Otherwise, the *d-q* transformation will contain time-varying components.
- It has limited accuracy up to frequencies below the switching frequency of the PE device, however, high switching frequencies for PE converters nowadays provides wider accurate modeling band.

2.3.2 Phasor-Based Modeling

Phasor-based modeling yields nonlinear quantities but all are constant under steady-state operation. Thus, the small-signal linearization analysis can be applied. However, some major drawbacks of this modeling technique that conflict with the admittance-based analysis are summarized as follows:

- The dimension of the phasor-based model is significantly high because each physical parameter has to be represented by two variables (e.g. amplitude and phase).
- Phasor models that are represented by magnitude and phase or real and imaginary components can't be explicitly converted to a single admittance-based model. In most cases, both input (or output) current and voltages are time-varying quantities; therefore, it becomes difficult to express them in the form of input (or output) admittance.
- Complex phasor models solve the problem of defining load or source admittances for PE converters. However, nonlinear models are often not differentiable which means that small-signal linearization can't be applied.

2.3.3 Harmonic Linearization Modeling

Harmonic linearization method has been used as a systematic modeling approach to linearize periodically time-varying nonlinear systems [37] – [39]. This technique uses Fourier analysis to describe the relations of current and voltage mapping through the converter switching circuits that are combined together to give an impedance mapping model. By this model, the dc-side impedance of PE converters can be transformed to the equivalent small-signal ac-side impedance, or vice-versa.

The main features of harmonic linearization techniques are as follows:

- It is compatible with admittance-based analysis.
- For three-phase converters, two admittances, one in the positive sequence and the other in the negative sequence result.
- Unlike the *d-q* transformation method, harmonic linearization can handle unbalanced and single-phase systems as well. Moreover, no cross coupling terms are yielded.
- Lengthy and relatively complex mathematical analysis is required to obtain the source or load admittance for PE converters as compared to *d-q* transformation method. Moreover, most of available models in literature are for single/three-phase diode rectifier circuits which are not the typical interfacing PE converter in the modern DG systems.

- More importantly, harmonic linearization has limited capabilities to accurately model the nonlinear dynamic behavior below the line fundamental frequency. Tightly-regulated PE converters show negative input admittance especially at low frequency region. However, with harmonic linearization method the obtained model shows ordinary positive input admittance as compared to the *d-q* transformation method [30]. This methods still demands more investigation to be compatible with interaction dynamics in PE systems with CP mode of operation.

2.3.4 Conclusion

Major draw backs characterize the phasor-based modeling method; in particular, the difficulty in defining a merged form for the source or load admittance for PE converter. Harmonic linearization method shows limited capabilities to predict the nonlinear dynamic behavior of tightly-regulated PE converters at low frequency range which implies a failure in modeling the negative source or load admittance.

In conclusion, the *d-q* transformation method is the most compatible tool with admittance-based analysis; accordingly it will be adopted to develop source or load admittances throughout this thesis.

2.4 Power Electronic Interface as a Key Element in Converter-Dominated Grids

Renewable energy sources (RESs) and DG units are gaining a global adoption from the utility-grid integrators to overcome the environmental and technical challenges that face the future of the conventional power system. Most RESs such as wind turbines, PV modules and fuel cells are interfaced by PE devices to be integrated to the distribution system [40] – [44]. With the progressive consideration of RESs, micro-grids that cluster parallel operated DG units to supply local loads are formed [45]. Micro-grids can operate in grid-connected or islanded mode of operation in case of fault conditions at the utility side. PE as RES interfaces in micro-grid applications improve the injected active power quality and provide reactive power on demand to regulate the voltage of the point of common coupling (PCC). The harmonic content of the PCC voltage and injected current can be also controlled by the PE interface [46]. Uninterrupted power supplies (UPS) that mainly depend on PE converters can be used

to provide reliable supply for critical loads such as hospitals, data centers, airports or sensitive industrial loads. UPS systems are used to supply critical loads up to approximately 0.5 hour. During this time, a backup diesel generator is automatically started up to supply these loads [47], [48].

From the end-user side, the penetration level of PE motor drives will increase from 40% in 2000 to 80% in 2015 [49]. Moreover, PE converters as load interface help to save energy and hence, save cost. The 50-60% of electrical energy that is supplied to motor drives loads in the developing world can be potentially reduced by 20-30% if advanced PE motor drives are used. In lighting systems, PE can save 30% of the consumed electrical energy currently used [49]. Most of modern residential loads will be interfaced by PE converters for better controllability and efficiency. Even heating loads will be electronically interfaced such as induction heating [50].

The concept of "more electric" vehicles recently motivates utility integrators to be considered as a visionary plan in the near future. Plug-in hybrid electric vehicles (PHEVs) have a high density battery that can be charged from external power source (charging station) so that the vehicle can run on electric power to significantly increase the miles per gallon (MPG) for the fossil fuel [51]. In June 2009, The Ford motor company launched the first prototype of PHEV to be tested. The Canadian Hydro-Québec utility company will field-test this vehicle to demonstrate its influence on the grid stability at different modes of charging or discharging [52]. Obviously, PHEV will be interfaced to the utility-grid through PE converters for charging and discharging process. However, the performance of the utility-grid may be an issue under high penetration of PHEV if simultaneous battery charging occurred. On the other hand, PHEV in the parking periods can contribute smartly to meet the grid requirements of active and reactive power. In [53], large number of PHEV has been utilized to operate as a virtual static synchronous compensator (STATCOM) during the parking times. The primary objective of the virtual STATCOM is to obtain controllable three-phase ac voltage at the PCC to regulate reactive power flow [54]. The proposed idea successfully emulates STATCOM operation in coordination with grid-side converter of a 400 MW wind farm in a 12-bus system.

Intelligent PE concept is currently emerged to cope with the "intelligent-grid" or "smart grid" era. The expected smart grids will exploit communication infrastructures

to facilitate the operational control and energy management among spatially distributed entities. Energy control center (ECC) that consists of smart meters, remotely operated breakers and data acquisition units will be employed for that purpose. With smart grids, artificial intelligence can be added to the system to improve the protection capabilities. The system will be able to perform transition between grid-connected and islanded mode of operation for certain clusters or micro-grids without exterior assistance. In the same manner, synchronization process, power sharing among parallel connected DG units, islanding detection and load shedding can be performed [50], [55].

A new class of PE applications with signaling technology is provided in [56]. PE devices are deployed to the power system as communicating interface for monitoring and information-oriented purposes. In these applications, PE devices are not utilized as a conventional electric energy converter but as communication routers to convey information signals through the power systems.

PE research and development (R&D) is driven by a multi-disciplinary approach to be more adaptive in the integration process to the power system. The semiconductor research is mainly motivated by two directions; reducing the overall cost of the materials and manufacturing process, and increasing the device efficiency and reliability by introducing innovated semiconductors such as silicon carbide that allow operation at higher switching frequencies without significant burden on the overall efficiency [57], [58].

As shown in all previous applied scenarios and current trends in the DG applications, advanced PE converters are progressively adopted in the distribution system in both generation- and load-sides. As a result, the conventional utility-grid with the thermo- and electro-mechanical distribution systems will be gradually transformed to a multi-stage PE converter-dominated system in which large number of converter-fed loads is loaded by others.

Figure 2.3 shows a schematic diagram of a possible converter-dominated power grid. As shown, two clusters of power plants are tied together via high voltage dc (HVDC) connection. HVDC is beneficial for connection of distant offshore wind farms to the ac grid, connection of two asynchronous ac systems and transmitting bulk power [59] – [62]. As shown, a wind turbine with ac-dc/dc-ac converter and a PV interfaced

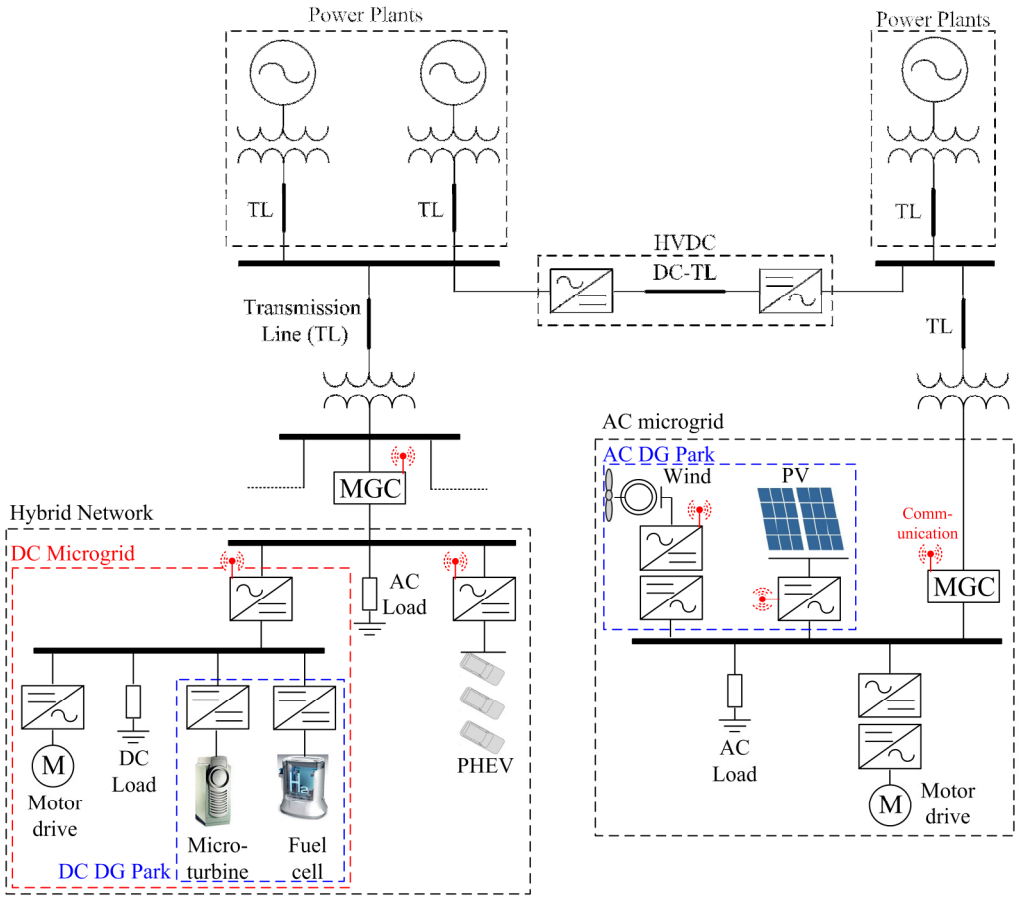

Figure 2.3: Schematic diagram of a converter-dominated power grid.

by a VSI are connected in parallel to form an ac DG park that supplies a common ac load with a motor drive. The resultant ac micro-grid can supply its local loads autonomously or with the help of the utility-grid. Energy management is achieved locally within the ac micro-grid or globally among other entities by a micro-grid controller (MGC).

This can be done by using a communication facility to provide monitoring, data acquisition and routing, enabling and disabling settings and control commands. In the same figure, a dc DG park that consists of a micro-turbine and a fuel cell forms a dc micro-grid to secure a reliable and efficient supply for the common dc load. The dc micro-grid is interfaced to the ac system by a controlled bidirectional VSR with communication facility to enhance smart power management. On the other hand, the PHEV station can positively interact with the overall system through its bidirectional

interfacing converter at the parking times to work in parallel with the dc micro-grid to supply the common ac load. As shown, a hierarchically interconnected and dynamically coupled small entities (DG parks, dc micro-grid, PHEV) are structured together to form an extended mix of ac and dc systems which is known as a hybrid network.

The advantages of the converter-dominated power grids can be summarized as follows:

- Incorporating advanced PE interfaces with fast and accurate switching capabilities for fast dynamic response and improved performance.
- Hierarchically structured ac, dc and hybrid micro-grids that reduce the successive need of energy conversions and hence reduce the overall power losses especially with the employed efficient PE converters.
- The hierarchical structure provides higher reliability of energy supply that is suitable for critical loads.
- Global and bidirectional energy routing among up/down steam entities with easier power management that is achieved by the communication facilities.
- Large number of advanced PE devices provides higher flexibility in control topology innovations for better performance and stabilization. For example, active damping techniques can be employed to mimic virtual resistive damping in different locations in the grid that positively affects the system stability without real passive losses.

On the other hand, the possible disadvantages of such systems are:

- Expensive infrastructure is needed with improved protection components that should have adaptive coordination capabilities to cope with the fast reconfiguration of the physical system.
- The wide dependence on wireless communication, networking and related softwares subjects the overall system security to the danger of data-viruses attacks, bugs and unauthenticated breaching. As a result, blackouts no longer depend on the physical equipment only but also on the accompanied softwares and operating systems [63].

- The advanced PE control topology induces the device to equivalently operate at CP mode that shows a resultant incremental negative admittance from its terminals with inherent negative damping.
- Strong dynamics coupling among the equivalent load and source-sides of PE stages that may violate the Nyquist criterion and challenge the overall system stability.
- High uncertainties in the added DG units and newly connected CILs influence the overall system stability. If the original system is stabilized, a sudden change in operating point, load dynamics and control parameters may affect system stability.
- Low inertia in PE dominated network requires improved control topology to ensure global stability under large-signal disturbances.

This thesis addresses dynamics and stability issues of converter dominated networks in an effort to mitigate undesirable interactions and increase the safe penetration level of PE converters in conventional distribution networks. In the following subsections, more details on emerging entities within the converter-dominated grids such as dc micro-grid, ac micro-grid and hybrid grids are provided.

2.5 DC Micro-grids

2.5.1 Background

Recent advances in PE converters technology increase the interest in dc active distribution systems. Dc power systems are used in some applications such as telecommunications, navy ships, aircraft, electric vehicles and traction [64] – [66]. Dc micro-grids can operate whether in grid-connected mode or islanded mode of operation. As compared to the ac type, dc systems offer several attractive benefits. From the generating side, most of the emerged DG systems are dc such as PV units, fuel cells and storage batteries. To connect a DG unit to a dc system, only voltage levels need to be regulated as opposed to ac systems which require synchronization process where the voltage magnitude, frequency and phase have to be matched with the grid [67]. From the load-side, many conventional loads such as computers, TV sets or even industrial loads such as motor drives require dc supply [50]. Multiple ac-dc or dc-ac power conversion stages are not needed in dc micro-grids as compared to the ac

type. Dc power system is transformer-less, therefore, high efficiency, compact size, low cost and high reliability are the main featuring characteristics of dc micro-grids.

Dc systems only operate with two-wire cables as compared to the three- or four-wire cables in ac systems. The current carrying capacity is higher with dc cables as compared to ac ones due to the absence of skin effect in dc transmission [68]. A cable in a dc system can handle $\sqrt{2}$ times higher root-mean square (rms) voltage as compared to ac system. The power transmitted with dc systems is also $\sqrt{2}$ times that of the ac systems with the same cable considering similar rms current [69]. Note that the maximum voltage is equal to the rms value in dc systems.

There is no reactive power flow in dc grids, as a result the voltage control is mainly dedicate by the active power flow unlike the ac micro-grids systems where the voltage control is dedicated by reactive power flow while the injected active power mainly define the local power angle of the interfacing VSI [70].

On the other hand, several challenges still face the wide adoption of dc micro-grids. Standard protection equipment which is used in ac systems such as circuit breakers and fuses are not compatible to dc systems [71]. Under faulty conditions in ac systems, an arc is created inside the circuit breaker. To extinguish this arc, the dielectric strength across it has to be increased so that the system is recovered at the first zero current crossing which happens twice per each cycle. The higher the dielectric strength, the faster the extinguish process occurs. Dielectric strength can be increased by cooling the arc or introducing fresh medium such as air or Sulfur hexafluoride gas (SF6) [72]. As there is no zero crossing in the dc current, protection of such systems is more challenging. However, some solutions have been proposed in literature such as using larger distance between the breaker contacts. In [73], the three-phase circuit breaker can be used by connecting its three contact pairs in series to be compatible with dc applications. Obviously, high cost is associated with the compatibility of the current protection systems to dc grids.

However, dc micro-grids are very promising and attractive. Lots of challenging problems are being solved and investigated. In [74], the unbalancing problem in dc networks has been mitigated. It is found that unbalanced dc load or generation between the positive and negative lines of the bipolar system in dc grids induces a net current that flows in the third reference (ground) dc cable which increases the system losses.

The authors proposed a dc current re-distributer that is based on PE interface with the associated control technique to successfully mitigate the unbalancing problem.

Modified operational control strategies and power sharing techniques for dc micro-grids have been proposed in literature [75]. Automatic power balancing technique is achieved in [76] based on coordination control between storage units and utility-grid converter. In islanded mode of operation, DG units with battery systems are employed to ensure functional operation of the dc micro-grid.

2.5.2 Interaction Dynamics and Instabilities

As an entity within the converter-dominated power grids, dc micro-grids suffer instabilities due to equivalent CP mode of operation that may violate the Nyquist admittance ratio criterion. Several stabilizing techniques are proposed to damp instabilities due to the CP effect. These techniques depend on satisfying the Nyquist criterion from the load or the source-side by either active methods that depend on control system modification or passive methods by considering additional passive elements(s).

An analytical investigation of dc-dc converters when loaded by a CPL in multi-converter power systems is provided in [77]. A linear model of a tightly-regulated dc-dc buck converter that equivalently operates at the CP mode is obtained. As a conclusion, a CPL can be approximately modeled by a negative resistance parallel with a constant current source. Stability criteria of dc-dc buck converters have been analytically obtained. It is found that the open loop converters are highly influenced by the selection of inductive-capacitive (LC) filter parameters. It is recommended to increase the dc-link capacitor or the inductor resistance to maintain the system stability. Similarly, the inductor size itself, when reduced gives better stability margin. These stability conditions are mainly obtained to satisfy the Nyquist admittance ratio criterion from the source-side. The CP effect implies that there is an excessive amount of energy that circulates between the inductor and capacitor of the LC filter. Hence, reducing the inductor size helps to reduce this energy. Similarly, if the capacitor value (C) increases, the circulating energy (E) will induce less voltage (V) oscillations ($E = \frac{1}{2}CV^2$).

Passive damping techniques are investigated to stabilize an ideal CPL that is represented by a negative resistance connected to a voltage source and LC filter [77] – [79]. Three different damping methods are proposed by adding a damping combination consisting of a series resistance and capacitor all in parallel with the original filter capacitor; adding a damping combination consisting of series resistance and inductor all in parallel with the original filter inductor; and adding additional parallel resistance and inductor all in series with the original filter inductor. Indeed, the system stability is significantly improved. However, it is not preferred to consider additional passive elements in PE converter circuits especially with renewable energy and DG applications. The added resistance increases the system losses; the inductor increases the bulk and weight whereas the additional capacitor (usually electrolytic) decreases the reliability of the overall system. Moreover, the recent trend in PE converter design is to reduce the size of the dc-link capacitor. Film capacitors are recently introduced to allow much higher current per unit volume which significantly reduces the size of the capacitor [80].

In [81], different strategies to mitigate the CP effect in dc micro-grids are provided, such as load shedding, addition of damping resistance, using storage units or filters and using control techniques for active damping purposes. For the load shedding, the equivalent CPL is reduced by shedding some of tightly-regulated converters within the dc micro-grid. However, it has been found that system oscillations can't be effectively reduced even with shedding a portion of the CPL unless there is a sufficient resistive element to damp these oscillations. Further, the shedding strategy depends on the importance of the load; if the CPL is crucial, it can't be interrupted. A nonlinear line regulating compensator is proposed as well. The main pros of nonlinear controllers in CPL mitigations are the resultant global stability, fast convergence to the desired control reference and providing better transient response with minimal overshoots and settling time if compared to linear controllers. However, the complexity of the nonlinear controller makes it less attractive. Moreover, the switching frequency is not well defined in this nonlinear controller which may complicate the magnetic component design. Alternatively, active damping has been accomplished through linear controllers by adding a virtual resistance embedded in the proportional and derivative controller gains.

Another method in [81] considers adding a resistance in parallel to the dc-link capacitor. This method, however, yields extra losses as mentioned. Ultra-capacitors can be used to improve the dc-bus voltage stability by satisfying the impedance ratio criterion. However this method requires a PE converter to interface the capacitor to the dc-bus besides the high cost of ultra-capacitors and the complexity added to the system.

An active damping method to mitigate the CPL instabilities in dc-dc converters is proposed in [82]. The proposed method depends on compensating the negative resistance induced due to the CP mode of operation by adding a virtual positive resistance. It is advantageous method as it is non-dissipative, so it is suitable to be used in DG applications. The virtual resistor is created by measuring the inductor current of the converter and subtracting it from the control voltage. This method has been successfully applied to buck, boost and buck-boost dc-dc converters when they are terminated by a CPL. Moreover, it has been implemented with isolated dc-dc converters. Opposite to passive techniques proposed in [78], [79], this method is completely non-dissipative with no additional passive elements.

A Power shaping stabilizing control strategy for dc power systems with CPL is proposed in [83]. The dynamic power balance equation that relates the injected power from a dc-dc converter minus the consumed power to the CPL to the rate of change of the energy stored in the capacitor is reformed to become linear. This is accomplished by introducing a new state variable of the square of the output dc voltage which is proportional to the energy stored in the capacitor. By controlling this state variable through a PI controller, the output voltage is indirectly controlled. Moreover, the power demand is the output of the voltage-square control loop. By this way, the overall system is completely linear while the presence of the CPL is seen by the control system as a disturbance.

Pulse adjustment control technique is proposed in [84] to achieve output dc voltage regulation based on generating high and low power pulses instead of the conventional pulse-width modulation (PWM) control techniques. If the output dc voltage is lower than the desired values, high-power pulses are generated to compensate this difference. Similarly, if the output dc voltage is higher than the desired values, low-power pulses

are generated. This method depends on energy balance among the filter inductor, capacitor and the CPL.

All proposed compensation methods in [77] – [84] focus on stabilization of the CPL effect from the source-side. The main advantage of these methods is their load-independence approach. The CPL model is modeled generically as a negative resistance while the source-side is reconfigured to mitigate its destabilizing effect. Though its simplicity, this modeling approach, however, has several disadvantages: 1) it ignores the frequency-dependent nature of the input admittance, so it might yield over-designed damping solutions. 2) It does not facilitate sensitivity and stability studies that combine the load, control, and active compensation dynamics to investigate the effects of the negative admittance compensator on the load dynamics.

The exact model of a typical CPL has been considered in other works. Using a load-side compensator, that is load dependent, the CPL instabilities are mitigated. Load dependent approach is adopted in motor drive applications that have tightly-regulated speed response and loaded by a constant load. Hence, they show incremental negative input admittance from the drive terminals. The incremental input admittance of a typical motor drive system has been accurately modeled in [85]–[92] to investigate the actual frequency range of the negative admittance and to assess the participation levels of different system parameters. Active compensation methods depend on feeding a portion of the dc-link voltage into the current (or torque) reference to provide the necessary damping performance. This approach is reported in [85]-[88] for permanent magnet synchronous motor (PMSM) drives and in [89], [91] for a PMSM with trapezoidal back electromotive force (emf). A similar approach can be applied to induction motor drives to compensate for the CPL behavior [93].

Further, in [87]–[90], the active compensation signal is generated via a high-pass (HP) filter with a tuned cut-off frequency. However, this compensator with the HP filter reshapes the input admittance in a wide frequency range depending on the designed cut-off frequency which affects system dynamics. A typical compensation strategy is proposed in [85] to yield enhanced characteristics by replacing the HP filter with a band-pass (BP) filter. With a proper design, the BP filter operates in the mid-frequency range, in which the Nyquist criterion is violated due to the resonant peak of the dc-side LC filter. This approach relatively immunes the low frequency (speed

control loop) and high frequency (current control loop) dynamics from interacting with the compensator.

The provided compensators from the source-side [81] – [84], or the load-side [85] – [92] depend on linear analysis. Nonlinear and large-signal stability of dc-dc converters have been considered to mitigate the CPL effect in multi-converter systems. A nonlinear feedback linearization is introduced in [94] to cancel the destabilizing effect of the CPL in dc grids. For buck dc-dc converter that operates in continuous-conduction mode (CCM), the relation between the output voltage and load current is defined by the CPL loop with negative resistance. If this loop is cancelled, the converter will operate as it has a conventional resistive load. The authors added a loop to compensate this effect using a derivative term and a gain to map the amount of the CPL effect that is required to be cancelled. The compensator gain depends on different operating points (inductor size, input voltage and the CPL). These points are not easy to be estimated and hence the compensator gain has to be selected so that the CPL loop becomes positive under all operating points. As result, positive damping of the CPL effect is added to the system. This technique can be applied to different types of dc-dc converters.

The Brayton-Moser's mixed potential theory, as a nonlinear tool, has been used in [95] to provide stability criteria for a CPL with multi-stage LC filters. Multi-stage LC filters are usually employed in aircraft to achieve better noise attenuation and reduce the overall required capacitance as compared to the single stage LC filter. By using this method, the stable operating points of this system are obtained. This analytical method provides a design criterion of multi-stage LC filters with an ideal CPL.

A system level global stabilization of multi-loads in dc power system is investigated in [96]. The considered multi-loads are a PMSM, dc-dc converter feeding a resistive load and a super capacitor controlled by a bidirectional dc-dc converter. The source-side is modeled by an ideal voltage source with LC filter. The global stability of the proposed system is maintained using a large-signal stabilizing compensator based on the Lyapunov theory. The principle is to implement stabilizing powers in the state space model that should be injected to each contributing load as a CPL to avoid instabilities. However, all loads are assumed to have efficient control objectives so that

they can be modeled as a perfect CPL without taking the exact dynamic model into account.

In the aforementioned techniques [77] – [96], all active compensation methods are mainly proposed to damp the CPL effect for dc-dc converters when they are interfaced by tightly-regulated PE converters. Dc micro-grids are usually interfaced to the ac-side by a PWM VSR. Therefore, active damping design in dc micro-grids employing PWM VSR interface demands special attention. Recently, a switched control strategy is proposed for a PWM VSR feeding a CPL [97]. The switching control directly stabilizes the CPL via the dc voltage control loop. A switched control strategy is adopted to adaptively change the dc voltage controller gains to preserve the system stability under different loading levels. This method, however, does not decouple the active damping and voltage tracking performances and demands continuous gain adaptation.

Chapter 3 in this thesis addresses dc micro-grid stability under high penetration of tightly-regulated PE converters; and proposes three simple and computationally-efficient active damping solutions that can be implemented to stabilize the VSR micro-grid interface.

2.6 AC Micro-grids

2.6.1 Background

In contrarily to the dc type, ac micro-grids are more prevalent in the power system because they have the advantage of utilizing the existing ac power grid infrastructure. Ac micro-grids may be combined with smart meters, communications and remote controls to become the building element in the future smart grid. Besides, utility operators are more familiar with ac micro-grids as compared to the dc type. Moreover, there is no need to reconfigure the end-user loads or building structures when they are supplied from ac micro-grids. Ac loads can be directly connected to the ac micro-grids without using interfacing converters whereas in dc micro-grids, these loads must be interfaced by ac-dc converter. Ac micro-grids also have the advantage that they provide the utility-grid with ancillary services and reactive power support.

Small-signal modeling and stability analysis of parallel connected VSI in micro-grid mode of operation have been provided in [98]. The authors considered the power sharing loop dynamics in the small-signal modeling. However, ideal inverter behavior is assumed with perfect and fast voltage and current controllers. As a result, the influence of the voltage and current control dynamics is ignored, which is very important especially with high VSI ratings where the switching frequency is usually limited. Modified and exact modeling and analysis of autonomously-operated VSI in an ac micro-grids have been considered in [99] based on state-space modeling approach and small-signal linearization that include the outer active and reactive power sharing controller, the ac voltage controller and the inner current controller. The modeled VSI is terminated by output LC filter. Based on the developed model, eigen values or modes that represent the overall dynamics are obtained and clustered in three regions; high frequency high damping region that combines the modes that are sensitive to the current controller dynamics, medium frequency medium damping modes that are sensitive to the voltage controller dynamics and finally, low frequency and lightly damped modes that are sensitive to the power sharing controller. Therefore, the power sharing loop dedicates the ac micro-grid stability.

Power sharing control for parallel connected inverters in ac micro-grids has been addressed in several works [100] – [105]. Generally, power sharing control in these systems depends on emulating the performance of the governor of synchronous generators where the active power is coupled to the operating frequency while the reactive power is related to the operating voltage, both according to the droop characteristics. Conventional droop control is considered in [98], [99] where static droop gains are considered to control the active and reactive power sharing. However, static droop gains have slow and oscillatory dynamics. Moreover, to change the transient response, the steady-state power sharing is affected. Therefore, a modified droop control method [100] with conventional droop coefficients in addition to dynamics ones with derivative and integral gains is proposed. Improved and controllable transient response result without influencing the steady state power sharing. Usually, inductive output impedance behavior of VSI is considered to achieve the regular active and reactive power sharing. However, the output impedance of the VSI is not always inductive which significantly affects the accuracy of the power

sharing [101]. Active-power/frequency and reactive-power/output-ac voltage relations are only valid with purely inductive output impedance behavior whereas the active power is defined by the output ac voltage and the reactive power is controlled by the operating frequency in purely resistive output impedance characteristics. Hybrid inductive/resistive characteristics of the output impedance yields completely coupled active and reactive power [102], [103]. As result, a proposed nonlinear controller is provided in [101] to introduce a virtual output inductive impedance of VSI to maintain the active and reactive power sharing. Moreover, accurate harmonic power sharing is yielded in case of supplying nonlinear loads. Further investigation of the effect of output impedance on the power sharing accuracy is provided in [102], [103]. A proposed power sharing controller is provided to accurately achieve proper active and reactive power sharing regardless the output impedance type. In [104], a proposed power sharing control method is presented to consider the impact of complex impedance (hybrid inductive/resistive) and avoid circulating currents. Low frequency relative stability in parallel connected inverter based DG is addressed in [105]. It has been shown that the low frequency modes of the power sharing dynamics drifts to new locations and relative stability is remarkably affected. A proposed power sharing controller is introduced to preserve the relative stability by introducing dynamic droop coefficient which can be adaptively tuned to preserve the dominant poles' loci. Hence, the relative stability can be preserved without affecting the steady state operation.

Based on droop control, energy management systems for a standalone micro-grid has been proposed in [106]. The proposed technique defines the optimal generator dispatch level by selecting the droop gains and maintains the system stability.

2.6.2 Interaction Dynamics and Instabilities

The concept of multi-port PE interface for renewable energy resources and storages is presented in [107]. A single phase VSI is used to interface different types of DG units; with their dc-dc converters, to the utility-grid. An integrated control structure for the source dc-dc converters is provided for better efficiency. However, a focused analysis is put on the source-side dc-dc converters by replacing the VSI with a common resistive load, by which interaction dynamics between DG units and the VSI as an interface to the utility-grid is ignored. In [108], a multi-inverter micro-grid is studied

with a computational method to determine the system stability. The model provided considers the effect of the power droop coefficients as they have low frequency eigen values which dominate the micro-grid stability [105]. It is shown that the analysis based on the complete models for three-inverter micro-grid is quite long and complex. Thus, in multi-converter networks with large number of converters, it is more convenient and computationally-efficient to model the system using cascaded input/output admittances that consider the physical topology and overall control parameters.

The Nyquist stability criterion can be also applied to evaluate the ac-bus stability of VSI. In this case, the input admittance is seen from ac capacitor of VSI to the common ac load with/without the utility-grid while the output admittance is that seen from ac capacitor towards the VSI switches. This ac admittance of a VSC is addressed in [109] to investigate the converter-grid interactions and stability conditions. Similarly, the ac-side admittance (or harmonic admittance) of VSI is addressed as in [110], [111] under different topologies but with assumption of ideal dc-link voltage. A similar recent work is presented in [112] to provide analytical modeling of harmonic interactions between the utility-grid and the DG inverters using their ac-side admittance. The importance of the output ac admittance of VSC also appears in [113] where a sub-synchronous torsional stability analysis is performed to study the interaction dynamics induced by a current controlled VSC that is located electrically nearby a synchronous machine. From [109] – [113], it can be concluded that the ac-side stability for VSC based on its output ac admittance is a well-defined problem in literature.

In [98] – [106], the common load considered in ac micro-grid application is mostly taken as a static resistive-inductive-capacitive (RLC) load. However, with the high penetration of advanced PE interfaced loads or generators within the ac micro-grids, static RLC modeling may not be indicative and efficient enough to reflect the real dynamics in the system.

Similar to dc micro-grid, interaction dynamics among VSCs in ac micro-grids is a significant problem that affects the overall system stability. However, the interaction dynamic problems due to the violation of the Nyquist admittance ratio criterion or the penetration of tightly-regulated converters in ac micro-grids have not been addressed in literature. In dc micro-grids, this problem is heavily tackled due to its early

involvement in the aircraft, navy ships and electric vehicles systems. With the emerging of dc micro-grids, those solutions were automatically imported.

The influence of the CPL on the ac micro-grid stability has been only addressed in [114]. With CP operation, it is concluded that the system stability cannot be preserved by only tuning the current and voltage controllers. The mitigation technique was achieved passively by adding additional resistive load in parallel to the aggregated CPL so that the overall load impedance increases, to satisfy the Nyquist stability criterion. However, the CPL is generically modeled by a negative resistance which ignores the load dynamics and its interactions with the ac micro-grid PE interface. Moreover, the damping criteria considered is to add a resistive load in parallel with the original CPL so that the resultant load damping increases. Obviously, very restricted loading conditions are yielded that conflict with the uncertain nature of DG systems. Indeed, it is not feasible to impose loading conditions on the end-user customers to avert probable instabilities. Moreover, the penetration level of resistive load sharing decreases as compared to CPL penetration; therefore, the natural damping of resistive loads might not be sufficient to mitigate the effect of the CP operation and maintain adequate stability margins in the micro-grid system under different loading conditions.

Interaction dynamics between DG converters and CPL becomes more significant in isolated ac micro-grids. In this mode, the aggregated source impedance of DG units increases, which might violate the Nyquist stability criterion. However, if the same CPLs are supplied in grid-connected mode, stability margins can be remarkably improved as the aggregated source impedance of DG units and the grid decreases significantly due to the relatively large stiffness of the grid as compared to DG units. Therefore, future considerations of such kind of loads should be adopted in micro-grid management and operational control or in weak grids.

To address the interaction dynamics problem in the converter-dominated ac micro-grids, Chapter 4 addresses ac micro-grid stability under high penetration of tightly-regulated CILs. Different scenarios for ac micro-grids are considered and investigated in this thesis:

- Interaction dynamics between the equivalent source-side that is represented by VSI as an ac micro-grid interface with a VSR terminating a resistive load as common

CIL. A LSC is proposed to successfully integrate the VSR interfaced load to the ac micro-grid.

- Interaction dynamics between the equivalent source-side that is represented by VSI as an ac micro-grid interface with a generic model of augmented CIL load that is represented by incremental negative admittance. A load independent design approach is followed to design a SSC on the VSI interface.

2.7 Hybrid Grids

2.7.1 Background

As discussed in the last two subsections, each of ac and dc micro-grids has advantages but also disadvantages. Hybrid grids combine both of them by employing multi bidirectional PE converters to combine their benefits with minimal drawbacks. Hybrid grids are gaining high interest. Note that with each deployed dc micro-grid to the utility-grid, an unintentional hybrid grid is formed [50].

Hybrid grids provide variety of ac or dc supply within the same vicinity so that ac or dc loads can be fed from the suitable supply without additional conversions. Obviously, this increases the overall efficiency and reliability. However, the mix of different ac and dc loads or generators requires well-coordinated control algorithms so that smooth power transfers are achieved with stable performance. Moreover, energy management and operational control of such grids is more complicated as compared to individual ac or dc micro-grids.

2.7.2 Interaction Dynamics and Instabilities

Interaction dynamics between ac and dc micro-grids within a hybrid system has not been extensively studied. In [115] the authors considered a dc micro-grid that consists of a wind turbine generator (WTG), a generator-side converter and some controllable loads interfaced by dc/dc converters (electric water heaters and battery systems). On the ac-side, the system is interfaced by a grid-side inverter that is connected to a diesel generator and variable ac load. By using a proposed droop control technique at the controllable dc loads that yields a modified current control dynamics, the common dc voltage fluctuations could be suppressed. This is achieved by sharing the power consumption levels of the dc loads according to their ratings when dc-bus voltage rises.

Similarly, the discharge rate of battery systems is shared among controllable loads when the dc-bus voltage falls. By that way, power balance between the loads and generators is achieved to minimize the coupled dynamics between the ac-side generation and the controllable dc loads.

As a facilitated operational control example of a proposed hybrid ac/dc grid, a coordination control scheme among multiple PE converters is proposed in [116]. The provided control emphasis on harnessing the maximum power from RES, minimize the circulating powers between the ac and dc entities and hence maintain the system stability in both grid-connected and islanded mode of operation. Power balance between the generation and consumption is the main objective to maintain the system stability in all modes of operations. Detailed control topologies for all PE converters in the proposed hybrid grid is provided to be coordinately controlled to supply efficient and high quality power to local loads and utility-grid as well.

Chapter 5 presents a comprehensive assessment and active damping mitigation strategies of the interaction dynamics in hybrid converter-dominated networks based on source/load admittance modeling of PE stages. In this scenario, the CILs are represented by two VSI entities, one supplies local load while the other interfaces the utility-grid, and augmented model of a dc micro-grid. The VSI entities and dc micro-grids are supplied from a dc DG park. It is shown that source/load admittance mismatch can occur between the equivalent load and source admittances which, as result, degrades the common dc-link stability. As a mitigation approach, three active compensation methods are proposed and implemented in VSI interfaces to virtually reshape their dc-side input admittance; hence the Nyquist criterion can be actively maintained with higher stability margin for the overall hybrid network. Sensitivity study of the hybrid network is conducted to investigate the effect of dc-link dynamics on the load-side performance with the proposed active compensators. The influence of the operating mode of the DG park with dispatchable or non-dispatchable DER on the ac micro-grid or grid-connected inverters are also investigated.

Chapter 3

Linear Active Stabilization of Converter-Dominated DC Micro-grids[1]

3.1 Introduction

Dc micro-grids are gaining high momentum under the smart grid environment. Dc micro-grid stability can be an issue under high penetration of tightly-regulated power converters used to interface distributed resources and loads. Figure 3.1 shows a configuration of a dc micro-grid system, where a bidirectional PWM ac-dc VSC is used to interface the dc micro-grid to an ac system. Within the dc micro-grid, DG units, such as PV cells, micro-turbines and wind turbines are integrated. Storage units are also available to provide energy back-up for critical loads. The voltage level conversions are handled by tightly-regulated dc-dc converters, whereas dc-ac converters can be used to supply ac loads and motor drives. Resistive load can be available within the dc micro-grid but with lower penetration level as compared to the penetration level of PE generators/loads. With the increased adoption of power converters to enhance the performance of line-start motors and other conventional loads, it is expected that the resistive load sharing will decrease to 15% to 20% by year 2015 [49]. This indicates that future micro-grids can be regarded as converter-dominated grids.

This Chapter addresses dc micro-grid stability under high penetration of tightly-regulated PE converters; and proposes three simple and computationally efficient active damping solutions that can be implemented to stabilize a controlled VSR interfacing a dc micro-grid to an ac system. The proposed active damping methods depend on reshaping the VSR impedance by injecting internal-model-based active damping signal at the outer, intermediate and inner control loops of the voltage-

[1] *Publications out of this Chapter:*

A. A. A. Radwan and Y. A.-R. I. Mohamed, "Linear active stabilization of converter-dominated dc micro-grids," *IEEE Transactions on Smart Grids*, in press [Available Online, Digital Object Identifier: 10.1109/TSG.2011.2162430].

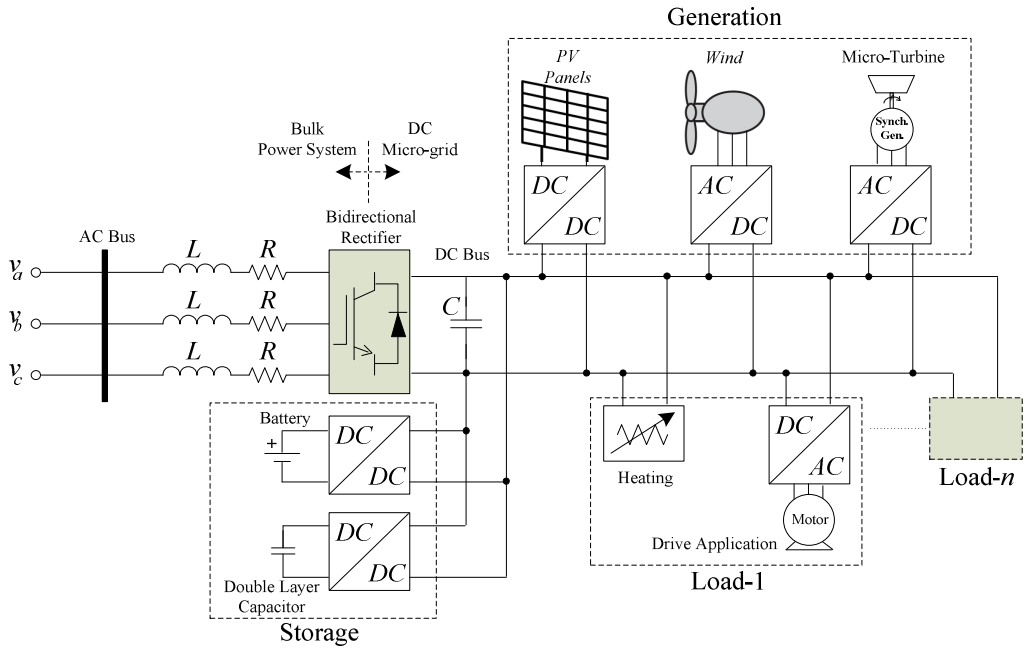

Figure 3.1: Schematic diagram of a dc micro-grid.

oriented VSR interface. Small-signal analysis is conducted to assess the system stability under different compensation schemes. Moreover, the reshaped source impedance of the VSR interface and the modified voltage-tracking dynamics are derived under different compensation schemes. Sensitivity and robustness analyses are provided to assess the dynamic coupling among active damping and voltage tracking controllers. Evaluation results, based on a detailed model of a dc micro-grid with multiple tightly-regulated CILs, are provided to validate the developed models and demonstrate the effectiveness and robustness of proposed techniques.

3.2 Modeling of DC Micro-grids Converter-Interfaced Loads

To show the influence of the tight regulation on dc micro-grid stability, typical dc micro-grid load models are presented. The first example considered is a dc-ac converter as a motor drive with TR motor speed. The second example is a dc-dc buck converter with resistive load and tightly-regulated output dc voltage. In both cases, due to the tight regulation, incremental negative impedance appears from the load terminals.

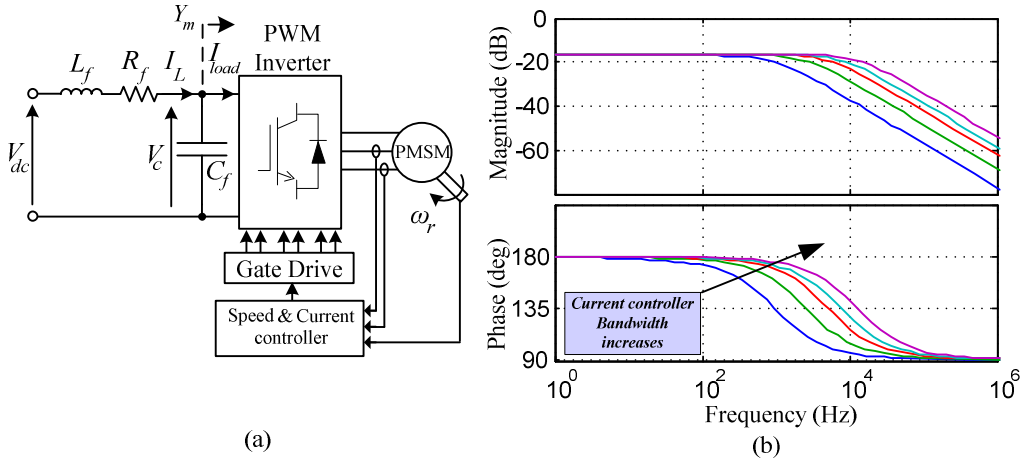

Figure 3.2: PMSM drive as a typical load in a dc micro-grid. (a) PMSM drive schematic. (b) Small-signal input admittance of the PMSM.

3.2.1 Motor Drive with DC-AC PWM Converter

A PMSM drive is shown in Figure 3.2 where a three phase PWM inverter is interfaced to the dc micro-grid by a dc filter. The objective of the drive controller is to tightly regulate the motor speed; hence incremental negative input impedance appears to the dc filter capacitor (C_f). As result, the dc-bus voltage (V_c) oscillates and may suffer instability. Based on the small-signal analysis of the PMSM drive system, the incremental input admittance (ΔY_m) as seen by the dc filter is:

$$\Delta Y_m = \frac{3}{2} V_{mq}^{\circ} \left(\frac{V_{mq}^{\circ} - I_{mq}^{\circ} K_{mp}}{V_c^{\circ 2}} \right) \frac{s + \frac{T_e}{J} \left(\frac{1.5(n_p\psi)^2 - JK_{mi}}{1.5(n_p\psi)^2 \omega_r^{\circ} - T_e K_{mp}} \right)}{L_m s^2 + \left(K_{mp} + \frac{K_{mi}}{K_{mp}} L_m \right) s + K_{mi}} \tag{3.1}$$

where K_{mp} and K_{mi} are the proportional and integral gains for the PMSM current controller, respectively; L_m is the stator inductance; n_p is the number of pole pairs; ψ is the flux linkage of the rotor magnets; T_e is the motor electrical torque; J is the motor inertia; ω_r° is the steady state motor speed; V_{mq}° and I_{mq}° are the steady state quadrature-(q-) axis component of the motor input voltage and current, respectively; V_c° is the steady state value of the dc-link voltage; s is the Laplace transform operator. The PMSM drive model is given in Appendix A3.1 [85] – [88].

The frequency response of (3.1) is shown in Figure 3.2(b). The phase value of the

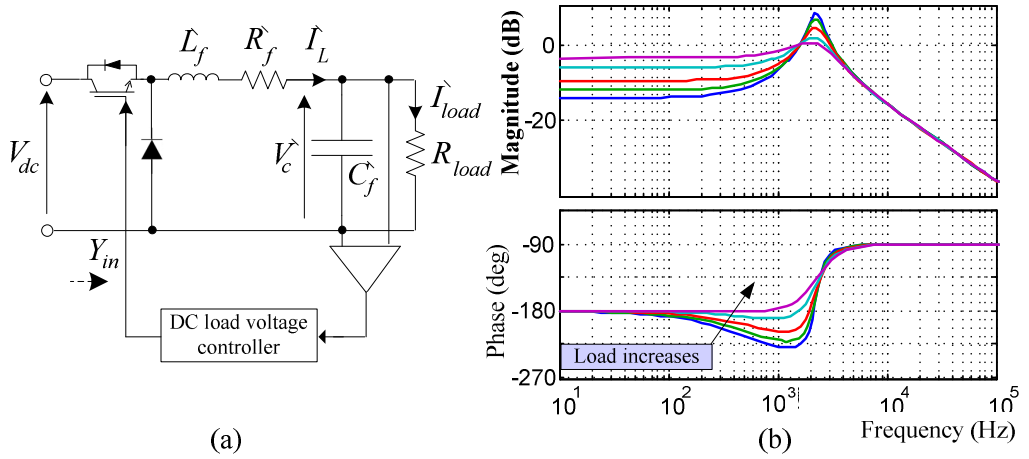

Figure 3.3: Tightly-regulated dc-dc buck converter load in a dc micro-grid. (a) System schematic. (b) Small-signal input admittance.

input admittance (180˚) depends on the current controller bandwidth. The higher the control bandwidth, the higher frequency range of the negative incremental admittance reflected to the dc-bus voltage.

3.2.2 DC-DC Buck Converter Supplying a Resistive Load

Figure 3.3(a) shows a dc-dc buck converter with a tightly-regulated output dc voltage. The output power of the converter is constant at each loading condition due to this regulation. Applying small-signal analysis, the incremental input admittance (ΔY_{in}) can be obtained by:

$$\Delta Y_{in} = \frac{\left(C_f' R_{load}\right)s - 1}{\left(C_f' L_f' R_{load}\right)s^2 + \left(C_f' R_f' R_{load} - L_f'\right)s + \left(R_{load} - R_f'\right)} \tag{3.2}$$

where R_f', L_f' and C_f' are the resistance, inductance and capacitance of the dc filter. The dc-dc converter model is given in Appendix A3.2 [33], [77].

Figure 3.3(b) shows the frequency response of (3.2) at different loading levels. As shown, the admittance has negative value (-180˚) over large frequency range and it depends on the loading conditions.

The aforementioned examples indicate that the penetration of tightly-regulated PE converters to the dc micro-grid degrades the system stability due to the inherent negative damping effect of these converters. As seen in Figure 3.2 and 3.3, the

frequency range of the negative admittance of the CIL varies with the load or controller variations. As a result, the best generic model for the augmented CPL is to consider the worst loading condition, which is a negative resistance at the whole frequency range.

3.3 Modeling of the DC Micro-grid Interface

The dc micro-grid interface is a PWM ac-dc bidirectional VSC. The interface is shown in Figure 3.4 where R and L represent the total resistance and inductance of the ac-side filter and grid parameters at the PCC. The dc micro-grid bus is connected to the tightly-regulated advanced PE loads and generators.

Using the two-phase (*d-q*) synchronous reference frame, the ac-dc bidirectional converter large-signal model can be given by [117], [118]:

$$V_q - V_{dc}D_q = (R + sL)I_q + I_d\omega L \tag{3.3}$$

$$V_d - V_{dc}D_d = (R + sL)I_d - I_q\omega L \tag{3.4}$$

$$sCV_{dc} = 1.5\left(I_qD_q + I_dD_d\right) - I_{dc} \tag{3.5}$$

where I_d and I_q are *d-q* components of the input ac currents; V_d and V_q are the *d-q* components of the input ac voltages and D_d, D_q are the rectifier duty ratios, respectively; C is the dc-link capacitance, ω is the synchronous angular frequency; $I_{dc} = P/V_{dc}$ is the dc current injected by the interfacing converter to the dc-bus of the micro-grid, where P is the total power drawn by the dc micro-grid loads; and V_{dc} is the dc-bus voltage.

The control strategy considered in this paper consists of vector controllers in terms of a reference frame aligned with the ac-bus voltage vector. An outer dc voltage controller is used for dc voltage tracking and regulation, whereas an inner current controller is used for voltage-orientation mechanism at a unity power factor by setting the quadrature component of the input ac current to zero [119], [120].

The mathematical model for the dc voltage controller is given by:

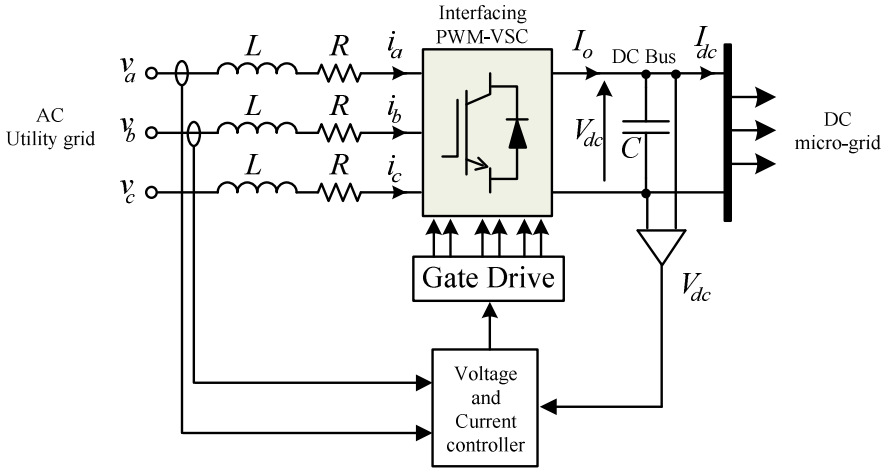

Figure 3.4: Bidirectional controlled ac-dc converter interfacing a dc micro-grid.

$$I_d^{ref} = \left(V_{dc}^{ref} - V_{dc}\right)G_v(s) \tag{3.6}$$

where V_{dc}^{ref} is the reference dc-bus voltage; $G_v(s)$ is the dc voltage controller and is implemented by proportional (K_{vp}) and integral (K_{vi}). This loop generates the direct- (*d*-) axis component of the ac-dc converter reference current (I_d^{ref}) whereas the quadrature reference component (I_q^{ref}) is set to zero for unity power factor operation.

In (3.3) and (3.4), cross coupling terms due to the input ac inductor appears with a voltage drop that should be cancelled especially at high power ratings. Compensating these terms can be accomplished by including decoupling loops in the current controller loop as follows:

$$V_{dc}D_d = -\left(I_d^{ref} - I_d\right)G_i(s) + V_d + I_q\omega L \tag{3.7}$$

$$V_{dc}D_q = -\left(I_q^{ref} - I_q\right)G_i(s) + V_q - I_d\omega L \tag{3.8}$$

where $G_i(s)$ is the current controller with proportional and integral gains, K_{ip} and K_{ii}, respectively. Figure 3.5 shows the overall large-signal block diagram of the micro-grid interface. The current controller synthesizes the duty ratios in the *d-q* frame which are used to generate the controlled signals of the insulated-gate bipolar transistor (IGBT) switches in the interface power circuit.

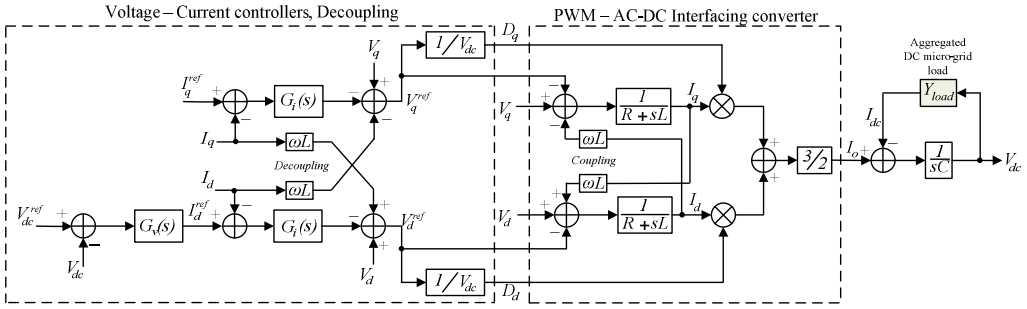

Figure 3.5: Large-signal model of ac-dc controlled interfacing converter.

The design procedures of the dc voltage and current controllers are addressed in literature [119]–[121]. Firstly, the inner current controller loops should be designed to achieve high bandwidth characteristics. Solving (3.4) and (3.7), the transfer function between I_d and I_d^{ref} is given by:

$$\frac{I_d}{I_d^{ref}} = \frac{K_{ip}\, s + K_{ii}}{L\, s^2 + (R + K_{ip})\, s + K_{ii}} \tag{3.9}$$

The zero and one of the poles in (3.9) are designed to cancel each other by setting $K_{ii}/K_{ip} = R/L$ which results in:

$$\frac{I_d}{I_d^{ref}} = \frac{K_{ip}/L}{s + K_{ip}/L} \tag{3.10}$$

From (3.10), the bandwidth of the current controller loop is K_{ip}/L.

Secondly, the dc voltage controller loop can be designed by using the control block diagram in Figure 3.5. The voltage tracking transfer function is given by (3.11), which can be used to design the voltage controller parameters based on the desired natural frequency and damping ratio. The voltage loop bandwidth is much slower than the current controller loop and can be designed within the 20 – 60 Hz.

$$\frac{V_{dc}}{V_{dc}^{ref}} = \frac{1.5D_d^{\circ}\left((K_{vp}K_{ip})s^2 + (K_{vp}K_{ii} + K_{ip}K_{vi})s + K_{vi}K_{ii}\right)}{LCs^4 + (R + K_{ip})Cs^3 + (CK_{ii} + 1.5D_d^{\circ}K_{vp}K_{ip})s^2 + 1.5D_d^{\circ}(K_{vp}K_{ii} + K_{ip}K_{vi})s + 1.5D_d^{\circ}K_{vi}K_{ii}} \tag{3.11}$$

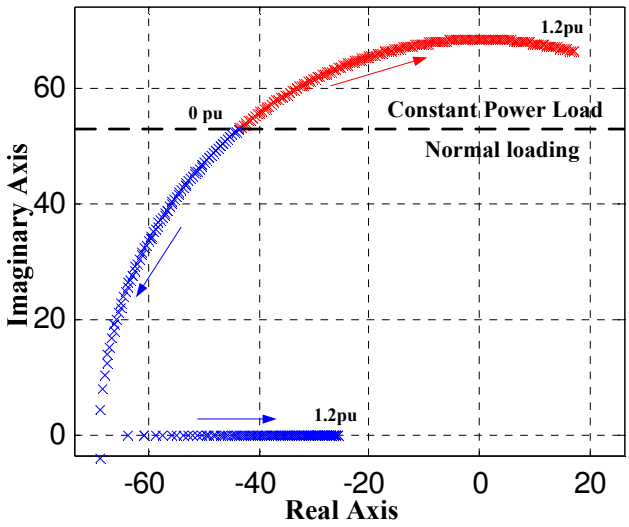

Figure 3.6: Root-locus graph of one component of the conjugate dominant pole of the system characteristic equation with a constant power and normal loading conditions.

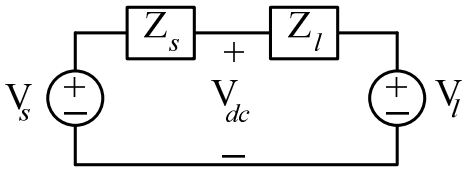

Figure 3.7: Impedance based stability criterion equivalent circuit.

3.4 Composite Loading Effect on the VSC Stability

In this section, small-signal analysis of the uncompensated system is presented to assess the effect of high penetration of tightly-regulated PE loads on the dc micro-grid stability. Initially, it is assumed that the dc micro-grid is loaded by 100% of tightly-regulated power converters to show their effect on the system stability. Then, the natural resistive load penetration to the dc micro-grid will be considered. Considering the existing resistive load (R_d), the dc-bus dynamics in (3.5) is modified to:

$$\left(sC + \frac{1}{R_d}\right)V_{dc} = 1.5\left(I_q D_q + I_d D_d\right) - I_{dc} \tag{3.12}$$

Using (3.4), (3.6) and (3.7), the small-signal *d*-axis current can be obtained in terms of ΔV_{dc} where:

$$\Delta I_d = -\frac{G_v(s)G_i(s)}{R+sL+G_i(s)}\Delta V_{dc} \tag{3.13}$$

Using (3.13) and applying small-signal linearization on (3.12), the small-signal transfer function between the dc-bus voltage (ΔV_{dc}) and the rectifier duty ratio (ΔD_d) can be given by:

$$\frac{\Delta V_{dc}}{\Delta D_d} = \frac{1.5I_d^{\circ}\left(Ls^3+\left(R+K_{ip}\right)s^2+K_{ii}s\right)}{\left[\begin{array}{c} LCs^4+\left(\left(R+K_{ip}\right)C+\left(\frac{1}{R_d}-\frac{P^{\circ}}{V_{dc}^{\circ 2}}\right)L\right)s^3+\left(CK_{ii}+\left(\frac{1}{R_d}-\frac{P^{\circ}}{V_{dc}^{\circ 2}}\right)\left(R+K_{ip}\right)+1.5D_d^{\circ}K_{vp}K_{ip}\right)s^2 \\ +\left(\left(\frac{1}{R_d}-\frac{P^{\circ}}{V_{dc}^{\circ 2}}\right)K_{ii}+1.5D_d^{\circ}\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\right)s+1.5D_d^{\circ}K_{vi}K_{ii} \end{array}\right]} \quad (3.14)$$

where I_q° and ΔI_q are zero in the small-signal sense; P° is the steady state active power flowing through the VSC; and V_{dc}° is the nominal dc-bus voltage. $1/R_d$ can be set to zero to get the 100% penetration of tightly-regulated power converters to the dc micro-grids.

Using the voltage dynamics in (3.14), the root-locus graph is shown in Figure 3.6 (with $\frac{1}{R_d} = 0$) under gradual change of the loading level from 0 to 1.2 per-unit (p.u.) (at 12 kW base power). The dc voltage controller is designed with 20 Hz bandwidth. One component of the dominant conjugate pole is shown only. The dominant pole travels to the right hand side (RHS) of the s-plane as loading increases, which indicates unstable conditions due to the tight regulation effect. Moreover, in the nominal loading conditions (1.0 p.u.) the system is stable but with a very low damping factor of 0.446×10^{-3}, which leads to instability under system disturbances. On the same figure, the dominant poles under positive resistive loading conditions and the same system parameters are shown. It is clear that the stability margin is much better even under the overload conditions.

For further analysis and justification, the impedance ratio (Nyquist) criterion is considered. To apply this criterion, the system in Figure 3.4 should be equivalently transferred to the simple circuit shown in Figure 3.7 where Z_s, V_s, Z_l and V_l are the Thevenin equivalent impedance and voltage of the supply and load, respectively. The

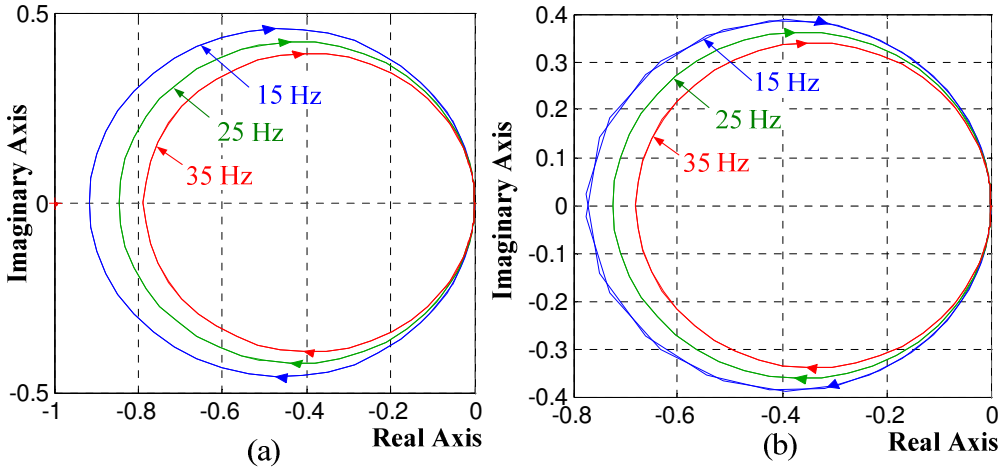

Figure 3.8: Impedance ratio criterion with different dc voltage control bandwidth. (a) Uncompensated system. (b) Composite resistive loading of 0.2pu

impedance ratio analysis will be applied to the small-signal linearized impedance due to the nonlinearity of the source-side.

The small-signal load impedance (ΔZ_l) as seen from the dc-bus is approximated by:

$$\Delta Z_l = \frac{\Delta V_{dc}}{\Delta I_{dc}} = -\frac{V_{dc}^{\circ 2}}{P^{\circ}} \tag{3.15}$$

The small signal source impedance (ΔZ_s) can be obtained by applying small-signal linearization to (3.4) and (3.5) and using (3.13) with $\Delta V_s = \Delta V_d$ as given by:

$$\Delta Z_s = \frac{Ls^3+(R+K_{ip})s^2+K_{ii}s}{\xi_4 s^4+\xi_3 s^3+\xi_2 s^2+\xi_1 s+\xi_0} \tag{3.16}$$

$$\xi_4 = LC$$

$$\xi_3 = C(R+K_{ip}) + \left(\frac{1.5I_d^{\circ}L}{V_{dc}^{\circ}}\right)(D_d^{\circ} - K_{vp}K_{ip}) + \frac{L}{R_d}$$

$$\xi_2 = CK_{ii} + (1.5/V_{dc}^{\circ})\begin{pmatrix} I_d^{\circ}D_d^{\circ}(R+K_{ip}) + (D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R)K_{vp}K_{ip} \\ -I_d^{\circ}L(K_{vp}K_{ii} + K_{ip}K_{vi}) \end{pmatrix} + \frac{R+K_{ip}}{R_d}$$

$$\xi_1 = (1.5/V_{dc}^{\circ})\left((D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R)(K_{vp}K_{ii} + K_{ip}K_{vi}) - I_d^{\circ}LK_{ii}K_{vi} + I_d^{\circ}D_d^{\circ}K_{ii}\right) + \frac{K_{ii}}{R_d}$$

$$\xi_0 = 1.5(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R)K_{ii}K_{vi}/V_{dc}^{\circ}$$

Using (3.15) and (3.16) with $1/R_d = 0$, Nyquist impedance ratio criterion can be

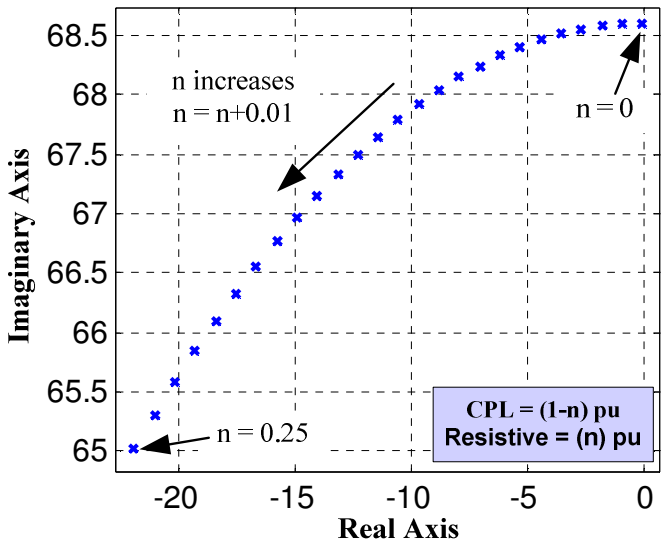

Figure 3.9: Damping effect of composite loading in the dc micro-grid.

investigated. The effect of the dc voltage controller bandwidth on the system stability is studied using this criterion. It is found that the dc voltage controller bandwidth is crucial for system stability as it affects the source impedance, and can violate the impedance ratio requirements. As shown in Figure 3.8(a), Nyquist contours are plotted at different values of the dc voltage controller bandwidth. As the bandwidth increases, the system stability margin increases. However, the dc voltage controller bandwidth is limited and accordingly, using the dc voltage controller to achieve high stability margins with CPL might not be feasible.

As shown in Figure 3.1, a typical dc micro-grid might supply composite loads of about 75%~80% of tightly-regulated PE converters (CPLs) and about 20%~25% of resistive loads [49]. The existence of such resistive loading provides natural passive damping.

Using (3.16) and considering the resistive load (R_d), Figure 3.8(b) shows the Nyquist contours for the impedance ratio along with the effect of the dc voltage controller on the stability margin. The improved stability margin is accomplished by considering a resistive load of 0.2 p.u.

Using the denominator of (3.14) with different values of R_d, Figure 3.9 shows the dominant root-locus of the dc voltage dynamics as the p.u. resistive loading increases from 0 to 0.25. The damping factor of the composite load increases from 0.446×10^{-3} with 1.0 p.u. CPL and zero resistive loading to 0.319 with 0.75 p.u. CPL and 0.25 p.u.

resistive loading. This clearly shows the damping capability of the natural resistive load penetration within the dc micro-grid.

Composite loading of the dc micro-grid shows better damping that compensates for the tight regulation effect; however, the damping obtained is not efficient to guarantee high stability margins. Also, the most optimistic case was considered, that is 20-25% of the dc micro-grid load is resistive. In some applications, dc micro-grid may be totally loaded with motor drives or CILs.

3.5 Proposed Active Damping Techniques in DC Micro-Grids

It has been analytically shown that the VSC micro-grid interface may suffer instabilities or dc-bus voltage oscillations due to the high penetration of tightly-regulated PE converters. This section introduces internal model-based active damping techniques to actively reshape the interface impedance to meet the impedance ratio criterion at different micro-grid loading conditions. To meet this objective, three different active techniques are investigated and evaluated in terms of the active compensation capability, robustness, and effects on the voltage tracking performance. The proposed methods inject active damping signal in the outer, intermediate and inner control loops of the voltage-oriented VSR interface. Since the dc-bus voltage is usually measured, the proposed methods use the dc-bus voltage for active damping control. The utilization of the dc-bus voltage at different loops provides internal model dynamics, where the frequency modes of the dc voltage dynamics can be mapped to the closed loop system. Therefore, dc voltage oscillations can be damped. The damping capability depends on the degree at which the frequency modes are mapped to the closed loop system. Therefore, it depends on the location of the active damping injection within the converter control loops and the interactions among the active damping controller and the converter controller. Theoretical analysis is presented to derive the voltage dynamics, converter output impedance and voltage tracking dynamics under different compensation schemes.

3.5.1 Outer- Loop-Based Active Compensation

In this method, the damping effect is obtained by injecting a scaled version of the dc-link voltage into the outer voltage control loop via a linear compensator and a scaling

gain to shape the converter impedance. A band-limited derivative compensator is used as a linear compensator to extract a scaled band-limited version of the capacitor current; the latter is used to inject a proportional signal in the outer voltage control loop. Equivalently, this technique emulates a virtual resistance and embeds the frequency modes of voltage oscillations in the stable closed loop system; therefore it will be possible to eliminate these oscillations. The active compensation loop is shown in Figure 3.10(a) with a compensator transfer function $C(s)$ with a cut-off frequency ω_c and virtual controller gain R_v.

From Figure 3.10(a), the controller model in (3.13) is modified to:

$$\Delta I_d = -\frac{G_v(s)G_i(s)(1+R_vC(s))}{R+sL+G_i(s)}\Delta V_{dc}\,,$$
$$C(s) = \frac{s}{s+\omega_c} \tag{3.17}$$

Using (3.17) and following similar procedures, the VSR dc voltage dynamics can be given by:

$$\frac{\Delta V_{dc}}{\Delta D_d} = \frac{1.5I_d^{\circ}\left(Ls^4+(\omega_cL+R+K_{ip})s^3+(K_{ii}+(R+K_{ip})\omega_c)s^2+K_{ii}\omega_cs\right)}{a_5s^5+a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \tag{3.18}$$

$a_5 = LC$

$a_4 = \left(R + K_{ip} + \omega_cL\right)C - LP^{\circ}/V_{dc}^{\circ 2}$

$a_3 = C\left(K_{ii} + \left(R + K_{ip}\right)\omega_c\right) - \left(R + K_{ip} + \omega_cL\right)P^{\circ}/V_{dc}^{\circ 2} + 1.5D_d^{\circ}K_{vp}K_{ip}(1 + R_v)$

$a_2 = CK_{ii}\omega_c - \left(K_{ii} + \left(R + K_{ip}\right)\omega_c\right)P^{\circ}/V_{dc}^{\circ 2}$
$\qquad + 1.5D_d^{\circ}\left(K_{vp}K_{ip}\omega_c + \left(K_{vp}K_{ii} + K_{ip}K_{vi}\right)(1 + R_v)\right)$

$a_1 = -K_{ii}\omega_c\,P^{\circ}/V_{dc}^{\circ 2} + 1.5D_d^{\circ}\left(K_{vi}K_{ii}(1 + R_v) + \left(K_{vp}K_{ii} + K_{ip}K_{vi}\right)\omega_c\right)$

$a_0 = 1.5D_d^{\circ}K_{vi}K_{ii}\omega_c$

The output impedance of the actively compensated VSC can be given by:

$$\Delta Z_s = \frac{Ls^4+\left(R+K_{ip}+\omega_cL\right)s^3+\left(K_{ii}+\left(R+K_{ip}\right)\omega_c\right)s^2+K_{ii}\omega_cs}{\alpha_5s^5+\alpha_4s^4+\alpha_3s^3+\alpha_2s^2+\alpha_1s+\alpha_0} \tag{3.19}$$

$\alpha_5 = LC$

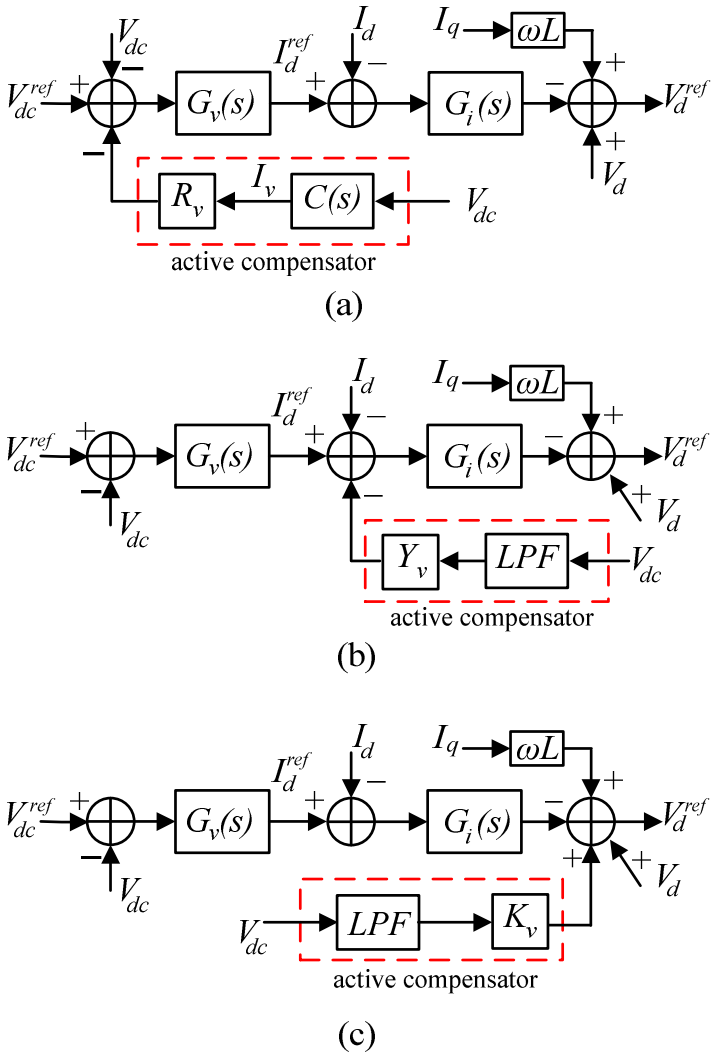

Figure 3.10: Proposed active compensators for VSR interfacing dc micro-grid. (a) Outer. (b) Intermediate. (c) Inner loop compensator.

$$\alpha_4 = \left(R + K_{ip} + \omega_c L\right)C + \left(1.5I_d^\circ L/V_{dc}^\circ\right)\left(D_d^\circ - K_{vp}K_{ip}(1 + R_v)\right)$$

$$\alpha_3 =$$

$$C\left(K_{ii} + \left(R + K_{ip}\right)\omega_c\right) +$$

$$\left(1.5/V_{dc}^\circ\right)\begin{pmatrix} I_d^\circ D_d^\circ\left(R + K_{ip} + \omega_c L\right) + \left(D_d^\circ V_{dc}^\circ - I_d^\circ R\right)(1 + R_v)K_{vp}K_{ip} \\ -I_d^\circ L\left(K_{vp}K_{ip}\omega_c + \left(K_{vp}K_{ii} + K_{ip}K_{vi}\right)(1 + R_v)\right) \end{pmatrix}$$

$$\alpha_2 =$$

$$CK_{ii}\omega_c + \frac{1.5}{V_{dc}^{\circ}}\begin{pmatrix} I_d^{\circ}D_d^{\circ}\begin{pmatrix} K_{ii} \\ +(R+K_{ip})\omega_c \end{pmatrix} + \left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)\begin{pmatrix} (K_{vp}K_{ii}+K_{ip}K_{vi})\times \\ (1+R_v)+K_{vp}K_{ip}\omega_c \end{pmatrix} \\ -I_d^{\circ}L\left(K_{ii}K_{vi}(1+R_v)+(K_{vp}K_{ii}+K_{ip}K_{vi})\omega_c\right) \end{pmatrix}$$

$$\alpha_1 = \left(1.5/V_{dc}^{\circ}\right)\begin{pmatrix} I_d^{\circ}D_d^{\circ}K_{ii}\omega_c + \left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)\times \\ \left((K_{vp}K_{ii}+K_{ip}K_{vi})\omega_c + K_{ii}K_{vi}(1+R_v)\right) \end{pmatrix} - I_d^{\circ}LK_{ii}K_{vi}\omega_c$$

$$\alpha_0 = \left(1.5/V_{dc}^{\circ}\right)\left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)K_{ii}K_{vi}\omega_c$$

3.5.2 Intermediate- Loop-Based Active Compensation

In this method, the dc-bus voltage is measured and multiplied by a virtual admittance to obtain a scaled time-domain version of the dc-link disturbance that is included in the reference current generation stage as an internal model. The damping signal is subtracted from the *d*- axis component of the reference current. Since the active damping injection is used at the current reference node, a virtual admittance is yielded. A low pass filter (LPF) is also used to eliminate dc-bus voltage ripples and control the compensation bandwidth. The modified current reference is then applied to the current controller to obtain the compensated voltage reference. Figure 3.10(b) shows a schematic of the intermediate-loop-based active compensator with a LPF with a cut-off frequency of ω_Y, whereas Y_v is the virtual admittance.

Using the intermediate-loop-based active compensator, the controller model in (3.13) is modified to:

$$\Delta I_d = -\frac{G_i(s)\left(G_v(s)+Y_v\frac{\omega_Y}{s+\omega_Y}\right)}{R+sL+G_i(s)}\Delta V_{dc} \tag{3.20}$$

Accordingly, the dc-bus voltage dynamics can be given by:

$$\frac{\Delta V_{dc}}{\Delta D_d} = \frac{1.5I_d^{\circ}\left(Ls^4+(\omega_Y L+R+K_{ip})s^3+(K_{ii}+(R+K_{ip})\omega_Y)s^2+K_{ii}\omega_Y s\right)}{b_5s^5+b_4s^4+b_3s^3+b_2s^2+b_1s+b_0} \tag{3.21}$$

$$b_5 = LC$$

$$b_4 = \left(R+K_{ip}+\omega_Y L\right)C - LP^{\circ}/V_{dc}^{\circ 2}$$

$$b_3 = C\left(K_{ii}+\left(R+K_{ip}\right)\omega_Y\right) - \left(R+K_{ip}+\omega_Y L\right)P^{\circ}/V_{dc}^{\circ 2} + 1.5D_d^{\circ}K_{ip}\left(Y_v\omega_Y + K_{vp}\right)$$

$$b_2 = CK_{ii}\omega_Y - \left(K_{ii} + \left(R + K_{ip}\right)\omega_Y\right)P^{\circ}/V_{dc}^{\circ 2} + 1.5D_d^{\circ}\begin{pmatrix}K_{vp}K_{ip}\omega_Y + K_{vp}K_{ii}\\ +K_{ip}K_{vi} + K_{ii}Y_v\omega_Y\end{pmatrix}$$

$$b_1 = -K_{ii}\omega_Y P^{\circ}/V_{dc}^{\circ 2} + 1.5D_d^{\circ}\left(K_{vi}K_{ii} + \left(K_{vp}K_{ii} + K_{ip}K_{vi}\right)\omega_Y\right)$$

$$b_0 = 1.5D_d^{\circ}K_{vi}K_{ii}\omega_Y$$

The output impedance of the VSC with this active damping method is given by:

$$\Delta Z_s = \frac{Ls^4 + \left(R + K_{ip} + \omega_Y L\right)s^3 + \left(K_{ii} + \left(R + K_{ip}\right)\omega_Y\right)s^2 + K_{ii}\omega_Y s}{\beta_5 s^5 + \beta_4 s^4 + \beta_3 s^3 + \beta_2 s^2 + \beta_1 s + \beta_0} \tag{3.22}$$

$$\beta_5 = LC$$

$$\beta_4 = \left(R + K_{ip} + \omega_Y L\right)C + \left(1.5I_d^{\circ}L/V_{dc}^{\circ}\right)\left(D_d^{\circ} - K_{vp}K_{ip} - Y_v K_{ip}\omega_Y\right)$$

$$\beta_3 =$$

$$C\left(K_{ii} + \left(R + K_{ip}\right)\omega_Y\right) + \frac{1.5}{V_{dc}^{\circ}}\begin{pmatrix}\left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)\begin{pmatrix}K_{vp}K_{ip}\\ +Y_v K_{ip}\omega_Y\end{pmatrix}\\ I_d^{\circ}D_d^{\circ}\left(R + K_{ip} + \omega_Y L\right) - I_d^{\circ}L\begin{pmatrix}K_{vp}K_{ip}\omega_Y + K_{vp}K_{ii}\\ +K_{ip}K_{vi} + Y_v K_{iI}\omega_Y\end{pmatrix}\end{pmatrix}$$

$$\beta_2 =$$

$$CK_{ii}\omega_Y + \frac{1.5}{V_{dc}^{\circ}}\begin{pmatrix}I_d^{\circ}D_d^{\circ}\begin{pmatrix}K_{ii}\\ +\left(R + K_{ip}\right)\omega_Y\end{pmatrix} + \left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)\begin{pmatrix}K_{vp}K_{ii} + K_{ip}K_{vi}\\ +Y_v\omega_Y K_{ii} + K_{vp}K_{ip}\omega_Y\end{pmatrix}\\ -I_d^{\circ}L\left(K_{ii}K_{vi} + \left(K_{vp}K_{ii} + K_{ip}K_{vi}\right)\omega_Y\right)\end{pmatrix}$$

$$\beta_1 = \left(1.5/V_{dc}^{\circ}\right)\left(I_d^{\circ}D_d^{\circ}K_{ii}\omega_Y + \left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)\begin{pmatrix}K_{ii}K_{vi}\\ +\left(K_{vp}K_{ii} + K_{ip}K_{vi}\right)\omega_Y\end{pmatrix}\right)$$
$$-I_d^{\circ}LK_{ii}K_{vi}\omega_Y$$

$$\beta_0 = \left(1.5/V_{dc}^{\circ}\right)\left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)K_{ii}K_{vi}\omega_Y$$

3.5.3 Inner- Loop-Based Active Compensation

In this method, the active damping signal is a low-pass-filtered scaled version of the dc-bus voltage that is directly injected to the modulator of the VSR. The active damping signals maps the dc voltage dynamics as internal model within the converter-reference voltage generation stage. Figure 3.10(c) shows a schematic of the inner-loop-based active compensator with a first order LPF with a cut-off frequency of ω_K and scaling gain K_v.

Using the inner-loop-based active compensator, the controller model in (3.13) is modified to:

$$\Delta I_d = -\frac{G_v(s)G_i(s)+K_v\frac{\omega_K}{s+\omega_K}}{R+sL+G_i(s)}\Delta V_{dc} \tag{3.23}$$

Accordingly, the dc-bus voltage dynamics can be given by:

$$\frac{\Delta V_{dc}}{\Delta D_d} = \frac{1.5I_d^\circ\left(Ls^4+\left(\omega_K L+R+K_{ip}\right)s^3+\left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right)s^2+K_{ii}\omega_K s\right)}{c_5s^5+c_4s^4+c_3s^3+c_2s^2+c_1s+c_0} \tag{3.24}$$

$$c_5 = LC$$

$$c_4 = \left(R+K_{ip}+\omega_K L\right)C - LP^\circ/V_{dc}^{\circ 2}$$

$$c_3 = C\left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right) - \left(R+K_{ip}+\omega_K L\right)P^\circ/V_{dc}^{\circ 2} + 1.5D_d^\circ K_{vp}K_{ip}$$

$$c_2 = CK_{ii}\omega_K - \left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right)P^\circ/V_{dc}^{\circ 2} + 1.5D_d^\circ\left(K_{vp}K_{ip}\omega_K + K_{vp}K_{ii} + K_{ip}K_{vi} + K_v\omega_K\right)$$

$$c_1 = -K_{ii}\omega_K P^\circ/V_{dc}^{\circ 2} + 1.5D_d^\circ\left(K_{vi}K_{ii} + \left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\omega_K\right)$$

$$c_0 = 1.5D_d^\circ K_{vi}K_{ii}\omega_K$$

The output impedance of the VSC with this compensator is given as follows:

$$\Delta Z_s = \frac{-Ls^4-\left(R+K_{ip}+\omega_K L\right)s^3-\left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right)s^2-K_{ii}\omega_K s}{\gamma_5s^5+\gamma_4s^4+\gamma_3s^3+\gamma_2s^2+\gamma_1s+\gamma_0} \tag{3.25}$$

$$\gamma_5 = LC$$

$$\gamma_4 = \left(R+K_{ip}+\omega_K L\right)C + \left(1.5I_d^\circ L/V_{dc}^\circ\right)\left(D_d^\circ - K_{vp}K_{ip}\right)$$

$$\gamma_3 = C\left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right) + \frac{1.5}{V_{dc}^\circ}\begin{pmatrix} I_d^\circ D_d^\circ\left(R+K_{ip}+\omega_K L\right) + \left(D_d^\circ V_{dc}^\circ - I_d^\circ R\right)K_{vp}K_{ip} \\ -I_d^\circ L\left(K_{vp}K_{ip}\omega_K + K_{vp}K_{ii} + K_{ip}K_{vi} + K_v\omega_K\right)\end{pmatrix}$$

$$\gamma_2 = CK_{ii}\omega_K + \frac{1.5}{V_{dc}^\circ}\begin{pmatrix} \left(D_d^\circ V_{dc}^\circ - I_d^\circ R\right)\begin{pmatrix} K_{vp}K_{ii}+K_{ip}K_{vi} \\ +K_v\omega_K + K_{vp}K_{ip}\omega_K\end{pmatrix} \\ I_d^\circ D_d^\circ\left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right) - I_d^\circ L\begin{pmatrix} K_{ii}K_{vi} \\ +\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\omega_K\end{pmatrix}\end{pmatrix}$$

$$\gamma_1 = \frac{1.5}{V_{dc}^\circ}\left(I_d^\circ D_d^\circ K_{ii}\omega_K + \left(D_d^\circ V_{dc}^\circ - I_d^\circ R\right)\begin{pmatrix} K_{ii}K_{vi} \\ +\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\omega_K\end{pmatrix}\right) - I_d^\circ LK_{ii}K_{vi}\omega_K$$

$$\gamma_0 = \left(1.5/V_{dc}^{\circ}\right)\left(D_d^{\circ}V_{dc}^{\circ} - I_d^{\circ}R\right)K_{ii}K_{vi}\omega_K$$

3.6 Performance Comparison of The Proposed Active Damping Techniques

In this section, the performance of the proposed active compensation methods is compared in terms of their damping capabilities and the corresponding drawbacks and tradeoffs.

3.6.1 Compensator Design and Damping Capabilities

Using the dc voltage dynamics with active damping control in (3.18), (3.21), (3.24), the loci of the dominant pole under 1.0 p.u. CPL conditions and at variable compensator design parameters are shown in Figure 3.11. For each active damping method, the compensator gain and the cut-off frequency are varied to design the compensator parameters. The design criteria are to maximize the damping capabilities and to minimize the dynamic interactions between the active damping compensator and the converter controllers. The interactions dynamics can be assessed using the voltage-tracking dynamics with active damping control as given by:

$$\frac{V_{dc}}{V_{dc}^{ref}} = \frac{1.5D_d\left(K_{vp}K_{ip}s^3+\left(K_{vp}K_{ip}\omega_c+K_{vp}K_{ii}+K_{ip}K_{vi}\right)s^2+\left(K_{ii}K_{vi}+\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\omega_c\right)s+\omega_cK_{ii}K_{vi}\right)}{\begin{bmatrix} LCs^5+\left(R+K_{ip}+\omega_cL\right)Cs^4+\left(C\left(K_{ii}+\left(R+K_{ip}\right)\omega_c\right)+1.5D_dK_{vp}K_{ip}\right)s^3 \\ +\left(1.5D_d^{\circ}\left(K_{vp}K_{ip}\left(\omega_c+R_v\right)+K_{vp}K_{ii}+K_{ip}K_{vi}\right)+C\omega_cK_{ii}\right)s^2 \\ +\left(1.5D_d^{\circ}\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\left(\omega_c+R_v\right)+K_{ii}K_{vi}\right)s+1.5D_d^{\circ}K_{vi}K_{ii}\left(\omega_c+R_v\right) \end{bmatrix}} \tag{3.26}$$

$$\frac{V_{dc}}{V_{dc}^{ref}} = \frac{1.5D_d\left(K_{vp}K_{ip}s^3+\left(K_{vp}K_{ip}\omega_Y+K_{vp}K_{ii}+K_{ip}K_{vi}\right)s^2+\left(K_{ii}K_{vi}+\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\omega_Y\right)s+\omega_YK_{ii}K_{vi}\right)}{\begin{bmatrix} LCs^5+\left(R+K_{ip}+\omega_YL\right)Cs^4+\left(C\left(K_{ii}+\left(R+K_{ip}\right)\omega_Y\right)+1.5D_dK_{vp}K_{ip}\right)s^3 \\ +\left(1.5D_d^{\circ}\left(K_{vp}K_{ip}\omega_Y+K_{vp}K_{ii}+K_{ip}K_{vi}+Y_v\omega_YK_{ip}\right)+C\omega_YK_{ii}\right)s^2 \\ +1.5D_d^{\circ}\left(\omega_Y\left(Y_vK_{ii}+K_{ip}K_{vi}+K_{vp}K_{ii}\right)+K_{vi}K_{ii}\right)s+1.5D_d^{\circ}K_{vi}K_{ii}\omega_Y \end{bmatrix}} \tag{3.27}$$

$$\frac{V_{dc}}{V_{dc}^{ref}} = \frac{1.5D_d\left(K_{vp}K_{ip}s^3+\left(K_{vp}K_{ip}\omega_K+K_{vp}K_{ii}+K_{ip}K_{vi}\right)s^2+\left(K_{ii}K_{vi}+\left(K_{vp}K_{ii}+K_{ip}K_{vi}\right)\omega_K\right)s+\omega_KK_{ii}K_{vi}\right)}{\begin{bmatrix} LCs^5+\left(R+K_{ip}+\omega_KL\right)Cs^4+\left(C\left(K_{ii}+\left(R+K_{ip}\right)\omega_K\right)+1.5D_dK_{vp}K_{ip}\right)s^3 \\ +\left(1.5D_d^{\circ}\left(K_{vp}K_{ip}\omega_K+K_{vp}K_{ii}+K_{ip}K_{vi}-\omega_KK_v\right)+C\omega_KK_{ii}\right)s^2 \\ +1.5D_d^{\circ}\left(\omega_K\left(K_{ip}K_{vi}+K_{vp}K_{ii}\right)+K_{vi}K_{ii}\right)s+1.5D_d^{\circ}K_{vi}K_{ii}\omega_K \end{bmatrix}} \tag{3.28}$$

where (3.26)–(3.28) for the outer-, intermediate-, and inner-loop-based compensators, respectively.

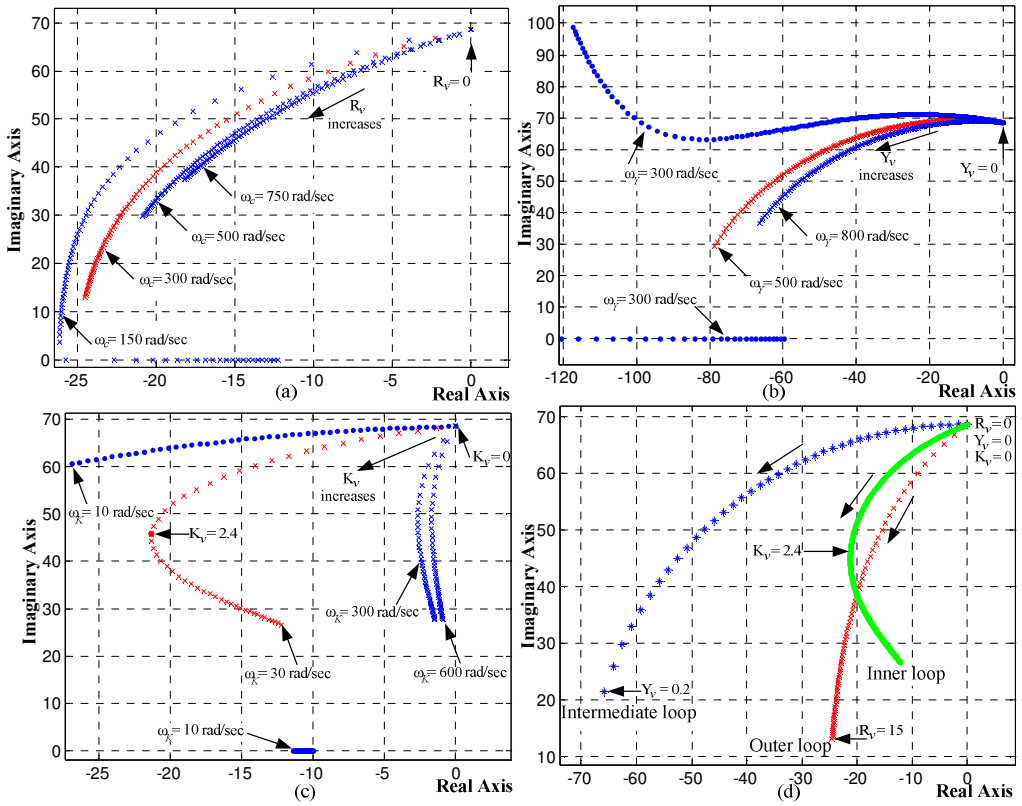

Figure 3.11: Damping effect of the proposed active compensators with 1.0 p.u. CPL. (a) Outer loop. (b) Intermediate loop. (c) Inner loop. (d) All loops.

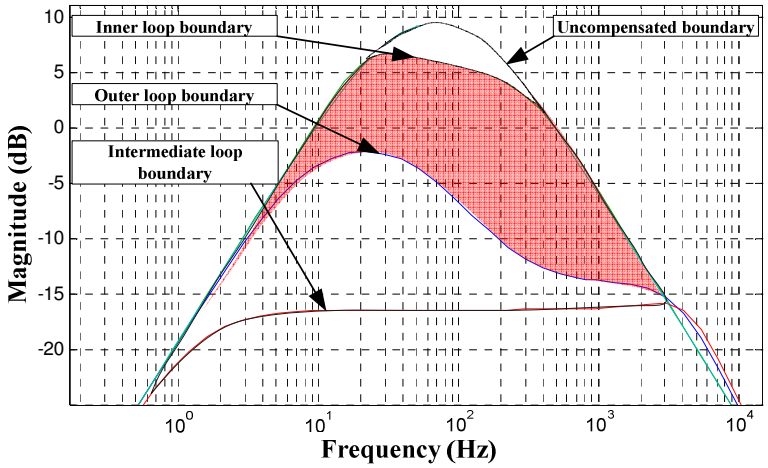

Figure 3.12: Source impedance reduction range with different active compensators.

Figure 3.11(d) shows the root loci of all active damping methods with optimized cut-off frequencies ($\omega_c = \omega_Y = 300\,rad/sec$ and $\omega_K = 30\,rad/sec$) and variable gains. It is clear that the intermediate-loop-based active compensator has the best damping capabilities among these methods. The outer loop based active compensator comes next, whereas the inner loop method has the lowest damping capabilities (maximum damping of 0.5). The difference among damping capabilities of different methods can be referred to the effectiveness of each method to map the frequency modes of the dc-bus voltage as an internal model with the closed loop converter control system. Also, depending on the location of the active damping signal injection, interactions between the active damping controller and converter controllers are yielded and affect the compensation capability.

The main function of the active damping controller is to reshape the source impedance to meet the impedance ratio criterion. Figure 3.12 shows the possible reduction range of the source input impedance that can be actively produced by each compensator. The source impedance magnitude can be widely reduced with the intermediate loop compensator; the range is narrower with the outer loop based compensator. For the inner loop compensator, the modification range is significantly reduced reflecting the restricted damping capabilities of this compensator. This analysis indicates that the converter current control loop has the highest effect in shaping the converter output impedance. Therefore, the intermediate loop compensator yields the best shaping performance.

3.6.2 Sensitivity to the DC Voltage Controller Bandwidth

The effect of the dc voltage controller bandwidth on the active impedance ratios are shown in Figure 3.13 at three values of the dc voltage controller bandwidth. The active damping methods are designed to yield a damping factor of 0.5; this can be achieved with the following gains: R_v = 4.7, Y_v = 0.099 and K_v = 2.4. Figure 3.13(a) shows the performance of the outer loop compensator. The compensation performance is investigated using Nyquist impedance ratio criterion. Using (3.15), (3.19), (3.22) and (3.25), the contour encirclements indicate high stability margins of this controller as compared to the uncompensated system. However, the encirclement points immigrate through a wide stability range as the bandwidth changes indicating relatively high

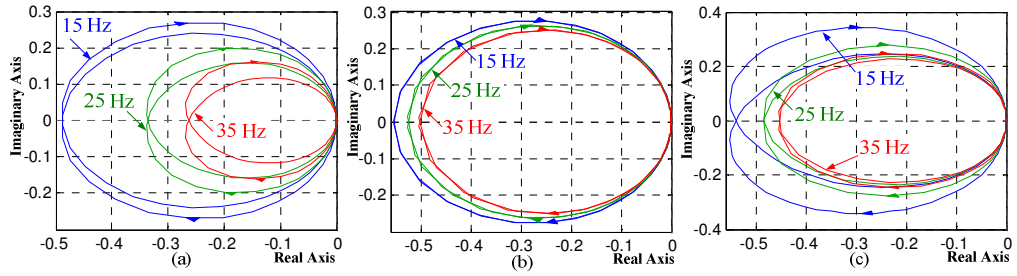

Figure 3.13: Impedance ratio criterion with different dc voltage control loop bandwidth. (a) Outer loop active compensator ($R_v = 4.7$). (b) Intermediate loop active compensator ($Y_v = 0.099$). (c) Inner loop active compensator ($K_v = 2.4$).

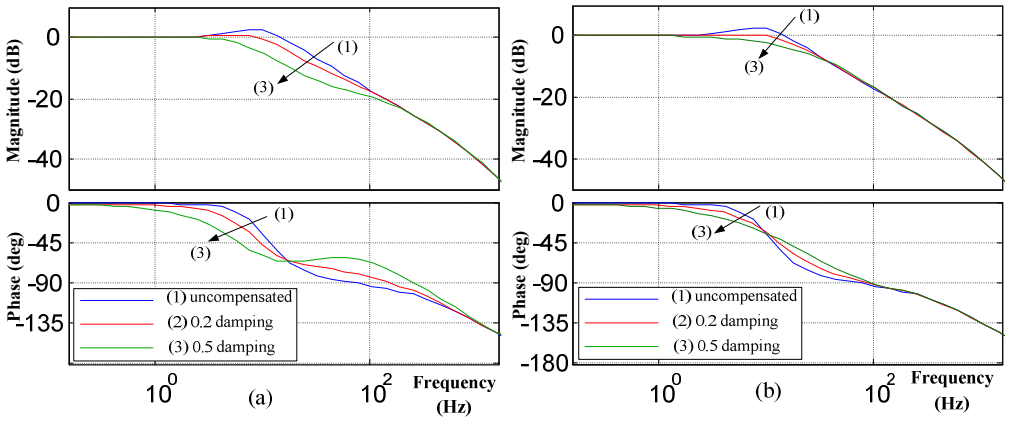

Figure 3.14: Frequency response of the closed loop transfer function for dc voltage tracking. (a) Outer loop compensator. (b) Intermediate loop compensator.

dynamic coupling among the active damping and voltage controllers despite maintaining the system stability. Figure 3.13(b) shows the performance of the intermediate loop compensator, which indicates less sensitivity to variations in the voltage controller bandwidth, and hence, the dynamic coupling among active damping and voltage controllers is reduced as compared to the outer-loop-based method. Figure 3.13(c) shows the performance of the inner loop compensator. The stability margin is the lowest due to the limited damping capabilities. Contour encirclements indicate less sensitivity to variations in the dc voltage controller bandwidth as compared to the outer loop compensator.

3.6.3 DC-Bus Voltage Tracking

Another comparison aspect that should be considered is the effect of the active compensation loops on the dc-bus voltage tracking performance. The modified tracking transfer functions can be obtained using block diagram reductions and are

TABLE 3.1
DC Micro-grid Loads in the Simulated Model

Loads	Load 1	Load 2	Load 3	Load 4	Load 5	Load 6
Type	PMSM drive		Converter fed load			Heating
Interface to the DC grid	Dc-Ac PWM converter		Dc-Dc buck converter			Direct
Ratings[kW]	6.1	2.25	1	1	1.4	0.75

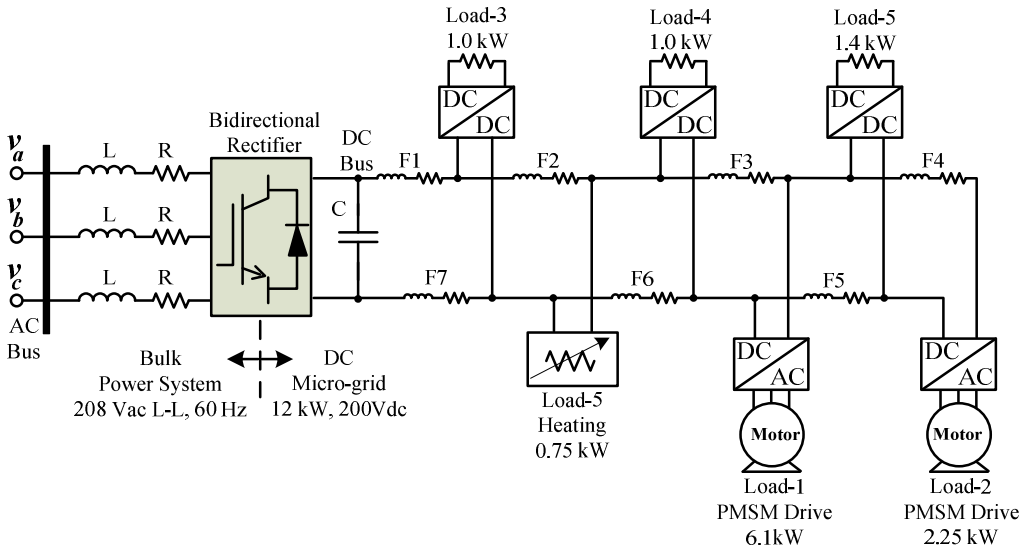

Figure 3.15: Implemented dc micro-grid system.

given in (3.26)–(3.28). Figure 3.14 shows the frequency response of the closed loop voltage tracking dynamics for the intermediate- and outer-loop-based active compensators as they offer high damping capabilities. The uncompensated voltage controller bandwidth is selected to be 20 Hz.

The intermediate loop compensator shows relatively high decoupled performance. With 0.2 and 0.5 damping, the effective voltage bandwidth is reduced to be 19 and 13 Hz, respectively. The outer loop compensator yields stronger dynamic coupling among the active damping and the voltage controller; and hence, under the same damping coefficients, the effective bandwidth is reduced to 15 and 8 Hz, respectively.

3.7 Evaluation Results

To evaluate the performance of the proposed active damping schemes, a low-voltage dc micro-grid study system – shown in Figure 3.15 – is implemented under the

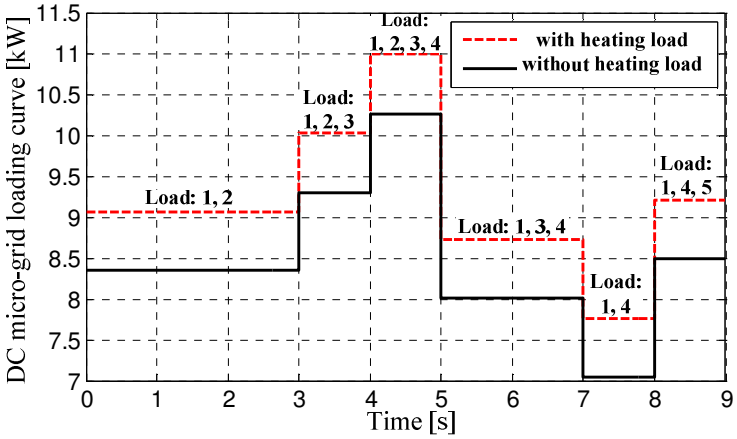

Figure 3.16: Aggregated load curve for a dc micro-grid as seen to the interfacing controlled VSC.

Matlab/Simulink® environment. The dc micro-grid model operates with a main dc-bus voltage of 200V and power ratings of 12 kW. The VSR interface and active compensators parameters are given in Appendix A3.3. Using the preceding analysis, the compensator gains are selected to optimize the damping performance and the dynamic interactions between the active compensator and voltage controller dynamics. The loads considered in this model are two PMSM drives, three dc-dc converter-fed loads and a heating load. The PE interfaced loads are tightly-regulated to achieve the required control objective. For the PMSM drive, the drive objective is to maintain the motor speed to 1500 rpm (157.08 rad/s), whereas for the dc-dc converter-fed loads, the control objective is to maintain the load-side voltage level at 100V. Table 3.1 depicts the dc micro-grid loads with their ratings and characteristics.

Figure 3.16 shows the loading curve for the dc micro-grid with and without the heating load. The loading scenario is characterized by sudden loading and unloading and varying the load mix to evaluate the system stability under dynamic loading conditions. For the sake of performance comparison, the following cases are presented.

3.7.1 Uncompensated System

The loading scenario in Figure 3.16 is applied without active compensation and without the heating load. The dc-bus voltage and total injected current responses are shown in Figure 3.17(a) and (b). The effect of tight regulation decreases the stability margins of the dc-bus voltage dynamics, and eventually instability can be yielded. This is obvious in Figure 3.17(a), when load-5 is applied at t=8 s. In spite the fact that the

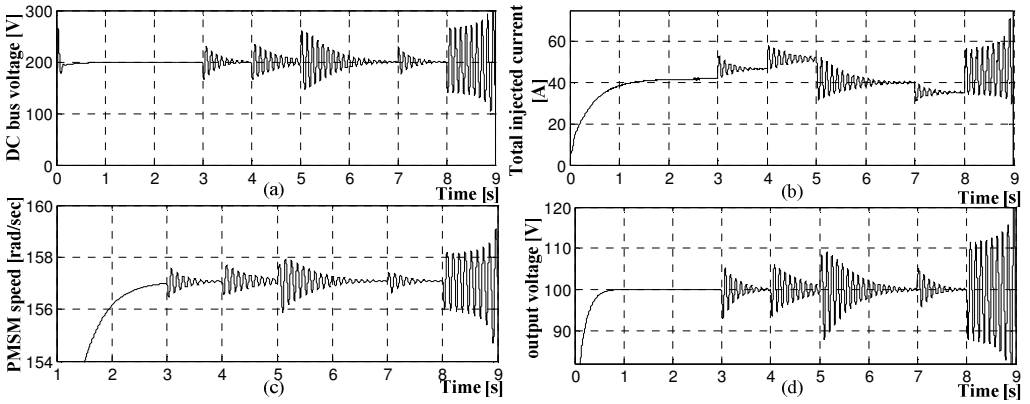

Figure 3.17: Uncompensated VSR micro-grid interface. (a) Dc-bus voltage. (b) Total injected dc current. (c), (d) Load performance: PMSM speed; and dc-dc converter output voltage.

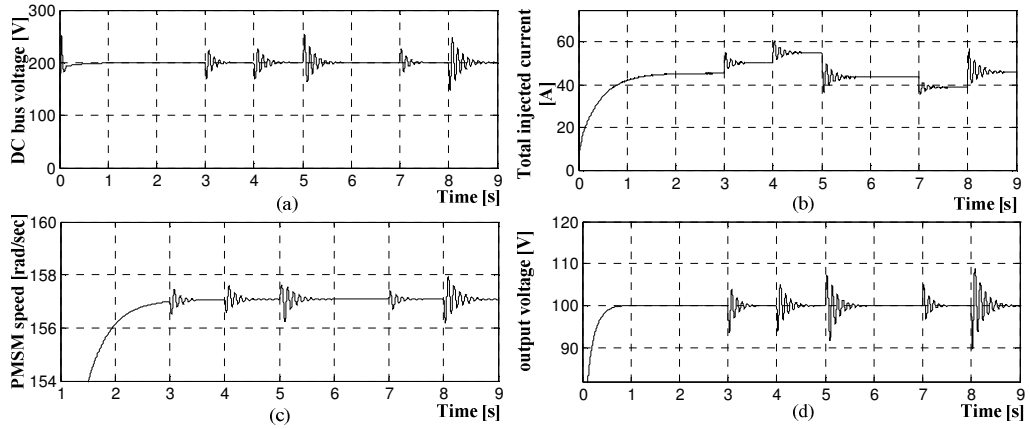

Figure 3.18: Compositely-loaded VSR micro-grid interface. (a) Dc-bus voltage. (b) Total injected dc current. (c), (d) Load performance: PMSM speed; and dc-dc converter output voltage.

total micro-grid loading level is 0.61 p.u. for $t \geq 8$ s, instability is yielded due the increased penetration of the tightly-regulated loads. Mutual interactions between micro-grid loads and the micro-grid interface are yielded via the dc-bus voltage dynamics. Figure 3.17(c) shows the speed response of the PMSM drive (load-1), whereas Figure 3.17(d) shows the dc voltage level of the dc-dc converter (load-3). It is clear that the load-side performance is significantly degraded due to the tight regulation effect reflected to the dc-bus voltage dynamics.

3.7.2 Compositely-Loaded DC Micro-grid

The loading scenario in Figure 3.16 is applied without active compensation and with the heating load. The dc-bus voltage and current responses are shown in Figure

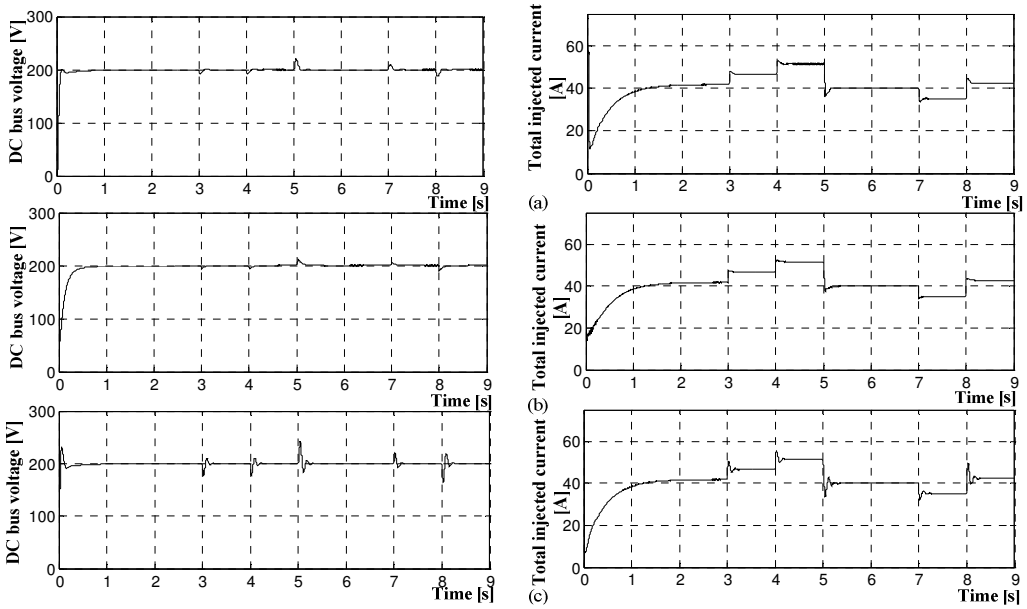

Figure 3.19: Actively compensated dc-bus response– Left: dc-bus voltage, Right: Total injected dc current. (a) Outer loop compensator. (b) Intermediate loop compensator. (c) Inner loop compensator.

3.18(a), (b); as expected, improved damping response is yielded due to the natural passive damping of the resistive load; however, considerable oscillations with high overshoots still exist. The dc-bus voltage start-up overshoot is around 0.3 p.u. The light damping effect adversely affects the load-side performance, as shown in Figure 3.18(c), (d), which shows the PMSM speed response (load-1) and the output voltage of the buck converter (load-3).

3.7.3 Actively-Compensated DC Micro-grid

The effectiveness of the active compensation techniques are investigated under the loading scenario in Figure 3.16 without the heating load (worst loading condition). Figure 3.19 shows the damped dc-bus voltage and currents under each of the three active compensators. The damping capabilities of each compensator meet the theoretical analysis. The outer-loop-based compensator gives better response with a dc-bus voltage start-up overshot of 0.03 p.u. as shown in Figure 3.19(a).

The intermediate-loop-based compensator gives the best damping at the expense of slower rise time as shown in Figure 3.19(b). The inner-loop-based-compensator has the lowest damping capability as shown in the voltage and current response in Figure 3.19(c), where the dc voltage start-up has an overshot of 0.13 p.u. It can be also noted

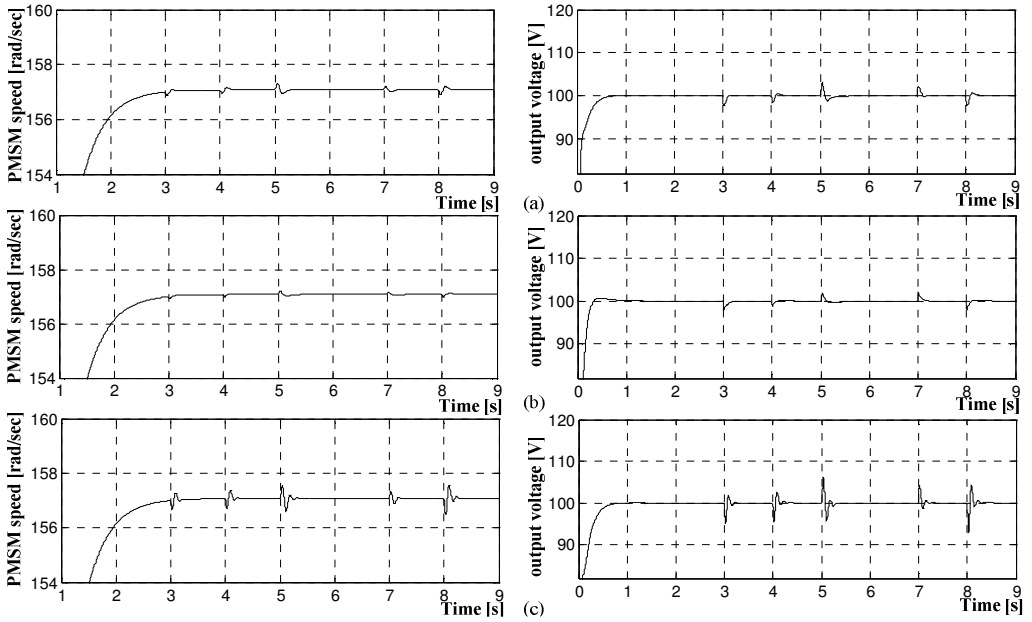

Figure 3.20: Load performance in the actively damped dc micro-grid – Left: PMSM speed, Right: dc-dc converter output voltage. (a) Outer loop compensator. (b) Intermediate loop compensator. (c) Inner loop compensator.

that the outer and intermediate compensators show high robustness against operating point variation. This indicates the effectiveness of these linear compensators in dealing with the nonlinear dc-bus voltage dynamics in a typical dc micro-grid, and hence, a computationally-efficient solution can be adopted. The damping characteristics are reflected to the load performance. Figure 3.20 shows the speed response of the PMSM (load-1) and the dc output voltage of load-3 for each compensator. The load-side performance is remarkably improved, even with the inner-loop-based compensator. It can be also seen that active damping control remarkably improves the disturbance rejection performance, where voltage perturbations are minimized under sudden changes in the load profile. This result is in-line with the internal model principle, where voltage disturbances can be effectively mapped to the closed loop control system via the active damping controller. In spite of the linear nature of the proposed controllers, their performance under the large-signal sense (e.g. during the staring phase with a step change in the voltage command from 0 to 200 V at $t = 0$) is robust as shown in Figure 3.19.

3.8 Conclusion

This Chapter has addressed dc micro-grid stability under high penetration of tightly-regulated PE converters; and proposed three simple and computationally efficient active damping solutions that can be implemented to stabilize a controlled VSC interfacing a dc micro-grid to an ac system. The proposed active damping methods depend on reshaping the VSC impedance by injecting internal-model-based active damping signal at the outer, intermediate and inner control loops of the voltage-oriented VSC interface. Theoretical and evaluation results have indicated that:

- The outer- and intermediate-loop-based compensators offer high damping capabilities, whereas the inner-loop-based compensator has limited damping characteristics.
- The inner-loop compensator has the highest influence on the dc voltage controller performance; the outer-loop compensator has higher influence on the dc voltage controller performance as compared to the intermediate-loop compensator.
- Under the same damping factor, the intermediate loop compensator offers the highest robustness against dc voltage controller bandwidth variation; the inner loop compensator is relatively robust whereas the outer loop compensator is not.
- Strong coupling and interaction dynamics among the dc micro-grid loads affect the load performance itself, not only the dc-bus voltage.
- Active damping techniques can preserve micro-grid stability and improve the load performance by mitigating dynamic interactions and improves the disturbance rejection.

Chapter 4

Modeling, Analysis and Stabilization of Converter-Fed AC Micro-grids with High Penetration of Converter-Interfaced Loads[1]

4.1 Introduction

This Chapter addresses ac micro-grid stability under high penetration of tightly-regulated CILs; and proposes different active damping solutions that can be implemented either from the load- or the source-side to stabilize the overall system at the common point of interactions. Two scenarios for interaction dynamics instabilities will be considered in this Chapter:

- A CIL consisting of a tightly-regulated VSR to supply a resistive load. The control objective is to maintain the output dc voltage at the required value. Admittance-based analysis is conducted to obtain the small-signal input admittance of the VSR. LSC will be proposed to actively reshape the input admittance of VSR so that the Nyquist criterion is maintained.
- In case of high uncertainties at the load-side, a generic model of augmented CILs will be considered; that is an incremental negative resistance only depending on the drawn load power and ignoring the load dynamics. Proposed compensators from the source-side will be provided to actively reshape the source admittance of the ac micro-grid interface (VSI) so that the Nyqusit admittance ratio criterion is maintained. Small-signal analysis is conducted to assess the system stability under different compensation schemes. Sensitivity and robustness analyses will be presented to assess the dynamic coupling among active damping and voltage

[1] *Publications out of this Chapter:*

A. A. A. Radwan and Y. A.-R. I. Mohamed, "Modeling, analysis and stabilization of converter-fed ac micro-grids with high penetration of converter-interfaced loads," Accepted with minor revisions in *IEEE Transactions on Smart Grids* [Manuscript ID: TSG-00253-2011].

A. A. A. Radwan and Y. A.-R. I. Mohamed, "Load- and Source-Side Active Stabilization of DG Micro-grid Supplying Converter-Fed Loads," Submitted for publication in *2012 IEEE Power & Energy Society General Meeting*, ID: 2012GM0148.

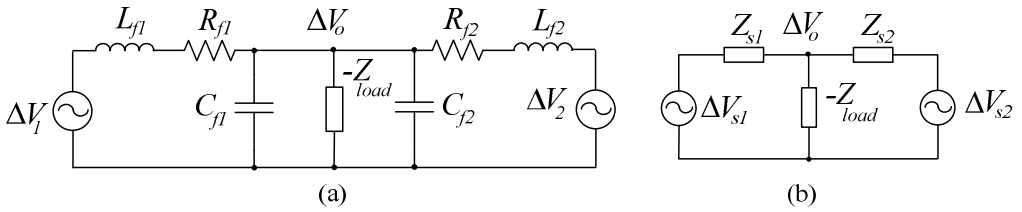

Figure 4.1: DG system. (a) Equivalent small-signal model. (b) Simplified model.

tracking controllers. The SSC technique is generic, efficient and load-independent as compared to LSC.

Throughout this Chapter, the actively compensated admittances from the load- or the source-side and the modified control dynamics are provided. Evaluation results, based on a detailed and exact model of ac micro-grid with multiple tightly-regulated CILs, are provided to validate the developed models and demonstrate the effectiveness and robustness of proposed techniques.

4.2 Stability Analysis of AC Micro-grids

Without loss of generality, a two-inverter ac micro-grid supplying a common aggregated load is used for the stability study [114]. The aggregated load represents high penetration of tightly-regulated CILs, or equivalently, a negative resistance in small-signal sense ($-Z_{load}$). Using the Routh-Hurwitz stability criterion [22], stability conditions is provided in terms of the physical system parameters.

Figure 4.1(a) shows the equivalent small-signal of the two-unit DG micro-grid system, whereas Figure 4.1(b) shows a simplified model from which the source impedance (Z_{s1}) and the equivalent Thevenin voltage (V_{s1}) are given by:

$$Z_{s1} = \frac{R_{f1}+sL_{f1}}{C_{f1}L_{f1}s^2+R_{f1}C_{f1}s+1} \tag{4.1}$$

$$\Delta V_{s1} = \Delta V_o \frac{1/sC_{f1}}{R_{f1}+L_{f1}s+1/sC_{f1}} \tag{4.2}$$

where V_{s1} is the terminal voltage of the DG inverter; R_{f1}, L_{f1} and C_{f1} are the equivalent resistance, inductance and capacitance of the ac input filter while V_o is the ac-bus common voltage; Δ represents small perturbations around the operating point. For the second DG units, similar equations can be written.

Using Kirchhoff current law gives:

$$\Delta V_o(1/Z_{s1} + 1/Z_{s2} - 1/Z_{load}) = \Delta V_{s1}/Z_{s1} + \Delta V_{s2}/Z_{s2} \tag{4.3}$$

Applying superposition:

$$\Delta V_o(1/Z_{s1} + 1/Z_{s2} - 1/Z_{load}) = \Delta V_{s1}/Z_{s1} \tag{4.4}$$

where (4.4) is also the same for unit 2.

Using (4.2)–(4.4), the transfer function between the output/input voltages for unit 1 is obtained as follows:

$$\frac{\Delta V_o}{\Delta V_1} = \frac{R_{f2}+sL_{f2}}{\begin{bmatrix}(C_{f1}+C_{f2})L_{f1}L_{f2}s^3+\left((C_{f1}+C_{f2})(R_{f1}L_{f2}+R_{f2}L_{f1})-\frac{L_{f1}L_{f2}}{Z_{load}}\right)s^2 \\ +\left((C_{f1}+C_{f2})R_{f1}R_{f2}+L_{f1}+L_{f2}-\frac{R_{f1}L_{f2}+R_{f2}L_{f1}}{Z_{load}}\right)s+R_{f1}+R_{f2}-\frac{R_{f1}R_{f2}}{Z_{load}}\end{bmatrix}} \tag{4.5}$$

The denominator of (4.5) is the characteristic equation that describes the stability behavior of the first DG unit. Using the Routh Hurwitz criterion for a third order polynomial, the following stability conditions are obtained:

$$\frac{(C_{f1}+C_{f2})(R_{f1}L_{f2}+R_{f2}L_{f1})}{L_{f1}L_{f2}} V_{o,rms}^2 > P_{load} \tag{4.6}$$

$$\frac{(C_{f1}+C_{f2})R_{f1}R_{f2}+L_{f1}+L_{f2}}{R_{f1}L_{f2}+R_{f2}L_{f1}} V_{o,rms}^2 > P_{load} \tag{4.7}$$

From (4.6), (4.7), the stability conditions in a two DG micro-grid system can be achieved by one of the following:

- By increasing *R*/*L* ratio of the ac filter. In case of low voltage micro-grids, this ratio is naturally increased due to the resistive nature of the distribution feeders.
- The active power (P_{load}) drawn by the tightly-regulated CILs must be less than the $V_{o,rms}^2$ term in (4.6) and (4.7).
- The equivalent capacitance can be increased to satisfy (4.6) and (4.7).

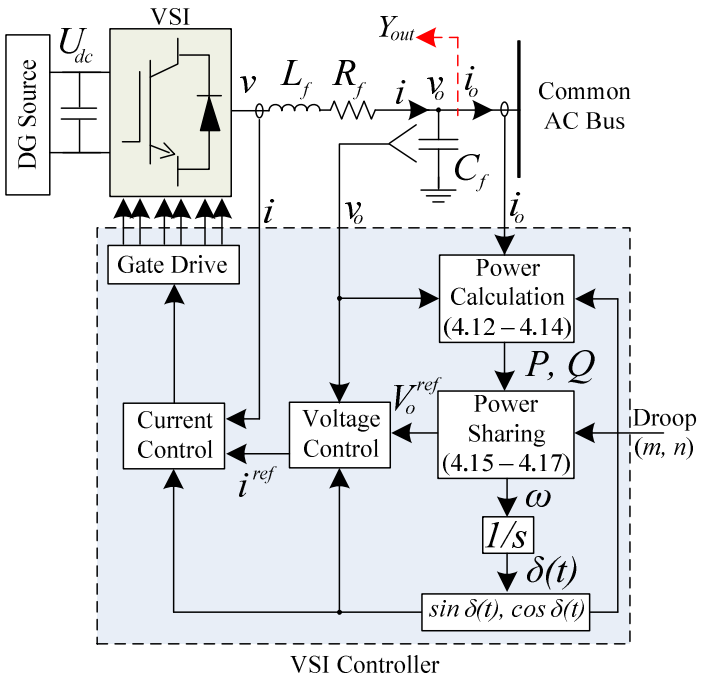

Figure 4.2: Power and control structure of one DG unit interfaced by VSI in ac micro-grid.

- The operating voltage level (V_o) can be increased to improve the stability margin.

All previous stability conditions depend on physical expansions of the micro-grid parameters to preserve the system stability under CP mode of operation. Increasing *R/L* ratio is not feasible as those parameters are fixed after the design stage and cannot be easily modified for a given converter. This also applies for the capacitance of the ac filter. Moreover, ac filter capacitors are preferred to be small for compact size and higher reliable applications especially with the recent efficient film capacitors that allow much higher current per unit volume [80]. Obviously, increasing the operating voltage of the overall micro-grid is not a valid option as well.

The aforementioned conditions clearly show that the active damping techniques can be a viable option as they can virtually achieve the stability conditions without any physical expansions in the ac micro-grid.

4.3 Admittance-Based Modeling of Voltage-Source Inverters in DG Applications

Figure 4.2 shows a VSI as an interface for a DG unit in ac micro-grid. Three control loops are utilized; namely they are the power sharing, voltage, and current controllers

[99], [105]. As shown in Figure 4.2, the power sharing controller is used to generate the local magnitude and angle of the reference output voltage according to the droop coefficients to emulate a conventional synchronous generator. The voltage controller is used to synthesize the reference value of the inverter output current $\left(i^{ref}\right)$. Finally, the current controller is adopted to generate the reference input voltage command for the VSI [$V_d^{inv}$and V_q^{inv} in (4.20) and (4.21)]; hence the inverter duty ratio can be determined. The controller structure is synthesized in the sense of the voltage-oriented control framework.

The current and voltage dynamics of the power circuits are modeled in the *d-q* frame that rotates synchronously with the inverter output voltage angular speed ω by:

$$V_d - V_{od} = I_d\left(R_f + sL_f\right) - \omega L_f I_q \tag{4.8}$$

$$V_q - V_{oq} = I_q\left(R_f + sL_f\right) + \omega L_f I_d \tag{4.9}$$

$$I_d - I_{od} = \left(sC_f + Y\right)V_{od} - \omega V_{oq} C_f \tag{4.10}$$

$$I_q - I_{oq} = \left(sC_f + Y\right)V_{oq} + \omega V_{od} C_f \tag{4.11}$$

where Y is the penetrated direct resistive load to the common ac-bus and is initially set to zero (passive damping effect); V_d, V_q, I_d and I_q are the *d-q* axis inverter output voltages and currents; V_{od}, V_{oq}, I_{od} and I_{oq} are the *d-q* axis load voltages and currents; R_f, L_f and C_f are the per-phase resistance, inductance and capacitance of the LC filter, respectively, and s is the Laplace operator.

In the *d-q* synchronous reference frame, the instantaneous active (p) and reactive (q) power delivered to the ac common bus are given by:

$$p = 1.5\left(V_{od} I_{od} + V_{oq} I_{oq}\right) \tag{4.12}$$

$$q = 1.5\left(V_{od} I_{oq} - V_{oq} I_{od}\right) \tag{4.13}$$

The average active (P) and reactive (Q) powers that correspond to the fundamental components are obtained by a LPF with a cut-off frequency ω_p to achieve high power quality injection; therefore:

$$P = \frac{\omega_p}{s+\omega_p} p,$$
$$Q = \frac{\omega_p}{s+\omega_p} q \tag{4.14}$$

Virtual droop characteristics are emulated in paralleled inverter systems to efficiently share the active and reactive power for the common load by introducing the following droops in the fundamental voltage frequency and magnitude of the load voltage:

$$\omega = \omega^* - mP \tag{4.15}$$
$$V_{od}^{ref} = V_{od}^* - nQ \tag{4.16}$$

where ω^* and V_{od}^* are the nominal frequency and voltage set points; m and n are the static droop gains and they are calculated as follows:

$$m = \frac{\omega_{max} - \omega_{min}}{P_{max}},$$
$$n = \frac{V_{od,max} - V_{od,min}}{Q_{max}} \tag{4.17}$$

The dynamics of the ac voltage and current controllers can be given as:

$$I_d^{ref} = \left(V_{od}^{ref} - V_{od}\right) G_v(s) - \omega C_f V_{oq} + H I_{od} \tag{4.18}$$
$$I_q^{ref} = \left(V_{oq}^{ref} - V_{oq}\right) G_v(s) + \omega C_f V_{od} + H I_{oq} \tag{4.19}$$
$$V_d^{inv} = \left(I_d^{ref} - I_d\right) G_i(s) - \omega L_f I_q + V_{od} \tag{4.20}$$
$$V_q^{inv} = \left(I_q^{ref} - I_q\right) G_i(s) + \omega L_f I_d + V_{oq} \tag{4.21}$$

where H is a feed-forward gain, $G_v(s)$ and $G_i(s)$ are the ac voltage and current controller functions with K_{vp} and K_{ip} as proportional gains and K_{vi} and K_{ii} as integral gains, respectively. The superscript "^{ref}" denotes the reference value. A large-signal

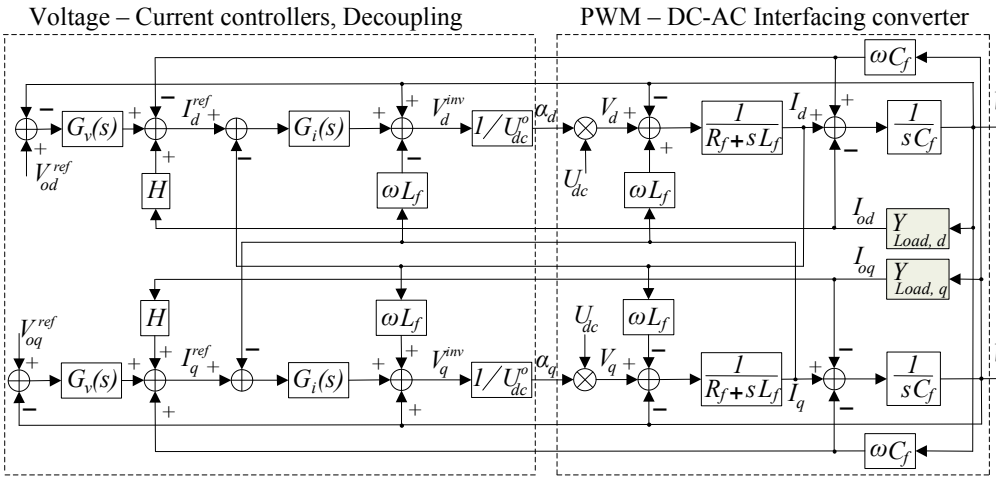

Figure 4.3: Large-signal model for VSI interface for DG system.

block diagram for the ac micro-grid interface is shown in Figure 4.3. The overall system parameters are given in Appendix A4.1.

For a DG unit, the source admittance of VSI can be obtained as follows. Using (4.10) in (4.18), (4.8) in (4.20) and solving the resultant two equations to eliminate I_d^{ref}:

$$I_d\left(R_f + sL_f\right) + G_i(s)(1-H)I_{od} + G_i(s)\left(sC_f + Y + G_v(s)\right)V_{od} - V_d = G_v(s)G_i(s)V_{od}^{ref} - V_d^{inv} \tag{4.22}$$

Applying small perturbations in (4.22) with $\Delta V_{od}^{ref} = 0$, approximating $\Delta V_d^{inv} \approx \Delta V_d$ and substituting ΔI_d from (4.10) with $\Delta V_{oq} = 0$ due to the zero-voltage orientation in the q-channel, the linearized source admittance of the VSI with passive load penetration is obtained as follows.

$$\Delta Y_{out} = \frac{\Delta I_{od}}{\Delta V_{od}} = \frac{L_f C_f s^4 + \left(R_f + K_{ip}\right)C_f s^3 + \left(C_f K_{ii} + K_{ip}\left(Y + K_{vp}\right)\right)s^2 + \left(K_{ip}K_{vi} + K_{ii}\left(Y + K_{vp}\right)\right)s + K_{ii}K_{vi}}{-L_f s^3 + \left(K_{ip}(H-1) - R_f\right)s^2 + (H-1)K_{ii}s} \tag{4.23}$$

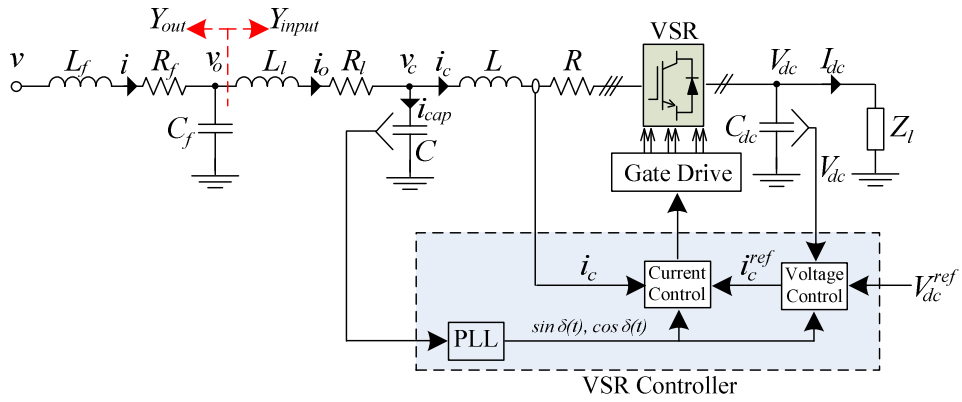

Figure 4.4: Power and control structure of a VSR

4.4 Voltage-Source Rectifier as a Converter-Interfaced Load in AC Micro-grids

This section introduces the VSR as a CIL in ac micro-grid applications. Based on small-signal linearization and admittance-based analysis, the input admittance of VSR is obtained. Active stabilization and reshaping techniques are also provided. The proposed solutions are evaluated under Matlab/Simulink platform with a complete ac micro-grid model.

4.4.1 Admittance-Based Modeling of Voltage-Source Rectifier

Figure 4.4 shows a schematic diagram of a VSR. Using the two-phase *d-q* synchronous reference frame that rotates by angular frequency ω dedicated by a phase-looked loop (PLL), the large-signal model of VSR power circuit can be given by [122], [123]:

$$V_{cd} = I_{cd}(R + sL) - \omega L I_{cq} + D_d V_{dc} \tag{4.24}$$

$$V_{cq} = I_{cq}(R + sL) + \omega L I_{cd} + D_q V_{dc} \tag{4.25}$$

$$V_{od} = I_{od}(R_l + sL_l) - \omega L_l I_{oq} + V_{cd} \tag{4.26}$$

$$V_{oq} = I_{oq}(R_l + sL_l) + \omega L_l I_{od} + V_{cq} \tag{4.27}$$

$$I_{od} = I_{cd} + sCV_{cd} - \omega CV_{cq} \tag{4.28}$$

$$I_{oq} = I_{cq} + sCV_{cq} + \omega CV_{cd} \tag{4.29}$$

$$sC_{dc}V_{dc} = 1.5\left(D_d I_{cd} + D_q I_{cq}\right) - I_{dc}\ ,$$

$$V_{dc} = I_{dc} Z_l \tag{4.30}$$

where R_l, L_l and R, L are the per phase equivalent resistance and inductance of the distribution line and the input ac filter of the VSR whereas C and C_{dc} are the ac-side and the dc-link capacitor, respectively; Z_l is the terminated load at the dc-side of the VSR with a dc-link voltage (V_{dc}) and input dc current (I_{dc}); R_f, L_f and C_f are the output ac filter parameters of the source-side which can be a VSI [Figure 4.2]; I_{cd}, I_{cq} are the *d-q* components of the rectifier input ac current (i_c); I_{od}, I_{oq} are the *d-q* components of i_o; while V_{cd}, V_{cq} and V_{od}, V_{oq} are the *d-q* components of the ac voltages v_c and v_o, respectively; D_d and D_q are the rectifier duty ratios in *d-q* frame and are determined by the control topology.

An outer PI dc voltage controller $\left(G_{vdc}(s)\right)$ is used for dc voltage tracking and regulation, whereas an inner PI current controller $\left(G_{ic}(s)\right)$ is used for voltage-orientation mechanism at a unity power factor by setting the quadrature component of the input ac current to zero $\left(I_{cq}^{ref} = 0\right)$. The mathematical model for the dc voltage controller is given by:

$$I_{cd}^{ref} = \left(V_{dc}^{ref} - V_{dc}\right)G_{vdc}(s) \tag{4.31}$$

where it generates the *d*-axis component of the VSR reference current $\left(I_{cd}^{ref}\right)$. The current controller synthesizes the duty ratios in the *d-q* frame which are used to generate the controlled signals of the IGBT switches.

$$D_d V_{dc} = -\left(I_{cd}^{ref} - I_{cd}\right)G_{ic}(s) + V_{cd} + \omega L I_{cq} \tag{4.32}$$

$$D_q V_{dc} = -\left(I_{cq}^{ref} - I_{cq}\right)G_{ic}(s) + V_{cq} - \omega L I_{cd} \tag{4.33}$$

The overall system parameters of the VSR are depicted in Appendix A4.2.

Applying small-signal linearization on (4.30) and (4.24) and solve together to eliminate ΔD_d:

$$\left(sC_{dc} + \frac{1}{Z_l} + 1.5\frac{\overset{\circ}{I_{cd}}\overset{\circ}{D_d}}{\overset{\circ}{V_{dc}}}\right)\Delta V_{dc} = \left(1.5\overset{\circ}{D_d} - 1.5\frac{\overset{\circ}{I_{cd}}(R+sL)}{\overset{\circ}{V_{dc}}}\right)\Delta I_{cd} + 1.5\frac{\overset{\circ}{I_{cd}}}{\overset{\circ}{V_{dc}}}\Delta V_{cd} \tag{4.34}$$

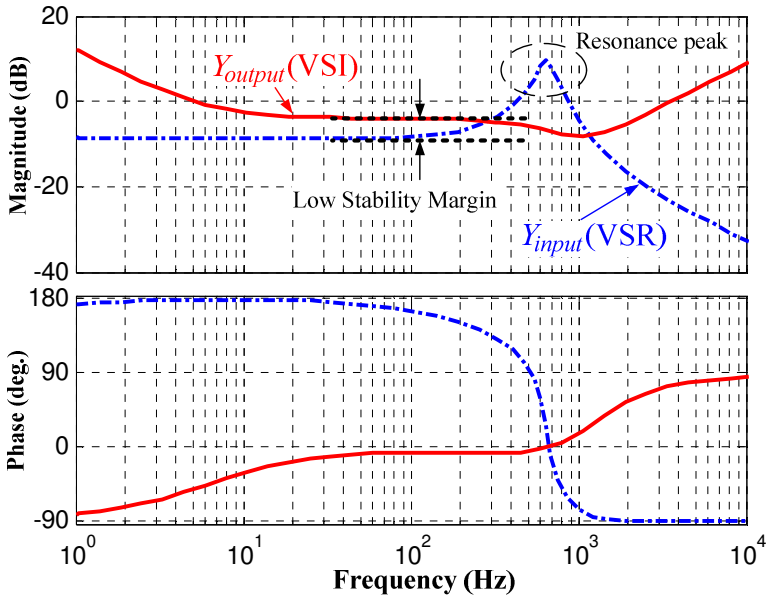

Figure 4.5: Frequency response of the input admittance of VSR and output admittance of VSI.

where the superscript " ° " represents the steady state value of the variable around which the linearization is applied.

Solving (4.24), (4.31) and (4.32) to eliminate $D_d V_{dc}$ and I_{cd}^{ref}:

$$\left(V_{dc}^{ref} - V_{dc}\right)G_{vdc}(s)G_{ic}(s) = I_{cd}\left(R + sL + G_{ic}(s)\right) \tag{4.35}$$

Applying small perturbations on (4.35) with $\Delta V_{dc}^{ref} = 0$, and solve with (4.34), a relation between ΔV_{cd} and ΔI_{cd} is obtained as:

$$-1.5\frac{\overset{\circ}{I_{cd}}}{\overset{\circ}{V_{dc}}}\Delta V_{cd} = \underbrace{\left[1.5\overset{\circ}{D_d} - 1.5\frac{\overset{\circ}{I_{cd}}(R+sL)}{\overset{\circ}{V_{dc}}} + \left(\frac{R+sL+G_{ic}(s)}{G_{vdc}(s)G_{ic}(s)}\right)\left(sC_{dc} + \frac{1}{Z_l} + 1.5\frac{\overset{\circ}{I_{cd}}\overset{\circ}{D_d}}{\overset{\circ}{V_{dc}}}\right)\right]}_{B(s)}\Delta I_{cd} \tag{4.36}$$

Applying small perturbation on (4.28) setting ΔV_{cq} to zero due to the unity power factor mode of operation and *d*-axis orientation with the input voltage, and solving with (4.36) to eliminate ΔI_{cd}:

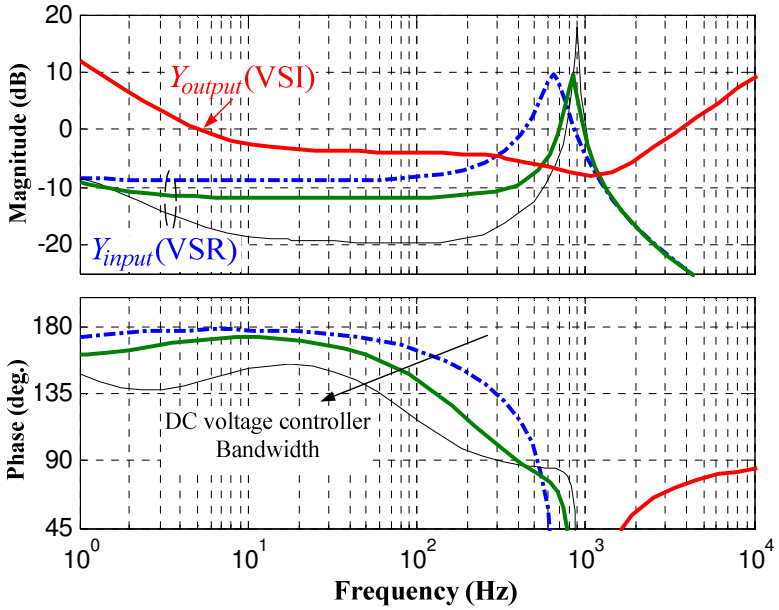

Figure 4.6: Influence of tight regulation of the dc voltage controller on the input admittance of VSR.

$$\left(-1.5\frac{\overset{\circ}{I_{cd}}}{\overset{\circ}{V_{dc}}} + sCB(s)\right)\Delta V_{cd} = B(s)\Delta I_{od} \tag{4.37}$$

Small perturbation is applied to (4.26) to be solved with (4.37); the small-signal input admittance of the VSR is obtained as:

$$\Delta Y_{in} = \frac{\Delta I_{od}}{\Delta V_{od}} = \frac{sCB(s) - 1.5\frac{\overset{\circ}{I_{cd}}}{\overset{\circ}{V_{dc}}}}{B(s) + \left(sCB(s) - 1.5\frac{\overset{\circ}{I_{cd}}}{\overset{\circ}{V_{dc}}}\right)(R_l + sL_l)} \tag{4.38}$$

where $B(s)$ is defined in (4.36).

4.4.2 Input-Output Admittance Mismatching

Using the small-signal input admittance of the VSR in (4.38) and the output admittance of the VSI in (4.23), the frequency response is shown in Figure 4.5. The effect of the LCL filter of the VSR is clearly reflected to its input admittance as a resonant peak. As shown, the resonant peak interacts with the output admittance of the VSI violating Nyquist criterion. Moreover, in the mid-frequency region, the stability margin is limited and subjects the overall system to instabilities in case of sudden load- or

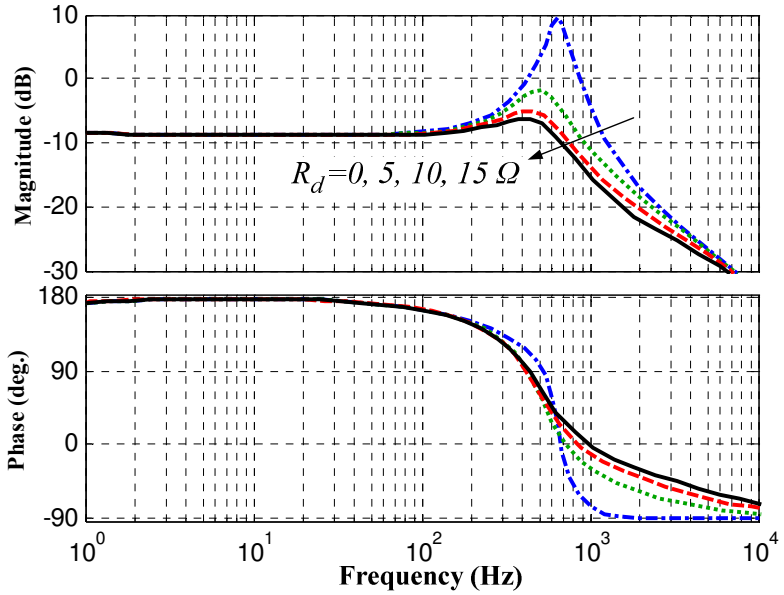

Figure 4.7: Frequency response of the input admittance of VSR – Effect of passive resonant damping.

source-side disturbances that may reshape their corresponding admittances with high possibilities of further interactions.

It can be noted that the input admittance of VSR in Figure 4.5 has a phase angle of almost 180˚ in the low- and mid-frequency range which implies negative resistance characteristics and negative damping. Figure 4.6 shows that the tight regulation objective of the dc voltage controller has a considerable influence on the input admittance of the VSR. With the reduction of the dc voltage controller bandwidth (reduction of tight regulation), the phase angle of the input admittance of VSR shifts away from the 180˚ and approaches positivity. Moreover, the magnitude of the input admittance decreases with a resultant higher stability margins as the probability of interactions with the output admittance of the VSI decreases.

For the high-frequency resonant peak, a physical resistor can be added in series with the ac filter capacitor (C) of the VSR to be damped [Figure 4.4]. In this case, the model in (4.28) is modified to:

$$I_{od} = I_{cd} + \left(\frac{sC}{1+sCR_d}\right)V_{cd} - \omega C V_{cq} \tag{4.39}$$

where R_d is the physical resistance added in series with C.

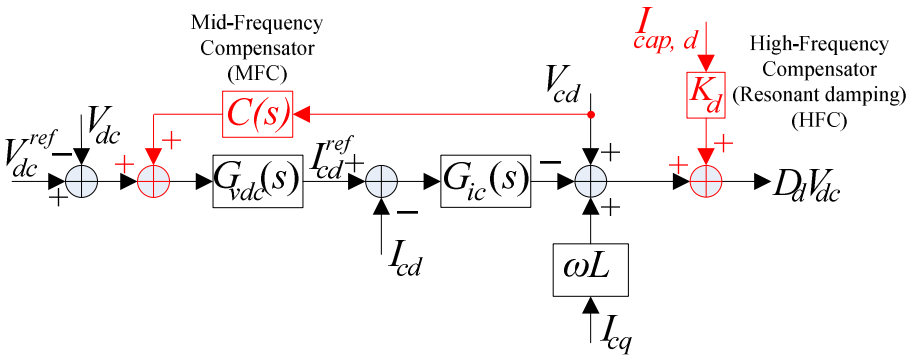

Figure 4.8: The proposed MFC and HFC for VSR as a common load in ac micro-grids.

Figure 4.7 shows the frequency response of the input admittance of the VSR with the employed R_d. As shown, with higher R_d, the resonant peak is successfully damped. However, this passive solution is not preferred in DG applications due to the associated power losses.

4.4.3 Active Stabilization and Input-Output Admittance Matching

Based on Figure 4.5, the main objective of the proposed active compensator is to reshape the input admittance of the VSR to avoid possible interactions in the mid- and high-frequency regions by maintaining the Nyquist criterion.

Figure 4.8 shows a schematic diagram of the modified control loops of the VSR. As shown, two proposed compensators are employed; mid-frequency compensator (MFC) to actively reshape the input admittance of the VSR to avoid possible interactions with the output admittance of the VSI at this region and high-frequency compensator (HFC) to damp the resonant peak due to the LCL ac filter of the VSR.

The HFC is employed by feeding the *d*-axis component of the ac capacitor current $(I_{cap,d})$ through a constant gain (K_d) to mimic a virtual voltage drop that is added to the generated control signal.

For the mid-frequency compensation, V_{cd} is applied through a compensator function $(C(s))$ to generate the active compensation signal that is added to the dc-link voltage reference. The selection of $C(s)$ is based on BP filter characteristics to allow the admittance reshaping around the required frequency band; $C(s)$ is given as follows:

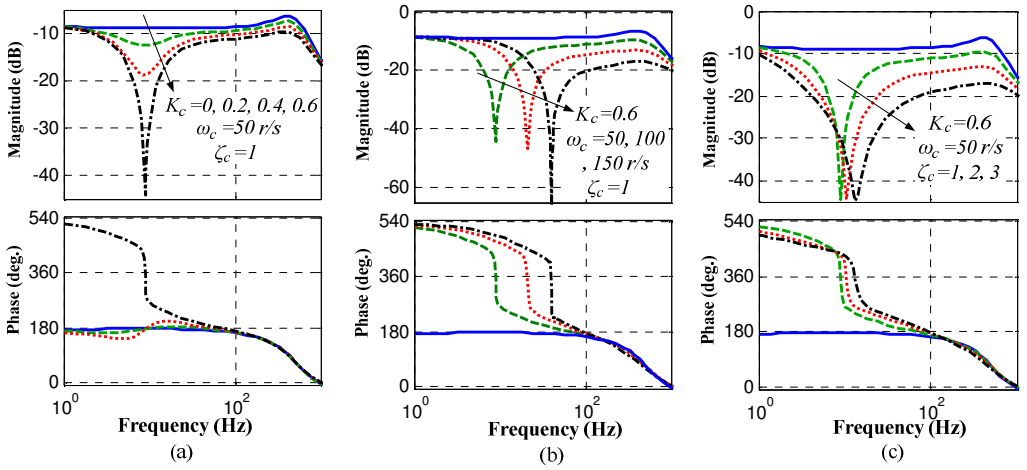

Figure 4.9: Influence of the HFC parameters on the input admittance of the VSR. (a) Effect of K_c. (b) Effect of ω_c. (c) Effect of ξ_c.

$$C(s) = K_c \frac{2\xi_c \omega_c s}{s^2 + 2\xi_c \omega_c s + \omega_c^2} \tag{4.40}$$

where ξ_c is the damping factor, ω_c is the operating frequency and K_c is the compensator gain.

By employing both MFC and HFC in (4.31) and (4.32), respectively; the modified system dynamics due to the proposed compensators is given by:

$$\begin{aligned} I_{cd}^{ref} &= \left(V_{dc}^{ref} - V_{dc} + C(s)V_{cd}\right)G_{vdc}(s), \\ D_d V_{dc} &= -\left(I_{cd}^{ref} - I_{cd}\right)G_{ic}(s) + V_{cd} + \omega L I_{cq} + sCK_d \end{aligned} \tag{4.41}$$

Following similar mathematical procedures, the compensated small-signal input admittance (ΔY_{in}^c) of the VSR is obtained as:

$$\Delta Y_{in}^c = \frac{\Delta I_{od}}{\Delta V_{od}} = \frac{sCB(s) + A(s)}{B(s) + \left(sCB(s) + A(s)\right)(R_l + sL_l)} \tag{4.42}$$

$A(s) = \frac{G_{vdc}(s)G_{ic}(s)C(s) - sCK_d}{G_{vdc}(s)G_{ic}(s)}\left(sC_{dc} + \frac{1}{Z_l} + 1.5\frac{\overset{\circ}{I_{cd}}\overset{\circ}{D_d}}{\overset{\circ}{V_{dc}}}\right) - 1.5\frac{\overset{\circ}{I_{cd}}}{\overset{\circ}{V_{dc}}}$, $B(s)$ is defined in (4.36).

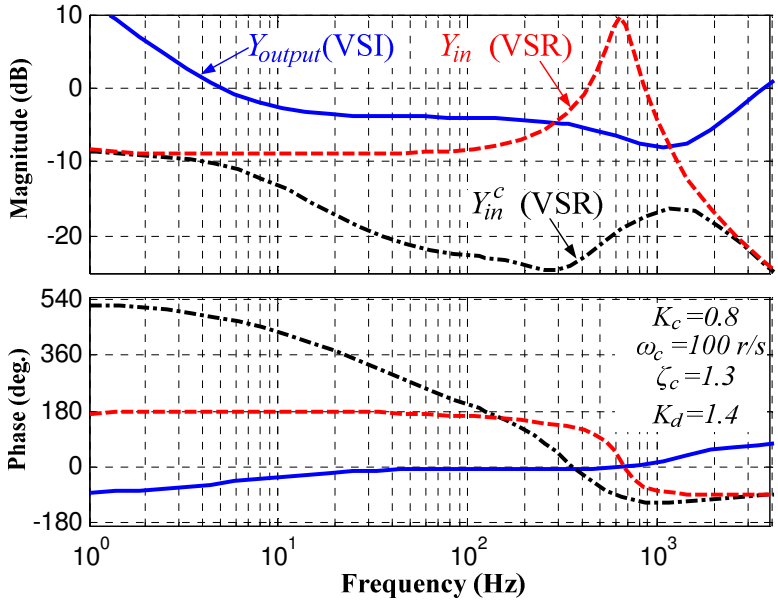

Figure 4.10: Frequency response of the compensated input admittance of VSR (ΔY_{in}^{c}) – $K_c = 0.8$, $\omega_c = 100$ rad/sec, $\xi_c = 1.3$, $K_d = 1.4$.

To show the pure influence of the BP characterized compensator $\big(C(s)\big)$ on the input admittance of the VSR, passive damping is considered with $R_d = 15\Omega$ to neutralize the interactions due to LCL resonance at high frequencies. As shown in Figure 4.9, the compensated input admittance of the VSR can be actively reshaped to avoid possible interactions with the source-side. The compensated input admittance follows the dynamics response of the BP filters. In Figure 4.9(a), the operating frequency (ω_c) of the proposed compensator $\big(C(s)\big)$ equals 50 rad/sec with a unity damping factor $(\xi_c = 1)$. With the increase of the compensator gain (K_c), the input admittance decreases accordingly around the designed frequency. Figure 4.9(b) shows the effect of changing the operating frequency of $C(s)$. The width of the resultant peak increases with the increase of the damping factor (ξ_c) as shown in Figure 4.9(c). The selection of the operating frequency of the proposed compensator depends on the output admittance of the source-side to avoid possible interactions. The proposed HFC and MFC compensators facilitate input-output admittance matching with four degree of freedom to satisfy the Nyquist criterion.

Figure 4.10 shows the input-output admittance matching by considering the compensated input admittance of VSR in (4.42) and the output admittance of the VSI in (4.23). As shown, the HFC successfully mitigates the resonant peak while the MFC

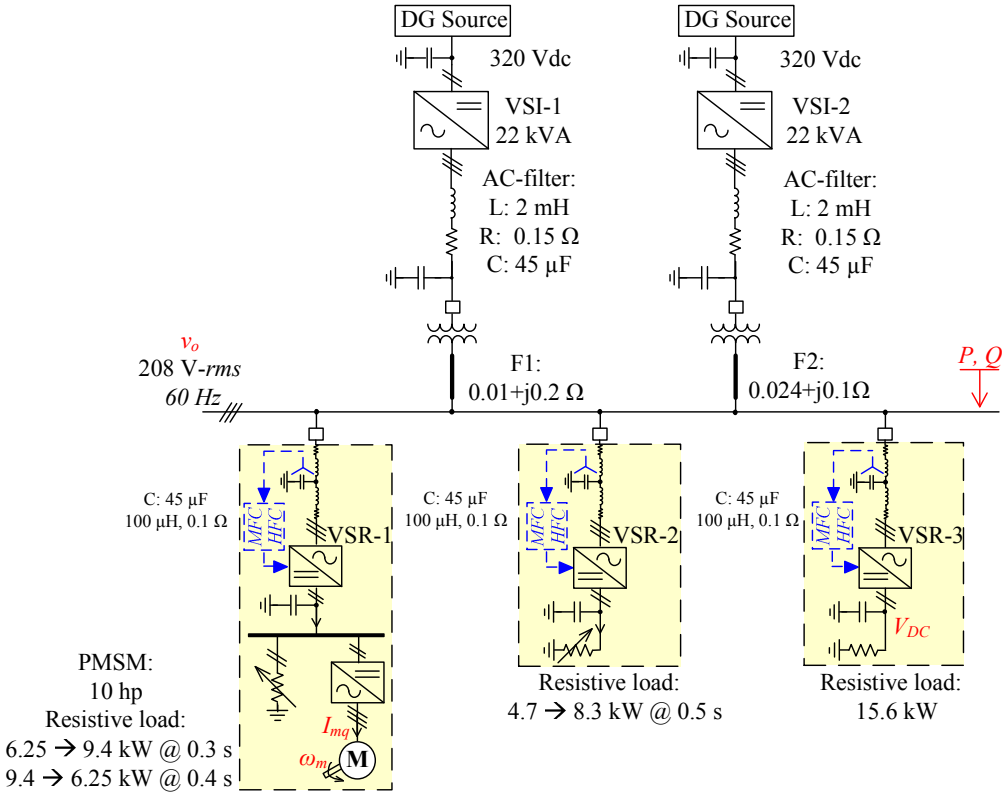

Figure 4.11: Implemented ac micro-grid system.

results in higher stability margin. Moreover, the active compensators mitigate the negative resistance effect. A shown in Figure 4.10, the 180˚ phase angle of the uncompensated input admittance at low- and mid-frequency region is shifted to be positive increasing the overall system damping.

4.4.4 Evaluation Results

To verify the preceding analytical results, a complete 44 kVA, 208V ac micro-grid system is implemented under the Matlab/Simulink environment. As shown in Figure 4.11, the implemented system consists of two DG units interfaced by two 22kVA VSIs operating in the isolated micro-grid mode of operation. The ac micro-grid system is penetrated by three CILs: VSR-1 is feeding a PMSM drive rated at 10 hp and resistive load at the dc-link side with power rating of 6.25kW that increases to 9.4kW at time t = 0.3s then returns back to 6.25kW at t = 0.4s; VSR-2 interfaces a resistive load rated at 4.7 kW and instantly increases to 8.3kW at t = 0.5s; and VSR-3 is feeding a constant

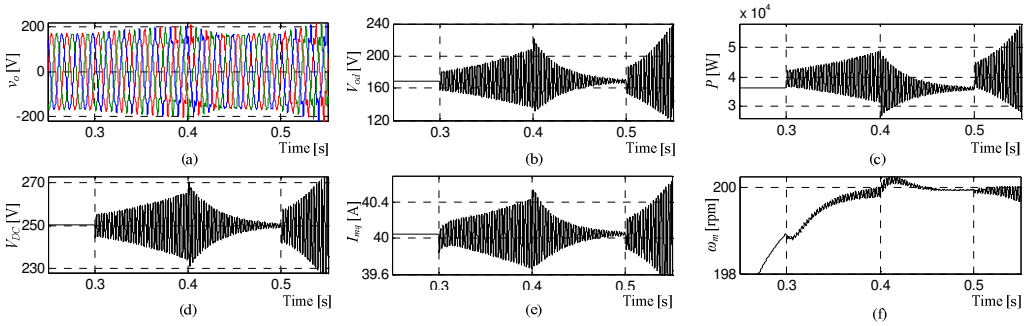

Figure 4.12: Uncompensated system response. (a), (b) Common ac voltage. (c) Total injected active power. (d) Dc-side voltage of VSR-3. (e) q-axis component of the PMSM stator ac current. (f) PMSM speed.

resistive load with power demand of 15.6kW. The overall implemented system parameters are depicted in Appendix A4.3. It is clear that the ac micro-grid is characterized by severe loading/unloading conditions to subject the proposed compensators to the worst loading conditions. The implemented system is tested under two conditions with the same loading/unloading scenario: without compensation and with the proposed compensator (LSC).

4.4.4.1 Uncompensated system

Applying the loading/unloading scenario, the system response is shown in Figure 4.12 without the proposed compensators. In Figure 4.12(a) and (b), the common ac voltage (v_o) and its d-axis component (V_{od}) are shown, respectively. It is clear that the response is unstable at the loading instant of VSR-1 at t = 0.3s whereas a decayed response is yielded due to removing the excessive loading at t = 0.4s. The system response builds-up again at t = 0.5s due to the increased load power of VSR-2. The unstable response is reflected to the total injected active power (P) to the augmented CILs as shown in Figure 4.12(c). Although the loading/unloading disturbances are applied to VSR-1 and -2, the dc-link voltage (V_{DC}) of VSR-3 is completely degraded with unstable response as shown in Figure 4.12(d). It is clear that the lightly-damped modes of the uncompensated system results in destabilized response that interacts to the whole entities of the ac micro-grid system. As shown in Figure 4.12(e) and (f), the q-axis component of the PMSM stator current $\left(I_{mq}\right)$ and the rotor speed (ω_m) are also affected with a similar trend.

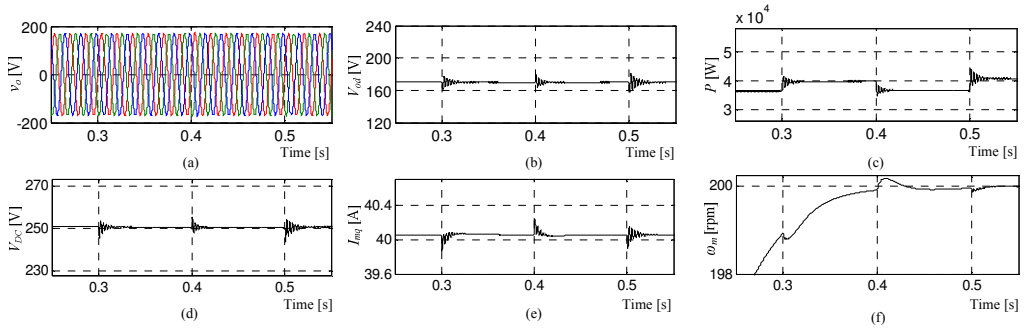

Figure 4.13: LSC system response. (a), (b) Common ac voltage. (c) Total injected active power. (d) Dc-side voltage of VSR-3. (e) q-axis component of the PMSM stator ac current. (f) PMSM speed.

4.4.4.2 Actively Compensated System from Load-Side

The LSC technique is investigated in this subsection under the same loading/unloading scenario. Figure 4.13(a) and (b) shows the common ac voltage response whereas the injected active power is shown in Figure 4.13(c); all responses are damped and remarkably improved as compared to Figure 4.12. This clearly implies that input-output admittance ratio criterion is satisfied by employing the LSC which validates the analytical results that obtained in Figure 4.10. The CILs performance is improved as shown in Figure 4.13(d) for V_{DC} of VSR-3 and the motor drive performance as in Figure 4.13 (e) and (f).

4.5 Augmented Converter-Interfaced Loads in AC Micro-grids Applications

It has been shown in the last section that tightly-regulated CILs appear from their input terminals as incremental negative input admittance. This is clear from Figure 4.5 where the input admittance of tightly-regulated VSR has negative value in low frequency range. Therefore, it is accepted to model the CIL as a negative resistance that only depends on the amount of drawn power regardless the load dynamics. This generic approach of modeling CIL provides a worst case condition that is negative resistance on the whole frequency range.

An example of a CIL is shown in Figure 4.14, which represents an industrial load with multiple motor drives fed from a front-end controlled rectifier. The aggregated motor drive loads on the dc-bus requires a second tightly-regulated control objective for the front-end controlled rectifier; that is the dc-link voltage should be regulated at

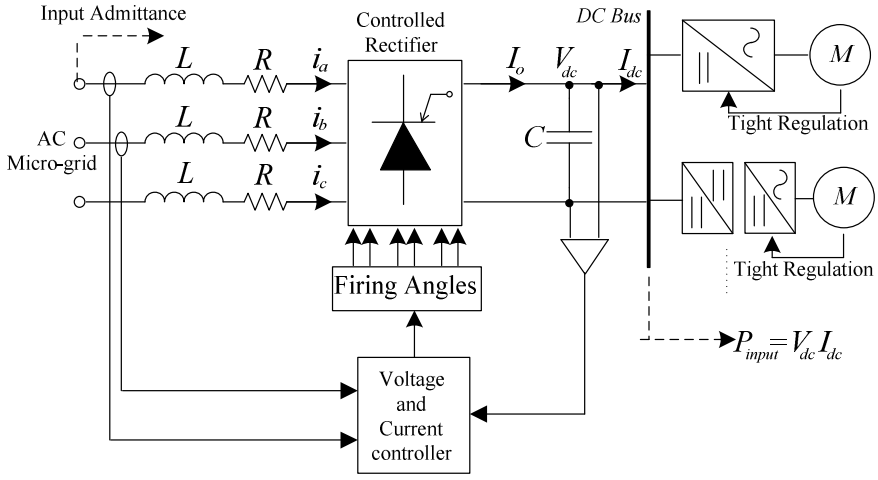

Figure 4.14: Motor drives system as a CIL.

different loading conditions. Such a load creates two-dimensional tight regulation which affects the micro-grid stability due to the penetrated incremental negative input admittance. For such a complicated load, the input admittance can be approximately obtained in terms of the constant power operation behavior of the load. For controlled rectifiers in CCM, the voltage and the current of the load can be given as:

$$v(t) = V_{max} cos(\omega t),$$
$$i(t) = I_{max} cos(\omega t - \alpha) \tag{4.43}$$

where α is the firing angle of the controlled rectifier. Applying small-signal linearization on the average per-phase power that is delivered to the rectifier load, $P_{ave} = V_{rms} I_{rms} cos\alpha$, the approximated incremental input resistance R_{cp} is given by:

$$\frac{\Delta I_{max}}{\Delta V_{max}} = -\frac{I_{max}}{V_{max}} = -\frac{1}{R_{cp}} \tag{4.44}$$

If a phase difference between the current and the voltage is considered, the equivalent small-signal resistance (r_{cp}) and inductance (L_{cp}) of the load are obtained as:

$$r_{cp} = -R_{cp} \cos(\alpha),$$

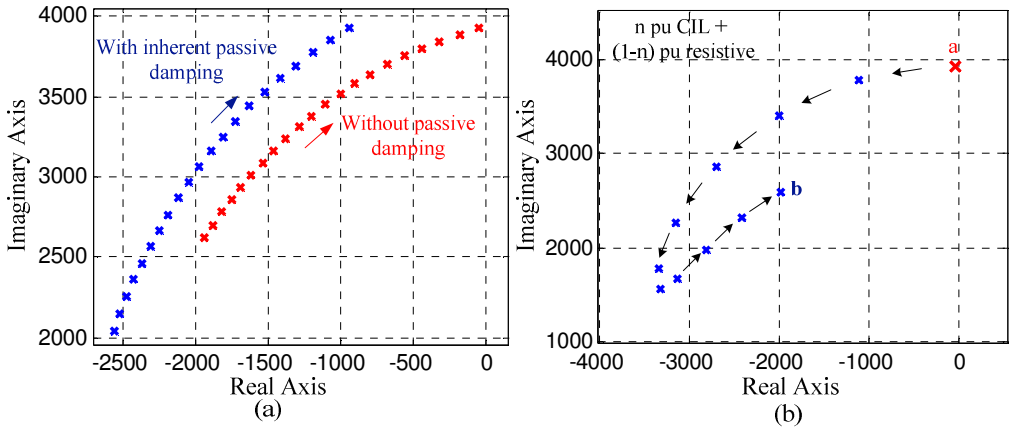

Figure 4.15: Dominant pole loci for VSI as an interface for ac micro-grid. (a) CIL increases from 0 to 1pu with the direction of the arrow – with, without 0.1pu inherent passive damping. (b) $n = 1$ at "a" (Full CIL), $n = 0$ at "b" (Full resistive).

$$L_{cp} = -R_{cp}\sin(\alpha)/\omega \tag{4.45}$$

From the exact input admittance in (4.38) and the approximated one in (4.45), it can be seen that the ac micro-grid is prone to instability due to the negative admittance reflected to the DG source terminals.

4.5.1 Effect of Pure Converter-Interfaced Load /Resistive-Load-Mix on the AC Micro-grid Stability

This section addresses the effect of load mix on the DG interface stability. With high penetration of CILs, negative input admittance can be reflected to the DG interface affecting the voltage dynamics. To study the effect of inherent passive damping due to resistive load, a resistive-CIL load mix is assumed. The DG interface dynamics is analyzed under this scenario.

To assess the DG interface stability at different penetration levels of CILs, V_{od} dynamics with respect to the VSI dc voltage (U_{dc}) [see Figure 4. 2] is derived by applying small-signal linearization on (4.12) which results in the generic model of CPL;

$$\frac{\Delta I_{od}}{\Delta V_{od}} = -\frac{I_{od}}{V_{od}} \tag{4.46}$$

which is an incremental negative admittance due to the CP operational mode of the CILs.

Considering the resistive load, Y, that is modeled in (4.10) and (4.11) and the generic CIL load model in (4.46), the aggregated load admittance seen from the ac micro-grid interface is represented by (4.47) in small-signal sense.

$$\Delta Y_l = Y - \frac{\overset{\circ}{I_{od}}}{\overset{\circ}{V_{od}}} \tag{4.47}$$

Obviously, with the increase of the delivered power to the resistive load, the total small-signal load admittance approaches the positivity, hence increasing the overall stability margin.

Solving (4.10) and (4.22) to eliminate I_d and apply small-signal linearization on the resultant equation with $\Delta V_d^{inv} = \Delta V_d - \left(V_d^{\circ}/U_{dc}^{\circ}\right)\Delta U_{dc}$ [from the average model of the VSI in Figure 4.3] and using the generic model of the CIL to substitute ΔI_{od} by ΔV_{od}, the characteristic equation that describes the VSI stability is obtained as the denominator of (4.48). For VSI with purely CIL termination, Y is set to zero.

$$\frac{\Delta V_{od}}{\Delta U_{dc}} = \frac{(V_d^{\circ}/U_{dc}^{\circ})s^2}{\begin{bmatrix} L_f C_f s^4 + \left(C_f(R_f + K_{ip}) + L_f\left(Y - I_{od}^{\circ}/V_{od}^{\circ}\right)\right)s^3 + \left(K_{ip}(Y + K_{vp}) + R_f\left(Y - I_{od}^{\circ}/V_{od}^{\circ}\right) + C_f K_{ii} - I_{od}^{\circ} K_{ip}(1-H)/V_{od}^{\circ}\right)s^2 \\ + \left(K_{ip}K_{vi} - I_{od}^{\circ} K_{ii}(1-H)/V_{od}^{\circ} + K_{ii}(Y + K_{vp})\right)s + K_{ii}K_{vi} \end{bmatrix}} \tag{4.48}$$

As a reference, the voltage tracking dynamics with pure CIL penetration ($Y = 0$), i.e., V_{od}/V_{od}^{ref}, can be obtained by using (4.8), (4.10) and (4.20) in (4.18), as given by (4.49).

$$\frac{V_{od}}{V_{od}^{ref}} = \frac{(K_{ip}K_{vp}Z_l)s^2 + (K_{ip}K_{vi} + K_{ii}K_{vp})Z_l s + K_{ii}K_{vi}Z_l}{\tau_4 s^4 + \tau_3 s^3 + \tau_2 s^2 + \tau_1 s + \tau_0} \tag{4.49}$$

$\tau_4 = L_f C_f Z_l$

$\tau_3 = L_f + C_f Z_l\left(R_f + K_{ip}\right)$

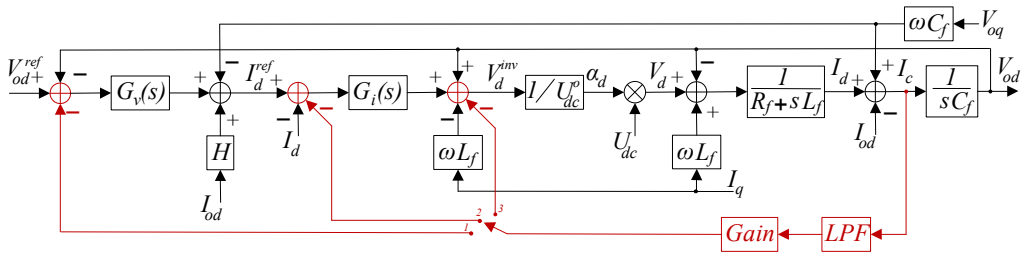

Figure 4.16: Proposed active compensators. (1) RLV compensator. (2) RIC compensator. (3) RIV compensator.

$$\tau_2 = R_f + C_f Z_l K_{ii} - K_{ip}(H-1) + Z_l K_{ip} K_{vp}$$

$$\tau_1 = -(H-1)K_{ii} + Z_l\left(K_{ip}K_{ii} + K_{ii}K_{vp}\right)$$

$$\tau_0 = Z_l K_{ii} K_{vi}$$

Figure 4.15(a) shows the dominant pole loci of uncompensated DG interface dynamics with $Y = 0$ in (4.48) as the penetration level of CILs increases from no-load to 1.0 p.u. As the penetration level of CILs increases, the damping of the dominant eigen value decreases significantly from -1941 to -53.25 s^{-1}, respectively, which yields to significant reduction in stability margins, and eventually instability can be yielded under loading or network disturbances. With direct resistive load penetration of 0.1 p.u., the dominant pole loci are shifted to -2567 s^{-1} at no load and -944 s^{-1} at full load. However, with 0.1 p.u. resistive loading, the system damping is not sufficient enough to maintain high stability margins and high power quality injection under the occurrence of system disturbances. Direct resistive loads may not be available at all. Therefore, relying on the inherent damping capabilities of resistive loads is unreliable. Accordingly, active compensation techniques are crucial to maintain the micro-grid stability.

Figure 4.15(b) shows the dominant pole loci when the penetration level of the resistive load gradually increases with a corresponding decrease of the CIL. As shown, the damping of the most dominant pole is shifted from -53.25 s^{-1} with 1.0. p.u. pure CIL (at "a") to -1992 s^{-1} with 1 p.u. pure resistive load (at "b"). This implies that a conventional ac micro-grid interface cannot be used for seamless plug-and-play integration in a micro-grid system with high penetration of CILs as the damping decreases dramatically.

4.5.2 Proposed Active Damping Techniques for AC Micro-grid Interface

Three active compensation techniques are investigated to actively reshape the source admittance of the interfacing inverter to meet the Nyquist ratio criterion, and accordingly the stability conditions at different micro-grid loading conditions. The proposed methods inject active damping signal to the outer, intermediate and inner control loops which corresponds to the load-voltage, the inverter-output-current and the inverter-output-voltage loops, respectively. Figure 4.16 shows a block diagram of the DG interface with the proposed compensators. All compensators are adopted in the direct axis loops only as the quadrature reference output voltage is set to zero.

The active compensators utilize the capacitor current, which is inherently small; therefore, the active damping signal will not saturate the inverter control voltage. In each of the proposed compensators, the capacitor current is scaled by a gain processed by a LPF stage to filter the high-frequency contents and to provide internal model dynamics within a specified frequency range. The active damping loops map the frequency modes of the output voltage to the closed loop system to provide damping capabilities by increasing the damping of poorly-damped modes associated with high penetration of CILs. Depending on the location of the active damping signal injection within the closed loop controlled system, the mapping of the output voltage frequency modes and the stabilization capabilities are generally different. Moreover, the location of the injected signals influences the ac voltage controller bandwidth which is a pertinent factor that affects the tracking of the output ac voltage.

It should be noted that the output ac voltage (V_{od}) can be used as an input signal to the compensator by utilizing a lead-lag transfer function instead of the LPF and including a derivative element to extract a band-limited version of the capacitor current. Both approaches are equivalent.

This section provides mathematical analysis for each compensation technique to evaluate their damping capabilities, and interactions between the damping controller and ac voltage dynamics.

4.5.2.1 Reference-Load-Voltage (RLV) Compensator

The compensator signal is applied to the selector “1” in Figure 4.16. The output load voltage (V_{od}) is virtually modulated by the compensator signal to embed a virtual

resistive voltage component in the output voltage that is proportional to the capacitor current. This compensator modifies (4.18) to actively reduce the source admittance of the VSI as follows:

$$I_d^{ref} = \left(V_{od}^{ref} - \left(1 + N_1(s)\right)V_{od}\right)G_v(s) - \omega C_f V_{oq} + HI_{od} \tag{4.50}$$

Where $N_1(s)$ is the RLV compensator transfer function and is given by:

$$N_n(s) = \frac{sK_n\omega_n C_f}{s+\omega_n},\ n = 1 \tag{4.51}$$

With the RLV compensator, the small-signal source admittance of the VSI is given by (4.52).

$$\frac{\Delta I_{od}}{\Delta V_{od}} = \frac{\alpha_5 s^5+\alpha_4 s^4+\alpha_3 s^3+\alpha_2 s^2+\alpha_1 s+\alpha_0}{-L_f s^4+\left(K_{ip}(H-1)-R_f-\omega_1 L_f\right)s^3+\left((H-1)\left(\omega_1 K_{ip}+K_{ii}\right)-\omega_1 R_f\right)s^2+\omega_1 K_{ii}(H-1)s} \tag{4.52}$$

$$\alpha_5 = L_f C_f$$

$$\alpha_4 = C_f\left(R_f + \omega_1 L_f + K_{ip}\right)$$

$$\alpha_3 = C_f\left(R_f\omega_1 + K_{ii} + \omega_1 K_{ip}\left(1 + K_1 K_{vp}\right)\right) + K_{ip}K_{vp}$$

$$\alpha_2 = \omega_1 C_f\left(K_{ii} + K_1\left(K_{ii}K_{vp} + K_{ip}K_{vi}\right)\right) + K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_1 K_{ip}K_{vp}$$

$$\alpha_1 = \left(1 + C_f K_1\omega_1\right)K_{ii}K_{vi} + \omega_1\left(K_{ii}K_{vp} + K_{ip}K_{vi}\right)$$

$$\alpha_0 = \omega_1 K_{ii}K_{vi}$$

The admittance in (4.52) is obtained to investigate the effect of the compensator on the admittance ratio criterion. Further, to assess the DG interface stability with the RLV compensator and at different penetration levels of CILs, the characteristic equation that describes the system stability is obtained as the denominator of the following transfer function.

$$\frac{\Delta V_{od}}{\Delta U_{dc}} = \frac{\left(V_d^{\circ}/U_{dc}^{\circ}\right)(s+\omega_1)s^2}{a_5 s^5+a_4 s^4+a_3 s^3+a_2 s^2+a_1 s+a_0} \tag{4.53}$$

$$a_5 = L_f C_f$$

$$a_4 = -I_{od}^{\circ}L_f/V_{od}^{\circ} + C_f\left(R_f + \omega_1 L_f + K_{ip}\right)$$

$$a_3 = -I_{od}^{\circ}R_f/V_{od}^{\circ} - I_{od}^{\circ}L_f\omega_1/V_{od}^{\circ} + C_f\left(R_f\omega_1 + K_{ii} + K_{ip}\omega_1\right) - I_{od}^{\circ}K_{ip}(1-H)/V_{od}^{\circ} + K_{ip}K_{vp}\left(1 + C_f K_1\omega_1\right)$$

$$a_2 = -I_{od}^{\circ}R_f\omega_1/V_{od}^{\circ} - I_{od}^{\circ}\left(K_{ii} + K_{ip}\omega_1\right)(1-H)/V_{od}^{\circ} + C_f\omega_1 K_{ii} + \omega_1 K_{ip}K_{vp} + \left(K_{ip}K_{vi} + K_{ii}K_{vp}\right)\left(1 + C_f K_1\omega_1\right)$$

$$a_1 = -I_{od}^{\circ}K_{ii}\omega_1(1-H)/V_{od}^{\circ} + K_{ii}K_{vi}\left(1 + C_f K_1\omega_1\right) + \omega_1\left(K_{ip}K_{vi} + K_{ii}K_{vp}\right)$$

$$a_0 = \omega_1 K_{ii}K_{vi}$$

To assess the effect of the RLV on the ac voltage tracking performance, the output ac voltage tracking transfer function with the RLV compensator can be obtained as follows.

$$\frac{V_{od}}{V_{od}^{ref}} = \frac{\left[\begin{matrix}K_{ip}K_{vp}Z_l s^3 + \left(K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_1 K_{ip}K_{vp}\right)Z_l s^2 + \left(K_{ii}K_{vi} + \omega_1\left(K_{ip}K_{vi} + K_{ii}K_{vp}\right)\right)Z_l s \\ + K_{ii}K_{vi}\omega_1 Z_l\end{matrix}\right]}{\eta_5 s^5 + \eta_4 s^4 + \eta_3 s^3 + \eta_2 s^2 + \eta_1 s + \eta_0} \quad (4.54)$$

$$\eta_5 = L_f C_f Z_l$$

$$\eta_4 = L_f + C_f Z_l\left(R_f + \omega_1 L_f + K_{ip}\right)$$

$$\eta_3 = R_f + \omega_1 L_f + C_f Z_l\left(\begin{matrix}K_{ii} + \omega_1\left(\begin{matrix}R_f + K_{ip} \\ + K_1 K_{ip}K_{vp}\end{matrix}\right)\end{matrix}\right) - K_{ip}(H-1) + Z_l K_{ip}K_{vp}$$

$$\eta_2 = R_f\omega_1 + C_f Z_l\omega_1\left(K_{ii} + K_1\left(K_{ii}K_{vp} + K_{ip}K_{vi}\right)\right) - (H-1)\left(K_{ii} + \omega_1 K_{ip}\right) + Z_l\left(K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_1 K_{ip}K_{vp}\right)$$

$$\eta_1 = Z_l\left(K_{ii}K_{vi} + \omega_1\left(C_f K_1 K_{ii}K_{vi} + K_{ip}K_{vi} + K_{ii}K_{vp}\right)\right) - \omega_1 K_{ii}(H-1)$$

$$\eta_0 = \omega_1 Z_l K_{ii}K_{vi}$$

4.5.2.2 Reference-Inverter-Current (RIC) Compensator

The compensator signal is applied to the selector "2" in Figure 4.16. As shown, I_d is virtually increased by the injected compensator signal. This compensator replaces (4.20) by:

$$V_d^{ref} = \left(I_d^{ref} - I_d - N_2(s)V_{od}\right)G_i(s) - \omega L_f I_q + V_{od} \quad (4.55)$$

where $N_2(s)$ is the RIC compensator transfer function and is given by (4.51) with $n = 2$. The small-signal source admittance is derived when the RIC is applied as follows.

$$\frac{\Delta I_{od}}{\Delta V_{od}} = \frac{\beta_5 s^5+\beta_4 s^4+\beta_3 s^3+\beta_2 s^2+\beta_1 s+\beta_0}{-L_f s^4+\left(K_{ip}(H-1)-R_f-\omega_2 L_f\right)s^3+\Big((H-1)\left(\omega_2 K_{ip}+K_{ii}\right)-\omega_2 R_f\Big)s^2+\omega_2 K_{ii}(H-1)s} \quad (4.56)$$

$$\beta_5 = L_f C_f$$

$$\beta_4 = C_f\left(R_f + \omega_2 L_f + K_{ip}\right)$$

$$\beta_3 = C_f\left(R_f\omega_2 + K_{ii} + \omega_2 K_{ip}(1+K_2)\right) + K_{ip}K_{vp}$$

$$\beta_2 = \omega_2 C_f K_{ii}(1+K_2) + K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_2 K_{ip}K_{vp}$$

$$\beta_1 = K_{ii}K_{vi} + \omega_2\left(K_{ii}K_{vp} + K_{ip}K_{vi}\right)$$

$$\beta_0 = \omega_2 K_{ii}K_{vi}$$

To assess the DG interface stability with the RIC compensator and at different penetration levels of CILs, the output voltage (V_{od}) dynamics with respect to the inverter input dc voltage (U_{dc}) is given by:

$$\frac{\Delta V_{od}}{\Delta U_{dc}} = \frac{\left(V_d^{\circ}/U_{dc}^{\circ}\right)(s+\omega_2)s^2}{b_5 s^5+b_4 s^4+b_3 s^3+b_2 s^2+b_1 s+b_0} \quad (4.57)$$

$$b_5 = L_f C_f$$

$$b_4 = -I_{od}^{\circ}L_f/V_{od}^{\circ} + C_f\left(R_f + \omega_2 L_f + K_{ip}\right)$$

$$b_3 = -I_{od}^{\circ}R_f/V_{od}^{\circ} - I_{od}^{\circ}L_f\omega_2/V_{od}^{\circ} + C_f\left(R_f\omega_2 + K_{ii} + K_{ip}\omega_2(1+K_2)\right) - I_{od}^{\circ}K_{ip}(1-H)/V_{od}^{\circ} + K_{ip}K_{vp}$$

$$b_2 = -I_{od}^{\circ}R_f\omega_2/V_{od}^{\circ} - I_{od}^{\circ}\left(K_{ii} + K_{ip}\omega_1\right)(1-H)/V_{od}^{\circ} + C_f\omega_2 K_{ii}(1+K_2) + K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_2 K_{ip}K_{vp}$$

$$b_1 = -I_{od}^{\circ}K_{ii}\omega_2(1-H)/V_{od}^{\circ} + K_{ii}K_{vi} + \omega_2\left(K_{ip}K_{vi} + K_{ii}K_{vp}\right)$$

$$b_0 = \omega_2 K_{ii}K_{vi}$$

With the RIC compensator, the output voltage tracking dynamics is given by:

$$\frac{V_{od}}{V_{od}^{ref}} = \frac{\left[\begin{matrix}K_{ip}K_{vp}Z_l s^3+\left(K_{ip}K_{vi}+K_{ii}K_{vp}+\omega_2 K_{ip}K_{vp}\right)Z_l s^2+\Big(K_{ii}K_{vi}+\omega_2\left(K_{ip}K_{vi}+K_{ii}K_{vp}\right)\Big)Z_l s \\ +K_{ii}K_{vi}\omega_2 Z_l\end{matrix}\right]}{\mu_5 s^5+\mu_4 s^4+\mu_3 s^3+\mu_2 s^2+\mu_1 s+\mu_0} \quad (4.58)$$

$$\mu_5 = L_f C_f Z_l$$
$$\mu_4 = L_f + C_f Z_l\left(R_f + \omega_2 L_f + K_{ip}\right)$$
$$\mu_3 = R_f + \omega_2 L_f + C_f Z_l\left(K_{ii} + \omega_2\left(R_f + (1+K_1)K_{ip}\right)\right) - K_{ip}(H-1) + Z_l K_{ip} K_{vp}$$
$$\mu_2 = R_f \omega_2 + C_f Z_l \omega_2 K_{ii}(1+K_1) - (H-1)\left(K_{ii} + \omega_2 K_{ip}\right) + Z_l\left(K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_2 K_{ip} K_{vp}\right)$$
$$\mu_1 = Z_l\left(K_{ii}K_{vi} + \omega_2\left(K_{ip}K_{vi} + K_{ii}K_{vp}\right)\right) - \omega_2 K_{ii}(H-1)$$
$$\mu_0 = \omega_2 Z_l K_{ii} K_{vi}$$

4.5.2.3 Reference-Inverter-Voltage (RIV) Compensator

As shown in Figure 4.16, with the selector at position "3", the RIV compensator modifies the direct component of the reference inverter voltage by injecting the active compensation signal. The injected reference inverter voltage is proportional to the capacitor current, and accordingly a virtual damping resistor is yielded. The modified small-signal source admittance is shown in (4.59).

$$\frac{\Delta I_{od}}{\Delta V_{od}} = \frac{\gamma_5 s^5 + \gamma_4 s^4 + \gamma_3 s^3 + \gamma_2 s^2 + \gamma_1 s + \gamma_0}{-L_f s^4 + \left(K_{ip}(H-1) - R_f - \omega_3 L_f\right)s^3 + \left((H-1)(\omega_3 K_{ip} + K_{ii}) - \omega_3 R_f\right)s^2 + \omega_3 K_{ii}(H-1)s} \quad (4.59)$$
$$\gamma_5 = L_f C_f$$
$$\gamma_4 = C_f\left(R_f + \omega_3 L_f + K_{ip}\right)$$
$$\gamma_3 = C_f \omega_3\left(R_f + K_{ip} + K_3\right) + C_f K_{ii} + K_{ip} K_{vp}$$
$$\gamma_2 = \omega_3 C_f K_{ii} + K_{ip} K_{vi} + K_{ii} K_{vp} + \omega_3 K_{ip} K_{vp}$$
$$\gamma_1 = K_{ii} K_{vi} + \omega_3\left(K_{ii} K_{vp} + K_{ip} K_{vi}\right)$$
$$\gamma_0 = \omega_3 K_{ii} K_{vi}$$

Further, to assess the DG interface stability with the RIV compensator and at different penetration levels of CILs, the output voltage dynamics with respect to the inverter input dc voltage is derived in (4.60) with the denominator as the characteristic equation that describes the DG interface stability.

$$\frac{\Delta V_{od}}{\Delta U_{dc}} = \frac{\left(V_d^{\circ}/U_{dc}^{\circ}\right)(s+\omega_3)s^2}{c_5 s^5 + c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s + c_0} \quad (4.60)$$

$$c_5 = L_f C_f$$

$$c_4 = -I_{od}^{\circ} L_f / V_{od}^{\circ} + C_f\left(R_f + \omega_3 L_f + K_{ip}\right)$$

$$c_3 = -\frac{I_{od}^{\circ} R_f}{V_{od}^{\circ}} - \frac{I_{od}^{\circ} L_f \omega_3}{V_{od}^{\circ}} + C_f \begin{pmatrix} R_f \omega_3 + K_{ii} \\ +\omega_3\left(K_{ip} + K_3\right) \end{pmatrix} - \frac{I_{od}^{\circ} K_{ip}(1-H)}{V_{od}^{\circ}} + K_{ip} K_{vp}$$

$$c_2 = -\frac{I_{od}^{\circ} R_f \omega_3}{V_{od}^{\circ}} - \frac{I_{od}^{\circ}\left(K_{ii} + K_{ip}\omega_3\right)(1-H)}{V_{od}^{\circ}} + C_f \omega_3 K_{ii} + K_{ip} K_{vi} + K_{ii} K_{vp} + \omega_3 K_{ip} K_{vp}$$

$$c_1 = -I_{od}^{\circ} K_{ii} \omega_3 (1-H) / V_{od}^{\circ} + K_{ii} K_{vi} + \omega_3\left(K_{ip} K_{vi} + K_{ii} K_{vp}\right)$$

$$c_0 = \omega_3 K_{ii} K_{vi}$$

With the RIV compensator, the output voltage tracking dynamics can be given by:

$$\frac{V_{od}}{V_{od}^{ref}} = \frac{\begin{bmatrix} K_{ip}K_{vp}Z_l s^3 + \left(K_{ip}K_{vi} + K_{ii}K_{vp} + \omega_3 K_{ip}K_{vp}\right)Z_l s^2 + \left(K_{ii}K_{vi} + \omega_3\left(K_{ip}K_{vi} + K_{ii}K_{vp}\right)\right)Z_l s \\ + K_{ii}K_{vi}\omega_3 Z_l \end{bmatrix}}{\xi_5 s^5 + \xi_4 s^4 + \xi_3 s^3 + \xi_2 s^2 + \xi_1 s + \xi_0} \quad (4.61)$$

$$\xi_5 = L_f C_f Z_l$$

$$\xi_4 = L_f + C_f Z_l\left(R_f + \omega_3 L_f + K_{ip}\right)$$

$$\xi_3 = R_f + \omega_3 L_f + C_f Z_l\left(K_{ii} + \omega_3\left(R_f + K_3 + K_{ip}\right)\right) - K_{ip}(H-1) + Z_l K_{ip} K_{vp}$$

$$\xi_2 = R_f \omega_3 + C_f Z_l \omega_3 K_{ii} - (H-1)\left(K_{ii} + \omega_3 K_{ip}\right) + Z_l\left(K_{ip} K_{vi} + K_{ii} K_{vp} + \omega_3 K_{ip} K_{vp}\right)$$

$$\xi_1 = Z_l\left(K_{ii} K_{vi} + \omega_3\left(K_{ip} K_{vi} + K_{ii} K_{vp}\right)\right) - \omega_3 K_{ii}(H-1)$$

$$\xi_0 = \omega_3 Z_l K_{ii} K_{vi}$$

4.5.3 Performance Analysis of The Proposed Active Damping Techniques

4.5.3.1 Damping Capabilities

The preceding mathematical analysis is utilized in this part to investigate the damping capabilities and performance of the proposed compensators. Using the small-signal source admittances in (4.52), (4.56) and (4.59), Nyquist plots are provided in Figure 4.17 to investigate the effect of the aggregated CILs on the ac micro-grid stability. As shown, Nyquist contours approach the (-1, 0) point with the uncompensated case implying very low stability margin. On the same figure, a passive damping due to direct resistive load of 0.1p.u. is obtained. However, with 0.1p.u, the system damping

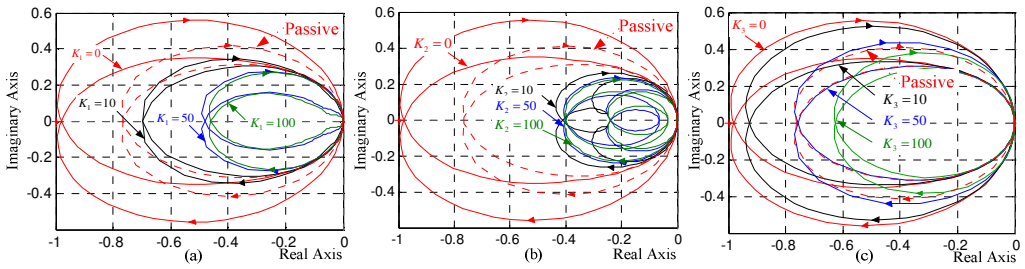

Figure 4.17: Admittance ratio criterion – uncompensated, passive damped and: (a) RLV compensator. (b) RIC. (c) RIV compensator.

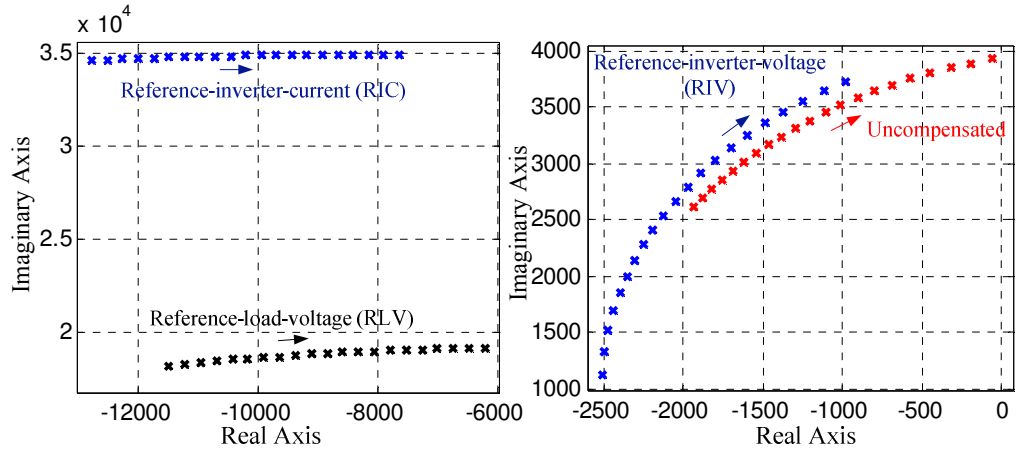

Figure 4.18: Dominant pole loci for VSI as an interface for ac micro-grid with proposed active damping controllers. Loading increases from 0 to 1.0 pu with the direction of the arrow.

has not been improved enough. This proves that relying on the resistive nature of the micro-grid loads is not sufficient.

With the proposed compensators, the stability margin increases with the increase of the compensator gain due to the increased mapping range of the lightly-damped modes to the closed loop system. For fair comparison, the cut-off frequency for the compensator LPF is selected to be 1000 rad/sec for all compensators with similar steps in the active compensation gains (10, 50, 100). It is clear that the reference-inverter-current (RIC) compensator has the best damping capabilities, while the reference-load-voltage (RLV) compensator comes after. The reference-inverter-voltage (RIV) compensator has the lowest damping capability. With compensator gain of 50; its damping is equivalent to a passive damping capability of 0.1p.u. due to direct resistive load.

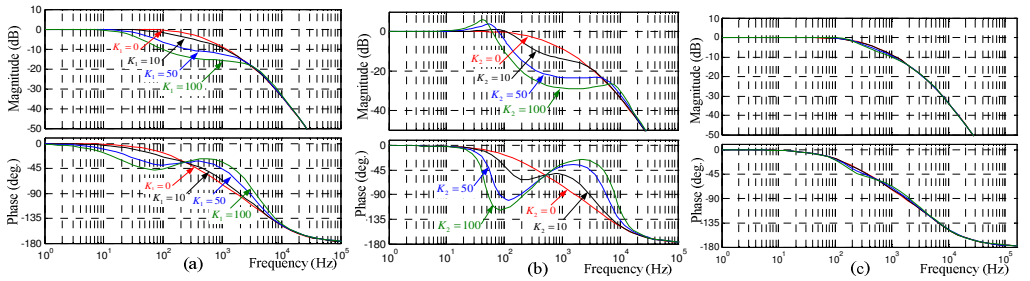

Figure 4.19: Influence of the proposed compensators on the ac voltage tracking. (a) RLV compensator. (b) RIC compensator. (c) RIV compensator.

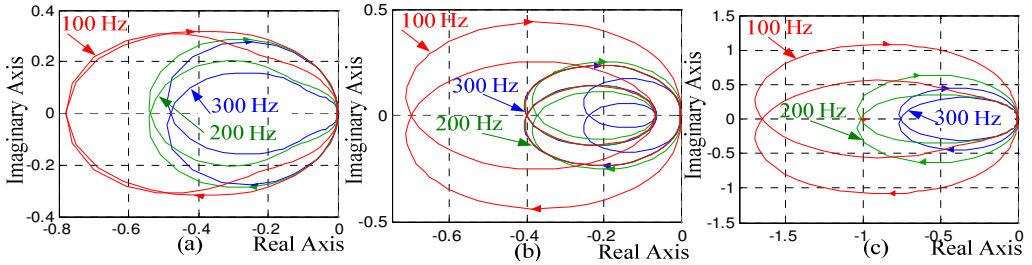

Figure 4.20: Stability robustness with ac voltage controller bandwidth variations. (a) RLV. (b) RIC. (c) RIV compensator.

The compensator gains and cut-off frequency are designed based on root-locus plots of the dominant pole loci. For the uncompensated system when loaded by aggregated tightly-regulated loads, root-locus plots are shown in Figure 4.18. As the loading increases from 0 to 1.0 p.u., the damping coefficient decreases significantly from -1941 to -53.25 s^{-1}, respectively, which subject the overall stability to collapse due to any possible disturbances. The dominant pole loci with the proposed compensators are depicted with active compensator gain of 50 and cut-off frequency of LPF of 1000 rad/sec using the denominator of (4.53), (4.57) and (4.60). As the power increases from 0 to 1p.u., the damping coefficients of the reference-inverter- current, reference-load-voltage, and reference-inverter-voltage compensators decreases from -12770, -11070 and -2511 s^{-1} to -7648, -5857, -980 s^{-1} which reflects the damping capabilities of those compensators.

4.5.3.2 AC Voltage Tracking

Figure 4.19 shows the frequency responses of the load voltage transfer functions in (4.54), (4.58) and (4.61). The uncompensated case is also plotted on the each figure. Note that the designed ac voltage controller bandwidth is around 300 Hz. For the RLV

compensator, the ac voltage controller bandwidth decreased to 150, 50, and 30 Hz with a virtual gain of 10, 50, and 100 respectively. For RIC compensator, the ac voltage controller bandwidth decreased to 160, 100 and 100 Hz with the same virtual gains. The RIV compensator almost doesn't affect the ac voltage controller dynamics as the bandwidths are 300, 280 and 250 Hz with the same virtual gains. This isolation from the voltage controller dynamics is due to injecting the compensation signal to the most inner control loop avoiding interactions with the ac voltage controller [selector "3" in Figure 4.16].

4.5.3.3 Interactions with the AC Voltage Controller Bandwidth

The voltage controller directly affects the stability due its relatively small bandwidth, as compared to the current controller. Further, the active compensator dynamics interact with the DG interface controller and might affect the overall system stability. Therefore, the system stability with each active compensator, is evaluated under parameter variations in the ac voltage controller bandwidth. Figure 4.20(b) shows that the interface dynamics with the RIC compensator has the same stability margin with 300 and 200 Hz ac voltage controller bandwidth, whereas the stability margin decreases significantly with a bandwidth of 100 Hz. A similar behavior is shown in Figure 4.20(a) when the RLV compensator is applied.

On the contrary, the system stability is very sensitive to the decrease in the ac voltage controller bandwidth when the reference-inverter-voltage compensator is used. Figure 4.20(c) indicates that the system becomes unstable with 200 and 100 Hz bandwidth.

It can be noted that with appropriate design and coordination between converter control parameters and the active damping controller, interactions between the active damping controller and the ac voltage controller can be minimized. As a result, a highly damped control performance can be yielded without affecting the ac voltage tracking requirements. On the other hand, the presence of the active damping controller maps the frequency modes of voltage disturbance within the stable closed loop voltage control dynamics. Therefore, better disturbance rejection can be yielded under load/network disturbances.

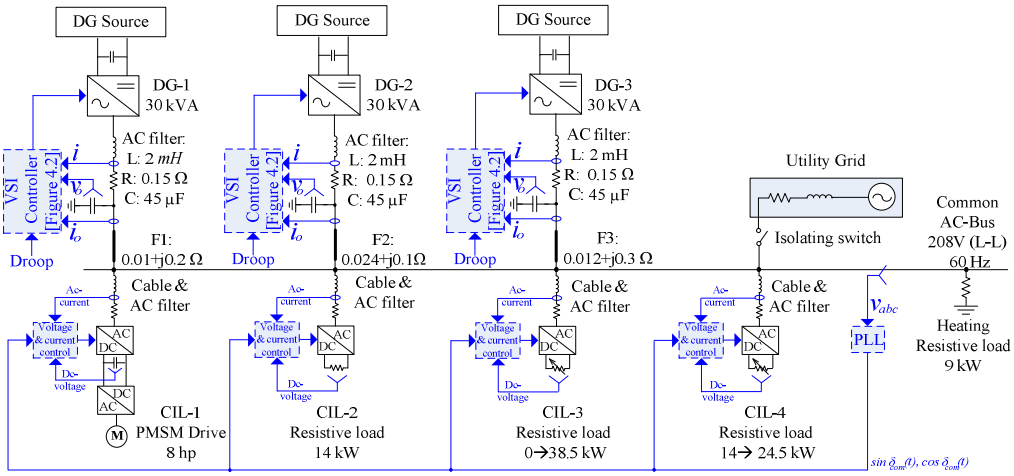

Figure 4.21: Schematic diagram of the implemented ac micro-grid.

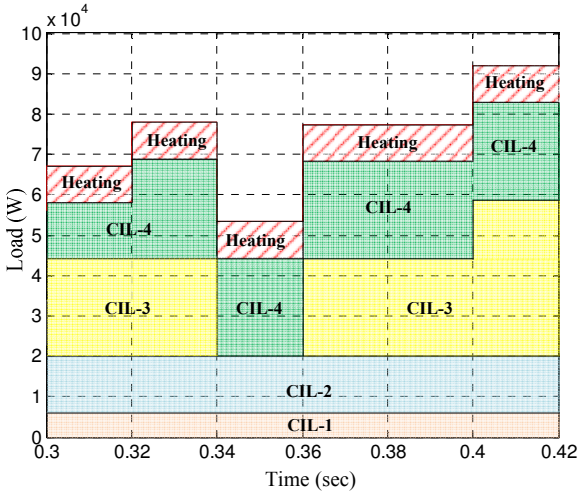

Figure 4.22: Implemented ac micro-grid loading curve in the 0.3→0.42 sec interval.

4.5.4 Evaluation Results

To investigate the effectiveness of the proposed active compensators in a micro-grid system with reasonably large number of power converters, a low voltage ac micro-grid system, rated at 90 kVA, is implemented under the Matlab/Simulink® environment. Figure 4.21 shows a schematic of the ac micro-grid system under study. The system consists of three DG units: DG-1, DG-2 and DG-3 each is with rated power of 30 kVA. At the load-side, four CILs are implemented. CIL-1 is an 8 hp PMSM drive system interfaced to the micro-gird via back-to-back PWM voltage-sourced controlled converters; CIL-2 is a 14 kW PWM voltage-sourced controlled-rectifier feeding a resistive load; CIL-3 is a 38.5 kW voltage-sourced controlled-rectifier feeding a

variable resistive load; and CIL-4 is a 24.5 kW voltage-sourced controlled-rectifier feeding a variable resistive load. All network-connected converters employ the standard voltage-oriented control strategy. For each DG unit, the VSI controller in Figure 4.2 is employed to define the local phase angle and the reference ac voltage at the LC filter capacitor. On the load-side, a PLL is employed at the common ac-bus to determine the common phase angle ($\delta_{com}(t)$) that is needed for voltage-oriented control at each CIL. A direct 9 kW resistive load (heating load) can be connected to the load bus to investigate the effect of the resistive load to the damping capabilities. The complete system parameters are given in the Appendix A4.4.

The micro-grid loading curve is shown in Figure 4.22. As shown, CIL-1 and 2 are base-loads whereas CIL-3 and 4 are variable loads. The load curve is characterized by sudden loading/unloading to evaluate the system stability under dynamic loading conditions. For the sake of performance comparison, the micro-grid performance is evaluated under the following scenarios:

1) Micro-grid system works parallel to the main grid.
2) Autonomous micro-grid operation without passive or active damping.
3) Autonomous micro-grid operation with passive damping (due the resistive heating load).
4) Autonomous micro-grid operation with proposed active damping controllers (no heating load).

4.5.4.1 Grid-Connected Micro-grid

In this scenario, the micro-grid system is connected to the low voltage utility-grid, i.e. the micro-grid isolation switch in Figure 4.21 is closed. The loading curve in Figure 4.22 is applied without the heating load to test the micro-grid stability in the grid-connected mode without the passive damping effect associated with resistive loads. Figure 4.23 shows the micro-grid performance in the grid-connected mode. Figure 4.23(a) shows the load-bus voltage, whereas Figure 4.23(b) shows the instantaneous *d*-axis component of the load-bus voltage. Figure 4.23(c) shows the total active power delivered to the load-bus. The dc-bus voltage of the CIL-2 is shown in Figure 4.23(d), the stator voltage components of the motor drive are shown in Figure 4.23(e), and the developed electromagnetic torque of the motor drive is shown in Figure 4.23(f). It can

be noted that stable and damped responses are obtained at different loading conditions. In spite of the negative admittance effect associated with the CILs, the aggregated source admittance (of DG units and the relatively strong grid with respect to the DG units) meets the Nyquist criterion with respect to the load admittances reflected to the load-bus. The stabilized load-bus voltage is reflected to the load-side, where the load-side performance is stabilized as well. Therefore, the operation of converter-dominated micro-grids parallel to the main grid improves the micro-grid stability, particularly in strong grids.

4.5.4.2 Autonomous Micro-grid Operation without Passive or Active Damping

In this scenario, the micro-grid system operates autonomously to the supply the connected loads, i.e. the micro-grid isolation switch in Figure 4.21 is opened. The loading curve in Figure 4.22 is applied without the heating load to test the micro-grid stability in the autonomous mode without the passive damping effect associated with resistive loads. Figure 4.24 shows the micro-grid performance in the autonomous mode. Figure 4.24(a) shows the load-bus voltage, whereas Figure 4.24(b) shows the instantaneous *d*-axis component of the load-bus voltage. Due to the tight regulation performance of CILs, poorly damped transient response is yielded even with relatively small load disturbances (e.g. 10 kW (0.1 p.u.) at t = 0.32 s). With relatively larger loading disturbances (e.g. 23 kW (0.25 p.u.) at t = 0.36 s), the micro-grid system can be driven into instability. It can be noted that instability effect occurs at loading levels, which are below the micro-grid rating. In other words, the micro-grid may have a reasonable reserve margin (e.g. 0.25 p.u. at t = 0.36 s) and suffers from instability due the high penetration of the CILs. The load-bus voltage builds up at t = 0.4 s with an additional increase in the load demand. The response of the injected active power is shown in Figure 4.24(c), which maps the voltage instability. Large circulating powers are yielded, which yields to remarkable overload for power converters, which are characterized by their limited thermal capacity. The instability of the load-bus voltage is reflected to the load-side performance. The dc-bus voltage of the CIL-2 is shown in Figure 4.24(d), the stator voltage components of the motor drive are shown in Figure 4.24(e), and the developed electromagnetic torque of the motor drive is shown in Figure 4.24(f).

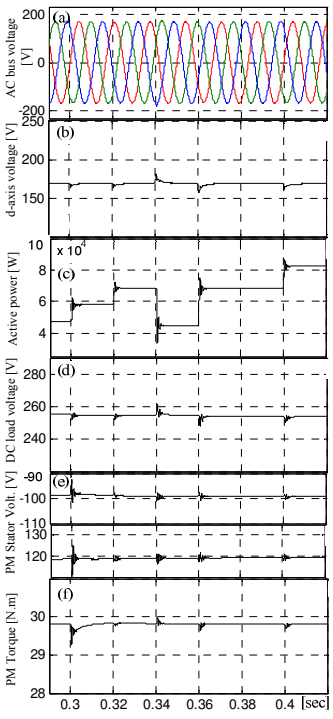

Figure 4.23: System response – Grid-connected, no heating loads.

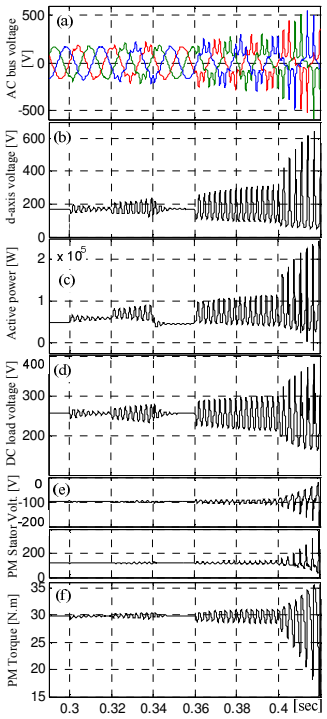

Figure 4.24: System response – uncompensated case.

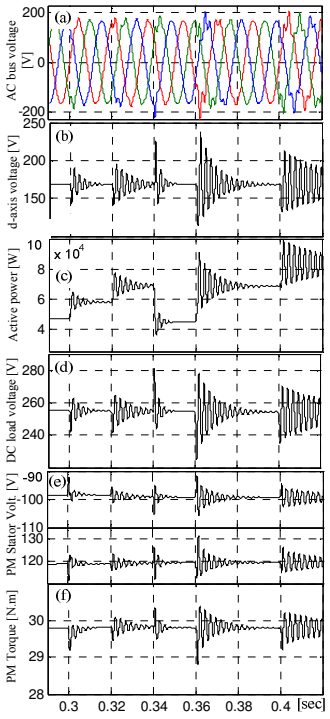

Figure 4.25: System response – uncompensated case with 9 kW heating load

(a) 3-phase ac common bus voltage. (b) *d*-component of the ac common bus voltage. (c) Delivered active power to the ac common bus. (d) Dc voltage at the load-side for CIL-2. (e) PMSM stator voltages in CIL-1 (top: *d*-axis, bottom: *q*-axis). (f) PMSM torque in CIL-1.

4.5.4.3 Autonomous Micro-grid Operation with Passive Damping

In this scenario, the micro-grid system operates autonomously to the supply the connected loads, i.e. the micro-grid isolation switch in Figure 4.21 is opened. The loading curve in Figure 4.22 is applied with the heating load (9 kW (0.1 p.u.) direct resistive load connected at the load-bus) to test the micro-grid stability in the autonomous mode with the passive damping effect associated with resistive loads. In the presence of the resistive load, additional passive damping is propagated to the equivalent load seen by each DG unit. As a result, the Nyquist stability criterion can be satisfied by increasing the load-side admittance. Similarly, the equivalent *R/L* ratio, as seen by each DG unit, increases as well which satisfies the Routh Hurwitz stability conditions in (4.6) and (4.7). Figure 4.25 shows the system response with the direct resistive load is added to the load-side. As shown in Figure 4.25(a), (b), the load-bus

voltage is more damped as compared to the uncompensated system. The active power delivered to the load-side experiences better damping characteristics as shown in Figure 4.25(c). The load-side performance is improved as well due to the damping effect associated with the passive load as shown in Figure 4.25(d), (e), (f). Although an improved damped response is yielded, the system performance is still unaccepted. In Figure 4.25(b), the over (>1) or under (<1) shoots in the *d*-component of the load-bus voltage are 0.85, 0.82, 1.32, 0.67, 0.77 p.u. at t = 0.3, 0.32, 0.34, 0.36 and 0.4 s, respectively. Further, the duration of system oscillation is high, which implies higher time for circulating powers among power converters and higher overload burden on these converters. Large voltage disturbances and poorly damped performance directly affect the sensitive CILs.

Relying on the inherent passive damping associated with resistive loads might not be the optimum solution to preserve micro-grid stability. Therefore, the substantial role of the active compensators appears as a viable solution

4.5.4.4 Autonomous Micro-grid Operation with Proposed Active Compensators

Figure 4.26, 4.27 and 4.28 respectively, show the system response when the proposed RLV, RIC and RIV compensators are utilized. The active compensator gain is selected to be 50 with a cut-off frequency of 1000 rad/sec. For the load-bus voltage, the response is more damped as compared to the uncompensated or the passively damped system. Obviously, the RIC compensator has the highest damping capability. With the RLV compensator, the overshoot (>1) and undershoot (<1) in the *d*-axis components of the load-bus voltage are 0.92, 0.91, 1.18, 0.84 and 0.89 p.u. at the loading/unload instants t = 0.3, 0.32, 0.34, 0.36 and 0.4 s; respectively, whereas the corresponding values are 0.96, 0.96, 1.06, 0.94 and 0.95 p.u. for the RIC which implies the superiority of the RIC in preserving the system stability while maintaining high power quality voltage profile. With the RIV compensator, the corresponding load-bus voltage over/undershoots are 0.84, 0.84, 1.34, 0.67 and 0.77 p.u. It can be noted that the damping performance of the RIV is similar to that of the 0.1 p.u. resistive load passive damping; however, the RIV compensator has faster response with much lower settling time.

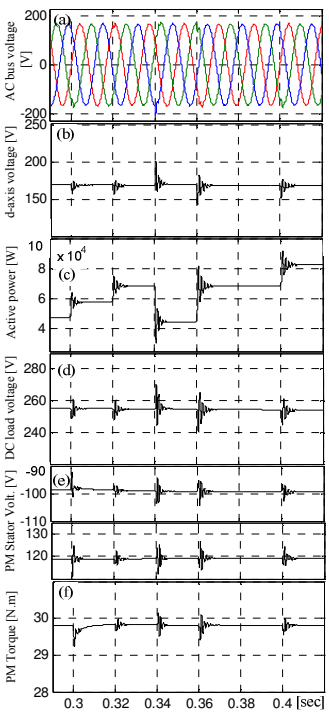

Figure 4.26: System response – RLV compensator, without heating load.

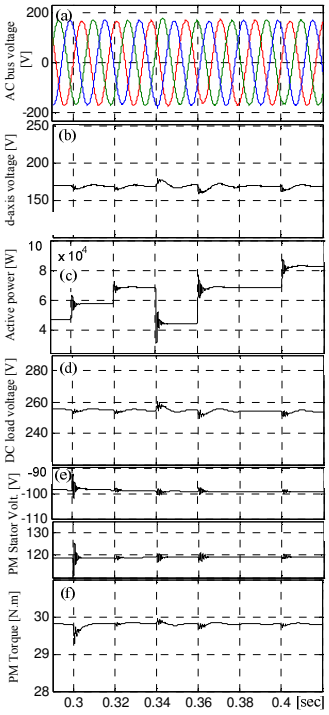

Figure 4.27: System response – RIC compensator, without heating load.

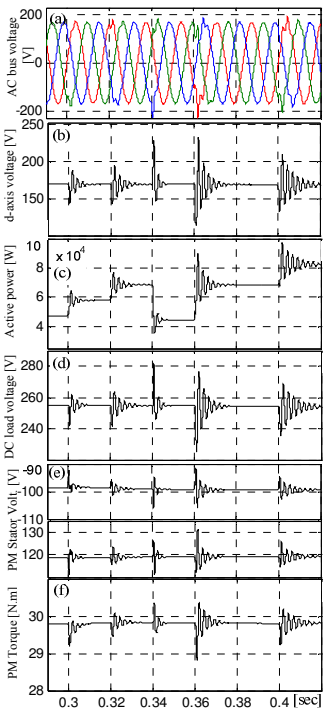

Figure 4.28: System response – RIV compensator, without heating load.

(a) 3-phase ac common bus voltage. (b) *d*-component of the ac common bus voltage. (c) Delivered active power to the ac common bus. (d) Dc voltage at the load-side for CIL-2. (e) PMSM stator voltages in CIL-1 (top: *d*-axis, bottom: *q*-axis). (f) PMSM torque in CIL-1.

The delivered active power responses, shown in Figure 4.26(c), 4.27(c), and 4.28(c) follow the same damping capabilities for the active compensators. In all cases, power oscillations are remarkably reduced, which implies less circulating power and reduced overload stress imposed on micro-grid converters. The load-side performance, shown in Figure 4.26, 4.27, 4.28(d)-(f), is remarkably improved with active damping, even with the RIV compensator. Therefore, the interactions between micro-grid converters and CILs can be remarkably reduced by stabilized the load-bus voltage with sufficient damping capability.

4.5.5 Conclusion

This Chapter introduced the interaction dynamics instabilities in ac micro-grid systems. Two approaches are considered for the interfacing VSI as follows:

Table 4.1 Comparison of the Proposed Compensators from the VSI side (SSC)

	Damping Capabilities	Robustness against Voltage-Controller Parameters	Influence on Load-Voltage Tracking
RLV	Moderate	High	Moderate
RIC	High	High	High
RIV	Low	Low	Low

- Exact CIL modeling and stabilization from the load-side. In this case, a VSR is taken as an exact CIL and a LSC (MFC and HFC) are proposed to satisfy the Nyquist criterion with the output admittance of the source VSI. MFC is employed with BP filtering characteristics to allow input admittance reshaping around a designed frequency region whereas HFC is utilized to mimic a virtual resistance connected in series with the ac filter capacitor of the VSR to damp the resonant peaks. This approach depends on exact input/output admittance matching and obviously it is load-dependent solution. Both compensators are employed in a modeled system using Matlab/Simulink platform to verify the analytical results and their effectiveness.
- The second approach is more generic with load-independent solutions. Augmented generic CILs model is considered as a negative resistance in the whole frequency range as a worst modeling case of the load-side. Three active compensators are proposed from the source-side (SSC) to stabilize the VSI for the DG unit. Modeling and analysis of typical micro-grid sources and loads have been presented. Compensated sources admittance and modified voltage tracking dynamics have been derived under the presence of the proposed active damping compensators to facilitate multi-objective design of the active damping controllers with reduced interactions with existing converter control loops. Table 4.1 depicts the main differences among the proposed compensators. Evaluation results, based on a detailed model of an ac micro-grid with multiple tightly-regulated CILs, have been provided to validate the developed models and to assess the effectiveness and robustness of proposed techniques.

Chapter 5

Assessment and Mitigation of Interaction Dynamics in Hybrid AC/DC Grids in DG Systems[1]

5.1 Introduction

Hybrid ac/dc power networks are recently emerged in DG systems with widespread acceptance under the smart grids environment. Therefore, both ac and dc micro-grids are integrated via bidirectional PE converters to reduce the number of multiple ac-dc and dc-ac conversions stages, and accordingly improve overall system efficiency and reliability. However, system-level dynamic interactions can be yielded in hybrid networks due to the active control nature and tight regulation of power converters to meet load/generation requirements. This Chapter presents an assessment and mitigation strategies of such interactions in hybrid networks.

Figure 5.1 shows the system structure of a hybrid ac/dc converter dominated network that contains typical PE interfaces in DG systems. As shown, a dc DG park is formed by multiple DG units that are all interfaced by PE converters. An ac micro-grid is terminated by an interfacing VSI to supply local loads via distribution feeders. A grid-connected VSI is also considered to interface the utility-grid to the hybrid network. A static switch (SW) is employed to allow switching capability between micro-grid and grid-connected mode of operation in case of local faults at the grid-side. A dc micro-grid is also considered in the hybrid network and is supplied directly from the common dc-link. As shown, dc micro-grid is highly penetrated by CILs including motor drives and resistive loads interfaced by dc-dc converters. With the emerging needs of highly reliable supplies, the dc micro-grid shown in Figure 5.1 secures two ways of supplies; from DG Park and/or utility-grid. Thus, it may include

[1] *Publications out of this Chapter:*

A. A. A. Radwan and Y. A.-R. I. Mohamed, "Assessment and Mitigation of Interaction Dynamics in Hybrid ac/dc Converter Dominated Networks in Distribution Generation Systems," Submitted for publication in *IEEE Transactions on Smart Grids. Manuscript ID: TSG-00550-2011.*

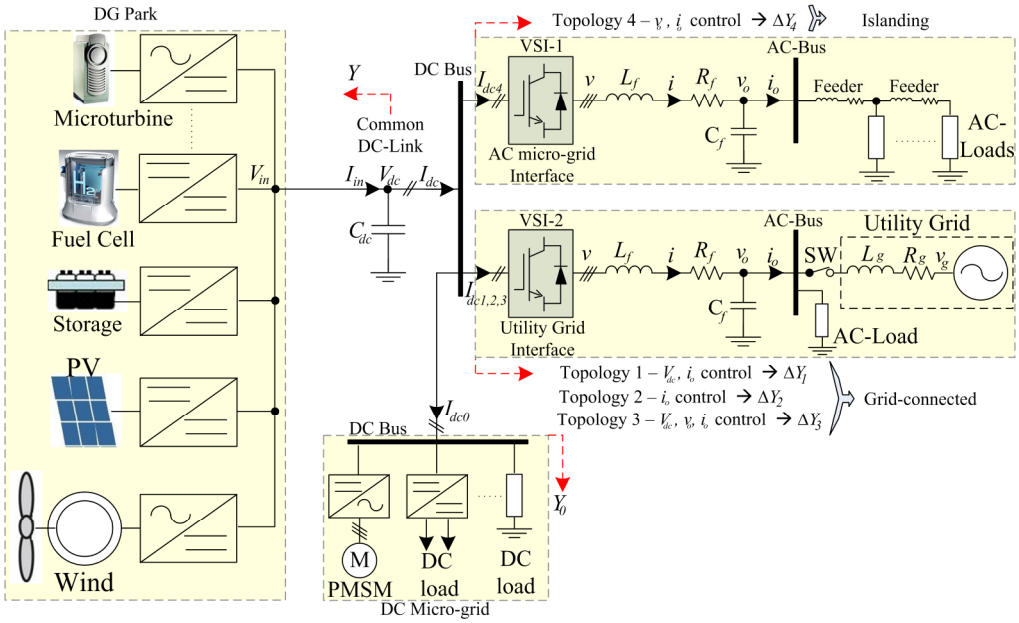

Figure 5.1: Ac, dc micro-grid and DG system configuration as a hybrid grid.

sensitive loads such as data centers, industrial machineries and other critical loads in hospitals, airports or military campuses.

Firstly, mathematical modeling and analysis of the dc-side source/load admittances of typical hybrid network entities are provided. The system in Figure 5.1 can be treated as a multi-converter network with one source (output) dc admittance (Y) for the aggregated DG park, and three load (input) dc admittances for islanded dc micro-grids, grid-connected VSI and ac micro-grid, respectively. The dc-side admittance models are obtained under different operating modes and control functions, such as grid-connected (weak and stiff) and isolated micro-grids with dispatchable and non-dispatchable DG units. For the dc micro-grid, augmented model is considered based on high penetration level of CILs to the dc-bus. Sensitivity functions of the output ac current and voltage of the VSI against dc-link disturbances are obtained. Systematic control loop design guidelines are also provided under different modes of DG operation and control functions. The developed small signal models are verified using time-domain large-signal models under Matlab/Simulink environment.

Secondly, the provided dc-side load/source admittances will be used to assess the system stability based on the Nyquist admittance ratio criterion. This criterion can be violated in two frequency regions; low frequency region due to the equivalent source

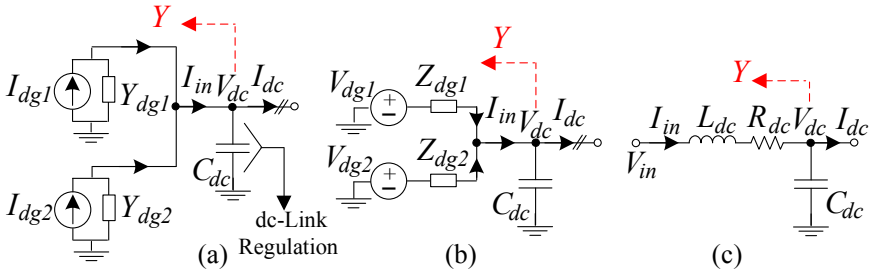

Figure 5.2: Equivalent models for DG units. (a) Non-dispatchable DG units. (b) Dispatchable DG units. (c) Circuit model for the equivalent DG source admittance.

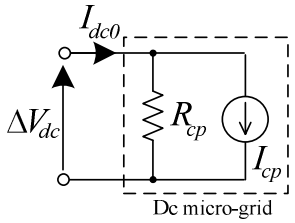

Figure 5.3: Dc micro-grid small-signal augmented model.

admittance of the DG park; and high frequency region due to the resonant peak of the equivalent ac-*LCL* filter of the ac micro-grid converter. However, the high frequency violation region can be mitigated by using an active damping loop, whereas the low frequency violation region is more challenging with a considerable destabilizing effect. Further, it can be shown that the tight regulation of power converter interfaces introduces the ac micro-grid or utility-grid interface as an incremental negative admittance to the common dc-link which significantly degrades the system stability margin. Therefore, active compensators are proposed to actively reshape the input dc-side admittance of the ac micro-grids and grid-connected inverters so that the Nyquist criterion is satisfied. Time-domain large-signal model of a typical hybrid network is implemented using Matlab/Simulink® environment to validate the analytical results.

5.2 Modeling of DC-side Output Admittance of DG Park

The DG park shown in Figure 5.1 consists of multiple dispatchable and non-dispatchable DG units. The dc-link voltage should be regulated by the interfacing VSI if source units are non-dispatched such as PV arrays and variable-speed WTG. In dispatched DG units, such as batteries or fuel cells, no dc-link voltage regulation is required from the VSI device [40], [116]. As shown in Figure 5.2(a), non-dispatchable

DG sources are equivalently modeled by a current source that injects dc current (I_{dg}) to the dc-link capacitor (C_{dc}), thus a dc-link voltage controller from the VSI side is required to regulate the charging/discharging process of C_{dc}. For dispatchable DG units, a dc voltage source (V_{dg}) is used with no dc-link control from VSI side as shown in Figure 5.2(b). Figure 5.2(c) shows a generic equivalent circuit model for the lump-summed source admittance (Y) of the dc DG park. The equivalent source admittance consists of the common dc-link capacitor with a series resistance (R_{dc}) and inductance (L_{dc}) to represent the output impedance of the DG converters, parasitic resistance, system wirings and cabling within the DG park [50], [124]. Thus, the small-signal output admittance for the DG park is obtained as follows.

$$Y(s) = \frac{L_{dc}C_{dc}s^2+R_{dc}C_{dc}s+1}{L_{dc}s+R_{dc}} \tag{5.1}$$

5.3 Modeling of DC-side Input Admittance of Augmented DC Micro-grid

As shown in Figure 5.1, the dc micro-grid is highly penetrated by CILs which degrade system stability due to the equivalent CP operational mode. The input dc current injected to the dc micro-grid (I_{dc0}) is given by:

$$I_{dc0} = P_0/V_{dc} \tag{5.2}$$

where P_0 is the delivered dc power to the dc micro-grid. Under the CP mode of operation, the small-signal linearization of (5.2) is given by:

$$\Delta Y_0 = \Delta I_{dc0}/\Delta V_{dc} = -P_0^{\circ}/V_{dc}^{\circ 2} \tag{5.3}$$

$$\Delta I_{dc0} = \underbrace{-\left(P_0^{\circ}/V_{dc}^{\circ 2}\right)}_{1/R_{cp}}\Delta V_{dc} + \underbrace{2P_0^{\circ}/V_{dc}^{\circ}}_{I_{cp}} \tag{5.4}$$

As shown in Figure 5.3 and (5.4), the aggregated dc micro-grid with multiple CILs can be represented in the small-signal sense, by a negative resistance (R_{cp}) in parallel with a constant current source (I_{cp}) to represent the CP mode [82].

5.4 Modeling of DC-side Input Admittance of VSI in Micro-grid Applications

The current and ac voltage dynamics of the power circuits are modeled in the *d-q* frame that rotates synchronously with the inverter output voltage angular speed ω by [125]:

$$V_d - V_{od} = I_d\left(R_f + sL_f\right) - \omega L_f I_q \tag{5.5}$$

$$V_q - V_{oq} = I_q\left(R_f + sL_f\right) + \omega L_f I_d \tag{5.6}$$

$$I_d - I_{od} = sC_f V_{od} - \omega V_{oq} C_f \tag{5.7}$$

$$I_q - I_{oq} = sC_f V_{oq} + \omega V_{od} C_f \tag{5.8}$$

where V_d, V_q, I_d and I_q are the *d-q* axis inverter output voltages and currents; V_{od}, V_{od}, I_{od} and I_{oq} are the *d-q* axis ac-bus voltages and injected currents; R_f, L_f and C_f are the per-phase resistance, inductance and capacitance of the *LC* filter, respectively; and s is the Laplace operator. In grid-connected mode, the *d-q* transformation is performed using the grid voltage angle as the common reference whereas virtual PLL is employed in islanded mode of operation.

In the *d-q* synchronous reference-frame, a VSI injects an active (P_o) and reactive (Q_o) power that are delivered to the ac common bus and given by:

$$P_o = 1.5\left(V_{od}I_{od} + V_{oq}I_{oq}\right) \tag{5.9}$$

$$Q_o = 1.5\left(V_{od}I_{oq} - V_{oq}I_{od}\right) \tag{5.10}$$

Assuming high efficient PE converter, so that the input power delivered from the dc-link $(V_{dc}I_{dc})$ is equal to the instantaneous output power delivered by the inverter terminals $\left(P = 1.5\left(V_d I_d + V_q I_q\right)\right)$, the ac-dc power balance is governed by:

$$V_{dc}I_{dc} = 1.5\left(V_d I_d + V_q I_q\right) \tag{5.11}$$

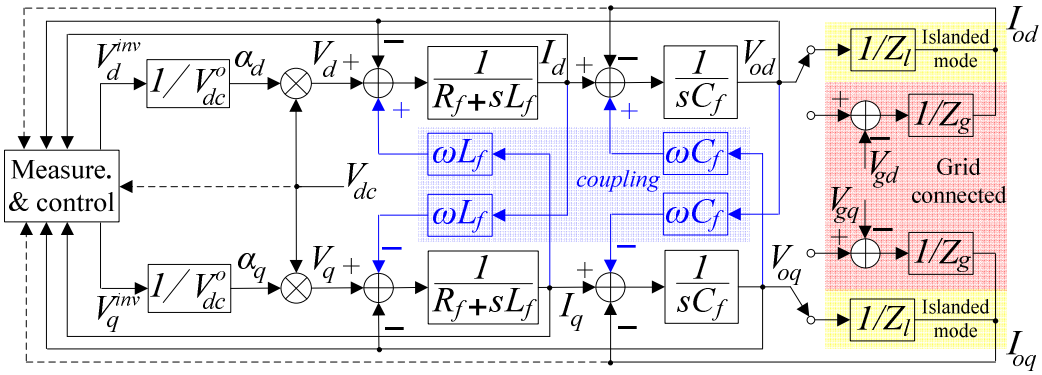

Figure 5.4: Large-signal model for ac micro-grid interface – grid-connected and islanded mode.

In the dc-side of the VSI, assuming lossless power conversion, the dc power balance dynamics are described by:

$$V_{in}I_{in} - V_{dc}I_{dc} = 0.5C_{dc}sV_{dc}^2 \tag{5.12}$$

where $V_{in}I_{in}$ is the dc power delivered from the DG sources, $V_{dc}I_{dc}$ is the filtered instantaneous power delivered from the dc capacitor while the RHS term is the rate of change in the energy of the dc-link capacitor.

If the VSI is tied to the grid, the ac voltage and current dynamics are governed by the grid dynamics as follows.

$$\begin{aligned} V_{od} - V_{gd} &= I_{od}Z_g \,, \\ V_{oq} - V_{gq} &= I_{oq}Z_g \end{aligned} \tag{5.13}$$

In islanded mode of operation with an ac common load, the load model is defined by:

$$\begin{aligned} V_{od} &= I_{od}Z_l \,, \\ V_{oq} &= I_{oq}Z_l \end{aligned} \tag{5.14}$$

where V_{gd}, V_{gq} are the d-q components of the utility-grid voltage with a grid impedance $Z_g = R_g + sL_g$whereas the ac common load is $Z_l = R_l + sL_l$ (ignoring the

inductive coupling terms in *d-q* reference frame) with R_g, R_l and L_g, L_l as the resistance and inductance of the grid or load impedance, respectively. Figure 5.4 shows the large-signal model of the interfacing VSI where $V_d^{inv}$and V_q^{inv} are the generated *d-q* inverter voltages to the PWM of the VSI from which the inverter *d-q* duty ratios (α_d and α_q) are determined.

The dc-side input admittance of VSI depends on the control topology and the micro-grid configurations. In this Chapter, typical converter control topologies in DG applications are considered; namely they are: grid- connected (or weak grid connection) or islanded mode of operation with/without the dc-link voltage regulation from the VSI side.

5.4.1 Topology 1: Grid-Connected with DC-Link Regulation

In grid-connected mode, the ac-bus voltage is defined by the utility-grid. A current control scheme is utilized in addition to dc-link voltage control that is required with non-dispatchable DG units. Figure 5.5(a) shows a schematic diagram for this control topology. From (5.12), the injection of active power depends on V_{dc}^2 so that the dc voltage controller $\left(G_{vdc}(s)\right)$ processes the difference between V_{dc}^2 and V_{dc}^{*2} to reduce the system nonlinearity and generate the *d*-axis component of the inverter output current (I_d^*). A feed-forward gain of "-1" is multiplied by output of the dc voltage controller to compensate for the negative injection of the dc-power [as in Figure 5.6(b)]. A current controller with a transfer function $G_i(s)$ ensures that the injected current (I_d) tracks I_d^*, and hence, the delivered active power to the grid can be controlled [126]. Note that, the *q*-axis component of the injected current $\left(I_q\right)$ is regulated to zero by a similar current controller $G_i(s)$ in the *q*-channel so that the VSI operates at unity power factor mode. The control loop dynamics are given by:

$$I_d^* = -\left(V_{dc}^{*2} - V_{dc}^2\right)G_{vdc}(s)\ ,$$

$$G_{vdc}(s) = K_p^{vdc} + K_i^{vdc}/s \tag{5.15}$$

$$V_d^{inv} = (I_d^* - I_d)G_i(s) - \omega L_f I_q + V_{od} \tag{5.16}$$

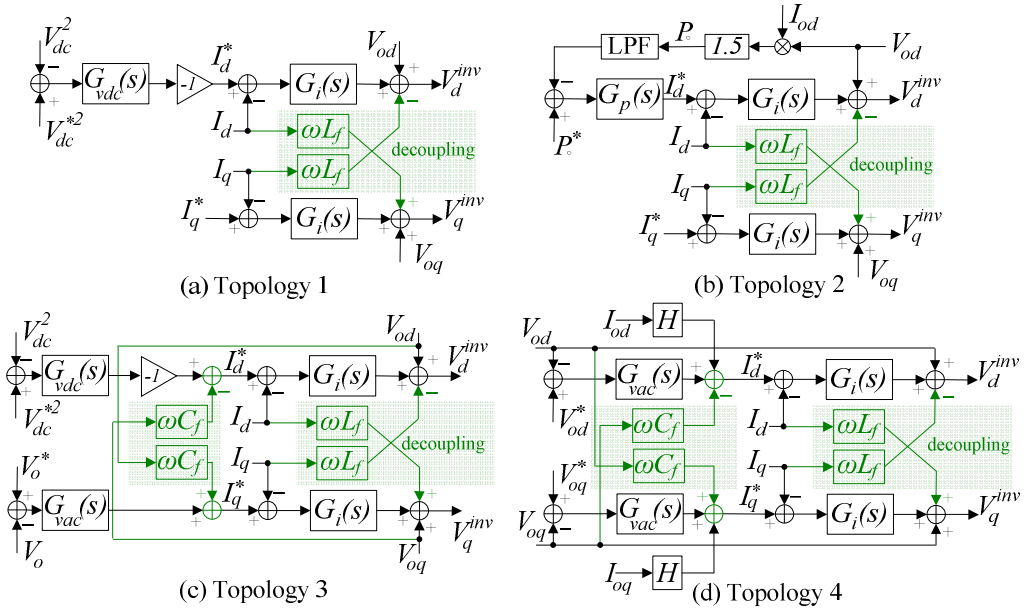

Figure 5.5: Controller schematics under different operating modes of the ac micro-grid. (a) Grid-connected – dc-link regulation. (b) Grid-connected – no dc-link regulation. (c) Weak grid connection – dc-link regulation. (d) Islanded mode (or weak grid) – no dc-link regulation.

$$V_q^{inv} = \left(I_q^* - I_q\right)G_i(s) + \omega L_f I_d + V_{oq}\ ,$$
$$G_i(s) = K_p^i + K_i^i/s \tag{5.17}$$

where $K_p^{vdc}$and K_p^i as proportional gains and $K_i^{vdc}$and K_i^i as integral gains, for $G_{vdc}(s)$ and $G_i(s)$ respectively, and the superscript "*" denotes the reference value. Decoupling terms $\left(\omega L_f I_d, \omega L_f I_q\right)$ are included in (5.16) and (5.17) to compensate the effect of coupled inductor currents in the *d-q* channels.

The dc-side input admittance of the VSI can be obtained by using the average model on the switching converter and small-signal linearization to approximate the nonlinear behavior of the dc/ac power conversion process. Applying small-signal linearization on the power balance equation in (5.11) gives:

$$V_{dc}^{\circ}\Delta I_{dc} + I_{dc}^{\circ}\Delta V_{dc} = 1.5\left(V_d^{\circ}\Delta I_d + I_d^{\circ}\Delta V_d\right) \tag{5.18}$$

where Δ represent small perturbation around the operating point, and the superscript "$^{\circ}$" is the steady state operating value of the parameter.

Note that $V_q^\circ = 0$ by the voltage-orientation while $I_q^\circ = 0$ for unity power factor operation.

Applying small perturbations on (5.7) and (5.13) with $\Delta V_{gd} = \Delta V_{gq} = 0$, and solve together:

$$\Delta I_d = \Delta V_{od}\left(sC_f + 1/Z_g\right) \tag{5.19}$$

Note that the q-channel in (5.13) is assumed to be zero in small-signal sense due to unity power factor mode of operation in which $I_{oq} \approx I_q = 0$.

Similarly, applying small perturbations on (5.5) and solving with (5.19),

$$\Delta V_d = \Delta V_{od}\left(1 + \left(sC_f + 1/Z_g\right)\left(R_f + sL_f\right)\right) \tag{5.20}$$

Using (5.19) and (5.20) in (5.18) to eliminate ΔI_d and ΔV_d :

$$V_{dc}^\circ \Delta I_{dc} + I_{dc}^\circ \Delta V_{dc} = 1.5\left(\left(sC_f + 1/Z_g\right)\left(V_d^\circ + I_d^\circ\left(R_f + sL_f\right)\right) + I_d^\circ\right)\Delta V_{od} \tag{5.21}$$

Applying small-signal linearization on (5.15) and (5.16), and solve together, ΔV_{od} can be given in terms of ΔV_{dc} as in (5.22).

$$\Delta V_{od}\left(sC_f + \frac{1}{Z_g}\right)\left(R_f + sL_f + G_i(s)\right) = \Delta V_{dc}\left(\frac{V_d^\circ}{V_{dc}^\circ} + 2V_{dc}^\circ G_{vdc}(s)G_i(s)\right) \tag{5.22}$$

Solving (5.21) and (5.22) to eliminate ΔV_{od} the small-signal input admittance of the VSI from the dc-side is obtained as follows:

$$\Delta Y_1 = \frac{\Delta I_{dc1}}{\Delta V_{dc}} = \left(\frac{1}{V_{dc}^{\circ 2}}\right)\frac{A_5 s^5 + A_4 s^4 + A_3 s^3 + A_2 s^2 + A_1 s + A_0}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s} \tag{5.23}$$

$$A_5 = L_g L_f C_f\left(1.5 I_d^\circ V_d^\circ - I_{dc}^\circ V_{dc}^\circ + 3 I_d^\circ K_p^i K_p^{vdc} V_{dc}^{\circ 2}\right)$$

$$A_4 = C_f\left(\left(L_g R_f + L_f R_g\right)\left(1.5 I_d^\circ V_d^\circ - I_{dc}^\circ V_{dc}^\circ + 3 I_d^\circ K_p^i K_p^{vdc} V_{dc}^{\circ 2}\right) - I_{dc}^\circ V_{dc}^\circ K_p^i L_g\right)$$

$$+3V_{dc}^{\circ 2}C_f\left(L_fL_gI_d^{\circ}\left(K_p^iK_i^{vdc}+K_i^iK_p^{vdc}\right)+K_p^iK_p^{vdc}L_gV_d^{\circ}+0.5L_g\right)$$

$$A_3=1.5I_d^{\circ}\left(L_f+L_g\right)\left(V_d^{\circ}+2V_{dc}^{\circ 2}K_p^iK_p^{vdc}\right)-I_{dc}^{\circ}V_{dc}^{\circ}L_f$$
$$+3C_fV_{dc}^{\circ 2}\left(K_p^iK_p^{vdc}\left(I_d^{\circ}R_fR_g+V_d^{\circ}R_g\right)+K_i^iK_i^{vdc}I_d^{\circ}L_fL_g\right)$$
$$+3C_fV_{dc}^{\circ 2}\left(K_p^iK_i^{vdc}+K_i^iK_p^{vdc}\right)\left(I_d^{\circ}\left(L_gR_f+L_fR_g\right)+V_d^{\circ}L_g\right)$$
$$+1.5C_fR_gV_d^{\circ}\left(I_d^{\circ}R_f+V_d^{\circ}\right)-C_fI_{dc}^{\circ}V_{dc}^{\circ}\left(K_i^iL_g+K_p^iR_g+R_fR_g\right)$$

$$A_2=1.5I_d^{\circ}\left(R_f+R_g\right)\left(V_d^{\circ}+2V_{dc}^{\circ 2}K_p^iK_p^{vdc}\right)-I_{dc}^{\circ}V_{dc}^{\circ}\left(K_p^i+R_f+K_i^iR_gC_f\right)$$
$$+3V_{dc}^{\circ 2}\left(K_p^iK_i^{vdc}+K_i^iK_p^{vdc}\right)\left(C_fR_g\left(I_d^{\circ}R_f+V_d^{\circ}\right)+I_d^{\circ}\left(L_f+L_g\right)\right)+1.5V_d^{\circ 2}$$
$$+3V_d^{\circ}V_{dc}^{\circ 2}\left(K_p^iK_p^{vdc}+K_i^iK_i^{vdc}L_gC_f\right)+3C_fI_d^{\circ}V_{dc}^{\circ 2}K_i^iK_i^{vdc}\left(L_gR_f+L_fR_g\right)$$

$$A_1=3V_{dc}^{\circ 2}K_i^iK_i^{vdc}\left(I_d^{\circ}\left(L_f+L_g\right)+C_fR_g\left(I_d^{\circ}R_f+V_d^{\circ}\right)\right)-I_{dc}^{\circ}V_{dc}^{\circ}K_i^i$$
$$+3V_{dc}^{\circ 2}\left(K_p^iK_i^{vdc}+K_i^iK_p^{vdc}\right)\left(I_d^{\circ}\left(R_f+R_g\right)+V_d^{\circ}\right)$$

$$A_0=3V_{dc}^{\circ 2}K_i^iK_i^{vdc}\left(I_d^{\circ}\left(R_f+R_g\right)+V_d^{\circ}\right)$$

$$a_5=L_fL_gC_f$$

$$a_4=C_f\left(K_p^iL_g+L_gR_f+L_fR_g\right)$$

$$a_3=L_f+C_f\left(K_i^iL_g+K_p^iR_g+R_fR_g\right)$$

$$a_2=K_p^i+R_f+C_fK_i^iR_g$$

$$a_1=K_i^i$$

In the grid-connected mode, the power is injected to the grid via direct current control. Therefore, the sensitivity transfer function between the injected ac current to the grid (ΔI_{od}) and the dc-link voltage (ΔV_{dc}) is obtained to assess the impact of dc-link dynamics on the injected ac current. Applying small-signal linearization to (5.5), (5.15), a transfer function between ΔI_d and ΔV_{dc} is obtained. Using this transfer function with (5.7) and the grid-side model in (5.13), the $\Delta I_{od}/\Delta V_{dc}$ sensitivity function is given by:

$$\frac{\Delta I_{od}}{\Delta V_{dc}}=\frac{\left(V_d^{\circ}+2K_p^iK_p^{vdc}V_{dc}^{\circ 2}\right)s^2+2V_{dc}^{\circ 2}\left(K_p^iK_i^{vdc}+K_i^iK_p^{vdc}\right)s+2V_{dc}^{\circ 2}K_i^iK_i^{vdc}}{V_{dc}^{\circ}\left(a_5s^5+a_4s^4+a_3s^3+a_2s^2+a_1s\right)} \tag{5.24}$$

The denominator parameters are defined in (5.23).

5.4.2 Topology 2: Grid-Connected without DC-Link Regulation

In this mode, current control scheme is adopted with an active power controller $G_p(s)$ that is used to generate the active current reference I_d^* [127]. The reactive power injection is usually set to zero for unity power factor operation. The controller schematic with the decoupling loops is shown in Figure 5.5(b). For high power quality injection via a slowly varying current reference, a LPF with low cut-off frequency (ω_p) is used to average the measured active power and reject grid-side distortions.

The active power controller dynamics are governed by:

$$I_d^* = \left(P_o^* - P_o \frac{\omega_p}{s+\omega_p}\right) G_p(s),$$
$$G_p(s) = K_p^p + K_i^p/s \tag{5.25}$$

while (5.16) and (5.17) for the inner current controllers are still applied, where P_o is the injected active power to the common bus and is calculated by (5.9), and K_p^p and K_i^p are the proportional and integral gains of the active power controller, respectively.

Following the same procedures used to obtain (5.23), the small-signal dc-side input admittance of the VSI is given by:

$$\Delta Y_2 = \frac{\Delta I_{dc2}}{\Delta V_{dc}} = \left(\frac{1}{V_{dc}^{\circ 2}}\right) \frac{B_6 s^6 + B_5 s^5 + B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s + B_0}{b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{5.26}$$

$$B_6 = L_g L_f C_f \left(1.5 I_d^{\circ} V_d^{\circ} - I_{dc}^{\circ} V_{dc}^{\circ}\right)$$

$$B_5 = 1.5 C_f L_g V_d^{\circ} \left(I_d^{\circ} L_f \omega_p + V_d^{\circ}\right) - I_{dc}^{\circ} V_{dc}^{\circ} C_f L_g \left(K_p^i + L_f \omega_p\right)$$
$$+ C_f \left(L_g R_f + L_f R_g\right)\left(1.5 I_d^{\circ} V_d^{\circ} - I_{dc}^{\circ} V_{dc}^{\circ}\right)$$

$$B_4 = 1.5 I_d^{\circ} V_d^{\circ} \left(L_f + L_g + C_f R_f R_g\right) + 1.5 C_f R_g V_d^{\circ 2} \left(1 + L_g \omega_p / R_g\right)$$
$$- C_f I_{dc}^{\circ} V_{dc}^{\circ} \left(K_p^i \left(R_g + L_g \omega_p\right) + R_f R_g + K_i^i L_g - L_f / C_f\right)$$
$$+ C_f \omega_p \left(L_g R_f + L_f R_g\right)\left(1.5 I_d^{\circ} V_d^{\circ} - I_{dc}^{\circ} V_{dc}^{\circ}\right)$$

$$B_3 = 1.5 I_d^{\circ} V_d^{\circ} \left(R_f + R_g + \omega_p \left(L_f + L_g\right)\right) + 1.5 V_d^{\circ 2} - I_{dc}^{\circ} V_{dc}^{\circ} \left(K_p^i + R_f\right)$$
$$+ 1.5 C_f R_g \omega_p V_d^{\circ} - I_{dc}^{\circ} V_{dc}^{\circ} \omega_p \left(L_f + 1.5 I_{od}^{\circ} K_p^i K_p^p L_g\right)$$
$$- C_f I_{dc}^{\circ} V_{dc}^{\circ} \omega_p \left(R_g \left(K_p^i + R_f\right) + K_i^i \left(L_g + R_g/\omega_p\right)\right)$$

$$B_2 = -I_{dc}^{\circ}V_{dc}^{\circ}\omega_p\begin{pmatrix}R_f + K_p^i\left(1 + 1.5K_p^pV_{od}^{\circ}\right) + K_i^i\left(1/\omega_p + C_fR_g\right)\\ +1.5I_{od}^{\circ}L_g\left(K_i^iK_p^i + K_p^i\left(K_i^p + K_p^pR_g/L_g\right)\right)\end{pmatrix}$$
$$+1.5I_d^{\circ}V_d^{\circ}\omega_p\left(R_g + R_f\right) + 1.5V_d^{\circ 2}\omega_p$$
$$B_1 = -I_{dc}^{\circ}V_{dc}^{\circ}\omega_p\left(K_i^i\left(1 + 1.5I_{od}^{\circ}K_i^pL_g\right) + 1.5\left(K_p^iK_i^p + K_i^iK_p^p\right)\left(I_{od}^{\circ}R_g + V_{od}^{\circ}\right)\right)$$
$$B_0 = -1.5I_{dc}^{\circ}V_{dc}^{\circ}K_i^iK_i^p\omega_p\left(I_{od}^{\circ}R_g + V_{od}^{\circ}\right)$$
$$b_6 = L_fL_gC_f$$
$$b_5 = C_f\left(L_g\left(K_p^i + R_f\right) + L_f\left(R_g + L_g\omega_p\right)\right)$$
$$b_4 = L_f + C_f\left(K_i^iL_g + R_g\left(K_p^i + R_f\right) + \omega_p\left(L_gR_f + L_fR_g + K_p^iL_g\right)\right)$$
$$b_3 = \left(K_p^i + R_f\right)\left(1 + C_f\omega_pR_g\right) + C_fK_i^iR_g + \omega_p\left(L_f + L_g\left(1.5I_{od}^{\circ}K_p^iK_p^p + C_fK_i^i\right)\right)$$
$$b_2 = K_i^i + K_p^i\omega_p + 1.5I_{od}^{\circ}L_g\omega_p\left(K_p^iK_i^p + K_i^iK_p^p\right) + \omega_p\left(R_f + C_fK_i^iR_g\right)$$
$$+1.5K_p^iK_p^p\omega_p\left(I_{od}^{\circ}R_g + V_{od}^{\circ}\right)$$
$$b_1 = K_i^i\omega_p\left(1 + 1.5I_{od}^{\circ}K_i^pL_g\right) + 1.5\omega_p\left(K_p^iK_i^p + K_i^iK_p^p\right)\left(I_{od}^{\circ}R_g + V_{od}^{\circ}\right)$$
$$b_0 = 1.5K_i^iK_i^p\omega_p\left(I_{od}^{\circ}R_g + V_{od}^{\circ}\right)$$

The sensitivity function $\Delta I_{od}/\Delta V_{dc}$ is obtained in (5.27).

$$\frac{\Delta I_{od}}{\Delta V_{dc}} = \frac{V_d^{\circ}\left(L_gs^2 + \left(R_g + L_g\omega_p\right)s + R_g\omega_p\right)s^2}{V_{dc}^{\circ}\left(\beta_7s^7 + \beta_6s^6 + \beta_5s^5 + \beta_4s^4 + \beta_3s^3 + \beta_2s^2 + \beta_1s + \beta_0\right)} \tag{5.27}$$

$$\beta_7 = C_fL_fL_g^2$$
$$\beta_6 = C_fL_g\left(L_g\left(K_p^i + R_f\right) + L_f\left(2R_g + L_g\omega_p\right)\right)$$
$$\beta_5 = L_fL_g + C_f\left(L_g^2\left(K_i^i + \omega_p\left(K_p^i + R_f\right)\right) + L_fR_g^2 + 2L_gR_g\left(K_p^i + R_f + L_fL_g\omega_p\right)\right)$$
$$\beta_4 = \left(K_p^i + R_f\right)\left(L_g + C_fR_g\left(2L_g\omega_p + R_g\right)\right) + L_fR_g\left(1 + C_fR_g\omega_p\right)$$
$$+C_fK_i^iL_g\left(2R_g + L_g\omega_p\right) + L_fL_g\omega_p + 1.5I_{od}^{\circ}K_p^iK_p^pL_g^2\omega_p$$
$$\beta_3 = K_i^iL_g\left(1 + 2C_fR_g\omega_p\right) + R_g\left(K_p^i + R_f\right)\left(1 + C_fR_g\omega_p\right)$$
$$+1.5I_{od}^{\circ}L_g^2\omega_p\left(K_p^iK_i^p + K_i^iK_p^p\right) + \omega_p\left(L_gR_f + L_fR_g\right)$$
$$+1.5K_p^iK_p^pL_g\omega_p\left(2I_{od}^{\circ}R_g + V_{od}^{\circ}\right) + C_fK_i^iR_g^2 + K_p^iL_g\omega_p$$
$$\beta_2 = K_i^iR_g + K_i^i\omega_p\left(1.5I_{od}^{\circ}K_i^pL_g^2 + C_fR_g^2 + L_g\right) + 1.5K_i^iK_p^p\omega_pR_g\left(I_{od}^{\circ}R_g + V_{od}^{\circ}\right)$$

$$+R_g\omega_p\left(K_p^i+R_f\right)+1.5L_g\omega_p\left(2I_{od}^{\circ}R_g+V_{od}^{\circ}\right)\left(K_p^iK_i^p+K_i^iK_p^p\right)$$

$$\beta_1=\omega_p\begin{pmatrix}K_i^iR_g+1.5L_gK_i^iK_i^p\left(2I_{od}^{\circ}R_g+V_{od}^{\circ}\right)\\+1.5R_g\left(K_p^iK_i^p+K_i^iK_p^p\right)\left(I_{od}^{\circ}R_g+V_{od}^{\circ}\right)\end{pmatrix}$$

$$\beta_0=1.5K_i^iK_i^p\omega_pR_g\left(I_{od}^{\circ}R_g+V_{od}^{\circ}\right)$$

5.4.3 Topology 3: Weak Grid Connection with DC-Link Regulation

In this mode with non-dispatchable resources (e.g. wind and PV sources), both ac and dc voltage control loops are used in the DG interface. The ac-bus voltage should be regulated by a voltage controller $G_{vac}(s)$. Simultaneously, dc-link voltage modulator $\left(G_{vdc}(s)\right)$ is utilized to maintain the referenced dc-link voltage [128]. This topology is valid with weak grids where the ac-bus voltage requires regulation by the DG interface. The dc-voltage control loop generates I_d^*, which is proportional to the injected active power, whereas the ac voltage control loop generates I_q^* which is responsible for injecting reactive power [125]. It is clear that the VSI interface can't be operated under unity power factor conditions as the reactive power is yielded to meet the voltage control requirements. Figure 5.5(c) shows the block diagram of this control topology.

The dc voltage controller is similar to that in topology 1 as follows:

$$I_d^*=-\left(V_{dc}^{*2}-V_{dc}^2\right)G_{vdc}(s)-\omega C_fV_{oq} \tag{5.28}$$

whereas the ac voltage controller treats the rms value of the ac-bus voltage by the following dynamics.

$$I_q^*=(V_o^*-V_o)G_{vac}(s)+\omega C_fV_{od}\ ,$$
$$G_{vac}(s)=K_p^{vac}+K_i^{vac}/s \tag{5.29}$$

where $V_o=\left(V_{od}^2+V_{oq}^2\right)^{1/2}$. The current controller dynamics in (5.16) and (5.17) still apply.

Small-signal linearization is applied on the power balance equation in (5.11) considering reactive power injection $(\Delta I_q \neq 0)$. It can be assumed that the q-axis component of the output voltage is neglected as compared to the d-axis component that is dictated by the grid voltage [129], so (5.18) still applies.

Applying small-signal linearization on (5.16), (5.28) and (5.5) and solve together:

$$\left(2V_{dc}G_{vdc}(s)G_i(s) + \frac{V_d^\circ}{V_{dc}^\circ}\right)\Delta V_{dc} = \left(R_f + sL_f + G_i(s)\right)\Delta I_d \tag{5.30}$$

Applying small perturbations on (5.6), ΔI_q and ΔI_d can be related to each other by:

$$\frac{\Delta I_q}{\Delta I_d} = -\frac{\omega L_f}{R_f + sL_f} \tag{5.31}$$

Using (5.31), linearizing (5.17) and (5.28), and solve all together:

$$\left(\omega C_f - \frac{V_{od}^\circ}{V_o^\circ}G_{vac}(s)\right)G_i(s)\Delta V_{od} = \left(R_f + sL_f + G_i(s)\right)\Delta I_q \tag{5.32}$$

Using (5.31) in (5.5) to eliminate I_d:

$$\Delta V_d - \Delta V_{od} = -\left(\frac{(R_f + sL_f)^2}{\omega L_f} + \omega L_f\right)\Delta I_q \tag{5.33}$$

By solving (5.7) and (5.13) after applying small perturbations so that the grid voltages (V_{gd}, V_{gq}) are zero in small-signal sense, ΔI_d and ΔV_{od} can be related together:

$$\Delta I_d = \left(\frac{1}{Z_g} + sC_f\right)\Delta V_{od} \tag{5.34}$$

Solving (5.33), (5.32) and (5.34), ΔV_d can be obtained in terms of ΔI_d:

$$\left(-\left(\frac{\left(R_f+sL_f\right)^2}{\omega L_f}+\omega L_f\right)\left(\omega C_f-\frac{V_{od}^{\circ}}{V_o^{\circ}}G_{vac}(s)\right)G_i(s)+1\right)\frac{\Delta I_d}{\left(\frac{1}{Z_g}+sC_f\right)}=\Delta V_d \qquad (5.35)$$

Using (5.35) in (5.18) to eliminate ΔV_d and then using (5.30) to substitute ΔI_d by ΔV_{dc}, and arranging, the small signal dc-side input admittance of the VSI is obtained as:

$$\Delta Y_3=\frac{\Delta I_{dc3}}{\Delta V_{dc}}=$$

$$\frac{V_o^{\circ}L_f\begin{pmatrix}1.5V_d^{\circ 2}\\-I_{dc}^{\circ}V_{dc}^{\circ}\left(G_i(s)+Z_f\right)\\+3G_i(s)G_{vac}(s)V_d^{\circ}V_{dc}^{\circ 2}\end{pmatrix}\left(1+sC_fZ_g\right)+1.5I_d^{\circ}Z_g\begin{pmatrix}\omega V_o^{\circ}L_f\\+G_i(s)\left(G_{vac}(s)V_{od}^{\circ}-\omega V_o^{\circ}c_f\right)\\\times\left(\omega^2L_f^2+Z_f^2\right)\end{pmatrix}\left(V_d^{\circ}+2G_i(s)G_{vdc}(s)V_{dc}^{\circ 2}\right)}{\left(1+sC_fZ_g\right)\left(G_i(s)+Z_f\right)\omega L_fV_{dc}^{\circ 2}V_o^{\circ}} \qquad (5.36)$$

where $Z_f=R_f+sL_f$

In weak grid connection, the output ac voltage is the driving output parameter of the VSI, so the sensitivity function between ΔV_{od} and $\Delta V_{dc}$is obtained in (5.37) by solving (5.30) and (5.34) to eliminate ΔI_d.

$$\frac{\Delta V_{od}}{\Delta V_{dc}}=\frac{2V_{dc}G_{vdc}(s)G_i(s)+\frac{V_d^{\circ}}{V_{dc}^{\circ}}}{\left(R_f+sL_f+G_i(s)\right)\left(\frac{1}{Z_g}+sC_f\right)} \qquad (5.37)$$

5.4.4 Topology 4: Islanded Mode without DC-Link Regulation

In dispatchable DG units, there is no dc-link voltage control from the VSI side; only ac voltage controllers $\left(G_{vac}(s)\right)$ are employed in both *d-q* channels. They are used to synthesis the output ac-bus voltage and generate I_d^* and I_q^* as inputs references for the current controllers $\left(G_i(s)\right)$. The current controller regulates the ac filter inductor currents to follow the reference commands generated by the outer voltage controller. Figure 5.5(d) shows the control scheme under that operating mode [105].

The modified ac voltage controllers are dynamically modeled as follows:

$$I_d^* = (V_{od}^* - V_{od})G_{vac}(s) - \omega C_f V_{oq} + HI_{od} \tag{5.38}$$

$$I_q^* = \left(V_{oq}^* - V_{oq}\right)G_{vac}(s) + \omega C_f V_{od} + HI_{oq} \tag{5.39}$$

where H is a feed-forward gain. The current control loops are similar to previous cases as in (5.16) and (5.17).

Following similar steps as in aforementioned analysis, the small-signal input admittance is given by:

$$\Delta Y_4 = \frac{\Delta I_{dc4}}{\Delta V_{dc}} = \left(\frac{1}{V_{dc}^{\circ 2}}\right)\frac{D_5 s^5 + D_4 s^4 + D_3 s^3 + D_2 s^2 + D_1 s + D_0}{d_5 s^5 + d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0} \tag{5.40}$$

$$D_5 = L_f L_g C_f\left(1.5 I_d^{\circ} V_d^{\circ} - I_{dc}^{\circ} V_{dc}^{\circ}\right)$$

$$D_4 = C_f\left(1.5\left(I_d^{\circ} V_d^{\circ}\left(L_l R_f + L_f R_l\right) + L_l V_d^{\circ 2}\right) - I_{dc}^{\circ} V_{dc}^{\circ}\left(L_l\left(K_p^i + R_f\right) + L_f R_l\right)\right)$$

$$D_3 = 1.5 V_d^{\circ}\left(I_d^{\circ}\left(L_l + L_f\right) + C_f R_l\left(I_d^{\circ} R_f + V_d^{\circ}\right)\right) - I_{dc}^{\circ} V_{dc}^{\circ}\left(L_l\left(C_f K_i^i + K_p^i K_p^{vac}\right) - L_f\right)$$
$$-C_f I_{dc}^{\circ} V_{dc}^{\circ} R_l\left(K_p^i + R_f\right)$$

$$D_2 = 1.5 I_d^{\circ} V_d^{\circ}\left(R_f + R_l\right) + 1.5 V_d^{\circ 2} - I_{dc}^{\circ} V_{dc}^{\circ} L_l\left(K_p^i K_i^{vac} + K_i^i K_p^{vac}\right)$$
$$-I_{dc}^{\circ} V_{dc}^{\circ}\left(K_p^i K_p^{vac} R_l + R_f + C_f K_i^i R_l + K_p^i(1 + H)\right)$$

$$D_1 = I_{dc}^{\circ} V_{dc}^{\circ}\left(K_i^i(H - 1) - K_i^i K_i^{vac} L_l - R_l\left(K_p^i K_i^{vac} + K_i^i K_p^{vac}\right)\right)$$

$$D_0 = -1.5 I_{dc}^{\circ} V_{dc}^{\circ} K_i^i K_i^{vac} R_l$$

$$d_5 = L_g L_f C_f$$

$$d_4 = C_f\left(L_l\left(K_p^i + R_f\right) + L_f R_l\right)$$

$$d_3 = L_f + L_l\left(C_f K_i^i + K_p^i K_p^{vac}\right) + C_f R_l\left(K_p^i + R_f\right)$$

$$d_2 = K_p^i(1 - H) + L_l\left(K_p^i K_i^{vac} + K_i^i K_p^{vac}\right) + R_f + R_l\left(C_f K_i^i + K_p^i K_p^{vac}\right)$$

$$d_1 = K_i^i(1 - H) + K_i^i K_i^{vac} L_l + R_l\left(K_p^i K_i^{vac} + K_i^i K_p^{vac}\right)$$

$$d_0 = K_i^i K_i^{vac} R_l$$

The sensitivity function $\Delta V_{od}/\Delta V_{dc}$ is obtained as:

$$\frac{\Delta V_{od}}{\Delta V_{dc}} = \frac{V_d^{\circ}(R_l + sL_l)s^2}{V_{dc}^{\circ}(\eta_5 s^5 + \eta_4 s^4 + \eta_3 s^3 + \eta_2 s^2 + \eta_1 s + \eta_0)} \tag{5.41}$$

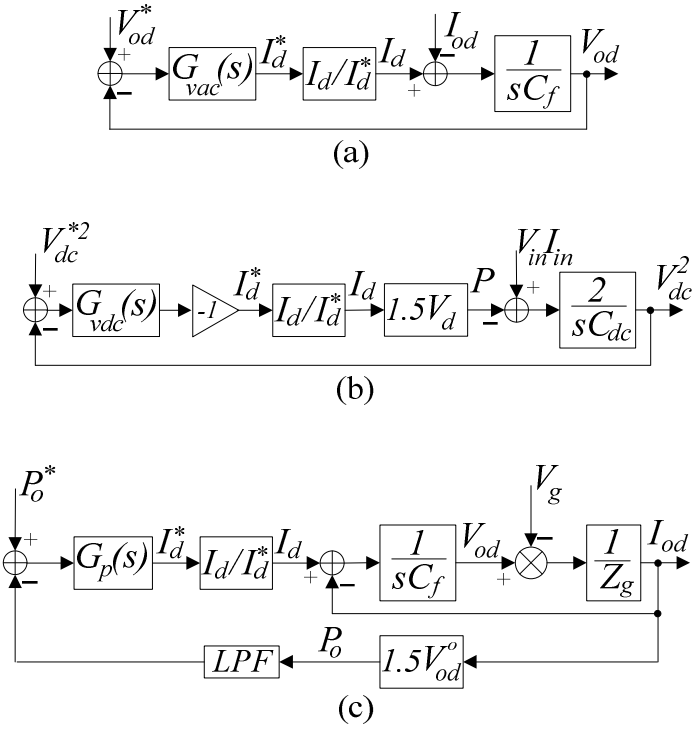

Figure 5.6: Voltage controller dynamics for the interfacing VSI. (a) Ac voltage controller. (b) Dc voltage controller. (c) Active power controller.

$$\eta_5 = L_l L_f C_f$$

$$\eta_4 = C_f\left(L_l\left(K_p^i + R_f\right) + L_f R_l\right)$$

$$\eta_3 = L_f + L_l\left(C_f K_i^i + K_p^i K_p^{vac}\right) + C_f R_l\left(K_p^i + R_f\right)$$

$$\eta_2 = K_p^i(1-H) + L_l\left(K_p^i K_i^{vac} + K_i^i K_p^{vac}\right) + R_f + R_l\left(C_f K_i^i + K_p^i K_p^{vac}\right)$$

$$\eta_1 = K_i^i(1-H) + K_i^i K_i^{vac} L_l + R_l\left(K_p^i K_i^{vac} + K_i^i K_p^{vac}\right)$$

$$\eta_0 = K_i^i K_i^v R_l$$

5.5 Controllers Parameters for VSI: General Design Approach

This section provides a general design approach for the different controllers adopted with VSI in this Chapter; $G_i(s)$, $G_{vac}(s)$, $G_{vdc}(s)$ and $G_p(s)$. The transfer function that describes each controller dynamics is obtained. Some systematic tools for designing the PI parameters can be used like symmetrical optimum method [130]. Alternatively, frequency response analysis of the closed loop dynamics provided hereafter can be

used to design the controller parameters with accepted performance. The designed system parameters with the controller gains are depicted in Appendix 5.1.

5.5.1 AC Current Controller

The closed loop current controller $\left(G_i(s)\right)$ dynamics can be evaluated by solving (5.5) and (5.16) to get:

$$\frac{I_d}{I_d^*} = \frac{K_p^i s + K_i^i}{L_f s^2 + \left(R_f + K_p^i\right)s + K_i^i} \tag{5.42}$$

The zero and one of the poles in (5.42) are designed to cancel each other by setting $K_p^i/K_i^i = L_f/R_f$ which results in:

$$\frac{I_d}{I_d^*} = \frac{K_p^i/L_f}{s + K_p^i/L_f} \tag{5.43}$$

From (5.43), the time constant (T_i) of the current controller loop is L_f/K_p^i whereas the controller bandwidth is $1/T_i$. The bandwidth of the current controller is usually 0.1~0.2× switching frequency ($2\pi F_{sw}$) of the VSI. The controller parameters are then selected by [126]:

$$K_p^i = L_f/T_i,\ K_i^i = R_f/T_i \tag{5.44}$$

5.5.2 AC Voltage Controller

The dynamics of the ac voltage controller $\left(G_{vac}(s)\right)$ in the islanded mode of operation can be obtained by using (5.38) with (5.42) to obtain I_d which is utilized with (5.7) and load model in (5.14) to close the control loop as shown in Figure 5.6(a). The ac voltage control dynamics depend on the ac filter parameters and the current controller bandwidth.

$$\frac{V_{od}}{V_{od}^{*}} = \frac{K_p^{vac}s + K_i^{vac}}{\left(L_f C_f / K_p^i\right)s^3 + C_f s^2 + K_p^{vac}s + K_i^{vac}} \tag{5.45}$$

For successful cascaded operation and time-scale separation between the outer loop voltage controller and the inner current controller, the bandwidth of the ac voltage controller is usually designed to be sufficiently slower than the current controller bandwidth with at least one decade [109]. This role is also applied for the remaining outer loop controllers with respect to the inner current controller.

5.5.3 DC Voltage Controller

Similar to the ac voltage controller and using (5.12), the dc voltage controller dynamics can be evaluated from the block diagram representation shown in Figure 5.6(b) and given as by:

$$\frac{V_{dc}^2}{V_{dc}^{*2}} = \frac{3V_d K_p^i\left(K_p^{vdc}s + K_i^{vdc}\right)}{\left(L_f C_{dc} / K_p^i\right)s^3 + C_{dc}s^2 + 3V_d K_p^{vac}s + 3V_d K_i^{vac}} \tag{5.46}$$

5.5.4 Active Power Controller

With topology 2, an active power controller is utilized as shown in Figure 5.6(c). As the ac-bus voltage is relatively constant in the grid-connected mode, it is used as a feed-forward gain and multiplied by the resultant output current to get the injected active power. Using block diagram reductions, the power controller dynamics are given by:

$$\frac{P_o}{P_o^{*}} = \frac{1.5V_{od}^{\circ}K_p^i\omega_p\left(sK_p^p + K_i^p\right)}{\rho_5 s^5 + \rho_4 s^4 + \rho_3 s^3 + \rho_2 s^2 + \rho_1 s + \rho_0} \tag{5.47}$$

$\rho_5 = L_g L_f C_f$

$\rho_4 = C_f\left(L_g\left(K_p^i + \omega_p L_f\right) + L_f R_g\right)$

$\rho_3 = L_f + \omega_p C_f\left(K_p^i L_g + R_g L_f\right) + C_f K_p^i R_g$

$\rho_2 = K_p^i + \omega_p\left(L_f + C_f K_p^i R_g\right)$

$\rho_1 = \omega_p K_p^i\left(1 + 1.5V_{od}^{\circ}K_p^p\right)$

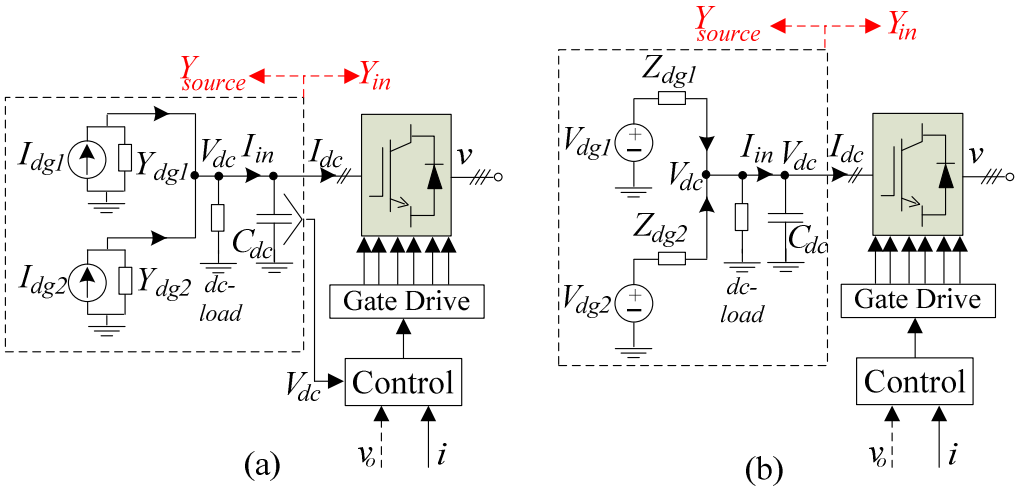

Figure 5.7: Small-signal model verification for dc-side input admittance of VSI when operating at: (a) Topology 1 and 3. (b) Topology 2 and 4.

$\rho_0 = 1.5V_{od}^{\circ}\omega_p K_p^i K_i^p$

5.6 Small-Signal Model Verification of DC-Side Input Admittances of VSI

Small-signal model verification is provided in this section to evaluate the small signal input admittance models of VSI as presented in this Chapter. For the verification purpose, detailed time-domain large-signal models for the VSI with the four configurations are implemented under the Matlab/Simulink environment.

According to Figure 5.7(a), the injected dc current from the DG sources (ΔI_{in}) is related to ΔI_{dc}, by:

$$\frac{\Delta I_{in}}{\Delta V_{dc}} = \frac{\Delta I_{dc}}{\Delta V_{dc}} + sC_{dc} \tag{5.48}$$

For topology 1 and 3, using (5.48) with (5.23) and (5.36), $\Delta V_{dc}/\Delta I_{in}$ can be obtained for each of them as follows;

$$\frac{\Delta V_{dc}}{\Delta I_{in}} = \frac{1}{\Delta Y_1 + sC_{dc}} \tag{5.49}$$

where (5.49) is for topology 1 and is typical for topology 3 but with ΔY_3 instead of ΔY_1.

The unit step response of the obtained $\Delta V_{dc}/\Delta I_{in}$ for each topology (1 or 3) should be equivalent to applying a small step disturbance in the injected dc current $\left(I_{dg1,2}\right)$ in the Simulink model as in Figure 5.7(a).

For topology 2 and 4, applying unit step and observe the response of ΔY_2 and ΔY_4 in (5.26) and (5.40) should be equivalent to applying small disturbance in the input dc voltage $\left(\Delta V_{dg1,2}\right)$ and observing I_{dc} in the Simulink model as in Figure 5.7(b). Note that $Z_{dg1,2}$, $Y_{dg1,2}$ and the dc load are not considered in the model verification. The small-signal verification results based on the aforementioned strategy are shown in Figure 5.8.

With a similar way, the sensitivity functions that are obtained in (5.24), (5.27), (5.37) and (5.41) can be verified. A step response to the analytical $\Delta I_{od}/\Delta V_{dc}$with topology *2* and $\Delta V_{od}/\Delta V_{dc}$ with topology 4 should be similar to applying a step disturbance in the input dc voltage and observing the resultant I_{od} and V_{od} in the Simulink model as in Figure 5.7(b). Both analytical and Simulink model responses are shown in Figure 5.9. From Figure 5.8 and 5.9, the step response for the analytical small-signal impedances/admittances and sensitivity functions is very close and equivalent to the small disturbances in the large-signal Simulink model. This clearly verifies the validity of the followed mathematical approach.

5.7 Analysis of DC-Side Input Admittance of VSI

This section presents a comprehensive analysis of the obtained small-signal input admittances in (5.23), (5.26), (5.36) and (5.40) and the corresponding sensitivity functions (5.24), (5.27), (5.37) and (5.41).

5.7.1 Properties of the DC-side Input Admittance

Figure 5.10 shows the frequency response of the input admittances given in (5.23), (5.26), (5.36) and (5.40). In Figure 5.10(a), the input admittance of topology 1 has almost zero phase angle with positive real part in most of frequency range. As shown, the resonance frequency (f_{res}) of the *LCL* filter composed of the *LC* filter and the grid inductance is reflected to the admittance response where it can be given by:

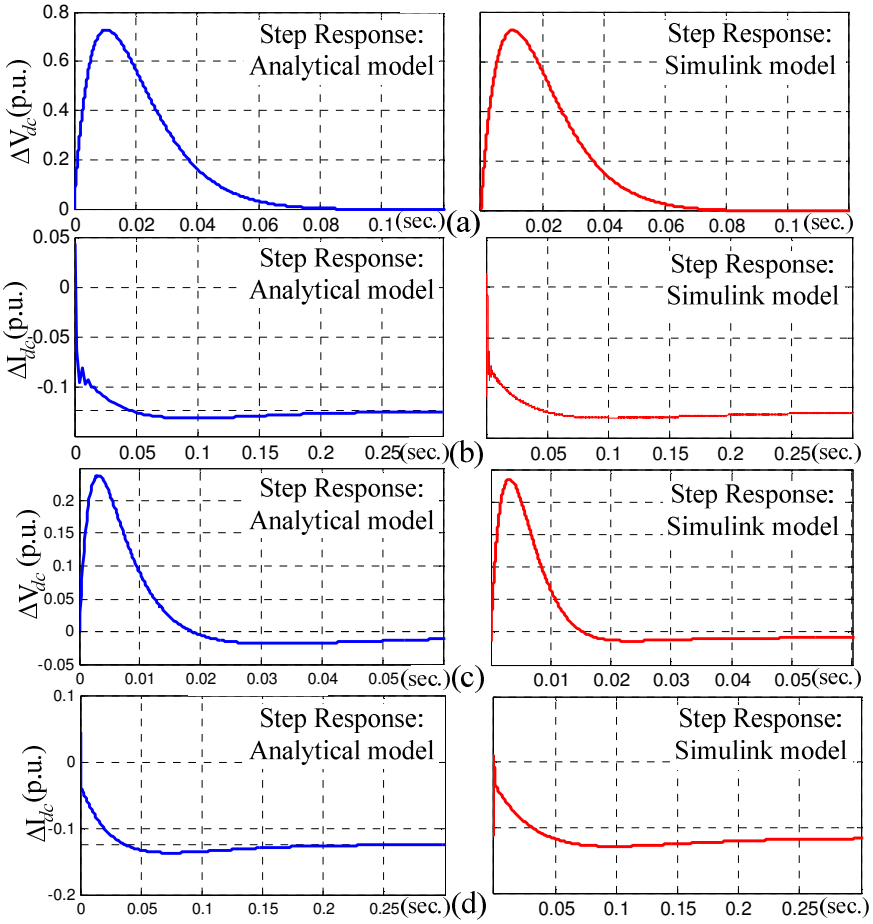

Figure 5.8: Small-signal input admittance verification. (a) Topology 1: dc current step response. (b) Topology 2: dc voltage step response. (c) Topology 3: dc current step response. (d) Topology 4: dc voltage step response.

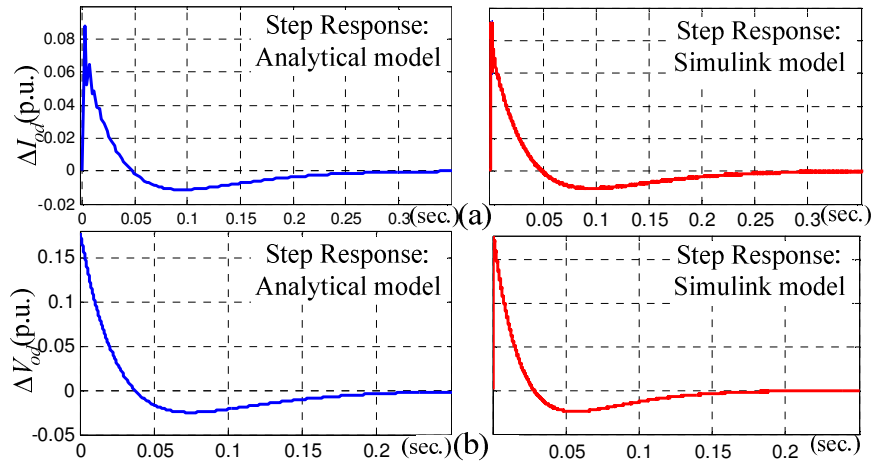

Figure 5.9: Sensitivity function verification. (a) Topology 2: dc voltage step response. (b) Topology 4: dc voltage step response.

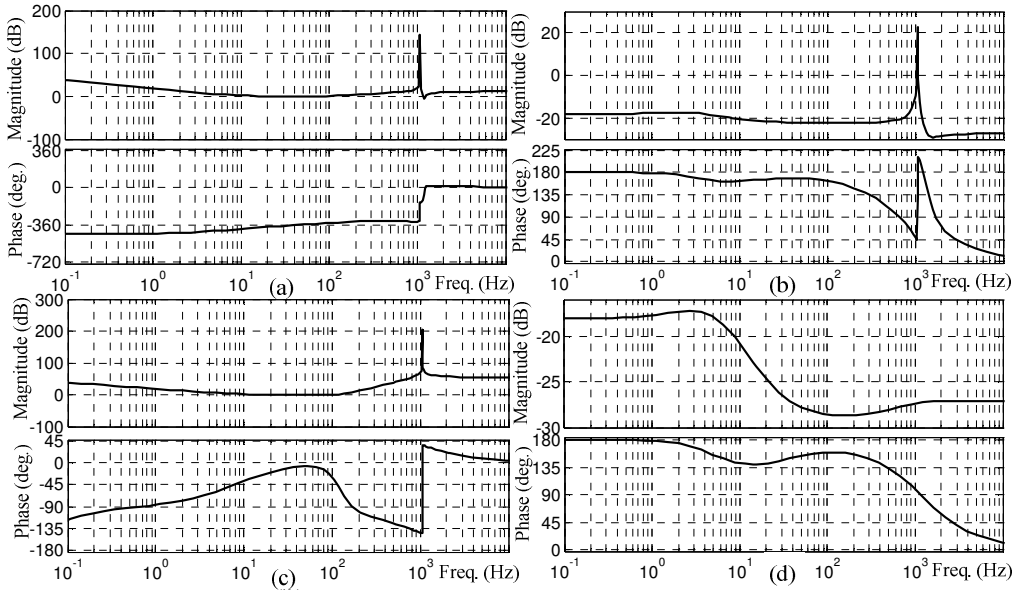

Figure 5.10: Input dc-side admittance of VSI. (a) Topology 1. (b) Topology 2. (c) Topology 3. (d) Topology 4.

$$2\pi f_{res} = \sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \tag{5.50}$$

As in Figure 5.10(a), the resonant frequency peak increases the sensitivity of the input I_{dc} with respect to V_{dc} which degrades the system stability. Resonance damping, in both ac- and dc-sides, can be mitigated by an active damping method in which the capacitor current is re-scaled by a constant gain (K_d) to mimic a virtual voltage drop that is added to V_d^{inv}. Alternatively, passive damping can be implemented by considering a series resistance (R_d) with C_f [131], [132]. However, the effect of resonant damping has no significant influence on the input admittance except in the resonant region. Figure 5.11 shows input admittance with the two damping methods by following the same procedures to obtain (5.23).

For further investigation, the real part of the input admittance is obtained after replacing "*s*" with "*jω*". For topology 1, Figure 5.12(a) shows $Real\{\Delta Y_1\}$ with/without active resonant damping. As shown, with $K_d = 0$, the input admittance is positive except around f_{res} where it appears as a high negative resistance which implies the destabilizing effect of the LCL resonant peaks on the dc-link stability. With the

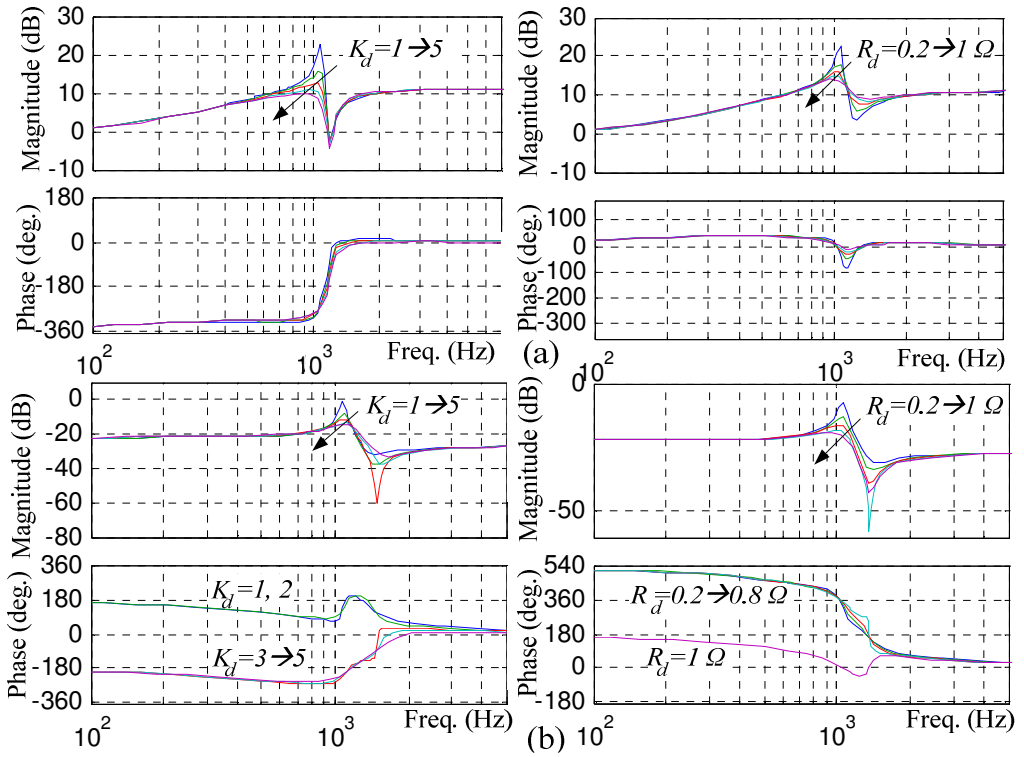

Figure 5.11: Influence of the resonance damping in LCL configuration in grid-connected mode. (a) Topology 1. (b) Topology 2. K_d: Active resonant damping gain, R_d: passive resonant damping resistor.

increase of K_d, the resonant peak decreases with almost a constant real part in low and high frequencies.

Using (5.26), the input admittance for topology 2 is shown in Figure 5.10(b). Similar to topology 1, a resonant peak for the LCL configuration appears around f_{res} which can be compensated as in Figure 5.11(b) by active or passive dampers. In Figure 5.10(b), the VSI appears to the dc-link capacitor as an incremental negative input admittance at the low frequency range. This is also clear from Figure 5.12(b) where $Real\{\Delta Y_2\}$ is negative up to 500 Hz with $K_d = 0$. Unlike topology 1, there is a considerable effect of the resonant damping. In spite of the mitigated resonant peak with $K_d > 0$, $Real\{\Delta Y_2\}$ is shifted more to be negative with higher K_d. As shown, with $K_d = 10$, $Real\{\Delta Y_2\}$ is negative up to 1700 Hz. Actually, most of recent DG sources operate at the maximum power point (MPP), thus the power delivered to the dc-link is probably constant [133]. This can subject the dc-link to instabilities or poorly-damped oscillations due to dc network disturbances. Accordingly, an increase in the dc-link voltage tends to reduce the injected dc current to maintain the delivered constant

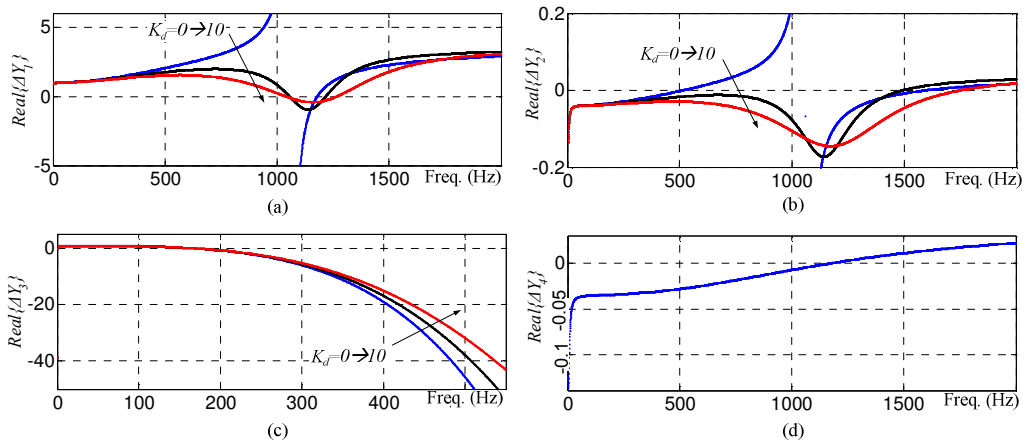

Figure 5.12: Real part of the Input dc-side admittance of VSI. (a) Topology 1. (b) Topology 2. (c) Topology 3. (d) Topology 4. K_d: Active resonant damping gain for topology 1, 2 and 3.

power; on the contrary, the negative slope of the small-signal input admittance causes further increase in the dc-link voltage, and hence the inherent load damping is negative.

Figure 5.10(c) shows the incremental input admittance of the VSI under topology 3 configuration. Due to the grid connection, resonant peak appears at f_{res}. $Real\{\Delta Y_3\}$ is shown in Figure 5.12(c) (up to 550 Hz for clear presentation), in which it appears as positive resistance up to 150 Hz. The negative part at mid-frequency region is due to the resonant peak. As shown, the same active damping technique is employed which compensates the negative values with the gain increase.

For topology 4, the incremental input admittance is plotted as in Figure 5.10(d). Only *LC* ac filter with terminated resistive load is considered in the islanded mode of operation, as result, the resonant frequency peak is naturally damped due to the local resistive load. However, there exists an incremental negative value of the input admittance in low- and mid-frequency range. In this topology, the input admittance is highly damped as compared to topology 2 with high actively resonant damping by $K_d = 10$. $Real\{\Delta Y_4\}$ is shown in Figure 5.12(d); the negative resistance appears up to 1200 Hz as compared to 1700 Hz in Figure 5.12(b) ($K_d = 10$). In Figure 5.12(b), a lower range of negative resistance of $Real\{\Delta Y_2\}$ with the uncompensated resonant damping ($K_d = 0$) appears as compared to $Real\{\Delta Y_4\}$ in Figure 5.12(d). However, the considerable high "$-\ Real\{\Delta Y_2\}$" around f_{res} significantly reduce the system stability margin.

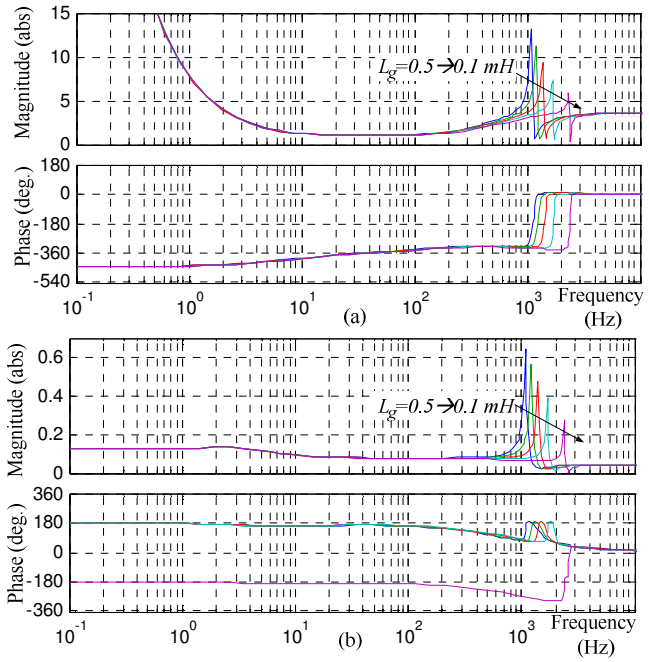

Figure 5.13: Influence of the grid inductance (L_g) on the dc-side input admittance of the VSI. (a) Topology 1. (b) Topology 2.

It can be noted that the trend of low frequency negative input admittance mainly appears with topology 2 and 4 in which no dc-link regulation is considered. The existence of the dc-link control loop adds more robustness to the dc-link dynamics against dc-side disturbances which, as result, is reflected as positive incremental input admittance as in topology 1 and 3.

This section shows that:

- In the grid-connected mode, the *LCL* filter resonant peak is reflected to the incremental input admittance. With topology 1, the damping methods affect only the magnitude around f_{res}, whereas the negative range of the input admittance increases by employing resonant damping for topology 2.
- At low frequency region, the incremental input admittance of VSI with dc-link voltage regulation (topology 1 and 3), has better characteristics as compared to the case without dc-link voltage control (topology 2 and 4) due to the damping effect of the feedback control.

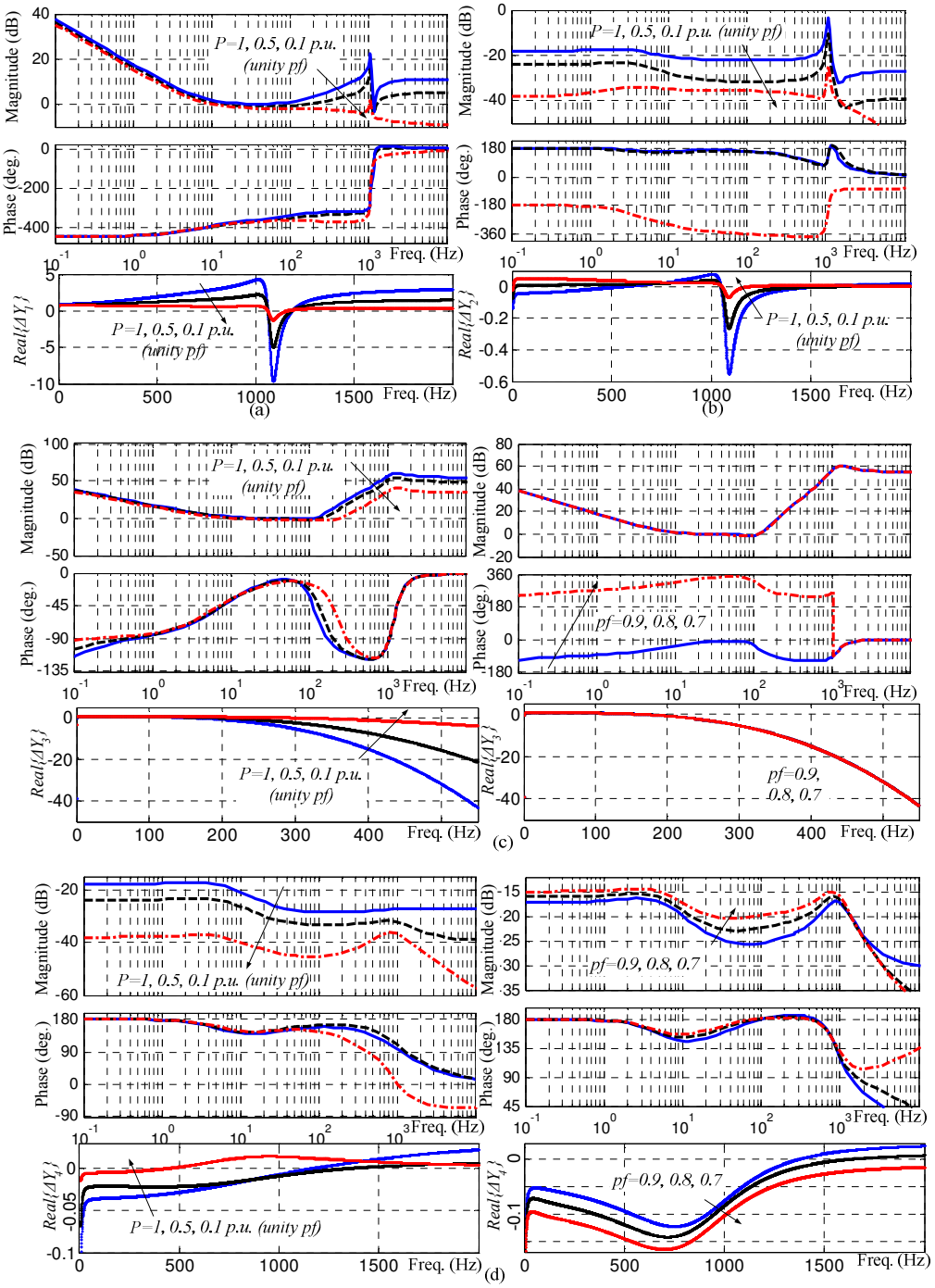

Figure 5.14: Influence of the injected active and reactive power on the input dc-side admittance of the VSI. (a) Topology 1. (b) Topology 2. (c) Topology 3. (d) Topology 4. For topology 1, 2 and 3; $K_d = 10$.

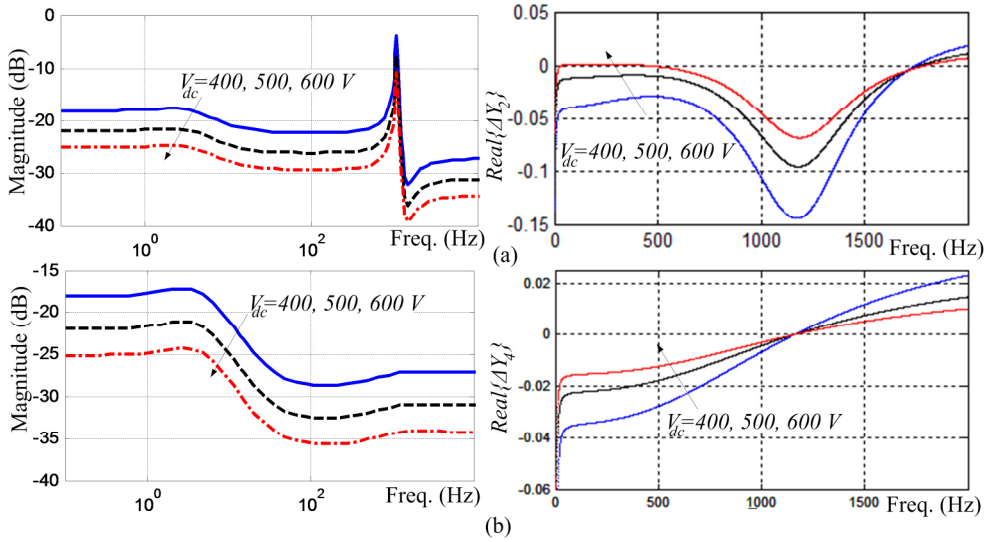

Figure 5.15: Influence of the dc-link voltage (V_{dc}) on the input dc-side admittance of the VSI. (a) Topology 2 (K_d = *10*). (b) Topology 4.

5.7.2 Loading/Grid Parameters Impact on the DC-side Input Admittance

The value of the grid inductance (L_g) and the loading conditions are varied to study their effect on the input admittance. For topology 1, Figure 5.13(a) shows the input admittance under variation of the grid inductance (L_g). As shown, with the decrease of L_g, the resonant peak frequency increases as also concluded from (5.50). Moreover, the magnitude of the resonant peak decreases with decreasing L_g. The same trend applies for topology 2 in Figure 5.13(b) without significant effect on the negative range of the input admittance. This is also applied for topology 3. As shown, it is advantageous to operate with low inductive grid impedance (stiff grid).

The influence of the injected power to the load/grid on the input admittance is investigated as shown in Figure 5.14. The reduction effect of injected active power level is shown for topology 1 as in Figure 5.14(a). The magnitude of the input admittance decreases with the decrease in the injected active power, which enhances the stability margin according to Nyquist admittance ratio criterion. As shown with $Real\{\Delta Y_1\}$, the resonant peak decreases with lower active power injection due to the resultant lower sensitivity of the dc-current (I_{dc}) to dc voltage disturbances.

The input admittance response for topology 2 is shown in Figure 5.14(b). The power level has higher influence on the input dc admittance. With lower injected active power, less magnitude of the input admittance is yielded and spans less frequency band

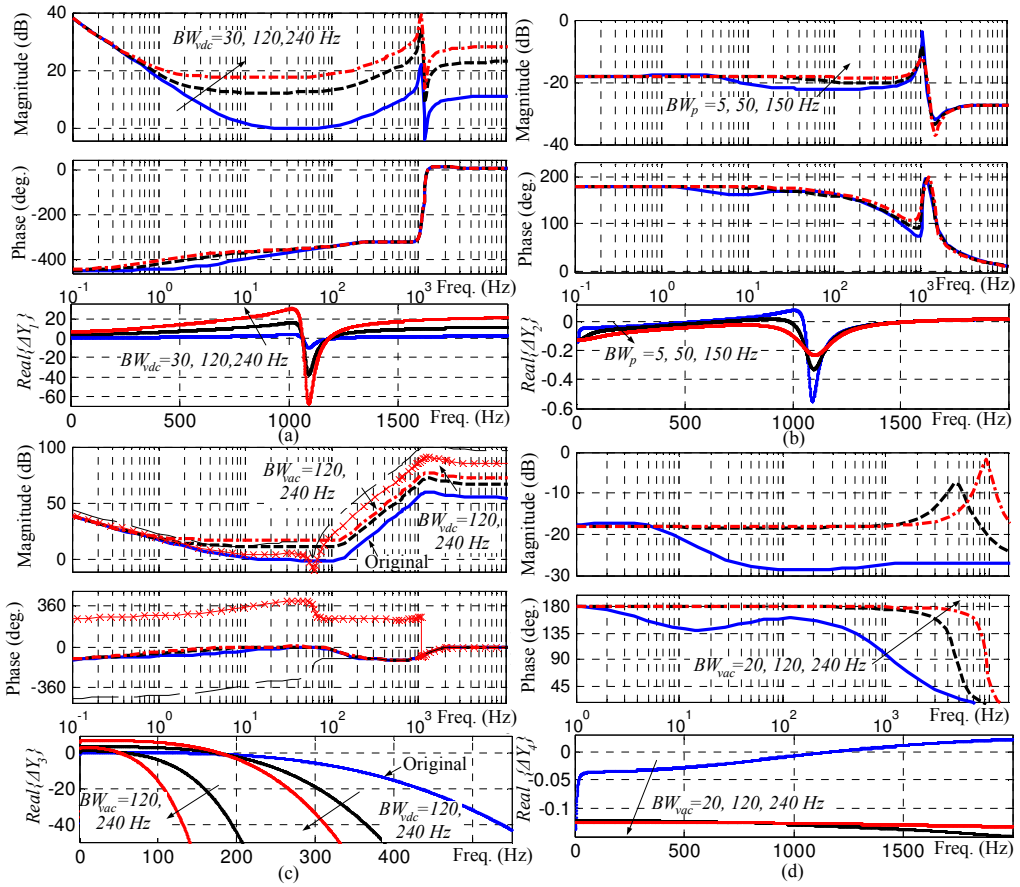

Figure 5.16: Impact of the outer loop controller on the input dc-side admittance of the VSI. (a) Topology 1. (b) Topology 2. (c) Topology 3. (d) Topology 4. For topology 1, 2 and 3; K_d = *10*.

of the negative admittance range. As shown, with the decrease of active power from 1.0 to 0.1 p.u., the admittance magnitude decreased by about 20 dB with lower negative phase angle up to 1 Hz. This is also shown by $Real\{\Delta Y_2\}$, where it has positive value in low frequencies with reduced resonant peak as the injected active power decreases. Note that $P_o \approx V_{dc} I_{dc}$, without V_{dc} regulation from VSI side in topology 2, the dynamics of the injected dc current (I_{dc}) from the dc-link is coupled to active power injection (P_o) which is defined by the outer loop active power controller. As result, high influence of the active power injection on reshaping the input dc-side admittance is yielded.

In topology 3, the magnitude of the input admittance decreases with the reduction of the supplied active power as shown in Figure 5.14(c). The negative value of $Real\{\Delta Y_3\}$ is positively shifted with 0.1 p.u. active power supply. With the reactive power

injection, the input admittance is also plotted with different values of the load power factor (pf) on the same Figure. Unlike the active power influence, the effect of low *pf* loading is negligible.

The input admittance for topology 4 is shown in Figure 5.14(d). The reduction of the supplied active power decreases the magnitude of the admittance and yields higher stability margin, which appears in $Real\{\Delta Y_4\}$ as it becomes more positive with lower active power generation. As the load *pf* decreases, the magnitude of ΔY_4 increases with lower stability margin. This is reflected to $Real\{\Delta Y_4\}$ as it becomes more negative with lower *pf*.

This subsection summarizes the following:

- The general trend is that the input admittance of VSI is more damped with low active power supply and high load *pf*.
- Active power injection has higher influence on topology 2 as compared to topology 1.
- Reactive power supply has higher influence on topology 4 as compared to topology 3.
- The un-regulated dc-link (from VSI side, as topology 2 and 4) is more sensitive to input admittance re-shaping due to power injection levels.

5.7.3 Reference DC-Link Voltage Impact on the DC-side Input Admittance

The dc-link voltage settings are taken into account to study its influence on reshaping the input admittance of VSI as shown in Figure 5.15. With higher dc-link voltage, the magnitude of ΔY_2 or ΔY_4 decreases (higher stability margin). $Real\{\Delta Y_2\}$ and $Real\{\Delta Y_4\}$ become more positive with higher dc-link voltage. Moreover, the resonant peak magnitude with topology 2 decreases with higher V_{dc}. There is no considerable variation on the phase angle of ΔY_2 or ΔY_4. Also, for topology 1 and 3, there is no considerable effect of the magnitude of V_{dc} on the input admittance due to the employed dc-link voltage regulators which increase the dc-link robustness.

5.7.4 Outer Loop Controllers Impact on the DC-side Input Admittance

The input admittance reshaping due to the outer loop controllers is investigated in each topology. For topology 1, the effect of the dc voltage controller $G_{vdc}(s)$ is shown as in Figure 5.16(a). With the increase of the dc voltage controller bandwidth, i.e. the tight regulation bandwidth, the magnitude of the input admittance increases with lower stability margin. As shown by $Real\{\Delta Y_1\}$, the resonant peak becomes more negative as the bandwidth increases.

The effect of outer power controller $G_p(s)$ on the input admittance of the VSI is shown in Figure 5.16(b). As the bandwidth increases, the input admittance degrades with higher negative frequency range. On the contrary, the increase of the tight regulation effect reduces the resonant peak in the magnitude of the input admittance.

In topology 3, the effect of both the outer ac voltage controller $G_{vac}(s)$ and dc-link voltage controller $G_{vdc}(s)$ is considered as in Figure 5.16(c). The increase of $G_{vdc}(s)$ bandwidth results in increasing the magnitude of the input admittance which may violate the Nyquist criterion. This is reflected to $Real\{\Delta Y_3\}$ as it goes further to negativity. As shown, similar influence is yielded with the increases of the bandwidth of $G_{vac}(s)$. However, the system stability is highly degraded by $G_{vac}(s)$ as compared to $G_{vdc}(s)$ bandwidth increase which is also clear from $Real\{\Delta Y_3\}$ as it has higher negative values.

The influence of $G_{vac}(s)$ in topology 4 on the input admittance is shown in Figure 5.16(d). With the increase of the ac voltage controller bandwidth, the phase angle of the input admittance approaches 180 °. The negative frequency range of $Real\{\Delta Y_4\}$ increases with larger negative resistance that appears to the dc-link, which degrades the system stability.

5.7.5 Sensitivity Analysis (VSI Output Against DC-Link Voltage Disturbances)

The influence of the dc voltage disturbances on the output currents in grid-connected mode as in (5.24) and (5.27) or the output ac voltage in islanded mode as in (5.37) and (5.41) is investigated in this section. In the grid-connected mode, the *LCL* resonant peak appears. The sensitivity functions reflect the performance of the VSI from the grid/load-side while the input admittance analysis in the previous section was

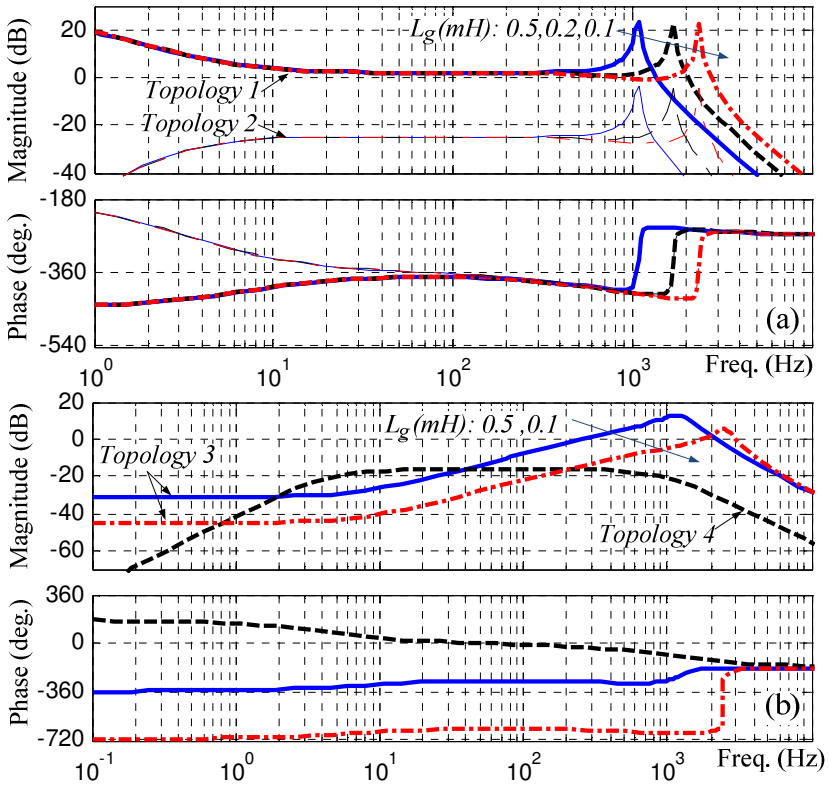

Figure 5.17: Sensitivity functions against dc-link voltage disturbance. (a) Output ac current. (b) Output ac voltage. For topology 1, 2 and 3; $K_d = 10$.

mainly concerned with the input characteristics of the VSI from the perspective of the dc-network around the common dc-link.

As shown in Figure 5.17(a), the injected ac current is more sensitive to the dc voltage disturbances with the case of dc-link voltage regulator. In Figure 5.17(b), the effect of reducing the grid inductance is to increase the resonant frequency with topology 3 according to (5.50) and to decrease the sensitivity of the output ac voltage against dc-link voltage disturbances.

The effect of the tight regulation of the outer loop controllers on the VSI output is also investigated using sensitivity functions. As shown in Figure 5.18(a), the increase of the tight regulation of the dc-voltage controller bandwidth in topology 1 increases the sensitivity of the injected current against V_{dc} disturbances. This effect is reversed when an outer average power controller is employed with dispatchable DG units (topology 2). This is clearly a tradeoff, because increasing the tight regulation bandwidth of $G_p(s)$ degrades the dc-link stability by increasing the negative

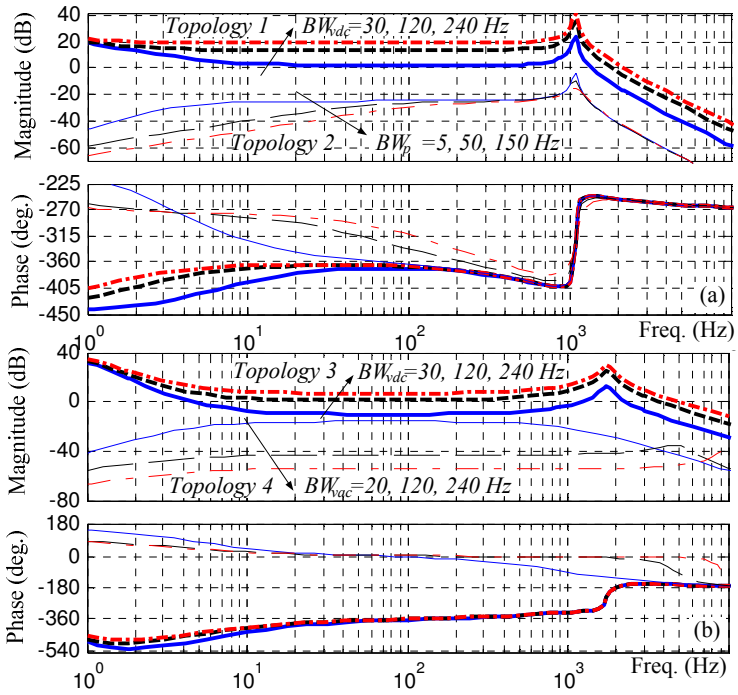

Figure 5.18: Influence of the outer loop controllers on the sensitivity functions against dc-link voltage disturbance. (a) Output ac current. (b) Output ac voltage.

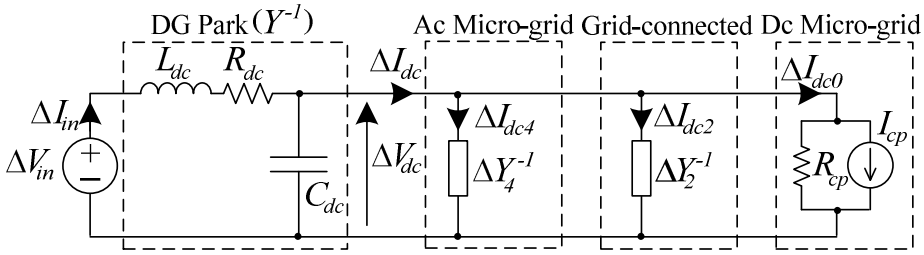

Figure 5.19: Small-signal model of the hybrid ac/dc converter dominated network.

characteristics of $Real\{\Delta Y_2\}$ [Figure 5.16(b)], however, the VSI outputs becomes more robust against V_{dc} disturbances. But note that the robustness increases only in the low frequency range (up to 100 Hz).

The sensitivity of the controlled output ac voltage in grid-connected mode for topology 3 and 4 is investigated in Figure 5.18(b). For topology 3, the increase of the bandwidth of $G_{vdc}(s)$ increases the output voltage sensitivity to V_{dc}. On the other hand, increasing the bandwidth of $G_{vac}(s)$ has no influence on the output ac-voltage (solid bolded line, topology 3). For topology 4, the increase of the bandwidth of

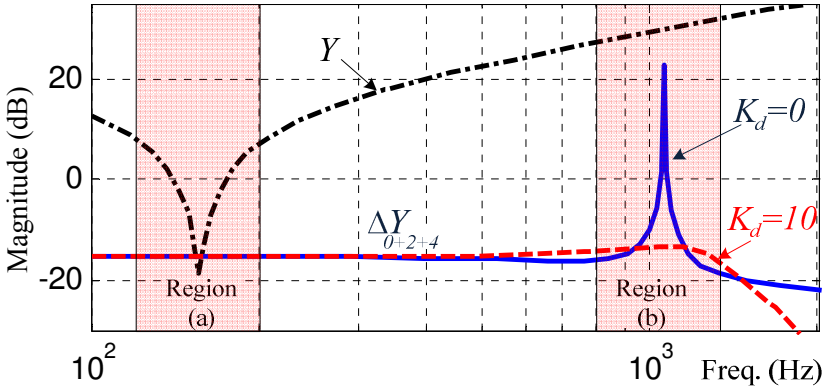

Figure 5.20: Possibilities of Nyquist criterion violation in hybrid network. Region (a): due to equivalent RLC circuit of DG Park. Region (b): due to ac-side resonant peak of the LCL filter.

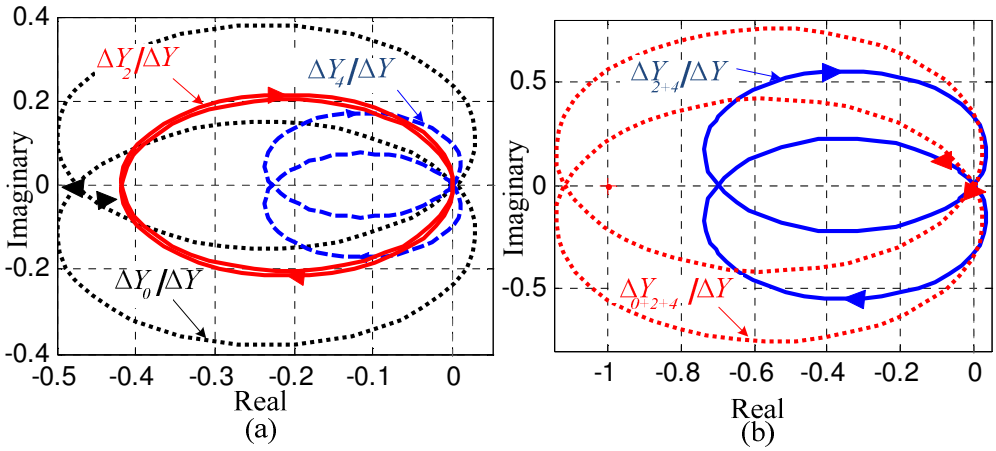

Figure 5.21: Nyquist criterion for the hybrid network.

$G_{vac}(s)$ decreases the sensitivity of the output ac voltage against V_{dc} disturbances implying the same tradeoff as with topology 2.

5.8 Interaction Dynamics in Hybrid Grids

The hybrid network in Figure 5.1 can be modeled as cascaded small-signal input/output admittance-based circuit as shown in Figure 5.19. In this section, dispatched DG units are only considered (ΔY_2, ΔY_4).

Admittance-based analysis can be easily conducted on the network to judge the system stability using Nyquist criterion. Interaction dynamics in multi-converter systems are mainly attributed to following reasons.

1- Interactions among the total input/output admittances of the multi-converter system at the point of investigation (such as the dc-link in Figure 5.1). Using (5.1), (5.3),

(5.26) and (5.40), the frequency response of the of Y and ΔY_{0+2+4} is shown in Figure 5.20. Admittances magnitude may interact around two resonant peaks; from the source-side at low frequency (region (a)) due to dc-RLC equivalent output circuit or from the load-side at high frequency (region (b)) due to ac-LCL filter. It is clear that region (b) is not critical as the ac-LCL resonant peak can be actively mitigated with the active compensation loop with a gain K_d. With $K_d = 10$, the ac-LCL resonant peak can be totally mitigated, which, increases the stability margin at that frequency range with less probability of load/source admittance magnitude interactions. The low-frequency violation region (Region (a)), can be passively mitigated by reshaping Y with higher resistance in series with R_{dc}, an inductance in parallel with L_{dc} or higher capacitance (C_{dc}) to satisfy the Nyqusit criterion. However, all of these methods are not preferred due to cost, reliability, efficiency and system size considerations. Alternatively, active compensators are proposed in this Chapter to actively reshape the equivalent input admittance (Y_{0+2+4}) based on the interfacing VSI.

Nyquist admittance ratio criterion is investigated in Figure 5.21. Active resonant damping is utilized with $K_d = 10$ for the grid-connected inverter whereas a pure resistive loading is considered for the micro-grid that creates natural resonant damping to neutralize the effect of ac-LCL filter [region (b) in Figure 5.20]. Figure 5.21(a) implies inherent stable operation of one-DG-one-converter system ($\Delta Y_0/\Delta Y, \Delta Y_2/\Delta Y, \Delta Y_4/\Delta Y$). However, multi-cascading of these converters may violate the Nyquist criterion. As shown in Figure 5.21(b), the Nyqusit criterion is violated when considering the combined PE interfaces for the ac micro-grid, utility-grid and dc micro-grid ($\Delta Y_{0+2+4}/\Delta Y$). Even when neglecting the dc micro-grid, Nyquist plots for ($\Delta Y_{2+4}/\Delta Y$) show low stability margin that subjects the dc-link to probable instabilities.

2- In advanced PE systems, tight regulation control objectives of the interfacing stages induces their incremental input admittance to be negative in the low frequency range. At that particular frequency, any increase/decrease of the dc-link voltage causes decrease/increase of the supplied dc current from the dc-link (CP mode). As the incremental input admittance is negative, further increase/decrease in the dc-link voltage is yielded causing sustained oscillations or instabilities with inherent

negative damping. This factor is clearly shown in Figure 5.12 where the real part of ΔY_2 and ΔY_4 appears to the dc-link with a negative value in the low frequency range. Passive mitigation techniques can be adopted but are not preferred due to cost and size issues. On the other hand, the proposed active compensators actively mitigate the negative real part of input admittance that appears due to the CP operation as it will be shown in the next section.

5.9 Linear Active Compensators for Hybrid AC/DC Network

In this section, proposed active compensation techniques are provided to reshape the incremental input admittance of the VSI, by which the overall system stability of the hybrid network is improved. Figure 5.22 shows the proposed active compensation loops in both micro-grid and grid-connected mode of operation. The dc-link voltage (V_{dc}) is applied through a compensation function ($C_{2n}(s)$ or $C_{4n}(s)$) and injected to three possible nodes; outer, intermediate and inner node according to selector position "*o*", "*m*" and "*i*", respectively where the sub-script "*n*" referees to the selector position. This active loop mimics a passive element(s) that reshape the input admittances ΔY_2 and ΔY_4 of VSIs.

5.9.1 Modified Control Dynamics

For the grid-connected mode in Figure 5.22(a), the modified active power and current control dynamics in (5.25) and (5.16), respectively, are modified to:

$$I_d^* = \left(P_o^* - P_o \frac{\omega_p}{s+\omega_p} + C_{2o}(s)V_{dc}\right) C_p(s) + C_{2m}(s)V_{dc} \tag{5.51}$$

$$V_d^{inv} - sC_f V_{od} K_d = (I_d^* - I_d)G_i(s) + C_{2i}(s)V_{dc} - \omega L_f I_q + V_{od} \tag{5.52}$$

Using (5.51) and (5.52), the compensated small-signal input admittance (ΔY_2^c) with the corresponding sensitivity function are given by:

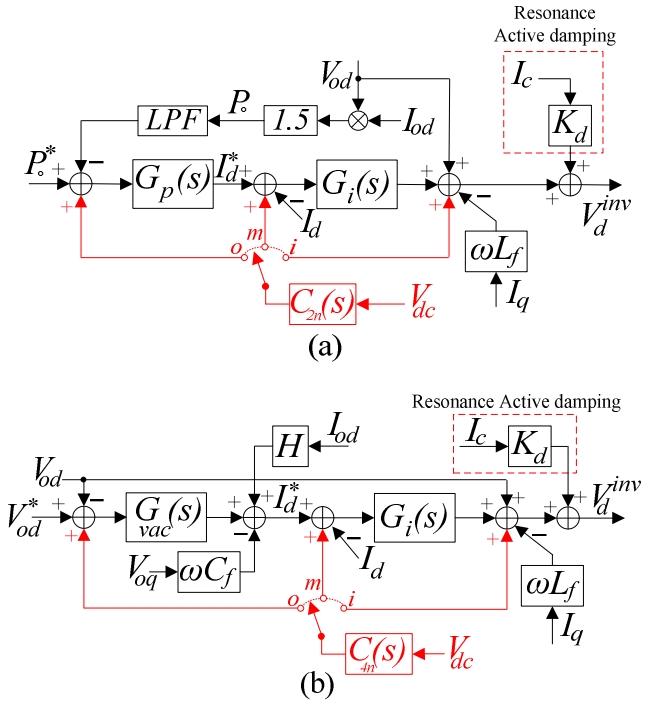

Figure 5.22: Proposed active compensators for hybrid networks. (a) Grid-connected inverter (topology 2). (b) Micro-grid inverter (topology 4).

$$\Delta Y_2^c(s) =$$

$$\frac{1}{V_{dc}^\circ}\left(\frac{1.5\left(\left(V_d^\circ+I_d^\circ(R_f+sL_f)\right)(sC_f+Z_l^{-1}+Z_g^{-1})+I_d^\circ\right)\left(\left(G_p(s)C_{2o}(s)+C_{2m}(s)\right)G_i(s)+C_{2i}(s)+\frac{V_d^\circ}{V_{dc}^\circ}\right)}{(sC_f+Z_l^{-1}+Z_g^{-1})\left(R_f+sL_f+G_i(s)\right)+1.5\frac{\omega_p}{s+\omega_p}G_p(s)G_i(s)\left(I_{od}^\circ+V_{od}^\circ(Z_l^{-1}+Z_g^{-1})\right)-K_d sC_f}-I_{dc}^\circ\right) \tag{5.53}$$

$$\frac{\Delta I_{od}^c}{\Delta V_{dc}^c}=\frac{\left(\left(G_p(s)C_{2o}(s)+C_{2m}(s)\right)G_i(s)+C_{2i}(s)+V_d^\circ/V_{dc}^\circ\right)(Z_l^{-1}+Z_g^{-1})}{(sC_f+Z_l^{-1}+Z_g^{-1})\left(R_f+sL_f+G_i(s)\right)+1.5\frac{\omega_p}{s+\omega_p}G_p(s)G_i(s)\left(I_{od}^\circ+V_{od}^\circ(Z_l^{-1}+Z_g^{-1})\right)-K_d sC_f} \tag{5.54}$$

One compensator is activated in (5.51)–(5.54) according to the selector position.

Utilizing the proposed compensators in the micro-grid mode as in Figure 5.22(b), the ac voltage and current control dynamics in (5.38) and (5.16), respectively, are modified as follows:

$$I_d^*=(V_{od}^*-V_{od}+C_{4o}(s)V_{dc})G_{vac}(s)+C_{4m}(s)V_{dc}-\omega C_f V_{oq}+HI_{od} \tag{5.55}$$

$$V_d^{inv}-sC_f V_{od}K_d=(I_d^*-I_d)G_i(s)+C_{4i}(s)V_{dc}-\omega L_f I_q+V_{od} \tag{5.56}$$

Using the modified control dynamics in micro-grid mode, the compensated small-signal input admittance (ΔY_4^c) is obtained in a compact form as follows.

$$\Delta Y_4^c(s) = \frac{1}{V_{dc}^{\circ}}\left(\frac{1.5\left(\begin{matrix}\left(V_d^{\circ}+I_d^{\circ}(R_f+sL_f)\right)\\ \times\left(sC_f+Z_l^{-1}\right)+I_d^{\circ}\end{matrix}\right)\left(G_{vac}(s)C_{4o}(s)+C_{4m}(s)\right)G_i(s)+C_{4i}(s)+\frac{V_d^{\circ}}{V_{dc}^{\circ}}}{\left(sC_f+Z_l^{-1}\right)\left(R_f+sL_f+G_i(s)\right)+G_{vac}(s)G_i(s)-Z_l^{-1}HG_i(s)-K_dsC_f} - I_{dc}^{\circ}\right) \quad (5.57)$$

The modified sensitivity function of the output ac voltage against dc-link voltage disturbances is given by:

$$\frac{\Delta V_{od}^c}{\Delta V_{dc}^c} = \frac{\left(G_{vac}(s)C_{4o}(s)+C_{4m}(s)\right)G_i(s)+C_{4i}(s)+V_d^{\circ}/V_{dc}^{\circ}}{\left(sC_f+Z_l^{-1}\right)\left(R_f+sL_f+G_i(s)\right)+G_v(s)G_i(s)-Z_l^{-1}HG_i(s)-K_dsC_f} \quad (5.58)$$

Note that only one compensator (out of three) is activated in (5.55) – (5.58) according to the selector position.

5.9.2 Design Approach and Stabilization

The provided active compensators in Figure 5.22 are proposed to actively reshape the incremental input admittance of VSI in hybrid network to satisfy two main objectives:

- Avoid input/output admittance magnitude interactions. [region (a) in Figure 5.20].
- Actively mitigate the negative value of the incremental input admittance at low frequency range (CP effect) especially around the resonant frequency of the equivalent DG park output admittance (Y).

Therefore, the proposed compensator function should be characterized by BP filtering capabilities to modify the admittance characteristics only around the probable frequency range of input/output admittance interactions (region (a)). Note that other compensation functions can be adopted with HP filtering characteristics but they influence the input admittance properties from the cut-off frequency of the HP filter and beyond. Accordingly, the proposed compensation function is given in the form of:

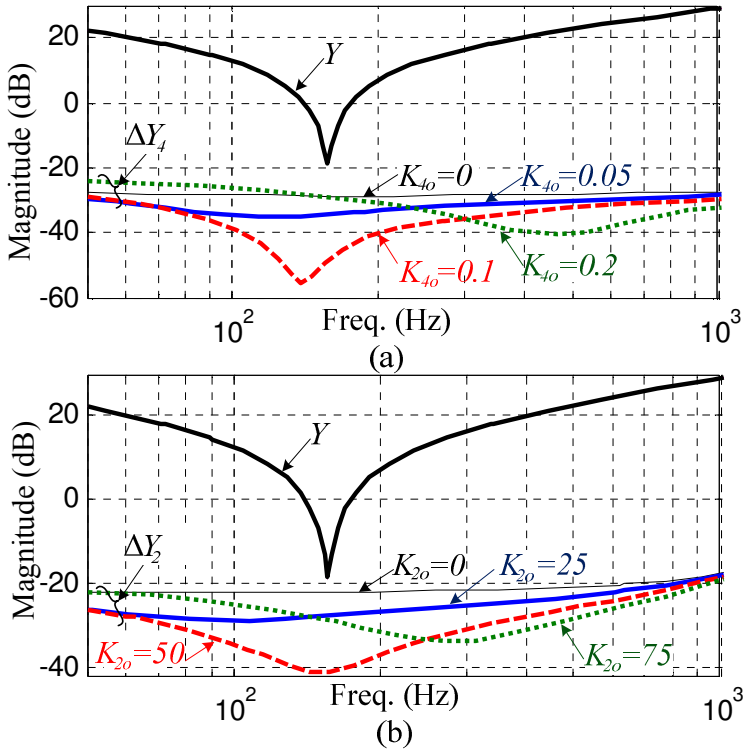

Figure 5.23: Influence of the proposed outer loop compensator on the incremental input admittance. (a) Micro-grid inverter – topology 4 (ω_{4o} = *550 r/s,* ξ_{4o} = *1*). (b) Grid-connected inverter – Topology 2 (ω_{2o} = *400 r/s,* ξ_{2o} = *1*).

$$C_{4n}(s) = K_{4n}\frac{2\xi_{4n}\omega_{4n}}{s^2+2\xi_{4n}\omega_{4n}s+\omega_{4n}^2} \tag{5.59}$$

where ξ_{4n} is the damping ratio, ω_{4n} is the operating frequency of the BP filter, and K_{4n} is the compensator gain. A similar form for $C_{2n}(s)$ is applied but with sub-script "$_{2n}$" instead of "$_{4n}$".

The influence of the proposed compensator on reshaping the incremental input admittance of VSI is investigated in Figure 5.23. As a design approach example, the outer loop compensator is employed in the micro-grid ($C_{4o}(s)$) and grid-connected inverter ($C_{2o}(s)$). For the intermediate and inner compensators in both VSI topologies, similar reshaping trend is obtained. In Figure 5.23(4), ΔY_4 is actively reshaped by selecting the operating frequency $\omega_{4o} = 550$ rad/sec to match the resonant peak of Y. With the increase of the compensator gain ($K_{4o} = 0.05, 0.1$), the magnitude of ΔY_4 is reduced as compared to the uncompensated case ($K_{4o} = 0$). Utilizing BP filtering

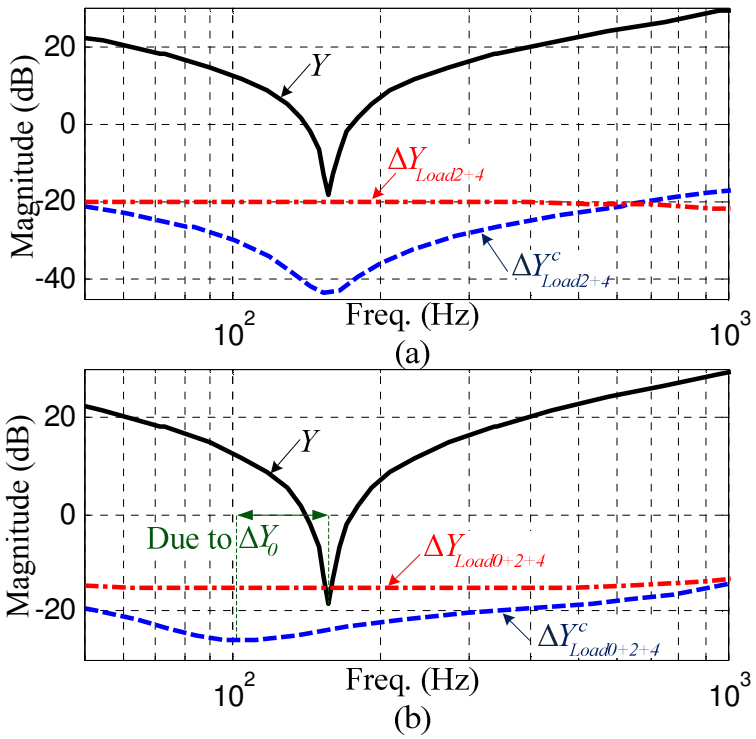

Figure 5.24: Influence of the proposed outer loop compensator on the hybrid network stability (ω_{4o} = *550 r/s,* ξ_{4o} = *1,* K_{4o} = *0.1,* ω_{2o} = *400 r/s,* ξ_{1o} = *1,* K_{2o} = *50*). (a) $\Delta Y_2 + \Delta Y_4$. (b) $\Delta Y_0 + \Delta Y_2 + \Delta Y_4$.

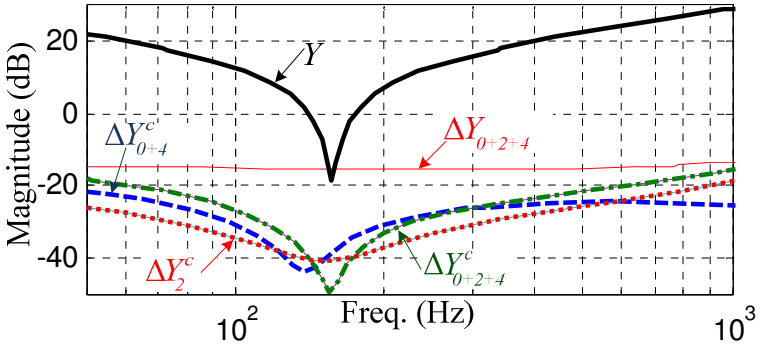

Figure 5.25: Augmented design of the hybrid network (ω_{4o} = *700 r/s,* ξ_{4o} = *1,* K_{4o} = *0.25,* ω_{2o} = *400 r/s,* ξ_{2o} = *1,* K_{2o} = *50*).

characteristics successfully reshapes the input admittance only around the region (a) in Figure 5.20 which, as result, immunes the system properties against significant deformation due to the employed active compensation loops. As shown, further increase of the compensator gain ($K_{4o} = 0.2$) reduces the stability margin. Therefore, careful selection of compensator gains should be considered in the design phase of the active compensators. Similarly, the outer loop compensator ($C_{2o}(s)$) is employed in

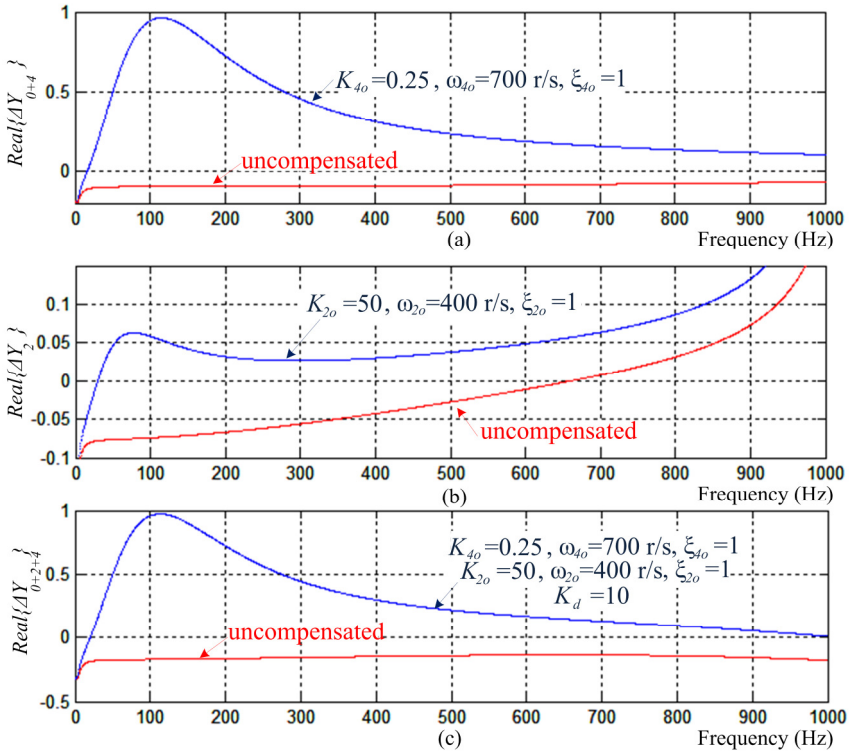

Figure 5.26: Real part of the uncompensated/compensated input dc-side admittances. (a) Ac micro-grid and generic dc micro-grid. (b) Grid-connected inverter. (c) Overall hybrid dc-side admittance.

the grid-connected inverter as shown in Figure 5.23(b) with a comparable response when $\omega_{2o} = 400$ rad/sec and $K_{2o} = 0 \rightarrow 50$.

The effect of activating both outer loop compensators on the hybrid network stability is investigated in Figure 5.24. In Figure 5.24(a), the generic model of the dc micro-grid is neglected in the design phase. As shown, the source (Y) and compensated load admittances $\left(\Delta Y_{2+4}^{c}(s)\right)$ are perfectly matched with the highest possible stability margin as compared to the uncompensated load admittance $\left(\Delta Y_{2+4}(s)\right)$. In Figure 5.24(b), the dc micro-grid model $\left(\Delta Y_{0}(s)\right)$ is considered in the hybrid network after selecting the compensator parameters where it shifts the undershot of the overall input admittance $\left(\Delta Y_{0+2+4}^{c}(s)\right)$ away from the resonant peak of Y which reduces the stability margin. Therefore, the generic model of the dc micro-grid has to be considered in the design phase of the VSI compensators. On other words, separate design of the proposed active compensators for the PE stages within the hybrid network is not preferred. Figure 5.25 shows how the stability margin can be

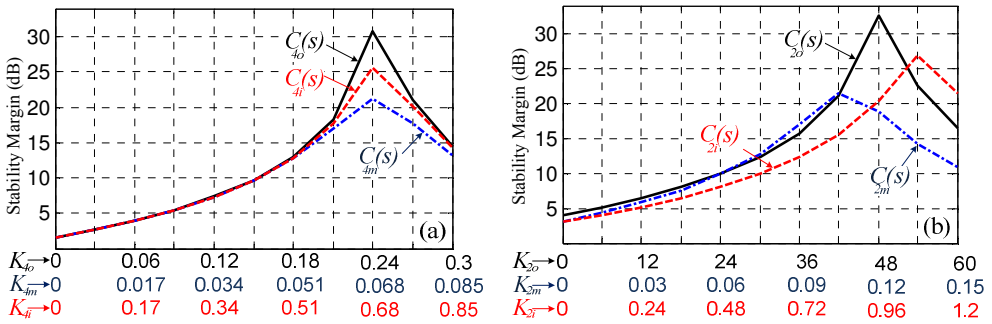

Figure 5.27: Influence of the proposed compensators on the hybrid network stability. (a) Ac micro-grid compensators ($C_{4n}(s)$). (b) Utility-interface compensators ($C_{2n}(s)$).

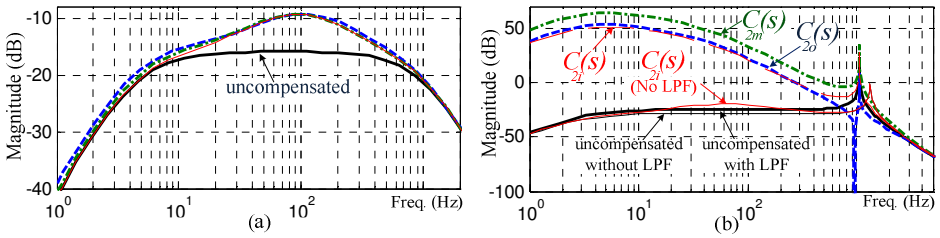

Figure 5.28: Sensitivity response with the proposed active compensators. (a) $|\Delta V_{od}/\Delta V_{dc}|$ in micro-grid inverter. (b) $|\Delta I_{od}/\Delta V_{dc}|$ in grid-connected inverter.

improved by considering the dc micro-grid model in the design phase of the active compensator. The parameters of $C_{4o}(s)$ are designed to actively reshape $\Delta Y^c_{0+4}(s)$ which demands higher ω_{4o} (700 rad/sec) and $K_{4o} = 0.25$. As result, the overall input admittance $\left(\Delta Y^c_{0+2+4}(s)\right)$ is reshaped with an "anti-resonant peak" to avoid any interaction with Y around region (a). With the proposed compensator, the difference between the magnitudes of the overall load and source admittances are about 40 dB in the whole frequency range implying high stability margin as compared to the uncompensated case, which clearly satisfies objective (1) [Section 5.8].

For further validation, objective (2) is investigated when employing the proposed compensator. Figure 5.26 (a) shows the real part of the input admittance of the ac micro-grid with the generic model of the dc micro-grid. As shown, with employing $C_{4o}(s)$, the real part of this combination is shifted to be positive as compared to the uncompensated one. Similarly, Figure 5.26 (b) shows the real part of the dc-side input admittance of the grid-connected inverter. The overall effect of both compensators on the hybrid network stability is clearly shown in Figure 5.26 (c) where $Real\{\Delta Y^c_{0+2+4}(s)\}$ is positive in a wide frequency range which satisfies objective (2).

Following a similar design approach, the compensator parameters in all topologies are depicted in Appendix A5.2.

5.9.3 Damping Capabilities

The stabilization capabilities of the proposed compensators are investigated in Figure 5.27. The influence of the $C_{4n}(s)$ on the hybrid network stability is shown in Figure 5.27 (a) where $C_{4n}(s)$ is activated but with fixed parameters (as depicted in Appendix A5.2). Similarly, Figure 5.27 (b) shows the influence of $C_{2n}(s)$ on the network stability margin when the corresponding $C_{2n}(s)$ is activated with fixed parameters as given in Appendix A5.2. The considered stability margin is calculated by taking the difference between $|Y|$ and $|\Delta Y_0 + \Delta Y_2^c + \Delta Y_4^c|$ at the resonant frequency of Y [region (a) in Figure 5.20] around which the Nyquist criterion can be violated.

As shown, the general trend is that the outer loop compensators yield the best damping capabilities, and then comes the intermediate loop compensator whereas the inner loop compensator yields the lowest stability margin. However, all stability margins are close to each other with a maximum difference of 10 dB. The idea behind the proposed compensators is that they map the lightly-damped modes in the open loop dynamics to the resultant closed loop system to be efficiently migrated to higher damped locations in the "*s*" plane. The mapping efficiency depends on the injection position of the compensation signal, the compensation function itself and the compensator gain. As noted, higher compensator gain does not imply higher stability margin. After certain gain limits, the generated compensator signal becomes heavily re-scaled causing significant deformation in the inverter dynamics with degraded input admittance characteristics [as concluded from Figure 5.23].

5.9.4 Sensitivity Analysis

The influence of employing the compensation loops to interfacing VSIs is investigated in this sub-section using the obtained sensitivity functions in (5.54) and (5.58). As shown in Figure 5.28(b), the influence of $C_{2n}(s)$ on the grid-connected inverters is higher than that of $C_{4n}(s)$ [Figure 5.28(a)] on the micro-grid inverter. Figure 5.28(a) shows that the voltage sensitivity is almost the same with the three compensation positions ($C_{4i}(s), C_{4m}(s)$ and $C_{4o}(s)$). In the grid-connected mode [Figure 5.28(b)],

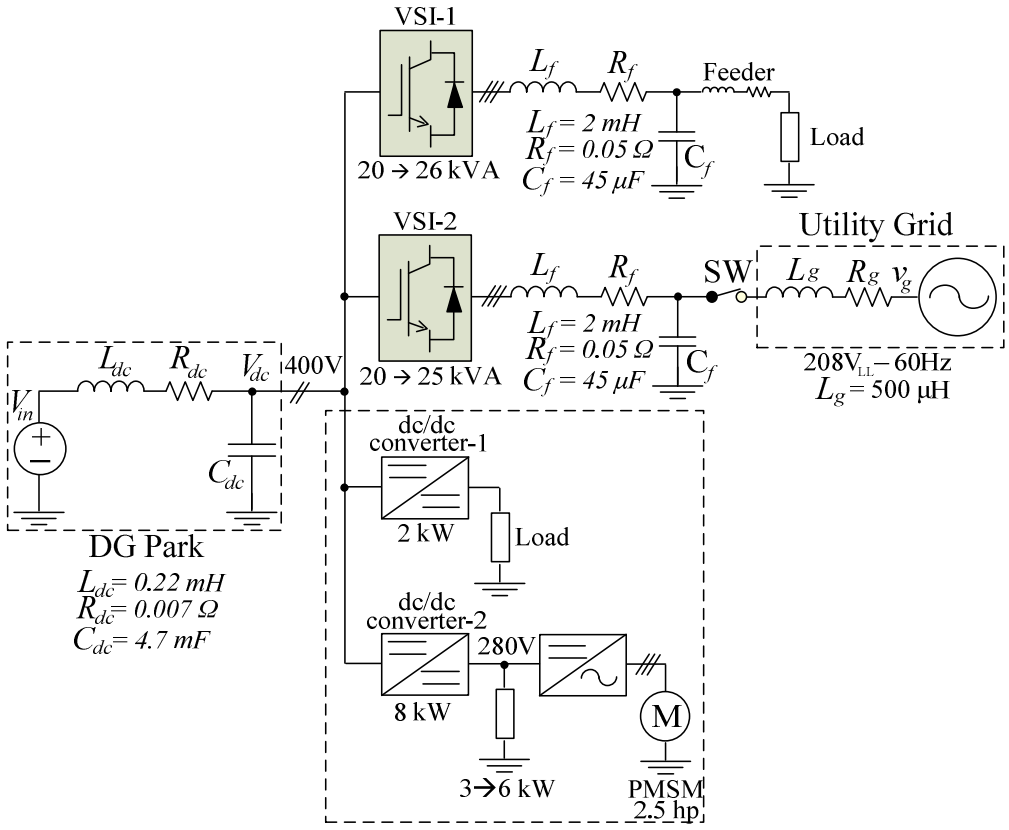

Figure 5.29: Schematic diagram of the implemented hybrid network.

the low frequency region of $\Delta I_{od}/\Delta V_{dc}$ is affected due to the utilized LPF with a low cut-off frequency in the active power control loop. As shown, the uncompensated sensitivity function without the LPF is almost the same when the LPF is considered. In contrarily, the LPF negatively interacts with the proposed compensators. For example, the inner loop compensator ($C_{2i}(s)$) is applied without considering the LPF of the power calculation loop which yields a close response to the uncompensated case as compared to $C_{2i}(s)$ response with the LPF. However, using LPF is significant as it isolate the grid-side disturbances from the control performance.

5.10 Evaluation Results

To evaluate interactions dynamics in hybrid ac/dc DG networks and proposed solutions, a 50 kVA hybrid network as shown in Figure 5.29 is implemented under Matlab/Simulink® environment. The system consists of a 20 kVA ac micro-grid

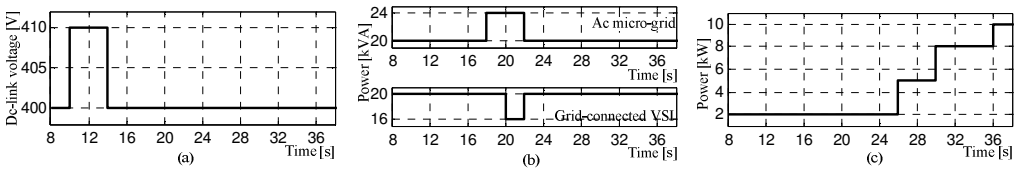

Figure 5.30: Loading curve of the hybrid network. (a) Dc voltage of DG Park. (b) Injected power to the ac micro-grid and utility-grid. (c) Injected power to the dc micro-grid.

interfaced by VSI-1, utility-grid interface rated at 20 kVA (VSI-2) and a dc micro-grid that includes two dc/dc converters; one supplies a resistive load of 2 kW while the other is connected to a variable resistive load (3 → 6 kW) and a 2.5 hp PMSM drive. All subsystems are connected to a DG park that is implemented by its aggregated equivalent model with a nominal dc voltage of 400 V. The power ratings with the physical parameters are all shown in Figure 5.29.

The operating scheme of the hybrid network is provided in Figure 5.30 by a loading curve for each entity. As shown, successive and harsh disturbances are applied to both source- and load-sides to emulate possible operating conditions in a hybrid DG system. For the source-side, Figure 5.30(a) shows the dc voltage profile of the equivalent source voltage of the overall DG Park. These disturbances can be induced due to connection/disconnection of a DG unit or variation in the renewable energy resource levels of a DG unit (wind energy, insolation level …etc.). Figure 5.30(b) shows the loading curve of the ac micro-grid with an instant loading increase from 20 kVA to 24 at t = 18 s before recovering back to the rated load (20 kVA) at t = 22 s. For the grid-connected inverter, Figure 5.30(b) shows the injected power profile. As shown, at t = 20 s, the injected power to the utility-grid is reduced to 16 kVA to cope with the increased loading at the ac micro-grid [at t = 18 s in ac micro-grid loading curve]. Figure 5.30(c) shows the loading curve of the dc micro-grid. With dc/dc converter-2, a base-load of 2.5 hp PMSM drive is considered while the variable resistive load is instantly varied from 3 kW to 6 kW at t = 30 s. The 2 kW resistive load of dc/dc converter-1 is only active at $t \geq 36$ *s*.

Different operating conditions are considered to investigate interaction dynamics in the hybrid network. These scenarios include interactions among the DG park (Y) and:

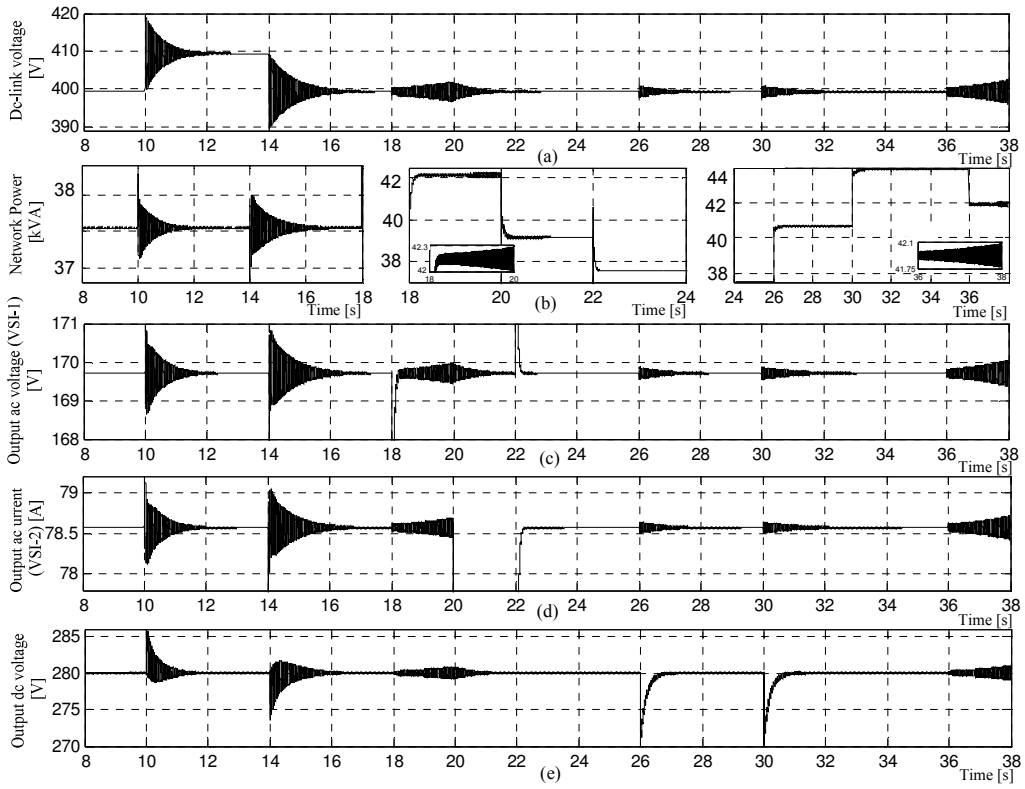

Figure 5.31: Hybrid network response – Uncompensated. (a) Dc-link voltage (V_{dc}). (b) Total injected power from the dc-link to the hybrid network. (c) Output ac voltage of micro-grid VSI (V_{od}). (d) Output ac current of the grid-connected VSI (I_{od}). (e) Output dc voltage of dc-dc converter- 2.

1- Grid-connected VSI (Y_2), Micro-grid VSI (Y_4) and dc micro-grid (Y_0) without the proposed compensators [Figure 5.31].

2- The hybrid network without the grid-connected VSI (Y_2) and without the proposed compensators [Figure 5.32(a)].

3- Grid-connected VSI (Y_2) only, without the proposed compensators [Figure 5.32(b)].

4- Micro-grid VSI (Y_4), Grid-connected VSI (Y_2) and dc micro-grid (Y_0) with the proposed compensators [Figure 5.33].

5.10.1 Uncompensated Conditions

Without employing the proposed compensators, and applying the load curve in Figure 5.30, the hybrid network response is shown in Figure 5.31. The influence of the DG park disturbances is reflected to V_{dc} in Figure 5.31(a) with decaying oscillatory response at t = 10 and 14 s. The effect ac micro-grid loading increase from 20 to 24 kVA at t = 18 s drives the dc-link voltage to instabilities. However, a decaying

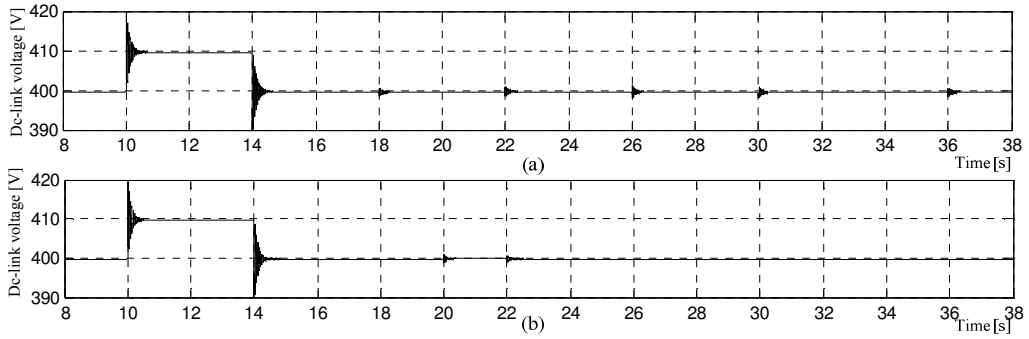

Figure 5.32: Dc-link voltage response in the hybrid network with individual entities combinations. (a) DG Park, micro-grid VSI and dc micro-grid interactions. (b) DG Park and grid-connected VSI interactions.

response from t = 20 s is noted due to the reduced injected power to the utility-grid that re-migrate the overall system modes to more stable positions. The influence of the dc micro-grid disturbances is also investigated at t = 26, 30 and 36 s.

As shown, the dc-loading increase causes a disturbed dc-link voltage response that may lead to complete instabilities as shown at t = 36 s when dc/dc converter-1 is activated.

The lightly-damped response of V_{dc} is spread to the hybrid network entities. As a result, the injected active power from the dc-link side, shown in Figure 5.31(b), has an unstable response at t = 18 and 36 s. Moreover, load-side performance in each entity is severely degraded. The d-axis component of the ac voltage (V_{od}) of the ac micro-grid VSI and ac current (I_{od}) of the grid-connected VSI are shown in Figure 5.31(c) and (d), respectively. In Figure 5.31(c), there is high undershoot of 152 V at t = 18 s and overshoot of 190 V at t = 22 s [not completely shown in Figure 5.31(c)] due to the loading (20 → 24 kVA) and unloading (24 →20 kVA) at these instants, respectively. Note that similar over/under shoots in I_{od} of grid-connected VSI does not appear as the loading disturbance is totally applied to the ac micro-grid load-side. The load-side performance of the dc micro-grid is investigated in Figure 5.31(e). Driven by the hybrid network dynamics, the dc-side voltage builds-up with unstable response at t = 18 and 36 s. High undershoots of 271 V are also produced due to the sudden loading increase of 3 kW at t = 26 and 30 s [as shown in Figure 5.30(c)].

The dc-link voltage response is shown in Figure 5.32(a) when the hybrid network includes the DG park, micro-grid VSI and the dc micro-grid only. As shown, with the same load curves in Figure 5.30, the dc-link voltage response is stable even with at

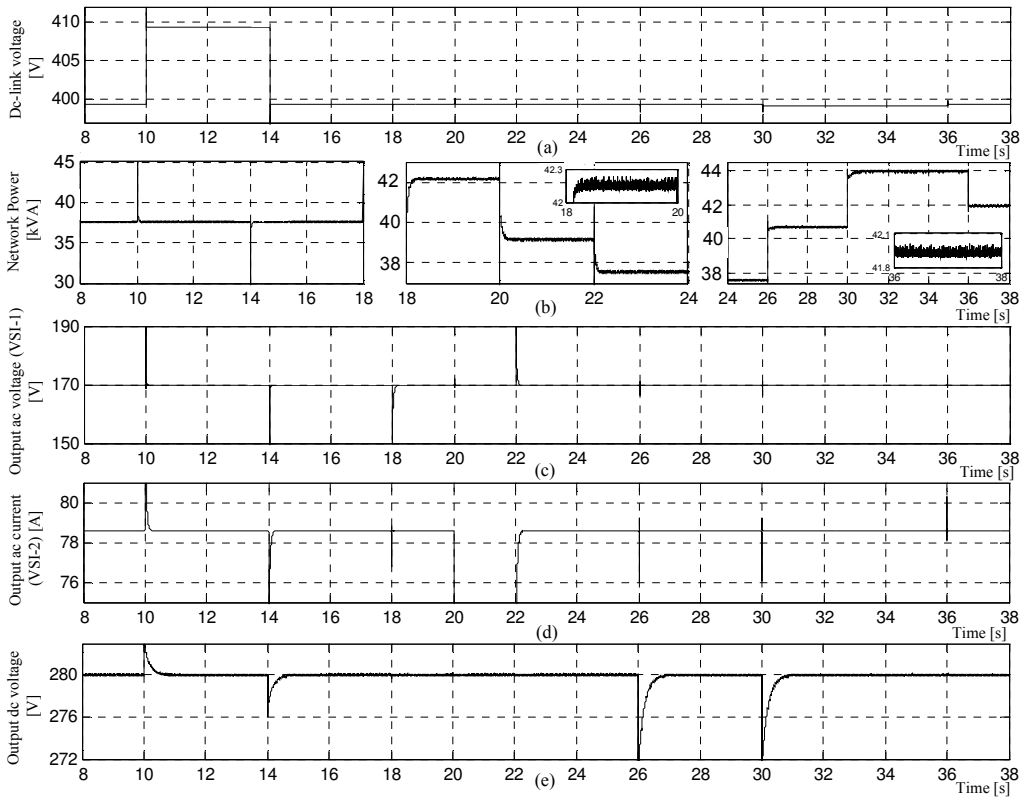

Figure 5.33: Hybrid network response – Outer loop compensator. (a) Dc-link voltage (V_{dc}). (b) Total injected power from the dc-link. (c) Output ac voltage of the micro-grid VSI (V_{od}). (d) Output ac current of the grid-connected VSI (I_{od}). (e) Output dc voltage of dc-dc converter-2.

sudden loading/unloading at t = 20 and 22 s, respectively. In Figure 5.32(b), only grid-connected VSI is individually interfaced to the DG Park which yields a similar stable dc-link response. However, if the overall hybrid network is considered, the system stability becomes a considerable issue as shown in Figure 5.31. These results imply that the Nyquist criterion may be violated even if each individual entity is inherently stable as analytically concluded in Figure 5.21.

5.10.2 Proposed Compensators

With the same hybrid network model in Figure 5.29 and loading curve in Figure 5.30, the system response is re-investigated with the proposed compensators. As shown in Figure 5.33(a), the outer loop compensator provides high damping capabilities for the dc-link voltage with minor overshoots instead of the oscillatory/unstable response with the uncompensated system [Figure 5.31(a)]. The stable response of the dc-link voltage

is propagated to the hybrid network entities and is reflected to the overall performance. As shown in Figure 5.33(b), the injected active power from the dc-link side is highly damped as compared to the uncompensated response in Figure 5.31(b).

The load-side performance of the hybrid network under the proposed outer loop compensator is also investigated. Figure 5.33(c) and (d) shows the ac voltage response for micro-grid VSI and the injected ac current from the grid-connected VSI. Both of them are stable with high damping capabilities as compared to the uncompensated case.

Similarly, the dc-side response of dc-dc converter-2 implies the high damping capabilities of the proposed compensator as shown in Figure 5.33(e).

In spite of the positive effect of the proposed compensators on system stability, the output performance of VSI is affected. As shown in Figure 5.33(c) and (d), the ac voltage and current responses are damped but with higher over/under shoots at the instants of disturbances as compared to the uncompensated case. For instance, at t = 10 s, the ac voltage overshoot peak is 209.7 V with the outer loop compensator (though its stabilized performance) while it is 171.6 V with the uncompensated case [Figure 5.31(c)]. Hence, there exists a tradeoff between stabilizing the dc-link voltage and magnifying over/under shoots in the output performance of the VSI. However, this tradeoff is not significant as compared to advantageous damping capabilities of the proposed compensators. Moreover, these over/under shoots can be avoided by reducing the compensator gain but at the expense of resultant lower damping capabilities. Figure 5.34 shows dc-link voltage response (V_{dc}), the output ac-voltage (V_{od}) of micro-grid VSI and the output ac current (I_{od}) of grid-connected VSI with high and low damping capabilities. As expected, the dc-link voltage damping is degraded as compared to the highly damped response in Figure 5.34(a). However as shown in Figure 5.34(b), with the lower damped conditions, the overshoot peak of V_{od} at t = 10 s is 186.1 V as compared to 209.8 V with the highly-damped performance. Similarly as shown in Figure 5.34(d), the overshoot peak of I_{od} at t = 10 s with the lightly-damped condition is 91.26 A while it is 112.7 with the highly-damped conditions. The three-phase response of both output ac voltage and current are shown in Figure 5.34(c) and (e), respectively. It can be noted that the highly-damped performance has no significant

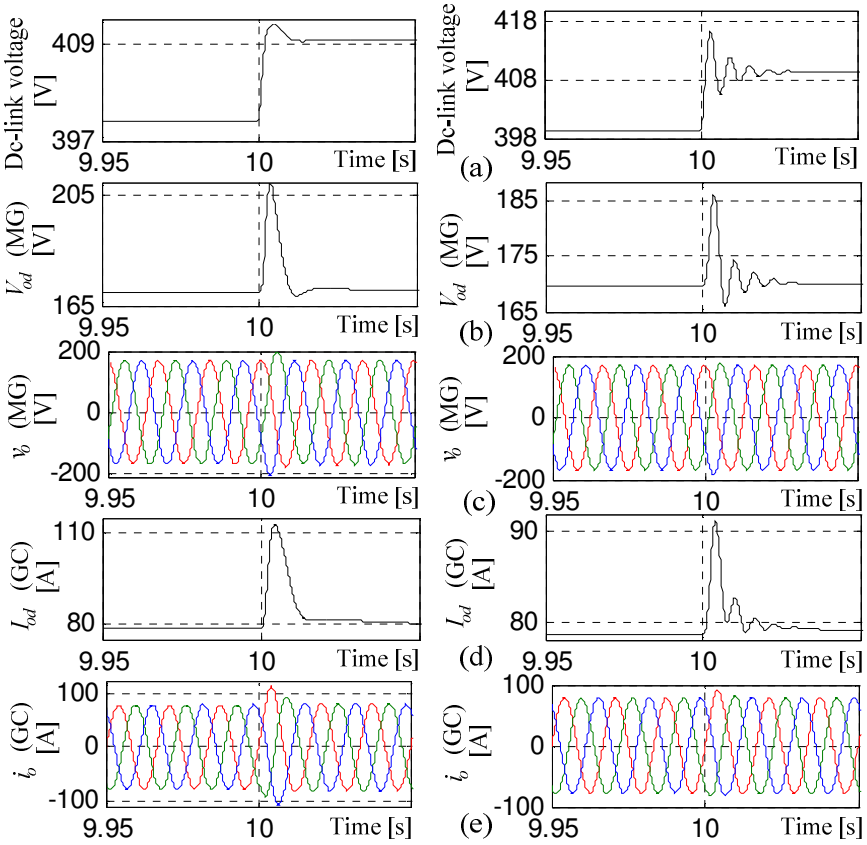

Figure 5.34: Tradeoff effect of the proposed active compensator. Left: Highly damped performance. Right: Lightly-damped performance. (a) Dc-link voltage. (b) *d*-axis component of the output ac voltage of the micro-grid (MG) VSI. (c) Three-phase output ac voltage of the micro-grid VSI. (d) *d*-axis component of the output ac current of the grid-connected (GC) VSI. (e) Three phase output ac current of the grid-connected VSI.

degradation on the output VSI parameters. As shown, less than one cycle is affected with overshoots in accepted limits.

Using the same hybrid network Simulink model, large-signal disturbances are applied at the load-side to check the robustness of the proposed compensators. As shown in Figure 5.35(a), the rated 20 kVA load is directly applied to VSI-1 at t = 0.3 s while a step active power injection from 10 kW to 20 kW is applied at t = 0.6 s for the grid-connected VSI. The hybrid network is assumed to startup at pre-charged dc-link condition by which the dc-link voltage is maintained at 400 V. As shown in Figure 5.35(b) and (c), the output ac voltage for micro-grid VSI or the ac current for the grid-

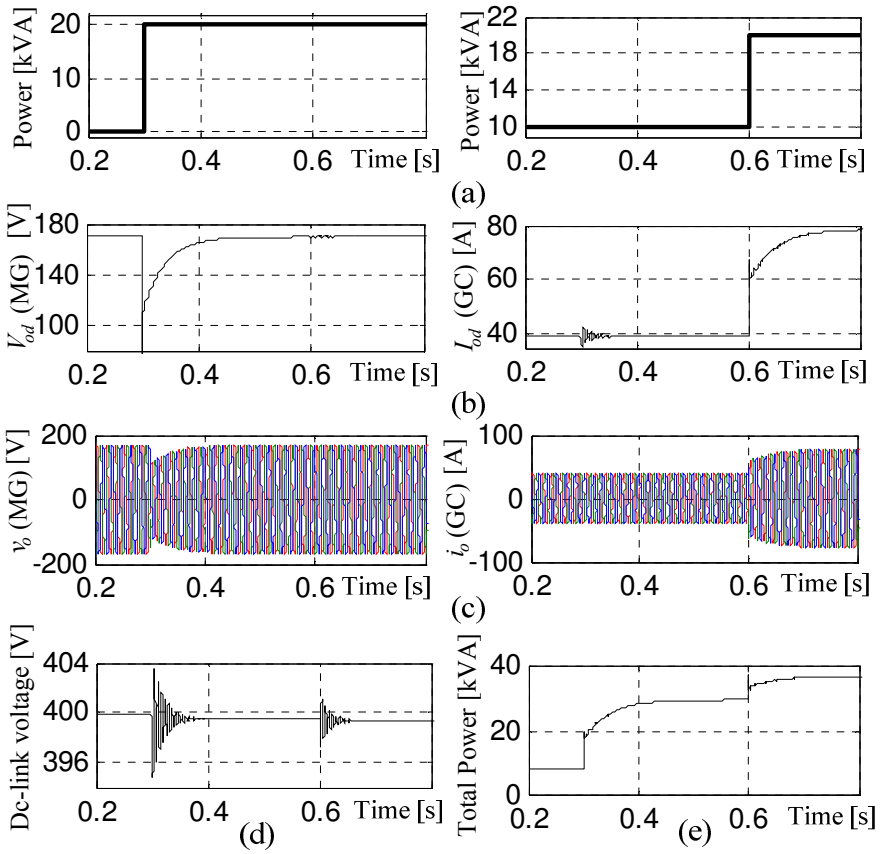

Figure 5.35: Large-signal response – Highly-damped outer loop compensator. (a) Left: Ac micro-grid (MG) load power. Right: Injected active power to the grid-connected (GC) VSI. (b) Left: *d*-axis component of the output ac voltage of the micro-grid VSI. Right: *d*-axis component of the output ac current of the grid-connected VSI. (c) Left: three phase ac voltage of the micro-grid VSI. Right: three phase ac current of the grid-connected VSI. (d) Common dc-link voltage. (e) Total injected active power from the dc-link.

connected VSI is sufficiently damped under large-disturbances implying the robustness of the proposed compensator. Due to the heavy loading condition at t = 0.3 s at micro-grid VSI, there exists a voltage dip in the output ac voltage. The minimum three phase peak voltage is 115.7 V at the loading instant (0.3 s). However, the voltage rapidly recovers with 152.2 V at t = 0.35 s.

The resultant robustness is reflected to the dc-link response as shown in Figure 5.35(d) and (e) for the dc-link voltage and the injected active power, respectively.

The outer loop compensator has been considered and presented with simulation results in this section while the results for the other two compensators are not included as they are close to Figure 5.33. They also satisfy the analytical results in Figure 5.27

that implies close damping capabilities for the proposed compensators. A similar influence on the ac-side parameters of the both VSIs is obtained as also concluded from the sensitivity analysis in Figure 5.28.

5.11 Conclusion

An analytical study of the input admittance of VSI in DG micro-grid systems has been presented. Depending on the system configuration, the VSI can be reflected to the dc-link side as an incremental negative input admittance. The characteristics of the input admittance of VSI are as follows:

- In non-dispatchable DG units, the input admittance is mainly negative in the low frequency region, whereas it is almost positive with dispatchable DG units.
- Resonant peaks may be reflected from the ac-side to the input admittance; hence system stability may be degraded.
- Resonant damping techniques can be used to suppress resonant peaks, however, a care should be taken when designing the resonant damper to limit the increase of the frequency range of the negative input admittance of VSI (especially with dispatched DG units).
- Away of the ac filter resonance frequency, the grid parameters have no significant influence on reshaping the input admittance of VSI.
- The input admittance of VSI is more damped at lower levels of injected active power and high load power factor.
- Higher system stability margin with more damped input admittance of VSI is obtained when operating under higher dc-link voltage levels.
- With non-dispatchable DG units, the sensitivity of the output ac currents in grid-connected mode or the output ac voltage is islanded mode to dc-link voltage disturbances is higher than these with dispatchable DG units; despite the fact that their dc-link voltage responses are lightly-damped.

It is shown that the Nyquist admittance ratio criterion can be violated in the cascaded multi-converter system even if each individual entity is inherently stable. Moreover, the tightly-regulated control objective of advanced PE converter in DG systems yields an incremental negative input admittance reflected to the common dc-link. Therefore, simple and effective active compensators solutions are proposed to

actively reshape the incremental input admittance of the VSI interfaced entities to satisfy the Nyquist criterion and virtually insert positive resistance to the negative incremental one in the low frequency region so that the stability margin is significantly improved. On the other hand, a tradeoff between stabilizing the common dc-link voltage in the hybrid network and increasing the sensitivity of the output parameters of VSIs towards the dc-link voltage disturbances is yielded. However, a well-designed compensator that compromises the associated tradeoff can be provided with low impact on the output parameters of VSIs. Moreover, the hybrid network shows well-damped performance under large-signal disturbances implying high robustness of the proposed compensators.

Chapter 6

Conclusions

6.1 Summary and Contributions

This thesis has assessed the interaction dynamic problems in converter-dominated power grids. The system stability is investigated by adopting the Nyquist admittance ration criterion. Small-signal linearization analysis is also utilized to obtain the equivalent load (input) or source (output) admittance of different PE converters around the interconnection point of interest. The stability criterion is maintained if the ratio between the equivalent load and source admittances is less than unity. The Nyquist criterion can be satisfied using passive elements in either the source- or load-side, however, this solution is not preferred in advanced PE converter grids and renewable energy systems. Therefore, proposed active compensators are provided in this thesis from load- or source-side according to each application to mimic passive damping characteristics and enable virtual input/output admittance reshaping. In all scenarios throughout the thesis Chapters, Matlab/Simulink platform has been used with different models of converter-dominated grids to validate the analytical results and the effectiveness of the proposed active solutions.

Chapter 3 emphasizes on dc micro-grid stability under high penetration of TR CIL to the common dc-link. A VSR is considered as the interfacing PE converter between the augmented dc micro-grid CILs and the ac system. It has been shown that TR PE converters are induced to operate at CP mode. Different examples for CILs are provided such as dc-dc converters and PMSM motor drive. In both applications, the output variables (such as output dc voltage or motor speed) are tightly-regulated by the converter controllers. Therefore, incremental negative input admittance appears at the low frequency region reducing the overall stability margin. If the common dc bus in a dc micro-grid is highly penetrated by such types of loads, the system stability is degraded. The evaluation process in this chapter depends on obtaining the linearized small signal source admittance of the VSR interface and the augmented model of the CILs; which is a negative resistance in the whole frequency region as a worst loading

condition. Proposed active compensators that are fed by the common dc-link voltage as an input signal and applied through a compensator function are provided. Three nodes in the VSR control structure are used for compensation signal injection; namely they are: outer, intermediate and inner nodes. As result, different dynamic characteristics and damping capabilities are yielded with each compensator. The design approach of each compensator is provided based on root-locus analysis and Bode plots. The proposed active damping techniques can preserve the dc micro-grid stability and improve the load performance by mitigating dynamic interactions and improves the disturbance rejection.

Chapter 4 evaluates the ac micro-grid stability under high penetration of CILs and PE converters. Two approaches are considered in this chapter to actively satisfy the Nyquist criterion; using active compensation from the load-side (LSC) so that they can be seamlessly integrated to the common ac-bus, or using active compensation from the ac micro-grid VSI (SSC) with load-independent dynamics. With the first approach, a VSR is considered as the common CIL that is supplied from the ac micro-grid interface (VSI). Based on input (VSR) and output (VSI) admittance-based analysis, the Nyquist criterion can be violated. Therefore, LSC is proposed to reshape the input ac admittance of the VSR to maintain the stability criterion. The compensator function has BP characteristics which provide three degree of freedoms to reshape the input admittance of the VSR around a certain frequency region (mid-frequencies). Moreover, the high-frequency resonant peak of the LCL ac filter of the VSR is actively damped using another active damper to mimic a resistance in series with the ac capacitor of the LCL filter. Both mid- and high-frequency compensators are employed together providing high reshaping capabilities of the VSR so that it can be directly plugged to ac micro-grids. The second approach in this Chapter is to consider a generic CIL model (negative resistance) that is supplied from the common ac-bus of the VSI. A proposed compensator from the VSI side (SSC) is provided with load-independent characteristics to virtually reshape the source admittance of the interfacing VSI to meet Nyquist criterion. The SSC injects the compensator signal to three different nodes in the VSI control structure. As result, three compensators are yielded; RLV, RIC and RIV. Each of them has unique dynamic behavior and damping capabilities according to

its ability to map the lightly damped modes of the uncompensated system to the closed loop system.

Chapter 5 analyze the interaction dynamic problem in hybrid grids that combine both ac and dc converter-dominated systems. The studied system consists of a dc DG park that interfaces different DG units to a common dc-bus from which ac and dc micro-grid are supplied. Using admittance-based analysis from the common dc-bus, the dc-side source admittance of the DG park and the load admittance of the ac and dc micro-grids are obtained under different operating modes and control functions, such as grid-connected (weak and stiff) and isolated micro-grids with dispatchable and non-dispatchable DG units. Analytical studies shows the VSIs are reflected to the common dc-bus as an incremental negative admittance based on the mode of operation and the system configurations. Simple and effective active compensators solutions are proposed to actively reshape the incremental input admittance of the VSI interfaced entities to satisfy the Nyquist criterion for the overall hybrid grid.

6.2 Future Work

The following research avenues can be followed in continuation of this line of work:

- Employing multi-frequency based active compensators to allow input/output admittance reshaping in multi-frequency bands. More than one active compensator, each with specific operating frequency and gain, can be used simultaneously to satisfy Nyquist criterion at different frequencies. This technique is beneficial when the PE converter is interfaced to multi-resonant system with different filtering topologies.
- Emphasis on active reshaping of input admittances of different types of loads such as induction motors or PMSM drives to provide seamless integration to the ac or dc micro-grids with plug-and-play features.
- Employing Nyquist criterion to other types of PE converters such as Matrix or Z-source converters to investigate their admittance reshaping capabilities.
- Development of equivalent input or output admittances of PE converters using other modeling techniques such as harmonic linearization methods.
- Investigation of nonlinear tools and large-signal stability analysis to provide active compensators with global stability.

Bibliography

[1] E. M. Lightner, and S. E. Widergren, "An orderly transition to a transformed electricity systems," *IEEE Trans. on Smart Grid*, vol. 1, no. 1, pp. 3-10, June 2010.

[2] J. M. Guerrero, J. C. Vasquez, J. Matas, L. Vicuna and M. Castilla, "Hierarchical control of droop-controlled ac and dc microgrids – a general approach toward standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158 – 172, Jan. 2011

[3] Z. Jiang and R. A. Dougal, "Hierarchical microgrid paradigm for integration of distributed energy resources," in *Proc. 2008 IEEE PES General Meeting*, pp. 1 – 8.

[4] J. Lee, B. Han and N. Choi, "Dc micro-grid operational analysis with detailed simulation model for distributed generation," in *Proc. 2010 IEEE ECCE Conf.,* pp. 3153-3160.

[5] K. Kurohane, T. Senjyu, Y. Yonaha, A. Yona, T. Funabashi, and C. H. Kim, "A distributed dc power system in an isolated island," in *Proc.2009 IEEE ISIE*, pp. 1–6.

[6] H. Kakigano, Y. Miura, T. Ise and R. Uchida, "Dc micro-grid for super high quality distribution — System configuration and control of distributed generations and energy storage devices," in *Proc. 2006 IEEE PESC Conf.,* pp. 1-7.

[7] H. Kakigano, Y. Miura and T. Ise, "Configuration and control of a dc microgrid for residential houses," in *Proc*. 2009 *Transmission & Distribution Conference & Exposition*, pp. 1-4.

[8] C. Jin, P. C. Loh, P. Wang, Y. Mi and F. Blaabjerg, "Autonomous operation of hybrid ac-dc microgrids," in *Proc. 2010 ICSET Int. Conf.*, pp. 1 – 7.

[9] P. C. Loh and F. Blaabjerg, "Autonomous operation of hybrid microgrid with ac and dc sub-grids," in *Proc. 2011 EPE Euro. Conf.*, pp. 1 – 10.

[10] H. Farhangi, "The path of the smart grid", *Power and Energy Magazine, IEEE*, vol. 8, no. 1, pp. 18-28, 2010.

[11] M. Hankaniemi, T. Suntio, M. Sippola and E. Oyj, "Load-impedance based interactions in regulated converters," in *Proc. 2005 INTELEC Int. Conf.*, pp. 569 – 573.

[12] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan and B. Fahimi, "Analysis and control of a buck dc-dc converter operating with constant power load in sea and undersea vehicles," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 559 –572, Mar./Apr. 2006.

[13] *IEEE Recommended Practice for Electronic Power Subsystems*, IEEE Standard 1573-2003, 2004.

[14] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc.* 1976 *IEEE IASAM Conf.*, pp. 366-382.

[15] J. M. Zhang, X. G. Xie, D. Z. Jiao and Z. Qian, "Stability problems and input impedance improvement for cascaded power electronic systems," in *Proc. 2004 IEEE APEC Conf.*, vol. 2, pp. 1018 – 1024.

[16] M. Hankaniemi, M. Karppanen and T. Suntio, "Load imposed instability and performance degradation in a regulated converter," *IET Trans. Power Appl.*, vol. 153, no. 6, pp. 781 – 786, Nov. 2006.

[17] X. Feng, J. Liu and F. C. Lee, “Impedance specifications for stable dc distributed power systems,” *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 157 – 162, Mar. 2002.

[18] S.D. Sudhoff, S.F. Glover, P.T. Lamm, D.H. Schmucker and D.E. Delisle, "Admittance space stability analysis of power electronic systems," *IEEE Trans. Aerospace and Electron. Sys.,* vol. 36, no. 3, pp. 965-973, 2000.

[19] J. Sun, “Impedance-based stability criterion for grid-connected inverters,” *IEEE Trans. Power Electron.*, in press [Available Online, Digital Object Identifier: 10.1109/TPEL.2011.2136439].

[20] A. Bin Jusoh, "The instability effect of constant power loads," in *Proc. 2004 National Power & Energy Conf.*, pp. 175-179.

[21] A. Emadi, A. Khaligh, C. H. Rivetta and G. Williamson, “Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives,” *IEEE Trans. Veh. Technol.*, vol. 55, no. 4, pp. 1112 – 1125, Jul. 2006.

[22] K. Ogata, *Modern control engineering*, New Jersey: Prentice Hall, 2002.

[23] Matlab/Simulink User Manual, The MathWorks Inc. [Online]. Available: http://www.mathworks.com

[24] J. A. Rosero, J. A. Ortega, E. Aldabas and L. Romeral, “Moving towards a more electric aircraft,” *Aerospace and Electronic Systems magazine, IEEE*, vol. 22, no. 3, pp. 3 – 9, 2007.

[25] A. Garcia, J. Cusido, J. A. Rosero, J. A. Ortega and L. Romeral, “Reliable electro-mechanical actuators in aircraft,” *Aerospace and Electronic Systems magazine, IEEE*, vol. 23, no. 8, pp. 19 – 25, 2008.

[26] J. Huang, K. A. Corzine and M. Belkhayat, “Small-signal impedance measurement of power-electronics-based ac power systems using line-to-line current injection,” *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 445 – 455, Feb. 2009.

[27] V. Valdivia, A. Lazaro, A. Barrado, P. Zumel, C. Fernandez and M. Sanz, “Black-box modeling of three-phase voltage source inverters for system-level analysis,” *IEEE Trans. Ind. Electron.*, in press [Available Online, Digital Object Identifier: 10.1109/TIE.2011.2167730].

[28] V. Valdivia, A. Barrado, A. Lazaro, P. Zumel, C. Raga and C. Fernandez, “Simple modeling and identification procedures for black-box behavioral modeling of power converters based on transient response analysis,” *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2776 – 2790, Dec. 2009.

[29] B. Miao, R. Zane and D. Maksimovic, “System identification of power converters with digital control through cross-correlation methods,” *IEEE Trans. Power Del.*, vol. 20, no. 5, pp. 1093 – 1099, Sep. 2005.

[30] J. Sun, “Small-signal methods for ac distributed power systems – a review,” *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2545 – 2554, Nov. 2009.

[31] P. T. Krein, J. Bentsman, R. M. Bass, and B. C. Lesieutre, “On the use of averaging for the analysis of power electronic systems,” *IEEE Trans. Power Electron.*, vol. 5, no. 4, pp. 182–190, Apr. 1990.

[32] A. Emadi, “Modeling and analysis of multiconverter dc power electronic systems using the generalized state-space averaging method,” *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 661 – 668, Jun. 2004.

[33] A. Emadi, “Modeling of power electronic loads in ac distribution systems using the generalized state-space averaging method,” *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 992 – 1000, Oct. 2004.

[34] M. Ilic and J. Zaborszky, *Dynamics and Control of Large Electric Power Systems*. New York: Wiley, 2000.

[35] P. Pillay and R. Krishnan, "Modeling, simulation, and analysis of permanent-magnet motor drives. I. the permanent-magnet synchronous motor drive," *IEEE Tran. Ind. Applicat.,* vol.25, no.2, pp.265-273, Mar/Apr 1989.

[36] *Electric Power Systems and Equipment—Voltage Ratings (60 Hertz)*, ANSI Standard Publication no. ANSI C84.1-1995.

[37] J. Sun and K. J. Karimi, “Small signal input impedance modeling of line-frequency rectifiers,” *IEEE Trans. Aerosp. Electron. Syst.*, vol. 44, no. 4, pp. 1489-1497, Oct. 2008.

[38] Z. Bing, K. J. Karimi, and J. Sun, “Input impedance modeling and analysis of line-commutated rectifiers,” *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2338-2346, Oct. 2009.

[39] J. Sun, J. Colon and K. J. Karimi, “Input impedance modeling of line-frequency rectifiers by the method of impedance mapping,” in *Proc. 2006 IEEE COMPEL,* pp. 69-75.

[40] F. Blaabjerg, R. Teodorescu, M. Liserre and A. V. Timbus, “Overview of control and grid synchronization for distributed power generation systems,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1398 – 1409, Oct. 2006.

[41] M. Mohr, W. T. Franke, B. Witting and F. W. Fuchs, “ Converter systems for fuel cells in the medium power range – a comparative study,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2024 – 2032, Jun. 2010.

[42] B. Kroposki, C. Pink, R. DeBlasio, H. Thomas, M. Simoes and P. K. Sen, “Benefits of power electronic interfaces for distribution energy systems,” *IEEE Trans. Energy Conv.*, vol. 25, no. 3, pp. 901-908, Sep. 2010.

[43] R. Teodorescu, M. Liserre and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*, Wiley-IEEE Press, 2011.

[44] M. Nehrir and C. Wang, *Modeling and Control of Fuel Cells: Distributed Generation Applications*, Wiley-IEEE Press, 2009.

[45] F. Katiraei, R. Iravani, N. Hatziargyriou and A. Dimeas, "Microgrids management," *Power and Energy Magazine, IEEE*, vol. 6, no. 3, pp. 54-65, 2008.

[46] F. Blaabjerg, Z. Chen and S. B. Kjaer, “Power electronics as efficient interface in dispersed power generation systems,” *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184 – 1194, Sep. 2004.

[47] P. Curtis, *Maintaining Mission Critical Systems in a 24/7 Environment*, Wiley-IEEE Press, 2007.

[48] J. M. Guerrero, L. Hang and J. Uceda, “Control of distributed uninterruptible power supply systems,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2845 –2859, Aug. 2008.

[49] ECPE European Center for Power Electronic, Strategic Research Agenda on Intelligent Power Electronics for Energy Efficiency, January 2008.

[50] D. Boroyevich, I. Cvetkovic, D. Dong, R. Burgos, F. Wang and F. Lee, "Future electronic power distribution systems – a contemplative view," in *Proc. 2010 12th OPTIM Int. Conf.*, pp. 1369-1380.

[51] A. Emadi, Y. J. Lee and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237 – 2245, Jun. 2008.

[52] Hydro-Québec, Strategic Plan, 2009 – 2013. Available online at http://www.hydroquebec.com/publications/en/strategic_plan/pdf/plan-strategique-2009-2013.pdf

[53] P. Mitra, G. K. Venayagamoorthy and K. A. Corzine, "Smartpark as a virtual STATCOM," *IEEE Trans. Smart Grid*, vol. 2, no. 3, pp. 445 – 455, Sep. 2011.

[54] B. Singh, R. Saha, A. Chandra and K. Al-Haddad, "Static synchronous compensators (STATCOM): a review," *IET Trans. Power Electron.*, vol. 2, no. 4, pp. 297 – 324, 2009.

[55] A. Ipakchi and F. Albuyeh, "Grid of the future," *IEEE Power Energy Mag.*, vol. 7, no. 2, pp. 52–62, Mar.–Apr. 2009.

[56] W. Xu and W. Wang, "Power electronic signaling technology – a new class of power electronics applications," *IEEE Trans. Smart Grid*, vo. 1, no. 3, pp. 332 – 339, Dec. 2010.

[57] F. Blaabjerg, A. Consoli, J. A. Ferreira and J. D. van Wyk, "The future of electronic power processing and conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 715 – 720, May 2005.

[58] S. Araujo and P. Zacharias, "Analysis on the potential of silicon carbide MOSFETs and other innovative semiconductor technologies in the photovoltaic branch," in *Proc. 2009 Int. Power Electron. Conf.*, pp. 1 – 10.

[59] S. Cole and R. Belmans, "Transmission of bulk power", *Industrial Electronics Magazine, IEEE*, vol. 3, no. 3, pp. 19-24, 2009.

[60] P. Bresesti, W. Kling, R. Hendriks and R. Vailati, "HVDC connection of offshore wind farms to the transmission system," *IEEE Trans. Energy Conv.*, vol. 22, no. 1, pp. 37 -43, Mar. 2007.

[61] S. M. Muyeen, R. Takahashi and J. Tamura, "Operation and control of HVDC-connected offshore wind farm," *IEEE Trans. Sustain. Energy*, vol. 1, no. 1, pp. 30 –37, Apr. 2010.

[62] J. Liang, T. Jing, O. G.-Bellmunt, J. Ekanayake and N. Jenkins, "Operation and control of multiterminal HVDC transmission for offshore wind farms," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2596 – 2604, 2011.

[63] M. M. Fouda, Z. Md. Fadlullah, N. Kato, R. Lu and X. Shen, "A lightweight message authentication scheme for smart grid communications," *IEEE Trans. Smart Grid*, in press [Available Online, Data Object Identifier: 10.1109/TSG.2011.2160661].

[64] P. Lindman and L. Thorsell, "Applying distributed power modules in telecom systems," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 365 – 373, Mar. 1996.

[65] M. Baran and N. Mahajan, "Dc distribution for industrial systems: opportunities and challenges," *IEEE Trans. Ind. Appl.*, vol. 39, no. 6, pp. 1596 – 1601, 2003.

[66] A. Kwasinski and P. Krein, "A microgrid-based telecom power system using modular multiple-input dc-dc converters," in *Proc. 2005 IEEE Telecom. Int. Conf.*, vol. 2, pp. 515-520.

[67] D. Salomonsson and A. Sannino, “Low-voltage dc distribution system for commercial power systems with sensitive electronic loads,” *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1620 – 1627, Jul. 2007.

[68] N. Idir, Y. Weens and J.-J. Franchaud, “Skin effect and dielectric loss models of power cables,” *IEEE Trans. Dielect. and Elect. Ins.*, vol. 16, no. 1, pp. 147 – 154, Feb. 2009.

[69] M. Saeedifard, M. Graovac, R.F. Dias and R. Iravani, “Dc power systems: challenges and opportunities,” in *Proc. 2010 PES General Meeting*, pp. 1 – 7.

[70] P. Karlsson and J. Svensson, “Dc bus voltage control for a distributed power system,” *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1405 – 1412, Nov. 2003.

[71] D. Salomonsson, L. Soder and A. Sannino, “Protection of low-voltage dc microgrids,” *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1045 – 1053, Jul. 2009.

[72] P. Anderson, *Power System Protection*, Wiley-IEEE Press, 1999.

[73] G. Gregory, “Applying low-voltage circuit breakers in direct current systems,” *IEEE Trans. Ind. Appl.*, vol. 31, no. 4, pp. 650 – 657, 1995.

[74] J. Lago and M. L. Heldwein, “Operation and control oriented modeling of a power converter for current balancing and stability improvement of dc active distribution networks,” *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 877 –885, Mar. 2011.

[75] W. Jiang and Y. Zhang, “Load sharing techniques in hybrid power systems for dc micro-grids,” in *Proc. 2011 APPEEC Conf.*, pp. 1 – 4.

[76] L. Xu and D. Chen, “Control and operation of a dc microgrid with variable generation and energy storage,” *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2513 – 2522, Oct. 2011.

[77] A. M. Rahimi and A. Emadi, “An analytical investigation of dc/dc power electronic converters with constant power load”, *IEEE Trans. Veh. Technol.,* vol. 58, no. 6, pp. 2689-2702, Jul. 2009.

[78] M. Cespedes, L. Xing and J. Sun, “Constant-power-load system stabilization by passive damping,” *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1832 – 1836, Jul. 2011.

[79] M. Cespedes, T. Beechner, L. Xing and J. Sun, “Stabilization of constant-power-load by passive impedance damping,” in *Proc. 2010 IEEE APEC Conf.*, pp. 2174 – 2180.

[80] K. Pietilainen, L. Harnefors, A. Petersson and H.-. Nee, "DC-link stabilization and voltage sag ride-through of inverter drives," *IEEE Trans. Ind. Electron.,* vol. 53, no. 4, pp. 1261-1268, 2006.

[81] A. Kwasinski, C. Onwuchekwa, "Dynamic behavior and stabilization of dc micro-grids with instantaneous constant-power loads," *IEEE Trans. Power Electron.,* vol. 26, no. 3, pp. 822-834, Mar. 2011.

[82] A.M. Rahimi and A. Emadi, "Active damping in dc/dc power electronic converters – A novel method to overcome the problems of constant power loads," *IEEE Trans. Ind. Electron.,* vol. 56, no. 5, pp. 1428-1439, 2009.

[83] J. Wang and D. Hower, “A power shaping stabilizing control strategy for dc power systems with constant power loads,” *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2982 – 2989, Nov. 2008.

[84] A. Khaliph, S. S. Williamson and A. Emadi, “Control and stabilization of dc-dc buck-boost converters loaded by constant power loads in vehicular systems using a novel digital scheme,” in *Proc. 2006 EPE-PEMC Int. Conf.*, pp. 1769 – 1775.

[85] P. Liutanakul, A.-B. Awan, S. Pierfederici, B. Nahid-Mobarakeh, and F. Meibody-Tabar, "Linear Stabilization of a DC Bus Supplying a Constant Power Load: A General Design Approach," *IEEE Trans. Power Electron.,* vol.25, no.2, pp.475-488, Feb. 2010.

[86] P. Liutanakul, S. Pierfederici, A. Bilal, B. Nahid-Mobarakeh, and F. Meibody Tabar, "Stability investigation of inverter motor drive system with input filter — Optimisation of the DC-link capacitance value," in *Proc. 2008 IEEE Power Electron. Specialists Conf.*, pp.3728-3734.

[87] L. Xinyun; N. Fournier; and A. J. Forsyth, "Active stabilisation of an HVDC distribution system with multiple constant power loads," in *Proc. 2008 IEEE Vehicle Power and Propulsion Conf.*, pp.1-6.

[88] L. Xinyun and A. J. Forsyth, "Active stabilisation of a PMSM drive system for aerospace applications," in *Proc. 2008 IEEE Power Electronics Specialists Conf.*, pp.283-289.

[89] L. Xinyun; A. J. Forsyth, and A. M. Cross, "Negative input-resistance compensator for a constant power load," *IEEE Trans. Ind. Electron.*, vol.54, no.6, pp.3188-3196, Dec. 2007.

[90] K. Pietilainen, L. Harnefors, and H.-P. Nee, “DC-link stabilization and voltage sag ride-through of inverter drives,” *IEEE Trans. Ind. Electron*., vol. 53, no, 4, pp. 1261 – 1268, 2006.

[91] X. Y. Liu and A. J. Forsyth, "Comparative study of stabilizing controllers for brushless DC motor drive systems," in *Proc. IEEE 2005 International Conf. on Electric Machines and Drives*, pp.1725-1731.

[92] A. M. Cross and A. J. Forsyth, "Small-signal input admittance characteristics of a brushless DC motor drive," *4th 2008 IET PEMD Conf.*, pp.520-526.

[93] H. Mosskull, J. Galic and B. Wahlberg, “ Stabilization of induction motor drives with poorly damped input filters,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2724-2734, Oct. 2007.

[94] A. M. Rahimi, G. A. Williamson, and A. Emadi, "Loop-cancellation technique: a novel nonlinear feedback to overcome the destabilizing effect of constant-power loads," *IEEE Trans. Veh. Technol.,* vol. 59, no. 2, pp. 650-661, Feb. 2010.

[95] X. Liu, Y. Zhou, W. Zhang and S. Ma, “Stability criteria for constant power loads with multi-stage LC filters,” *IEEE Trans. Veh. Technol.*, vol. 60, no. 5, pp. 2042 – 2049, Jun. 2011

[96] P. Magne, B. N.-Mobarakeh and S. Pierfederici, “General active global stabilization of multi-loads dc-power networks,” *IEEE Trans. Power Electron.*, in press [Available Online, Digital Object Identifier: 10.1109/TPEL.2011.2168426].

[97] W. Zhang, Y. Hou, X. Liu and Y. Zhou, “Switched control of three-phase voltage source PWM rectifier under a wide-range rapidly varying active load,” *IEEE Trans. Power Electron.,* in press [Available Online, Digital Object Identifier: 10.1109/TPEL.2010.2095507].

[98] E. A. A. Coelho, P. C. Cortizo and P. F. D. Garcia, “Small-signal stability for parallel-connected inverters in stand-alone ac supply systems,” *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 533 – 542, 2002.

[99] N. Pogaku, M. Prodanovic and T. C. Green, "Modeling, analysis and testing of autonomous operation of an inverter-based microgrid", *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 613 – 625, Mar. 2007.

[100] J. M. Guerrero, L. G. de Vicuna, J. Matas, M. Castilla and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems*," IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1205 – 1213, Sep. 2004.

[101] J. M. Guerrero, L. G. de Vicuna, J. Matas, M. Castilla and J. Miret, "Output impedance design of parallel-connected ups inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126 – 1135, Aug. 2005.

[102] J. M. Guerrero, J. Matas, L. G. de Vicuna, M. Castilla and J. Miret, "Wireless-control strategy for parallel operation of distribution-generation inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1461 – 1470, Oct. 2006.

[103] J. M. Guerrero, J. Matas, L. G. de Vicuna, M. Castilla and J. Miret, "Decentralized control for parallel operation of distributed generation inverters using resistive output impedance*," IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 994 – 1004, Apr. 2007.

[104] W. Yao, M. Chen, J. Matas, J. M. Guerrero and Z.-M. Qian, "Design and analysis of the droop control methid for parallel inverters considering the impact of the complex impedance on the power sharing," *IEEE Trans. Ind. Electron.*, vol. 85, no. 2, pp. 576 – 588, Feb. 2011.

[105] Y. A.-R. I. Mohamed and E. F. El-Saadany, "Adaptive decentralized droop controller to preserve power sharing stability of parallel inverters in distributed generation microgrids," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2806 – 2816, 2008.

[106] E. Barklund, N. Pogaku, M. Prodanovic, C. H.-Aramburo and T. C. Green, "Energy management in autonomous microgrids using stability-constrained droop control of inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2346 – 2352, Sep. 2008.

[107] W. Jiang and B. Fahimi, "Multi-port power electronic interface: concept, modeling and design," *IEEE Trans. Power Electron*., vol. 26, no. 7, pp. 1890 – 1900, Jul. 2011.

[108] S. V. Iyer, M. N. Belur and M. C. Chandorkar, "A generalized computational method to determine stability of a multi-inverter microgrid," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2420-2432, Sep. 2010.

[109] L. Harnefors, M. Bongiorno and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3323-3334, Dec. 2007.

[110] E. Twining and D. G. Homes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.*, Vol. 18, no. 3, pp. 888-895, May 2003.

[111] Y. A.-R. I. Mohamed, "Mitigation of dynamic, unbalanced and harmonic voltage disturbances using grid-connected inverters with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3914 – 3924, Sep. 2011.

[112] F. Wang, J. Duarte, M. A. M. Hendrix and P. F. Ribeiro, "Modeling and analysis of grid harmonic distortion impact of aggregated DG inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 786-797, Mar. 2011.

[113] L. Harnefors, "Analysis of subsynchronous torsional interaction with power electronic converters," *IEEE Trans. Power Sys.*, vol. 22, no. 1, pp. 305-313, Feb. 2007.

[114] D. P. Ariyasinghe and D. M. Vilathgamuwa, “Stability analysis of microgrids with constant power loads,” in *Proc. 2008 IEEE ICEST Conf.*, pp. 279-284.

[115] K. Kurohane, T. Senjyu, A. Yona, N. Urasaki, T. Goya and T. Funabashi, “A hybrid smart ac/dc power system,” *IEEE Trans. Smart Grid*, vol. 1, no. 2, pp. 199 – 204, Sep. 2010.

[116] X. Liu, P. Wang and P. C. Loh, “A hybrid ac/dc microgrid and its coordination control,” *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 278-286, June 2011.

[117] V. Blasko and V. Kaura, "A new mathematical model and control of a three-phase ac-dc voltage source converter," *IEEE Trans. Power Electron.,* vol. 12, no. 1, pp. 116-123, 1997.

[118] J. Doval-Gandoy and C.M. Penalver, "Dynamic and steady state analysis of a three phase buck rectifier," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 953-959, 2000.

[119] K.-N. Areerak, S.V. Bozhko, G.M. Asher and D.W.P. Thomas, "DQ-transformation approach for modelling and stability analysis of ac-dc power system with controlled PWM rectifier and constant power loads," in *Proc. 2008 EPE-PEMC*, pp. 2049-2054.

[120] Wei Ke-xin and Wang Shui-ming, "Modeling and Simulation of Three-Phase Voltage Source PWM Rectifier," in *Proc. 2008 ICACTE Int. Conf.*, pp. 982-986.

[121] P. Verdelho and G.D. Marques, "DC voltage control and stability analysis of PWM-voltage-type reversible rectifiers," *IEEE Trans. Ind. Electron.*, vol. 45, no. 2, pp. 263-273, 1998.

[122] M. Liserre, F. Blaabjerg and S. Hansen, “Design and control of an LCL-filter-based three-phase active rectifier,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281 – 1291, Sep./Oct. 2005.

[123] M. Liserre, A. D. Aquila and F. Blaabjerg, “Genetic algorithm-based design of the active damping for an LCL-filter three-phase active rectifier,” *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 76 – 86, Jan. 2004.

[124] J. Yang, J. E. Fletcher and J. O’Reilly, “Short-circuit and ground fault analysis and location in VSC-based DC network cables,” *IEEE Trans. Ind. Electron.*, in press [Available Online, Digital Object Identifier: 10.1109/TIE.2011.2162712].

[125] A. Yazdani and R. Iravani, *Voltage-sourced converters in power systems: Modeling, control, and applications*, New Jersey: John Wiley & Sons, 2010.

[126] A. Yazdani and P. P. Dash, “A control methodology and characterization of dynamics for a photovoltaic (PV) system interfaced with a distribution network*,” IEEE Trans. Power Delivery*, vol. 24, no. 3, pp. 1538-1551, July 2009.

[127] A. A. Salam, M. A. Hannan, A. Mohamed and H. Shareef, “A 50KW PEM fuel cell inverter-based distributed generation system for grid connected and islanding operation,” *in Proc. 2009 IEEE TENCON Conf.*, pp. 1-5.

[128] A. Elmitwally and M. Rashed, “Flexible operation strategy for an isolated PV-diesel microgrid without energy storage,” *IEEE Trans. Energy conver.*, vol. 26, no. 1, pp. 235-244, Mar. 2011.

[129] H. Fujita and H. Akagi, “Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system,” IEEE Trans. Power Electron., vol. 22, no. 3, pp. 1046 – 1053, May 2007.

[130] K. J. Åström and T. Hägglund*, PID Controllers Theory: Design and Tuning*. Research Triangle Park, NC: Instrument Society of America, 1995.

[131] W. Zhao and G. Chen, "Comparison of active and passive damping methods for application in high power active power filter with LCL-filter," *in Proc. 2009 IEEE SUPERGEN Int. Conf.*, pp. 1-6.

[132] M. Liserre, A. D. Aquila and F. Blaabjerg, "Generic algorithm-based design of the active damping of an LCL-filter three-phase active rectifier," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 76-86, Jan. 2004.

[133] E. Figueres, G. Garcera, J. Sandia, F. G.-Espin and J. C. Rubio, "Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter," *IEEE. Trans. Ind. Electron.*, vol. 56, no. 3, pp. 706-717, Mar. 2009.

Appendix A3.1

PMSM Drive Modeling as Shown in Figure 3.2

The model of the PMSM drive system is given below.

- **PMSM Model**

$$V_{md} = (R_m + sL_m)I_{md} - L_m n_p \omega_r I_{mq} \quad \text{(A3.1)}$$

$$V_{mq} = (R_m + sL_m)I_{mq} + (\psi + L_m I_{md}) n_p \omega_r \quad \text{(A3.2)}$$

$$T_e(s) = \frac{3}{2} n_p \psi I_{mq} \quad \text{(A3.3)}$$

$$sJ\omega_r = T_e(s) - T_{Load} \quad \text{(A3.4)}$$

- **Input DC Filter Model**

$$V_{dc} = \left(R_f + sL_f\right)I_L + V_c \quad \text{(A3.5)}$$

$$I_L = sC_f V_c + I_{load} \quad \text{(A3.6)}$$

- **Controller loops**

$$(\omega_* - \omega_r)G_\omega(s) = I_q^* \quad \text{(A3.7)}$$

$$(I_d^* - I_d)\left(K_{mp} + \frac{K_{mi}}{s}\right) - L_m n_p \omega_r I_{mq} = V_d^* \quad \text{(A3.8)}$$

$$\left(I_q^* - I_q\right)\left(K_{mp} + \frac{K_{mi}}{s}\right) + (\psi + L_m I_{md}) n_p \omega_r = V_q^* \quad \text{(A3.9)}$$

where ω_*, I_d^* and I_q^* are the reference values of the motor speed and *d-q* component of the motor current, respectively; V_d^* and V_q^* are the reference *d-q* voltages generated by the current controller $\left(G_I(s) = K_{mp} + \frac{K_{mi}}{s}\right)$ to determine the inverter duty cycle; $G_\omega(s)$ is the speed controller and s is the Laplace operator. I_d^* is set to zero for constant air-gap flux mode.

- **System Parameters**

$R_m = 0.5\,\Omega$, $L_m = 3.1mH$, $n_p = 4$, $\omega_r = 157\,rad/sec$, $\psi = 0.124\,V.\mathrm{s}$,
$J = 3.1 \times 10^{-3} Kg.m2$, $K_{mp} = 2000$, $K_{mi} = 5000$.

Appendix A3.2

DC-DC Buck Converter Model as Shown in Figure 3.3

- **System Model**

  Using average modeling method, the model of dc-dc buck converter that operates in CCM is given by:

$$dV_{dc} - V_c' = I_L'\left(R_f' + sL_f'\right) \quad \text{(A3.10)}$$

$$sC_f'V_c' = I_L' - I_{load}' \quad \text{(A3.11)}$$

  where d is the converter duty ratio to control the input dc voltage (V_{dc}).

- **System Parameters**

  $V_{dc} = 200V$, $R_f' = 0.01\ \Omega$, $L_f' = 100\mu H$

Appendix A3.3

AC-DC Converter Parameters for the System in Figure 3.15

Three phase, $120Vac/200Vdc, 12kW, 60\ Hz$

- **Input/output filter**

  $R = 0.1\Omega$, $L = 0.1\ mH$, $C = 2000$ μF

- **Voltage and current controller**

  $K_{vp} = 0.136$, $K_{vi} = 7.294$, $K_{ip} = 0.6283$, $K_{ii} = 628.32$.

  $V_{dc}^{ref} = 200$V, $I_q^{ref} = 0$

- **Active compensators**

  Outer Loop compensator: $R_v = 1 \rightarrow 15$, $\omega_c = 300\ rad/sec$.

  Intermediate Loop compensator: $Y_v = 0.01 \rightarrow 0.2$, $\omega_Y = 300\ rad/sec$.

  Inner Loop compensator: $K_v = 0.1 \rightarrow 2.4$, $\omega_K = 30\ rad/sec$.

Appendix A4.1

DC-AC Converter Parameters for the System in Figure 4.2

Three phase, $120Vac/400Vdc, 20kVA, 60\ Hz$

- **Filter parameters**

  $R_f = 0.15, L_f = 1\ mH, C_f = 45\ \mu H$

- **AC voltage and current controller**

  $K_{vp} = 0.265, K_{vi} = 10, K_{ip} = 10.05, K_{ii} = 251.33, H = 0.7$

  $V_{od}^{ref} = 120\sqrt{2}\ V, V_{oq}^{ref} = 0$

- **Power Sharing Loop**

  $m = 0.8 \times 10^{-4}, n = 1 \times 10^{-3}, \omega_p = 30\ rad/sec$

Appendix A4.2

AC-DC Converter Parameters for the System in Figure 4.4

Three phase, $120Vac/200Vdc, 20kW, 60\ Hz$

- **Input/output filter of VSR**

  $R = 0.1, L = 0.1\ mH, C = 45\ \mu H, C_{dc} = 2000\ \mu H$

- **DC voltage and current controller**

  $G_{vdc}(s) = 2.2 + \frac{7.3}{s}, G_{ic}(s) = 0.6283 + \frac{628.32}{s}$

  $V_{dc}^{ref} = 200\text{V}, I_{cq}^{ref} = 0$

- **Distribution feeder**

  $R_l = 0.05, L_l = 0.7\ mH$

- **Output ac filter parameters of the source side**

  $R_f = 0.15, L_f = 1\ mH, C_f = 45\ \mu H$

Appendix A4.3

AC Micro-Grid Parameters Shown in Figure 4.11

- **VSI-1 (typically, VSI-2)**

  Ac voltage controller: $0.165 + 400/s$

  Current controller: $50 + 15300/s$

  Droop coefficients: $m = 1 \times 10^{-6}$, $n = 1 \times 10^{-3}$, $\omega_c = 30$

- **VSR-1**

  Dc voltage controller: $2 + 0.7294/s$

  Current controller: 0.5

  10 hp, 4 pole pairs, $R_{stator} = 0.5\ \Omega$, $L_{stator} = 3.1mH$; flux linkage = 0.124 *V*.s, inertia constant = 1.1 $mKg.m^2$; friction factor = 0.024 *N.m.s,* Mechanical Load = *25 N.m.*

  Speed controller: $K_p = 0.1$, $K_i = 2$.

  Current controller: $K_p = 50$, $K_i = 5000$.

- **VSR-2, VSR-3**

  Dc voltage controller: $2 + 0.7294/s$

  Current controller: 0.5

Appendix A4.4

AC Micro-Grid Parameters Shown in Figure 4.21

- **DG-1, 2 and 3**

  $K_{vp} =$ 0.165, $K_{vi} = 400$, $K_{ip} = 50$, $K_{ii} = 15300$, $H = 0.7$

- **CIL-1**

  208 V (L-L), 60 Hz

  8 hp, 4 pole pairs, $R_{stator} =$ 0.5 Ω, $L_{stator} =$ $3.1mH$; flux linkage = 0.124 *V*.s, inertia constant = 1.1 $mKg.m^2$; friction factor = 0.024 *N.m.s*

  Speed controller: $K_p = 0.1$, $K_i = 2$.

  Current controller: $K_p = 50$, $K_i = 5000$.

- **CIL-2, 3 and 4**

  208 V (L-L), 60 Hz;

  Voltage controller: $K_p = 2$, $K_i = 0.7294$.

  Current controller: $K_p = 0.5$, $K_i = 1$.

  Ac filter: L = 100 μH, R = 0.1 Ω;

Appendix A5.1

System Parameters for VSIs Shown in Figure 5.5

Three phase, $120Vac/400Vdc, 20kVA, 60\ Hz$

- **RLC Parameters**

  $R_f = 50\ m\Omega,\ L_f = 2mH,\ C_f = 45\mu F$

  $R_{dc} = 5\ m\Omega,\ L_{dc} = 250\ \mu H,\ C_{dc} = 4.7\ mF$

  $L_g = 0.5\ mH$

- **AC Current Controller**

  $K_p^i = 10.05, K_i^i = 251.33$

- **AC Voltage Controller**

  $K_p^{vac} = 0.265, K_i^{vac} = 10$

- **DC Voltage Controller**

  $K_p^{vdc} = 0.0015, K_i^{vdc} = 0.07$

- **Active Power Controller**

  $K_p^p = 0.002, K_i^p = 0.07, \omega_p = 30$

Appendix A5.2

Designed Parameters for the Proposed Compensators Shown in Figure 5.22

- **AC Micro-grid Interface**

  Outer Loop Compensator $(C_{4o}(s))$: $K_{4o} = 0.25, \omega_{4o} = 700, \xi_{4o} = 1$

  Intermediate Loop Compensator $(C_{4m}(s))$: $K_{4m} = 0.065, \omega_{4m} = 600, \xi_{4m} = 1$

  Inner Loop Compensator $(C_{4i}(s))$: $K_{4i} = 0.65, \omega_{4i} = 600, \xi_{4i} = 1$

- **Grid-Connected Inverter**

  Outer Loop Compensator $(C_{2o}(s))$: $K_{2o} = 50, \omega_{2o} = 400, \xi_{2o} = 1$

  Intermediate Loop Compensator $(C_{2m}(s))$: $K_{2m} = 0.1, \omega_{2m} = 400, \xi_{2m} = 1$

  Inner Loop Compensator $(C_{2i}(s))$: $K_{2i} = 1, \omega_{2i} = 400, \xi_{4i} = 1$