University of Alberta

Low-Area Low-Power
Delta-Sigma Column and Pixel Sensors

by

Alireza Mahmoodi

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Integrated Circuits & Systems

Department of Electrical and Computer Engineering

Fall 2011
Edmonton, Alberta

To my dear parents,

Fatemeh and Ezzollah.

Abstract

Delta-sigma analog-to-digital converters (ADCs) are widely used in audio applications, but their use in video applications is emerging. By introducing novel decimator and modulator design flows, this thesis advances the state-of-the-art in delta-sigma data conversion and image sensing. As the approach concerns arrays of many ADCs, it is essential to minimize the layout area and power consumption of each ADC. For maximum scalability, each column or pixel must include a decimator. Conventional decimation, e.g., based on comb filters, is unsuitable for this purpose. Instead, finite-impulse response decimation may be realized efficiently in bit-serial fashion by generating optimal coefficients at the chip-level. As for the modulator, architectural choices and modeling approaches are taken to reduce both area and power while realizing specifications and tolerating mismatch. Very small capacitors suffice to achieve reasonable specifications. These design flows are used with 0.18 μm CMOS technology to fabricate specific designs. In a first chip with several data converters, column and pixel-level ADCs achieve figures of merit (150 and 137 dB) comparable to state-of-the-art delta-sigma ADCs, but with smaller modulator areas (1,850 and 627 μm^2). In a second chip with two image sensors, logarithmic pixels are combined with column and pixel-level ADCs to make digital video cameras. Both image sensors achieve peak signal-to-noise-and-distortion ratios (35 and 46 dB) comparable to the human eye and better than state-of-the-art logarithmic cameras. Although the present results are immediately useful, the approach is also suitable for low-voltage nanoscale CMOS processes, which would further reduce the layout area and power consumption.

Acknowledgements

This thesis would have been impossible without the support and encouragement of many people. First and foremost, I would like to thank my advisor, Dr. Dileepan Joseph, for his support and supervision. During the last five years, he taught me invaluable skills including digital signal processing, image sensors, circuit design, and communicating and presenting research results. His positive influence on my discipline and character is very obvious to me. His insight, enthusiasm, and encouragement made a huge impact on my studies and career path.

I would also like to thank Dr. Vincent Gaudet for being supportive all these years. Dr. Gaudet, and the other members of my examining committee, Dr. Bruce Cockburn, Dr. Kambiz Moez, Dr. Herbert Yang, and Dr. David Nairn, all provided me with very constructive feedback.

I am indebted to Dr. Mohammad Reza Yazdani for his help and support all these years. He showed me the way to Canada, a country enriched with wonderful people and full of opportunities. Without his support, it would have been impossible to start this journey.

My special gratitude goes to my friends in the Electronic Imaging Lab. Adam Harrison was always a valuable friend and helped me in so many ways. I really appreciate his help in proofreading parts of my thesis. Moreover, Adam's witty character and sense of humor created a very pleasant atmosphere in the lab. My other friend, Dr. Orit Skorka, was crucial in aiding my progress, as she shared her considerable knowledge, ranging from CAD tools to image sensor design. Dr. Kamal Ranaweera was also an invaluable source of knowledge, especially with C++ programming and FPGA design and interfacing. More than that, Kamal is a fantastic friend. Jing Li, who joined our lab at the end of my PhD, soon became an excellent lab mate. I appreciate his help in developing and programming the FPN correction algorithm. Cindy Wong was a great friend and I enjoyed our discussions on various occasions.

As a newcomer to Canada, my life in Edmonton was an adjustment and change from my life in Iran—but it was full of joyful moments, which I will never forget. I was exposed to new fun activities, sharing great times with my excellent friends. Big thanks go to all of them, especially Sama, Katy, Lukasz, Lee, Razhia, Behrooz, Akbar, Abraham, Aydin, and Khalil for sharing their wonderful moments with me.

Life in Edmonton made me discover my passion for music. Along with the pictures that are shown in Chapter 5, I included a short movie in my thesis seminar, which was made using the camera I designed as part of my project. This movie not only presents a technical achievement of this work, but it also includes a short guitar improvisation of mine. I think this movie perfectly sums up the skills and passions, both technical and musical, that I have developed during my time here in Edmonton. I believe both sets of skills will serve me well.

The work presented in this thesis was funded by the University of Alberta, the Natural Sciences and Engineering Research Council of Canada, and CMC Microsystems.

Lastly, I take this opportunity to express my profound appreciation to my family for all their love and encouragement. Thanks to my parents who raised me with an enthusiasm and passion to learn, and thanks to my sisters and brothers who have been always understanding and supportive in every aspect of my life. They mean the world to me.

Table of Contents

List of Figures

List of Tables

List of Symbols

List of Abbreviations

ADC	Analog-to-digital converter	1
CCD	Charge coupled device	4
CDF	Cumulative distribution function	69
CMFB	Common-mode feedback	41
CMOS	Complementary metal-oxide-semiconductor	1
CT	Continuous time	37
DAC	Digital-to-analog converter	18
DCS	Digital column sensor	77
DDA	Differential-difference amplifier	41
DNL	Differential nonlinearity	70
DPS	Digital pixel sensor	5
DR	Dynamic range	1
FIFO	First-in, first-out	57
FIR	Finite impulse response	21
FOM	Figure of merit	70
FPGA	Field-programmable gate array	57
FPN	Fixed pattern noise	2
GND	Ground voltage	29
IIR	Infinite impulse response	23
INL	Integral nonlinearity	70
LPF	Low-pass filter	16
LSB	Least significant bit	70
MIM	Metal insulator metal	47
OTA	Operational transconductance amplifier	37
PCB	Printed circuit board	56
PSD	Power spectral density	16
SC	Switched capacitor	37
SLR	Slew rate	37
SNDR	Signal-to-noise-and-distortion ratio	2
SNR	Signal-to-noise ratio	2
UGB	Unity gain bandwidth	37
USB	Universal serial bus	57
VI	Vertically integrated	107
VLSI	Very large scale integration	1
VDD	Voltage drain-to-drain	29

Chapter 1

Introduction

Oversampling analog-to-digital converters (ADCs) have become very popular in recent years for low-bandwidth applications because they can achieve high resolution without the need for precise analog components [1–6]. The delta-sigma ADC is the dominant form of oversampling ADCs. Invented in the 1950s, it was not widely used until the 1980s, when complementary metal-oxide-semiconductor (CMOS) technology became advanced enough to integrate the required digital signal processing circuits. Delta-sigma ADCs rely mainly on digital signal processing rather than precise analog circuits. On the other hand, Nyquist-rate ADCs are vulnerable to analog component imperfection. Therefore, delta-sigma ADCs are well suited for very large scale integration (VLSI) technology.

Delta-sigma ADCs are preferred for high resolution applications. Also, since the sampling frequency of delta-sigma ADCs is higher than the Nyquist rate by a factor of the oversampling ratio, this ADC is mostly used for low-speed applications. A well-known application that takes full advantage of the inherent qualities of delta-sigma ADCs is digital audio, which involves 14–20 bits of resolution [3].

As VLSI technology continues to advance, higher speed with smaller area is possible with CMOS technology, and new applications of delta-sigma ADCs for array sensors are emerging [7–14]. A variety of applications, such as visible-band imagers, X-ray sensors, biosensor arrays, and infrared cameras, demand high performance readout circuits. In fact, each application requires a certain specification. For example, in consumer cameras, the focus is more on bit resolution, pixel resolution, power consumption, and to a lesser extent on dynamic range (DR). X-ray imagers require high bit resolution and larger DR, but allow a larger pixel size. Thus, imagers need to be customized for their end application.

Smart focal plane processing has increasingly become a suitable solution to efficiently extract the information from an array. Column and pixel-parallel data conversion, in which the conversion is performed in each column or each pixel, are important elements of focal plane processing. As will be discussed, delta-sigma ADCs can fully realize the advantages of column

and pixel-level data conversion.

This thesis proposes a design methodology for delta-sigma ADC arrays. Column-level and pixel-level data conversion using delta-sigma ADCs will be evaluated stand-alone and using a visible-band logarithmic sensor. Although the focus of this work is on visible-band imagers, a similar method could be used for other applications.

1.1 Motivation for the Research

Different applications, e.g., photography, machine vision, automotive, and surveillance, call for image sensors with high DR and high signal-to-noise-and-distortion ratio (SNDR) [15–17]. Effective bit resolution in an image is determined by SNDR, which is limited by the signal-to-noise ratio (SNR) and fixed pattern noise (FPN). Hence, in the applied part of this thesis, the main focus is to enhance the SNDR of an image sensor. Unlike noise, distortion is the residual error in the signal that does not change with time. DR is defined as the ratio of the largest non-saturating signal to the smallest detectable signal. Also, a high frame rate and a large array size are required in some applications. Despite more than two decades of research, it is still not easy to achieve these requirements with CMOS image sensors at a low power consumption.

Natural scenes have a DR of more than 160 dB ranging from 10^{-3} cd/m^2 at night to 10^3 cd/m^2 in indoor scenes and up to 10^5 cd/m^2 in direct sunlight [18]. The human eye can capture over 100 dB of this range with roughly 40 dB SNDR in most of the range. The performance of the human eye is approximated by Weber's law, which says that an object can be distinguished from its surroundings if the contrast between them is about 1–10%. This means that the SNDR should be 40 dB to achieve 1% contrast sensitivity [19].

A high frame rate and array size is also demanded in various fields such as scientific measurements and motion analysis. The conventional chip-level data conversion approach puts constraints on readout speed, which limits the frame rate and array size. For example, ultra-high-definition video requires 33 megapixels at 240 fps, which implies a sampling rate of 8 GHz with chip-level data conversion [17].

CMOS image sensors can be categorized into three groups, namely linear sensors, logarithmic sensors, and other sensors. While standard linear CMOS sensors have almost 55 dB peak SNR, their DR is in the range 40–65 dB [15]. On the other hand, logarithmic sensors achieve a high DR of more than 100 dB, but various works show that these sensors have relatively a low peak SNR (PSNR) of 32 dB, which is less than the requirements of a camera with a performance comparable to the human eye [16, 20].

A variety of methods have been developed aiming for high performance image sensors [21–25]. A main motivation of this thesis is to present a new

architecture as a solution to improve the performance of CMOS image sensors. In this architecture, column or pixel-parallel delta-sigma data conversion is utilized to enhance the performance of logarithmic sensors.

1.1.1 Delta-Sigma Column and Pixel Sensors

Delta-sigma ADCs provide several advantages for parallel data conversion, which are not obtained using Nyquist-rate ADCs. These advantages, including higher SNR, flexibility of trading frame rate with bit resolution, and higher linearity, are discussed in this section.

In order to increase the SNR, the photodetector's output needs to be filtered before the sampling and readout. Based on the Nyquist theorem, in pixel-level data conversion, the bandwidth of the low-pass filter (LPF) should be half the frame rate in order to minimize the noise contribution to the signal. In column-level ADC, the filter bandwidth must be multiplied by the number of pixels in each column. Therefore, less noise is filtered and lower SNR is expected compared to the pixel-level data conversion method. With the chip-level architecture, filtering the temporal noise is not possible because the sampling is done at a very high rate and the analog output of each pixel needs to settle before sampling. The wire capacitance of the readout circuit both in column-level and chip-level acts as a low-pass filter, which would limit the readout speed.

Implementing a low-pass filter in each pixel is not practical because large capacitors are needed to provide a bandwidth equal to half the frame rate. Also, implementing a low-pass filter at the column level limits the readout speed. Using a delta-sigma ADC, this issue could be resolved. Unlike the Nyquist-rate ADCs, a delta-sigma ADC can low-pass filter the noise without employing a sharp analog filter before the ADC [3, 4, 26]. Using the delta-sigma ADC, the required bandwidth of the low-pass filter is increased by the oversampling ratio. This theory suggests that a delta-sigma ADC can fully realize the advantages of pixel-level or column-level data conversion.

Flexibility of trading frame rate with bit resolution is another advantage of delta-sigma ADCs. By decreasing the oversampling *ratio* in the ADC, the output SNR is decreased and the Nyquist rate is increased for a fixed oversampling *rate*. Therefore, a higher frame rate can be achieved at the cost of a lower SNR. This could be very useful in some applications.

Nonlinearity and temporal noise in the analog readout circuits are major constraints for achieving high SNDR in low-voltage CMOS image sensors [2]. As CMOS technology scales down to achieve higher speed and lower power consumption for digital circuits, analog circuits are becoming more nonlinear. Simultaneously, reductions in supply voltage are forcing a lower voltage range at the input of the ADC with respect to the temporal noise. These trends conspire, it seems, to lower the maximum-achievable SNDR. For example, as the power supply voltage reduces from 5 V to 1.8 V,

corresponding to changing the process from 0.5 μm to 0.18 μm, linear image sensors lose 8.8 dB of DR. But a properly designed ADC could improve both the SNDR and nonlinearity of the image sensor. In contrast to Nyquist-rate ADCs, delta-sigma ADCs use fewer analog components and rely more on digital circuits. Delta-sigma ADCs can achieve a high resolution in a low voltage range. This logic makes them an ideal choice for image sensors in low-voltage CMOS technology.

Delta-sigma ADCs are preferred for data conversion in column or pixel sensors. The main issue is the area usage and power consumption, which should both be minimized. This is more critical in pixel-level data conversion, where a limited area is available.

1.2 Data Conversion in Image Sensors

Data conversion in image sensors plays a critical role in determining the performance of the sensor in term of SNDR, DR, frame rate, etc. The design can be discussed in two aspects: level of data conversion and method of data conversion, which are discussed in the next sections.

1.2.1 Levels of Data Conversion

In modern CMOS image sensors, data conversion may be performed either at chip-level, column-level, or pixel-level. Each method has its own advantages and drawbacks. Data conversion may also be done off chip but this is uncommon today except for charge coupled device (CCD) image sensors, where it is the only possibility.

Chip-level data conversion uses one ADC for all of the pixels. Using the row and the column decoder, pixel outputs are multiplexed to the ADC input. In this case, the ADC must be very fast to support all of the pixels at a desired frame rate. Since the analog signal must propagate a greater distance and through multiple stages before digitization, the noise level is higher than in the other two approaches. The analog signal needs to settle before being sampled; therefore, the readout speed is limited. This method facilitates a high spatial resolution (small pixels). It is is used in most of the commercial CMOS cameras [15].

Fig. 1.1(a) shows a block diagram of an image sensor with column-level data conversion. With this method, an ADC array is used, where each ADC is dedicated to one or more columns of the pixel array [14, 27–31]. An important advantage of column-level conversion is that digital readout at very high speed is possible. The output rate of an array is proportional to the frame rate and the array size. Therefore, this method is suitable for applications with a high frame rate and large array size. Also, the pixel size is not affected, so the image sensor can achieve a high spatial resolution, the same as an image sensor with chip-level data conversion. Medium speed ADCs

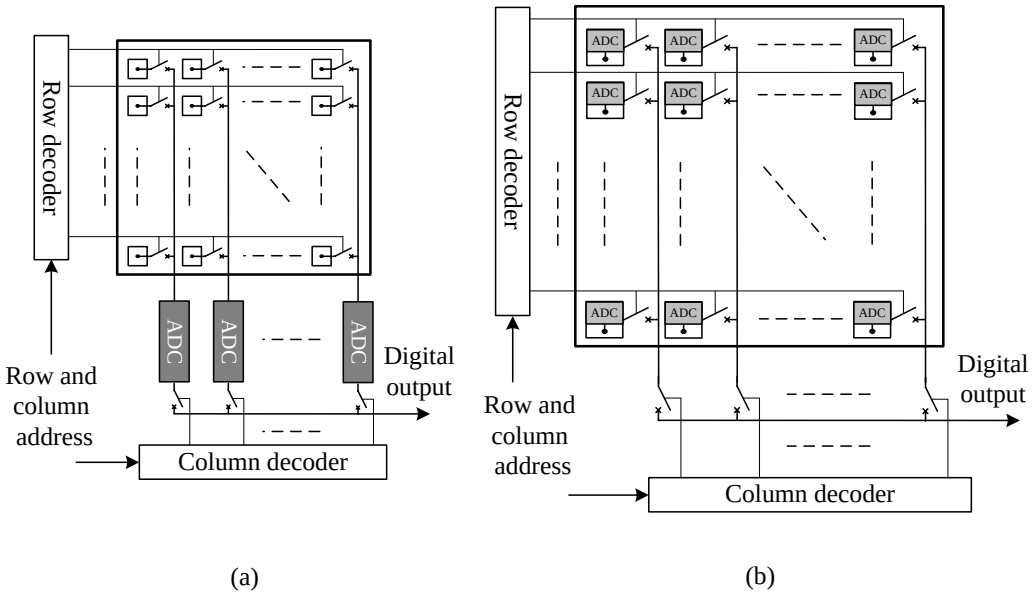


Figure 1.1: Block diagram of an image sensor using (a) column-level data conversion and (b) pixel-level data conversion.

are required. The readout path is shorter than the chip-level structure but longer than the pixel-level architecture. Therefore, the SNR is expected to be medium. Similar to pixel-level ADC, column-level data conversion can use the benefits of delta-sigma ADCs. Temporal noise is filtered without using a low-pass filter. This method presents a compromise between the chip and pixel-level methods. Column-level data conversion has become increasingly popular since it can achieve some advantages of both approaches [17, 32].

In pixel-level data conversion, an ADC is dedicated for each pixel (or for each group of neighboring pixels) and the ADCs are operated in parallel [15, 33–37]. Fig. 1.1(b) shows the structure of an image sensor with pixel-level data conversion. Since the output of each pixel is digital, the sensor is called a digital pixel sensor (DPS).

An important advantage of using DPS is high SNR. Less noise is added to the signal before sampling, which means a higher SNR may be achieved. Moreover, all pixels output digital signals, which are robust to multiplexing. The readout speed is not as limited by bus capacitance and digital readout is possible at very high bit rates [7]. Therefore, high frame rates and large array sizes are achievable. Also, the same pixel layout may be used for a wide range of image sensor sizes. Hence, the array is readily scalable.

Another possible advantage of this method is low power consumption. Since the sampling is done at a low frequency, low-speed ADCs, which could work in the subthreshold region, may be used and a low power con-

sumption is possible. It is believed that the overall power consumption would be less than in the other approaches [33]. In digital pixel sensors, image processing algorithms such as edge detection, object location, and image compression can be done in parallel at very high frame rates [38]. Pixel-level data conversion may also be used to increase the DR of the sensor [39].

The main drawback of pixel-level data conversion is a relatively large pixel size, which makes it difficult to achieve high spatial resolution. Presently, high spatial resolutions are not easy to achieve. But as CMOS technology keeps scaling down, following Moore's law, more transistors may be integrated in a fixed pixel area and parallel processing at the pixel-level becomes more feasible. New developments, such as vertical integration, are expected to help in the same way [33].

These three approaches to data conversion have different influences on the FPN of the image sensor. The FPN is defined as the distortion of the image due to variation in device parameters across the sensor. In the chip-level approach, there is no ADC mismatch as only one ADC exists. However, analog mismatch in the analog read-out circuit may be significant and difficult to correct. Conversely, with the pixel-level approach, the read-out circuit is digital; therefore, it contributes no FPN. However, as there are multiple ADCs, ADC mismatch will contribute to FPN. The column-level approach is somewhere in between. Column-specific FPN shows as vertical line artifacts in the image. FPN can significantly reduce the image quality. Several techniques have been proposed to reduce the effect of FPN, including digital correlated double sampling (CDS) [17]. Using a robust linear ADC, such as the delta-sigma ADC, gives a linear FPN, which is not difficult to correct. One must correct for offset and gain variation of pixel responses across the image sensor.

Recently, column and pixel-level conversion have gained more attention among researchers [15, 17, 33]. Depending on the requirements of an application, each architecture might be preferred. Column-level ADC is preferred for the applications with high spatial resolution and pixel-level ADC is preferred for applications with high bit resolution.

1.2.2 Methods of Data Conversion

Various structures have been proposed to convert the photodetector current to a signal, which is then sampled by the ADC. The goal is to achieve a high DR and high SNDR with an acceptable frame rate, power consumption, and pixel size. Signal preconditioning may be categorized as linear or logarithmic or a variation of one or both methods. Signal digitization leads to other choices, which are discussed later in this section.

Fig. 1.2(a) shows a schematic of the pixel in linear sensors. This type of linear pixel is called an active pixel sensor (APS). In a linear APS, the

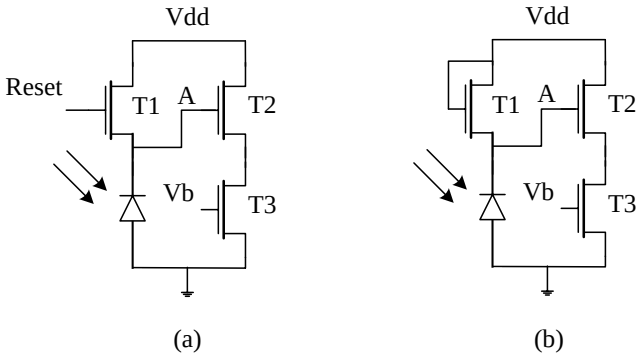


Figure 1.2: (a) Schematic of a linear active pixel sensor (APS). (b) Schematic of a logarithmic APS.

photodetector current is integrated on the capacitance of node A during the sampling interval, and it will be read out at the end of each integration period [15]. Transistor T2 works as a source follower to amplify the signal before readout. Before the next sampling interval begins, node A is reset to the voltage supply. In this method, because of the nature of integration, the signal is low-pass filtered and a peak SNR greater than 55 dB may be achieved [15]. The DR of the linear APS is low because it depends on the integration time, voltage supply, and the noise level. The integration time is limited by the frame rate. The voltage supply and noise floor are restricted by the technology. As the voltage supply of nanometer circuits shrinks down, this issue becomes worse. Some linear sensors have a higher DR but need a long integration time, which limits the frame rate [40].

Logarithmic sensors employ a transistor in the subthreshold region to convert the logarithm of photodetector current to a voltage [16,18]. Fig. 1.2(b) shows the schematic of a logarithmic APS. This is done using a transistor in the subthreshold region, where the I-V curve of the transistor is logarithmic. This method achieves a very high DR, much greater than 100 dB, since the input signal is compressed. But high SNR is not achieved partly because integration does not happen. In [20], the peak SNR for the logarithmic part of the sensor is reported to be 32 dB. The output response is continuous and a high frame rate is easily possible, which is mainly limited by the readout speed. It has been shown that the 3 dB bandwidth of a logarithmic pixel in indoor conditions is 97.5 kHz [19].

Another drawback of logarithmic sensors is high FPN, which is caused by variations of device parameters from pixel to pixel. FPN is less problematic in linear sensors. Some methods of FPN correction for logarithmic sensors have been proposed [18, 41–43]. However, real time implementation of these methods is a subject of ongoing research.

With linear sensors, 23 bits are required to capture a scene with five decades of illumination and 1% accuracy. By contrast, only 10 bits are

needed to accomplish this task in logarithmic sensors [19]. Therefore, compared to linear sensors, a lower bit rate is required in logarithmic sensors to capture the same scene. In fact, logarithmic sensors work in a similar way to the human eye. By converting light to voltage signals on a logarithmic scale, a large light intensity range is mapped to a small electrical voltage range, which can be represented by a smaller number of bits.

A combination of logarithmic and linear sensors are used in some image sensors to achieve a good quality [20, 44]. In linear-logarithmic sensors, the pixel output is linear at low illuminations and logarithmic at high illuminations. One issue with this method is complexity of pixel output.

A lot of research has been conducted to improve the DR of linear sensors [16]. Some of these methods include well capacity adjustment [45], multiple exposure [23, 39], self reset [46], delta-sigma modulation [7], time-domain logarithmic encoding [24, 25], and time-to-saturation [40]. A comparative study of various methods for extending the DR in image sensors is discussed in the literature [21, 22]. The authors conclude that with the present methods, if not impossible, it would be difficult to achieve high DR and SNR with a reasonable pixel size in a planar technology. But recent interest in vertically-integrated image sensors and scaling of CMOS technology provides more area inside the pixel to process the sensitive signal of the photodetector.

ADC architecture is another aspect of the design. Generally, the ADC architecture is selected based on different requirements of the application, such as the bit resolution and the sampling rate. Fig. 1.3 compares some ADC architectures for different sampling rates and resolutions [47]. With the chip level, a high-speed data converter, such as a pipeline ADC, may be employed; for column or pixel, slower ADCs with higher resolution can be used. The ADCs can be grouped into Nyquist-rate ADCs and oversampled ADCs, i.e., delta-sigma ADCs [28].

Nyquist-rate ADCs, such as successive-approximation register (SAR) [48], single-slope [49], and cyclic [17] ADCs, are widely used in image sensors. SAR ADCs have been used for high-speed column-level conversion. The main drawback of these ADCs is the need for matched capacitors and a DAC that occupies relatively a large area. Cyclic ADCs require high power consumption and large area while their noise level is high. Single-slope ADCs have smaller area with higher resolution but high-speed clocks are required, which would lead to high power consumption for high-speed image sensors. In this structure, the conversion time increases exponentially with the resolution, which limits the high-speed readout [50].

Delta-sigma ADCs can provide a high resolution but a decimator filter with large area is required [28, 32]. As explained in Section 1.1.1, unlike with Nyquist-rate ADCs, the temporal noise of the sensor output can be filtered using the delta-sigma ADC without the need for a sharp low-pass filter. Thereby, a higher resolution can be achieved.

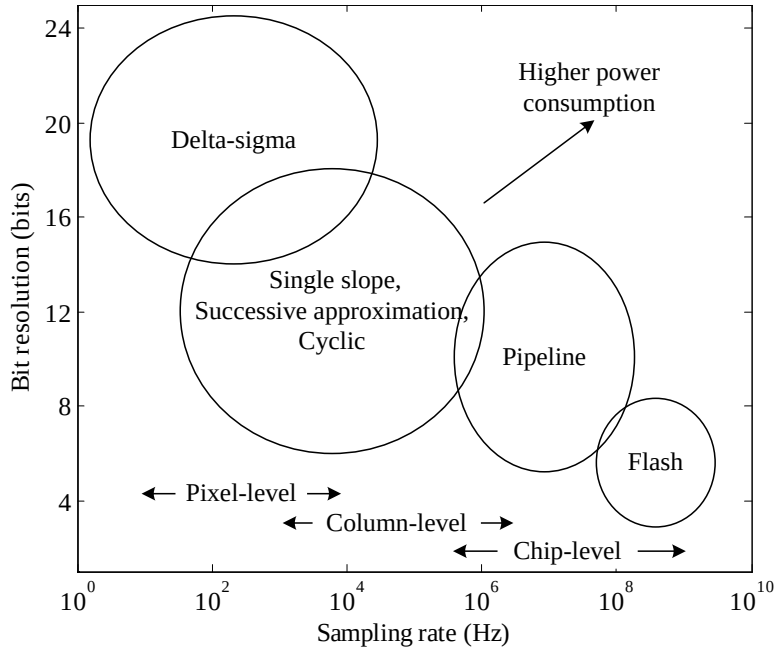


Figure 1.3: Comparison of ADC architectures for different sampling rates and bit resolutions.

Combining logarithmic sensors with delta-sigma ADCs is a good way to digitize video signals. As with the methods used in digitizing audio signals, such as logarithmic predictive coding, which are based on the characteristics of audio signals, the logarithmic sensor is a proper structure for source coding of the high DR light signal into a very small voltage range. In both cases, the non-uniform probability distribution of the signal is exploited through non-uniform quantization. A high resolution delta-sigma ADC can extract the information from the very small voltage range signals of logarithmic sensors.

1.3 State of the Art

A wide variety of approaches have been reported for analog-to-digital conversion in image sensors, most of which pertain to chip-level ADC, many of which pertain to column-level ADC, and some of which pertain to pixel-level ADC. As mentioned in Section 1.1.1, there are strategically good reasons to choose delta-sigma ADCs over other types of ADCs. Within the context of delta-sigma ADCs, there are some publications related to column and pixel-level data conversion, which are discussed here.

1.3.1 Delta-Sigma Column Sensors

Column-level delta-sigma ADCs have been implemented by some researchers. Most of the previous works use simple circuits for the modulator to reduce the power dissipation and area usage at the cost of reducing the tolerance of the circuit to noise. Also the decimator is often implemented using a counter, which is not an efficient method.

The first image sensor employing column-level delta-sigma ADCs was implemented by Mendis *et al.* [51]. The array used a switched-capacitor first-order modulator. The decimation was done using a 10-bit counter in each column. An APS with $40 \times 40\,\mu m^2$ pixel size was employed. Each pixel was a single CCD stage, which was implemented using conventional CMOS technology. A relatively noisy picture was achieved.

Nakamura *et al.* designed a current-mode second-order delta-sigma ADC in a $2\,\mu$m CMOS process for column-level data conversion [52]. Only the modulator was fabricated, which had an area of $80 \times 1920\,\mu m^2$. The decimator filter was implemented off-chip.

Also, another image sensor using column-level first-order structure was fabricated in $0.35\,\mu$m CMOS by Morris *et al*. The ADC took $8.2 \times 1690\,\mu m^2$, including a 13-bit counter, which was used for decimation. Detailed performance of the image sensor was not presented in the paper [53]. A similar architecture was only simulated in [54].

Column-level data conversion using a delta-sigma ADC has also been combined with focal-plane image compression. In [31], the APS array is integrated with a group of first-order incremental delta-sigma ADCs and a Haar wavelet transform is realized to achieve a low bit rate for high frame-rate video. The decimation is performed using a counter.

In [27], a 4×4 array of pixels using switched-capacitor second-order delta-sigma ADCs is fabricated in $0.18\,\mu$m CMOS. The ADC uses a single-ended circuit to reduce the area at the cost of less tolerance to noise. A standard three-transistor APS is used. The ADC takes $15 \times 500\,\mu m^2$. Decimation is performed off-chip using a second-order sinc filter. The pixel size is $225\,\mu m^2$ and the fill factor is 50.1%. The fill factor is defined as the ratio of photodetector area to total area of the pixel. The prototype can detect three decades of light level. This is improved to five decades using the saturation detection technique.

Column parallel delta-sigma ADC has also been used in an electrochemical DNA-detection array [14]. A first-order current-input delta-sigma ADC is used in an array of 24×24 electrodes, where the electrode-electrolyte capacitance is used as the integrator. The decimation is performed off-chip.

The most recent work on column-parallel delta-sigma ADCs was done by Chae *et al.* [28, 29] in $0.13\,\mu$m CMOS. A block diagram of the circuit is shown in Fig. 1.4. The second-order modulator is implemented with single-ended inverter-based switched-capacitor circuits [55]. The image sensor has

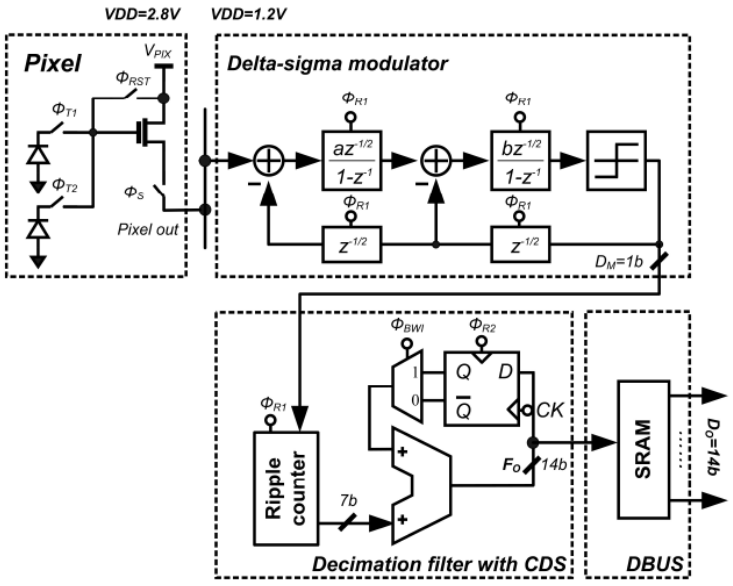


Figure 1.4: Schematic of a readout circuit using a column-level delta-sigma ADC, taken from Chae *et al.* [28].

180 mW of power consumption and 73 dB of DR at 120 fps. The second-order decimator with CDS is implemented for each column using a counter and an accumulator. Although a high frame rate is achieved at low power consumption, the sensor achieves a limited DR because a linear sensor is used.

Unlike the previous works, the architecture proposed in this thesis uses a robust circuit to achieve a high SNR. Every effort was made to reduce the area usage and the power consumption of the modulator and the decimator. A design flow is presented for the modulator and decimator to accomplish this task. The decimation is performed with an optimum filter while the circuit has a small area. Therefore, as will be shown, for the same oversampling ratio, a higher SNR is achieved. Smaller ADCs provide more area for the sensor array and a larger array can be fabricated in the same die.

1.3.2 Delta-Sigma Pixel Sensors

Designing a pixel-parallel delta-sigma ADC is a challenging task, especially in long-channel CMOS technology. In this section, the previous works on pixel-level delta-sigma ADC are discussed. In all the previous works, because of a limited available area, the modulator circuit has been designed using only a small number of transistors. Therefore, a limited SNR has been achieved. Also, the decimation has been performed outside the pixel. Performing the decimation outside the pixel would limit the maximum bit rate, oversampling ratio, and SNR.

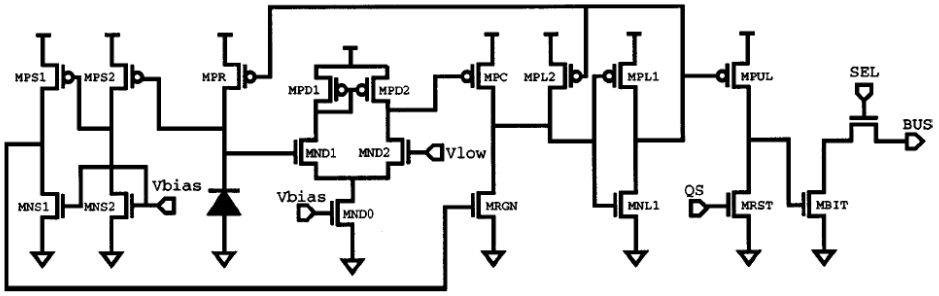


Figure 1.5: Schematic of a pixel using a pixel-level delta-sigma ADC, taken from McIlrath [7].

The first implementation of a pixel-level delta-sigma ADC was done by Fowler *et al.* [8]. They designed a very simple in-pixel first-order modulator with a linear sensor. The pixel size was $60 \times 60\,\mu\text{m}^2$ with a low fill factor of 3%. The sensor suffered from a high FPN of 10% [34]. The peak SNR was reported to be 33 dB, which is very low for linear sensors.

Later, Yang *et al.* modified the design to improve its performance [56]. The new design was $20.8 \times 19.8\,\mu\text{m}^2$ with a fill factor of 30%. The pixel output suffered from a high gain variation or FPN, poor low light response, nonlinear response, and charge mixing between multiplexed pixels. A similar approach was used by Ignjatovic *et al.* [57, 58], where part of the ADC was moved to the row and shared between the pixels of each row. Thereby, the fill factor was increased.

McIlrath used the linear sensor structure to design a free-running asynchronous oscillator, which works similar to a delta-sigma modulator [7]. Fig. 1.5 shows a schematic of the pixel in this design. The photodetector capacitance is used to implement the delta-sigma integrator and simplify the structure of the modulator. The circuit has four sections: a differential amplifier, which compares the photodetector output to a reference voltage; a latch, which generates the reset signal; a regenerative section, which switches the latch and restarts the integration; and one-bit memory, which stores the output bit after the reset. The pixel that was implemented in $0.5\,\mu$m CMOS occupied $30 \times 30\,\mu\text{m}^2$. Decimation was performed off-chip. She used a recursive method in a decimator outside the pixel to decrease the required bit rate but a high SNR was not achieved due to a limited oversampling ratio. As discussed by Kavusi *et al.* [21, 22], high DR is also not achievable by this structure.

A pixel-parallel delta-sigma modulator was designed for a scalable array of 8×8 pixels in $0.8\,\mu$m Si CMOS by Joo *et al.* [36]. In this work, delta-sigma data conversion at the pixel-level is proposed as a proper solution to realize smart CMOS focal plane arrays with a high frame rate and a large array size. Fig. 1.6 shows the modulator circuit, which is laid out in a $125 \times$

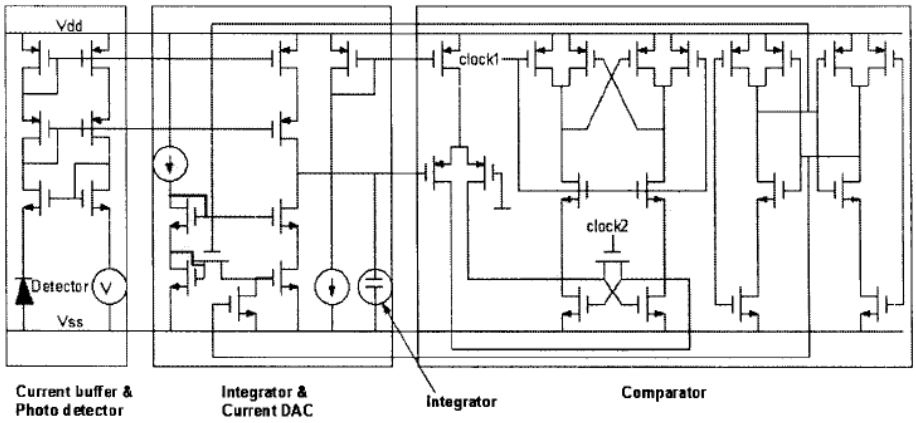


Figure 1.6: Schematic of a pixel using a pixel-level delta-sigma ADC, taken from Joo *et al.* [36].

$125\,\mu m^2$ pixel. The current-input first-order modulator is composed of a photodetector with a current buffer, an integrator, a DAC, and a comparator. The circuit is simple and requires little area but it is very susceptible to noise.

A similar architecture was also proposed for X-ray applications, where a larger pixel size is allowed [9, 59]. An array of 64×64 pixels, employing current-input first-order delta-sigma ADCs, is fabricated in $0.7\,\mu m$ technology. The ADC is designed in an area of $118 \times 48\,\mu m^2$.

In the previous works, the decimation was done outside the pixel. Also, a simple modulator with a limited performance was used. Moreover, only linear sensors were used. In this thesis, a pixel-level ADC is designed and combined with a logarithmic sensor. Unlike the prior art, the decimation is performed in the pixel to increase the frame rate and SNR and to make the array scalable.

1.4 Scope of the Thesis

In this thesis, column and pixel-level data conversion using delta-sigma ADCs are explored. The ADC, especially at the pixel-level, has to be designed in a limited area. Digital circuits can be designed as small as the design rules allow. But analog circuits with smaller area would have more mismatch and variation in their specifications, which can cause nonlinearity in the ADC. To avoid mismatch, the ADC should be designed with large enough transistors and a sophisticated layout. Also, hundreds of ADCs should be working in parallel. Therefore, the power consumption of each one should be minimized. A methodology for designing low-area low-power switched-capacitor delta-sigma ADCs is presented. Based on that, two stand-alone ADCs with specifications for column and pixel-level

data conversion are fabricated and tested. They advance the state of the art.

While higher-order delta-sigma ADCs have been widely studied [1, 3, 60], first-order delta-sigma ADCs have not been popular because of issues with high power consumption and the need for high-speed clocking. Using the new methodology presented in this thesis, the first-order architecture can be realized with very low power consumption, which is comparable to state-of-the-art ADCs at column or pixel level [60, 61].

In order to evaluate the effectiveness of the proposed architectures in a specific application, two image sensors using column and pixel-level delta-sigma ADCs were fabricated and tested. Unlike previous works, the designs are targeted to logarithmic-response image sensors, which suffer from low SNDR, instead of linear-response image sensors, which suffer from low DR. Delta-sigma ADCs at column or pixel level can reduce temporal noise, and thereby improve the DR and SNDR in linear and logarithmic sensors. Previous works have shown that using delta-sigma data conversion can improve the DR of linear sensors, which is still smaller than the DR of logarithmic sensors [7]. This work shows that the SNDR of logarithmic sensors is improved and can rival that of the human eye.

In all the previous works on pixel-parallel delta-sigma ADCs, the decimation was performed either at chip-level or off-chip. Hence, the pixel output had a high bit rate, limiting the frame rate and array size. In this work, the decimator is implemented inside the pixel to reduce the output bit rate. This permits a high oversampling ratio and, consequently, a high SNR.

In Chapter 2, the architecture of delta-sigma ADCs is discussed and a design flow to reduce the area and power consumption of the decimator is presented. This includes a new architecture for decimation, which is suitable for parallel decimation. The presented method enables a significant reduction in area usage and power consumption of decimators for ADC arrays. A design flow for designing the modulator is detailed in Chapter 3, which complements the decimator design flow and reduces the area and power consumption of first-order modulators significantly, making it possible to use them efficiently in pixel and column-level data conversion. The work includes theoretical calculations, as well as behavioral and circuit simulation. In Chapter 4, the experimental results of two delta-sigma ADC arrays fabricated in 0.18 μm CMOS technology are discussed and compared with state-of-the-art delta-sigma ADCs, showing comparable figures of merit but with smaller area. Experimental results of a second chip, comprising two image sensors fabricated in 0.18 μm CMOS technology, are presented in Chapter 5, showing a higher SNDR compared to state-of-the-art logarithmic sensors. The image sensors utilize column and pixel-level delta-sigma data conversion with logarithmic sensors. In Chapter 6, the main contributions of the thesis and future work are presented.

Chapter 2

Decimator Design Flow

Delta-sigma ADCs require two components [3, 4]: a modulator, and a decimator. The modulator samples the input signal with a sampling rate greater than the Nyquist rate, and quantizes the signal using a coarse step size. In the decimator, the output signal of the modulator is low-pass filtered to remove out-of-band quantization noise and high frequency components. Then the signal is downsampled to the Nyquist rate.

A goal of this thesis is to design a delta-sigma ADC for parallel data conversion either at the column or pixel levels. To do so, the area and power consumption of the ADC should be reduced as much as possible while maintaining a high SNDR. In this chapter, the basic principles of the delta-sigma ADC are reviewed. After reviewing delta-sigma ADCs, the chapter focuses on decimator design, which is a critical component in parallel data conversion.

In previous works, especially on pixel-level data conversion, the decimator is shared among the ADCs. This limits the sampling rate, oversampling ratio, and SNDR of the ADC [7, 8]. In some other works, a simple counter is used to perform the decimation, which is not efficient. In this chapter, different methods of decimation are explained. These methods are intended for stand-alone ADCs and are not suitable for ADC arrays. Therefore, a design flow for parallel decimation is proposed. Based on the specifications of the application, one can use this design flow to implement a small-area and low-power circuit for decimation.

In Section 2.1, the concept of oversampling is explained, and the basic fundamentals of delta-sigma ADCs are briefly introduced. Also, the decimation methods for stand-alone ADCs are discussed. The design flow for parallel decimation is presented in Section 2.3. In Section 2.4, the significance of the proposed architecture is explained.

2.1 Delta-Sigma ADCs

The main motivation behind oversampling, in oversampled ADCs, is that if an analog signal is sampled and quantized at a sampling frequency higher than the Nyquist rate, the quantization noise from the quantizer will spread though the spectrum uniformly [4]. A higher sampling rate will result in a lower quantization noise power in the signal bandwidth and ,consequently, a higher bit resolution. Using a digital low-pass filter (LPF), the out-of-band quantization noise can be filtered and finally the signal is down-sampled to the Nyquist rate. The delta-sigma ADC is the main form of oversampling ADCs. By using a feedback loop in the modulator, the quantization noise is shaped to further reduce the quantization noise power in the signal bandwidth. In this section, the basic theory behind the delta-sigma ADC is explained.

2.1.1 Oversampling

Oversampling allows noise filtering to be done in the digital domain but at higher frequency. This can be easily performed using digital signal processing in CMOS technology [3]. Fig. 2.1 shows the block diagram of an oversampling ADC with the signal spectrum illustrated at each stage. Consider an analog signal $x(t)$ with useful bandwidth f_B. The input signal is passed through a soft analog LPF to cancel components at very high frequencies. Then the signal is oversampled, i.e., sampled at many times the Nyquist rate of $2f_B$, and coarsely quantized. Using a sharp digital LPF, out-of-band noise is removed from the signal. This includes the noise introduced by quantization as well as temporal noise in the original analog signal.

Assuming that the quantizer input is uniformly distributed over its domain, the quantization noise can be modeled as a uniformly distributed noise. As Fig. 2.1 illustrates, quantization noise power is uniformly spread over the entire bandwidth. This white noise assumption is robust in practice due to dithering of the quantizer by analog noise. For a larger oversampling ratio (M), the power spectral density (PSD) of the quantization noise is lower because the noise power is a constant function of the quantization step size, whereas the bandwidth depends on the oversampling ratio (M). After digital low-pass filtering, less noise would remain in the signal band for a larger oversampling ratio. This structure is called a zeroth-order delta-sigma ADC.

Assuming that the quantization noise is uniformly distributed within bounds $\pm\Delta/2$, where Δ is the quantization step size, the quantization noise power is [62]

$$P\{e[n]\} = \frac{\Delta^2}{12}. \tag{2.1}$$

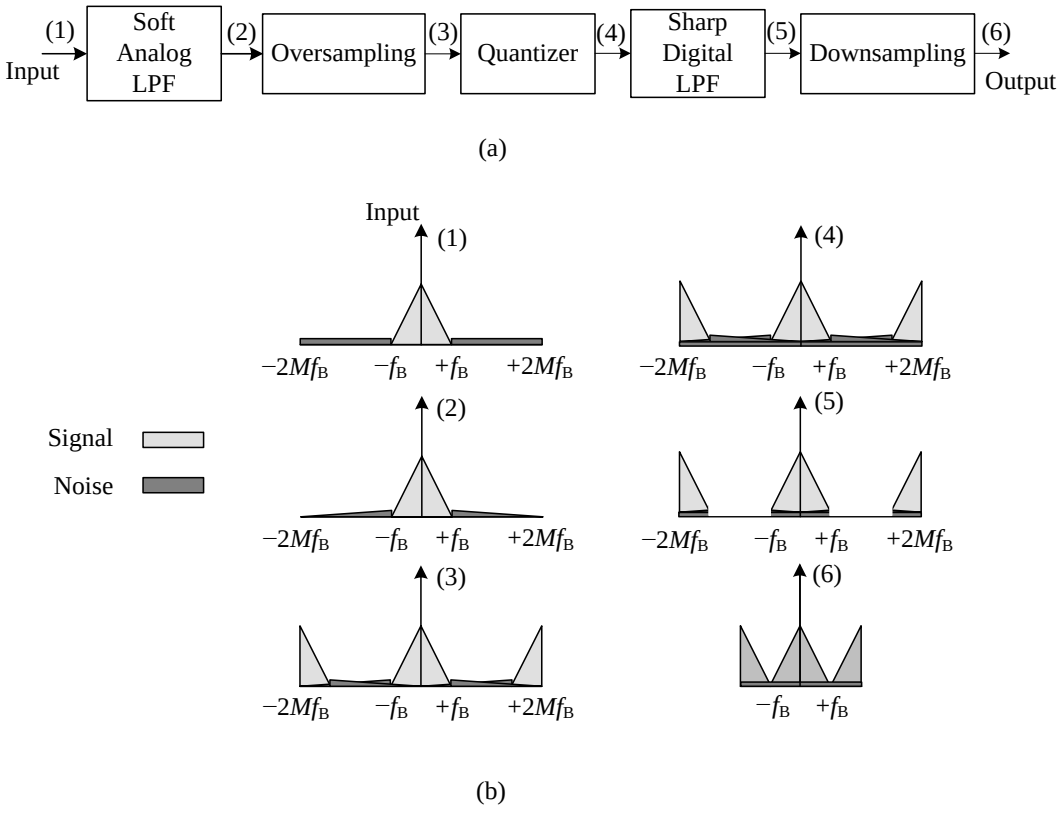


Figure 2.1: (a) Block diagram of an oversampled ADC without noise shaping. (b) Signal spectrum at different stages in the oversampled ADC.

If an ideal digital LPF is used, the filtered quantization noise power would be [62]

$$\sigma_q^2 = \frac{\Delta^2}{12M}. \tag{2.2}$$

Thus, for every doubling of the oversampling ratio, the quantization noise is reduced by 3 dB.

2.1.2 Noise Shaping

The purpose of noise shaping is to modify the oversampled ADC architecture so that the quantization noise power is concentrated outside the signal band, instead of having a uniform power spectral density. In this way, digital low-pass filtering removes more of the quantization noise and the quantization is performed more efficiently.

Fig. 2.2(a) gives a block diagram of an oversampling ADC with first-order noise shaping, which is called a first-order delta-sigma ADC. The embedded low-resolution ADC is usually a one-bit comparator. With a comparator, a high linearity is easily achieved. In this case, a one-bit digital-to-

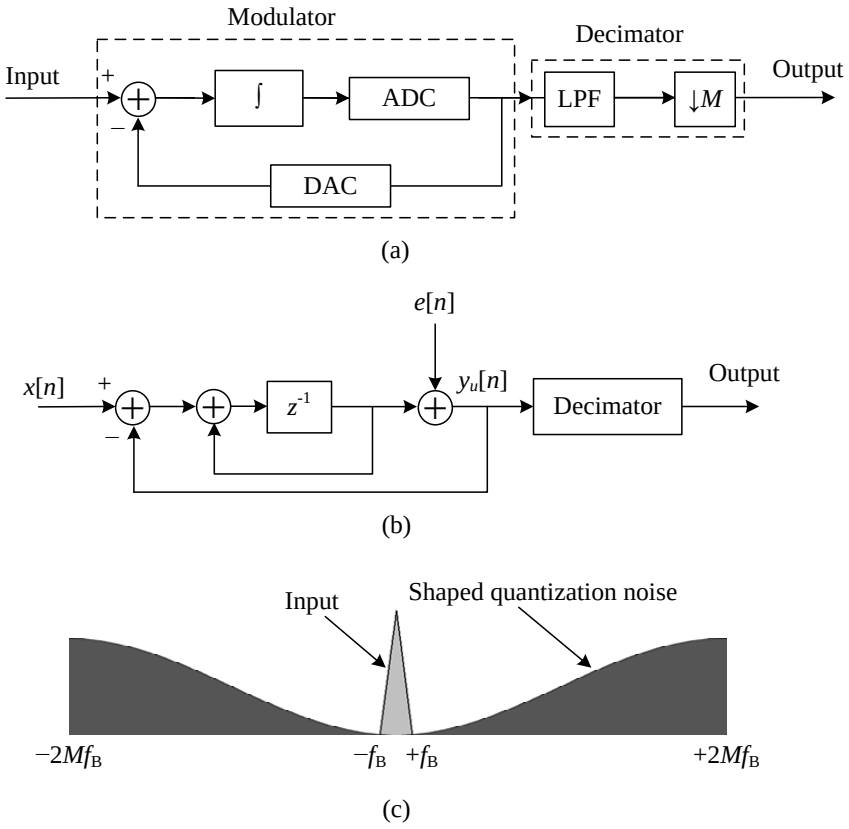


Figure 2.2: (a) The first-order delta-sigma ADC. (b) Signal waveforms when the input signal is close to an internal reference voltage. (c) Linear discrete-time model of the first-order delta-sigma ADC. (d) Shaped spectrum of the quantization noise.

analog converter (DAC) is implemented using reference voltages representing zero and one. If a multi-bit ADC-DAC combo is used, a higher SNR is possible with the same oversampling ratio. But linearity of the multi-level quantizer is critical to achieving a high SNDR. Example signal waveforms are given in Fig. 2.2(b). Fig. 2.2(c) shows the discrete-time model of the first-order delta-sigma ADC when a one-bit ADC and DAC are used [63,64]. Fig. 2.2(d) shows the output spectrum of the first-order modulator. In this case, the quantization noise is shaped and there is less quantization noise power inside the signal bandwidth.

The modulator is responsible for oversampled noise shaping. The decimator is responsible for low-pass filtering and downsampling. It can be shown that, for the first-order delta-sigma ADC, the output of the modulator is [4]

$$y_u[n] = x[n-1] + (e[n] - e[n-1]). \tag{2.3}$$

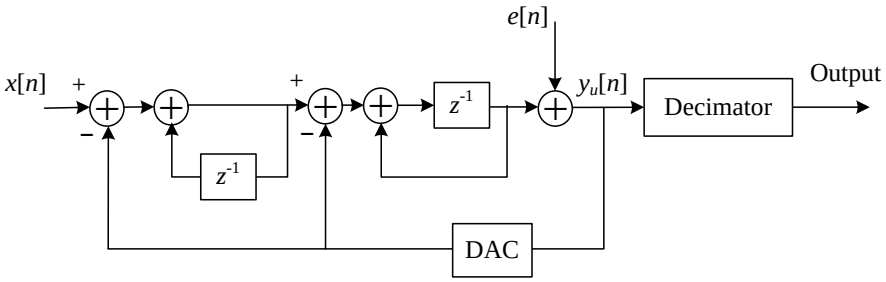


Figure 2.3: Linear discrete-time model of the second-order delta-sigma ADC.

The z-transform of the modulator output $y_u[n]$ is

$$Y_u(z) = z^{-1}X(z) + E(z)\cdot(1-z^{-1}), \tag{2.4}$$

where $E(z)$ is the z-transform of the quantization noise $e[n]$. After decimation using an ideal filter, the quantization noise power is approximately [62]

$$\sigma_q^2 = \frac{\Delta^2\pi^2}{36M^3}. \tag{2.5}$$

In the first-order modulator, for every doubling of the oversampling ratio, the quantization noise is reduced by 9 dB and provides 1.5 bits of extra resolution [3]. Comparing (2.2) and (2.5), the final quantization noise power in a zeroth-order delta-sigma ADC is proportional to the inverse of M, whereas it is proportional to the inverse of M^3 in a first-order delta-sigma ADC. Consequently, by using the noise shaping method, increasing the oversampling ratio decreases the final quantization noise power faster.

As (2.4) shows, the delta-sigma modulator output is the delayed input plus filtered quantization noise. To decrease the final quantization noise power further, higher-order noise-shaping modulators may be used. For a K^{th}-order delta-sigma ADC, (2.4) becomes [3]

$$Y_u(z) = z^{-1}X(z) + E(z)\cdot(1-z^{-1})^K. \tag{2.6}$$

Fig. 2.3 shows the discrete-time model of the second-order delta-sigma ADC [64]. In this case, the output signal can be expressed using (2.6) as

$$Y_u(z) = z^{-1}X(z) + E(z)\cdot(1-z^{-1})^2. \tag{2.7}$$

After decimation using an ideal LPF, the quantization noise power is [4]

$$\sigma_q^2 = \frac{\Delta^2\pi^4}{60M^5}. \tag{2.8}$$

In the second-order modulator, every doubling of the oversampling ratio reduces the quantization noise by 15 dB, providing 2.5 extra bits of resolution [3]. Comparing (2.5) and (2.8), we can say that a second-order

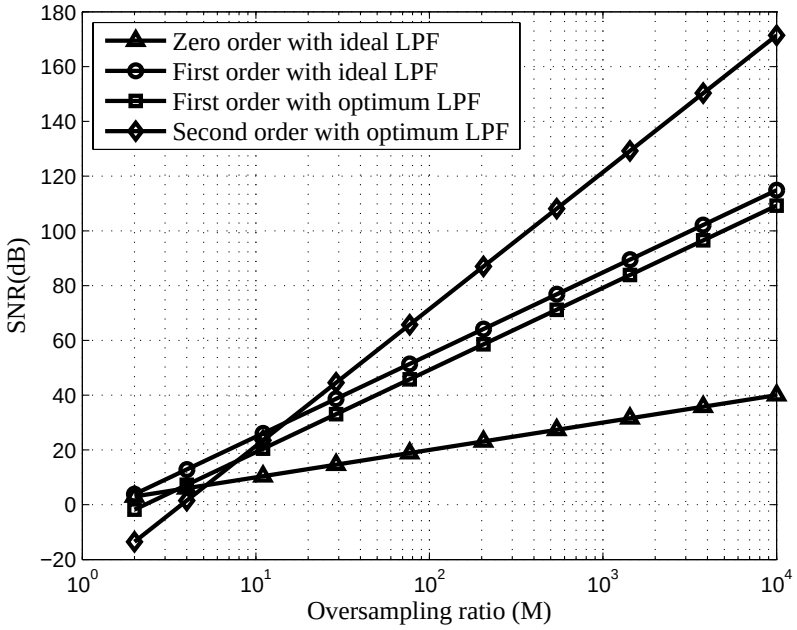


Figure 2.4: SNR versus oversampling ratio for different orders of the delta-sigma ADC and different decimation filters.

delta-sigma architecture gives higher SNR for the same oversampling ratio. Therefore, a lower clock speed is needed. The second-order modulator is usually preferred over the first-order design. But since the first-order system requires much less area, it is more suitable for parallel data conversion.

As with the first-order modulator, the second-order one is tolerant to circuit imperfections. However, the second-order system has more components and one more design parameter—the gain ratio of the two feedback paths. Gains have to be more precise compared to the simpler system.

Fig. 2.4 plots the SNR at the ADC output versus oversampling ratio for different orders and different decimation filters. Increasing the order of the noise-shaping modulator can improve the SNR at the output. However, higher-order modulators are more difficult to realize for orders greater than two due to stability problems [3] but they do exist in practice. Also, the SNR is partly determined by the structure of the decimator filter. Decimation filter design will be discussed in the next section.

2.2 Conventional Decimation

The output of the modulator, which is the input of the decimator, represents the input signal together with the out-of-band components. The purpose of the decimator is twofold: to remove out-of-band quantization noise and other noises in the oversampled signal; and to downsample the signal

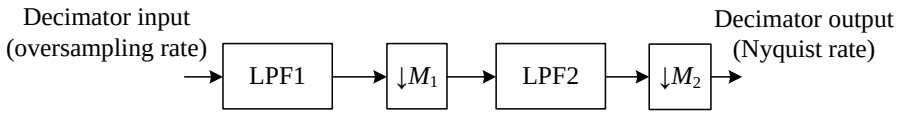


Figure 2.5: Decimating the output of the modulator in two stages. The oversampling ratio is equal to $M_1 \times M_2$.

by M. Decimation exchanges temporal resolution for bit resolution. Decimation filters can be easily implemented using CMOS technology. A simple decimator filter is a counter, which is used in some designs [31,51,53]. This method is very simple but not efficient. A variety of architectures have been proposed for decimation in stand-alone ADCs. In this section, these methods are briefly discussed.

The decimation may use a finite-duration impulse response (FIR) [65] filter, an infinite-duration impulse response (IIR) filter [66,67], a nonlinear filter, etc. Apart from causality and stability, there are two major requirements for the decimator filter. The first is that the frequency response is designed to pass the in-band signal at the input of the modulator. The second is that the frequency response is designed to attenuate the out-of-band signals, including quantization noise. Given other constraints, there is an optimal FIR filter for the decimator, which corresponds to the modulator order. The optimum decimation filter for the first-order system has a parabolic shape [68].

Decimation at high oversampling rate requires a large area and consumes a high power. Conventional implementations of delta-sigma ADCs focus on the design of a few ADCs per chip (usually one). Decimation is often performed in several stages, and usually in two stages [3]. Fig. 2.5 shows how the decimation is performed in two stages.

In the first stage, a simple LPF is used predominantly to remove the quantization noise because this noise dominates at high frequencies. Since the input signal of the filter is one bit, the word length is smaller than the second stage, but the bit rate is higher. After the first LPF, the signal is down-sampled to an intermediate frequency. Then the second LPF, which is sharper, is used to remove the out-of-band components of the signal, which dominate at the lower frequency. The filter is designed to meet the anti-aliasing requirements of the input signal. Because the bit rate is low, the circuit may process bits in serial manner. Since the second filter needs to be sharper, it has a higher order compared to the first LPF.

Using the method of multi-stage decimation, power consumption is reduced because most of the processing is done at a lower frequency. An intermediate frequency, four times greater than the Nyquist rate, is a good choice for many applications [4].

Designing the first stage LPF is more challenging since it works at a high

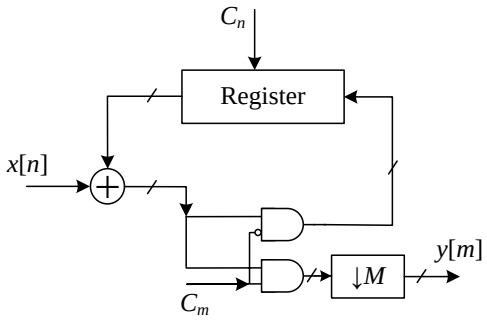


Figure 2.6: Block diagram of an accumulate-and-dump circuit. C_n is the input clock and C_m is the output clock.

bit rate with high power consumption. A simple way to implement the first stage LPF is to use the accumulate-and-dump circuit. Fig. 2.6 shows an accumulator-and-dump circuit [3]. The output clock is M_1 times slower than the input clock with a duty cycle of $1/M_1$. Input data is accumulated in the register. When C_m is one, the content of the register is read out, while the register is cleared. If the filter inputs are $x[n]$ at the oversampling frequency of $f_n = 1/T_n$, and the output samples are $y[m]$ at the intermediate sampling frequency of f_m, then

$$y[m] = \frac{1}{M_1} \sum_{n=1}^{M_1} x[M_1 m - n], \tag{2.9}$$

where M_1 is the downsampling ratio. The transfer function of the filter is a finite geometric series:

$$H(z) = \frac{1}{M_1} \sum_{i=0}^{M_1-1} z^{-i} = \frac{1}{M_1} \frac{1 - z^{-M_1}}{1 - z^{-1}}. \tag{2.10}$$

For $z = e^{j2\pi f T_n}$, the frequency response of the filter is given by [4]

$$H(f) = \frac{\mathrm{sinc}(\pi f M_1 T_n)}{\mathrm{sinc}(\pi f T_n)}. \tag{2.11}$$

It has been shown that for decimating the signal of modulators of order K, a comb filter is close to the optimum filter and its frequency response is given by

$$H(f) = \left(\frac{\mathrm{sinc}(\pi f M_1 T_n)}{\mathrm{sinc}(\pi f T_n)} \right)^{K+1}. \tag{2.12}$$

For K=1, the filter has a triangular-shaped impulse response. Ignoring $1/M_1$, the DC gain of each stage of the filter, the transfer function of the

comb filter is given by [69]

$$H(z) = \left(\frac{1 - z^{-M_1}}{1 - z^{-1}} \right)^{K+1}. \tag{2.13}$$

2.2.1 Implementation Methods

Different architectures have been proposed to implement the comb filter [65, 66, 69–73]. Fig 2.7(a) shows the simplest implementation method of this filter. In this method, $K+1$ accumulate-and-dump circuits are cascaded together. Since the processing is performed at a very high speed with a large word length, the power consumption is very high. Also, the circuit occupies a large area.

The comb filter can be decomposed into two filters, an IIR filter H_1 and an FIR filter H_2, as follows [66]:

$$H(z) = H_1(z) \times H_2(z), \tag{2.14}$$

where

$$H_1(z) = \left(\frac{1}{1 - z^{-1}} \right)^{K+1}, \tag{2.15}$$

and

$$H_2(z) = \left(1 - z^{-M_1} \right)^{K+1}. \tag{2.16}$$

As shown in Fig. 2.7(b), the filter can be implemented in two stages. The first stage is a cascade of $K+1$ integrators. The second stage is a cascade of $K+1$ differentiators, which can be done after downsampling [66]. The integrators work at a high speed while the differentiators work at a very low speed. To avoid overflow, the filter is implemented with two's complement arithmetic with the proper size for the registers. A large word length is required for each stage. The IIR-FIR filter consumes less power compared to the previous method.

For the first-order system, the IIR-FIR decimator needs two accumulators and two differencers. The word length at all the stages should be

$$W = (K+1)\log_2(M_1) + B_{\text{in}} - 1, \tag{2.17}$$

where B_{in} is the input word length of the decimator, which is one, and K is the order of the modulator [66]. For an oversampling ratio of 1024, 80-bit registers with 4 multi-bit adders are required to implement the decimator using this method. Truncation or rounding may be used at each filter stage to reduce the size of the register at the cost of creating some rounding error [66].

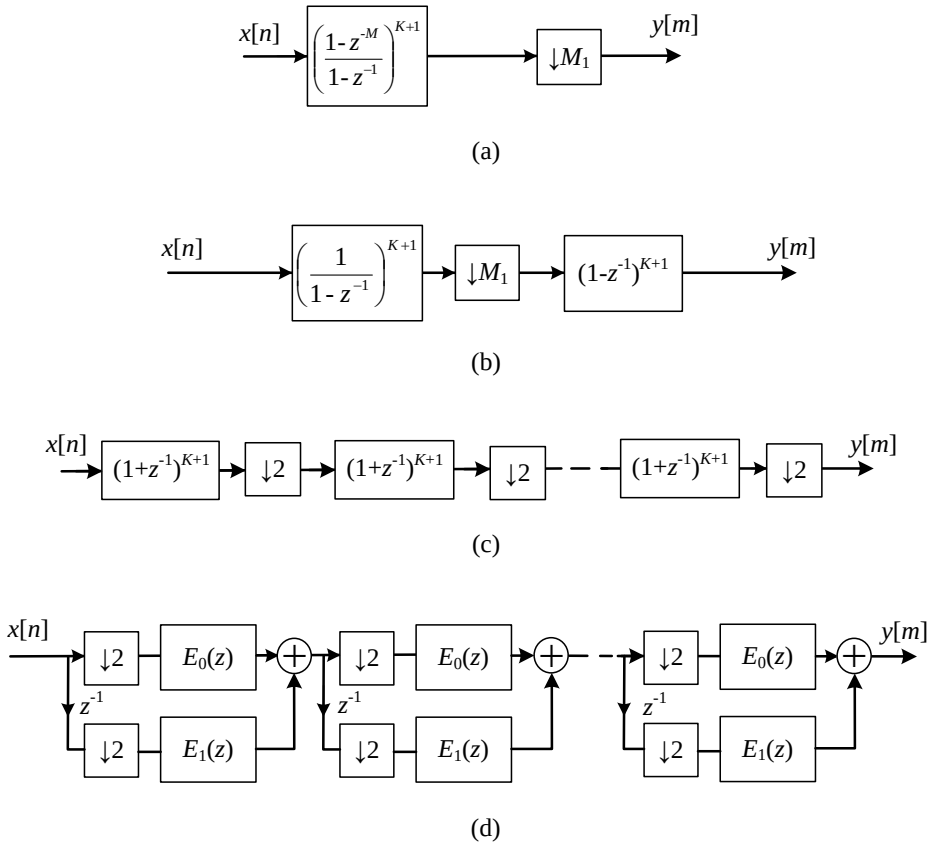


Figure 2.7: Implementation methods of comb filters: (a) simple; (b) IIR-FIR; (c) FIR2; and (d) POLY-FIR2.

If the decimation factor M_1 is a power of 2, by using a commutative rule, (2.10) can be rewritten as [65]:

$$H(z) = \left(\sum_{i=0}^{2^N-1} z^{-i} \right)^{K+1} = \prod_{i=0}^{N-1} (1 + z^{-2^i})^{K+1}. \tag{2.18}$$

Using (2.18), a non-recursive architecture of the comb filter can be implemented with a lower power consumption than the IIR-FIR filter. This method is called FIR2, which is shown in Fig. 2.7(c). Every stage is a simple FIR filter. The word length in each stage i is $B_{\text{in}} + (K+1)i$ bits but the sampling rate decreases through every stage by a factor of 2. For example, in the first-order system with a 1024 oversampling ratio, a 120-bit register with 10 multi-bit adders are required to realize the filter.

Polyphase decomposition of the FIR2 filter can lead to a more efficient structure, which is called POLY-FIR2 [70]. This method is illustrated in Fig. 2.7(d). The structure is obtained by representing the sequence as a superposition of polyphase components; therefore, the unnecessary computation is eliminated and power consumption is reduced. For example,

for $K = 1$, each block in the FIR2 method can be written as [70]:

$$H_i(z) = (1 + z^{-1})^2 = 1 + z^{-2} + 2z^{-1} = E_0(z^2) + z^{-1}E_1(z^2), \tag{2.19}$$

where

$$E_0(z) = 1 + z^{-1}, \tag{2.20}$$

and

$$E_1(z) = 2. \tag{2.21}$$

Similar to the FIR2 architecture, the word length of each stage i is limited to $B_{\text{in}} + Ki$. The power consumption of this method is significantly lower than the other methods [69].

Other authors have tried to enhance the performance of the comb filters. For instance, in [73], a method has been presented also using polyphase decomposition to reduce the power consumption of the comb filter further. In [72, 74], other methods are proposed to improve the frequency response of the filter but the power consumption or the area usage is not reduced.

Comparing the above methods, polyphase decomposition tends to have the lowest power consumption, while the IIR-FIR filter has the lowest area. The main parameter for the decimator in parallel data conversion is the area usage and then the power consumption. The previous works on decimation filters focus mainly on reducing the power consumption. Therefore, these methods are not suitable for delta-sigma ADC arrays. The decimator design flow proposed in the next section presents a novel FIR filter, which has an area smaller than the previous works, while its power consumption is low. Therefore, it is suitable for delta-sigma ADC arrays.

2.3 Parallel Decimation

For parallel decimation, the available decimator designs require an unworkably high area usage and power consumption. For instance, in the first-order system, using the IIR-FIR method with a 1024 oversampling ratio, 80-bit registers with four one-bit adders are required and integrators must be clocked at the oversampling rate. With column-level data conversion, there will be upwards of a thousand ADCs per chip for a megapixel array. With pixel-level data conversion, there will be upwards of a million ADCs per chip for a megapixel array. Inevitably, it would be very difficult to use the conventional decimator filters for parallel decimation. Using the design flow presented in this section, a decimator filter equivalent to the optimal FIR filter is obtained. The filter has lower area usage and power consumption for ADC arrays.

The coefficients of the optimum filter are generated at the chip level using a coefficient generator and are sent to each column or pixel, where

they are convolved with the modulator output. The result is then stored in the accumulator. In each column or pixel, the decimator only needs one accumulator plus an AND gate. This method is very well suited for parallel decimation. The reason is because the coefficient generator is shared by all the ADCs. Therefore, its area usage and power consumption per ADC is negligible.

The filter structure is similar for column-level and pixel-level data conversion. Moreover, using the same circuit in the decimator, filters corresponding to higher-order modulators may be implemented. In each case, only the coefficient generator needs to be modified. As was discussed in Section 2.2, conventionally, a triangular impulse response (second-order comb filter) is used in the first-order system since it is easier to implement. In the proposed method, the optimum parabolic filter is implemented.

2.3.1 Coefficient Generation

The coefficient generator for the first-order system is presented here. A similar method may be used to design the circuit for higher-order systems. The optimal FIR decimation filter, for the first-order delta-sigma modulator with DC input signal, has a parabolic impulse response [68]. Therefore, the M-tap impulse response of the filter can be written as:

$$h[n] = \begin{cases} a_2 n^2 + a_1 n + a_0, & 0 \le n \le M-1 \\ 0, & \text{otherwise} \end{cases} . \tag{2.22}$$

As (2.3) shows, the modulator outputs the delayed input signal plus the shaped quantization noise. For a DC input signal, the input signal of the ADC is constant for exactly M samples. While filtering the quantization noise, the FIR decimation filter multiplies the input signal by a constant gain, which is equal to the sum of the impulse response coefficients of the filter. Therefore, distortion is avoided in the decimator. If the filter has more than M taps, distortion appears when the input signal changes from one Nyquist interval to the next, and it may limit the output SNR. The gain does not affect the performance and is set to be one, i.e.,

$$\sum_{n=0}^{M-1} h[n] = 1. \tag{2.23}$$

Using (2.1) and (2.3), the quantization noise power at the output of the decimation filter is determined to be

$$\sigma_q^2 = \frac{\Delta^2}{12} \sum_{n=0}^{M-1} (h[n] - h[n-1])^2. \tag{2.24}$$

In order to maximize the SNR, the quantization noise power in (2.24) should be minimized while the constraint in (2.23) is maintained. Using the Lagrange method, the coefficients of the impulse response in (2.22) are calculated as follows:

$$h[n] = \frac{1}{S}\begin{cases} -n^2 + n(M-1) + M, & 0 \le n \le M-1 \\ 0, & \text{otherwise} \end{cases}, \tag{2.25}$$

where

$$S = \frac{M(M+1)(M+2)}{6} \tag{2.26}$$

provides normalization.

Therefore, the quantization noise power at the output of the optimum filter may be obtained from (2.24), which gives:

$$\sigma_q^2 = \frac{\Delta^2}{M(M+1)(M+2)} \approx \frac{\Delta^2}{M^3}. \tag{2.27}$$

Comparing (2.27) and (2.5) shows that the SNR in the optimum filter is 5.6 dB less than in the ideal filter.

It can be shown that de-normalized coefficients $h[n]$ from (2.25) obey the recurrence

$$h[n+1] = 2h[n] - h[n-1] - 2. \tag{2.28}$$

Therefore, the impulse response of the filter can be generated using a simple sequential logic circuit. Fig. 2.8 shows the block diagram of the coefficient generator. Registers 1 and 2 store $h[n]$ and $h[n-1]$ and are initialized to M and 0, respectively. After one Nyquist interval of M samples, $h[n+1]$ will be zero according to the recurrence. Thus, zero detection may be used to create a reset signal. Registers 1 and 2 will be reset to M and 0, respectively, and the next Nyquist interval will begin. Therefore, no separate reset signal or counter is needed for the decimator. The circuit can be readily implemented in an FPGA or in CMOS technology.

2.3.2 Column and Pixel Decimation

Fig. 2.9(a) shows the decimation architecture in the column-level data conversion. In each column, the coefficients must be multiplied by the modulator output and accumulated. At the end of a Nyquist interval, each accumulator is read out and the accumulator is reset. Since the modulator output is a stream of single bits, multiplication reduces to a logical AND. However, if the bit stream from the modulator drives the clock of the accumulator, even the AND logic is not required. Therefore, the decimation filter is only an

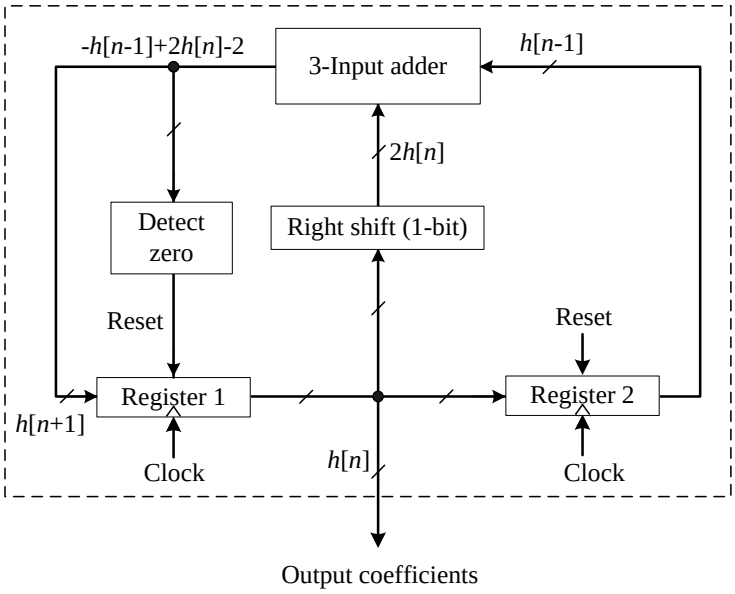


Figure 2.8: Expanded version of the coefficient generator in Fig. 2.9, which is implemented at the chip level. The generated coefficients are sent to each column or pixel.

accumulator for the coefficients coming from the generator located at the chip level, and its clock is the output of the modulator. The accumulated value is read out and dumped every M samples.

The coefficients may be rounded to decrease the size of the accumulator. Simulation shows that to achieve 80 dB of SNR, for example, 10 bits are needed to represent the coefficients, and 19 bits are required to store the value of the accumulator without overflowing. To reduce the area, the addition may be done bit serially. Thus, only a one-bit adder is needed to add the 19-bit accumulator output with a 10-bit coefficient input. Most of the area of the decimator is taken by the two registers, which are implemented using 20 D flip-flops. As discussed in Section 2.2, the IIR-FIR method needs 80-bit registers, half of them working at the oversampling rate.

Decimation in the pixel-level ADC is similar to the column-level ADC. The main difference is that the accumulation is performed serially in the pixel and the registers are implemented using pulsed latches to reduce the area. Fig. 2.9(b) shows a block diagram of the decimator. The coefficients of the FIR filter are sent bit serially to all pixels. In each pixel, an accumulator integrates the coefficients when the modulator output is one. At the end of a Nyquist interval, each pixel is read out and the accumulator is reset.

The accumulator is composed of a one-bit adder, a one-bit register to store the output carry of the adder, and an N-bit register to store the accumulator data. A resettable D flip-flop needs 22 transistors [75]. But using two pulsed latches, a D flip-flop with only eight transistors can be

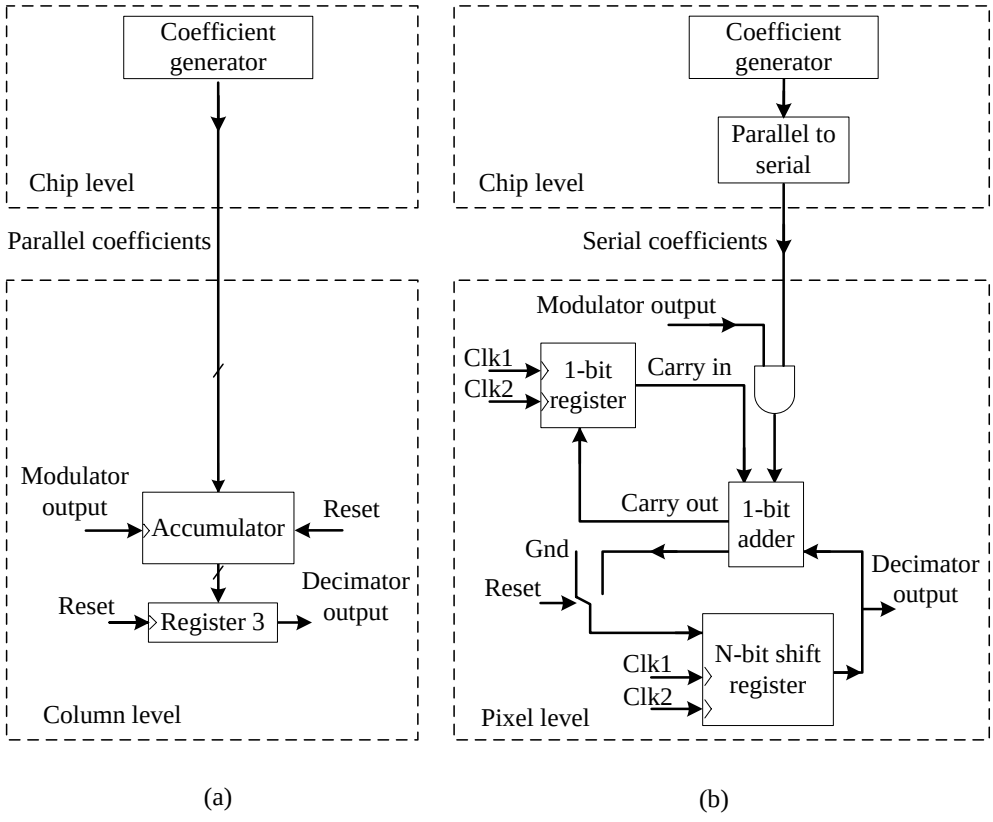


Figure 2.9: (a) The decimator structure in a column-level delta-sigma ADC. (b) The decimator structure in a pixel-level delta-sigma ADC. For both cases, the coefficient generator is at the chip-level.

designed [76]. This structure is shown in Fig. 2.10(a). The number of transistors can be reduced further by using more clocks.

The register, which is made up of multiple D flip-flops in series, may be divided into identical blocks, one of which is outlined by dots in Fig. 2.10(a). Since each transistor in the block has its source or drain shared with another transistor of the same type, the block may be laid out compactly with an area of $2.4\,\mu\text{m}^2$ per transistor. A layout using standard cells occupies almost $8\,\mu\text{m}^2$ per transistor in $0.18\,\mu$m CMOS technology [75].

The pulsed latches are driven by two non-overlapped clocks that are shown in Fig. 2.10(b). These clocks may be generated from the rising and falling edges of the main clock, ϕ_1, in the modulator. As shown in the figure, a PMOS transistor connects the inverter output to its input. Therefore, when the latch output is at GND volts, node A will be stable and connected to node VDD. But when the latch output is at VDD volts, node A will be in a high impedance state that is initially discharged to ground. During the time that the input switch is off, this node will gradually charge up to VDD volts. Circuit simulation shows that it takes at least 2.8 ms to lose the data in the latch. Since the input clock is 1 MHz, there is a negligible probabil-

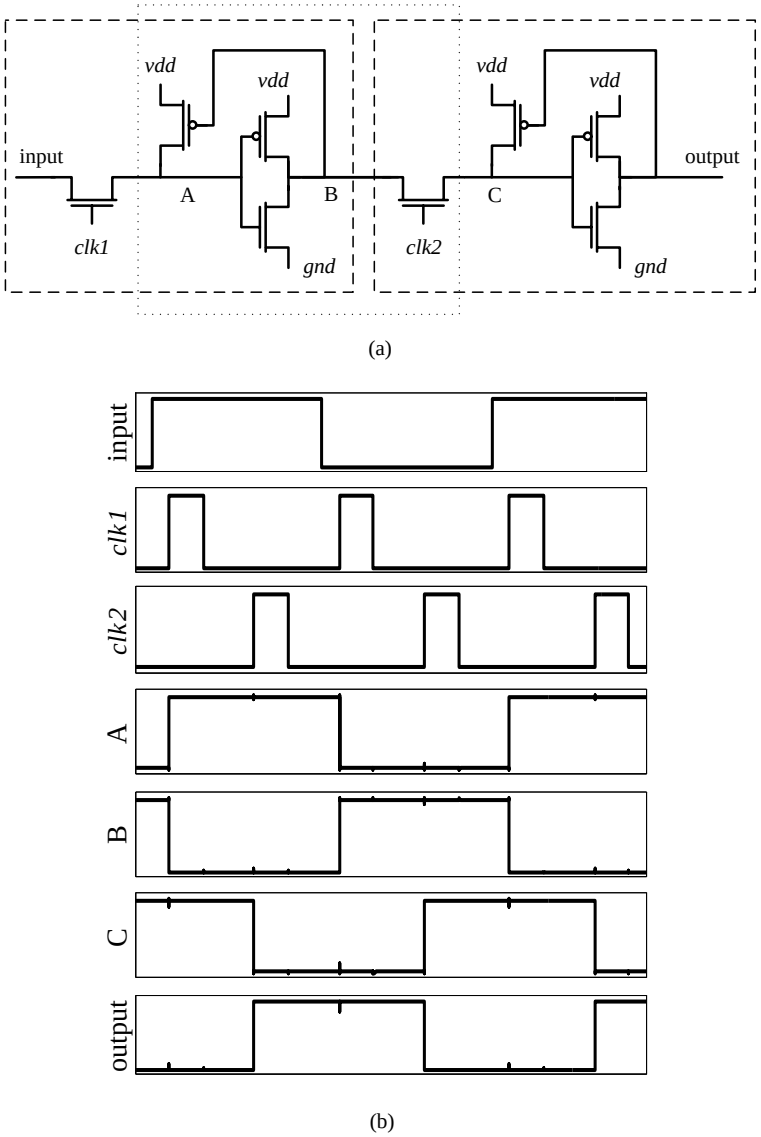


Figure 2.10: (a) Two pulsed latches of a D flip-flop. (b) Circuit simulation.

ity of bit error. However, the circuit is still susceptible to noise. To reduce the noise vulnerability of the circuit, switches must be turned on as long as possible without having any overlap between the pulses.

2.4 Conclusion

In this chapter, the basic concept of delta-sigma ADCs was briefly discussed. Different architectures of delta-sigma ADCs were explained. Conventional methods of decimation for the delta-sigma ADCs, such as recursive (IIR-FIR), non-recursive (FIR2), and polyphase (POLY-FIR2), were compared in terms of power consumption and area usage. Although POLY-FIR2

has the minimum power consumption and IIR-FIR has the smallest area usage, none of them are suitable for parallel decimation mainly because they need a very large area. Thus, the size of the decimator has been a limiting factor in delta-sigma array sensors.

For this reason, a new design flow for decimation was presented, which requires less area for ADC arrays than the prior art, while low power consumption is obtained. The optimum FIR filter is realized at a low complexity; therefore, the decimation is performed more efficiently. When the new architecture is used for column-level data conversion, less die area is used for decimation and a larger pixel array can be fabricated in the same die size. For pixel-level data conversion, the decimator can fit inside a pixel, allowing a higher frame rate, array size, and SNR.

Similar to the decimator, the area and power consumption of the modulator needs to be reduced. In the next chapter, a novel modulator design flow is introduced. In Chapters 4 and 5, experimental results from specific designs will be presented and compared to the state-of-the-art.

Chapter 3

Modulator Design Flow

The role of the modulator is to oversample the input signal and quantize it with a coarse step size. Unlike the decimator, which is purely a digital circuit, the modulator is mostly an analog circuit. Delta-sigma ADCs are well known for their tolerance to component mismatch and circuit nonidealities but this does not mean that the analog circuit of the modulator can be designed without careful analysis. Nonidealities of the analog circuit can affect the performance of the delta-sigma ADC [60], though this issue is more problematic with Nyquist rate ADCs. Some of the nonidealities can be controlled by power consumption. Also, it is always desirable to minimize the power consumption. To do so, it is important to analyze the effects of the nonidealities on performance. Hence, power consumption can be minimized for a desired ADC performance.

In this thesis, the focus is on a first-order architecture since it is very suitable for low-area data conversion. Optimizing the modulator is the most difficult part of the delta-sigma ADC design. Many articles discuss techniques to reduce the power consumption of the modulator [4,60,61,77–80]. However, in these works area is not very critical and, therefore, they use these techniques to design higher-order modulators. Some of these techniques will be used in this chapter. But this chapter primarily introduces a new design flow, which is customized for a first-order system. It is demonstrated that, unlike with higher-order architectures, the first-order modulator can be implemented using very small capacitors.

As area is important in parallel data conversion, this design flow provides an effective method to reduce the area of the circuit. However, one important challenge associated with reducing the modulator area is mismatch in the analog circuitry. Therefore, mismatch must be taken into account in small-area analog circuits. Thus, one important component of the design flow is properly sizing the transistors to avoid performance degradation.

To illustrate the design flow, two specific delta-sigma modulators are designed for use in a logarithmic image sensor at the column and pixel levels. The goal is to realize an image sensor with similar performance to the

human eye.

In Section 3.1, the specifications of the ADCs are derived based on the specifications of the image sensor. In Section 3.2, the architectural considerations of the modulators are discussed. In Section 3.3, a schematic of the circuit is explained and a behavioural model is derived. In Section 3.4, the circuit parameters are determined using a new theoretical model and the behavioural model. Also, circuit simulation is employed to facilitate design. In Section 3.6, the main contributions of this chapter are summarized.

3.1 ADC Specifications

A camera with a performance comparable to the human eye needs to achieve at least 1% contrast sensitivity over a 100 dB dynamic range [81]. This means that the input-referred SNDR of the sensor should be at least 40 dB. Also, the camera should be able to provide a 50 Hz frame rate. The array size is selected to be $1\,\mathrm{k} \times 1\,\mathrm{k}$ pixels, which is in the resolution range of high quality standard displays. The pixel yield is selected to be 95%; dead pixels can be easily corrected using image processing techniques without a noticeable degradation in image quality. Table 3.1(a) gives the desired specifications for an image sensor designed using pixel-level and column-level data conversion.

We choose a logarithmic sensor for the following reasons. The peak SNR of linear CMOS sensors is typically 50 dB, which varies design by design [15], while this value is reported to be 32 dB in logarithmic sensors [81]. On the other hand, linear sensors have a dynamic range of 40–60 dB [15], while logarithmic sensors can achieve more than 100 dB dynamic range [16]. Logarithmic sensors suffer from having high FPN. Based on reported data [20], their peak SNDR is calculated to be 26 dB [20]. Using the methods presented by Joseph and Collins [18], the FPN can be greatly reduced. Using column and pixel-level data conversion, we seek to boost the SNDR/SNR of logarithmic sensors to 40 dB. This will make these sensors a suitable choice for high performance imaging.

The ADCs should be designed such that if they are integrated into the image sensor, the desired performance in Table 3.1(a) is achieved. Therefore, the specifications of each ADC are determined based on the specifications of the image sensor. It should be mentioned that dynamic range of the image sensor is different from dynamic range of the ADC.

Fig. 3.1 shows a noise model of the imaging system. It is assumed that the ADC only adds noise to the system. In a logarithmic sensor, the output voltage y is approximately given by [18]:

$$y = b \cdot \log(x), \tag{3.1}$$

where x is the input light illumination and b is the subthreshold slope. The

Table 3.1:

(a) Specifications of an image sensor.

Parameter	Image sensor
Dynamic range	100 dB
SNDR	40 dB
Frame rate	50 Hz
Array size	1 k × 1 k
Pixel yield	95%

(b) Specifications of the column-level ADC.

Parameter	Theory	Behavioural	Circuit
σ_y	.43 mV	.43 mV	.20 mV
V_{i-pp}	.7 V	.7 V	.7 V
V_{o-pp}	.93 V	.93 V	.93 V
g	1/3	1/3	1/3
DCG	> 31 dB	41 dB	63 dB
SLR	5.9 V/μs	6.5 V/μs	9.5 V/μs
UGB	23 MHz	26 MHz	36 MHz
C_i	60 fF	60 fF	60 fF
C_s	20 fF	20 fF	20 fF
F_s	50 kHz	50 kHz	50 kHz
Power	2.5 μW	2.8 μW	6.7 μW

(c) Specifications of the pixel-level ADC.

Parameter	Theory	Behavioural	Circuit
σ_y	.43 mV	.43 mV	.22 mV
V_{i-pp}	.7 V	.7 V	.7 V
V_{o-pp}	.93 V	.93 V	.93 V
g	1/3	1/3	1/3
DCG	> 31 dB	41 dB	63 dB
SLR	5.3 V/ms	5.9 V/ms	8.68 V/ms
UGB	21 kHz	23 kHz	35 kHz
C_i	60 fF	60 fF	60 fF
C_s	20 fF	20 fF	20 fF
F_s	50 Hz	50 Hz	50 Hz
Power	2.3 nW	2.6 nW	7.6 nW

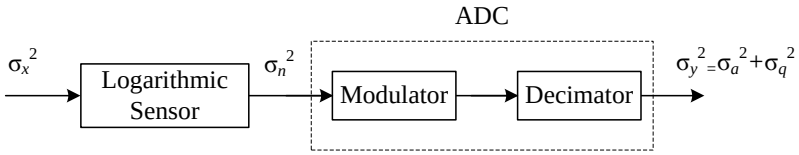


Figure 3.1: Noise model of the logarithmic sensor with delta-sigma ADC.

input-referred SNDR of the sensor is derived from (3.1) to be:

$$SNDR_x = \frac{x}{\sigma_x} = \frac{x}{\frac{dx}{dy}\sigma_y} = \frac{b}{\ln(10)\cdot\sigma_y}, \tag{3.2}$$

where σ_x and σ_y are the standard deviation, respectively, of input and output-referred noise-and-distortion. Assuming a subthreshold slope of 100 mV per decade [81], σ_y should be .43 mV to achieve 40 dB for $SNDR_x$ in the logarithmic sensor. A dynamic range of 100 dB is needed to compete with the human eye, which corresponds to 5 decades of illumination. Using (3.1), the logarithmic sensor output y needs .5 V of dynamic range. Considering the threshold voltage variation in the sensor, a .2 V margin is added to the sensor output. Therefore, the ADC is designed to achieve an output-referred noise less than .43 mV in a .7 V range. The ADC is designed to have low distortion. Therefore, the distortion is smaller than the temporal noise and may be neglected in this calculation.

The image sensor has a 50 Hz frame rate. If there are 1000 pixels per column and 1000 columns, a sampling frequency of 50 kHz for the column-level design and 50 Hz for the pixel-level design is implied. In the pixel-level design, it is critical to minimize the area of the ADC and reduce the pixel size. In the column-level design, the area of all ADCs may be comparable to the area of the pixel array. Therefore, it is important to minimize the area usage of the ADC in both arrays to maximize the number of pixels.

3.2 Circuit Architecture

A first-order architecture was selected because it has a simple circuit and, therefore, is suitable for low-area data conversion. Considering the fact that, in the first-order system, the oversampling ratio is much higher compared to higher-order modulators, one may expect the first-order modulator to have a much higher power consumption. However, because smaller capacitors are used, the power consumption will be significantly reduced. Consequently, it will be comparable to power consumption of higher-order modulators.

In higher-order modulators, mismatch limits the minimum size of the capacitors. This issue is less problematic in the first-order modulator. Therefore, very small capacitors can be used. In higher-order designs, the output

of the first integrator will be subtracted from the DAC output. Therefore, the integrator gain can easily affect the performance. But in the first-order modulator, the integrator output is connected to the quantizer. Hence, integrator gain is not important at this stage. The integrator gain is related to a capacitor ratio. Smaller capacitors have larger mismatch. Any mismatch between the capacitors alters the integrator gain. Unlike the higher-order models, the first-order modulator is not sensitive to the capacitor mismatch. For this reason, small capacitors can be used in the first-order modulator while large capacitors are required in higher-order modulators. Power consumption of the circuit is directly proportional to the capacitor size of the load. Compared to higher-order designs, power consumption of the first-order modulator is reduced using smaller capacitors.

Because of a greater oversampling ratio, the decimator of the first-order architecture has a higher power consumption compared to higher-order designs. But since the area of the first-order ADC is significantly smaller, the first-order architecture was selected for both the column and pixel-level designs.

The ADCs are designed so that the quantization noise power (σ_q^2) is equal to the analog noise power (σ_a^2). Using (2.27), with the first-order modulator and an optimum decimator, the required oversampling ratio is calculated to be 170 in order to achieve the desired input-referred noise.

In the column-level ADC, which has a 50 kHz sampling rate, 20 μs is available to sample each pixel in a column. Circuit simulation shows that a small portion of this interval (3 μs) is enough for the pixel output to settle at the input of the ADC. Thus, there is actually 17 μs available to digitize the output of each pixel. Since the oversampling ratio is 170, the oversampling period of the modulator (T_n) is 100 ns, which should be apportioned between sampling time (T_s) and integration time (T_i). From this total, 50 ns has been alloted to switched-capacitor sampling and the rest to integration. The ratio of integration time to sampling time could be optimized with further circuit simulation.

In the pixel-level ADC, which has a 50 Hz sampling rate, 20 ms is available to sample each pixel. The settling time of the pixel output is negligible. Thus, with an oversampling ratio of 170, 110 μs is available for each sampling interval, which is equally apportioned between sampling time (T_s) and integration time (T_i). Similarly, the ratio of integration time to sampling time could be optimized with further circuit simulation.

3.3 Behavioural Model

In this section, the schematic of the first-order modulator is explained, and based on that, a behavioural model is derived considering the nonidealities of the integrator. This includes the finite DC gain (DCG), unity gain

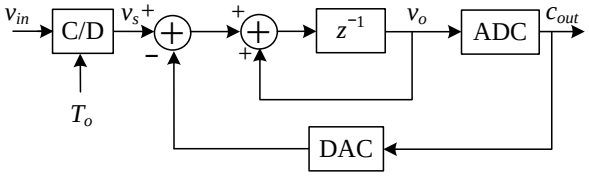


Figure 3.2: Block diagram of a first-order delta-sigma modulator. The modulator is composed of a differencer, an integrator, an ADC, and a DAC.

bandwidth (UGB), and slew rate (SLR) of an operational transconductance amplifier (OTA).

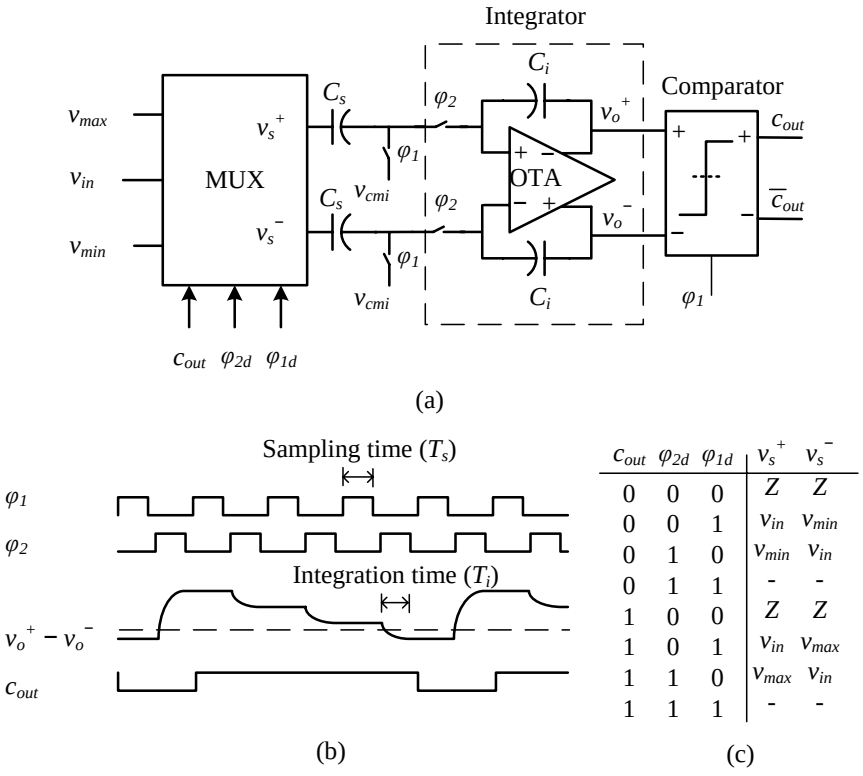
3.3.1 Modulator Circuit

Fig. 3.2 shows a block diagram of the first-order modulator [4]. The modulator is composed of four parts: a differencer, an integrator, an ADC, and a DAC. The ADC is implemented by a one-bit comparator since it offers a high linearity. Therefore, the DAC is also one bit and converts the output of the ADC to two reference voltages.

Delta-sigma modulators can be realized using either a switched-capacitor (SC) or a continuous-time (CT) approach. While CT modulators tend to have a lower power consumption for the same speed, they require area-consuming resistors and are more vulnerable to mismatch variation [77]. For these reasons, we use SC modulators in our design flow. The block diagram is realized using the SC circuit shown in Fig. 3.3(a).

Fig. 3.3(a) gives the modulator schematic of both example ADCs, with an illustration of signal waveforms in Fig. 3.3(b), and the analog multiplexer truth table in Fig. 3.3(c). The DAC and differencer are implemented using an analog multiplexer. A differential architecture is used since it can reject the common-mode noise in the circuit. As the pixel is single ended, the modulator is designed with a single input.

The novel differencer has a single input but differential output. The operation is done in two phases using two non-overlapped clocks—a sampling clock (ϕ_1) and an integration clock (ϕ_2)—together with their delayed versions (ϕ_{1d}, ϕ_{2d}). When ϕ_1 is one, in the upper branch v_{in} is sampled to C_s, while in the lower branch, based on the value of c_{out}, either v_{min} or v_{max} is sampled to C_s. When ϕ_2 is one, in the upper branch, based on the value of c_{out}, the difference between either v_{min} or v_{max} and the voltage of C_s is integrated to C_i, and in the lower branch the difference between v_{in} and the voltage of C_s is integrated to C_i. The differential output of the integrator can be explained with a difference equation, i.e.,



c_{out}	φ_{2d}	φ_{1d}	v_s^+	v_s^-
0	0	0	Z	Z
0	0	1	v_{in}	v_{min}
0	1	0	v_{min}	v_{in}
0	1	1	-	-
1	0	0	Z	Z
1	0	1	v_{in}	v_{max}
1	1	0	v_{max}	v_{in}
1	1	1	-	-

Figure 3.3: (a) Schematic of the first-order delta-sigma modulator. (b) Signal waveforms when v_{in} is close to v_{max}. The output is c_{out}. (c) Truth table of the analog multiplexer. Each oversampling interval includes a sampling time in which C_s will be charged, and an integration time in which C_s will be discharged to C_i.

$$v_o^+[n] - v_o^-[n] = \begin{cases} v_o^+[n-1] - v_o^-[n-1] + \dfrac{2C_s}{C_i}(v_s^+[n-1] - v_{min}),\ c_{out}[n-1] = 0 \\ v_o^+[n-1] - v_o^-[n-1] + \dfrac{2C_s}{C_i}(v_s^+[n-1] - v_{max}),\ c_{out}[n-1] = 1 \end{cases}. \tag{3.3}$$

The comparator output is determined as follows:

$$c_{out}[n] = \begin{cases} 1, & v_o^-[n] \le v_o^+[n] \\ 0, & \text{otherwise} \end{cases}. \tag{3.4}$$

Fig. 3.4 shows the analog multiplexer schematic for the column-level and pixel-level designs. In the column-level ADC, the modulator is working at high speed so switches with very low resistance are needed. Therefore, switches are implemented using transmission gates. In the pixel-level ADC, area is critical. Therefore, switches are implemented using single transistors. Here, the modulator works at very low clock speed, and switches do

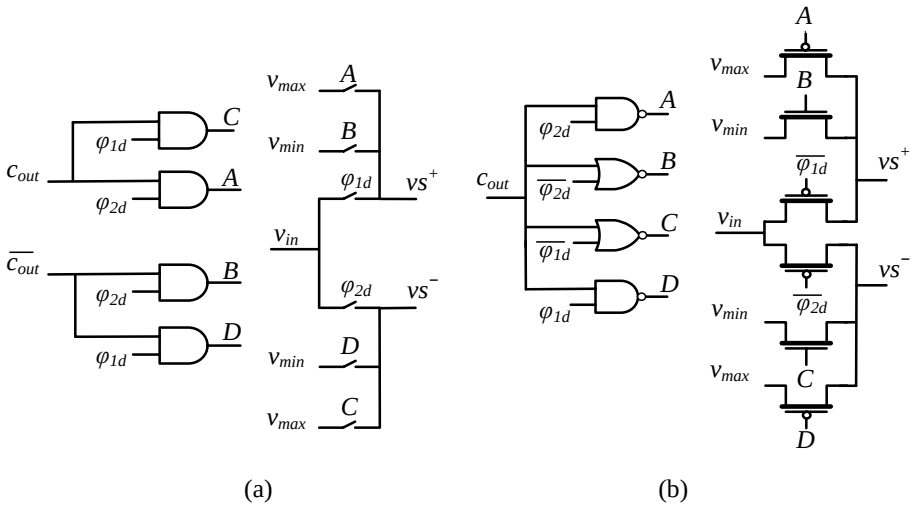


Figure 3.4: Schematic of the analog multiplexer for (a) the column-level modulator and (b) the pixel-level modulator. In the column-level modulator, switches are implemented using transmission gates.

not need to have very low resistance. To save area, switches are implemented using single transistors and, instead of using four AND gates, two NAND and two NOR gates are used.

The output of the quantizer (c_{out}) is also the output of the modulator. The digital parts of the design can be easily implemented. The analog parts must be carefully designed because their nonidealities may limit the overall ADC performance. The integrator is the most critical part of the modulator, while the OTA is the most critical part of the integrator [3]. Nonidealities of the analog circuit create finite UGB, SLR, and DCG for the OTA. This will limit the performance of the integrator. As shown in Fig. 3.5(a), the integrator can be modeled with a time constant and a limited SLR. The main issue in the design is to determine the minimum values of UGB and SLR for the integrator.

Differential integrator output is in the range of $\pm V_{o-pp}/2$. Fig. 3.5(b) shows an example of integrator output when the output is settling to its maximum value $V_{o-pp}/2$ and is slewing for $t < t_0$. The output signal of the integrator can be expressed as:

$$v_o^+(t) - v_o^-(t) = \begin{cases} 2SLR \cdot t, & t \le t_0 \\ \frac{V_{o-pp}}{2} + \left(2SLR \cdot t_0 - \frac{V_{o-pp}}{2}\right)\exp\left(\frac{-(t-t_0)}{\tau}\right), & t_0 \le t \le T_i \end{cases}, \quad (3.5)$$

where SLR is the slew rate of each output branch in the OTA.

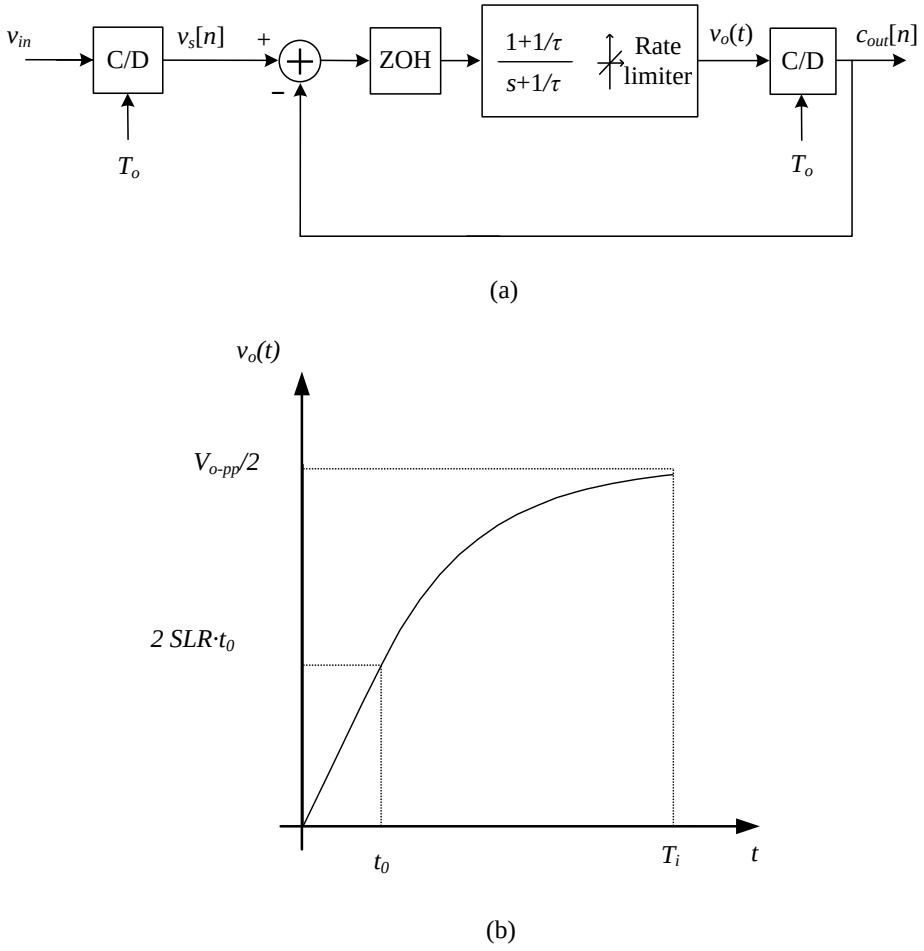


Figure 3.5: (a) Modulator of first-order delta-sigma ADC, using a practical integrator. (b) An example of the integrator output waveform. The output is slewing for $t < t_0$.

3.3.2 Operational Amplifier

Fig. 3.6(a) shows the structure of the main OTA, which is used in the pixel-level ADC. The folded-cascode OTA structure is well known for switched-capacitor applications [82]. In this structure, the input transistors convert the input voltage to I_1 and inject it to the output branch. The drains of transistors P2 and P3 have a high input impedance, while the sources of P4 and P5 have low impedance. Therefore, this current will mostly flow to the output branch. Since the output has very high impedance, a large gain can be achieved at the output nodes (v_o^+, v_o^-). Transistor N7 converts the output voltage of the CMFB circuit to current in order to adjust the common-mode output of the OTA.

If gain of the folded-cascode OTA is insufficient for the ADC, the gain-boosting technique may be employed at the cost of requiring two supplementary OTAs [82]. Fig. 3.6(b) shows the schematic of the OTA using gain

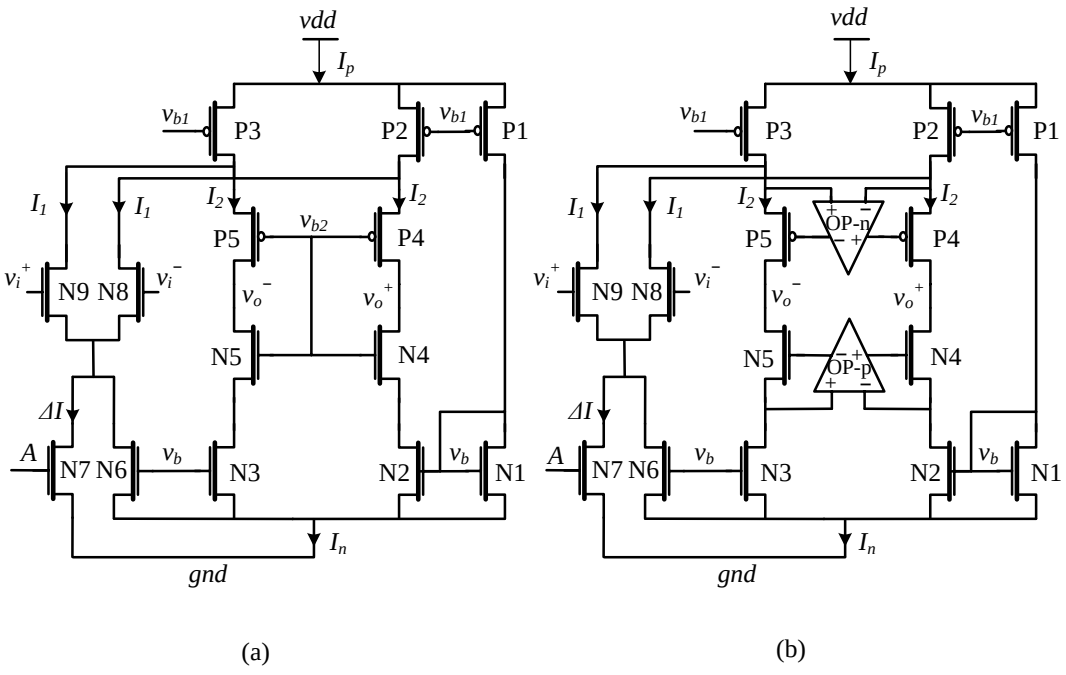


Figure 3.6: (a) Schematic of the folded-cascode OTA without gain boosting. (b) Schematic of the folded-cascode OTA with gain boosting to achieve higher gain. The supplementary OTAs are folded-cascode with NMOS (OP-n) or PMOS (OP-p) input devices.

boosting. This technique can raise two significant problems, i.e., doublets and instability. Thus, zero and pole locations must be designed carefully.

A differential-mode OTA has the advantage of rejecting the common-mode noise but it needs a common-mode feedback (CMFB) circuit to specify the output common mode. Conventional switched capacitor CMFB (SC-CMFB) circuits have high output swing with high accuracy and low static power consumption, and are preferred for switched-capacitor applications [82], but they load the output of the OTA, reducing its UGB and SLR. Also, SC-CMFB circuits occupy a large area.

Instead of SC-CMFB circuits, continuous-time CMFB circuits may be employed to control the common mode of the OTA outputs. Fig. 3.7 shows a continuous-time circuit, which is called a differential-difference amplifier CMFB (DDA-CMFB). Since it can offer enough swing and linearity with a small area, a DDA-CMFB may be used in the main OTA [83]. In this structure, the common mode of the OTA outputs is compared to the voltage v_{cmo}. The difference appears as a voltage at node A (Fig. 3.6 and Fig. 3.7), which controls the common mode of the OTA output by modifying ΔI. A similar CMFB circuit is used for supplementary OTAs, when gain boosting is needed.

The design of the CMFB circuit is similar to the literature [84]. One issue

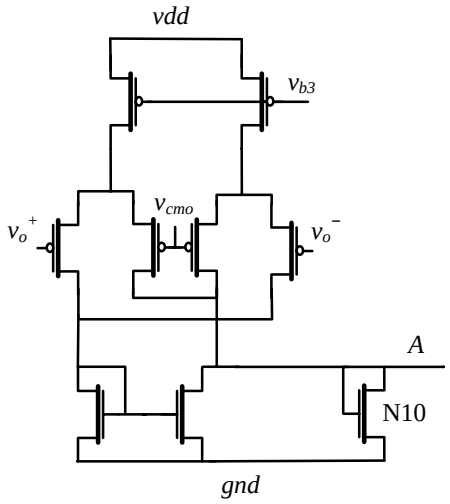


Figure 3.7: Schematic of the differential-difference common-mode feedback circuit, used to set the common mode voltage of the OTA's output to v_{cmo}.

with the original design is that, because of a very high impedance, node A will contribute a pole at low frequency. Together with the pole at the output of the OTA, which is again at low frequency, they cause an oscillation in the common mode. To fix this issue, N6, and N8 are added to the circuit. N8 is a diode-connected transistor, which will reduce the impedance of the output node; therefore, the associated pole is moved to higher frequency and the oscillation is reduced. To decrease the oscillation further, the loop gain of the CMFB must be minimized; therefore, N7 should provide the minimum current. Transistor N6 is added to provide bias current that is required in the OTA input branch, and reduce the current of N7. Reducing the current of N7 will reduce the gain. Also, because N8 is a diode-connected transistor, N7 cannot provide high current but this problem is fixed by adding N6 to the circuit. The amount of the current in N7 must be high enough to compensate for any effect of process or mismatch variations; also, it should have the minimum gain to minimize the CMFB loop gain.

For the example designs, Table 3.2 summarizes the bias voltages in the OTAs. The device size of sensitive transistors are given in the Table 3.3. Other transistors have a minimum size. The OTA of the ADCs were designed based on the specifications derived from theory and behavioural simulation. Since process variation can affect the OTA performance, the OTAs were designed with enough margin to tolerate the process variation. Monte Carlo process simulation was done to ensure the OTAs meet the specifications in spite of process variation. However, we did not simulate mismatch variation as the design kit did not provide mismatch data.

Table 3.2:

(a) Bias levels in the column-level ADC.

Node	Voltage	Node	Voltage
v_{cmi}	1.1 V	v_{cmo}	.75 V
v_{min}	.70 V	v_{max}	1.4 V
v_{b1}	1.1 V	v_{b2}	.75 V
v_{b3}	1.3 V		

(b) Bias levels in the pixel-level ADC.

Node	Voltage	Node	Voltage
v_{cmi}	1.1 V	v_{cmo}	.75 V
v_{min}	.70 V	v_{max}	1.4 V
v_{b1}	1.5 V	v_{b2}	.75 V
v_{b3}	1.5 V		

3.3.3 Comparator

The quantizer was implemented using a one-bit comparator. In the column-level ADC, a regenerative latch was used as the comparator [85], which is shown in Fig. 3.8(a) . The power consumption of the standard circuit is much higher than the power consumption of the pixel-level decimator. When ϕ_1 is high, the circuit drives a large current. To make it suitable for pixel-level ADC, power consumption of the comparator must be reduced. To do so, transistors Q1, Q2, and Q3 are added to each branch to limit the current of each branch. In this way, the power consumption is reduced at the cost of lower speed, which is still enough for pixel-level ADC. Fig. 3.8(b) shows a schematic of the comparator for pixel-level ADC. The required bias voltage v_b is provided by the OTA.

3.4 Circuit Parameters

In this section, a theoretical model for the first-order modulator is introduced. Specifications of the analog circuit are derived using this model and the behavioural model presented in the previous section. Also, circuit simulation is performed to confirm the theoretical and behavioural models. Table 3.1(b) and 3.1(c) show the circuit parameters for column and pixel-level ADCs derived from theory, as well as behavioural and circuit simulation.

Behavioural simulation using Simulink has been done in other works [77–80]. The behavioural model presented here precisely models the slewing in the integrator. Also, the other circuit nonidealities are considered in the model. Using a finite number of input samples, the developed model is used to calculate the output-referred noise.

In the theoretical model, the effect of each nonideality is modeled as a

Table 3.3:

(a) Device sizes in the column-level ADC.

Device	W/L	Device	W/L
N1	2.0 μm/4.8 μm	P1	2.0 μm/5.0 μm
N2	2.0 μm/5.0 μm	P2	2.0 μm/2.5 μm
N3	2.0 μm/5.0 μm	P3	2.0 μm/2.5 μm
N4	3.0 μm/.18 μm	P4	3.0 μm/.40 μm
N5	3.0 μm/.18 μm	P5	3.0 μm/.40 μm
N6	2.0 μm/2.5 μm	N7	2.0 μm/.18 μm
N8	1.0 μm/.18 μm	N9	1.0 μm/.18 μm

(b) Device sizes in the pixel-level ADC.

Device	W/L	Device	W/L
N1	.75 μm/5.3 μm	P1	.75 μm/7.5 μm
N2	.75 μm/7.5 μm	P2	.75 μm/3.75 μm
N3	.75 μm/7.5 μm	P3	.75 μm/3.75 μm
N4	1.0 μm/.50 μm	P4	2.0 μm/1.0 μm
N5	1.0 μm/.50 μm	P5	2.0 μm/1.0 μm
N6	.75 μm/3.75 μm	N7	2.0 μm/.18 μm
N8	1.0 μm/.18 μm	N9	1.0 μm/.18 μm

noise source and is referred to the input of the ADC. The circuit parameters are designed so that the total noise contribution does not exceed the maximum allowed input-referred noise of the ADC, an approach that has not been used before. Input-referred noise is related to output-referred noise, which was specified in Section 3.1.

Modulator design involves determining the differential peak-to-peak - range of the OTA output (V_{o-pp}), the integrator gain (g), the integrating capacitance (C_i), the sampling capacitance (C_s), the time-constant of the integrator (τ), the UGB and SLR of the OTA, and the OTA bias currents. Not all of these are independent.

In the first-order modulator, the differential output range of the integrator with unity gain is four times the single input range of the modulator. The gain is also a capacitance ratio [3], i.e.,

$$g = \frac{C_s}{C_i} = \frac{V_{o-pp}}{4V_{i-pp}}, \tag{3.6}$$

where V_{i-pp} and V_{o-pp} are the modulator input range and the integrator output range, respectively.

A higher integrator gain increases the required voltage range of the OTA and, as will be explained, reduces the kTC noise. For the latter, it is desired to maximize the gain. Circuit simulation shows that the maximum output voltage range of the OTA for this design is .6V with 20% (.12V) deviation budgeted for mismatch in the OTA. Therefore, the integrator gain is chosen

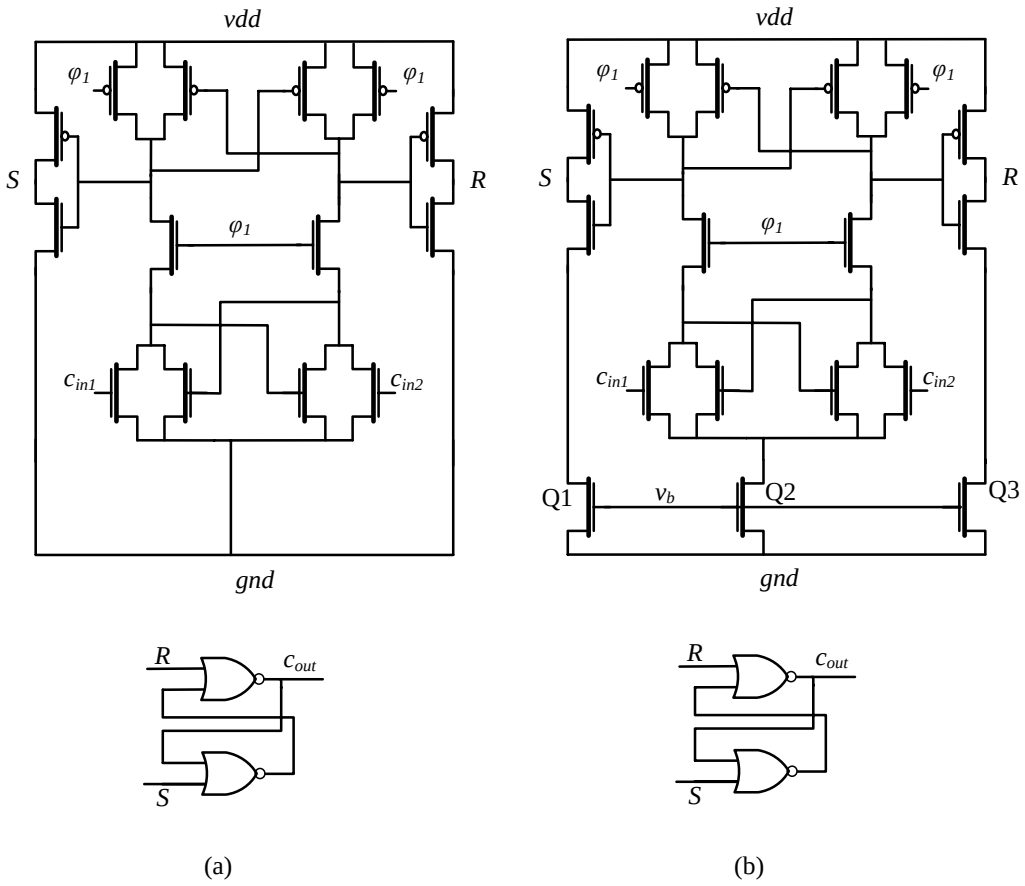


Figure 3.8: (a) Schematic of the comparator in the column-level ADC. (b) Schematic of the comparator in the pixel-level ADC. The outputs of the OTA are c_{in1} and c_{in2}, which are inputs here.

to be 1/3 for both ADC examples. A .13 V margin is added to the .47 V voltage range, giving a .6 V figure (round number), to compensate for mismatch in the OTA and integrator gain variation due to capacitor mismatch.

There are different sources of nonidealities in the modulator. Some of them, such as finite DCG, finite UGB, and finite SLR, cause a settling error in the integrator. These sources contribute distortion because they depend on the input signal. Other nonidealities, such as kTC noise, thermal noise, flicker noise, clock jitter, clock-feedthrough, nonlinear on-resistance of switches, charge injection, and comparator offset [77] contribute random noise. Measures must be taken to reduce the noise and distortion in the output signal to achieve the desired specifications.

In the example designs, as will be explained, the integrator settling error is the dominant nonideality for both ADCs. Using techniques described below, the other sources would be smaller than a threshold level and, therefore, they are negligible. The settling error must be reduced to the order of the random noise for this distortion to be negligible.

3.4.1 Input-Referred Noise

The output signal of a delta-sigma modulator is equal to its input signal plus filtered quantization noise. Assume that the total input-referred noise of the ADC is white with power σ_n^2. Then the filtered analog noise power at the ADC output σ_a^2, which together with the filtered quantization noise σ_q^2 determines the performance, depends on a (causal) decimation filter $h[n]$ according to Parseval's theorem, i.e.,

$$\sigma_a^2 = \sigma_n^2 \sum_{n=0}^{\infty} |h[n]|^2. \tag{3.7}$$

As discussed in Chapter 2, the optimal FIR decimation filter of the first-order delta-sigma ADC, over a Nyquist interval of M samples with input DC signal, has a parabolic impulse response, i.e.,

$$h[n] = \frac{1}{S} \begin{cases} -n^2 + n(M-1) + M, & 0 \le n \le M-1 \\ 0, & \text{otherwise} \end{cases}, \tag{3.8}$$

where

$$S = \frac{M(M+1)(M+2)}{6}. \tag{3.9}$$

For large M, it can be shown using the above equations that the analog noise of the output is given to a good accuracy by

$$\sigma_a^2 = \frac{6}{5M}\sigma_n^2. \tag{3.10}$$

The total output-referred noise-and-distortion of the ADC is a summation of the analog noise σ_a^2 and the quantization noise σ_q^2, i.e.,

$$\sigma_y^2 = \sigma_a^2 + \sigma_q^2. \tag{3.11}$$

Assuming that the analog noise power σ_a^2 is equal to the quantization noise power σ_q^2, the input-referred noise σ_n^2 of the ADC is given by

$$\sigma_n^2 = \frac{5M \cdot \sigma_y^2}{3}. \tag{3.12}$$

As discussed in Section 3.1, the ADC is designed with the output-referred noise-and-distortion σ_y equal to .43 mV. Using (3.12), σ_n should be less than 7.2 mV in order to meet the specifications. Given that there are multiple uncorrelated noise sources in the modulator, for both of the ADCs, the total input-referred noise power should be less than σ_n^2.

3.4.2 Capacitor Size

To minimize the power consumption, capacitances should be minimized. However, smaller capacitors have larger mismatch and, therefore, lead to higher gain error in the integrator. They also create more kTC noise. The first-order structure is not sensitive to capacitance mismatch and the resulting gain error. Therefore, the minimum value for the capacitances in the integrator is determined by kTC noise. Assuming that kTC noise from different capacitors are uncorrelated, and the integrator gain is 1/3, the total kTC noise power referred to the input can be determined, i.e.,

$$\sigma^2_{n-kTC} = \frac{2kT}{g^2 C_i} + \frac{2kT}{gC_i} = \frac{24kT}{C_i}. \tag{3.13}$$

The total kTC noise must be less than σ_n^2. Thus, the minimum theoretical value for the integrating capacitance C_i is 5.7 fF, which means the minimum theoretical value for the sampling capacitance is 1.9 fF. On the other hand, the capacitors should be larger than parasitic capacitors. Also they should have small mismatch. Metal-insulator-metal (MIM) capacitors have a high capacitance with low mismatch despite a small area. Therefore, they are a good choice for this design.

The minimum MIM capacitor size in the process that we used was 20 fF. Therefore, the sampling capacitor is designed to be 20 fF. The integration capacitor is selected to be 60 fF to achieve the gain of 1/3. These are both greater than the theoretical values, leaving enough margin to account for any mismatch in the capacitors. Therefore, kTC noise is negligible compared to σ_n^2 for the example ADC designs.

3.4.3 DC Gain

Since input-referred noise of the ADC and oversampling ratio are the same for both example ADCs, the required DCG is the same. The finite DCG of the OTA introduces gain error and leakage in the integrator. Although gain error of the integrator is not a serious problem in a first-order modulator, leakage can greatly affect the output SNR. The differential output range of the integrator is V_{o-pp}. In a simple model, the leakage could be modeled as uniformly-distributed noise over the voltage range (V_{o-pp}/A), where A is the OTA gain. Variance of this error should be less than σ_n^2. This suggests that the OTA gain should be higher that 31 dB. The OTA of Section 3.3.2 can easily achieve a high DCG at no power consumption cost. Therefore, the DCG is designed to be high enough so that the leakage error is negligible compared to σ_n^2.

An integrator with leakage was simulated to determine the required DCG of the OTA for the example ADCs. The simulation results showed that a gain of at least 41 dB was needed to achieve the desired input-referred

noise. Nonlinearity effects of the OTA are difficult to analyze [77,86]. But as long as the overall DCG of the OTA, including nonlinearity, is higher than the desired threshold, the performance will not degrade. This was confirmed by circuit simulation. Differences between theory and behavioural simulation may occur because the integrator leakage may not correspond exactly to uniformly-distributed noise.

3.4.4 Settling Error

Since the example ADCs function at different clock speeds, their OTAs have different UGB and SLR. For each case, the OTA is optimized to have minimum power consumption with enough UGB and SLR so that the settling error is less than the threshold. Therefore, given the integration period (T_s), capacitor sizes (C_i, C_s), and output range of the integrator (V_{o-pp}), the optimum values for UGB and SLR must be determined.

Assuming a single dominant pole (ω_1) for the OTA, the UGB of the integrator when responding to a step input is given by [3]

$$UGB \approx \frac{A}{\tau}, \tag{3.14}$$

where

$$A = \frac{1}{2\pi}\left(1 + \frac{C_s}{C_i}\right). \tag{3.15}$$

Also, assuming the UGB is mainly determined by DCG and the single dominant pole ($\omega_1 = r_o C_i$) of the OTA, the UGB is determined by

$$UGB = DCG \cdot \omega_1 = \frac{g_m}{r_o}\frac{r_o}{C_i} = \frac{2I_1}{C_i \cdot V_{od}}, \tag{3.16}$$

where g_m is the transconductance of the input stage, r_o is the output resistance, and V_{od} is the overdrive voltage of the input transistors in the OTA.

The SLR of the OTA is given by

$$SLR = \frac{\min(I_1, I_2)}{C_i}, \tag{3.17}$$

where I_1 and I_2 are the currents of the input and output branch. For a certain value of UGB, in order to maximize the SLR, I_1 and I_2 should be equal. Using (3.14) and (3.16), (3.17) can be rewritten, i.e.,

$$SLR = \frac{I_1}{C_i} = \frac{V_{od} A}{2\tau}. \tag{3.18}$$

To ensure no slewing at the OTA output, the SLR should be greater than the maximum possible slope at the integrator output, which is $V_{o-pp}/2\tau$.

Considering τ in (3.14), the UGB should be less than $2A \cdot SLR/V_{o-pp}$ to avoid slewing. On the other hand, using (3.14) and (3.18), it can be shown that

$$UGB = \frac{2SLR}{V_{od}}. \tag{3.19}$$

For reasonable values of A and V_{od}, it is impossible to avoid slewing.

The optimum solution in the OTA design is to have slewing at the OTA output, which is compensated by a reasonable UGB and corresponding τ. In (3.5), because the derivative of $v_o^+(t) - v_o^-(t)$ is continuous at $t = t_0$, we require:

$$SLR = \frac{V_{o-pp}/2 - 2SLR \cdot t_0}{2\tau}. \tag{3.20}$$

Let the parameter N be defined as:

$$N = \frac{T_i - t_0}{\tau}. \tag{3.21}$$

Using (3.20) and (3.21), the time constant of the integrator can be determined as follows:

$$\tau = \frac{-2SLR \cdot T_i + V_{o-pp}/2}{-2SLR \cdot N + 2SLR}. \tag{3.22}$$

Using (3.18), (3.20), and (3.21), the SLR of the OTA is determined:

$$SLR = \frac{V_{od}A(N-1) + V_{o-pp}/2}{2T_i}. \tag{3.23}$$

Assuming the integrator output is uniformly distributed in its range, the settling error at the integrator output (differential mode) would be uniformly distributed over $\pm(V_{o-pp}/2 - 2SLR \cdot t_0)e^{-(T_i - t_0)/\tau}$. By referring the integrator output error to the input and comparing it to the threshold level σ_n^2, the maximum settling error and also N can be determined, i.e.,

$$N = \ln\left(\frac{2(V_{o-pp}/2 - 2SLR \cdot t_0)}{\sqrt{12\sigma_n^2}}\right). \tag{3.24}$$

Using (3.21)–(3.24), N, SLR, τ, and t_0 can be derived iteratively. The equations can be solved using a few iterations starting with t_0 equal to zero. The values converge after a few iterations. Thereafter, UGB is calculated using (3.19). For example, with the column-level ADC, the SLR and UGB are calculated to be 5.9 V/ms and 23.0 MHz. With the pixel-level ADC, these parameters are calculated to be 5.3 V/ms and 21.2 kHz. Using (3.18), the current in each branch of the OTA may be determined. Considering that power consumption is mostly determined by this current, an estimation of

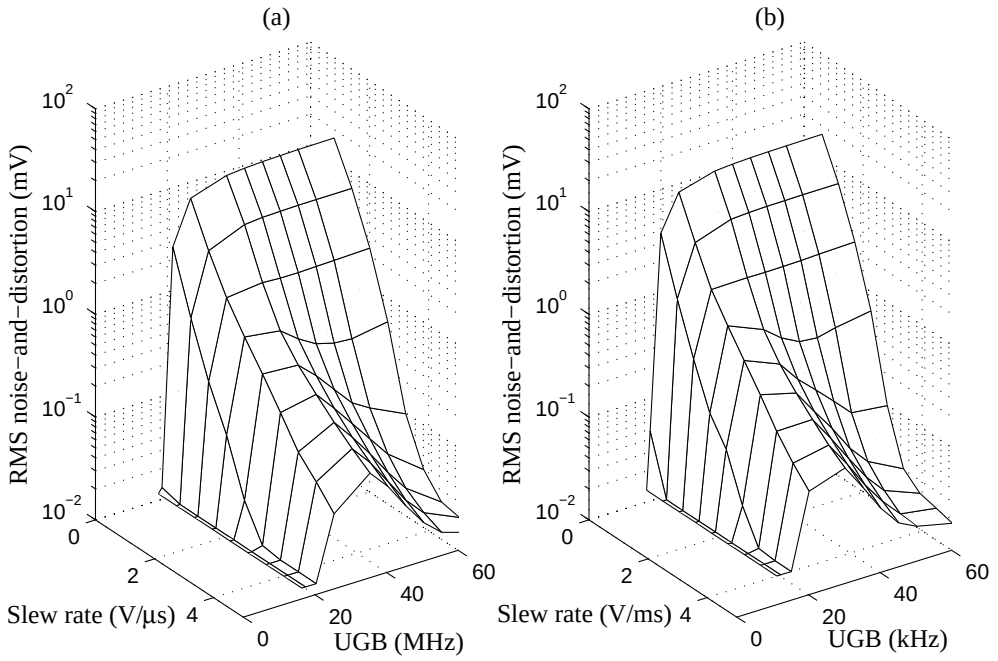


Figure 3.9: RMS noise-and-distortion versus SLR and UGB of the OTA for (a) the column-level ADC and (b) the pixel-level ADC. The simulation is done using the behavioural model with 50 uniformly-distributed samples.

power consumption is obtained. However, other parts of the circuit will also add to the power consumption.

Using the behavioural model, an ADC having an integrator with slewing and limited UGB was simulated. The ADC was tested with 1000 samples, which were uniformly distributed over the input range. As shown in Table 3.1(b), for the column-level example, the minimum values for SLR and UGB are 6.5 V/μs and 26.0 MHz, respectively, to achieve the required σ_y. These parameters for pixel-level ADC are 5.9 V/ms and 22.5 kHz, as shown in Table 3.1(c). The difference between theory and behavioural simulation is because the integrator output is not exactly uniformly distributed. Also a limited number of samples were simulated. However, the theory resulted in good estimates of UGB and SLR.

Using the behavioural model, the effect of varying the UGB and SLR on RMS noise-and-distortion σ_y was simulated in both ADC examples. Fig. 3.9 shows the RMS noise-and-distortion versus UGB and SLR. In both cases, for high values of SLR, σ_y is not sensitive to UGB. It is because a smaller UGB, which corresponds to a larger time constant, only reduces the integrator gain. As discussed before, the first-order modulator is not sensitive to the integrator gain. Therefore, as long as there is no slewing, σ_y is not sensitive to UGB. Also, for small values of UGB, σ_y is small and independent of SLR.

Because slewing does not happen, varying the UGB only affects the integrator gain. Therefore, the performance is not affected by the SLR. In practice, a high SLR implies a high UGB; it is impossible for the OTA to have high SLR with low UGB. Therefore, the OTA is designed with high enough SLR and UGB to meet the required σ_y.

3.4.5 Other Nonidealities

Thermal or flicker noise may also be present at the OTA input. The thermal noise of a long-channel MOS device can be modeled by a voltage source in series with the gate and having a power spectral density (PSD) of [82]

$$\overline{V_n^2(f)} = \frac{4kT\gamma}{g_m}, \tag{3.25}$$

where k is Boltzmann's constant, T is temperature, and γ is 2/3 for a long-channel device. The flicker noise of one transistor can also be modeled as a voltage source in series with its gate, with a PSD of [82]

$$\overline{V_n^2}(f) = \frac{F}{C_{ox}WL} \cdot \frac{1}{f}, \tag{3.26}$$

where W and L are the width and length of the transistor and F is a process-dependent constant on the order of 10^{-25}. Even using minimum-size transistors with an overdrive voltage of .2 V, one can ensure that the thermal and flicker noise of input transistors in the OTA are much less than the threshold and, therefore, will not degrade the performance of the ADC. Consequently, no correlated double-sampling circuit is needed to alleviate the flicker noise.

For both of the example ADCs, kTC noise, thermal noise, and flicker noise were simulated by adding a noise source at the input of the modulator in the behavioural model. To accurately simulate the output range of the OTA, the output of the integrator is limited using a saturation block.

Nonidealities due to the switches are mostly nonlinear resistance, clock feedthrough, and charge injection [3]. A differential-mode integrator will greatly attenuate the common-mode noise, thereby decreasing the effect of charge injection and clock feedthrough. Transistors must be large enough so that the nonlinearity of their on-resistance does not affect the settling behavior. This is assured by circuit simulation.

The effect of clock jitter in the ADC is mostly a variation in the sampling time of the analog input signal [77]. This issue is more problematic when the oversampling ratio is small and the signal varies during the oversampling period. In both examples, the input signal does not have a rapid change during the oversampling interval and so the performance is not affected by clock jitter.

Noise and distortion due to circuit nonidealities occurring after the integrator will be greatly attenuated when referred back through the integrator. Therefore, nonidealities of the comparator used to implement the one-bit quantizer can be widely tolerated. A comparator offset would change the signal range that is fed back in the delta-sigma loop to the integrator. As long as there is enough voltage range at the integrator input, this offset will not degrade performance. It is taken into account by adding a .13 V margin to the .47 V voltage range, as previously specified. Circuit simulation shows that comparator hysteresis must be less than .1 V.

3.5 Mismatch Considerations

In the previous section, using the theoretical model together with behavioural and circuit simulations, circuit parameters of the modulator were determined. Since the ADC is designed for minimum area, transistors are sized for minimum area in general. However, as explained below, some minimum transistor sizes must be determined by mismatch considerations.

For the example ADCs, the OTA is designed for minimum area. With the pixel-level ADC, it is important to reduce the area as it limits the pixel size. With the column-level ADC, the ADC array would occupy a considerable portion of a chip. By saving this area, there would be more space for pixels, and a larger pixel array is achievable.

The major constraint for small area is mismatch because smaller transistors are more susceptible to device mismatch. Mismatch creates variation in the OTA bias point in the example ADCs and, therefore, it modifies the modulator performance. The OTA must be designed with enough tolerance to this variation.

Transistors N1–4 and P1–3 in the OTA (Fig. 3.6) are more sensitive to variation, compared to the other transistors, because there is a high gain from their gate voltage to the OTA output. Therefore, these transistors should be sized carefully. Their mismatch could be divided into two parts—common mode and differential mode. Differential-mode mismatch does not affect performance because the ADC can easily correct it. The integrator output is forced to oscillate around the common mode. Therefore, any initial difference between outputs will be canceled after a few clock cycles.

To simulate common-mode mismatch, a voltage source was added to the gate voltage of transistors P1–3, and RMS noise-and-distortion σ_y was calculated. The voltage represents a variation in threshold voltage (V_t). Fig. 3.10 shows the RMS noise-and-distortion versus this voltage. The simulation may be divided into two regions. In the first region, the V_t variation is less than 3 mV. Here, the CMFB circuit compensates for any current difference between the upper and lower branches of the OTA, and the OTA remains at the proper bias point. In the second region, the current difference is more than what the CMFB circuit tolerates. Therefore, the OTA bias

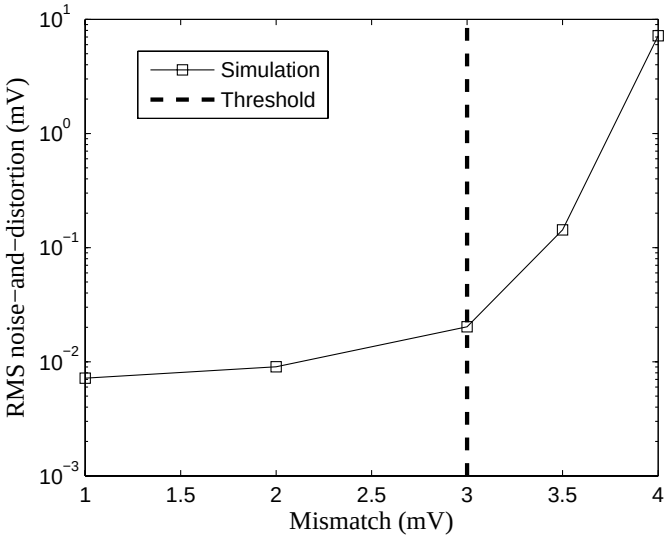


Figure 3.10: Effect of common-mode mismatch on RMS noise-and-distortion of the ADC. The oversampling ratio is set to 1024.

point changes. This reduces the DCG, UGB, and/or SLR of the OTA, which degrades the performance. To avoid this problem, the CMFB should be designed with maximum tolerance, and the OTA should be designed with small enough mismatch. This means the transistor sizes should be large enough and the transistor layouts should be carefully done.

The CMFB circuit should be optimized to tolerate the mismatch as much as possible. This may be done by increasing the CMFB gain. Higher gain in the CMFB causes more nonlinearity in the OTA and more oscillation in the common mode of the OTA. Therefore, there is a limit for CMFB gain.

Mismatch in the OTA may be controlled by the transistor sizes and layouts. Transistor sizes are determined based on the maximum tolerable mismatch in the circuit. As shown in Fig. 3.6, the CMFB circuit provides the current difference ΔI between the up branch (I_p) and down branch (I_n), i.e.,

$$\Delta I = I_p - I_n. \tag{3.27}$$

As long as the CMFB provides enough current, the OTA is working in the proper region and the ADC performance is high. Assuming that ΔI has a zero-mean Gaussian distribution, its standard deviation should be less than some constant $2\sigma_I$ to achieve 95% pixel yield.

Currents of each branch in the OTA can be determined as follows [82]:

$$I_{n(p)} = \frac{\mu_{n(p)} C_{ox} W (V_{gs} - V_t)^2}{2L}. \tag{3.28}$$

Assuming that the dominant variation in the current comes from the variation of threshold voltage, current variation may be expressed in terms of

threshold voltage variation:

$$\sigma_I = \frac{dI}{dV_t}\sigma_{V_t} = \frac{2I}{(V_{gs} - V_t)}\sigma_{V_t}. \tag{3.29}$$

The threshold voltage variation of MOS transistors may be expressed in turn as a function of their size [82]:

$$\sigma_{V_t} = \frac{B}{(WL)^{1/2}}, \tag{3.30}$$

where B is a constant that depends on the process. Using circuit simulation, the maximum value of ΔI that the CMFB circuit can provide with tolerable nonlinearity and negligible oscillation is determined. Based on that, the minimum transistor size WL may be found:

$$\Delta I < \frac{20.52I}{(V_{gs} - V_t)(WL)^{1/2}}. \tag{3.31}$$

In order to avoid the undesired mismatch effects, transistors N1–4 and P1–3 should be designed with their width times length equal to the derived minimum size. Using this technique, an OTA may be designed to meet the required specifications without wasting layout area. Because the above theory involves some approximations, circuit simulation is needed for verification. Some adjustments may be required. Also, layout design techniques should be used to reduce the mismatch effect further [82].

3.6 Conclusion

In this chapter, a new design flow for designing a first-order delta-sigma modulator was presented. The design flow was used to design two example ADCs, one with specifications for column-level data conversion, and the other with specifications for pixel-level data conversion. Unlike with higher-order modulators, very small capacitors can be used with the first-order modulator. Therefore, a very small ADC with low power consumption can be designed. This method of design differs from the state-of-the-art, which mostly concerns higher-order modulators.

The design flow includes a theoretical model together with behavioural and circuit simulation. In the theoretical model, all the nonidealities of the analog circuit are referred to the input. Circuit parameters are determined to ensure that the total input-referred noise is less than the threshold level. Using the behavioural model, nonidealities were simulated with Simulink and the optimal value for each parameter was determined. A circuit may be designed with the parameters derived from theory and the behavioural model. Circuit simulation was employed to confirm and refine the design.

This design flow also presents a method to reduce the transistor size without violating a specified mismatch tolerance. Thus, one can use this design flow to design a modulator based on given specifications that reduces area usage and also possesses low power consumption.

In the next chapter, experimental results of two fabricated ADCs are presented. They were designed using an incomplete version of the design flow in this chapter. As will be demonstrated, the theoretical and behavioural models of the completed modulator design flow correspond to and account for the experimental results.

Chapter 4

Data Converter Advances

In this chapter, we describe how two ADC arrays with specifications of column and pixel-level data conversion were designed, fabricated, and tested. The ADCs are significantly smaller than state-of-the-art delta-sigma ADCs but have comparable figures of merit. This makes them very suitable for use in column or pixel-level data conversion. The pixel-level ADC is the first to integrate in-pixel decimation. Performance of the ADCs is explained using the completed modulator design flow presented in Chapter 3.

Although the ADCs are designed to be used in an image sensor, at this stage the ADCs are stand-alone and their inputs are not connected to a photodetector. Instead, a voltage source is used as the input to the ADCs. Using a ramp input signal, ADC performance was measured. This includes output RMS noise, output RMS noise-and-distortion, and dynamic range for a certain sampling rate and power consumption, which are the key parameters that would limit the performance of an image sensor.

In Section 4.1, the architecture of the fabricated chip is explained. The test platform is discussed in Section 4.2. This includes the printed circuit board (PCB) design, interfacing of the PCB to a PC, the FPGA program, and the method of performance measurement. Later, in Section 4.2.2, test results of both ADCs are presented. Results are discussed further, in Section 4.3, using the theoretical and behavioural models of Chapter 3. The main results of this chapter are summarized in Section 4.4.

4.1 Fabricated Designs

Fig. 4.1 shows a micrograph of the chip fabricated in 0.18 μm standard CMOS technology. The chip occupies an area of $1930 \times 930\,\mu\text{m}^2$, including the bond pads, and has 11,540 transistors. Two converters, one with specifications for column-level data conversion and the other with specifications for pixel-level data conversion, were designed and fabricated. These specifications are not the same as the modulator designed in Chapter 3. At the time that the modulators were being prepared for fabrication, the de-

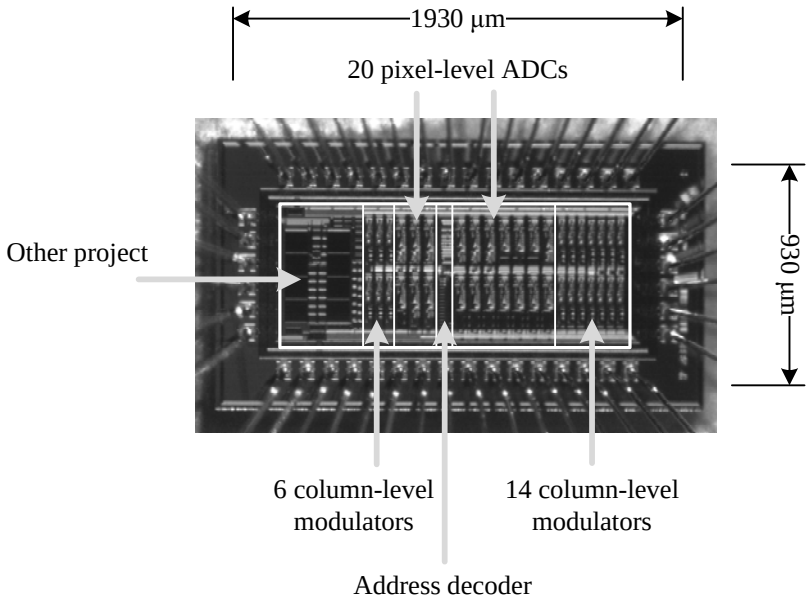


Figure 4.1: Micrograph of the fabricated chip containing a column-level modulator array and a pixel-level ADC array. Using an address decoder, each of the converters may be turned on and their outputs may be read out.

sign flow was incomplete. As a result, the desired RMS noise was chosen to be .064 mV for both cases, instead of .43 mV.

Fig. 4.2 shows a block diagram of the chip. The chip has an array of 20 column-level modulators and an array of 20 pixel-level ADCs. Using a 5:32 decoder inside the chip, ADCs could be selected. To measure the power consumption of groups of ADCs, several of them could be turned on at the same time. 7 pixel-level ADCs are only used in groups to measure the power consumption per ADC, and 13 of them are used for performance measurement. Two versions of pixel-level ADCs were designed, 9 of one type and 4 of another, for the 13 ADCs used for performance measurement. Similarly, 4 column-level ADCs are only used in groups to measure the power consumption per ADC, and 16 of them are used for performance measurement.

As shown in Fig. 4.2(b), the decimator of the column-level ADC was not fabricated. Instead, the decimation was performed in a field-programmable gate array (FPGA). The sampling clock of the modulator, ϕ_1, was generated in the FPGA and was sent to the chip. Other clocks, i.e., the integration clock, ϕ_2, and delayed clocks (ϕ_{1d}, ϕ_{2d}), are generated inside the chip, based on ϕ_1, using clock buffer circuits. The required delay is generated using inverters with capacitive load. Via a digital buffer, the digital output of the modulator is sent to the FPGA. The decimation is performed in the FPGA. Decimator output is stored in a first-in first-out (FIFO) buffer. Using the universal serial bus (USB) interface, the buffer is periodically read out

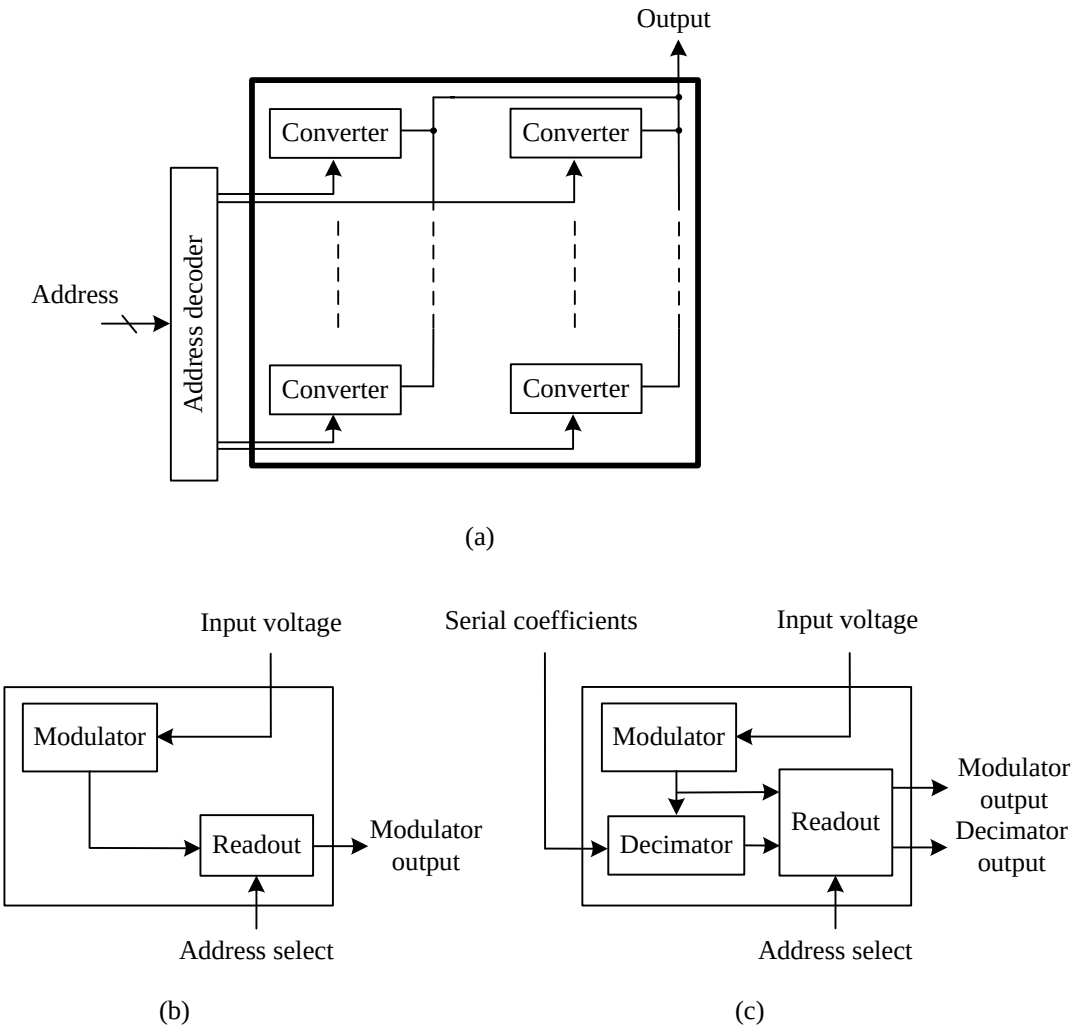


Figure 4.2: (a) Block diagram of the chip containing two types of delta-sigma designs: (b) a column-level modulator, and (c) a pixel-level ADC. Decimation for the column-level design is implemented in an FPGA.

to a PC. ADCs are characterized by processing the captured data in Matlab. Using analog buffers, the OTA outputs are read out for monitoring and testing purposes.

The pixel-level ADC, shown in Fig. 4.2(c), includes the modulator, the decimator, and the readout circuit, which is controlled by the decoder. In this design, ϕ_1, ϕ_2, and their delayed versions (ϕ_{1d}, ϕ_{2d}) are generated off the chip, and other clocks ($\bar{\phi}_{1d}$, $\bar{\phi}_{2d}$) are generated on the chip. Filter coefficients are generated in the FPGA and are sent to the decimator bit serially. Digital outputs of the in-pixel decimator are read out bit serially and are stored in a FIFO buffer. The buffer is periodically read out to a PC using the USB interface. It is also possible to capture the modulator output for monitoring purposes. Using an analog buffer, the output of the OTA is sent

off the chip for testing and troubleshooting purposes.

To save pins, all of the bias voltages and clock signals are shared between the column-level modulators and the pixel-level ADCs. In order to measure the power consumption of each converter, the power supply voltage is connected to each converter via a switch. Thereby, each time only one converter can be turned on, and its power consumption is measured. Power consumption variation among the ADCs is small and negligible.

4.1.1 Circuit Specifications

The design flow for both the fabricated ADCs was similar to the method presented in Chapter 3. However, the design flow was actually completed after testing the chip. Behavioural simulation was done using Simulink. Circuit simulation of the designed ADCs was done for a $0.18\,\mu$m CMOS process. Since a simulation of the whole circuit in Cadence would take a long time, only the modulator was simulated in Cadence and the output bit stream was exported to Simulink for decimation and SNR calculation. One assumes that the digital part of the ADC would work without any degradation in performance. Tables 4.1(a) and 4.1(b) compare specifications of the fabricated modulators derived from theory, behavioural, and circuit simulation, as well as experimental results.

The ADCs were designed and fabricated with similar specifications of the ADCs presented in Chapter 3 except with an output-referred noise of $.064\,$mV instead of $.43\,$mV. Although an oversampling ratio of 500 is enough to achieve this output-referred noise, an oversampling ratio of 1024 was chosen to ensure that quantization noise was not the dominant noise at the ADC output. In this way, the performance derived by experiment measures the performance of the modulator alone.

Using a similar method to what is presented in Chapter 3, the integration time is determined based on the required frame rate and the oversampling ratio. Using the theoretical and behavioural model, specifications of the modulators are determined and are shown in Table 4.1(a) and 4.1(b). In the theoretical and behavioural model, the power consumption is calculated based on the required current at the OTA output branch. This current is determined based on the desired slew rate. Both the theory and behavioural model estimate lower power consumption compared to the circuit simulation because power consumption of the supplementary OTAs, the CMFB circuit, and bias-generating circuits are not considered in the former calculations.

Circuit simulation of the fabricated modulators show a lower output-referred noise since the kTC noise is not simulated in the circuit simulation. Also the circuit was designed based on the incomplete design flow. Therefore, the modulator specifications were somewhat incorrect. Experimental results will be discussed in Section 4.2.1.

Table 4.1:

(a) Specifications of the fabricated column-level modulator, derived from theory, behavioural and circuit simulations, and experimental results. P_{mod} is the modulator power.

Parameter	Theory	Behavioural Simulation	Circuit Simulation	Experimental Results
σ_y	.064 mV	.064 mV	.02 mV	1 mV
V_{i-pp}	.7 V	.7 V	.7 V	.7 V
g	1/3	1/3	1/3	1/3
T_s	7 ns	7 ns	7 ns	$7 \pm .325$ ns
DCG	50 dB	60 dB	90 dB	-
SLR	34 V/μs	34 V/μs	125 V/μs	40 ± 2 V/μs
UGB	345 MHz	347 MHz	300 MHz	190 ± 8.5 MHz
C_i	20 fF	20 fF	20 fF	20 fF
C_s	60 fF	60 fF	60 fF	60 fF
F_s	50 kHz	50 kHz	50 kHz	50 kHz
P_{mod}	15 μW	15 μW	150 μW	79 μW

(b) Specifications of the fabricated pixel-level ADC, derived from theory, behavioural and circuit simulations, and experimental results. P_{mod} is the modulator power.

Parameter	Theory	Behavioural Simulation	Circuit Simulation	Experimental Results
σ_y	.064 mV	.064 mV	.02 mV	.3 mV
V_{i-pp}	.7 V	.7 V	.7 V	.7 V
g	1/3	1/3	1/3	1/3
T_s	10 μs	10 μs	10 μs	10 μs
DCG	40 dB	51 dB	80 dB	-
SLR	26 V/ms	25 V/ms	65 V/ms	$22 \pm .77$ V/ms
UGB	259 kHz	255 kHz	290 kHz	240 ± 8.4 kHz
C_i	20 fF	20 fF	20 fF	20 fF
C_s	60 fF	60 fF	60 fF	60 fF
F_s	50 Hz	50 kHz	50 kHz	50 kHz
P_{mod}	12 nW	13 nW	120 nW	4 μW

If the quantization noise is the dominant noise at the ADC output, the behavioural and circuit simulations achieve lower output-referred noise compared to the theoretical value. It is because the former involves a limited number of input voltages. Only 50 input voltages have been considered in Cadence because each transient simulation takes a long time. Since the behavioral simulation in Simulink has a moderate speed, 500 input samples were used in Simulink to achieve a higher precision. In a first-order delta-sigma ADC, quantization noise power depends on voltage for constant inputs, varying by up to 10 dB. Therefore, the simulations with 50

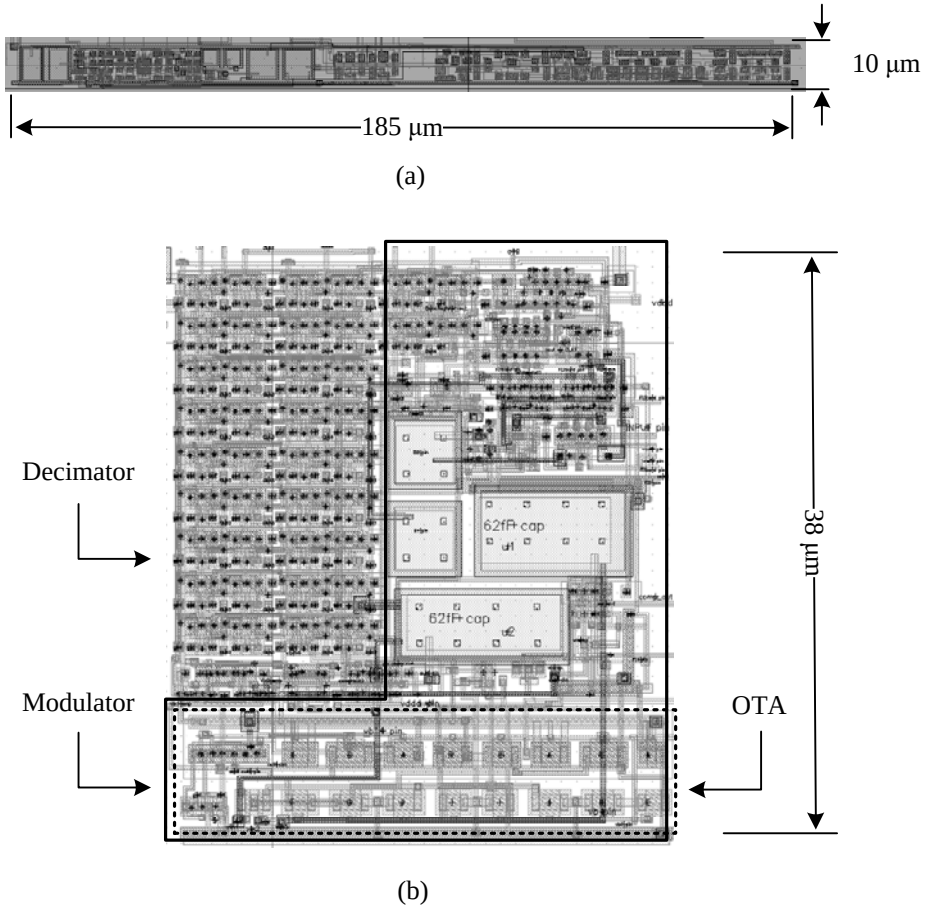


Figure 4.3: (a) Layout of the column-level modulator designed with a 10 μm pitch, a suitable pitch for visible-band image sensors. (b) Layout of the pixel-level ADC. These ADCs use $33\times38\,\mu m^2$ in 0.18 μm CMOS technology.

samples have lower output-referred noise compared to the theory. Hence, it appears the quantization noise for 50 equally-spaced input voltages over the dynamic range is lower than the expected noise over the whole range.

4.1.2 Circuit Layouts

Schematics of the fabricated ADCs are similar to the column and pixel-level ADCs presented in Chapters 2 and 3, except the fabricated ADCs are designed for .064 mV output-referred noise. The OTA in the column-level modulator was designed using the gain boosting technique to provide the required DC gain. CTM (capacitor top metal) capacitors were used since they have a high capacitance per unit area and low mismatch.

Fig. 4.3(a) shows the layout of the column-level modulator. The modulator is designed using 148 transistors, with a 10 μm pitch that is suitable for pixels in visible-band image sensors. The modulator only occupies an

area of $10\,\mu\text{m} \times 185\,\mu\text{m}$, which would be equivalent to 19 pixels.

Fig. 4.3(b) shows the layout of the pixel-level ADC, which uses 275 transistors. The modulator, the OTA, and the decimator are indicated. Almost 50% of the area is taken by the decimator. In order to assess the impact of mismatch variation, two different OTAs (OTA1 and OTA2) with the same specifications but different transistor layouts and sizes were designed for the modulator. Smaller transistors suffer from more mismatch variation compared to larger transistors [87]. The area of OTA1 was $6 \times 32\,\mu\text{m}^2$, and the area of OTA2 was $9 \times 32\,\mu\text{m}^2$. The ADCs are in two groups: one uses the smaller OTA (4 ADCs), and the other uses the larger OTA (9 ADCs). The ADCs in the first and second groups have areas of $32 \times 33\,\mu\text{m}^2$ and $33 \times 38\,\mu\text{m}^2$, respectively.

4.2 Characterization

In this section, the experimental setup is explained. This includes the PCB design and the FPGA programming. Then, the experimental results of column and pixel-level ADCs are presented and compared to state-of-the-art delta-sigma ADCs. In Section 4.3, performance will be discussed further using the design flow of the previous chapter, which was incomplete at the time of chip design.

4.2.1 Experimental Setup

Several specifications of the ADCs, such as RMS noise-and-distortion, RMS noise, dynamic range, and power consumption are measured. To do so, the chip is affixed to a PCB. Fig. 4.4 gives a block diagram of the designed PCB. It is connected to an Altera Cyclone II FPGA. The FPGA is interfaced to a PC over USB using a QuickUSB module from Bitwise Systems. With enough flexibility to implement various kinds of tests, the chip is controlled by the FPGA .

Layout of the designed PCB is shown in Fig. 4.5. The PCB is interfaced to the FPGA board via a 40-pin LVDS connector. It is mounted in a PGA68 package. A 16-bit commercial ADC (AD7680) and a 16-bit commercial DAC (LTC2641) is provided on the PCB to facilitate the testing method. To characterize the performance of the fabricated ADCs, the commercial ADC, DAC, and signal generator must have an accuracy higher than the fabricated ADCs. Using a switch, provided on the PCB, the input of the commercial ADC and the fabricated ADCs can be selected between the DAC output and the signal generator output. Using the DAC in the PCB, some part of the test could be done automatically through Matlab. The analog output of the DAC is buffered using a low-noise operational amplifier. The performance of the fabricated ADC may be compared to the commercial one provided on the PCB.

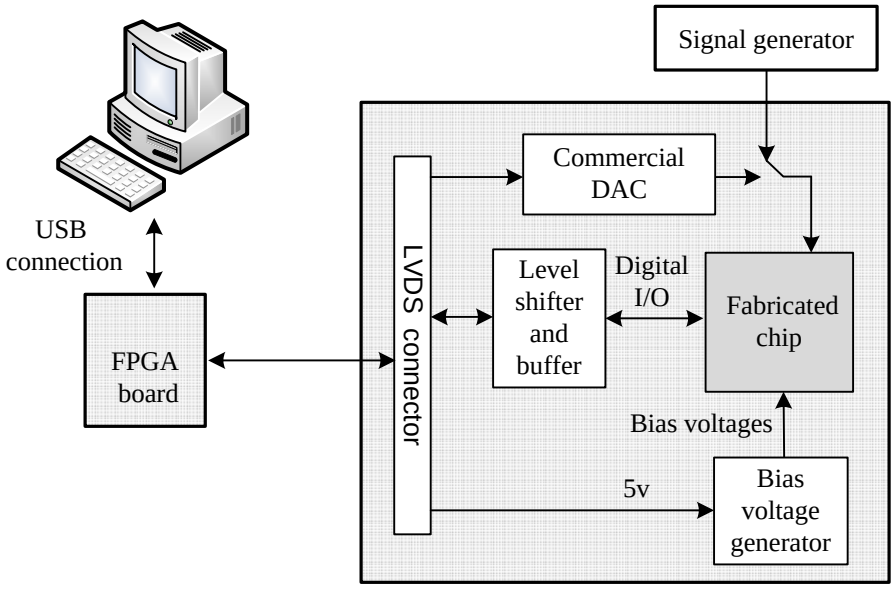


Figure 4.4: Block diagram of the designed printed circuit board (PCB).

Different analog and digital testing points of the chip are available on the PCB for analog testing and monitoring. The required analog biasing signals of the chip are generated in the PCB using a bias-voltage generator. Voltage regulators are employed to convert the 5 V provided from the FPGA to the digital and analog supply voltages required on the PCB. Also, all the clocks and digital signals required by the chip are generated in the FPGA. Translators are used to buffer and adapt the digital voltage levels of the chip and the FPGA. For power consumption measurement, the input currents of the chip are measured using small resistors. The voltage across each resistor is amplified using low-offset operational amplifiers.

Since we are trying to measure very low noise levels, the PCB is designed with special care to minimize interference and noise. Analog and digital grounds are separated. One layer of the PCB is mostly used as a ground plane. Digital and analog grounds are connected at one point close to the chip using a small resistor. Also, analog and digital signals are separated and laid out over the appropriate ground plane. In this way, current loops are minimized and noise coupling is reduced.

Fig. 4.6 shows block diagrams of the digital circuits used to test the column and pixel-level converters. They are implemented in the FPGA. The designs are similar, except in the column-level ADC the decimation is performed in the FPGA. Also, in the column-level ADC, only ϕ_1 is generated in the FPGA. The other required clocks of the column-level modulator are generated on the chip.

The FPGA is interfaced to the PC, fabricated chip, DAC, and commercial ADC through the PCB. Using a 48 MHz clock provided in the FPGA, all

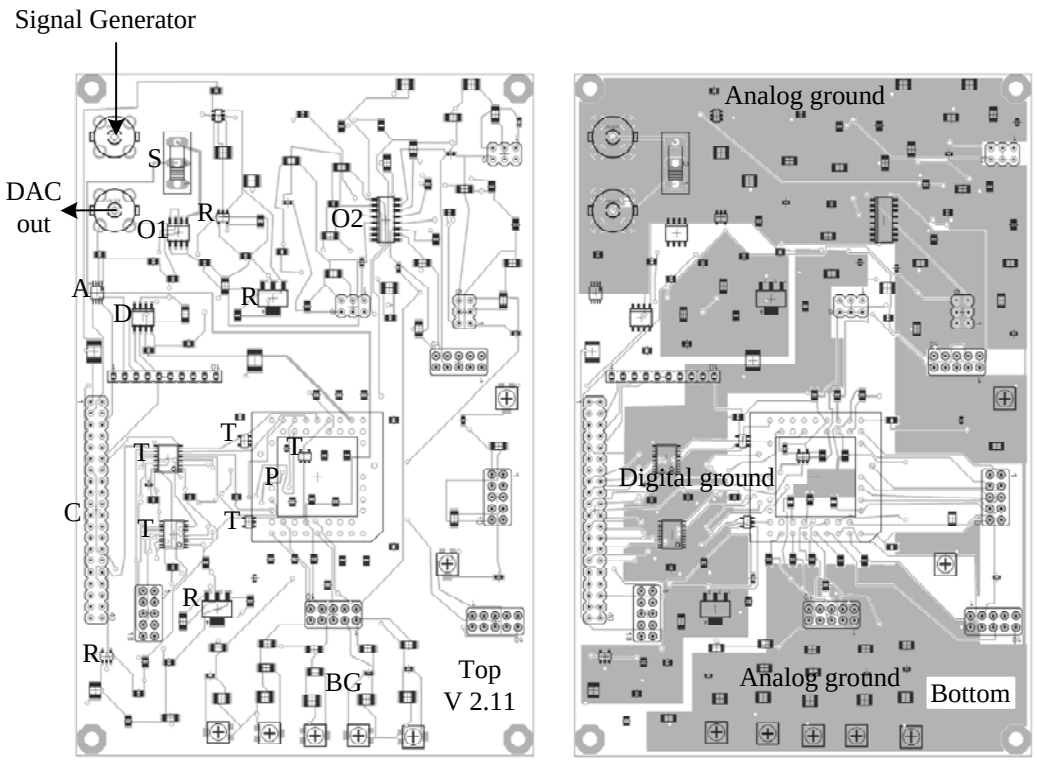


Figure 4.5: Layout of the designed PCB for testing of the fabricated column and pixel-level ADCs, showing the LVDS connector (C), PGA68 package (P), commercial ADC (A), commercial DAC (D), switch (S), buffer OPAMP (O1), voltage regulators (R), bias-voltage generator (BG), translators (T), and low-offset OPAMP (O2). Substantial ground planes are required for low-noise measurements.

the required clocks are generated. Fig. 4.7 shows a sample waveform of the signals for ADCs when the oversampling ratio is 1024. For simplicity, unlike the actual circuit, the coefficients are not rounded and truncated in the figure. Sampling starts when the start signal is set to one through the PC. With the pixel-level ADC, generated coefficients are converted to serial and sent to the chip, and decimation is done in the chip. With the column-level modulator, coefficients are accumulated in the FPGA when the modulator output is one. At the end of each interval, reset and write signals are generated by the coefficient generator. Data is written to the FIFO and the accumulator is reset. The data in the FIFO is read out by the PC periodically.

The required signals of the commercial and fabricated ADCs are synchronized to the DAC so that the DAC output settles before the sampling interval in each ADC starts.

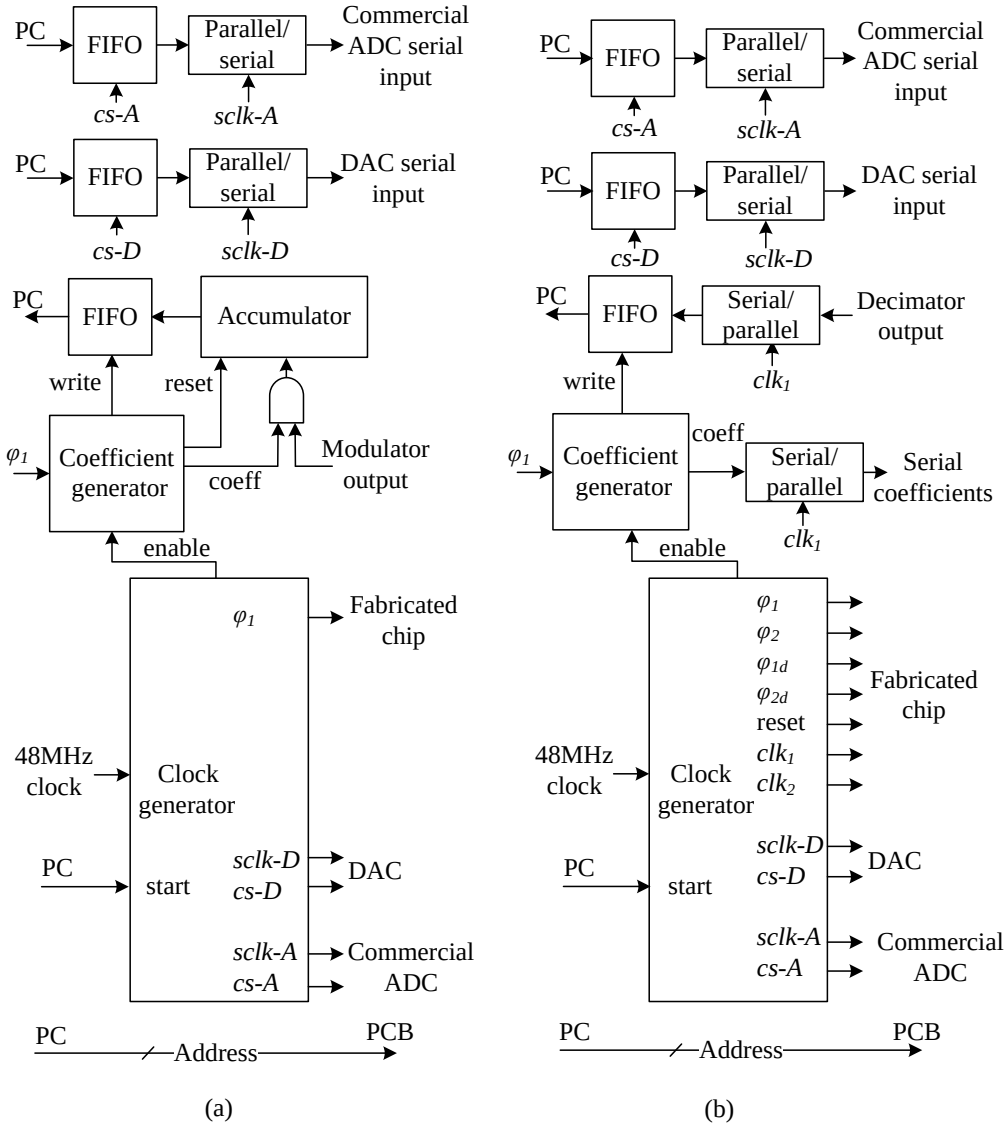


Figure 4.6: Block diagram of the circuit designed in the FPGA used in testing (a) the column-level ADC and (b) the pixel-level ADC.

4.2.2 Experimental Results

Column and pixel-level ADCs were tested using the same testing method. Since the ADCs are to be used for image sensors, instead of using a sinusoid input, the ramp input method was used in the testing procedure. The input ramp signal must be pure enough to provide the desired resolution. For automated testing of multiple ADCs, the DAC was used to generate the ramp signal. Dynamic ranges of typical column and pixel-level ADCs were measured using input sine waves, which were generated by the signal generator. Using the commercial ADC and the signal generator, it was confirmed that the resolution is not limited to the PCB or the DAC. Therefore,

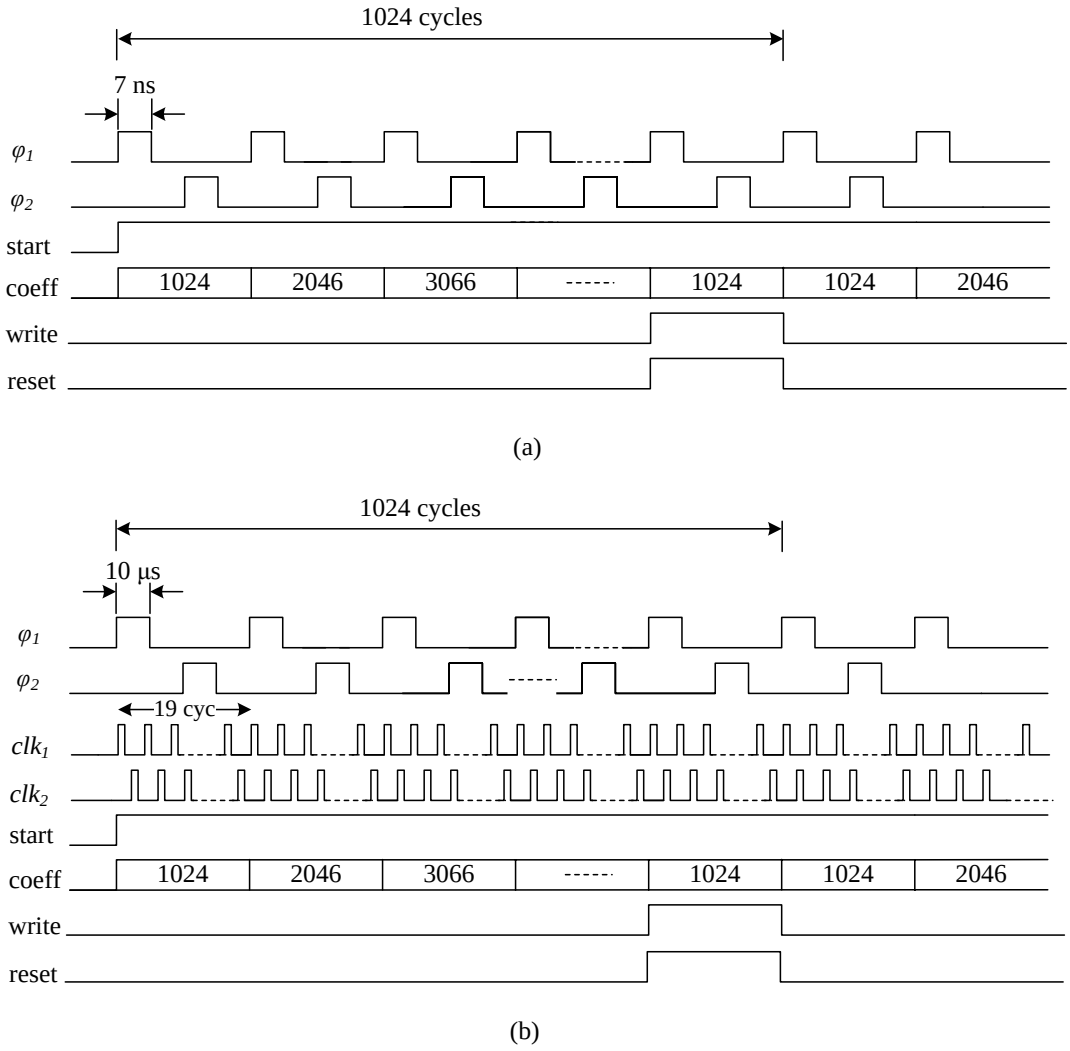


Figure 4.7: Waveform of the signals generated in the FPGA for (a) the column-level ADC and (b) the pixel-level ADC. Coefficients are generated for an oversampling ratio of 1024, which are also the values of the first and last coefficients.

the measured noise of the fabricated ADC is the dominant noise source.

The output of each ADC was read by the PC. Using linear regression, a straight line was fitted to the ADC output. The oversampling ratio was 1024 and the voltage range was .7 V.

Fig. 4.8 shows the output ramp signal of typical column and pixel-level ADCs and their corresponding residual error. By repeating the experiment multiple times, in both the ADCs, it was discovered that the residual errors of the linear regression fit are composed of two parts. One part, the large undulations, does not change from experiment to experiment. It defines a nonlinear distortion. The other part, the small oscillations in the same figure, does change from experiment to experiment. It defines the temporal

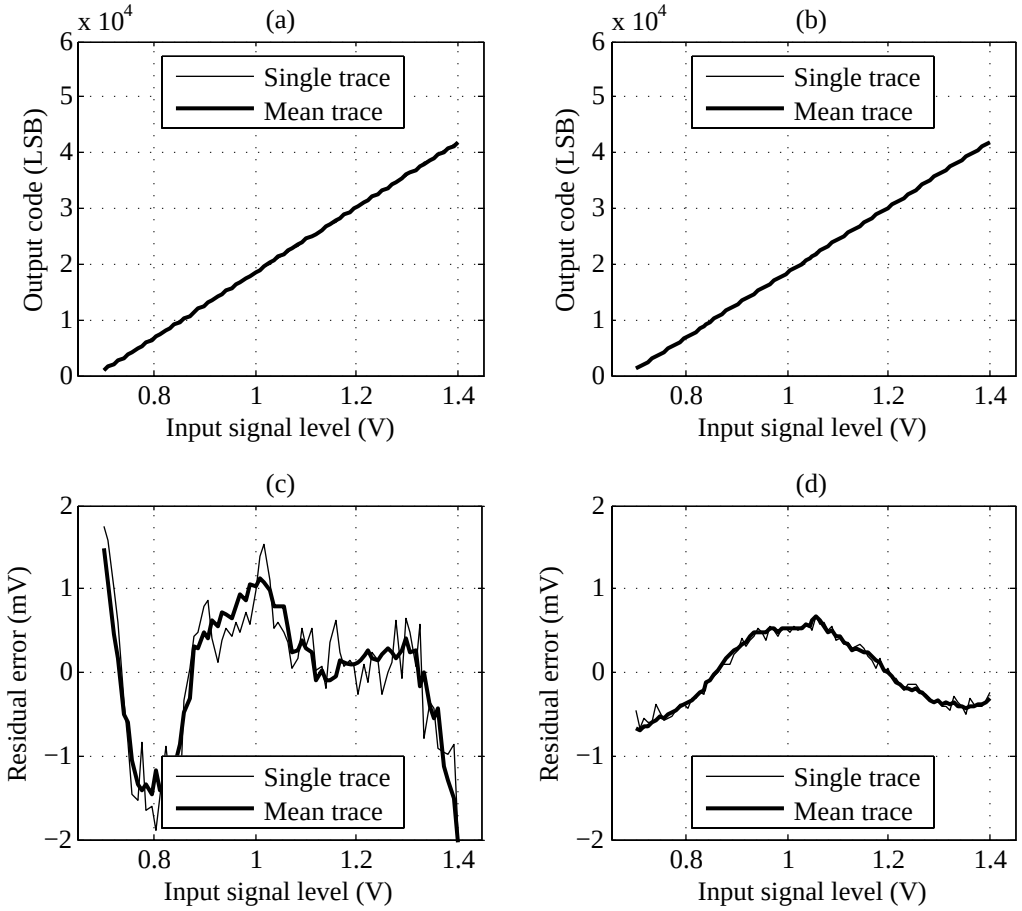


Figure 4.8: Measurement results of typical ADCs for a ramp input signal. Output code versus input signal level for (a) the column-level ADC and (b) the pixel-level ADC. Residual error of (c) the column-level ADC and (d) the pixel-level ADC. The error is measured after linear regression versus input signal level. The mean trace is the average of 10 single traces, each of which has a different temporal noise component.

noise. If the nonlinear distortion is factored out, the temporal noise can be measured, which is much lower than the former. This shows that the ADCs have been very successful at reducing temporal noise. Nonlinear distortion is a consequence of low UGB and SLR in the OTA, which is caused by mismatch variation within the circuit.

Fig. 4.9 shows the minimum, median, and last decile of RMS noise-and-distortion among the ADCs versus power consumption. In each case, the power consumption is modified by changing the bias point of the OTA and all the ADCs are biased using the same bias voltages. While the pixel-level modulator achieves lower RMS noise-and-distortion, both of the modulators have similar performances. As expected, the performance of the ADCs exhibits less variation in a small bias range due to tolerances of the CMFB

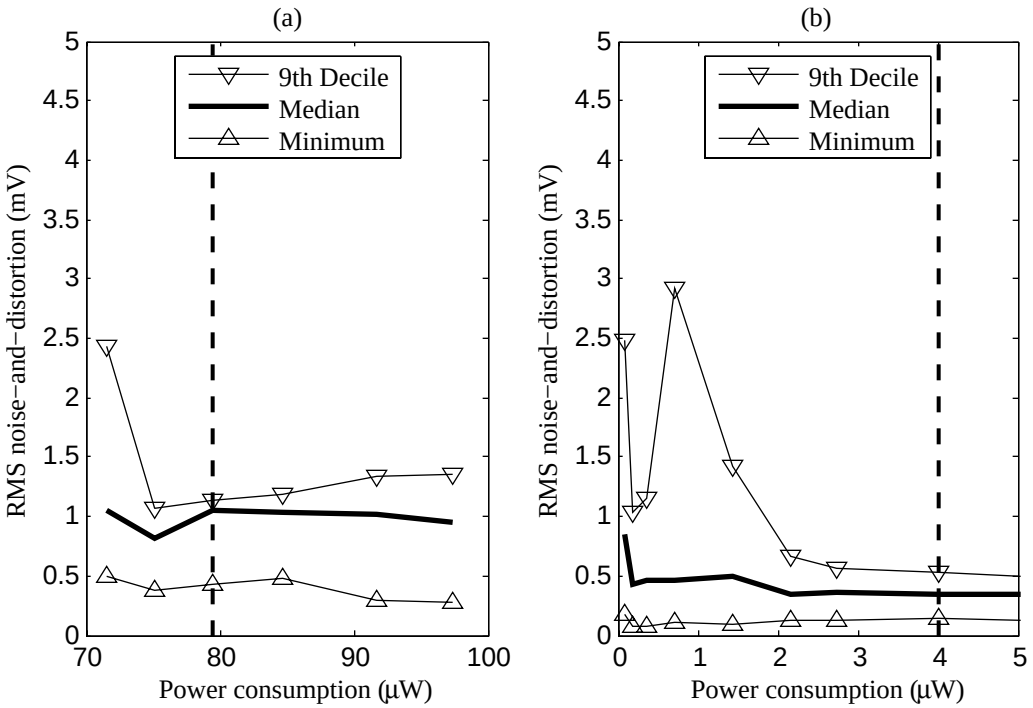


Figure 4.9: The minimum, median, and last decile of RMS noise-and-distortion versus power consumption of the modulator for: (a) 16 column-level ADCs and (b) 36 pixel-level ADCs with the larger OTA. Power consumption is varied by modifying the bias current of the OTA. The dotted line shows the bias point of the modulators in Fig. 4.10.

circuit. Also, in both cases, performance is limited by distortion.

Fig. 4.9(a) gives the performance of the 16 column-level modulators. The maximum values ranged from 1.5 to 14 mV. In the median case, the RMS noise-and-distortion is 1 mV with a Nyquist rate of 50 kHz and a power consumption of 79 μW. Using circuit simulation, the decimator is estimated to have 60 μW power consumption in all cases.

The pixel-level ADC was designed with two different OTAs to evaluate the effect of transistor size on performance. Fig. 4.9(b) shows the minimum, median, and last decile of RMS noise-and-distortion for the 36 pixel-level ADCs of the second type (larger) versus the modulator power consumption. Maximum values were undefined for power consumptions less than 2.1 μW and ranged from .7 to 2.5 mV at higher power consumption. Although the ADCs have low RMS noise-and-distortion for power consumption less than 1 μW, they exhibit a large variation. For higher power consumption, the RMS noise-and-distortion has less variation, which means the ADCs are more reliable. Therefore, the working point of the ADCs was chosen to be 4 μW. The median is .3 mV at this power consumption. The decimator has 3 μW power consumption in all cases.

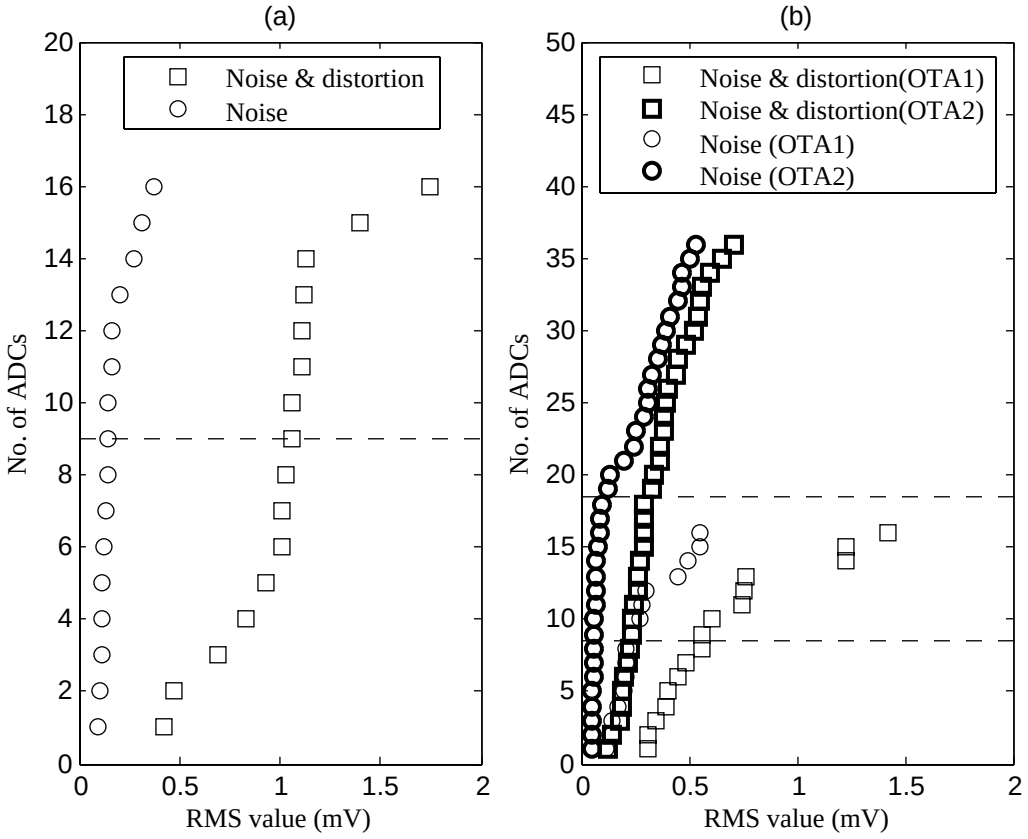


Figure 4.10: (a) Cumulative distribution function of number of ADCs versus RMS noise-and-distortion and RMS noise in (a) 16 column-level ADCs, (b) 36 pixel-level ADCs with the larger OTA, and (b) 16 pixel-level ADCs with the smaller OTA. Dotted lines indicate the median values.

Fig. 4.10 shows the cumulative distribution function (CDF) of number of ADCs versus RMS noise-and-distortion and RMS noise in the column and pixel-level ADCs. When normalized, the CDF estimates the probability that a given variable is less than or equal to a certain value. Measurement were done at the power consumptions indicated in Fig. 4.9, at which the ADCs have reliable performance with little variation. The variability is mainly a result of mismatch variation because of very small transistors used in the OTA. Variability could be reduced by using larger transistors, as will be discussed in Section 4.3.

Tables 4.2(a) and 4.2(b) summarize the RMS noise-and-distortion and RMS noise in the column and pixel-level ADCs. Performance of the column-level ADC is measured when the modulator has 79 μW power consumption. Clearly, nonlinearity error is the dominant error. Also, variation in performance is because of mismatch.

Each pixel-level modulator has 4 μW power consumption, while the decimator has 3 μW power consumption. Pixel-level ADCs using the larger

Table 4.2:

(a) RMS noise-and-distortion in the column and pixel-level ADCs.

Parameter	Column-Level ADC	Pixel-Level ADC with Larger OTA	Pixel-Level ADC with Smaller OTA
Maximum	1.8 mV	.70 mV	1.4 mV
Median	1.0 mV	.30 mV	.56 mV
Minimum	.40 mV	.13 mV	.30 mV

(b) RMS noise in the column and pixel-level ADCs.

Parameter	Column-Level ADC	Pixel-Level ADC with Larger OTA	Pixel-Level ADC with Smaller OTA
Maximum	.35 mV	.53 mV	.55 mV
Median	.14 mV	.11 mV	.22 mV
Minimum	.10 mV	.05 mV	.11 mV

OTA (36 ADCs) with less mismatch variation achieve lower RMS noise-and-distortion and RMS noise. The median ADC using the larger OTA achieves 5.1 dB lower RMS noise-and-distortion and 6 dB lower RMS noise compared to the median ADC using the smaller OTA. This shows that the performance of the ADCs using the smaller OTA (16 ADCs) is limited because of mismatch variation. In both cases, RMS noise is significantly smaller than the distortion level, showing that nonlinearity error is the dominant error in the output.

Dynamic ranges of the typical ADCs are measured using an input sine wave, which is generated by the signal generator. Fig. 4.11 shows signal-to-noise-and-distortion ratio (SNDR) versus peak-to-peak voltage of a sine wave for typical column and pixel-level ADCs. Dynamic range of a typical column-level ADC is measured to be 62 dB, which means 10-bit resolution. A typical pixel-level ADC has 66 dB dynamic range, which means 11-bit resolution.

For a typical pixel-level ADC with 11-bits resolution, differential nonlinearity (DNL) and integral nonlinearity (INL) were measured to be 1.5 and 2.6 LSB, respectively. DNL and INL for a typical column-level ADC with 10-bit resolution were 3.5 and 17 LSB, respectively.

4.2.3 Figures of Merit

To evaluate the performance of the column and pixel-level ADCs against the state of the art, consider two commonly-used figures-of-merit (FOMs), which are defined as follows [1, 12, 61, 88]:

$$FOM_1\,\mathrm{dB} = DR_{\mathrm{dB}} + 10\log\frac{BW}{P_{mod}}, \tag{4.1}$$

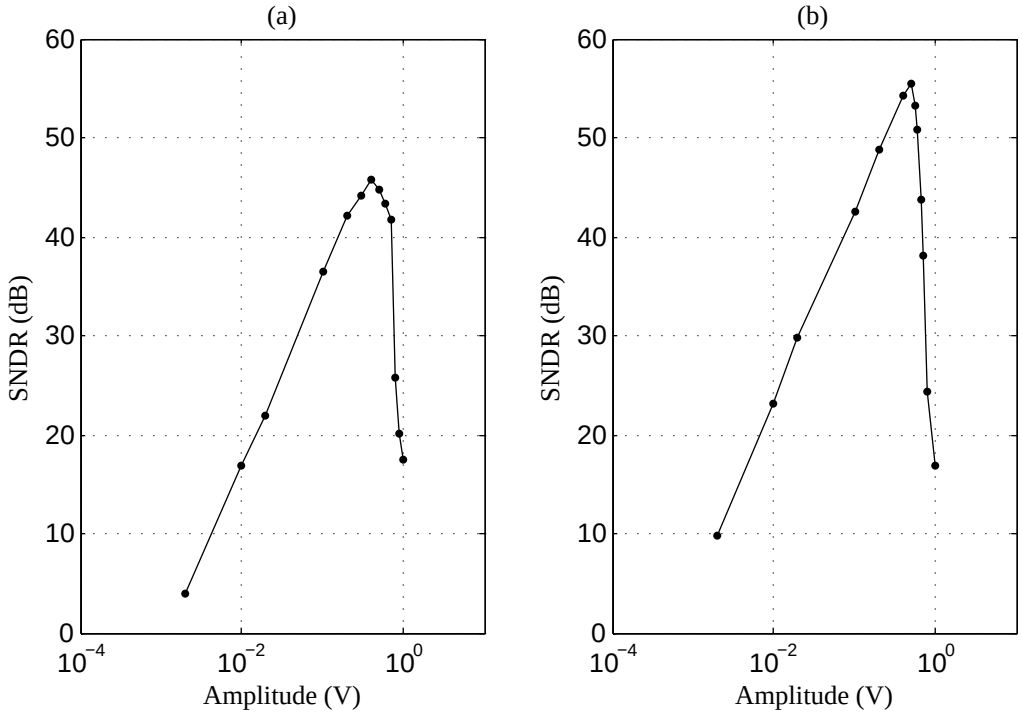


Figure 4.11: Signal-to-noise-and-distortion ratio versus amplitude of an input sine wave for a typical (a) column-level and (b) pixel-level ADC.

$$FOM_2 = \frac{P_{mod}}{2 \cdot BW \cdot 2^{ENOB}}, \tag{4.2}$$

where DR is the dynamic range of the modulator, which should not be confused with the dynamic range of the image sensor. DR is defined as the ratio of maximum and minimum amplitudes of sinusoid tests for which $SNDR > 0\,\text{dB}$ [60]. BW is the Nyquist sampling rate, P_{mod} is the power consumption of the modulator, and $ENOB$ is the effective number of bits, which is defined as $(SNDR - 1.76)/6.02$. Both definitions give similar results. The first definition will be used in this thesis.

Table 4.3 compares the modulator performance of the fabricated ADCs to state-of-the-art OTA-based modulators. Only the modulator is considered because only FOM and power consumption of the modulator is reported in the literature [29, 61, 89].

The FOM of a typical column-level modulator with the measured dynamic range of 62 dB is 150 dB. Since the modulator is going to be used in an array, the area of the modulator matters. Although the FOM of the designed modulator is not better than the other modulators, its area usage is significantly smaller. For example, the modulator area is 227 times or 47 dB smaller than the modulator with the best FOM.

The FOM of a typical pixel-level modulator is 137 dB when its power consumption is $4\,\mu$W. The ADC achieves a low RMS noise but the FOM

Table 4.3: Performance of the fabricated designs, as compared to state-of-the-art OTA-based modulators in the literature.

Design	Process	*DR*	*BW*	P_{mod}	*FOM*	Area
Column-Level Modulator	0.18 μm	62 dB	50 kHz	79 μW	150 dB	1850 μm^2
Pixel-Level Modulator	0.18 μm	66 dB	50 Hz	4.0 μW	137 dB	627 μm^2
Kuo *et al.* [90], 2010	0.18 μm	88 dB	20 kHz	1.52 mW	159 dB	1.57 mm^2
Agah *et al.* [12], 2010	0.18 μm	90 dB	1.0 MHz	38.1 mW	164 dB	3.50 mm^2
Lee *et al.* [88], 2009	0.18 μm	82 dB	1.9 MHz	8.10 mW	166 dB	1.27 mm^2
Roh *et al.* [61], 2008	0.13 μm	83 dB	20 kHz	0.06 mW	168 dB	0.42 mm^2
Kim *et al.* [89], 2008	0.13 μm	92 dB	24 kHz	1.50 mW	164 dB	1.40 mm^2
Safi-Harb *et al.* [60], 2005	0.18 μm	78 dB	2.0 MHz	19.0 mW	158 dB	6.40 mm^2

is not high because the power consumption is set high to make sure that the modulators are biased so as to minimize variability. At lower power consumptions, better FOM is achieved but the performance has more variability. Although the designed pixel-level ADC has lower FOM than the other modulators, its area usage is significantly smaller. The ADC area is 1254 μm^2, of which the modulator takes half. It is 670 times or 57 dB smaller than the modulator with the best FOM.

Recently, there has been an increased interest in employing inverter-based integrators in delta-sigma ADCs to reduce the area and power consumption of the modulator [1, 28]. In this approach, the OTA is replaced with an inverter. Chae *et al.* [29] design a second-order delta-sigma ADC this way, in 0.13 μm technology, with an FOM of 172 dB. The ADC occupies 2700 μm^2, which is 2.2 times larger than the pixel-level ADC presented here.

4.3 Discussion

In this section, experimental results are analyzed and explained based on the theory presented in the previous chapter. Also, the behavioural model is used to simulate the circuit and justify the results. The same method is

used to explain both the column and pixel-level ADCs. Hence, the design flow is validated using the experimental results.

In principle, delta-sigma ADCs are less sensitive to analog nonidealities as compared to Nyquist-rate ADCs. But in order to achieve certain specifications, the OTA, which is the most critical component in the ADC, must provide minimum requirements. These requirements include the DC gain, unity gain bandwidth, slew rate, etc [60,77]. These parameters are affected by mismatch variation. Mismatch variation can change the bias current of the OTA and, therefore, modify its specifications.

The digital section of the ADC, which functioned perfectly, is not sensitive to mismatch variation and could be implemented using minimum size transistors. However, the analog part of the design, mainly the OTA, is sensitive to mismatch variation. To eliminate these variations, the OTA should be designed with a large enough area using robust layout techniques. This is not easily possible in a very small pixel. Mismatch is more problematic when instead of switched-capacitor CMFB circuits, a DDA-CMFB is used to save area. The DDA-CMFB circuit is less tolerant to mismatch and also creates more nonlinearity in the OTA output.

What is desired is to design the smallest OTA that meets a required mismatch specification based on the ADC specification. The effect of mismatch variation on ADC performance was included in the completed design flow to ensure that the ADC can achieve the required performance. At the time of actual design, however this was not done partly because the data regarding mismatch variation for the CMOS process was not available.

As Fig. 4.8(c) and (d) show, the nonlinearity error is larger than the temporal noise. Chapter 3 discussed how the nonlinearity error is caused by settling error, which depends on the input signal. This means that either the SLR or UGB is not enough for the available integration time or vice versa. Degradation in the SLR and UGB is caused by mismatch in the OTA.

In addition, the column-level modulator was designed so that the integration and sampling times are 7 ns, and the oversampling period is 15 ns. The clock ϕ_2, a delayed version of ϕ_1, is generated using a delay circuit, while ϕ_1 is generated in the FPGA. The delay circuit for ϕ_2 is designed to provide 7.5 ns delay. Any variation more than .5 ns in the delay provided by the delay circuit inside the chip will cause an overlap between the clocks. This can cause a large degradation in performance. Therefore, the sampling clock ϕ_1 must have a very accurate duty cycle with sharp edges.

The effect of modifying the duty cycle of ϕ_1 on column-level ADC performance was checked in another experiment. It was shown that any variation of the duty cycle can easily affect the RMS noise-and-distortion and RMS noise. Therefore, degradation in performance is partly because of this problem. The clocks should be generated in a different way to avoid this issue.

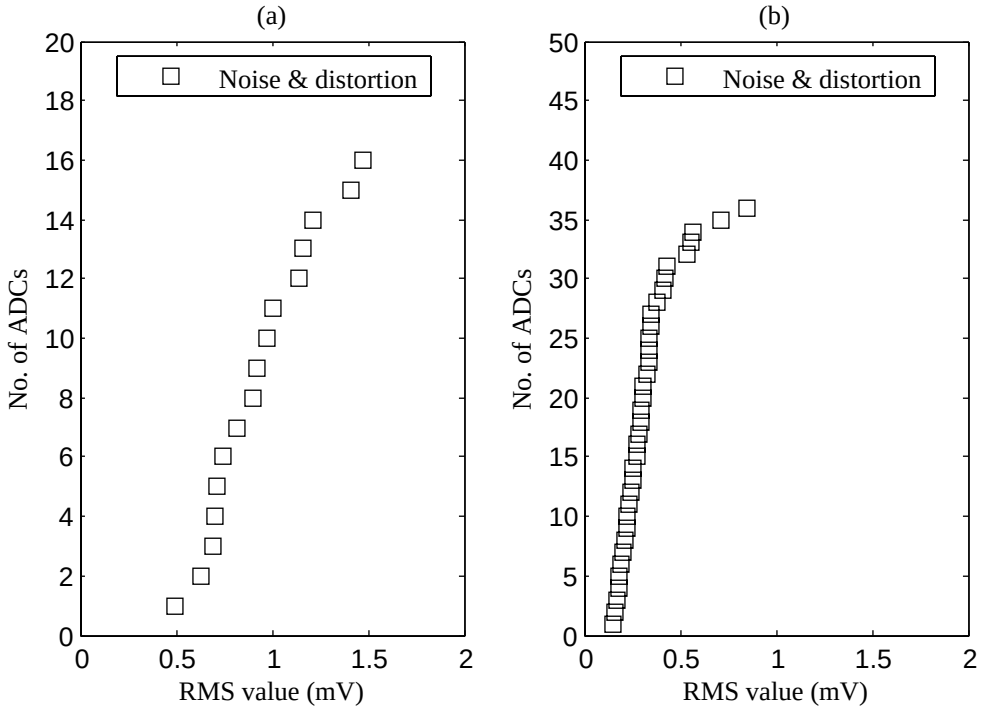


Figure 4.12: Simulated cumulative distribution function of number of ADCs versus RMS noise-and-distortion in (a) column-level and (b) pixel-level ADCs, when the UGB, SLR, and integration time have a normal distribution with reasonable mean and standard deviation. Other specifications of the ADCs are the same as the original values.

4.3.1 Behavioural Simulation

As explained in the previous chapter, nonlinear distortion is mostly because the SLR or UGB of the OTA is smaller than the desired value. To justify the experimental results, the behavioural model presented in Chapter 3 was used to simulate the modulators and estimate the UGB, SLR, and integration time. Column and pixel-level modulators were simulated with randomly-varying UGB and SLR around the mean values. Also, for the column-level modulator, variation of the integration time was considered in the simulation.

Fig. 4.12 shows the CDF of number of ADCs versus RMS noise-and-distortion in column and pixel-level ADCs, where the mentioned parameters have a normal distribution. It was assumed that other specifications of the fabricated modulators are the same as the original values. The simulated column and pixel-level modulators have similar performance to the experimental results in Fig. 4.10(a) and (b) when UGB, SLR, and integration time have reasonable values. Therefore, the behavioural model can explain the experimental results.

In the simulated column-level modulator, the UGB was set to a mean of

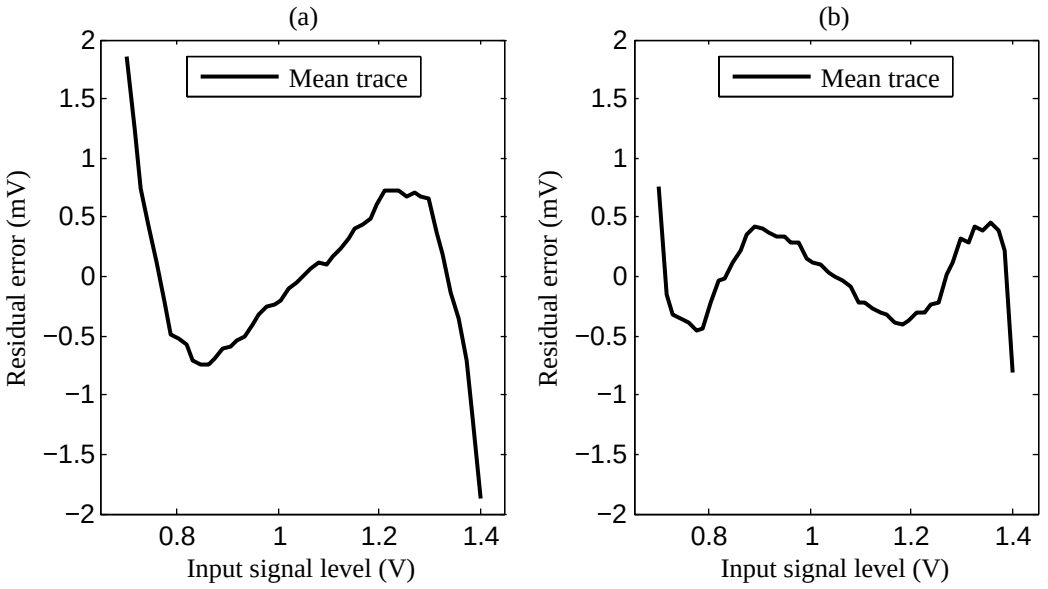


Figure 4.13: Residual error of simulated (a) column-level and (b) pixel-level ADCs, when the SLR and UGB of the OTA are smaller than the required values.

190 MHz with a standard deviation of 8.5 MHz, the SLR was set to a mean of 40 V/μs with a standard deviation of 2 V/μs, and the integration time had a 7 ns mean with a .325 ns standard deviation. Compared to the circuit simulation, smaller UGB and SLR are expected with the experimental results because the power consumption in the experimental results is half that of the circuit simulation. These values are comparable to the behavioural and theoretical results presented in Table 4.1(a).

In the simulated pixel-level modulator, the UGB was set to a mean of 240 kHz with a standard deviation of 8.4 kHz. The SLR had a 22 V/ms mean with a .77 V/ms standard deviation, and the integration time was fixed to 10 μs. Once again, these values are comparable to the behavioural and theoretical results presented in Table 4.1(b).

Fig. 4.13 shows the residual error for a ramp input signal when the SLR and UGB of the column and pixel-level modulators are the mean values used for Fig. 4.12. The error shape from the simulation of low SLR and UGB is similar to the error shape, shown in Fig. 4.8, of the experimental results. This resemblance supports the theory that the performance degradation in the experimental results is a result of low SLR and UGB.

In order to increase the SLR and UGB, the bias current should be increased. However, the OTA is designed only for a certain bias current. Increasing the current after fabrication of the design will change the common-mode output voltage and modify the OTA bias voltages.

Simulink simulation shows that kTC noise generated because of the 60 fF

capacitors results in random temporal noise, and it limits the RMS noise-and-distortion to .045 mV. This is one factor that determines the RMS noise, which is two to three times as large in the experimental results, i.e.,Tables 4.2(b).

It was shown that performance of both the ADCs can be predicted using the Chapter 3 model. This means that the experimental results validate the design flow presented in the previous section. To improve the modulator performance, the completed design flow must be used.

4.4 Conclusion

In this chapter, the design and experimental results of two arrays of column and pixel-level ADCs were discussed. The fabricated ADCs have figures of merit comparable to state-of-the-art delta-sigma ADCs while their area usage is significantly smaller. This makes them more suitable for ADC arrays. The pixel-level ADC is the first to integrate in-pixel decimation.

A platform was designed to facilitate the testing procedure. This included PCB design, FPGA programming, and data measurement. The output bit stream of the ADCs were transfered to a PC through the designed PCB and the programmed FPGA for processing and performance measurement.

With both the column and pixel-level ADCs, the RMS noise-and-distortion and RMS noise are degraded and show variability because of mismatch variation. This was explained using the completed modulator design flow presented in Chapter 3. Therefore, the design flow was validated using the experimental results of two ADC designs.

With the pixel-level ADCs, two different versions were designed, one using a larger OTA, and the other using a smaller OTA with the same specifications. The ADC with the larger OTA achieves a lower RMS noise-and-distortion, which also implies that mismatch variation affects the ADC performance.

In the next chapter, two logarithmic image sensors are designed and fabricated using column and pixel-level ADCs similar to the ones presented in this chapter. The experimental results of both arrays will be discussed and compared to state-of-the-art image sensors.

Chapter 5

Image Sensor Advances

For this chapter, two image sensors, one using column-level data conversion and the other using pixel-level data conversion, were fabricated on one chip, and tested. Experimental results are compared to the state of the art, which demonstrates a significant improvement to the SNDR of logarithmic sensors. This means that using column or pixel-level delta-sigma ADCs is a promising approach to boost the SNDR of logarithmic sensors. Because the column or pixel outputs are digital, these structures are called digital column or pixel sensors (DCS or DPS).

Both array sensors use a photodetection circuit with a logarithmic response. Logarithmic sensors are chosen over linear sensors because they can easily achieve high dynamic range, whereas their main drawback is low SNDR. Apart from dynamic range, effective bit resolution in an image is determined by SNDR, which is limited by SNR and residual FPN. Therefore, our main focus is to improve the SNDR.

Using column or pixel-level data conversion, readout noise is reduced and SNDR is improved, something that cannot be done with a chip-level approach. Nyquist-rate ADCs need a sharp low-pass filter with a large area, making them impractical for the column or pixel-level approach. Instead, delta-sigma ADCs are employed to perform data conversion so that the temporal noise can be reduced without using a sharp low-pass filter. Therefore, the approach of column or pixel-level data conversion based on delta-sigma ADCs is beneficial in removing noise and improving the SNDR of logarithmic sensors.

Section 5.1 explains the architecture of the fabricated chip. The experimental setup and results are presented in Section 5.2. Also, performance of the image sensors is compared to state-of-the-art image sensors. The experimental results are discussed further in Section 5.3. Moreover, DCS and DPS approaches are compared to each other. The main contributions of this chapter are summarized in Section 5.4.

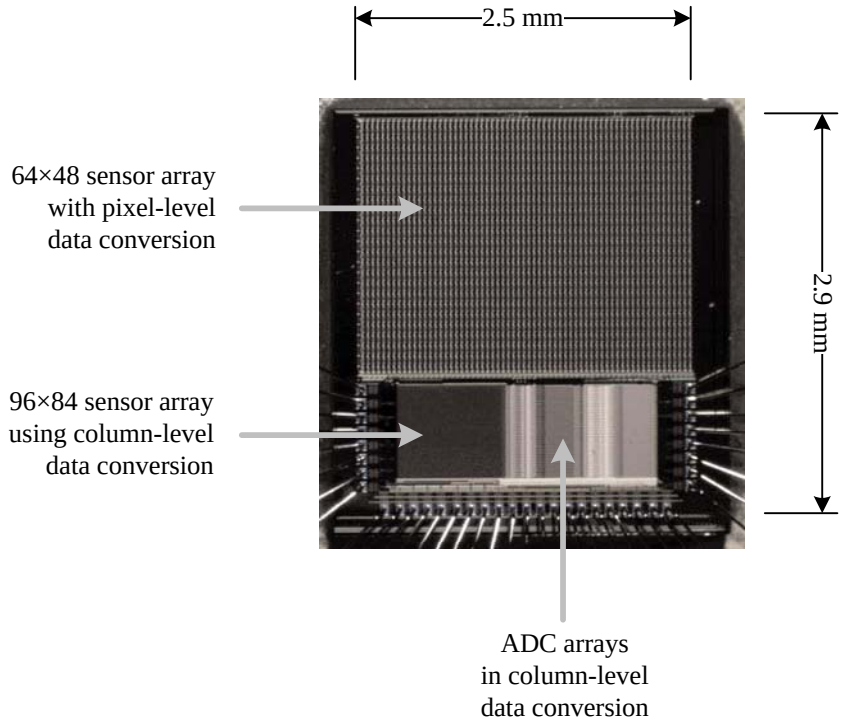


Figure 5.1: Micrograph of the prototype fabricated in 0.18 μm CMOS technology. The chip contains two logarithmic image sensors, one using column-level data conversion and the other using pixel-level data conversion. In both arrays, the conversion is done using delta-sigma ADCs.

5.1 Fabricated Designs

The chip, fabricated in 0.18 μm 1P5M standard CMOS technology, includes two logarithmic image sensors. Fig. 5.1 shows a micrograph of the $2.5 \times 2.9\,\text{mm}^2$ chip, which has 1,004,786 transistors. To save resources, small arrays were fabricated, which suffice to show the feasibility of the approaches. The DCS has 84×96 pixels, each with size $8 \times 8\,\mu\text{m}^2$. The image sensor using pixel-level data conversion has 48×64 pixels, each with size $38 \times 38\,\mu\text{m}^2$.

Fig. 5.2 gives a block diagram of the chip. Both image sensors use first-order delta-sigma ADCs, which are very similar to the stand-alone ADCs presented in the previous chapter. Row and column decoders are shared between the arrays. Clock signals and analog bias voltages are also shared by the image sensors. Sampling and integration clocks (ϕ_1, ϕ_2), and their delayed versions (ϕ_{1d}, ϕ_{2d}), for both image sensors are generated in an FPGA and are sent to the chip.

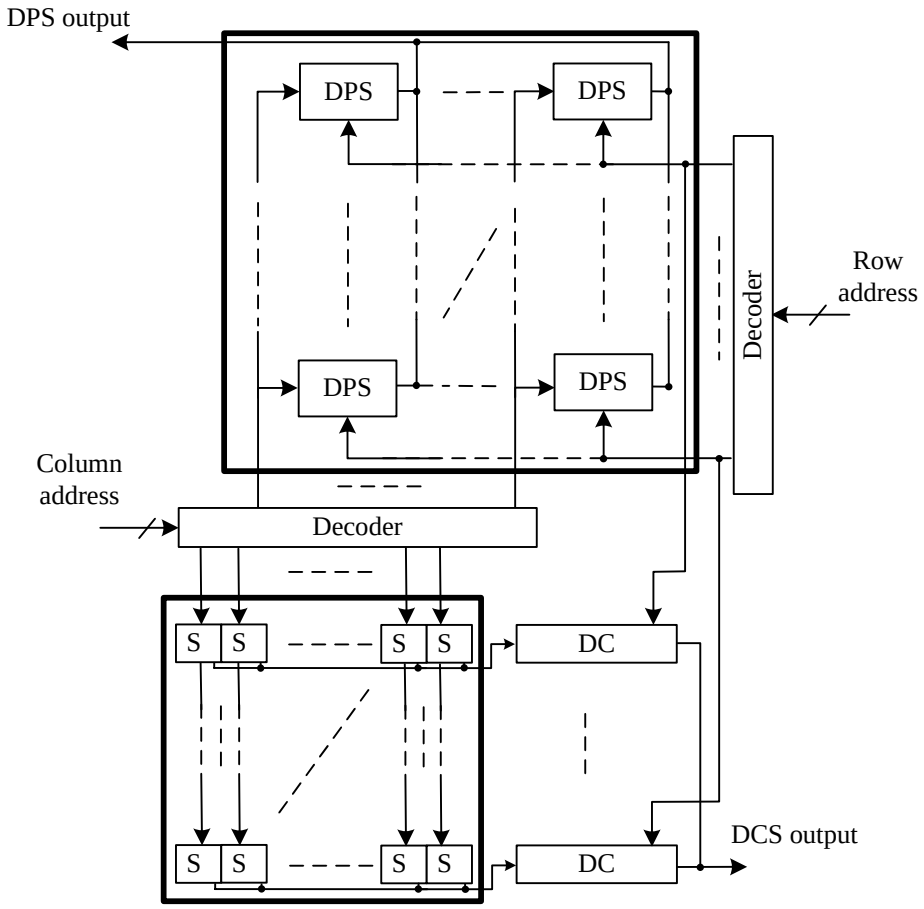


Figure 5.2: Floor plan of the chip, including the digital column sensor (DCS), which is divided into multiplexed sensors (S) and a digital column (DC), and the digital pixel sensor (DPS), where a sensor is integrated into a digital pixel. The DCS is actually a digital row sensor in this case.

5.1.1 Circuit Specifications

Table 5.1 compares the target specifications of both image sensors. In both cases, the ADCs were designed so that the image sensors would achieve 40 dB SNDR with 50 Hz frame rate (suitable for video) and 100 dB dynamic range, which is comparable to human vision. The pixel size in DCS is smaller than DPS, making it more suitable for visible-band applications.

In the DCS, a new ADC was designed, using an incomplete version of the design flow presented in Chapters 2 and 3, for an image sensor with a 84×96 array size and an $8\,\mu$m pixel pitch. Pixel pitch in the visible band is typically less than $10\,\mu$m [15]. A 19-bit accumulator was used to realize the decimator. The modulator in each column samples the output of each pixel at 4.9 MHz. The decimator downsamples the signal to 4.8 kHz. Each column has 96 pixels. Therefore, each pixel is sampled at 50 Hz.

The pixel-level ADC that was designed in Chapter 4 was used in the

Table 5.1: Specifications used in the design of a DCS and DPS.

Parameter	DCS	DPS
Array size	84×96	48×64
Pixel size	$8 \times 8\,\mu m^2$	$38 \times 38\,\mu m^2$
SNDR	40 dB	40 dB
Dynamic range	100 dB	100 dB
Frame rate	50 Hz	50 Hz

DPS. The pixel size was the smallest layout possible in the time available. However, the pixel size makes the design more suitable for imaging applications outside the visible band. The modulator oversamples the output signal of the logarithmic sensor at 53 kHz. The decimator filters the signal and downsamples it to 52 Hz when the oversampling ratio is 1024. Because it takes 14.5 ms to read out each frame, the video rate is 30 fps. Reducing the oversampling ratio increases the video rate but decreases the SNR.

5.1.2 Circuit Schematics and Layouts

The schematic of a column in the DCS is shown in Fig. 5.3(a). The first-order delta-sigma ADC includes a modulator and a decimator. Unlike the version of the column-level ADC presented in the previous chapter, the decimator is designed inside the chip here. It is implemented using an accumulator with serial addition similar to the pixel-level decimator except, instead of using pulsed latches, regular D flip-flops are used.

The layout of one column in the DCS is shown in Fig. 5.3(b). In the DCS, the output of each column of pixels is connected to one ADC having a 16 μm pitch. Each ADC has the same pitch as two columns of pixels. Two ADCs are laid out beside each other, where each one is connected to one column of pixels. The modulator and decimator take almost the same area, which in total is $570 \times 16\,\mu m^2$, almost the same area as 142 pixels. Area of the ADCs are comparable to the area of the pixel array. Hence, the area should be minimized to save room for pixels.

Fig. 5.4 shows the schematic and layout of one pixel in the DPS, which includes a logarithmic sensor and a first-order delta-sigma ADC. The oversampling ratio may be up to 1024. The modulator and decimator are implemented in the pixel using 298 transistors. As the pixel-level ADC with large OTA from Chapter 4 is suitable for the target specifications, the same circuit was used in the DPS. Only readout and sensor circuits were added to the design.

For both the DCS and DPS arrays, coefficients required for decimation are generated in an FPGA and are sent to all decimators through buffers. The output of both the decimator and modulator can be read out. If a dec-

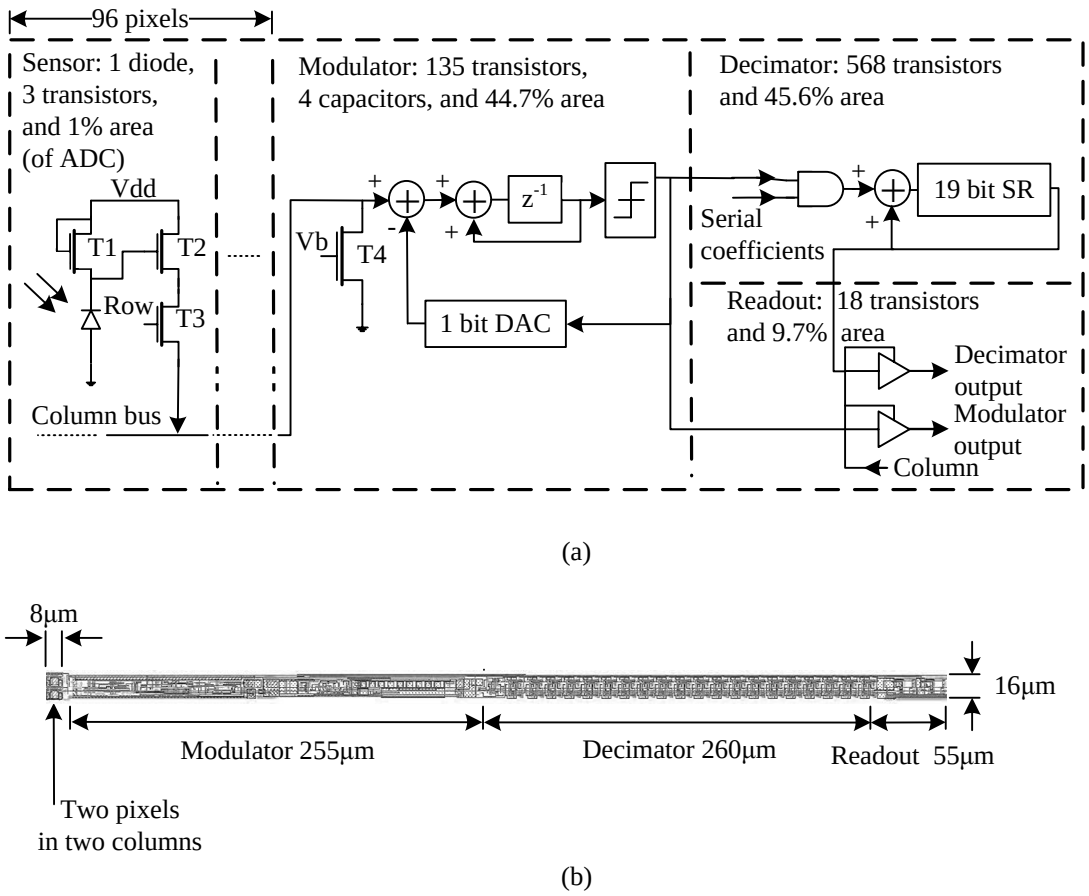


Figure 5.3: (a) Schematic and (b) layout of a column in the DCS, which comprises multiplexed logarithmic sensors, a modulator, a decimator, and a readout circuit. Two ADCs with 16 μm pitch are designed in every two columns. The pixel pitch is 8 μm. Only one ADC is shown in the figure. The DCS array occupies $1900 \times 672\,\mu\text{m}^2$ and uses 83,244 transistors.

imator is not functional, the modulator output may be decimated in the FPGA.

5.2 Characterization

In this section, a characterization of the image sensors is presented. Dynamic range, SNR, SNDR, power consumption, and frame rate are important parameters in determining the performance of an image sensor.

Both the DCS and DPS arrays use logarithmic sensors. Therefore, high dynamic range is easily achieved. However, logarithmic sensors suffer from FPN, which needs to be corrected. The response y of a pixel to stimulus x is

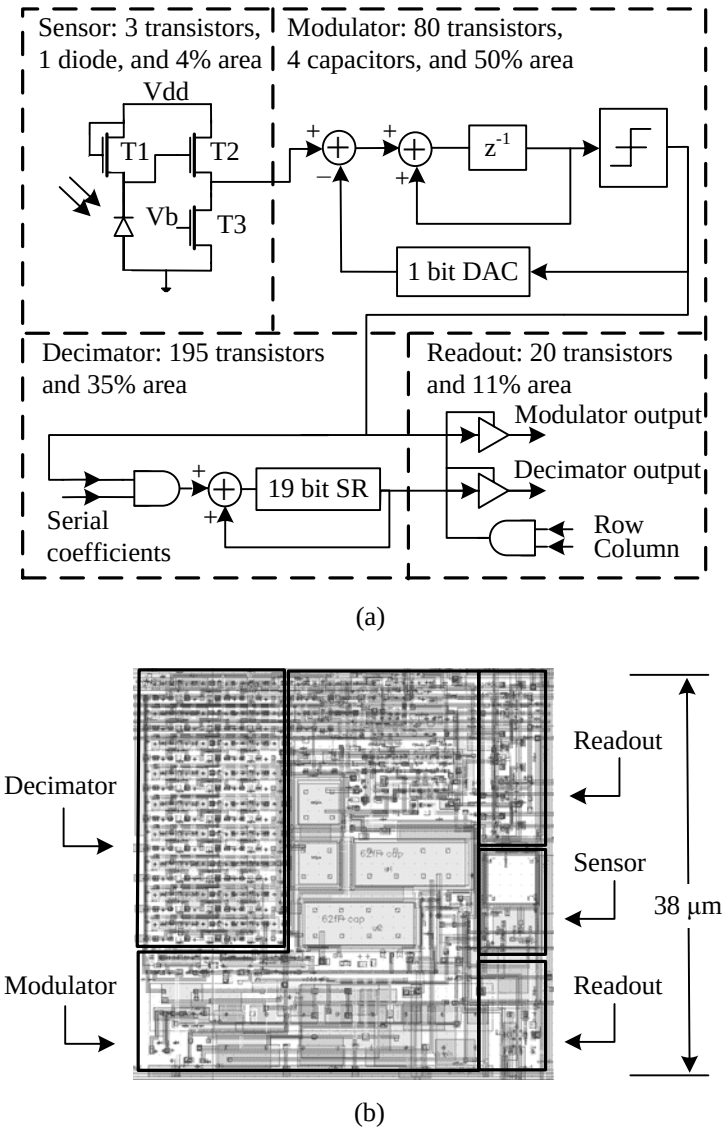


Figure 5.4: (a) Schematic and (b) layout of a pixel in the DPS, which comprises a logarithmic sensor, a modulator, a decimator, and a readout circuit. The pixel is laid out with a $38\,\mu$m pitch. The DPS array occupies $2500 \times 1900\,\mu\text{m}^2$ and uses 915,456 transistors.

accurately modeled by [18]:

$$y(x) = a + b\log(c + x) + \epsilon. \tag{5.1}$$

Whereas a, b, and c are temporally-constant spatially-varying parameters, ϵ is temporally-varying noise with spatially-constant statistics. 3-parameter (a, b, and c) correction was implemented in real time on a PC connected to the image sensor. 3-parameter calibration was done once offline after capturing 20 images from a uniform scene at different luminances. The PC also implemented 5-point median filtering in real time to replace each dead

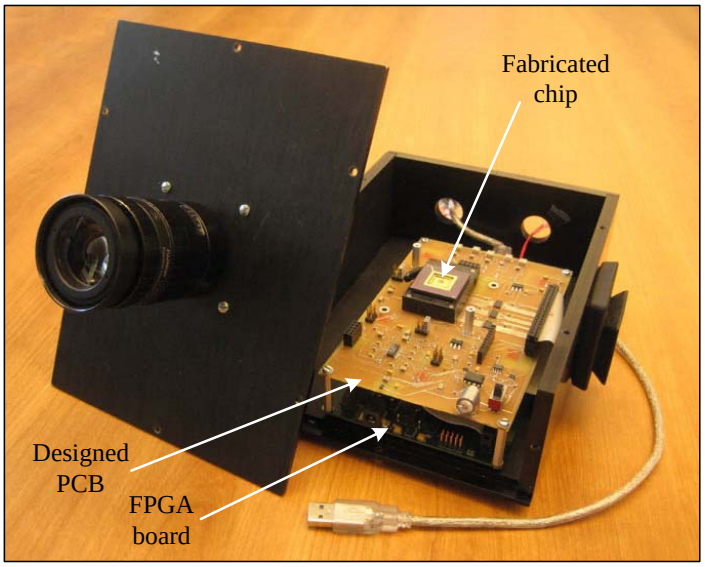


Figure 5.5: Photo of a digital camera including the body, the FPGA board, the PCB, and the fabricated chip. The camera body was designed by Orit Skorka, another student in the lab.

pixel with a nearest neighbour.

Non-uniformity or variation of luminance in the scene affects FPN calibration. Sunlight was used as the light source for calibration and photos were taken of its reflection off a clear patch of sky. In order to make the scene more uniform, the lens is focused near. Unlike the light from a lamp, sunlight does not have any oscillations. Measurements were done at noon on days with no clouds to minimize spatial and temporal variations in stimulus. By changing the aperture of the lens, which is already calibrated, the effective luminance can be controlled.

For each pixel, the result of FPN correction and median filtering is an estimate $\hat{x}$ of the true x. The difference $x - \hat{x}$ measures noise and distortion. The SNDR is determined as the ratio of true x to the RMS noise-and-distortion:

$$SNDR(x) = \frac{x}{\sigma_{nd}(x)}. \tag{5.2}$$

If $\bar{x}$ is the temporal average of $\hat{x}$ then the difference $\bar{x} - \hat{x}$ measures noise only, and the ratio of true x to the RMS noise measures SNR:

$$SNR(x) = \frac{x}{\sigma_{n}(x)}. \tag{5.3}$$

5.2.1 Experimental Setup

In order to test the image sensor, a PCB and a camera body equipped with a lens was designed. Fig. 5.5 gives a picture of the setup. As with our

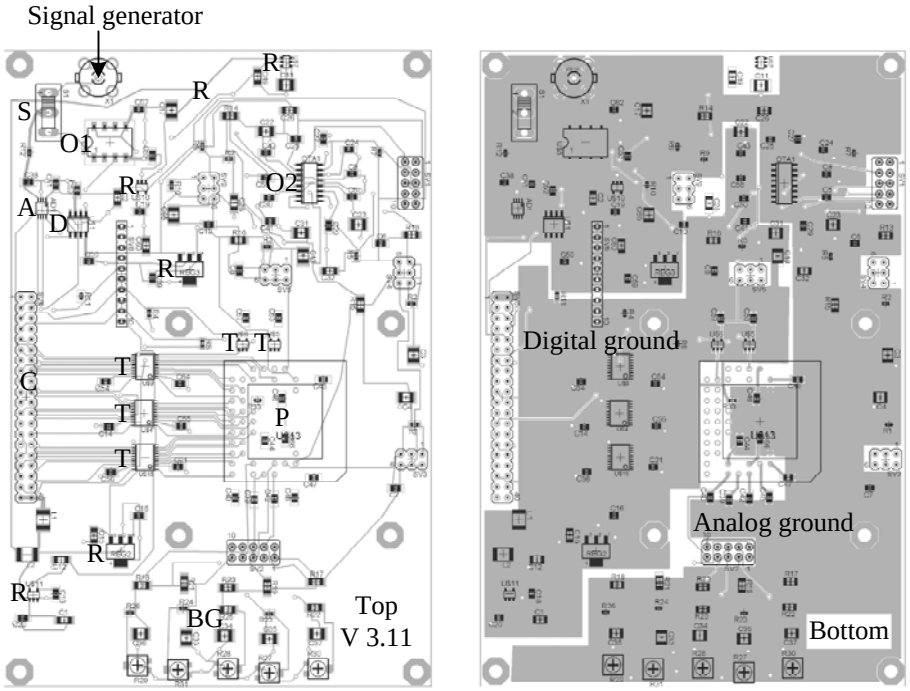


Figure 5.6: Layout of the designed PCB for characterization of the image sensors, showing the LVDS connector (C), PGA68 package (P), commercial ADC (A), commercial DAC (D), switch (S), buffer OPAMP (O1), voltage regulators (R), bias-voltage generator (BG), translators (T), and low-offset OPAMP (O2).

previous design in Chapter 4, the PCB is connected to a board incorporating an Altera Cyclone II FPGA. The PCB and FPGA board are mounted inside the camera body. Digital inputs and outputs of the chip are connected to the FPGA via buffers and level converters. The FPGA is interfaced to a PC over USB using a QuickUSB module from Bitwise Systems. Thereby, the chip is controlled with enough flexibility to implement various testing methods. The frames are captured in the PC and after FPN correction and image processing through software, image frames are displayed.

Figure 5.6 shows a layout of the PCB. The PCB and the FPGA board are connected via a 40-pin LVDS connector. The chip is mounted in a PGA68 package. For other testing purposes, a commercial ADC and a commercial DAC are mounted on the PCB, which are not used in the characterization of the image sensors. Using a switch, the input of the commercial ADC can be selected between the DAC output and the signal generator output.

Analog and digital testing points are available across the PCB for testing and monitoring. A bias-voltage generator is used to provide the required analog signals of the chip. Voltage regulators convert the 5V provided by

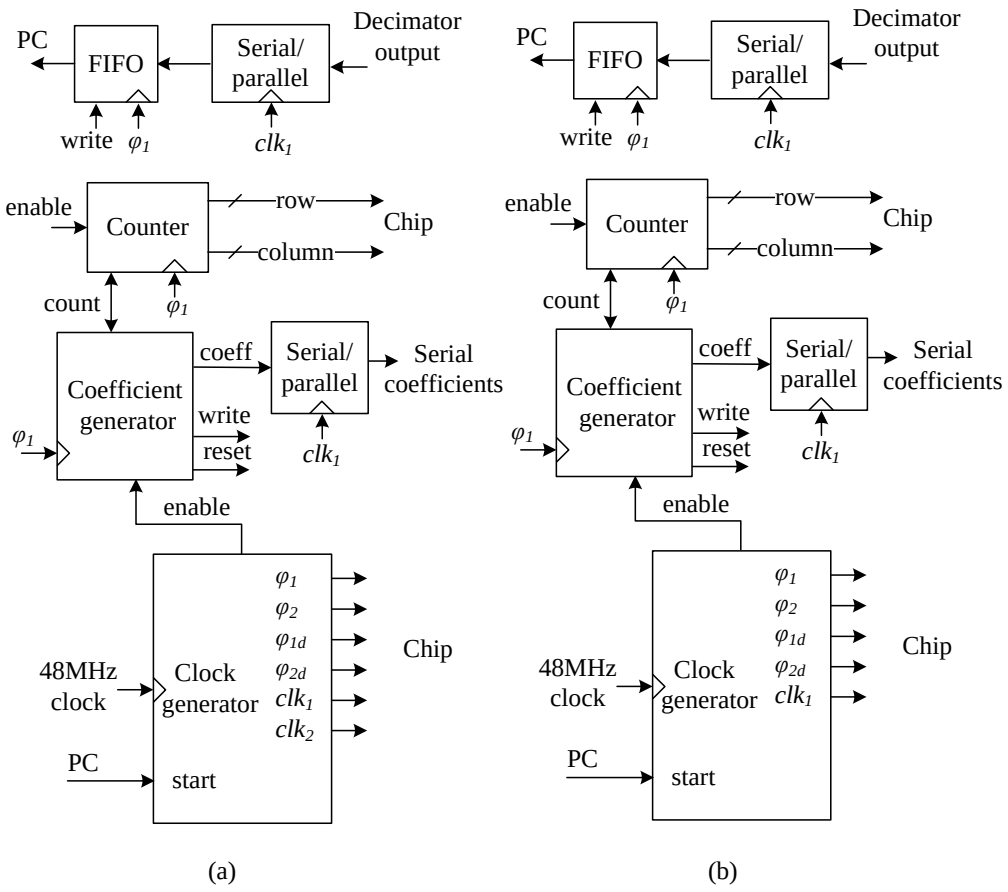


Figure 5.7: Block diagram of the circuits designed in the FPGA for (a) characterization of the DCS and (b) characterization of the DPS.

the FPGA to the required digital and analog supply voltages in the PCB. The required digital signals of the chip are produced by the FPGA and are sent to the chip. Translators are employed to buffer and convert the digital voltage levels of the chip and the FPGA. In order to measure the power consumption of the chip, input currents of the chip are sensed with 1 Ω resistors. The voltage across each resistor is amplified and low-pass filtered using low-offset operational amplifiers.

The PCB is designed with special care to minimize interference and noise. Analog and digital grounds are separated. The bottom layer is mostly used as a ground plane. To reduce the interference of digital signals over sensitive analog signals, analog and digital circuits are isolated and laid out over separated and corresponding ground planes.

Two FPGA circuits were designed and implemented to capture and process the modulator or decimator outputs from both image sensors. Block diagrams of these digital circuits are shown in Fig. 5.7. The required digital signals are generated in the FPGA using a 48 MHz clock available in the

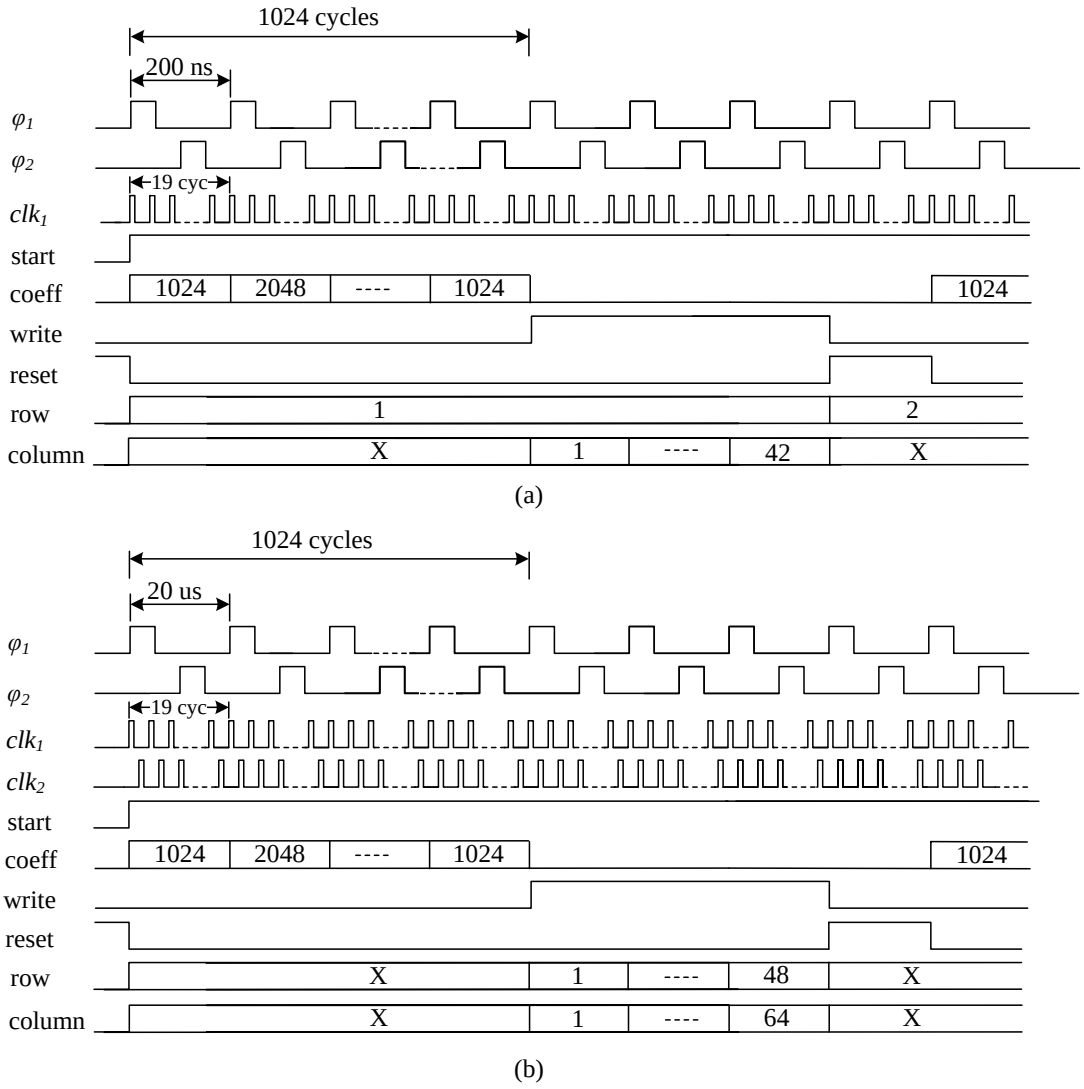


Figure 5.8: Signal waveforms generated in the FPGA for (a) the DCS and (b) the DPS. Coefficients are generated for an oversampling ratio of 1024, which are also the values of the first and the last coefficients.

FPGA. Also, the coefficients of the decimator are generated in the FPGA and are sent to the chip serially. The captured data in the FPGA is stored in a FIFO buffer, which is periodically read by the PC over USB.

A sample waveform of the signals in the FPGA is shown in Fig. 5.8. The oversampling ratio is 1024. In the DCS array, sampling begins with the selection of a row of pixels. The decimator is reset before the sampling starts. During the oversampling period, coefficients are generated and are sent to the decimators. After each oversampling period, the data from 84 ADCs are read out in sequence. For one frame, each ADC samples the outputs of 96 rows. In the DPS array, after the decimator is reset, generated coefficients are distributed to all pixels in the chip. At the end of each oversampling

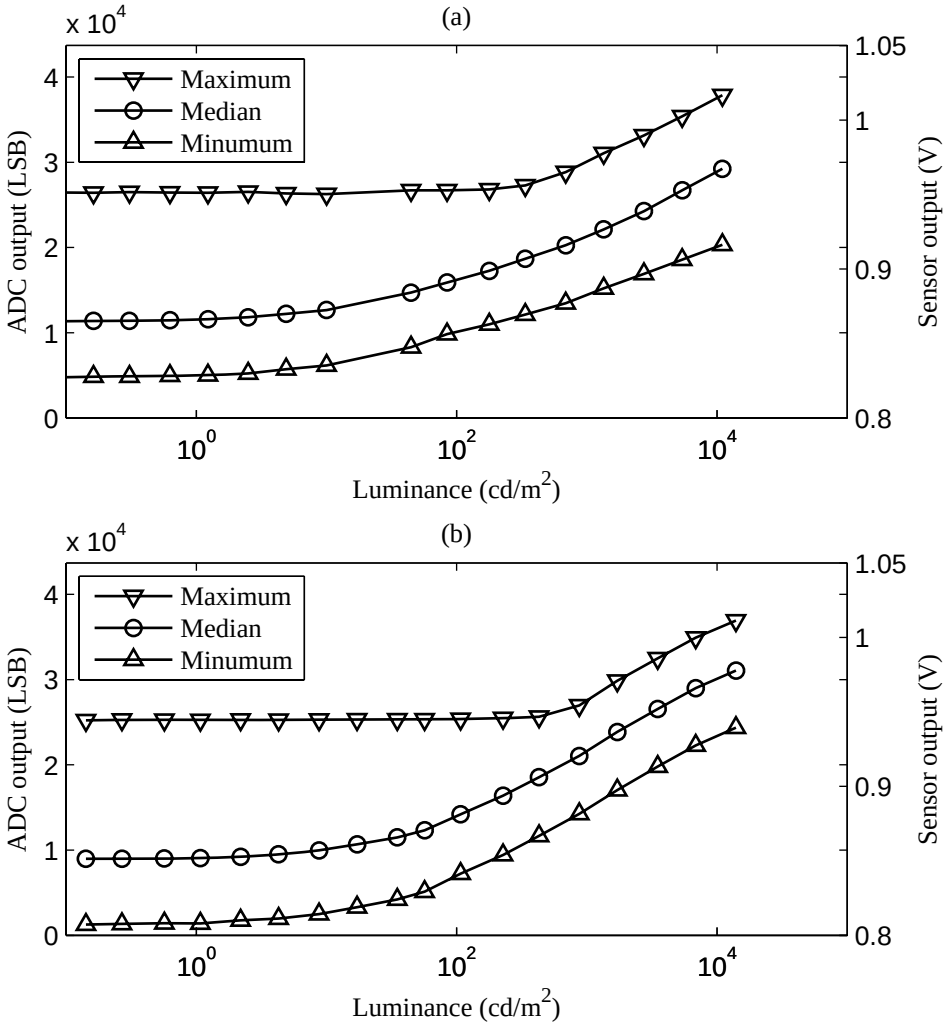


Figure 5.9: The maximum, median, and minimum ADC output of all pixels versus scene luminance with (a) the DCS and (b) the DPS. Sensor output is calculated using fixed ADC reference voltages (.8 and 1.05V). Luminance of the uniform scene is measured with a Sekonic L-758CINE meter.

period, the output of 48×64 pixels are read out serially.

5.2.2 Experimental Results

DCS and DPS arrays were tested with a uniform patch of clear sky at 18 different light levels. Fig. 5.9 plots the ADC and sensor output versus luminance input for both arrays. The maximum value of the ADC output is 43691 LSB, which is determined by the oversampling ratio. In both cases, output varies greatly across the array because of FPN, which always exists in logarithmic sensors. The main cause of FPN is threshold variation of the

transistors inside pixels.

One advantage of logarithmic sensors is the compression of a high luminance DR to a low voltage range. The input range of all ADCs is defined by two external references, which are set on the PCB to cover the 250 mV range shown. However, the ADCs are able to cover up to a .7 V range in this 1.8 V technology. Because delta-sigma ADCs are capable of high precision and accuracy in low voltage processes, it makes sense to combine them with logarithmic sensors.

All 48×64 ADCs in the DPS array worked. However, with the DCS, 8 out of 84 modulators (9.5%) did not function because of mismatch effects. Varying the bias point of the OTA changes the number of functional modulators, showing that the OTA is sensitive to mismatch. Columns related to the dysfunctional modulators were removed from the picture. Also, because of a timing issue, most of the decimators did not work in the DCS. Therefore, the output of the modulators are decimated by the FPGA instead. This reduces the frame rate of the DCS by the number of columns.

Fig. 5.10 shows the cumulative distribution function (CDF) of number of pixels versus SNDR and SNR for different oversampling ratios. In both of the arrays, SNR and SNDR vary among the pixels because of mismatch variation in the delta-sigma ADC and FPN in the logarithmic sensor.

An advantage of using the delta-sigma ADC is that frame rate can be traded with bit resolution. As shown in Fig. 5.10, using a higher oversampling ratio, higher SNDR is achieved at the cost of a lower frame rate.

Fig. 5.11 shows the median of SNDR versus luminance for both image sensors. SNDR of the sensor outputs are calculated after FPN correction with three parameters per pixel and median filtering. In the DCS, the peak SNDR is 35 dB. In the DPS, the peak SNDR is 46 dB. As expected, the DPS is more successful in reducing noise and distortion.

Median SNR of both image sensors versus illumination at different oversampling ratios is shown in Fig. 5.12. The peak SNR for the DCS is 39 dB, while this value for the DPS is 49 dB. In both cases, it is hard to measure the upper limit of the dynamic range because the input luminance received from the sky is limited to almost $10,000\,\mathrm{cd/m^2}$. The lower limit is set by the dark current in the image sensor.

Fig. 5.13 shows images of scenes captured with the DCS and DPS arrays. Each scene is imaged at 4 effective luminances spanning 48 dB. With the DCS, the luminances across each image span 18 dB, totaling 66 dB across all images. With the DPS, the luminances across each image span 38 dB, totaling 86 dB across all images. The luminance of a scene feature is indicated for all images, and is cross-referenced in Figs. 5.11 and 5.12.

For both image sensors, the image quality of non-uniform scenes can be explained based on the SNDR performance with uniform scenes. Features look good where SNDR rivals that of the human eye, or 40 dB according to Webers law [19]. For higher light levels, the SNDR is high and good picture

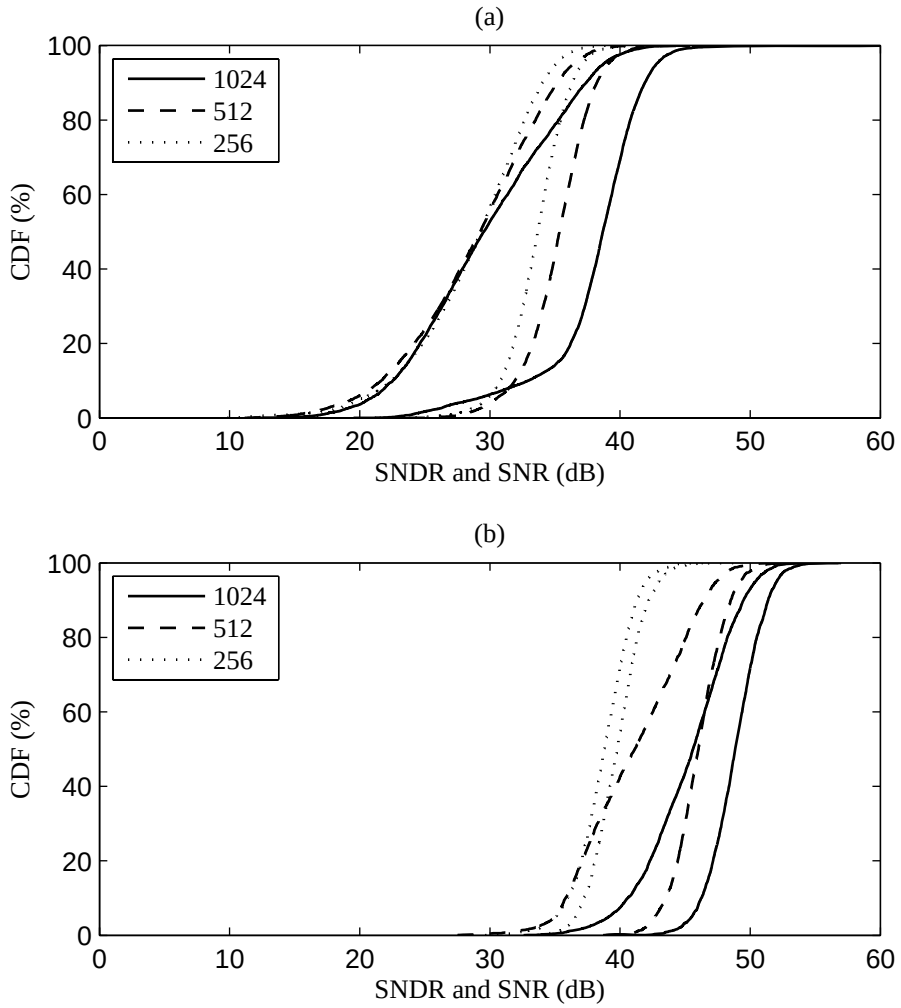


Figure 5.10: Cumulative distribution function of pixel count versus SNDR and SNR, at three oversampling ratios, with (a) the DCS for a $5,400\,\mathrm{cd/m^2}$ uniform scene and (b) the DPS for a $7,000\,\mathrm{cd/m^2}$ uniform scene. Left and right curves of each line style represent the SNDR and SNR, respectively.

quality is achieved. For lower light levels, the SNDR is low and, therefore, the picture quality is fair or poor. This could be improved by reducing the dark current of the pixels, which limits performance, as shown in Fig. 5.9.

Although the camera can capture a large dynamic range, rendering and showing the image using only the 8 bits suitable for display is difficult. At present, the PC maps tones $\hat{x}$ for display in real time using a simple method. Given a white point, whiter tones are saturated before scaling, gamma correction, and bitmap conversion. More complex tone mapping is possible, to improve the effective dynamic range of the displayed image.

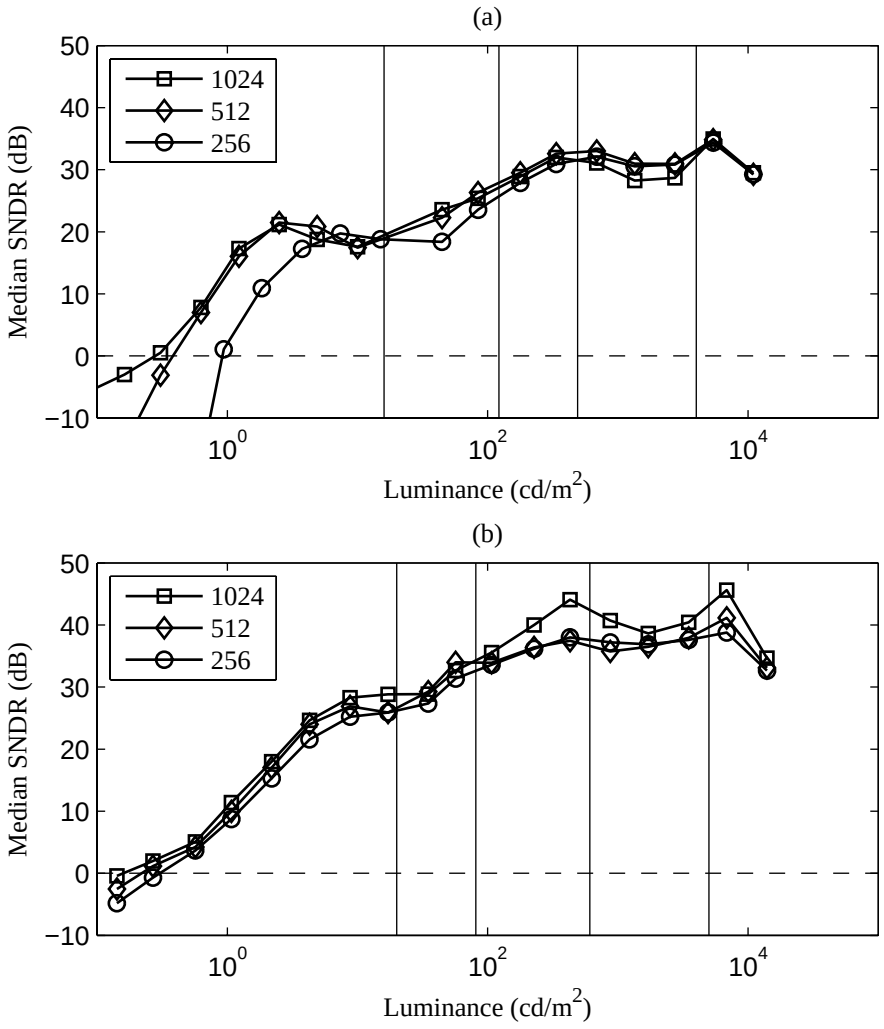


Figure 5.11: Median SNDR of all pixels versus scene luminance and three oversampling ratios with (a) the DCS and (b) the DPS. Effective luminance is varied using 9 aperture settings on the camera lens and a calibrated HOYA NDx400 neutral density filter. Vertical lines mark highlights in Fig. 5.13.

5.2.3 Figures of Merit

In this section, performance of the fabricated image sensors are compared to recent works on image sensors, showing that by using the proposed DCS and DPS architectures, performance of the logarithmic sensors is competitive with the state of the art. Specifications of the designed DCS and DPS circuits are given in Table 5.2. The DPS has lower dark limit with higher SNDR and SNR. But the DCS has smaller pixels and lower power consumption.

The image sensor of Storm *et al.* [20] uses a linear mode for low lu-

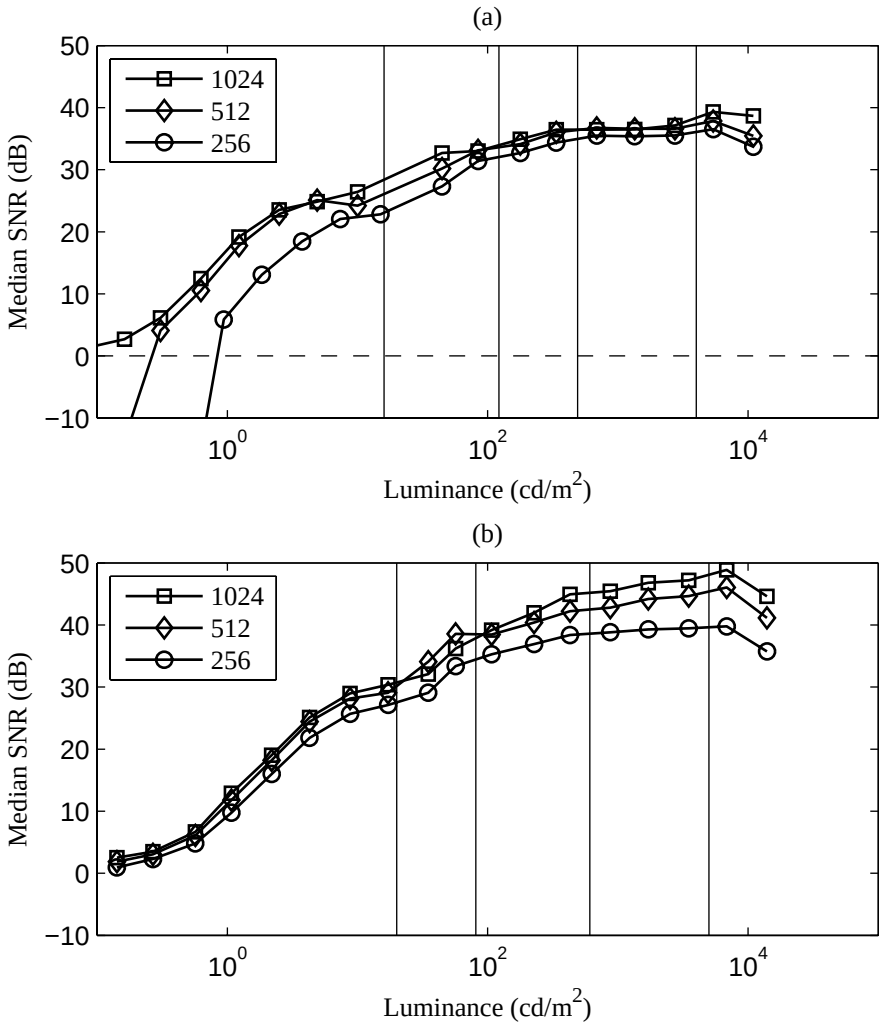
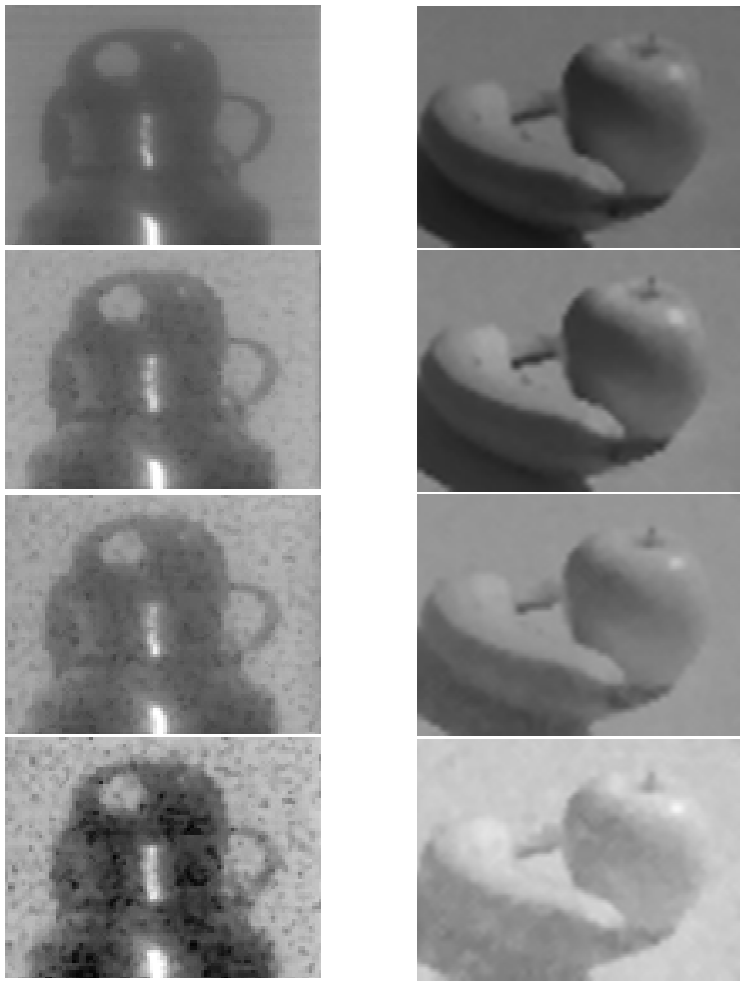


Figure 5.12: Median SNR of all pixels versus scene luminance and three oversampling ratios with (a) the DCS and (b) the DPS. Vertical lines mark highlights in Fig. 5.13.

minance and a logarithmic mode for high luminance. Although SNDR is not given, 32 dB peak SNR (PSNR) and 2% residual FPN per decade are reported in the logarithmic mode. Assuming output-referred noise-and-distortion are uncorrelated, peak SNDR (PSNDR) is calculated to be 26 dB. Ruedi *et al.* [25] employ time-domain logarithmic encoding to increase the dynamic range of linear sensors. The PSNR is reported to be 40 dB and residual FPN is .8% per decade. Based on that, the PSNDR is determined to be 34 dB.

The DCS and DPS achieve 35 dB and 46 dB PSNDR respectively, which are 9 dB and 20 dB higher than the state-of-the-art logarithmic sensors by Storm *et al.* [20]. Compared to some non-logarithmic sensors, however, the



(a) (b)

Figure 5.13: Images of non-uniform scenes, using 4 aperture settings on a Fujinon CF25HA-1 lens. The images are taken with (a) the DCS and (b) the DPS. With the DCS, lower highlights from top to bottom are 4,000, 490, 122, and 16 cd/m^2. With the DPS, apple highlights are 5,000, 610, 81, and 20 cd/m^2. Tones are mapped for display using the sRGB specification.

PSNDR is smaller. Nonetheless, the PSNDR of the DPS is high enough compared to the human eye. Higher SNDR cannot be perceived by the human eye. The main issue is at low light levels, where performance could be improved by reducing the dark current of the sensor. The main advantage of this method is that a high dynamic range can be easily achieved.

Dynamic range of the DCS and DPS are measured to be 91 and 96 dB, respectively, which are the ratio of maximum and minimum light levels in between which the SNDR is greater than zero. It was not possible to get a brighter uniform scene with natural lighting and show a higher DR.

Table 5.2: Specifications of the DCS and the DPS arrays. Due to lens geometry, 1 cd/m^2 in the scene implies .4 Lx on the sensor. With the DCS, because the decimators do not function properly, the modulator output is read out. Hence, frame rate is limited to 1.2 fps. If the decimator output could be read out, frame rate of the DCS would be 51 fps.

Parameter	DCS array	DPS array
Process	0.18 μm 1P6M CMOS	0.18 μm 1P6M CMOS
Analog power	290 μW	4.5 mW
Digital power	2.4 mW	11.2 mW
Video rate	1.2 fps (51 fps)	30 fps
Array size	96×84	48×64
Pixel size	8 μm $\times$ 8 μm	38 μm $\times$ 38 μm
Fill factor	33%	2.33%
Median SNDR	35 dB at 5400 cd/m^2	46 dB at 7000 cd/m^2
Median SNR	39 dB at 5400 cd/m^2	49 dB at 7000 cd/m^2
Dark limit	.30 cd/m^2	.16 cd/m^2
Dynamic range	> 91 dB	> 96 dB

Although Storm *et al.* [20] and Ruedi *et al.* [25] report dynamic ranges of 143 and 132 dB, as measured for SNR greater than zero, their dark limits appear comparable to this work. Assuming a long integration time, the 726 mV/Lx/s sensitivity and 37.3 mV/s in the linear mode of the first work [20] suggests a .051 Lx dark limit. Supplementary material of the second work [25] shows a .033 Lx dark limit. When measured for SNR greater than zero, dark limits of the DCS and DPS are below .11 Lx and .056 Lx. Given that human colour vision extends to .001 cd/m^2, it is equally important to reduce dark limit for our method and the literature methods.

5.3 Discussion

With both the DCS and DPS, high SNDR (and SNR) is achieved at high light levels. But at low luminance, SNDR (and SNR) drops as dark current dominates the response, which effectively reduces the image quality. This may be mitigated with better CMOS photodetector design and layout. With the DPS, an alternate strategy is to exploit vertically-integrated CMOS technology [91]. For example, CMOS and photodetector dies may be fabricated independently and then assembled by fine-pitch flip-chip bonding. Photodetector dies may be designed to boost photo-to-dark current ratios. CMOS dies with pixel-level delta-sigma ADCs and logarithmic front-ends may be designed for nanoscale processes, including ones unsuitable for photodetection. In this manner, pixel size and power consumption may be reduced.

The difference between SNR and SNDR measures the residual distortion or nonlinearity component in the output signal. Nonlinearity is generated either from the ADC or the sensor. Some of it is treated by FPN correction. Because the OTA of the delta-sigma modulator is designed in a very small area, mismatch variation can affect the OTA bias point, unity gain bandwidth (UGB), and slew rate (SLR). Degradation of UGB and SLR will cause more nonlinearity in the ADC output. The ADCs were designed using an incomplete design flow. The impact of mismatch issue within the ADCs can be greatly reduced using the completed design flow.

The DCS array has the advantage of higher spatial resolution, while the DPS array has higher SNDR (and SNR). Also, with the DCS array, each ADC is biased at a higher power consumption, at which the variation in performance is reduced.

With the DPS, the pixel size is large, which makes it more suitable for applications other than visible-band imaging, such as infrared imaging. The pixel size can be decreased using technologies smaller than $0.18\,\mu$m. Also, the register size in the decimator can be reduced based on the required SNDR. Another way to reduce the area is to lay modulator capacitors on top of the decimator. This violates the design rules but, as digital circuits are less susceptible to noise, we expect that performance will not be affected.

5.4 Conclusion

For this chapter, DCS and DPS arrays were designed, built, and tested. With these image sensors, SNDR is improved compared to state-of-the-art logarithmic image sensors. The test platform that was developed included a PCB and FPGA circuits. Also, C++ and Matlab programming were employed to process the captured data in real time on a PC.

The experimental results show that column or pixel-level data conversion using delta-sigma ADCs are feasible methods to enhance the SNDR of logarithmic image sensors. These results represent a significant step towards the goal of realizing an image sensor that rivals the human eye. The DPS achieved better performance, partly because more readout noise is filtered. In both image sensors, the SNDR is still low at low light levels because of dark current. This could be improved by designing a sensor with lower dark current. For example, using vertical integration, a photodiode could be fabricated in a long channel process with smaller dark current. SNDR variability in both image sensors is partly due to mismatch within the ADC. The ADC performance could be improved using the completed design flow presented in Chapter 3.

In this chapter, it was shown that using the delta-sigma ADC in focal plane processing is a feasible approach to improve the performance of logarithmic sensors. Similarly, the proposed approach may be used in other sensor arrays. Employing delta-sigma ADCs is a strategy that is robust to

mismatch and suitable for low-voltage technology. As CMOS technology scales down to the nanometer range, more transistors can be put into each pixel or column and the focal plane processing becomes more applicable to array sensors requiring smaller pixel sizes.

Chapter 6

Conclusion

Delta-sigma ADCs have been mainly used for low-bandwidth high-resolution applications such as digital audio. The main advantage of delta-sigma ADCs over Nyquist-rate ADCs is the fact that they have more tolerance to the non-idealities of analog circuits, which is a serious concern in low-voltage processes [3]. Additionally, there is no need for a sharp low-pass filter before sampling the analog signal. With ongoing advances in speed and sizing of VLSI technology, new applications of delta-sigma ADCs are appearing. One important field is array sensors, which includes video sensors, infrared cameras, biosensors, DNA detection, and X-ray imagers, where the analog signal output of large numbers of sensors needs to be efficiently converted to a digital signal [11, 14, 59].

Digital video increasingly demands better quality at a lower expense [15]. Better quality includes higher SNDR, dynamic range, frame rate, and pixel resolution. Lower expense means lower power consumption, smaller die, smaller pixel size, and cheaper fabrication. Smart focal plane processing is a well-known solution, which is expected by many experts to be the future of video sensors [31]. Delta-sigma data conversion as focal plane processing, i.e., as column or pixel-parallel data conversion, has several benefits at the cost of requiring high-speed small-size components, which are becoming cheaper thanks to advances in VLSI technology.

CMOS image sensors are either linear, logarithmic, or a variation of one or both [16, 20]. Linear sensors are well known to achieve high SNDR, mainly through their use of integration. Unfortunately, they have a low dynamic range. On the other hand, logarithmic sensors convert light intensity into voltage using a logarithmic scale. A high dynamic range is achieved; however, these sensors are not widely used because of low SNDR and high FPN. New methods have been proposed for FPN correction; therefore, FPN is less problematic in these sensors [18]. Having a low SNDR remains the main issue in logarithmic image sensors. By employing the architectures proposed in this thesis, the SNDR of logarithmic sensors can be improved. This would enable the development of image sensors enjoying high SNDR, high DR, and high frame rate.

Similar to the source coding methods used to digitize voice signals, which are based on the non-uniform probability distribution of the signal, logarithmic compression is an efficient source coding method for image sensors [92]. A wide range of illumination is mapped into a small voltage range, which must be digitized. This voltage range is even smaller in low-voltage technologies.

The delta-sigma ADC is very well suited for low-voltage technologies; thus, it is a suitable architecture to digitize the output signal of logarithmic sensors. Unlike Nyquist-rate ADCs, delta-sigma converters can remove out-of-band noise and achieve a high SNR in a small voltage range. Using delta-sigma ADCs, the advantages of column and pixel-parallel data conversion are fully realized. However, the area usage and power consumption of the ADC is a major constraint that needs to be minimized.

This thesis explored the design of delta-sigma ADC arrays, where there is one ADC per column or per pixel in an array of sensors. The method presented was applied to logarithmic sensors. Advantages were shown and challenges were discussed. The main contributions of the thesis are summarized in Section 6.1. Section 6.2 discusses avenues for future work.

6.1 Contributions

Area usage and power consumption are two major constraints in column and pixel-parallel data conversion. Thus, ADCs should be designed in a small area and for low power. This thesis introduced a novel design flow for reducing the area usage and power consumption of delta-sigma ADCs for parallel data conversion. Part of the design flow has been published in refereed conference proceedings [93, 94]. A patent application regarding innovations in the decimator and part of the modulator has been filed in the US and Canada [95]. Unlike previous works on delta-sigma ADC design, the focus of this work is not only to decrease the power consumption, but also to reduce the area usage of the ADC so that it can fit inside a pixel and also be efficient for the column-level approach.

The contributions of this thesis are categorized into four sections. Section 6.1.1 summarizes a novel decimator design flow for array ADCs, which provides a means to minimize area and power given a certain noise specification. Section 6.1.2 summarizes a modulator design flow, which complements the decimator design flow and reduces the area and power of the modulator. Section 6.1.3 reviews two delta-sigma ADCs with comparable performance to state-of-the-art delta-sigma ADCs but substantially less area; the pixel-level ADC is also the first to integrate in-pixel decimation. Section 6.1.4 reviews two logarithmic image sensors having column and pixel-level delta-sigma ADCs; they achieve higher SNDR compared to state-of-the-art logarithmic image sensors.

6.1.1 Decimator Design Flow

Conventional decimation circuits have not been designed for small area. Instead, the focus has been mainly to minimize the power consumption for a single ADC [4]. In this thesis, a new design flow was proposed for decimation in parallel data conversion, which is applicable to both column and pixel-level delta-sigma ADCs. Given a specified noise requirement, this design flow provides a means to minimize area usage and power consumption for ADC arrays, making it possible to perform decimation inside the pixel or more efficiently at the column. A key aspect of the design is to reduce the number of transistors insofar as possible.

In the previous works on column-level delta-sigma ADCs, the decimation, mostly using a counter for first-order approaches [28, 31, 54], is performed inefficiently. Hence, a higher oversampling ratio is required for a certain SNR, which leads to higher power consumption. Though neglected, small area is important because, as shown in Chapter 5, the ADC takes a considerable portion of the die area. Reducing the area leaves more room for the pixel array and allows a bigger array to occupy the same die size.

Also, in previous designs of pixel-level delta-sigma ADCs, the decimator was implemented outside the pixel [7, 8, 36]. The decimator input has a much higher bit rate compared to its output and readout speed of an image sensor is limited by bus capacitance. Therefore, by performing the decimation outside of the pixel, the oversampling ratio, frame rate, and window size are limited. A limited oversampling ratio leads to a limited SNR.

The optimal decimator filter for a first-order delta-sigma ADC has a parabolic shape [4]. In prior art, this decimator is approximated using a multi-stage process [3]. A triangle-shaped comb filter is implemented in the first stage. The filter may be realized using one of various methods, such as IIR-FIR, FIR2, and POLY-FIR2. Among them, IIR-FIR has the smallest area [69]. It needs two accumulators and two differencers, which are implemented using 80-bit registers with 4 multi-bit adders. Truncation or rounding may be used at each filter stage to reduce the size of the registers at the cost of introducing some rounding error.

In contrast, this thesis introduces a decimator design realizable using a multi-bit register and a one-bit adder. The area of this method is smaller than the IIR-FIR method. Moreover, the circuit layout is customized to reduce the area further. The optimum parabolic filter is implemented, which achieves a higher SNR. Decimation is accomplished using an FIR filter, which is implemented by an accumulator. The coefficients of the filter are generated at the chip level and are sent to each pixel or column.

The accumulator is implemented using bit-serial addition to reduce the area even more. Since the input signal is one bit, the multiplication is done using an AND gate. In the column-level ADC, the AND gate is not even needed since the modulator output can be the clock input of the accumu-

lator, which has the same effect. The coefficients of the filter are generated at the chip-level based on the required oversampling ratio and are sent to the accumulator serially. At the end of a Nyquist interval, each decimator is read out and the accumulator is reset.

The accumulator size is specified based on the required output-referred noise of the ADC, which is determined according to the specifications of the image sensor. Similarly, the coefficients are also rounded at the chip level so that a smaller accumulator may be realized. The generated rounding error is negligible compared to the ADC output-referred noise.

Conventional decimation methods are more appropriate to build one ADC but, with multiple ADCs, the method presented in this thesis is more area efficient and less power hungry because some of the circuitry can be placed at the chip level. Thereby, the decimator can be placed inside the pixel and it is also more efficient for column-level data conversion.

6.1.2 Modulator Design Flow

Similar to the decimator design flow, the main goal of the modulator design flow is to reduce the area usage and power consumption, while achieving a low output-referred noise. Previous works on delta-sigma column and pixel sensors, because of area limitations, mostly use very simple circuits with a non-differential architecture in the modulator, which are susceptible to noise and have limitations in achieving high SNR. The SNR limitation is more problematic when the decimation is performed inside the pixel and more noise is injected into the analog circuits of the modulator.

In the proposed design flow, the modulator is designed based on the performance requirements of an image sensor, which are translated to the output-referred RMS noise-and-distortion, sampling rate, and input voltage range of the ADC. The modulator is designed using theoretical modeling, behavioural simulation, and circuit simulation. While the theoretical model of the circuit has less precision, it requires a short processing time. On the other hand, behavioural simulation requires a longer processing time but a moderate accuracy is achieved. The circuit simulation has the highest precision with the longest processing time. Using a combination of the three methods, the modulator design flow introduced in this thesis achieves a high accuracy in a short amount of time.

In the theoretical model, all non-idealities of the modulator are referred to an input noise source. A threshold level is defined based on the required output-referred noise-and-distortion. Then, the maximum noise power for each non-ideality is derived and referred to the input. Each analog component is designed based on the maximum allowed non-ideality. The OTA is designed with enough DC gain, UGB, and SLR. Sampling and integration capacitor sizes are determined based on the kTC noise limitation and capacitor matching requirements.

In the behavioural simulation, all the components of the modulator were abstracted in Simulink. This included a model for a slewing integrator with limited bandwidth, which plays a key role in determining the performance of the modulator. The model was used to calculate the output-referred noise-and-distortion of the modulator and confirm that the required performance was achieved.

Next, using specifications derived from the behavioural simulation, the modulator is designed and simulated in Cadence to ensure that the required performance is achieved. The output of the modulator in circuit simulation was imported into Simulink for decimation and performance calculations. Decimation was performed in Simulink because the digital part of the design was expected to work perfectly in circuit simulation.

Mismatch was also considered in the design flow. The heart of the modulator, the OTA, has to be designed with enough tolerance to mismatch variation, which is a serious concern in low-area analog design. Smaller circuits are more susceptible to mismatch. For a given ADC yield, minimum transistor sizes in the OTA were determined. Also, using different layout techniques, the OTA was laid out to tolerate the maximum possible variation.

A first-order architecture was selected for column and pixel-level data conversion because it reduces area through a simpler structure and smaller capacitors, as compared to higher-order modulators. Previous works on delta-sigma modulators for single ADCs mostly use higher-order designs to decrease the oversampling ratio and, therefore, to reduce the power consumption. A higher oversampling ratio is required in the first-order modulator but the capacitor size is smaller. Also, higher-order modulators need more hardware. Therefore, power consumption of the first-order modulator may be comparable to higher-order designs.

In this thesis, it was shown that, unlike higher-order structures, very small capacitors can be used in the first-order modulator because the first-order modulator is not sensitive to capacitor mismatch, which is problematic with small capacitors. Power consumption of the circuit is directly proportional to the capacitor size of the load. Thus, despite having a high oversampling ratio, the first-order modulator has a low power consumption by using very small capacitors.

The modulator uses a differential architecture, while output of the pixel sensor is single-ended. Therefore, a novel circuit was designed to use the pixel output in differential mode. The number of transistors was reduced further for the pixel-level modulator. As the pixel-level modulator works at a lower speed, single transistors were used instead of transmission gates. This simplified design lessened the area of the modulator. The comparator in the column-level ADC was modified to work at a lower speed and with less power consumption for the pixel-level ADC.

Overall, a design flow was proposed to realize a low-area low-power

modulator suitable for delta-sigma ADC arrays. The low area of the modulator makes it more vulnerable to mismatch. This was considered in the design flow and the minimum transistor sizes were determined according to the required yield. As examples, two modulators were designed based on the performance requirements of a logarithmic image sensor.

6.1.3 Data Converter Advances

Using preliminary versions of the decimator and modulator design flows, two arrays of stand-alone ADCs were designed and fabricated in 0.18 μm CMOS technology. The design and testing of the fabricated ADCs validated the decimator and modulator design flow and realized specific designs, enabling comparison to the state of the art.

Yield is an important parameter in array ADC design. In single ADC design, performance of one ADC is typically reported and variation is not explained. This makes sense since, after fabrication, each ADC is tested and if the performance is not as expected, chips are discarded. But in array ADC design, a certain percentage of the ADCs must work properly. Therefore, ADCs are designed for a certain yield. Also, it is important to measure the performance across the array. A testing system was automated to test all ADCs. To do so, in contrast with the sinusoid input method, the ramp input method was used, which could be easily automated. It is harder to implement the sinusoid input method automatically.

An automated measurement system was developed and all the ADCs were tested automatically. The chip was mounted on a designed PCB, which was equipped with an FPGA. The FPGA was also connected to the PC over USB using a QuickUSB Module. Therefore, the testing procedure was fully controlled by programming the FPGA and the PC. Using this platform, RMS noise-and-distortion and RMS noise of each ADC versus power consumption of the modulator were measured using a ramp input signal. The ramp signal was generated using a DAC mounted on the PCB.

The column-level modulator was designed for a .064 mV output-referred noise in a .7 V voltage range with a 50 kHz sampling rate. It was laid out with a 16 μm pitch. The decimator was implemented in the FPGA. The ADCs achieved an RMS noise-and-distortion with maximum, median, and minimum values of 1.8, 1.0, and .4 mV, respectively, at a power consumption of 79 μW. Maximum, median, and minimum of the measured RMS noise was .35, .14, and .10 mV, respectively. The ADCs had very low power consumption but had a higher noise level compared to design specifications.

The pixel-level ADC was designed with similar specifications as the column-level ADC except with a 50 Hz sampling rate. The layout of the pixel-level ADC was customized to fit in a pixel. The decimator was designed with a register using 19 D flip-flops and a one-bit adder. Each D

flip-flop was implemented using pulsed latches with only 8 transistors and was laid out compactly with an area of $2.4\,\mu m^2$ per transistor. In contrast, a layout using standard cells occupies almost $8\,\mu m^2$ per transistor. Experimental results demonstrated that 100% of the decimators functioned perfectly. The modulator was implemented in two different versions, one with a large OTA and the other with a small OTA. The median ADC using the large OTA achieves 5 dB lower RMS noise-and-distortion and 6 dB higher RMS noise compared to the median ADC using the small OTA. Both ADCs consumed $3\,\mu W$ power. In the ADCs using the large OTA, RMS noise-and-distortion and RMS noise have medians of .30 and .11 mV, respectively.

The main factor limiting performance in the column and pixel-level ADCs was mismatch, which was not simulated at the time of design. The pixel-level ADC with the large OTA was less sensitive to mismatch; therefore, lower RMS noise-and-distortion was achieved. Once the effect of mismatch on the performance of the ADCs was incorporated into the behavioural model, the ADCs were simulated again in Simulink. These updated simulation results match the experimental results of the ADCs. This shows that the behaviour of the modulator was modeled accurately.

Compared to state-of-the-art switched-capacitor modulators in the literature, the area usage of column and pixel-level ADCs is smaller in this work. For example, the area of the column-level modulator is 227 times smaller than the modulator presented by Roh *et al.* [61] and the area of the pixel-level modulator is 670 times smaller than the same. Although, in both cases, the figure of merit is not currently the best, the performance can be improved using the completed design flow presented in Chapter 3.

Performance of the fabricated column and pixel-level ADCs is limited because of mismatch, which can be predicted using the developed theoretical and behavioural model. While performance of both ADCs is comparable to the state of the art, the area is substantially smaller than in prior works.

6.1.4 Image Sensor Advances

Two arrays of logarithmic image sensors, one using column-level data conversion and the other using pixel-level data conversion, were designed and fabricated in $0.18\,\mu m$ CMOS technology using 1,004,786 transistors. Data conversion in both cases was done using delta-sigma ADCs. The main goal was to evaluate and compare the performance of these two approaches. Compared to state-of-the-art logarithmic sensors, the experimental results show that in both cases the SNDR has been improved while a high dynamic range is achieved. The key contributions of the thesis regarding the image sensor design and testing results are explained in this section.

The digital column sensor (DCS) was designed with 96×84 pixels. Each pixel was sized to $8 \times 8\,\mu m^2$. A revised version of the stand-alone column-level modulator described above was used in the digital column. A readout

circuit and a bit-serial decimator with standard D flip-flops were integrated with each modulator.

The digital pixel sensor (DPS) had 48×64 pixels, each with $38\,\mu$m pitch. The DPS used the same design of the previous stand-alone ADC with the large OTA, as the ADC performance was high enough for the image sensors. A logarithmic sensor and a readout circuit were incorporated.

To perform FPN correction, multiple images were captured from a uniform scene at different illumination levels. The FPN was corrected using a regression method with three parameters. Dead pixels were fixed by five-point median filtering. Then, the SNR and SNDR of the corrected images were calculated.

Unlike audio signals, a video signal is a time-varying 2-D signal. Hence, audio characterization approaches cannot be used easily to characterize video signals. Performance variation across the sensor was presented using median values and cumulative distribution functions. In this way, more detail about the distribution of performance was presented.

Although the decimator in the DCS works well in simulation, experimental results show that most of the decimators do not function properly because of a timing error. Therefore, the modulator output was read out and decimation was performed in an FPGA. This limited the frame rate to 1.2 fps. The modulator suffers from mismatch and 8% of the modulators do not respond to input. The reason is because the variation of current in the OTA output branch is more than what the CMFB circuit could correct. Experimental results of the DCS at 51 fps sampling rate and 1.2 fps readout rate show that 35 dB peak SNDR is achieved while a very low power consumption is maintained. This shows 9 dB improvement over a recent work on logarithmic sensors using column-level data conversion [20].

The DPS achieved 46 dB peak SNDR at a 30 Hz frame rate. This shows almost 20 dB improvement compared to previous work on logarithmic sensors. Although the sampling rate supports 52 fps, the video rate is 30 fps because it takes 14.5 ms to read out each frame.

In both image sensors, the frame rate was varied by changing the oversampling ratio of the sensor. It was shown that by reducing the oversampling ratio, a higher frame rate with lower SNDR may be achieved. This means that SNDR may be traded against the oversampling ratio to achieve a desirable specification within limits.

For both image sensors, a high dynamic range was achieved. Also, the SNDR is high at bright light levels, which is important in machine vision applications [25]. However, at dim light levels, the SNDR is reduced because of dark current. This could be improved by a photodiode with a lower dark current. At high light levels, the SNDR is limited by ADC performance and the non-uniformity of sensor response, while at low light levels, the performance is limited by the dark current and low signal power.

Experimental results show that by using the DCS or DPS approaches,

the SNDR of logarithmic sensors are improved. This is an important step towards realizing high-dynamic-range, high-SNDR cameras. As was expected, the DPS achieved higher SNDR partly because more readout noise is filtered. On the other hand, the DCS used very small pixels and is more suitable for applications needing small pixel size such as visible-band imaging.

6.2 Future Work

The research presented in this thesis can be extended in several directions. Some of them are briefly discussed in this section. While the effectiveness of column and pixel-level delta-sigma data conversion in logarithmic image sensors was proved, other applications of the proposed methods need to be investigated. Also, different techniques can be used to further improve the performance of the image sensors, enabling digital camera to rival the human eye. Vertical integration, which is an emerging fabrication technology, can also be used to enhance the performance of array sensors.

6.2.1 Applications of Delta-Sigma ADC Arrays

It was shown that, using column and, especially, pixel-level delta-sigma data conversion, low-voltage readout circuits with very low noise can be developed. A variety of applications, such as lab-on-a-chip, infrared sensors, X-ray cameras, and terahertz imagers, require arrays of readout circuits with very low noise while a large pixel is allowed.

Lab-on-a-chip technology is widely being used for disease diagnostics. New circuits are being developed that integrate the system into one IC [96], which incorporates a single sensor to detect light intensity. Interphase fluorescence in situ hybridization (FISH) is a detection tool in which the alterations in the genome among the cells is detected using a sensor array [97]. A column or pixel-parallel delta-sigma ADC is a suitable solution to reduce the noise and increase the sensitivity of the system.

X-ray cameras are widely used for medical imaging [37]. In radiography, X-ray technology is an effective method for diagnostic imaging. It is always desired to minimize the X-ray radiation power in order to avoid cellular damage and to reduce the side effects of this method. To do so, low noise readout circuits play a key role. The proposed architectures can be effective solutions in this manner.

Terahertz technology is finding uses in a variety of applications, such as process and quality control, biomedical imaging, and security screening. New terahertz array sensors are being developed [98]. An array of low-noise readout circuits can increase the sensitivity of the system by reducing the readout noise. For example, this technology is used in security screening, where higher resolution under less radiation is always desired. Column or

pixel-level delta-sigma ADCs are suitable readout solutions to meet these requirements.

Column-level data conversion is more suitable for applications that require a small pixel size. Example applications for this approach are line-scan cameras, where there is only one pixel per column in the camera [99]. Unlike other column-level ADCs, a delta-sigma column-level ADC can filter the temporal noise robustly and improve the signal-to-noise ratio. It can also be used to efficiently trade the scan rate against the bits per pixel.

Overall, similar to image sensors, depending on the requirements of the application in terms of readout noise and pixel size, column or pixel-level delta-sigma ADCs can be an effective solution to improve the performance of the system.

6.2.2 Digital Camera to Rival the Human Eye

The developed imaging system achieved a high dynamic range with high SNDR at high illuminations. However, some parameters of the sensor must still be enhanced in order to compete with the performance of the humane eye. These factors include the pixel size, dark current, and SNDR at low light levels. Also, in some applications, higher frame rates are required and it is usually desirable to reduce the power consumption. In this section, new ideas to improve these factors are discussed.

In order to reduce the pixel size, the decimator must be sized carefully based on the SNDR requirement of the image sensor. The decimator was designed for .064 mV output-referred noise while the ADC needs to have only .43 mV output-referred noise in order to provide 40 dB SNDR for the image sensor. This means that the decimator could be designed with fewer bits and smaller area. Power consumption will also be reduced by decreasing the register size in the decimator.

Another method of reducing the pixel size is to put the capacitors over the digital circuit. As shown in Fig. 6.1, the capacitors take almost ten percent of the pixel area. To satisfy a well-known design rule, no transistors have been put under the capacitors. But this design rule exists to decrease variability in the capacitances, as well as coupled noise. Since the first-order delta-sigma ADC is not sensitive to capacitor mismatch and also filters the noise effectively, the rule may be broken. Part of the decimator may be put underneath the capacitors, which belongs to the modulator, thereby saving almost 10% of the area.

Smaller pixel-level (and column-level) ADCs are also possible by using one ADC for several pixels (or columns). In this case, an analog multiplexer, which is small, is used to switch the analog outputs from each pixel (or column) to the shared ADC. For instance, an ADC can be shared between four pixels, shrinking the pixel size by up to 25% at the cost of adding more readout noise. The added noise may be negligible.

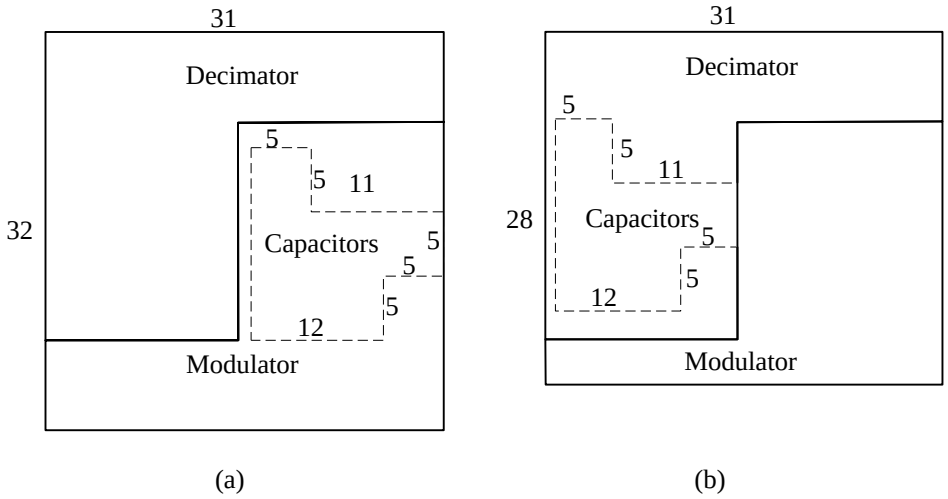


Figure 6.1: (a) Layout diagram of original pixel-level delta-sigma ADC. (b) Layout diagram of modified pixel-level delta-sigma ADC, where the area of the ADC is reduced by placing the capacitors over the decimator.

In addition to the mentioned methods, vertical integration is another effective solution, which can be used to shrink the pixel size. This method also has other advantages, which are discussed in the next section.

The dark limit may be improved by modifying the current source in each pixel by using a higher fill factor. Increasing the current source will reduce the amount of noise added by the source follower. Also, better photodetectors need to be investigated to reduce the dark current and improve the SNDR at low light levels.

The imaging system was designed for a 50 Hz frame rate. An important advantage of pixel-level data conversion is the fast readout, which allows very high frame rates and window size. Also, unlike linear sensors, logarithmic sensors can capture very high frame rates, which is required for some applications. The possibility of achieving higher frame rates should be investigated.

Overall, while several techniques could be used to enhance the performance, the system should be customized based on the requirements of the application. For example, some applications allow for large pixel size but require a high bit resolution. On the other hand, some other applications, such as visible-band imaging, require high spatial resolution, which may be traded with peak SNDR, i.e., multiple pixels or columns may share one ADC. Also, other modulator architectures might be used in some applications. If a lower SNDR is acceptable, single-ended circuits, which require half the area, might be employed. In contrast to switched-capacitor circuits, current-mode modulators need only one capacitor and a simpler circuit at the cost of having less tolerance to noise.

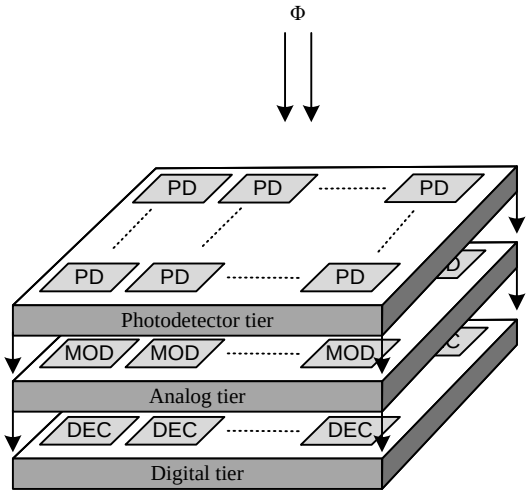


Figure 6.2: Delta-sigma digital pixel sensor using vertical integration, where it is fabricated by stacking multiple tiers. Photodiodes (PDs) are implemented in the top tier, modulators (MODs) are implemented in the middle tier, and decimators (DECs) are implemented in the bottom tier.

6.2.3 Vertically-Integrated CMOS Technology

Undoubtedly, vertical integration will play an important role in the development of high-performance VLSI circuits. 3D integrated circuits (ICs) are emerging suites of technologies, where semiconductor devices (transistors, diodes, etc) can be built in vertically-integrated (VI) tiers [91]. The main advantages of using this technology for image sensors are higher spatial resolution, higher fill factor, lower power consumption, heterogeneous processes, more functionality, and more compact systems.

Fig. 6.2 shows a block diagram of a VI-CMOS image sensor employing pixel-level delta-sigma ADCs, where different parts of the circuit are stacked vertically. The pixel area is thereby reduced. The top tier consists of the photodetectors. The middle tier contains analog signal processing, in particular the delta-sigma modulators. The bottom tier consists of digital signal processing, in particular the delta-sigma decimators.

An image sensor needs photodetectors, analog circuits, and digital circuits. Using vertical integration, each part can be fabricated in a process optimized for the type of elements it contains. Photodetectors may be fabricated in a long channel process, which has better optical performance. Analog circuits may be fabricated in an intermediate process with less imperfection and mismatch, and digital circuits may be fabricated in a nanoscale process with minimum size and high speed. By separating the analog and digital tiers, analog circuits are isolated from digital noise and a higher SNR is achieved.

In addition, the same readout circuits could be used for different sensor

arrays with vertical integration. For instance, the photodetector tier may be the only one that is changed to realize infrared or X-ray image sensors. In this manner, design and fabrication costs may be reduced.

Also, with vertical integration, higher speed and higher frame rates are possible. In 2D ICs, wire delays are an inherent problem that limits the circuit speeds. Instead of long traces on a PCB with 2D ICs, very small bond pads with low capacitance are used in 3D ICs. Therefore, higher bit rates with larger array sizes may be easily achieved. This can help to reduce digital power consumption, which is a key parameter in today's mixed-signal VLSI designs.

Bibliography

[1] J.M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey," *IEEE Transactions on Circuits and Systems*, vol. 58, no. 1, pp. 1–21, 2011.

[2] L. Yao, M. Steyaert, and W. Sansen, Eds., *Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS*, Springer, 2006.

[3] S.R. Norsworthy, R. Schreier, and G.C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, 1996.

[4] J.C. Candy and G.C. Temes, "Oversampling Methods for Data Conversion," in *IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, May 1991, vol. 2, pp. 498–502.

[5] B.E. Boser and B.A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, 1988.

[6] F. Medeiro, B. Perez-Verdu, and A. Rodriguez-Vazquez, "A 13-bit, 2.2-MS/s, 55-mW Multibit Cascade Sigma-Delta Modulator in CMOS 0.7um Single-Poly Technology," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 748–760, 1999.

[7] L.G. McIlrath, "A Low-Power, Low-Noise, Ultrawide-Dynamic-Range CMOS Imager with Pixel-Parallel A/D Conversion," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 846 – 853, May 2001.

[8] B. Fowler, A. El Gamal, and D.X.D. Yang, "A CMOS Area Image Sensor with Pixel-Level A/D Conversion," in *IEEE International Solid-State Circuits Conference*, 16-18 Feb. 1994, pp. 226–227.

[9] A. Fernandes, J.G. Rocha, and G. Minas, "Smart-Pixel Array for Imaging Sensors," in *Proceedings of the 14th IEEE International Conference*

on Electronics, Circuits and Systems, 2007, pp. 395–398.

[10] C. Baumer, S. Eick, R. Steadman, G. Vogtmeier, M. Gnade, A. Kemna, and D. Weiler, "Design and Evaluation of a CMOS-Photosensor with In-Pixel Sigma-Delta Modulator for X-ray Computed Tomography," in *Proceedings of the 32nd European Solid-State Circuits Conference*, 2006, pp. 432–435.

[11] M. Crescentini, M. Rossi, M. Bennati, F. Thei, A. Baschirotto, and M. Tartagni, "A Nanosensor Interface Based on Delta-Sigma Arrays," in *Proceedings of the 3rd International Workshop on Advances in Sensors and Interfaces*, 2009, pp. 163–167.

[12] A. Agah, K. Vleugels, P.B. Griffin, M. Ronaghi, J.D. Plummer, and B.A. Wooley, "A High-Resolution Low-Power Incremental Delta-Sigma ADC With Extended Range for Biosensor Arrays," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1099–1110, 2010.

[13] L. Harik, J.M. Sallese, and M. Kayal, "SOI Pixel Based on a Floating Body Partially Depleted MOSFET in a Delta-Sigma Loop," *IEEE Sensors Journal*, vol. 9, no. 8, pp. 994–1001, 2009.

[14] F. Heer, M. Keller, G. Yu, J. Janata, M. Josowicz, and A. Hierlemann, "CMOS Electro-Chemical DNA-Detection Array with On-Chip ADC," in *Proceedings of IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2008, pp. 168–604.

[15] A. El Gamal and H. Eltoukhy, "CMOS Image Sensors," *IEEE Circuits and Devices Magazine*, vol. 21, no. 3, pp. 6–20, May-June 2005.

[16] A. Spivak, A. Belenky, A. Fish, and O. Yadid-Pecht, "Wide-Dynamic-Range CMOS Image Sensors—Comparative Performance Analysis," *IEEE Transactions on Electron Devices*, vol. 56, no. 11, pp. 2446–2461, 2009.

[17] J.H. Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito, "A High-Speed Low-Noise CMOS Image Sensor With 13-b Column-Parallel Single-Ended Cyclic ADCs," *IEEE Transactions on Electron Devices*, vol. 56, no. 11, pp. 2414–2422, 2009.

[18] D. Joseph and S. Collins, "Modeling, Calibration, and Correction of

Nonlinear Illumination-Dependent Fixed Pattern Noise in Logarithmic CMOS Image Sensors," *IEEE Transactions on Instrumentation and Measurement*, vol. 51, no. 5, pp. 996–1001, Oct. 2002.

[19] D. Joseph, *Modelling and calibration of logarithmic CMOS image sensors*, Ph.D. thesis, University of Oxford, Oxford, U.K., 2002.

[20] G. Storm, R. Henderson, J.E.D. Hurwitz, D. Renshaw, K. Findlater, and M. Purcell, "Extended Dynamic Range From a Combined Linear-Logarithmic CMOS Image Sensor," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2095–2106, 2006.

[21] S. Kavusi, H. Kakavand, and A. El Gamal, "Quantitative Study of High Dynamic Range Sigma-Delta-based Focal Plane Array Architectures," in *Proceedings of the SPIE*, Aug. 2004, vol. 5406, pp. 341–350.

[22] S. Kavusi and A. El Gamal, "Quantitative Study of High Dynamic Range Image Sensor Architectures," in *Proceedings of the SPIE*, Jun. 2004, vol. 5301, pp. 264–275.

[23] W. Bidermann, A. El Gamal, S. Ewedemi, J. Reyneri, H. Tian, D. Wile, and D. Yang, "A 0.18um High Dynamic Range NTSC/PAL Imaging System-on-Chip with Embedded DRAM Frame Buffer," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, 2003, vol. 1, pp. 212–488.

[24] A. Bermak and A. Kitchen, "A Novel Adaptive Logarithmic Digital Pixel Sensor," *IEEE Photonics Technology Letters*, vol. 18, no. 20, pp. 2147–2149, 2006.

[25] P.F. Ruedi, P. Heim, S. Gyger, F. Kaess, C. Arm, R. Caseiro, J.L. Nagel, and S. Todeschini, "An SoC Combining a 132dB QVGA Pixel Array and a 32b DSP/MCU Processor for Vision Applications," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2009, pp. 46–47,47a.

[26] Y. Geerts, A.M. Marques, M.S.J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, Delta-Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Applications," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 927–936, 1999.

[27] J. Fortier, N.G. Tarr, A. Swaminathan, and C. Plett, "1.2 V 0.18um CMOS Imager with Column-Level Oversampling," in *Proceedings of the 27th European Solid-State Circuits Conference*, Sept. 2001, pp. 105–108.

[28] Y. Chae, J. Cheon, S. Lim, D. Lee, M. Kwon, K. Yoo, W. Jung, L. Dong-Hun, S. Ham, and G. Han, "A 2.1Mpixel 120frame/s CMOS Image Sensor with Column-Parallel delta-sigma ADC Architecture," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2010, pp. 394 – 395.

[29] Y. Chae, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.H. Lee, S. Ham, and G. Han, "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel Delta-Sigma ADC Architecture," *IEEE Journal of Solid-State Circuits*, , no. 99, pp. 1–12, 2010, Early Access.

[30] M.F. Snoeij, A.J.P. Theuwissen, K.A.A. Makinwa, and J.H. Huijsing, "Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2968–2977, 2007.

[31] A. Olyaei and R. Genov, "Focal-Plane Spatially Oversampling CMOS Image Compression Sensor," *IEEE Transactions on Circuits and Systems*, vol. 54, no. 1, pp. 26–34, 2007.

[32] L. Lindgren, "A New Simultaneous Multislope ADC Architecture for Array Implementations," *IEEE Transactions on Circuits and Systems*, vol. 53, no. 9, pp. 921–925, 2006.

[33] A. El Gamal, D.X.D. Yang, and B. Fowler, "Pixel Level Processing - Why?, What?, and How?," in *Proceedings of SPIE*, Jan. 1999, vol. 3650, pp. 2–13.

[34] B. Fowler, A. El Gamal, and D.X.D. Yang, "Techniques for Pixel Level Analog to Digital Conversion," in *Proceedings of SPIE*, 1998, vol. 3360, pp. 1–12.

[35] J. Dubois, D. Ginhac, M. Paindavoine, and B. Heyrman, "A 10 000 fps CMOS Sensor With Massively Parallel Image Processing," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 706–717, 2008.

[36] Y. Joo, J. Park, M. Thomas, K.S. Chung, M.A. Brooke, N.M. Jokerst, and D.S. Wills, "Smart CMOS Focal Plane Arrays: A Si CMOS Detector Array and Sigma-Delta Analog-to-Digital Converter Imaging System," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 5, no. 2, pp. 296–305, 1999.

[37] J.G. Rocha, N.F. Ramos, R.F. Wolffenbuttel, and J.H. Correia, "CMOS X-ray Image Sensor with Pixel Level A/D Conversion," in *Proceedings of the 29th European Solid-State Circuits Conference*, 2003, pp. 121–124.

[38] J.P. Crooks, S.E. Bohndiek, C.D. Arvanitis, R. Speller, H. XingLiang, E.G. Villani, M. Towrie, and R. Turchetta, "A CMOS Image Sensor With In-Pixel ADC, Timestamp, and Sparse Readout," *IEEE Sensors Journal*, vol. 9, no. 1, pp. 20–28, 2009.

[39] D.X.D. Yang, A.E. Gamal, B. Fowler, and H. Tian, "A 640*512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1821–1834, 1999.

[40] Q. Luo, G.H. John, and Z.J. Chen, "A time-to-first spike CMOS image sensor with coarse temporal sampling," *Analog Integrated Circuits and Signal Processing*, vol. 47, no. 3, pp. 303–313, 2006.

[41] B. Choubey, S. Aoyoma, S. Otim, D. Joseph, and S. Collins, "An Electronic-Calibration Scheme for Logarithmic CMOS Pixels," *IEEE Sensors Journal*, vol. 6, no. 4, pp. 950–956, 2006.

[42] S. Kavadias, B. Dierickx, D. Scheffer, A. Alaerts, D. Uwaerts, and J. Bogaerts, "A Logarithmic Response CMOS Image Sensor with On-Chip Calibration," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1146–1152, 2000.

[43] S. Otim, B. Choubey, D. Joseph, and S. Collins, "Characterization and Simple Fixed Pattern Noise Correction in Wide Dynamic Range Logarithmic Imagers," *IEEE Transactions on Instrumentation and Measurement*, vol. 56, pp. 1910 – 1916, Oct. 2007.

[44] K. Hara, H. Kubo, M. Kimura, F. Murao, and S. Komori, "A Linear-Logarithmic CMOS Sensor with Offset Calibration Using an Injected Charge Signal," in *IEEE International Solid-State Circuits Conference -*

Digest of Technical Papers, 2005, pp. 354–603.

[45] S. Decker, D. McGrath, K. Brehmer, and C.G. Sodini, "A 256*256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2081–2091, 1998.

[46] D. Park, J. Rhee, and J. Youngjoong, "A Wide Dynamic-Range CMOS Image Sensor Using Self-Reset Technique," *IEEE Electron Device Letters*, vol. 28, no. 10, pp. 890–892, 2007.

[47] M. Vogels and G. Gielen, "Architectural selection of A/D converters," in *Processdings of the Design Automation Conference*, 2003, pp. 974–977.

[48] Z. Zhou, B. Pain, and E.R. Fossum, "CMOS Active Pixel Sensor with On-Chip Successive Approximation Analog-to-Digital Converter," *IEEE Transactions on Electron Devices*, vol. 44, no. 10, pp. 1759–1763, 1997.

[49] S. Lim, J. Lee, D. Kim, and G. Han, "A High-Speed CMOS Image Sensor With Column-Parallel Two-Step Single-Slope ADCs," *IEEE Transactions on Electron Devices*, vol. 56, no. 3, pp. 393–398, 2009.

[50] M.R. Snoeij, P. Donegan, A.J.P. Theuwissen, K.A.A. Makinwa, and J.H. Huijsing, "A CMOS Image Sensor with a Column-Level Multiple-Ramp Single-Slope ADC," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2007, pp. 506–618.

[51] S.K. Mendis, B. Pain, R.H. Nixon, and E.R. Fossum, "Low-light-level image sensor with on-chip signal processing," in *Proceedings of the SPIE*, 1993, vol. 1952, pp. 23–33.

[52] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E.R. Fossum, "On-Focal-Plane Signal Processing for Current-Mode Active Pixel Sensors," *IEEE Transactions on Electron Devices*, vol. 44, no. 10, pp. 1747–1758, 1997.

[53] T. Morris, E. Fletcher, C. Afghahi, S. Issa, K. Connolly, and J.C. Korta, "A column-based processing array for high-speed digital image processing," in *Proceedings of the 20th Anniversary Conference on Advanced Research in VLSI*, Mar. 1999, pp. 42–56.

[54] K. Yap and R.J. Baker, "Gain Error Correction for CMOS Image Sensor Using Delta-Sigma Modulation," in *Proceedings of the IEEE Workshop Microelectronics and Electron Devices*, 2010, pp. 1–4.

[55] Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, 2009.

[56] D.X.D. Yang, B. Fowler, and A. El Gamal, "A 128*128 Pixel CMOS Area Image Sensor with Multiplexed Pixel Level A/D Conversion," in *IEEE Custom Integrated Circuits Conference*, 5-8 May 1996, pp. 303–306.

[57] D. Maricic, Z. Ignjatovic, and M.F. Bocko, "An Oversampling Digital Pixel Sensor with a Charge Transfer DAC Employing Parasitic Capacitances," in *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, 2009, pp. 415–418.

[58] Z. Ignjatovic and M.F. Bocko, "A 0.88nW/pixel, 99.6 dB Linear-Dynamic-Range Fully-Digital Image Sensor Employing a Pixel-Level Sigma-Delta ADC," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, 2006, pp. 23–24.

[59] J.G. Rocha, G. Minas, and S. Lanceros-Mendez, "Pixel Readout Circuit for X-Ray Imagers," *IEEE Sensors Journal*, vol. 10, no. 11, pp. 1740–1745, 2010.

[60] M. Safi-Harb and G.W. Roberts, "Low Power DeltaSigma Modulator for ADSL Applications in a Low-Voltage CMOS Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 10, pp. 2075–2089, Oct. 2005.

[61] J. Roh, S. Byun, Y. Choi, H. Roh, Y. Kim, and J. Kwon, "A 0.9-V 60-uW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 361 – 370, Feb. 2008.

[62] A.V. Oppenheim, R.W. Schafer, and J.R. Buck, *Discrete-Time Signal Processing*, Prentice-Hall, Inc., 1999.

[63] R.W. Stewart and E. Pfann, "Oversampling and sigma-delta strategies for data conversion," *Electronics and Communication Engineering Jour-*

nal, vol. 10, no. 1, pp. 37–47, 1998.

[64] P.M. Aziz, H.V. Sorensen, and J. van der Spiegel, "An Overview of Sigma-Delta Converters," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 61–84, 1996.

[65] S. Chu and C. Burrus, "Multirate Filter Designs Using Comb Filters," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 11, pp. 913–924, 1984.

[66] E. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 29, no. 2, pp. 155–162, 1981.

[67] S.S. Abeysekera, Y. Xue, and C. Charoensak, "Design of Optimal and Narrow-Band Laguerre Filters for Sigma-Delta Demodulators," *IEEE Transactions on Crcuits and Systems*, vol. 50, no. 7, pp. 368–375, 2003.

[68] J. Candy, Y. Ching, and D. Alexander, "Using Triangularly Weighted Interpolation to Get 13-Bit PCM from a Sigma-Delta Modulator," *IEEE Transactions on Communications*, vol. 24, no. 11, pp. 1268–1275, Nov. 1976.

[69] H. Aboushady, Y. Dumonteix, M.M. Louerat, and H. Mehrez, "Efficient Polyphase Decomposition of Comb Decimation Filters in Sigma-Delta; Analog-to-Digital Converters," in *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, 8-11 Aug. 2000, vol. 1, pp. 432–435.

[70] Y. Gao, L. Jia, and H. Tenhunen, "A fifth-order comb decimation filter for multi-standard transceiver applications," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2000, vol. 3, pp. 89–92.

[71] D.D. Kim and M.A. Brooke, "Scalable Delta-Sigma Modulator Readout Architecture for Array-based Sensor System," in *Proceedings of IEEE International Symposium on Circuits and Systems*, 2006.

[72] M. Laddomada, "Comb-Based Decimation Filters for Sigma-Delta A/D Converters: Novel Schemes and Comparisons," *IEEE Transactions on Signal Processing*, vol. 55, no. 5, pp. 1769–1779, 2007.

[73] H. Aboushady, Y. Dumonteix, M.M. Louerat, and H. Mehrez, "Efficient

Polyphase Decomposition of Comb Decimation Filters in Sigma-Delta Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems*, vol. 48, no. 10, pp. 898–903, 2001.

[74] L. Lo Presti, "Efficient Modified-Sinc Filters for Sigma-Delta A/D Converters," *IEEE Transactions on Circuits and Systems*, vol. 47, no. 11, pp. 1204–1213, 2000.

[75] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Reading, MA: Addison-Wesley, 3rd edition, 2005.

[76] J.J. Kubinec, "Two phase CMOS shift register bit for optimum power dissipation," *United states Patent*, 1991.

[77] H. Zare-Hoseini, I. Kale, and O. Shoaei, "Modeling of Switched-Capacitor Delta-Sigma Modulators in SIMULINK," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 4, pp. 1646–1654, Aug. 2005.

[78] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators," *IEEE Transactions on Circuits and Systems*, vol. 50, no. 3, pp. 352–364, 2003.

[79] P. Arpaia, F. Cennamo, P. Daponte, and H. Schumny, "Modeling and Characterization of Sigma-Delta Analog-to-Digital Converters," *IEEE Transactions on Instrumentation and Measurement*, vol. 52, no. 3, pp. 978–983, 2003.

[80] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, and F. Maloberti, "Modeling sigma-delta modulator non-idealities in SIMULINK(R)," in *Proceedings of IEEE International Symposium on Circuits and Systems*, 1999, vol. 2, pp. 384–387.

[81] Bernd. Hoefflinger, Ed., *High-Dynamic-Range (HDR) Vision*, Springer, 2007.

[82] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Inc., 2000.

[83] L. Luh, J. Choma, and J. Draper, "A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current Mode Appli-

cation," in *IEEE International Conference on Electronics, Circuits and Systems*, Sept. 1998, vol. 3, pp. 347–350.

[84] S. Mallya and J.H. Nevin, "Design Procedures for a Fully Differential Folded-Cascode CMOS Operational Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 6, pp. 1737–1740, 1989.

[85] A. Yukawa, "A CMOS 8-Bit High-Speed A/D Converter IC," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 3, pp. 775–779, 1985.

[86] J. Ruiz-Amaya, J.M. de la Rosa, F.V. Fernandez, F. Medeiro, R. del Rio, B. Perez-Verdu, and A. Rodriguez-Vazquez, "High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time Sigma-Delta Modulators Using SIMULINK-Based Time-Domain Behavioral Models," *IEEE Transactions on Circuits and Systems*, vol. 52, no. 9, pp. 1795–1810, 2005.

[87] K.R. Lakshmikumar, R.A. Hadaway, and M.A. Copeland, "Characterisation and Modeling of Mismatch in MOS Transistors for Precision Analog Design," *IEEE Journal of Solid-State Circuits*, vol. 21, pp. 1057 – 1066, Dec. 1986.

[88] K. Lee, M.R. Miller, and G.C. Temes, "An 8.1 mW, 82 dB Delta-Sigma ADC With 1.9 MHz BW and -98 dB THD," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2202–2211, 2009.

[89] M.G. Kim, G.C. Ahn, P.K. Hanumolu, S.H. Lee, S.H. Kim, S.B. You, J.W. Kim, G.C. Temes, and U.K. Moon, "A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1195–1206, 2008.

[90] C. Kuo, D. Shi, and K. Chang, "A Low-Voltage Fourth-Order Cascade Delta–Sigma Modulator in 0.18um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 9, pp. 2450–2461, 2010.

[91] O. Skorka and D. Joseph, "Design and Fabrication of a VI-CMOS Image Sensor," CMC Application Note, University of Alberta, Aug. 2010.

[92] D. Joseph, "VLSI Source Coding for Efficient Analogue-to-Digital Conversion," *Transfer-of-Status Report, University of Oxford, Oxford, UK*, 1998.

[93] A. Mahmoodi and D. Joseph, "Optimization of Delta-Sigma ADC for Column-Level Data Conversion in CMOS Image Sensors," in *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*, 1-3 May 2007, pp. 1–6.

[94] A. Mahmoodi and D. Joseph, "Pixel-Level Delta-Sigma ADC with Optimized Area and Power for Vertically-Integrated Image Sensors," in *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, Aug. 2008, pp. 41–44.

[95] D. Joseph and A. Mahmoodi, "Pixel Sensor Converters and Associated Apparatus and Methods," *United States Patent Application Publication*, , no. US 2011/0035427 A1, pp. 1–22, Feb. 2011.

[96] M. Behnam, G.V. Kaigala, M. Khorasani, S. Martel, D.G. Elliott, and C.J. Backhouse, "Integrated circuit-based instrumentation for microchip capillary electrophoresis," *IET Nanobiotechnology*, vol. 4, no. 3, pp. 91–101, 2010.

[97] V.J. Sieben, C.S.D. Marun, P.M. Pilarski, G.V. Kaigala, L.M. Pilarski, and C.J. Backhouse, "FISH and chips: Chromosomal analysis on microfluidic platforms," *IET Nanobiotechnology*, vol. 1, no. 3, pp. 27–35, 2007.

[98] C. Fumeauxa, W. Herrmanna, F.K. Kneubhla, and H. Rothuizenb, "Nanometer thin-film Ni-NiO-Ni diodes for detection and mixing of 30 THz radiation," *Infrared Physics and Technology*, vol. 39, pp. 123–183, 1998.

[99] C.A. Luna, M. Mazo, J.L. Lazaro, and J.F. Vazquez, "Calibration of Line-Scan Cameras," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 8, pp. 2185–2190, 2010.