Design and Implementation of 60 GHz CMOS Power Amplifiers

by

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Abstract

The availability of an unlicensed 7 GHz bandwidth around 60 GHz offers great potential for establishment of high-data-rate short-range wireless communication links. Although previously left unutilized, recent advances in electronics enable the development of wireless transceivers at millimeter-wave frequencies. Despite offering a large bandwidth, the high signal attenuation caused by oxygen absorption in 60 GHz band requires the wireless transmitters to transmit signals with power as large as 27 dBm, so the receivers can detect greatly attenuated signals. Therefore, the design of power amplifiers capable of generating such large output powers proves to be a major challenge in the development of 60 GHz wireless transceivers, especially if CMOS technology is chosen for implementation of fully integrated 60 GHz wireless systems.

In this dissertation, we present new architectures for power combining transformers, as well as new circuit topologies to improve the performance of 60 GHz power amplifiers implemented in CMOS technology. Although CMOS offers a higher level of integration and lower fabrication cost compared to high-speed compound semiconductor technologies, low supply and breakdown voltages, as well as operation near cutoff frequencies of MOSFETs make the design of power amplifier extremely challenging. Optimization of the efficiency/power performance of CMOS power amplifiers operating at millimeter-wave frequencies requires novelty in the design of active/passive structures. An overview on the technological advances and the challenges

in millimeter-wave CMOS power amplifiers is presented by comparing previously reported active/passive power combination techniques. A comprehensive analysis and modeling of the matching circuits and on-chip spiral transformers are developed in order to estimate the passive power efficiency of the coupling circuits and power combining transformers. A new area-efficient power-combining configuration is proposed to achieve a high output power per occupied area. A 60 GHz power amplifier is fabricated utilizing the new combining technique with a measured output power of 18.8 dBm.

Second we propose a new circuit topology to enable the capability of dual-mode operation. Also, a new enhancement technique is utilized in order to improve the gain-bandwidth product of cascode gain stages. Fabricated in 65 nm technology, the 60 GHz power amplifier could achieve measured maximum power added efficiency of 17.2% while delivering 18.1 dBm output power.

Finally, we explore the utilization of a new dual-mode technique in a distributed active transformer power amplifier. A new power amplifier circuit topology and a new DAT layout technique is proposed in order to improve the power added efficiency and output power simultaneously. Fabricated in 65nm CMOS technology, the maximum measured gain of the 60 GHz power amplifier is 22 dB within a wide 3dB bandwidth of 14 GHz. A maximum saturated output power of 19.7 dBm is measured in high-power mode while a high power added efficiency of 25% is achieved.

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Contents

List of Figures

List of Tables

List of Abbreviations

ADS	Advanced design system
AM-AM	Amplitude-to-amplitude distortion
AM-PM	Amplitude-to-phase distortion
b	Balanced amplifier topology
BIST	Built in self test
BWRC	Berkeley wireless research center
BW	Bandwidth
Cas	Cascode amplifier topology
CBM	MIM capacitor's bottom metal layer
CE	Common emitter amplifier
CG	Common gate amplifier
CMOS	Complementary metal oxide semiconductor
CS	Common source amplifier
CTM	MIM capacitor's top metal layer
d	Differential amplifier topology
DAC	Digital to analog converters
DAT	Distributed active transformer
dB	Decibels
dBi	Decibels-isotropic
dBm	Decibels-milliwatts
DUT	Device under test
EIRP	Equivalent isotropic radiated power
EM	Electromagnetic
EVM	Error vector magnitude
FCC	Federal communication commission
FDSOI	Fully depleted silicon on insulator

FEM	Front-end-module
f_{max}	Transistor's maximum frequency of operation
FoM	Figure-of-merit
f_T	Transistor's transit (cut-off) frequency
GaAs	Galium arsenide
Gbps	Giga bit per second
GBW	Gain bandwidth product
GMSK	Gaussian minimum-shift keying
g_m	Transistor's transconductance
G_P	Power gain
GSG	Ground-signal-ground
HB	Harmonic balance
HBT	Heterojuction bipolar transistors
HD	High definition
HEMT	High electron mobility transistors
HP	High power mode
IF	Intermediate frequency
IIP3	Third order intercept point
IL	Insertion loss
I/O	Input/output
Im	Imaginary
IMD	Inter-modulation distortion
IMD3	Third order inter-modulation distortion
Inp	Indium-phosphide
ITR	Impedance transformation ratio
ITRS	International technology roadmap for semiconductors
K	Stability factor
k	Transformer's coupling factor
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LNA	Low noise amplifier
LTI	Linear time invariant
LP	Low power
M	Transformer's mutual inductance

MAG	Maximum available gain
MIM	Metal-insulator-metal
mmW	Millimeter-wave
MMIC	Monolithic microwave integrated circuit
MOM	Metal-oxide-metal
MOS	Metal-oxide-semiconductor
MOSFET	Metaloxidesemiconductor field effect transistor
MSG	Maximum stable gain
MUG	Mason's unilateral gain
n	Transformation ratio
N_f	Transistor's number of fingers
NMOS	n-Channel MOSFET
PAs	Power amplifiers
PAE	Power added efficiency
PDK	Process design kit
PLL	Phase locked loop
PM-PM	Phase-to-phase distortion
PNA	Performance network analyzer
P_{sat}	Saturated output power
PSK	Phase shift keying
PUF	Power utilization factor
P_{1dB}	1 dB compression point
Q	Quality factor
Re	Real
RF	Radio frequency
RFIC	Radio frequency integrated circuits
s	Single-ended amplifier topology
Si	Silicon
SiGe	Silicon germanium
SiO_2	Silicon dioxide
SNR	Signal to noise ratio
SoC	System-on-chip
SOLT	Short-open-load-thru
SOI	Silicon-on-insulator

S-Parameter	Scattering parameter
SRF	Self resonant frequency
S_{11}	Input reflection coefficient
S_{12}	Reverse isolation coefficient
S_{22}	Output reflection coefficient
S_{21}	Forward gain coefficient
TF	Transformer
TIT	Tokyo Institute of Technology
TL	Transmission line
UCB	University of California at Berkeley
UTM	Ultra-thick metal
VCCS	Voltage controlled current sources
V_{DD}	Supply voltage
VCO	Voltage controlled oscillator
VNA	Vector network analyzer
V_T	Transistor's threshold voltage
WiGig	Wireless gigabit alliance
$WirelessHD^{TM}$	High-definition video streaming standard
WLAN	Wireless local area network
WPAN	Wireless personal area networks
W_f	Transistor's width of a single finger
ZDVS	Zero derivative voltage switching
ZVS	Zero voltage switching
μ factor	Stability parameter
1P9M	1 poly 9 metal technology

Chapter 1

Introduction

The wide 7 GHz unlicensed band from 57 GHz to 64 GHz, known as "60 GHz band", makes it an ideal candidate for the development of short-range high-data-rate wireless communication links enabling applications such as wireless High-Definition (HD) video streaming, high speed file transfer and synchronization of cellular phones, wireless gigabit Ethernet, and high quality wireless gaming. However, strong oxygen absorption along with limited performance of semiconductor devices at these millimeter-Wave (mmW) frequencies makes the design of wireless transceivers, especially Power Amplifiers (PAs) , extremely challenging.

In this chapter, we begin with the introduction of 60 GHz wireless communication and its advantages and limitations. Choosing the architecture and implementation of PAs is the focus of this research. We describe the design challenges considering the higher path loss and the lower performance of semiconductor devices at 60 GHz compared to low GHz PA design. As single-transistor PAs fail to provide the required output power at 60 GHz, the design of power-efficient passive power combiners is considered to be a determining factor in the overall performance of Complementary Metal Oxide Semiconductor (CMOS) PAs . A comprehensive literature review on the implemented 60 GHz PAs will be presented. A comparison of the proposed modern topologies is presented and the technical challenges are described.

1.1 60 GHz Short Range Communication

The last decade has witnessed phenomenal growth of the wireless industry such that wireless connectivity is now considered to be an indispensable service in our modern

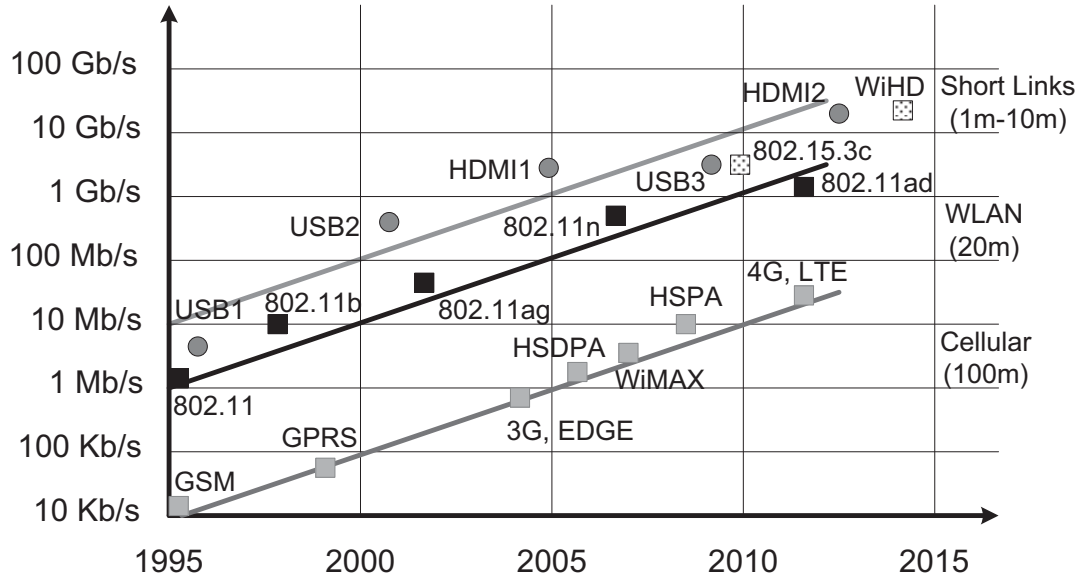


Figure 1.1: Growth of high data rate communications over the last two decades.

lives today. As shown in Fig. 1.1, the ever-increasing demand for higher data rate communication both for long-range (e.g. cellular) and short-range (e.g. Wireless Local Area Networks (WLAN) , Bluetooth, etc) applications motivate researchers and designers to develop new wireless standards capable of fulfilling these consumer demands [1]. Driven by the need for higher data-rates, standards have evolved towards packing more bit per second by using higher order modulation schemes. The 7 GHz band around 60 GHz is a promising contender because it is free to use and well suited to high-data rates for indoor Wireless Personal Area Networks (WPAN) applications. Newer standards such as IEEE 802.15.3c and WiGig are also being developed that seek to utilize this mmW band to create very high-data rate short-range WPAN [2].

The Federal Communication Commission (FCC) set aside this band in 2001 [3]. The nearest licensed mmW short-range bands are the 24 GHz and 77 GHz bands, dedicated to automotive radar applications (Fig. 1.2). Consequently, there are no interference issues between these mmW applications. Moreover, they operate in different environments: the indoor environment for WPAN communications, and the outdoor environment for automotive radar applications. In addition to the high-data rates that can be achieved in this spectrum, energy propagation in the 60 GHz band has unique characteristics which necessitates discussion.

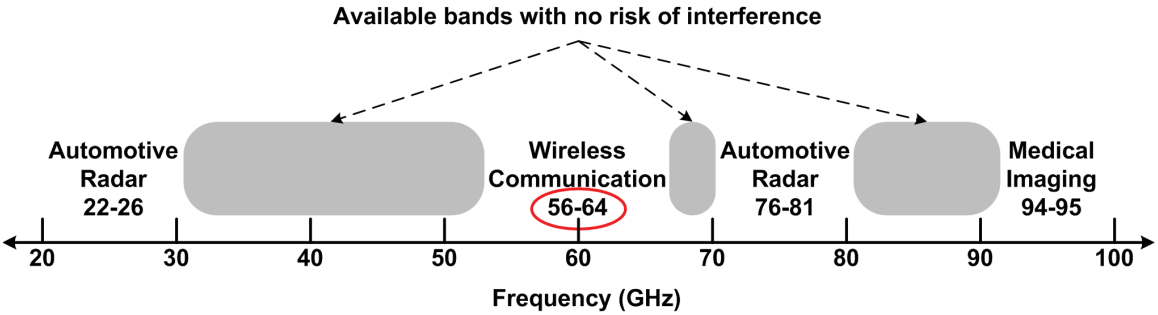


Figure 1.2: 60 GHz unlicensed band and the millimeter wave neighbors.

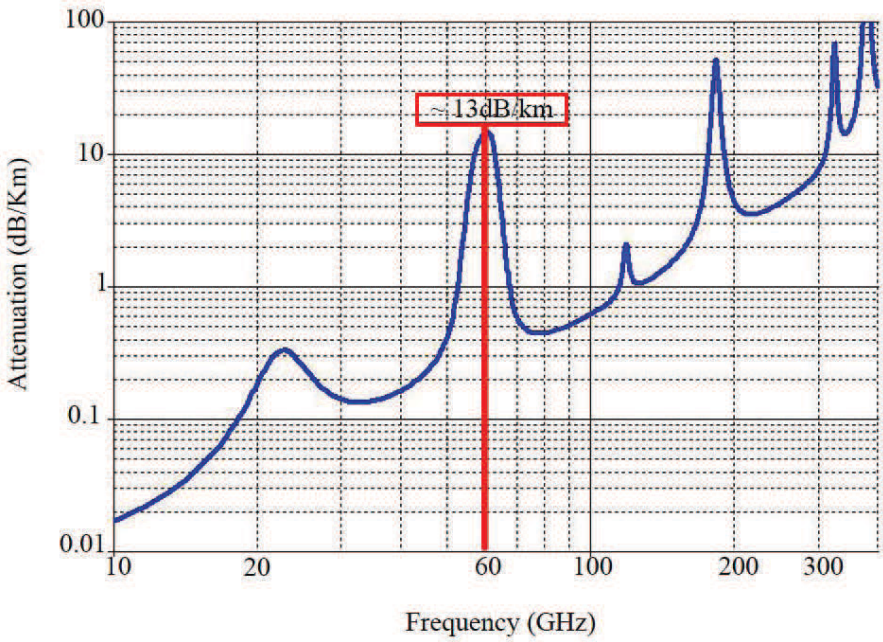


Figure 1.3: Oxygen absorption at 60 GHz.

1.1.1 60 GHz band overview

One particular drawback of the 60 GHz band is that the oxygen molecules absorb electromagnetic energy at these specific frequencies at higher rate, compared to low GHz frequencies. The strong oxygen energy absorption causes a total of 13 dB/km attenuation (Fig. 1.3) [4] [5]. The signal attenuation requires a 60 GHz transmitter to transmit higher output powers than their lower GHz counterparts in order for the receiver to successfully detect the transmitted signal. To determine the power specifications at 60 GHz, a link budget analysis must be performed based on the application requirements, such as distance and data rate.

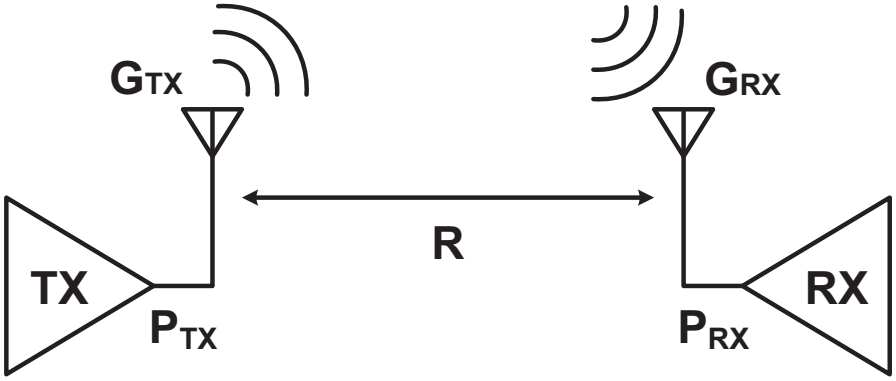


Figure 1.4: Wireless link with TX/RX distance of R.

Fig. 1.4 shows a wireless link with a transmit-to-receive antenna distance of R. The transmitter delivers an output power of P_{TX}, and the antenna gains are G_{TX} and G_{RX} for the transmitter and receiver side respectively. According to the Friis transmission equation, the received signal power at the receiver input is

$$P_{RX} = P_{TX} \times G_{TX} \times G_{RX} \times (\frac{\lambda}{4\pi R}). \tag{1.1}$$

The Friis equation can be written in dB format as

$$P_{RX} = EIRP + G_{RX} - FSPL, \tag{1.2}$$

$$EIRP = P_{TX} + G_{TX}, \tag{1.3}$$

$$FSPL = 20log(\frac{\lambda}{4\pi R}), \tag{1.4}$$

where Equivalent Isotropic Radiated Power (EIRP) is the transmitter output power plus the transmitter antenna gain, and the last term is the Free Space Path Loss (FSPL) . FSPL describes the loss in signal power level due to line-of-sight (LOS) propagation through free space. It assumes isotropic antennas on both the transmit and receive side.

Table. 1.1 lists the FSPL for various link distances at four different carrier frequencies. One can already observe the challenge for the 60 GHz transmitter design. The FSPL increases with the carrier frequency, e.g. the FSPL at 2.4 GHz for 10

Table 1.1: The assigned EIRP and FSPL for various distances and frequencies.

Frequency [GHz]	FSPL [dB]			EIRP [dBm]
	R=2m	R=10m	R=100m	
2.4	46	60	80	36
5	52	66	86	53
24	66	80	100	55
60	74	88	108	85

meters is around 60 dB, but it increases by 28 dB when the carrier frequency goes up to 60 GHz. To maintain the same transmission distance, the transmitter EIRP must be increased accordingly.

The link specifications are ultimately set by the receiver's Signal to Noise Ratio (SNR) requirement. The SNR at the receiver output can be expressed as

$$SNR_{RX} = EIRP + G_{RX} - FSPL - (NF + 10log(BW) + 174), \qquad (1.5)$$

where 174 dBm is the noise floor, BW is the receiver bandwidth and NF is the receiver noise figure. From (1.5) one can see the second challenge for mmW transmitters. For the same received SNR , larger data rate links require larger receiver bandwidth and therefore require larger EIRP . Current mmW standards demand a radio bandwidth significantly larger than any existing WiFi or cellular standard. For example, the WiGig standard utilizes a RF bandwidth of 1.76 GHz, which is 44 times larger than the 40 MHz bandwidth utilized by the 802.11n standard. As a result, transmitters need to deliver larger EIRP at mmW frequencies to achieve the same SNR level. The maximum allowable EIRP of 85 dBm is assigned by FCC for 60 GHz applications [3]. Achieving such high level of EIRP requires mmW PAs delivering high output power which is challenging especially for transistors operating near transient frequencies. Utilizing this drawback in our favor, radiation from one particular 60 GHz radio link is quickly reduced to a level that will not interfere with other 60 GHz links operating in the same geographic vicinity. This reduction enables higher "frequency reuse" — the ability for more 60 GHz links to operate in the same geographic area than links with longer ranges [6].

Directivity, a measure of how well an antenna focuses its energy in an intended direction, is particularly important in the design of 60 GHz communication links [6]. Point-to-point radios should have highly directional antennas as the goal is to connect

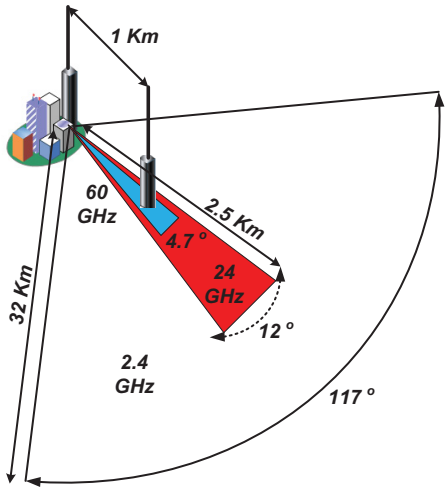


Figure 1.5: Antenna focus for unlicensed bands [6].

Frequency	Beam Width
2.4 GHz	117 degrees
24 GHz	12 degrees
60 GHz	4.7 degrees

Table 1.2: Antenna focus for unlicensed bands [6].

only end points of a link. Ideally, all the transmitted energy is directed just toward the intended recipient. "Highly focused antennas minimize the possibility of interference between links in the same geographic area, and the risk that the transmission will be intercepted, while maximizing the overall performance" [6]. Operating at higher frequencies inherently results in a more focused antenna. Antenna directivity is limited by the physical principle of diffraction which states that the beam width is inversely proportional to the operating frequency. Therefore, the beam width is far narrower at 60 GHz than that of lower frequency bands. Table 1.2 shows the beam width for several unlicensed frequency bands [6].

The combined effects of oxygen absorption and narrow beam spread result in high security, high frequency reuse, and low interference for 60 GHz communications [6]. Fig. 1.5 shows two buildings which are 1 km apart. The wedges show the radiation pattern for 2.4 GHz, 24 GHz and 60 GHz links operating with the same performance at 1 km. The links have equivalent 1 ft diameter antennas. The three wedges show the locations where the radiation at each frequency remain high. The largest wedge

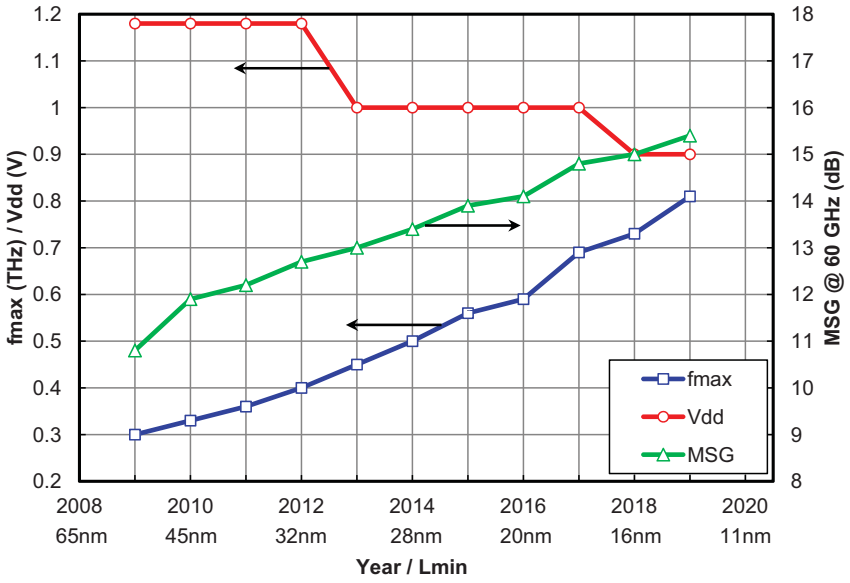


Figure 1.6: ITRS Roadmap for RF CMOS Technology [8].

represents the radiation pattern for a 2.4 GHz link. The 60 GHz link has the narrowest and the shortest wedge, and it can be barely seen except in the enlarged figure. The wedges for 2.4 GHz and 24 GHz links are substantially larger than that for 60 GHz link, even though their operational link distance is the same (1 km). Therefore, a 60 GHz link can only be intercepted in the tiny wedge and will only interfere with another 60 GHz link in that wedge. A 24 GHz link has interference and interception risks over a much longer and relatively broader wedge, while a 2.4 GHz link has interference and interception risks over a very large area, both in distance and in breadth [6].

1.1.2 CMOS technology for 60 GHz RFIC

Traditionally, mmW designs have been limited to expensive III-V compound technologies due to their higher frequency of operation, and thus higher gain compared to silicon technologies. However, the microprocessor and memory industry has continued to push advances in silicon, increasing the maximum frequency of operation (f_{max}) of CMOS devices year by year. Due to its aggressive scaling, CMOS technology, which was mainly used for digital computations and certain low frequency analog circuits, is now capable of operating at speeds in excess of 300 GHz. According to

ITRS roadmap for RF CMOS technology as shown in Fig. 1.6, the f_{max} of CMOS devices will reach 1 THz by the end of this decade [7]. With recent advances in CMOS technologies, ultra deep sub-micron MOSFETs (e.g. 65nm, 40nm and 28 nm) with more than enough f_{max} (up to 300 GHz) are available for mmW design. Hence, the available power gain at 60 GHz continues to increase. This increase in operating frequency, however, has to come at the expense of a continued reduction in supply voltage (V_{DD}). This can be understood by deriving the dynamic power consumption for a basic digital gate as

$$P_{dyn} = \alpha \times C \times f \times V_{DD}^2, \tag{1.6}$$

where α is the activity factor, C is the total load capacitance, f is the clock frequency and V_{DD} is the supply voltage. Therefore, for digital signal processing, lowering the supply voltage helps to significantly reduce power consumption. Unfortunately, noise, linearity, and output power all require higher supply voltages to improve. Therefore, analog design becomes more challenging with reduced supply voltages. This means we must be more careful when designing with CMOS and we must make the right architectural choices to enable circuit design at reduced supply voltages. Holistic optimization from overall architecture down to individual building blocks is a necessity. At the same time, CMOS provides many advantages over other compound technologies. The first advantage comes from the low power consumption of baseband signal processors in CMOS . This enables complete integration of mmW circuits with low frequency mixed-signal circuits and digital baseband processors all on the same die, eliminating the need for complex and costly packaging of multiple dies. Moreover, the integration capability of CMOS technology eliminates additional cost of the Front-End-Module (FEM) design because all signals are processed on the same die, so no high frequency or high dynamic range I/O are required.

Also, integrating mmW circuitry with CMOS digital signal processing units allows built-in-self-test (BIST) capabilities on the same die, therefore reducing test time and test complexity. BIST allows transceivers to self-test and self-calibrate, helping to quickly screen out faulty parts or debug problems to increase reliability. Finally, the small wavelength of 60 GHz signals also provides advantages for integration of passive components. At 60 GHz, the free-space wavelength is approximately 5 mm, while the on-chip wavelength is approximately 2.4 mm on silicon dioxide (SiO_2) substrate. These dimensions are on the order of typical die sizes for integrated circuits. One

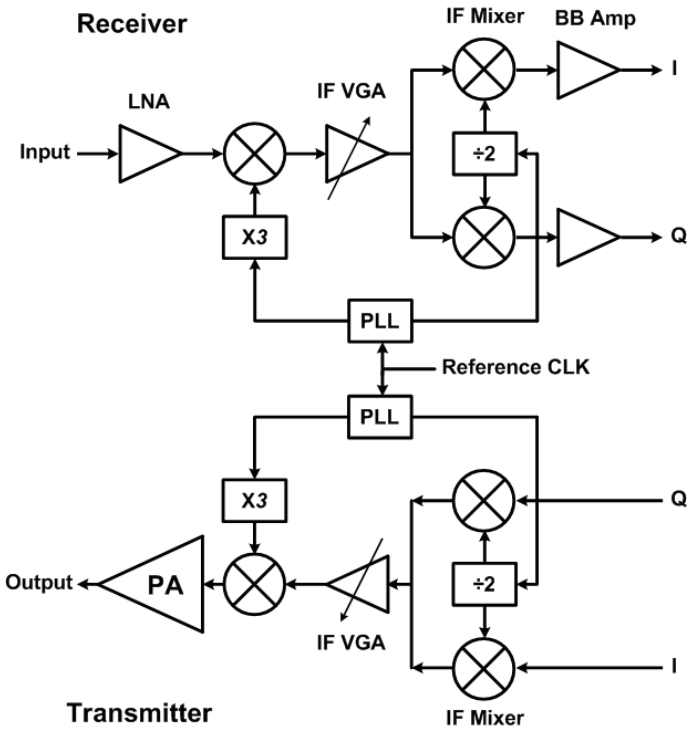


Figure 1.7: Block diagram of a 60 GHz transceiver.

consequence is distributed effects which must be taken into account, making mmW circuit design more difficult. From another point of view, required on-chip passive components such as capacitors and inductors become very small and easy to integrate at mmW frequencies. At these frequencies, even antennas can be integrated on-chip thus mmW signals are not required to be transferred off-chip.

1.1.3 60 GHz transceivers

The block diagram of a typical 60 GHz transceiver is shown in Fig. 1.7. It consists of a transmitter path and receiver path, and baseband signals (I and Q) which are generated and processed by the digital processors. At the transmitter side, the base band analog signals produced by Digital to Analog Converters (DAC) are converted to RF signal, by up-conversion mixers. The up-conversion procedure can be performed directly (direct conversion) or it can be done using dual conversion or sliding IF architectures where two mixers are used to generate the IF and RF signals. The up-converted signals are then amplified by a PA before being propagated through the antenna. As the last stage of the transmitter front-end, PA plays a critical rule in

signal. Antennas with high gain are expensive, area inefficient and therefore not compatible with low cost mobile applications. Increasing the maximum communications distance requires increasing the transmitted or radiated power. Thus, the FCC assigned high allowable EIRP for 57-64 GHz unlicensed frequency band for short-range high-speed communication [3].

In 2005, an alternative group of 802.15.TG3C was formed to develop an alternative mmW -based standard to the 802.15.3-2003 standard for WPAN applications. Berkeley Wireless Research Center (BWRC) at the University of California at Berkeley (UCB) , and IBM were the pioneers who started the research in this field. IBM Watson Research Center presented a 60 GHz chip set in 2006. The transceiver was packaged in a chip-on-board assembly and was implemented in 0.13 μm Silicon-Germanium (SiGe) technology [8]. The transceiver achieved a 630 Mbps data rate over 10 meters. After SiGe 60 GHz transceivers were demonstrated, BWRC implemented a 60 GHz transceiver in 0.13 μm CMOS [9]. The design consists of a three-stage Low Noise Amplifier (LNA) , Phase Locked Loop (PLL) , low pass filter, Voltage Controlled Oscillator (VCO) , frequency divider, multiplexer and IF mixer, occupying a total chip area of 3.4mm $\times$ 1.7mm.

Another 60 GHz receiver with on-chip incorporated antennas has been reported by Toshiba in 2007 [10]. The on-chip receiver is designed in 90 nm CMOS technology including a one-stage LNA, PLL synthesizer, and down-conversion mixer in only a 2.6 mm^2 area. The receiver required only 144 mW of power [10]. In 2009, the Georgia Institute of Technology presented two up-conversion transmitters in 90 nm CMOS technology [11]. A single ended transmitter for low power applications was used in the first transmitter, while the second transmitter was a differential design for high performance applications. The designs contained a VCO, a local amplifier, a mixer, and a three-stage power amplifier with the gain of 8.6 dB, compression point of 1.5 dBm, and 76 mW power consumption.

Other 60 GHz prototype transmitter and receiver chips in SiGe for IEEE 802.15.3c standard were demonstrated by IBM and MediaTek in 2010 [12]. The receiver achieved 72 dB gain with 1.8 W power consumption from a 2.7 V supply in an area of 6.08mm $\times$ 6.2mm. Although the transmitter could achieve a gain of 40 dB, it required a substantial area of 44 mm^2, and a complex 16-way spatial power splitter to distribute and combine the signals for separated elements in the array. Meanwhile, designing RF front-ends in SiGe technology with high level of core supply voltage in-

creases the cost of design because it cannot be integrated with the commercial CMOS base-band core.

Since 2010, CMOS transceivers for 60 GHz applications are interested with migrating to more advanced ultra-deep submicron CMOS technologies with higher gain-bandwidth product. A fully integrated 60 GHz module is presented in 65 nm CMOS technology for wireless high-definition video streaming ($WirelessHD^{\text{TM}}$ standard) [13]. It could achieve a maximum data rate of 3.8 Gbps. To achieve more than 1 meter transmission range in an office-like area, while consuming 1.37 W in transmitter mode. The PA consumed 1 W (75% of total power) to deliver the maximum power of 13.5 dBm. Maximum Power Added Efficiency (PAE) of 8% was measured and the power gain of the amplifier was measured to be 16.5 dB. Power consumption and smaller die area challenges were slightly improved using modern CMOS technologies with short channel width and low core voltage supply. However, it was still challenging to achieve more than 10 Gbps data rate because of I/Q mismatch, gain flatness and phase noise, which degrade the Error Vector Magnitude (EVM) performance.

The highest data-rates of 20 Gbps and 28.16 Gbps are reported by Tokyo Institute of Technology (TIT) with 60 GHz transceivers implemented in 65 nm CMOS technology [14] [15]. Direct-conversion architecture using a digital calibration technique is used to improve the I/Q mismatch of the system [14]. Although the very high achieved data-rate make the designs attractive for use in the next generation of wireless communications, they still suffer from the power consumption issues. With the 6 dBi built-in antenna, the transmitters achieved a transmission gain of 30 dB and only 9 dBm of saturated output power (P_{sat}), which degraded the transmission range to less than a meter.

Aforementioned transceiver chips prove that the 60 GHz CMOS products are on the verge of commercial viability, although technical problems remain to be solved for improving power efficiency to minimize transceivers power consumption, increasing output power to achieve longer transmission range, and decreasing the chip area to reduce the overall cost of 60 GHz communication systems. This dissertation investigates the challenges of designing mmW power amplifiers for 60 GHz applications, proposes concepts and techniques that ease the power/efficiency bottleneck for incorporating 60 GHz transceivers into the next generation mobile devices implemented in the low cost digital CMOS process. The scope of investigation and proposal extends from the architecture level down to the transistor level.

1.2 Thesis Organization

This research focuses on the design challenges and implementation of 60 GHz power amplifiers in 65 nm CMOS technology. The design, modeling and layout optimization of passive structures such as on-chip transformers, power combiners as well as mmW power transistors are investigated. Three power amplifiers are designed and implemented in standard 65 nm CMOS technology. The rest of this thesis is organized as follows.

Chapter 2 introduces some basic concepts about power amplifiers including classification of amplifiers, characteristics and figure of merits. Subsequently, we review the state of the art of 60 GHz CMOS power amplifiers. This review focuses on the technology challenges that face the design and implementation of 60 GHz PA in CMOS process such as: delivering high output power in presence of low supply voltage of MOSFETs, efficiency-gain trade off in cascaded multiple stages, and power combining techniques as a solution to increasing the output power of PAs.

Chapter 3 describes the methodology of PA design in 65 nm standard CMOS technology. The modeling methodology of 60 GHz passive circuits and active devices is presented in this chapter. The development of a new multi-conductor power combining topology is illustrated through EM simulations and layout optimization. Fabricated PA employing the proposed compact combiner is compared with others based on the measured performance.

Chapter 4 presents design, implementation and performance evaluation of a 60 GHz PA employing a new circuit technique which targets an efficiency improvement. The theory of the proposed dual-mode topology is discussed and used in a three stage PA. Design of high-gain driver stages using a new gain enhancement technique is presented. Fabricated PA is compared with others based on measured results.

Chapter 5 presents a highly-efficient high-power 60 GHz distributed active transformer PA. This PA circuit includes three stages: the DAT stage including PA cells, a common source driver, and a neutralized cascode stage. The design technique utilized in DAT layout topology is discussed. A new dual-mode circuit topology is used to increase the efficiency of PA cells. Design procedure of driver/gain stages are presented with simulation of inter-stage matching and gain-enhancement techniques. Performance evaluations are performed based on the measured results of the fabricated PA. Conclusions are given in chapter 6.

Chapter 2

60 GHz Power Amplifiers

As the last active building block in a wireless transmitter responsible for producing the required transmission signal power, PA is the most power consuming block responsible for 50% to 80% of the total power consumption of 60 GHz transceivers [13–15]. As a result, the power efficiency of the PA is directly related to the efficiency of the transmitter and the battery life for portable wireless devices. A major challenge in the design of mmW PA is balancing the operation of the active devices near their cut-off frequencies, while achieving a high level of RF power and acceptable linearity. Moreover, the process of power conversion directly depends on the small and large-signal behavior of the active devices. This chapter covers the fundamental theory of RF PAs. Figure of merit for RF PAs are introduced with respect to the class of operation. For a practical RF PA design, it is necessary to do both small-signal and large-signal analysis of active stages. The major difference of the PA design compared to a conventional small-signal amplifier design is that the simple linear conjugate matching cannot deliver the optimum power to the desired output impedance [16]. In other words, the theory of maximum power delivery cannot be applied simply to PAs. Design challenges of PAs at mmW frequencies are presented by reviewing the state of the art of 60 GHz power amplifiers.

2.1 Fundamentals of Power Amplifiers

The theory and analysis of a single-stage RF amplifier have been covered by RF design references [17] [16]. Fig. 2.1 shows a RF PA as a black box. As a RF building block, we can consider a PA operating as a power converter which must be able to

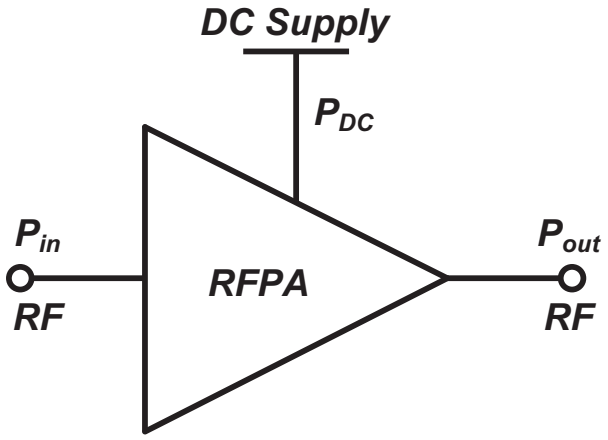


Figure 2.1: Block diagram of a conventional PA.

increase input RF signal power by consuming DC power. To quantify the efficiency of PAs, several efficiency measures are used. The so-called drain efficiency (η_D) of the PA is defined as the ratio of the output power P_{out} to the DC power supplied to the drain of the PA device as

$$\eta_D = \frac{P_{out}}{P_{DC}}. \tag{2.1}$$

The drain efficiency tells how much power is being dissipated during the DC to AC power conversion. The losses include power dissipation in the transistor as well as in the passive matching network. The other widely used efficiency measure is the PAE expressed as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}, \tag{2.2}$$

takes into account the additional power used to drive the PA device and is defined as the ratio of the added power P_{out} - P_{in} to the DC power P_{DC}. PAE is related to the drain efficiency by the power gain of the PA (G_P) as

$$PAE = (1 - \frac{1}{G_P}) \times \eta_D. \tag{2.3}$$

An advantage of using the PAE measure is the simplicity in the calculation of power efficiency of a cascaded chain of similar amplifiers. Cascading amplifier stages is a common technique to improve the overall power gain of a PA. Assume each

amplifier has a drain efficiency of η_D and power gain of G_P, the output power of the n^{th} stage is

$$P_{out}n = \frac{P_{out}}{G_P^{(N-n)}}. \tag{2.4}$$

Summing the DC power of each stage, the total DC power is

$$P_{DC} = \sum_{n=1}^{N} P_{DC}(n) = \frac{P_{out}}{\eta_D} \times \frac{1 - \frac{1}{G_P^N}}{1 - \frac{1}{G_P}}. \tag{2.5}$$

The PAE of the cascades PAs is

$$PAE_{cascaded} = P_{out} \frac{1 - \frac{1}{G_P^N}}{\frac{P_{out}}{\eta_D} \frac{1 - \frac{1}{G_P^N}}{1 - \frac{1}{G_P}}} = (1 - \frac{1}{G_P}) \times \eta_D = PAE_{core}. \tag{2.6}$$

Therefore, the cascaded PAE is identical to the single-stage PAE . When number of stages (N) approaches a sufficiently large number, the input power becomes negligible and the PAE represents the total power efficiency of the amplifier chain.

Internally, the PA is designed utilizing semiconductor devices operating as a voltage-dependent current source. For metal-oxide-semiconductor field effect transistor (MOSFET) devices, the current of the transistor is controlled by the input voltage across the gate-source and drain-source junctions. The output voltage will then be defined by the amount of current flowed into the load network. As a result, the output power and the efficiency of amplifiers directly relates to the behavior of the internal transistors. Amplification must be done using transistors which are biased to handle a certain gate-source voltage and drain current flow (quiescent point). For the case of PA, transistor nodes experiences signals with very large swing. Hence, the quiescent point is input-dependent meaning that RF PAs cannot be characterized as a Linear Time Invariant (LTI) system. Depending on the voltage-current characteristics, PAs are usually classified as linear amplifiers and non-linear amplifiers. Within each category, multiple classes are defined according to the voltage and current waveforms. PAs operating in different classes are analyzed in following subsections.

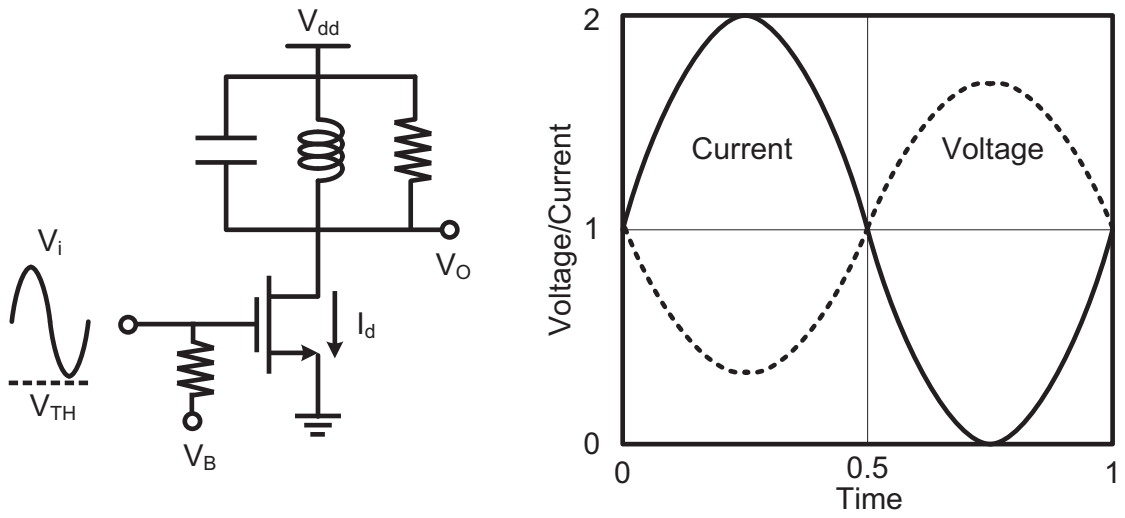


Figure 2.2: Schematics and V-I waveforms of Class-A amplifiers.

2.1.1 Linear Class PAs (Class A)

Linear amplifiers produce an output signal proportional to the input signal with a specific time delay. In other words, the gain of a linear amplifier is constant, independent of the input signal level. MOSFET devices in such an amplifier must operate between cutoff and triode region to achieve a constant transconductance. Hence, linear amplifiers are known as transconductance amplifiers, meaning the device operates as a current source with a constant transconductance gain of g_m. The most simple amplifier that produces such a behavior is the Class-A amplifier. In Class-A amplifiers, the transistor is biased in saturation region, so that conducts current at all time. Hence, the overdrive voltage must be high enough in order to keep the device in saturation region. A basic MOS Class-A amplifier and the voltage/current waveforms at the drain node are shown in Fig. 2.2. Theoretically, if the input drive signal is perfectly sinusoidal, then the output current will also be sinusoidal with no harmonic content. In order to maximize the linear current swing, the DC bias current I_{bias} is usually set to half of the maximum current I_{max} that the transistor can sink and the maximum available voltage swing is V_{dd}-V_{ov}. As a result, the available maximum output power is

$$P_{out}^{A} = \frac{1}{2} V_{pp} I_{pp} = \frac{1}{4} (V_{dd} - V_{ov}) I_{max}. \tag{2.7}$$

According to the maximum power transfer theorem, this maximum available output power is achieved when the amplifier is loaded by an appropriate load impedance to maximize the voltage and current swings simultaneously. This optimal load impedance can be expressed as a ratio of the maximum available voltage swing and the current swing as

$$R^A_{opt} = 2 \times \frac{V_{dd} - V_{ov}}{I_{max}}. \tag{2.8}$$

The MOSFET device cannot handle enough current to generate the maximum voltage swing for load impedances smaller than R^A_{opt}. Likewise, if the load impedance is larger than R^A_{opt}, the amplifier becomes voltage limited, meaning that only a fraction of the current swing is sufficient to saturate the voltage swing. In both cases, the output power decreases from P^A_{out}. The peak drain efficiency of Class-A amplifiers in presence of the load impedance R^A_{opt} is

$$\eta^A_D = \frac{P^A_{out}}{P_{DC}} = \frac{\frac{(V_{dd}-V_{ov})I_{max}}{4}}{\frac{V_{dd}I_{max}}{2}} = \frac{V_{dd} - V_{ov}}{2V_{dd}} = 50\%. \tag{2.9}$$

Class-A amplifiers achieve the highest possible linearity, gain and output power because the device operates as a transconductance amplifier at all time. On the other hand, Class-A amplifier dissipates DC power for all the period of time during a cycle. As shown in Fig. 2.2, Both of the current and voltage waveforms contain DC value that is dissipated by transistor. However, 50% of the total consumed power is dissipated when the load is not being driven by the transistor. In the other words, the transistor dissipates power regardless of weather the load has been driven or not.

2.1.2 Non-Linear PA Classes (Class B, AB, and C)

One possible solution to improve the efficiency is keeping the transistor near the cutoff region when the load is experiencing non-zero voltage/current. Thus, there will not be overlap between the driving and power consuming cycles. A simple technique to achieve this goal is to bias the transistor at the threshold voltage (V_T) such that the transistor is conducting current during half of the cycle. For the next half of the cycle, the resistive load is derived by the LC tank. Fig. 2.3 shows the circuit implementation, drain current and voltage waveforms of such amplifiers known as Class-B. Since the transistor is only conducting current for half of the cycle, the

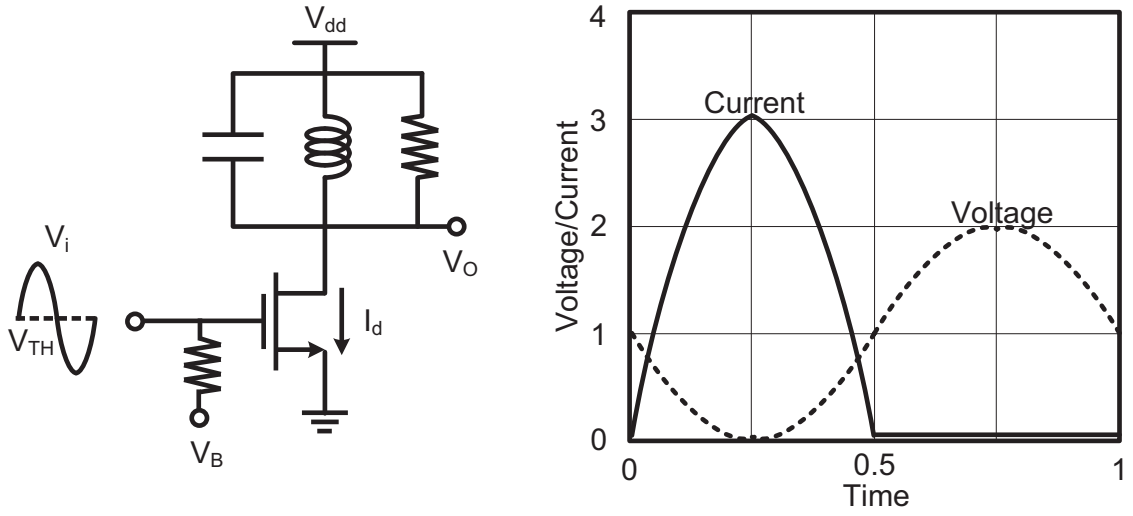


Figure 2.3: Schematics and V-I waveforms of Class-B amplifiers.

amount of V-I overlap is reduced by 50%.

The transistor consumes a half-wave rectified sinusoidal current, with a fundamental component of $\frac{I_{max}}{2}$ and a DC value of $\frac{I_{max}}{\pi}$. The output power, optimal load impedance and the drain efficiency of Class-B amplifiers can be found as

$$P_{out}^{B} = \frac{1}{2} V_{pp} I_{pp} = \frac{1}{4}(V_{dd} - V_{ov}) I_{max}, \tag{2.10}$$

$$R_{opt}^{B} = 2\frac{V_{dd} - V_{ov}}{I_{max}}, \tag{2.11}$$

$$\eta_{D}^{B} = \frac{P_{opt}^{B}}{P_{DC}} = \frac{\frac{(V_{dd}-V_{ov})I_{max}}{4}}{\frac{V_{dd}I_{max}}{\pi}} = \frac{\pi(V_{dd} - V_{ov})}{4V_{dd}} = 80\%. \tag{2.12}$$

Compared to Class-A amplifiers, Class-B amplifier achieves 30% higher peak drain efficiency, but delivers the same peak output RF power. The main drawback is that the amplifier becomes slightly nonlinear, because the effective bias condition of the MOSFET varies by the input signal. A substantial amount of second harmonic is generated because of the semi-switching behavior of the amplifier. However, the amplifier can be considered as a semi-linear class due to the constant transconductance of the device during the conduction time. Another disadvantage of the Class-B operation is the higher drive level required in Class-B to maintain a peak current of

I_{max} compared to the peak of $I_{max}/2$ in Class-A mode. Increasing of 6 dB in drive level results in a reduction in the power gain of the device which is a challenge for mmW designs. To improve the linearity of Class-B amplifiers, the gate bias of the transistor can be set slightly higher than the threshold voltage so that the transistor is conducting current more than half of the cycle, but still much less than the entire cycle. This method is so-called Class-AB amplification. As a result, the efficiency will lie between Class-A and Class-B amplifiers depending on the conduction time of the transistor. To find the power and efficiency of Class-AB amplifiers, the conduction angle (α) can be defined as the total number of radians in one cycle when the transistor is conducting current. Then, the DC and RF components of the truncated output current waveform are expressed as a function of the conduction angle. The mean value (DC component) of the current waveform will be decreased as the α reduced. If a truncated waveform is input into an RLC network, harmonic components will be generated. The fundamental component can be found by Fourier analysis of the waveforms. The total RF current of the transistor can be written as

$$I_d(\theta) = \begin{cases} 0 & 0 < \theta < \alpha \\ I_{bias} + I_{max}cos(\theta) & \alpha < \theta < 2\pi \end{cases}, \tag{2.13}$$

$$\alpha = cos^{-1}(-\frac{I_q}{I_{pk}}), \tag{2.14}$$

$$I_{pk} = I_{max} - I_q. \tag{2.15}$$

Substituting 2.14, and 2.15 into 2.13 gives the total output current as a function of conduction angle and the maximum available current as

$$I_d^\theta = \frac{I_{max}}{1 - cos(\alpha)/2}[cos(\theta) - cos(\alpha/2)]. \tag{2.16}$$

Integration over the conduction angle gives the DC component or the mean value of the current as

$$I_{DC} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)}[\cos(\theta) - \cos(\alpha/2)]d\theta. \tag{2.17}$$

And the magnitude of the n^{th} harmonic can be written as

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)}[\cos(\theta)-\cos(\alpha/2)]\cos(\theta)d\theta. \tag{2.18}$$

The DC value and fundamental value of the peak-to-peak RF current can be calculated as

$$I_{DC} = \frac{1}{2\pi} \times [\frac{2sin(\alpha/2)-\alpha cos(\alpha/2)}{1-cos(\alpha/2)}], \tag{2.19}$$

$$I_{pp}(\alpha) = \frac{1}{2\pi} \times [\frac{\alpha - sin(\alpha)}{1-cos(\alpha/2))}] \times I_{max}. \tag{2.20}$$

Finally, the output power, optimal load impedance and the drain efficiency of Class-AB amplifiers can be found as

$$P_{out}^{AB}(\alpha) = \frac{1}{4\pi}[\frac{\alpha - sin(\alpha)}{1-cos(\alpha/2))}]I_{max}(V_{dd}-V_{ov}), \tag{2.21}$$

$$R_{opt}^{AB}(\alpha) = 2\pi[\frac{1-cos(\alpha/2)}{\alpha - sin(\alpha)}]\frac{V_{dd}-V_{ov}}{I_{max}}, \tag{2.22}$$

$$\eta_D^{AB} = \frac{P_{out}^{AB}}{P_{DC}} = \frac{1}{2}[\frac{\alpha - sin(\alpha)}{2sin(\alpha/2)-\alpha cos(\alpha/2)}][1-\frac{V_{ov}}{V_{dd}}]. \tag{2.23}$$

$$\alpha \in [\pi, 2\pi]. \tag{2.24}$$

By decreasing the conduction angle to very lower than half of the cycle, the resulted current waveform has lower DC component, and also lower fundamental RF component compared to the Class-AB conditions. Such amplifiers are known as Class-C amplifiers as shown in Fig. 2.4. Class-C amplifiers conduct current less than the previous counterparts so that experience such smaller overlap between voltage and current waveforms. Hence, the transistor experiences more relaxed time and Class-C amplifiers achieves even higher efficiency compared to linear amplifiers. The expressions for output power, optimal load impedance and efficiency of Class-C amplifiers are the same as Class-AB amplifiers, but the conduction angle is smaller than π. Unfortunately, Class-C amplifier produces significant amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions. Hence, it cannot be directly used for

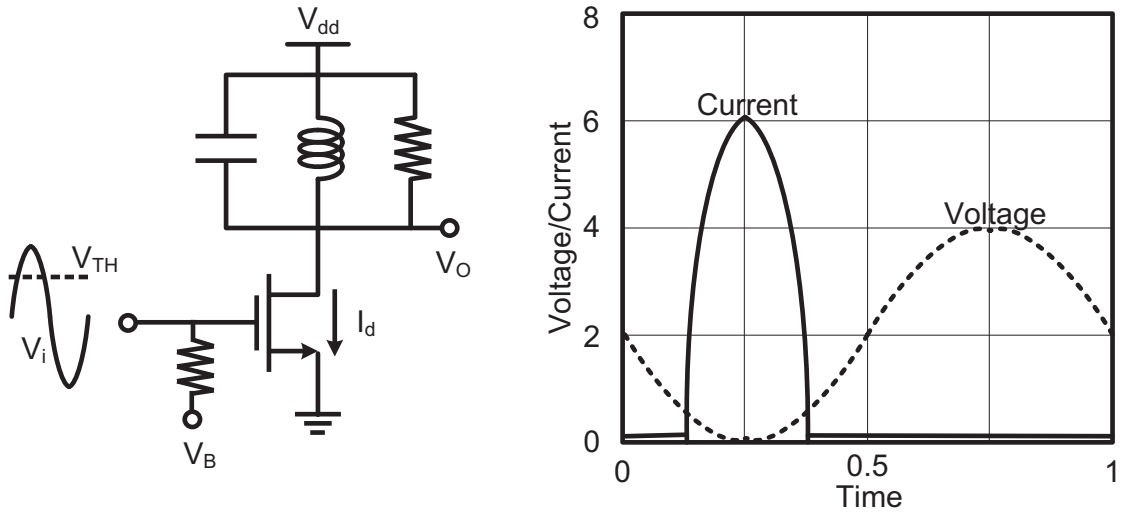


Figure 2.4: Schematics and V-I waveforms of Class-C amplifiers.

amplitude modulations. However, most non-linear amplifiers are still linear in phase, and have no phase-to-phase (PM-PM) distortions. Therefore, they are often used for amplifying phase modulated signals such as Phase Shift Keying (PSK) or Gaussian Minimum-Shift Keying (GMSK)) signals. The main advantage of most non-linear amplifiers is the high drain efficiency. A linear transconductance amplifier can be turned into a non-linear amplifier by biasing the transistor below threshold voltage. The output power, optimal load impedance and the drain efficiency of Class-C amplifiers can be found as

$$P_{out}^{C}(\alpha) = \frac{1}{4\pi}[\frac{\alpha - sin(\alpha)}{1 - cos(\alpha/2))}]I_{max}(V_{dd} - V_{ov}), \tag{2.25}$$

$$R_{opt}^{C}(\alpha) = 2\pi[\frac{1 - cos(\alpha/2)}{\alpha - sin(\alpha)}]\frac{V_{dd} - V_{ov}}{I_{max}}, \tag{2.26}$$

$$\eta_{D}^{C} = \frac{P_{out}^{AB}}{P_{DC}} = \frac{1}{2}[\frac{\alpha - sin(\alpha)}{2sin(\alpha/2) - \alpha cos(\alpha/2)}][1 - \frac{V_{ov}}{V_{dd}}], \tag{2.27}$$

$$\alpha \in [0, \pi]. \tag{2.28}$$

In theory, Class-C amplifiers can reach drain efficiency as high as 100%. However, this is achieved at zero conduction angel, which means the output power also drops

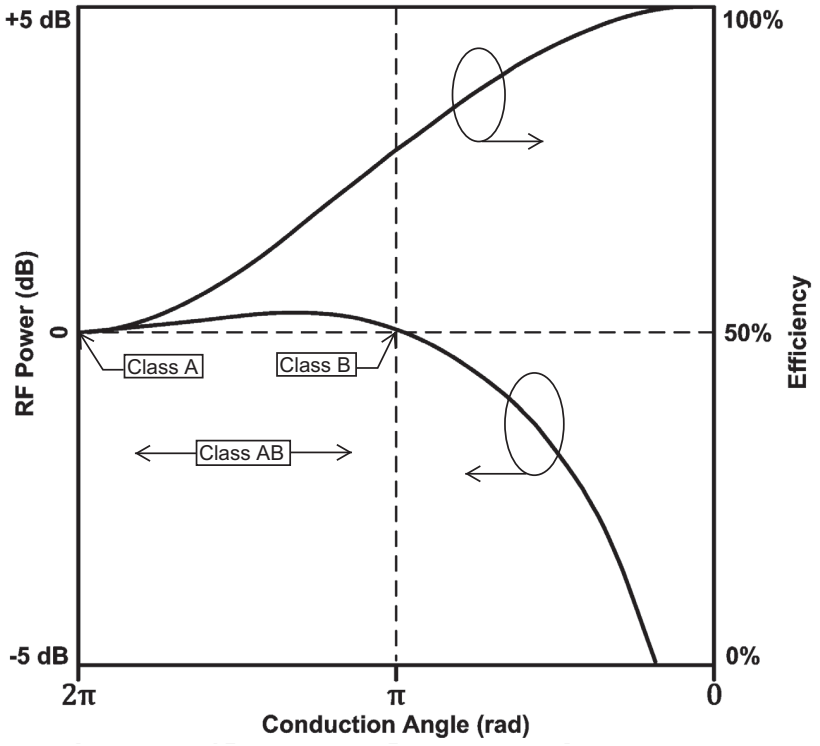


Figure 2.5: RF power and efficiency trade-offs for different class of operations.

to zero according to (2.25). The efficiency and normalized maximum available power are illustrated in Fig. 2.5 with respect to the conduction angle. The harmonic level increases progressively when the conduction angle is reduced and the output signal will not be a pure sinusoidal. "One of the most important concepts in comparing different PA configurations is the Power Utilization Factor (PUF) . The PUF is the ratio of RF power delivered by the device in particular mode under consideration to the power it would deliver as a Class-A amplifier. On the other hand, PUF is a statement on cost efficiency, or watts per dollar" [16]. Although the efficiency increases rapidly for conduction angle lower than π, the reduced conduction time reduces the RF power transmitted. Unlike Class-AB amplifiers, Class-C amplifier has a clear trade-off between output power and drain efficiency. For 60 GHz applications, where attenuation is the main issue, the maximum available RF power is a major concern as well as the PAE . One of the major challenges in designing Class-C PAs is the large negative swing of input voltage, which coincides with the drain output voltage peaks. This is precisely the worst condition for reverse breakdown in MOSFET transistors, and even small amounts of leakage current flowing at this point of the cycle

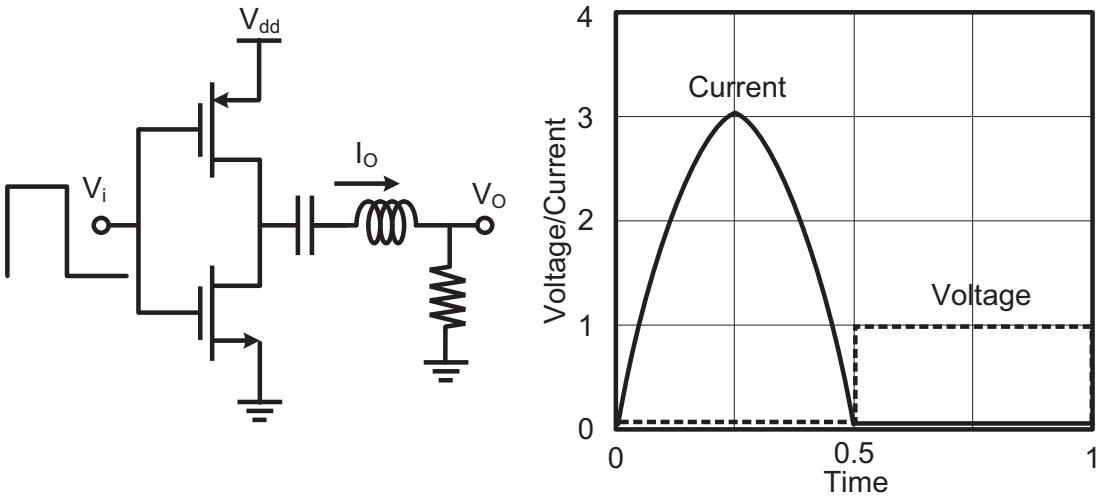


Figure 2.6: Schematics and V-I waveforms of Class-D amplifiers.

will have a detrimental effect on the efficiency. Considering the definitions above, the Class-A is the most preferred PA which fulfills the 60 GHz power requirements due to its high PUF and highly linear voltage swing. Class-B and Class-AB PAs could be alternatives where a design technique is used to achieve an acceptable RF power at 60 GHz.

2.1.3 Switching Mode PAs (Class D, E and F)

More widely used non-linear amplifiers at lower frequency communications are switching amplifiers [16]. However, recent advances in CMOS technology improved the operation frequency of devices up to 300 GHz meaning that high performance switching is enabled at mmW frequencies. In switching amplifiers, the operation region of transistor changes from triode region to cut-off region and vice versa. This behavior is in contrast with transconductance amplifiers in which transistors remain in saturation region. So-called Class-D amplifiers utilize two transistors in push-pull configuration as shown in Fig. 2.6. Driven in such a way that transistors are alternately on and off, an ideal Class-D PA produces a square voltage waveform. In order to achieve a sinusoidal output, the load circuit contains a series LC band-pass filter. Fig. 2.6 shows the voltage and current waveforms generated by one transistor and flowing into the load.

Since only fundamental frequency current can flow through the filter, each of the

two transistors contribute half cycle of the sinusoidal current waveform. It must be noted that the amplitude of the fundamental component of a square wave voltage is $2/\pi$ times the amplitude of the square wave. Since there is not overlap between drain voltage and the transistor's current, zero DC power is dissipated and the peak drain efficiency can be 100% theoretically. The maximum voltage and current swings are

$$V_{pp} = \frac{2}{\pi} V_{dd}, \tag{2.29}$$

$$I_{pp} = I_{max}. \tag{2.30}$$

Therefore the output power, optimal load impedance and the drain efficiency can be found as

$$P_{out}^{D} = \frac{1}{\pi} V_{dd} I_{max}, \tag{2.31}$$

$$R_{out}^{D} = \frac{V_{pp}}{I_{pp}} = \frac{2}{\pi} V_{dd} I_{max}, \tag{2.32}$$

$$\eta_{D}^{D} = \frac{V_{pp} I_{pp}}{2 V_{DC} I_{DC}} \simeq \frac{\frac{1}{\pi} V_{dd} I_{max}}{V_{dd} \frac{1}{\pi} I_{max}} = 100\%. \tag{2.33}$$

The main advantage of Class-D PA is its high power capability compared to Class-A to C. However, switching operation modes in CMOS devices are applicable for frequencies substantially below the f_T. Unfortunately, transistor's gate node parasitic capacitance increases linearly with charging the gate. Hence, the high frequency component of the input waveform will be filtered. Moreover, the drain-source capacitor (C_{ds}) removes the output high frequency components and smooths the edges of the square waveform, and thereby creates overlap between voltage and current waveforms. Hence, efficiency drops because of the limited switching performance and the large parasitic drain-source capacitance of transistors at high frequencies. Accordingly, Class-D amplifiers are not widely used for high frequency designs due to dramatically reduced efficiency.

In order to overcome the hard switching issues imposed on the transistors, Class-E amplifiers are developed. The transistor output parasitic capacitance (C_{ds}) can be absorbed into an impedance matching network in Class-E configuration and an

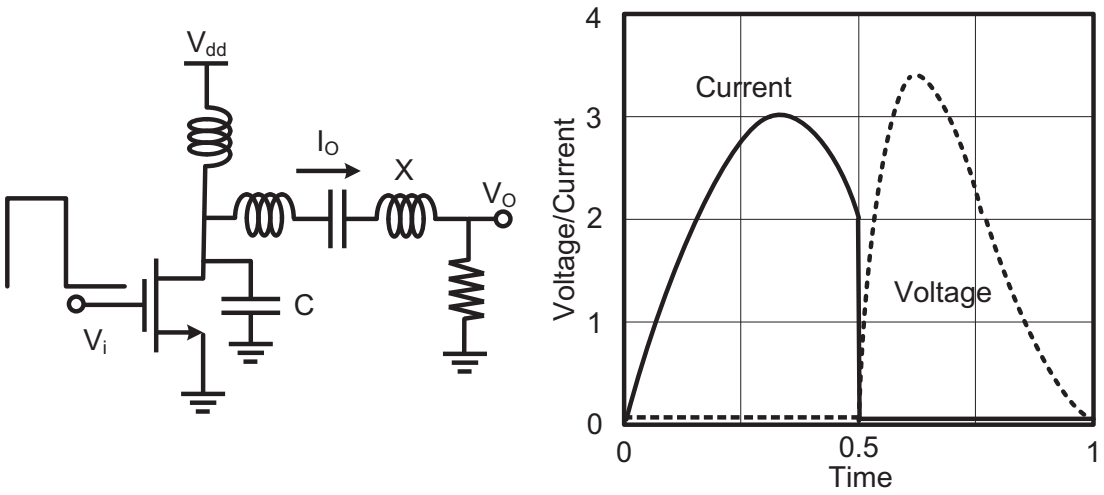


Figure 2.7: Schematics and V-I waveforms of Class-E amplifiers.

inductor choke can relax the output voltage waveform so that no sharp transition is required as shown in Fig. 2.7 [18].

When the transistor is ON, current flows through the inductor choke. At the transition time, when the transistor turns into OFF state, the current is driven into the capacitor increasing the drain voltage. When the switch is off, the current flowing into the drain is zero while the drain experiences a non-zero voltage. The switch can be activated when the voltage drops to zero, so that no switching losses occur. Such transition behavior is called soft switching or Zero Voltage Switching (ZVS) [19] [20]. ZVS not only ensures non-overlapping V/I waveforms, but also avoids charge loss when the switch turns on. In fact, Class-E amplifiers satisfy not only ZVS but also Zero Derivative Voltage Switching (ZDVS) , meaning the derivative of the voltage waveform at the time instant when the switch turns on is also zero [19] [20]. This property significantly reduces the efficiency sensitivity due to the passive component variations. A conventional Class-E implementation is shown in Fig. 2.7. A series LC filter is used to pass the fundamental frequency to the load impedance. As a result, the transistor sees inductive load impedance at the fundamental frequency while it only sees the parasitic drain capacitor at all harmonics. The derivation for the required tuning impedances, output power and efficiency of Class-E PAs are given in references [19] [20] as

$$P_{out}^{E} \simeq V_{DC} I_{DC} = \frac{1}{F_{PI}} V_{dd} I_{max} = \frac{1}{2.86} V_{dd} I_{max}, \tag{2.34}$$

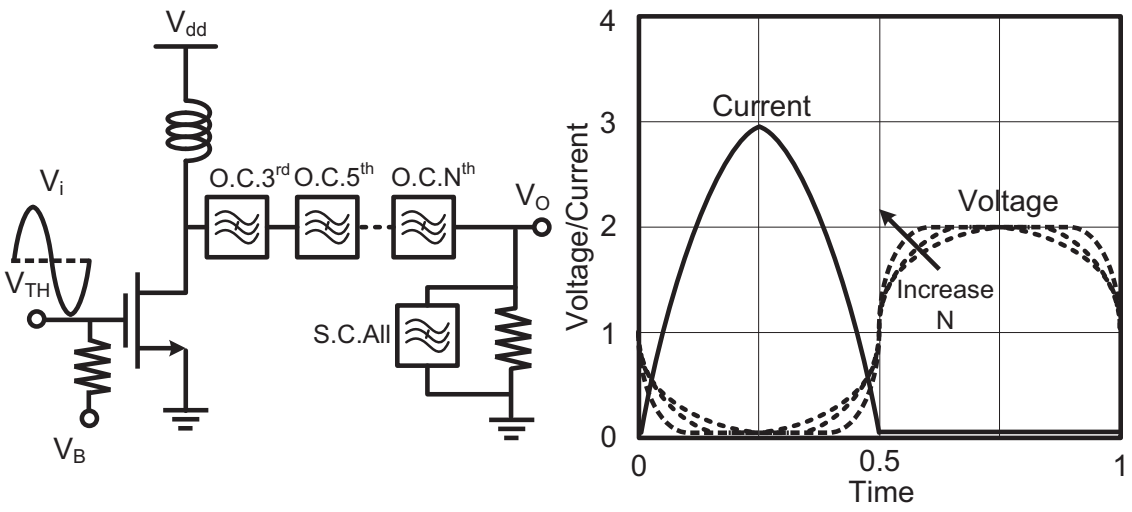


Figure 2.8: Schematics and V-I waveforms of Class-F amplifiers.

$$Z^E_{C,opt} = F_{PI}F_C\frac{V_{dd}}{I_{max}} = 8.98\frac{V_{dd}}{I_{max}}, \tag{2.35}$$

$$R^E_{opt} = 1.83Z^E_{C,opt} = 1.65\frac{V_{dd}}{I_{max}}, \tag{2.36}$$

$$X^E_{opt} = 1.15R^E_{opt} = 1.90\frac{V_{dd}}{I_{max}}, \tag{2.37}$$

$$F_{PI} = 2.86, F_C = \pi, \tag{2.38}$$

$$\eta^E_D = 100\%. \tag{2.39}$$

Although the hard switching problem is solved at the drain node, detecting such high frequency activating pulse at gate node is challenging at mmW frequencies because of the gate capacitance of the MOS devices. Moreover, the input resistance of RF MOSFETs at mmW frequencies is very small meaning that there is a power loss at the gate node and efficiency reduces. Recent advances in ultra deep sub-micron devices (e.g. 28nm CMOS technology) and developing process with extremely high f_T (e.g. 28 nm FD-SOI CMOS with $f_T = 300$ GHz) enables Class-E PAs as an alternative for mmW applications.

Class-F PAs were designed to achieve high efficiency performance by properly choosing the value of the output load at the fundamental frequency and its harmonics [21]. The output sees high and low impedances to the odd and even harmonics of the drain voltage respectively. Therefore, the drain voltage will be shaped from a sine to a square waveform. As a result, the overlap between V and I waveforms is reduced meaning that the efficiency is increased. The 100% efficiency can be achieved by increasing the number of harmonics. Circuit diagram and voltage/current waveforms of a Class-F PA is shown in Fig. 2.8. The Class-F PA is biased same as the Class-B PA in order to create the harmonics, so that the current waveform is a half rectified sinusoidal wave. In order to reject all the odd harmonics at the drain node, bank of filters with infinite number of resonators can be inserted in series at amplifier's output [21]. At the same time, a low-pass filter is required at the output to eliminate all the even order harmonics. When sufficient harmonics are added, the waveform resembles that of Class-D amplifiers. The output power, optimal impedance and efficiency of Class-F amplifiers are

$$P_{out}^{F} = \frac{1}{2} \times \frac{4}{\pi} V_{dd} \frac{1}{2} I_{max} = \frac{1}{\pi} V_{dd} I_{max}, \tag{2.40}$$

$$R_{opt}^{F} = \frac{V_{pp}}{I_{pp}} = \frac{8}{\pi} \frac{V_{dd}}{I_{max}}, \tag{2.41}$$

$$\eta_{D}^{F} = \frac{V_{pp} I_{pp}}{2 V_{DC} I_{DC}} \simeq \frac{\frac{1}{\pi} V_{dd} I_{max}}{V_{dd} \frac{1}{\pi} I_{max}} = 100\%. \tag{2.42}$$

The idea of using Class-F amplifiers suffers from implementation issues at mmW frequencies. Similar to Class-D amplifiers, the efficiency of Class-F amplifiers is also degraded by the parasitic capacitance at the transistor's drain node. In addition, implementation of large number of filters with low quality factor (Q) of the mmW integrated inductors and capacitors cannot be realized without excessively degrading the PA efficiency.

2.2 Power Match vs. Gain Match

Satisfying the maximum power transfer conditions, the load resistor must be equal to the real part of the output impedance of the amplifier [17]. For the matched

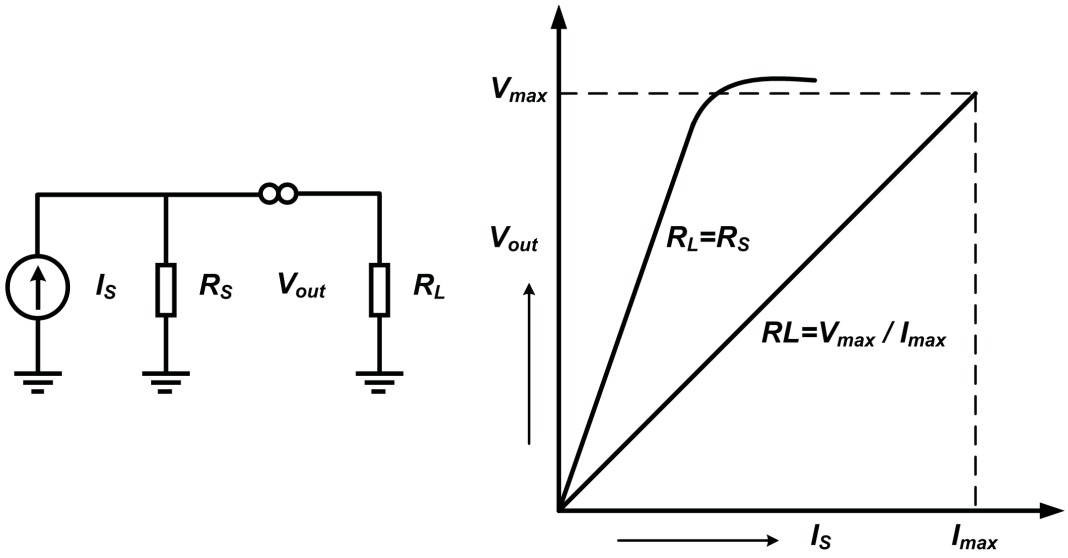


Figure 2.9: Non-ideal current source and the load lines.

condition analysis, it is assumed that any reactive component of the impedance has been reduced to zero. Although the max power condition seems to be satisfied, there is still an item not considered here: the difference between an ideal current source and a transistor-based current generator. There will always be a power limit due to the maximum current that a transistor can produce and the maximum voltage it can sustain across its terminals. For instance, consider a current generator that can supply a maximum current of 1 A and has an output resistance of 100 Ω (Fig.2.9). By applying the conjugate match theorem, a load of 100 Ω must be selected for maximum power transfer [17]. The voltage due to the driven current would be 50 V. The transistor voltage will be limited by the DC power supply which is typically less than 5 V for modern silicon technologies. To utilize the maximum voltage and current of the transistor, a lower load resistance, called optimum resistance R_{opt}, would need to be selected. The value of the R_{opt} can be found using the load line match technique [16]. For a comparable source resistance, R_{opt} is given by

$$\frac{R_{opt} + R_s}{R_{opt} \times R_s} = \frac{V_{max}}{I_{max}}. \tag{2.43}$$

The example stated above demonstrates the main concept of the matching technique used for PA design. For a practical transistor-based power amplifier, the load-pull technique of power match is developed based on the load line theory [16]. "The

maximum linear RF power or the so called 1 dB compression point (P_{1dB}) achieved by load-pull matching is always 2 dB greater than the one obtained by a simple conjugate gain match" [16].

2.3 Literature Review on 60 GHz PAs

Over the last two decades, mmW power amplifiers in Galium-Arsenide (GaAs) , Indium-Phosphide (Inp) , Silicon-Germanium (SiGe), and silicon CMOS technologies are reported and listed in Table. 2.1. Although, the typical figure-of-merit (FoM) is proposed by ITRS [7], by taking account the area used in this comparison table, we can emphasis the cost of implementation in FoM as

$$FoM = \frac{G_p \times P_{sat} \times PAE_{max} \times f_c}{Area}, \tag{2.44}$$

where, P_{sat} is the saturated or maximum power in Watts, G_P is the linear power gain, PAE_{max} is the maximum power added efficiency in percent, f_c is the center frequency in GHz and $Area$ is the total chip area. In addition, linearity is another important parameter which can be measured by P_{1dB}. Also, the chip area and bandwidth are important parameters which determine the fabrication cost and data-rate respectively.

Traditionally, GaAs and Inp-based High Electron Mobility Transistors (HEMT) have been the premier FET devices for mmW applications because of the higher electron mobility and the higher cutoff frequency (f_T) compared to silicon devices. On the other hand, silicon devices have been considered as low-gain low-frequency devices that could not compete with III-V HEMTs at mmW frequencies. High level of output power with high PAE have been achieved using HEMT and GaAs devices on very large occupied die area [22–36]. However, one major drawback of using GaAs is the high thermal resistance that limits the maximum power in a defined area [24]. Increased fabrication cost and integration issues are two of the major drawbacks of designing PAs in III-V technologies. Therefore, PAs designed in these technologies had been usually used for high performance military applications and satellite-to-satellite communications in the nineteens.

With continuation of advancements in device scaling, SiGe Heterojuction Bipolar Transistors (HBT) devices have achieved cutoff frequencies as high as 200 GHz which makes SiGe an ideal technology for mmW wireless communication systems [37–48].

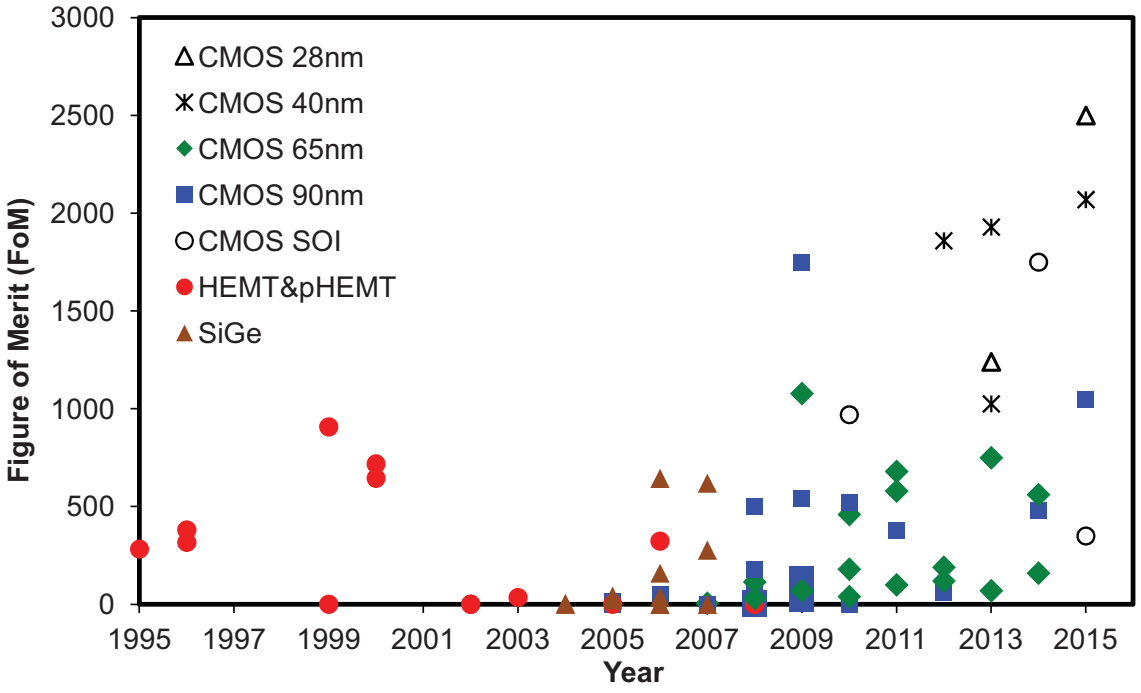


Figure 2.10: Development of the 60 GHz PAs.

SiGe technology offers lower manufacturing costs as well as lower power consumption compared to III-V technologies [48]. Compared with silicon MOSFETs, SiGe transistors offer higher cutoff frequency ($f_T > 200$ GHz). However, CMOS typically requires less masking steps than the SiGe for a given technology node which results in lower wafer costs and faster manufacturing cycle times.

With recent advances in ultra-deep submicron CMOS technologies, the design of low-cost highly integrated mmW PAs is possible in silicon technology [49–81]. Very high cutoff frequency ($f_T > 150$ GHz) is achievable with modern CMOS devices which enables the mmW RF front-ends being integrated with the low power baseband. Since 2007, most of the reported 60 GHz PAs were designed in CMOS (Fig. 2.10). CMOS PAs are promising candidates for 60 GHz applications because of the very high reported FoM compared to other technologies.

Table 2.1: Literature review on 60 GHz power amplifiers.

Process	Tech [nm]	Freq. [GHz]	B.W. [GHz]	Stages	Mode	Topology	Combiner	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	P_{DC} [mW]	Size [mm^2]	FoM	Ref.
GaAs pHEMT	100	60	-	2	s	cs	2x	24.3	24	12.0	24	-	5.46	283	[22]
		60	-	2	b	cs	-	9.5	7.5	12.8	-	-	7.6	-	[22]
		62	9	2	b	cs	-	27.5	25	13.0	21	-	10.4	322	[24]
		62	-	2	s	cs	-	24.7	23	13.5	26	-	7.0	324	[24]
	150	60	20	3	s	cs	-	12.5	9.0	18	-	-	6	-	[25]
		50	7	3	s	cs	-	16	14	15.5	-	-	3	-	[26]
		60	15	3	s	cs	-	16	15	12		525	4.25	13	[27]
		60	9	3	s	cs	2x	15	16	12	-	-	2.2	-	[28]
		60	5	2	s	cs	-	25	23	18	27	-	10.7	382	[29]
		60	6	3	s	cs	2x	19	17	13.4	7.3	975	4.5	36	[30]
		60	-	1	s	cs	-	16	15	8.0	-	-	2	-	[31]
		60	-	2	s	cs	-	16	15	15	-	-	2.5	-	[31]
InP HEMT	100	60	15	1	s	cs	-	23.5	23	10.5	43	-	3	645	[32]
	120	60	7.0	2	s	cs	-	24	22	10	43	-	2.9	79	[33]
	150	62	5.0	2	s	cs	-	30	29	20	21	-	-	-	[34]
		95	16	2	d	cs	-	26.3	24	12	20	-	3.6	909	[35]
SiGe	120	61	-	2	d	ce	-	16.2	11.2	10.8	4.3	375	1.7	23	[37]
		77	5.0	2	s	cas	-	14.4	12	19	15.7	161	-	-	[38]
		77	15	4	s	ce	2x	17.5	14.5	17	12.8	405	0.61	646	[39]
	130	58	-	1	s	ce	-	11.5	-	4.2	20.9	-	-	-	[40]
		60	7	1	d	cas	-	20	13.1	18	12.7	240	0.98	621	[41]
		61	5	1	d	cas	-	17	10.5	15	10	288	-	-	[42]
		61	-	1	d	cas	-	14	8.5	12	4.2	264	0.63	41	[43]
		77	-	2	d	ce	-	12.5	11.6	6.1	3.5	325	1.6	6	[44]
		85	20	8	s	cas	4x	21	-	8.0	3.4	-	2.4	38	[45]
		60	5	1	d	cas	4x	23	21.5	22	6.3	1200	3.4	278	[46]
	180	60	-	3	b	ce	-	15.8	11.2	11.5	16.8	281	0.9	160	[47]
	200	77	-	1	d	cas	-	18.5	-	-	5.4	-	-	-	[48]

Table 2.1: Literature review on 60 GHz PAs— Continued.

Process	Tech [nm]	Freq. [GHz]	B.W. [GHz]	Stages	Mode	Topology	Combiner	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	P_{DC} [mW]	Size [mm^2]	FoM	Ref.
CMOS	130	60	6	3	s	cas	-	-	2	12	2.7	54	1.3	-	[77]
		60	7	5	s	cas	-	7.8	7.0	13.5	3	-	1.8	2.8	[78]
	90	60	12	3	s	cs	-	9.3	6.4	5.2	7.4	39.75	0.15	45	[62]
		60	22	2	d	cs	-	12.3	9	5.5	8.8	-	0.25	67	[63]
		60	-	4	s	cs	2x	10.6	8.2	8.3	2.35	228	0.98	4.5	[64]
		60	4	3	s	cs	2x	11.0	10	14.3	8.2	150	0.18	178	[65]
		60	8	4	d	cs	-	12	10.2	15	14	84	0.15	499	[67]
		51	-	3	s	cas	-	8.2	3.1	19.5	4.2	150	1.13	12	[68]
		60	12	2	s	cs	2x	11.6	10.1	8.2	11.5	81	1.03	25	[69]
		60	8	4	s	cs	2x	12	8.2	20	9.0	146	0.65	132	[70]
		60	16	3	s	cas	4x	14.5	10.5	26	10.2	286	0.64	538	[71]
		60	20	3	s	cas	-	13.8	10.3	30	12.6	180	0.33	1738	[72]
		60	8	4	s	cs	4x	20	18	20.6	14.2	-	1.8	519	[73]
		61	8	2	s	cas	-	8.4	5.1	17	5.8	54	-	-	[74]
		62	5	2	s	cs	-	-	4	12.2	24	10.4	0.48	-	[75]
		70	70	2	s	cas	-	10	8	7	6.14	122	0.72	13	[76]
		77	17	4	s	cs	2x	6.3	4.7	8.5	1.7	142	0.98	1.5	[63]
	65	60	20	3	s	cs	-	7	1.5	13	2.4	125	0.6	5	[50]
		60	8	2	s	cs	-	13	8.9	8	11	64.8	0.29	114	[51]
		60	8	3	d	cs	-	11.5	2.5	15.8	11	43.5	0.05	1078	[52]
		60	10	2	d	cs	4x	17.9	15.4	18.8	11.7	460	0.83	457	[52]
		60	15	2	b	cas	8x	18.1	11.5	15.5	3.6	1504	0.46	180	[54]
		62	10	1	s	cs	-	9	6	4.5	9	27.6	0.27	27	[56]
		58	-	4	s	cs	-	13.8	12.2	13.4	7.6	300	1.28	39	[57]
		61	5	3	d	cs	-	11	-	15	-	138	-	-	[58]
		60	8	2	s	cs	-	10.6	9.2	13.2	8.9	80	0.29	97	[59]
		60	6	3	d	cs	-	14.6	10	23.2	16.3	135	0.6	680	[60]
		60	6	3	s	cs	2x	17.8	13.8	11	12.6	-	0.28	577	[61]
	40	60	5.5	3	d	cs	2x	17.4	14	21.2	28.5	150	0.56	1927	[82]
		60	12	3	d	cs	2x	19.6	16.2	20.3	18.3	-	0.5	2073	[83]
	28	60	11	3	d	cas	-	16.5	11.7	24.4	12.6	-	0.12	1219	[84]

Meanwhile, the Silicon-On-Insulator (SOI) CMOS technology is designed specifically to reduce the power losses by offering a highly resistive substrate. Compared to bulk CMOS, SOI technology significantly reduces junction capacitance that allows transistors to operate at higher frequencies and consume substantially lower power. In addition to this, the latch-up problem of bulk CMOS technology is eliminated in SOI because transistors are isolated from each other using dielectric and from the underlying substrate. Higher efficient PAs with the ability to reduce operating voltage and power loss without compromising the RF performance are designed in CMOS SOI technology. The SOI technology is considered to be an alternate as the current deep submicron CMOS devices on bulk silicon reached the physical limit in controlling the leakage currents [85]. Although CMOS technology is the most cost effective available process, achieving maximum output power near the cutoff frequency of CMOS devices imposes a challenge for the designers. The maximum achieved output power by 60 GHz CMOS PAs are still less than 20 dBm (100 mW) which is much lower than the allowable power assigned by FCC. To satisfy the power, efficiency and linearity specifications at mmW frequencies, 60 GHz CMOS PAs in different topologies have been proposed.

A common source (CS) stage, single-ended (s) PA implemented in 65 nm CMOS technology is the simplest topology and has been used in references [49–51, 56]. The schematic of the single stage common source PA core designed in CMOS technology is illustrated in Fig. 2.11. Transmission lines (TL) have been used for impedance matching and DC bias purposes.

The amplifier could achieve a peak power gain of 4.5 dB with 1 dB compression and saturation output power levels of +6 dBm and +9 dBm, respectively, with peak PAE of 8.5% [56]. A Transistor with a large channel width is used to achieve high current as a power device. Measured results proves the low efficiency and low gain of single MOSFET devices with large channel width. Meanwhile, utilizing area inefficient transmission lines to match the impedances is the other source of loss which degrades the efficiency of the PA dramatically.

In an attempt to achieve high output power with high gain, the multi-stage cascaded topology was developed as shown in Fig. 2.12. The design was implemented in 65 nm, and 90 nm bulk CMOS technologies. Four cascaded Class-A stages with common source topologies were designed to achieve 13.4 dB of power gain. The f_T/f_{max}

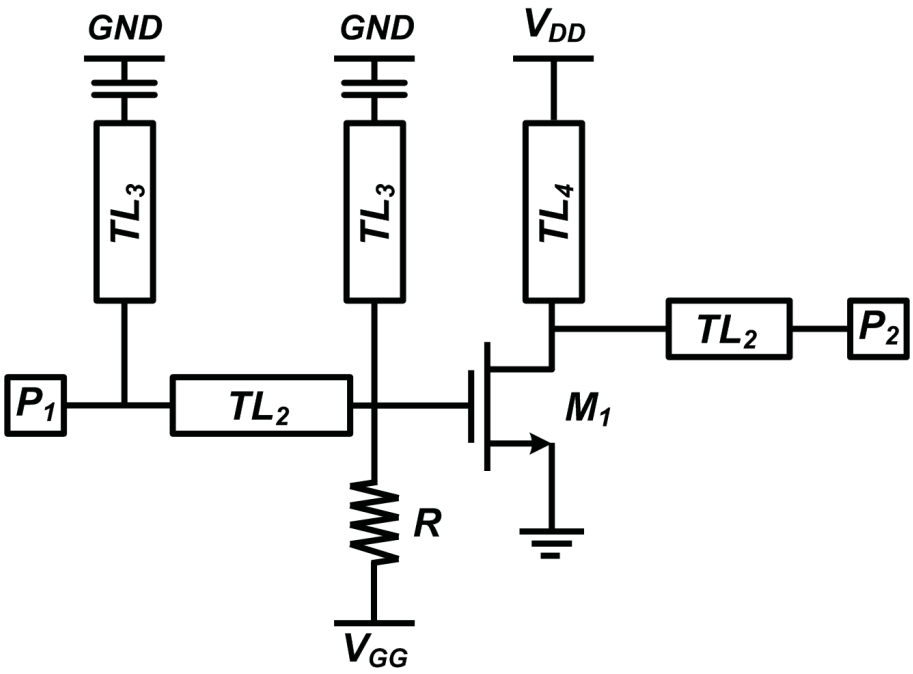


Figure 2.11: Single stage CS transmission-line based PA.

of the technology were reported to be 160/200 GHz. Power MOSFET with channel width of 180 μm in a singe-ended topology could deliver the maximum output power of 13.8 dBm to a 50Ω load. the PAE of the whole PA is still 7% because of the large number of transmission lines used for inter-stage matching purposes. However, cascaded driver stages consume DC power to provide desired power gain. Although number of driver stages increase the gain, the output RF power is delivered only by the last stage. On the other hand, cascading number of stages reduces the overall PAE practically.

The gain compression is a phenomenon which is caused by non-linearity and it is very critical to be considered in cascaded PAs. When operating within the linear region of amplification, gain through the amplifier stages must be constant for a given frequency. As the input signal is increased in power, a point is reached where the power of the signal at the output is not amplified by the same amount as the smaller signal. At the point where the input signal is amplified by an amount 1 dB less than the small-signal gain, the 1 dB compression point has been reached. A rapid decrease in gain will be experienced after the 1 dB compression point is reached. If the input power is increased to an extreme value, the amplifier will be destroyed. In a

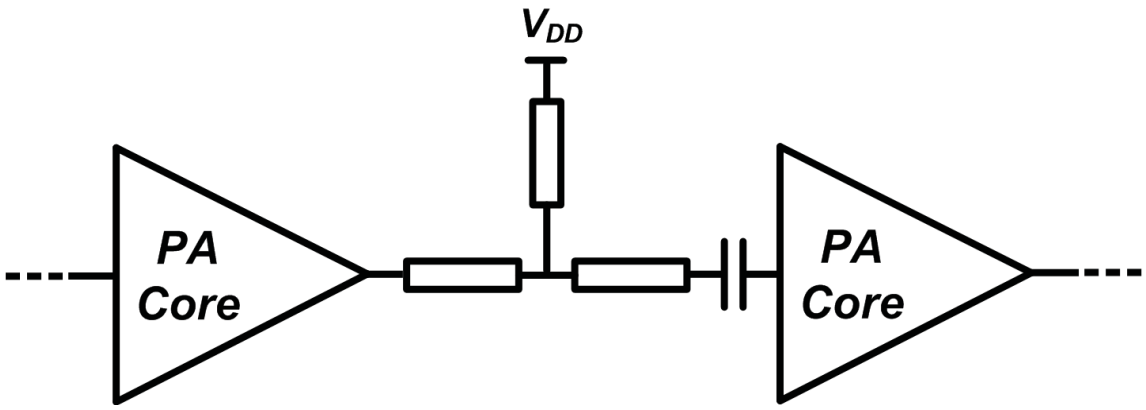


Figure 2.12: Topology of cascaded PAs with TL inter-stage matching.

cascaded topology it is very important to keep the driver and gain stages away from the compression, results in effectively high 1 dB compression point at the last stage. The channel width of transistors are increased linearly after designing each stage to ensure a high linearity of the power amplifier, while at least 4 dB of gain is added per stage. Single-ended amplifiers suffer from early compression because transistors are directly driven by a high input power. The power amplifier reported by [64] uses ring inductors extensively instead of transmission lines to achieve a power gain of 5.2 dB with a 1 dB compression point of +6.4 dBm and a saturation output power level of +9.3 dBm with a peak PAE of 7% [64].

The cascade technique is utilized by [74] in a 3-stage wide-band power amplifier implemented in 90 nm CMOS. One advantage of cascading technique is the feasibility of a wide-band design. The gain and driver stages are designed to achieve maximum gain at different center frequencies. As a result, the cascaded structure achieves a flat gain over a wide range of frequencies. Using a high supply voltage of 1.8 V, higher gain and power are obtained compared to the same reported designs in Table 2.1. Other technique includes TL-based matching circuits to achieve a wide bandwidth [74].

Achieving higher small-signal gain, the cascode (cas) topology has been used in amplifiers due to its higher output resistance [70–74]. A three stage cascade power amplifier in 90 nm bulk CMOS was presented in [70]. The main PA core is based on the cascode topology for all three stages. High power gain in this amplifier is also achieved by increasing the supply voltage up to 2 V. The prime objective of the design was to benchmark the 90 nm CMOS technology and its design kit in mmW application that could be used to further improve computer simulation models and

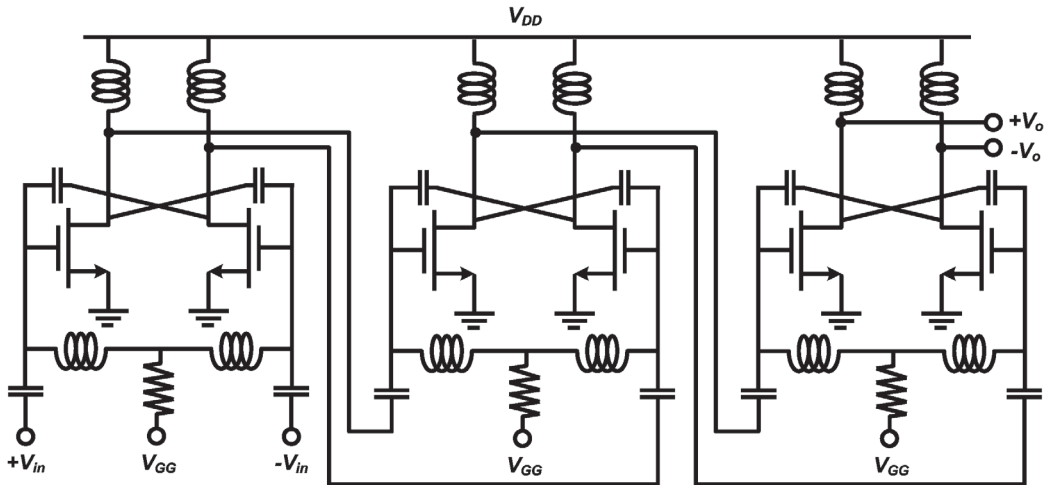


Figure 2.13: Cascaded differential stages with simple π section inter-stage matching.

identify potential problems in the design flow [70]. Also, the results obtained for this mmW PA prototype do not completely agree with the simulations, indicating that the proper extraction of capacitive parasitics from the physical layout is necessary to obtain a robust design [70].

Differential CS stages are one of the common solutions to increase the voltage swing at the output. A differential PA is presented with MOS capacitors as a cross connected feedback to achieve better stability conditions. Fig. 2.13 shows the cascaded differential stages proposed by [81]. Each transistor experiences half of the input power which leads to a wider range of gain compression. Using cascode structures should be avoided here due to disadvantages of reduced headroom voltage and drain efficiency. LC resonant π section interstage matching is utilized to cascade three differential stages. Extensive use of passive elements in a ladder configuration is one of the major source of loss at mmW frequencies which can degrade the efficiency of the whole amplifier. The power amplifier achieves a power gain of 15 dB and a maximum output power of 11 dBm at 60 GHz.

While increasing the number of active stages can increase the overall power gain, the output power level is determined by the last stage. Since the last stage gain should not be made less than unity, the power gain - output power tradeoff plays a fundamental role in determining the size of the output stage, and thus puts an upper limit on the maximum output power that can be delivered from a single unit amplifier. Combining the power from a number of unit amplifiers is proposed as

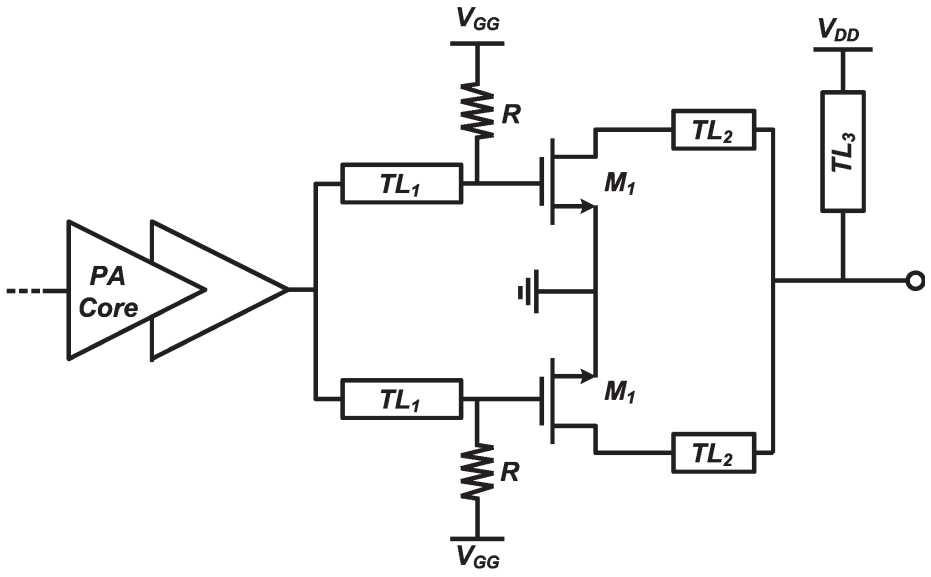


Figure 2.14: Transmission line based parallel power combining topology.

a solution to achieving considerably higher output power levels. The multi-stage amplifiers implemented in 90 nm bulk CMOS and presented in [67, 68] use two maximum size transistors in parallel in the last stage. By the use of Wilkinson power splitter/combiner the first PA delivers 1dB compression and saturation output power levels of +10.5 dBm and +11.3 dBm respectively whereas the second PA provides power gain of 8 dB and delivers 1dB compression and saturation output power levels of +8.2 dBm and +10.6 dBm respectively. The Wilkinson power combining topology used in a cascaded PA is shown in Fig. 2.14. Large size transistors exhibit low gain characteristics due to the added parasitic losses in the gate and drain networks. Thus, in order to obtain high gain from the overall amplifier, more than two stages are needed in this topology. Wilkinson power combiners are not area efficient due to long transmission lines [71]. In order to optimize the output power, power gain, and efficiency of the amplifier, the output power from two unit amplifiers each employing a maximum size transistor at the output stage can be combined using on-chip transformer based power combiners.

Fully integrated two-way 60 GHz transformer-coupled differential power amplifiers were implemented in 90 nm standard CMOS [65]. Transformers are interested as they can simultaneously perform impedance transformation and differential-to-single-ended conversion in a compact die area. In a multistage design, they also provide

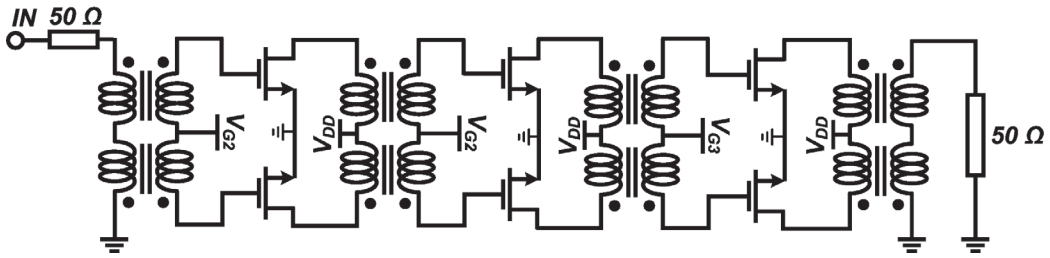


Figure 2.15: Transformer based inter-stage matching and differential power combineing.

easy DC biasing through the center-taps. Fig. 2.15 shows the basic idea behind the transformer based PA. Implemented PA in 90 nm CMOS, could achieve +12.3 dBm RF power over a 1V supply voltage. Since 2008, circuit techniques have been proposed to optimize the transformer-based PAs in terms of efficiency, bandwidth and output power. A neutralized differential CMOS PA implemented in 65 nm is reported by [66]. Higher power gain and reverse isolation are achieved here using differential topology and cross connected miller capacitors. Shielded transformers couple the gain and allow low supply voltage operations. Over a 1V supply voltage, three stage PA achieved +11.5 dBm power and PAE is improved to 15.2% thanks to the low-loss spiral stacked transformers.

A two stage transformer coupled PA has been designed and reported with such a high output power in [86]. A comprehensive distributed model of on-chip transformers has been developed. Due to parasitic components and different loss mechanisms, the impedance transformation ratio is highly frequency and size-dependent. Hence, the paper aims to optimize the size of the transformer at a given frequency and load resistance. For very small sizes, the impedance of the shunt magnetizing inductance becomes too small and most of the signal current is lost through it. A large transformer, on the other hand, results in higher substrate losses and an increased series leakage inductance which also reduces the signal transfer to the secondary winding.

While using on-chip transformers for combining the output power of two unit PAs results in a relatively small occupied area, this technique has two main disadvantages. First, as the transformer maximum gain is less than unity, power combining through the transformers can result in power loss and thus reduced output power levels and drain efficiency. Second, while combining the output power from two unit amplifiers using transformers is relatively easy, combining the output power from a

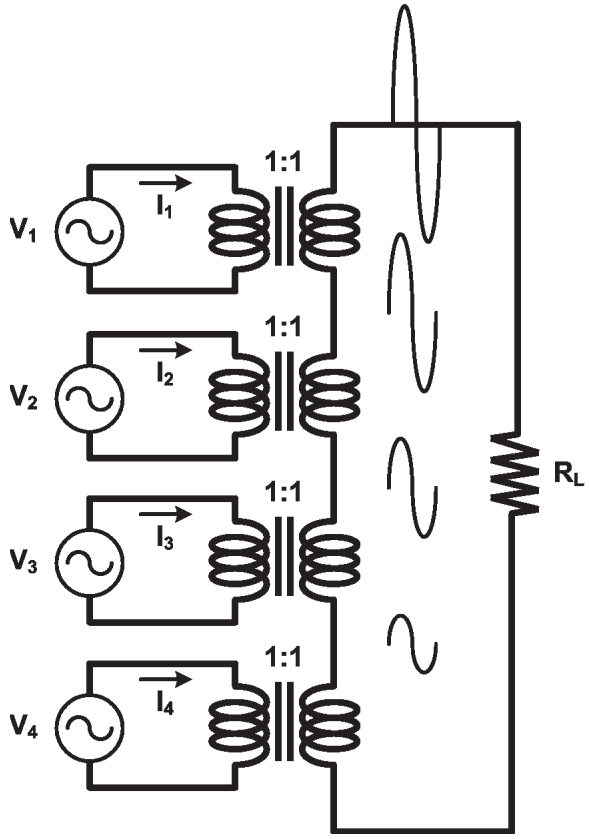


Figure 2.16: Transformer based 4-way series power combining topology.

larger number of unit amplifiers in order to provide even higher output power levels becomes increasingly more difficult. This could be more challenging when high efficiency transformers are required because the insertion loss of a transformer depends on the physical size of the windings. Also, increasing number of PA units require a large DC biasing network which introduce additional loss to the circuit. Designing such complex network is challenging due to physical layout problems as the coupling between RF and DC feed-lines increases. A new approach for PA design in deep submicron CMOS has been proposed by [87] to improve the output power. A transformer based voltage combiner has been proposed to combine power generated from several low-voltage CMOS amplifiers. Unlike other voltage combining transformers, the architecture presented in this paper provides greater flexibility to access and control the individual amplifiers in a voltage combined amplifier.

Fig. 2.16 shows the main idea of the proposed combining technique. An ideal four-way power combined linear amplifier is used here to demonstrate the concept. It is

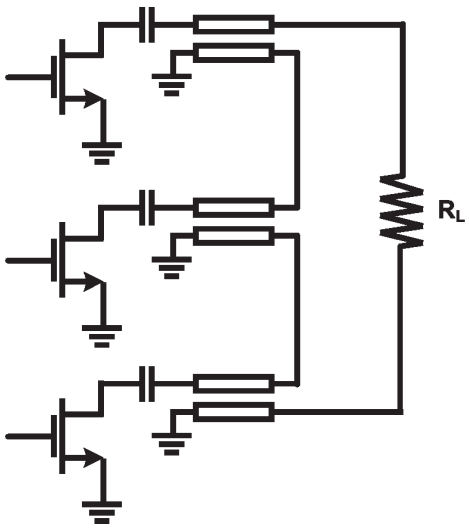


Figure 2.17: Coupled transmission line based series power combining topology.

known that both output power and DC power of an ideal linear amplifier are inversely proportional to the load R_L. The transformer will transform the load impedance to a lower value seen by each unit amplifier at the primaries and combine power generated from each unit amplifier at the secondary, using stacked 1:1 transformers. The primary sides of the four independent unity transformers are driven by four independent but synchronized sources with the same signal level in parallel. At 60 GHz and beyond, it becomes feasible to integrate TL-based power combiners in CMOS. Hence, another approach to realize an N-to-1 combination is using a TL-based combiner as shown in Fig. 2.17 [88].

A series-parallel power combining topology is shown in Fig. 2.18. Utilizing both parallel and series combining, electrically each port is identical even with unwanted parasitics [51]. A maximum PAE of 12 with P_{sat} of 17.9 dBm is achieved using four differential stages as PA core on each side. By the use of new planar transformer configuration, high quality and coupling factors is achieved. The planar transformers designed by slab inductors are being widely used by the references due to their higher quality factor and simple configuration.

One of the critical issues for CMOS PA design are the low breakdown voltage and higher knee voltage of the devices compared to other semiconductor technologies, which limits the allowable drain voltage swing. Break-down and degradation mechanism in submicron CMOS include gate-oxide breakdown, hot carrier degradation, punch-through and drain-bulk breakdown [89]. One of the earliest proposed

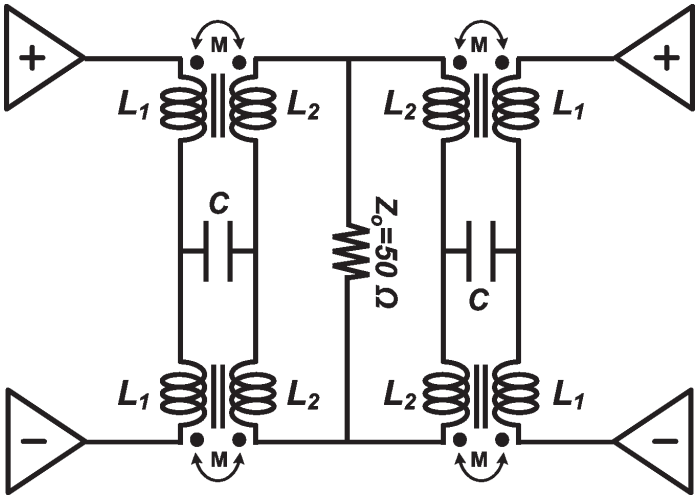


Figure 2.18: Series-parallel transformer based power combining topology.

techniques to overcome the breakdown challenge is combining multiple transistors in series. The so-called beanstalk amplifier proposed by K.J. Dean in 1964 [90]. Shown in Fig. 2.19, several MOS transistors connected in series such that the voltage stress is divided across all devices.

Analysis and design of stacked-FET mmW PA in CMOS technology have been discussed and reviewed by [91]. Design of stacked-FETs with multiple stages are formulated in terms of efficiency and intermediate nodes matching methods are discussed. Measured at 47 GHz, the stacked-FET amplifiers could achieve high PAE of 25% to 32.7% by changing the supply voltage from 5V to 2.5V. Although the amplifier could achieve 21 dBm output power from 5V supply, the measured 15.9 dBm output power from 2.5V supply is very low, compared to today's CMOS designs. A 60GHz triple-stacked FET PA is implemented using 0.13 μm HEMT [92]. Input power is divided into series stacked-FETs using wilkinson parallel combiner. A maximum output power of 20 dBm is achieved with a high PAE of 19%. Measured wide band width of 15 GHz demonstrates that the design is promising for broadband 60 GHz applications.

A mmW PA designed in 45 nm SOI CMOS proposed multi-drive stacked-FET as an alternative to passive power combining technique [93]. The gate resistance of the stacked-FET PA is demonstrated to be a dominant source of loss at high frequency, and the proposed PA minimizes this effect. Pre-amplifiers with tranmission line based interstage matching networks are used to increase the overall gain. Measured at 90

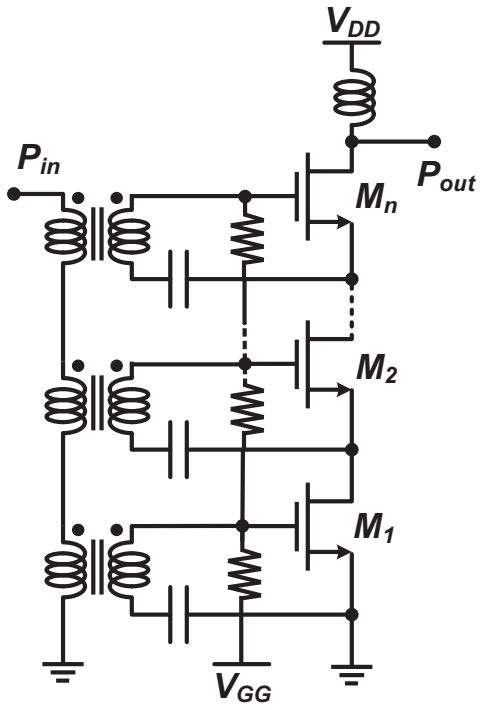


Figure 2.19: Circuit topology of a stacked-FET PA.

GHz, 19 dBm saturated output power and 14% peak PAE from a 3.4V power supply. Measured results demonstrates 2dB increment in gain and 4% more PAE compared to the conventional technique in the same CMOS technology.

The stacked-FET technique, however, has various disadvantages to be widely used in CMOS technology. It is only suitable for low-frequency or high voltage applications since the input signal has to propagate up to the gates of all stacked devices so the devices are not well synchronized to add up in phase, degrading the output power, efficiency, and linearity. The gate and drain bias voltages shall be increased as the number of stages increases which is not suitable for today's low power applications. Moreover, number of transistors stacked in series is susceptible to be used in bulk CMOS technology because of the process variations, supply sensitivity and substrate conductivity [94]. As the frequency increases, the gain of each transistors falls because of the gate-source and drain-source capacitances. In stacked topology, at mmW frequencies, the junction capacitor created at the drain-source between each stages creates a dominant pole which degrades the gain and output impedance of the stacked devices dramatically.

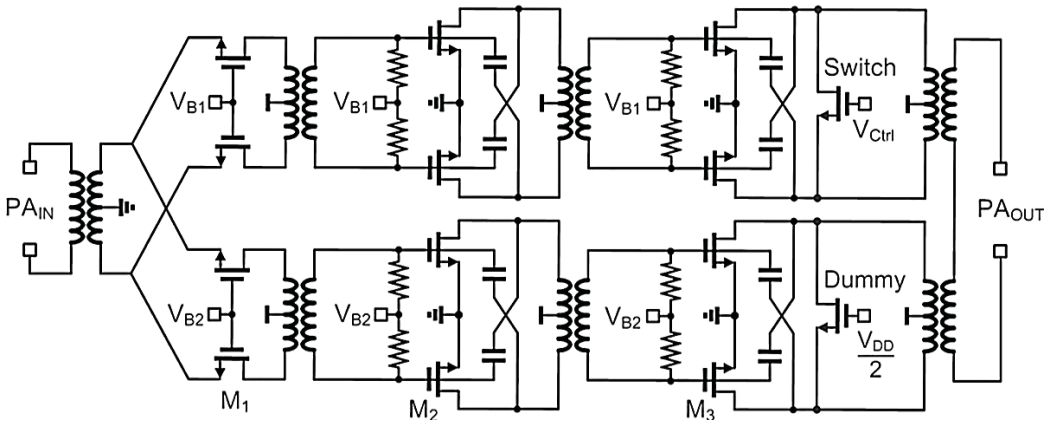


Figure 2.20: Simplified schematic of the dual-mode PA topology.

The most recent advanced circuit technique in 60 GHz PAs is using the dual-mode configuration to take the advantages of operating at highest possible PAE and achieving maximum output power [82]. Fig. 2.20 demonstrates the basic idea of the dual-mode PA proposed by [82]. Input transformer splits the power into two individual rails, where each unit PA consists of differential common-source output and driver stages and a common-gate (CG) input stage. The neutralization technique is utilized in the output and driver stages to improve the gain, stability and reverse-isolation. The driver and input stages are sized down by a factor of two progressively to deliver sufficient driving power and not to saturate prior to the output stage. A transformer-based power combiner combines the differential outputs from the two unit PAs and provides the impedance transformation simultaneously. A switch is placed on the second unit to basically turn off one of the units during the low power mode. When higher power needed, the second unit can share the power by changing the state of the switch. Fabricated in 40 nm CMOS, the dual-mode PA could provide maximum output power of 17.4 dBm to a differential load. The peak PAE of 30% is the maximum reported PAE in CMOS technology.

2.4 Summary of PA Design Challenges at 60 GHz

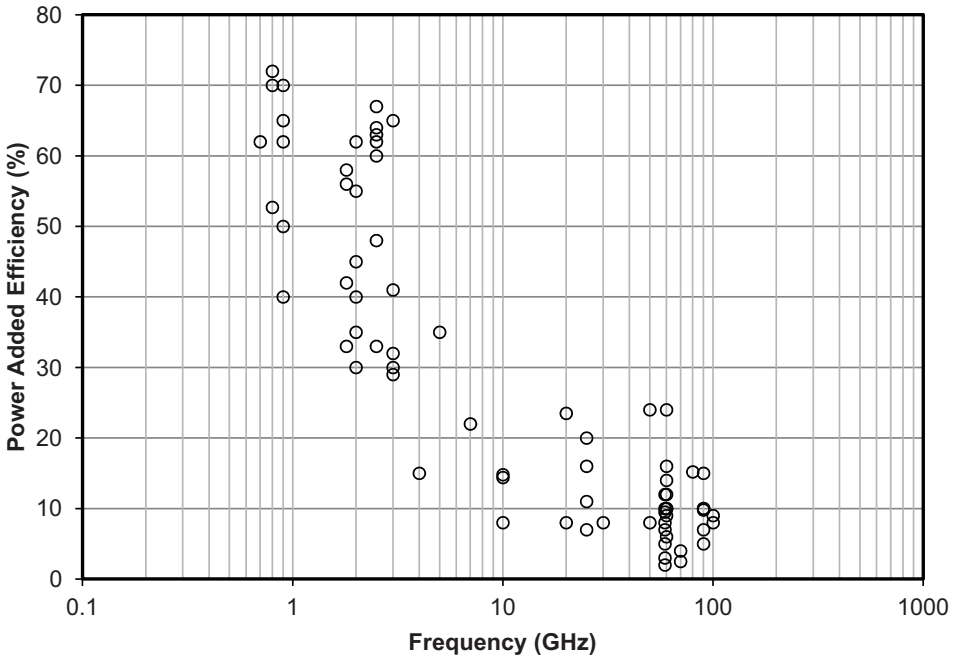
Although the operating frequency of transistors has been improved with recent CMOS technology scaling, design of CMOS PAs at mmW frequencies still face many challenges. Fig. 2.21 shows a performance survey of the state-of-the-art CMOS PA over a wide frequency range. Achieved PAE and output power are investigated as major evaluation metrics. It can be observed that the output power and efficiency drop with increasing the operating frequency. Multiple reasons can be emphasized to explain this phenomenon. The main factor that contributes to the reduced efficiency at high frequency is the reduced transistor power gain. For linear amplifiers, the drain efficiency of mmW PA is comparable to their low frequency counterpart, however, since the Maximum Stable Gain (MSG) drops with increasing frequency, more power is needed to drive the PA. This reduces the PAE as it is inversely proportional to the input power. At 60 GHz for example, a single stage PA can only provide 5-6 dB power gain after including the passive loss. According to (2.3), the PAE can be much lower than the drain efficiency due to the low power gain. Driver stages are usually used to boost the overall gain of the PA chain, but cascading gain stages do not affect the PAE theoretically as shown in (2.6). In practice, adding driver stages could improve the overall PAE since the drive stages are impedance matched for maximum gain, but they consume DC power to provide gain which must be considered when calculating the overall efficiency.

In order to overcome the power gain challenge of single MOSFETs, channel length of devices are scaled down and therefore the f_T increases in modern CMOS technologies. Although technology scaling could increase the operation frequency, the supply voltage and breakdown voltage reduces dramatically because of shrinking the thin oxide layers. Assuming oxide breakdown voltage of 15 MV/cm, a technology with thin oxide thickness in the order of 1 nm can handle the breakdown voltage around 1 V. Hence, the supply voltage must be reduced in modern technologies. This can directly affect the maximum available output power as it is proportional to the voltage square.

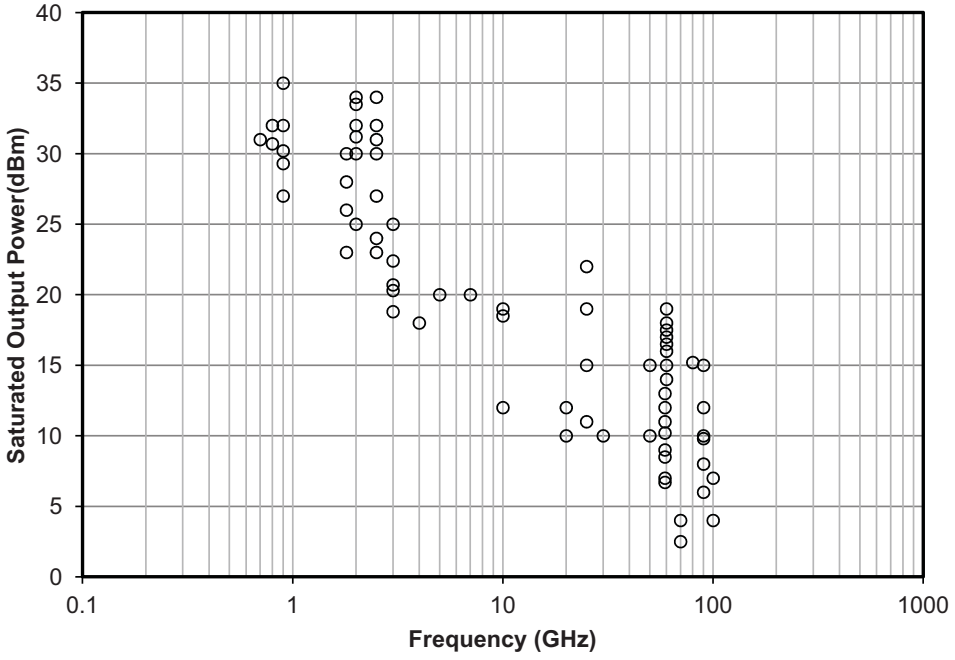
Power transistors must be biased at very high current densities to overcome the supply voltage reduction and therefore they presents smaller load impedance. As a result, a high Impedance Transformation Ratio (ITR) is required to match the output impedance of PAs. Technology scaling shrinks the metal layer thickness as well as the

oxide thickness. This reduces the distance between signal path and the conductive silicon substrate and therefore, insertion loss of on-chip impedance tuning circuits increases with increasing the ITR . In another word, larger output power results in higher loss in matching circuits and lower efficiency.

Another consequence of shrinking metal layers is low quality factor of passive components at high frequencies. TL-based or transformer-based structures are extensively used passive components to combine the output power of multiple PA cells. They are inseparable part of the inter-stage matching circuits and DC biasing networks. It can be shown that the maximum obtainable power transfer efficiency of on-chip passive circuits is proportional to the square of the Q factor. Hence, another important factor which determines the overall performance of the PA (PAE, G_p and P_{sat}) is the efficiency of power combiners and matching circuits. Accordingly, new topology power combiners with low insertion loss are desired to improve the performance of PAs.



(a)



(b)

Figure 2.21: Review on CMOS power amplifier performance, (a) power added efficiency (b) maximum saturated output power.

Chapter 3

Multi-Conductor Power Combined 60 GHz PA

As discussed in previous chapter, the main challenge in the design of 60 GHz PAs is to obtain a high-level of P_{sat} using CMOS transistors with relatively low gain at 60 GHz. Common approaches to improve the P_{sat} and PAE of 60 GHz PAs are to combine the output powers of several single-stage PAs using power combiners. In addition, to obtain the desired overall power gain, each single-stage PA must be preceded by a single gain stage or multiple cascaded gain stages. However, the necessity of multi-stage amplification introduces extra power dissipation because of the biasing power consumption and losses of the passive inter-stage impedance matching networks. Therefore, it is desired to develop new layout or circuit design techniques capable of power combining of multiple cascaded stags with minimum loss for designing 60 GHz PAs with high power, gain and PAE .

A 60 GHz PA topology using a new multi-conductor power combiner is presented in this chapter. Design flow process of 60 GHz PAs consists characterization and optimization of active device and passive components before designing the PA. Power MOSFETs with large channel width are characterized at mmW highlighting the high frequency design challenges. Various impedance matching networks and power combining networks are analyzed using proposed mmW circuit models and compared based on the power transfer efficiency. A new compact layout topology for power combining approach for integrated mmW PAs and compares its power efficiency with those of the conventional structures. Design process of the proposed 60 GHz fully integrated power amplifier in a standard 9 metal layer 65 nm CMOS process is de-

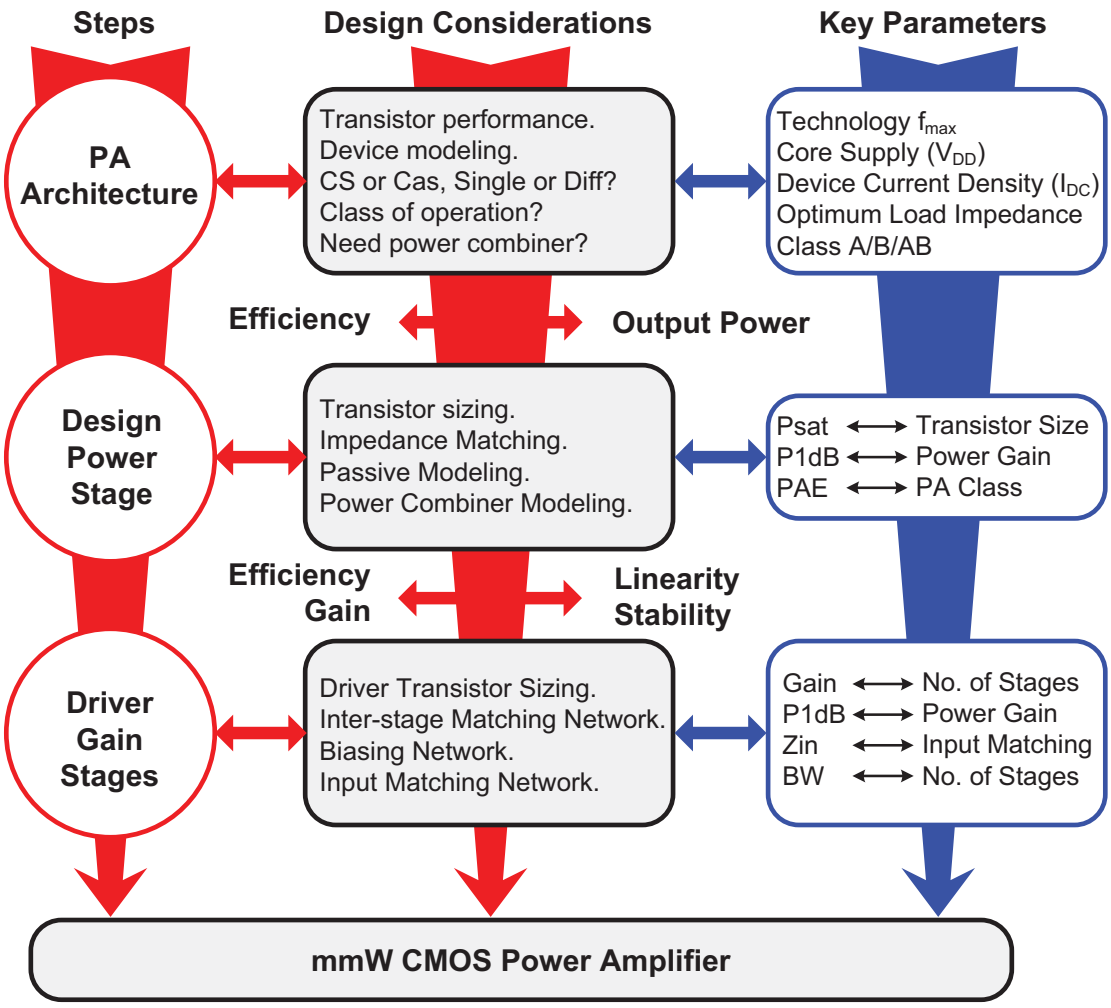


Figure 3.1: Design flow diagram of a mmW PA.

scribed. Finally, the measurement results of the fabricated PA are reported.

3.1 mmW PA Design Methodology

A conventional mmW PA consists of a power stage, driver stages, impedance matching networks and biasing circuits. Fig. 3.1 demonstrates the design flow of a mmW CMOS PA. The PA architecture will be designed based on the required maximum output power which can be generated using a single MOSFET at 60 GHz. At this step, the large-signal and small-signal performances of the power MOSFET devices available in our target technology node must be investigated. Maximum available output power

in a certain semiconductor technology depends on the supply voltage and current capabilities of power MOSFETs. The amplifier circuit topology is chosen based on available gain and output power of a single device. To increase the efficiency of power stages, nonlinear class of operations can be chosen (e.g. Class-AB). However, operating in nonlinear classes will decrease the maximum output power, gain and linearity of the PA as discussed in previous chapter.

In the next step, a power combining circuit topology must be chosen to combine the power of multiple power stages and increase the output power to the desired level. The power combining topology must be able to transform the standard 50 Ω to the optimum load impedance of all power stages simultaneously. The bottleneck of a mmW PA is not only to provide a high output power but a sufficient gain to meet the linearity specifications of the input stages. Driver and gain stages are required to increase the overall power gain of the PA. However, these additional amplifiers consumes DC power and decrease the overall efficiency of the PA. Moreover, inter-stage impedance matching circuits must be modeled using EM simulations to analyze frequency response and loss of mmW matching networks. A mmW PA must be designed to provide a flat gain over a wide range of frequency for 60 GHz applications. Hence, amplifier stages must be designed at different center frequencies to meet the BW specifications which decreases the overall gain of the PA. The biasing circuit is chosen based on the amplifier topology, class of operation and reliability conditions. Choke inductors are a given solution at lower frequencies in order to isolate the MOSFETs from supply fluctuations. Area inefficient choke inductors are avoided to be used at mmW frequencies because of their low self resonant frequency and high insertion loss. Meanwhile, they are not area-efficient to be used in amplifiers with multiple number of stages. On-chip transformers are extensively used in mmW amplifier designs because they can be used as DC bias rails and impedance transformation simultaneously. However, they must be modeled and characterized before they can be used in a mmW design because accurate models are not provided in design kits quite often.

3.2 MOSFETs for 60 GHz PA Design

In addition to lossy passive devices, a major challenge in the design of a fully integrated mmW PA is the low power gain of the large transistors operating near their

cutoff frequencies. Hence, the layout of power devices must be optimized for maximum performance at the frequency of interest. The optimization techniques of mmW MOSFETs has been discussed previously [95]. To provide a high output power, transistors with a large channel width are required. Unlike devices used for small-signal amplification, power MOSFETs with large channel width experience large-signal effects and more parasitics at high frequencies. Modeling complexity of large power transistor increases significantly due to lossy parasitic elements. This requires the 60 GHz designer to model the devices accurately at the frequency of interest. Key parameters that characterize the gain performances of a MOSFET at high frequencies are the transition frequency (f_T) and the maximum frequency of operation (f_{max}) [95]. f_T is defined as the frequency which the current gain is unity, and strongly depends on the CMOS technology features and the physical dimensions of the transistor. The physical layout of a single finger MOSFET is shown in 3.2, along with the dominant high-frequency loss mechanisms. f_{max} is defined as the frequency which the power gain is unity, and it gives the maximum frequency of an active device. For a transistor, f_T and f_{max} are given as

$$f_T \simeq \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{3.1}$$

$$f_{max} = \frac{1}{2} f_T \sqrt{\frac{R_{ds}}{R_g}}. \tag{3.2}$$

For mmW MOSFETs, the f_{max} is primarily limited by by the resistive losses such as gate resistance (R_g) and series drain/source resistance (R_{ds}). The series source and drain resistances are less sensitive to layout changes because they are dominated by the intrinsic sheet resistance. The effective increase in gate resistance because of the finite channel charging time must be modeled as channel resistance (r_{ch}). Considering the distributed RC nature of the polysilicon gate, the gate resistance (R_g) can be approximated using a lumped resistor as

$$R_g = \frac{R_{poly}.W_f}{3.L}, \tag{3.3}$$

where R_{poly} is the polysilicon gate sheet resistance, W_F is the finger width, L is the channel length [96]. To gain insight into the effect of layout, [95] proposed a formula

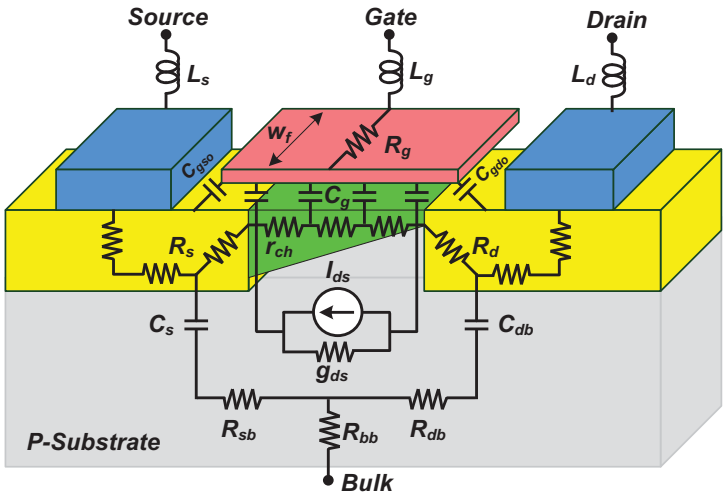


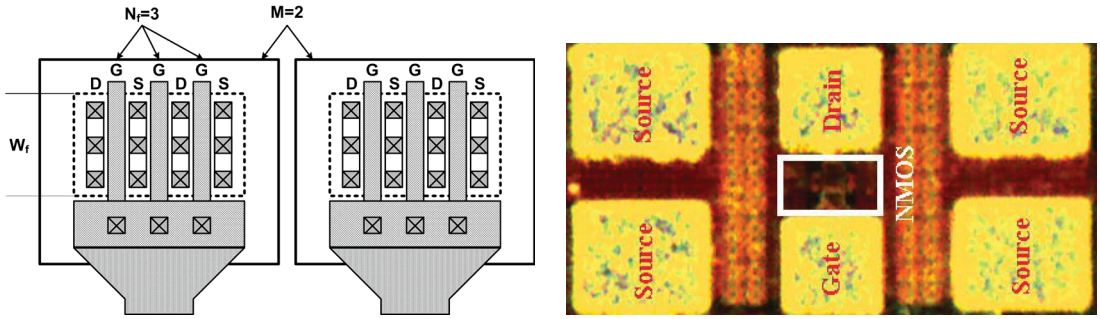
Figure 3.2: Physical model for one finger of an NMOS device [96].

to approximate the f_{max} as

$$f_{max} = \frac{f_T}{2\sqrt{R_g(g_m \frac{C_{gd}}{C_{gg}}) + (R_g + r_{ch} + R_s)g_{ds}}}, \tag{3.4}$$

where the f_T is the unity current gain frequency calculated by (3.1), g_m is the transconductance of the transistor, C_{gg} is the total capacitance appearing at the gate terminal, g_{ds} is the transistor's output conductance, and R_g, r_{ch} and R_s are the gate, channel and source resistances, respectively. As large transistors has small Input/Output (I/O) impedances, they are more sensitive than small transistors to the impedance values seen at the I/O terminals. Although the output power is the primary specification to be satisfied, the gain of a PA must be high enough to decrease the linearity constraints of using driver stages as

The multi-finger parallel configurations are used to achieve both wide channel width and high current as shown in Fig. 3.3(a). A 120 μm power MOSFET is fabricated in 65nm CMOS technology as shown in Fig. 3.3(b). The performance of this kind of power transistor is determined by three physical parameters: the number of fingers (N_f), the width of a single finger (W_f), and the number of cells in parallel (M). W_f affects directly the gate resistance and degradation of the f_{max}. Using multiple fingers is a common way in order to build high power MOSFETs at RF frequencies. However, this has a negative effect, that increasing the total number



(a) (b)

Figure 3.3: Paralleled multi-finger NMOS device with total channel width of 120 μm (a) layout (b) taped-out in 65nm CMOS technology.

of fingers with a fixed finger width leads to a large layout. In this case, although the polysilicon gate resistance per finger remains fixed, large inter-connections are required to connect the gates and drains of multiple fingers, which introduces additional resistive/capacitive losses and leads to a lower f_{max} and gain. The other solution is using fingered transistors in parallel connection as well as increasing the finger width. Hence, large transistors with high current handling capabilities can be obtained using these techniques. However, the I/O impedances drop when the size is increased which leads to higher matching network losses because of the required high impedance transformation ratio.

From simulation or device measurement results, f_{max} can be obtained by calculating the Maximum Available Gain (MAG) or Mason's Unilateral Gain (MUG) of a device. MUG of a two-port device can be defined as

$$MUG = \frac{1}{4}.\frac{|Y_{21} - Y_{12}|^2}{Re[Y_{11}]Re[Y_{22}] - Re[Y_{21}]Re[Y_{12}]}. \tag{3.5}$$

One major advantage of using MUG is the robustness against lossless parasitics [97]. Although the definitions of MUG and MAG are equivalent (MAG=MUG=1 at f_{max}), MAG can be defined only for unconditionally stable devices.

$$MAG = \frac{S_{21}}{S_{12}}.(K - \sqrt{1 - K^2}), \tag{3.6}$$

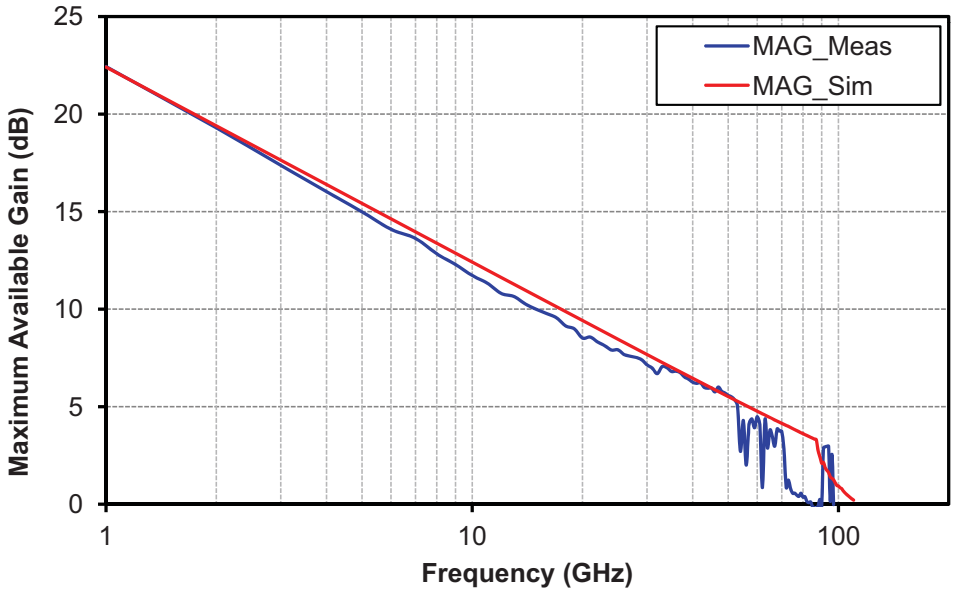


Figure 3.4: Measured and simulated maximum available gain for a $30 \times 4\mu$m/65nm NMOS device biased at 300 μA/μm.

where, K is the stability factor of the device as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}, \tag{3.7}$$

and Δ is an auxiliary condition for stability determined as

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}|. \tag{3.8}$$

Device is unconditionally stable where $K > 1$ and $\Delta < 1$, otherwise there will be a potentially unstable condition. Stability factor less than unity increases the chance to oscillate under certain load impedances. μ factor has been widely used as amplifier stability parameter to summarize the K and Δ factors into one equation as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|}. \tag{3.9}$$

High frequency amplifier is unconditionally stable where $\mu > 1$. The bigger the μ the more stable design. Measured and simulated MAG for the fabricated $30 \times 4\mu m/65nm$ NMOS device biased at 300 μA/μm are shown in Fig. 3.4. For this device, the maximum frequency of operation is measured to be $f_{max} = 100$ GHz. The location of the point where the device becomes unconditionally stable is measured to

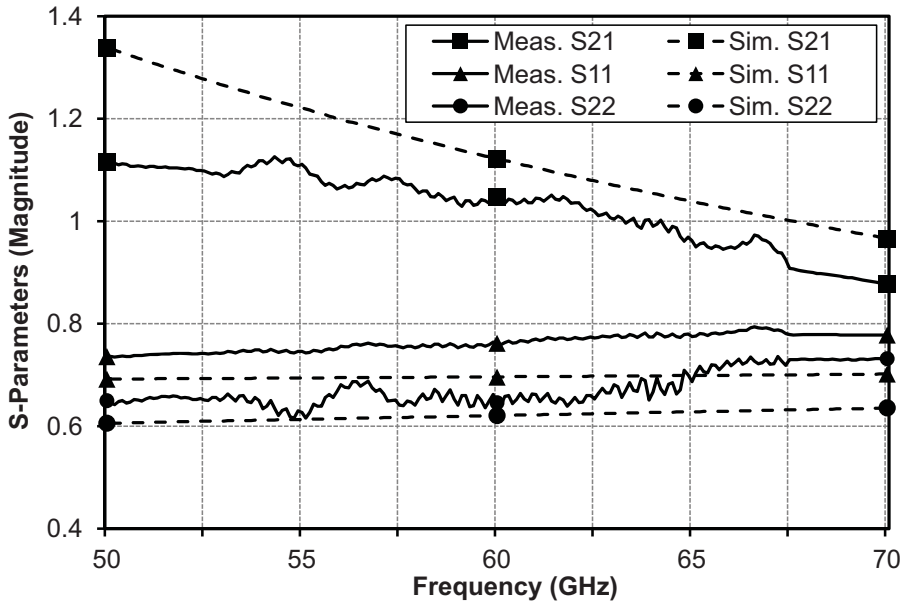


Figure 3.5: Simulated and measured S-parameters of the power NMOS.

be 70 GHz. It can be seen that the gain drops after reaching the knee point. At mmW frequencies, where the gain of the device is very low, gate-drain parasitic capacitance (C_{gd}) plays an important role. Using the Miller theorem, it can be shown that the C_{gd} is the dominant capacitance seen by the drain and gate connection. By taking a closer look at the measured results, a large discrepancy can be observed over the desired frequency range between the measured and simulated S-parameters of the fabricated power MOSFET as shown in Fig 3.5. Although an accurate quesi-3D inter-connection electromagnetic (EM) modeling leads to better performance estimation for PAs , the final performance still depends on the power transistors which must be characterized at mmW frequencies.

f_{max} of various NMOS transistors with minimum channel length as a function of finger width and bias current density are extracted from simulations to find an optimal size of the power devices. Fig. 3.6 illustrates f_{max} dependence on finger widths and bias conditions. The f_{max} shown in Fig. 3.6 is calculated by the Mason's unilateral power gain. Devices with W_f = 1-5 μm and N_f = 32 are simulated in CS configuration. The bulk and source of the transistors are connected to ground. For various bias points, current densities are adjusted (I_{DS}/W = 10-300 μA/μm) per device and the constant f_{max} contours are plotted. According to Fig. 3.6, using

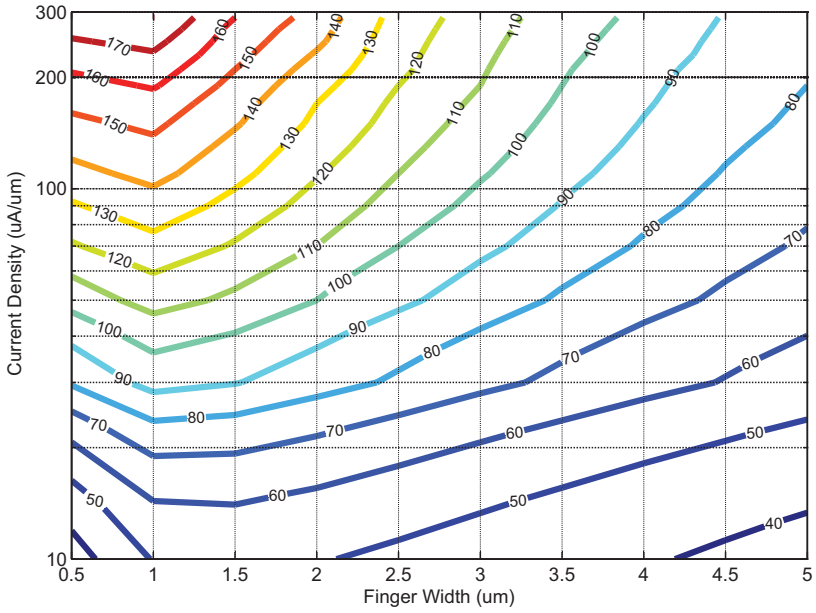


Figure 3.6: Simulated f_{max} of NMOS devices in 65nm technology extracted from MUG.

a finger width of 1 μm to 4 μm with 30 fingers keeps the f_{max} beyond 100 GHz. Furthermore, the device must be biased well into strong inversion (around 100 to 300 μA/μm) for mmW operation.

Optimization of transistor sizes for non-linear applications such as power amplifiers requires precise knowledge of non-linear characteristics of devices over a wide range of operating points. Large-signal device characteristics including current capabilities (I-V measurements) and load-pull simulations are required at this step. The DC I-V curves and extracted transconductance (G_m) of 120 μm common-source NMOS transistor are illustrated in Fig. 3.7 and 3.8. It is demonstrated that a single 120 μm power NMOS can handle drain currents of zero to 100 mA depending on the operating bias points. For class A operation mode, transistor can be biased to deliver 35 mA to 45 mA over a supply voltage of 1.2 V. Considering this bias condition as our quiescent point, transistor's drain voltage and current can handle maximum swing of 1 V and 40 mA respectively. As a result, a 120 μm device can deliver maximum power of 40 mW (16 dBm). However, the transconductance for such a large transistor is low when the device is biased to deliver high drain current (e.g. G_m = 80 mS for

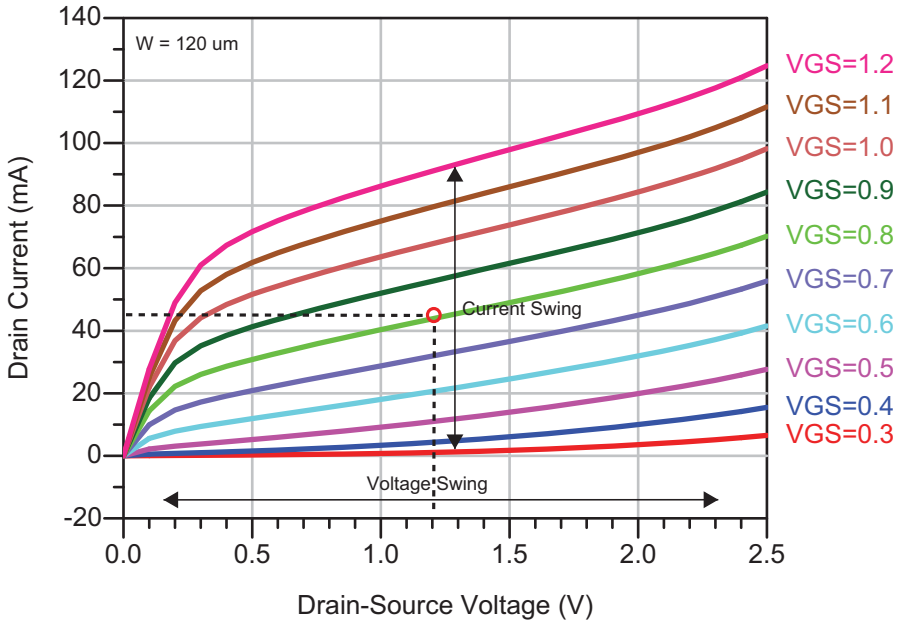


Figure 3.7: Simulated V-I characteristics of the 120 μm power NMOS.

I_{DC} = 50 mA and V_{GS} = 1.0 V).

As it is indicated in introduction section, there is a strong correlation between the output power of a PA and the output impedance matching network. One particularly important test is the load-pull simulation which must be performed on the device to achieve highest possible output power and efficiency and determining the optimal load impedance . Also the size of the impedance transformer can be chosen based on the required load impedance. The load-pull simulation setup consists of a Device Under Test (DUT) in CS configuration, Harmonic Balance (HB) simulator and an impedance tuner to precisely control the load impedance seen at the drain port. Amplifier is biased in class A mode (e.g. V_{GS}=0.9V, V_{DD}=1.2V) to achieve the highest possible output power. Amplifier is excited by a power source and input power (P_{in}) was swept from -10 dBm to 5 dBm at a fundamental frequency of 60 GHz. The process is repeated in order to find the optimal active-passive combination for highest PAE as well. Fig. 3.9 demonstrates the maximum PAE and maximum power contours extracted out of load-pull simulation of a 120 μm NMOS. With the maximum PAE of 48%, a 120 μm NMOS device is able to deliver maximum saturated power of 15.39 dBm to a $0.23 + j0.27$ normalized load impedance. The optimum load

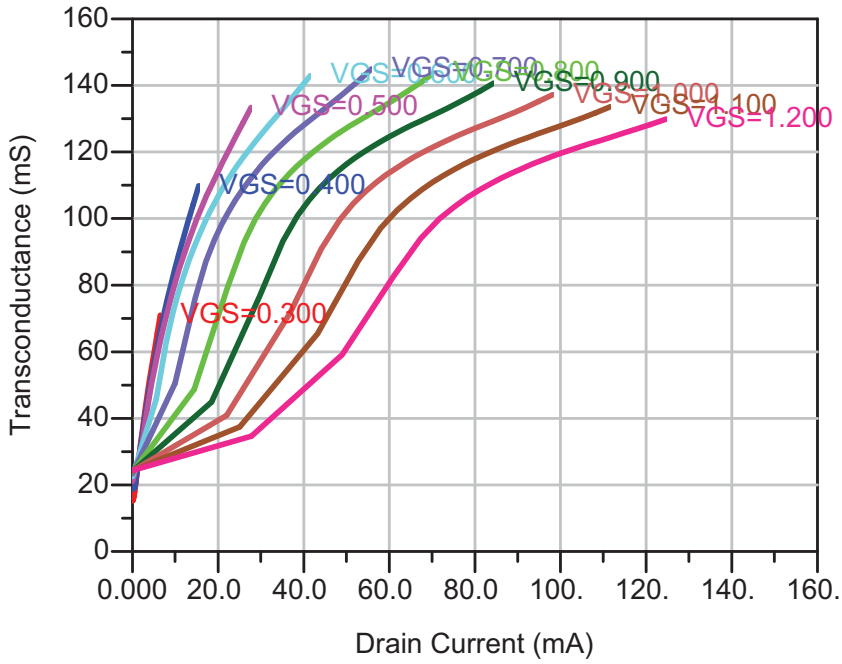


Figure 3.8: Simulated transconductance of the 120 μm power NMOS.

impedance to achieve maximum PAE of 50% (Class-A) is measured to be $0.25 + j0.1$. Load pull simulations are performed at 60 GHz over power MOSFETs with various total channel widths in class A mode.

Table. 3.1 summarizes the load-pull simulation results of NMOS devices with various sizes. With ideal I/O impedance tuners (lossless components), power MOSFETs are able to achieve maximum PAE of 50% in class A mode. Load-pull and small-signal simulation results indicate that the gain of a power MOSFET with large channel width is relatively low at mmW frequencies. Hence, a single-stage PA cannot deliver a high gain and high power simultaneously. As a result, the output power must be further increased by combining the output power of two or more PA stages. However, as a passive structure, power combiners introduce insertion loss which reduce the overall power gain and efficiency. New topology power combiners are required to improve the gain/efficiency while increasing the overall output power.

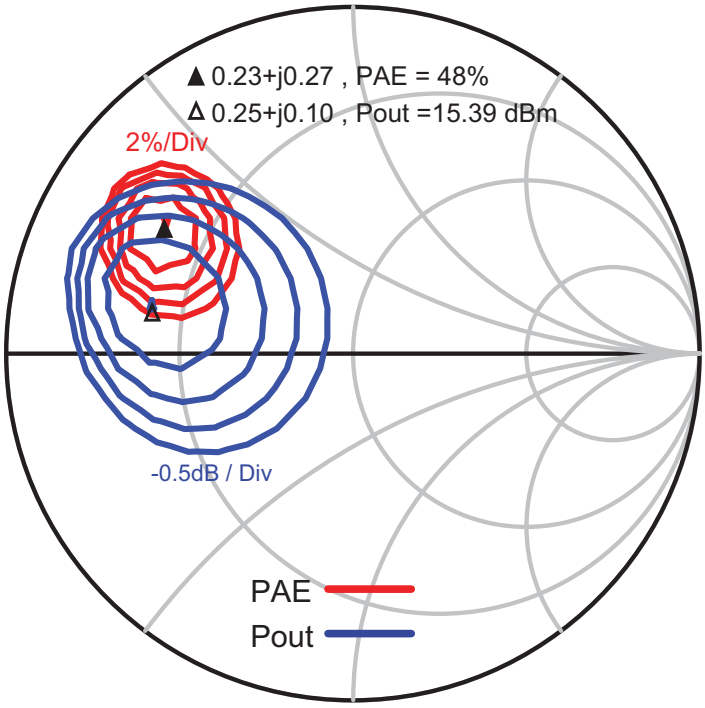
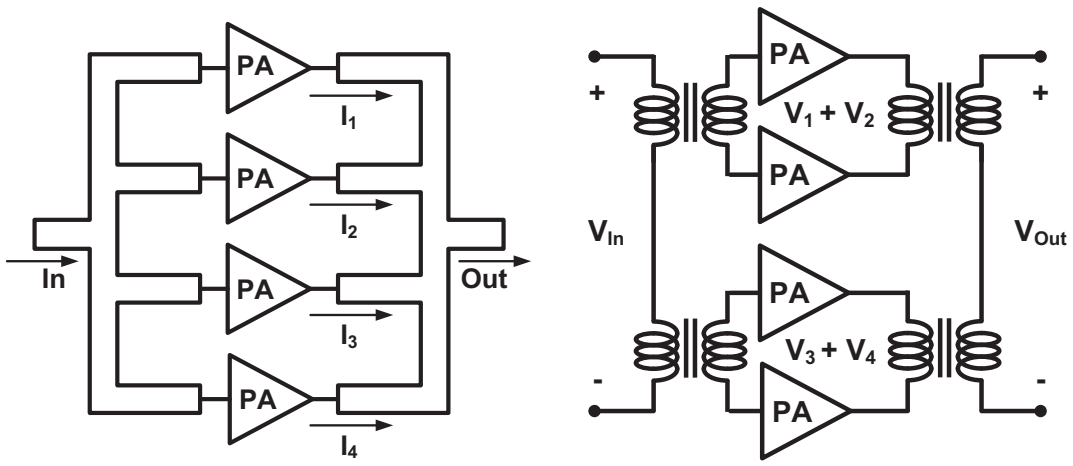


Figure 3.9: Load-pull simulation of 120 μm NMOS in CS configuration biased in class A mode of operation (V_{GS} = 0.9 V, V_{DD} = 1.2 V).

Table 3.1: Summary of load-pull simulations for NMOS devices.

Size [μ**m**]	$\mathbf{Z}_{opt}/50\Omega$	$\mathbf{PAE}_{max}$ [%]	$\mathbf{P}_{sat}$ [**dBm**]	$\mathbf{P}_{1dB}$ [**dBm**]
50	0.56+j0.59	50	11.83	10.40
64	0.42+j0.43	50	12.87	11.20
72	0.35+j0.39	50	13.37	11.57
80	0.34+j0.37	50	13.79	11.95
90	0.28+j0.33	50	14.27	12.37
100	0.27+j0.33	50	14.69	12.75
120	0.23+j0.27	50	15.39	13.43



(a) (b)

Figure 3.10: Power combiner topologies (a) current combining (b) voltage combining.

3.3 Proposed Multi-Conductor Power Combiner

One of the main challenges in the design of power stage is to achieve a high level of maximum saturated output power using CMOS transistors with relatively low gain at 60 GHz. Considering the fact that the gain of the power MOSFETs with large channel width is relatively low at mmW frequencies, a single-stage PA cannot deliver a high gain and high power simultaneously. A common approach to improve the P_{sat} and PAE of 60 GHz PAs is to combine the output powers of several single-stage PAs using spatial power combiners, distributed transmission lines and on-chip transformers. Some other reasons to utilize power combiner are the low output impedance of the transistors, low supply voltage and low breakdown voltage in CMOS technology. Employing a proper power combining architecture, the output voltage/current can be divided into multiple transistors increasing the reliability of the circuit. Two major topologies are used to combine the power of multiple PAs: combining the current or combining the voltage as shown in Fig. 3.10.

By the use of current combining, transistors do not experience high voltage excursion which ensures the reliability. However, the structure can be used for only one operating mode that means the amplifier will not operate functional if one of the PA cells is turned off or experiences a mismatch. Using voltage combining topology, PA cells can work independently so that the overall power or efficiency of the amplifier

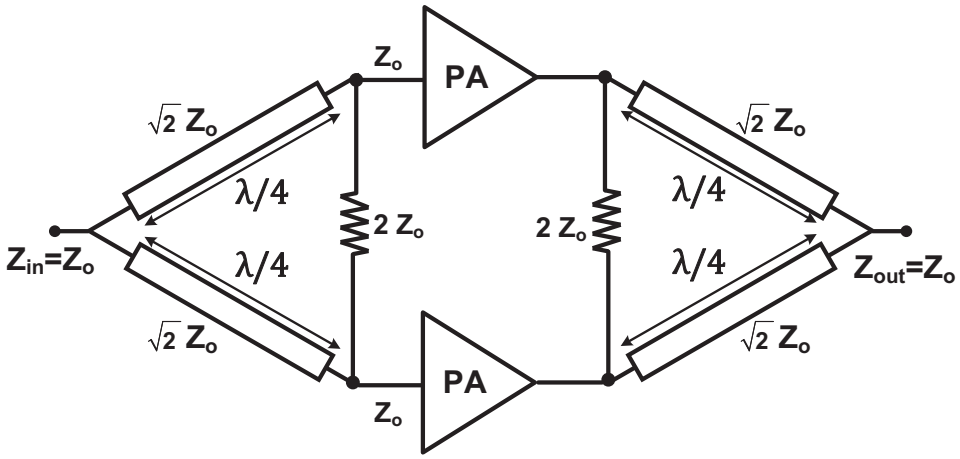


Figure 3.11: Wilkinson power combiner/divider topology.

can be controlled. However, the topology suffers from stability issues because of low self resonant frequency of inductors in series configuration.

Power combiners based on Wilkinson topology are popular current combining strategies [17]. Fig. 3.11 demonstrates the Wilkinson power combining structure. Using on-chip microstrip transmission lines, Wilkinson topology introduces equal phase delay to the output of each PA cell which is mandatory for proper power combining. The characteristic impedance of the microstrip lines can be designed to match the output impedance to the output of the PAs. If the input and output impedance are Z_o, the combiner consists of two quarter wavelength transmission lines with characteristic impedance of $\sqrt{2}Z_o$. In order to provide power to each of the PA cells, a power divider is required at the input. Hence, Wilkinson topology uses four quarter wavelength transmission lines to combine output power of two PA cells. The length of an on-chip quarter wavelength transmission line is 600 μm in silicon technology. Implementing such bulky passive components on chip introduce significant power loss and thus lower the overall output power and efficiency. Moreover, using Wilkinson power combiner is not area efficient for combining of more than two PA stages. Another drawback of the Wilkinson topology is lack of ability to provide DC biasing path for PA cells. Independent DC biasing circuit introduces significant power loss and increases the chance of mismatch between stages.

On-chip transformers are preferred over the spatial power combiners because of their smaller physical size and lower loss. Voltage combining can be realized using

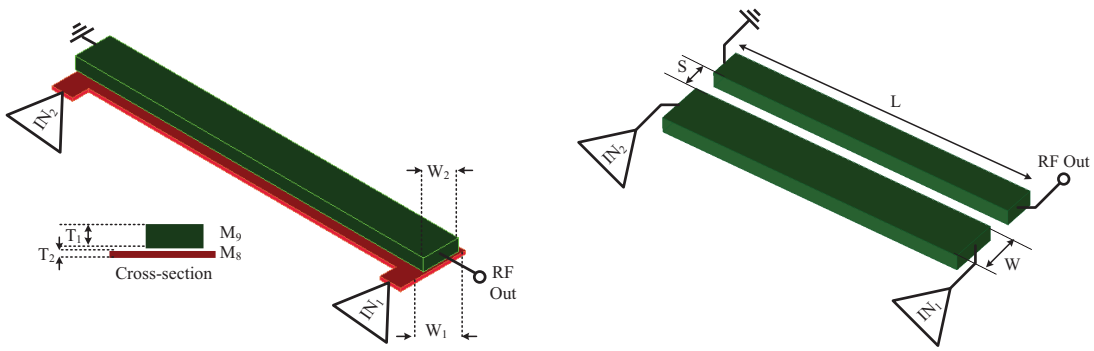


Figure 3.12: Realization of mmW power combiners (a) stacked transformer (b) planar transformers.

multiple transformers in series as shown in Fig. 3.10(b). The use of transformer-based power combining was first proposed by [98] for 2 GHz cellular PA design. However, they are extensively used in advanced mmW PAs to combine the output power of several single-stage power amplifiers in series configuration [62–65]. Transformers provide high efficiency and impedance matching ability. At the same time, they can be designed to provide DC biasing of transistors in compact chip area [98]. Stacked transformers and planar coupled lines are common methods to realize the transformer-based power combiners as shown in Fig. 3.12 [99] [52].

Windings with large occupied area are required to realize transformer-based combining of more than two PA cells. Eddy current produced by the induced electromagnetic waves into the substrate can cause high energy dissipation. The amount of the power dissipation is proportional to the size of the windings [88]. Hence, these physically large structures are lossy components. A thick top metal layer with low sheet resistance is available in today's semiconductor technologies. However, one of the primary or secondary windings can be constructed with quality factor. The other winding can be constructed of metal layers beneath the top metal layer which is typically several times thinner than the top metal layer. In side-by-side transformers (Fig. 3.12(b)), both primary and secondary windings are constructed using the top metal layer to improve the quality factor because of lower sheet resistance of primary windings compared to stacked transformers. However, the coupling factor between the windings is reduced because of the minimum allowable spacing between the metal traces and fixed vertical cross-section imposed by process design rules.

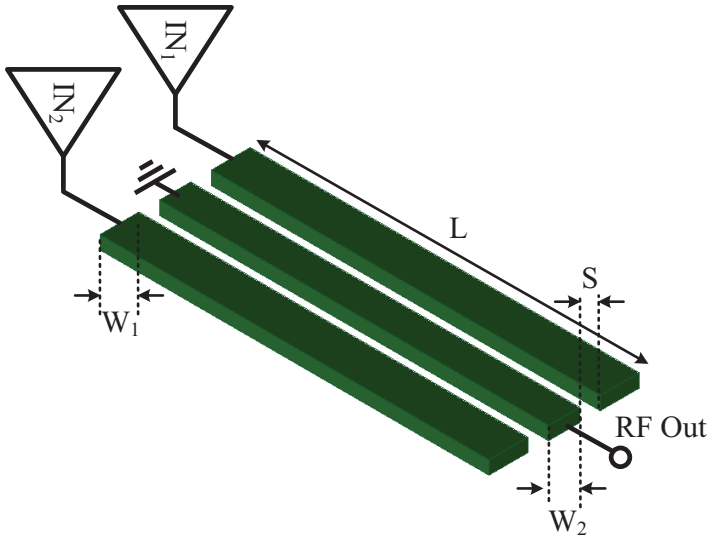


Figure 3.13: Proposed multi-conductor planar transformer.

Finally, physically large secondary winding of the stacked and planar series combiners introduce high output inductance which dramatically reduces SRF of transformers. Hence, the series power combining structures are not practically feasible for combining of more than a few amplifiers at mmW frequencies as the resonance frequency falls below 60 GHz in complex structures. Breaking the trade-off between the low quality factor of stacked transformers and low coupling factor of planar transformers, we propose a planar multi-conductor power combiner that can be implemented on the top layer of the technology while producing the desired coupling using multiple primary windings.

Fig. 3.13 illustrates the basic idea of the proposed parallel power combining topology. Low loss windings with very high SRF are feasible at mmW frequencies with the metal layer available in most standard CMOS technologies. Implemented on 700 μm silicon substrate with 10 Ω.cm conductivity, an ultra thick metal layer (M_9) and a thick metal layer (M_8) underneath are the two top layers developed in 1P9M TSMC 65 nm standard CMOS technology with 5 m$\Omega/\square$ and 22 m$\Omega/\square$ sheet resistances respectively.

The cross-section of the 1P9M 65nm CMOS technology is shown in Fig. 3.14. Although a distance of 0.75 μm between two layers improves the EM coupling, the high sheet resistance of M_8 increases the power loss. The proposed topology has the advantage of high Self Resonant Frequency (SRF) because of the shorter and

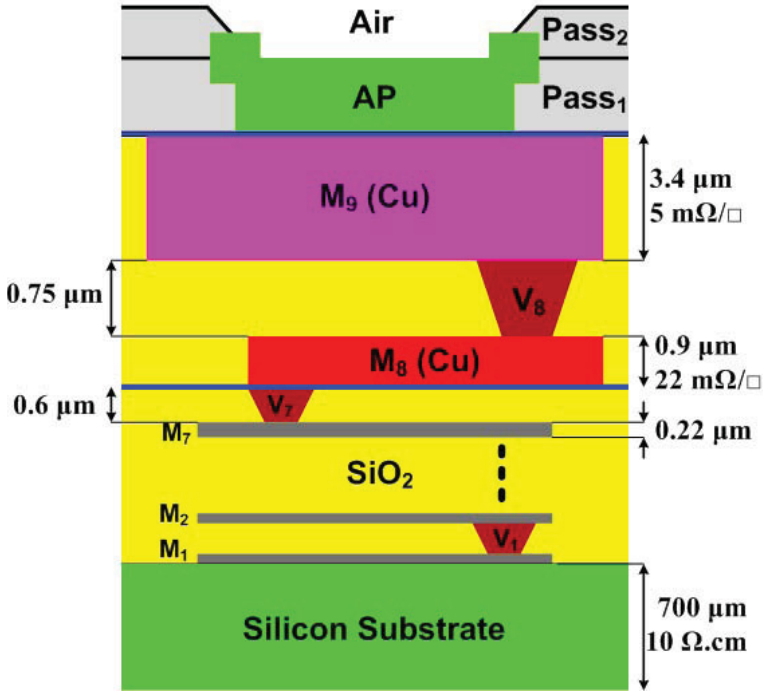


Figure 3.14: 1P9M TSMC 65nm CMOS process cross-section.

higher-Q secondary traces in comparison with the series power combiners. The challenging aspect of designing the combiner is to choose a topology which can provide the impedance transformation, bias requirements and power combining simultaneously. By implementing both primary and secondary winding on a same metal layer, higher quality factor is achievable and results in a low loss highly efficient combiner. To achieve a high coupling factor and lower the substrate loss, primary windings are implemented on both sides of the secondary winding. EM simulations have been performed to match the output impedance of our 120 μm power transistors to the 50Ω load. Windings with 80-100 μm length can be chosen to provide impedance matching based on EM simulations. The width of the metal traces vary from 6 um to 8 μm based on the required output current. The metal width of the center winding should be 8 μm to be able to deliver more than 150 mA to the load.

3D EM simulations are performed to compare the coupling factor and efficiency of the proposed multi-conductor topology with the stacked and side-by-side transformer-based power combiners. Insertion loss of a stacked transformer with total length of 90 μm, planar transformer with same length, and proposed multi-conductor transformer with 90 μm length are illustrated in Fig. 3.15.

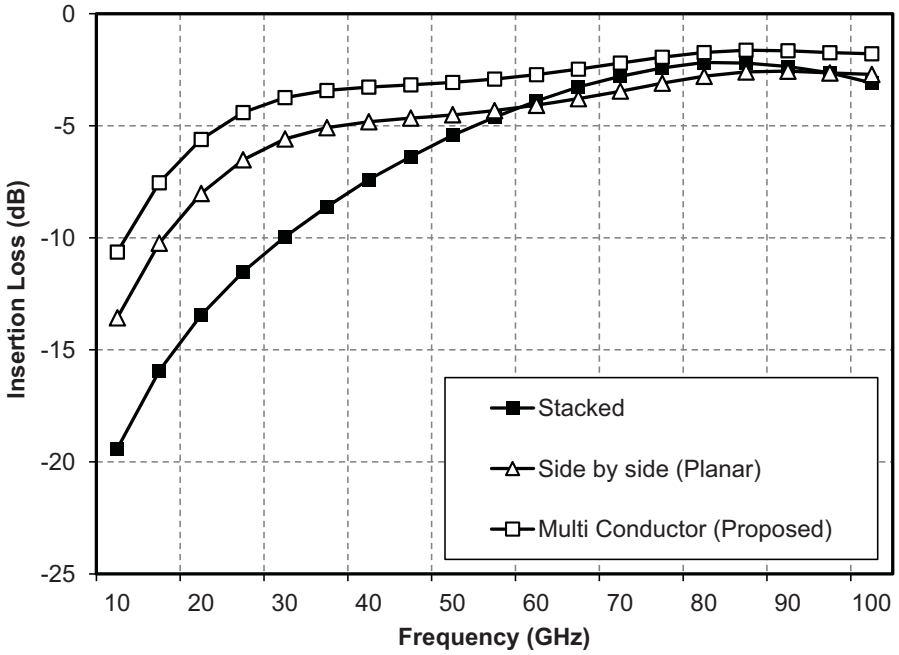


Figure 3.15: Insertion loss of same sized power combiners.

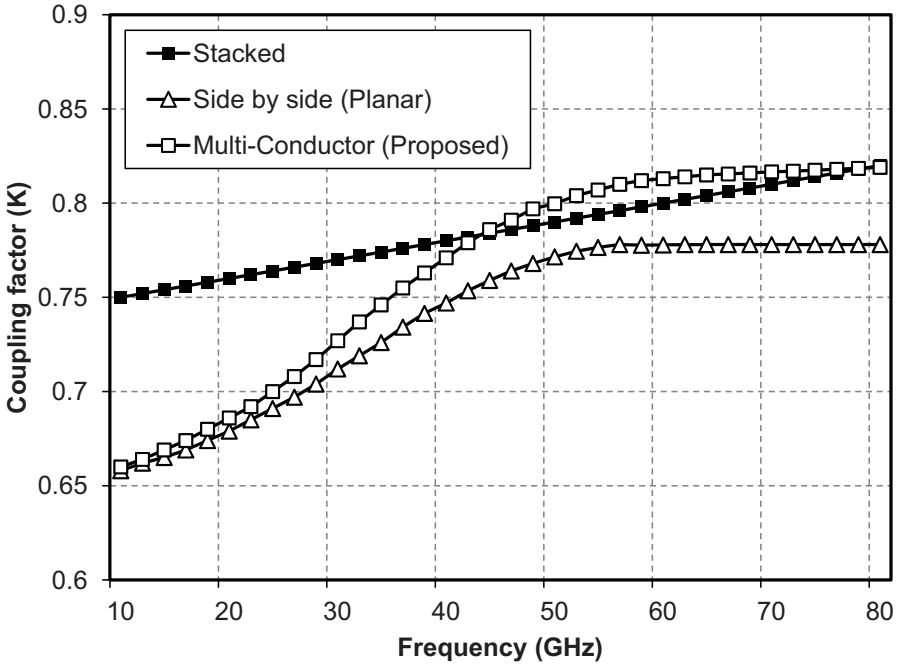


Figure 3.16: Effective coupling factor of on-chip power combiners.

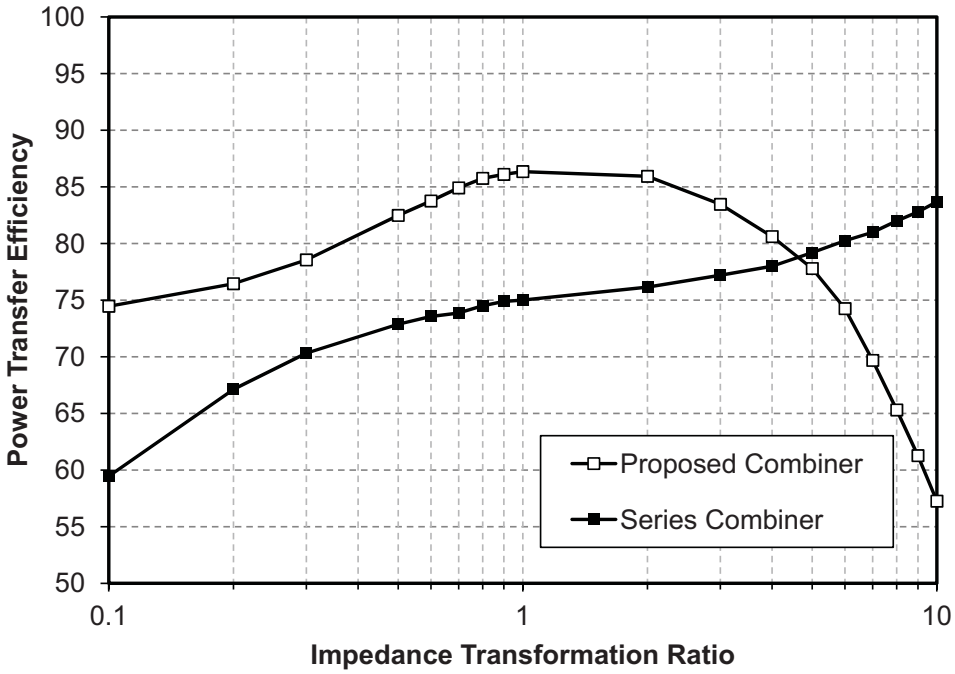
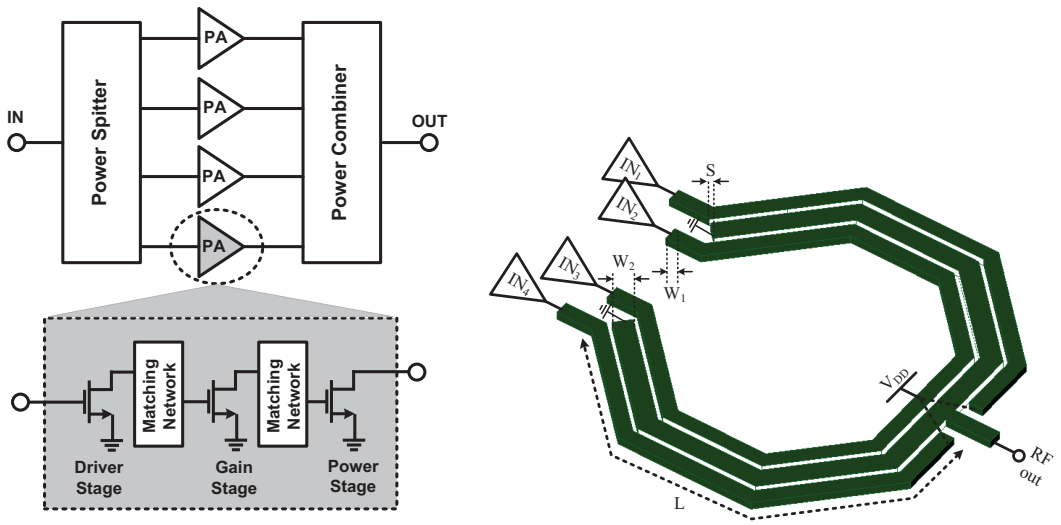


Figure 3.17: Power transfer efficiency versus ITR for parallel and series combiners.

Effective coupling factor between windings is extracted from EM simulations and demonstrated in Fig. 3.16 for all three structures. Compared to the other counterparts, the proposed multi-conductor structure shows larger gain performance over a wide bandwidth based on the simulated insertion loss, and the effective coupling factor between windings is comparable with the stacked transformer at high frequencies as shown in Fig. 3.16. 3D EM simulations have been performed to compare the power transfer efficiency of the proposed structure and the conventional series power combiner for different Impedance Transformation Ratios (ITR) ranging from 0.1 to 10. Power transfer efficiency of the proposed method and the conventional series combiner are compared in Fig. 3.17 based on the maximum available gain at 60 GHz. For ITRs less than unity, the proposed method results in power transfer efficiencies higher than 80% for ITRs from 0.4 to 5 which are significantly higher than the efficiency obtained by conventional series combiners. For ITRs higher than unity, the proposed power combiner still shows higher efficiency for ITRs less than five.



(a) (b)

Figure 3.18: Proposed architecture of the 60 GHz PA (a) Building-block diagram of the proposed 60 GHz PA (b) realization of multi-conductor 4-way parallel power combiner.

Although the basic structure of the proposed combiner exhibits significant efficiency improvement, a modification is required to realize combination of multiple PA stages. As shown in Fig. 3.18, a 4-way parallel power splitter/combiner, based on the proposed multi-conductor cross-coupled transformer architecture, is required to combine the output current of four individual PAs to achieve a higher output power than the conventional structures.

Fig. 3.18(b) illustrates the physical realization of the proposed power combiner. Two branches of multi-conductor planar transformers are connected in parallel to form a four-way combiner with four primary windings and two parallel secondary windings. The primary and secondary windings are designed on the ultra-thick metal layer (M_9) to achieve the lowest sheet resistance and consequently highest possible quality factor. By designing the primary windings in adjacent of the secondary winding, frequency response of the proposed structure can be controlled by the wall-to-wall distance between the windings (S), width of the primary/secondary windings (W_1, W_2) and the length of each branches. The primary windings will be excited by individual power amplifiers and RF power will be transferred to the output via the electromagnetic coupling between the windings. A premier advantage of the proposed structure is

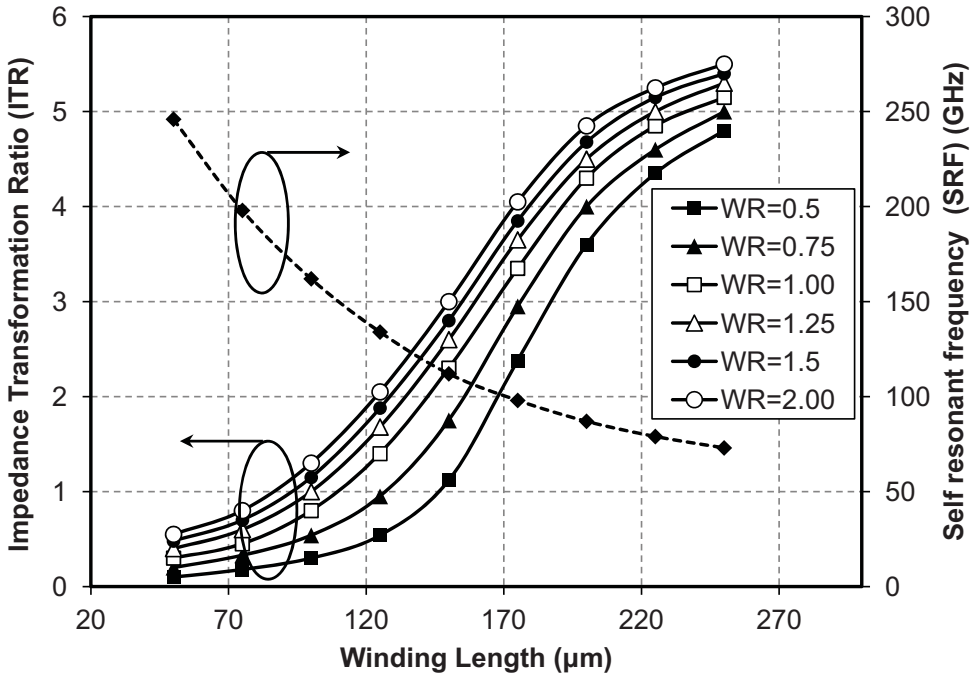


Figure 3.19: Impedance transformation ratio versus windings length and width ratio.

to get the maximum available coupling by designing three ultra-thick windings in adjacent. In this case, the primary windings can prevent the extra energy loss on the secondary windings because of the EM wave induction in the substrate. Lower wall-to-wall distance of traces in adjacent results in low parasitic coupling capacitance and increases the SRF.

Power combiner must be able to transform the output impedance of the power transistors to the 50 Ω load while combining the output of four individual stages. The maximum available ITR achieved by the proposed combiner determines the maximum size of the transistors in power stages. As discussed in previous sections, power transistor with large channel width and low output impedance will be feasible with capability of producing a high ITR at 60 GHz. In addition, the SRF of the power combiner must be far from 60 GHz to prevent the oscillation and instability. To calculate the design requirements for different ITRs at 60 GHz, a set of 3D EM simulations are performed. Fig. 3.19 illustrates the achieved ITRs and SRF at 60 GHz for different values of secondary-to-primary width ratio ($W_R = W_2/W_1$), ITR, and the length of the primary/secondary windings (L). Simulation results show that the higher ITR is achievable by increasing the length of the power combiner with high W_R.

By changing the width of the metal traces for a range of 6μm to 12μm, the parasitic metal-to-ground capacitance can be controlled to achieve different inductance for primary/secondary windings. The coupling factor between the secondary/primary windings and the parasitic coupling capacitance can be controlled by changing the spacing distance between the windings (S). The minimum allowed spacing of 2 μm is chosen to achieve highest possible coupling factor while satisfying the process design rule requirements. The coupling factor also depends on the length of the windings. Windings with longer traces introduce more mutual inductance and coupling factor. Maximum and minimum power transfer efficiency of 85% and 70% are obtained based on the transmission loss of -0.55 dB and -1.5 dB respectively. To achieve an ITR of 4 to 5, proposed topology with 200 μm winding length, width ratio of 1.5 is designed to combine the output power of four PA stages.

3.4 Design of Inter-Stage Matching Networks and Driver Stages

To provide sufficient power gain, each PA cell includes cascaded CS driver and gain stages. Inter-stage matching circuits consist of passive components are required between driver and PA stages in order to ensure maximum power transfer efficiency. Design of mmW inter-stage matching circuits providing high power transfer efficiency is challenging as well as satisfying the stability requirements. Passive networks consisting of on-chip inductors, capacitors, transmission lines, and on-chip transformers are the key building blocks of mmW power amplifiers as discussed in the previous chapter. It is necessary to utilize the passive structures for the purpose of impedance transformation, inter-stage matching and DC biasing. However, all passive networks have non-zero Insertion Loss (IL) which directly impacts the power efficiency. Due to the high impedance transformation ratio, design of low-loss matching components is rather difficult in designing a mmW power amplifier in the deep submicron low power CMOS technology. This section discusses the design of gain stages consisting inter-stage matching circuits, circuit simulations and measured results of the fabricated PA.

Three different matching networks are typically used for power amplifier applications: spatial transmission line based power combiners, LC resonant matching circuits

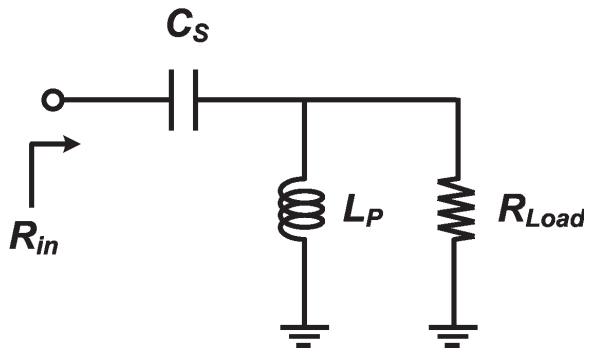


Figure 3.20: LC matching circuit with a series capacitor and a parallel inductor.

and on-chip transformers. The transmission line based strategies consisting of Wilkinson power combiners are avoided due to their low efficiency, area limitations and high cost of implementation as discussed in previous section. In this section, a comprehensive study on the different types of matching circuits for amplifier design will be presented, including modeling methods for on-chip transformers. For both the LC matching and transformer networks, mmW equivalent circuit models are proposed to estimate the power transfer efficiency of various structures. Effects of low quality factor capacitors at mmW frequencies are considered in the proposed models. Finally, transformers are characterized with EM simulations and measurements.

Finally, design of driver stages including transformer-based inter-stage matching circuit is discussed in this section. EM simulation results have been used to the chose optimum size of passive components. Simulation results and measured performance of the fabricated 60 PA are demonstrated.

3.4.1 LC resonant matching networks

Matching circuits are the passive structures to transform the I/O impedance of the amplifiers to the desired source/load resistors. Design of LC resonant matching circuit at low frequencies is covered by microwave design text books [17]. However, design of efficient passive components at mmW frequencies requires accurate modeling of parasitics. A single stage LC matching network is shown in Fig. 3.20, consisting of a capacitor and an inductor which need to be designed. A lossy inductor with finite quality factor can be modeled as a parallel equivalent circuit. By adding a resistor to model the loss as shown in Fig. 3.10 the power loss of the matching circuit can be

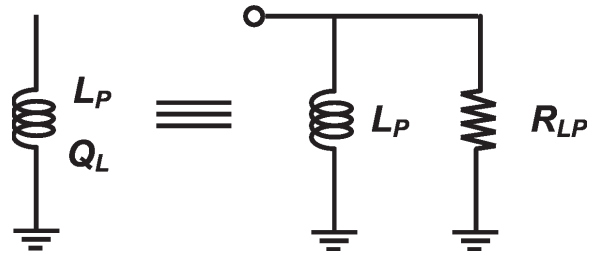


Figure 3.21: Parallel circuit model of loss in an inductor.

calculated [98–100]. The value for this resistance is given by

$$R_{LP} = \omega.L_P.Q_L, \tag{3.10}$$

where ω is angular frequency, L_P is the value of inductor and Q_L is the quality factor of the inductor.

For the matching circuit shown in Fig. 3.21, the quality factor of the network (Q_N) at the frequency which L_P and C_S resonates can be defined as

$$Q_N = \frac{R_{LP}||R_{Load}}{\omega L_P} = \frac{R_{Load}}{\omega L_P + \frac{R_{Load}}{Q_L}}, \tag{3.11}$$

where R_{Load} is the load impedance that needs to be matched at the input impedance (R_{in}) [98]. Therefore, the total input resistance is given by

$$R_{in} = \frac{R_{LP}||R_L}{1+Q_N^2} = \frac{1}{1+Q_N^2}.\frac{R_L}{1+\frac{R_L}{\omega L_P Q_L}}. \tag{3.12}$$

The impedance transformation ratio shows the ratio of the load impedance to the achieved input impedance and is given as

$$ITR = \frac{R_L}{R_{in}} = \frac{R_L}{R_{LP}||R_L}(1+Q_N^2) = (1+Q_N^2)(1+\frac{R_L}{\omega L_P Q_L}). \tag{3.13}$$

The efficiency of a passive network can be defined as the ratio of the power delivered to the load to the power delivered into the network. The power transfer efficiency (η) can be calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{|V_{out}|^2/(2R_L)}{|V_{out}|^2/(2(R_{LP}||R_L))} = \frac{1/R_{LP}}{1/R_{LP}+1/R_L} = \frac{1}{1+\frac{R_L}{\omega L_P Q_L}}. \tag{3.14}$$

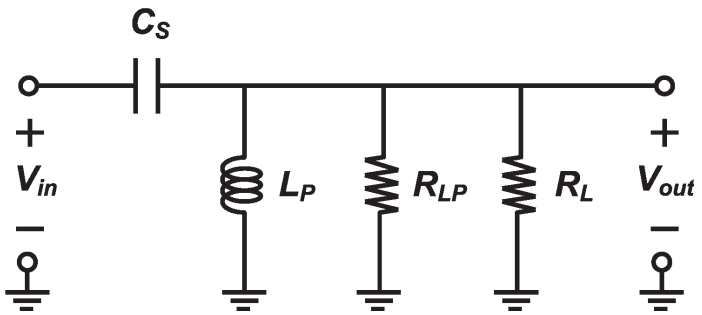


Figure 3.22: Single stage matching network with lossy inductor.

where P_{out} is the power achieved at output, P_{in} is the input power and V_{out} is the output voltage across the load impedance.

The required inductance can be calculated in terms of the ITR, load resistor (R_L), and inductor quality factor (Q_L) as

$$L_P = \frac{R_{LP}}{\omega Q_L} = \frac{2(Q_L + 1/Q_L)}{ITR - 2 + \sqrt{ITR^2 + 4Q_L^2(ITR-1)}} \frac{R_L}{\omega}. \tag{3.15}$$

The efficiency of the network can be simplified in terms of the ITR and Q_L by substituting (3.15) into (3.14), resulting in (3.16) [98]:

$$\eta = \frac{1 + Q_L^2}{Q_L^2 + \frac{ITR + \sqrt{ITR^2 + 4Q_L^2(ITR-1)}}{2}} \approx \frac{1}{1 + \frac{ITR}{Q_L^2}}. \tag{3.16}$$

The efficiency of the LC matching network is plotted in Fig. 3.23 for different inductor quality factors. As can be seen in the plot, the power efficiency drops quickly as ITR increases for a given quality factor. The reason for this is that in the resonant network, the energy that circulates in the LC tank is Q_N times greater than the energy delivered to the load [98]. As ITR increases, Q_N increases, so more energy is dissipated in the lossy inductor. This is a fundamental problem in mmW PA design since often a high ITR is required. Although the quality factors of the inductors are the main source of energy dissipation for RF frequencies, the quality factor of capacitors must be taken into account at mmW frequencies.

A more accurate model for a single stage matching network at mmW frequencies taking into account the losses of n-chip capacitors is shown in Fig. 3.24. The impact of capacitors with low quality factor can be modeled as a resistor in series with an ideal capacitor as shown in the dotted region. The quality factor of the inductor and

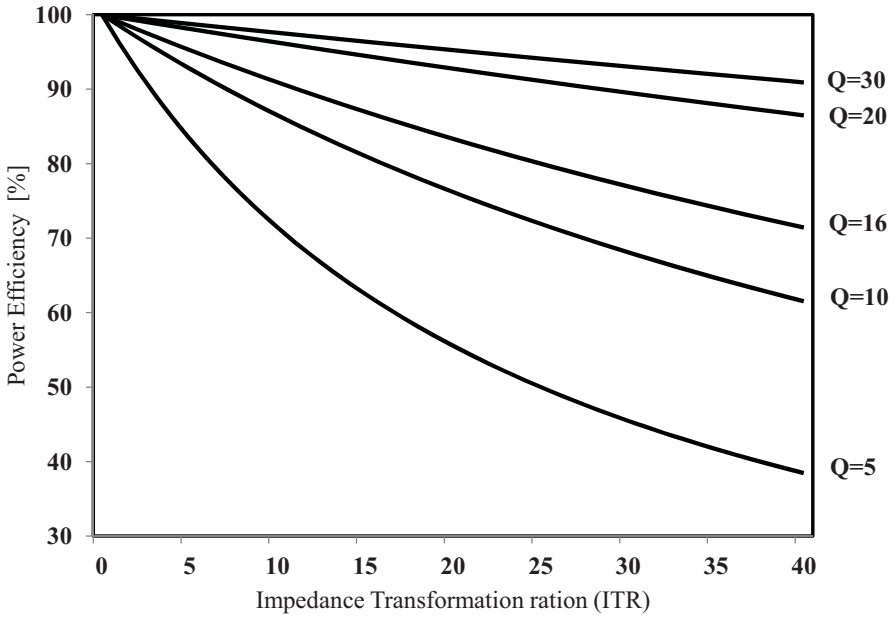


Figure 3.23: LC matching network efficiency for different inductor quality factors.

the capacitor with respect to the parallel and series resistors can be calculated as

$$Q_L = \frac{R_{LP}}{\omega L_P}, \tag{3.17}$$

$$Q_C = \frac{1}{\omega C R_C}. \tag{3.18}$$

These values can then be used to evaluate the efficiency of the proposed model. Another important metric is the voltage gain. The voltage gain of the resonant matching network is always less than unity and can be found as

$$K = \frac{V_{out}}{V_{in}} = \frac{R_L || R_{LP}}{(R_L || R_{LP}) + R_C}. \tag{3.19}$$

The power transfer efficiency (η) of the network can be determined as the power delivered to the load (P_{out}) divided by the power (P_{in}) at the input as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2/2R_{out}}{V_{in}^2/2R_{in}}, \tag{3.20}$$

where R_{out} and R_{in} are the resistances seen from input and output respectively. Next

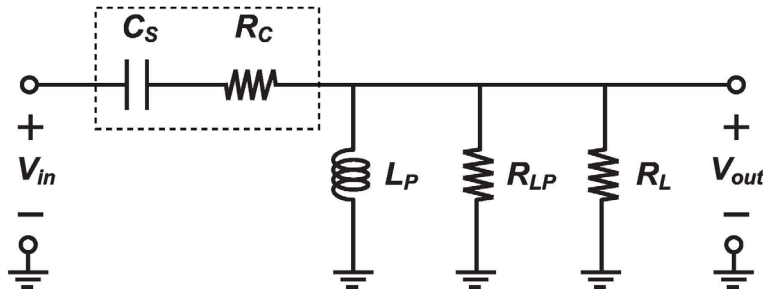


Figure 3.24: LC matching network model including lossy components.

substitute (3.19) into (3.20) to calculate the efficiency as

$$\eta = K^2 \frac{(R_L||R_{LP}) + R_C}{R_L}. \tag{3.21}$$

Finally, substituting (3.19) into (3.21) gives (3.22), which is a closed form equation for calculating the efficiency as

$$\eta = \frac{(R_L||R_{LP})^2}{R_L[(R_L||R_{LP}) + R_C]}. \tag{3.22}$$

Although the efficiency can be calculated by (3.22), it is necessary to provide an expression which can evaluate the passive matching circuit directly from the circuit element not the extracted parasitics. For simplicity, equation (3.22) can be divided in two separated expressions as

$$\eta = A \times B. \tag{3.23}$$

where,

$$A = \frac{1/R_L}{(1/R_L) + (1/R_{LP})} = \frac{1}{1 + \frac{R_L}{\omega Q_L L_P}}, \tag{3.24}$$

$$B = \frac{1}{1 + \frac{R_C}{R_L||R_{LP}}}. \tag{3.25}$$

Finally, expression for power efficiency is found to be

$$\eta = \frac{1}{1 + \frac{R_L}{\omega Q_L L_P}} \times \frac{1}{1 + \frac{R_C}{R_L} + \frac{R_C}{R_{LP}}}. \tag{3.26}$$

Finally, we propose a closed-form equation to give the efficiency of a matching

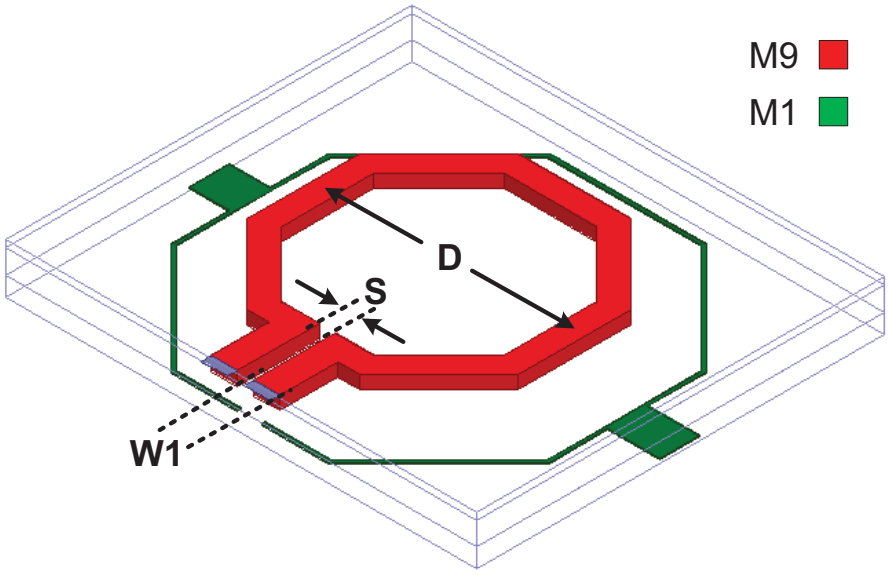


Figure 3.25: On-chip spiral inductor in CMOS technology.

circuit in respect to the quality factor and value of the inductor and capacitor, the value of the load resistance and the frequency of operation as

$$\eta = \frac{1}{1+\frac{R_L}{\omega Q_L L_P}} \times \frac{1}{1+\frac{1}{\omega C Q_C R_L}+\frac{1}{Q_C Q_L \omega^2 L_P C_S}}. \tag{3.27}$$

Passive inductors used in mmW designs are typically on the order of 100 pH and, therefore, occupy small area on chip. Smaller the area, less capacitance between the inductor's metal traces and the silicon substrate allowing the inductors to operate at higher frequencies [101]. Design methodologies of CMOS on-chip inductors and capacitors at mmW frequencies have been reviewed by researchers [97, 101, 102]. However, every CMOS process has unique technology features which affects the characteristics and high performance of the on-chip passive structures.

Spiral inductors, presented in Fig. 3.25, are being used extensively in CMOS RFICs to take the advantage of compact design. A guard ring is used to isolate the inductor from the other components on a single chip. Designed in TSMC 1P9M CMOS technology, the on-chip inductor uses an ultra-thick metal (UTM) layer (M_9) with 3.4 μm thickness implemented on 5.4μm SiO_2 and 700μm Si substrates respectively. Top metal layers are desired for on-chip inductors because of low sheet resistance and high current handling of those thick layers. EM simulations using Advanced Design

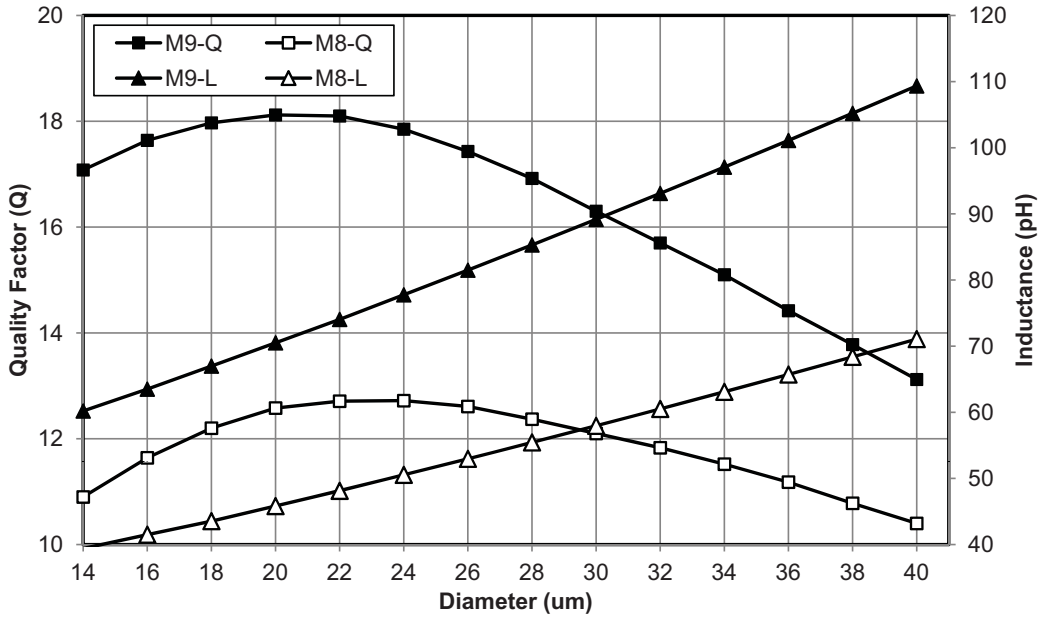


Figure 3.26: Extracted inductance and quality factor of On-chip spiral inductors in 65nm 1P9M CMOS technology at 60 GHz.

System (ADS) Momentum are performed for characterization of on-chip inductors. From two port S-parameter simulations, inductor parameters can be extracted as

$$S_{\Delta} = \frac{S_{11} + S_{22} - S12 - S21}{2}, \tag{3.28}$$

$$Z_{\Delta} = 2 \times R_0 \times \frac{1 + S_{\Delta}}{1 - S_{\Delta}}, \tag{3.29}$$

$$L = \frac{Im[Z_{\Delta}]}{2 \times \pi \times f}, \tag{3.30}$$

$$R_0 = 50\ \Omega, \tag{3.31}$$

$$Q = \frac{Im[Z_{\Delta}]}{Re[Z_{\Delta}]}. \tag{3.32}$$

Fig. 3.26 shows the extracted inductance and quality factor of spiral inductors with various diameters implemented on top metal layers (M_9 and M_8) in 1P9M 65nm CMOS technology. Simulation results indicates that the average quality factor of

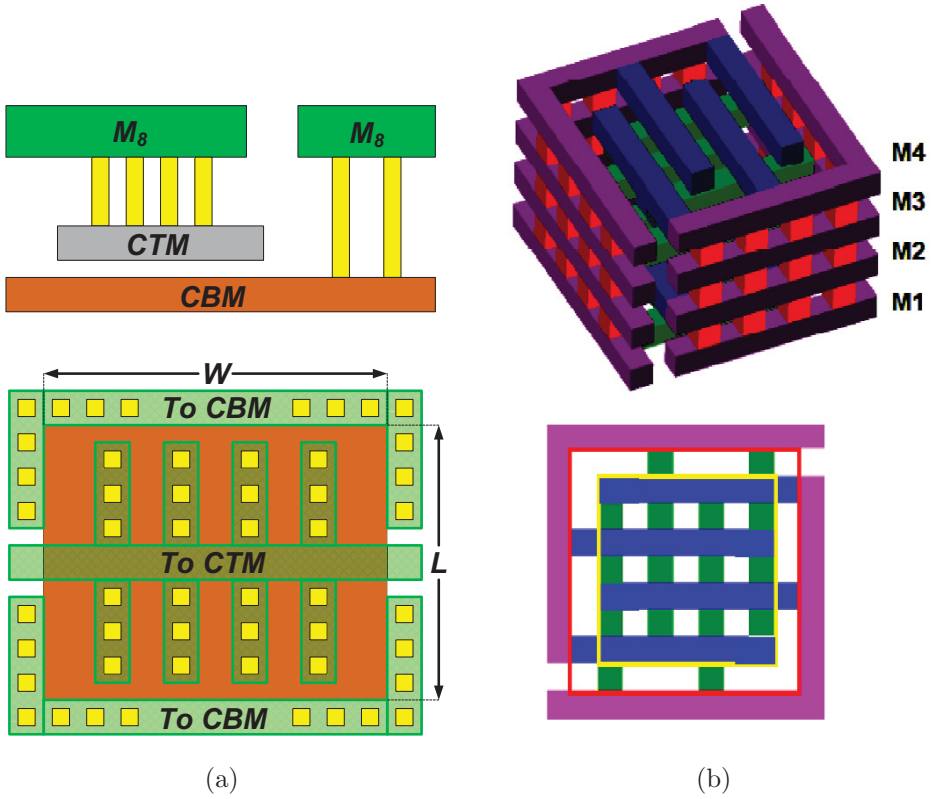


Figure 3.27: Layout cross-section of on-chip passive capacitors, (a) MOM capacitors (b) MIM capacitors.

on-chip inductor varies from 10 to 18 at 60 GHz.

To meet different purposes of circuit applications, various type of on-chip capacitors are available in CMOS technology. Three type of commonly used capacitors are MOS, Metal-Oxide-Metal (MOM) and Metal-Insulator-Metal (MIM) capacitors. MOS capacitors are basically developed using the gate-oxide junction capacitance. These capacitors have significantly high capacitance per unit area because of the very small gate-oxide thickness in modern CMOS technologies. However, they cannot be used in many RF applications because of the non-linearity, high temperature/process sensitivity and low breakdown voltage. The layout cross-section for MIM capacitors designed in 9 metal layer 65 nm CMOS standard technology are shown in Fig. 3.27(a). MOM capacitors are realized utilizing the metal interconnections. Basically, every pair of two metal lines can form the MOM capacitor. Although the parasitic capacitance between metal interconnections is increased with the dimension shrink-

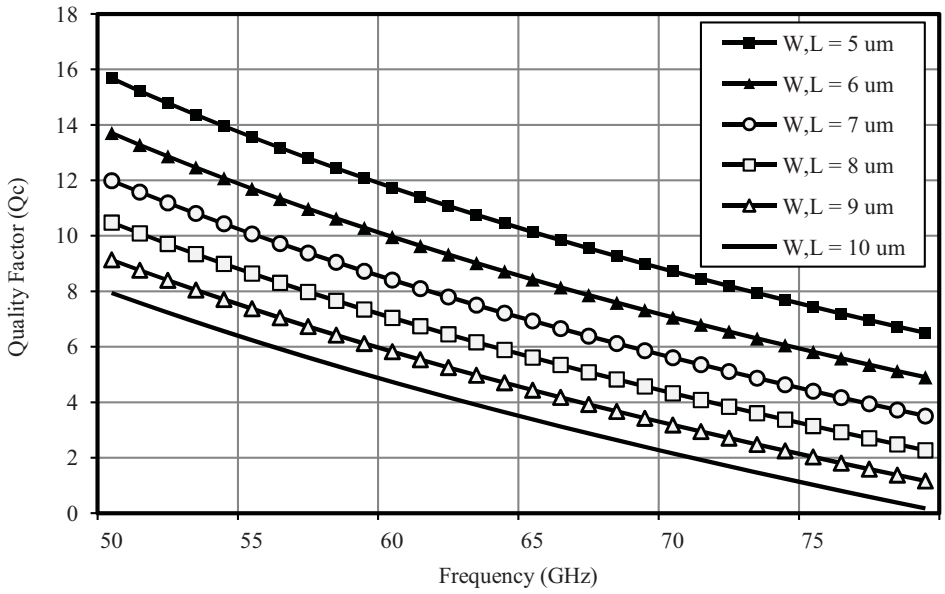


Figure 3.28: Quality factor of on-chip MIM capacitors.

age in advanced CMOS processes, still the capacitance density of MOM capacitor is very low compared to the two other solutions as a result of the lateral and vertical distances between metal layers.

Contrary to MoM capacitors, MIM capacitors can be formed using ultra thin metal layers (CTM and CBM) and high K dielectric, which are developed in modern CMOS processes for high quality capacitors. Because of the very short distance between two metal layers, MIM capacitors exhibit high capacitance density. Unfortunately, CTM and CBM layers are not directly accessible in a technology and high resistive vias and interconnections are required to connect these components to other part of the circuit. Hence, the quality factor of these on-chip capacitors, are typically low at mmW frequencies [103]. With the increasing frequency, the inductive impedances of the parallel plates become comparable to the impedance of the series capacitance which results in less total capacitance at higher frequencies. In addition, series resistance of the capacitor plates is increased with frequency because of the skin and proximity effects. The quality factor of several MIM capacitors ranging with plate sizes of $5\mu m \times 5\mu m$ to $10\mu m \times 10\mu m$ are plotted in Fig. 3.28. As shown, the quality factor of the MIM capacitors drop from 12 to 5 as the capacitor size is increased from 55 fF to 210 fF for the simulated structures. The relatively low quality factor of on-chip capacitors has a considerable impact on the power transfer efficiency of mmW power

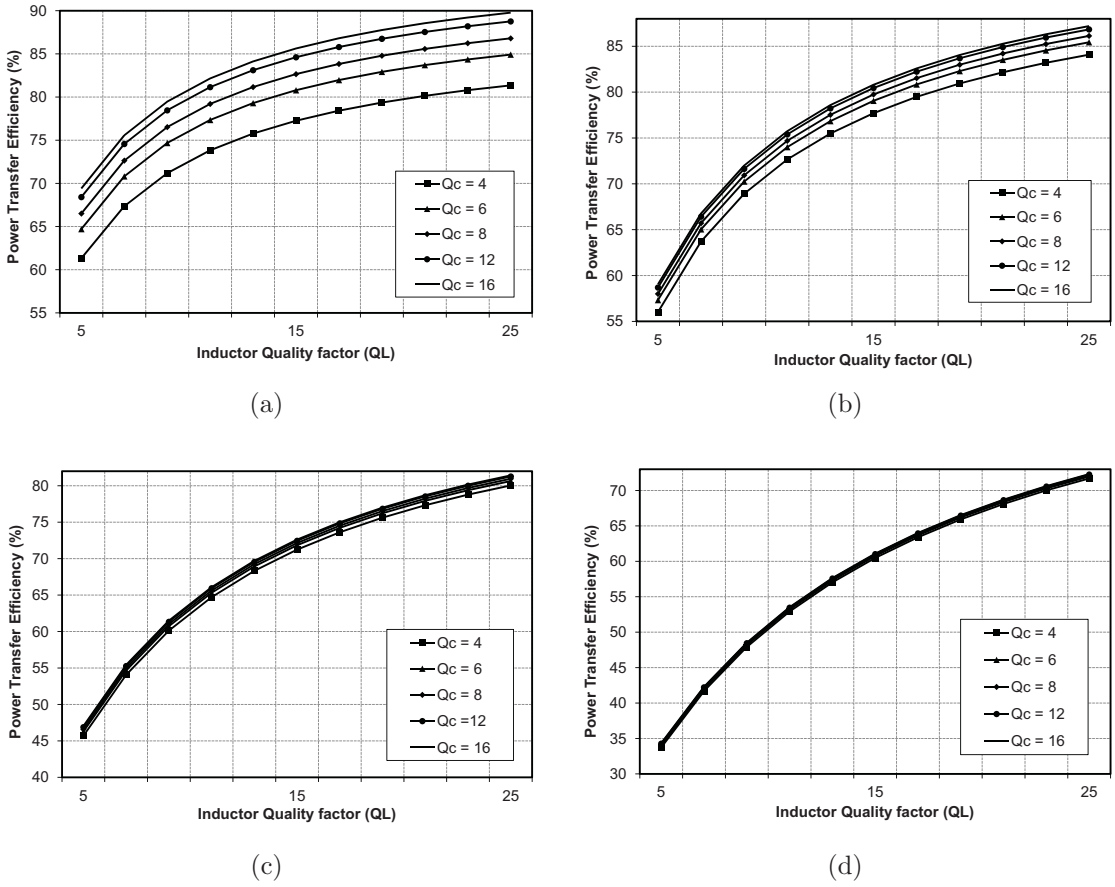


Figure 3.29: Power efficiency of LC matching network, (a) ITR of 2 (b) ITR of 5 (c) ITR of 10 (d) ITR of 20.

amplifiers.

Fig. 3.29 demonstrates a plot of power transfer efficiency for LC resonant matching circuits, calculated by 3.27. The input resistance is assumed to be 10 Ω and the load resistance changes from 20 Ω to 200 Ω to achieve various ITRs. The capacitor and inductor values are designed to perform the impedance transformation at 60 GHz with minimum reflection loss. The typical Q_L for mmW inductors is 15 in our target technology node. Hence, the efficiency of this LC matching circuit varies from 75% to 85% depending on the Q_C. Efficiency plots demonstrate that this LC matching circuit can be used for PA applications at mmW frequencies with certain considerations. One important parameter is the low quality factor of mmW capacitors which can cause a 20% drop in efficiency. For a large ITR, e.g. 200 Ω load, the power efficiency of a LC resonant matching circuit will be degraded to less than 40%.

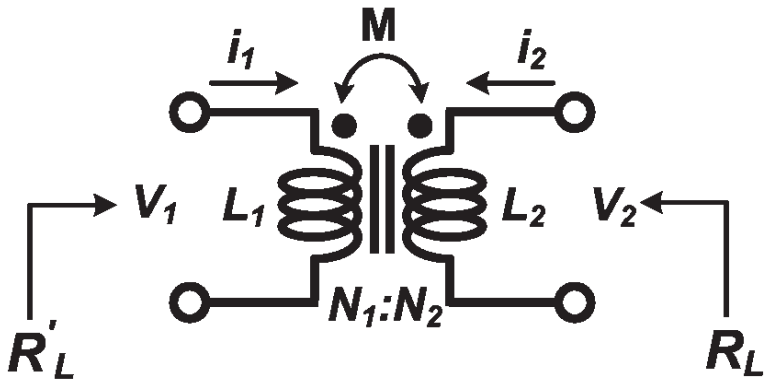


Figure 3.30: Ideal transformer model.

3.4.2 Transformer-based matching networks

Transformers have received significant attention at lower GHz frequencies, but their usage in mmW circuits design has not been analyzed so far. Microwave circuits usually utilize transmission lines to perform the impedance matching. However, using bulky transmission lines at 60 GHz is not area efficient and incurs higher cost than transformers. As the operating frequency increases, the required inductance can be reduced proportionally and transformers will be considerably more compact at mmW frequencies than transmission lines. The first advantage of transformers over LC matching circuits is the ability to overcome the ITR-efficiency tradeoff. They can simultaneously work as an RF choke to bias the MOSFETs. In comparison with transmission lines, they are area efficient at mmW frequencies. Also, they can be simply used to combine the output power of two differential amplifiers. These are the reasons why transformers have recently attracted interest from PA designers. Transformers are based on the principle of electromagnetic induction. In silicon, a transformer is implemented by two coupled inductors. In a coupled-inductor transformer, Fig. 3.30, the magnetic field created by the primary inductor L_1 generates a voltage in the secondary inductor L_2. At the same time, the current through the secondary winding (I_2) magnetically induces a voltage in the primary inductor. The voltage and currents illustrated in Fig. 3.30 are theoretically related to each other by

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & j\omega M \\ j\omega M & j\omega L_2 \end{bmatrix} . \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{3.33}$$

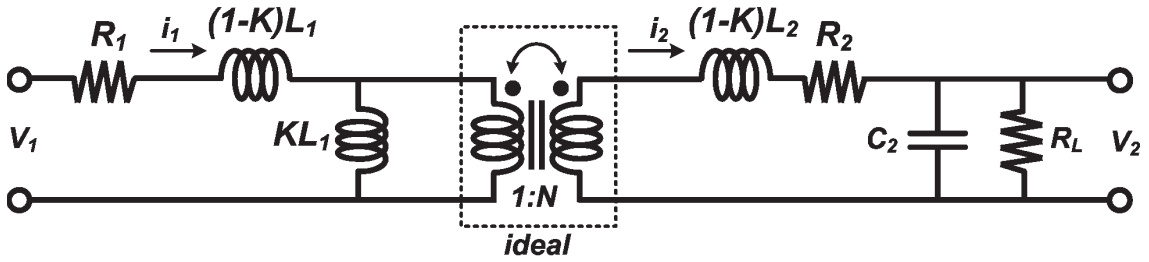


Figure 3.31: Simplified model of a transformer including loss of windings.

$$M = k.\sqrt{L_1 L_2}, \tag{3.34}$$

$$n = \frac{N_2}{N_1} = \sqrt{\frac{L_2}{L_1}} = \frac{I_1}{I_2} = \frac{V_2}{V_1}. \tag{3.35}$$

where, M is the mutual inductance, k is the coupling factor, and n is the turn ratio between the second and first windings [104]. Real transformers are not ideal because of the finite quality factor of the first and secondary inductors and the coupling factor of less than unity. In attempt to calculate the power efficiency of transformers for PA applications, a simplified model of a real transformer is proposed by [98] [100] shown in Fig. 3.31.

In Fig. 3.31, R_1 and R_2 represent the quality factor of the primary and secondary inductors, R_L is the load resistance and C_2 is the shunt tuning capacitor. The shunt capacitor-resistor (C_2, R_L) can be converted into an equivalent series circuit using the equations (3.36) and (3.37) as

$$R_{eq} = \frac{R_L}{1 + (\omega R_L C_1)^2}, \tag{3.36}$$

$$C_{eq} = \frac{1 + (\omega R_L C_1)^2}{\omega^2 R_L^2 C_1}. \tag{3.37}$$

To compare with other matching schemes, the power transfer efficiency η of a transformer is defined as

$$\eta = \frac{P_{load}}{P_{load} + P_{diss}}. \tag{3.38}$$

where P_{load} and P_{diss} are the power delivered to the load and dissipated in the parasitic

components of the transformer respectively. Calculating the P_{load} and P_{diss} using the theory of circuits and substituting into 3.38, an expression for efficiency can be found as

$$\eta = \frac{\frac{R_1}{1+(\omega R_L C_2^2)}}{\frac{R_2}{1+(\omega R_L C_2^2)} + R_2 + |\frac{Z_1 + j\omega k L_P}{j\omega k L_P}|^2 R_1}. \tag{3.39}$$

where Z_1 is the primary side impedance transformed into the secondary side as

$$Z_1 = \frac{R_1 + j\omega(1-k)L_1 + \frac{1}{j\omega C_{eq}} + R_{eq}}{n^2}. \tag{3.40}$$

The efficiency will be maximized when C_{eq} and L_1 resonate as in

$$\omega^2 L_2 C_{eq} = 1. \tag{3.41}$$

From the equivalent circuit, the optimum value for the primary winding can be calculated. Another way to find the optimum value of the inductors is by taking the derivative of the efficiency with respect to L_1 and set it to zero. This gives an optimum inductance value as

$$L_1 = \frac{\alpha}{1+\alpha^2}\frac{R_L}{n^2}\frac{1}{\omega}, \tag{3.42}$$

where,

$$\alpha = \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2}k^2}}. \tag{3.43}$$

Q_1 and Q_2 represent the quality factor of the primary and the secondary inductors respectively. Using this optimum inductance and writing the parasitic winding resistances using winding quality factor (Q), the optimum efficiency (η_{opt}) is

$$\eta_{opt} = \frac{1}{1 + \frac{2}{Q_1 Q_2 k^2} + 2\sqrt{\frac{1}{Q_1 Q_2 k^2}(1 + \frac{1}{Q_1 Q_2 k^2})}}. \tag{3.44}$$

Equation (3.44) shows that the passive efficiency (η_{max}) can be maximized using a k as close as possible to unity; a smaller k value results in a larger fraction of the primary inductor current I_1 going through the magnetizing inductor kL_1. This smaller k value reduces the power that is delivered to the load resistor. Moreover,

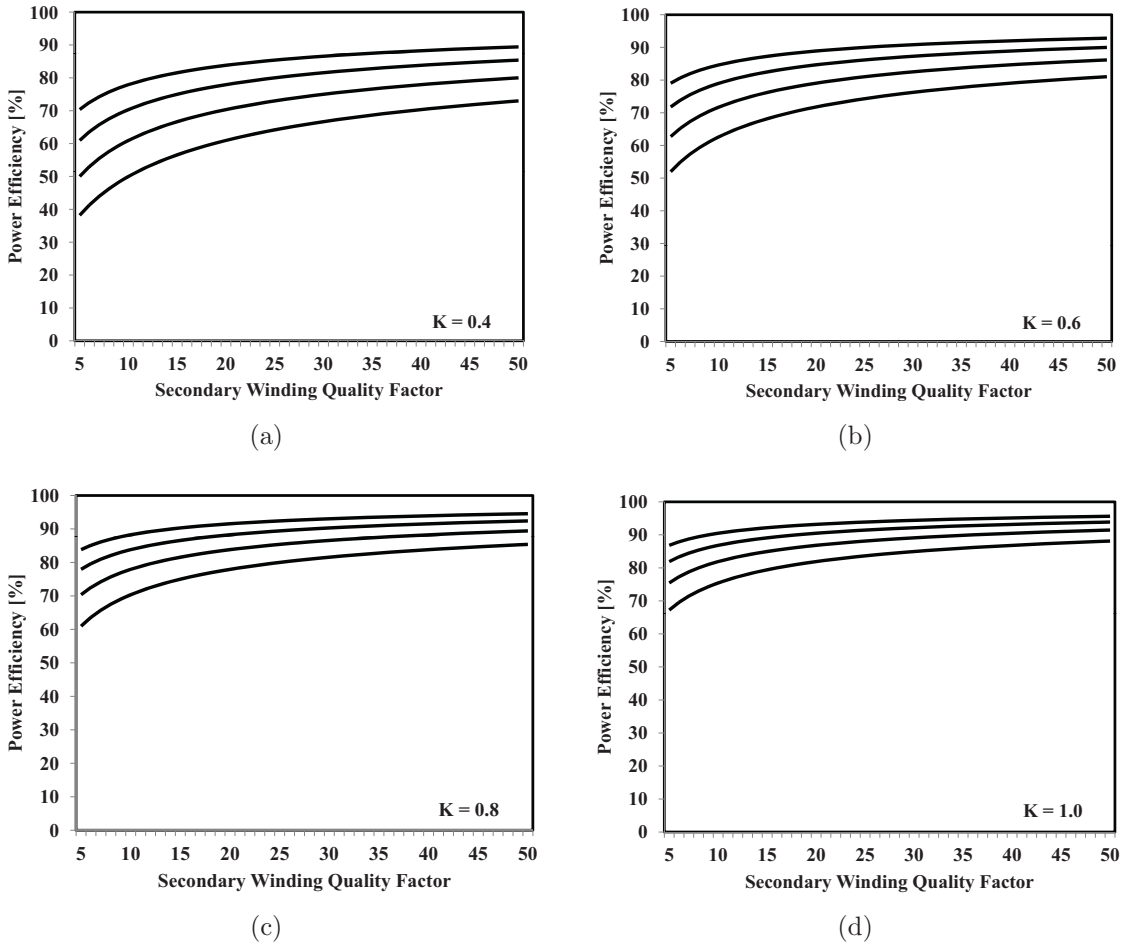


Figure 3.32: Power efficiency of transformers evaluated by (3.44) for different coupling factors of: (a) k=0.4; (b) k=0.6; (c) k=0.8; and, (d) k=1.0.

unlike the LC matching network, (3.44) shows that the transformer efficiency is not affected by the transformation ratio. The power efficiency of the transformer-based matching network is plotted in Fig. 3.32. The efficiency is calculated using the equation proposed by [98] for different Q_L and k. For coupling factor of unity the expression will be simplified to

$$\eta_{max} = \frac{1}{1 + \sqrt{\frac{12}{Q_1 Q_2}}}. \tag{3.45}$$

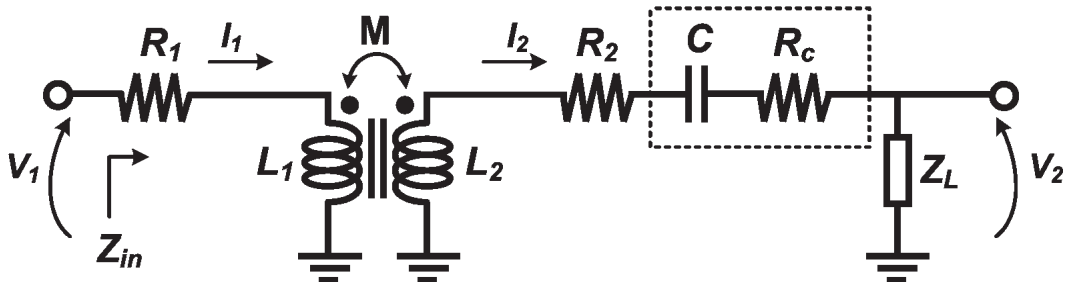


Figure 3.33: Proposed model for the transformer-based matching networks.

3.4.2.1 Proposed model for mmW transformer-based matching circuits

Transformers designed in CMOS technology have been individually measured and characterized at mmW frequencies since the last decade [86] [87]. Although the compact low frequency model for inductors were developed, a comprehensive analysis is required to calculate the power transfer efficiency of coupled inductors at mmW frequencies. A closed-form equation helps the designer to choose the best topology and perform the proper sizing as well as estimating the passive power transfer efficiency. The quality factor of inductors, coupling factor between windings, loading effect and the quality factor of tuning capacitors are the main parameters which are considered in proposed model of mmW transformer-based matching networks. From the reported measurements, mmW planar and stacked inductors have quality factors of greater than fifteen due to lower via resistance and higher effective inductance. The average coupling factor is reported to be 0.75 for both planar and stacked structures [86].

The efficiency of low frequency transformer can be estimated using equation 3.44, but tuning capacitors with low quality factor and the required ITR have a considerable impact on the passive efficiency which must be taken into account at mmW frequencies. Figure 3.33 illustrates the proposed model of mmW transformer-based matching networks. It uses a real transformer with tuning capacitor and lossy parasitic elements. The tuning capacitor is modeled as a series capacitor (C) with a finite quality factor of Q_C. The quality factors of the capacitor and the inductors are represented by series resistances R_C, R_1 and R_2 respectively. The voltages and currents at the input and output ports can be determined by Ohm's law as

$$V_1 = Z_{in} I_1 = (R_{in} + jX_{in}) I_1, \tag{3.46}$$

$$V_2 = Z_L I_2 = (R_L + jX_L) I_2. \tag{3.47}$$

The current-voltage equation of the transformer can be written as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & -j\omega M \\ j\omega M & -R_2 - j\omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{3.48}$$

where M is the mutual inductance between windings. The inherent resistance of the tuning capacitor and the resistance of the secondary inductor are in series. Hence, they can be merged into R_2 for simplicity. The tuning capacitor by itself can be considered as the imaginary part of the load (X_L).

It is necessary to evaluate the real part of the input and output impedances to calculate the active power applied to the input and received in the output. In order to find the real part of the input impedance (R_{in}), V_1 must be calculated with respect to I_1. Relation between I_1 and I_2 can be found as (3.49). Writing a KVL at the secondary and considering the relation between the current at the primary and secondary, the output voltage (V_2) can be written with respect to the I_1 as

$$I_2 = \frac{j\omega M}{Z_L + R_2 + R_C + j\omega L_2} I_1, \tag{3.49}$$

$$V_2 = Z_L I_2 = \frac{j\omega M Z_L}{Z_L + R_2 + R_C + j\omega L_2} I_1. \tag{3.50}$$

Substituting (3.49) and (3.50) into the expanded version of (3.48) gives an equation which demonstrates the input voltage with respect to the input current as

$$V_1 = (R_1 + j\omega L_1) I_1 - j\omega M \frac{j\omega M I_1}{Z_L + R_2 + R_C + j\omega L_2}. \tag{3.51}$$

The real and imaginary part of the (3.51) can be separated like in

$$\begin{aligned} V_1 = [R_1 + \frac{\omega^2 M^2 (R_L + R_2 + R_C)}{(R_L + R_2 + R_C)^2 + (X_L + \omega L_2)^2} + ... \\ ... + j(\omega L_1 - \frac{\omega^2 M^2 (X_L + \omega L_2)}{(R_L + R_2 + R_C)^2 + (X_L + \omega L_2)^2})]. I_1. \end{aligned} \tag{3.52}$$

The input resistance and reactance are extracted and simplified as

$$R_{in} = R_1 + \frac{\omega^2 M^2 (R_L + R_2 + R_C)}{(R_L + R_2 + R_C)^2 + (X_L + \omega L_2)^2}, \tag{3.53}$$

$$X_{in} = \omega L_1 - \frac{\omega^2 M^2 (X_L + \omega L_2)}{(R_L + R_2 + R_C)^2 + (X_L + \omega L_2)^2}. \tag{3.54}$$

The impedance transformation ratio (n) of the transformer is a key parameter for designers and can be found from (3.55) assuming that, $R_2 = R_C = X_L = 0$. Equation (3.55) shows that, unlike the expression shown in [98], the ITR depends on the load resistance. Hence, the efficiency of the transformer will be affected by the ITR calculated as

$$n = \frac{R_L}{R_{in}} = \frac{R_L^2 + (\omega L_2)^2}{(\omega k)^2 L_1 L_2}. \tag{3.55}$$

For power transfer efficiency calculations, it is necessary to demonstrate the input and output power with respect to the same current or voltage. Substituting the (3.52) into the well known power calculation expression, (3.56), gives the input power of the transformer as (3.57). For the ideal case where $R_2 = R_C = X_L = 0$, the input power can be calculated as

$$P_{in} = \frac{1}{2} Real \left\{ V_1 I_1^* \right\} = \frac{1}{2} R_{in} |I_1|^2, \tag{3.56}$$

$$P_{in} = \frac{R_L \omega^2 M^2 |I_1|^2}{(R_L + R_2 + R_C)^2 + (X_L + \omega L_2)^2}, \tag{3.57}$$

$$P_{in} = \frac{R_L \omega^2 k^2 L_1 L_2 |I_1|^2}{R_L^2 + (\omega L_2)^2} = \frac{R_L}{n^2} |I_1|^2. \tag{3.58}$$

Substituting (3.50) and (3.57), the power delivered to the load will then be

$$P_{out} = \frac{1}{2} R_L |I_2|^2 = \frac{R_L \omega^2 M^2 |I_1|^2}{(R_L + R_2 + R_C) + (X_L + \omega L_2)^2}. \tag{3.59}$$

The passive power transfer efficiency of the transformer (η) is determined as the power delivered to the load (P_{out}) over the total power entering the transformer (P_{in}),

given by

$$\eta = \frac{P_{out}}{P_{in}}. \tag{3.60}$$

Expanding (P_{out}) and (P_{in}) gives

$$\eta = \frac{R_L \omega^2 M^2}{[(R_L + R_2 + R_C) + (X_L + \omega L_2)^2]R_1 + (R_L + R_2 + R_C)\omega^2 M^2}. \tag{3.61}$$

To simplify, at the center frequency, the imaginary part of the load (X_L) and the secondary inductance (L_2) must resonate and cancel out each other as in

$$X_L = -\omega L_2. \tag{3.62}$$

Applying (3.62) to (3.61) gives the closed-form equation as

$$\eta = \frac{R_L \omega^2 M^2}{(R_2 + R_C + R_L)[R_1(R_2 + R_C + R_L) + \omega^2 M^2]}, \tag{3.63}$$

where,

$$R_1 = \frac{\omega L_1}{Q_{L1}}, \tag{3.64}$$

$$R_2 = \frac{\omega L_2}{Q_{L2}}, \tag{3.65}$$

$$R_C = \frac{1}{\omega C Q_C}, \tag{3.66}$$

$$M = k\sqrt{L_1 L_2}. \tag{3.67}$$

Using some mathematic operations, (3.63) can be simplified by multiplying the both nominator and denominator to $R_1 R_2$ as shown in (3.68). Then the expression can be simplified as

$$\eta = \frac{R_L}{R_L + R_2 + R_C} \frac{M^2 \omega^2}{R_1(R_L + R_2 + R_C) + M^2 \omega^2} \times \frac{R_1 R_2}{R_1 R_2}, \tag{3.68}$$

$$\eta = \frac{R_L}{R_L + R_2 + R_C} \frac{(M\omega)^2/(R_1 R_2)}{\frac{R_L+R_2+R_C}{R_2} + \frac{(\omega M)^2}{R_1 R_2}}. \tag{3.69}$$

The quality factor of the inductors (Q_1, Q_2) and the coupling factor (k) are the key parameters which can be utilized to design a transformer-based matching circuit. The nominator of (3.69) can be written as (3.70) with respect to the specifications of the primary and secondary inductors and finally gives

$$\frac{(\omega M)^2}{R_1 R_2} = k^2 Q_1 Q_2, \tag{3.70}$$

$$\eta = \frac{P_1}{P_2} = \frac{1}{1 + \frac{R_2+R_C}{R_L}} \frac{k^2 Q_1 Q_2}{k^2 Q_1 Q_2 + \frac{R_L+R_C}{R_2} + 1}. \tag{3.71}$$

Substituting (3.64) and (3.67) into (3.71), η can be written in terms of the quality factor of the circuit components as

$$\eta = \frac{k^2 Q_1 Q_2}{k^2 Q_1 Q_2 + (\frac{Q_2 R_L}{\omega L} + \frac{Q_2}{Q_C LC\omega^2} + 1)} \frac{1}{1 + \frac{\omega L/Q_2 + 1/Q_C \omega C}{R_L}} \times \frac{R_L/\omega L}{R_L/\omega L}. \tag{3.72}$$

At the center frequency, (when $LC\omega^2 = 1$), the loaded quality factor can be defined as $Q_{LD} = \omega L/R_L$ which is a parameter that depends on the size of the load resistance and is inversely proportional to the ITR. The larger the load resistance, the lower the loaded quality factor Q_{LD}. Substituting Q_{LD} into (3.72) gives

$$\eta = \frac{k^2 Q_1 Q_2}{k^2 Q_1 Q_2 + (\frac{Q_2}{Q_{LD}} + \frac{Q_2}{Q_C} + 1)} \frac{1}{1 + \frac{Q_{LD}}{Q_C} + \frac{Q_{LD}}{Q_2}}. \tag{3.73}$$

Assuming a fixed quality factor for the primary and secondary inductors at mmW frequencies, the closed-form equation for power efficiency of transformers can be obtained as

$$\eta = \frac{(kQ_L)^2}{(kQ_L)^2 + (\frac{Q_L}{Q_{LD}} + \frac{Q_L}{Q_C} + 1)} \frac{1}{1 + \frac{Q_{LD}}{Q_C} + \frac{Q_{LD}}{Q_L}}. \tag{3.74}$$

This equation is a function of the coupling factor (k), quality factor of inductors (Q_L), quality factor of capacitor (Q_C), and the loaded quality factor of the second winding (Q_{LD}). The proposed expression indicates the challenge of designing mmW

transformers. Although for typical values, (3.44) results in a passive efficiency of more than 95%, (3.74) shows that the efficiency also depends on the load/ITR and the tuning components, resulting in a much lower value. Figure 3.34 illustrates the passive power efficiency of the transformers at 60 GHz for different values of coupling factor (k), load resistance (R_L), and the quality factors (Q_L, Q_C, Q_{LD}). Efficiency plots demonstrate the significant impact of the lossy capacitor on the power transfer efficiency of transformers. By eliminating tuning capacitors, the power transfer efficiency of the proposed technique will be affected by only the coupling factor and the quality factors of primary/secondary windings as

$$\eta = \frac{1}{(\frac{1}{kQ_L})^2 + (\frac{1}{k^2 Q_{LD} Q_L}) + 1}. \tag{3.75}$$

Comparison of Figs. 3.34 indicate that the efficiency depends more on the quality factor of the capacitor and inductors than the value of k. The quality factor of the high frequency capacitors is a parameter which depends on the CMOS technology features: the number of thick metal layers, thickness of the dielectric and the distance between the metal layers. The coupling factor of the transformer also depends on the technology features. The fixed distance between top and bottom metal layers in a technology, and the minimum allowed distance between two metals in the same layer are the main factors that determine the coupling factor in a technology. The quality factor of windings are determined by the thickness, line width and sheet resistances of the metal layers. Technologies with thicker metal layers are the best choice for inductors. Various spiral and slab transformer topologies are well known and can be designed to produce an efficiency that is as high as possible.

Despite the potential for transformers to be very compact at mmW frequencies, for transformer based mmW design to be practical, it needs to be demonstrated that the insertion loss of transformers at these frequencies is small enough to be competitive with alternative solutions. Furthermore, a predictable and scalable modeling methodology must be developed for a specific technology based on the EM simulations. Basic active and passive devices have been implemented, modeled, and verified in CMOS technologies for RF and microwave frequencies. However, passive and active models for complex mmW devices like spiral transformers are usually not available in Process Design Kits (PDK). The substrate loss, thin lossy dielectrics between layers, distributed effects, and the sheet resistances of metal layers are the technology limita-

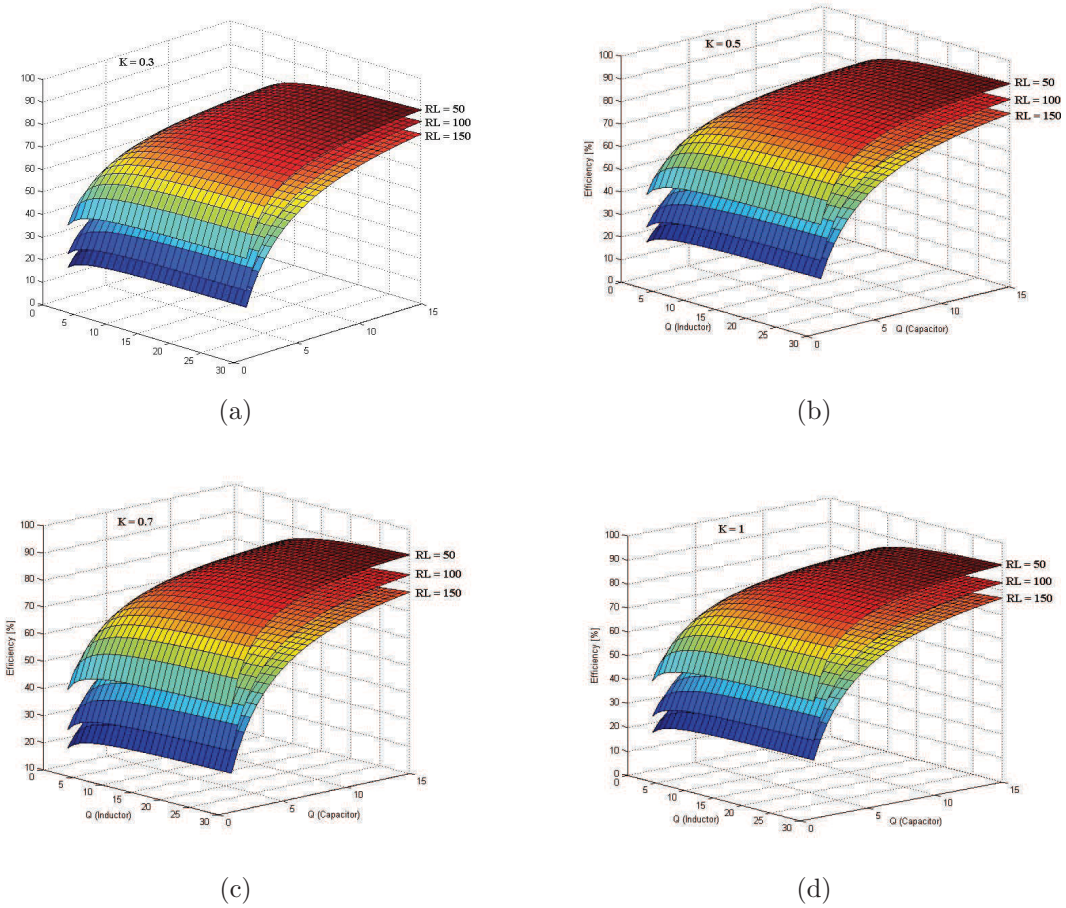


Figure 3.34: Power efficiency of millimeter wave Transformer based matching circuits, for different coupling factors of: (a) k=0.3; (b) k=0.5; (c) k=0.7; and, (d) k=1.0.

tions that make the models non-applicable for mmW design. A systematic approach based on EM simulations is the way for developing models at such high frequencies. Technology features and physical limitations are the basic information that must be known.

The cross-section of the 1P9M 65nm CMOS technology is shown in Fig. 3.14. There are two thick metal layers (M_9 as ultra thick and M_8 as thick) which are developed for design of transmission lines and on-chip inductors. The thickness and width of the metal layers are the parameters which determine the quality factor of the inductors while the gap between two layers determines the coupling factor between the two metal layers [104]. A smaller distance between the layers result in a higher coupling factor and a thicker layer will result in a higher quality factor [104].

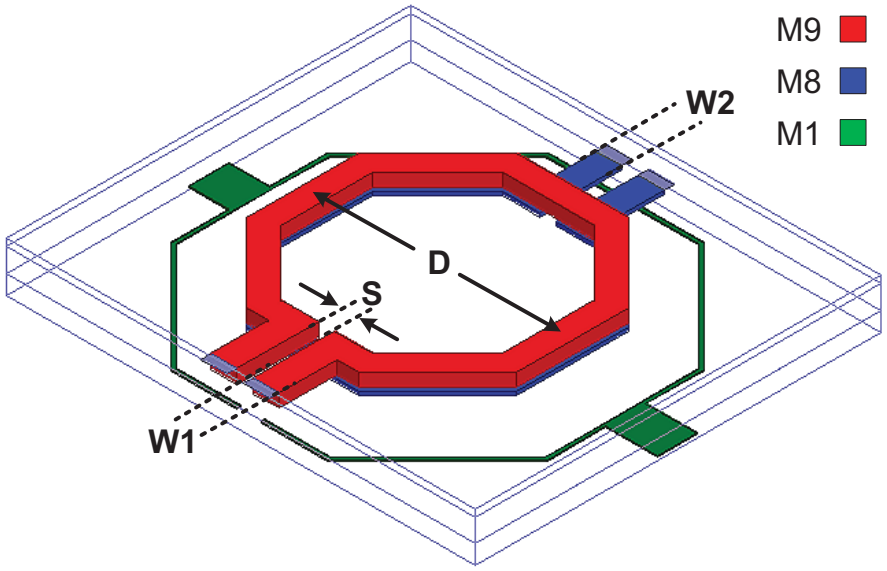


Figure 3.35: HFSS layout of stacked spiral transformer in 1p9M 65nm process.

Two traditional transformer topologies are the top-bottom (stacked) and side-side configurations. For both topologies, the thick metal layers are preferred to maximize the quality factor. Stacked spiral transformer topologies are area-efficient and extensively used for impedance matching purposes because of their low insertion loss [96]. The minimum distance between two metal lines on the same layer and the dielectric gap between two different metal layers are the technology limitations which limit the performance of mmW transformers. Another important parameter for designing mmW transformers is the Self Resonant Frequency (SRF). The performance of the transformer will be highly frequency and size dependent, since it operates at such high frequencies close to SRF [104].

Fig. 3.35 shows HFSS setup of octagonal spiral transformer implemented on top metal layers in 1P9M technology. To realize a transformer with maximum winding quality factor, a single turn transformer is preferable. Using multi-turn windings increases the wall-to-wall capacitance and decreases the effective inductance of windings but also increases the mutual inductance. Full 3D EM simulations are performed to evaluate the performance of the transformers in terms of the quality factor and the insertion loss. The large difference between the thicknesses of these layers (M_9 is four times thicker than M_8) poses a challenge for the design of mmW transformers in TSMC 1P9M CMOS process because it will produce a high mismatch between the

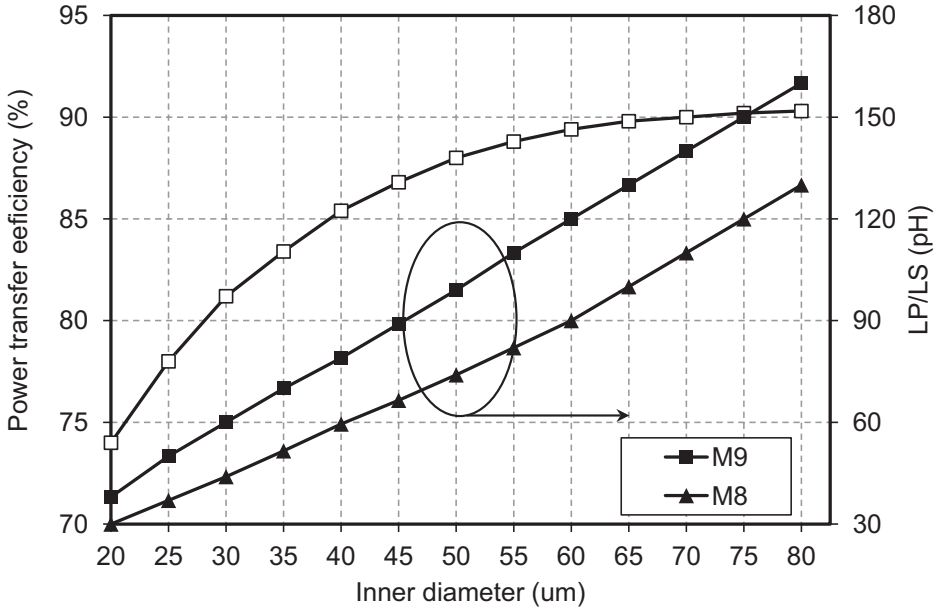


Figure 3.36: Simulated maximum power transfer efficiency and effective inductance on M_8 and M_9 metal layers versus inner diameter at 60 GHz.

primary and secondary windings. However, it can provide ITRs of higher than unity with single turn which results in less parasitics and area efficient design. The second challenging factor is the fixed M_9 to M_8 gap, which is five times greater than the M_7 to M_6. Although using the bottom metal layers (M_7 to M_6) gives more coupling, the small thickness of these layers reduces the quality factor and current handling capability of transformers.

Fig. 3.36 shows extracted efficiency and effective inductance of stacked transformers at 60 GHz with various inner diameters. The tail spacing (S) is 4 μm and the winding traces (W_1 and W_2) are set to be 6 μm. Diameter of the guard ring is kept 20 μm larger than the diameter of the transformer windings. Fig. 3.37 demonstrates the minimum insertion loss of stacked transformers versus the winding diameter.

By sweeping the inner diameter (D) from 20 μm to 80 μm, maximum efficiency of the transformer increases by 15%. The efficiency of the transformer can be calculated from the measured maximum available gain or insertion loss using (3.77) [105]. Using (3.79), primary and secondary self-inductances (L_P/L_S) are measured to be from 40 pH to 160 pH and 30 pH to 130 pH for windings implemented on M_9 and M_8 respectively. Achieving more self-inductance at mmW frequencies compared to lower

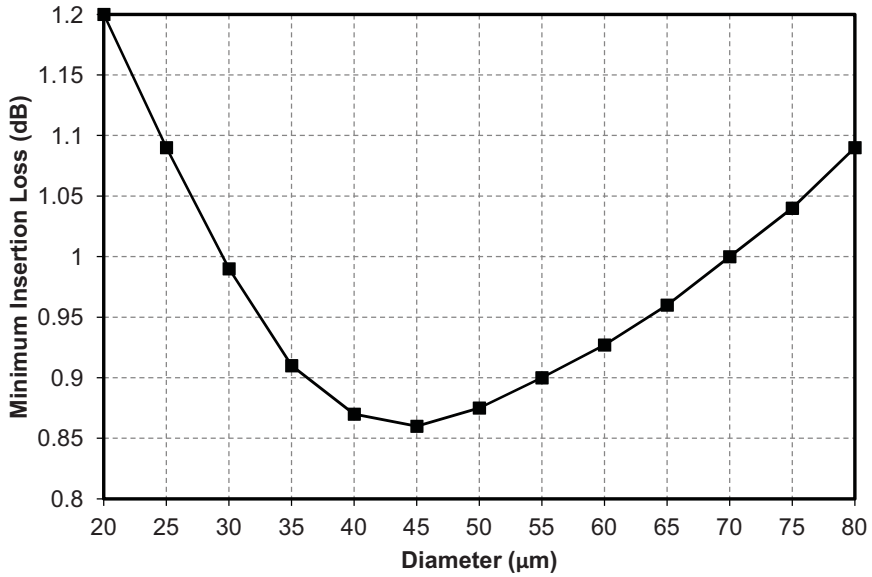


Figure 3.37: Minimum insertion loss of stacked transformers versus winding diameter.

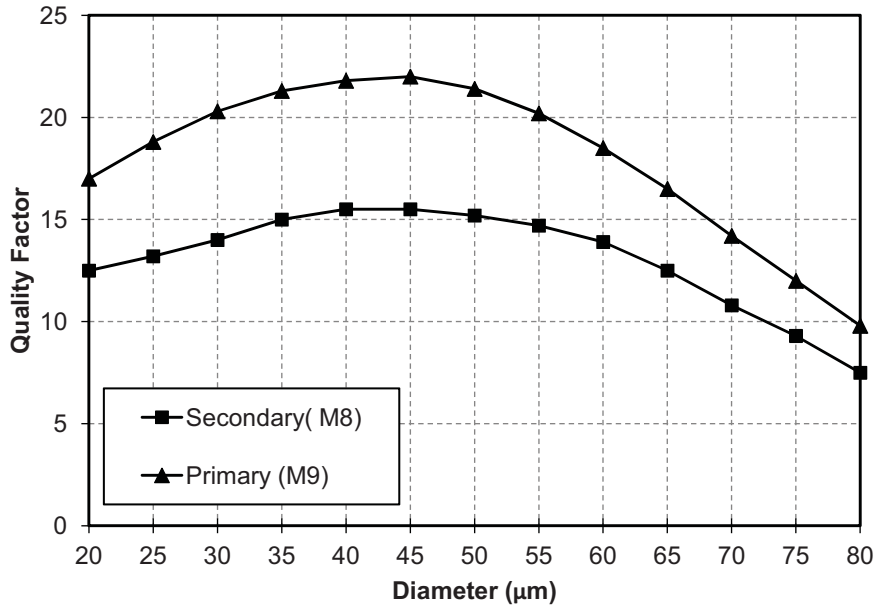


Figure 3.38: Quality factor versus diameter of the stacked transformer at 60 GHz.

GHz frequencies results in higher quality factor inductors. As shown in Fig. 3.38, the simulated maximum quality factors of 22 and 15 are found at 60 GHz using (3.80) for primary/secondary windings on M_9 and M_8 layers respectively. Increasing the winding

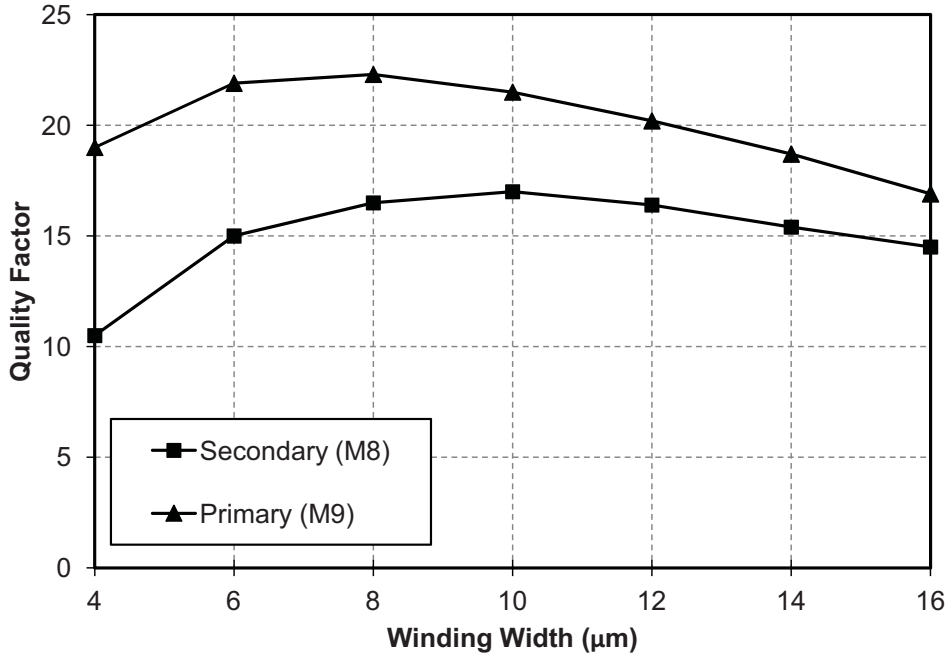


Figure 3.39: Maximum quality factor versus metal width of stacked transformer.

width of a transformer results in less conductive loss and higher winding quality factor. However, capacitive coupling of windings to the substrate and between layers increase simultaneously. Hence, the quality factor drops after reaching a maximum point. The other factor is the skin-depth effect that should be considered in finding the optimum metal width of the windings. Fig. 3.39 demonstrates the maximum quality factor of a single-turn stacked transformer with 40 μm diameter versus the winding width. Quality/coupling factors and effective inductances are extracted using simulated insertion loss as

$$IL_{max} = -10\log_{10}(G_{max}), \tag{3.76}$$

$$G_{max} = \eta_{max} = 1 + 2(x - \sqrt{x^2 + x}), \tag{3.77}$$

$$x = \frac{Re(Z_{11}).Re(Z_{22}) - [Re(Z_{11})]^2}{[Im(Z_{12})]^2 + [Re(Z_{12})]^2}, \tag{3.78}$$

$$L_P = \frac{Im[Z_{11}]}{\omega}, L_S = \frac{Im[Z_{22}]}{\omega}, \tag{3.79}$$

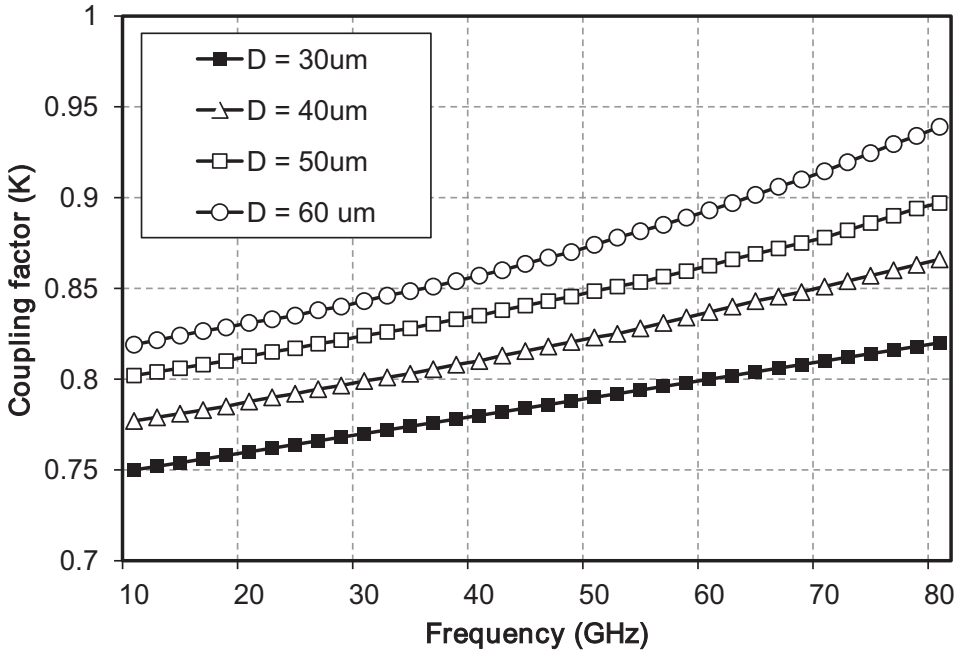


Figure 3.40: Extracted coupling factor for on-chip stacked transformers.

$$Q_P = \frac{Im[Z_{11}]}{Re[Z_{11}]}, Q_S = \frac{Im[Z_{22}]}{Re[Z_{22}]}. \tag{3.80}$$

Fig. 3.40 shows the effective coupling factor between windings, defined as

$$k = \sqrt{\frac{Im[Z_{12}]^2}{Im[Z_{22}].Im[Z_{11}]}}, \tag{3.81}$$

varies as a function of frequency for different inner diameters. Stacked transformer architectures exploit both the lateral and vertical magnetic couplings. The lateral magnetic coupling degrades at low frequencies in small sized mmW transformers so that the coupling factor and efficiency are reduced.

Fig. 3.41 illustrates the efficiency of stacked transformers fabricated in 65nm 1P9M technology over a wide frequency range. Simulation results indicate the benefit of using transformers for power combining as well as the impedance matching at mmW frequencies, due to high power transfer efficiency. However, the other important factor is SRF of the transformer which decreases by increasing the winding width and the diameter. Utilizing on-chip transformers operating close to their SRF increases the

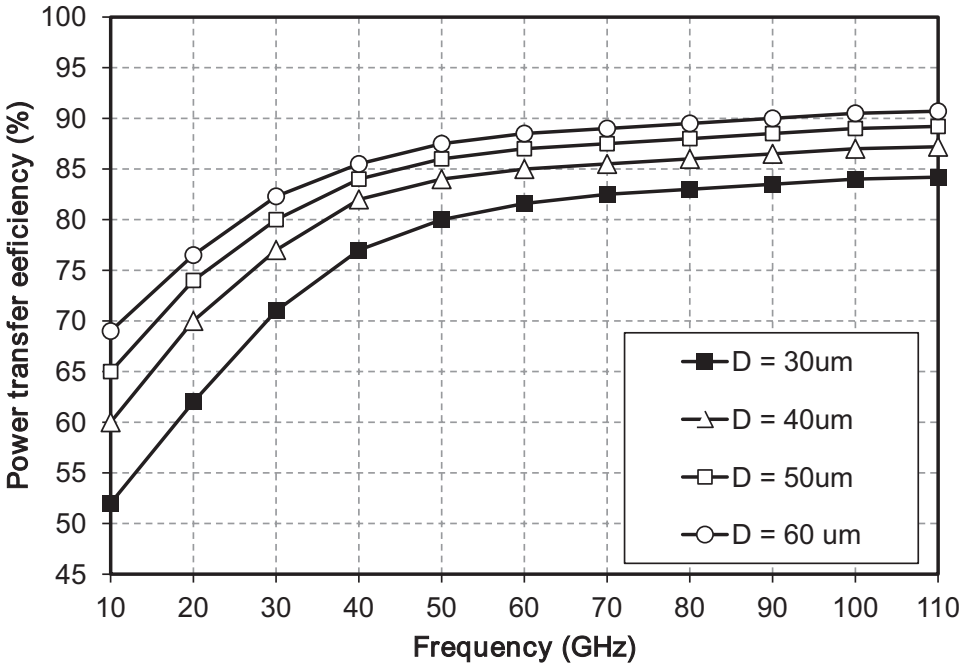


Figure 3.41: Power transfer efficiency of on-chip transformers with various diameters.

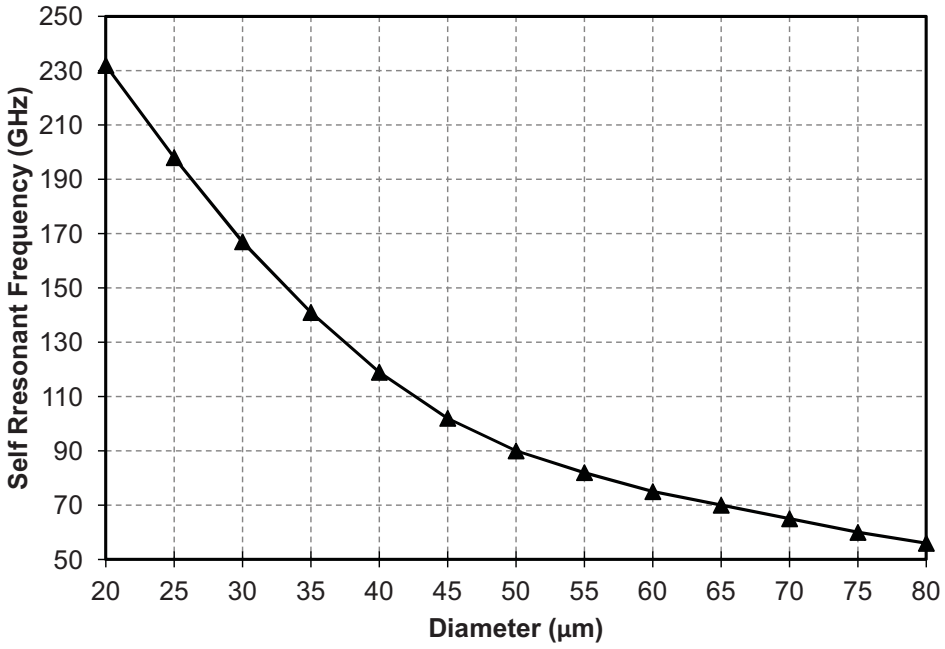


Figure 3.42: Self resonant frequency of stacked transformers versus winding diameter.

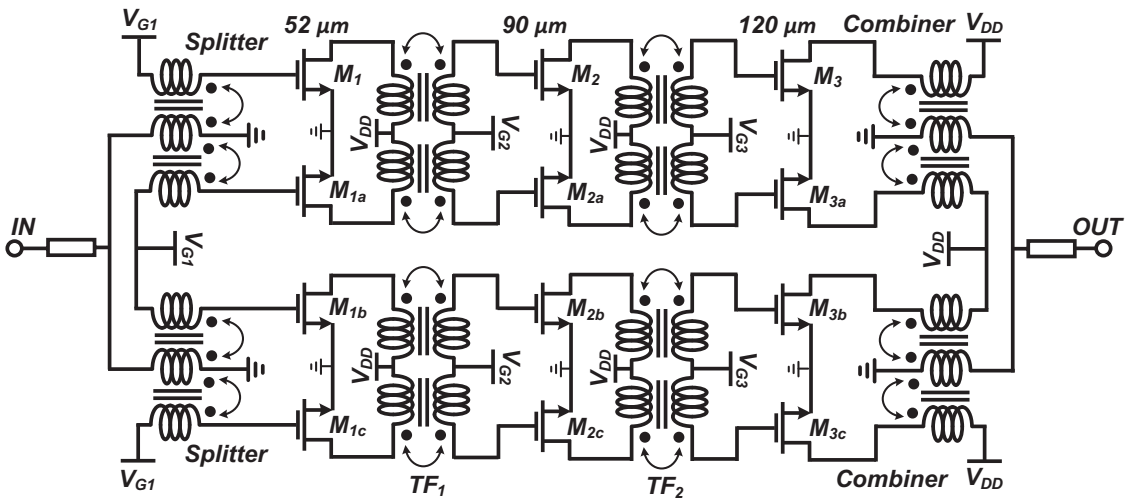


Figure 3.43: Circuit schematic of 60 GHz CMOS power amplifier.

possibility of oscillation and causes stability issues. Hence, transformers with large diameters and winding width must be avoided in amplifier design. so that the SRF of transformer will be less than its intrinsic value. Fig. 3.42 demonstrates the SRF of stacked transformers versus inner diameter. Although large transformers shows high efficiency, high quality factor and high coupling factor, they are not practical for power amplifier designs because of low SRF.

3.4.3 60 GHz PA simulations and measurement results

The schematic of the proposed 60 GHz CMOS power amplifier is presented in Fig. 3.43. The PA is a 4-way combined single-ended cascaded CS amplifiers. Power gain is increased using the driver stages and the gain stages cascaded before the main power stages. Transistor sizes for gain stages are designed to achieve the highest possible gain and linearity to drive the power stages. The power stage transistors are laid out in 30 fingers with 4 μm wide fingers. The optimum size for power transistors is chosen based on the load-pull and small-signal simulations provided in previous sections. As discussed in section 3.2, transistor with these sizes can provide 15 dBm output power when lossless components are used for I/O matching circuits. However, the actual output power will be less than this value considering the loss of interconnects, input matching circuit and the power combiner windings. NMOS transistors with 32 fingers, 1.6 μm and 2.8 μm wide are designed for driver and gain stages, respectively.

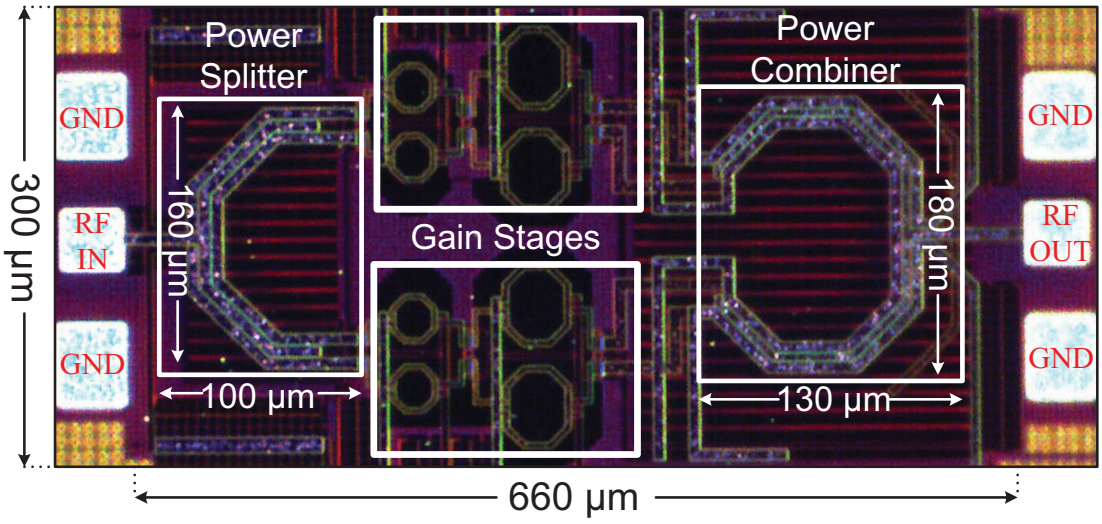


Figure 3.44: Chip micrograph of 60 GHz PA fabricated in 65nm CMOS technology excluding the DC PADs.

All the stages are biased in same conditions using on-chip transformer networks. The gate bias (V_{GG}) voltage is set to be 0.9 V while the supply voltage (V_{DD}) varies from 1 V to 1.6 V for all the stages. 60 fF MOM capacitors paralleled with 10 KΩ resistors are used to create AC grounded bias rails. For the first and second stages inter-stage matching circuits, stacked transformers are designed on the M_9 and M_8 metal layers with conductor width of 6 μm and radii of 15 μm and 25 μm respectively. Transformer sizes are optimized in order to offer maximum power gain by performing conjugate impedance matching between driver and gain stages. Using the M_8 and M_9 metal layers in stacked configuration, an average coupling factor of 0.7 is achieved at 60 GHz. The I/O capacitive parasitics of the transistors are taken into account when tuning the transformers. As a result, tuning capacitors are avoided which is desirable because of their low quality factors at mmW frequencies. A power splitter based on the proposed combiner architecture is designed at the input to divide the input power into four amplifier cores. The proposed splitter architecture could perform the impedance matching of the first gain stages simultaneously. For the very low ITR required at the input, 130μm length splitter can split the input power with achieved power efficiency as high as 85%. This results in a higher efficiency compared to using a lossy and non-area efficient Wilkinson power divider.

The proposed 60 GHz PA is fabricated in a 1P9M 65nm standard CMOS process.

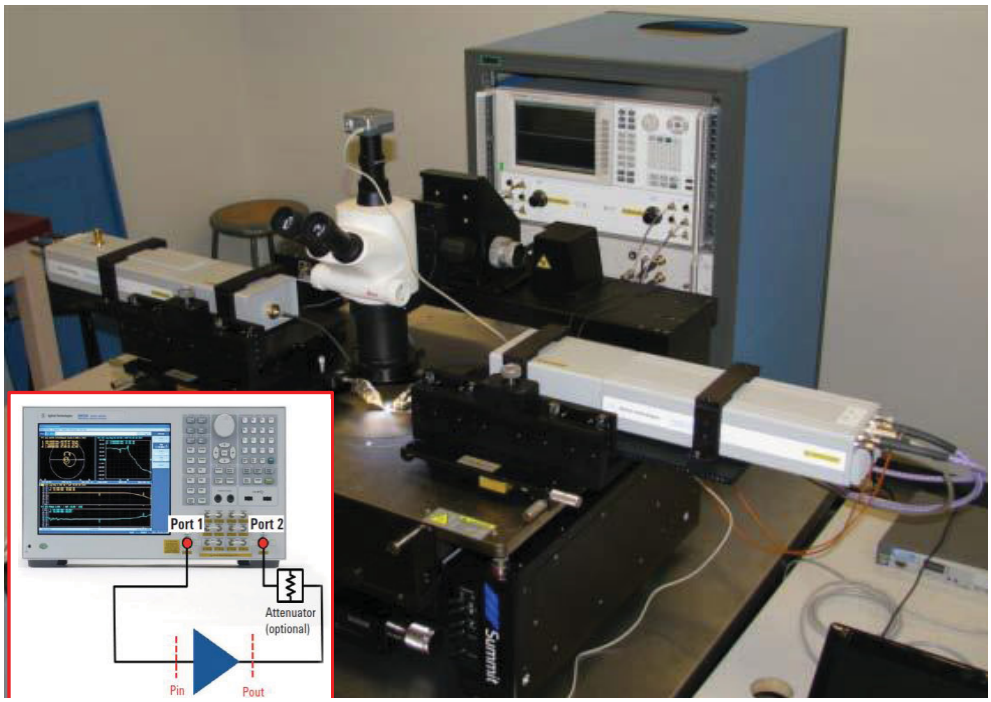


Figure 3.45: Test setup for small-signal measurement using Agilent 110 GHz solution.

The chip micrograph of the PA is shown in Fig. 3.44. Due to the absence of bulky transmission lines, the PA only occupies a core area of 0.19 mm^2 using the proposed area-efficient power combiner and splitter. Considering all the RF/DC pads, MOM capacitors and DC supply rails, the design occupies the total area of 0.42 mm^2. The ground plate is distributed in all areas on the chip using M_1 and M_2 layers to minimize the resistive/inductive parasitics of the ground connections. Finally, all ground planes are connected to the substrate using contact vias. The S-parameter measurements are performed using Agilent N5251A Vector Network Analyzer (VNA) solution which uses an E8361 Performance Network Analyzer (PNA), millimeter wave test controller and broadband frequency extenders. Fig. 3.45 demonstrates the test setup for small-signal measurements of the 60 GHz PA.

The measured S-parameters are compared with the simulation results as shown in Fig. 3.46. Applying 1.4V supply, maximum power gain of 18.8 dB at 60 GHz and 3dB bandwidth of 4 GHz (58 to 62 GHz) are measured. The PA operates functional inside the IEEE802.15.3c band and it offers minimum power gain of 10 dB at 67 GHz. The input matching demonstrates -20 dB return loss whereas the S_{22} is measured to be -10 dB. The PA offers a good performance in terms of the output matching with

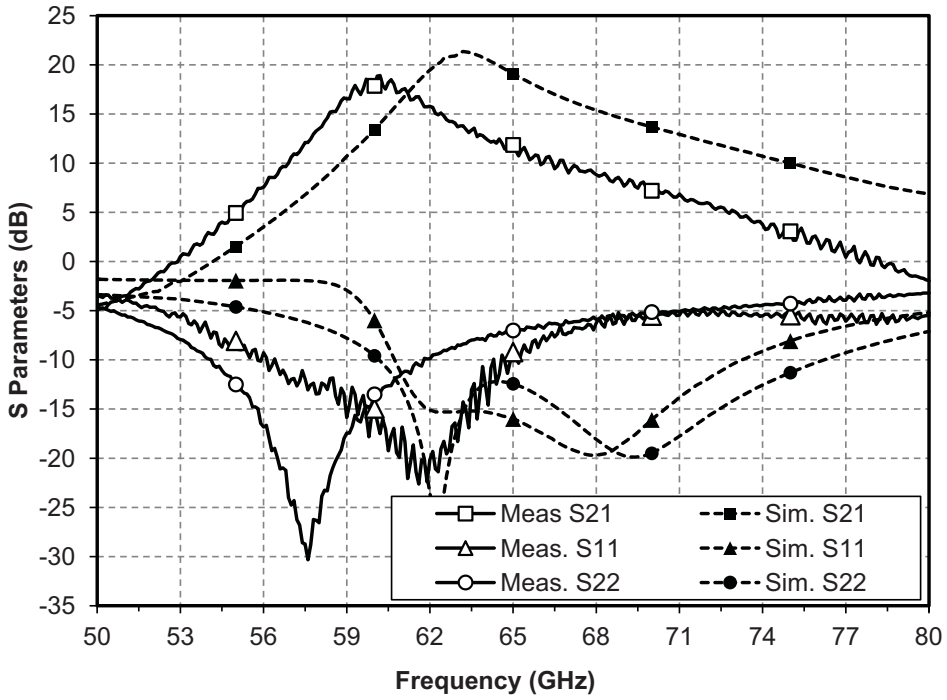


Figure 3.46: Measured and simulated S-parameters at the bias point $(V_G, V_{DD}) = (0.9V, 1.4V)$.

minimum S_{22} of -30 dB whereas the S_{11} is measured to be -13 dB. With the measured stability factor of greater than unity, the amplifier is unconditionally stable over the frequency range of operation. Compared to the simulation results, a 3 GHz frequency shift is observed in measured results probably because of the inaccurate models of MOSFETs at 60 GHz.

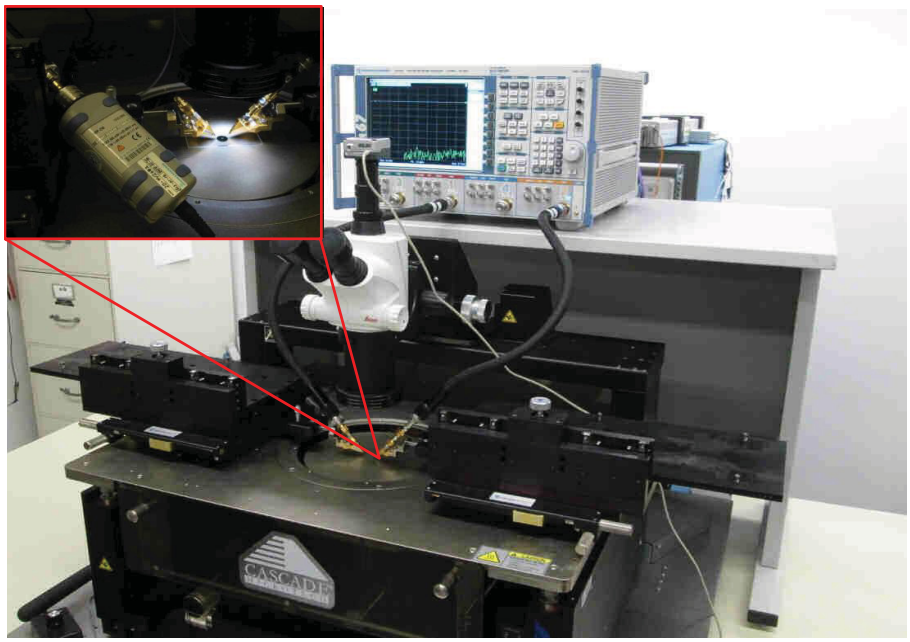


Figure 3.47: Large-signal measurement setup using Rohde-Schwarz VNA.

Large-signal measurements are performed using Rohde-Schwarz NRP-Z power sensors and the Rohde-Schwarz ZVA67 VNA inside the 60GHz band as shown in Fig. 3.47. The measured results summarizing the PA power characteristics are shown in Fig. 3.48. The PA is matched to the input/output impedance of 50 Ω. The supply voltage is slightly higher than the standard voltage (1.2 V) to guarantee the class A operation and keep the devices inside the saturation region. With 1.4V supply voltage, the saturated output power of 18.3 dBm is measured whereas peak PAE is measured to be 15.9% at 60 GHz. The PAE has a value close to its maximum when the amplifier reaches the compression. It still presents PAE of 10 % at 6 dB back-off. Compared to the reported 60 GHz PAs, the proposed PA is smaller in size for comparable higher output power while improving the linearity based on the measured 16.9 dBm 1dB compression point. Due to the large transistors used for driver and gain stages, the compression point is very close to the saturation point which proves the high linearity performance of the PA. However, the efficiency could be improved by decreasing the size of the driver stages and reducing the DC power consumed by driver stages.

Large-signal performance of the PA is measured at various bias points over six different frequencies inside the IEEE802.15.3c band. The supply voltage is swept

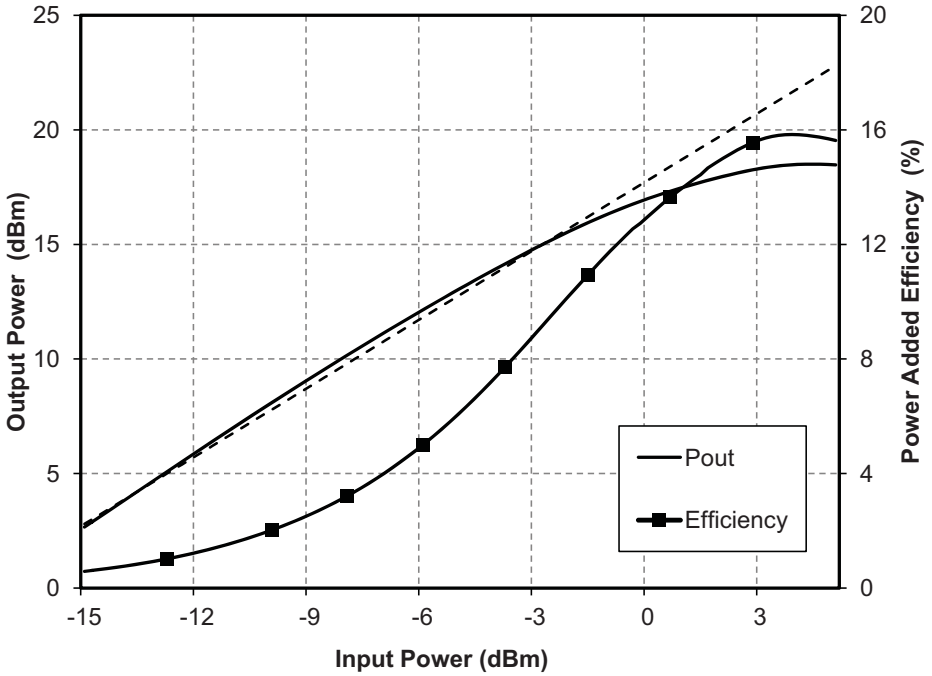


Figure 3.48: Measured output power and efficiency performances of the 60 GHz PA at the bias point $(V_G, V_{DD}) = (0.9V, 1.4V)$.

from 1.0V to 1.6V to increase the current density of the PA stages. output power of the PA for different levels of supply voltages are presented in Fig. 3.49. The PA maintains the 15dBm output power inside the IEEE mmW band which satisfies the specifications for short-range communication applications. The power gain and efficiency performances are also measured over the IEEE802.15.3c band at various bias points. Using 1.0V supply, an average power gain and PAE of 11 dB and 10% are measured over the frequency band as shown in Fig. 3.50 and Fig. 3.51 respectively. Although the PA exhibits positive power gain for all channels, its performance drops when it reaches the bandwidth boundaries because of the huge gain reduction. The reason is probably the low bandwidth of the proposed power combiner. The amplifier is optimized to operate at high current densities so that the measured performance is marginally acceptable when the supply voltage decreases to 1.0 V.

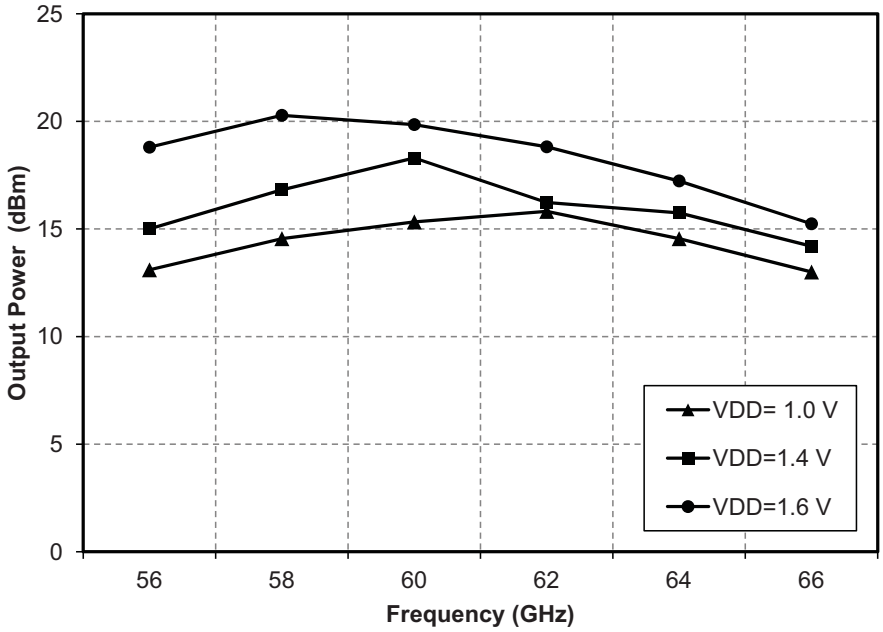


Figure 3.49: Measured output power of the PA at various bias points inside IEEE802.15 band.

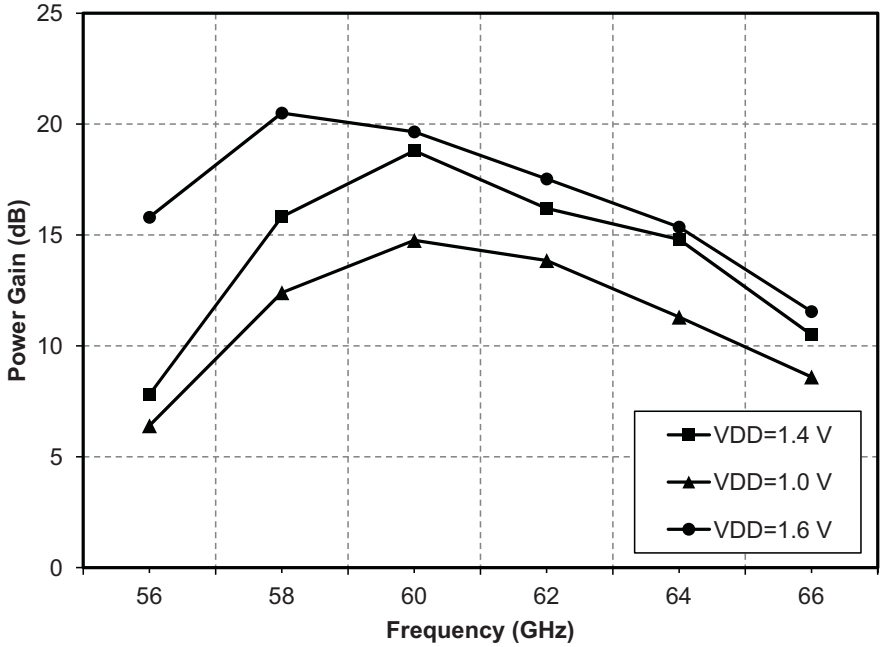


Figure 3.50: Measured power gain of the PA at various bias points inside IEEE802.15 band.

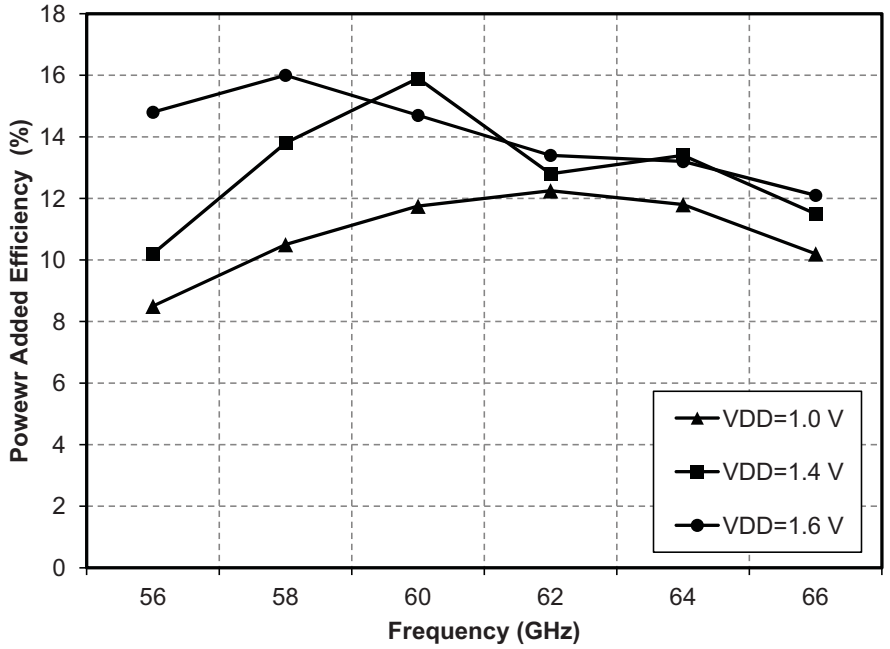


Figure 3.51: Measured efficiency of the PA at various bias points inside IEEE802.15 band.

3.5 Summary

This chapter presented design flow of a 60 GHz PA introducing a new multi-conductor power combiner topology. The proposed topology provides power combining of four individual PA stages as well as the impedance matching and DC biasing. Using the proposed parallel combining method, PA stages demonstrate significant improvement in output power and efficiency based on EM simulations. A comparison of performances of the fabricated PA with 60 GHz PAs reported in literature is presented in Table. 3.2 based on the ITRS [1] FoM. Presented in [106], the proposed class-A PA delivers output power of 18.3 dBm at maximum PAE of 15.9%. Compared to other PAs in 65nm CMOS, the compact new power combining method provides higher output power per unit area on chip. Also, the amplifier exhibits high linearity with a measured P_{1dB} of 16.9 dBm. Although the bandwidth of the PA is narrow probably because of the combiner parasitics, the PA is functional and satisfies specifications of 60 GHz WiGig.

Table 3.2: Performance comparison of 60 GHz PAs in 65nm CMOS technology.

V_{DD} [V]	B.W [GHz]	Stages	Mode	Topology	Combiner	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	Size [mm^2]	mW/mm^2	FoM	Reference
1.4	4	3	s	cs	4x	18.3	16.9	18.8	15.9	0.19	356	85	T.W
1.0	6	3	d	cs	2x	17.8	13.8	11	12.6	0.28	215	75	[62]
2.4	9	2	s	cs	2x	15.4	13.7	17.2	14.3	0.25	139	79	[53]
1.8	7	4	d	cs	4x	15.6	13.5	20	6.6	2.25	16	79	[55]
1.0	8	3	d	cs	-	11.5	2.5	15.8	11	0.05	283	73	[51]
1.0	10	2	d	cs	4x	17.9	15.4	18.8	11.7	0.83	74	83	[52]
1.2	15	2	b	cs	8x	18.1	11.5	15.5	3.6	0.46	140	74	[54]
1.2	6	3	d	cs	-	14.6	10	23.2	16.3	0.6	48	85	[60]

[1] FoM = P_{sat}[dBm] + G_P[dB] + 20 log(f_c[GHz]) + 10log(PAE_{max}[%]).

Chapter 4

60 GHz Dual-Mode Highly Efficient PA

This chapter discusses design procedure of a 60 GHz power amplifier using a new circuit technique to achieve high efficiency at high output power levels. The proposed topology provides the capability of dual-mode amplification. The output power of a conventional Class-A power amplifier will be combined with the power provided by an amplifier operating in a non-linear class to achieve high efficiency at high output levels. Driver stages are used to provide high power gain and consist of an enhanced cascode stage followed by a common source amplifier with transformer-based inter-stage impedance matching networks. The PA is fabricated in 65 nm CMOS technology. The functionality of the PA is proven based on simulations and measured results. The overall performance of the proposed 60 GHz PA is compared with the reported PAs in literature which target the 60GHz WPAN standard.

4.1 Dual-mode Power Amplification

As discussed earlier, P_{sat} and PAE are two key parameters in designing of 60 GHz PAs. Power combining techniques have been used as a solution to improve the output power of a PA. However, they cause additional losses limiting the maximum PAE of CMOS PAs. DC power consumption of driver stages is another important factor which decreases the overall PAE. One possible solution to overcome the PAE tradeoffs is to design PAs in non-linear classes for mmW applications [107] [108]. In spite of a significant improvement in PAE by operating in non-linear classes, these PAs are

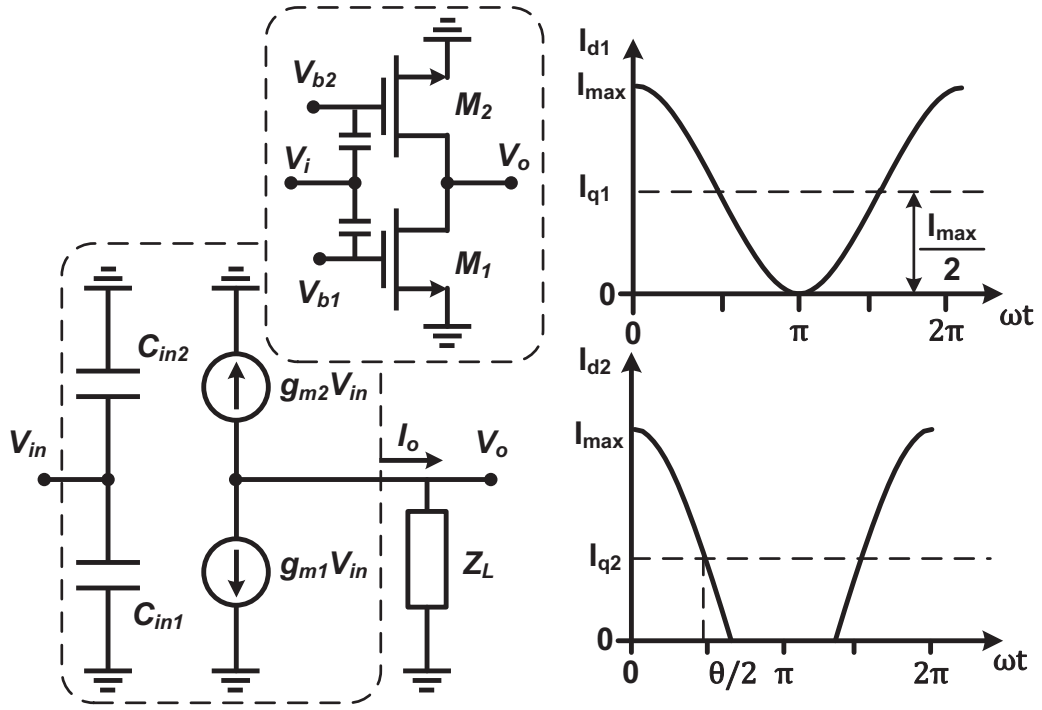


Figure 4.1: Circuit model and output current waveforms of the proposed dual-mode amplification topology.

usually avoided because they need MOSFETs to be in OFF state for a portion of time which lowers the maximum available RF power. Meanwhile, low current density of non-linear PAs decreases the f_{max} and gain of power MOSFETs dramatically. Hence, non-linear PA classes cannot use wide-channel transistors. In order to achieve high power efficiency for the PA stage, a new topology based on the dual-mode operation is proposed. Fig. 4.1 shows the basic idea of the dual-mode technique using ideal model of MOSFET devices. The proposed circuit consists of two MOSFET amplifier units which are modeled as parallel current sources. The effects of the output impedance of the MOSFETs are neglected at this step for simplicity and MOSFETs are considered as ideal Voltage Controlled Current Sources (VCCS). Although the performance of the practical circuit depends on the high frequency parasitics, but parasitic effects can be neglected here to prove the idea of dual-mode power amplification. Additional matching circuit will be designed at final step to resolve the impedance mismatch problems. The main amplifier (M_1) provides a linear class A operation. An auxiliary amplifier (M_2) is added to provide a tunable class of operation by changing the

conduction angle.

The conduction angle is tunable using an independent bias rail for amplifier M_2. Fig. 4.1 illustrates the current wave forms for the basic idea of the dual-mode operation. The output current is the summation of two independent current sources. Forcing the main amplifier to operate in class A mode, results in the highest possible output RF power and linearity. The second amplifier can be biased to inject more power when higher output power is required and M_1 reaches the saturation. Assuming a pure sinusoidal voltage at the input, the V-I function of two amplifiers can be written as

$$V_{in} = V_i \ cos(\omega t), \tag{4.1}$$

$$I_1 = g_{m1} \ V_i \ cos(\omega t), \tag{4.2}$$

$$I_2 = \begin{cases} g_{m2}.V_i.cos(\omega t) & -\theta \leqslant \omega t \leqslant \theta \\ 0 & -\pi \leqslant \omega t \leqslant -\theta, \theta \leqslant \omega t \leqslant \pi \end{cases}. \tag{4.3}$$

where θ is the conduction angle of the auxiliary amplifier. The DC and fundamental values of the output current must be calculated to derive an equation for power efficiency of the proposed method. To simplify the equations, the parameter $\alpha = g_{m1}/g_{m2}$ can be defined as the gain ratio of two amplifiers. The normalized output power can be calculated assuming a resistive load and maximum output voltage swing of unity. The DC value of the output current can be calculated by

$$\begin{aligned} I_{o,DC} &= \frac{1}{2\pi}\int_{-\pi}^{\pi} g_{m1}V_i cos(\omega t)dt + \frac{1}{2\pi}\int_{-\theta}^{\theta} g_{m2}V_i cos(\omega t)dt \\ &= \frac{I_{max}}{2\pi}\left[\pi + \alpha\left(\frac{sin(\theta/2) - \theta cos(\theta/2)}{1 - cos(\theta/2)}\right)\right]. \end{aligned} \tag{4.4}$$

Efficiency of the PA can be directly calculated as a function of output current for a unity supply voltage. The fundamental or RF component of the output current can

be calculated using

$$\begin{aligned} I_{o,RF} &= \frac{1}{2\pi}\int_{-\pi}^{\pi} g_{m1}V_i cos(\omega t)cos(\omega t)dt+ \\ &\quad \frac{1}{2\pi}\int_{-\theta}^{\theta} g_{m2}V_i cos(\omega t)cos(\omega t)dt \\ &= \frac{I_q}{2\pi}\left[\pi + \alpha\left(\frac{\theta - \theta sin(\theta)}{1-cos(\theta/2)}\right)\right]. \end{aligned} \tag{4.5}$$

For the main amplifier, the quiescent point is located at the center of the load-line resulting in the maximum available power. The drain efficiency of the power amplifier can be calculated as the ratio of the output RF power to the consumed DC power. Using the current relations, the efficiency of the dual-mode amplifier is given by

$$\eta = \frac{\pi\left(1-cos\left(\frac{\theta}{2}\right)\right) + \alpha\left(\theta - sin(\theta)\right)}{2\pi\left(1-cos\left(\frac{\theta}{2}\right)\right) + \alpha\left(sin(\frac{\theta}{2}) - \theta cos(\frac{\theta}{2})\right)}. \tag{4.6}$$

Fig. 4.2 illustrates the efficiency-power tradeoff of the proposed topology as a function of conduction angle for different gain ratios (α). Utilizing the new topology, the auxiliary stage can deliver more RF current when the main stage runs into the saturation mode. In comparison with the same size conventional Class-A topology ($\alpha = 0$), higher power and higher efficiency (78%) is achievable using the proposed dual-biased PA as demonstrated in Fig. 4.2.

The other advantage of the proposed topology is the capability of tuning the auxiliary stage to operate both in the linear and non-linear modes of operations. This can be realized by changing the transistor's gain ratio and gate biasing of the auxiliary unit from zero to V_{DD}. Setting the gate biasing of the auxiliary transistor to be slightly above threshold voltage (V_T) enables the operation of auxiliary transistor M_2 as a Class-AB PA that results in injection of extra output power with better power efficiency than that of a Class-A PA. For very low input power levels, the auxiliary transistor still operates as a Class-A PA as it is ON for the whole signal cycle. As the input power increases, the auxiliary transistor is ON only for a portion of signal cycle. Hence, it injects additional output RF power in class AB mode proportional to the input power and the transistors' channel-width.

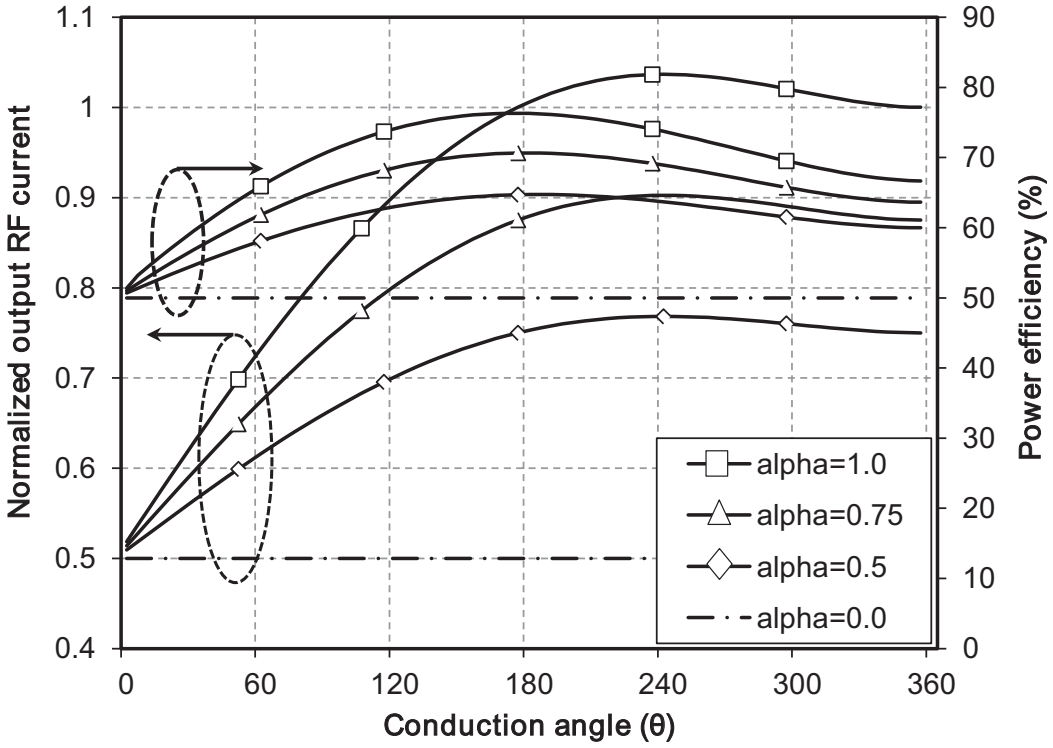


Figure 4.2: Dual-mode amplification power and efficiency performance.

4.2 Design of Three-Stage 60 GHz Dual-Mode Differential PA

In this section, the methodology of designing a 60 GHz PA stages in 1P9M 65 nm technology are discussed. The schematic of the proposed 60 GHz CMOS power amplifier is presented in Fig. 4.3. The three-stage PA consists of a wide bandwidth cascode gain stage, a common source driver stage to boost the overall gain and dual-mode power stages. Amplifiers are implemented in differential mode to achieve 100% higher voltage swing in comparison with the single ended topology. A transformer balun combined with microstrip transmission line network is used to split the input power into the first differential cascode stages. A circuit technique is utilized to enhance the power gain of the cascode stages at 60 GHz. On-chip transformers are used to match the impedances and combine the power of amplifier stages. Transformers with center tap are used to perform the DC biasing and differential power combining simultaneously.

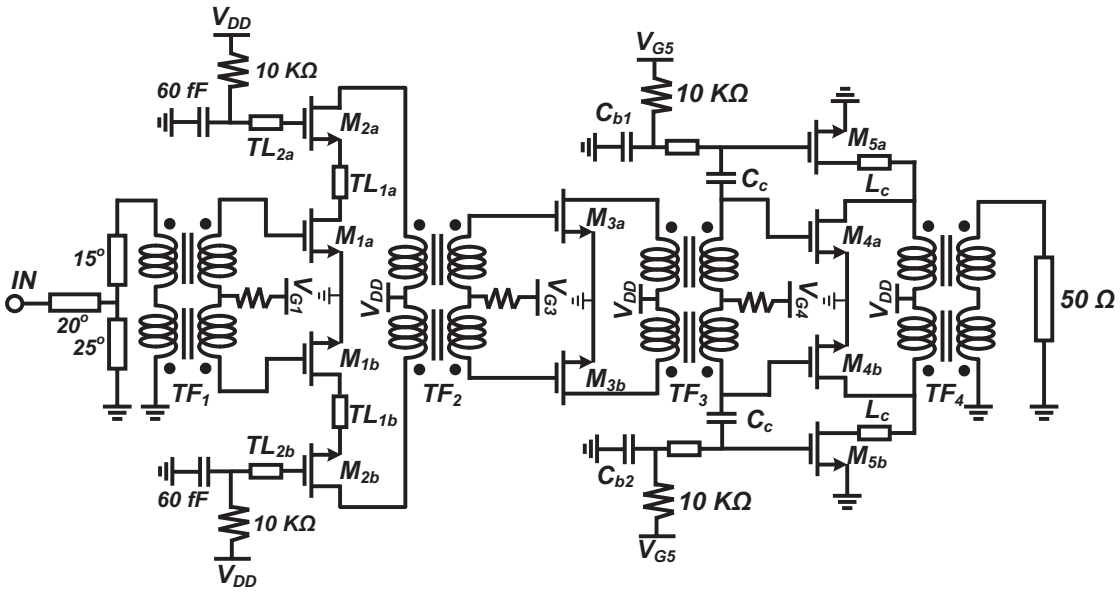


Figure 4.3: Schematic of 60 GHz dual-mode amplifier in 65nm technology.

4.2.1 Dual-mode power stages

Differential dual-mode power amplifier stages are designed for 60 GHz applications as shown in Fig. 4.3. Each of the differential power stages consist of two units. Each unit incorporates a main transistor (M_4) and an auxiliary transistor (M_5). M_4 provides amplification in class A mode and must be able to drive the output at high saturation level. As a result, a transistor with large channel-width must be chosen for this unit. The f_{max} of power transistors is a key parameter that characterizes the frequency dependent gain performance of a MOSFET. The current density of the class-A power transistor must be chosen as high as 300 μA/μm to satisfy the output power and f_{max} specifications. The gate-source of the auxiliary transistor (M_5) can be biased at threshold voltage for class B operation or under threshold voltage for operating in class C. In this scenario, the size of the auxiliary transistor must be chosen to obtain same power gain as the main stage but with different biasing condition. The maximum frequency of operation of the dual-mode power stage depends on the total size of the main and auxiliary transistors. The f_{max} for N-channel MOSFETs with various channel widths and current densities are extracted and demonstrated in Fig. 3.6. As discussed in section 3.2, the total channel width of 120 μm can be chosen to keep the f_{max} of power devices beyond 90 GHz so that the devices can be used for amplification. However, the extra parasitic capacitance introduced by the output

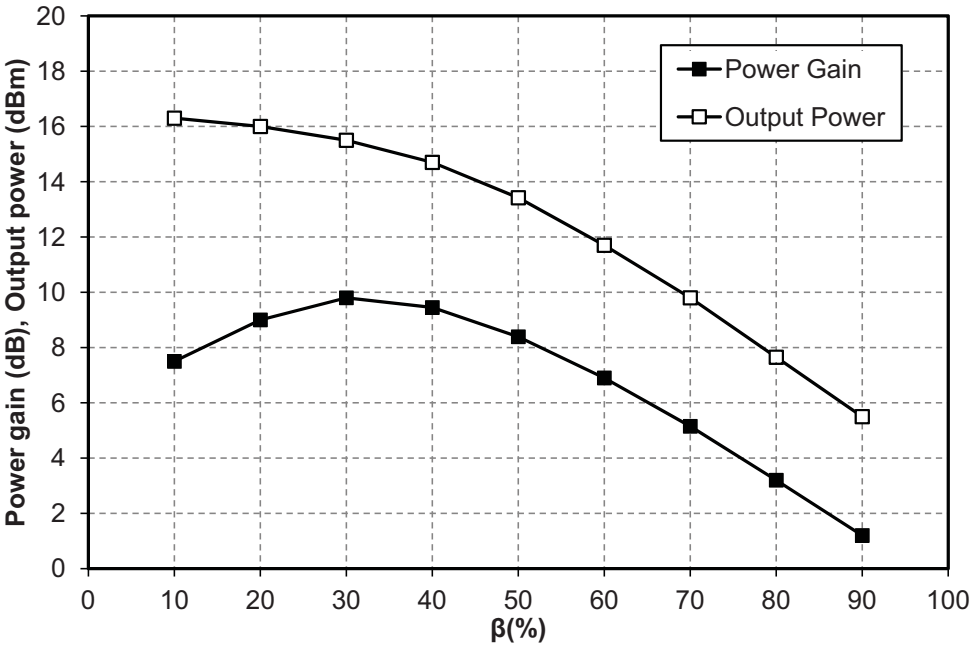


Figure 4.4: Performance of the dual-mode stage versus transistors' width ratio.

impedance of the auxiliary transistor in dual-mode topology will decrease the overall f_{max}. Simulations are performed to optimize the sizes of the main and auxiliary transistors. The parameter β is defined as the width ratio of the auxiliary transistor (W_{M5}) over the total channel width of the dual-mode stage (W_{total}=W_{M5} + W_{M4}). The output power and the power gain of the amplifier is simulated when the overall channel width of dual-mode stage is fixed to be 100 μm. Fig. 4.4 shows the maximum power gain and output power of the dual-mode stage for various transistor sizes at 60 GHz. The maximum available output power of the dual-mode stage decreases when the auxiliary transistor becomes larger. However, the power gain of the dual-mode stage reaches its maximum value when the auxiliary transistor occupies about 30% of the total size.

By choosing 72 μm channel width, transistor M_{4a} can drive 66% of the required output power in class A mode while keeping the f_{max} beyond 120 GHz. This transistor is able to handle the output current of 40 mA with gate bias of 0.8 V and supply voltage of 1.2 V. A channel width of 24 μm is chosen for auxiliary transistor (M_{5a}) to deliver the 33% of the remained current to the load while keeping the f_{max} of the unit beyond 60 GHz. Using a matching circuit is inevitable to compensate the delay/impedance mismatch between two units. The output matching circuit consists

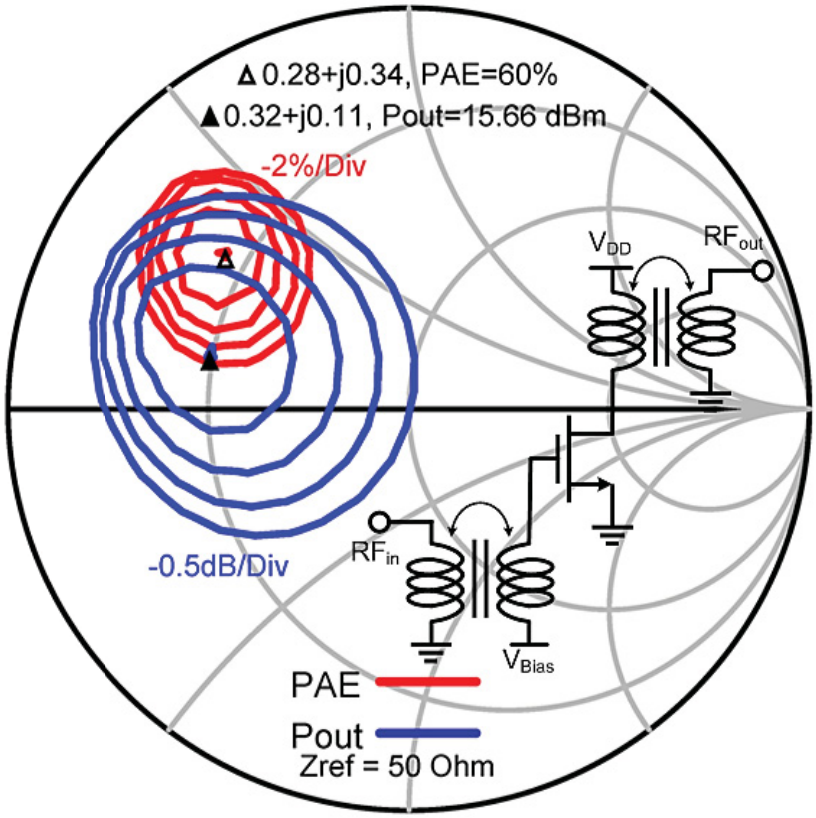


Figure 4.5: Load-pull simulation results of the dual-mode power stage.

of two parts: a transmission line (L_c) incorporated with the inherent capacitance of transistor M_{4a}. This circuit topology can combine the output of two transistors in a single unit. In addition, the I/O impedances drop when the number of fingers is increased which leads to higher matching network losses because the higher impedance transformation ratio is required. Load-pull simulations are performed to obtain the optimum impedance required for highest possible power/efficiency capabilities.

Fig. 4.5 illustrates the load-pull simulation results for the dual-mode power stage with total channel width of (72+24) μm. According to load-pull simulations, transistor must see normalized optimum load impedance of 0.32 + j0.11 to obtain high output power. The transformer-based loss-less impedance tunning network is used to match the 50 ohm load to this impedance level. However, the practical matching network introduces extra loss which degrades the overall efficiency. Maximum output power of 15.66 dBm is achieved by combined class-A and class-B biasing (V_{G1} = 0.8V, V_{G2} = 0.3V and V_{DD} = 1.2V) with 60% maximum PAE. According to the

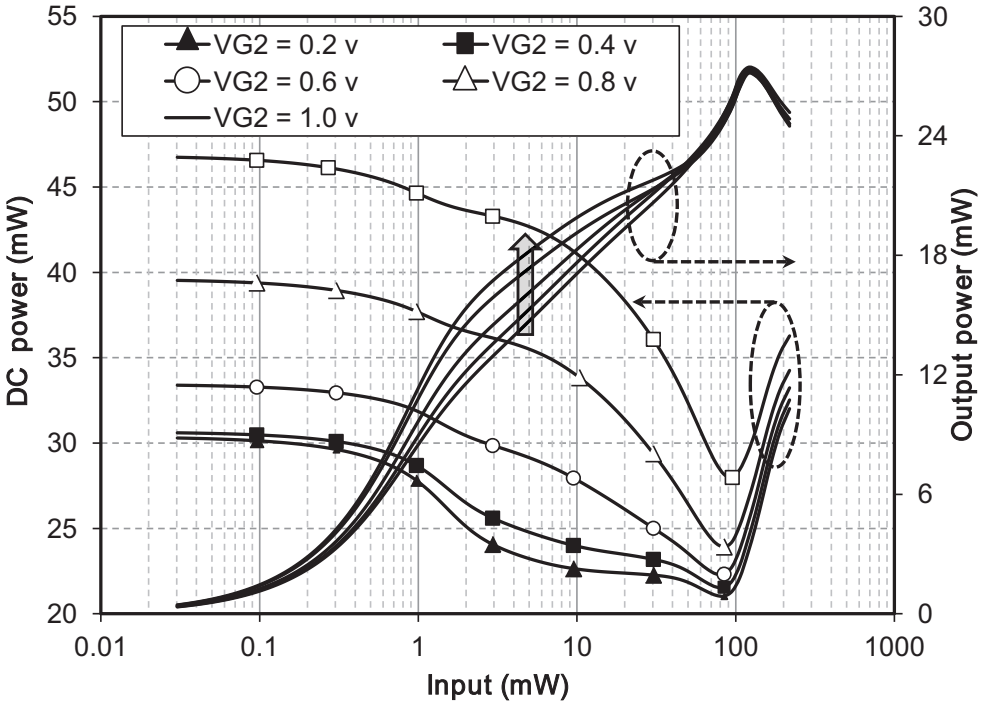


Figure 4.6: Output power and DC power consumption of the dual-mode power stage under various bias conditions.

PAE contours, a high PAE is achievable for a wide range of impedances. However, the maximum output power is achieved whereas the efficiency is measured to be 52% which is very close to class A operation. By changing the bias condition of the auxiliary transistor, it can operate in various classes. However, the optimum bias point is chosen based on the simulated output power and efficiency.

Fig. 4.6 shows the obtained output and DC power of the designed single stage dual-mode power amplifier at 60 GHz. Increasing the bias voltage of the auxiliary amplifier increases the DC power consumption of the circuit and decreases the efficiency of the whole amplifier. The proposed topology could improve the output power of the stages for input levels from 1 mW to 10 mW. The output voltage of the amplifier will not be a pure sinusoid when the input power exceeds 30 mW. Hence, amplifier experiences saturation for input power levels higher than 30 mW. The amplifier will not be a simple Class-A for inputs larger than 30 mW because the transistor experiences triode and off states as well as the deep inversion. The calculated drain efficiency of the designed stage is presented in Fig. 4.7 for various bias conditions. Compared to a single Class-A amplifier with 72μm transistor, the maximum drain efficiency

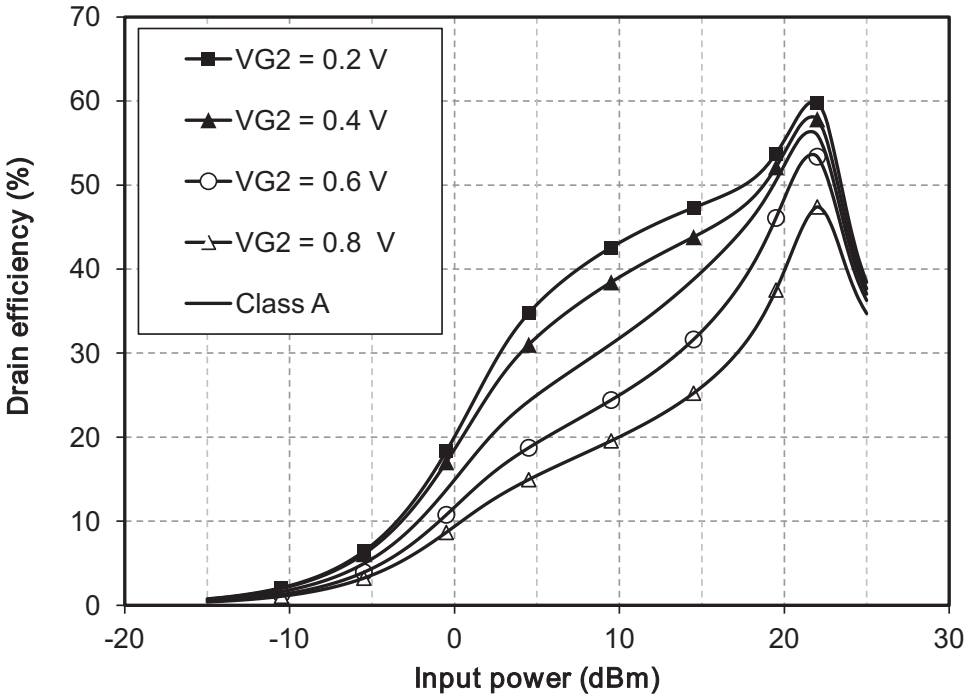


Figure 4.7: Drain efficiency of proposed dual-mode PA stage under various biasing conditions.

is improved using dual-mode configuration for high input power values. Also, the dual-mode topology exhibits more efficiency at back-off levels.

The output power of the power amplifier is further increased by combining two dual-mode stages in differential topology. An on-chip octagonal stacked transformer (TF_4) with a center tap is implemented on top metal layers to combine the output power of stages. In this design, inner diameter of 30 μm is chosen for output transformer while the PA can still deliver sufficient output power at 60 GHz. At the same time, the transformer matches the 50 Ω load impedance to the optimum impedance of the power stages obtained using loadpull simulations (Fig. 4.5). The center tap of the transformer is used to bias the drain node of power transistors at V_{DD}.

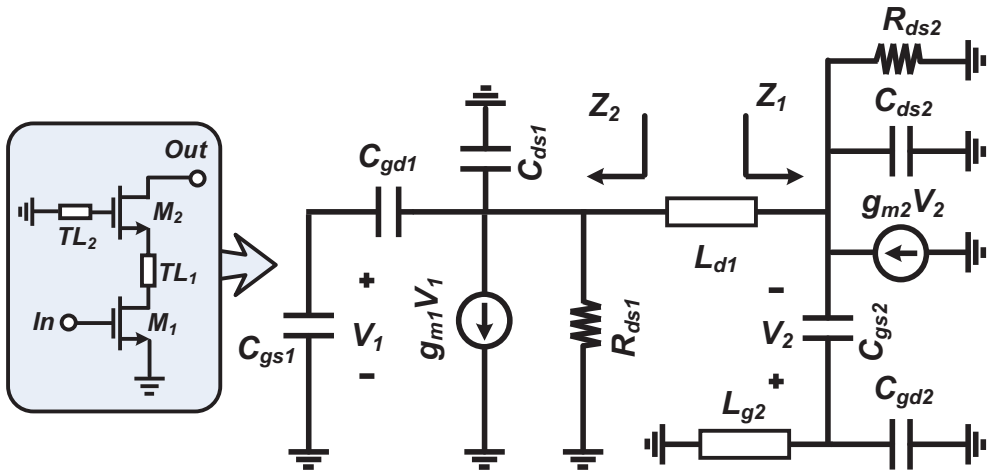


Figure 4.8: Small-signal model of the cascode amplifier at high frequencies.

4.2.2 Gain-enhanced cascode stage

To ensure a reasonable power gain at 60 GHz, the driver stage and the gain stage are cascaded before the dual-mode PA. Differential cascode amplifier followed by a differential CS stage are designed as gain and driver stages respectively. Achieving wide band-width for gain stages is desired to increase the gain-bandwidth performance of the whole PA. A compensation technique is used to improve the bandwidth of the cascode stage. Transmission lines (T_{L1a} and T_{L2a}) are used to compensate the effect of intrinsic capacitances and increase the f_{max} of the cascode stage as shown in Fig. 4.3. By increasing the f_{max} of the cascode stage, transistors with larger channel width can be used in driver stage which can improve the maximum available input power of the drive stage and results in higher P_{1dB}.

In addition, a high f_{max} results in a high small-signal gain/bandwidth of the cascode stage. Fig. 4.8 shows a small-signal model of the enhanced cascode amplifier. The total parasitic capacitance seen by the drain connection of M_{1a}, and source/gate connections of M_{2a} are the parameters which degrade the f_{max} of the cascode pair. The overall capacitance presented at the source node of M_{2a} creates a dominant pole in transfer function of the cascode stage. A transmission line with specific length can compensate the impact of the dominant pole by introducing a zero in the small-signal gain transfer function. This transmission line (L_{d1} or TL_{1a}) which is placed between the source of M_{2a} and drain of M_1, can resonate with total capacitance seen by these two nodes canceling the gain reduction by the initial pole. The second

transmission line (L_{g2} or TL_{2a}) can be connected between the gate of the transistor M_{2a} and the bias network to cancel the negative reactance of the impedance seen by the gate-drain and gate-source connections. The other impact of this element is gain-boosting mechanism by introducing a negative resistance to the output impedance of the cascode stage. The real part of the impedance seen by the source of M_{2a} in presence of an inductive element at the gate node of M_{2a} can be calculated as

$$Re[Z_1] = \frac{1 - \omega^2 L_{g2} g_{m2}(C_{gs2} - C_{ds2})}{\omega^2 (C_{gs2} - C_{ds2})^2 + g_{m2}^2}. \tag{4.7}$$

where, C_{gs2} and C_{gd2} are the main capacitors which create a dominant pole at the gate connection of M_{2a}. Considering the fact that $\omega^2.L_g.C_{total}.g_{m2}$ is much larger than 1 at high frequencies, the impedance equation can be simplified as

$$Re[Z_1] = \begin{cases} \frac{\omega^2 L_{g2}(C_{ds2} - C_{gs2})}{g_{m2}}, & g_{m2} \gg \omega C_{total} \\ \\ \frac{-L_{g2} g_{m2}}{C_{gs2}}, & g_{m2} \ll \omega C_{total} \end{cases}. \tag{4.8}$$

As the frequency increases, the resulting negative resistance also increases, and the voltage gain of the cascode architecture can be increased. The other advantage of using inductive elements is frequency compensation by shifting the dominants poles which are created by capacitive part of the impedances. The total imaginary part of the impedances seen at the source connection of M_{2a} and drain connection of M_{1a} can be derived as

$$Im[Z_1] + Im[Z_2] \simeq \omega L_{g2} - \frac{1}{\omega C_{gs2}} + \frac{1}{\omega C_{ds2}} + \frac{2}{\omega(2C_{ds1} + C_{gs1})}. \tag{4.9}$$

Transmission line TL_{2a} creates inductive impedance between the connections of transistors M_{2a} and M_{1a} to compensate for the effect of dominant pole on the gain. Fig. 4.9 illustrates the simulation results for power gain and f_{max} of the enhanced cascode amplifier for different electrical lengths (θ). Although using the proposed technique could improve the frequency response, the T-line added to the gate node of M_{2a} can potentially create stability problems. Stability parameter (μ) is extracted from simulation results with respect to the length of the T-line. As shown in Fig. 4.10, the cascode amplifier will be unconditionally stable with factor of greater than unity. T-Lines have been optimized to get 20 GHz more stable f_{max} with θ of 10^o or 60 μm physical lengths. Bias conditions (V_{DD} = 1.2 V, V_{G1}=0.8 V, V_{G2}=1.2 V) are

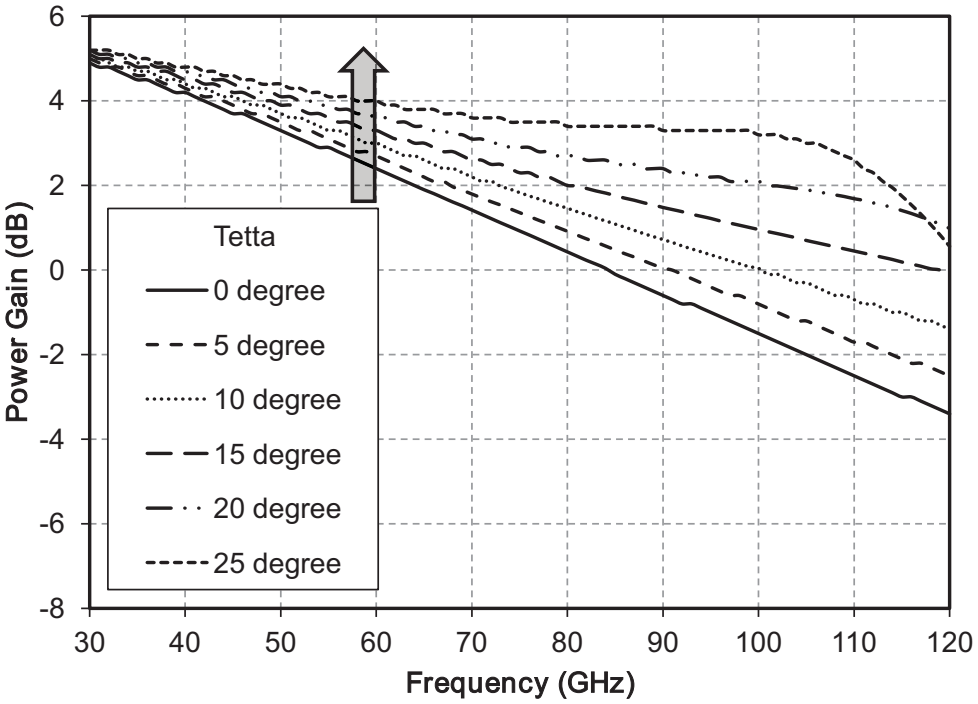


Figure 4.9: Simulation results for maximum power gain of enhanced and conventional cascode stages.

set to achieve the maximum current density at operating frequency. In the cascode stage,transistors are laid out in 30 fingers with 1 μm and 1.5 μm channel width respectively. The normalized output impedance of $Z_o = 0.25 + j0.15$ is measured for the cascode stages. An octagonal stacked transformer with radius of 22 μm is implemented on top metal layers to perform the inter-stage matching between cascode and CS stages.

The CS stage transistors are laid out in 30 fingers with total channel width of 45 μm. The gate bias (V_{G3}) voltage is set to 0.8 V while the supply voltage (V_{DD}) is 1.2 V for all the driver stages. With this biasing condition, cascode and driver stages could achieve power gains of 15 dB and 9 dB, respectively. However, the overall power gain is reduced by the losses of matching networks and power combiners. CS driver stages will be able to deliver 25 mA output current which delivers 14.5 dBm output power to a normalized optimum output impedance of $Z_{o,cs} = 0.52+j0.47$. The output impedance of the CS stages are matched to the power stages using stacked transformers with radius of 25 μm. Simulated gain and I/O reflections of the proposed 60 GHz PA are illustrated in Fig. 4.12. The simulated 3dB bandwidth is 20 GHz from

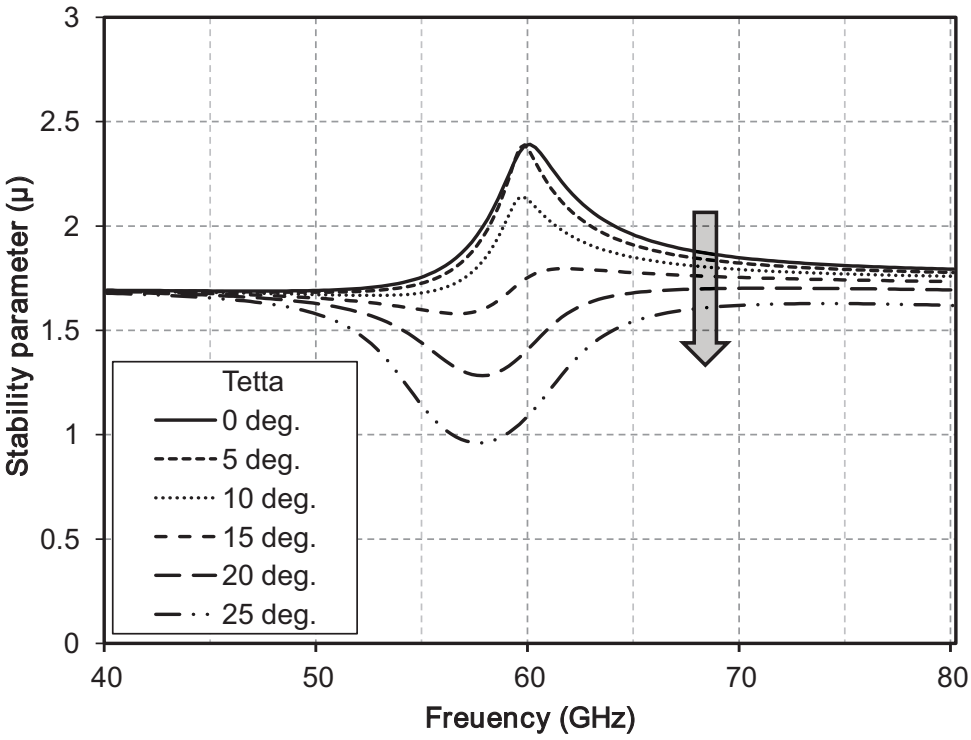


Figure 4.10: Simulated stability parameter of the enhanced cascode stage.

53 GHz to 73 GHz which proves the high performance of the cascode and CS stages. The I/O reflection coefficients are less than -10 dB inside the 20 GHz bandwidth.

4.2.3 60 GHz PA simulation and measured results

The proposed dual-mode 60 GHz PA is fabricated in 1P9M 65nm standard CMOS technology. The chip micrograph of the PA is shown in Fig. 4.11. The PA only occupies a core area of 0.32 mm^2 excluding the DC/RF pads. The S-parameter measurements are performed using Agilent N5251A 110 GHz solution which uses an E8361 PNA and the results are calibrated using SOLT (short-open-load-thru) calibration substrate. The measured S-parameters are compared with the simulation results in Fig. 4.12. The PA is matched to I/O impedances of 50 Ω. Applying 1.2V core supply voltage and gate bias (V_G) of 0.8 V to all the stages, maximum small-signal gain of 17.7 dB within a 3dB bandwidth of 12 GHz are measured. Compared to the wide band-width of 20 GHz achieved in simulation, the 8 GHz difference in measured results is probably due to the inaccurate MOSFET models at 60 GHz.

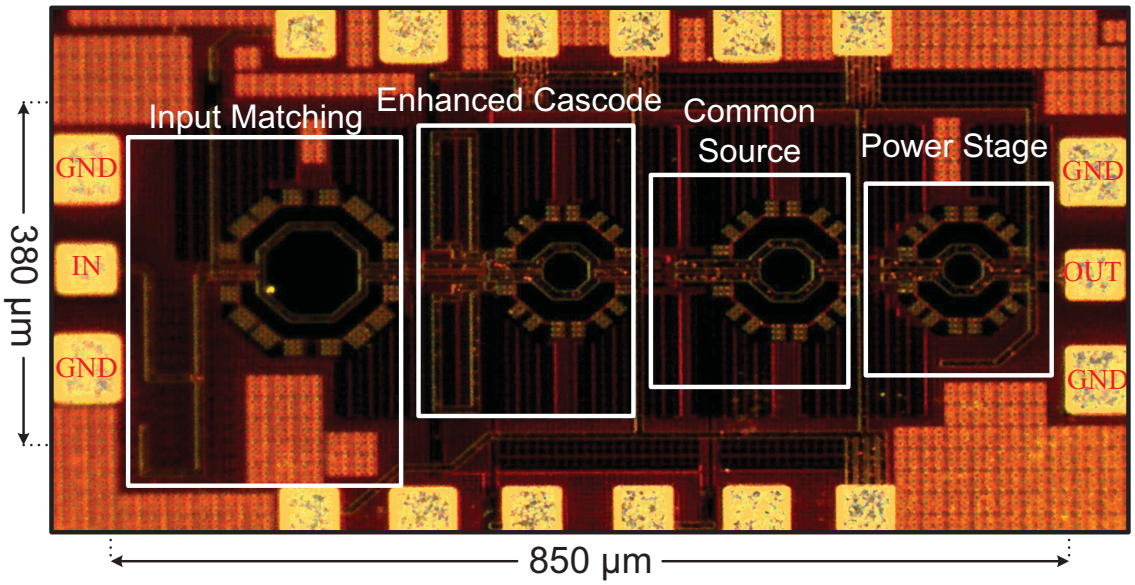


Figure 4.11: Chip micrograph of the proposed dual-mode 60 GHz PA.

Another reason is a -6GHz frequency shift between the measured and simulated S_{11} which depends on the input matching network and the performance of the cascode stage. However, the measured gain of the amplifier is higher than the simulated gain at 57 GHz because both S_{11} and S_{22} reach their minimum value at this frequency. The PA operates functional inside the IEEE802.15.3c band and offers minimum power gain of 13.7 dB at 67 GHz. The input matching network reaches -26 dB whereas the S_{22} is measured to be -20 dB. The measured S_{22} is less than -15 dB for wide range of frequency so that the PA could obtain +10 dB power gain for 17 GHz bandwidth from 53 GHz to 70 GHz. The measured stability factor of the fabricated PA is demonstrated in Fig. 4.13. With the measured stability factor of larger than unity, the fabricated PA is unconditionally stable from DC to 80 GHz.

The large-signal measurements are performed using Rohde-Schwarz NRP-Z power sensors and the Rohde-Schwarz ZVA67 VNA at 60 GHz. The P_{sat} and PAE are measured in low-power and high-power modes as shown in Fig. 4.14. For low-power mode with 1.2V core supply voltage and V_G of 0.8 V for all the stages, the measured 1dB compressed output power is 15.5 dBm and the P_{sat} is 16.8 dBm. With relatively high measured P_{1dB}, the PA exhibits linear gain up to the saturation level. The measured maximum PAE is 14.5% in LP mode. The PAE has a value close to its maximum value when the PA runs into saturation. One particular parameter which

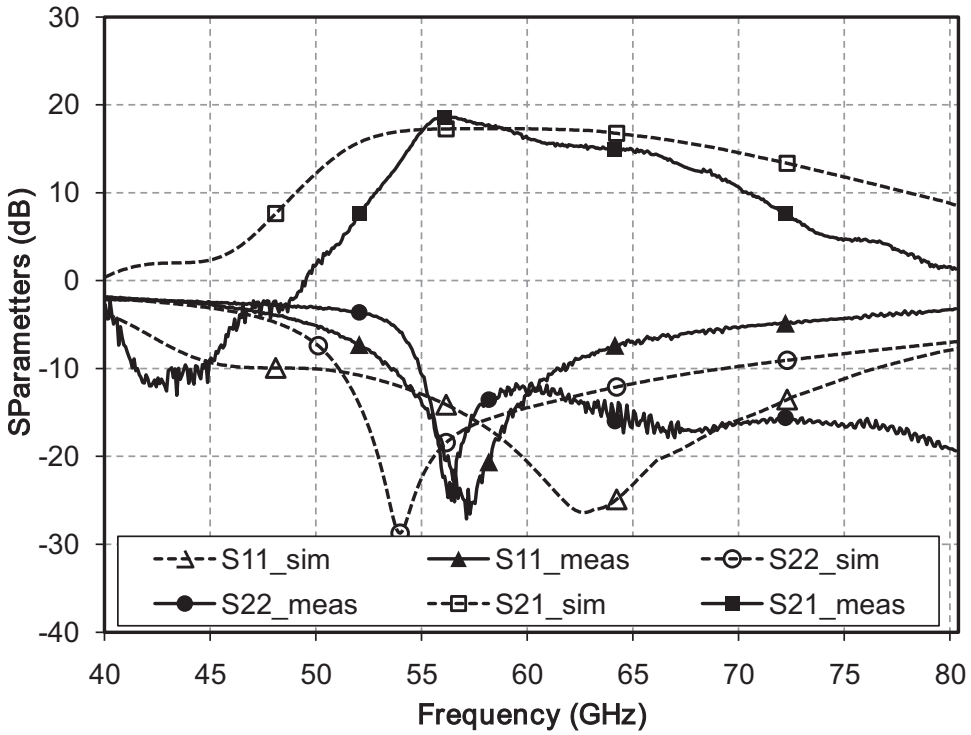


Figure 4.12: Measured and simulated S-parameters of the proposed 60 GHz PA.

affects the PAE is the consumed DC power of cascode and driver stages. Higher PAE could be achieved by biasing these stages at considerably lower drain currents. However, the driver stage runs into saturation earlier reducing the P_{1dB} dramatically. Although the measured PAE at P_{1dB} is about 10%, P_{1dB} of 15.5 dBm enables the PA to operate at high input power levels. One particular drawback of the proposed PA is low PAE at 6dB back-off level which could be improved by optimizing the driver and gain stages at lower current densities.

High-power mode measurements are performed by applying a higher supply voltage of 1.4 V to the power stage and 1.2 V to the gain and driver stages. The gate biasing voltages are adjusted to be 0.7 V and 1.0 V for gain and power stages to keep the gain as high as the achieved gain in low power mode. Biasing in these conditions, larger amount of the output power will be delivered by the power stage. In addition, driver stages consumes less DC power compared to the LP mode using low bias current. Hence, the overall efficiency will be increased. The saturated power of 18.1 dBm is measured while the maximum PAE is improved to 17.2% by achieving more power from the last PA stages. Compared to the state-of-the-art 60 GHz PAs in the

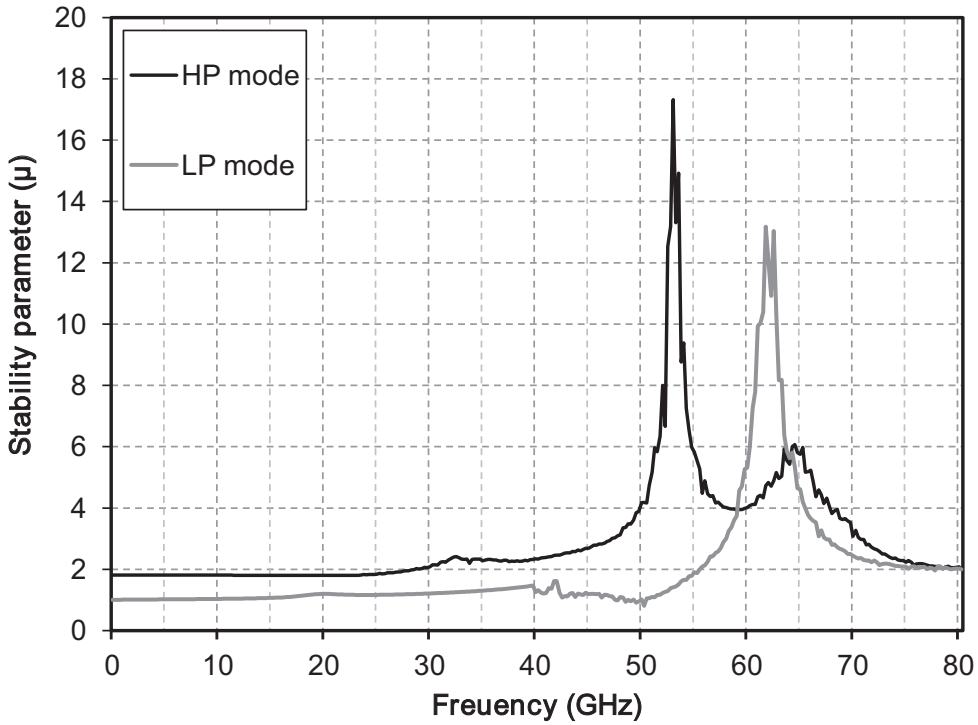


Figure 4.13: Measured stability factor of 60 GHz PA.

65nm technology, proposed dual-mode 60 GHz PA is smaller in size with comparable higher output power which results in a high power/area figure of merit.

In spite of using small core supply of 1.4 V, the measured output power and P_{1dB} are considerably higher compared to other designs in the same technology. Compare to the reported PAs in 40nm technology [82] [109, 110], the proposed PA achieves higher P_{sat} and P_{1dB} using lower supply voltage and in smaller die area. Moreover, the measured bandwidth of 15 GHz in HP mode enables high data rates and frequency reuse around 60 GHz. Compared to other reported dual-mode PAs, the proposed PA achieves 100% wider bandwidth due to the proper sizing of transistors and the gain enhancement techniques. Large-signal performance of the PA is measured at various bias points over six different frequencies inside the IEEE802.15.3c band. The supply voltage is swept from 1.0V to 1.4V to demonstrate the supply dependence and reliability of the fabricated PA. Output power of the PA for various supply voltage levels are demonstrated in Fig. 4.15. Using only 1.0V supply voltage, the PA maintains the +14dBm output power inside the IEEE mmW band which satisfy the specifications for low power short-range transmitters. The measured gain variations

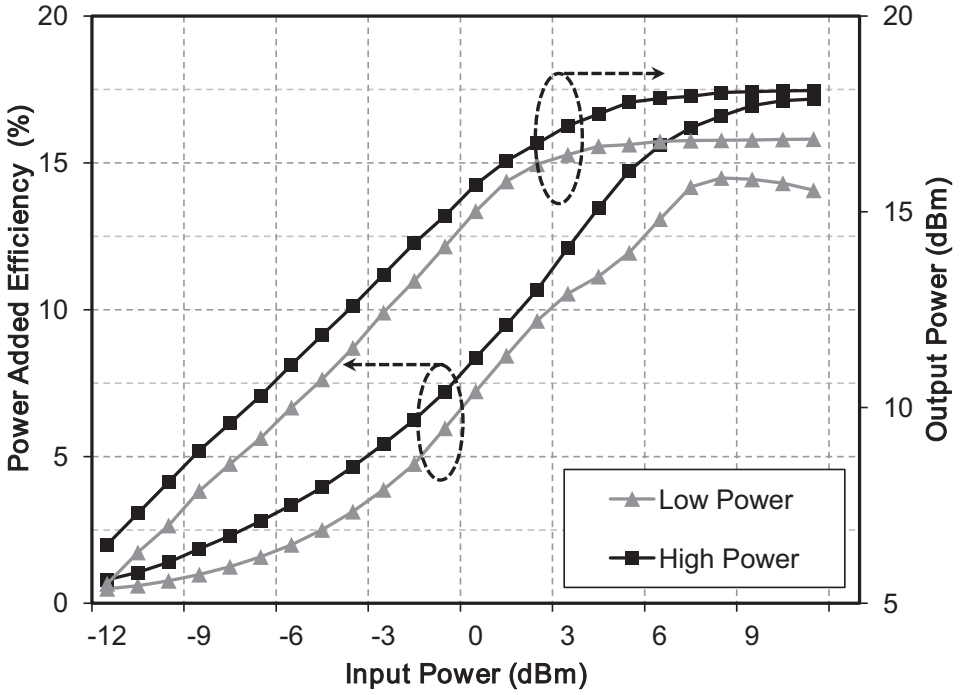


Figure 4.14: Measured output power and power added efficiency of the fabricated dual-mode 60 GHz PA.

for different levels of supply voltages are shown in Fig. 4.16. The PA obtains a +15 dB power gain using only 1V power supply. Also, the power/gain variations is less than 1dB inside the IEEE 802.15.3c band. The measured PAE of the PA is still higher than 10% for low supply values with very low variations over different channels. Fig. 4.18 shows simulated third-order inter-modulation distortion (IMD3) of the PA in both LP and HP modes. Although the IMD3 is increased at high output power levels, the amplifier achieves IMD3 of less than -25 dBc at P_{1dB} of 14.5 dBm.

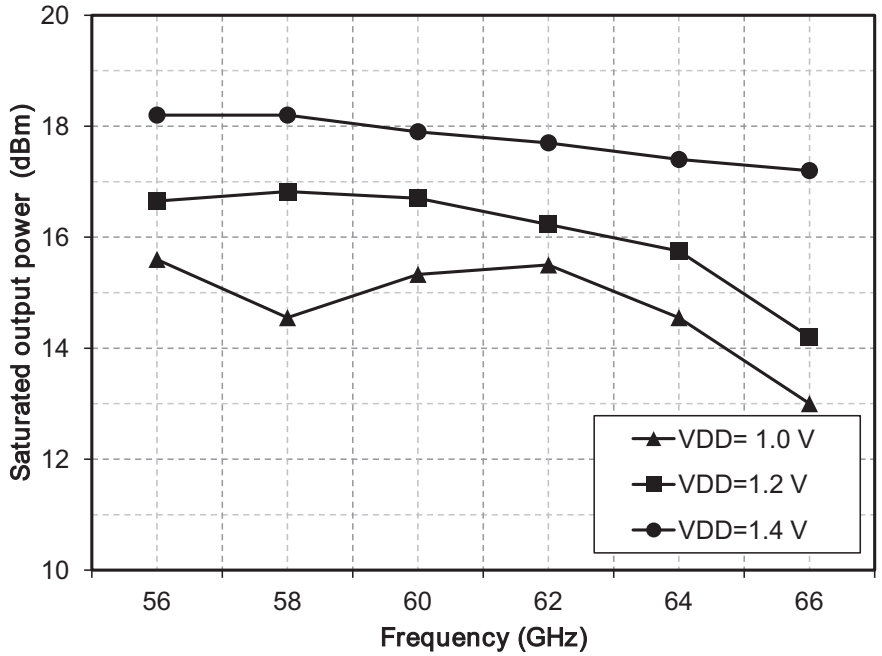


Figure 4.15: Measured output power of the proposed dual-mode 60 GHz PA versus frequency and supply changes.

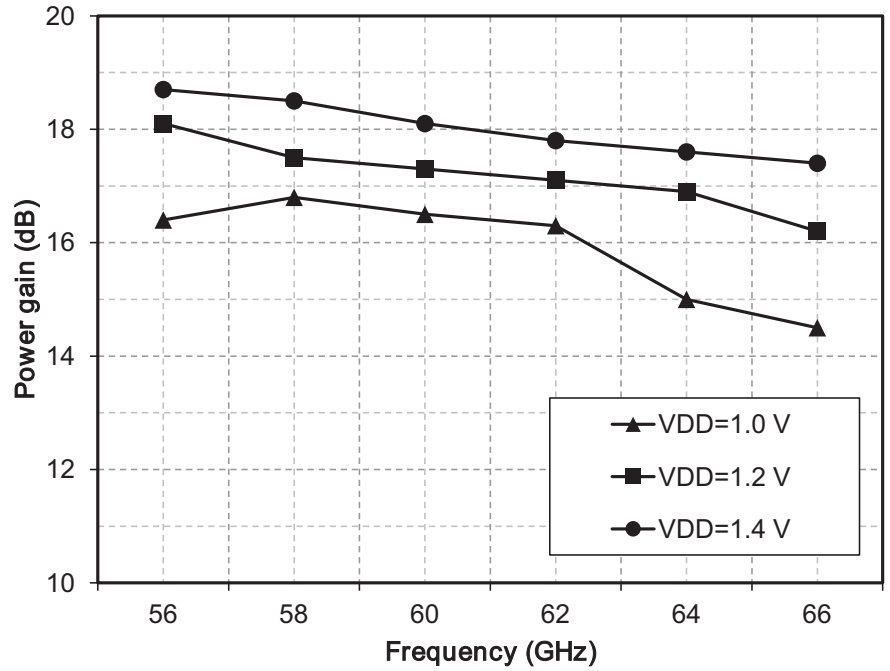


Figure 4.16: Measured power gain of the proposed dual-mode 60 GHz PA versus frequency and supply changes.

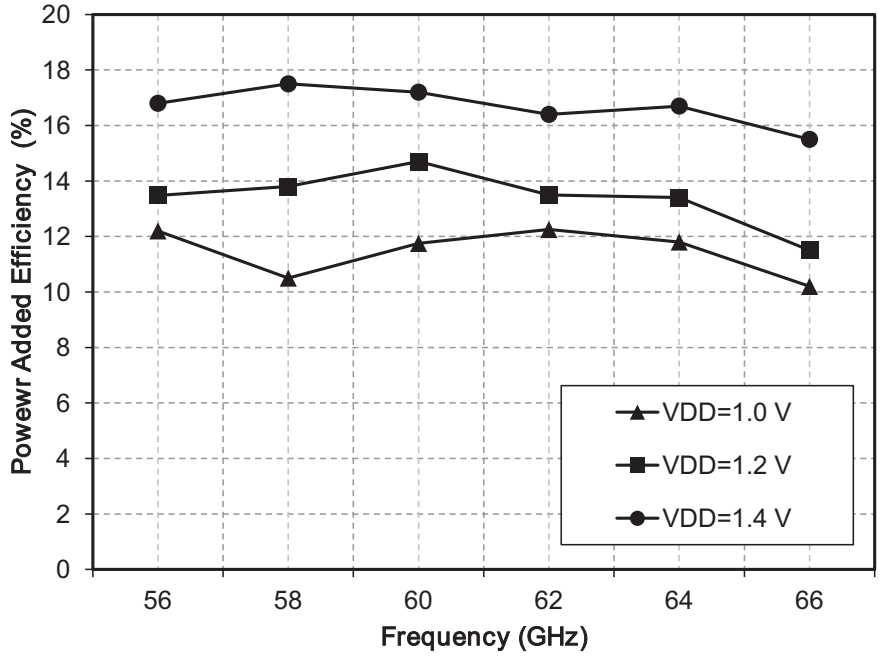


Figure 4.17: Measured power added efficiency of the proposed dual-mode 60 GHz PA versus frequency and supply changes.

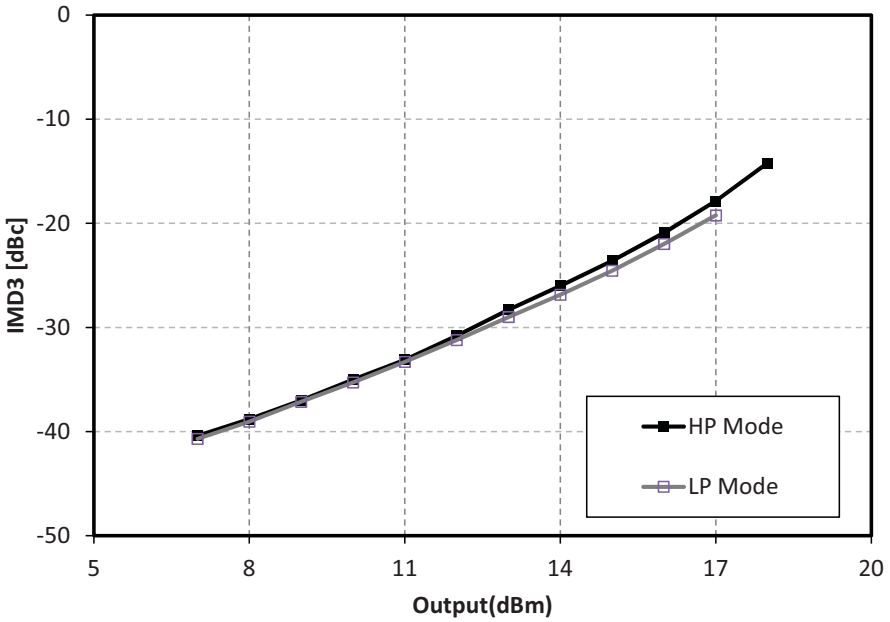


Figure 4.18: Simulated IMD3 of the proposed dual-mode 60 GHz PA.

4.3 Summary

A 60 GHz PA introducing a new dual-mode power combiner topology is implemented in 65nm CMOS technology. Two CS stages operating in different classes are combined in our proposed technique. Using this topology, a high PAE is obtained when amplifier runs into saturation. In comparison with the conventional Class-A PA, the proposed topology provides a higher efficiency. Driver stages are optimized to ensure sufficient gain at 60 GHz. In order to increase the gain-bandwidth product of the amplifier, a new parasitic cancellation technique is utilized in cascode stages. The fabricated PA exhibits 15 GHz bandwidth due to the enhanced cascode stages. Performance comparison of the fabricated PA with reported 60 GHz PAs in 65nm CMOS is presented in Table. 4.1. Presented in [111], the proposed dual-mode PA obtained maximum PAE of 17.2% whereas the output power is measured to be 18.1 dBm. Compared to other PAs, the new power amplification method provides high output power per unit area on chip. Due to a considerably high BW of 15 GHz, the PA exhibits highest reported $G_P \times$BW compared to other similar works.

Table 4.1: Performance comparison of 60 GHz PAs in 65nm CMOS technology.

V_{DD} [V]	B.W [GHz]	Stages	Mode	Topology	Combiner	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	Size [mm^2]	mW/mm^2	FoM	Reference
1.2	12	3	d	cs	-	16.8	15.5	17.7	14.5	0.32	150	82	LP
1.4	15	3	d	cs	-	18.1	15.8	18.3	17.2	0.32	202	84	HP
1.0	6	3	d	cs	2x	17.8	13.8	11	12.6	0.28	215	75	[62]
2.4	9	2	s	cs	2x	15.4	13.7	17.2	14.3	0.25	139	79	[53]
1.8	7	4	d	cs	4x	15.6	13.5	20	6.6	2.25	16	79	[55]
1.0	8	3	d	cs	-	11.5	2.5	15.8	11	0.05	283	73	[51]
1.0	10	2	d	cs	4x	17.9	15.4	18.8	11.7	0.83	74	83	[52]
1.2	15	2	b	cs	8x	18.1	11.5	15.5	3.6	0.46	140	74	[54]
1.2	6	3	d	cs	-	14.6	10	23.2	16.3	0.6	48	85	[60]

Chapter 5

Dual-Mode Distributed Active Transformer

In this chapter, design and implementation of a dual-mode 60 GHz power amplifier is discussed based on distributed active transformer technique. Although the DAT topologies have been used at very low frequencies, we propose a new layout topology to perform the power splitting and combining of four differential PA stages simultaneously. Hence, the overall power and efficiency are improved by removing lossy TL-based power dividers. Combining maximum number of PA cores in a compact area, the proposed technique achieves a very high RF power density compared to the other techniques. In order to decrease the insertion loss, proposed DAT topology has the advantage of using stacked transformer topology for both the combiner and divider in a small die area. The idea of dual-mode operation is used in designing power amplifier cells to overcome the efficiency trade-off. The proposed circuit topology combines Class-A and Class-AB differential PA stages in a single PA core at 60 GHz using parallel connection of CS and cascode amplifier stages to increase the PAs' PAE. The power gain of gain stages are boosted using a new transformer-feedback frequency compensation technique. Thus, the overall gain and PAE of the proposed PA are improved using high-gain drivers.

5.1 Design of Dual-Mode DAT PA

Distributed active transformers are conventional methods to combine the output power of multiple individual PA cells. In this circuit technique, output power of PA

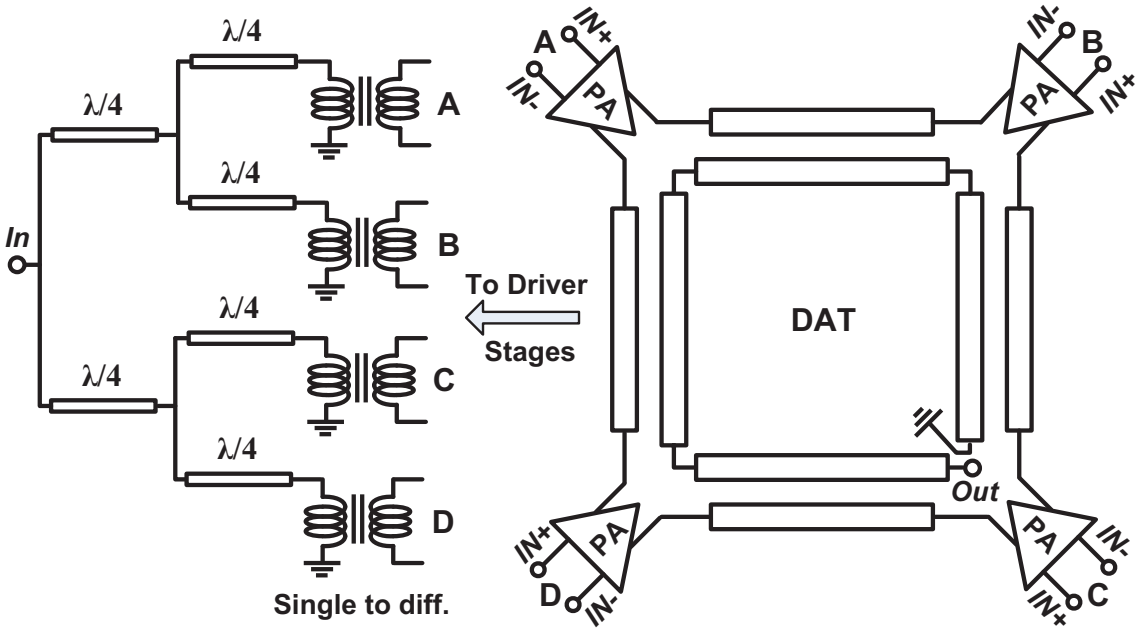


Figure 5.1: Conventional implementation of distributed active transformer.

cells are combined serially using a circular-geometry distributed transformer network. The first demonstrations of watt-level DAT CMOS PAs were reported by [98] [100] at 2 GHz. Fig. 5.1 shows block diagram of the conventional DAT topology. PA cells are differential CS amplifiers combined using slab inductors. The inner turn combines the output power of PA cells using magnetic coupling between the slabs. The output impedance of the PA is boosted up using DAT because of the series connection of PA cells. Hence, a low ITR is required at output and the circuit loss of the output matching network is decreased on Si substrate. Meanwhile, the channel width of each individual transistor could be decreased using this structure which results in higher gain and f_{max}. Using differential DAT topology solves the challenge of the low breakdown voltage of the short-channel MOS transistors because each transistor experiences only 12.5% of the maximum output voltage on its drain node. Despite these advantages, the DAT topology still has some drawbacks to be used in 60 GHz PA design.

The DAT structure, shown in Fig. 5.1, consists of four parts which are: 1) coupled inductors forming the output combiner, 2) PA cells to generate RF power and amplify the input signal, 3) a single-ended to differential transformer network, and 4) a four-way quarter-wavelength power divider to split the power into individual cells.

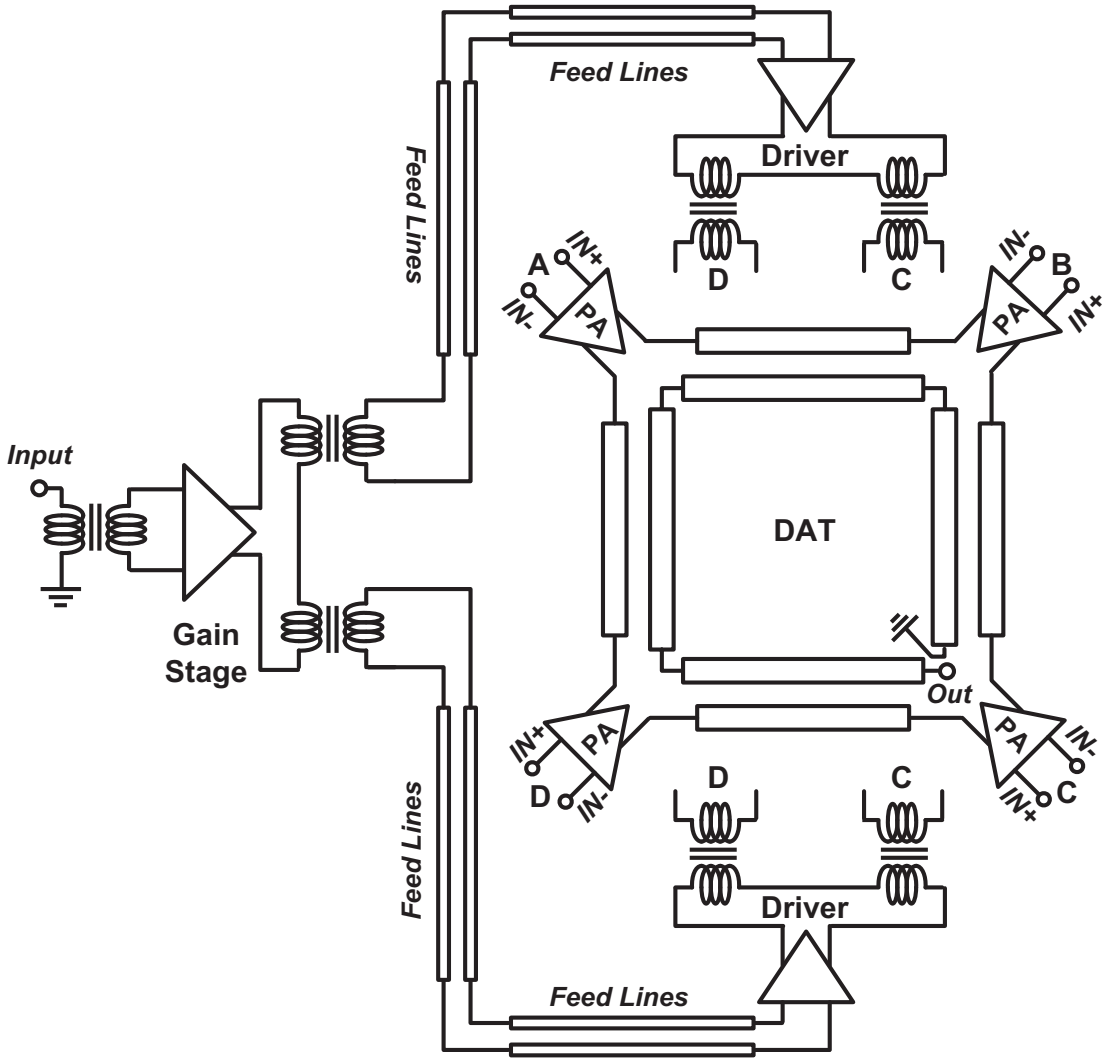


Figure 5.2: DAT topology for 60 GHz PA design including driver and gain stages.

Additionally, feed lines and bias networks are required to drive the signal to the gate of each transistor cells. There are three problems with this circuit topology to be used in a practical PA design. The first problem is the bulky impedance transformation circuits and lossy power divider networks to split the input power. Considering 600 μm length transmission lines for each quarter-wavelength line at 60 GHz, the power divider takes a large area on die. In addition, practical transmission lines cause additional loss which reduces the efficiency and output power. The second problem is the gain requirements at 60 GHz.

Fig. 5.2 shows a possible solution to the design of high-gain DAT PA at 60 GHz.

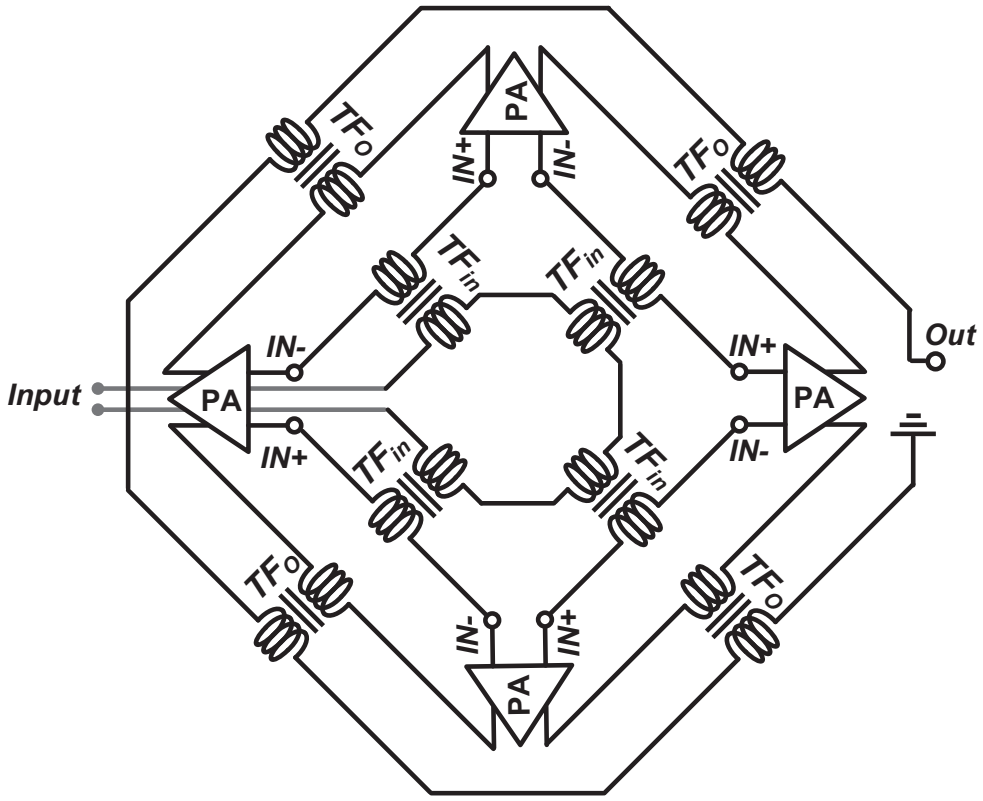


Figure 5.3: Circuit topology of the proposed distributed active transformer.

In the conventional DAT topology, the driver and gain stages require very long feed lines and additional transformers for power conversion and inter-stage impedance matching. Moreover, two driver stages consume two times more DC power compared to a single one which degrades the overall PAE. The third problem is the difficulties in the design of DC biasing network of the 60 GHz DAT topology because of the EM coupling between RF and DC lines. The DAT topology, shown in Fig. 5.2, uses a symmetric topology to increase the stability and robustness of the amplifier against process variations. However, a symmetric DC biasing network must be designed with minimum magnetic coupling between RF/DC paths. High magnetic coupling between the RF, DC and feed lines cause positive feedback and oscillation in the circuit.

In this study, we propose a novel structure DAT in smaller die area to improve the overall efficiency. The circuit topology of the proposed DAT structure is shown in Fig. 5.3. Differential input power is divided into four PA cells using four transformers in series. As discussed in Chapter 3, compact transformers with high ITR are feasible at

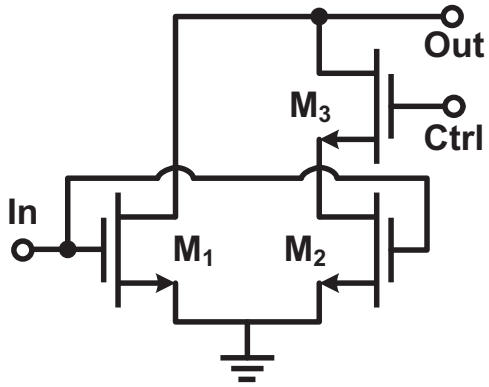
60 GHz using stacked metal layers. In order to decrease the overall size of the DAT, power splitter transformers are implemented inside the output combiners. Using the proposed technique, quarter-wavelength transmission lines are eliminated. Also, transformer-based power splitter performs the inter-stage impedance matching as well as the DC biasing. Hence, the proposed DAT structure satisfy symmetry problem and occupies a small die area. Moreover, PA cells can be driven using a differential amplifier instead of two stages shown in Fig. 5.2. Lossy feed-lines are eliminated in the proposed topology and inter-stage matching can be designed using compact one-turn stacked transformers. Inter-stage feed-lines are eliminated to avoid additional losses and obtain more power gain.

PA cells of the proposed DAT topology are dual-mode power amplifiers optimized to increase the PAE. The advantage of the dual-mode operation is reviewed in the previous chapter. A new topology for dual-mode amplification is investigated in this design to obtain a high power gain as well as the efficiency. Circuit realization and implementation challenges of the proposed dual-mode technique are discussed in next sections along with the design and optimization of gain-boosted driver stages and inter-stage matching components.

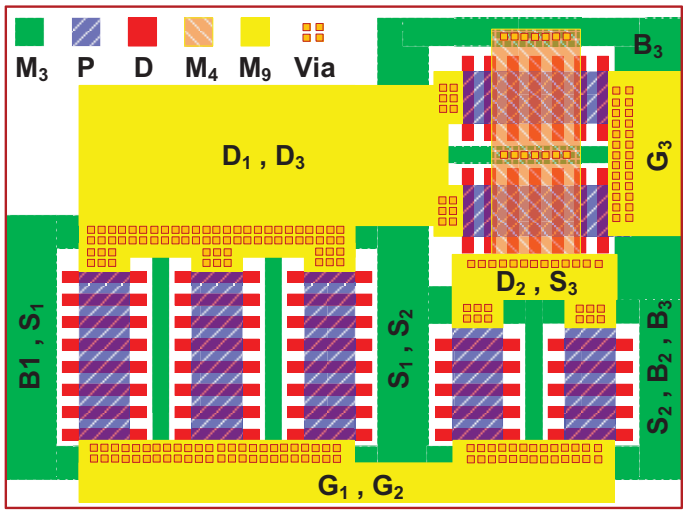
5.1.1 Dual-mode PA stages

In order to increase the power efficiency of the PA stage, a new topology based on the dual-mode operation is proposed as shown in Fig. 5.4(a). The proposed topology consists of a common source stage combined with a cascode amplifier. During the low-power mode operation, cascode stage is turned off and the CS stage (M_1) is biased to operate as a Class-A PA. In this case, the I/O terminals of M_1 experience additional capacitive parasitics introduced by parallel cascode stage. In high-power mode, the cascode amplifier adds to the output power of the CS stage when the switch M_3 is turned on. In this state, more current will be delivered to the load which increases the output power. The gate node can be biased slightly more than the threshold voltage to achieve a high PAE by operating in class AB mode. Interconnections and f_{max} of devices are two dominant causes which limits the efficiency of the proposed topology at mmW frequencies. Thus, a parasitic aware layout design is required.

For PA applications, power transistors with large channel width must be designed to deliver large amounts of current to the load. Large channel width of transistors



(a)



(b)

Figure 5.4: Proposed dual-mode amplification, a) single-ended power amplifier circuitry for illustration purpose b) optimized layout of the proposed topology.

increases the I/O capacitance and lowers the f_{max} of the whole stage. As operation frequency gets closer to the f_{max}, output power and power gain of the device is reduced dramatically because I/O parasitics presents as a large portion of the I/O impedances. The layout of the proposed circuit is optimized to minimize the effect of I/O parasitics. Fig. 5.4(b) shows the optimized layout of a dual-mode PA cell. Gate resistance (r_g), source resistance (r_s), gate-to-drain capacitance (C_{gd}) and source inductance (L_s) are the parasitics which are considered to be minimized. r_g and C_{gd} are two parasitics

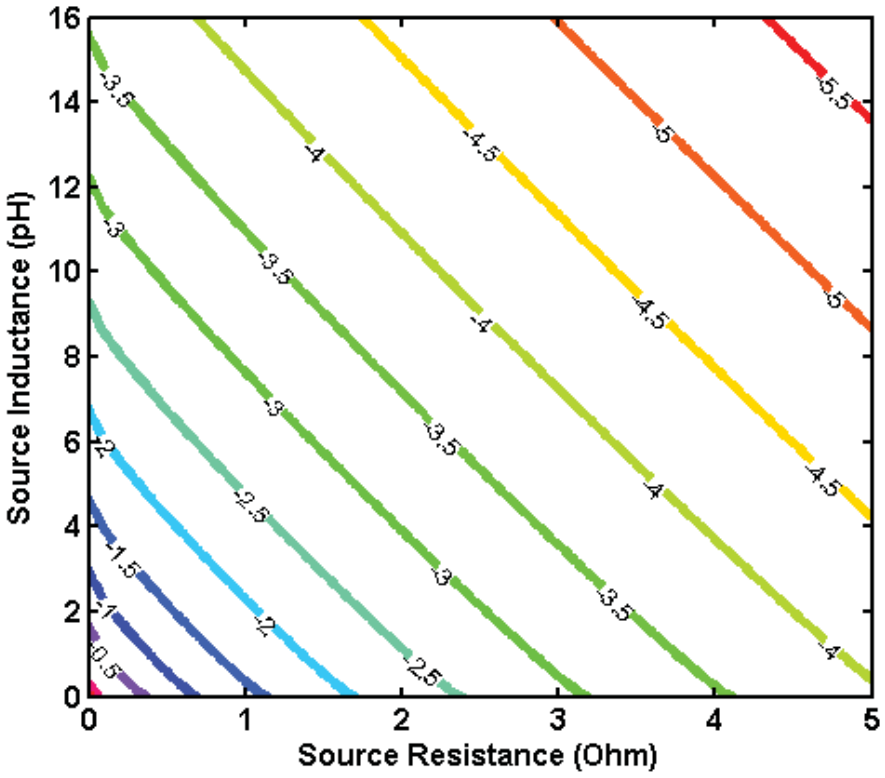


Figure 5.5: Power gain degradation of dual-mode stages due to the parasitic source resistance and inductance added to all unit cells.

which are minimized by choosing multi-finger topology and optimizing the width-to-length ratio of each finger. Although the C_{gd} and r_g plays important roles in defining the f_{max} of a single transistor, interconnections should not be neglected for a complex circuit when employing two or more transistors.

For a single-ended power stage with total channel width of W_1+W_2+W_3=120 μm biased at 300 μA/μm, lumped parasitics are added to the source of the transistors to simulate the effect of interconnections. Fig. 5.5 illustrates the power loss caused by the source parasitic resistance/inductance introduced by interconnects. These parasitic elements create a local feedback, so that a very large gain reduction is observed. Despite the gate and drain resistive/inductive parasitics have relatively low impact on the gain of the stage, the overall occupied area must be reduced to achieve the lowest possible capacitance. Source nodes are connected from both sides on Metal 3 and connected to the bulk and virtual ground planes around the transistors. Wide

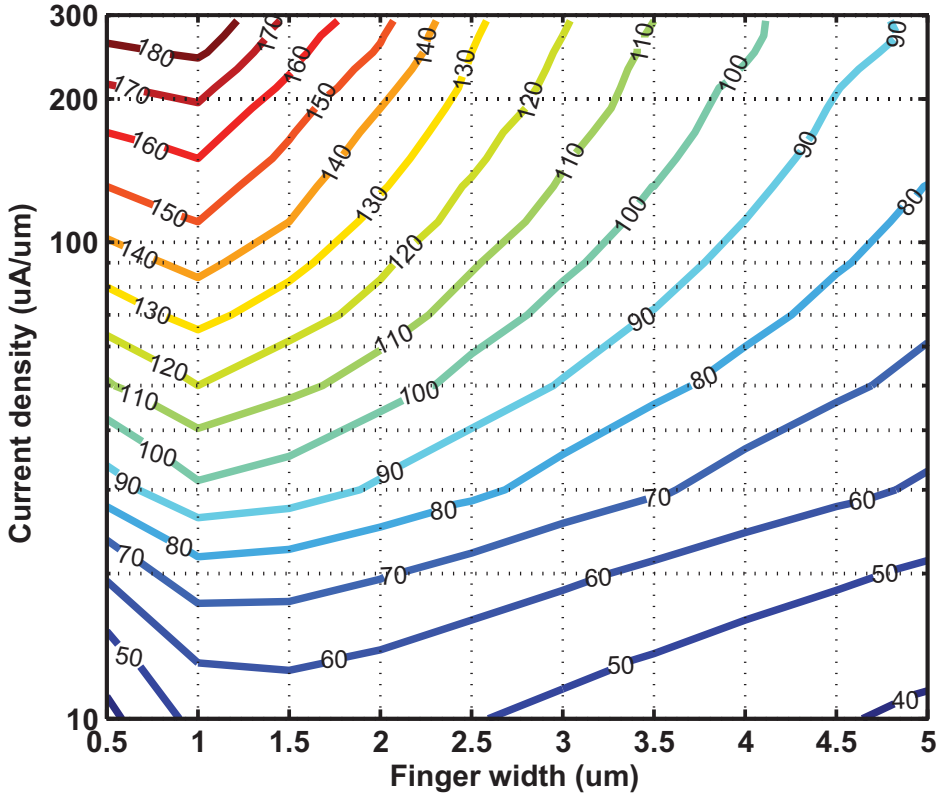


Figure 5.6: Extracted f_{max} of dual-mode power stages from unilateral power gain with respect to the total size of the stage and current density. Devices are 30 numbers of fingers.

metal tracks are used to decrease the series resistance/inductance. By implementing a virtual ground plane on Metal 1 and Metal 2 layers, small physical distance between source nodes and the ground planes helps to reduce the parasitics. The drain and gate connections are connected at one side. The one-side connection increases the gate resistance. However, it helps to reduce the C_{gd} parasitic capacitance, thus more isolation between I/O can be obtained by minimizing the overlap between gate and drain nodes. Via contacts are used to bring up the gate/drain connections to a wide top metal layer (M_9) which results low resistive drain/gate nodes. To choose a proper sizing for transistors, unilateral gain of the proposed dual-mode stage is simulated and f_{max} is extracted as shown in Fig. 5.6. It can be seen that a total channel width of 120 μm biased at 300 μA/μm can keep the f_{max} above 100 GHz.

Small-signal and large-signal simulations are performed to optimize the size of the transistors satisfying the gain, power and PAE specifications at 60 GHz. The main

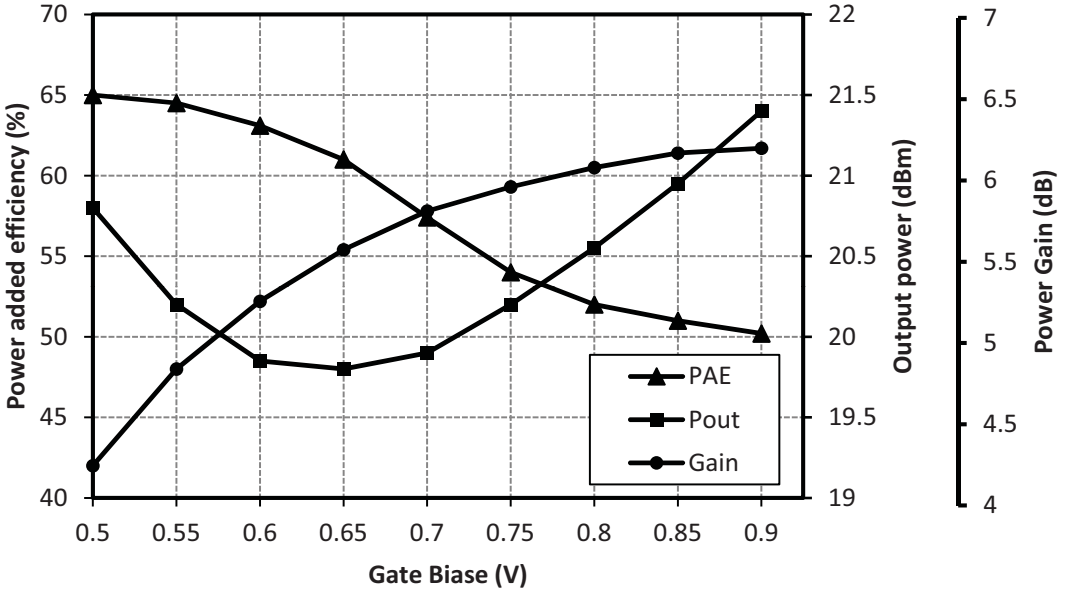


Figure 5.7: Simulated maximum power gain, output power and PAE of the proposed dual- mode stage at 60 GHz versus the gate bias (V_G).

transistor's (M_1) layout consists of 32×2μm fingers to deliver 60% of the total output current and auxiliary transistor cells are laid out in 30×0.8μm and 30×1.2μm fingers for M_2 and M_3 respectively. Fig. 5.7 shows simulation results of the proposed circuit for ideally I/O matched conditions at 60 GHz. In low-power mode, the cascode stage is turned off and the CS stage will be biased at 0.9 V which forces the amplifier to operate in class A. By connecting the gate of M_3 to V_{DD} and applying a gate bias voltage slightly greater than threshold voltage (0.5 V to 0.75 V), dual-mode stage operates in class AB mode and delivers average power of +13 dBm at such high PAE of greater than 60%. The low power gain of dual-mode stage will be boosted by cascading driver and gain stages. To obtain a +3dB rise in output power, two dual-mode units are designed in differential mode. Hence, the maximum voltage swing of the power stage will be increased by 100%.

We propose a topology to combine four individual differential units using a 4-way power combiner. Hence, the output power can be increased by +6dB theoretically. In addition to increasing output power, the proposed combiner topology is designed to match the 50Ω load to the optimum output impedance of each differential stage simultaneously. Load-pull simulations are performed to choose the optimized load impedance of dual-mode units. Fig. 5.8 shows the simulated load-pull contours for

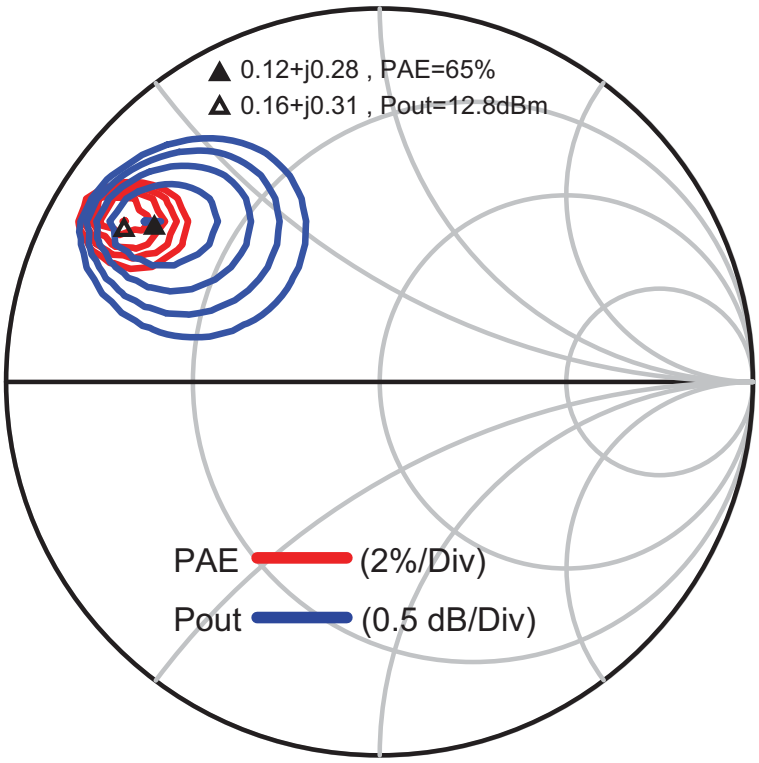


Figure 5.8: Load-pull simulation of the proposed dual-mode stage ($V_G = 0.75$).

a 120 μm single-ended dual-mode stage biased at 300 μA/μm. The optimum load impedance of 6-7 Ω is found in simulations to obtain 65% PAE and maximum output power of 12.8 dBm. Also, load-pull simulations reveal that inductive impedance is required to cancel the parasitic capacitor of the transistor outputs. The differential mode topology results in 12-14 Ω output impedance which requires combining of four individual units in series to be matched at 50 Ω.

Fig. 5.9 illustrates the circuit topology of the 60 GHz PA including dual-mode differential DAT PA stages followed by a CS driver and transformer-feedback neutralized cascode gain stages respectively. Using the proposed topology for DAT combiner and splitter, four dual-mode differential PA cells can be combined and matched to the 50Ω load in such a small occupied area. Unlike the conventional DAT structures, using spatial power dividers (e.g. Wilkinson) are avoided in our proposed topology because of the large occupied area and high insertion loss of bulky transmission lines. Small occupied area by passive structures decreases the power loss and increases the

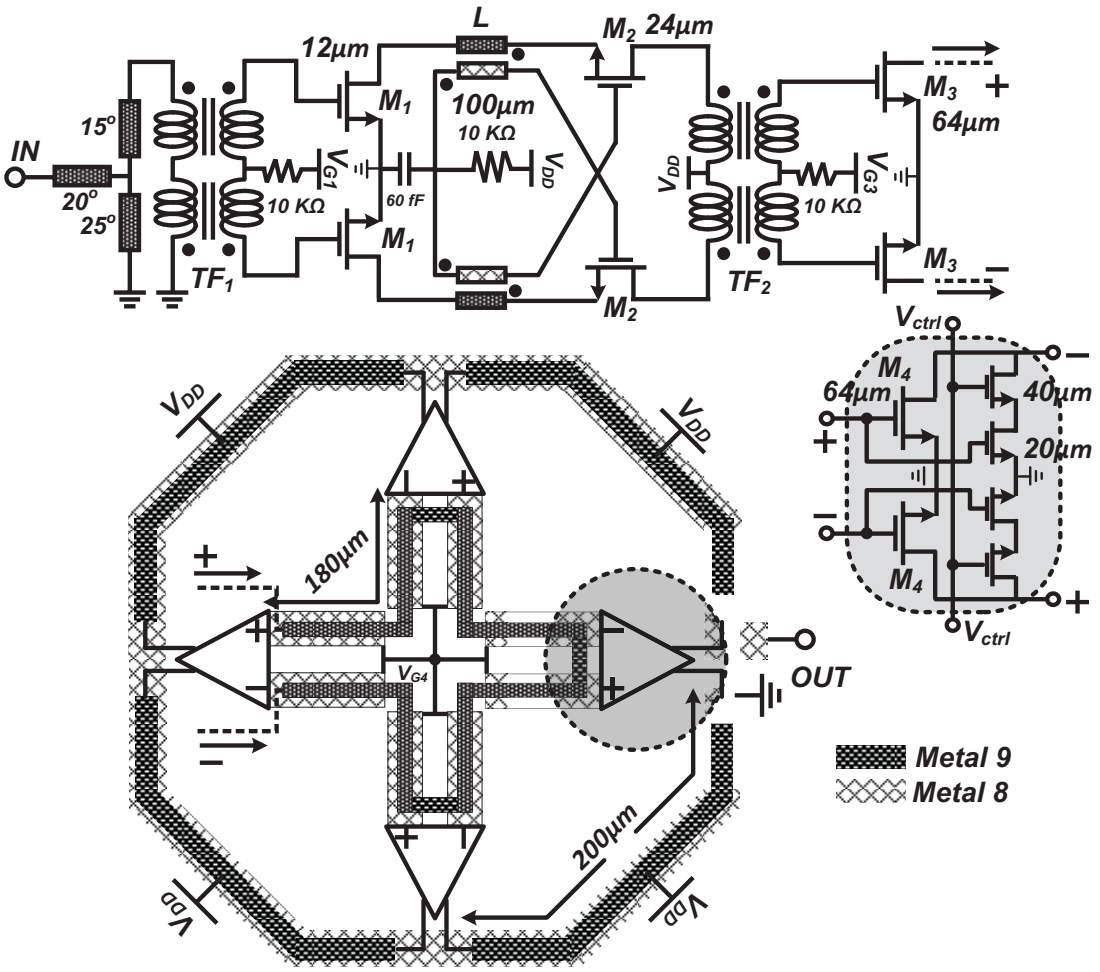


Figure 5.9: Schematic of the proposed three-stage 60 GHz differential dual-mode PA including layout of the proposed DAT topology.

resonance frequency of transformer power combiners. The major advantage of the proposed DAT topology is designing a compact, low-loss power divider inside the power combiner. Moreover, the proposed technique enables power combining of four differential PA stages instead of two PAs which has been implemented using conventional DAT structures reported in literature.

Design procedure of the proposed DAT topology begins with optimizing the size of the output windings to achieve the required impedance transformation ratios. Using series combining configuration, each differential stage has to be matched to the $50\Omega/4 = 12.5\Omega$ which requires ITR of unity. The low ITR required for this topology enables

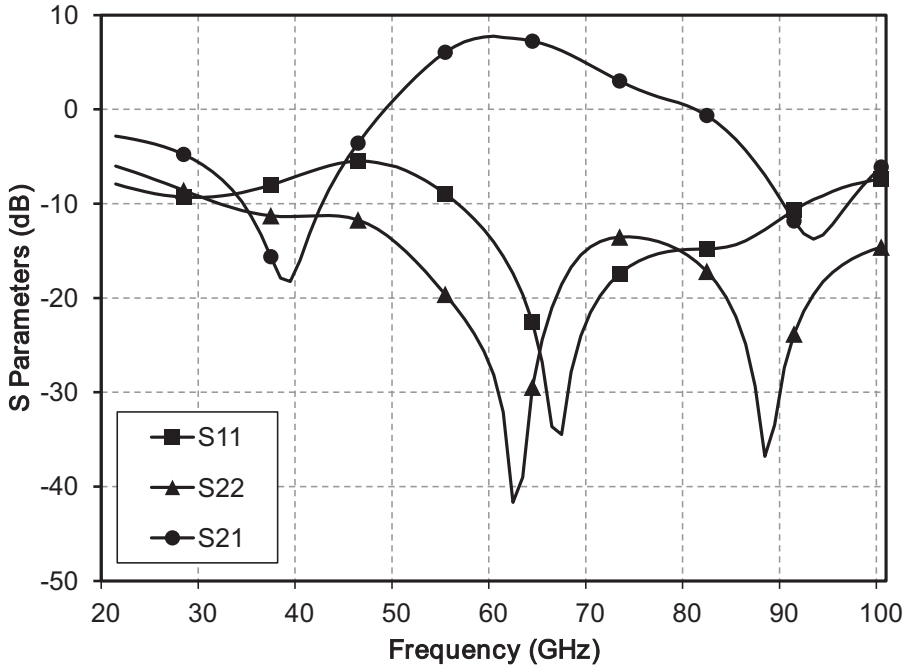


Figure 5.10: Simulated S-parameters of the proposed dual-mode DAT.

power combining at higher efficiency compared to conventional counterparts at 60 GHz. Implementing such a low ITR is feasible using small sized primary/secondary windings in a stacked transformer topology. The primary and secondary windings of the proposed DAT are implemented on ultra-thick (M_9) and thick (M_8) metal layers with 3.4 μm and 0.85 μm thickness featured in 1P9M technology respectively. Small-size low loss stacked transformers are designed in this technology due to the availability of ultra thick metal layers. The metal layers with different thicknesses with less than a micrometer gap between them allows for realization of different ITR by small changes in the size of the transformers. With the maximum DC current handling (I_{max}) of 10 mA/μm^2, the ultra-thick layer enables the transformers to be used as compact biasing network of power devices. Design procedure of stacked transformers are studied in chapter 3. The effective inductance and power transfer efficiency based on EM simulation results are demonstrated in previous chapter (Fig. 3.26) for octagonal-shape stacked transformers with various inner diameters.

EM simulations are performed to optimize the length and width of primary/secondary windings of the DAT combiner. With less than +1dB return loss, 200μm length windings with 6 μm width metal traces satisfy the required ITR. The input power of the

DAT structure is provided by a differential driver stage along with the power divider. Simultaneously, the power divider performs the impedance matching between the second stage and the DAT PA stages. The gate contacts of the 120 μm dual-mode power devices are connected to the top layer using via array and the input impedance is calculated to optimize the size of the power divider. Assuming a 7 dB power gain for the last stage, the driver stage must be designed to provide a minimum output power of +10 dBm in order to achieve a power of +14 dBm at output stages.

Such output power is achievable using differential CS amplifier with 64 μm channel width (M_3). Thus, an ITR of 0.5 is required for power divider which is obtained by 180 μm windings implemented on M_9 and M_8. Fig. 5.10 illustrates the S-parameter simulation results of the last stage of the proposed DAT structure for a wide frequency range. Dual-mode amplifier is biased in class AB using a low V_G of 0.75 V. Maximum power gain of 6.5 dB is achieved due to the low loss I/O power combiner/divider. The maximum output power is 21 dBm based on the simulation results.

5.1.2 Design of driver stages

A commonly used technique to increase the PAE of the amplifier is to increase the power gain, thus the PA can be driven with very low input power levels. In order to achieve high power gain, the DAT structure is driven by a differential CS stage followed by an enhanced cascode stage. The output of the CS stage is matched and divided into four PA stages using 180μm length 4-way stacked transformer-based splitter implemented on M_9 and M_8 metal layers. As it is shown in Fig. 5.6, NMOS transistors with 64μm channel width are chosen for this stage. Biased at 300 μA/μm, this stage could achieve +10 dB power gain and deliver +9dBm output power at 1dB compression point.

Although a total power gain of 17 dB could be achieved at 60 GHz, the final design must be able to provide enough gain for a wide frequency range which is a primarily requirement for 60 GHz application. In order to achieve a wide bandwidth, each stage is designed at different center frequency with 5 GHz frequency differentiation. Hence, an extra gain stage is required to fulfill the 60 GHz wide bandwidth requirements. To increase the overall gain of the amplifier, a neutralized cascode stage is cascaded before the CS stage. Using cascode stage improves isolation between I/O and increases stability of the whole amplifier by decreasing the

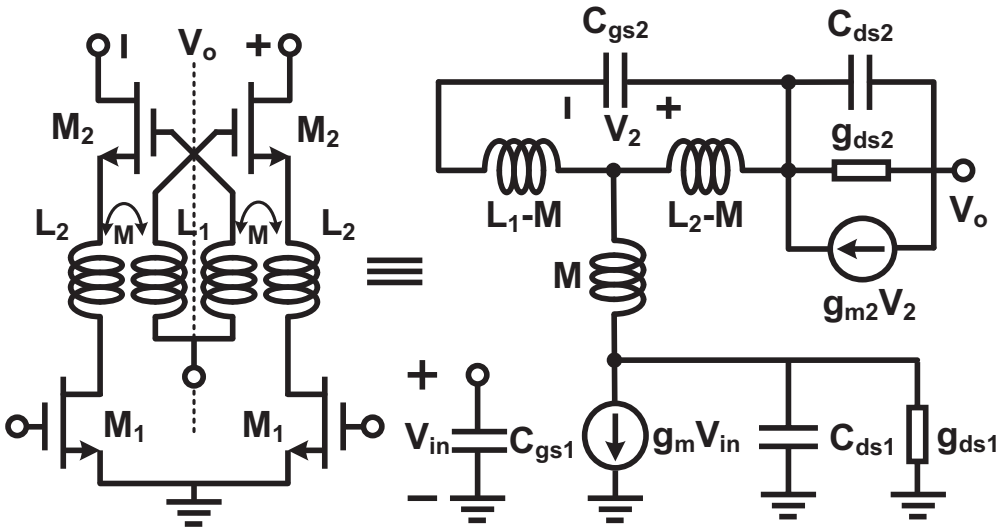


Figure 5.11: Small-signal model of the gain-boosted cascode stage.

S_{12}. Inter-stage matching circuits are implemented using highly efficient stacked octagonal transformers at 60 GHz (TF_2) to achieve low loss coupling between cascode and CS stages. Neutralization techniques utilizing transmission lines, cross-coupled capacitors, and on-chip inductors are conventional methods to boost the power gain of cascode amplifiers [55] [61] [112]. The proposed neutralization technique, as shown in Fig. 5.9, uses small sized cross-coupled transformer feedback between differential cascode stages to perform the parasitic canceling and current reuse techniques simultaneously. Fig. 5.11 illustrates the equivalent small signal circuit model of the proposed technique. The transformer is replaced by an equivalent T-circuit model for simplicity. In order to compensate the frequency response, the transformer primary/secondary windings can be sized to resonate with inherent parasitic capacitance of MOSFETs. The following conditions must be applied to fully compensate the capacitances.

$$M.C_{ds1}.\omega^2 \simeq 1. \tag{5.1}$$

$$(L - M).C_{gs2}.\omega^2 \simeq 1. \tag{5.2}$$

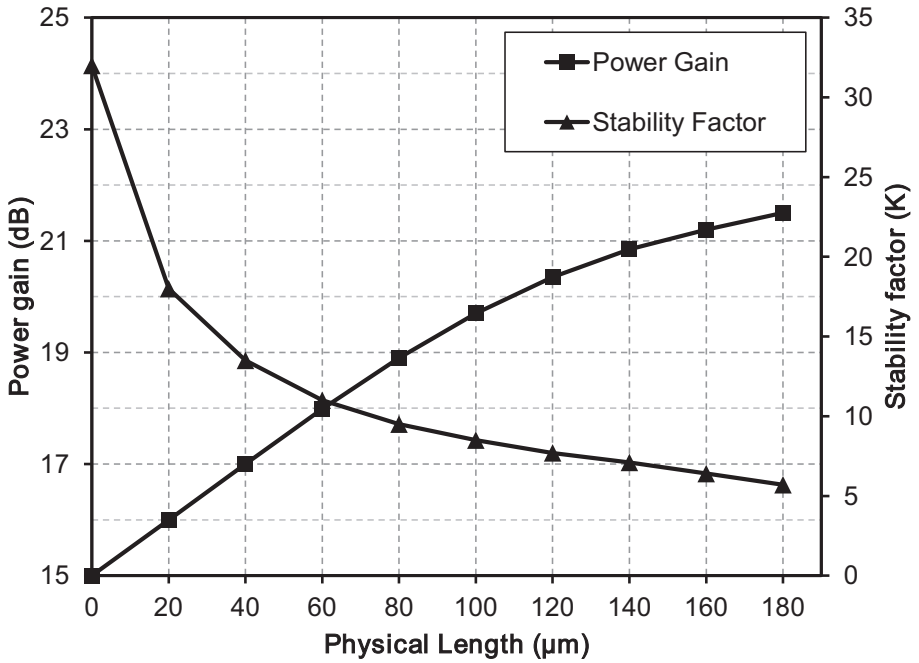


Figure 5.12: Simulated power gain and stability factor of transformer-based neutralized cascode stage.

$$(L - M).C_{ds2}.\omega^2 \simeq 1. \tag{5.3}$$

where, L_1 and L_2 are the primary/secondary inductors respectively and M is the mutual inductance between windings defined as $M_2 = L_1.L_2$. Fig. 5.12 shows simulated gain and stability of the enhanced cascode stage respect to the physical length of the slab transformer. In this design, total channel width of 12 μm and 24 μm with 24 fingers are selected for cascode stage transistors (M_1 and M_2), respectively. The main transistor M_1 is miniaturized to consume less than 5% of the overall DC power while achieving high gain and high input impedance. Stability issues are important concern while using neutralization techniques as they apply a feedback on the circuit. Although the stability factor (K) of the stage is decreased, the power gain of the cascode stage could be improved by +4 dB with 100 μm length transformer under stable conditions with K higher than five. Obtaining higher gain from neutralized stage improves the overall PAE of the PA compared to a normal cascode stage biased

at equal current level. In order to obtain a low return loss within a wide bandwidth, a two stage input matching network is designed. T-section bended microstrip line followed by a stacked transformer (TF_1) is used to match the high impedance (100Ω) of the differential cascode stage to a 50Ω input.

The stacked transformer operates as a differential to single-ended balun and the microstrip T matching circuit tunes the S_{11} at the desired center frequency. One particular feature of using on-chip transformers is the availability of low parasitic compact DC feed networks. Center tap of on-chip transformers are connected to DC pads to create biasing paths for gate and drain of transistors. 60 fF MOM capacitors are paralleled along the DC rails to create capacitive path to ground for all DC nodes. The gain and driver stages are biased at 300 μA/μm (V_G = 0.9 V, V_{DD} = 1.2 V). The overall power gain of 25 dB is achieved within a wide bandwidth of 18 GHz based on S-parameter simulation results. Saturated output power of 21 dBm is obtained at 29% PAE by performing single-tone large signal simulations.

5.2 Three-stage Dual-Mode DAT 60 GHz PA Simulations and Measurement Results

The 60 GHz DAT dual-mode PA prototype is fabricated in 1P9M 65nm standard CMOS technology. Fig. 5.13 presents the chip micrograph of the fabricated PA. It occupies only 0.27 mm^2 including the pads and DC feed networks. The S-parameter measurements are performed using Agilent N5251A 110 GHz solution which uses an E8361 PNA and the results are calibrated using SOLT (short-open-load-thru) calibration substrate. Amplifier's I/O are matched to 50 Ω. Fig. 5.14 illustrates the measured S-parameters compared to the simulation results in HP and LP modes. Maximum power gain of 22 dB is measured in HP mode within a 3dB bandwidth of 14 GHz from 57 to 71 GHz shown in Fig. 5.14(a). The amplifier exhibits 20 dB maximum power gain within 13 GHz bandwidth in LP mode as shown in Fig. 5.14(b). Although the matching circuits are designed for HP mode operation, the gain difference between two modes is only 2dB inside the bandwidth. The output of the amplifier is perfectly matched for wide frequency range because of the measured S_{22} less than -20 dB. Compared with the simulation results, the S_{21} has a negligible shift to higher frequency and degraded by only 2 dB due to the inaccuracy of transistor

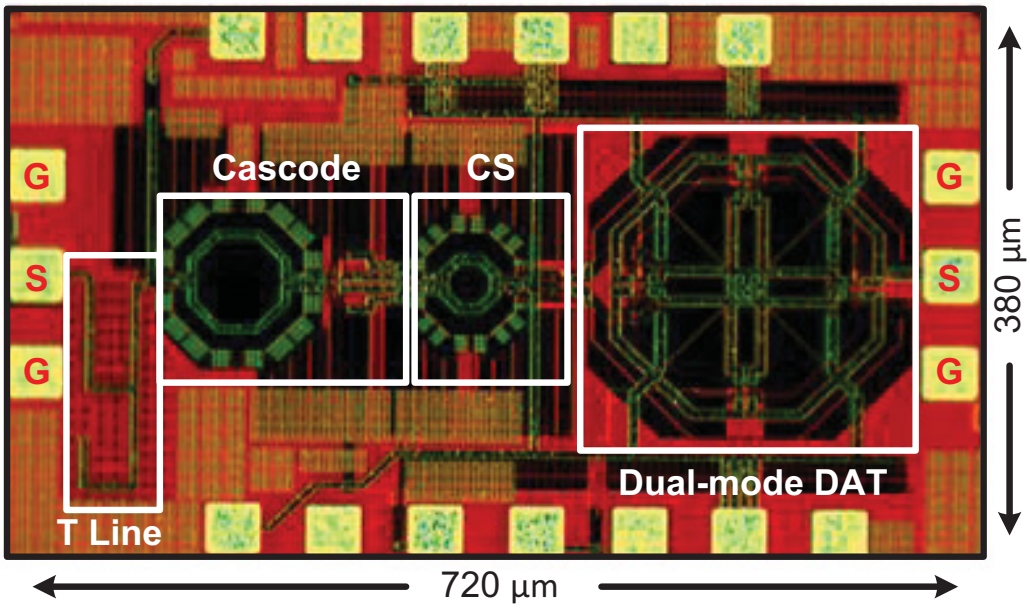
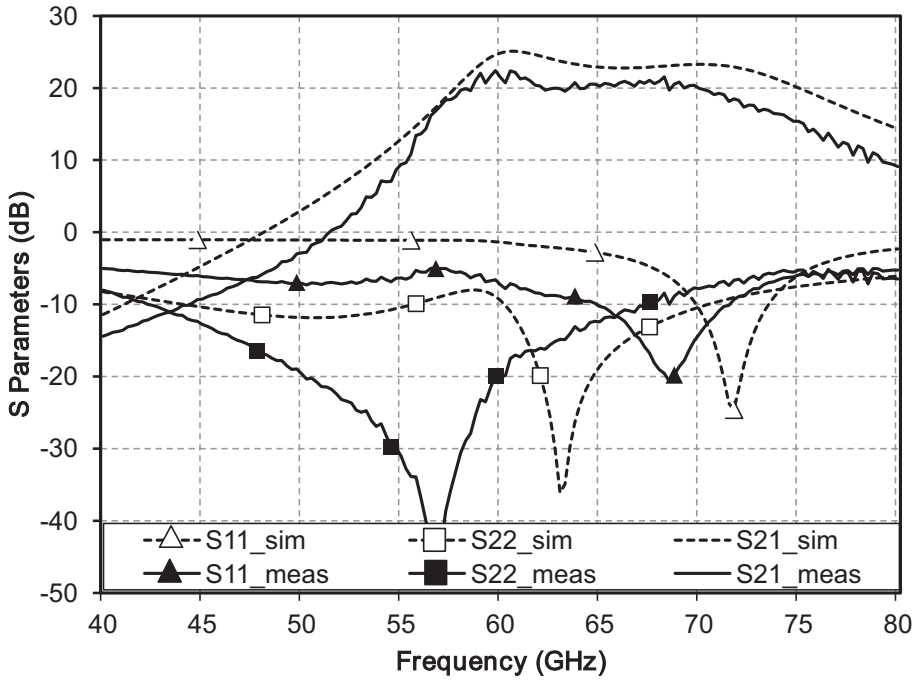


Figure 5.13: Chip micrograph of fabricated 60 GHz dual-mode DAT power amplifier.

model at 60 GHz. Also, measured S_{11} and S_{22} experience frequency shift compared to simulation results probably because of the in-accurate models of active devices or matching components. However, S_{22} reaches minimum value of -45 dB which presents an excellent output matching at 57 GHz. The input return loss reaches -20 dB whereas the S_{22} is measured to be -10 dB. Although the PA is optimized to operate in HP mode, the measured results in LP mode show a minimum gain of 17 dB and wide bandwidth which guarantees the functionality in LP mode as well as HP. Measured S_{22} reaches minimum value of -22 dB at 55 GHz and 63 GHz in LP mode. The PA demonstrates good output matching based on the measured S_{22} of less than -10 dB from 40 GHz to 70 GHz. In LP mode, there is a frequency shift in S_{22} because of the changes in capacitive parasitics seen by output stage. The PA operates functional inside the IEEE802.15.3c band and it offers a minimum power gain of 20 dB at 64 GHz. As shown in Fig. 5.15, with the stability parameter (μ-factor) of greater than unity, the amplifier is unconditionally stable from 10 MHz to 80 GHz.



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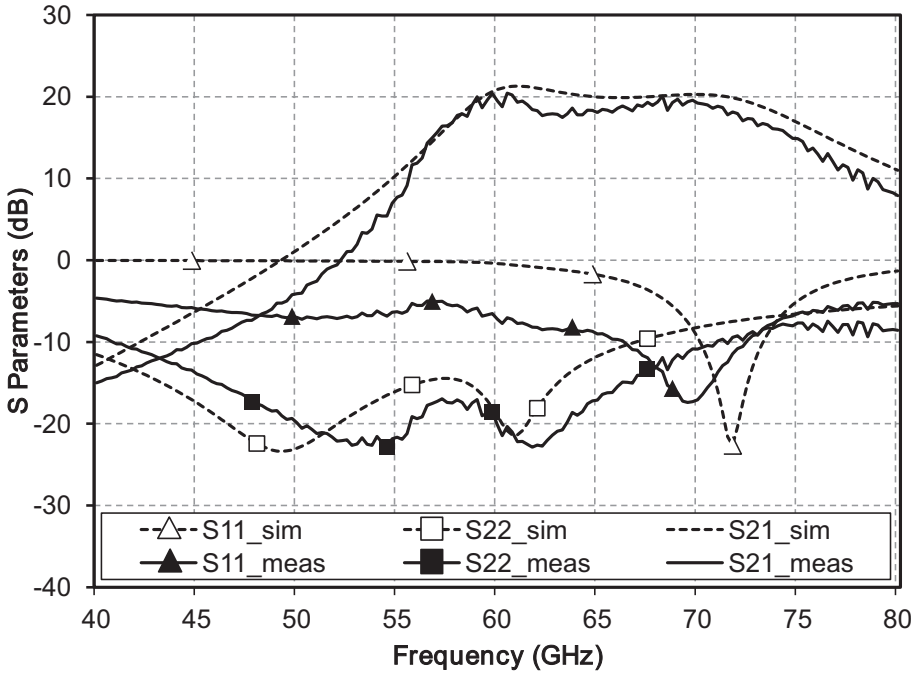


(b)

Figure 5.14: Small-signal measurements and simulation results, a) low power (LP) class A mode, b) high power (HP) class AB dual-mode.

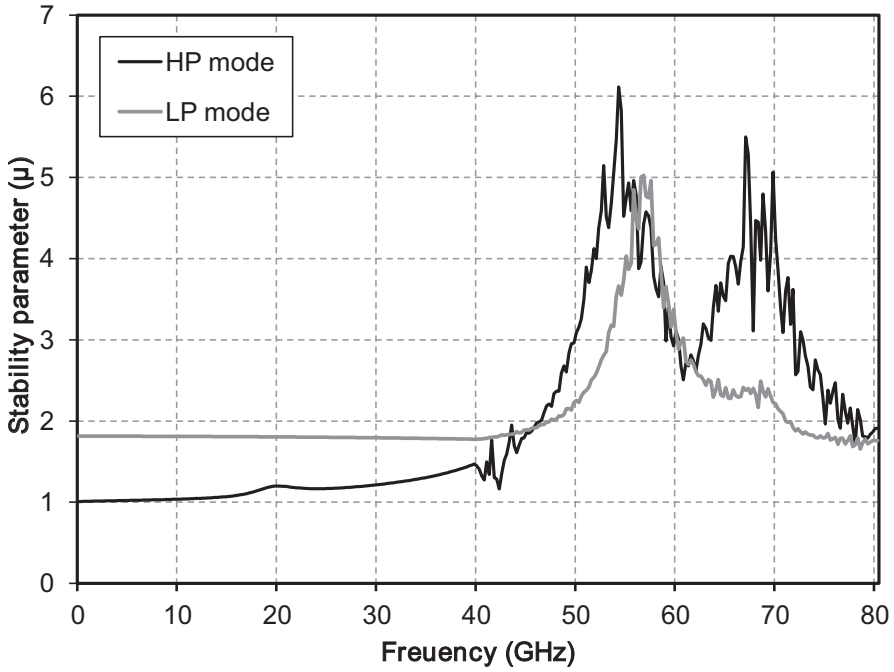


Figure 5.15: Measured stability parameters for low/high power modes.

Large-signal measurements are performed using Rohde-Schwarz 110 GHz NRP-Z precision thermal power sensors and the Rohde-Schwarz ZVA67 VNA up to 67 GHz. The losses of the probe tips, port adapters and coaxial cables are measured and de-embedded from the raw data during the power calibration process. The P_{sat} and PAE are measured at 60 GHz in LP and HP modes as shown in Fig. 5.16. By applying a 1.2V core supply, 1dB compressed output power of 15.5 dBm and the P_{sat} of 19.7 dBm are measured which are only 0.8 dB less than the simulation results. With relatively high measured P_{1dB}, the PA exhibits linear gain up to 4 dB below the saturation level. The measured peak PAE is 25% while the PA could achieve 29% in simulations probably because of the frequency shift and inaccurate large-signal device models at 60 GHz. The PAE has a value close to its maximum value when the PA runs into saturation. Power stages are biased in class A ($V_G = 0.9$ V) to achieve high saturated output power. With the same biasing condition, P_{sat} of 17.8 dBm with maximum PAE of 19% is measured in LP mode biased in class A. The proposed PA achieves more than 10% PAE at 6dB back-off level which could be improved by optimizing the driver and gain stages at lower current densities.

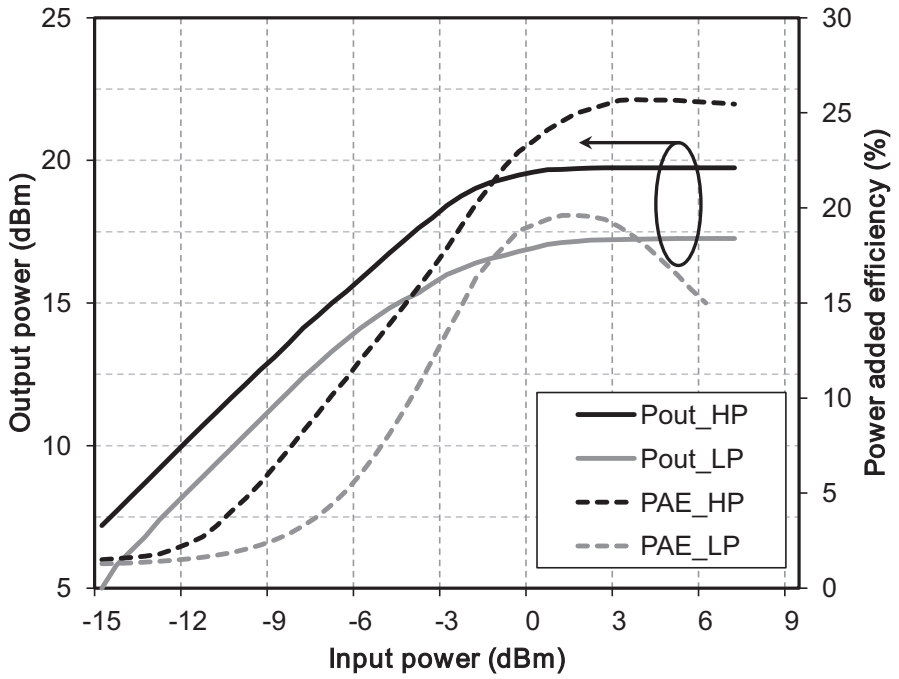


Figure 5.16: Measured output power and PAE of the fabricated PA in HP and LP modes.

Linearity measurements of the PA are performed using two-tone measurement and evaluating the inter-modulation products. Two internal signal sources are connected to the combiner in the mmW extension unit provided by four-port R&S ZVA67 so that a two-tone signal is available at the probe tips. The wide RF modulation bandwidth of the baseband generator allows the relative tone spacing of 50 MHz around the carrier frequency of 61 GHz. Measured IMD3 products of the PA are illustrated in Fig. 5.17 for both LP (Class-A) and HP (Class-AB) modes of operation. Although the 2dB more IMD3 is measured at lower input power levels, but the amplifier exhibits an IMD3 of less than -20 dBc at P_{1dB} (15.5 dBm).

Output power and efficiency of the PA are measured over IEEE 802.11.3c band to clarify the robustness of the PA against the frequency. Measured results are shown in Fig. 5.18 versus frequency. As shown in Fig. 5.18(a), the PA maintains an average P_{sat} of 19.3 dBm in HP. The average P_{sat} is degraded by only 2 dBm in LP mode. The average P_{1dB} of 14.9 and 12.6 are measured within 8 GHz bandwidth from 58 GHz to 66 GHz. The measured PAE of the PA varies from 13.4% to 25% based on the mode of operation and the frequency band. The amplifier exhibits a flat power gain

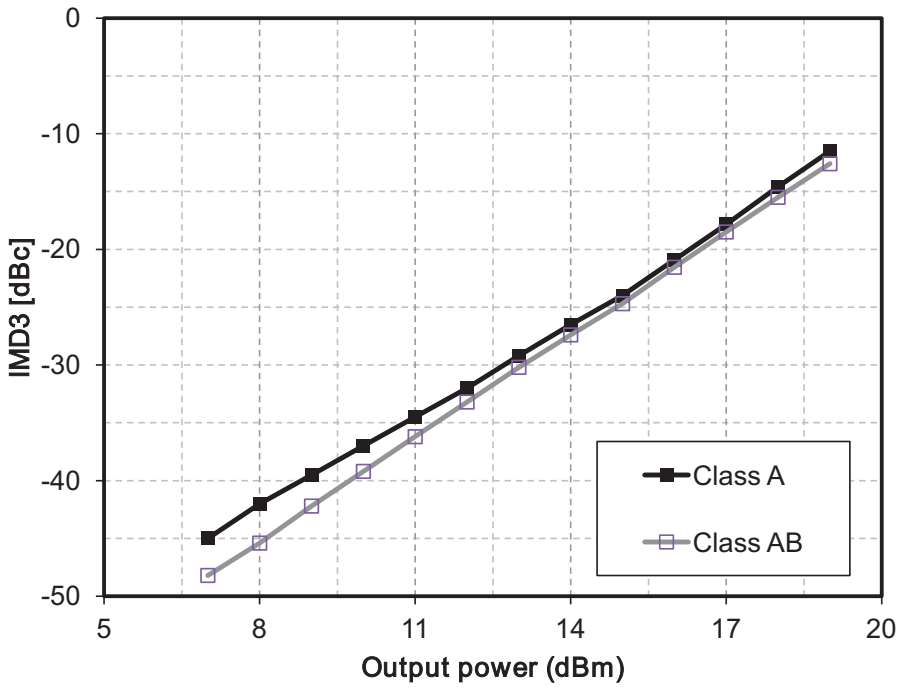
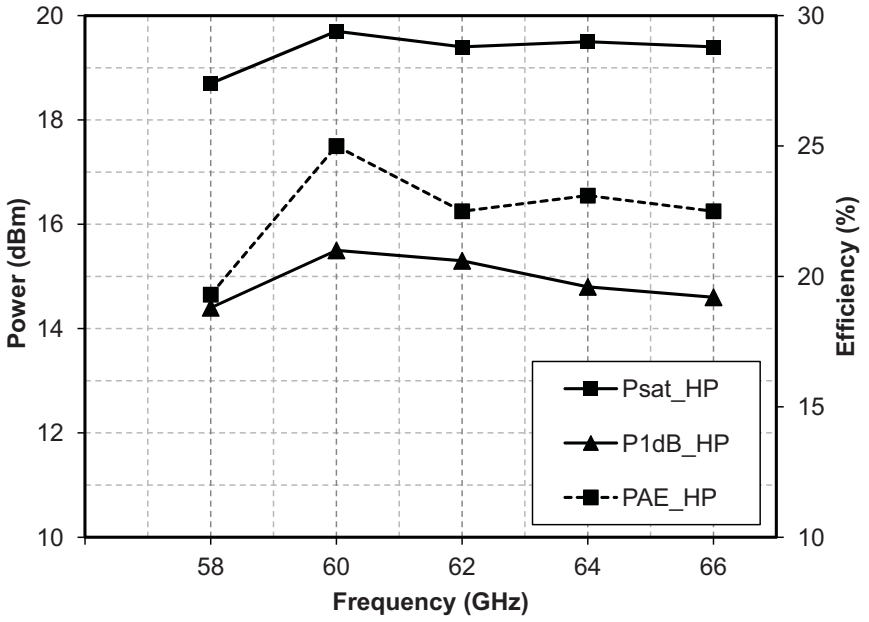


Figure 5.17: Measured third-order inter-modulation in class A and class AB.

and output power versus frequency which guarantee a high performance for 60 GHz wireless HD applications. Table. 1.2 summarizes a comparison with state-of-the-art 60 GHz PAs in modern CMOS technologies. The PA reported by [82] achieved the highest reported PAE in 40nm CMOS technology which has much higher f_{max} and power gain compared to the 65nm technology. Although the achieved PAE is lower than the value reported by [82], the proposed DAT structure could deliver highest reported P_{sat} of 19.7 dBm. Based on the ITRS figure of merit, proposed 60 GHz dual-mode PA is smaller in size and achieves comparable higher output power which results in higher FoM compared to the reported PAs in 65 nm technology.



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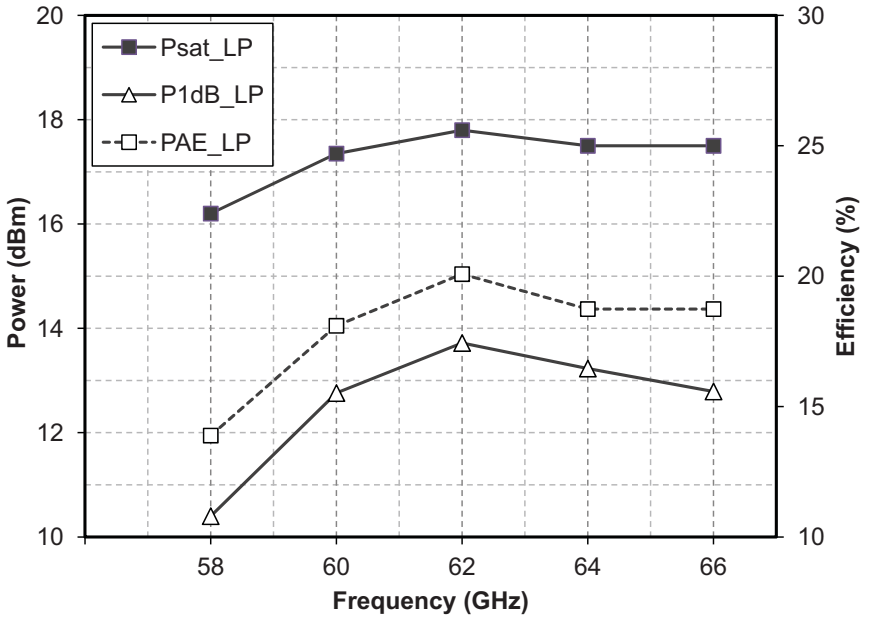

(b)

Figure 5.18: Measured PA saturated output power, P_{1dB}, and PAE over the IEEE 802.15.3c band, a) low power (LP) class A mode, b) high power (HP) class AB dual-mode.

5.3 Summary

This chapter presents design flow of a 60 GHz differential DAT PA introducing a new topology of dual-mode power amplification. The proposed topology employs a Class-AB cascode stage combined with a Class-A CS stage in order to increase the overall PAE. A new DAT layout topology is designed to combine the output power of four differential PA cells. Compared to the previous DAT structures, our topology could perform the power splitting as well as the power combining in very small area on chip. In order to increase the overall power gain, a new parasitic cancellation technique is employed the cascode stage. Using our proposed structure, the fabricated PA exhibits an output power of 19.7 dBm which is the highest reported P_{sat} in 65 nm CMOS technology. The dual-mode PA topology could increase the maximum PAE to 25% whereas the power gain is measured to be 22 dB. Performance comparison of the fabricated PA with the state-of-the-art 60 GHz CMOS PAs reported in literature is presented in Table. 5.1. Presented in [113], our proposed PA exhibits better performance based on the FoM provided by ITRS. Designing compact and efficient DAT topology, the PA obtained higher power density per area on chip compared to other similar works. Moreover, proposed PA offers 14 GHz BW which enables high data-rate wireless HD video streaming within the 60 GHz band.

Table 5.1: Performance comparison of the state of the art 60 GHz PAs.

L_{min} [nm]	V_{DD} [V]	B.W [GHz]	Stages	Mode	Topology	Combiner	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	Size [mm^2]	mW/mm^2	FoM	Ref.
65	1.2	14	3	d	cs	4x	19.7	15.5	22.0	25.0	0.27	345	91	T.W
65	1.0	6	3	d	cs	2x	17.8	13.8	11	12.6	0.28	215	75	[62]
65	2.4	9	2	s	cs	2x	15.4	13.7	17.2	14.3	0.25	139	79	[53]
65	1.8	7	4	d	cs	4x	15.6	13.5	20	6.6	2.25	16	79	[55]
65	1.0	10	2	d	cs	4x	17.9	15.4	18.8	11.7	0.83	74	83	[52]
65	1.2	15	2	b	cs	8x	18.1	11.5	15.5	3.6	0.46	140	74	[54]
65	1.2	6	3	d	cs	-	14.6	10	23.2	16.3	0.6	48	85	[60]
90	1.2	6	3	d	cs	4x	18.5	14.7	15.7	10.2	0.38	186	80	[114]
40	1.2	6	3	d	cs	2x	17.4	14.0	21.2	28.5	0.56	98	89	[82]
28	2.1	11	3	d	cas	2x	16.5	11.7	24.4	7.4	0.15	298	85	[84]

Chapter 6

Conclusion and Future Research

6.1 Conclusion

The unlicensed 60 GHz band offers a large bandwidth of 7 GHz that enables multi-Gbps wireless communications. The significantly high path loss at 60 GHz requires mmW transceivers to deliver high level of output power in order to attain a reliable communication range. As PAs consume the majority of power in the 60 GHz transceiver, the efficiency of PAs significantly influence the overall power efficiency of the system. Low-power high-speed 60 GHz front-ends on a single chip are feasible considering the continuous scaling of CMOS technology. However, design of efficient CMOS power amplifiers delivering high output power remains challenging because of low power gain of transistors at mmW frequencies, low breakdown voltage of CMOS transistors, losses of interconnects and on-chip passive components in deep sub-micron CMOS process. To address the aforementioned issues, several mmW power combining methods, new circuit topologies and layout techniques have been introduced.

In this dissertation, we have proposed new power combining and circuit topologies to improve the output power and efficiency of 60 GHz PAs. First, a new 4-way power combining topology is designed based on multi-conductor coupled lines that addresses the shortcoming of conventional topologies such as low coupling/quality factor of two conductor transformers. The design flow and measured results of a fully integrated three-stage 60 GHz PA are presented. Power transistors are modeled based on the DC, small-signal measurements and load-pull simulations. Passive impedance matching networks including on-chip inductors and transformers are fully characterized using circuit models and 3D EM simulations. The proposed technique is compared with

conventional power combining methods using EM simulation. Inside 60 GHz band, our approach exhibits higher power transfer efficiency and higher coupling factor compared to classic combiners. Biased in class A mode, the PA delivers an output power of 18.3 dBm at maximum PAE of 15.9%. Compared to the 60 GHz CMOS PAs reported in literature, proposed PA significantly improves the output power per area on the chip.

Second a dual-mode differential CMOS power amplifier for 60 GHz applications has been implemented in 65 nm CMOS technology. New power amplification method is developed to improve the efficiency of mmW PAs. Utilizing the new dual-mode technique, the proposed PA topology provides higher PAE at higher output power rates in comparison with the conventional Class-A amplifiers. The PA core consists of an enhanced cascode driver stage followed by two cascaded common source stages with transformer-based inter-stage matching in order to increase the overall power gain. The bandwidth of the cascode stage is optimized using an inductive compensation technique. The proposed technique compensates the undesired intrinsic parasitic capacitances of the cascode stage. Hence, the operating bandwidth of cascode stage is increased. Compared to the conventional cascode stage, enhanced cascode topology provides higher power gain at 60 GHz. Hence, the overall PAE of the PA is increased. The peak power gain of 17.7 dB and 16.8 dBm saturated output power are measured inside 12 GHz bandwidth. The 3dB bandwidth of the PA is significantly increased using our proposed topology in high power mode. Fabricated PA achieves a maximum PAE of 17.2% and 14.5% in low power and high power modes respectively. The 0.32 mm^2 die consumes 378 mA from a 1.2V supply.

Finally, a new differential DAT topology for 60 GHz PA applications is developed to improve the PAE and P_{sat} simultaneously. In this study, we have shown that the implementation of switching 60 GHz PAs are not feasible in 65 nm technology because of the f_{max} limitations. A new dual-mode amplifier circuit topology is proposed to overcome the power/efficiency trade-offs of non-linear PAs. Utilizing the proposed technique, the 60 GHz PA provides a higher PAE compared to the conventional Class-A amplifiers. A new layout topology of DAT power combiner and splitter is developed in order to increase the output power. The proposed DAT topology enables power combining of four differential stages in a very compact die area and with a high power transfer efficiency. Hence, the output power and PAE are increased significantly. The PA core consists of a 4-way DAT power stages with new layout topology followed

by CS and neutralized cascode stages with transformer-based inter-stage matching circuits. Dual-mode differential power stages enable the power amplification in both Class-A and Class-AB modes to increase the PAE. The performance of the cascode gain stage is optimized using a new cross-coupled transformer-based compensation technique. The peak power gain of 22 dB and 19.7 dBm saturated output power are measured over a wide bandwidth of 14 GHz. The 0.27 mm^2 die area consumes 320 mA from a 1.2V supply in HP mode and obtains 25% PAE. The proposed PA achieves the highest reported PAE and gain-BW product in comparison with the fabricated 60 GHz PAs in 65nm technology. With comparable linearity based on the measured P_{1dB} and IMD3, implemented PA obtained the highest saturated output power per area on die among the reported 60 GHz CMOS PAs.

6.2 Future Research

We suggest further research to improve the performance of the 60 GHz PAs as described below:

Continuing the presented work on the design of area-efficient power combiners, new topologies can be developed to combine output power of more than four PA cells to achieve a higher output power and efficiency. This can be obtained probably using a combination of octagonal stacked transformers and side-by-side slab conductors to enable efficient eight-way power combining. A combination of T-Line based combiners with on-chip transformers might be an alternative solution.

Design of non-linear PA classes with sufficient output power is not feasible in 65 nm CMOS technology with low gain and f_{max} (e.g. f_{max} = 180 GHz). However, with the recent advances in CMOS technologies, ultra deep sub-micron and FD-SOI devices are available with relatively high f_{max} (e.g. 28 nm technology with f_{max} = 300 GHz). Design of nonlinear classes such as Class-AB or switching PAs like Class-E can be realized using ultra deep submicron MOSFETs. This can potentially increase the efficiency of the next generation 60 GHz PAs possibly to 30% or more.

We presented dual-mode techniques to improve the efficiency of the PA when amplifier operated near compression point. The fabricated PAs exhibits 10% PAE at 6dB back-off levels. However, efficiency enhancement at higher backed-off power levels and good linearity characteristics are desired for high data rate communication with high peak-to-average power ratios (e.g. 9 dB back-off is required for 54 Mbps). Doherty PA has emerged as one of the main solutions in efficient PA designs at high back-off levels. The application of Doherty amplifier is not investigated in 60 GHz CMOS PAs because of the low f_{max} of the devices and poor AM-PM distortion of the Doherty PA. With availability of ultra-deep sub-micron devices, Doherty amplifiers can be implemented at 60 GHz. In addition to this, availability of linearization techniques such as digital predistortion can potentially solve the key linearity problem with Doherty PAs.

6.3 Related Publications

As the result of the presented research work, the following articles have been published or submitted for publication:

- Payam Masoumi Farahabadi, and Kambiz Moez, "A 60 GHz Dual Mode Distributed Active Transformer Power Amplifier in 65nm CMOS", IEEE Transactions on Very Large Scale Integration Systems, Issue: 99, Nov. 2015.
- Payam Masoumi and Kambiz Moez, "A Dual-Mode Highly Efficient 60 GHz Power Amplifier in 65 nm CMOS", IEEE Radio Frequency Intergated Circuits Symposium, Miami, Florida, USA, pp.155-158, June 2014.
- Payam Masoumi and Kambiz Moez, "Compact High-Power 60 GHz Power Amplifier in 65 nm CMOS", IEEE Custom Integrated Circuits Conference, San Jose, California, USA, pp. 1-4, Sept. 2013.

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