CIRCUITS, ARCHITECTURES AND ANTENNA DESIGN FOR 5G WIRELESS TRANSCEIVERS

By

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ABSTRACT

The upcoming fifth mobile generation (5G) standard – scheduled to be launched by 2020 – has recently attracted the attention of the industrial and research communities in different fields owing to its promises to achieve higher bandwidth, data rates and support the continuously growing mobile traffic which is beyond what the current fourth mobile generation (4G) resources can afford. Huge efforts are exerted on both the system and hardware levels to shape this new standard expected to provide a paradigm shift in the wireless communications.

The limited bandwidth in the sub-6GHz bands motivated the use of the underutilized spectrum in the mm-Wave frequency bands for 5G. However, many challenges are accompanied with building the mm-Wave wireless transceivers. This includes the high path loss experienced by the transmitted/received signal owing to the high frequency propagation which requires a high gain antenna to compensate for. Moreover, on the battery-operated mobile device side, the integrated circuits blocks should provide the required high-performance levels with low power for longer battery life and the high gain antenna should have compact size and high efficiency.

This dissertation aims to share in the 5G research by providing solutions and designs to some of the mm-Wave 5G transceivers building blocks, namely; the fractional-N frequency synthesizer serving as the local oscillator (LO) for the transceiver, the analog-to-digital converter (ADC) required for the hybrid beamfoming and the antenna array.

For the LO clock generation, two mm-Wave quadrature fractional-N synthesizers were designed and fabricated in the 65-nm CMOS process; a single-stage fractional-N phase locked loop (PLL) and a cascaded fractional-N PLL. Both prototypes achieve good performance over the frequency range from 26-GHz to 32-GHz. First, the single-stage PLL is presented which

consumes 35.8-mW while achieving 500-fs jitter. For enhanced performance, the cascaded PLL is then proposed which consumes 26.9-mW and achieves less than 100-fs jitter with -112.6-dBc/Hz phase noise at 1-MHz offset in the fractional-N mode. The single-stage and cascaded PLLs achieve figure-of-merits (FoM) of -230.58-dB and -248.75-dB, respectively. The proposed cascaded PLL FoM outperforms that of the reported state-of-the-art mm-Wave synthesizers making it a suitable candidate for 5G transceivers.

For analog-to-digital conversion, two prototypes were designed and fabricated in the 65-nm CMOS process. First, a first-order noise-shaped time-domain ADC is introduced. It employs a successive approximation register time-to-digital converter (SAR-TDC) as a quantizer for higher resolution and lower quantization noise level. In addition, a 1-bit folded VCO is utilized for enhanced VCO linearity. The SAR-TDC achieves 1.15-ps time resolution with peak DNL/INL of 0.64/0.65-LSB and the 1-bit folded VCO improves the VCO linearity from 12% to 0.17%. The enhanced TDC and VCO performances are the key factors for attaining high-performance levels from the ADC. The fabricated 675-MS/s time-domain ADC achieves peak SNDR/SFDR of 79.5/86.4-dB in 10-MHz bandwidth while consuming a total of 11.65-mW. Second, a Nyquist-rate reconfigurable time-based ADC is presented. It employs a reconfigurable TDC that can be configured as a high resolution correlated double sampling SAR-TDC for the high resolution modes or as a Flash-TDC for the high sampling rate modes. The ADC supports continuous sampling rate variations from 100-MS/s to 5-GS/s providing 13- to 5-bits resolution with exponential power scaling from 8.4-mW to 22.3-mW, respectively and FoM ranging from 14.6- fJ/conv to 196-fJ/conv.

Finally, a mm-Wave substrate-integrated vertically-polarized electric dipole antenna is presented. The dipole is fabricated using vias in standard PCB process to fit at the mobile device

edge featuring wide fan-beam with high HPBW in the elevation plane ($HPBW_{ELEV}$), high gain and high front-to-back radiation ratio (F/B). For enhanced gain, parasitic-vias are added in front of the dipole. To improve HPBW without sacrificing gain, V-shaped split parasitic-vias are employed. A via-fence surrounds the dipole structure to suppress back radiation and enhance F/B. The dipole is connected to a parallel-strip line (PS) which is interfaced to the main SIW feed through a novel SIW-to-PS transition. A single-dipole, 2×1 array, and 4×1 array prototypes were designed and fabricated on the Rogers RO5880 substrate achieving measured $HPBW_{ELEV}$ > 133.1º, F/B > 36-dB, cross-polarization < -39.6-dB and 12.61-dBi gain from the 4×1 array with 95.8% radiation efficiency. The low cost, compactness, and good performance of the proposed dipole make it a competing candidate for the future 5G mobile devices transceivers.

PREFACE

This thesis is an original work by Waleed El-Halwagy under the supervision of Prof. Pedram Mousavi and Prof. Masum Hossain and was industrially sponsored by *Samsung Research America, Texas, USA* and *TELUS Communications, Canada*. Some parts of the thesis have been published or submitted for future publication as follows;

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- W. El-Halwagy, A. Nag, P. Hisayasu, F. Aryanfar, P. Mousavi and M. Hossain, "A 28GHz quadrature fractional-N synthesizer for 5G mobile communication with less than 100fs jitter in 65nm CMOS," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 118-121.

I was responsible for the system design, measurements, data collection, and analysis as well as the manuscript composition. A. Nag assisted in the system design. M. Hossain is the supervisory author and was involved with concept formation and manuscript composition. F. Aryanfar is the industrial partner from *Samsung Research America, Texas, USA* who helped with chip and PCB fabrication and financially supported this work.

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- W. El-Halwagy, P. Mousavi, and M. Hossain, "A 79dB SNDR, 10MHz BW, 675MS/s open-loop time-based ADC employing a 1.15ps SAR-TDC," *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Toyama, 2016, pp. 321-324.

I was responsible for the system design, measurements, data collection, and analysis as well as the manuscript composition. M. Hossain is the supervisory authors and was involved with concept formation and manuscript composition.

Chapter 5 has been published as

- W. El-Halwagy, R. Mirzavand, J. Melzer, M. Hossain and P. Mousavi, "Investigation of Wideband Substrate-Integrated Vertically-Polarized Electric Dipole Antenna and Arrays for mm-Wave 5G Mobile Devices," in *IEEE Access*, vol. 6, pp. 2145-2157, 2018.
- W. El-Halwagy, J. Melzer, M. Hossain and P. Mousavi, “A 28 GHz Compact Vertically-Polarized Dipole for 5G Smartphone Edge”,2017 *IEEE International Symposium on Antennas and Propagation (APSURSI)*, San Diego, 2017, pp. 2573-2574.

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ACRONYMS

ADC	Analog-to-Digital Converter
C^2MOS	Clocked-CMOS
CML	Current-mode Logic
CP	Charge-pump
CPPLL	Charge-pump phase-locked loop
CPW	Coplanar Waveguide
D2D	Device-to-device
DAC	Digital-to-Analog Converter
DCC	Duty Cycle Correction
DNL	Differential non-lineartity
DTC	Digital-to-time converter
ENOB	Effective Number of Bits
ENZ	Epsilon-near-zero
F/B	Front-to-back radiation ratio
FCC	Federal Communications Commission
GCPW	Grounded Coplanar Waveguide
GRO	Gated-ring oscillator
HPBW	Half-power beamwidth
IC	Integrated Circuits
IF	Intermediate Frequency
ILO	Injection-locked oscillator
INL	Integral non-linearity
LF	Loop filter
LO	Local Oscillator
LoS	Line-of-Sight
LSB	Least significant bit
M2M	Machine-to-machine
ME	Magneto-electric dipole
MIMO	Multiple-Input Multiple-Output
mm-Wave	Millimeter Wave
MP-TDC	Multi-phase TDC
MRC	Maximal Ratio Combining

NLoS	Non-Line-of-Sight
NTF	Noise Transfer Function
PEC	Perfect Electric Conductor
PFD	Phase-frequency detector
PGEN	Pulse Generator
PLL	Phase Locked Loop
PM	Phase Margin
PQ	Phase Quantizer
PS	Parallel-strip line
QFN	Quad Flat No-leads
RF	Radio Frequency
RX	Receiver
SAR	Successive approximation register
SHPD	Sample-and-hold phase detector
SIW	Substrate-integrated waveguide
SNR	Signal-to-noise ratio
SoC	System on Chip
SSPLL	Sub-sampling phase-locked loop
TDC	Time-to-digital converter
TI	Time-interleaved
TX	Transmitter
V→I	Voltage-to-current converter
VCO	Voltage-controlled Oscillator
VNI	Visual Network Index

1. INTRODUCTION

The upcoming fifth wireless mobile generation (5G) scheduled to be launched in 2020 is increasingly attracting the attention of the industrial and research communities in different fields. Huge efforts are exerted on both the system and hardware levels to shape this new standard expected to provide a paradigm shift in wireless communications. The interesting competition among the research community greatly motivated the 5G research. In this chapter, an introduction to 5G wireless is introduced followed by the thesis scope and outline.

1.1 Background and Motivation

The demand for wireless data services by cellular devices users is increasing exponentially over the years to support new applications and context-rich features. The Visual Network Index (VNI) reports conducted by CISCO provide quantitative data supporting this postulate [1],[2]. According to its recent reports, Cisco VNI indicated that the global mobile data traffic grew 74% in 2015 where it reached 3.7 Exabytes/month at the end of 2015 compared to 2.1 Exabytes/month at the end of 2014. The number of mobile devices reached 7.9 billion devices in 2015 compared to 7.3 billion devices in 2014. The mobile data traffic has grown 4000-fold and 400-million-fold during the past 10 years and 15 years, respectively. Besides, the report provided some interesting predictions for the mobile data traffic in 2020 where the global mobile data traffic is expected to increase by nearly 13-fold from 3.7 Exabytes/month in 2015 to 49 Exabytes/month in 2020 with the number of mobile devices increasing from 7.9 billion to 11.6 billion devices. In general, the number of devices connected to IP networks is expected to be more than 3-times the global population by 2020 [3]. Fig. 1.1 provides a plot of the expected regional mobile data traffic growth over years from 2015 to 2020 extracted from the Cisco VNI forecast report predicting a huge mobile data traffic explosion by 2020. This dictates the need for higher bandwidth and data rates which is beyond what the current 4th mobile generation (4G) resources can afford. Hence, the burden of meeting this increased capacity falls upon the upcoming 5th mobile generation (5G).

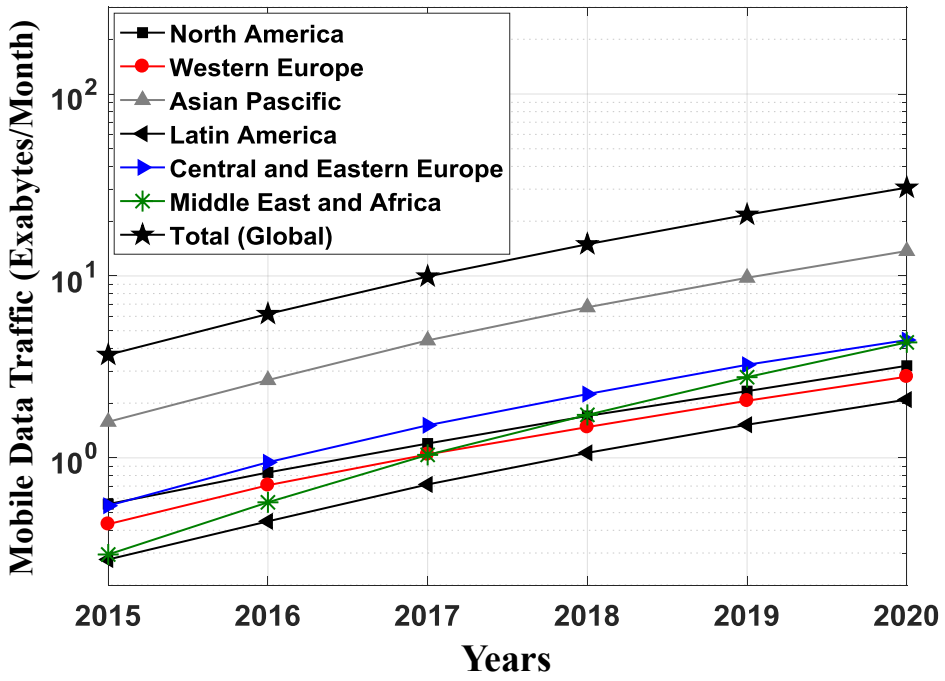


Fig. 1.1. Regional growth in mobile data traffic over years from 2015 to 2020 as predicted by Cisco VNI [2].

1.1.1 5G Expectations and Spectrum Allocation

The upcoming 5G standard is expected to provide a paradigm shift in the future of mobile communications [4]. It should achieve lower round trip latency of less than 1 ms as opposed to 10 ms in the current 4G standard [5]. Moreover, 5G should support 100× data rates compared to 4G (providing 100 Mbps for high-mobility devices to 1 Gbps for low-mobility devices) with a minimum of 1 Gbps data rate anywhere, 5 Gbps for high mobility users and 50 Gbps for low-mobility users [6]. In addition to that, the 5G handset devices are expected to have longer battery life while supporting massive multiple-input-multiple-output (MIMO) communications, Device-to-Device (D2D) communications, Machine-to-Machine (M2M) communications and Internet of Things (IoT) [7],[8]. For the 5G to be able to support higher data rates and increased capacity, a wider bandwidth is required [9]. The frequency spectrum in the sub-6 GHz bands is crowded by the current wireless mobile communications, WiMAX, Wi-Fi, GPS standards …etc. Fig. 1.2 shows the current cellular wireless standards spectrum allocation in North America on the International Telecommunications Union (ITU) radio bands scale and Table 1.1 provides detailed information of the spectrum allocated for those standards. The limited bandwidth in the wireless spectrum below 6 GHz will not be able to meet the expected mobile traffic explosion by

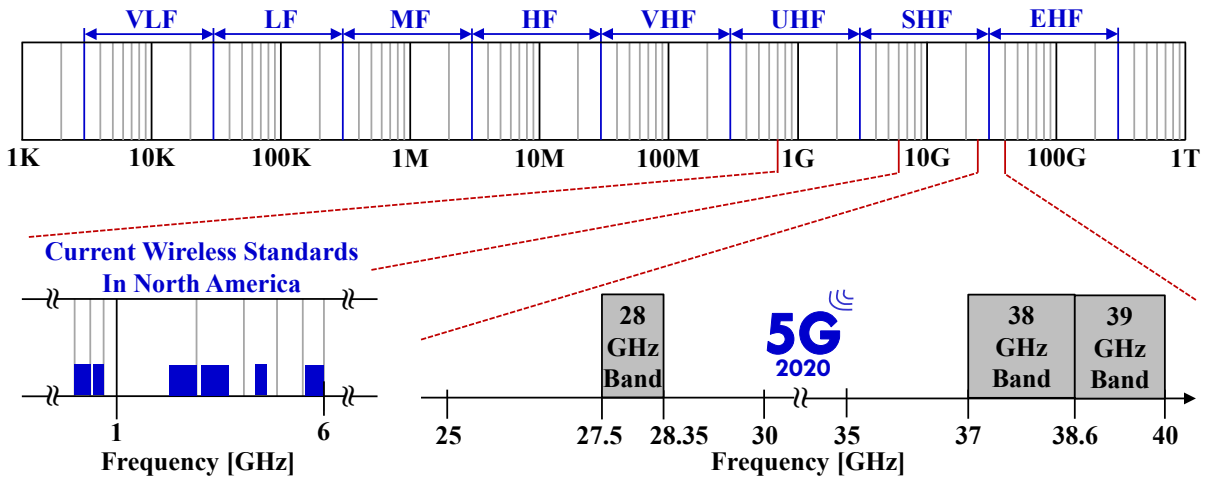


Fig. 1.2. The current wireless standards spectrum allocation in North America on the ITU radio bands scale and the spectrum allocated by the FCC for the upcoming 5G standard.

Table 1.1
Cellular Wireless Bands Spectrum Allocation in North America

	Bands/Standards	**Uplink [MHz]**	**Downlink [MHz]**	**Bandwidth [MHz]**
Wireless Mobile Bands and WiMAX (802.16)	700a	699-716	729-746	1.4MHz to 10MHz
	700b	704-716	734-746	5MHz and 10MHz
	700c	777-787	746-756	5MHz and 10MHz
	GSM – 850	824 – 850	870 – 894	1.4MHz to 10MHz
	PCS – 1900	1850 – 1910	1930 – 1990	1.4MHz to 20MHz
	AWS-1	1710-1755	2110-2155	1.4MHz to 20MHz
	2300 WCS	2305-2315	2350-2360	5MHz and 10MHz
	TD 2300	N/A	2300-2400	5MHz to 20MHz
	TD 2500	N/A	2496-2690	5MHz to 20MHz
	TD 2600	N/A	2570-2620	5MHz to 20MHz
	TD 3500	N/A	3400-3600	5MHz to 20MHz
	Unlicensed NII-1	N/A	5150-5250	20MHz
	Unlicensed NII-3	N/A	5725-5850	20MHz
Wi-Fi 802.11	802.11b/g/n	N/A	2400-2500	20MHz to 40MHz
	802.11a/n/ac	N/A	5150-5350	20MHz to 80MHz
			5470-5850	

2020. This motivated the use of the underutilized spectrum in the mm-Wave bands for the 5G standard [10],[11]. The idea of migrating to the mm-Wave band for higher data rates and bandwidths was applied to the Wi-Fi resulting in the so-called Wireless Gigabit (WiGig) referred to as the IEEE 802.11ad standard which supports data rates up to 7 Gbps in the unlicensed mm-Wave 60 GHz bands [12]. This was made possible owing to the advances in the semiconductor

technology which allowed building integrated circuits (IC) and Systems-on-Chip (SoC) that can operate efficiently at mm-Wave frequencies [13]. Following the same trend, the 5G is expected to take its place in the mm-Wave frequency range. Accordingly, the Federal Communications Commission (FCC) has recently allocated a total of 3.85 GHz bandwidth to be used by the 5G standard in the 28 GHz, 38 GHz and 39 GHz bands [14] as shown in Fig. 1.2. The most critical challenge in designing mm-Wave transceivers is trying to overcome the free space path loss due to the high frequency propagation. This will be discussed in the next section.

1.1.2 Path-Loss due to mm-Wave Frequency Propagation

The high-frequency mm-Wave propagation results in high path loss experienced by the transmitted signal in the communication channel. For more insight, the *Friis Transmission Formula* used to relate the received power *(P_R)* and transmitted power *(P_T)* in a communication link is considered [15], [16]. First, we need to see how the received power is related to the carrier frequency. The power received *(P_R)* by an antenna is the product of its effective aperture (A_{eR}) and the power density of the transmitted signal (S_T)

$$P_R = S_T \times A_{eR} \tag{1.1}$$

where S_T is a function of the gain of the transmit antenna (G_T), the distance between the transmitter and the receiver *(D)* and the transmitted power (P_R), while the effective aperture of the receiver antenna is a function of its gain *(G_R)* and the carrier frequency *(f_C)* as follows

$$S_T = \frac{G_T P_T}{4\pi D^2} \tag{1.2}$$

$$A_{eR} = \frac{G_R c^2}{4\pi f_C^2} \tag{1.3}$$

where *c* is the speed of light. By combining (1.1), (1.2), and (1.3) we get

$$P_R = P_T G_T G_R \frac{c^2}{(4\pi D f_C)^2} \tag{1.4}$$

which is the *Friis Transmission Formula*. For isotropic transmit and receive antennas where G_T=G_R=*1*, the received power can be written as

$$P_R = P_T \frac{c^2}{(4\pi D f_C)^2} = \frac{P_T}{L_S} \; ; \; L_S = \frac{(4\pi D f_C)^2}{c^2} \tag{1.5}$$

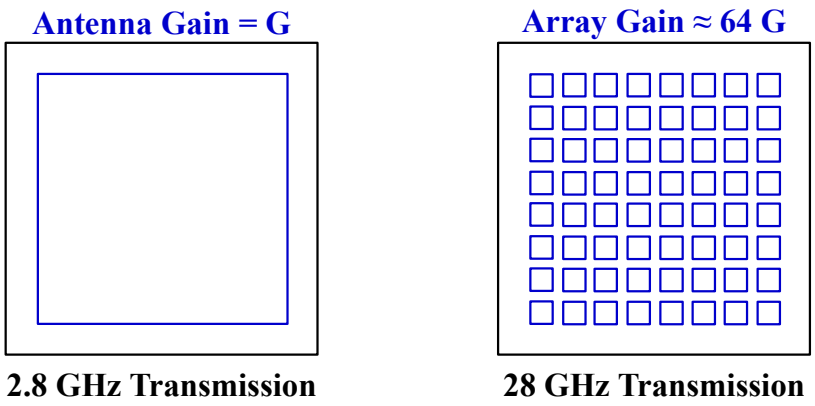


Fig. 1.3. Transmit/receive microstrip patch antennas located on the same aperture area. (a) Single patch antenna in case of 2.8 GHz Transmission. (b) A high gain patch array in case of 28 GHz Transmission.

where L_S is the free space path loss. For a given distance D and transmitted power P_T, the received power is inversely proportional to the square of the carrier frequency. Hence, compared to the current mobile standards operating below 6 GHz, the 5G expected to operate in the mm-Wave range will experience higher path loss (lower received power level) due to the high frequency propagation.

However, practically both transmit and receive antennas exhibit a significant amount of gain. Rewriting (1.4) by providing the antenna gain in terms of the effective aperture we get

$$P_R = P_T \frac{A_{eT} A_{eR} f_C^{\,2}}{(Dc)^2} \tag{1.6}$$

showing that the non-isotropic high gain transmit and receive antennas result in a direct relation between the received power and the square of the carrier frequency for a given aperture area. This is attributed to the smaller electrical length of antennas at higher frequencies where more antennas can be packed in the same area resulting in higher antenna array gain. Thus theoretically, a 10× increase in the carrier frequency results in 20 dB increase in the received power. This concept can be demonstrated by a simple example assuming two communications links one operating at 2.8 GHz and another at 28 GHz. For the 2.8 GHz case, a single square patch antenna with side length close to $0.5 \times \lambda_{2.8G}$ is used at the transmitter and the receiver where $\lambda_{2.8G}$ is the wavelength at 2.8 GHz. The area of the patch antenna is

$$A_{2.8\,GHz\,Patch} = (0.5 \times \lambda_{2.8G})^2 \tag{1.7}$$

On the other hand, for the 28 GHz transmission case, the single patch area is

$$A_{28\,GHz\,Patch} = (0.5 \times \lambda_{28\,GHz})^2 = \frac{A_{2.8\,GHz\,Patch}}{100} \tag{1.8}$$

where λ_{28G} is the wavelength at 28 GHz. Thus, more antennas can be packed in the same area for the 28 GHz transmission case compared to the 2.8 GHz case as illustrated in Fig. 1.3. And accordingly, assuming a given transmitted power P_T, a given distance D and 100% aperture efficiency, the ratio of the received power in the 28 GHz link case to that in the 2.8 GHz case can be written based on (1.4) as,

$$\frac{P_{R,28GHz}}{P_{R,2.8GHz}} = \frac{f_{C,2.8G}^2}{f_{C,28G}^2} \times \frac{G_{28G}^2}{G_{2.8G}^2} = \left(\frac{1}{10}\right)^2 \times \left(\frac{64}{1}\right)^2 = 40.96 \cong 16\,dB \tag{1.9}$$

which agrees with what was concluded from (1.6). This case study was conducted experimentally in [6] considering 3 GHz and 30 GHz communication links which showed 20 dB improvement in the received power for the 30 GHz transmission compared to the 3 GHz case. Thus, to overcome the path loss due to mm-Wave propagation, high gain antenna array together with adequate beamforming scheme should be adopted with high scanning capabilities to direct the high gain beam in the desired direction. The beamforming techniques will be discussed in the next section.

1.2 Beamforming for 5G Wireless Transceivers

Beamforming is a signal processing system built on top of an antenna array to steer its beam in the desired direction. From one perspective, beamforming can be viewed as spatial filtering [17]. Efficient beamforming is a necessity for enabling mm-Wave communication to alleviate the unfavorable path loss by providing the ability to steer a high gain antenna beam to the direction of the signal arrival for maximizing the signal-to-noise ratio (SNR). First, we will start by discussing the advantages of the directional-beam coverage for mm-Wave communications over the omnidirectional coverage used in the current wireless sub-6GHz mobile technologies.

1.2.1 Directional Beam versus Omni-directional Coverage

Considerable effort was exerted by the research community in modeling the path loss and conducting field measurements for mm-Wave propagation especially at 28 GHz and 38 GHz.

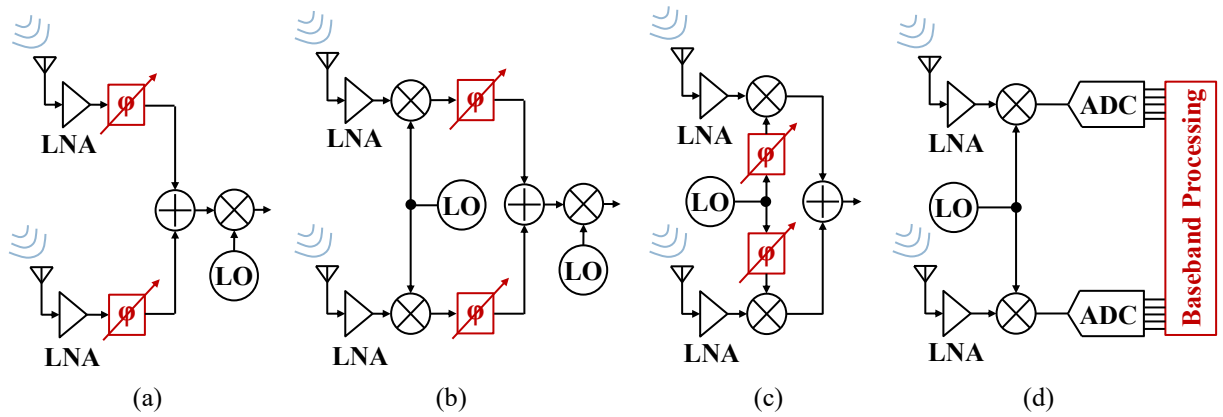


Fig. 1.4. Beamforming techniques. (a) RF Beamforming. (b) IF Beamforming. (c) LO Beamforming. (d) Digital beamforming.

This included in-door and out-door measurements for both line-of-sight (LoS) and non-line-of-sight (NLoS) scenarios while using omnidirectional and directional antennas [18]–[20]. Based on those studies and the nature of the short wavelength mm-Wave propagation, it was concluded that the omnidirectional antenna coverage that was deployed in previous mobile generations [21] are no longer a suitable candidate for the upcoming mm-Wave 5G mobile standard. This is due to the large path-loss in the mm-Wave range dictating the need for a high gain directional beam with high steering capabilities. Also owing to their narrow beamwidth, steerable directional antenna coverage will results in reduced co-channel and inter-cell interferences as compared to the omnidirectional antenna case [5]. Hence, a directional antenna array with high steering capabilities controlled by efficient beamforming scheme is a must for enabling mm-Wave communications. In the next section, the different types of beamforming architectures will be discussed.

1.2.2 Beamforming Techniques

Beamforming is performed by applying different weighting factors and phase shifts to each RF channel for beam steering and achieving optimal signal-to-noise ratio (SNR). The phase shifting operation can be performed at different locations of the receiver/transmitter channel resulting in the different categories of beamforming [22]–[24] as illustrated in Fig. 1.4, namely; Radio-Frequency (RF), Intermediate-Frequency (IF), Local-Oscillator (LO) and Digital beamforming.

In RF beamforming, the phase shifting operation is performed on the RF signal before down conversion as illustrated in Fig. 1.4(a). The spatial filtering action of the beamforming is performed on the received RF signal before the mixing operation. This relaxes the requirements

on the mixer design and reduces the risk of I/Q imbalance. However, the phase shifter is required to operate at higher frequencies complicating its design and making it more challenging, power consuming, in addition to the difficulty to attain high resolution which limits the achieved performance.

In the IF beamforming, shown in Fig. 1.4(b), the phase shifting is performed in the baseband (IF domain) after down conversion. This scheme is also referred to as baseband beamforming. The fact that the phase shifting is performed at lower IF frequency relaxes the design requirements of the phase shifter and hence fine resolution can be attained with lower power consumption. However, since the phase shifting is performed after the mixer, mixer design becomes critical where I/Q mismatch is a major concern and can result in SNR degradation. Also, additional mixers are required resulting in higher area and power penalty.

It can be noted that in RF and IF beamforming schemes the phase shifting operation is performed in the signal path which is lossy resulting in degrading the SNR. The LO beamforming can alleviate this issue and provide enhanced SNR by performing the phase shifting in the LO clock path rather than the signal path as illustrated in Fig. 1.4(c). Performing the phase shift on the LO clock makes the transceiver's SNR insensitive to the phase shifter losses, non-linearity, and noise.

The RF, IF and LO beamforming schemes are considered analog beamforming techniques. On the other hand, digital beamforming performs the phase shifting in the digital domain as shown in Fig. 1.4(d). The RF signal is first down converted then digitized using an analog-to-digital converter (ADC) whose digital output is passed to a digital baseband processing block where the beamforming operation is performed. Compared to analog beamforming schemes, digital beamforming provides higher flexibility which is necessary for massive MIMO. However, each RF channel requires a high-speed, high-resolution analog-to-digital converter (ADC) which is challenging to implement and will increase the overall power consumption especially in the case of large arrays.

For mm-Wave 5G wireless transceivers, large antenna arrays are required to provide the high beamforming gains necessary to compensate for the high path loss experienced by the signal. Hence digital beamforming would be complex and expensive to implement since an ADC will be required for each antenna array element. On the other hand, the analog beamforming which is simpler to implement would not provide the required flexibility for the massive MIMO.

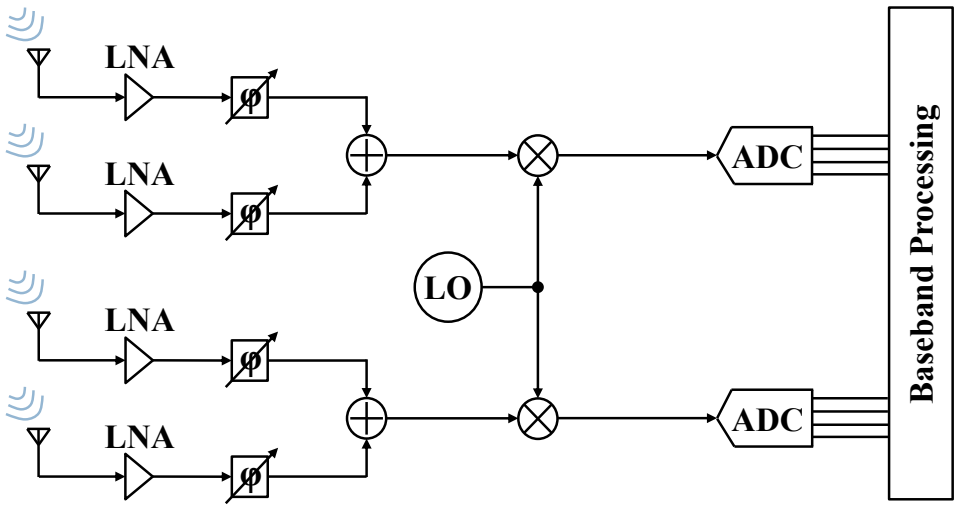


Fig. 1.5. RF-Digital Hybrid Beamforming technique for mmWave communications.

This trade-off paved the way for the hybrid beamforming architecture which combines analog and digital beamforming together. In [25],[26] the RF beamforming was combined with digital beamforming as illustrated in Fig. 1.5 where each RF channel is connected to an RF beamformer and then every N-channels are combined, down-converted and applied to an ADC for digital beamforming. The hybrid architecture combines the advantages of both the analog and digital beamforming schemes, that is, less number of ADCs is used while still providing the required flexibility for massive MIMO.

1.2.3 Discussion on Beamforming Schemes

In this section, the beamforming schemes will be further discussed. First, the digital beamforming will be considered.

1.2.3.1 Digital Beamforming

The digital beamforming was first proposed for radar applications by P. Barton in 1980 [27]. Since then, digital beamforming started to gain more interest from the research community. The main advantage of the digital beamforming over its analog counterparts is its higher degree of flexibility in forming and controlling the radiation pattern [28]. This is accomplished by its ability to provide improved adaptive pattern nulling, lower side lobe levels, pattern correction and enhanced scanning resolution [29]. However, the performance of the digital beamformers is limited by the analog-to-digital conversion process [30]. More specifically, the non-linearity, quantization noise and the high power of the ADC [31]. Higher ADC resolution is required for

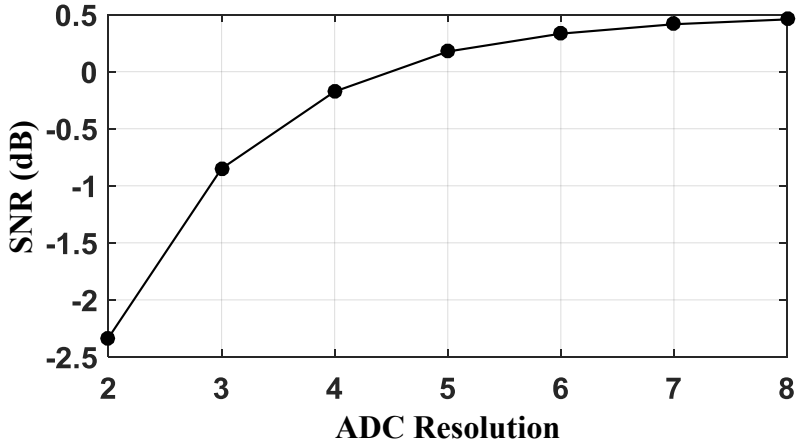


Fig. 1.6. The output SNR of the digital beamforming versus ADC resolution.

lower quantization noise level and improved SNR which comes at the cost of higher complexity and power consumption. Also, the ADC non-linearity will be translated to harmonics in the output spectrum resulting in performance degradation. To get rid of the non-linearity, ADC calibration is required which adds to the complexity and power of the ADC. The case becomes even more severe when high resolution is required over wide operating bandwidth. Fig. 1.6 provides the simulated output SNR versus the ADC resolution for a 1×2 digital beamforming scheme taking into account the channel noise and the quantization noise of the ADC showing that higher ADC resolution is required for enhanced SNR.

The future mm-Wave 5G transceivers are expected to feature large antenna arrays while operating over a wide bandwidth. This makes digital beamforming a costly option for the following reasons; (1) large number of ADCs will be required (one for each RF channel); (2) For high bandwidth operation, the high resolution ADC will need to operate at high sampling rate resulting in increased complexity and power; (3) In addition to that, the digital processing block will be more complicated as it is required to manage and process the high data rates produced by the ADC. For example, assume that the ADC within the digital beamformer is required to operate over 500 MHz bandwidth. Then this requires a Nyquist rate ADC operating with at least 1 GS/s sampling rate. Given that the ADC is capable of delivering 10-bits resolution, then the data rate output of the ADC is 10 Gb/s. That is, the digital processing block is required to support such high data rate.

Hence, to overcome these limitations and still benefit from the advantages of the digital beamforming, digital beamforming can be combined with analog beamforming forming a hybrid

beamforming structure. In the next section, the three analog beamforming architectures (RF, IF and LO) will be discussed and analyzed using simplified models. Based on this discussion the analog beamforming scheme to be combined with the digital beamforming to form the hybrid architecture will be chosen.

1.2.3.2 Analog Beamforming

Most mobile communication services operate in urban areas where there is no direct line-of-sight between the transmitter (TX) and the receiver (RX). The transmitted signal experiences three basic propagation mechanisms due to the presence of buildings and obstacles between the transmitter and the receiver, namely, reflection, diffraction, and scattering. This forces the signal to travel along different paths of varying lengths commonly referred to as multipath propagation. The signals from different paths arrive at the receiver at slightly different times and combine giving the resultant signal. Multipath propagation results in fading [32] which is the main cause of latency and SNR degradation. Employing antenna arrays at the TX and RX results in antenna diversity (each element of the array represents an RF channel) where by combining the signals received by the different RF channels, the link SNR can be improved. Maximal Ratio Combining (MRC) is one of the most effective diversity combining techniques [33],[34] for maximizing the SNR where the signal at each RF channel is multiplied by a weighting factor proportional to the signal strength at that channel.

To compare the performance of the analog beamforming schemes, simplified models were created for each of them with the main noise sources taken into account assuming a communication link with one TX and two RXs. The MRC combining algorithm was applied to each of the beamforming techniques for optimal SNR. From that comparison, it would be clear which of the RF, LO and IF beamforming schemes is the best choice to be combined with digital beamforming for creating the hybrid beamforming architecture.

RF Beamforming

The RF beamforming noise model for the 1×2 communication link is illustrated in Fig. 1.7 where the channel noise, the phase shifter noise, and the local oscillator phase noise are considered together with the correlation coefficient between the noise sources of channel 1 and channel 2 of the receiver. The following variables are adopted; w_C is the carrier frequency, w_O is the local oscillator frequency, $\alpha_{1,2}$ are the attenuation coefficient for channels 1 and 2, $n_{ch1,2}$ are the

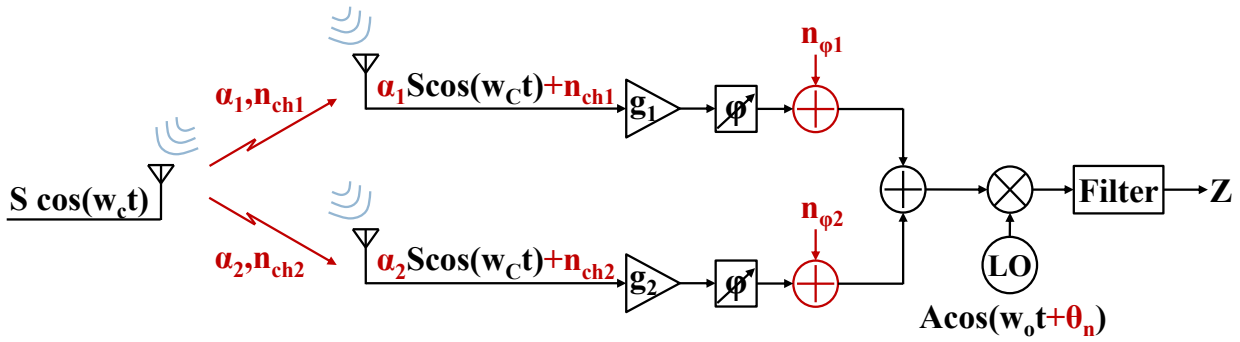


Fig. 1.7. Simplified RF Beamforming Noise Model.

additive white Gaussian noise added by channels 1 and 2, $n_{\varphi 1,2}$ are the noise added by the phase shifters in channels 1 and 2, θ_n represents the phase noise of the local oscillator clock and $g_{1,2}$ are the weighting factors of the MRC combining algorithm for channels 1 and 2. To compute the SNR we first write expressions for the signal and noise power at the receiver output (node Z) based on the model provided in Fig. 1.7. The signal component at Z can be written as

$$Z_{Sig} = (\alpha_1 g_1 S + \alpha_2 g_2 S)\, cos(w_C t) \times A cos(w_o t + \theta_n) \tag{1.10}$$

Since θ_n is small, we can write $cos(w_O t+\theta_n)=cos(w_O t)-\theta_n\, sin(w_O t)$. Hence, the signal component Z_{Sig} can be written as

$$Z_{Sig} = AS(\alpha_1 g_1 + \alpha_2 g_2)\, cos(w_C t)\, cos(w_o t) = \frac{AS(\alpha_1 g_1 + \alpha_2 g_2)}{2} cos\big((w_C - w_o)t\big) \tag{1.11}$$

where it is assumed that the filter ideally rejects the high frequency component. The signal power P_{Sig} is computed as the expected value of the square of the Z_{Sig}.

$$P_{Sig} = E\big[{Z_{Sig}}^2\big] = \frac{1}{T}\int {Z_{Sig}}^2 dt = \frac{A^2 S^2}{8}\,(\alpha_1 g_1 + \alpha_2 g_2)^2 \tag{1.12}$$

Similarly, the noise component Z_N can be written as

$$\begin{aligned} Z_N = A cos(w_o t)\big(n_{ch1} g_1 + n_{ch2} g_2 + n_{\varphi 1} + n_{\varphi 2}\big) + \frac{AS(\alpha_1 g_1 + \alpha_2 g_2)}{2}\theta_n \sin\big((w_C - w_o)t\big) \\ - A\theta_n sin(w_o t) \times \big(n_{ch1} g_1 + n_{ch2} g_2 + n_{\varphi 1} + n_{\varphi 2}\big) \end{aligned} \tag{1.13}$$

The noise power is derived as the expected value of the square of the Z_N which yields

$$P_N = \frac{A^2}{2} \times \left(g_1^2\sigma_{nch1}^2 + g_2^2\sigma_{nch2}^2 + 2g_1g_2\sigma_{nch1}\sigma_{nch2}\rho_{nch} + \sigma_{n\varphi1}^2 + \sigma_{n\varphi2}^2 + 2\sigma_{n\varphi1}\sigma_{n\varphi2}\rho_{n\varphi}\right) \times (1 + \sigma_{\theta n}^2) + \frac{A^2S^2}{8}\,(\alpha_1 g_1 + \alpha_2 g_2)^2\sigma_{\theta n}^2 \tag{1.14}$$

where $\sigma_{nch1,2}$ is the standard deviation of the channel noise, $\sigma_{\theta n}$ is the standard deviation of the LO clock phase noise, ρ_{nch} is the correlation coefficient between n_{ch1} and n_{ch2} and $\rho_{\varphi n}$ is the correlation coefficient between $n_{\varphi 1}$ and $n_{\varphi 2}$. By dividing (1.12) by (1.14) we get an expression for the SNR for the RF beamforming model shown in Fig. 1.7.

$$SNR = \frac{S^2\,(\alpha_1 g_1 + \alpha_2 g_2)^2}{4\left[1 + \sigma_{\theta n}^2\right]\left[g_1^2\sigma_{nch1}^2 + g_2^2\sigma_{nch2}^2 + 2g_1g_2\sigma_{nch1}\sigma_{nch2}\rho_{nch} + \sigma_{n\varphi1}^2 + \sigma_{n\varphi2}^2 + 2\sigma_{n\varphi1}\sigma_{n\varphi2}\rho_{n\varphi}\right] + S^2\,(\alpha_1 g_1 + \alpha_2 g_2)^2\sigma_{\theta n}^2} \tag{1.15}$$

From which we can conclude that as the correlation coefficient between the two channels decreases, the SNR increases. This can also be concluded intuitively since uncorrelated channels result in higher diversity and hence higher SNR.

For optimal SNR, the weighting factors g_1 and g_2 should be properly chosen. However, a power constraint should be taken into account where the sum of gains applied to both channels should not exceed a maximum value G_{max}, that is $g_1+g_2=G_{max}$. Now, to get an expression for g_1 for maximal SNR, substitute the G_{max} condition into (1.15) and differentiate the resultant equation with respect to g_1 then equate to zero

$$\frac{\partial}{\partial g_1}(SNR)\Big|_{\;g2=Gmax-g1} = 0 \tag{1.16}$$

This yields,

$$g_1 = \frac{(\alpha_1 - \alpha_2)\left(\sigma_{n\varphi1}^2 + \sigma_{n\varphi2}^2 + 2\sigma_{n\varphi1}\sigma_{n\varphi2}\rho_{n\varphi}\right) + G_{max}^2(\alpha_1\sigma_{nch2}^2 - \alpha_2\sigma_{nch1}\sigma_{nch2}\rho_{nch})}{G_{max}(\alpha_1\sigma_{nch2}^2 + \alpha_2\sigma_{nch1}^2 - (\alpha_1 + \alpha_2)\sigma_{nch1}\sigma_{nch2}\rho_{nch})} \tag{1.17}$$

For more insight, a simplified version of equation (1.17) can be obtained by neglecting the local oscillator and phase shifter noise and only considering the channel noise and assuming that n_{ch1} and n_{ch2} are totally uncorrelated $\rho_{nch}=0$,

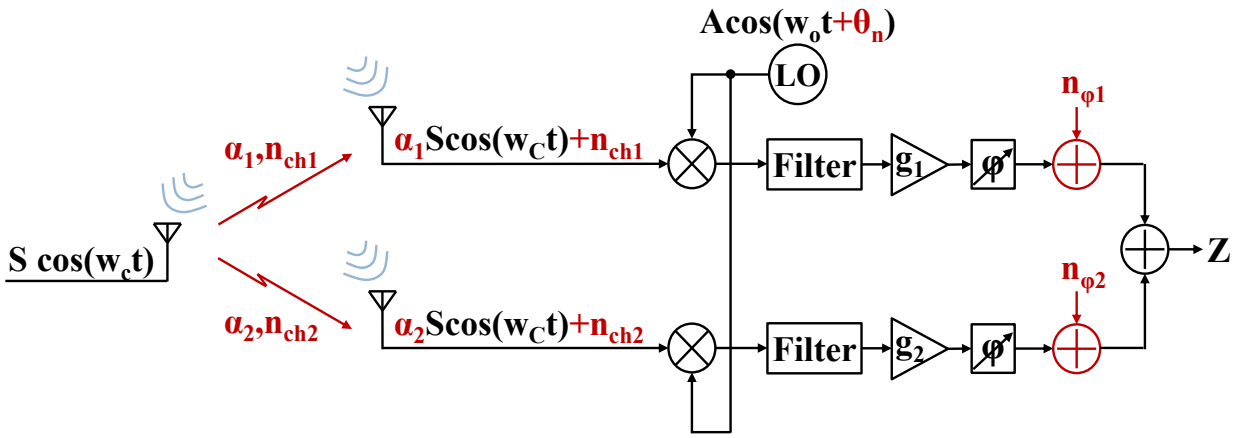


Fig. 1.8. Simplified IF Beamforming Noise Model.

$$g_1 = G_{max} \times {\alpha_1\sigma_{nch2}^2}\Big/{\alpha_1\sigma_{nch2}^2 + \alpha_2\sigma_{nch1}^2} \tag{1.18}$$

$$g_2 = G_{max} \times {\alpha_2\sigma_{nch1}^2}\Big/{\alpha_1\sigma_{nch2}^2 + \alpha_2\sigma_{nch1}^2} \tag{1.19}$$

$$\frac{g_1}{g_2} = \frac{\left({\alpha_1}/{\sigma_{nch1}^2}\right)}{\left({\alpha_2}/{\sigma_{nch2}^2}\right)} \tag{1.20}$$

The above equations provide expressions of the weighting factors for channel 1 (g_1) and channel 2 (g_2) for optimal SNR where it can be concluded that the weighting factor assigned to each channel is proportional to its individual SNR which agrees with the MRC concept where higher weighting factor is given to the channel with higher SNR.

IF Beamforming

The noise model for the IF beamforming is shown in Fig. 1.8. Similar to the RF beamforming, the IF beamforming noise model was analyzed and the signal component at Z and the signal power were extracted as

$$Z_{Sig} = {AS}/{2}\ (\alpha_1 g_1 + \alpha_2 g_2)\cos(w_c - w_o)t \tag{1.21}$$

$$P_{Sig} = \frac{A^2S^2}{8}\ (\alpha_1 g_1 + \alpha_2 g_2)^2 \tag{1.22}$$

which is similar to that of the RF beamforming. The noise component at Z can be found as

$$Z_N = \left(A\cos w_o t\,(n_{ch1}g_1 + n_{ch2}g_2) + n_{\varphi 1} + n_{\varphi 2}\right) + \frac{AS}{2}\theta_n \sin(w_c - w_o)\,t(\alpha_1 g_1 + \alpha_2 g_2) - A\theta_n \sin w_o t\,(n_{ch1}g_1 + n_{ch2}g_2) \tag{1.23}$$

And consequently, the noise power can be computed as

$$P_N = \frac{A^2}{2}(1+\sigma_{\theta n}^2)(g_1^2\sigma_{nch1}^2 + g_2^2\sigma_{nch2}^2 + 2g_1g_2\sigma_{nch1}\sigma_{nch2}\rho_{nch}) + \frac{A^2S^2}{8}\sigma_{\theta n}^2(\propto_1 g_1 + \alpha_2 g_2)^2 + (\sigma_{n\varphi 1}^2 + \sigma_{n\varphi 2}^2 + 2\sigma_{n\varphi 1}\sigma_{n\varphi 2}\rho_{n\varphi}) \tag{1.24}$$

where ρ_φ is the correlation coefficient between $n_{\varphi 1}$ and $n_{\varphi 2}$. The SNR can be computed by dividing P_{Sig} by P_N

$$SNR = \frac{A^2S^2\,(\alpha_1 g_1 + \alpha_2 g_2)^2}{4A^2(1+\sigma_{\theta n}^2)(g_1^2\sigma_{nch1}^2 + g_2^2\sigma_{nch2}^2 + 2g_1g_2\sigma_{nch1}\sigma_{nch2}\rho_{nch}) + A^2S^2\sigma_{\theta n}^2(\propto_1 g_1 + \alpha_2 g_2)^2 + 8(\sigma_{n\varphi 1}^2 + \sigma_{n\varphi 2}^2 + 2\sigma_{n\varphi 1}\sigma_{n\varphi 2}\rho_{n\varphi})} \tag{1.25}$$

To get the expression for g_1 for maximal SNR, apply the G_{max} condition and take the derivative of (1.25)

$$g_1 = \frac{2(\alpha_1 - \alpha_2)\left(\sigma_{n\varphi 1}^2 + \sigma_{n\varphi 2}^2 + 2\sigma_{n\varphi 1}\sigma_{n\varphi 2}\rho_{n\varphi}\right) + A^2G_{max}^2(\alpha_1\sigma_{nch2}^2 - \alpha_2\sigma_{nch1}\sigma_{nch2}\rho_{nch})(1+\sigma_{\theta n}^2)}{A^2G_{max}(1+\sigma_{\theta n}^2)(\alpha_1\sigma_{nch2}^2 + \alpha_2\sigma_{nch1}^2 - (\alpha_1+\alpha_2)\sigma_{nch1}\sigma_{nch2}\rho_{nch})} \tag{1.26}$$

LO Beamforming

Similarly, a noise model was constructed for the LO beamforming as illustrated in Fig. 1.9. The phase shifter noise is excluded since in LO beamforming the receiver performance is insensitive to the phase shifter noise as phase shifting is not performed in the signal path. A similar analysis was performed for the LO beamforming. For getting an expression for the SNR, first, extract the signal component at node *Z* and compute the signal power

$$Z_{Sig} = {}^{AS}/_{2}\;(\alpha_1 g_1 + \alpha_2 g_2)\cos(w_c - w_o)t \tag{1.27}$$

$$P_{Sig} = \frac{A^2S^2}{8}\,(\alpha_1 g_1 + \alpha_2 g_2)^2 \tag{1.28}$$

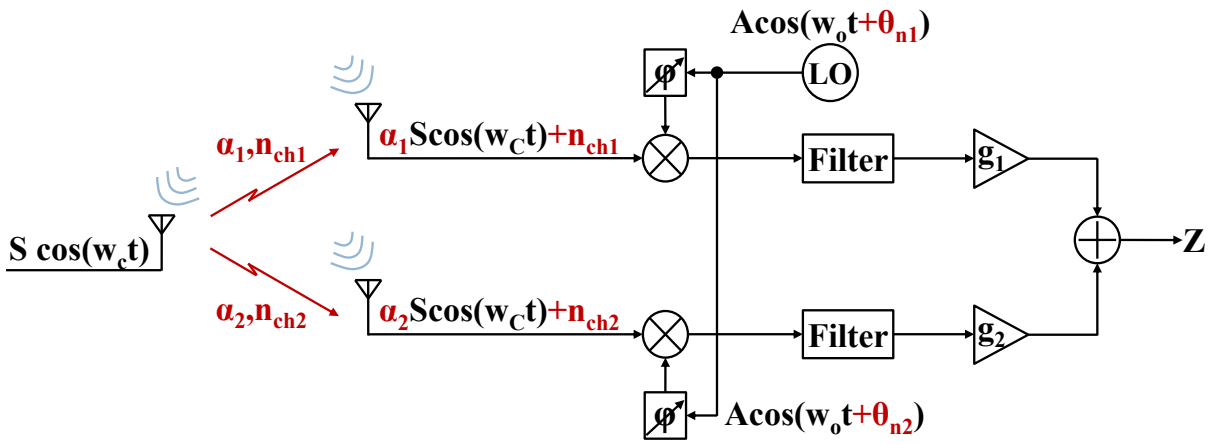


Fig. 1.9. Simplified LO Beamforming Noise Model.

where it can be concluded that the signal power for LO, IF and RF beamforming is the same. The noise component Z_N can be found as

$$Z_N = A\cos w_o t\,(n_{ch1}g_1 + n_{ch2}g_2) + \frac{AS}{2}\sin(w_c - w_o)\,t(\alpha_1 g_1\theta_{n1} + \alpha_2 g_2\theta_{n2}) - A\sin w_o t\,(n_{ch1}g_1\theta_{n1} + n_{ch2}g_2\theta_{n2}) \tag{1.29}$$

The noise power is computed as the expected value of the square of Z_N

$$P_N = \frac{A^2}{2}\left[g_1^2\sigma_{nch1}^2(1+\sigma_{\theta n1}^2) + g_2^2\sigma_{nch2}^2(1+\sigma_{\theta n2}^2) + 2g_1g_2\sigma_{nch1}\sigma_{nch2}\rho_{nch}(1+\sigma_{\theta n1}\sigma_{\theta n2}\rho_\theta)\right] + \frac{A^2S^2}{8}\left[\alpha_1^2g_1^2\sigma_{\theta n1}^2 + \alpha_2^2g_2^2\sigma_{\theta n2}^2 + 2\alpha_1g_1\alpha_2g_2\sigma_{\theta n1}\sigma_{\theta n2}\rho_\theta\right] \tag{1.30}$$

where ρ_θ is the correlation coefficient between θ_{n1} and θ_{n2}. The SNR can be found as P_{Sig}/P_N

$$SNR = \frac{S^2\,(\alpha_1g_1 + \alpha_2g_2)^2}{4\left[g_1^2\sigma_{nch1}^2(1+\sigma_{\theta n1}^2) + g_2^2\sigma_{nch2}^2(1+\sigma_{\theta n2}^2) + 2g_1g_2\sigma_{nch1}\sigma_{nch2}\rho_{nch}(1+\sigma_{\theta n1}\sigma_{\theta n2}\rho_\theta)\right] + S^2\left[\alpha_1^2g_1^2\sigma_{\theta n1}^2 + \alpha_2^2g_2^2\sigma_{\theta n2}^2 + 2\alpha_1g_1\alpha_2g_2\sigma_{\theta n1}\sigma_{\theta n2}\rho_\theta\right]} \tag{1.31}$$

Then apply the G_{max} condition and take the derivative of (1.31) to get an expression for g_1 for maximal SNR

$$g_1 = \frac{G_{max}[4\sigma_{nch2}^2\alpha_1(1+\sigma_{\theta n2}^2) + \alpha_1\alpha_2^2S^2(\sigma_{\theta n2}^2 - \sigma_{\theta n1}\sigma_{\theta n1}\rho_{\theta n}) - 4\sigma_{nch1}\sigma_{nch2}\rho_{nch}\alpha_2(1+\sigma_{\theta n1}\sigma_{\theta n1}\rho_{\theta n})]}{4\left[\sigma_{nch1}^2\alpha_2(1+\sigma_{\theta n2}^2) + \sigma_{nch2}^2\alpha_1(1+\sigma_{\theta n1}^2) - \sigma_{nch1}\sigma_{nch2}\rho_{nch}(\alpha_1+\alpha_2)(1+\sigma_{\theta n1}\sigma_{\theta n1}\rho_{\theta n})\right] + S^2[\alpha_1^2\alpha_2\sigma_{\theta n1}^2 + \alpha_2^2\alpha_1\sigma_{\theta n2}^2 - \sigma_{\theta n1}\sigma_{\theta n1}\rho_{\theta n}(\alpha_1^2\alpha_2 + \alpha_2^2\alpha_1)]} \tag{1.32}$$

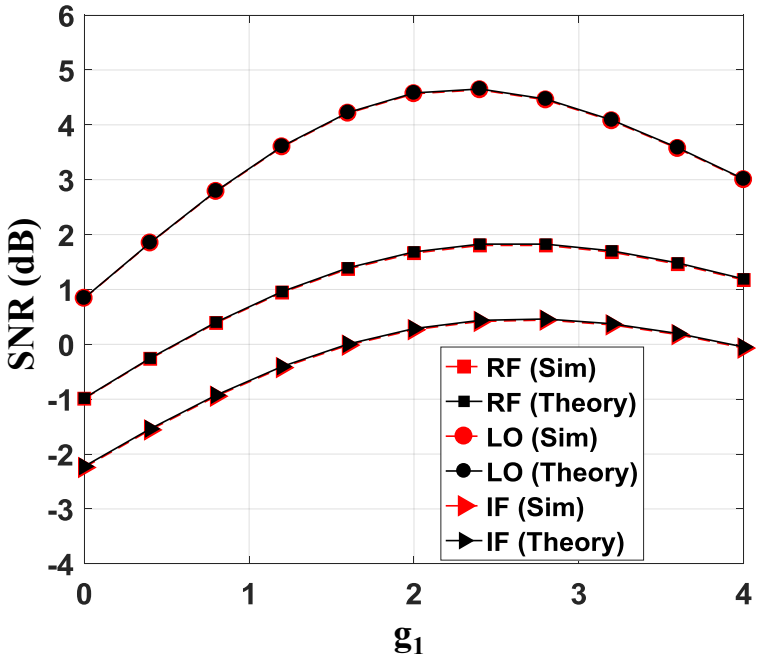


Fig. 1.10. SNR versus g_1 plot using the theoretical derivations and MATLAB models for the RF, IF and LO beamforming.

Comparing RF, IF and LO Beamforming Schemes

To validate the obtained expressions, MATLAB models were constructed for the RF, IF and LO beamforming techniques. Both the theoretical derivations and MATLAB models were evaluated with $G_{max}=4$, $\alpha_1=0.9$, $\alpha_2=0.7$. Fig. 1.10 shows the SNR versus g_1 plot where for the theoretical evaluation equations (1.15) and (1.17) were used for the RF beamforming, equations (1.25) and (1.26) for the IF beamforming and equations (1.31) and (1.32) for the LO beamforming. Since $\alpha_1 > \alpha_2$, the peak SNR is attained when the weighting factors are adjusted such that $g_1>g_2$, that is the channel with higher signal strength (in this case channel 1) is assigned higher weighting factor which agrees with the MRC combining methodology. From the obtained results it can be concluded that the theoretical derivations and MATLAB models are in close agreement where the LO beamforming is providing higher SNR as compared to the RF and IF beamforming architectures.

It worth to be noted that the analysis performed for the analog beamforming schemes is based on very simplified models. Thus to validate the obtained results, a performance comparison of state-of-the-art [35]–[43] analog beamformers is provided in Table 1.2. From which it can be concluded that the LO beamforming achieves lower noise figure (NF) per channel compared to RF/IF beamforming. In addition, using LO beamforming allows embedding

Table 1.2
State-of-the-art Analog beamformers

Architecture	Reference	Process	Number of Channels	Frequency (GHz)	Area (mm^2)	Power (mW)	NF/Channel (dB)
RF	[35]	0.13 µm CMOS	4	24	2.11×1.43	115	8
	[36]	0.13 µm CMOS	4	25	1.1×1.3	30	9.3
	[37]	0.13 µm SiGe BiCMOS	4	34	2×2.02	142	9
	[38]	90 nm CMOS	4	56	1.6×1	52	8.7
IF	[39]	90 nm CMOS	32	60	14.5	507	11
LO	[40]	0.18 µm CMOS	8	24	3.5×3.3	910	7.1
	[41]	0.18 µm CMOS	1	24	2.06×2.04	108	6
	[42]	0.13 µm CMOS	4	24	2.35×2.13	520	7.9
	[43]	90 nm CMOS	2	52	1.4×1	65	7.1

the phase shifter within the LO which adds to the advantages of the LO beamforming scheme. Hence, the LO beamformer is combined with the digital beamforming to construct the hybrid beamforming scheme. The block diagram of the LO-Hybrid beamforming is shown in Fig. 1.11.

1.3 Thesis Scope and Outline

This work proposes solutions and designs for three of the main building blocks for the 5G transceiver on the handset device side. As illustrated in Fig. 1.11 the blocks that are targeted by this thesis are highlighted. This includes the fractional-N frequency synthesizer, the ADC supporting both oversampling and Nyquist rate modes, and the antenna array. The dissertation is organized as follows.

First, the fractional-N frequency synthesizer is discussed in Chapter 2 and Chapter 3. In the beginning, a quick overview of frequency generation techniques and charge pump phase-locked loops (CPPLL) is presented. Two fractional-N synthesizer prototypes were designed and fabricated in the TSMC 65 nm CMOS process. The first is a single stage quadrature 28 GHz CPPLL employing a phase interpolator for the fractional division. The second prototype is a 28 GHz cascaded PLL utilizing a first stage 7 GHz fractional-N CPPLL followed by a second stage quadrature divider-less subsampling PLL (SSPLL). The phase noise analysis and design of both single stage and cascaded PLL prototypes are introduced with detailed implementation of the fractional divider, high frequency phase detector, etc. Based on this analysis, the limitations of the single-stage architecture are pointed out and the performance improvements of the cascaded phase locked loop (PLL) over single stage PLL in terms of jitter and power consumption are

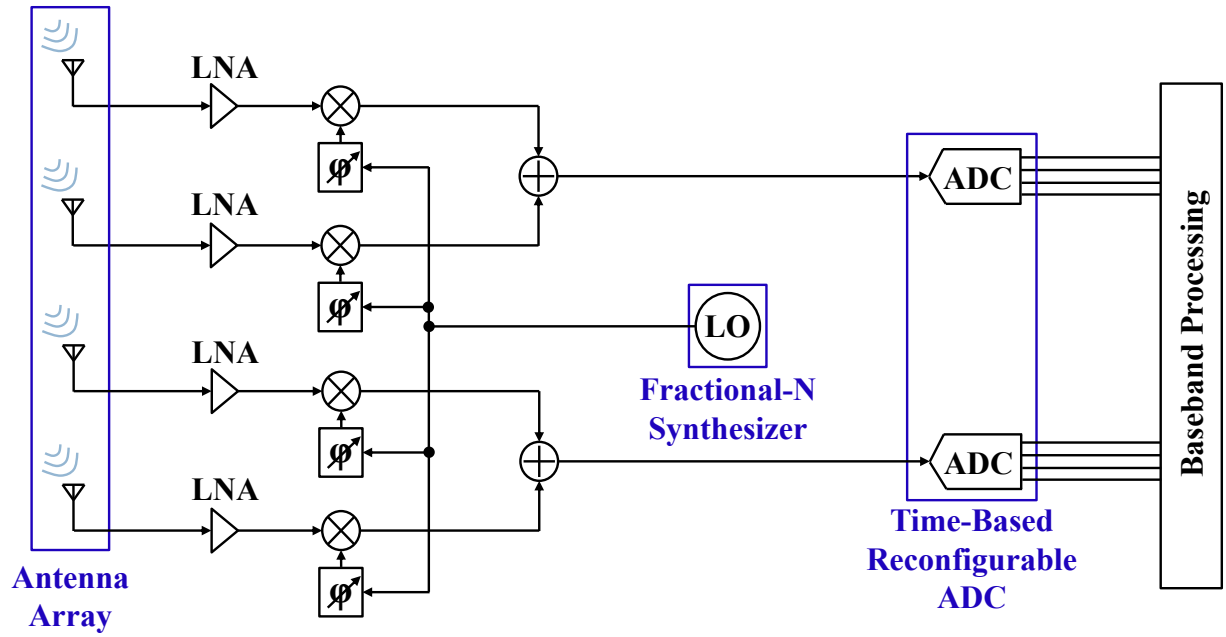


Fig. 1.11. The LO-Hybrid Beamforming for 5G wireless transceiver with the blocks targeted in the thesis marked by blue boxes

highlighted. Also, the cascaded PLL design perspectives and jitter optimization are introduced. Finally, the measured results of both the single-stage and cascaded fractional-N PLLs and comparison with the state-of-the-art synthesizers are provided.

Second, the analog-to-digital converter design is introduced in Chapter 4. In the beginning, an introduction to time-based ADCs and time-to-digital converters (TDC) is provided. Two time-based ADC prototypes are proposed and fabricated in the TSMC 65 nm CMOS process. The first is an oversampling time-based ADC. It employs a high-resolution successive approximation register (SAR) time-to-digital converter (TDC) with time-domain correlated double sampling for improved quantization noise level. For enhanced linearity, a 1-bit folded voltage-controlled oscillator (VCO) is utilized. The design and operation of the SAR-TDC and folded VCO are presented. Also, the measured results of both the SAR-TDC and the overall ADC together with a comparison with the state-of-the-art TDCs and time-based oversampling ADCs are provided. The second prototype is a reconfigurable Nyquist-rate time-based ADC. The time-domain nature of the ADC allows for efficient hardware reuse and a wide range of reconfigurability employing a reconfigurable SAR/Flash TDC. The theory, implementation details and measurement results of the reconfigurable ADC are presented.

Third, the antenna design is presented in Chapter 5 where a mm-Wave substrate-integrated vertically polarized dipole antenna is proposed to fit at the mobile devices edge. The chapter begins with a literature review on reported 5G antennas and the requirements for the 5G antennas on the cellular device side are pointed out. Following, the proposed electric dipole structure, design procedure together with the parametric study for its different design parameters are introduced. The dipole employs a novel substrate-integrated waveguide (SIW) to parallel-strip line (PS) transition. The feed and array structure together with the parametric study of the SIW-to-PS transition are provided. The dipole array was designed and fabricated on Rogers RO5880 substrate. The simulated and measured results of the fabricated prototypes are reported and compared with the state-of-the-art mm-Wave linearly polarized antenna.

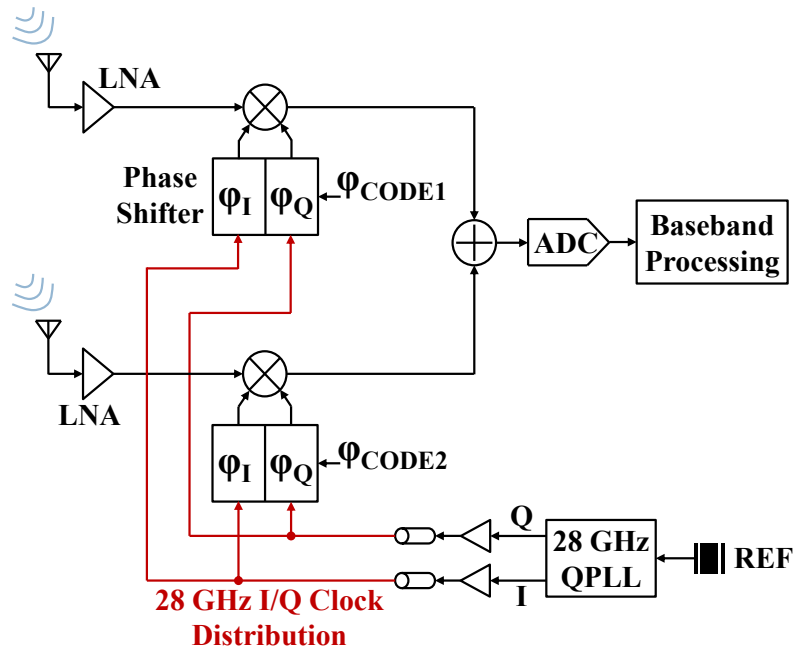
Finally, Chapter 6 concludes the thesis and highlights the dissertation contribution. Also, possible future work based on what is presented in this dissertation is introduced.

2. THE SINGLE STAGE FRACTIONAL-N FREQUENCY SYNTHESIZER

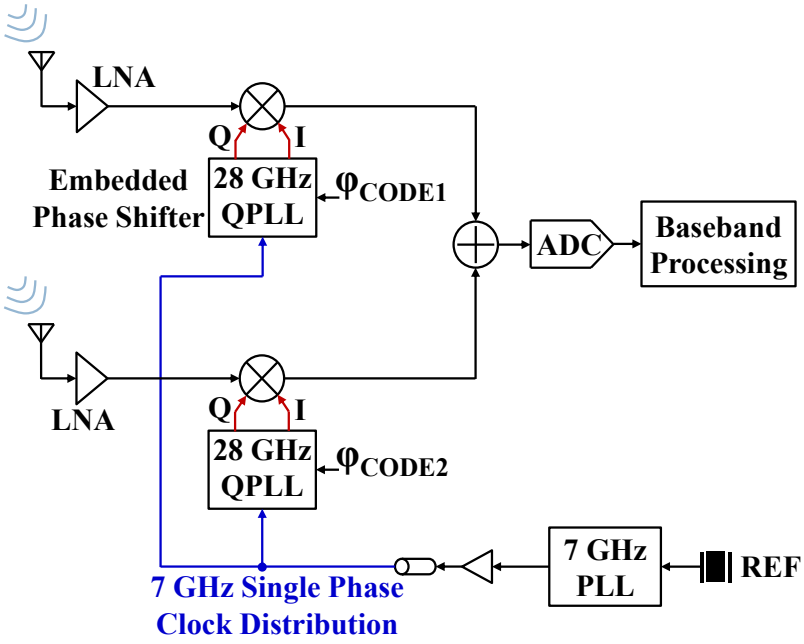
In RF receivers a local oscillator (LO) is required to down-convert the received RF signal to the baseband domain. Several challenges are involved in the LO design for 5G transceivers where it should provide clean, low jitter clock in the mm-Wave frequency range while consuming low power. In addition, the fine frequency resolution required by wireless transceivers dictates the need for fractional-N synthesis without sacrificing the jitter performance of the output clock. Phase-locked loops (PLLs) can efficiently perform the frequency synthesis. In this chapter, a quadrature mm-Wave single-stage fractional-N charge-pump PLL is presented where the fractional division is performed using a high-resolution phase mixer. The PLL is designed and fabricated in the 65 nm CMOS process. First, the LO clock distribution for mm-Wave wireless transceivers will be briefly discussed.

2.1 Clock Distribution for mm-Wave Wireless Transceivers

Millimeter-Wave frequency propagation suffers from high path loss and to overcome that, handset receivers could employ beamforming architectures by implementing four to eight parallel receiver paths. In such architectures, each of these paths requires high-quality low jitter clock to up/down convert the signal to/from each antenna. Since per receiver path LC PLL is expensive, a central shared PLL is often preferred [44]. In scenarios where a single stage quadrature PLL (QPLL) is used as the local oscillator (LO), mm-Wave I/Q clocks are distributed to each receiver path that can be several millimeters apart as shown in Fig. 2.1(a). In addition to the high power consumption encountered in this approach due to high frequency clock distribution, I/Q imbalance limits the phase resolution. Alternatively, using a cascaded PLL can alleviate this issue where the PLL is broken into two stages. As shown in Fig. 2.1(b), the output of the first stage 7 GHz PLL will be distributed to different RF channels then locally in each channel the quadrature mm-Wave (28 GHz) clock will be generated via the second stage PLL. Hence in the cascaded PLL approach, relatively lower frequency 7 GHz single phase clock is distributed resulting in lower power consumption and relaxes the design of the clock distribution



(a)



(b)

Fig. 2.1. Clocking in Future 5G Transceivers. (a) Single Stage synthesizer as the local oscillator. (b) Cascaded synthesizer as the local oscillator.

network in the transceiver. Moreover, the phase shifters required for the beamforming can be embedded within the second stage PLL resulting in further power saving.

Prototypes for both the single stage and cascaded PLLs were designed and fabricated in the 65 nm CMOS process. First, the single stage fractional-N PLL will be presented in this chapter,

then the fractional-N cascaded PLL will be introduced in Chapter 3. In the beginning, an overview of frequency generation techniques will be presented and the reason why PLLs were chosen for this work will be elaborated.

2.2 Background on Frequency Generation Techniques

There exist different ways for frequency generation. This includes injection-locked oscillators (ILOs), frequency multipliers, high-quality factor resonators, voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs). In this section, each of those techniques will be presented and their suitability to serve as LO for mm-Wave wireless transceivers will be discussed.

First, a VCO – as its name implies – is a circuit that generates an output clock whose frequency depends on an input control voltage that is applied to the VCO. There are two popular flavors of the VCO, namely, the ring VCO [45] and the LC VCO [46], [47]. LC VCOs have lower phase noise compared to ring VCOs. However, standalone LC VCO cannot be used as an LO for mm-Wave wireless applications owing to its degraded jitter and phase noise performance [48] which would degrade the overall performance of the wireless transceiver.

High-quality factor (Q) resonators can also be employed as frequency generators. Owing to their high Q, they can provide low jitter clocks even in open loop. Several examples of high-Q resonators can be found in the literature. In [49], two micromachined high-Q resonators were proposed. The first uses suspended microstrip lines on thin dielectric membranes achieving a quality factor of over 450 at 29 GHz and the second is a 3-dimensional micromachined waveguide cavity resonator with planar feedlines achieving 1117 quality factor at 24 GHz. In [50], a non-radiative dielectric guide Gunn oscillator using a metal rod resonator which is supported by Polyether-ether-ketone dielectric pieces was proposed. It attains more than 1500 quality factor at 60 GHz. In [51], a high-Q photonic crystal resonator was presented achieving 5000 quality factor at 100 GHz. Although high-Q resonators are capable of providing good jitter performance, they are not a good choice to serve as an LO for mm-Wave wireless transceivers since they are difficult to be integrated in CMOS technology to provide a fully integrated CMOS solution.

To overcome the limited jitter performance of the standalone VCO and provide better CMOS integration capability, injection-locked oscillators [52], [53] can be employed to improve

the phase noise and jitter performance of the output clock. By injecting a signal into the oscillator, the oscillator output will be locked to the injected signal given that the injection is strong enough. However, great care should be taken in designing the ILO since insufficient injection strength would cause the output clock to be pulled to the injected signal producing unwanted modulation. Under lock, the phase of the output clock follows that of the injected signal. Hence, given that the injected signal is clean, improved jitter performance can be attained for the output clock. Several interesting ILOs were reported in the literature. In [54], a 60 GHz quadrature ILO was proposed which utilizes a 20 GHz injected input coming from a sub-sampling PLL achieving 290 fs jitter while consuming 7.8 mW. In [55], an inverter-based injection-locked quadrature clock generator with phase interpolators was proposed. The injection-locked ring oscillator takes its input from a transformer-based LC VCO generating a 16 GHz output clock with 143 fs jitter while consuming 22.4 mW.

Another technique for clock generation is the frequency multiplication. The frequency multiplier comprises a non-linear circuit that disturbs the input signal generating harmonics of the input signal. Then using a filter, one of the generated harmonics is selected. Having a look at the literature, some interesting frequency multiplier designs can be found. In [56], an injection-locked frequency multiplier was proposed which employs a frequency tracking loop to correct the frequency drift of the quadrature VCO. It generates an output clock with frequency in the range from 27.4 – 30.8 GHz from a 2 – 2.4 GHz input achieving 86 fs jitter while consuming 24.9 mW. The 2 – 2.4 GHz input to the frequency multiplier comes from a PLL. In [57], a 60 GHz 8× frequency multiplier is presented. It employs three amplifiers stages and three stages of frequency doublers consuming 55 mW and achieving 37 dBc harmonic suppression.

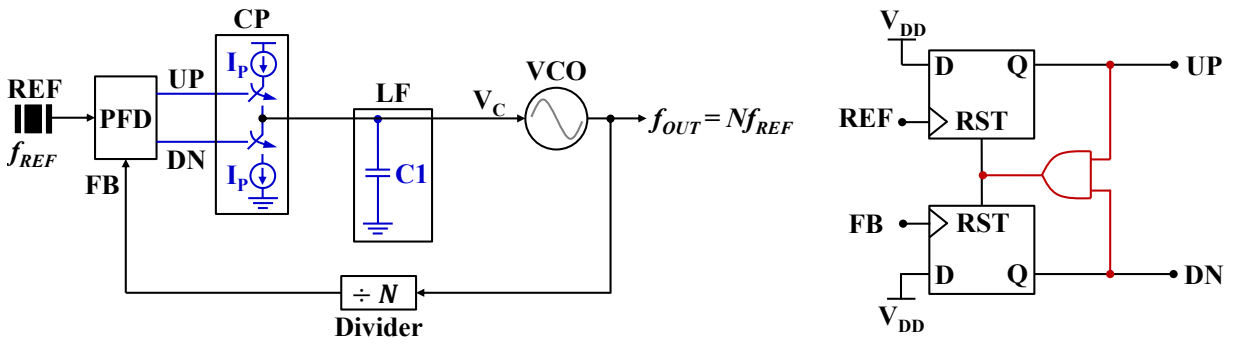
Although the high-quality factor resonators, injection locking and frequency multiplication techniques are capable of generating mm-Wave frequencies with good jitter performance, they are not the best choice to serve as LOs for mm-Wave 5G wireless transceivers. This is due to the fact that the frequency generator's output clock jitter is not the only concern we need to worry about, there are other aspects that have to be taken into account while choosing the LO topology. As discussed in the previous section, in mm-Wave wireless transceivers the high frequency LO clock need to be routed to different locations on the chip which are several millimeters apart. If a central ILO or frequency multiplier is used as the LO, a long chain of buffers will be required for routing such high mm-Wave frequency clock. This will

result in high power consumption in the clock routing network. Also, the clock jitter after the buffer chain will be degraded since each one of those buffers would add around 50 fs of jitter to the output clock. From another perspective, it can be noted that ILOs and frequency multipliers utilize high frequency input reference. If a MHz input reference is used, it will be very difficult to extract the output clock. This is because the separations between the different harmonics will be very small which dictates the need for a filter with very narrow bandwidth to extract the desired output frequency. Such filter is very difficult to design. Also, as the order of the harmonic increases, its power reduces. Hence, the higher the output frequency (i.e., the higher the multiplication factor), the multiplier will need to lock to a higher order harmonic resulting in lower output clock power.

To alleviate those limitations and provide enhanced jitter performance, a PLL was chosen for this work. The PLL is a closed loop feedback system built around a VCO. It locks the VCO's output clock phase to that of a clean MHz reference clock usually generated from a crystal oscillator. By properly choosing the PLL loop parameters and bandwidth, enhanced jitter performance can be attained. In addition, the PLL architecture enables employing the cascaded technique as discussed in the previous section and Fig. 2.1(b) where the PLL is broken into 2 stages allowing low-frequency routing which greatly simplifies the routing network and reduces its power and jitter. In the next section, an introduction to charge-pump PLLs will be introduced.

2.3 Background on Charge Pump PLL

A CPPLL comprises a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a feedback divider as illustrated in Fig. 2.2(a). The loop locks the VCO clock phase to that of a clean input reference clock. The PFD provides digital pulses proportional to the phase error between the input reference clock and the feedback signal. The CP converts the PFD pulses to error current that is introduced to the LF to filter the error current and generate the VCO control voltage. The placement of the divide-by-N frequency divider in the feedback path allows the PLL to perform frequency multiplication, where the frequency of the PLL output (f_{OUT}) becomes N-times that of the input reference clock (f_{REF}). Several textbooks and journal articles discussed charge-pump PLLs [58]–[61]. This section briefly summarizes the operation of the charge pump PLL, its loop dynamics, and design perspectives.



(a) (b)

Fig. 2.2. (a) The Block Diagram of the Type II Charge Pump PLL. (b) The Schematic of the PFD.

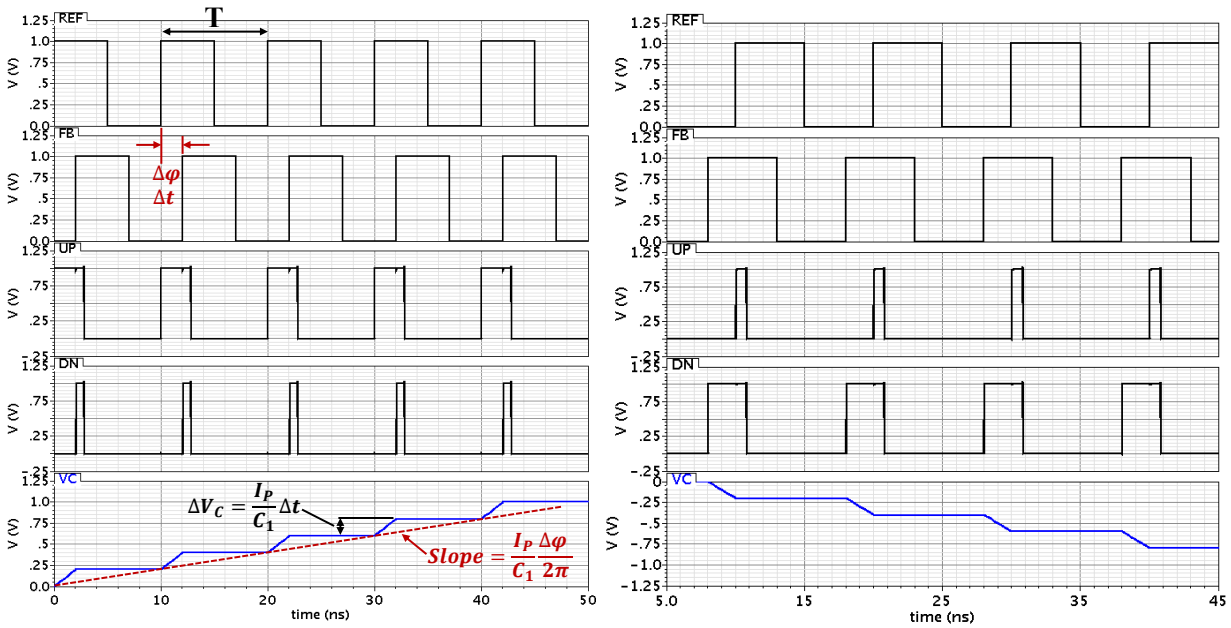
2.3.1 The CPPLL Operation

The type I PLL employing only phase detection suffers from limited acquisition range [58]. This issue is resolved in the type II CPPLL by adding frequency detection to the loop where a PFD is employed. The schematic of the PFD is illustrated in Fig. 2.2(b). The PFD provides pulses at the UP and DN outputs based on the phase relation between its inputs – the reference (REF) and feedback (FB) clocks. As illustrated in Fig. 2.3(a) when REF leads FB, pulses are generated at the UP output of the PFD. In that case, UP goes high at the REF rising edge and remains high till the occurrence of the FB rising edge where DN also rises triggering the flip-flops' reset. Ideally no pulses should appear on the DN output for this case, however, due to the finite delay of the AND and Reset operations, both UP and DN outputs remain high for some time before they are reset. This does not alter the operation of the PFD since we are interested in the difference between the UP and DN signals. The case of REF lagging FB is illustrated in Fig. 2.3(b) where error pulses will be generated at the DN output of the PFD.

The UP/DN outputs control CP switches. The CP sinks or pumps current into the LF based on the UP/DN decision taken by the PFD. In the case when REF leads FB, pulses of width Δt are generated at the UP output of the PFD. Thus results in switching on the UP switch of the CP pumping current I_P to charge the capacitor (C_1) as illustrated in Fig. 2.3(a). For now, the LF only comprises a capacitor C_1. This causes a change in the VCO control voltage given by

$$\Delta V_C = \frac{I_P}{C_1}\Delta t = \frac{I_P}{C_1}T\frac{\Delta\varphi}{2\pi} \tag{2.1}$$

where T is the input period and $\Delta\varphi$ is the phase difference between REF and FB. The increase in the control voltage results in speeding up the VCO and hence the FB signal frequency will be



(a) (b)

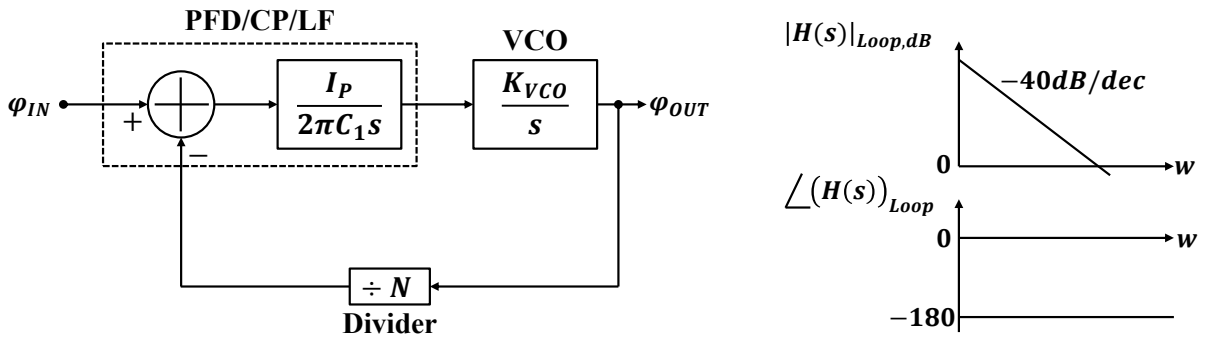
Fig. 2.3. The PFD/CP response with I_P = 100 µA, C_1 = 1 pF and T = 10 ns. (a) When REF leads FB. (b)When REF lags FB.

able to catch up with the REF signal eliminating the phase difference between them. A similar argument can be made in the case when REF lags FB where a drop in V_C occurs as shown in Fig. 2.3(b) and C_1 discharges due to sinking current I_P from the charge pump. The loop exhibits an infinite open loop gain; this can be concluded from the fact that a constant phase difference between REF and FB slowly drives the CP output towards ∞ or -∞. Hence, the PFD/CP combination exhibits an integrator-like transfer function where it produces a ramp output in response to a constant phase difference [59]. The infinite open loop gain also implies that when locking is attained, the phase difference between REF and FB drops to zero. This is unlike the type I PLL which exhibits a finite phase error during locking.

The behavior of the CP output is non-linear, however, it can be linearized by employing the continuous-time (CT) approximation where the CP is assumed to continuously charge C_1 as illustrated by the dotted line in Fig. 2.3 (a) whose slope is $I_P\Delta\varphi/2\pi C_1$. Hence the linearized transfer function of the PFD/CP in response to an input phase step $\Delta\varphi\, u(t)$ can be written as

$$V_C = \frac{I_P}{2\pi C_1}\Delta\varphi t u(t) \tag{2.2}$$

where by taking Laplace transform we get the s-domain model of the PFD/CP as



(a) (b)

Fig. 2.4. (a) The Linear phase model of the CPPLL. (b) The Loop gain frequency response of the CPPLL.

$$\frac{V_C}{\Delta\varphi}(s) = \frac{I_P}{2\pi C_1 s} \tag{2.3}$$

2.3.2 The CPPLL Loop Dynamics

The linear phase model of the CPPLL is illustrated in Fig. 2.4(a). The VCO characteristic can be written as

$$\omega_{OUT} = K_{VCO} V_C \tag{2.4}$$

where ω_{OUT} is the VCO output radian frequency, V_C is the input control voltage and K_{VCO} is the VCO sensitivity in (rad/sec)/V. Since phase is the integral of frequency, we can write

$$\varphi_{OUT} = \int w_{OUT}\, dt = \int K_{VCO} V_C\, dt \tag{2.5}$$

where φ_{OUT} is the phase at the VCO output. By taking the Laplace transform of (2.5) we get the s-domain transfer function of the VCO as

$$\frac{\varphi_{OUT}}{V_C}(s) = \frac{K_{VCO}}{s} \tag{2.6}$$

where the VCO is modeled as an integrator. The open-loop gain (A), feedback factor (β) and the loop gain $H(s)_{LOOP}$ of the CPPLL can be written as

$$A = \left(\frac{\varphi_{OUT}}{\varphi_{IN}}\right)_{OPEN} = \frac{I_P}{2\pi C_1 s}\frac{K_{VCO}}{s}, \qquad \beta = \frac{1}{N}, \qquad H(s)_{Loop} = A\beta = \frac{I_P K_{VCO}}{2\pi C_1 N s^2} \tag{2.7}$$

This PLL is referred to as type II PLL since its open-loop transfer characteristics have two poles at the origin. The presence of two poles at the origin results in an unstable loop as can be

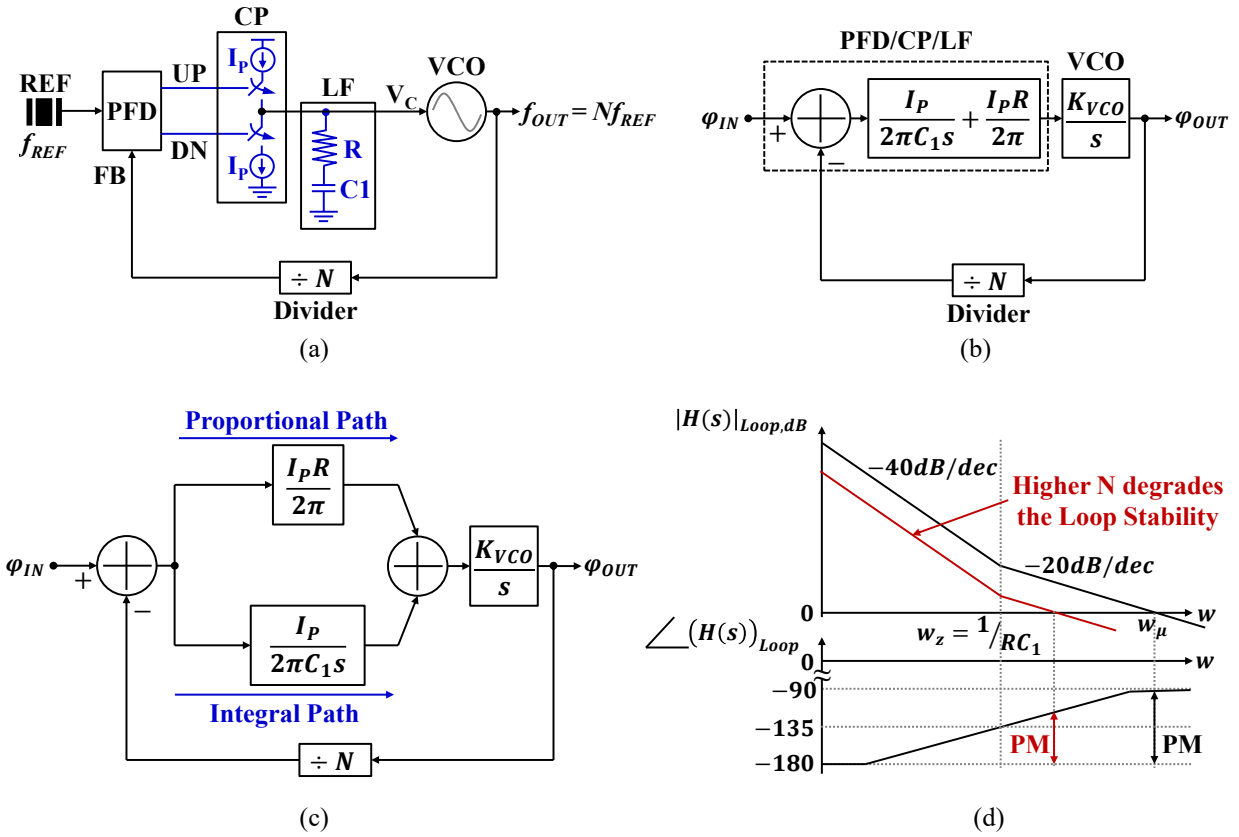


Fig. 2.5. The CPPLL after adding the resistor R to the LF. (a) The Block diagram. (b)The Linear phase model. (c) The proportional and integral paths. (d) The Loop gain frequency response.

concluded from the magnitude and phase responses of the loop gain illustrated in Fig. 2.4 (b). Hence a zero should be added to the transfer characteristics to attain stability. This is achieved by adding a resistor R in series with C_1. Fig. 2.5(a) shows the CPPLL after adding the resistor R to the loop filter. Accordingly, the transfer function of the PFD/CP/LF becomes

$$\frac{V_C}{\Delta\varphi}(s) = \frac{I_P}{2\pi}\left(R + \frac{1}{sC_1}\right) \tag{2.8}$$

as illustrated in Fig. 2.5(b) showing the modified linear phase model of the CPPLL after adding R. The employed LF is referred to as the Proportional–Integral LF. The resistor (R) represents the proportional-path which provides instantaneous phase correction without affecting the average VCO frequency, while the capacitor (C_1) representing the integral-path that integrates the CP current to set the average VCO frequency. The model can be redrawn as illustrated in Fig. 2.5(c) where a proportional path and integral path can be distinguished. The loop gain $H(s)_{LOOP}$ of the CPPLL can be written as

$$H(s)_{Loop} = \frac{I_P}{2\pi}\left(R + \frac{1}{sC_1}\right)\frac{K_{VCO}}{s}\frac{1}{N} = \frac{I_P K_{VCO}(1 + sRC_1)}{2\pi N C_1 s^2} \tag{2.9}$$

showing two poles at the origin in addition to a zero at $\omega_z = {}^1/_{RC_1}$ that helps in stabilizing the loop as illustrated in Fig. 2.5(d). It can also be concluded that increasing the frequency multiplication factor (*N*) provided by the loop results in degrading the phase margin (PM) and hence makes the loop less stable. The closed loop transfer function *H(s)* can be given as

$$H(s) = \frac{\varphi_{OUT}}{\varphi_{IN}} = \frac{A}{1 + A\beta} = \frac{\frac{I_P K_{VCO}}{2\pi C_1}(1 + sRC_1)}{s^2 + \frac{I_P K_{VCO}}{2\pi N}Rs + \frac{I_P K_{VCO}}{2\pi C_1 N}} = N\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.10}$$

where ζ and ω_n are the damping factor and natural frequency of the second order system, respectively given as

$$\zeta = \frac{R}{2}\sqrt{\frac{I_P C_1 K_{VCO}}{2\pi N}}, \qquad \omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1 N}} \tag{2.11}$$

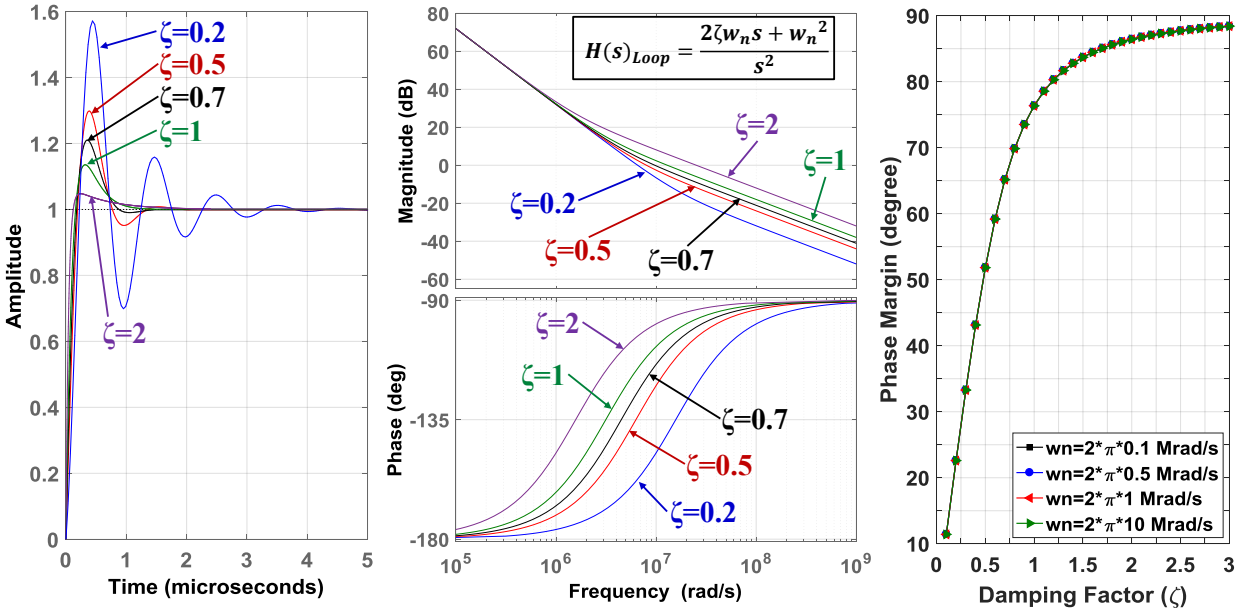
The closed-loop transfer function in (2.10) implies the existence of 2 poles and one zero given as

$$\omega_{P1,2} = \omega_n\left(-\zeta \pm \sqrt{\zeta^2 - 1}\right), \qquad w_z = \frac{-\omega_n}{2\zeta} \tag{2.12}$$

The loop proportional and integral gains denoted as K_P and K_I, respectively can be written as

$$K_P = \frac{I_P R K_{VCO}}{2\pi N} = 2\zeta\omega_n \quad , \qquad K_I = \frac{I_P K_{VCO}}{2\pi C_1 N} = {\omega_n}^2 \tag{2.13}$$

The step response of the CPPLL can be overdamped, critically damped or underdamped based on the value of ζ. If $\zeta > 1$, the poles are real and the system is overdamped, if $\zeta = 1$, the system is critically damped and if $\zeta < 1$, the poles are complex and the system is underdamped. The transfer function of the CPPLL was modeled and simulated in MATLAB. Fig. 2.6(a) shows the simulated step response of the CPPLL for different damping factors with $\omega_n = 2\pi \times 10^6\ rad/s$ where large ringing is observed at lower damping factors. The higher the damping factor, the more stable the PLL is. The phase margin (PM) of the loop gain can also be used as a metric to quantify the loop stability



(a) (b) (c)

Fig. 2.6. (a) The CPPLL step response at different values of damping factor with the natural frequency set to $\omega_n = 2\pi \times 10^6\ rad/s$. (b) The CPPLL Bode Plot of the Loop Gain at different values of damping factor with the natural frequency set to $\omega_n = 2\pi \times 10^6\ rad/s$. (c) Phase Margin of the Loop Gain versus damping factor at different values of w_n.

$$PM = \tan^{-1}\left(\frac{\omega_\mu}{\omega_z}\right) = \tan^{-1}(\omega_\mu R C_1) \tag{2.14}$$

where ω_μ is the unity gain frequency of the loop gain which can be computed by equating the magnitude of the loop gain transfer function given in (2.9) to unity

$$\left|H(s)_{Loop}\right| = \frac{-I_P K_{VCO}}{2\pi N C_1 {\omega_\mu}^2}\sqrt{1+(\omega_\mu R C_1)^2} = 1 \;\rightarrow\; -\omega_\mu^4 + 4\zeta^2\omega_n^2\omega_\mu^2 + \omega_n^4 = 1 \tag{2.15}$$

which yields

$$\omega_\mu = \omega_n\sqrt{2\zeta^2 + \sqrt{4\zeta^4+1}} \tag{2.16}$$

and by substituting in (2.14), the phase margin can be written as

$$PM = \tan^{-1}\left(2\zeta\sqrt{2\zeta^2 + \sqrt{4\zeta^4+1}}\right) \tag{2.17}$$

From which it can be concluded that the phase margin is only dependent on the damping factor ζ. The higher ζ, the higher is the PM and the better the loop stability. This result is also emphasized

with simulations. The simulated loop gain is plotted in Fig. ⁇2.6(b) for different damping factors showing higher PM and enhanced loop stability for larger ζ. Also, the simulated PM of the loop gain versus ζ at different values of ω_n is provided in Fig. ⁇2.6(c) showing that loop stability is independent on ω_n and only depends on ζ which agrees with (⁇2.17).

The closed-loop transfer function of the charge pump PLL, *H(s),* given in (⁇2.10), exhibits a low-pass behavior. The loop bandwidth of the CPPLL can be computed as the frequency at which the magnitude of the closed loop transfer function |*H(s)*| drops by 3 dB from its low-frequency value

$$|H(s)| = \frac{1}{\sqrt{2}} \qquad \rightarrow \qquad \frac{\sqrt{(2\zeta\omega_n\omega)^2 + \omega_n^4}}{\sqrt{(\omega_n^2 - \omega^2)^2 + (2\zeta\omega_n\omega)^2}} = \frac{1}{\sqrt{2}} \tag{2.18}$$

From which we can compute the loop bandwidth (w_{BW}) as

$$\omega_{BW} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{1 + (1 + 2\zeta^2)^2}} \tag{2.19}$$

And the settling speed of the loop is dictated by its time constant (τ) given as

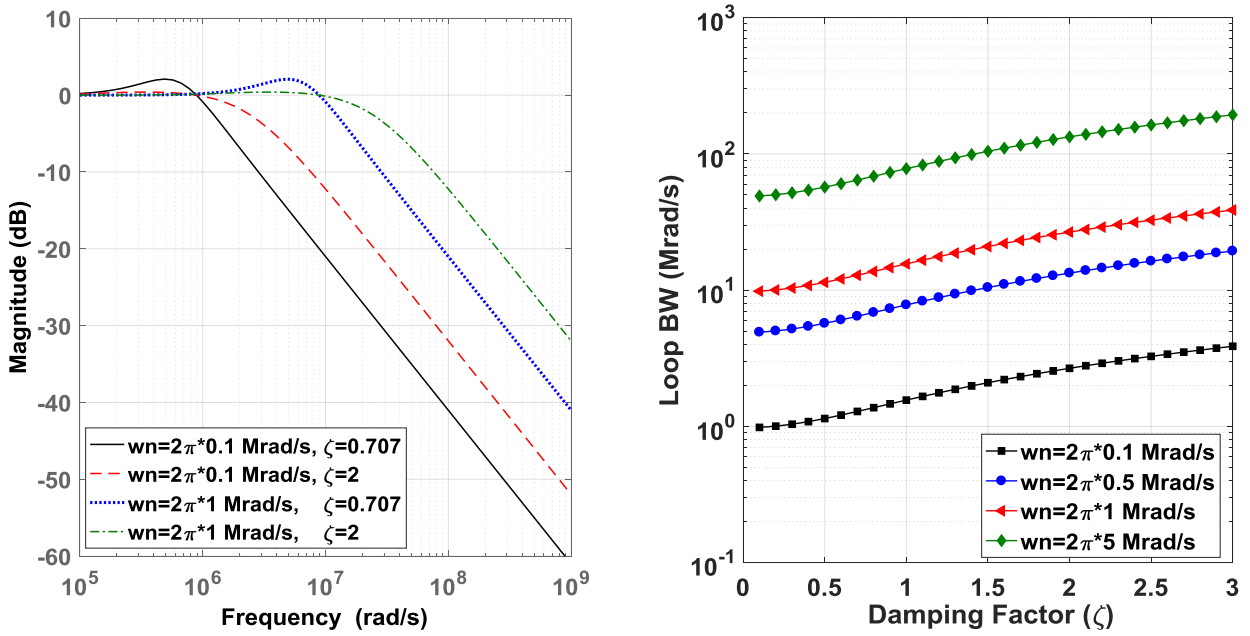
$$\tau = \frac{1}{\omega_{BW}} = \frac{1}{\omega_n \sqrt{1 + 2\zeta^2 + \sqrt{1 + (1 + 2\zeta^2)^2}}} \tag{2.20}$$

Simplified expressions for the loop bandwidth can be extracted for the $\zeta=1/\sqrt{2}$, $\zeta=1$ and $\zeta^2 >> 1$ cases as follows

$$\omega_{BW} = \begin{cases} 2.06\,\omega_n\,, & \zeta = 1/\sqrt{2} \\ 2.48\,\omega_n\,, & \zeta = 1 \\ 2\zeta\,\omega_n\,, & \zeta^2 \gg 1 \end{cases} \tag{2.21}$$

For $\zeta^2>>1$ the loop approaches a single pole system. This can be explained by looking at the poles and zeros given in (⁇2.12) for the case $\zeta^2>>1$ whereby applying Taylor expansion $\sqrt{\zeta^2 - 1} = \zeta\sqrt{1 - 1/\zeta^2} \cong \zeta - 0.5 \times (1/\zeta^2)$, we get

$$\begin{aligned} &\omega_{P1,2} = \omega_n\left(-\zeta \pm \left(\zeta - \frac{1}{2\zeta^2}\right)\right), && \omega_z = \frac{-\omega_n}{2\zeta} \\ &\omega_{P1} = \frac{-\omega_n}{2\zeta} \quad , \omega_{P2} = -2\zeta\omega_n, && \omega_z = \frac{-\omega_n}{2\zeta} \end{aligned} \tag{2.22}$$



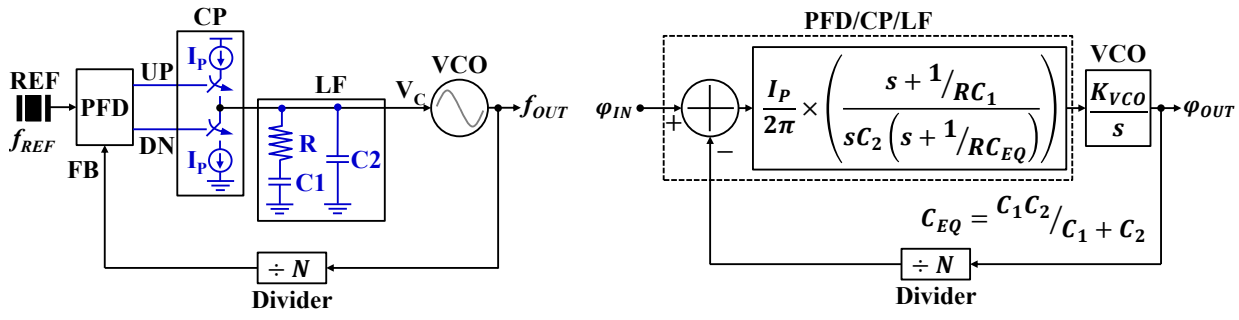
(a) (b)

Fig. 2.7. (a) The CPPLL closed loop magnitude response with N=1. (b) A plot of the Loop Bandwidth versus damping factor for different values of natural frequency.

where the first pole ω_{P1} and the zero ω_Z are co-located canceling the effect of each other's and leaving the loop with only one pole $\omega_{P2} = -2\zeta\omega_n$. This fact can also be shown by simulations. Fig. 2.7(a) shows the simulated closed loop magnitude response of the CPPLL for different combinations of ζ and ω_n where for the case of $\zeta = 2$ ($\zeta^2 >> 1$), the loop approaches a single pole system. The simulated loop bandwidth versus the damping factor at different values of the natural frequency is provided in Fig. 2.7(b) where the bandwidth increases with both ζ and ω_n which agrees with (2.19). For the previous analysis to be valid, it is important to make sure that the continuous-time approximation holds. This is attained by designing the loop such that its time constant is much longer than the input reference period or in other words design the loop bandwidth such that its much smaller than the input reference frequency – as a rule of thumb use $\omega_{BW} = 0.1 \times \omega_{REF}$ where ω_{REF} is the frequency of the input reference clock.

2.3.3 The Third Order CPPLL

The resistor R in the LF adds a zero to the transfer function and helps stabilize the PLL. However, it results in high ripples in the VCO control line. In each cycle when the CP sources or sinks current into the LF an instantaneous jump of magnitude $I_P R$ occurs on V_C. The ripples on the control voltage result in added jitter at the PLL output clock degrading its jitter performance.



(a) (b)

Fig. 2.8. The Third-order CPPLL after adding C_2 to the LF. (a) The Block Diagram. (b) The Phase Model.

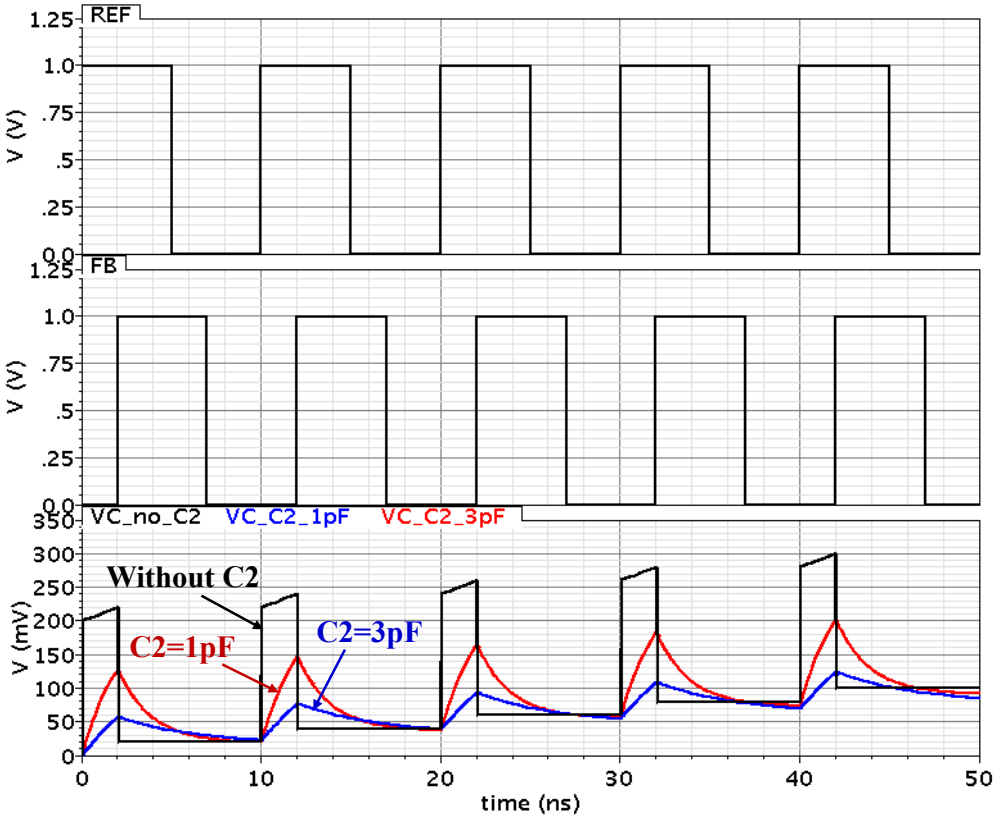


Fig. 2.9. The Capacitor C_2 effect on the PFD/CP/LF response when REF leads FB with I_P = 100 µA, C_1 = 10 pF, R = 2 KΩ and input period T = 10 ns.

By tying the VCO control line to a second capacitor C_2 as illustrated in Fig. 2.8(a), those ripples can be filtered out and lower jitter can be achieved. Fig. 2.9 illustrates the effect of adding the capacitor C_2 on reducing the ripples on V_C where higher C_2 results in quieter V_C signal. The addition of C_2 to the loop filter increases the loop order to a third order CPPLL and adds another pole to its transfer function degrading its stability. Hence we cannot indefinitely increase the value of C_2. This creates a trade-off between lower V_C ripples and loop stability. Fig. 2.8(b)

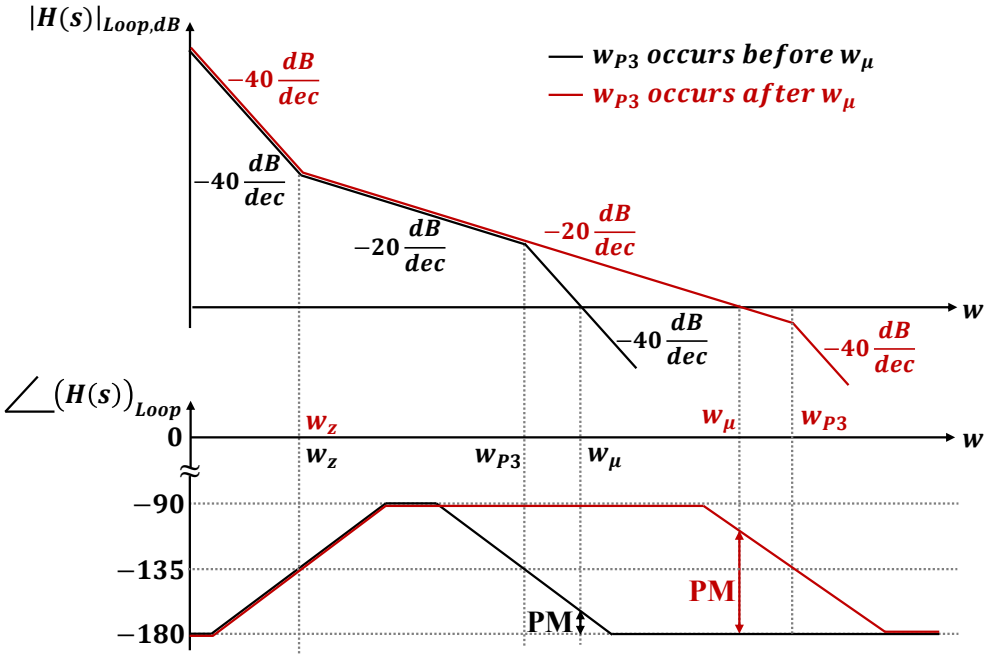


Fig. 2.10. The Loop gain frequency response of the third-order CPPLL for $w_{P3} > w_\mu$ and $w_{P3} < w_\mu$.

illustrates the phase model for the third order loop. The open loop gain of the third order CPPLL is given as

$$H(s)_{Loop} = \frac{I_P}{2\pi}\left(\frac{s + {}^{1}/_{RC_1}}{sC_2\left(s + {}^{1}/_{RC_{EQ}}\right)}\right)\frac{K_{VCO}}{s}\frac{1}{N} = \frac{I_P K_{VCO}}{2\pi N C_2 s^2}\left(\frac{s + {}^{1}/_{RC_1}}{s + {}^{1}/_{RC_{EQ}}}\right) \tag{2.23}$$

where C_{EQ} is the equivalent capacitance of the LF given as $C_{EQ}=C_1C_2/(C_1+C_2)$. The loop gain imposes two poles at the origin, one pole at $\omega_{P3} = {}^{1}/_{RC_{EQ}}$ and a zero at $\omega_z = {}^{1}/_{RC_1}$. The loop gain frequency response is illustrated in Fig. 2.10 where it can be concluded that for improved phase margin and hence loop stability, the choice of C_2 should be such that the pole w_{P3} occurs after the unity gain frequency w_μ. The phase margin of the third order loop can be written as [59], [62]

$$PM = \tan^{-1}\left(\frac{w_\mu}{w_z}\right) - \tan^{-1}\left(\frac{w_\mu}{w_{P3}}\right) = \tan^{-1}(\omega_\mu RC_1) - \tan^{-1}(\omega_\mu RC_{EQ}) \tag{2.24}$$

According to [59], ω_μ is approximately the same for the second and third order CPPLLs. Hence, by substituting (2.16) in (2.24) we get

$$PM = \tan^{-1}\left(4\zeta^2\left(1+\frac{1}{32\zeta^2}\right)\right) - \tan^{-1}\left(4\zeta^2\frac{C_{EQ}}{C_1}\left(1+\frac{1}{32\zeta^2}\right)\right) \cong \tan^{-1}(4\zeta^2) - \tan^{-1}\left(4\zeta^2\frac{C_{EQ}}{C_1}\right) \quad (2.25)$$

That approximation is valid if $32\zeta^2$ >>1. To find the value of ω_μ that maximizes the phase margin, differentiate (2.24) with respect to ω_μ and equate to zero. This yield

$$\omega_{\mu,opt} = \omega_z\sqrt{1+\frac{C_1}{C_2}} = \frac{1}{RC_1}\sqrt{1+\frac{C_1}{C_2}} \quad (2.26)$$

By substituting in (2.24), the optimal phase margin can be found to be

$$PM_{Max} = \tan^{-1}\left(\sqrt{1+\frac{C_1}{C_2}}\right) - \tan^{-1}\left(\frac{1}{\sqrt{1+\frac{C_1}{C_2}}}\right) = \tan^{-1}\left(\frac{\frac{C_1}{C_2}}{2\sqrt{1+\frac{C_1}{C_2}}}\right) \quad (2.27)$$

The corresponding damping factor can be found to be

$$\zeta_{PMmax} = \frac{1}{2}\sqrt[4]{\frac{C_1}{C_{EQ}}} \quad (2.28)$$

Moreover, it worth to be noted that in the presence of C_2, R cannot be indefinitely large since in that case, ω_μ will be higher than ω_{P3} causing stability issues as depicted from Fig. 2.10. Thus, the upper limit for R can be extracted by equating ω_μ and ω_{P3},

$$R \le \sqrt{\frac{2\pi}{I_P K_{VCO} C_{EQ}}} \quad , \quad \frac{C_2}{C_1+C_2} \le \frac{1}{4\zeta^2} \quad (2.29)$$

An expression relating the third order PLL parameters can be derived by substituting the unity gain frequency given by (2.26) into the magnitude of the loop gain defined in (2.23) and equating to unity;

$$\left|H(s)_{Loop}\right|_{s=jw_\mu} = 1 \quad \rightarrow \quad \frac{I_P K_{VCO}}{2\pi N} = \left(\frac{1}{RC_1}\right)^2 \times (C_1+C_2) \times \sqrt{1+\frac{C_1}{C_2}} \quad (2.30)$$

The closed loop frequency response of the third order CPPLL can be written as

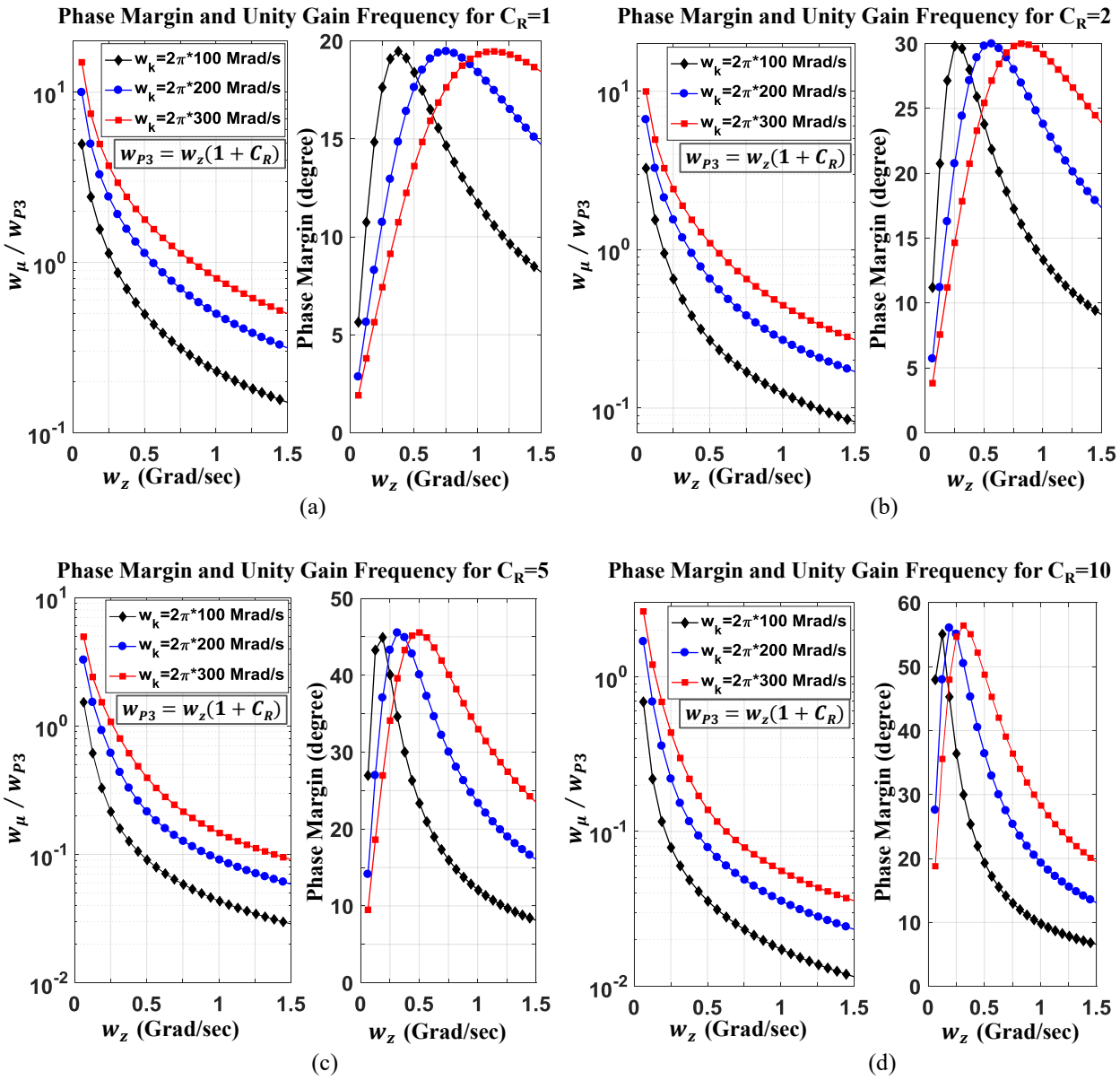


Fig. 2.11. The unity gain frequency and phase margin versus w_z for different values of w_k. (a) For $C_R = 1$. (b) For $C_R = 2$. (c) For $C_R = 5$. (d) For $C_R = 10$.

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_2}\left(s + \frac{1}{RC_1}\right)}{s^3 + \frac{1}{RC_{EQ}}s^2 + \frac{I_P K_{VCO}}{2\pi N C_2}s + \frac{I_P K_{VCO}}{2\pi N R C_1 C_2}} \tag{2.31}$$

Since it is not easy to formulate a simple closed form of the frequency response of the third order PLL in terms of damping factor and natural frequency, we shall rely on the MATLAB analysis of the third systems and monitor the effect of the different PLL parameters on its performance. The loop gain and closed loop frequency responses can be re-written as

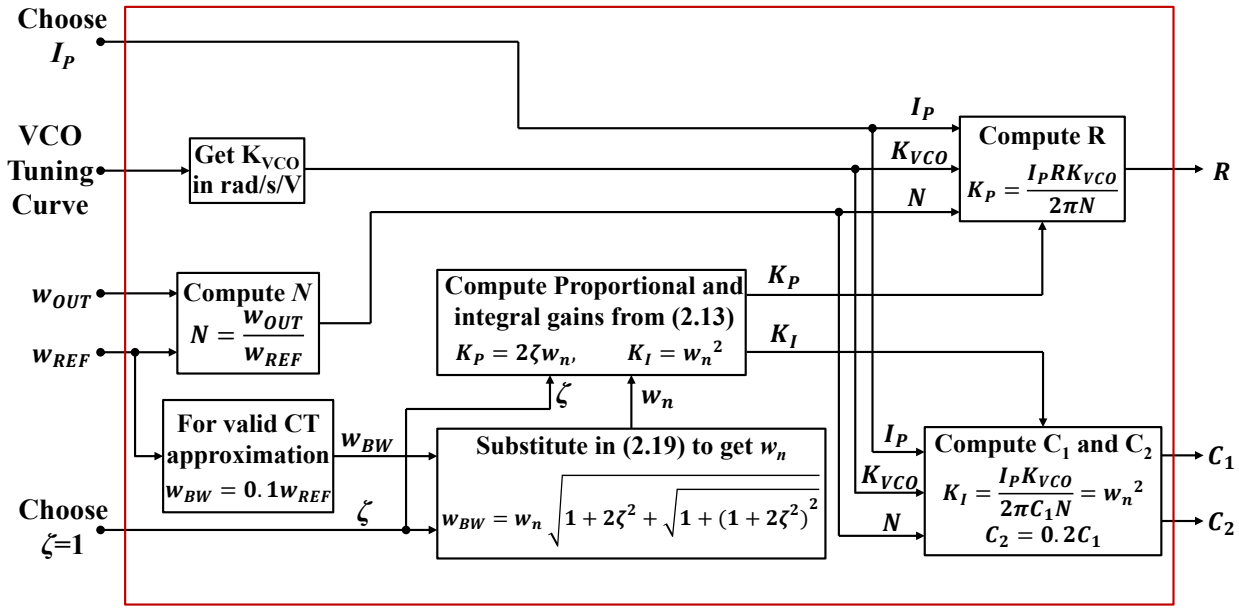


Fig. 2.12. Design perspectives to determine the CPPLL loop parameters.

$$H(s)_{Loop} = = \frac{{w_K}^2(s + w_z)}{s^2\left(s + w_z(1 + C_R)\right)} \tag{2.32}$$

$$H(s) = \frac{{w_K}^2(s + w_z)}{s^3 + w_z(1 + C_R)s^2 + {w_K}^2 s + {w_K}^2 w_z} \tag{2.33}$$

where

$$w_z = \frac{1}{RC_1}, \qquad C_R = \frac{C_1}{C_2}, \qquad w_K = \sqrt{\frac{I_P K_{VCO}}{2\pi N C_2}} \tag{2.34}$$

Plots of the unity gain frequency w_μ and phase margin versus w_z for different values of w_k and C_R are shown in Fig. 2.11. From the obtained results it can be concluded that at higher values of C_R (i.e., lower C_2), the ratio w_μ/w_{p3} reduces resulting in improved phase margin which agrees with (2.27). This improvement in the phase margin comes at the cost of increased ripples on the VCO control voltage line. Also, it can be concluded that lower w_K and/or higher C_R results in the peak phase margin occurring at lower w_z with steeper phase margin versus w_z transfer function.

Fig. 2.12 illustrates an algorithm for determining the loop parameters of the CPPLL [59] where C_R is set to 5 and ζ is set to 1 to guarantee PM of 45°. However, other choices of ζ and C_R can be made. The higher C_R, the higher the PM and the better the loop stability, however, the more will be the ripples on the VCO control line. Hence, this trade-off has to be considered while choosing the value of C_2.

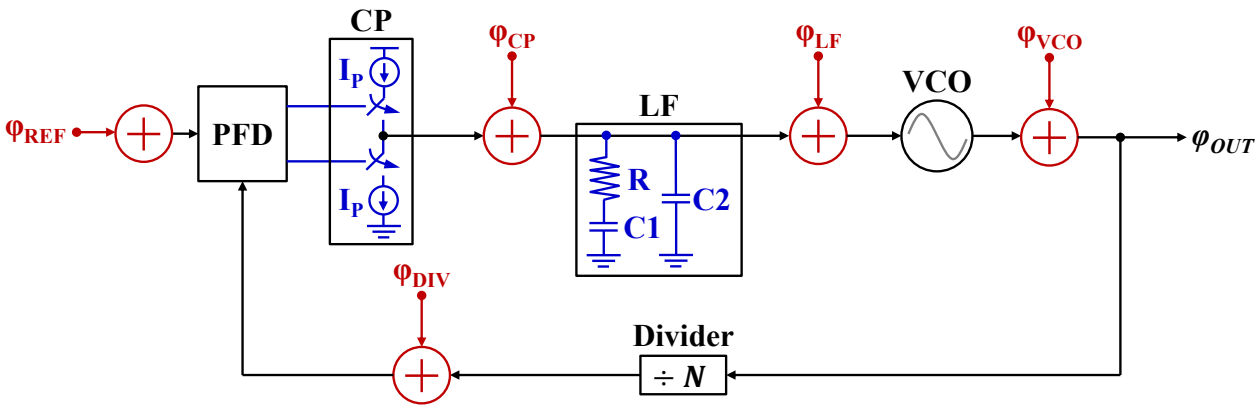


Fig. 2.13. The noise sources of the CPPLL.

2.3.4 Phase Noise in CPPLL

Each component of the PLL contributes to noise and affects the PLL's overall output phase noise [63],[64]. Fig. 2.13 illustrates the block diagram of the CPPLL with the different noise sources added, namely, the input reference noise (φ_{REF}), the CP noise (φ_{CP}), the LF noise (φ_{LF}), the VCO noise (φ_{VCO}) and the divider noise (φ_{DIV}). The phase noise of element X – denoted by $\pounds_X$ – can be thought of as $\varphi_X{}^2$. The overall phase noise at the CPPLL output ($\pounds_{OUT}$) is the superposition of all the noise PLL noise sources each multiplied by its corresponding noise transfer function (NTF)

$$\pounds_{OUT} = \pounds_{REF} \times NTF_{REF} + \pounds_{VCO} \times NTF_{VCO} + \pounds_{CP} \times NTF_{CP} + \pounds_{LF} \times NTF_{LF} + \pounds_{DIV} \times NTF_{DIV} \tag{2.35}$$

where $\pounds_{REF}$, $\pounds_{VCO}$, $\pounds_{CP}$, $\pounds_{LF}$, and $\pounds_{DIV}$ are the phase noise for the reference clock, the VCO, the charge pump, the loop filter, and divider, respectively, and NTF_{REF}, NTF_{VCO}, NTF_{CP}, NTF_{LF}, NTF_{DIV} are their corresponding noise transfer functions. The charge pump noise comprises two components [65], the flicker noise component and the thermal noise component. The overall charge pump phase noise can be written as

$$\pounds_{CP} = 4KTg_m \times D\left(1 + D\frac{f_c}{f}\right) \tag{2.36}$$

with $4KTg_m$ as the thermal noise component, K is Boltzmann's constant, T is the absolute temperature, g_m is the CP transconductance, D is the CP duty cycle in the locked state, f_c is the $1/f$ noise corner frequency and f is the offset frequency. The loop filter noise is dominated by its resistor (R) thermal noise. Hence the phase noise of the loop filter can be written as

$$£_{LF} = 4KTR \tag{2.37}$$

For the VCO, the flicker noise contributes to a $1/f^3$ phase noise component while the white noise contributes to a $1/f^2$ phase noise component [48]

$$£_{VCO} = \frac{\alpha}{f^3} + \frac{\beta}{f^2} \tag{2.38}$$

where α and β are proportionality constants. The VCO phase noise is dominated by the $1/f^2$ component at high offset frequencies. The noise transfer function for each of the above noise sources – denoted by X – is computed as

$$NTF_X = \frac{A_X(s)}{1 + H(s)} \tag{2.39}$$

where $A_X(s)$ is the forward gain experienced by the noise source and $H(s)$ is the loop gain. The loop gain $H(s)$ is given as

$$H(s) = K_D \times L(s) \times \left(\frac{K_{VCO}}{s}\right) \times \left({}^1/_N\right) = \left({}^{I_P}/_{2\pi}\right) \times \left(R + \frac{1}{sC_1}\right) \times \left(\frac{K_{VCO}}{s}\right) \times \left({}^1/_N\right) \tag{2.40}$$

where K_D is the PFD/CP gain, $L(s)$ is the loop filter transfer function, I_P is the charge-pump current and K_{VCO} is the VCO sensitivity in (rad/s/V). The forward gain for the different noise sources can be found to be

$$A_{REF}(s) = K_D L(s) \left(\frac{K_{VCO}}{s}\right) = \left({}^{I_P}/_{2\pi}\right) \left(R + \frac{1}{sC_1}\right) \left(\frac{K_{VCO}}{s}\right) \tag{2.41}$$

$$A_{DIV}(s) = -K_D L(s) \left(\frac{K_{VCO}}{s}\right) = -\left({}^{I_P}/_{2\pi}\right) \left(R + \frac{1}{sC_1}\right) \left(\frac{K_{VCO}}{s}\right) \tag{2.42}$$

$$A_{CP}(s) = L(s) \left(\frac{K_{VCO}}{s}\right) = \left(R + \frac{1}{sC_1}\right) \left(\frac{K_{VCO}}{s}\right) \tag{2.43}$$

$$A_{LF}(s) = \left(\frac{K_{VCO}}{s}\right) \tag{2.44}$$

$$A_{VCO}(s) = 1 \tag{2.45}$$

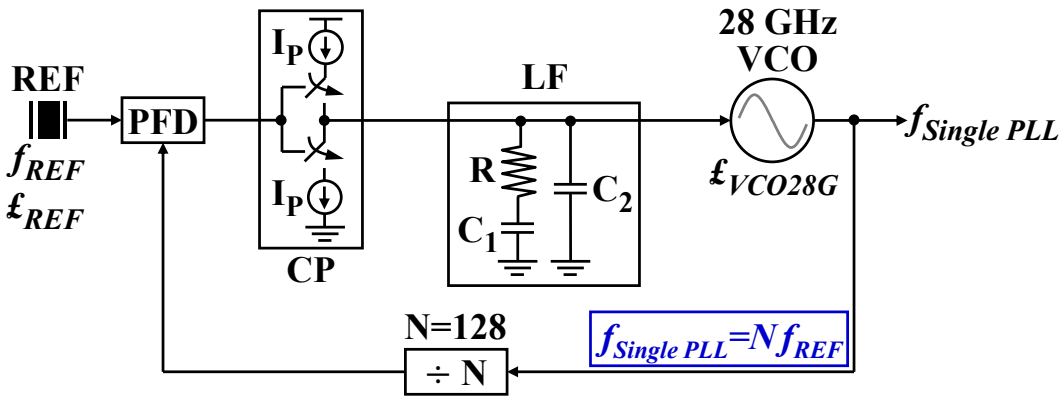


Fig. 2.14. The block diagram of the single stage 28 GHz Integer-N CPPLL.

The overall PLL phase noise can be written by substituting in (2.35)

$$\pounds_{OUT} = \pounds_{REF} \times N^2|G(s)|^2 + \pounds_{VCO} \times |1 - G(s)|^2 + \pounds_{DIV} \times N^2|G(s)|^2 + \pounds_{CP} \times \left(\frac{2\pi N}{I_P}\right)^2 |G(s)|^2 + \pounds_{LF} \times K_{VCO}\left|\frac{s}{(1 - G(s))}\right|^2 \quad (2.46)$$

with *G(s)* given as

$$G(s) = \frac{{}^{I_P R K_{VCO}}/_{2\pi N}\, s + {}^{I_P K_{VCO}}/_{2\pi N C_1}}{s^2 + {}^{I_P R K_{VCO}}/_{2\pi N}\, s + {}^{I_P K_{VCO}}/_{2\pi N C_1}} \quad (2.47)$$

2.4 The Single Stage 28 GHz Fractional-N Frequency Synthesizer

In this section, the single stage frequency synthesizer is discussed. It is designed as a fractional-N 28-GHz CPPLL in the TSMC 65 nm CMOS process. First, the phase noise analysis of the single stage CPPLL will be introduced.

2.4.1 Phase Noise Analysis of the Single Stage 28 GHz CPPLL

The block diagram of the 28 GHz integer-N CPPLL is illustrated in Fig. 2.14 employing a PFD, CP, LF, 28 GHz VCO, and a feedback divider. The 28 GHz single stage synthesizer carries out frequency multiplication of $N = 128$ to lock the 28 GHz VCO output to a 220 MHz reference clock. The loop bandwidth ($f_{BW,Single}$) greatly influences the PLL performance. It should be chosen to balance the noise transfer functions from different sources. The simulated phase noise

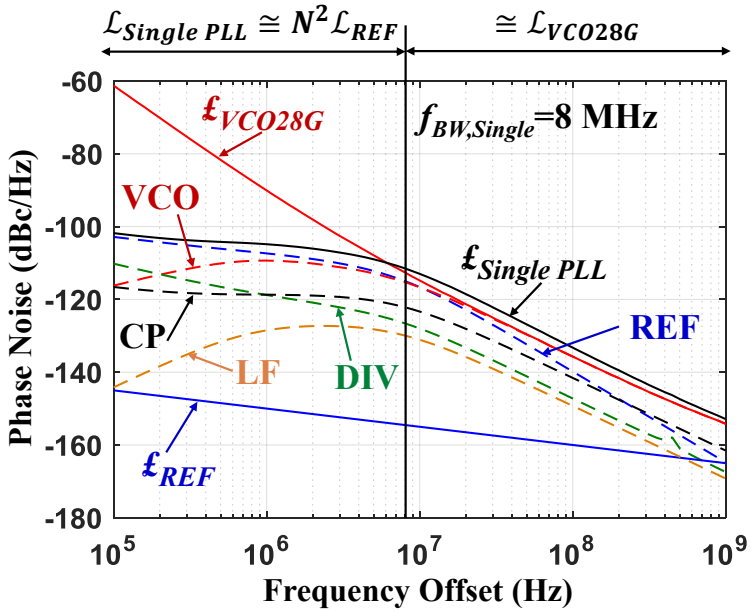


Fig. 2.15. The Simulated Phase Noise performance of the Single-stage Integer-N 28 GHz synthesizer.

Table 2.1
Contribution of the Different PLL Elements to the overall output Jitter

Noise Contributor	PN Integral	Jitter (σ_{RMS})	% Contribution
Reference	409.3×10^6	162.63 fs	48.62%
VCO	329.38×10^6	145.89 fs	39.13%
Charge Pump (CP)	61.05×10^6	62.81 fs	7.25%
Loop Filter (LF)	9.47×10^6	24.73 fs	1.11%
Divider	32.7×10^6	46.02 fs	3.89%
Overall PLL	841.9×10^6	233.24 fs	

of the 28 GHz single-stage synthesizer taking into account all of the PLL noise sources is illustrated in Fig. 2.15. The RMS jitter (σ_{RMS}) at the PLL output can be computed as

$$\sigma_{RMS} = \frac{1}{2\pi f_{Single\ PLL}}\sqrt{2\int_{f_A}^{f_B} \mathcal{L}_{Single\ PLL}\ df} \tag{2.48}$$

where $f_{Single\ PLL}$ is the PLL output frequency and f_A and f_B are the integration limits. The output phase noise for each of the noise sources shown in Fig. 2.15 was integrated from 100 kHz to 1 GHz to quantify their integrated jitter and relative jitter contribution in Table 2.1. The two dominant contributors are the VCO for its poor phase noise at 28 GHz and the reference due to the large multiplication factor. Carrying out the integration in (2.48), generally, does not result in

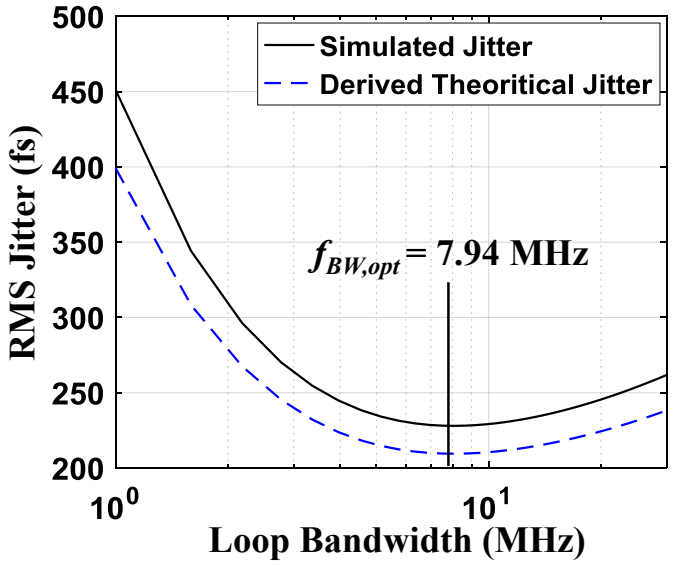


Fig. 2.16. The Simulated/Theoretical RMS Jitter versus Loop bandwidth of the conventional Single-stage Integer-N 28 GHz synthesizer.

a closed form and requires numerical techniques. Hence to get a closed form expression we are approximating similar to [66] considering only the reference and VCO phase noise that contribute to more than 88% of the overall output jitter. Thus, without loss of generality, we can neglect the CP, LF and divider phase noise to get a closed form expression for the PLL output jitter. Since the PLL output jitter is dominated by the reference and VCO phase noise, the main trade-off in the choice of the PLL bandwidth arises from the fact that the PLL shapes the reference noise by a low-pass transfer function while it shapes the VCO noise by a high-pass transfer function as can be concluded from (2.46). That is, lower PLL bandwidth filters out more reference noise at the cost of higher VCO noise, and vice versa. At low offset frequencies $f \leq f_{BW,Single}$, the PLL output phase noise is dominated by the reference phase noise and is given as $N^2 £_{REF}$ while at high offset frequencies $f > f_{BW,Single}$, the PLL output phase noise is dominated by the VCO phase noise and is given as $£_{VCO}$. Hence, the phase noise of the single stage PLL can be defined in two regions as

$$£_{Single\ PLL} = \begin{cases} N^2 £_{REF} & , f \leq f_{BW,Single} \\ £_{VCO28G} = \dfrac{\beta}{f^2} & , f > f_{BW,Single} \end{cases} \tag{2.49}$$

where at high offset frequencies, the VCO is dominated by the $1/f^2$ component with β as the proportionality constant. By substituting (2.49) in (2.48) we get

$$\sigma_{RMS} = \frac{\sqrt{2}}{2\pi f_{Single\ PLL}} \times \sqrt{£_{REF} \times N^2\left(f_{BW,Single} - f_A\right) - \frac{\beta}{f_B} + \frac{\beta}{f_{BW,Single}}} \tag{2.50}$$

Now, to get the optimal loop bandwidth $f_{BW,opt}$ for minimum RMS jitter, we need to differentiate (2.50) with respect to $f_{BW,Single}$ and equate to zero. This yield

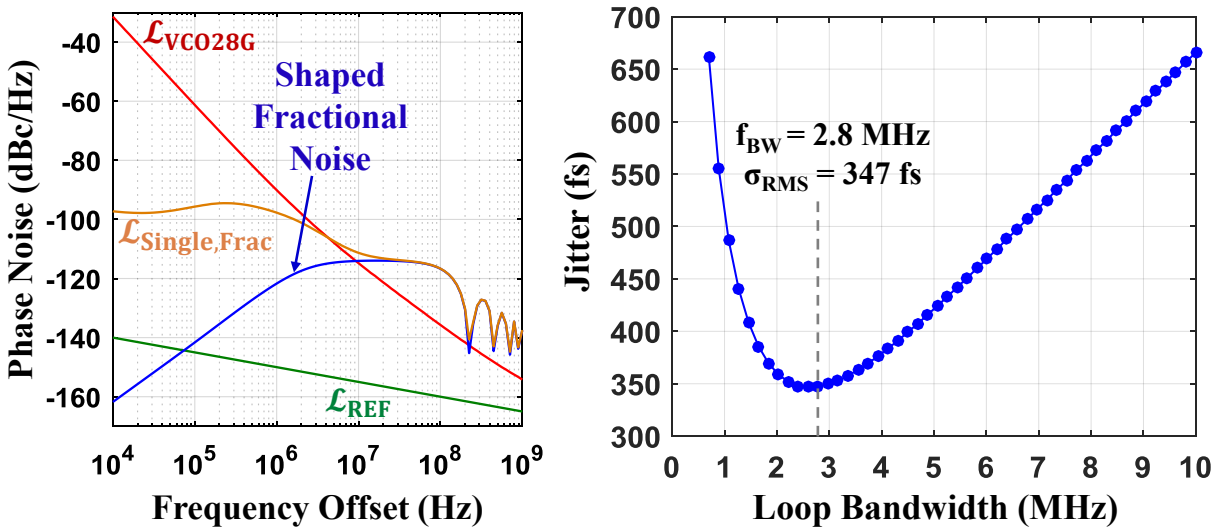
$$f_{BW,opt} = \sqrt{\frac{\beta}{N^2 £_{REF}}} \tag{2.51}$$

The result obtained in (2.51) agrees with the rule of thumb in designing the PLL loop bandwidth where the loop bandwidth is chosen as the intersection of the amplified reference phase noise and the VCO phase noise, i.e., $N^2£_{REF} = \beta/f^2$. In case the phase noise performance of the VCO and the input reference clock are known, it is more efficient to use (2.51) for determining the loop bandwidth instead of setting it to $0.1 \times f_{REF}$. Fig. 2.16 provides a plot of the simulated and derived RMS jitter versus loop bandwidth for the 28 GHz single stage PLL showing an optimal bandwidth of 8 MHz. From the obtained results it can be concluded that the derived jitter expression in (2.50) is a bit optimistic since it neglects CP, divider and LF noise. However, it is accurate in determining the optimal loop bandwidth as the PLL phase noise is dominated by the reference phase noise and the VCO phase noise that are considered in the theoretical derivation.

Fractional division in synthesizers is required for fine frequency resolution at the PLL output which is necessary for wireless transceivers. In this work, the fractional division is attained using phase interpolation as will be discussed in the next section. Fractional division introduces additional noise resulting in degraded phase noise performance of the fractional-N PLL compared to its integer-N counterpart. The fractional division noise is given as [67],

$$Fractional\ Noise = \frac{\Delta^2}{12 f_{REF}} \left(2 \sin\left(\frac{\pi f}{f_{REF}}\right)\right)^{2m-2} \tag{2.52}$$

where m is the modulator order and Δ is $2\pi/n$ for the multi-phase fractional-N synthesizer with n as the number of phases involved in the fractional division. Similar to the reference noise, the fractional noise is shaped by the low-pass transfer function of the PLL and hence lower PLL loop bandwidth is required to filter out the fractional noise. Fig. 2.17(a) provides the phase noise performance of the fractional-N single stage PLL assuming a first-order 256 phase fractional divider where the shaped fractional noise is shown in blue. The simulated jitter versus loop



(a) (b)

Fig. 2.17. (a) The simulated phase noise performance of the single-stage Fractional-N 28 GHz PLL. (b) The simulated jitter versus PLL loop bandwidth for the single stage Fractional-N 28 GHz PLL.

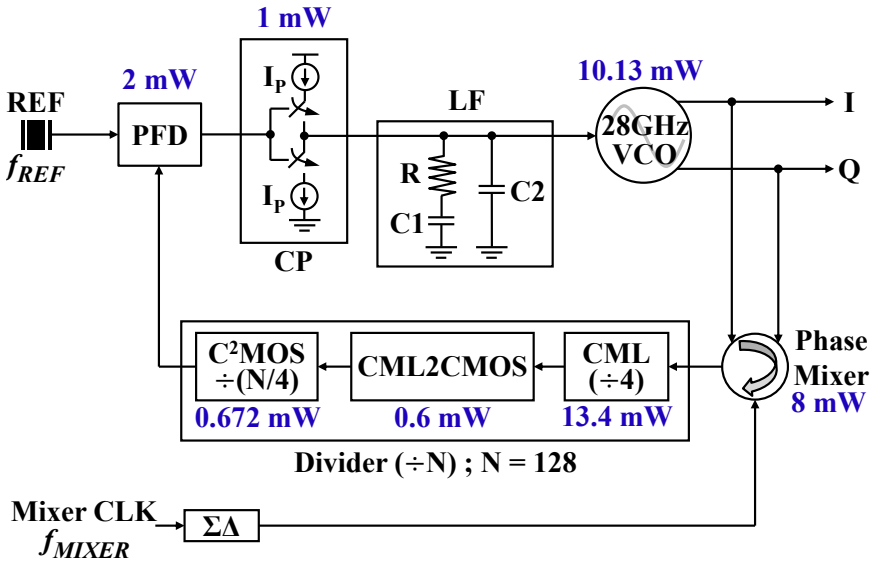
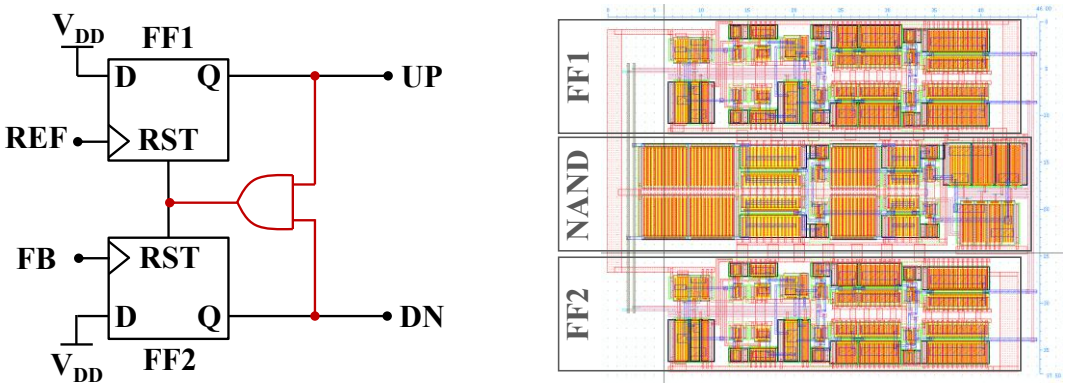


Fig. 2.18. The block diagram of the proposed single stage 28 GHz fractional-N frequency synthesizer.

bandwidth for the single stage fractional-N PLL is shown in Fig. 2.17(b) where optimal jitter performance is attained at loop bandwidth of 2.8 MHz.

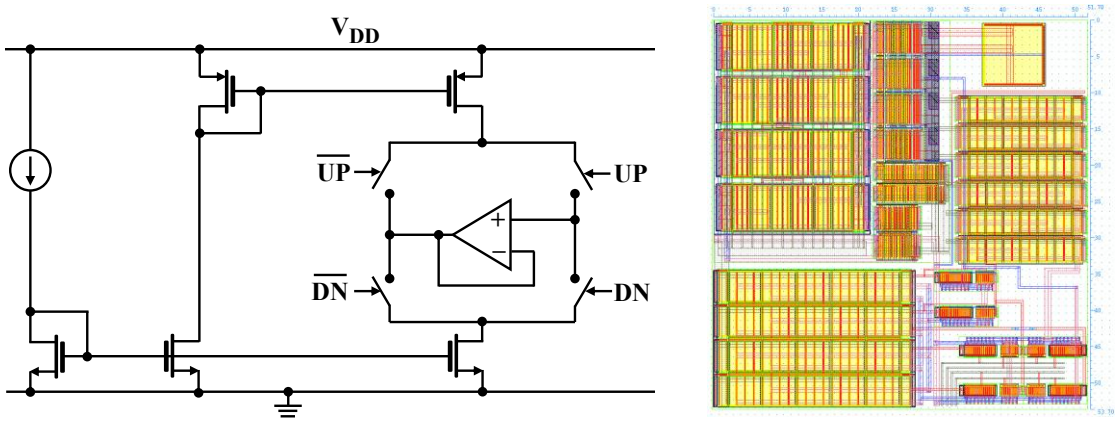
2.4.2 Transistor-level Implementation of the Single Stage Synthesizer

The block diagram of the proposed 28 GHz single stage fractional-N synthesizer is illustrated in Fig. 2.18 comprising a PFD, a CP, a second-order LF, a quadrature 28 GHz VCO, a phase mixer for the fractional division and a divide-by-128 feedback divider.



(a) (b)

Fig. 2.19. The implemented phase-frequency detector (PFD). (a) Schematic. (b) Layout.



(a) (b)

Fig. 2.20. The implemented charge pump (CP). (a) Schematic. (b) Layout.

2.4.2.1 The PFD/CP Implementation

A conventional PFD is employed to compare the reference and feedback clocks using two reset flip-flops and an AND gate as illustrated in Fig. 2.19(a). The layout of the PFD is illustrated in Fig. 2.19(b) occupying an area of 46 µm × 37.5 µm. The schematic of the CP is illustrated in Fig. 2.20(a). To reduce the mismatch within the CP and hence the reference spurs, the CP employs long channel devices and an error amplifier. This resulted in reduced CP duty cycle error in the locked state and hence lowering the CP phase noise and reference spurs significantly. The layout of the CP occupies an area of 51.7 µm × 53.7 µm as illustrated in Fig. 2.20 (b).

2.4.2.2 The 28 GHz Quadrature VCO Implementation

The schematic of the 28 GHz quadrature VCO together with its design parameters are illustrated in Fig. 2.21(a) employing both active and passive (through LC) coupling. A 7-bit digital

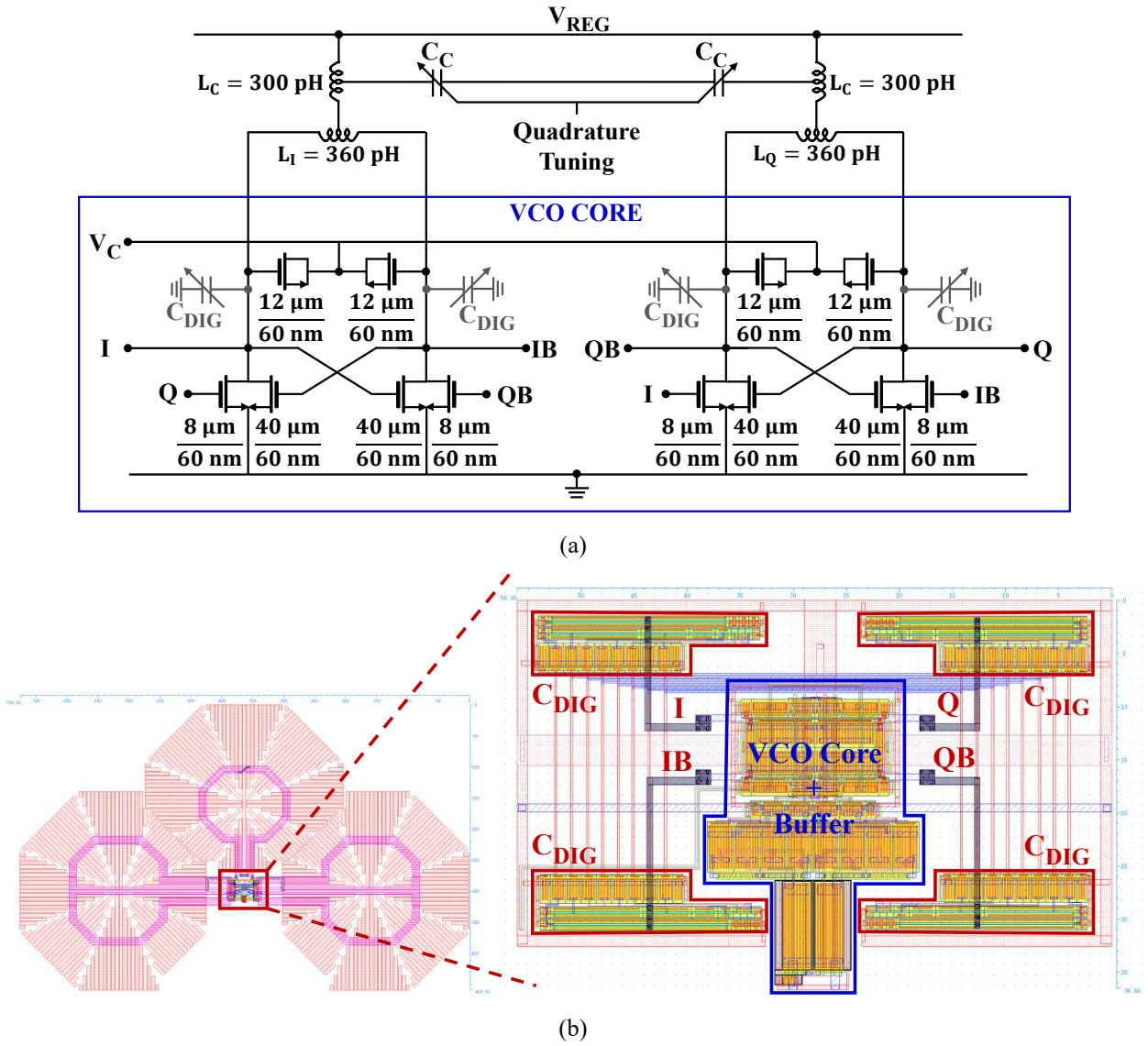


Fig. 2.21. The implemented 28 GHz Quadrature VCO. (a) Schematic. (b) Layout.

capacitor bank C_{DIG} is employed for extended VCO tuning range. The overall VCO layout occupies an area of 724.5 µm × 458.9 µm with the VCO core, buffer, and digital capacitor occupying 56 µm × 36.5 µm as shown in Fig. 2.21(b). By adjusting the coupling varactors' capacitance (C_C), the quadrature correction is provided. Fig. 2.22 shows the post layout simulated I/Q error versus C_C where zero I/Q error is attained at C_C=*700 fF*.

2.4.2.3 The Divide-by-128 Divider Implementation

A feedback frequency divider is employed for the divide-by-128 operation comprising a 2-stage master-slave current-mode logic (CML) divide-by-2 followed by a CML-to-CMOS circuit then a

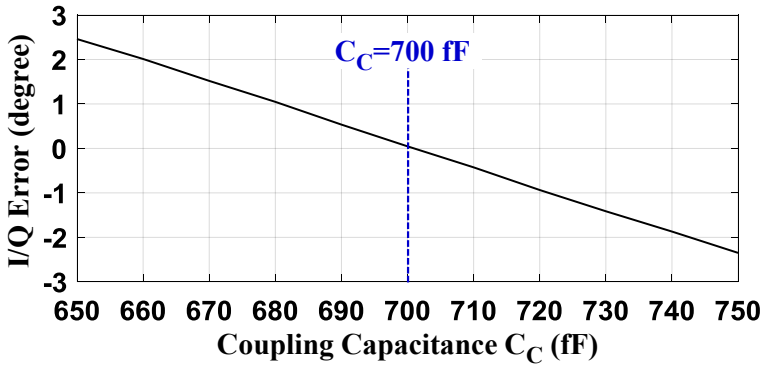


Fig. 2.22. The Post layout simulated I/Q error versus coupling capacitance for the 28 GHz quadrature VCO.

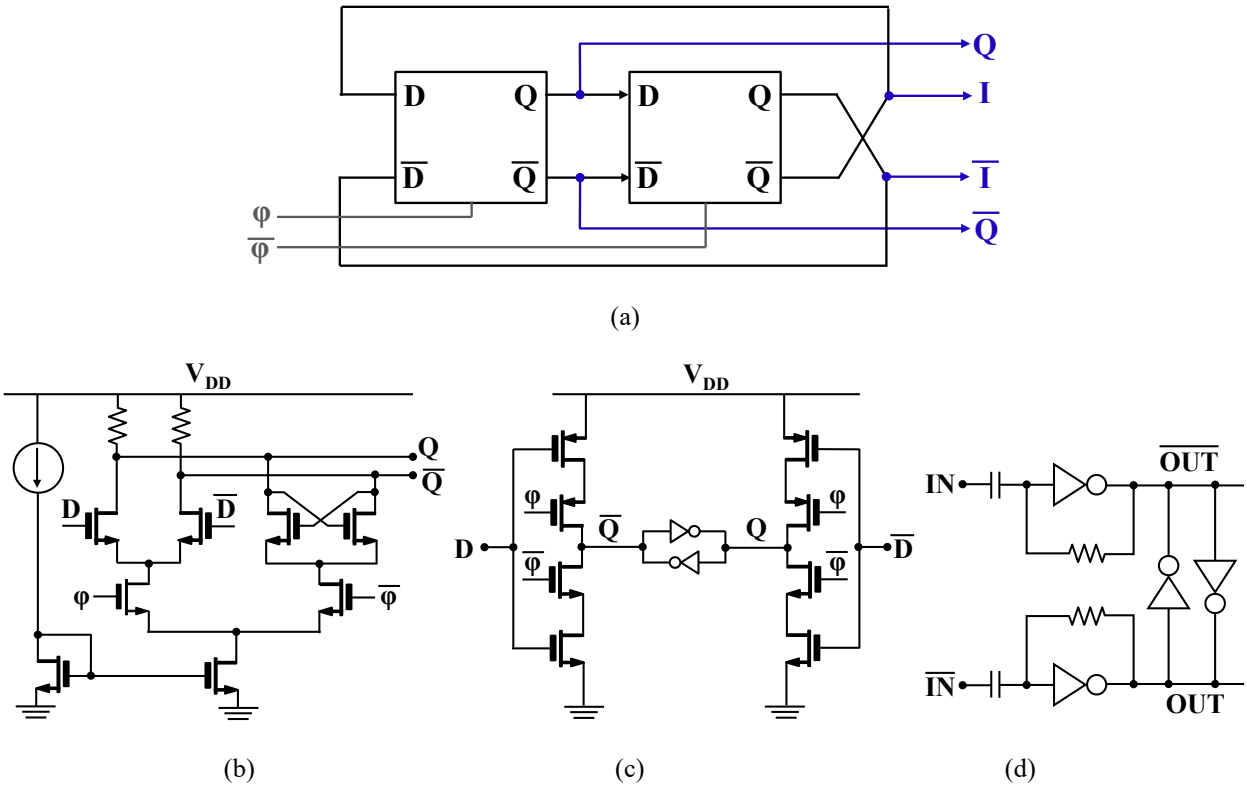
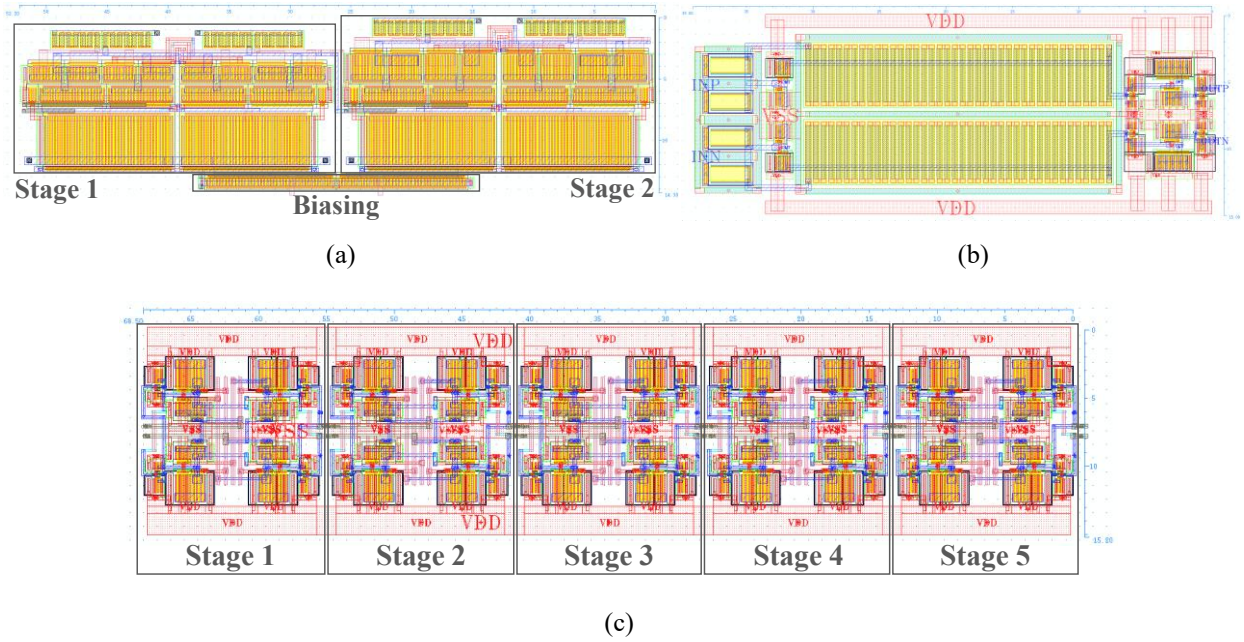


Fig. 2.23. (a) The master-slave divide-by-2 circuit. (b) The CML latch schematic. (c) The C^{2}MOS Latch schematic. (d) The CML-to-CMOS schematic.

5-stage master-slave Clocked-CMOS (C^{2}MOS) divide-by-2 [68]. The CML divider is adequate for high frequency operation where it takes the 28 GHz output of the phase mixer and performs divide-by-4 by cascading two divide-by-2 circuits. The 7 GHz CML divider output is then introduced to a CML-to-CMOS circuit to achieve rail-to-rail swing. For low power operation, the rest of the divider chain is implemented using C^{2}MOS divider where a divide-by-32 is performed by cascading five divide-by-2 circuits. The block diagram of the master-slave divide-by-2 circuit is illustrated in Fig. 2.23(a) utilizing two D-latches where for CML divider a CML latch is used



(a) (b)

(c)

Fig. 2.24. The Divide-by-128 circuit layout. (a) The Divide-by-4 CML divider layout. (b) The CML-to-CMOS circuit layout latch. (c) The Divide-by-32 C^{2}MOS divider layout.

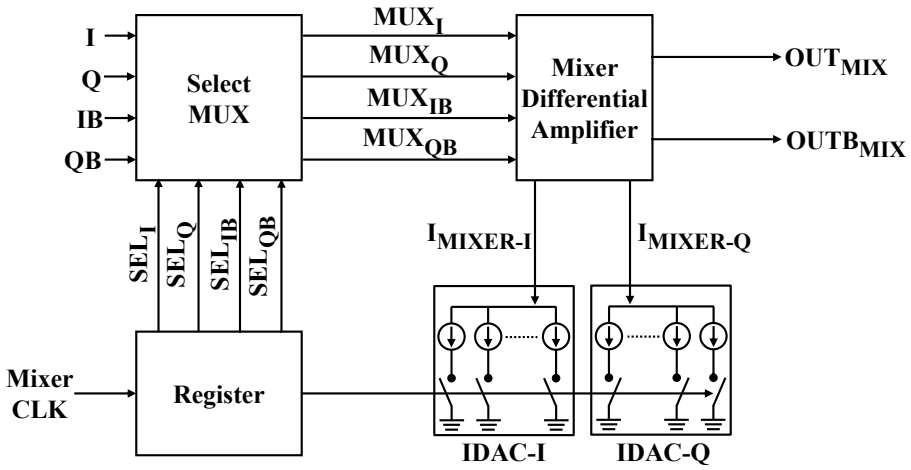


Fig. 2.25. The block diagram of the phase mixer.

(shown in Fig. 2.23(b)) while for C^{2}MOS divider a C^{2}MOS latch is employed (shown in Fig. 2.23(c)). The schematic of the CML-to-CMOS is shown in Fig. 2.23(d). The layouts of the CML divider, CML-to-CMOS, and C^{2}MOS divider are shown in Fig. 2.24 occupying area of 52.2 µm × 14.3 µm, 39 µm × 15 µm, and 68.5 µm × 15.2 µm, respectively.

2.4.2.4 The Phase Mixer Implementation and Operation

Conventionally, dual modulus dividers are used for the fractional division but they suffer from high quantization noise that degrades the phase noise performance of the fractional-N mode

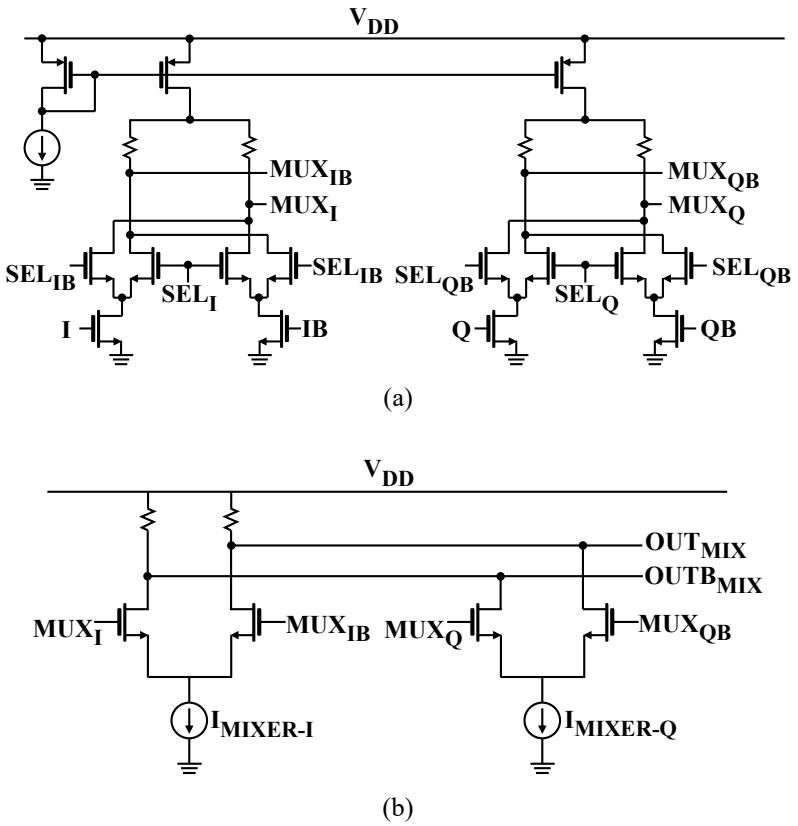


Fig. 2.26. (a) The Select MUX Schematic. (b) The Mixer Amplifier Schematic.

compared to that of the integer-N mode. In [69] a second order noise shaping ΣΔ modulator is combined with a digital-to-analog converter (DAC) cancellation path that reduces the noise at the loop filter node. However, this technique is limited by the DAC resolution and linearity. Another way to improve the quantization noise is to use a multi-phase fractional divider [70]–[78]. As can be concluded from (2.52), the more the number of phases, the lower the quantization noise level.

This work proposes a phase mixing technique that provides 256 phase steps by simply interpolating between the quadrature phases readily available at the 28 GHz VCO output. The block diagram of the phase mixer is illustrated in Fig. 2.25 comprising a select MUX followed by a Mixer differential amplifier whose tail current is supplied through a thermometric current-DAC (IDAC). The schematics of the Select MUX and Mixer Amplifier are illustrated in Fig. 2.26(a) and Fig. 2.26(b), respectively. Phase interpolation within the mixer is performed by varying the weighting factors for the in-phase and quadrature signals each mixer clock cycle. To avoid the complexity of sinusoidal weighting, weighting is performed in a linear manner where the mixer devices are sized for optimal DNL. Different weighting factors are assigned to the *I*

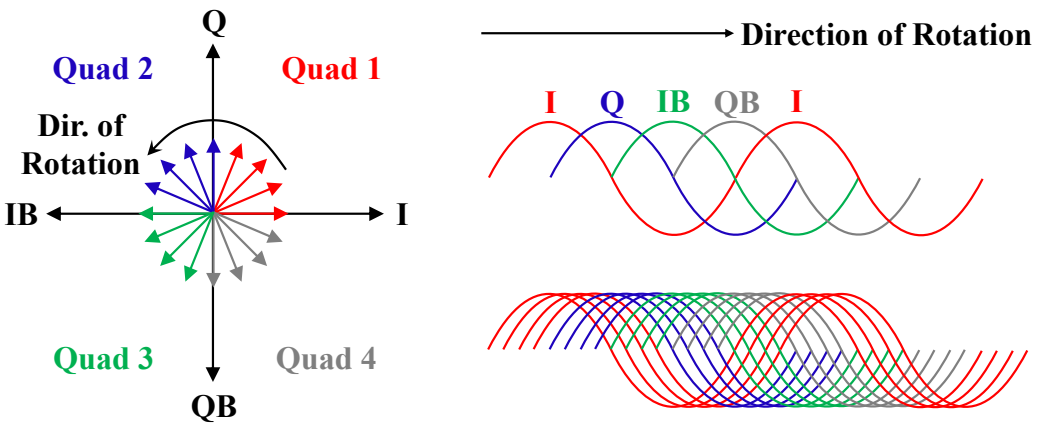


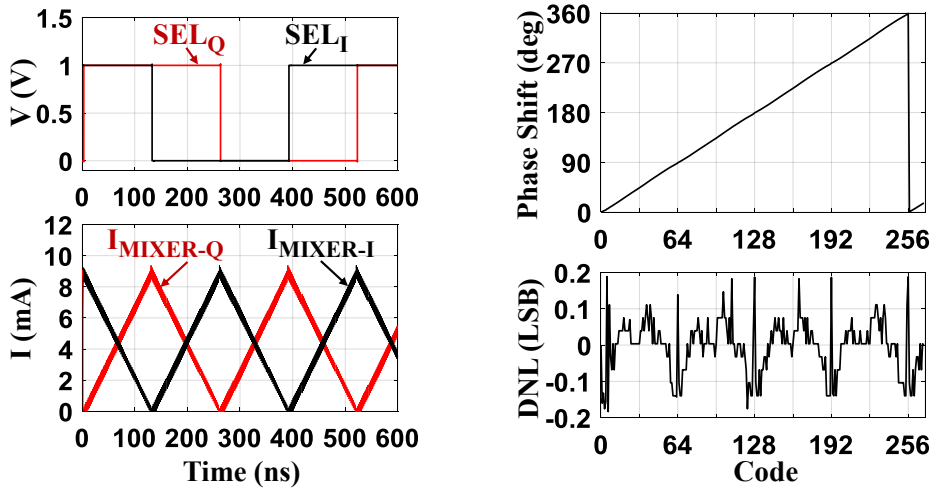
Fig. 2.27. Phasor diagram describing phase interpolation in the phase mixer.

and *Q* signals by controlling the mixer amplifier tail currents $I_{Mixer\text{-}I}$ and $I_{Mixer\text{-}Q}$ through the current DACs, *IDAC-I,* and *IDAC-Q*, respectively. For improved linearity, thermometric current DACs are employed. To reduce the complexity of the thermometric IDACs and provide enhanced linearity, phase interpolation is carried out per-Quad where Quad switching is performed using the Select MUX which reduces the required IDAC resolution by 2-bits. That is, for the 256-phase mixer, only 6-bit resolution is required from the IDAC instead of 8-bits.

The operation of the phase mixer is described in Fig. 2.27 assuming a 16-phase phase mixer with anti-clockwise rotation direction (*I-Q-IB-QB*). The mixer clock rotates a shift register that provides the thermometric input code to the IDACs and controls the Select MUX responsible for Quad selection. To interpolate the phases in the first Quad, the Select MUX will provide phases *I* and *Q* to the mixer amplifier where during the first mixer clock cycle, the thermometric output code will be *0*. This results in $I_{Mixer\text{-}I}= I_{DAC,max}$ and $I_{Mixer\text{-}Q}=0$ and hence the mixer output will be the same as the *I*-signal, i.e., phase=0, where $I_{DAC,max}$ is the maximum DAC current. Then as the mixer clock progresses, the thermometric code will increase resulting in a linear increase in $I_{Mixer\text{-}Q}$ accompanied by an equivalent linear decrease in $I_{Mixer\text{-}I}$. Consequently, a linear variation in the output phase is attained where the output phase will be 22.5°, 45°, and 67.5° during the 2nd, 3rd and 4th mixer cycles, respectively. Then in the fifth cycle, the Select MUX will change the inputs to the mixer to be *Q* and *IB* to interpolate the phases in the second Quad with $I_{Mixer\text{-}Q}=I_{DAC,max,}$ and $I_{Mixer\text{-}I}=0$, generating the 90° phase and so on. The mixer will finish interpolating all 16-phases after 16 mixer clock cycles with 4 phases interpolated in each Quad and then the process will repeat again. To avoid glitches, the switching from one Quad to the

Table 2.2
Quad Switching in the Phase Mixer

Quad	SEL_I	SEL_Q	MUX_I	MUX_{IB}	MUX_Q	MUX_{QB}
1	1	1	I	IB	Q	QB
2	0	1	IB	I	Q	QB
3	0	0	IB	I	QB	Q
4	1	0	I	IB	QB	Q



(a) (b)

Fig. 2.28. Post Layout Simulation of the 256-phase phase mixer in 65 nm CMOS process. (a) SEL_I, SEL_Q and IDAC currents variation over the four Quads. (b) The mixer transfer characteristics and DNL plot.

next should only involve one signal switching as illustrated in Table 2.2. For example, switching from the first to the second Quad will be accomplished by changing MUX_I from *I* to *IB* while MUX_Q kept unchanged. Fig. 2.28 provides the post-layout simulation results of the 256-phase mixer rotated with a 230 MHz clock where the SEL_I and SEL_Q signals over different Quads and the corresponding in-phase and quadrature DAC currents are shown together with the transfer characteristics and DNL plot of the mixer output achieving maximum DNL of 0.18 LSB.

Performing the phase shift every clock cycle in the direction illustrated in Fig. 2.27 is equivalent to a fractional increase in the period, hence resulting in a fractional decrease in the output frequency. To quantify the amount of fractional frequency deviation due to phase mixing, assume the mixer is rotated using the reference clock while performing 2^L phase steps per VCO cycle with the phase rotator shifting 2^P-*1* phase steps per mixer cycle. Fig. 2.29 shows the frequency deviation due to phase mixing assuming 2^L=*16* phase steps within the VCO period with the rotator taking single (2^P-*1*=*1*) phase step per mixer cycle for exact fraction mode. In

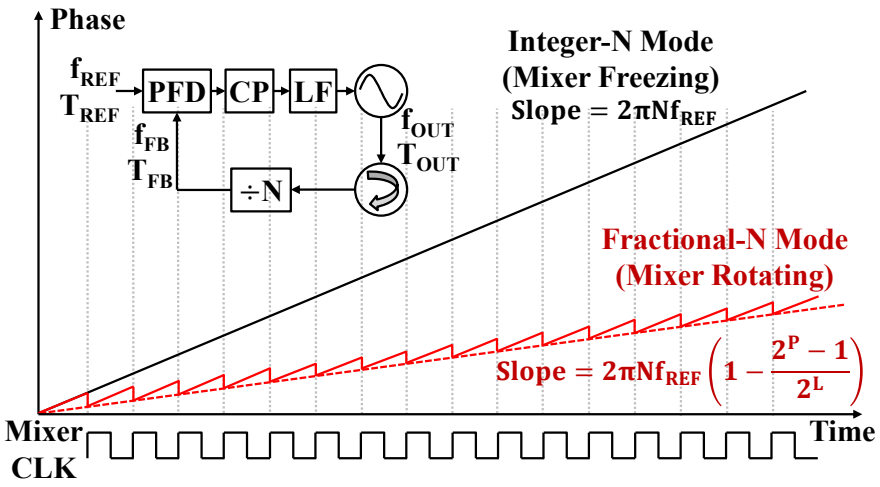


Fig. 2.29. Frequency deviation due to phase mixing operation.

integer-N mode (freezing the phase mixer), the PLL output frequency is $f_{OUT} = Nf_{REF}$ with the output sinusoid given as

$$V_{OUT,integer} = A\sin(2\pi f_{OUT}t) = A\sin(2\pi N f_{REF}t) \tag{2.53}$$

Plotting the sinusoidal output phase versus time (the black line) yields a straight line with *slope* $= 2\pi f_{OUT} = 2\pi N f_{REF}$. In the fractional mode where the mixer is allowed to rotate, the mixer takes the VCO output and performs constant phase shift every mixer clock cycle. The value of the phase shift is dictated by the chosen values of L and P. This results in modulating the average output frequency. To get an expression for the output frequency, we start by the locking condition where the feedback period (T_{FB}) is equal to the reference period (T_{REF})

$$T_{FB} = T_{REF} \tag{2.54}$$

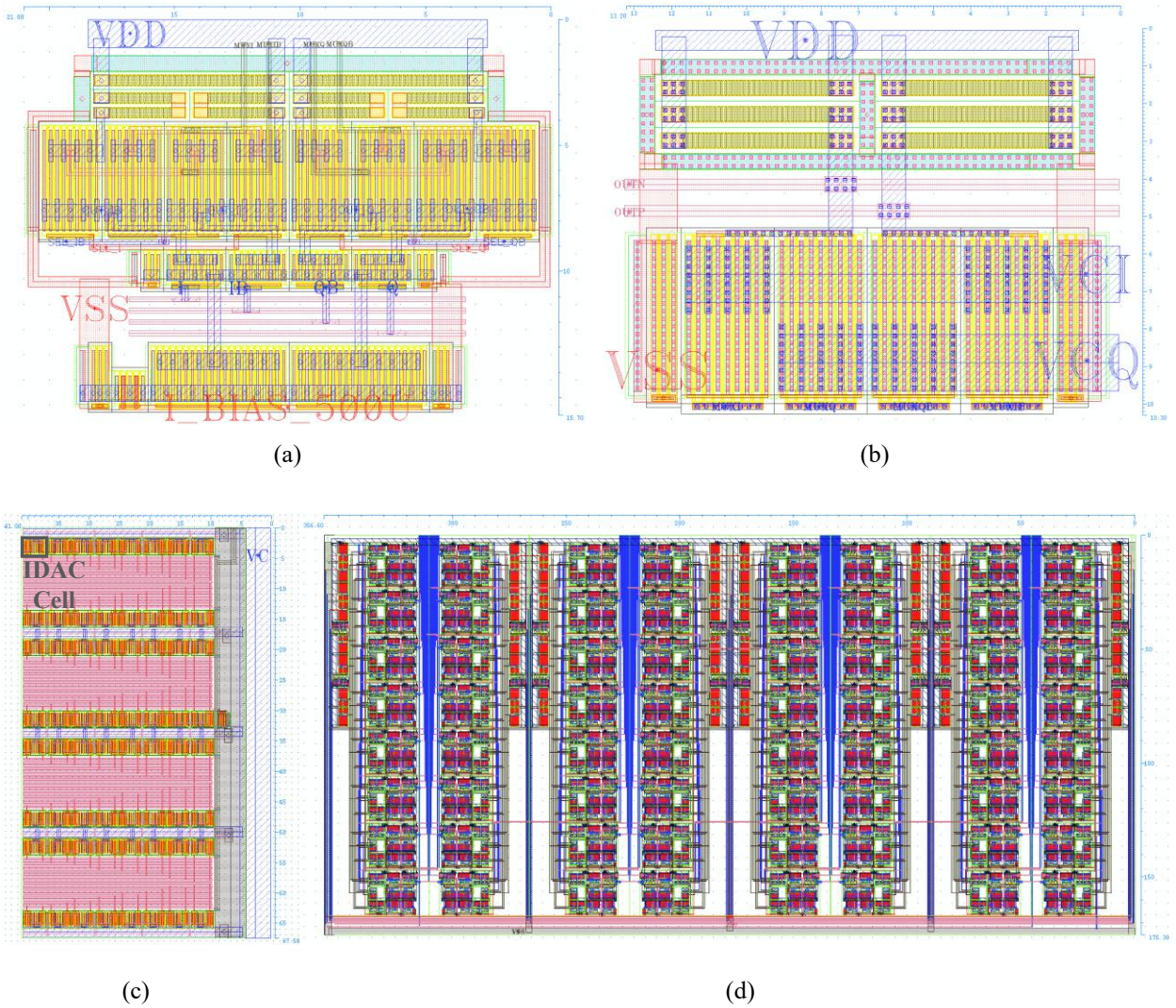
The period of the feedback signal can be written as

$$T_{FB} = NT_{OUT} \pm NT_{OUT}\frac{2^P - 1}{2^L} \tag{2.55}$$

where T_{OUT} is the PLL output period. By substituting (2.54) in (2.55) we get

$$f_{OUT} = f_{REF}N\left(1 \pm \frac{2^P - 1}{2^L}\right) \tag{2.56}$$

where the '–' sign is for the anti-clockwise phase rotation (*I-Q-IB-QB*) and the '+' sign is for clockwise phase rotation (*I-QB-IB-Q*). The red plot of Fig. 2.29 illustrates the phase versus time plot in the fractional-N mode.



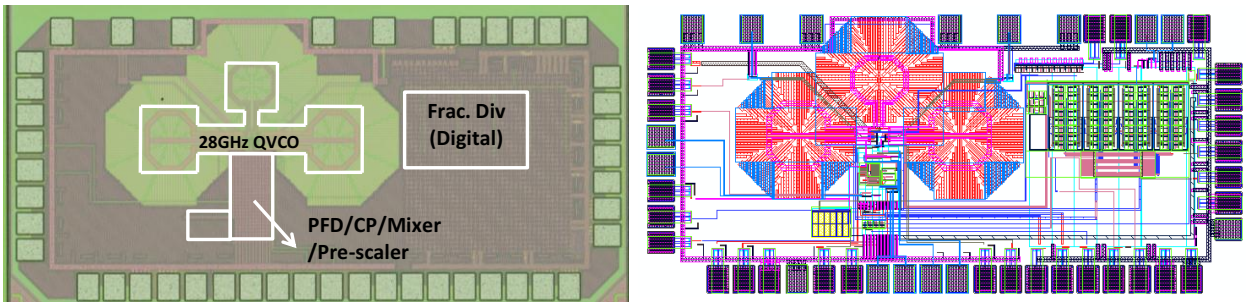
(a) (b)

(c) (d)

Fig. 2.30. The Phase mixer layout. (a) The Select MUX layout. (b) The Mixer differential amplifier layout. (c) The IDAC layout. (b) The Register layout.

One way to improve fractional resolution is by employing dithering through ΣΔ modulation; however, this will result in higher phase noise compared to the exact fraction case that is employed in this work. Another way – that is employed in the proposed exact fraction design – is to use a higher number of phases (in our case 256 phases were utilized). The resolution can be further improved by having separate clocks for the reference and the mixer where different clock frequencies can be applied to the mixer to control the fractional resolution given as $f_{Mixer}/256$ for the employed 256-phase mixer.

The layouts of the Select MUX, Mixer differential amplifier, IDAC and Register are illustrated in Fig. 2.30 occupying areas of 21 µm × 15.7 µm, 13.2 µm × 10.3 µm, 41 µm × 67.58 µm, and 356.6 µm × 175.3 µm, respectively.



(a) (b)

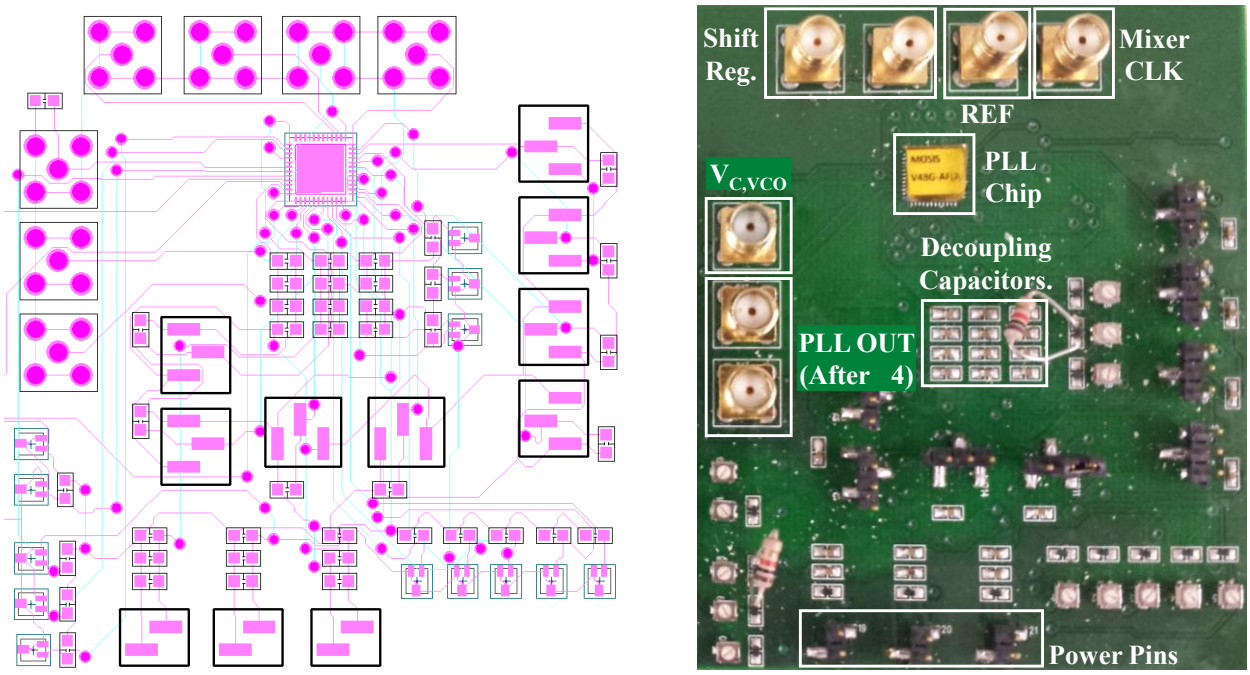
Fig. 2.31. The fabricated 28 GHz single stage fractional-N frequency synthesizer prototype. (a) Die micrograph. (b) The complete chip layout.

Table 2.3
Power and Area Breakdown for the 28 GHz Single Stage Fractional-N Synthesizer

	Power (mW)	**Area (μm^2)**
PFD	2	46 × 37.5
CP	1	51.7 × 53.7
28 GHz Quadrature VCO	10.13	724.5 × 458.9
Phase Mixer	8	435 × 270
CML Divider	13.4	52.2 × 14.3
CML-to-CMOS	0.6	39 × 15
C^{2}MOS Divider	0.672	68.5 × 15.2

2.4.3 Measurement Results of the Single Stage 28 GHz Fractional-N Synthesizer

A single stage 28 GHz fractional-N synthesizer prototype was fabricated in the TSMC 65 nm CMOS process. The die micrograph of the fabricated prototype is illustrated in Fig. 2.31 occupying an active area of 0.18 mm^2. The single stage PLL consumes a total of 35.8 mW from 1 V supply. The power and area breakdown of the fabricated prototype is provided in Table 2.3. A two-layer FR-4 PCB was designed for testing the fabricated packaged die as illustrated in Fig. 2.32. Each of the analog VDD, the digital VDD and the VCO's VDD are tied to four off-chip 10 μF decoupling capacitors. For testing the fabricated prototype, a 230 MHz reference clock was employed. In order to be able to test the QFN packaged dies, a divide-by-4 output of the 28 GHz synthesizer was observed in the measurements. The measured phase noise of the free running 28 GHz VCO and the locked 28 GHz synthesizer in both integer-N and fractional-N modes after divide-by-4 are illustrated in Fig. 2.33. For the fractional-N phase noise plots, a fractional spur can be observed at 90 MHz owing to applying a 90 MHz mixer clock for rotating the mixer. The single stage PLL (after divide-by-4) in the integer-N and fractional-N modes

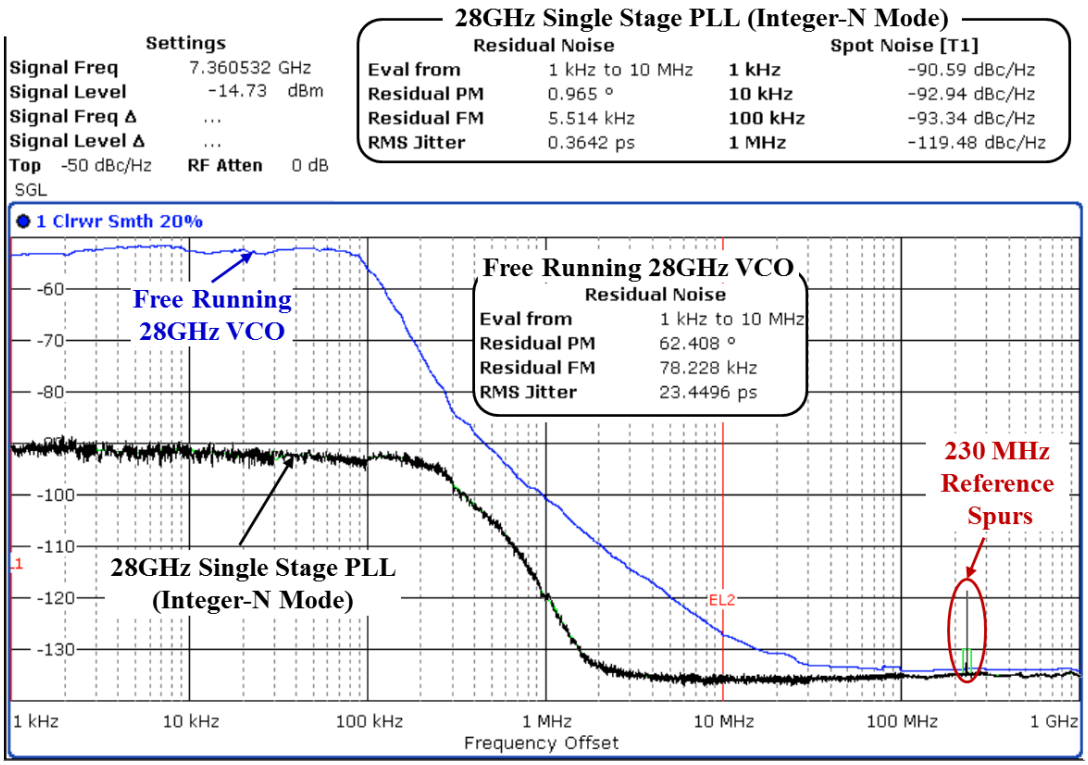


(a) (b)

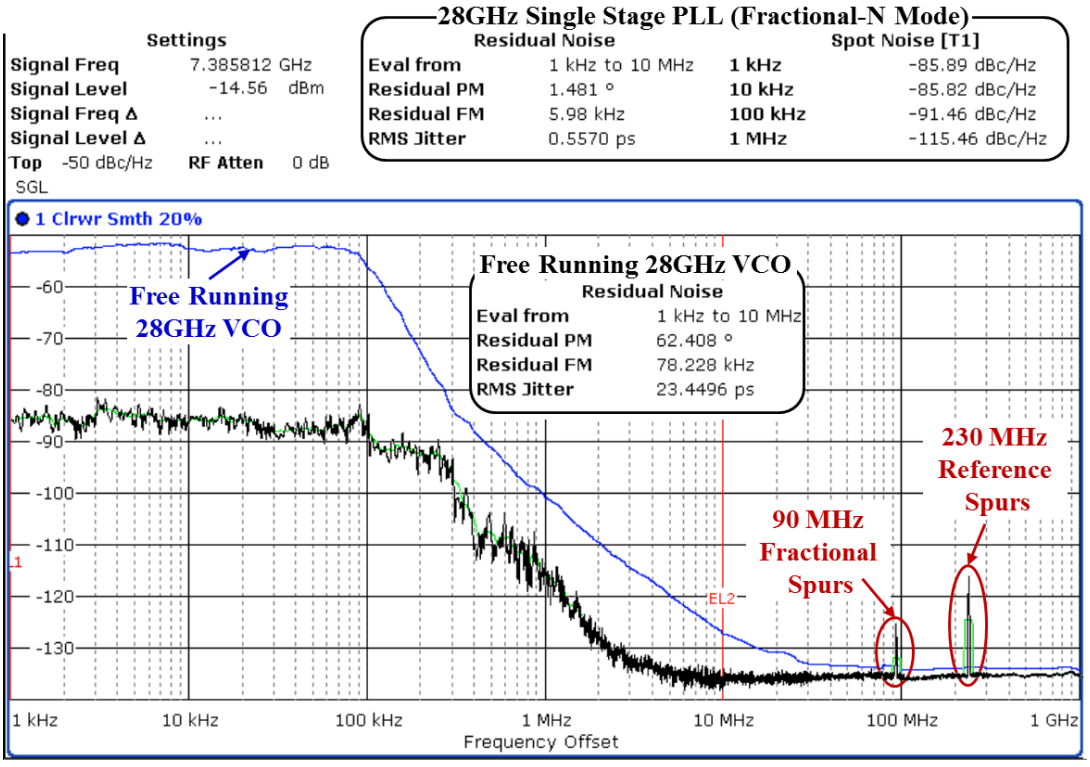
Fig. 2.32. Testing PCB board for the single stage 28 GHz synthesizer. (a) PCB layout. (b) PCB with the fabricated chip mounted.

achieves a 1 MHz offset phase noise of –119.48 and –115.46 dBc/Hz, respectively that translates to –107.48 and –103.46 dBc/Hz at 28 GHz.

The locked spectrum of the synthesizer in the fractional-N mode after divide-by-4 is illustrated in Fig. 2.34 where the fractional division is attained using a 100 MHz mixer clock achieving reference spurs less than –56.56 dBc and fractional spurs less than –75.18 dBc. Fig. 2.35 shows the measured locked spectrum of the cascaded PLL after divide-by-4 for integer-N and fractional-N modes with different mixer clock frequencies for the fractional mode showing fractional resolution of 16 kHz and 880 kHz at 5 MHz and 230 MHz mixer clock frequencies, respectively. The measured fractional resolution agrees with the theoretical fractional resolution given as $f_{Mixer}/256$ in case of the 256-phase mixer. Note that the fractional resolution is taken as 4× the frequency separation between the integer-N and fractional-N tones since the output is observed on the analyzer after divide-by-4. Fig. 2.36 shows the phase noise at 1 MHz offset of the single-stage PLL over the PLL's tuning range (26.2-32.4 GHz) for the integer-N and fractional-N modes. The designed single-stage PLL achieves good performance with respect to phase noise, jitter, reference/fractional spurs, fractional resolution, and power consumption.



(a)



(b)

Fig. 2.33. Measured phase noise of the fabricated 28 GHz single stage synthesizer. (a) Integer-N mode. (b) Fractional-N mode.

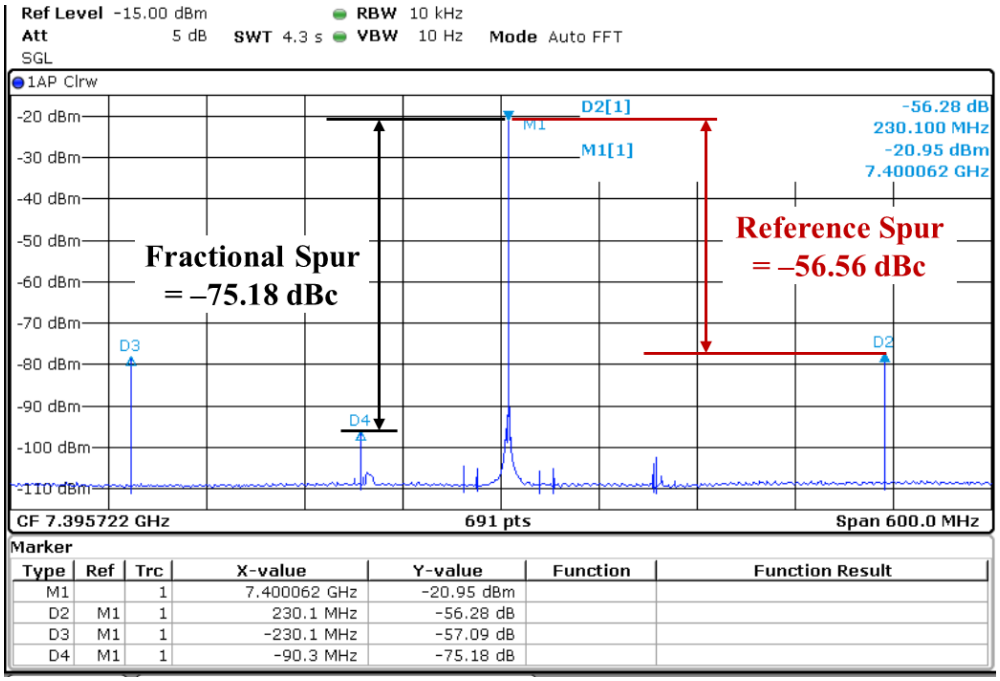


Fig. 2.34. The Measured Spurious content of the locked 28 GHz single stage synthesizer after divide-by-4.

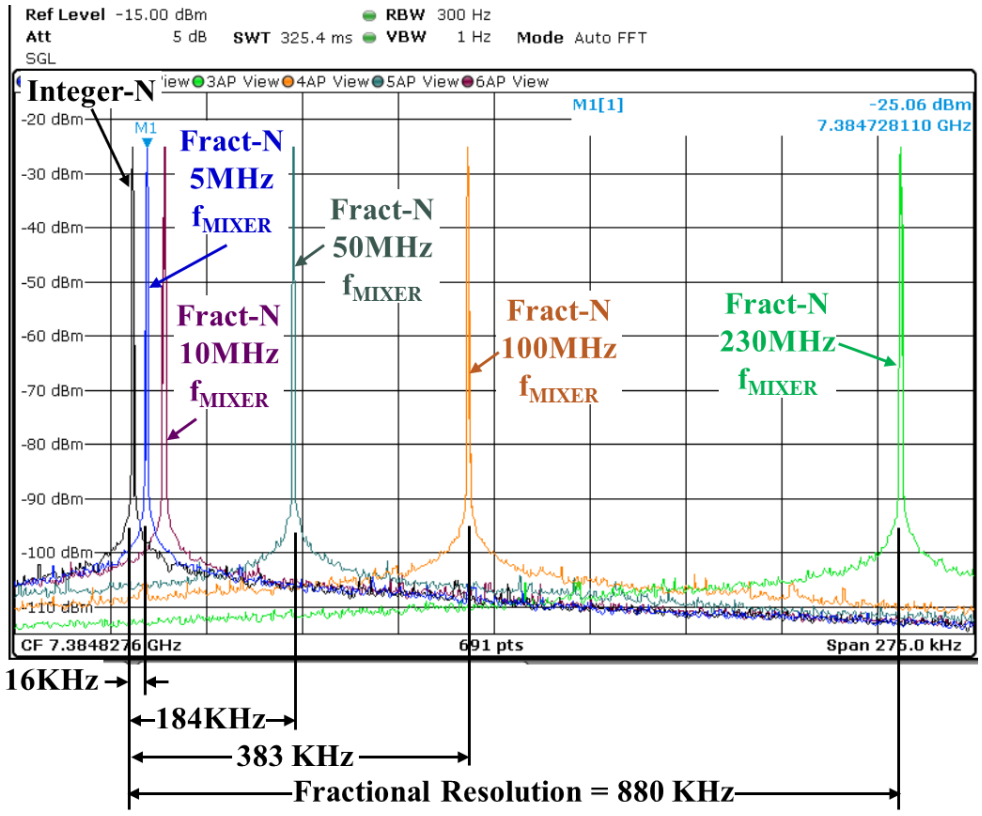


Fig. 2.35. The Measured locked spectrum of the 28 GHz single stage PLL (after divide-by-4) for the integer-N and fractional-N modes showing the fractional resolution at different mixer clock frequencies.

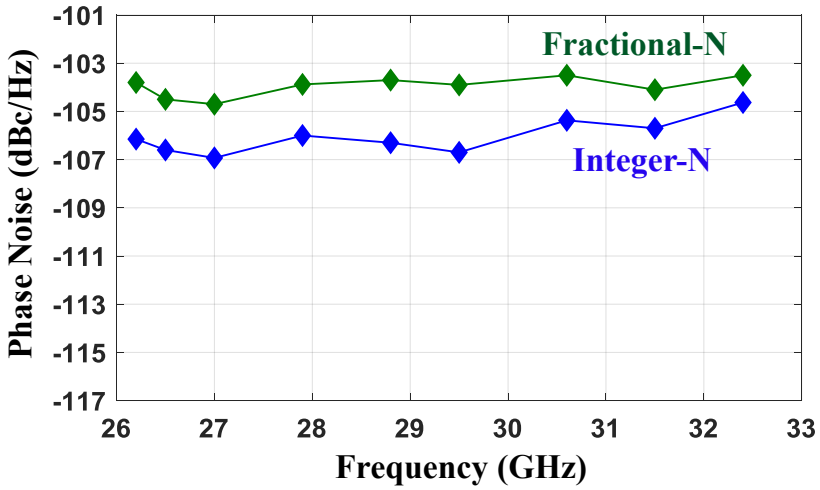


Fig. 2.36. Measured Single-stage PLL Phase Noise at 1MHz offset over the PLL Tuning Range.

2.5 Conclusion

A 28 GHz quadrature single stage fractional-N frequency synthesizer implemented as a CPPLL was presented. The proposed synthesizer employs phase mixing for fractional division achieving good performance with 500 fs integrated jitter.

It can be noted that the jitter performance of the single stage PLL is limited by the challenging tradeoff in choosing the PLL loop bandwidth for the single-stage PLL, where low bandwidth results in lower reference and fractional noise while high bandwidth filters more of the VCO phase noise. A Cascaded PLL can provide a viable solution to overcome this trade-off and achieve enhanced jitter performance by breaking the PLL into two stages as will be discussed in the next Chapter.

3. THE CASCADED FRACTIONAL-N FREQUENCY SYNTHESIZER

In this chapter, the 28 GHz fractional-N cascaded PLL will be discussed. The performance improvement of the cascaded phase-locked loop (PLL) over single-stage PLL in terms of jitter and power consumption is theoretically presented and verified with measured results. First, the limitations of the single stage PLL will be pointed out.

3.1 Limitations of the Single Stage PLL

Millimeter-wave single stage PLL jitter performance is limited by the inflexible tradeoff between higher phase noise of the local VCO and the large amplification of the reference clock phase noise. This can be explained as follows. First, a large frequency multiplication factor is required to lock the mm-Wave VCO output to a MHz range reference clock resulting in large amplification of the reference phase noise. Second, wide tuning range CMOS LC VCOs operating at high mm-Wave frequencies suffer from degraded phase noise performance Fig. ℨ.1(a) shows the schematic of a conventional differential LC VCO. The simulated phase noise performance of the 10% tuning range 28 GHz differential VCO in 65 nm CMOS process is shown in Fig. ℨ.1(c) achieving -100 dBc/Hz phase noise at 1 MHz offset. The 5G transceivers will not only need the synthesizer to have wide tuning range but also it is required to be quadrature. This justifies the use of a quadrature VCO. The schematic of a conventional quadrature VCO is shown in Fig. ℨ.1(b). Since quadrature oscillation happens at a frequency offset from resonance, tank quality factor is lower compared to its differential counterpart, and as a result, exhibits higher phase noise. This explains the -90 dBc/Hz phase noise at 1 MHz offset from the quadrature 28 GHz VCO shown in Fig. ℨ.1(c). This raises a challenging trade-off in choosing the PLL's loop bandwidth for the single-stage PLL, where low bandwidth results in lower reference noise while high bandwidth filters more of the VCO phase noise. The case becomes more severe in the fractional-N mode where the fractional noise comes into act. One possible solution is to implement the VCO in GaAs or InGaP processes for improved VCO phase noise [79]. However, this does not provide a fully integrated CMOS solution. Cascaded PLL can

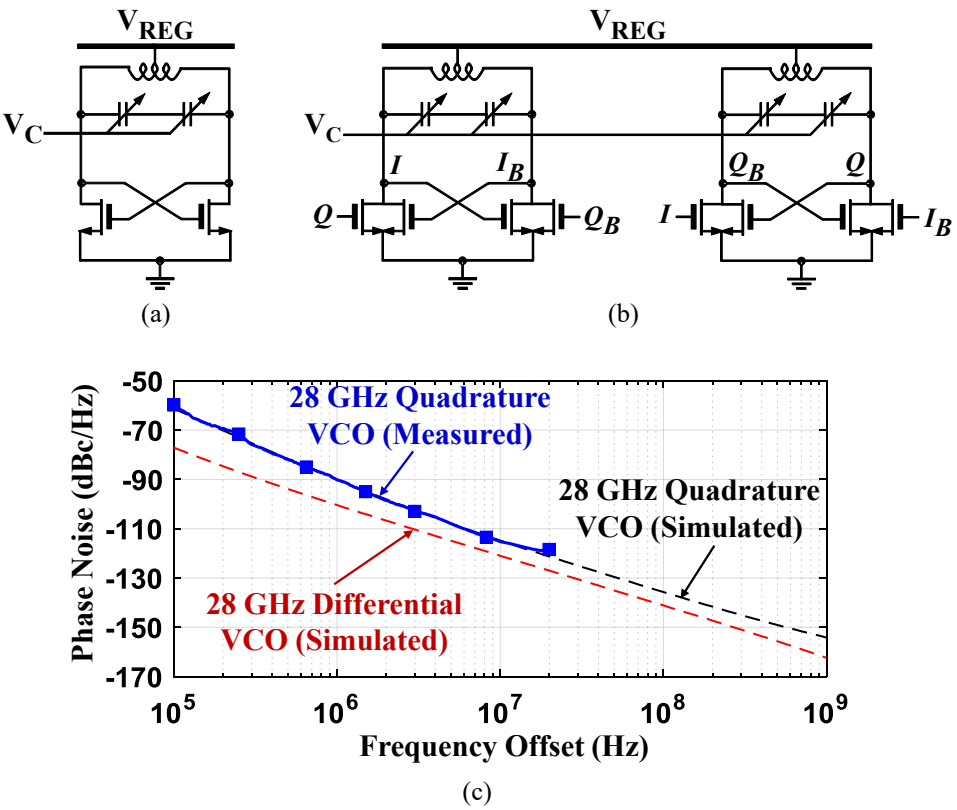


Fig. 3.1. (a) Differential LC VCO Schematic. (b) Quadrature LC VCO Schematic. (c) The 28 GHz Differential and Quadrature LC VCOs Post Layout Simulated / Measured Phase noise in 65 nm CMOS process.

provide a viable solution to overcome the required jitter challenges at mm-Wave frequencies using standard bulk CMOS process.

3.2 Literature Review of Cascaded PLL Architectures

Several combinations of fractional-N and integer-N cascaded PLLs are published in the recent literature. In [80] a 2.4 GHz fractional-N cascaded PLL was proposed (shown in Fig. 3.2(a)) where the fractional division is performed outside the PLL at the input. The first stage PLL is used to clean up the fractional spurs keeping the bandwidth very low, 2 kHz only. The second stage PLL is then used to provide the integer multiplication (16×) to provide the 2.4 GHz output. Usually, fractional division in the feedback path allows better frequency resolution. Due to the large multiplication provided by the second PLL, the bandwidth cannot be set optimally high to filter the second VCO's phase noise. Therefore, when VCO phase noise filtering is considered, this architecture does not provide a significant improvement over a single stage PLL.

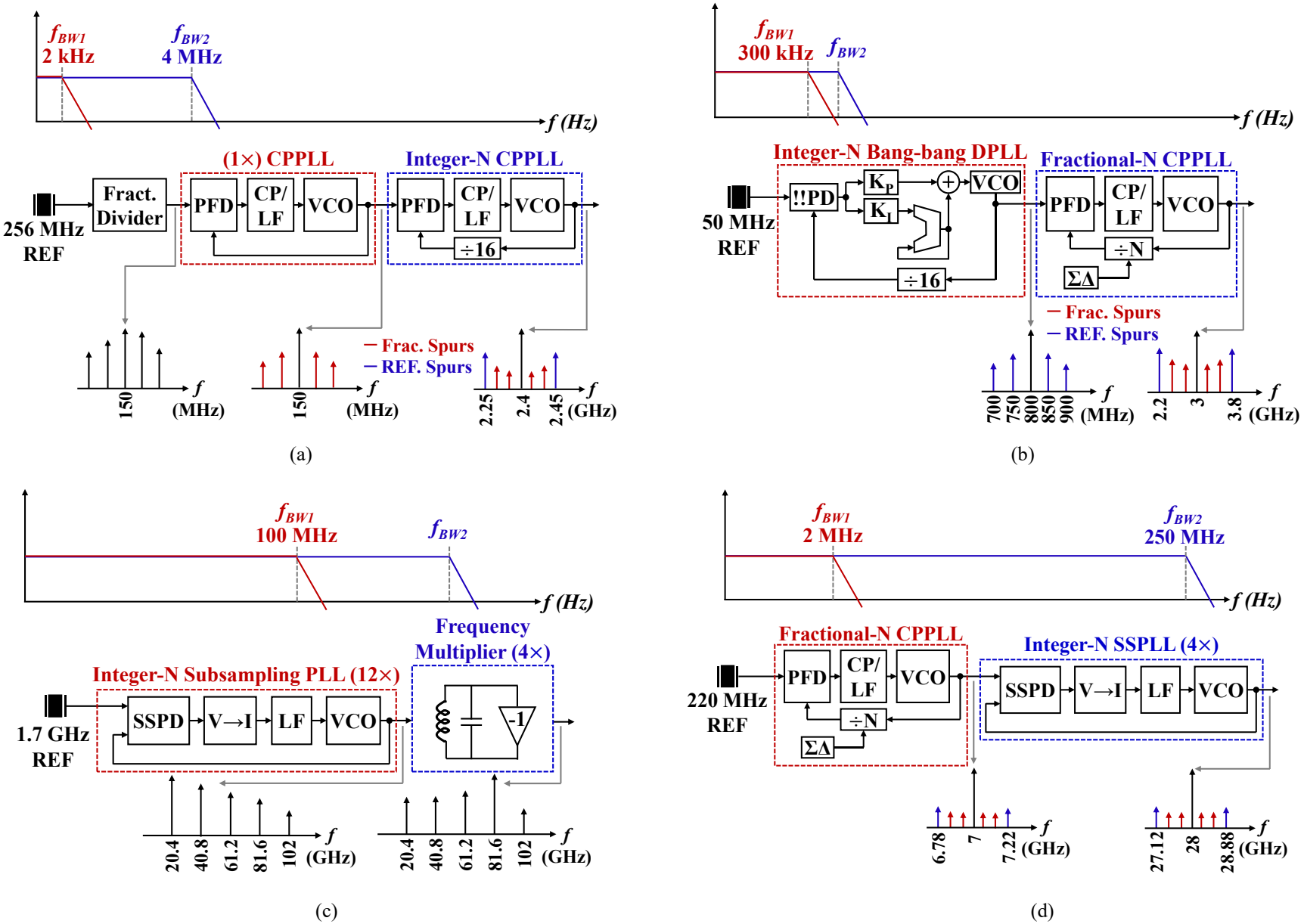


Fig. 3.2. Block diagram of cascaded PLLs previously reported in literature together with the one proposed in this work. (a) PLL in [80]. (b) PLL in [81]. (c) PLL in [82]. (d) The PLL proposed in this work.

In [81] a 3 GHz fractional-N cascaded PLL was implemented employing a first stage integer-N digital bang-bang PLL followed by a second stage fractional-N CPPLL (shown in Fig. 3.2(b)). Having the fractional division in the second stage leads to challenging tradeoff between fractional divider noise and VCO phase noise. In addition to the VCO phase noise, high frequency dividers are also challenging to design and are power hungry.

In [82] requirements for high frequency dividers are avoided using (4×) multiplying injection locked oscillator (ILO), that is injected from a K-band integer-N PLL output (Fig. 3.2(c)). Note that the ILO is locked to the 4^{th} harmonic of the PLL output clock. However, the fundamental tone still appears as frequency spur degrading the receiver performance. While multiplying ILO (MILO) can achieve low phase noise similar to MDLL, its spur performance is a major concern. Unlike PLL, ILO has 1^{st} order jitter transfer characteristics. Therefore, reference spurs are attenuated by a single pole that provides only 20 dB/dec attenuation. Compared to that, PLL can provide better reference spur attenuation due to 2^{nd} order jitter transfer characteristics. Also, the lock range on MILO decreases exponentially with the multiplication factor. In addition, ILOs are open loop system – practically PLL would still be required to provide 4× frequency locking over PVT.

The proposed cascaded PLL is shown in Fig. 3.2(d), comprising a first stage low bandwidth fractional-N CPPLL followed by a second stage wide bandwidth integer-N SSPLL. This combination provides several advantages over previously published cascaded PLLs. First, the low bandwidth of the fractional PLL efficiently filters fractional divider and reference noise whereas the 2^{nd} PLL bandwidth is chosen very high to filter the 28 GHz VCO phase noise. As a result, this architecture eliminates the tradeoff between input noise and VCO phase noise filtering. The low bandwidth of the first stage helped in reducing the reference and fractional spurs. The reference spurs were further reduced by implementing the charge-pump of the first stage using long channel devices and employing an error amplifier which reduced the mismatch within the CP. This resulted in reduced CP duty cycle error in the locked state and hence lowering the CP phase noise and reference spurs significantly. To further lower the fractional spurs, a high-resolution 256-phase phase mixer was employed for the fractional division. Having the second stage as a SSPLL with high frequency reference clock eliminates the need for high frequency dividers which significantly reduces the power consumption. Also, the absence of the feedback divider in the SSPLL results in the sample-and-hold phase detector (SHPD) and

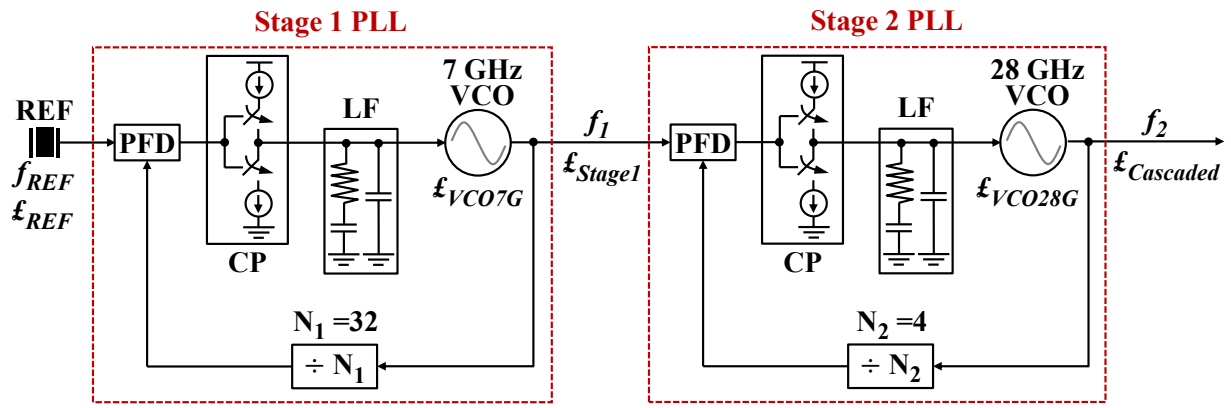
voltage-to-current converter (V→I) noise not being amplified by N^2 hence improving the jitter and phase noise performance of the PLL [83]. In addition to that, by appropriately choosing the first LC VCO frequency and phase noise, it is possible to optimize the overall cascaded PLL phase noise and get improved performance. Cascaded PLL has the potential for injection pulling especially if the second PLL is fractional-N where it is possible for two LC VCOs that are 100 ppm apart to pull each other. Fortunately, in this case, the two LC VCOs are related by an integer multiple, where their pulling concern is greatly reduced. All the above factors allowed the proposed cascaded PLL to provide low reference and fractional spurs, improved jitter performance and low power consumption making it a suitable candidate for 5G transceivers. Detailed analysis of the phase noise optimization for the cascaded PLL will be discussed in the next section.

3.3 Cascaded PLL Analysis and Design Perspectives

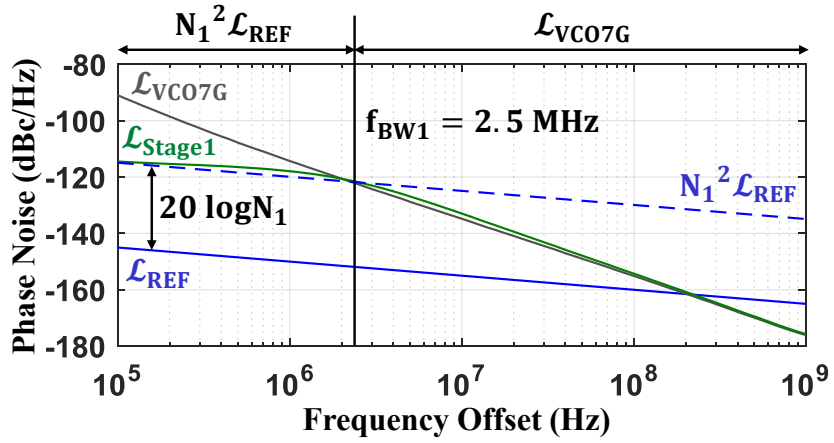
Theoretical analysis of the cascaded PLL phase noise was presented in [84] and showed the conditions under which the cascaded PLL is advantageous over the single stage PLL. Since the focus of [84] was wireline communications, fractional-N modes were not considered. This work shows that the benefit of the cascaded PLL is more prominent when fractional-N modes are considered. In addition, the phase noise benefit of the cascaded PLL can be maximized by optimally distributing the multiplication ratio over the two PLLs. However, to realize the theoretical benefits of cascaded PLL, we need to overcome implementation challenges such as high frequency phase frequency detector (PFD). This work addresses those implementation challenges and demonstrates the benefits of cascaded PLL over single stage PLL through measured results from implemented prototypes in the 65 nm CMOS process.

3.3.1 The Cascaded 28 GHz Integer-N Synthesizer

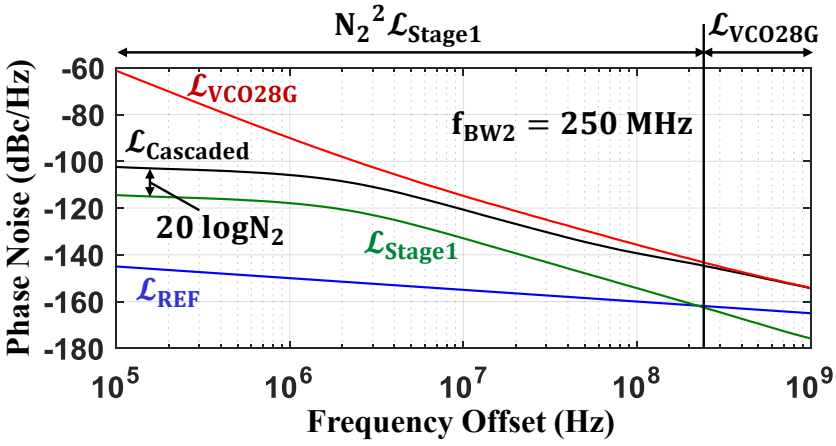
The cascaded PLL is analyzed assuming a first stage 7 GHz PLL whose output is applied as a reference to the second stage 28 GHz PLL as illustrated in Fig. 3.3(a). The first and second stage PLLs provide frequency multiplication of N_1 and N_2, respectively, where the product of N_1 and N_2 is equal to the overall frequency multiplication factor of the single-stage PLL $N=N_1 \times N_2$. Let the first stage 7 GHz VCO phase noise be denoted as $£_{VCO7G}$, the first stage PLL output phase noise as $£_{Stage1}$ and the second stage PLL output phase noise as $£_{Cascaded}$. The loop bandwidth of



(a)



(b)



(c)

Fig. 3.3. The Cascaded Integer-N 28 GHz PLL. (a) Block diagram. (b) The first stage phase noise performance. (c) The second stage phase noise performance.

the first stage PLL is designed for optimal jitter performance based on equations (2.50) and (2.51) resulting in loop bandwidth of f_{BW1} = 2.5 MHz as illustrated in Fig. 3.3(b). It can be noted that the first stage PLL loop bandwidth is much lower than that of the single stage PLL (found to

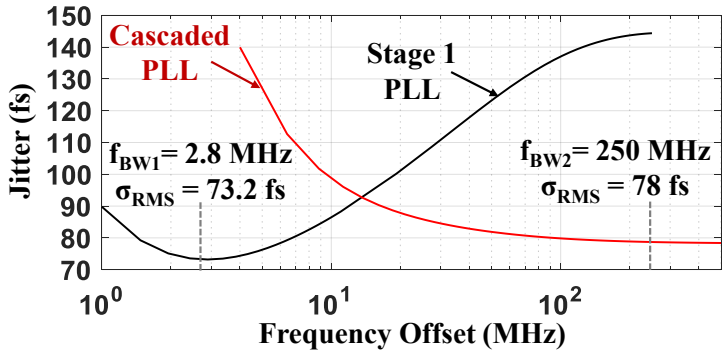


Fig. 3.4. Simulated Jitter versus PLL loop bandwidth for the Stage 1 and Stage 2 of the cascaded PLL.

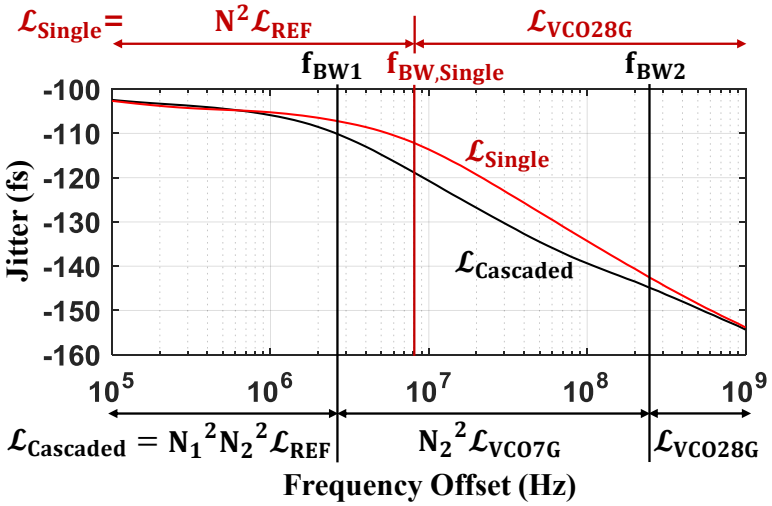


Fig. 3.5. Cascaded PLL versus Single-stage PLL phase noise performance.

be 8 MHz as shown in Chapter 2) resulting in filtering more of the reference noise. The locked 7 GHz output of the first stage PLL is used as the reference for the (4×) second stage PLL. The phase noise analysis for the second stage PLL is illustrated in Fig. 3.3(c) where its loop bandwidth (f_{BW2}) is designed similar to that of the first stage PLL resulting in f_{BW2} = 250 MHz. Fig. 3.4 provides the simulated jitter performance versus loop bandwidth for the first and second PLL stages. The optimal loop bandwidth for lowest jitter performance matches our theoretical prediction. The cascaded PLL phase noise can be approximated to three regions as

$$\pounds_{Cascaded} \cong \begin{cases} N_2^2\pounds_{Stage1} = N_1^2N_2^2\pounds_{REF}, & f < f_{BW1} \\ N_2^2\pounds_{Stage1} = N_2^2\pounds_{VCO7G} & f_{BW1} \le f \le f_{BW2} \\ \pounds_{VCO28G}, & f > f_{BW2} \end{cases} \quad (3.1)$$

The phase noise performance of the cascaded PLL versus that of the single-stage PLL is shown in Fig. 3.5. From which it can be concluded that at offset frequencies lower than f_{BW1}, both the

single-stage and cascaded PLLs have the same phase noise performance of $N^2£_{REF}=N_1^2N_2^2£_{REF}$. Similarly, for offset frequency higher than f_{BW2}, the phase noise of both the cascaded and single-stage PLLs are the same and equal to the second stage 28 GHz VCO phase noise $£_{VCO28G}$. The improvement in the phase noise of the cascaded PLL over that of the single-stage PLL is pronounced in the frequency offset range between f_{BW1} and f_{BW2}. Hence, to improve the phase noise performance of the cascaded PLL, the optimization should be performed in the region $f_{BW1}<f<f_{BW2}$.

3.3.2 Cascaded PLL Phase Noise Optimization

The proper choice of the optimal loop bandwidth of the two stages of the cascaded PLL is critical for the cascaded PLL to have improved performance over the single stage PLL. But that is not the only key to designing the cascaded PLL. As pointed out in [84] not always will the cascaded PLL be able to provide improved performance over its single stage counterpart, it depends on the VCO phase noise performance of the 1st and 2nd stage PLLs. Based on the VCO phase noise trend we choose the first stage PLL frequency f_1 that also dictates the frequency multiplication factors of the first and second stage PLLs N_1 and N_2. Before discussing the choice of the first stage PLL frequency, we need first to study the behavior of the LC VCO phase noise as oscillation frequency increases. For a VCO with parallel LC tank, the oscillation frequency (w_{osc}) and quality factor (Q_{tank}) are given as [85]

$$w_{osc} = {}^{1}/_{\sqrt{L \times C}} \tag{3.2}$$

$$Q_{tank} = \frac{1}{{}^{1}/_{Q_L} + {}^{1}/_{Q_C}} = \frac{1}{R_S}\sqrt{\frac{L}{C}} \tag{3.3}$$

where R_S is the series parasitic resistance of the inductor, Q_L is the inductor quality factor and Q_C is the varactor quality factor. From (3.2) we conclude that the $L\times C$ product scales inversely with the oscillation frequency. If a 10% VCO tuning range is to be maintained as we go higher in frequency, then the varactor capacitance C should increase with frequency resulting in degraded Q_C where a trade-off exists between the VCO phase noise and its tuning range [86]. This results in using lower inductance L with higher R_S. And since in mm-Wave frequency range, Q_L starts to saturate, then the overall tank quality factor would be greatly influenced by Q_C. Hence, the overall tank quality factor will degrade at higher frequencies due to lower Q_C resulting in

Table 3.1
Design Parameters for Fabricated VCO Prototypes

	7 GHz VCO	10 GHz VCO	15 GHz VCO
Cross Coupled $(W/L)_{CROSS}$	10 µm/240 nm	16 µm/240 nm	20 µm/240 nm
Inductor (L)	4 nH	1.5 nH	600 pH
Varactor $(W/L)_{VAR}$	11 µm/60 nm	15 µm/60 nm	20 µm/60 nm

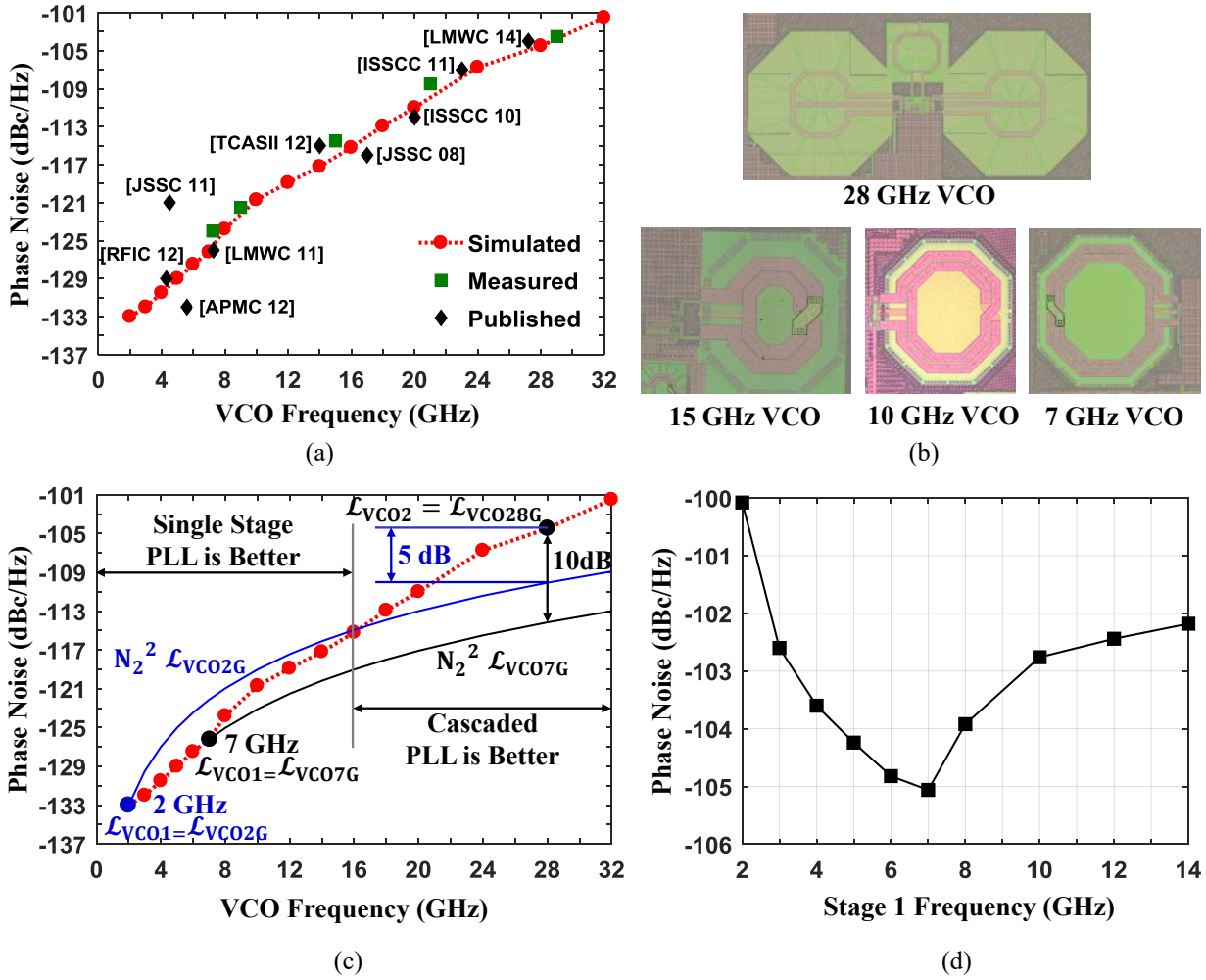


Fig. 3.6. The Cascaded PLL design perspectives. (a) Simulated/Measured/Published VCO Phase Noise Trend in 65 nm CMOS Process at 10 MHz offset. (b) Die micrograph of implemented VCOs in 65 nm CMOS process. (c) Cascaded PLL versus single stage PLL phase noise performance at different first stage PLL frequencies. (d) Simulated cascaded PLL phase noise at 10 MHz offset for different first stage PLL frequencies.

degraded VCO phase noise. Moreover, tank losses increase with frequency which requires higher transconductance to meet the oscillation condition resulting in higher flicker and thermal noise from the MOSFETs. Fig. 3.6(a) illustrates the VCO phase noise trend with the oscillation frequency in the 65 nm CMOS process where the simulated VCO phase noise at 10 MHz offset is plotted versus oscillation frequency. The provided plot is not a general plot; it is applicable to

the given 65 nm CMOS process considering 10% VCO tuning range and reasonable power budget. However, this still enables a general procedure to optimize cascaded PLL phase noise. The VCOs are designed based on the structures shown in Fig. 3.1 and are operated from 0.5 V supply. Also, the simulated trend is populated with previously published work with the required tuning range as well as process. The simulated trend is correlated with previously implemented VCO prototypes operating at 7 GHz, 10 GHz, 15 GHz and 28 GHz whose die micrographs are illustrated in Fig. 3.6(b). The 7 GHz, 10 GHz, and 15 GHz VCOs are differential VCOs based on the schematic illustrated in Fig. 3.1 (a) with their design parameters shown in Table 3.1 where $(W/L)_{CROSS}$ is the aspect ratio of the cross-coupled transistors, L is the inductance of the inductor and $(W/L)_{VAR}$ is the aspect ratio of the MOSCAP used to implement the varactor.

To optimize the cascaded PLL performance, we shall consider the region $f_{BW1} < f < f_{BW2}$ where the performance of the cascaded PLL differs from that of the single stage PLL. In this region, the cascaded PLL phase noise is equal to N_2^2 $£_{VCO1}$ with $N_2=f_2/f_1$ and $£_{VCO1}$ is the first stage VCO phase noise, while the single stage PLL phase noise is approximated as the second stage VCO phase noise $£_{VCO2}$ – for simplicity. As an example, let's assume a 2 GHz first stage PLL where $£_{VCO1}=£_{VCO2G}$ and $£_{VCO2G}$ is the phase noise of the 2 GHz VCO. Fig. 3.6(c) shows a plot of N_2^2 $£_{VCO2G}$ in blue projecting cascaded PLL phase noise performance for different multiplication factor N_2. Note that the cascaded PLL starts to outperform the single stage PLL at output frequencies where N_2^2 $£_{VCO2G}$ becomes lower than the second stage VCO phase noise $£_{VCO2}$. It can be seen that with a 2 GHz first stage PLL, single stage PLL outperforms cascaded PLL below 16 GHz, whereas cascaded PLL provides advantage above 16 GHz and at 28 GHz this improvement is approximately 5 dB. Hence we can conclude that as the required output frequency goes higher, the cascaded PLL improvement over single stage PLL increases.

A relevant question at this point is what is the optimal frequency for the 1st stage PLL to provide maximum performance improvement for a 28 GHz output clock? The choice of the first stage PLL frequency requires obtaining the minimum value of N_2^2 $£_{VCO1}$ where for 28 GHz output $N_2 = 28\ GHz / f_1$. Here, there is a trade-off that needs to be taken into account where lower f_1 provides lower $£_{VCO1}$ but at the cost of higher second stage frequency multiplication N_2 and vice versa. This trade-off suggests that there would be a value of f_1 where a global minimum phase noise can be achieved. Fig. 3.6(c) provides the cascaded PLL phase noise performance N_2^2 $£_{VCO7G}$ assuming a 7 GHz first stage (shown in black). From this plot, we can conclude that with

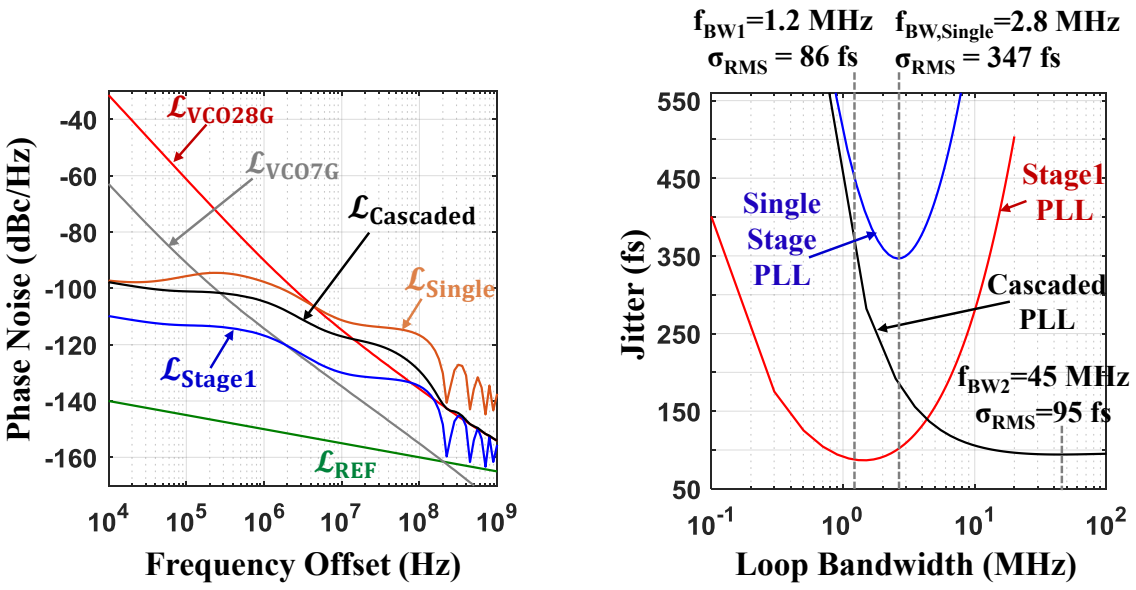


Fig. 3.7. The Fractional Mode. (a) The simulated phase noise performance of the cascaded PLL. (b) The simulated jitter versus PLL loop bandwidth for the Single Stage PLL and the first and second stages of the Cascaded PLL.

a 7 GHz first stage PLL, the cascaded PLL will always give better performance compared to the single stage PLL with an improvement of about 10 dB at 28 GHz output frequency. Fig. 3.6(d) introduces the simulated 28 GHz cascaded PLL phase noise performance at 10 MHz offset for different first stage PLL frequencies showing optimal performance at $f_{1.opt} = 7\ GHz$. The optimal first stage PLL frequency $f_{1.opt}$ is dependent on the technology node, the required output frequency, and the VCO phase noise trend.

3.3.3 Phase Noise Optimization with Fractional Noise

The phase noise of the fractional-N cascaded PLL composed of a first stage fractional-N 7 GHz PLL followed by a second stage integer-N 28 GHz PLL is illustrated in Fig. 3.7(a) together with that of the 28 GHz single stage PLL. Due to the fact that the first stage 7 GHz fractional-N PLL has lower loop bandwidth compared to the single stage PLL, the cascaded PLL is capable of filtering more fractional noise. The simulated jitter versus loop bandwidth for the single stage PLL and the first and second stages of the cascaded PLL are shown in Fig. 3.7(b).

3.4 Transistor-level Implementation of the Cascaded PLL

The block diagram of the proposed cascaded PLL implemented in the TSMC 65 nm CMOS process is illustrated in Fig. 3.8. The proposed cascaded PLL consumes lower power compared

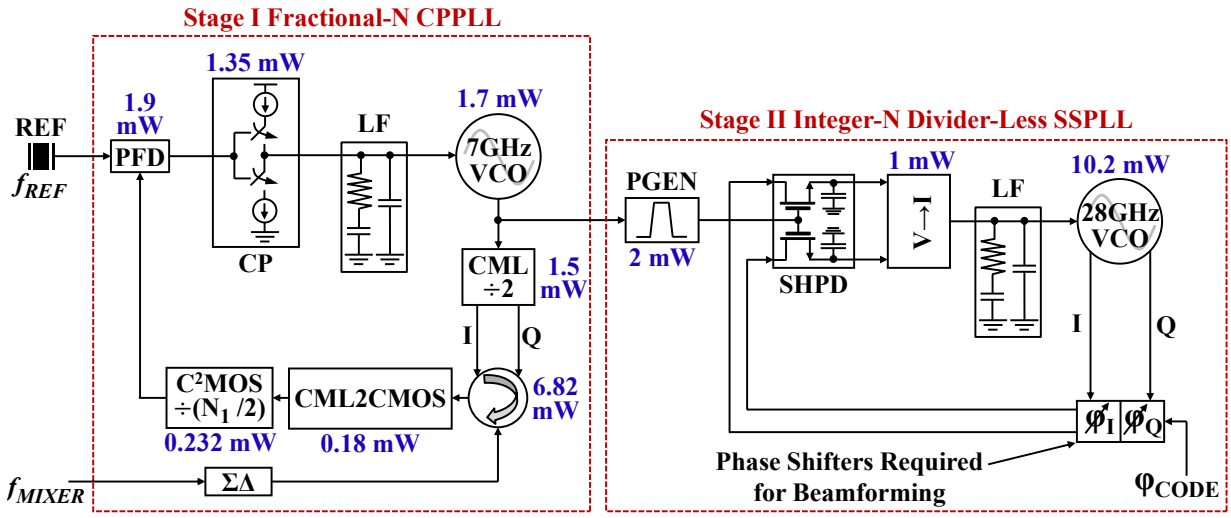


Fig. 3.8. The block diagram of the cascaded 28 GHz fractional-N frequency synthesizer.

to the single stage PLL due to the absence of the 28 GHz and 14 GHz high frequency dividers in the cascaded PLL owing to employing a divider-less SSPLL in the second stage. As the second stage 28 GHz QPLL is to be employed as a local PLL in each RF channel of the 5G transceiver as previously explained in Fig. 2.1(b), a phase shifter is added in the feedback path of the second stage PLL to provide the phase shifting required for beamforming. The amount of this phase shift is determined by φ_{CODE}. In this section, the implementation of the first stage CPPLL and the second stage SSPLL is discussed.

3.4.1 The First Stage 7 GHz Fractional-N CPPLL

The first stage PLL is implemented as a type II CPPLL that multiplies the input reference clock to provide a clean low jitter 7 GHz clock output. The design of the first stage PLL is similar to that of the single stage PLL. It comprises a PFD, CP, LF, a 7 GHz differential VCO, phase mixer and the feedback divider as illustrated in Fig. 3.8. Improved phase noise performance is required from the first stage PLL as its output will serve as the reference to the second stage. Hence, the first stage utilizes a differential VCO instead of a quadrature one for its improved inductor quality factor and consequently provides enhanced VCO phase noise. Since a differential VCO is utilized in the first stage, its output is first introduced to a master-slave CML divider before the phase mixer to provide the in-phase and quadrature signals required by the phase mixing operation. It is possible to use injection locked divider [87] instead of CML divider. However, they not only need to have wide lock range but also they need to cover the entire VCO tuning

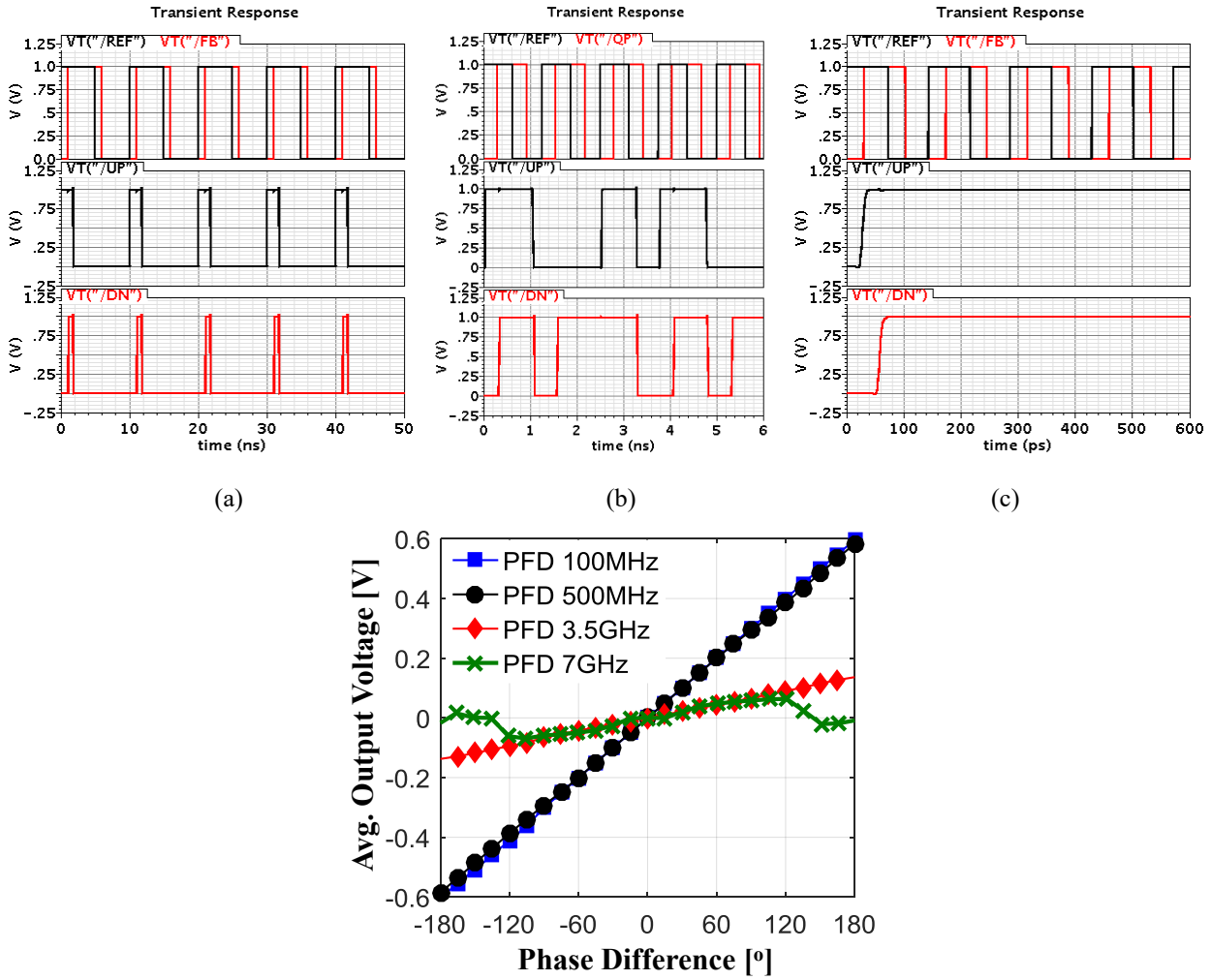


Fig. 3.9. PFD Post layout simulation, (a) Transient response at 100MHz. (b) Transient response at 800MHz. (c) Transient response at 7GHz. (d) PFD transfer characteristics.

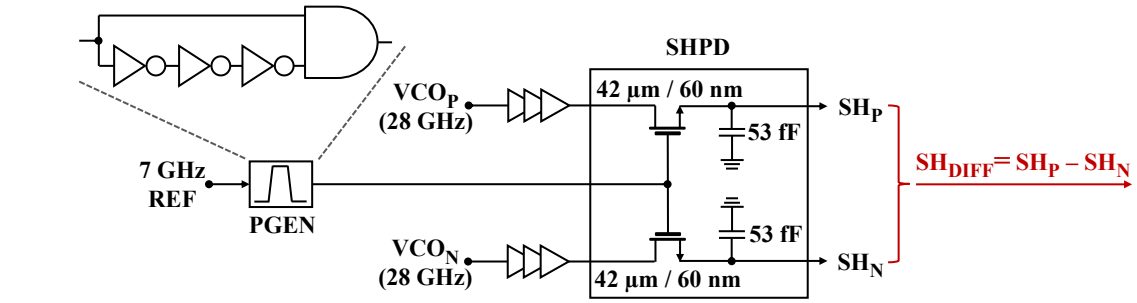
range which is very challenging. Therefore, using CML divider is a more reliable solution. The phase mixer output is then introduced to a CML-to-CMOS circuit for rail-to-rail swing required by the low-frequency master-slave C^2MOS dividers chain providing the remaining division ratio ($N_1/2$).

3.4.2 The Second Stage Divider-less Subsampling PLL

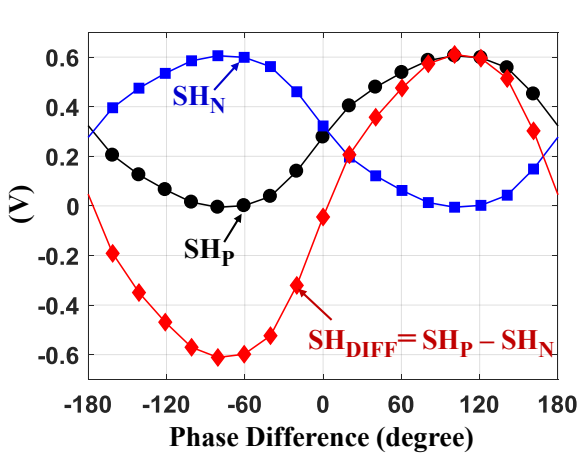
The 7 GHz output from the first stage fractional-N PLL is input to the second stage PLL as its reference for the (4×) frequency multiplication to provide the final 28 GHz output clock. A conventional CPPLL cannot serve as the second stage for two main reasons. First, the conventional PFD cannot operate at such high reference frequency due to the limitation by the

feedback path where at 800 MHz the PFD starts to fail. This can be concluded from the post layout simulated PFD performance provided in Fig. ß3.9. To enable high frequency operation, the PFD would require burning more power to meet the critical feedback NAND gate operation. Second, the 28 GHz and 14 GHz dividers are area and power consuming. A possible candidate to serve as the second stage PLL and resolve the above issues is the divider-less SSPLL [54], [88]–[91]. The block diagram of the SSPLL is shown in Fig. ß3.8 comprising a pulse generator (PGEN), a SHPD, a V→I, a LF and the quadrature 28 GHz VCO. The use of the SSPLL as the second stage adds a couple of advantages to the architecture. First, no 28 GHz and 14 GHz high frequency dividers are required resulting in lower power consumption. The absence of the feedback dividers results in the SHPD and V→I noise not being amplified by N_2^2, hence improving the PLL jitter performance. In addition to that, the SHPD can operate at high frequencies with low power consumption.

To get more insight into the operation of the SSPLL, the SHPD characteristics need to be studied. The 7 GHz reference from the first stage PLL is applied to the pulse generator that samples the 28 GHz VCO output via the SHPD. To avoid the VCO being loaded by the SHPD, buffers are introduced between the VCO and the SHPD. The schematic of the differential SHPD designed using two NMOS switches and two 53 fF MOSCAPs is illustrated in Fig. ß3.10(a). To plot the SHPD transfer characteristics, the delay between the 7 GHz reference and the VCO output is varied from -18 ps to 18 ps which is equivalent to a phase error of -180º to 180º. Fig. ß3.10(b) shows the post-layout simulated SHPD transfer characteristics where both the single ended (SH_P and SH_N) and differential (SH_{DIFF}) outputs are plotted showing 0.6 V_{PP} and 1.2 V_{PP} swings, respectively. From which it can be concluded that the locking point where the phase error between the SHPD inputs diminishes is the intersection between SH_P and SH_N. Near the locking point, the output of the SHPD is proportional to the phase error with a sufficiently linear behavior. It can also be noted out that the SHPD can operate at the high 7 GHz reference clock without consuming a large amount of power. The layout of PGEN and SHPD is shown in Fig. ß3.10(c) occupying an area of 20.4 µm × 15.2 µm. The output of the SHPD is introduced to the V→I. The schematic and layout of the V→I are illustrated in Fig. ß3.11 occupying an area of 15.8 µm × 13.3 µm.



(a)



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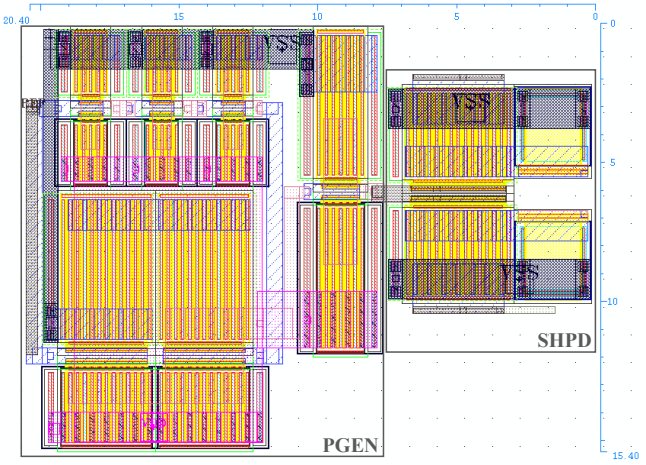
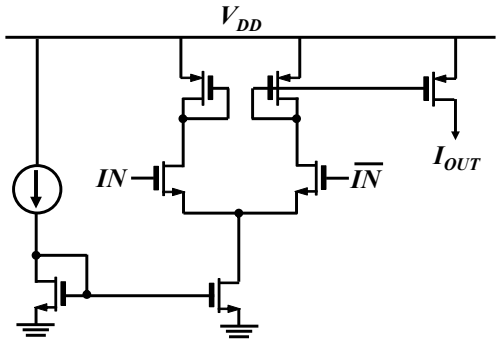
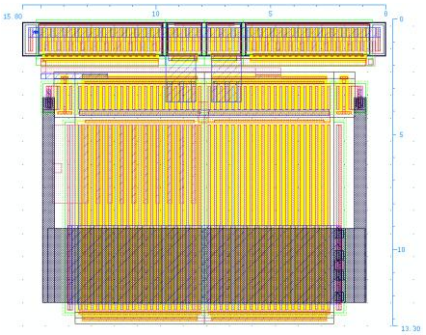


(c)

Fig. 3.10. (a) The SHPD schematic with design parameters. (b) The post layout simulated SHPD transfer characteristics. (c) The layout of the PGEN and SHPD.



(a)



(b)

Fig. 3.11. The V2I implementation. (a) Schematic. (b) Layout.

Operating the SSPLL with a high-frequency reference clock has a couple of benefits. The SSPLL is prone to false lock as it can lock to any harmonic (Kf_{REF}) of the input reference, where K=1, 2… In addition to that, the sinusoidal nature of the SHPD limits its capture range. Hence, typically an additional frequency locked loop is required for proper locking [92]. However, if the

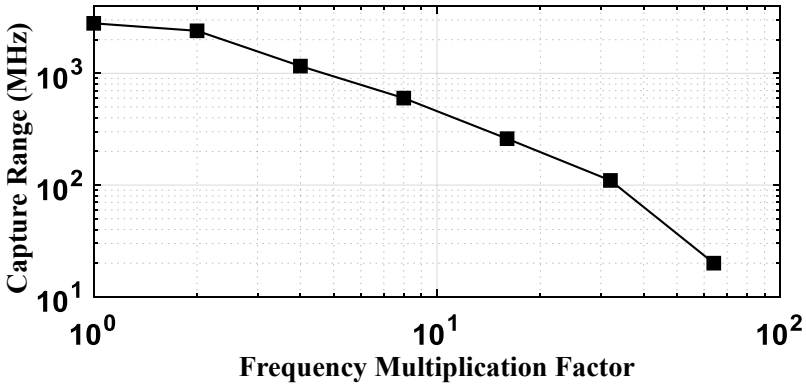
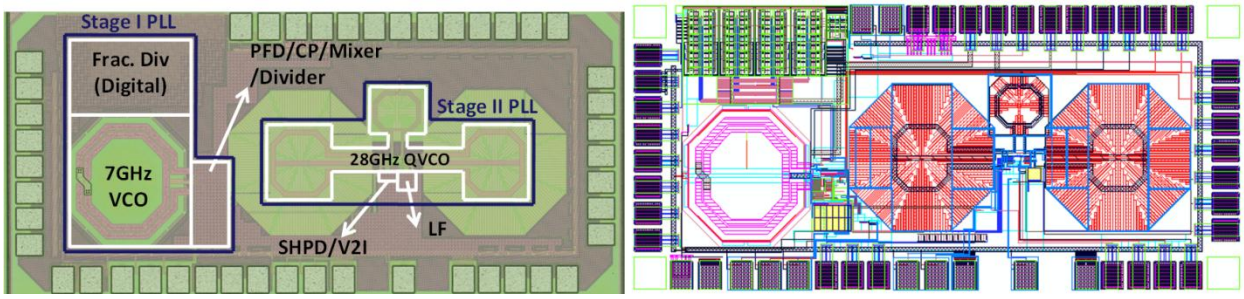


Fig. 3.12. Simulated capture range versus frequency multiplication factor for the 28 GHz subsampling PLL.



(a) (b)

Fig. 3.13. The fabricated 28 GHz cascaded fractional-N frequency synthesizer prototype. (a) Die micrograph. (b) The complete chip layout.

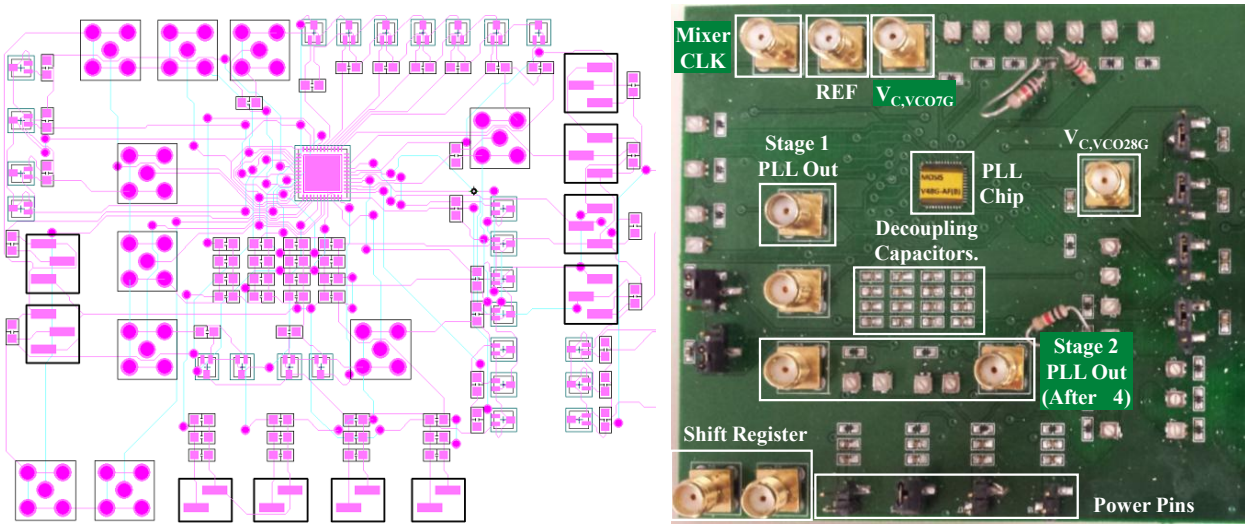
VCO tuning range is lower than the reference frequency input to the SSPLL, false locking will be avoided [93]. Using high frequency 7 GHz reference eliminates the possibility of false locking where the nearest harmonics that the second stage 28 GHz SSPLL can falsely lock to, are at 21 GHz and 35 GHz which are beyond the VCO tuning range. Hence, no frequency locking loops are required reducing the SSPLL complexity and power. Moreover, the high frequency input reference results in higher SSPLL capture range. Fig. ƀ.12 provides the simulated 28 GHz SSPLL capture range versus frequency multiplication showing that for 4× multiplication factor the capture range is higher than 1 GHz. Also, the high frequency reference allows for high PLL loop bandwidth and hence more filtering of the 28 GHz VCO phase noise.

3.5 The Measurement Results of the Cascaded PLL

A 28 GHz fractional-N cascaded PLL prototype for 5G transceivers was implemented in the TSMC 65 nm CMOS process. The die micrograph of the implemented prototype is illustrated in Fig. ƀ.13 occupying an active area of 0.28 mm^2. The cascaded PLL consumes a total of 26.9 mW

Table 3.2
Power and Area Breakdown for the 28 GHz Cascaded Fractional-N Synthesizer

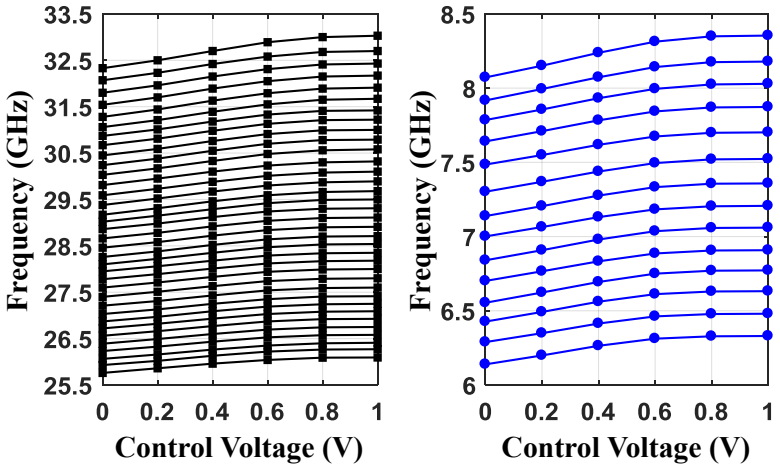
		Power (mW)	Area (μm^2)
Stage I CPPLL	**PFD**	1.9	46 × 37.5
	CP	1.35	51.7 × 53.7
	7 GHz Differential VCO	1.7	327.1 × 350.6
	Phase Mixer	6.82	435 × 270
	CML Divider	1.5	26.1 × 14.3
	CML-to-CMOS	0.18	39 × 15
	C^{2}MOS Divider	0.232	68.5 × 15.2
Stage II SSPLL	**PGEN + SHPD**	2	20.4 × 15.2
	V→I	1	15.8 × 13.3
	28 GHz Quadrature VCO	10.2	724.5 × 458.9



(a) (b)

Fig. 3.14. Testing PCB board for the cascaded 28 GHz synthesizer. (a) PCB layout. (b) PCB with the fabricated chip mounted.

from 1 V supply. The power and area breakdown of the fabricated prototype are provided in Table 3.2. The first stage consumes 13.7 mW while the second stage consumes 13.2 mW. Two factors resulted in lower power consumption from the cascaded PLL compared to the single stage PLL, (1) the absence of the high frequency 28 GHz and 14 GHz CML dividers, (2) the cascaded PLL has its fractional divider operating at a lower frequency than that in the single stage PLL.



(a) (b)

Fig. 3.15. The VCOs Tuning Characteristics. (a) The 28 GHz VCO. (b) The 7 GHz VCO.

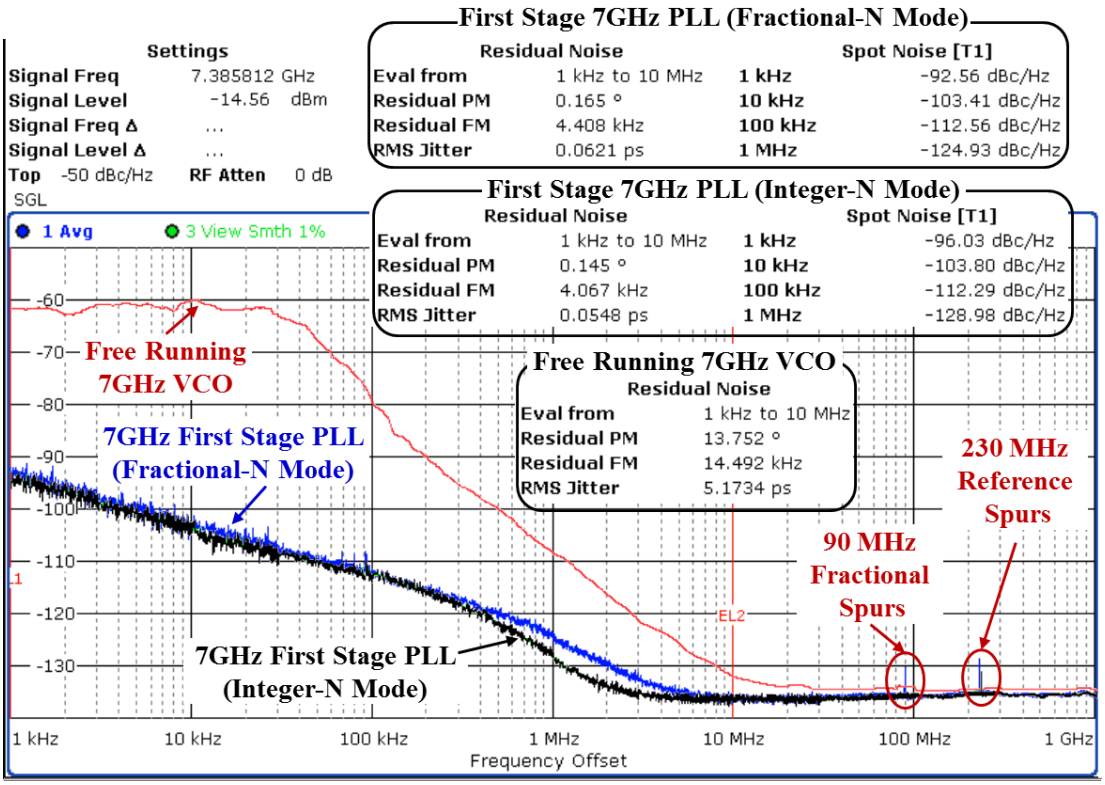


Fig. 3.16.The Measured Phase noise performance of the 1st stage 7 GHz PLL in integer-N and fractional-N modes together with that of the 7 GHz VCO.

A two-layer FR-4 PCB was designed for testing the fabricated packaged die as illustrated in Fig. 3.14 where to test the QFN packaged dies, the divide-by-4 output of the 28 GHz synthesizer was observed in the measurements. The 7 GHz and 28 GHz VCOs tuning characteristics are illustrated in Fig. 3.15. For testing the implemented prototypes, a 230 MHz reference clock was

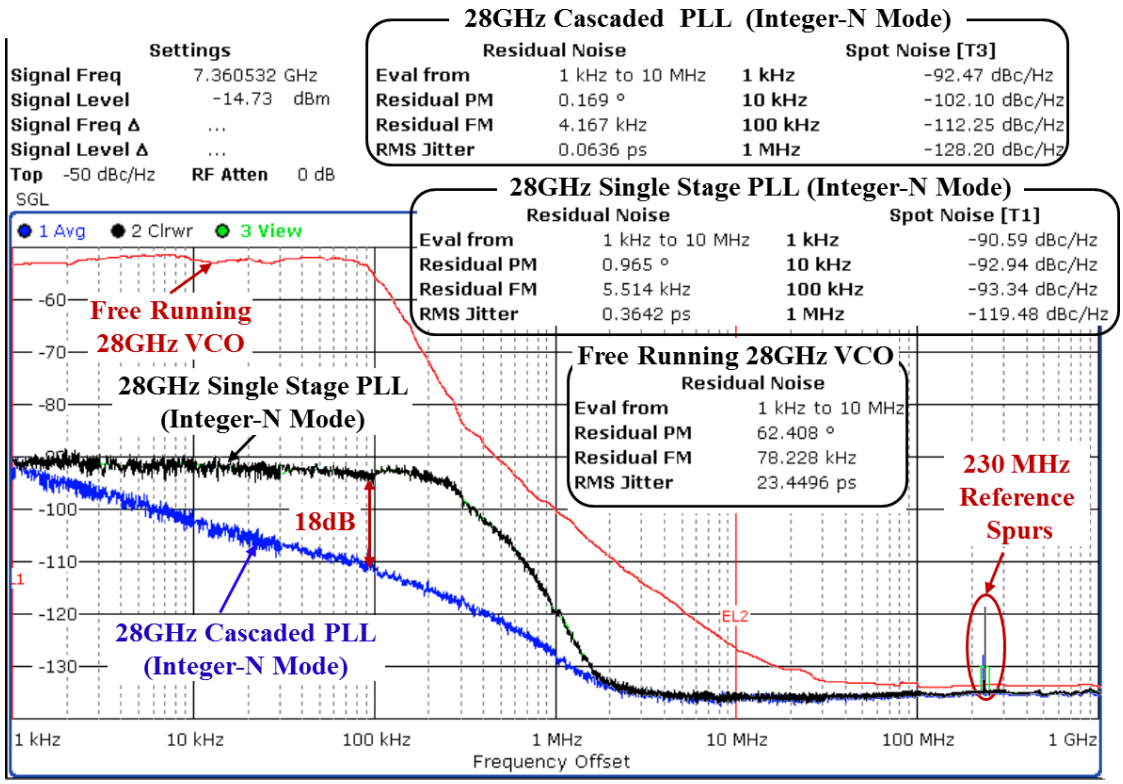
Table 3.3
Integrated Jitter for the Fabricated Synthesizers

		Integration Interval (MHz)			
		0.001–10	**1–10**	**0.001–100**	**0.001–240**
First Stage 7 GHz PLL	**Integer-N**	54.8 fs	48.84 fs	71.6 fs	90.21 fs
	Fractional-N	62 fs	51.25 fs	77.92 fs	94.9 fs
Cascaded 28 GHz PLL	**Integer -N**	63.6 fs	49.9 fs	79.24 fs	95.6 fs
	Fractional-N	70.4 fs	51.53 fs	84.74 fs	98.9 fs
Single Stage 28 GHz PLL	**Integer -N**	364.2 fs	51.32 fs	367.79 fs	373.98 fs
	Fractional-N	557 fs	59 fs	565.16 fs	572.1 fs

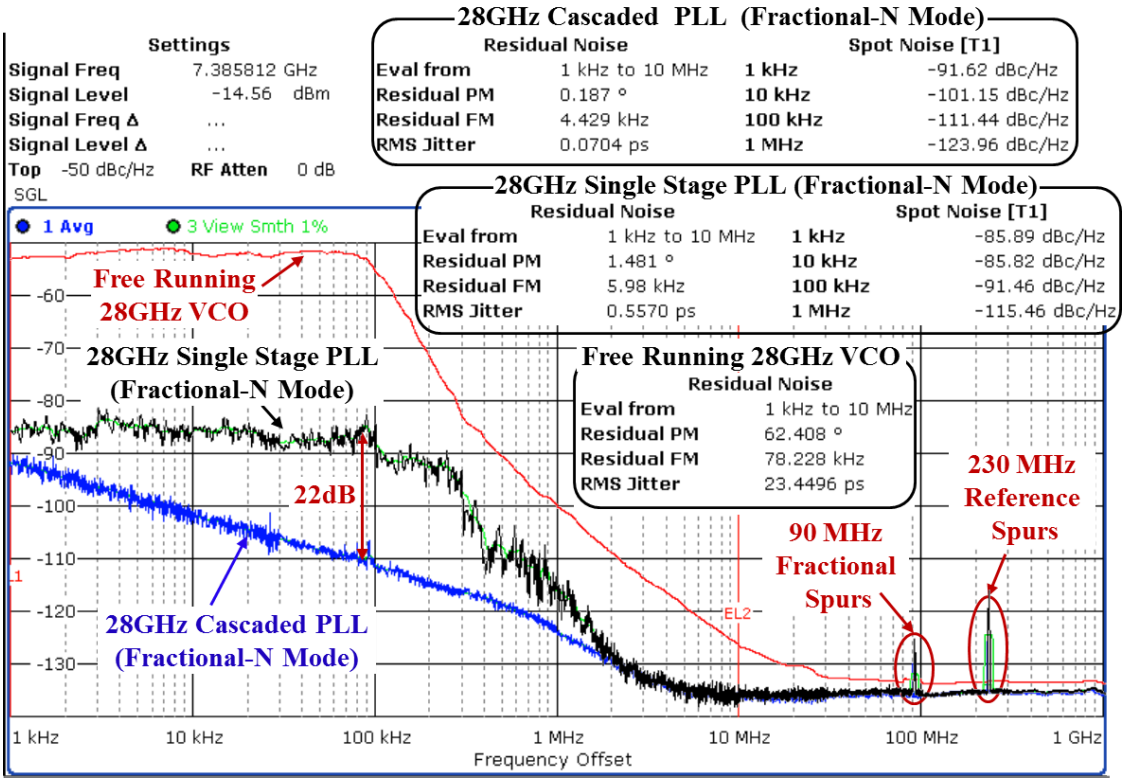
used. The measured phase noise performance of the first stage 7 GHz PLL in both integer-N and fractional-N modes together with the 7 GHz VCO phase noise are shown in Fig. 3.16. Fig. 3.17 provides the measured phase noise of the 28 GHz cascaded PLL together with that of the free running 28 GHz VCO and the 28 GHz single stage PLL after divide-by-4 for both integer-N and fractional-N modes where the three phase noise regions in the analysis provided in Fig. 3.5 can be distinguished in the measured results. For the fractional-N phase noise plots, a fractional spur can be seen at 90 MHz due to applying a 90 MHz mixer clock for rotating the mixer. From the obtained results it can be found that the free-running 7 GHz and 28 GHz VCOs have phase noise of –109 dBc/Hz and –89.91 dBc/Hz at 1 MHz offset with Figure-of-merit (FoM_{VCO}) of 183.55 dB and 287.9 dB, respectively where FoM_{VCO} is computed as [94]

$$FoM_{VCO} = 10\log\left(\left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{£(\Delta f)P_{diss}(mW)}\right) \tag{3.4}$$

The first stage 7 GHz PLL shows phase noise at 1 MHz offset of –129 dBc/Hz and –125 dBc/Hz for the integer-N and fractional-N modes, respectively. The cascaded PLL (after divide-by-4) in the integer-N and fractional-N modes achieves a 1 MHz offset phase noise of -128.2 and -124.6 dBc/Hz, respectively that translates to –116.2 and –112.6 dBc/Hz at 28 GHz. Compared to single stage PLL; the cascaded 28 GHz PLL shows 22 dB improvement in phase noise near 100 kHz offset for the fractional mode, which also agrees with the theoretical analysis performed predicting that at high mm-Wave frequencies the cascaded PLL will outperform the single stage PLL. Table 3.3 shows the integrated jitter of the 7 GHz first stage PLL, the cascaded PLL and the single stage PLL over different integration intervals where it can be seen that over different intervals the cascaded PLL with both its integer-N and fractional-N modes achieves integrated jitter below 100 fs.



(a)



(b)

Fig. 3.17. The Measured Phase noise of the 28 GHz VCO, Single stage, and Cascaded PLL after divide-by-4. (a) Integer-N Mode. (b) Fractional-N Mode

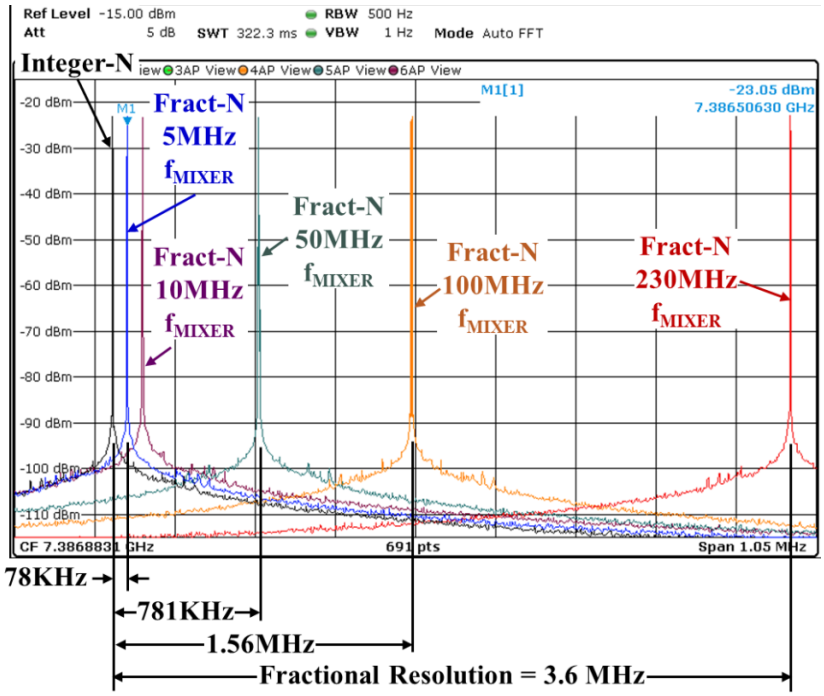


Fig. 3.18. The Measured locked spectrum of the 28 GHz cascaded PLL (after divide-by-4) for the integer-N and fractional-N modes showing the fractional resolution at different mixer clock frequencies.

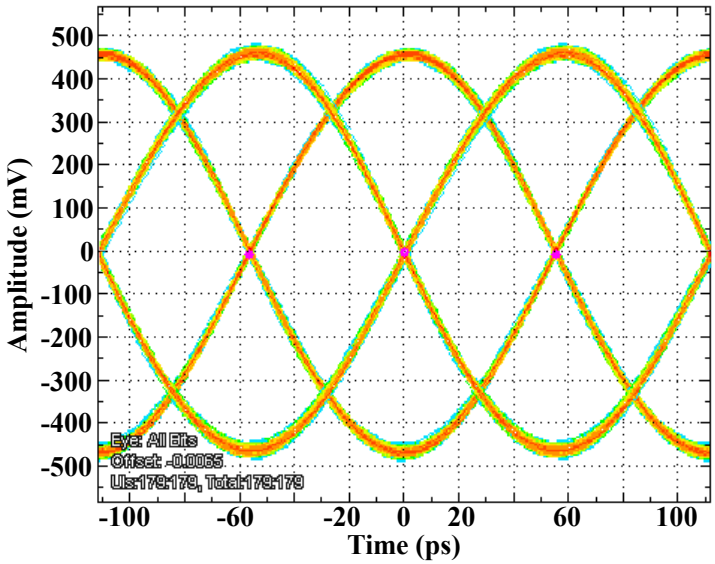


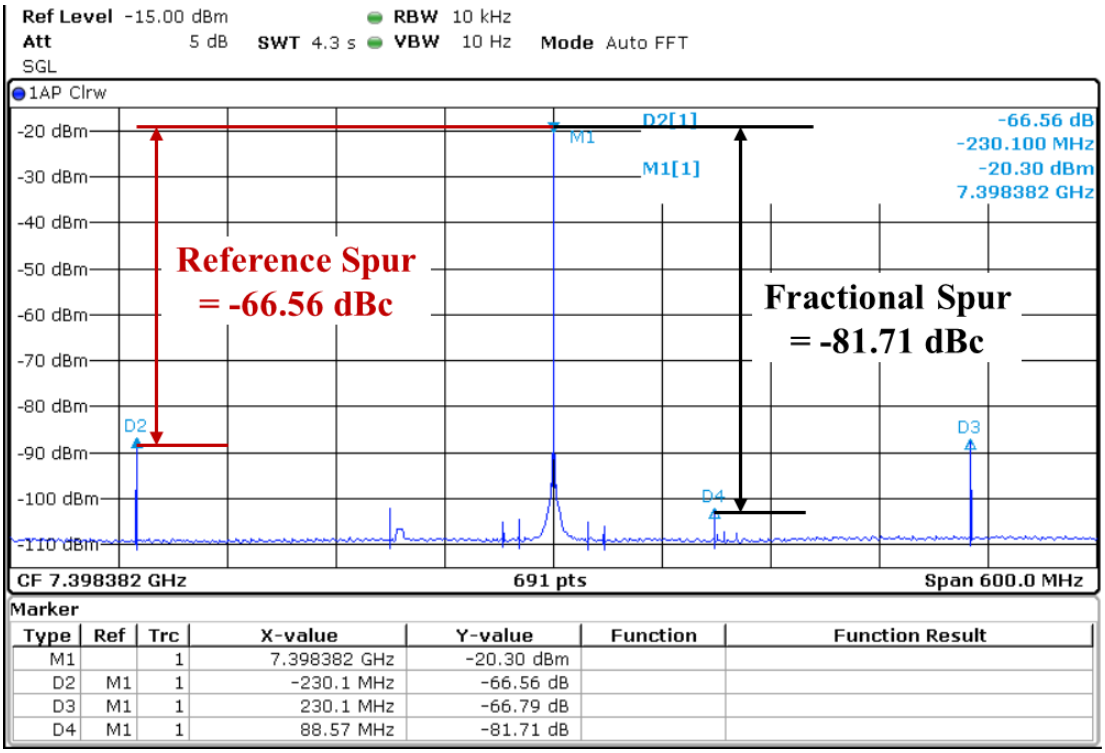
Fig. 3.19. The Measured Eye Diagram of the divided version of the Locked Cascaded PLL output I/Q clock.

Fig. 3.18 shows the measured locked spectrum of the cascaded PLL after divide-by-4 for integer-N and fractional-N modes with different mixer clock frequencies for the fractional mode showing fractional resolution of 78 kHz and 3.6 MHz at 5 MHz and 230 MHz mixer clock frequencies, respectively. The measured fractional resolution agrees with the theoretical

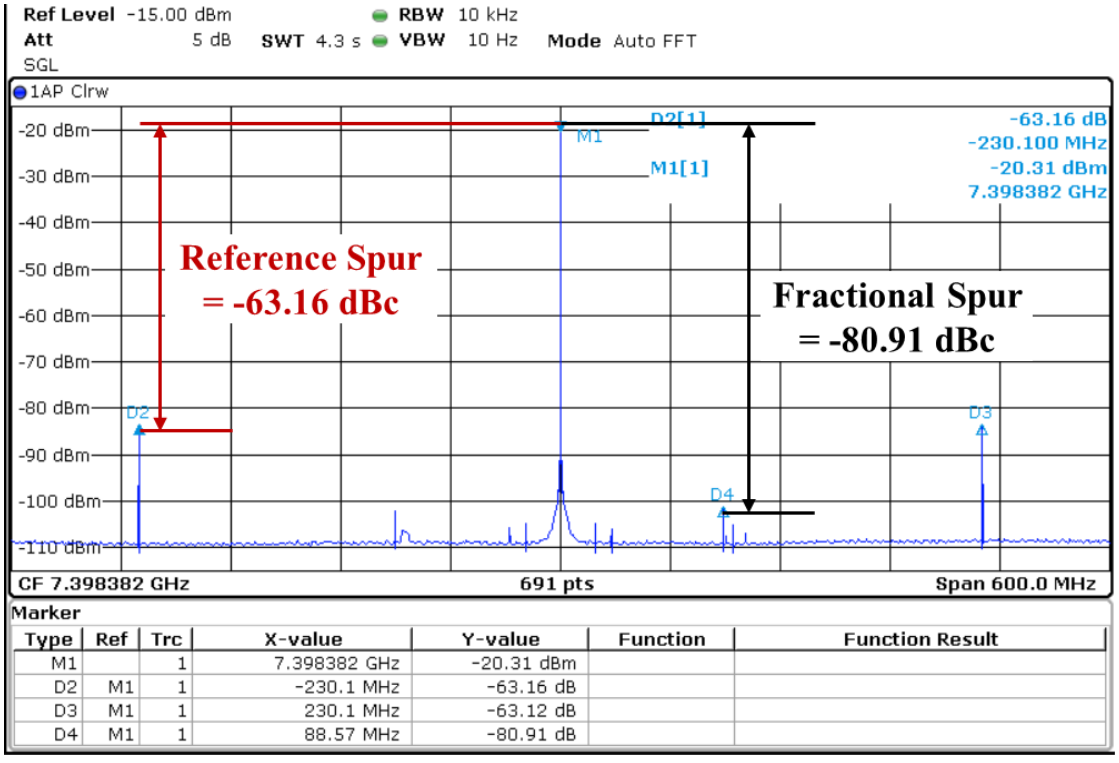
fractional resolution given as $f_{Mixer}/256$ in case of the 256-phase mixer. The measured eye diagram of the divided version of the locked cascaded PLL output I/Q clock is illustrated in Fig. ß3.19 showing an I-Q error of 0.87^{o} (measured from time domain exported data). Fig. ß3.20 shows the measured spurious content of the first stage 7 GHz PLL and the final 28 GHz cascaded PLL output (after divide-by-4) where fractional division is attained using a 100 MHz mixer clock achieving reference/fractional spurs of –66.56 dBc/–81.71 dBc and –63.16 dBc/–80.91 dBc for the first stage and cascaded PLL outputs, respectively. The highest fractional spur is located at 100 MHz due to using a 100 MHz mixer clock. Fig. ß3.21 shows the phase noise at 1 MHz offset of the cascaded and single-stage PLLs over the PLL's tuning range (26.2–32.4 GHz) for integer-N and fractional-N modes. Fig. ß3.22 provides the FoM plot of the implemented single stage and cascaded PLLs with state-of-the-art synthesizers. Table ß3.4 provides a summary of the 28 GHz cascaded PLL and single stage PLL performance compared to the state-of-the-art frequency synthesizers [95]–[103].

3.6 Conclusion

A 28 GHz fractional-N cascaded PLL was presented. It is implemented with the fractional division performed in the first stage CPPLL using phase mixing and the second stage is implemented as a divider-less sub-sampling PLL. A significant performance improvement was shown in comparison to the single stage PLL both in terms of jitter and power consumption. The results were also compared to state-of-the-art solutions, and it was shown that the proposed PLL achieves excellent phase noise performance with comparable power consumption suitable to meet the stringent requirements for the upcoming 5G mobile transceivers.



(a)



(b)

Fig. 3.20. (a) The Measured Spurious content of the first stage 7 GHz PLL output. (b) The Measured Spurious content of the Final Cascaded PLL output (after divide-by-4).

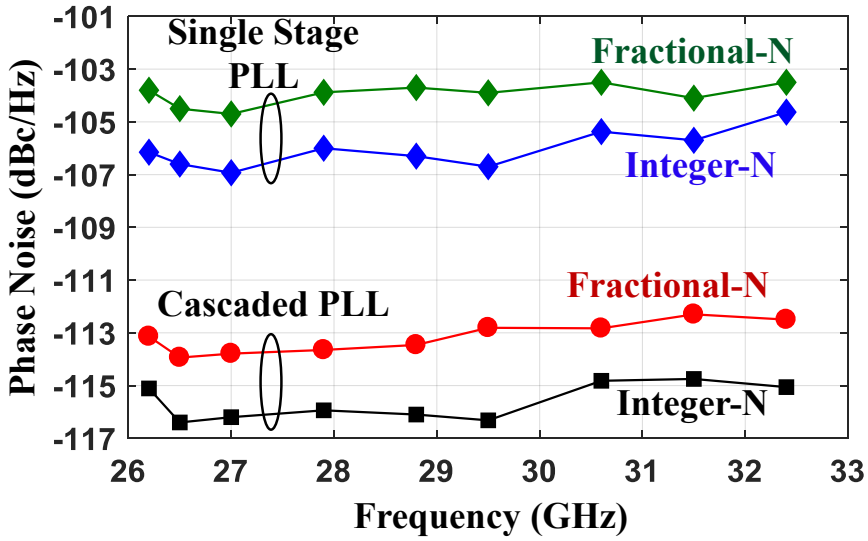


Fig. 3.21. Measured Cascaded PLL Phase Noise at 1MHz offset over the PLL Tuning Range.

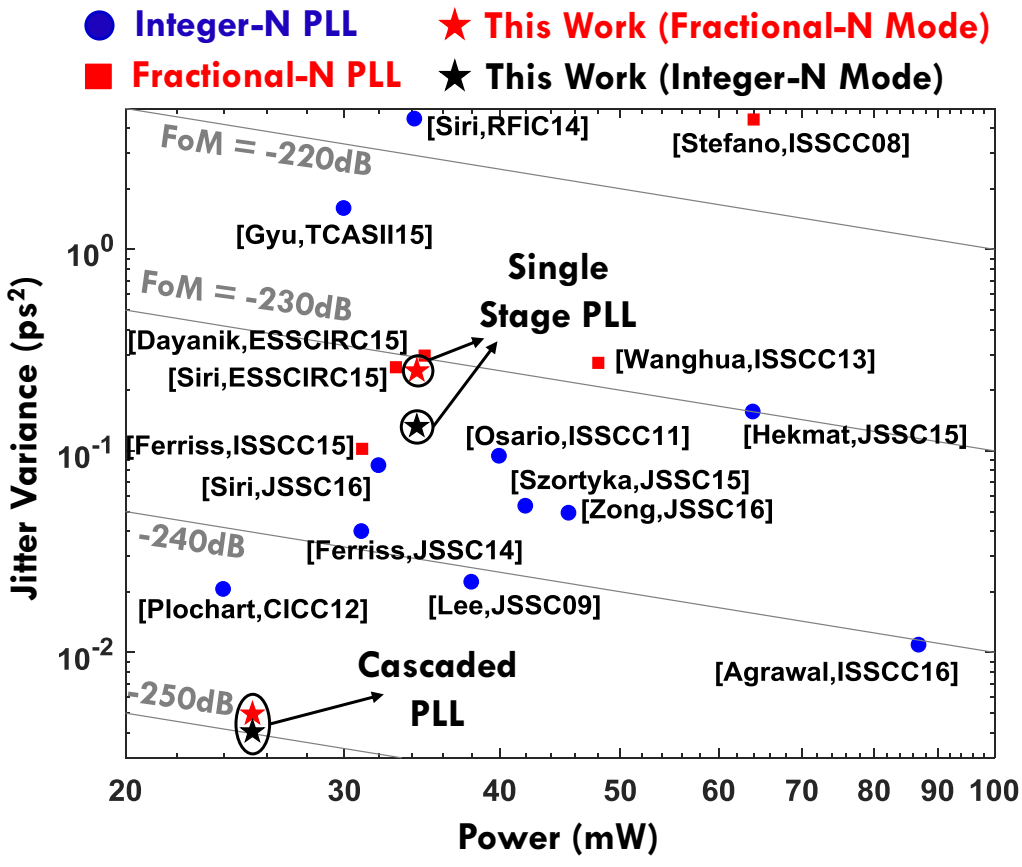


Fig. 3.22. FoM plot of the implemented single stage and cascaded PLLs with state-of-the-art synthesizers.

Table 3.4
Comparison With State-of-the-art mm-Wave Frequency Synthesizers

		This Work		**[95]**	**[96]**	**[97]**	**[98]**	**[99]**	**[100]**	**[101]**	**[102]**	**[103]**
		Cascaded	**Single Stage**									
Process (nm)		CMOS65	CMOS65	CMOS28	CMOS65	SOI32	CMOS45	SOI 32	CMOS40	SOI 32	CMOS65	CMOS65
Type		Fractional	Fractional	Integer-N	Integer-N	Fractional	Integer-N	Fractional	Integer-N	Integer-N	Fractional	Fractional
Reference (MHz)		230	230	125	N/A	133	48	104	390	194	40	52
Resolution		$0.015F_{MIXER}$	$0.0039\ F_{MIXER}$	F_{REF}	N/A	N/A	F_{REF}	$0.023\ F_{REF}$	F_{REF}	F_{REF}	*N/A*	*N/A*
Output Clock (GHz)		26.2-32.4	26.2-32.4	21-32	22.6-32.4	12-26	21.7-27.8	13.1-28	21.4-25.1	23.8-30.2	27.5-29.6	20.4-24.6
Area (mm^2)		0.28	0.18	0.015	1.8	0.28	0.139	0.24	0.1	0.02	1.2	0.48
Power (mW)		26.9	35.8	30	87	30	40	31	64	31	33	19.7
Supply (V)		1V	1V	1V	1V	1V	N/A	1V	1V	1V	1V	1V
PN @ 1 MHz (dBc/Hz)	**Integer**	-116.2	-107	-91	-106.8	-90	-95	-80.5	-101	-92	-95	-90
	Fractional	-112.6	-103.4									
Norm. PN @ 1 MHz**	**Integer**	-116.2	-107	-96.3	N/A	-94.76	-108.61	-87.39	-96.41	-93.48	-110.19	-102.91
	Fractional	-112.6	-103.4									
Integrated Jitter (fs)	**Integer**	63.6	364.2	1260	103.9	N/A	306.2	320	394	199	510	242
	Fractional	70.4	500									
FoM* (dB)	**Integer**	-249.63	-233.23	-223.22	-235.5	N/A	-234.26	-235	-230	-239.1	-231	-239.4
	Fractional	-248.75	-230.58									

* FoM = $10\ \log_{10}((\text{Jitter}/1\text{s})^2*(\text{Power}/1\text{mW}))$ **Normalized to 230 MHz reference: PN(dBc/Hz)+20log(f_{REF} /230MHz)

4. THE TIME-DOMAIN ANALOG-TO-DIGITAL CONVERTER

For the hybrid-beamforming transceiver, a high-performance low-power ADC is required. In this chapter, the proposed time-based analog-to-digital converters are discussed. Time-domain ADCs comprises a voltage-controlled oscillator (VCO) followed by a time-to-digital converter (TDC). Two ADC prototypes are introduced. The first is a first-order noise shaped 675 MS/s oversampling ADC that employs a high-resolution SAR-TDC as a quantizer. The second prototype is a Nyquist-rate reconfigurable ADC employing a reconfigurable TDC that can be configured as a high-resolution SAR-TDC for the high-resolution modes or as a 4× asynchronous time-interleaved (TI) Flash-TDC for the high sampling rate modes. Both prototypes utilize a highly linear 1-bit folded VCO for improved linearity. In the beginning, an introduction to time-based ADCs and time-to-digital converters will be provided.

4.1 Background and Introduction to Time-based ADCs

First, we need to discuss the rationale for migrating from voltage-domain ADC to their time-domain counterparts. What has driven the interest towards time-based architectures is the continuous scaling in CMOS technologies. Technology scaling with shorter channel transistors is accompanied with lower supply voltages, lower intrinsic transistor gain, and higher speed devices. The degraded intrinsic transistor gain and the lower supply voltage which results in limited voltage headroom add more challenges and limitations to designing the analog blocks. This has its reflection on the voltage-based architectures whose performance is dependent on the analog blocks constructing them including operational amplifiers, comparators … etc where high gain, wide bandwidth amplifiers and matching between components are obviously more difficult to achieve with technology scaling. Moreover, the lower voltage headroom limits the output signal swing resulting in degrading the signal-to-noise ratio of the analog-based voltage-domain architectures. On the other hand, technology scaling comes with improvements in device switching speed which translates to enhancement in the time resolution. Hence, by representing the signal in time-domain rather than in the voltage-domain, improved resolution can be

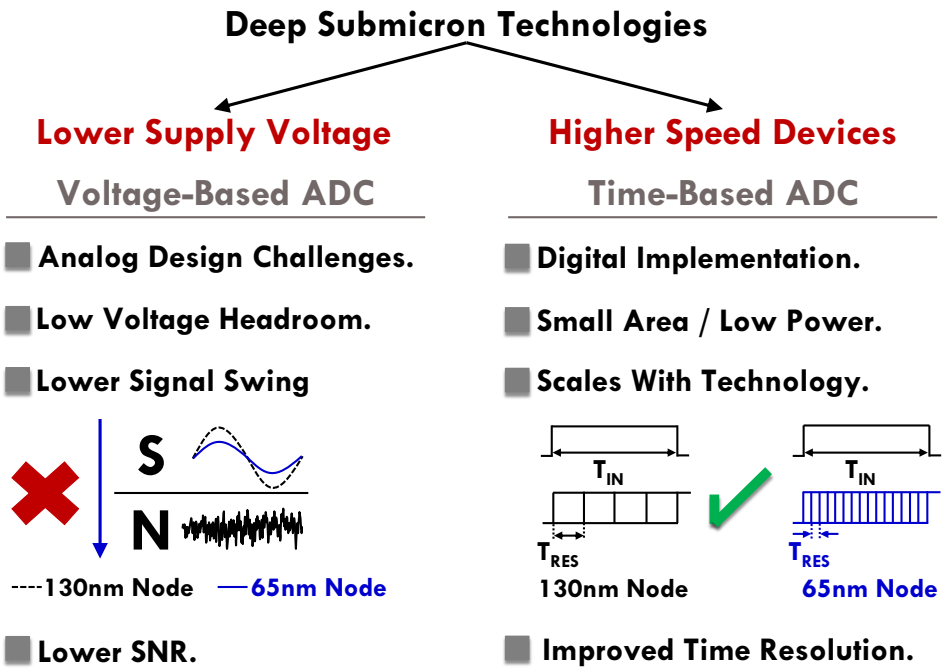


Fig. 4.1. Voltage-based ADC versus Time-based ADC in deep submicron technologies.

achieved in deep submicron technology nodes. In addition, time-domain architectures are digital in nature which eliminates the analog design challenges and guarantees small implementation area, low power operation and resolution/speed improvement with technology scaling. Fig. 4.1 summarizes the main comparison points between voltage-domain and time-domain ADCs. For the time-based operation, a VCO is utilized for the voltage-to-time conversion where the analog input is converted to time period.

Now, let's consider the following example to have more insight into the advantages of the time-domain ADC over its voltage-domain counterpart. Assume that we have a 50 μV_{PP} analog input sinusoid that is required to be digitized using a voltage-domain flash ADC which utilizes comparators with 50 mV threshold. This requires first amplifying the analog input using an operational amplifier with at least 60 dB gain over the operating bandwidth of the ADC. This is very challenging at deep submicron technologies with respect to achieving the required gain over a wide bandwidth while maintaining the high linearity. On the other hand, if a time-based ADC is used to digitize this analog input, the required voltage-to-time gain can be easily attained by adjusting the gain sensitivity of the VCO.

Moreover, when reconfigurability is required from the ADC, the time-based architectures can offer more flexibility, better hardware re-use and a wider range of reconfigurability over

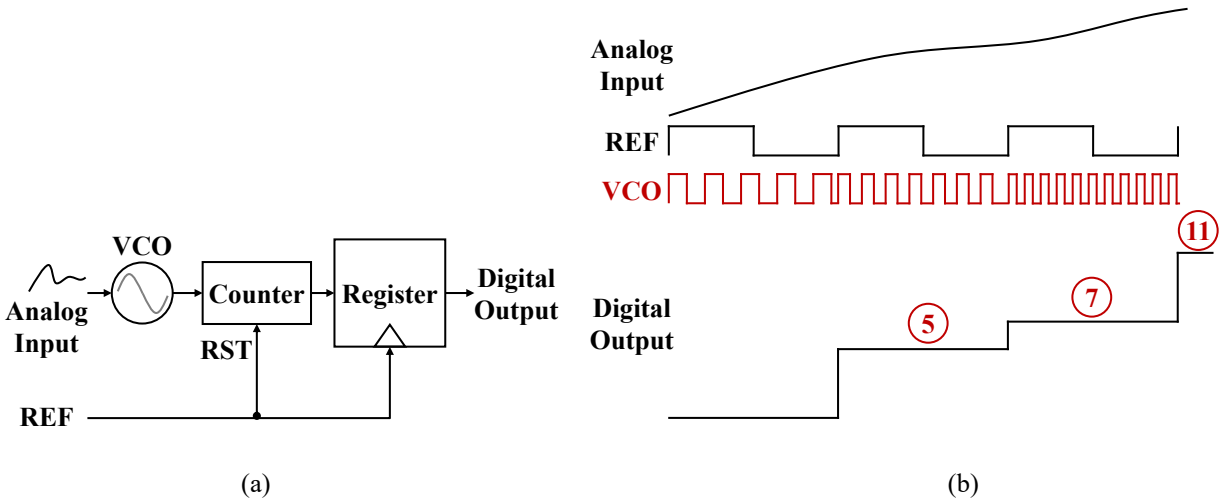
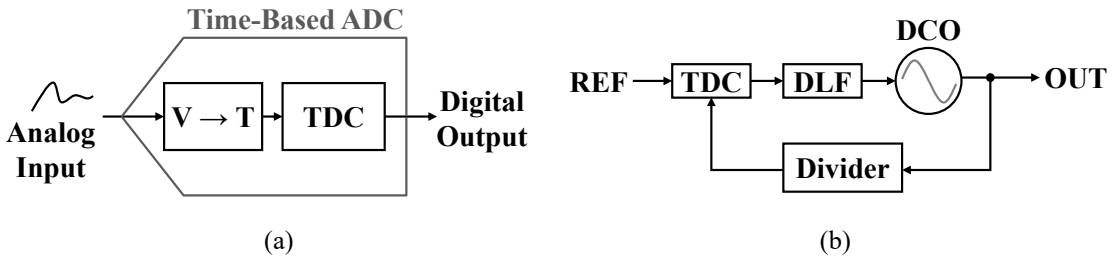


Fig. 4.2. The single-phase time-based ADC. (a) Block Diagram. (b) Timing Diagram.

both resolutions and bandwidth as will be further discussed in Section 4.4. All of this greatly motivated the research in time-based ADCs.

The idea of time-domain ADCs was first proposed by Victor B. Boros in 1977 where a time-based ADC was designed as a part of a digitally-controlled switching regulator [104]. The ADC was designed as a single-phase time-based ADC employing a VCO, a counter and a sampling register as illustrated in Fig. 4.2(a). Its operation is shown in Fig. 4.2(b) where the analog input is applied to the control voltage node of the VCO modulating its frequency while the counter continuously accumulates the number of transitioning edges during the reference sampling period. At the end of the sampling period, the counter output is sampled by a register and reset to zero and the process repeats. That ideal was revisited in 1998 when A. Iwata proposed using the time-based ADC as a multi-bit quantizer within a ΔΣ modulator [105]. However, the resolution of the single-phase ADC is limited since only one phase is available for counting. To improve its resolution a multi-phase time-based ADC was proposed in [106] taking advantage of the multiple phases available by the ring VCO, where each phase drives a counter providing higher resolution than the single-phase time-based ADC. This opened the door to designing more time-based ADCs; as quantizers integrated within closed-loop ΔΣ modulators [107]–[116], standalone oversampling time-based ADCs [117]–[121] and Nyquist rate time-based ADCs [122]–[131].

In general, the time-based ADC comprises a voltage-to-frequency converter (or equivalently a voltage-to-time converter (V→T)) followed by a frequency-to-digital converter



(a) (b)

Fig. 4.3. TDC employed in time-based systems. (a) Time-based ADC. (b) All-digital PLL.

(or equivalently a time-to-digital converter (TDC)) as illustrated in Fig. 4.3(a). To achieve high-resolution time-based ADC, both the voltage-to-time converter and the time-to-digital converter need to be highly linear and the TDC should provide high resolution for improved quantization noise level. Since the TDC represents the core of the time-based ADC, an introduction to TDCs will be provided in the next section.

4.2 Background and Introduction to Time-to-Digital Converters

Time-to-digital converters are circuits that convert time information to digital code [132]. Lots of research has been conducted on TDCs during the previous decades for exploring new implementation techniques and enhancing their performance. This encouraged utilizing the TDC as a main and critical building block in several time-based systems including time-based ADCs and all-digital PLL as illustrated in Fig. 4.3**.** The time-based ADC employs a TDC as a phase quantizer together with a V→T while the all-digital PLL [133] uses a TDC as a phase detector along with digital loop filter (DLF), a digitally-controlled oscillator (DCO) and a feedback divider. In addition to that TDCs are used for on-chip time measurements including jitter and skew measurements [134].

Early time-to-digital conversion designs were performed in the analog-domain where the time is first converted to voltage then the voltage is converted to a digital code using an ADC [135],[136]. Owing to the previously discussed limitations of the analog approach, the TDC started to migrate to the time-domain and gain the digital flavor [137]. One way to implement the TDC in the digital domain is the delay-line approach [138]. The delay line TDC illustrated in Fig. 4.4 is considered a flash-type TDC that digitizes the time duration between the start and stop signals. This is accomplished by delaying the start signal along a delay line with a unit delay of t_d and sampling the delayed versions of the start signal by the stop signal. This results in a thermometer code representing the final TDC output. The time resolution of that TDC is equal to

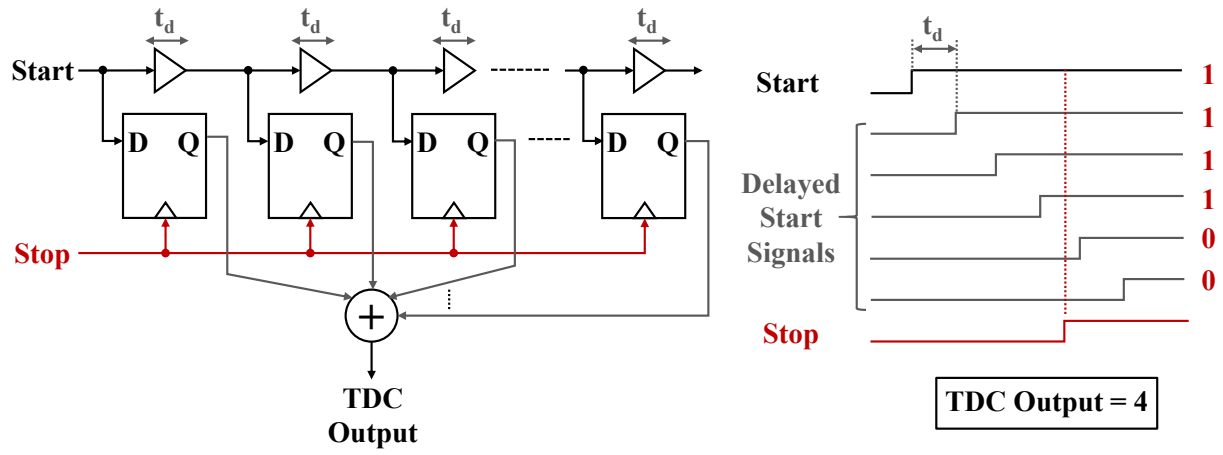


Fig. 4.4. Block diagram and operation of the conventional Delay line TDC.

the gate delay (t_d) employed within the delay line. Although this architecture is simple, it suffers mainly from two limitations. First, its resolution is limited by technology where it cannot go lower than the minimum gate delay supported by the fabrication process. Second, its maximum time interval that can be measured is limited by the length of the delay line. Hence, to measure larger time intervals, longer delay lines are required resulting in undesirable larger area and power consumption. The second limitation can be avoided by using a looped delay-line TDC illustrated in Fig. 4.5. In this architecture, a looped delay line is employed and the start signal is applied to the looped delay line through a MUX. In the beginning of the measurement, the MUX allows the start signal through the delay line then it switches to allow the feedback signal from the delay line to loop. The number of loops through the delay line is determined by a counter providing the coarse quantization of the TDC. The fine quantization is performed by the sampling registers similar to the case of the conventional delay line TDC.

To resolve the limited resolution issue, sub-gate delay TDC architectures were proposed. A Vernier TDC – a variation of the delay line TDC – can be designed to provide sub-gate resolution [139]–[141]. In its simplest form, it employs two delay lines, one for the start signal and another for the stop signal with delays of t_{d1} and t_{d2}, respectively as illustrated in Fig. 4.6 . By setting t_{d1} slightly larger than t_{d2}, a sub-gate resolution of $t_{d1} - t_{d2}$ can be achieved from the TDC. Apart from the Vernier TDC, other TDC architectures are also capable of providing sub-gate resolution. This includes pulse-shrinking TDCs [142],[143], two-step TDCs [144],[145], pipelined TDCs [146]–[148], SAR TDCs [149],[150] and oversampling TDCs [151]–[153]. In

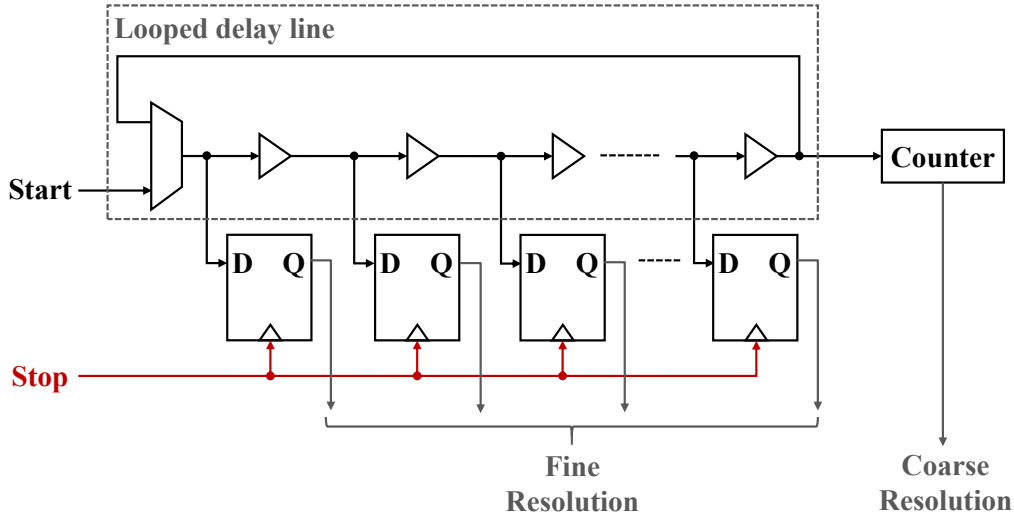


Fig. 4.5. Block diagram of the looped delay line TDC.

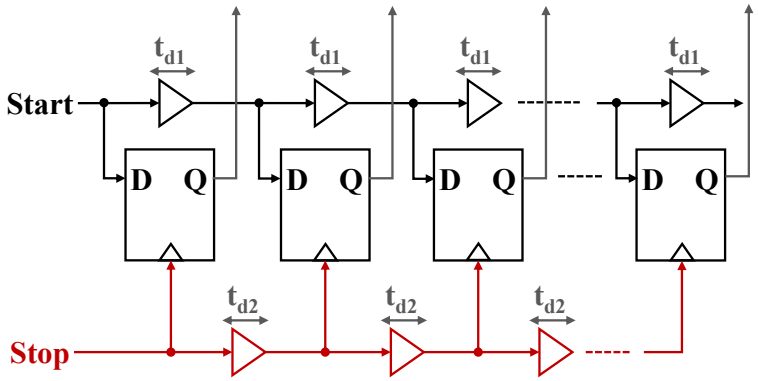


Fig. 4.6. Block diagram of the vernier TDC.

addition to that, the TDC time resolution can be further enhanced by applying passive and active phase interpolation and techniques for reducing the gate delay [154]–[157].

In the next two sections, the proposed open-loop first order noise shaped time-based ADC and the Nyquist-rate reconfigurable time-based ADC will be discussed. A high-resolution SAR-TDC is also proposed to be used as the quantizer for the time-based ADC.

4.3 The Oversampling Open-loop Time-Based ADC Employing SAR-TDC

Oversampling delta-sigma converters are a popular choice for high-resolution ADCs. Since they are built using integrators that require high intrinsic gain transistors and high supply voltages, their scalability below 90 nm node is challenging. In contrast, time-domain ADCs use the VCO as phase integrator that accumulates phase in every cycle. The accumulated phase is converted to the

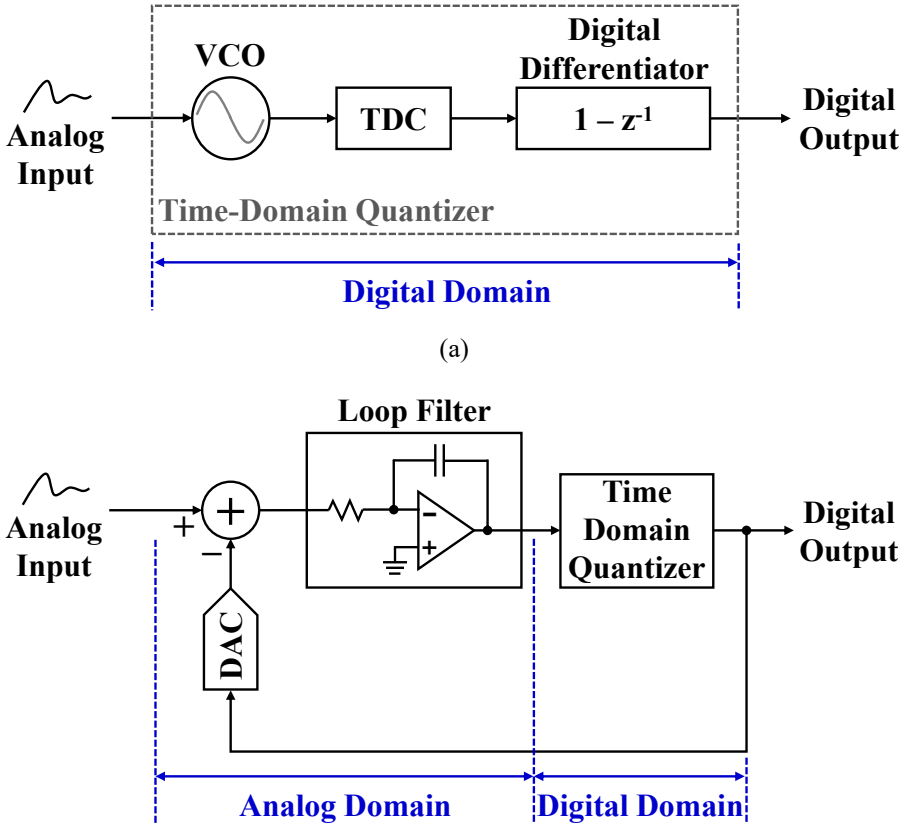


Fig. 4.7. (a) Block diagram of the oversampling open-loop time-based ADC. (a) Block diagram of the oversampling closed-loop time-based ADC.

digital domain using a TDC. The digital differentiation is then performed providing 1st order noise shaping. Due to its digital nature, the time-domain open-loop ADC architecture shown in Fig. 4.7(a) scales more graciously to deepest sub-micron nodes. However, its resolution is limited by two factors, the VCO non-linearity, and the TDC quantization noise level. The linearity of the open-loop time-based ADC can be improved using different techniques like applying pseudo-differential configuration and digital calibration [119]. But the quantization noise level is still limited by the TDC resolution and the first order noise-shaping. One possible solution is to use higher order modulator to achieve higher-order noise shaping [108] by placing the quantizer in a closed loop as shown in Fig. 4.7(b). Unfortunately, this approach requires highly linear multi-bit DAC and OTA, resulting in similar analog challenges faced by voltage-domain ADCs. Our goal is to improve the quantization noise level by enhancing the TDC resolution so that the same digital friendly open-loop time-based ADC architecture can achieve higher resolution. Improving the TDC resolution will also enable wide bandwidth oversampling time-domain ADCs.

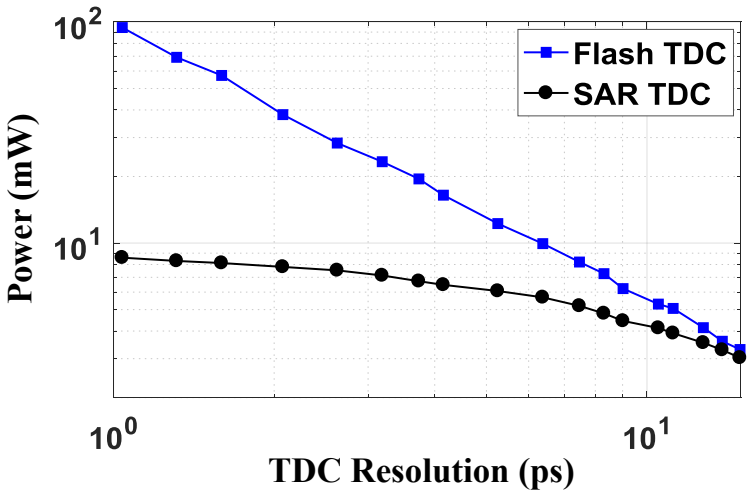


Fig. 4.8. Simulated power versus resolution for Flash and SAR TDCs.

Conventional Flash TDCs [151] employ a multiphase gated-ring oscillator (GRO) followed by a phase quantizer (PQ). The GRO is enabled during the input time period (T_{IN}). The flash TDC resolution (t_{flash}) is dictated by the GRO delay given as

$$t_{flash} = t_{GRO} = \frac{1}{N_P \times f_{GRO}} \tag{4.1}$$

where N_p is the number of GRO phases and f_{GRO} is the GRO frequency. Higher TDC resolution requires higher GRO frequency and/or more GRO phases resulting in significant power and area penalty. In other words, the flash TDC – similar to flash ADC – requires an exponentially higher number of comparisons to improve resolution (N-bit TDC will need 2^N phase quantizers). Therefore, achieving pico-second (ps) resolution will require TDC power exceeding 100 mW, simply not affordable for low power solutions. On the other hand, SAR technique can provide high TDC resolution with much lower power consumption as illustrated in Fig. 4.8.

In this section, the proposed first-order noise shaped open-loop time-based ADC is introduced. The ADC quantization noise level is improved by employing a high-resolution correlated double sampling SAR-TDC. For improved ADC linearity, a highly linear 1-bit folded VCO is utilized. The ADC linearity is further enhanced by applying foreground digital calibration [117]. First, the architecture and operation of the proposed SAR-TDC are discussed.

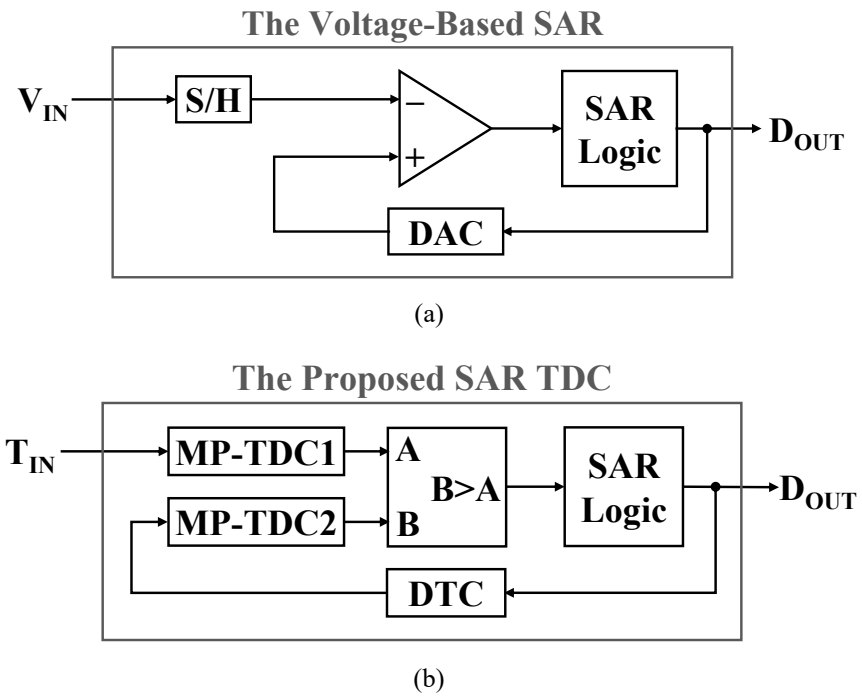


Fig. 4.9. (a) Block diagram of the voltage-based SAR. (b) Block diagram of the proposed SAR-TDC.

4.3.1 The SAR TDC Architecture and Operation

SAR-TDC is capable of providing high resolution with low power. The SAR-TDC is analogous to the voltage-based SAR. Fig. 4.9 provides the block diagrams of the conventional voltage-based SAR and the proposed SAR-TDC where the digital-to-analog converter (DAC) and comparator in the voltage-based SAR are replaced with a digital-to-time converter (DTC) and digital comparator in the SAR-TDC, respectively. The SAR-TDC employs two low-resolution multi-phase flash TDCs (MP-TDCs) to convert the time information to digital code to be used by the digital comparator. The MP-TDC comprises a multi-phase gated-ring oscillator (GRO) followed by a phase quantizer.

A couple of interesting SAR-TDCs were reported in the literature. In [149] the binary search operation is performed by adjusting the delay of both the start and stop signals resulting in long loop propagation delay and limiting the sampling rate. In addition to that, the DTC used employs 128 load capacitors resulting in a large area. Also, it consumes a large amount of power and the degraded linearity limits its performance. In [150] only the delay of the stop signal is adjusted reducing the loop delay. However, the required complicated calibration adds design complexity. In this work, the proposed SAR-TDC uses a capacitor-less DTC and provides high

TDC linearity without added complexity or loop delay while reducing the quantization noise level by employing correlated double sampling. In addition, it provides the good linearity without the need for calibration.

The proposed SAR-TDC successively employs a Coarse MP-TDC while updating the input period (T_{IN}). Its operation is based on coarse-fine architecture to quantize half the input VCO period $T_{IN}=0.5\times T_{VCO}$. During the positive half cycle, the Coarse MP-TDC1 – that is enabled by the rising edge and stopped by the falling edge of the TDC input (TDC_{IN}) – coarsely quantizes T_{IN} with time resolution t_{COARSE} dictated by the resolution of the GRO used within the MP-TDC $t_{GRO,MP\text{-}TDC}$ providing the MSBs of the SAR-TDC

$$t_{COARSE} = t_{GRO,MP-TDC} = \frac{1}{N_P \times f_{GRO}} \tag{4.2}$$

The fine resolution is attained by quantizing the time residue ($t_{RESIDUE}$) from the coarse quantization using the SAR algorithm. This is performed during the negative half cycle where T_{IN} is modulated (shrunk) in fine steps by blending additional stop edges with time step t_{FINE} as illustrated in Fig. 4.10(a). Each of the blended stop edges corresponds to a SAR code. That is, for N_S-bit SAR operation, $N_{BL}=2^{Ns}$ blended edges are required. Following a binary search algorithm, the stop edge that occurs just before the last GRO edge is selected (i.e., results in 1 LSB reduction in the MP-TDC output). The proposed SAR-TDC operation is equivalent to having a Flash-TDC with additional interpolated GRO phases as illustrated in Fig. 4.10(b). However, the generation of those interpolated phases in the GRO would significantly increase power consumption – instead, those phases are generated and selected in a decision-directed manner that simplifies the implementation.

Now, practically how this SAR operation can be achieved? The block diagram of the SAR-TDC is shown in Fig. 4.11. The digital code from the Coarse MP-TDC1 obtained during the positive half cycle serves as the reference for the SAR operation which is performed during the negative half cycle. A DTC is employed to modulate T_{IN} by providing the blended stop edges and based on the SAR Logic output one of those edges is chosen to stop the MP-TDC. The DTC is designed by delaying the TDC input by t_{COARSE} and blending N_{BL} phases with t_{FINE} time step.

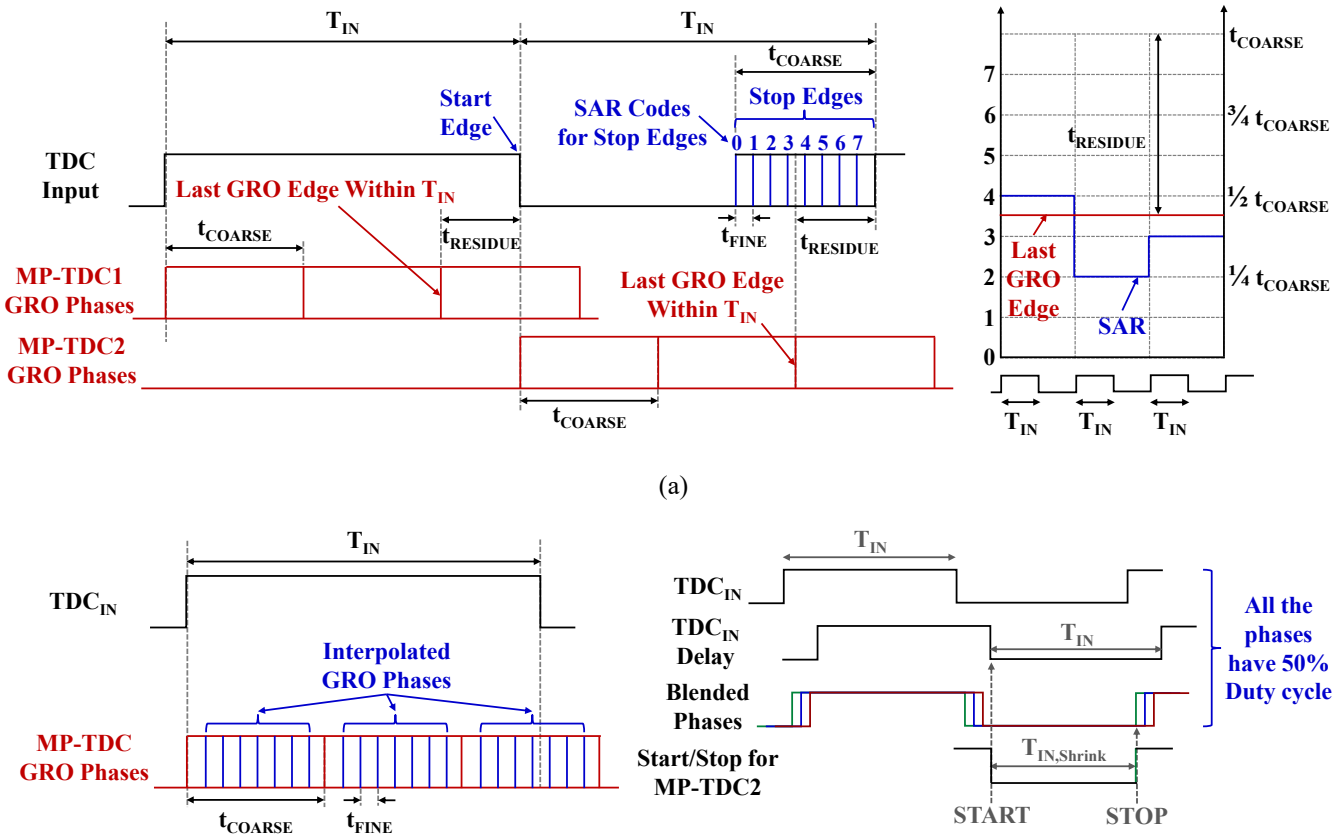


Fig. 4.10. (a) Conceptual operation of the SAR-TDC assuming 3-bit SAR operation. (b) Equivalent Flash TDC by interpolating additional number of GRO phases. (c) Shrinking the negative half cycle.

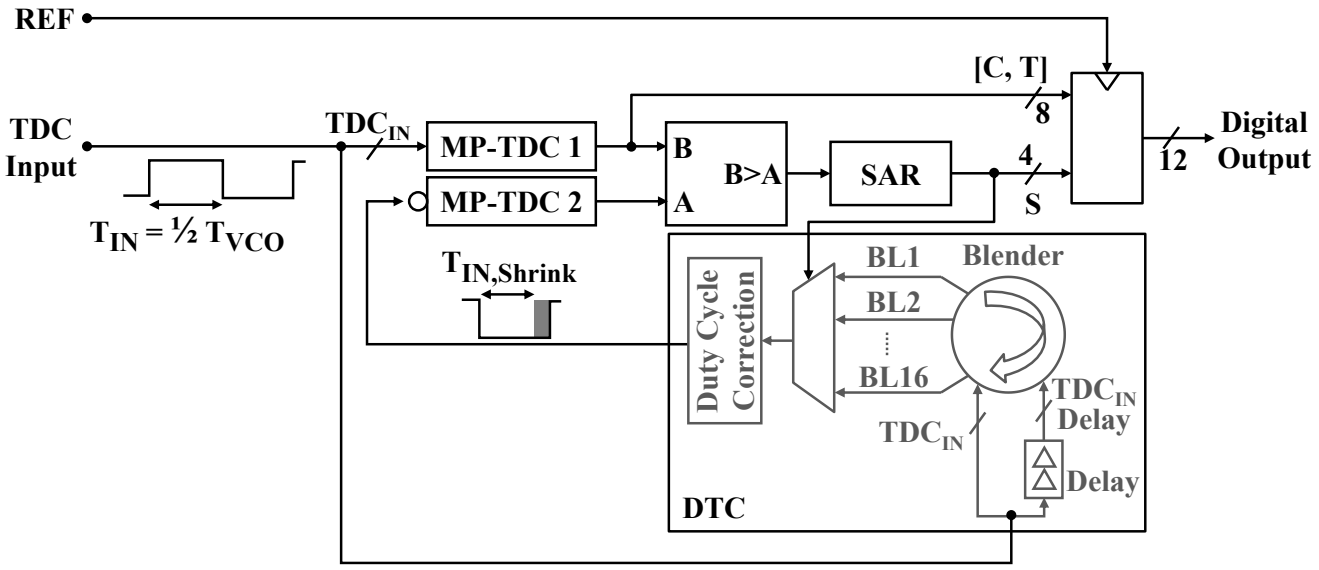


Fig. 4.11. The block diagram of the SAR-TDC.

The delay is performed using a delay circuit utilizing the same delay unit as that of the GRO. The blended edges are introduced to a MUX that is controlled by the SAR Logic output as illustrated in Fig. 4.11. The shrunk period ($T_{IN,Shrink}$) is quantized by a second MP-TDC2 (which is a duplicate of MP-TDC1) during the negative half cycle where MP-TDC2 is started by the falling edge of the delayed signal and stopped by one of the blended edges provided by the DTC as illustrated in Fig. 4.10(c). To know whether the chosen stop edge occurs before or after the last GRO edge, the outputs of MP-TDC1 (acting as the reference) and MP-TDC2 are compared each cycle using a digital comparator. The digital comparator output is fed to the SAR logic that makes a one-bit decision and the SAR output is introduced to the DTC to select a new blended edge to stop MP-TDC2 on the next cycle. For N_S-bits SAR, N_S cycles are required to obtain the LSBs provided by the SAR. Fig. 4.12 provides a detailed timing diagram describing the operation of the SAR mode. The reference clock period (T_{REF}) is given as

$$T_{REF} = N_s T_{VCO,max} + t_{d,SAR} + t_{COARSE} \cong N_s T_{VCO,max} \tag{4.3}$$

where $T_{VCO,max}$ is the maximum VCO period and $t_{d,SAR}$ is the SAR logic delay. The time resolution of the SAR-TDC (t_{SAR}) is equal to t_{FINE} and is given as

$$t_{SAR} = t_{FINE} = \frac{t_{COARSE}}{N_{BL}} \tag{4.4}$$

In voltage-domain SAR, the input voltage is sampled and held constant during the whole SAR operation that takes several cycles. However, in time domain SAR, the VCO period T_{IN} input to the SAR TDC cannot be held constant due to accumulated phase noise and supply noise that accumulates over cycles resulting in degrading the noise level. To resolve this issue time-domain correlated double sampling (CDS) is proposed which is analogous to voltage-domain CDS [158]–[160]. This is attained by the differential measurement of the input period and re-computing the MP-TDC1 output (serving as the reference for the SAR operation) each cycle to account for any change in T_{IN} due to phase noise. Each cycle, differential measurement is performed by comparing MP-TDC2 output (quantizing $T_{IN,Shrink}$) with the most recent MP-TDC1 output (quantizing T_{IN}) which cancels the accumulated noise from the 1st to the nth cycle reducing the quantization noise level and enhancing the SNR. Fig. 4.13 shows the SAR-TDC noise model from which it can be noted that time-domain CDS can eliminate VCO noise (φ_{VCO}) and provide a low-noise signal to the SAR Logic.

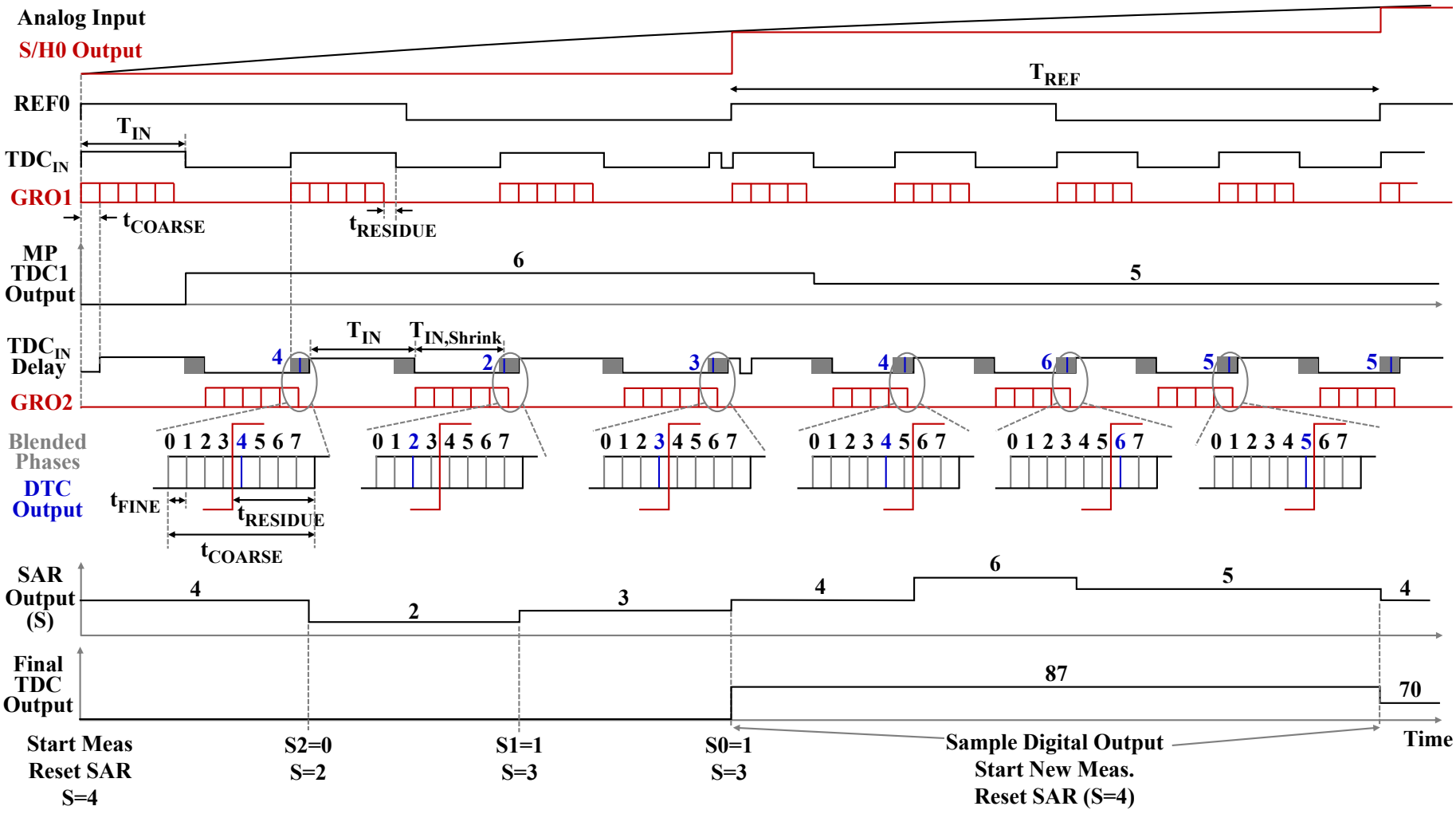


Fig. 4.12. The Timing Diagram for the SAR-TDC with 3-bit SAR operation.

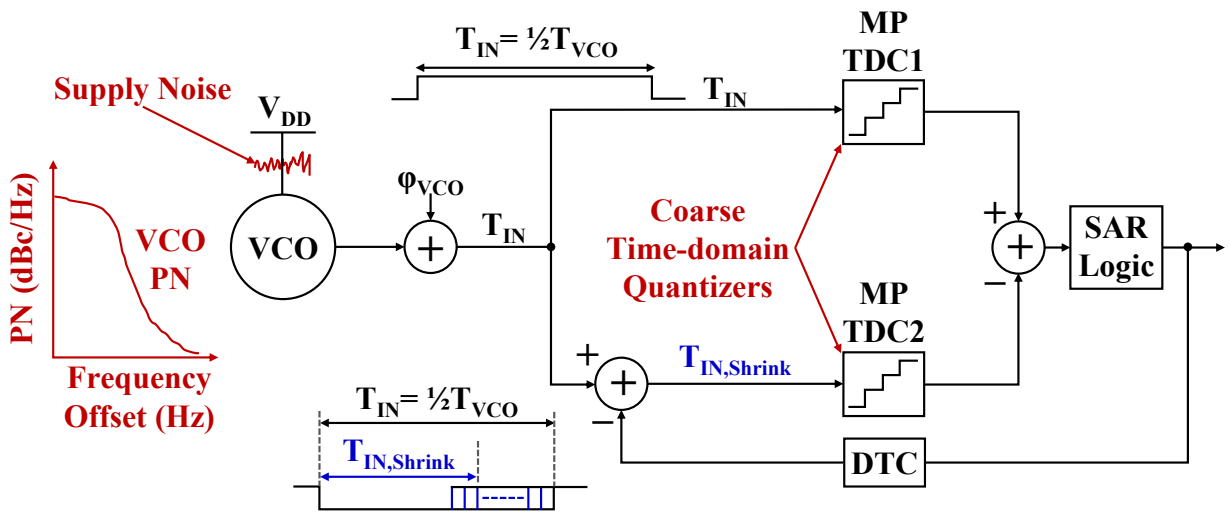


Fig. 4.13. Correlated double sampling SAR-TDC noise model.

This can be further explained as follows. First, assume a noise-less VCO. In this case, the period of the nth VCO cycle $T_{IN}(n)$ will be similar to that of the first VCO cycle $T_{IN}(1)$ since no jitter is there to modulate the VCO period. Hence, for the jitter-free VCO case, we can write

$$T_{IN}(n) = T_{IN}(1) \quad ; For\ noise - less\ VCO \tag{4.5}$$

However, this VCO is hypothetical and does not exit. Usually, the VCO suffers from some jitter. In this case, the period of the nth VCO cycle $T_{IN}(n)$ will be expressed as follows

$$T_{IN}(n) = T_{IN}(1) + \Delta T_N \quad ; For\ noisy\ VCO \tag{4.6}$$

where ΔT_N represents the amount of accumulated jitter from the first to the nth VCO cycle. This results in limiting the SNR of the ADC. This limitation can be mitigated by applying the CDS where the SAR resolution t_{SAR} is computed by comparing the input period T_{IN} and its shrunk version $T_{IN,Shrink}$

$$t_{SAR} = T_{IN}(n) - T_{IN,Shrink}(n);\ For\ Noisy\ VCO\ with\ CDS \tag{4.7}$$

where during the nth cycle both T_{IN} and $T_{IN,Shrink}$ experience approximately the same amount of jitter since they are both generated from the same VCO. This results in canceling out the accumulated noise.

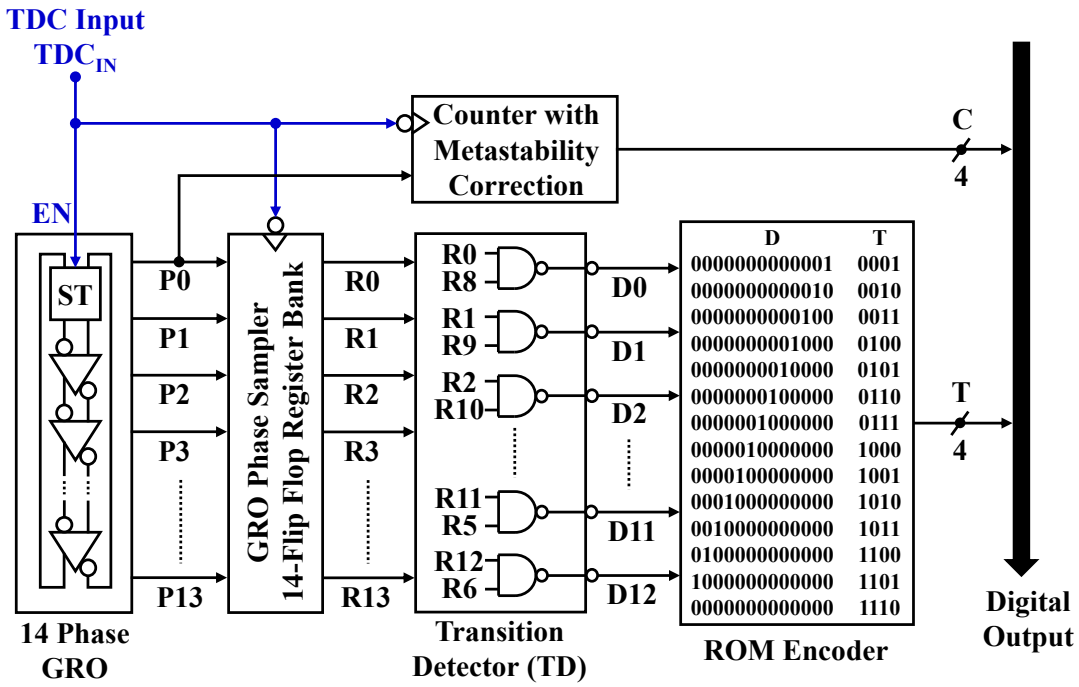
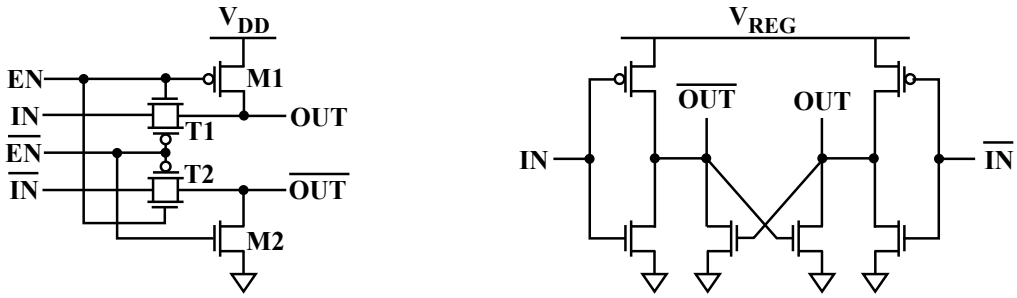


Fig. 4.14. The block diagram of the Coarse multi-phase TDC (MP-TDC).

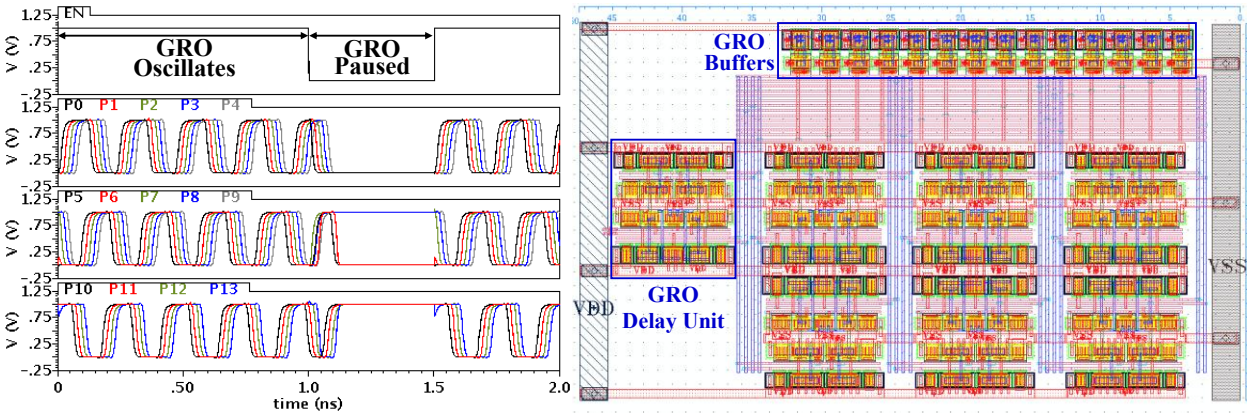
4.3.2 The SAR-TDC Implementation

The proposed SAR-TDC employs a MP-TDC, a digital comparator, a DTC and SAR logic. In this section, the implementation details of each of these blocks will be discussed. First, we shall start with the MP-TDC. The block diagram of the MP-TDC is shown in Fig. ‎4.14. It employs an N_P-phase GRO. The schematics of the start-up circuit (ST) and delay unit utilized within the GRO are illustrated in Fig. ‎4.15(a) and Fig. ‎4.15(b), respectively. The V_{REG} of the GRO delay unit is tied to V_{DD}. In conventional GRO start-up approaches, like in [138], switches are added in series with the supply where the GRO is enabled/disabled by connecting/disconnecting the supply to/from the delay units. In this case, the GRO oscillation is dependent on the internal noise build-up through the positive feedback loop where the GRO requires a couple of cycles to maintain the oscillation and reach the desired frequency. To alleviate this issue and allow the GRO to maintain its oscillation frequency directly after it is enabled, the start-up circuit shown in Fig. ‎4.15(a) is placed within the loop to provide a well-defined initial state for the GRO to start from. The post-layout simulation results of the 14-phase GRO are illustrated in Fig. ‎4.16(a). The start-up circuit operation is as follows; when EN=0, the GRO is in the ‘paused’ mode. In this mode, the transmission gates T1 and T2 break the oscillator feedback loop, while M1 and M2 connect the first GRO delay unit inputs to V_{DD} and GND, respectively to set its initial state.



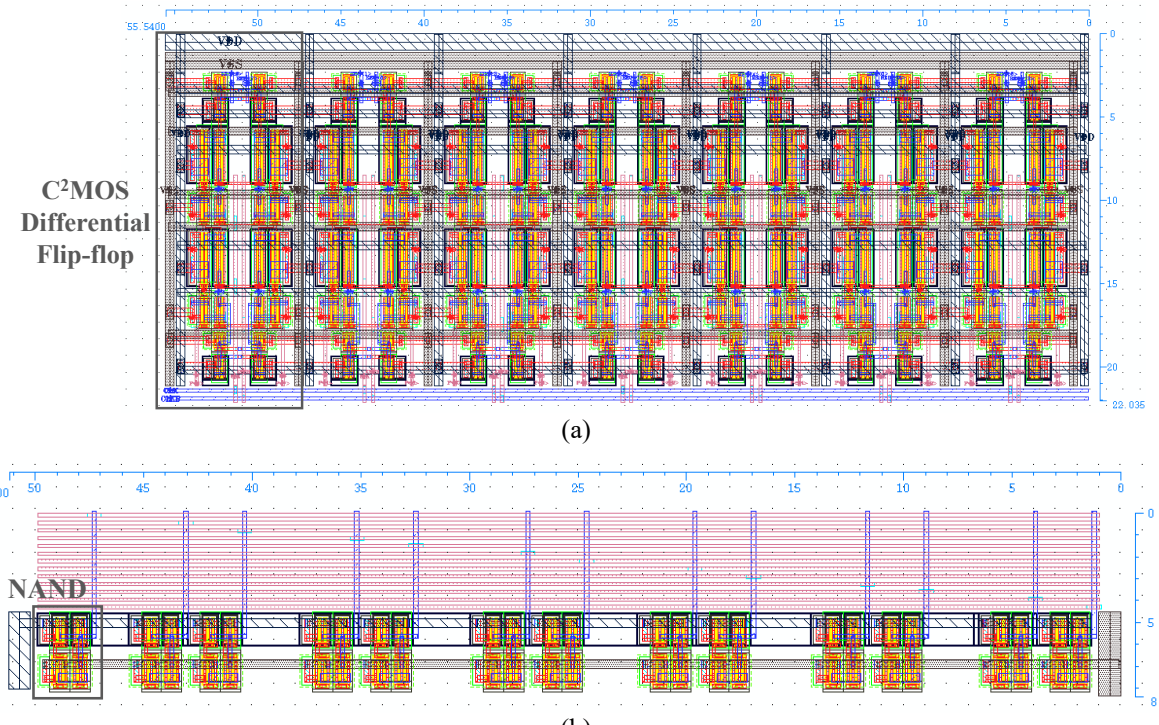
(a) (b)

Fig. 4.15. (a) The Schematic of the GRO start-up circuit. (b) The Schematic of the GRO differential delay unit.



(a) (b)

Fig. 4.16. (a) Post layout simulated GRO output phases. (b) Layout of the implemented GRO.



(a)

(b)

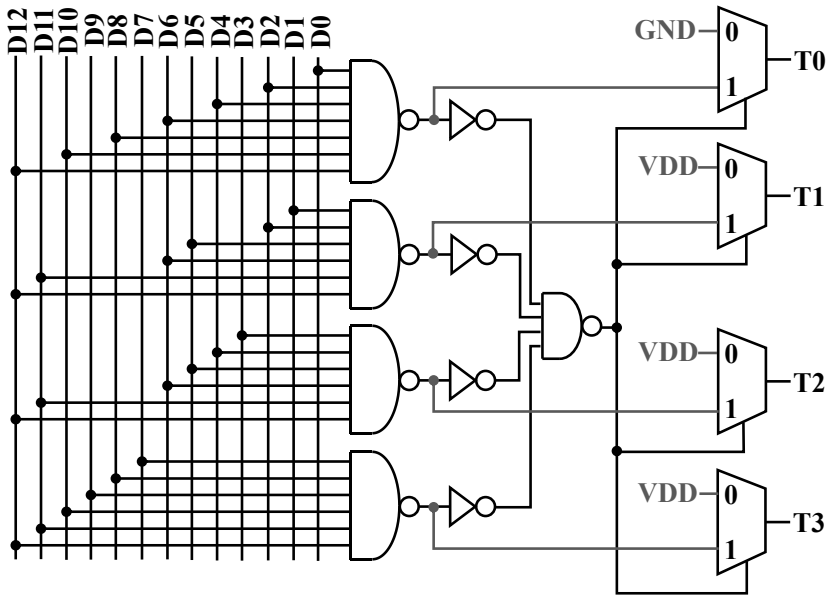
Fig. 4.17. (a) Layout of the implemented Register bank. (b) Layout of the implemented transition detector.

When EN switches to 1, T1 and T2 turn ON reconnecting the loop and wakes up the GRO from that known state. As can be noted from the obtained post-layout simulation results, the known initial state fed to the first delay unit helped GRO to sustain the oscillation once it is enabled without the need to wait for a couple of cycles to build-up the oscillation.

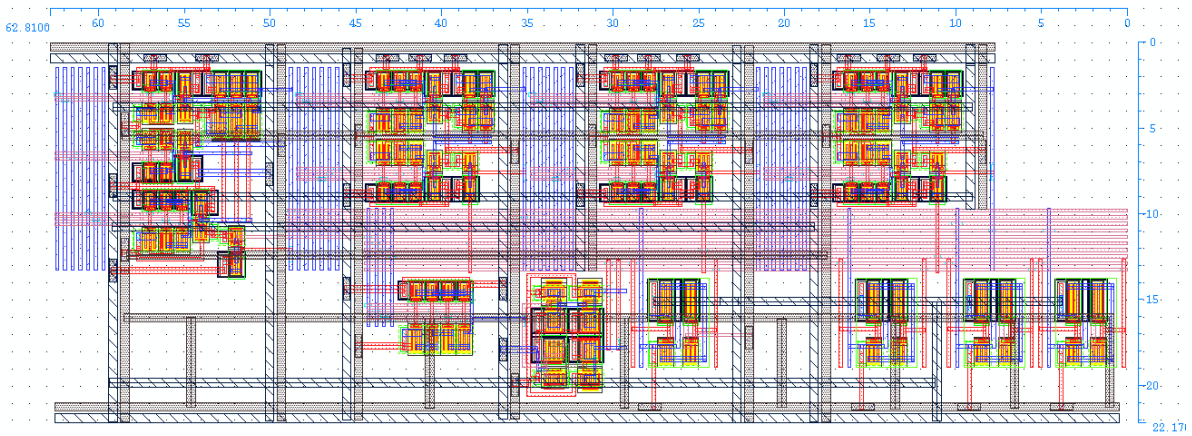
The MP-TDC operates as follows; the TDC input (TDC_{IN}) is applied to the GRO through its enable (EN) input. The GRO oscillates when EN is high. Conventionally, a counter is applied to each GRO phase for phase quantization. However, this is power inefficient. Instead only the first GRO phase *P0* is introduced to a counter providing the MSBs (*C*) of the MP-TDC. An N_P–register bank samples all the GRO phases by the falling edge of TDC_{IN} followed by a transition detector and ROM encoder to provide the LSBs (*T*) [152]. The transition detector employs N_P–*1* NAND gates to compare adjacent sampled GRO phases and detect the phase that occurs just before the GRO is stopped providing a thermometer-like code (bubble code). The inverted output of the transition detector is converted to a binary code using the ROM encoder.

The designed MP-TDC employs a 14-phase GRO using 7 differential delay unit stages, that is N_P = 14. The layout of the 4.5 GHz GRO is shown in Fig. 4.16(b) occupying an area of 47.375 µm × 26.97 µm. The layout of the register bank and transition detector are illustrated in Fig. ⁋4.17 occupying an area of 55.54 µm × 22.035 µm and 51.17 µm × 8.405 µm, respectively where the register bank is composed of 7 differential C^2MOS flip-flops. The logic used to implement the ROM encoder is provided in Fig. 4.18(a). The ROM logic is designed to realize the truth table shown in Fig. ⁋4.14 providing the LSBs of the MP-TDC. The Logical Effort method was employed to optimize the design of the 7-input NAND and 6-input NAND gates taking into account the trade-off between speed and power/area [161]. The layout of the ROM encoder is shown in Fig. 4.18(b) occupying an area of 62.81 µm × 22.17 µm.

For improved TDC performance, any error in the MSBs should be avoided. Hence, metastability correction is applied to the sampled counter output *C*. The counter output is sampled by the TDC_{IN} falling edge. Metastability occurs when either the setup or hold times of the sampling register are violated. Hold time is not a major concern since there is ½ cycle after the TDC_{IN} falling edge where the counter output is kept unchanged. Unfortunately, that is not the case with the setup time (t_{setup}). Fig. ⁋4.19 provides a couple of examples to help demonstrate when setup time failure occurs. If the last *P0* edge occurs well before the TDC_{IN} falling edge as illustrated in Fig. ⁋4.19(a), the setup time will be met. This is accompanied by large *T* output



(a)



(b)

Fig. 4.18. The ROM Encoder implementation. (a) Schematic. (b) Layout.

where $T=13$ in the shown case. The setup time starts to be violated once T becomes 1 which signifies the occurrence of a new $P0$ edge just before the TDC_{IN} falling edge as illustrated in Fig. ⁋4.19(b). The setup time is violated as long as the last $P0$ edge occurs within the t_{setup} window. As T exceeds a certain threshold (T_M) as illustrated in Fig. ⁋4.19(c), this signifies the occurrence of the last $P0$ edge outside the t_{setup} window and the fulfillment of the setup time condition The threshold T_M can be viewed as the quantized digital code representation of t_{setup} where $t_{setup} \approx T_M \times t_{flash}$. Hence, the T output can be used as a metric to determine whether or not there is an error in sampling the counter output where setup time violation occurs for $T<T_M$.

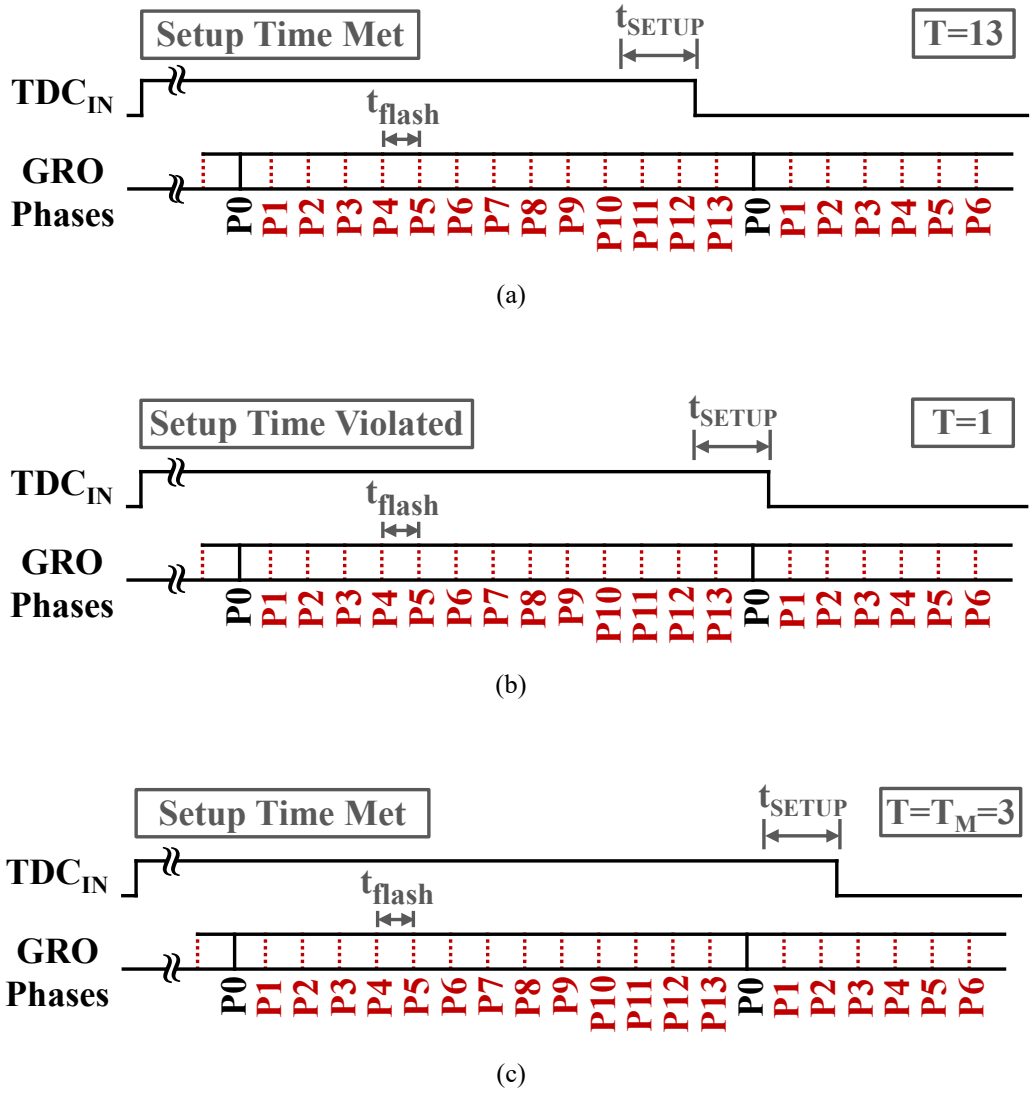


Fig. 4.19. Different scenarios for sampling the MSBs of the MP-TDC. (a) The last P0 edge occurs well outside the t_{setup} window ($T>T_M$). (b) The last P0 edge occurs within the t_{setup} window ($T<T_M$). (c) The threshold case when $T=T_M$.

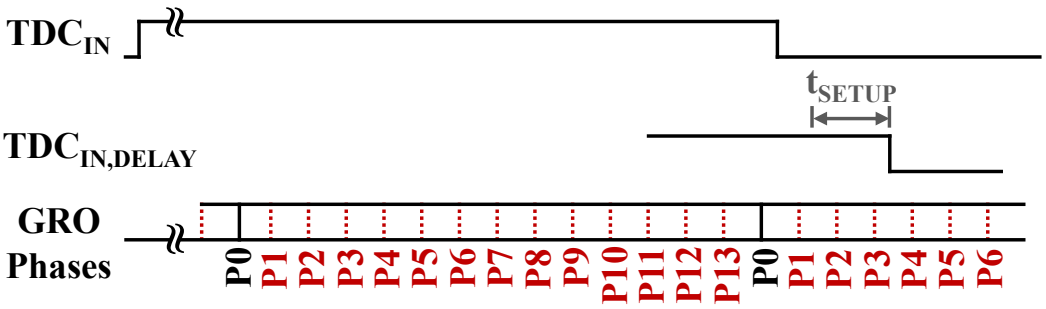


Fig. 4.20. Resolving the setup time violation issue for $T<T_M$.

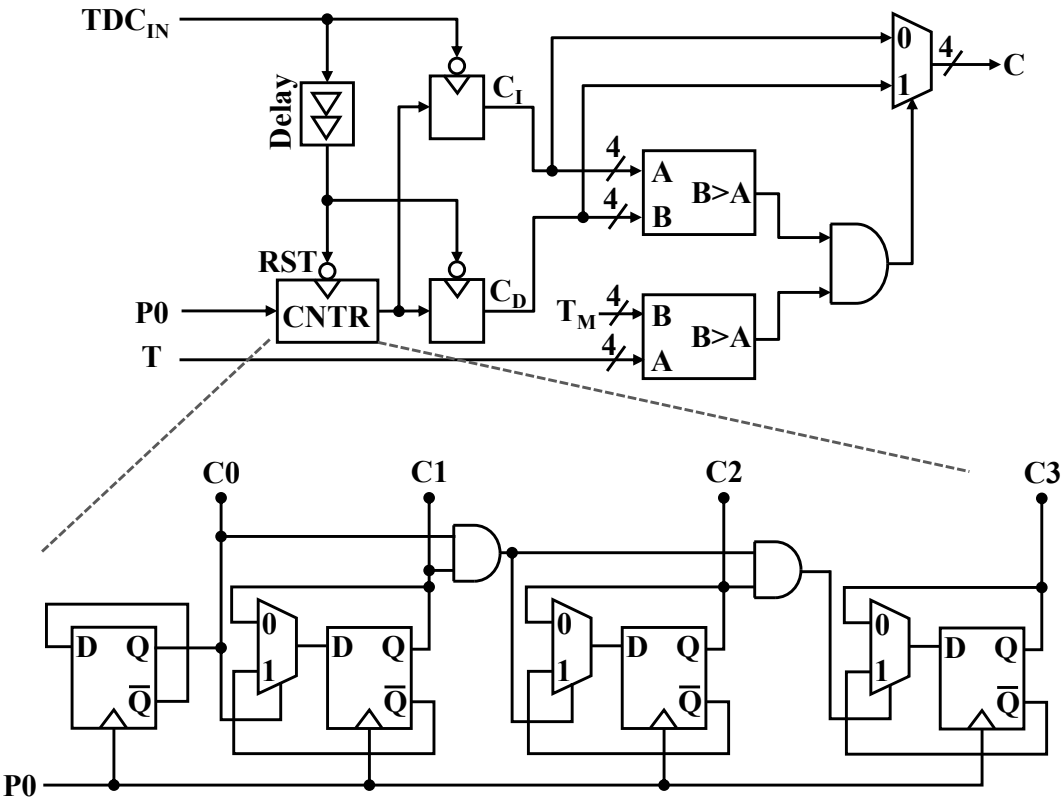


Fig. 4.21. Block diagram of the counter with metastability correction.

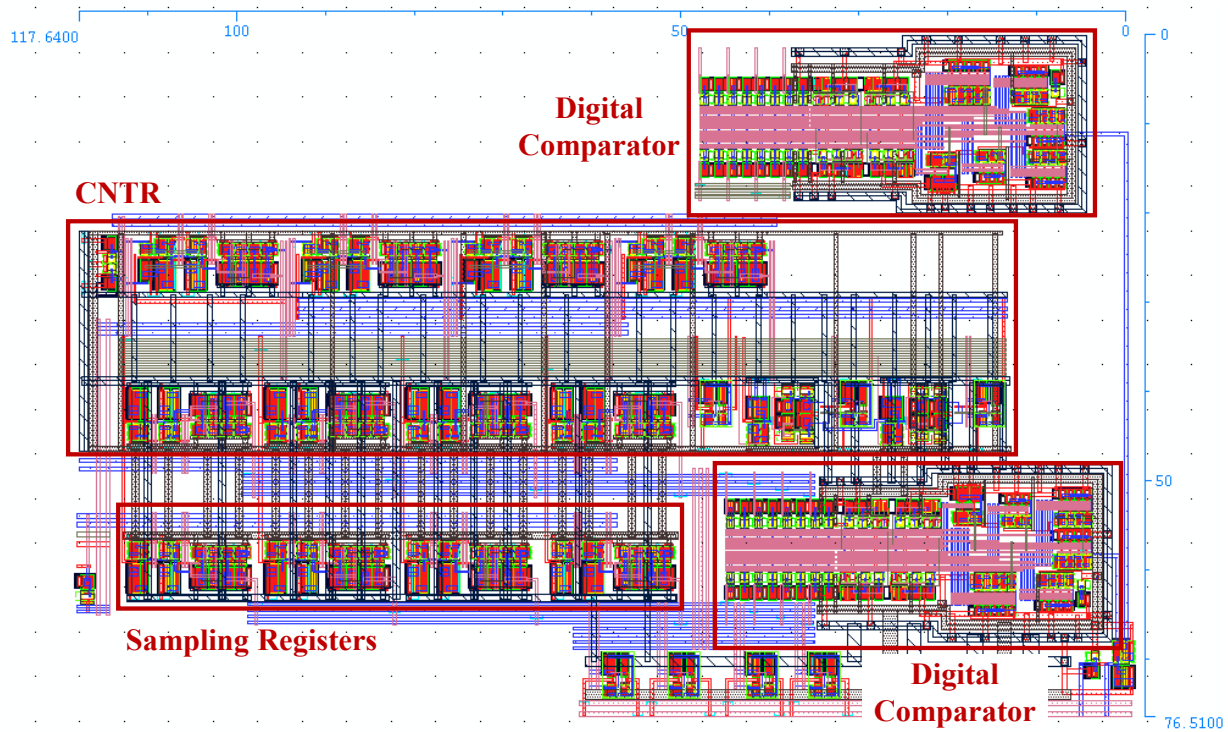


Fig. 4.22. The layout of the counter with metastability correction.

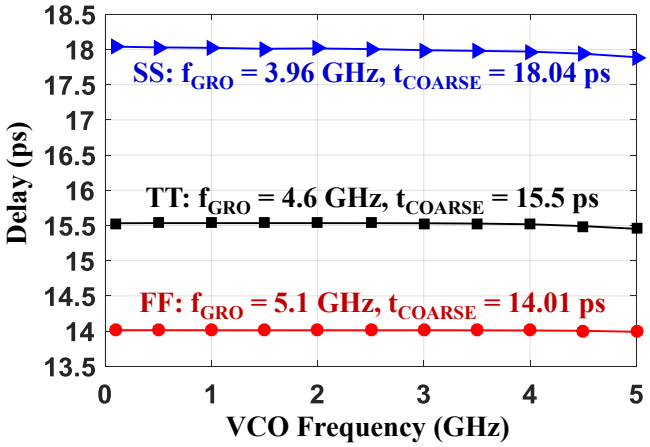


Fig. 4.23. The simulated DTC delay versus VCO frequency at different corners.

To resolve the setup time violation when $T<T_{M,}$ the counter output is sampled by a delayed version of the TDC_{IN} falling edge as illustrated in Fig. 4.20. The block diagram of the counter with metastability correction is shown in Fig. 4.21 where the counter output is sampled by the TDC_{IN} falling edge and a delayed version of it providing the C_I and C_D outputs, respectively. The sampled values C_I and C_D are compared and also the T output is compared with T_M using digital comparators. If $T<T_M$ and $C_I<C_D$, then C_D is selected, otherwise C_I is selected. The layout of the counter is illustrated in Fig. 4.22 occupying an area of 117.64 µm × 76.51 µm.

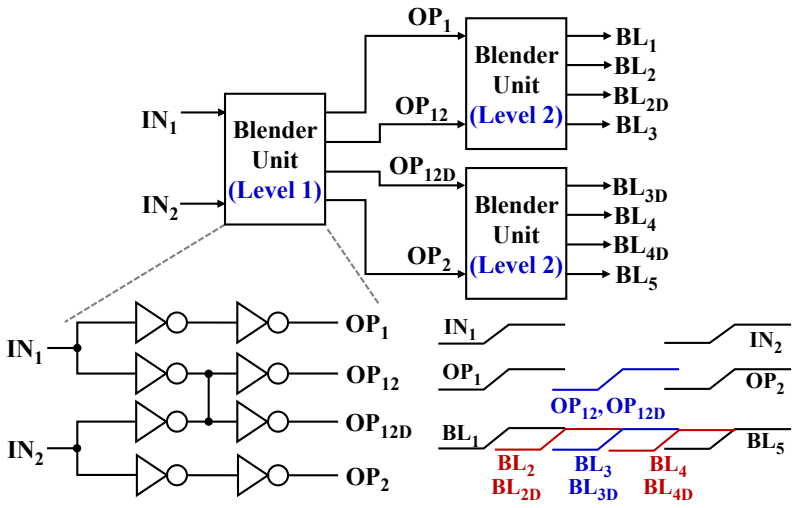
Next, the implementation of the DTC will be discussed. The MP-TDC provides resolution of t_{COARSE} set by the delay unit of the GRO. The TDC input is required to be delayed with the same t_{COARSE} for the blending operation. This is accomplished by using the same delay unit employed in the GRO with replica loading in the *TDC* input path to generate the adjacent edges for blending. As a result, when the GRO frequency is calibrated, the same capacitor trim code is used for the delay element. Note that this delay is also a function of the input frequency. To keep the high linearity levels, the variation in the obtained delay across the VCO tuning range should be much less than the SAR-TDC resolution. Fig. 4.23 provides a plot of the post-layout simulated delay at TT, FF and SS corners as the VCO frequency varies from 100 MHz to 5 GHz showing that the delay variation is less than 0.12 ps.

The blender circuit – which is basically a phase interpolator – used within the DTC is based on tree implementation architecture. Fig. 4.24(a) shows the block diagram of a two-level 4-phase blender circuit that utilizes duplicate paths to ensure the symmetry of the blended phases

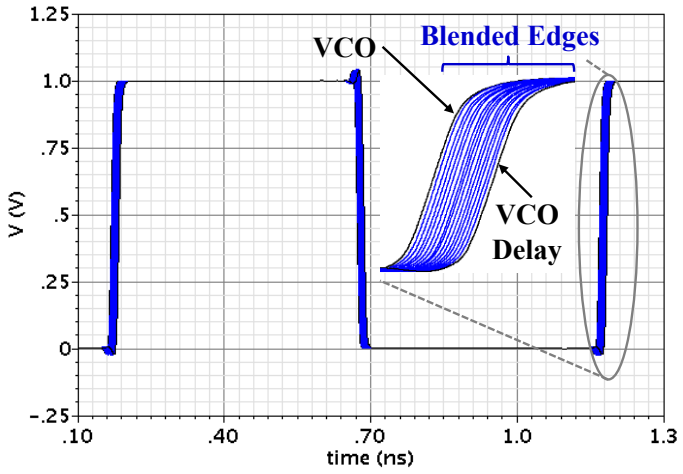
[162],[163]. For the blender unit cell, inverters $I_{1\text{-}4}$ are sized as $(W/L)_{PMOS}$ = (4µm/60nm) and $(W/L)_{NMOS}$ = (2µm/60nm) while inverters $I_{5\text{-}8}$ are sized as $(W/L)_{PMOS}$ = (8µm/60nm) and $(W/L)_{NMOS}$ = (4µm/60nm). For blending more phases, more levels can be added to the blender tree. The implemented SAR-TDC utilizes 4-bit SAR employing a 4-level 16-phase blender. The linearity of the DTC is mainly influenced by the symmetry of the blended output phases (i.e., the linearity of the blender). The post-layout simulated phases of the 16-phase blender are introduced in Fig. 4.24(b) and the blender (or equivalently the DTC) linearity is illustrated in Fig. 4.24(c) over the TT/SS/FF process corners showing maximum DNL/INL of 0.16/0.31, 0.13/0.18, 0.22/0.38 LSB for the TT, SS, and FF corners, respectively. It is obvious from the obtained results that the blender (and accordingly the DTC) achieves good linearity and does not require any calibration.

Monte Carlo Simulations were performed on the DTC over 500 runs and the effect of the mismatch on the DTC linearity is reported in Fig. 4.25 showing mean/standard deviation of 0.14/0.026 LSB and 0.321/0.052 LSB for the DNL and INL, respectively. The effect of the DTC mismatch on the overall SAR-TDC linearity was also investigated. Fig. 4.26 shows a plot of the SAR-TDC INL versus the percentage mismatch in the DTC blended edges. From the obtained results it can be concluded that for DTC mismatch < 30%, the SAR-TDC can attain better than 1 LSB INL.

After the blending operation, the edges at the blender output are slightly slanted due to the interpolation operation. This results in a slight change in the duty cycle of the blended phases. To restore the duty cycle back to 50% a duty cycle correction circuit (DCC) is added after the blender. The schematic of the digitally-controlled DCC circuit is illustrated in Fig. ⁋4.27(a). The duty cycle is adjusted by digitally controlling the rise and fall times of the two-stage inverters constituting the DCC using the digital bits (D_0 – D_{15}). Fig. ⁋4.27(b) illustrates the post-layout simulated duty cycle for each of the 16 blended phases. The digital code D<15:0> is set by monitoring the unshrunk negative half cycle. This is performed by hardcoding the MUX present within the DTC to select the last edge from the blender. Then the digital code D<15:0> is adjusted till both MP-TDC1 (quantizing the unshrunk positive half cycle) and MP-TDC2 (quantizing the unshrunk negative half cycle) become equal which signifies a 50% duty cycle. The layout of the DTC is illustrated in Fig. ⁋4.28 occupying an area of 136.46 µm × 82.99 µm.



(a)



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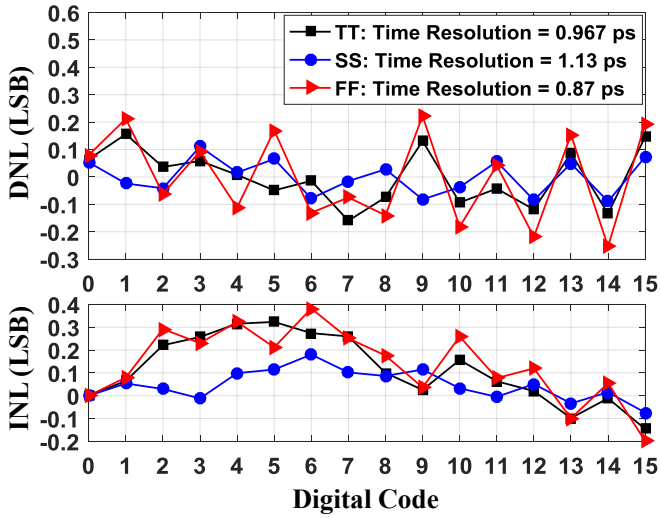


(c)

Fig. 4.24. (a) Schematic of a 2-level 4-phase blender. (b) Post layout simulation of the 4-level 16-phase blender employed for the 4-bit SAR operation. (c) DNL/INL plot for the 16-phase blender over the TT/SS/FF corners.

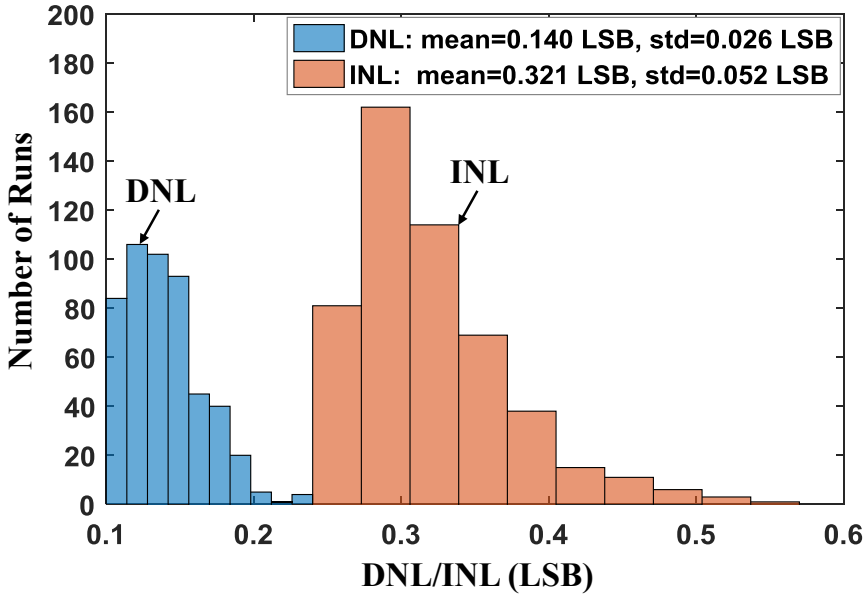


Fig. 4.25. Monte Carlo Simulation of the DTC over 500 runs.

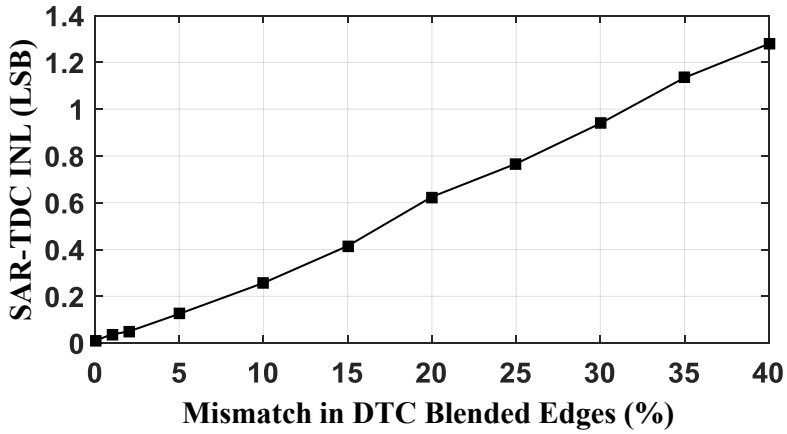


Fig. 4.26. Simulated SAR-TDC INL versus percentage mismatch in the DTC blended edges.

The SAR logic was implemented using the sequencer – coder technique [164]. It employs set/reset differential C^2MOS flip-flops as illustrated in Fig. 4.29(a) and controlled by the digital comparator output bit (M). The layout of the SAR logic is illustrated in Fig. 4.29(b) occupying an area of 120.71 µm × 23.305 µm.

Finally, the schematic and layout of the digital comparator are shown in Fig. 4.30 occupying an area of 43.53 µm × 19.95 µm. The counter is excluded from MP-TDC2 to save area/power and the comparison between MP-TDC1 and MP-TDC2 outputs is performed between their *T* outputs with the compare logic accounting for the *T* code rotation.

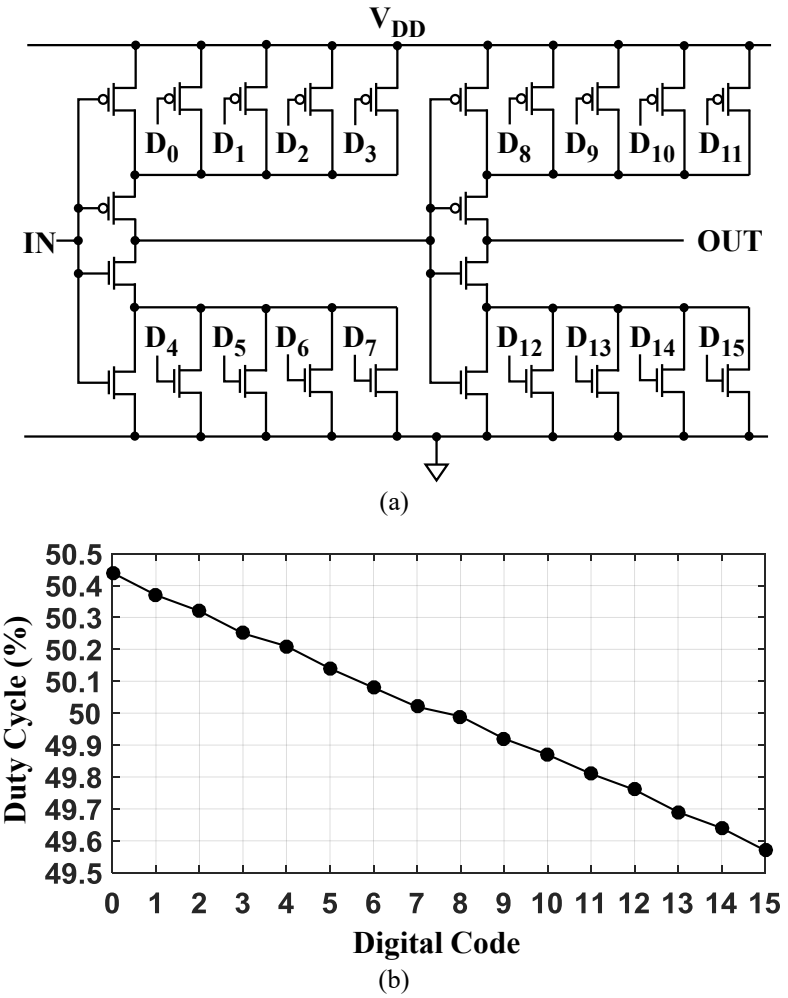


Fig. 4.27. (a) Digitally-controlled duty cycle correction circuit schematic. (b) The post layout simulated duty cycle for the 16-phases of the blender.

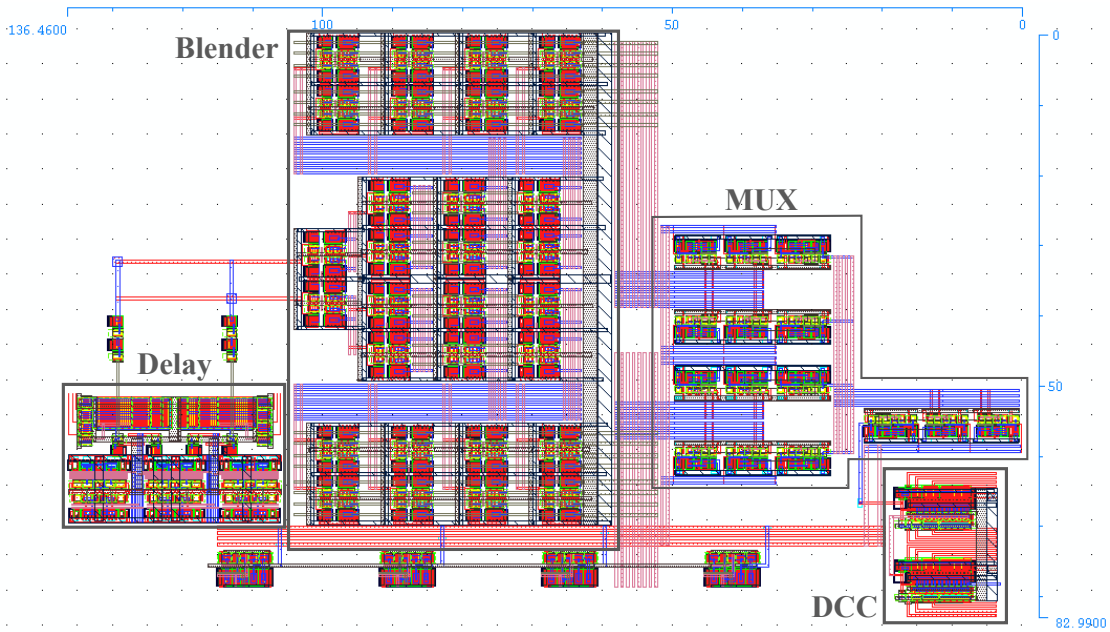
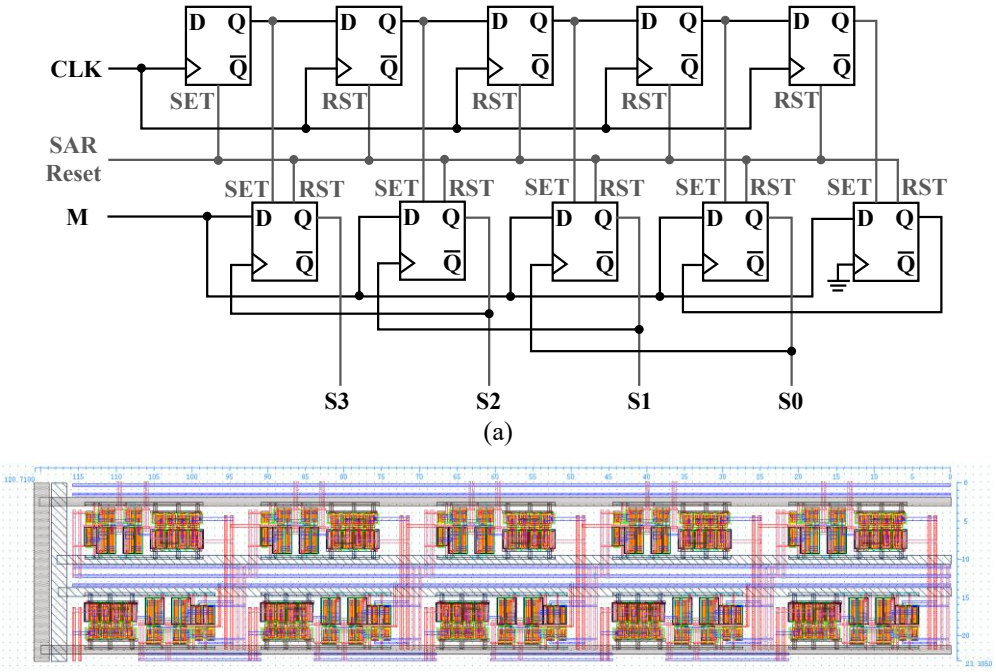


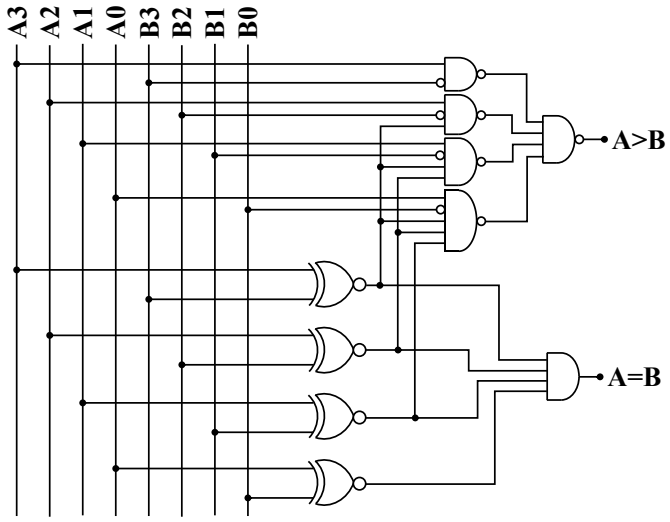
Fig. 4.28. Layout of the implemented DTC.



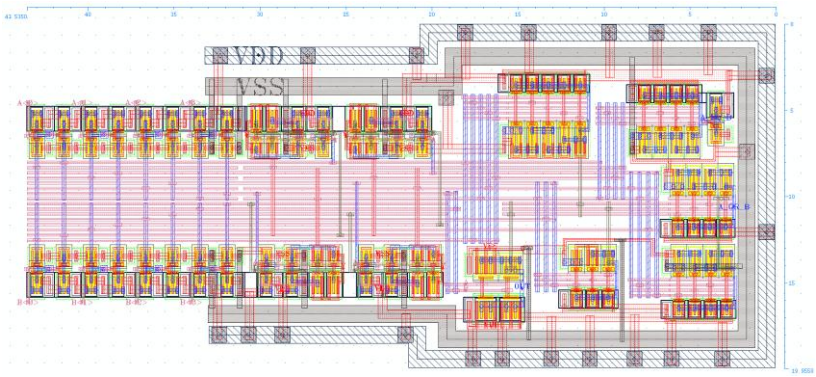
(a)

(b)

Fig. 4.29. SAR Logic implementation. (a) Schematic. (b) Layout.

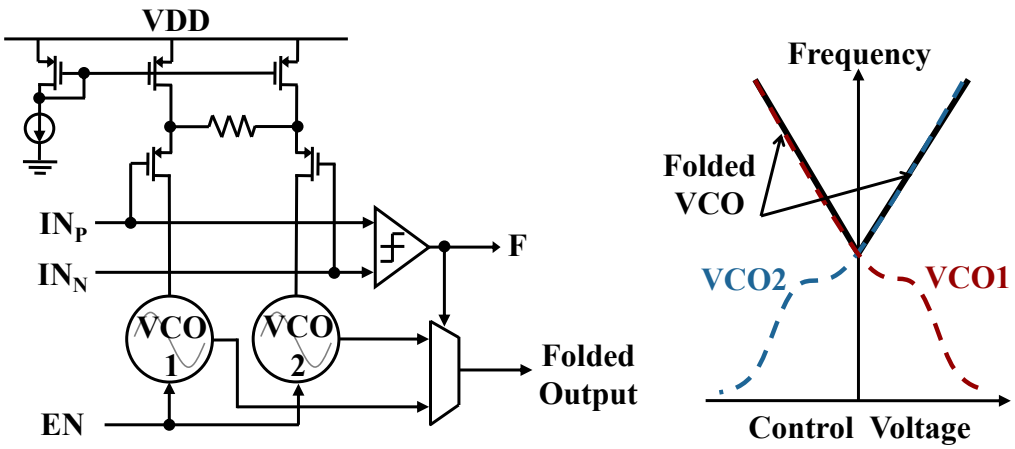


(a)

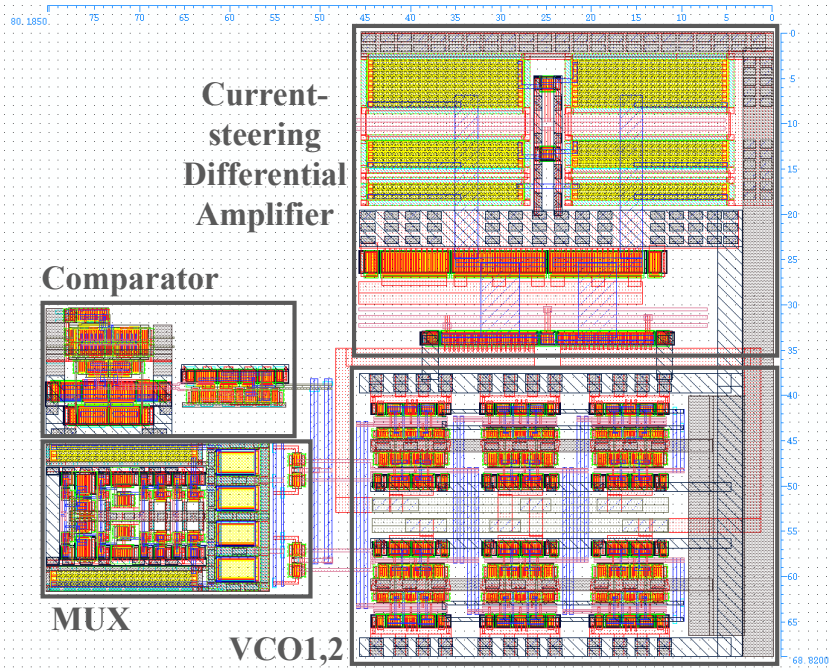


(b)

Fig. 4.30. Digital comparator implementation. (a) Schematic. (b) Layout.



(a) (b)



(c)

Fig. 4.31. The Folded-VCO implementation. (a) Schematic. (b) Folded VCO characteristics. (c) Layout.

4.3.3 The Folded VCO and ADC linearization

VCO Linearity is the bottleneck for obtaining high SNDR from time-based ADCs. Fig. 4.31(a) shows the schematic of the proposed 1-bit folded VCO for enhancing the VCO linearity. The folded VCO comprises two duplicate three stage VCOs that employ the same start-up and differential delay units as the GRO. The folded VCO operates as follows. The differential input is converted to differential current through the transconductance stage that feeds the differential

VCOs, VCO1 and VCO2 through their V_{REG} nodes. This results in the two VCOs having complementary tuning characteristics. A pseudo-differential ADC can be implemented by applying the outputs of VCO1 and VCO2 to two TDCs and subtracting their outputs. However, for larger input signal swing, the VCO will be forced to operate in the non-linear region part of its tuning characteristics which would make the voltage to time conversion operation non-linear and hence degrades the SNDR of the ADC. Actually, the purpose this configuration is not to have a pseudo-differential ADC, but to implement a folded VCO for enhanced VCO linearity. This is performed by selecting only the linear portion of the VCO tuning characteristics through a differential MUX where as illustrated in Fig. 4.31(b) we are switching between VCO1 and VCO2 to utilize the linear portion of their transfer characteristics. The MUX is controlled by the output of a 1-bit comparator that takes its decision based on the value of the analog input. Accordingly, the selection between the two VCO outputs is performed resulting in the Up-fold VCO tuning curve shown in Fig. 4.31(b). The output of the 1-bit comparator (F) also serves as the MSB of the ADC. The folding technique encounters two main advantages; (1) each of VCO1 and VCO2 operates over smaller control voltage range which can be easily linearized by properly designing the VCO parameters. (2) The folded VCO has higher minimum VCO frequency compared to VCO1 and VCO2 alone, hence resulting in higher sampling rates. The folded VCO provides a differential output as both VCO1 and VCO2 are differential utilizing a differential delay unit and the MUX utilized within the folded VCO is also differential. The folded VCO linearity is further enhanced by improving the linearity of the differential amplifier by adding a source degenerative resistance. The folding operation does not suffer from any non-linearity since it's performed using only 1-bit. The layout of the folded VCO is illustrated in Fig. 4.31(c) occupying an area of 80.185 μm × 68.82 μm

The folding operation helps reduce the VCO non-linearity. However, it does not completely eliminate it. To get rid of the remaining VCO nonlinearity, foreground digital calibration [117] is applied as illustrated in Fig. 4.32. It is also worth to be noted that, the ADC output is inversely proportional to the analog input due to the inverse relation between the VCO output period and its input. This inverse operation is reversed using the foreground digital calibration.

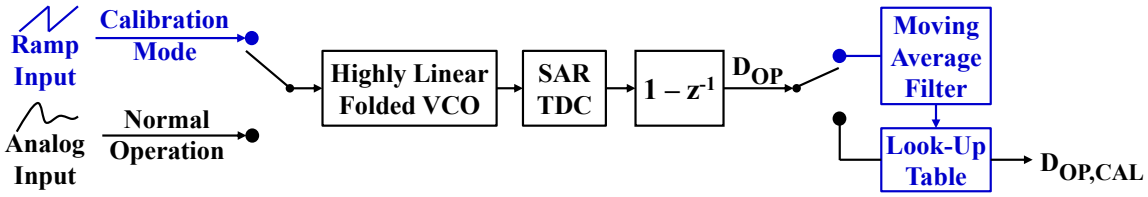


Fig. 4.32. ADC Linearization using foreground digital calibration

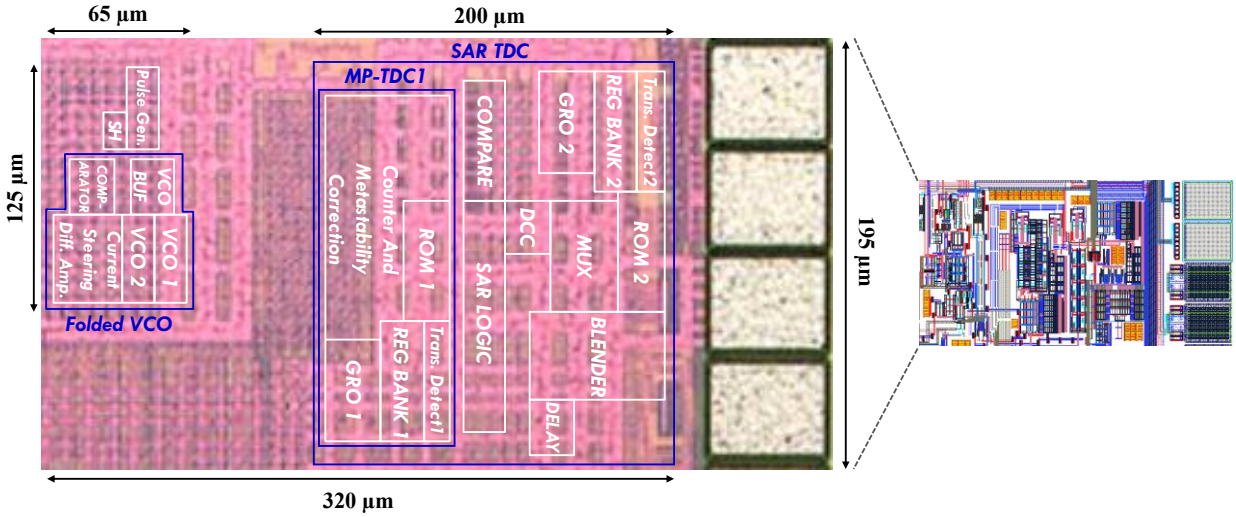
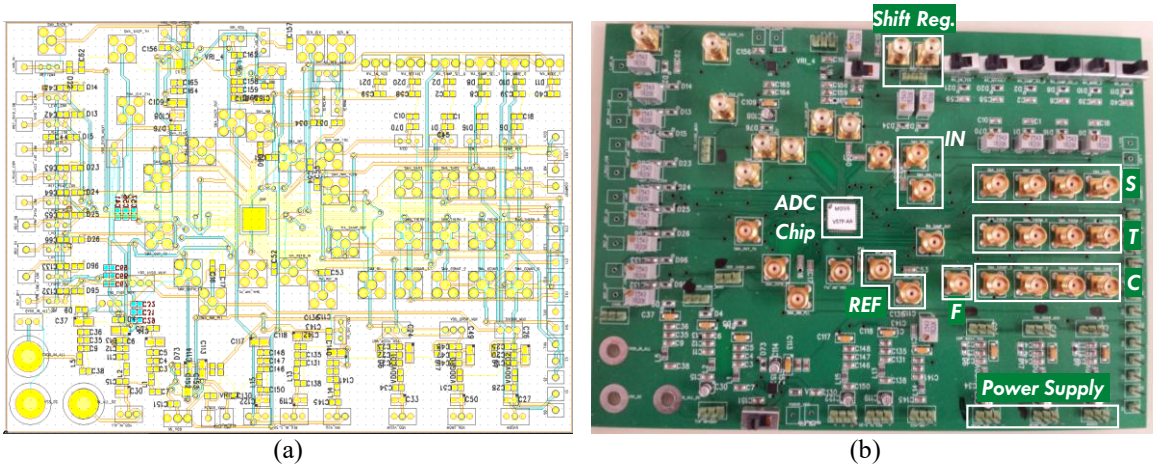


Fig. 4.33. Die micrograph of the oversampling SAR-TDC based open-loop time-domain ADC.

Table 4.1
Power and Area Breakdown for the oversampling open-loop SAR-TDC based time-domain ADC

	Power (mW)	Area (µm^2)
MP-TDC1	3.53	178.41 × 83.13
MP-TDC2	2.26	120.7 × 67.89
Digital Comparator	0.027	43.53 × 19.95
SAR Logic	1.152	120.71 × 23.305
DTC	1.076	136.46 × 82.99
Folded VCO	3.6	80.185 × 68.8



(a) (b)

Fig. 4.34. Testing PCB board for the time-based ADC. (a) PCB layout. (b) PCB with the fabricated chip mounted.

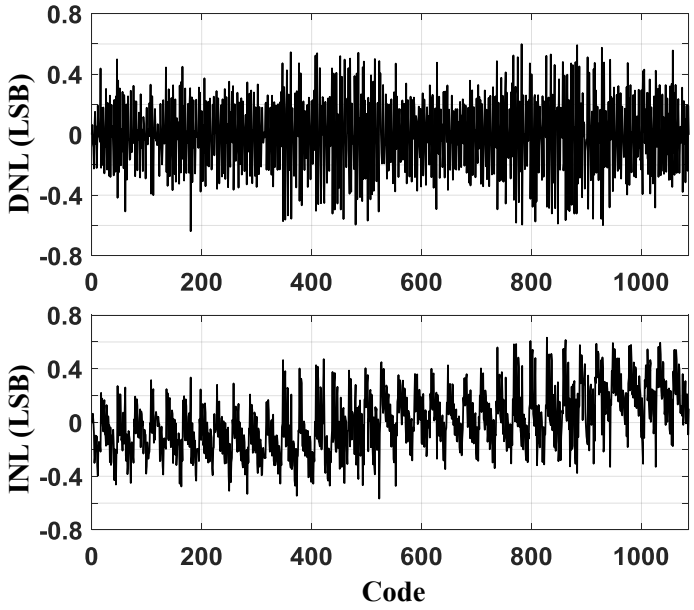


Fig. 4.35. Measured DNL/INL of the standalone 100MS/s 10-bit TDC.

Table 4.2
Comparison with State-of-the-art TDCs

	[150]	[149]	[165]	[166]	[146]	This Work
Process (nm)	65	350	65	14	65	65
Type	SAR	SAR	Two-Step	Phase Interpolation	Pipeline	SAR
Time Resolution (ps)	9.77	1.22	0.63	1.17	1.12	1.15
Resolution N_{bits} (bits)	10	13	9	10	9	10
Rate (MS/s)	80	12.5	120	100	250	100
DNL/INL(LSB)	1.35/2	N/A	0.98/3.01	0.8/2.3	0.6/1.9	0.64/0.65
Supply (V)	1.2	3.3	1.2	0.6	1	1
Power (mW)	9.6	33	3.73	0.78	15.4	8.05
N_{linear} (Bits)	8.4	N/A	6.99	8.28	7.57	9.28
FoM (pJ/conv)	0.355	N/A	0.244	0.025	0.325	0.129
Area (mm^2)	0.11	0.79	0.064	0.036	0.14	0.039

4.3.4 Measurement Results

A prototype of the proposed SAR-TDC based time-domain ADC was fabricated in the TSMC 65 nm CMOS process occupying an active area of 0.047mm^2. The die micrograph is shown in Fig. 4.33. The SAR-TDC was implemented using a 14-phase differential 4.5GHz GRO and 16-phase blender circuit for 4-bit SAR (equivalent to a Flash-TDC with 224 GRO phases).

The SAR-TDC consumes a total of 8.05mW from 1V supply and with the folded-VCO consumes 3.6mW from 1.2V supply resulting in overall ADC power of 11.65 mW. The power and area breakdown of the ADC are provided in Table 4.1. A two-layer FR-4 PCB was designed

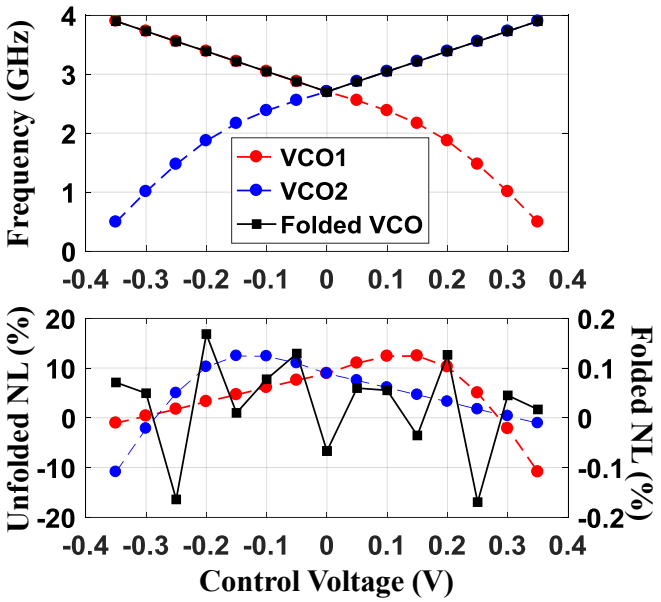


Fig. 4.36. The measured Unfolded/Folded VCO tuning characteristics and linearity.

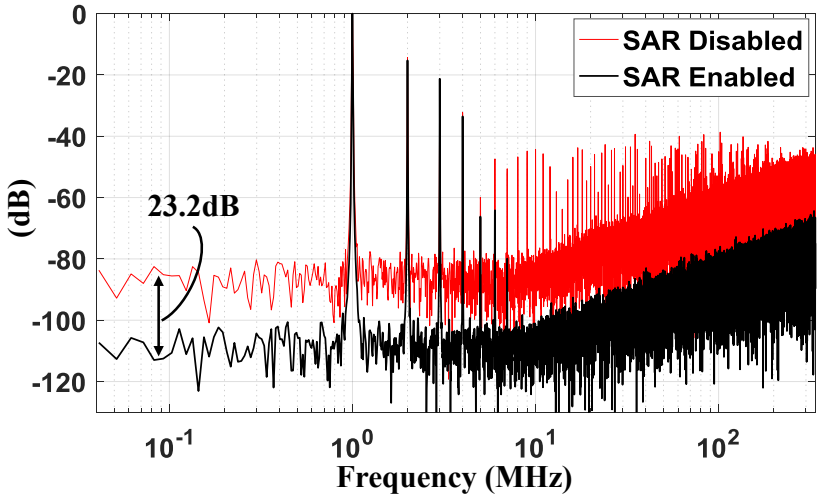


Fig. 4.37. The Measured Output Spectrum of the 675 MS/sec ADC in response to a -4.68 dBFS 1 MHz input sinusoid for the Unfolded ADC with SAR enabled and disabled.

for testing the ADC as shown in Fig. 4.34. The measured *Coarse MP-TDC* resolution is 17ps and the overall *SAR-TDC* measured resolution is 1.15ps. Fig. 4.35 provides the measured DNL-INL plot of the stand-alone TDC operating at 100MS/s and providing 10-bit resolution showing maximum DNL/INL of 0.63/0.64 LSB. The factors affecting TDC linearity are the asymmetry in GRO phases, asymmetry of blended phases and mismatch between MP-TDC1 and MP-TDC2 which is resolved by the duty cycle correction circuit. Table 4.2 provides comparison with state-of-the-art TDCs [146], [149], [150], [165], [166] showing that the proposed TDC achieves good linearity, resolution and FoM with low power compared to previously reported TDCs.

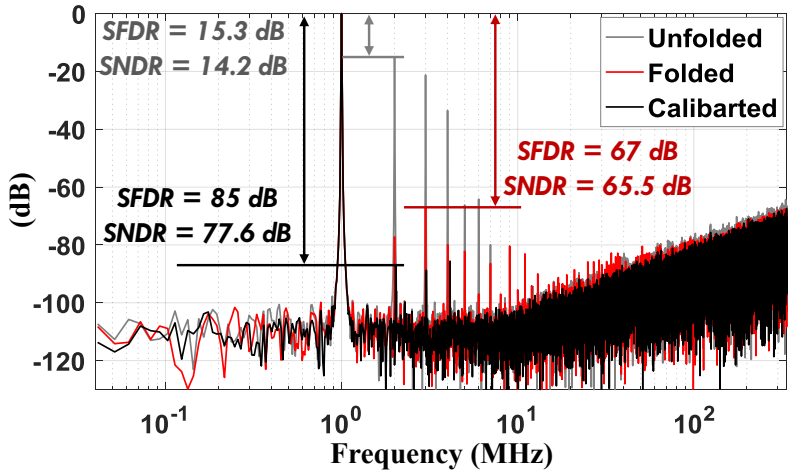


Fig. 4.38. The Measured Output Spectrum of the 675 MS/sec ADC in response to a -4.68 dBFS 1 MHz input sinusoid for the Unfolded/Folded/Calibrated ADC with SAR enabled.

The TDC effective resolution N_{linear} and figure-of-merit (FoM) are given as

$$N_{Linear} = N_{bits} - log_2(INL + 1) \tag{4.8}$$

$$FoM = {Power}/{f_s \times 2^{N_{Linear}}} \tag{4.9}$$

where f_s is the sampling rate and N_{bits} is the TDC resolution. Applying the folding technique helps improve the VCO linearity. The measured tuning curves of the two-three stages unfolded VCOs and the folded output are illustrated in Fig. 4.36 showing unfolded VCO maximum non-linearity of 12.43%. The folded VCO frequency ranges from 2.71 GHz to 3.95 GHz with 0.17% maximum non-linearity showing significant linearity improvement over its unfolded counterpart. VCO non-linearity is computed as $NL(\%)=100\times(f_{NL}-f_L)/f_{tuning}$ with f_{NL} is the frequency of the nonlinear VCO at a given input control voltage, f_L is the frequency of the linearized version of the VCO at the same input control voltage and f_{tuning} is the VCO tuning range.

The ADC sampling rate is one-fourth the minimum folded VCO frequency since 4-bit SAR operation is employed. The main advantage of using SAR over Flash TDC is its high resolution which results in lowering the noise floor of the time-based ADC. This is verified by Fig. 4.37 showing the measured FFT of the unfolded 675MS/s ADC output in response to a -4.68 dBFS 1 MHz input sinusoid with the SAR disabled (only the flash MP-TDC1 is employed) and enabled (the overall SAR-TDC is in action) showing 23.2 dB SNR improvement due to SAR operation. Theoretically, the improvement in the noise floor due to the additional 4 SAR bits is $6.02\times log_2(2^4)=24.08$ dB.

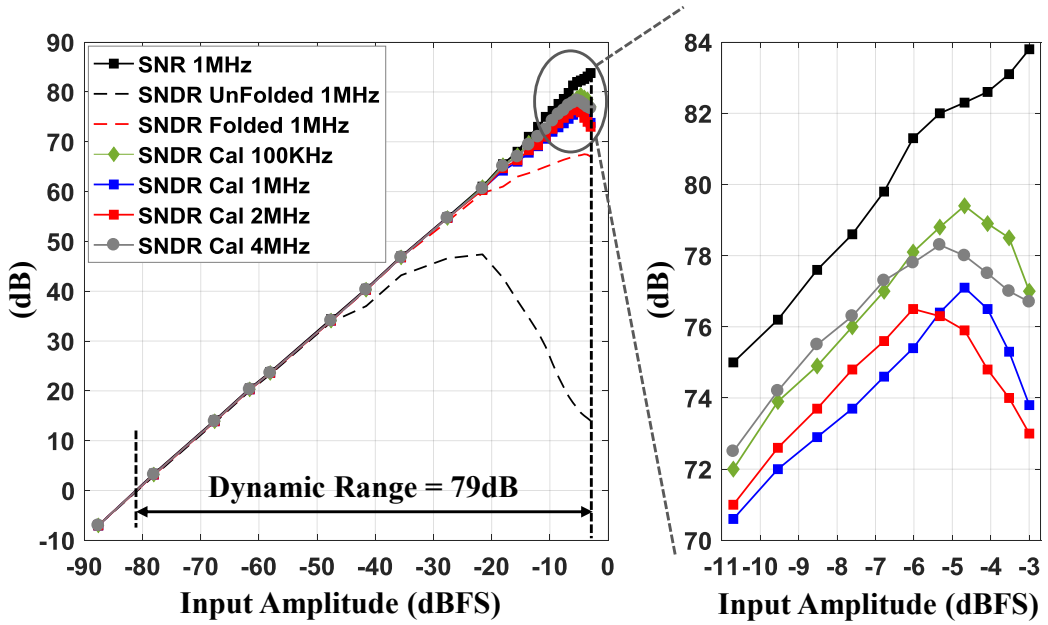


Fig. 4.39. The Measured input amplitude plot of the 675 MS/s ADC for unfolded/ folded/calibrated ADC at different input frequencies in10 MHz bandwidth.

The measured FFT of the 675 MS/sec ADC with the unfolded VCO, folded VCO and calibrated ADC are provided in Fig. 4.38 showing SNR/SNDR/SFDR of 82.9 dB/77.6 dB/85 dB in 10 MHz bandwidth for the calibrated ADC. The folding results in 51.8 dB improved SNDR over the unfolded VCO, while the calibration adds another 12.1 dB SNDR improvement. Fig. 4.39 provides the input amplitude plot of the 675 MS/sec ADC for the unfolded VCO, folded VCO, and calibrated ADC at different input frequencies in 10 MHz bandwidth showing 79 dB dynamic range. The performance of the proposed ADC is compared to previously reported time-based ADCs [167]. Fig. 4.40 introduces a FoM versus input bandwidth plot for this work together with state-of-the-art published work with resolution higher than 10-bits and Table 4.3 shows the detailed performance comparison with time-based ADCs in [114], [119], [121], [168], [169], [170] The FoM of the ADC is computed as

$$FoM = \frac{Power}{2 \times BW \times 2^{ENOB}} \tag{4.10}$$

where BW is the bandwidth and ENOB is the effective number of bits of the ADC. From the provided comparison it can be concluded that the proposed ADC achieves superior performance beyond 10 MHz compared to state-of-the-art oversampling time-based ADCS with best FoM of 76 fJ/conv.step at 10 MHz bandwidth. This is attributed to the low quantization noise level provided by the high-resolution SAR-TDC and the improved linearity of the folded-VCO.

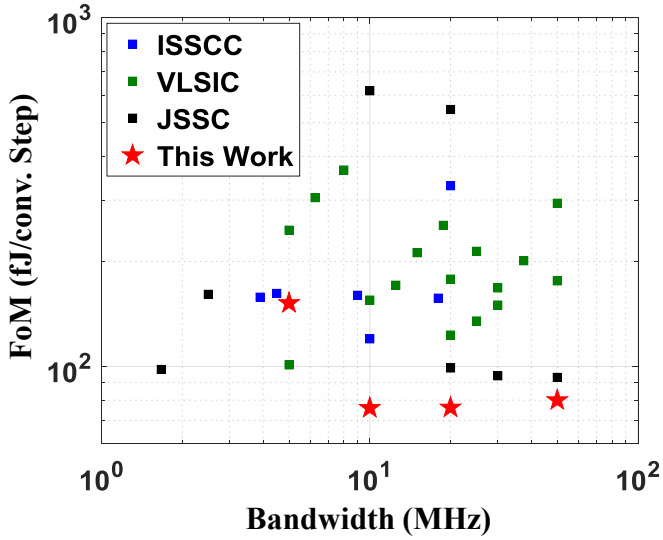


Fig. 4.40. FoM versus bandwidth comparison plot for published oversampled time-based ADCs with resolution higher than 10-bits from 2008 till now

Table 4.3
Comparison With State-of-the-art Oversampling Time-Based ADC

	Process (nm)	Supply (V)	Power (mW)	F_S (MS/s)	BW (MHz)	F_{in} (MHz)	SNR (dB)	SNDR (dB)	ENOB (bits)	FoM (pJ/conv)	Area (mm^2)
[121]	90	1	4.1	640	5	1	75.4	73	11.8	0.112	0.16
[119]	65	1	12.2	300	30	10	N/A	64	10.3	0.15	0.02
[114]	65	1.2	8	500	3.9	1	71.5	71	11.5	0.35	0.07
[168]	65	1.2	16	600	10	1	80.5	76.6	12.4	0.148	0.36
[169]	40	0.9	2.57	1600	40	10	60.7	59.5	9.59	0.042	0.017
[170]	65	1	8.2	1000	50	5	N/A	60.6	9.77	0.093	0.62
This Work	65	1/1.2V	11.65	675	50	10	65.7	65	10.5	0.08	0.047
					20	5	74.8	73.4	11.9	0.0762	
					10	0.1	82.9	79.5	12.9	0.076	
						1	82.9	77.6	12.6	0.0938	
						2	82.9	77.1	12.5	0.1	
						4	82.9	78.3	12.7	0.088	
					5	1	84	79.4	12.9	0.152	

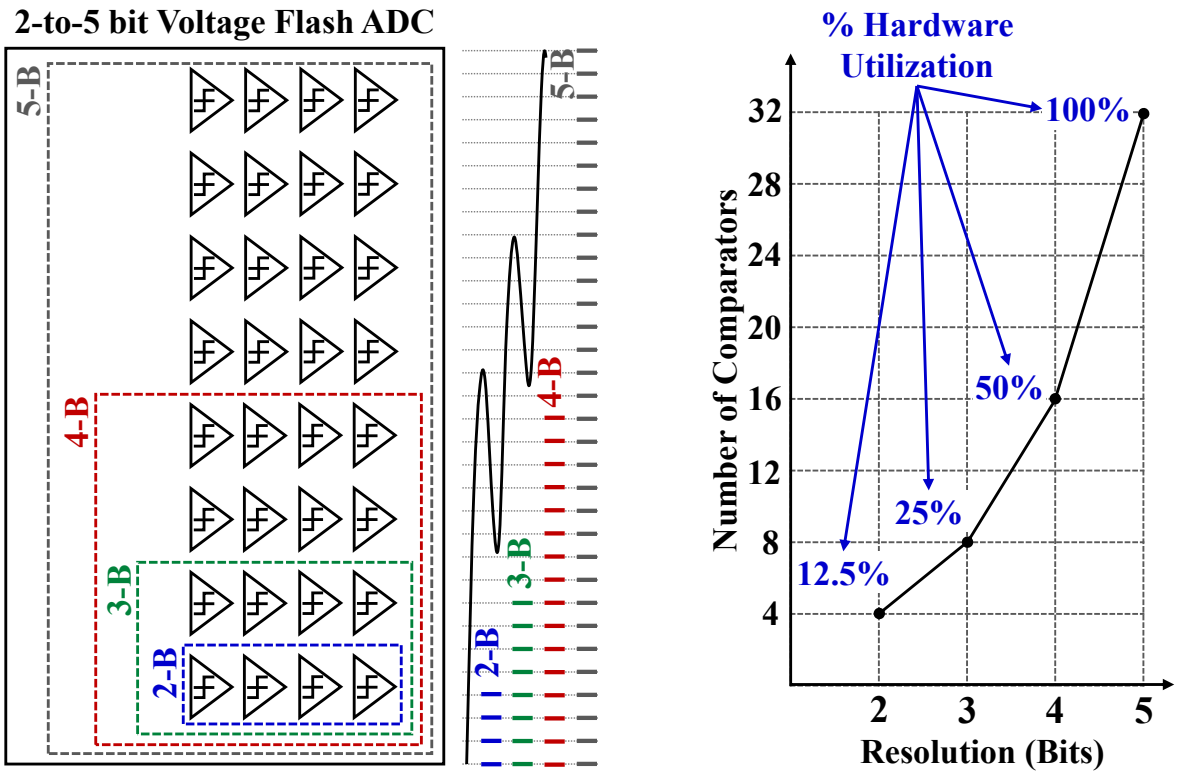
4.4 The Nyquist-rate Reconfigurable Time-based ADC

Reconfigurable analog-to-digital converters (ADCs) have recently gained much attention from the research community owing to the rapid evolution in multi-standard wireless transceivers [171],[172], biomedical sensors [173],[174] and wireless sensor networks [175]. Current battery-operated multi-standard wireless handset transceivers are required to support the bandwidth requirements for the fourth generation mobile technology (4G) while providing back

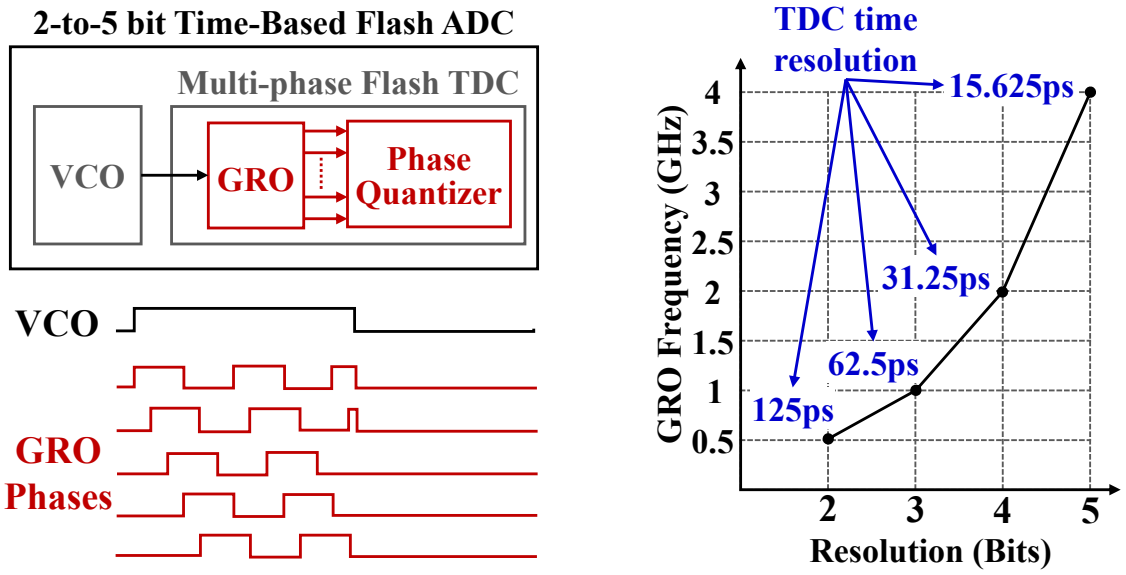
compatibility with the 2G and 3G mobile standards in addition to GPS, WiFi, Bluetooth, WiMax, …etc standards [176]. The design of the reconfigurable ADC for such transceivers is challenging as it is required to support a wide range of data rates, resolutions, and bandwidths with low power/area consumption. Reconfigurable ADCs for the future 5G handset transceivers will be even more challenging as 5G is required to support higher bandwidths and data rates. Reconfigurable ADCs can be designed with different levels of reconfigurability. They can be reconfigurable over both resolution and bandwidth [177], over bandwidth only [178] or over resolution only [179],[180].

The performance of voltage-domain reconfigurable ADCs is limited owing to the non-recoverable area/power penalty when switching between different modes. As shown in Fig. 4.41(a), a 2-to-5 bit flash ADC requires 32 comparators where for the 5-bit mode all comparators are used, while for the 2-bit mode 87.5% of the hardware is wasted as only 4 comparators are needed. Extending the reconfigurability range of voltage-based ADCs results in higher power/area penalty. The time-domain flavor of the ADC can overcome this limitation. Time-based ADCs has two main components, a voltage-controlled oscillator (VCO) and a time-to-digital converter (TDC). The TDC employs a gated-ring oscillator (GRO) followed by a phase quantizer (PQ). In this case, higher resolution can be achieved by increasing the number of GRO phases resulting in finer granularity in time scale. Alternatively, if the GRO is running at a faster rate relative to the VCO, higher resolution can be achieved keeping the same number of phases. Therefore, time-domain architectures have the potential to provide a wide range of reconfigurability by varying the TDC time resolution with excellent hardware utilization as shown in Fig. 4.41(b).

Several Nyquist-rate voltage-based reconfigurable ADCs were reported in the literature. In [181] a 128× time-interleaved (TI) single-slope ADC was proposed. Due to a large number of TI channels, the ADC has large input capacitance and needs 128 phase-shifted ramp signals adding complexity to the design. In [182] reconfigurability was attained by switching between flash and multi-step architectures. It requires complicated clocking and the use of four flash ADCs operating at high frequency resulted in high power consumption. In [183] a two-channel TI pipeline ADC was proposed which consumes a large amount of power. Voltage-domain SAR ADCs can provide flexible operation over sampling rate and resolution [184]–[187]. However, their maximum speed, area, and performance are limited at the high-resolution modes.



(a)



(b)

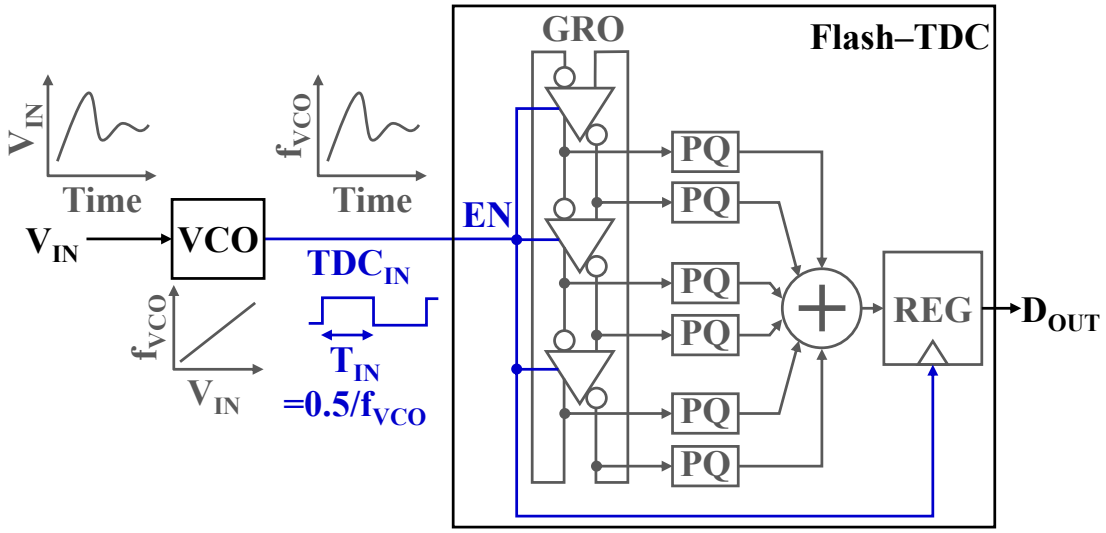
Fig. 4.41. Voltage-based versus Time-based Reconfigurable Flash ADC. (a) Voltage-based Flash ADC using 32 comparators. (b) Time-based Flash ADC comprising VCO and TDC assuming a VCO with 1 GHz center frequency and 16-phase GRO.

To conclude, the limitations of the voltage-based architectures are mainly due to the analog nature of their implementation using a large number of comparators and OTAs which also makes it difficult to scale with technology. Time domain ADCs serve as a digital alternative that can scale graciously with technology while providing continuous sampling rate variation over a wider range. They can also provide higher flexibility and efficient hardware reuse. In addition to that, time interleaving is also significantly simpler in time domain ADCs where instead of a multi-phase time interleaver, a simple divider is needed. The divided sub-rate outputs are then digitized by the TDC. This section proposes a power-efficient time-based ADC employing a SAR/Flash reconfigurable TDC. The TDC enables programmable resolution and sampling rates. In the high sampling rate flash mode, the TDC resolution is solely set by the GRO. For higher resolution, the TDC is switched to the SAR mode. At higher TDC resolution, quantization noise is no longer the SNDR limiting factor – instead, the ADC performance is limited by the non-linearity of the VCO. To address non-linearity, this work introduces a programmable 1-bit folded-VCO that is capable of providing a wide range of tuning characteristics with high linearity for the different sampling rate modes supported by the ADC. The ADC linearity is further enhanced using foreground digital calibration [117].

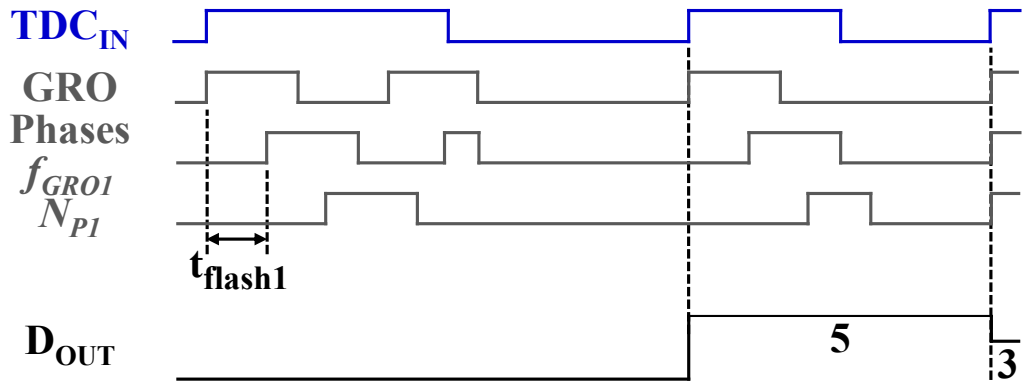
4.4.1 The SAR/Flash Reconfigurable TDC

The reconfigurable TDC is the key element enabling the time-based reconfigurable ADC to cover a wide range of sampling rates/resolutions while consuming a reasonable amount of power. Hence, it is critical to choose the proper TDC topology that can provide a wide range of reconfigurability. By combining the SAR and Flash architectures in the TDC, an efficient reconfigurable TDC can be implemented.

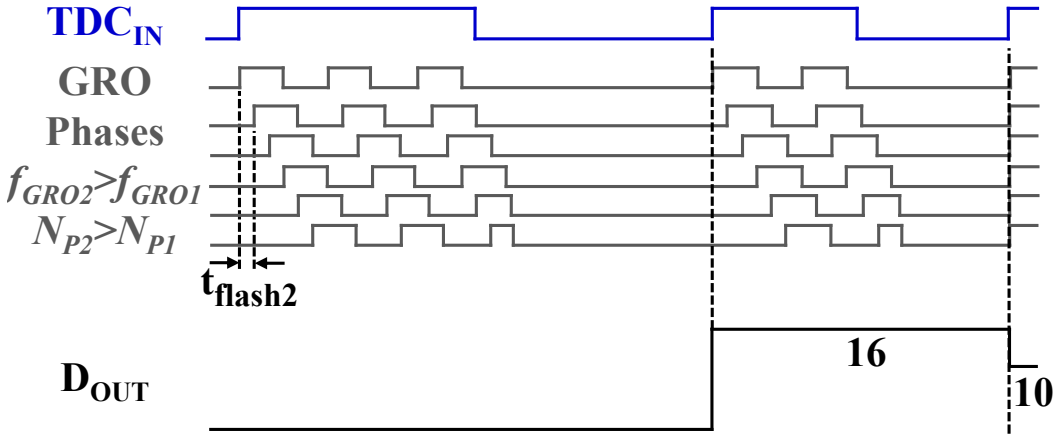
Among the different TDC topologies, Flash TDC [188] is the simplest and is capable of operating at high sampling rates. Fig. 4.42(a) shows the block diagram of a conventional multi-phase Flash TDC (MP-TDC) whose operation is analogous to Flash ADCs. The TDC converts the input time duration T_{IN} to a digital output where the digital code indicates the number of GRO edges occurring within T_{IN}. A simple way to implement this concept is to use the rising edge of T_{IN} to initiate and the falling edge to stop the oscillation of the GRO and count the number of GRO edges available at the different GRO phases as illustrated in Fig. 4.42(b). The Flash TDC time resolution (t_{flash}) is only dependent on the GRO time resolution (t_{GRO}) dictated by number of phases N_P and frequency f_{GRO} of the GRO



(a)



(b)



(c)

Fig. 4.42. (a) The block diagram of a conventional multi-phase Flash-TDC (MP-TDC). (b) Timing diagram of conventional Flash-TDC. (c) Enhancing Flash-TDC resolution by increasing the GRO frequency and number of phases.

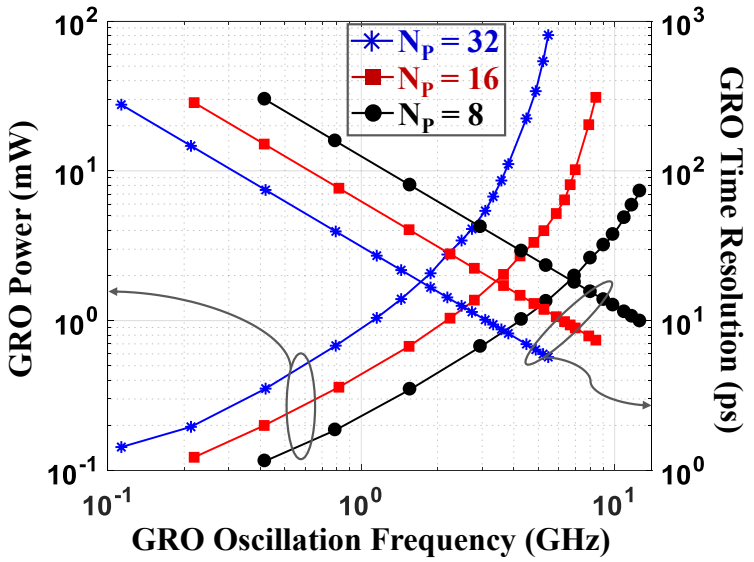


Fig. 4.43. Simulated GRO power/time resolution versus oscillation frequency for different number of GRO phases in 65 nm CMOS process.

$$t_{flash} = t_{GRO} = \frac{1}{N_P \times f_{GRO}} \tag{4.11}$$

Obviously, achieving higher resolution, in this case, will require higher GRO frequency and/or higher number of GRO phases as illustrated in Fig. 4.42(c). However, as N_P and f_{GRO} increase, the GRO power increases drastically. This can be concluded from Fig. 4.43 showing the simulated GRO power/resolution versus frequency for different values of N_P in the 65 nm CMOS technology node where the GRO consumes more than 80 mW to achieve only 5.7 ps time resolution. This is also attributed to the fact that, for N-bits resolution, 2^N PQs are required.

A typical implementation of time-based flash ADC is shown in Fig. 4.42 where the analog input directly modulates the VCO's frequency, f_{VCO}. The Flash TDC quantizes half the VCO period T_{VCO} (i.e., T_{IN} = ½ T_{VCO}) where the TDC is enabled during the positive half cycle of the VCO and then the TDC output is sampled by the edge TDC_{IN}. Hence, the ADC sampling rate is set by the periodicity of the TDC_{IN}, or in other words, the VCO frequency. Although the VCO frequency changes with the input signal, the GRO frequency remains fixed and that sets the sampling rate ($f_{S,Flash}$) relative to the center frequency of the VCO ($f_{VCO,0}$)

$$f_{s,Flash} = f_{VCO,0} = \frac{f_{GRO}}{M} \tag{4.12}$$

where M represents the number of GRO cycles within the VCO period (for N_P-phase GROs, the f_{GRO} is multiplied by N_P). The digital output code in flash mode ($D_{OP,Flash}$) can be written as

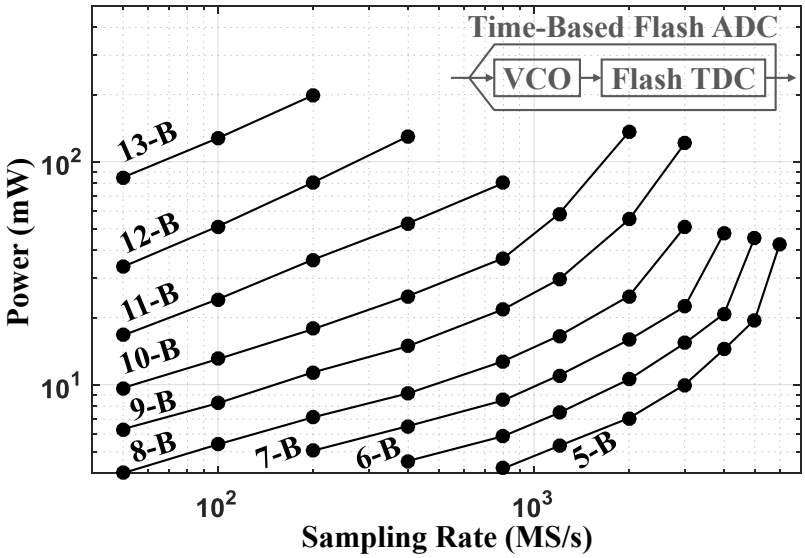


Fig. 4.44. Simulated Time-Based Flash ADC power versus sampling rate for different ADC resolutions.

$$D_{OP,Flash} = \frac{½T_{VCO}}{t_{flash}} = \frac{N_P \times f_{GRO}}{2 \times f_{s,Flash}} \tag{4.13}$$

Therefore, the time-based flash ADC sampling rate is set by the VCO's center frequency and its resolution is set by the GRO number of phases (N_P) and frequency (f_{GRO}). Fig. 4.44 presents the simulated time-based Flash ADC power versus sampling rate for different resolutions where power increases exponentially with resolution similar to its voltage domain counterpart. This is due to the fact that achieving higher resolution requires higher GRO frequency and number of phases which is accompanied by an increase in power consumption as predicted by Fig. 4.43.

To overcome the resolution limitation of the Flash architecture, other TDC topologies such as two-step TDCs and pipelined TDCs were proposed adopting techniques to enhance the TDC resolution without increasing the number of GRO phases and frequency. However, the non-linearity of the time amplifiers used in such structures requires careful design consideration. On the other hand, SAR TDC topologies offer an attractive alternative that does not require time amplification. As discussed in the previous section, the SAR-TDC employs two MP-TDCs, a digital comparator, SAR logic and DTC. The MP-TDC provides the coarse resolution (t_{flash}) while the SAR operation provides the fine resolution (t_{SAR}),

$$t_{SAR} = {t_{flash}}/{2^{N_S} - 1} \tag{4.14}$$

where N_S is the number of SAR bits. Note that compared to the flash operation, in SAR the

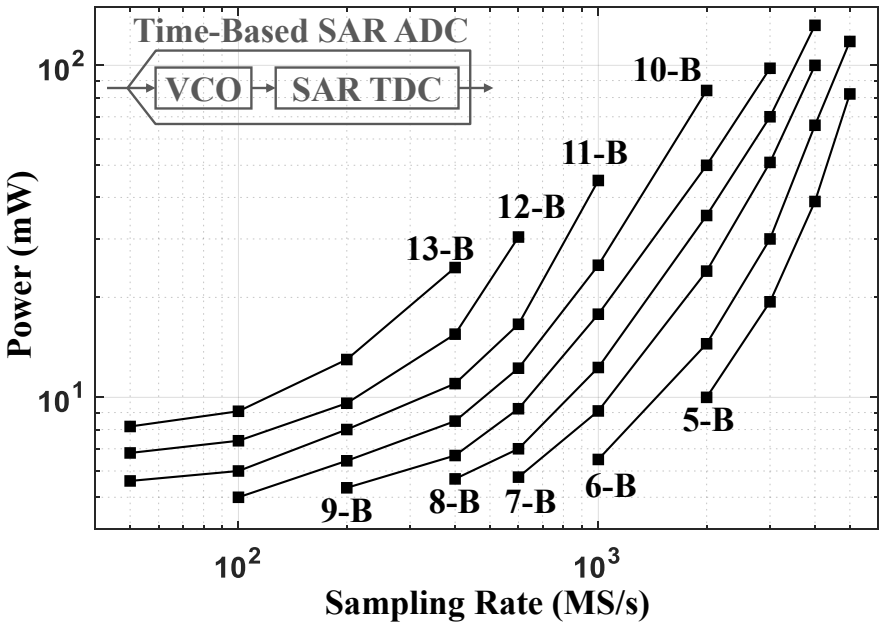


Fig. 4.45. Simulated Time-Based SAR ADC power versus sampling rate for different ADC resolutions.

resolution is improved by $2^{Ns} - 1$ without increasing the GRO frequency and the number of phases. A time-based SAR ADC can be designed using a VCO followed by a SAR-TDC. For N_S-bit SAR operation, the final digital output will be available after N_S VCO-cycles. Therefore, the sampling rate of the ADC in the SAR mode ($f_{s.SAR}$) is also scaled by the factor N_S

$$f_{s,SAR} = {f_{VCO,0}}/{N_S} \tag{4.15}$$

Similar to the Flash mode, the digital output code of the ADC in the SAR-mode ($D_{OP,SAR}$) can be written as

$$D_{OP,SAR} = \frac{½T_{VCO}}{t_{SAR}} = \frac{N_P \times f_{GRO} \times (2^{N_S} - 1)}{2 \times f_{s,SAR} \times N_S} \tag{4.16}$$

Obviously, the SAR mode is more suitable for higher resolution. However, to achieve the same sampling rate as flash, VCO frequency must be increased by *Ns* or requires *Ns* time-interleaved paths. Both factors make SAR ADCs expensive at higher sampling rates. The simulated time-based SAR ADC power versus sampling rate for different resolutions is illustrated in Fig. 4.45 showing that it can provide higher resolution with low power consumption at moderate sampling rates. However, at higher sampling rates, the SAR ADC power goes up drastically even for

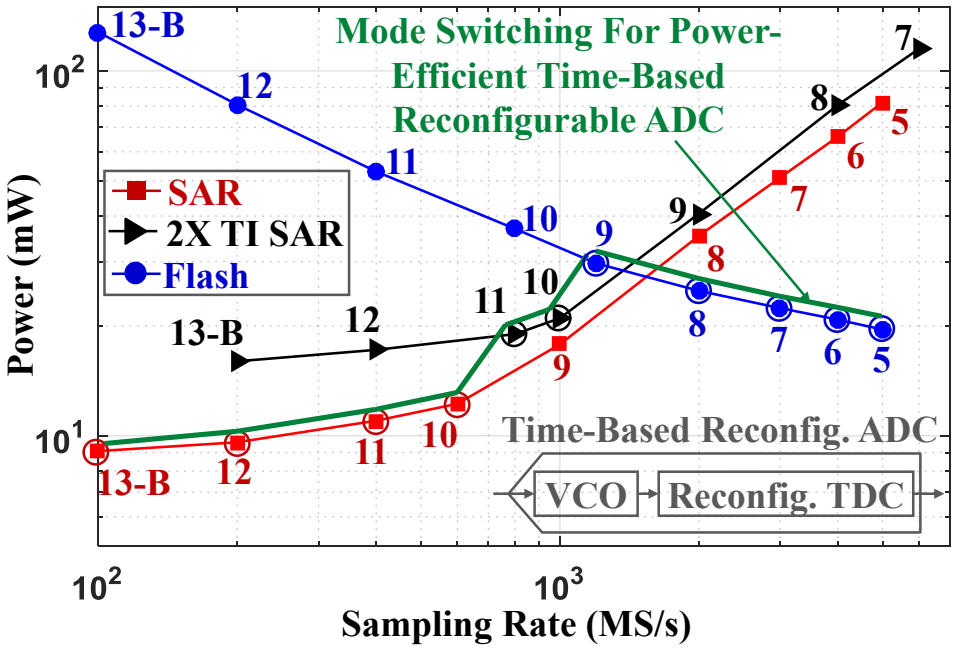


Fig. 4.46. Simulated power versus sampling rate for the reconfigurable time-based ADC.

moderate resolution. At those rates flash ADCs are more energy efficient for the same resolution.

From the foregoing discussion, we conclude that obtaining a wide range of reconfigurability over sampling rate and resolution with low power, using only one TDC flavor (either Flash or SAR) can be sub-optimal. The required number of phase comparators in Flash TDC increases exponentially with resolution, hence power consumption follows the same trend. In contrast, the number of comparisons increases linearly in SAR but requires much faster VCO frequency for high sampling rates which results in high power consumption. Hence for a wide range of reconfigurability, Flash and SAR need to be combined together. Although this observation is same as voltage domain flash and SAR, time domain provides a unique advantage. In voltage domain, reconfiguring between flash and SAR is difficult due to limited hardware reuse. However, in time domain it is simpler to reconfigure the ADC between flash and SAR by simply adjusting VCO and GRO frequencies. Therefore, to provide a wide range of reconfigurability, it is required to design a reconfigurable TDC that can easily switch between SAR and Flash modes with efficient hardware re-use. Fig. 4.46 overlays the time-based Flash ADC (shown in blue) and time-based SAR ADC (shown in red) plots from Fig. 4.44 and Fig. 4.45 together where for each sampling rate one design point is chosen that provides the best compromise between resolution and power. Also, a 2× TI time-based SAR-ADC plot (shown in

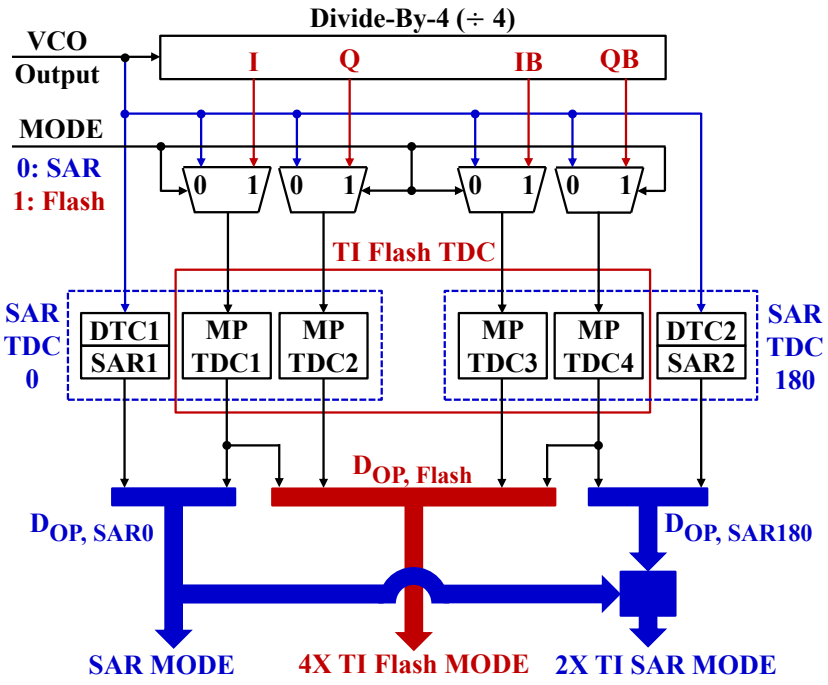


Fig. 4.47. The block diagram of the proposed SAR/Flash reconfigurable TDC with efficient hardware reuse.

black) is added that employs two SAR-TDCs. In order to cover a wide range of sampling rates with low power, mode switching is performed (as shown in green), where SAR is used for low sampling rates, Flash for high sampling rates and 2× TI SAR for moderate sampling rates. To show how the switching between different modes is selected, the choice of the best architecture for the 9-bits mode will be considered as an example. At 1 GHz sampling rate, the power consumption of the 10-bit 2× TI SAR and that of the 9- bit SAR are quite close, hence the 10-bit 2× TI SAR was chosen for this sampling rate since it will be more efficient. At 2 GHz sampling rate, the 9-bit 2× TI SAR consumes a large amount of power compared to the 8-bit Flash mode, hence the 8-bit Flash mode was chosen for this sampling rate. The best choice for the 9-bit which provides reasonable power is at 1.2 GHz sampling rate where switching is performed from the 2× TI SAR to the Flash mode.

The block diagram of the proposed SAR/Flash reconfigurable TDC is shown in Fig. 4.47. It employs four MP-TDCs, two SAR logic blocks, two DTCs and a divide-by-4 circuit. The divide-by-4 circuit is implemented by cascading two master-slave clocked-CMOS (C^2MOS) divide-by-2 stages. For the Flash mode, the four MP-TDCs are employed where they take the I/Q divider outputs and operate as 4× TI asynchronous Flash TDC. In the 2× TI SAR mode, two

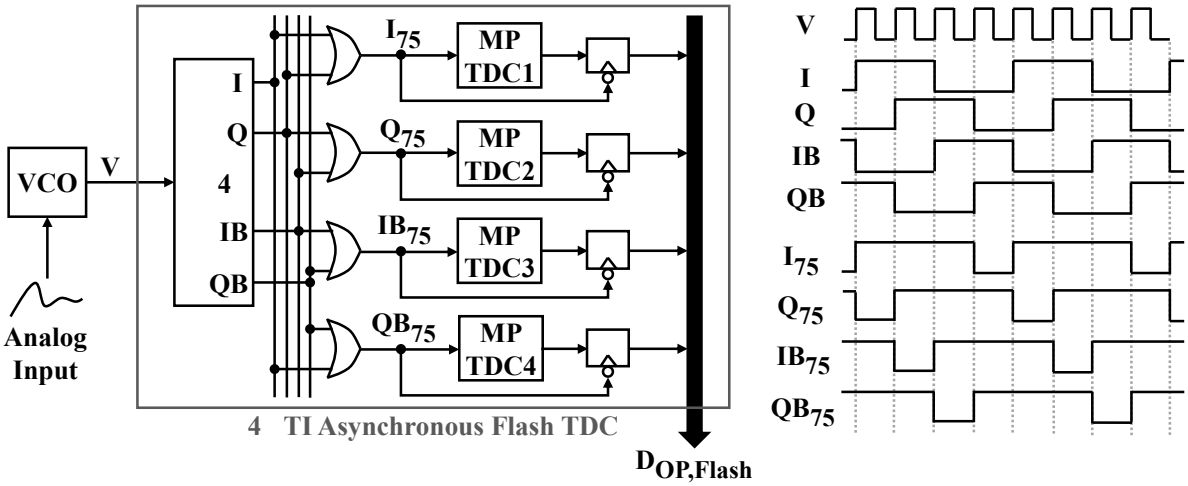


Fig. 4.48. The block diagram of the asynchronous 4× TI Flash mode with extended duty cycle input to the MP-TDCs.

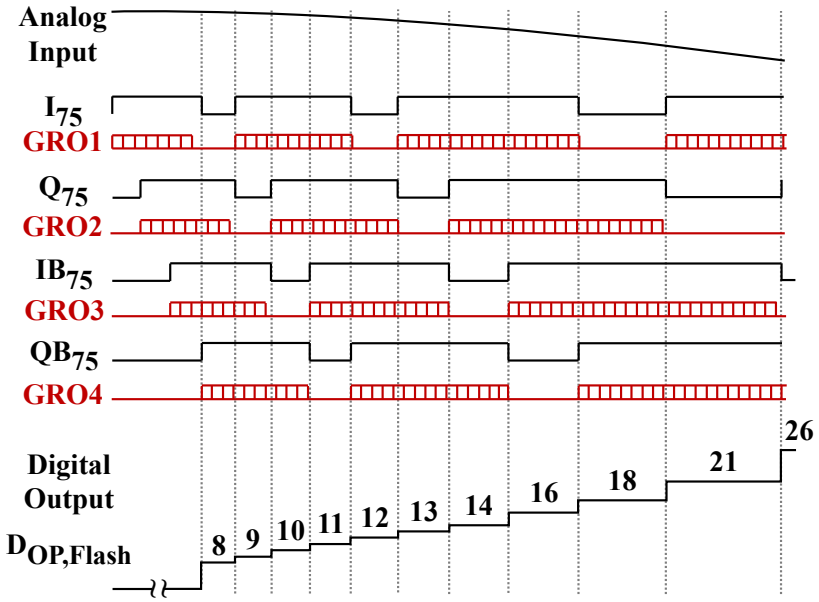


Fig. 4.49. The Timing diagram describing the operation of the asynchronous 4× TI Flash mode.

SAR-TDCs are employed utilizing the four MP-TDCs, the two SAR blocks, and the two DTC blocks. In the SAR mode, only two MP-TDCs, one SAR block, and one DTC are used.

4.4.2 The 4× Time-interleaved Asynchronous Flash Mode

The flash mode serves at high sampling rates. Increasing resolution at high sampling rates is challenging as resolution in time-domain is inversely related to the sampling rate. Using a single MP-TDC is not an appropriate choice as it requires the GRO to run at a very high frequency

resulting in high power consumption. Instead, time interleaving is applied [189]. Time interleaving is performed in the time domain. The VCO output is introduced to a divide-by-4 circuit to increase the time period introduced to the TDC and hence achieving higher resolution. To keep the same sampling rate after division, the I/Q outputs of the divider are introduced to four MP-TDCs for 4× time interleaving as shown in Fig. 4.48. To further enhance the resolution, the 50% duty cycle I/Q divider outputs are introduced to a bank of OR gates providing 75% duty cycle I_{75}/Q_{75} signals that are input to the MP-TDCs. This has the effect of extending the input period introduced to the MP-TDCs and hence enhancing the resolution without sacrificing the sampling rate. No sample-and-hold (S/H) is needed for this mode since the VCO output frequency is proportional to the average input signal due to the averaging nature of the VCO. The absence of the S/H results in an inherent sinc filtering function as predicted in [117] which helps filter the spurs in the ADC output spectrum. The timing diagram describing the operation of the 4× asynchronous TI flash mode is illustrated in Fig. 4.49 where the MP-TDC is enabled when its input is high. The MP-TDC time resolution is dictated by that of the GRO. The resolution of the ADC in the 4× TI flash mode (R_{Flash}) can be written as

$$R_{Flash} = \frac{¾ \times 4 \times T_{VCO,max}}{t_{flash}} - \frac{¾ \times 4 \times T_{VCO,min}}{t_{flash}} = 3 \times N_P \times f_{GRO} \times \left(\frac{1}{f_{VCO,min}} - \frac{1}{f_{VCO,max}} \right) \quad (4.17)$$

where the MP-TDC quantizes the 75% duty cycle (resulting in the ¾ factor) divide-by-4 version (and hence the factor 4) of the VCO period.

Note that, the ADC is not significantly affected by the time interleaving skew effect in flash ADC modes where resolution is relatively low. Skew effect in this 4-way time-interleaved ADC originates from duty cycle distortion at the VCO output that we have carefully mitigated in this design. The I/Q clocks for time-interleaving come from a master-slave divide-by-4 circuit that is properly designed at the different corners and implemented with symmetric layout. Finally, the absence of the S/H played an important role as it allowed for inherent sinc filtering that helped filter the spurs arising from time skew.

4.4.3 The High-Resolution SAR mode

For high resolution, the TDC is configured in the SAR mode as illustrated in Fig. 4.50. The synchronous SAR-mode employs a sample-and-hold (S/H) ahead of the VCO. Using 2 channels

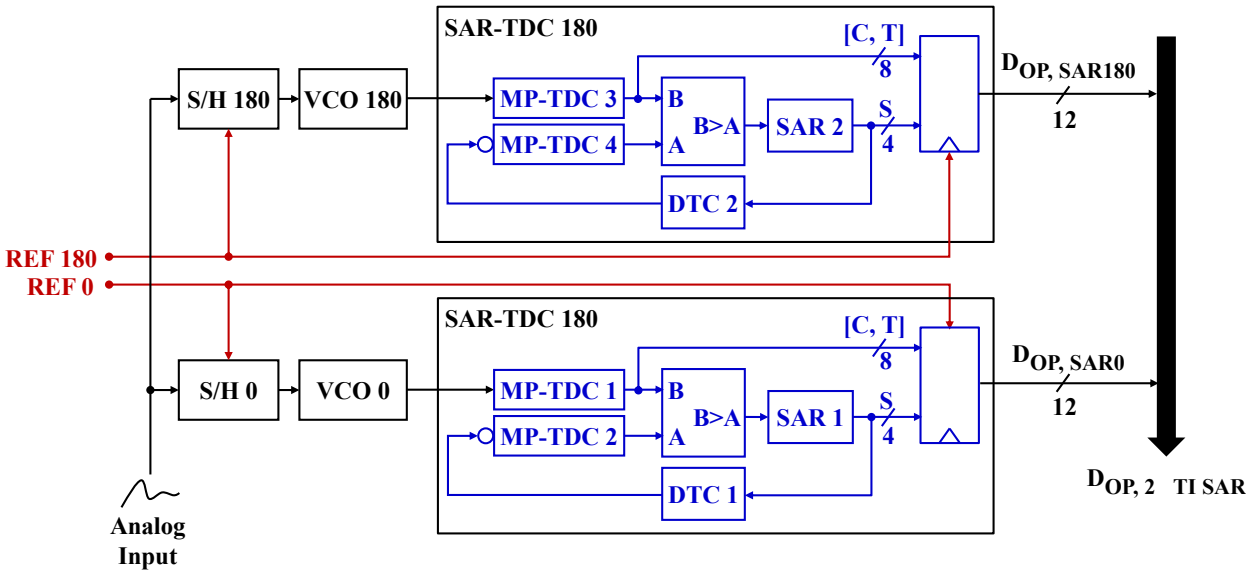


Fig. 4.50. The block diagram of the high resolution SAR mode.

(0 and 180) and clocking the S/H circuits with out-of-phase reference clocks configure the ADC in a 2× TI SAR mode. The SAR mode employs the SAR-TDC presented in the previous section. The designed SAR-TDC achieves fine resolution of 1 ps. The ADC resolution in the SAR mode *(R_{SAR})* can be given as

$$R_{SAR} = \frac{½ \times T_{VCO,max}}{t_{SAR}} - \frac{½ \times T_{VCO,min}}{t_{SAR}} = \frac{N_P \times f_{GRO} \times (N_{BL} - 1)}{2} \times \left(\frac{1}{f_{VCO,min}} - \frac{1}{f_{VCO,max}} \right) \quad (4.18)$$

For all-digital small-area implementation, a ring-VCO is utilized which has higher phase noise than LC VCOs. Fig. 4.51 provides the measured VCO phase noise at 1.2 GHz showing integrated RMS jitter of 7.5 ps which results in degrading the ADC quantization noise level. Hence correlated double sampling is applied to the SAR-TDC. To quantify the effect of VCO jitter on the SNR and how much improvement can time-domain CDS provide, Fig. 4.52 shows the simulated SNR versus VCO jitter normalized with respect to the TDC resolution *(t_{SAR})* for the time-domain SAR ADC with/without CDS applied. CDS is disabled by allowing the MP-TDC1 to operate during the first SAR cycle only and disabling it during the rest of the SAR operation. From the obtained results it can be concluded that for very low VCO jitter (which is not practical) the ADC with and without CDS provides approximately the same SNR. As VCO jitter increases, the SNR starts to degrade significantly for the ADC without CDS. However,

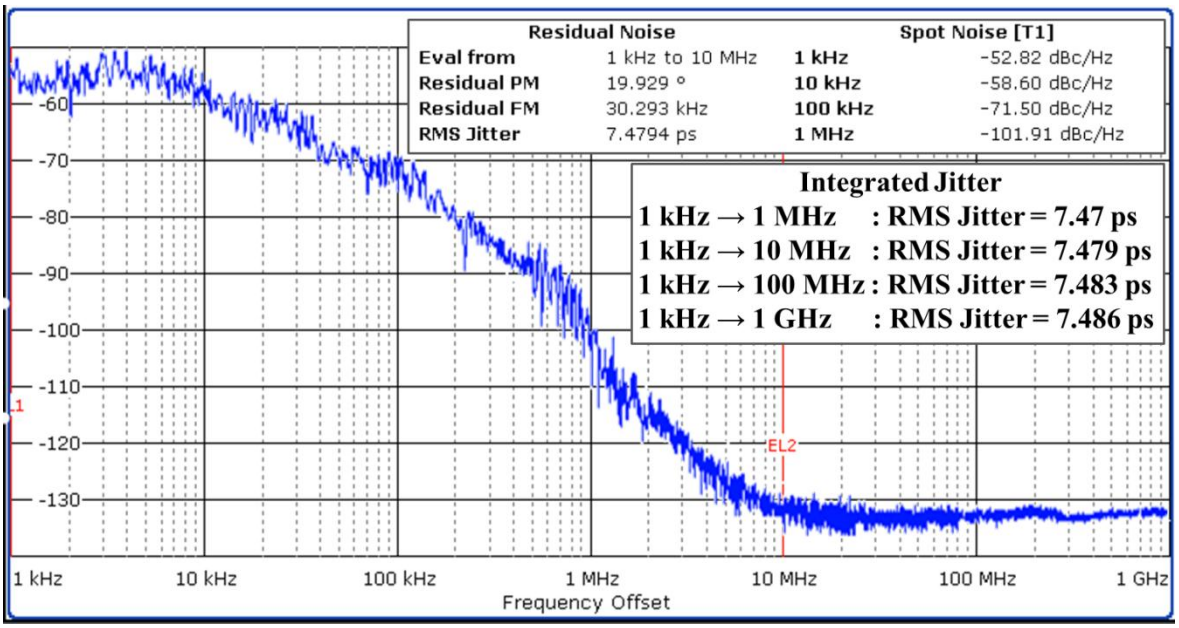


Fig. 4.51. Measured ring VCO phase noise at 1.2 GHz.

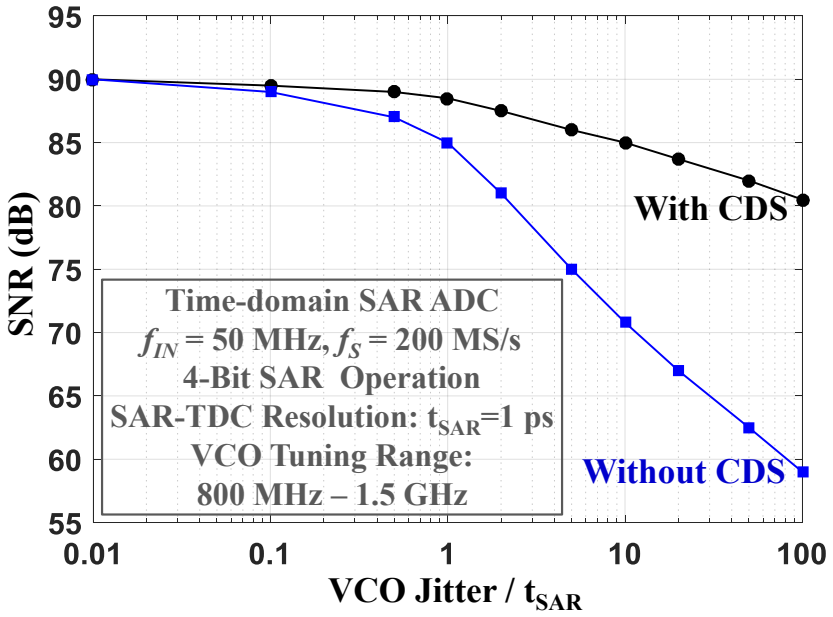


Fig. 4.52. The simulated SNR versus VCO jitter normalized with respect to the TDC resolution for the time-domain SAR ADC with/without CDS.

significant improvement in SNR can be noted when applying CDS. The SNR improvement due to CDS continues to increase with VCO Jitter. Fig. 4.53 shows the simulated output spectrum of the 200 MS/s SAR-mode ADC with/without CDS for 10 ps VCO jitter where it can be concluded that CDS provides 14 dB improvement in SNR compared to the without CDS case. From this

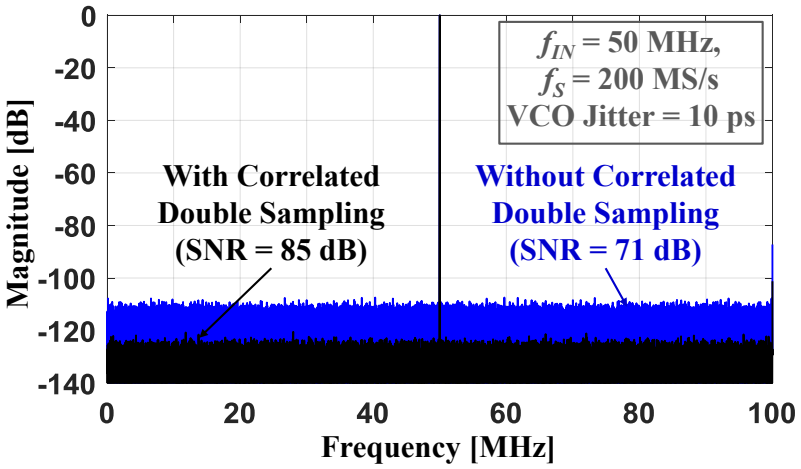


Fig. 4.53. Simulated output spectrum of the 200 MS/s SAR-mode ADC with / without CDS for 10 ps VCO jitter.

Table 4.4
Noise Breakdown

	VCO	MP-TDC1	MP-TDC2	Comparator	SAR	DTC	Total
RMS Noise (μV)	4.442	7.64	7.129	1.79	2.08	4.75	12.9
Equivalent RMS Noise in time-domain (ps)	0.041	0.071	0.0658	0.0166	0.019	0.051	0.119

discussion, we can conclude the following. First, to obtain a time resolution t_{SAR} (which represents the LSB in time-domain) from an N-bit SAR operation, the accumulated jitter over N VCO cycles should be less than ½LSB. This is very difficult to accomplish provided that we are employing a ring VCO which results in degrading the SNR. To overcome this issue, the time-domain CDS is applied where the differential measurement of the input period helps cancel the accumulated jitter and allows getting good SNR even while using a ring VCO. It can be concluded from Fig. 4.52 that with CDS applied, a VCO with RMS jitter of 10× the TDC resolution results in only 5 dB SNR degradation compared to the noise-less VCO case. It also worth to be noted that, the jitter during the N-cycles where the SAR is computed is much less than the RMS jitter we get from the spectrum analyzer that is evaluated over a large number of VCO cycles.

The simulated noise breakdown in the high resolution 100 MS/s SAR mode of the ADC is illustrated in Table 4.4 where the noise sources are referred to the input and the amplitude of the input signal is 0.35 V which is equivalent to 3.23 ns in the time domain.

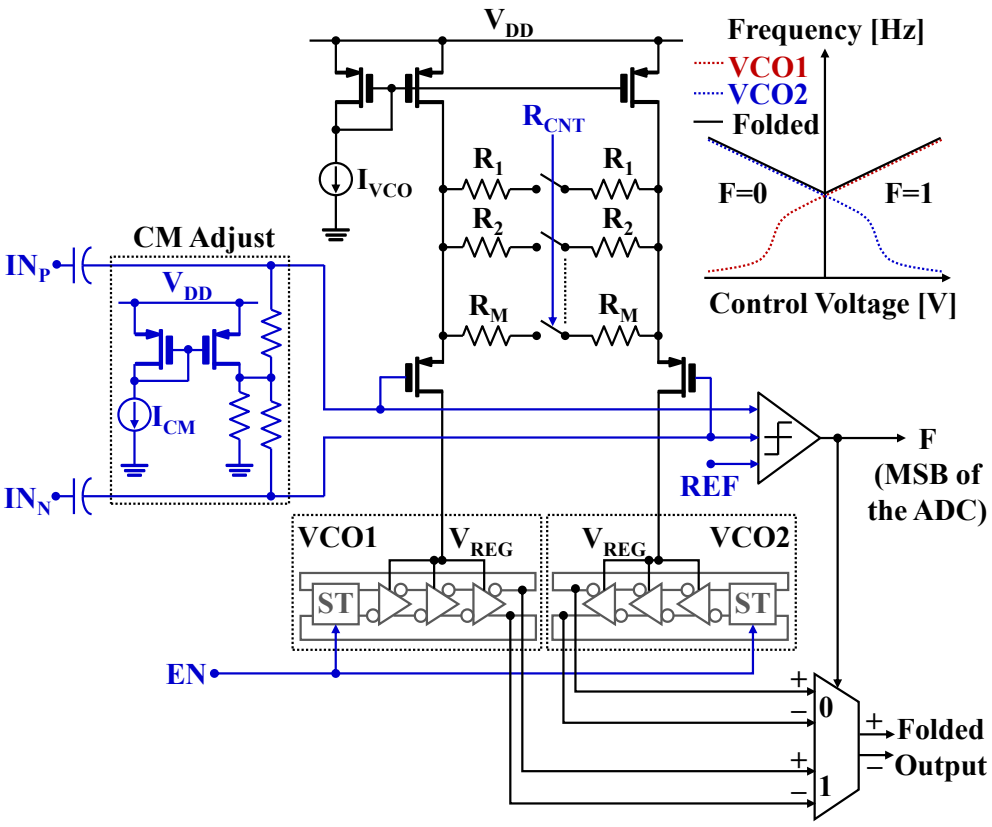


Fig. 4.54. The Programmable 1-bit Folded VCO Schematic.

To summarize and highlight the main design consideration for the SAR mode the following need to be pointed out. First, the jitter from the VCO has great influence on the SNR. Thus, careful design and layout of the VCO together with the proper choice of its delay unit are necessary to enhance its jitter performance. In addition, the CDS is important to help reduce the negative impact of the VCO jitter on the ADC output. Second, to be able to attain high linearity from the DTC without the need for additional calibration, a blender was used for phase interpolation owing to its good performance and high linearity. Also, the fact that the DTC only operates with 4-bits and 16-phases made it design relatively easy. Interpolating more phases within the DTC may result in degrading its linearity in which case calibration would be required.

4.4.4 The Programmable 1-bit Folded VCO

VCO linearization is a key enabler for achieving high ADC resolution. For reconfigurable time-based ADCs, it is even more challenging as the VCO is required to be programmable to provide the tuning characteristics for each sampling rate with high linearity. Hence, a programmable

highly linear 1-bit folded VCO is proposed to serve that purpose. This was achieved by adding programmability to the folded VCO employed in the oversampling ADC. The schematic of the programmable folded VCO is shown in Fig. ⁋4.54. The programmability of the folded VCO is performed by controlling the current going to the V_{REG} nodes by modulating the input current (I_{VCO}) and the input common mode (CM) voltage of the differential amplifier. The input CM is set using a CM Adjust circuit by adjusting the current (I_{CM}). Also, a bank of digitally-controlled source degenerative resistance is used for programming the VCO tuning range where lower source resistance results in higher VCO tuning range. The enable (EN) of the VCO is controlled by the reference clock in the SAR mode. In the flash mode, the VCO is always enabled.

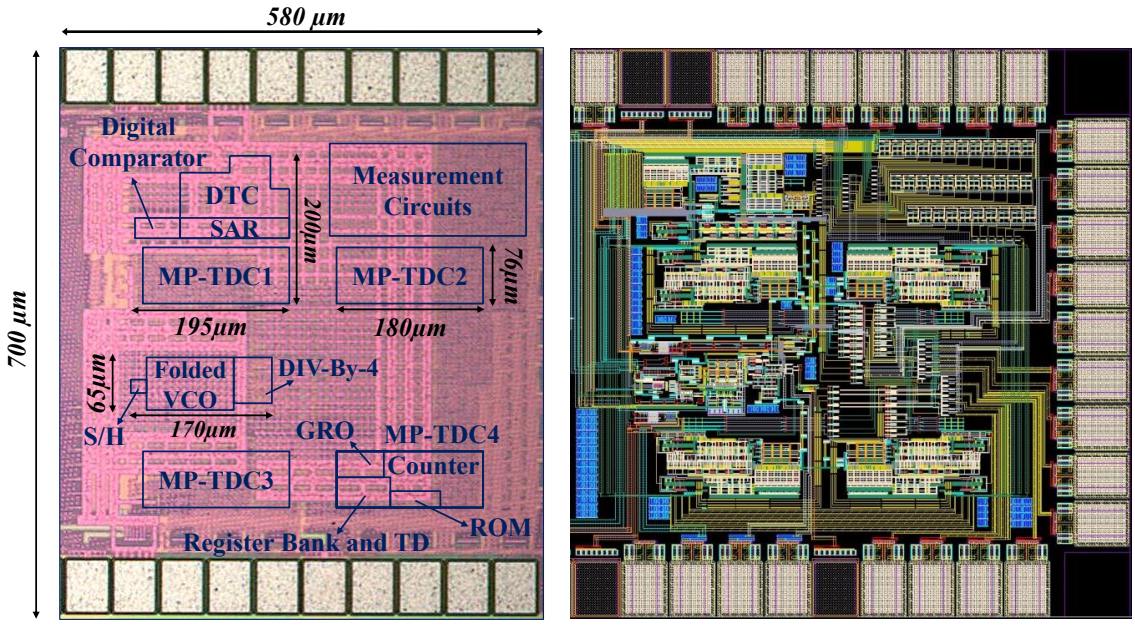
4.4.5 Measurement Results

The die micrograph of the reconfigurable time-based ADC prototype implemented in the TSMC 65 nm CMOS process is illustrated in Fig. 4.55 occupying an active area of 0.091 mm^2. Only one SAR/DTC and one Folded-VCO were implemented. The 2× TI SAR mode was tested by first applying the in-phase and then out-of-phase reference clocks separately and then combining their results together to get the final ADC output. The reconfigurable ADC was tested using the same PCB used for the oversampling ADC. The implemented reconfigurable ADC supports continuous sampling rate variation from 100 MS/s to 5 GS/s while providing resolution ranging from 13-bits to 5-bits.

The programmability of the folded-VCO allowed the generation of different VCO tuning characteristics with high linearity for the different sampling rates supported by the ADC. Fig. ⁋4.56 shows the unfolded and folded-VCO characteristics for the 200 MS/s 12-bits SAR mode where the folding improved the non-linearity of the VCO from 12.8% to 0.102%. Table ⁋4.5 provides the different setups of the VCO including the tuning range of the folded characteristics and its non-linearity.

The Coarse MP-TDC is implemented employing a 14-phase 4.6 GHz GRO providing coarse resolution of 16.2 ps. In the SAR mode, the SAR-TDC was implemented using a 16-phase blender for 4-bit SAR operation. The measured SAR-TDC characteristics and DNL/INL plots are illustrated in Fig. ⁋4.57 showing maximum DNL/INL of 0.67/0.72 LSB and 1.1 ps resolution.

The 13-bits constituting the ADC output are as follows (from MSB to LSB); 1-bit from the Folded VCO, 8-bits from the multiphase TDC and 4-bits from the SAR.



(a) (b)

Fig. 4.55. (a) The die micrograph of the reconfigurable time-based ADC. (b) Chip Layout.

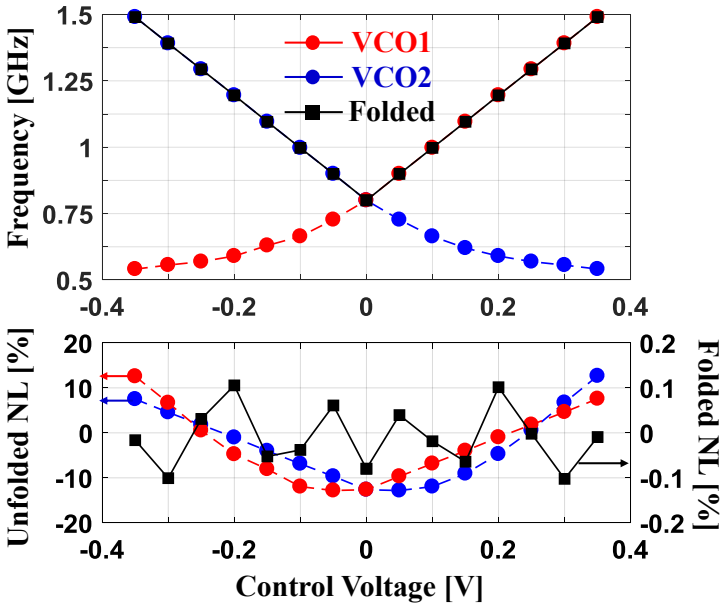
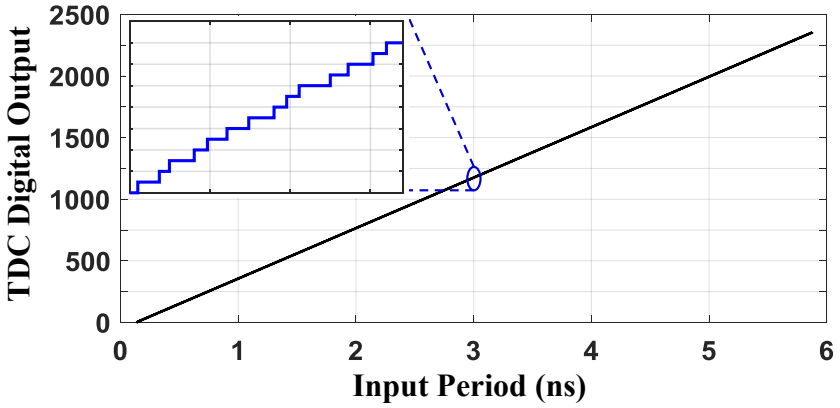


Fig. 4.56. The Unfolded/Folded VCO Tuning Characteristics and non-linearity for the 200 MS/s SAR mode.

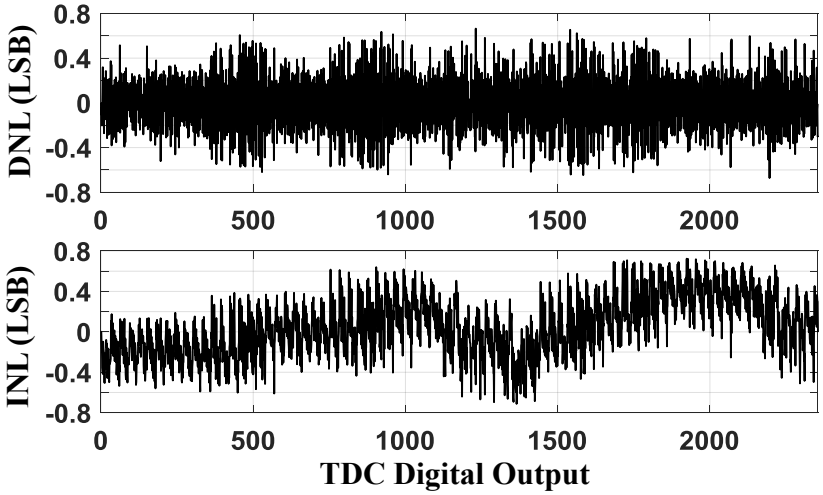
Table 4.5
Folded VCO Characteristics For Different ADC Sampling Rates

Setup	A	B	C	D	E	F	G	H	I	J
$f_{VCO,min}$ (GHz)	0.21	0.4	0.8	1.2	1.61	2	2.4	3.1	4	5
$f_{VCO,max}$ (GHz)	0.39	0.73	1.49	2.1	2.9	3.6	4.3	4.9	5.8	6.9
Unfolded NL (%)	9.8	11.04	12.8	13.2	13.3	13.6	13.8	14.2	15	15.7
Folded NL (%)	0.075	0.083	0.102	0.11	0.12	0.15	0.18	0.23	0.3	0.35
Power (mW) **	1.54	1.68	1.8	2.34	2.52	2.93	3.4	4.4	5.9	6.7

** VCO buffer power is included.



(a)



(b)

Fig. 4.57. (a) The measured SAR-TDC Characteristics. (b) The measured DNL/INL plot of the SAR-TDC.

The ADC consumes a total of 9.01 mW in the 200 MS/s, 12-bit SAR mode with the Folded-VCO operating with Setup-C as follows 1.8 mW folded-VCO, 3.2 mW MP-TDC1, 2.5 mW MP-TDC2, 1.26 mW SAR logic, 10 µW digital comparator and 240 µW DTC. For the 5 GS/s, 5- bits Flash mode with a Setup-J Folded VCO, the ADC consumes 22.3 mW as follows; 6.7 mW folded-VCO, 700 µW divider and OR-bank, and 3.73 mW for each of the four multiphase TDCs.

Fig. 4.58 provides the spectrum of the 200 MS/s SAR-mode ADC output in response to an $0.7V_{PP}$ 10 MHz input sinusoid for the unfolded VCO, folded VCO and calibrated ADC showing SFDR/SNDR of 81/70.8dB after calibration. Fig. 4.59 shows the output spectrum of the reconfigurable ADC in response to an $0.7V_{PP}$ near Nyquist input sinusoid for the 200 MS/s SAR-mode, the 800 MS/s 2× TI SAR-mode and the 5 GS/s 4× TI Flash mode achieving SNDR of 69.8 dB, 62.5 dB, and 28.9 dB, respectively. Also, it can be concluded that the uncalibrated SFDR is

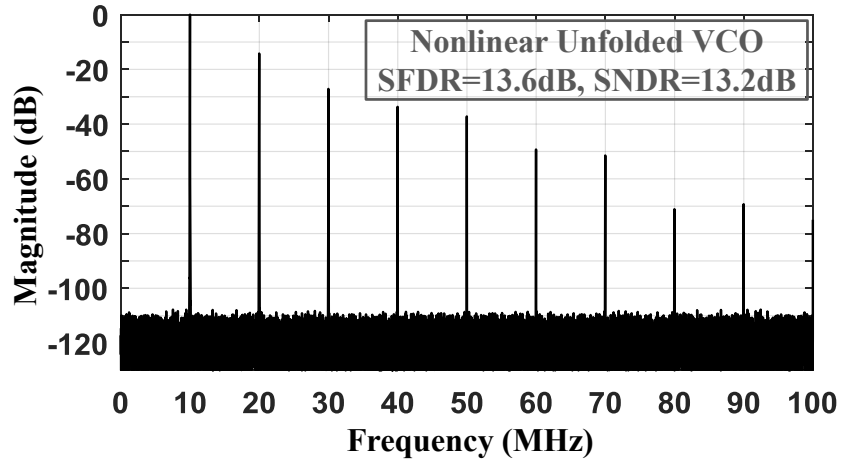
lower for the 5 GS/s mode and higher for lower sampling rate modes. This is attributed to the fact that the ADC non-linearity is dominated by the VCO and each sampling rate mode utilizes different VCO transfer characteristics. For the 5 GS/s mode, the VCO utilizes setup J from Table II where the VCO experiences non-linearity of 0.35% while for the 200 MS/s mode the VCO utilizes the setup C with 0.1% non-linearity. Hence, since the 200 MS/s mode has enhanced VCO linearity compared to the 5 GS/s mode, it features improved SFDR. An important point that should be pointed out is that the generated LUT used for calibration can be used for the different ADC modes. However, similar to other foreground calibration schemes, from time to time the LUT needs to be regenerated to account for supply voltage and temperature variations. A plot of the SNDR versus input frequency for the different ADC modes is provided in Fig. 4.60.

A FoM versus sampling rate plot of the proposed reconfigurable ADC together with previously published SAR, Flash, time-domain and reconfigurable ADCs is introduced in Fig. 4.61 showing that the fabricated prototype achieves good FoM ranging from 14.6 fJ/conv to 196 fJ/conv. Table 4.6 provides a comparison of this work with state-of-the-art reconfigurable ADCs [181], [182], [190]. From which it can be concluded that the proposed time-based reconfigurable ADC provides a wider range of reconfigurability and enhanced FoM.

4.5 Conclusion

In this chapter two time-based ADC prototypes were presented. First, an oversampling time-based ADC is proposed utilizing a correlated double sampling SAR-TDC for improved quantization noise level. A folded VCO is employed for higher sampling rate, higher resolution, and enhanced linearity. The fabricated oversampling ADC prototype achieves superior performance compared to previously reported designs.

Second, a time-based reconfigurable Nyquist-rate ADC was proposed operating over a wide range of sampling rates and resolutions. This was achieved by employing a highly linear programmable folded-VCO and a reconfigurable-TDC that is configured as SAR-TDC for high-resolution modes and as Flash-TDC for high sampling rate modes with power-efficient hardware reuse.



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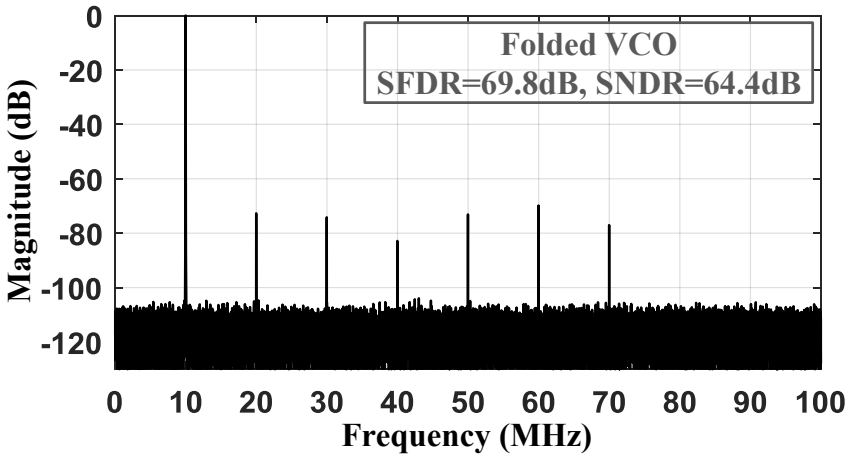

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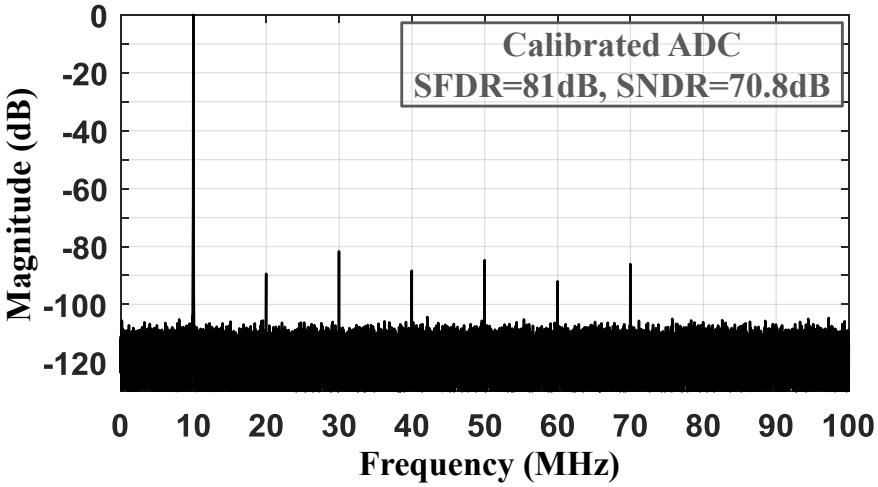
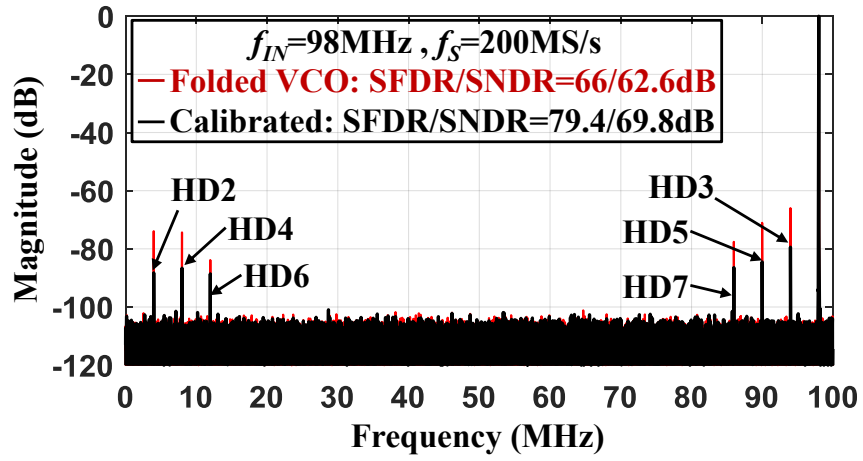
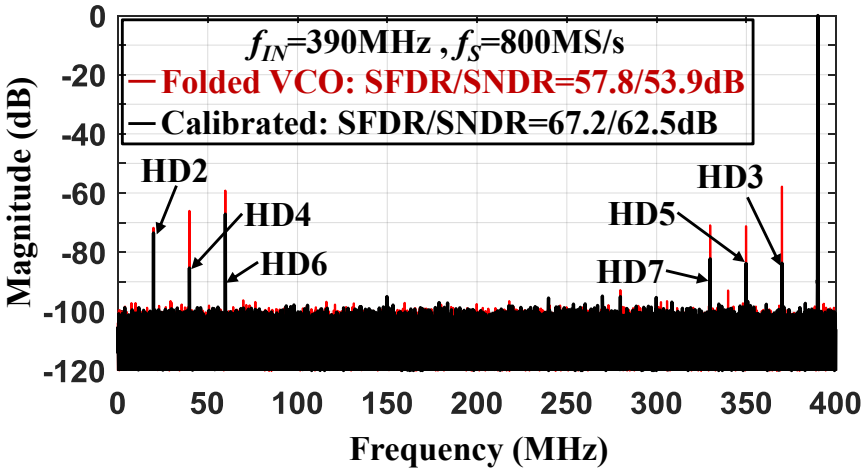


(c)

Fig. 4.58. The measured output spectrum of the 200 MS/s CDS SAR-mode ADC output (2^{16}-point FFT) in response to an 0.7 V_{PP} 10 MHz input sinusoid for (a) Non-Linear VCO (Without Folding). (b) Folded VCO. (c) Calibrated ADC.



(a)



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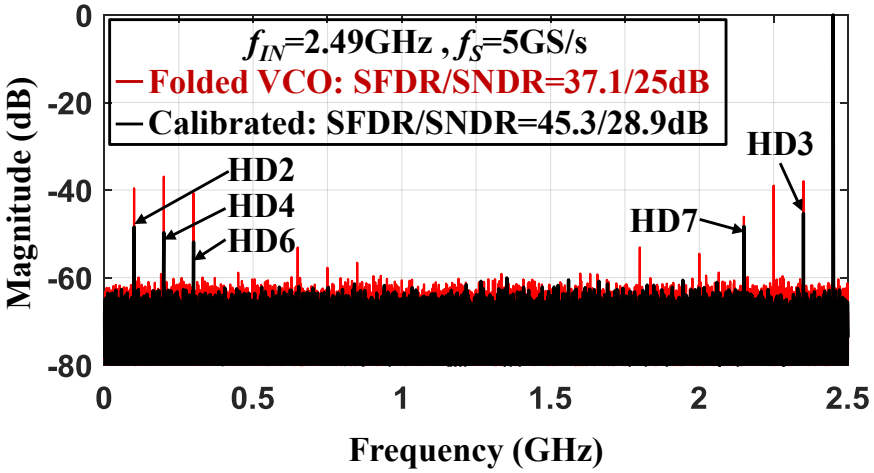

(c)

Fig. 4.59. The measured output spectrum of the calibrated reconfigurable ADC output (2^{16}-point FFT) in response to 0.7 V_{PP} near Nyquist input sinusoid. (a) 200 MS/s CDS SAR-mode. (b) 800 MS/s 2× TI CDS SAR-mode. (c) 5 GS/s 4× TI Flash mode.

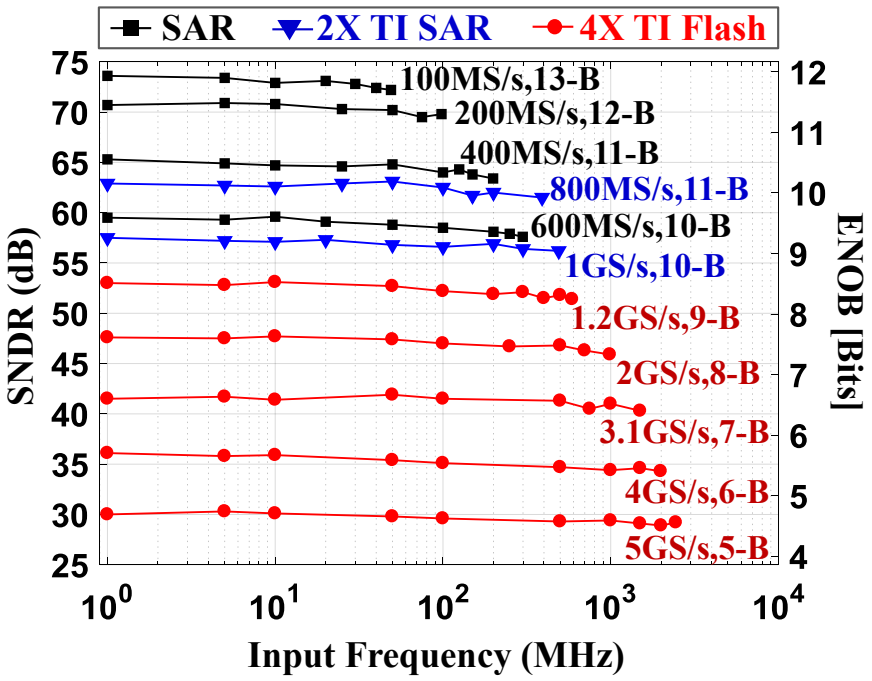

Fig. 4.60. SNDR versus input frequency plot for the different ADC modes.

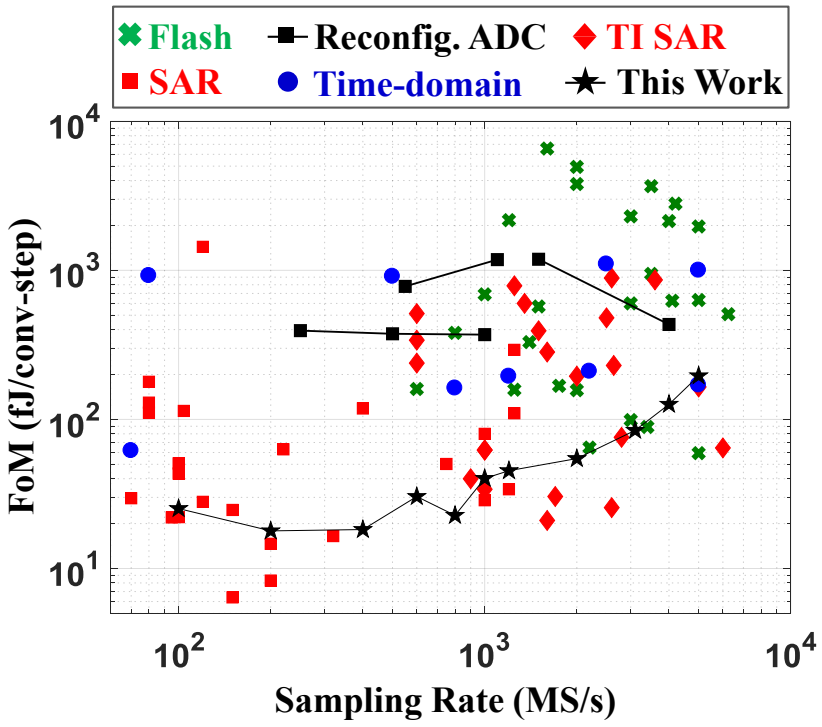

Fig. 4.61. FoM plot for this work compared with previously published work from 2004-2017 from ISSCC/VLSIC/CICC/A-SSCC/JSSC/TCASI.

Table 4.6
Comparison With State-of-the-art Reconfigurable ADCs

	[181]			**[182]**					**[190]**				**This Work**									
Process (nm)	130			65					16				65									
Supply (V)	1.2			1.2					0.9				1V (TDC) , 1.2V (VCO)									
Area (mm^2)	0.55			0.15					0.018				0.124*									
Mode	TI Single Slope			Two-Step			Flash		Flash				SAR				2× TI SAR		4× TI Flash			
Sampling Rate (GS/s)	0.25	0.5	1	1.5	1.5	1.5	4	4	4	4	4	4	0.1	0.2	0.4	0.6	0.8	1	1.2	2	3.1	4	5
ERBW (GHz)	> 0.5 f_S			0.6	0.6	> 0.5 f_S			> 0.5 f_S				> 0.5 f_S									
Resolution (Bits)	9	8	7	7	6	5	4	3	6	5	4	3	13	12	11	10	11	10	9	8	7	6	5
Power (mW)	25.3	26	26.5	41	35	29	20	12	34.4	23.5	16.9	10.9	8.4	9.01	9.9	11.3	19.8	21.2	16.5	17.6	19.5	21.4	22.3
Peak SNDR (dB)	50.1	45	40	39.1	34	28.6	24.2	19.6	32	28	24.2	18.4	73.6	70.8	66.3	59.5	63.9	57.5	53.1	47.7	41.9	36.1	30.3
SNDR @ Nyquist (dB)	49.95	44.6	38.8	32	28	26	23	18.5	30.6	27.6	24	18.3	72.2	69.8	64.4	57.6	62.5	56.2	50.7	45.9	40.3	34.3	28.9
Peak ENOB (dB)	8.03	7.18	6.35	6.21	5.36	4.46	3.72	2.96	5.02	4.36	3.72	2.76	11.93	11.5	10.72	9.59	10.32	9.26	8.53	7.63	6.67	5.7	4.74
ENOB @ Nyquist (bits)	8	7.11	6.16	5.02	4.36	4.03	3.52	2.78	4.8	4.3	3.7	2.75	11.7	11.3	10.4	9.27	10.1	9.04	8.24	7.33	6.4	5.4	4.51
Best-case FoM (fJ/conv)	387	358	324	461	712	877	377	383	265	286	320.6	402	21.4	15.7	14.6	24.4	19.3	34.6	37.2	44.3	61.8	102.6	166.8
FoM@Nyquist (fJ/conv)	399	380	364	1050	1421	1186	433	436	303	295	320	399	25.2	17.8	18.25	30.3	22.7	40.2	45.3	54.6	74.3	126.2	196

FoM = Power/(min(f_S,2ERBW) x 2^{ENOB})

* Including the additional area of the second SAR/DTC and folded VCO blocks for the 2× TI SAR Mode.

5. THE ANTENNA DESIGN

Building mm-Wave antennas for 5G transceivers faces several challenges. The most critical of which is the large path loss predicted by Friis formula [15] due to the high frequency propagation that requires high antenna gain for compensation. This dictates the use of directional antennas as opposed to the low/moderate gain omnidirectional antennas deployed in previous mobile generations [21]. Antenna implementation for mobile devices adds more requirements including small size, low cost, and simple fabrication using conventional PCB processes avoiding bulky [191] and 3D structures [192] for ease of integration. Moreover, high front-to-back radiation ratio (F/B) is required to minimize the undesired interaction between the array and the cellular RF circuitry. High radiation efficiency is also a major concern for better performance and increased battery life. Also, given that the array attains the phase shift required for beam scanning from an RF chip as illustrated in Fig. 5.1, the high gain should be achieved using the minimum number of array elements to reduce the number of phase shifters needed and hence reduce the complexity/power of the RF phase shifter chip and added parasitics of the chip-to-array routing. In this chapter, an antenna array for mobile devices is proposed which aims at achieving all those requirements with high-performance levels.

5.1 Background and Literature Review

Designing antennas for mm-Wave communications has recently been a hot topic. Many research teams have reported interesting antenna structures for both mobile devices and base stations. For base stations, arrays with dual or circular polarization and large number of antennas elements (100 or more) are the most convenient choice to provide high gain, and high channel capacity increasing the ability of accommodating many co-channel users in the cell covered by the base station [193] together with mitigating the multipath fading through polarization diversity [194],[195]. On the other hand, for mobile devices – which is the focus of this work – the antenna array needs to have a simple and compact structure for reduced cost and power. Hence, linearly polarized array is used for mobile devices for its simplicity [196]. In this case, diversity on the mobile device is attained using space diversity by placing two or more arrays on the mobile device [197].

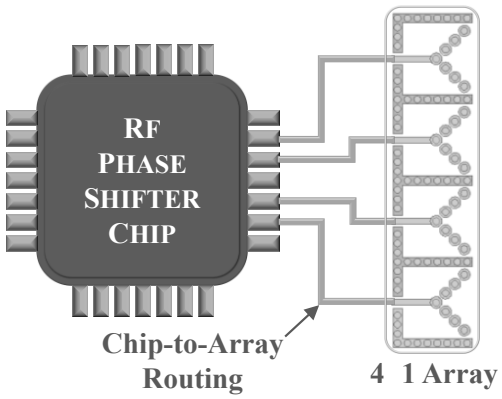

Fig. 5.1. Antenna Array fed from an RF Phase Shifter chip (Top View).

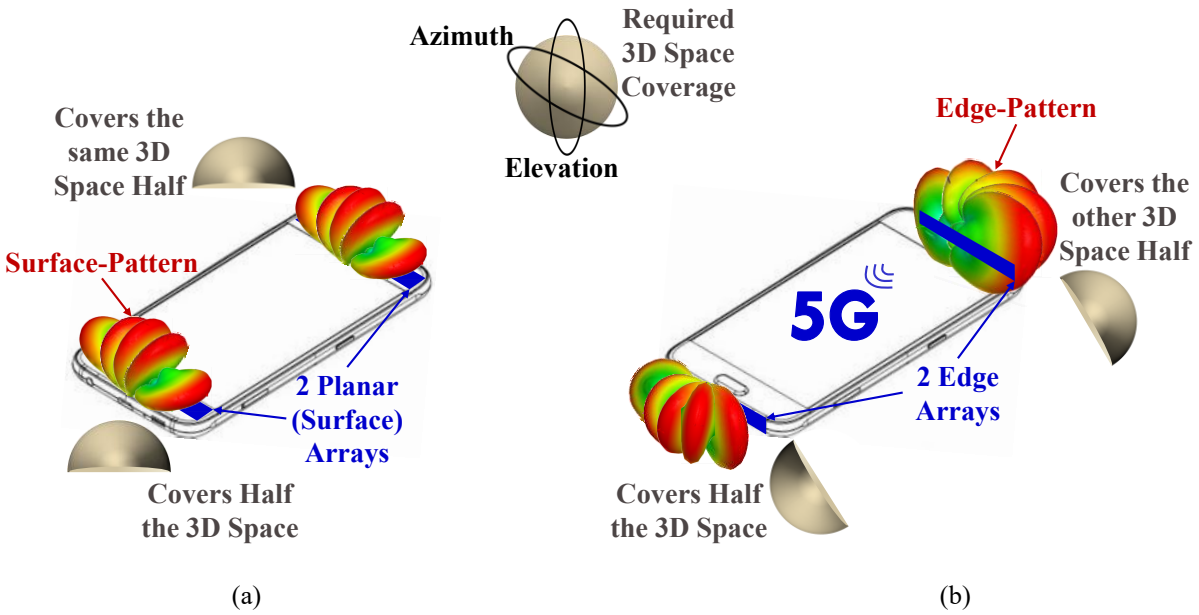

Fig. 5.2. Planar versus Edge Arrays for handset devices. (a) Planar Array. (b) Edge Array.

For the current wireless communications standards occupying the sub-6GHz spectrum, planar structures are the favorable choice for the antenna design owing to their ease of fabrication [198]–[201]. As the 5G wireless transceivers start moving towards the mm-Wave frequency range, the choice of the antenna structure needs to be revisited to account for the high frequency operation. This dictates the need for high antenna gain to mitigate the high free space path loss at the high mm-Wave frequency. In addition, at the high mm-Wave frequencies, antenna structures are subject to higher material losses which include substrate and conductor losses together with losses resulting from gluing multiple PCB layers together. This makes the planar antenna structures an appropriate choice for base stations for simplicity, lower cost and

lower material losses (and hence enhanced radiation efficiency and power consumption). However, for mobile devices, other aspects need to be considered (like the limited area and the need for complete 3D coverage) which make edge antennas a more convenient choice. This will be further discussed in the next section.

5.1.1 Planar Versus Edge of the Phone Antennas for mm-Wave Mobile Devices

For mm-Wave wireless communications, planar structures are easy to fabricate and are appropriate for base stations. However, they are not the best choice for mobile devices. This is mainly due to two reasons; first, the large LCD panel, battery, sensors, cameras, cellular RF circuitry, etc., limit the area available for placing the planar array and consequently limit the antenna gain. Second and most importantly, planar arrays are not capable of providing the full 3D space coverage required for mobile devices. Fig. 5.2(a) illustrates a mobile device packed with two planar arrays for MIMO. As the planar array aperture resides on the surface of the mobile device, it is referred to as Surface Array. The radiation pattern of both surface arrays – denoted by Surface-Pattern – covers the same space failing to provide the full space coverage (in the best case can only cover half the 3D spherical angle). To mitigate this issue and get better coverage, antenna arrays can be implemented at the edge of the mobile devices (Edge-Arrays) as shown in Fig. 5.2(b). By placing two edge-arrays at the two opposite phone edges, each can cover half of the entire 3D space resulting in full space coverage. The Edge-Pattern will denote radiation patterns from edge-arrays. Moreover, better coverage can be achieved by fan-beam edge-arrays that provide wider half-power beamwidth (HPBW) in the elevation plane [202]. It is worth to note out that planar antenna can be used in conjunction with the edge antenna to provide circular or dual polarization as in [203].

In the next two sections literature review on state-of-the-art planar and edge mm-Wave antenna design for base stations and mobile devices will be presented.

5.1.2 Literature Review on Planar Antenna Structures for 5G Wireless

Several planar antenna prototypes were proposed for 5G transceivers. In [204] a planar 4×4 2D series-fed patch array was proposed for 3D scanning with a reduced number of phase shifters where the $N\times N$ array uses 2N phase shifters instead of N^2. This resulted in reduced complexity and power consumption. The concept of reducing the number of phase shifters was revisited in

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[205] where a 3×3 2D series fed patch array was designed using only 4 phase shifters, that is the $N\times N$ array utilizes only $N+1$ phase shifters given that N is odd. In [206] a phased array with configurable polarization was implemented using two elements series-fed patch and substrate-integrated waveguide (SIW) based four slot sub-arrays as the array elements. The 32 interleaved patch and slot sub-arrays achieve peak gain of 22 dBi. In [207] a planar 4-element dipole array was presented where the individual element gain is 3 dBi while the 4×1 array gain is 7 dBi. In [208] a 4×2 patch array with improved circular polarization for the base station was proposed using a 45^{o} tilted microstrip feed. The 45^{o} tilted feed helped to improve the alignment between the impedance and axial ratio bandwidths and enhanced the impedance bandwidth compared to the conventional untilted feed. the A hybrid feed approach was applied to reduce the complexity of the array feed network. The array achieves 1.3 GHz impedance bandwidth and 370 MHz axial ratio bandwidth. In [209] a 4-element circular dense dielectric patch array was designed. The array achieves 12.48 dBi gain, 2.4 GHz bandwidth with 11^{o} half-power beamwidth (HPBW) in the H-plane and 34.4^{o} in the E-plane. The low HPBW in the E-plane limits the coverage capability of the array. In [210] an 8-element SIW antenna array using cavity-backed aperture coupled elements is presented. The sidelobe levels were reduced by using unequal T-junction dividers with Taylor distribution for the SIW feed. The array achieves a fan-beam with 13.9 dBi gain,-20 dB side lobe level, 2.3 GHz impedance bandwidth, HPBW of 10^{o} in the azimuth plane and 79^{o} in the elevation plane. In [211] a unit cell was designed using a four-layer proximity coupled stacked dual patch antenna. The main patch is fed by proximity coupling with the feed line while the second parasitic patch is used to add another resonance for enhanced bandwidth. The unit element achieves 7 dBi gain and 34.4% impedance bandwidth. In [212] a 2×4 slot antenna array was proposed showing 1.4 GHz impedance bandwidth with 10 dBi gain. In [213] a substrate integrated waveguide (SIW) multibeam 2×4 slot array employing a Butler matrix is presented. It achieves 4 GHz impedance bandwidth while providing $\pm 13^{o}$ and $\pm 55^{o}$ azimuth plane beams with 11 dBi gain. In [214] an 8-element circularly polarized SIW antenna array was implemented with 1.6 GHz impedance bandwidth, 1.2 GHz axial ratio bandwidth while providing 3 dBi gain. In [215] a dual-band aperture antenna array is proposed to operate in the 28 GHz band and the E-band. For the 28 GHz band, a 2×2 stripline-fed U-shaped patch array is utilized while 4×4 slot apertures array fed using SIW is employed for the E-band. The 28 GHz array achieves an input impedance bandwidth of 5 GHz with 9 dBi gain.

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5.1.3 Literature Review on Edge Antenna Structures for 5G Wireless

A couple of interesting edge arrays for 5G mobile devices operating in the 28-GHz band was reported in the literature. In [216], a 4-element open-ended SIW antenna was implemented on the edge of a multilayer PCB providing wide beamwidth (180^o in the E-plane and 90^o in the H-plane) with 3.9 GHz bandwidth and gain of 3 dBi. However, it suffers from low gain and large back radiation. A 16-element linearly polarized mesh grid array was built at the edge of the cell phone using a standard 10 layer FR-4 PCB in [217], [218]. The antenna is characterized by a fan-beam like radiation pattern. The mesh-grid is created by arranging the vias in a tightly spaced periodic manner across 7 layers of the PCB. The array is fed by a microstrip line located on the fifth PCB layer. The 16 element mesh grid array achieves 3 GHz input bandwidth and 10.9 dBi gain with $\pm 75^o$ steerable beam in the azimuth plane. In [203] a dual polarized antenna array was proposed utilizing two discrete antenna elements as the unit cell of the array. The first element is a planar Yagi-Uda antenna built on the fourth and fifth layers of the FR-4 PCB providing the horizontal polarization. The vertical polarization is attained using the second element designed as mesh–grid Yagi-Uda antenna. The 16-element phase array constructed using eight of the two-discrete antenna elements showed 1 GHz impedance bandwidth and 10 dBi gain. The large number of elements in [203], [217], [218] power/complexity of the RF phase shifter chip and feeding network and degrades the array efficiency, gain, and F/B. In [219], a dipole array loaded substrate-integrated horn antenna is presented. It achieves 9 – 12 dBi gain over 12 GHz bandwidth. However, it suffers from degraded F/B of 10 – 20 dB and HPBW in the elevation plane of less than 60°. In [220], an 8×1 cavity-backed slot antenna array was proposed. The single element and 8×1 array achieve 6.5 dBi and 15 dBi gain, respectively and 2.5 GHz bandwidth with only 70° HPBW in the elevation plane.

5.1.4 The Proposed Dipole Antenna for 5G Wireless Mobile Devices

This work proposes a mm-Wave substrate-integrated vertically-polarized electric dipole edge antenna for 5G mobile devices. By implementing the dipole using vertical vias at the PCB edge, the vertical-polarization is attained. The proposed electric dipole provides a wideband superior radiation performance with respect to gain, HPBW in the elevation plane ($HPBW_{ELEV}$), F/B and cross polarization (X-pol) owing to the following; first enhanced gain was attained by adding parasitic vias in front of the dipole. Second, the parasitic vias are flared in V-shaped fashion with

each via split into two halves for improved $HPBW_{ELEV}$. Finally, for F/B enhancement, the dipole structure is surrounded by a via fence. In contrast to the magneto-electric dipole in [221] whose fence does not affect the radiation pattern, the via-fence in the proposed electric dipole influences the radiation pattern and by the proper choice of its design parameters, higher F/B can be achieved. Compared to previously reported mm-Wave edge arrays, the fabricated 4×1 array achieves more than 15 dB higher F/B, more than 23º higher $HPBW_{ELEV}$, together with lower cross-polarization, higher radiation efficiency, compact size, high gain from only 4-element array (which simplifies the design of the RF phase shifter chip) and wide bandwidth.

5.2 The Proposed Electric Dipole Design Procedure

The dipole is a convenient choice for handset devices owing to its low profile and high radiation efficiency. In this section, the proposed dipole will be presented. The antenna was designed and simulated using the ANSYS HFSS electromagnetic solver. Throughout the paper, the elevation is taken as the y-z plane while the azimuth is the x-y plane as illustrated in Fig. 5.3. First, the single dipole behavior will be discussed. Then the design perspectives for choosing each of the parameters of the proposed dipole will be introduced and backed with parametric study. Since the proposed dipole is designed with center frequency at 28 GHz, all the optimizations and parametric studies were performed at this frequency. In the sub-6GHz mobile generations, the antennas were built on FR-4 substrates for its low cost and ease of integration with the rest of the RF circuitry which were also implemented on FR-4 substrates. However, as 5G is moving towards higher frequencies in the mm-Wave range, the high dielectric loss of the FR-4 at such high frequencies will limit the efficiency of both the antenna and the RF circuitry. Hence, a substrate with lower dielectric losses is chosen for this work to implement the mm-Wave antenna. The proposed dipole is designed and fabricated using the Rogers RO5880 substrate (with dielectric constant $\varepsilon_r = 2.2$ and loss tangent $tan\ \delta = 0.0009$). This substrate has been successfully used in [220] for integration within the handset device.

5.2.1 Single Dipole in Air/Dielectric Slab

The radiation pattern and peak directivity of an electric dipole depend on the dipole length and the medium where it is placed [222]. Fig. 5.3(a) illustrates the geometry of an electric dipole in air. The dipole is realized using two metallic cylinders with diameter $d_{DIPOLE} = 0.6\ mm$. The

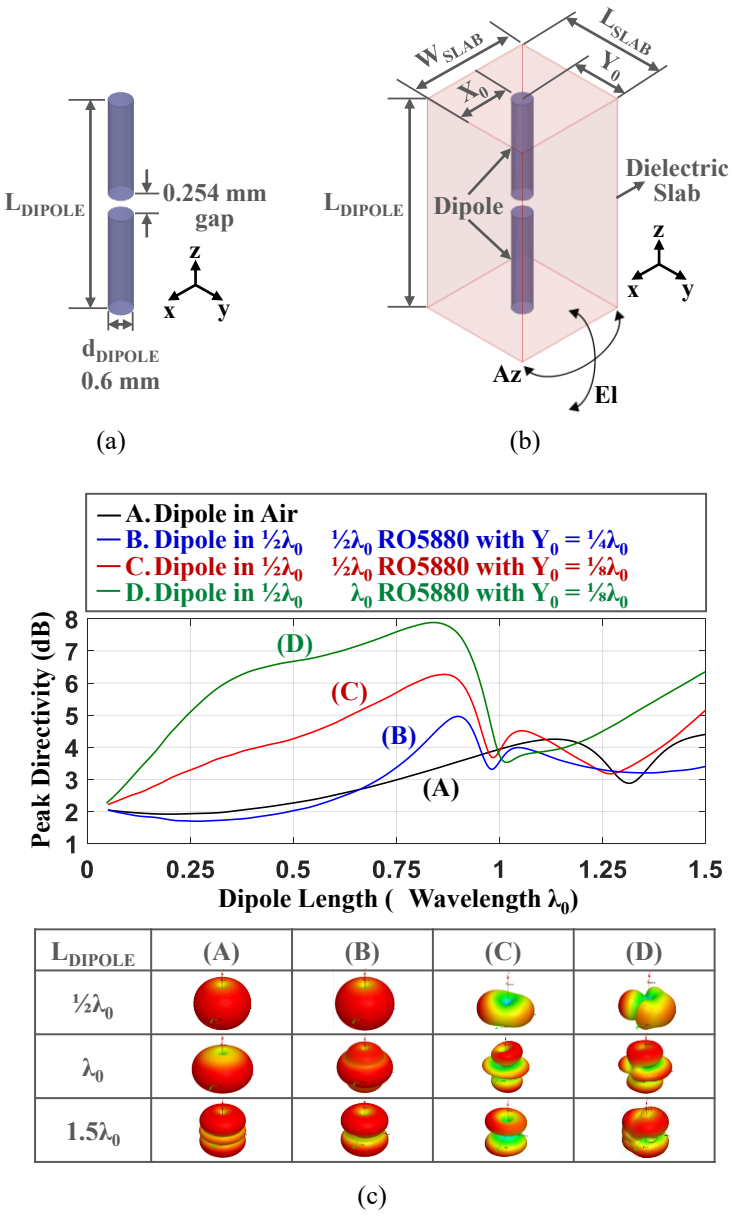
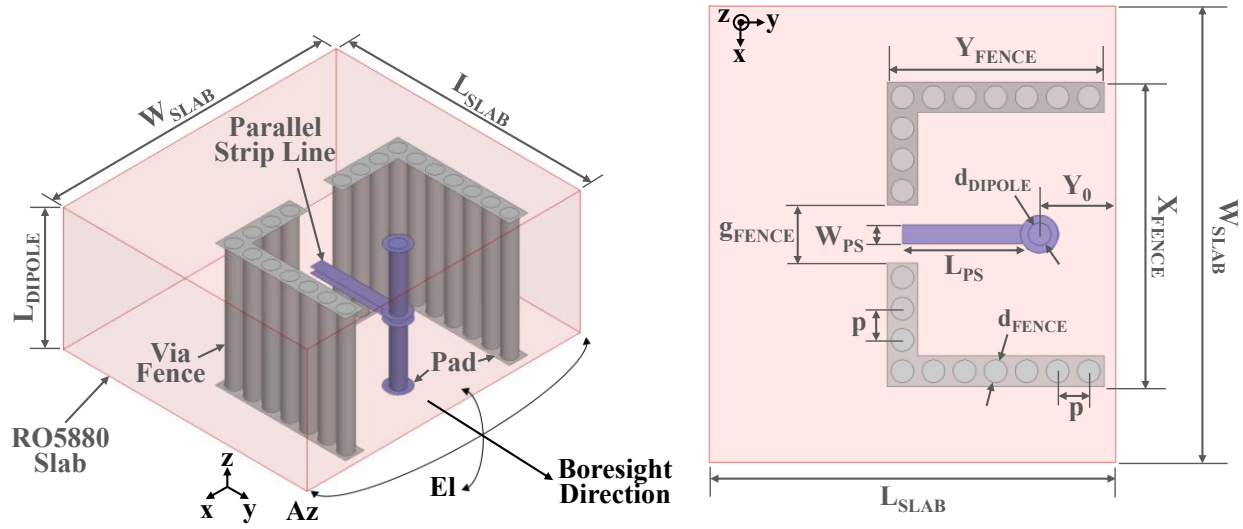


Fig. 5.3. (a) Geometry of electric dipole in air implemented using two metallic cylinders with a gap in between to realize the two dipole arms. (b) Geometry of electric dipole inside dielectric slab. (c) The simulated 3D radiation pattern and peak directivity versus dipole length at 28GHz with $X_0 = ½\ W_{SLAB}$ and varied L_{SLAB}, W_{SLAB}, and Y_0.

overall dipole length is denoted by L_{DIPOLE}. The gap between the two dipole arms is *0.254 mm*. The simulated 3D radiation pattern and peak directivity versus L_{DIPOLE} for the electric dipole in air at 28 GHz are shown in *case A* of Fig. 5.3(c) where the dipole length is expressed in terms of the free space wavelength (λ_0) at 28 GHz. Placing the dipole in a dielectric slab greatly influences its performance [223], [224]. Fig. 5.3(b) illustrates the geometry of the dipole inside a Rogers RO5880 dielectric slab. The slab length and width are L_{SLAB} and W_{SLAB}, respectively, while its thickness is equal to L_{DIPOLE} where the dipole spans the whole slab thickness. The



(a) (b)

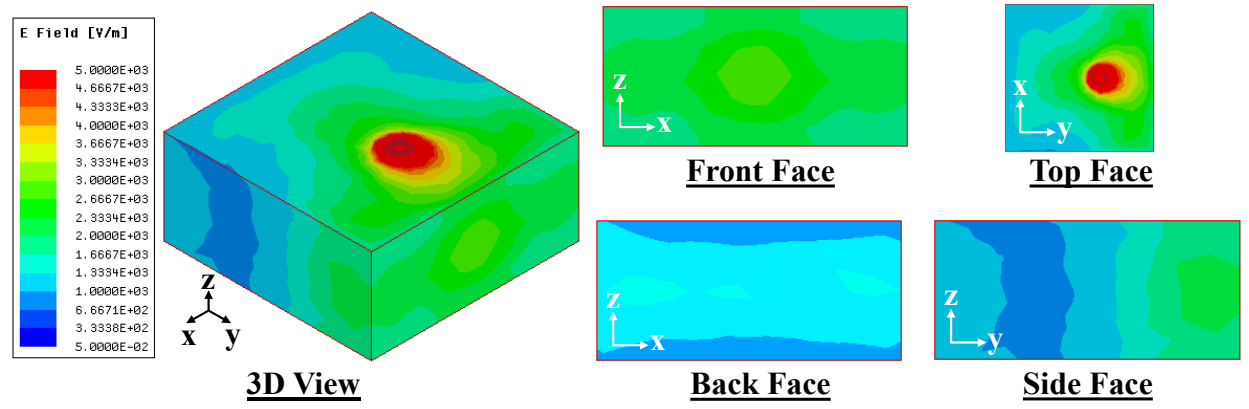
Fig. 5.4. Geometry of electric dipole with via fence. (a) Isometric 3D View. (b) Top View.

dipole is implemented as two 0.6 mm diameter metallic vias in the slab. The *0.254 mm* dipole gap is implemented using an *0.254 mm* thick Rogers R05880 slab. The clearance of the dipole from the slab edge is X_0 and Y_0 in the x- and y-directions, respectively. The dipole is placed at the center of the x-axis, i.e., $X_0 = ½W_{SLAB}$. *Cases B, C, and D* of Fig. 5.3(c) illustrate the simulated 3D radiation pattern and peak directivity versus dipole length of the dipole within the RO5880 slab at 28 GHz for different L_{SLAB}, W_{SLAB}, and Y_0. It can be noted that the slab dimensions and the dipole clearance from the slab edge have a great impact on the antenna performance where the larger the slab dimensions (W_{SLAB} and L_{SLAB}) and the closer the dipole from the slab edge (smaller Y_0), the higher the peak directivity.

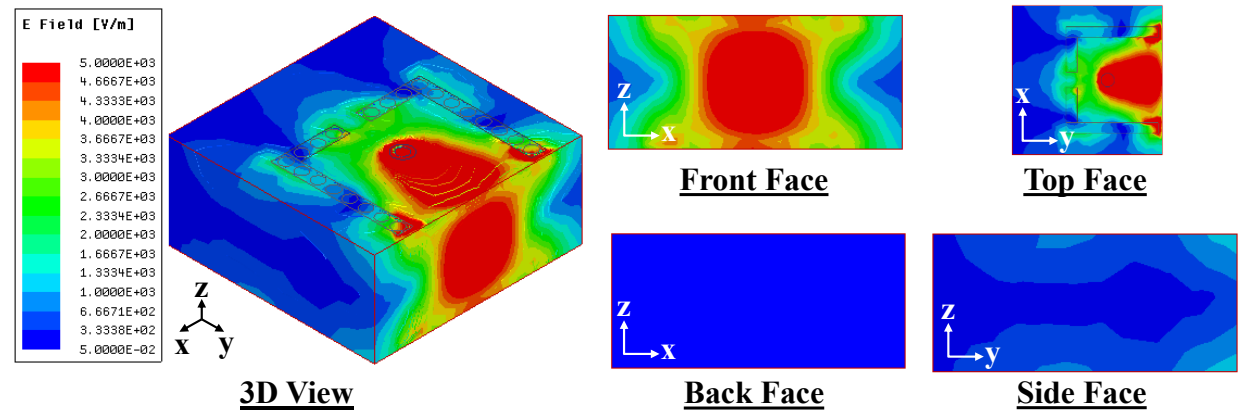
However, a standalone dipole in the slab is not suitable for 5G due to its degraded front-to-back radiation ratio and pattern-dependence on the slab dimensions. Hence, the dipole is surrounded by a via-fence to mitigate these issues.

5.2.2 Dipole With Via Fence

The first step in designing the proposed dipole structure is to surround the dipole with a via-fence as shown in Fig. 5.4 to suppress the back radiation and control the radiation pattern. The dipole is fed through a parallel-strip (PS) line of length L_{PS} and width W_{PS}. The gap between the two dipole arms is 0.254 mm. The fence is constructed using vias with diameter d_{FENCE} of 0.6 mm and pitch p of 0.83 mm and has overall dimensions of $X_{FENCE}\times Y_{FENCE}\times L_{DIPOLE}$. The dipole is centered within



(a)



(b)

Fig. 5.5. Complex magnitude electric field distribution for the dipole. (a)Without Via-Fence. (b) With Via-Fence.

the fence along the x-axis and its clearance from the substrate edge along the y-axis is Y_0. For practical implementation, the platted metallic vias require the presence of metallic pads. The pads are implemented with 1 mm diameter. The fence effect is demonstrated in Fig. 5.5 by showing the electric field distribution in its presence/absence. From which we can conclude the following; (1) the fence is able to confine the fields. This is apparent from the 3D View field distribution where the electric field in the absence of the fence is distributed everywhere while for the dipole with fence case the electric field is mainly confined within the fence and attenuates outside it. (2) The fence has the ability to reduce the back radiation. This is clear from the electric field distribution on the back face which is very weak for the dipole with the fence while it has significant value in the absence of the fence. (3) By properly designing the fence parameters, wide HPBW can be achieved in the elevation. This is concluded from the uniform electric field distribution on the front face of the dipole with the fence where uniform field distribution can be monitored along the z-axis.

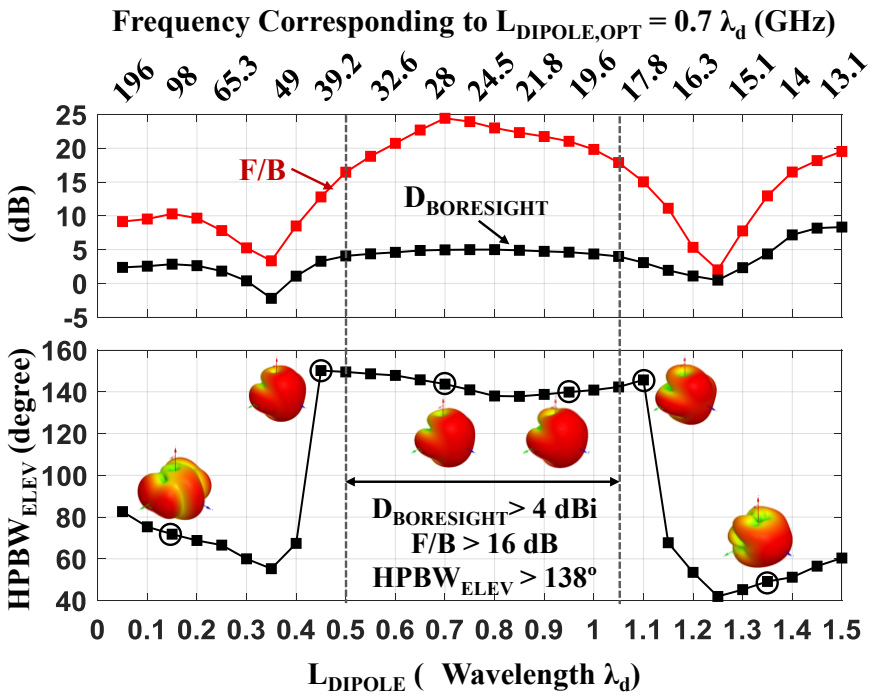


Fig. 5.6. Simulated Directivity, F/B and $HPBW_{ELEV}$ versus dipole length for $X_{FENCE} = Y_{FENCE} = \lambda_d$ and $Y_0 = ½\ \lambda_d$.

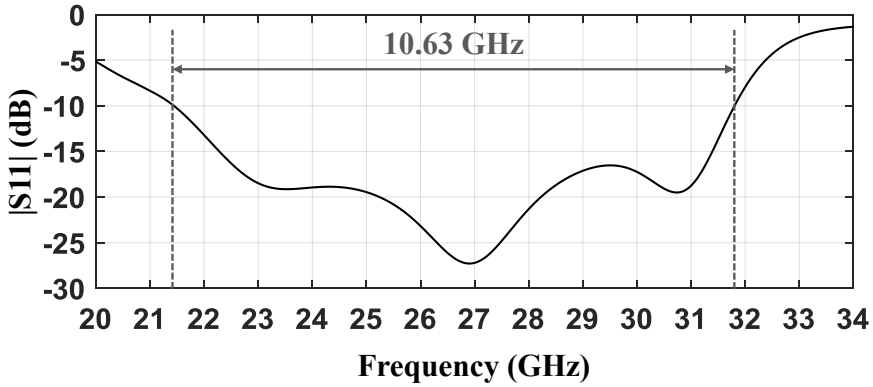


Fig. 5.7. Simulated |S11| for the $0.7\lambda_d$ dipole.

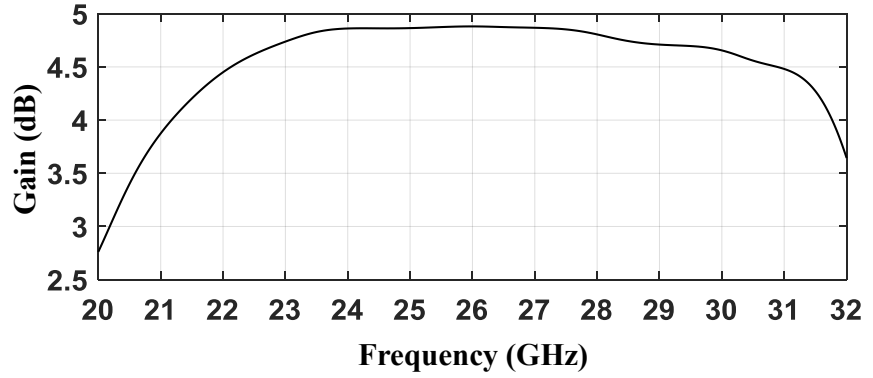


Fig. 5.8. Simulated Gain for the $0.7\lambda_d$ dipole.

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(4) The peak directivity of the dipole with the fence is higher than that in the absence of the fence that is evident from the fact that the dipole with fence has higher peak electric field on the front face compared to the case where the fence is absent.

From another perspective, the dipole surrounded with via fence can be thought of as a cavity-backed antenna [225]–[227]. With the chosen diameter d and pitch p of the via fence that satisfies the condition $p<2d$ for substrate integrated metallic wall [228], the fence creates three metallic walls surrounding the dipole leaving the front face open for radiation.

For the proposed dipole structure to satisfy the 5G requirements of high directivity, high F/B and wide fan-beam with high $HPBW_{ELEV}$, all the dipole design parameters need to be thoroughly studied and optimized. The design parameters at hand are L_{DIPOLE}, X_{FENCE}, Y_{FENCE}, and Y_0. First, with the fence dimensions and Y_0 fixed, the effect of the dipole length was studied. Fig. 5.6 illustrates a plot of the simulated Directivity, F/B and $HPBW_{ELEV}$ versus the dipole length expressed in terms of the wavelength (λ_d) inside the RO5880 slab. It is important to note that we are more interested in the directivity at the boresight direction ($D_{BORESIGHT}$) not just the peak directivity. Around the optimal design points, both the peak directivity and boresight directivity are coincident. From the obtained results it can be noted that the dipole can operate with stable radiation performance over dipole lengths ranging from $0.5\times\lambda_d$ to $1.05\times\lambda_d$ achieving F/B > 16 dB, $HPBW_{ELEV}$ > 138º and Directivity > 4.03dBi. The optimal dipole length was chosen as $L_{DIPOLE,OPT} = 0.7\times\lambda_d$ since it has superior F/B performance of 24.4 dB together with high directivity of 5 dBi and high $HPBW_{ELEV}$ of 143.6º. As illustrated in Fig. 5.6, the $0.7\lambda_d$ dipole (at 28 GHz) can maintain superior radiation performance over a wide bandwidth. For example, in this case, stable radiation patterns with directivity of around 5 dBi, F/B > 20 dB and $HPBW_{ELEV}$ > 138º are obtained from 19.6 GHz to 34.5 GHz (that is 55.19% bandwidth). The simulated S11 plot for the $0.7\lambda_d$ dipole is illustrated in Fig. 5.7 showing 40.88 % bandwidth. Also, the simulated gain versus frequency plot for the $0.7\lambda_d$ dipole is illustrated in Fig. 5.8.

Second, since the fence is of great influence on the antenna performance, its design parameters (X_{FENCE} and Y_{FENCE}) will be studied. A small gap g_{FENCE} is created in the fence allowing the PS line out to be connected to the rest of the feeding structure where g_{FENCE} is taken as 1 mm. The fence dimensions were swept with the dipole placed in the middle of the fence ($Y_0 = ½\ Y_{FENCE}$). Fig. 5.9 shows the simulated Directivity, F/B and $HPWB_{ELEV}$ versus Y_{FENCE} for different values of X_{FENCE}. Optimal performance is attained for $Y_{FENCE} = X_{FENCE} = \lambda_d$.

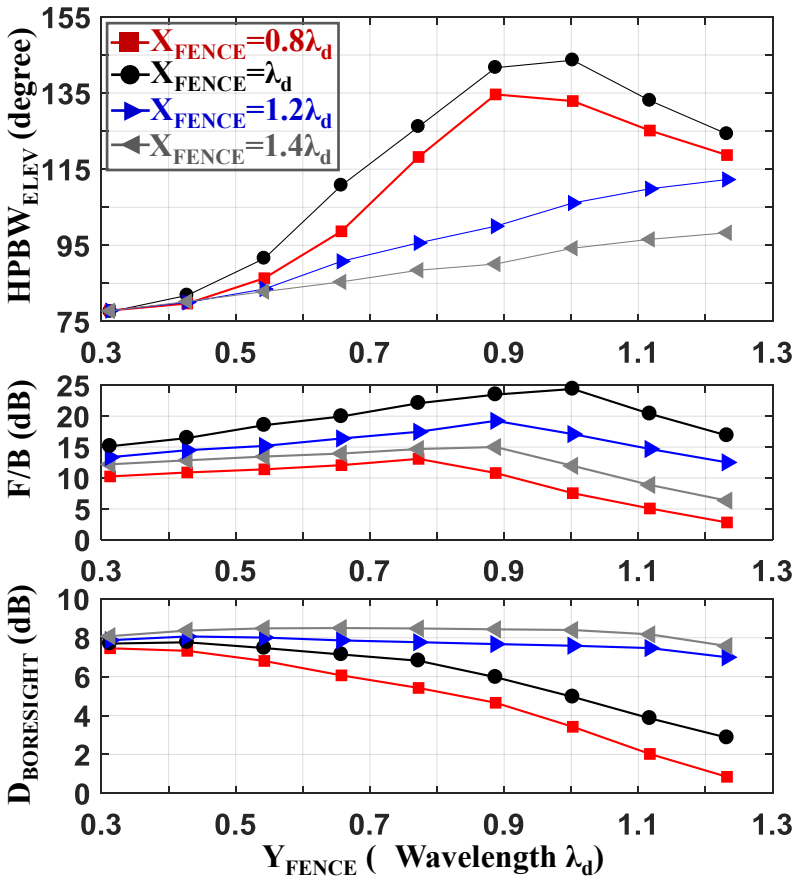


Fig. 5.9. Simulated Directivity, F/B and $HPBW_{ELEV}$ versus Y_{FENCE} for different X_{FENCE} with the $0.7\lambda_d$ dipole placed in the middle of the fence (Y_0 = ½ Y_{FENCE}).

The last parameter that needs to be studied and optimized to further enhance F/B and $HPBW_{ELEV}$ is Y_0. Fig. 5.10 shows the simulated Directivity, F/B and $HPBW_{ELEV}$ versus Y_0 where the optimal $HPBW_{ELEV}$ and F/B are achieved at Y_0 slightly higher than $½\lambda_d$, exactly at $0.543\lambda_d$. It can be noted that unlike the ME dipole in [221] whose fence has no effect on its radiation performance, the fence for the electric dipole can influence the radiation pattern which adds more degree of freedom to the design. By the proper choice of the fence parameters, the proposed electric dipole achieves 5.1 dBi directivity, 145.39º $HPBW_{ELEV}$, 31.67 dB F/B and less than –43 dB cross polarization as illustrated in Fig. 5.11, compared to 5 dBi directivity, 110º $HPBW_{ELEV}$, 24 dB F/B and –31 dB cross polarization from the ME dipole. Table 5.1 provides a summary of the optimized design parameters for the electric dipole. It can be noted that both the electric dipole and ME dipole achieves approximately the same directivity. However, the gain of the proposed electric dipole is further enhanced by adding parasitic vias in front of the dipole as will be discussed in the next section.

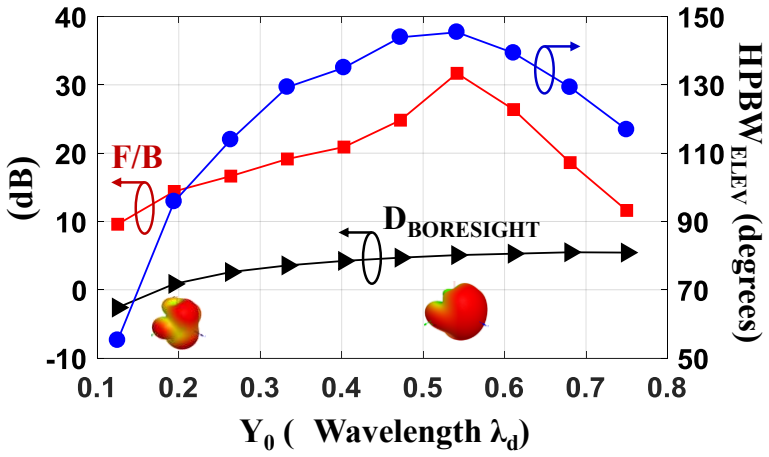


Fig. 5.10. The simulated Directivity, F/B and $HPBW_{ELEV}$ versus Y_0 for the $0.7\lambda_d$ electric dipole with $X_{FENCE} = Y_{FENCE} = \lambda_d$.

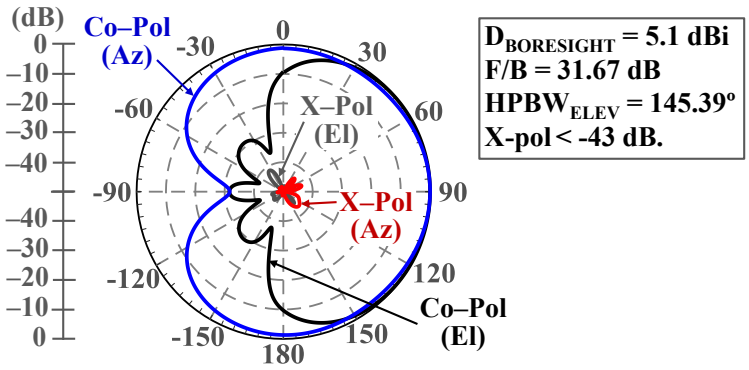
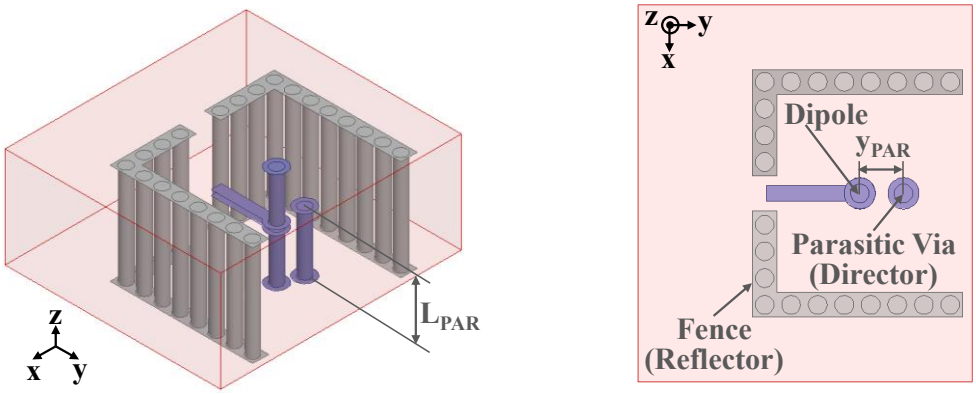


Fig. 5.11. The simulated radiation pattern of the optimized 28 GHz dipole in both the elevation and azimuth planes.

Table 5.1
The Optimized 28 GHz Dipole Design Parameters

L_{DIPOLE}	X_{FENCE}	Y_{FENCE}	Y_0
$0.7\times\lambda_d$	λ_d	λ_d	$0.543\times\lambda_d$



(a) (b)

Fig. 5.12. Geometry of electric dipole with single unsplit parasitic via. (a) Isometric 3D View. (b) Top View.

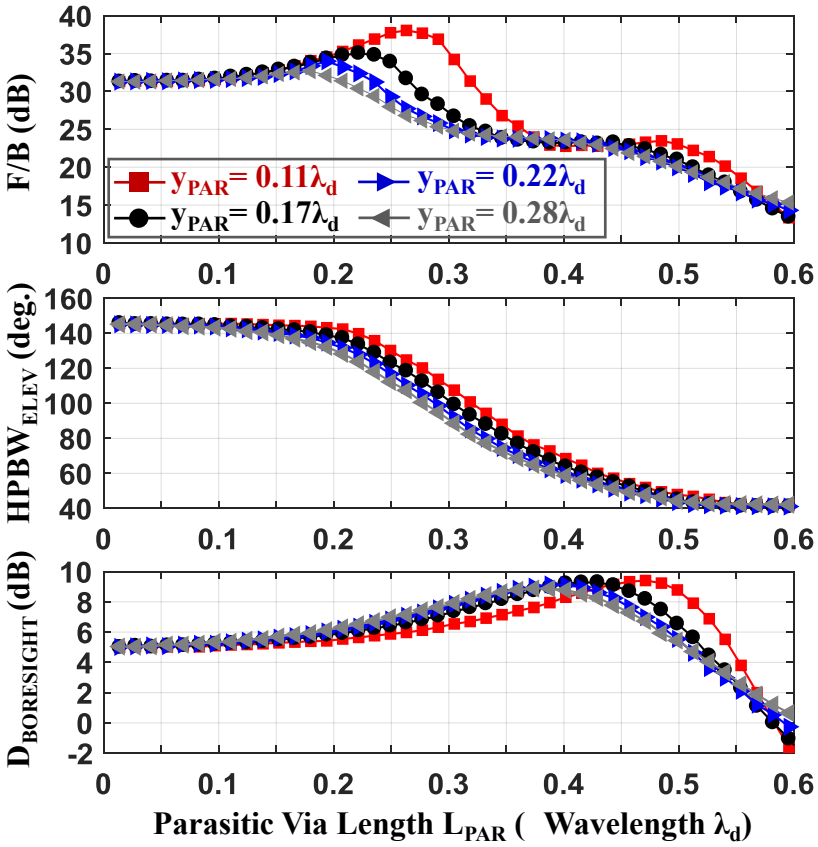
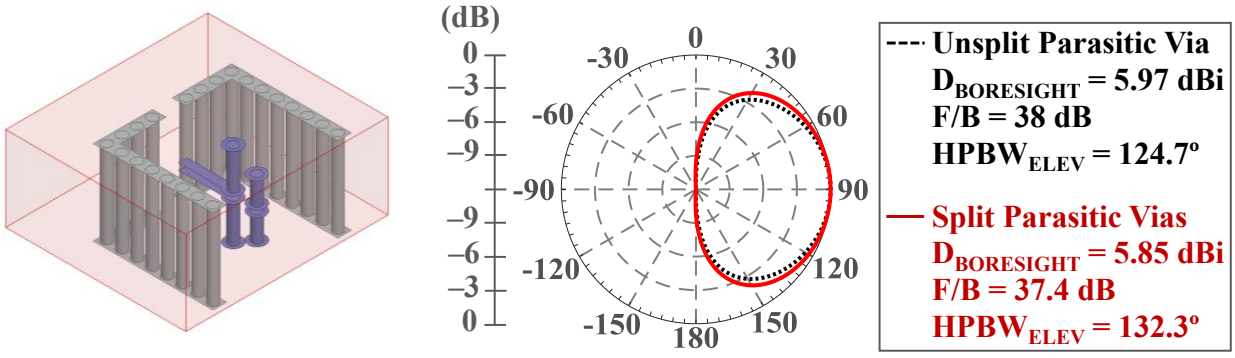


Fig. 5.13. Simulated Directivity, F/B and $HPBW_{ELEV}$ versus L_{PAR} for different y_{PAR}.

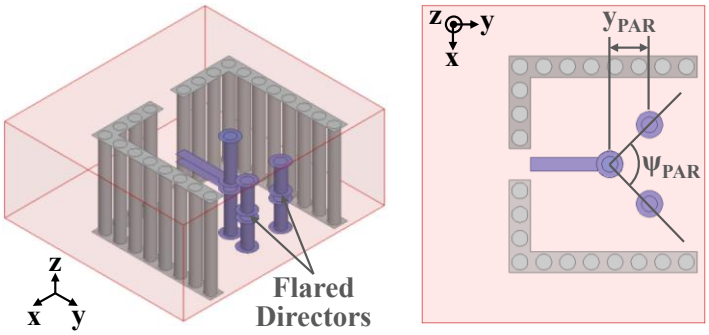
5.2.3 Adding Parasitic Vias for Gain Enhancement

Now that the via-fence is optimized for enhanced F/B and $HPBW_{ELEV}$, the structure needs to be modified for higher directivity. The challenge here is to preserve the high $HPBW_{ELEV}$ together with the enhanced directivity. For directivity enhancement, additional parasitic vias are added in front of the dipole. The geometry of the dipole with a single parasitic via in front of it is illustrated in Fig. 5.12. The parasitic via diameter is taken as d_{PAR} = 0.6 mm similar to that of the dipole. Two parameters need to be studied for optimal performance, namely, the length of the parasitic via L_{PAR} and its separation from the dipole y_{PAR}. The simulated Directivity, F/B and $HPWB_{ELEV}$ versus L_{PAR} for different y_{PAR} are illustrated in Fig. 5.13. The closer the parasitic via to the dipole (i.e., the smaller y_{PAR}), the higher are the F/B and $HPBW_{ELEV}$. Regardless of y_{PAR}, for L_{PAR} less than $\frac{1}{2}\lambda_d$, the directivity is higher than the 5.1 dBi achieved without the parasitic via. Hence, y_{PAR} is selected as $0.11\lambda_d$ for higher $HPBW_{ELEV}$ and F/B. For $y_{PAR} = 0.11\times\lambda_d$, optimal F/B is attained at L_{PAR} close to $0.25\lambda_d$, exactly at $L_{PAR} = 0.263\lambda_d$ achieving F/B of 38 dB with the



(a) (b)

Fig. 5.14. (a) Geometry of electric dipole with the parasitic via split into two halves. (b) Zoomed-in Radiation pattern in the elevation plane of the dipole with unsplit/split parasitic via.



(a) (b)

Fig. 5.15. Geometry of the dipole with split parasitic vias flared in a V-fashion. (a) 3D View. (b) Top View.

corresponding $HPBW_{ELEV}$ of 124.7º and directivity of 5.97 dBi. Thus, adding a single parasitic via in front of the dipole results in 0.9 dB improvement in the directivity and 6.3 dB improvement in the F/B at the cost of reduced $HPBW_{ELEV}$ (degraded by 19º).

To restore the degraded $HPBW_{ELEV}$, two techniques are proposed. First, the parasitic via is split into two halves separated by a gap equal to the dipole gap as illustrated in Fig. 5.14(a). This does not only enhance the $HPBW_{ELEV}$ but also reduces the fabrication complexity. The unsplit parasitic via is practically realized as buried via which is hard to fabricate while splitting it into two halves results in a simpler fabrication process. The zoomed-in radiation patterns in the elevation plane of the dipole with unsplit/split parasitic via are illustrated in Fig. 5.14(b) showing 7.6º improvement in the $HPBW_{ELEV}$ from the split via without much effects on the directivity and F/B.

The second proposed technique for enhancing $HPBW_{ELEV}$ is using a couple of parasitic vias flared in a V-fashion as illustrated in Fig. 5.15. The performance of the flared parasitic vias is

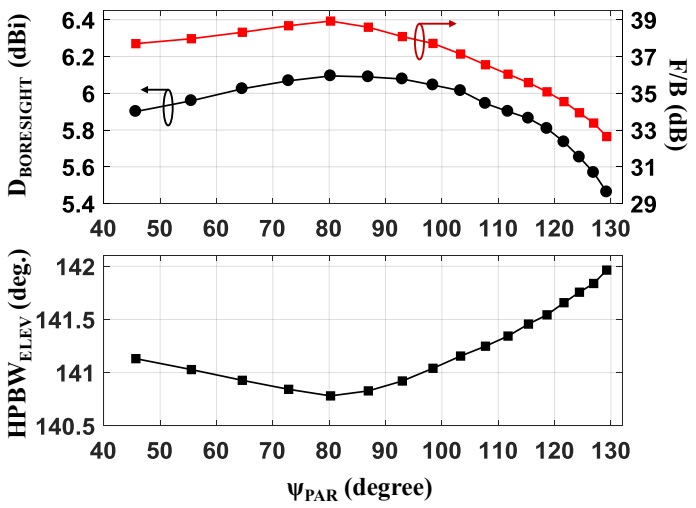
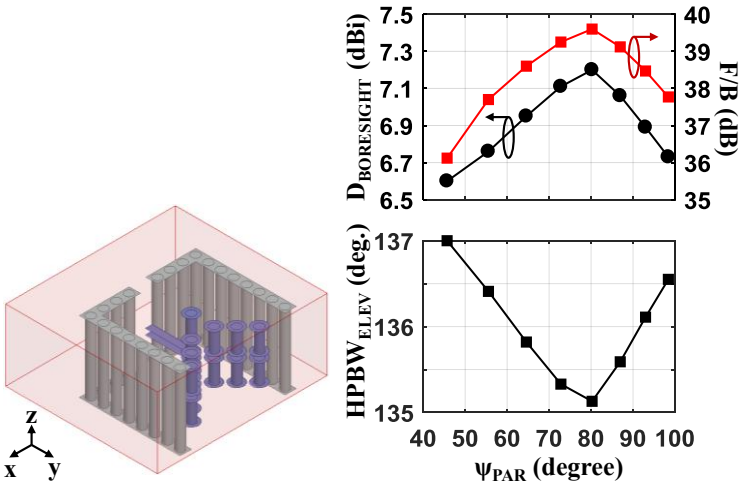


Fig. 5.16. Simulated Directivity, F/B and $HPBW_{ELEV}$ versus ψ_{PAR} for the electric dipole with single pair of flared V-shaped parasitic vias.



(a) (b)

Fig. 5.17. The electric dipole with three pairs of flared V-shaped parasitic vias. (a) Isometric 3D View. (b) Simulated Directivity, F/B and $HPBW_{ELEV}$ versus ψ_{PAR}.

governed by the flaring angle (ψ_{PAR}).To study the effect of the flared parasitic vias and the design parameter ψ_{PAR}, the simulated Directivity, F/B and $HPWB_{ELEV}$ versus ψ_{PAR} are reported in Fig. 5.16. It can be concluded that the proposed flared parasitic vias structure results in an improvement in the $HPBW_{ELEV}$ of at least 8.3º compared to the single parasitic vias case regardless of ψ_{PAR}. For optimal F/B and directivity, ψ_{PAR} is taken as 80º achieving 6.1 dBi directivity, 38.9 dB F/B and 140.8º $HPBW_{ELEV}$. It is worth to be noted that the improvement in the $HPBW_{ELEV}$ from the flared parasitic vias is accompanied with lower HPBW in the azimuth plane ($HPBW_{AZ}$). That is, the V-shaped flared parasitic vias have the ability to reshape the radiation pattern. This adds an

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additional design degree of freedom compared to the mesh grid antenna in [176] and the ME dipole in [221].

A single pair of flared parasitic vias results in 6 dBi directivity. For higher directivity, more parasitic vias can be added. Let the number of pairs of flared parasitic vias be denoted by N_{PAR}. Having parasitic vias with descending lengths resembling the Yagi-Uda structure [229] would require more PCB layers. The more the PCB layers, the higher the cost and the more complicated the fabrication process will be due to the increased number of fabrication steps. Adhesive prepreg material (for the Rogers 5880 substrate, the Rogers 3001 prepreg is used) is needed to stack each two PCB layers together. This requires repeated heating and pressing of the structure in a high-temperature furnace to assemble the different layers together. Also, the quality of the vias plating is important especially at high frequencies. The presence of vias at different PCB layers will require multiple drilling and platting operations. Also, it is possible to have the vias partially filled with prepreg resin. Hence, to reduce the fabrication complexity and avoid all the fabrication non-idealities, all the parasitic vias are designed with the same length. Using two pairs of flared parasitic vias ($N_{PAR} = 2$) increases the directivity by 0.8 dBi while a third pair ($N_{PAR} = 3$) adds another 0.4 dBi. Increasing the parasitic vias beyond that has no significant improvement on the directivity. Fig. 5.17 shows the finalized dipole structure with three pairs of equal length flared parasitic vias and the simulated Directivity, F/B and $HPWB_{ELEV}$ versus ψ_{PAR}. It worth to be noted that, by having another look at the equal-length V-shaped parasitic vias, it can view as a small substrate-integrated horn [219],[230]. This note is true since the parasitic via array with diameter $d_H = 0.6mm$ and pitch $p_H = 0.8\ mm$ satisfies the substrate integrated via wall design criteria $p_H < 2\times d_H$. Table 5.2 provides the optimized parasitic vias design parameters. The simulated radiation patterns in the elevation and azimuth planes in Fig. 5.18 shows 7.19 dBi directivity, 135.13º $HPBW_{ELEV}$, 39.6 dB F/B and cross polarization less than -44 dB. The simulated S11 plot for the dipole with flared parasitic vias is illustrated in Fig. 5.19 showing 10.04 GHz bandwidth.

5.3 The Feed Structure and Dipole Array

The two arms of the dipole are directly fed using a parallel-strip line. Having the parallel-strip line embedded within the dielectric slab results in back radiation. Those are suppressed using the via-fence. However, as the parallel strip line is extended outside the fence by $L_{PS,Ext}$ as illustrated in Fig. 5.20(a), the back radiation starts to increase with $L_{PS,Ext}$ that translates into degraded F/B

Table 5.2
The Optimized Parasitic via Design Parameters for the 28 GHz Dipole

L_{PAR}	y_{PAR}	ψ_{PAR}	N_{PAR}
$0.263\times\lambda_d$	$0.11\times\lambda_d$	80°	3

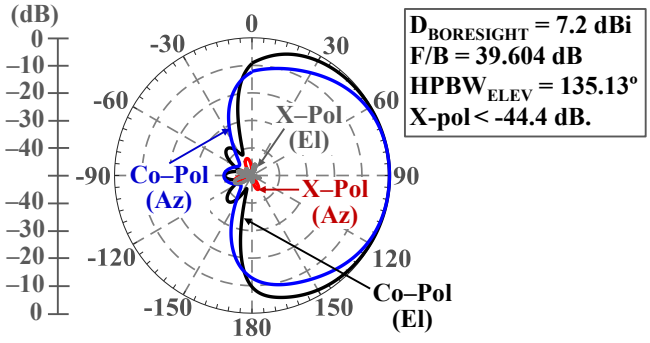


Fig. 5.18. The simulated radiation patterns of the optimized 28 GHz electric dipole with the flared parasitic vias in both the elevation and azimuth planes.

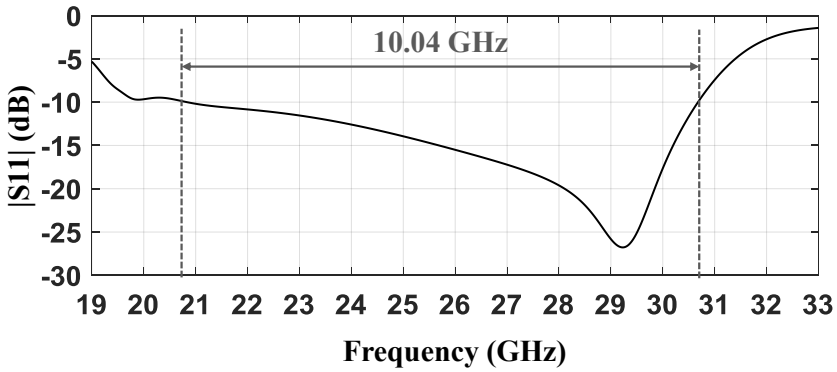
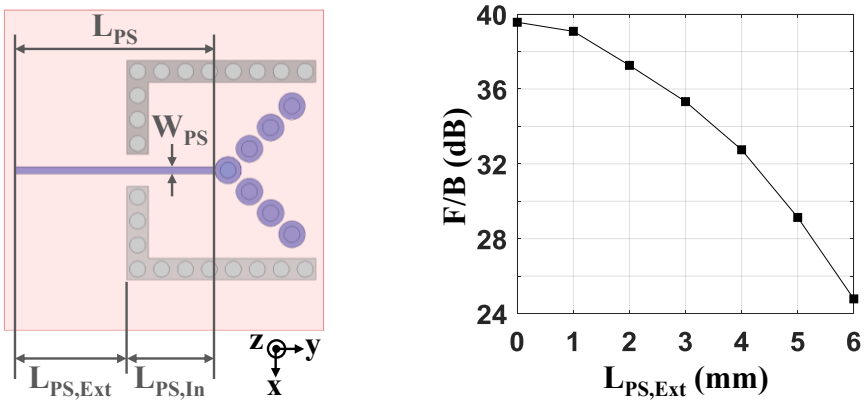


Fig. 5.19. Simulated |S11| for the dipole with flared parasitic vias.

as shown in Fig. 5.20(b). Hence the parallel strip line is stopped by the end of the fence. The feed structure outside the fence can be implemented using SIW. The SIW was chosen owing to its low profile, low radiation loss, easy integration with PCB circuits and compatibility with mm-Wave applications. This dictates the need for an efficient SIW-to-PS line transition. The dipole feed structure is illustrated in Fig. 5.21. The SIW via diameter d_{SIW} and pitch p_{SIW} were designed as $d_{SIW} = 0.6\ mm$ and $p_{SIW} = 0.8\ mm$ satisfying the SIW design rules to suppress leakage [231]

$$d_{SIW} < {}^{\lambda_d}/_{5} \tag{5.1}$$

$$p_{SIW} \leq 2 \times d_{SIW} \tag{5.2}$$



(a) (b)

Fig. 5.20. Effect of extending the PS line outside the fence. (a) Geometry of the electric dipole with extended PS line. (b) Simulated F/B versus $L_{PS,Ext}$ with W_{PS} = 0.25 mm and $L_{PS,In}$ = 3.2 mm.

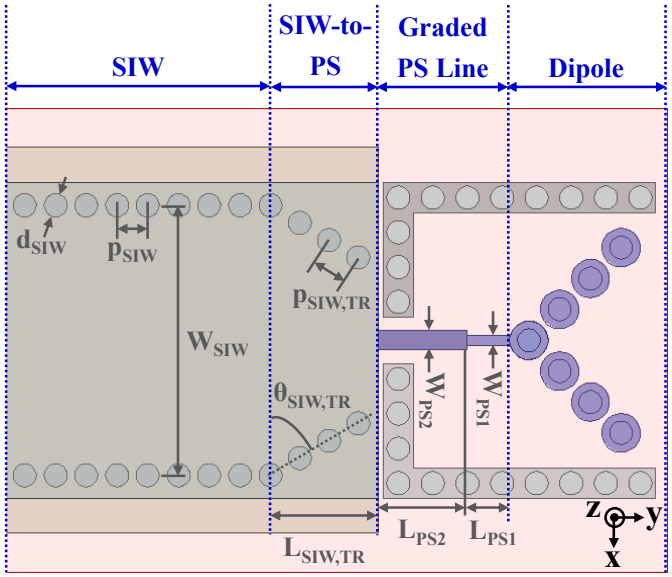


Fig. 5.21. Geometry of the electric dipole with Feed (Top View).

The SIW width W_{SIW} was designed as 7 mm based on the SIW design equations in [232]

$$W_{SIW} = \frac{W_{REC}}{\zeta_1 + \frac{\zeta_2}{\frac{p_{SIW}}{d_{SIW}} + \frac{\zeta_1 + \zeta_2 - \zeta_3}{\zeta_3 - \zeta_1}}} \tag{5.3}$$

$$W_{REC} = \frac{c}{2 \times f_c} \tag{5.4}$$

$$\zeta_1 = 1.0198 + \frac{0.3465}{p_{SIW}/d_{SIW} - 1.0684} \tag{5.5}$$

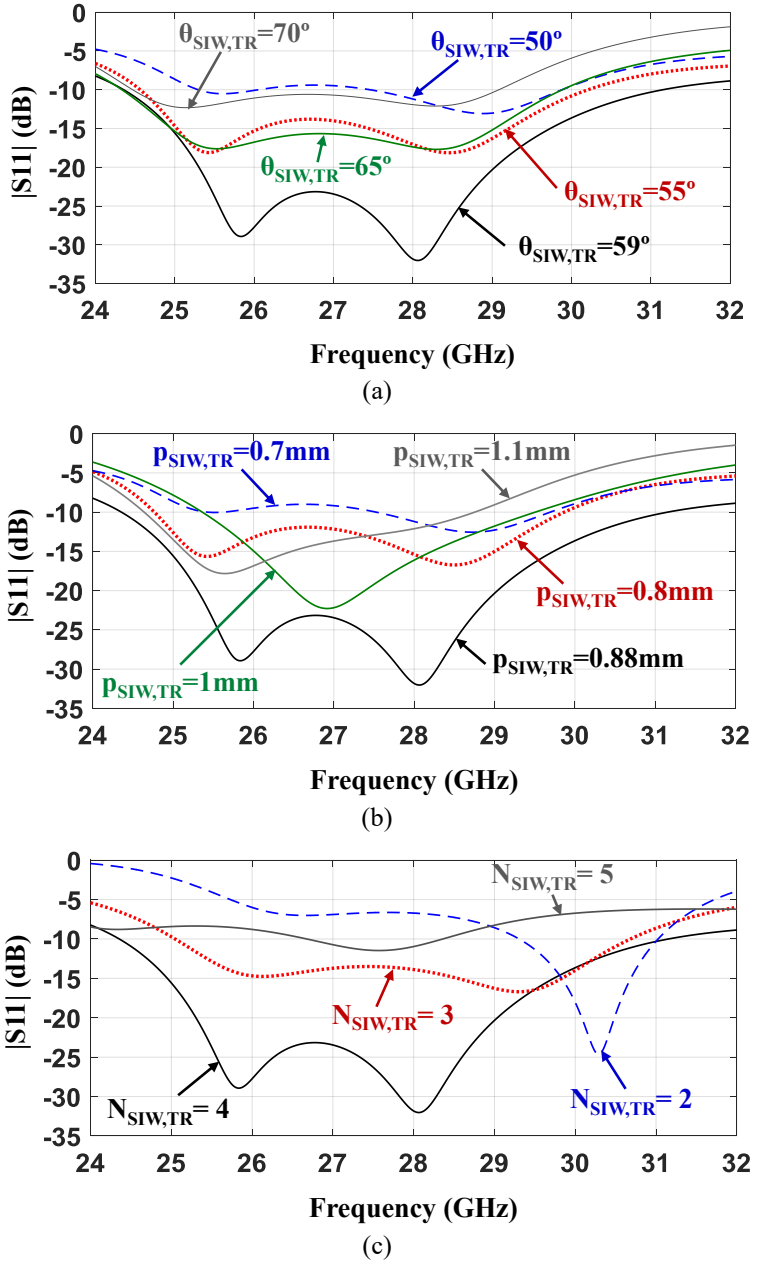


Fig. 5.22. SIW-to-PS line transition parametric study. (a) Simulated S11 for different $\theta_{SIW,TR}$ with $N_{SIW,TR}$ = 4 and $p_{SIW,TR}$ = 0.88 mm. (b) Simulated S11 for different $p_{SIW,TR}$ with $\theta_{SIW,TR}$ = 59º and $N_{SIW,TR}$ = 4. (c) Simulated S11 for different $N_{SIW,TR}$ with $\theta_{SIW,TR}$ = 59º and $p_{SIW,TR}$ = 0.88 mm.

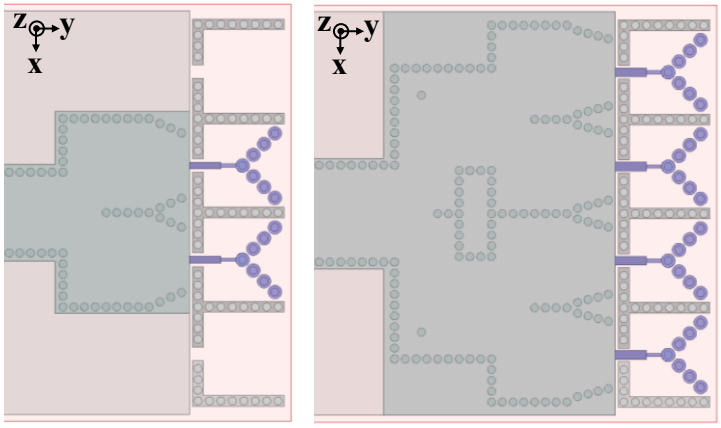
$$\zeta_2 = -0.1183 - \frac{1.2729}{p_{SIW}/d_{SIW} - 1.201} \tag{5.6}$$

$$\zeta_3 = 1.0082 - \frac{0.9163}{p_{SIW}/d_{SIW} + 0.2152} \tag{5.7}$$

where W_{REC} is the width of the conventional rectangular waveguide that is equivalent to the SIW, f_c is the cut-off frequency and c is the speed of light.

Table 5.3
Optimized SIW-To-PS Line Transition Design Parameters

W_{SIW}	d_{SIW}	p_{SIW}	L_{PS1}	W_{PS1}
7 mm	0.6 mm	0.8 mm	1.12 mm	0.25 mm
L_{PS2}	W_{PS2}	$\theta_{SIW,TR}$	$p_{SIW,TR}$	$N_{SIW,TR}$
2.3 mm	0.4 mm	59º	0.88 mm	4



(a) (b)

Fig. 5.23. Electric dipole array geometries (Top View). (a) The two-element array. (b) The 4-element array.

A couple of microstrip, CPW, and waveguide to PS line transitions were reported in the literature [233]–[238]. To the best of the authors' knowledge, the proposed transition is the first reported transition from SIW to PS line. The transition from the SIW to PS line is created in two stages. The first stage is constructed by gradually decreasing the width of the SIW using vias. For a smoother transition, the second stage is used by employing a graded PS-line instead of a single PS line. Since the PS line is required to be kept within the optimized dipole fence, only two levels of graded PS line are used. The SIW-to-PS line transition performance depends on the SIW taper angle $\theta_{SIW,TR}$ and its length $L_{SIW,TR}$ dictated by the number of SIW tapering vias $N_{SIW,TR}$ and its pitch $p_{SIW,TR}$. The graded PS line was optimized where the lengths and widths of its two stages were set as L_{PS1} = 1.12 mm, W_{PS1} = 0.25 mm, L_{PS2} = 2.3 mm, and W_{PS1} = 0.4 mm. For optimal performance of the SIW-to-PS line transition, its design parameters ($\theta_{SIW,TR}$, $N_{SIW,TR}$, $p_{SIW,TR}$) were thoroughly studied. To examine the effect of the taper angle $\theta_{SIW,TR}$ on the transition performance, Fig. 5.22(a) presents the S11 plot of the complete electric dipole structure for different $\theta_{SIW,TR}$ with $N_{SIW,TR}$ and $p_{SIW,TR}$ set to 4 and 0.88 mm, respectively where the optimal performance was found at $\theta_{SIW,TR}$ = 59º. A similar analysis was performed for parameters $p_{SIW,TR}$ and $N_{SIW,TR}$ as illustrated in Fig. 5.22(b) and Fig. 5.22(c). The optimized design parameters for the proposed transition are summarized in Table 5.3.

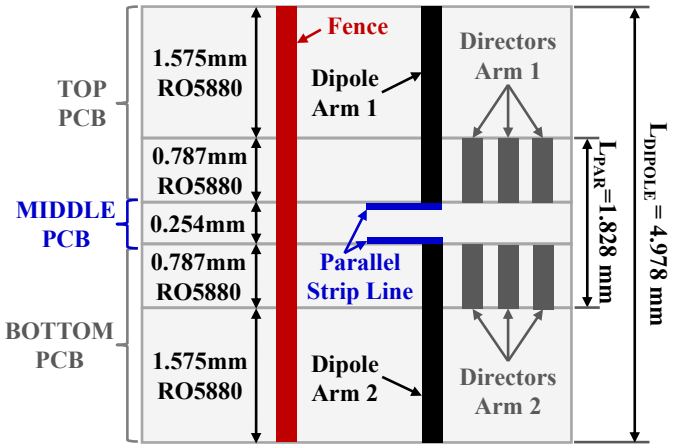
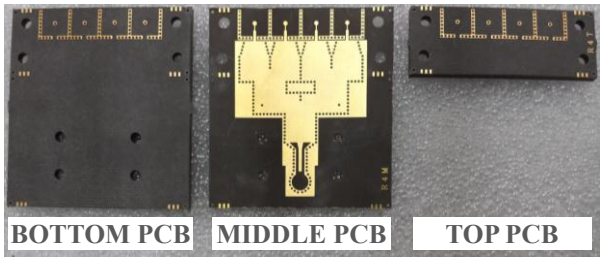
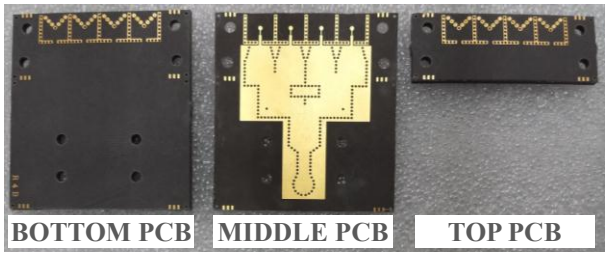


Fig. 5.24. The 5-layer substrate stack-up and vias arrangement used for fabricating the proposed dipole prototypes.



(a)



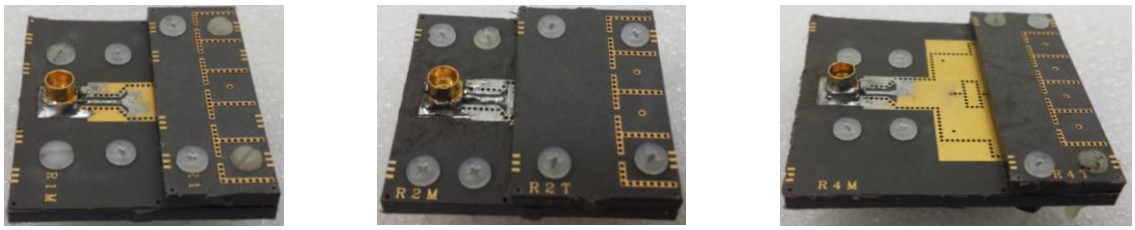
(b)

Fig. 5.25. The BOTTOM/MIDDLE/TOP separate PCBs for the 4-element electric dipole array. (a) Upper PCB side. (b) Lower PCB side.

In addition to the single element dipole structure, two and four element arrays were designed. The arrays geometries are shown in Fig. 5.23 where 2×1 and 4×1 SIW dividers were utilized for the two-element and four-element arrays, respectively employing Y- and T- SIW junctions [239], [240].

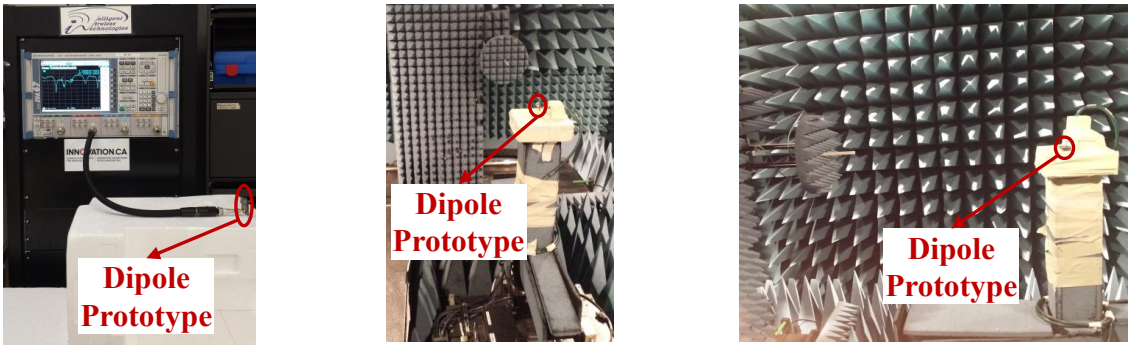
5.4 Measurement Results

This section presents the fabricated prototypes and the simulated/measured results for the single dipole and its array.



(a) (b) (c)

Fig. 5.26. The assembled dipole prototypes. (a) Single element. (b) 2-elements array. (c) 4-elements array.



(a) (b) (c)

Fig. 5.27. Measurement Setup. (a) S-parameters measurements setup. (b) Elevation plane radiation pattern measurement setup inside the near field anechoic chamber. (c) Azimuth plane radiation pattern measurement setup inside the near field anechoic chamber.

5.4.1 The Fabricated Prototypes and Measurement Setup

The proposed electric dipole was fabricated on the Rogers RO5880 substrate. For ease of fabrication, buried vias should be avoided, which implies that the dipole and parasitic vias lengths need to be equal to the commercially available substrate thicknesses. Hence, the thicknesses of the different substrate layers were chosen to meet this constraint without compromising the optimal lengths obtained in Section 5.3. The stack-up employed for the fabricated prototypes in Fig. 5.24 shows the different substrate layer thicknesses and the vias arrangement. Five substrate layers were used. The realized 4.958 mm dipole's length and 1.828 mm parasitic vias' length are close to their optimal values of 5 mm and 1.9 mm, respectively. For simplicity, the electric dipole prototypes were fabricated as 3 separate PCBs and were assembled using Nylon screws.

The TOP and BOTTOM PCBs have the top and bottom dipole and parasitic vias arms, respectively while the MIDDLE PCB contains the dipole feed. Three prototypes were fabricated, namely, the single electric dipole, the 2-elements dipole array, and the 4-elements dipole array. Fig. 5.25 shows the upper and lower sides of the TOP, MIDDLE and BOTTOM PCBs for the 4-

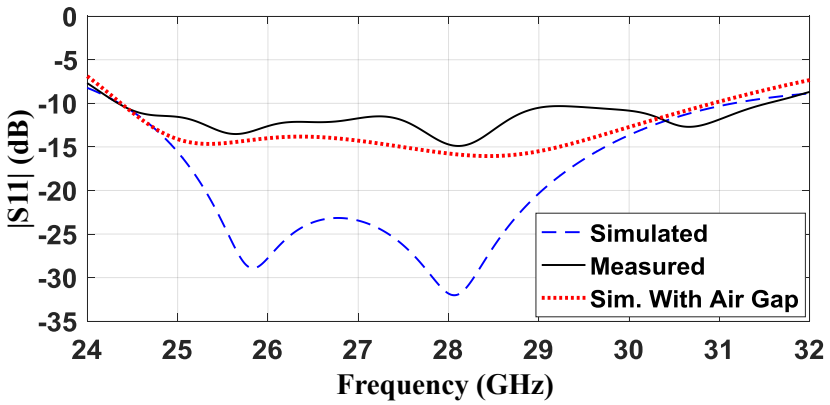


Fig. 5.28. Measured/Simulated S11 plot for the single electric dipole.

elements array while Fig. 5.26 shows the assembled PCBs for the single dipole element, 2-elements array and 4-elements array with overall sizes of 10×24.2×4.9 mm^3, 15×26.47×4.9 mm^3, and 30×35.62×4.9 mm^3, respectively. The prototypes are excited using a 40 GHz SMP connector which needs a GCPW footprint. Hence, for the sake of excitation during measurements, the SIW is interfaced to a GCPW through a GCPW-to-SIW transition which was optimized for 50 Ω matching [195],[196]. The measurement setups for testing the fabricated prototypes are presented in Fig. 5.27. The S-parameters were measured by the ZVA67 Rohde&Shwarz VNA as shown in Fig. 5.27(a) and the radiation patterns were measured inside an NSI 2000 near field anechoic chamber. Two different measurement setups were applied inside the chamber as illustrated in Fig. 5.27(b) and (c) to measure the complete 360º radiation patterns in the elevation and azimuth planes and report the measured HPBW and F/B.

5.4.2 The Single Electric Dipole Measured Results

The proposed single element dipole operates over 26% bandwidth around 28 GHz with stable radiation performance over the operating bandwidth. The S11 plot of the single element dipole is illustrated in Fig. 5.28 showing simulated/measured impedance bandwidth for $|S11| \leq -10$ dB of 6.93/7.23 GHz. It can be noted that the peak measured S11 value is degraded with respect to the simulated one. This is attributed to the presence of an airgap between the assembled PCBs. This postulate is verified by reporting the simulated S11 with 30 µm airgap in Fig. 5.28.

The radiation performance of the proposed 28 GHz electric dipole compared to that of the vertically-polarized 60 GHz magneto-electric dipole presented in [221] is illustrated in Fig. 5.29 where on the x-axis, the frequency is normalized with respect to the antenna's center frequency.

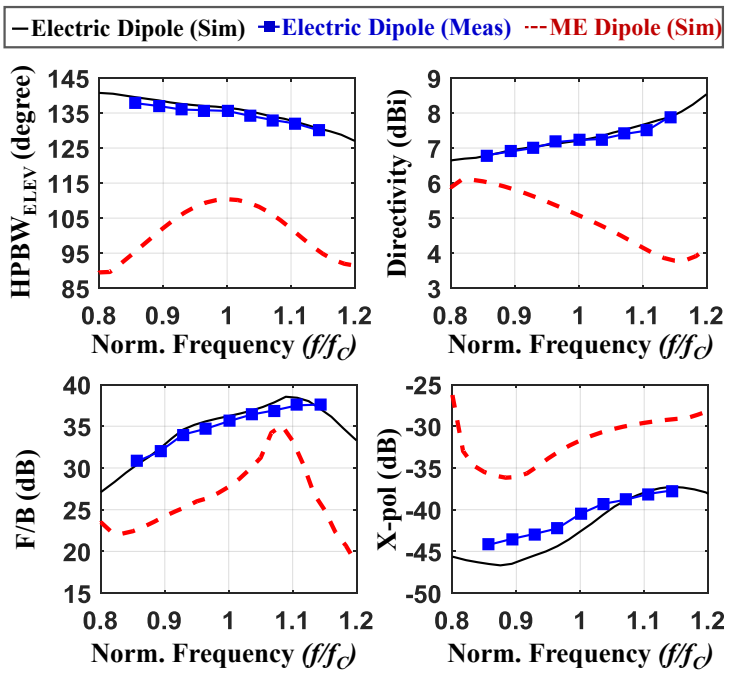


Fig. 5.29. The radiation performance of the proposed electric dipole compared to that of the vertically-polarized ME dipole in [221].

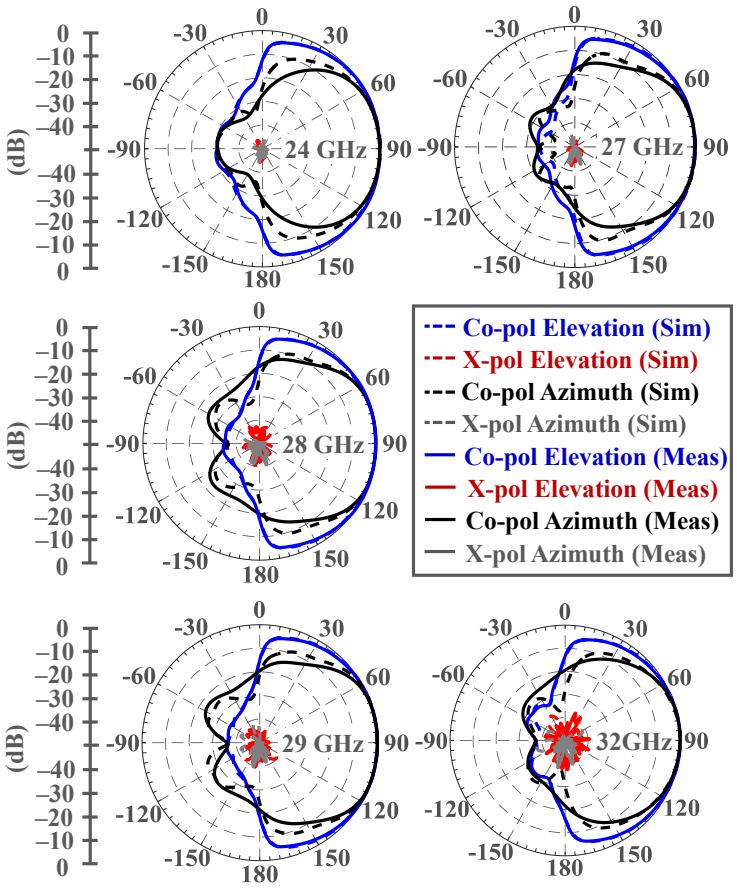


Fig. 5.30. The measured/simulated normalized radiation pattern of the proposed electric dipole.

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The proposed dipole shows superior radiation performance compared to the ME dipole with respect to HPBW, directivity, F/B and X-polarization (the reported X-pol is the worst case cross polarization). This is owing to the following aspects; first, the enhanced gain was attained due to employing the parasitic vias in front of the dipole. Second, the higher HPBW is due to flaring the parasitic vias in V-shaped fashion with each via split into two halves. Finally, the improved F/B was achieved by properly optimizing the via-fence parameters for suppressing the back radiation. The simulated/measured normalized radiation patterns of the proposed electric dipole are illustrated in Fig. 5.30 reported over the bandwidth from 24 GHz to 32 GHz. At 28 GHz the dipole achieves simulated/measured $HPBW_{ELEV}$ of 136.5°/135.6°, $HPBW_{AZ}$ of 78.8°/76.1°, directivity of 7.21/7.22 dBi, F/B of 36.2/35.6 dB and cross-polarization less than -42.6/-40.5 dB. The effective area (without feed) of the proposed electric dipole and that of the ME dipole are $0.96\lambda_d \times 0.94\lambda_d \times 0.67\lambda_d$ and $0.83\lambda_d \times 1.41\lambda_d \times 0.715\lambda_d$, respectively.

5.4.3 The Electric Dipole Array Measured Results

The measured S11 plot for the 2×1 and 4×1 electric dipole arrays are illustrated in Fig. 5.31 achieving simulated/measured impedance bandwidths of 2.5/2.42 GHz and 2.27/2.38 GHz, respectively. The bandwidth of the arrays is limited by the SIW divider. The simulated S11 of the back-to-back 4×1 SIW divider is illustrated in Fig. 5.32 showing a bandwidth of 3.27 GHz. The obtained bandwidth from the array well covers the 28-GHz band specified by the FCC for 5G (27.5 GHz – 28.35 GHz). The SIW divider is only added for the sake of measuring the array performance. Practically, when the array is connected to the RF phase shifter chip for beam scanning as illustrated in Fig. 5.1, the SIW feed will not be needed and the system will be able to operate over the 7.23 GHz bandwidth attained by every single element. From another perspective, in the industry usually the bandwidth of the different elements is designed for $|S11| < -14$ dB to give a sufficient design margin when integrating the different elements together.

The simulated/measured normalized radiation patterns of the arrays in both the elevation and azimuth planes are illustrated in Fig. 5.33. The 2×1 array and 4×1 array achieve measured HPBW in the elevation plane higher than 133º, measured F/B higher than 36 dB and measured cross polarization lower than -39.6 dB. The sidelobe level (SLL) for the 4×1 array is higher than 10.6 dB. Table 5.4 provides a summary of the measured and simulated radiation pattern performances for the fabricated prototypes.

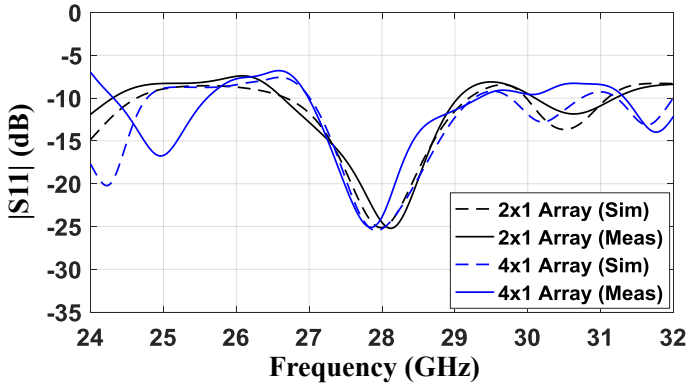

Fig. 5.31. Measured/Simulated S11 plot for the 28 GHz 2×1 and 4×1 dipole arrays.

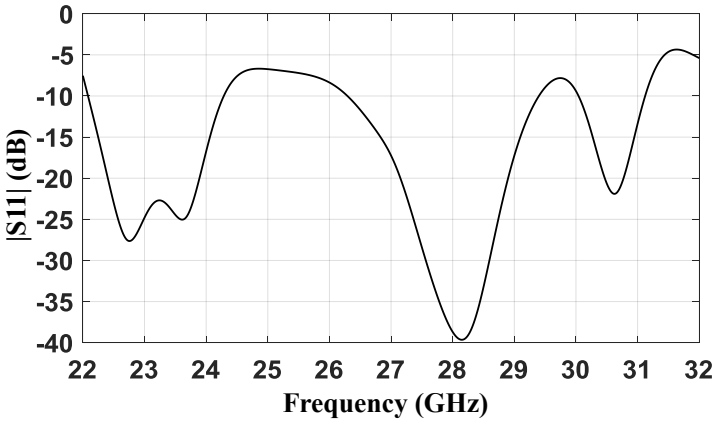

Fig. 5.32. Simulated S11 plot for the back-to-back SIW 4×1 divider.

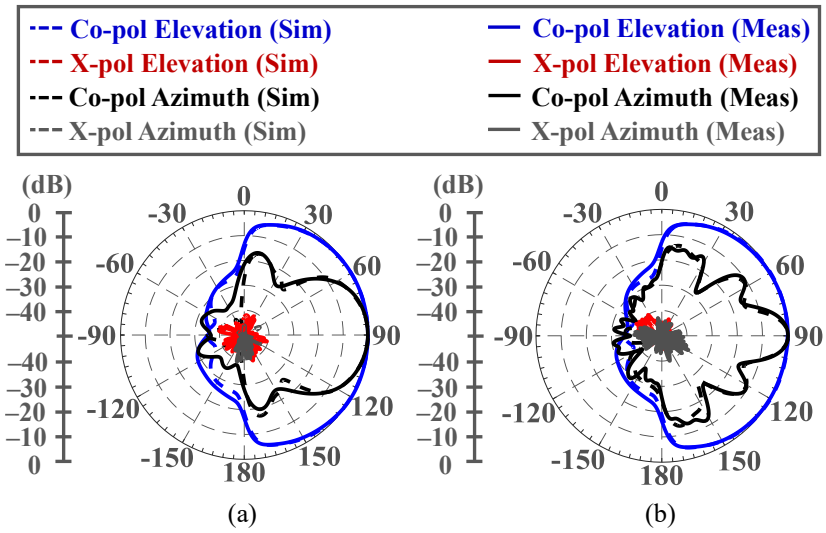

Fig. 5.33. The measured/simulated normalized radiation pattern of the proposed electric dipole arrays. (a) 2×1 Array. (b) 4×1 Array.

Table 5.4
Measured/Simulated Radiation Pattern Performance Parameters

	Single Element		2×1 Array		4×1 Array	
	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
$HPBW_{ELEV}$ (deg.)	136.5	135.6	134.1	134.8	134.3	133.1
F/B (dB)	36.2	35.6	35.1	36	35.3	36.4
X-pol (dB)	-42.6	-40.5	-40.8	-39.6	-43.5	-39.8
$HPBW_{AZ}$ (deg.)	78.8	76.1	39.7	40.3	17	17.3

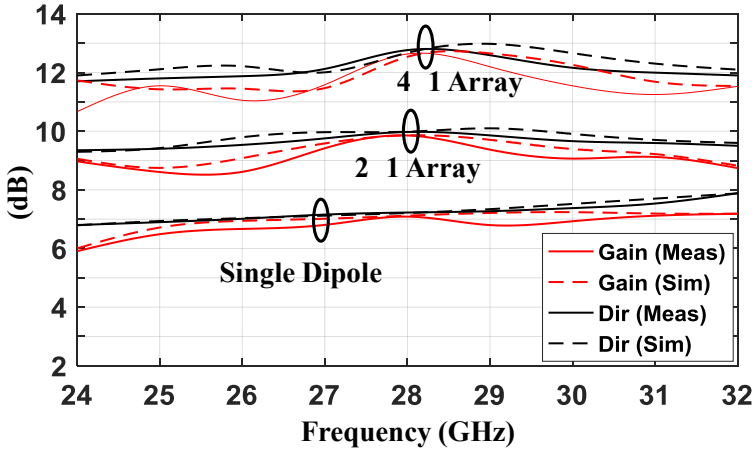

Fig. 5.34. Measured/Simulated Gain and Directivity of the fabricated prototypes

The simulated/measured directivity and gain of the fabricated prototypes are illustrated in Fig. 5.34. The single dipole, 2×1 array, and 4×1 array achieving gains at 28 GHz of 7.13 dBi, 9.83 dBi and 12.61 dBi, respectively. The radiation efficiency of the implemented electric dipole array is 95.8 %. The directivity was measured by the aid of standard horn antenna while the measured realized gain was estimated by combining the measured directivity, the simulated efficiency, and the measured S11.

A comparison of the proposed dipole array with state-of-the-art linearly-polarized antennas for mobile devices operating in the 28 GHz band is presented in Table 5.5. It can be noted that the proposed array achieves the highest HPBW in the elevation plane and the highest F/B. This was accomplished by selecting the optimal design parameters and shape for the dipole, fence, and parasitic vias. In addition to that, the array achieves a high gain of more than 12 dBi with only a 4-elements array and low cross-polarization levels with a compact structure.

5.5 Conclusion

A compact mm-Wave vertically-polarized edge dipole array was proposed for 5G mobile devices. The proposed array achieves high gain, high radiation efficiency, wide matching

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Table 5.5
Comparison With State-of-the-art Linearly Polarized Antennas For Mobile Devices operating in the 28 GHz Band

	[210]	**[218]**	**[219]**	**[220]**	**This Work**
Structure	8×1 SIW Array	16×1 Mesh Grid Array	Dipole Array Substrate Integrated Horn	8×1 Cavity Backed Slot Antenna Array	4×1 Electric Dipole Array
Radiation Pattern Type	Surface Pattern	Edge Pattern	Edge Pattern	Edge Pattern	Edge Pattern
Bandwidth (GHz)	2.3	3	12	2.5	Single Element: 7.23 Array: 2.38
Gain (dBi)	13.9	10.9	9 – 12	Single Element: 6.5 Array: 15	Single Element: 7.13 Array: 12.61
$HPBW_{ELEV}$ (degree.)	79.6	109	60	70	133.1
$HPBW_{AZ}$ (degree)	9.9	12	15	N/A	17.3
F/B (dB)	14	15	10 – 20	10	36.6
X-pol (dB)	< –20	N/A	< –25	N/A	< –39.8
Size*	$12.5\lambda_d \times 3.8\lambda_d \times 0.4\lambda_d$	$8.32\lambda_d \times 1.06\lambda_d \times 0.2\lambda_d$	$4.5\lambda_d \times 6.57\lambda_d \times 0.86\lambda_d$	$7.1\lambda_d \times 0.21\lambda_d \times 0.55\lambda_d$	$3.84\lambda_d \times 0.94\lambda_d \times 0.67\lambda_d$

* Effective area of the antenna without feed.

bandwidth, and low cross-polarization levels while featuring wide fan-beam with high HPBW in the elevation plane together with high F/B making it a suitable candidate for the future 5G transceivers. The optimal designs were evaluated in the single element, 2×1 array and 4×1 array structures and all requirements were fulfilled.

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6. CONCLUSION AND FUTURE WORK

This chapter will conclude the thesis, provide the major contributions presented in the dissertation and introduce possible future work.

6.1 Summary

In this work, three of the main building blocks for the future 5G transceivers were designed and fabricated. Those blocks are the fractional-N frequency synthesizer acting as the local oscillator for the transceiver, the analog-to-digital converter required for the hybrid beamforming and the antenna responsible for transmitting/receiving the signal.

First, the fractional-N frequency synthesizer was presented. Two prototypes were designed and fabricated in the TSMC 65 nm CMOS process; a single stage 28 GHz fractional-N PLL and a 28 GHz fractional-N cascaded PLL. The cascaded PLL implemented using a first stage fractional-N CPPLL followed by a second stage SSPLL improved the state-of-the-art jitter performance and figure-of-merit of mm-Wave frequency synthesizers. Table 6.1 provides a performance summary of the proposed frequency synthesizers.

Second, the analog-to-digital converter designed in the time-domain was discussed. Two prototypes were proposed and designed in the TSMC 65 nm CMOS process; an oversampling ADC and a Nyquist-rate ADC. The oversampling time-based ADC employs a SAR-TDC for enhanced resolution and lower quantization noise level. The Nyquist-rate ADC utilizes a SAR/flash reconfigurable TDC to allow for wide range of reconfigurability over both resolution and sampling rates. Both ADCs employs a 1-bit folded VCO for enhanced linearity. A performance summary of both ADCs is provided in Table 6.2.

Finally, the antenna design was introduced. A mm-Wave vertically-polarized dipole array implemented to fit at the edge of the 5G handset devices was proposed. The dipole is implemented using vias at the edge of a Rogers RO5880 substrate. A via-fence was added surrounding the dipole to reduce the back radiation. The proposed antenna features superior radiation performance compared to state-of-the-art mm-Wave antennas for mobile devices. The performance summary of the implemented dipole antenna is illustrated in Table 6.3.

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Table 6.1
Summary of the proposed fractional-N PLL Performance Implemented in the 65nm CMOS Process

		Single Stage PLL	**Cascaded PLL**
Description		28 GHz CPPLL with fractional division performed using Phase mixing.	Implemented using 2 stages First Stage: 7 GHz fractional-N CPPLL Second Stage: 28 GHz Dividerless SSPLL
Output Clock (GHz)		26.2-32.4	26.2-32.4
Area (mm^2)		0.18	0.28
Power (mW)		35.8	26.9
PN @ 1 MHz (dBc/Hz)	**Integer**	-116.2	-107
	Fractional	-112.6	-103.4
Integrated Jitter (fs)	**Integer**	63.6	364.2
	Fractional	70.4	500
FoM* (dB)	**Integer**	-249.63	-233.23
	Fractional	-248.75	-230.58

Table 6.2
Summary of the proposed Time-based ADC Performance Implemented in the 65nm CMOS Process

	Oversampling Time-Based ADC	**Nyquist-Rate Time-Based ADC**
TDC Type	SAR-TDC	Reconfigurable SAR/Flash TDC
VCO	1-bit Folded VCO	Programmable 1-bit Folded VCO
Area (mm^2)	0.047	0.124
Sampling Rate (MS/s)	675	100 – 5000
Resolution (bits)	12.9	13 – 5
Power (mW)	11.65	8.4 – 22.3
FoM (fJ/conv.)	76	14.6 – 196

Table 6.3
Summary of the Measured Performance of the proposed Dipole Antenna Implemented on a Rogers RO5880 Substrate

	Single Element	**4×1 Array**
Gain (dBi)	7.13	12.61
$HPBW_{ELEV}$ (deg.)	135.6	133.1
F/B (dB)	35.6	36.4
X-pol (dB)	<–40.5	< –39.8
Size (mm^3)	$0.96\lambda_d \times 0.94\lambda_d \times 0.67\lambda_d$	$3.84\lambda_d \times 0.94\lambda_d \times 0.67\lambda_d$

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6.2 Thesis Contribution

This work focused on implementing three building blocks for the future 5G transceivers. For each of those blocks, it was targeted to push the state-of-the-art and provide reliable solutions.

In Chapter 2 and Chapter 3, two fractional-N frequency synthesizer prototypes were implemented. The first is a single stage 28 GHz fractional-N CPPLL that employs a phase interpolator to achieve the fractional division with high resolution. The fabricated prototype achieves good performance with integrated jitter of 500 fs while consuming a total of 35.8 mW. For enhanced jitter performance, the second architecture that is designed as a fractional-N 28 GHz cascaded PLL was investigated. The first stage of the cascaded PLL is a 7 GHz fractional-N CPPLL that employs a high-resolution phase mixer for the fractional division to lower the quantization noise. The second stage is implemented as a divider-less SSPLL. The cascaded PLL provides much better performance compared to the single-stage PLL achieving integrated jitter of 70.4 fs and consumes low power of 26.9 mW. Detailed analysis and design perspectives for the cascaded PLL were provided. Also, the performance improvement of the cascaded PLL over the single-stage PLL in terms of jitter and power consumption is theoretically presented and verified with measured results. The results of the cascaded PLL were compared with the state-of-the-art solutions, and it was shown that the proposed architecture achieves excellent phase noise performance and allows high resolution in phase and frequency control with comparable power consumption suitable to meet the stringent requirements for the upcoming 5G mobile transceivers. The analysis and measurement results for the single stage and cascaded PLLs are summarized in the following publications

- W. El-Halwagy, A. Nag, P. Hisayasu, F. Aryanfar, P. Mousavi and M. Hossain, "A 28-GHz Quadrature Fractional-N Frequency Synthesizer for 5G Transceivers With Less Than 100-fs Jitter Based on Cascaded PLL Architecture," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 396-413, Feb. 2017
- W. El-Halwagy, A. Nag, P. Hisayasu, F. Aryanfar, P. Mousavi and M. Hossain, "A 28GHz quadrature fractional-N synthesizer for 5G mobile communication with less than 100fs jitter in 65nm CMOS," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 118-121.

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Two time-based analog-to-digital converter prototypes were presented in Chapter 4 featuring both the oversampling and Nyquist-rate modes. The time-based architecture was chosen for its digital nature and scalability compared to its voltage-domain counterpart. The oversampling time-based ADC employs a novel high-resolution SAR-TDC for lower quantization noise level and a 1-bit folded VCO for enhanced linearity. The SAR-TDC achieves 1.15 ps time-resolution with INL/DNL of 0.64/0.65 LSB. The folded VCO was able to enhance the VCO linearity from 12% to 0.17%. That allowed the 675 MS/s oversampling ADC to achieve 12.9 bits resolution at 10 MHz while consuming a total of 11.65 mW. Compared to previously reported oversampling time-based ADCs, the proposed ADC achieves better FoM of 76 fJ/conv in 10 MHz bandwidth. In addition to the oversampling time-based ADC, a reconfigurable Nyquist-rate time-based ADC was implemented. The time-domain nature of the ADC allowed for a wide range of reconfigurability and efficient hardware reuse. The reconfigurable ADC employs a SAR/flash reconfigurable TDC that can efficiently switch between SAR and flash modes. Also, programmability was added to the 1-bit folded VCO to provide the tuning characteristics required by the different sampling rate modes supported by the ADC with high linearity. The Nyquist-rate ADC supports continuous sampling rate variations from 100 MS/s to 5 GS/s providing 13- to 5-bits resolution with exponential power scaling from 8.4 mW to 22.3 mW, respectively while achieving FoM ranging from 14.6 to 196 fJ/conv. Compared to the previously reported reconfigurable ADCs, the proposed structure achieves the widest reconfigurability range over both resolution and bandwidth with superior FoM. The analysis, performance and measured results of both ADC prototypes are summarized in the following publications

- W. El-Halwagy, P. Mousavi, and M. Hossain, “A 100 MS/s to 5 GS/s, 13-Bit to 5-Bit Nyquist-Rate Reconfigurable Time-Domain ADC*”, IEEE Transactions on Very Large Scale Integration, (Under Peer Review).*
- W. El-Halwagy, P. Mousavi, and M. Hossain, "A 79dB SNDR, 10MHz BW, 675MS/s open-loop time-based ADC employing a 1.15ps SAR-TDC," *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Toyama, 2016, pp. 321-324.

Chapter 5 presents the antenna design for 5G handset devices. The proposed antenna array is designed as a vertically-polarized dipole array. The dipole features wide fan-beam with high HPBW in the elevation plane, high gain and high front-to-back radiation ratio (F/B). For

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enhanced gain, parasitic-vias are added in front of the dipole. To improve HPBW without sacrificing gain, V-shaped split parasitic-vias are employed. A via-fence surrounds the dipole structure to suppress back radiation and enhance F/B. The dipole is connected to a parallel-strip line (PS) which is interfaced to the main SIW feed through a novel SIW-to-PS transition. The array prototypes achieve high gain, high F/B, wide HPBW in the elevation plane and low cross polarization. The low-cost, compactness and good performance of the proposed array make it a competing candidate for the future 5G handset devices. The design, performance and measured results of the proposed dipole are summarized in the following publications

- W. El-Halwagy, R. Mirzavand, J. Melzer, M. Hossain and P. Mousavi, "Investigation of Wideband Substrate-Integrated Vertically-Polarized Electric Dipole Antenna and Arrays for mm-Wave 5G Mobile Devices," in *IEEE Access*, vol. 6, pp. 2145-2157, 2018.
- W. El-Halwagy, J. Melzer, M. Hossain and P. Mousavi, “A 28 GHz Compact Vertically-Polarized Dipole for 5G Smartphone Edge”,2017 *IEEE International Symposium on Antennas and Propagation (APSURSI)*, San Diego, 2017, pp. 2573-2574.

6.3 Future Work

Recently, the research activity in the topics related to the future mm-Wave 5G wireless has massively increased. This greatly encouraged more researchers to navigate more into this new standard. Following that perspective, the work presented in this dissertation can be extended to explore more ideas for the upcoming 5G wireless transceivers. Some of those ideas are presented in this section as follows.

A. The mm-Wave Frequency Synthesizer

On the frequency synthesizer side, a digital implementation can be investigated to get rid of the large area of the loop filter as in [243] where a mixed-mode phase accumulator and a hybrid phase detector that features double edge sampling were employed for enhanced jitter performance. Also, the proposed SAR-TDC can be employed as a phase-detector in all-digital PLL implementations like in [244].

B. The Analog-to-digital Conversion

For the hybrid beamforming architecture, a high-performance low-power ADC is required. For the work presented in Chapter 4, it can be concluded that the time-domain architectures are very

promising especially with the continuous technology scaling. The SAR-TDC can be further explored at higher speed technology nodes like the 28 nm process to make better use of Moore's law [245] where improved TDC resolution with lower power consumption can be achieved. For the overall ADC, the VCO can be replaced with a pulse width modulator. Moreover, background digital calibration can be employed instead of the foreground digital calibration.

C. The mm-Wave Antenna Design

Also, for the mm-Wave 5G antenna design more ideas can be explored where higher gain is required to mitigate the large path loss at such frequencies. Metamaterials can be utilized for gain enhancement, more specifically the epsilon-near-zero (ENZ) materials which have low permittivity compared to that of the free space. Such materials have the potential of providing enhanced directivity [246]. Metamaterials are artificial dielectrics whose electromagnetic properties are governed by their shape/geometry and the placed periodic or amorphous inclusions [247]. Such inclusions can be vias placed within the dielectric. And given that the proposed antenna structure in Chapter 5 is based on vias placed in the dielectric, it can make good use of the metamaterials for improved gain. Several interesting metamaterial designs were reported in the literature. In [248], a team from the University of California San Diego proposed a rectangular ENZ volume whose upper and lower faces are covered with a perfect electric conductor (PEC) with a monopole placed in the middle of the bottom of the PEC. The ENZ block is surrounded by a flared-shaped non-ENZ material. In [249], a dipole antenna loaded with a C-shaped metamaterial is proposed achieving 4 GHz bandwidth and gain higher than 10 dBi where the utilization of the metamaterials resulted in 5 dBi gain enhancement. Also, reconfigurability can be added to the proposed structure to allow for beam scanning. In addition, the effect of changing the fence shape on the dipole radiation performance can be investigated [250].

D. The Overall 5G Transceiver Design

With respect to the overall 5G transceiver design, the proposed separate blocks can be integrated with mixers and LNAs to constitute the complete 5G transceiver like in [251], [252] and test its overall performance.

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