Engineering Considerations for the Design of High Performance Zinc Oxide Thin Film Transistors

by

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Abstract

The thin film transistor (TFT) is a field-effect device that is critical to the function of many large-area electronics including flat panel display (FPD) technologies. However, continued improvements in transistor speed, stability, and performance are crucial for future innovation and progress. Zinc oxide (ZnO) TFTs are garnering significant interest recently due to their unique combination of high optical transparency, moderately high electron mobility, good stability, and compatibility with low temperature processing. If a low temperature processed, high performance ZnO TFT is demonstrated, it can open the way to new applications that are inaccessible for current TFT technologies e.g. flexible and paper electronics.

Typically, to enhance TFT performance, improvements in the intrinsic electronic properties of the device materials are needed. However, in this research, the device architecture's role on TFT performance is investigated in detail. To that end, a bottom-gated ZnO source-gated thin film transistor (SGTFT) that utilizes a gate-controlled Schottky source injection barrier with a ZnO active channel deposited by pulsed laser deposition (PLD) is presented. The ZnO SGTFT exhibits unique capacitance-voltage ($C-V$) and transconductance (g_m)-gate-source voltage (V_{GS}) characteristics that give important insight into its device physics. Based on these measurements, it is expected that the SGTFT can offer a new approach to engineering an enhancement-mode ZnO TFT by limiting the device's off-state current (I_{off}) with a source Schottky barrier. Building on these results, a top-gated, drain-offset ZnO SGTFT fabricated entirely using low temperature atomic layer deposition (ALD) is demonstrated. Besides being

more compatible with real-world circuit applications, these ZnO SGTFTs exhibit promising device performance featuring a positive threshold voltage (V_{th}), low subthreshold swing (SS) of 192 mV/decade, high breakdown voltages exceeding 20 V, and a saturation mobility (μ_{sat}) of 3.9 $cm^2V^{-1}s^{-1}$. Furthermore, the device can be easily adapted for flexible electronics applications due to its low processing temperatures ($< 130°C$). Consequently, the SGTFT device architecture could be an effective means to achieve a high performance ZnO TFT.

To better discern the source-and-drain (S/D) contacts' influence on TFT performance, identical top-gate staggered ALD ZnO TFTs employing symmetrical gold (Au), titanium tungsten (TiW), and ruthenium (Ru) bottom electrodes are studied with emphasis on analysing the metal/ZnO interface. The ZnO TFT's characteristics are highly influenced by the metallization scheme at the S/D. After correlating the properties of the metal/ZnO interface with TFT electrical measurements, it is found that Au contacts uniquely induce a highly n-doped ZnO film that makes the TFT unable to turn off and the drive current difficult to saturate. On the other hand, TiW contacts form Schottky barriers with the ZnO, restricting carrier injection into the channel, which then reduces the TFT's on-state current and mobility. The Ru ZnO TFTs exhibit the best overall performance highlighted by extremely low SS values of ~ 89 V/decade, a positive V_{th}, a high current on-to-off ratio ($I_{on/off}$) of $> 10^7$, and a moderately high μ_{sat} of ~ 1.4 $cm^2V^{-1}s^{-1}$. Their excellent TFT characteristics are attributed to an ohmic metal/ZnO junction with limited adsorbed dopants at the metal-ZnO interlayer.

Accurate compact models of ZnO TFTs are necessary for implementation into established and emerging applications. In the final section of this research, ZnO TFTs with varying S/D metallization schemes and device layouts are mod-

elled using a gradual channel approximation (GCA)-based direct current (DC) model that considers a gate-enhanced mobility, S/D contact resistance, and a non-constant saturation current (I_{sat}). Compared to a top-gate, staggered TFT with symmetrical bottom Ru S/D electrodes, the on-state performance dramatically increases after changing the drain electrode to Au from Ru due to Au's lower resistivity and doping effect. When a copper (Cu) Schottky contact is employed for the source, the lower mobility and drive currents indicative of the source-gated effect emerge. Likewise, after removing the gate-to-drain overlap, the drive current and mobility also decrease because of parasitic losses at the channel edge (opposite to the drain). If the gate-to-drain distance (L_{GD}) is increased, space-charge limited current (SCLC) is observed, and the on-state TFT performance further decreases. Thus, a range of TFT characteristics is measured from exploiting only the S/D contacts and drain-side geometry. All these different behaviours are effectively modelled with parasitic elements at the S/D connected in series with an ideal TFT. According to these results, the ZnO TFT's characteristics can be individually tailored with precise engineering of the device architecture and S/D contact materials.

Preface

This thesis is an original work by Alex Ma. Chapter 2 of this thesis has been published as A. M. Ma, M. Gupta, F. R. Chowdhury, M. Shen, K. Bothe, K. Shankar, Y. Tsui, and D. W. Barlage. "Zinc oxide thin film transistors with Schottky source barriers," *Solid-State Electronics*, vol. 76 (2012), pp. 104-108. The work presented in Chapter 3 is an extended discussion of A. M. Ma, M. Gupta, A. Afshar, G. Shoute,Y. Y. Tsui, K. C. Cadien, D. W. Barlage. "Schottky Barrier Source-Gated ZnO Thin Film Transistors by Low Temperature Atomic Layer Deposition," *Applied Physics Letters*, vol. 103, no. 25 (2013), p. 253503. Additionally, the device of interest in that chapter has also been patented in D. Barlage, A. Ma, M. Gupta, K. Bothe, K. Cadien, A. Afshar. "Buried Source Schottky Barrier Thin Film Transistor and Method of Manufacture" (2013). Chapter 4 contains work that has been previously published in A. M. Ma, M. Shen, A. Afshar, Y. Y. Tsui, K. C. Cadien, D. W. Barlage. "Interfacial Contact Effects in Top Gated Zinc Oxide Thin Film Transistors Grown by Atomic Layer Deposition," *IEEE Transactions on Electron Devices*, vol. 63, no. 9 (2016), pp. 3540-3546. For the above mentioned publications, I was the main contributor to device fabrication, data collection, data analysis, and manuscript composition. My supervisor, Professor D. W. Barlage, also assisted with the data analysis, manuscript composition, and was responsible for the overall research direction. Professor K. C. Cadien and his research group (Dr. A. Afshar and Dr. T. Muneshwar) were responsible for the thin film growth by atomic layer deposition, and Professor Y. Y. Tsui and his research group (Dr. M. Gupta, F. Chowdhury, and Dr. M. Shen) helped with the thin film deposition by pulsed laser deposition. My research colleagues (Dr. K. Bothe, G. Shoute, M. Benlamri, and Dr. M. Shen) assisted with device fabrication, data collection, and analysis.

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Without the support from Professor Kenneth C. Cadien, Professor Ying Y. Tsui, and their respective research groups, I would not have been able to conduct this research. My sincere thanks goes to Dr. Amir Afshar and Dr. Triratna Muneshwar for their expertise and support. They were always ready to fulfil my (sometimes) demanding deposition requirements, and I am extremely grateful for that. I would also like to sincerely thank Professor Karthik Shankar, Dr. Manisha Gupta, Arash Mohammadpour, and Fatema Chowdhury for assisting and mentoring me during my first research experience at the University of Alberta.

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Contents

List of Figures

List of Tables

List of Abbreviations

BE	binding energy.
$C-V$	capacitance-voltage.
C_{GD}	gate-to-drain capacitance.
C_{GS}	gate-to-source capacitance.
$I-V$	current-voltage.
I_{DS}	drain-source current.
I_{off}	off-state current.
$I_{on/off}$	current on-to-off ratio.
I_{on}	on-state drain current.
I_{sat}	saturation current.
KE	kinetic energy.
L	channel length.
L_{GD}	gate-to-drain distance.
L_{SD}	source-to-drain spacing.
L_{SG}	source-to-gate overlap.
L_{ov}	overlap between the gate-and-S/D electrodes.
N_D	n-type doping concentration.
R_H	Hall coefficient.
R_q	root mean squared roughness.
R_CW	contact resistance.
R_{on}	on-resistance.
SS	subthreshold swing.
V_H	Hall voltage.
V_{BD}	breakdown voltage.
$V_{DS,sat}$	saturation voltage.

V_{DS}	drain-source voltage.
V_{GD}	gate-drain voltage.
V_{GS}	gate-source voltage.
V_{on}	turn-on voltage.
V_{th}	threshold voltage.
W	channel width.
W/L	channel width-to-length ratio.
W_{dep}	depletion width.
Φ_B	Schottky barrier height.
μ	mobility.
μ_H	Hall mobility.
μ_{FE}	field-effect mobility.
μ_{eff}	effective mobility.
μ_{sat}	saturation mobility.
g_m	transconductance.
g_{ds}	output conductance.
n	ideality factor.
r_{ch}	W-normalized channel resistance per unit length.
2-D	two-dimensional.
3-D	three-dimensional.
a-Si	amorphous silicon.
AFM	atomic force microscopy.
Ag	silver.
Al	aluminium.
Al_2O_3	aluminium oxide.
ALD	atomic layer deposition.
AMOLED	active-matrix organic light emitting diode.
Au	gold.
CLM	channel length modulation.
CMOS	complementary metal-oxide-semiconductor.

Cu	copper.
CVD	chemical vapour deposition.
DC	direct current.
DCTL	direct-coupled tranisistor logic.
DEZn	diethylzinc.
DI	de-ionized.
DOS	density of states.
E/D-mode	enhancement- and depletion-mode.
$FeCl_3$	ferric chloride.
FPD	flat panel display.
GaN	gallium nitride.
GCA	gradual channel approximation.
GIXRD	grazing incidence X-ray diffraction.
HfO_2	hafnium oxide.
IGZO	indium-gallium-zinc-oxide.
ITO	indium-tin-oxide.
KrF	krypton fluoride.
LED	light emitting diode.
LT	low-temperature.
MBE	molecular beam epitaxy.
MOCVD	metal-organic chemical vapour deposition.
MOSCAP	metal-oxide-semiconductor capacitor.
MOSFET	metal-oxide-semiconductor field effect transistor.

MTR	multiple trapping-and-release.
OFET	organic field effect transistor.
OSC	organic semiconductor.
Pd	palladium.
PEALD	plasma enhanced atomic layer deposition.
PECVD	plasma-enhanced chemical vapour deposition.
PEN	polyethylene naphthalate.
PET	polyethylene terephthalate.
PLD	pulsed laser deposition.
poly-Si	polysilicon.
Pt	platinum.
PVD	physical vapour deposition.
rf	radio frequency.
rms	root mean squared.
ROP	remote oxygen plasma.
RT	room-temperature.
Ru	ruthenium.
S/D	source-and-drain.
SB-FET	Schottky barrier field effect transistor.
SCLC	space-charge limited current.
SCS	Semiconductor Characterization System.
SGT	source-gated transistor.
SGTFT	source-gated thin film transistor.
Si	silicon.
SiN	silicon nitride.
SiO_2	silicon oxide.
SPM	scanning probe microscopy.
TCAD	technology computer-aided design.

TDMAH	tetrakis(dimethylamino)hafnium.
TDT	tail distributed trap.
TE	thermionic emission.
TFE	thermionic field emission.
TFT	thin film transistor.
Ti	titanium.
TiW	titanium tungsten.
TLM	transfer length method.
TMA	trimethylaluminum.
TU	tunnelling.
VRH	variable range hopping.
WO_3	tungsten(VI) oxide.
XPS	X-ray photoelectron spectroscopy.
XRD	X-ray diffraction.
ZnO	zinc oxide.
ZrO_2	zirconium oxide.

Chapter 1

Introduction

Semiconductor technology has progressed significantly since the first transistor was invented at Bell Labs in 1947. In today's societies that are highly integrated with electronics, finding methods to improve transistor speed, stability, and performance are crucial for future innovation and progress. Currently, the electronics industry is dominated by silicon-based transistors. Improvements in transistor performance have been traditionally achieved by scaling down their size through Moore's Law. However, for certain applications, compound metal oxide semiconductor materials are being investigated as a legitimate replacement for silicon to achieve improvements in transistor mobility and stability. In particular, thin film transistors (TFTs) based on wide band-gap metal oxide semiconductor films, such as zinc oxide (ZnO), are especially promising for large area electronics applications like flat panel displays (FPDs) and transparent electronics. The FPD industry is a billion dollar market that is projected to increase dramatically in the near future with the advent of emerging transparent electronics technologies [1]. Hence, if a high performance ZnO-based TFT is achieved, it can have a significant impact on next-generation FPD applications as well as unlock new markets that are presently inaccessible by current technologies.

ZnO, a wide band-gap, II-VI binary metal oxide semiconductor, has garnered considerable attention lately due to its unique electrical and optical properties that are attractive for many important optoelectronics, electronics, acoustics, and sensing applications. For instance, there is a large effort in utilizing ZnO for solar cells [2], phosphors [3], light emitting diodes (LEDs) [4], lasers [5], and TFTs [6, 7,

1]. Some of ZnO's most appealing properties include its large band-gap (3.4 eV), transparency and good stability in visible light, non-toxicity, good compatibility with low temperature processes, high exciton binding energy (60 meV), which is especially advantageous for laser applications, and its ability to form nanostructures (e.g. nanowires). For TFTs, employing ZnO as the active channel layer offers many potential advantages compared to the commonly used hydrogenated amorphous silicon (a-Si) including higher electron mobilities (leading to higher drive currents and faster switching) and better stability in the presence of visible light (due to its high band-gap). Furthermore, ZnO thin films can be deposited using physical vapour deposition (PVD) techniques such as pulsed laser deposition (PLD) and radio frequency (rf) magnetron sputtering, in addition to low-cost, large-area deposition techniques such as sol-gel, spray pyrolysis, and atomic layer deposition (ALD). The relative ease of growing ZnO thin films makes ZnO TFTs encouraging for low-cost transparent electronics. ZnO TFTs have demonstrated good electrical performance and are highly promising for next-generation FPD applications. For example, Bayraktaroglu *et al.* have reported mobility values as high as 100 $cm^2V^{-1}s^{-1}$ for ZnO TFTs grown by PLD, which is comparable to low temperature polysilicon TFTs [8]. However, before ZnO TFTs establish themselves as a viable candidate for real-world industrial applications, there are some issues that need resolving. For instance, achieving lower processing temperatures, higher device mobilities, and reducing their naturally high residual electron concentrations are required for ZnO TFTs to compete with some of the new TFT technologies that are also becoming popular e.g. organic and indium-gallium-zinc-oxide (IGZO) TFTs. As-grown ZnO thin films are customarily structurally polycrystalline, which is also problematic for TFT uniformity and stability [1]. Consequently, this research is focused on the design and fabrication of a high performance, low temperature ZnO TFT that can be easily integrated. From studying prototype ZnO TFTs of varying device architectures and materials, a roadmap on how to improve device performance by choosing appropriate design, material, and process parameters are described.

1.1 Properties of Zinc Oxide (ZnO)

In ambient conditions, the stable crystal structure of zinc oxide is the wurtzite structure, which consists of alternating planes of O^{2-} and Zn^{2+} ions as shown by Fig. 1.1. The wurtzite structure lacks inversion symmetry in the plane perpendicular to the c-axis due to the tetrahedral coordination of ZnO [9]. Therefore, wurtzite ZnO possesses piezoelectric properties wherein electric charge is produced from mechanical stress. ZnO can also exist in the zinc blende and rocksalt configurations [10]. The surface of wurtzite ZnO commonly terminates with four distinct faces: two polar, c-axis oriented faces, either polar Zn terminated (0001) or polar O terminated $(000\bar{1})$, and two non-polar faces, $(11\bar{2}0)$ and $(10\bar{1}0)$ [11]. Each face is known to produce different chemical and physical properties that can affect etching, growth, defects, etc.

Some of the main physical and electrical properties of wurtzite ZnO are shown in Table 1.1. Intrinsic ZnO naturally exhibits n-type doping strongly believed to be caused by inherent point defects (e.g. oxygen and zinc vacancies) [12, 10, 13]. Hence, p-type ZnO is notoriously difficult to grow consistently and reliably. This doping asymmetry is presently the major hurdle for ZnO bipolar devices such as LEDs. Fortunately, for the TFT structure, p-doped regions are not required, which is different from metal-oxide-semiconductor field effect transistors (MOSFETs).

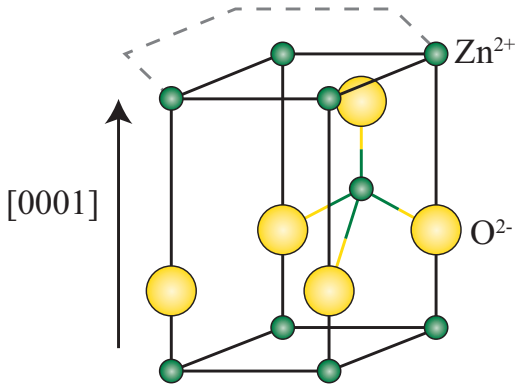

Figure 1.1: The wurtzite crystal structure of ZnO

Table 1.1: Physical and Electrical Properties of Wurtzite ZnO (from [14])

Property	Value
Lattice parameters at 300 K	$a_0 = 0.32495$ nm
	$c_0 = 0.52069$ nm
Density	5.606 g cm^{-3}
Melting point	1975°C
Thermal conductivity	0.6, 1 - 1.2 W cm^{-1} K^{-1}
Linear expansion coefficient	$a_0 = 6.5 \times 10^{-6}\ {}^{\circ}C^{-1}$
	$c_0 = 3.0 \times 10^{-6}\ {}^{\circ}C^{-1}$
Static dielectric constant	8.656
Refractive index	2.008, 2.029
Energy gap (direct)	3.4 eV
Intrinsic carrier concentration	$< 10^6$ cm^{-3}
Exciton binding energy	60 meV
Electron effective mass	0.24
Electron Hall mobility at 300 K (for low n-type conductivity)	200 cm^{2}V^{-1}s^{-1}
Hole effective mass	0.59
Hole Hall mobility at 300 K (for low p-type conductivity)	5 - 50 cm^{2}V^{-1}s^{-1}

1.2 Experimental Procedures

The following sections outline the procedures and techniques utilized to prepare and characterize ZnO TFTs. There are many different techniques that can be used to grow ZnO thin films. PVD techniques such as rf magnetron sputtering [15, 16] and PLD [8, 17, 18, 19] have been used to grow high quality ZnO thin films. Additionally, other prevalent ZnO growth techniques include metal-organic chemical vapour deposition (MOCVD) [20, 21], molecular beam epitaxy (MBE) [22], ALD [23, 24], and solution-based growth techniques such as sol-gel spin-coating [25, 26] and spray pyrolysis [27]. Each technique has its own advantages and disadvantages. For instance, PVD-grown films have demonstrated higher film quality, but they usually require high temperature annealing steps. Whereas, although solution- and ALD-grown films possess good qualities for large-area, low cost electronic applications, they typically show poorer electrical properties.

In this research, several materials characterization techniques were used to study the properties of the ZnO thin films. The thin films' crystal structure can be identified visually, e.g. using microscopic techniques such as atomic force microscopy (AFM), and characterized by grazing incidence X-ray diffraction (XRD). Whereas, thin film chemistry can be investigated in detail with X-ray photoelectron spectroscopy (XPS). The Hall effect was employed to measure the film's carrier type, density, and mobility when applicable.

1.2.1 Pulsed Laser Deposition (PLD)

Pulsed laser deposition (PLD) is a common technique for depositing complex materials (including oxides, nitrides, or carbides) in thin-film research [28]. It is a fast and reproducible oxide thin film growth technique with relatively precise thickness control. Typically, PLD is done in a vacuum system similar to sputter deposition and MBE [29]. In PLD, a pulsed laser is directed towards a target composed of the material to be deposited. If the energy density of the laser pulse is high enough, a small chunk of the target is ablated to form a highly directional plasma plume. The ejected material then accumulates on a substrate forming the thin film. One of the main advantages of PLD is the stoichiometry transfer between the target and substrate from the strong heating at the target surface

due to the laser, which is difficult to achieve using evaporation or sputtering; this allows alloyed targets to be used [28]. Another benefit of PLD is that the particles ejected from the the target are usually highly energetic, leading to better film quality.

When using PLD to deposit ZnO thin films, the properties of the ZnO thin film (e.g. mobility, doping concentration, crystallinity) can be controlled quite well by manipulating the major growth parameters (e.g. laser energy density/fluence, oxygen pressure, and substrate temperature) as well as the post-growth annealing conditions [30, 10, 31, 32, 33]. During ZnO growth, the deposition chamber is filled with oxygen to form a reactive gas atmosphere. For this work, a custom PLD set-up, similar to the one described in Ref. [34], was utilized to grow ZnO thin films for TFT applications. A schematic diagram of the PLD set-up is shown in Fig. 1.2.

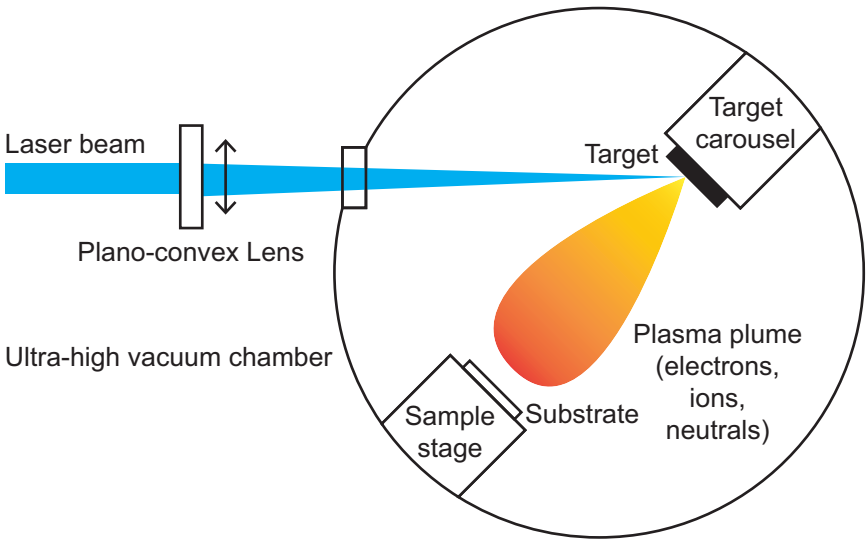

Figure 1.2: Top-view schematic diagram of the PLD set-up.

1.2.2 Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) is a chemical gas-phase thin film deposition technique that employs alternating self-limiting surface reactions. In ALD, precursor gas sources are pulsed into a reaction chamber alternately and, therefore, never

interact with each other, which is different from other chemical vapour deposition (CVD) techniques. Typically, each growth cycle consists of exposing the substrate to each precursor gas followed by a reaction chamber purge [35]. This process is then repeated for the duration of the deposition. During each cycle, the precursor species chemisorb or surface react completely (due to the separate dosing of the precursor gases); consequently, the thickness increase for each deposition cycle is constant [36]. A simple schematic of the ALD process is shown in Fig. 1.3. The cyclic manner of ALD means that film thickness depends only on the number of cycles being used (allowing for precise film thickness control). The films deposited using this technique also show excellent conformality and uniformity over large areas like other CVD processes. Another notable advantage of ALD is its low temperature processes ($< 200°C$) making ALD compatible for deposition on inexpensive plastic or paper substrates.

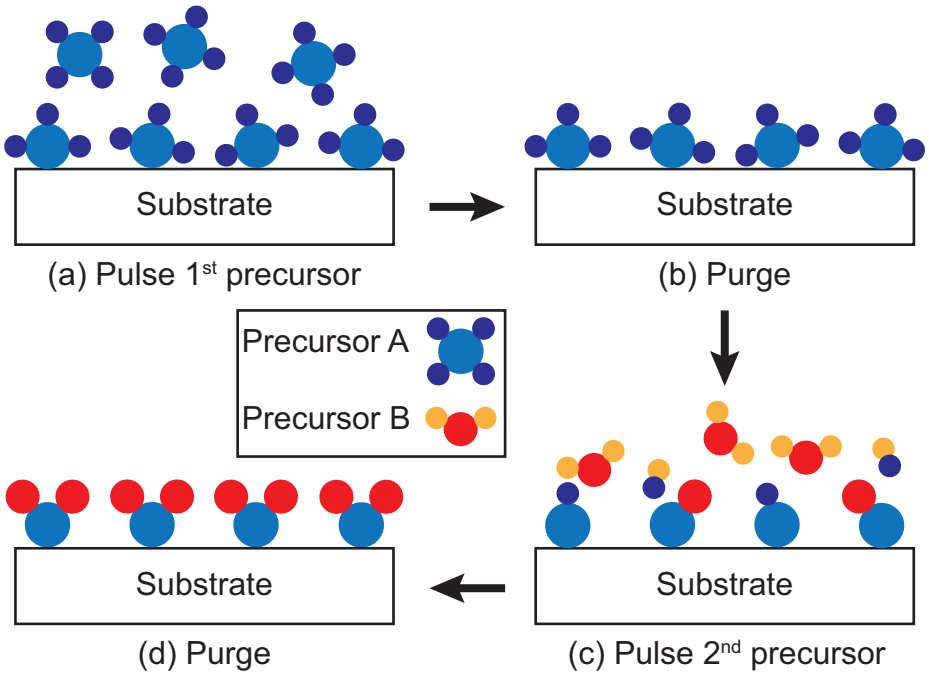

Figure 1.3: Schematic diagram of the ALD process.

1.2.3 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a form of scanning probe microscopy (SPM) that utilizes a probe to image a material's surface at extremely high resolutions. A schematic of a typical AFM set-up is presented in Fig. 1.4. Information from the specimen's surface is gathered by the cantilever probe, which is equipped with a very sharp tip at the end. As the tip approaches the sample surface, close-range atomic forces, e.g. van der Waals and electrical forces, between the tip and sample cause deflections in the cantilever beam. Hence, as the surface morphology changes, so too do the atomic forces acting on the probe leading to measurable displacements in the free end of the cantilever. By accurately measuring these minute beam deflections, e.g. with a laser deflection system, as the probe is raster scanned over the sample, a three-dimensional topography image with excellent horizontal and vertical resolutions can be produced. Prototype AFM systems have demonstrated a lateral and vertical resolution of 3 nm and < 0.1 nm respectively [37].

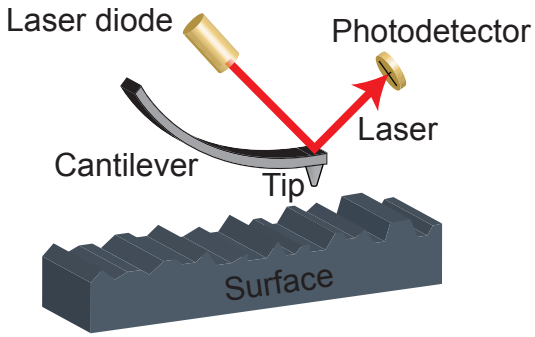

Figure 1.4: Schematic diagram of AFM using beam deflection detection.

In this research, AFM images of various thin films were acquired using the JPK Nanowizard II and Bruker Dimension Edge instruments via tapping mode. AFM operation is usually separated into three different operating modes depending on the tip's nature: contact mode, non-contact mode, and tapping mode. In tapping mode, the cantilever is oscillated near its resonance frequency, usually by a piezoelectric element. During each oscillation cycle, the tip strikes against the surface and then immediately detaches by using a large oscillation amplitude

(typically from 20 to 100 nm) to overcome the stickiness of the surface, which is an issue for non-contact mode AFM [38]. By monitoring the oscillation amplitude, which is affected by the sample's surface topography, a three-dimensional (3-D) topographic image can be generated.

1.2.4 Grazing Incidence X-ray Diffraction (GIXRD)

X-ray diffraction (XRD) is a phenomenon that occurs when a beam of X-rays upon irradiation on a crystal is reflected by the atomic planes of the crystal only at certain angles of incidence. As illustrated in Fig. 1.5(a), when a monochromatic X-ray beam is fired towards a crystal lattice, the atoms in the lattice interact and scatter the X-rays producing a diffracted X-ray beam from constructive interference. Constructive interference can only occur when conditions satisfy Bragg's Law (shown in Equation 1.1 [39]), which relates the incident angle of the reflected beam (θ) with the lattice spacing of the crystalline sample (d) and the wavelength of the beam (λ) (the remaining parameter, n, is any integer).

$$n\lambda = 2d\sin\theta \tag{1.1}$$

By measuring the diffracted beam's θ and applying Bragg's Law, the spacing between atoms in the crystal, crystal structure and orientation, and average crystallite size can all be determined. Consequently, XRD is a powerful tool for characterizing the crystal structure of unknown materials.

For thin film characterization, the large incident angles typically utilized for conventional XRD are inadequate due to the weak signals from the thin film being overpowered by the larger signal from the substrate. Thus, grazing incidence (also known as glancing angle) XRD (GIXRD) with a small, fixed glancing incidence angle close to the critical angle for total external reflection (α_i) of the film material is used instead. When performing GIXRD on a two-dimensional (2-D) sample, X-rays are weakly scattered only by the top few monolayers of atoms on the sample's surface [40]. A simple schematic of GIXRD is depicted in Fig. 1.5(b). In this geometry, the incidence wavevector (k_i) is fixed at a small angle α_i to the surface and the reflected wavevector (k_f) is measured by the detector. During sweeping, α_i is held constant while the angle between k_i and k_f (2θ) is

varied [e.g. by rotating the sample around the surface normal (n) or moving the detector]. For GIXRD, the crystal planes being observed are not parallel to the surface but are instead at an incline. In this research, GIXRD measurements were performed using the Rigaku Ultima IV In-plane system with copper K-alpha radiation (wavelength = 0.15405 nm) and an α_i of 0.5 degrees.

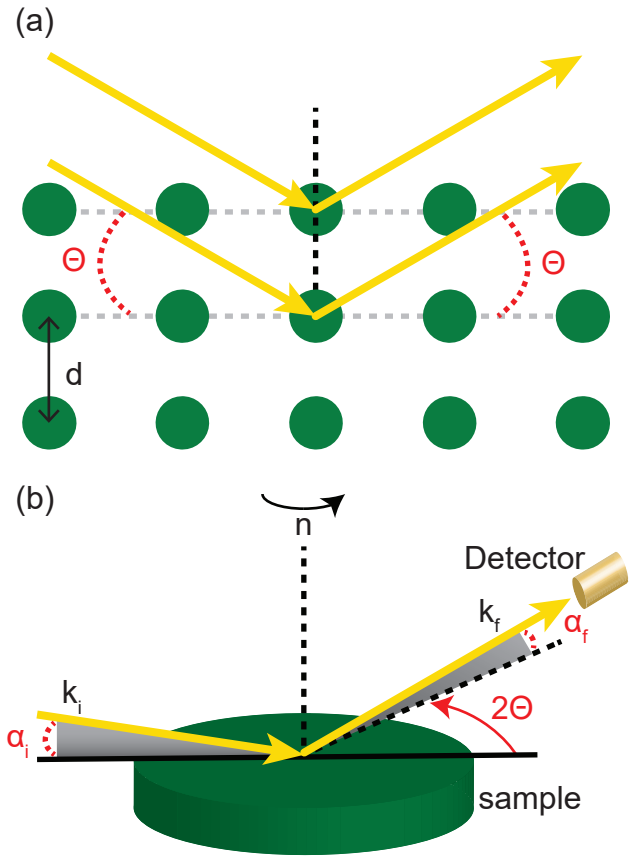

Figure 1.5: (a) Schematic diagram of conventional XRD. The reflected X-ray beam (pointing right) is the result of X-ray wave interference due to scattering of the incoming X-ray beam from the atoms in the crystal lattice. (b) Geometry for GIXRD. The incident angle, α_i, is fixed close to the sample's critical reflection angle while the angle between the incident and diffracted beam, 2θ, is varied.

1.2.5 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a quantitative technique for analysing the surface chemistry of a material. A XPS spectra is obtained by irradiating a material with a monochromatic X-ray beam while measuring the energy of the emitted electrons due to the photoelectric effect with a spectrometer; i.e. if the energy of the X-rays ($h\nu$) is greater than the electron binding energy (BE) of the surface electrons (which is unique for each elemental state), those electrons will be emitted with a kinetic energy (KE) equal to the energy difference after accounting for the spectrometer's work function (ϕ_s), as shown in Equation 1.2 [41].

$$KE = h\nu - BE - \phi_s \tag{1.2}$$

Photoelectrons are only emitted within a maximum of approximately 5 nm from the surface therefore limiting XPS as a surface analysis technique. Nonetheless, by discretely recording the intensity of ejected electrons over a range of KEs using a spectrometer, a photoelectron spectrum (wherein the count rate of photoelectrons detected is plotted against BE) can be generated. Each different element within the sample volume has its own unique set of BEs that is related to its allowed electronic transitions; hence, the measured XPS spectra is made up of characteristic peaks that occur only at select BEs. By analysing the BEs and intensities of the characteristic peaks, the elemental composition, chemical state, and quantity of a detected element can all be determined. A photoelectron's BE is also sensitive to the oxidation state and local chemical environment of the element. E.g. shifts in the BE can arise from differences in the chemical potential and polarizability of compounds [41].

In this research, XPS measurements were performed using an Kratos Analytical AXIS Ultra imaging spectrometer featuring monochromatic aluminium K-alpha radiation (wavelength = 0.83386 nm) running at a power of 210 W. The samples were measured without argon sputter etching the surface prior to data collection. Before analysis, the XPS data was calibrated to the carbon 1s core level (at 284.8 eV) using CasaXPS software.

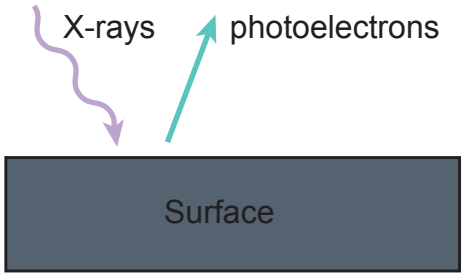

Figure 1.6: Schematic diagram of XPS. Photoelectrons are ejected from the sample upon irradiation from a monochromatic X-ray beam with kinetic energies characteristic of the sample surface's elemental make-up

1.2.6 Hall Effect Measurement

The Hall effect describes the phenomenon wherein a charge particle in a conductor experiences a force, denoted as the Lorentz force, that causes its pathway to curve when a magnetic field is applied perpendicular to the current flow [42]. Consider a bar-shaped n-type semiconductor with conventional current (I_x) flowing in the $+x$-direction as shown by the schematic in Fig. 1.7(a). When a magnetic field (B_z) is applied in the $+z$-direction, the resulting Lorentz force deflects electrons off their normal path, and they collect on the semiconductor's $(-y)$-most face. If holes are present, they also gather at the semiconductor's $(-y)$-most face since they flow in the opposite direction to electrons. This accumulation of charge carriers causes a potential drop known as the Hall voltage (V_H) that opposes further charge migration. I.e. the induced electric field (E_y) increases until it becomes equal to the Lorentz force creating an equilibrium state [43],

$$E_y = B_z v_x = \frac{B_z I_x}{qnwt} \tag{1.3}$$

where v_x is the current's drift velocity, q is the elementary charge, n is the charge carrier density, and wt is the semiconductor's cross-sectional area. The Hall voltage induced by the electric field is calculated by,

$$V_H = -\int_w^0 E_y dy = \frac{B_z I_x}{qnt} \tag{1.4}$$

The Hall coefficient (R_H) is defined by,

$$R_H = \frac{tV_H}{I_x B_z} = \frac{-1}{qn} \tag{1.5}$$

Equation 1.5 applies for the case of a n-doped semiconductor; for a p-type semiconductor R_H is opposite in sign. The Hall mobility (μ_H) is defined by,

$$\mu_H = \frac{R_H}{\rho} = R_H \sigma \tag{1.6}$$

where ρ and σ are the semiconductor's resistivity and conductivity respectively. Typically, the sample's ρ is measured in the Hall instrument by utilizing a four-terminal van der Pauw configuration [43]. The van der Pauw measurement allows the average ρ and R_H to be measured for any flat sample of arbitrary shape as long as the contacts are sufficiently small and the sample is uniformly thick [43]. A common configuration used for van der Pauw measurements is the cloverleaf structure presented below in Fig. 1.7(b). Basically, to make a measurement, a current is made to flow along one edge of the sample between two probes (e.g. I_{12}) while the voltage across the remaining two probes (e.g. V_{34}) is measured. This then allows the resistance along one direction (e.g. $R_{12,34} = \frac{V_{34}}{I_{12}}$) to be calculated by Ohm's law. After repeating the same process to calculate the resistance for the other perpendicular direction (e.g. $R_{23,41}$), the sample's resistivity can be determined by Van der Pauw's formula [44],

$$1 = e^{\frac{-\pi t R_{12,34}}{\rho}} + e^{\frac{-\pi t R_{23,41}}{\rho}} \tag{1.7}$$

In this thesis, Hall effect measurements were carried out using the Nanometrics HL55000 instrument to characterize resistivity, carrier concentration, and mobility of semiconductor films.

1.3 Thin Film Transistors (TFTs)

The traditional metal-oxide-semiconductor field effect transistor (MOSFET) employs highly doped source-and-drain (S/D) regions with an insulated gate (see Fig. 1.8 for a simple schematic). It is the most significant device used for integrated

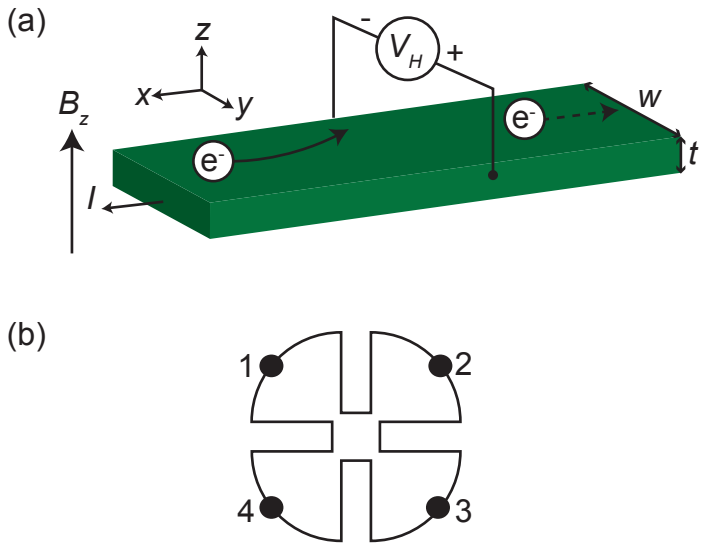

Figure 1.7: (a) Schematic diagram of the Hall effect. Electrons in the n-type semiconductor follow the curved arrow due to the Lorentz force induced by the perpendicular magnetic field. After enough electrons accumulate on the semiconductor's $(-y)$-most face for the Lorentz force to be cancelled by the opposing electric field, the remaining electrons follow the straight pathway indicated by the dashed arrow. (b) Cloverleaf van der Pauw configuration.

circuits and memory and is also becoming more relevant for power electronics [45]. The conventional MOSFET is fabricated from a single crystal silicon (Si) wafer and improvements in performance are achieved through miniaturizing the device and correspondingly increasing circuit density. However, for applications that require large-areas or flexible substrates, single crystalline Si transistors are not feasible and too expensive [45]. For these large area electronics applications, e.g. flat panel displays (FPDs), the thin film transistor (TFT) is better suited. In the TFT structure, the active semiconductor is deposited as a thin film on a substrate. In principal, the substrate can be any insulated material such as plastics, glass, or insulated Si wafers. Currently, the most widely used active semiconductor materials for TFT manufacturing processes are hydrogenated amorphous silicon (a-Si) and polysilicon (poly-Si) [46]. However, a-Si TFTs are limited by their low mobilities (< 1 cm^{2}V^{-1}s^{-1}) and performance degradation under visible light; whereas, poly-Si TFTs are limited by their high processing temperatures and high non-uniformity. Metal oxide semiconductor TFTs can potentially achieve high device performance while offering the advantages of low-temperature (LT) processing, potentially even at room-temperature (RT), and optical transparency. Amorphous oxide semiconductors based on alloyed zinc oxide (ZnO) thin films such as indium-gallium-zinc-oxide (IGZO) have already demonstrated comparable performance to LT poly-Si, and thus they are the leading candidate material for next-generation active-matrix organic light emitting diode (AMOLED) displays [47, 48]. Its amorphous structure gives IGZO better electronic properties than polycrystalline ZnO, but IGZO is not as cost effective (due to the indium) and can be more difficult to process. A general comparison of ZnO with the major TFT technologies is shown in Table 1.2.

1.3.1 TFT Structure and Operation

Schematics of the most popular TFT configurations are shown in Figure 1.9 [46]. The two main classifications are whether the device is staggered or coplanar and whether it is bottom-gated or top-gated. In all configurations, carriers are injected into the channel at the source electrode and extracted out of the channel by the drain electrode. The gate electrode is separated from the channel by a gate

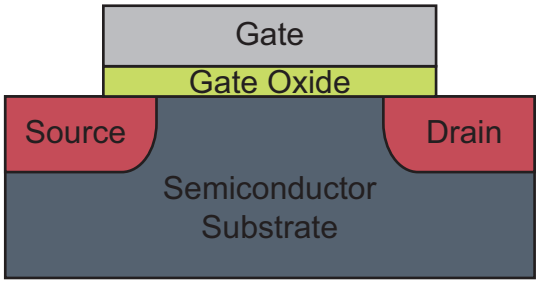

Figure 1.8: Schematic diagram of a conventional MOSFET.

Table 1.2: Comparison Between the Relevant TFT Technologies (From Ref. [1, 48, 49])

TFT properties	ZnO	IGZO	a-Si	LT poly-Si	Organic Semiconductors
Carrier mobility ($cm^2V^{-1}s^{-1}$)	$0.1-30$	$1-100$	<1	$50-100$	$0.1-10$
Manufacturing cost	Low	Low	Low	High	Low
Long term TFT reliability	High (forecast)	High (forecast)	Low	High	Low (in air)
Yield	High	High	High	Medium	High
Process temperature (°C)	RT -500	RT -350	250	<500	RT

dielectric film, and, when a bias is applied to it, is responsible for modulating the charge density in the channel. Because the TFT utilizes a semiconductor thin film as the active channel layer, the TFT's transport process differs from the MOSFET, which uses a single-crystalline bulk semiconductor. In the TFT, carrier transport occurs due to the accumulation of majority carriers at the active channel layer/gate dielectric interface in response to the gate-to-channel electric field; whereas, in a MOSFET, current transport occurs due to minority carriers in an inversion layer [50]. An illustration of the ideal energy band diagrams in a TFT from the perspective of the gate for different gate biasing conditions are shown in Fig. 1.10. For an n-channel TFT, when a negative gate-source voltage (V_{GS}) is applied, mobile carriers are repelled from the channel leading to lower channel conductance. If there is limited current flow, the TFT is considered to be in its "off" state. On the other hand, when a positive V_{GS} is applied, mobile carriers are attracted to the channel, and a thin, high carrier density accumulation layer is formed at the semiconductor/insulator interface [50]. In this operating regime, there is high channel conductance and the TFT is in its "on" state.

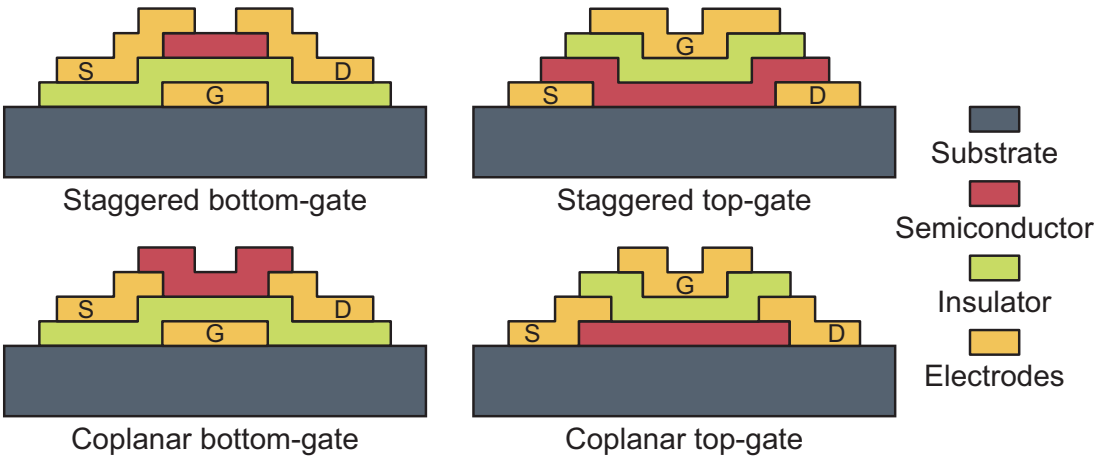

Figure 1.9: Schematics of the conventional TFT configurations.

Despite the differences in their operating mechanism, the modulation of the TFT's source-to-drain channel conductance, and consequently drain-source current (I_{DS}), follows a similar dependency on the applied gate and drain voltage (V_{GS} and V_{DS}) analogous to the conventional MOSFET. As in the MOSFET, the

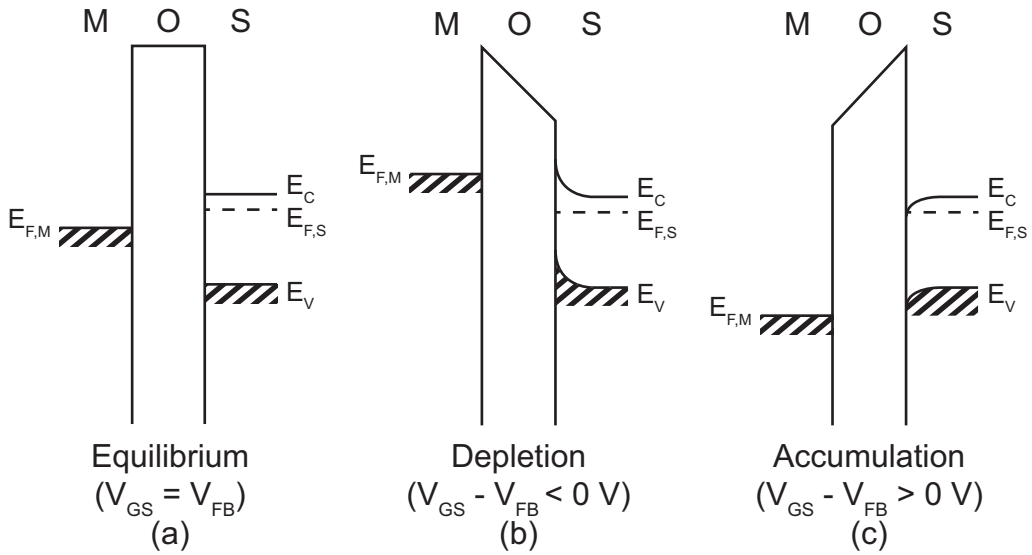

Figure 1.10: Energy band diagrams of the gate MOS stack in a TFT for various biasing conditions: (a) equilibrium ($V_{GS} = V_{FB}$), (b) depletion ($V_{GS} < V_{FB}$), and (c) accumulation ($V_{GS} > V_{FB}$). V_{FB} is the flatband voltage, which is the built-in voltage of the MOS stack. For TFTs, it is assumed that V_{FB} is much lower than the threshold voltage (V_{th}), hence making it negligible [51].

TFT basically operates in two regimes: the linear regime (for small V_{DS}) and the saturation regime (for large V_{DS}). By using the gradual channel approximation (GCA), which assumes that the channel's lateral field is much smaller than its vertical field, one can use the generic square model for I_{DS} in ideal conditions to evaluate TFT performance [46, 52],

$$I_{DS} = \begin{cases} 0 & V_{GS} \leq V_{th} \\ \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] & V_{DS} \leq V_{GS} - V_{th} \\ \frac{W}{2L}\mu C_{ox}\left[V_{GS} - V_{th}\right]^2 & V_{DS} > V_{GS} - V_{th} \end{cases} \tag{1.8}$$

where W, L, μ, C_{ox}, and V_{th} are the channel width, channel length, gate dielectric capacitance per unit area, channel mobility, and threshold voltage respectively. An illustration of a typical output characteristics (I_{DS} versus V_{DS}) showing the two different regimes given in Equation 1.8 is presented in Fig. 1.11. Note that Equation 1.8 in its simplest form does not account for transistor non-idealities such as finite source-and-drain (S/D) resistance, channel length modulation (CLM), short channel effects, etc. To account for these more complicated phenomena, a more elaborate model is needed.

From the ideal TFT model (Equation 1.8), several key TFT figure of merits can be derived to quantitatively evaluate the TFT performance. The key performance metric used to quantify how efficient electrons move through the channel is the channel mobility (μ). Unlike the Hall mobility, which is used to describe a material's bulk mobility, the TFT channel mobility is influenced by scattering at interfaces (particularly the channel/insulator interface) [43]. There are three variations of channel mobilities typically reported for TFT assessment, all of which are derived from manipulating the ideal TFT equation (Equation 1.8): effective mobility (μ_{eff}), field-effect mobility (μ_{FE}), and saturation mobility (μ_{sat}) [43].

μ_{eff} and μ_{FE} are derived from Equation 1.8 in the linear regime ($V_{DS} << V_{GS} - V_{th}$); whereas μ_{sat} is derived from Equation 1.8 in the saturation regime ($V_{DS} > V_{GS} - V_{th}$). By making the appropriate approximations for long channel

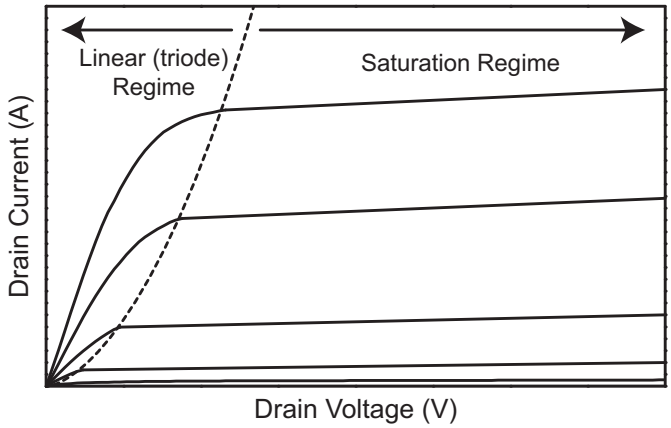

Figure 1.11: Typical output characteristics of an arbitrary n-channel TFT. The dashed line separates the two regimes according to the ideal TFT model (Equation 1.8).

TFTs at low V_{DS}, μ_{eff} can be determined by the following equation [43],

$$\mu_{eff} = \frac{g_d}{\frac{W}{L}Q_n} \tag{1.9}$$

where $g_d = \frac{\partial I_{DS}}{\partial V_{DS}}$ is the drain conductance in the linear regime and $Q_n \cong C_{ox}(V_{GS} - V_{th})$ is the cumulative mobile charge per unit area induced in the channel by the gate. Similarly, the equations for μ_{FE} and μ_{sat} are as follows [43]:

$$\mu_{FE} = \frac{g_m}{\frac{W}{L}C_{ins}V_{DS}} \tag{1.10}$$

$$\mu_{sat} = \frac{(\frac{\partial\sqrt{I_{DS,sat}}}{\partial V_{GS}})^2}{\frac{W}{2L}C_{ins}} \tag{1.11}$$

where $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ is the transconductance.

Of the three commonly used mobilities, μ_{eff} is the least ambiguous as it is calculated in the device's linear regime of operation where the channel thickness and electric field profile is the most uniform (hence, the GCA is the most valid), and it accounts for $\frac{\partial\mu}{\partial V_{GS}}$ [43, 53]. However, μ_{eff} is dependent on Q_n, which is

difficult to measure precisely for ZnO TFTs [54]. Although easier to calculate, both μ_{FE} and μ_{sat} do not account for $\frac{\partial \mu}{\partial V_{GS}}$, which is untrue for ZnO TFTs (i.e. at large V_{GS}, the accumulation channel thickness decreases resulting in more intense scattering at the interface) [6, 53]. Additionally, μ_{sat} is taken at high V_{DS} where the fields are the most non-uniform, which could make the GCA invalid [43, 53]. However, unlike μ_{eff} and μ_{FE}, μ_{sat} is rather insensitive to the S/D contact resistance. Consequently, all three types of mobility have their own benefits and drawbacks.

Traditionally, V_{th} is the parameter employed for quantifying the V_{GS} where the transistor begins to turn "on". From this concept, the definitions of an enhancement-mode (or normally-off) and depletion-mode (or normally-on) device are established. For an enhancement-mode TFT, the TFT is "off" at zero gate bias; whereas for a depletion-mode TFT, a non-zero negative gate bias is necessary to turn the TFT "off". Therefore, for most real-world applications, enhancement-mode devices are preferred as they are easier to implement in circuits and have reduced power consumption. In the conventional MOSFET, V_{th} is equal to the voltage at the onset of strong inversion in the channel [45]. However, V_{th} is ambiguous when applied to TFTs because TFTs operate in accumulation; i.e. it is confusing whether V_{th} is simply a model parameter in Equation 1.8 or the actual voltage where the TFT turns on [54]. Nonetheless, V_{th} is the predominant parameter used to evaluate a TFT's turn-on characteristics. Besides the mobility and turn-on characteristics, other important parameters used to characterize TFTs include S/D contact resistance, subthreshold swing (SS), current on-to-off ratio ($I_{on/off}$), which is the ratio of the TFT's maximum-to-minimum drain current, dynamic response, and reliability [6].

1.3.2 ZnO TFTs

There has been a recent surge in interest in ZnO-based TFTs principally for its potential for high mobility and high visual transparency devices especially for flat panel displays (FPDs). A higher mobility device leads to higher drive currents as well as faster switching; consequently, the applications of TFTs increase tremendously with improvements in their performance. Currently, ZnO TFTs reported

in literature have demonstrated varied characteristics. A table summarizing the device performances of notable ZnO TFTs is presented in Table 1.3. It is important to note that the quantitative data reported in Table 1.3 are not directly comparable due to possible differences in the parameter extraction, bias conditions, processing conditions, materials, and device structure. Nonetheless, based on the literature reported thus far, it is possible to assess the general status and future direction of ZnO TFT research. Usually, to improve the TFT performance, the growth parameters of the device materials are tailored to attain better electrical characteristics (e.g. changing the substrate temperature, employing surface treatments, and introducing extrinsic dopants). Another approach, however, is to modify the device architecture to achieve certain device characteristics. In this research, both methods are exploited to realize a high performance, low-cost

TFT suitable for low temperature processes.

Table 1.3: Results from Notable ZnO TFTs

Technique	T ($^{\circ}C$)	μ ($cm^2/V\,s$)	I_{on}/I_{off}	V_{th} (V)	Ref.
rf sputtering	RT	20*	2×10^5	21	[15]
ion beam	600 - 800	0.3 - 2.5	10^7	10 - 20	[55]
rf sputtering	∼RT	1 - 2	10^6	∼0	[56]
PLD	450	0.031 - 0.97	10^6	-1 to 2.5	[57]
PLD	300	up to 7	10^7	> 0	[58]
rf sputtering	250	17.6	10^6	6	[59]
rf sputtering	350	1.689	10^5	2.5	[16]
rf sputtering	150	5.2	7.2×10^8		[60]
ALD	100	1	10^7	1.7	[61]
ALD	150	1.13	10^6	0.8	[62]
PLD	350	110	10^{12}	< 0	[8]
PLD	400	12.85	10^6	8	[17]
sol-gel	500	5 - 6	$10^5 - 10^6$	18.6	[25]
ALD	90	0.13	10^6	13.1	[63]
PEALD	200	20 - 30	10^9	4.5	[24]
sol-gel	300 - 500	12 - 13	10^5	0.62 to 1.16	[64]
PLD	360	21.7	10^6	-3.9	[65]
ALD	150	11 - 13	10^6	-2.7 to 6.3	[23]
PEALD	225	0.06	10^5	11.6	[66]
thermal ALD	125	0.25	10^6	-16.54	[66]
ALD	110	11.86*	10^7	9.24	[67]
spray pyrolysis	400	32*	10^5	< 0	[27]
PLD	200	14	10^9	1.5	[68]

* Most likely overestimated due to the use of a un-patterned channel layer.

Chapter 2

ZnO Schottky Barrier Source-gated Thin Film Transistors

In this research, a ZnO-based Schottky barrier source-gated thin film transistor (SGTFT), which was originally demonstrated on silicon (Si) by Shannon *et al.* [69, 70], is fabricated and tested for the first time. The crucial distinction between the SGTFT and the conventional TFT is that a Schottky barrier metal contact is employed for the source electrode instead of a traditional ohmic metal contact. This important difference introduces different device physics from the regular TFT and offers many potential benefits.

2.1 Metal-Semiconductor Contact Physics

Whenever a metal comes into contact with a semiconductor, a potential barrier forms at the metal/semiconductor interface [45]. Based on the height of this barrier, the metal/semiconductor junction can be rectifying or non-rectifying. A rectifying contact is referred to as a Schottky contact; whereas a non-rectifying contact is referred to as an ohmic contact. In a Schottky contact, the height of the potential barrier that forms is referred to as the Schottky barrier height (Φ_B). In ideal conditions (i.e. no defects and interface trap states between the metal

and semiconductor), Φ_B is a function of the metal's work function (Φ_M) and the semiconductor's electron affinity (χ_S) according to the relation shown below (for a n-type semiconductor), which is referred to as the Schottky-Mott model [71, 72],

$$\Phi_B^{(n)} = \Phi_M - \chi_S \tag{2.1}$$

An illustration depicting how the Schottky barrier forms between the semiconductor and metal is shown in Fig. 2.1. When a positive bias is applied to the anode of the Schottky barrier, the effective barrier height is reduced [see Fig. 2.1(c)], and vice versa [see Fig. 2.1(d)]. In reality, the Schottky-Mott model rarely applies because of non-idealities including surface effects, defects, image force lowering, lateral barrier inhomogenities, etc. [73]. The Φ_B for ZnO Schottky barriers are especially unpredictable due to the strong influence of external factors such as surface cleaning and impurities.

2.2 Metal Contacts for ZnO

In order to build reliable ZnO devices, high quality, reproducible ohmic and rectifying contacts are needed. A wide range of metallization schemes have been successfully implemented for ohmic contacts on n-type ZnO such as aluminium (Al) [74, 75, 76], titanium (Ti) [77, 78, 79, 80], ruthenium (Ru) [81, 82], and conductive oxides such as indium-tin-oxide (ITO) [82, 83]. The most common ohmic contacts utilized for TFTs have been either Al- or Ti-based. Additional ohmic contacts for ZnO that have been reported in literature are given in Ref. [84] and [85].

Rectifying contacts are usually evaluated by their Φ_B and ideality factor (n). These parameters can be extracted by fitting the Schottky junction's current-voltage ($I-V$) curves to the idealized current transport equation across the metal/semiconductor interface according to thermionic emission (TE) theory [45, 73],

$$J = A \times A^* \times T^2 e^{\frac{-q\Phi_B}{k_B T}} (e^{\frac{qV - JR_S}{nk_B T}} - 1) \tag{2.2}$$

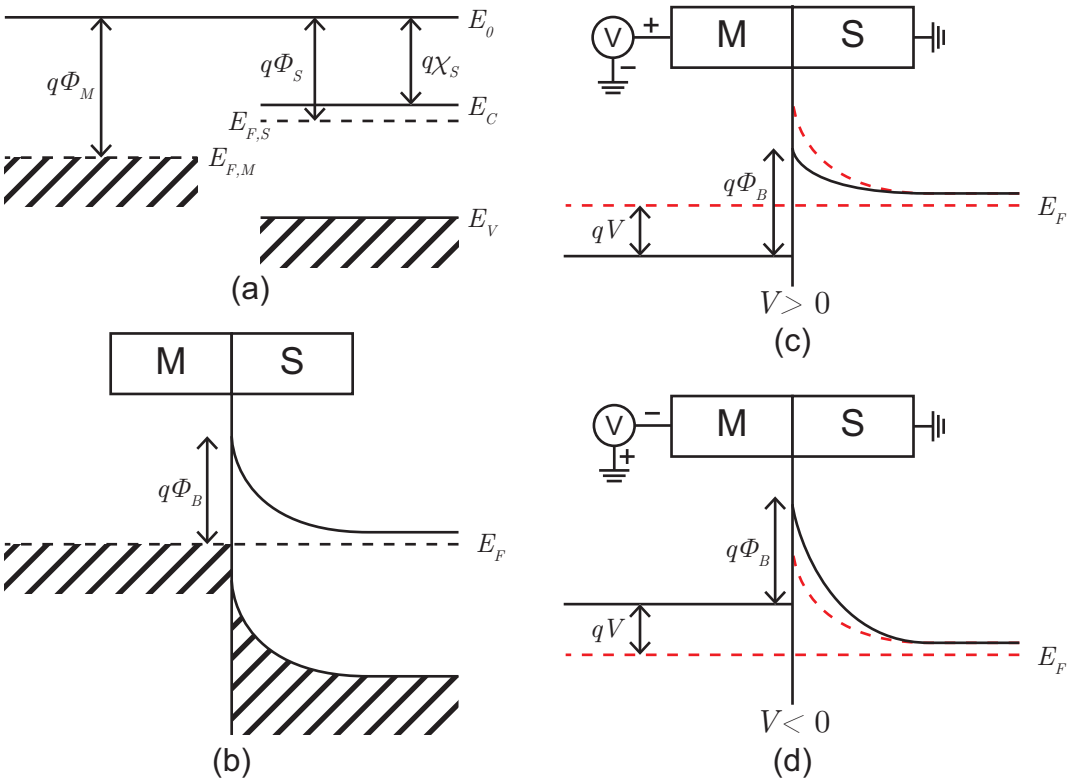

Figure 2.1: Idealized band diagrams (energy vs distance) of (a) a Schottky metal and corresponding n-type semiconductor in vacuum and the Schottky barrier formed at a metal-semiconductor junction under (b) zero bias, (c) applied forward bias ($V > 0$ V), and (d) applied reverse bias ($V < 0$ V).

Table 2.1: Notable Schottky contacts on ZnO (based on Table I. in Ref. [84])

Metal	$q\Phi_B^{(n)}$ (eV)	Ideality Factor	Surface Treatment	Ref.
Ag	0.9	1.3	AG BSC($11\bar{2}0$)	[86]
Ag	0.69 - 0.70	1.6 - 1.8	CC BSC(0001)	[87]
Ag	0.77 - 1.02	1.1 - 1.2	CC BSC($000\bar{1}$)	[88]
Ag	0.95	1.7	PLD @ 620°C	[89]
Au	0.67	1.9	ROP BSC($000\bar{1}$)	[90]
Au	0.65	1.6 - 1.8	CC BSC(0001)	[87]
Au	0.69 - 0.70	1.1	CC BSC($000\bar{1}$)	[88]
Au	1.02	2.0	sputtering @ 300°C	[91]
Au	0.68	2.4	PLD @ 620°C	[89]
Pd	0.59	1.2	CC BSC($000\bar{1}$)	[88]
Pd	0.8	1.5	PLD @ 620°C	[89]
Pt	0.7	1.5	UVOC BSC(0001)	[92]
Pt	0.68	1.2	CC BSC($000\bar{1}$)	[88]
Pt	0.9	2.0	PLD @ 620°C	[89]
IrO_x	0.85	1.1	CC BSC($000\bar{1}$)	[93]
W	0.45	2	UVOC BSC(0001) @ 700°C	[92]
PEDOT:PSS	0.9	1.2	UVOC BSC(0001)	[94]

where J is the current density, A is the area, A^* is the Richardson's constant, T is the temperature, V is the applied voltage, R_S is the series resistance, and n is the ideality factor. The Richardson's constant is a material parameter of the semiconductor and is equal to 32 cm^{-2} K^{-2} for ZnO. TE is not the only mechanism for current flow through a Schottky barrier however. As the semiconductor's doping levels increase, the Schottky barrier's depletion region becomes thinner, and after a certain threshold, carriers can tunnel across the barrier via field emission or thermionic field emission (TFE) processes for instance as shown by Fig. 2.2. Hence, a rectifying contact can be converted to ohmic by locally doping the semiconductor around the electrode so that carriers can easily tunnel through the contact barrier.

The most well-known reports of Schottky metals demonstrated on ZnO (and

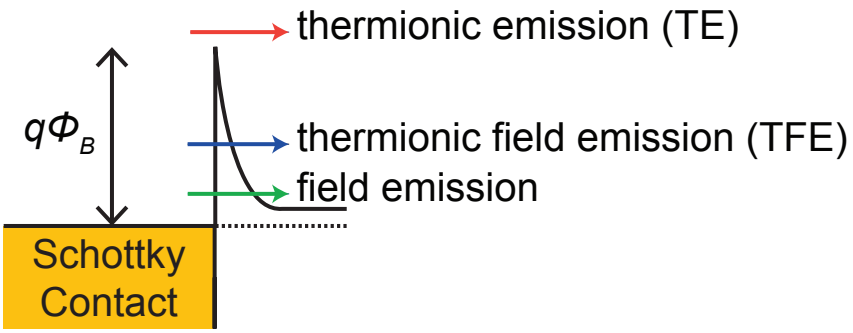

Figure 2.2: Idealized band diagram of a Schottky contact illustrating thermionic emission and tunnelling current transport processes.

their properties) are tabulated in Table 2.1. It is important to note that the studies are generally not comparable due to differences in the ZnO material [e.g. thin film, and bulk single crystal (BSC)], surface preparation [e.g. as-grown (AG), remote oxygen plasma (ROP), UV-ozone cleaned (UVOC), and chemically cleaned (CC)], and measurement technique [e.g. current-voltage ($I-V$) or capacitance-voltage ($C-V$)]. Nonetheless, Table 2.1 gives a good picture of the work done on Schottky contacts for ZnO; A more comprehensive review of ZnO Schottky metals can be found in Ref. [84]. Most of the metals employed as Schottky contacts are noble metals with large work functions such as gold (Au), silver (Ag), platinum (Pt), and palladium (Pd). However, the Schottky junction's properties are very sensitive to the fabrication process and experimental conditions. Even if the same metal is utilized, results are unpredictable and difficult to reproduce. For example, the adsorption of oxygen or hydrogen on the ZnO surface can cause charge transfer, band bending, and diffusion into the Schottky metal [73]. Surface treatments also play a major role for the formation of a high quality Schottky barrier. Most of the work involving ZnO Schottky contacts are formed on bulk single crystal ZnO wafers, which have different material properties from the ZnO thin films utilized for TFTs. Nonetheless, in light of the results presented in literature, well-known Schottky and ohmic metals were employed for the fabrication of a ZnO Schottky barrier source-gated thin film transistor (SGTFT).

2.3 Schottky Barrier Source-gated Thin Film Transistors (SGTFTs)

Transistors are key components for many important technologies; therefore, there is always the need for continuous improvements in transistor performance such as higher switching speeds, lower power consumption, better reliability, higher power handling capability, and reduced production costs. To that end, many different transistor architectures have been tested to achieve better performance or special features. Schottky barrier field effect transistors (SB-FETs), which use Schottky barrier contacts for the source-and-drain (S/D) instead of p-n junctions or ohmic contacts, have been employed for silicon (Si) and gallium nitride (GaN) in the past for their different S/D contact characteristics, easier fabrication procedures, potentially lower temperature processing, and better scalability [95, 96]. In this research, the asymmetrical Schottky barrier S/D structure, which is also referred to as a source-gated transistor (SGT) by Shannon *et al.* [69], is utilized for a ZnO-based source-gated thin film transistor (SGTFT) for the first time. The SGTFT is based off of the SB-FET except that only the source electrode is replaced with a Schottky contact while the drain electrode is kept as an ohmic contact, and the semiconductor is a thin film rather than a bulk substrate. Through these modifications, a potential barrier is introduced at the source, which alters the device operation leading to some unique device characteristics.

2.3.1 Operation of Schottky Barrier SGTFTs

Compared to the conventional TFT, the operation of the Schottky barrier SGTFT is fundamentally different due to the presence of the potential barrier at the source. For instance, the SGTFT's drain current-voltage ($I_{DS} - V_{DS}$) characteristics are noticeably different from the conventional TFT (see Fig. 2.3 for examples of typical output characteristics) [69, 97]. A schematic of a simple SGTFT structure is shown in Fig. 2.3(a). In the SGTFT, current flow in the device is restricted by the Schottky barrier at the source, which leads to several advantages and disadvantages. Particularly, when a positive V_{DS} is applied to the device, carriers in the channel near the source are depleted due to the reverse-

biased source barrier. As V_{DS} is increased further, the depletion region grows larger until it extends all the way to the gate dielectric. At that moment, the current saturates due to pinch-off at the source and can only be increased further by increasing the gate-source voltage (V_{GS}). This is different from the conventional TFT where the current saturates from being pinched-off at the drain end of the channel. Consequently, in the SGTFT, the charge transport is mostly controlled by the electrostatics of the gate-controlled potential barrier at the source rather than by the channel conductance leading to unique output characteristics featuring lower saturation voltages and higher output impedances compared to the regular TFT (even at similar drive currents) [69, 70]. However, because the current is constricted by the source barrier, the drive current and effective device mobility is significantly lowered [97, 98]. Furthermore, it has been demonstrated that the SGTFT is more insensitive to the semiconductor material quality and is better suited for disordered semiconductor films (e.g. films with many defects) because the lower carrier concentration at the source improves the transistor's current control [99]. This makes the SGTFT structure especially attractive for dealing with ZnO thin films' high residual electron concentrations and instabilities from their polycrystalline structure.

2.4 ZnO Schottky Barrier SGTFTs using PLD

The upcoming content is an extended description of the work published in Ref. [19]. In this study, ZnO is utilized with a Schottky barrier SGTFT structure for the first time. The Schottky source barrier concept was analysed by studying bottom-gated SGTFTs with ZnO thin films deposited by pulsed laser deposition (PLD). Fabrication of the ZnO SGTFT was done on a heavily n-doped silicon (Si) substrate insulated with 200 nm thick silicon oxide (SiO_2). The PLD ZnO thin films ($\sim$ 50 nm thick) were grown at room temperature with a vacuum pressure of 5×10^{-5} Torr and an ambient oxygen pressure of 100 mTorr directly on the SiO_2. A krypton fluoride (KrF) laser (248 nm, 15 ns, 20 Hz) was used to ablate a 99.9% pure ZnO target, which was fixed 3 cm away from the substrate. Afterwards, post-growth annealing was performed for 2 hours at 600°C on a hotplate in a regular atmospheric environment. The post-growth anneal makes this

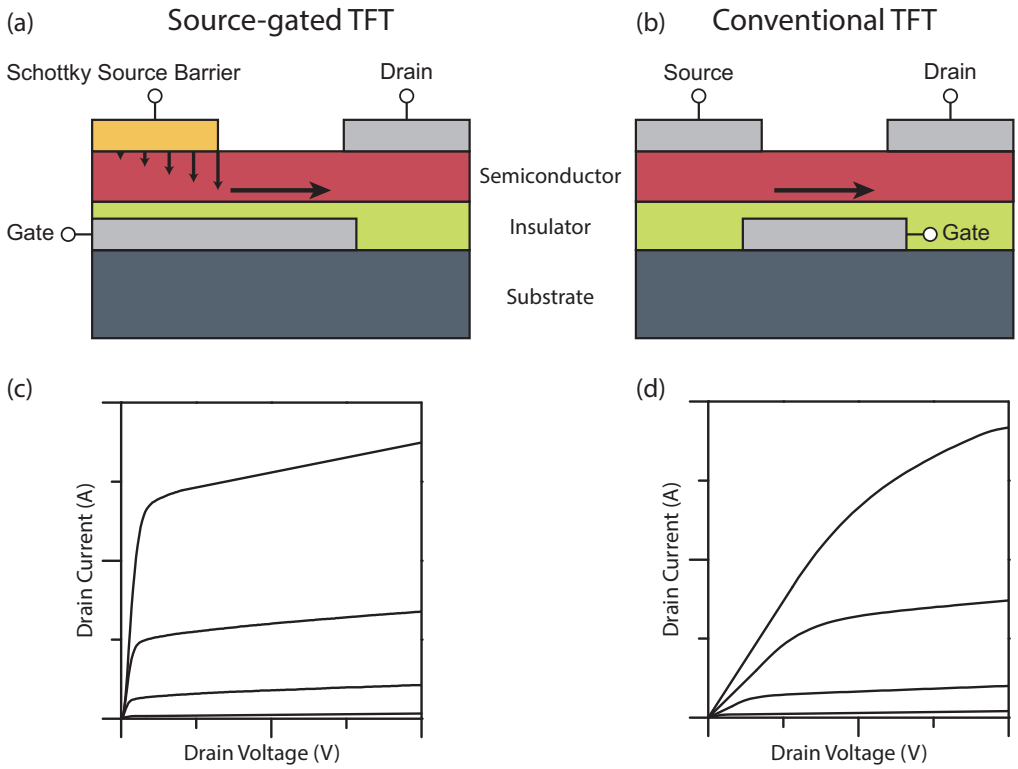

Figure 2.3: Cross-section schematics of a simple (a) SGTFT and (b) conventional TFT. The electron transport pathway is depicted by the arrows. Typical output characteristics of an arbitrary (c) SGTFT and (d) conventional TFT (based on the measurements from Ref. [52]).

device incompatible with flexible substrates but was needed to help increase the mobility as the PLD system was not capable of substrate heating during the time of this study.

2.4.1 PLD ZnO Material Properties

The material properties of the PLD ZnO thin films were investigated using atomic force microscopy (AFM) in tapping mode, grazing incidence X-ray diffraction (GIXRD), with Cu-Kα radiation (wavelength = 1.5405 Å), and the Hall effect. Fig. 2.4(a) displays an AFM image of the ZnO film surface in a 2 μm $\times$ 2 μm area. Small crystallite sizes and a low root mean squared (rms) roughness value of $\sim$ 3 nm were observed in the scan. The low rms roughness is attractive for TFTs as it promotes reduced scattering at the semiconductor/insulator interface. In the AFM image, there are some noticeable ZnO debris particles formed during the PLD growth, which increased the z-scale data range to an upper limit of 20 nm. These particles can potentially lead to higher leakage currents, but are difficult to remove from PLD processes [100]. A XRD scan of the film at a glancing angle of 0.5 degrees is shown in Fig. 2.4(b). The results reveal that the films were polycrystalline as multiple distinct peaks were present; the dominant peak corresponded to the (110) ZnO diffraction plane, while the other noticeable peaks corresponded to the (100), (002), and (101) diffraction planes. From Hall effect measurements, the ZnO electron concentration was determined to be in the order of 10^{15} - 10^{16} cm^{-3}.

2.4.2 Bottom-gated ZnO SGTFT Fabrication

The back-gated ZnO SGTFTs were fabricated according to the process flow diagram shown in Fig. 2.5. Firstly, PLD was used to grow 50 nm thick ZnO films at room temperature on a chemically cleaned SiO_2-coated Si substrate for use as the active channel layer [Fig. 2.5(a-ii)]. The hot-plate anneal at 600°C for 2 hours was done afterwards. Next, photolithography was performed to define the mesa isolation before the ZnO was wet chemically etched using ferric chloride ($FeCl_3$) [Fig. 2.5(a-iii)]. Before metallization, the ZnO surface was ultrasonically cleaned in acetone and isopropyl alcohol for 5 minutes each, rinsed

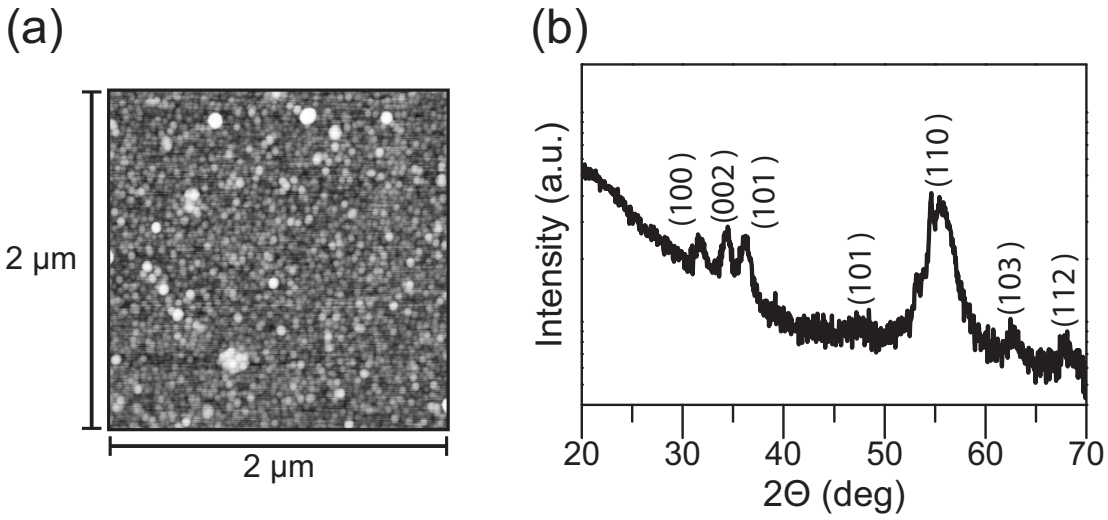

Figure 2.4: (a) Surface AFM image and (b) XRD profile of the PLD ZnO film with post-growth annealing (2 hours at 600°C). The AFM scan was conducted in tapping mode, and the data range for the z-scale is from 0 to 20 nm.

with de-ionized (DI) water, and then blown dry with nitrogen. For this study, a coaxial source-and-drain (S/D) layout [see Fig. 2.5(b)] was employed where circular gold (Au) Schottky contacts (50 nm thick) were utilized for the source while annular aluminium (Al) ohmic contacts (150 nm thick) were utilized for the drain electrodes. This layout allowed the Schottky diode characteristics of the source Schottky barrier to be easily measured by biasing the S/D contacts as a two terminal Schottky diode (i.e. the source is the anode while the drain is the cathode). Both the S/D electrodes were deposited and patterned using electron beam evaporation (at room temperature) and lift-off respectively [Fig. 2.5(a-iv,v)]. The heavily doped Si substrate was utilized as the common back gate (with the aid of Al tape), and the 200 nm thick SiO_2 layer acted as the gate insulator layer. A micrograph image of the device is shown in the top inset of Fig. 2.6, and a schematic cross-section of the device is shown in Fig. 2.7(a). In this study, the L ranged from 5 to 20 μm and the channel width (W) was determined using the equation for W/L in a coaxial S/D layout shown below [50],

$$\frac{W}{L} \cong \frac{2\pi}{\ln(D/d)} \tag{2.3}$$

where D is the is the inner diameter of the outer annulus, and d is the diameter of the inner circle.

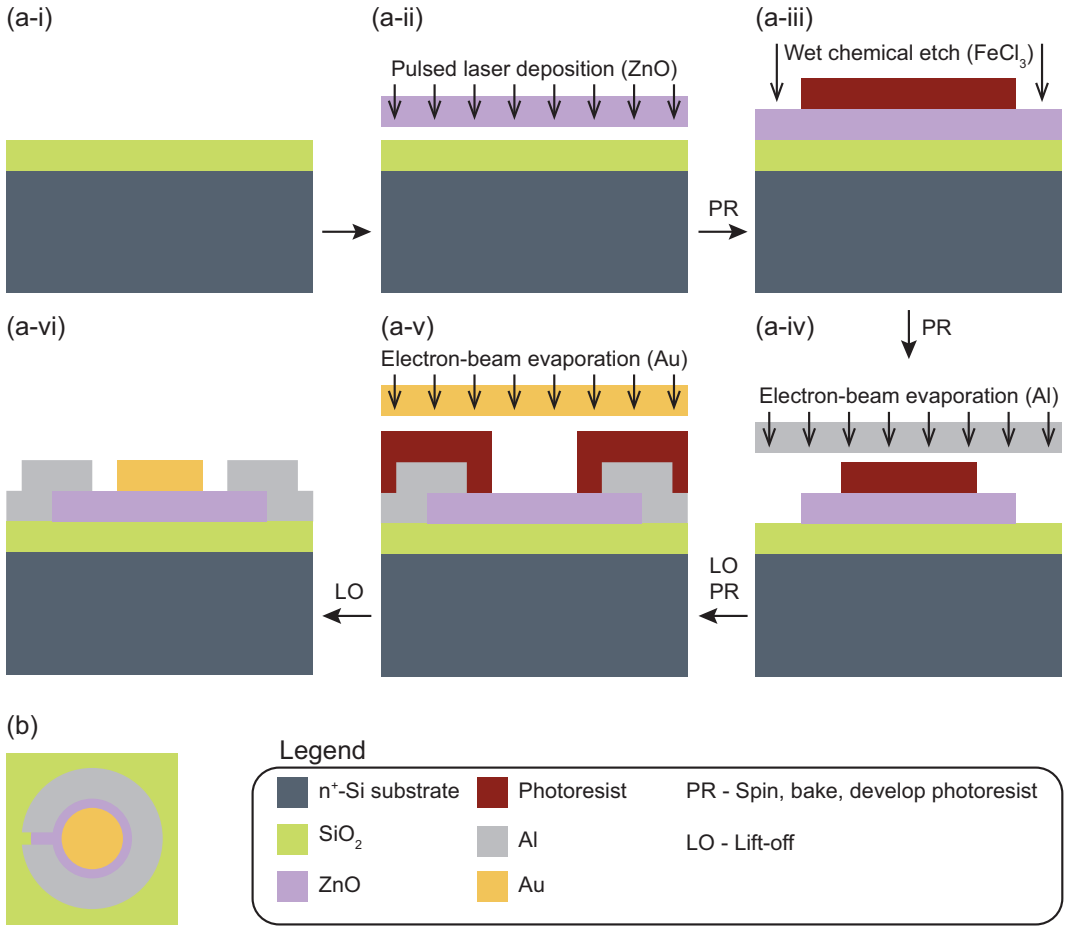

Figure 2.5: (a) Process flow for the fabrication of the bottom-gated ZnO SGTFT. (b) Top view schematic of the bottom-gated ZnO SGTFT.

2.4.3 Electrical Characteristics of the ZnO/Au Schottky Junction

The Keithley 4200 Semiconductor Characterization System (SCS) was utilized to measure the ZnO SGTFT's electrical current-voltage ($I-V$) and capacitance-voltage ($C-V$) characteristics at room temperature and in dark conditions. Firstly, the Schottky barrier at the source was characterized by biasing the

SGTFT as a two-terminal Schottky diode from the source to the drain according to the schematic shown in the bottom inset of Fig. 2.6. A typical $I-V$ and $C-V$ measurement of the source Schottky diode is depicted in Fig. 2.6. The current rectifying ratio reaches a maximum of 10 at $\pm$ 1 V, and the reverse leakage current was in the order of 10^{-7} A. From fitting the $I-V$ curves to the thermionic emission model (Equation 2.2) using the method devised by Lee *et al.* [101], the ideality factor (n) and Schottky barrier height (Φ_B) were determined to be 2.3 and 0.68 eV respectively, which are similar to the values reported in literature (e.g. Table 2.1). Lee *et al.*'s parameter extraction technique is more systematic than the conventional approach of just fitting a straight line to the diode's $\ln(I)$ plotted as a function of V. It employs an auxiliary function, $F(V) = V - V_a \ln(I)$, where V_a is an arbitrary voltage independent of V, that allows curve fitting to be used for the extraction of n and series resistance (R_S) without the uncertainty involved with graphical extraction methods. Afterwards, n and R_S can be inserted into Equation 2.2 to calculate Φ_B. The low rectification ratio and high ideality factor observed were most likely the result of using a polycrystalline ZnO thin film rather than a bulk single crystalline substrate as crystalline quality, impurities, and native point defects have been demonstrated to be important factors for the Schottky barrier quality [73]. From the $C-V$ characteristics of the Schottky junction, the ZnO n-type doping concentration (N_D) was calculated to be in the order of 10^{15} cm^{-3} (agreeing with the Hall effect measurement) using the equation for the Schottky junction's depletion-layer capacitance (under the abrupt depletion layer approximation) [45],

$$\frac{1}{C_D^2} = \frac{2\left(\psi_{bi} - V - \frac{k_B T}{q}\right)}{q\varepsilon_S N_D} \tag{2.4}$$

where C_D is the depletion capacitance (when the diode is reverse biased), ψ_{bi} is the built-in potential of the Schottky barrier, V is the applied voltage, and ε_S is the permittivity of ZnO ($8.5 \times 8.85 \times 10^{-12}$ F·m^{-1}). Consequently, from these measurements, it is evident that Au formed a rectifying junction with the PLD-grown ZnO.

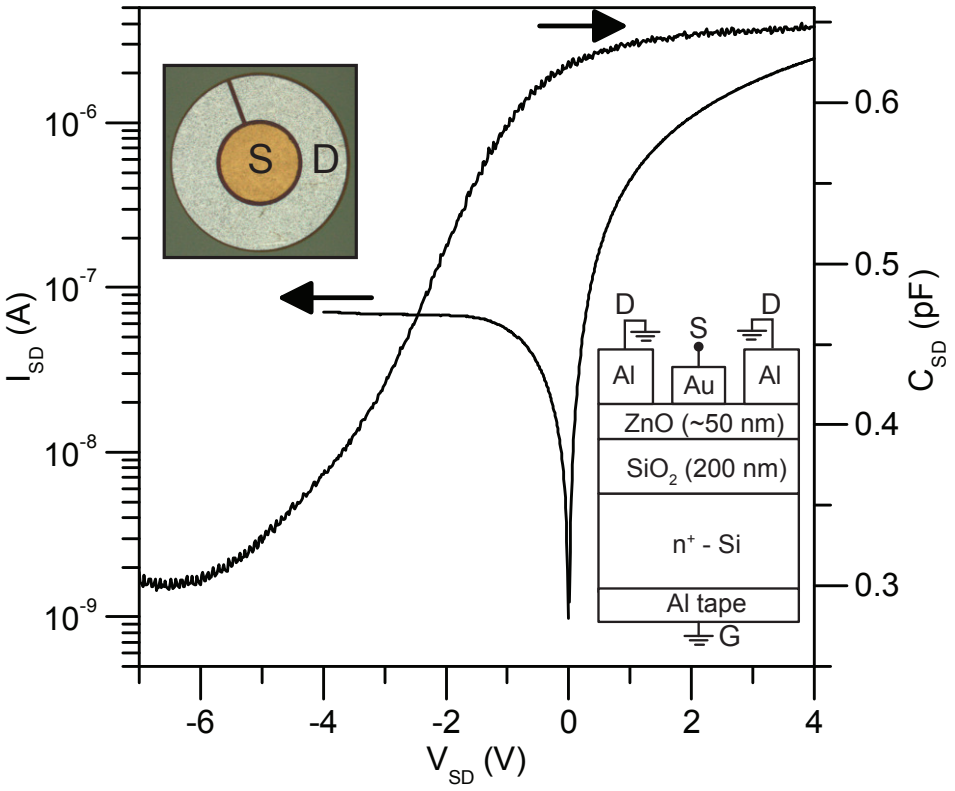

Figure 2.6: $I-V$ and $C-V$ characteristics of the ZnO/Au Schottky junction at the ZnO SGTFT's source electrode. Insets: (Top) A micrograph image of the bottom-gated ZnO SGTFT using the coaxial S/D layout. The inner radius of the outer annulus and radius of the inner circle are 120 μm and 100 μm respectively (leading to a gap of 20 μm). (Bottom) Schematic diagram of the SGTFT biased as a two terminal Schottky diode. Both the drain and substrate (which serves as the gate in the SGTFT) were grounded during the measurement.

2.4.4 Electrical Characteristics of the Bottom-gated ZnO SGTFT

Transistor electrical characteristics of the same devices were measured by biasing the bottom-gate according to the schematic shown in the inset of Fig. 2.9. Output characteristics [drain-source current (I_{DS}) versus drain-source voltage (V_{DS})] of a typical ZnO SGTFT are displayed in Fig. 2.7. The device's channel width-to-length ratio (W/L) was $\sim$ 689 μm/20 μm. N-channel transistor characteristics were observed as I_{DS} increased as the gate-source voltage (V_{GS}) was increased in the positive direction. All measured devices demonstrated transistor behaviour featuring saturation voltages of $\sim$ 6 V. As a comparison, an identical ZnO TFT with Al contacts for both the S/D electrodes (that was also concurrently fabricated on the same substrate) was measured, and its output characteristics are presented in Fig. 2.8. Even at low I_{DS} in the range of values depicted in Fig. 2.7, the Al/Al TFT did not demonstrate any current saturation in the measurement range (before V_{DS} = 10 V); i.e. the lower saturation voltages expected from the source-gated effect were observed when comparing these two devices at similar current outputs (after normalising each for W/L). Besides not saturating, the Al/Al TFT exhibited much larger currents at equivalent V_{GS} (even after accounting for the differences in W/L). The SGTFT's lower currents and saturation voltage ($V_{DS,sat}$) values are explained by the lower electron concentrations at the source due to the Au Schottky contact's depletion region. Nevertheless, transistor action was attained only using the source barrier approach, supporting the assertion made by Shannon *et al.* that the SGTFT is better suited for highly disordered semiconductors [99].

Transfer characteristics (I_{DS} vs V_{GS}) of the same ZnO SGTFT at V_{DS} = 50 mV are shown in Fig. 2.9. Evidently, the device exhibited depletion-mode behaviour as the threshold voltage (V_{th}) was less than 0 V. Moreover, the current on-to-off ratio ($I_{on/off}$) was in the order of 10^5, and the pinch-off or turn-on voltage (V_{on}) was approximately -45 V. From fitting the transfer characteristics to the ideal TFT current equation (Equation 1.8), the device's field-effect mobility (μ_{FE}) was extracted to be < 0.1 cm^{2}V^{-1}s^{-1}. The low on-state current and mobility were a product of the restricted carrier injection at the source barrier [70, 98].

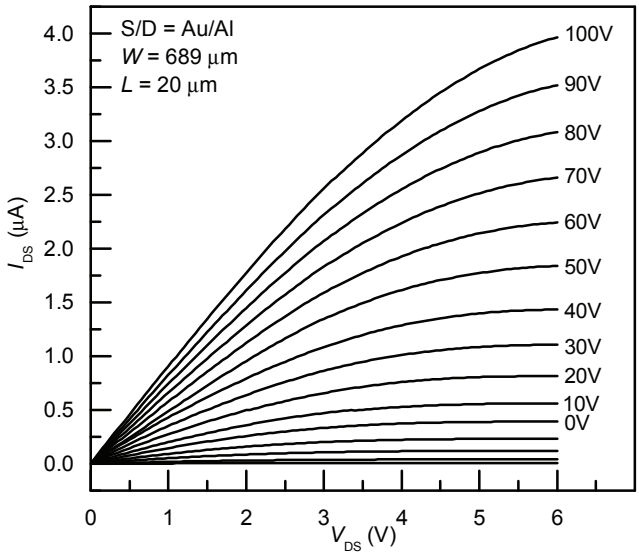

Figure 2.7: Output characteristics of the bottom-gate ZnO SGTFT with Au source and Al drain metal contacts. The gate bias ranges from -40 V to 100 V in steps of 10 V.

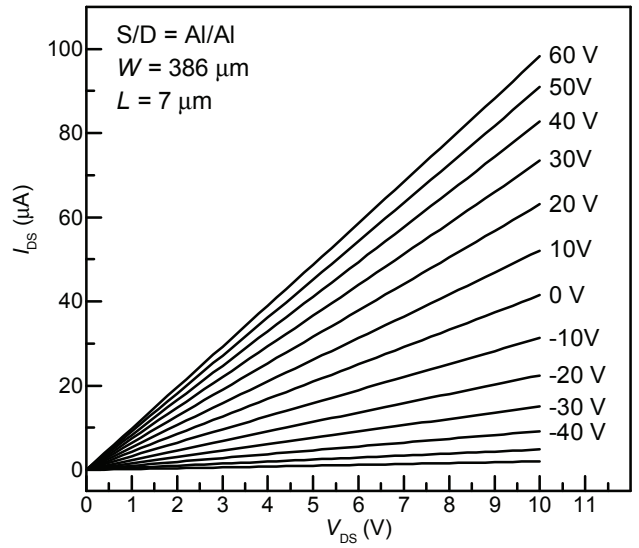

Figure 2.8: Output characteristics of a conventional bottom-gate ZnO TFT with symmetrical Al/Al S/D electrodes. The gate bias ranges from -60 V to 60 V in steps of 10 V.

Additionally, the polycrystalline PLD ZnO thin film's relatively small grain sizes would lead to reduced electrical performance due to increased hopping transport and scattering across grain boundaries [102]. The mobility values exhibited by the ZnO SGTFT were comparable to other studies that utilized physical vapour deposition (PVD) techniques at room temperature, which also resulted in films with fine grain sizes [103, 104, 105].

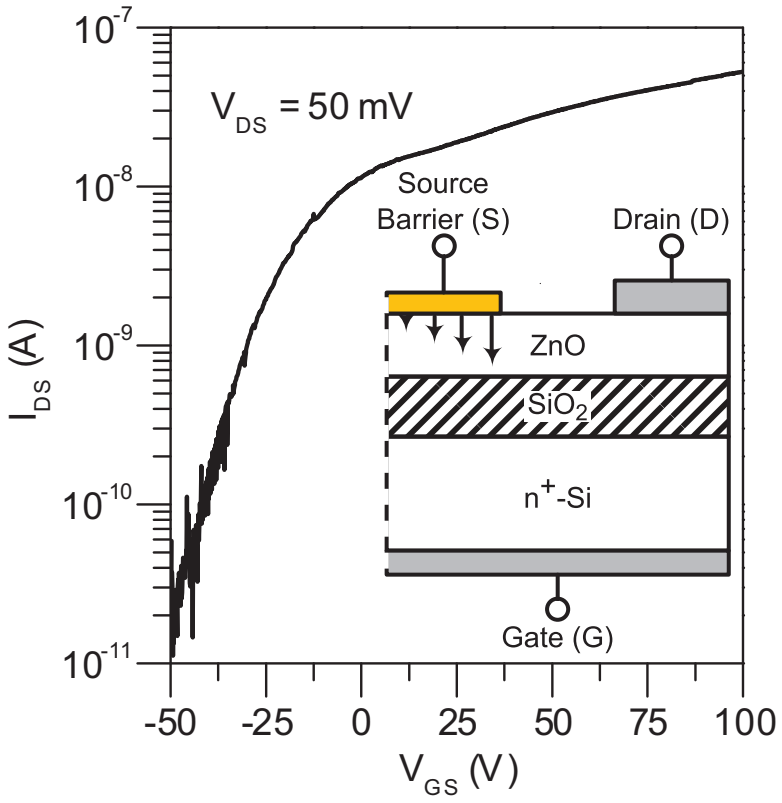

Figure 2.9: Transfer characteristics of the ZnO SGTFT with Au/Al S/D contacts at V_{DS} = 50 mV in log scale. (Inset) Schematic cross-section diagram of the SGTFT from the centre of the source to the outer edge of the drain. The current injection at the source barrier is illustrated by the arrows.

2.4.5 Physical Operation of the Bottom-gated ZnO SGTFT

Fig. 2.10 depicts the device's gate-to-source capacitance (C_{GS}) and transconductance (g_m), which was determined by applying the Savitzky-Golay differential

filter to the transfer characteristics in OriginLab's Origin software, as a function of V_{GS} at different values of V_{DS}. In the g_m-V_{GS} characteristics for $V_{DS} = 7$ V, there was a sharp spike around $V_{GS} \simeq 10$ V because of an abrupt increase in the slope of I_{DS}-V_{GS} in the transfer characteristics. Interestingly, both the g_m-V_{GS} and C_{GS}-V_{GS} characteristics show a well-defined transition at $V_{GS} \simeq 8$ V, suggesting that something changed in the SGTFT as V_{GS} was increased. In particular, the g_m-V_{GS} characteristics are surprising as the measurements differ from what is observed in conventional TFTs. A conventional transistor's g_m gradually reaches a peak before falling as V_{GS} increases due to mobility degradation, which mostly results from increased surface interface scattering as the thickness of the accumulation channel decreases with V_{GS} [106, 107, 53]. However, in these devices, after peaking, g_m underwent a second regime where it increased again with increasing V_{GS} (after $V_{GS} \simeq 8$ V) , implying that by replacing the source electrode with a Schottky barrier metal contact, there is a significant change in the device physics.

Choi *et al.* also observed a similar phenomena in their investigation of Schottky barrier field effect transistors (SB-FETs) [108]. They concluded that the second regime of increasing g_m arises from a transition in the way carriers are injected into the channel across the source Schottky barrier. The two principal transport mechanisms for carriers to move across a Schottky barrier are thermionic emission (TE) and tunnelling (TU), which can include thermionic field emission (TFE). According to thermionic emission theory (Equation 2.2), carriers can only pass through the Schottky barrier if they have enough energy to overcome the potential barrier. However, if the Schottky barrier's width is thin enough, carriers can tunnel through, and TU can become the dominant carrier injection mechanism. In n-channel SB-FETs, it was observed (from simulations and experiments) that the gate potential modulates the Schottky barrier's width so that there is a transition in the dominant current injection mechanism at the source from TE to TU as V_{GS} increases [108, 109, 110, 111, 96]. Hence, the gate potential controls the tunnelling current that gets injected through the source Schottky barrier. An illustration of this concept using idealized energy band diagrams is given in Fig. 2.11. When no bias is applied to the gate and drain [Fig. 2.11(a)], the current injected across the source barrier is mostly determined by TE (with limited TU) if the Schottky barrier is not too thin. If a negative V_{GS} is applied to

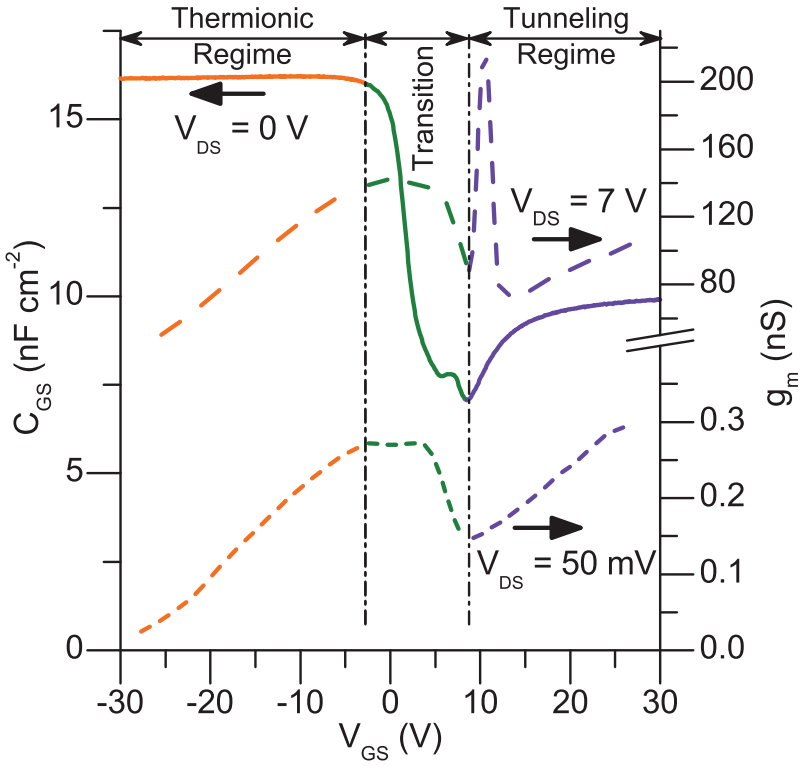

Figure 2.10: (Left) C_{GS} of the ZnO SGTFT at $V_{DS} = 0$ V. (Right) g_m of the ZnO SGTFT at $V_{DS} = 7$ V (long-dash) and $V_{DS} = 50$ mV (short-dash).

the gate, the energy bands shift upward as shown by Fig. 2.11(b), and barrier's width increases thereby reducing the TU current ($J_{e,tunnelling}$). Thus, the current across the Schottky barrier is mostly consisted of TE current ($J_{e,thermionic}$). On the other hand, if a positive V_{GS} is applied to the gate, the energy bands shift downward as shown by Fig. 2.11(c), and the width of the barrier decreases. As V_{GS} is further increased, $J_{e,tunnelling}$ eventually becomes the dominating component passing across the Schottky barrier. Consequently, for an ideal SB-FET, the off-current and on-current are primarily comprised of $J_{e,thermionic}$ and $J_{e,tunnelling}$ respectively.

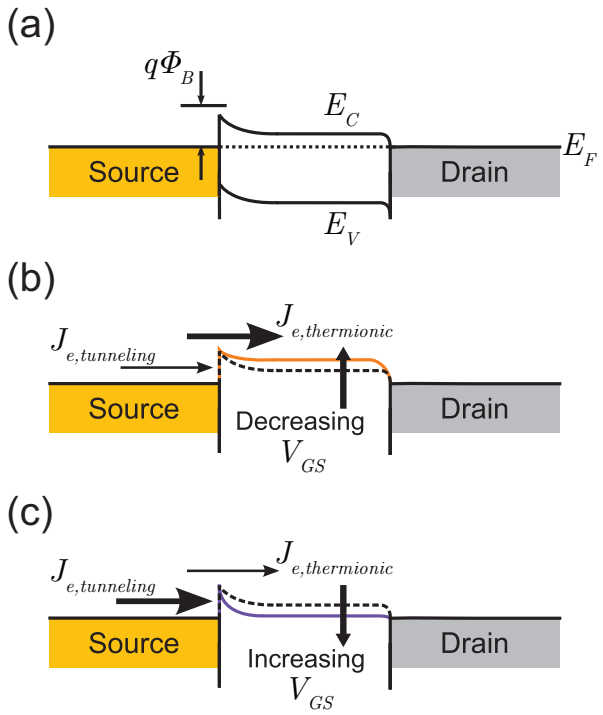

Figure 2.11: (a) Idealized energy band diagram of the SGTFT at zero V_{GS} and V_{DS}. Conceptual energy band diagrams of the SGTFT showing the variation in the Schottky barrier width and the dominant carrier injection mechanism at the source with (b) decreasing and (c) increasing V_{GS}.

Based on the aforementioned device description, the distinct transition around $V_{GS} = 8$ V shown by both the g_m-V_{GS} and C_{GS}-V_{GS} characteristics can be interpreted as the moment where the dominant carrier injection mechanism changed

from TE to TU. Therefore, in Fig. 2.10, the segment of the curve before and after $V_{GS} = 8$ V are labelled as the thermionic and tunnelling regimes respectively. According to these results, it should be possible to take advantage of the different device physics to specifically engineer an enhancement-mode (normally-off) ZnO TFT using the SGTFT architecture. Since the transition between TE-dominated current to TU-dominated current was observed at $V_{GS} > 0$ V, if the device is modified so that $J_{e,thermionic}$ and $J_{e,tunnelling}$ are minimal when the device is off, then V_{th} would be pushed higher, approaching the transition voltage. For instance, if the quality of the source Schottky barrier is improved (e.g. lower ideality factor and better rectification ratio), the leakage current through the barrier will be reduced until V_{GS} reaches the transition voltage. At the transition point, the Schottky barrier width is, presumably, thin enough for carriers to easily tunnel through, and the drive current greatly increases, effectively making the device more enhancement-mode as long as the off-current is low. Henceforward, the SGTFT architecture offers an unique approach to engineering an enhancement-mode ZnO TFT by controlling the properties of the source Schottky barrier to tailor device performance. The usual method to achieve a normally-off ZnO TFT is to optimize a growth recipe that yields high resistivity ZnO thin films with low carrier concentrations. With a highly ordered, low defect semiconductor material, a high performance, normally-off TFT can be achieved. However, for most ZnO growth techniques, high growth temperatures and/or high temperature post-growth annealing are necessary to obtain the material properties suitable for a high performance, enhancement-mode ZnO TFT. This makes the fabrication process more expensive and incompatible with emerging flexible electronics. Therefore, the SGTFT can be an effective means to realise a normally-off ZnO TFT with a lower thermal budget.

2.5 Summary of Bottom-gated PLD ZnO SGTFTs

In this chapter, the Schottky barrier SGTFT device architecture is introduced, and its unique method of current control using a gate-controlled source injection barrier is discussed. A bottom-gated ZnO SGTFT that utilized a Schottky source and ohmic drain contact with a ZnO channel deposited by room-temperature

PLD was fabricated and studied. Although the device exhibited low mobility values and a negative V_{th}, transistor characteristics were observed only when using the SGTFT approach. Moreover, the ZnO SGTFT exhibited unique C_{GS}-V_{GS} and g_m-V_{GS} characteristics that gave insight into the physics of the SGTFT device operation. Based on these measurements, it is expected that the SGTFT can offer a new approach to engineering an enhancement-mode ZnO TFT by exploiting the source Schottky barrier to limit the device's off-current. Thus, if the SGTFT device architecture can enable the production of high-performance, normally-off ZnO TFTs without needing high processing temperatures, it can have a significant impact on the future of ZnO-based electronics.

Chapter 3

Top-gated Zinc Oxide Source-gated Thin Film Transistors by Low Temperature Atomic Layer Deposition

While the bottom-gated zinc oxide (ZnO) Schottky barrier source-gated thin film transistors (SGTFTs) presented in the previous chapter showed many promising device characteristics, its device structure is not practically useful beyond use as a proof-of-concept device (i.e. for demonstrating the ZnO film's electrical performance and the physics of the SGTFT concept) [6]. Moreover, because of the device's relatively large dimensions, some important factors such as contact resistance may have been understated. Thus, a new TFT structure utilizing the Schottky source barrier concept that is better suited for integrated circuits used in real-world applications was designed and fabricated. For this new design, low-temperature atomic layer deposition (ALD) was employed for depositing both the ZnO active channel and high-κ gate insulator layer, introducing many advantages such as compatibility with flexible electronics and high scalability. The content of this chapter was previously published in Ref. [112].

3.1 Zinc Oxide and Hafnium Oxide Films Grown by Low Temperature ALD

ALD is an attractive thin film deposition technique for fabricating both the semiconductor and dielectric materials in ZnO TFTs because of its highly conformal and uniform films, which are especially appealing for inexpensive, highly scalable manufacturing processes. ZnO films grown by ALD have demonstrated many desirable electrical characteristics for TFT applications such as moderately high mobilities (reported values range from 0.1 to 20 $cm^2V^{-1}s^{-1}$) at low processing temperatures below 200°C [59, 23, 24, 113, 67]. Thus, a major advantage of ALD ZnO films is its compatibility with inexpensive plastic- or polymer-based flexible substrates. However, they also typically exhibit high residual carrier concentrations and high conductivities, widely accepted to be the result of native defects and impurities [113, 66, 61], which could make them unsuitable for TFT applications.

For good transistor performance, it is imperative that the gate dielectric is of high quality. In the bottom-gated SGTFT device, this was easily achieved using high quality thermal SiO_2. For this top-gated device, however, the gate dielectric layer is deposited as a thin film and patterned afterwards. Notably, high-κ gate dielectrics such as hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) deposited by ALD at low temperatures have shown appealing dielectric properties (e.g. low gate leakage currents, high dielectric strength, and low interface trap densities) [59, 114, 115]. Consequently, if these high quality gate dielectrics are implemented for ZnO TFTs, the device performance can be dramatically increased [59, 23, 68]. For instance, in the work by Grundbacher *et al.*, low temperature ALD processes were utilized for fabricating a bottom-gated ZnO TFT with a HfO_2 dielectric. These devices exhibited excellent TFT characteristics including a saturation mobility (μ_{sat}) of 11 $cm^2V^{-1}s^{-1}$, current on-to-off ratio ($I_{on/off}$) $> 10^6$, threshold voltages (V_{th}) ranging from -2.7 V to 6.3 V depending on the ZnO channel thickness, and a subthreshold swing (SS) of $\sim$ 500 mV. Based on these reports, the feasibility of an entirely ALD-based ZnO TFT that can be fabricated at low temperature with good device performance is extremely promising.

Thermal ALD at 130°C in a Kurt J. Lesker ALD-150LX system was used to

deposit a 30 nm thick ZnO film on a silicon (Si)/silicon oxide (SiO_2) substrate for characterization of its material properties before being employed for a ZnO TFT. The precursors used for the deposition were diethylzinc (DEZn) and water. A J.A. Woollam M-2000DI ellipsometer was used to monitor the film thickness *in situ*. X-ray diffraction (XRD) and atomic force microscopy (AFM) were utilized to analyse the ZnO films, and the results are shown in Fig. 3.1. From the XRD scan of the ZnO by itself [Fig. 3.1(a, top)], it is apparent that the low temperature ALD ZnO films were polycrystalline by the presence of multiple distinct peaks. The strongest peaks correspond to the (002), (101), (100), and (110) diffraction planes. It has been reported that the crystallinity can be improved by increasing the growth temperature on account of the columnar (002) phase becoming the sole dominant crystal orientation [116]. However, increasing the growth temperature is not feasible for flexible electronics. Fig. 3.1(b, left) displays a AFM scan of the ZnO film. The ZnO films were found to be uniformly smooth with a low root mean squared (rms) surface roughness of 0.25 nm over a 1 μm $\times$ 1 μm area and have small grains with indistinguishable boundaries. Thus, the low temperature ALD ZnO showed promising material properties for use as active channel layers in TFT devices.

A limitation of ALD-grown ZnO is its intrinsic high carrier concentrations ($>$ 10^{18} cm^{-3}) [113, 61, 66]. Active channel layers with high carrier concentrations are unattractive as they are too conductive in the absence of a gate voltage (causing high off-currents and making it difficult for the drive current to saturate). It has been reported that the ZnO n-type doping concentration (N_D) can be reduced by lowering the growth temperature [113, 61]. However, this also correspondingly reduces the film's mobility meaning that growth temperature should be set at a value that balances the ZnO mobility and N_D. Nevertheless, the SGTFT device architecture can help achieve good transistor behaviour when using these highly doped films because of the lowered carrier concentration at the source from the Schottky barrier's depletion region. Consequently, the SGTFT could potentially allow for higher ALD growth temperatures to help maximize the device mobility while still realising good TFT characteristics.

To improve the device performance and scalability, ALD-grown HfO_2 films were employed as the gate insulator layer for the ZnO SGTFT. Directly on the

ALD ZnO films, a 10 nm thick (equivalent to 60 ALD cycles) HfO_2 film was deposited using plasma enhanced atomic layer deposition (PEALD) at 100°C. The HfO_2 deposition was done using tetrakis(dimethylamino)hafnium (TDMAH) and remote oxygen plasma (ROP) as the hafnium and oxygen precursors respectively. Fig. 3.1(a, bottom) depicts the XRD scan of the ZnO/HfO_2 multilayer structure. The peaks in the XRD spectra were broadened compared to the peaks from the XRD scan of the ZnO by itself; however, no additional peaks other than the ones observed for ZnO were present. Consequently, the XRD scan implies that the HfO_2 film structure was amorphous, which is highly desirable for high performance electronics [117]. This was also confirmed by the AFM image of the ZnO/HfO_2 stack shown in Fig. 3.1(b, right) that showed no noticeable changes in the grain size and structure compared to Fig. 3.1(b, left). The rms roughness of the multilayer stack increased from 0.25 nm to 1.3 nm indicating that the HfO_2 was relatively smooth. Therefore, the entirely ALD-grown ZnO/HfO_2 stack demonstrated promising characteristics for a high performance ZnO TFT.

3.2 Top-gated Buried Source ZnO Schottky Barrier SGTFT Fabrication

Schematics and a micrograph image of the top-gated ZnO SGTFT are shown in Fig. 3.2. The fabrication procedure for the top-gated ZnO SGTFT is presented in Fig. 3.3. Firstly, 13 nm of titanium tungsten (TiW) was deposited onto an insulated Si/SiO_2 wafer via sputtering and patterned using lift-off to form the buried source Schottky barrier electrode [Fig. 3.3(a-ii)]. A bottom source contact was utilized for this updated SGTFT structure to help control the properties of the Schottky metal/semiconductor junction and protect it from contamination during the device processing. TiW was chosen as the source metal due to its good material properties (e.g. high thermal reliability and good resistance to wet chemical etches) and its relatively low cost (which is attractive for high throughput manufacturing processes). Although gold (Au) exhibited good Schottky characteristics in the bottom-gated ZnO SGTFTs from the previous chapter, it did not display rectifying behaviour when employed as a bottom

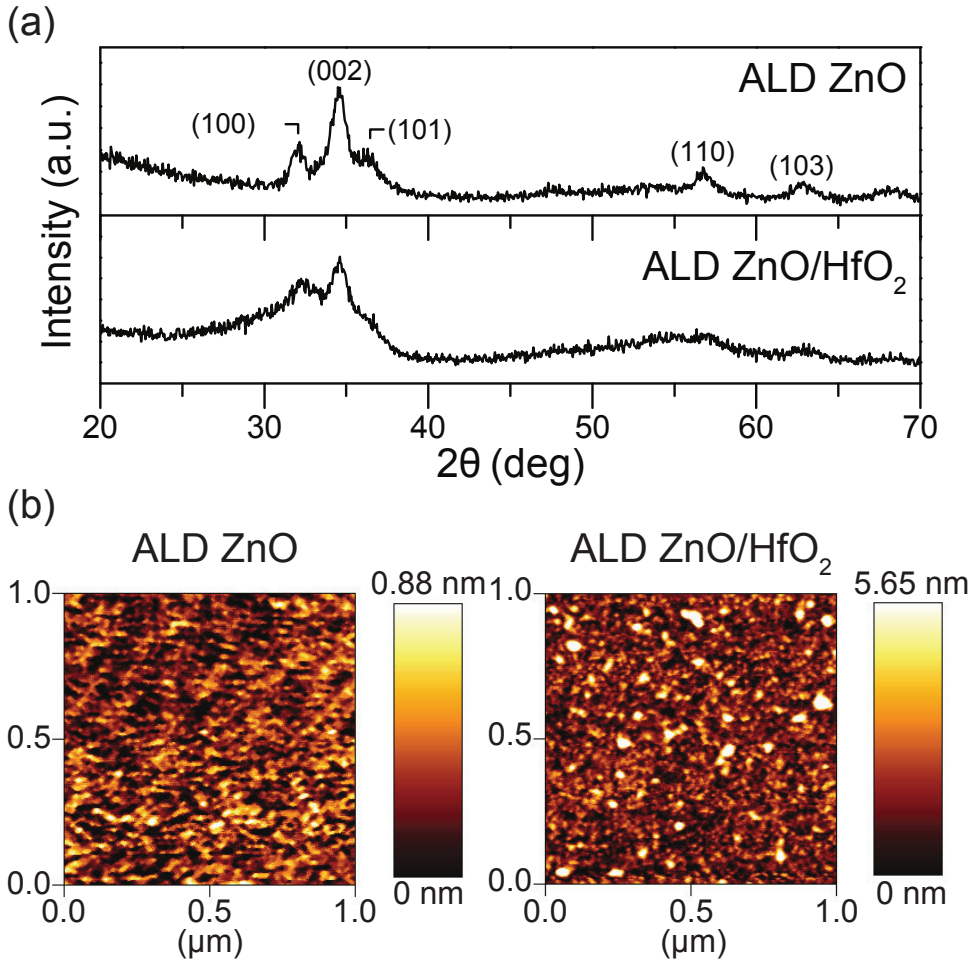

Figure 3.1: (a) XRD scans of the (top) ALD ZnO and (bottom) ALD ZnO/HfO_2 multilayer stack. (b) AFM images of the (left) ALD ZnO and (right) ALD ZnO/HfO_2 multilayer stack.

electrode due to the ALD ZnO's higher residual electron concentrations induced by the Au (details are presented in Chapter 4). Afterwards, a short 20 second ROP clean was done to clean the surface before 15 nm of ZnO was deposited by thermal ALD at 130°C to form the semiconductor channel [Fig. 3.3(a-iii)]. The pre-growth ROP clean also caused the ZnO doping concentration to increase when compared to identical films grown without the pre-deposition treatment (which were utilized in the devices presented in the following chapters); the extent that the electron concentrations increased was not quantified however. It is likely that the ROP oxidized the bottom metal contact thereby attracting more interface dopants such as OH^- during the first few cycles of thermal ALD ZnO growth (as observed in Section 4.3). Thus, the electronic properties of the ALD ZnO employed in these ZnO SGTFTs were not the same as the films grown for the upcoming top-gated staggered and drain-offset ZnO TFTs in Chapters 4 and 5. Once again, ferric chloride ($FeCl_3$) was used to pattern the channel via wet chemical etching [Fig. 3.3(a-iv)]. Lift-off was used to pattern the gate insulator layer that was deposited next; in order to do so, a thin $\sim$ 1.7 nm thick (equivalent to 10 ALD cycles) HfO_2 layer was first blanket deposited using PEALD at 100°C before forming the photoresist. This HfO_2 cap oxide layer helped protect the ZnO film from being etched by the photoresist developer. According to the report by Grundbacher *et al.* [23], the HfO_2 cap oxide layer is more practical than using an aluminium (Al) sacrificial layer, but it reduces the drive current and increases the contact resistance slightly. When measuring the lateral current between two top drain contacts deposited on ZnO with the thin HfO_2 cap layer sandwiched in-between, slightly non-ohmic current-voltage ($I - V$) characteristics were observed unfortunately. After patterning the photoresist, another 50 cycles of HfO_2 was deposited to finish forming the gate insulator layer (resulting in a $\sim$ 10 nm thick HfO_2 film in total) [Fig. 3.3(a-v)]. Lastly, the top gate and drain ohmic contacts were formed and patterned simultaneously by depositing an Al/Au (20 nm/60 nm thick) multilayer metal stack via sputtering and lift-off respectively [Fig. 3.3(a-vi)]. Because the gate and drain were fabricated together, a drain-offset region between the gate-and-drain was necessarily formed. A side and top view schematic of the completed top-gated ZnO SGTFT is shown in Fig. 3.3(a-vii) and Fig. 3.3(b) respectively.

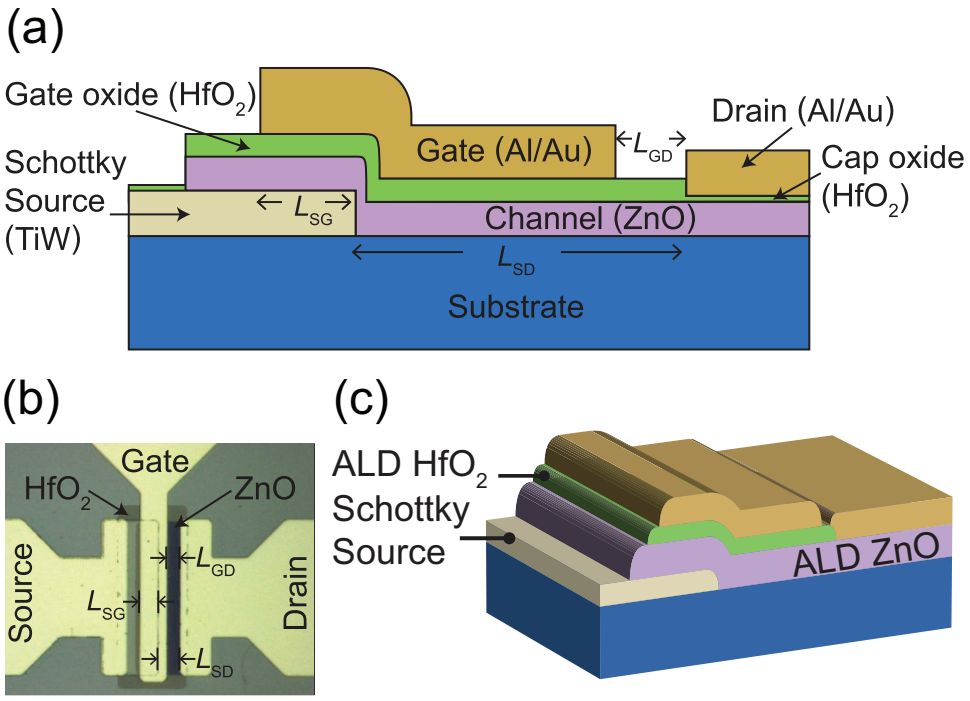

Figure 3.2: (a) Cross-sectional schematic diagram of the top-gated ZnO SGTFT. (b) Micrograph of the ZnO SGTFT (top view). (c) Three-dimensional schematic image of the top-gated ZnO SGTFT.

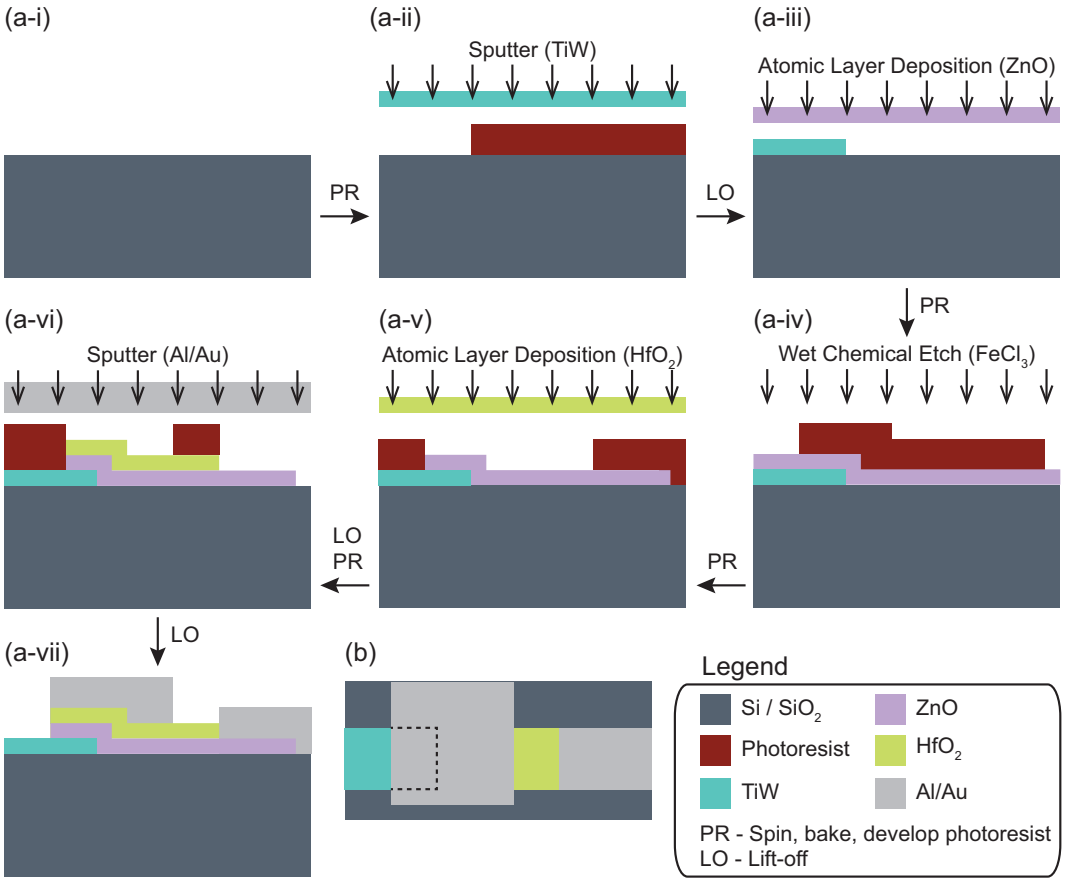

Figure 3.3: (a) Illustration of the process flow for the fabrication of the top-gated ZnO SGTFT. (b) Top view schematic of the top-gated ZnO SGTFT.

3.3 Electrical Characteristics of the Top-gated ZnO SGTFT

The output characteristics, drain-source current (I_{DS}) versus drain-source voltage (V_{DS}), of a typical top-gated ZnO SGTFT, with a source-to-drain spacing (L_{SD}) and channel width (W) equal to 16 μm and 100 μm respectively, is shown in Fig. 3.4. Relatively high drive currents were observed for the device's dimensions reaching 1.6 mA/mm at a gate-source voltage (V_{GS}) of 2.5 V. A clear advantage of this device was its ability to operate at $V_{DS} > 20$ V while still maintaining excellent saturation characteristics due to the combination of the drain-offset and source-gated structures (their effects are discussed in the following paragraphs). The device's output conductance (g_{ds}) ranged from 3.0 nS to 3.6 μS as V_{GS} was increased, which were calculated from the slope of I_{DS}-V_{DS} in the saturation regime,

$$g_{ds} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right) \tag{3.1}$$

From Hall effect measurements, the ALD ZnO film's residual electron concentration was calculated to be approximately $\sim 10^{17}$ cm^{-3}. Therefore, the good saturation characteristics exhibited by the transistor despite the ALD ZnO film's relatively high N_D is attributed to the source-gated effect (where the source Schottky barrier helps deplete carriers at the source thus improving current control and reducing g_{ds} [99]). The inclusion of an offset region between the gate-and-drain for this device delayed the device saturation however (an investigation of the offset-drain is described in Section 5.6); hence, the low saturation voltages expected from the source-gated effect were not observed. Fig. 3.5 displays the I_{DS}-V_{DS} characteristics of the same device while biased as a two terminal Schottky diode from the drain-to-source (where the Schottky junction is forward biased for negative V_{DS} and vice versa). It is apparent from this measurement that there was rectifying behaviour at the TiW/ZnO interface; however, it was not consistently observed for all devices. Most likely, the device-to-device variations resulted from processing non-uniformities such as unclean interfaces or inconsistencies during sputtering of the TiW film. For instance, in the upcoming Section 4.3, there is

evidence that the oxidation of TiW prior to thermal ALD ZnO growth attracted the adsorption of interface dopants at the TiW/ZnO interface, which would make it more difficult to attain consistent TiW/ZnO Schottky barriers.

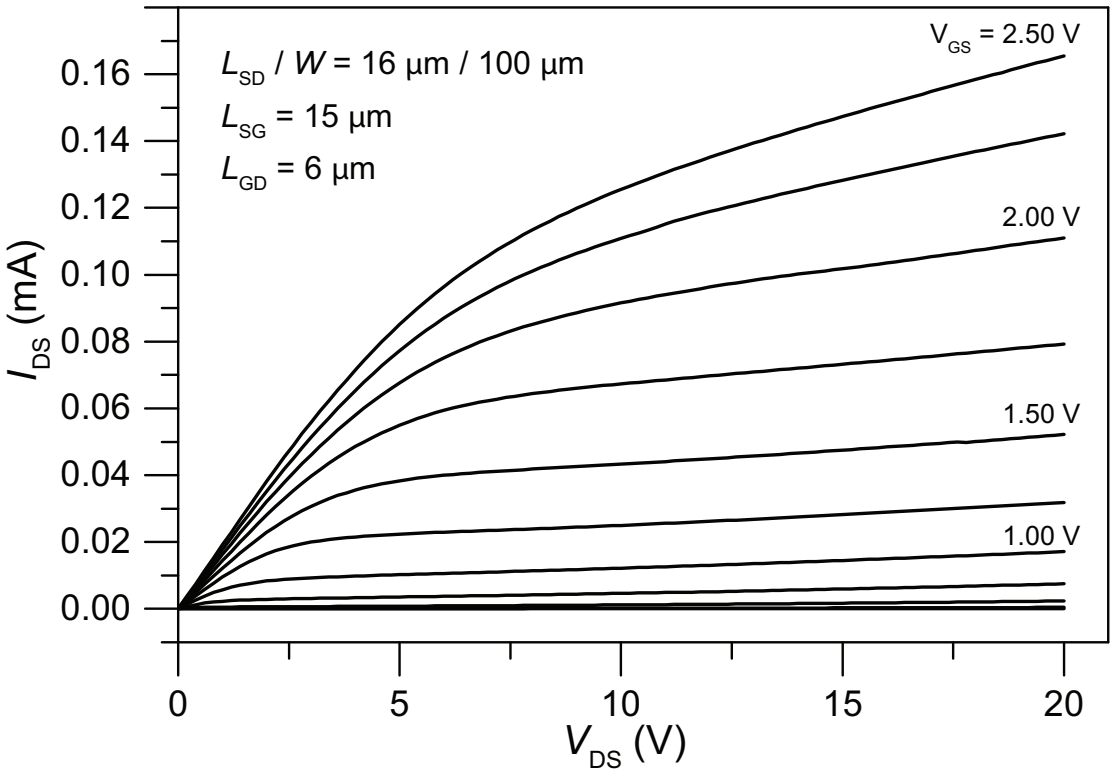

Figure 3.4: (a) Output characteristics of the top-gated ZnO SGTFT. V_{GS} increases from 0 to 2.5 V in 0.25 V steps.

Fig. 3.6 displays the transfer (I_{DS} versus V_{GS}) characteristics of the top-gated ZnO SGTFT. Compared to the bottom-gated SGTFTs presented in the previous chapter, the operating voltage range is much lower due to the high-κ dielectric, which is attractive for reducing power consumption. From fitting a straight line to the square root of I_{DS}, the threshold voltage (V_{th}) was extracted to be 0.91 V. Additionally, the current on-to-off ratio ($I_{on/off}$) reached 7×10^7, and the off-state current (I_{off}) was $\sim 1 \times 10^{-12}$ A. Therefore, this device showed enhancement-mode behaviour. From the transistor's saturation regime, the saturation mobility (μ_{sat}) was determined to be 3.9 $cm^2V^{-1}s^{-1}$, which is much greater than the maximum ~ 1 $cm^2V^{-1}s^{-1}$ demonstrated by hydrogenated amorphous silicon (a-

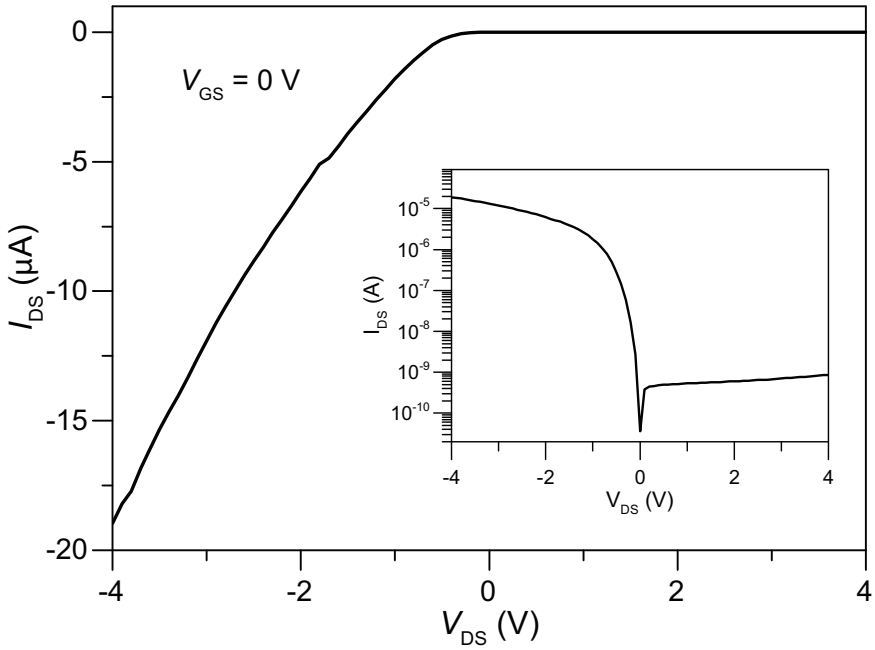

Figure 3.5: $I - V$ characteristics of the Schottky diode at the top-gated ZnO SGTFT's source where I_{DS} was measured from the drain-to-source electrodes with the gate floating. The inset shows the same $I - V$ characteristics in log scale.

Si) TFTs, by fitting I_{DS} to Equation 1.11. Typically in source-gated transistors (SGTs), the drive current and mobility are reduced because of the source Schottky barrier's current limiting nature [97]. Nonetheless, these top-gated ZnO SGTFT devices achieved comparable performance (e.g. μ_{sat}, V_{th}, $I_{on/off}$) with other low temperature ALD-based ZnO TFTs [61, 62, 63, 23], which indicates that the TiW/ZnO Schottky barrier did not dramatically restrict carrier injection at the source. A low subthreshold swing (SS) of 192 mV/decade was measured from the maximum slope in the transfer curve using the following equation,

$$SS = \frac{\partial V_{GS}}{\partial \log_{10}(I_{DS})} \tag{3.2}$$

The thin high-κ gate dielectric allowed for more efficient charge control in the channel (from higher electric fields) leading to lower values of SS. These results are promising for low power switching applications.

The device's I_{DS}-V_{DS} characteristics at the onset of soft breakdown is shown in Fig. 3.7(a). For this device, a breakdown voltage (V_{BD}) of $\sim$ 30 V was observed. The breakdown voltages of similar devices with all equal dimensions except for the gate-to-drain distance (L_{GD}), which was the key dimension affecting V_{BD}, are plotted in Fig. 3.7(b). The lowest V_{BD} measured was $\sim$ 20 V for a L_{GD} of 2 μm. Thus, all the devices exhibited high V_{BD} for their dimensions, making them very appealing as circuit drivers in any application requiring high pull-down voltages. The high V_{BD} resulted from a reduced peak electric field at the gate edge (closest to the drain) due to the top-gated SGTFT's drain-offset structure [118, 119]. More in-detail analysis of the drain-offset device architecture is given in Chapter 5.

When the device's source-to-gate overlap (L_{SG}) and L_{SD} were manipulated, a confident conclusion of their effects on the transistor characteristics was unable to be formulated because of inconsistent behaviours from device-to-device. In two-dimensional (2-D) cross-sectional technology computer-aided design (TCAD) simulations of the SGT done by Sporea *et al.* [120], it was observed that I_{DS} increased linearly with L_{SG} before it saturates due to current crowding at the edge of the source (opposite to the drain). However, in the top-gated ZnO SGTFTs, as L_{SG} was increased from 5 to 20 μm, there was no discernible effect on the

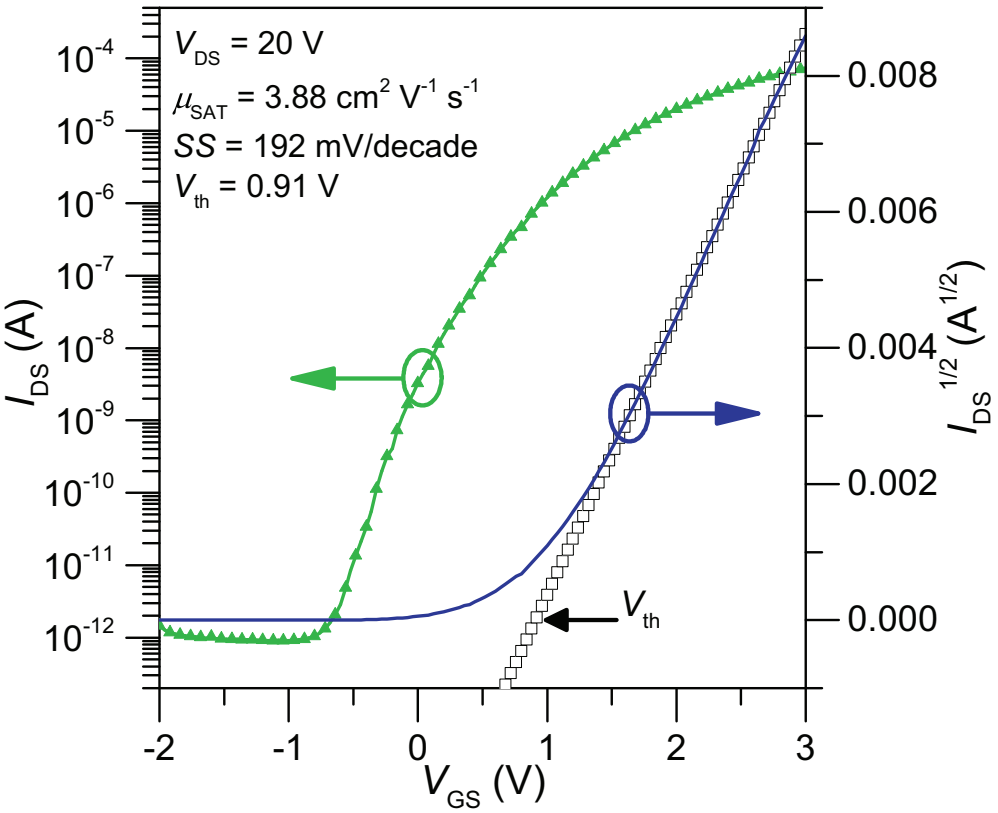

Figure 3.6: (Left) Transfer characteristics of the top-gated SGTFT at a V_{DS} of 20 V in log scale. (Right) The linear least squares fit to the square root of I_{DS} used to determine V_{th}.

transistors' output characteristics. Similarly, there was no significant relationship between I_{DS}-and-L_{SD} as L_{SD} was increased from 4 to 64 μm. 2-D simulations of the SGTs also predict that L_{SD} should have no influence on I_{DS}, which is a major difference from the conventional TFT, because the modulation of current is controlled by the source barrier (for an ideal SGTFT) [120, 97, 98]. Since the ZnO SGTFTs presented in Chapters 2 and 3 do not completely exhibit the characteristics of the Si-based SGTFTs (e.g. saturation voltages < 2 V) reported in literature [69, 99], the devices in this research were presumably not fully ideal SGTFTs. Most likely, the current in these devices was controlled primarily by the modulation of the source barrier with some secondary influence from the channel conductance. Nonetheless, the device-to-device variations in this study are attributed to processing non-uniformities rather than the TFT's dimensions. To gain an in-depth understanding of L_{SD} and L_{GD}'s effect on the top-gated ZnO SGTFT device performance, future measurements on more consistent devices will be required (this study is described later in Chapter 5).

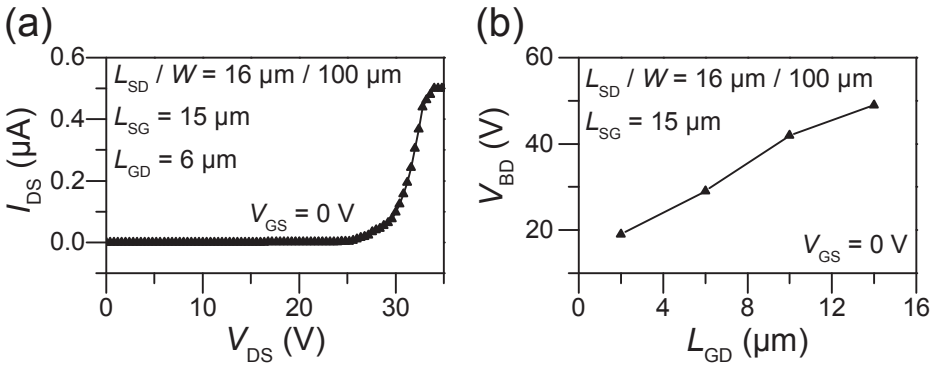

Figure 3.7: (a) Breakdown characteristic of the top-gated ZnO SGTFT at zero gate bias. (b) Breakdown voltages (V_{BD}) of the ZnO SGTFT with varying gate-to-drain spacing (L_{GD}).

3.4 Summary of Top-gated ZnO SGTFTs

The characteristics of the top-gated ZnO SGTFT presented herein this chapter performed better than the device in the previous chapter due to the many

changes in the transistor design and materials. Firstly, the mobility and doping concentrations of the ALD ZnO deposited at 130°C were higher than the pulsed laser deposition (PLD) ZnO grown at room temperature contributing to better on-state TFT performance. Next, employing high-κ HfO_2 as the gate insulator instead of SiO_2 also improved the top-gated ZnO SGTFT's drive currents and reduced the operating voltages because of HfO_2's better dielectric properties such as its larger capacitance densities. Utilizing the top-gated TFT structure instead of the alternative bottom-gated design was done based on processing considerations as it allowed the gate and offset-drain to be simultaneously fabricated and the HfO_2 gate insulator to function as a pseudo-passivation layer as well. The bottom contact TiW Schottky barrier was not consistently observed unlike the Au top Schottky contact in the previous devices presumably due to the ALD ZnO's comparably higher electron concentrations and also because of interface dopants at the TiW/ZnO interface (which will be discussed in the following chapter). Nonetheless, both Schottky barrier contacts were able to produce the characteristics of the source-gated effect when incorporated in the ZnO SGTFT.

In summary, a normally-off, top-gated ZnO SGTFT employing a TiW buried source Schottky barrier electrode was demonstrated with an ALD-grown ZnO active channel and HfO_2 gate insulator. Processing temperatures were kept below 130°C to allow for integration with low-cost flexible substrates in the future. The source-gated effect was exploited to achieve enhancement-mode operation featuring a positive V_{th}, high $I_{on/off}$, and low SS. A relatively high mobility of 3.9 $cm^2V^{-1}s^{-1}$ was also demonstrated. The device structure included an offset region between the gate-and-drain leading to consistently large breakdown voltages greater than 20 V (for a gate-to-drain spacing as low as 2 μm). Consequently, the top-gated ZnO SGTFT is especially promising for integration in next-generation flat panel displays (FPDs), emerging flexible electronics, and large area integrated circuits.

Chapter 4

Contact Effects in Top-gated Staggered Zinc Oxide Thin Film Transistors

In the previous chapter, a source Schottky barrier was utilized to counter the negative effects from the high residual electron concentrations in atomic layer deposition (ALD)-grown zinc oxide (ZnO) to attain a ZnO thin film transistor (TFT) with good saturation characteristics and a moderate device mobility. However, in order for continued improvements in device performance and reliability, more insight on how the TFT's design, material, and process parameters influence device behaviour is required. Notably, the role of contact effects in ZnO TFTs is still unclear despite it being a widely investigated topic for TFTs based on amorphous oxide semiconductors [e.g. indium-gallium-zinc-oxide (IGZO)] and organic semiconductors [121, 122, 123, 124].

Organic field effect transistors (OFETs) typically suffer from high contact resistance at the source-and-drain (S/D) contacts that limit the carrier injection and cause non-linear current-voltage ($I-V$) characteristics [123]. Similarly, metal oxide semiconductor TFTs are also strongly influenced by the nature of the contact interfaces at the S/D electrodes. For instance, in a study by Xu *et al.* [125], the TFT's threshold voltage (V_{th}) and drive current were noticeably affected when the S/D metallization was altered. They attributed this to differ-

ences in the ZnO/metal interface arising from oxidation and doping effects during the sputtering of their top S/D electrodes. Consequently, it is expected that contact effects in ZnO TFTs are non-trivial. In the upcoming content, which is an extended description of the work published in Ref. [126], the characteristics of top-gated, staggered ZnO TFTs with gold (Au), ruthenium (Ru), and titanium tungsten (TiW) S/D contacts are compared to better understand the influence of the metal/ZnO interface on device performance.

4.1 Top-Gated Staggered ZnO TFT Device Fabrication

Top-gated ZnO TFTs were fabricated using the same procedure as the top-gated ALD ZnO source-gated thin film transistors (SGTFTs) discussed in the previous chapter with some minor alterations. A summary of the fabrication process is given in Fig. 4.1. Firstly, 10 nm of aluminium oxide (Al_2O_3) was blanket deposited on a thermal silicon oxide (SiO_2) covered Si wafer to modify the substrate's surface properties to aid with lift-off processes. The Al_2O_3 was grown with plasma enhanced atomic layer deposition (PEALD) at 100°C using trimethylaluminum (TMA) and oxygen plasma as the precursors for the Al and O respectively. Once again, the film thickness was monitored during deposition *in-situ* via a J. A. Woollam M-2000DI ellipsometer. Afterwards, the bottom S/D electrodes were deposited using sputtering and patterned with lift-off [Fig. 4.1(a-ii)]. In this study, Au (12 nm thick with an $\sim$ 3 nm thick chrome adhesion layer), TiW (15 nm thick), and Ru (15 nm thick) were employed for the S/D contacts. All three metallization schemes are relatively stable and thus suited for use as bottom contacts. Low temperature thermal ALD was then used to grow 20 nm of ZnO at 130°C as the active channel layer [Fig. 4.1(a-iii)]. For this study, there was no pre-deposition remote oxygen plasma (ROP) treatment before ZnO ALD growth as it increased the film's residual electron concentrations when comparing untreated and ROP-treated ZnO films (the latter were utilized in Chapter 3). More investigations are needed to determine the exact mechanism for this observation however. The ZnO was wet etched using ferric chloride ($FeCl_3$) solution following

photolithography to define the channel region [Fig. 4.1(a-iv)]. As mentioned in Section 2.2, aluminium (Al) and titanium (Ti) are common S/D metals for ZnO TFTs; however, they are less desirable as bottom electrodes because they are susceptible to the $FeCl_3$ wet etch. Afterwards, 10 nm of hafnium oxide (HfO_2) was grown by PEALD at 100°C and patterned using lift-off [Fig. 4.1(a-v)]. These set of devices did not require a blanket HfO_2 cap layer for protection (unlike the previously described top-gated SGTFTs) because the photoresist developer was switched to one that did not etch ZnO. Lastly, a Ti/Au gate metal stack (200 nm/50 nm thick respectively) was sputtered and patterned with lift-off to complete fabrication of the top-gated staggered ZnO TFT [Fig. 4.1(a-vi)]. Following device fabrication, a hot-plate anneal at 130°C for 30 min was performed to help improve device stability; in the study described in the following chapter, it was found that this hot-plate anneal may have contributed to reducing the Au contact's contact resistance as well. A three-dimensional (3-D) schematic diagram of the device is presented in Fig. 4.2. To evaluate the device's contact effects, the channel length (L) was varied from 2 to 32 μm, while the overlap between the gate-and-S/D electrodes (L_{ov}) and channel width (W) were held constant at 20 μm and 50 μm respectively. Multiple devices' electrical characteristics for each S/D metallization scheme were measured using the Keithley 4200 Semiconductor Characterization System (SCS) at room temperature. Furthermore, several materials studies on the metal/ZnO interface were performed to complement the electrical measurements.

4.2 Electrical Characterization of the Top-Gated Staggered ZnO TFTs

Typical $I-V$ characteristics for each S/D metal are shown in Fig. 4.3. Only transistors with a W/L ratio of 50 μm/8 μm are presented; but their characteristics are representative of all devices measured for this study (with L ranging from 2 to 32 μm). The drain-source current (I_{DS}) in all three TFTs' $I-V$ characteristics saturate before the drain-source voltage (V_{DS}) reached 4 V because of the high-κ HfO_2 gate insulator's high capacitance density. Corresponding transfer

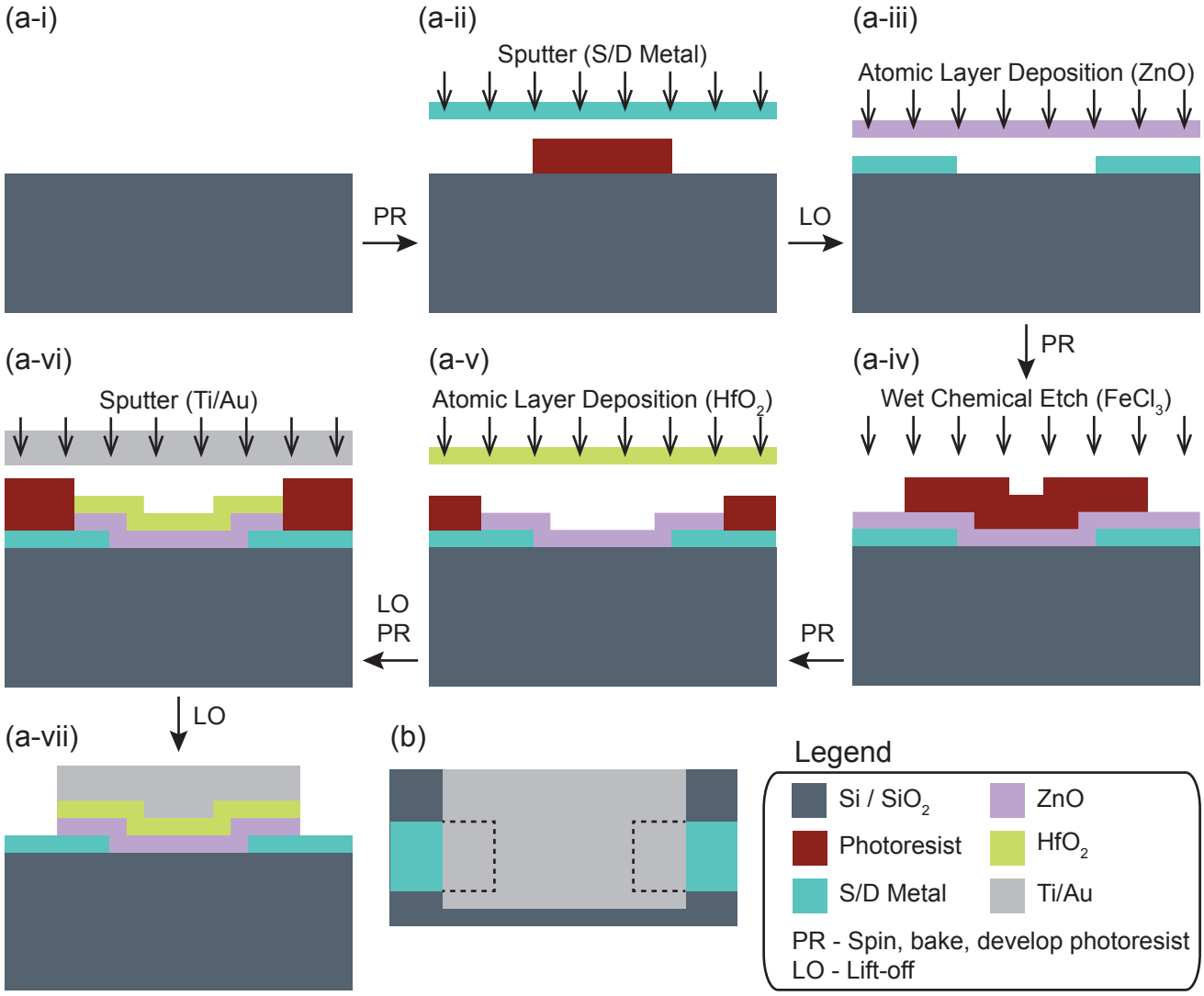

Figure 4.1: (a) Illustration of the top-gate staggered ZnO TFT's process flow. (b) Top view schematic of the top-gated ZnO TFT.

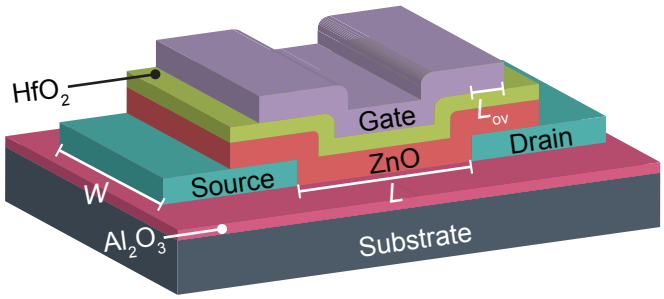

Figure 4.2: 3-D schematic of the bottom-contact, top-gate staggered ZnO TFT. Dimensions of interest (L, W, and L_{ov}) are labelled in white.

$I-V$ characteristics of the same devices at $V_{DS} = 0.1$ and 3 V are shown in Fig. 4.4. In Fig. 4.3 and Fig. 4.4, there are clear differences in the TFT performance from only changing the metallization at the S/D electrodes; i.e. the influence of L, W, and L_{ov}, for the range of values tested, were minimal in comparison. The TFT with Au S/D contacts displayed the highest on-state drain current (I_{on}), reaching up to $\sim$ 175 μA at a gate-source voltage (V_{GS}) of 2.5 V; but it suffers from high saturation output conductances (g_{ds}) and large off-state current (I_{off}) at zero V_{GS}, which are unattractive for most circuit applications e.g. amplifiers and switches. These are characteristics of a highly n-doped ZnO active channel. As mentioned in previous chapters, high n-type doping concentrations (N_D) are commonly found in ALD ZnO thin films and are believed to be caused by oxygen vacancies and zinc interstitials [12, 127]. The Ru/ZnO TFT exhibited much better off-state characteristics highlighted by a lower I_{off} and g_{ds} compared to the Au/ZnO device, while still producing an I_{on} of the order of 10^{-5} A. Differences in S/D contact resistance ($R_C W$) can cause variations in device behaviour; however, it is not possible to discern from just the $I-V$ characteristics alone if $R_C W$ was the sole cause. The TiW/ZnO TFT showed the lowest I_{on} of the three devices and was the only one to exhibit current crowding in the output characteristics' linear regime at high V_{GS}. These results are indications of Schottky S/D contacts where the conductance of the accumulation channel below the ZnO/HfO_2 interface is relatively unaffected by V_{GS} because of the large voltage drop across the Schottky barrier [123, 124, 98]. This agrees with the Schottky characteris-

tics displayed by the TiW/ZnO source contact in the top-gated ZnO SGTFTs presented in Chapters 2 and 4. It is expected that the Schottky TiW contacts limited carrier injection at the S/D leading to non-linear $I-V$ characteristics.

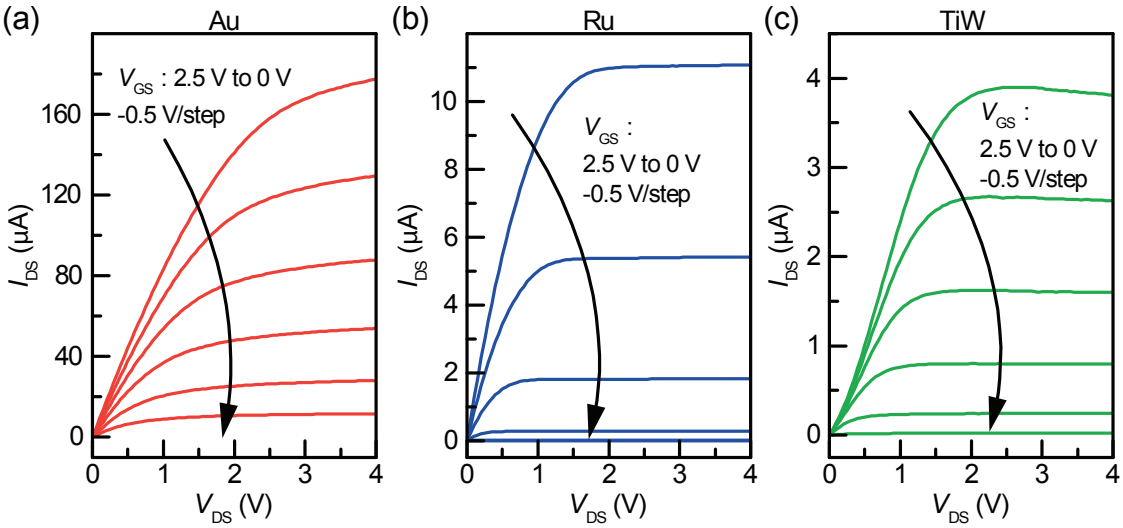

Figure 4.3: Output characteristics (I_{DS}-V_{DS}) of top-gate, bottom contact ZnO TFTs with (a) Au, (b) Ru, and (c) TiW S/D metal electrodes. V_{GS} varies from 0 to 2.5 V in 0.5 V steps. All three TFTs have the same W/L of 50 μm/8 μm.

Table 4.1: Summary of the Electrical Properties of Top Gated ZnO TFTs

S/D Metal	V_{th} [V]	μ_{sat} [cm^{2}V^{-1}s^{-1}]	SS [mV/dec]	$I_{on/off}$ [A/A]	N_D [cm^{-3}]
Au	-0.82	5.17	824	920	1×10^{19}
Ru	0.92	1.40	89	7.1×10^8	7×10^{17}
TiW	-0.16	0.22	198	4.5×10^7	4×10^{18}

The performance metrics were calculated from the transfer characteristics at $V_{DS} = 3$ V in Fig. 4.4 and the C_{GS}-V_{GS} characteristics in Fig. 4.5.

The TFT's turn-on voltage (V_{on}) noticeably varied for each S/D metal, as demonstrated by Fig. 4.4, with the Au/ZnO TFT showing the most negative value (< -1.5 V as current pinch-off was not observed). Conversely, the Ru/ZnO TFT's V_{on} approached 0 V, making it very attractive for low-power switching applications and high efficiency amplifiers. Surprisingly, TiW S/D contacts did not

show the lowest I_{off} even with the reduced carrier injection from the TiW/ZnO Schottky barrier. Based on the material studies presented in Section 4.3, this was because of the Ru/ZnO interface's smaller leakage currents. A summary of the important performance metrics extracted from each TFT's electrical measurements is given in Table 4.1. Accordingly, the Au/ZnO TFT exhibited poor switching potential as highlighted by its large subthreshold swing (SS) and low current on-to-off ratio ($I_{on/off}$), despite showing the highest I_{on}. In contrast, the Ru/ZnO TFT produced the best switching performance, as exemplified by its positive V_{th}, high $I_{on/off}$ of 7.1×10^8, and extremely low SS of 89 mV/decade, while demonstrating a moderately high saturation mobility (μ_{sat}) of 1.4 $\mathrm{cm^2V^{-1}s^{-1}}$. These excellent characteristics are indications of low interface defects and a moderate channel N_D [128]. In addition, considering that the Ru/ZnO device's I_{on} was higher than that of the TiW/ZnO TFT's, and its $I-V$ characteristics remained linear at low V_{DS}, the Ru/ZnO interface was likely near-ohmic. Note that the classical Schottky-Mott model (described in Section 2.1) unfortunately cannot confirm the nature of the metal/ZnO interface due to the contact barrier's sensitivity to surface contaminants and defects [84].

An approximation of the ZnO N_D was calculated by biasing the ZnO TFT as a two-terminal metal-oxide-semiconductor capacitor (MOSCAP) from the gate-to-source and then measuring its capacitance (the drain contact is floating during the measurement). The gate-to-source capacitance (C_{GS}) plotted versus V_{GS} for the previously discussed ZnO TFTs is shown in Fig. 4.5. C_{GS} was clearly heavily influenced by the choice of metal used in the S/D electrodes, especially during the on-state. When a MOSCAP is biased in depletion (i.e. $V_{GS} < 0$ V), N_D is inversely related to the slope of C_{GS}^{-2} versus V_{GS} according to the following equation [129],

$$N_D = 2\left[q\varepsilon_S A^2 \left(\frac{\partial {C_{GS}}^2}{\partial V_{GS}}\right)\right]^{-1} \tag{4.1}$$

where q is the electron charge (1.6×10^{-19} C), ε_S is the permittivity of ZnO ($8.5 \times 8.85 \times 10^{-12}$ $\mathrm{F{\cdot}m^{-1}}$), and A is the effective area, which was estimated to be the source-to-gate overlap area (20×50 $\mu\mathrm{m}^2$) in this case as $\partial C_{GS}^{-2}/\partial V_{GS}$ was relatively unaffected by L during depletion. Each device's approximate N_D is

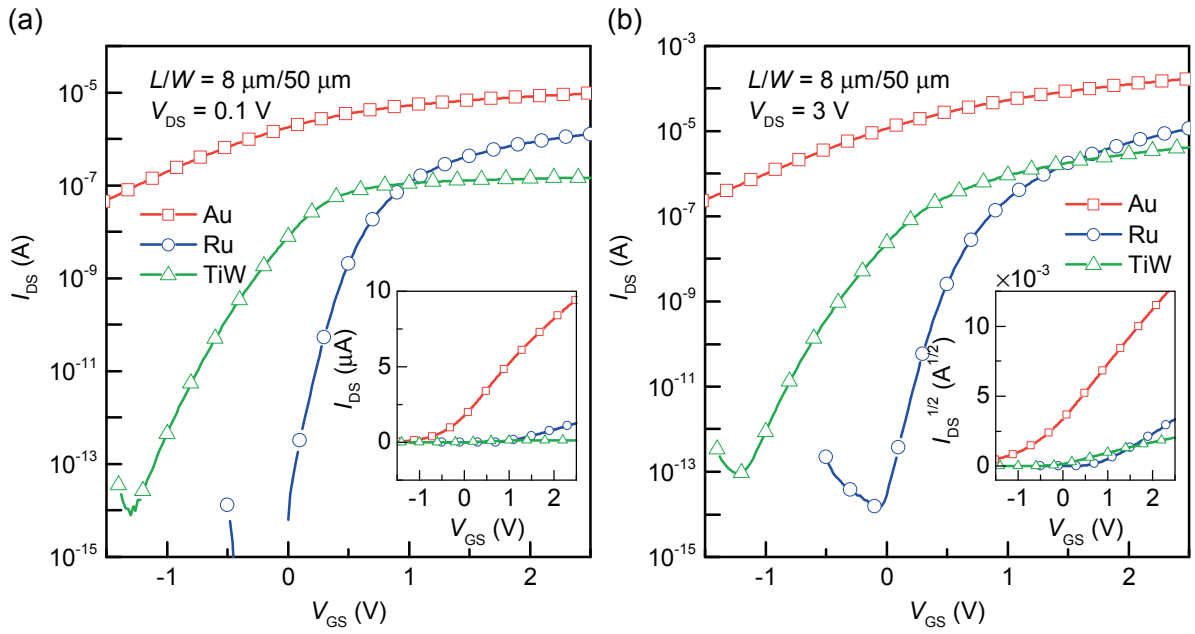

Figure 4.4: Transfer characteristics (I_{DS}-V_{GS}) in semi-log scale at a constant V_{DS} of (a) 0.1 V and (b) 3 V for top-gated ZnO TFTs with Au, Ru, and TiW S/D contacts. The inset in (a) depicts the same characteristics in linear scale; whereas the inset in (b) contains the square root of I_{DS} plotted as a function of V_{GS}, which was used to calculate μ_{sat} and V_{th}. All three TFTs have the same W/L of 50 μm/8 μm.

also given in Table 4.1. As alluded by the $I-V$ characteristics, the Au/ZnO TFT possessed the highest N_D ($\sim 1 \times 10^{19}$ cm^{-3}). These relatively high electron concentrations are likely why Schottky characteristics were not observed in this study's Au/ZnO TFTs (unlike the rectifying ZnO/Au contact employed for the bottom-gated ZnO SGTFTs in Chapter 2). Growth temperature is the main factor that determines the N_D for ALD ZnO films [116, 130]. However, considering that all devices were processed simultaneously, the differences in N_D and the C_{GS}-V_{GS} characteristics should be narrowed down to just contact effects. After analysing X-ray photoelectron spectroscopy (XPS) measurements of the metal/ZnO interfaces, which are presented following the electrical measurements in Section 4.3, Ru presumably induced a ZnO film or metal/ZnO interface with fewer donor species therefore lowering N_D. Similarly, the different on-state C_{GS} values in Fig. 4.5 can be attributed to contact effects. The Ru/ZnO TFT's reduced on-state C_{GS} compared to the Au/ZnO TFT's is explained by a series capacitance at the source on account of non-negligible depletion charge at the S/D contacts from its lower N_D. In that regard, for the TiW/ZnO TFT, the depletion layer from the source Schottky barrier caused an even larger reduction in the on-state C_{GS}. In summary, both $I-V$ and C_{GS}-V_{GS} characteristics demonstrate that contact effects were present and clearly affected TFT performance.

4.2.1 Quantifying the Source/Drain (S/D) Contact Resistance in Top Gated ZnO TFTs

To further quantify the $R_C W$ of each S/D metal, the conventional transfer length method (TLM) technique was applied using the output characteristics of at least four different TFTs for each S/D metal [131]. Besides the TFTs presented in Fig. 4.3, devices with L ranging from 2 to 32 μm for each S/D electrode, all with the same W and L_{ov}, were tested. In the linear regime at low V_{DS}, the total TFT on-resistance can be approximated using the following equation:

$$R_{on}W = W\left(\frac{\partial V_{DS}}{\partial I_{DS}}\right) \approx W(r_{ch}L + R_S + R_D) \tag{4.2}$$

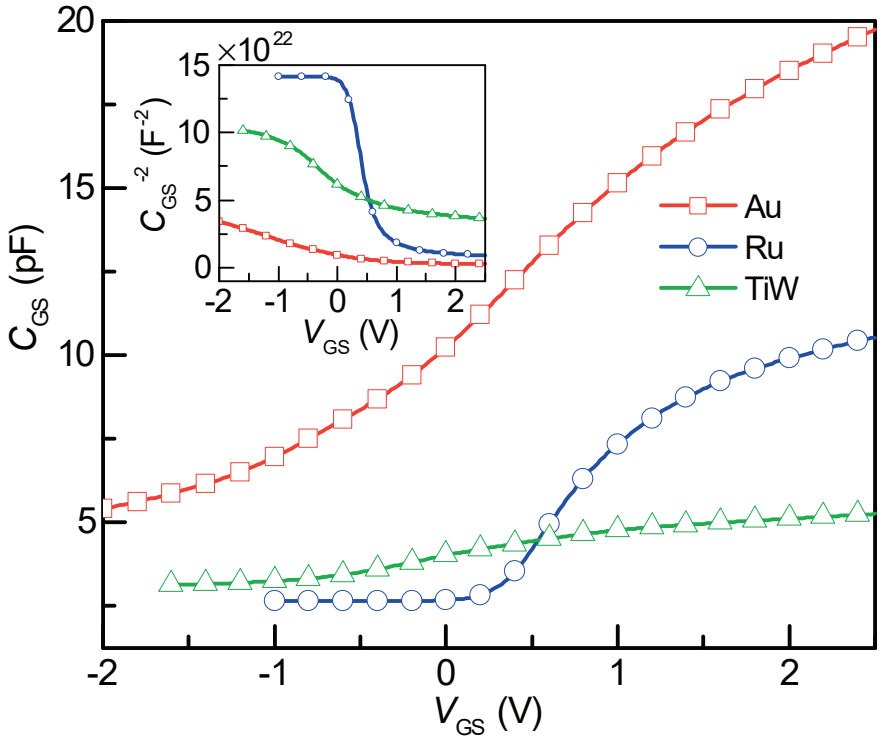

Figure 4.5: C_{GS} as a function of V_{GS} (measured at 1 MHz and $V_{DS} = 0$ V) for top-gated ZnO TFTs utilizing Au, Ru, and TiW S/D contacts. The drain contact was floating during measurement. Inset: Reciprocal of C_{GS} squared versus V_{GS}, which was used to determine ZnO's N_D.

where $R_{on}W$ is the W-normalized on-resistance, r_{ch} is the W-normalized channel resistance per unit length, and $(R_S + R_D)W$ is the sum of the contact resistances at the S/D. As the TFT layout is symmetrical, the contact resistance at each electrode is approximated by $R_S W = R_D W \approx R_C W$ (please note that the definition of $R_C W$ in Equation 4.2 is different from the notation used in the following chapter). The calculated $R_{on}W$ for each S/D metal is shown in Fig. 4.6. Both the Au and Ru TFTs scale relatively linearly with L implying good ohmic behaviour of the S/D contacts. Whereas, the ZnO TFTs with TiW S/D contacts were contact-limited and as a result, L barely had an influence on the TFT characteristics. By fitting $R_{on}W$ versus L to a straight line at each V_{GS} according to Equation 4.2, each metal's r_{ch} and $R_C W$ was extracted from the slope and intercept respectively; the results are plotted in Fig. 4.7 in semi-log scale for easier readability. Both $R_C W$ and r_{ch} decreased as V_{GS} increased. Increasing V_{GS} raises the carrier concentration in the channel while also reducing the effective height of the contact barriers, which both contribute to lowering R_{on}. At high V_{GS} when the devices were in their on-state, the $R_C W$ of the TiW contacts remained large, which provides further evidence of TiW/ZnO Schottky barriers being present. Owing to these large $R_C W$ values, there was little L dependence in the TiW/ZnO TFTs' $I - V$ characteristics as most of the applied voltage was dropped at the contacts rather than in the channel [123, 98]. Consequently, the effective voltage in the channel (i.e. V_{DS} and V_{GS}) was much lower than the applied voltage because of large $R_C W$, leading to diminished device performance compared to the other devices that displayed lower $R_C W$. There was also noticeable variation in r_{ch}, indicating that the characteristics of the ZnO channel were also affected by the S/D metallization. Evidence for this is provided by the materials studies presented next.

4.3 Material Characterization of the S/D Metal/ZnO Interface

The electrical characterization of the ZnO TFTs provided strong evidence of highly influential contact effects determined by the metallization at the S/D.

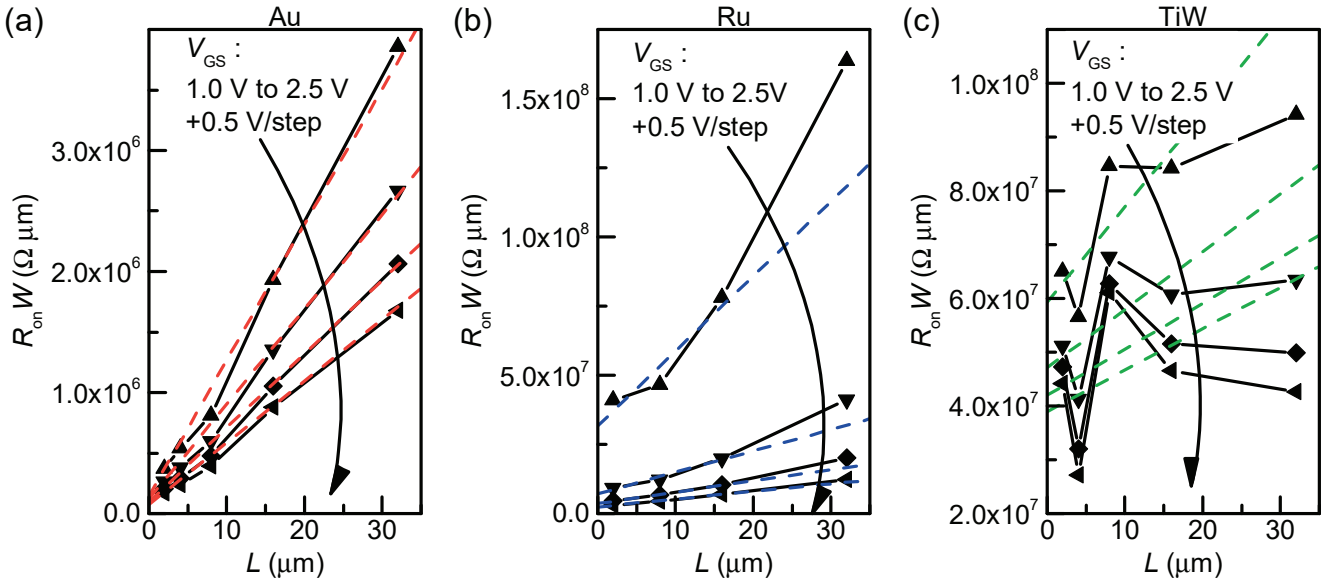

Figure 4.6: On-resistance ($R_{on}W$) dependence on L for a set of top-gated ZnO TFTs with (a) Au, (b) Ru, and (c) TiW S/D contacts with V_{GS} varying from 1 V to 2.5 V in 0.5 V steps (from top to bottom). The dashed lines are the linear regression fits of $R_{on}W$ to L at each V_{GS} using the TLM. ZnO TFTs with TiW S/D contacts were clearly contact-limited as shown by the poor linearity of $R_{on}W$ with L compared to the other devices.

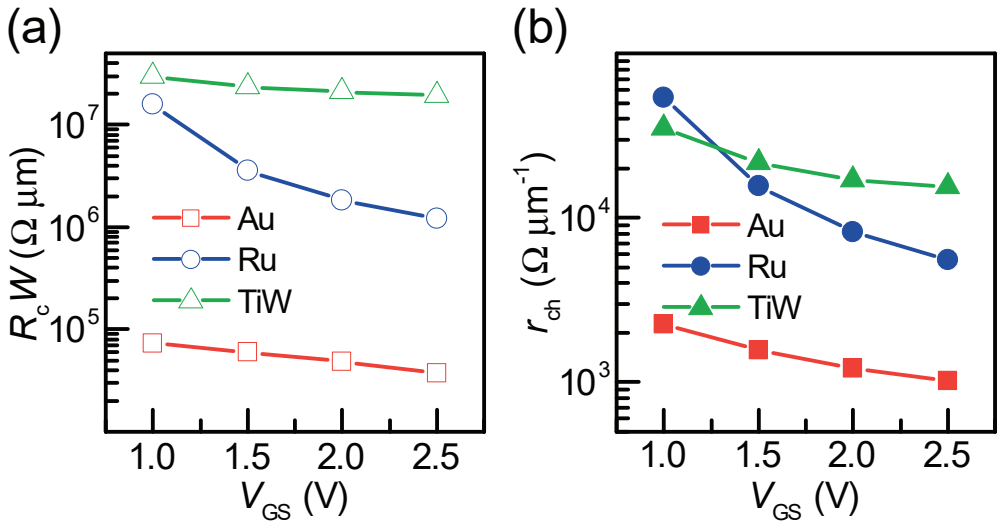

Figure 4.7: (a) Contact resistance ($R_C W$) and (b) intrinsic channel resistance per unit length (r_{ch}) plotted as a function of V_{GS} in semi-log scale extracted by the TLM for ZnO TFTs with Au, Ru, and TiW bottom S/D contacts.

Considering that all devices were fabricated under the same conditions, the difference in TFT performance can be almost entirely attributed to the properties of the S/D metal contact/ZnO channel interface. Thus, to delve deeper into the nature of the metal/ZnO interface, several material studies were performed. Fig. 4.8 contains a plot of offset scans from grazing incidence X-ray diffraction (XRD) measurements of ZnO thin films (30 nm thick) grown on various substrates. Like the TFTs, these samples were also subjected to a hot-plate anneal at 130°C for 30 min. The incident glancing angle was 0.5 degrees with a copper K-alpha radiation (wavelength = 0.15405 nm) source. Diffraction peaks produced from both the ZnO film and substrate were detected; nonetheless, the peaks originating from the wurtzite ZnO crystal structure are indexed and labelled on the plot in Fig. 4.8. Excluding the Au/ZnO sample, the XRD patterns show multiple peaks of similar intensity, implying that the ZnO films were polycrystalline - where no single crystal orientation was dominant. This agrees well with other ALD ZnO films grown at low temperatures [116, 132]. However, for the Au/ZnO sample, a single dominant diffraction peak corresponding to the (103) crystal orientation ($2\theta \sim 63°$) was uniquely exhibited, which explains why the electri-

cal characteristics of the Au/ZnO TFTs were so different. ZnO thin films are energetically favoured to grow along the (002) orientation where the c-axis of the wurtzite structure is oriented perpendicular to the substrate [116]. Previous works, however, have established that the preferential orientation of ALD ZnO can be controlled by manipulating the kinetics of the atoms on the substrate during growth, e.g. by adjusting the deposition temperature and gas purging times [116, 133]. From how the (103) ZnO peak partially overlapped with the (220) Au peak (at $2\theta \sim 65°$) from the substrate, the relatively inert Au likely influenced the surface energy in a manner that promoted growth in the (103) direction. It is speculated that there were comparatively less oxygen-terminated reaction sites available on the Au surface for the Zn precursor (DEZn) to bind to during initial growth; this would affect the nucleation of the ZnO film that could propagate into the Au/ZnO's different crystal structure. Furthermore, in the experiments described in the following chapter, it was discovered that the Au/ZnO interface's conductivity clearly increased after a post-processing hot-plate anneal at 150°C for 60 min. Accordingly, the hot-plate anneal used for this experiment (130°C for 30 min) could have also been responsible for changing the ZnO crystal structure from polycrystalline to predominately (103)-orientated. However, presently there is no quantifiable information on the exact nature of the Au/ZnO interface.

Fig. 4.9 contains images of the ZnO surface from the same metal/ZnO samples acquired with atomic force microscopy (AFM) in tapping mode. The surface topography was relatively disordered for all three films; but the polycrystalline Ru/ZnO and TiW/ZnO films showed higher surface roughness in comparison with the (103)-dominated Au/ZnO film. As measured by AFM, the root mean squared roughness (R_q) of the Ru/ZnO and TiW/ZnO films were 1.19 and 1.07 nm respectively; whereas the Au/ZnO film had a lower R_q of 0.66 nm. In light of the results from both XRD and AFM, the nature of the Au/ZnO film was markedly different from the rest and likely the main reason for the Au/ZnO TFTs' unique electrical properties.

To investigate the chemistry of the metal/ZnO interface in detail, XPS studies were performed at room temperature on a series of 5 nm thick ZnO films grown on each metal of interest. High resolution XPS spectra detected from the metal/ZnO interfaces are shown in Fig. 4.10. The XPS spectra's binding energy

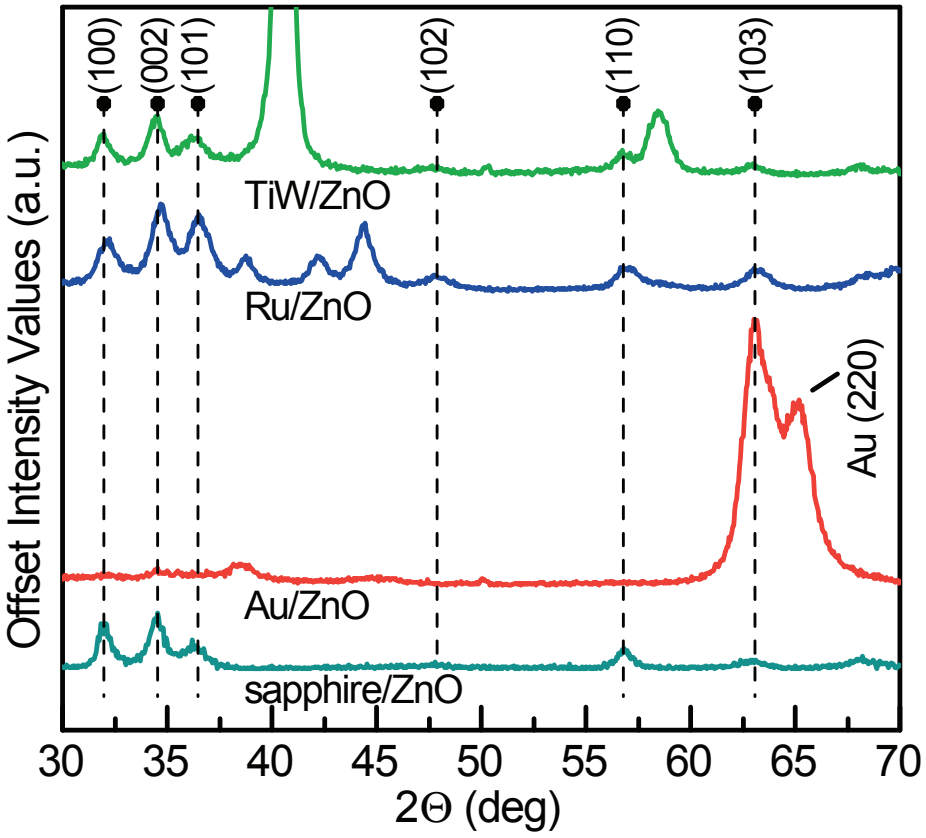

Figure 4.8: Offset grazing incidence XRD patterns of ALD ZnO thin films grown on various substrates. The diffraction peaks originating from wurtzite ZnO are indexed; unlabelled diffraction peaks correspond to peaks from each respective substrate. For the Au/ZnO sample, the Au (220) peak is overlapping with the (103) ZnO peak at $\sim 63°$.

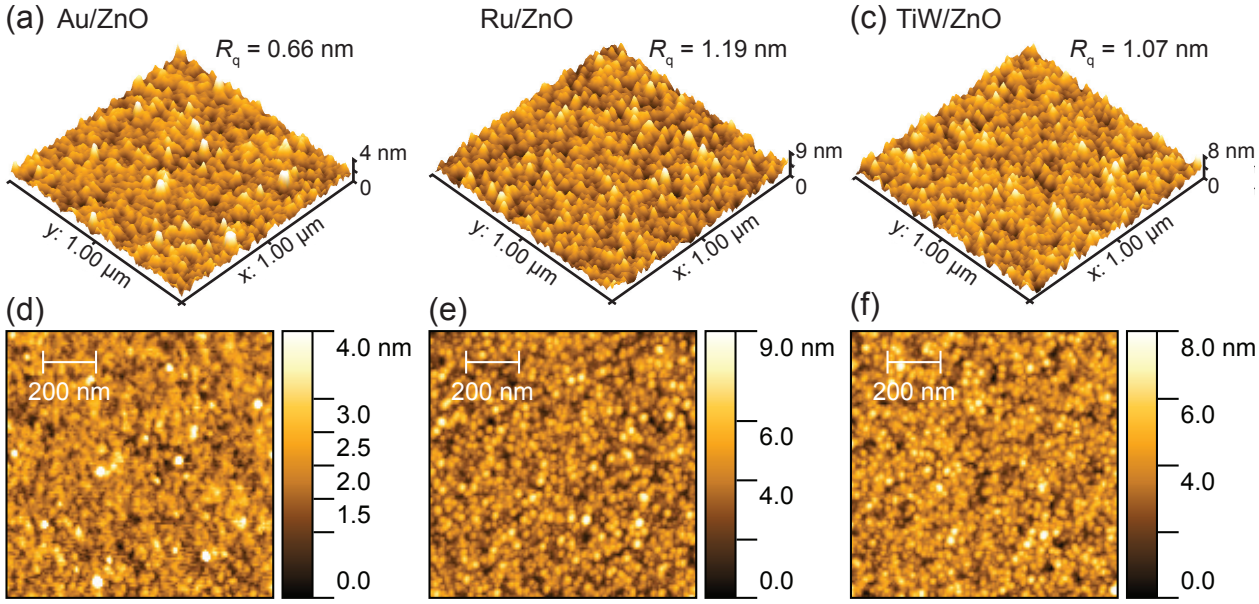

Figure 4.9: Surface topography of ZnO grown on (a,d) Au, (b,e) Ru, and (c,f) TiW as measured by AFM in tapping mode. The calculated root mean squared roughness values (R_q) are labelled above.

(BE) was calibrated to the carbon 1s core level (at 284.8 eV). For the Au/ZnO and Ru/ZnO samples, there was relatively low oxidation at the metal/ZnO interface by analysing the shape and binding energies of the core level peaks [41]. Whereas, tungsten(VI) oxide (WO_3) peaks were detected from the TiW/ZnO sample revealing that TiW formed a native oxide from reacting with oxygen. The intensity of the Ti core-level peaks was too weak to confirm if Ti oxidation states were also present. Taking into account the high R_CW and current crowding exhibited by the TiW/ZnO TFTs, the insulating properties of WO_3 likely increased the energy barrier at the TiW/ZnO interface, thereby resulting in poor current injection and Schottky behaviour [134]. Thus, a clean metal/ZnO interface without an oxidized interlayer should assist with realising low R_CW S/D contacts, which agrees with the findings from previous contact studies for ZnO [125].

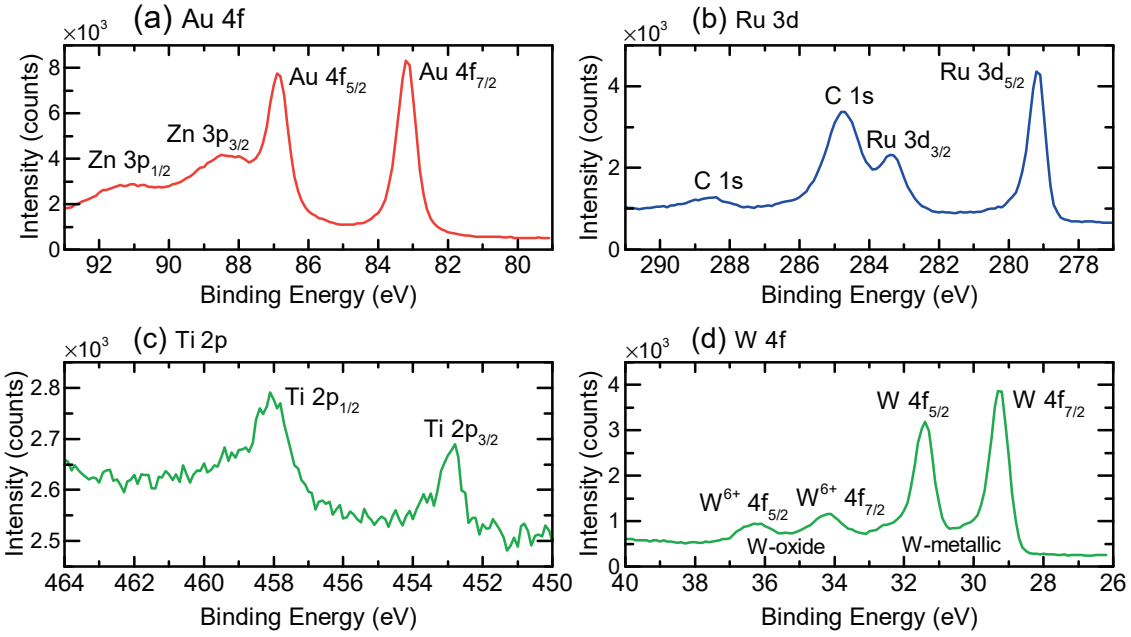

Figure 4.10: Metal core-level XPS spectra of the metal/ZnO interface from (a) Au/ZnO, (b) Ru/ZnO, and (c,d) TiW/ZnO.

Fig. 4.11 shows the core O 1s XPS spectra obtained from the same samples in Fig. 4.10. In ZnO, the O 1s peak can usually be de-convoluted into two

Gaussian components - one main peak characterized at a BE of $\sim$ 530 eV and another smaller shoulder peak characterized at a BE of $\sim$ 531.5 eV. The taller peak at 530 eV is associated with O^{2-} species from the fully stoichiometric ZnO lattice; whereas the smaller peak at 531.5 eV is typically attributed to Zn-OH components or O_2^{2-} defects [135, 90]. In this work, it is presumed that hydroxide species (OH^-) were responsible for the high BE component (at 531.5 eV) because of the thermal ALD growth mechanism. During the initial growth stages, a large concentration of Zn-OH reaction sites is present during the first few monolayers from the use of water as the oxidizing agent [136, 137]. As the ZnO film continues to grow in thickness however, the Zn-OH interactions begin to decrease. This was determined by comparing XPS measurements of 20 nm thick thermal ALD-grown ZnO films (deposited at 50°C, 150°C, and 250°C), which are reported in Ref. [138], with the spectra in Fig. 4.11. The ratio of the Zn-OH to Zn-O peaks in the bulk ZnO films' O 1s spectra was much smaller for all temperatures compared to the localized metal/ZnO interfaces' O 1s spectra displayed in Fig. 4.11. Thus, the OH^- reactions sites are prominent only during the beginning of the thermal ALD deposition process. In Fig. 4.11, the area of the fully oxidized O^{2-} peak was relatively consistent between samples; whereas the area of the OH^- peak varied depending on the underlying metal substrate. TiW/ZnO had the largest OH^- peak, indicating that the oxidized surface of TiW was more easily hydrolysed compared to the other non-oxidized metal surfaces. This is a likely reason for the higher off-state current (I_{off}), SS, and N_D observed in the TiW/ZnO TFTs compared with the Ru/ZnO TFTs, considering that OH^- acts as a surface donor in ZnO [139, 90, 140]. The higher OH^- concentrations at the TiW/ZnO interface would thin the contact barrier and thus increase the TiW/ZnO TFTs' leakage current or I_{off} [130, 141]. As previously mentioned, the TiW/ZnO TFTs' I_{on} were lower than that of the Ru/ZnO TFTs' despite the higher observed N_D because of the TiW/ZnO Schottky barrier, which restricted carrier accumulation in the channel. Although the smallest OH^- peak was recorded for the Au/ZnO sample, the N_D calculated from the Au/ZnO TFT's C_{GS}-V_{GS} characteristics was the highest, implying that the (103)-oriented ZnO film induced by the Au contacts (rather than OH^- dopants at the Au/ZnO interface) was mainly responsible for the n-type dopants in these devices. More insight into the physical nature of the

(103) ZnO is needed to determine the source of these higher carrier concentrations.

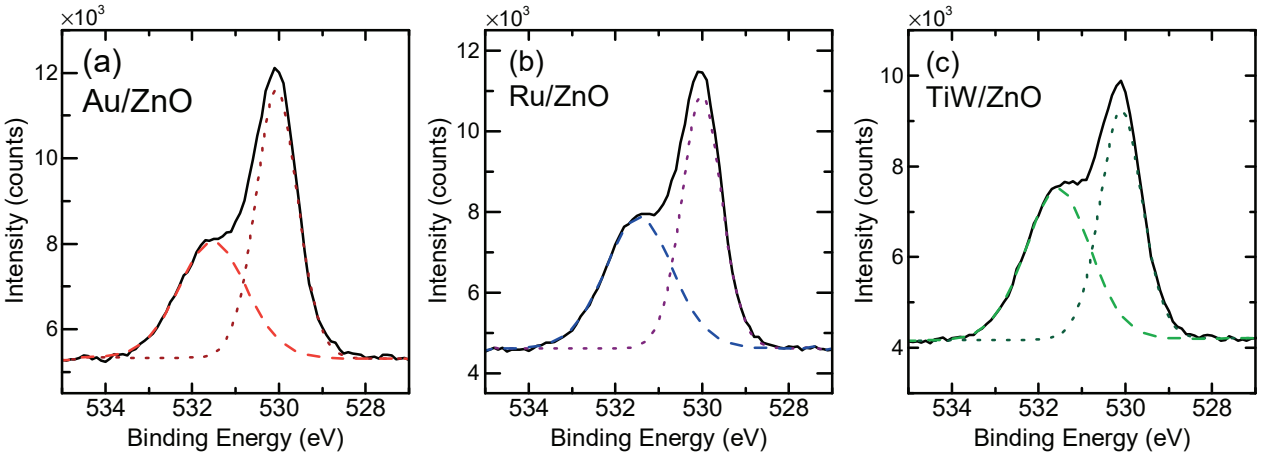

Figure 4.11: High resolution XPS O 1s spectra of the metal/ZnO interface from (a) Au/ZnO, (b) Ru/ZnO, and (c) TiW/ZnO. The O 1s peak is de-convoluted into a taller main peak (dotted line) centred at $\sim$ 530 eV and a smaller shoulder peak (dashed line) centred at $\sim$ 531.5 eV using Gaussian components.

4.4 Summary of the Top-gated Staggered ZnO TFTs with Varying S/D Metal Contacts

The contact effects observed in the top-gated ZnO TFTs from utilizing Au, Ru, and TiW bottom S/D metal electrodes predominantly ensued from differences in the metal/ZnO interface during the thermal ALD growth of ZnO. The chemistry of the metal/ZnO interface and, for Au contacts especially, the nature of the ZnO film itself were both influenced by the S/D metal. A summary of each S/D metal's contact effects is tabulated in Table 4.2. From the results of the electrical measurements, Schottky barrier contacts are undesirable for high device performance as they have an effectively high $R_C W$, consequently lowering the TFT's speed and switching capabilities. The source Schottky barrier's benefits (e.g. lower saturation voltages and lower I_{off}) were not observed in the TiW/ZnO TFTs because the gate was able to fully deplete the lower doped ZnO channel (compared to the ZnO film employed in the previous chapter); hence, the extra

depletion at the source from the reverse-biased Schottky barrier (intended for improving current control in source-gated transistors) was not needed. Based on the results of the material studies, a non-oxidized metal/ZnO interface helped reduce the concentration of OH^- interfacial donors and improve the TFT's I_{on} through better interface energetics for carrier injection. Although Au contacts showed the lowest concentration of adsorbed OH^-, the expected performance improvement was undermined by the high N_D of the (103) orientation-dominated ZnO that the Au surface exclusively promoted. Correlating the properties of the metal/ZnO interface with TFT performance, ohmic S/D contacts in conjunction with moderate channel doping concentrations ($\sim 10^{17}$ cm^{-3}) provided the balance between high current output and good switching performance as exemplified by the Ru/ZnO TFTs. A thorough understanding of the interactions between the S/D contacts, ZnO active channel, and TFT electrical performance will greatly contribute toward building a practical high performance ZnO-based transistor.

Table 4.2: Summary of the Contact Effects in Top-gated ZnO TFTs

S/D Metal	Summary
Au	• Exclusively induced a highly doped (103)-oriented ZnO film that degraded the Au/ZnO TFTs' switching performance and gate control • Based on XPS measurements, the high residual electron concentrations were not caused by OH^- interface dopants
Ru	• Displayed te best overall device performance featuring excellent switching characteristics and a moderately high mobility • Good device behaviour presumably originated from an oxidation-free Ru/ZnO interface that inhibited the absorption of OH^-.
TiW	• Formed Schottky barriers with ZnO restricting the TiW/ZnO TFTs' on-state performance • Oxidation of TiW at the metal/ZnO interface was likely the cause for Schottky barrier formation and the adsorption of OH^- interface dopants

Chapter 5

Modelling of Top-gated Zinc Oxide Thin Film Transistors

Zinc oxide (ZnO) thin film transistors (TFTs) have demonstrated the potential to disrupt markets requiring large-area circuitry due to their moderately high device mobilities, optical transparency, good stability in visible light, and compatibility with low temperature processing [139, 1]. However, before integrated circuits based on ZnO can be commercially feasible, a compact model that can reproduce ZnO TFT operation is necessary. With an accurate ZnO TFT model, conventional circuit design and simulation practices (e.g. SPICE) can be easily exploited for designing practical ZnO-based circuits. ZnO TFTs reported in literature exhibit a large range of device characteristics because of differences in materials, fabrication procedures, and device geometries. If all this variability can be modelled by a compact model, the design challenges with implementing ZnO TFTs in electronic circuits will be significantly reduced.

As seen by the TFT characteristics presented in the previous chapters, a wide range of device characteristics can be attained by only altering the nature of the source-and-drain (S/D) contacts. For instance, when a Schottky metal was utilized as the source electrode, the TFT behaviour changed significantly resulting in so-called source-gated thin film transistor (SGTFT) characteristics [99, 98]. Additionally, adding an drain-offset region between the gate-and-drain can enable drive voltages beyond the operating range that conventional staggered TFTs

with symmetrical gate-and-S/D overlaps are capable of [142, 118, 112]. Thus, a universal compact model that can consider all these different behaviours and their current-voltage ($I-V$) characteristics is extremely attractive for circuit design and can be a valuable tool for tailoring a ZnO TFT's electrical characteristics for specific purposes. In this chapter, conventional top-gate staggered ZnO TFTs with symmetrical bottom S/D contacts are compared with identical TFTs but with asymmetrical S/D contacts wherein the drain electrode is changed to gold (Au) (which demonstrated excellent ohmic contact properties from the devices reported in Chapter 4). Moreover, the influence of the drain-offset structure is studied and also compared with the conventional staggered TFT. To help evaluate all these different device architectures, a direct current (DC) compact circuit model originally developed by Marinov *et al.* is adopted to model experimental measurements of various top-gated ZnO TFTs [143]. The resulting parameters from device modelling are then interpreted for determining guidelines on how to engineer ZnO TFTs with precise attributes, e.g. higher device mobility, larger breakdown voltages (V_{BD}), and better switching characteristics, through modifying the S/D contact metallization and gate-to-drain structure.

5.1 Top-gated Zinc Oxide TFT Fabrication

The ZnO TFTs used in this work can be separated into three classes based on the S/D metallization and gate-to-drain structure: (1) symmetrical S/D-overlapped (or conventional staggered) TFTs with equal overlaps between the gate-and-S/D electrodes and the same metal contacts at the S/D, (2) asymmetrical S/D-overlapped TFTs with equal overlaps between the gate-and-S/D electrodes but utilizing different metal contacts for the S/D, and (3) asymmetrical drain-offset TFTs with a gate-to-source overlap, a drain-offset between the gate-and-drain, and different metal contacts for the S/D. For this thesis, only one device for each transistor architecture at one particular set of dimensions is presented. However, the results are consistent and typical characteristics of measurements over several devices (> 3) with the same dimensions or with only the channel length (L) being manipulated. Only a 10 μm overlap between the gate-and-S/D electrodes (L_{ov}), where the channel width-to-length ratio (W/L) was equal to 50 μm/32

μm, was tested to directly compare all the devices. $L = 32$ μm was chosen to allow for a wider range of gate-to-drain distance (L_{GD}) values in the drain-offset devices. For this experiment, the TFT's source electrode was either ruthenium (Ru), Au, or copper (Cu); whereas, the drain electrode was either Ru or Au. All TFTs were fabricated concurrently with the following process. Firstly, 50 nm of plasma-enhanced chemical vapour deposition (PECVD) silicon nitride (SiN) was blanket deposited on an isolated silicon (Si)/thermal silicon oxide (SiO_2) wafer to aid with the lift-off of photoresist. Because some devices required two different metals for the S/D, the fabrication process needed two separate lift-off steps for the bottom electrodes, one for each. The first electrode, i.e. Ru (15 nm thick) or Cu (12 nm thick on a $\sim$ 3 nm thick titanium adhesion layer), was deposited by sputtering and then patterned via lift-off to serve as both the S/D in the symmetrical devices and only the source in the asymmetrical devices. Afterwards, Au (12 nm thick on a $\sim$ 3 nm thick chrome adhesion layer) was deposited via electron beam evaporation and patterned with lift-off to serve as the asymmetrical devices' drain. Symmetrical S/D-overlapped TFTs were also fabricated using the Au metal contacts formed during this step; but these devices were not modelled and instead were employed to evaluate the Au/ZnO contact properties. Following metallization of the bottom electrodes, 20 nm of ZnO was grown as the active channel layer using thermal atomic layer deposition (ALD) at 130°C without any pre-growth plasma treatments. The channel was then wet etched using diluted phosphoric acid following photolithography. Next, 10 nm of hafnium oxide (HfO_2) was grown using plasma enhanced atomic layer deposition (PEALD) at 100°C as the gate insulator layer and patterned with lift-off as well. Lastly, 80 nm of Ru was sputtered and patterned with lift-off to form the top-gate electrode. A post-processing anneal was performed subsequently on a hot plate at $\sim$ 150°C for 60 min in ambient atmosphere. The anneal helped improve device stability while noticeably reducing the bottom Au contact's resistivity, indicating that some entity in the Au/ZnO interface was thermally active; however, further studies are needed to determine the exact mechanism by which the hot-plate anneal reduced the Au's contact resistance. Compared to the fabrication procedures for the previous chapter's staggered ALD-ZnO TFTs, the only major difference in this process was adding an extra lithography step during S/D metallization

to separate the deposition of the bottom S/D electrodes into two steps (for the asymmetrical devices). Schematics of the three main classifications of devices utilized for this study are shown in Fig. 5.1(a), (b), and (c). The TFT's electrical characteristics were all measured using the Keithley 4200 Semiconductor Characterization System (SCS) at room temperature.

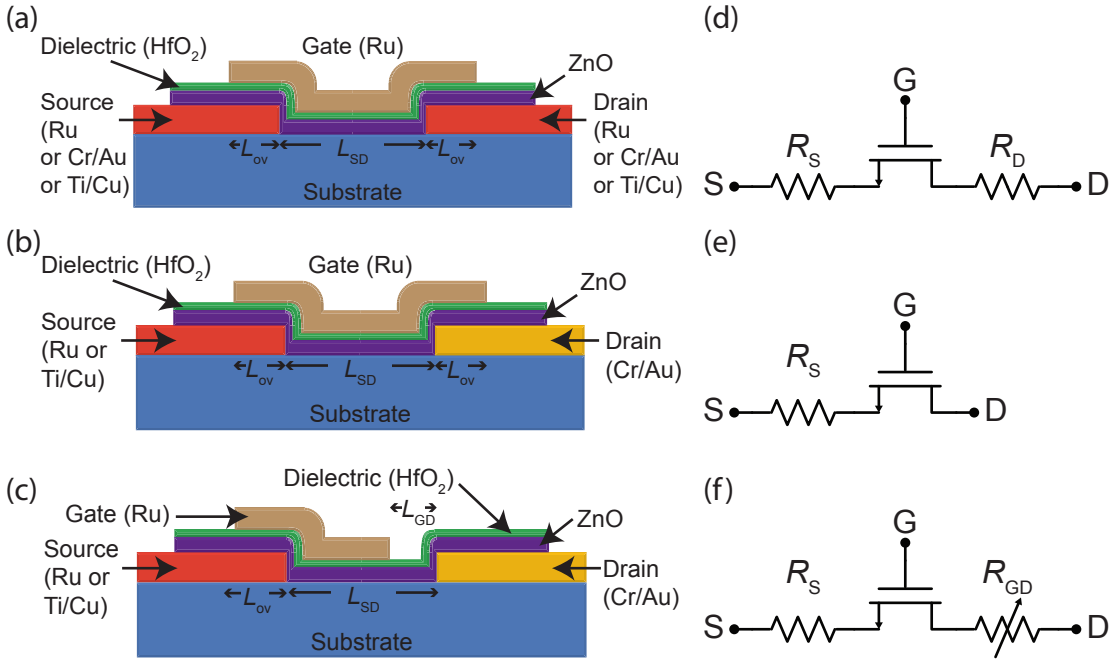

Figure 5.1: Schematic cross-sections of (a) a symmetrical S/D-overlapped (staggered) (b) an asymmetrical S/D-overlapped, and (c) an asymmetrical drain-offset top-gate ZnO TFT. Dimensions of interest (L, L_{ov}, and L_{GD}) are labelled when applicable. Equivalent circuit models for the TFT structures in (a), (b), and (c) are displayed on the right in (d), (e), and (f) respectively.

5.2 ZnO TFT Compact Model

A transistor compact model is encompassed of a system of equations and parameters that can accurately reproduce a device's $I-V$ characteristics without needing to consider its inner workings or physics. Carrier transport in ZnO TFTs is still commonly analysed using the classical DC model for metal-oxide-semiconductor

field effect transistors (MOSFETs), which relates the transistor's drain-source current (I_{DS}) to its drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}),

$$I_{DS} = \frac{W}{L}\mu C_{ox} \begin{cases} (V_{GS} - V_{th} - \frac{1}{2}V_{DS})V_{DS} \text{ for } V_{DS} < (V_{GS} - V_{th}) \\ \frac{1}{2}(V_{GS} - V_{th})^2 \text{ for } V_{DS} > (V_{GS} - V_{th}) \end{cases} \tag{5.1}$$

where W/L is the transistor channel width-to-length ratio, μ is the device mobility, C_{ox} is the gate insulator capacitance per unit area, V_{th} is the threshold voltage, and $(V_{GS} - V_{th})$ is the transistor's saturation voltage ($V_{DS,sat}$). Although this model is suitable for calculating μ and V_{th} in certain regimes of the TFT operation, it usually cannot replicate the entire measured $I - V$ curves due to non-idealities. For example, the polycrystalline nature of ZnO thin films introduces complications such as grain boundary trapping and a V_{GS}-dependent mobility [54, 144, 145]. Contact effects such as parasitic series resistance and contact barriers also cause deviations particularly at low V_{GS} and V_{DS}. Short channel effects similar to those found in MOSFETs, e.g. lowering of V_{th}, degradation of subthreshold swing (SS), and increasing of saturation current (I_{sat}), are also observed [146]. A more complete TFT model is thus needed to account for these non-idealities. Currently. there have not been many attempts at modelling ZnO TFTs compared to organic field effect transistors (OFETs) and Si-based TFTs. Like ZnO TFTs, OFETs and silicon-based TFTs also exhibit the non-idealities mentioned above suggesting that previously proposed universal TFT models can be adapted for ZnO [147, 123, 145, 124, 148]. For this work, a gradual channel approximation (GCA) DC compact model developed by Marinov *et al.* for OFETs was modified to model top-gate ZnO TFTs with different S/D metallizations and drain-side geometries [143, 149]. This model is attractive because it can account for the deviations caused by contact resistance, a non-constant mobility, and increasing I_{sat} without requiring many non-physical empirical parameters or extra complementary measurements and simulations. It is also universal in that it does not require physical parameters that are unique only to organic semiconductors (OSCs). Previously reported ZnO TFT compact models utilize approximations of the surface potential at the S/D contacts that make it difficult to extract ac-

curate parameter values from experimental data [150, 151]. Another advantage of the model by Marinov *et al.* is that its parameter values can be extracted graphically with curve fitting rather than using numerical methods.

One major component of the model by Marinov *et al.* is the gate voltage-enhanced mobility, which is modelled by the following power law,

$$\mu = \mu_o \Big[V_G - V_{th} - V(x) \Big]^{\gamma} \tag{5.2}$$

where V_G is the independent gate electrode voltage, $V(x)$ is the voltage along the channel at location x, μ_o is the mobility prefactor, and γ is the mobility enhancement factor, which accounts for the movement of the Fermi level in the band-gap with gate bias [152, 145]. A superlinear dependence of mobility on V_{GS} is frequently observed in TFTs; however, there is not a universally accepted theory regarding the exact origins of mobility enhancement. Bias dependency of μ has been attributed to traps [144, 153], particularly for polycrystalline semiconductors, as well as the semiconductor's charge carrier transport mechanism [154, 155, 156]. In fact, Equation 5.2 is derivable from several different charge transport theories when assuming an exponential density of states (DOS) approximation with localized states distributed in some manner in the semiconductor's bandgap including carrier transport based on tail distributed traps (TDTs) [152], variable range hopping (VRH) [155], and multiple trapping-and-release (MTR) [144, 153], which also has been considered for polycrystalline ZnO [150]. In these cases, γ is related to the effective characteristic energy width of the exponential DOS tail [156]. For ZnO transistors, a non-constant mobility is likely caused by charge trapping-and-releasing at the grain boundaries of the polycrystalline ZnO channel [54, 150].

Similar to the generic MOSFET DC model in Equation 5.1, the drift current in the model by Marinov *et al.* is approximated by the movement of the gate-induced accumulation charge using the equation below,

$$\frac{I_D}{W} = Q(x)\mu(x)\frac{dV}{dx} = \mu_o C_{ox}(V_G - V_{th} - V_x)^{\gamma+1}\frac{\partial V_x}{\partial x} \tag{5.3}$$

where I_D is the independent drain current and $Q(x)$ is the charge density. Independent electrode voltages and currents are employed to match the notation used

by the original authors. The right-most expression in Equation 5.3 is obtained from substituting in Equation 5.2 and $Q(x) = C_{ox}\big[(V_G - V_{th}) - V(x)\big]$. Afterwards, the GCA is applied and the current is integrated over the entire length of the channel,

$$\int_0^L \frac{I_D}{W} dx = \int_{V_S}^{V_D} \mu_o C_{ox}(V_G - V_{th} - V_x)^{\gamma+1} dV \tag{5.4}$$

where V_S and V_D are the independent electrode voltages for the S/D respectively. Performing the integrations in Equation 5.4 result in the following equation denoted by Marinov *et al.* as the TFT generic charge drift model [143],

$$I_D = \frac{W}{L}\mu_o C_{ox} \times \frac{(V_G - V_{th} - V_S)^{\gamma+2} - (V_G - V_{th} - V_D)^{\gamma+2}}{\gamma + 2} \tag{5.5}$$

A step-by-step derivation of Equation 5.5 can be found in Ref. [143]. The TFT generic charge drift model closely resembles the classical MOSFET model as the only difference in their derivation is the mobility enhancement from V_{GS}. In fact, when $\gamma = 0$, the TFT generic charge drift model reduces to Equation 5.1. Equation 5.5 is valid only for operation in the above threshold ($V_G > V_{th}$) regime and cannot account for the exponential behaviour of the TFT's subthreshold regime. Hence the interpolation function presented below, referred to as the effective gate overdrive function, is used to add the subthreshold, linear-to-saturation transition, and below-to-above V_{th} transition behaviours to the TFT generic charge drift model [143],

$$f(V_G, V_x) = V_{SS} \ln\left\{1 + \exp\left[-\frac{V_G - V_{th} - V_x}{V_{SS}}\right]\right\} \tag{5.6}$$

where V_{SS} determines the slope of the exponential subthreshold current and can be approximated from the TFT's SS near V_{th} by [149],

$$V_{SS} = \frac{\gamma + 2}{2\ln(2)} \frac{\partial V_G}{\partial \ln(I_D)} \approx 0.31(\gamma + 2)SS \tag{5.7}$$

The form of TFT generic charge drift model after interpolation is as follows,

$$I_D = \frac{W}{L}\mu_o C_{ox} \times \frac{\left[f(V_G, V_S)\right]^{\gamma+2} - \left[f(V_G, V_D)\right]^{\gamma+2}}{\gamma + 2} \tag{5.8}$$

where $f(V_G, V_S)$ and $f(V_G, V_D)$ are defined by Equation 5.6.

The basic TFT generic charge drift model in Equation 5.8 can be further modified to include device non-idealities. To model the effects of finite contact resistance (R_C), a parasitic series resistance can be added at both S/D terminals resulting in a voltage drop V_C. Practically, this can be added to the model by replacing V_x with $V_x - V_C$ in Equation 5.6 [143, 157]. Unfortunately, because V_C itself depends on I_D, there is not a fully analytical solution for I_D when $\gamma > 0$ [157, 148]; i.e. there will be uncertainties in the model parameters unless they are extracted from multiple transistors that are identical in behaviour. Nonetheless, it was possible to extract meaningful values from a single TFT when using transfer (I_{DS} versus V_{GS}) characteristics at several different V_{DS} values, which is described in the upcoming section. Another non-ideality that was considered in the ZnO TFT model was imperfect saturation in the TFT's output (I_{DS} versus V_{DS}) characteristics. To include a non-constant I_{sat} in the model, the conventional channel length modulation (CLM) factor (λ), which is related to the slope of the TFT's I_{sat} versus V_{DS}, was employed (although the imperfect saturation may not necessarily be caused by CLM) [158]. With the addition of these two specific non-idealities, the complete model for a n-type TFT is given below (written in the conventional form where V_S is grounded),

$$\begin{aligned} I_{DS} &= \frac{W}{L}\mu_o C_{ox} \times (1 + \lambda V_{DS}) \times \frac{\left[f(V_{GS}, V_{CS})\right]^{\gamma+2} - \left[f(V_{GS}, V_{DC})\right]^{\gamma+2}}{\gamma + 2} \\ f(V_{GS}, V_{CS}) &= V_{SS} \ln\left\{1 + \exp\left[-\frac{V_{GS} - V_{th} - V_{CS}}{V_{SS}}\right]\right\} \\ f(V_{GS}, V_{DC}) &= V_{SS} \ln\left\{1 + \exp\left[-\frac{V_{GS} - V_{th} - V_{DC}}{V_{SS}}\right]\right\} \end{aligned} \tag{5.9}$$

where $V_{CS} = I_{DS} \times R_S$ and $V_{DC} = V_{DS} - I_{DS} \times R_D$. R_S and R_D are the effective parasitic resistances at the S/D respectively from contact effects. For symmetrical

S/D-overlapped devices, the assumption that $R_S = R_D = 0.5R_C$ was made based on the device's symmetry (it should be noted that the notation here is different from the previous chapter).

In the works published by Marinov *et al.* regarding the TFT generic charge drift model [143, 149, 157], only the symmetrical device structure was considered. Thus, for this study, the modelling of the S/D contact resistances was expanded to adapt the model for asymmetrical device architectures. In devices with asymmetrical S/D contacts (including both gate-to-drain-overlapped and drain-offset structures), R_D was approximated to be zero to simplify the parameter extraction process; this approximation was valid as the extracted R_C from Au contacts was more than 150 times lower than the extracted R_C from Ru contacts using the transfer length method (TLM). Details of this analysis are presented in the later sections [see Fig. 5.6(a) and Fig. 5.9(c)]. The modelling of asymmetrical drain-offset TFTs was more complicated, however, due to the inclusion of the un-gated offset region that changed the TFT's device physics. To include the effects of the offset region in the TFT generic charge drift model, an additional parasitic element R_{GD} was added between the gate-and-drain (details can be found in Section 5.6). Equivalent circuits for each type of TFT are presented in Fig. 5.1(d), (e), and (f). For each device structure, the complete TFT behaviour is modelled by the series connection between an intrinsic TFT and relevant parasitic elements at the S/D for contact and drain-offset effects.

5.3 Parameter Extraction Method

A single TFT extraction method based on the techniques proposed by Marinov *et al.* was utilized to extract parameters for the TFT generic charge drift model in Equation 5.9 [157, 149]. Although parameter extraction was also possible using plural device methods, for example the TLM used in the previous chapter [131], they necessitate measuring multiple TFTs all with similar and consistent characteristics. In this study, V_{th} and R_C, which the TLM assumes are constant, varied from device-to-device likely due to processing non-uniformities making the TLM not as accurate for those parameters. The main drawback to the single transistor extraction approach though, as mentioned previously, is the absence of

a fully analytical solution for I_{DS} in the TFT generic charge drift model when including R_C. To help improve the accuracy of the extracted parameter values, the main TFT parameters (γ, μ_o, V_{th}, and R_C) were extracted from transfer characteristics of the same device at different conditions (i.e. in the linear and saturation regimes) to mitigate their interference with each other. Firstly, to calculate γ, the transfer curve when the device is in saturation ($V_{DS} > V_{GS} - V_{th}$) was modified using the so-called H_{VGS} function [159, 149], which is defined by the equation below,

$$H_{VGS} = \frac{\int_{V_{th}}^{V_{GS}} I_{DS}(V_{GS}) dV_{GS}}{I_{DS}(V_{GS})} = \begin{cases} = \frac{V_{GS}-V_{th}}{\gamma+3} \text{ for } V_{DS} > (V_{GS} - V_{th}) \\ \approx \frac{V_{GS}-V_{th}}{\gamma+2} \times \left[1 - \text{Err}\left(\frac{V_{DS}}{V_{GS}-V_{th}}\right)\right] \\ \text{for } V_{DS} << (V_{GS} - V_{th}) \end{cases} \tag{5.10}$$

where the rightmost expressions result from substituting in Equation 5.8 for $I_{DS}(V_{GS})$ (see Ref. [149] for more details). Because H_{VGS} is a linear function of the gate overdrive voltage, $(V_{GS} - V_{th})$, a linear regression fit of H_{VGS} versus V_{GS} can be used to calculate γ and V_{th} from its slope and x-intercept respectively. In Equation 5.10, the slope is different for the saturation and linear regimes as there is an error term when calculating γ from H_{VGS} in the linear regime. Thus, in this work, γ was extracted from the transfer characteristics wherein the device was fully saturated to avoid the error term. To extract μ_o and R_C, the I_{DS} from the linear regime transfer characteristics was partially linearised first. If $V_{DS} << V_{GS} - V_{th}$ and the total contact voltage drops, $(I_{DS}R_S + I_{DS}R_D)$, are $<< V_{DS}$, the Taylor series expansion of $(1 + x)^n \approx 1 + nx$ for $|x| << 1$ (also known as the binomial approximation) can be utilized on Equation 5.5 around $V_{DS} = 0$ V to partially linearise the TFT generic charge drift model as shown

below [157],

$$
\begin{aligned}
I_{DS} &= K(V_{GS}-V_{th})^{\gamma+2} \times \frac{\left(1-\frac{I_{DS}R_S}{V_{GS}-V_{th}}\right)^{\gamma+2}-\left(1-\frac{V_{DS}-I_{DS}R_D}{V_{GS}-V_{th}}\right)^{\gamma+2}}{\gamma+2} \\
&\approx K(V_{GS}-V_{th})^{\gamma+2} \times \frac{\left(1-(\gamma+2)\frac{I_{DS}R_S}{V_{GS}-V_{th}}\right)-\left(1-(\gamma+2)\frac{V_{DS}-I_{DS}R_D}{V_{GS}-V_{th}}\right)}{\gamma+2} \\
&\approx K(V_{GS}-V_{th})^{\gamma+1}(V_{DS}-I_{DS}R_S-I_{DS}R_D) \\
&\approx K(V_{GS}-V_{th})^{\gamma+1}(V_{DS}-I_{DS}R_C)
\end{aligned}
\tag{5.11}
$$

where $K = \frac{W}{L}\mu_o C_{ox}$ and $R_C = R_S + R_D$. The first line in Equation 5.11 is Equation 5.5 rewritten with the addition of contact resistance and rearranged to a form that can exploit the aforementioned binomial approximation, which is demonstrated in the next line. After partially linearising I_{DS}, the current degradation from R_C can be compensated by employing the so-called Y_{VGS}-function [160, 157]. The Y_{VGS} function when considering mobility enhancement is defined by the expression below [157],

$$
Y_{VGS} = \frac{I_{DS}}{\sqrt{g_m V_{DS}}} \approx \sqrt{\frac{\frac{W}{L}C_{ox}\mu_o}{1+\gamma}} \times (V_{GS}-V_{th})^{1+\gamma/2} \tag{5.12}
$$

where $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ is the TFT transconductance. Since the right-most expression is derived from the partially linearised I_{DS} shown in Equation 5.11, it is only valid when the TFT is operating at low V_{DS}. According to the form of Equation 5.12, it is apparent that a linear regression fit to $\sqrt[1+\gamma/2]{Y_{VGS}}$ versus V_{GS} will allow μ_o and V_{th} to be calculated from its slope and x-intercept respectively. The main feature of Equation 5.12 is that R_C is not present as Y_{VGS} compensates for it (but only in the linear regime where the approximation in Equation 5.12 is valid). Consequently, the parameters extracted from Y_{VGS} should be independent of R_C. An accurate value for γ is a prerequisite however (which was obtained from H_{VGS} while the TFT was in saturation). To determine R_S and R_D, a point-by-point method was used as described in Ref. [157]. The mathematical difference between the measured on-state resistance (R_{on}) and modelled intrinsic channel resistance (R_{ch}), which was calculated from the extracted V_{th}, μ_o, and γ,

was attributed to R_C. This is summarized by the expressions below,

$$\begin{aligned} R_C = R_S + R_D \approx R_{on} - R_{ch} \text{ where} \\ R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}} \text{ (measured)} \\ R_{ch} = \frac{1}{W/LC_{ox}\mu_o(V_{GS} - V_{th})^{1+\gamma}} \text{ (modelled)} \end{aligned} \tag{5.13}$$

where the expression for R_{ch} is derived from the partially linearised I_{DS} (see Equation 5.15 shown in the following section for specific details). From the plot of R_C versus V_{GS}, a constant R_C was approximated from its average value in the nearly constant region of the plot, which typically occurred when $V_{GS} >> V_{th}$.

Following parameter extraction, TFT output characteristics were re-simulated using Equation 5.9 to verify the accuracy of the TFT generic charge drift model. The re-simulated $I-V$ curves match the measured characteristics quite well in the $V_{GS} > V_{th}$ regime, and results will be discussed in the following sections. Before that, a summary of the single TFT parameter extraction method is described below:

Step 1. Determine an initial value of V_{th} from the transfer characteristics. In this study, V_{th} was graphically calculated from the voltage where the current begins to rise in the transfer curve. V_{th} can also be extracted during steps 3 and 4 as well but an initial approximation for V_{th} is needed first.

Step 2. Calculate SS from the slope of the transfer curve in semi-log scale in the region around V_{th} (see Equation 3.2 for the definition of SS). Afterwards, V_{SS} can be estimated by $0.31(\gamma + 2)SS$ [149].

Step 3. From the transfer characteristics when the TFT is in saturation, calculate H_{VGS} and then determine γ and V_{th} (if necessary) from the slope and x-intercept respectively of a straight line fit to H_{VGS} versus V_{GS} using Equation 5.10.

Step 4. From the transfer characteristics in the linear regime at $V_{DS} << V_{GS} - V_{th}$, calculate $\sqrt[1+\gamma/2]{Y_{VGS}}$ using Equation 5.12 and γ extracted in the previous step. Afterwards, extract μ_o and V_{th} (if necessary) from the slope and x-intercept respectively from a straight line fit to $\sqrt[1+\gamma/2]{Y_{VGS}}$ versus V_{GS}. It was found that

the V_{th} extracted from this step was not as accurate during the re-simulation of the output characteristics for parameter verification. Most likely, the device's V_{th} shifted at high V_{GS} and V_{DS} (reasons why are described in the following paragraph) making the V_{th} extracted from the saturation transfer curves more compatible with the output characteristics.

Step 5. Calculate R_C from Equation 5.13, and then estimate its average value from the flat region of R_C versus V_{GS} (usually at $V_{GS} >> V_{th}$). Depending on the TFT structure and S/D metallization, R_C can be further separated into R_S and R_D. For symmetrical S/D contacts, the assumption that $R_S = R_D$ was made based on the device's symmetry. Whereas, for the asymmetrical S/D-overlapped devices, Au's low resistivity was assumed to be negligible making $R_C = R_S$. Lastly, for the drain-offset devices, which also utilized Au for the drain but a different metal for the source, R_S was assumed to be the same as the value extracted from the symmetrical overlapped TFTs to allow $R_D = R_{GD} = R_C - R_S$ to be calculated; R_{GD} is the parasitic element used to model the drain-offset's influence on the device characteristics and will be discussed in detail afterwards in Section 5.6. Without making this assumption, there is not enough information to confidently separate R_S and R_D.

Step 6. If I_{sat} is not constant, then λ can be employed to add a slope to I_{sat} in the output characteristics' saturation regime. λ was determined by curve fitting when necessary.

Step 7. Re-simulate the TFT $I-V$ characteristics using the extracted parameters and Equation 5.9 to verify the accuracy of parameter extraction. Multiple attempts with different values of V_{th} and γ may be required to obtain accurate $I - V$ curves.

This parameter extraction procedure was utilized for all three classes of TFTs used in this experiment, and matching re-simulations of the output characteristics were realized for all device structures. The experimental ZnO TFTs' current increased over each measurement, making the parameter values extracted from the transfer curves not completely match the output characteristics during parameter verification, which is attributed to instabilities caused by gate bias stress. A change in device mobility, shift in V_{th}, and change in SS can all manifest from the prolonged application of the gate bias due to the charging of traps at the

grain boundaries of the polycrystalline channel [161, 162, 163], charging of traps in the gate insulator or at the channel/gate insulator interface [164, 165, 68], and defect creation in the ZnO channel itself [164, 166]. Fortunately, notwithstanding the device instabilities, after tweaking some of the parameters (mainly μ_o and R_C), a close fit to the measured $I-V$ characteristics can be reproduced with the parameters extracted via the single TFT method.

5.4 Symmetrical S/D-overlapped Top-Gated ZnO TFTs with Ru/Ru S/D Contacts

Symmetrical S/D-overlapped (or staggered) TFTs using Ru/Ru for the S/D metallization were measured and modelled first. For this device structure, the TFT characteristics were fairly consistent even when varying L. Thus, the TLM was suitable for extracting the intrinsic mobility, V_{th}, and R_C from a series of devices (with L ranging from 4 to 32 μm), and these extracted values are then compared with the values produced by the single TFT extraction technique to verify their accuracy. Transfer characteristics of a typical TFT where $W/L = 50\ \mu\text{m}/32\ \mu\text{m}$ in the linear and saturation regimes are shown in Fig. 5.2. Employing the conventional approach (Equation 5.1), the saturation mobility (μ_{sat}) and V_{th} were calculated to be 0.62 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and 1.06 V respectively by fitting a straight line to the transfer curve at $V_{DS} = 3$ V. As noted in Section 5.1, multiple devices for each device architecture were tested, and the $I-V$ characteristics in Fig. 5.2 were representative of all the measured symmetrical Ru/Ru staggered devices (which includes the TFTs used for the TLM study presented afterwards). The Ru/Ru TFTs exhibited both excellent switching performance [highlighted by their positive V_{th}, high current on-to-off ratio ($I_{on/off}$) of 6.5×10^6, and low SS of 0.2 V/decade] and respectable on-state performance, such as their moderately-high on-state drain current (I_{on}) and mobility.

The V_{th} calculated using the conventional method of fitting the transfer characteristics to Equation 5.1 was not compatible for the TFT generic charge drift model however. After parameter verification by simulating Equation 5.9, a value of $V_{th} = 0.53$ V produced the closest match to the measured data suggesting that

the TFT generic charge drift model works better with a V_{th} that is closer to the TFT's turn-on voltage (V_{on}) - where I_{DS} first begins to rise in the transfer curve. Parameter extraction for model by Marinov *et al.* was done according to the procedure outlined in the previous section. The H_{VGS} and linear Y_{VGS} ($\sqrt[1+\gamma/2]{Y_{VGS}}$) functions derived from the transfer curves in the saturation and linear regimes respectively (and their corresponding linear regression fits) are displayed in Fig. 5.3(a), (b). For the H_{VGS} function, a numerical method was utilized to calculate the integral in Equation 5.10. Although γ was relatively consistent throughout the linear portion of the curve, V_{th} was more dependent on the initial V_{th} input and where the fit was performed. For this particular device, V_{th} and γ eventually converged to 0.53 V and 0.64 respectively after multiple linear regression fits to H_{VGS} using the extracted V_{th} value from the previous iteration. In Fig. 5.3(b), a value of $\mu_o = 0.32$ cm^{2}V^{-1}s^{-1} was extracted from the slope of the linear fit to $\sqrt[1+\gamma/2]{Y_{VGS}}$ versus V_{GS}. The x-intercept can also be used to calculate V_{th} although it was found that the V_{th} extracted from $I-V$ curves during saturation matched the output characteristics better. Last of all, the estimated R_C using Equation 5.13 is presented in Fig. 5.3(c); the dashed line shows the average R_C (in semi-log scale for easier readability) once it flattened out at higher V_{GS}. Because of the device's symmetry, the assumption that $R_S = R_D = \frac{1}{2}R_C$ was made for the TFT generic charge drift model (Equation 5.9). From Fig. 5.3(c), it is apparent that R_C was likely not constant especially as V_{GS} approaches V_{th}. V_{GS} dependence is also observed in the R_C values extracted by the TLM approach described afterwards. Nonetheless, the TFT generic charge drift model produced an accurate simulation in the $V_{GS} > V_{th}$ range despite the constant R_C assumption (which is seen in the re-simulated output characteristics below). If better accuracy around V_{th} is required, then an empirical fit of the V_{GS} dependence of R_C can be performed [167, 168]. From Fig. 5.3(c), an average value of $R_S = R_D = 15$ kΩ was extracted to complete parameter extraction. A summary of the extracted values for the TFT generic charge drift model is shown in Table 5.1.

The re-simulated output characteristics for parameter verification along with the measured data are shown in Fig. 5.4. By slightly adjusting $R_S = R_D$ to 13 kΩ, a good match to the simulated and measured characteristics was realized. In particular, the modelled current saturated at similar values to the experimental

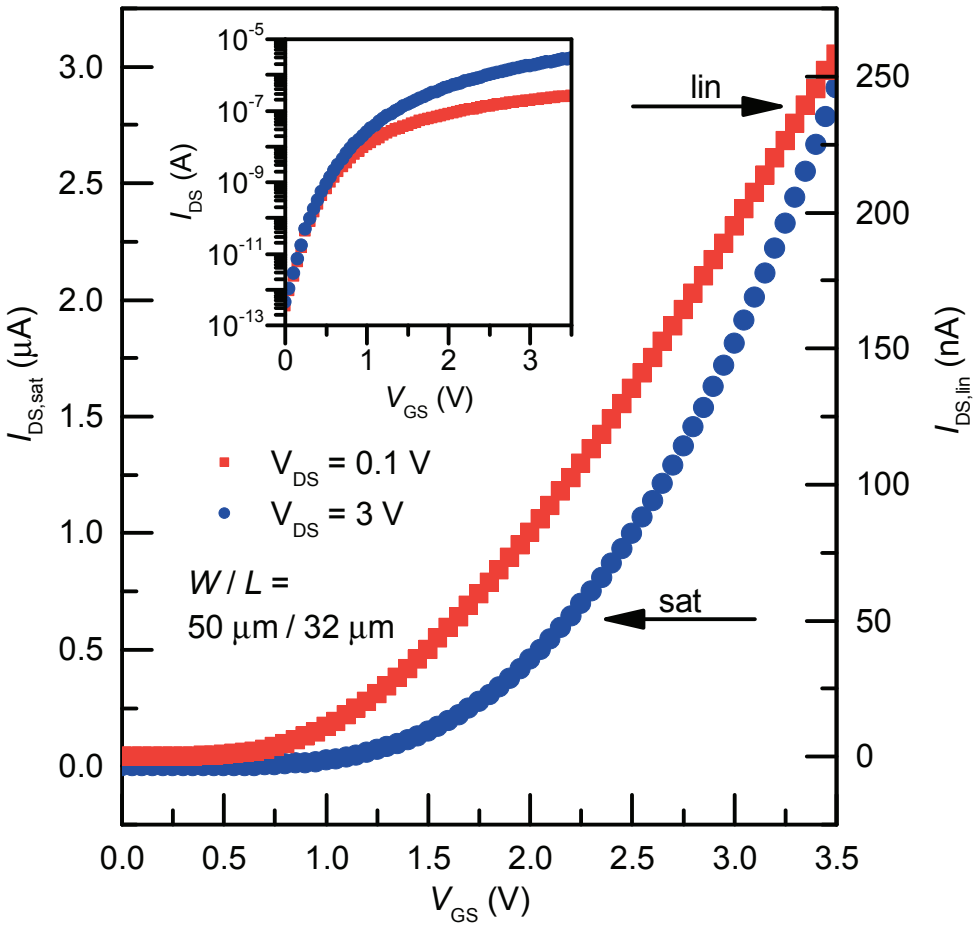

Figure 5.2: Transfer characteristics of an symmetrical S/D-overlapped ZnO TFT with Ru S/D contacts where $W/L = 50$ μm/32 μm at $V_{DS} = 0.1$ V (red squares) and 3 V (blue circles). The inset shows the same data in semi-log scale.

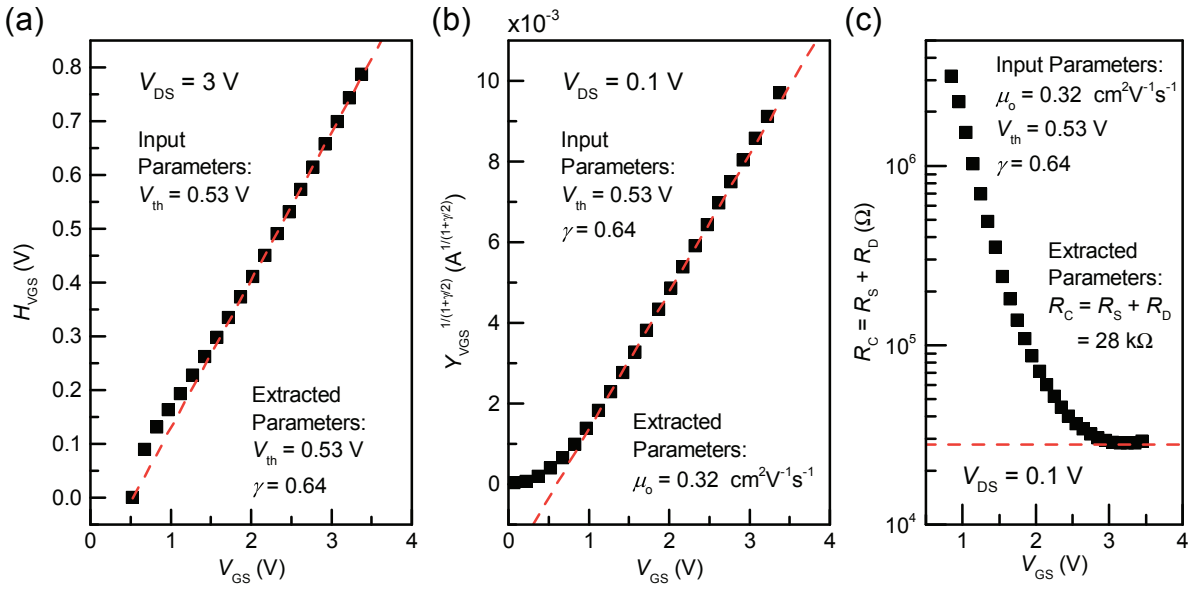

Figure 5.3: Modified $I-V$ characteristics for parameter extraction from a symmetrical S/D-overlapped ZnO TFT with Ru S/D contacts where $W/L = 50$ μm/32 μm. (a) H_{VGS} versus V_{GS} at $V_{DS} = 3$ V calculated with an input of $V_{th} = 0.53$ V. The linear regression fit used to extract γ and V_{th} is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at $V_{DS} = 0.1$ V. The linear regression fit used to extract μ_o is shown by the dashed line. (c) Contact resistance at the S/D terminals ($R_C = R_S + R_D$) calculated from the transfer characteristics at $V_{DS} = 0.1$ V plotted in semi-log scale. The average R_C at moderate $V_{GS} > V_{th}$ is shown by dashed line.

$I-V$ curves without needing to deliberately set $V_{DS,sat}$ with an external fitting parameter, which is another useful feature of the TFT generic charge drift model. To quantitatively assess the goodness of fit, the mean percent difference was calculated by averaging the percent difference between the measured and simulated I_{DS} values at each $V_{GS} > V_{th}$ step. From this calculation, there was a mean 3.0% percent difference between the experimental and simulated output characteristics (in the after threshold regime) supporting the efficacy of the model. Consequently, the TFT compact model by Marinov *et al.* and its accompanying single TFT extraction procedure were capable of accurately fitting the characteristics of ZnO TFTs with the conventional staggered top-gate architecture especially in the $V_{GS} > V_{th}$ regime, wherein the main deviations from the ideal transistor model can be captured entirely by contact resistance and a V_{GS} dependent mobility.

To double check the accuracy of the parameter values extracted using the single TFT extraction procedure, the TLM was employed with a series of symmetrical S/D-overlapped ZnO TFTs [131]. In the TLM analysis, TFT on-resistance (R_{on}) at very small V_{DS} was calculated from the output characteristics at each V_{GS} step for multiple TFTs with L ranging from 4 to 32 μm while every other dimension was constant ($W = 50$ μm and $L_{ov} = 10$ μm). At very low V_{DS}, R_{on} can be approximated as a series combination of the L-independent S/D contact resistances ($R_S + R_D$) and the L-dependent intrinsic channel resistance (r_{ch}), as shown by the width-normalised equation below,

$$R_{on}W = W\left(\frac{\partial V_{DS}}{\partial I_{DS}}\right) \approx W(r_{ch}L + R_S + R_D) \tag{5.14}$$

where the approximation of $R_S = R_D = 0.5R_C$ can be made based on the device's symmetry (please note that the notation for R_C is different from Equation 4.2 in the previous chapter to match the definition of R_C in Equation 5.9). The calculated $R_{on}W$ plotted as a function of L is presented in Fig. 5.5. In the range of L measured, all devices displayed consistent behaviours except for some variance in their V_{th}, which made the TLM less accurate at lower V_{GS} values. Nevertheless, according to Equation 5.14, from the linear regression fit of R_{on} versus L, r_{ch} and R_C can be calculated from its slope and intercept respectively at each V_{GS} step. The resulting R_C and r_{ch} plotted versus V_{GS} are shown in Fig.

Table 5.1: Extracted Parameter Values from Modelling ZnO TFTs using the TFT Generic Charge Drift Model

TFT Structure	L [μm]	L_{GD} [μm]	SS [V/dec]	V_{th} [V]	γ	μ_o [$\mathrm{cm^2V^{-1}s^{-1}}$]	R_S [kΩ]	R_D [kΩ]	λ	Mean Percent Difference [%]
Ru/Ru S/D-overlapped	32	-10	0.2	0.53	0.64	0.31	13	13	0	3.0
Ru/Ru S/D-overlapped	16	-10	0.2	0.85	0.39	0.42	14	14	0.003	9.6
Ru/Ru S/D-overlapped	8	-10	0.2	0.80	0.33	0.41	18	18	0.005	4.8
Ru/Ru S/D-overlapped	4	-10	0.2	1.14	0.39	0.37	15	15	0.015	7.6
Ru/Au S/D-overlapped	32	-10	0.55	-0.55	0.00	7.10	9.5	0	0	5.2
Ru/Au Drain-offset	32	0	0.1	1.10	0.40	0.70	13	$\frac{1.3\times10^3}{V_{GS}-1.10}$	0	7.7
Ru/Au Drain-offset	32	2	0.1	1.10	0.40	0.69	13	$\frac{2.4\times10^3}{V_{GS}-1.10}$	0	13.0
Ru/Au Drain-offset	32	8	0.1	1.15	0.40	0.82	13	$\frac{2.7\times10^3}{V_{GS}-1.15}$	0	14.7
Ru/Au Drain-offset	32	16	0.1	1.10	0.65	0.47	13	$\frac{5.3\times10^3}{V_{GS}-1.10}$	0	17.6
Cu/Au S/D-overlapped	32	-10	0.2	2.4	1.00	2.00	1.6×10^3	0	0.08	12.0

All devices have the same W of 50 μm. The parameters were extracted using the single TFT parameter extraction method. $L_{GD} = -10$ μm refers to a gate-to-S/D overlap of 10 μm, whereas a positive L_{GD} refers to a drain-offset length of the entered value. If R_D varies with V_{GS}, the empirical formula for the V_{GS} dependence of R_D will be given instead of a constant value. For the Ru/Au drain-offset ZnO TFTs, R_S was assumed to be equal to the extracted value from the symmetrical Ru/Ru S/D-overlapped device. The mean percent difference was calculated from comparing the simulated and experimental output characteristics in the after-threshold ($V_{GS} > V_{th}$) regime.

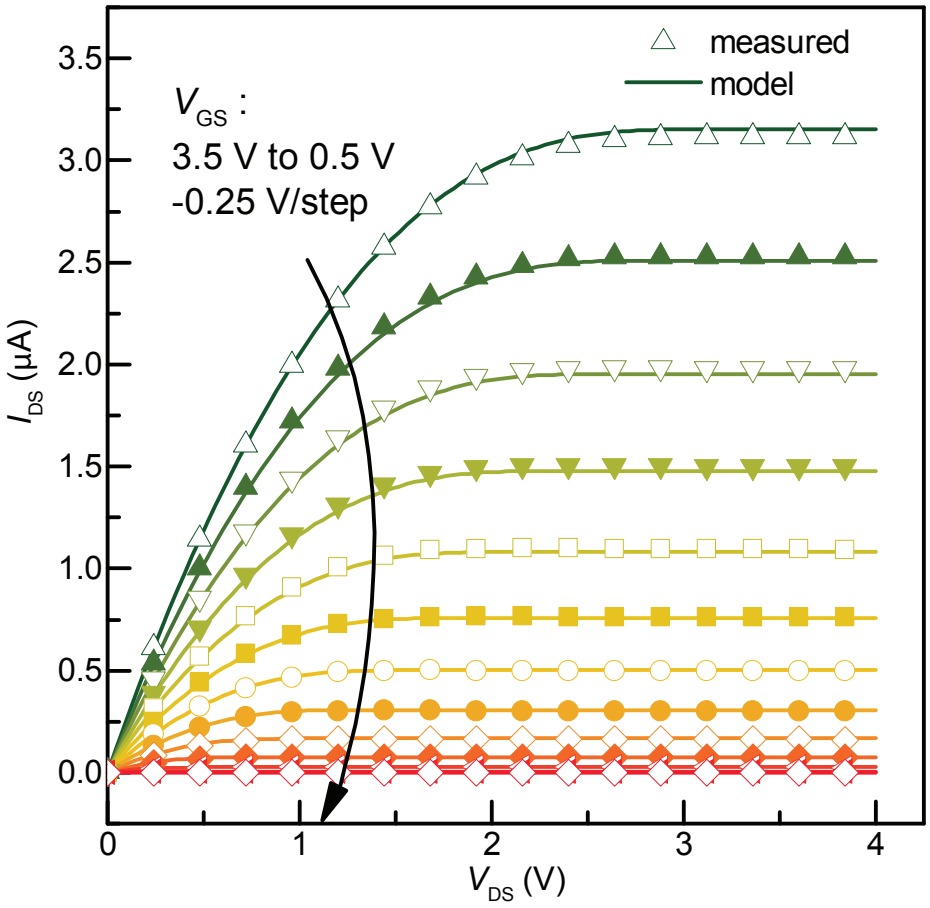

Figure 5.4: Output characteristics of a symmetrical S/D-overlapped ZnO TFT with Ru/Ru S/D contacts where $W/L = 50\ \mu$m$/32\ \mu$m. V_{GS} is increasing from 0.5 V to 3.5 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

5.6 (in semi-log scale for easier readability). Using the TLM approach, it is clear that both the extracted r_{ch} and R_C are dependent on V_{GS}. Furthermore, much like Fig. 5.3(c), there is less variation in R_C at higher V_{GS} although the exact values for R_C are different (e.g. 30 kΩ for the single TFT approach versus 60 kΩ for the TLM approach at $V_{GS} = 3.5$ V). By inserting the partially linearised expression for I_{DS} (shown in Equation 5.11) into Equation 5.14, an expression for R_{on} that is compatible with the TFT generic charge drift model can be obtained like so,

$$\begin{aligned} \frac{\partial I_{DS}}{\partial V_{DS}} &\approx \frac{\frac{W}{L}\mu_o C_{ox}(V_{GS}-V_{th})^{\gamma+1}}{1+R_C\times\frac{W}{L}\mu_o C_{ox}(V_{GS}-V_{th})^{\gamma+1}} \\ R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}} &\approx R_{ch}+R_C = \frac{1}{\frac{W}{L}\mu_o C_{ox}(V_{GS}-V_{th})^{\gamma+1}}+R_C \end{aligned} \tag{5.15}$$

where $R_{ch} = r_{ch}L = \left[\frac{W}{L}\mu_o C_{ox}(V_{GS}-V_{th})^{\gamma+1}\right]^{-1}$. If γ is known, r_{ch} can be linearised with V_{GS} by taking its reciprocal and then applying the $\gamma+1$ root to both sides. Afterwards, the TFT intrinsic μ_o and V_{th} can be calculated from the slope and intercept respectively of a linear regression fit to $r_{ch}^{\frac{-1}{\gamma+1}}$ versus V_{GS} as shown by Fig. 5.7. Using $\gamma = 0.64$ extracted from the TFT presented previously, μ_o and V_{th} was determined to be 0.3 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and 0.5 V respectively for a $L = 32\mu$m device, which is almost equal to the values obtained using the single device approach. Unfortunately, γ cannot be reliably extracted using the TLM. After performing the single TFT extraction method on each device utilized for the TLM in Fig. 5.5, it was observed that V_{th} (ranging from 0.5 to 1.1 V) and γ (ranging from 0.33 to 0.64) randomly varied from device-to-device, likely from non-uniformities during device processing. The variation in γ introduces some uncertainty into the TLM-extracted intrinsic V_{th} and μ_o values. If the lowest observed $\gamma = 0.33$ was used instead of 0.64, the TLM results in $V_{th} = 0.76$ V and $\mu_o = 0.46$ $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, which is similar to the $V_{th} = 0.8$ V and $\mu_o = 0.41$ $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ extracted from the $\gamma = 0.33$ device using the single TFT extraction procedure (see Table 5.1 for details). Thus, given a TFT's γ value, the TLM approach produce values for V_{th} and μ_o suitable for the TFT generic charge drift model. In spite of that, since both parameter extraction methods output similar

values, the single TFT parameter extraction approach is more attractive as it is faster and simpler to employ.

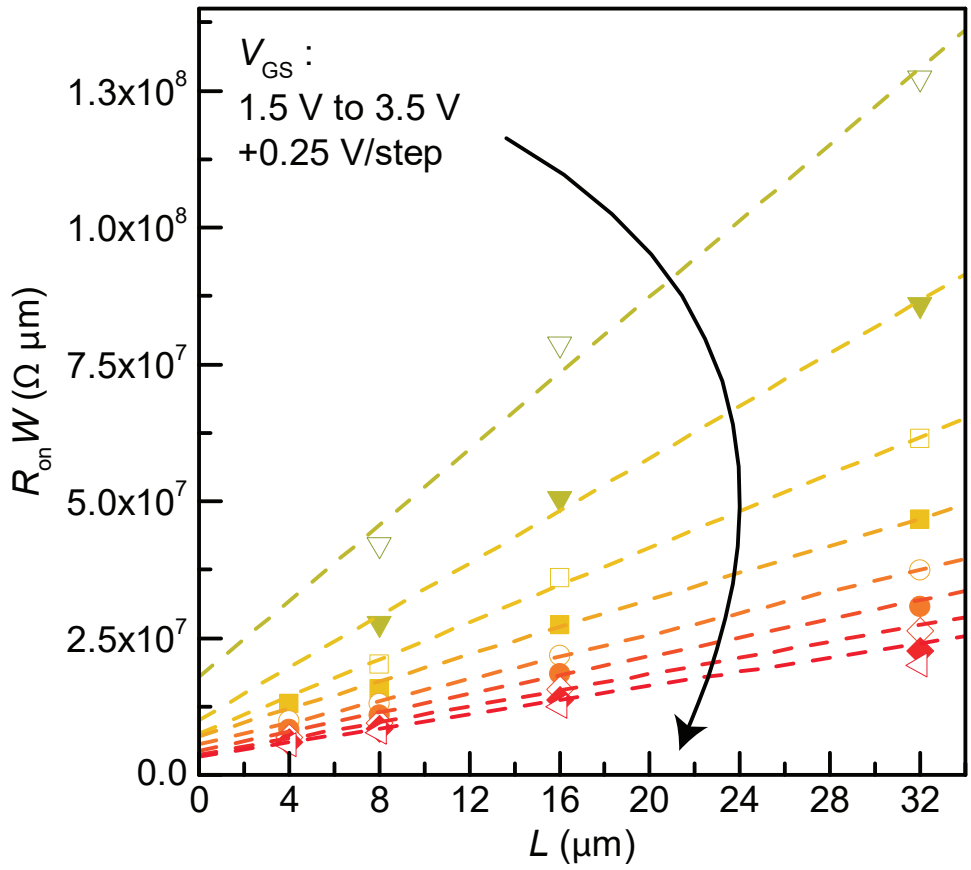

Figure 5.5: Width-normalised on-resistance ($R_{on}W$) versus L for a set of symmetrical S/D-overlapped ZnO TFTs with Ru/Ru S/D contacts. V_{GS} varies from 1.5 V to 3.5 V increasing in 0.25 V steps (from top to bottom). The linear regression fits to $R_{on}W$ for each V_{GS} step are shown by the overlaid dashed lines.

5.4.1 Symmetrical S/D-overlapped Top-Gated ZnO TFTs with Au/Au S/D Contacts

In the previous chapter, the bottom Au/ZnO metal contact induced high electron densities and low contact resistances that can be applied to an asymmetrical transistor structure for improving the TFT on-state performance. Therefore,

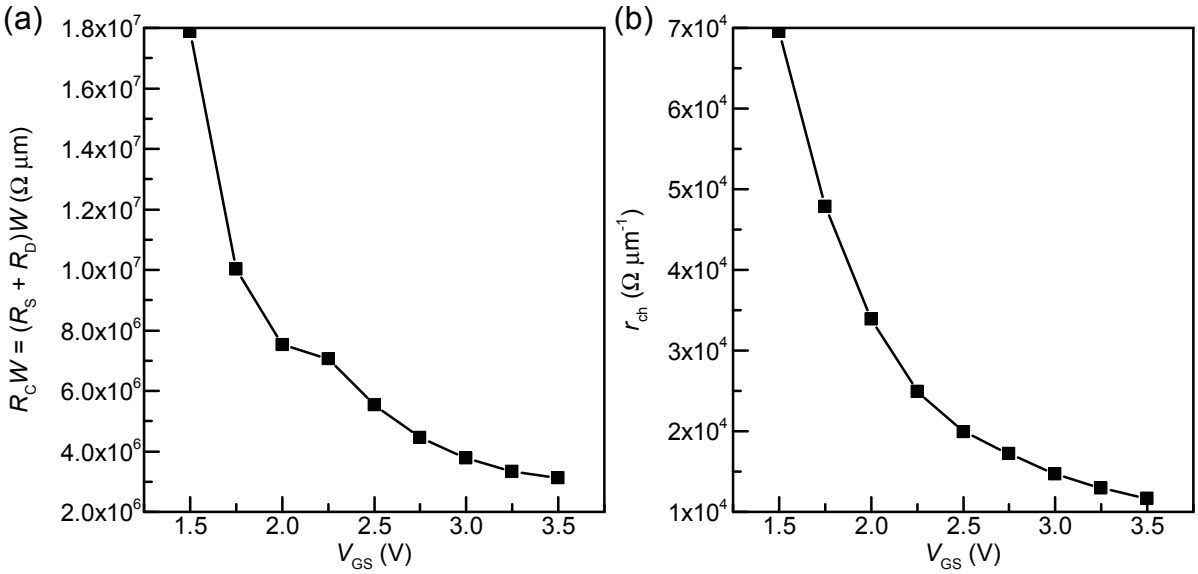

Figure 5.6: (a) Width-normalised contact resistance (R_CW) and (b) intrinsic channel resistance per unit length (r_{ch}) as a function of V_{GS} in semi-log scale extracted by the TLM for symmetrical S/D-overlapped TFTs with Ru/Ru S/D contacts.

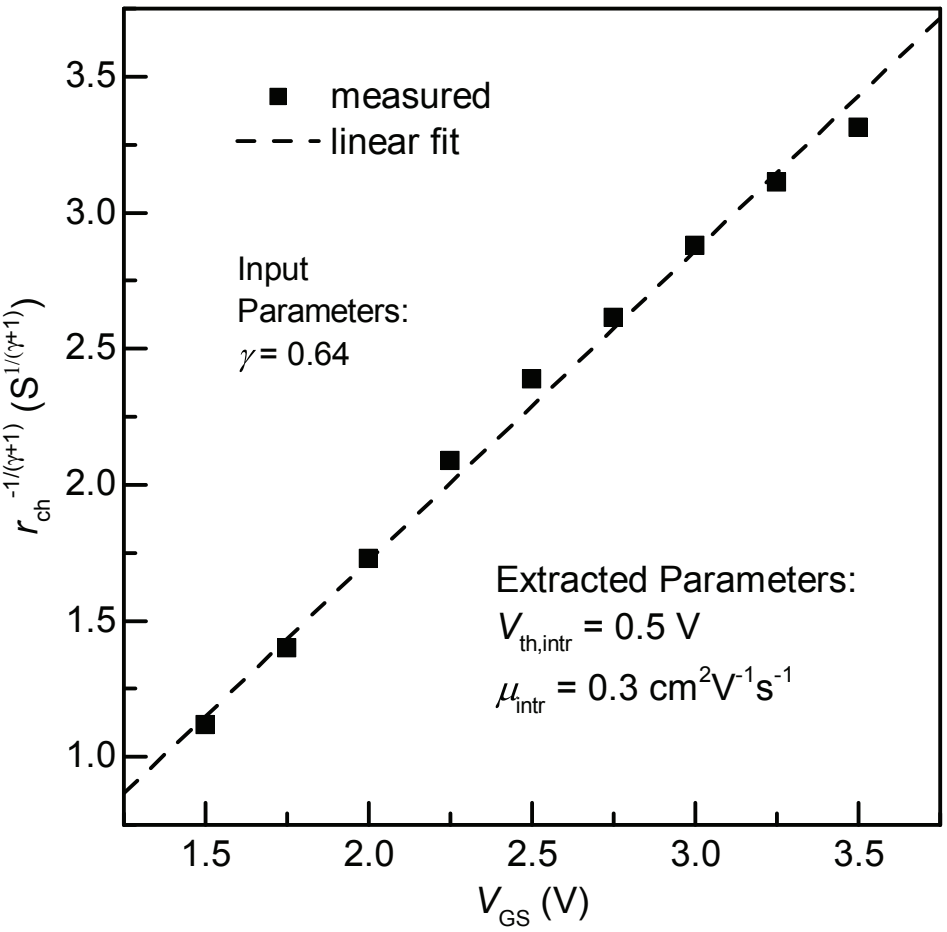

Figure 5.7: Linearised r_{ch} function versus V_{GS} extracted from the TLM . The linear regression fit to $r_{ch}^{\frac{-1}{\gamma+1}}$ (dashed line) is overlaid on the measured data (symbols).

symmetrical S/D-overlapped ZnO TFTs with Au/Au S/D contacts were also simultaneously fabricated on the same sample to analyse the properties of the Au/ZnO contact, which are employed for the upcoming asymmetrical structures. $I-V$ characteristics of a typical Au/Au TFT, with the same dimensions as the Ru/Ru TFT presented earlier, are shown in Fig. 5.8. Compared to the Ru/Ru TFT's I_{on} in Fig. 5.4 that reached 0.06 A/m at $V_{GS} = 3.5$ V, the Au/Au TFT's I_{on} was much higher displaying 14 A/m at the same conditions. Moreover, the Au/Au devices' V_{th} were not within the measurement range making them unable to be easily modelled with the TFT generic charge drift model. As revealed by the experiments performed in the previous chapter, the Au metal surface induces a much lower R_C and higher electron concentrations in the ALD ZnO, which would manifest into the higher observed I_{on}. Furthermore, there was evidence that the post-fabrication hot-plate anneal (60 min at 150°C) also contributed a major role in reducing the contact resistance of the Au bottom contacts. To characterize the R_C of the Au bottom contacts, the TLM was again utilized on symmetrical S/D-overlapped Au/Au TFTs using the same procedure as with the Ru/Ru TFTs. Fig. 5.9(a), (b) contains plots of the extracted $R_{on}W$ and R_CW as a function of L from two sets of Au-source devices without and with hot-plate annealing. According to the TLM results, the post-fabrication anneal dramatically reduced the Au's R_CW; the annealed contacts' R_CW was $\sim$ 28 k$\Omega\mu$m at $V_{GS} = 3$ V, which was much lower than the $\sim$ 2 M$\Omega\mu$m extracted from the non-annealed contacts. Hence, the hot-plate anneal induced a change in the chemistry at the Au/ZnO interface resulting in lower contact resistance; based on these results, it is also likely that the higher electron concentrations of the Au/ZnO structure is diffusion-related. The exact details regarding the mechanism behind this phenomena requires further inquiry however. Since the R_CW of the annealed Au was practically negligible compared to the R_CW extracted from the Ru contacts, the contact effects in the asymmetrical ZnO TFTs with bottom Ru source and Au drain contacts (that are presented hereafter) were attributed entirely to the Ru source electrode during device modelling.

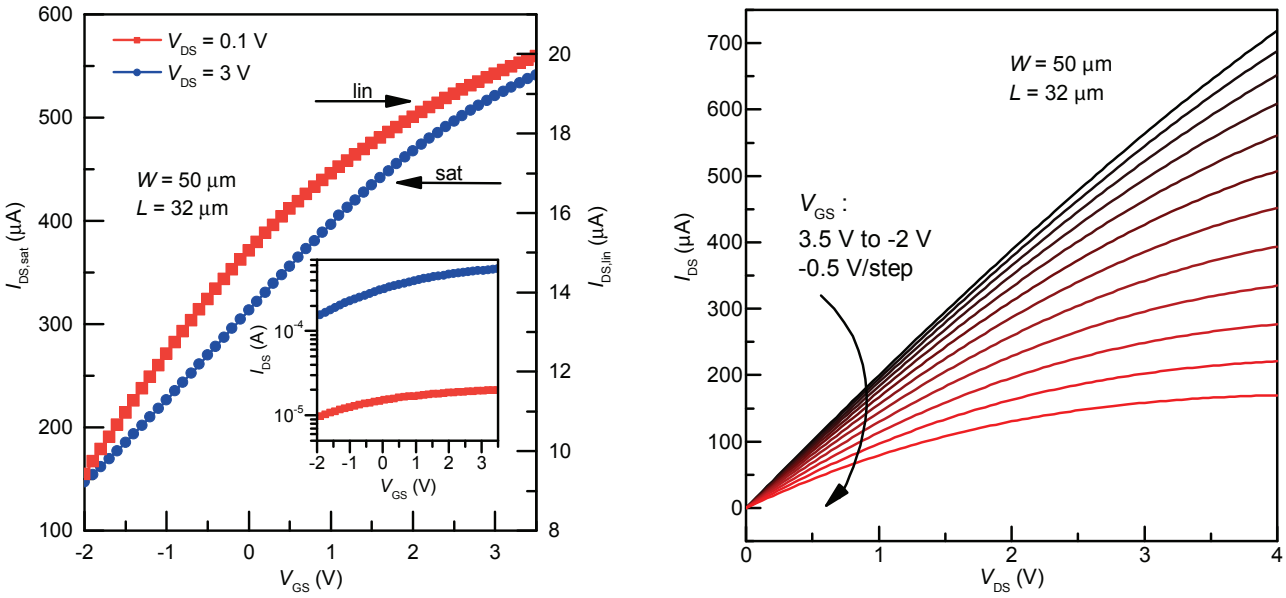

Figure 5.8: (a) Transfer characteristics of a symmetrical S/D-overlapped ZnO TFT with Au/Au S/D contacts where $W/L = 50\ \mu$m/32 μm at $V_{DS} = 0.1$ V (red squares) and 3 V (blue circles). The inset shows the same data in semi-log scale. (b) Output characteristics of the same device at V_{GS} increasing from -2 to 3.5 V in 0.5 V steps.

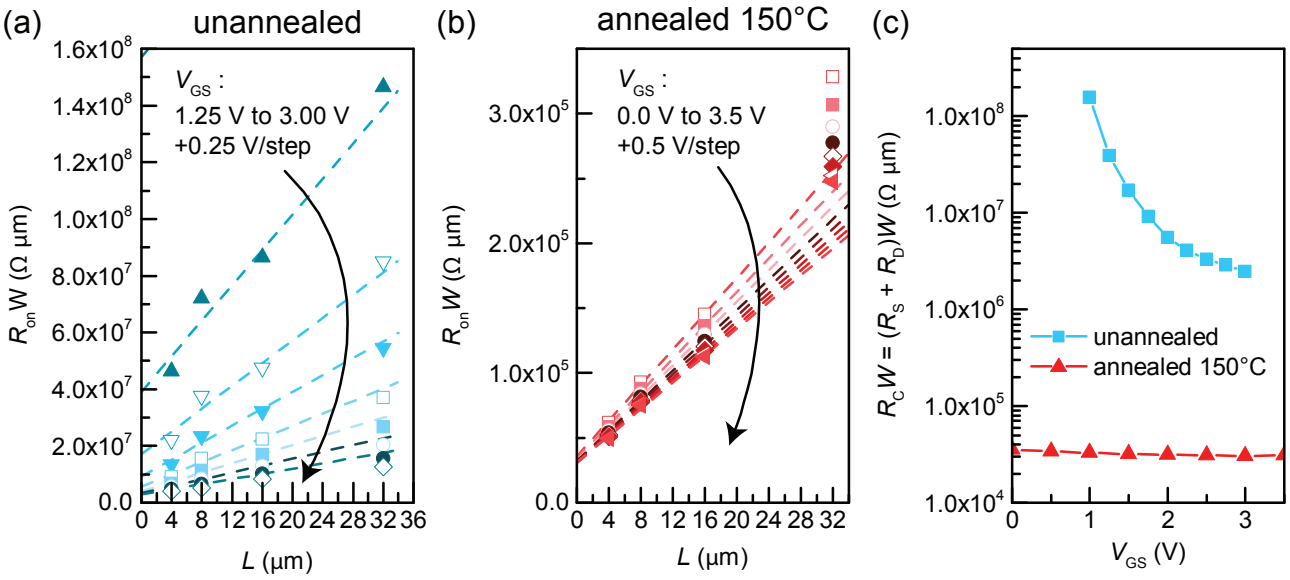

Figure 5.9: Width-normalised on-resistance ($R_{on}W$) versus L from a set of symmetrical S/D-overlapped top-gate ZnO TFTs with Au/Au S/D contacts (a) before annealing, where V_{GS} varies from 1.25 V to 3 V (increasing in 0.25 V steps from top to bottom), and another set (b) after hot plate annealing at 150°C for 60 min, where V_{GS} varies from 0 V to 3.5 V (increasing in 0.5 V steps from top to bottom). Linear regression fits to $R_{on}W$ for each V_{GS} step are shown by the overlaid dashed lines. (c) Width-normalised contact resistance as a function of V_{GS} in semi-log scale extracted by the TLM analysis displayed in (a) and (b). The hot-plate anneal noticeably reduced the contact resistance.

5.5 Asymmetrical S/D-overlapped Top-Gated ZnO TFTs with Ru Source and Au Drain Contacts

Despite the high drive current capabilities exhibited by the staggered Au/Au TFT in Fig. 5.8, its TFT characteristics are not well-suited for most electronics applications as the devices do not turn off even at $V_{GS} = -2$ V. Additionally, the Au/Au TFT's suffer from low $I_{on/off}$ and large SS. A ZnO TFT that can retain the high current driving potential of the Au/Au TFTs without sacrificing its off-state characteristics, preferably with a positive V_{th} for enhancement-mode operation, would be more attractive. Therefore, as a means to improve the Ru/Ru TFTs' I_{on} and mobility without compromising their switching characteristics, asymmetrical S/D-overlapped ZnO TFTs with Ru source and Au drain (Ru/Au) bottom electrodes were fabricated concurrently with the previously presented devices. Typical transfer characteristics of an asymmetrical Ru/Au S/D-overlapped TFT with the same dimensions as the symmetrical Ru/Ru TFT (W/L = 50 μm/32 μm and L_{ov} = 10 μm) are plotted in Fig. 5.10. Contrary to the symmetrical Au/Au TFTs, the asymmetrical Ru/Au TFT has an obvious off-state featuring a SS of 0.55 V/decade and a maximum $I_{on/off}$ of 4.6×10^5. Using the conventional MOSFET equation (Equation 5.1), $V_{th} = -0.7$ V and $\mu_{sat} = 4.6$ cm^{2}V^{-1}s^{-1} were extracted from the transfer characteristics at V_{DS} = 3 V. Hence, the mobility and drive current dramatically improved, at the cost of a more negative V_{th} and slightly higher SS, by swapping the drain contact with Au.

There was also evidence that the Au contact increased the ZnO n-type doping concentration (N_D) at the drain region. From Equation 4.1, with the gate-to-drain capacitance (C_{GD}) and gate-drain voltage (V_{GD}) replacing C_{GS} and V_{GS} respectively, the slope of inverse of C_{GD} squared (C_{GD}^{-2}) versus V_{GD} during the transition from depletion to accumulation is inversely proportional to the ZnO N_D (once again, the effective area was assumed to be equal to $W \times L_{ov} = 500$ μm^2) [129]. Thus when each TFT's C_{GD}^{-2} was plotted as a function of V_{GD}, which is presented in Fig. 5.11, it was evident that ZnO's N_D around the drain was affected by the S/D metallization with the symmetrical Ru/Ru TFT exhibiting

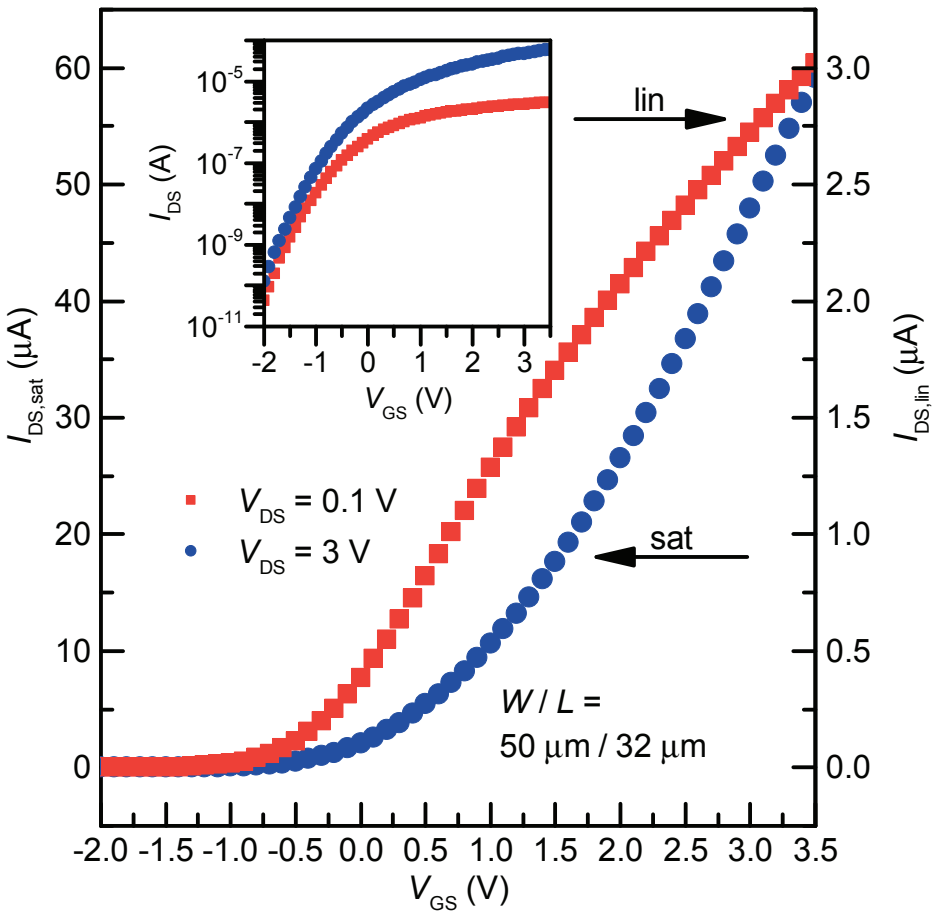

Figure 5.10: Transfer characteristics of an asymmetrical S/D-overlapped ZnO TFT with Ru source and Au drain electrodes where $W/L = 50\ \mu$m/32 μm at $V_{DS} = 0.1$ V (red squares) and 3 V (blue circles). The inset shows the same data in semi-log scale.

the lowest N_D ($\sim 1 \times 10^{18}$ cm^{-3}). Surprisingly, the N_D of the Ru/Au ($\sim 8 \times 10^{18}$ cm^{-3}) and Au/Au ($\sim 4 \times 10^{20}$ cm^{-3}) devices were different despite having the same drain metallization suggesting that the ZnO N_D in the Au/Au TFT was higher throughout the entire channel (and not just localized at the drain). The larger N_D promoted by the Au drain contacts is beneficial for enhancing the tunnelling injection current (thus effectively lowering R_C) similar to the contact doping techniques commonly employed for Si-based MOSFETs [169]. Reducing the parasitic losses at the metal/ZnO interface alone can cause an apparent improvement in mobility (as the measured device mobility is only a fitting parameter rather than the intrinsic material property) [170]. But it was found in the previous chapter that the Au surface induced a distinct ZnO micro-structure (see Fig. 4.8 for details), which could have also impacted the device mobility. Presently, details of the Au/ZnO film structure's electronic properties are unknown, and further studies into the different ZnO micro-structures are required. For the ZnO TFTs with Au drain contacts, the higher N_D made the drive current difficult to modulate, and as a result, their SS degraded and V_{th} became more negative. To minimize SS, one of the key prerequisites is a fully depleted off-state [171]. As N_D increases, the ZnO depletion width (W_{dep}) becomes smaller making it challenging for the channel to fully deplete, especially when W_{dep} is less than the channel thickness. From the one-sided abrupt junction depletion approximation, the maximum depletion width ($W_{dep,max}$) is [45],

$$W_{dep,max} = \sqrt{\frac{4\varepsilon_S \psi_b}{qN_D}} \approx \sqrt{\frac{4\varepsilon_S k_B T \ln\left(\frac{N_D}{n_i}\right)}{q^2 N_D}} \tag{5.16}$$

where q is the elementary charge (1.6×10^{-19} C), and ε_S is the permittivity of ZnO ($8.5 \times 8.85 \times 10^{-12}$ F·m^{-1}); $\psi_b \approx \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right)$ is the difference between the Fermi level and intrinsic Fermi level, where k_B is the Boltzmann constant (1.38×10^{-23} J·K^{-1}), T is the temperature (in Kelvin), and n_i is the ZnO intrinsic doping level $\left(10^6 \text{ cm}^{-3} \text{ [172]}\right)$. For a channel thickness of 20 nm, $W_{dep,max}$ will be approximately the same thickness as the channel at $N_D \approx 3.5 \times 10^{18}$ cm^{-3}. Consequently, any TFT that employed a Au bottom contact would have trouble fully depleting (based on the N_D extracted from the devices' C_{GD}^{-2}-V_{GD} characteristics). Nonetheless, the trade-offs (in V_{th}, I_{off}, and SS) to attain a higher

I_{on} and mobility with the asymmetrical S/D layout (from replacing Ru with Au at the drain electrode) were not as detrimental as when both S/D contacts were switched to Au. This implies that most of the device behaviour is still governed by the source electrode.

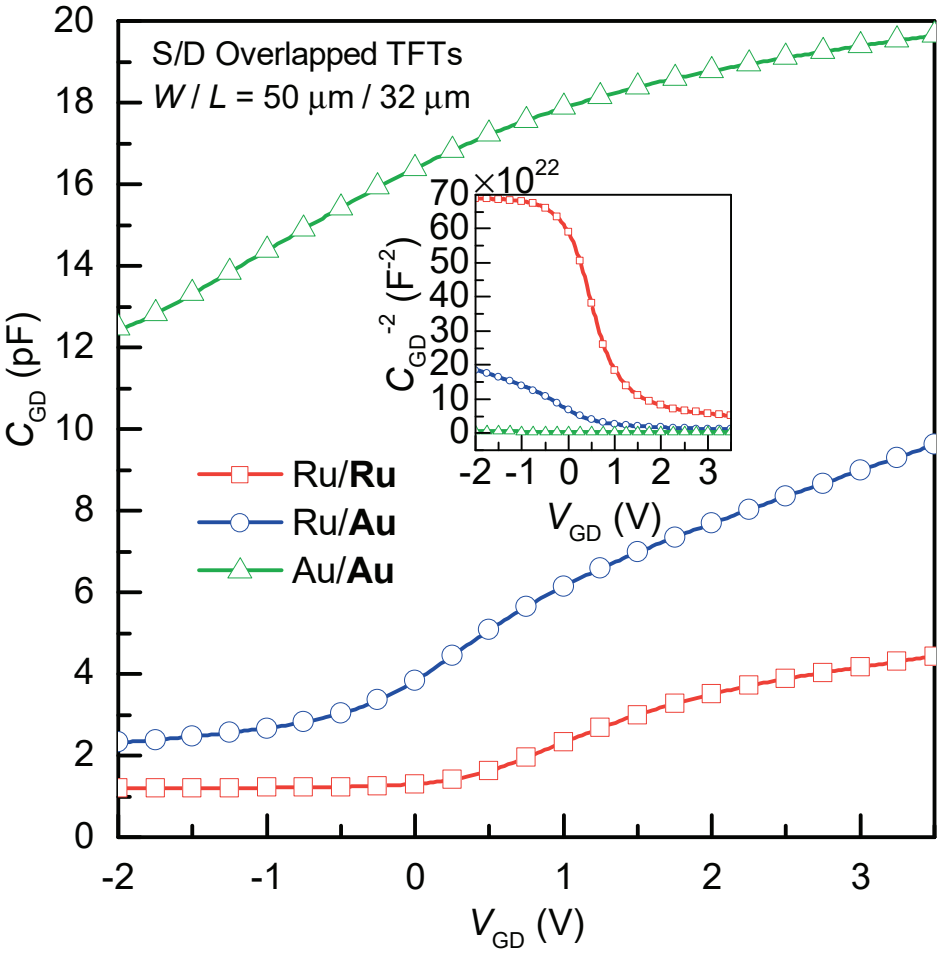

Figure 5.11: C_{GD} as a function of V_{GD} at zero V_{DS} for S/D-overlapped top-gated ZnO TFTs utilizing Ru/Ru (red squares), Ru/Au (blue circles), and Au/Au (green triangles) S/D contacts at 1 MHz. The source contact was floating during measurement, and the drain metal of interest is bolded in the legend. Inset: Reciprocal of C_{GD} squared versus V_{GD}. The slope of the linear transition from depletion to accumulation is inversely proportional to the ZnO doping concentration.

Modelling the asymmetrical S/D-overlapped ZnO TFTs was accomplished

using the same procedure as with the symmetrical TFTs apart from that the Au drain electrode's contact resistance (R_D) was neglected. As a result, the asymmetrical TFTs' contact effects were assumed to be originating entirely from the source electrode. The H_{VGS} function of the TFT in Fig. 5.10 (using an input V_{th} of -0.55 V) is displayed in Fig. 5.12(a). For these class of TFTs, the current did not completely saturate before $V_{DS} = 4$ V after $V_{GS} \sim 2.5$ V meaning that the top expression in Equation 5.10 is not accurate after that V_{GS} threshold. From the slope of H_{VGS} versus V_{GS}, a value of $\gamma = 0.0$ was extracted revealing that there was no discernible V_{GS} dependence of μ in the V_{GS} range measured likely because of the much larger drive currents and negative V_{th}. The extracted V_{th} from the x-intercept of the linear fit to H_{VGS} did not converge to an accurate value during parameter verification. Instead, it was found that $V_{th} = -0.55$ V matched the re-simulated output characteristics with the measured data. The linearised Y_{VGS} function versus V_{GS} is shown in Fig. 5.12(b), and $\mu_o = 7.1$ cm^{2}V^{-1}s^{-1} was extracted from its slope. Finally, the device's R_C, which was assumed to be dictated entirely by R_S, is displayed in Fig. 5.12(c). At $V_{GS} = 3.5$ V, R_C trends towards 11 kΩ, which is around the value extracted from the symmetrical Ru/Ru TFTs supporting the assumption that the Au electrode does not contribute much to R_C. After parameter verification, it was found that $R_S = 9.5$ kΩ matched the measured $I - V$ curves better.

The simulated output characteristics overlaid on the experimental data is given in Fig. 5.13. Once again, the single TFT extraction method was capable of producing values for the TFT generic charge drift model that resulted in a close match to the measured $I-V$ characteristics (featuring a calculated mean percent difference of 5.2% in the after-threshold regime). Based on the extracted parameter values, which are summarized in Table 5.1, the main effects of substituting Ru with Au at the drain electrode were an improvement of the device mobility and I_{on} with the compromise of making V_{th} more negative and increasing SS. The influences of R_C on the TFT characteristics can also be entirely accounted for by the contact resistance at the Ru source electrode only. Thus, the asymmetrical S/D contact architecture is an easy, yet effective way to improve TFT on-state performance without diminishing the off-state characteristics adversely.

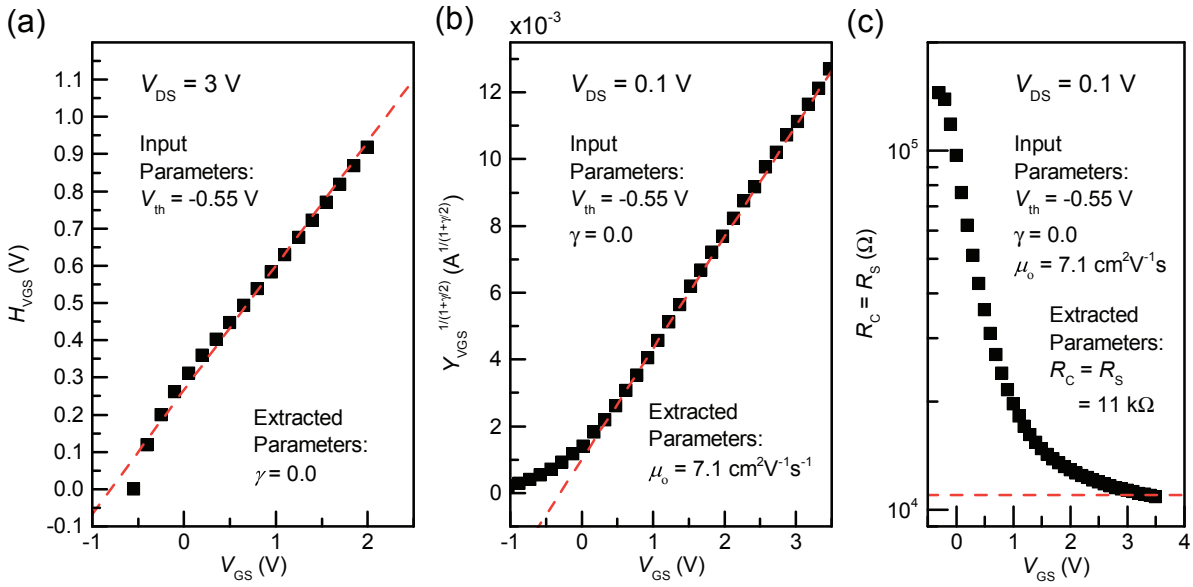

Figure 5.12: Modified $I-V$ characteristics for parameter extraction from an asymmetrical S/D-overlapped ZnO TFT with Ru source and Au drain contacts where W/L = 50 μm/32 μm. (a) H_{VGS} versus V_{GS} at V_{DS} = 3 V calculated with an input of $V_{th} = -0.55$ V. The linear regression fit used to extract γ is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at V_{DS} = 0.1 V. The linear regression fit used to extract μ_o is shown by the dashed line. (c) Contact resistance at the S/D terminals ($R_C = R_S$) calculated from the transfer characteristics at V_{DS} = 0.1 V plotted in semi-log scale. The average R_C at moderate $V_{GS} > V_{th}$ is shown by dashed line.

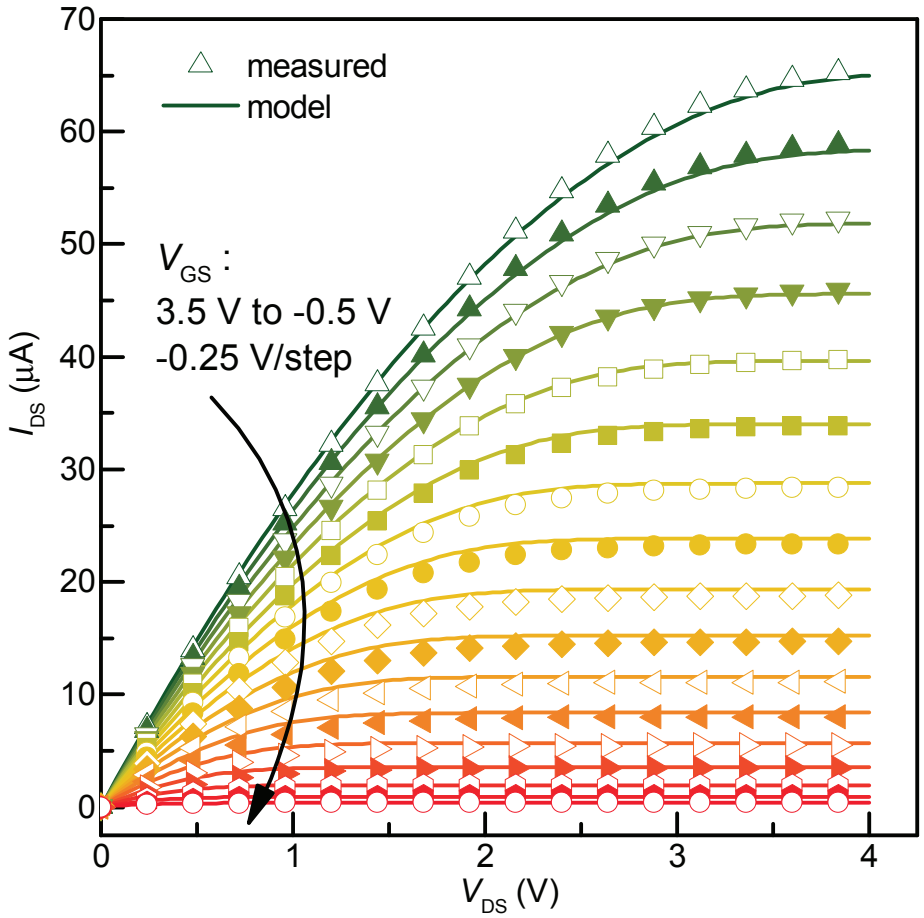

Figure 5.13: Output characteristics of an asymmetrical S/D-overlapped ZnO TFT with Ru source and Au drain contacts where $W/L = 50\ \mu$m/32 μm. V_{GS} is increasing from -0.5 V to 3.5 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

5.6 Asymmetrical Drain-offset Top-Gated ZnO TFTs with Ru Source and Au Drain Contacts

The S/D-overlapped TFTs were prone to breakdown when V_{DS} surpassed $\sim$ 5 V at high V_{GS} making them unsuitable for applications that require high drive voltage operation. A simple solution to overcome this limitation is to insert an un-gated offset region between the gate-and-drain to create so-called drain-offset TFTs as illustrated by Fig. 5.1(c) [142, 118, 173]. At the cost of decreased device mobility and I_{on}, the drain-offset structure enables high V_{DS} operation and improved V_{BD} capabilities by dropping the majority of V_{DS} across the intrinsic offset region, as demonstrated by the bottom titanium tungsten (TiW) source, top aluminium (Al) drain-offset SGTFTs featured in Chapter 3. The absence of a gate-to-drain overlap also lowers the TFT's C_{GD}, which is beneficial for improving circuit speeds [174, 175]. In a drain-offset TFT, the device physics of the gated and offset regions are different. Current flow in the un-gated intrinsic offset region is primarily restricted by space-charge limited current (SCLC) where I_{DS} is proportional to V_{DS} squared [176, 173, 119]. The space-charge effect occurs because the concentration of injected carriers from the channel is much greater than the equilibrium value in the intrinsic offset region [45]. Hence, non-linear $I - V$ characteristics are typically observed in drain-offset TFTs at low V_{DS}. In the gated region, current flow occurs in a thin accumulation channel at the semiconductor/gate insulator interface and adheres to the GCA like in the conventional TFT. When V_{DS} is high enough for I_{DS} to saturate, pinch-off occurs at the gate edge before the drain-offset rather than at the drain electrode. Any additional V_{DS} is then steadily dropped across the offset region, which reduces the effective V_{DS} at the channel edge keeping the gated channel approximately at V_{GS} [173, 119, 177]. Effectively, the behaviour of the drain-offset TFT can analysed as a gate-controlled channel region connected in series with a resistive intrinsic offset region. Using this interpretation, the TFT generic charge drift model by Marinov *et al.* can easily be adapted for the drain-offset structure by adding a series parasitic element before the drain (R_{GD}) as illustrated by the equivalent

circuit diagram in Fig. 5.1(f). In the upcoming sections, asymmetrical drain-offset ZnO TFTs with the same W/L (50 μm/32 μm) and source-side L_{ov} (10 μm) while varying L_{GD} from 0 to 30 μm were fabricated and then modelled with the TFT generic charge drift model. Note that L for these drain-offset devices is still defined as the distance between the S/D and therefore includes L_{GD}.

Transfer characteristics in the linear and saturation regimes of a drain-offset, top-gate ZnO TFT with Ru source and Au drain contacts where $L_{GD} = 0$ μm is presented in Fig. 5.14. Using the conventional TFT equation, μ_{sat} and V_{th} were extracted to be 1.1 $cm^2V^{-1}s^{-1}$ and 1.4 V respectively from the transfer characteristics during saturation ($V_{DS} = 6$ V). In addition, the TFT featured a high $I_{on/off}$ ($> 1 \times 10^6$) and low SS (~ 0.1 V/decade). Compared to the asymmetrical S/D-overlapped TFT in Fig. 5.10, there was a prominent reduction in μ_{sat} and I_{on}, which decreased by ~ 17 times at $V_{GS} = 3.5$ V, from removing the gate-to-drain overlap. On the other hand, the switching performance improved as I_{off} and SS also decreased indicating that the drain-offset TFTs were fully depleted; this was facilitated by the un-gated region's lower N_D and is described in the following paragraphs. Since the offset region in this particular device was basically negligible, the removal of the gate-to-drain overlap presumably diminished the electric field at the channel edge enough to substantially alter the TFT characteristics. Particularly, the maximum V_{DS} before breakdown was much higher than the ~ 5 V exhibited by the S/D-overlapped structures and exceeded 10 V without needing $L_{GD} > 0$ μm. According to two-dimensional (2-D) cross-sectional device simulations of drain-offset TFTs reported in literature [178, 173, 179, 177], the drain-offset TFT behaviour can be primarily attributed to a voltage drop originating from the cumulative parasitic losses in the drain-offset and in the transition region after the gate edge, which is present even for $L_{GD} = 0$ μm. After the accumulation channel ends at the gate edge, the electron density rapidly decreases because of the un-gated channel's comparably lower residual N_D. Hence when $V_{DS} > 0$ V, this lower doped intrinsic region gets depleted and most of the applied voltage is dropped across here thereby reducing the effective V_{DS} that is seen by the channel. In the S/D-overlapped TFTs, the gate-to-drain overlap can accumulate carriers beyond the channel edge, and therefore there was no depletion until the accumulation channel itself pinches off. In another set of

devices, a 2 μm gate-to-drain overlap was enough for the S/D-overlapped TFTs' characteristics to re-emerge (and for drain-offset TFT's properties to disappear). For the case of $L_{GD} = 0$ μm, the gate fringing fields were supposedly not strong enough to accumulate carriers beyond the channel, and consequently there was still a large potential spike at the gate edge [178, 173, 177].

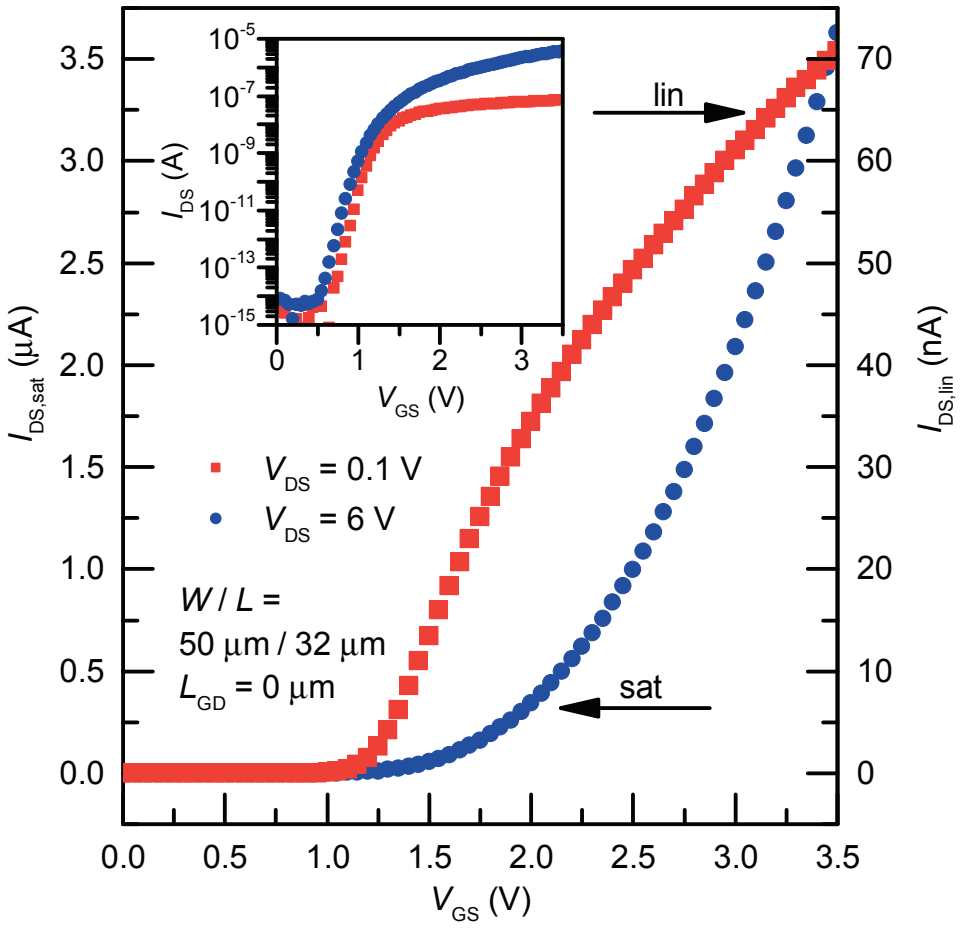

Figure 5.14: Transfer characteristics of an asymmetrical drain-offset ZnO TFT with Ru source and Au drain electrodes where $W/L = 50$ μm/32 μm and $L_{GD} = 0$ μm at $V_{DS} = 0.1$ V (red squares) and 6 V (blue circles). The inset shows the same data in semi-log scale.

Modelling of the asymmetrical drain-offset ZnO TFTs with the TFT generic charge drift model was accomplished using basically the same parameter extraction method besides some additional steps to account for the effects of the un-

gated offset region. Starting with the H_{VGS} function calculated from the saturation transfer characteristics at $V_{DS} = 6$ V, which is shown in Fig. 5.15(a), $\gamma = 0.4$ and $V_{th} = 1.1$ V were extracted from the slope and x-intercept of the linear fit to the curve respectively. Afterwards, the linear Y_{VGS} function at $V_{DS} = 0.1$ V, which is presented in Fig. 5.15(b), was used to extract $\mu_o = 0.7$ cm^{2}V^{-1}s^{-1} from its slope. The drain-offset devices' $V_{DS,sat}$ were much higher than the S/D-overlapped devices' (which is seen from the output characteristics plotted in Fig. 5.17 below for example) because of the voltage drop from the depletion of the un-gated offset region [178, 173]. To account for the higher $V_{DS,sat}$ in the TFT generic charge drift model, a series parasitic resistor, R_{GD}, was added in between the gate-and-drain. By doing so, the applied V_{DS} is reduced by $I_{DS} \times R_{GD}$ making the effective V_{DS} seen by the channel smaller (therefore delaying $V_{DS,sat}$). With the addition of R_{GD} to the model however, there is an extra degree of freedom that makes it difficult to separate R_S and R_{GD} from the calculated $R_C = R_S + R_{GD}$ shown in Fig. 5.15(c) (the resistance from the Au/ZnO interface at the drain electrode was once again ignored). To work around this problem, R_S was assumed to be equal to 13 kΩ, which was the value extracted from the symmetrical S/D-overlapped Ru/Ru TFTs. Afterwards, R_{GD} can be calculated from the difference between R_C and R_S.

In Fig. 5.15(c), the calculated R_C had a strong dependence on V_{GS} and is attributed to the fringing fields from the gate altering the Fermi level of the channel-to-offset transition region. Accordingly, a variable resistor element that is dependent on V_{GS} was employed to model R_{GD} instead of the constant resistor approach. Although not a problem for the $L_{GD} = 0$ μm device, current crowding from the SCLC in the offset region was too prominent at $V_{DS} = 0.1$ V and led to errors when calculating R_C and R_{GD} from the transfer curve measurements [see Fig. 5.19(c) for example]. Alternatively, non-linear curve fitting based on Equation 5.9 was utilized to calculate R_{GD} from the difference between the simulated and measured output characteristics' R_{on} in the linear regime at each V_{GS} step (where R_D is replaced with R_{GD} in Equation 5.9). The extracted R_{GD} versus V_{GS} for the $L_{GD} = 0$ μm device using this procedure is plotted in Fig. 5.16. From how R_{GD} decreased with V_{GS}, it was easy to fit R_{GD} to an empirical formula of

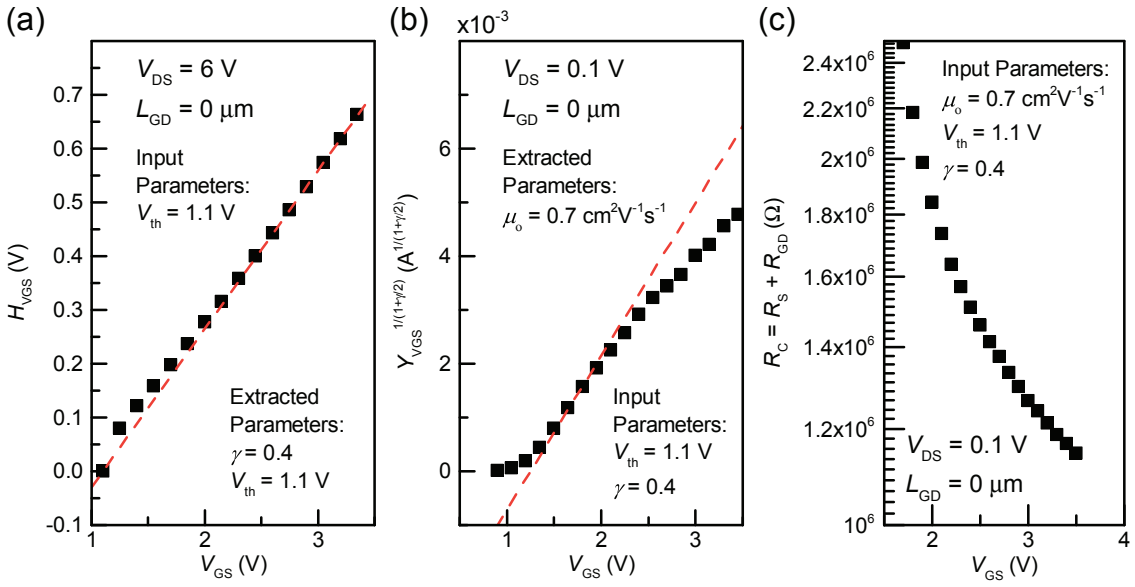

Figure 5.15: Modified $I-V$ characteristics for parameter extraction from an asymmetrical drain-offset ZnO TFT with Ru source and Au drain contacts where $W/L = 50\ \mu$m/32 μm and $L_{GD} = 0\ \mu$m. (a) H_{VGS} versus V_{GS} at $V_{DS} = 6$ V calculated with an input of $V_{th} = 1.1$ V. The linear regression fit used to extract γ and V_{th} is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at $V_{DS} = 0.1$ V. The linear regression fit used to extract μ_o is shown by the dashed line. (c) Contact resistance at the S/D terminals ($R_C = R_S + R_{GD}$) calculated from the transfer characteristics at $V_{DS} = 0.1$ V plotted in semi-log scale.

the form,

$$R_D \approx R_{GD} = \frac{R_{GD0}}{V_{GS} - V_{th}} \tag{5.17}$$

where R_{GD0} is a bias-independent fitting parameter. This empirical formula was able to accurately capture the V_{GS}-dependence of the extracted R_{GD} for all drain-offset devices tested. After determining R_{GD0}, which was extracted to be 1.3 MΩ, the output characteristics were simulated using Equation 5.9 with $R_D = R_{GD}$ (where R_{GD} was calculated from Equation 5.17). The simulated output characteristics overlaid on top of the measured data are plotted in Fig. 5.17. Both I_{sat} and $V_{DS,sat}$ match well with the experimental data (as the mean percent difference was 7.7%) indicating that drain-offset TFTs can be effectively simulated with the TFT generic charge drift model as well after adding R_{GD}. During re-simulation, R_{GD} had a limited effect on I_{sat}; instead, the drain-offset TFTs' lower on-state performance was accounted for mostly by R_S and μ_o. Using $R_S = 13$ kΩ along with the extracted γ, V_{th}, and μ_o values, the re-simulated I_{sat} matched well with the experimental measurements for any value of R_{GD} (until R_{GD} became large enough to change $V_{DS,sat}$). Hence, the two main roles of R_{GD} was to adjust the slope of the $I - V$ curves in the linear regime and to control $V_{DS,sat}$.

Starting with $L_{GD} = 2$ μm, drain-offset TFTs with increasing L_{GD} while keeping the other dimensions constant were also tested to discern L_{GD}'s effect on device performance. Comparing with the previous $L_{GD} = 0$ μm transistor, the $L_{GD} > 0$ μm devices demonstrated very similar behaviour except for larger $V_{DS,sat}$ values and a curvature in the output characteristics at low V_{DS}, which is the signature of SCLC [173, 119, 45]. The transfer characteristics in the linear and saturation regimes of a drain-offset TFT where $L_{GD} = 2$ μm are plotted in Fig. 5.18. From fitting the saturation transfer characteristics to the conventional MOSFET equation (Equation 5.1), μ_{sat} and V_{th} were extracted to be 1.1 $cm^2V^{-1}s^{-1}$ and 1.4 V respectively, which matched the $L_{GD} = 0$ μm device. At low L_{GD} values, the drain-offset TFTs' characteristics in saturation were consistent (which is seen by Fig. 5.21 presented below). However, the $L_{GD} = 2$ μm device's transfer curve at $V_{DS} = 0.1$ V suffered from current crowding at higher V_{GS} due to I_{DS} being restricted by the SCLC in the offset region. This current

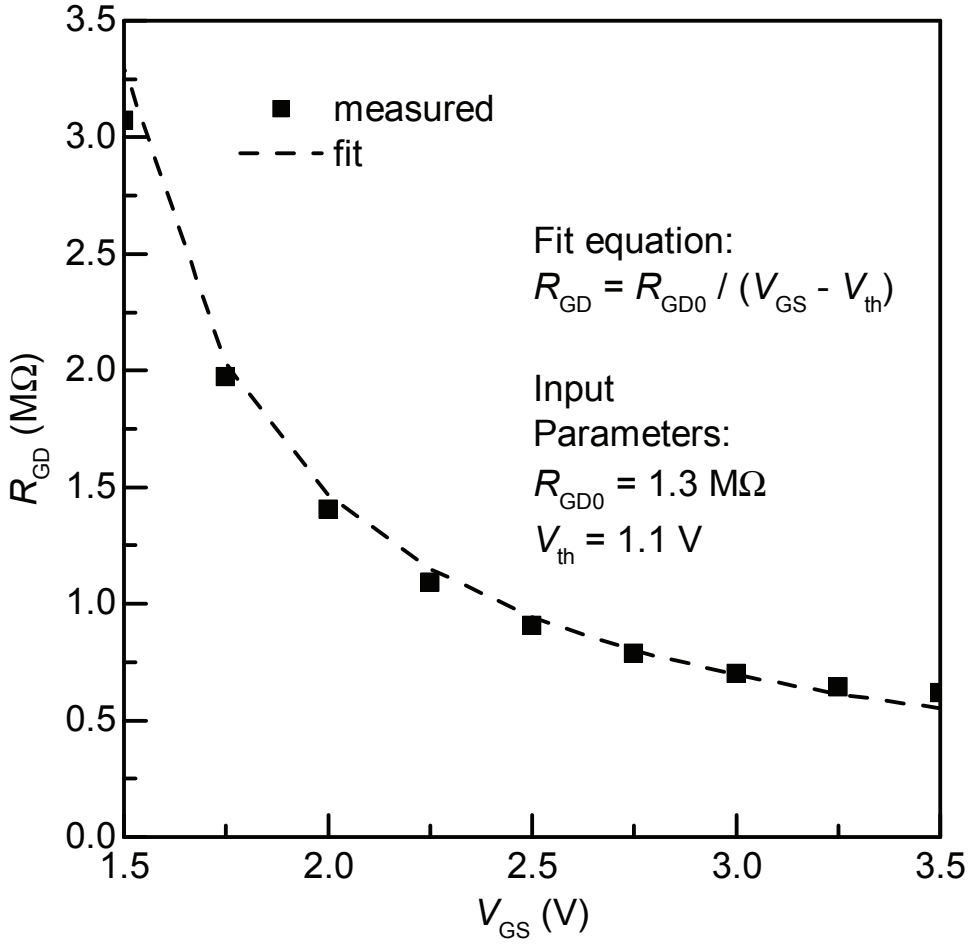

Figure 5.16: Extracted R_{GD} as a function of V_{GS} from an asymmetrical drain-offset ZnO TFT with Ru source and Au drain contacts where $W/L = 50$ μm/32 μm and $L_{GD} = 0$ μm. R_{GD} was extracted by fitting the linear regime of the output characteristics to the TFT generic charge drift model given by Equation 5.9. The extracted values (symbols) are fitted (dashed line) to the empirical formula shown above the plot.

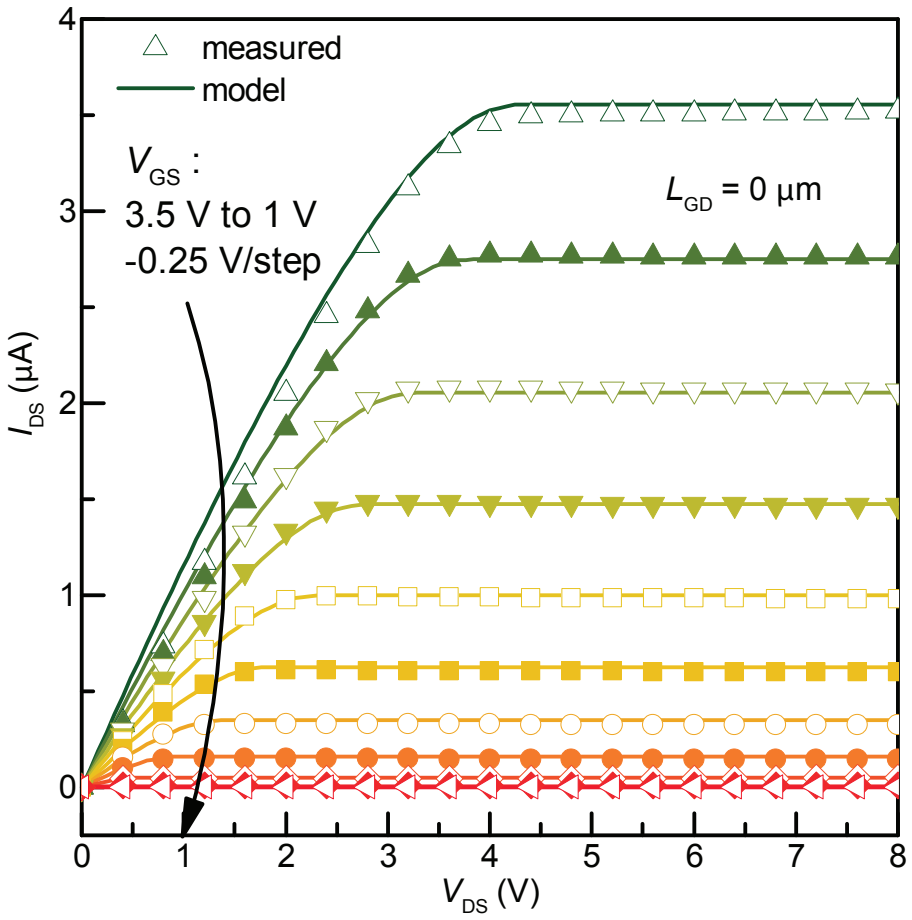

Figure 5.17: Output characteristics of an asymmetrical drain-offset ZnO TFT with Ru source and Au drain contacts where $W/L = 50\ \mu$m/32 μm and $L_{GD} = 0$ μm. V_{GS} is increasing from 1.0 V to 3.5 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

crowding was the reason why the R_{GD} extracted from the linear transfer curve was inaccurate.

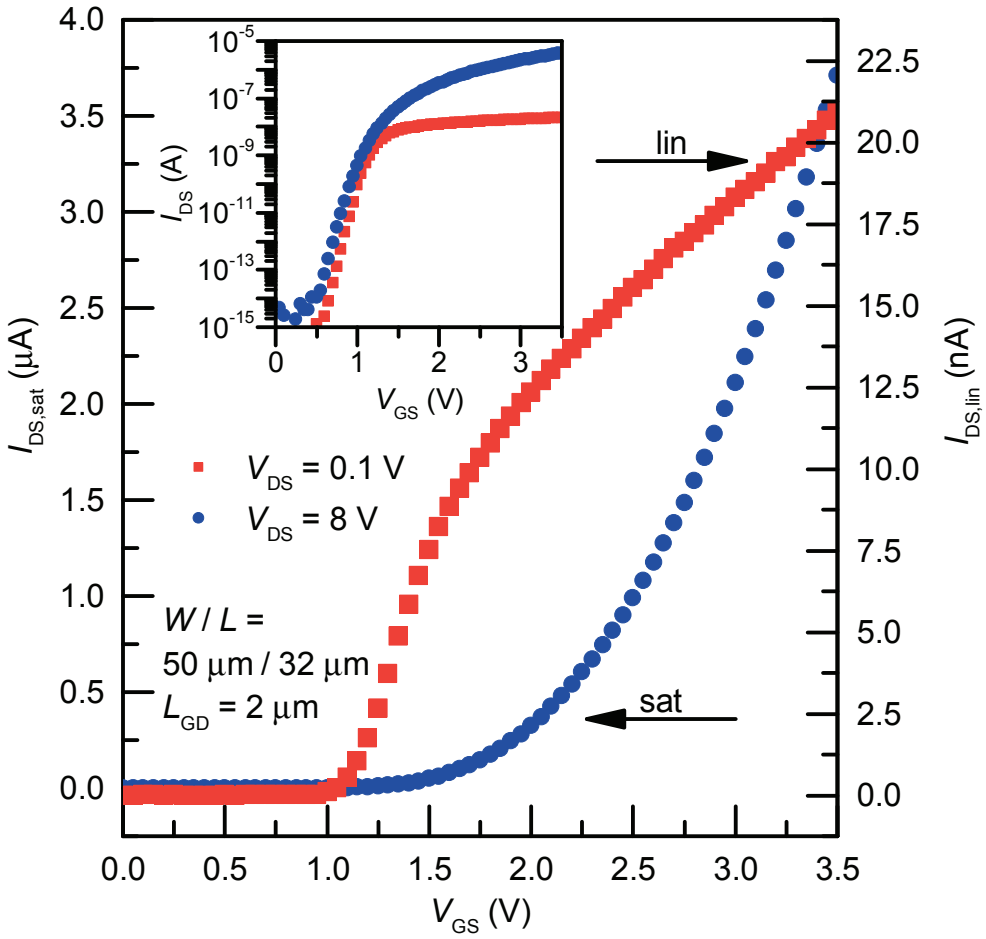

Figure 5.18: Transfer characteristics of an asymmetrical drain-offset ZnO TFT with Ru source and Au drain electrodes where $W/L = 50\ \mu m/32\ \mu m$ and $L_{GD} = 2\ \mu m$ at $V_{DS} = 0.1$ V (red squares) and 8 V (blue circles). The inset shows the same data in semi-log scale.

The $L_{GD} = 2\ \mu m$ device was modelled using the same approach as with the $L_{GD} = 0\ \mu m$ device by incorporating a V_{GS}-dependent resistor, R_{GD}, to model the drain-offset region. As shown by Fig. 5.19(a), $\gamma = 0.4$ and $V_{th} = 1.1$ V were extracted from the slope and x-intercept respectively of the linear regression fit to the device's H_{VGS} at $V_{DS} = 8$ V. Then the linearised Y_{VGS} function, displayed

in Fig. 5.19(b), was fitted with a straight line before current crowding appeared to extract $\mu_o = 0.69$ cm^{2}V^{-1}s^{-1}. Once again, R_S was assumed to be equal to the 13 kΩ extracted from the symmetrical S/D-overlapped Ru/Ru TFT, and the calculated R_C using the measured transfer characteristics at $V_{DS} = 0.1$ V was not used to extract R_{GD}. As was done with the previous device, R_{GD} was determined by fitting the output characteristics' linear regime to Equation 5.9 at each V_{GS} step. However, because R_{GD} was only a function of V_{GS}, this model unfortunately cannot reproduce the approximately quadratic relationship between I_{DS} and V_{DS} induced by the offset region's SCLC. Hence, the re-simulated output characteristics' mean percent differences increased in the $L_{GD} > 0$ μm devices (see Table 5.1 for details). If better accuracy in the linear regime is needed, the R_{GD} model needs to be expanded to include a dependency on V_{DS}. One approach could be to incorporate the SCLC's $I_{DS} \sim V_{DS}^2$ relationship at low V_{DS} and then transition into the standard TFT generic charge drift model through interpolation. Nevertheless, for this work, the main purpose of R_{GD} was to match the drain-offset TFTs' $V_{DS,sat}$, which the variable resistor model was capable of doing even without accounting for SCLC. The extracted R_{GD} as a function of V_{GS} was fitted to the empirical formula in Equation 5.17 resulting in a R_{GD0} value of 2.4 MΩ. Thus, the longer L_{GD} increased the effective parasitic resistance at the drain. The re-simulated output characteristics along with the experimental data are shown in Fig. 5.20. Besides not being able to replicate the curvature at low V_{DS}, the TFT generic charge drift model produced a close simulation to the drain-offset TFT's $I - V$ characteristics when $L_{GD} > 0$ μm as well.

As L_{GD} was increased further while keeping $L = 32$ μm constant, it was observed that for $L_{GD} \lessapprox 16$ μm, the asymmetrical drain-offset TFTs exhibited similar device characteristics. For instance, I_{on}, mobility, SS, V_{th}, and $I_{on/off}$ were all consistent wherein differences from device-to-device can be attributed to random processing variations. Evidently, for small L_{GD}, device performance remained mainly contingent on the gated channel region. Somewhere in-between $L_{GD} = 8$ and 16 μm however, I_{on} and mobility began to drop as L_{GD} increased. This can be ascribed to the offset region becoming the more dominant component of the drain-offset TFT. With longer L_{GD}, the offset region's SCLC rises less steeply with V_{DS}, and eventually the SCLC becomes the limiting factor on device

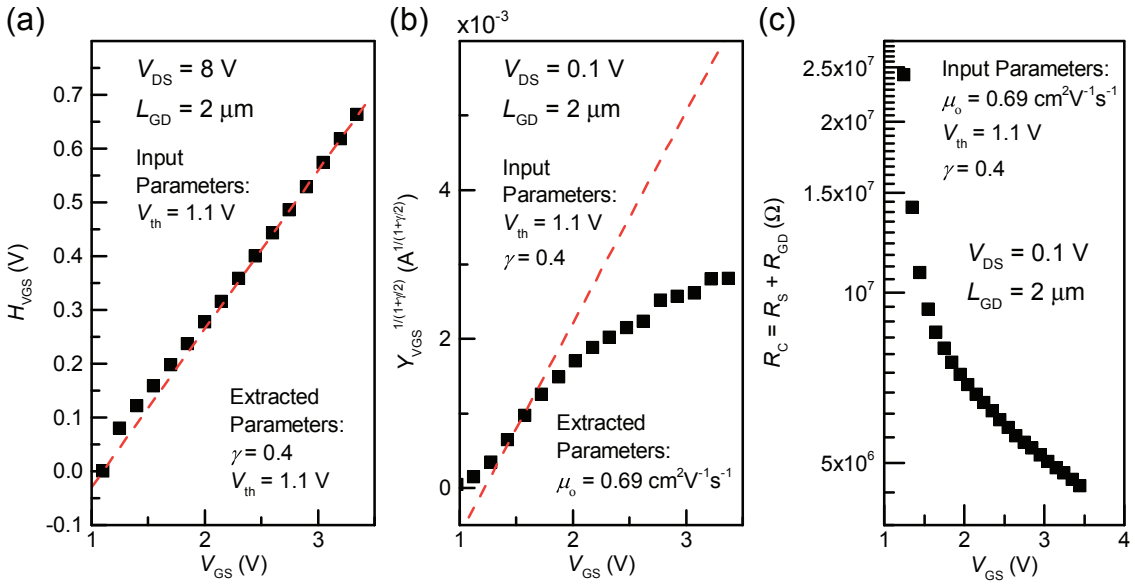

Figure 5.19: Modified $I-V$ characteristics for parameter extraction from an asymmetrical drain-offset ZnO TFT with Ru source and Au drain contacts where $W/L = 50\ \mu$m/32 μm and $L_{GD} = 2\ \mu$m. (a) H_{VGS} versus V_{GS} at $V_{DS} = 8$ V calculated with an input of $V_{th} = 1.1$ V. The linear regression fit used to extract γ and V_{th} is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at $V_{DS} = 0.1$ V. The linear regression fit used to extract μ_o is shown by the dashed line. (c) Contact resistance at the S/D terminals ($R_C = R_S + R_{GD}$) calculated from the transfer characteristics at $V_{DS} = 0.1$ V plotted in semi-log scale.

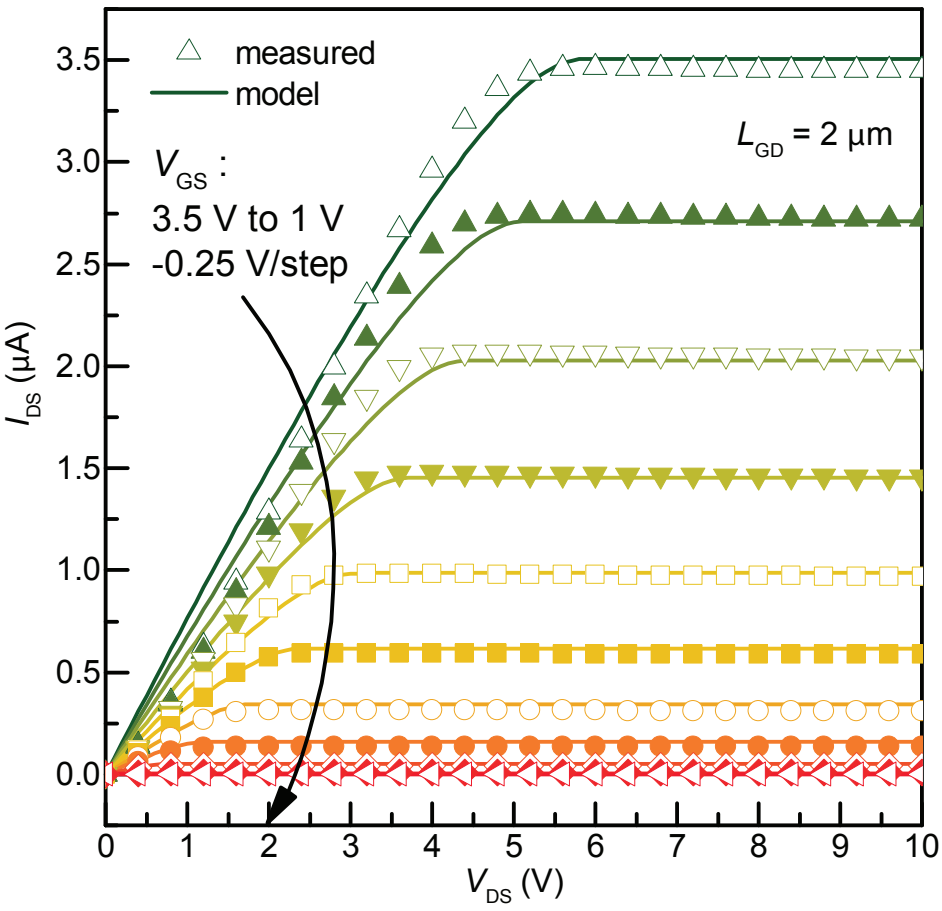

Figure 5.20: Output characteristics of an asymmetrical S/D-overlapped ZnO TFT with Ru source and Au drain contacts where $W/L = 50$ μm/32 μm and $L_{GD} = 2$ μm. V_{GS} is increasing from 1.0 V to 3.5 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

performance (as seen by the $L_{GD} = 16$ μm device presented below). From Fig. 5.21, which depicts the output characteristics of multiple drain-offset devices with $L_{GD} = 0$, 2, 8, and 16 μm on the same plot, it is apparent that L_{GD} has the greatest effect on the transistor's $V_{DS,sat}$. As mentioned before, increasing L_{GD} reduces the effective V_{DS} seen by the gated channel therefore delaying $V_{DS,sat}$ and increasing the maximum V_{DS} before breakdown. These set of devices' exact breakdown voltages were not measured but they are expected to be > 20 V when $L_{GD} > 2$ μm. Drain-offset devices with $L_{GD} = 24$ and 30 μm were also tested but no current modulation was observed, and I_{DS} did not saturate. When L_{GD} approaches L, the effective gated channel length is very small and $<< L_{GD}$; therefore, I_{DS} is predominantly dictated by a combination of the offset region's SCLC (especially at high V_{GS} where the accumulation channel's carrier densities are larger) and short-channel effects.

The ZnO drain-offset TFTs where $L_{GD} = 8$ and 16 μm in Fig. 5.21 were also modelled with the TFT generic charge drift model via the standard procedure. As a reference, their measured transfer characteristics, calculated H_{VGS}, Y_{VGS}, and R_C functions, and re-simulated output characteristics are plotted in Fig. 5.22, 5.23, and 5.24 for the $L_{GD} = 8$ μm device, and Fig. 5.25, 5.26, and 5.27 for the $L_{GD} = 16$ μm device. A complete summary of the extracted parameter values for all modelled TFTs is displayed in Table 5.1. The drain-offset TFTs' extracted R_{GD} consistently increased with L_{GD} (at constant V_{GS}) as shown by the plot in Fig. 5.28. Moreover, the fitted R_{GD0} (from the empirical formula in Equation 5.17) plotted as a function of L_{GD} also displayed the same positive correlation. Therefore, if the dependence of R_{GD} on L_{GD} and V_{GS} is investigated further and captured by a mathematical formula, the modelling of drain-offset TFTs with the TFT generic charge drift model can be further simplified. Lastly, the drain-offset TFTs' C_{GD} plotted as a function of V_{GD} is given in Fig. 5.29. Overall, C_{GD} is relatively tiny when compared to the values displayed in Fig. 5.11 due to the removal of the overlap capacitance. These low C_{GD} values could be taken advantage of to increase TFT circuit speeds [174, 175]. The hump after $V_{GD} > 0$ V can be explained by the filling of traps at the semiconductor/insulator interface and/or in the polycrystalline ZnO itself as the gate's fringing fields accumulate carriers in the intrinsic offset region [173, 180]. Additional investigations into the

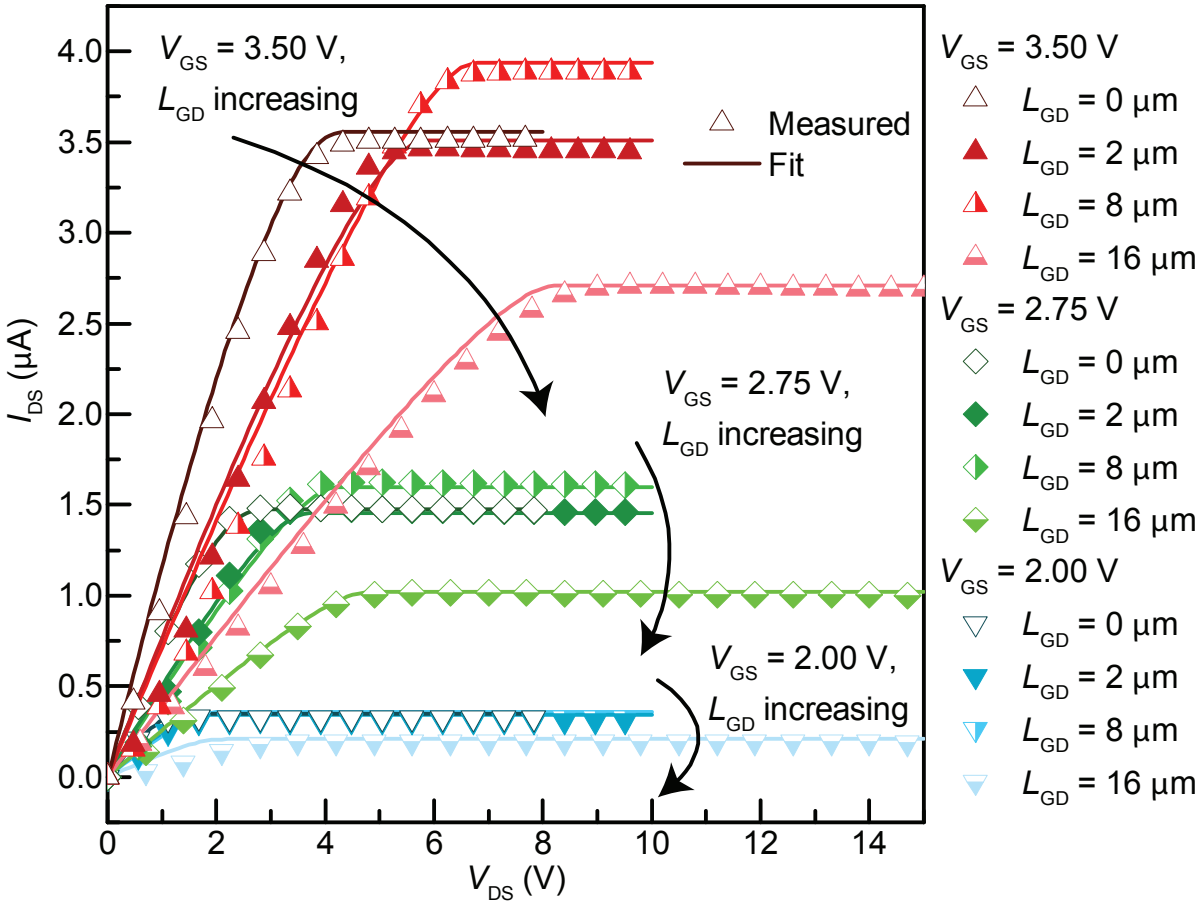

Figure 5.21: Output characteristics of multiple asymmetrical drain-offset ZnO TFTs with Ru source and Au drain contacts where $W/L = 50\ \mu$m/32 μm and $L_{GD} = 0, 2, 8$, and 16 μm. V_{GS} varies from 2.0 to 3.5 V in 0.75 V steps. Re-simulated output characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols) for each device.

drain-offset TFT's stability will be needed to ascertain the exact nature of this hump nonetheless.

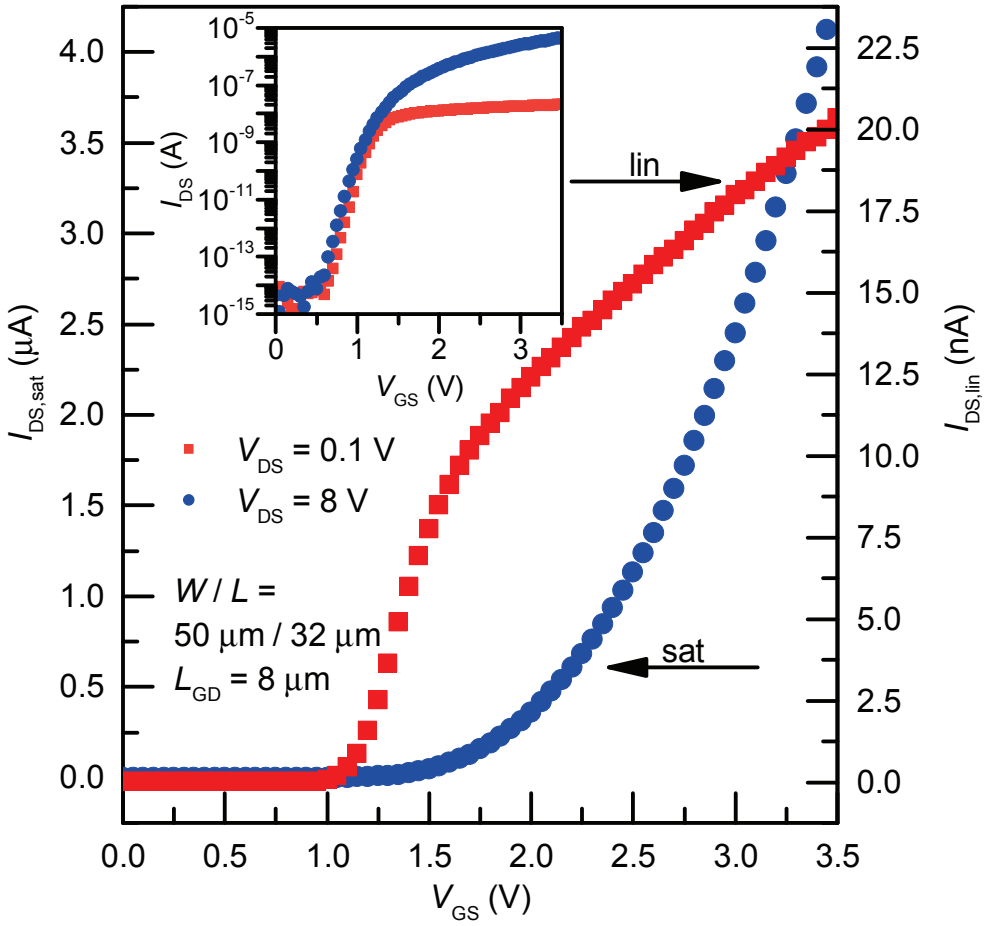

Figure 5.22: Transfer characteristics of an asymmetrical drain-offset ZnO TFT with Ru source and Au drain electrodes where $W/L = 50\ \mu$m$/32\ \mu$m and $L_{GD} = 8\ \mu$m at $V_{DS} = 0.1$ V (red squares) and 8 V (blue circles). The inset shows the same data in semi-log scale.

To counterbalance the non-linearity in the TFT's linear regime from SCLC, the carrier concentration in the offset region needs to be increased. Besides doping the offset region with donor species, a field plate over the drain-offset can also accomplish this task [119, 181]. A field plate is an additional metal-oxide-semiconductor structure that behaves as a secondary gate and is utilized to modify the device's electric field profile. For a top-gated drain-offset TFT, a simple

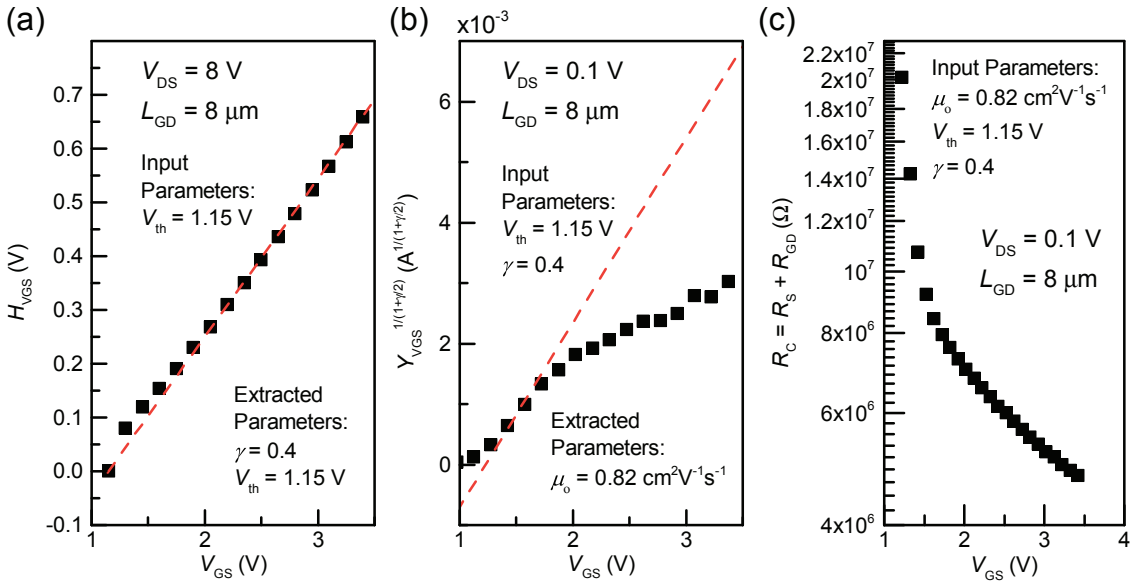

Figure 5.23: Modified $I-V$ characteristics for parameter extraction from an asymmetrical drain-offset ZnO TFT with Ru source and Au drain contacts where W/L = 50 μm/32 μm and L_{GD} = 8 μm. (a) H_{VGS} versus V_{GS} at V_{DS} = 8 V calculated with an input of V_{th} = 1.15 V. The linear regression fit used to extract γ and V_{th} is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at V_{DS} = 0.1 V. The linear regression fit used to extract μ_o is shown by the dashed line. (c) Contact resistance at the S/D terminals ($R_C = R_S + R_{GD}$) calculated from the transfer characteristics at V_{DS} = 0.1 V plotted in semi-log scale.

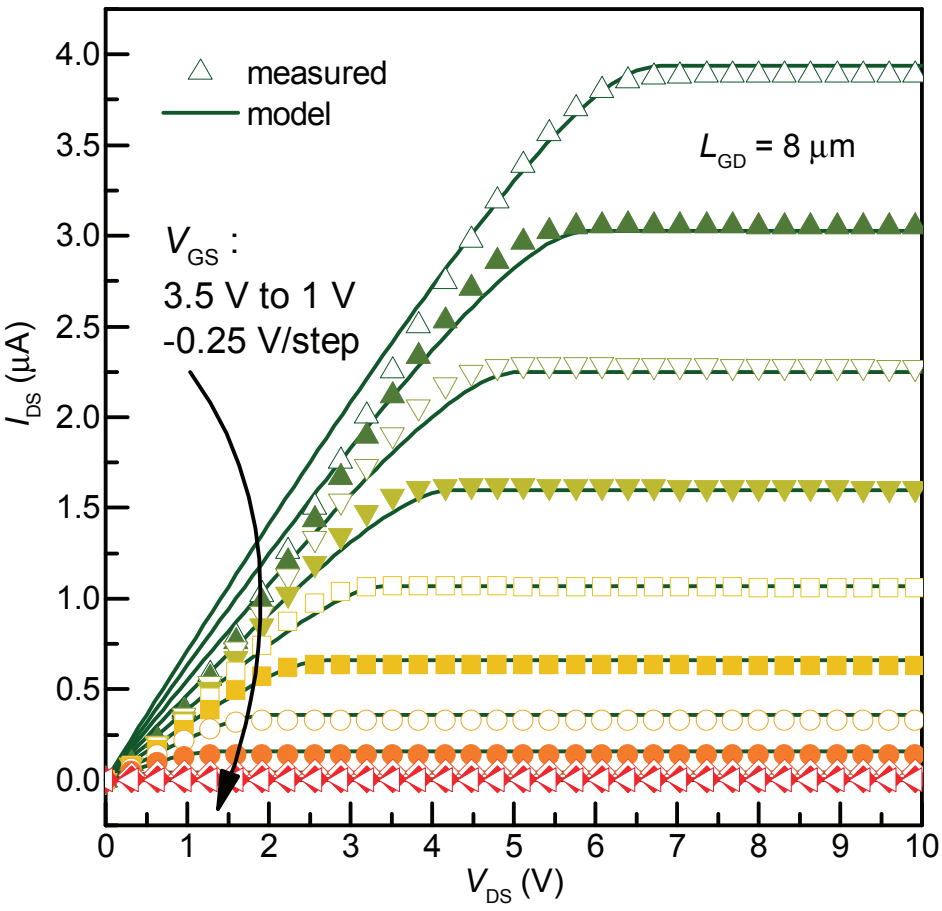

Figure 5.24: Output characteristics of an asymmetrical S/D-overlapped ZnO TFT with Ru source and Au drain contacts where $W/L = 50$ μm/32 μm and $L_{GD} = 8$ μm. V_{GS} is increasing from 1.0 V to 3.5 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

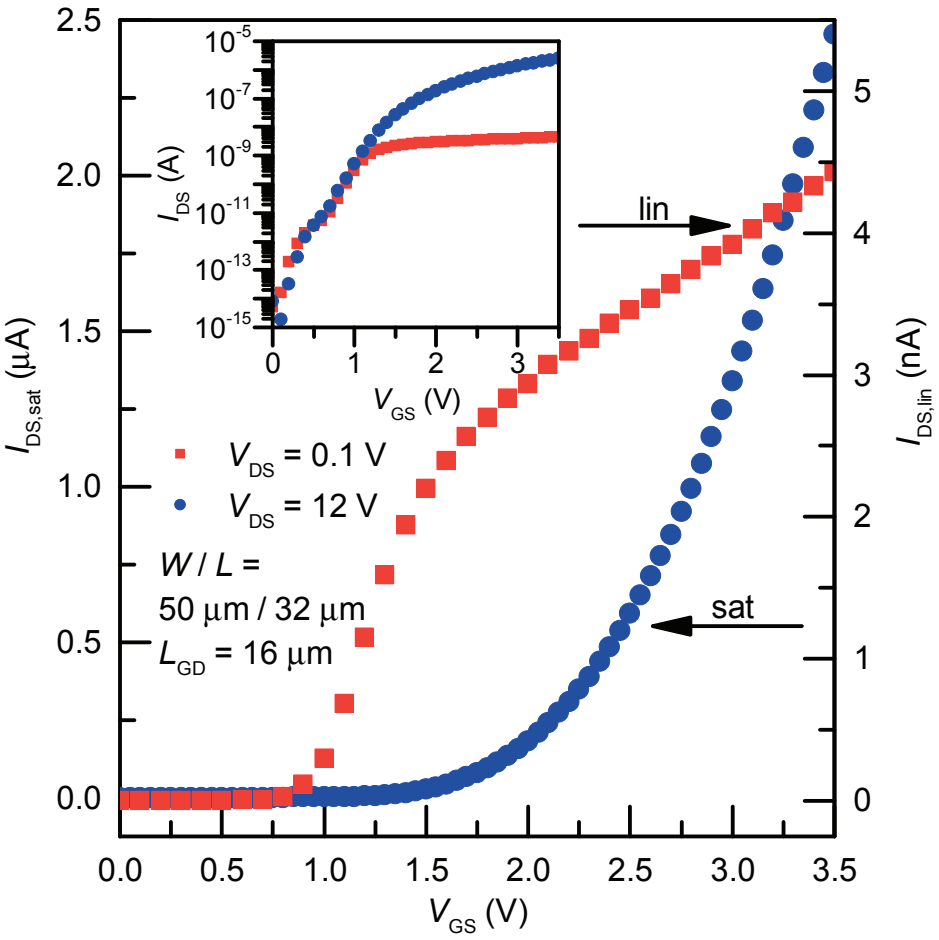

Figure 5.25: Transfer characteristics of an asymmetrical drain-offset ZnO TFT with Ru source and Au drain electrodes where $W/L = 50\ \mu$m/32 μm and $L_{GD} = 16\ \mu$m at $V_{DS} = 0.1$ V (red squares) and 12 V (blue circles). The inset shows the same data in semi-log scale.

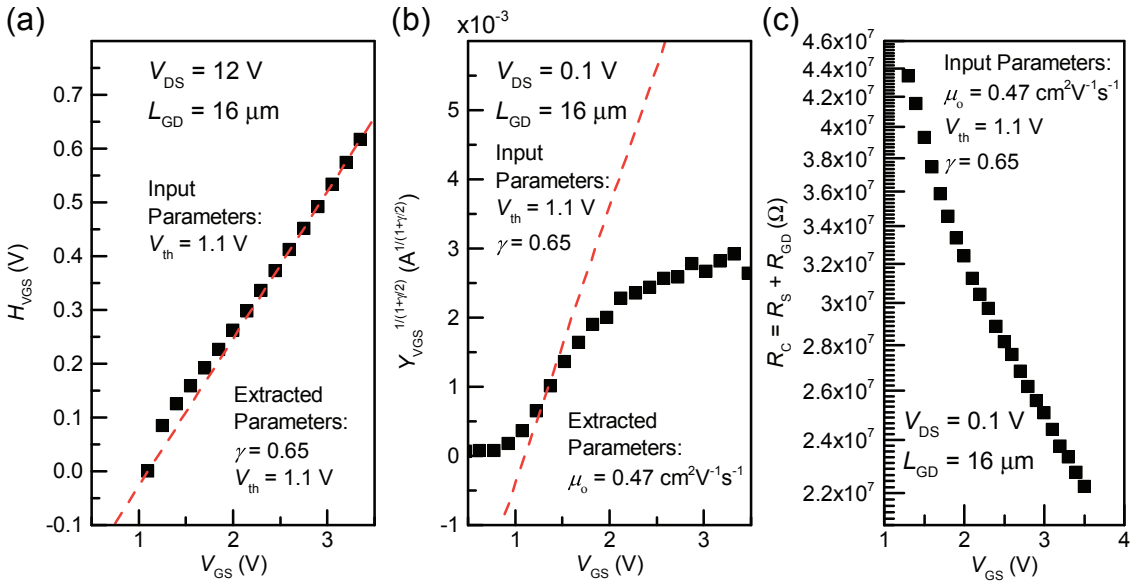

Figure 5.26: Modified $I-V$ characteristics for parameter extraction from an asymmetrical drain-offset ZnO TFT with Ru source and Au drain contacts where W/L = 50 μm/32 μm and L_{GD} = 16 μm. (a) H_{VGS} versus V_{GS} at V_{DS} = 12 V calculated with an input of V_{th} = 1.1 V. The linear regression fit used to extract γ and V_{th} is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at V_{DS} = 0.1 V. A dashed line with a slope of the final μ_o after parameter verification is also displayed. (c) Contact resistance at the S/D terminals ($R_C = R_S + R_{GD}$) calculated from the transfer characteristics at V_{DS} = 0.1 V plotted in semi-log scale.

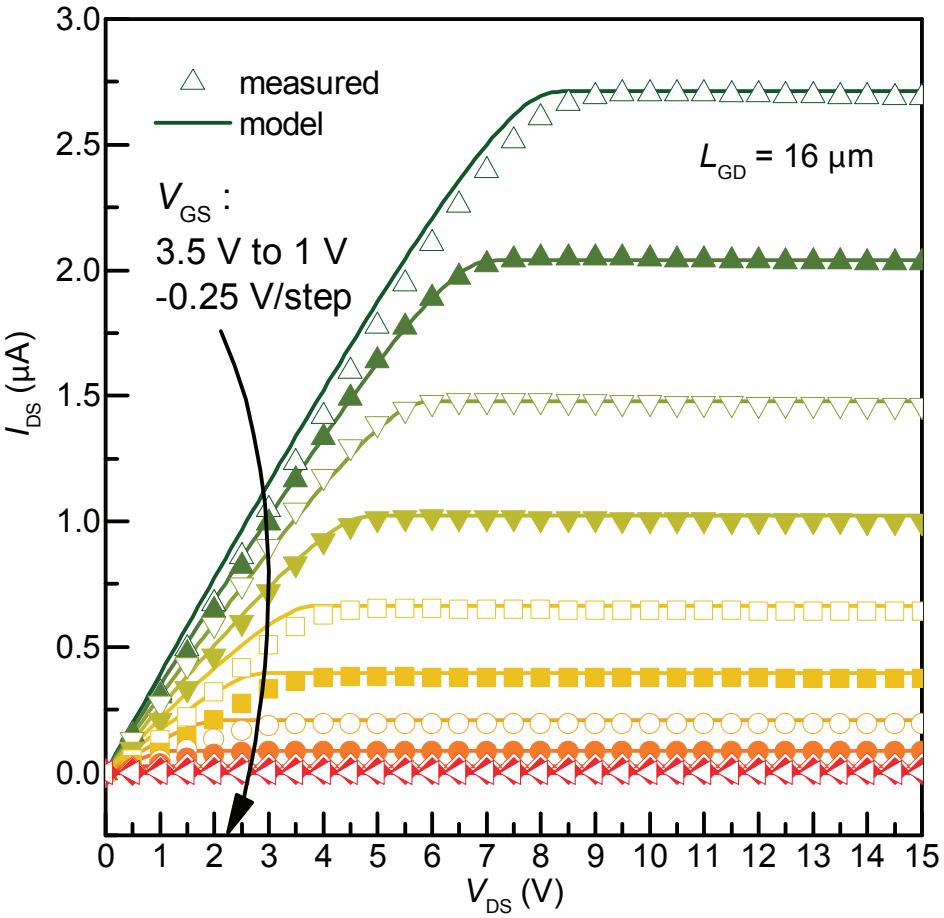

Figure 5.27: Output characteristics of an asymmetrical S/D-overlapped ZnO TFT with Ru source and Au drain contacts where $W/L = 50\ \mu$m$/32\ \mu$m and $L_{GD} = 16\ \mu$m. V_{GS} is increasing from 1.0 V to 3.5 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

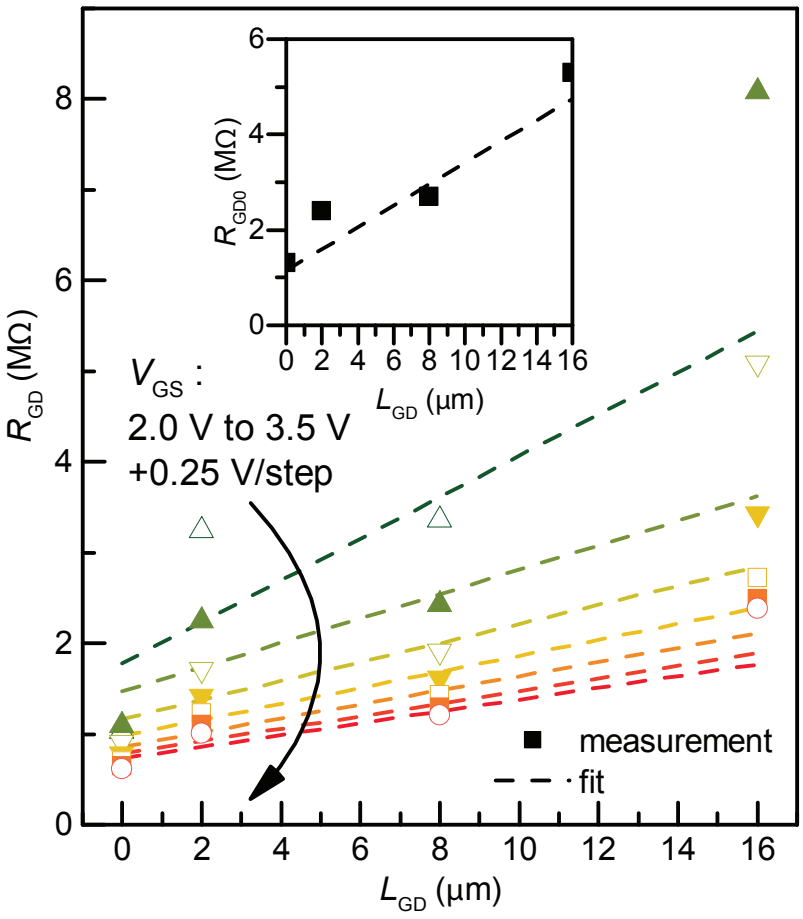

Figure 5.28: R_{GD} plotted as a function of L_{GD} extracted from the TFT generic charge drift model. Linear regression fits to R_{GD} for each V_{GS} step are shown by the overlaid dashed lines. The inset depicts the extracted R_{GD0}, from fitting R_{GD} to the empirical formula presented in Equation 5.17, plotted versus L_{GD} along with a linear regression fit to the data herein.

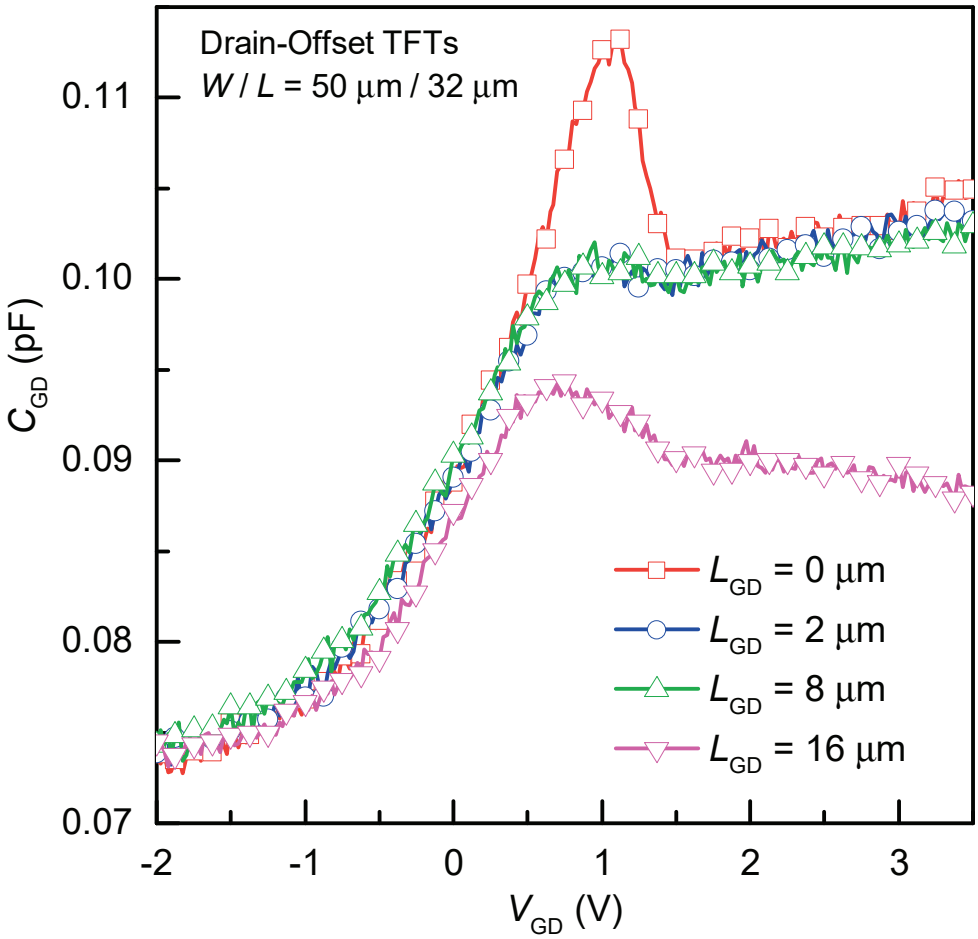

Figure 5.29: C_{GD} as a function of V_{GD} at zero V_{DS} for drain-offset top-gated ZnO TFTs utilizing bottom Ru source and Cr/Au drain contacts with varying L_{GD} at 1 MHz. The source contact was floating during measurement.

"T"-shaped gate where the primary gate is extended over the offset region with a thick dielectric spacer layer isolating the field plate from the rest of the device is sufficient [182] (see Fig. 5.30 for a conceptual schematic cross-section of a top-gated drain-offset TFT employing a "T"-shaped field plate). When the field plate is biased, the offset region is weakly accumulated and more free charges are available thus increasing the SCLC and mitigating the parasitic losses in the applied V_{DS} [119, 181]. As long as the field plate is isolated from the device by a thick dielectric layer, the gate insulator will not see a large field and the high voltage operation can be retained while simultaneously improving the TFT's on-state performance.

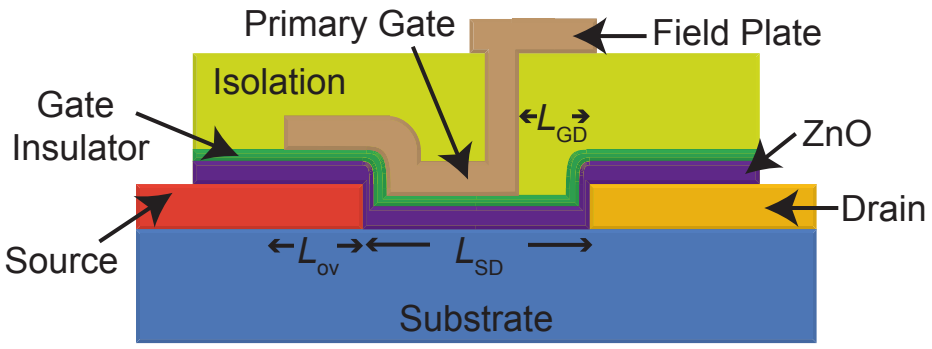

Figure 5.30: Schematic cross-section of a ZnO drain-offset TFT utilizing a field plate to weakly accumulate the offset region between the gate-and-drain. Note that the primary gate and field plate can also be separated and independently biased as well.

The ZnO TFTs presented thus far in this work show a wide variation in performance from changing only the drain-side contact metallization (from Ru to Au) and geometry (from a gate-to-drain overlap to drain-offset structure). Therefore, if their influences on the TFT's characteristics can be reliably predicted, a whole new approach to engineering ZnO TFTs can emerge without requiring complicated modifications to the device structure, fabrication process, or film growth recipes. Arising out of the efforts to model each class of device fabricated in this study with the TFT generic charge drift model by Marinov *et al.*, some guidelines of how to optimize the device geometry and S/D contact materials to specifically tailor a TFT's electrical characteristics was determined. Note that

since the compact model did not require any material parameters specific to ZnO, the conclusions derived from this analysis are also compatible with any TFT material system. Beginning with the conventional top-gate S/D-overlapped TFT with Ru S/D contacts, the on-state current and device mobility, at the cost of a higher SS and more negative V_{th}, were greatly enhanced from just changing the drain electrode to Au due to the Au/ZnO interface's lower contact resistance and higher electron densities. Hence, drain contact engineering can give a large boost in performance without needing to scale down the device dimensions. Similarly, the effects from changing the source metal can also be analytically captured by the TFT generic charge drift model, which is described in the next section.

The addition of an un-gated offset region between the gate-and-drain significantly altered the device characteristics. From just removing the gate-to-drain overlap alone, V_{th} became more positive, SS decreased, I_{on} and I_{off} decreased, mobility decreased, and C_{GD} decreased while $V_{DS,sat}$ noticeably increased along with the maximum V_{DS} before breakdown. After studying drain-offset devices with varying L_{GD}, only $V_{DS,sat}$ and the maximum V_{DS} were affected until the L_{GD}-to-L ratio reached ~ 0.5; after that point, the TFT's on-state performance began to diminish considerably. Therefore, L_{GD} requires optimization in order to maximize the drain-offset TFT's performance. When choosing a L_{GD} value, there are a few considerations. Firstly, increasing L_{GD} increases the device's high voltage handling capabilities and $V_{DS,sat}$, which needs to be acknowledged when designing circuits. But if L_{GD} reaches $\sim 0.5L$, the device's I_{on} and mobility begin to decline. Furthermore, when $L_{GD} > 0$ μm, there is a curvature in the drain-offset TFT's output characteristics arising from the offset region's restrictive SCLC. The SCLC eventually dominates the $I-V$ characteristics once L_{GD} approaches L. In light of these observations, as long as the V_{BD} requirements are met, 0 μm was found to be the best value for L_{GD} overall. The measured drain-offset ZnO TFT with $L_{GD} = 0$ μm did not suffer from the SCLC's limiting effects and demonstrated close to the best on-state performance while still substantially increasing the maximum drive voltage compared to the conventional staggered structure. To tailor the drain-offset TFT's saturation characteristics, besides scaling the device dimensions (e.g. W/L, L_{GD}, and L_{ov}), contact engineering of the source can be employed. According to the experiments conducted in the pre-

vious chapters, the injection characteristics of the source electrode plays a large role on TFT performance. In the upcoming section, a ZnO SGTFT employing a source Schottky barrier is modelled with the same TFT generic charge drift model to quantitatively determine how the ZnO TFT is affected by the source contact engineering.

5.7 Top-Gated ZnO TFTs with Cu Source Contacts

In this final section, the SGTFT structure is revisited to discern if the TFT generic charge drift model can also reproduce its unique characteristics. The SGTFT employs a Schottky barrier contact for the source electrode that alters the TFT's device physics. Its main advantages include a much lower $V_{DS,sat}$ and output conductance (g_{ds}) due to channel pinch-off occurring at the source rather than at the drain; however, the trade-offs are a lower device mobility and I_{on} [70, 98]. These qualities essentially originate from the additional depletion at the source because of the reverse biased Schottky barrier when $V_{DS} > 0$ V. Hence, using a similar approach as was used for the drain-offset TFTs, the voltage drop from the depletion region can be modelled with the parasitic series resistance, R_S. For this study, asymmetrical ZnO SGTFTs utilizing both the S/D-overlapped and drain-offset architectures were fabricated. A Ti/Cu contact was used for the source while Cr/Au was employed for the drain. The SGTFT dimensions and thicknesses were the same as the previously presented devices where $W/L = 50$ μm/32 μm and $L_{ov} = 10$ μm (if applicable) to allow for a direct comparison between Ru and Cu. These Cu-source TFTs were processed concurrently with the Ru-source devices (albeit not on the same wafer). Cu was chosen as the source metallization due to its consistent formation of a highly rectifying Schottky barrier with ZnO [183, 184]. After depositing the Ti/Cu stack (3 nm/12 nm thick) via sputtering and patterning with lift-off, surface plasma treatments were again avoided to minimize the oxidation of Cu before ZnO growth. This ensured the formation of a Cu/ZnO Schottky contact with very small reverse leakage currents, which would accentuate the unique features of the SGTFT.

The properties of the Cu/ZnO junction were first tested by measuring the $I-V$ characteristics of a simple lateral Schottky diode with a separation of 4 μm between the anode (Cu) and cathode (Au), which is presented in Fig. 5.31. A 2-D cross-section schematic of the diode is given in the figure's inset. The Cu contact was clearly rectifying featuring an ideality factor (n) of 2.0, current on-to-off ratio of ~ 10, and Schottky barrier height (Φ_B) of 0.74 eV when fitting the $I-V$ characteristics to the conventional Schottky barrier thermionic emission model (given by Equation 2.2). n and Φ_B were calculated using the Schottky diode parameter extraction method reported by Lee *et al.* (described in Chapter 2) [101]. Overall, the Cu/ZnO junction was more stable and rectifying than the previously presented TiW/ZnO junctions making the Cu-source ZnO TFTs a better representation of the SGTFT architecture [185, 184].

Symmetrical S/D-overlapped ZnO TFTs with bottom Cu/Cu S/D contacts were not investigated because of excessively low currents, which made it difficult to measure with the parametric analyser and extract TFT performance metrics. The transfer characteristics at $V_{DS} = 0.1$ and 3 V of an asymmetrical S/D-overlapped ZnO TFT based on Cu source and Au drain electrodes where $W/L = 50$ μm/32 μm and $L_{ov} = 10$ μm are plotted in Fig. 5.32. Compared to the S/D-overlapped Ru/Au ZnO TFT presented earlier (in Fig. 5.10), the electrical characteristics of the Cu/Au ZnO TFT were substantially different highlighted by its much lower maximum I_{on} at large V_{GS}. The Cu/Au TFT's μ_{sat} and V_{th} were extracted to be 0.27 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and 2.6 V respectively from fitting the saturation transfer characteristics to Equation 5.1. Consequently, the lower mobility and I_{on} expected of SGTFTs were demonstrated by these Cu-based devices. The Cu/Au TFT's V_{th} was comparatively high, which is attributed to the Cu/ZnO's high Φ_B. In the device's off-state, the source barrier prevents the injection of electrons into the channel thus keeping the device current low. As V_{GS} becomes more positive, the conduction band is pulled down by the gate field, and after a certain threshold, electrons can tunnel through the thinned source barrier greatly increasing I_{DS} (see Fig. 2.11 for an illustration of the idealized energy band diagrams in a SGTFT) [110, 186]. Therefore with a higher Φ_B, a larger V_{GS} is needed to pull down the conduction band to the point where tunnelling of carriers through the source barrier becomes significant, effectively delaying V_{th} [187]. From Fig. 5.33, which

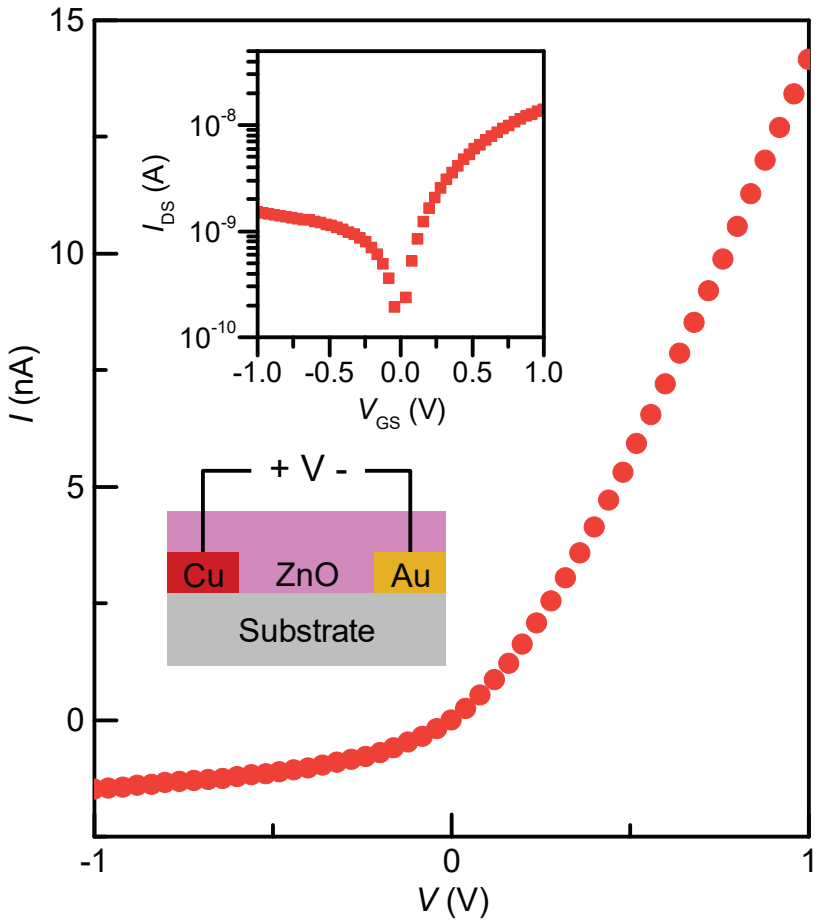

Figure 5.31: $I - V$ characteristics of a lateral Schottky diode with Cu/Au bottom anode/cathode electrodes. A 2-D cross-section schematic of the device is presented in the bottom inset. The top inset depicts the same electrical data in semi-log scale.

shows the Ru/Au and Cu/Au asymmetrical S/D-overlapped TFTs' C_{GS} plotted versus V_{GS}, it is evident that the Cu Schottky barrier brought about less electron accumulation likely because the Cu/ZnO barrier heavily prevented the thermionic emission of carriers that would have been present in a TFT employing ohmic S/D contacts. Furthermore, the Schottky barrier's depletion region also induces a series capacitance that lowers the effective C_{GS}. In the depletion regime (at negative V_{GS}), both devices' C_{GS} were similar in value implying that both TFTs were fully depleted. Hence, the benefits of the SGTFT's source barrier would be more apparent in a more disordered and highly doped ZnO film (which can be attained from a higher growth temperature or with an oxygen pre-deposition plasma treatment) [99].

The TFT generic charge drift model was applied to the Cu-based ZnO SGTFTs by modelling the reverse biased source barrier's depletion region as a parasitic series resistor using R_S. By choosing an appropriate value for R_S, the effect of the Schottky junction's voltage drop can be accounted for. Once again, the single TFT parameter extraction method was used to extract the parameter values; details of the parameter extraction are depicted in Fig. 5.34. Firstly, from an input V_{th} of 2.4 V, a γ of 1.0 was extracted from the H_{VGS} function at $V_{DS} = 3$ V using Equation 5.10. Afterwards, a μ_o of 2.0 $\mathrm{cm^2V^{-1}s^{-1}}$ was extracted from the linearised Y_{VGS} function at $V_{DS} = 0.1$ V using Equation 5.12. In the Cu/Au ZnO TFTs, the calculated R_C did not settle to a constant value at $V_{GS} < 3.5$ V, revealing that the resistor model for R_S employed thus far would not be as accurate for the Cu/Au TFTs. After re-simulating the output characteristics, which are displayed in Fig. 5.35, it was found that $R_S = 1.6$ MΩ provided the closest fit to the measured data. Nonetheless, the model was unable to accurately reproduce the $I-V$ characteristics over the entire V_{GS} range and caused the fit's mean percent difference to be comparatively higher at 12.0%. Because the SGTFTs' drive current is contact-limited, R_S plays a large role on the electrical characteristics. In order to improve the accuracy of the TFT generic charge drift model over the entire measurement range, a more elaborate model for R_S that includes its V_{GS} and V_{DS} dependence is required. One popular approach to model a TFT with non-linear contact effects is to split the device into two entities: one ideal transistor with the intrinsic TFT parameters connected in series with another parasitic

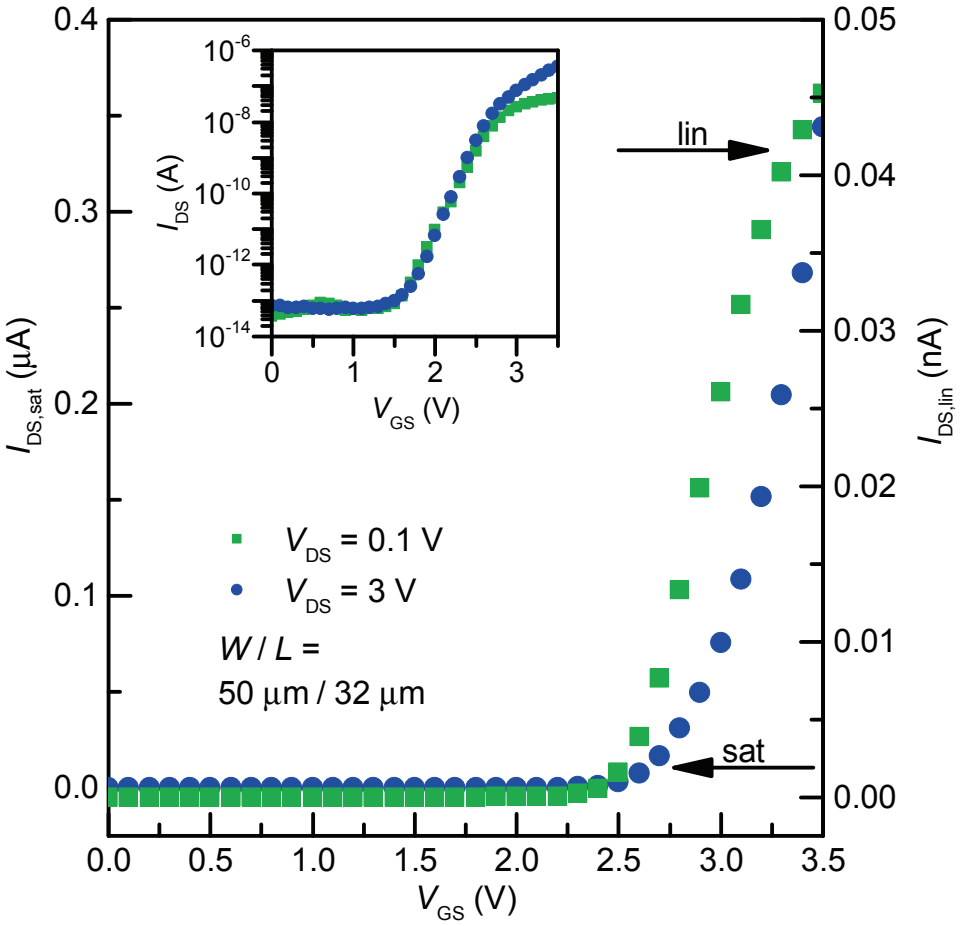

Figure 5.32: Transfer characteristics of an asymmetrical S/D-overlapped ZnO TFT with Cu source and Au drain electrodes where W/L = 50 μm/32 μm at V_{DS} = 0.1 V (green squares) and 3 V (blue circles). The inset shows the same data in semi-log scale.

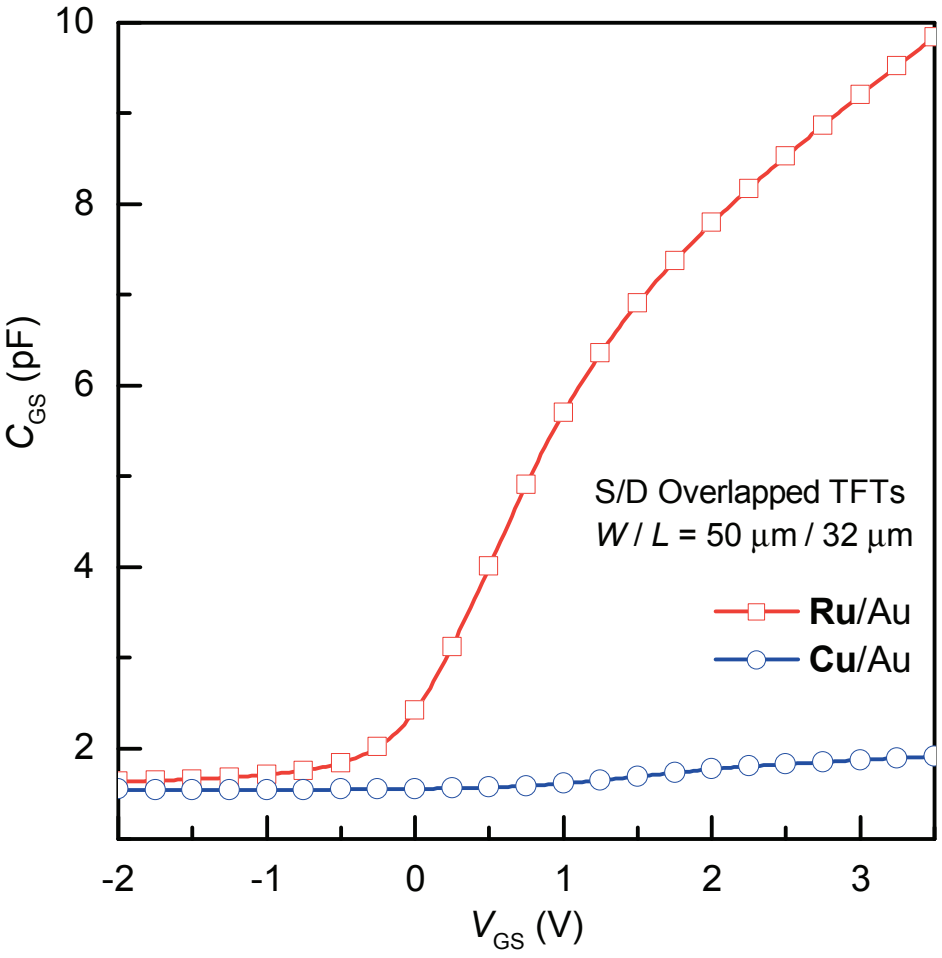

Figure 5.33: C_{GS} plotted as a function of V_{GS} at zero V_{DS} for asymmetrical S/D-overlapped top-gated ZnO TFTs utilizing Ru/Au (red squares) and Cu/Au (blue circles) S/D contacts at 1 MHz. The drain contact was floating during measurement, and the source metal of interest is bolded in the legend.

three-terminal element at the source to consider contact effects. Because the drain/ZnO junction is forward biased during normal operation, a parasitic load at the drain impacts the TFT much less (compared to a parasitic load at the source) and is usually ignored [188]. Typically, a reverse-biased diode is used to model the source contact [189, 98, 188], but a separate contact transistor is also applicable [145]. Both approaches include the V_{GS} and V_{DS} dependence of R_S unlike the resistor model used herein. Device simulation, however, is more complicated as the current through the parasitic source element and intrinsic TFT need to converge. Thus, the parameters for both elements need to be compatible with each other, and usually a circuit simulation software (e.g. Spice) is required to verify the model. The two element model also has too many degrees of freedom to accurately extract parameter values from a single device. Henceforward, multiple devices are usually utilized for parameter extraction. For the device dimensions used in this experiment, the TLM parameter extraction technique was unable to extract any useful parameters because R_S was too large and masked the transistors' L-dependence in their electrical characteristics. An alternative approach is to extract the intrinsic TFT parameters first from a long-channel device (assumed to have no contact effects) and the parasitic source element's parameters from a short-channel device afterwards (after eliminating the effects of the ideal transistor) [145, 188]. This necessitates the assumption that the ideal TFT parameters are constant over the entire L-range however. Nevertheless, for $V_{GS} > V_{th}$, the SGTFT is operating in a tunnelling-dominated injection regime, and the contact effects should be stable enough for the constant R_S approximation to work. The discrepancy between the modelled and measured current at $V_{GS} = 3.5$ V in Fig. 5.35 is therefore attributed mostly to gate bias stress causing the current to drop over time through charging effects or V_{th} shifts for instance. The $I-V$ curve at $V_{GS} = 3.5$ V was the initial measurement in Fig. 5.35 and was the most inconsistent when the output characteristics were re-measured. A possible solution to this problem could be to employ pulsed $I-V$ measurements [190]; however, the Keithley 4200 SCS did not have the technical capabilities/features to measure < 1 mA with a pulsed $I-V$ set-up.

Last of all, asymmetrical drain-offset ZnO SGTFTs utilizing Cu source and Au drain contacts were investigated. Typical transfer characteristics of a drain-

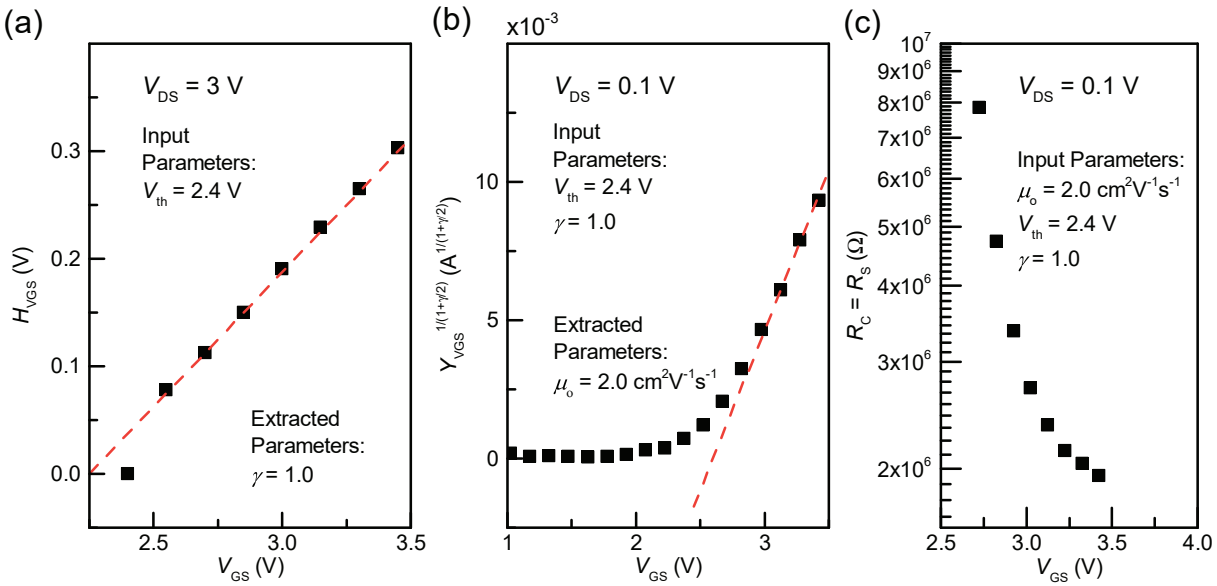

Figure 5.34: Modified $I - V$ characteristics for parameter extraction from an asymmetrical S/D-overlapped ZnO TFT with Cu source and Au drain contacts where $W/L = 50\ \mu$m$/32\ \mu$m. (a) H_{VGS} versus V_{GS} at $V_{DS} = 3$ V calculated with an input of $V_{th} = 2.4$ V. The linear regression fit used to extract γ is shown by the dashed line. (b) Linearised Y_{VGS} function ($\sqrt[1+\gamma/2]{Y_{VGS}}$) versus V_{GS} at $V_{DS} = 0.1$ V. The linear regression fit used to extract μ_o is shown by the dashed line. (c) Contact resistance at the S/D terminals ($R_C = R_S$) calculated from the transfer characteristics at $V_{DS} = 0.1$ V plotted in semi-log scale.

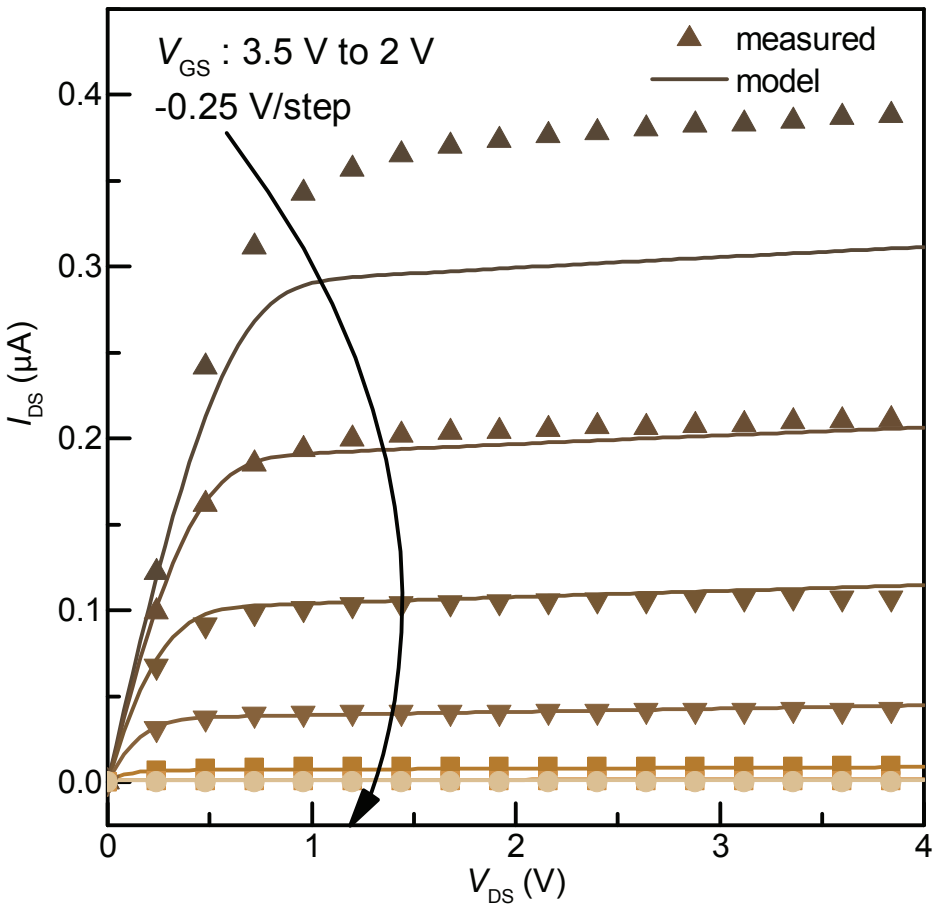

Figure 5.35: Output characteristics of an asymmetrical S/D-overlapped ZnO TFT with Cu source and Au drain contacts where $W/L = 50\ \mu$m/32 μm. V_{GS} is increasing from 2.00 V to 3.50 V in 0.25 V steps. The re-simulated characteristics using the TFT generic charge drift model (lines) are overlaid on top of the measured data (symbols).

offset SGTFT where L_{GD} = 8 μm at V_{DS} = 0.1 V and 8 V are presented in Fig. 5.36; whereas its corresponding output characteristics are shown in Fig. 5.37. Unlike the Ru/Au drain-offset TFTs, neither I_{sat}, mobility, nor V_{th} noticeably changed in the Cu-based drain-offset TFT compared to its corresponding S/D-overlapped device (e.g. Fig. 5.35). This is by cause of the Cu/Au ZnO SGTFTs being contact-limited wherein the source barrier controls most of the device characteristics. From fitting the conventional MOSFET equation to the saturation transfer characteristics, 0.31 $cm^2V^{-1}s^{-1}$ and 2 V were extracted for μ_{sat} and V_{th} respectively. Using just the output characteristics alone, it is difficult to determine if channel pinch-off occurred at the source (as expected in a pure SGTFT [99, 98]) or at the gate edge nearest to the drain. Once again, the most obvious impact of adding a drain-offset was delaying $V_{DS,sat}$ for the same reasons described previously - due to parasitic losses in the intrinsic un-gated offset region reducing the effective V_{DS} seen by the channel and source electrode. In the Ru/Au drain-offset TFTs, I_{on} was restricted by the offset region's SCLC at $L_{GD} > 0$ μm. However, the space-charge effect was less pronounced in these devices because there were less carriers available to be injected from the channel, which in turn were restricted by the source Schottky barrier through the mechanism explained above. Therefore, the difference between the channel's and offset region's carrier concentrations was small enough for the SGTFT's current conduction to remain mainly ohmic [45]. Fig. 5.38 shows the output characteristics of Cu/Au drain-offset SGTFTs where L_{GD} = 0, 2, 8, and 16 μm at high $V_{GS} > V_{th}$. In all instances, there was no indication of SCLC based on the linear $I - V$ characteristics in the linear regime. Moreover, like with the Ru/Au drain-offset TFTs, on-state device performance began to decline between L_{GD} = 8 to 16 μm. When L_{GD} approached L, although SCLC was not present, the drain-offset TFT's current did not saturate after $V_{GS} > V_{th}$ most likely from short-channel-like effects as the effective channel length (that is gated) is much less than L.

Unfortunately, accurate simulations of the Cu/Au drain-offset SGTFTs with the TFT generic charge drift model were not realized. Previously, for the Ru/Au drain-offset devices, R_S was assumed to be equal to the value extracted from the symmetrical staggered Ru/Ru TFTs. However, the R_S utilized for Fig. 5.13

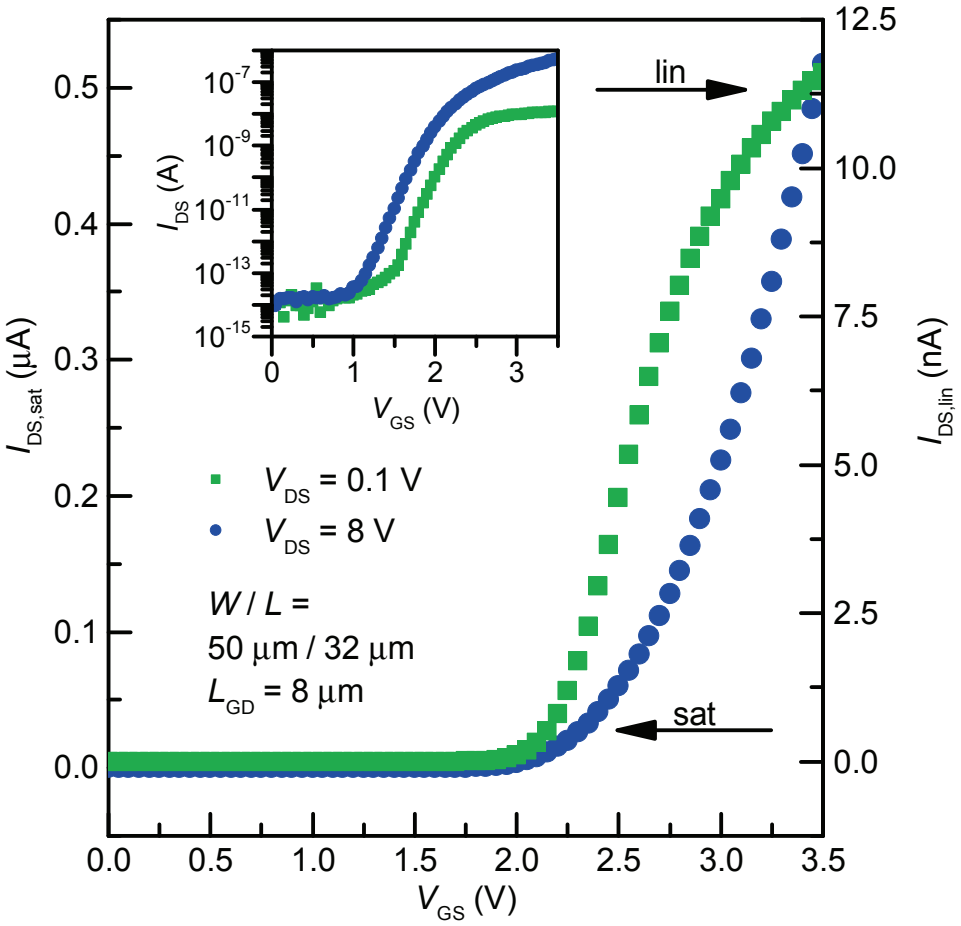

Figure 5.36: Transfer characteristics of an asymmetrical drain-offset ZnO TFT with Cu source and Au drain electrodes where $W/L = 50\ \mu$m$/32\ \mu$m and $L_{GD} = 8\ \mu$m at $V_{DS} = 0.1$ V (green squares) and 8 V (blue circles). The inset shows the same data in semi-log scale.

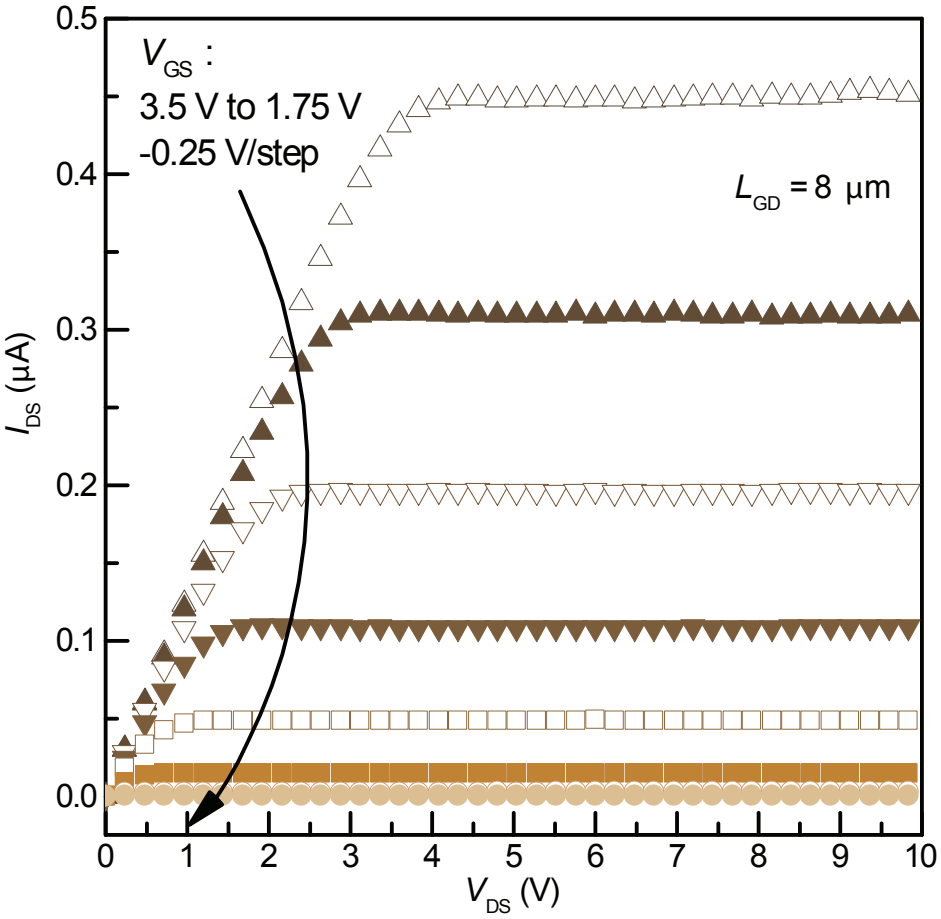

Figure 5.37: Output characteristics of an asymmetrical drain-offset ZnO TFT with Cu source and Au drain contacts where $W/L = 50$ μm/32 μm and $L_{GD} = 8$ μm. V_{GS} is increasing from 1.75 V to 3.5 V in 0.25 V steps.

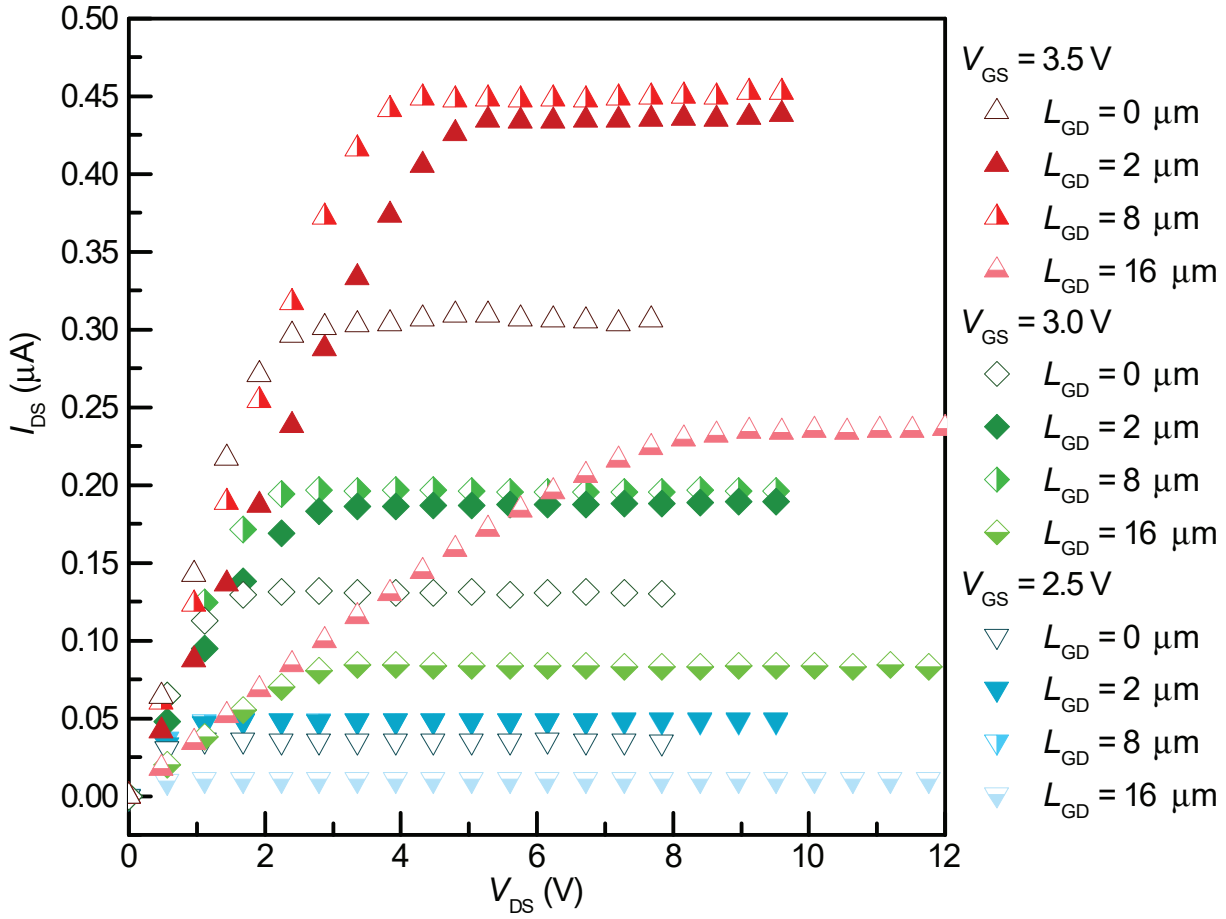

Figure 5.38: Measured output characteristics of multiple asymmetrical drain-offset ZnO TFTs with Cu source and Au drain contacts where $W/L = 50$ μm/32 μm and $L_{GD} = 0, 2, 8$, and 16 μm. V_{GS} varied from 2.5 to 3.5 V in 0.5 V steps.

did not work for the drain-offset SGTFTs. Moreover, the single TFT parameter extraction technique as a whole was unable to produce viable parameter values to match the Cu/Au drain-offset TFT's output characteristics despite being able to fit the measured transfer curves. Most likely, the Cu/Au TFTs were not in the same state when the transfer and output characteristics were measured; i.e. the parameters changed between measurements presumably from bias stress. Accordingly, investigations into the instabilities present within the ZnO TFTs will be needed in the future to reduce their effects during device measurements.

In summary, the Cu/Au ZnO TFTs as a whole were less stable than the Ru/Au TFTs making it difficult to accurately model them with the single TFT parameter extraction method. Nonetheless, from comparing the characteristics of the Cu/Au and Ru/Au ZnO TFTs, some insight into the SGTFT can still be deduced. As expected, the SGTFT exhibited much lower drive current and a more positive V_{th}. The SGTFT's lowered on-state performance, caused by the source barrier's depletion region, can be accounted for by an increase in the parasitic resistance at the source and a lower mobility. Since injection of carriers by thermionic emission in a SGTFT is limited by the source barrier, the SGTFT's V_{th} is more positive and is an indication of when the device's tunnelling current becomes significant (as theorized in Chapter 2). Although the device physics between the Cu/ZnO and Ru/ZnO TFTs were different, the TFT generic charge drift model was able to reproduce the $I-V$ characteristics of both class of devices. The source Schottky barrier TFT architecture did not perform as well as the conventional TFT using ohmic contacts overall as the ZnO electron concentration was low enough for the Ru-based TFTs to fully deplete as well (which is one of the main advantages of SGTFTs). It is expected that if the semiconductor is more disordered and highly doped, the SGTFT architecture would exhibit comparatively better V_{th}, SS, and I_{off} due to the influence from the source Schottky contact's depletion region. For Cu/ZnO drain-offset SGTFTs, the function of L_{GD} remains the same - to increase V_{BD} and $V_{DS,sat}$. The Cu/Au Schottky junction reduced the accumulation channel's carrier densities enough to remove the SCLC-induced curvature observed in the Ru/Au drain-offset SGTFTs. Likewise, because the source barrier controlled most of the on-state device behaviour, the Cu/Au drain-offset SGTFTs did not suffer any noticeable degradation in I_{on}, mo-

bility, SS, and V_{th} compared to the corresponding S/D-overlapped SGTFT with the same W/L. Thus, for Cu/Au ZnO TFTs, the removal of the gate-to-drain overlap did not lead to any drawbacks in device performance.

5.8 Summary of ZnO TFT Modelling

ZnO TFTs of various device architectures and S/D materials can be realistically modelled with the TFT generic charge drift model developed by Marinov *et al.* [143]. From the transfer characteristics of a single TFT, suitable parameter values for the model were precisely extracted and verified through re-simulation of the measured output characteristics. Prototype devices employing a symmetrical overlap between the gate-and-S/D contacts were compared with equivalent devices utilizing an intrinsic offset region between the gate-and-drain. Moreover, while manipulating the drain-side geometry, several different S/D metallization schemes were also simultaneously studied. TFTs using symmetrical Ru/Ru contacts for the S/D were compared with devices with Ru/Au and Cu/Au S/D metal electrodes. Measured output characteristics from the symmetrical S/D-overlapped Ru/Ru ZnO TFTs were successfully fitted to the TFT generic charge drift model, and the extracted parameters from the single TFT parameter extraction method were further verified by comparing them to the values extracted from the plural device TLM approach. Improvements in the TFT on-state performance, with the loss of slightly degraded switching characteristics, after changing the drain metal to Au from Ru were easily accounted for in the model through choosing appropriate values for μ, γ, V_{th}, and contact resistance that was modelled by a single series parasitic resistor, R_S, at the source terminal. Characteristics of ZnO SGTFTs employing Cu/Au S/D contacts were also modelled in the $V_{GS} > V_{th}$ regime by the TFT generic charge drift model after increasing R_S, increasing V_{th}, and lowering μ to replicate the SGTFT's reduced on-state performance facilitated by the reverse-biased source Schottky barrier's depletion region. Similarly, the drain-offset device architecture's higher $V_{DS,sat}$ was successfully modelled by adding a V_{GS}-dependent parasitic series resistance, R_{GD}, between the gate-and-drain. The reduced on-state TFT behaviour from removing the gate-to-drain overlap was attributed to parasitic losses at the edge of the

gated channel causing the effective mobility to decrease. For small values of L_{GD}, the TFT performance was basically equivalent with the $L_{GD} = 0$ μm device besides a higher V_{BD} and $V_{DS,sat}$, which was accounted for by increasing R_{GD}. For the case where Ru was used for the source electrode though, $L_{GD} > 0$ μm led to a curvature in the output characteristics resulting from SCLC in the intrinsic offset region that the model was unable to reproduce. A summary of all the influences observed when manipulating the S/D metallization and drain-side geometry is tabulated in Table 5.2.

In this study, a single fabrication run was able produce a variety of different ZnO TFT behaviours by manipulating only the S/D contact metallization and gate-to-drain layout. With a thorough understanding of the impact of contact engineering and the device architecture, a wide range of transistor characteristics can be designed and engineered using ZnO TFTs. The successful modelling of the various ZnO devices using Marinov *et al.*'s TFT generic charge drift model would significantly simplify the design and integration of ZnO TFTs with real-world electronic circuits. Additionally, due to the universal nature of the compact model, the techniques described herein can also be applied for the design and engineering of TFTs based on any semiconductor such as amorphous indium-gallium-zinc-oxide (IGZO) and Si TFTs.

Table 5.2: Summary of the S/D Metallization's and Drain-side Geometry's Impact on the Device Performance of Top-gated ZnO TFTs

Action	Physical Effect	Impact on TFT Performance
Changing the drain electrode to Au from Ru	• Increases the drain's electron concentration making the TFT more difficult to fully deplete • Reduces the drain's contact resistance	• V_{th} is more negative (from 0.53 to -0.7 V) • SS increases (by $\sim 175\%$) • μ increases (by $\sim 1045\%$)
Removing the gate-to-drain overlap ($L_{GD} = 0$ μm)	• Reduces electric field at the drain • Lowers the drain's electron concentration making the TFT easier to fully deplete • Introduces voltage loss at the gated channel's edge	• V_{BD} increases • V_{th} is more positive (from -0.55 to 1.1 V) • SS decreases (by $\sim 81\%$) • $V_{DS,sat}$ increases • μ decreases (by $\sim 85\%$)
Increasing $L_{GD} > 0$ μm	• Introduces space-charge-limited current in the offset region • Increases voltage losses in the offset region • Reduces the electric field seen by the channel	• Induces a curvature in the output characteristics at low V_{DS} • Reduces μ at large enough L_{GD} • $V_{DS,sat}$ increases • V_{BD} increases
Changing the source electrode to Cu from Ru	• Schottky barrier formation at the source reduces the source's electron concentration making the TFT easier to fully deplete • Source Schottky barrier restricts the injection of carriers into the channel • Reduces the influence of space-charge limited current in drain-offset devices	• V_{th} is more positive (from -0.55 to 2.4 V) • SS decreases (by $\sim 64\%$) • μ decreases (by $\sim 69\%$)

The conclusions were drawn based on the modelling of the various devices presented throughout this chapter. Values for percent change (when applicable) were calculated by comparing the relevant devices and parameters before and after the specific action was performed.

Chapter 6

Conclusions and Future Work

The utility of zinc oxide (ZnO) thin film transistors (TFTs) has yet to meet its enormous potential. Hence, continued efforts on improving ZnO TFT performance without sacrificing its compatibility with low temperature processes are still important endeavours. This research documents investigations on the many factors that can influence a ZnO TFT's performance. Different prototype ZnO TFTs were designed, fabricated, and tested to study the impact of the device materials, layout, and physics on their characteristics. Analysis of the ZnO TFTs presented herein provided insight into the avenues toward boosting TFT performance and how to tailor for specific device behaviours. Lastly, compact modelling of ZnO TFTs was described to allow for the design of ZnO electronic circuits.

ZnO source-gated thin film transistors (SGTFTs) that utilize a Schottky source injection barrier were studied in detail. Firstly, bottom-gated SGTFTs employing a ZnO channel grown by pulsed laser deposition (PLD) at room temperature with post-growth annealing revealed good transistor behaviour featuring lower saturation voltages ($V_{DS,sat}$) and output conductances (g_{ds}) compared to identical TFTs with ohmic source-and-drain (S/D) contacts. The ZnO SGTFTs also displayed low mobilities and drive currents from a combination of the source barrier inhibiting the injection of carriers and the small grain sizes of the PLD-grown films. Insight into how the SGTFT operates differently from the conventional TFT was derived from studying the ZnO SGTFTs' unique gate-to-source capacitance (C_{GS})-gate-source voltage (V_{GS}) and transconductance (g_m)-V_{GS} characteristics. Specifically, these measurements suggested the dominant

current injection mechanism at the source Schottky barrier transitioned from being principally thermionic emission to tunnelling at a particular positive gate voltage. Based on this observation, it is believed that this behaviour could be exploited to achieve an enhancement-mode ZnO SGTFT by focusing on the engineering of a high quality Schottky injection barrier to restrict the device's off-state current (I_{off}) before the tunnelling current dominates.

Building on these works, a top-gated ZnO SGTFT more suited for practical implementation in conventional integrated circuits was studied. Atomic layer deposition (ALD) at temperatures less than 130°C was utilized to deposit both the ZnO channel and high-κ hafnium oxide (HfO_2) gate dielectric, making the transistor compatible with flexible substrates. Besides demonstrating good device performance, featuring a positive threshold voltage (V_{th}) of 0.91 V and a saturation mobility (μ_{sat}) of 3.9 $cm^2V^{-1}s^{-1}$, the top-gated ZnO SGTFTs displayed excellent breakdown characteristics for their relatively small dimensions from employing an un-gated offset region between the top drain-and-gate electrodes. Particularly, the lowest breakdown voltage (V_{BD}) measured was $\sim$ 20 V for a gate-to-drain distance (L_{GD}) of 2 μm. The devices also exhibit the characteristically low output conductances and low saturation voltages of SGTFTs. Consequently, these optimized SGTFT devices could potentially be applied for any application that can utilize enhancement-mode TFTs requiring high pull-down voltages.

Although promising transistor characteristics were observed, the behaviour of the ZnO SGTFTs was inconsistent from device-to-device. To better understand the disparities originating from the source-and-drain (S/D) contacts, a study on top-gate staggered ALD ZnO TFTs with differing S/D metallization schemes was performed. When comparing the transistor characteristics of identical TFTs with symmetrical gold (Au), ruthenium (Ru), and titanium tungsten (TiW) bottom S/D contacts, the contact effects from the S/D electrodes greatly impacted device behaviour. X-ray diffraction (XRD) measurements revealed that the Au contacts exclusively facilitated the growth of a highly n-doped ZnO film that degraded the Au ZnO TFTs' output conductance and gate control. Conversely, the TiW ZnO TFTs' on-state performance was restricted by the Schottky barriers formed at the TiW/ZnO interface. The best overall performance was demonstrated by the Ru ZnO TFTs that showed a moderately high μ_{sat} of 1.4 $cm^2V^{-1}s^{-1}$ and

excellent switching characteristics including a low subthreshold swing (SS) of 89 V/decade, low off-state current (I_{off}), and positive V_{th}. Using X-ray photoelectron spectroscopy (XPS), it was found that the Ru ZnO TFT's superior device characteristics originated from an oxidation-free metal/ZnO interface at the S/D electrodes that inhibits the adsorption of hydroxide surface dopants. Consequently, the chemistry of the S/D metal/ZnO interface played a large role on the ALD ZnO film growth and nature of the interface energetics.

Finally, top-gate ZnO TFTs with differing S/D metallizations and drain-side layouts were fabricated and all modelled with the TFT generic charge drift model developed by Marinov *et al.* [143]. The compact model is based on the gradual channel approximation (GCA) and considered several transistor non-idealities including a V_{GS}-enhanced mobility, S/D contact resistance, and non-constant saturation currents (I_{sat}). A single TFT's transfer characteristics during saturation and in the linear regime were utilized to extract suitable parameter values for the model. The accuracy of the model was verified by comparing re-simulated TFT output characteristics with the measured data. Manipulating the S/D metallization changed the device's drive current, mobility, and switching characteristics. The best overall performance was demonstrated by an asymmetrical S/D contact metallization scheme where Ru was employed for the source and Au for the drain. Asymmetrical Ru/Au ZnO TFTs with the conventional staggered structure employing equal overlaps between the gate-and-S/D contacts exhibited good switching performance and excellent on-state characteristics when compared to symmetrical staggered Ru/Ru TFTs. When a drain-offset was added between the gate-and-drain contacts, the TFT's drive current and mobility significantly decreased due to a combination of parasitic losses at the gated channel edge and space-charge limited current (SCLC) in the un-gated offset region. However, $V_{DS,sat}$ and V_{BD} substantially increased as well. When Ru was replaced with copper (Cu) at the source, which was observed to be an excellent Schottky contact for ZnO, the asymmetrical Cu/Au ZnO SGTFTs demonstrated noticeably lower currents and mobilities as expected from the source-gated effect [70]. However, the benefits of the source Schottky barrier approach would be more apparent with a higher doped semiconductor than what was utilized for this study. All of these different device architectures and behaviours were accurately reproduced

by the TFT generic charge drift model from manipulating the parasitic elements for modelling the S/D contact resistance. The Schottky source injection barrier was adequately emulated in the $V_{GS} > V_{th}$ regime with a parasitic resistance at the source; whereas, the drain-offset structure was modelled with a parasitic V_{GS}-dependent resistance at the drain. In summary, the modelling efforts presented in this work can be exploited for the design of ZnO electronic circuits.

6.1 Directions for Future Work

6.1.1 Improvements to Device Performance

The ZnO TFTs presented in this work have demonstrated promising device performance that is suitable for any technology that can use large-area, low density circuitry. However, there is room for improvement before ZnO TFTs can be considered for commercial applications. Particularly, a better understanding of the device instabilities is required to reduce their impact on TFT performance. From the efforts of testing and modelling ZnO TFTs, it was clear that the current-voltage ($I-V$) characteristics were not consistent from device-to-device. Furthermore, hysteresis and threshold voltage (V_{th}) shifts were observed during device testing. Thus, quantifying the effects of positive and negative gate bias stress, temperature, and illumination on the transistor characteristics are necessary in the future to evaluate and reduce the instabilities in ZnO TFTs. One obvious solution for improving device reliability that was not implemented yet is device passivation. Previous works regarding passivating ZnO TFTs have demonstrated good results for bottom-gate TFT architectures by preventing back-channel doping and hydrogen diffusion into the ZnO with inorganic dielectrics [24, 191]. Although the top-gate insulator utilized for the ALD ZnO devices reported in this thesis can act as a pseudo-passivation layer for the ZnO channel (since it encapsulates the entire active channel layer) the device characteristics were still affected by instabilities. An additional thicker passivation layer will aid device reliability by acting as a diffusion barrier and preventing the charging of the gate dielectric. Henceforward, high quality passivation will be necessary for future technologies

built on ZnO TFTs.

The ALD ZnO TFTs presented in this thesis form a solid base for future applications in next-generation flat panel displays (FPDs) and other ZnO-based large area circuits e.g. energy harvesting circuits [192]. This research was primarily focused on the device architecture's and S/D electrodes' impact on TFT performance. However, the electronic properties of the ALD ZnO films utilized herein can still be optimized further. Particularly, the ALD ZnO's residual electron concentration was seemingly affected by pre-growth oxygen and argon plasma treatments. Furthermore, in the ALD ZnO TFTs utilizing bottom Au S/D contacts, the contact resistance was evidently reduced by a post-fabrication hot-plate anneal. The exact nature by which the Au contact's resistivity decreased requires further inquiry. If the Au/ZnO ohmic contact's resistivity and doping can be controlled precisely, the reliability and reproducibility of the ALD ZnO TFTs would improve tremendously. It would also allow the use of lower temperature ALD ZnO films, which is beneficial for reducing the film non-uniformities arising from non-ALD growth components observed in the higher temperature ALD ZnO [193]. Thus, a detailed understanding of how the substrate and pre-growth surface treatments affect the ALD ZnO growth is a worthwhile venture and can unlock ways to further improve the performance of ALD ZnO TFTs.

6.1.2 Integration with Circuit Applications

Based on the performance and reliability of the ALD ZnO TFTs demonstrated in this thesis already, the integration of ZnO TFTs into useful electronic circuits such as amplifier, display, and sensor circuits should be possible. A variety of simple circuits such as inverters and ring oscillators can give some insight on the performance of ZnO-based analog and digital circuits [194, 195]. However, application demonstrations of the successful integration of ZnO TFTs are also valuable building blocks for future ZnO technologies. Without a viable p-type ZnO TFT, building conventional complementary metal-oxide-semiconductor (CMOS) integrated circuits using only ZnO TFTs is not possible. A simple alternative is direct-coupled tranisistor logic (DCTL) utilizing only n-channel ZnO TFTs. Because enhancement- and depletion-mode (E/D-mode) ZnO devices can be fab-

ricated on the same substrate by adjusting the S/D metallization as described in Chapters 4 and 5, it is possible to implement E/D-mode ZnO circuits relatively easily. E/D-mode ZnO logic can potentially be used to build low-cost, low power integrated ZnO circuits for various applications [196, 197, 198, 199]. If an inverter is built using E/D-mode logic [see Fig. 6.1(a) for a simple schematic], the enhancement-mode transistor is used as the driver, whereas the depletion-mode transistor is used as the load [200]. The output "low" voltage of an inverter employing E/D-mode logic is non-zero, unlike the CMOS inverter, because of static losses in the depletion-mode transistor. Hence, circuits employing E/D-mode logic have a reduced voltage swing, lower noise margins, and greater power consumption [200]. Some initial work on simple amplifier circuits built with E/D-mode ZnO TFTs has already begun. Fig. 6.1(b) shows a circuit schematic of a fully differential amplifier using E/D-mode logic and current-source loads (the feedback circuit for the output is not shown). If successfully implemented, the ZnO-based amplifier can be easily expanded using conventional analog circuit design techniques to build more complex circuits. The simulated frequency response of the E/D-mode differential amplifier using ZnO TFTs with similar device performance to the ones presented in Chapter 4 is also plotted in Fig. 6.1(c). The maximum gain is ~ 5 dB with a cut-off frequency of $1 - 5$ MHz. This simulation is just a preliminary work but gives an estimation of the performance that a ZnO-based amplifier can realise.

Other important application demonstrations are transparent and flexible electronics using ZnO TFTs. Because of the low processing temperatures of the ALD growth recipes, flexible polymer-based substrates, e.g. polyethylene terephthalate (PET) and polyethylene naphthalate (PEN) films, are compatible with the device processing utilized for the ALD ZnO TFTs. Flexible and transparent electronics are expected to be key technologies for emerging new applications such as smart labels, wearable electronics, and flexible screens [201, 202].

Finally, as FPD resolutions continue to increase, the TFT's area needs to be minimized. Currently, the effects of device scaling on the ZnO TFT's characteristics are still unknown in the regime of channel length (L) < 1 μm where short-channel effects are expected to be present. If ZnO TFTs with sub-micron channel-lengths are investigated, then the upper-limit of ZnO TFT performance

can be better understood, which would be invaluable for circuit design.

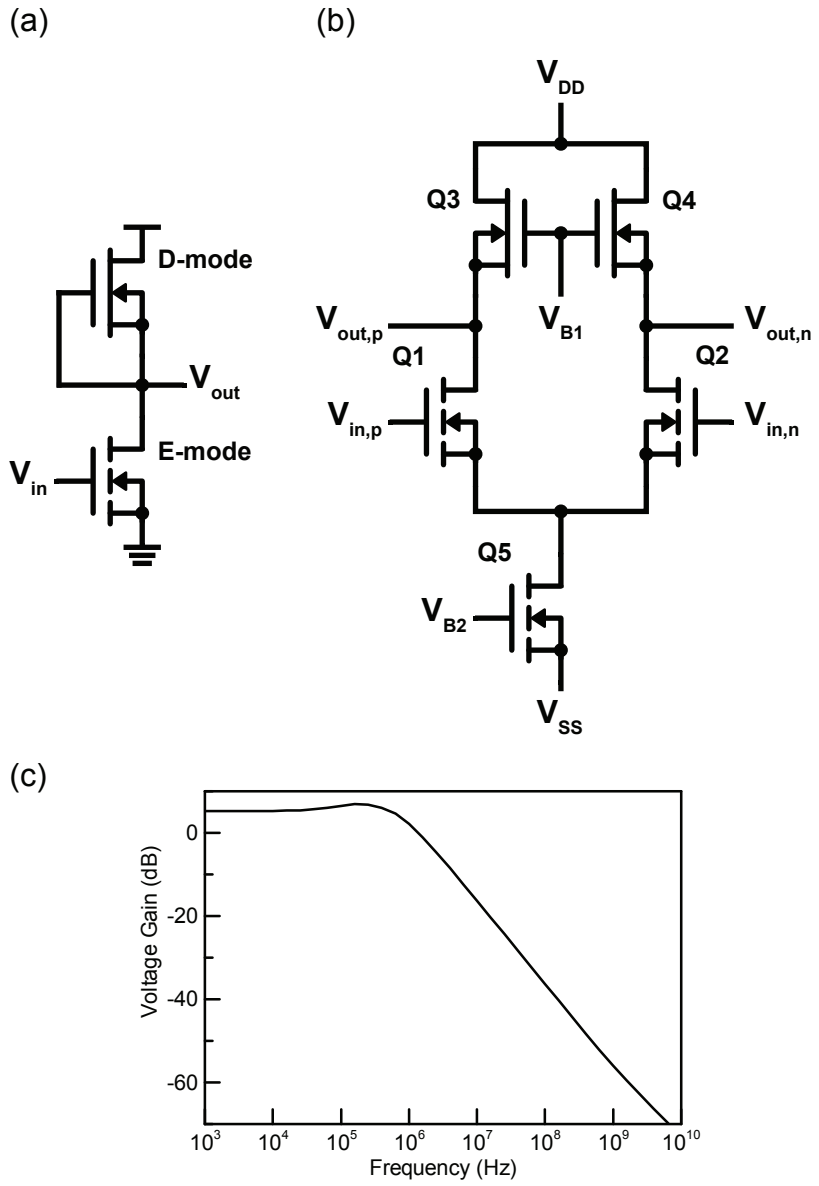

Figure 6.1: Schematic of a direct-coupled tranisistor logic (DCTL) (a) inverter and (b) fully differential amplifier circuit utilizing enhancement- and depletion-mode (E/D-mode) transistors. (c) Simulated frequency response of the amplifier circuit in (b). The transistor dimensions were: $\frac{W_{34}}{L_{34}} = 40\ \mu$m/4 μm, $\frac{W_{12}}{L_{12}} = 1000\ \mu$m/2 μm, and $\frac{W_5}{L_5} = 40\ \mu$m/4 μm. V_{B1} and V_{B2} were biased at +0.5 V and -0.5 V respectively, whereas V_{DD} and V_{SS} were set at +4 V and -4 V respectively.

Overall there are still some fundamental questions regarding the ZnO TFT's stability and reliability that need to be solved. On the other hand, integration of the ZnO TFTs presented in this research with compatible applications are also important. Nonetheless, the future prospects of ZnO TFTs are very promising. If a low-cost, high performance ZnO TFT can be achieved with low processing temperatures, it would unlock many useful applications extending beyond just future FPD technologies.

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