

Detailed Magnetic Equivalent Circuit Based Real-Time Nonlinear Power Transformer Model on FPGA for Electromagnetic Transient Studies

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Abstract—A detailed power transformer electromagnetic transient model would help in accurately predicting transient stresses and formulating adequate protection strategies in power systems. This paper presents a real-time nonlinear high-resolution magnetic equivalent circuit (HR-MEC) based transformer model on the field-programmable gate array for hardware-in-the-loop simulation. This model is inspired by the mesh generated in finite-element method (FEM) tools to depict the major flux paths in the transformer. All of the major nonlinear phenomena such as saturation, hysteresis, and eddy currents are captured in the transformer hardware emulation whose modules were developed in a 32-bit floating point precision VHDL. The developed HR-MEC model and nonlinear numerical solution have been fully parallelized in hardware to achieve the lowest latency in the real-time implementation. The hysteresis in the transformer core is modeled using Preisach theory, and eddy currents are incorporated using a frequency-dependent network. The real-time results are validated using 3-D FEM analysis in JMAG software.

Index Terms—Electromagnetic transient (EMT) analyses, embedded systems, field-programmable gate arrays (FPGAs), hysteresis, magnetic equivalent circuit, parallel algorithm, parallel process, pipelining, real-time systems, saturation, transformer modeling.

I. INTRODUCTION

ELECTROMAGNETIC transients (EMTs) can impose severe stresses on the components of power transformers, leading to expensive repair or replacement. Therefore, a detailed study of EMT impact on transformers is important from the viewpoint of asset management and power system security and reliability. Interphase coupling, core saturation, residual fluxes, hysteresis, and eddy current behavior are all important phenomena in transformer modeling. To model such phenomena for real-time EMT simulation, the physical geometry of

the power transformer needs to be taken into account while developing the model. Not modeling these phenomena leads to incorrect estimation of transient overvoltages, in turn, resulting in dubious protection strategies, controller settings, compensation equipment rating choice, etc., which adversely impact the transformer behavior in this field. Most commonly used transformer models (lumped parameters with circuit representation such as BCTRAN [1], [2]) for EMT simulation ignore the detailed transformer geometry to speed up the transient simulation in both offline and real time. Ideally, the finite-element model (FEM), either 2-D or 3-D, should be used for detailed transient studies to study the aforementioned phenomena; however, the computational burden to perform repeated FEM simulations is prohibitively excessive even for offline simulation, let alone real-time simulation.

Non-FEM topology-based transformer models began to appear in the literature in the early 1990s [3]–[6]. A comprehensive review of topology-based models can be found in [7]. Basically, there are two types of such models: duality based and geometry based. Both models are based on the magnetic equivalent circuit theory [8]; however, the duality-based models do not require the transformer design data, whereas the geometry-based models rely on detailed core geometry. The most widely used geometry-based model is the unified magnetic equivalent circuit (UMEC) model [9], [10] implemented in the PSCAD/EMTDC software. It is formulated in terms of magnetomotive force (MMF) sources and magnetic flux path reluctances (nonlinear reluctances through iron and linear reluctances for leakage paths through the air), which results in transformer nodal equations being nonlinear and time variant. Thus, the power system admittance matrix needs to be updated in each time step of the transient simulation, resulting in longer simulation time and restricting the size of the modeled power system. A hybrid transformer model (XFMR) has also been proposed [11], which takes advantage of both duality-based and geometry-based models, and it is implemented in ATPDraw [12] and compared with respect to the UMEC model in terms of accuracy [13]. All of the aforementioned topology-based models have only been implemented and tested in offline simulation, with the exception of the UMEC model which was implemented [14] in real time in the RTDS simulator. Limited nonlinear behavior is incorporated using a piecewise linear saturation curve (flux versus MMF) which is precomputed and

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stored on the processor. This type of modeling caused numerical oscillations which were damped using a compensation circuit. Complex behavior such as hysteresis and eddy currents in the physical core are omitted. The resulting real-time model was compared with respect to the offline UMEC model in PSCAD/EMTDC.

This paper develops a field-programmable gate array (FPGA) based nonlinear high-resolution magnetic equivalent circuit (HR-MEC) based model for the power transformer for real-time simulation of EMTs. The advantages of this approach include the following.

- 1) The accounting of the major flux paths in the transformer core using a detailed magnetic equivalent circuit inspired by the mesh generated for FEM analysis. Transformer core hysteresis modeling using the Preisach theory [15] and eddy current behavior modeling using a frequency-dependent equivalent network.
- 2) Reduced model latencies due to the exploitation of full hardware parallelism and pipelining on the FPGA; thus, smaller time steps can be used for capturing higher frequency transients. FPGAs have proven to be quite efficacious in industrial control as well as in power system and power electronic system EMT modeling [24]–[41]; however, a detailed real-time modeling of the power transformer on the FPGA is yet to be reported.
- 3) Sparse matrix methods are exploited to further increase computational efficiency. A parallel LU decomposition method that is both time and resource efficient is proposed to solve the transformer and network nodal equations.
- 4) The implementation of the UMEC model on the traditional sequential processor takes up a lot of computational resources, not only for the model execution but also to update and invert the system admittance matrix in each time step. Therefore, the test system size becomes smaller for a given simulator hardware. With a low-latency HR-MEC-based transformer model on the FPGA, larger system sizes can be accommodated. The GPU is another good candidate for high-performance parallel-computing application; however, the long memory access latency and inefficient data-dependent computing prevent it from being a suitable platform either in real-time simulation or hardware-in-the-loop (HIL) applications [42]. The various I/O ports enable the FPGA-based real-time model to be interfaced to other platforms to achieve a smaller simulation time step.
- 5) The detailed real-time nonlinear HR-MEC of the power transformer emulation on the FPGA is validated using 3-D FEM under various operating conditions.

The remainder of this paper is organized as follows. Section II provides the details of the modeling and hardware design of the HR-MEC-based power transformer model. Section III provides the details of the interfacing of this transformer model to the power system network and its transient simulation. Section IV provides the case study and results to validate the emulated transformer on the FPGA. Section V gives the conclusion of this paper.

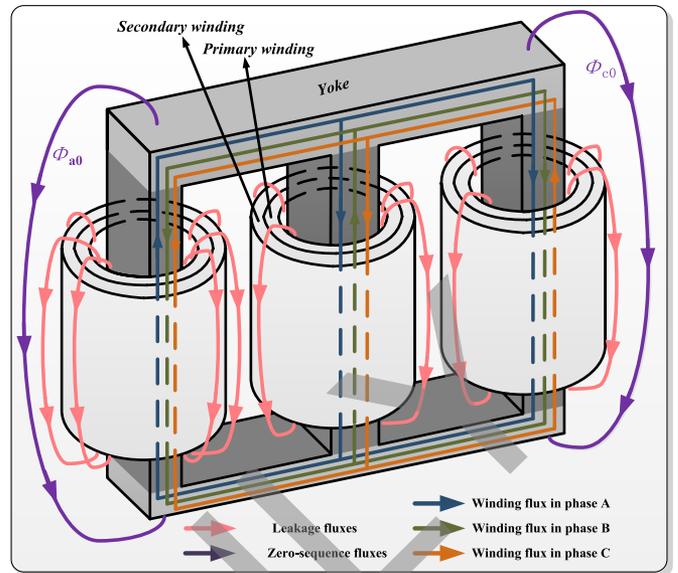


Fig. 1. Major flux paths in a three-phase three-limb transformer.

II. DETAILED HARDWARE EMULATION OF THE POWER TRANSFORMER

A. HR-MEC-Based Transformer Model

1) **HR-MEC Representation:** Fig. 1 shows a three-phase three-limb transformer with the major flux paths. The MEC representation is developed based on magnetic equivalent circuit theory [9] and can be used to represent the transformer core construction and the flux paths. The passage of various fluxes in the magnetic circuit is governed by Ampere's and Gauss' laws analogous to Kirchhoff's voltage and current laws in an electrical circuit. In the MEC, each transformer winding is represented by a permeance element and an MMF; however, the flux in the transformer winding is different at different points, even in the same winding. To obtain the detailed representation of the flux path, an HR-MEC is developed in this paper, where each coil is divided into several subcoils with a smaller number of turns. In the MEC network, this subcoil is represented by a group consisting of different values of nonlinear permeances and MMFs in the winding branches. Consequently, the linear leakage permeances are also divided to connect in parallel with each subcoil group. Fig. 2 shows the HR-MEC with two groups of subcoils in each winding for a three-phase three-limb transformer. There are three types of components in this equivalent circuit.

- 1) Nonlinear iron core permeances:
 - a) P_{pa1} , P_{pa2} , P_{pb1} , P_{pb2} , P_{pc1} , and P_{pc2} represent iron permeances for the transformer primary winding in phases a , b , and c , respectively; P_{sa1} , P_{sa2} , P_{sb1} , P_{sb2} , P_{sc1} , and P_{sc2} represent iron permeances for the transformer secondary winding in phases a , b , and c , respectively.
 - b) P_{ab} and P_{bc} represent iron permeances for the transformer yoke between phase- a and phase- b , and phase- b and phase- c , respectively.

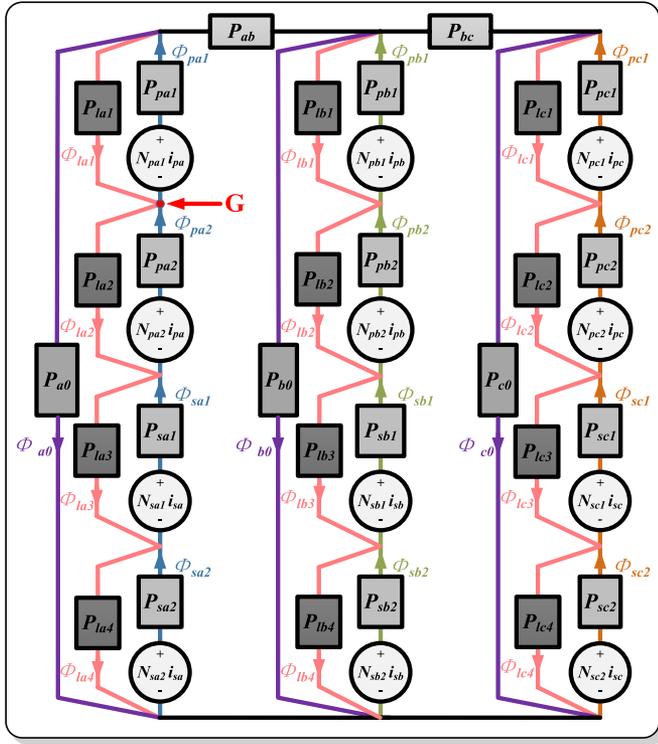


Fig. 2. HR-MEC model for a three-phase three-limb transformer.

2) Linear leakage permeances:

- P_{la1} to P_{la4} , P_{lb1} to P_{lb4} , and P_{lc1} to P_{lc4} represent the transformer leakage air permeances in phases a , b , and c , respectively.
- P_{a0} , P_{b0} , and P_{c0} are zero-sequence permeances obtained for the three phases.

3) MMF sources:

- $N_{pa1}i_{pa}$, $N_{pa2}i_{pa}$, $N_{pb1}i_{pb}$, $N_{pb2}i_{pb}$, $N_{pc1}i_{pc}$, and $N_{pc2}i_{pc}$ are generated by the currents flowing in the primary winding in phases a , b , and c , respectively; $N_{sa1}i_{sa}$, $N_{sa2}i_{sa}$, $N_{sb1}i_{sb}$, $N_{sb2}i_{sb}$, $N_{sc1}i_{sc}$, and $N_{sc2}i_{sc}$ are generated by the currents flowing in the secondary winding in phases a , b , and c , respectively.

2) HR-MEC Formulation: The relationship between the branch fluxes and the MMFs can be written as

$$\phi = \mathbf{P}(\mathbf{N}\mathbf{i} - \mathfrak{S}') \quad (1)$$

where ϕ , \mathbf{i} , and \mathfrak{S}' are $n \times 1$ vectors of branch fluxes, winding currents, and branch MMFs, respectively, expressed as $\phi = [\phi_1(t) \ \phi_2(t) \ \dots \ \phi_n(t)]^T$, $\mathbf{i} = [i_1(t) \ i_2(t) \ \dots \ i_n(t)]^T$, and $\mathfrak{S}' = [\mathfrak{S}'_1(t) \ \mathfrak{S}'_2(t) \ \dots \ \mathfrak{S}'_n(t)]^T$. n is the number of magnetic branches. \mathbf{P} and \mathbf{N} are $n \times n$ diagonal matrices of branch permeances and number of winding turns, respectively, given as

$$\begin{aligned} \mathbf{P} &= \text{diag} \{P_1(t) \ P_2(t), \dots, P_n(t)\} \\ \mathbf{N} &= \text{diag} \{N_1 \ N_2, \dots, N_n\}. \end{aligned} \quad (2)$$

The entries of vector \mathbf{i} and matrix \mathbf{N} are zero for the branches with only permeance elements.

According to the Gauss' law for magnetism, the algebraic sum of fluxes entering or leaving a node must be zero. For example, at node "G" in Fig. 2, $-\phi_{pa1} + \phi_{pa2} + \phi_{la1} = \phi_{la2}$. In general,

$$\mathbf{A}^T \phi = \mathbf{0} \quad (3)$$

where \mathbf{A}^T is the node-branch connection matrix, with 1, -1, and 0 entries for branch flux entering, leaving, and no connection to the node, respectively.

Applying matrix \mathbf{A}^T to node MMF vector $\mathfrak{S}'_{\text{node}}$ results in the branch MMF vector

$$\mathbf{A}\mathfrak{S}'_{\text{node}} = \mathfrak{S}' \quad (4)$$

Combining (1), (3), and (4) gives

$$\phi = \mathbb{P}\mathbf{N}\mathbf{i} \quad (5)$$

where

$$\mathbb{P} = \mathbf{I} - \mathbf{P}\mathbf{A}(\mathbf{A}^T\mathbf{P}\mathbf{A})^{-1}\mathbf{A}^T \quad (6)$$

with \mathbf{I} being the $n \times n$ identity matrix.

Let the permeance network fluxes be partitioned into two sets, namely, ϕ^M , for the branches with MMF sources $N_j i_j$ and permeance elements, and ϕ^P , for the branches with only permeance elements; then, (5) can be rewritten as

$$\begin{bmatrix} \phi^M \\ \phi^P \end{bmatrix} = \begin{bmatrix} \mathbb{P}^{\text{MM}} & \mathbb{P}^{\text{MP}} \\ \mathbb{P}^{\text{PM}} & \mathbb{P}^{\text{PP}} \end{bmatrix} \begin{bmatrix} \mathbf{P}^M & \mathbf{0} \\ \mathbf{0} & \mathbf{P}^P \end{bmatrix} \begin{bmatrix} \mathbf{N}^M \mathbf{i}^M \\ \mathbf{0} \end{bmatrix}. \quad (7)$$

For the three-phase three-limb HR-MEC as shown in Fig. 2, applying (7) results in

$$\phi^M = \mathbb{P}^{\text{MM}}\mathbf{P}^M\mathbf{N}^M\mathbf{i}^M \quad (8)$$

where \mathbb{P}^{MM} is a 12×12 submatrix of \mathbb{P} . ϕ^M and \mathbf{i}^M are 12×1 vectors, and \mathbf{P}^M and \mathbf{N}^M are diagonal 12×12 matrices, given as

$$\begin{aligned} \phi^M &= [\phi_{pa1}(t) \ \phi_{pa2}(t) \ \phi_{pb1}(t) \ \phi_{pb2}(t) \ \phi_{pc1}(t) \ \phi_{pc2}(t) \\ &\quad \phi_{sa1}(t) \ \phi_{sa2}(t) \ \phi_{sb1}(t) \ \phi_{sb2}(t) \ \phi_{sc1}(t) \ \phi_{sc2}(t)]^T \\ \mathbf{i}^M &= [i_{pa}(t) \ i_{pa}(t) \ i_{pb}(t) \ i_{pb}(t) \ i_{pc}(t) \ i_{pc}(t) \\ &\quad i_{sa}(t) \ i_{sa}(t) \ i_{sb}(t) \ i_{sb}(t) \ i_{sc}(t) \ i_{sc}(t)]^T \\ \mathbf{P}^M &= \text{diag} \{P_{pa1}(t) \ P_{pa2}(t) \ P_{pb1}(t) \ P_{pb2}(t) \ P_{pc1}(t) \ P_{pc2}(t) \\ &\quad P_{sa1}(t) \ P_{sa2}(t) \ P_{sb1}(t) \ P_{sb2}(t) \ P_{sc1}(t) \ P_{sc2}(t)\} \\ \mathbf{N}^M &= \text{diag} \{N_{pa1}(t) \ N_{pa2}(t) \ N_{pb1}(t) \ N_{pb2}(t) \ N_{pc1}(t) \ N_{pc2}(t) \\ &\quad N_{sa1}(t) \ N_{sa2}(t) \ N_{sb1}(t) \ N_{sb2}(t) \ N_{sc1}(t) \ N_{sc2}(t)\}. \end{aligned} \quad (9)$$

For each of the transformer windings, the terminal voltages can be derived from Faraday's law, where k denotes the winding index

$$v_k = N_{k1} \frac{d}{dt} \phi_{k1} + N_{k2} \frac{d}{dt} \phi_{k2}. \quad (10)$$

In matrix format, (10) can be rewritten as

$$\mathbf{v}_T = \mathbf{N}_Z \frac{d}{dt} \phi^M(t) \quad (11)$$

where \mathbf{N}_Z is a 6×12 winding turns matrix. \mathbf{v}_T is a 6×1 terminal voltage vector, given as

$$\mathbf{v}_T = [v_{pa}(t) \ v_{pb}(t) \ v_{pc}(t) \ v_{sa}(t) \ v_{sb}(t) \ v_{sc}(t)]^T$$

$$\mathbf{N}_Z = \begin{bmatrix} N_{pa1} & N_{pa2} & 0 & 0 & \dots & 0 & 0 \\ 0 & 0 & N_{pb1} & N_{pb2} & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \dots & N_{sc1} & N_{sc2} \end{bmatrix}.$$

3) HR-MEC Model Discretization: Applying trapezoidal rule to discretize (11), the discrete-time difference equations can be obtained

$$\mathbf{N}_Z \phi^M(t) = \frac{\Delta t}{2} \mathbf{v}_T(t) + \phi_{\text{hist}}^M(t) \quad (12)$$

where Δt is the simulation time step, with $\phi_{\text{hist}}^M(t)$ being the 6×1 history vector term expressed as

$$\phi_{\text{hist}}^M(t) = \frac{\Delta t}{2} \mathbf{v}_T(t - \Delta t) + \mathbf{N}_Z \phi^M(t - \Delta t). \quad (13)$$

Using (8), the left side of (12) can be expressed as

$$\mathbf{N}_Z \phi^M(t) = \mathbf{Z} \mathbf{i}^M \quad (14)$$

where \mathbf{Z} is a 6×12 matrix given as

$$\mathbf{Z} = \mathbf{N}_Z \mathbb{P}^{\text{MM}} \mathbf{P}^M \mathbf{N}^M. \quad (15)$$

Furthermore, (14) can be rewritten as

$$\mathbf{N}_Z \phi^M(t) = \mathbf{Z} \mathbf{i}^M = \mathbf{Z}_{(\text{HR-MEC})} \mathbf{i}_T(t) \quad (16)$$

with $\mathbf{Z}_{(\text{HR-MEC})}$ being the 6×6 matrix and $\mathbf{i}_T(t)$ being the 6×1 winding current vector, which are given as

$$\mathbf{Z}_{(\text{HR-MEC})} = \begin{bmatrix} Z_{1,1} + Z_{1,2} & \dots & Z_{1,11} + Z_{1,12} \\ Z_{2,1} + Z_{2,2} & \dots & Z_{2,11} + Z_{2,12} \\ \vdots & \vdots & \vdots \\ Z_{6,1} + Z_{6,2} & \dots & Z_{6,11} + Z_{6,12} \end{bmatrix}$$

$$\mathbf{i}_T(t) = [i_{pa}(t) \ i_{pb}(t) \ i_{pc}(t) \ i_{sa}(t) \ i_{sb}(t) \ i_{sc}(t)]^T.$$

Combining (12) and (16), the relationship between transformer terminal currents $\mathbf{i}_T(t)$ and voltages $\mathbf{v}_T(t)$ can be obtained

$$\mathbf{Z}_{(\text{HR-MEC})} \mathbf{i}_T(t) = \frac{\Delta t}{2} \mathbf{v}_T(t) + \phi_{\text{hist}}^M(t) \quad (19)$$

which finally gives the Norton equivalent formula

$$\mathbf{i}_T(t) = \mathbf{Y}_T \mathbf{v}_T(t) + \mathbf{I}_{\text{hist}T}(t) \quad (20)$$

where

$$\mathbf{I}_{\text{hist}T}(t) = \mathbf{Z}_{(\text{HR-MEC})}^{-1} \phi_{\text{hist}}^M(t) \quad (21)$$

$$\mathbf{Y}_T = \frac{\Delta t}{2} \mathbf{Z}_{(\text{HR-MEC})}^{-1}. \quad (22)$$

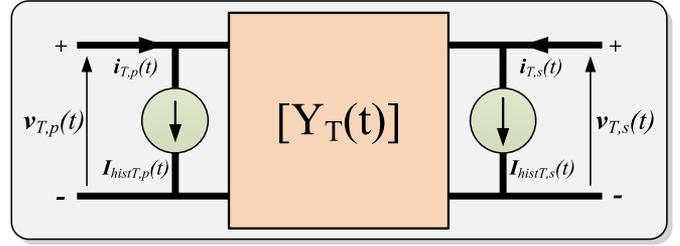


Fig. 3. Norton equivalent circuit of the HR-MEC model over one simulation time step with a time-varying admittance matrix.

The transformer terminal voltage vector in (20) $\mathbf{v}_T(t)$ can be split into two subvectors $\mathbf{v}_T(t) = [\mathbf{v}_{T,p}(t) \ \mathbf{v}_{T,s}(t)]$, where $\mathbf{v}_{T,p}(t)$ and $\mathbf{v}_{T,s}(t)$ are the primary-side and secondary-side voltage vectors, respectively. The vectors \mathbf{i}_T and $\mathbf{I}_{\text{hist}T}(t)$ can also be split into subvectors to present the primary-side current $\mathbf{i}_{T,p}(t)$ and history term $\mathbf{I}_{\text{hist}T,p}(t)$, and secondary-side current $\mathbf{i}_{T,s}(t)$ and history term $\mathbf{I}_{\text{hist}T,s}(t)$. The discrete-time Norton equivalent circuit for the HR-MEC-based transformer model is shown in Fig. 3. The inputs for this discretized model are the primary $\mathbf{i}_{T,p}(t)$ and secondary $\mathbf{i}_{T,s}(t)$ winding currents, the primary $\mathbf{I}_{\text{hist}T,p}(t)$ and secondary $\mathbf{I}_{\text{hist}T,s}(t)$ history terms, and the admittance matrix $\mathbf{Y}_T(t)$, while the outputs are the transformer primary $\mathbf{v}_{T,p}(t)$ and secondary $\mathbf{v}_{T,s}(t)$ terminal voltages, calculated by its nodal analysis method. Since the nonlinear permeance matrices \mathbb{P}^{MM} and \mathbf{P}^M in (15) are time varying, the resulting admittance matrix \mathbf{Y}_T is not constant but needs to be recalculated in every simulation time step. Thus, an efficient parallel LU decomposition solver, described in Section III-B, is used for the network solution. This is the significant difference from a lumped-parameter-based transformer model such as the BCTRAN model [2], in which the admittance matrix is constant.

4) HR-MEC Model Hardware Design: It is obvious from the equations involved in the HR-MEC calculation process that matrix–matrix multiplications are necessary. Some of the matrices are sparse matrices, such as \mathbf{A} , \mathbf{P} , \mathbf{N} . The entries in these sparse matrices may keep changing in each emulation time step, but the pattern remains unchanged. In order to reduce the computational latency, a sparse–dense matrix multiplication unit (SMxDM) has been developed for this purpose. Two example matrices and their corresponding storage formats are shown in Fig. 4. As shown in Fig. 4(b), three RAMs are defined to store the two matrices: 1) two 32-b-wide RAMs rmA and rmB to store the value of the matrix entries of sparse matrix \mathbf{A} and dense matrix \mathbf{B} in row and column order, respectively, and 2) a 20-b-wide RAM $rmcfg$ consisting of the first bit sel is used to label the same column entries in rmB with “0” or “1,” the middle 11-b adb to store the address in rmB , the last 8-b ada to store the address in rmA , due to the fact that sparse matrices contain less number of entries than dense matrices. This storage scheme can be extended to save larger size matrix easily.

In Fig. 5(a), the three RAMs rmA , rmB , and $rmcfg$ are generated by the aforementioned rules. The signals ada , adb , and $adcfg$ are controlled to access the three RAMs sequentially, and the data are sent to the multiplication accumulator

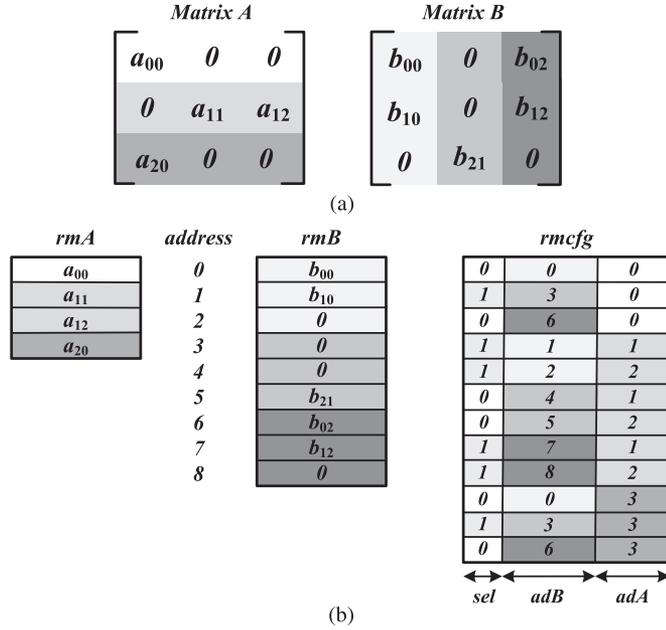


Fig. 4. Sparse matrix storage format. (a) Example matrices. (b) Corresponding storage formats.

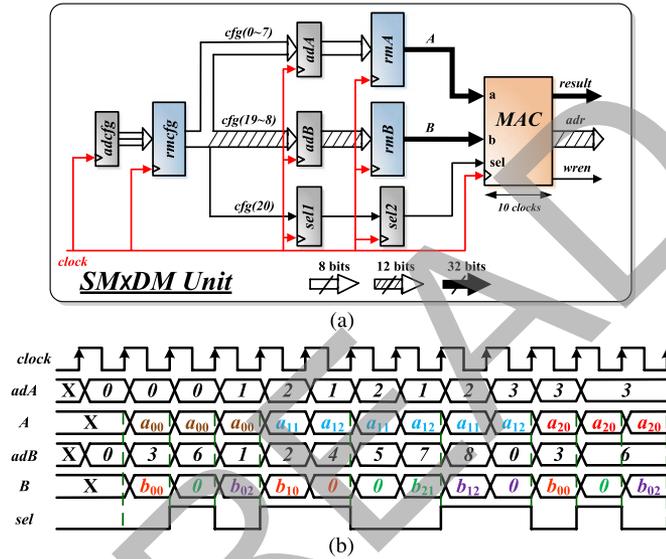


Fig. 5. Pipelined design for the sparse-dense matrix multiplication SMxDM unit. (a) Hardware design. (b) Timing diagram.

calculation unit (MAC) in the pipeline to perform the matrix multiplication. The timing diagram of this operation is shown in Fig. 5(b).

The MAC unit, as shown in Fig. 6(a), consists of one floating point multiplier, one floating-to-fix point converter, one fixed-to-floating point converter, and two fixed-point adders. The reason to employ a fixed point adder instead of a floating point adder here is to increase the maximum frequency purpose when the addition operation is forced to finish in one clock cycle. The fixed point results are converted back to floating point to get involved in further computations. Moreover, the two fixed point adders with opposite reset signals are for the pipeline

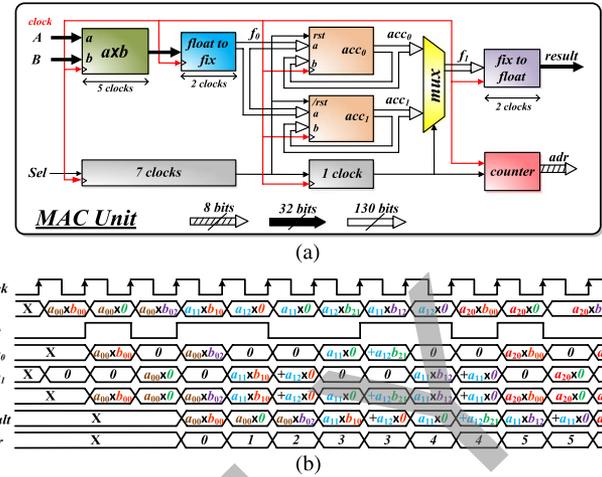


Fig. 6. Pipelined design for the multiplication-accumulator calculation MAC unit. (a) Hardware design. (b) Timing diagram.

purpose so that there is no stall between two row-column multiplications, as shown in the timing diagram of the MAC unit in Fig. 6(b). The fixed point result signals f_1 are converted back to floating point result signals $result$ in two clock cycles, and the signal adr increases by one if signal sel is changed. The inserted registers are used for synchronization purpose.

The SMxDM hardware implementation can also be used to perform dense-sparse, sparse-sparse, and sparse-diagonal matrix multiplications. The sparse and diagonal matrices can be treated as a special dense matrices, and for these matrix multiplications, the rmA , rmB , and $rmcfg$ are generated by similar rules.

B. PHU

The diagonal matrix P is composed of linear entries and nonlinear entries. The linear entries representing the leakage and zero-sequence permeances are constant; however, the nonlinear entries representing the winding and yoke permeances change in every simulation time step so that a nonlinear evaluation unit is needed to model this phenomenon. In this paper, in order to further include the hysteresis behavior, the Preisach model [15] was selected to represent the nonlinearity.

The major loop hysteresis function is geometrically represented by the following hyperbolic function [15]

$$\phi_{p-m}(i_m) = \frac{1}{2} \sum_{u=1}^3 a_u [\tanh(b_u i_m) + c_u \operatorname{sech}^2(b_u i_m)] \quad (23)$$

where a_u , b_u , and c_u are the parameters used to define this hyperbolic template, $i_m = [i_{m1} \ i_{m2} \ \dots \ i_{mnl}]^T$ is the magnetization current vector flowing through the nonlinear elements, and $\phi_{p-m} = [\phi_{p-m1} \ \phi_{p-m2} \ \dots \ \phi_{p-mnl}]^T$ are the fluxes corresponding to this current vector on the major loop. The subscript “p_m” stands for the Preisach major loop, and n_l stands for the number of nonlinear permeance.

Once the major loop function is fixed, all of the minor loop trajectories from a reversal point follow this uniform

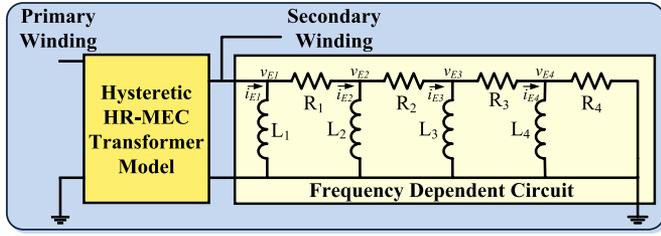


Fig. 7. Caer equivalent circuit coupled to the hysteretic HR-MEC model for representation of eddy currents.

template. In general, Preisach upward ϕ_{p_u} and downward ϕ_{p_d} trajectories from a reversal point (i_{rl}, ϕ_{rl}) can be expressed as (24) and (25), respectively [16], with $\mathbf{i}_r = [i_{r1} \ i_{r2} \ \dots \ i_{rn_l}]^T$ and $\phi_r = [\phi_{r1} \ \phi_{r2}, \dots, \phi_{rn_l}]^T$

$$\begin{aligned} \phi_{p_u}(i_m) = & -\phi_{p_m}(-i_m) - \phi_{p_m}(i_r) + \phi_r \\ & + 2\mathbf{K}(-i_r)\mathbf{K}(i_m) \end{aligned} \quad (24)$$

$$\begin{aligned} \phi_{p_d}(i_m) = & \phi_{p_m}(i_m) + \phi_{p_m}(-i_r) + \phi_r \\ & - 2\mathbf{K}(i_r)\mathbf{K}(-i_m) \end{aligned} \quad (25)$$

where

$$\begin{aligned} \mathbf{K} = & [K_1 \ K_2, \dots, K_{n_l}] \\ K_l(x) = & \begin{cases} \sqrt{\phi_{p_m}(-x)}, & x < 0 \\ \frac{\phi_{p_m}(-x) + \phi_{p_m}(x)}{2\sqrt{\phi_{p_m}(x)}}, & x > 0 \end{cases} \\ & l = 1, 2, \dots, n_l. \end{aligned}$$

After calculating the vector ϕ^M (composed of ϕ_{p_u} and ϕ_{p_d}) by using (8), the magnetizing current vector \mathbf{i}_m can be obtained from (24) and (25). The k th branch nonlinear permeance P_k can then be calculated as

$$P_k = \frac{\phi_k^M}{i_{mk} N_k} \quad (26)$$

where N_k is the number of the k th winding turns.

C. Frequency-Dependent Eddy Current Model

The eddy currents in the transformer core are induced by the alternating flux and seek to redistribute the flux in the core. The eddy current which is a frequency-dependent current heats the core, which is, in turn, dissipated as the transformer core loss. In this paper, a cascade $R-L$ lumped circuit (Caer equivalent circuit) [17] was chosen to represent the frequency-dependent eddy current phenomena in the transformer core. As shown in Fig. 7, four $R-L$ circuits are coupled with the hysteretic HR-MEC-based transformer model. The accuracy of this representation depends on the number of $R-L$ sections, and four sections are considered enough to accurately represent the behavior up to 200 kHz with an error less than 5%. The parameter determination of the Caer model can be found in [18]. After discretizing the cascaded $R-L$

equivalent circuit, the Norton equivalent formula is given as (27), where $\mathbf{i}_E(t) = [i_{E1}(t) \ i_{E2}(t) \ i_{E3}(t) \ i_{E4}(t)]^T$ and $\mathbf{v}_E(t) = [v_{E1}(t) \ v_{E2}(t) \ v_{E3}(t) \ v_{E4}(t)]^T$ are the node current and voltage vectors, respectively, and $\mathbf{I}_{\text{hist}E}(t)$ is the eddy current history term vector which is updated by (28)

$$\mathbf{i}_E(t) = \mathbf{Y}_E \mathbf{v}_E(t) + \mathbf{I}_{\text{hist}E}(t) \quad (27)$$

$$\mathbf{I}_{\text{hist}E}(t) = \mathbf{G}_E \mathbf{v}_E(t - \Delta t) + \mathbf{I}_{\text{hist}E}(t - \Delta t) \quad (28)$$

where

$$\mathbf{G}_E = \text{diag} \left\{ \frac{\Delta t}{2L_1} \ \frac{\Delta t}{2L_2} \ \frac{\Delta t}{2L_3} \ \frac{\Delta t}{2L_4} \right\}. \quad (29)$$

III. POWER SYSTEM NETWORK TRANSIENT SIMULATION

A. Interfacing of the HR-MEC-Based Transformer Model to the Power System Network

The interfacing of the real-time hysteretic HR-MEC-based transformer model to the power system network is shown in Fig. 8. The supervisor module sends a command signal (\mathbf{cmd}) to each module to enable it to perform the designed function and also waits to receive the signals sent back from each module, so that all modules can work either in parallel or sequentially as required by the power system transient algorithm. The transformer parameters saved in the initial RAMs are sent to the proper calculation units involved. The nonlinear permeance matrix \mathbf{P}^M computed by the Preisach hysteresis unit (PHU), combined with linear permeance matrix \mathbf{P}^P , gives the overall permeance matrix \mathbf{P} . After calculating the matrix \mathbb{P} by (6), the matrices \mathbf{Z} and $\mathbf{Z}_{(\text{HR-MEC})}$ are computed by (15) and (17). As indicated by (21) and (22), the matrix $\mathbf{Z}_{(\text{HR-MEC})}$ needs to be inverted to obtain the transformer admittance matrix \mathbf{Y}_T and history term vector $\mathbf{I}_{\text{hist}T}$. A LU-based inverse matrix calculator (IMC) described in Section III-B is used to invert the matrix. As shown in Fig. 8, the entire power system network admittance matrix \mathbf{Y} is composed of the transformer admittance matrix \mathbf{Y}_T and the remainder power system network admittance matrix \mathbf{Y}_N . The history term vector \mathbf{I}_{hist} is the summation of the transformer history term $\mathbf{I}_{\text{hist}T}$, the eddy current history term $\mathbf{I}_{\text{hist}E}$, and the other power system network history term $\mathbf{I}_{\text{hist}N}$. Then, the network solver model, consisting of a LU decomposition (LUD), a forward substitution unit (FWS), and a backward substitution unit (BWS), is executed to find the power system network nodal voltages \mathbf{v} which are displayed on the oscilloscope through a digital-to-analog converter board and are also sent back to the other power system models, as well as the eddy current model to update their respective history terms. The permeance network's flux term ϕ^M is updated by metering the transformer terminal currents in (8), and the history term ϕ_{hist}^M is updated by (13).

Fig. 9 shows the detailed finite state machine (FSM) for this hardware design. In state S_1 , the transformer winding and yoke fluxes are updated, and the eddy current module and the linear passive element and transmission line modules update their history terms $\mathbf{I}_{\text{hist}E}$ using (28) and $\mathbf{I}_{\text{hist}N}$ in parallel. State S_2 performs two functions in parallel: 1) updates the

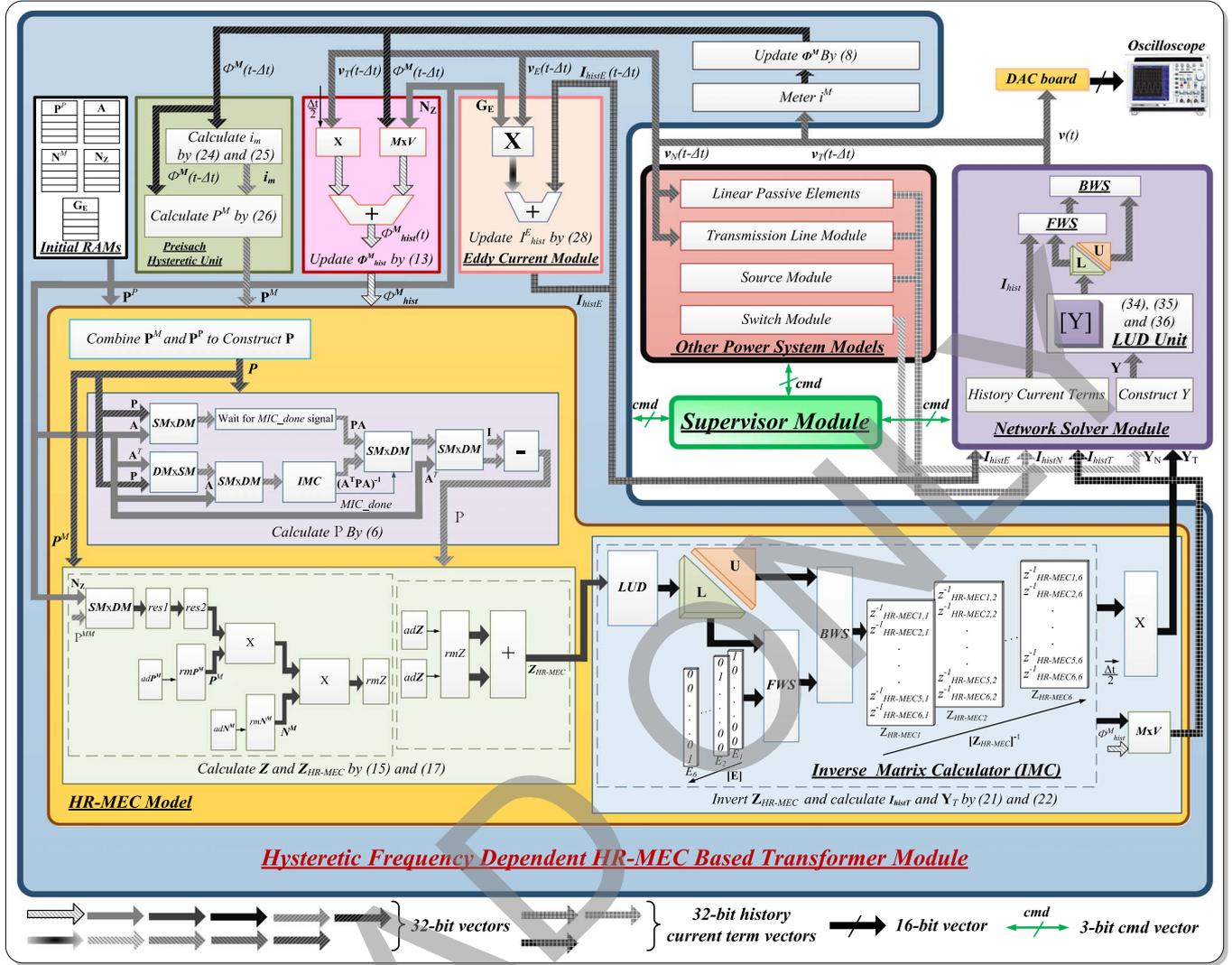


Fig. 8. Hardware design of the interface between the HR-MEC transformer model and the power system network for transient simulation.

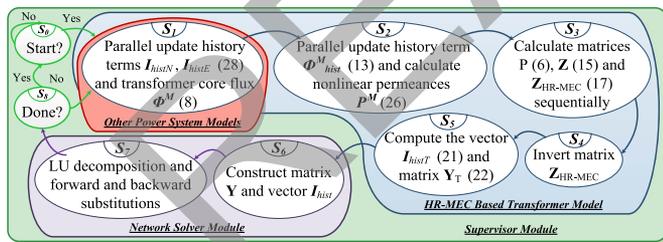


Fig. 9. FSM of the supervisor module in Fig. 8.

transformer history term ϕ_{hist}^M using (13) and 2) calculates the nonlinear permeance values in the PHU. State S_3 calculates matrices \mathbb{P} , \mathbb{Z} , and $\mathbb{Z}_{(\text{HR-MEC})}$ sequentially from (6), (15), and (17), respectively. State S_4 inverts matrix $\mathbb{Z}_{(\text{HR-MEC})}$, and state S_5 computes the vector $\mathbf{I}_{\text{histT}}$ and the matrix \mathbf{Y}_T from (21) and (22), respectively. State S_6 calculates the summation of all of the history current terms \mathbf{I}_{hist} and constructs the entire power system network matrix \mathbf{Y} . State S_7 performs LU decomposition and forward and backward substitutions to obtain the nodal network voltages \mathbf{v} .

B. LU-Decomposition-Based Network Solver Module

In the power system transient simulation algorithm, the nodal analysis formulation results in the following equation for each simulation time step:

$$\mathbf{Y}\mathbf{v} = \mathbf{i} - \mathbf{I}_{\text{hist}} \quad (30)$$

where \mathbf{Y} is an $n \times n$ admittance matrix and \mathbf{v} , \mathbf{i} , and \mathbf{I}_{hist} are the $n \times 1$ nodal voltage, node injection current, and history current vectors, respectively, in which n denotes the total number of nodes of the modeled power system. In this paper, instead of inverting the matrix \mathbf{Y} , the vector of \mathbf{v} is calculated by an LU-based network solver. Previous works on FPGA-based LU implementations have been reported; however, in some of these works, fixed-point or single-precision floating point is employed [19], which gives low accuracy. In the LU solver in [20], part of the factorization is done in a host microprocessor, which increased the amount of communication between the microprocessor and the FPGA. The other LU-based solvers [21], [22] are developed based on the block LU decomposition algorithm to partition the \mathbf{Y} into several blocks. With these

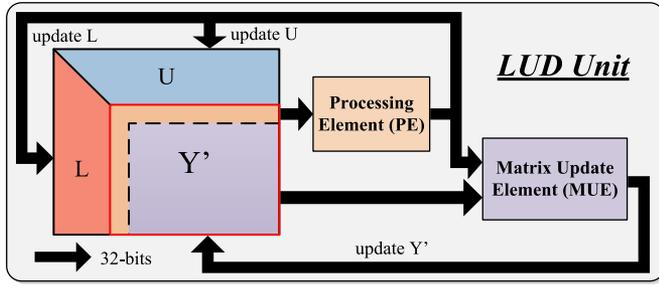


Fig. 10. LU decomposition hardware design.

algorithms, the efficiency of the solver is improved by overlapping the communication and the computation; however, the block decomposition algorithm is reported to have numerical problems and cannot be used in all cases [23]. The LU-based network solver presented in this work is developed using 32-bit floating point precision for high accuracy and implemented entirely on FPGA without communication with a host processor. The implementation is fully pipelined and paralleled to achieve real-time simulation.

The LU factorization of an $n \times n$ matrix \mathbf{Y} into a lower triangular $n \times n$ matrix \mathbf{L} and an upper triangular $n \times n$ matrix \mathbf{U} can be written as

$$\mathbf{Y} = \mathbf{L}\mathbf{U}. \quad (31)$$

The relationship between the entries of \mathbf{Y} and \mathbf{L} and \mathbf{U} is given as

$$l_{i,k} = \frac{y_{i,k} - \sum_{r=1}^{k-1} l_{i,r}u_{r,k}}{u_{k,k}} \quad (32)$$

where $k = 2, \dots, n-1$ and $i = k+1, \dots, n$, and

$$u_{k,j} = y_{k,j} - \sum_{r=1}^{k-1} l_{k,r}u_{r,j} \quad (33)$$

where $k = 2, \dots, n$ and $j = k, \dots, n$.

By expanding the summation components in (32) and (33), the LU decomposition of the $n \times n$ matrix can be finished in n iterations, and there are two steps in each iteration. In the k th iteration, the first step is to find the k th column of the matrix \mathbf{L} , $l_{i,k}$ by

$$l_{p,k} = \frac{y_{p,k}}{y_{k,k}}, \quad p = k, \dots, n \quad (34)$$

and the k th row of the matrix \mathbf{U} is found by

$$u_{k,q} = y_{k,q}, \quad q = k, \dots, n. \quad (35)$$

In the second step of each iteration, the $(n-k) \times (n-k)$ submatrix \mathbf{Y}' at the right down corner of matrix \mathbf{Y} is updated by

$$y_{p,q} = y_{p,q} - l_{p,k}u_{k,q}, \quad p, q = k+1, \dots, n. \quad (36)$$

In the LUD unit, as shown in Fig. 10, the entries in the first row and the first column of the submatrix \mathbf{Y}' are sent to the processing element (PE) to calculate the elements of \mathbf{L} and \mathbf{U} by (34) and (35), respectively. Then, the calculated entries of \mathbf{L}

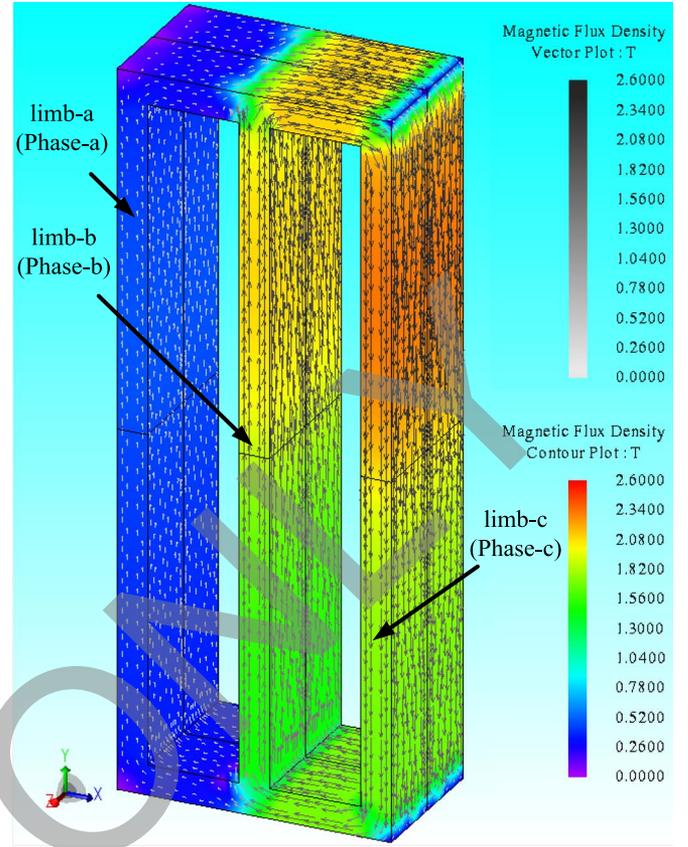


Fig. 11. Magnetic flux density distribution of the modeled transformer in JMAG Designer at the peak of the phase-c current.

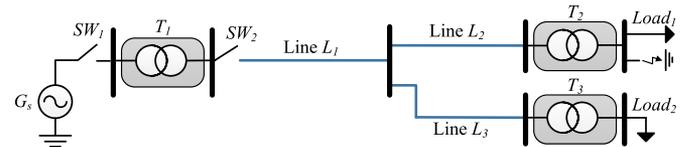


Fig. 12. Single-line diagram of the modeled power system for the case study with the HR-MEC-based transformer model.

and \mathbf{U} , as well as the rest of the entries of submatrix \mathbf{Y}' , are sent to the matrix update element (MUE) to update the matrix \mathbf{Y}' .

An LU-based IMC is developed in this paper to compute the inverse matrices in (6), (21), and (22). The multiplication of an $n \times n$ square matrix \mathbf{A} and its inverse matrix \mathbf{A}^{-1} must be an identity matrix \mathbf{E}

$$\mathbf{A}\mathbf{A}^{-1} = \mathbf{E} \quad (37)$$

which can be expressed as

$$\mathbf{A} [\mathbf{A}_1^{-1} \mathbf{A}_2^{-1}, \dots, \mathbf{A}_n^{-1}] = [\mathbf{E}_1 \mathbf{E}_2, \dots, \mathbf{E}_n] \quad (38)$$

where \mathbf{A}_k^{-1} and \mathbf{E}_k are the k th column of matrices \mathbf{A}^{-1} and \mathbf{E} ($k = 1, 2, \dots, n$), respectively. By applying forward and backward substitutions to the following equation:

$$\mathbf{A}\mathbf{A}_k^{-1} = \mathbf{E}_k \quad (39)$$

the vector \mathbf{A}_k^{-1} can be obtained. As shown in Fig. 8, in the IMC, the matrix $\mathbf{Z}_{\text{HR-MEC}}$ undergoes LU factorization only once. The

TABLE I
MODULE LEVEL HARDWARE RESOURCE UTILIZATION AND OPERATOR IMPLEMENTATION

	Slice Registers	Slice LUTs	BRAM/FIFO	DSP48E1	BUFG	Adder	Multiplier	Divider
HR-MEC Module	79160 (13%)	122255 (40.3%)	85 (2.8%)	746 (26.6%)	12 (37.5%)	147	146	34
Network Solver Module	15996 (2.6%)	26221 (8.6%)	21 (0.7%)	151 (5.4%)	1 (3.1%)	37	36	11
Transmission Line Module	2600 (0.4%)	6434 (2.1%)	22 (0.7%)	32 (1.1%)	3 (9.3%)	6	10	0
Source Module	851 (0.1%)	9787 (3.2%)	1 (0.0%)	6 (0.0%)	0 (0.0%)	2	1	0

vector E_k ($k = 1, 2, \dots, 6$) is pushed into the input port of FWS sequentially, and the vector $Z_{(HR-MEC)k}^{-1}$ is obtained at the output port of BWS.

IV. CASE STUDY AND REAL-TIME SIMULATION RESULTS

A. Validation by Finite-Element Simulation

A 3-D FEM is built in the JMAG Designer for a three-phase 187.5-MVA transformer to validate the hardware emulation of the developed HR-MEC model. The ratings of the transformer and the geometric parameters are given in the Appendix. A half transformer core and coil model was developed in the FEM software, and the full transformer model was simulated by setting the symmetry boundary and using the full model and circuit conversion features of JMAG. The size of the element is 0.15 m, and there are 37750 elements and 7753 nodes to build the mesh of the half transformer. The nonlinearity is solved by employing the Newton–Raphson method, and the maximum number of iteration is set to 50 to ensure convergence in every time step. The primary side of the built transformer is fed by a three-phase voltage source with the secondary side open. After energizing the transformer, an inrush current flows through the coil of the primary side, and the simulated magnetic flux density contour and vector plot is shown in Fig. 11 when the current in phase-*c* reaches its peak value. As can be seen, the direction of the flux lines in limb-*c* is different from the direction of limb-*a* and limb-*b* because the current directions are different between phase-*c* and phase-*a* and phase-*b*. The flux lines in limb-*b* and limb-*c* flow into limb-*c*, which results in the limb-*c* being the most saturated limb and the maximum flux density is close to 2.6 T. This highly saturated limb-*c* results in the phase-*c* inrush current being higher compared to the inrush currents in phase-*a* and phase-*b*. The JMAG Designer took almost 13 h to run a 4-s simulation with the step time $\Delta t = 500 \mu\text{s}$ on a PC featured by Intel i7 CPU and 8-GB memory. The precomputed method is another candidacy approach to predict the behaviors of the transformer, which computes the values in advance in JMAG Designer and stores them in LUTs to save simulation time. However, it is very difficult to build a large enough LUT to save all of the results when the transformer is under all different circumstances, due the long simulation time and including massive circumstances, especially under the transient conditions.

B. Case Study

In the case study, a power system network shown in Fig. 12 is emulated to show the accuracy and effectiveness of the

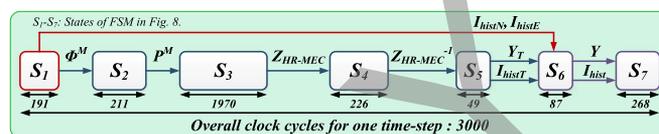


Fig. 13. Latencies for one emulation time step for the HR-MEC-based transformer model emulation.

proposed real-time nonlinear frequency-dependent HR-MEC transformer model. The network consists of three transformers (T_1, T_2, T_3), modeled by the HR-MEC transformer model, and three transmission lines (L_1, L_2, L_3), modeled by the distributed parameter line model. The primary side of transformer T_1 is fed by a three-phase voltage source G_s through a circuit breaker SW_1 . The system parameters are listed in the Appendix. The real-time detailed nonlinear transformer EMT model and other power system network models were emulated on the Xilinx Virtex-7 VC707 XC7VX485T device, and the module level hardware resource utilizations and number of operator implementations are summarized in Table I. The maximum clock frequency for this design was 90 MHz. The detailed latencies of the model for each simulation time step are also summarized and shown in Fig. 13. In this figure, the latency is labeled for each FSM in Fig. 9, and the overall latency is 3000 clock cycles. With the maximum frequency of 90 MHz, the execution time for one simulation time step is $34 \mu\text{s}$. During one simulation time step for the HR-MEC model, 5816 floating point operations are carried out, resulting in 0.17 GFLOPS. The Coregen provided by ISE is used to generate the basic 32-b floating point operations such as adder and subtractor which are further employed to implement the other complex functional units such as SMxDM and LUD. The maximum frequency of the generated operations can reach up to 500 MHz; however, for the HR-MEC-based real-time transformer model, the maximum frequency is 90 MHz. This is mainly due to the massive operations involved in each clock cycle that result in high complexity of the hardware implementation which increases the latency between two flip-flops. Moreover, the other sequential statements in the VHDL textural program such as the *if* and *case* statements can also increase the complexity of the hardware implementation and result to a decreased maximum frequency that can be achieved in this hardware emulation model.

1) **Energization Transients and Steady-State Waveforms:** For the energization transient study, initially, the circuit breakers SW_1 and SW_2 are opened. The energization current transient is simulated by closing SW_1 at time $t = 0.05$ s, and the real-time three-phase breaker current results are captured and plotted along with the JMAG Designer simulation results

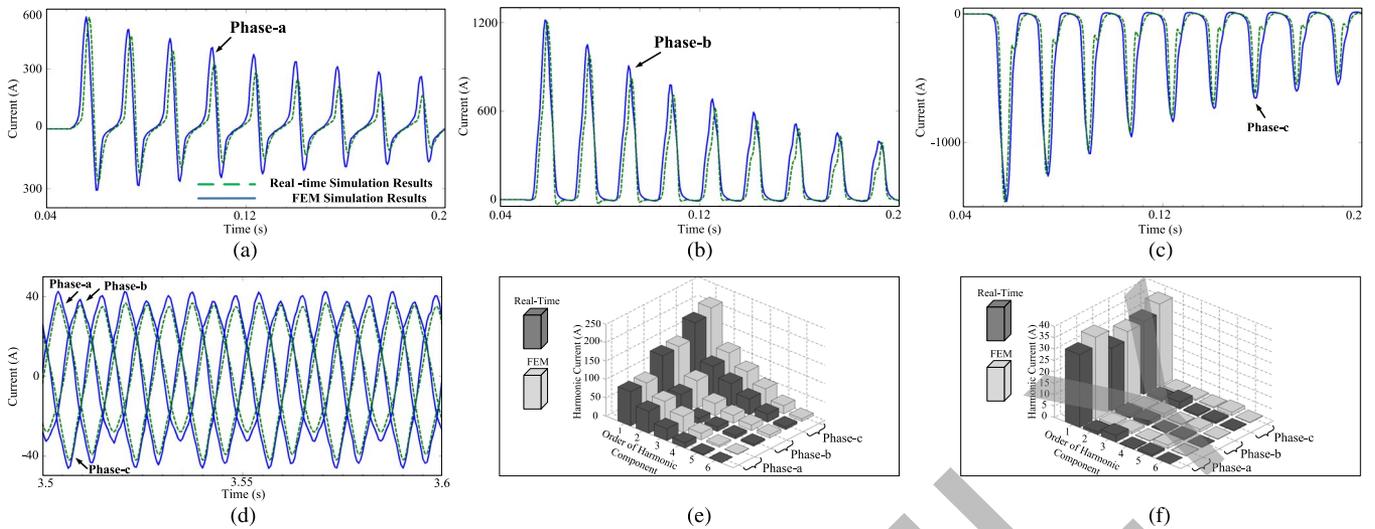


Fig. 14. Real-time and JMAG Designer simulation results. (a)–(c) Energization transient current. (d) Steady-state current. (e) Frequency analysis of the energization transient current. (f) Frequency analysis of the steady-state current.

in Fig. 14(a)–(c). In these waveforms, the phase-*b* and phase-*c* currents are seen to be of larger magnitude compared to the phase-*a* current due to the different values of supplied voltage at the instant of energization. All of the currents decay to steady state after 3.5 s as shown in Fig. 14(d). While there is a close agreement of the wave shape of inrush currents between the real-time and FEM results, small discrepancies exist in the magnitudes. That is because, for the HR-MEC model, the initial fluxes in each limbs cannot be all zero; otherwise, the entries in matrix \mathbf{P} would be all zero, which, in turn, makes the term $\mathbf{A}^T \mathbf{P} \mathbf{A}$ in (6) cannot be inverted. Thus, in the HR-MEC model, the initial fluxes are assigned to very small values close to zero; however, in the FEM simulation, the initial fluxes are all zero. Another reason is that, even though the real-time model is based on an HR-MEC approach, the mesh size is still much smaller compared to that of the 3-D FEM simulation. Despite these discrepancies, the proposed HR-MEC model provides acceptably accurate results and runs in real time compared to the long execution time of the FEM simulation.

The frequency analyses of the transient state from $t = 0.04$ s to $t = 0.2$ s and the steady state from $t = 3.5$ s to $t = 4$ s are also given in Fig. 14(e) and (f) as the order of harmonic components with respect to harmonic current magnitude. As can be seen, under steady state, only the fundamental is the dominant component; however, for the transient state, the harmonic components of orders 2 and 3 have larger values than the other order harmonic components, which is due to the high nonlinear distortion current in each phase when the transformer is energized. In both transient and steady states, the harmonic current values of the FEM simulation results are somewhat different from those of the real-time simulation results due to the reason given previously. The maximum differences under transient and steady states both happen in the first order of phase-*c*, which are 9% and 11%, respectively.

2) Fault Transients: The fault transient simulation was achieved by creating a three-phase ground fault at the secondary winding of T_2 at $t_1 = 2$ s, and the voltage and current wave-

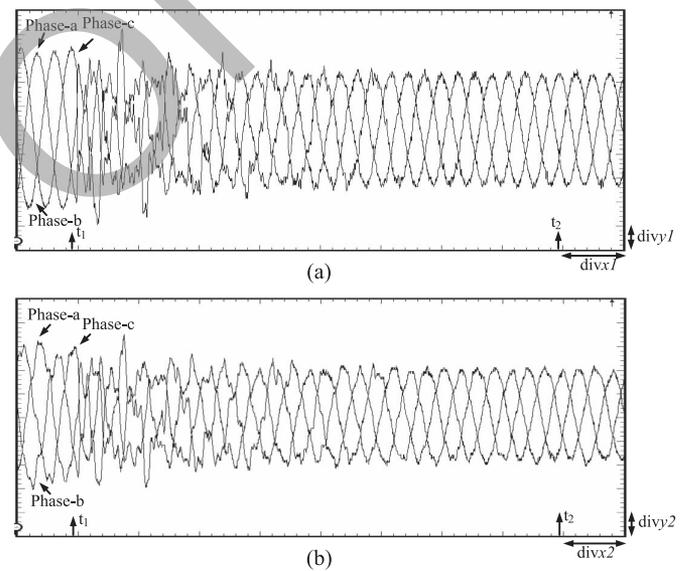


Fig. 15. Ground fault at $t_1 = 2$ s real-time simulation results. (a) Transient voltage waveform ($1 \text{div}x1 = 20$ ms; $1 \text{div}y1 = 20$ kV). (b) Transient current waveform ($1 \text{div}x2 = 20$ ms; $1 \text{div}y2 = 39$ A).

forms at the primary winding of T_3 are captured in real time on the oscilloscope. As shown in Fig. 15(a), both waveforms are highly distorted, and the distorted voltage magnitude is up to 121% of the steady-state voltage, and the currents are unbalanced in the three phases. The fault voltage and current waveforms decay to steady state after $t_2 = 2.16$ s.

V. CONCLUSION

This paper has proposed an FPGA-based digital hardware emulation of an HR-MEC nonlinear frequency-dependent real-time power transformer model. This model is fully paralleled and deeply pipelined in hardware to achieve real-time simulation with low hardware resource utility. The proposed real-time

model is able to accurately predict the transformer behavior under both transient- and steady-state conditions. The low latency of the proposed HR-MEC model makes it suitable for closed-loop HIL simulation setups to test power system protection and control systems. This FPGA-based model can also be employed to design a power transformer because the geometry-oriented features, within much shorter time compared to FEM, can also predict the local information of the transformer, such as flux distribution in the core, which are the advantages over a simpler transformer model such as the matrix representation model. Future work would include extending the HR-MEC model for a multiwinding transformer for power flow control applications in power systems.

APPENDIX

- A) Geometry parameters of the transformer: limb length: 3.59 m, limb cross-sectional area: 0.454 m^2 , yoke length: 2.66 m, and yoke cross-sectional area: 0.454 m^2 .
- B) Parameters of the case study, for energization transient: voltage source G : 130.6 kV; transformer T_1 : 187.5 MVA, 65 kV/450 kV.
- C) Parameters of the case study, for fault transient: voltage source G : 10 kV; load Load_1 : 100Ω ; Load_2 : 50Ω and 10 mH ; transformer T_1 : 187.5 MVA, 65 kV/350 kV, $X_{\text{leakage}} = 0.113 \text{ p.u.}$, Y-Y connection; transformer T_2 : 187.5 MVA, 350 kV/60 kV, $X_{\text{leakage}} = 0.113 \text{ p.u.}$, Y-Y connection; transformer T_3 : 187.5 MVA, 350 kV/100 kV, $X_{\text{leakage}} = 0.113 \text{ p.u.}$, Y-Y connection. Transmission line inductance: mode 0: $5.819 \times 10^{-7} \text{ H/m}$, mode +: $1.556 \times 10^{-7} \text{ H/m}$; transmission line capacitance: mode 0: $0.012 \times 10^{-8} \text{ F/m}$, mode +: $0.0194 \times 10^{-8} \text{ F/m}$; transmission lines L_1 , L_2 , and L_3 : 10, 200, and 160 km.

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