DSP-Based PWM Carrier Transition Technique for Parallel Connected Two-level VSCs

by

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Abstract

The developments in the field of electrical engineering over the years have expanded the types of electricity generation, distribution and utilization. With these developments, power conversion plays an important role. As the demand grows, higher power handling capacity is expected of the converters. Three-phase two level voltage source converters are connected in parallel to increase the current rating and thereby meet the increasing power handling requirement under restrained voltages. Interleaved switching of parallel converters improves the system performance and can be achieved using phase-shifted carrier-based PWM. The line-to-line voltage can be further improved by alternating between two sets of carriers, although it results in jumps in the circulating current and in the flux in the inductor cores between the parallel inverters.

A transition technique to switch between carriers is presented, which eliminates the jumps in the circulating currents and the flux. The technique uses high frequency transitional carriers to switch from one set of carriers to the other. This technique ensures that the output voltage is unaffected and the output current waveforms are glitch-free during the transitions, which is an important feature over the techniques in already existing literature. The high frequency carrier transition technique is generalized for an arbitrary number of parallel converters and is tested in a coupled inductor inverter with 2 inverter legs per phase connected in parallel. It is implemented in a low-cost DSP environment. Sawtooth carriers are used to transition between carriers with different frequencies easily and reliably. But to maintain the quality of the output similar to that of the triangular carriers, the reference and the PWM switching logic is manipulated appropriately.

The effectiveness of the developed PWM technique has been verified using simulations and experimental results obtained with a dc link voltage of 300 V. The performance of the technique is compared with regular phase-shifted PWM and enhanced phase-shifted PWM where carriers are changed instantaneously. The circulating currents, flux in the cores, line-to-line output voltages and load currents show significant improvement over the other techniques.

~To My Mother and Father~

Acknowledgement

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– Dohitha Yapa

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Abbreviations

CSC	Current Source Converter
DSP	Digital Signal Processor
DSC	Digital Signal Controller
EV	Electric Vehicle
GTO	Gate Turn-Off Thyristor
HF	High Frequency
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
MMF	Magnetomotive Force
PD	Phase Disposition
PS	Phase Shift
PWM	Pulse Width Modulation
SV	Space Vector
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

Chapter 1

Introduction

Power conversion technologies have been in the spotlight in recent years with developments in applications involving electrical energy. Electric vehicles (EVs), EV chargers, distributed generation, expansion of large-scale and medium scale renewable energy generation in addition to modifications in the existing network to accommodate rising demands involve different types of power conversion scenarios. A commercially viable solutions demand cost effectiveness, simplicity, and compactness in addition to the technical performance (quality of the output, efficiency) [1].

Voltage-source converters are one of the most widely used type of converters, and they can be connected in parallel to achieve higher currents ratings. The flow of circulating currents among the paralleled converters, integration of coupled inductors and different PWM techniques to improve the quality of the output are discussed. The complications created by the existing PWM techniques are identified leading in to the thesis statement.

1.1 Power Converters

Power converters can be categorized in different ways [2]. Type of the inputs/outputs (ac or dc), power electronic switches used, direction of power flow, nature of commutation and many other criteria has been used for the classification. Out of many different types, ac/dc converters are the focus of the work presented in this thesis.

Ac/dc converters can be further classified into subcategories. One of the most common types of classification is based on the nature of the dc side of the converter.

- Current-source Converter (CSC): In CSCs, the dc side of the converter acts as a current source; i.e., the polarity of dc current does not change. Hence, to regulate the direction of the power flow, the polarity of the dc side voltage needs to be reversed.
- Voltage-source Converter (VSC): In VSCs, the dc side acts as a voltage source, with a stiff dc voltage polarity and the power flow can be regulated by reversing the direction of the dc current.

CSCs haven't gained much popularity as the VSCs due to the lack of availability of fast, fully controllable bipolar switches which are required to reverse the voltage polarity. Even the bipolar GTOs and IGCTs are limited in switching speeds [2], [3].

On the other hand, VSCs require reverse conducting switches and those are available in the form of IGBTs and also reverse conducting IGCTs. Hence, VSCs have been predominantly popular over the CSC.

CSCs have been widely used in HVDC applications, but with increased ratings of new semiconductor devices and modular circuit topologies are gaining popularity in those applications as well.

Therefore, VSCs have been the focus of work presented herein too.

1.2 Voltage-Sourced Converters

Two-level VSC is one of the simplest 3-phase converter topologies, Fig. 1.1. With regular sinusoidal PWM it produces a line-to-line voltage as shown in Fig. 1.2.

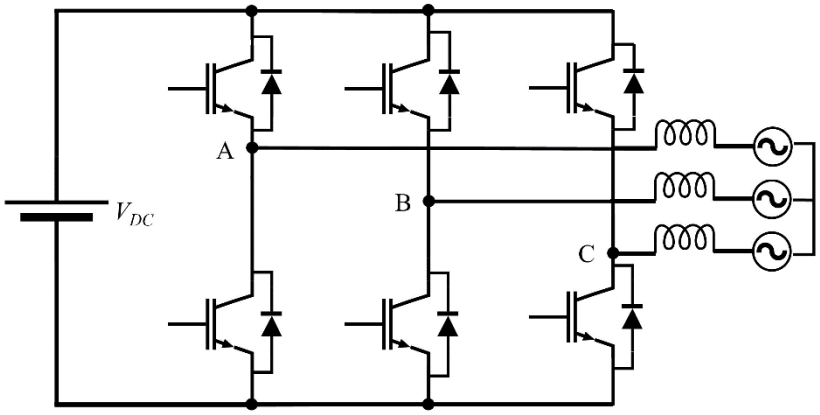

Fig. 1.1 3-Phase 2-level VSC

Due to the lack of number of levels in the output, 2-level VSCs have a high harmonic distortion. Also, due to the limitations on current and voltage handling capability of power electronic switches, the use of 6-switch VSCs in high power applications is limited. To high power ratings different circuit configurations with more switches sharing the current and/or voltage have been developed over the years [4], [5].

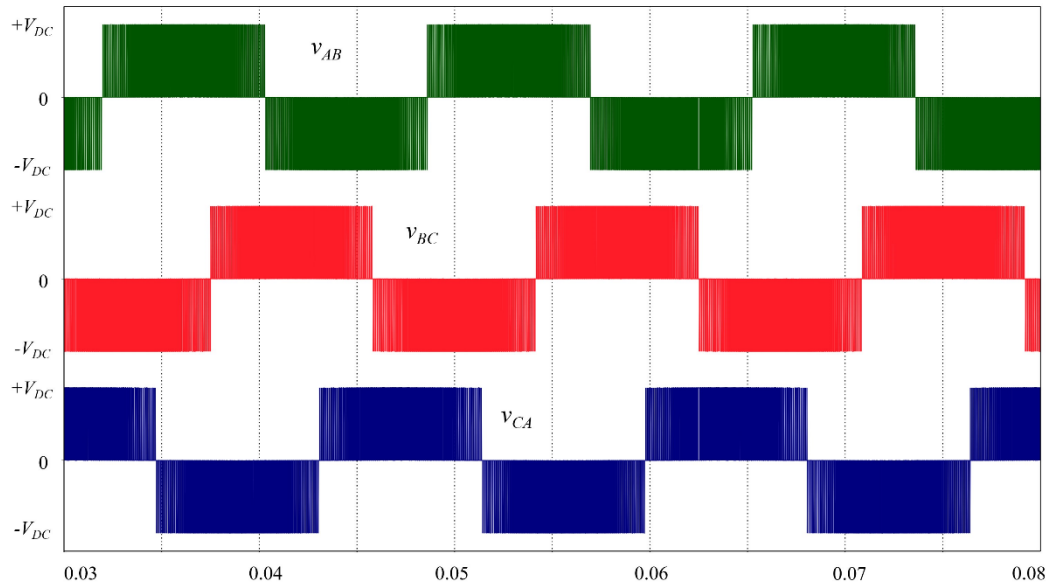

Fig. 1.2 Line-to-line voltage waveform of 3-ph 2-level VSC

1.3 Parallel connection of VSCs

Increased demand for power and limitation on voltage levels in some applications such as EV chargers, points in the direction of dealing with high currents. And still, the current handling capability of power electronic devices is limited. For this reason, connecting converters in parallel so that the current, and hence the power, can be shared between the converters under the restrained voltage, is becoming popular [6], [7], [8].

Parallel connection of converters comes with its own challenges. The outputs of the converters connected together needs to be properly coordinated to avoid any adverse interactions among them and to ensure that the load is shared among the converters in the intended proportions. Circulating currents among the converters is also one of the main concerns when connecting converters parallelly. This has been a widely researched area which progresses with improvements in different aspects such as circuit configurations, PWM techniques, different magnetic configurations etc.

The basic circuit configuration on which the work presented in this thesis based is shown, Fig. 1.3. As the DC side is acting as a voltage source, it is mandatory to have some sort of inductance

between the outputs of the inverter legs. For the clarity of illustrations, only one phase (A) is represented and the same is applicable to other phases as well.

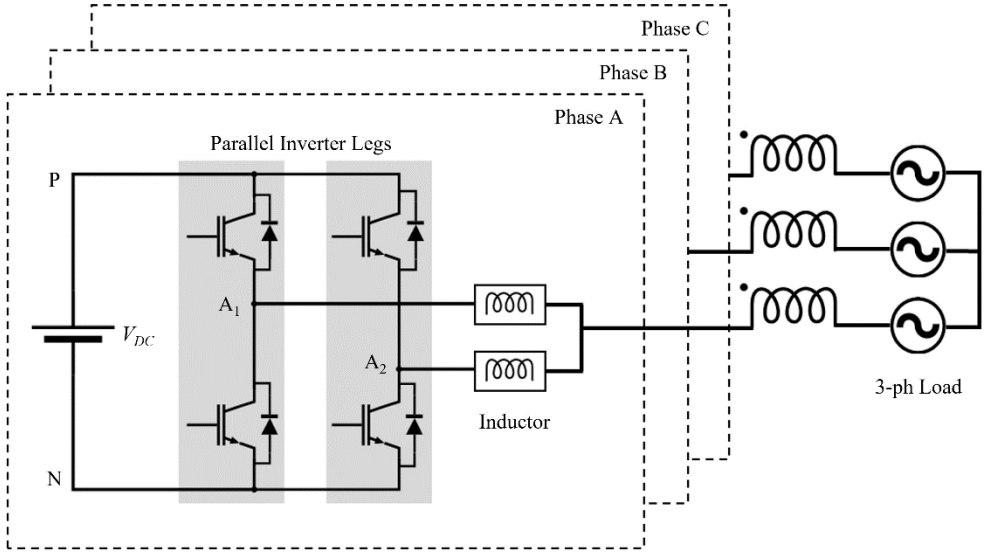

Fig. 1.3 Parallel connection of VSIs - 2 inverter legs per phase

1.4 Circulating Current

Circulating currents flow between the inverter legs of the same phase or among different phases. Either way they don't contribute to the power output of the converter.

The circulating current can have a high frequency (PWM frequency) component, a fundamental frequency component and a dc component. The high frequency circulating current is caused by the PWM switching scheme used and non-ideal operation of power semiconductor switches. The circulating current in fundamental frequency is mainly contributed by different non-idealities and asymmetricities in the passive components in the system.

A. Effects of Circulating Current

Circulating currents add up to the currents flowing through the power electronic switches and the magnetic components demanding their current ratings to be higher; i.e. to be over-designed for a given power rating making the overall power density of the converter small. Higher

currents result in higher conduction losses resulting in higher temperature rises. As the current increases, the flux in the magnetic cores increase too, and can result in core saturation. All these adverse effects without contributing to the output of the converter makes the circulating currents highly undesirable.

B. Minimizing Circulating Current

Minimizing the circulating currents in parallel connected inverters is an extensively researched area [9]. Different control algorithms [10], [11], [12], [13], [14], [15], [16], external circuitry [17], PWM techniques [18], [19], [20], [21], [22], [23], [24], [25] inductor arrangements [26], or a combination of these [27], have been proposed to suppress these circulating currents.

1.5 Coupled Inductor Inverter

The outputs of the parallel legs of the inverters are connected via inductors. Using coupled inverters in place of the conventional inductors proved to be highly effective in suppressing the circulating currents while offering a low inductance to the output current which makes the voltage drop across it low [26], [28], [29], [30], [31].

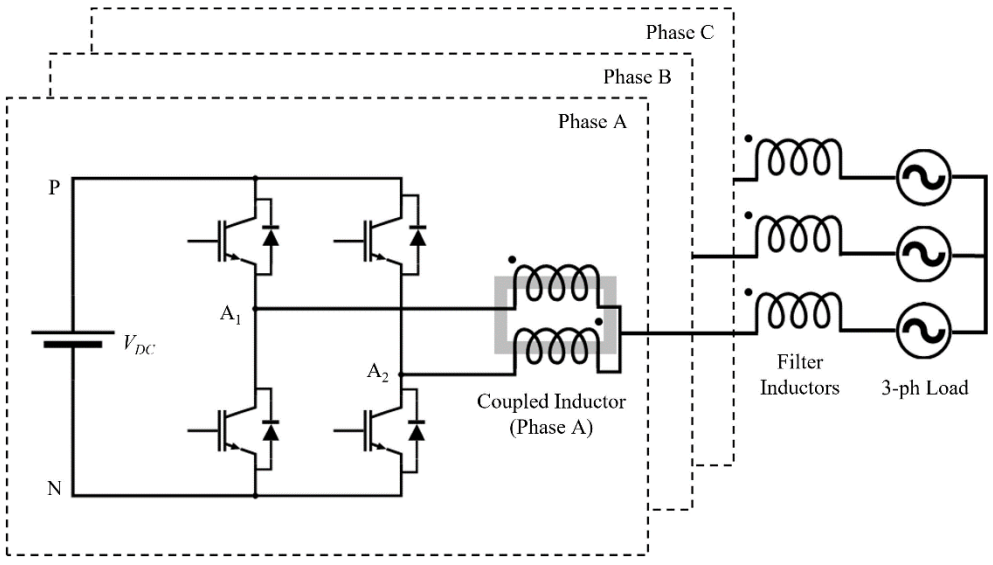

Fig. 1.4 Coupled inductor inverter with 2 parallel legs

The currents flowing in the coupled inductor determine the amount of flux produced in it. The magnetic components need to be designed such that they will not saturate under the intended operation and the temperature rise due to losses is limited within the permissible range.

The phase output current (i_A) is assumed to be contributed equally by the 2 inverter leg output currents i_{A1} and i_{A2}. The current i_{circ} is circulating between the two inverter legs, Fig. 1.5.

Considering the winding arrangement, represented by the dot notation, and the directions of the currents, magnetomotive force (MMF) produced by the components of the load current in the two windings are in the opposing directions and if the current is shared equally between the two inverter legs, that MMF is balanced and produce no flux. Therefore, the flux in the core is primarily resulted by the circulating current, i_{circ}.

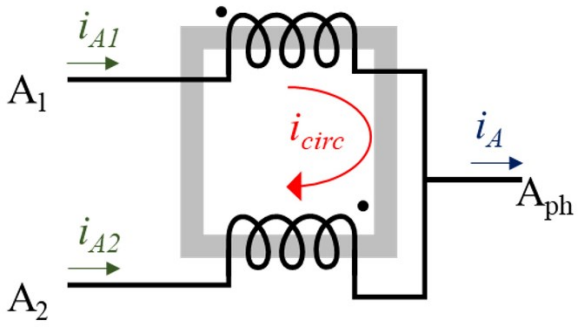

Fig. 1.5 Currents flowing through the coupled inductor

A coupled inductor inverter system is used in the work presented due to its effectiveness in reducing overall circulating currents, but the concept of eliminating jumps in the circulating current is generally applicable to systems with conventional inductors as well.

1.6 Interleaved Switching of Parallel Inverters

Interleaved switching of inverters is switching them at different times by shifting the PWM signals of the parallel inverter legs with respect to each other. As a result, the switching patterns of the paralleled inverter legs are shifted as well and the phase voltage output is the average of the outputs of all the parallel branches which now can have different values.

As the PWM pulses of the parallel inverter legs are shifted relative to one another, and the output is the average of the parallel inverter legs, the PWM output will have a high frequency. Achieving higher PWM frequency relative to the switching frequency reduces the output current ripple and thereby the filter inductor requirement, without impacting the switching losses. Also, interleaved PWM switching generates multi-level voltage output with smaller voltage steps which reduces the common mode voltage and the total harmonic distortion (THD).

For example, a system with 2 parallel inverter legs per phase has 2-level phase and 3-level line-to-line voltage output. With interleaved switching, it can generate 3-level phase and 5-level line-to-line voltages with a PWM frequency twice the switching frequency.

The main drawback of interleaving is the increase in the circulating currents between the parallel legs because of the difference in the inverter leg outputs which becomes more prominent with the offset in pulse positioning [32], [33]. The circulating current caused by the interleaved switching is a high frequency current and can be suppressed to a great extent by the use of coupled inductors. As the advantages of interleaved switching outweighs the disadvantages, it is widely used in parallel connected VSIs.

A. Interleaved PWM Switching Techniques

Interleaved switching can be achieved in different ways depending on the PWM technique used. In carrier-based PWM techniques, it can be achieved by shifting the carriers with respect to one another.

The phases of the carriers for parallel inverter legs can be changed to obtain phase-shifted PWM (PS PWM). Previous work has determined that the system performance is at its best when the carriers of the parallel legs of the same phase are equally apart. Therefore, the phase shift between the carriers will depend on the number of parallel inverter legs per phase.

Phase disposition PWM is obtained by level-shifting the carriers. In this method the level-shifted carriers are scaled-down such that they all fit within the original range of the carrier (i.e. -1 to +1)

Interleaved switching using space vector PWM for parallel VSIs is achieved by predetermined mapping of the switching states of the converters. The resultant PWM pulse patterns would be comparable to those obtained with the carrier-based PWM methods even though the techniques used in generating the pulses are different.

The use of a carrier-based technique deemed suitable to provide non-complex solution to generate interleaved PWM switching signals and phase-shifted PWM technique results in highly predictable circulating current and inductor waveforms with no jumps or dc offsets.

1.7 Carrier Change - Enhanced PS PWM

It is observed that the phase-shifted PWM for parallel inverters achieves interleaved switching and creates multi-level phase and line-to-line voltages. Yet, the line-to-line voltage does not switch exclusively between adjacent levels due to the alignment of pulses in different phases. As a result, line-to-line voltage steps between non-adjacent levels during some sections of the fundamental cycle resulting in increased output voltage THD and output current ripple, left half of Fig. 1.6.

The positioning and the duration of these sections depend on the phase shift between the carriers which is related to the number of parallel inverter legs per phase.

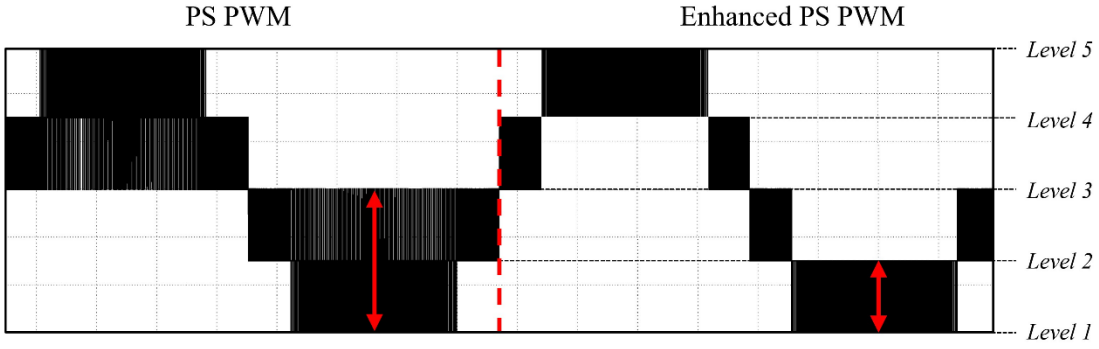

Fig. 1.6 Line-to-line voltage with PS PWM and Enhanced PS PWM

A carrier swapping technique referred to as enhanced phase-shifted PWM [34] which has been implemented in different applications [35], [36], [37], [38], is proved to be an effective method to improve the quality of the output line-to-line voltage.

The enhanced phase-shifted carrier PWM uses two sets of carriers for each phase and alternates between those two sets at specific instances. This re-aligns the PWM pulses of different phases resulting the line-to-line voltage to step exclusively between adjacent levels, right half of Fig. 1.6. As the levels in the line-to-line voltage become more distinct, the quality of the output substantially improved which is reflected in the THD of the.

1.8 Circulating Current Waveform Distortion

The carrier changes have been observed to result in jumps in the circulating current flowing between the parallel inverter legs of the same phase causing high peak values and dc offsets. That causes the magnetic flux in the inductor cores to jump as well. These jumps and dc offsets can saturate the magnetic cores. Also, this can increase the rms of the circulating current increasing current stress on the power electronic switches and increase the overall losses.

It should be noted that these jumps are in addition to the already existing circulating currents and hence, are highly undesirable.

This problem has been the subject of some previous work and different approaches have been tested to mitigate, or to eliminate these jumps and/or dc offsets; each approach with their own merits and demerits.

1.9 Thesis Statement

A PWM technique is presented which eliminates the jumps in the circulating currents while preserving the quality of the output of parallel connected VSIs along with its implementation on a digital signal processor (DSP) environment.

The key contributions of the presented work can be summarized as follows:

- Carrier based PWM technique for parallel connected VSIs that is easily adopted, especially as the number of parallel inverters increases.
- Adopted carrier change technique to improve line-to-line voltage quality
- Carrier transition technique to eliminate circulating current jumps

- Implementation on a DSP which is a trade-off among cost, user-friendliness, reliability, speed, replicability and integrability.

The importance of this thesis over the existing work lies in the fact that the technique presented herein eliminates the jumps in the circulating currents while ensuring high quality output voltage waveforms, and thereby load current waveforms.

Chapter 2

PWM Techniques for Parallel-Connected 2-Level VSIs

Parallel connection of VSIs has been becoming increasingly popular in recent years and a substantial amount of research has been conducted addressing various issues yielding improvements in different aspects such circuit topology, magnetic components, PWM scheme, control techniques etc.

Developments in PWM techniques and improvements related to parallel connected VSIs are discussed in this chapter. The existing techniques to improve the output and their complications are reviewed. Restorative approaches to remedy the complications, and their limitations are analyzed to identify and emphasize the importance of work presented.

2.1 PWM Techniques for VSIs

The 2-level VSI is one of the simplest 3-phase inverter topologies with just six switches and hence, the control techniques are less complex compared to that of other topologies. Different pulse-width modulation techniques have been in use for decades with each technique having its pros and cons [39].

A. Carrier-Based PWM

Carrier-based PWM techniques have been widely used due to the popularity gained during the time of analog systems and continue to be popular with digital controllers as well because of the simplicity in implementation. Also, digital signal processors have dedicated built-in peripheral modules to generate PWM pulses based on reference-carrier comparisons. These peripheral PWM units do not use much computational power from the main core of the DSP under normal operation, allowing other computations to be carried out without any interference or delays. Hence, it's easily integrable with additional closed-loop control algorithms.

i. Carrier-Reference Comparison

The concept of carrier-based PWM is the output is generated based on the comparison between a carrier and a reference, Fig. 2.1. The output PWM pulse have an average proportional to the value of the *reference* over the carrier period. The width of the output pulse is manipulated by changing the *reference* value. Therefore, by updating the reference continuously, the required output is synthesized.

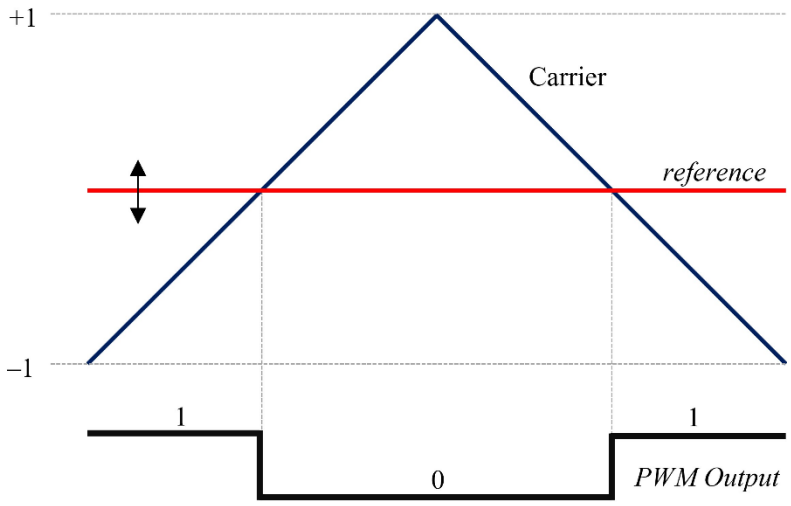

Fig. 2.1 Carrier-based PWM Operation

In practice, the carrier is either triangular or sawtooth in shape. The reference takes different shapes depending on the circuit topology, required output and control algorithm in place.

To generate a sinusoidal AC output, a sinusoidal signal is used as the reference. The output is synthesized with pulses of magnitude varying proportional to the magnitude of the sinusoidal reference. The output contains additional harmonics as it is synthesized using discrete pulses. The harmonic content is reduced by increasing the frequency of the carrier. This involves power electronic switches turning ON and OFF more frequently and it is limited by the switching speed of the devices and switching losses produced.

For 3-phase AC systems sinusoidal signals phase shifted by equal amounts as references for different inverter legs and the output PWM follows the same patter. To utilize the DC voltage more effectively, a 3rd harmonic of the sine wave is superimposed on to the reference of each phase. It allows the use of modulation depths beyond 1 (up to 1.15) and will have no impact since it gets canceled in the line-to-line voltages in a 3-phase system [40].

ii. Carrier-Based PWM for Interleaved Parallel VSIs

When it comes to paralleled VSIs interleaved PWM has proved to produce better performance characterized by the multilevel output and the higher output pulse frequency over non-interleaved counterparts [26], [41], [42], [38], [28], [29].

In carrier-based PWM techniques, interleaving is achieved by shifting the carriers of the parallel inverter legs with respect to each other, thereby offsetting output PWM pulses. Each inverter leg has its own carrier, therefore, a system with *N* parallel inverter legs per phase has *N* number of different carriers per phase too. Depending on how the carriers are shifted, two main types of PWM techniques are defined

Phase-Shifted Carrier PWM

In phase-shifted carrier PWM (PS PWM), the carriers are shifted horizontally, along the time (or the phase angle) axis with respect to each other, Fig. 2.2. That makes pulses to shift by the same delay (phase angle). The phase shift between the carriers of the same phase can be set as required but to produce the best performance with interleaving, the carriers should be equally separated over a full carrier cycle [43]. Hence, the phase shift ($\emptyset_{shift}$) between the carriers of the same output phase can be calculated using (2.1).

$$\emptyset_{shift} = \frac{360°}{N} \tag{2.1}$$

where *N* is the number of parallel inverter legs per phase.

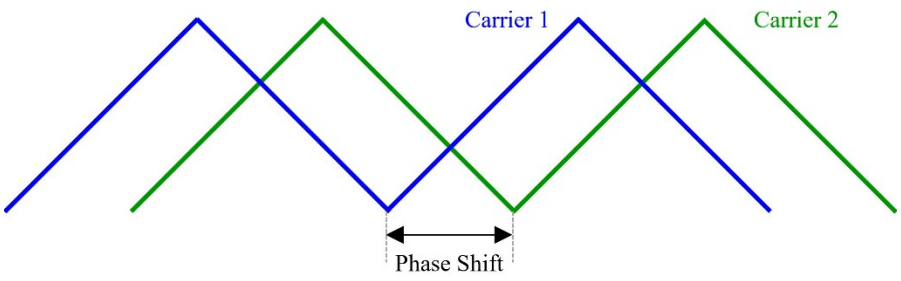

Fig. 2.2 Phase-shifted carriers

Level-Shifted Carrier (Phase-Disposition) PWM

In phase disposition PWM (PD PWM), the carriers are shifted vertically and scaled down to fit in the range of the original carrier, i.e. from -1 to +1, Fig. 2.3. The carriers are stacked on top of each other (commonly referred to as bands) without leaving any gaps and the amplitude (m_c) of the scaled down carriers would depend on the number of different carriers used, and is given by (2.2).

$$m_c = \frac{2}{N} \tag{2.2}$$

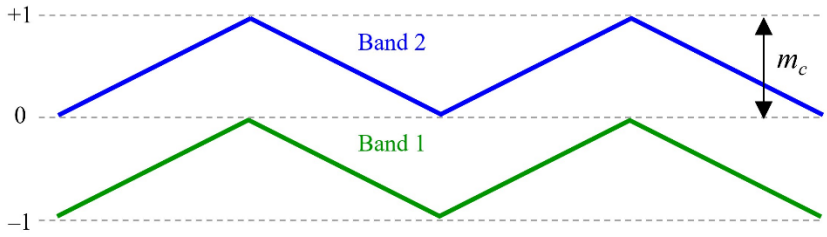

Fig. 2.3 Phase-disposition carriers for $N = 2$

The PD PWM produces better quality output compared to PS PWM is stacked converters [44] but for inverters connected in parallel, the phase disposition carrier technique cannot be implemented directly as it results in a DC flux injection during the transition between the bands and thereby saturates the coupled inductor. Even though several methods are developed to the commutation distribution among the parallel converters balanced, the DC flux injection is not addressed [45], [46].

A PWM technique is developed to balance the flux while addressing even distribution of commutation [45]. The implementation of this technique deviates from the traditional level-shifted carrier approach in PD PWM. A single carrier with replaces the different carriers in a phase, and the reference is manipulated to mimic the switching patterns similar to PD PWM. The frequency of this single carrier (f_{single}) is a multiple of the normal carrier frequency and is given by (2.3).

$$f_{single} = 2 * N * f_c \tag{2.3}$$

The reference manipulation logic depends on the corresponding band number in the conventional PD PWM and hence extending this technique to different number of parallel converters is complicated. Also, manipulating separate references for different inverter legs at a very high frequency demands substantial processing power from the controller which is not desirable.

B. Space Vector PWM

Space vector PWM (SV PWM) operates based on the principle of synthesizing the required voltage vector using different switching combinations. The switching states and the different vectors synthesized using their combinations are listed and it is programmed to select the relevant combination as the reference voltage vector progresses with time.

When inverters are parallelly connected, more switching states are introduced and hence, more switching combinations. To synthesize certain voltage vectors there may be more than one combination and additional criteria is required which consumes processing power of the digital controller [47]. And this complexity worsens as more parallel inverter legs are connected.

The different SV PWM algorithms developed to improve the performance of a system with a certain number of parallel legs cannot be easily adopted by systems with different numbers of parallel legs.

All the PWM strategies have their own merits and demerits and their suitability mainly depend on the type of application and a proper strategy needs to be selected considering the case-specific requirements [44], [48].

2.2 Phase-Shifted PWM

The phase-shifted carrier PWM (PS PWM) is used as the basis for the work presented in this thesis due to its adaptability in systems with different number of parallel inverters connected with the potential to produce high quality output using low processing power.

A 3-phase system with 2 inverter legs per phase is operated using interleaved switching with 180° phase-shifted carriers, Fig. 2.4 (low carrier frequency is used for the clarity of illustration).

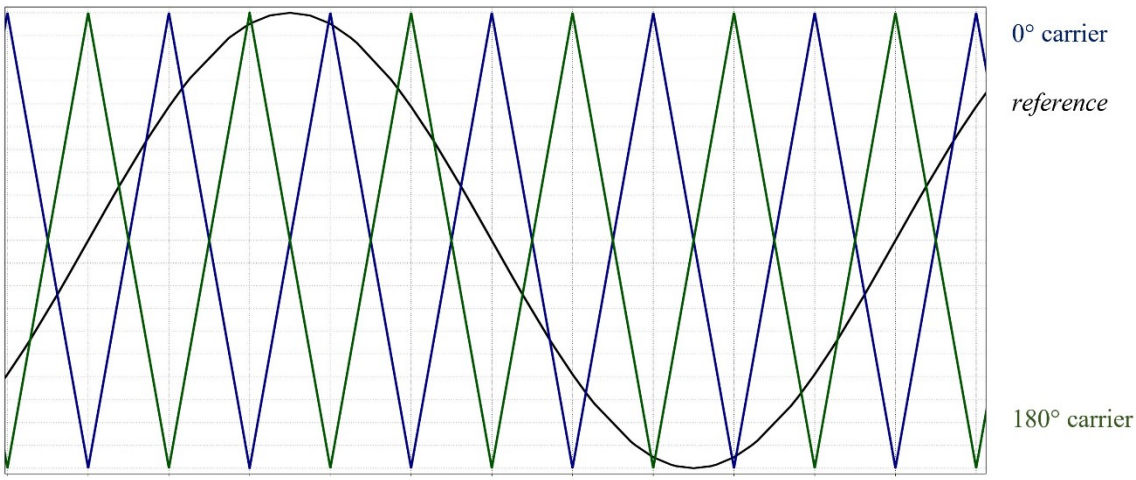

Fig. 2.4 PS carriers for 2-legs per phase (phase A)

The phase voltage output (v_A) is the average of the two inverter leg outputs v_{A1} and v_{A2}. All the measurements are relative to the negative terminal of the dc link. The inverter leg outputs vary between two levels, while the phase output varies between three levels. Also, the phase voltage has a PWM frequency double the carrier frequency, Fig. 2.5.

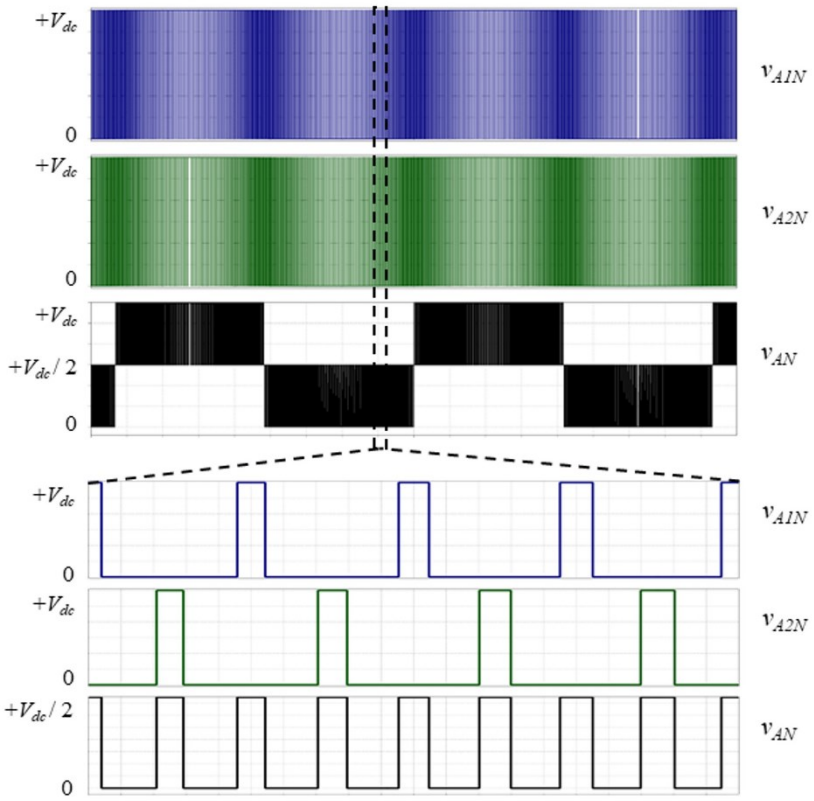

Fig. 2.5 Inverter leg outputs and phase output

Even though a multi-level output is generated, it still carries considerably high harmonic content. These additional harmonics are caused by the pulse positions of different phases, which produce line-to-line voltages that pulsate between non-adjacent levels during some sections of the fundamental cycle, Fig. 2.6.

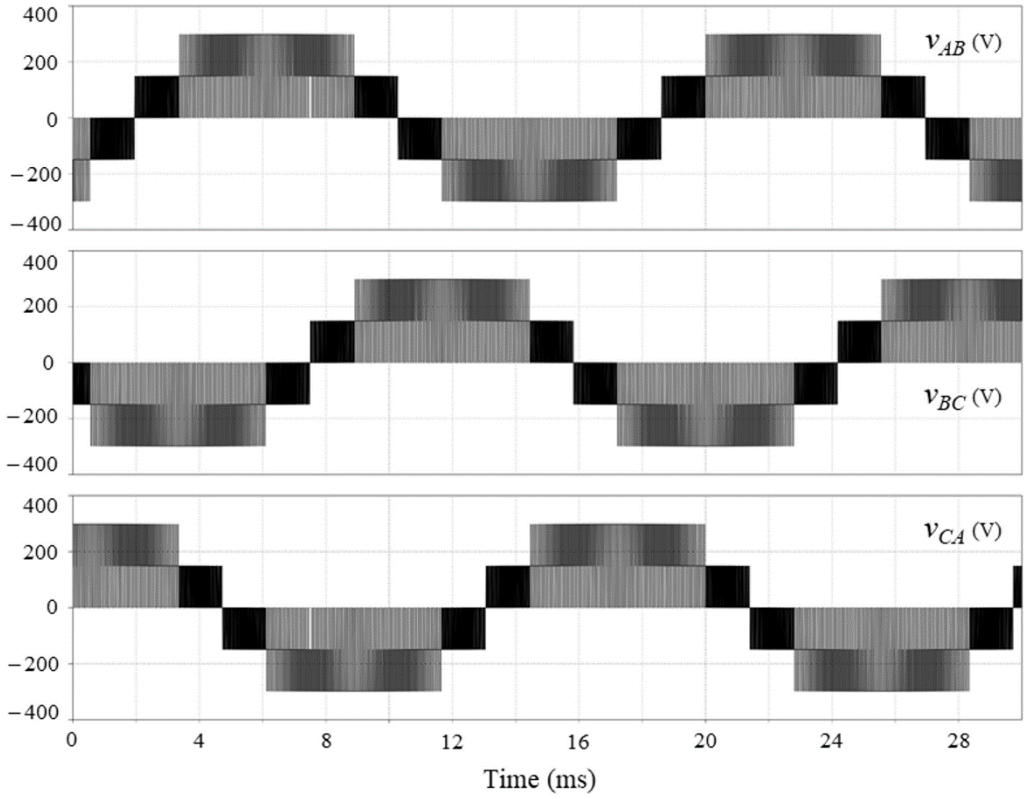

Fig. 2.6 Line-to-line voltages of 2-legs per phase system with PS PWM

A. Enhanced Phase-Shifted PWM

Enhanced phase-shifted carrier PWM introduces a method to improve the quality of the output by addressing the issue with the line-to-line voltages in regular PS PWM [34]. In enhanced PS PWM technique, each inverter leg alternates between two carriers at predetermined positions of the reference. The two carriers are phase shifted by an angle which depends on the total number of parallel inverter legs per phase. Switching between the two carriers adjusts the positioning of output pulses such that they are aligned with the pulses from other phases to produce line-to-line voltage that pulsate only between adjacent levels.

For a system with *N* inverter legs connected in parallel per phase, *N* equally separated carriers are used in PS PWM. Enhanced PS PWM introduces another set of *N* number of carriers, also equally spaced but with having different phase compared to the first set. The carriers within a set are phase shifted by an angle such that the carriers are spread across one carrier period equally which is given by (2.1). The phase shift between the two sets of carriers is selected such that the new set of carriers are placed between the original set, and is given by (2.4).

$$\theta_{set1-set2} = \frac{360°}{2N} \tag{2.4}$$

The carrier phase shifts for the most common number of parallel inverter legs are summarized in Table 2-1.

Table 2-1 Carrier Phase Shifts for Enhanced PS PWM

N	**Carrier Set 1**	**Carrier Set 2**
2	0°, 180°	90°, 270°
3	0°, 120°, 240°	60°, 180°, 300°
4	0°, 90°, 180°, 270°	45°, 135°, 225°, 315°
n	$0°, \frac{360°}{n}, \dots, \frac{(\mathrm{n}-1)*360°}{n}$	$0° + \frac{360°}{2n}, \dots, \frac{(2\mathrm{n}-1)*360°}{2n}$

The improvement in the output line voltages is verified using simulation and experimental results [34].

The main issue with the enhanced phase-shifted PWM technique is the jumps in the circulating currents that occur at the instants where carriers are switched. This causes the flux in the magnetic cores connecting the parallel inverter legs to jump and to offset from its usual average value. As these carrier changes occur continuously at least twice (for 2 inverter legs per phase) in a fundamental cycle remedial action is required for this enhanced PS PWM technique to be implemented in a viable manner.

2.3 Restorative Approaches for Jumps in Circulating Currents

Previous research had already identified the issue of circulating current jumps and presented some mitigatory techniques. Even though those techniques focus on addressing the main concern, i.e. the jumps in the flux in the inductors, they lack a holistic approach in terms of quality of output voltage and current.

A couple of carrier transition techniques for enhanced PS PWM has been presented in [35]. One of the techniques inject a pulse to the reference at the point of carrier change. This compensates for any jump of flux forced by the carrier transition. The simulation and experimental results verify the effectiveness of the approach. The second method, manipulates the carrier, within one half-cycle to prevent the flux jump.

Another PWM scheme is presented in [41] eliminates the carrier changes altogether and the reference is modified to produce high quality line-to-line voltage outputs. This introduces rapid changes in the reference signal where a different carrier would have been used.

All the aforementioned techniques have successfully suppressed the inductor flux jumps from occurring. But all these changes forced on the reference signal is reflected in the phase output voltages and thereby affecting the quality of the load current. This contradicts the use of enhanced PS PWM to improve the quality of the output. All these techniques lack a holistic approach to address the jumps in circulating current and flux, while maintaining the quality of the output.

Therefore, developing a feasible method to eliminate the flux jumps while maintaining the quality of the output voltage and current is an integral necessity.

2.4 Summary

PWM techniques for VSIs are discussed briefly before moving into the parallel VSIs and into the interleaving of VSIs. Phase-shifted PWM, phase-disposition PWM, and space vector PWM are explored as possible contenders for control of interleaved parallel VSIs, and pros and cons of each technique are identified. PS-PWM is explored further and shortcomings in the quality of line voltage, and techniques that have been developed to overcome those shortcomings are

analyzed. How implementing one remedial technique bring about additional complexities is studied in order to develop a holistic solution.

Chapter 3

High Frequency Carrier Transition Technique

Phase-shifted carrier PWM for parallel VSIs require alternating between two carriers to produce better quality voltage output. This carrier change results in jumps in the circulating current and the magnetic flux in the inductor core. In this chapter, the reasons for the circulating current jumps are analyzed using fundamental principles. A theoretical carrier transition technique to eliminate the current jumps while maintaining the output unaltered is presented followed by simulation results.

3.1 Carrier Transition

The two sets of carriers for a system with 2 parallel inverter legs per phase are phase shifted by 90°. That is, 0° carrier switches to a 90° carrier and 180° carrier switches to a 270° carrier. These occur at the minimum or the maximum of the carrier and an immediate transition will cause the value of the carrier to jump. The region from this jump to the point where the new carrier reaches the value of the old carrier at the point of carrier change is referred to as the "Transition Region".

Consider a case where the carriers are changed at the minimum of 0°-carrier. The 0°-carrier switches to 90° and the 180° carrier which is at the maximum, switches to 270°-carrier. The duration from this instantaneous carrier change until it reaches the minimum in the 90°-carrier, t_{t1} in Fig. 3.1 (a), is the "transition region" for this transition. This region represents the phase shift between the carriers, which is 90° in this case. Hence, it is equal to one-fourth of the normal carrier period.

For the reverse carrier change, 90° to 0° and 270° to 180°, transition initiating at the maximum of the 90°-carrier is considered and the transition region is denoted by t_{t2}, Fig. 3.1 (b). It corresponds to 270° shift, which is three-fourths of the normal carrier period.

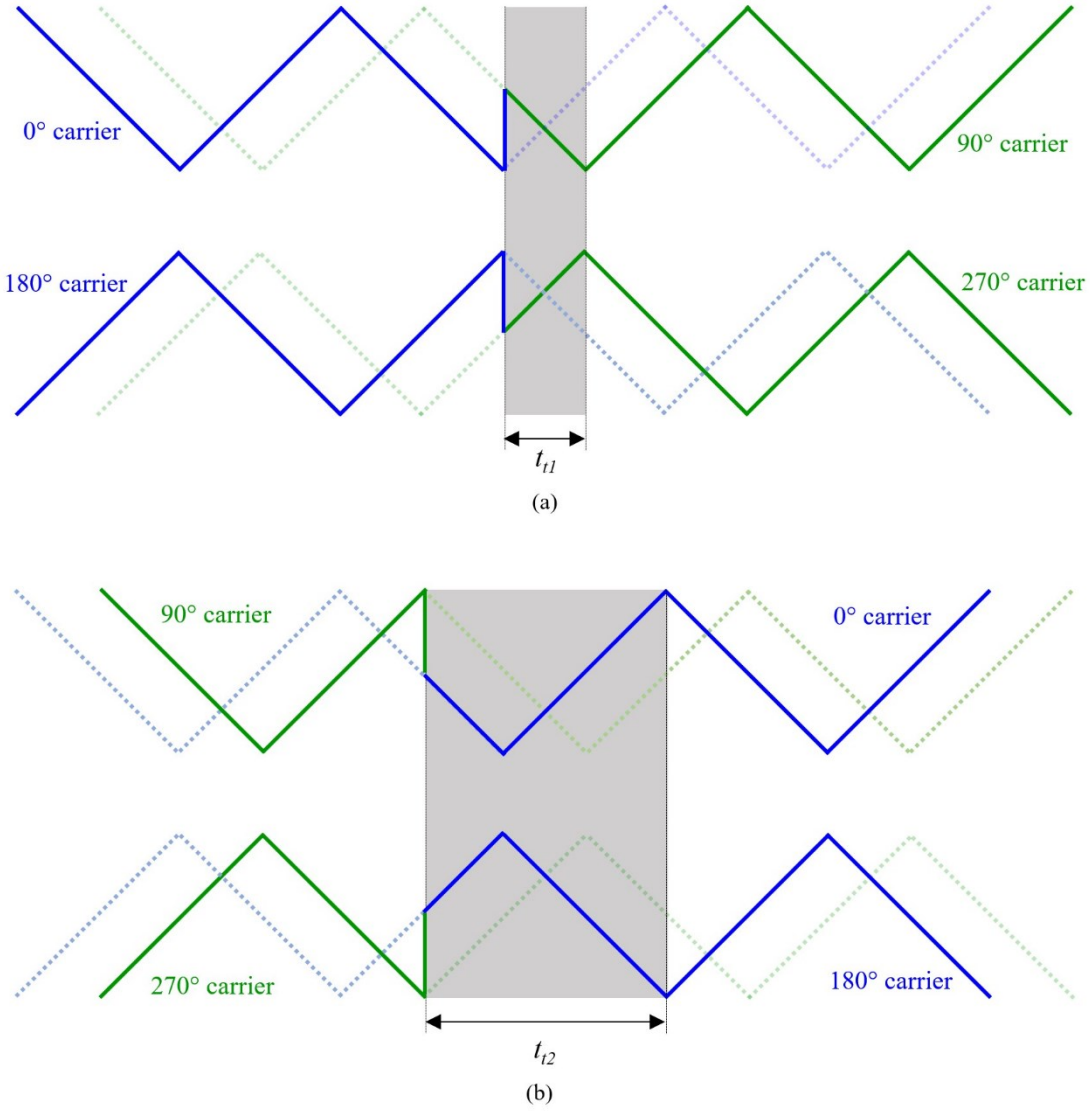

Fig. 3.1 Carrier transitions and transition regions (a) 0° to 90° transition (b) 90° to 0° transition

3.2 Circulating Current / Flux Jumps

It has been observed that immediate carrier change causes the flux in the inductor between the parallel inverter legs of the same phase to show abrupt changes and to end up with a dc offset.

The carriers, PWM outputs, the voltages applied across the inductors and the resultant flux patterns around the carrier change are studied to narrow down the exact cause for the behavior of the flux.

When using coupled inductors, the primary flux in the core is produced by the circulating current flowing between the legs of the same phase and not the output current.

The voltage driving the circulating current, and thereby generating the flux in the core, is the instantaneous difference between the inverter leg outputs.

Consider the inverter legs of Phase A, A_1 and A_2. Outputs at A_1, v_{A1}, and at A_2, v_{A2}, are determined by the PWM outputs with 0° and 180° carriers respectively. The differential voltage is calculated as ($v_{A1} - v_{A2}$).

Using basic magnetic theory for the coupled inductor, expressions for the flux in the core and the circulating current can be derived using (3.1) and (3.2), and the circulating current (flux) pattern can be sketched against the time as in Fig. 3.2. Constant reference is assumed for the clarity of illustration.

$$v = n\frac{d\varphi}{dt} \Longrightarrow \varphi = \frac{1}{n}\int v\,dt \tag{3.1}$$

And,

$$v = L\frac{di}{dt} \Longrightarrow i_{circ} = \frac{1}{L}\int v\,dt \tag{3.2}$$

where i_{circ} represents circulating current, φ represents the flux, v, the voltage and n, the number of turns in the inductor.

It is evident from the equations that the circulating current and the flux waveforms have similar shapes.

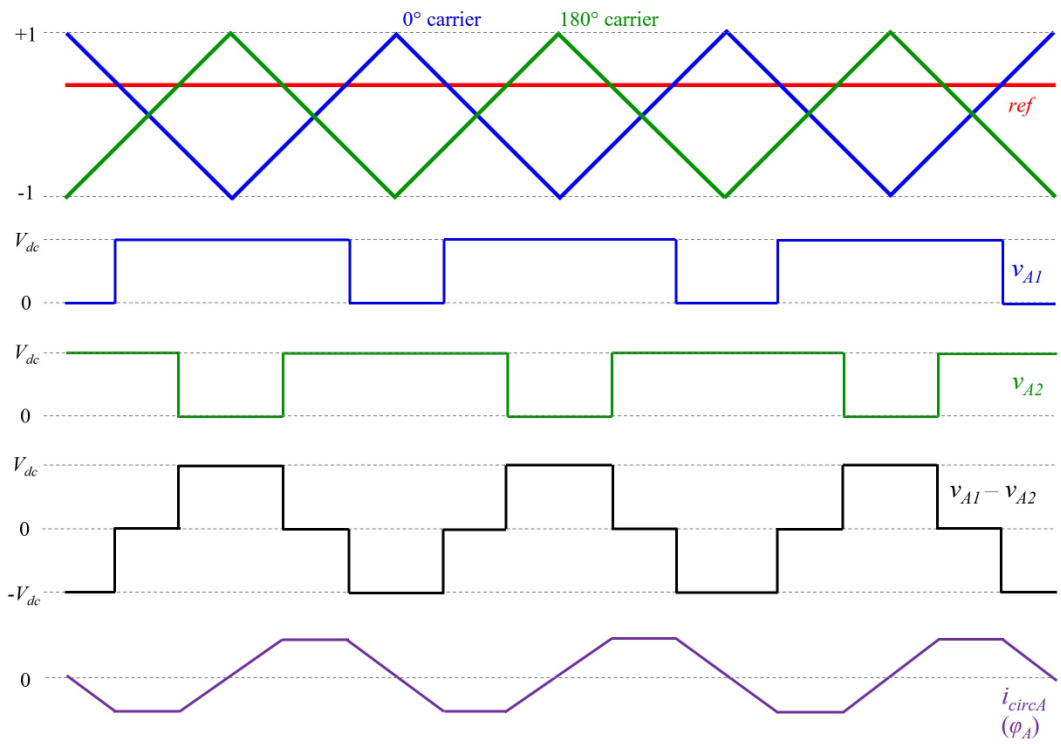

Fig. 3.2 Inverter leg outputs and derived coupled inductor flux in a phase

The output voltage and hence, the differential voltage waveforms are periodic with a frequency equal to the carrier frequency. The resultant circulating current (and flux) pattern also shows similar periodic behavior. In addition to the variations shown, the pulse widths of the voltage waveforms change with sinusoidal reference, and the rising and falling time durations of the flux pattern will change accordingly. One notable instance is at the zero crossing of the reference, where the carrier changes will also take place. The inverter leg outputs are directly opposite, and the flux pattern will no longer have a plateau region, Fig. 3.3.

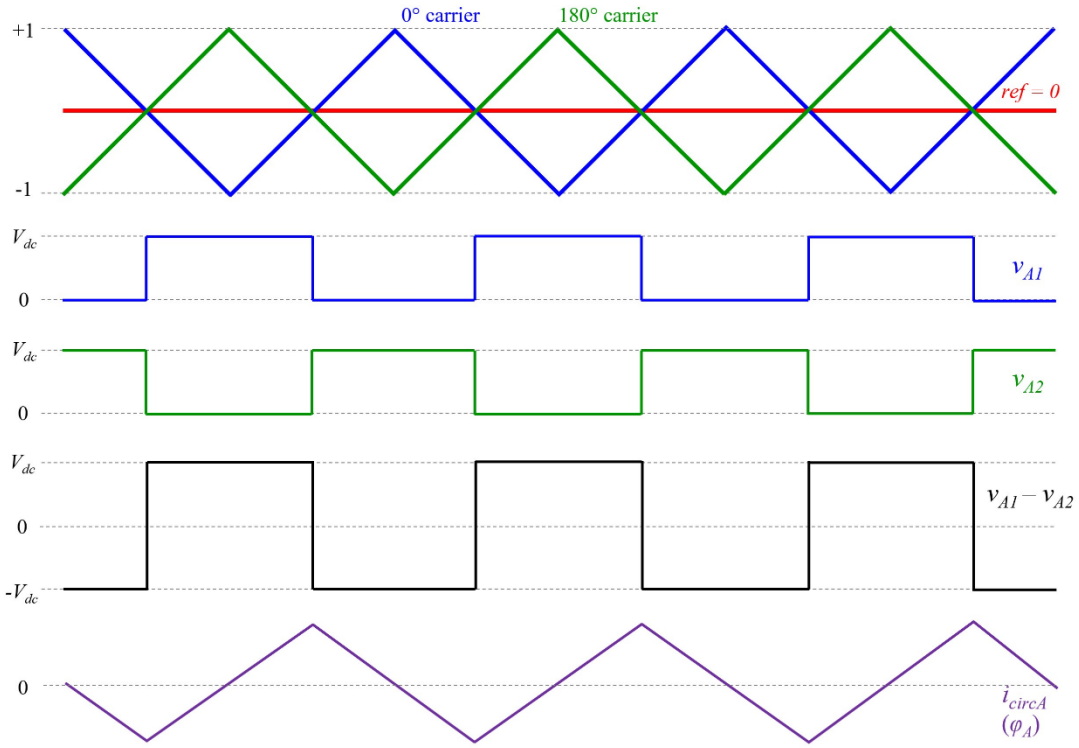

Fig. 3.3 Inverter leg outputs and derived coupled inductor flux at reference zero crossing

It is evident that the circulating current and the flux reaches their maxima around the zero crossing of the reference. It is also verified using simulation and experimental results in the subsequent sections.

The enhanced phase-shifted PWM scheme requires the carriers to switch right at the reference zero crossing. The PWM output of the two inverter legs at the instant of switching carriers is derived by comparing the reference and the new carrier and is visualized in Fig. 3.4. Accordingly, the voltage outputs of the inverter legs and the resultant flux patterns in the inductor core can also be derived, Fig. 3.4.

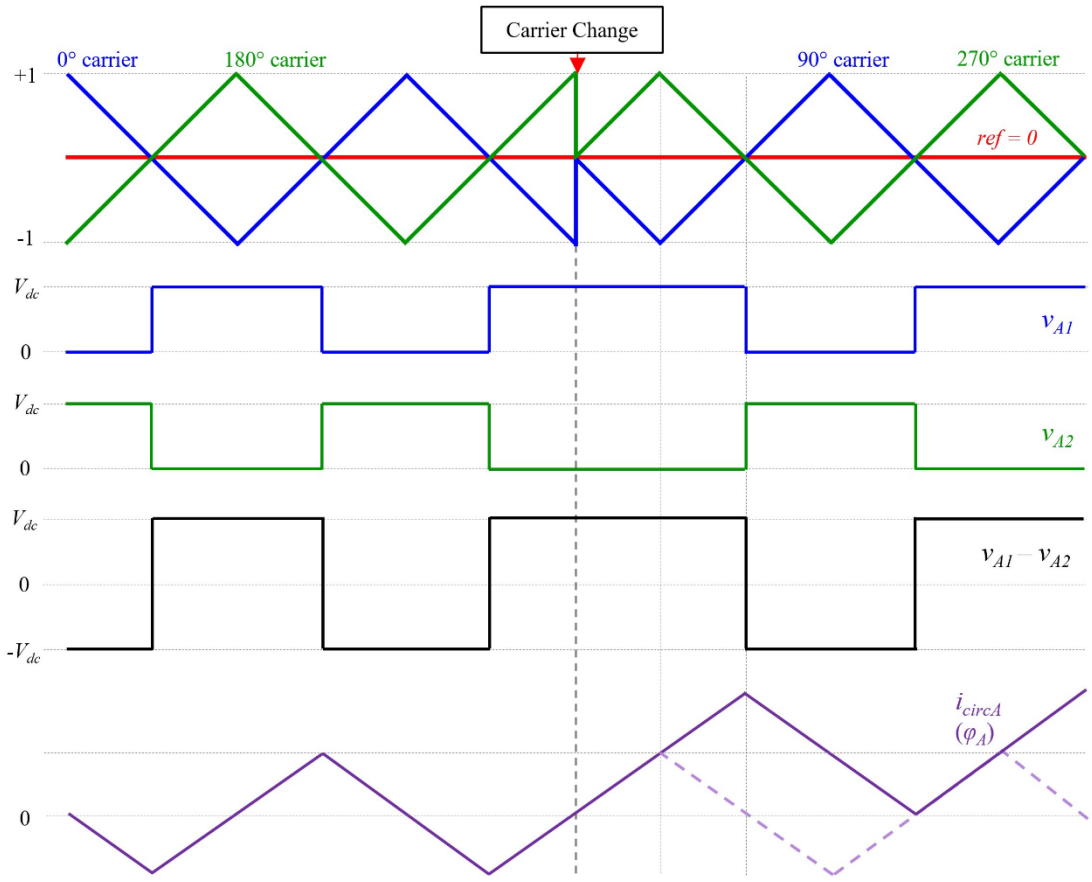

Fig. 3.4 Inverter leg outputs and derived coupled inductor flux at instantaneous carrier change

When the carrier phase angle changes, the flux pattern continues with the new carrier without being adjusted to the new phase shift. The output voltage pulses are observed to stay at one level for longer duration than the usual. This causes the flux to increase in magnitude beyond their usual maximum or minimum. This is observed as a jump in the flux pattern at the instants of carrier change. Also, this will cause an offset in the flux pattern since it won't return to the previous maximum (or minimum), because of the jump occurred at transition.

3.3 High Frequency Carrier Cycle Concept

The reason for the flux jump is caused by the instantaneous phase change forced on the flux. The high frequency (HF) carrier cycle concept aims to give flux the required phase shift in a gradual manner rather than forcing it suddenly.

High frequency carrier starts where the carrier usually switches to the other. And it completes one full cycle before returning to the normal frequency. During that HF cycle, it generates PWM pulses at the same high frequency, which results in a similar voltage output at the inverter legs. The differential voltage follows the same pattern generating a flux pattern that completes one period at the high frequency. Completing a full cycle ensures that the flux pattern returns to the starting point. I.e. volt-seconds are balanced and no offset in flux is resulted. The carrier frequency returns to its normal value immediately after completing the high frequency cycle, so will the PWM outputs, voltage outputs and the flux patterns.

The high frequency cycle introduces a phase delay to the carrier but without pausing the PWM action and thereby having the control of output voltage throughout. The length of this phase delay is determined by the period of the high frequency carrier.

In the presented technique, the high frequency is selected such that the phase delay is the same as the duration of the "Transition Region". That way the carrier will automatically shift to the required phase. Also, the flux pattern gradually adjusts to the new carrier without any abrupt changes.

2-Inverter Legs per Phase

The carriers in a two inverter legs per phase system switch between 90°-shifted carriers. I.e. 0°-carrier switches to 90° and 180°-carrier switches to 270°. The reverse transition is a phase shift of 270°; 90°-carrier going back to 0° (360°) and 270°-carrier going back to 180° (540°).

90° phase shift is ¼ of the carrier cycle, and 270° is ¾ of the cycle. Hence, the high frequencies required to fit in these phase shifts can be calculated using (3.3) and (3.4).

$$f_{HF90} = \frac{360}{90} * f_c = 4 * f_c \tag{3.3}$$

And,

$$f_{HF270} = \frac{360}{270} * f_c = \frac{4}{3} * f_c \tag{3.4}$$

3.4 Flux and Output Voltage with HF Carrier Transition

The PWM outputs, inverter leg voltage outputs and the circulating current (flux) patterns in the cores during the 0°-90° (180°-270°) carrier transition using high frequency (four times the normal carrier frequency) carriers can be derived and visually represented as in Fig. 3.5.

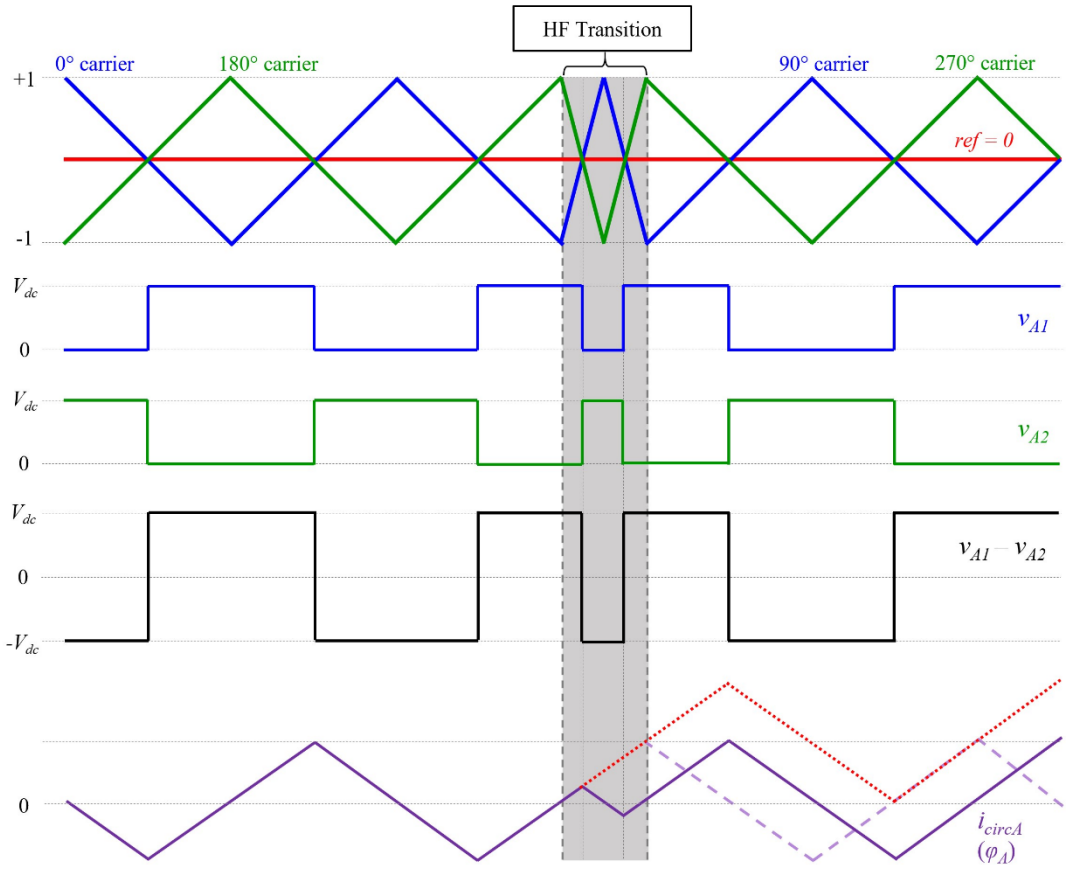

Fig. 3.5 Inverter leg outputs and derived circulating during 0°-90° carrier transition

The 90°-0° (270°-180°) transition uses a high frequency carrier with four-thirds the normal carrier frequency. The differential voltage and the circulating current (flux) patterns can be derived in a similar manner, Fig. 3.6.

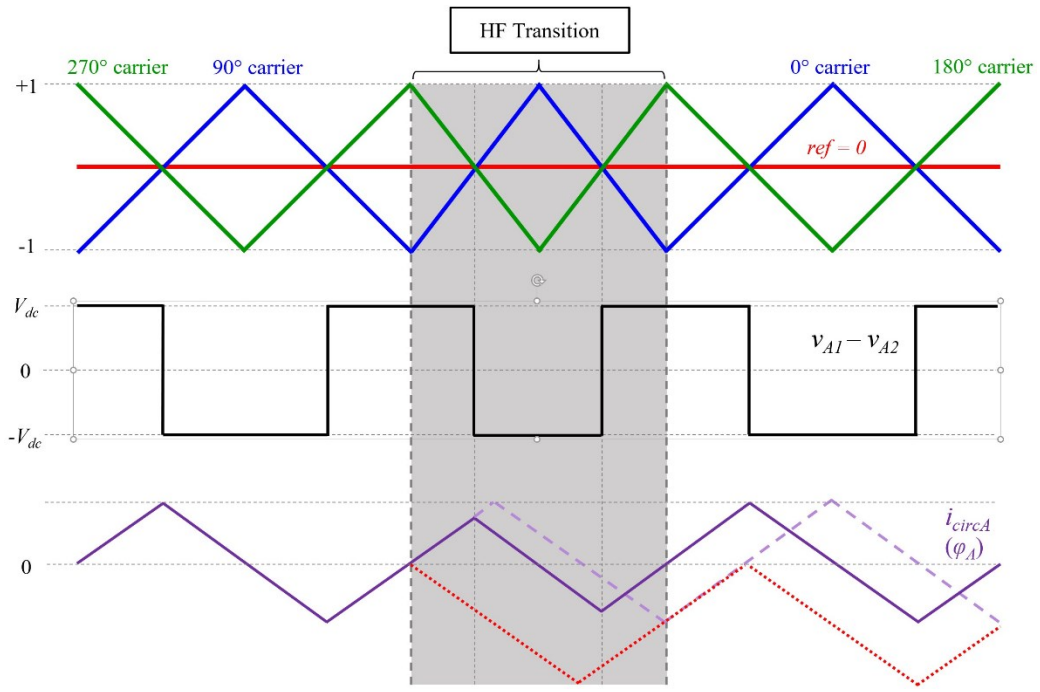

Fig. 3.6 Differential voltage and circulating current during 90-0 carrier transition

A. Impact of HF Carrier Cycle on the Circulating Current (Flux) Pattern

With the introduction of the high frequency carrier cycle, PWM pulses are generated at the same high frequency. Hence, during that period the switching frequency is temporarily increased which limits the duration that the flux increases in one direction, preventing the flux from reaching abruptly high values. Theoretically derived circulating current (flux) patterns for the 3 cases, without carrier change, with instantaneous carrier change and carrier change via HF carrier cycle are compared in Fig. 3.5 and Fig. 3.6, represented by dashed-purple, dashed-red and solid-purple lines respectively. The circulating current (flux) is maintained within the same range as in the case without carrier change, by using HF carrier transition.

B. Average Output Voltage

Another important outcome of this high frequency carrier cycle is that the output phase voltage is maintained at its intended average value. This is a major improvement over the existing methods of eliminating the flux jumps in the core. It ensures that the quality of the output voltage waveform is not compromised, while the advantages of carrier change are used.

By maintaining the average output voltage unscathed, the load current will remain unaffected by the carrier change and the high frequency carrier cycle used to eliminate the flux jumps.

3.5 High Frequency Carrier Transition Algorithm

An algorithm for the implementation of enhanced phase-shifted PWM combined with high frequency carrier transition is developed. The algorithm is generalized for an arbitrary number (N) of parallel inverter legs per phase. The important calculations include determining the instances of carrier transitions and determining the frequency of the transitional carriers:

A. Determination of Carrier Transition Instances

The carrier transition instances are the places where high frequency carrier cycles are introduced. These instances are dictated by the enhanced phase-shifted PWM scheme [34] and are dependent on the number of the parallel inverter legs (N). The transitions are triggered based on the value of the reference signal and the number of transitions during a fundamental cycle (n_{tr}) is also dependent on the number of parallel legs (3.5).

$$n_{tr} = 2(N-1) \tag{3.5}$$

The reference value at the x^{th} transition (ref_{trx}) is given by (3.6), where 'x' is the transition number as counted from the lowest reference value. $x \in [1, (N-1)]$

$$ref_{trx} = -1 + x * \frac{2}{N} \tag{3.6}$$

B. Determination of Frequency of the Transitional Carrier

Frequencies of the high-frequency carriers depend on the carrier frequency (f_c) and the phase difference between the two sets of the carriers ($\emptyset_{shift}$), given by (3.7), which in turn depends on the number of parallel inverter legs (N). Each system has two different high frequencies; to switch from one carrier to the other and to switch back to the original carrier.

$$\emptyset_{shift} = \frac{2\pi}{2N}\, rad = \left(\frac{360}{2N}\right)^{\circ} \tag{3.7}$$

The two high-frequencies, f_{HF1} and f_{HF2}, correspond to the transitions from 1st carrier set to the 2nd and from 2nd to the 1st respectively, and are given by (3.8) and (3.9).

$$f_{HF1} = \frac{2\pi}{\emptyset_{shift}} * f_c \tag{3.8}$$

where $\emptyset_{shift}$ is used in radians.

$$f_{HF2} = \left(\frac{2\pi}{2\pi - \emptyset_{shift}}\right) * f_c \tag{3.9}$$

The summary for commonly used number of parallel legs are tabulated, Table 3-1, and it is extendable to any value of *N* using (3.5) – (3.9).

Table 3-1 Summary of Transitions for Typical Number of Parallel Inverter Legs

N	n_{tr}	$[ref_{tr}]$	$\emptyset_{shift}$	f_{HF1}	f_{HF2}
2	2	[0]	90°	$4 * f_c$	$\frac{4}{3} * f_c$
3	4	[-1/3, +1/3]	60°	$6 * f_c$	$\frac{6}{5} * f_c$
4	6	[-1/2, 0, +1/2]	45°	$8 * f_c$	$\frac{8}{7} * f_c$
N	2(*N*-2)	[-1+2/*N*, -1+4/*N*,…]	$\left(\frac{360}{2N}\right)^{\circ}$	$2N * f_c$	$\frac{2N}{2N-1} * f_c$

3.6 Simulation Results

The high frequency carrier transition technique is simulated with a dc link voltage of 300 V to be in par with the experimental setup. The phase voltages, line voltages and load currents are captured, Fig. 3.7. The line-to-line voltages only pulsate within adjacent levels in each section and the load currents do not have any glitches during the transitions.

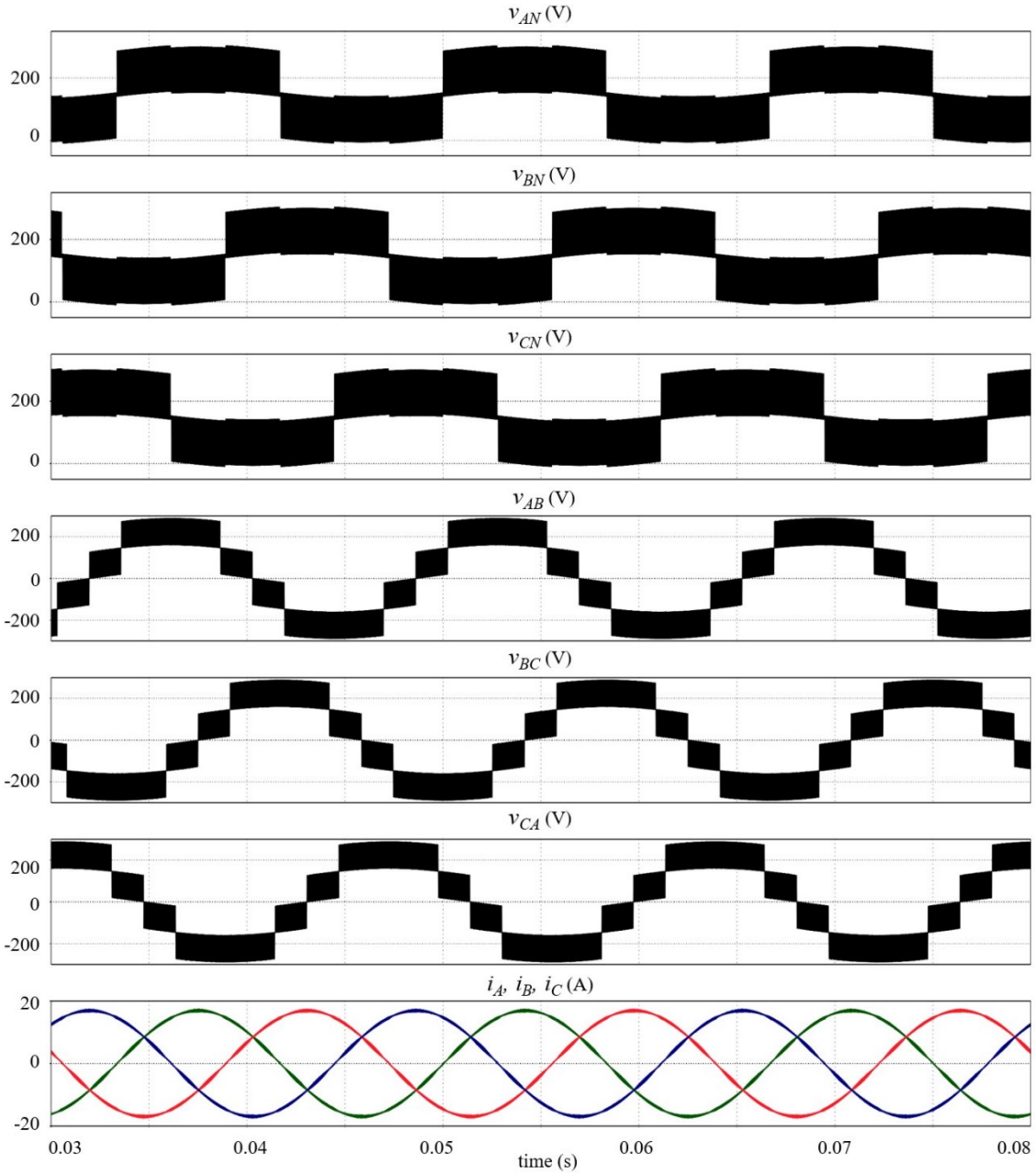

Fig. 3.7 Simulated output waveforms with HF carrier transition

The circulating currents for the three phases with the HF transition are compared against the enhanced PS PWM scheme with instantaneous carrier changes Fig. 3.8. The maximum difference between the peak circulating currents of the two cases (considering maximum difference from all the phases) was calculated to be 106%. This circulating current directly relates to the flux in the core. Therefore, in order to accommodate this jump, the core needs to be twice the size as for the case with HF transition. Also, dc offsets during certain sections can be observed as anticipated.

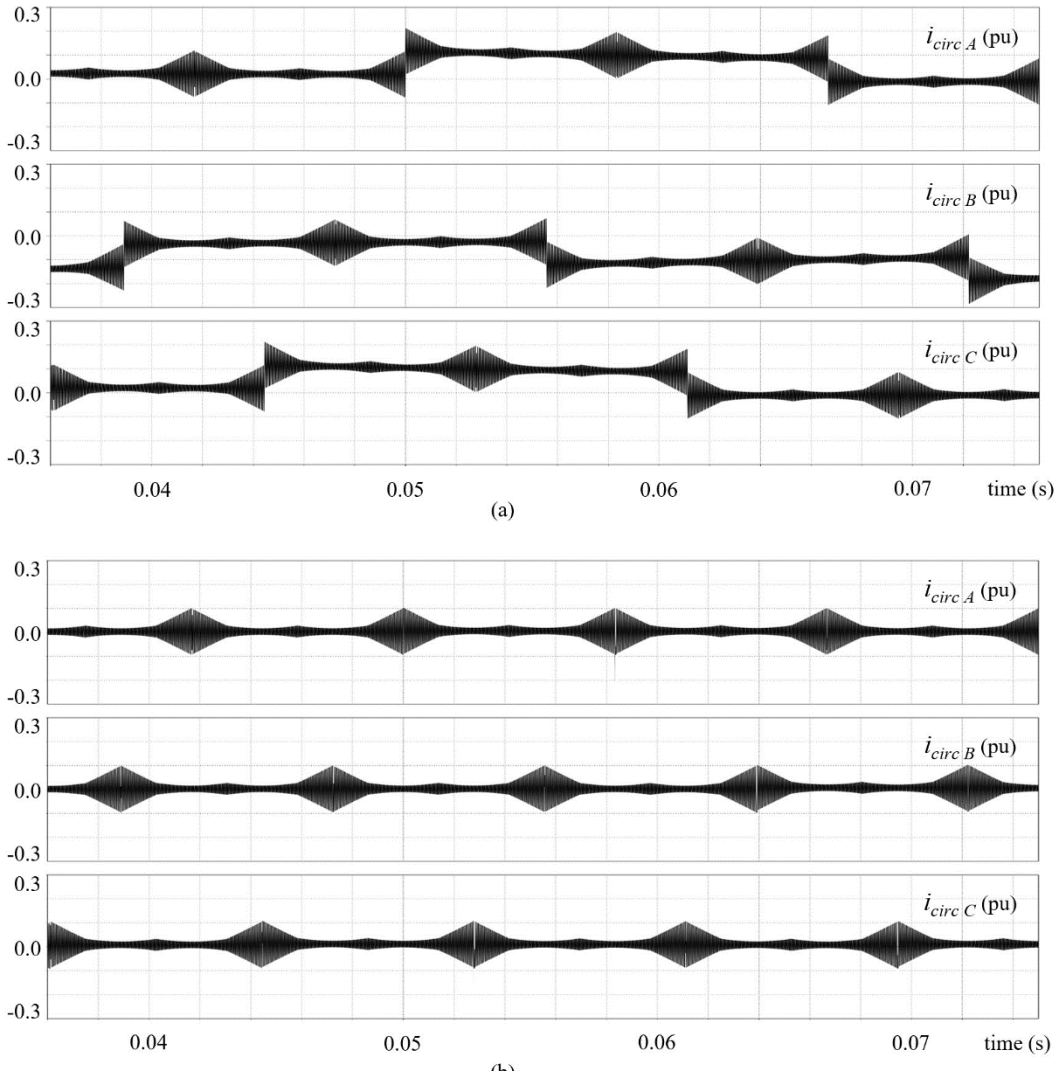

Fig. 3.8 Simulated circulating currents (a) instantaneous carrier change (b) carrier change with HF carrier transition

3.7 Summary

The carrier changes and the consequent jumps in the circulating current and flux are discussed in detail. The high-frequency carrier concept is introduced for two inverter legs per phase system. The voltage outputs and derived flux patterns are demonstrated to explain the action of the HF carrier cycle. The HF carrier cycle concept is then generalized for arbitrary number of parallel inverter legs. At the end of the chapter, simulation results are presented, which supports the previous discussion.

Chapter 4

Implementation on DSP

The Digital Signal Processors (DSPs) are widely used in commercial applications as well as in academic research due to low cost, reliability, versatility and excellent performance. It is preferred over hardware platforms specially designed for research, testing and prototyping due to the cost effectiveness and adaptability to commercial applications.

There are several ways to program a DSP out of which coding in C language is one of the most common methods. Software packages like MATLAB, PLECS have dedicated libraries to program DSPs using software-generated C code based on simulation models. Even though using simulator-generated C code seems to be more user friendly, availability of functions in those library blocks are limited and hence, some control techniques might not be able to be implemented and the resources available in the DSP might not be used to the fullest.

4.1 DSP TMS320F28379D

TMS320F28379D, technically, a Digital Signal Controller (DSC), which is a Digital Signal Processor (DSP) integrated with other peripherals such as analog-to-digital converters, digital-to-analog converters, pulse width modulators, communication interfaces etc. As both the terms DSP and DSC have been used interchangeably in literature and due to the popularity of the term, TMS320F28379D is henceforth referred to as the DSP.

TMS320F28379D, a 32-bit fixed-point processor with an integrated floating-point unit, which belongs to the C2000 family of DSPs from Texas Instruments is a dual-core processor in the TMS320 series. The C2000 family is well-known for cost-effectiveness and performance in control system applications including motor controllers and power supply controllers [49].

Even though F28379D is a dual core DSP only one core is used for the work presented herein, while the other core is reserved for extending the system for closed-loop control which is future work.

As the work presented focuses on a PWM technique, the pulse-width modulator peripheral in the DSP is thoroughly studied and used extensively, in addition to the timer interrupt.

Timer Interrupt

The DSP TMS320F28379D has 3 timers out of which 2 are available for user applications. An "interrupt" is, as the name suggests, an event which interrupts the running program in the processor. The processor will return to the original program after executing the service routine dedicated to the interrupt (known as the Interrupt Service Routine - ISR). The ISR is user programmable and can be used to perform different tasks. Interrupts can be generated internally or externally, in this particular case by one of the Timer units. The Timer will be triggering the interrupt event periodically, and hence the ISR for the Timer interrupt will be executed periodically. In addition to the Timer interrupt, PWM interrupts are used frequently in the work presented.

4.2 Pulse Width Modulator in TMS320F28379D

One of the main reasons for choosing the DSP TMS320F28379D is the availability of functions for PWM control. To improve system performance the PWM functions are separated for the main processing unit and assigned as a peripheral module. Operation of the PWM and the specific functions used for the implementation of the presented carrier transition technique are discussed.

A. Peripheral PWM Module

The processor F28379D has 12 PWM modules as peripherals which are equipped with functionalities required to implement carrier-based PWM directly. As peripheral units, these modules, once configured at initialization stage of the program, generate PWM output pulses without consuming processing power of the main controller. Registers of the PWM modules can be accessed from either cores of the processor, and also, the interrupts thrown by PWM

modules can be programmed to execute on either of the cores. During initialization, permission to access a particular peripheral should be assigned to one of the cores. By default, the core number1 has the permission to access the PWM peripherals and is used as it is in the program.

Each PWM module (of the 12) has its own carrier and two output signals, PWM_A and PWM_B, which can be programmed to operate together or independent of each other. In the work presented, these 2 outputs are used as gate signals for the upper and lower switches of an inverter leg. Also, each PWM module has its own set of configuration registers and registers for storing the reference signals which gives freedom for the modules to operate independently, if required. Refer *Appendix A* for the list of PWM registers used.

B. Carrier Synthesis

To use the PWM modules for the carrier-based techniques, specific registers should be configured in order to generate the required carrier. Ideally, the carrier would be an analog signal, but within the DSP which is a digital platform, it is composed of numerous discrete steps in a counter (Time-Base counter) which can count in either direction, up or down. The DSP has the flexibility to configure different aspects of the carrier during initialization and to update them as required during the progression of the program execution.

- Counter Mode: Counter mode defines the shape of the carrier; whether it is a triangular or sawtooth carrier. The PWM counter can be configured to count up and/or count down. Count-up, Fig. 4.1(a), and count-down, Fig. 4.1(b), correspond to sawtooth carriers, where the counter counts up to (or count down from) a predefined value and then resets at the end of the period. Count up-down, Fig. 4.1(c), corresponds to triangular carrier where the counter increments up to a predefined value and then counts down until it reaches 0. The predefined value, which the counter counts up to or count down from is termed as the Time-Base Counter Period and can be accessed at the register *TBPRD* under PWM registers.

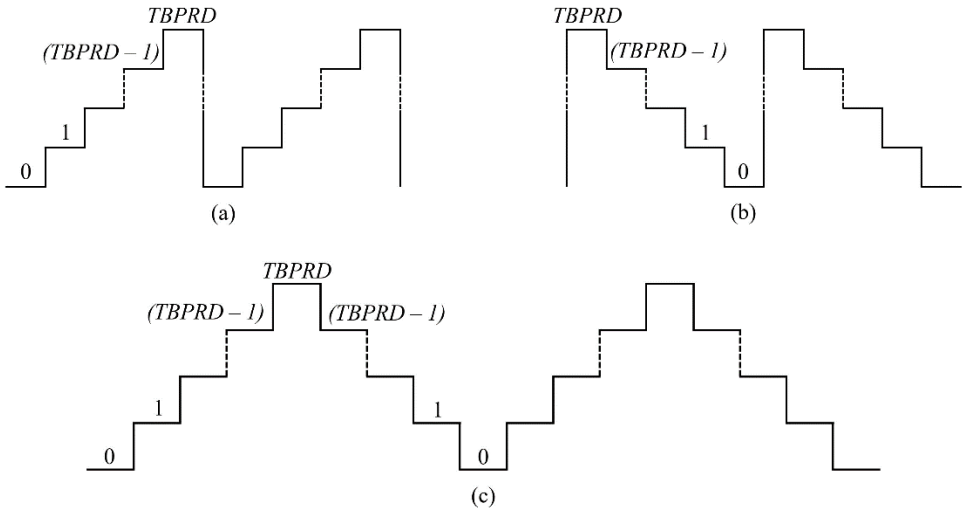

Fig. 4.1 Counter modes and carrier types (a) Up-count - Sawtooth, (b) Down-count - Sawtooth, (c) Up-Down count - Triangular

- Frequency: The frequency of the carrier depends on how fast the PWM counter increments (or decrements) and the set Time-Base Counter Period (*TBPRD*) value. The speed of counting can be changed by scaling the system frequency as required. The *TBPRD* value can be set at initialization and updated as required during the course of execution of the program.

- Carrier Resolution: As the carrier is synthesized using discrete steps in the counter, the total number of steps will determine the resolution of the carrier. Higher the number of steps, better the resolution; i.e. the carrier will be closer to an analog signal. Since the number of steps is also related to the frequency of the carrier, the freedom to increase the resolution is bound by the system frequency and the expected carrier frequency, Fig. 4.2.

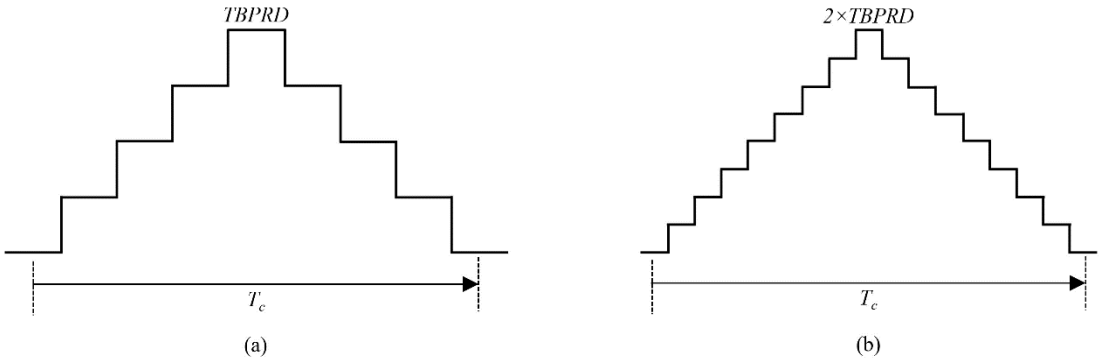

Fig. 4.2 Carrier of same frequency with (a) low resolution and low TBPRD, (b) high resolution and high TBPRD

C. Reference Signal and Counter Compare Submodule

Carrier-based PWM operates based on the comparison of the reference and the carrier. The main function of the "Counter Compare" submodule is to carry out this comparison and take appropriate action. The comparison is an equality check rather than a comparator, and hence it captures the instances where the references intersect the carrier. The action taken can be setting the PWM output or throwing an interrupt depending on how it's programmed.

Each PWM module has 4 signals (*CMPA*, *CMPB*, *CMPC* & *CMPD*) that are compared with the counter, out of which only 2 can set the PWM output pulses. All 4 are capable of generating other events. As the time-base counter increments or decrements, these compare signals are compared with the counter value in each step.

D. Action Qualifier Submodule

Action qualifier defines what changes in the PWM output occur at different events. The action can be setting the output high or low, toggle the output or to proceed without any change.

i. Generating PWM Output Signals

For conventional PWM, the output is set high when the reference is greater than the carrier and it is set low when the reference is smaller, Fig. 4.3. Note that the carrier, which is the time-base counter (*TBCTR*), is now varying between 0 and *TBPRD*. The events triggering these switching actions would be the intersection of the carrier and the reference.

- Set HIGH - Intersection on down-count

- Set LOW - Intersection on the up-count

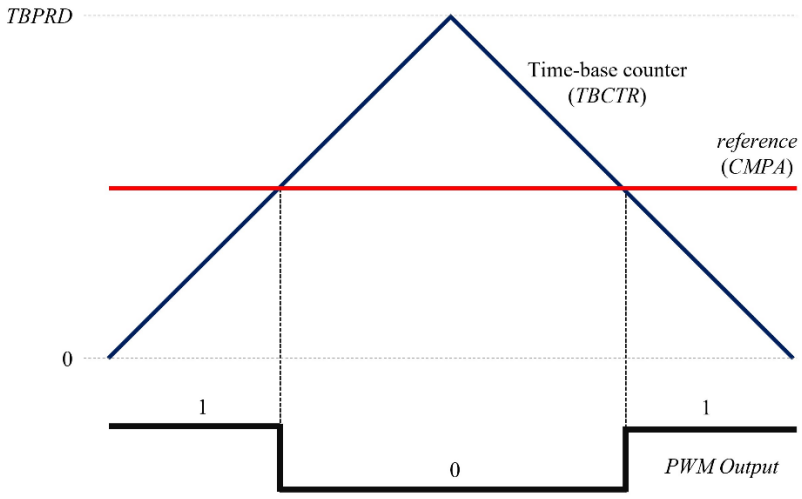

Fig. 4.3 Conventional PWM output generation using DSP

ii. Events and Actions

An action can be forced on the PWM output once an event is triggered by one of the following instances [50]:

- *Counter* = *CMPA* on up-count or down-count
- *Counter* = *CMPB* on up-count or down-count
- *Counter* = 0
- *Counter* = *TBPRD*
- External Event T_1 on up-count or down-count
- External Event T_2 on up-count of down-count
- Software-forced Event

DSP has the freedom to select PWM output switching actions based on the aforementioned events. The possible switching actions are:

- Set HIGH
- Set LOW
- TOGGLE
- No Action

E. PWM Interrupts

PWM modules have the capability to throw interrupts to one of the cores of the processor and the corresponding interrupt service routines (ISRs) will be executed. The interrupts can be triggered by the same events that switch the PWM outputs. The reference signal updates are done within PWM interrupts at *Counter* = 0 and *Counter* = *TBPRD*, which corresponds to minimum and maximum of the carrier.

At the every PWM interrupt two main functions are carried out:

- Update the compare signals
- Check the conditions for the reference zero-crossing and if a zero crossing is detected, run the appropriate high-frequency carrier transition algorithm

F. Dead-band Submodule

A dead-band is used between upper and lower switches of an inverter leg in order to prevent a shoot through with both switches being on at the same time. The PWM module has the option to generate complementary signals at its two outputs using the "Dead-band" submodule. This will reduce the number of comparator operations needed to carry out since only one reference is used and the second PWM output is auto-generated.

The rising edge and falling edge delays can be programmed separately or one of the predefined cases (active high complementary, active low complementary, active high or active low) can be selected. Considering the conditions to avoid a shoot-through, active-high complementary is selected as the dead-band mode where none of the switches are ON at the same time, but both will be OFF for a small duration, Fig. 4.4.

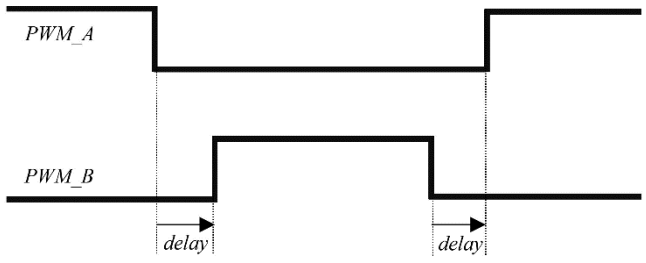

Fig. 4.4 Active High Complementary PWM

4.3 Sinusoidal PWM and Carrier Changing

The implementation of phase-shifted PWM for a parallel VSI system with carrier changing has two main components; generating 3-phase reference signals, and changing between carriers at the appropriate values of the reference. The resources in the DSP can be managed to obtain a high-resolution reference while utilizing the computational power in an optimal manner.

A. Reference Update and Carrier Change Instances

The reference sine waveform is synthesized within the DSP and sampled at regular intervals to be update the PWM peripherals. At the same time, the reference value should be checked to identify the exact instances to initiate the carrier changes. These tasks are assigned to different peripheral interrupt service routines. Each phase has its own reference signal and own carrier change instances.

i. Sine Wave Generation

C Function *__sinpuf32(θ)* is used to generate the sine function, where θ is in per unit and the conversion from radians to p.u. is given by (4.1) in which α is in radians.

$$\theta = \frac{\alpha}{2\pi} \tag{4.1}$$

Resolution of the sine wave, which depends on the step size of incrementing θ, is selected such that it is higher than double the carrier frequency. It ensures that the sampling at every half carrier cycle yields an updated sine value. Increasing the resolution too high doesn't yield any improvement on the system performance and it just adds to the burden on the processor.

Timer interrupt is used to generate the sine wave with precise fundamental frequency in steps of 10 μs.

ii. Reference Update - Compare Signal Update

The generated sine wave needs to be scaled appropriately for the required modulation depth and offset to match the actual carrier, which is a counter which goes from zero to Time Base Period (*TBPRD*) instead of -1 to +1. In the first step the sine wave is scaled to the range [0,1] from [-1,1], (4.3). And then it is scaled to the size of the PWM carrier (4.4).

$$ref_a = m_a Sin(\theta) \tag{4.2}$$

where ref_a phase A reference, m_a modulation depth

$$ref_a{}^{*} = \frac{1}{2}(m_a Sin(\theta) + 1) \tag{4.3}$$

where $ref_a{}^{*}$ is the reference scaled to the range [0,1]

$$ref_a{}^{**} = \frac{1}{2}(m_a Sin(\theta) + 1) \tag{4.4}$$

where $ref_a{}^{**}$ is the reference scaled to the size of the actual carrier.

The compare signal, CMPA of each PWM channel is updated with this scaled reference, $ref_a{}^{**}$, every half carrier cycle; i.e. at the minimum and the maximum of the carrier. This has been common practice when implementing carrier based PWM in DSP as more frequent reference updates (in between carrier maximum and minimum) can lead to abnormal PWM output.

iii. PWM Scheme Carrier Change Instances

The enhanced phase-shifted PWM requires alternating between two carriers in each inverter leg of each phase; i.e. in all the PWM channels in the DSP.

The instance of the changing the carrier is based on the reference for the particular phase and this value depends on the number of parallel inverter legs per phase.

2 Inverter Legs per Phase

The PWM scheme for a system with two parallel inverter legs per phase requires the carrier to change phase at every zero crossing of the reference signal.

Basically, there are two main carrier changes; 0° to 90° transition occurring when reference goes from negative to positive and 90° to 0° transition occurring when the reference goes from positive to negative, Table 4-1. For the zero-crossing detection, the reference value at adjacent carrier half cycle points (minimum and maximum) are compared.

Table 4-1 Detecting Zero Crossing and Corresponding Carrier Transitions

$[ref_a]_t$	$[ref_a]_{t+1}$	Zero Crossing	Transition
> 0	< 0	Yes	90° to 0°
> 0	> 0	No	-
< 0	> 0	Yes	0° to 90°
< 0	< 0	No	-

B. Changing the Carrier

Once the reference reaches the point where the carriers need to be switched, the relevant phase of the new carrier is loaded and will come into effect when the next synchronization signal is sent out from the master carrier.

The phase of the carrier should be in the form of PWM counter value. Hence, the phase angle needs to be converted to be compatible with the counter values. Also, counter direction should be specified as different carrier phases have the same counter value and the difference is only in the direction.

2 Inverter Legs per Phase

The carriers will shift from 0° and 180° to 90° and 270°, and vice versa. Initially the phase loading of the carriers would be 0° and 180°, that is equivalent to 0 and *TBPRD* in the counter. The counter direction is not significant here, as they are at the minimum or the maximum there is only one direction to count from. At the transition, 90° and 270° need to be loaded, where both these correspond to the same *TBPRD*/2 counter value. And the counter direction will specify them apart, Fig. 4.5.

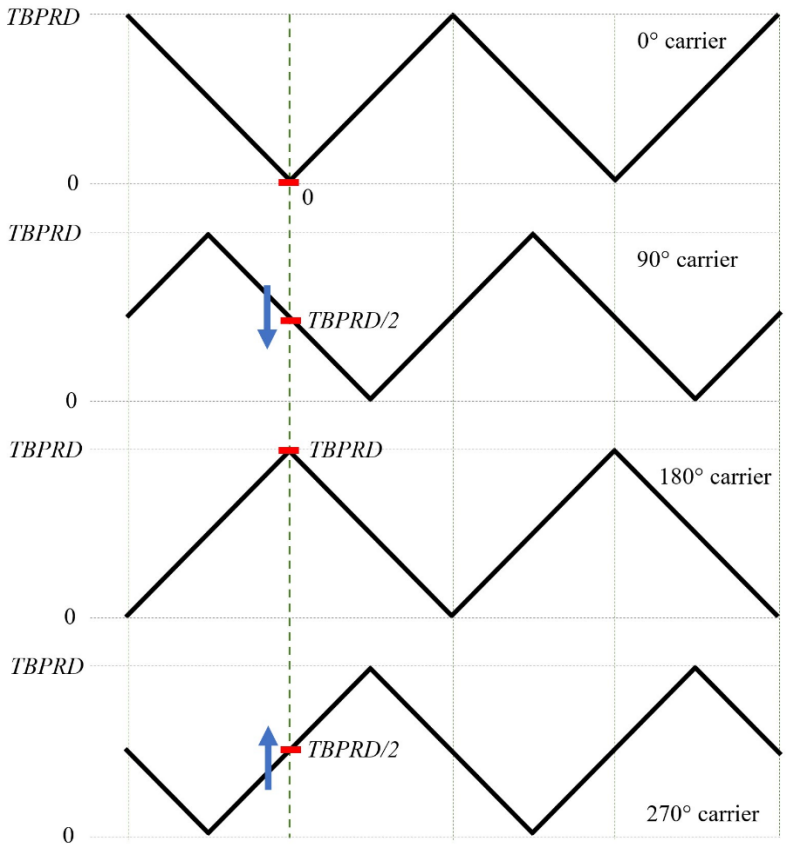

Fig. 4.5 Triangular carrier phase shifts in DSP implementation

C. PWM Output with Instantaneous Carrier Change

The PWM output during the carrier change slightly differs from the theoretical explanation because of the delay from identifying the carrier change instance to the synchronization with the new phase shift. Still, the switch from one carrier to another takes place instantaneously and hence the imbalances in the circulating currents (and flux patterns) occur as explained. It is verified with the experimental setup as well. The PWM pulse at the zero-crossing of the reference, where the carriers are switched, is captured and the wider than usual PWM pulse is observed, Fig. 4.6.

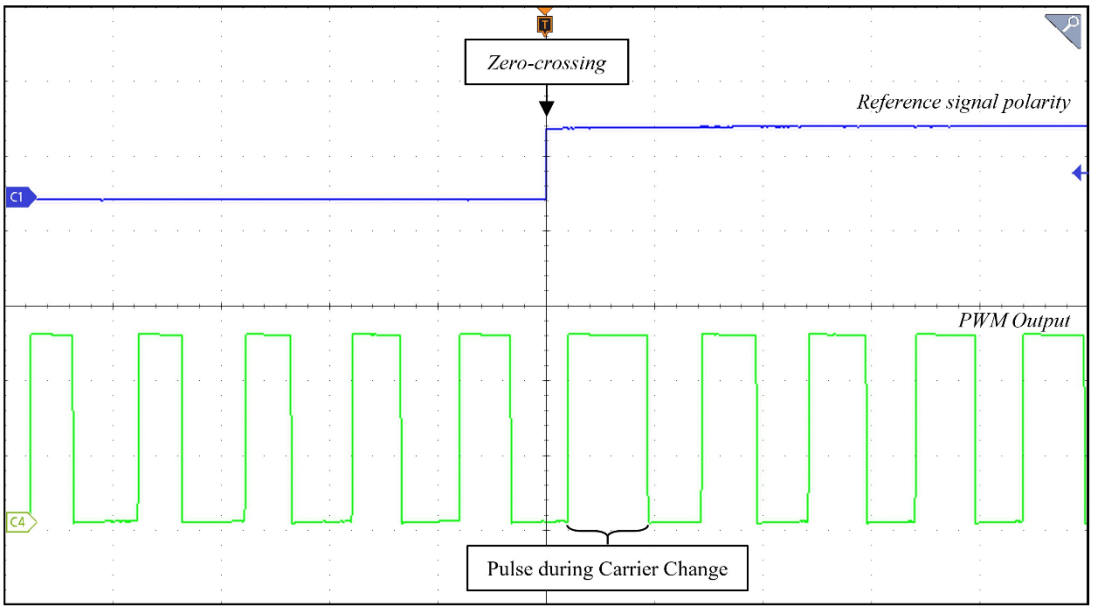

Fig. 4.6 Widened pulse at carrier change in Enhanced PS PWM (instantaneous carrier change)

4.4 High-Frequency Carrier Transition Implementation

The carrier changes in the Enhanced PS PWM technique are implemented by transitioning through a high frequency carrier cycle, and hence creating the expected carrier phase shifts.

A. High Frequency Carrier in DSP

The frequency of the carrier is mainly determined by the Time Base Counter Period (*TBPRD*), the number which the counter will count up to and/or count down from. The new value for the Time Base Counter Period, $TBPRD^*$, required to generate a carrier with a frequency different from the original frequency is calculated using the ratio of the two frequencies, f_c, the normal carrier frequency and f_{HF}, the high frequency (4.5).

$$TBPRD^* = \frac{f_c}{f_{HF}} \times TBPRD \tag{4.5}$$

The *TBPRD* register in the DSP is shadowed to ensure the stability of the value updates. That is, the new value is written to a shadow register first and then to the actual register in the next cycle. Hence, it is required to determine the carrier change instances in the previous cycle and

update the new *TBPRD* value. Also, to return to the original frequency, the *TBPRD* value needs to be reset, which is also going through the shadow register.

The reference signals for the PWM modules are updated every half-cycle of the carrier; therefore, the *TBPRD* update can take place either at the top or the bottom of the carrier.

2 Inverter Legs per Phase

The 2 main transitions in a 2-legs per phase system are 0°-carrier to 90°-carrier and 90°carrier to 0°-carrier. At the same time, the second leg goes through 180°-carrier to 270°-carrier and 270°-carrier to 180°-carrier transitions. Both the transitions involve moving to a lagging carrier and therefore, the phase shifts are 90° and 270° rather than 90° and -90°. The corresponding high frequencies would be $4f_c$ and $(4/3)f_c$ and the new *TBPRD* values would be one-fourth and three-fourths of the original value yielding proportionate carrier periods.

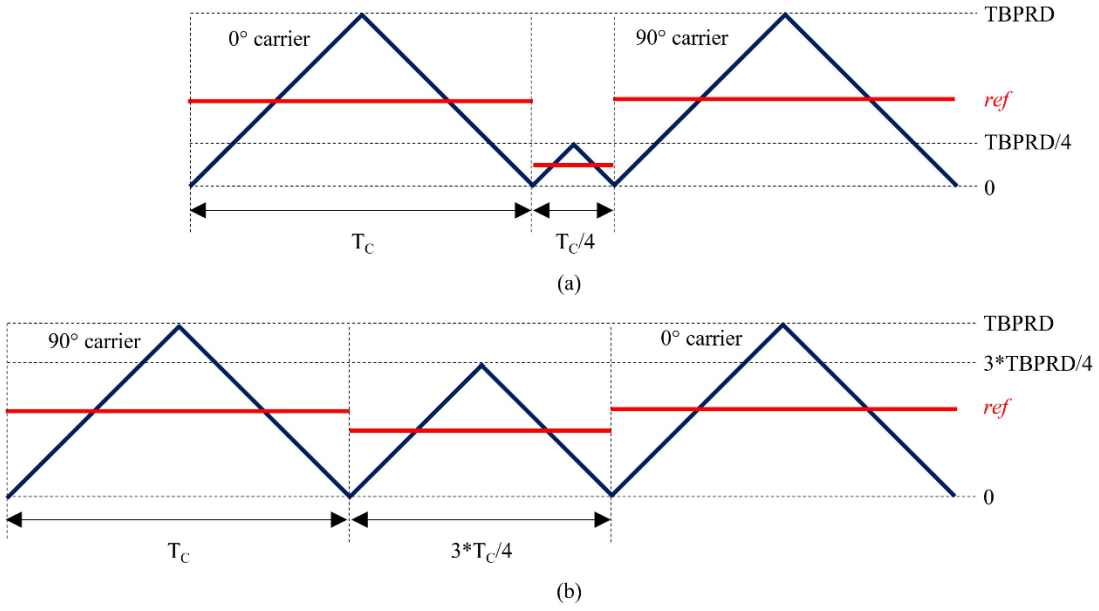

Fig. 4.7 High frequency carrier transitions in DSP (a) 0°-90° transition (b) 90°-0° transition

Furthermore, the transitions are classified based on the position of the carrier at the beginning of the transition. Based on the implementation of carrier frequency updates, there are two possible scenarios for each transition.

- At the carrier minimum (*Counter = 0*), Fig. 4.8 (a) and (b)
- At the carrier maximum (*Counter = TBPRD*), Fig. 4.8 (c) and (d)

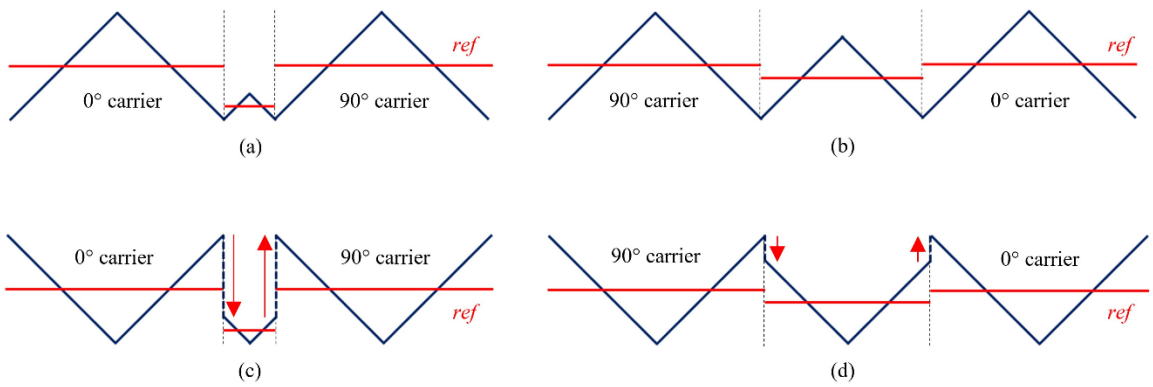

Fig. 4.8 Possible carrier transition scenarios (a) 0°-90° at carrier minimum (b) 90°-0° at carrier minimum (c) 0°-90° at carrier maximum (d) 90°-0° at carrier maximum

- Carrier Minimum Scenario: The Time-Base Counter is at zero at the beginning of the high frequency carrier cycle and therefore, the counter can proceed without any disruptions.
- Carrier Maximum Scenario: If the transition occurs at a maximum of the carrier, i.e. at counter = *TBPRD*, the counter value needs to be set to the new *TBPRD* before continuing with the high frequency. Also, at the end of the high frequency cycle, the counter value needs to be overwritten. These overwrites make the counting to be discontinuous as shown by red arrows in Fig. 4.8 (c) and (d).

Even though we can overwrite the counter value (*TBCTR* register), the bit representing the direction of counting (*TBSTS* register – *CTRDIR* bit) is read-only, and cannot be programmed as required. Therefore, the proper direction of counting cannot be assured after the forced discontinuity in the counter.

This scenario occurs at every transition as the carriers of the 2 legs of a phase are always 180° shifted and one of the carriers will be at the maximum when the other is at minimum.

4.5 Triangular and Sawtooth Carriers

The approach to avoid the discontinuity in the carriers is to use sawtooth-shaped carriers. The PWM pulses can be generated using asymmetric sawtooth carriers in the same way as the triangular carriers, but the quality of the output is compromised which is reflected in the total harmonic distortion of the voltage waveform [39].

A. Modified Sawtooth-Carrier Based PWM

The output pulses of the symmetrical and asymmetrical carriers are studied closely and an algorithm is developed to replicate the same PWM pattern as with the symmetrical carrier but using an asymmetrical carrier instead. The frequency of the asymmetrical sawtooth carrier is double the frequency of the symmetrical triangular carrier.

The output of the conventional triangular carrier, Fig. 4.9 (b), is constructed by the superimposition of outputs from two sawtooth carriers, one conventional, Fig. 4.9 (d), and the other with inverted reference and inverted switching logic, Fig. 4.9 (f). The resultant pulse pattern, Fig. 4.9 (g), is identical to the output from the triangular carrier PWM, Fig. 4.9 (b).

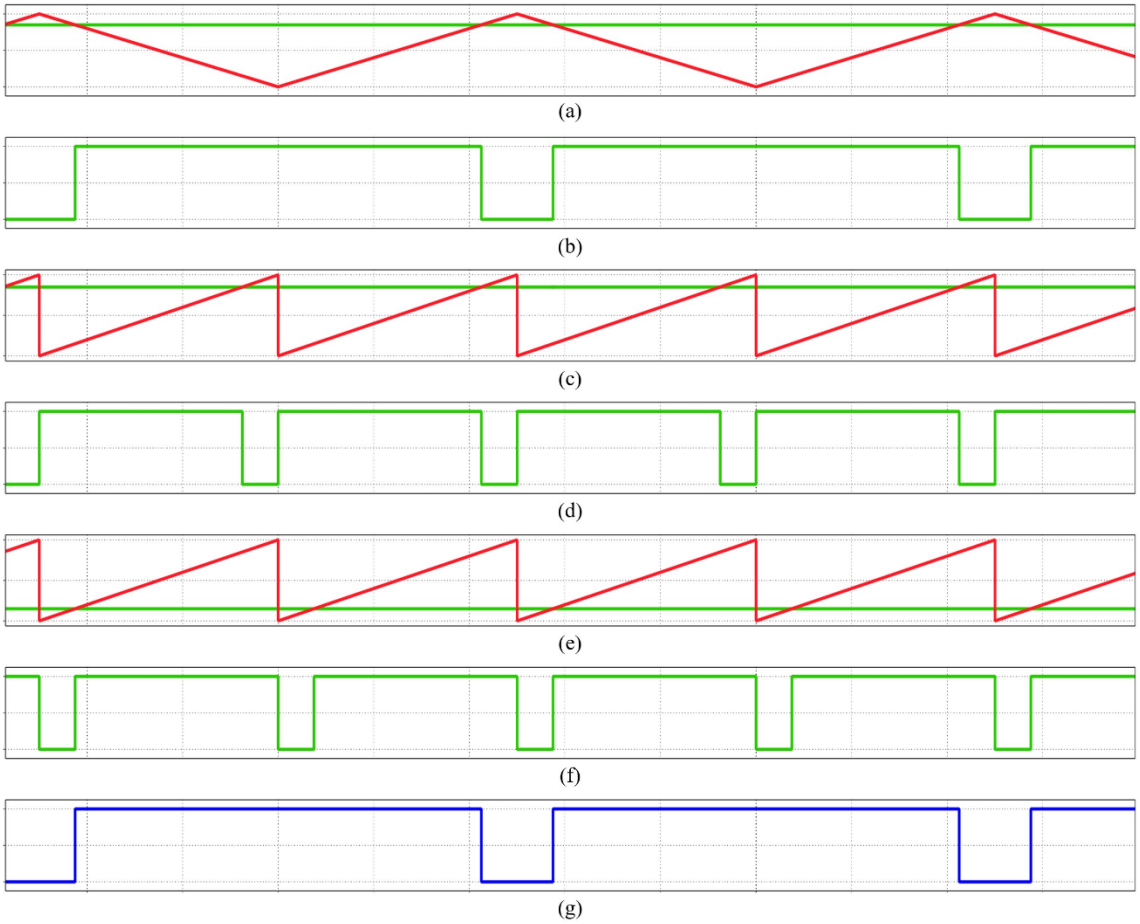

Fig. 4.9 Stepwise construction of modified sawtooth carrier PWM (a) conventional triangular carrier with reference (b) conventional PWM output (c) conventional sawtooth with reference (d) conventional sawtooth PWM output (e) sawtooth with inverted reference (f) sawtooth PWM with inverted reference and switching logic (g) combined sawtooth PWM output

There are two main actions that need to be taken every sawtooth cycle:

- Alternate between the *reference* and complement of the *reference,* (*1 - reference*)
- Alternate the switching logic

The reference signal is written to the compare signal register every carrier half-cycle (of the triangular carrier), and therefore alternating between the reference and its complement doesn't need extra processing power.

Alternating the switching logic can be done with a program code running every sawtooth cycle. This obviously uses up processing power of the DSP and can interfere with the rest of the program resulting in maloperation. Replacing the real-time run code with the TOGGLE function in the Action Qualifier submodule of the PWM module has been proved effective in reducing the burden on the processor and improving the reliability of the program.

B. Carrier Phase Shifts with Modified Sawtooth Carrier PWM

Obtaining the relevant carrier phase shifts with the modified sawtooth carrier PWM needs proper coordination among the phase of the sawtooth, switching logic and the modified reference as all of these aspects contribute towards the phase of the PWM pulses. The carriers of a phase will be 180° shifted with respect to each other at all times. In the implementation of modified sawtooth PWM, the carriers are in phase but the references are complementary and the switching logic is reversed. For the clarity of the illustrating the concept, carriers of one phase (phase A) are considered along with a constant reference, Fig. 4.10. Both the reference and its complement are shown, and the effective reference signal during a particular sawtooth cycle is denoted by solid lines.

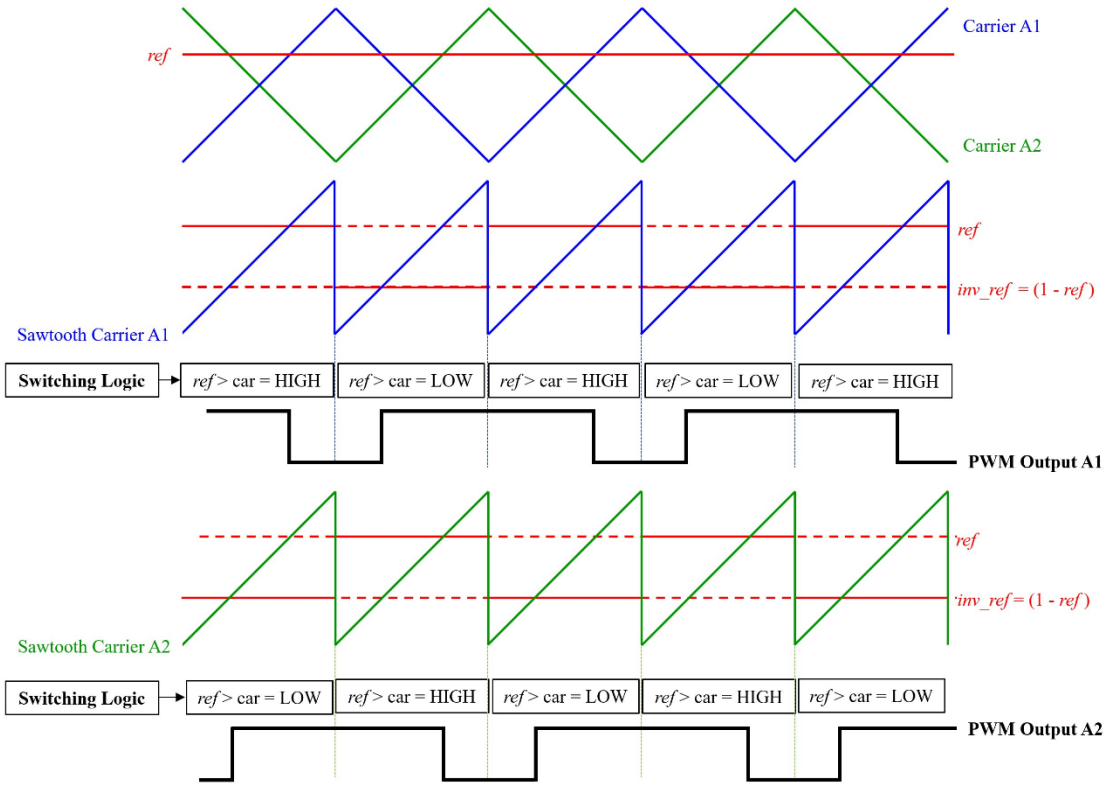

Fig. 4.10 Modified sawtooth PWM for 180° shifted carriers

C. HF Carrier Transition using Modified Sawtooth Carrier PWM

Once the relevant carrier phases are set, the same patterns are followed during the transitional high frequency carrier. The algorithm for the high frequency transition is the same as for the triangular carrier, with the only exception that there is no forced counter value overwrites with the sawtooth carrier as the counter resets every sawtooth cycle (or corresponding triangular half-cycle). It simplifies some logical expressions in the program and reduces the number of register value overwrites which improves the reliability of the execution of the program.

Zero-crossing of the sinusoidal wave corresponds to 0.5 when it is scaled to the interval [0,1]. Once scaled, the complement of the *reference* is given by *1 – reference*. Therefore, at the zero-crossing of the sinusoidal wave, both the reference and its complement are equal. But to get the 180° shift between the carriers, the switching logic needs to stay inverted. For the clarity of illustrations, the reference is assumed to be constant during and around the carrier transition, but in operation it is continuously updated maintaining the fundamental frequency precisely.

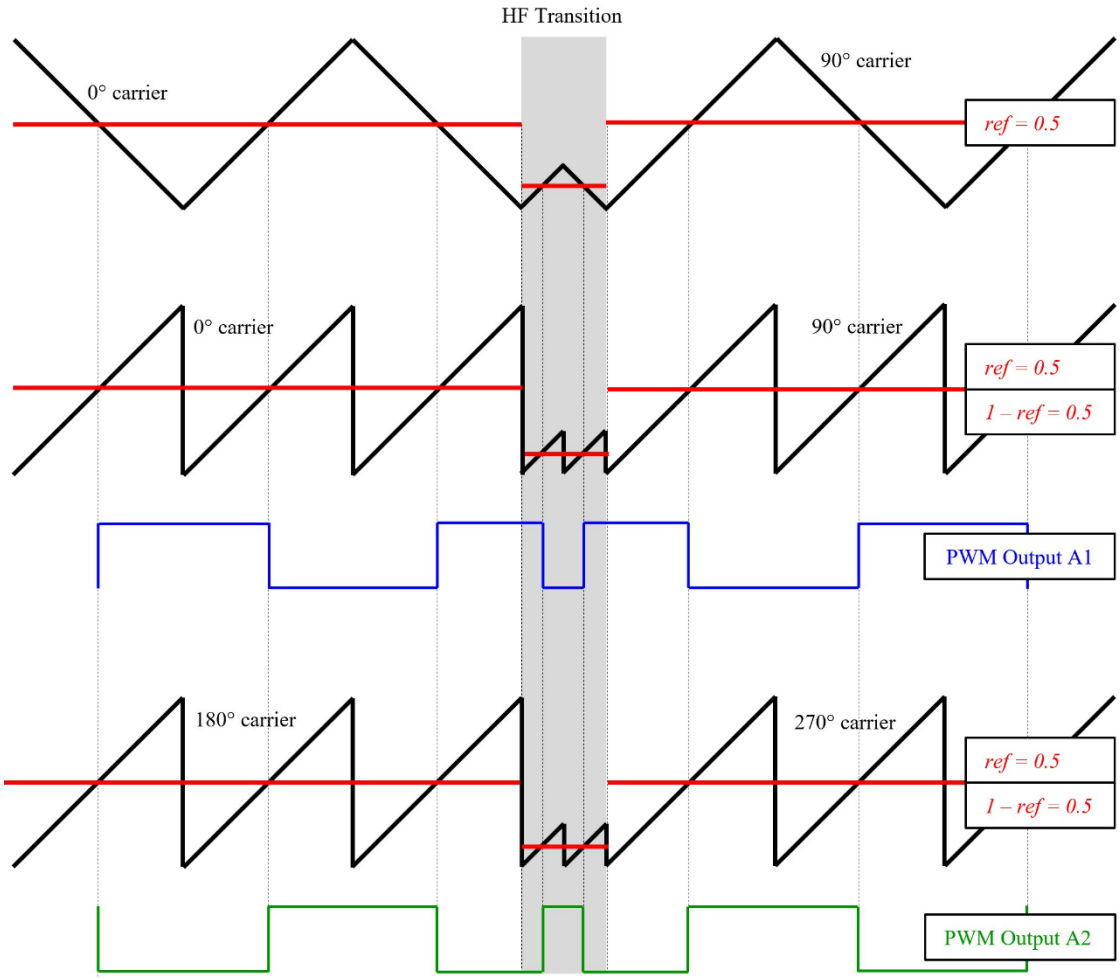

Fig. 4.11 High frequency carrier transition with modified sawtooth carrier PWM (0°-90° transition)

4.6 Carrier Synchronization

The PWM scheme requires carriers of different legs of the same phase to have a phase difference. Also, carriers need to have different phase shifts based on the value of the reference signal as well.

It is important that the carriers maintain the expected phase shifts precisely. Otherwise, they will result in PWM pulses shifting with respect to each other thereby possibly deteriorating the quality of the output voltage.

A. Unsynchronized Carriers

The carrier of each PWM channel is generated separately, in the Time Base Counter within the PWM module. These hardware units can experience delays which differ from one to another and they can get accumulated over time if left unaddressed.

Also, in the carrier transition technique used, PWM counters are continuously updated externally which can introduce further inconsistencies among different channels.

B. Continuous Synchronization

Synchronizing all the PWM carriers with a common signal ensures that any irregularities caused by delays within the counter are restored and the output PWM pulses are aligned such that expected results are produced. Synchronization is done periodically as carriers are being manipulated continuously and required to be monitored regularly.

C. Structure of Synchronization Scheme

The arrangement of PWM modules in the DSP limits the freedom in inter-module communication and it applies to input and output synchronization signals as well.

According to the Time-Base counter synchronization scheme (*Appendix B*) of the DSP [50], only the PWM channel 1 can generate a synchronizing signal that is accessible to all the other PWM channels. Hence, PWM1 is chosen as the master carrier. The 12 PWM channels of the are grouped into sets of 3, and one set each is reserved per phase. Only 2 PWM channels are used for the 2-legs per phase system, but the remaining output can be used for extending the system for a 3-legs per phase case, Fig. 4.12.

The master carrier, PWM1, is generating a sawtooth carrier with double the switching frequency, and a synchronizing signal every time it hits the minimum (0).

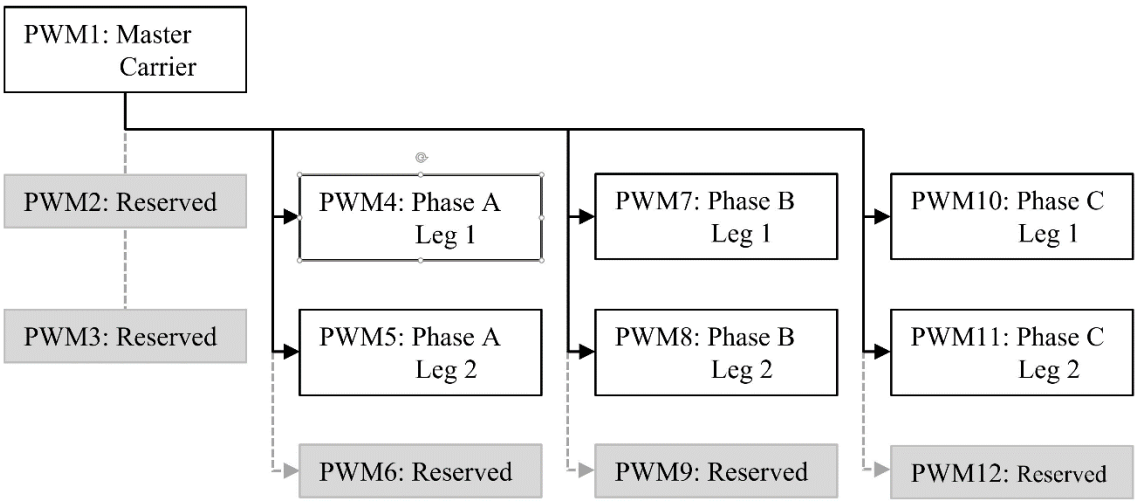

Fig. 4.12 PWM carrier synchronizing structure

D. Synchronizing with Different Phase Shifts

The master carrier is considered as the 0° carrier and all the other phase shifts are determined with respect to that. The master carrier generates the synchronizing signal which is directly passed on to other PWM channels.

The required phase shifts for the implementation of the presented PWM technique are 0°, 90°, 180° and 270° which will be applied to different inverter legs of different phases at different times. As the synchronizing pulse is generated, the respective counter values are fed into the phase loading register and the switching logic set as shown in Fig. 4.13 to force the required phase shift.

During high-frequency carrier cycles synchronization is disabled since the master carrier only generates synchronizing signals at the regular frequency. It is re-enabled with the new phase shift which ensures the high frequency transition produces the phase shift as expected.

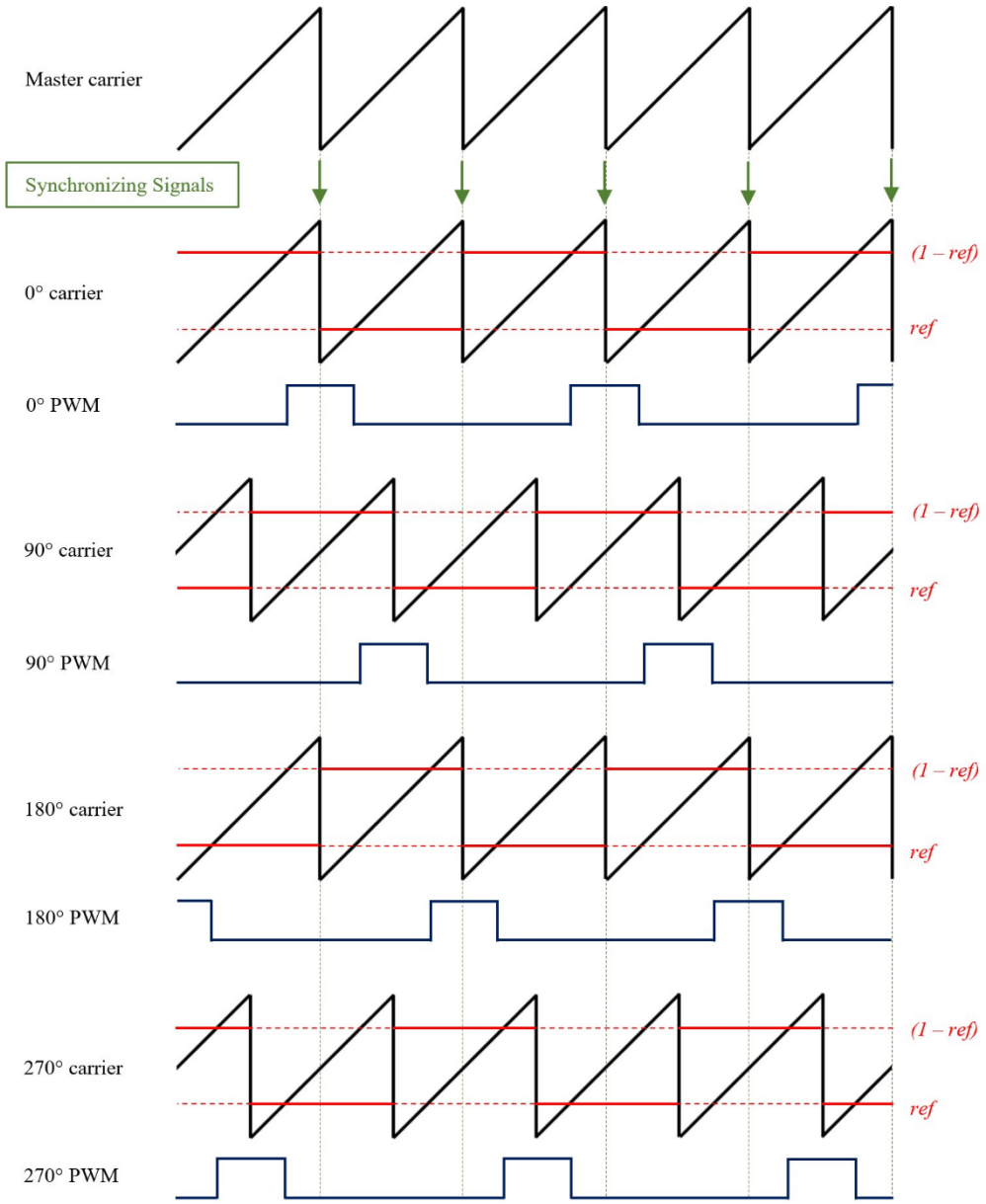

Fig. 4.13 Synchronizing signals and different phase shifts

4.7 Experimental Results

The presented high frequency carrier transition technique is implemented SiC MOSFET based prototype converter. Even though parallel inverters are primarily used to handle high power, the focus of the thesis is to test and validate the concept of high frequency carrier transition. Hence the system was tested under 300 V dc link, delivering slightly over 4 kW. Also, it was tested with an RL load instead of directly connecting to the grid.

A. Experimental Setup

i. Hardware Setup

DSP control card: Delfino™ TMS320F28379D controlCARD R1.3

Power electronic switches: Half-bridge modules with SiC MOSFETs

Coupled inductor type: Separate C-cores

DC power supply: Sorensen SGX400X25

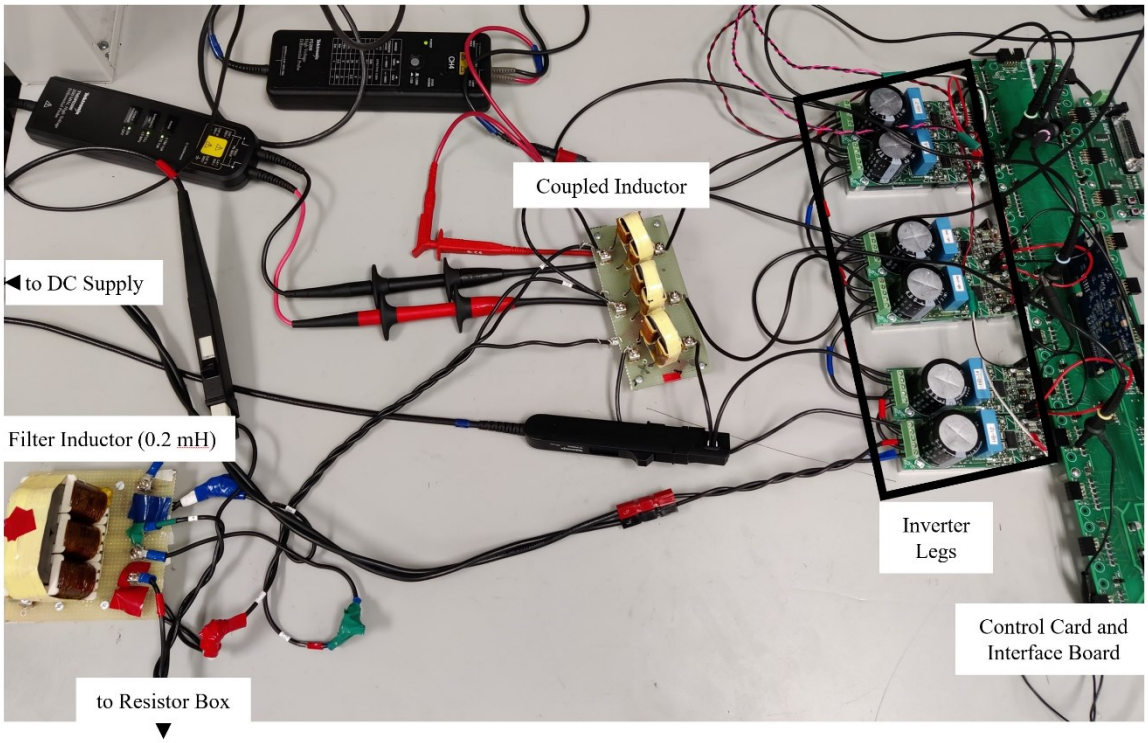

Fig. 4.14 Experimental setup

ii. System Parameters

The dc link voltage of 150 V is used to get the results for instantaneous carrier change as higher voltages might saturate the magnetic cores. Hence, 150 V is taken as the base voltage for the comparison.

Table 4-2 System Parameters

Parameter	Value
Carrier frequency	10 kHz
Fundamental frequency	60 Hz
DC-link Voltage	150 V*, 300 V
Coupled inductor winding inductance	0.7 mH
Filter inductor inductance (per phase)	0.2 mH
Load resistance (per phase)	22 Ω

B. PWM Output Signals

PWM output signals are observed initially to ensure the proper implementation of carrier transitions and the consistency of program. The reference signals, sine waves superimposed with the 3rd harmonic are shown in Fig. 4.15.

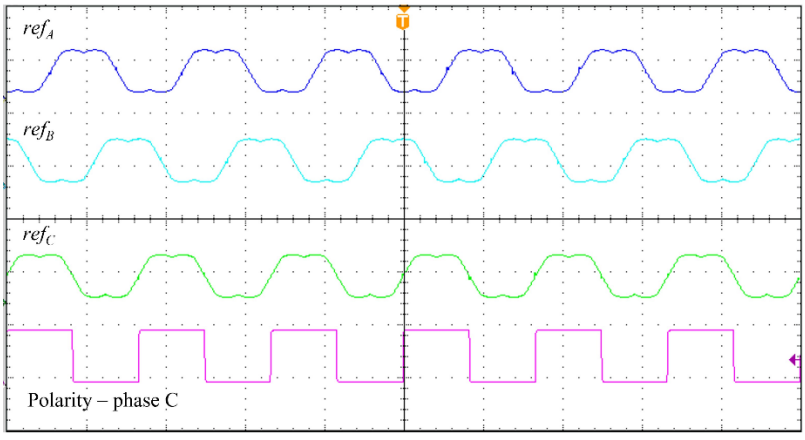

Fig. 4.15 3-ph reference signals (with 3rd harmonic)

The two transitions 0°-90°, Fig. 4.16 (a), and 90°-0°, Fig. 4.16 (b), for phase B is captured. The transitions complete as expected and other two phases continue to operate in the regular pattern.

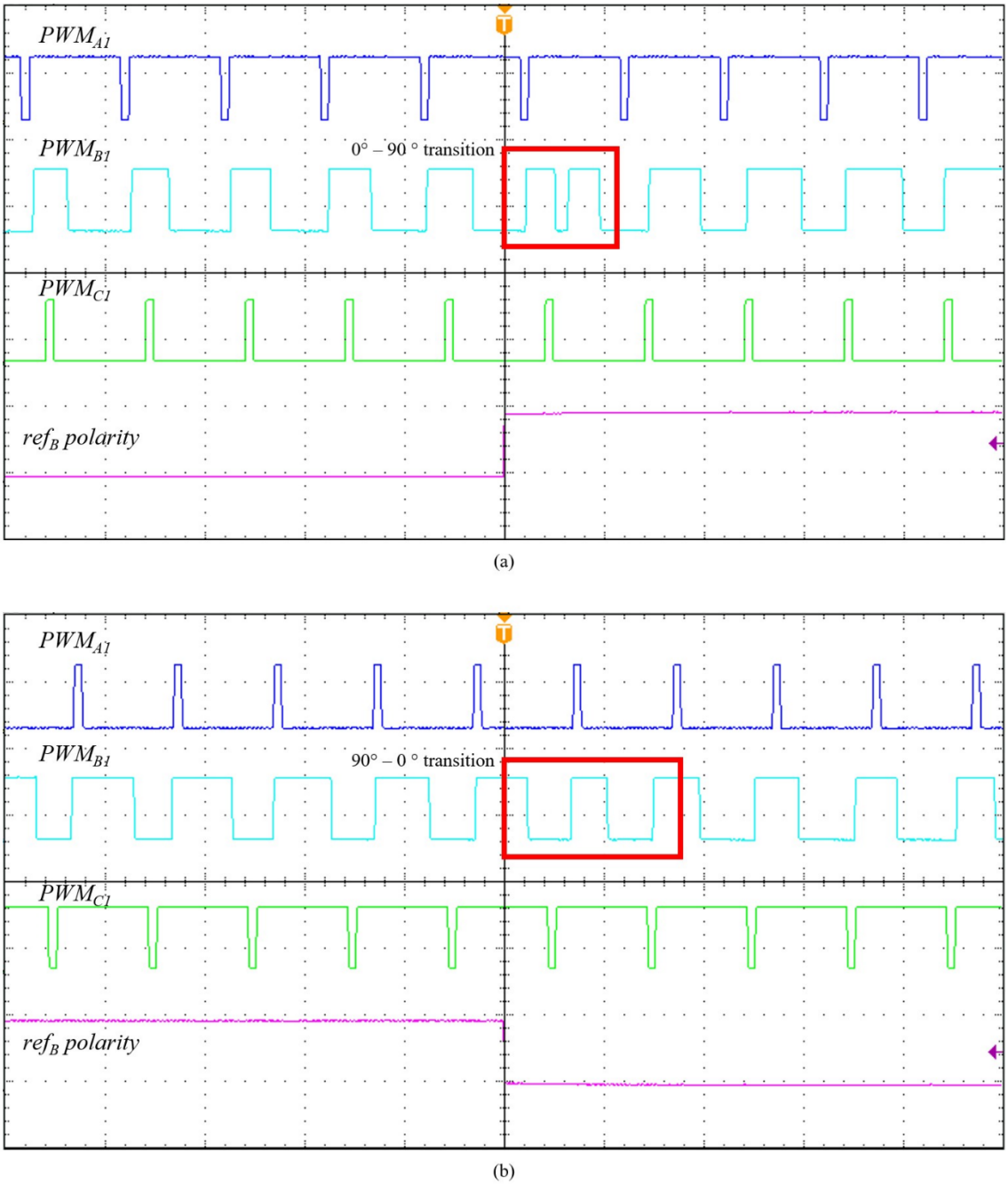

Fig. 4.16 PWM pulses for three legs from 3-phases at carrier transitions of phase B (a) 0°-90° transition (b) 90°-0° transition

C. Steady-State Operation

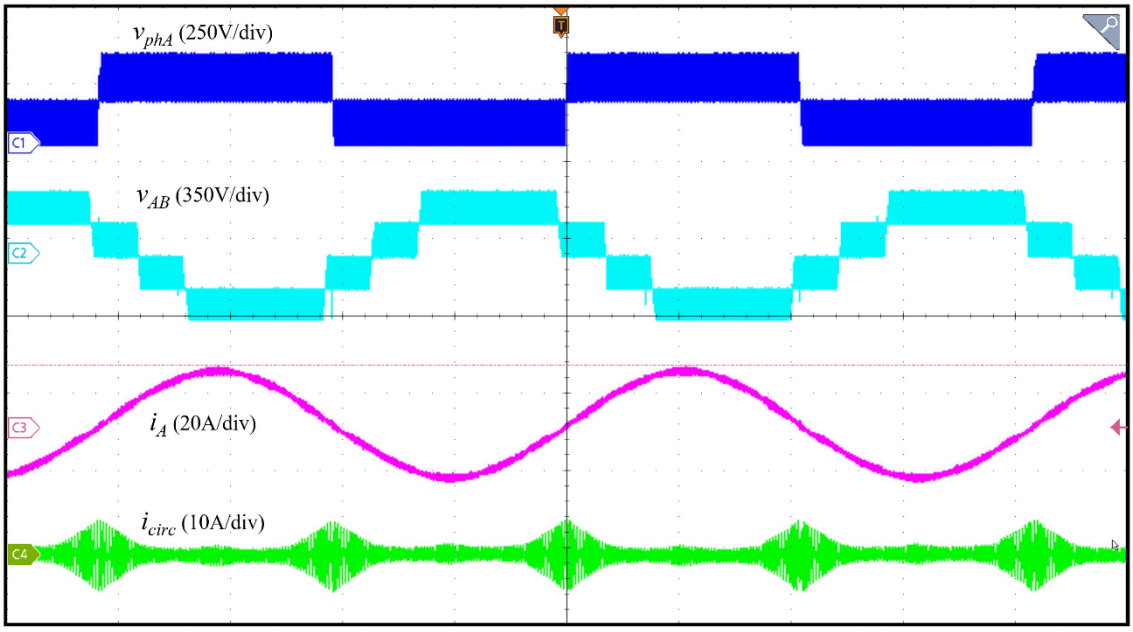

Fig. 4.17 Steady state operation with HF carrier transitions (V_{dc} = 300 V, f_c = 10 kHz, m_a = 1.13, f_1 = 60 Hz)

The phase voltage output v_{phA}, line-to-line voltage v_{AB}, load current i_A and the circulating current i_{circ} of phase A is captured, Fig. 4.17. All the waveforms are in order with good quality attainable with the circuit topology.

i. Comparison between Different PWM Techniques

A steady-state comparison for the phase voltage, v_{phA}, winding currents, i_{A1}, i_{A2}, circulating current, i_{circ}, line-to-line voltage, v_{AB}, and the load currents, i_A, i_B, i_C, is done among the cases; PS PWM, Enhanced PS PWM and Enhanced PS PWM with HF transition, Fig. 4.18,

With PS PWM the line voltage has very high harmonic content while the rest of the waveforms are normal. With the implementation of PS PWM, the line voltage is made better at the expense of winding currents and the circulating current. Also, glitches are present in the load current waveforms at the instances of carrier changes in at least one of the phases. The HF carrier transition resolve the jumps in the winding and circulating currents and the glitches in the load current while preserving the quality of the rest of the waveforms. This has been lacking in previous work.

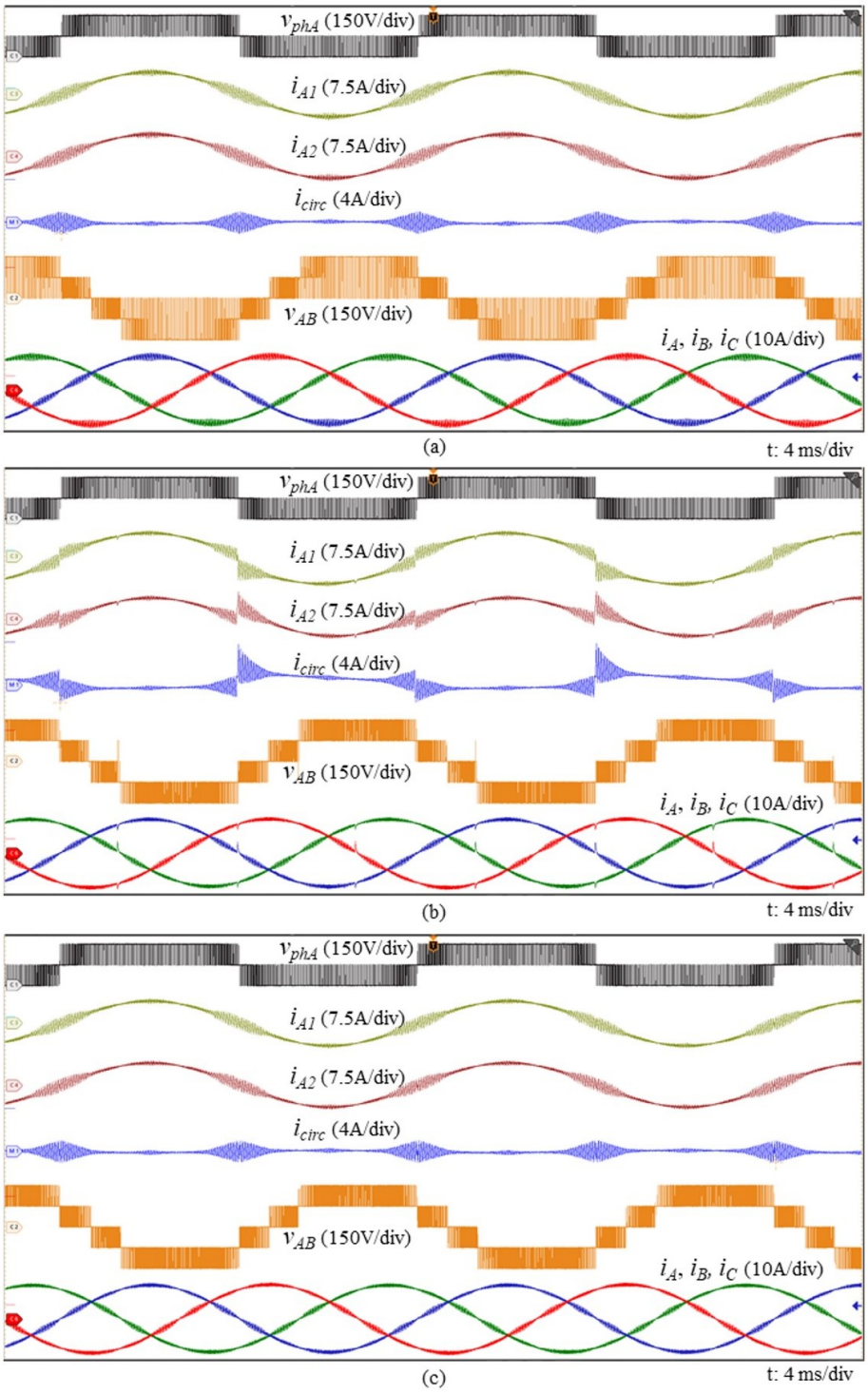

Fig. 4.18 Steady state operation (a) PS PWM (b) enhanced PS PWM (c) enhanced PS PWM with HF carrier transitions (V_{dc} = 150 V, f_c = 10 kHz, m_a = 1.13, f_1 = 60 Hz)

ii. Transient during Carrier Transition

The transient behavior of the circulating current during the instantaneous carrier change, Fig. 4.19 (a), and the carrier change with high frequency transition, Fig. 4.19 (b), clearly shows how the high frequency carrier cycle reverses the direction of increasing circulating current and thereby prevent any high peaks.

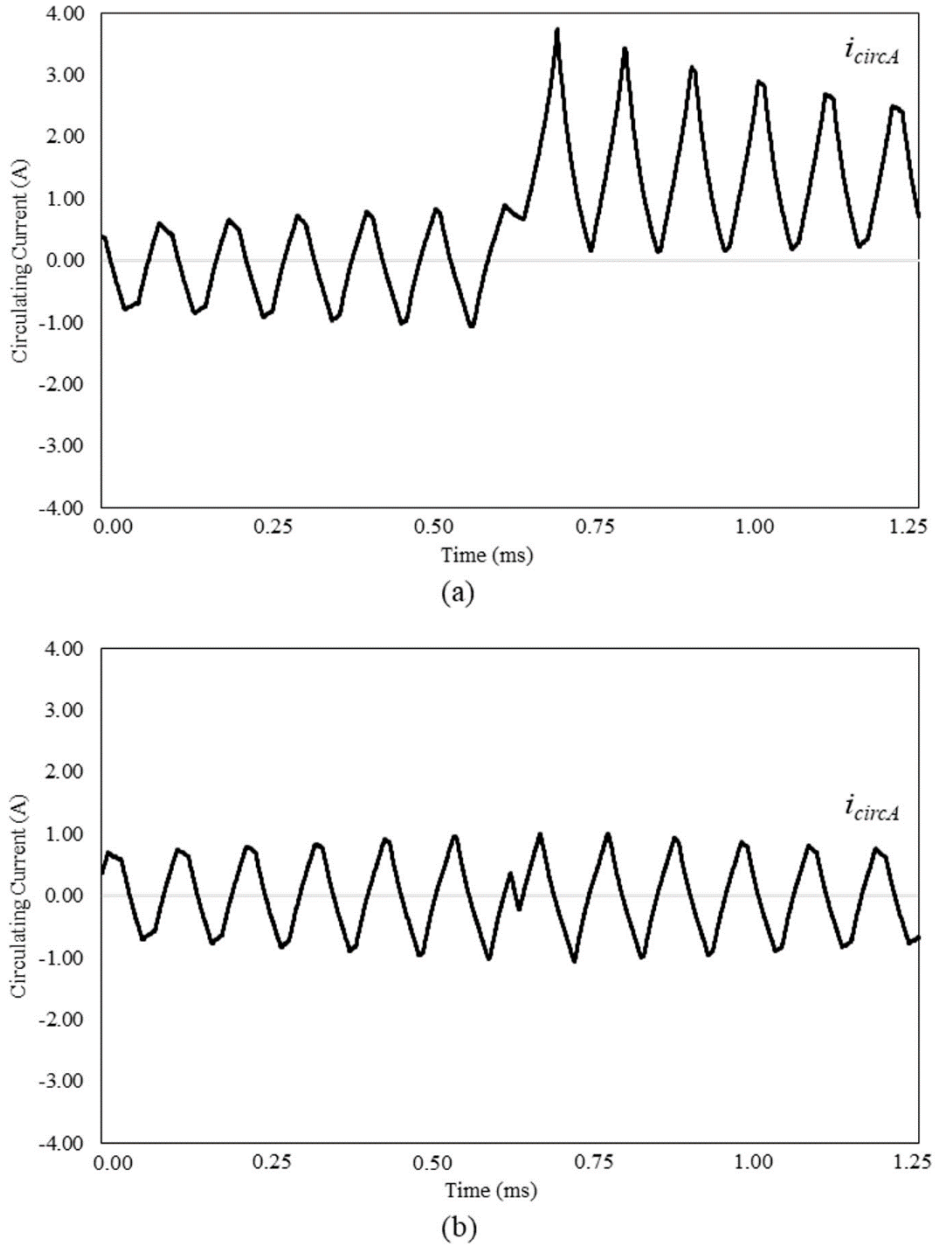

Fig. 4.19 Circulating current in phase A (a) enhanced PS PWM (b) enhanced PS PWM with HF carrier transition (V_{dc} = 150 V, f_c = 10 kHz, m_a = 1.13, f_1 = 60 Hz)

D. Step Change Response

The performance of the system under a forced step change in the modulation depth is presented in Fig. 4.20. The waveform confirms that the system responds to the change without any distortion. Also, it confirms that the system operates without any jumps in the circulating current or distortions in the line-to-line voltage at low modulation depths as well as at high modulation depths.

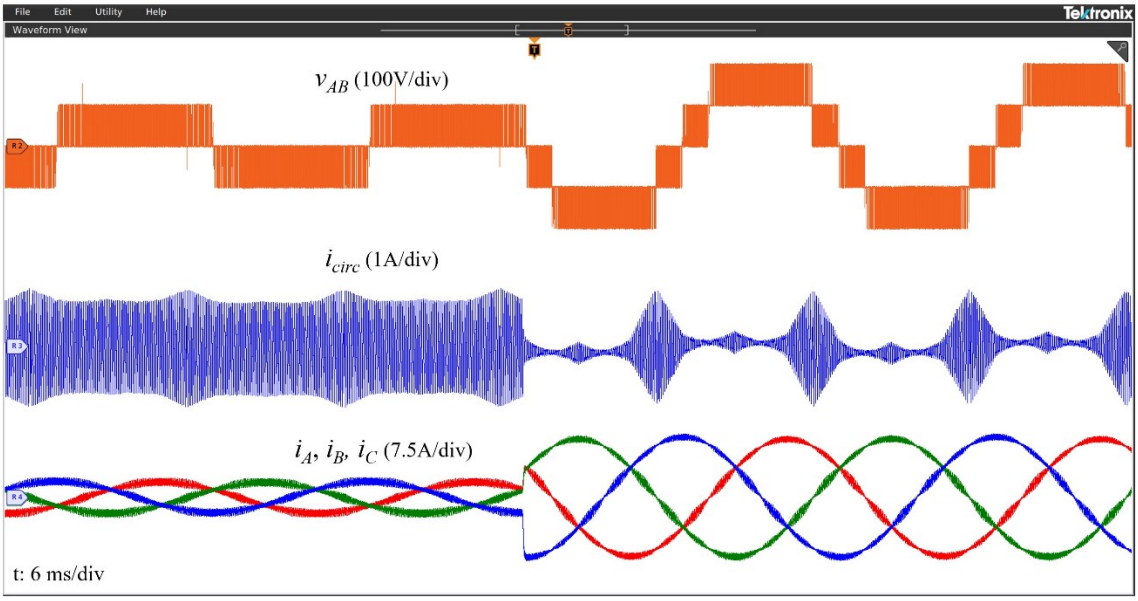

Fig. 4.20 Operation under a step change in m_a (a) enhanced PS PWM (b) enhanced PS PWM with HF carrier transitions (V_{dc} = 150 V, f_c = 10 kHz, m_a = 0.3 to 1.13, f_1 = 60 Hz)

4.8 Summary

This chapter focuses on the practical realization of the high-frequency carrier concept introduced in the previous chapter. Basic features of the DSP related to the implementation of the technique is discussed at first. Next, the execution of instantaneous carrier change in the DSP is explained along with the output PWM pulses. The implementation of high frequency transition is investigated and the resulting discontinuities in the carrier counters are identified. Sawtooth carrier is considered as an alternative approach and an algorithm is developed to generate PWM output similar to triangular carrier as it is better in quality. The HF transitions as well as tactics to maintain the proper phase shifts with the sawtooth carriers are explained and the synchronization scheme is discussed before moving in to the experimental results. Under the experimental results, the setup is briefed along with the system parameters. Experimental results are presented categorized into steady state and step change in modulation depths and a comparison with other techniques is conducted before concluding.

Chapter 5

Conclusion

Parallel connection of voltage-source converters is becoming popular as the demand for high power converters under restrained voltage increases. Using interleaved PWM for parallel VSCs is advantageous as it generates a multi-level output with a ripple frequency that is a multiple of the switching frequency. There are several interleaving techniques with their own merits and demerits, and phase-shifted PWM is chosen due to its easy adaptability to systems with higher number of parallel inverters.

PS PWM produces line-to-line voltages with high harmonic content due to unaligned output pulses from different phases. Enhanced PS PWM is adopted to improve the quality of line voltages but in turn, it makes the circulating current, and the flux in the inductors between the parallel inverter legs, to jump and result in dc offsets within certain sections of the reference as verified by simulation and experimental waveforms.

The high-frequency carrier cycle concept is presented as a solution to the jumps in the circulating currents and flux. High-frequency carrier cycle offers a smooth transition for the carrier changes demanded by the enhanced PS PWM as the current jumps are resulted from the abrupt changes forced on the carriers. The carriers transition through a higher frequency which is determined by the phase shift between the two carrier sets.

The HF carrier transition technique is explained for 2 inverter legs per phase system and then it is generalized to an arbitrary number of inverter legs. The only difference when the number of parallel legs is increased is the change in the frequency of the transitional carriers, while the concept remains the same. This technique maintains the average phase output at the same level which ensures the quality of the output current waveforms.

Finally, the concept is implemented in a DSP environment. The basics needed for carrier frequency manipulation on the DSP platform are discussed. The triangular carrier PWM is implemented with sawtooth carriers by manipulating the reference and the switching logic as sawtooth carriers offer more reliable control over changing the carrier frequency in quick

succession. The DSP is programmed using C-program as it provides more freedom to access the registers easily.

It is then used to drive an inverter with 2 parallel legs per each phase and transfer power from a dc power source to an R-L load. The system is run under steady state conditions and under a forced step change in modulation depth. The resultant waveforms are presented and the improvements made on those are discussed. The line voltages are made to have distinct levels and the circulating currents maintained as if the carriers are untouched. Also, the output voltage and load current waveforms are also undisturbed.

Hence, it can be concluded that the presented HF carrier transition technique is an improvement over the existing techniques.

A. Future Work

The work presented here concentrates on conceptualizing the high-frequency carrier transition concept. And it has been implemented on a 2-parallel legs per phase system as a proof of concept. There are several avenues to extend this work and to make the best use of it.

i. Extend to Higher Number of Parallel Legs per Phase

The concept is already generalized to an arbitrary number of parallel legs. Hence, it is only a matter of hardware implement. It should be noted that as the number of parallel inverter legs increases the line-to-line voltage acquire more levels and therefore, switching between non-adjacent level makes little impact on the overall quality. That being said, it is still beneficial to adopt this system up to about 5 parallel legs

ii. Incorporate closed-loop control

Most of the applications of parallel VSIs involve connecting to the main grid and for that closed loop current control algorithm needs to be incorporated. It requires further studies related to interactions that might occur between control algorithm and the carrier transition technique. It is an important step ahead as the quality of the output is one of the main concerns related to grid connected systems.

iii. Implementing with Other Circuit Topologies

Case-by-case studies are required to determine the effectiveness based on the benefits, limitations and disadvantages of adopting carrier transition technique. The gain from the implementing an additional algorithm, which consume some resources, should substantially outweigh its cons.

iv. Single-Carrier Approach

Obtaining the similar performance using a single carrier with reference manipulation instead of carrier change through transitions can be explored. This approach could simplify the implementation on the DSP.

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Appendices

Appendix A – Frequently Used PWM Registers

Register Name	Acronym
Action Qualifier Control Register for Output A	AQCTLA
Counter Compare A Register	CMPA
Time Base Control Register	TBCTL
Time Base Period Register	TBPRD
Time Base Phase High	TBPHS
Event Trigger Selection Register	ETSEL
Dead-Band Generator Rising Edge Delay Count Register	DBRED
Dead-Band Generator Falling Edge Delay Count Register	DBFED
Dead-Band Generator Control Register	DBCTL
Event Trigger Pre-Scale Register	ETPS

Appendix B – Time-Base Counter Synchronization Scheme

(Extracted from TI Technical Reference Manual – TMS320F2837xD Dual-Core Microcontrollers)