University of Alberta

Damping and Harmonic Control of DG Interfacing Power Converters

by

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Abstract

A large number of renewable energy resources have been installed in the power distribution system in the form of distribution generation. To interconnect renewable energy resources to the utility power system, the power electronics converter is often used as an efficient interface of distributed generation units. However, the presence of power converters with high order LC or LCL filters also introduces many harmonic and resonance problems to power distribution systems. In addition, the growing application of distributed nonlinear loads further aggravates the harmonic distortions in the power distribution system.

To solve these problems, this thesis discusses interfacing converter control method that actively mitigates the resonances and harmonics in power distribution systems. The first objective is to provide sufficient damping effect to distributed generation unit interfacing converter filters through improved inverter control. To realize this objective, this thesis conducts an in-depth investigation on resonances in both a single inverter and multiple parallel inverters. The virtual impedance based damping method is proposed to realize better control of interfacing converters. The second objective of this thesis is to compensate the impact of nonlinear loads in the low voltage distribution system through flexible operation of interfacing converters. In the scenario, the interfacing converter essentially works as a virtual harmonic filter. A number of power distribution system harmonic compensation methods are proposed. They aim to realize better power quality of future power electronics intensive power distribution systems.

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List of Abbreviations

AC	Alternating Current
APF	Active Power Filter
CB	Circuit Breaker
CCM	Current Control Method
CFL	Compact Fluorescent Lamp
DC	Direct Current
DG	Distributed Generation
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array
FLL	Frequency Locked Loop
GCC	Generalized Closed-loop Control
HCM	Hybrid Control Method
PCC	Point of Common Coupling
PoC	Point of Connection
PLL	Phase Locked Loop
PR	Proportional and Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Resource

SOGI	Second Order Generalized Integrator
THD	Total Harmonic Distortion
VCM	Voltage Control Method
WT	Wind Turbine

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Chapter 1

Introduction

Increasing concerns about costs associated with and pollution caused by fossil fuel energy based power generation have popularized renewable energy sources (RES) such as photovoltaic energy, wind energy, and fuel cells as means to provide power [1]-[4]. As most RESs have DC or uncontrolled AC output power characteristics that are not ready for grid integration, a power electronics converter is often adopted as an efficient interface to interconnect these distributed generation (DG) systems to the utility grid [5]-[7].

Power electronics converters must be designed and controlled properly to avoid the injection of harmonic pollution to the power distribution system. The application of nonlinear loads (e.g., a compact fluorescent lamp), together with the integration of many small power DG units, can cause a wide range of problems [8]-[10]. To solve these problems, various types of passive filters or active filters can be used, but a better way of improving power quality is to absorb harmonics through improved control of power electronics interfacing converters. The research reported in this thesis was undertaken to (1) reduce harmonic pollution from DG units, and (2) compensate nonlinear load harmonics by using DG unit power electronics converters.

1.1. Harmonics and resonance in a DG system power electronics interface

This section starts with a review of resonances in both single inverter and multiple inverters. Passive and active damping methods are introduced.

1.1.1. Harmonic and resonance in a single DG system

Due to the intermittent nature of many renewable energy sources and the complexity of power electronic circuits, interfacing converters have introduced problems to conventional power distribution systems, such as harmonics, protection interference, leakage current, grounding issue, and reversed power flow. The harmonic pollution from a DG interfacing converter can be divided into three categories: switching ripples, harmonics caused by output filter resonance, and harmonics caused by control.

- **Switching ripples**

The modern interfacing converter normally adopts fully controllable switches such as insulated gate bipolar transistors (IGBT) and metal-oxide-semiconductor field-effect transistors (MOSFET) to form the converter bridge. The pulse width modulation (PWM) in the converter produces switching harmonics in the output voltage of the inverter. Typically, these switching ripples can be attenuated by output filters such as series choke or high-order low-pass filters. Passive output filters that are not designed properly can inject switching ripples to the utility grid.

- **Harmonics caused by output filter resonance**

High-order filters such as LC and LCL filters (Fig. 1. 1) have been adopted to absorb switching harmonics from the converter. However, the internal resonance of high-order filters might adversely introduce some resonance current at the characteristic frequency. In addition, the output filter might interact with other passive components in the power distribution system, causing additional resonance current in the filter.

- **Harmonics caused by control**

The control scheme of a DG power converter can have a significant impact on the power quality of the DG line current. For instance, a maximum power point tracking (MPPT) scheme is often used to realize better energy harvesting from photovoltaic (PV) panels. The time-varying feature of current reference for

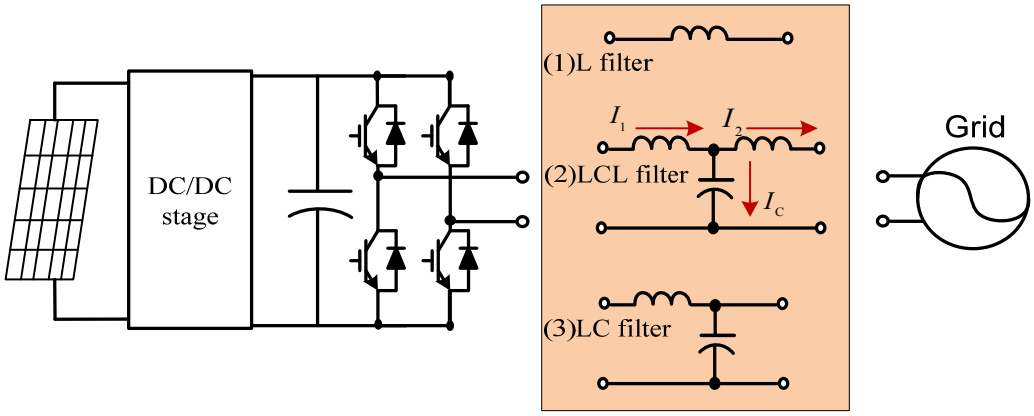

Fig. 1. 1. Interfacing converter with various types of output filters.

MPPT may cause inter-harmonics and sub-harmonics in the DG unit line current [19]. Additionally, if the control scheme is designed without sufficient grid disturbance rejection capability, grid disturbances such as sags, swells, and flickers might cause nontrivial harmonic pollution in the DG unit line current.

As most DG units are interfaced to the power distribution system by controlling the line current, the requirements for DG line current quality are specified by national or international grid codes such as IEEE-1547 and IEEE-519 [27][28]. IEEE-1547 sets the limits for individual low order harmonic and total harmonic distortion (THD) to 2% and 5%, respectively.

1.1.2. Interactions between multiple interfacing converters

Multiple parallel DG systems are increasingly used to achieve better energy harvesting from RESs. For instance, many small power PV inverters and wind power converters are installed in a low voltage residential power distribution system [9]. Fig. 1. 2 shows a diagram of a simple distribution system with multiple DG units. In addition to resonance in interfacing converter output filters, interactions between interfacing converters may cause other power distribution system problems.

The most obvious problem is voltage regulation. Due to the high penetration level of RESs, the reversed power flow in a low voltage distribution system can

cause noticeable voltage variations in the distribution feeders [25]. To alleviate this problem, the grid code of Germany [26] was revised to allow a solar inverter to control reactive power generation to assist voltage regulation. Only a few cases of harmonic aggregation problem in multiple DG units have been reported [9]. However, the standard [27] is specified to cover a high penetration of solar inverters that is expected to cause more harmonic distortions in the near future.

Similar to multiple DG units, a single centralized high power DG unit can adopt multiple parallel inverter modules to connect a renewable energy source to the grid. A typical example is the full power rating converter for the wind power synchronous generator as shown in Fig. 1. 3. Due to current rating limits of

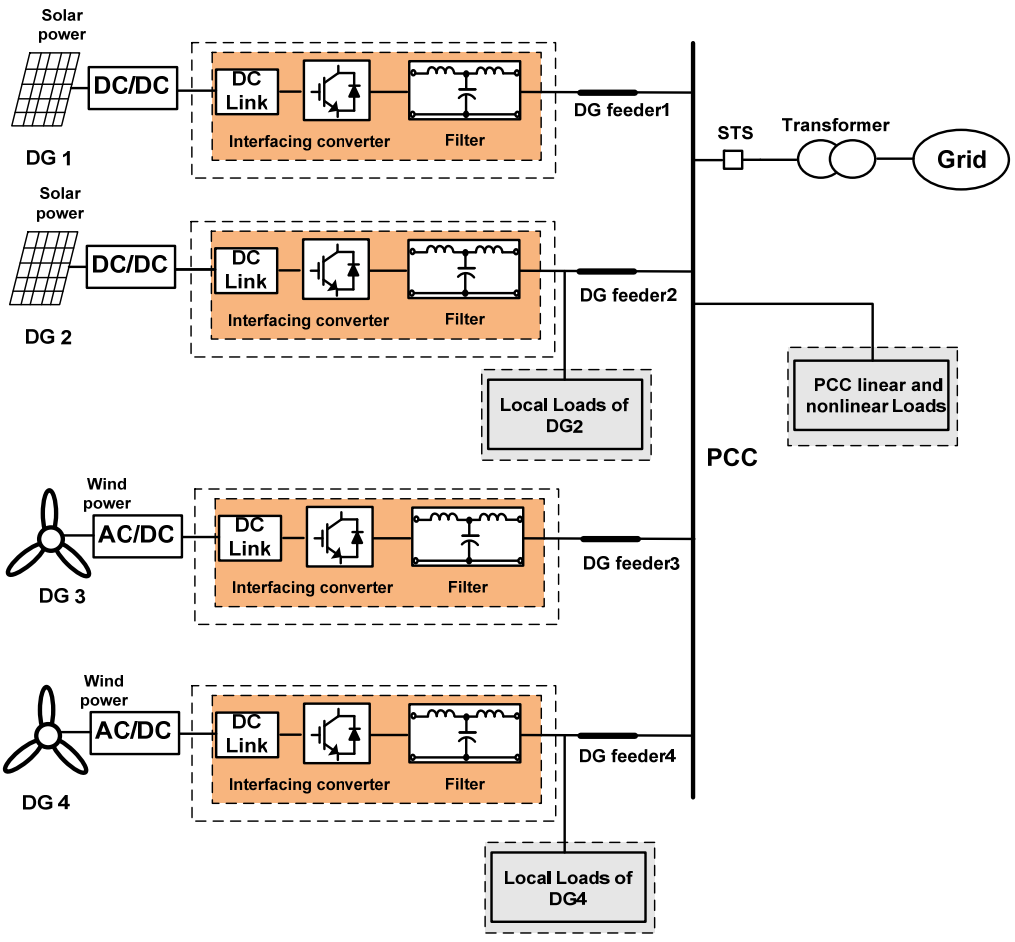

Fig. 1. 2. Distribution system with multiple DG units.

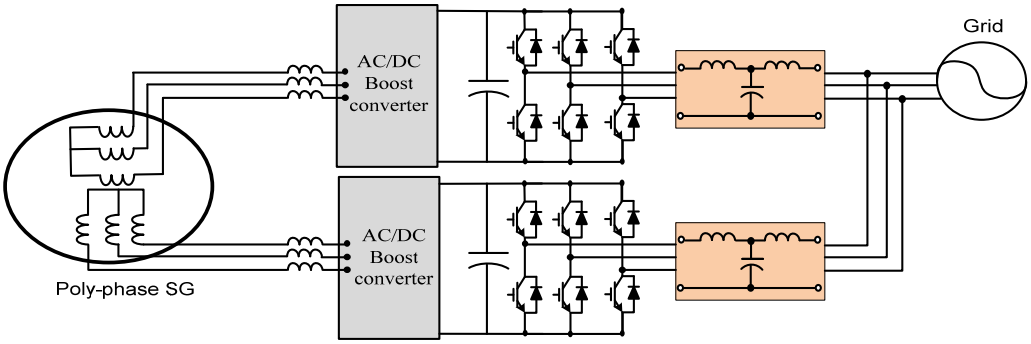

Fig. 1. 3. Wind power conversion using parallel converters.

power electronics switches, two parallel inverters are used to connect the poly-phase synchronous generator to the utility grid. As two inverters are coupled together, the resonance in one inverter can interact with the resonance in the other converter, resulting in more harmonic distortions in the inverter line current.

1.1.3. Harmonic distortion mitigation methods for DG systems

To mitigate the harmonic distortions from DG units, both the interfacing converter power circuit and the control scheme need to be properly designed. First, a series choke can be placed at the interfacing converter output to reduce the switching ripples from the interfacing power electronic converter. Alternatively, high-order LCL and LC filters are proposed to reduce the size of the output filter and to reduce power loss on the filter [29]. However, ideal LCL and LC filters have zero impedance at resonant frequency, which can adversely introduce some resonance current. To obtain high power quality DG line current, a high order filter with proper damping is mandatory. Damping can be achieved by either passive or active methods.

- **Passive damping**

Passive damping can be realized by using physical resistors to absorb the resonance energy. For an LCL filter in Fig. 1. 4, there are six places to install the damping resistor [29]. A damping resistor connected in series with the shunt

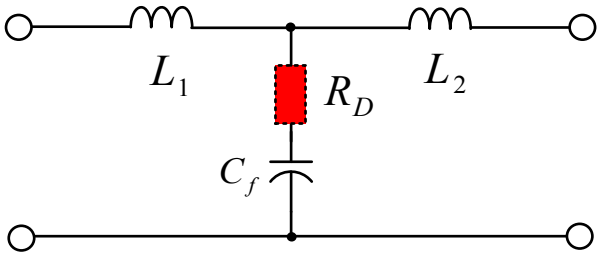

Fig. 1. 4. Installation of passive damping resistor in an LCL filter.

capacitor is more widely used, as the power loss is lower compared to the power loss from damping resistor installed in other parts of the LCL.

With sufficient passive damping, conventional current control methods without any active damping effects, such as deadbeat control, hysteresis bang-bang control, or single-loop proportional-integral derivative (PID) control, can be used to control the inverter current.

- **Active damping**

Thanks to advances in hard switching power electronic semiconductors, the switching frequency and control bandwidth of a DG power electronics converter can be much higher than the resonant frequency of output filters, even for wind power converters at a few megawatts (MW) [31]. As a result, active control methods are a better way to provide damping effects to the filter. The goal of active damping is to dynamically update the inverter output voltage according to resonance mitigation requirements.

Active damping methods can be divided into two categories: high order controllers without using additional measurement [32] and multi-loop control with additional measurement. The aim of using a high order controller is to alleviate the zero-impedance effect of the LCL or LC filter at resonant frequency. Many high order controllers have been proposed such as the lead-leg compensator based method [33] (Fig. 1. 5), where only line current I_2 is measured to realize active damping, and the pole-zero cancellation method [34] [35].

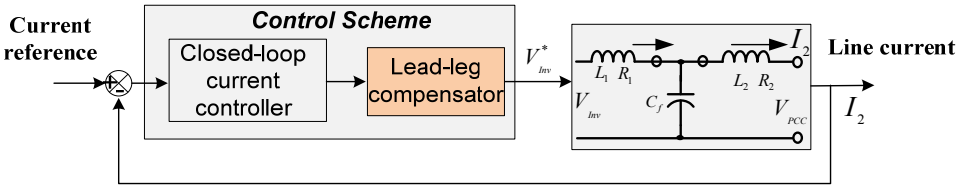

Fig. 1. 5. Average model of active damping using a single-loop control with lead-leg compensator.

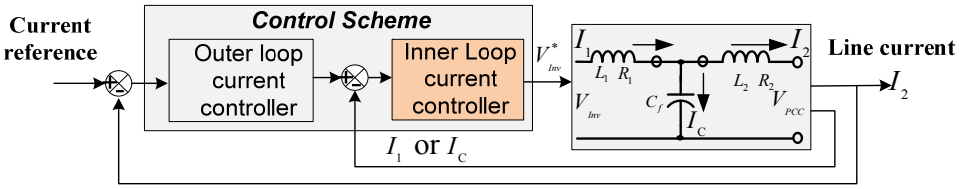

Fig. 1. 6. Average model of active damping using a double-loop current control scheme.

Note that a high order controller often brings additional noise to the system. Furthermore, system stability cannot be guaranteed if there are nontrivial parameter variations in the system such as dramatic changes in source impedance. Alternatively, multi-loop control is proposed to improve the quality of the interfacing converter line current. Due to more state feedback measurement [32], damping performance can be less sensitive to parameter variations. In [36], a double-loop control is applied to a grid-connected inverter where the outer loop is the line current control and the inner loop is the filter capacitor current control. Fig. 1. 6 shows that either the capacitor current I_c or the inverter output current I_1 (illustrated in Fig. 1. 1) can be measured as inner loop feedback. Similarly, the double-loop control is also used to control the LC filter capacitor voltage [37]. In this case, the inverter can work in an autonomous islanding operation mode which offers continuous power to the critical loads in the case of utility mains interruption.

In addition to multi-loop control, virtual impedance based control methods have been proposed to further improve damping performance in the system [29].

Virtual impedance control emulates the behavior of passive damping impedance by modifying the control reference. However, the position and value of virtual impedance have not been clarified in the literature. As the virtual impedance control modifies the original output filter plant, the conventional control scheme parameter design criteria need to be revised considering the impact of the modified filter.

1.2. Harmonic distortion compensation in a power distribution system

To compensate for harmonic distortions in a power distribution system, passive filters, including single-frequency tuned filters and high pass filters, are normally adopted due to their low cost and high reliability. Although passive filters are the dominant filtering component in power systems nowadays, they are not very flexible and might introduce additional resonances by interacting with other components in the system. Due to the limitations of conventional passive filters and the significant advances in power electronics technology, attention has been focused on power electronics conditioners for harmonic compensation. The power electronics conditioner can be either an active power filter (APF) with rapid harmonic current tracking capability or a multifunctional interfacing converter with auxiliary harmonic compensation service [53][54]. The major advantage of a power electronics converter is that a single device can dynamically compensate for a wide frequency range of harmonics.

An active power filter can compensate for different types of distribution system harmonics, such as local load harmonic current, PCC (point of common coupling) harmonic voltage, and resonance aggregated in the long feeders. In this section, the control schemes of active power filters under various situations are reviewed.

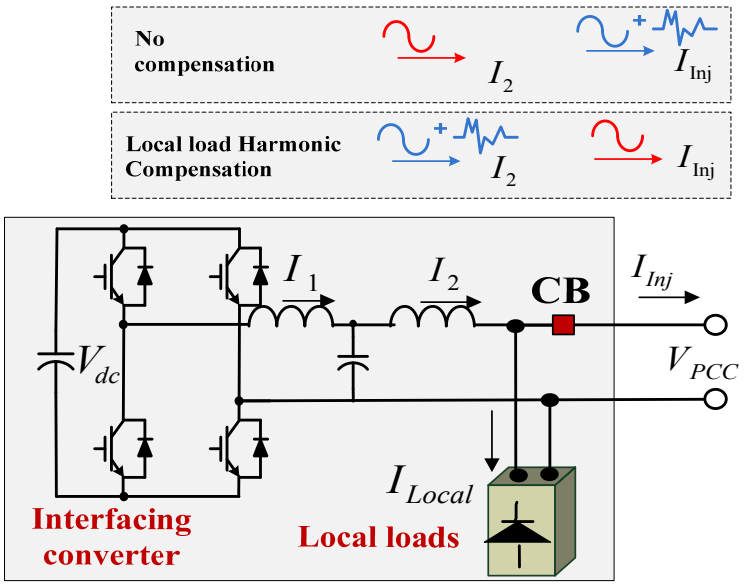

Fig. 1. 7. Simplified diagram of an interfacing converter with a local nonlinear load.

1.2.1 Local load harmonic current compensation

Fig. 1. 7 shows a diagram of an interfacing converter with a local nonlinear load, where the nonlinear local load is connected to the output terminal of the LCL filter. In a conventional interfacing converter without harmonic compensation, the line current I_2 is sinusoidal. In this case, the harmonic current of the local load flows to the main grid side and the injected current I_{inj} is distorted. To reduce the harmonic distortions in I_{inj}, the local load harmonic current can be absorbed by the interfacing converter. To realize this task, an accurate detection of the local load harmonic current and a rapid tracking of the harmonic current reference in the interfacing converter are important.

Fig. 1. 8 shows a diagram of the local load harmonic compensation scheme in an interfacing converter. First, the local load current is measured and the harmonic component is detected by a digital filter. Various types of digital filters have been proposed such as the Fourier transformation based detection method in

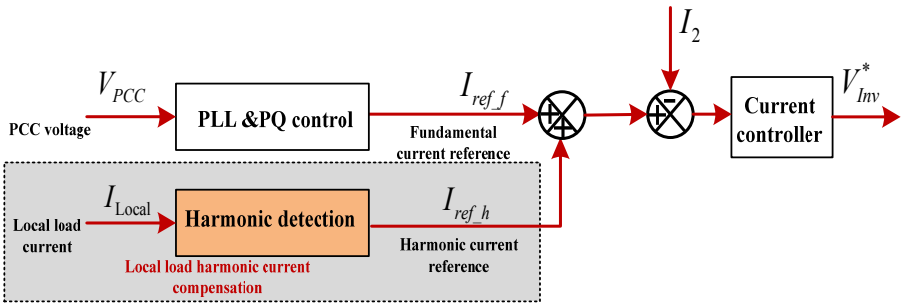

Fig. 1. 8. Control schemes of an interfacing converter with local nonlinear load compensation.

[74], a detection scheme using instantaneous real and reactive power theory in [75], a second-order generalized integrator (SOGI) in [76], and a delayed signal cancellation based detection method in [77].

In the inner current tracking loop, the local load harmonic current component is used as a reference (I_{ref_h}). Wide bandwidth controllers such as proportional and multiple resonant controllers, a deadbeat controller, etc., can ensure rapid current tracking. Compared to the conventional DG unit interfacing converter with limited current control bandwidth, the adoption of harmonic detection and the modification of current tracking loop bandwidth can increase the computational load of a DG unit microcontroller. For a DG interfacing converter with limited computational ability, these modifications might be unacceptable. Therefore, a key research objective for DG based distribution system harmonic compensation is to improve the programming efficiency in the DG unit microcontroller.

In addition, DG real and reactive power control performances should not be affected by the harmonic compensation schemes. To satisfy this requirement, the fundamental interfacing current reference (I_{ref_f}) should be calculated according to power references. Conventionally, the fundamental current reference can be determined based on the assumption of ripple-free grid voltage with fixed magnitude, and the phased locked loop (PLL) is used to synchronize the

fundamental current reference with the main grid. However, considering that the PCC voltage magnitude often varies due to power flow fluctuations in the distribution system [25], this method may cause nontrivial power control errors. In addition, for an interfacing converter with ancillary harmonic compensation capability, the interactions between distorted converter output current and PCC harmonic voltages may contribute some real and reactive power bias, and the power bias cannot be directly addressed using the conventional open loop power control method [81]. To ensure accurate power tracking performance, closed-loop DG power control is necessary.

1.2.2 Distribution system voltage harmonic compensation

In addition to local load harmonic compensation, a power electronics interfacing converter is also utilized to actively improve the voltage quality of a power distribution system via harmonic voltage detection.

For instance, a diagram of a simple distribution system with two parallel interfacing converters is shown in Fig. 1. 9, where two interfacing converters are connected to PCC with feeders and LCL filters. The PCC is connected to the main utility with the main grid feeder and an isolation transformer. Conventionally, the DG unit current is sinusoidal and the PCC nonlinear load current flows to the main grid side. Accordingly, the harmonic voltage drop on the main grid feeder causes significant harmonic voltage distortion at the PCC. In this system, the measurement of PCC load current is difficult due to the distributed nature of nonlinear loads. Alternatively, the harmonic voltage at the PCC is extracted to control the DG unit as a small damping resistor at selected harmonic frequencies [82]. As the small resistor provides a path for the flow of load harmonic current, this method can indirectly improve the quality of the PCC voltage.

A control diagram of PCC harmonic voltage compensation is shown in Fig. 1. 10. Except for the harmonic current reference generation block, the control diagram in Fig. 1. 10 is similar to the scenario in Fig. 1. 8 that shows local load

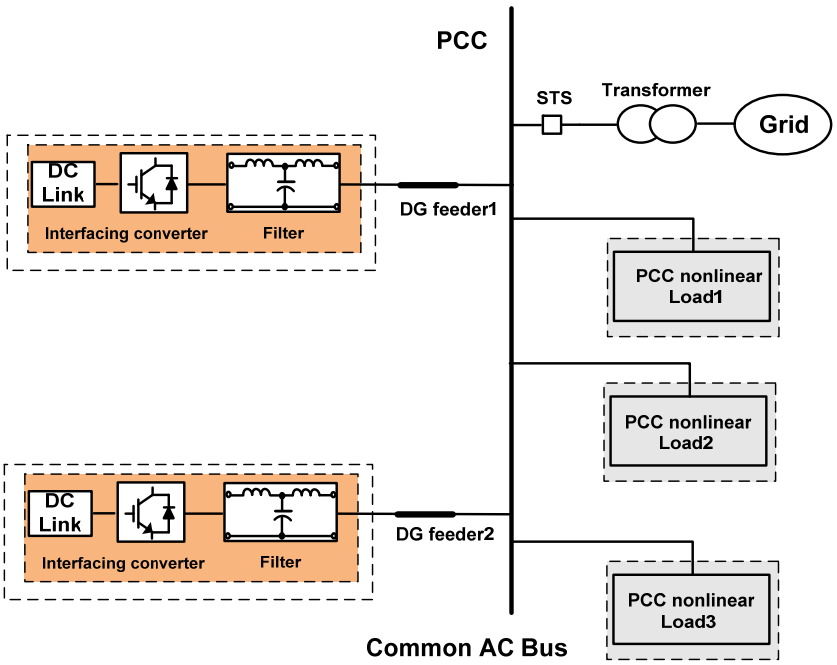

Fig. 1. 9. Two DG units with a PCC harmonic voltage compensation service.

harmonic compensation. When a DG unit is adopted to compensate PCC voltage distortion, the harmonic current reference is obtained as the PCC harmonic voltage (V_{PCC_h}) multiples by a gain ($-1/R_V$). Accordingly, the interfacing converter behaves as a damping resistor (R_V) at selected harmonic frequencies.

When multiple DG units are used in the distribution system, the harmonics compensation task should be properly shared among DG systems according to

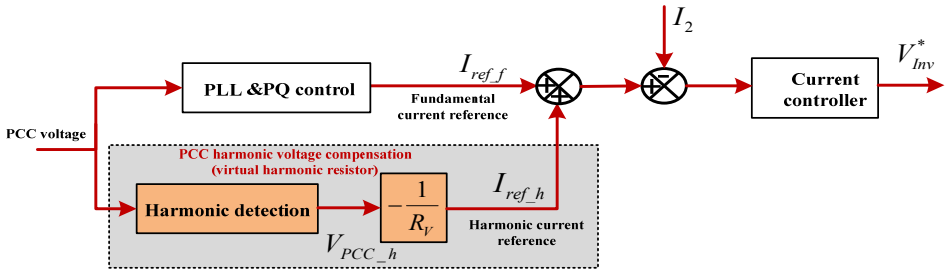

Fig. 1. 10. PCC harmonic compensation using a virtual harmonic resistor.

their available power ratings. As the harmonic voltage detection based compensation method controls the entire DG unit as a virtual damping resistor, the PCC load harmonic current is automatically shared in reverse proportion to the DG virtual resistance [84].

1.2.3 Voltage controlled power system harmonic issues

The growing penetration of distributed energy resources has inspired the control of DG unit interfaces to emulate the operation of a synchronous generator through voltage regulation [87][88][100]. Compared to current controlled methods, voltage control schemes can effectively address the challenges of islanding operations, as the system voltage support is provided by DG unit interfacing converters.

A diagram of a distribution system with two voltage controlled DG units is shown in Fig. 1. 11. In this system, the DG unit output LC filter capacitor voltage (V_C) is controlled to be sinusoidal. The control schemes of these DG units are shown in the lower part of Fig. 1. 11. First, in the power control loop, real power-frequency droop and reactive power-voltage magnitude droop control methods are used to share the load demand among multiple parallel DG units. In the inner loop, a voltage controller is used to ensure high performance DG filter capacitor voltage tracking. When the voltage control method is used for both grid-connected and islanding operations, the transition between them is very smooth. Due to this feature, a voltage controlled DG unit is often preferred for dual-mode microgrid applications, where the transfer between grid-connected and islanding operations is required to improve the reliability and efficiency of the microgrid.

Compared to a current controlled grid-connected system, a voltage controlled system is more sensitive to the disturbance from nonlinear loads. This is mainly because voltage controlled DG units are not capable of realizing closed-loop control of DG line current. When the DG capacitor voltage is controlled to be ripple-free, the DG unit can be modeled as a short circuit connection at low order harmonic frequencies [50]. Accordingly, the PCC load harmonic current is

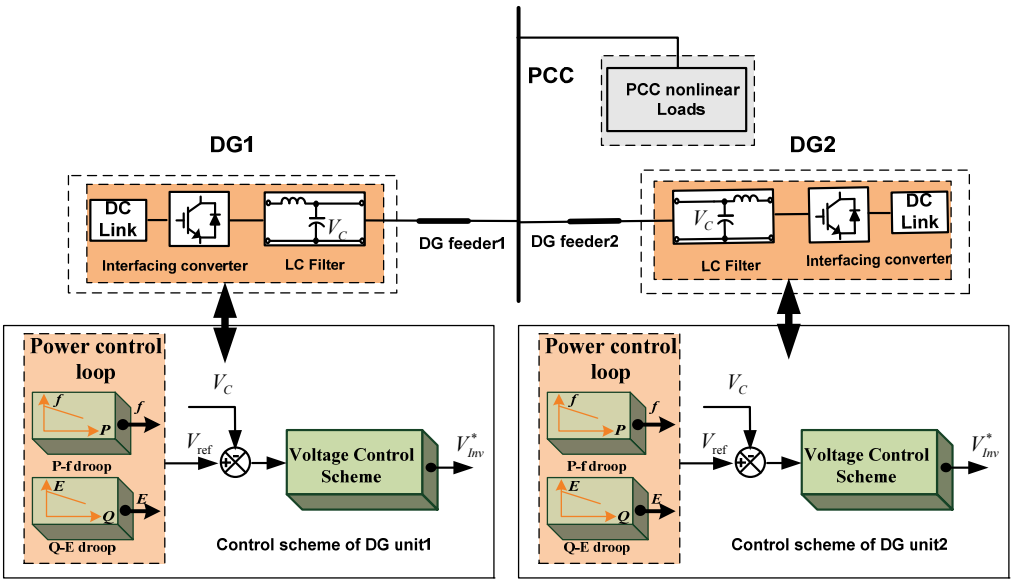

Fig. 1. 11. Distribution system with voltage controlled DG units.

passively shared by DG units, according to their existing feeder harmonic impedance values. Therefore, DG units with smaller feeder harmonic impedance absorb more harmonic load current, which may cause over-current protection in the DG units.

1.3. Research objectives and thesis layout

To reduce power distribution system harmonics, a comprehensive study of DG unit interfacing converter control is conducted in this thesis. The research aims to actively mitigate the resonance in both single DG unit and multiple parallel DG units. Flexible control of interfacing converters to compensate for different types of harmonics in the power distribution system is developed and discussed.

Several DG interfacing converter control schemes are developed to address harmonic pollution. The first control scheme can accurately track converter control reference, and at the same time actively dampen the resonance in interfacing converter output filters. In addition, an accurate model for parallel grid-tied inverters is established and the effectiveness of conventional damping

methods for single inverters is verified in the case of multiple inverters. Finally, power distribution system harmonic compensation methods using flexible control of interfacing converters are proposed. They can reduce the computing load in the DG unit digital controller, and some of them can also be directly used for autonomous islanding microgrid applications. A summary of the research objectives addressed in each chapter is listed here.

Chapter 2

The impact of existing control schemes on single inverter filter resonance is investigated in this chapter. First, the internal mode principle based single-closed-loop control and double-closed-loop control are reviewed. The model-based deadbeat current control is also discussed. To simplify the control parameter design, a generalized closed-loop controller (GCC) is proposed. The proposed controller controls an internal virtual impedance to compensate resonance in inverter output filters. Additionally, a virtual impedance based active damping method is embedded in the conventional deadbeat control scheme. The proposed revised deadbeat control can provide sufficient damping effects to an interfacing converter output filter without sacrificing the rapid dynamic response of the conventional deadbeat control.

Chapter 3

The interactions between coupled grid-connected inverters are studied in Chapter 3. The research indicates that the harmonic current in the interfacing converter is not determined only by its own filter circuit and the control scheme. Couplings between parallel interfacing converters at the PCC bring additional frequency-varying resonance to each interfacing's line current. To investigate this frequency varying resonance, an accurate equivalent circuit model considering interactions between multiple inverters is established and the active damping methods designed for single inverters are verified in the case of multiple parallel inverters.

Chapter 4

To address the impacts of increasingly installed nonlinear loads in the modern power distribution system, the multifunctional DG unit is discussed in this chapter. Considering that both current control and voltage control methods can be applied to DG unit interfacing converters, corresponding compensation methods are developed. The proposed current controlled method (CCM) scheme features a very simple structure to improve the efficiency of microcontroller programming. As the islanding operation of the DG system has been receiving increasing attention in recent years, a voltage controlled method (VCM) based harmonic compensation is proposed in this chapter. Compared to the conventional VCM based DG unit without any closed-loop line harmonic current tracking capability, this proposed method can improve the voltage quality at the PCC using a simple feed-forward term.

Chapter 5

Further improvements in the harmonic compensation performance of power distribution systems are discussed in this chapter. A flexible hybrid control method (HCM) with three well decoupled control terms is proposed to address different harmonic issues in the power distribution system. To improve interfacing converter harmonic compensation performance when the main grid has some frequency deviations, a simple frequency adaptive control without a frequency estimator is proposed.

Chapter 6

The conclusions of the research are presented in this chapter and a suggested future research is also presented.

Chapter 2

Interfacing Converter Control and Active Damping

Resonances caused by converter output filters and the interactions between multiple DG units often challenge the control of interfacing converter line current. Considering the study of interactions between multiple inverters is dependent on the knowledge of single inverter model, this chapter focuses on the modeling and damping of the single inverter system. A few well accepted current control methods, including single-loop control and double-loop control, which are developed based on internal mode principle, and the model-based deadbeat control, are investigated regarding their sensitivity to output LCL or LC filter resonance. The concept of virtual impedance is used to simplify the design, implementation, and comparison of interfacing converter controller schemes. First, a generalized closed-loop control (GCC) scheme with inherent virtual impedance is proposed. In addition, this chapter extends the concept of virtual impedance from GCC to the deadbeat control that is traditionally developed without any damping effects to filter resonance. Investigations and comprehensive verification results in this chapter prove that virtual impedance based active damping control is a good candidate to improve the line current quality of grid-connected DG units.

Publications out of this chapter:

(1) J. He and Y. W. Li, "Generalized Closed-Loop Control (GCC) Schemes with Embedded Virtual Impedances for Voltage Source Converters with LC or LCL Filters," IEEE Transactions on Power Electronics, vol. 27, pp. 1850-1861, Apr. 2012.

2.1. Single-loop control scheme

First, a single-phase interfacing converter with an LCL filter is shown in Fig. 2. 1. To realize grid synchronization, PCC voltage is measured and the voltage angle phase is detected by a phase-locked-loop (PLL). Considering that this chapter is focused on the performance of single inverter system, it is assumed that the PCC is connected to an infinite bus. In a single-loop control system, either the inverter output current I_1 or the inverter line current I_2 can be measured as the feedback.

In recent years, the proportional and resonant (PR) controllers in stationary reference frame are proposed to replace the traditional PI controller in the synchronous rotating reference frame [43][44]. According to the internal mode principle, the PR controller at the stationary reference frame has the capability to track AC signal with zero steady-state errors, and the current control performance can be less sensitive to parameter variations. Furthermore, multiple parallel harmonic resonant controllers [45][46] can also be used in the current control scheme to provide better harmonic rejection capability at characteristic harmonic orders, such as 5th and 7th harmonics. The transfer function of a PR current controller is given as

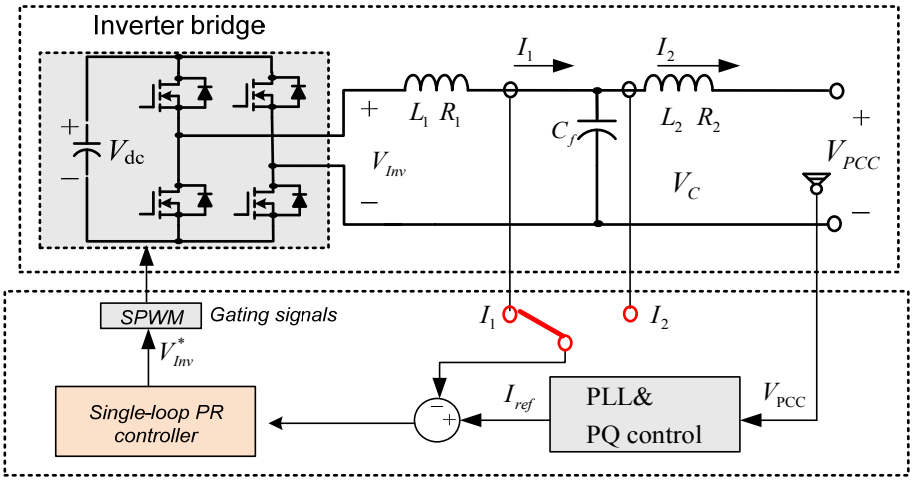

Fig. 2. 1. Diagram of a single-loop current controlled interfacing converter.

$$G_{\mathrm{Cur}}(s) = k_P + \sum_h R_{\mathrm{h}}(s) = k_P + \sum_h \frac{2k_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_h^2} \tag{2-1}$$

where k_p is the proportional gain, R_h is the resonant controller at the order h, k_{ih} is the resonant controller gain at the order h, ω_h is the resonant angular frequency at the order h, and ω_{ch} is the cut-off frequency of the resonant controller.

With a PR controller at stationary reference frame, a single-phase and a three-phase inverter control can be realized in a similar manner, without involving any reference frame transformations. Since a three-phase three-wire system can be modeled in the stationary two-axis reference frame without cross coupling, the findings and conclusions from single-phase system are also valid for three-phase three-wire system.

2.1.1. Single-loop control with inverter output current I_1 feedback

To provide over-current protection, the inverter output current feedback I_1 is preferred. In this case, the current flowing to the LCL filter capacitor bank needs to be compensated, in order to ensure high power factor operation of the DG unit. When the current controller as shown $G_{cur}(s)$ in (2-1) is used, the reference inverter output voltage V_{Inv}^* is described as

$$V_{Inv}^* = G_{Cur}(s) \cdot (I_{ref} - I_1) \tag{2-2}$$

where I_{ref} is the reference current of the interfacing converter, $G_{Cur}(s)$ is the single-loop current controller.

Fig. 2. 2 shows the detailed information of an LCL filter. The response is given as

$$I_1 = H_1(s) \cdot V_{Inv} + H_2(s) \cdot V_{PCC} \tag{2-3}$$

$$I_2 = H_3(s) \cdot V_{Inv} + H_4(s) \cdot V_{PCC} \tag{2-4}$$

where V_{PCC} is the PCC voltage as shown Fig. 2. 1 and V_{Inv} is the average inverter output voltage. The gains $H_1(s)$ to $H_4(s)$ are listed as

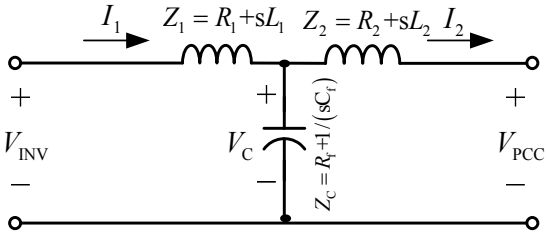

Fig. 2. 2. An LCL filter interfaced to PCC.

$$H_1(s)=\frac{z_2+z_C}{z_1\cdot z_2+z_1\cdot z_C+z_2\cdot z_C},$$

$$H_2(s)=\frac{-z_C}{z_1\cdot z_2+z_1\cdot z_C+z_2\cdot z_C},$$

$$H_3(s)=\frac{z_C}{z_1\cdot z_2+z_1\cdot z_C+z_2\cdot z_C},$$

and $H_4(s)=\frac{-(z_1+z_C)}{z_1\cdot z_2+z_1\cdot z_C+z_2\cdot z_C}$.

The coefficients in $H_1(s)$ to $H_4(s)$ are given as $Z_1 = sL_1 + R_1, Z_2 = sL_2 + R_2,$ and $Z_c = 1/(sC_f) + R_c,$ where L_1 and R_1 are inverter side choke inductance and its stray resistance, L_2 and R_2 are line side choke inductance and its stray resistance. C_f is the filter capacitance. R_c is the damping resistance placed in series with the filter capacitor.

By solving the equations (2-2) to (2-4), and assuming $V_{Inv}^* = V_{Inv}$, the inverter line current response can be described as shown in (2-5)

$$I_2 = G_{eq}(s)\cdot I_{ref} - Y_{eq}(s)\cdot V_{PCC} \tag{2-5}$$

where $G_{eq}(s)$ is the closed-loop gain of the current source and $Y_{eq}(s)$ is the shunt admittance of the current source circuit. Their detailed expressions are shown as

$$G_{eq}(s)=\frac{H_3(s)\cdot G_{Cur}(s)}{1+H_1(s)\cdot G_{Cur}(s)} \tag{2-6}$$

$$Y_{eq}(s)=\frac{G_{Cur}(s)\cdot H_2(s)\cdot H_3(s)}{1+H_1(s)\cdot G_{Cur}(s)}-H_4(s) \quad (2\text{-}7)$$

With (2-5), the line current response of this interfacing inverter can also be represented by using a Norton equivalent circuit as shown in Fig. 2. 3.

For a single-phase converter with the circuit and control parameters as listed in TABLE. 2. 1 (with inverter output current feedback), the closed-loop response of the inverter is given in Fig. 2. 4 and Fig. 2. 5. First, it can be seen from Fig. 2. 4 that reference current to inverter line current ($G_{eq}(s)$) has a resonant peak at around 1050Hz. This resonant frequency is mainly determined by the parameters of the inverter LCL filter. In addition, the line current response caused by PCC voltage disturbance ($Y_{eq}(s)$) is illustrated in Fig. 2. 3. It shows that the frequency

Fig. 2. 3. Equivalent circuit of a current controlled DG interfacing converter.

TABLE. 2. 1. Parameters of a single-phase 120V/1KVA converter with single-loop current control.

Parameters	Symbols	Values
Circuit Parameter		
Inverter side inductor	L_1 , R_1	2.1mH (0.092pu), 0.05Ω (0.003pu)
Filter capacitor	C_f , R_C	10uF (0.050pu), 0.25Ω (0.015pu)
Line side inductor	L_2 , R_2	1.3mH (0.057pu), 0.05Ω (0.003pu)
Control Parameter (single-loop with output current feedback)		
Switching frequency	12.0kHz	
PR controller proportional	$k_p = 20$ $k_{if} = k_{i3} = k_{i5} = k_{i7} = 40000$ $k_{i9} = k_{i11} = 30000$ $k_{i13} = k_{i15} = 20000$	
Control Parameter (single-loop with line current feedback)		
Switching frequency	12.0kHz	
PR controller proportional	$k_{\mathrm{p}} = 1.05$ $k_{\mathrm{if}} = 140$	

domain response has a resonance at around 1050Hz, which is the same as the resonance frequency in Fig. 2. 4.

2.1.2. Single-loop control with inverter line current I_2 feedback

Similar to the case of using inverter output current as the feedback, the line current I_2 can also be sensed to realize closed-loop current control. In this scenario, the inverter reference voltage is revised as

$$V_{Inv}^{*} = G_{Cur}(s) \cdot (I_{ref} - I_{2}) \tag{2-8}$$

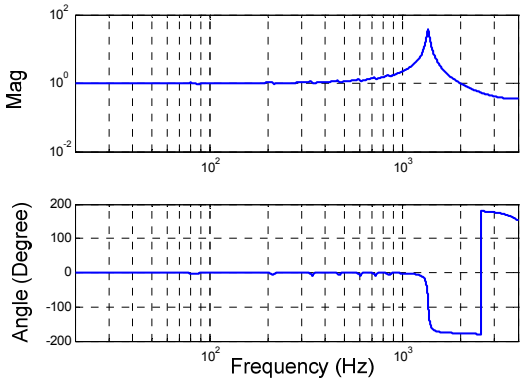

Fig. 2. 4. Closed-loop response of single loop current control with inverter output current I_1 feedback ($G_{eq}(s) = I_2/I_{ref}$).

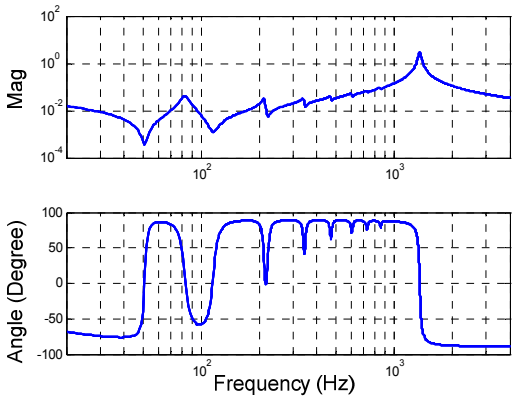

Fig. 2. 5. Closed-loop response of single loop current control with inverter output current I_1 feedback ($Y_{eq}(s) = -I_2/V_{PCC}$).

It is important to note that harmonic resonant controllers are often removed from $G_{Cur}(s)$ in (2-8), mainly due to the reduced stability margin caused by the offset current from filter capacitor branch [33]. With line current feedback and only fundamental frequency resonant controller in $G_{Cur}(s)$, the closed-loop response of line current I_2 can be obtained in a similar way as

$$I_2 = G_{eq}(s) \cdot I_{ref} - Y_{eq}(s) \cdot V_{PCC} \tag{2-9}$$

In this case, the coefficients of $G_{eq}(s)$ and $Y_{eq}(s)$ are expressed as

$$G_{eq}(s) = \frac{H_3(s) \cdot G_{Cur}(s)}{1 + H_3(s) \cdot G_{Cur}(s)} \tag{2-10}$$

$$Y_{eq}(s) = -\frac{H_4(s)}{1 + H_1(s) \cdot G_{Cur}(s)} \tag{2-11}$$

With different closed-loop equivalent circuit coefficients, the performance of the system is also different. This can also be verified by examining the closed-loop response of an inverter in frequency domain. For an inverter with the control and circuit parameters as shown in TABLE. 2. 1 (with line current feedback), the closed-loop response of this system is shown in Fig. 2. 6 and Fig. 2. 7. The frequency domain analysis demonstrates that the response of the inverter using line current feedback has a resonant peak at around 1075 Hz.

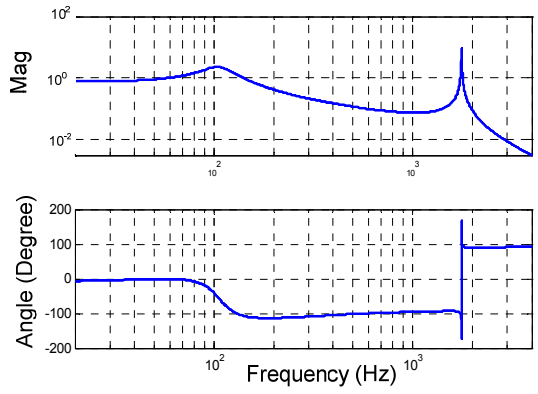

Fig. 2. 6. Closed-loop response of single loop current control with line current I_2 feedback ($G_{eq}(s) = I_2/I_{ref}$).

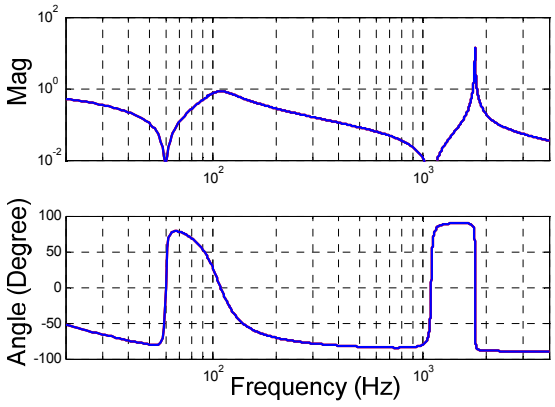

Fig. 2. 7. Closed-loop response of single loop current control with line current I_2 feedback ($Y_{eq}(s) = -I_2/V_{PCC}$).

Based on the discussions, it can be concluded that a conventional single-loop control without active damping cannot mitigate the resonant peak in an LCL filter. To over this limitation, either passive damping or active damping is needed.

2.2. Double-loop control scheme

A double-loop control scheme has been considered as an efficient method to mitigate the resonance of output LCL filters. Fig. 2. 8 shows the control diagram of a grid-connected interfacing converter with double-loop line current control scheme. In the outer control loop, the inverter line current is measured as the feedback and the outer control loop is expressed as

$$I_{Inner}^{*} = G_{Outer}(s)\cdot(I_{ref} - I_2) = (k_P + \sum_h \frac{2k_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_h^2})\cdot(I_{ref} - I_2) \tag{2-12}$$

where the outer loop $G_{Outer}(s)$ consists of a PR controller. In order to ensure good harmonic rejection capability, the harmonic resonant controllers can be used in (2-12). I_{Inner}^{*} is the output of outer control loop.

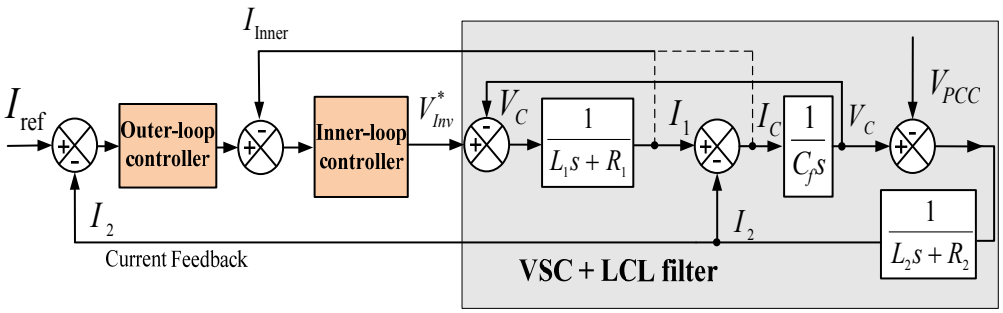

Fig. 2. 8. Double-loop control diagram for current-controlled interfacing converter with an LCL filter.

In the inner control loop, either the inverter output current I_1 or the LCL filter capacitor current I_c can be used as feedback, and the proportional control is normally used as

$$V^*_{Inv} = G_{Inner}(s) \cdot (I^*_{Inner} - I_{Inner}) = k_{Inner} \cdot (I^*_{Inner} - I_{Inner}) \quad (2\text{-}13)$$

where V^*_{Inv} is the reference voltage for PWM modulation, $G_{Inner}(s)$ is the inner loop proportional controller with the gain k_{Inner}.

Although this chapter is focused on the performance of grid-tied converter with current control, it is necessary to point out that similar double-loop control can also be used for islanding interfacing converter with voltage control. In this case, the interfacing converter often adopts an LC filter and the filter capacitor voltage is controlled to provide direct voltage support to the autonomous load. The outer loop of a voltage controller is shown in (2-14) as

$$I^*_{Inner} = G_{Outer}(s) \cdot (V_{ref} - V_C) = (k_P + \sum_h \frac{2k_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_h^2}) \cdot (V_{ref} - V_C) \quad (2\text{-}14)$$

where V_{ref} is the reference voltage and V_C is the measured LC filter capacitor voltage.

For a voltage controlled interfacing converter, the inner loop is the same as the inner loop of a current controlled interfacing converter as shown in (2-13).

Similarly, either inverter output current I_1 or LC filter capacitor current I_c can be used as the inner loop feedback.

Compared to the damping techniques using high order controllers, such as PR controller with lead-leg compensator in [33][47], double-loop controller involves more feedbacks and control variables. Accordingly, the controller parameter tuning is difficult. One parameter tuning approach is to assume that the dynamics of the inner-loop is much faster than the outer-loop [48]. As a result, outer and inner control loops are decoupled and their parameters can be tuned through an iterative process [49]. However, this iterative method is complicated and the outer- and inner-loop parameters cannot be determined together. Alternatively, an interesting design method through pole-zero placement is reported in [34]. In this method, high order outer-loop controller is approximated as a PI controller during parameter design stage. Therefore, accurate effects of the outer-loop controller can hardly be examined.

The selection of inner-loop feedback is also important for double-loop controllers. Some analysis of the system performance regarding different feedback variables can be found in [50].

2.3. Generalized closed-loop control scheme

The virtual impedance based active damping using additional measurement has been discussed in recent literature. For instance, the inverter output current or capacitor current can be measured to realize the virtual impedance control. This makes the system feedback variable as same as that in double-loop control. However, what essentially makes the double-loop control similar to virtual impedance control has not been understood in a more intuitive way.

Motivated by aforementioned factors, this section proposes a generalized closed-loop control (GCC) scheme, which incorporates an interfacing converter closed-loop control term, an internal virtual impedance term and an external virtual impedance term into a parallel control structure. Unlike the conventional

cascaded double-loop control, the effects of the internal virtual impedance control term is to add a virtual damping impedance to the output filter circuit, which ensures a well dampened filter plant at first. Therefore, the closed-loop control term in GCC can provide satisfactory tracking control based on the modified filter plant. In addition, with distinct physical meaning of the internal impedance term, the feedback variable selection and the parameter design of GCC scheme can be achieved in a more intuitive way. Furthermore, the external impedance in the GCC scheme is very flexible and it can be implemented to facilitate the control of active power filters and interfacing converter closed-loop series impedance, without modifying the original control references as in the conventional methods*.

2.3.1. GCC scheme structure

First, the diagram of GCC scheme is shown in (2-15). When the external

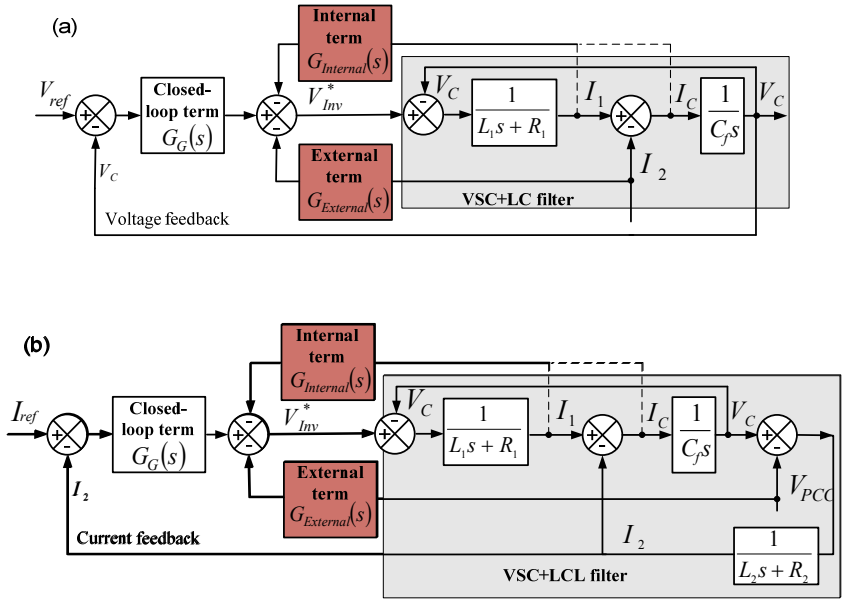

Fig. 2. 9. Proposed GCC scheme: (a) Voltage-controlled interfacing converter with an LC filter. (b) Current-controlled interfacing converter with an LCL filter.

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*Note that the external impedance in the GCC scheme is not discussed here, as it is not directly related to the damping of filter resonance. The detailed discussion on external virtual impedance can be found in "Generalized Closed-Loop Control (GCC) Schemes with Embedded Virtual Impedances for Voltage Source Converters with LC or LCL Filters," IEEE Transactions on Power Electronics, vol. 27, pp. 1850-1861, Apr. 2012.

impedance term is not included, the GCC scheme contains a closed-loop control of the reference and an embedded virtual impedance term (internal impedance)

$$V_{Inv}^{*} = G_G(s)\cdot\left(x_{\mathrm{G,ref}} - x_G\right) - G_{Internal}(s)\cdot x_{internal} \tag{2-15}$$

where $G_G(s)$ is the closed-loop reference tracking controller in GCC and $G_{Internal}(s)$ is the control term for the internal virtual impedance. $x_{G,ref}$ and x_G are the control reference and the measured feedback (such as capacitor voltage V_C or line current I_2, see Fig. 2. 9). $x_{Internal}$ is the selected variable (such as inverter output current I_1 or capacitor current I_C) for internal impedance control.

In the GCC scheme, the closed-loop term is used for reference tracking, which has similar function as the single-loop control. The internal impedance is mainly used to provide sufficient damping to the filter plant. By flexible control of the internal impedance term, the GCC scheme can easily achieve similar performance compared to multi-loop control scheme. In addition, the selection of internal impedance term feedback variable and the control parameter design can be more straightforward and robust.

2.3.2. Internal virtual impedance control

For the GCC scheme, it is very easy to realize the traditional single-loop control by removing the internal virtual impedance control term from (2-15) (corresponding to $G_{Internal}(s) = 0$).

To establish the connection between GCC scheme and conventional double-loop control, the double-loop controller in voltage controlled interfacing converter is revisited as

$$I_{\mathrm{Inner}}^{*} = G_{\mathrm{Outer}}(s)\cdot\left(V_{\mathrm{ref}} - V_{\mathrm{C}}\right) \tag{2-16}$$

$$V_{Inv}^{*} = G_{Inner}(s)\cdot\left(I_{Inner}^{*} - I_{Inner}\right) \tag{2-17}$$

where $G_{Outer}(s)$ and $G_{Inner}(s)$ are the outer loop and inner loop controller, respectively. V_{ref} and V_C are the reference voltage and feedback filter capacitor voltage. I^*_{Inner} and I_{Inner} are the inner-loop reference and feedback. As mentioned earlier, I_{Inner} can be the inverter output current I_1 or capacitor current I_C.

By merging (2-16) and (2-17) together yields

$$\begin{aligned} V^*_{\text{Inv}} &= G_{Outer}(s)\cdot G_{Inner}(s)\left(V_{ref}-V_C\right)-G_{Inner}(s)\cdot I_{Inner} \\ &= G_G(s)\cdot\left(V_{ref}-V_C\right)-G_{Internal}(s)\cdot I_{Inner} \end{aligned} \tag{2-18}$$

As shown, the double-loop controller is a single-loop control plus an additional control term. Comparing (2-18) to the GCC scheme in (2-15) reveals that the double-loop control is actually a single-loop control and an internal impedance with ($G_G(s) = G_{Outer}(s)G_{Inner}(s)$ and $G_{Internal}(s) = G_{Inner}(s)$). Therefore, it can be concluded that the double-loop control essentially provides active damping through the internal virtual impedance realized by the inner-loop.

However, unlike the traditional double-loop control, the internal virtual impedance control term in the proposed GCC scheme can be more flexibly tuned as the gains of $G_G(s)$ and $G_{Internal}(\mathrm{s})$ are regulated separately without having the constraint of $G_G(s) = G_{Outer}(s)G_{Inner}(s)$ as in the double-loop control scheme. Furthermore, the performance variation of a double-loop controlled system with different inner-loop feedbacks [50] can also be explained by examining the positions and values of their corresponding internal virtual impedance.

By carrying out similar analysis for grid-tied converter with LCL filter, the double-loop current control of an interfacing converter with LCL filter is represented by the GCC scheme using a single-loop control and an additional internal impedance term as shown in (2-19)

$$\begin{aligned} V^*_{Inv} &= G_{Outer}(s)\cdot G_{Inner}(s)\left(I_{ref}-I_2\right)-G_{Inner}(s)\cdot I_{Inner} \\ &= G_G(s)\cdot\left(I_{\text{ref}}-I_2\right)-G_{Internal}(s)\cdot I_{Inner} \end{aligned} \tag{2-19}$$

where I_{ref} and I_2 are the reference current and interfacing converter line current, respectively. Similarly, the closed-loop control performance difference with

different inner-loop feedbacks is related to the position and value of the internal virtual impedance.

2.3.3. Positions of internal virtual impedance

As discussed earlier, the internal virtual impedance in the GCC scheme helps to provide active damping to the interfacing inverter system. This function is similar to the physical damping resistor that addresses the resonance problems of LC and LCL filters [55][56]. Further considering the internal impedance control term takes effect in an open-loop manner (without closed-loop control) and it adjusts the inverter output voltage reference directly, its associated bandwidth is sufficient to address the LC or LCL filter resonance as long as the inverter switching frequency is much higher than the filter resonant frequency. To simplify the discussion here, the closed-loop control term is defined as V_{Inv_R} as

$$V_{Inv\_R} = G_{\mathrm{G}}(s) \cdot \left(x_{\mathrm{G,ref}} - x_{\mathrm{G}}\right) \tag{2-20}$$

Due to the limited gain of the closed-loop control at harmonic frequency, the internal impedance term $G_{Internal}(s) \cdot x_{Internal}$ is considered as the dominant term around the resonant frequency, which is typically much higher than the fundamental frequency. As a result, the system damping performance is regulated by this internal virtual impedance term.

First, when the inverter output current I_1 is selected as the internal term feedback, the effect of the internal impedance term is to introduce an additional voltage drop at the inverter output voltage reference. Without considering the delay of voltage modulation, this equals to place a series internal virtual impedance $Z_{VI}(s) = G_{Internal}(\mathrm{s})$ at the converter side inductor as shown in Fig. 2. 10(a) and (b). In this figure, the filter input voltage V_{Inv_R} is described in (2-20). It is obvious that if a proportional controller is used in $G_{Internal}(s)$, the internal impedance is just a damping resistor. Moreover, with the proposed GCC scheme, complex impedance can also be realized by selecting the desired $G_{Internal}(\mathrm{s})$.

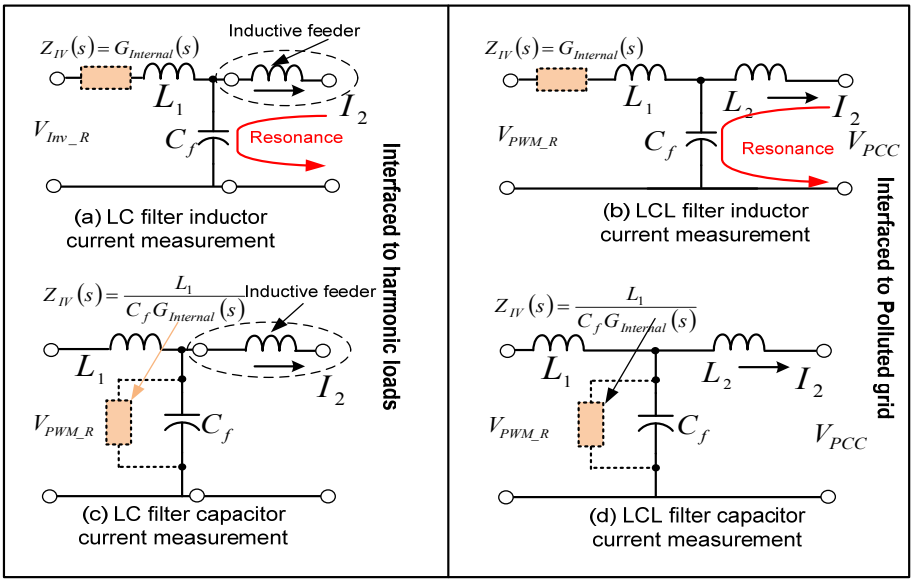


Fig. 2. 10. Illustration of internal virtual impedance with different feedbacks.

Alternatively, when the capacitor current is selected as the internal impedance feedback variable, its physical meaning is not obvious. This is because the modification of inverter output voltage reference cannot be directly associated with the internal virtual circuit at the filter capacitor branch, due to the presence of converter side filter inductor. However, the effect of internal impedance term on the filter capacitor branch can be established indirectly. Without implementing the internal impedance control term, the line/load harmonic current I_2 is determined as (parasite resistors of filter inductors are neglected here)

$$I_2 = I_1 - I_c = -\left(sC_f V_C + \frac{V_C}{sL_1} \right) \tag{2-21}$$

When the internal impedance term is added, the harmonic current in (2-21) needs to be modified as shown in (2-22)

$$\begin{aligned} I_{2,IV} &= I_{1,IV} - I_C = -\left(\frac{V_C - G_{Internal}(s) I_C}{sL_1} + sC_f V_C \right) \\ &= -\left(\frac{V_C}{sL_1} + sC_f V_C + \frac{G_{Internal}(s) I_C}{sL_1} \right) \end{aligned} \tag{2-22}$$

From (2-22), it can be noticed that the internal virtual impedance control term brings an additional term to line/load current. The impact of this term can be accurately modeled as shunt impedance in parallel with the filter capacitor as

$$Z_{IV}(s)=\frac{V_C}{-(I_{2,IV}-I_2)}=\frac{sL_1V_C}{G_{Internal}(s)I_C}=\frac{L_1}{C_fG_{Internal}(s)} \tag{2-23}$$

This equivalent internal impedance in parallel with the filter capacitor is shown in Fig. 2. 10(c) and (d).

Based on the above discussions, the physical meaning of the internal impedance control term with different feedbacks is clarified. It also reveals that modeling the filter capacitor current feedback control as a series impedance with filter capacitor [55][56] is not accurate, as the effects of filter inductor between the converter and the filter capacitor is not considered.

2.3.4. Analysis and design of GCC control parameters

With distinct physical meaning of the control terms in the GCC scheme, the parameter tuning process can be more straightforward. A line current controlled interfacing converter with LCL filter is presented as an example. It worth mentioning that the proposed parameter design method can also be directly applied to the tuning of double-loop control due to the equivalence between double-loop control and GCC scheme, as discussed in the previous section.

With the proposed GCC scheme, the control parameter tuning can be simplified as the following two steps.

- **Design of the internal virtual impedance**

For the current controlled interfacing converter with an LCL filter, the modified filter plant in Fig. 2. 10(b) and (d) can be described as

$$I_2=H_{1\_GCC}(s)\cdot V_{Inv\_R}-H_{2\_GCC}(s)\cdot V_{PCC} \tag{2-24}$$

where V_{Inv_R} is defined in (2-20). When the inverter output current I_1 is selected as the internal impedance feedback variable, $H_{1\_GCC}(\mathrm{s})$ and $H_{2\_GCC}(\mathrm{s})$ can be expressed as

$$H_{1\_GCC}(s)=\frac{Z_2(s)}{\left(Z_1(s)+Z_{\mathrm{IV}}(s)\right)\left(Z_2(s)+Z_3(s)\right)+Z_2(s)Z_3(s)} \tag{2-25}$$

$$H_{2\_GCC}(s)=\frac{Z_1(s)+Z_{IV}(s)+Z_2(s)}{\left(Z_1(s)+Z_{\mathrm{IV}}(s)\right)\left(Z_2(s)+Z_3(s)\right)+Z_2(s)Z_3(s)} \tag{2-26}$$

where $Z_1(s)=L_1s+R_1$, $Z_2(s)=1/(C_fs)$, and $Z_3(s)=L_2s+R_2$. $Z_{IV}(s)=G_{Internal}(s)$ is the internal impedance connected in series with choke L_1.

It can be seen from Fig. 2. 11 that $H_{2\_GCC}(s)$ has a significant resonance peak when $Z_{IV}(s)$ is 0, and the resonance peak can be dampened by the internal impedance term. However, if a large internal impedance term (such as $G_{Internal}(\mathrm{s})$=100) is added to the plant, an additional resonance can be introduced. This can be explained by the derived equivalent circuit in Fig. 2. 10(b), where large virtual impedance blocks the harmonic current in the converter side of the LCL filter. Therefore, when the grid voltage is polluted, an additional LC resonance might be introduced between C_f and L_2.

On the other hand, a large internal impedance term also decreases the magnitude of $H_{1\_GCC}(\mathrm{s})$ in the low frequency range as shown in Fig. 2. 12. When there is a step change of reference current, the dynamic tracking performance is inevitably affected. With the above considerations, if the output current internal impedance term is desired, a moderate internal impedance term $\mathrm{Z_{IV}(s)}$=25 can be selected.

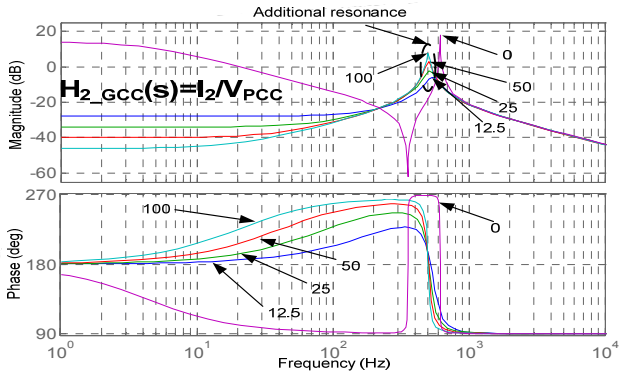


Fig. 2. 11. H_{2_GCC}(s) with the modified LCL filter plant (with inverter output current I_1 based internal impedance)

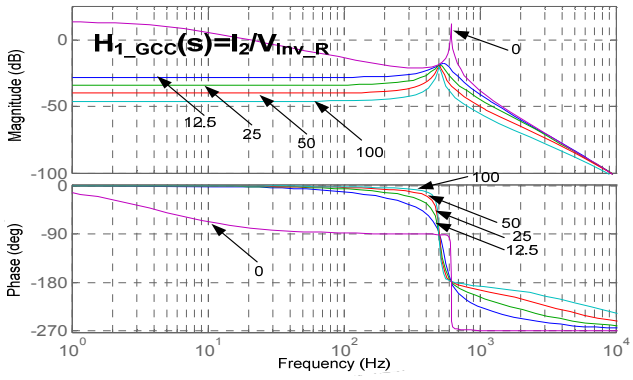


Fig. 2. 12. H_{1_GCC}(s) with the modified LCL filter plant. (with inverter output current I_1 based internal impedance)

When capacitor current I_c is chosen as the internal impedance feedback, parameter design can also be done in a similar manner.

Unlike the internal impedance using inverter output current feedback, when the capacitor current is considered, the filter resonance peak in $H_{2\_GCC}(s)$ is effectively dampened. There is no obvious additional LC resonance even a large damping gain is selected for $G_{Internal}(s)$. However, when the LCL filter is over dampened by a large damping gain $G_{Internal}(s)$, it is equivalent to adding small parallel impedance at the capacitor branch. Considering the small impedance essentially provides a path for grid voltage harmonics, the modified filter plant might be sensitive to low order grid harmonic voltages (such as 2nd) in this situation.

TABLE. 2. 2. Parameters of a three-phase 104V/5KVA interfacing converter with GCC scheme.

3-phase Inverter with LCL filter	Value
Grid voltage (RMS)	104V, 60Hz (3 phase)
LCL filter	L_1 = 4 mH (0.697pu),L_2 = 2.5 mH (0.437pu), C_f= 40μF (0.033pu).
DC Link voltage	260V
DC Link capacitor	2000 μF (1.650pu)
$G_G(s)$	k_p=0.15, k_{if}=25

- **Design of closed-loop tracking term**

After obtaining the dampened filter plant, the closed-loop controller $G_G(s)$ can be designed based on the modified filter plant [57]. Note that when the inverter output current is used as the internal impedance term, the equivalent effect of the modified filter plant is close to a resistor (see the zero phase angle around line frequency in Fig. 2. 12). As a result, conventional assumption in [57] that LCL filter can be simplified as a single equivalent inductor at line frequency is not valid in this case.

Compared to the two-step method in [57], the proposed approach here provides a well dampened LC or LCL filter model at first, and then the closed-loop control term is designed based on the dampened model. Therefore, this design method guarantees a robust system performance with sufficient damping.

Note that although the line current interfacing converter with LCL filter is considered here, the proposed analysis method can also be applied to the voltage controlled interfacing converter with LC filter. Similar conclusions can also be found in voltage controlled system. For instance, when large internal virtual resistance (with inverter output current feedback) blocks the current flow in the choke of the LC filter, additional resonance can also be introduced by the interaction among the filter capacitor and the inductive feeder impedance (see Fig. 2. 10(a)). This phenomenon is actually consistent with the finding in [58], where a

large bandwidth of the inner-loop controller can adversely introduce resonances in a parallel-connected UPS system. In addition, if the internal impedance with capacitor current feedback is implemented with a large proportional gain, the equivalent small parallel impedance can provide a path for the harmonic load current. Accordingly, the distortion of capacitor voltage (with reduced stability margin) is mitigated.

2.4. Deadbeat control scheme

As PR controllers are developed based on the internal mode principle, these closed-loop control methods are less sensitive of parameter variations. However, the dynamic response of PR controller based interfacing converter can hardly be very fast, due the limitation of PR controller gains. On the other hand, the model-based one-step deadbeat control method has also been used in many commercial interfacing converters. The deadbeat controller aims to realize zero tracking error at the end of each switching period [59]-[61]. Therefore, it has very rapid response. Conventionally, the deadbeat current control is mainly used in the situation where interfacing converter is connected to PCC with only a series choke [59]. For the case of high order LCL filter, the deadbeat current control can be used in a similar way. The schematic diagram of the inverter system is presented in Fig. 2. 13. To reduce the number of feedback sensors, the inverter output current I_1 is measured as the current feedback and the filter capacitor voltage V_C is measured for system synchronization.

2.4.1. Principle of deadbeat control

When the conventional discrete-time deadbeat controller is used in the presented inverter system, the output voltage reference is obtained as

$$V_{Inv}^{*}(k) = 1.5V_c(k) - 0.5V_c(k-1) + L_1\frac{I_{ref}(k) - I_1(k)}{T_S} \tag{2-27}$$

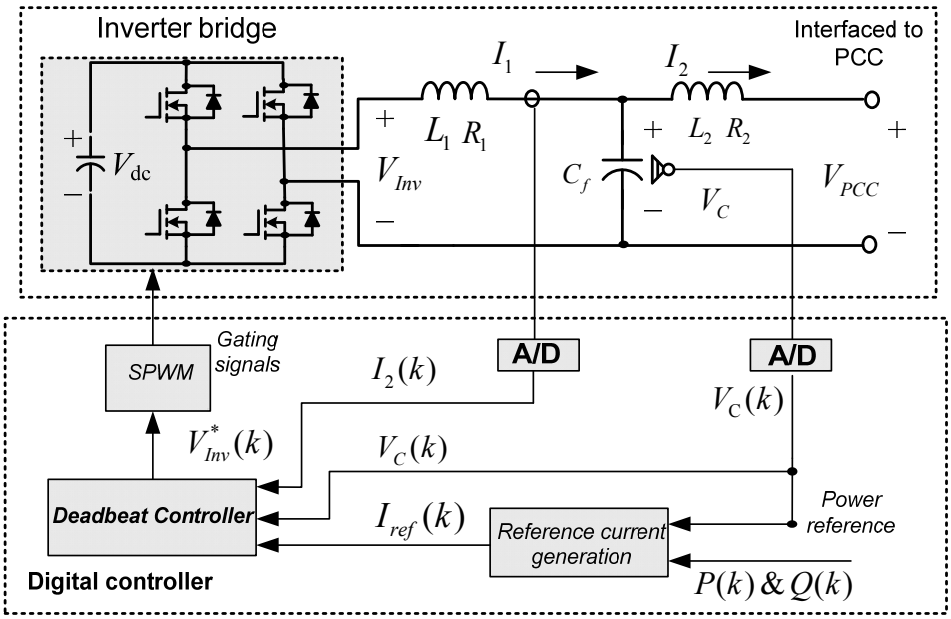


Fig. 2. 13. Conventional deadbeat controlled inverter system.

where T_s is the sampling and switching period and L_1 is the inverter side choke inductance. $V^*_{Inv}(k)$ is the reference voltage of the k^{th} switching period, I_{ref}(k) and I_1(k) are the reference current and the measured inverter output current at the k^{th} switching period. V_c(k) and V_c(k-1) are the measured capacitor voltage at the k^{th} and k-1^{th} switching period, respectively.

- **Closed-loop circuit model using conventional deadbeat control**

This subsection develops the closed-loop current source model of the conventional deadbeat current controlled inverter system. Due to the inherent discrete-time nature of deadbeat controller, the discussion here is based on z-domain models. First, the z-domain transfer functions of an LCL filter plant are obtained as

$$I_1(z) = H_1(z) \cdot V_{Inv}(z) + H_2(z) \cdot V_{PCC}(z) \tag{2-28}$$

$$I_2(z) = H_3(z) \cdot V_{Inv}(z) + H_4(z) \cdot V_{PCC}(z) \tag{2-29}$$

$$V_C(z) = H_5(z) \cdot V_{Inv}(z) + H_6(z) \cdot V_{PCC}(z) \tag{2-30}$$

where $V_{Inv}(z)$ and $V_{PCC}(z)$ are the inverter output voltage and PCC voltage, $I_2(z)$ is the line current. The transfer functions $H_1(z)$ to $H_6(z)$ are determined using bilinear transformation as

$$H_1(z)=Z_{s\to z}\left\{\frac{z2(s)+zc(s)}{z1(s)\cdot z2(s)+z1(s)\cdot zc(s)+z2(s)\cdot zc(s)}\right\} \tag{2-31}$$

$$H_2(z)=Z_{s\to z}\left\{\frac{-zc(s)}{z1(s)\cdot z2(s)+z1(s)\cdot zc(s)+z2(s)\cdot zc(s)}\right\} \tag{2-32}$$

$$H_3(z)=Z_{s\to z}\left\{\frac{zc(s)}{z1(s)\cdot z2(s)+z1(s)\cdot zc(s)+z2(s)\cdot zc(s)}\right\} \tag{2-33}$$

$$H_4(z)=Z_{s\to z}\left\{\frac{-(z1(s)+zc(s))}{z1(s)\cdot z2(s)+z1(s)\cdot zc(s)+z2(s)\cdot zc(s)}\right\} \tag{2-34}$$

$$H_5(z)=Z_{s\to z}\left\{\frac{z2(s)\cdot zc(s)}{z1(s)\cdot z2(s)+z1(s)\cdot zc(s)+z2(s)\cdot zc(s)}\right\} \tag{2-35}$$

$$H_6(z)=Z_{s\to z}\left\{\frac{z1(s)\cdot zc(s)}{z1(s)\cdot z2(s)+z1(s)\cdot zc(s)+z2(s)\cdot zc(s)}\right\} \tag{2-36}$$

Without considering the delay of the PWM voltage modulation ($V_{Inv}(z)=V_{Inv}^{*}(z)$), the closed-loop behavior of an inverter can be obtained in (2-37) through the manipulation on (2-27) to (2-30) as

$$I_2(z)=G_{eq}(z)\cdot I_{ref}(z)-Y_{eq}(z)\cdot V_{PCC}(z) \tag{2-37}$$

where $G_{eq}(z)$ and $(-Y_{eq}(z))$ describe line current responses to the current reference and the PCC voltage, respectively. Their detailed expressions are described as

$$G_{Eq}(z)=\frac{H_1(z)A(z)}{1+H_5(z)B(z)+H_1(z)A(z)} \tag{2-38}$$

$$Y_{Eq}(z)=\frac{H_1(z)H_3(z)A(z)+H_1(z)H_6(z)B(z)}{1+H_5(z)B(z)+H_1(z)A(z)}-H_4(z) \tag{2-39}$$

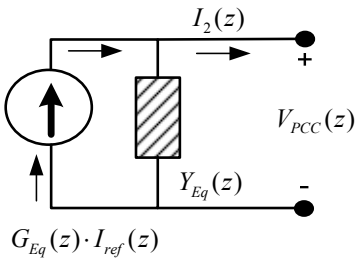


Fig. 2. 14. Closed-loop Norton equivalent circuit of an inverter system.

where the coefficients $A(z)$ and $B(z)$ are expressed as: $A(z) = L_1/T_s$, and $B(z) = 1.5 - 0.5z^{-1}$, respectively.

Fig. 2. 14 illustrates the corresponding Norton equivalent circuit of a single inverter system (2-37), where $G_{eq}(z)$ behaves as the coefficient of the controlled current source and $Y_{eq}(z)$ represents the associated parallel admittance. Note that the closed-loop transfer functions here are expressed in the discretized z-domain. This is because the deadbeat control scheme is developed in the discretized z-domain, and therefore the LCL filter plants are also intentionally discretized in the z-domain for the convenience of analysis.

2.4.2. Proposed active damping scheme for deadbeat current control

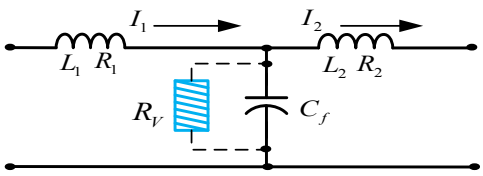
It is necessary to point out that the conventional deadbeat control in (2-27) is typically applicable to an inverter with single choke filter. Accordingly, the LCL resonance problem can be serious in a deadbeat current controlled inverter system [61]. To alleviate the LCL resonance issues, [61] presented an improved deadbeat control method. In this method, both inverter output current and line current measurements are required in the implementation. Also the control accuracy relies on the knowledge of grid impedance. Alternatively, [62] proposed an optimal pole placement method which can be less sensitive to grid impedance uncertainty.

On the other hand, the virtual impedance based active damping method has been applied to a few grid-connected inverters with closed-loop current control, as shown the previous sections. It can be seen that the effectiveness of virtual impedance is less sensitive to the parameter variations. However, the previous virtual impedance control, including the virtual impedance realized by GCC scheme, is effective at both fundamental and harmonic frequencies and the impact at the fundamental frequency can be properly compensated by the closed-loop line current controller [63]. For the deadbeat current controlled inverter with only inverter output current regulation, virtual impedance at the fundament frequency may bring some steady-state line current offset. To overcome this limitation, this section develops a novel harmonic virtual impedance scheme that controls a virtual impedance in parallel with filter capacitor. The developed harmonic virtual impedance does not affect the flow of fundamental current.

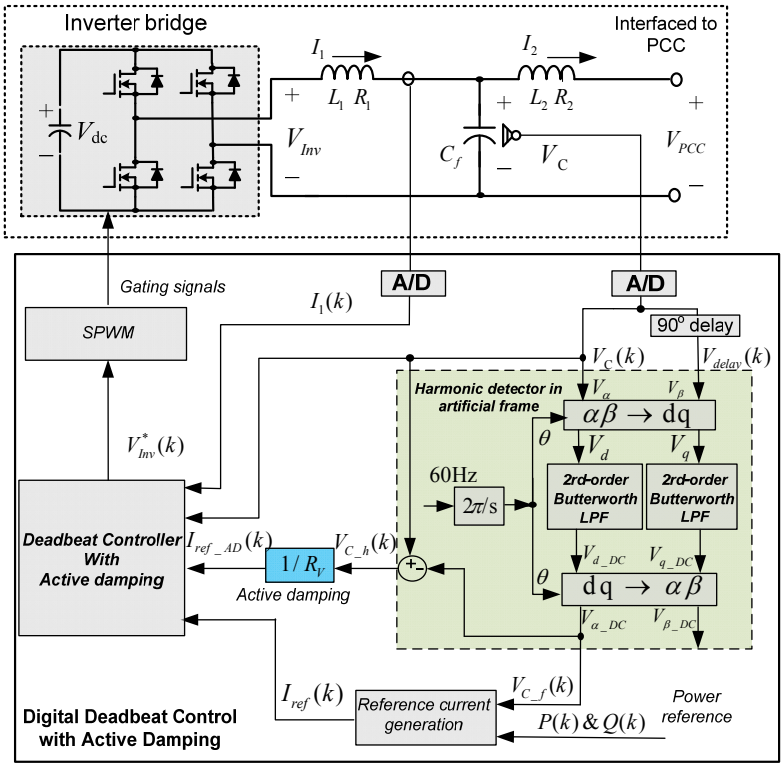
To achieve the virtual damping resistor as shown in Fig. 2. 15 (a), digital implementation scheme is developed as shown in Fig. 2. 15 (b). As shown, the fundamental (V_{c_f}(k)) and the harmonic (V_{c_h}(k)) capacitor voltages are separated using a harmonic detector, which is constructed in the artificial rotating reference frames [64]. For a virtual damping resistance that is effective at the harmonic frequencies, the associated harmonic damping current can be described in the z-domain as

$$I_{ref\_AD} = \frac{V_{C\_h}}{R_{\mathrm{V}}} = \frac{H_{Har}(z) \cdot V_{\mathrm{C}}}{R_{\mathrm{V}}} \tag{2-40}$$

where R_V is the resistance of the virtual damping resistor. $H_{Har}(z)$ is the transfer function of the harmonic detector. The detailed diagram of this harmonic detection process is shown in Fig. 2. 15 (b). For this type of single-phase system, an artificial two-axis rotating reference frame is constructed and the fundamental component is captured by using 2rd-order Butterworth LPFs (15Hz cut-off frequency) in the rotating reference frame [64].



(a) An LCL filter with virtual damping resistor.



(b) Deadbeat scheme with active damping.

Fig. 2. 15. Illustration of single inverter with active damping.

If the active damping current derived in (2-40) is compensated by the regulation of inverter output current I_1, the system response can be similar to the case of using passive damping. Since the bandwidth of deadbeat control is very high, which is also good for harmonic current tracking [60], the damping current in (2-40) can be directly added to the original current reference. With this arrangement, the flow of fundamental current is not affected. The improved deadbeat control is obtained as

$$V^*_{Inv}(k) = 1.5V_c(k) - 0.5V_c(k-1) + L_1 \frac{I_{ref}(k) + I_{ref\_AD}(k) - I_1(k)}{T_S} \qquad (2\text{-}41)$$

After the implementation of the modified controller in (2-41), the deadbeat controller can also provide damping effects to the LCL filter plant.

Compared to many other active damping methods where the resonance mitigation is normally achieved through multi-loop control or redundant measurements, the proposed method does not need any additional current or voltage feedback and it is realized by simple current reference modification. Note that the capacitor voltage measurement is always needed for grid synchronization. Therefore, it is a cost effective method to provide enhanced interfacing converter line current quality.

2.5. Verification results

In order to demonstrate the effectiveness of virtual impedance based active damping method, both simulated and experimental results are obtained in this section.

2.5.1. GCC scheme verification results

First, experiments on a current controlled inverter with LCL system are conducted to verify the performance of the proposed GCC scheme. The controller of this system is developed based on TMS320F2812 DSP and Atmel FPGA. The detailed system parameters are shown in TABLE. 2. 2. In this experiment, 0.4 % 11^{th} and 1% 2^{nd} harmonics are added to the PCC voltage V_{PCC}, and there is no harmonic resonant controller in $G_G(\mathrm{s})$.

As shown in Fig. 2. 16, when a large inductor current internal impedance terms is adopted ($G_{Internal}(\mathrm{s}) = 75$), the line current is distorted (THD=5.58%). Consistent with the previous analysis, a large series virtual resistor through measuring I_1 blocks the harmonic current flow in the converter side filter circuit, and the system becomes sensitive to the resonance between the filter capacitor and grid side inductor.

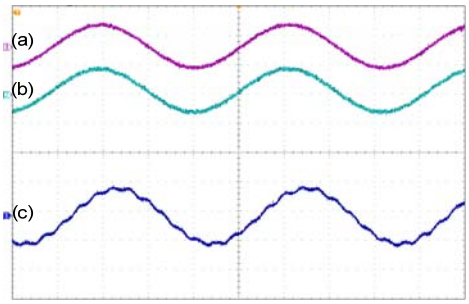


Fig. 2. 16. Current controlled grid interfacing converter with LCL filter. (Inverter output current I_1 based internal virtual impedance) (Over-dampened impedance term with $G_{Internal}(s) = 70$). (a: V_{PCC} (100V/div); b: (V_C 100V/div); c: I_2 (2.5A/div). (**Experiment**)

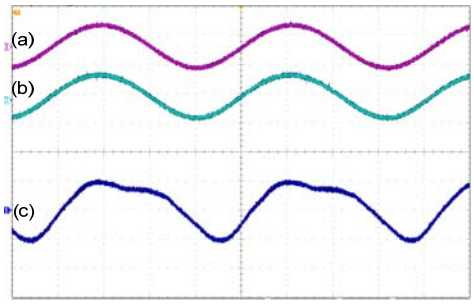


Fig. 2. 17. Current controlled grid interfacing converter with LCL filter. (Capacitor current I_{C} based internal virtual impedance). (Over-dampened impedance term with $G_{Internal}(s) = 110$). (a: V_{PCC} (100V/d); b: (V_C 100V/div); c: I_2 (2.5A/div). (**Experiment**)

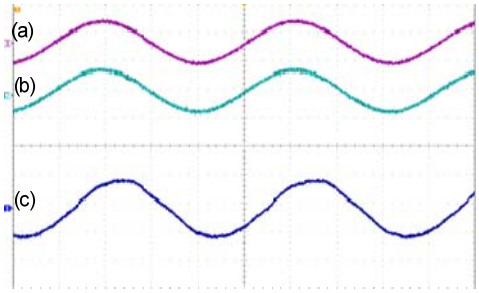


Fig. 2. 18. Current-controlled grid-connected interfacing converter with LCL filter. (capacitor current I_{C} based internal virtual impedance). Internal impedance term with $G_{Internal}(s) = 25$. (a: V_{PCC} (100V/div); b: V_C (100V/div); c: I_2 (2.5A/div).)

The performance of the system with large capacitor current internal impedance term gain ($G_{Internal}(\mathrm{s}) = 110$) is obtained in Fig. 2. 17. Since large internal impedance gain represents a small parallel virtual damping impedance at capacitor branch, the 11$^{\mathrm{th}}$ harmonic current disappears while the low order harmonics (2$^{\mathrm{nd}}$ harmonic current) is amplified. Here the 2$^{\mathrm{nd}}$ harmonic current is 27.5%. Finally, an improved line current (THD=4.51%) can be seen in Fig. 2. 18 when an internal impedance with $G_{Internal}(\mathrm{s}) = 25$ is adopted.

2.5.2. Deadbeat control scheme verification results

The performance of interfacing converter using both conventional and the proposed deadbeat current control schemes is also tested in the Matlab/Simulink. The circuitry and control parameters are listed in TABLE. 2. 3.

First, the performance of the system with a step change of reference current from 6A to 20A is shown in Fig. 2. 19 and Fig. 2. 20. It is obvious that the reference change introduces significant transient resonances in the interfacing converter with conventional deadbeat control (transient line current THD=25.89%, for one cycle after the step change) in Fig. 2. 19, and this resonance can be dampened with the proposed virtual impedance control method as shown in Fig. 2.

TABLE. 2. 3. Circuit and control parameters of a single-phase 120V/1KVA inverter with deadbeat control

Parameters	Symbols	Values
Circuit Parameter		
Inverter side inductor	L_1 , R_1	3mH (0.079pu), 0.25Ω (0.017pu)
Filter capacitor	C_f	40 uF (0.215pu)
Line side inductor	L_2 , R_2	0.2mH(0.005pu), 0.05Ω(0.004pu)
PCC voltage	V_{PCC}	60V/60Hz(experiment)
DC Link voltage	V_{DC}	180V(experiment)
Control Parameter		
Switching frequency		12kHz
Virtual impedance	*Rv*	6.5 Ω

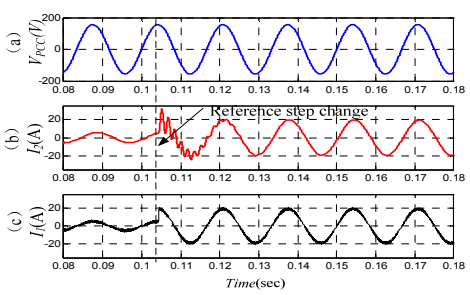


Fig. 2. 19. Performance of deadbeat control during reference step change (without damping). (a. PCC voltage: 200v/div; b. line current: 10A/div; c. output current: 10A/div). (**Simulation**)

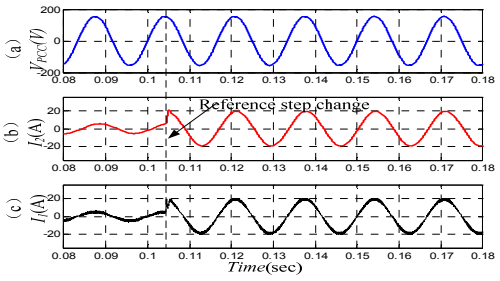


Fig. 2. 20. Performance of deadbeat control during reference step change (active damping). (a. PCC voltage: 200v/div; b. line current: 10A/div; c. output current: 10A/div). (**Simulation**)

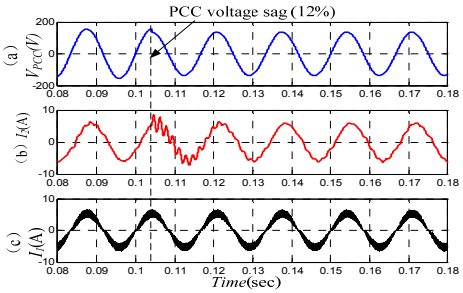


Fig. 2. 21. Performance of deadbeat control during grid voltage sags (without damping). (a. PCC voltage: 200v/div; b. line current: 10A/div; c. output current: 10A/div). (**Simulation**)

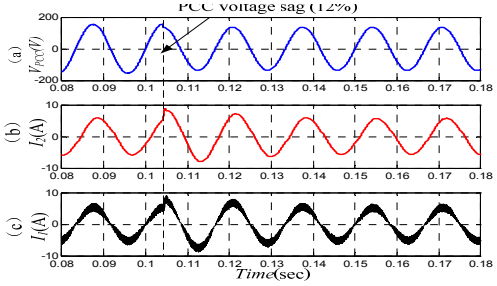


Fig. 2. 22. Performance of deadbeat control during grid voltage sags (active damping). (a. PCC voltage: 200v/div; b. line current: 10A/div; c. output current: 10A/div). (**Simulation**)

20 (transient THD=6.63%).

The transient resonance introduced by grid voltage disturbances is also investigated. The associated dynamic responses of inverter1 are examined in Fig. 2. 21 and Fig. 2. 22. As shown in Fig. 2. 21, the performance of conventional deadbeat control is sensitive to grid voltage disturbances. The improved performance using virtual impedance based active damping is shown in Fig. 2. 22. During voltage sag transients, conventional deadbeat control gives a 21.85% transient THD while the active damping control reduces the THD to 4.52%.

To verify the theoretical analysis, experiments are also conducted on a scaled single-phase laboratory H-bridge inverter. The main grid is emulated by a programmable AC power supply. The DC link voltage is provided by three-phase diode rectifiers with isolation. Due to the impact of diode rectifiers, the inverter DC link voltage has some ripples.

The performances of the inverter with reference step changes for 2.5A to 7A are shown in Fig. 2. 23 and Fig. 2. 24. When the conventional control without damping is implemented, the line current has significant harmonics during reference step change transient. Moreover, due to the effects of non-ideal DC link voltage with small voltage ripples, there are also some steady-state harmonics in Fig. 2. 23. However, the investigation on the contribution of DC link voltage

ripples to system resonance is out of the scope of the discussion here. When the active damping scheme is enabled, the improved results are shown in Fig. 2. 24.

The experimental results of single inverter during 15% grid voltage sag are also obtained in Fig. 2. 25 and Fig. 2. 26. With the conventional control, it can be seen in Fig. 2. 25 that the grid voltage sag introduces some transient line current harmonics. With the active damping, the transient harmonics are properly mitigated as shown in Fig. 2. 26.

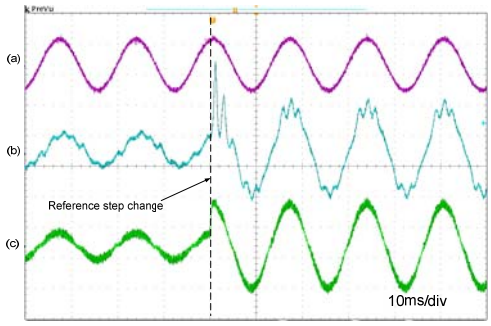


Fig. 2. 23. Performance of deadbeat control during reference step change (without damping). (a. PCC voltage: 100v/div; b. line current: 5A/div; c. output current. 5A/div). (**Experiment**)

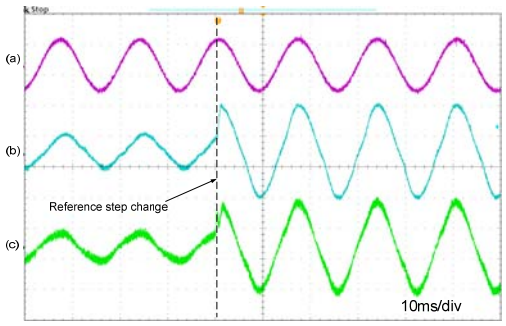


Fig. 2. 24. Performance of deadbeat control during reference step change (active damping). (a. PCC voltage: 100v/div; b. line current: 5A/div; c. output current: 5A/div). (**Experiment**)

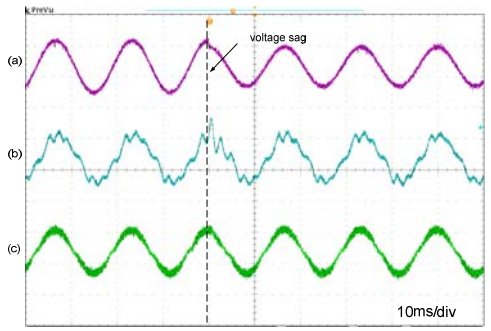


Fig. 2. 25. Performance of deadbeat control during grid voltage sag (without damping). (a. PCC voltage: 100v/div; b. line current: 5A/div; c. output current: 5A/div). (**Experiment**)

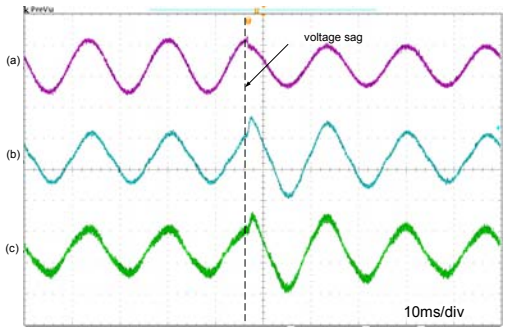


Fig. 2. 26. Performance of deadbeat control during grid voltage sag (active damping). (a. PCC voltage: 100v/div; b. line current: 5A/div; c. output current: 5A/div). (**Experiment**)

2.6. Summary

A resonance problem is described that is caused by LC and LCL filters in the DG unit power electronics interface. First, this chapter adopts the closed-loop Norton equivalent circuit to evaluate the resonance problem. The performance of interfacing converter using a few well accepted control schemes is discussed. It shows that although the single-loop control and the conventional deadbeat control feature simple control structure, they do not have any damping effects to the output filter resonance. As a result, they can easily cause harmonic problems in the interfacing converters.

In order to improve the performance of grid-interfacing converters, a generalized closed-loop control (GCC) scheme is proposed. It has an internal impedance to mitigate the resonance problem. Further discussion indicates the proposed GCC scheme can be used to explain the performance of double-loop current control with different inner loop feedbacks. Additionally, the proposed GCC scheme can also simplify the parameter design process of the double-loop control.

To provide active damping to the traditional deadbeat current control scheme, a shunt virtual harmonic impedance control scheme is proposed. This proposed control scheme is realized through modifying the inverter output current reference with a compensation term (associated with LCL filter capacitor voltage). As the filter capacitor voltage is also measured for grid synchronization, this proposed method easily realizes active resonance damping without using any additional sensors. Verification results show that the proposed GCC and deadbeat control schemes can effectively mitigate the resonance in the interfacing converter filters, and the line current quality can be improved accordingly.

Chapter 3

Modeling and Active Damping of Multiple Resonances for Parallel Grid-Tied Inverters

Distributed RESs are often integrated into the power system by using multiple DG units, which are often named as "grid-interactive microgrid" in recent literature. Since multiple DG interfacing inverters are coupled together, the disturbances from other parallel inverters may cause complex resonances in an inverter's line current. This chapter investigates the resonance interactions of grid-interactive microgrid. First, an accurate microgrid model is developed based on a closed-loop transfer function matrix. With this model, different types of resonances can be easily investigated and evaluated.

In addition, the active damping methods for a single inverter system are examined in the situation of multiple parallel inverters. It shows that virtual impedance based damping methods are also very effective in mitigating multiple resonances in parallel inverters based grid-interactive microgrid. Extensive simulated and experimental results are provided to support the discussion.

3.1. Modeling of multiple parallel inverters

The modeling of multiple parallel inverters can be performed in either discretize-time z-domain or continuous-time s-domain. For the converter controller designed in s-domain, such as single-loop, multi-loop control, and GCC

Publications out of this chapter:

(1) J. He, Y. W. Li, D. Bosnjak, and B. Harris, "Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter Based Microgrid," IEEE Transactions on Power Electronics, vol. 28, pp. 234-246, Jan. 2013.

scheme, the analysis is conducted in the continuous-time s-domain for the sake of convenience. On the other hand, z-domain analysis is adopted for controllers developed in a digital manner, such as the deadbeat controller discussed in Chapter 2.

3.1.1. Multiple parallel inverters with controllers developed in s-domain

The model of parallel inverters with current tracking controllers developed in s-domain is analyzed here. First, the configuration of a grid interactive microgrid with multiple parallel inverters is shown in the upper part of Fig. 3. 1.

To form a microgrid, each inverter is connected to PCC with an LCL filter. Then, the microgrid is connected to the main grid with the main grid feeder, which is described as L_{grid} and R_{grid}. In this section, we assume that all parallel inverters are controlled by the same closed-loop current controller.

Since each interfacing inverter is modeled as a Norton equivalent circuit in the s-domain, the equivalent circuit of the entire microgrid can be established with the help of single inverter model. The equivalent circuit of multiple parallel inverters is shown in the lower part of Fig. 3. 1. As shown, for a microgrid with *N* parallel inverters, it can be modeled by *N* controlled current sources and *N* parallel admittances. The grid voltage V_{grid} is connected to PCC with the microgrid feeder series admittance.

With the developed model, line current of inverters can be determined accordingly. For instance, the line current of inverter1 ($I_{2,1}$) is obtained by applying Kirchhoff's law as

$$V_{PCC} = \frac{(\sum_{i=1}^{N} G_{eq,i}(s) \cdot I_{ref,i} + Y_{grid}(s) \cdot V_{grid})}{\sum_{i=1}^{n} Y_{eq,i}(s) + Y_{grid}(s)} \tag{3-1}$$

$$I_{2,1} = G_{eq,1}(s) \cdot I_{ref,1} - Y_{eq,1}(s) \cdot V_{PCC} \tag{3-2}$$

where $G_{eq,1}(\mathrm{z})$ to $G_{eq,N}(z)$ are the closed-loop gains of current sources, and $Y_{eq,1}(\mathrm{z})$ to $Y_{eq,N}(\mathrm{z})$ are their associated parallel admittances, respectively. $Y_{grid}(\mathrm{z})$ is the grid admittance. $I_{ref,1}$ to $I_{ref,N}$ are current references of multiple parallel inverters.

From (3-1) and (3-2), the line current of inverter1 can be re-expressed as

$$I_{2,1} = \overbrace{R_1(s)\cdot I_{ref,1}}^{\text{Internal Resonance}} + \overbrace{\sum_{t=2}^{N} P_{1,t}(s)\cdot I_{ref,t}}^{\text{Parallel Resonance}} - \overbrace{S_{G,1}(\mathrm{s})\cdot V_{grid}}^{\text{Series Resonance}} \qquad (3\text{-}3)$$

It can be noticed that (3-3) has three terms and each term represents one type of resonance in the system. Specifically, the first term (internal resonance) represents the resonance introduced by the change of inverter1's current reference signal. The second term is the parallel interaction among inverters, which is introduced by changes of reference signal in other inverters. Finally, the third term demonstrates the series interaction between the main grid and the multiple-inverter based microgrid system. The elements of (3-3) are obtained as

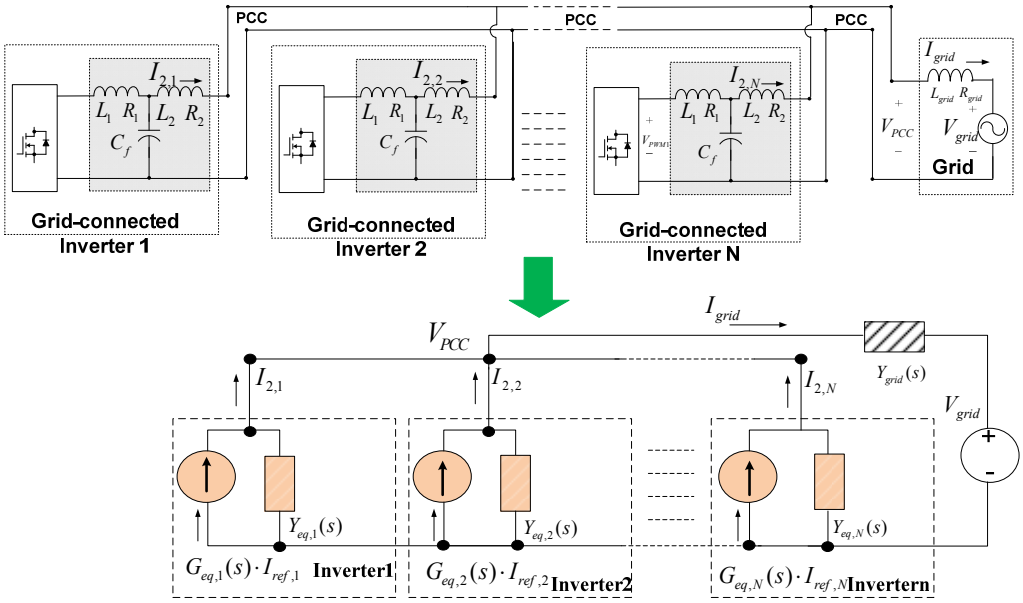


Fig. 3. 1. Illustration of the proposed closed-loop model of parallel grid-connected inverters.

$$R_1(s) = G_{eq,1}(s) - \frac{Y_{eq,1}(s) \cdot G_{eq,1}(s)}{\sum_{i=1}^{N} Y_{eq,i}(s) + Y_{grid}(s)} \tag{3-4}$$

$$P_{1,t}(z) = \frac{-Y_{eq,1}(s) \cdot G_{eq,t}(s)}{\sum_{i=1}^{N} Y_{eq,i}(s) + Y_{grid}(s)}, \quad t \in [2, N] \tag{3-5}$$

$$S_{G,1}(z) = \frac{Y_{eq,1}(s) \cdot Y_{grid}(s)}{\sum_{i=1}^{N} Y_{eq,i}(s) + Y_{grid}(s)} \tag{3-6}$$

When a similar analysis approach is applied to other inverters, the behavior of the microgrid can be described using a closed-loop transfer function matrix with reference currents and grid voltage as inputs and inverter line currents as outputs

$$\begin{pmatrix} I_{2,1} \\ I_{2,2} \\ \cdots \\ I_{2,N} \end{pmatrix} = \begin{pmatrix} R_1(s) & P_{12}(s) & \cdots & P_{1N}(s) \\ P_{21}(s) & R_2(s) & & \\ \cdots & \cdots & \cdots & \\ P_{N1}(s) & P_{N2}(s) & & R_N(s) \end{pmatrix} \cdot \begin{pmatrix} I_{ref,1} \\ I_{ref,2} \\ \cdots \\ I_{ref,N} \end{pmatrix} - \begin{pmatrix} S_{G,1}(s) \\ S_{G,2}(s) \\ \cdots \\ S_{G,2}(s) \end{pmatrix} \cdot V_{grid} \tag{3-7}$$

It is obvious that the parallel inverters are always coupled when the non-diagonal elements of (3-7) are not zero. For the ideal stiff grid with zero grid impedance, the non-diagonal elements become zero and the inverters are decoupled. However, as a low voltage microgrid or a remote microgrid often have nontrivial grid impedance, strong inverter couplings may introduce significant resonant current in the microgrid.

3.1.2. Multiple parallel inverters with controllers developed in z-domain

For parallel grid-tied inverters regulated by controllers developed in the discretized z-domain, such as the one-step deadbeat control, it is convenient to investigate the performance of the microgrid using z-domain closed-loop transfer function matrix.

For the grid interactive microgrid with parallel inverters using controllers developed in the z-domain, the response can be calculated by (3-8) and the equivalent circuit is given in Fig. 3. 2.

$$\begin{pmatrix} I_{2,1}(z) \\ I_{2,2}(z) \\ \cdots \\ I_{2,N}(z) \end{pmatrix} = \begin{pmatrix} R_1(z) & P_{12}(z) & \cdots & P_{1N}(z) \\ P_{21}(z) & R_2(z) & & \\ \cdots & \cdots & \cdots & \\ P_{N1}(z) & P_{N2}(z) & & R_N(z) \end{pmatrix} \cdot \begin{pmatrix} I_{ref,1}(z) \\ I_{ref,2}(z) \\ \cdots \\ I_{ref,N}(z) \end{pmatrix} - \begin{pmatrix} S_{G,1}(z) \\ S_{G,2}(z) \\ \cdots \\ S_{G,N}(z) \end{pmatrix} \cdot V_{grid}(z) \tag{3-8}$$

where $I_{ref,1}(z)$ to $I_{ref,N}(z)$ are reference currents of inverter1 to inverter N, which are considered as the inputs of the system. The inverter line side currents are $I_{2,2}(z)$ to $I_{2,N}(z)$, which are treated as the output of the system. The coefficients in (3-8) are determined according to the inverter output filters and the control parameters.

From (3-8), the response of inverter1 line current $I_{2,1}(z)$is obtained as

$$I_{2,1}(z) = \overbrace{R_1(z) \cdot I_{ref,1}(z)}^{\text{Internal Resonance}} + \overbrace{\sum_{t=2}^{N} P_{1,t}(z) \cdot I_{ref,t}(z)}^{\text{Parallel Resonance}} - \overbrace{S_{G,1}(z) \cdot V_{grid}(z)}^{\text{Series Resonance}} \tag{3-9}$$

Similar to the previous analysis for multiple inverters with controllers developed in s-domain, the response of inverter1 line current is also composed of three parts. They are defined as internal resonance, parallel resonance, and series resonance, respectively. The coefficients in (3-9) are expressed as

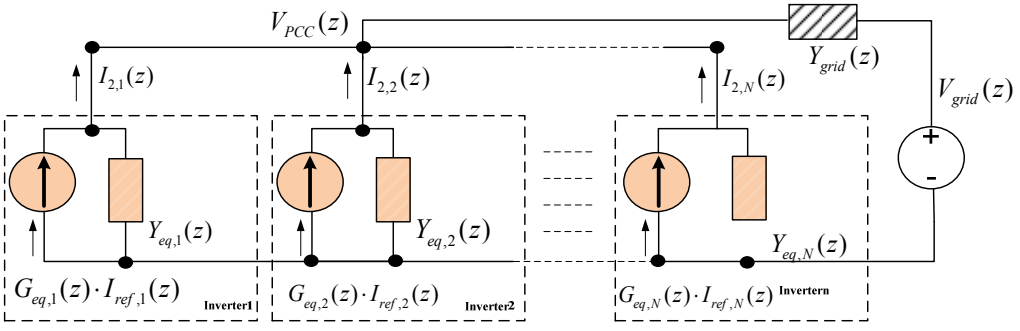


Fig. 3. 2. Diagram of multiple parallel inverters and its closed-loop equivalent circuit.

$$R_1(z) = G_{eq,1}(z) - \frac{Y_{eq,1}(z) \cdot G_{eq,1}(z)}{\sum_{i=1}^{N} Y_{eq,i}(z) + Y_{grid}(z)} \tag{3-10}$$

$$P_{1,t}(z) = -\frac{Y_{eq,1}(z) \cdot G_{eq,t}(z)}{\sum_{i=1}^{N} Y_{eq,i}(z) + Y_{grid}(z)} \qquad t \in [2, N] \tag{3-11}$$

$$S_{G,1}(z) = \frac{Y_{eq,1}(z) \cdot Y_{grid}(z)}{\sum_{i=1}^{N} Y_{eq,i}(z) + Y_{grid}(z)} \tag{3-12}$$

3.2. Frequency response analysis of multiple parallel inverters

With the closed-loop transfer function matrix for multiple inverters, the response of multiple inverters can be easily evaluated using the closed-loop Bode plots.

3.2.1. Analysis of multiple inverters with deadbeat current control

In this subsection, the responses of the system using the conventional deadbeat current control and the proposed virtual impedance based deadbeat control are compared.

- **Inverters using conventional deadbeat control without active damping**

In order to make the discussion easier, we assume that all the inverters in the microgrid have identical circuit and control parameters. Nevertheless, the current reference of each inverter is generated independently (like in PV systems with individual MPPT). The parameters are selected to be the same as in the simulation, which can be found from TABLE. 2. 3 in the previous chapter and the main grid impedance is selected as $L_{grid} = 1.4\text{mH}$ and $R_{grid} = 0.1\Omega$. The Bode plots of inverter1 are shown from Fig. 3. 3 to Fig. 3. 5.

Fig. 3. 3 shows the Bode plots of inverter1's internal resonance with different parallel inverter numbers. As illustrated, when only inverter1 is connected to the PCC, there is only one resonance peak in the Bode plot. In a microgrid with parallel inverters, the frequency response of inverter1 has two resonance peaks. Among them, the frequency of one resonance is fixed while the frequency of the other one moves to the low frequency region with more parallel inverters. By examining the expression of $R_1(z)$, it can be seen that the fixed frequency resonance peak is determined by $G_{eq,1}(z)$, while the moving resonance peak is introduced by the remaining term in $R_1(z)$. Due to these resonances, the line current of inverter1 can have transient harmonic current during the step change of its current reference signal.

In addition to the harmonics introduced by the internal resonance, the reference changes of other inverters also bring parallel resonances to inverter1. The associated Bode plots are shown in Fig. 3. 4. Similar to Fig. 3. 3, the parallel resonance also contains two resonance peaks, and one of them drifts to the low frequency region with more inverters connected to the microgrid.

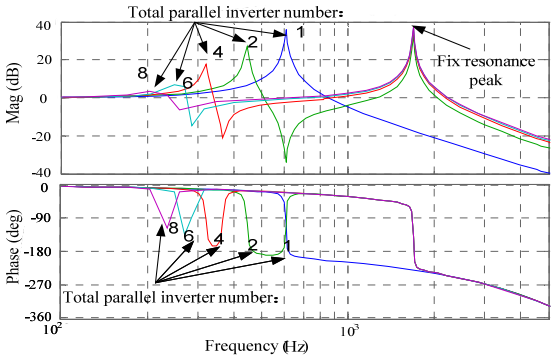


Fig. 3. 3. Inverter1's internal resonance with different parallel inverter numbers ($R_{1\mathrm{T}}(z) = I_{2,1}(z)/I_{ref1}(z)$). (Deadbeat control without active damping)

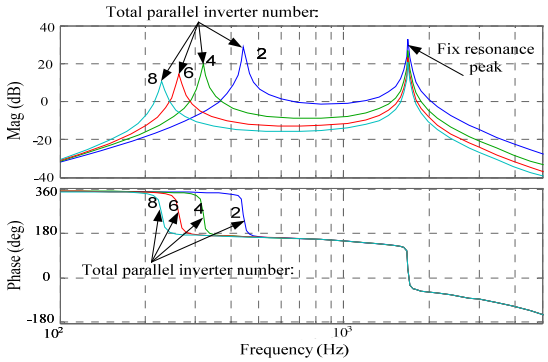


Fig. 3. 4. Inverter1's parallel resonance with different parallel inverter numbers ($P_{12}(z) = I_{2,1}(z)/I_{ref2}(z)$). (Deadbeat control without active damping)

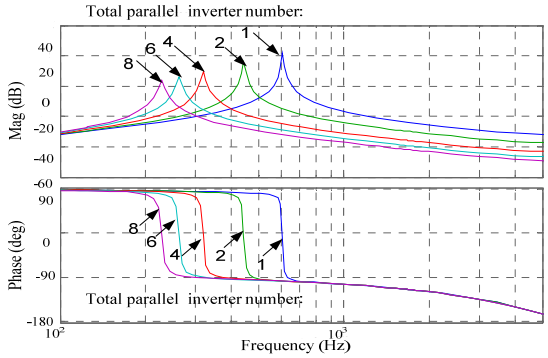


Fig. 3. 5. Inverter1's series resonance with different parallel inverter numbers ($S_G(z) = -I_{2,1}(z)/V_{grid}(z)$). (Deadbeat control without active damping)

Note that the magnitudes of frequency-varying resonances are attenuated when more parallel inverters are placed in the microgrid. This feature can be explained using the proposed equivalent circuit in Fig. 3. 1. Suppose inverter2 has a reference step change, a portion of the current $G_{eq,2}(z)I_{ref,2}(z)$ flows to the parallel admittances of inverter1. When more inverters are connected to PCC, the current flowing to inverter1's parallel admittance is attenuated as the current $G_{eq,2}(z)I_{ref,2}(z)$ is shared by more parallel admittances.

The series resonances in inverter1 are excited by the main grid. As shown in Fig. 3. 5, the frequency of series resonance is also affected by parallel inverter numbers. Further considering that the main grid voltage often has some low order steady-state background noises, significant steady-state harmonic line current can be produced by the effects of series resonance. For instance, when 4 parallel

inverters are included the microgrid, the series resonance frequency is around 300Hz, which may excite the 5th steady-state resonance in a 60Hz line frequency system.

- **Impact of main grid feeder resistance**

It is important to note that the grid feeder resistance also has non-trivial impact to system resonance, especially for the low voltage distribution system with higher feeder R/X ratio ranging from 1.5 to 4 [99]. The following Bode plots investigate the sensitivity of resonance to grid feeder resistance variations.

First, a microgrid with two parallel inverters is considered. These inverters are controlled by conventional deadbeat scheme without active damping. The parallel resonance of inverter1 is shown in Fig. 3. 6. It can be seen that large grid feeder resistance (R_{grid}) can passively mitigate some of the resonance in inverter1. However, the low frequency resonant peak is still around 10 dB even when the grid feeder has 1Ω resistance. At the same time, it can also be seen that high frequency resonant peak is less sensitive to the changes of grid feeder resistance.

Similarly, the series resonance of inverter1 is also examined. As illustrated in Fig. 3. 7, passive damping by grid feeder resistance can reduce series resonant peak. When 1Ω resistance appears in grid feeder, the series resonant peak is mitigated to around 0dB.

From Fig. 3. 6 and Fig. 3. 7, it can be concluded that active damping is needed even when the microgrid feeder resistance can provide some passive damping effects to the resonance.

- **Inverters using the proposed deadbeat control with virtual impedance based active damping**

The effectiveness of the virtual impedance aided deadbeat control method (see (2-41)) to microgrid resonances mitigation is examined using the closed-loop Bode plots.

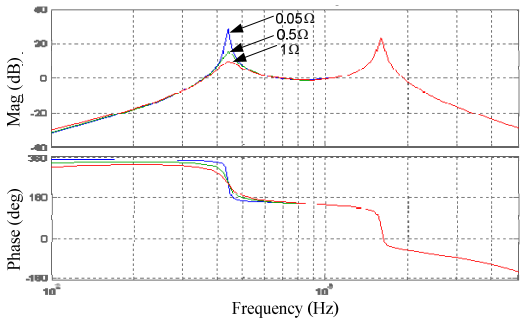


Fig. 3. 6. Inverter1's parallel resonance with different grid feeder resistance. ($P_{12}(z) = I_{2,1}(z)/I_{ref2}(z)$). (Two inverters are connected to the system. Conventional deadbeat control is used.)

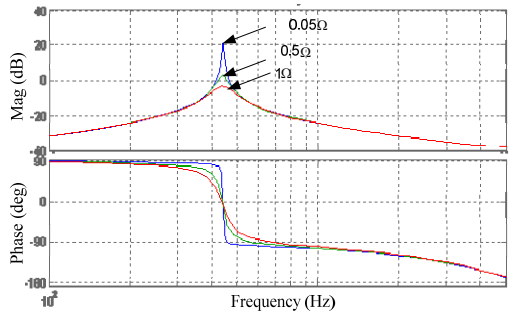


Fig. 3. 7. Inverter1's series resonance with different grid feeder resistance. ($S_G(z) = -I_{2,1}(z)/V_{grid}(z)$). (Two inverters are connected to the system. Conventional deadbeat control is used.)

Fig. 3. 8 to Fig. 3. 10 show the mitigation of resonances in inverter1 after the implementation of 6.5Ω virtual harmonic damping resistance for all the inverters. Fig. 3. 8 demonstrates inverter1's internal resonance mitigation performance. It is obvious that the previous fixed frequency resonance peak around 35dB in Fig. 3. 3 is reduced to 5dB. Also the frequency-varying resonances are around 0 dB in Fig. 3. 8. Similarly, by using the active damping method, the parallel and series resonances in inverter1 are also suppressed as shown in Fig. 3. 9 and Fig. 3. 10, respectively. Compared to the case using conventional deadbeat control without any active damping, it can be seen that the proposed active damping method is effective in addressing various types of resonances in a microgrid.

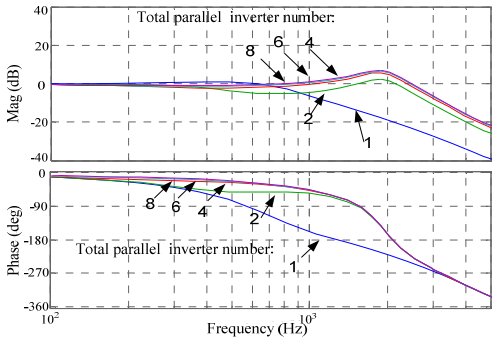


Fig. 3. 8. Inverter1's internal resonance mitigation with different parallel inverter numbers ($R_{1T}(z) = I_{2,1}/I_{ref,1}$). (Deadbeat control with virtual impedance based active damping)

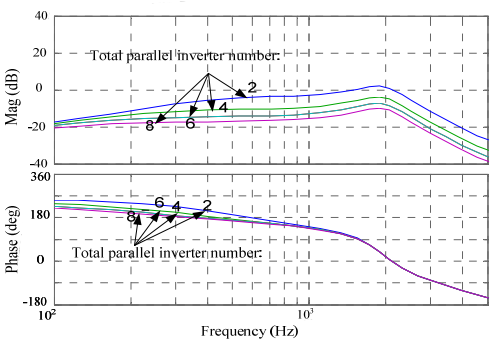


Fig. 3. 9. Inverter1's parallel resonance mitigation with different parallel inverter numbers ($P_{12}(z) = I_{2,1}/I_{ref,2}$). (Deadbeat control with virtual impedance based active damping)

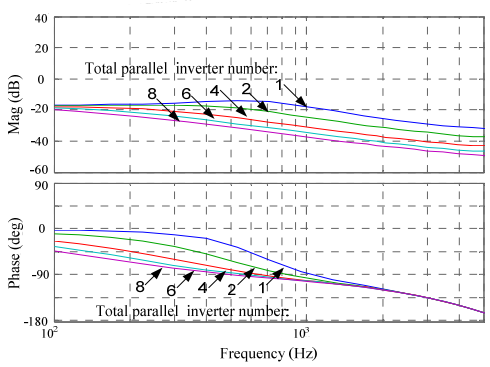


Fig. 3. 10. Inverter1's series resonance mitigation with different parallel inverter numbers ($S_{G,1}(z) = -I_{2,1}/V_{grid}$). (Deadbeat control with virtual impedance based active damping)

3.2.2. Analysis of multiple inverters with single-loop current control

The performance of multiple inverters with single closed-loop control can be analyzed in a similar manner. In this subsection, the system with inverter output current feedback is selected for case study.

When the inverter output current is selected as the feedback, the performance of multiple inverters is shown in Fig. 3. 11, Fig. 3. 12, and Fig. 3. 13. The grid impedance in this case is set to L_{grid}=1.5mH and R_{grid}=0.05Ω. Fig. 3. 11 shows the internal resonance of inverter1. It is obvious that there are two resonance peaks in the internal resonance. One resonance peak is fixed to around 1050Hz

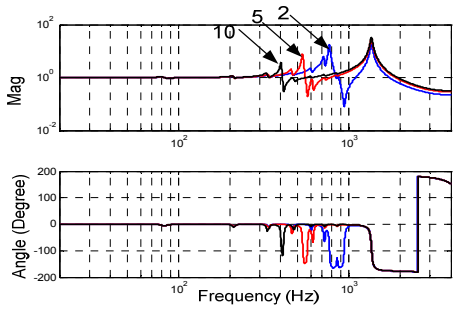


Fig. 3. 11. Internal resonance of inverter1 ($I_{2,1}/I_{ref,1}$). (2, 5, and 10 in the figure mean parallel inverter numbers of the system) (single-loop control with inverter output current feedback)

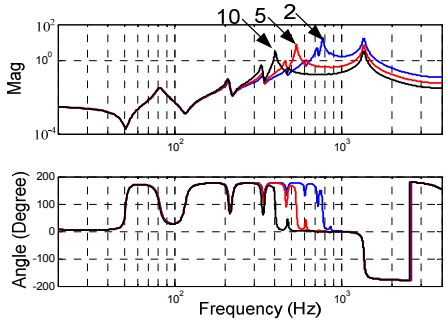


Fig. 3. 12. Parallel resonance of inverter1 ($I_{2,1}/I_{ref,2}$). (2,5, and 10 in the figure mean parallel inverter numbers of the system) (Single-loop control with inverter output current feedback)

while the other one moves to low frequency region when more parallel inverters are connected to PCC.

Similarly, the performance of the parallel resonance is also given in Fig. 3. 12. The parallel resonance illustrated in Fig. 3. 12 describes the performance of inverter1 when other inverters' references have changes. It is obvious there are also two resonant peaks and they can degrade line current quality of inverter1 during the reference changes of others inverters.

Finally, the frequency response of series resonance is shown in Fig. 3. 13. This resonant frequency moves to low frequency region when more parallel inverters are connected to the system.

It is obvious that the frequency of fixed resonance peak in Fig. 3. 11, Fig. 3. 12, and Fig. 3. 13 is close to the characteristic resonant frequency of the single inverter LCL filter as

$$f_{RES1} \approx \frac{1}{2\pi\sqrt{(L_1 \cdot L_2 / (L_1 + L_2)) \cdot C_f}} \tag{3-13}$$

The moving resonant peak at low frequency region is mainly caused by interactions between multiple inverters. The estimation of this resonant frequency without using complex closed-loop transfer function matrix is not very straightforward. Considering that harmonic resonant controllers are used in the closed-loop current tracking scheme in (2-1), it is reasonable to assume that the inverter current I_1 can accurately follow the reference current I_{ref} in the low order harmonic frequency region. As a result, a simplified equivalent circuit can be established without complex closed-loop transfer function equations, as shown in the upper part of Fig. 3. 14.

It is important to note that this equivalent circuit is only effective at the low order harmonic frequency region that is within the control bandwidth of inverter output current regulation. It cannot be used to analyze high frequency resonant in (3-13), as the inverter output current response cannot be treated as an idea controlled current source around the resonant frequency in (3-13).

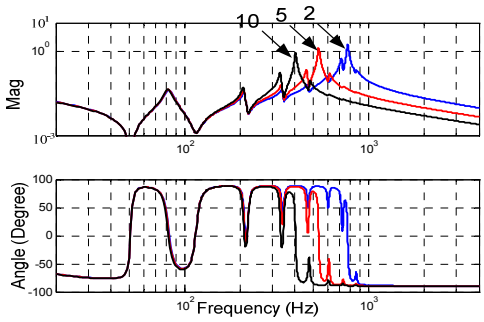


Fig. 3. 13. Series resonance of inverter1 ($-I_{2,1}/V_{Grid}$). (2,5, and 10 in the figure mean parallel inverter numbers of the system) (single-loop control with inverter output current feedback)

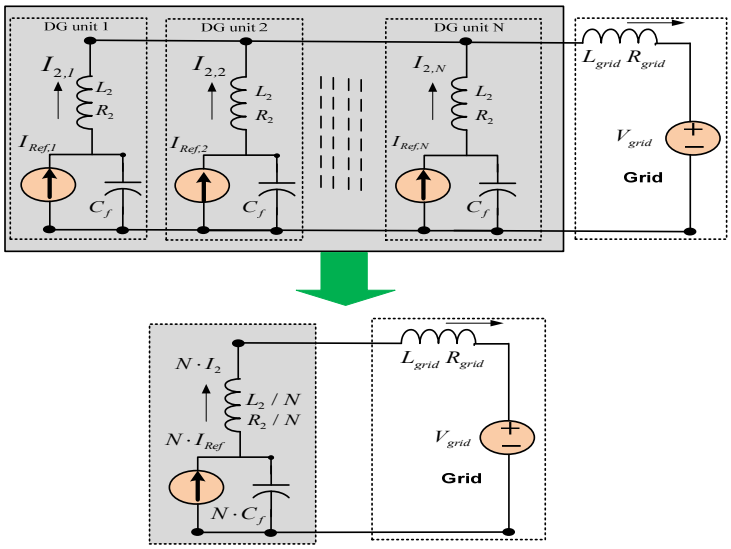


Fig. 3. 14. Simplified equivalent circuit of parallel inverters with single-loop current control and inverter output current feedback.

Considering a system has N identical parallel inverters with the same control and circuit parameters for the sake of simplicity, the N parallel inverters as shown in the upper part of Fig. 3. 14 can be further merged as a single inverter with revised parameters. Through simple calculation, it can be seen that the equivalent shunt capacitance is this case is $N \cdot C_f$ and the equivalent line side choke impedance is L_2/N and R_2/N. With this simple equivalent circuit developed in

the lower part of Fig. 3. 14, the moving resonant frequency can be easily determined as

$$f_{RES2} \approx \frac{1}{2\pi\sqrt{(L_{grid} + (L_2 / N)) \cdot (N \cdot C_f)}} \approx \frac{1}{2\pi\sqrt{(N \cdot L_{grid} + L_2) \cdot C_f}} \quad (3\text{-}14)$$

The frequency in (3-14) is in good agreement with the resonant frequency determined by complex closed-loop transfer function matrix. Considering a system with 10 parallel inverters with the parameters as shown in TABLE. 2. 1, one resonant frequency is 394.21Hz according to (3-14). On the other hand, it is obvious that one resonant frequency with 10 parallel inverters in Fig. 3. 13 is around 400Hz, which is very close to the calculated value using (3-14).

3.2.3. Analysis of multiple inverters with GCC control scheme

Finally, the performance of multiple single-phase inverters using GCC scheme is briefly discussed. The discussion here is based on the control and circuit parameter in TABLE. 3. 1. The frequency domain response of inverter1 is shown in Fig. 3. 15, Fig. 3. 16, and Fig. 3. 17. In contrast to the conventional

TABLE. 3. 1. Parameters of multiple inverters (single-phase 120V/1KVA) with GCC control scheme

Parameters	Symbols	Values
Circuit Parameter		
Inverter side inductor	L_1 , R_1	2.1mH (0.056 pu), 0.05Ω (0.004pu)
Filter capacitor	C_f , R_C	10uF (0.055pu), 0.25Ω (0.017pu)
Line side inductor	L_2 , R_2	1.3mH (0.035pu), 0.05Ω (0.004pu)
Main grid impedance	L_{grid} , R_{grid}	1.5mH (0.040pu), 0.05Ω (0.004pu)
Parallel Inverter Control Parameter		
Switching frequency		12.0kHz
PR controller proportional	$K_p = 7$ $K_{if} = 200$ $K_{i3} = K_{i5} = K_{i7} = K_{i9} = 40$ $K_{i11} = K_{i13} = K_{i15} = 20$ $K_p = 10$	

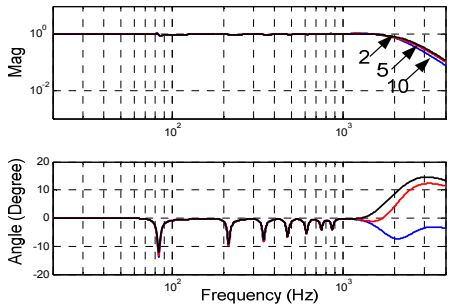


Fig. 3. 15. Internal resonance of inverter1 ($I_{2,1}/I_{ref}$). (2, 5, and 10 in the figure mean parallel inverter numbers of the system) (GCC control for multiple inverters)

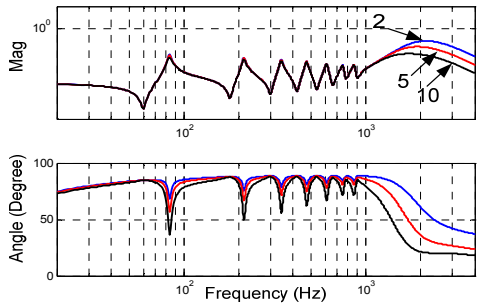


Fig. 3. 16. Parallel resonance of inverter1 ($I_{2,1}/I_{ref}$). (2,5, and 10 in the figure mean parallel inverter numbers of the system) (GCC control for multiple inverters)

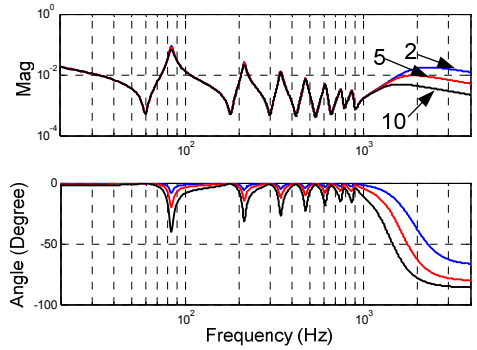


Fig. 3. 17. Series resonance of inverter1 ($I_{2,1}/V_{Grid}$). (2,5, and 10 in the figure mean parallel inverter numbers of the system) (GCC control for multiple inverters)

single-loop current control without any active damping, it shows in Fig. 3. 15, Fig. 3. 16, and Fig. 3. 17 that the GCC control scheme effectively mitigates resonances in parallel interfacing inverters.

3.3. Verification results

In this section, detailed simulated and experimental results are provided to evaluate the performance of multiple grid-tied inverters.

3.3.1. Performance with deadbeat control scheme

- Simulated results

First, a grid-interactive microgrid with deadbeat current controlled parallel inverters is considered. The control and circuitry parameters for each inverter can be seen in TABLE. 2. 3 in the previous chapter.

To verify the parallel resonances, this microgrid is originally constructed with two identical inverters (inverter1 and inverter2). The reference of inverter2 is fixed to 10A, while the reference of inverter1 changes from 6A to 20A. As discussed before, the reference changes of inverter1 can also affect the line current of inverter2. Their transient line current without damping is shown in Fig. 3. 18. As illustrated in the middle trace, the ripples of both line currents have two resonances at different frequencies around 1650Hz and 420Hz (these harmonics frequencies are determined by the investigation on the off-line harmonic spectra). In this simulation, THDs of inverter1 and inverter2 line current is 23.13% and 37.57%, respectively.

To verify the frequency-varying parallel resonance feature, four identical inverters are placed in the microgrid. The reference current of inverter1 has a step increase from 6A to 20A, while the current references of other inverters are constant during the transient. The distorted waveforms of line current without active damping are shown in Fig. 3. 19. Once again, there are considerable ripples in the line currents of inverter1 and inverter2. Compared to the microgrid with two inverters, the low frequency resonance in this case further drifts to around 300Hz.

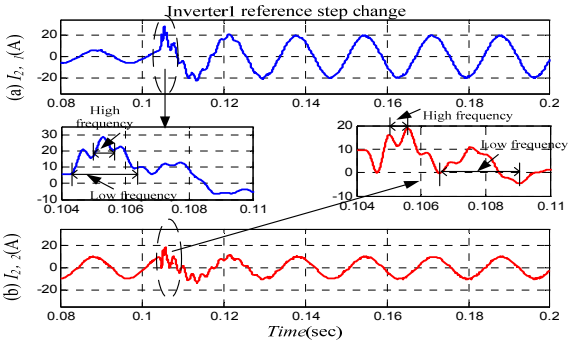


Fig. 3. 18. Parallel resonance without damping (two-inverter microgrid). (**Simulation**)

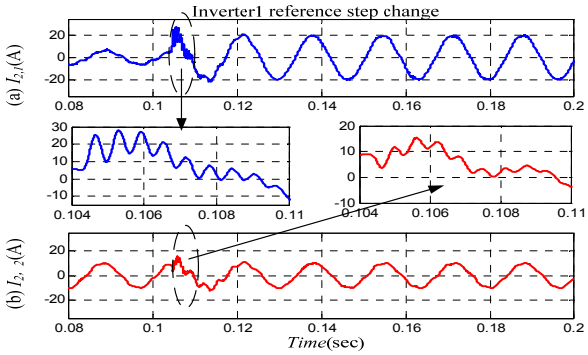


Fig. 3. 19. Parallel resonance mitigation without active damping. (four inverter microgrid). (**Simulation**)

When the active damping control is enabled, the performance of the two-inverter based microgrid is shown in Fig. 3. 20, where inverter1 and inverter2 have 4.33% and 4.95% transient THD, respectively.

To further verify multiple resonances caused by parallel resonance, a harmonic spectrum of inverter1 is provided in Fig. 3. 21. When the conventional deadbeat control without active damping is applied to multiple inverters, it can be seen that the inverter1's line current has two resonance peaks. One is at high frequency region close to the resonant of frequency of inverter1's LCL filter, while the other one is at low frequency region.

When the proposed virtual impedance based active damping control is enabled, harmonic spectrum of inverter1 is also provided in Fig. 3. 21. In this situation, it can be seen that multiple resonances are effectively mitigated.

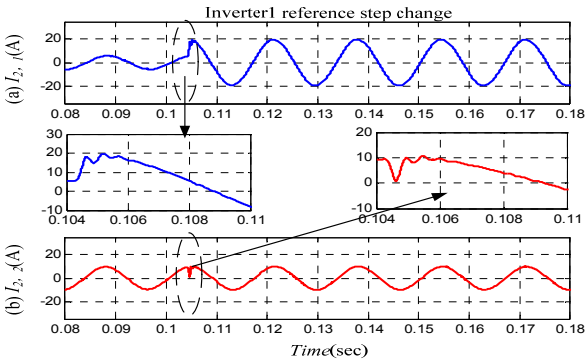


Fig. 3. 20. Parallel resonance mitigation with active damping (two-inverter microgrid). (**Simulation**)

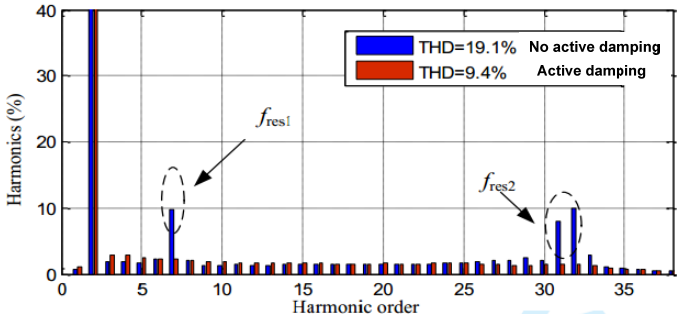


Fig. 3. 21. Harmonic spectra of inverter1 during parallel resonance transient.

In addition to transient resonance, the steady-state series resonances are investigated in Fig. 3. 22. In this simulation, 2% 5th steady-state harmonic voltage is intentionally added to the grid voltage. The microgrid originally operates with four parallel inverters. Since the series resonance peak is close to 5th harmonic frequency when four inverters are included, the line current of inverter1 has 15.59% THD before 0.25sec.

After the disconnection of three inverters (inverter2 to inverter4) at 0.25sec, the steady-state line harmonic current of inverter1 is attenuated with 4.38% THD. To demonstrate the effectiveness of the proposed active damping method, the enhanced performance during the disconnection of three inverters is also shown in Fig. 3. 23, where inverter1's line current THD is 4.01% before the transition and it reduces to 3.54% after the transition.

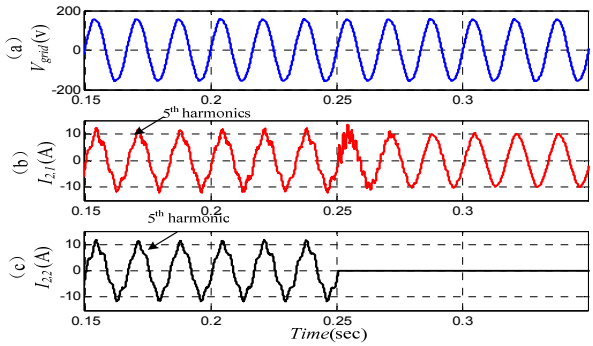


Fig. 3. 22. Series resonance without damping (Inverter2 to Inverter4 shut down at 0.25sec). (**Simulation**)

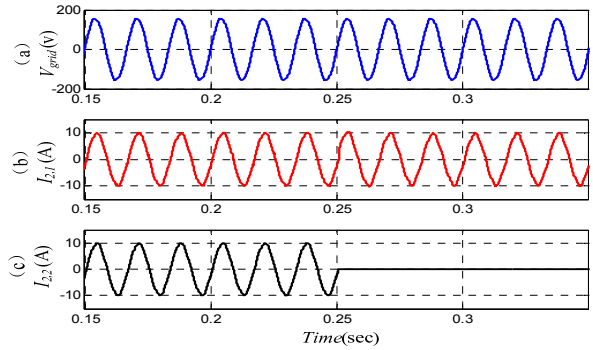


Fig. 3. 23. Series resonance mitigation with active damping. (Inverter2 to Inverter4 shut down at 0.25sec). (**Simulation**)

- Experimental results

To verify the theoretical analysis, experiments are also conducted on a scaled single-phase laboratory prototype.

To investigate the parallel resonances, two identical inverters are connected to the PCC. In this test, the reference of inverter1 has a step reference jump from 1.5A to 7.5A, while the reference of inverter2 keeps constant (1.5A) during the process. The line current without damping is shown in Fig. 3. 24. Similar to the simulation results, line currents of both inverters are distorted after current reference signal step change of inverter1. In addition to transient resonances, there are also some steady-state resonances after the reference jump. This is because the

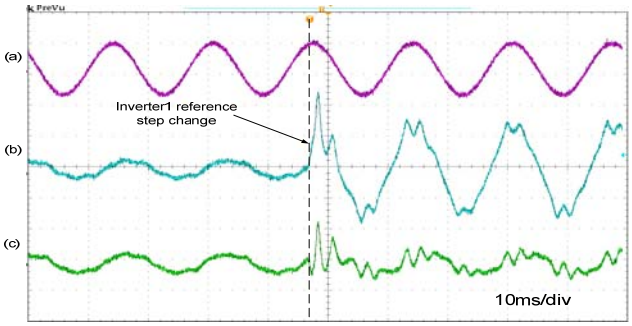


Fig. 3. 24. Parallel resonances between two-inverter microgrid without damping. (a. main grid voltage: 100v/div; b. line current of inverter1: 5A/div; c. line current of inverter2: 5A/div). (**Experiment**)

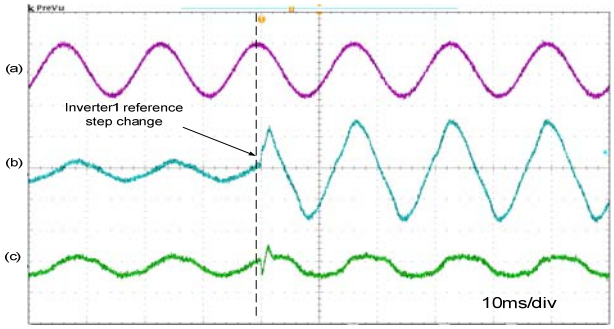


Fig. 3. 25. Mitigation of parallel resonances between two-inverter microgrid with active damping. (a. main grid voltage: 100v/div; b. line current of inverter1: 5A/div; c. line current of inverter2: 5A/div). (**Experiment**)

DC link voltage of the inverter is provided by diode rectifiers. The DC voltage ripples are amplified when more power flows through the diode bridge rectifier.

The associated experimental results with active damping are also presented in Fig. 3. 25. Once again, the active damping control gives better line current quality by reducing the magnitude of parallel resonance peaks.

Finally, the steady-state series resonances between the microgrid system and the main grid are examined. As mentioned earlier, this phenomenon often appears in the distribution system with weak main grid. Therefore, the grid impedance is increased to 3.4mH and 1Ω to test the performance of the system. In addition, the grid voltage contains 2.8% 5^{th} and 2.8% 7^{th} steady-state harmonics.

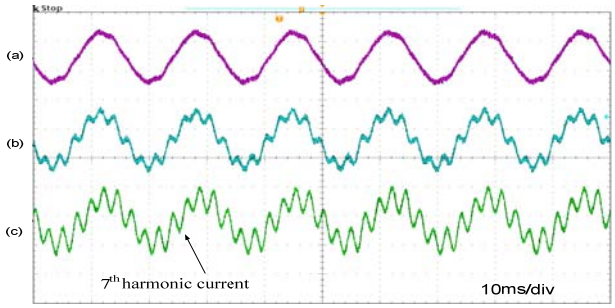


Fig. 3. 26. Series resonances of inverter1 in a single-inverter based microgrid without damping. (a. grid voltage: 100v/div; b. PCC voltage: 100v/div; c. line current of inverter1: 5A/div). (**Experiment**)

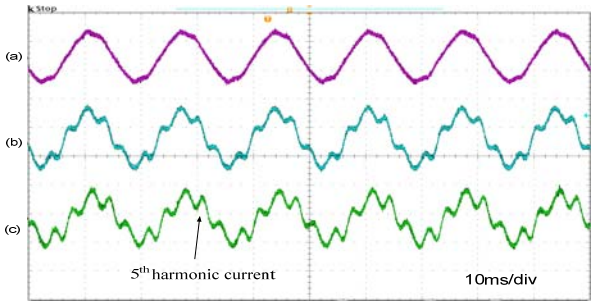


Fig. 3. 27. Series resonances of inverter1 in a double-inverter based microgrid without damping. (a. grid voltage: 100v/div; b. PCC voltage: 100v/div; c. line current of inverter1: 5A/div). (**Experiment**)

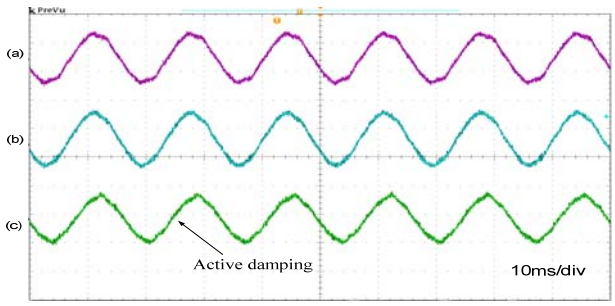


Fig. 3. 28. Mitigation of series resonances of inverter1 in a double-inverter based microgrid with active damping. (a. grid voltage: 100v/div; b. PCC voltage: 100v/div; c. line current of inverter1: 5A/div). (**Experiment**)

When only a single inverter (inverter1) is placed in the microgrid, the corresponding waveforms are obtained in Fig. 3. 26. Although the nontrivial resistive component of grid impedance can provide more passive damping effects

to the system, the line current of inverter1 and the PCC voltage are still severely polluted by the series interaction between microgrid and main grid. It is obvious that the major harmonics here are 7^{th} harmonics.

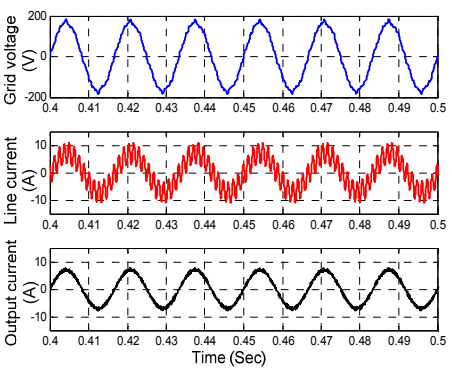
On the other hand, when another inverter (inverter2) is placed in the microgrid, the waveforms of inverter1 are shown in Fig. 3. 27. As expected, the dominate resonance in the PCC voltage and line current changes from 7^{th} harmonics to 5^{th} harmonics due to the operation of inverter2. Therefore, for a distribution system with variable DG unit numbers, the steady-state harmonics can change.

With the proposed active damping method, the steady-state power quality of the microgrid can be significantly improved. The enhanced performance of inverter1 is obtained in Fig. 3. 28.

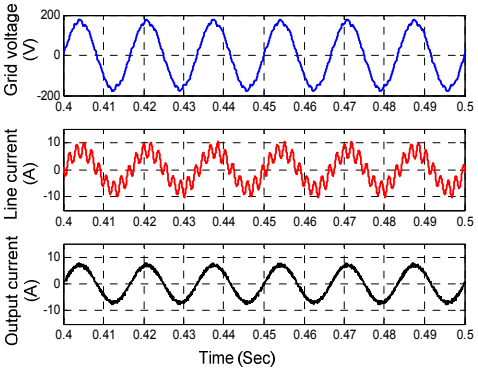
3.3.2. Performance with single-loop control

When parallel inverters are regulated by single-loop PR controller with inverter output current feedback, the steady-state performance of inverter1 is shown in Fig. 3. 29. In this simulation, 2.5% harmonic distortion is added to 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}, and 15^{th} harmonic frequencies, respectively. When only two inverters are connected to PCC, it can be seen from Fig. 3. 29(a) that the 13^{th} harmonic current is the dominant harmonic distortion in the inverter1 line current and the line current THD in this case is 55.04%.

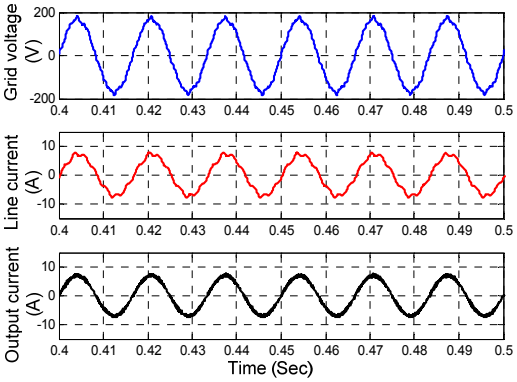
When five parallel inverters are connected to PCC, it can be observed that the dominant harmonic distortion in the line current drifts to 9^{th} harmonic frequency and the line current THD is 44.28%. When ten parallel inverters are simulated in Fig. 3. 29(c), it can be seen the resonance further dips to 7^{th} harmonic frequency.



(a) with two parallel inverters



(b) with five parallel inverters



(c) with ten parallel inverters

Fig. 3. 29. Performance of inverter1 with single-loop current control and inverter output current feedback. (**Simulation**)

To test the parallel and internal resonance of the system, two inverters are connected to a ripple-free main grid. During this test, inverter2's reference current signal has a step change while the reference current signal of inverte1 keeps constant. It can be seen from Fig. 3. 30 that both inverter1 and inverter2 line currents are distorted during the transient. This proves that when a current reference signal step jump happens in inverter1, the line current power quality of other inverters can also be affected.

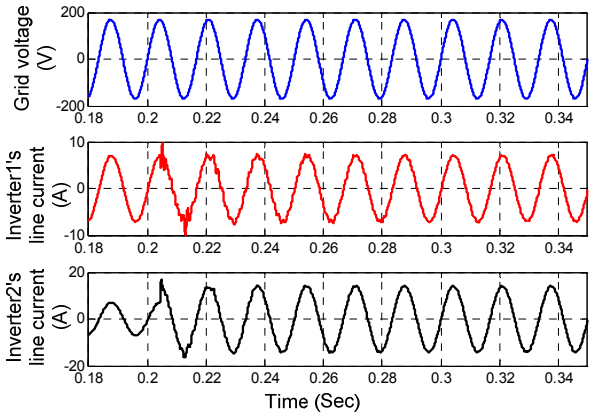
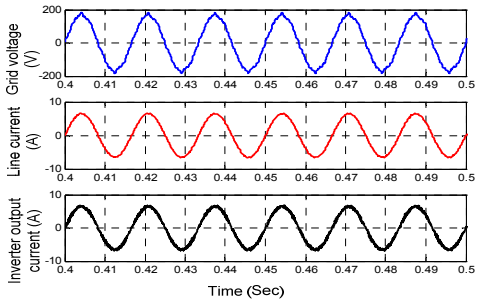
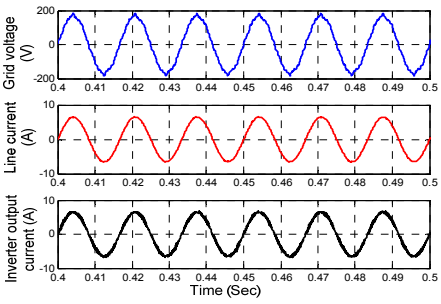


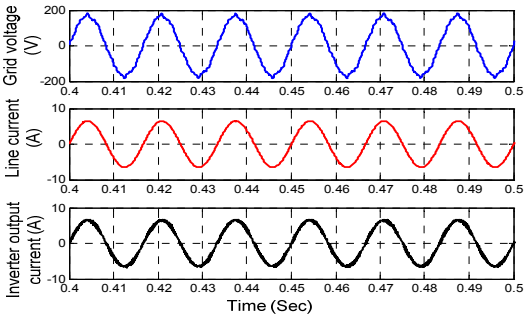
Fig. 3. 30. Performance of inverter1 and inverter2 during the reference step change of inverter. (**Simulation**)



(a) with two parallel inverters



(b) with five parallel inverters



(c) with ten parallel inverters

Fig. 3. 31. Performance of inverter1 with GCC control scheme. (**Simulation**)

3.3.3. Performance with GCC scheme

Similar to the previous simulation, the performance of inverter1 in a grid-interactive microgrid with various parallel inverter numbers is tested. In this simulation, the LCL filter capacitor current is measured to produce the internal virtual impedance (see (2-15)). Fig. 3. 31 shows that the parallel inverters are not sensitive to grid voltage harmonic disturbances, due to the effects of internal virtual damping impedance. The THDs of inverter1 line current in the case of two parallel inverters, five parallel inverters, and ten parallel inverters, are 4.13%, 3.25%, and 2.37%, respectively.

The transient performance of two parallel inverters during reference step change is also tested, as illustrated in Fig.3. 32. In this test, it can be seen that inverter1 and inverter2 line currents have minor low frequency distortions during the transient. Nevertheless, the distortion disappears a few cycles after the transient.

3.4. Summary

Resonance problems in a grid-interactive microgrid with multiple parallel interfacing converters are discussed. As the power rating of a microgrid can be much higher than that of a single inverter system, the PCC voltage is not stiff especially when the microgrid is connected to a weak grid with higher upstream grid impedance. Accordingly, multiple parallel interfacing converters are coupled due to PCC voltage variations. With the help of the closed-loop Norton equivalent circuit for a single inverter modeling, a closed-loop transfer function matrix is proposed to evaluate the resonance problem in grid interactive mirogrids. From the derived closed-loop transfer function matrix, it can be seen that the line current of an interfacing converter can be separated into three parts, namely internal resonance, parallel resonance, and series resonance. Further investigation also shows that resonance frequency in the grid-interactive microgrid is affected by parallel inverter numbers. As a result, conventional passive power filters can

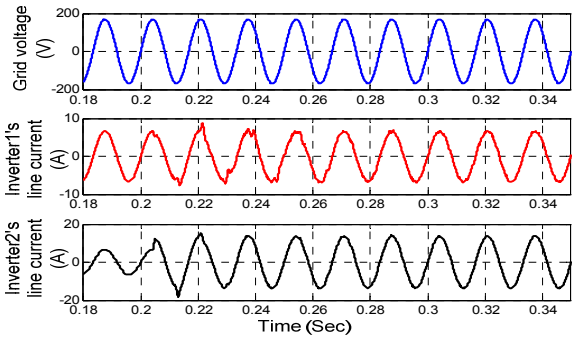


Fig.3. 32. Performance of inverter1 and inverter2 during the reference step change of inverter2 (inverters are controlled by GCC scheme). (**Simulation**)

be less effective in mitigating the resonances of a microgrid with varying parallel inverter numbers.

This chapter also verifies the effectiveness of the virtual impedance aided damping schemes in addressing the multiple resonances in the grid-interfacing microgrid. Different control schemes are considered, including the GCC scheme and the modified deadbeat control scheme. Simulated and experimental results show that all microgrid resonances can be effectively suppressed by using the proposed GCC scheme or the proposed deadbeat control with virtual harmonic damping impedance.

Chapter 4

Distribution System Harmonic Compensation Using DG Interfacing Converters

In a modern low voltage power distribution system, the increasing presence of nonlinear loads can cause severe harmonic pollutions. Chapter 4 mainly studies the feasibility of using DG units to compensate the harmonics caused by nonlinear loads. Since DG units can operate using current controlled method (CCM) or voltage controlled method (VCM), corresponding harmonic compensation methods are developed in this chapter.

First, a simple CCM based compensation method is discussed. The proposed method can avoid the adoption of phase-locked-loop (PLL) and the harmonic detection which are required in the conventional active power filters. Therefore, it can easily improve the programming efficiency in many existing DG units with limited computational capability. On the other hand, a conventional VCM based DG unit controls the power flow without using direct line current tracking loop. This feature challenges the effectiveness of harmonic compensation methods developed for CCM. Alternatively, the proposed VCM based compensation is focused on the PCC harmonic voltage reduction using feed-forward control. Verification results show that the proposed method can flexibly control PCC harmonic distortions without using the direct line current regulation.

Publications out of this chapter:

(1) J. He, Y. W. Li, F. Blaabjerg, and X. Wang, "Active Harmonic Filtering Using Current Controlled Grid-Connected DG Units with Closed-Loop Power Control," IEEE Transactions on Power Electronics, in press, 2013.

(2) J. He, Y. W. Li, and M. S. Munir, "A Flexible Harmonic Control Approach through Voltage Controlled DG-Grid Interfacing Converters," IEEE Transactions on Industrial Electronics, vol. 59, pp. 444-455, Jan. 2012.

4.1. Improved CCM for harmonic compensation

To compensate distribution system harmonic distortions, current controlled interfacing converter with harmonic compensation capability has already been proposed in recent literature, such as in [71][72]. In contrast to conventional APFs where the fundamental power flow is regulated to stabilize DC link voltage, the fundamental power flow of DG units is normally determined by the available power from back stage energy resources. As a result, it is important to avoid any conflicts between harmonic compensation and power generation in a DG system.

To actively compensate distribution system harmonics using DG units, the measurement of harmonics is needed. It mainly consists of two types:

(1) Local load harmonic current compensation with load harmonic current acquisition.

(2) Harmonic mitigation with PoC harmonic voltage detection. Note that in this category, a converter sets the line harmonic current reference as the measured harmonic voltage multiplies by an adjustable gain. As a result, it can control the DG unit like a small resistor (also named as R-APF [71][72][80]) at selected harmonic frequencies. In addition to PCC harmonic voltage compensation, this method can also be used to mitigate the resonance propagation in a long feeder with nontrivial distributed capacitance. In this situation, the inverter shall be installed at the end of the feeder to realize the resonance termination.

To simplify the operation of interfacing converter with ancillary harmonic compensation capabilities while maintaining accurate power control, this section presents an improved current controller with two parallel control branches. The first control branch is responsible for an interfacing converter fundamental current control, and the second one is employed for a distribution system harmonic compensation. In contrast to the conventional control methods with harmonic detection, the PoC voltage or local load current can be directly used as the input of the proposed current controller, without affecting the harmonic compensation accuracy of the interfacing converter. Moreover, with the simple PI regulation in

the outer power control loop, the proposed interfacing converter also achieves zero steady-state power tracking errors even when the fundamental current tracking has some steady-state errors.

4.1.1. Principle of harmonic compensation with PLL and harmonic detection

In this subsection, a single-phase interfacing converter using the compensation strategies in the conventional active power filters is briefly reviewed. Fig. 4. 1 illustrates the configuration of a single-phase system, where the interfacing converter is connected to the distribution system with a coupling choke (L_1 and R_1). There is a local load connected to the output terminal of the coupling choke. In order to improve the power quality of line current I_2, the harmonic component of local load current I_{Local} shall be absorbed through inverter output current I_1 regulation.

The DG unit control scheme is illustrated in the lower part. As shown, the current reference consists of two parts (I_{ref_f} and I_{ref_h}). The first one is the fundamental current reference I_{ref_f} for DG power control and the second one is the harmonic current reference I_{ref_h} for system harmonic compensation.

The fundamental current reference I_{ref_f} is synchronized with PCC voltage V_{PCC} as

$$I_{ref\_f} = \frac{(\cos(\theta) \cdot P_{ref} + \sin(\theta) \cdot Q_{ref})}{E^*} \tag{4-1}$$

where θ is the PCC voltage phase angle detected by PLL, P_{ref} and Q_{ref} are the real and reactive power reference, and E^* is the nominal voltage magnitude of the system.

The current reference generator in (4-1) is not accurate in controlling DG power, due to variations of the PCC voltage magnitude. To overcome this drawback, an improved power control method with the consideration of PCC voltage magnitude fluctuations is developed [81]. The details are described here.

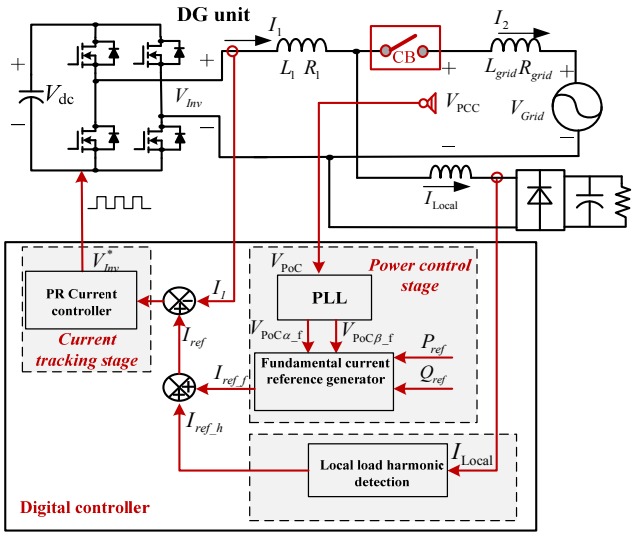


Fig. 4. 1. Diagram of a single-phase interfacing converter using conventional current control method for local load harmonic compensation.

First, the fundamental PCC voltage $V_{PCC\alpha\_f}$ and its orthogonal component $V_{PCC\beta\_f}$ (quarter cycle delayed respect to $V_{PCC\alpha\_f}$) are obtained as

$$V_{PCC\alpha\_f} = \frac{2\omega_{D1}s}{s^2 + 2\omega_{D1}s + \omega_f^2} \cdot V_{PCC} \tag{4-2}$$

$$V_{PCC\beta\_f} = \frac{2\omega_{D1}\omega_f}{s^2 + 2\omega_{D1}s + \omega_f^2} \cdot V_{PCC} \tag{4-3}$$

where ω_{D1} is the cut-off bandwidth of the filter and ω_f is the fundamental angular frequency.

For a single-phase interfacing converter system, relationships between the power reference and the fundamental reference current can be established in the artificial stationary $\alpha - \beta$ reference frame as shown in (4-4) and (4-5)

$$P_{ref} = 1/2 \cdot (V_{PCC\alpha\_f} \cdot I_{ref\alpha\_f} + V_{PCC\beta\_f} \cdot I_{ref\beta\_f}) \tag{4-4}$$

$$Q_{ref} = 1/2 \cdot (V_{PCC\beta\_f} \cdot I_{ref\alpha\_f} - V_{PCC\alpha\_f} \cdot I_{ref\beta\_f}) \tag{4-5}$$

where $I_{ref\alpha\_f}$ and $I_{ref\beta\_f}$ are the interfacing converter fundamental current reference and its orthogonal component in the artificial $\alpha-\beta$ stationary reference frame. Similarly, $V_{PCC\alpha\_f}$ and $V_{PCC\beta\_f}$ are PCC fundamental voltage and its orthogonal component. According to (4-4) and (4-5), the instantaneous fundamental current reference I_{ref_f} of a single-phase system can be obtained as

$$I_{ref\_f} = I_{ref\alpha\_f} = \frac{2(V_{PCC\alpha\_f} \cdot P_{ref} + V_{PCC\beta\_f} \cdot Q_{ref})}{V_{PCC\alpha\_f}^2 + V_{PCC\beta\_f}^2} \tag{4-6}$$

To absorb the harmonic current of local nonlinear load, the output current harmonic reference (I_{ref_h}) is determined as

$$I_{ref\_h} = G_{Har}(s) \cdot I_{Local} = \sum_{h=3,5,7,9....} \frac{2\omega_{D2}s}{s^2 + 2\omega_{D2}s + \omega_h^2} \cdot I_{Local} \tag{4-7}$$

where $G_{Har}(s)$ is the transfer function of the harmonic extractor. To realize selective harmonic compensation performance, $G_{Har}(s)$ is designed to have a set of band-pass filters with cutoff frequency ω_{D2}.

With the derived fundamental and harmonic current references, the interfacing converter output current reference is written as $I_{ref} = I_{ref\_f} + I_{ref\_h}$. Afterwards, the proportional and multiple resonant controllers are adopted to ensure current tracking as

$$\begin{aligned} V_{Inv}^* &= G_{cur}(s) \cdot (I_{ref} - I_1) \\ &= (k_p + \sum_{h=f,3,5,...15} \frac{2k_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_h^2}) \cdot (I_{ref\_f} + I_{ref\_h} - I_1) \end{aligned} \tag{4-8}$$

It should be pointed out that the objective of local load harmonic compensation is to ensure sinusoidal line current I_2 in Fig. 4. 1, and the local load current is measured to realize this task. For the harmonic filtering using harmonic voltage detection, the harmonic current reference is calculated as

$$I_{ref\_h} = (-\frac{1}{R_v}) \cdot (G_{Har}(s) \cdot V_{PoC}) \tag{4-9}$$

where R_V is the virtual damping resistance at harmonic frequencies and V_{PoC} is the DG unit installation point voltage. With this harmonic current reference (4-9), the interfacing converter essentially works as a small equivalent harmonic resistor, when it is viewed at power distribution system level [82]. For the sake of simplicity, only interfacing inverter installed at end the end of a long feeder is considered for case study, as illustrated in Fig. 4. 2. The DG feeder is modeled by an LC ladder. By providing sufficient damping effects to the long feeder, the voltage quality at different positions of the feeder can be improved.

4.1.2. Proposed harmonic compensation method

For the local load harmonic current compensation using harmonic current detection or the harmonic compensation using voltage detection, the harmonic current is absorbed by the interfacing converter. Consequently, interactions between the converter harmonic current and the grid harmonic voltage may cause some steady-steady DG harmonic power offset [83]. Nevertheless, the power control using fundamental current reference in (4-6) still operates in an open-loop manner, which can not address the power offset contributed by harmonics interactions. In order to achieve accurate power control performance in current

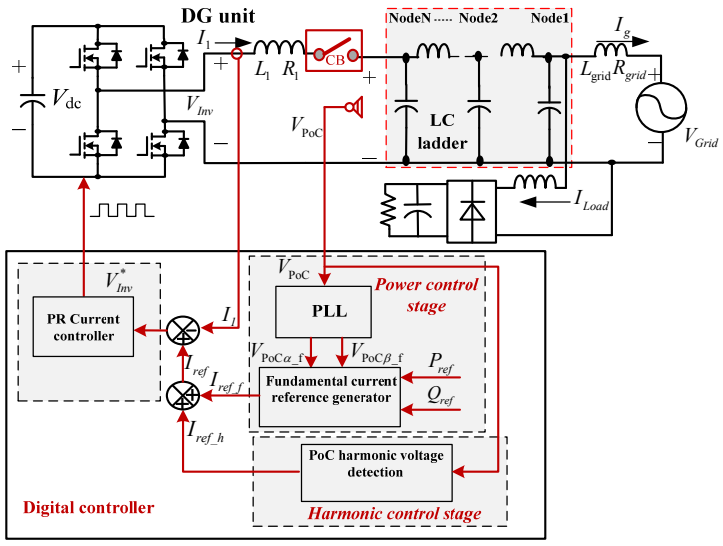


Fig. 4. 2. Diagram of a single-phase interfacing converter using conventional current control method for feeder resonance mitigation.

controlled DG units, the instantaneous fundamental output current reference can be determined by a simple closed-loop power control strategy as

$$I_{ref\_f} = g_1 \cdot V_{PCC\alpha} + g_2 \cdot V_{PCC\beta} \tag{4-10}$$

where $V_{PCC\alpha}$ is the non-filtered PCC voltage expressed in the $\alpha - \beta$ reference frame ($V_{PCC\alpha} = V_{PCC}$) and $V_{PCC\beta}$ is its orthogonal component.

The gains $g1$ and $g2$ are adjustable and they are used to control DG unit real and reactive power, respectively. The detailed regulation law is shown in (4-11) and (4-12) as

$$g_1 = (k_{p1} + \frac{k_{I1}}{s}) \cdot (\frac{1}{\tau s + 1} \cdot P_{ref} - P_{DG}) + \frac{P_{ref}}{(E^*)^2} \tag{4-11}$$

$$g_2 = (k_{p2} + \frac{k_{I2}}{s}) \cdot (\frac{1}{\tau s + 1} \cdot Q_{ref} - Q_{DG}) + \frac{Q_{ref}}{(E^*)^2} \tag{4-12}$$

where k_{p1}, k_{I1}, k_{p2}, k_{I2} are proportional and integral control parameters, P_{ref} and Q_{ref} are the real and reactive power references, E^* is the nominal voltage magnitude of the DG unit, τ is the time constant of first-order low-pass filters. P_{DG} and Q_{DG} are measured DG power with low pass filtering as

$$P_{DG} = \frac{1}{2(\tau s + 1)} \cdot (V_{PCC\alpha} \cdot I_{1\alpha} + V_{PCC\beta} \cdot I_{1\beta}) \tag{4-13}$$

$$Q_{DG} = \frac{1}{2(\tau s + 1)} \cdot (V_{PCC\beta} \cdot I_{1\alpha} - V_{PCC\alpha} \cdot I_{1\beta}) \tag{4-14}$$

where $I_{1\alpha}$ is the non-filtered interfacing inverter output current expressed in the stationary $\alpha - \beta$ reference frame ($I_1 = I_{1\alpha}$) and $I_{1\beta}$ is the delayed orthogonal component. Note that in (4-13) and (4-14), the power offset caused by harmonic voltage and harmonic current interactions is also included.

Although the proposed closed-loop power control method eliminates power tracking errors, it can be seen that the fundamental current reference in (4-10) has some distortions if PCC voltage is distorted. When it is applied to the current

controller in (4-8), the distorted fundamental current reference affects the performance of harmonic current tracking.

To overcome this drawback, an improved proportional and resonant controller with two control branches is proposed as

$$
\begin{aligned}
V_{Inv}^{*} = & \overbrace{\frac{2k_{if}\omega_c s}{s^2+2\omega_c s+\omega_f^2}\cdot(I_{ref\_f}-I_1)}^{Branch1:\ power\ control} \\
& + \overbrace{(k_P+\sum_{h=3,5,\ldots 15}\frac{2k_{ih}\omega_c s}{s^2+2\omega_c s+\omega_h^2})\cdot(I_{ref\_h}-I_1)}^{Branch2:\ harmonic\ control} \\
= & \underbrace{G_f(s)\cdot(I_{ref\_f}-I_1)}_{Branch1:\ power\ control}+\underbrace{G_h(s)\cdot(I_{ref\_h}-I_1)}_{Branch2:\ harmonic\ control}
\end{aligned}
\tag{4-15}
$$

As shown, the fundamental current reference in (4-10) is regulated by the "power control" branch in (4-15). As only fundamental resonant controller is adopted in this branch, the impacts of harmonic components in I_{ref_f} can be automatically filtered out. Therefore, the power control branch cannot introduce any obvious harmonic disturbances to the harmonic control branch in (4-15). Meanwhile, the harmonic current reference I_{ref_h} is regulated by the "harmonic control" branch, where only harmonic resonant controllers are included. Considering the control of non-characteristic harmonics in the system, a small proportional gain k_P is used to ensure better harmonic current tracking.

As fundamental resonant controller is not included in the harmonic control branch, it is possible to remove the harmonic extraction blocks in (4-7). Accordingly, the local load current or PoC voltage without any filtering can be directly used as the input of the harmonic control branch. Note that when the harmonic current reference I_{ref_h} is set to zero, the harmonic control branch ensures that the inverter output current is ripple-free. This is very similar to the performance of conventional DG unit without any compensation, where the DG unit current is controlled to be sinusoidal.

In summary, the harmonic current reference in (4-15) can have three options as given in (4-16)

$$I_{ref\_h} = \begin{cases} I_{Local} & \text{Local nonlinear load compensaion} \\ -V_{PoC} / R_V & \text{Harmonic voltage compensaion} \\ 0 & \text{Harmonic current rejection} \end{cases} \tag{4-16}$$

With the proposed method in (4-15) and the control reference in (4-16), it seems there is a complication. When the local load current or the PoC voltage are directly employed as the input of the harmonic control branch and the proportional gain k_P is used in (4-15), the output of harmonic control branch has some fundamental component. These fundamental components may cause interferences with the power control branch. As a result, the fundamental current tracking has some steady-state errors. However, further considering that the fundamental current tracking in (4-15) essentially behaves as an inner loop of the proposed closed-loop DG unit power (P_{DG} and Q_{DG}) regulation in (4-10), the DG unit still has zero steady-state power control error even when its fundamental current tracking has some errors.

The diagram of the proposed control method is presented in Fig. 4. 3. It shows that the PLL and the harmonic detection in the conventional harmonic compensation schemes are removed from the proposed interfacing converter digital controller. Also an accurate real and reactive power control is guaranteed by two PI regulators in the power control loop.

Note that this proposed control method using two decoupled terms can also be used to realize many other control objectives, which are traditionally challenging for conventional closed-loop control. In addition, this idea is extended to realize control of DG voltage and line current at different frequencies, as shown in the next chapter.

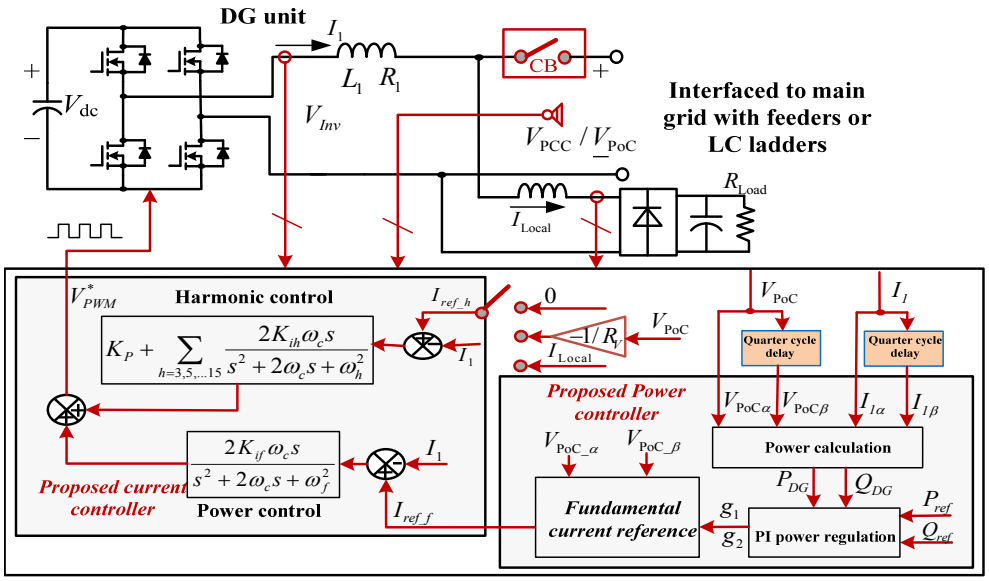


Fig. 4. 3. Diagram of an interfacing converter with the proposed control scheme.

4.2. Improved VCM for distribution system PCC harmonic voltage compensation

For microgrid applications, especially considering its autonomous islanding operation requirement, direct voltage support from interfacing converter is required. Unfortunately, CCM cannot directly provide voltage support to the system. Hence, the VCM based interfacing converter control methods are also proposed. To facilitate the sharing of load demand in an islanding microgrid with multiple DG units, VCM based on V-f droop control (real power-frequency droop and reactive power-voltage magnitude droop) is usually adopted to control the DG interfacing converters. In this case, DG unit interfacing converter can be controlled to emulate the behavior of synchronous generators. With VCM, virtual inertia [98] can be produced and it can be used to improve the transient performance of the power system. When DG unit is controlled to emulate synchronous generator, interfacing converters can also collaborate with real distributed synchronous generators.

Although VCM has unique advantage for islanding microgrid application, the harmonic compensation schemes which are traditionally used for APF applications cannot be directly implemented in the VCM controlled interfacing converters. This is mainly because VCM method does not have direct control of inverter line current. In order to overcome this limitation, a novel VCM based harmonic control method, which does not require line current tracking loops, is developed in this section. The proposed voltage controlled method is very flexible and it has similar compensation performance compared to the conventional current controlled compensation method.

The simplified equivalent circuit of a DG unit with VCM is shown in Fig. 4. 4, where the interfacing converter is interconnected to the PCC with an LC filter, and the filter capacitor voltage is controlled to integrate the DG system to grid. To ensure the stability of VCM operation, the inductive series feeder impedance Z_{feeder} between LC filter and PCC is required (This can be done by adopting transformers or additional coupling choke, if necessary). Note that for the interfacing converter with an LCL filter, the filter capacitor voltage can also be controlled, and the line side choke impedance is treated as a part of the feeder impedance. To simplify the discussion, the grid is represented as a voltage source V_{Grid} and the grid impedance Z_{Grid}. The harmonic current from the nonlinear load at PCC and can flow to either grid side or DG side, depending on how the interfacing converter voltage control strategy is. The DG interfacing converter controller using double-loop voltage scheme is shown in the lower part of this figure.

First, the power flow of the DG unit is regulated by the well-understood frequency and voltage magnitude control as

$$f_{DG} = f^* + D_P \cdot H_{LPF}(s) \cdot (P_{ref} - P_{Inst}) \tag{4-17}$$

$$E_{DG} = E^* + (D_q + \frac{k_E}{s}) \cdot H_{LPF}(s) \cdot (Q_{ref} - Q_{Inst}) \tag{4-18}$$

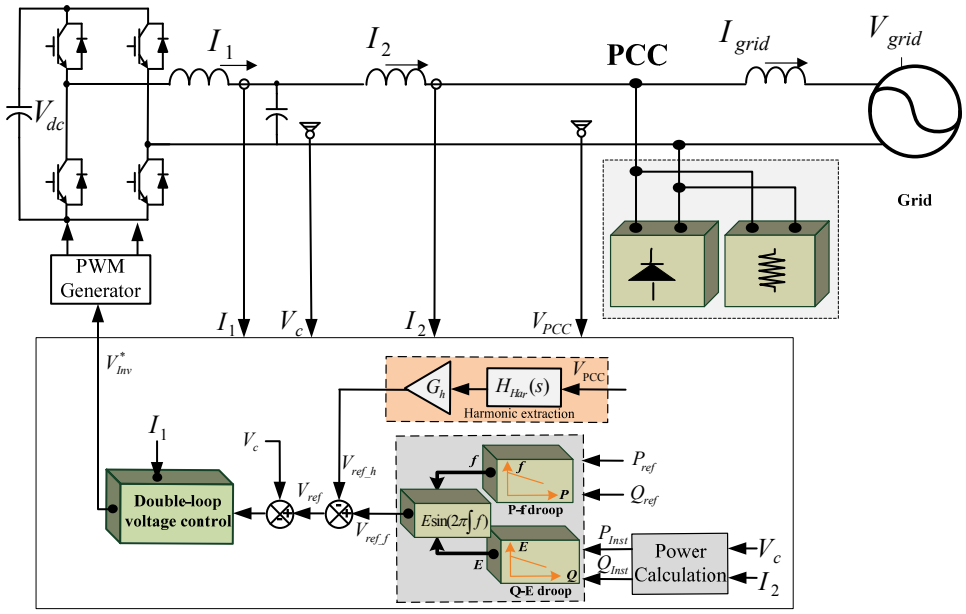


Fig. 4. 4. Diagram of an interfacing converter controlled by VCM.

where f^* and f_{DG} are the nominal and DG reference frequencies. E^* and E_{DG} are the nominal and DG reference voltage magnitudes. D_p and D_q are the droop coefficients for the real power and reactive power control, respectively. $H_{LPF}(s)$ in (4-17) and (4-18) is the low pass filter to reduce the ripples in the calculated instantaneous real and reactive DG power (P_{Inst} and Q_{Inst}). k_E in (4-18) is the integral gain, which ensures the steady-state reactive power tracking error during interfacing converter grid-connected operation. It should be noted that k_E needs to set to zero if the DG unit switches to autonomous islanding operation. For an islanding system with multiple DG units, the controllers in (4-17) and (4-18) can automatically set the frequency and voltage magnitude to an equilibrium point, which ensures power sharing between multiple interfacing converters without using any communication links between them. This control method is also often named as "*V-f* droop control" is the literature [51][52].

With the derived frequency and voltage magnitude reference, a ripple-free instantaneous voltage reference V_{ref_f} can be determined.

In the interfacing converter controller, the PCC harmonic voltage is also detected. The DG harmonic voltage reference V_{ref_h} is determined according to the PCC harmonic voltage V_{PCC_h} as

$$V_{ref\_h} = -G_h \cdot V_{PCC\_h} \tag{4-19}$$

where G_h is a gain which controls the PCC harmonic voltage at the harmonic order h. The DG unit interfacing converter can work under difference control mode by changing the value of the gain G_h .

With the derived fundamental and harmonic voltage references, the interfacing converter voltage reference V_{ref} is derived as

$$V_{ref} = V_{ref\_f} + \sum_h V_{ref\_h} \tag{4-20}$$

In the inner voltage tracking part, a wide bandwidth voltage controller shall be used to realize satisfied closed-loop *LC* filter capacitor voltage tracking. If the dynamics of inverter closed-loop voltage tracking is ignored, it can assume that the interfacing converter harmonic voltage V_{C_h} (the harmonic voltage of the LC filter capacitor) equals to the harmonic voltage reference V_{ref_h} as

$$V_{c\_h} = V_{ref\_h} \tag{4-21}$$

Afterwards, the equivalent harmonic impedance Z_{DG_h} of the entire DG unit (including DG unit feeder impedance) at PCC can be derived through simple manipulations as

$$\begin{aligned} I_{2\_h} &= (V_{C\_h} - V_{PCC\_h}) / Z_{feeder\_h} = -(1+G_h) V_{PCC\_h} / Z_{feeder\_h} \\ Z_{DG\_h} &= -V_{PCC\_h} / I_{2\_h} = Z_{feeder\_h} / (1+G_h) \end{aligned} \tag{4-22}$$

where I_{2_h} is the line harmonic current and Z_{feeder_h} is the harmonic impedance of the feeder between DG installation point and PCC. This equivalent impedance at harmonic frequencies is also shown in the left side of Fig. 4. 5.

From the above analysis, it is obvious that by properly controlling the interfacing converter harmonic voltage with a positive feedback gain of G_h , the

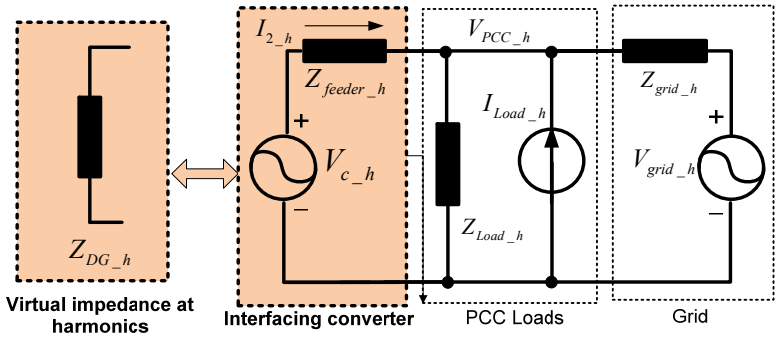


Fig. 4. 5. Simplified equivalent circuit at harmonic frequency.

DG unit harmonic impedance can be scaled down by a factor of $(1+G_h)$. Therefore, the harmonic impedance at DG side can be substantially lower than that at the grid side. As a result, most of the nonlinear load current is absorbed by the DG unit, leaving an improved grid current and PCC voltage. Obviously, a higher G_h value further reduces the PCC voltage harmonics.

With G_h =0, the system is a standard voltage controlled DG unit without any active compensation. The harmonic current can be shared automatically according to the DG side and grid side harmonic impedances. This is in contrast to the current controlled method, where the interfacing converter line current is sinusoidal if the active power filtering function is not enabled.

Furthermore, it is well known that the focus of *V-f* droop control of parallel DG systems is the fundamental power flow and therefore the DG line current is prone to have harmonic problems. If desired, this proposed method can also be used to control the inverter line current I_2 with lower harmonics and better THD to meet the present grid connection requirement. This can be done by using a negative feedback gain ($-1<G_h<0$), so that the DG equivalent impedance is increased at the harmonic frequencies. As a result, the PCC harmonic voltage is amplified compared to the conventional *V-f* droop control. Indeed, if inverter line harmonic current I_{2_h} can be properly attenuated with a negative G_h, the performance is similar to the conventional current controlled interfacing converter without any active harmonic compensation.

Therefore, with different compensation requirements or operation objectives, the value of G_h can be controlled adaptively (with a theoretical range from -1 to ∞). Since a high value of G_h tends to cause over modulation problems in the interfacing converter, a practical top limit of G_h should be selected carefully. Finally, it is important to note that G_h should not be less than -1, as this case introduces capacitive equivalent impedance, which may induce some additional system resonances. In this work, G_h >0 is named as harmonic compensation mode, G_h =0 is named as uncontrolled mode, and G_h <0 is defined as harmonic rejection mode.

4.3. Verification results

In order to verify the correctness of the proposed CCM and VCM strategies, comprehensive simulated and experimental results are obtained.

4.3.1. CCM based compensation scheme verification

- **Simulation results of CCM based interfacing converter with local nonlinear load**

First, the CCM controlled DG unit with a local diode rectifier load is tested in the simulation. The configuration of the system is the same as Fig. 4. 1 and PCC is connected to a stiff controlled voltage source (to emulate the main grid). The main grid voltage contains 2.8% 3rd and 2.8% 5th harmonic voltage. In this simulation, the reference power is set to 600W and 200Var. The detailed parameters of the system are provided in TABLE. 4. 1.

When the local load harmonic current is not compensated by the interfacing converter (corresponding to $I_{ref\_h} = 0$ in (4-15) and (4-16)), the performance of the interfacing converter is shown in Fig. 4. 6. It can be seen from Fig. 4. 6(b) that the converter output current is sinusoidal with 5.57% THD. At the same time, the harmonic load current flowing to the main grid is illustrated in Fig. 4. 6(a).

TABLE. 4. 1. Parameters in for a single-phase 230V/1KVA interfacing converter with CCM

System Parameter	Value
Single-phase grid voltage	Simulation 230V/50Hz Experiment 115V/50Hz
inverter filter	L_1=6.5mH (0.039pu), R_1=0.15Ω (0.003pu)
Grid feeder	L_{grid}=3.4mH (0.020pu), R_{grid}=0.15Ω (0.003pu)
LC ladder with five identical LC filter	L=1.0mH (0.006pu), C=25μF (0.42pu) for each LC filter
Sampling/Switching frequency	20kHz/10kHz
Power Control Parameter	**Value**
Real power control k_{p1}, k_{I1}	k_{p1}=0.00001, k_{I1}=0.001
Reactive power control k_{p2}, k_{I2}	k_{p2}=0.00001, k_{I2}=0.001
LPF time constant τ	0.0322 Sec
Current control Parameter	**Value**
Proportional gain k_p	48
Resonant gains k_{ih}	1500(h=f); 900 (h=3, 5, 7, 9); 600 (h=11, 13, 15)
R_V (for long feeder resonance mitigation)	5Ω

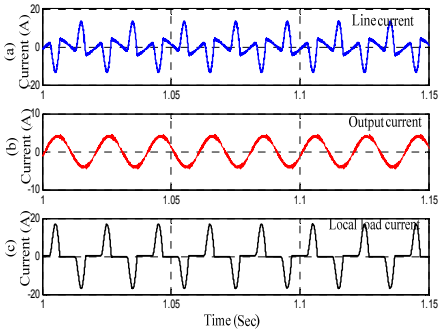


Fig. 4. 6. CCM interfacing converter during harmonic rejection. (a: line current I_2; b: output current I_1; c: local load current I_{Local}.)

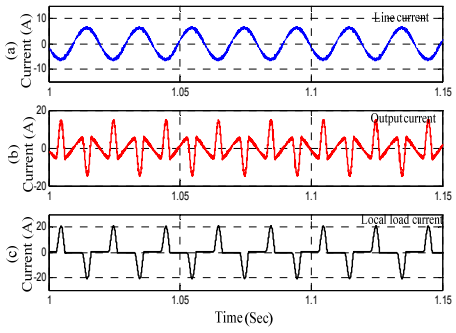


Fig. 4. 7. CCM interfacing converter during local harmonic compensation. (a: line current I_2; b: output current I_1; c: local load current I_{Local}.)

Once the local load harmonic current compensation is activated by setting $I_{ref\_h} = I_{Local}$ in the proposed method, the performance of the system is shown in Fig. 4. 7. Although harmonic extractions are not used in this simulation, the proposed method can still realize satisfied local load harmonic current

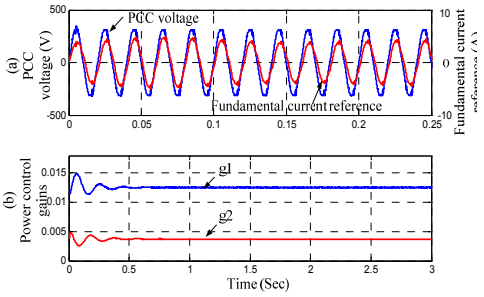


Fig. 4. 8. Power control reference during local load harmonic compensation. (a: PCC voltage and fundamental current reference I_{ref_f}, b: power control gains $g1$ and $g2$). (**Simulation**)

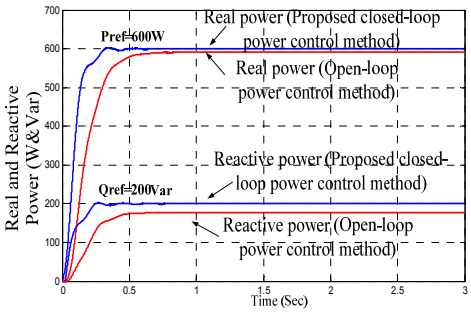


Fig. 4. 9. Power flow of the CCM based interfacing converter during local load harmonic current compensation. (P_{ref}=600W and Q_{ref}=200Var.) (**Simulation**)

compensation, resulting in an enhanced line current quality with 5.88% THD. Meanwhile, interfacing converter output current is polluted with 201.5% THD.

For the converter operating under local load harmonic compensation mode, its fundamental current reference adjusted by the proposed closed-loop power control scheme is shown in Fig. 4. 8(a). As the DG unit also provides 200Var reactive power to the grid, it can be seen that the fundamental current reference is slightly lagging of the PCC voltage.

The effectiveness of the proposed closed-loop power control strategy is verified in Fig. 4. 9, where the real and reactive power is calculated by (4-13) and (4-14). When the conventional open-loop power control schemed in (4-6) is applied, it can be noticed that the DG real and reactive power control is not accurate. On the other hand, as the proposed control strategy regulates DG output power in a closed-loop manner, it guarantees zero steady-state power tracking error.

- **Simulation results of CCM based interfacing converter with long underground feeder**

R-APF through voltage detection can be used to compensate different types of harmonic distortions. In this section, a DG unit installed at the end of a long feeder is considered for case study. To emulate the long feeder with nontrivial parasitic capacitance, an LC ladder five cascaded LC filters (see Fig. 4. 2) is connected between the utility mains and the DG unit. The inductance and capacitance of each LC filter is 1mH and 25μF, respectively. A single-phase diode rectifier is placed at the upstream of the feeder to excite some resonance. The performance of this system is shown from Fig. 4. 10 to Fig. 4. 14.

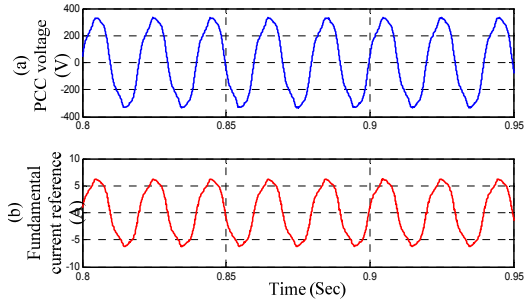


Fig. 4. 10. PoC voltage and the fundamental current reference for DG unit with long feeder under harmonic rejection control. (a: PCC voltage V_{PCC}; b: fundamental current reference I_{ref_f}.) (**Simulation**)

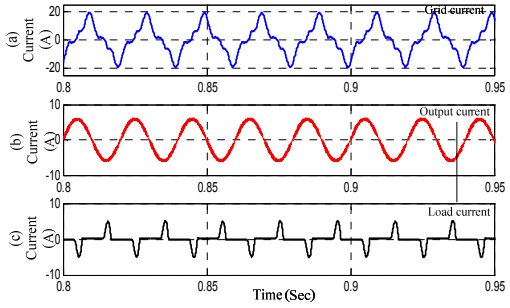


Fig. 4. 11. Performance of the DG unit with long feeder under harmonic rejection control. (a: grid current I_{grid}; b: inverter output current I_1; c: Load current I_{Load}.)) (**Simulation**)

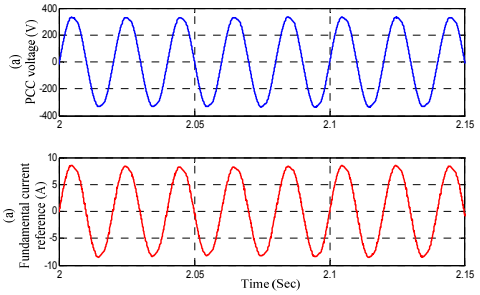


Fig. 4. 12. PoC voltage and its corresponding fundamental current reference during feeder resonance voltage compensation. (a: PoC voltage V_{PoC}; b: fundamental current reference I_{ref_f}.)(**Simulation**)

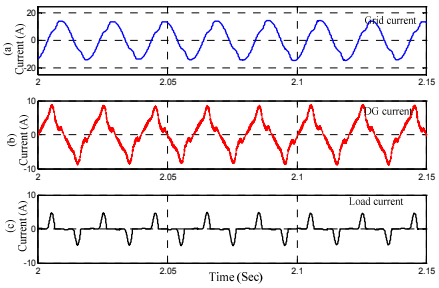


Fig. 4. 13. Performance of the DG unit during feeder resonance voltage compensation. (a: grid current I_{grid}; b: output current I_1; c: Load current I_{Load}.) (**Simulation**)

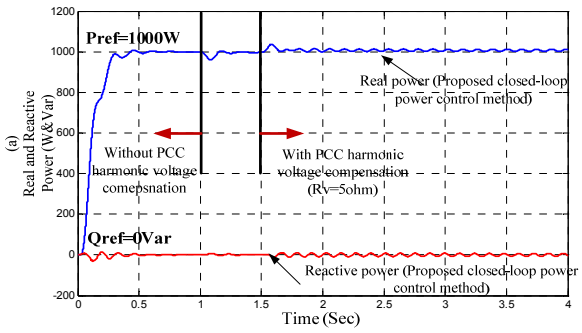


Fig. 4. 14. Power flow of the DG unit with LC ladder. (P_{ref}=1000W and Q_{ref}=0 Var). (**Simulation**)

The performance of the proposed current controller under harmonic rejection mode ($I_{ref\_h} = 0$) is given in Fig. 4. 10 and Fig. 4. 11. As shown in the upper part of Fig. 4. 10, the PoC voltage is distorted with 13.6% THD, due to the resonance aggregated in the LC ladder. Since the fundamental current (I_{ref_f}) is synchronized with the non-filtered PoC voltage and its orthogonal component, it is also distorted as presented in the lower part of Fig. 4. 10.

Although the fundamental current reference derived by (4-10) is distorted, it can be seen from Fig. 4. 11(b) that the inverter output current is sinusoidal with

5.61% THD. Meanwhile, the main grid current contains non-trivial harmonics with 34.2% THD.

When the feeder resonance voltage compensation is enabled by controlling the interfacing converter as a virtual resistance (*Rv*=5) at selected harmonic frequencies, corresponding responses of the system are shown in Fig. 4. 12 and Fig. 4. 13. In contrast to the performance in Fig. 4. 10, Fig. 4. 12 shows that the PoC harmonic voltage is mitigated and its THD reduces to 3.07%.

The associated current waveforms during feeder resonance voltage compensation are shown in Fig. 4. 13. It is obvious that inverter output current has more distortions (with 35.09% THD), while the main grid current THD reduces to 8.12%.

Finally, the power flow performance of the DG unit using the proposed power control scheme is shown in Fig. 4. 14. From the time range 0 sec to 1.0 sec, the DG unit is controlled to eliminate interfacing converter output current harmonics ($I_{ref\_h} = 0$). From 1.0 sec to 1.5 sec, feeder resonance voltage compensation is slowly activated by changing *Rv* from ∞ to 5Ω. It can be seen that the power control is always accurate during the transitions between different control modes.

- **Experimental results of CCM based interfacing converter with local nonlinear load**

Similar tests are also conducted in the laboratory prototype, where a single-phase *Danfoss* inverter is connected to a scaled down single-phase grid with 115V/50Hz voltage. The real-time code for the experiment is generated by dSPACE 1005.

First, the performance of the proposed CCM in addressing local load harmonic is tested. The detailed system configuration and parameters can be seen from Fig. 4. 1 and TABLE. 4. 1, respectively. In order to absorb the switching ripples of the inverter, a small shunt capacitor (2μF) is also connected at PCC.

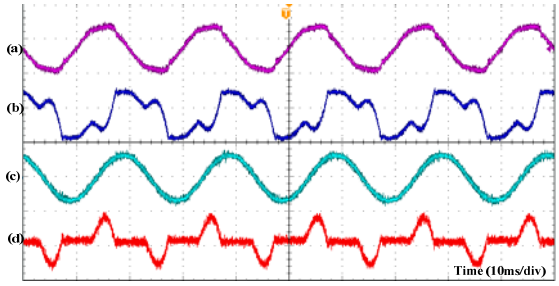


Fig. 4. 15. Performance with local nonlinear load. DG unit works under harmonic rejection mode (a: PCC voltage 250v/div; b: line current 10A/div; c: inverter output current 10A/div; d: local load current 10A/div.) (**Experiment**)

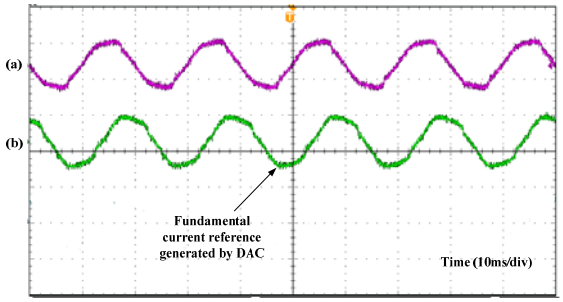


Fig. 4. 16. Performance with local nonlinear load. DG unit works under harmonic rejection mode. (a: PCC voltage 250v/div; b: fundamental current reference I_{ref_f} 10A/div.) (**Experiment**)

Fig. 4. 15 shows the performance of the interfacing converter operating in harmonic rejection mode, where the real and reactive power references are 200W and 500Var. Fig. 4. 15 (b) and (c) show that the inverter output current is sinusoidal and the local load harmonic current is pushed to the main grid side. In this case, the THDs of output current (I_1) and line current (I_2) are 5.16% and 41.73%, respectively. Meanwhile, due to the harmonic voltage drops on the grid feeder (L_{grid} and R_{grid}), the PCC voltage is also distorted with 9.49% THD.

By using the DAC (digital to analog converter) ports of dSPACE controller, the fundamental current reference during harmonic rejection operation is captured in the middle of Fig. 4. 16. As the fundamental current reference is derived from the combination of non-filtered PCC voltage and it conjugated component, it is also distorted. Nevertheless, thanks to the unique feature of the proposed controller, inverter output current is still sinusoidal.

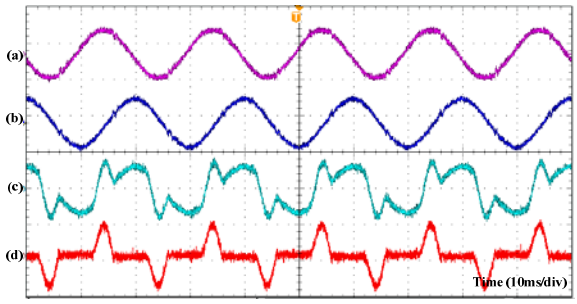


Fig. 4. 17. Performance with local nonlinear load. DG unit works under local load harmonic compensation mode. (a: PCC voltage 250v/div; b: line current 10A/div; c: inverter output current 10A/div; d: local load current 10A/div.) (**Experiment**)

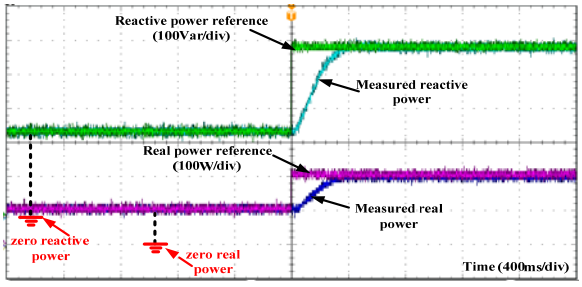


Fig. 4. 18. Real and reactive power flow using the proposed closed-loop power control method. (Under local nonlinear load compensation mode and the PoC voltage magnitude is reduced to 106V) (**Experiment**)

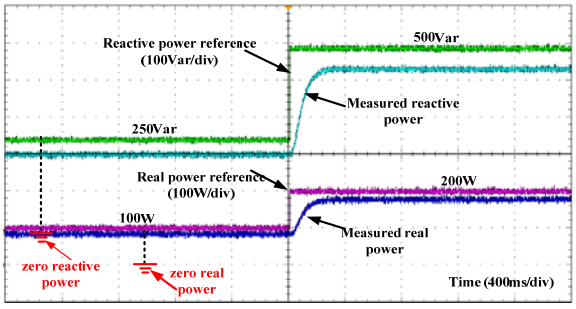


Fig. 4. 19. Real and reactive power flow using the conventional open-loop power control method in (1). (Under local nonlinear load compensation mode and the PoC voltage magnitude is reduced to 106V) (**Experiment**)

When the interfacing converter works at local load harmonic compensation mode, the corresponding performance of the system is shown in Fig. 4. 17. In this experiment, the measured local load current is directly employed as the input of the harmonic control branch. It shows that the local load harmonic current is compensated by the interfacing converter, resulted in an improved line current

(with 3.64% THD) in Fig. 4. 17(b). At the same time, the interfacing converter output current is polluted with 51.08% THD.

The real and reactive power control under harmonic compensation mode is also tested. To demonstrate the effectiveness of the proposed closed-loop power control method, the magnitude of main grid voltage is intentionally reduced to 106V. The performance using the proposed power control method is shown in Fig. 4. 18, where the real and reactive power references have a step jump from 100W/250Var to 200W/500Var. It is obvious that the proposed method maintains an accurate power tracking even when the main grid voltage varies.

The power control performance using the fundamental current reference in (4-1) is also illustrated in Fig. 4. 19. In this experiment, E^* in (4-1) is fixed to nominal voltage magnitude 115V. In contrast to the performance using the proposed closed-loop power control, the variation of main grid voltage magnitude introduces nontrivial steady-state real and reactive power control errors.

- **Experimental results of CCM based interfacing converter with voltage detection**

To produce some feeder resonance propagation, an LC ladder consists of five LC filter components is used as the feeder. The parameters of each LC filter are 1mH and 25μF. The corresponding performances are shown from Fig. 4. 20 to Fig. 4. 23.

In the first test, the interfacing converter works under harmonic rejection mode. Due to the disturbance of diode rectifier at the upstream of the LC ladder (see Fig. 4. 2), the voltages at different nodes of the LC ladder are distorted. Fig. 4. 20 shows the waveforms of the distorted voltages. The THDs of node 1, 3, and PoC voltage are 11.46%, 14.09%, and 17.03%, respectively. It proves that feeder voltage quality is sensitive to upstream nonlinear load disturbance when the conventional interfacing converter without active resonance damping control is installed at the end of a feeder.

During interfacing converter harmonic current rejection operation, the fundamental current reference is shown in Fig. 4. 21 (b). As the fundamental current is directly derived from the non-filtered PoC voltage, it is also distorted. Nevertheless, the interfacing converter output current in Fig. 4. 20(d) is still sinusoidal with 6.02% THD.

The performance of feeder resonance voltage mitigation using virtual harmonic resistance (*Rv*) is shown Fig. 4. 22 and Fig. 4. 23. In this case, a 5Ω harmonic virtual resistance is used in (4-16). Compared to the situation using harmonic rejection control, the control of virtual damping resistance can effectively mitigate voltage distortions in the LC ladder, leaving an enhanced voltage quality. The voltage THDs of node1, node3, and PoC are 7.49%, 5.54%, and 5.25%, respectively.

In the case of feeder resonance voltage mitigation, the fundamental current reference as shown in Fig. 4. 23(b) contains less distortion as compared to the case

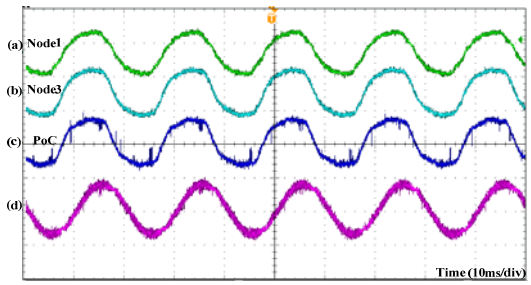


Fig. 4. 20. Performance with an upstream LC ladder. DG unit works under harmonic rejection mode. (a: node1 voltage 250v/div; b: node3 voltage 250v/div; c: PoC voltage 250v/div; d: Inverter output current 5A/div.) (**Experiment**)

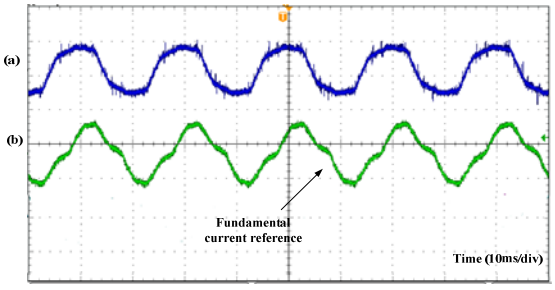


Fig. 4. 21. Performance with an upstream LC ladder. DG unit works under harmonic rejection mode. (a: PoC voltage 250v/div; b: fundamental current reference I_{ref_f} 5A/div.) (**Experiment**)

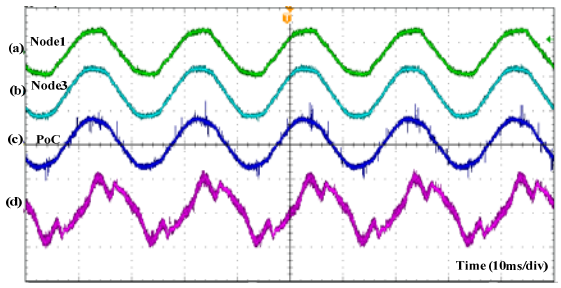


Fig. 4. 22. Performance with an upstream LC ladder. Interfacing converter works under harmonic compensation mode. (a: node1 voltage 250v/div; b: node3 voltage 250v/div; c: PoC voltage 250v/div; d: inverter output current 5A/div.) (**Experiment**)

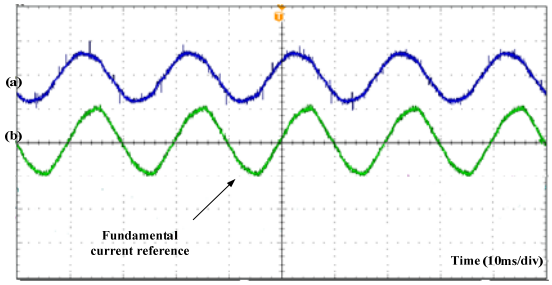


Fig. 4. 23. Performance with an upstream LC ladder. Interfacing converter works under harmonic compensation mode. (a: PoC voltage 250v/div; b: fundamental current reference I_{ref_f} 5A/div.) (**Experiment**)

in Fig. 4. 21(b). However, since the input of the harmonic control branch is not zero, it can be seen that the interfacing converter output current in Fig. 4. 22(d) is polluted with 28.25% THD.

4.3.2. VCM based compensation scheme verification

In addition to the performance of interfacing converter using CCM, the VCM based compensation method is also tested by simulation and experiments in a three-phase laboratory prototype. The results are shown in Fig. 4. 24, Fig. 4. 25, and Fig. 4. 26. The parameters of the setup can be seen in TABLE. 4. 2.

- **Simulated results of VCM based interfacing converter**

Fig. 4. 24 shows the results without any harmonic compensation. In this simulation, the interfacing converter LC filter capacitor voltage V_C (see Fig. 4.

4(b)) is controlled with pure sinusoidal voltage. In this case, the interfacing converter and grid share the nonlinear load current as can be seen from Fig. 4. 24 (c) and (d). Consequently, the PCC voltage is distorted due to the nonlinear currents through the grid impedance.

To improve the PCC voltage, harmonic compensation is implemented as shown in Fig. 4. 25(with G_5=12, G_7=12, G_{11}=5). As the DG equivalent harmonic impedance (Z_{DG_h}) at harmonic frequencies is reduced by a factor of $(1 + G_h)$, the interfacing converter absorbs most of the load nonlinear currents as can be seen in Fig. 4. 25(d). As a result, the grid current and PCC voltage are improved. Finally, the harmonic rejection mode is tested and the results are presented in Fig. 4. 26. As shown, with G_h=-1, the interfacing converter line current is controlled to be sinusoidal (see Fig. 4. 26(d)) due to the very high DG equivalent harmonic impedance at harmonic frequencies. In this case, the grid provides all nonlinear load current, and therefore the grid current and PCC voltage are further distorted compared to the harmonic uncontrolled mode in Fig. 4. 24.

The associated harmonic analysis of PCC voltages under different operation modes is provided in Fig. 4. 27. As shown, the PCC voltage has almost 6% 5th harmonic voltage and the THD is 6.72% when the conventional voltage control without any active PCC harmonic control is adopted in the interfacing converter. On the other hand, when harmonic compensation control is adopted, the 5th

TABLE. 4. 2. Parameters of a three-phase 104V/5KVA inverter controlled by VCM

Parameters	Simulations	Experiments
Grid voltage	104V, 60Hz (3 phase)	104V, 60Hz (3 phase)
DC link voltage	260V	260V
LC filter	L_1 = 1.25mH (0.219pu), C_f = 40μF (0.03pu)	L_1 = 1.25mH (0.219pu), C_f = 40μF (0.03pu)
DG Impedance	R_{feeder} = 1Ω (0.436pu), L_{feeder} = 5mH (0.873pu)	R_{feeder} = 1Ω (0.436pu), L_{feeder} = 5mH (0.873pu)
Grid impedance	R_{grid} = 1Ω (0.436pu), L_{grid} = 5mH (0.873pu)	R_{grid} = 1Ω (0.436pu), L_{grid} = 5mH (0.873pu)
Switching frequency	12kHz	12kHz
Power reference	P*=300W, Q*=125Var	P*=120W, Q*=75Var

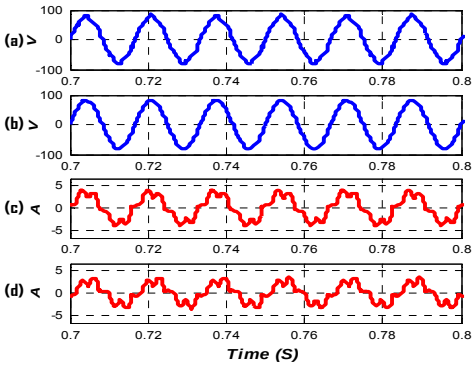


Fig. 4. 24. VCM based interfacing converter without compensation: (a) PCC phase voltage, (b) DG phase voltage, (c) grid current, (d) line current. (**Simulation**)

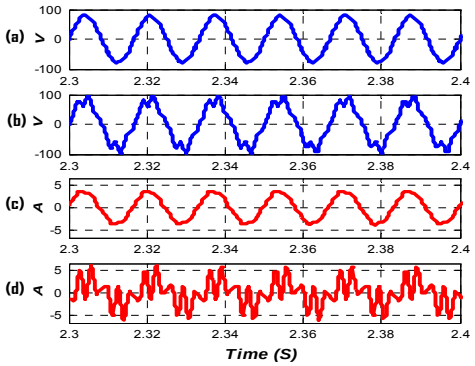


Fig. 4. 25. VCM based interfacing converter with PCC harmonic compensation: (a) PCC phase voltage, (b) DG phase voltage, (c) grid current, (d) line current. (**Simulation**)

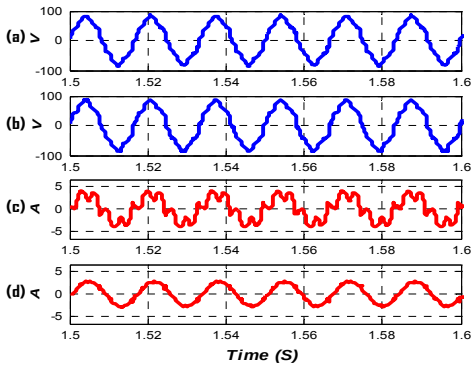


Fig. 4. 26. Voltage control method with harmonic rejection: (a) PCC phase voltage, (b) DG phase voltage, (c) grid current, (d) line current. (**Simulation**)

harmonic voltage at PCC is reduced to around 1.5% and the THD is reduced to 2.43%. Finally, the harmonic rejection mode introduces a further polluted PCC voltage with THD of 10.08%.

- **Experimental results of VCM based interfacing converter**

Experiments are also conducted on a three-phase grid-connected interfacing converter to verify the proposed VCM based PCC harmonic voltage compensation scheme. In the experiment, a three-phase programmable power supply is used to represent the grid, and the three-phase interfacing converter system is controlled by a DSP-FPGA platform.

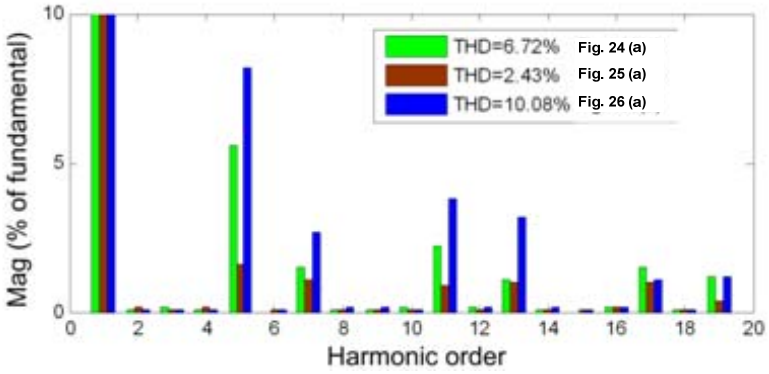


Fig. 4. 27. Harmonic analysis of PCC voltage (VCM). (**Simulation**)

The performance of the uncontrolled mode (without harmonic control) is shown in Fig. 4. 28, in which the interfacing converter and grid share the nonlinear PCC load current. Since the DG real and reactive power references are relatively small in the experiment, the grid current contains higher fundamental current. Without harmonic compensation, the THD of PCC voltage and grid current are 10.5% and 16.9% respectively.

When the PCC harmonic compensation is implemented (with G_5=7.5, G_7=3.4, G_{11}=0), the interfacing converter absorbs the nonlinear load current. As a result, both the grid current and PCC voltage are improved as shown in Fig. 4. 29. In this case, the THD of PCC voltage and grid current is improved to 5.2% and 6.6% respectively.

For the harmonic rejection mode, the interfacing converter line current is controlled to contain very few harmonics as the DG unit equivalent impedance increases significantly at the selected harmonic frequencies. It can be seen from Fig. 4. 30 that most of the nonlinear load current is supplied through the source, resulting in a further deteriorated PCC voltage. With harmonic rejection control, the THD of PCC voltage and grid current are 15.3% and 26.3% respectively.

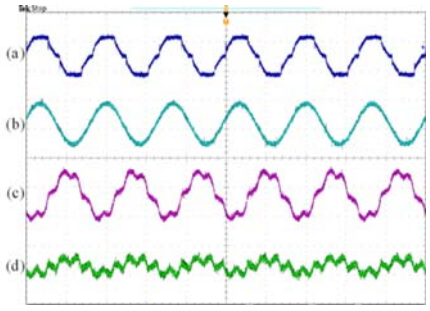


Fig. 4. 28. Voltage control method without harmonic compensation: (a) PCC line-to-line voltage (200V/div), (b) DG line-to-line voltage (200V/div), (c) grid current (5A/div), (d) DG current (5A/div). (**Experiment**)

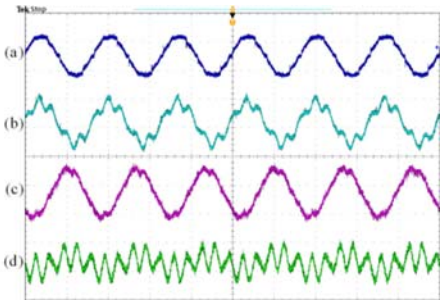


Fig. 4. 29. Voltage control method with harmonic compensation: (a) PCC line-to-line voltage (200V/div), (b) DG line-to-line voltage (200V/div), (c) grid current (5A/div), (d) DG current (5A/div). (**Experiment**)

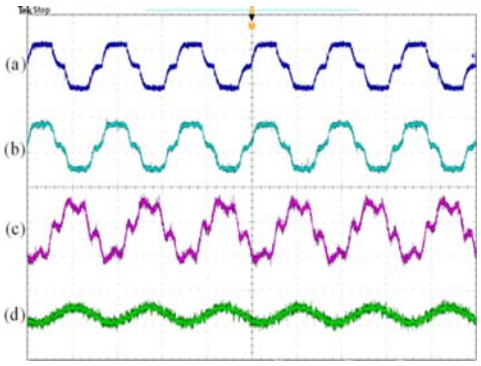


Fig. 4. 30. Voltage control method with harmonic rejection: (a) PCC line-to-line voltage (200V/div), (b) DG line-to-line voltage (200V/div), (c) grid current (5A/div), (d) DG current (5A/div). (**Experiment**)

4.4. Summary

This chapter proves that the interfacing converter can also be used to provide very flexible power line conditioning services. First, the current controlled interfacing converter is studied and an improved current control scheme with closed-loop power control is proposed. By using two well decoupled terms to realize fundamental and harmonic components tracking, the proposed method features many advantages compared to the conventional harmonic compensation methods. The first advantage is the reduced computational load. The proposed method can realize harmonic compensation without using any harmonic detection processes or phase-locked loops. Therefore, it is very suitable for low cost interfacing converter with limited computing capability. Additionally, this proposed method also ensures zero steady-state power control errors even when the harmonic compensation function is enabled in the interfacing converter.

Further considering that distributed power generation systems can be controlled to emulate the behavior of synchronous generator through voltage control, this chapter discusses the PCC harmonic voltage compensation scheme using voltage controlled interfacing converter. By deducting the harmonic voltage reference from the fundamental voltage reference, this proposed method can realize very flexible control of PCC harmonic voltage without having any closed-loop regulation of interfacing converter line current. Compared to the current controlled method that is only effective for grid-tied converters, this proposed control method can be used for both grid-tied and islanding applications.

Finally, inspired by the idea of fundamental and harmonic component tracking scheme in the proposed CCM, a hybrid control method for voltage and current tracking is proposed in this work, and is discussed in Chapter 5.

Chapter 5

Hybrid Voltage and Current Control Method to Improve DG Units Performance

Inspired by the previously proposed CCM with two decoupled control branches, a hybrid control method (HCM) is proposed in this chapter. The HCM realizes the control of DG fundamental voltage and line harmonic current at the same time. Accordingly, it is more flexible compared to CCM and VCM and it can be used to realize better harmonic compensation for both grid-tied and islanding power distribution systems. Additionally, the frequency adaptive HCM is also developed to address the impact of frequency deviation in a microgrid. Both simulated and experimental results verify the correctness of the proposed method.

5.1. The proposed HCM

Resonant controllers have a high gain at the selected frequency, and this gain decreases rapidly when the frequency is out of the bandwidth of a resonant controller. Due to this unique frequency selective feature, an improved CCM, which controls the fundamental and harmonic current tracking, has been applied to grid-connected interfacing converter as shown in Chapter 4. By using similar techniques, it is also possible to control the capacitor voltage and line current at

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Publications out of this chapter:

(1) J. He and Y. W. Li, "Hybrid Voltage and Current Control Approach for DG-Grid Interfacing Converters with LCL filters," IEEE Transactions on Industrial Electronics, vol. 60, pp. 1797-1809, May 2013.

(2) J. He, Y. W. Li, and F. Blaabjerg, "Flexible Microgrid Power Quality Enhancement Using Adaptive Hybrid Voltage and Current Controller," IEEE Transactions on Industrial Electronics, in press.

different frequencies.

For the VCM without any active harmonic compensation as shown in Chapter 4, the instantaneous voltage reference V_{ref} is almost ripple-free. This is because the droop control coefficients D_p and D_q in (4-17) and (4-18) are typically small and low pass filters are used in the DG real and reactive power calculation. Accordingly, it can be concluded that DG output power flow can be regulated through only fundamental capacitor voltage control using fundamental resonant controller. Considering that only interfacing converter line harmonic current regulation is needed to compensate power distribution system harmonics, corresponding harmonic resonant controllers can be used to realize this task.

With the above considerations, a hybrid voltage and current controller is proposed for interfacing converter with an LCL filter. It can be seen from (5-1) that the proposed controller has three parallel control branches as

$$\begin{aligned} V_{Inv}^{*} &= G_{Vol}(s)\cdot(V_{\text{ref}} - V_{\text{C}}) \\ &\quad + G_{Cur}(s)\cdot(I_{\text{ref}} - I_2) + G_{AD}(s)\cdot I_1 \end{aligned} \tag{5-1}$$

where the first term is responsible for controlling LCL filter capacitor voltage, the second term realizes closed-loop control of LCL filter line current, and the third term is a damping term, which measures the inverter output current I_1 to achieve active damping.

The voltage tracking controller in (5-1) is shown in (5-2) as

$$G_{Vol}(s) = \frac{2k_{if}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_f^{\,2}} \tag{5-2}$$

where k_{if} is the resonant controller gain in the voltage tracking controller. The purpose of term (5-2) is to control only the fundamental component of capacitor voltage, as the reference voltage V_{ref} derived from droop control contains only the fundamental voltage. It has been revealed that the proportional gain has very limited contribution to the voltage control dynamics and it is even removed in the

controller in [89]. Therefore, only fundamental frequency resonant controller is used for voltage tracking.

The second branch in (5-1) is the harmonic current control branch, which is described as

$$G_{\text{cur}}(s) = k_p + \sum_{h=3,5,..} \frac{2k_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + \omega_h^2} \tag{5-3}$$

where k_p is the proportional gain, $k_{ih}$is the resonant controller gain at the selected harmonic frequencies, ω_h is the angular frequency at the selected harmonic frequencies, ω_{ch} is the cut-off bandwidth, and h is the harmonic order.

The harmonic current controller in (5-3) is used to track the harmonic current reference. Considering that line current may have some non-characteristic harmonic compensation, a small proportional gain k_p is used in (5-3) to achieve better harmonic tracking.

Since there is no fundamental frequency resonant controller in (5-3) and the gain k_p is small, the regulation of line harmonic current and DG fundamental voltage are very well decoupled.

Finally, the controller in the third term is obtained as

$$G_{AD}(s) = k_{AD} \tag{5-4}$$

The major purpose of using this damping term is to provide good damping to the LCL filter resonance. This is similar to the internal impedance in the GCC scheme. In this case, the inverter output current is measured to realize the active damping.

Fig. 5. 1 is the diagram of a hybrid controller. It shows that three parallel branches are used in the controller, and they are responsible for filter capacitor fundamental voltage tracking, line current harmonic tracking, and LCL filter resonance damping, respectively.

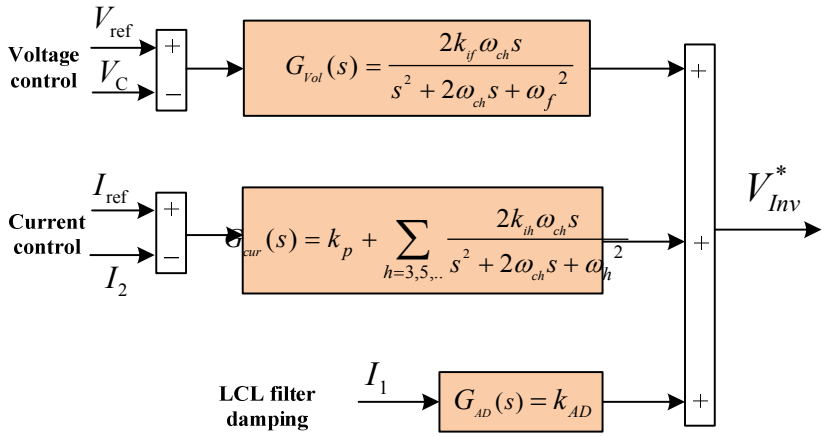

Fig. 5. 1. Diagram of a hybrid voltage and current controller.

5.2. Flexible operation of DG units using HCM

By using the proposed HCM, an interfacing converter can operate with great harmonic compensation flexibility when it is connected to a power distribution system, as shown in Fig. 5. 2. Furthermore, the transition between the grid-connected mode and islanding mode can be realized seamlessly. The details are described below:

- Local load harmonic compensation

The primary aim of using (5-3) is to control the line harmonic current. When the reference current I_{ref} is selected as the harmonic current I_{Local_h} of local load, this term controls the interfacing converter to compensate harmonics produced by local load, leaving an improved current injection I_{Inj} to PCC. The local load harmonic current is detected using a harmonic detector $H_{Har}(s)$ as

$$I_{Local,h} = H_{Har}(s) \cdot I_{Local} = \frac{s^2 + (\omega_f)^2}{s^2 + 2\omega_D s + (\omega_f)^2} \cdot I_{Local} \quad (5\text{-}5)$$

where I_{Local} is the local load current and $H_{Har}(s)$ is the harmonic component extractor with bandwidth ω_D.

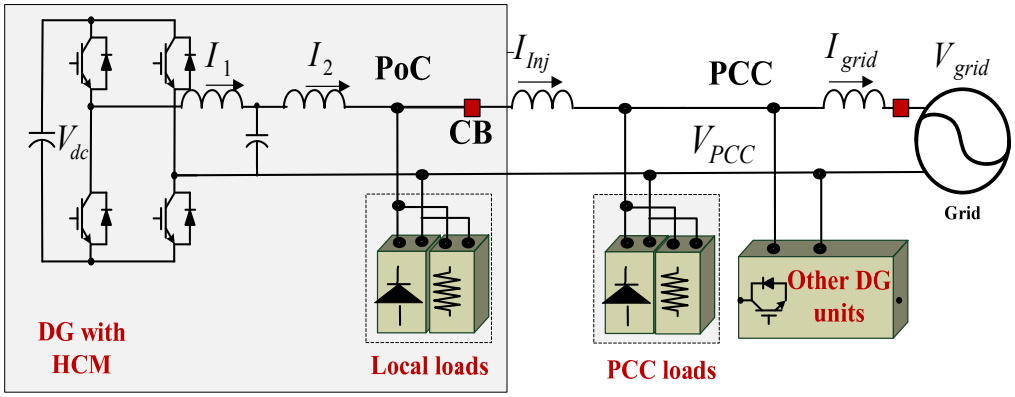

Fig. 5. 2. Simplified diagram of a DG unit connected to distribution system.

Further investigation finds that (5-3) has very small gain at the fundamental frequency. Hence, to realize the purpose of shunt active harmonic filtering, the measured local current I_{Local} can even be directly used as the reference current I_{ref} in (5-1) while without involving any harmonic extraction. This feature is similar to the CCM that has been proposed in Chapter 4.

- PCC harmonic voltage compensation

It should be pointed out that when the HCM is used to compensate local load harmonics, it cannot directly regulate the PCC voltage quality of the system. For instance, interactions between the shunt capacitor bank at PCC and inductive grid feeder may cause some PCC voltage distortions even when the local load harmonic current is properly compensated by the DG unit interfacing converter. To address this issue, the R-APF concept as discussed in Chapter 4 can also be realized by using the proposed HCM in a similar way.

First, the PCC harmonic voltage $V_{PCC,h}$ needs to be detected as

$$V_{PCC,h} = H_{Har}(s) \cdot V_{PCC} \tag{5-6}$$

where V_{PCC} is the PCC voltage. With the knowledge of PCC harmonic voltages, the reference current of HCM can be obtained as

$$I_{ref} = -V_{pcc,h} / R_V \tag{5-7}$$

where the coefficient R_V is designed to determine the reference current in the HCM. By using (5-7), the DG unit interfacing converter also works as a virtual damping resistor at the selected harmonic frequencies.

- Line current harmonic rejection

In addition to harmonic compensation ability, when I_{ref} in (5-1) is set to zero, it reduces interfacing converter line current harmonics. In this case, the steady-state performance is similar to that in an interfacing converter with conventional CCM.

Fig. 5. 3 illustrates a complete schematic diagram of a single-phase interfacing converter system. The converter is interconnected to PCC with an LCL filter and the local load is connected at the output terminal of LCL filter. The diagram of the controller is given in the lower part of Fig. 5. 3. It mainly consists of three control loops. The inner loop is the HCM controller, which has been given in Fig. 5. 1. The references of HCM are determined according to outer loop, intermediate loop, and system power quality enhancement task. The outer loop is the droop control which controls the output power of the DG unit through adjusting the voltage reference V_{ref_f} as

$$f_{DG} = f^* + D_P \cdot H_{LPF}(s) \cdot (P_{ref} - P_{Inst}) \tag{5-8}$$

$$E_{DG} = E^* + (D_q + \frac{k_E}{s}) \cdot H_{LPF}(s) \cdot (Q_{ref} - Q_{Inst}) \tag{5-9}$$

where f^* and f_{DG} are the nominal and DG reference frequencies. E^* and E_{DG} are the nominal and DG reference voltage magnitudes. D_p and D_q are the droop coefficients for the real power and reactive power control, respectively. k_E is the integral gain which ensures zero reactive power control errors for grid-tied interfacing converters at the steady-state. $H_{LPF}(\mathrm{s})$ in (5-8) and (5-9) is the low pass filter.

The droop control for VCM as shown in Chapter 4 is developed based on the assumption of inductive impedance between filter capacitor and PCC [87]. In

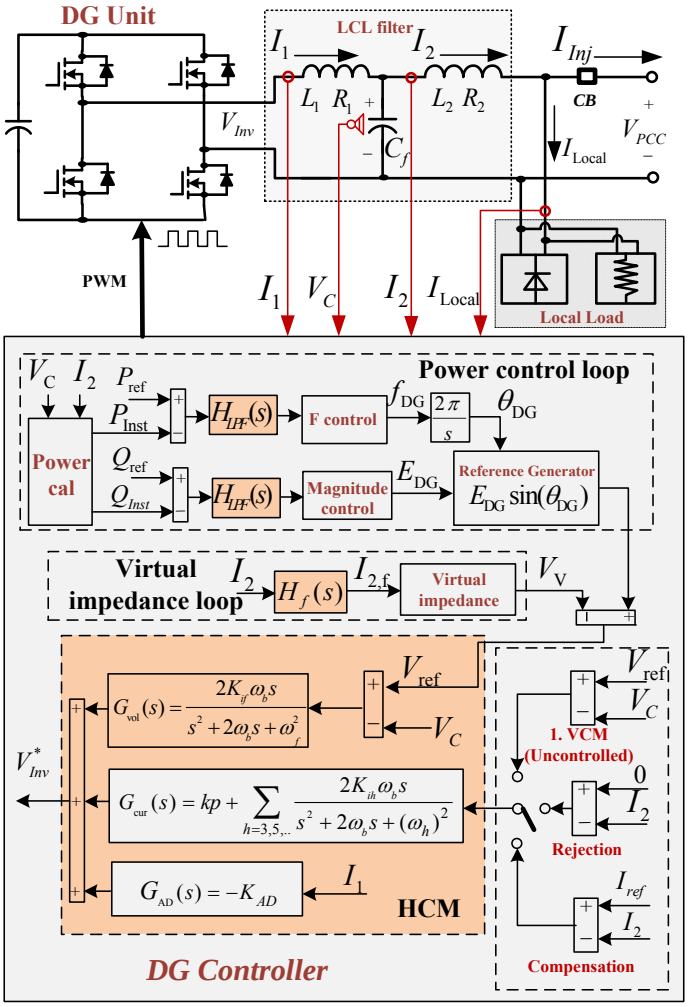

Fig. 5. 3. Diagram of interfacing converter controlled by HCM.

order to compensate the impacts of resistive feeder in some direct coupled DG units using output LC filters, inductive virtual series impedance is often produced through interfacing converter control [87] and [88]. This virtual fundamental frequency impedance control formulates the intermediate virtual impedance loop. To emulate the behavior of series impedance in a single-phase system, the corresponding voltage drop V_V shall be calculated as

$$V_V = R_{Vf} \cdot I_{2,f} - 2\pi f^* \cdot L_{Vf} \cdot I_{2,f\_delay} \tag{5-10}$$

where R_{Vf} and L_{Vf} are the virtual resistance and inductance produced by interfacing converter control. $I_{2,f}$ is the fundamental current and I_{2,f_delay} is obtained by delaying $I_{2,f}$ for quarter fundamental cycle.

The fundamental current $I_{2,f}$ in (5-10) is obtained as

$$I_{2,f} = H_f(s) \cdot I_2 = \frac{2\omega_D s}{s^2 + 2\omega_D s + (\omega_f)^2} \cdot I_2 \tag{5-11}$$

where $H_f(s)$ is a fundamental component detector realized by a band-pass filter with the bandwidth ω_D.

The voltage drop on the virtual impedance shall be deducted from V_{ref_f}, and the voltage reference for voltage control branch in HCM is determined as

$$V_{ref} = V_{ref\_f} - V_V \tag{5-12}$$

where V_{ref} is the revised voltage reference..

5.3. Modeling of interfacing converter with HCM

It is well understood that the conventional voltage and current controlled interfacing converter shall be modeled using Thevenin equivalent circuit and Norton equivalent circuit, respectively.

Since the proposed HCM provides an interfacing converter with unique hybrid voltage and current source features, the conventional Norton or Thevenin equivalent circuits cannot be directly applied to describe such a system. Instead, this section discusses a modified Thevenin and Norton equivalent circuits in Fig. 5. 4 and Fig. 5. 5 to address the modeling issues at the fundamental and harmonic frequencies.

First, similar to the analysis in Chapter 1, an LCL filter is presented in Fig. 5. 6, the filter impedances are expressed as $z1 = L_1 s + R_1$, $z2 = L_2 s + R_2$, and $zc = 1/(C_f s) + R_c$. Accordingly, the following matrix equation can be established according to Kirchhoff's laws as

$$\begin{bmatrix} V_C \\ I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \\ a_{31} & a_{32} \end{bmatrix} \cdot \begin{bmatrix} V_{Inv} & V_{PCC} \end{bmatrix}^T \tag{5-13}$$

where the coefficients a11 to a32 is expressed as

$$a11 = \frac{z2 \cdot zc}{z1 \cdot z2 + z1 \cdot zc + z2 \cdot zc},$$

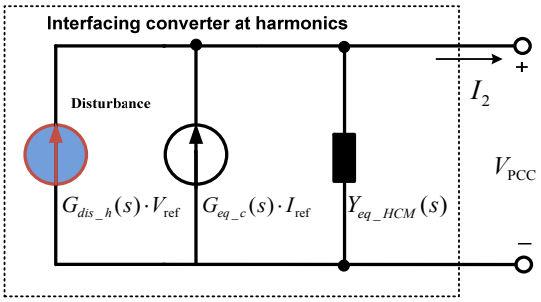

Fig. 5. 4. Modified Norton equivalent circuit for DG interfacing converter with HCM. (Valid at selected harmonic frequencies)

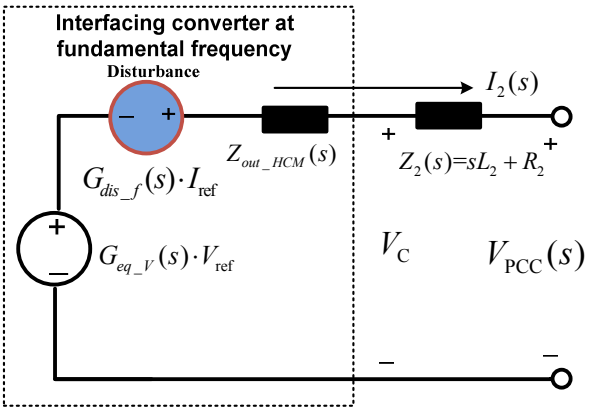

Fig. 5. 5. Modified Thevenin equivalent circuit for DG interfacing converter with HCM. (Valid at fundamental frequency)

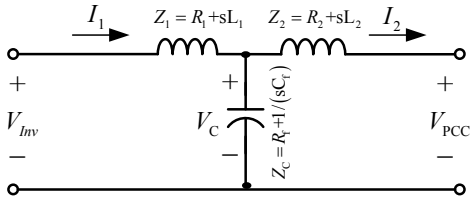

Fig. 5. 6. The diagram of an LCL filter.

$$a_{12} = \frac{z_1 \cdot z_c}{z_1 \cdot z_2 + z_1 \cdot z_c + z_2 \cdot z_c},$$

$$a_{21} = \frac{z_2 + z_c}{z_1 \cdot z_2 + z_1 \cdot z_c + z_2 \cdot z_c},$$

$$a_{22} = \frac{-z_c}{z_1 \cdot z_2 + z_1 \cdot z_c + z_2 \cdot z_c},$$

$$a_{21} = \frac{z_c}{z_1 \cdot z_2 + z_1 \cdot z_c + z_2 \cdot z_c},$$

and $a_{32} = \frac{-(z_1 + z_c)}{z_1 \cdot z_2 + z_1 \cdot z_c + z_2 \cdot z_c}$.

Through simple manipulations on (5-1) and (5-13), and assuming $V_{inv} = V_{inv}^*$, the closed-loop current source model can be derived as shown in (5-14) and Fig. 5. 4

$$I_2 = G_{eq\_c}(s) \cdot I_{\text{ref}} + G_{dis\_h}(s) \cdot V_{\text{ref}} - Y_{eq\_HCM}(s) \cdot V_{\text{PCC}} \tag{5-14}$$

where the coefficients $G_{eq\_c}(\text{s})$ and $G_{dis\_h}(\text{s})$ are the closed-loop gains of current and voltage references at harmonic frequencies. At the selected harmonic frequencies, the voltage reference V_{ref} shall be treated as a disturbance. $Y_{eq\_HCM}(\text{s})$ is the parallel admittance of the modified current source. The detailed expressions of the gains are shown as

$$G_{eq\_c}(s) = \frac{a_{31} \cdot G_{Cur}(s)}{1 + G_{Vol}(s) \cdot a_{11} + G_{Cur}(s) \cdot a_{31} - G_{AD}(s) \cdot a_{21}} \tag{5-15}$$

$$G_{dis\_h}(s)=\frac{a_{31}\cdot G_{Vol}(s)}{1+G_{Vol}(s)\cdot a_{11}+G_{Cur}(s)\cdot a_{31}-G_{AD}(s)\cdot a_{21}} \tag{5-16}$$

$$Y_{eq\_HCM}(s)=\frac{a_{31}\cdot[G_{\text{power}}(s)\cdot a_{12}+G_{\text{harmonic}}(s)\cdot a_{32}-G_{\text{damping}}(s)\cdot a_{22}]}{1+G_{Vol}(s)\cdot a_{11}+G_{Cur}(s)\cdot a_{31}-G_{AD}(s)\cdot a_{21}}-a_{32} \tag{5-17}$$

On the other hand, the interfacing converter needs to be modeled as a voltage source around the fundamental frequency. Accordingly, the PCC side LCL filter choke L_2 is considered as a part of the DG unit feeder. The response of an LC filter can be obtained as

$$\begin{bmatrix} V_C \\ I_1 \end{bmatrix}=\begin{bmatrix} b11 & b12 \\ b21 & b22 \end{bmatrix}\cdot\begin{bmatrix} V_{Inv} & I_2 \end{bmatrix}^{\mathrm{T}} \tag{5-18}$$

The coefficients b_{11} to b_{22} are expressed as

$$b_{11}=\frac{z_{\mathrm{c}}}{z_1+z_{\mathrm{c}}},\ b_{12}=\frac{-z_1\cdot z_c}{z_1+z_{\mathrm{c}}},\ b_{21}=\frac{1}{z_1+z_{\mathrm{c}}},\ \text{and}\ b_{22}=\frac{z_c}{z_1+z_{\mathrm{c}}}.$$

Similarly, through simple manipulations on (5-1) and (5-18), the closed-loop characteristic of a HCM controlled interfacing converter around fundamental frequency is given in (5-19)

$$\begin{aligned} &V_{\mathrm{C}}= \\ &G_{eq\_v}(s)\cdot V_{\mathrm{ref}}+G_{dis\_f}(s)\cdot I_{\mathrm{ref}}-Z_{out\_HCM}(s)\cdot I_2 \end{aligned} \tag{5-19}$$

where the coefficients $G_{eq\_v}(\mathrm{s})$ and $G_{dis\_f}(\mathrm{s})$ are the closed-loop gains of voltage and current references at fundamental frequency. Around the fundamental frequency, the current reference for line harmonic current regulation shall be treated as a disturbance. $Z_{out\_HCM}(\mathrm{s})$ is the series impedance of the modified voltage source circuit. The detailed expressions of the gains in (5-19) are shown as

$$G_{eq\_v}(s)=\frac{b_{11}\cdot G_{Vol}(s)}{1+G_{\mathrm{Vol}}(s)\cdot b_{11}-G_{AD}(s)\cdot b_{21}} \tag{5-20}$$

$$G_{dis\_f}(s)=\frac{b_{11}\cdot G_{Cur}(s)}{1+G_{Vol}(s)\cdot b_{11}-G_{AD}(s)\cdot b_{21}} \tag{5-21}$$

$$Z_{out\_HCM}(s)=\frac{b_{11}\cdot[G_{Vol}(s)\cdot b_{12}+G_{Cur}(s)-G_{AD}(s)\cdot b_{22}]}{1+G_{Vol}(s)\cdot b_{11}-G_{AD}(s)\cdot b_{21}}-b_{12} \tag{5-22}$$

- Bode Plot Analysis

In this subsection, the Bode plot of the coefficients in (5-14) and (5-19) are plotted to analyze the features of interfacing converter controlled by HCM.

Fig. 5. 7 shows the current tracking gains $G_{eq\_c}(\mathrm{s})$ in (5-14). In order to make the discussion more straightforward, the closed-loop gain $G_{eq}(s)$ of the interfacing converter using conventional double-loop current control is also presented for comparison. With the HCM, the closed-loop magnitude response of $G_{eq\_c}(\mathrm{s})$ is close to 0dB at the harmonic frequencies. It is obvious that the HCM has similar line current tracking gains compared to the conventional double-loop CCM ($G_{eq}(s)$) at the selected harmonic frequencies. It is important to note that the focus of Fig. 5. 7 is the harmonic frequencies, as the interfacing shall be modeled as a voltage source at the fundamental frequency.

The disturbance from the voltage reference (see (5-14)) is also examined in Fig. 5. 8. As shown, the disturbance ($G_{dis\_h}(\mathrm{s})$) has very small gain at the harmonic frequencies. Further considering that the voltage reference is obtained from droop control with very little harmonics, the input of voltage reference disturbance here can be ignored for line harmonic current tracking.

The effects of parallel admittances are obtained in Fig. 5. 9. It can be seen that both $Y_{eq}(s)$ using the conventional double-loop CCM and $Y_{eq\_HCM}(s)$ using the proposed HCM have limited gains at the selected harmonics. As a result, the line harmonic current control is not very sensitive to PCC voltage disturbances. If necessary, an additional compensator can be used to further alleviate the effects of parallel admittances [90].

Furthermore, the voltage source behavior of the HCM based interfacing converter around fundamental frequency is studied in Fig. 5. 10, Fig. 5. 11, and Fig. 5. 12. Note that the focus here is around the fundamental frequency. The response of the closed-loop voltage tracking gains is shown in Fig. 5. 10. As mentioned earlier, although the proportional gain k_p is removed from the voltage control branch $G_{Vol}(s)$ in (5-1), the closed-loop tracking gain $G_{eq\_v}(s)$ has similar performance compared to the counterpart $G_{eq}(s)$ using the traditional double-loop VCM. Consequently, the dynamics of the power control for an interfacing

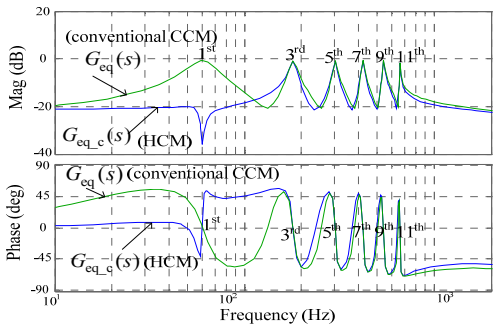

Fig. 5. 7. Bode plot of current tracking gains $G_{eq}(s)$ using conventional CCM and $G_{eq\_c}(s)$ using the proposed HCM. (Valid at selected harmonic frequencies)

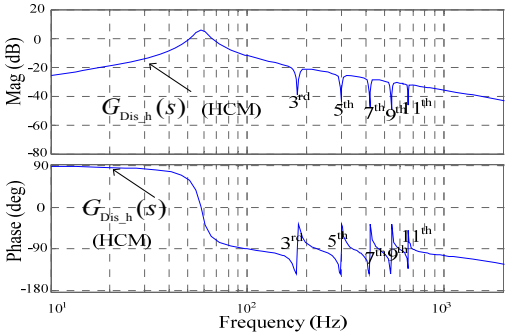

Fig. 5. 8. Bode plot of disturbance gain $G_{Dis\_h}(s)$ using the proposed HCM. (Valid at selected harmonic frequencies)

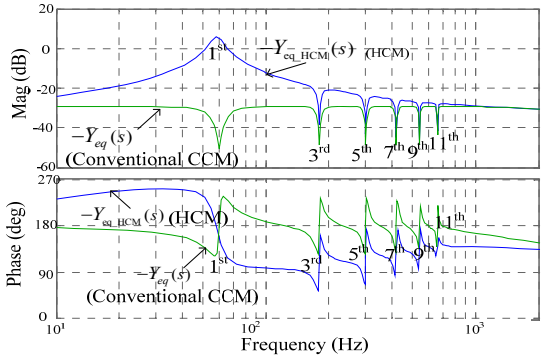

Fig. 5. 9. Bode plot of shunt admittance $(-Y_{eq}(s))$ using conventional CCM and $(-Y_{eq\_HCM}(s))$ using the proposed HCM.

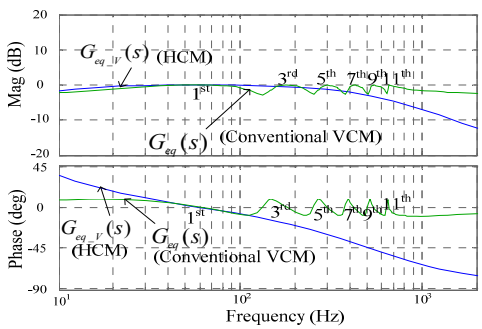

Fig. 5. 10. Bode plot of voltage tracking gains $G_{eq}(s)$ using conventional VCM and $G_{eq\_v}(s)$ using the proposed HCM. (Valid at fundamental frequency).

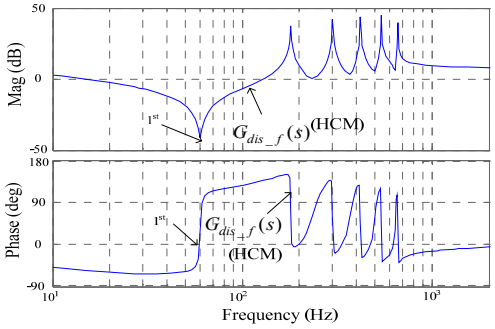

Fig. 5. 11. Bode plot of disturbance gain $G_{dis\_f}(s)$ using the proposed HCM. (Valid at fundamental frequency).

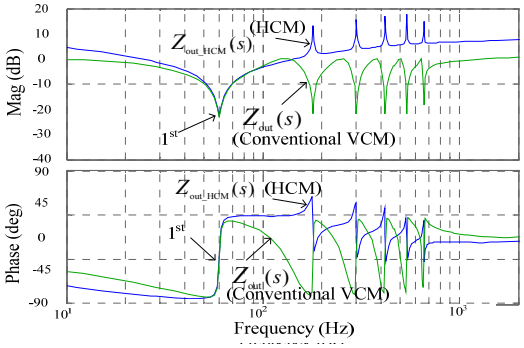

Fig. 5. 12. Bode plot of series output impedance $z_{out}(s)$ using conventional CCM and $z_{out\_HCM}(s)$ using the proposed HCM. *(*Valid at fundamental frequency*).*

converter with HCM shall be close to the conventional VCM. This conclusion is verified by the simulation and experimental results later in this chapter.

Around the fundamental frequency, the effects of current reference in HCM to capacitor fundamental voltage tracking are presented in Fig. 5. 11. It is clear that the disturbance has a very limited gain around 60Hz and the disturbance effect can therefore be ignored.

Finally, the series impedances $Z_{out}(s)$ with conventional double-loop VCM (13) and $Z_{out\_HCM}(s)$ with the proposed HCM are compared in Fig. 5. 12. It shows that these two impedances have similar responses around 60Hz.

The above analysis confirms that the interfacing converter with HCM can be modeled by two decoupled equivalent circuits (Fig. 5. 4 and Fig. 5. 5) at the fundamental and selected harmonic frequencies, respectively. For the control parameter design in HCM, the damping term shall be first tuned to realize a well dampened LCL filter plant, similar to the design criteria for the proposed GCC in Chapter 2. Then the voltage and current control terms can be designed for good reference tracking. Due to the decoupled nature of the fundamental voltage control (power control term) and harmonic current control (power quality control term), their control parameters can be tuned independently, as long as the gain k_p in (5-3) is selected to be small enough.

5.4. Adaptive HCM to compensate impact of frequency disturbance

The control of power converter under the situation of grid frequency disturbance has received increasing attentions in recent years. In [91], the adaptive frequency estimation method is proposed and the estimated grid frequency is used to improve the performance of direct power control scheme for grid-tied inverters. Additionally, the resonant controller [92] and reduced order generalized integrator [93] are also revised in order to alleviate the impacts of frequency deviations in the grid-tied inverter systems.

In this section, the HCM is also used to address the impact of variable frequencies in power system. This revised HCM provides very good frequency adaptive feature especially considering that HCM is recommended to be used in microgrid applications with more frequency deviations, such as the frequency dips causes by droop control [96]. Moreover, this section also shows that the complexity of interfacing controller can be reduced via flexible utilization of the

proposed adaptive HCM. At first, the conventional real power-frequency droop control is replaced by a PI regulator when DG unit works in the grid-connected mode. Thus, accurate steady-state real power control is achieved even when the microgrid frequency varies. In contrast to [91] and [92] where the phase-locked loops (PLL) or frequency-locked loops (FLL) are used to determine the frequency of the microgrid, the frequency reference obtained from power control loop is directly adopted as a time-varying parameter of the proposed HCM. With this arrangement, the line current control accuracy can be improved in a PLL-less manners. Moreover, the proposed adaptive HCM is further exploited to simplify the power control and virtual impedance control loops. Note that similar idea can also be applied to CCM and VCM to improve the performance of interfacing converter under grid frequency disturbances. The details of the proposed adaptive HCM are shown below.

- **Revised power control loop**

During the grid-connected operation, the real power control scheme using (5-8) can achieve zero steady-state real power control error only when the main grid frequency is fixed at the nominal value. TABLE. 5. 1 illustrates the allowed grid frequency ranges for interconnecting wind turbines in Denmark. It shows that wind turbines need to avoid shunting down when there are only small amount of frequency variations in the main grid voltage.

In order to ensure accurate real power control of grid-connected DG system under grid voltage frequency disturbances, a simple integral term is added to the conventional real power -frequency control scheme. Thus, the revised power loop control scheme becomes

$$f_{DG} = f^* + (D_p + \frac{k_f}{s}) \cdot H_{LPF}(s) \cdot (P_{ref} - P_{Inst}) \tag{5-23}$$

$$E_{DG} = E^* + (D_q + \frac{k_E}{s}) \cdot H_{LPF}(s) \cdot (Q_{ref} - Q_{Inst}) \tag{5-24}$$

where k_f is the integral gain for real power control. Similar to k_E for reactive power control, the gain k_f is only effective in grid-connected operation and it

TABLE. 5. 1. Requirement for integration wind turbines in Denmark [92].

Frequency Range	Clearing Time
Less than 47.0 Hz	0.3sec
From 47Hz to 47.5Hz	10sec
From 47.5Hz to 48.0Hz	5min
From 48.0Hz to 49.0Hz	25min
From 49.0Hz to 50.2Hz	Continuous operation
From 50.2Hz to 53.0Hz	1min
Higher than 53.0Hz	0.3sec

needs to be set to zero in DG unit islanding operation. Note that the droop control is inherently sensitive to the disturbance from the main grid, due to the low pass filters used in the power calculation stage. The aim of integral control in (5-23) is to ensure zero steady-state real power control errors when grid frequency drifts from the nominal value. It can be seen from [94] that the grid frequency deviation is typically slow even when the synchronous generator failure occurs in the power system. Consequently, the proposed method is capable of addressing frequency variations in the grid-tied microgrid.

- **Adaptive HCM**

In addition to power control loop, the conventional HCM as discussed in the previous section is also designed to compensate fixed frequency harmonics in a microgrid. Note that the bandwidth (ω_{ch}) of resonant controllers as illustrated in (5-2) and (5-3) can be adjusted to make the closed-loop DG voltage and current tracking less sensitive to grid frequency deviation. When the fundamental frequency of the microgrid varies, the frequency deviation of system harmonics is in proportion to their respective harmonic orders. Therefore, harmonic resonant controllers with wide bandwidth have to be adopted. However, wide bandwidth harmonic resonant controllers may cause additional coupling that may adversely affect the stability of the DG system.

To ensure accurate current tracking even under adverse frequency conditions, a few adaptive controllers were proposed before. However, they were mainly applied to CCM based grid-connected inverter, in which the existing PLL is ready to provide instantaneous frequency information. For the HCM based DG unit operating in a PLL-less manner, the adoption of additional PLLs increases the complexity of DG control system. On the other hand, it can be seen that the microgrid frequency information has already been reflected in the real power-frequency control scheme in (5-23). Indeed, to inject controllable real power to the microgrid, interfacing converter voltage must be synchronized with the microgrid voltage. In other words, the reference frequency in (5-23) always equals to the microgrid frequency at the steady-state. Based on this fact, the reference frequency f_{DG} can be directly adopted to construct adaptive resonant controllers. Accordingly, the voltage control and current control branches shall be updated as

$$G_{\mathrm{Vol}}(s) = \frac{2k_{if}\omega_{ch}s}{s^2 + 2\omega_{ch}s + (2\pi f_{DG})^2} \tag{5-25}$$

$$G_{Cur}(s) = kp + \sum_{h=3,5,7,9} \frac{2k_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + (h2\pi f_{DG})^2} \tag{5-26}$$

It has been demonstrated that the resonant controller can be implemented using the concept of Second Order Generalized Integrator (SOGI) [95]. For the implementation of adaptive HCM using SOGI, the diagram is presented in Fig. 5. 13. It shows that the reference frequency f_{DG} from (5-23) is used to realize the frequency adaptive capability of HCM.

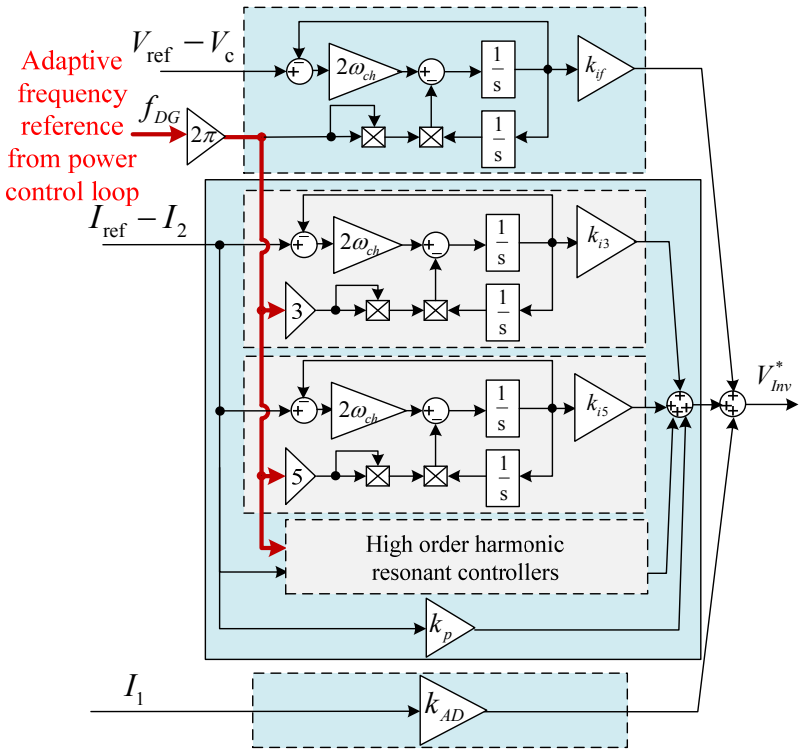

Fig. 5. 13. Implementation of frequency adaptive HCM using SOGI.

- **Controller complexity reduction**

With the revised power control loop in (5-23) and (5-24), and the adaptive HCM in (5-25) and (5-26), the control of the interfacing converters can be less sensitive to microgrid frequency variations. In this subsection, the control scheme is further simplified by removing some low/high pass filters in the power control and virtual impedance loops.

First, it can be noticed that the voltage reference V_{ref} from power control and virtual impedance loops are regulated by the voltage control branch of HCM, where only fundamental frequency resonant controller is adopted. Thus, the ripples in the voltage reference V_{ref} is automatically filtered out by $G_{vol}(s)$ in (5-25). Due to this feature, it is practical to remove the low pass filter in the

reactive power-voltage magnitude control scheme and the fundamental component extraction in the virtual impedance loop. This can be done by setting $H_{LPF}(s)$=1 in (5-24) and $H_f(s)$=1 in the virtual impedance control loop (see (5-10)).

In order to maintain an excellent closed-loop harmonic current tracking using adaptive HCM, it is better to suppress the ripples of f_{DG} in (5-25) and (5-26). Accordingly, the low pass filter is still necessary in the real power-frequency control in (5-23).

Note that, the aforementioned simplified power control and virtual impedance loops without low/band pass filters are only effective for the DG unit operating in local harmonic compensation mode and DG harmonic rejection mode. When HCM switches to conventional VCM (harmonic uncontrolled mode) mode, the input of current control branch can be set to $0 - V_C$ to reduce the filter capacitor voltage distortion.

The improved adaptive HCM control diagram is shown in Fig. 5. 14. As illustrated, it is also composed of three control loops. In the revised power control loop, the PI regulator is applied to maintain accurate real power control when microgrid frequency varies. Also, the low/band pass filters in the virtual impedance loop and the reactive power-voltage magnitude controller are removed in order to simplify the control system. Additionally, a set of adaptive SOGI based resonant controllers are adopted to form the HCM. The updates of adaptive DG controller compared to the conventional fixed frequency HCM controller are highlighted in Fig. 5. 14.

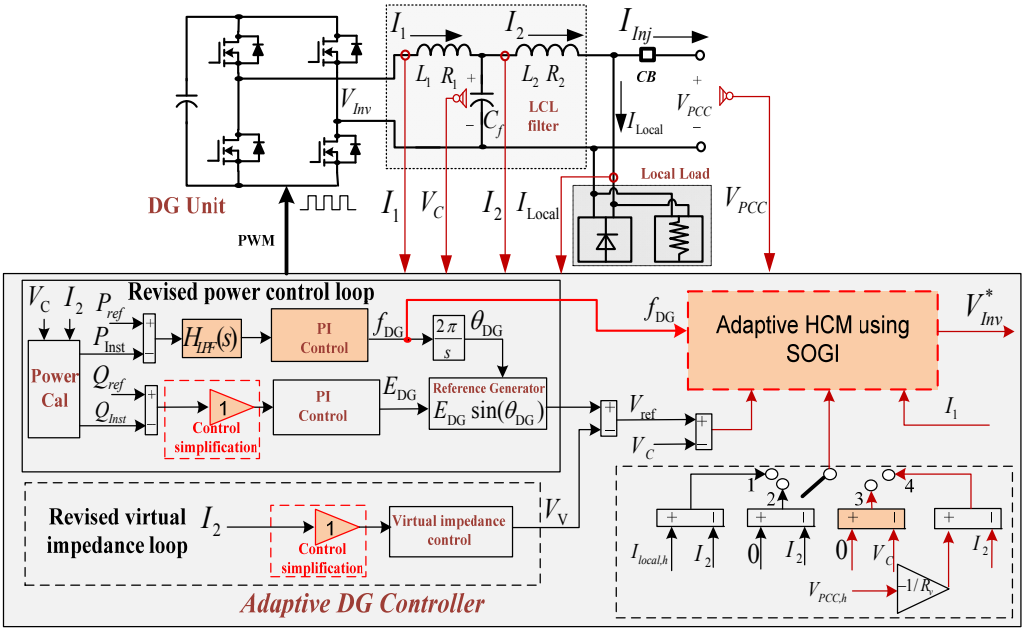

Fig. 5. 14. Diagram of frequency adaptive HCM.

5.5. Verification results

In order to verify the correctness of the proposed HCM, simulated and experimental results are obtained from a single phase DG unit.

5.5.1. Fixed frequency HCM verification

- **Simulated results**

The performances of interfacing converter using fixed frequency HCM are verified by both simulation and experiments. The parameters of the system are provided in TABLE. 5. 2.

At first, a single-phase grid-connected interfacing converter system is tested in the simulation. To make the comparison more obvious, a diode rectifier is adopted as the local load and a resistive load is employed as PCC load.

TABLE. 5. 2. Parameters for fixed frequency HCM verification on a single-phase 120V/1KW inverter

System Parameter	Value
LCL filter	L1=1mH (0.027pu), R1=0.5Ω (0.035pu),L2=0.6mH (0.016pu),R2=0.4Ω (0.028pu), Cf=15uF (0.082pu) and Rc=0.85Ω (0.059pu)
DC Link	180V/3000uF (16.36pu)
Switching frequency	12 kHz
Main grid	Single-phase 60V (RMS) /60Hz
Grid feeder	Lgrid=0.6mH (0.016pu) and Rgrid=0.4Ω (0.028pu)
HCM Parameter	**Value**
k_p	3.75
ω_{ch}	4rad/s
k_{ih}	312.5 (h=1,3), 250 (h=5,7,9), 150 (h=11)
Power Control Parameter	**Value**
Real power control D_P	1/628 (islanding and grid-connected, droop control)
Reactive power control D_Q	1/250 (islanding and grid-connected, droop control)
Reactive power control K_E	1/30 (grid-connected) 0 (islanding)

When the grid-connected converter is controlled with the conventional VCM, the harmonic load currents are shared by the main grid current I_{grid} and the interfacing converter line current I_2 as shown in Fig. 5. 15, where THDs of I_{grid} and I_2 are 31.62% and 53.17%, respectively. In this occasion, DG capacitor voltage is almost ripple-free with only 0.61% THD.

Fig. 5. 16 depicts the grid-connected converter performance when the HCM with local nonlinear loads compensation is applied (corresponding to $I_{ref} = I_{local}$ in HCM). As mentioned earlier, the harmonic extraction for conventional APFs is not used in this occasion. Since the local harmonic current is compensated by the DG unit and a linear load is placed at PCC, the main grid current I_{grid} is significantly improved with 6.85% THD. Meanwhile, the interfacing converter

line current is further pollution with 63.78% THD and the capacitor voltage THD is 2.90%.

Fig. 5. 17 demonstrates the performance of the system when the line harmonic current rejection (corresponding to $I_{ref} = 0$) is selected for the HCM. As illustrated, almost all the harmonic current are pushed to the main grid side and the THDs of I_{grid} and I_2 are 98.12% and 2.27%, respectively. At the same time, the capacitor voltage THD is 3.04%. This performance is similar to that of an interfacing converter controlled by the conventional CCM without power line conditioning, where resonant compensator significantly reduces line harmonic current.

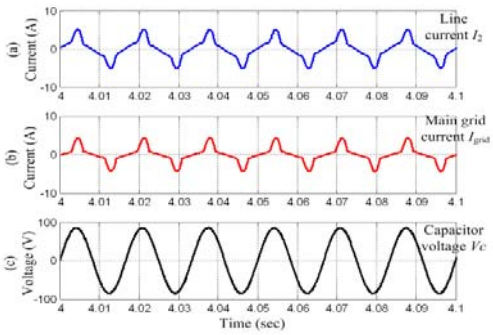

Fig. 5. 15. Performance of interfacing inverter with HCM (local harmonic compensation) (a: inverter converter line current; b: main grid current; c: DG voltage). (**Simulation**)

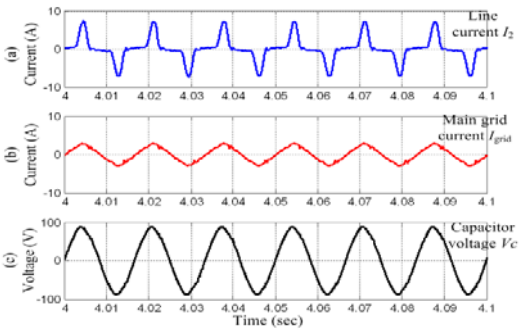

Fig. 5. 16. Performance of interfacing inverter with HCM (local harmonic compensation) (a: inverter converter line current; b: main grid current; c: DG voltage). (**Simulation**)

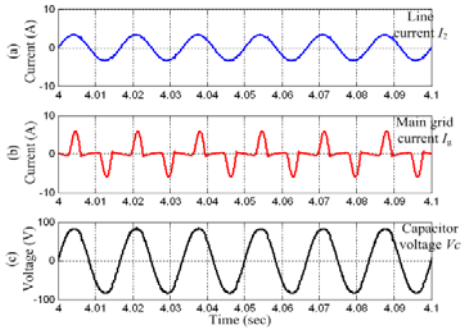

Fig. 5. 17. Performance of interfacing inverter with HCM (line harmonic rejection) (a: inverter converter line current; b: main grid current; c: DG voltage). (**Simulation**)

The power tracking performance of the DG unit with both VCM and HCM is shown in Fig. 5. 18, where the reactive power reference is 0 during the whole process while the real power reference has a step increase from 30W to 140W at 2.5sec. It can be seen that the response of power control using HCM is the same as that using VCM. Note that there is noticeable power coupling in Fig. 5. 18 and power tracking response are slow. This is mainly caused by the adoption of low pass filters in the power calculation/measurement and the slow integral control of reactive power error in the voltage magnitude control in (5-8).

To test the response of HCM controlled interfacing converter to current reference changes, simulated results are obtained in Fig. 5. 19. It shows the performance of the interfacing converter when the HCM switches from local

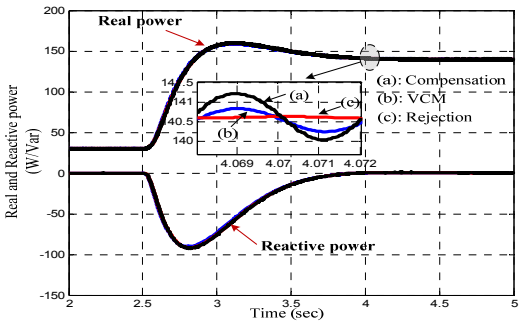

Fig. 5. 18. Power flow during real reference step increase. (**Simulation**)

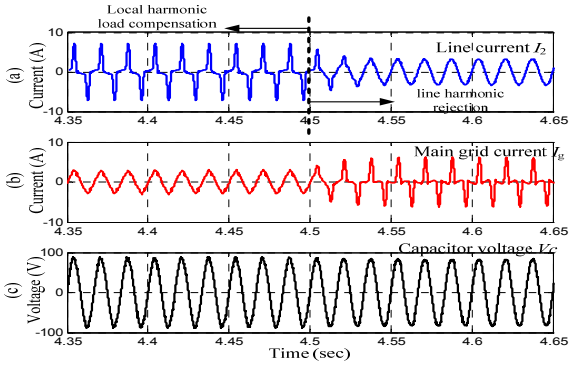

Fig. 5. 19. Control mode transfer performance in grid-connected operation. (a: DG line current; b: main grid current; c: DG voltage). (Transfer from local harmonic load compensation to line harmonic compensation at 4.5sec). (**Simulation**)

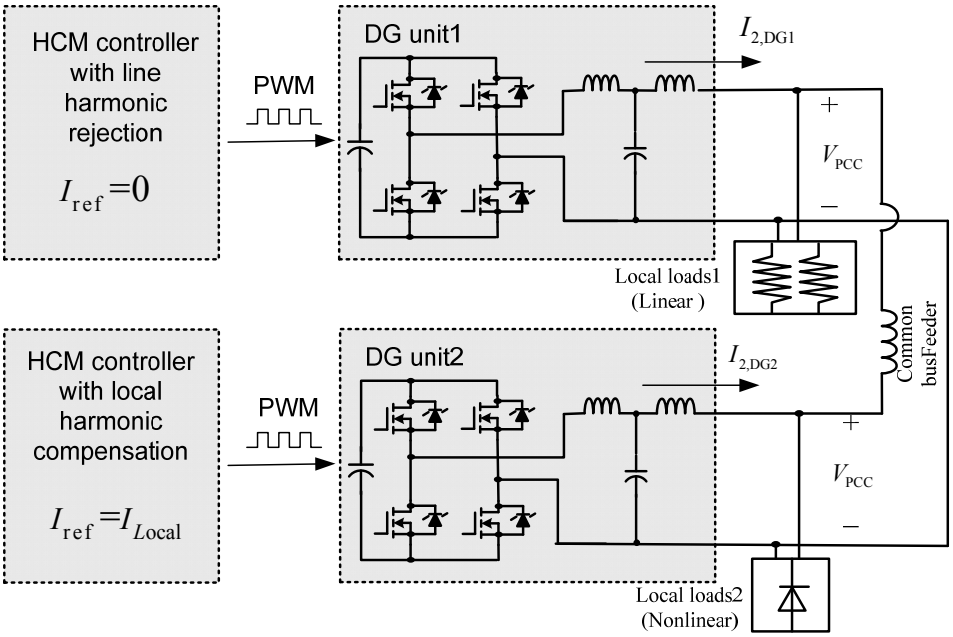

Fig. 5. 20. An islanding microgrid with two identical DG units. (DG1 controlled with line harmonic rejection; DG2controlled with local harmonic load compensation)

harmonic load compensation mode to line harmonic current rejection mode at 4.5sec.

The performance of HCM controlled interfacing converter in an islanding microgrid is also examined by the simulation. As shown in Fig. 5. 20, the islanding system consists of two DG units at the same power rating. A linear load is connected to DG1 and the nonlinear load is placed at DG2 terminal. In this case, the line current control objective of DG1 is to reduce its harmonic current by setting $I_{ref} = 0$, and DG2's task is to compensate its local harmonic current using $I_{ref} = I_{Local}$ in the fixed frequency HCM.

The output power of these islanded DG units during a sudden increase of loads is shown in Fig. 5. 21. Similar to the islanding microgrid with the conventional VCM, it can be seen that proper power sharing can always be maintained.

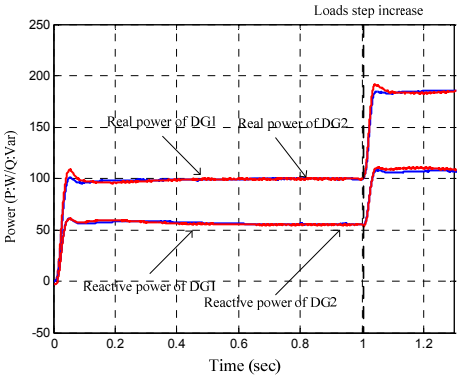

Fig. 5. 21. Power sharing in islanding DG units. (**Simulation**)

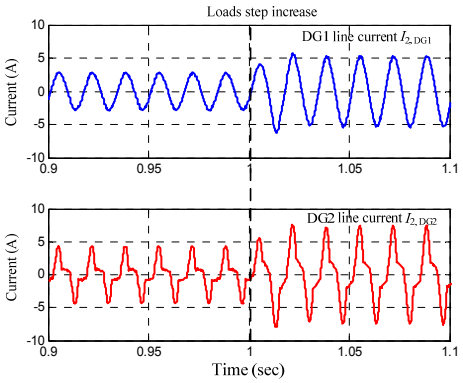

Fig. 5. 22. Line currents of DG units during loads variation. (**Simulation**)

The associated line currents of these two DG units are shown Fig. 5. 22. It is obvious that the loads current harmonics are absorbed by DG2 (THD=44.32%) and the line current of DG1 contains very little harmonics (THD=2.25%).

- **Experimental results**

The experimental results are presented to verify the proposed HCM in grid-connected operation. First, Fig. 5. 23 shows the operation of an interfacing converter using the VCM. In this situation, the load harmonic current is shared by the DG unit and the main grid according to their respective harmonic impedances.

The steady-state performance of the DG unit using HCM has also been confirmed as presented in Fig. 5. 24 and Fig. 5. 25. In Fig. 5. 24, the interfacing converter works at the harmonic rejection mode. As a result, the local load harmonic current is pushed to the main grid side. When the interfacing converter with harmonic compensation is tested in Fig. 5. 25, the majority of the local load harmonic current flows to the DG unit side. Accordingly, the power quality of main grid current is improved. It can be noticed that the main grid current still contains some 2nd and 3rd harmonic currents, as shown in Fig. 5. 25. This phenomenon is mainly caused by the measurement errors and the effects of parallel admittance $Y_{eq\_HCM}(s)$ in the low-power prototype [90].

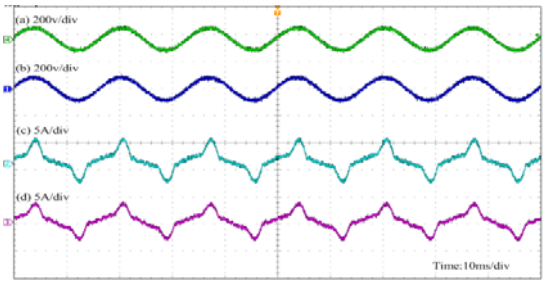

Fig. 5. 23. Experimental waveforms of grid-connected DG with VCM (a: PCC voltage; b: filter capacitor voltage; c: main grid current; d: DG line current). (**Experiment**)

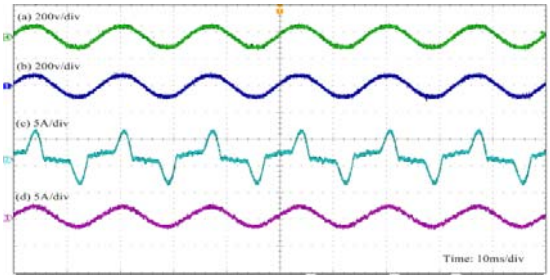

Fig. 5. 24. Experimental waveforms of grid-connected DG with HCM (Line harmonic currents rejection. a: PCC voltage; b: filter capacitor voltage; c: main grid current; d: DG line current). (**Experiment**)

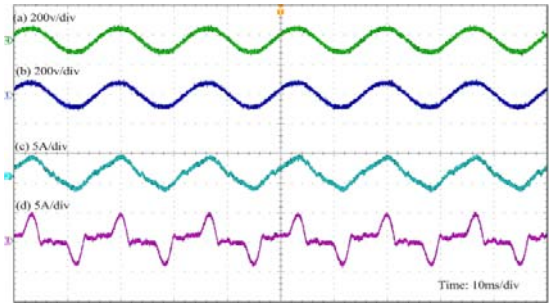

Fig. 5. 25. Experimental waveforms of grid-connected DG with HCM (Local harmonic currents compensation. a: PCC voltage; b: filter capacitor voltage; c: main grid current; d: DG line current). (**Experiment**)

5.5.2. Adaptive HCM verification

To evaluate the performance of the proposed adaptive HCM during system frequency deviations, comprehensive simulated and experimental results are obtained from a scaled 50Hz single-phase microgrid. In the experimental

verification part, the DC link voltage of each DG unit is provided by an isolated high voltage DC supply from Delta Electronics, and the control code is generated by dSPACE 1005 and its peripheral FPGAs.

- **Islanding Operation**

The effectiveness of the proposed adaptive HCM has been verified in an islanding microgrid with two DG units at the same power rating. Nevertheless, their interfacing converters are connected to PCC with different feeders. Fig. 5. 26 shows the configuration of the single-phase islanding microgrid and TABLE. 5. 3 illustrates key parameters of this system.

First, the fixed frequency HCM is applied to interfacing converter. In this case, HCM works in harmonic uncontrolled mode by setting the input of the current control branch as $(V_{ref} - V_C)$. Also, low pass filter and fundamental component extractor are used in the power control and virtual impedance control loops, respectively. Note that the virtual series impedance is only produced in DG1, in order to improve the reactive power sharing accuracy. The performance of the islanding system is shown in Fig. 5. 27. It can be seen that the voltages of DG1 and DG2 are sinusoidal and their THDs are 2.85% and 2.41%, respectively.

To demonstrate the impact of low pass filter (5-9) and fundamental component extractor (5-27) in the conventional fixed frequency HCM, the

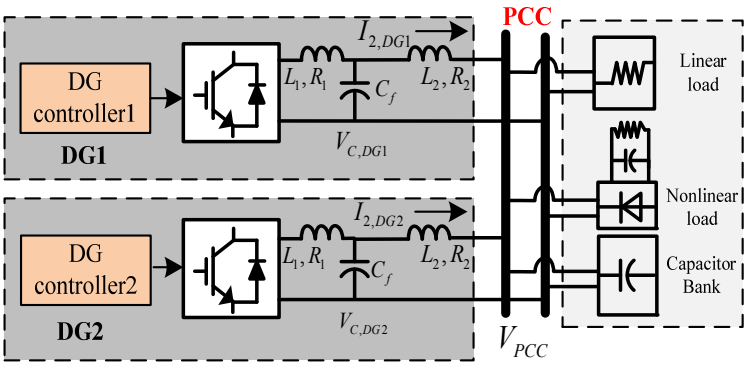

Fig. 5. 26. Experimental single-phase islanding microgrid with two DG units.

performance without using them in DG1 is also tested. The corresponding waveforms are shown in Fig. 5. 28, where it can be seen that DG1 voltage has some distortions with 5.61%THD. At the same time, DG2 voltage is still sinusoidal.

The performance of using the proposed frequency adaptive HCM is given in Fig. 5. 29. In this situation, both of the DG units work under harmonic uncontrolled mode by setting the input of the current control branch as $(0 - \mathrm{V_C})$. The fundamental component extraction in the virtual impedance loop and the low pass filters in the reactive power-voltage magnitude control are removed from these DG units. As expected, the voltages of DG1 and DG2 are all sinusoidal with 2.91% and 2.48% THDs, respectively. However, due to the interactions between PCC shunt capacitor bank and DG unit LCL filters, it can also be noticed that the

TABLE. 5. 3. Parameters for adaptive HCM verification (islanding operation) on single-phase inverters (120V/1KVA)

DG Units Circuit Parameters	Value
Output inductor L_1 and R_1	DG1&DG2:1.5mH (0.033pu) and 0.05Ω (0.003pu)
Feeder inductor L_2 and R_2	DG1:3.0mH (0.065pu) and 0.1Ω (0.006pu) DG2:6.5mH (0.142pu) and 0.2Ω (0.012pu)
Filter capacitor C_f	DG1&DG2: 25uF (0.112pu)
Rated voltage f^* and E^*	50Hz and 110V (RMS)
DC link voltage V_{dc}	DG1&DG2: 250V
Switching/Sampling Frequency	10kHz
Power Control & Virtual Impedance Loops Parameters	Value
D_P and K_f	DG1&DG2:1/3450 and 0
D_Q and K_E	DG1&DG2:1/550 and 0
ω_{LPF}	35rad/s
L_{Vf} and R_{Vf}	DG1:3.5mH (0.076pu) and 0.1Ω (0.006pu) DG2:0mH (0pu)and 0Ω (0.0pu)
HCM Control Parameters	Value
k_{if}	700
k_p	2.4
k_{ih}	500(h=3,5,7); 300(h=9)
ω_b	2rad/s
k_{AD}	-20
ω_D	62.8rad/s

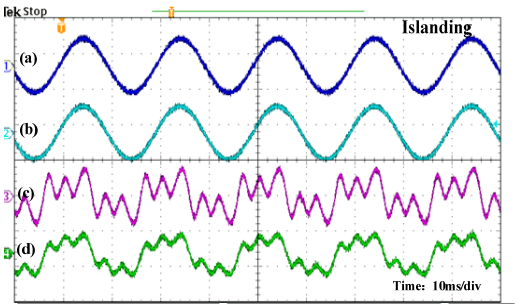

Fig. 5. 27. Performance of fixed frequency HCM operating in harmonic uncontrolled mode . (a: DG1 voltage 250V/div; b: DG2 voltage 250V/div; c: DG1 line current 10A/div; D: DG2 line current 10A/div.) (**Experiment**)

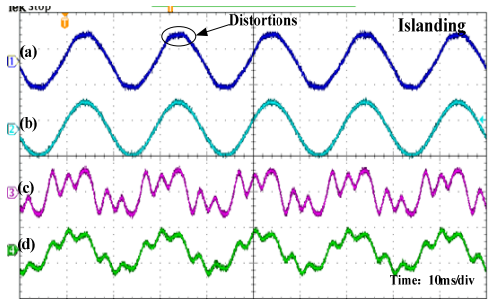

Fig. 5. 28. Performance of fixed frequency HCM operating in harmonic uncontrolled mode. (with simplified power control and virtual impedance control loops) (a: DG1 voltage 250V/div; b: DG2 voltage 250V/div; c: DG1 line current 10A/div; D: DG2 line current 10A/div.) (**Experiment**)

PCC voltage has nontrivial distortions with 17.63% THD.

The sharing of the load current corresponding to Fig. 5. 29 is shown in Fig. 5. 30. It has been pointed out in that the DG units working in VCM (harmonic uncontrolled mode) share PCC harmonic load according to the ratio of their respective feeder harmonic impedance (L_2 and R_2). As interfacing converters in this microgrid have mismatched harmonic feeder impedances, there are some harmonic circulating currents among the DG units. Fig. 5. 30(c) shows the difference between DG line currents ($I_{2,DG1}-I_{2,DG2}$).

To improve the PCC voltage quality of this islanding micrgorid, the adaptive HCM switches to PCC harmonic voltage compensation mode and the coefficient R_V is set to 3.5Ω in both of the DG units. Compared to the performance in Fig. 5. 29, the PCC harmonic voltage in Fig. 5. 31 is effectively compensated and the PCC voltage THD reduces to 6.69%.

Additionally, the sharing of load current under PCC harmonic voltage compensation mode is given in Fig. 5. 32. It shows that the difference between DG1 and DG2 line currents ($I_{2,DG1}-I_{2,DG2}$) is reduced compared to its counterpart in Fig. 5. 30(c).

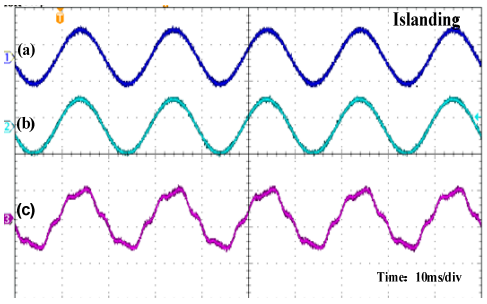

Fig. 5. 29. Performance of adaptive HCM operating in harmonic uncontrolled mode. (a: DG1 voltage 250V/div; b: DG2 voltage 250V/div; c: PCC voltage 250V/div.) (**Experiment**)

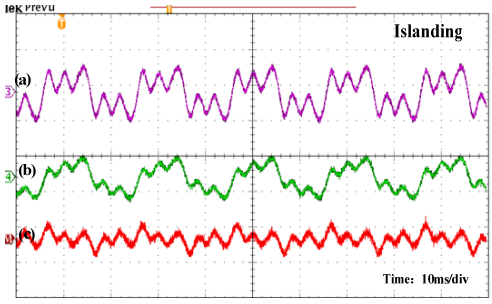

Fig. 5. 30. Performance of adaptive HCM operating in harmonic uncontrolled mode. (a: DG1 line current 10A/div; d: DG2 current line 10A/div; c: current difference 10A/div.) (**Experiment**)

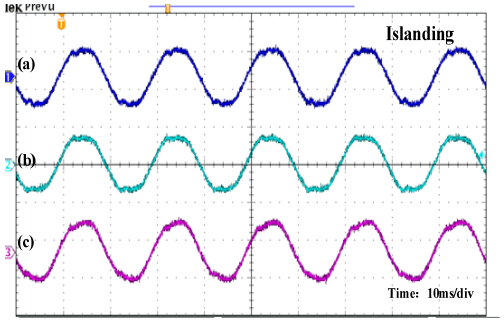

Fig. 5. 31. Performance of adaptive HCM operating in PCC harmonic compensation mode. (a: DG1 voltage 250V/div; b: DG2 voltage 250V/div; c: PCC voltage 250V/div.)(**Experiment**)

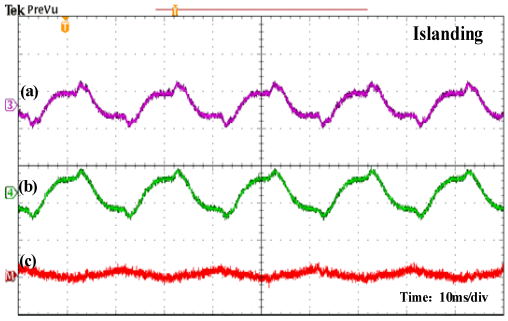

Fig. 5. 32. Performance of adaptive HCM operating in PCC harmonic compensation mode. (a: DG1 line current 10A/div; d: DG2 line current 10A/div; c: current difference 10A/div.)(**Experiment**)

- **Grid-Connected Operation**

The grid-connected operation of a DG unit is investigated in this subsection. The configuration of the system is shown in Fig. 5. 33, where the DG unit is connected to PCC with an LCL filter. Note that there are two types of loads in this system. The first one is the interfacing converter local load, which is connected to the output terminal of the LCL filter. Meanwhile, PCC also has a few linear and nonlinear loads, which are separated from local load by the circuit breaker (CB). The key parameters of this grid-connected system are listed in TABLE. 5. 4.

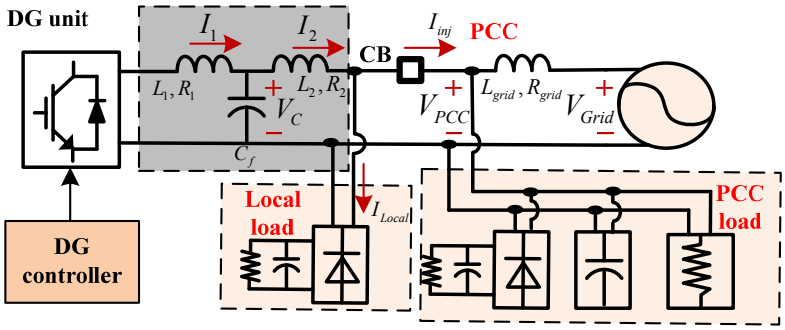

Fig. 5. 33. Experimental single-phase grid-tied microgrid with single DG units.

TABLE. 5. 4. Parameters for adaptive HCM verification on a grid-tied singl-phase 120V/1KVA inverter

DG Unit Circuit Parameters	Value
Grid feeder L_{grid} and R_{gird}	3mH (0.065pu) and 0.1Ω (0.006pu)
Output inductor L_1 and R_1	1.5mH (0.033pu) and 0.05Ω (0.003pu)
Feeder inductor L_2 and R_2	1.5mH (0.033pu) and 0.05Ω (0.003pu)
Filter capacitor C_f	12.5uF (0.056pu)
Rated voltage ω^* and E^*	314.15rad/s and 110V
DC link voltage V_{dc}	250V
Switching Frequency	10kHz
Power Control & Virtual Impedance Loops Parameters	Value
D_P *and* K_f	1/4750 and 1/1180
D_Q *and* K_E	1/350 and 1/45
ω_{LPF}	35*rad/s*
L_{Vf} *and* R_{Vf}	0*mH and* 0Ω
HCM Control Parameters	Value
k_{if}	700
k_p	2.4
K_{ih}	500(h=3,5,7); 300(*h=9*)
ω_{ch}	2*rad/s*
k_{AD}	*-20*
ω_E	62.8*rad/s*

The steady-state performance of the interfacing converter operating at 50.5Hz main grid voltage frequency is obtained from Fig. 5. 34 to Fig. 5. 39. In Fig. 5. 34 and Fig. 5. 35, the DG unit power control loop adopts the controller in (5-28) to maintain zero steady-state power control errors. However, fixed frequency HCM with $f^* = 50\text{Hz}$ in (5-2) and (5-3) is still employed for closed-loop current and voltage tracking.

Fig. 5. 34 shows the performance of the DG unit operating at local load harmonic compensation mode. It can be seen that the local load harmonic current are supplied by both PCC and DG unit. The distribution of local load harmonic current proves that fixed frequency HCM cannot fully compensate local load harmonics when the main grid appears frequency variations.

Likewise, the performance of the interfacing converter under line harmonic rejection mode is also investigated in Fig. 5. 35. When line harmonic rejection mode is employed, it is supposed to mitigate the harmonic distortions in the interfacing converter line current. However, due to the attenuation of closed-loop current tracking gain ($G_{eq\_c}(s)$ in (5-14)) at the characteristic harmonic frequencies, some sort of local load harmonic current still flows to the DG unit as shown in Fig. 5. 35 (c). As a result, the THD of interfacing converter line current is 27.05%.

The operation of DG unit using the revised power control scheme and the frequency adaptive HCM is also examined. In the first test, the local load harmonic compensation performance is shown in Fig. 5. 36. As the adaptive HCM can automatically adjust the band-pass frequencies of resonant controllers according to main grid frequency, it achieves better local load harmonic compensation compared to the case in Fig. 5. 34. When the harmonic current flowing from the local nonlinear loads is compensated by this control mode, the THD of injected current I_{Inj} (the current flowing to PCC after local load, see Fig. 5. 33) in Fig. 5. 36 is 5.41%.

When the control mode switches to interfacing converter line harmonic rejection mode, it can be seen from Fig. 5. 37 that all local load harmonic current flows to the PCC side and the interfacing converter line current distortion reduces to only 5.62% THD. In this case, as PCC voltage is distorted, the DG voltage is also distorted in order to maintain sinusoidal current flowing through the choke (L_2 and R_2).

If lower distortion of DG capacitor voltage is desired, the harmonic uncontrolled mode can be applied to the DG unit by setting the input of the

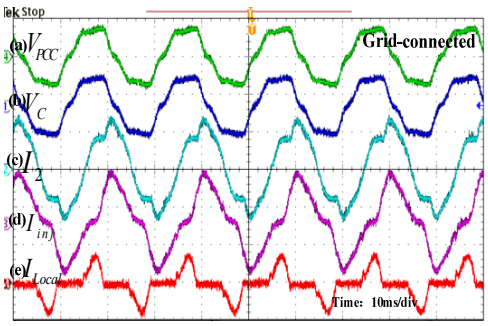

Fig. 5. 34. Grid-connected DG using fixed frequency HCM and revised power control loop operating in local load harmonic compensation mode. (a: PCC voltage 250V/div; b: DG voltage 250V/div; c: line current 5A/div; d: Injected current 5A/div; e: Local load current 5A/div). (**Experiment**)

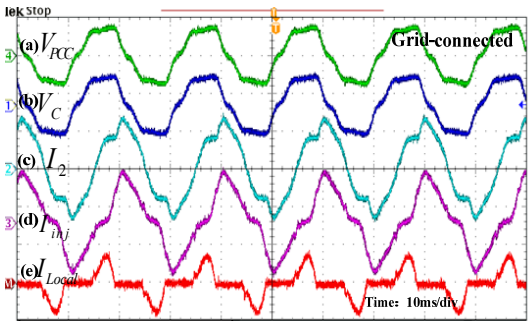

Fig. 5. 35. Grid-connected DG using fixed frequency HCM and revised power control loop operating in DG harmonic current rejection mode. (a: PCC voltage 250V/div; b: DG voltage 250V/div; c: line current 5A/div; d: Injected current 5A/div; e: Local load current 5A/div.) (**Experiment**)

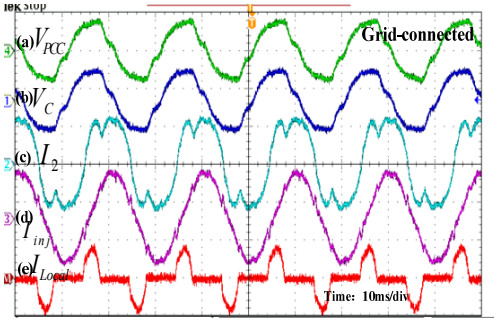

Fig. 5. 36. Grid-connected DG using adaptive HCM operating in local load harmonic compensation mode. (a: PCC voltage 250V/div; b: DG voltage 250V/div; c: line current 5A/div; d: Injected current 5A/div; e: Local load current 5A/div.) (**Experiment**)

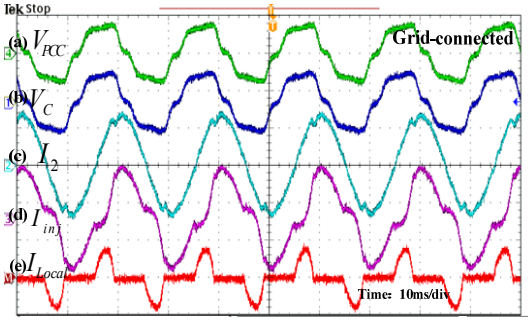

Fig. 5. 37. Grid-connected DG using adaptive HCM operating in DG harmonic rejection mode. (a: PCC voltage 250V/div; b: DG voltage 250V/div; c: line current 5A/div; d: Injected current 5A/div; e: Local load current 5A/div.) (**Experiment**)

current control branch as $(0 - V_C)$. Consequently, it can be seen from Fig. 5. 38 (b) that the DG voltage distortion is reduced to 4.84% THD.

Note that for the control modes as shown from Fig. 5. 36 to Fig. 5. 38, the PCC voltage distortion is not actively addressed. To compensate PCC voltage distortion, the PCC harmonic compensation mode is also applied to the

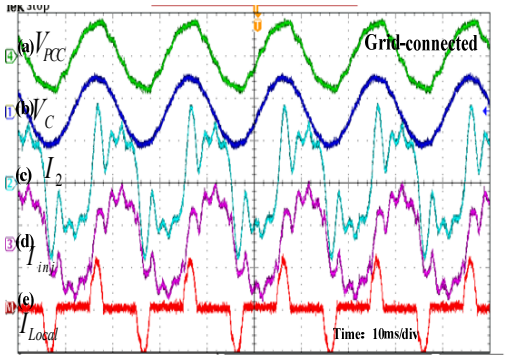

Fig. 5. 38. Grid-connected DG using adaptive HCM operating in DG harmonic uncontrolled mode. (a: PCC voltage 250V/div; b: DG voltage 250V/div; c: line current 5A/div; d: Injected current 5A/div e: Local load current 5A/div.) (**Experiment**)

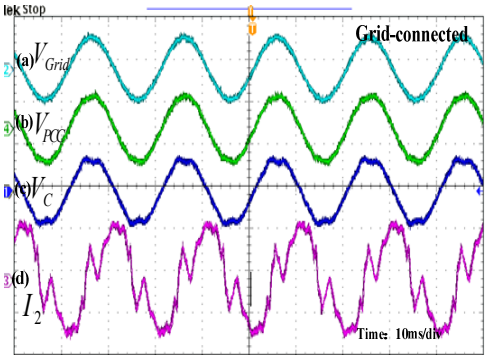

Fig. 5. 39. Grid-connected DG using adaptive HCM operating in PCC harmonic compensation mode. (a: main grid voltage 250V/div; b: PCC voltage 250V/div; c: DG voltage 250V/div; d: line current 5A/div.) (**Experiment**)

interfacing converter. In this case, *Rv* in (5-7) is selected as 0.8Ω. Accordingly, Fig. 5. 39 show that excellent PCC harmonic voltage compensation performance is realized in this control mode. The PCC voltage THD in Fig. 5. 39(b) is reduced to 4.72%.

5.6. Summary

A hybrid voltage and current control method (HCM) for DG interfacing converters with LCL filters is proposed. The proposed method realizes simultaneous control of fundamental capacitor voltage and harmonic line current. Therefore, it can overcome the limitations of the traditional voltage control method and current control method. In the proposed control scheme, the interfacing converter fundamental power control is regulated through the fundamental voltage tracking with droop control. At the same time, the harmonic line current is regulated to compensate the power distribution system harmonics or to improve the line current quality at the selected harmonic frequencies.

Additionally, the chapter also presents the frequency adaptive HCM to improve the performance of DG interfacing converter under grid frequency

deviation conditions. First, the second order generalized integrators (SOGI) are used to construct the HCM and the resonant frequency of the SOGI is determined by the frequency reference in the outer power control loop. With this modification, the frequency estimation is not needed. In addition, some digital filters for the conventional harmonic compensation or the virtual impedance control can be removed with the help of the proposed adaptive HCM. Although the frequency adaptive control is only applied to HCM as an example, this idea can be extended to improve the performance of CCM and VCM based controllers in a similar manner.

Chapter 6

Conclusions and Future Work

From a power electronics perspective, harmonic distortions in the power distribution system are mainly caused by two sources: (1) interfacing converter circuits, control schemes, and couplings between multiple converters, and (2) nonlinear loads and passive components/filters in the power distribution system. To reduce the harmonic distortion in the power distribution system, improved DG interfacing converter control schemes are proposed in this thesis. Note that some control schemes in this thesis can be extended to three-phase three-wire system, as they are developed in the stationary reference frame without using frame transformations.

6.1. Conclusions

The conclusions from the research addressed in each chapter of the thesis are presented below.

Chapter 2

To improve the line current quality of a DG unit, active damping methods can be implemented in the interfacing converter controller. In this chapter, a few well understood current control methods, including the single-loop, the double-loop, and the deadbeat are evaluated. The GCC scheme is proposed to provide virtual impedance to the filter plant and the interfacing converter closed-loop equivalent circuit. To enhance the performance of deadbeat current control, a harmonic damping method using virtual harmonic impedance is introduced. This guarantees a high quality interfacing converter line current by adding a harmonic virtual damping resistor to the LCL filter plant.

Chapter 3

Chapter 3 discusses an accurate equivalent circuit model that is valid for investigating the performance of parallel interfacing converters. As this proposed equivalent circuit can easily estimate the resonant frequencies of multiple parallel inverters, it helps the design and implementation of passive filters if conventional passive filtering methods are adopted by microgrid designers. The frequency domain analysis and extensive verification results in Chapter 3 show that the GCC and the virtual impedance aided deadbeat control schemes are effective in mitigating multiple resonances in parallel inverters.

Chapter 4

Chapter 4 discusses ways in which low voltage power distribution system harmonic distortions can be compensated using a DG interfacing converter with active power line conditioning functions. CCM and VCM are both used for DG unit integration, therefore, their respective harmonic compensation schemes are developed. This chapter proposes a simple modified CCM that achieves accurate control of distributed generation of real and reactive power when the harmonic compensation is performed in the interfacing converters. The PLL and the harmonic detection, which are mandatory for conventional grid-connected APFs, can be avoided by using the proposed method. To provide harmonic compensation for the future islanding distribution systems, VCM based compensation strategies are proposed. The proposed VCM can be used for both grid-tied and islanding operations.

Chapter 5

An HCM scheme is proposed to realize the merits of both CCM and VCM, through simultaneous control of the interfacing converter fundamental voltage and the harmonic current. Interfacing converter control issues during power distribution system frequency deviations are also investigated in this chapter. A frequency adaptive HCM is presented to improve the performance of an

interfacing converter under frequency varying situations. By using the frequency reference from the power control loop as a variable control parameter of HCM, the proposed frequency adaptive HCM scheme couples the power control loop and the voltage/current tracking loop. This modification makes HCM harmonic current tracking less sensitive to system frequency disturbances.

6.2. Thesis contribution

The research reported in this thesis contributes to the field of distributed generation interfacing converter control in four areas.

1) Virtual impedance based active damping

The analysis and control of virtual impedance is necessary to realize active damping of resonance. Previous research failed to clarify the effects and position of virtual impedance. The proposed GCC scheme with virtual impedance control provides straightforward parameter tuning. Moreover, the harmonic virtual impedance for improving the deadbeat control performance is realized without using additional sensors, and this harmonic virtual impedance is essentially a nonlinear virtual resistor that provides high impedance at fundamental frequency. This shows that virtual impedance can be more flexibly tuned than physical impedance, and the idea of nonlinear or harmonic selective virtual impedance can be extended to other controllers to improve the line current quality of grid-interfacing converters.

2) Accurate modelling of multiple parallel inverters

A straightforward closed-loop equivalent circuit is proposed to investigate couplings between multiple grid-tied inverters. This model accurately predicts the resonance frequency variations caused by parallel inverter interactions. With this model, the impacts of various types of current control schemes, including single-loop control, multi-loop control, and deadbeat control on microgrid damping can be evaluated. Accordingly, the analysis and modeling method can be used to guide the design and construction of future power electronics intensive systems.

Further investigation suggests that the GCC scheme and the virtual impedance aided deadbeat current control scheme as presented in Chapter 2 can be used to effectively address the frequency-varying resonances in a multiple-inverter based grid-interactive microgrid.

3) Active harmonic filtering provided by DG interfacing converters

A compensation method is proposed that uses interfacing converters to achieve harmonic filtering in the power distribution system. Considering that both CCM and VCM can be used to interconnect DG units to the power system, their corresponding harmonic compensation methods are developed. CCM based grid-tied converters with low cost microcontrollers face a major challenge through conflicts between limited microcontroller computational capability and complicated PLL and harmonic detection schemes. To solve this issue, a CCM based harmonic filtering method without harmonic detection and PLL is proposed for interfacing converters with cost effective microcontrollers.

4) Islanding system power quality enhancement

VCM and HCM with direct voltage support capability are mainly used for high power DG units, and the dual-mode (grid-tied and islanding) operation naturally requires strong microcontroller. To realize better harmonic compensation for future power electronics intensive power distribution systems, VCM and HCM are used to mimic the operation of distributed synchronous generators at fundamental frequency. Therefore, many operation schemes for synchronous generators can also be used for interfacing converters. Additionally, VCM and HCM can satisfy harmonic compensation without any interference with the control of the inverter at fundamental frequency. In other words, these proposed methods have the capability to control DG interfacing converters as virtual synchronous generators, while providing active power line conditioning services. Compared to VCM, HCM is an improved control scheme that provides direct closed-loop control of DG line current. The capability of HCM to address the impact of microgrid frequency deviation on harmonic compensation

performance shows that the interfacing converter can be insensitive to frequency disturbances with the help of adaptive HCM.

6.3. Future work

Three areas where further work is needed are indicated.

1) **Development of low switching frequency active damping methods for grid interfacing converters.**

A few active damping methods are proposed in Chapter 2. However, these damping methods are developed based on relatively high switching frequency at a few kilohertz. In this case, the average model of interfacing converter is suitable for filter resonance investigation. Considering that the high power converter with less than one kilohertz switching frequency can be adopted for high power renewable energy resources integration, development of an enhanced damping method that is insensitive to a lower system state updating rate is recommended.

2) **Distribution system harmonic compensation through collaborative control of multiple DG unit interfacing converters.**

Harmonic compensation capability is successfully integrated in DG unit interfacing converters. When the harmonic compensation function is implemented in a large number of interfacing converters at the same time, multiple interfacing converters may compete with each other for harmonic compensation, adversely affecting the stability of the entire system. A supervisory central controller could be developed and installed in the power distribution system to assign optimal harmonic compensation to be shared by the interfacing converters.

3) **Other auxiliary functions using DG unit interfacing converters.**

This thesis focuses on the harmonic compensation of distribution systems. It is possible to provide many other power quality enhancement services, such as reactive power support and imbalanced voltage compensation, through the flexible control of interfacing converters. It has already been specified by a few

European counties that the DG unit can inject reactive power to the grid during main grid sags. In addition, the grid-tied converter can be controlled as negative sequence virtual impedance, which can reduce the imbalanced voltage of the system by absorbing the negative sequence current from local and PCC loads.

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