DSP Based Realization of Pre-Processed Discontinuous PWM Schemes for 3-Limb Core Coupled Inductor Inverters

by

Srilak Nirmana Perera

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Energy Systems

Department of Electrical and Computer Engineering
University of Alberta

UNIVERSITY OF ALBERTA

Abstract

Faculty of Graduate Studies and Research
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The design of most power electronic systems is ultimately linked to the devices being used, the system efficiency and the system cost. A Digital Signal Processor (DSP) based 3-phase Pulse Width Modulation (PWM) switching scheme for a 3-Limb Core Coupled Inductor Inverter (CII) is presented as a low cost controller solution to provide better excitation for the magnetic core. This is consistent with lowering the cost of the power converter system with the use of a 3-limb core, as opposed to three separate inductors, and reduced switch count for the inverter. A modified interleaved discontinuous PWM scheme is examined that restrains the main inductor magnetic flux to lie within the magnetic core. This basic guideline for a suitable PWM scheme is to guarantee that all the inverter switching states maintain a zero inductor net winding voltage for the three phases. The scheme also smoothens the high frequency winding current ripple. In a practical sense, such a scheme normally requires extensive control and PWM tasks which calls for a high-end processor with parallel and post-processing capacities, hence increasing system costs. A low cost solution, by manipulating the original conceptual scheme, is introduced as an alternative Pre-Processed PWM scheme for a DSP environment, using only one carrier signal. Experimental results verify that the DSP PWM module can successfully implement the target scheme in a less complex manner. The DSP realization of the PWM scheme not only provides cost effectiveness by eliminating the need for a high-end processor, but also minimizes the size of the control circuitry. Experimental results confirm that the DSP based scheme offers the same system high power conversion efficiency as the original conceptual PWM scheme, due to benefits related to the reduction of the high-frequency winding current ripple.

"One is one's own master or refuge"

$\sim$ *Buddha*

To my mother, father, sister and myself...

Acknowledgements

There are a few unique persons that I would like to thank here: do forgive me if I stray away from the formal prose in this note.

First and foremost, I would like to express my utmost gratitude to my thesis supervisor, Professor John Salmon, for his support, not only as an academic supervisor, but also as a human being. I feel that I am really fortunate to be given the opportunity to follow graduate studies under his unique way of supervision. The atmosphere he created with his way of research, allowing me to build power electronic circuits to gain practical knowledge, guiding me in to better technical writing, and sometimes with his witty remarks, is quite remarkable in his own way.

While I was busy doing my graduate studies in Canada, my mother and sister provided all the moral support that I could ask for. They do not know it, but nothing could match such an understanding. And I would like to thank them for just hanging in there for nearly two and a half years while I was away. And, I am forever indebted to my late father for the foundation he built for my family so that we could live a better life after he was gone.

We all have endured hardships during many stages of our life. Though one is one's own refuge, sometimes a good friend is the rock that you hold on to. I would like to thank Kasun, Amali, Sachini and Hiranya for just being good friends of mine.

I would like to thank Albert Terheide for his friendly support in helping me to overcome technical problems during many stages of my thesis work. I have never met a technician with such an amazing technical prowess. Special thanks go to my laboratory colleague Reaz Ul Haque and my friend Prasanna Herath for their friendship and help over the years.

On a special note, I would like to express my sincere gratitude to Dr. Sunil Abeyratne for his enlightening guidance during my early stages of engineering studies and research.

And finally, I would like to thank the University of Alberta Supplementary Bursary Program and the University of Alberta for their benevolence and support for graduate students.

~ Nirmana, June 2015

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Abbreviations

ADC	**A**nalogue to **D**igital **C**onverter
AHC	**A**ctive **H**igh **C**omplementary
BJT	**B**ipolar-**J**unction **T**ransistor
CII	**C**oupled **I**nductor **I**nverter
CPU	**C**entral **P**rocessing **U**nit
CSI	**C**urrent **S**ource **I**nverter
DB	**D**ead **B**and
DSC	**D**igital **S**ignal **C**ontroller
DSP	**D**igital **S**ignal **P**rocessor
DPWM	**D**iscontinuous **P**ulse **W**idth **M**odulation
ECD	**E**mbedded **C**ontrols **D**eveloper
EMDS	**E**lectric **M**otor **D**riven **S**ystems
EMI	**E**lectro-**M**agenetic **I**nterference
ESR	**E**quivalent **S**eries **R**esisitance
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
GaN	**Ga**llium **N**itride
GUI	**G**raphical **U**ser **I**nterface
IGBT	**I**nsulated **G**ate **B**ipolar-junction **T**ransistor
IM	**I**nduction **M**otor
LPF	**L**ow-**P**ass **F**ilter
MCU	**M**icro-**C**ontroller **U**nit

MDPWM	**M**odified **D**iscontinuous **P**ulse **W**idth **M**odulation
MMF	**M**agneto-**M**otive **F**orce
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NPC	**N**eutral **P**oint **C**lamped
RAM	**R**andom **A**ccess **M**emory
SBD	**S**chottky **B**arrier **D**iode
SCR	**S**ilicon **C**ontrolled **R**ectifier
SiC	**Si**licon **C**arbide
SDPWM	**S**tandard **D**iscontinuous **P**ulse **W**idth **M**odulation
SHE	**S**elective **H**armonic **E**limination
SPWM	**S**inusoidal **P**ulse **W**idth **M**odulation
SVPWM	**S**pace **V**ector **P**ulse **W**idth **M**odulation
PLL	**P**hase-**L**ocked **L**oop
PWM	**P**ulse **W**idth **M**odulation
TI	**T**exas **I**nstruments
USB	**U**niversal **S**erial **B**us
VSI	**V**oltage **S**ource **I**nverter
WEF	**W**inding **E**xication **F**lipping
μC	**M**icro-**C**ontroller
μP	**M**icro-**P**rocessor

Physical Constants

Permeability of free space	μ_0	=	$4\pi \times 10^{-7}$ NA^{-2}
Permittivity of free space	ϵ_0	=	$8.854\ 187\ 817 \times 10^{-12}$ Fm^{-1}
Speed of light	c	=	$2.997\ 924\ 58 \times 10^{8}$ ms^{-1}

Symbols

c_{gd}	gate-to-drain capacitance of a MOSFET	F
f_c	carrier frequency	Hz
f_{sys}	DSP system clock frequency	Hz
f_{sw}	switching frequency	Hz
i_a	phase-A output line current	A
i_b	phase-B output line current	A
i_c	phase-C output line current	A
i_{a_F}	fundamental of phase-A output line current	A
i_{aCM-HF}	high freq. component of phase-A com. mode current	A
i_{aDM-HF}	high freq. component of phase-A dif. mode current	A
$i_{a_{dc}}$	dc component of phase-A dif. mode current	A
i_{a1}	phase-A top leg output current	A
i_{a2}	phase-A bottom leg output current	A
i_{a-circ}	phase-A winding circulating (= differential) current	A
i_{a1CM}	top winding current in com. mode cct.	A
i_{a1DM}	top winding current in dif. mode cct.	A
i_{a2CM}	bottom winding current in com. mode cct.	A
i_{a2DM}	bottom winding current in dif. mode cct.	A
i_{aCM}	phase-A com. mode current	A
i_{aDM}	phase-A dif. mode current	A
i_{aU}	phase-A upper winding current	A

i_{aL}	phase-A lower winding current	A
i_{DS}	instantaneous drain-to-source current of a MOSFET	A
i_{G-max}	maximum gate current	A
L	self inductance of either winding when $L_1 = L_2$	H
L_1	top winding self inductance	H
L_2	bottom winding self inductance	H
L_{eff}	effective inductance	H
L_L	leakage inductance of either winding when $L_{L1} = L_{L2}$	H
L_{L1}	top winding leakage inductance	H
L_{L2}	bottom winding leakage inductance	H
L_{t1}	top winding total inductance	H
L_{t2}	bottom winding total inductance	H
m_a	modulation index	no units
M	mutual inductance between top and bottom windings	H
$P_{loss-on}$	on-state loss for power switches	W
Q_{rr}	reverse recovery charge of a MOSFET body diode	C
R_{DS-on}	static on-state resistance of a MOSFET	Ω
R_G	external gate resistance of the gate circuitry	Ω
T_c	carrier period	s
t_{DB}	dead-time	s
T_{rr}	reverse recovery time of a MOSFET body diode	s
T_{sys}	DSP system clock period	s
T_{sw}	switching period	s
V_{AB}	line-to-line voltage: phase-A to phase-B	V
V_{An}	phase voltage: phase-A to dc-link negative rail	V
V_{Ao}	phase voltage: phase-A to dc-link mid-point	V
V_{base}	base voltage	V
V_{Bo}	phase voltage: phase-B to dc-link mid-point	V
V_{CE-sat}	on-state voltage across an IGBT	V

V_{Co}	phase voltage: phase-C to dc-link mid-point	V
V_{dc}	dc-link voltage	V
V_{GS}	gate-to-source voltage of a MOSFET	V
v_{WA}	phase-A total winding voltage	V
v_{WB}	phase-B total winding voltage	V
v_{WC}	phase-C total winding voltage	V
$v_{W_{tot}}$	sum of the winding voltages of the three phases	V
Φ_{1CM}	flux induced by top winding in the limb for com. mode cct.	Wb
Φ_{2CM}	flux induced by bottom winding in the limb for com. mode cct.	Wb
Φ_{1DM}	flux induced by top winding in the limb for dif. mode cct.	Wb
Φ_{2DM}	flux induced by bottom winding in the limb for dif. mode cct.	Wb
Φ_{CM}	resultant flux in the limb for com. mode cct.	Wb
Φ_{DM}	resultant flux in the limb for dif. mode cct.	Wb
$\Re$	magnetic reluctance	H^{-1}
$\Re_a$	air path magnetic reluctance	H^{-1}
$\Re_L$	phase-A limb magnetic reluctance	H^{-1}

Terminology

$6-CII/12-CII$	Six/Twelve switch versions of the coupled inductor inverter system
$AQCTLA$	Action Qualifier register A of a PWM module
$AQCTLB$	Action Qualifier register B of a PWM module
CM	Common mode
$CMPA$	Comparator-A register of a PWM module
$CMPB$	Comparator-B register of a PWM module
DM	Differential mode
$DPWM1$	60° discontinuous type modulation technique
$ePWMxA$	Unit A of a particular PWM module x
$ePWMxB$	Unit B of a particular PWM module x
FLT	Fault pin in the control side of an inverter leg
$MDPWM1$	Modified discontinuous PWM without Winding Excitation Flipping
$MDPWM2$	Modified discontinuous PWM with Winding Excitation Flipping
RST	Reset pin in the control side of an inverter leg
$SDPWM1$	Standard discontinuous PWM with interleaved carrier
$SDPWM2$	Standard discontinuous PWM with inverse interleaved carrier
$TBCLK$	Clock for DSP PWM modules
$TBCTR$	16-bit Counter register of a PWM module
$TBPRD$	16-bit Timer Period register of a PWM module
$TIMER0PRD$	16-bit Timer0 Period register of the DSP Timer0 module
TZ	Trip Zone pin unit of a PWM module

Chapter 1

Synthesis of Sinusoids in Switch-Mode Power Converters

There is no doubt that, if there were ever to be a fictional work named Power Electronics, its protagonist would be "The Inverter".

Over the past few decades, new Switch-Mode topologies and control methods have been studied to enhance the performance of inverters. This work concerns such a topology for a three-phase power system, and a new DSP based control strategy with a simplified design intended to lower the cost in delivering the required PWM waveforms for the converter. The thesis work is placed in context here, highlighting the key conceptual contributions. A foundation is provided for the conceptual subject content while establishing suitable background knowledge to the interests of those unfamiliar with the subject. Chapter 1 and Chapter 2 present a background review on basic PWM concepts for three-phase converters where the concepts established are built upon in Chapter 3.

1.1 Significance of Three-Phase Switch-Mode Converters

Inverters have become the essential building block of modern power electronic systems. The development of efficient megawatt level inverters alongside with other power converters is of significant interest to the electrical engineer in finding solutions to the ever

increasing global power demand. An understanding of the inception and subsequent development of inverter technology is important as it signifies the technical issues faced by the early engineer and how the corresponding solutions resulted in the present power converter systems. This allows the reader to appreciate the context of subject material with proper insight.

As creatures of both 20^{th} and 21^{st} centuries, we have witnessed a significant development[1] in electrical technology for the past few decades. The contribution of this technological advancement in the evolution of inverters is twofold:

1. The progression in semiconductor physics and device materials has revealed new semiconductor devices with better performance (for example; Silicon Carbide, SiC, and Gallium Nitride, GaN, devices) while improving characteristics such as device current and voltage blocking capabilities of still dominating Silicon semiconductor devices. The better the device characteristics, the higher the inverter efficiency.
2. Digital Electronics has also shown a development in a similar rate, producing faster digital signal processors (DSP), yet with a smaller size. This has allowed the engineers to perform complex control tasks on inverters (and on other related systems) which were not possible a few decades ago.

The important fact emerging out of these developments is that it has allowed power electronic engineer's imagination of new topologies and control schemes to be practically tested; it is no longer imagination.

Applications of inverters are vast and can be found in audio amplifiers; lighting equipment; un-interruptible power supplies; renewable energy systems; and most significantly, in ever used ac machine drives [4]. According to the International Energy Agency's 2011 report "Energy-Efficiency Policy Opportunities for Electric Motor-Driven Systems" [5], Electric Motor Driven Systems (EMDS) are responsible for approximately 43-45% of global energy consumption, being the single largest end-user of electricity.[2] Therefore, the efficiency of EMDS has a significant influence on the preservation of global energy, and most importantly, on the sustainability of environment. As the efficiency and sound performance of

[1] Of course, true development is when the development is sustainable and environmentally conscious. In this regard, it is encouraging to witness the emergence of renewable energy concepts, especially in European countries. For instance, 85% of Iceland's primary energy comes from domestic renewable energy sources [3].

[2] The second largest consumer is lighting and it consumes half of what EMDS consume. It is stated that EMDS account for around 6000 metric tonnes of CO_2 emissions per year and that it is increasing [5].

EMDS are primarily dependent on their drives,[3] the strategies used to enhance inverter drive performance are of vital importance.

1.2 Inverters, Sinusoidal Voltage Synthesis and Efficiency

The prime objective of an inverter is to generate a sinusoidal ac output with desired frequency and magnitude. The grid frequency and the magnitude are always fixed (for example, $460V$ at $60Hz$). Fig. 1.1 shows a typical inverter setup with a motor load. The input to the inverter is a fixed dc voltage, and the inverter is responsible for generating an average output voltage of variable magnitude and frequency for the load. This is achieved by Pulse Width Modulating (PWM) the on/off times (duty ratio) of the inverter switches. The efficiency of the output stage depends on how the inverter is configured and operated (i.e. what inverter topology is used and how the switching for the inverter is generated). Therefore, inverter topologies and PWM schemes are a prime research focus for power converters.[4]

The major criterion which decides whether a converter is suitable for a particular application or not is its losses: wasted energy not only lowers the system performance, but also causes for undesired costs (ex: removal of generated extra heat [4]). The system size, weight and cost are the other factors which affect the realization of a power converter.

Assuming that the reader is fairly familiar with the concept of switching power electronic topologies [4, 6, 7], consider the inverter power losses. In high power switching applications, a significant amount of the inverter load power loss is caused by harmonics [4, 6]. Harmonics primarily occur when the generated output waveform is not a perfect

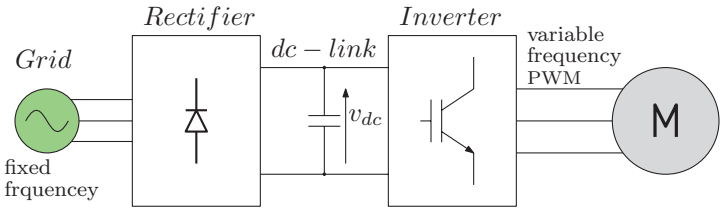
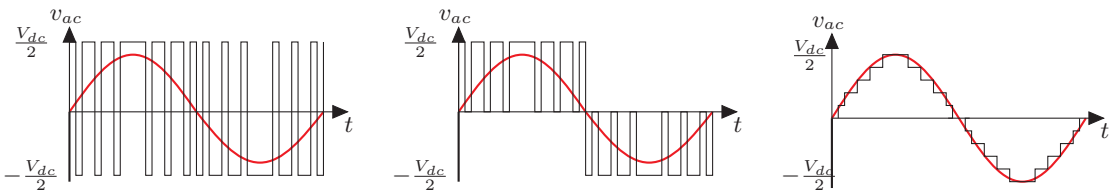


FIGURE 1.1: A basic inverter setup for an Induction Motor (IM) application

[3]The overall efficiency of the system also depends on motor characteristics, the final load, wiring and few other factors. But it is safe to say that the drive system is the major factor.

[4]Generally, the term "converter" is used to refer to either rectifiers or inverters. In rectifier mode, the power flow is from the ac side to the dc side; and in inverter mode, it is from the dc side to the ac side [4].



(a) 2-level (b) 3-level (c) Multi-level

FIGURE 1.2: Different voltage synthesis approaches

sinusoid. The obvious solution is, to try and shape the output ac voltage to be as close as possible to a sinusoid. The early solutions of inverter switching had only two levels of switching (see Fig. 1.2(a)). Therefore, with that setup, to obtain a better resemblance to a sinusoid, especially in reference to the inverter output current, inverters are switched at very high switching frequencies, so that the inverter switching harmonics are in a much higher frequency range than the fundamental sinusoidal output. However, this in turn introduces another major concern in converter losses: the switching losses. The higher the switching frequency (f_{sw}), the higher the switching losses. In finding solutions for these difficulties, strategies should be devised to synthesize voltage waveforms with more than two levels, but still trying to maintain a lower switching frequency.

The concept of multi-level inverters originated as Nabae, Takahashi, and Akagi first proposed the *Three-Level Neutral Point Clamped Converter* back in early 1980s [7, 8]. Since then, researchers have proposed and implemented various kinds of multi-level converter topologies looking for the synthesis of the perfect sinusoid at the ac output. The underlying idea is to produce an approximate sinusoidal voltage waveform with an available set of dc voltage levels [9]. The higher the number of voltage level states available, the more the steps that can be used in the converter output in the form of a staircase-type voltage waveform. Fig. 1.2 illustrates 2-level, 3-level and multi-level approaches of sinusoidal voltage synthesis.

The PWM scheme is as important as the topology itself in multi-level realization of the output voltages. For instance, the 3-level bipolar realization of the Full-bridge converter [4] from the 2-level unipolar realization is achieved by a simple altering of the PWM scheme: without any change to the topology. Furthermore, the PWM scheme is what determines the ultimate efficiency of the overall system. Evidently, the PWM scheme also plays a major role in shaping the output ac voltage as close as possible to the perfect sinusoid.

1.3 The Coupled Inductor Inverter and Discontinuous PWM Schemes for Three-Phase Power Systems

The core of the thesis material lies on a recent topology and a modified PWM scheme which facilitates aforementioned characteristics. The key contributions of the topology and the requirements of a suitable scheme are highlighted, and the thesis statement is defined.

1.3.1 A Brief on the CII Topology and Suitable PWM Schemes

The Coupled Inductor Inverter (CII) topology was introduced in 2008 by Salmon et al. as a novel inverter topology with significant performance benefits [10]. The basic CII topology with six switches for a three-phase system is illustrated in Fig. 1.3. The topology claims to

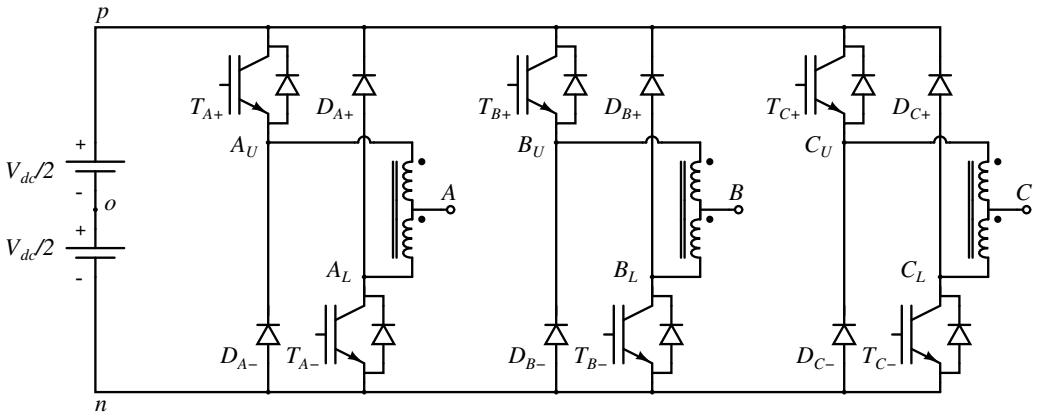


FIGURE 1.3: The basic six-switch Coupled Inductor Inverter topology (6-CII)

have the following benefits over standard inverter topologies [10, 11]:

1. 5-level PWM voltage synthesis with half the number of power electronics of standard inverter topologies.
2. Lowering of high frequency output current and ac filter inductance size.
3. Elimination of dead-time requirements and inherent protection for dc-rail shoot-through conditions.

The topology relies on internal coupled inductors in generating multi-level PWM outputs in contrast to traditional solutions such as addition of more switches or increase of

external ac inductor sizes. Subsequent research on the topology investigated the physical implementation of coupled inductors within suitable cores and PWM schemes which provide better magnetic performance for the inductor cores [12–16].[5] A 3-limb magnetic core based coupled inductor unit lowers the magnetic losses, improves the inverter efficiency and reduces the size and weight of the magnetics for the CII topology [12].

Discontinuous PWM (DPWM), in contrast to traditional continuous Sinusoidal PWM (SPWM), offers better utilization of the four operating states of a CII phase leg in a three-phase converter.[6] The original three-phase reference signals of the "60° *Discontinuous Modulation Technique*" discussed in [1] is shown in Fig. 1.4. These reference signals are the

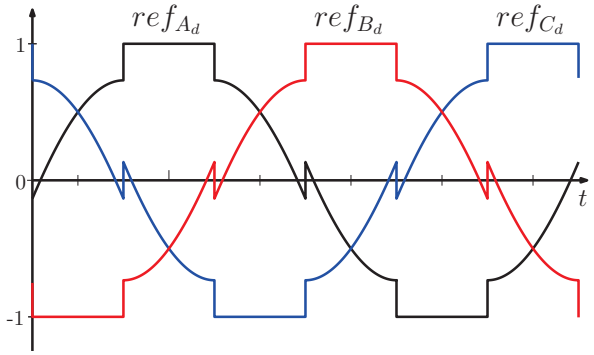


FIGURE 1.4: Three-phase reference signals for 60° discontinuous modulation (see DPWM1 in chapter 6 of [1])

basis of subsequent schemes considered in this work: as far as the output voltage pattern is concerned, all the schemes on average try to synthesize these original references. The PWM scheme is the key criterion which determines the magnetization of the coupled inductor core. A proper core magnetization is essential in reducing the high frequency component in the inverter output and inductor winding currents to increase the inductor and inverter efficiency. Over the last few years since its inception, various PWM schemes have been studied in handling the core magnetization of the CII topology [15–17]. Although these schemes establish improved magnetic performance, their implementation is quite complex in contrast to conventional SPWM or DPWM schemes. In fact, high-end signal processing capabilities were required for the practical implementation of the schemes. Investigating this subject matter and finding a pragmatic solution mark the foundation of this thesis.

[5] Note that, a thorough analysis on the CII topology and suitable PWM schemes and resulting benefits are presented in Chapters 2 and 3 to establish a clear line of thought on arriving at the thesis statement.

[6] The conventional inverter leg has only two operating states. Chapters 2 and 3 cover these details in depth.

1.3.2 Thesis Statement

This thesis work presents a *Digital Signal Processor Based Pre-Processed DPWM Control Algorithm for a Three-Phase, 3-Limb Core, Six-Switch CII Topology* as simpler solution in magnetizing the inductor core while offering expected system performances. In contrast to existing schemes of [15–17], the proposed PWM scheme renders the following key benefits:

1. Requires only one carrier signal, in contrast to two carriers used in previous schemes.
2. Unlike the Field Programmable Gate Array (FPGA) based solutions (as in [15, 17]), this does not require access to the output logic after the PWM signal generators.
3. Depends on sequential processing for logic generation and does not require parallel processing capabilities.
4. Can be implemented in a low cost DSP eliminating the need for high-end processor units like FPGA systems.
5. Simpler control circuitry and reduced space requirement for the control board.
6. Supports Winding Excitation Flipping (WEF) for the windings ([16]) with simpler control logic, that halves the high frequency ripple of the inductor winding current.

In addition, this work provides a comprehensive analysis on the operation of coupled inductor based parallel inverter systems, followed by an in-depth theoretical analysis of DPWM schemes (for 3-limb core excitation) with experimental performance comparisons.

Subsequent chapters are forged in a logical manner, such that the reader can clearly identify the transition from one stage to another in arriving at the final outcome of this work. The structure of the report is as follows: the inception and the current situation of inverter topologies and PWM schemes are investigated (Chapter 2), establishing the base for the conceptual arrival of the CII topology. The reader is given the opportunity (Chapter 3) to delve deeply into the theoretical aspects of the CII topology and associated PWM schemes. Then, the thesis work is placed in context (Chapter 4), explaining the need for a simpler PWM approach for the 3-limb core based CII topology. A low cost MOSFET based inverter system (Chapter 5) was developed to verify the proposed scheme experimentally with suitable performance analyses (Chapter 6). The report is concluded by summarizing the key points of the work and identifying potential concepts in further enhancing the existing system and its performance (Chapter 7).

Chapter 2

Synthesis of Sinusoids: Topological Platforms and PWM Architectures

No matter how sophisticated a dedicated/embedded digital hardware system gets, the digital system needs the appropriate elements suitable for a specific application. An improved inverter topology is promising; however, it still requires appropriate digital PWM controller hardware and software that can deliver the promised topological benefits.

An understanding of ongoing developments in inverters and PWM schemes is imperative for understanding the concepts presented in this thesis. This chapter provides a brief, but explanatory review on inverter topologies and PWM schemes. The chapter contents is intended to establish a clear transition of events behind the subject material of this thesis.

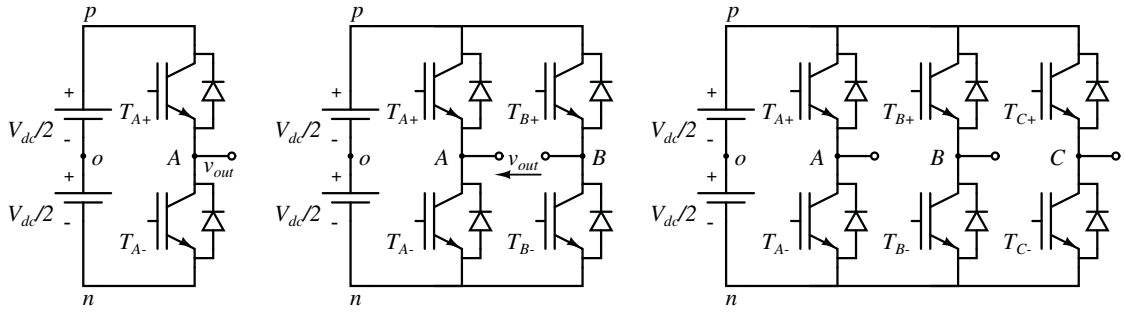
2.1 A Brief History of Inverter Topologies

A brief review on recent developments of inverter topologies is presented. In addition, the basics of multi-level voltage synthesis, which is an essential concept in high power systems, is also discussed. Note that, Appendix A provides a comprehensive discussion on basic inverter topologies and PWM schemes. A thorough description of PWM theory with vivid waveform and logic circuit diagrams, and common misconceptions on PWM logic are also included. Therefore, the reader is encouraged to refer to Appendix A for a review of the basic concepts on inverter PWM theory assumed in subsequent discussions.

2.1.1 The Core: Inverters

In technical literature, an inverter is more commonly referred to as a *Voltage Source Inverter* (VSI). The basic idea behind a VSI is to generate pulsed output voltages. The term "Voltage Source" identifies that the power source for the inverter is a fixed dc source at the input.[1] There are also *Current Source Inverters* (CSI) where the output is pulsed currents and the input power source is a current source (ex: a controlled SCR unit).

The basic unit of a VSI system is an *Inverter Leg* (also referred to as an *Inverter Arm*) and is shown in Fig. 2.1(a). Different combinations of these legs result in different inverter topologies, and this is an ongoing research area since the inception of the inverter leg. Fig. 2.1(b) shows a simple combination of two inverter legs forming a topology more commonly known as the *H-bridge* (also known as the *Full-bridge Converter*).



(a) An inverter leg (b) A simple H-bridge (c) A standard three-phase inverter

FIGURE 2.1: Basic topological building blocks of inverter systems

Since a standard inverter system has a common dc power rail for all inverter legs,[2] the two switches in an inverter leg never receive an ON state signal simultaneously.[3] This is commonly referred to as *Complementary Switching*. Therefore, an inverter leg has only two switching states in such arrangements: for the phase A of the topologies in Fig. 2.1, the two states are defined as follows;

$$[1] : T_{A+} = ON,\ T_{A-} = OFF \qquad [0] : T_{A+} = OFF,\ T_{A-} = ON$$

[1] The dc source can be a simple battery or a rectifier with a dc capacitor-filter at the output.
[2] A common dc power rail in a power system is usually referred to as the *dc-link*.
[3] This is to avoid the short-circuiting of the dc-link.

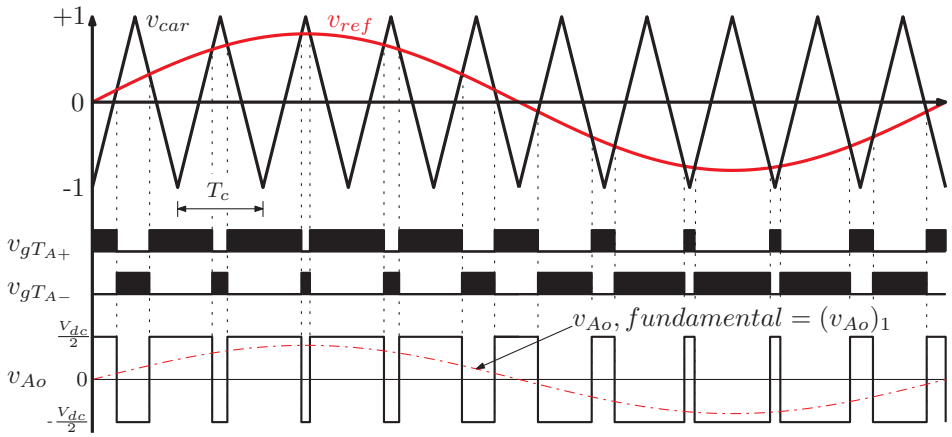


FIGURE 2.2: The simplest PWM scheme for an inverter leg

Fig. 2.2 shows how an inverter leg is switched in a complementary manner when a carrier signal (v_{car}) and a reference signal (v_{ref}) are compared according to the following logic:

$$\begin{aligned} if \quad v_{ref} > v_{car} \longrightarrow T_{A+} = ON,\ T_{A-} = OFF \longrightarrow state\ [1] \\ if \quad v_{ref} < v_{car} \longrightarrow T_{A+} = OFF,\ T_{A-} = ON \longrightarrow state\ [0] \end{aligned} \tag{2.1}$$

The switching technique used in Fig. 2.2 is known as a carrier based sinusoidal PWM modulation scheme.[4] The output voltage v_{Ao} varies only between two levels of voltages ($+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$) and is said to have a *2-level* output voltage. With topologies with two or more inverter legs, it is possible to have more than two levels for the output voltage. For example, with *Unipolar PWM*,[5] the full-bridge converter can produce an output voltage with three levels.

Fig. 2.1(c) shows a standard *Three-Phase Inverter* which is a combination of three inverter legs. Three sinusoidal reference signals (phase shifted to each other by 120°) are compared with a single carrier signal using the same logic expressed in Eq. (2.1) to derive the switching signals. Note that, the use of a single carrier signal, associated with the 2-level output for each leg, automatically results in a unipolar output line voltage pattern for the three phases. Here also, each leg is switched complementarily, and therefore, with each leg having two switching states ([0] and [1]) the system of three legs have $2 \times 2 \times 2 = 8$ possible

[4] More detail on modulation schemes is presented in the next section of this chapter.
[5] Refer to Appendix A.2 for a detailed explanation on unipolar and bipolar PWM techniques.

switching states. These 8 states can be summarized as $[A \;\; B \;\; C]$ where A, B, and C can be either 0 or 1 representing the state of each phase leg.

The three phase inverter is the most widely used inverter topology still to date, especially in low and medium level voltage drives (generally voltage levels below 1200 V). The obvious choice for these applications are the IGBTs with their higher voltage and current capabilities. But, more recently, Silicon Carbide (SiC) MOSFETs have been developed that can handle voltages up to 1200 V with very low losses and higher switching frequencies.[6]

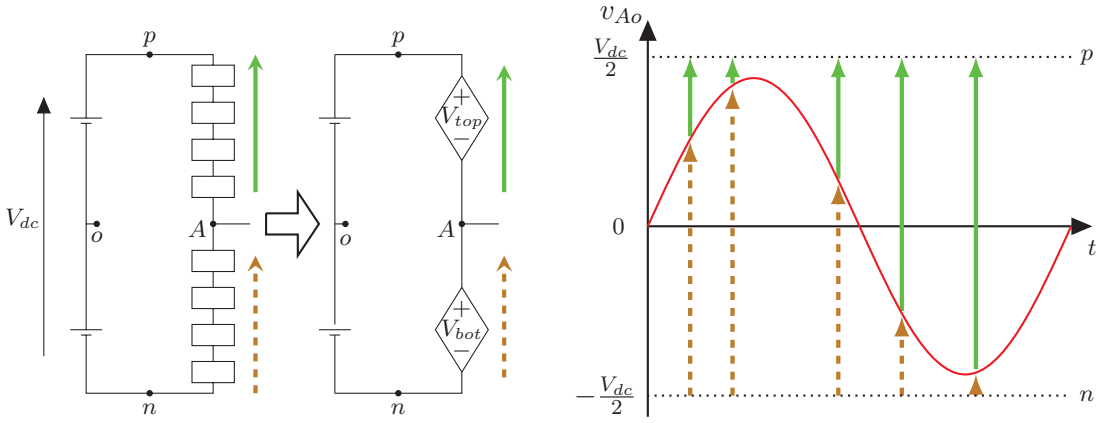
2.1.2 Evolution of Multi-Level Voltage Synthesis

With the limitation of device voltage ratings, means were developed to use low voltage power semiconductor devices on high voltage applications that require voltage levels far greater than 1200 V. A simple solution would be to stack more than one switch in series in a leg to handle a higher voltage rating (for example, four switches in series in the place of T_{A+} and another four in the place of T_{A-}). With slight modification to the topology with added diodes and capacitors, more levels can be introduced to the output voltage signal [9]. This way, the voltage rating of the inverter is increased as well as the quality of the output voltage waveform.

As Chapter 1 describes, the concept of multi-level voltage synthesis originated with the introduction of the 3-level NPC converter: which is a modified version of the standard three-phase inverter topology with strategically added diodes and capacitors. The topology generates a 3-level voltage at the output of each leg, resulting a 5-level output line voltage [6, 7]. Consequently, numerous research efforts have been carried out in finding better multi-level topologies with more voltage levels: the resulting topologies could generally be classified into the following topologies; 1) Magnetic transformer coupled multi-pulse voltage source converters, 2) Diode clamped converters, 3) Flying (floating) capacitor converters, 4) Cascaded converters with separate dc sources and, 5) Modular multi-level converters.

Recently, multi-level converters of the modular type have found a greater attention in the power electronics field [18, 19]. In general, the operation principle of these converters can be described as illustrated in Fig. 2.3 [20]. Each phase leg consists of sub-modules

[6] ROHM Semiconductor© and Cree© have put SiC MOSFETs already into market and they are readily available. For example, the power MOSFETs $SCH2080KE$ and $SCT2080KE$ of ROHM and $C2M0160120D$ of Cree can handle voltages up to 1200 V.



(a) Concept of multi-level voltage synthesis (b) Generating a sinusoid using upper and lower legs

FIGURE 2.3: Understanding the basics of multi-level voltage synthesis

(m number of modules in both top and bottom halves of the leg), where the voltage of a capacitor in each sub-module is kept at V_{dc}/m [21]. For the system in Fig. 2.3(a), m equals to 4. It is understood that top and bottom groups of sub-modules can be represented as controllable dc voltage sources, where the group voltage magnitude can range from 0, $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$ and V_{dc}. Identifying the following relationship for each phase leg,

$$V_{dc} = V_{top} + V_{bot} \tag{2.2}$$

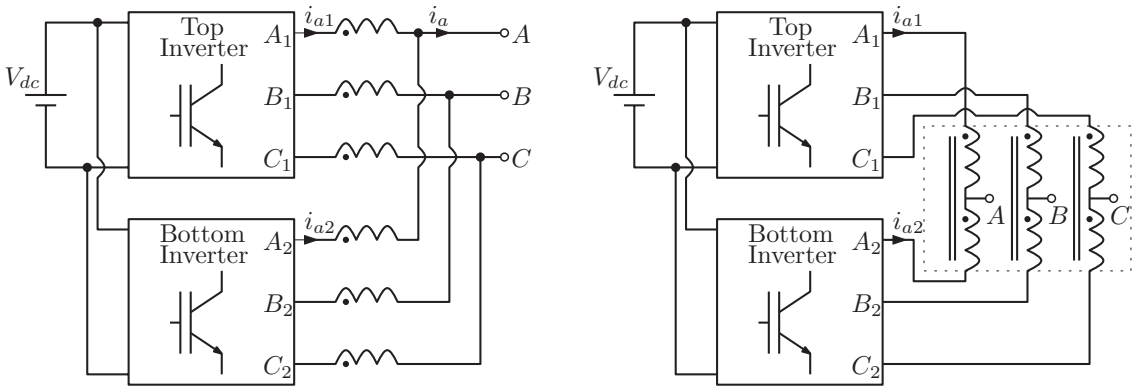
it is understood that changing the output of the two controlled dc voltage sources, a sinusoidal waveform can be synthesized as illustrated in Fig. 2.3(b).

An in-depth analysis on each of the aforementioned multi-level topologies is beyond the scope of this report; however, the reader is encouraged to refer to the reference literatures [9, 18, 19, 22] that offer a broader analysis on these topologies.[7] Note that, though the multi-level topologies were originally developed aiming for high voltage/power applications, they can still be used, especially for medium voltage applications, to get higher number of voltage levels compared to three levels of the standard three-phase inverter.

[7] Especially, [9] by Lai and Peng is an excellent read on early stages of multi-level topologies, whereas [19] by Akagi carries out an in-depth analysis on more recent modular multi-level converter topologies.

2.1.3 Another Perspective: Parallel Inverters

Multi-level topologies allow high voltage operation with higher number of levels in the output voltage; the latter causes significant efficiency benefits due to reduced harmonic levels in the output current. On the other hand, parallelly connected inverters are more concerned about the latter benefit; they provide means of increasing the quality of the output current as well as the current rating of the system in contrast to voltage related benefits. Fig. 2.4(a) and Fig. 2.4(b) show two variations of standard parallel inverter systems.



(a) Ac ripple cancellation method (b) Inter-phase transformer method

FIGURE 2.4: Commonly used parallel inverter topologies

Consider upper and lower legs of phase A of the system shown in Fig. 2.4(a). If the legs are switched without any overlap in the switching pattern, the output current is shared between the two legs and are in phase ($i_{a1} = i_{a2} = i_a/2$). This reduces the current stress on each inverter by half, or alternatively, doubles the systems current capacity. Note that, here the output phase-voltage is 2-level. But, if the switching between the two legs are interleaved (see Section 2.2) [23], then i_{a1} and i_{a2} become out of phase by half a carrier period ($T_c/2$), and interestingly results in a 3-level pattern for the phase-voltage, while still sharing the fundamental output current [24]. This is commonly known as the *AC Ripple Cancellation* method of parallel inverters [10, 11], and is beneficial as it reduces the ripple of the output current [10, 25] and minimizes output ac filtering requirements.

Now with a slight modification to the setup, a center-tapped coupled inductor is placed between the outputs of each leg as shown in Fig. 2.4(b) (consider the case where the three phases are not coupled to each other and have separate magnetic cores). With

interleaved switching, the tight coupling of two windings results in a significant reduction in the high frequency winding current ripple. Moreover, since the two top and bottom winding portions of the center-tapped inductor are on the same magnetic core for each phase, the resulting fundamental fluxes due to each winding cancels out. This phenomenon is a key concept in CII theory, and marks the arrival of the topological platform of this thesis work. The operation principles of parallel inverters and how it is tied with the principles of the CII is described in more detail in Chapter 3.

2.2 Modulation Techniques

Choosing a correct PWM scheme is essential in designing an efficient power electronic converter system. In an inverter, the power semiconductor switches have to be switched in a certain pattern such that the underlying fundamental of the pulsed output waveform is what is required by the load. The technical method of generating these switching patterns is known as a *Modulation Technique (or a Modulation Scheme)* in the literature. Following are the basic techniques that are widely used:

- Square Wave Switching
- Selective Harmonic Elimination (SHE)
- Pulse Width Modulation

The choice as to which technique to use depends upon the application requirement, but it is safe to state that PWM is the most widely used modulation technique in power electronic systems. And when it comes to PWM, there are numerous sub techniques known as *PWM Schemes* which are discussed in the latter part of this chapter.[8]

The square wave switching method can be regarded as the simplest of modulation techniques [4]. Here, the power switches themselves switch at the fundamental frequency (i.e. switching frequency and the fundamental frequency are the same: $f_{sw} = f_1$). This allows the use of slow switching semiconductors, resulting in less complex gate drivers and lower switching and conduction losses. The frequency of the output waveform could be controlled by adjusting the square wave frequency should a need for varying the output fundamental frequency arises. However, the controlling of the converter output waveform

[8] Actually, square wave switching is a special case of the PWM technique.

magnitude requires an additional converter at the input, usually a thyristor converter [4].[9] As promising as the above factors sound, there is an important drawback of this method. Square wave switching introduces a significant amount of lower order harmonics to the power converter output which are practically hard to filter.

Selective Harmonic Elimination is an extension of square wave switching with an added extra feature. This technique manipulates the phase shift of the square waves such that the occurrence of some lower order harmonics are inherently avoided.

With the advent of power semiconductor devices with higher operating frequencies (such as IGBTs and MOSFETs), pulse width modulation was introduced as a viable solution for the low order harmonic problem of square wave switching. The key concept behind PWM is that it allows generation of the same fundamental output waveform with required magnitude, but shifts the harmonics in the switching voltage waveform to a higher frequency range where filtering is quite practicable.[10] It should be emphasized that PWM is distinct from the two schemes described above: in PWM, the width of the pulses changes with time, generally using a constant switching/carrier frequency.

2.3 Pulse Width Modulation: Demystifying Concepts

Although there are quite a number of modulation schemes based on PWM in current literature, there are two major sub techniques of PWM which are identified as follows:

1. Carrier based PWM: (a) Sinusoidal (b) Non-Sinusoidal
2. Space Vector based PWM

The modulation technique of PWM was invented on a principle known as *Carrier based Sinusoidal PWM* [27]. As the name implies, a carrier signal (usually triangular) is compared with a sinusoidal reference signal (also known as the *Modulating Signal*) to generate the switching signals for the switches. A known limitation with carrier based PWM is its linear modulation range which is limited to 1 ($m_a \leq 1$). If the system is operated above this limit, over modulation occurs and low order harmonics are introduced to the system [4].

[9] For a full-bridge converter, the need for this extra converter can be eliminated by allowing phase shifted switching (overlap angle control) of the two arms.

[10] For instance, in motor drive applications, the motor leakage inductances are quite sufficient to filter out these high frequency harmonics, and therefore, no additional output filters are required [26].

As a solution to the limited modulation range problem, a PWM method with an altered reference signal, where the original sinusoidal signal is injected with a zero sequence component, was introduced.[11] This allows to increase the linear modulation range above 1. These methods are known as *Non-Sinusoidal Carrier based PWM* as the original sinusoidal signal is altered. The method originated in early 1980s when Houldsworth and Grant in [28] proposed a concept of injecting a third harmonic to the modulating signal. Although various zero sequence injection methods were proposed which allowed different non-sinusoidal modulating signals [27], there still exist another problem with carrier based PWM: the higher switching losses caused by high frequency switching of power semiconductor devices.

To address the above issue, a *Space Vector* based PWM (SVPWM) method was proposed by van der Broeck, Skudelny, and Stanke in 1986-1988 [29]. In simple terms, SVPWM in reality is a digital implementation of the modulating signal. With the current development of micro-controllers and DSPs, SVPWM has found to be one the most used PWM methods for three-phase converters [27]. An important fact to note here is, that in SVPWM, the combined effect of all the three phases are considered when generating the switching signals; which provides better performance [26]. Furthermore, SVPWM also offers the same increased linear modulation range to that of third harmonic injection method.

Although SVPWM sounds promising, achieving the same benefits becomes impracticable when the number of levels increases in multi-level systems [30]. The selection of switching states becomes quite complex. In this regard, carrier based PWM still provides pragmatic solutions with a much simpler approach. Recently, some researchers have concentrated on identifying the relationship between carrier based PWM and SVPWM to investigate the possibilities of a hybrid modulation scheme [27, 30, 31]. With correct adjustments to the reference signals, or with suitable post processing logic, carrier based PWM can be made to closely offer the benefits of SVPWM [32, 33]. The proposed DPWM method's space vector counterpart is briefly presented in Chapters 3 and 4.

The space vector based perspective offers much insight to the operation of the circuit, especially the magnetizing aspects of the magnetic core. Furthermore, unlike the conventional carrier based PWM, the implemented DPWM scheme considers the combined effect of all three phases when the switching signals are generated, offering some benefits

[11] Zero sequence injection does not add any harmonics to three-phase systems as their components are inherently cancelled in three-phase line voltages.

of SVPWM. Therefore, it is fair to consider the proposed scheme as a hybrid version of conventional SVPWM and carrier based PWM techniques.

The following is a summary of some important terms in reference to the principles of basic PWM, which sometimes are not quite clearly distinguished in the literature. A clear comprehension of these terms is essential as the report quite frequently refers to them.

Carrier based PWM: A carrier signal v_{car} of carrier frequency f_c is compared with a reference signal v_{ref} to generate the gate signals for the power semiconductor switches. Carrier based PWM is twofold: 1) Sinusoidal carrier based PWM where the reference signal is a perfect sinusoidal signal, 2) Non-Sinusoidal carrier based PWM where the original sinusoidal reference signals are altered according to certain criteria.

Space Vector based PWM: In space vector PWM, a fundamental cycle (which is equal to the period of the reference signal, T_1) is divided into sectors [6]. Depending upon the current sector and the position of the rotating reference vector within the sector, a suitable set of switching signals is selected digitally, usually from a look-up table.

Discontinuous PWM: The technique of conventional discontinuous PWM can be regarded as a PWM approach with a set of non-sinusoidal references. The term "*discontinuous*" means that either one or more switches are not continuously switched for a certain part of the fundamental cycle.[12] For instance, in the proposed work, phase A is held at the positive rail voltage for a 60° period of the fundamental cycle (both T_{A+} and T_{A-} in Fig. 1.3 are kept at ON state to be precise). Note that, it is also possible to implement discontinuous PWM using space vector PWM methods [6].

Interleaved Switching: The term "*interleaved*" is more often used in juxtaposition with parallelly connected inverters. Interleaving is not strictly speaking a PWM method, but an operation principle of the total inverter system (i.e. a combination of the used topology and the PWM scheme and its logic scheme). The simplest example is the interleaved boost inverter [34], where two regular boost converters are connected in parallel and operating 180° out of phase. The interleaving between two inverter legs (top and bottom) is usually acquired by comparing a reference signal with two carriers overlapping each other by a certain phase (usually 180°). The important fact to note here is that there exist time periods where both top and bottom switches,

[12] A comprehensive analysis on DPWM is presented in the book *Pulse Width Modulation for Power Converters* by Holmes and Lipo [1].

of the two boost converters for example, are at *ON* state simultaneously. This is an inherent characteristic of interleaved systems; for instance, in the CII topology this is what allows the energization of the magnetic core (both T_{A+} and T_{A-} in Fig. 1.3 are switched *ON* simultaneously to provide a positive excitation for the phase-A winding). A simple analysis on interleaving with example waveforms is presented in Appendix A.3 as supplementary material should the reader is interested in simulating or testing the technique.

2.4 The Coupled Inductor Inverter and Discontinuous PWM Approach as a Beneficial Three-Phase Inverter Solution

The material presented so far in this chapter is aimed at familiarizing the reader on current developments in inverters and PWM techniques with some important terminology.[13] However, it is quite important to identify the underlying reasons that resulted in the proposed work; and therefore, a brief summary of the relevant developments is presented, laying forward the potential design problems identified during the early stages of the work.

To this date, the standard 2-level three-phase inverter is the prevalent choice for low to medium voltage systems due to its low cost and simplicity [15]. However, 3-level topologies such as 3-level NPC and parallel inverters are emerging as better solutions due to their finer output quality and reduced filter requirements. As mentioned in Section 2.1.3, although the standard parallel inverters with interleaved switching offer significant advantages in the output current quality, the practical problems of increased number of power semiconductor switches and the still existing need for output ac filter inductors put the researcher once again in the task of finding a better topology.

The CII topology was introduced as a pragmatic solution to the problems with the conventional 3-level inverter solutions. The topology reduces the number of power semiconductors by half and practically eliminates the need for output filter inductances, while providing better performance than the conventional parallel inverter system. The introduction of the CII offered better topological benefits and cost performances; however, the

[13] Note that, as the proposed work is based on a DPWM scheme with interleaved switching, the operating aspects of basic DPWM and interleaved switching are extensively discussed in the next chapter.

conventional interleaved PWM approach still hindered its performance potential. Furthermore, selection of a proper magnetic core was another issue under consideration for few years. It was found that a 3-limb magnetic core offers substantial performance benefits for a three-phase CII system in contrast to three independent toroidal cores [12].

The next problem under consideration was to develop a suitable PWM scheme which would offer better utilization of power switches while providing suitable excitation for the 3-limb magnetic core. In this regard, interleaved DPWM inherently offers some basic requirements of the core excitation; for example, standard DPWM inherently avoids some of the undesirable switching states in the 3-limb core based CII topology [11, 12].

Firstly, in this work, a modified version of the conventional DPWM scheme (MD-PWM1) is studied as a baseline. The major design problem at hand was to realize a complex scheme in a DSP with lower resources. A summary of the design problems is as follows:

- Generation of the reference signals for the modified DPWM scheme inside a DSP environment for three phases.
- The modified DPWM scheme compares the two reference signals with two carriers. The DSP only supports comparison of two reference signals with only one carrier.
- The modified DPWM scheme requires post-processing of output logic signals of the modulation unit: this requires access to carriers internally. But, a DSP usually does not allow post-processing of PWM signals, and therefore, this necessity had to be eliminated.
- It is required to flip the winding excitation at the midpoint of each carrier cycle. Therefore, switching logic has to be altered twice during a carrier cycle.

All these design problems were successfully solved and more details on these issues and how they were overcome are presented in Chapter 4. Furthermore, in parallel to addressing the PWM based design problems, a low voltage inverter system with power MOSFETs as switches was to be developed as a laboratory prototype system for PWM concept testing. The design issues with the development of this experimental hardware setup and the practical solutions to those issues are addressed in Chapter 5.

Chapter 3

The Coupled Inductor Inverter and the Excitation of the 3-Limb Core

The English chemist and physicist Michael Faraday (1791-1867) introduced the concepts of electric and magnetics fields as invisible fields transmitting force. But, Faraday was not clear on how the force was transmitted. Later, the British physicist James Clark Maxwell (1831-1879) took the works of Faraday and others, and delivered the classical electromagnetic theory with the famous Maxwell's equations stating that the forces are carried by electromagnetic waves. In modern physics, now it is well established that electromagnetic force is indeed transferred by photons, the particles of light.

The principles of electromagnetism are a critical substance of modern electrical engineering: from microwave circuits and transformers to studies on high energy electromagnetic transients. It is studied how magnetic coupling between two windings helps to deliver a better inverter topology; and more importantly, how to enhance the performance of the corresponding magnetic unit with a modified version of the conventional DPWM technique.

An in-depth analysis of a CII leg is presented with reference to common and differential mode circuits, alongside with its four switching states that are utilized to excite windings on a 3-limb core. Two standard DPWM schemes (SDPWM1 and SDPWM2) and one modified DPWM scheme (MDPWM1) are analysed for their suitability to excite the 3-limb core, with detailed explanations on design equations and modulation logic. It is shown, conceptually, that MDPWM1 can deliver the excitation requirements of the 3-limb core.

3.1 Inverters in Parallel: a Different View on Implications

THE operation of the coupled inductor inverter from a topological perspective is presented. It is shown how there exists a logical transition from the basic principles of parallel inverters in to the operation of the CII topology. This approach provides a clear and meaningful arrival at the topology of this work. Note that, a brief introduction to inverters in parallel operation is provided in Section 2.1.3.

3.1.1 Common and Differential Mode Analysis of Parallel Inverter Legs

Consider the representation of a single phase (*phase-A*) of a standard parallel inverter system as shown in Fig. 3.1. The dc rails of the top and bottom legs are connected to a common dc source, V_{dc}. The outputs of each leg (A_1 and A_2) are in series with two inductors whose common point acts as the phase-A output node, A. The output voltages of each leg with respect to the common negative rail (n) are expressed as v_{A_1n} ($= v_x$) and v_{A_2n} ($= v_y$), where they can assume voltages of either V_{dc} or 0.

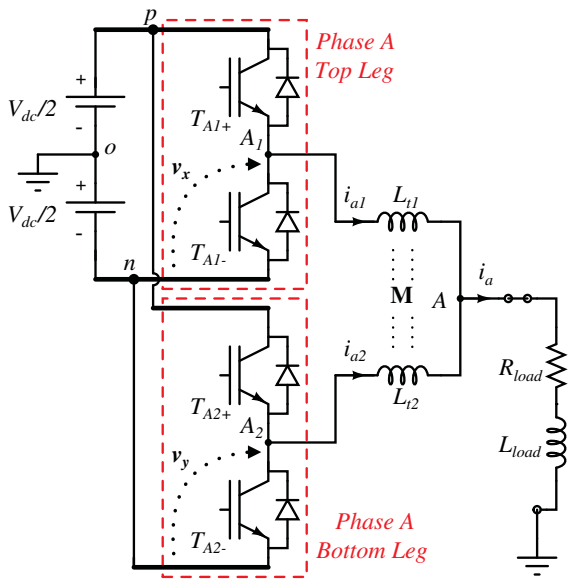


FIGURE 3.1: Single phase (A) equivalent of a standard three-phase parallel inverter system with output inductors at each leg's output

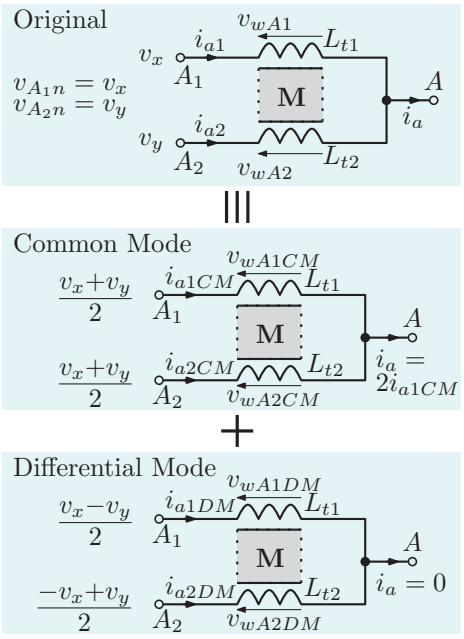


FIGURE 3.2: Common Mode and Differential Mode views of the output as seen from the load side

The two inductors have self inductances L_1 and L_2 and leakage inductances L_{L1} and L_{L2}, and L_{t1} and L_{t2} give the total of the these inductances ($L_{t1} = L_1 + L_{L1}$ and $L_{t2} = L_2 + L_{L2}$). The mutual inductance between the two windings is M, and both $M = 0$ (not-coupled) and $M \neq 0$ (coupled) cases are applicable.[1] For $M = 0$, the two windings are wound on separate cores; and for $M \neq 0$, they are mutually coupled windings wound on the same core: in other words they are the top and bottom parts of a centre-tapped inductor.

The operation of the output side of the circuit, comprising the voltages v_{A_1} and v_{A_2} and the two inductors, can be easily described if the common and differential modes of operations are considered [24]. This is illustrated in Fig. 3.2 where the top circuit is equivalent to the summation of two bottom circuits (for instance, $v_x = \frac{v_x+v_y}{2} + \frac{v_x-v_y}{2}$ and $v_y = \frac{v_x+v_y}{2} + \frac{-v_x+v_y}{2}$). For this analysis, assume that the two inductors are identical; i.e. $L_{L1} = L_{L2}$ $(= L_L)$ and $L_1 = L_2$ $(= L)$, so that $L_{t1} = L_{t2}$ $(= L_t)$. It should be emphasized, that in this circuit, the voltages are the driving force and the fluxes in the core are the result (not the other way around). For instance, the dot convention of the two inductors simply dictates the direction of the flux (not the voltage) that each winding induces in the core.

In the common mode circuit, the voltages at points A_1 and A_2 are the same $(v_x + v_y)$, and therefore, the currents flowing in both windings are equal ($i_{a1CM} = i_{a2CM}$). The general expression for the voltage across the top winding is:

$$v_{wA1} = L_t \frac{d}{dt} i_{a1} + M \frac{d}{dt} i_{a2} \tag{3.1}$$

Now, for the common mode circuit this translates to the following:

$$\begin{aligned} v_{wA1CM} &= L_t \frac{d}{dt} i_{a1CM} + M \frac{d}{dt} i_{a2CM} \\ v_{wA1CM} &= (L_t + M) \frac{d}{dt} i_{a1CM} = v_{wA2CM} \end{aligned} \tag{3.2}$$

Therefore, the common mode circuit resembles two inductors operating in parallel with equal voltages dropped across them.

[1] The terms self, leakage and mutual (as well as magnetizing) inductances could be confusing. Therefore, it is recommended to refer to Appendix C for a well documented step-by-step derivation of these terms based on magnetic theory.

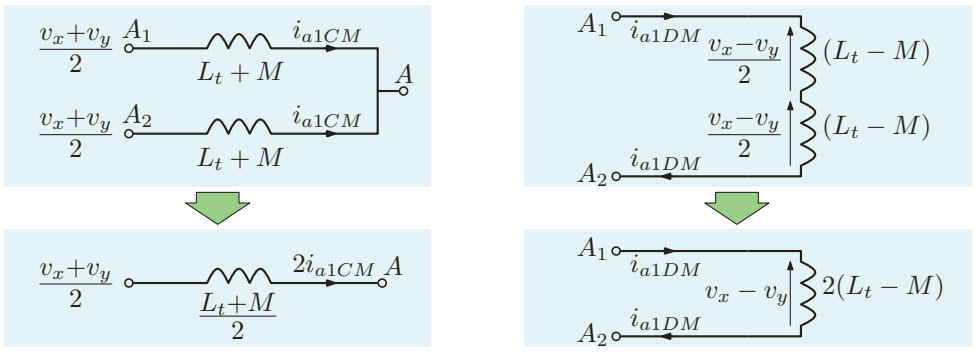
For the differential mode circuit (or the circulating mode), there exists a current that circulates from point A_1 to A_2 as shown in Fig. 3.2 such that $i_{a1DM} = -i_{a2DM}$. And, the voltage across the top winding for the differential mode (v_{wA1DM}) is derived as:

$$v_{wA1DM} = L_t \frac{d}{dt} i_{a1DM} + M \frac{d}{dt} i_{a2DM} = (L_t - M) \frac{d}{dt} i_{a1DM} \tag{3.3}$$

And the voltage across the bottom winding for the differential mode is given by:

$$\begin{aligned} v_{wA2DM} &= L_t \frac{d}{dt} i_{a2DM} + M \frac{d}{dt} i_{a1DM} \\ v_{wA2DM} &= -(L_t - M) \frac{d}{dt} i_{a1DM} \end{aligned} \tag{3.4}$$

Therefore, the differential mode circuit resembles two inductors in series across a total voltage of: $\frac{v_x - v_y}{2} - \frac{-v_x + v_y}{2} = v_x - v_y$. This suggests, that in this mode, the voltage at point A (v_A) is equal to 0 V (which is equal to the dc-link mid point voltage). Therefore, no current flows out of this point to the load (see how the load's other end is connected to the ground terminal in Fig. 3.1, which is connected to the dc-link mid point). This is an important result as it proves that the load current exists only in the common mode operation. Above realizations are illustrated in Fig. 3.3 as the final equivalent circuits of the two modes of operation.



(a) For common mode operation

(b) For differential mode operation

FIGURE 3.3: Equivalent circuits for a single leg of a parallel inverter system

The analysis presented above, as represented by the inductor equivalent circuits in Fig. 3.3, establishes some important characteristics of the CII systems connected in parallel, whilst serving as a useful aid to describe the evolution of different types of parallel inverter concepts:

1. **The Basic Parallel Inverter (no interleaving/not coupled):** the basic parallel inverter operates without interleaved switching. The top and bottom legs are switched using the same PWM logic, and therefore, v_x is always equal to v_y. And consequently, the voltage driving the differential mode operation ($v_x - v_y$) becomes zero. This is why, theoretically, there is no circulating current in standard parallel inverters. However, there exists a circulating current in practical circuits, mainly due to device mismatches and switching synchronization problems.

2. **Parallel Inverters with Interleaved Switching (not coupled):** in a simple parallel inverter setup, the load voltage and current is fully controlled by the common mode voltage $\frac{v_x+v_y}{2}$ (irrespective of the differential mode operation). Without interleaved switching of the top and bottom legs (of each phase), v_x and v_y are always equal and have the values 0 or V_{dc}: resulting in a 2-level voltage of either 0 ($\frac{0+0}{2}$) or V_{dc} ($\frac{V_{dc}+V_{dc}}{2}$) as the common mode driving voltage. Now, if the switching is interleaved (i.e. the two legs are switched using two carriers with 180° phase shift), we are presented with a very interesting option with the emergence of two additional switching states: 1) $v_x = 0$ and $v_y = V_{dc}$ and, 2) $v_x = V_{dc}$ and $v_y = 0$. Both states result in an additional voltage level, $\frac{v_x+v_y}{2} = \frac{V_{dc}}{2}$, in the common mode driving voltage. Therefore, with interleaved switching, it is possible to achieve 3-level output voltages at each phase output; for example, v_A can take the voltage levels 0, $\frac{V_{dc}}{2}$ or V_{dc}.

3. **Parallel Inverters with Interleaved Switching and Coupled Inductors:** so far, the analysis is carried out with disregard to the role of the mutual inductance M of the two inductors (top and bottom). First, consider the case with non-coupled inductors ($M = 0$): the term M in the equivalent circuits in Fig. 3.3 becomes zero. The load current sees an effective inductance of $L_t/2$, which results in a fundamental voltage drop that lowers the effective load voltage [11]. The circulating current sees an inductance $2L_t$, which opposes the high frequency winding current ripple.

   Now consider the case where the two inductors are coupled. Since $L_{t1} = L_{t2}$, $|M|$ equals to L ($|M| = k\sqrt{L_1 L_2} = L_1 = L$,[2] assuming the coupling factor $k = 1$ with tight coupling between the two windings). The most interesting case occurs when M is a negative quantity ($M = -L$).[3] For this case, the effective inductance seen by the

[2] See Appendix C.2.1 for the derivation of this result.

[3] Whether M is negative or positive depends upon the dot convention of the two windings, and this has no effect on the directions of the circuit currents as $|M| < L$.

load current is calculated as (considering the common mode circuit in Fig. 3.3(a)):

$$L_{eff} = \frac{L_t + M}{2} = \frac{(L + L_L) - L}{2} = \frac{L_L}{2} \tag{3.5}$$

It is apparent, that now the inductance seen by the total load current is half the leakage inductance of a winding, as opposed to $L/2 + L_1/2$ of the non-coupled case. This causes a dramatic reduction of the fundamental voltage drop across the inductors and hence offers more voltage to the load.

And most importantly, the inductance opposing the circulating winding current is further increased (beyond $2L_t = 2L + 2L_L$ of the non-coupled case):

$$2(L_t - M) = 2[(L + L_L) - (-L)] = 2[2L + L_L] = 4L + 2L_L \tag{3.6}$$

This result shows that with negative mutual inductance, it causes a 200 % increase (neglecting L_L) in the impedance seen by the circulating current. This causes a significant reduction in the high frequency winding current ripple.

Note that, since it is assumed that the two windings are identical, the following terminology is used for the rest of the chapter: $L_{L1} = L_{L2} = L_L$ and $L_1 = L_2 = L$.

3.1.2 Coupled Inductors: Behaviour of the Flux in the Magnetic Core

Another important aspect of coupling two inductors is the distribution of the magnetic flux inside the common core. For the non-coupled case, there is no mutual flux existing between two windings. However, when the two windings are coupled such that $M = -L$ as discussed in Section 3.1.1, the behaviour of the common mode circuit shows interesting results.

The apparent similarity between the modulation techniques of interleaved switching (with 180° phase-shifted carriers) for two parallel inverter legs and unipolar PWM for full-bridge converter is quite interesting. This is an important practical consideration, and might incur confusion as the two methods have a similar logic, although they have a clear distinction. It is recommended to refer to Appendix A.3 to obtain a clear understanding of this matter.

If the two windings are coupled such that $M = -L$, the resulting common mode circuit is illustrated in Fig. 3.4 with required dot conventions to achieve a negative value

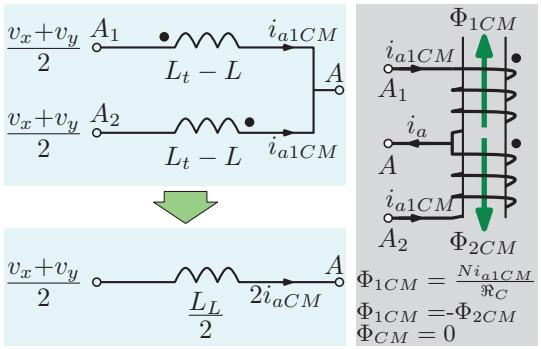


FIGURE 3.4: Common mode operation with coupled inductors ($M = -L$) and the resulting flux distribution in the core

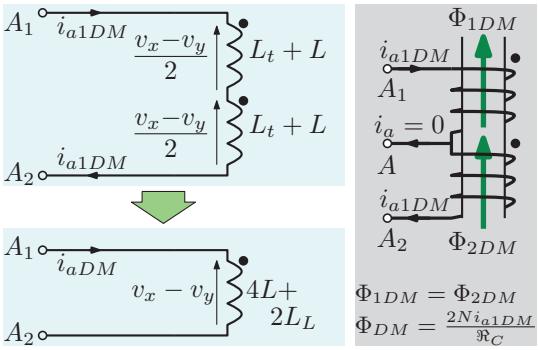


FIGURE 3.5: Differential mode operation with coupled inductors ($M = -L$) and the resulting flux distribution in the core

for M. Before performing flux analyses on the core, it is quite important to understand the dc, high frequency and fundamental components of the winding currents.

The common and differential mode currents of the final equivalent models are defined as i_{aCM} $(= i_{a1CM} = i_{a2CM})$ and i_{aDM} $(= i_{a1DM} = -i_{a2DM})$ respectively. The total common mode output current $(2i_{aCM})$ consists of the fundamental output load current, i_{a_F}, and a high frequency component, i_{aCM-HF}; where i_{aCM} is given by:

$$i_{aCM} = i_{a1CM} = i_{a2CM} = \frac{1}{2}(i_{a_F} + i_{aCM-HF}) \tag{3.7}$$

And the differential mode current consists of a dc and a high frequency component:

$$i_{aDM} = i_{a1DM} = -i_{a2DM} = i_{a_{dc}} + i_{aDM-HF} \tag{3.8}$$

Note that, $i_{a_{dc}}$ is ideally zero for the basic parallel inverter system since the voltage that is driving it, $v_x - v_y$, in an average sense (over a fundamental cycle) has a zero dc component. But, practically it is not zero due to various non-ideal aspects. With the aid of above derivations, the winding currents of the top and bottom coils can be expressed as follows;

$$\begin{aligned} \textit{Top Winding}: \quad & i_{a1} = i_{a1CM} + i_{a1DM} \\ & i_{a1} = \frac{1}{2}(i_{a_F} + i_{aCM-HF}) + (i_{a_{dc}} + i_{aDM-HF}) \end{aligned} \tag{3.9}$$

$$\begin{aligned} \textit{Bottom Winding}: \quad & i_{a2} = i_{a2CM} + i_{a2DM} = i_{a1CM} + (-i_{a1DM}) \\ & i_{a2} = \frac{1}{2}(i_{a_F} + i_{aCM-HF}) - (i_{a_{dc}} + i_{aDM-HF}) \end{aligned} \tag{3.10}$$

The common mode current and circulating current of the final equivalent models (i_{aCM} and i_{aDM}) are related to the top and bottom winding currents as follows:

$$i_{aCM} = \frac{i_{a1} + i_{a2}}{2} \tag{3.11}$$

$$i_{aDM} = \frac{i_{a1} - i_{a2}}{2} \tag{3.12}$$

Since the windings are identical and carry the same current in common mode circuit, they produce fluxes of equal magnitude, but in opposite directions in the magnetic core limb; and therefore, result in a zero resultant flux (Φ_{CM}) in the core (see Fig. 3.4).

$$\Phi_{CM} = \Phi_{1CM} + \Phi_{2CM} = \Phi_{1CM} + -\Phi_{1CM} = 0 \tag{3.13}$$

This shows that the effective flux induced in the phase core due to the output load current is zero (due to both i_{a_F} and i_{aCM-HF}). Since the flux induced in the core at load fundamental frequency becomes zero, this results in a significant reduction the core size for the magnetics [12]. Continuing the analysis: with reference to Eqs. (3.9) and (3.10) the output current of leg A, i_a, is the addition of i_{a1} and i_{a2};

$$\begin{aligned} i_a &= i_{a1} + i_{a2} \\ i_a &= 2 \times \frac{1}{2}(i_{a_F} + i_{aCM-HF}) + (i_{a_{dc}} + i_{aDM-HF}) - (i_{a_{dc}} + i_{aDM-HF}) \\ i_a &= i_{a_F} + i_{aCM-HF} = 2i_{aCM} \end{aligned} \tag{3.14}$$

This result shows that the leg output current only contains components (i_{a_F} and i_{aCM-HF}) of the common mode circuit. These components effectively face an inductance of $L_L/2$ at the leg output. A similar analysis on the differential mode operation shows that flux induced by the two windings due to the differential current adds up in the magnetic core (see Fig. 3.5).

$$\Phi_{DM} = \Phi_{1DM} + \Phi_{2DM} = \Phi_{1DM} + \Phi_{1DM} = 2\Phi_{1DM} \tag{3.15}$$

This flux consists of two components: a high frequency flux and a dc flux due to the current components i_{aDM-HF} and $i_{a_{dc}}$ respectively. Both these current components see an effective inductance of $4L + 2L_L$ when circulating through the winding.

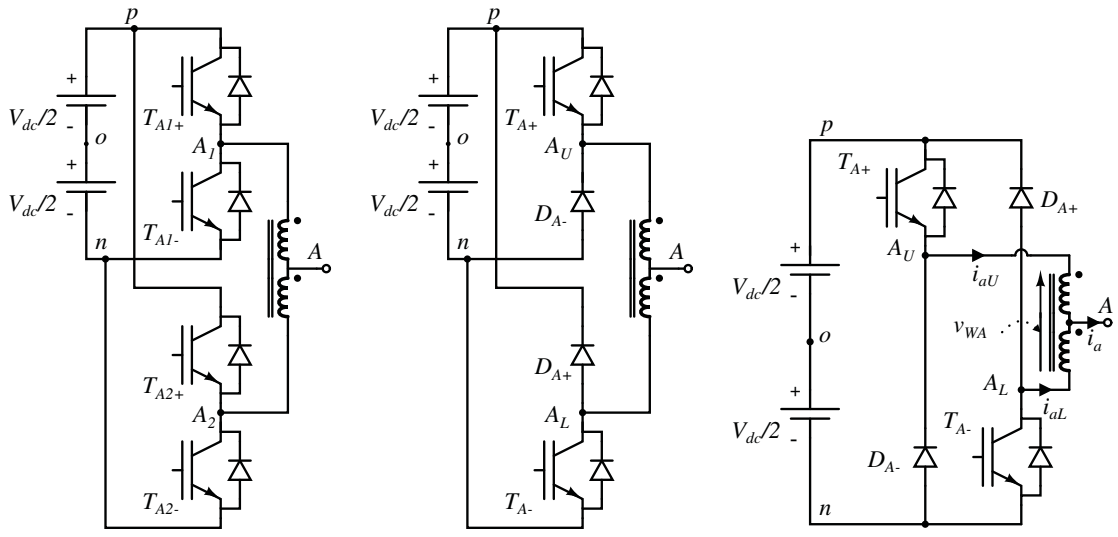
In conclusion, for the coupled case ($M = -L$), the magnetic core is excited due to the operation of the differential mode circuit only. And the common mode circuit has no effect

on the flux in the core. In other words, only the dc and high frequency circulating currents excite the magnetic core. So far in this chapter, a step-by-step analysis has been presented to provide an in depth insight to the concept of coupling two inductors in a parallel inverter system. This serves as a formidable introduction to the operation of coupled inductor inverters.

3.2 The Coupled Inductor Inverter

The coupled inductor inverter concept can be considered as an extension of the parallel inverter concept presented earlier, but with some additional and interesting benefits. For comparison, Fig. 3.6(a) and Fig. 3.6(b) show single phase representations of the two systems. If the two inductors are coupled in each phase, it is logical to consider the three-phase parallel inverter approach as a *Twelve-Switch CII Topology (12-CII)*; and with same convention, the CII topology with 6 switches can be named as a *Six-Switch CII Topology (6-CII)*.

The work in this thesis concerns the six-switch CII topology, and therefore, for the remainder of the report, the term CII refers to the six-switch version. Consider Fig. 3.6. From a hardware perspective, the most apparent distinction is that a 6-CII topology has



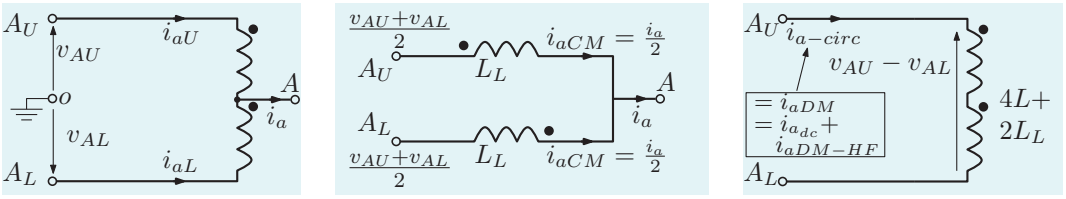
(a) case: 12-CII (b) case: 6-CII (c) case: Simplified 6-CII

FIGURE 3.6: Representation of a coupled inductor inverter leg: phase A

only six active switches compared to the twelve of the three-phase parallel inverter (for instance, in 6-CII, the switches T_{A1-} and T_{A2+} of 12-CII are replaced with diodes). Note that the presence of the split dc-link in both topologies is to facilitate the illustration of some conceptual voltage waveforms. In practise, only a single dc-link capacitor is sufficient; and note that, the 3-level NPC topology exclusively requires a split dc-link [13].

Standard interleaved switching (or other modulation scheme introduced later in the report) results in the same voltage pattern (at points A_U and A_L) for both 12-CII and 6-CII topologies.[4] In the 12-CII topology, the switch pairs T_{A1+}, T_{A1-} and T_{A2+}, T_{A2-} are made to be complementary to avoid dc-link shoot-through conditions. However, a simple look at the 6-CII topology shows that there is no dc-link shoot through problems for the top and bottom legs in an individual sense (due to the diodes D_{A+} and D_{A-} in each leg). In fact, due to the presence of the coupled inductor, a dc-link shoot-through via switches T_{A+} and T_{A-} (when the two legs are considered together) is also not possible. This is one of appealing characteristics of the six-switch approach that is inherent to the topology [10].

One of the main distinctions of the 6-CII topology is the behaviour of its circulating current. Consider Fig. 3.7 which shows the redefined common and differential mode circuits for the 6-CII topology alongside with Fig. 3.6. The inclusion of diodes D_{A+} and D_{A-} (in place of IGBTs/MOSFETs of 12-CII) inhibits the bi-directionality of the circulating current (i_{a-circ}) passing through the two windings.[5] In fact, the circulating current has a positive dc bias ($i_{a_{dc}}$) approximately equal to a half of the peak value of the leg's output current (i_a): $(i_a)_{peak}/2$ [25, 35, 36]. When the system is first powered up, it can be observed that



(a) Actual circuit (b) Common mode (c) Differential mode

FIGURE 3.7: Common and differential modes redefined with new variable names in accordance to Fig. 3.6(c)

[4] Gate signals for the switch T_{A1+} in 12-CII and T_{A+} in 6-CII are identical. And the same applies for the switches T_{A2-} and T_{A-}.

[5] Throughout the report, the terms circulating current (i_{a-circ}) and differential mode current (i_{aDM}) are used interchangeably to denote the same parameter.

i_{a-circ} builds up to this value and finally settles (see Fig. A.18 in Appendix A.5). During this period, the upper winding current (i_{aU}), ramps up while the lower winding current (i_{aL}), essentially stays at zero. After i_{a-circ} is settled at its dc value, i_{aL} gradually starts settling at its steady state behaviour; which is a 180° phase-shifted replica of i_{aU}. Neglecting high frequency current ripples, and considering only fundamental and dc currents, the two winding currents can be expressed as:

$$i_{aU} = i_{a_{dc}} + \frac{i_{a_F}}{2} \tag{3.16}$$

$$i_{aL} = i_{a_{dc}} - \frac{i_{a_F}}{2} \tag{3.17}$$

Investigation of the behaviour of the circulating dc current is quite an extensive subject and is not the main focal point of this work. However, the key points are summarized below as their effects are essential in understanding the experimental current waveforms in the latter part of the report. References [35, 36] address these points in more depth.

- The inverter is said to operate in *Continuous Conduction Mode* (CCM) if the two winding currents are unidirectional (i.e. not crossing zero current level). For this to happen, the circulating dc current should have a net positive value. The anti-parallel diodes of the switches are redundant for this mode as i_{aU} and i_{aL} are always positive.
- The circulating current is affected by parameters such as turn-on and turn-off delays of the switches, diode voltage drops and active device voltage drops.
- The dc value of i_{a-circ} ideally equals to $(i_a)_{peak}/2$. If i_{a-circ} goes below this value, the inverter goes in to the *Discontinuous Conduction Mode* (DCM) of operation.
- DCM results in a degradation in output voltage waveforms (PWM voltage pulses are distorted) as the two windings cannot sustain same voltage levels across them.

In summary, it is shown, that if the paralleling is achieved using coupled inductors for a parallel inverter system, significant benefits can be obtained for the same system: such as reduced high frequency winding current ripple and reduced fundamental voltage drops for the output current. The six-switch CII topology is introduced in place of the conventional parallel inverter system with twelve switches as a better solution. The benefits of the 6-CII over the 12-CII can be summarized as follows [2013]:

- Has half the number of switches that of 12-CII.

- Generates exactly the same voltage pattern at the phase outputs with same control logic with half the number of gate driver and control circuits.
- No occurrence of dc-rail shoot-through conditions.
- There exists an inherent circulating current (always positive) in the windings. This makes certain that the windings always have a negative dc bias voltage: so that the circulating current is inherently controlled to a steady state value in an open loop manner. In conventional parallel inverter systems, the non-ideal circulating current needs complex closed loop controlling.

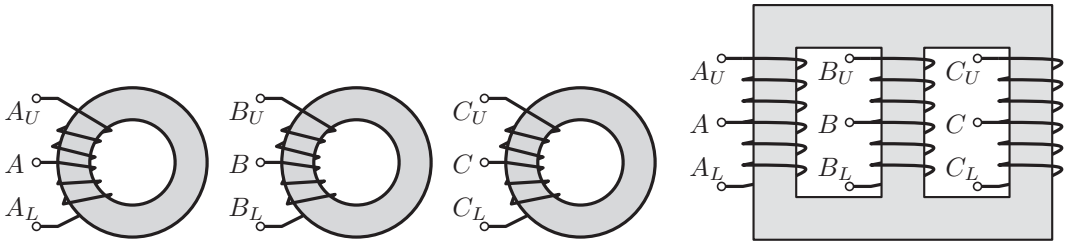
Note that, Appendix A.5 presents a collection of simulated results analysing the effects of using coupled inductors in 12-CII and 6-CII phase legs. These results show the characteristics of winding current ripple and the fundamental voltage drop across windings for four different topology arrangements. The reader is encouraged to refer to these results to obtain a better understanding of the material discussed so far.

3.2.1 Realizing a Three-Phase Coupled Inductor Unit

The 6-CII topology is heavily reliant on its coupled inductors. Therefore, an understanding of the magnetic requirements of these inductors is important. As the modulation schemes are tailored for the switches for basic operation, all the subsequent fine tuning of the schemes are specifically aimed at providing proper excitations for the circuit magnetics. There are, essentially, two ways to implement a three-phase coupled inductor unit [12].

1. Coupling upper and lower coils of each phase (i.e. a centre-tapped coupled inductor) where each phase is magnetically independent of other two phases. An example system with toroidal cores is shown in Fig. 3.8(a).
2. Winding the three sets of coupled inductors on legs of a 3-limb core such that the three phases are magnetically coupled as shown in Fig. 3.8(b).

It was proved that the effective inductance seen by the differential circuit's circulating current is $4L + 2L_L$. The important fact to notice here is that, if the three phases are magnetically independent, this effective inductance is constant and independent of the switching state of each phase. However, if the three phases are magnetically coupled, in the 3-limb core for instance, the fluxes of the three phases interact with each other and



(a) Separate toroidal coupled inductors (b) 3-limb core coupled inductor unit

FIGURE 3.8: Realization of three-phase coupled inductor systems

result in a combined flux distribution. And consequently, the effective inductance seen by the differential mode currents are changed: in fact, it depends upon the switching states of the three phases. Note that, the inductances seen by common mode circuit currents are not affected by this phenomenon as their fluxes are already cancelled in their respective phases (see Section 3.1.1), and therefore, has no bearing to the following analysis.

As shown in Fig. 3.9, consider the mmf generated in the common core due to a single phase x where N is the number of turns of a single winding of the coupled pair of a phase:

$$MMF_x = 2Ni_{xDM} = 2N(i_{x_{dc}} + i_{xDM-HF}) \qquad where,\ x = phase\ a, b\ or\ c \tag{3.18}$$

Here, the $\Re$ terms represent the reluctance of various magnetic flux paths within the 3-limb core (for the time being, neglect the leakage flux paths). If it is assumed that the three limbs are identical (such that $\Re_a = \Re_b = \Re_c$ and $\Re_{ab} = \Re_{bc}$),[6] then the magnetic circuit is

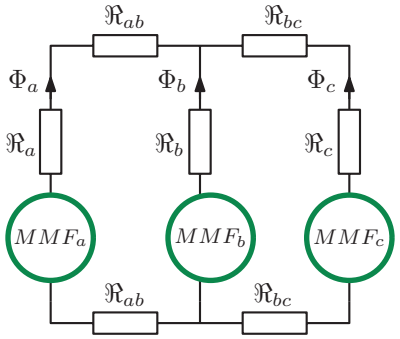


FIGURE 3.9: MMF and flux circuit for the 3-limb magnetic core

[6]The reluctance of a magnetic circuit path is defined as $\Re = l/\mu A$, where l and A are the length and the cross sectional area of the magnetic path respectively. μ is the permeability of the magnetic core [4].

symmetric. Although the fundamental currents in the three phases are 120° apart, the dc components of circulating currents of the three phases ($i_{a_{dc}}$, $i_{b_{dc}}$ and $i_{c_{dc}}$) are equal in ideal conditions. Therefore, the fluxes in the 3-limb core produced by the dc components of the circulating current cancel due to the symmetry of the magnetic circuit [12]. In summary, the following key distinctions are made between 3-limb core and three separate core approaches for the CII magnetic design [12, 14]:

1. The 3-limb core offers significant size benefits due to the compact design compared to three separate cores which effectively result in a larger size.
2. The resultant dc flux in the core due to $i_{a_{dc}}$, $i_{b_{dc}}$ and $i_{c_{dc}}$ is zero for the 3-limb core design. This lowers the core flux density and allows to further reduce the core size.

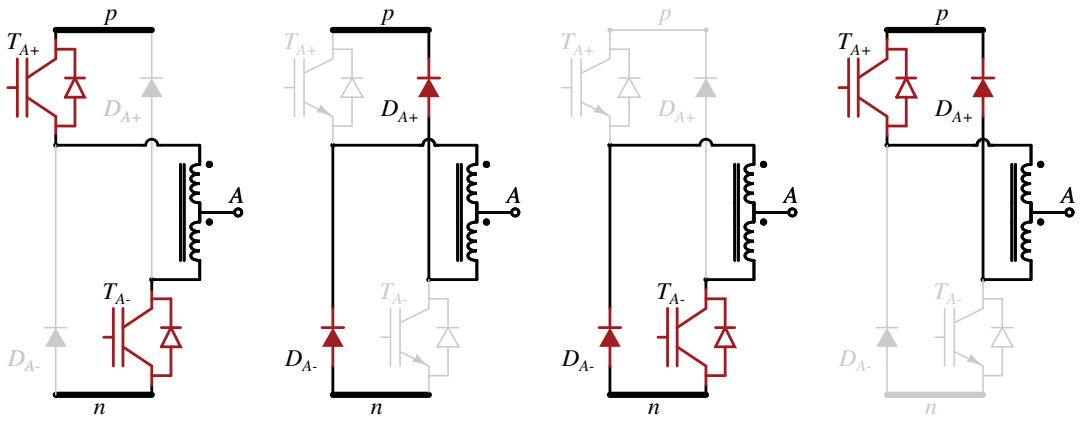
As the 3-limb core offers both size and cost benefits, it presents itself as a formidable option for the magnetic realization of the three-phase inductor system for the CII.

3.2.2 CII Switching States

A modulation scheme controls available switching states of a circuit topology to deliver the required output voltage patterns. The task gets complex when additional requirements, other than the output voltage requirement, have to be satisfied; for example, controlling of the excitation pattern of the magnetic core. In fact, achieving this for a CII topology with a 3-limb core is the main concern of this work. However, before dealing with the modulation scheme, it is important to understand the available switching states of the 6-CII topology (this is a characteristic of the topology and is independent of the modulation scheme) with attention to 3-limb and separate core approaches for the magnetic unit.

In both 6-CII and 12-CII topologies, a single phase consists of two legs (top and bottom or upper and lower). The two legs of a particular phase of the 6-CII topology is collectively termed as a *Phase Leg* as it makes much sense since a single phase usually consists of two switches.

With interleaved switching, four possible states are found for a phase leg as illustrated in Fig. 3.10. The states of two switches, the output voltage at the phase output point A, and the state of the centre-tapped inductor are elaborately tabulated in Table 3.1. The two states $0^E(11)$ and $0^D(00)$ are referred to as the *Zero Voltage States* as they produce an



(a) State 1: $0^E(11)$ (b) State 2: $0^D(00)$ (c) State 3: $-1^S(01)$ (d) State 4: $+1^S(10)$

FIGURE 3.10: The four Switching Modes (States) of a CII leg

TABLE 3.1: Switching States of a CII Phase Leg and Resulting Winding Conditions

T_{A+}	T_{A-}	V_{An}	V_{Ao}	**Winding Voltage**	**Winding Condition**	**State Name**
ON	ON	$V_{dc}/2$	0	$+V_{dc}$	Energized	$0^E(11)$
OFF	OFF	$V_{dc}/2$	0	$-V_{dc}$	De-energized	$0^D(00)$
OFF	ON	0	$-V_{dc}/2$	0	Short circuited	$-1^S(01)$
ON	OFF	V_{dc}	$V_{dc}/2$	0	Short circuited	$+1^S(10)$

Note: the superscripts E, D and S signify the winding conditions 'Energized', 'De-energized' and 'Short Circuited' respectively.

output voltage of 0 V with respect to dc-link mid point o [37]: these two states are only possible due the interleaved switching. With standard switching, only the complementary states $-1^S(01)$ and $+1^S(10)$ exist. The required switching logic to generate the above four switching states for phase A is given by:

$$if \quad v_{refA} > carX \rightarrow T_{A+} = ON \qquad and \qquad if \quad v_{refA} < carX \longrightarrow T_{A+} = OFF \tag{3.19}$$

$$if \quad v_{refA} > carY \rightarrow T_{A-} = ON \qquad and \qquad if \quad v_{refA} < carY \longrightarrow T_{A-} = OFF \tag{3.20}$$

Here, $carX$ and $carY$ refer to two triangular carriers simply phase shifted by 180° (i.e. $carX = -carY$) and v_{refA} is a standard sinusoidal reference signal representing phase A. Both the carrier signals and the reference signals vary between $+1$ and -1 within the control logic unit. The four switching states produce three different voltage levels with a step of $V_{dc}/2$. Conventionally, to get the $V_{dc}/2$ level, a neutral (mid point) connection to the dc-link

is required (ex: 3-level NPC). The advantage of the coupled/non-coupled inductor approach with interleaved switching is that $V_{dc}/2$ voltage level is inherently produced at the output, without any need for a neutral point.

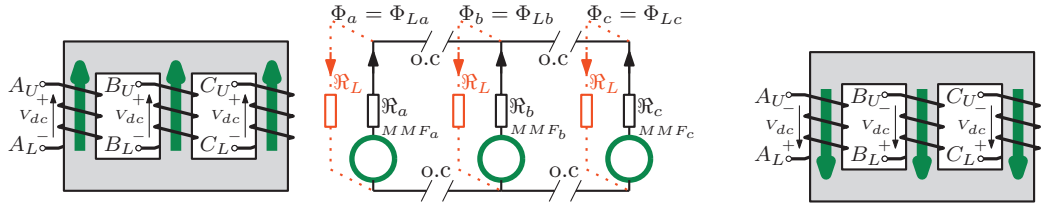
3.2.3 3-Limb Core: How to Channel the Flux

Any potential modulation scheme should satisfy the output voltage requirement on an average sense. However, the core excitation should be handled on an instantaneous basis. The main reason for this is that the fluxes in the magnetic core limbs are voltage driven [15]. Any mishandling of the flux in the core could result in low performance effects as well as some singular catastrophic effects on the system [12].

So far, it has been established that the resultant flux induced in the 3-limb core due to common mode circuit current and the differential mode dc circulating current is zero. Therefore, the only available driving force for the flux in the core is the differential mode high frequency current components of each phase (i_{aDM-HF}, i_{bDM-HF} and i_{cDM-HF}). These currents are driven by the differential voltages (instantaneous) of respective phases (ex: $v_{WA} = v_{aU} - v_{aL}$ for phase A) through corresponding effective inductances. This is why the overall flux in the core is said to be voltage driven in an instantaneous manner. In other words, this means that the flux in the core is operating only in a high frequency mode corresponding to the switching frequency, with no fundamental or dc components.

If the three limbs have identical magnetic characteristics, an interesting condition takes place: consider the situation where the three phases assume either 0^E or 0^D states simultaneously on a particular switching instant (i.e. all the switches in the three phases are either ON or OFF at the same time). In this situation, the instantaneous flux produced in the three phases are the same. And this results in a cancellation of flux: the resultant core flux is zero. This is illustrated in Fig. 3.11 (refer to Fig. 3.10 for the switching states).

Since there is no mutual flux in the core, the circulating currents in each phase see zero effective inductance. Note that, in this case, since the flux is voltage driven, the applied voltages forces the flux to flow through air. However, this only provides a small impedance for the circulating current due to the small leakage inductance of the air path. And, should one consider a flux driven perspective, this essentially represent a short circuited condition for all three windings: winding voltage $= \frac{d}{dt}(\Phi) = \frac{d}{dt}(0) = 0$. Having the windings short



(a) All switches are ON: $MMF_a = Ni_{a-HF} = \Phi_{La}(\Re_L + \Re_a)$. Also, note that $\Re_{ab} = \Re_{bc} = \infty$ due to zero mutual core flux

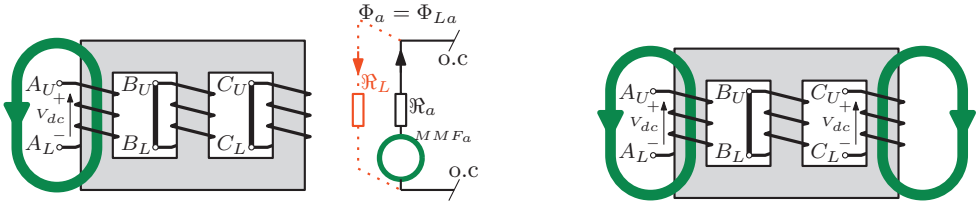
(b) All switches are OFF

FIGURE 3.11: Instantaneous flux cancellation in the 3-limb core with identical limbs

circuited is acceptable; however, the issue here is that, on this particular instant the voltage applied across each winding is either V_{dc} or $-V_{dc}$, and that voltage sees zero impedance. This is catastrophic as this simply short circuits the dc-link capacitor. The modulation scheme, therefore at any cost, must avoid this switching state. Note that, this situation only occurs in the 3-limb core due to the mutual coupling of the three coils, and does not occur in the separate core approach [12].

Other requirements of the magnetic core are mostly performance related criteria (without any harmful effects on the topology). With reference to Fig. 3.10, the switching states -1^S and $+1^S$ apply a zero voltage across the corresponding winding. A winding driven by a zero voltage makes certain that the flux through the winding is always zero causing a magnetic open circuit [15]. On the other hand, the switching states 0^E and 0^D excite the magnetic core, producing positive $\frac{d}{dt}\Phi$ and negative $\frac{d}{dt}\Phi$ flux variations respectively.

Consider the particular switching state of the topology in Fig. 3.12(a) for instance. Here, both B and C phase legs are either in the state -1^S or $+1^S$; such that, both phase windings result in magnetic open circuits in their limbs. Therefore, no flux is allowed to flow through phase B and C limbs. Since phase-A winding is positively excited (0^E), flux



(a) Phase-A positively excited while phases B and C are shorted :$MMF_a = Ni_{a-HF} = \Phi_{La}(\Re_L + \Re_a)$.

(b) Phase A and B positively excited while phase C is shorted

FIGURE 3.12: Undesirable flux paths in the 3-limb core

is forced to increase through phase-A limb, but has no means of flowing through other two limbs. Therefore, this flux is forced to flow through the air, which is a low permeability path offering very low inductance. The combined effective inductance experienced by the flux is therefore determined by air path reluctance ($\Re_L$) and phase-A limb reluctance ($\Re_a$). A similar situation occurs for both phases A and C in Fig. 3.12(b) as phase B is still magnetically open circuited. In this case, phase A and C windings are excited with same polarity. Due to this reason, the mutual flux within the core cancels out and results in zero resultant flux. However, the two mmfs can still force the flux to flow through air gap paths due to the voltage driven nature of the flux.

In the light of above example, the importance of selecting proper switching states (for a given instant) for all the three phases becomes apparent. If any chosen switching state forces flux paths through air, then the effective inductance seen by the high frequency circulating current is altered. In fact, it is lowered: air path presents a low permeability path. Low permeability means higher reluctance, which in turn, means lower inductance.

$$\Re = \frac{l}{\mu A} \quad \longrightarrow \quad \mu \downarrow \rightarrow \Re \uparrow \quad and \quad L = \frac{N^2}{\Re} \quad \longrightarrow \quad \Re \uparrow \rightarrow L \downarrow \tag{3.21}$$

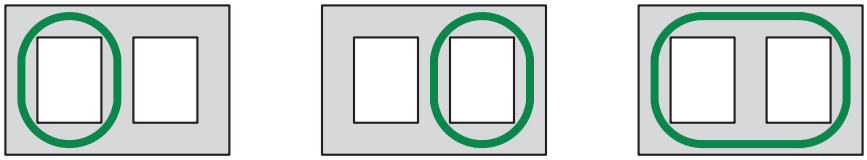
The effective inductance (L_{eff}) seen by a particular phase is what determines the rate of change of the winding current in that phase for a particular switching state ($di/dt = v/L_{eff}$). Therefore, a lower L_{eff} results in a higher current ripple, which is undesirable. This suggests that, if any of the windings are excited, the resulting flux (high frequency flux to be precise) should be maintained within the high permeability core [15].

At this stage, we can identify two basic requirements of the switching states for a 3-limb core based 6-CII topology that should be provided by a potential modulation scheme:

1. The system state where all the three phases assume either 0^E or 0^D states simultaneously (on a particular switching instant) must be avoided.
2. Every switching state should provide maximum effective inductance for the phases with excited windings.

According to these requirements, we can arrive at the following conclusion: there are two possible groups of switching configurations.

1. **One phase is always shorted with either of the states -1^S or $+1^S$. One of the remaining phases is at the state 0^E while the other is at state 0^D. The corresponding flux patterns (and how they are contained within the core) are illustrated in Fig. 3.13.**
2. **All three windings of the three phases are shorted with the states -1^S or $+1^S$ such that there is no flux in the core.**[7]



(a) phase C shorted (b) phase A shorted (c) phase B shorted

FIGURE 3.13: Desirable flux paths for the 3-limb core: one phase winding is shorted while other two windings are excited in opposite directions

Note that, with both configurations, the sum of the three winding voltages is zero for all possible switching states. Therefore, this can be identified as a simple criterion to determine whether a particular PWM scheme is suitable for a 3-limb core excitation [16].

$$\sum v_{WA} + v_{WB} + v_{WC} = v_{W_{tot}} = 0 \tag{3.22}$$

With configuration 2, there are 8 possible switching states for the system (with 2 options for each phase we have $2 \times 2 \times 2 = 8$ possible states). These switching states are illustrated graphically in Fig. 3.14 as vectors $\vec{V_o}$ and $\vec{V_{13}}$ to $\vec{V_{18}}$.

With configuration 1, there are 12 possible switching states for the three phase unit. When one phase is tied, it has 2 options: -1^S or $+1^S$. The other two phases present $0^E, 0^D$ or $0^D, 0^E$ configurations: another 2 options there as well. Therefore, for the three phases, we have $3 \times 2 \times 2 = 12$ possible states. The resulting vectors $\vec{V_1}$ to $\vec{V_6}$ are shown in Fig. 3.14.

Note that, without aforementioned flux channelling requirements of the 3-limb core, a standard 6-CII topology presents 64 possible switching states (with four possible switching states per each phase, we have $4 \times 4 \times 4 = 64$ system states). And with the separate core approach for the three phases, it is possible to use these extra system states. A thorough

[7] This is not in contradiction to the rules. This is an acceptable configuration since the exerted voltages on the windings are also zero.

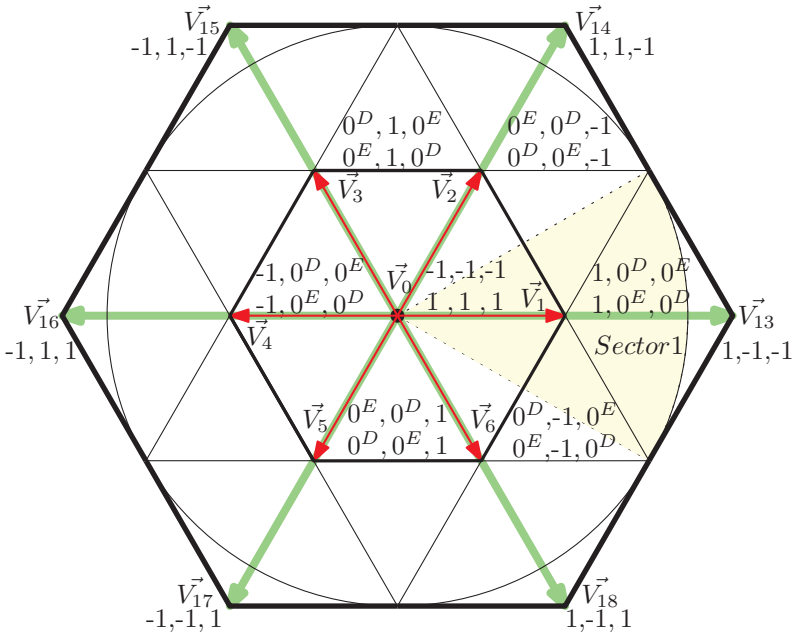


FIGURE 3.14: Desirable switching vectors for a 3-limb core based CII

analysis on these states and their effect on L_{eff} is presented in the references [14] and [37] by Vafakhah et al.. Furthermore, Appendix B provides the basic knowledge on space vector analysis of a three phase system and aids to comprehend the details in above references. The reader is encouraged to refer to these references and Appendix B to acquire a better grasp on the space vector perspective of these states.

3.3 Control of the CII Switches: Modulation Techniques for the 3-Limb Core Approach

A suitable modulation should generate three-phase PWM output voltages while adhering to the general rules of 3-limb core winding excitation. It is shown how a modified discontinuous PWM scheme offers significant performance benefits for a 3-limb core six-switch coupled inductor inverter system.

Standard interleaved switching with regular sinusoidal references allows generation of 3-level output voltages for the 6-CII topology (as well for standard parallel inverter systems). However, handling a 3-limb core based system is not that simple. As identified

in the previous section, the magnetic circuit has its own requirements, independent to the output voltage requirements of the inverter. It is shown that major modifications have to be made to both reference signals and interleaved switching logic to satisfy to 3-limb core requirements.

One requirement identified in the previous sections is that, one winding out of three windings always has to be short circuited (magnetically open circuited): i.e. one phase leg has to be always in the states $+1^S$ or -1^S. As it happens, there already exist a common modulation technique known as Discontinuous PWM (DPWM) which inherently supports this requirement. The DPWM technique can be integrated with interleaved switching to produce a suitable modulation technique for a 3-limb core based 6-CII topology. Note that, additional modifications have to be made to the basic modulation technique such that it satisfies all the above requirements.

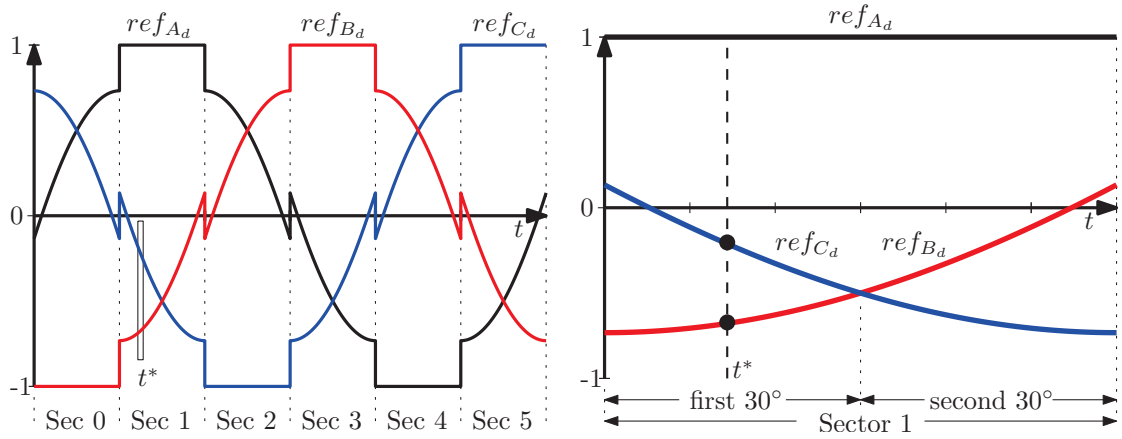
3.3.1 Identifying Suitable Modulation Schemes: Discontinuous Reference Signals with Interleaved Switching

From a practical implementation perspective, discontinuous PWM is not a technique readily explained in text books or publications.[8] But, more importantly the technique of practical execution of DPWM is essential to the development of subsequent schemes of this work; and therefore, this is comprehensively discussed in this report.

The main distinction between conventional sinusoidal PWM and DPWM is the altered reference signals. In DPWM, a fundamental cycle (360° of the original sinusoidal reference) is divided into six *Sectors* of duration 60°; where in each sector, one phase out of the three is kept at either $+1^S$ or -1^S states. This is shown graphically in Fig. 3.15(a), where the modified three phase reference signals are given by ref_{A_d}, ref_{B_d} and ref_{C_d}.

The important equations on how to derive these reference from the original sinusoidal references ref_A, ref_B and ref_C are tabulated in Table 3.2. For the remainder of this report, all the logic comparisons and modulation techniques are explained for ***Sector 1*** as the groundwork (other sectors simply follow the same technique). For instance, consider sector 1 where $ref_{A_d} = 1$. The other two phases are derived by adhering to one simple

[8] The book [1] by Holmes and Lipo thoroughly discusses about DPWM, but it is rather too theoretical and does not present a good sense to its practical realization.



(a) All sectors (b) Sector 1 (phase-A reference tied at +1)

FIGURE 3.15: 60° discontinuous type three-phase reference signals used in the modulation technique known as "Standard DPWM" in technical literature

TABLE 3.2: Standard Three-Phase DPWM Reference Signal Generation Equations

Sector	Tied Phase	Tied Phase State	$\mathbf{ref_{A_d}}$	$\mathbf{ref_{B_d}}$	$\mathbf{ref_{C_d}}$
0	B	-1^S	$-1-(b-a)$	-1	$-1-(b-c)$
1	A	$+1^S$	1	$1-(a-b)$	$1-(a-c)$
2	C	-1^S	$-1-(c-a)$	$-1-(c-b)$	-1
3	B	$+1^S$	$1-(b-a)$	1	$1-(b-c)$
4	A	-1^S	-1	$-1-(a-b)$	$-1-(a-c)$
5	C	$+1^S$	$1-(c-a)$	$1-(c-b)$	1

Note: for simplicity a, b and c represents the original three phase sinusoidal reference signals such that: $a = ref_A$, $b = ref_B$ and $c = ref_C$.

rule: all the new line voltages should produce the same line voltages as the three original sinusoidal references do. For instance, consider the line voltage v_{AB};

$$v_{AB} = ref_A - ref_B = ref_{A_d} - ref_{B_d} \quad \longrightarrow \quad ref_{B_d} = ref_{A_d} - (ref_A - ref_B) \tag{3.23}$$

Since $ref_{A_d} = 1$ for sector 1,

$$ref_{B_d} = 1 - (ref_A - ref_B) \tag{3.24}$$

$$\text{and similarly,} \quad ref_{C_d} = 1 - (ref_A - ref_C) \tag{3.25}$$

By following the same logic, the DPWM references for all the sectors are derived as expressed in Table 3.2. Since the DPWM references inherently produce the states $+1^S$ and -1^S for all

the sectors, this satisfies the requirement of the 3-limb core of always having a magnetically open limb.

It is not a disadvantage of DPWM, during in sector 1 for example, that the output voltage of phase A is not modulated using a sinusoidal shape, but a fixed constant of 1. The reason for allowing such a characteristic is a practical fact that provides better performance. Note that sector 1 is the portion where phase A is highest at its positive voltage, and therefore, carries the highest current under low inductive loads. But, by keeping phase A tied to the positive rail, phase A is not switched throughout the whole sector. This means that there is zero switching losses for phase-A leg during this period; where if switched, would produce the highest switching losses for a phase out of the 360° cycle (similar situation occurs in sector 4, where phase A is at its lowest negative voltage). This is the original reason why DPWM was introduced. And for the 3-limb 6-CII, it just happens that this behaviour exactly suits one of the crucial magnetic circuit requirements.

While phase-A switching is resolved for the specified sector, phases B and C still have sinusoidally varying reference signals that should be modulated with a carrier in a certain manner to produce gate signals for phase B and C legs. For the 3-limb core, the ideal scheme should make certain, that during sector 1, phase B and C windings are excited such that the condition "$v_{W_{tot}} = \sum v_{WB} + v_{WC} = 0$" is always satisfied ($v_{WA} = 0$ for sector 1 as already satisfied by DPWM). It is already established that interleaved switching is the suitable candidate for the 6-CII topology. Therefore, each of the phase B and C legs are expected to switch using interleaved switching with there corresponding references for sector 1. However, there is a question; would simple interleaved switching of the two phases (in an independent manner) satisfy the above 3-limb core requirement of $v_{W_{tot}} = 0$?

TABLE 3.3: Standard Interleaved PWM logic for Phase B (for Sectors 1, 2, 4 and 5)

Carrier Comparison Logic	Phase-B Switches					
	Parallel Inverter				6-CII	
	T_{B1+}	T_{B1-}	T_{B2+}	T_{B2-}	T_{B+}	T_{B-}
$ref_{B_d} > car\ X$	ON	OFF	-	-	ON	-
$ref_{B_d} < car\ X$	OFF	ON	-	-	OFF	-
$ref_{B_d} > car\ Y$	-	-	ON	OFF	-	OFF
$ref_{B_d} < car\ Y$	-	-	OFF	ON	-	ON

Note: in standard interleaved logic, same logic applies for phase C as well : ref_{B_d} is replaced by ref_{C_d}, while phase-C switches replace phase-B ones. The corresponding sectors are: 0, 1, 3 and 4.

The modulation logic for the standard interleaved case is tabulated in Table 3.3. Note the omission of the two switches in 6-CII approach compared to standard parallel inverter (=12-CII) switches and how the logic for the remaining switching is transitioned (see Fig. 3.6 for the topologies). The two phase shifted carriers are defined as *car X* and *car Y*. This is a simple redefinition of the same carrier signals defined in Appendix A: $car\ X = car$ and $car\ Y = -car$. The corresponding waveforms for the time instant t^* (see Fig. 3.15 to identify t^*) in sector 1 are illustrated in Fig. 3.16. Here, the following notation is used:

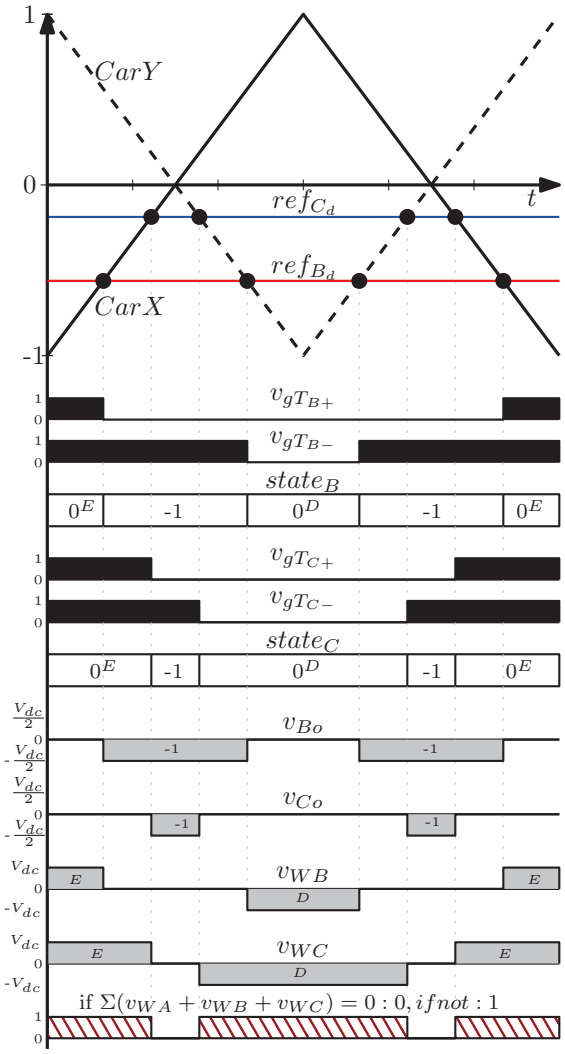


FIGURE 3.16: Standard DPWM with Interleaved Carrier Modulation (SDPWM1): gate signals and voltage waveforms

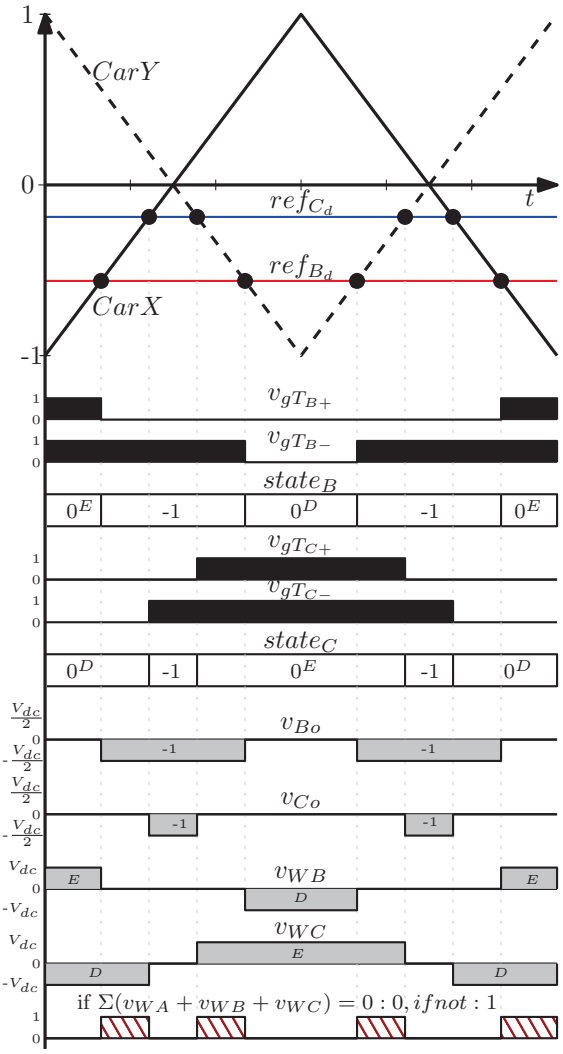


FIGURE 3.17: Standard DPWM with Inverse Interleaved Carrier Modulation (SDPWM2): gate signals and voltage waveforms

$v_{gT_{B+}}$, $v_{gT_{B-}}$, $v_{gT_{C+}}$, $v_{gT_{C-}}$ are power switch gate signals; $state_B$ and $state_C$ represent the variation of the switching states within the carrier cycle; v_{Bo} and v_{Co} are phase output voltages with respect to the dc-link mid-point (o); and, v_{WB} and v_{WC} are the voltages across the phase inductors (top + bottom windings of the centre-tapped inductor). This notation is followed for the rest of the report to refer to these parameters.

Consider the variation of each parameter for phase B and C in Fig. 3.16. It is evident that simple interleaved switching provides required average output voltages for the carrier cycle. However, the winding voltage variations show that whenever a winding is excited, the other winding is either shorted or excited in the same direction; and therefore, not satisfying the requirement "$\sum v_{WB} + v_{WC} = 0$". In fact, this indicates that standard and independent interleaved switching of the two phases is not the obvious solution for 3-limb core magnetization requirements. The two phases have to be treated as a combined unit to manipulate the common flux in the core. This makes sense as the resultant core flux itself is a result of the combined effect of the three phases.

A simple first solution is to devise an *Inverse Carrier Interleaved* DPWM scheme (SDPWM2) in place of the standard interleaved scheme [15]. This is a simple change to the

TABLE 3.4: Comparison of Logic Schemes for DPWM: Standard Interleaved DPWM (SDPWM1), Inverse Carrier Interleaved DPWM (SDPWM2) and Modified DPWM1 (MDPWM1)

Switch	**Standard Interleaved (SDPWM1)**	**Inverse Interleaved (SDPWM2)**	**Modified DPWM1 (MDPWM1)**			
			First $30° = N_u$		Second $30° = N_d$	
			Logic	Name	Logic	Name
T_{B+}	$ref_{B_d} > car\ X$	$ref_{B_d} > car\ X$	$ref\ M > car\ X$ & $ref\ N > car\ Y$	$\boldsymbol{\alpha}$	$ref\ M > car\ Y$ || $ref\ N < car\ Y$	$\boldsymbol{\gamma}$
T_{B-}	$ref_{B_d} < car\ Y$	$ref_{B_d} < car\ Y$	$ref\ M < car\ Y$ || $ref\ N < car\ X$	$\boldsymbol{\beta}$	$ref\ M < car\ X$ & $ref\ N > car\ X$	$\boldsymbol{\delta}$
T_{C+}	$ref_{C_d} > car\ X$	$ref_{C_d} > car\ Y$	$ref\ M > car\ Y$ || $ref\ N < car\ Y$	$\boldsymbol{\gamma}$	$ref\ M > car\ X$ & $ref\ N > car\ Y$	$\boldsymbol{\alpha}$
T_{C-}	$ref_{C_d} < car\ Y$	$ref_{C_d} < car\ X$	$ref\ M < car\ X$ & $ref\ N > car\ X$	$\boldsymbol{\delta}$	$ref_M < car\ Y$ || $ref\ N < car\ X$	$\boldsymbol{\beta}$

Note: the symbols '&'and '||' refer to logical 'AND' and 'OR' operations respectively.

comparison logic which makes the two phases not follow the same interleaved scheme. The new scheme is introduced and compared with the standard case in Table 3.4. Note how phase-B logic is kept unchanged, while for phase C, the corresponding carriers are swapped. The effect of this change is twofold: 1) it does not affect the output voltage patterns of the two phases; and 2) the winding excitation of phase C is swapped such that, for instants where the two phases are excited at the same time, the condition "$\sum v_{WB} + v_{WC} = 0$" is satisfied. The corresponding winding voltage patterns are illustrated in Fig. 3.17.

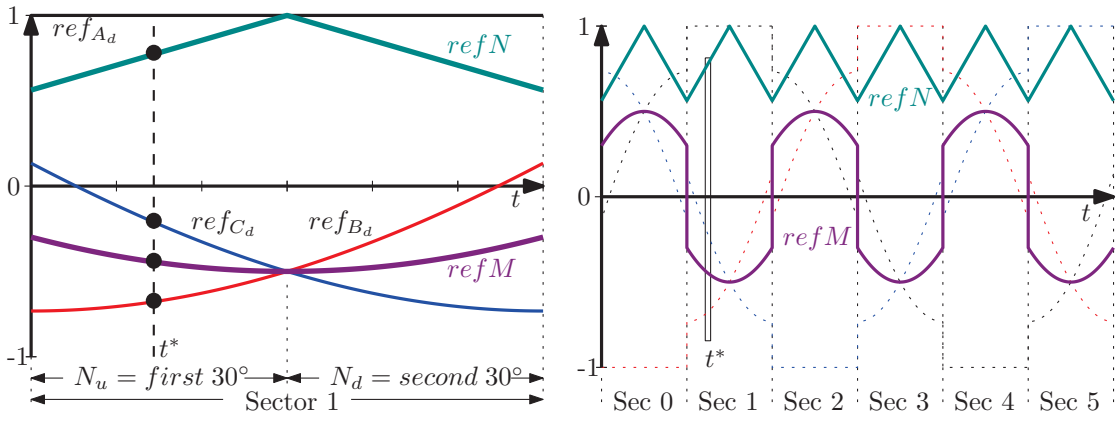
The winding excitation requirement is satisfied only during specific parts within the carrier cycle (but, note the reduction of the total time duration where the condition is not satisfied in contrast to Fig. 3.16). There still exist parts where one winding is excited while the other is shorted such that $\sum v_{WB} + v_{WC} \neq 0$. Therefore, additional measures have to be introduced to the altered modulation scheme, to ensure that the above requirement is satisfied throughout the carrier cycle.

3.3.2 A DPWM Scheme with Modified References and Altered Interleaved Logic: MDPWM1

The main reason, even with the inverse interleaved switching technique, for the existence of time periods within the carrier cycle where the total winding voltage $v_{W_{tot}}$ is non-zero, is the difference between the two reference signals (see ref_{Cd} and ref_{Bd} in Fig. 3.16 and Fig. 3.17) within that carrier cycle. A better solution can be identified with modifications to the reference signals with suitable revisions to modulation logic. As a preliminary solution, an effective reference signal, $ref\ M$, for the two phases is introduced [15].

The new reference signal, considering sector 1 for instance, is the simple average of the two references as illustrated in Fig. 3.18(a) (for sector 1: $ref\ M = (ref_{B_d} + ref_{C_d})/2$). The required formulae to calculate the $ref\ M$ signal for each sector are tabulated in Table 3.5 and the variation of $ref\ M$ within the sectors is plotted in Fig. 3.18(b). Note that the new reference is still derived from the DPWM reference signals (not the original sinusoidal references); and therefore, in each sector, a certain phase is still tied to the power rail.

The logic scheme used for each phase is the same inverse carrier interleaved scheme introduced in the previous subsection. The only difference is the change of the reference signal: for both phases, there exists a common reference signal $ref\ M$. Therefore, the logic



(a) MDPWM1 with Ref M and Ref N: sector 1 (b) MDWPM1 with Ref M and Ref N: all sectors

FIGURE 3.18: Modified DPWM1 (MDPWM1): generation of the signals Ref M and Ref N

TABLE 3.5: Generating the Reference Signals $RefM$ and $RefN$

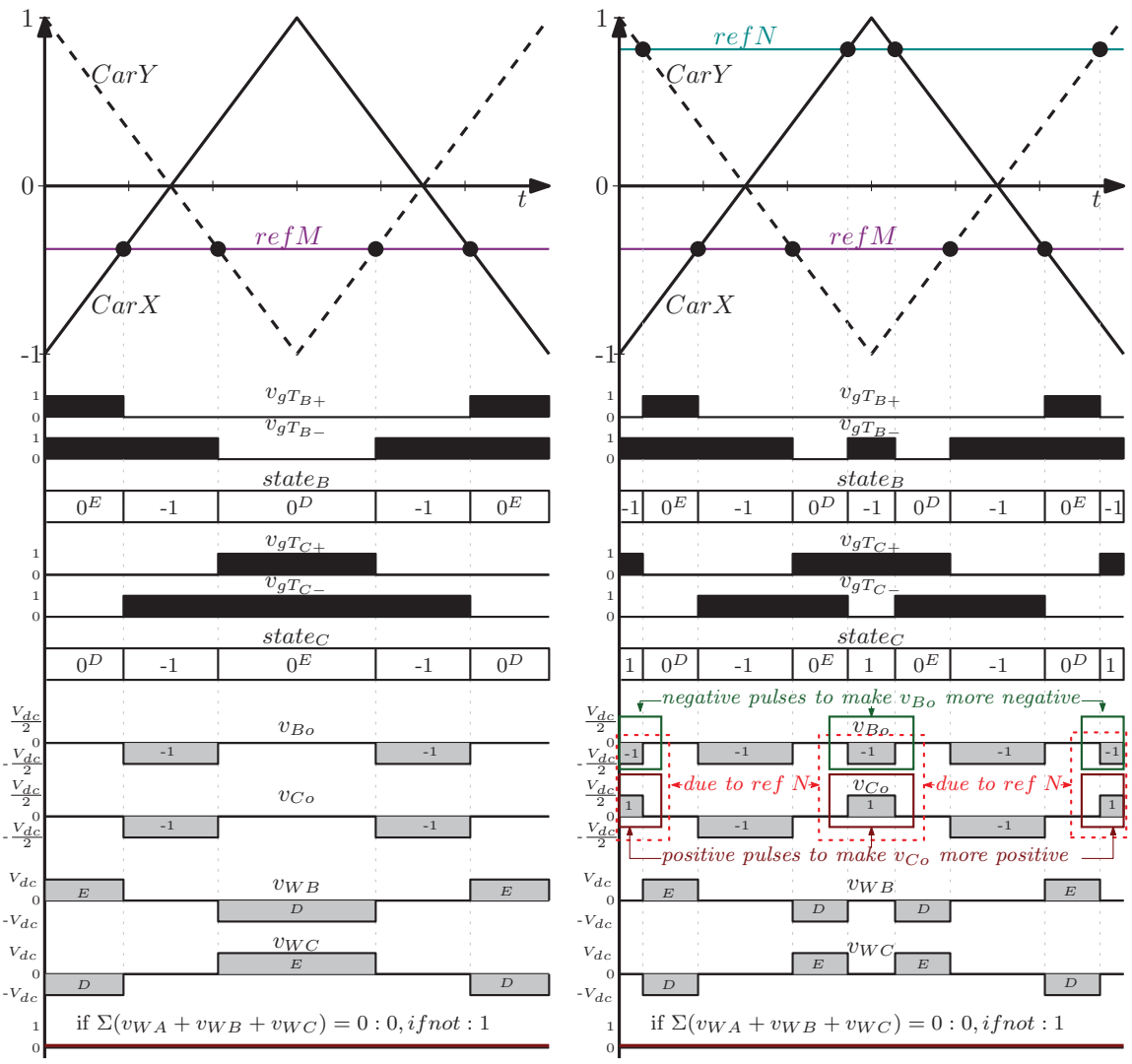
Sector	Tied Phase	***ref M***	***ref N***
0	B(-)	$\frac{a'+c'}{2}$	$1-\lvert\frac{a'-c'}{2}\rvert$
1	A(+)	$\frac{b'+c'}{2}$	$1-\lvert\frac{b'-c'}{2}\rvert$
2	C(-)	$\frac{a'+b'}{2}$	$1-\lvert\frac{a'-b'}{2}\rvert$
3	B(+)	$\frac{a'+c'}{2}$	$1-\lvert\frac{a'-c'}{2}\rvert$
4	A(-)	$\frac{b'+c'}{2}$	$1-\lvert\frac{b'-c'}{2}\rvert$
5	C(+)	$\frac{c'+b'}{2}$	$1-\lvert\frac{a'-b'}{2}\rvert$

Note: for simplicity a', b' and c' represents the standard DPWM reference signals such that: $a' = ref_{A_D}$, $b' = ref_{B_D}$ and $c' = ref_{C_D}$.

in the column "Inverse Interleaved (SDPWM2)" of Table 3.4 is used where ref_{B_d} and ref_{C_d} are now replaced with $ref\ M$. The effect of the new reference signals can be seen with the aid of familiar waveforms shown in Fig. 3.19(a) which describes sector 1.

Two important observations can be made with regard to this method:

1. The output voltage patterns v_{Bo} and v_{Co} of phase B and C are identical and do not reflect the average output voltage required for the carrier cycle in contrast to Fig. 3.17. In fact, this is expected as both phases have the same reference.



(a) Effect of Ref M: gate signals and corresponding voltage waveforms

(b) MDPWM1 with Ref M and Ref N: gate signals and corresponding voltage waveforms

FIGURE 3.19: MDPWM1: gate signals and corresponding voltage waveforms

2. Whenever the winding excitations occur, they occur simultaneously within the carrier cycle. And the requirement "$\sum v_{WB}+v_{WC}=0$" is satisfied for the total carrier cycle.

A complete solution, that satisfies both the winding excitation and average output voltage requirements, namely *Modified DPWM1* (MDPWM1), is derived by Salmon and Ewanchuk in [15] with the aid of some additional modifications to the existing scheme: an additional reference, $ref\ N$, and the already derived $ref\ M$ are used as reference signals

while a new logical scheme is derived for their comparison with the two carriers *car X* and *car Y*.

For sector 1, $ref\ N$ is half the value of the difference between the references ref_{B_d} and ref_{C_d} as illustrated in Fig. 3.18(a). The calculation of $ref\ N$ for each sector is tabulated in Table 3.5 and the corresponding logic scheme is tabulated in Table 3.4 with previously discussed schemes for better comparison. The logic scheme is quite complex compared to the schemes presented thus far; and therefore, it is easier to look at the resulting waveforms and then understand the underlying logic scheme which resulted in the waveforms. The corresponding waveforms of MDPWM1 scheme (for the time instant t^* in sector 1) are illustrated in Fig. 3.19(b).

The new scheme can be considered as a superimposition of the effects of $ref\ N$ on top of the effects of $ref\ M$. A simple inspection of the two side by side figures Fig. 3.19(a) and Fig. 3.19(b) clarifies this claim. In other words, what $ref\ N$ does is that it introduces some additional switching states changing the original duration of some switching states. This results in two changes:

1. Consider the output voltage pulses of the two phases: negative pulses are added to v_{Bo} while positive pulses are added to v_{Co}. This makes certain that now the original average output voltage values are followed by the phase outputs (equivalent to voltage patterns in Fig. 3.17 in an average sense).
2. Consider the winding voltage patterns. The duration of excited winding states is reduced (in contrast to the waveforms in Fig. 3.19(a)) due to the effect of $ref\ N$. However, the requirement "$\sum v_{WB} + v_{WC} = 0$" is still completely satisfied.

An important fact to realize here is that there still exist a minor problem with the derived solution when the complete sector is considered. Consider Fig. 3.18(b) which plots the variation of $ref\ M$ and $ref\ N$ for all sectors. It can be seen that both $ref\ M$ and $ref\ N$ are symmetric waveforms around sector mid-point for each sector. This is clearly illustrated in Fig. 3.18(a), which specifically zooms in to sector 1. Consider the first half of sector 1 where time instant t^* resides. The added negative pulses make v_{Bo} more negative and make it follow the average voltage demanded by ref_{B_d} rather than $ref\ M$: which is the desired case as ref_{B_d} is more negative compared to $ref\ M$ during the first 30° of sector 1 (portion N_u). Similarly, added positive pulses make v_{Co} more positive and make it follow the average voltage demanded by ref_{C_d} (rather than $ref\ M$) for portion N_u.

TABLE 3.6: Change of Logic Patterns for Sectors 1 and 4

Switch	Logic Pattern for Each Sector			
	Sector 1		Sector 4	
	First $30° = N_u$ $[b' - c' = (-)]$	Second $30° = N_d$ $[b' - c' = (+)]$	First $30° = N_u$ $[b' - c' = (+)]$	Second $30° = N_d$ $[b' - c' = (-)]$
T_{B+}	$\boldsymbol{\alpha}$	$\boldsymbol{\gamma}$	$\boldsymbol{\gamma}$	$\boldsymbol{\alpha}$
T_{B-}	$\boldsymbol{\beta}$	$\boldsymbol{\delta}$	$\boldsymbol{\delta}$	$\boldsymbol{\beta}$
T_{C+}	$\boldsymbol{\gamma}$	$\boldsymbol{\alpha}$	$\boldsymbol{\alpha}$	$\boldsymbol{\gamma}$
T_{C-}	$\boldsymbol{\delta}$	$\boldsymbol{\beta}$	$\boldsymbol{\beta}$	$\boldsymbol{\delta}$

However, if the same logic scheme is followed for the second 30° of sector 1 (portion N_d) a problem arises. Since $ref\ M$ and $ref\ N$ are symmetric around the sector the mid-point, the individual average voltage requirements of the two phases are not satisfied for this portion of the sector: v_{Bo} is still accompanied with added negative pulses which make it more negative though it should be made more positive (as ref_{B_d} is more positive compared to $ref\ M$ in the time portion N_d). Similarly, v_{Co} is still accompanied with added positive pulses which make it more positive when it should be made more negative (as ref_{C_d} is more negative compared to $ref\ M$ in the time portion N_d). This suggests that the switching logics for the two phases has to be swapped after the sector mid-point for each sector. This distinction is clearly presented in Table 3.4: note the change of logics α, β, γ and δ when moving from first 30° (N_u) to second 30° (N_d) during a sector.

A simple method to decide the current position within a sector (i.e. to determine whether in N_u or N_d) is to consider the difference between the two original DPWM references. For example, consider sector 1: if $ref_{B_d} - ref_{C_d} < 0$, then the current portion is N_u; and if $ref_{B_d} - ref_{C_d} > 0$, then the current portion is N_d. This is useful when deriving logic for sector pairs which have a common tied-phase. For instance, sector 1 and sector 4 are a sector pair whose common tied-phase is phase A. Since ref_{B_d} is larger compared to ref_{C_d} in the first 30° of sector 4 (which is not the case for sector 1), the correct logic scheme for time portion N_u of sector 4 is the one that corresponds to "$ref_{B_d} - ref_{C_d} > 0$" condition. The complete logic patterns for sectors 1 and 4 are tabulated in Table 3.6 for a clear comprehension of this matter for the reader, especially if one is interested in simulating such a system.

It could be concluded that, with adherence to required logic patterns for each sector

(also considering the time portion within the sector), MDPWM1 scheme is capable of satisfying both the average output voltage and winding excitation requirements for the complete carrier cycle.

3.4 Review of PWM Schemes for the 3-Limb Core 6-CII Topology

Parallel inverters are a well established solution for increasing current and power capabilities of inverter systems. With the introduction of interleaved switching, they have become quite formidable among 3-level inverter solutions. Furthermore, the notion of coupling the inductors, instead of regular non-coupled output ac reactors, produced more benefits: 1) reduction of system losses due to the lowered high frequency content and, 2) reduction of the fundamental voltage dropped across output reactors. A six switch solution, 6-CII, for the parallel inverter topology provides same performances as the standard twelve switch topology with added benefits (ex: half the number of switches and gate driver units). As a three-phase coupled inductor unit, the 3-limb core approach offers significant size benefits over three separate sets of coupled inductor units due to several reasons.

With the aid of better modulation techniques, the 3-limb magnetic core energization can be enhanced to minimize inductor winding losses, that further reduces inverter losses. Standard DPWM with interleaved switching (SDPWM1) is the starting point of developing a more potent scheme where the effect of all the three phases could be considered in an effective manner. With proper modifications to original DPWM reference signals and carrier-reference comparison logic, a better modulation scheme is introduced: *MDPWM1*.

An important fact to realize here is that the modulation technique derived so far is a conceptual one. However, implementing a such a scheme, with its quite complex logic accompanied with two carrier signals, is not as that straightforward as it seems. The practical implementation of the scheme in control units such as DSPs and FPGAs introduces additional design constraints.

Chapter 4

Pre-Processed PWM Approach for a Single-Carrier DSP Control Unit

Controllers for Power Electronics have moved to the digital domain with the rapid development of digital electronics. It may seem, at first, that the most important characteristic of these units is the processing power as it allows tighter control loops. However, such a supposition is not a well comprehended engineering principle. What is important, on a broader engineering perspective, is achieving an acceptable processing power with the minimization of the following important criteria: system cost, electric power consumption, effective program memory and RAM, unit's physical size, and software and hardware development effort.

The practical nature of the MDPWM1 scheme is discussed in order to identify the requirements of a potential solution. The conceptual scheme is converted to a more pragmatic scheme, *MDPWM2* (with WEF); that requires only a single carrier, and slight modifications to modulation logic to support a DSP environment. It is shown how the low-cost DSP based PWM control unit can be utilized to handle the developed scheme with the aid of two independent control loops, presenting the main material of this work. An extra feature, the flipping of the winding excitations (WEF) at carrier cycle's mid-point [16], is also incorporated to the proposed scheme (with added modifications to be suitable for a DSP environment), to further enhance the 3-limb magnetic core performance.

4.1 The Control Approach

With the advent of digital electronics, quite a number of different processor technologies can be identified in the technical literature. The most elementary digital control unit is a *Microprocessor* (μP) whose functioning simply relies on the execution of commands in a sequential manner [38]. This consists of two main units: 1) Control Unit, and 2) Central Processing Unit (CPU). Note that, external devices are required to communicate with the μP to provide inputs and obtain required outputs. When such external devices are incorporated to a μP, the resulting unit is called a *Micro Computer System*. Program code memory, data memory, digital/analogue input pins and digital/analogue output pins are examples of such external units.

When a micro computer system is built in to a single chip (with pins for inputs and outputs), a *Micro-controller* (μC) is obtained.[1] The processing power of μPs are somewhat limited, especially when the need arise to perform complex mathematical functions such as digital filters, phase-locked loops (PLL), etc. When additional hardware units capable of such processing is equipped to a μP, a *Digital Signal Processor* (DSP) is built. However, a *Digital Signal Controller* (DSC) is considered more appropriate to perform the tasks required for the application being considered. In simple words, a DSC is an advanced μC where the processing unit is a DSP instead of a μP. In technical literature, the term "DSC" is interchangeably used with "DSP" as both of signify the processing power of the latter.[2]

The MDPWM1 scheme is a formidable modulation scheme (as Chapter 3 describes) for the 3-limb core based 6-CII topology. However, that is only a conceptual solution; and therefore, does not reflect the requirements that the scheme demands from a control unit when it comes to the practical realization of it. It is shown that MDPWM1 requires complex and extensive processing, while the proposed scheme, MDPWM2, achieves the same tasks with much simpler requirements.

4.1.1 Requirements of the Control Unit to Realize MDPWM1 Scheme

In standard sinusoidal carrier based PWM schemes, the modulation logic is quite simple: if the reference is greater than the carrier signal, logic 1 is fed to the power switch (logic

[1] TI's *MSP430* is one of the most used μCs.

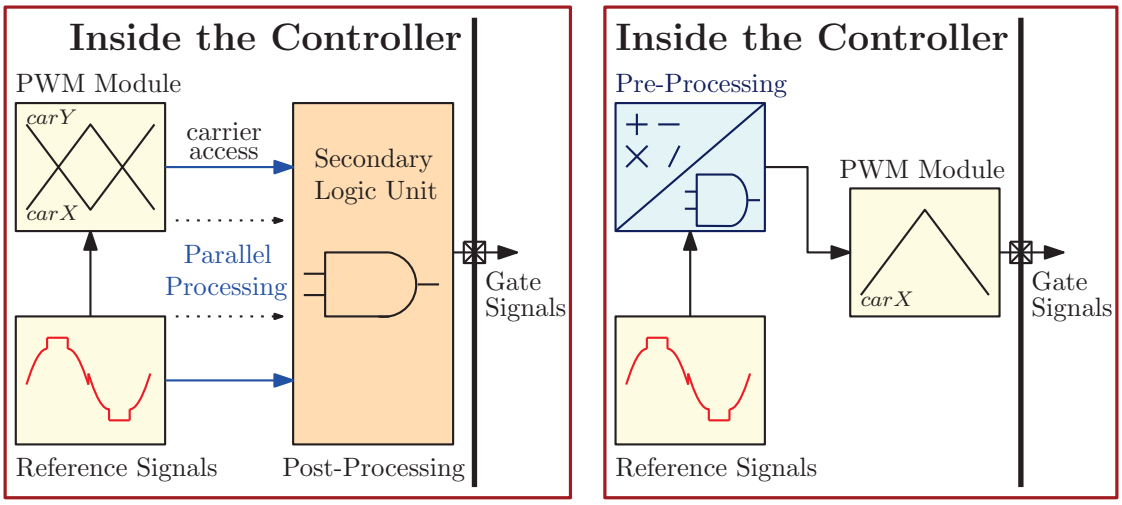
[2] For the remainder of the report, the term DSP is used.

0 is fed otherwise). However, a glimpse of Table 3.4 shows that the modulation logic is not that simple for MDPWM1 scheme. The following characteristics can be identified as the major distinctions of the MDPWM1 scheme in contrast to standard sinusoidal carrier based PWM schemes.

1. The scheme requires two carrier signals which are phase shifted by 180°.
2. There are two reference signals, $ref\ M$ and $ref\ N$, that are derived from DPWM1 reference signals for each carrier cycle.
3. Most importantly, the modulation logic for each switch (α, β, γ and δ) is derived by two comparison logics that are then fed into a logical gate: either AND or OR. For example, consider logic α: $ref\ M$ is compared with $car\ X$ and $ref\ N$ is compared with $car\ Y$; and then, the two results are fed into a logical AND gate to derive the gate signals for T_{B+} in N_u portion of sector 1.
4. *Turn-ON* and *Turn-OFF* logics for each switch (for instance, T_{B+}, T_{B-}, T_{C+} and T_{C-} for sector 1) are different from each other, and therefore, require additional logical comparisons to determine the final gate signal logic.
5. *Turn-ON* and *Turn-OFF* logics for each switch alter at every half cycle point of the fundamental cycle (note the portions N_u and N_d in Table 3.4).

Let us look at the requirement 3 in the above list more closely . There, two reference signals are to be compared with two carrier signals. Then, the results are fed to a secondary logic gate [17, 25]. However, this is not a function generally available in simple processors: it requires internal access to the logic outputs of the PWM module if the comparison results are to be fed into another internal secondary logic unit. Another important aspect to be understood here is that the two comparisons have to be implemented in a parallel manner– not in a sequential manner. This is because the two results should not have any time delays between them before they are fed into the secondary logic gate. With these realizations, three important conclusions can be made about the control unit processor requirements for MDPWM1 scheme:

1. Each PWM module of the control unit should be equipped with two carrier signals.
2. The control unit processor should support parallel processing.
3. The control unit should provide internal access to its carrier-reference compare results: the *Post-Processing* of carrier-compared signals.



(a) Post+Parallel Processed PWM (b) Proposed Pre-Processed PWM

FIGURE 4.1: Modulation control strategies

These requirements are pictured in Fig. 4.1(a). The industry solution for parallel processing is usually high-end processor technologies such as FPGA systems [39]. For instance, the works presented in [17, 40] on MDPWM1 use the *LabVIEW* based FPGA system *NI 7851R*.

The main objective of this thesis work was to devise an alternate modulation strategy that would simplify the above processor requirements: that allows use of a much simpler controller processor without any modification to the output gate signals.[3] A DSP based control unit is chosen as the target solution mainly due to its simplicity, low cost and size, and low power consumption. A comparison of controller unit technologies is presented in Table 4.1 to further justify the selection of the DSP technology.

TABLE 4.1: Comparison of Control Unit Processors: Power Electronics Applications [2]*

Technology	Time to Market	Performance	Price	Development Ease	Power	Feature Flexibility	Overall
MCU(μC)	Excellent	Fair	Excellent	Good	Fair	Excellent	Good
DSP	Excellent	Excellent	Good	Excellent	Excellent	Excellent	Excellent
FPGA	Good	Excellent	Poor	Excellent	Poor	Good	Fair

*The data is directly extracted from the reference [2].

[3] In fact, it is shown later that the proposed scheme (MDPWM2) changes the output gate signal pattern to accommodate winding excitation flipping [16] that further increases magnetic core performance.

However, with the selection of a DSP, the support to parallel processing and post-processing (access to carrier signals inside the chip) is compromised as opposed to the high-end FPGA solution. Therefore, a new modulation strategy has to be formulated where such requirements are not involved. Such a modulation scheme, $MDPWM2$, is proposed as a novel solution for a DSP based controller environment.

4.2 The TI TMS320F28335 DSP Environment

Acquiring proper knowledge on the selected DSP environment, its general capabilities and limitations as power electronic control units is an important design step. Furthermore, this helps to gain a better perspective on the basic requirements of the new scheme and to tailor its characteristics to be realizable.

Digital signal processors usually operate within the range 1 MHz up to several hundred megahertz [41]. Generally, this provides small enough time steps for power electronic control loops for all practical purposes as long as parallel processing is not a requirement. For this particular work, a ***Delfino TMS320F28335*** DSP by *Texas Instruments* (TI) is used [42]. This is one of the mostly used DSPs in inverter and motor drive control applications and belongs to the *TI C2000* family of DSPs [43].

The DSP has a maximum clock frequency $f_{sys} = 150\ MHz$: i.e. instruction cycle time $T_{sys} = 6.67\ ns$. As with other modern DSPs and μCs, TMS320F28335 is equipped with a *PWM Module* which is run using its own clock, $TBCLK$. The term "*Module*" signifies the fact that the PWM functions are carried independent of the main program code: the module behaves as a separate hardware unit. The selected DSP has six of such PWM modules where each module has its own carrier signal. Each module has two PWM outputs, $ePWMxA$ and $ePWMxB$, where x is an integer from 1 to 6 representing each of the six modules. These two outputs are usually used in a complementary manner for a standard inverter leg. It can be concluded that, therefore, the DSP supports the operation of six separate inverter legs: making it suitable for both 6-CII and 12-CII topologies.

Consider a single PWM module, for example $ePWM1$ module. The module is incorporated with a carrier devised by a high resolution counter register, $TBCTR$, where the carrier period T_c is set in the 16-bit register $TBPRD$ ($0 < TBPRD < 2^{16} - 1 = 65535$). At

each system clock pulse, the counter $TBCTR$ is incremented by 1 till it reaches the value in $TBPRD$ register (where time duration of a single counter step is determined by $TBCLK$). Then, $TBCTR$ is decremented by 1 till it reaches zero. This up-down counter mode results in a triangular shaped carrier wave varying between 0 and $TBPRD$ as illustrated in Fig. 4.2.

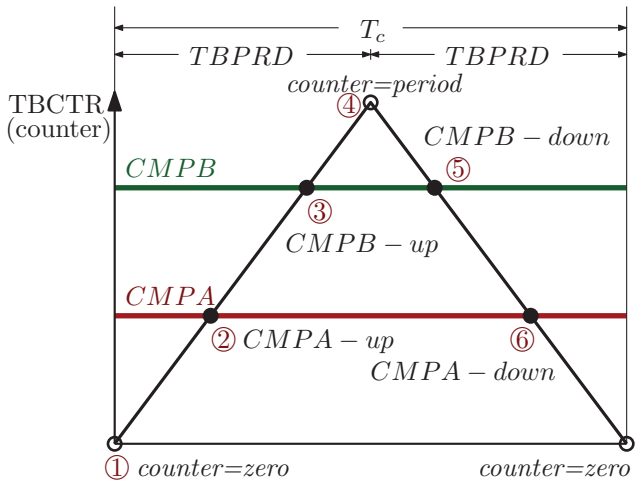


FIGURE 4.2: F28335 DSP PWM Compare Unit events: 6 events within a carrier cycle

Each module supports two reference signal comparisons: the values written two compare registers $CMPA$ and $CMPB$ corresponds to the two reference values in the particular carrier cycle. Four possible compare events are generated when the value of the up-down counter matches the compare register values: $CMPA - up$, $CMPB - up$, $CMPA - down$ and $CMPB - down$. When the counter register equals 0 or $TBPRD$, two further events are generated. All the six events are depicted in Fig. 4.2.

Note that, the PWM module can be configured such that, at each event, it triggers an action on the both PWM output lines, A and B: to drive the output either Low or $High$. The required action for each event is set by configuring the *Action Qualifier* registers $AQCTLA$ and $AQCTLB$ for each module. Also, during each of these events, the PWM module generates interrupt signals so that module configuration can be changed at each event if necessary. It is shown later how the "$counter = period$" event's interrupt allows performing a winding excitation flipping at the carrier cycle mid-point.

With reference to Fig. 4.2, following relationship between $TBPRD$ value and the carrier period T_c (in seconds) can be identified:

$$T_c = (2 \times TBPRD) \times TBCLK \ \ seconds \tag{4.1}$$

For this work, $TBCLK$ is configured such that it is equal to the DSP original clock period $T_{sys}(= 1/(150 \times 10^6)\ s)$. And, therefore,

$$TBPRD = \frac{T_c}{2 \times T_{sys}} = \frac{f_{sys}}{2 \times f_c} \tag{4.2}$$

For instance, for a carrier frequency of 5 kHz, the TBPRD value is calculated as:

$$TBPRD = \frac{f_{sys}}{2 \times f_c} = \frac{150 \times 10^6}{2 \times 5 \times 10^3} = 15000$$

4.3 The Proposed PWM Scheme: MDPWM2

In generic DSP environments, there exist only one carrier signal for a particular PWM module and there is no explicit support for parallel processing. Therefore, the proposed scheme is devised with following distinctions:

- Uses only one carrier signal in contrast to two carrier signals used in MDPWM1.
- Introduces four reference signals which effectively work as two reference signals as a complete carrier cycle is completed. With setting different actions for PWM outputs on each PWM compare event, and with the aid of four reference signals, a Pre-Processing scheme is devised to inhibit the need for parallel processing.

The proposed scheme relies on two additional reference signals, $refM'$ and $refN'$:

$$ref\ M' = -ref\ M \qquad and \qquad ref\ N' = -ref\ N \tag{4.3}$$

These additional signals make it possible to develop a single carrier system as illustrated in Fig. 4.3 (for the time instant t^* in sector 1). $refM'$ and $refN'$ alongside with $car\ X$ compensate for the lost carrier-reference match points due to the removal of carrier signal $car\ Y$ from the MDPWM1 scheme. A comparison of Fig. 3.19(b) and Fig. 4.3 shows that MDPWM2 generates exactly the same carrier-reference match points as MDPWM1.

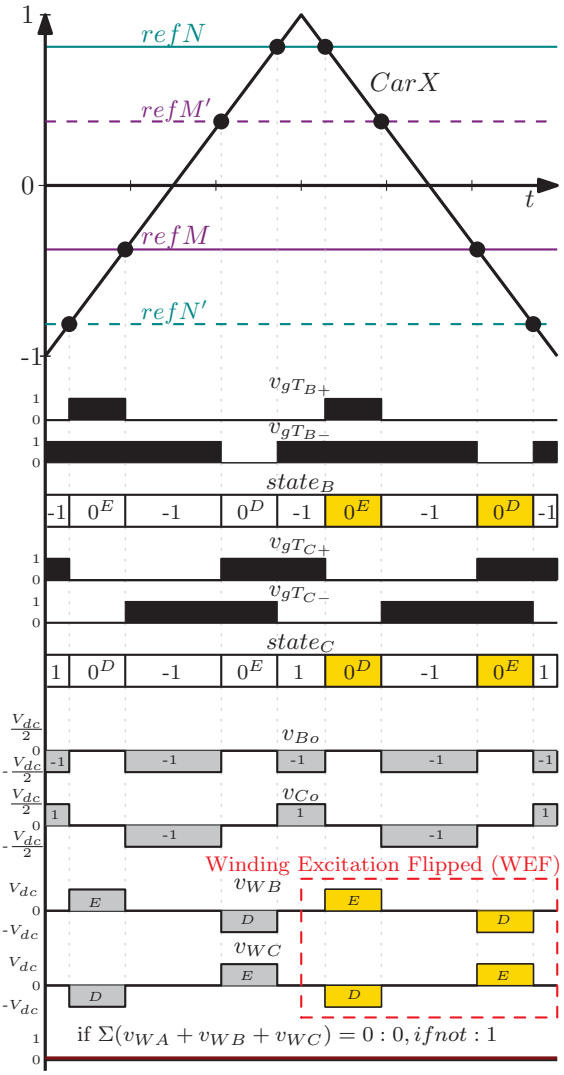
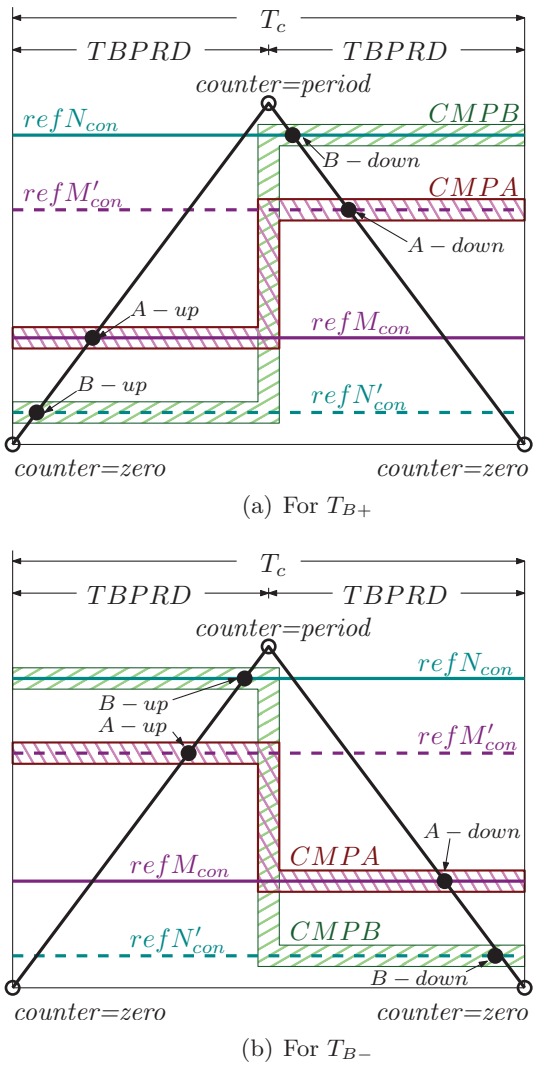


FIGURE 4.3: Proposed scheme with Winding Excitation Flipping, Modified DPWM2 (MDPWM2), with four reference signals: gate signals and corresponding voltage waveforms



*note: subscript *con* refers to level shifted values of the references for a carrier between 0 and +1

FIGURE 4.4: Pre-processing of references: variation of CMPA and CMPB for phase B

One additional distinction can be observed in the second half of the carrier cycle with the highlighted winding states. In contrast to MDPWM1, here the winding excitation is flipped in the second half of the carrier cycle still maintaining the "$\sum v_{WB} + v_{WC} = 0$" requirement with undisturbed output voltage patterns. The continuous alteration of the winding excitation of each phase, between positive and negative rails, further lowers the high frequency winding current ripple in contrast to the non-flipped case [16].

However, there is a catch: the DSP PWM comparator supports comparison of only two reference signals (with the aid of $CMPA$ and $CMPB$ registers) although it is required to incorporate four reference signals according to Fig. 4.3. But, a careful examination of switching transitions in the figure shows, that for a particular switch, only two references are required for a particular half of the carrier cycle. For instance, consider the switch T_{B+}: for the first half of the carrier cycle, it requires $ref\ M$ and $ref\ N'$; and for the second half, it requires $ref\ M'$ and $ref\ N$. Therefore, if the reference signals are changed accordingly at the mid-point of the carrier period, it is possible to effectively compare four reference signals in a full carrier cycle. This is where the advantage of the DSP event interrupts comes into the picture. The "*counter* = *period*" event occurs at the mid-point of the carrier period; and therefore, during its interrupt service routine, the reference signals fed to the $CMPA$ and $CMPB$ registers are changed accordingly.[4] How this alteration is performed inside the DSP is graphically presented in Fig. 4.4(a) and Fig. 4.4(b) for phase-B switches for the time instant t^*. Here, the subscript "*con*" in the reference signals refers to the level shifted and scaled values of the original four reference signals for a carrier between 0 and $TBPRD$.

The switch actions for phase B and C switches and corresponding reference signals for the two halves of the carrier period is comprehensively tabulated in Table 4.2. Note that, the overall logic patterns have to be changed accordingly at the second half of the fundamental cycle as explained in Section 3.3.2 and Table 3.6 in the previous Chapter 3.[5] Furthermore, Table 4.3 summarizes this fact with reference to both schemes (MDPWM1 and MDPWM2) and the corresponding switching state arrangements within a carrier cycle.

TABLE 4.2: Switching Logic for the DSP Based Modulation of MDPWM2: Phase B and C Switches During a Single Carrier Cycle in Sector 1 (for First 30° of Fundamental Cycle)

Carrier State: Cycle Position	Event	T_{B+}		T_{B-}		T_{C+}		T_{C-}	
		Ref.	Action	Ref.	Action	Ref.	Action	Ref.	Action
First half	$CMPA-up$	M	OFF	M'	OFF	M'	ON	M	ON
	$CMPB-up$	N'	ON	N	ON	N'	OFF	N	OFF
Second half	$CMPA-down$	M'	OFF	M	OFF	M	OFF	M'	ON
	$CMPB-down$	N	ON	N'	ON	N	ON	N'	OFF

Note: "Ref." is the required reference signal during a particular carrier position for each switch.

[4] The $CMPA$ and $CMPB$ registers are updated during both "*counter* = *period*" and "*counter* = *zero*" events. However, in the former, the values are only negated while the magnitudes of the original references remain unchanged. The magnitudes are updated only after a complete carrier cycle.

[5] The first and second halves of the fundamental cycle (N_u and N_d) represent a different aspect and this has nothing to do with the first and second halves of the carrier cycle.

TABLE 4.3: Temporal Arrangement of Switching States Used within a Carrier Cycle in Sector 1: for Both MDPWM1 and MDPWM2 Schemes

Scheme	Fund. Cycle Position	States within the Carrier Cycle								
MDPWM1	First 30°	1,-1,1	1,0^E,0^D	1,-1,-1	1,0^D,0^E	1,-1,1	1,0^D,0^E	1,-1,-1	1,0^E,0^D	1,-1,1
	Second 30°	1,1,-1	1,0^D,0^E	1,-1,-1	1,0^E,0^D	1,1,-1	1,0^E,0^D	1,-1,-1	1,0^D,0^E	1,1,-1
MDPWM2	First 30°	1,-1,1	1,0^E,0^D	1,-1,-1	1,0^D,0^E	1,-1,1	1,0^E,0^D	1,-1,-1	1,0^D,0^E	1,-1,1
	Second 30°	1,1,-1	1,0^D,0^E	1,-1,-1	1,0^E,0^D	1,1,-1	1,0^D,0^E	1,-1,-1	1,0^E,0^D	1,1,-1

Note: the switching states within the carrier cycle are derived for the time instant t^* introduced in Fig. 3.15. For the second half of the fundamental cycle, an equivalent time instant is considered.

The difference between the two schemes, as far as the winding excitation is considered, is the change in the second half of the carrier cycle as the highlighted cells in the table show.

4.4 DSP Control Loops

The proposed scheme is realized using two independent control loops inside the DSP. The two loops are triggered by two independent interrupts generated inside the DSP: 1) *Timer0* interrupt and, 2) *EPWM1* interrupt. Note that, while the program code in the interrupt routines are run, the PWM modules still run without any interruption: i.e. the PWM modules' timer counters are not halted during these interrupt routines.

1) Control Loop 1: this is used to generate the original three-phase sinusoidal signals (ref_A, ref_B and ref_C) and is powered by the *Timer0* interrupt routine of the DSP. The module is set to run at a frequency f_{ref} ($= 1/T_{ref}$) determined by the required fundamental frequency, f_1. A counter C_t (counter time step $= \delta t_c$ seconds) is incremented at each interrupt . At each time step, a sine function is calculated: for example, consider ref_A;

$$ref_A = sin\big(\frac{2\pi}{R \times \delta t_c} \times C_t \times \delta t_c\big) \qquad where\ R\ is\ the\ sine\ wave\ resolution \tag{4.4}$$

$$T_{ref} = R \times \delta t_c = R \times \frac{TIMER0PRD}{f_{sys}}\ \ seconds \tag{4.5}$$

The generated ref_A is shown in Fig. 4.5 for a complete fundamental cycle, where R is chosen as 1800. Therefore, a sector is synthesized using 300 points. According to Eq. (4.5), for a fundamental of 60 Hz, the *Timer0* period register $TIMER0PRD$ has to be set to 1389, if $R = 1800$ (to 13889, if $R = 180$). The important fact to remember here is that the

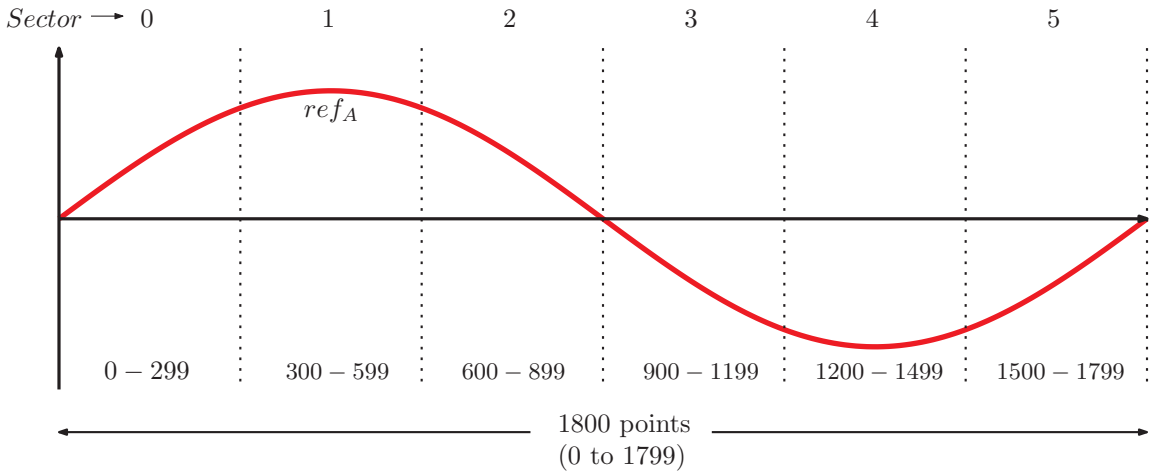


FIGURE 4.5: Sector and original sinusoid generation inside the DSP

frequency of the reference signal solely depends upon the update frequency of C_t and that its resolution depends upon the value of R.

2) Control Loop 2: this is executed each time a "*counter=zero*" or "*counter=period*" interrupt occurs in PWM module 1. Note that, PWM module 1 is selected as the central synchronizing module for all the six modules. During each interrupt routing, due to "*counter=zero*" event, the values of the four reference signals, $ref\ M$, $ref\ N$, $ref\ M'$ and $ref\ N'$, are calculated for the current iteration of the carrier cycle. The new values (the two required references out of the four, depending upon the particular half cycle of the carrier) are written instantaneously to *CMPA* and *CMPB* registers of each module for comparison. Note that, at the "*counter=period*" interrupt, an auxiliary subroutine is run to change the values fed to *CMPA* and *CMPB* registers as for the requirements discussed in Section 4.3. It should be emphasized that reference values are not calculated again at this interrupt as they are already calculated at the "*counter=zero*" event's interrupt routine for the whole carrier cycle.

In conclusion, the grounds are established for practically implementing the proposed MDPWM2 scheme on a DSP environment; in this work, on a TI TMS320F28335 DSP.

Chapter 5

Experimental Apparatus: SiC-MOSFET based Versatile Inverter Leg System

As the electric signals are transmitted with the speed of light, for signal frequencies up to several gigahertz, we can assume that there is no significant delay in the transmission of the signals as long as the circuit size is kept within several centimetres. However, the signal frequencies are getting increased day by day (especially in the domain of digital circuits), and therefore, the corresponding signal wavelengths go down asking for further reduction of the circuit size. Eventually, a physical limit will be reached where we can not further reduce the circuit size, and hence, the ultimate higher limit for clock frequencies will be reached for processors. But that is a problem for engineers in a futuristic world.

The hardware development of the inverter system and the control unit is described in detail. The circuit boards were designed using *EAGLE PCB Design Software* version 4.16 computer package [44]. The schematic and layout design files of the developed hardware unit are provided in Appendix D. For sake of the brevity of the report, a detailed explanation of the design steps of both control and power electronic level circuits is not presented here. However, the important design concerns and their solutions that need clear attention are addressed: with the design files in Appendix D alongside with material presented in this chapter, the readers interested in circuit design are exposed to some interesting design facts.

5.1 The Overall Design Approach

THE development of an efficient and low cost hardware setup is essential in both laboratory and final levels of production. Even within the current technological state, there are difficulties in circuit design within applicable frequency ranges, such as: Electro-Magnetic Interference (EMI), increased line inductance due to high frequency operation and increased capacitive coupling. Therefore, the layout design of electronic circuits, especially in power electronics, is a task that requires a high level of attention.

The experimental hardware system is developed as a universal test platform for DSP based PWM concepts. The system consists of the following units.

- Main Control Board: acts as the central hardware unit and provides interfacing between the peripheral units and the DSP.
- MOSFET based *Versatile Inverter Legs*: the system supports up to six individual inverter legs that can be connected according to user preference. For instance, two three-phase inverters or three H-bridge units.
- Analogue Sensor Boards: each board supports three analogue inputs between -40 *to* $+40$ voltage swings with configurable attenuations. Four such boards can be incorporated to a single control board as the DSP supports sixteen analogue channels [42].

An overall block diagram of the system is shown in Fig. 5.1. The DSP itself comes as a module called *TMS320F28335 controlCARD* which is plugged into the main board [45]. The controlCARD is a board-level module and provides easy communication to the DSP.

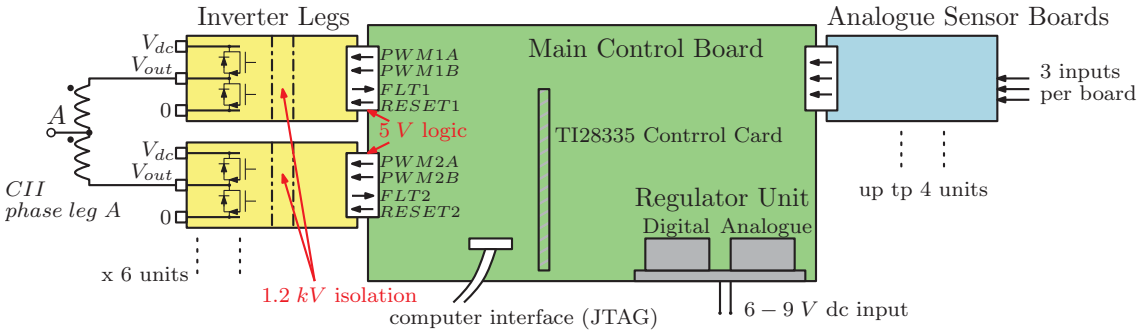


FIGURE 5.1: Overall hardware unit: main control board, analogue sensor boards, inverter legs and the CII connection

5.2 Design of the Main Control Board

The Main Control Board unit is tailored to be compatible with the TMS320F28335 DSP controlCARD. A $6-9\ V$ dc voltage supply powers the board and a dc current around 200 mA is consumed when no peripheral units are connected. The input dc voltage is fed to two sets of 5 V and 3 V regulators: where one set provides regulated 5 V and 3 V power to analogue units of the DSP while the other set provides the same to digital units. Separation of analogue and digital power lines (also with separate ground planes) on the control board is an important design practice as it allows cleaner measurement of analogue signals [46].

Access to all six PWM modules is supported with pin headers consisting of the following logic lines: two PWM lines ($PWMA$ and $PWMB$), a fault line (FLT) connected to DSP trip-zones (TZ) and a reset line (RST) (see Fig. 5.1). This is a control level circuit, and therefore, all the above logic signals are $0-5\ V$ signals.

The board is designed to access all the sixteen analogue channels of the DSP for measurements such as dc-link voltages, grid voltages and line currents. Voltages up to 1000 V and currents up to 100 A are expected to be measured using external isolation voltage and current probes (whose outputs are usually voltages between -10 and $+10$ volts). The purpose of the designed peripheral analogue sensor board is to further attenuate these signals and provide dc offsets. This is required due to the nature of the DSP Analogue to Digital Converter (ADC) module: it only accepts voltages between 0 and 3 volts. Note that, the design of the analogue units is to serve the purpose of the universal test platform and to facilitate the system's capacity for analogue measurements for future testing. For experimental testing of the MDPWM2 scheme, the operation of this peripheral unit is not required. Note that, all the design schematics of the main control board and the analogue sensor boards are presented in Appendix D.

5.3 Design of the Inverter Leg

One of the goals of this work, from a hardware perspective, is to develop an inverter leg with following characteristics: compact in size, robust protection features, better EMI performance, low losses and low cost.

A block digram view of the designed inverter leg is shown in Fig. 5.2. There are six units of these legs attached to a main control board (see Fig. 5.1). The schematic and layout design files of the developed inverter leg are provided in Appendix D.

The versatility[1] of this design allows the system to be easily adapted to feature different topologies:

1. Each leg used as a half-bridge: combine three legs with a common dc-link and other three with another separate dc-link to form a back-to-back inverter system.
2. Two legs combined to form an H-bridge: this results in three H-bridge units that can act as a floating three-phase H-bridge system.
3. Combine two legs to form a phase leg of the 12-CII topology: by combining remaining four legs in a similar manner for other phases, a three-phase 12-CII topology is derived.
4. Each leg used as an asymmetrical bridge: here, only one MOSFET is switched in the leg while the other is always kept in the OFF state. The latter one's body diode acts as the diode of the asymmetrical bridge.

Some clarification should be offered on the last two items in the above list. Consider the connection of two inverter legs as a CII phase leg as shown in Fig. 5.1. If all four switches in the two inverter legs are switched, then the result is a phase leg of a 12-CII topology (see Fig. 3.6(a)). On the other hand, if only the top switch in leg 1 (bottom switch not

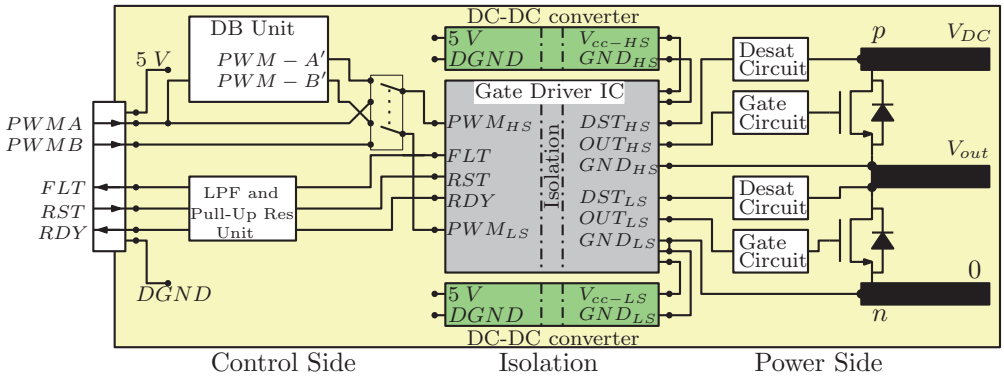


FIGURE 5.2: The design of MOSFET inverter leg: a macro view

[1]The idea is to use the design for future projects: this is cost effective when compared to buying inverter modules directly from the market. Moreover, the versatility of the design allows testing of many topological concepts and modulation techniques which is not easy to achieve with pre-designed modules.

switched) and the bottom switch in leg 2 (top switch not switched) are switched, then the result is a phase leg of a 6-CII topology (see Fig. 3.6(c)). The latter method is how the system is configured for this work to test the 6-CII topology with MDPWM2 scheme.

On the *Control Side* of the design (i.e. the 5V logic side), a dead-band unit is integrated to generate on-board dead times for complementary configurations of PWM inputs. There is also a low-pass filter (LPF) unit for signal conditioning of control signals and a pull-up resistor unit (as these signals are usually *active-low*).[2] The control side and the *Power Side* are interfaced using a gate driver chip with galvanic isolation. The 15 V dc power required for the gate circuitry on the power side is derived from 5 V-to-15 V isolated dc-dc converters whose input power is drawn from 5 V power line on the control side.[3]

On the power side of the design, three main units can be observed according to Fig. 5.2: 1) two MOSFETs with the dc-link, 2) gate circuitry for each MOSFET, and 3) *Desaturation Protection* for each MOSFET. The details of the selection of the MOSFET and the gate driver chip, and the design of the gate driver circuitry and protection circuitry are discussed in the subsequent sections of this chapter. The complete list of components used in the design of the inverter leg is tabulated in the bill of materials table (Table D.1) in Appendix D.

5.3.1 Selection of the MOSFET

IGBTs and MOSFETs are the commonly used power semiconductor devices for inverter leg designs in current era of power electronic technologies. IGBTs are commonly used in medium to high voltage applications due to their higher voltage and current ratings. However, for low to medium voltage applications, MOSFETs are quite advantageous due to their higher switching speeds (allowing lower filter sizes) and lower conduction losses (due to their very low on-state resistances). Also, with the low *turn-on* and *turn-off* times of modern MOSFETs, the increase of switching losses due to high frequency operation is quite low. Moreover, the same gate driver circuitry that is used for an IGBT system can

[2] For instance, if there are no faults in the system, the *FLT* line is kept at logic HIGH (no action). But, if there is a fault, then the *FLT* line is drawn to logic LOW (the line is active).

[3] A boot-strap circuit on the power side could be used with a single dc-dc converter setup rather than having two dc-dc converters. However, the latter method is considered a better solution as the boot-strap method introduces additional design limitations [47, 48]. Furthermore, having separate dc supplies provide much flexibility when the two switches are to be switched independently.

be directly used for a MOSFET system (maybe with a slight change to the gate resistance value).

For example, consider a 200 $V/10$ A system. For an IGBT, the on-state loss can be calculated as: $P_{loss-on} = V_{CE-sat} \times I_{on} = 1.2\ V \times 10A = 12W$, where V_{CE-sat} is the on-state voltage across an IGBT and is usually around 1.1 $V - 1.5$ V for medium voltage applications. But, for a MOSFET, the on-state loss is: $P_{loss-on} = R_{DS-on} \times I_{on}^2 = 0.08\ \Omega \times 100A = 8W$, where R_{DS-on} is the static on-state resistance of the MOSFET which is usually below 100 $m\Omega$ for voltage levels below 500 V for Silicon MOSFETs.

A list of tested MOSFET devices from different manufacturers is tabulated in Table 5.1. The first four devices in the list are surface mount devices where Silicon is the semiconductor material. The devices A and C have a very large *Reverse Recovery Charge* (Q_{rr}) and *Reverse Recovery Time* (T_{rr}) values for the body diode. With inductive load tests, it was experimentally verified that these devices offer very large voltage spikes during reverse recovery transitions [49].[4] Furthermore, it was experienced that this also produces large EMI and induces ringing in the gate terminal of the MOSFET, which is highly undesirable. The devices B and D are good solutions to this problem due their lower Q_{rr} and T_{rr} values. These devices are designed for applications in *Synchronous Rectifiers* where extremely good reverse recovery characteristics of the body diode are a must [50]. As their voltage rating is usually limited to 100 volts, their application is limited for only low voltage

TABLE 5.1: Comparison of Device Parameters of Different MOSFETs Available in the Market that were Tested During the Prototype Stage of the Inverter Leg Design

Name	Device	Type	V_{DS} (V)	I_D (A)	R_{DS-on} ($m\Omega$)	Q_g (nC)	Body Diode			C_{iss} (pF)	C_{rss} (pF)	Package
							t_{rr} (ns)	Q_{rr} (nC)	V_d (V)			
A	STD17NF25	Si	250	10	140	29.5	157	910	1.6	1000	28	TO-252
B	IRFR4510PbF	Si	100	45	11.1	54	34	47	1.3	3031	104	TO-252
C	IPx60R125C6	Si	600	19	125	96	510	10000	0.9	2127	-	TO-263-3
D	FDB120N10	Si	100	52	9.7	66	44	67	1.3	4215	170	TO-263-3
E	SCT2080KE	SiC	1200	28	80	106	31	44	4.6	2080	16	TO-247
F	SCH2080KE	SiC	1200	28	80	106	37	60	1.3	1850	20	TO-247

Note 1: for packages; TO-252=DPAK and TO-263-3=D2PAK.
Note 2: the device parameters have their usual meaning in common data sheet literature.

[4] This effect presents itself due the MOSFETs' low turn-on and turn-off times. One can considerably mitigate this effect by increasing the value of the gate resistance, thus forcing the MOSFET to switch slowly. But, this hinders the object of using MOSFETs in the first place: which is faster switching.

testing. A system using FDB120N10 MOSFETs is currently used in the laboratory as a $Low\ Voltage\ Test\ Platform$ for PWM concept testing.

However, it was decided to further extend the voltage capability of the inverter system. Therefore, two Silicon Carbon (SiC) devices, E and F, were chosen due to their higher voltage rating and good body diode reverse recovery characteristics. Both devices perform extremely well as far as voltage spikes, EMI and gate ringing are concerned. The only difference between the two devices is that device E has a body diode whose forward voltage drop (V_d) is significantly large (4.6 V):[5] this results in considerable conduction losses when the diode conducts. However, device F eliminates this issue by integrating a SiC Schottky Barrier Diode (SBD) in parallel to the integral body diode and results in a V_d of only 1.3 V. Therefore, device F, $SCH2080KE$ from $ROHM\ Semiconductor$, was chosen as the MOSFET of the final medium-voltage inverter leg system. Some interesting discussions on SiC MOSFETs and their selection can be found in [51–53].

An important device parameter of MOSFETs is its *Miller Capacitance* which represents the gate-to-drain capacitance, C_{gd} [50, 54–56]. This is signified by the parameter C_{iss} in Table 5.1. Consider an inverter leg where the bottom switch is turned off and the top is just turning on. Two important events can be identified here:

1. Due to the high dv/dt across the top switch, a capacitive current flows through the bottom device. The higher the value of C_{gd}, the higher value of the developed spurious voltage across the bottom device's gate terminal (*Miller Effect*): and results in fault triggering in the bottom device. Therefore, lower C_{iss} values are usually preferred.
2. Body diode of the top device turns off forcing its reverse recovery current through the bottom device. In this case, the miller capacitance as well as the gate-source capacitance C_{gs} act as a snubbers [57] and help to mitigate the voltage spike developed across the bottom device due to stray inductances [4].

5.3.2 The Gate Driver Circuit and Protection Features

The IC *2ED020I12-F2* from *Infineon* [58] was selected as the gate driver chip. This is a dual IGBT/MOSFET gate driver chip with following appealing features: 1) isolation of 1.2 kV from control to power side, 2) support for IGBTs and MOSFETs up to 1200 V of

[5] This is an inherent characteristic of SiC MOSFETs due to their higher bandgap voltage.

V_{DS}, 3) 2 A rail-to-rail output gate current, 4) Desaturation Monitoring for short circuit protection, 5) Active Miller Clamp for faster turn-off and prevention of fault triggering due to miller effect. The chip has two independent and isolated power side circuits, *High Side and Low side*, to control two switches (see Fig. 5.2).

A detailed analysis of the gate driver chip is out of the scope of this report; but, the reader is encouraged to refer to the literature [59] as it provides a comprehensive application note of the device. The following sub sections present some important aspects of gate driver design that are quite essential to any gate driver design.

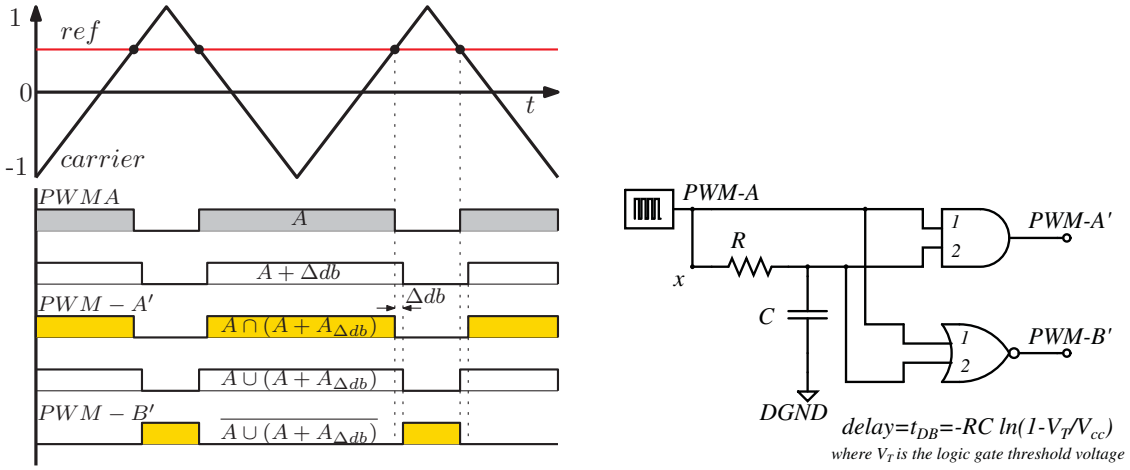
5.3.2.1 Dead-Band Unit

Dead-time or (dead-band) is a protective feature for an inverter leg to prohibit the two switches from turning on at the same time when complementary switching is used. This is achieved by delaying a switch turn-on event by a small time delay (allowing the other switch to fully turn off). The advanced designer is accustomed to programming the dead-time within the program code. But, sometimes it is safer to have an in-built hardware dead-band unit as well. Therefore, such a unit is integrated to the inverter leg circuit as shown in Fig. 5.2.

The user is provided with the option of by-passing this unit using an on-board switch. This is because, for independent switching of the two switches, as in the case of MDPWM2 scheme, separate access to the two switches is required. The implemented dead-band unit uses *Active High Complementary* [60] method as illustrated in the waveforms in Fig. 5.3(a). The practical realization of this using logic gates is shown in Fig. 5.3(b).

Consider the instant where $PWM-A$ is set to logic high ($t=0$). The voltage across the capacitor with time, v_c, is given by $v_c = v_x(1-e^{-t/RC})$. In this case, the voltage at point x, v_x is simply the control side supply voltage $V_{cc} = 5\ V$. The logic input 2 of both *AND* and *OR* gates see logic high only when the voltage across the capacitor goes above the IC's logic threshold voltage, V_T (which is 2.5 V for *SN74LVC* series). Therefore, for the instant where $v_c = V_T$ (that marks the end of the dead-band, $t = t_{DB}$), we can write, $V_T = V_{cc}(1-e^{-t_{DB}/RC})$. Simplifying the expression, the dead-time is given by:

$$t_{DB} = -RC \times \ln\left(1 - \frac{V_T}{V_{cc}}\right) \tag{5.1}$$



(a) Corresponding logic waveforms (b) Circuit diagram

FIGURE 5.3: A simple dead-band unit design with minimum components: Active High Complementary (AHC) dead-band logic

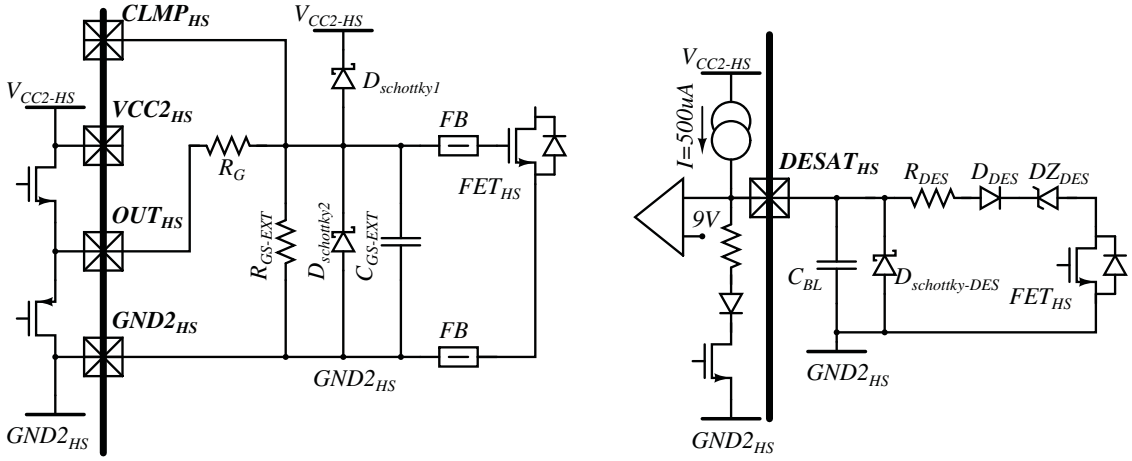
For the design, R is chosen as 510 Ω and C is chosen as 100 pF: which results in a dead-band around 35 ns.

5.3.2.2 Gate Driver Circuitry

The most important part of an inverter leg design is the gate drive circuitry, and therefore, this needs careful attention during the design process. A detailed version of the power side gate circuit portion of Fig. 5.2 is shown in Fig. 5.4(a). The output pin names are quite self explanatory, although they are derived with accordance to the gate driver chip's terminology. The reader is encouraged to refer to the references [58] and [59] for additional details.

One of the major problems in high speed MOSFET gate driving is the high frequency ringing of the gate terminal [49, 50, 57, 61]. Two main reasons exist: 1) the reverse recovery current of MOSFET body diodes, and 2) the effect of miller capacitance. Furthermore, the ringing of the gate propagates to the gate driver chip's inside circuitry through OUT_{HS} and $GND2_{HS}$ pins, and challenges the OUT_{HS} pin's ability to hold a particular gate voltage level. To overcome this problem, *Ferrite Beads* (FB)[6] are put in series with the signal

[6]Ferrite beads provide a large impedance, but only to very high frequency signals, usually well above the kHz range and act as a short circuit for signals below that range.



(a) Gate driving concerns: performance and protection features for fast switching

(b) Desaturation Detection for short circuit (or over current) protection

FIGURE 5.4: Gate driver circuit implementation with Infineon 2ED020I12-F2 chip

paths as illustrated in Fig. 5.4(a) [54–56]. Note that, the capacitor C_{GS-EXT} acts as a gate snubber to limit the ringing of the gate terminal. This is an extremely important and effective solution to the effects of reverse recovery problems and is not a commonly found solution on literature.[7] Extensive experiments were carried out to examine the effect of this and a capacitance of 4.7 nF was selected. However, large capacitance values are not suitable since they increase the MOSFET turn-on and turn-off times.

Two schottky diodes are placed to protect the gate terminal from exceeding the supply voltage above 15 V or below 0 V. The diodes become forward biased and clamp the gate node to the supply lines if the gate voltage exceeds these limits. The resistor R_{GS-EXT} is used to tie the gate node to the local ground. This is to protect the gate node from static discharges. The value of this resistance should be very large compared to the gate resistance R_G, so that the full supply voltage is delivered to the gate terminal:

$$V_{GS} = V_{OUT_{HS}} \frac{R_{GS-EXT}}{R_{GS-EXT} + R_G} \tag{5.2}$$

The chosen values for R_{GS-EXT} and R_G are 2.2 $k\Omega$ and 10 Ω respectively. This results in $V_{GS} = 0.9954\, V_{OUT_{HS}}$ which is acceptable.[8]

[7] The only reference on this is found on [57].

[8] At steady states, $V_{OUT_{HS}}$ is either at 0 V (OFF state) or 15 V (ON state).

The gate resistor R_G determines the turn-on and turn-off times of the MOSFET, and therefore, effectively determines the switching losses of the system as well. The turn-on and turn-off times, should not be very small as it increases high frequency voltage spikes across the power switches. But on the other hand, they should not be very large as it slows down the system and increases switching losses. Accepted range for gate resistor values for both MOSFETs and IGBTs lies within $1 - 10$ ohms [62]. Also, note that the gate resistor should be of a relatively high-wattage package as the peak gate current can rise up to few amperes.[9] The total gate resistance $R_{G-total}$ is given by:

$$R_{G-total} = R_G + R_{G-FET} \tag{5.3}$$

where R_{G-FET} is the MOSFET's internal gate resistance which is equal to 6.3Ω [58] for the selected MOSFET. For this design, therefore, the maximum gate current I_{G-max} can be calculated as:

$$I_{G-max} = \frac{V_{CC2-HS}}{R_{G-total}} = \frac{15}{10 + 6.3} = 0.92\ mA \tag{5.4}$$

This is below 2 A, which is the maximum allowable gate current limit for the selected gate driver chip [58].

Note that, for the SiC devices, a gate voltage of 15 V is still acceptable,[10] and therefore, the same gate driver chips that are used for IGBTs and Silicon MOSFETs can be directly used for SiC devices. The design guidelines that were carried out for $SCH2080KE$ MOSFET usage can be found on the literatures [51–53].

5.3.2.3 Additional Protection Features

1) Desaturation Detection: this is a protection feature used by smart gate driver [58, 63] chips to turn off the power switches should an excessive current flows through them due to fault conditions (such as load over currents or dc-link short circuits) [59, 64, 65]. When an excessive current flows through an MOSFET in *ON* state, the drain-to-source

[9] A resistor of 0.5 W with *0805* surface mount package is used in the design.

[10] The recommended value is 18 V. But, a lower gate voltage would only increase the value of R_{DS-ON} slightly, and therefore, this does not pose a significant design issue. Note that, isolated dc-dc converters with 18 V outputs are not a common product in the market as well.

voltage ($V_{DS} = R_{DS-ON} \times i_{DS}$) exceeds its normal value by a considerable margin.[11] The desaturation detection circuit detects this and commands the gate driver chip to turn off both high and low side outputs: $v_{OUT_{HS}} = v_{GND2_{HS}}$ and $v_{OUT_{LS}} = v_{GND2_{LS}}$.

Consider the operation of the high side circuit as shown in Fig. 5.4(b). Note that this protection feature is activated only if PWM_{HS} (see Fig. 5.2) from the control side states that the high side output should be driven high. Assuming this is the case, a current source ($I_{desat} = 500\mu A$) is activated whose current is forced to flow out through the $DESAT_{HS}$ pin to the external circuit. This current will charge the *Blanking Capacitor* C_{BL} till its voltage reach a value where it could forward bias the diode D_{DES}. When this happens, C_{BL} stops charging: and I_{desat} flows through D_{DES} and then through the MOSFET and back to $GND2_{HS}$. The voltage across C_{BL} during this state is given by,

$$v_{C_{BL}(max)} = I_{desat}.R_{DES} + V_{D_{DES}} + V_{DZ_{DES}} + i_{DS}.R_{DS-ON} \tag{5.5}$$

The value of $v_{C_{BL}(max)}$ is determined by the product $i_{DS}.R_{DS-ON}$ (other parameters are fixed). In normal operating conditions, $v_{C_{BL}(max)}$ is always less than a certain threshold voltage (9 V in this case). However, the value of $i_{DS}.R_{DS-ON}$ can move beyond normal operating condition value under excessive currents: forcing $v_{C_{BL}(max)}$ to go beyond 9 V. When this happens, the chip's desaturation circuit comparator detects an over current condition and shuts off both gate outputs. Assume a low power circuit where we want to turn off the circuit if the current through the MOSFET goes beyond 5 A. From the component values, we have: $V_{D_{DES}} = 0.4\ V$, $R_{DES} = 100\ \Omega$ and $R_{DS-ON} = 80\ m\Omega$ (see Appendix D). Then the zener voltage of $V_{DZ_{DES}}$ is calculated from Eq. (5.5):

$$9 = 500 \times 10^{-6} \times 100 + 0.4 + V_{DZ_{DES}} + 5 \times 0.08 \qquad \longrightarrow \qquad V_{DZ_{DES}} = 8.15\ V \tag{5.6}$$

A zener diode of 8.2 V can be selected and the value of R_{DES} can be slightly adjusted to get the required current limit. The schottky diode $D_{schottky-DES}$ is placed to protect the $DESAT$ pin from over voltages.

The protection circuit is enabled as soon as PWM_{HS} is set high. But, during the initial turn-on phase of the MOSFET, its voltage is in the process of coming from the very

[11] This concept was originally introduced for IGBTs. An IGBT switch that is in *ON* state under normal operating conditions is said to operate in the *Saturation Region* [4]. When an excessive current above normal conditions flows through an on-state IGBT, the operating region moves to the *Hard Saturation* region creating a collector-to-emitter voltage greater than V_{CE-sat}: and hence, the name *Desaturation Detection*.

large blocking voltage (usually V_{dc}) to the very low on-state saturation voltage. Therefore, a certain time delay, *Blanking Time* $= T_{BL}$, should be allowed for this process to be completed to avoid false turn-off of the circuit [59]. This is accomplished by selecting a suitable value for the blanking capacitor (value usually chosen in the range $50 - 200\ pF$). The worst case calculation is as follows: the capacitance should make certain that it takes a time equal to the required blanking time to be charged by I_{desat}, if it were to reach 9 V. The value of C_{BL} is given by,

$$C_{BL} = \frac{I_{desat} \times T_{BL}}{9} \tag{5.7}$$

For a 1 μs delay, $C_{BL} = (500 \times 10^{-6} \times 1 \times 10^{-6})/9 = 55.55\ pF$. For the design, C_{BL} was selected to be 56 pF.

2) Active Miller Clamp: this feature is used to avoid false triggering of switches (that are already turned off) due to the miller current caused by the Miller Effect. For example, consider the high side circuit. When the PWM_{HS} is set to logic low (from logic high), the gate terminal voltage of the switch is directly monitored through the $CLMP_{HS}$ pin as shown in Fig. 5.4(a) [58, 59]. As soon as this voltage goes below a certain threshold voltage V_{CLMP} (in this case 2 V), an internal circuit clamps the $CLMP_{HS}$ pin to $GND2_{HS}$. This clamping is kept active as long as PWM_{HS} is in logic low. Therefore, the miller current is forced to be diverted to the local ground, $GND2_{HS}$. This ensures that the gate terminal voltage is kept at $v_{GND2_{HS}}$, hence avoiding false turning on of the switch. The circuit is deactivated when PWM_{HS} is set to logic high again.

5.3.3 Layout Considerations

If the layout of a circuit is not properly designed, an army of problems would hinder the expected operation of the circuit; rather than testing the concepts it is originally built for, one would end up dealing with a diverse set of non related circuit issues (such as EMI issues, voltage spikes, false triggering, etc.).[12] This is really important when it comes to the design of power side of the circuit; where stray inductances and capacitances,and trace

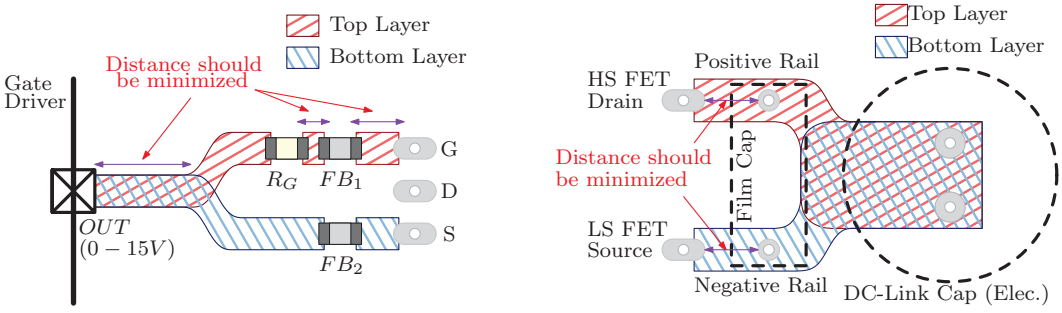
[12]This was something the author had to learn the hard way. Layout design is not as easy at it looks, and it takes time to learn and come up with the optimum layout. It is worth spending additional time on the layout design: otherwise, one would end up spending more time on non-related problems when it comes to experimental testing of the concepts.

resistance and inductances come in to play with the high frequency switching of the power switches. A detailed explanation on the carried out layout design is quite out of the scope of this report. However, the key aspects that should be followed in a good layout design are summarized below the for reader's attention [46, 61, 66–69].

On the Main Board and the Control Side of Inverter Leg:

- Digital and analogue units should have separate voltage regulators whose input power is drawn from a common original power source ($6 - 9\ V$ supply on the main board).
- Digital and analogue grounds have to be separated. The two ground planes are connected only at a single point near the original power source's ground terminal.
- Separate the PWM side ground plane from the common digital ground and connect them only at a single point.
- Avoid ground loops.
- All filter capacitors should be placed near the input sides of considered signal lines. This filters out the noise picked up by the line before the signal is fed to an input.
- For all signal lines, a width of 10 *mil* is quite enough. For power rail lines on the control side, a larger width is recommended (at least greater than $30 - 40$ *mil*).[13] [70–72] are some good online resources that help to decide the trace width.

On the Power Side of the Inverter Leg:



(a) Chip-to-gate design: minimizing gate terminal oscillations (ringing)

(b) DC-ink design: EMI and voltage spike minimization at power rail and ouput terminals

FIGURE 5.5: Important layout considerations for the inverter leg design

[13] 1 *mil* is equivalent to a 1/1000 *th* of an inch.

- For any trace: the higher width, the better the chances of reducing effects of stray inductances. However, the size limitation of the circuit should also be considered here.
- The gate resistor and the ferrite bead should be placed as close as possible to the gate terminal of the MOSFET. This is illustrated in Fig. 5.5(a). The width of the gate signal line has number 1 priority as far as the signal lines of power side are considered. The higher the width, the better the gate circuit performance.
- If possible, gate signal's return path back from the source of the MOSFET should be kept directly below the forward signal path (see how signal lines are on top of each other in Fig. 5.5(a)). This minimizes the loop area for the overall gate signal path (loop areas act as antennas for high frequency signals).
- The distance between the OUT_{HS} pin and the gate of the MOSFET should be as short as possible.
- The terminals of the dc-link film capacitor should be as close as possible to the high side MOSFET's drain and the low side MOSFET's source terminals. This is the number one priority for the power rails of the power circuit and is shown in Fig. 5.5(b). The film capacitor should have a very small equivalent series resistance (ESR) value: and is usually selected around $1 - 5\ uF$.
- The paths leading from the film capacitor to the electrolytic capacitor should have a minimum loop area. Usually, this is accomplished by overlapping the two paths on top and bottom layers as shown in Fig. 5.5(b).
- One important solution to minimize the generated EMI is to curve the traces with a round shape where they have to be bent. This offers better performance than having 45° bends (note that 90° bends are not acceptable and is a bad layout habit).

With consideration to design parameters, protection features and layout requirements presented in this chapter, the final design of the inverter leg was developed as shown in Fig. 5.6. Note that, although the design guidelines concentrated on the main board and the inverter leg, the presented techniques are quite general and can be applied to other related designs as well.

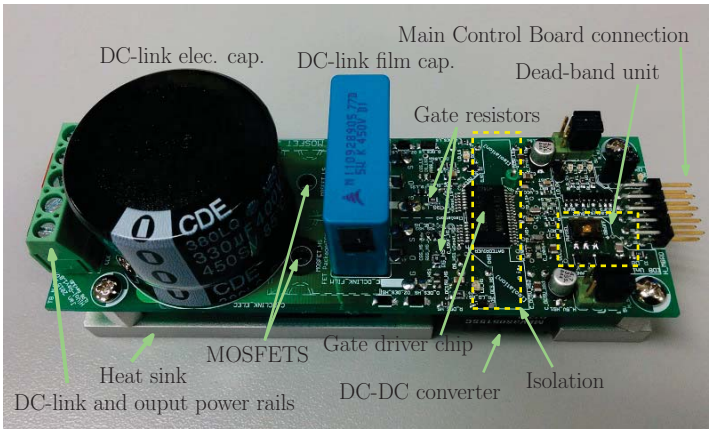


FIGURE 5.6: The developed SiC-MOSFET based Versatile Inverter Leg

5.4 VISSIM ECD Environment

The *VisSim/Embedded Controls Developer* (VisSim/ECD) is the computer integrated software environment used for the control of the DSP [73]. This is a model-based development environment for embedded units and is compatible with many DSPs from Texas Instruments. The main advantage of this, compared to the conventional code based (for example, the *Code Composer Studio* design environment for TI controllers) environment, is the visual representation of control blocks, DSP registers, signal monitoring and signal controlling.

The designed controller inside the VisSim/ECD environment for TMS320F28335 DSP to implement the DPWM schemes is presented graphically in Appendix D (Fig. D.1 and Fig. D.2) . The software communicates with the main board mounted DSP using a *Blackhawk USB2000 Emulator (USB2000)*[74, 75]. The control interface has the following key features:

1. Supports execution of all four DPWM schemes (SDPWM1, SDPWM2, MDPWM1 and MDPWM2) on a single interface.
2. Supports dynamic control of PWM carrier frequency, reference modulation index and reference frequency (therefore, allows V/F control).
3. Supports fault detection and forced resetting of inverter legs.

Chapter 6

Experimental Results and Performance Analysis

The difference between simulating a concept in a computer simulation program and actually testing it with real hardware could only be understood by facing the demons of experimental testing. The variety of problems faced during the hardware development and experimental testing, especially in power electronic circuits, is quite surprising. More often than not, the hardest part in this is finding the root of the problem, not the solution: that is, finding the part of the circuit that causes the problem and the cause itself.

Experimental analysis on various performance criteria of the developed concept is presented to verify its benefits over other schemes. Firstly, to provide a comparison of graphical nature, important experimental waveforms of the considered schemes are presented. With collected performance data at various modulation indices, with the aid of two watt meters, the second part of the chapter compares the performance factors of MDPWM2 scheme to other schemes. It is shown that the MDPWM2 is a successful scheme for a low cost DSP environment and performs expected excitations in the magnetic core.

6.1 Experimental Setup, Test Conditions and Waveforms

THE three-phase 3-limb core coupled inductor unit used in the experiments is designed with 6 mil laminations and has a self inductance of 12.5 mH for each phase inductor

(top + bottom windings). Before moving into the experimental results, it is important to clearly state the test conditions of the experiments.

- The fundamental (or reference) frequency (f_1) is always kept at 60 Hz.
- For the two modified DPWM schemes (MDPWM1 and MDPWM2), the dc-link voltage is kept fixed at 180 V (unless otherwise stated).
- SDPWM1 (standard DPWM with interleaved carriers) scheme is always operated at $V_{dc} = 150V$ (to limit the large winding current).
- SDPWM2 (standard DPWM with inverse interleaved carriers) scheme is operated at either 150 V and 180 V dc-link voltages, and this is specified in each graph or plot.
- The three-phase RL load is fixed at $R = 20\ \Omega$ and $L = 1.5\ mH$ for all the experiments.
- The PWM carrier frequency (f_c) is altered between 6, 8, 10 and 12 kilohertz and is specified in each graph or plot.

6.1.1 Hardware Setup and Control Interface

Fig. 6.1 shows a full view of the experimental setup. A single phase autotransformer of 115 V ($VARIAC^{®}$ from General Radio Company) is used with a diode rectifier (with a filter capacitor) to get a dc-link voltage of $150 - 180\ V$. A *Tektronix DPO3014* Digital

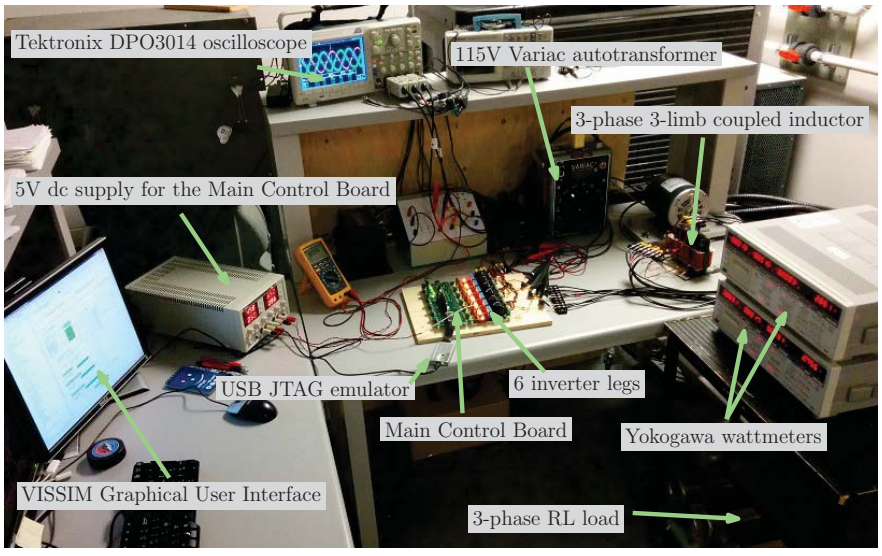


FIGURE 6.1: A full view of the experimental setup

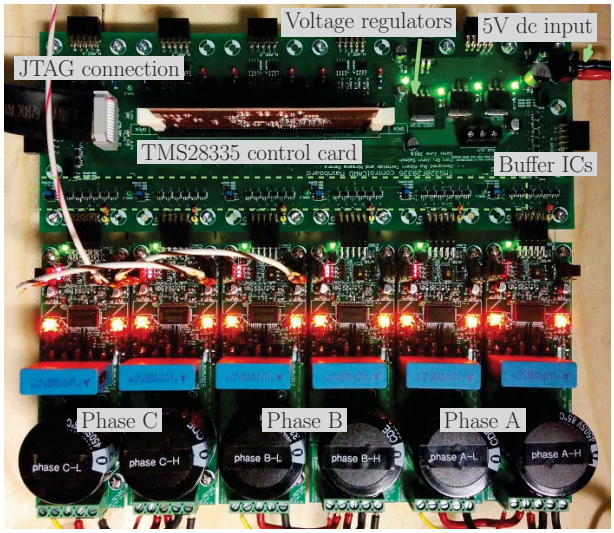
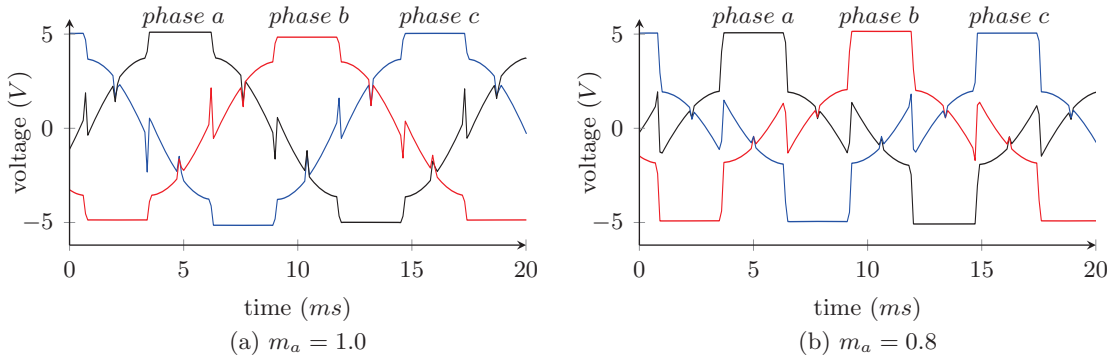


FIGURE 6.2: A closer view of the control unit and the inverter legs

Phosphor Oscilloscope is used to observe and record waveform data with the aid of *Tektronix TCP0030* current probes and *Tektronix P5200* high voltage differential voltage probes. The control board and MOSFET inverter boards are closely shown in Fig. 6.2. The control board communicates with the PC based VISSIM/ECD control program using the JTAG interface. This allows dynamic updating of control parameters such as modulation index, fundamental frequency and carrier frequency without the need to reprogram the DSP.

As a preliminary test result showing the correct implementation of the proposed scheme, Fig. 6.3 illustrates a waveform obtained through a special mode of the oscilloscope.



(a) $m_a = 1.0$ (b) $m_a = 0.8$

Note: *phase a* $= v_{gTA+} - v_{gTA-}$, *phase b* $= v_{gTB+} - v_{gTB-}$ and *phase c* $= v_{gTC+} - v_{gTC-}$

FIGURE 6.3: Experimental waveforms showing 5 V reference signal synthesis (60° discontinuous modulation type) for three phases by MDPWM2 scheme ($f_1 = 60\ Hz$, $f_c = 10\ kHz$)

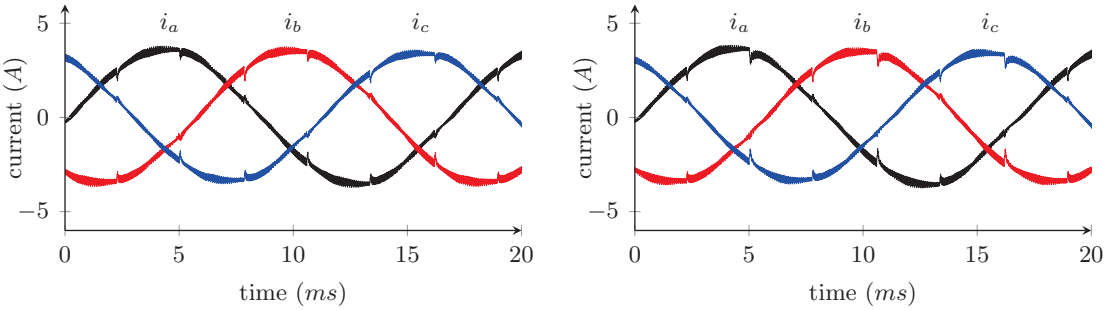
This is measured using only 1000 *Samples* in the *High Resolution* mode of the oscilloscope, which effectively provides a low-pass filter behaviour. Note the similarity between the jumps in sector transition points of this and the DPWM reference pattern in shown Fig. 3.15(a). The smaller jumps in mid-sector points are due to the change of the switching logic of the two operating phases at each mid sector point (see Section 3.3.2).

The following subsections compare experimental current and voltage waveforms addressing the key differences of the proposed scheme in contrast to other schemes.[1]

6.1.2 Three-Phase Output Current Waveforms

Fig. 6.4 shows the three-phase output current waveforms for the two standard DPWM schemes; however, they do not explicitly illustrate the difference between them. This is expected as the distinction between them lies on the circulating current pattern which does not appear on the output current (circulating currents are compared in the next subsection). The same observation applies for the two MDPWM schemes.

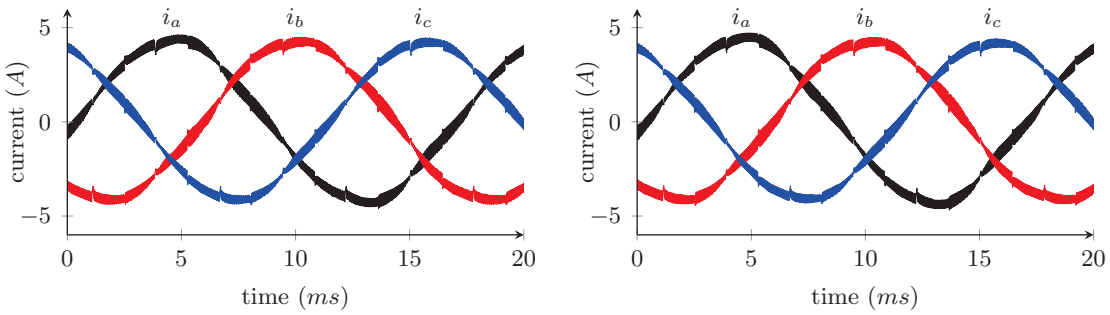
Fig. 6.5 shows the three-phase output current waveforms for the two modified DPWM schemes. The effect of the sector transitions can be seen as small jumps in the waveforms after each 60° portion of the current for both standard and modified DPWM schemes. But, for the MDPWM schemes, the effect of the mid sector transitions can also be seen as



(a) Standard DPWM - same carrier (SDPWM1) (b) Standard DPWM - inverse carrier (SDPWM2)

FIGURE 6.4: Experimental waveforms comparing three-phase output currents of the two standard DPWM schemes (V_{dc} =150 V, $f_c = 12\ kHz$, $m_a = 1$)

[1] The waveform data were saved as "*.csv*" data files in the oscilloscope and were imported to the computer in the same format. Then, the "*.csv*" files were processed in MATLAB, and subsequently in LaTeX and its package *PGFPLOTS*, to deliver the graphical illustration shown in the figures.



(a) Modified DPWM without WEF: MDPWM1 (b) Modified DPWM with WEF: MDPWM2

FIGURE 6.5: Experimental waveforms comparing the three-phase output currents of the two modified DPWM schemes (V_{dc} =180 V, f_c = 12 kHz, m_a = 1)

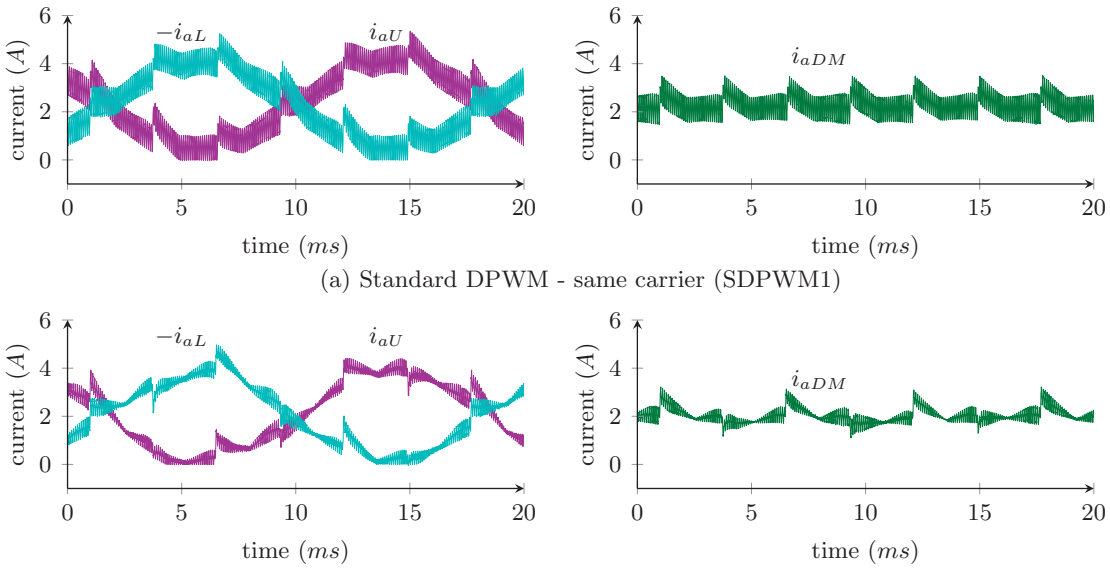
additional jumps occurring at 30° intervals (between the primary sector jumps). Note that, there are no mid sector transitions in the SDPWM waveforms as there is no change in the switching logic at mid-sector points.

It can be observed that the output current ripple's peak-to-peak value, on an average sense, is slightly higher for the MDPWM schemes compared to the SDPWM schemes. The reason for this can be explained by referring to the output voltage patterns of the two schemes in Section 6.1.4. For instance, consider the line voltage patterns: the two MDPWM schemes have voltage steps of V_{dc} for a certain portion of the fundamental cycle (and therefore, a higher ripple), while the two SDPWM schemes always have $V_{dc}/2$ steps. The effect of this on the complete system is not that significant as the reduction of inductor losses with MDPWM schemes offers far superior efficiency benefits (see Section 6.2).

6.1.3 Comparison of Winding Currents and Circulating Currents for Different Schemes

The main characteristic that distinguishes the schemes considered in this work is the circulating winding current pattern and the individual winding currents themselves (the work itself is intended to reduce the high-frequency ripple of these two types of currents). When transiting from one scheme to another, unlike in the phase output current, a clear distinction can be seen in the waveforms of these two parameters.

Fig. 6.6 illustrates the top and bottom winding currents (i_{aU} and $-i_{aL}$) and the circulating current (i_{aDM}) of the two standard DPWM schemes for a dc-link voltage of



(a) Standard DPWM - same carrier (SDPWM1)

(b) Standard DPWM - inverse carrier (SDPWM2)

FIGURE 6.6: Experimental waveforms comparing phase-A winding (upper & lower) and circulating currents for the two SDPWM schemes (V_{dc} =150 V, $f_c = 12\ kHz$, $m_a = 1$)

150 V.[2] The first observation on both SDPWM1 and SDPWM2 is that the circulating current has a dc value approximately equal to a half of the peak value of the winding currents. This confirms the fact that the winding current is always positive (from the upper side to the lower side of the phase inductor) and has a differential mode (circulating) component according to Eq. (3.12): $i_{aDM} = (i_{aU} - i_{aL})/2$.

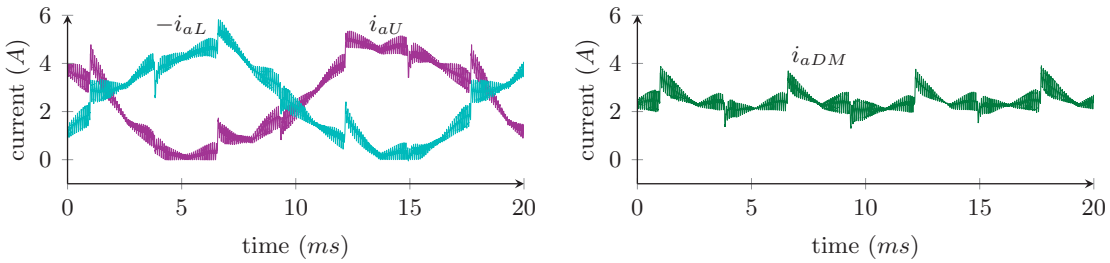
Consider the high frequency winding current ripple of the two schemes. SDPWM1 scheme has a ripple with a peak-to-peak value around 1 A, whereas SDPWM2 shows a significant reduction of this with a value less than $0.5A$ (neglecting the jumps at sector transitions). It can be concluded that, with moderate reduction of the time periods during which the magnetic flux leaves the magnetic core (within a carrier cycle), SDPWM2 scheme greatly reduces the high frequency current ripple. The circulating current waveforms explicitly confirm this observation.

With the introduction of MDPWM1 scheme, unlike the two SDPWM schemes, the winding voltage condition "$\sum v_{WA}+v_{WB}+v_{WC} = v_{W_{tot}} = 0$" is satisfied for all the switching states. Therefore, the magnetic flux is always contained within the 3-limb magnetic core

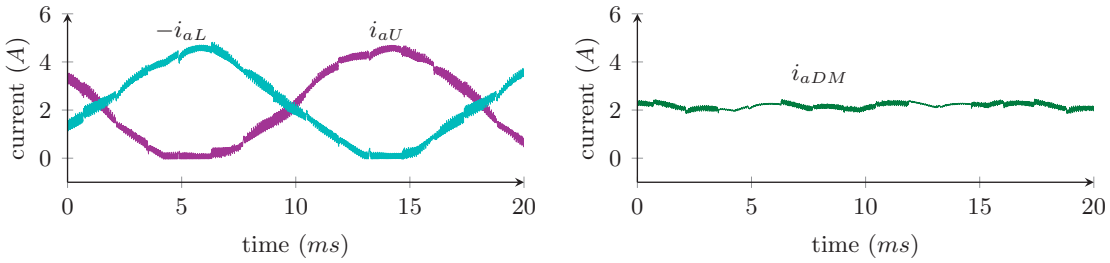
[2]Note that, the negative value of bottom winding current is chosen (for illustrative purposes) to keep both illustrated winding currents flowing in the positive direction of the circulating current.

irrespective of the switching state. And consequently, the high frequency winding current ripple is significantly reduced with the two MDPWM schemes as illustrated in Fig. 6.7. The figure compares winding and circulating currents of SDPWM2, MDPWM1 and MDPWM2 schemes at a dc-link voltage of $180V$. The distinction of the ripple in MDPWM schemes is quite articulate and essentially presents a simple dc value for the circulating current: with significantly lower sector transition effects on winding currents.

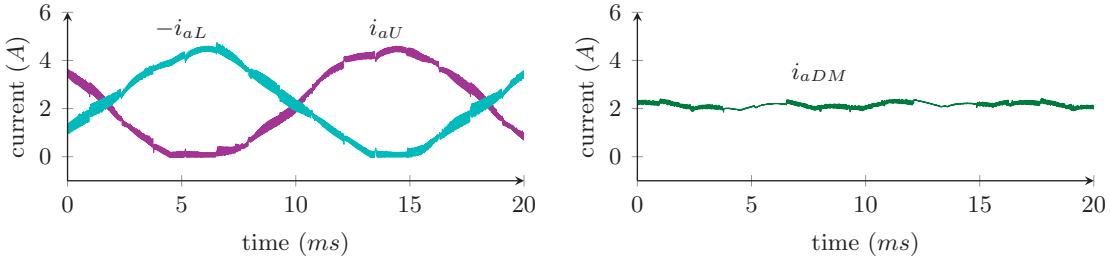
Note that, as far as the depicted waveforms in Fig. 6.7 are concerned, there is no clear distinction between the two MDPWM schemes. One reason for this is, as the both schemes satisfies "$v_{W_{tot}} = 0$" condition, the effects of flipping the winding excitation in MDPWM2 are not as significant as the effects observed when moving from SDPWM to the two MDPWM schemes. The other reason is that, the use of a high carrier frequency



(a) Standard DPWM - inverse carrier (SDPWM2)



(b) Modified DPWM without WEF: MDPWM1

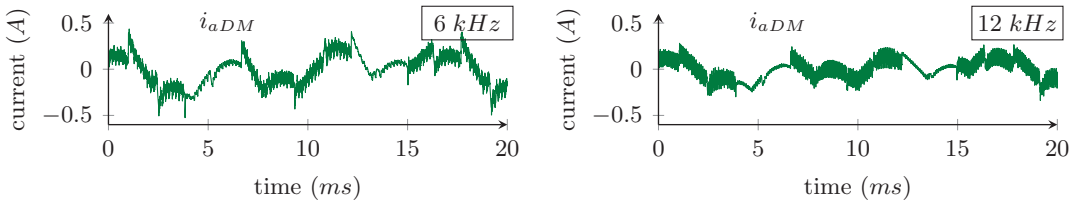


(c) Modified DPWM with WEF: MDPWM2

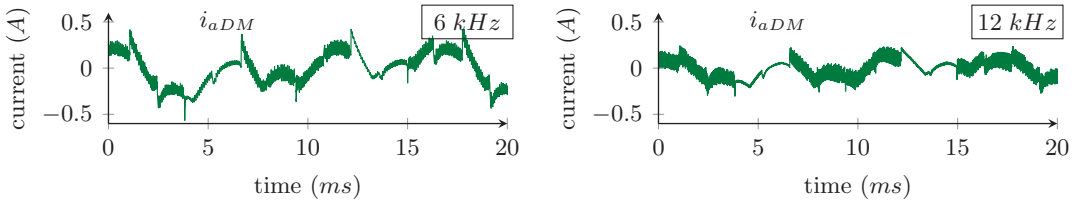
FIGURE 6.7: Experimental waveforms comparing phase-A winding (upper & lower) and circulating currents: SDPWM2 vs MDPWM (V_{dc} =180 V, $f_c = 12\ kHz$, $m_a = 1$)

of 12 kHz reduces the ripple to very lower value so that a clear distinction can not be observed.

Therefore, to present a clear visualization, the circulating currents of the two MDPWM schemes were captured with the *ac coupling* (removing the dc component) mode of the oscilloscope as illustrated in Fig. 6.8. The results are given for two carrier frequencies of 6 and 12 kHz. The 6 kHz version of the two schemes offer a better resolution: the effects of the flipped winding excitation of MDPWM2 is observable as opposed to the MDPWM1 scheme which has no flipping. Furthermore, the superior benefits of the flipping of the winding excitation is presented in the second part of this chapter with coherent winding loss calculations.



(a) Modified DPWM without WEF: MDPWM1



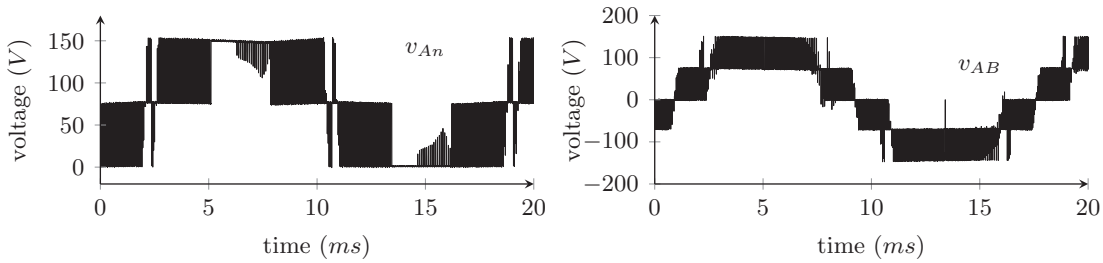
(b) Modified DPWM with WEF: MDPWM2

FIGURE 6.8: Experimental waveforms comparing phase-A winding circulating current (oscilloscope AC-coupled mode) for the two MDPWM schemes (V_{dc} =180 V, $m_a = 1$)

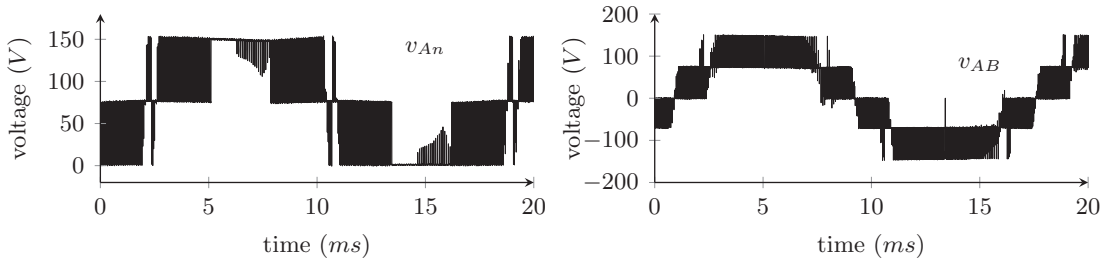
6.1.4 Output Voltage Patterns: Standard and Modified DPWM Schemes

The output phase-voltage for phase A (v_{An}), and the line voltage (v_{AB}) are compared between the considered schemes to provide another perspective, especially for the distinction between the standard and modified DPWM schemes as a whole.

Fig. 6.9 shows the voltage patterns for the two SDPWM schemes (for $m_a = 1$) and it can be observed that output voltage patterns for the two schemes are identical. This is expected as there is no alteration on the output voltage patterns when SDPWM2 is derived

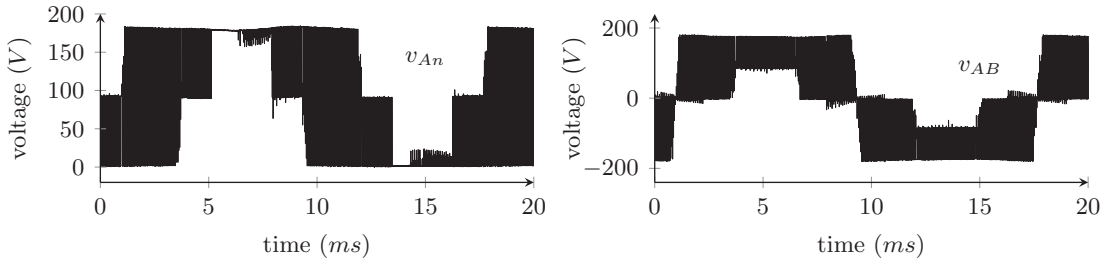


(a) Standard DPWM - same carrier (SDPWM1)

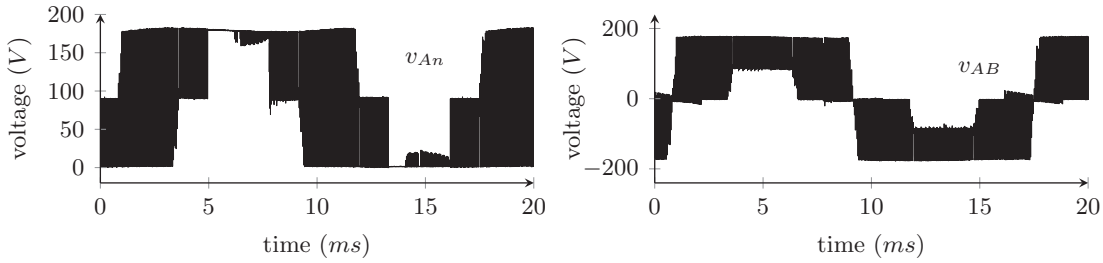


(b) Standard DPWM - inverse carrier (SDPWM2)

FIGURE 6.9: Experimental waveforms comparing phase and line voltages for the two standard DPWM schemes (V_{dc} =150 V, $f_c = 12\ kHz$, $m_a = 1$)



(a) Modified DPWM without WEF: MDPWM1



(a) Modified DPWM with WEF: MDPWM2

FIGURE 6.10: Experimental waveforms comparing phase and line voltages for the two modified DPWM schemes (V_{dc} =180 V, $f_c = 12\ kHz$, $m_a = 1$)

from SDPWM1 (see Section 3.3.1). The phase voltage pattern is 3-level (with $V_{dc}/2$ steps) while the line voltage has a 5-level (with $V_{dc}/2$ steps) pattern as expected from a standard

interleaved parallel inverter system.

Fig. 6.10 shows the voltage patterns for the two MDPWM schemes (for $m_a = 1$). As with the two SDPWM schemes, the output voltage patterns for the two MDPWM schemes are identical. But, a clear distinction can be made between the two groups: SDPWM and MDPWM schemes. The SDPWM phase voltage v_{An} shows a clear 3-level voltage pattern with $V_{dc}/2$ steps, though MDPWM at a first glance looks as a hybrid of 2-level and 3-level patterns with both V_{dc} steps and $V_{dc}/2$ steps. For example, at $t = 10\ ms$, v_{An} appears to switch between 0 and V_{dc} (essentially mimicking a bipolar voltage pattern): but, in fact, v_{An} transits to the voltage level $V_{dc}/2$ in between, and therefore, always having a 3-level pattern (mimicking the expected unipolar voltage pattern).

Furthermore, a closer look at v_{AB} is illustrated in Fig. 6.11. The figure shows a 10 ms duration of the fundamental period of the voltage pattern of v_{AB} for MDPWM2. It can be observed that the voltage pattern consists of both V_{dc} and $V_{dc}/2$ voltage steps. Here, v_{AB} can be considered as a hybrid of 3-level and 5-level line voltage patterns. And the type of voltage level varies depending upon the particular operating sector (or rather the half sector) of the considered phase.

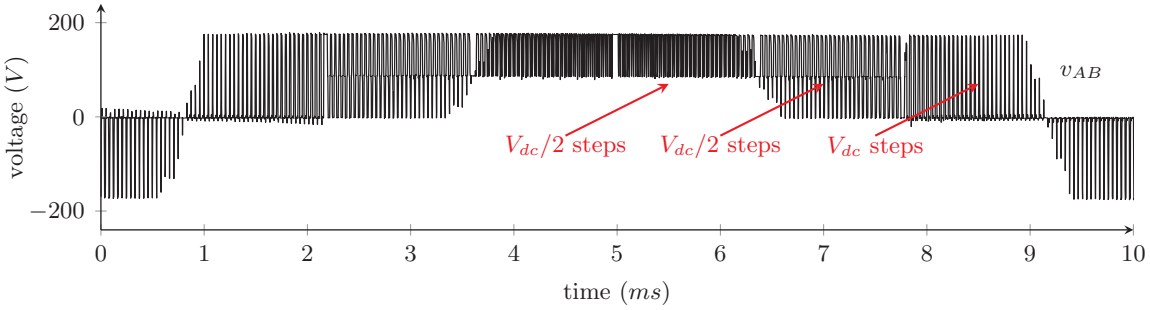


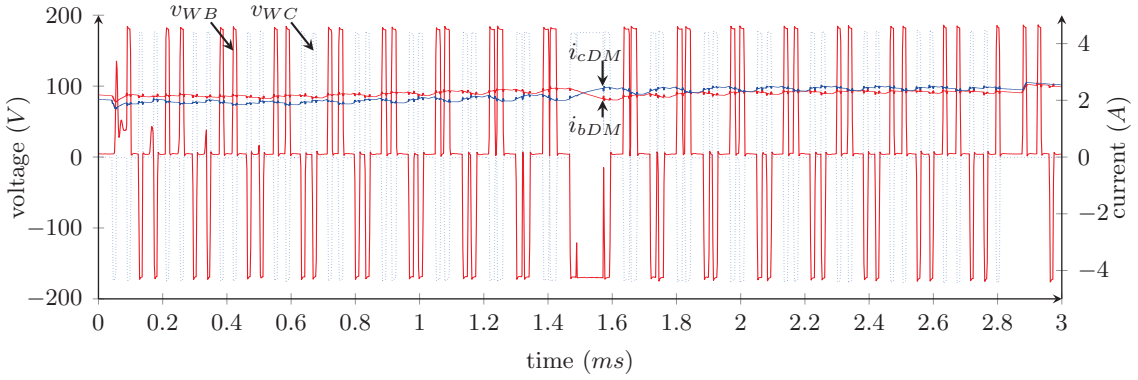
FIGURE 6.11: Experimental waveforms showing the voltage levels of the output line voltage (v_{AB}) of MDPWM2 scheme (V_{dc} =180 V, $f_c = 12\ kHz$, $m_a = 1$)

6.1.5 Winding Voltage Patterns: MDPWM1 vs MDPWM2

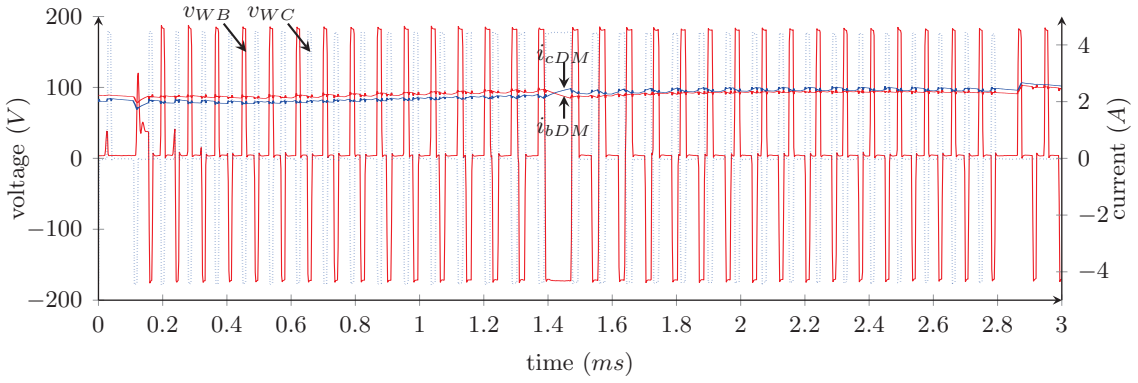
The proposed work in this thesis signifies the superiority of the MDPWM2 scheme over MDPWM1 scheme. In order to present a clear graphical verification of this fact, the winding voltages v_{WB} and v_{WC} of phase B and C windings (for sector 1) are illustrated for the two

schemes in Fig. 6.12. Furthermore, the circulating currents i_{bDM} and i_{cDM} of the two phases are superimposed on the same graph.

The flipping of the winding excitation in MDPWM2 scheme can be clearly observed in the voltage patterns. Also, note the effect on the winding voltage pattern at the mid sector point due to the altering of the switching logic at this point. Here, with reduced sampling points, but with a zoomed time axis, the reduction of the circulating current's peak-to-peak value in MDPWM2 is quite distinctive. The variation of the circulating current about its dc value is essentially halved in the MDPWM2 scheme as compared to MDPWM1.



(a) Modified DPWM without WEF: MDPWM1



(b) Modified DPWM with WEF: MDPWM2

FIGURE 6.12: Experimental waveforms showing the winding voltages and circulating currents for phases B and C during sector 1 (V_{dc} =180 V, $f_c = 12\ kHz$, $m_a = 1$)

6.2 Performance Analysis: Choosing the Better Scheme

The first part of this chapter examined the graphical nature of the system parameters such as currents and voltages as waveforms. And certain conclusions can be made on the viability of the considered schemes to excite a 3-limb magnetic core. However, performance parameters such as losses and efficiency, particularly at different modulation depths and carrier frequencies, offer a better picture on the capability of the system: and sometimes, details which are not readily observable in graphical waveforms. Therefore, some important performance factors are evaluated while placing the advantages of the proposed scheme in context.

To obtain the required data, two *Yokogawa* power analysers with 500 kHz bandwidth are used: $WT1030-253630-C1-1-D/5B$ and $WT1030-253630-C1-1-D/B5/HRM$. Note that, in order to save space in figure environments, the DPWM scheme names are abbreviated in plot legends as follows : $S1 = SDPWM1$, $S2 = SDPWM2$, $M1 = MDPWM1$ and $M2 = MDPWM2$.

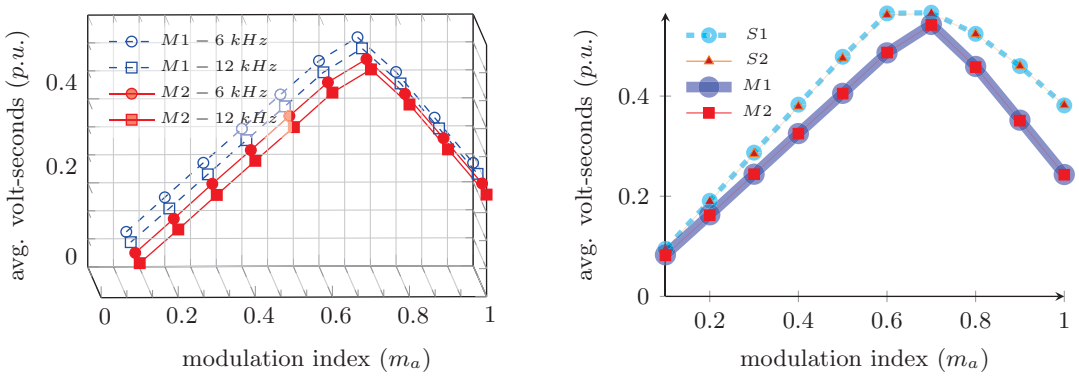
6.2.1 Inductor Iron Losses: Concept of Winding Average Volt-Seconds

The average value of the volt-seconds dropped across the phase inductors can be used to model the iron losses induced in the inductor magnetic core [15, 16]. The higher the value of this measure, the higher the losses induced in the magnetic core. This parameter can be calculated according to the following expression, where T_1 is the fundamental period and v_W is the voltage drop across any phase inductor (top winding + bottom winding):

$$average\ volt-seconds\ (p.u.) = \frac{1}{V_{base}} \cdot \frac{\int_{t_0}^{t_0+nT_1} |v_W|\ dt}{nT_1} \tag{6.1}$$

Here, n is the number of fundamental cycles where the measurements are accounted for, and a value greater than 3 gives better accuracy. The dc-link voltage is chosen as V_{base}.

Fig. 6.13(a) compares the variation of average volt-seconds with modulation index for the two MDPWM schemes at two different carrier frequencies (phase A is considered here, $v_W = v_{WA}$). Since the curves coincide on a 2-D graph, a 3-D view is used show all the four curves separately. Two important observations can be made here:



(a) Modified DPWM schemes: effect of f_c

(b) Different schemes at $f_c = 12\ kHz$

FIGURE 6.13: Winding average volt-seconds based on simulation results ($V_{base} = V_{dc}$)

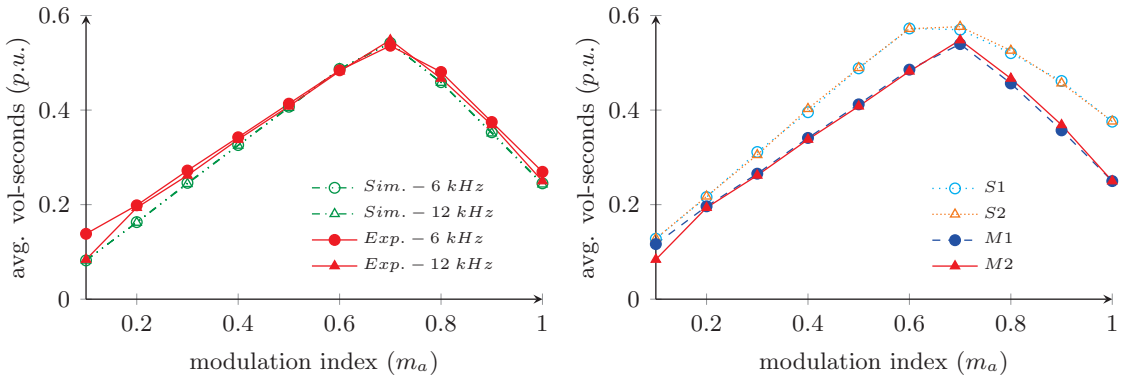
1. The value of average volt-seconds does not depend upon the carrier frequency f_c: increasing f_c has no effect when voltages are averaged over a fundamental cycle.[3] This depends only upon the winding excitation pattern inside a carrier period.
2. The curves of both MDPWM1 and MDPWM2 are identical: since the absolute values of v_W are identical for the two schemes.

Fig. 6.13(b) compares the average volt-seconds for all the schemes: both SDPWM and MDWPM schemes at $f_c = 12\ kHz$.[4] The modified scheme has lower average volt-seconds, hence lower iron losses, for the total range of modulation indices in contrast to the two SDPWM schemes. This is expected as the two MDPWM schemes have lower durations of winding excitations inside a carrier period when compared to the two SDPWM schemes (compare the winding excitation pattens in Fig. 3.16, Fig. 3.17 and Fig. 3.19).

Fig. 6.14 shows the average volt-seconds values based on experimental data, verifying the predictions made with the simulation results. The experimental curves closely follow the curves obtained with simulation results except for slight offsets in lower modulation indices ($m_a < 0.3$). This is due to the effect of slightly increased distortion in the winding PWM voltages, that is caused by the increased ripple and jumps in the winding circulating current

[3] The slight variations in the values are due to the non-ideal PWM voltages caused by the clipping of the winding circulating current at 0 A.

[4] For the two SDPWM schemes, the switching frequency f_{sw} and the carrier frequency f_c are the same, as there is only one switching cycle for the gate signals inside a carrier period. However, for the two MDPWM schemes, they are not the same: in fact, $f_{sw} = 2f_c$ as there are two switching cycles for the gate signals inside a carrier period (see Section 3.3). Note that, since f_c has no effect on the value of average volt-seconds for a given scheme, the same $f_c = 12\ kHz$ can be used to compare average volt-seconds for all the schemes.



(a) MDPWM2: simulated vs experimental

(b) Experimental: all schemes at $f_c = 12\ kHz$

FIGURE 6.14: Experimental comparison of winding average volt-seconds ($V_{base} = V_{dc}$)

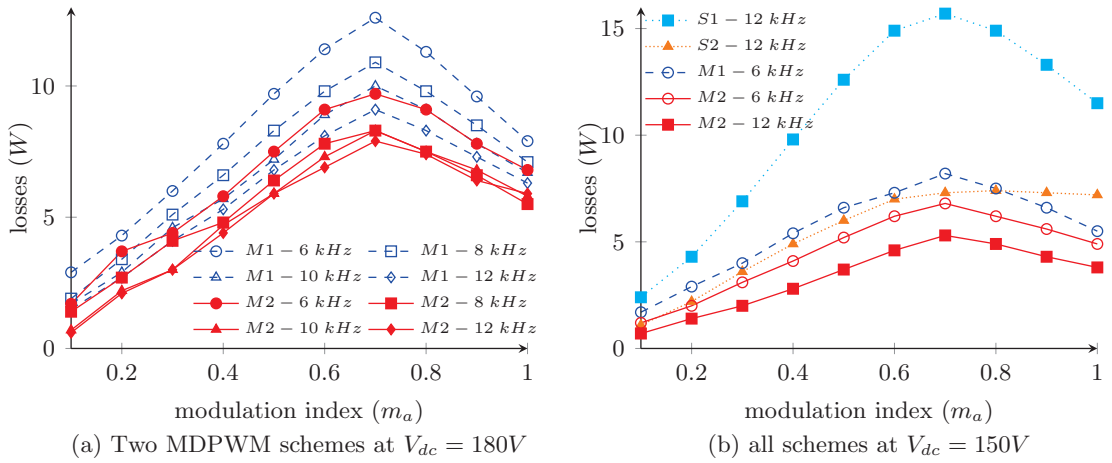
at lower modulation depths. In conclusion, the experimental results verify the superiority of the MDPWM schemes over the SDPWM schemes in reducing inductor iron losses.

6.2.2 Total Inductor Losses and its Relation to the Windings' Average Volt-Seconds

A good measure of the capability of the considered DPWM schemes in exciting a 3-limb coupled inductor core is a sound comparison of total losses (both iron and Cu) induced in the inductor core (for fixed dc-link and load conditions).

However, a proper measurement of the total inductor losses can only be made by individually measuring losses across each phase inductor with the aid of high-bandwidth watt meters. Therefore, to obtain the required results, two watt meters were used where each could measure active losses across three windings: one watt meter measured the losses of the top three windings of the three phases separately, while the other watt meter measured bottom winding losses for the three phases.

Consider the first plot in Fig. 6.15 which compares the inductor losses for the two MDPWM schemes at four different carrier frequencies. At lower carrier frequencies, the losses are higher due to the Cu losses caused by relatively large high-frequency winding current ripple. However, as the carrier frequency increases, the Cu losses go down (as the ripple is reduced) and the effect of iron losses becomes more visible.



(a) Two MDPWM schemes at $V_{dc} = 180V$

(b) all schemes at $V_{dc} = 150V$

FIGURE 6.15: Experimental comparison of total inductor losses (iron+Cu) at different f_c

For instance, consider the curves of MDPWM2: as f_c goes up, the loss curves tend to merge together and start to closely follow the average volt-seconds curve of the scheme. This is in complete agreement with the independence of the iron losses upon the carrier frequency as explained in Section 6.2.1. As far as the two schemes are concerned, MDPWM2 offers better performance in contrast to MDPWM1 at all carrier frequencies. This is mainly due to the reduced high-frequency winding current ripple of MDPWM2 scheme that lowers the Cu losses induced in the inductor core. This result marks one of the major advantages of MDPWM2 scheme over MDPWM1.

The second plot in Fig. 6.15 compares the total inductor losses of all four schemes at $V_{dc} = 150$. For the two MDPWM schemes, results for the carrier frequency of 6 kHz are also included to compare both SDPWM and MDPWM schemes at the same switching frequency of 12 kHz (see Footnote 4). SDPWM1 offers the worst performance at any modulation depth; and changing the scheme from SDPWM1 to SDPWM2, the losses are practically reduced by half. It is clear that MDPWM2 offers the best performance: and if the same carrier frequency of 12 kHz is considered, MDPWM2 offers superior performance having losses lower than a quarter of the losses produced by SDPWM1.

6.2.3 Total Harmonic Distortion of Winding Currents and Line Currents

Another measure of system performance for power electronics systems is the Total Harmonic Distortion (T.H.D.) of the output line currents and, especially for this work, the winding currents. The latter parameter for the two MDPWM schemes is plotted in Fig. 6.16 for different m_a values based on simulation results. MDPWM2 offers lower T.H.D. values at both carrier frequencies due to the flipping of the winding excitation.

The first plot of Fig. 6.17 compares the experimental and simulation T.H.D. values of phase-A line current (i_a) for MDPWM2, whereas the second plot compares the experimental T.H.D. values of i_a between MDPWM1 and MDPWM2. For same f_c, there is no significant difference in output current T.H.D performances of the two schemes: because, theoretically, the common mode currents ($i_{aCM} = i_a/2$) of the two schemes (see Section 3.1.1) are the same.

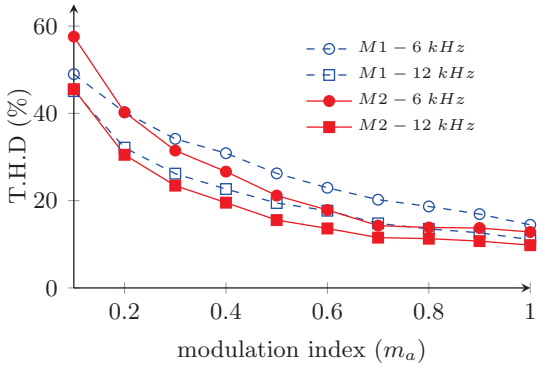
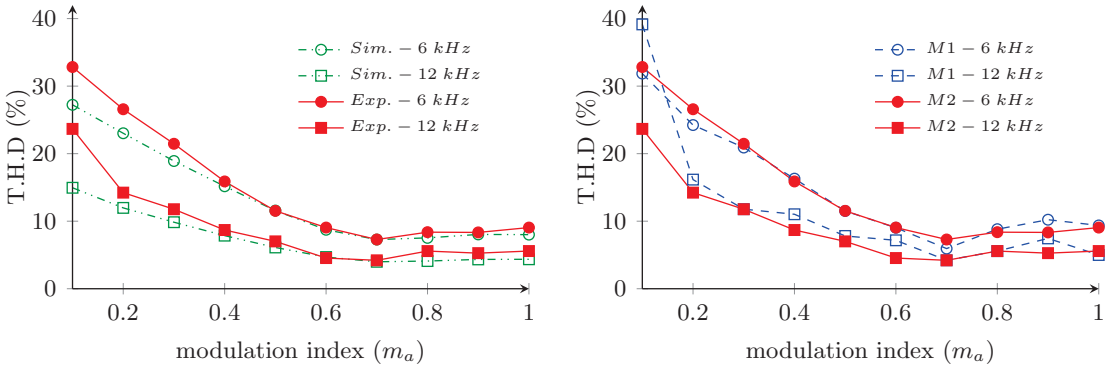


FIGURE 6.16: Simulated winding current T.H.D. curves: MDPWM schemes ($V_{dc} = 180$)



(a) MDPWM2: simulated vs experimental

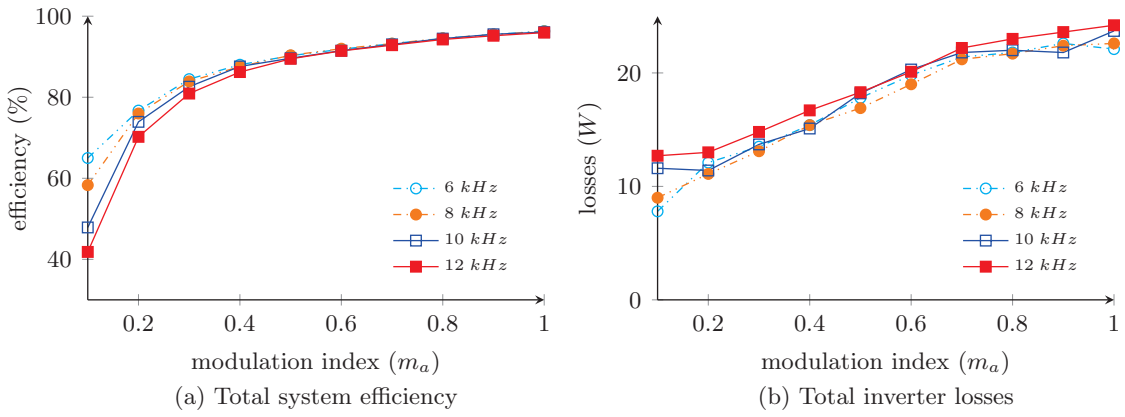
(b) Experimental: MDPWM1 vs MDPWM2

FIGURE 6.17: Experimental output current T.H.D. curves: MDPWM schemes ($V_{dc} = 180$)

6.2.4 Overall System Efficiency and Losses

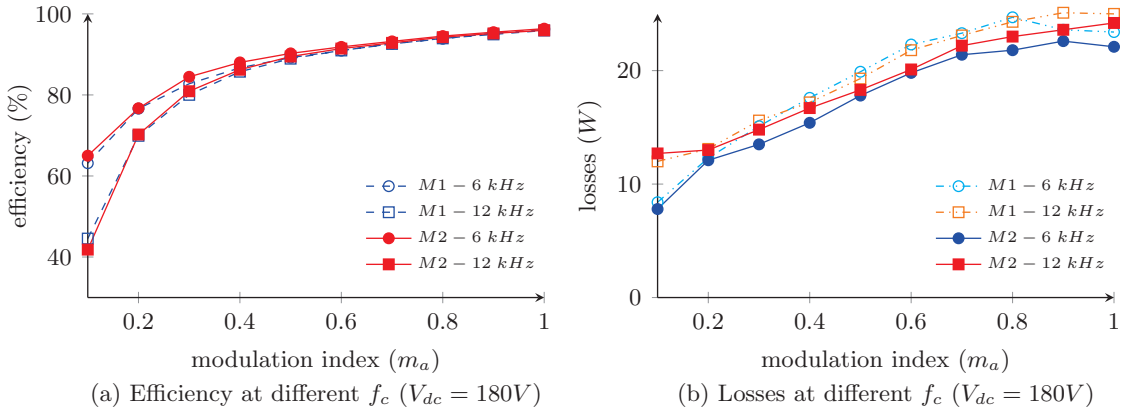
As a final and complete evaluation of the considered schemes, overall system efficiency of each scheme is analysed. Fig. 6.18 compares total system efficiency and losses of the MDPWM2 scheme at different carrier frequencies. And, Fig. 6.19 offers efficiency and loss variations of the two MDPWM schemes to draw conclusions on the better scheme.

Consider the standalone performance of MDPWM2 scheme as illustrated in Fig. 6.18 at $V_{dc} = 180V$. The slight increase of losses with increasing f_c can be attributed to the higher switching losses at higher carrier frequencies. However, as for the total system efficiency, the effect of f_c is insignificant for modulation indices greater than 0.2. The highest efficiency



(a) Total system efficiency (b) Total inverter losses

FIGURE 6.18: Experimental results showing overall performance of the MDPWM2 scheme at different carrier frequencies ($V_{dc} = 180V$)



(a) Efficiency at different f_c ($V_{dc} = 180V$) (b) Losses at different f_c ($V_{dc} = 180V$)

FIGURE 6.19: Experimental comparison of efficiency and losses: MDPWM1 vs MDPWM2

value is found to be 96.35% at $f_c = 6\ kHz$ (for $m_a = 1.0$) and for all the carrier frequencies the system efficiency is greater than 94% for $m_a \geq 0.8$.

Fig. 6.19 compares the performance of MDPWM2 scheme against MDPWM1 at $V_{dc} = 180V$. For m_a greater than 0.2, MDPWM2 has lower total losses at both carrier frequencies: in fact, losses of MDPWM2 at $f_c = 12\ kHz$ is lower than losses of MDPWM1 at $f_c = 6\ kHz$. It can be concluded that, where the lower inductor losses being the main reason behind, MDPWM2 offers better performance in contrast to MDPWM1.

Which Scheme Gives the Best Overall Performance?

For a fair comparison of the overall efficiency of SDPWM schemes against MDPWM schemes, a fixed switching frequency of $f_{sw} = 12\ kHz$ is considered rather than a fixed carrier frequency (see Footnote 4).

Fig. 6.20 first compares the two SDPWM schemes at $V_{dc} = 150V$, and then SDPWM1 is compared with the two MDPWM schemes at $V_{dc} = 180V$. SDPWM1 has the worst performance: and moving in to SDPWM2, by just inverting the carrier logic in the scheme, a significant increase in system efficiency is gained. SDPWM2 at both dc-link voltages offers approximately equal efficiency curves while they tend to merge with the curve of MDPWM1 when m_a is above 0.6. However, for the whole range of m_a, MDPWM2 offers the best efficiency performance in contrast to both SDPWM2 and MDPWM1. In conclusion, the effect of flipping the winding excitation in MDPWM2, though achieved by a simple change in modulation logic, results in a considerable performance increase.

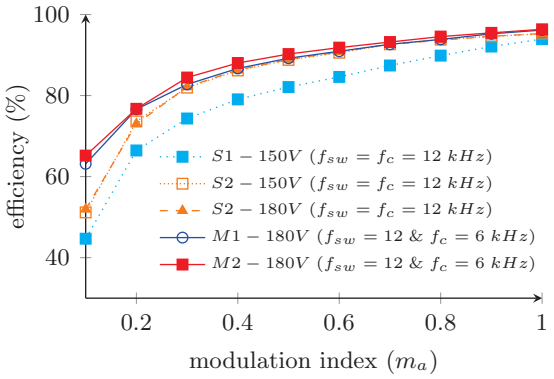


FIGURE 6.20: Experimental comparison of overall system efficiency of different schemes at the same switching frequency ($f_{sw} = 12\ kHz$): SDPWM vs MDPWM

Chapter 7

Conclusions and Future Work

One famous quote by Leonardo da Vinci states: "Learning never exhausts the mind ". Studying might exhaust the mind as well as the physical body, but not learning new things or contemplating new research ideas.

The material provided in this report proves a simple and low cost technique for exciting a three-phase, 3-limb core, 6-CII topology with a DSP based control environment. However, it is interesting to learn other potentials of the DSP based environment and the 6-CII topology itself. And especially, it is important to further investigate some design limitations found during the work, itself. Therefore, some noteworthy avenues for future extensions of the discussed work are presented. But first, the presented work is summarized, drawing some key conclusions as a concluding remark to the thesis work.

7.1 Summary of the Thesis Work

POWER electronic converters can be considered as the heart of modern power systems, especially with the emergence of renewable energy concepts. Inverters with lower losses are a key component in this regard. However, the resulting solutions should be low-cost and practicable (without unnecessarily complex design needs) to be thought of as acceptable solutions.

For low to medium voltage applications, 3-level inverters offer a low cost solution with a simpler design approach. One commonly used solution for this is parallel inverter systems. As far as parallel three-phase inverter systems are concerned, the 12-CII topology with coupled inductors increases the output conversion quality with some additional benefits. In contrast to the 12-CII topology, the 6-CII topology is introduced as a better solution due to its low cost and lower size with same conversion quality. To further enhance the system efficiency with additional cost reductions, a 3-limb magnetic core excited with discontinuous PWM schemes is introduced for the 6-CII topology. A thorough theoretical analysis on the topology is carried out in the first few chapters on this report to lay the foundation to the proposed study.

The standard DPWM schemes are identified as the best candidates which satisfy the basic requirements of the 3-limb core excitation. In fact, with modifications to the original references and modulation logic, two modified DPWM schemes can be identified as high potential candidates. However, the modified schemes are relatively complex and require extensive computations: which in turn calls for high-end processors. In this particular thesis work, a DSP based DPWM scheme is introduced as a simple and a low cost solution to excite the 3-limb core based coupled inductor inverter approach. The DSP itself is a less complex machine when compared to high-end processor systems like FPGAs. Therefore, the proposed scheme is tailored to be less complex: there is no post or parallel processing and exists only one carrier signal. A detailed presentation of the modulation strategy of the proposed scheme is presented in Chapter 4.

A MOSFET based versatile inverter leg system (for low to medium voltage applications) was designed and fabricated to test the proposed scheme. A fair amount of time was dedicated to tailor the inverter leg to perform well at high switching frequencies: though a detailed explanation on the design process is not presented due to space limitations of the report, a basic description is presented in Chapter 5.

Experimental results validate the DSP's ability to perform the required modulation task, with very low processing resources required from the DSP: the heap size, stack size or program memory are not exceeded beyond their limits. The experimental waveforms presented in Chapter 6 show that the winding currents show lower high frequency current ripple for MDPWM2 scheme, suggesting an overall improvement of system efficiency. And, the loss analyses performed on the candidate schemes show that MDPWM2 offers the best

performance benefits: at $m_a = 1$ and $f_c = 6\ kHz$, MDPWM2 results in an efficiency of 96.35% which was the best efficiency value recorded for all the four schemes considered.

7.2 Future Work

The proposed PWM scheme in this work is a carrier based modulation technique where the basic requirement is to satisfy the requirement "$v_{W_{tot}} = 0$". Therefore, only certain switching states are exploited in the scheme: not all the available states within a particular sector are utilized for their potential. Such an approach requires a new perspective on the switching states, the obvious tool being the space vector analysis. However, even if the space vector methods allow a new switching strategy, it will be quite interesting to see how such an approach would be reflected in the much familiar carrier based environment: or rather, to see whether it is possible to implement the extra switching states with a simple carrier based approach for a DSP environment; and if not, whether the benefits gained with new switching strategy are compelling enough to transfer to a new control environment to implement it.

One important result that could be identified with the experimental waveforms is the primary jumps (which occur due sector transitions) and the secondary jumps (at mid-sector points due to alternating modulation logic) in output and winding currents. The primary jumps are inherent due to the nature of the reference signals of the 60° discontinuous modulation technique. And, the secondary jumps are a direct result of the mid-sector modification of the modulation logic introduced by MDPWM schemes. However, the magnitude of the jumps are affected by several factors:

1. The *Frequency Modulation Ratio* ($f_m = f_c/f_1$) [4] of the scheme.
2. How the logic changes are updated in $AQCTLA/AQCTLB$ registers in the DSP.
3. The carrier frequency (f_c) itself, since it determines the duration of the jumps.

Therefore, with the effect both f_m and f_c, certain carrier frequencies may offer jumps with relatively lower magnitudes, and it is worth looking into avenues of determining optimal carrier frequencies. It is important to note, that a DSP only allow a limited number of options in configuring its PWM modules. Therefore, even if a method is found to limit these jumps, the DSP itself might not be able to achieve this task. Then, it should be decided

whether to reach for a high-end processor to achieve this while increasing the design cost. In this regard, it should be determined whether the benefit offered by the reduced jumps are significant enough so that it justifies the increased system cost.

One aspect observed during the loss calculations of the inductor windings is that the individual losses (iron+Cu) of the three inductors (of the three phases) are not exactly the same (neglecting the effects of the unbalance of three-phase output currents). It was observed that phase A and C winding losses are more or less equal; however, phase B winding losses were lower by a certain margin. This could be understood by the physical difference of the phase-B limb to phase A and C limbs in the 3-limb configuration (the magnetic reluctance is different for the middle limb as opposed to the two outer limbs). Furthermore, when a single phase is considered, it was observed that losses of the top and bottom windings of that phase inductor were different. Apart from the physical differences between the windings, one way to explain this would be to consider the possibility of winding-to-winding energy transfer between the top and bottom windings due to non-idealities in the system. In fact, it was observed that, for certain modulation indices and f_c values, the top winding showed negative values for the losses, suggesting energy transfer from the bottom winding. However, the possibility of phase-to-phase (or limb-to-limb) energy transfer is another possibility. It is worth allocating thought lines on this observation, as it aids to build a better theoretical model for the 3-limb core coupled inductor unit.

7.3 A Closing Remark

The DSP based approach allows a much simpler PWM solution, with a lower system cost, and provides better excitation for a 3-limb magnetic core. And this is the underlying principle of engineering: finding a simpler and low-cost solution to achieve a given task.

Appendix A

A Look on Inverter and PWM Theory

It is assumed that the reader has a basic understanding on operating principles of inverters and the concept of PWM. The intention of this appendix is to have a brief review on these, with emphasis on identifying some notions which are somewhat implicit in many text books. These points are very important, especially when it comes to practical implementation of PWM schemes, either in simulations or hardware experiments.

A.1 Basics of Inverters and Pulse Width Modulation

The most elementary part of an inverter system is an inverter leg, as shown in Fig. A.1. The midpoint o is usually not accessible in a practical system; but here, it is included to provide another perspective to the output voltage pattern. In standard inverters, the top switch (T_{X+}) and the bottom switch (T_{X-}) of a leg are switched in a complementary manner (here X refers to the phases A, B or C).[1] This is a mandatory requirement to avoid short circuiting of the dc-link. This concept can be implemented as shown in Fig. A.2 and could be directly adapted as the logical circuit unit for simulation (for instance, in MATLAB SIMULINK).

[1] Complementary means that, when one switch is ON , the other is OFF.

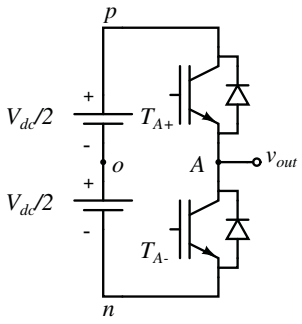


FIGURE A.1: A simple inverter leg

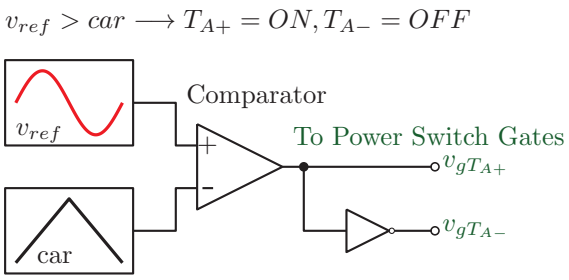


FIGURE A.2: Standard logic for switching a single leg

A *Reference Signal* (or *Modulating Signal*), v_{ref} $(-1 \leq v_{ref} \leq 1)$, is compared with a *Carrier Signal*, *car* $(-1 \leq car \leq 1)$ to generate the gate signals for the power switches. For a single inverter leg with bipolar PWM,[2] the corresponding logic would simply be:

$$v_{ref} > car \longrightarrow T_{A+} = ON, T_{A-} = OFF$$

$$v_{ref} < car \longrightarrow T_{A+} = OFF, T_{A-} = ON \tag{A.1}$$

The peak values of the carrier signal and the reference signal are denoted by $\hat{V}_{car}$ and $\hat{V}_{ref}$ respectively, and are usually equal to 1. Consider a power system with a fundamental frequency f_1 and an associated PWM control unit with a carrier frequency f_c. Sometimes the usage of the terms "*Carrier Frequency*", "*PWM Frequency*" and "*Switching Frequency*" is somewhat confusing. Therefore, a clear definition of the terms is important to avoid any confusion in future usages of the terms.

Carrier Frequency: The carrier frequency $(f_c = 1/T_c)$ is always the frequency of the triangular carrier wave.

Switching Frequency: The Switching Frequency $(f_{sw} = 1/T_{sw})$ and **PWM Frequency** are the same and refer to the final switching frequency of the power switches, and is not necessarily equal to the carrier frequency. If the power switch's ON time is t_{on} and the OFF time is t_{off}, then $T_{sw} = t_{on} + t_{off}$.

In the excellent book [4] by Ned Mohan et al., it is stated that carrier frequency is also known as the switching frequency. And as far as simple sinusoidal PWM is concerned, the

[2] For a standard single leg, the only possible PWM technique is *Bipolar PWM*. However, for topologies with more than one leg, other PWM techniques do exist; for instance, *Unipolar PWM* (explained in the following sections).

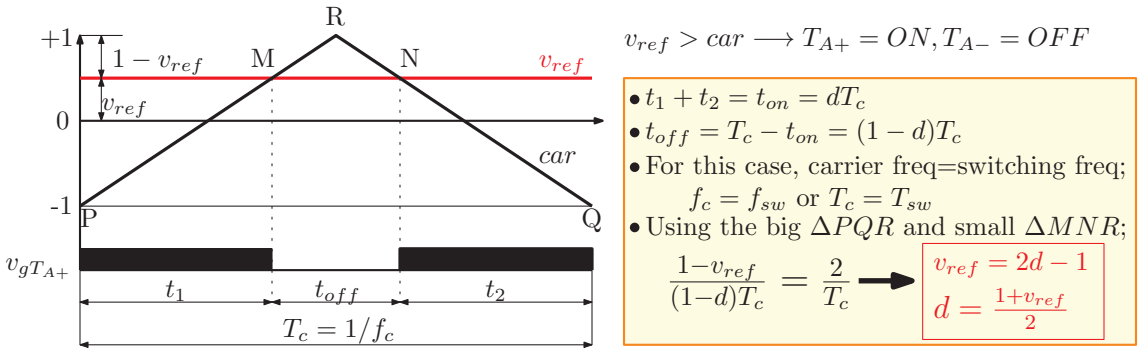


FIGURE A.3: The relationship between the duty and the reference signal values in sinusoidal PWM

carrier frequency and the switching frequency are indeed the same: i.e. $f_c = f_{sw}$. However, as the schemes get complex, the terminology got mixed up and ended up confusing the reader. The book [6] by Bin Wu addresses this issue (in its chapter 6 to be precise) and clearly states the relationship between f_c and f_{sw} for different multi-level PWM schemes. Therefore, it is advisable to keep the distinction between the two terms. For example, in the proposed MDPWM2 method in this work, carrier frequency and switching frequency are not the same (as a single power switch switches two times within a carrier period).

The ratio between the duration of the ON time of a power switch to the switching period ($= T_{sw} = 1/f_{sw}$) is defined as the *Duty*, d, and is generally expressed as a percentage ($0 \leq d \leq 1$).

$$d = \frac{t_{on}}{T_{sw}} = \frac{t_{on}}{t_{on} + t_{off}} \tag{A.2}$$

This is illustrated in Fig. A.3 for a simple sinusoidal PWM scheme. The figure shows a single carrier period, where the reference signal is approximately constant (assuming $f_c >> f_1$). In this case, the carrier and switching frequencies are the same, hence T_c and T_{sw} can be used interchangeably to define the duty ratio. However, it should be emphasized, that this relationship does not hold for complex schemes, and the new relationships should be derived according to the used scheme. The relationship between the duty and the reference signal is quite important when realizing PWM schemes in simulation (or in software, to be compiled into a hardware processor). For example, the PWM blocks in *VisSim Embedded* ^{TM} environment accept the duty value, whereas PWM blocks in *MATLAB SIMULINK* ^{TM} accept the direct reference signal. And when it comes to the hardware implementation of the schemes using *dSPACE*, for example when using the slave DSP three-phase PWM generation block of *DS1104 dSPACE system*, it requires duty ratios to be fed in.

There are two other terms that are quite important when it comes to generating voltages with variable magnitude and frequency in a dynamic sense.

1. **Modulation Index or Amplitude Modulation Ratio (m_a):** this is simply the normalized magnitude of the sinusoidal reference signal, v_{ref}.

$$m_a = \frac{\hat{V}_{ref}}{\hat{V}_{car}} \tag{A.3}$$

The value of m_a is between 0 and 1 which makes certain that v_{ref} always varies between $+1$ and -1 (such that it lies within the carrier magnitude).

$$v_{ref} = m_a sin(\omega_1 t) \tag{A.4}$$

Here, $\omega_1 = 2\pi f_1$.

2. **Frequency Modulation Ratio (m_f):** this is defined as the ratio between the fundamental reference frequency and the carrier frequency.

$$m_f = f_c / f_1 \tag{A.5}$$

This is also equal to f_{sw}/f_1 for standard sinusoidal PWM, where $f_c = f_{sw}$.

The underlying circuit theory behind this operation is best understood by observing the resulting voltage waveforms. Fig. A.4 underlies the core concept behind pulse width modulation of an inverter leg and delivering the required voltage output. Note that, [4] offers an excellent guide into basic operation of inverter systems, and [6] provides an in depth analysis of various PWM schemes. The reader is encouraged to refer to these text books to cover elementary theory, should the following sections prove to be far advanced.

The core concept behind pulse width modulation is *Time Averaging* that can be summarized in the following sentence:

> *The average value of the PWM output voltage during a single switching cycle T_{sw} is equal to the average value of the fundamental sinusoidal voltage signal over the same period T_{sw}.*

And as it happens, comparing the reference signal (which is a normalized version of the fundamental sinusoid that we want to synthesize) with a carrier signal just allows us to do

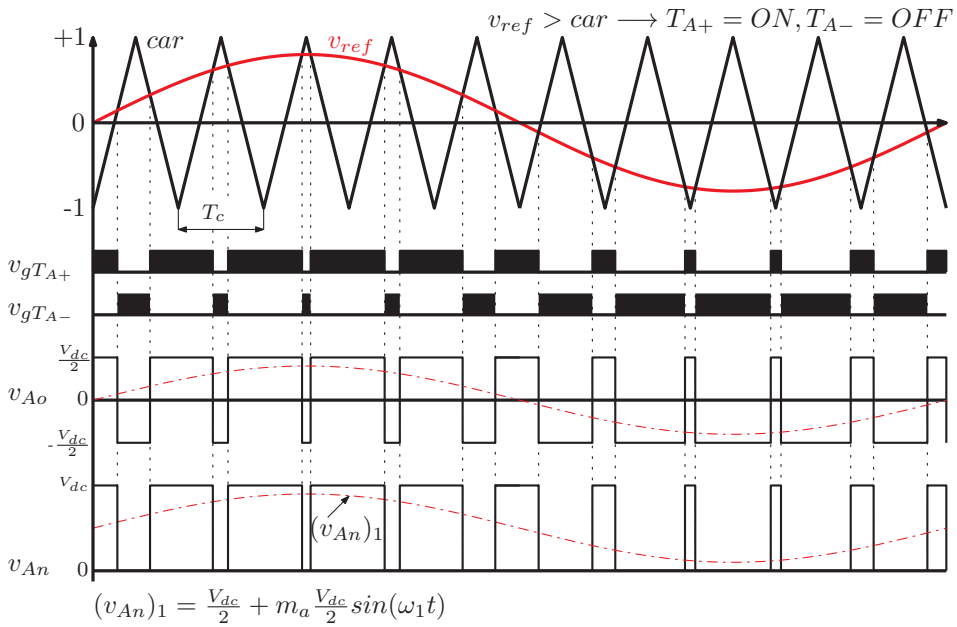


FIGURE A.4: The simplest PWM scheme

this. Fig. A.4 shows that the resulting output voltage pattern has only two levels: $+V_{dc}$ and 0 (if v_{An} is considered) or $+V_{dc}/2$ and $-V_{dc}/2$ (if v_{Ao} is considered).[3] Hence, the inverter is said to be a *2-level inverter* [6]. The fundamental of the output voltage is given by:

$$(v_{An})_1 = v_{ref}\frac{V_{dc}}{2} = m_a sin(\omega_1 t)\frac{V_{dc}}{2} \tag{A.6}$$

and the peak value of the fundamental output voltage is given by:

$$(\hat{V}_{An})_1 = \hat{V}_{ref}\frac{V_{dc}}{2} = m_a\frac{V_{dc}}{2} \tag{A.7}$$

A.2 The Full-Bridge Converter (H-Bridge Converter) and the Concept of Bipolar and Unipolar Switching

Compared to the single leg inverter, the full-fridge converter offers more flexibility in controlling the output PWM voltage pattern. The basic setup is illustrated in Fig. A.5 where the output voltage is v_{out} $(= v_{AB})$. And this topology aids to address quite a few dubious

[3] It is a matter of personal preference whether to consider v_{An} or v_{Ao} to refer to the output voltage for a single leg.

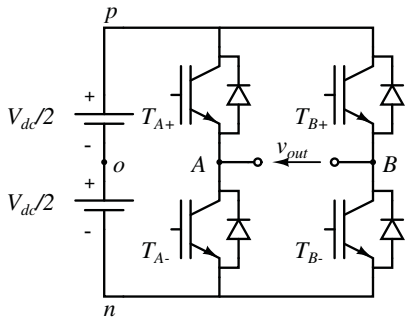


FIGURE A.5: The full-bridge converter

points that one might trap into while trying to understand the concepts of unipolar and bipolar PWM schemes. Note that the full-bridge converter can be operated using either of these schemes.

A.2.1 Bipolar PWM

Bipolar PWM simply means that the output voltage swings between only two levels of voltages (between $+V_{dc}$ and $-V_{dc}$, resulting in a jump of magnitude $2V_{dc}$ when transiting between two levels). The output voltage waveform of the full bridge converter in this case is similar to the single leg output voltage shown in Fig. A.4. The switching logic for this case is illustrated in Fig. A.6 and can be expressed as follows:

$$v_{ref} > car \longrightarrow T_{A+}, T_{B-} = ON, T_{B+}, T_{A-} = OFF$$

$$v_{ref} < car \longrightarrow T_{A+}, T_{B-} = OFF, T_{B+}, T_{A-} = ON \tag{A.8}$$

As in the single leg case, two switches on a same leg are switched complementarily (T_{A+} and T_{A-} are a complementary pair as well as the pair $T_{B+}$and T_{B-}). However, it

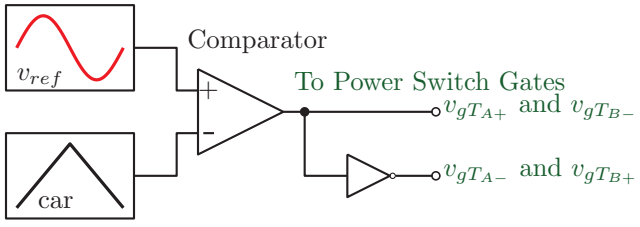


FIGURE A.6: Full-bridge inverter: logic circuit for generating bipolar PWM

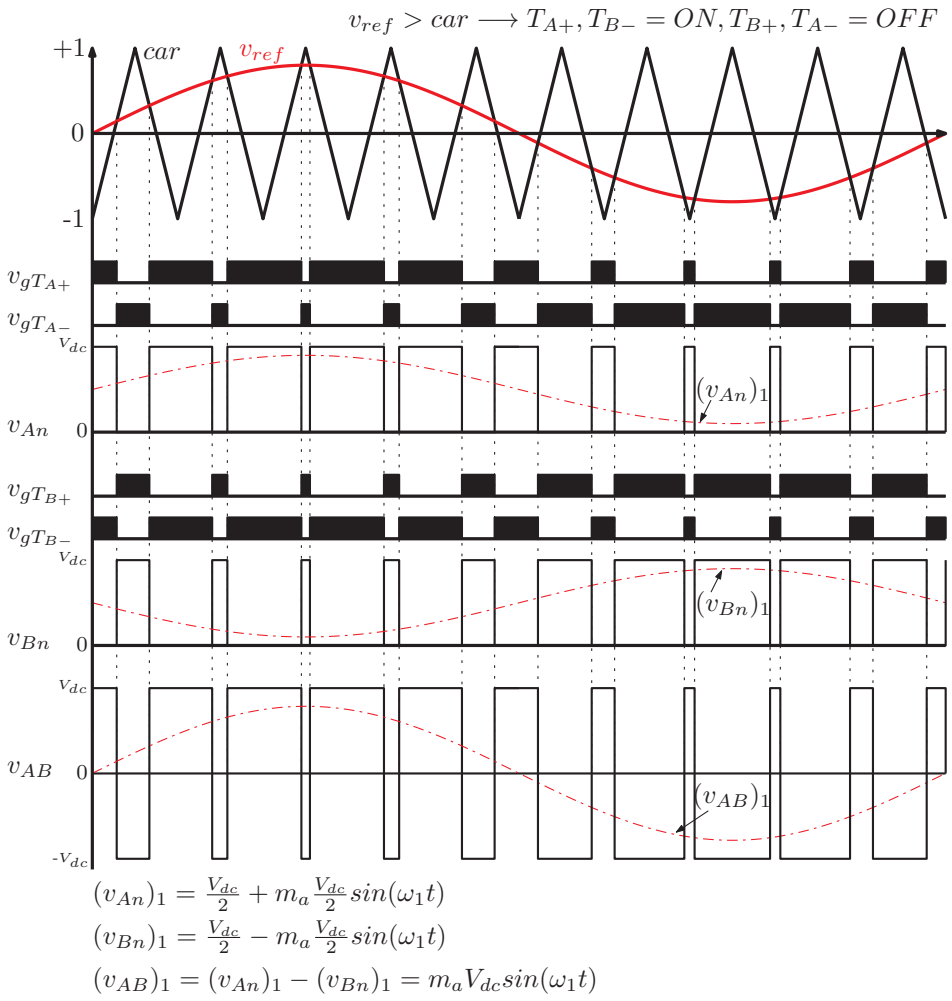


FIGURE A.7: Full-bridge inverter: output voltage pattern for bipolar PWM

is interesting to note that T_{A+} and T_{B+} are also complementary to each other (as well as T_{A-} and T_{B-}). The resulting waveforms illustrating the gate signals and relevant output voltages are shown in Fig. A.7. The fundamental output voltage expressions are again similar to the single leg case, but with doubled magnitude ($V_{dc}/2$ replaced by V_{dc}).

$$(v_{AB})_1 = v_{ref} V_{dc} = m_a sin(\omega_1 t) V_{dc} \tag{A.9}$$

And the peak value of the fundamental output voltage is given by:

$$(\hat{V}_{AB})_1 = \hat{V}_{ref} V_{dc} = m_a V_{dc} \tag{A.10}$$

A.2.2 Uniploar PWM

Unipolar PWM is the preferred choice over the bipolar case as it introduces an extra voltage level in the output voltage pattern of v_{AB}. During the first half of the fundamental period, v_{AB} switches between $+V_{dc}$ and 0; and during the second half, the voltage switches between $-V_{dc}$ and 0. Therefore, the jumps are always of magnitude V_{dc} in contrast to the bipolar case, where the jumps have a magnitude of $2V_{dc}$.

This is achieved by controlling the two legs separately. And it is really important to note that there are two carrier based methods to get the same unipolar output voltage. This is where sometimes one might get confused in determining the correct logic; the two methods use two different logical schemes, although they result in the same output voltage pattern in the end.

A.2.2.1 Method 1: Using Two References and One Carrier Signal

In this approach, the switching signals for phase-A switches are determined by the same logic that is used for the single leg case (see Appendix A.1).

$$v_{ref} > car \longrightarrow T_{A+} = ON, T_{A-} = OFF$$
$$v_{ref} < car \longrightarrow T_{A+} = OFF, T_{A-} = ON \tag{A.11}$$

But, to generate the switching signals for phase-B switches, an additional reference signal ($-v_{ref}$) is introduced: this is simply obtained by multiplying v_{ref} by -1. And, this

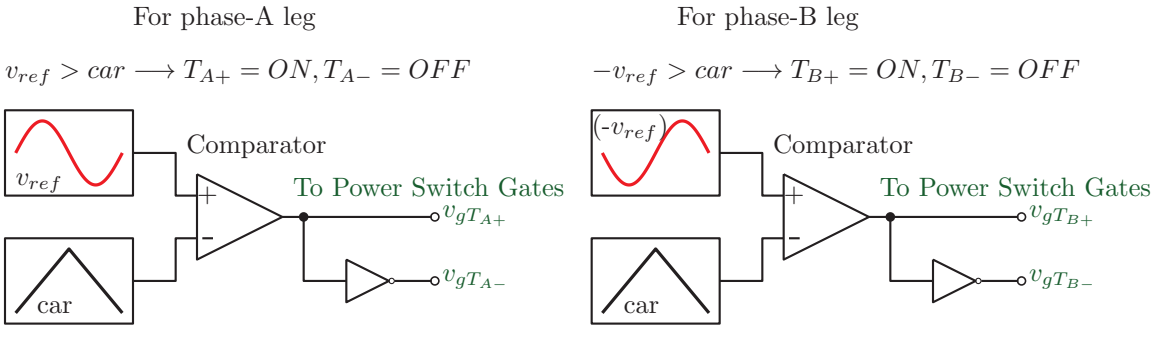


FIGURE A.8: Full-bridge inverter: logic circuit for generating unipolar PWM with two reference signals

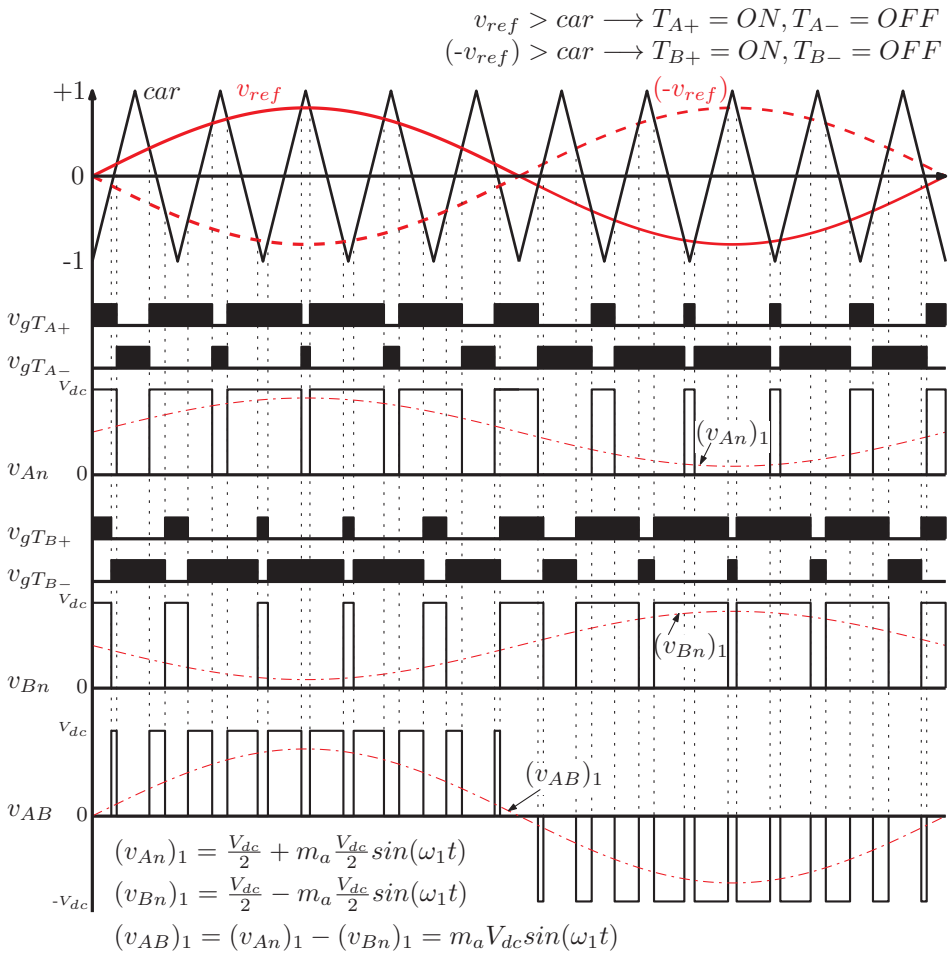


FIGURE A.9: Full-bridge inverter: output voltage pattern for unipolar PWM with two reference signals

reference signal is compared with the same carrier signal (with the same logic) as expressed below:

$$(-v_{ref}) > car \longrightarrow T_{B+} = ON, T_{B-} = OFF$$

$$(-v_{ref}) < car \longrightarrow T_{B+} = OFF, T_{B-} = ON \tag{A.12}$$

The corresponding logic circuit and the resulting gate signals and output voltage patterns are shown in Fig. A.8 and Fig. A.9 respectively.

A.2.2.2 Method 2: Using Two Carriers and One Reference Signal

Also in this approach, the logic generation for phase-A switches is unchanged.

$$v_{ref} > car \longrightarrow T_{A+} = ON, T_{A-} = OFF$$
$$v_{ref} < car \longrightarrow T_{A+} = OFF, T_{A-} = ON \tag{A.13}$$

However, for the two phase-B switches, a different logic is used with introducing an additional carrier which is phase shifted by 180° to the standard carrier signal *car*. This way, the same reference signal which is used for the phase-A switching can be used to generate switching signals for phase B, but with one important distinction: the comparison logic is swapped for phase B as shown in Fig. A.10.

$$v_{ref} < (-car) \longrightarrow T_{B+} = ON, T_{B-} = OFF$$
$$v_{ref} > (-car) \longrightarrow T_{B+} = OFF, T_{B-} = ON \tag{A.14}$$

The reason of the change in the comparator logic is quite obvious: if both sides of Eq. (A.14) is multiplied by -1, then we arrive at the same switching logic that is used for method 1. The corresponding gate signals and output voltage waveforms are illustrated in Fig. A.11. A comparison with Fig. A.9 confirms that the output voltage patterns produced by two methods are identical.

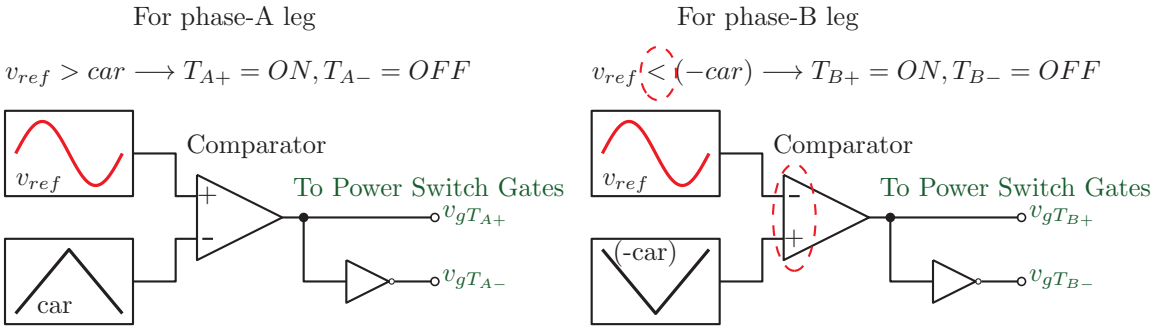


FIGURE A.10: Full-bridge inverter: logic circuit for generating unipolar PWM with two carrier signals

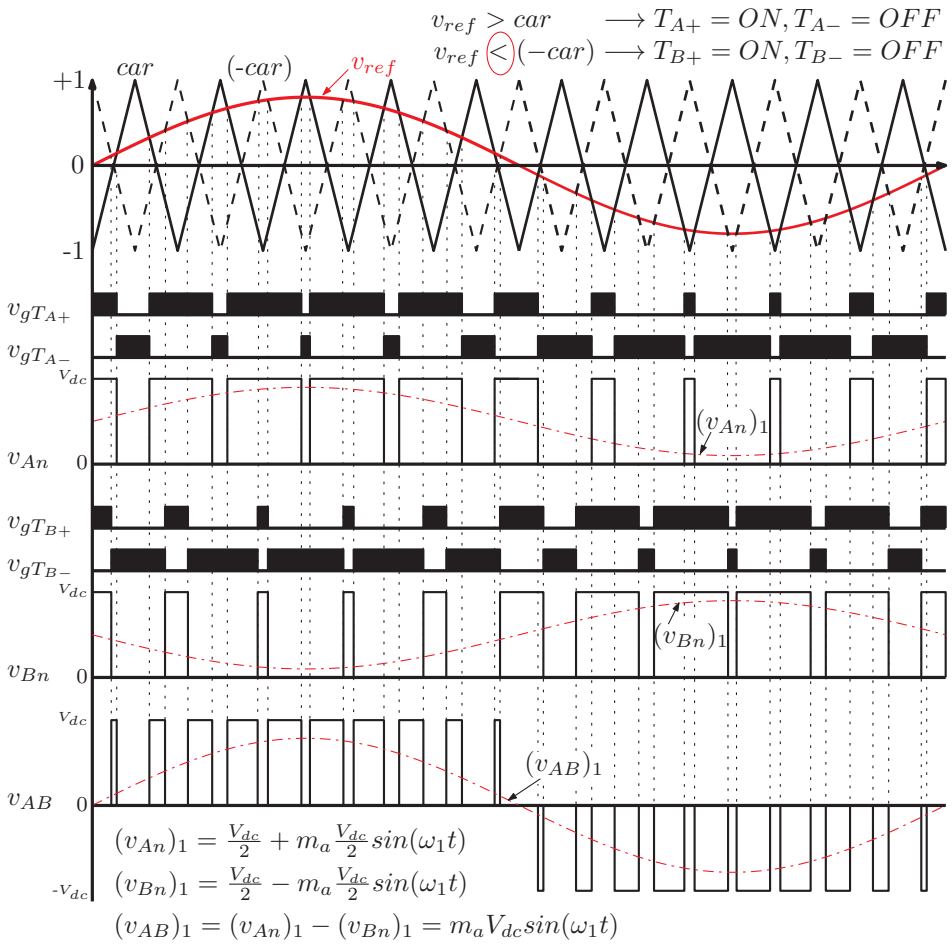


FIGURE A.11: Full-bridge inverter: output voltage pattern for unipolar PWM with two carrier signals

A.2.2.3 Output Voltage Pattern with Unipolar PWM

The output voltage expression for the unipolar PWM is independent of the two logic schemes discussed above (both methods result in the same output voltage pattern). The fundamental output voltage expressions are similar to that of the bipolar case.

$$(v_{AB})_1 = v_{ref} V_{dc} = m_a sin(\omega_1 t) V_{dc} \tag{A.15}$$

and the peak of the fundamental output voltage is given by;

$$(\hat{V}_{AB})_1 = \hat{V}_{ref} V_{dc} = m_a V_{dc} \tag{A.16}$$

The difference between the bipolar and the unipolar schemes becomes apparent when the output current waveforms are observed.[4] The unipolar case provides a significantly reduced ripple for the output current [4]. In other words, the unipolar PWM method introduces less switching harmonics to the system.

A.3 Interleaved PWM

Interleaved Switching is commonly known in parallel inverter systems for ripple cancellation. However, the concept of interleaving is an essential component in many complex switching schemes. Consider a single phase of a parallel inverter system as shown in Fig. 3.1 in Chapter 3: the configuration is similar to that of a simple full-bridge converter. The only difference is that in the parallel inverter case, the leg outputs are usually connected to output inductors, which ultimately give a single output node A as shown in Fig. 3.1 (as opposed to the two output nodes of the full bridge setup in Appendix A.2).

The logic circuit for the interleaved switching of the top and bottom legs of phase A is depicted in Fig. A.12. The modulation logic for the top leg of the parallel inverter phase

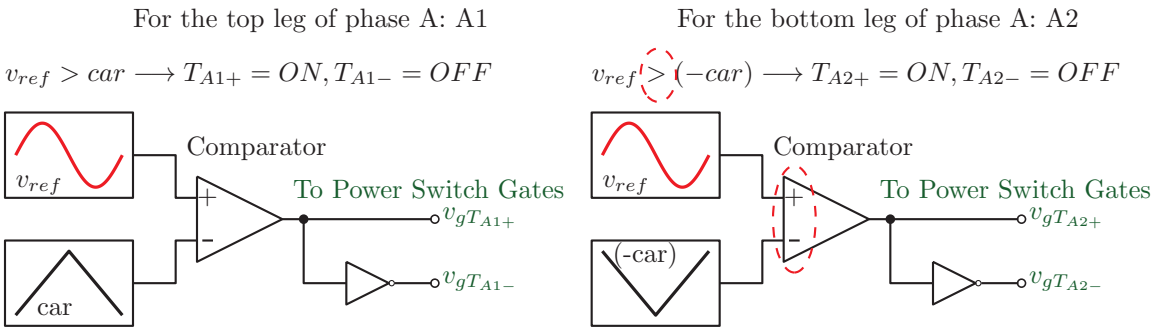


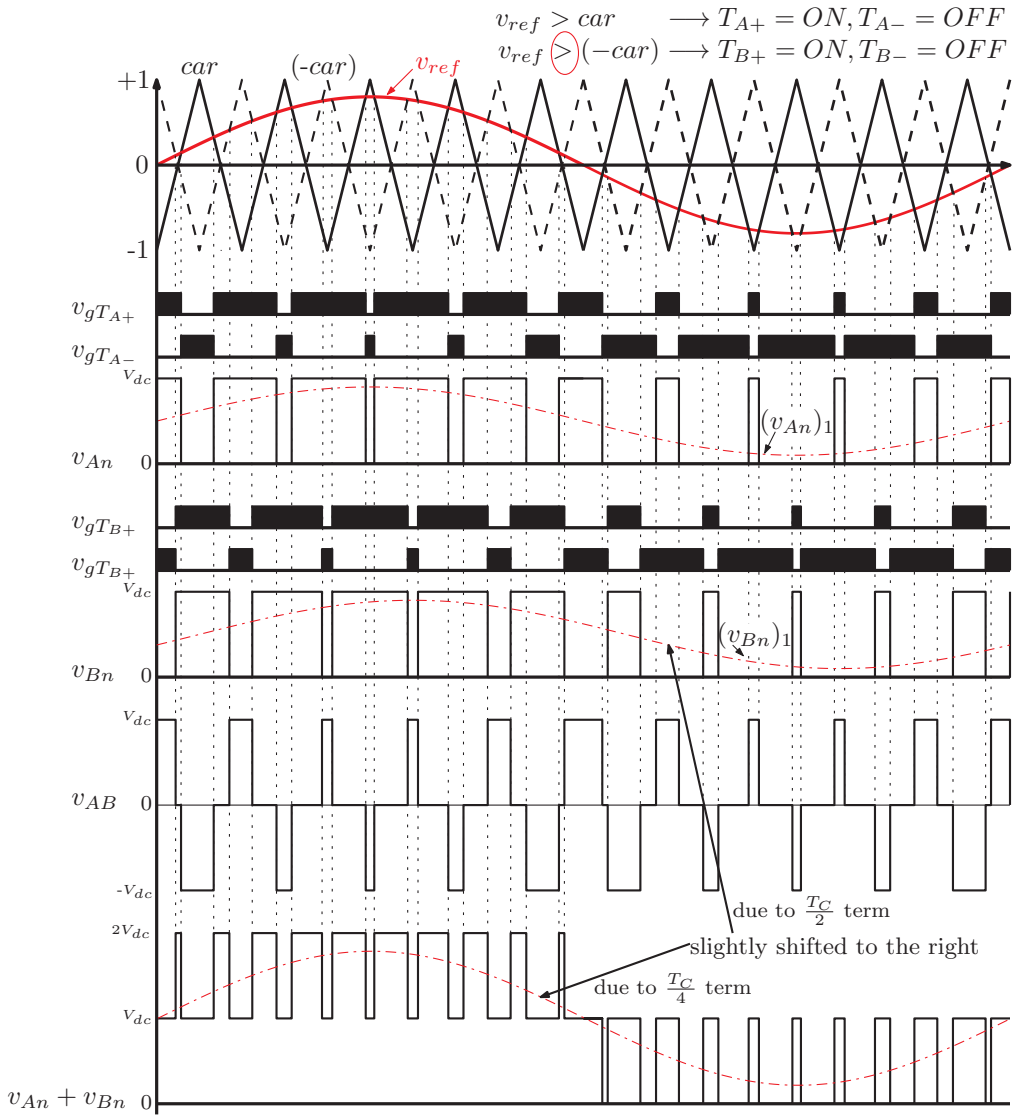
FIGURE A.12: Parallel inverter legs: logic circuit for generating interleaved switching for the two legs in phase A

leg is similar to the scheme that is used for the phase-A leg in a full-bridge converter. Now, consider the switching logic for the bottom leg of the parallel inverter case in contrast to the phase B-leg in the full-bridge converter: both use v_{ref} and $-car$ for comparator inputs, but with comparator's + and - signs swapped. The logic is quite simple, but sometimes

[4] Refer to [4] for well documented analyses on the output current ripple and the harmonics.

it is easier to get confused with such elementary differences, and end up using the wrong scheme for a given topology.

The switching signals and relevant output voltage waveforms for interleaved switching are shown in Fig. A.13.



$$(v_{An})_1 = \frac{V_{dc}}{2} + m_a \frac{V_{dc}}{2} sin(\omega_1 t)$$
$$(v_{Bn})_1 = \frac{V_{dc}}{2} + m_a \frac{V_{dc}}{2} sin(\omega_1 t - \frac{T_C}{2})$$
$$(v_{AB})_1 = m_a V_{dc} cos(\omega_1 t - \frac{T_C}{4}) sin(\frac{T_C}{4}) \approx 0)$$
$$(v_{An})_1 + (v_{Bn})_1 = V_{dc} + m_a V_{dc} sin(\omega_1 t - \frac{T_C}{4}) cos(\frac{T_C}{4}) \approx V_{dc} + m_a V_{dc} sin(\omega_1 t)$$

FIGURE A.13: Basic interleaved PWM: for a standard parallel inverter phase leg

A.4 The Standard Three-Phase Inverter

The essentials of generating a PWM voltage at the output of a single inverter leg has been established in the previous sections. A standard three-phase inverter is a collection of three inverter legs (shown in Fig. A.14) and relies upon the PWM strategies discussed above for its standard operation.

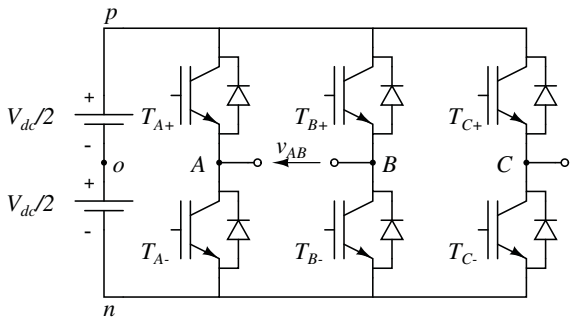


FIGURE A.14: The standard three-phase inverter

It makes no sense to define a bipolar scheme for a three-phase inverter as it has three legs. Therefore, the standard PWM scheme essentially is an extension of the unipolar PWM scheme used for the full-bridge converter with an additional phase, C. The PWM scheme can be implemented using two methods:

1. With three reference signals: here, three reference signals of fundamental frequency f_1 (ref_A, ref_B and ref_C) which are dispersed by $120_\circ$ to each other are compared with a single carrier signal.
2. With three carrier signals: in this case, three carrier signals which are dispersed by $120_\circ$ to each other are compared with a single reference signal (ex: ref_A) to generate the gate signals for the each leg.

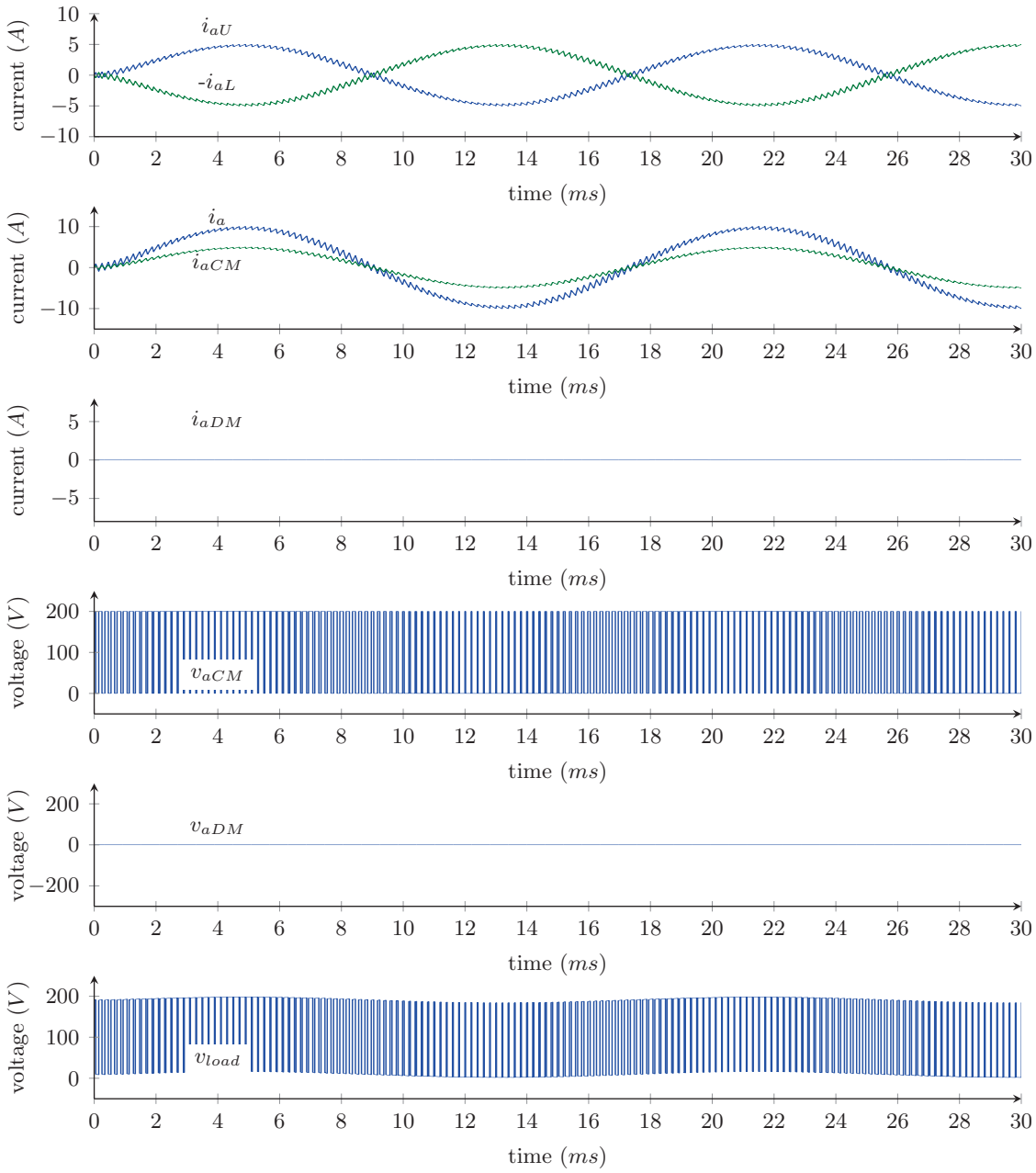
Note that, for all the standard inverter systems discussed in this appendix, the two switches in a single leg are always switched in a complementary manner to avoid short circuiting of the dc-link. However, there are topologies where this is not mandatory (for instance the coupled inductor inverter topology).

A.5 Simulation Results for a CII Leg

The following pages contain some simulation results with reference to the material presented in Chapter 3. The simulated systems are:

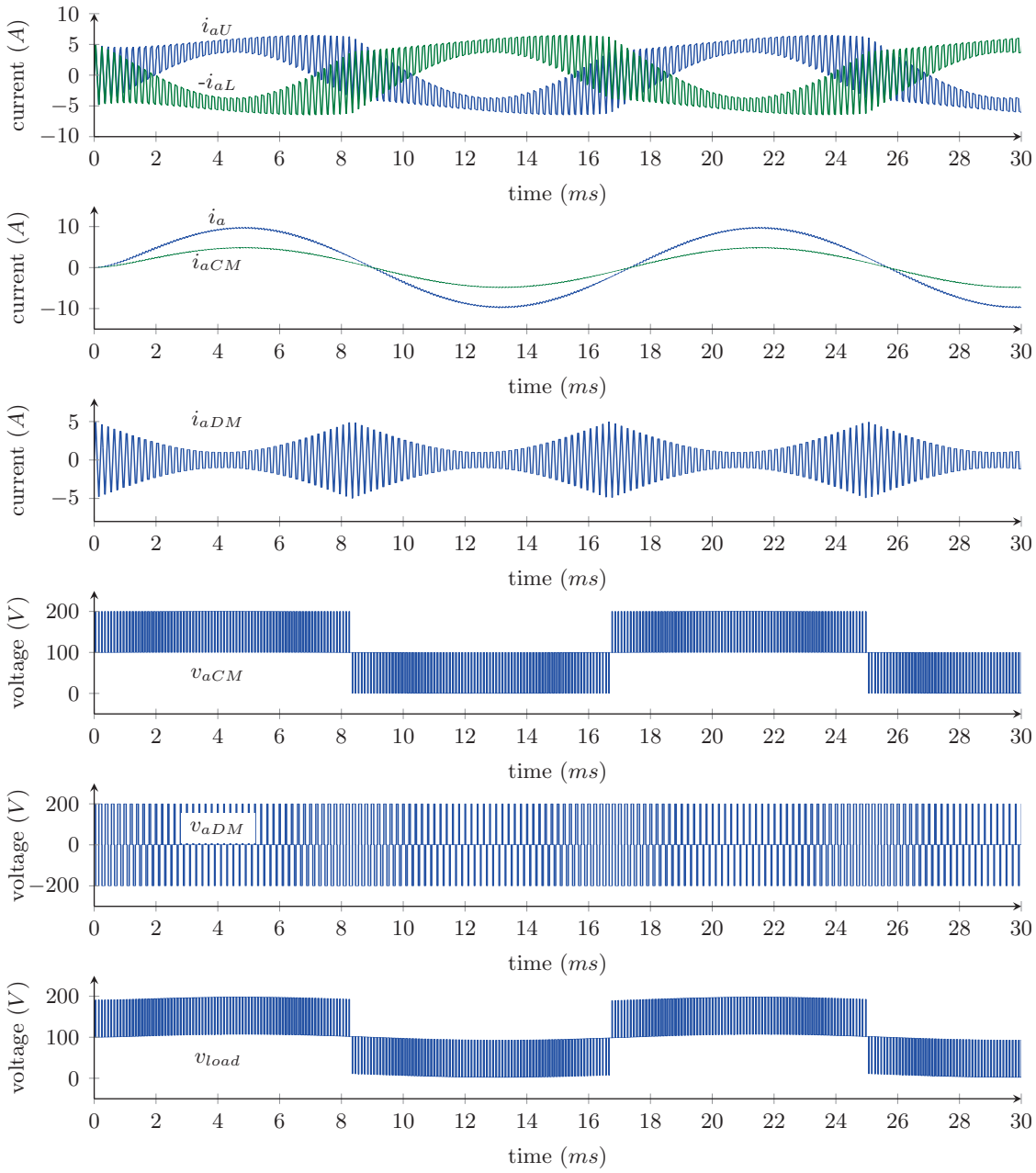
1. A single phase of a non-coupled parallel inverter system with basic (non-interleaved) switching.
2. A single phase of a non-coupled parallel inverter system with standard interleaved switching.
3. A single phase of a coupled parallel inverter system with standard interleaved switching.
4. A single phase coupled 6-CII leg with standard switching.

The simulations were carried out using MATLAB SIMULINK simulation software (SimPowerSystems).



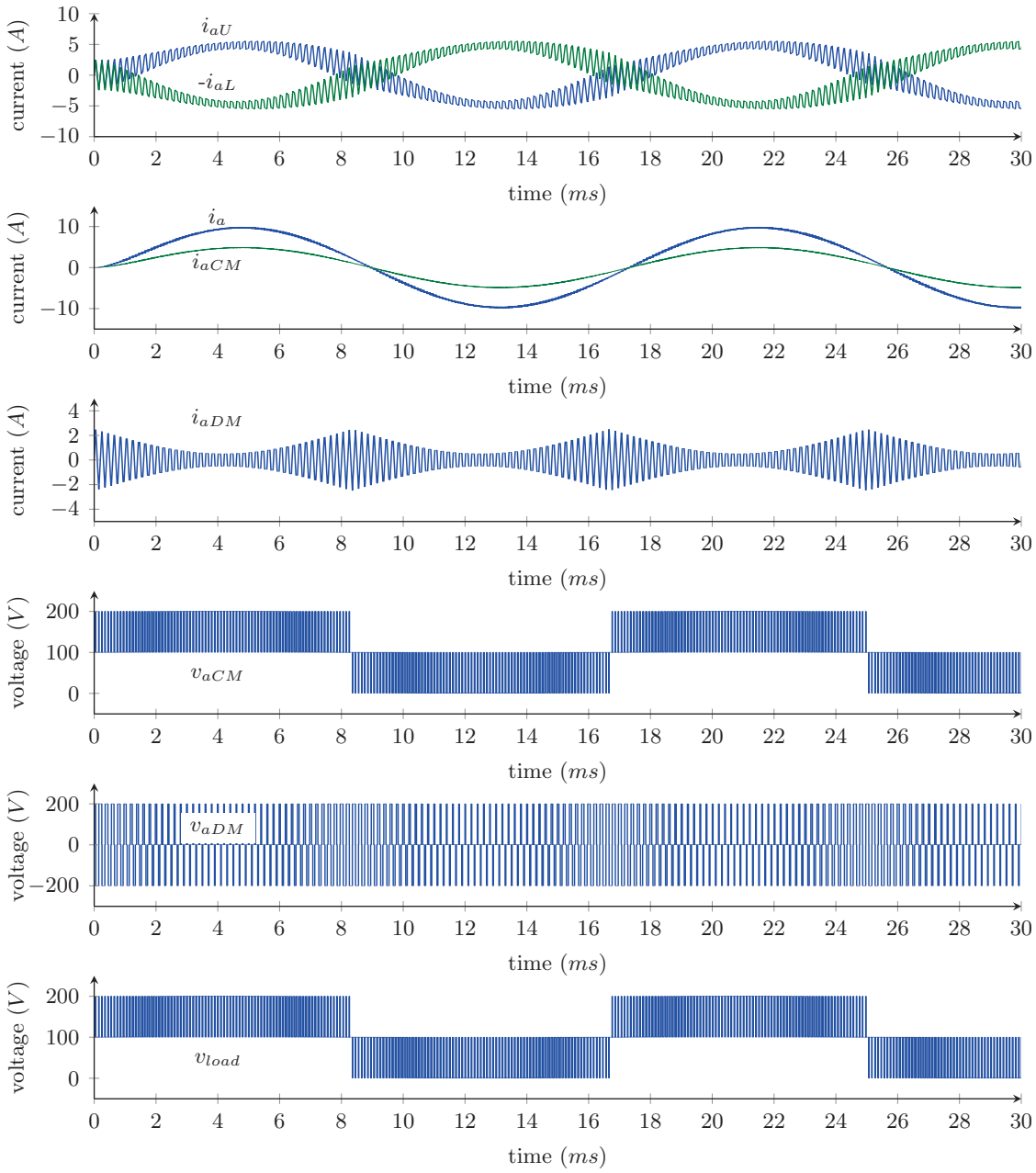
System Parameters: dc-link voltage (V_{dc}) =200 V, fundamental frequency (f_1) =60 Hz, carrier frequency (f_c) = 5 kHz, self inductance of a winding (L) = 1 mH, mutual inductance of the two windings (M) = 0, load resistance (R_{load}) = 8 Ω, load inductance (L_{load}) = 5 mH, simulation time step = 1 μs

FIGURE A.15: Simulation results for a single phase of a non-coupled parallel inverter system with basic (non-interleaved) switching



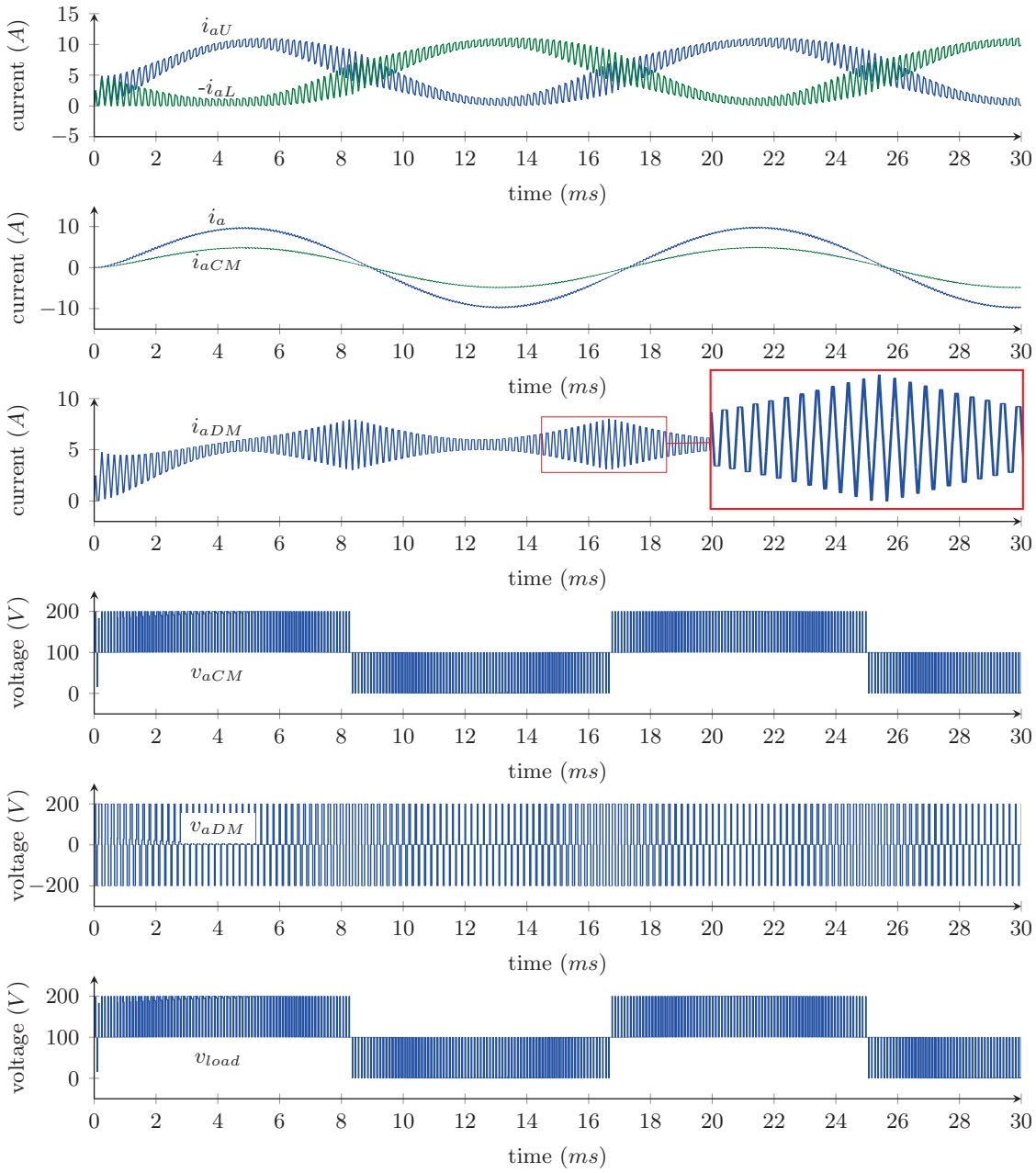
System Parameters: dc-link voltage (V_{dc}) =200 V, fundamental frequency (f_1) =60 Hz, carrier frequency (f_c) = 5 kHz, self inductance of a winding (L) = 1 mH, mutual inductance of the two windings (M) = 0, load resistance (R_{load}) = 8 Ω, load inductance (L_{load}) = 5 mH, simulation time step = 1 μs

FIGURE A.16: Simulation results for a single phase of a non-coupled parallel inverter system with standard interleaved switching



System Parameters: dc-link voltage (V_{dc}) =200 V, fundamental frequency (f_1) =60 Hz, carrier frequency (f_c) = 5 kHz, self inductance of a winding (L) = 1 mH, mutual inductance of the two windings (M) = 0.9999 mH, load resistance (R_{load}) = 8 Ω, load inductance (L_{load}) = 5 mH, simulation time step = 1 μs

FIGURE A.17: Simulation results for a single phase of a coupled parallel inverter system with standard interleaved switching



System Parameters: dc-link voltage (V_{dc}) =200 V, fundamental frequency (f_1) =60 Hz, carrier frequency (f_c) = 5 kHz, self inductance of a winding (L) = 1 mH, mutual inductance of the two windings (M) = 0.9999 mH, load resistance (R_{load}) = 8 Ω, load inductance (L_{load}) = 5 mH, simulation time step = 1 μs

FIGURE A.18: Simulation results for a single phase of a coupled 6-CII system with standard interleaved switching

Appendix B

A Note on Space Vector Modulation

General Relativity (or rather Special Relativity) states that nothing can move faster than the speed of light. But more often, it is not spoken explicitly that the space itself can expand or shrink faster than the speed of light. Therefore, the correct way to express the idea of speed limit is like this: nothing can move through a pre-existing space at a speed faster than the speed of light. The universe is expanding as we speak. But, it should be made clear that the fabric of the universe is what that expands, it is not that that galaxies are moving away from each other while the fabric of universe is stationary.

Luckily, we wouldn't have to be concerned about the speed of light as far as *Space Vectors* are concerned. And, unlike the universe and galaxies, in space vectors we have stationary a frame (where the vectors move). Establishing a clear connection between the vector representation and the actual three-phase waveforms is quite important. This is vital in mapping switching states in carrier based PWM solutions into the space vector domain.

B.1 A Brief on Arriving at Space Vectors

The space vectors are simply a mathematical tool which allows to picture a three-phase system in a different, yet an effective way. Of course, the frame can rotate as well, but

that is if we were to move in to the realm of *Space Phasors* [7]. As Chapter 2 has briefly introduced the concept of space vector modulation, here the concentration is on specific topics that complements the report material.

The ultimate intention of a PWM process is to provide a sinusoidal waveform of adjustable frequency and magnitude (more specifically, the fundamental voltage required by the load), as the voltage available from the grid-mains is of fixed frequency and magnitude and offers no variability. Furthermore, with power switches switching at higher frequencies (in contrast to the fundamental), the switching harmonics are moved to a higher range in the frequency spectrum. This allows use of smaller filters at the inverter outputs to smoothen the output waveforms.

Depending upon the PWM technique, the number of switching transitions per carrier cycle may vary. An increased number of switchings per cycle causes increased switching losses, and may compromise the system efficiency. In PWM techniques like sinusoidal carrier based PWM and selected harmonic elimination, the PWM patterns are calculated per phase, irrespective of the switchings of other phases [26]. The difference in the space vector approach is that it considers the effect of all the three phases when generating the switching signals for the switches of a particular phase. It is important to understand the position of space vectors on a 360° *Space Phasor Diagram*, and how to map this position with the variation of the actual three-phase voltage signals.

But, before moving on to that, a small distinction in the definitions of space phasors and space vectors should be clarified. The terms "*Space Phasors*" and "*Space Vectors*" are often used interchangeably, and it could be confusing to the first time learner. In simply put, space phasors are more of a general description of the conventional phasors and refer to a three-phase system. And, depending upon the chosen reference frame, the operation of the three-phase system offers different perspectives of the same system. Primarily, the concept of space phasors are used in control of three-phase power systems [7]. On the other hand, the concept space vectors is more often used at the end product of the control system, the modulation of the power switches. *Space Vector Modulation* refers to a modulation method which actually follows the original concept of space phasors. Simply put, a space vector can be treated as a particular snapshot of a rotating space phasor on the *Stationary Reference* (or $\alpha - \beta$) frame [7]. An in depth description of these concepts is out of the scope of this report; however, some excellent reads on these concepts are suggested as follows to the

interests of the curious reader: the book *Voltage-Sourced Converters in Power Systems* [7] by Yazdani and R.Iravani presents an excellent explanation on space phasors and three-phase control systems, whereas *High-Power Converters and AC Drives* [6] by Bin Wu offers a good introduction to space vector based modulation schemes.

B.2 Space Vector Modulation: Basic System Representation

The analysis starts with a balanced three phase system as illustrated in Fig. B.1, where the z is the load neutral point. For a balanced three-phase system, the sum of line-to-line voltages (as well as the sum of phase voltages) equals to zero:

$$v_{AB} + v_{BC} + v_{CA} = 0 \tag{B.1}$$

$$v_{Az} + v_{Bz} + v_{Cz} = 0 \tag{B.2}$$

Now, the line-to-line voltage v_{AB} can be described in terms of the switching functions $S(A)$ and $S(B)$ as described in Table B.1:

$$v_{AB} = v_{An} - v_{Bn} \Rightarrow v_{AB} = V_{dc}.S(A) - V_{dc}.S(B) \Rightarrow v_{AB} = V_{dc}[S(A) - S(B)]$$

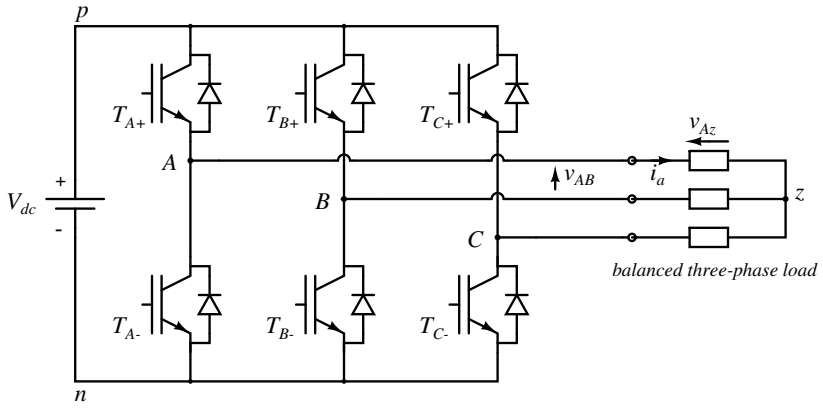


FIGURE B.1: A standard three-phase inverter with a three-phase y-connected load

TABLE B.1: Switching States for the Three Phases

Switching Function	Value	Condition
$S(A)$	0	$T_{A+} = OFF$ and $T_{A-} = ON$
	1	$T_{A+} = ON$ and $T_{A-} = OFF$
$S(B)$	0	$T_{B+} = OFF$ and $T_{B-} = ON$
	1	$T_{B+} = ON$ and $T_{B-} = OFF$
$S(C)$	0	$T_{C+} = OFF$ and $T_{C-} = ON$
	1	$T_{C+} = ON$ and $T_{C-} = OFF$

Following the same approach, the expressions for the line-to-line voltages of the three phases can be written as:

$$v_{AB} = V_{dc}[S(A) - S(B)] \tag{B.3}$$

$$v_{BC} = V_{dc}[S(B) - S(C)] \tag{B.4}$$

$$v_{CA} = V_{dc}[S(C) - S(A)] \tag{B.5}$$

The trick of illustrating the space vectors alongside with the actual three-phase sinusoidal voltages is based on expressing the phase voltages with respect to the load neutral, z (see Fig. B.1). The line-to-line voltages can be expressed in terms of line-to-neutral voltages as follows:

$$v_{AB} = v_{Az} - v_{Bz} \tag{B.6}$$

$$v_{BC} = v_{Bz} - v_{Cz} \tag{B.7}$$

$$v_{CA} = v_{Cz} - v_{Az} \tag{B.8}$$

Now using Eq. (B.2) and Eqs. (B.6)-(B.8), the line-to-neutral voltages can be expressed as:

$$v_{Az} = \frac{1}{3}(v_{AB} - v_{CA}) \tag{B.9}$$

$$v_{Bz} = \frac{1}{3}(v_{BC} - v_{AB}) \tag{B.10}$$

$$v_{Cz} = \frac{1}{3}(v_{CA} - v_{BC}) \tag{B.11}$$

And finally, using Eqs. (B.3)-(B.5) and Eqs. (B.9)-(B.11), the line-to-neutral voltages can be expressed in terms of the switching functions as follows:

$$v_{Az} = \frac{V_{dc}}{3}[2S(A) - S(B) - S(C)] \tag{B.12}$$

$$v_{Bz} = \frac{V_{dc}}{3}[2S(B) - S(C) - S(A)] \tag{B.13}$$

$$v_{Cz} = \frac{V_{dc}}{3}[2S(C) - S(A) - S(B)] \tag{B.14}$$

Note that there are two possible switching states for each phase; for example, $S(A) = 1$ and $S(A) = 0$ for phase A. Therefore, for the combined three phases of the system, there are 8 ($2 \times 2 \times 2 = 8$) possible combinations of states. This is tabulated in Table B.2. The eight vectors consist of two *Zero Vectors* and six *Active Vectors* [6] and can be mapped to a phasor map.

Since v_{Az}, v_{Bz} and v_{Cz} are also balanced three-phase quantities, a *Space Phasor* $\vec{V_s}$ can be defined as follows (refer to [7] for basic definition of space phasor representation of a three-phase system):

$$\vec{V_s} = \frac{2}{3}[v_{Az(t)}e^{j0} + v_{Bz(t)}e^{j\frac{2\pi}{3}} + v_{Cz(t)}e^{j\frac{4\pi}{3}}] \tag{B.15}$$

Now, substituting the values for v_{Az}, v_{Bz} and v_{Cz} for state 1 (refer to Eqs. (B.12)-(B.14) and $\vec{V_1}$ in Table B.1):

$$\begin{aligned} \vec{V_{s=1}} &= \frac{2}{3}[\frac{2}{3}V_{dc}e^{j0} - \frac{1}{3}V_{dc}e^{j\frac{2\pi}{3}} - \frac{1}{3}V_{dc}e^{j\frac{4\pi}{3}}] \\ \vec{V_1} &= \frac{2}{3}V_{dc}e^{j0} \end{aligned} \tag{B.16}$$

Similarly, for all the six active vectors, a general expression can be given as:

$$\vec{V_s} = \frac{2}{3}V_{dc}e^{j(s-1)\frac{\pi}{3}} \qquad s = 1, 2, 3, 4, 5, 6 \tag{B.17}$$

The zero vectors, as their name imply, makes all three line-to-line voltages to be zero; whereas, the active vectors produce non-zero voltages in all three phases. The corresponding line-to-neutral voltages of the eight vectors are also tabulated in Table B.2. This relationship

TABLE B.2: Eight Space Vectors with Corresponding Switching States and Load-to-Neutral Voltages

Vector Type	Vector	Switching Function Value ([A B C])	v_{Az}	v_{Bz}	v_{Cz}
Zero	$\vec{V}_0$	[0 0 0]	0	0	0
	$\vec{V}_7$	[1 1 1]	0	0	0
Active	$\vec{V}_1$	[1 0 0]	$+\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$
	$\vec{V}_2$	[1 1 0]	$+\frac{1}{3}V_{dc}$	$+\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$
	$\vec{V}_3$	[0 1 0]	$-\frac{1}{3}V_{dc}$	$+\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$
	$\vec{V}_4$	[0 1 1]	$-\frac{2}{3}V_{dc}$	$+\frac{1}{3}V_{dc}$	$+\frac{1}{3}V_{dc}$
	$\vec{V}_5$	[0 0 1]	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$+\frac{2}{3}V_{dc}$
	$\vec{V}_6$	[1 0 1]	$+\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$+\frac{1}{3}V_{dc}$

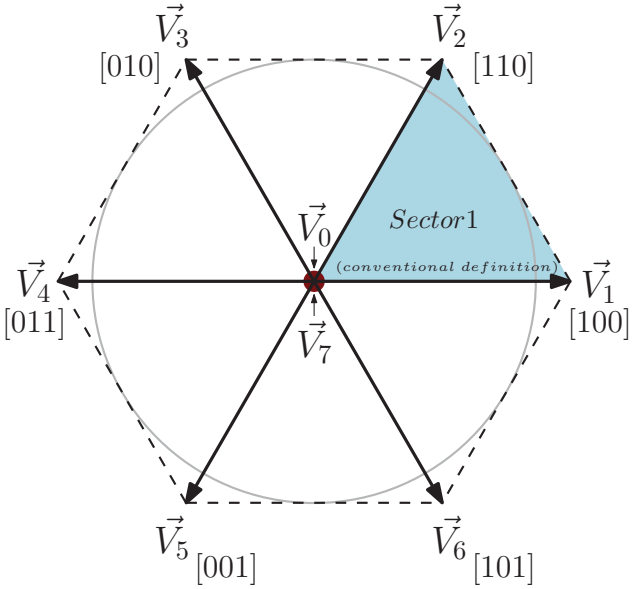


FIGURE B.2: Space vectors for a standard three-phase inverter

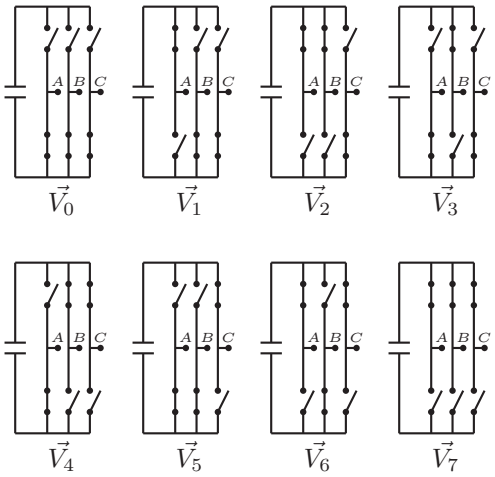


FIGURE B.3: Corresponding switching states in the inverter

is what allows the mapping of the vectors to actual three-phase signals. For instance, consider the vector $\vec{V}_1$, whose switching function is [100] ($A = 1$, $B = 0$, $C = 0$). According to Eqs. (B.12)-(B.14), the values of the line-to-neutral voltages for this state are:

$$v_{Az} = \frac{2}{3}V_{dc} \qquad v_{Bz} = -\frac{1}{3}V_{dc} \qquad v_{Cz} = -\frac{1}{3}V_{dc} \tag{B.18}$$

A careful examination of $\vec{V}_1$ to $\vec{V}_6$ reveals that each phase goes through six steps of

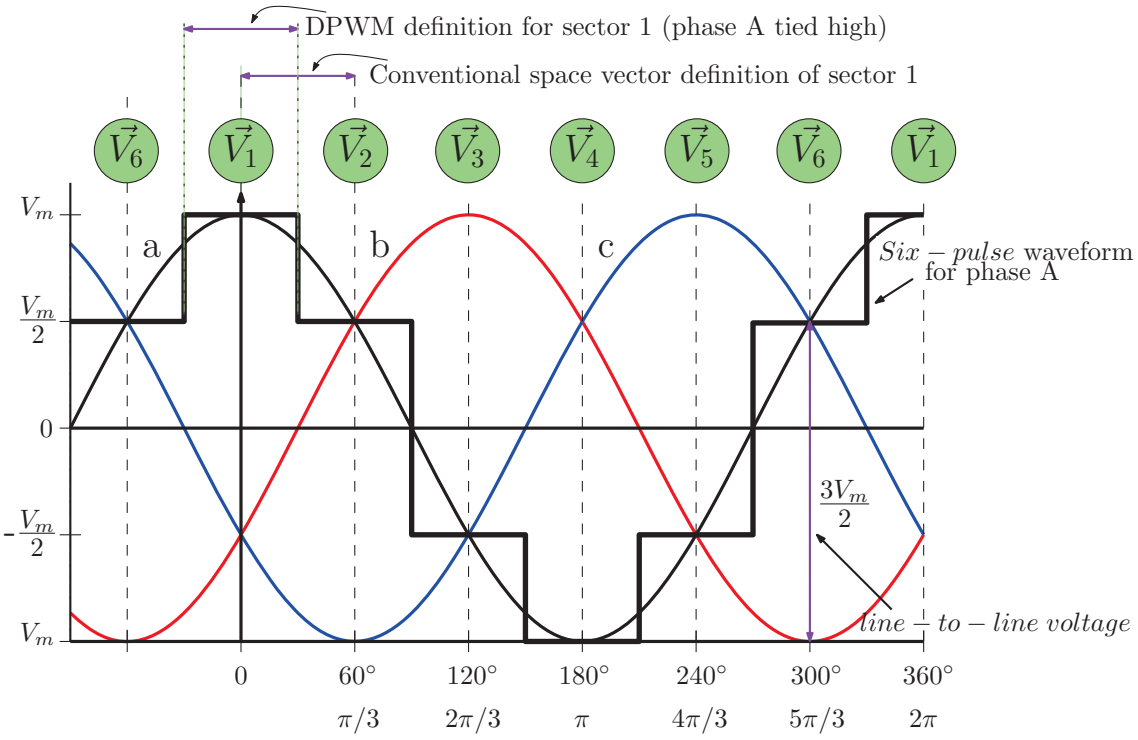


FIGURE B.4: The connection between space vectors and the three-phase six-pulse system

voltages following an approximated sinusoidal pattern. This is the basis of conventional *Six-Step Switching* of three-phase inverters.[1] The eight space vectors and particular switching states of each switch of the three phases are illustrated in Fig. B.2 and Fig. B.3 respectively.

The relationship between the six active vectors, the conventional six-step switching pattern and the original three-phase sinusoidal signals are graphically explained in Fig. B.4. Note that only six-step variation phase A is shown for the clarity of the figure. Following are very important observations that should be kept in mind when following the work of this thesis, especially when defining the *Sectors*.

- In conventional space vector modulation schemes for VSI systems, a *Sector* is defined as the stage between two vectors. For example, sector 1 is defined as the part between $\vec{V_1}$ and $\vec{V_2}$ as illustrated in Fig. B.4.

[1] Of course, in conventional six-step modulation, there is no space vector based modulation scheme governing the switching. But as it happens, it actually switches between these six vectors.

- It is important to realize, that according to the above definition, the peak of phase A does not occur at the mid point between $\vec{V_1}$ and $\vec{V_2}$, but at the exact occurring point (or the position) of $\vec{V_1}$.
- The DPWM based sector definition is not the same as the above sector definition. In DPWM based sector definition, $\vec{V_1}$ is indeed the midpoint of sector 1 (see Fig. B.4).

Note that in Fig. B.4, the peak of the sinusoids are defined as a particular value V_m. Another important observation can be made here with particular reference to the book [1] by Holmes and Lipo. For example, consider the occurrence of $\vec{V_1}$ and the sinusoidal variations of the three phases. At this point, the phase A is at its maximum voltage and the line-to-line voltages v_{AB} and v_{AC} both are equal to $\frac{3}{2}V_m$. But, if the real three-phase system is considered (as shown in Fig. A.1), and the switching state is stated according to the function [100], the values of the line-to-line voltages are equal to V_{dc} (i.e. $v_{AB} = V_{dc}$ and $v_{AC} = V_{dc}$). This results in the following realization:

$$\frac{3}{2}V_m = V_{dc} \quad \Rightarrow \quad V_m = \frac{2}{3}V_{dc} \tag{B.19}$$

In the book [1], authors interpret this as follows: The magnitudes of the six active vectors can be regarded as still snapshots of a three-phase sinusoidal system with a magnitude V_m. Note that this particular three-phase system (shown in Fig. B.4) has a fundamental of magnitude V_m (which is also equal to the peak value of the six step waveform). However, the important fact to realize is, that in practise, we have only eight vectors to synthesize a three-phase sinusoidal system, not a continuous set of vectors with magnitude V_m. Therefore, when a sinusoid is synthesized with only eight vectors, the magnitude of the generated fundamental voltage signal is always less than V_m. For instance, the value of the fundamental of the above six-step waveform is less than V_m. Furthermore, with the aid of dwell-time calculations, it can be shown that the maximum magnitude of the fundamental that can be achieved for this space vector system is $\frac{1}{\sqrt{3}}V_{dc}$ [6].

Appendix C

Relevant Magnetic Theory

Electromagnetism is the basis for the Quantum Electrodynamics–a field theory that is part of the Quantum Field Theory of Particle Physics. There are four forces in quantum field theory including Electromagnetism; while, Strong, Weak and Gravity being the other three. Photons are the force carriers in quantum electrodynamics. This is a micro view of electromagnetism. However, what we work on as electrical engineers is more of a macro view of electromagnetism.

An understanding of the basic relationship between the parameters in magnetic circuits is essential in deriving secondary relationships. And sometimes, the terminology could be confusing for the novice reader. Therefore, a clear picture of relevant magnetic theory is presented in this appendix as supplementary material.

C.1 Basics of Circuit-Magnetics

Sometimes it can be harder to picture magnetic circuits as opposed to picturing much familiar electrical circuits. For instance, the relationship between magnetic flux and inductance can be confusing when certain basic requirements are not explicitly mentioned. This section tries to derive commonly used equations in magnetics, with a clear logical flow.

C.1.1 The Voltage Across an Inductor and the Self Inductance

Faraday's law states that the voltage induced across an inductor, v_L, is proportional to the rate of change of the flux linkage, λ:

$$v_L = \frac{d\lambda}{dt} \tag{C.1}$$

Here, λ is simply the product of the flux (Φ) through the inductor coil and the number of turns (N) of the inductor coil .

$$\lambda = N\Phi \tag{C.2}$$

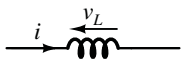


FIGURE C.1: An inductor

The relationship between the flux linkage and the current is a non-linear relationship, and is dependent upon the core material. This characteristic can be linearized if the magnetic core has a constant relative permeability (μ_R). This is illustrated in Fig. C.2. Air core inductors are a good example of this linearized characteristic. For ferromagnetic cores, the assumption is still valid as far as the excitation is minimum.

Assuming a linearized characteristic, the slope (gradient) of the graph is given by:

$$slope = \frac{d\lambda}{di} = \frac{\lambda}{i} \tag{C.3}$$

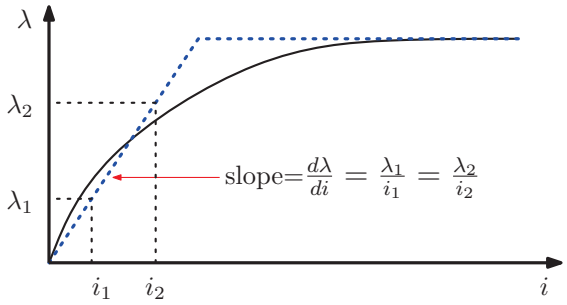


FIGURE C.2: Variation of flux linkage (λ) vs current (i)

For the linearised curve, the slope is a constant. We define this new constant parameter as the *Self Inductance* (L) of the inductor, and therefore referring to Eqs. (C.2) and (C.3):

$$L = \frac{d\lambda}{di} = \frac{\lambda}{i} = \frac{N\Phi}{i} \tag{C.4}$$

Now referring back to Eq. (C.1), we arrive at the familiar equation for the voltage across an inductor:

$$v_L = \frac{d\lambda}{dt} = \frac{d\lambda}{di} \times \frac{di}{dt} = L\frac{di}{dt}$$

$$\therefore v_L = L\frac{di}{dt} \tag{C.5}$$

C.1.2 Magneto Motive Force, Permeability and Reluctance

The Magneto Motive Force (MMF) is the ability of a magnetic circuit to drive magnetic flux through the core, and is defined as:

$$mmf = \sum Ni \tag{C.6}$$

The ability of the magnetic circuit path to oppose the building up of magnetic flux (due to applied mmf) is defined as the *Magnetic Reluctance* ($\Re$). And therefore, as a result of Ampere's law:

$$\sum Ni = \Phi\Re \tag{C.7}$$

Fig. C.3 provides simple depiction of these ideas.

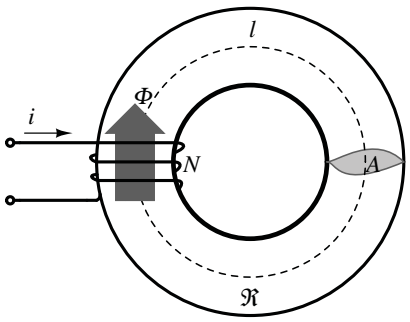


FIGURE C.3: Magnetic flux path

The reluctance of the magnetic circuit depends upon the magnetic material, and the physical dimensions of the magnetic circuit itself. This can be described according to the following expression:

$$\Re = \frac{l}{\mu A} \tag{C.8}$$

Here, l and A are the length and the cross sectional area of the magnetic path respectively. And, μ is the permeability of the magnetic material.

A very important result is obtained by, substituting $\Phi = \frac{Ni}{\Re}$ from Eq. (C.7) in Eq. (C.4):

$$L = \frac{N\Phi}{i} = \frac{N}{i} \times \frac{Ni}{\Re}$$

$$\therefore L = \frac{N^2}{\Re} \tag{C.9}$$

This result states that the self inductance depends only on physical parameters of the magnetic circuit, and more importantly, does not depend on the current i (provided that the assumption of linearity between λ and i is valid).

C.2 Mutual Inductance and Coupled Inductors

As the relationship between basic parameters in magnetic circuit terminology is already developed in Appendix C.1, let us move forward and derive some important results underlying the concepts of mutual inductance, magnetizing inductance and coupled inductors.

C.2.1 Mutual Inductance

A simple system of two coils wound on a common magnetic core is shown in Fig. C.4. Due to the presence of a path for the flux to flow through the core common to both windings, the system is said to have mutual flux.

The resultant flux through the magnetic core is dictated by the individual flux contributions of the two windings. If the total flux through winding 1 is denoted by Φ_{Total}, then the voltage across winding 1 (v_{w1}) can be derived as follows with reference to Fig. C.4:

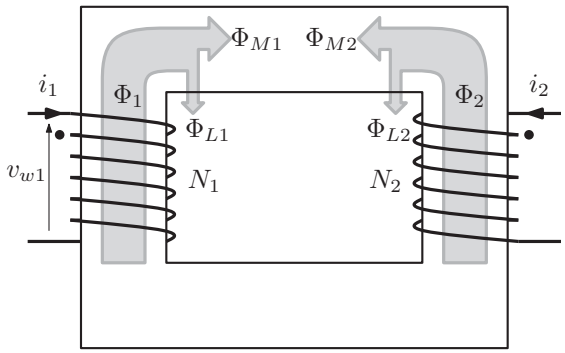


FIGURE C.4: Magnetic flux path for mutual coupling

$$\begin{aligned} v_{w1} &= \frac{d}{dt}\lambda_{Total} = \frac{d}{dt}(N_1\Phi_{Total}) \\ &= \frac{d}{dt}\big(N_1(\Phi_1 - \Phi_{M2})\big) \\ &= \frac{d}{dt}\big(N_1(\Phi_{L1} + \Phi_{M1} - \Phi_{M2})\big) \\ \therefore v_{w1} &= N_1\frac{d}{dt}(\Phi_{L1}) + N_1\frac{d}{dt}(\Phi_M) \end{aligned} \tag{C.10}$$

Note that, $\Phi_M = \Phi_{M1} - \Phi_{M2}$ is the flux common to both windings: i.e. the mutual flux $= \Phi_M$. Now, realizing that $\Phi = Ni/\Re$ (in general) from Eq. (C.7) and continuing on the above derivation:

$$v_{w1} = N_1\frac{d}{dt}(\frac{N_1 i_1}{\Re_{L1}}) + N_1\frac{d}{dt}(\frac{N_1 i_1 - N_2 i_2}{\Re_C}) \tag{C.11}$$

$$\therefore v_{w1} = \frac{N_1^2}{\Re_{L1}}\frac{d}{dt}i_1 + \frac{N_1^2}{\Re_C}\frac{d}{dt}i_1 - \frac{N_1 N_2}{\Re_C}\frac{d}{dt}i_2 \tag{C.12}$$

Here, $\Re_{L1}$ is leakage path's (of winding 1) reluctance, where $\Re_C$ is the reluctance of the common magnetic path which is mutual to both windings. From Eq. (C.9) it is clear that, $N_1^2/\Re_C$ is winding 1 self inductance L_1; and, similarly for winding 2, $N_2^2/\Re_C = L_2$. Now, considering the product of these two terms, we arrive at the following interesting result:

$$L_1 L_2 = \frac{N_1^2 N_2^2}{\Re_C^2} \qquad \longrightarrow \qquad \sqrt{L_1 L_2} = \frac{N_1 N_2}{\Re_C} \tag{C.13}$$

With the aid of this result, Eq. (C.12) can be simplified as:

$$v_{w1} = L_{L1}\frac{d}{dt}i_1 + +L_1\frac{d}{dt}i_1 - \sqrt{L_1 L_2}\frac{d}{dt}i_2 \tag{C.14}$$

We define the quantity $\sqrt{L_1 L_2}$ as the *Mutual Inductance* (M) between the two windings:

$$Mutual\ Inductance = M = \sqrt{L_1 L_2} \tag{C.15}$$

Finally, the voltage expression for winding 1 due to the total flux through it can be stated as,

$$v_{w1} = L_{L1}\frac{d}{dt}i_1 + L_1\frac{d}{dt}i_1 - M\frac{d}{dt}i_2 \tag{C.16}$$

Note that, if the windings are wound such that the fluxes Φ_{M1} and Φ_{M2} adds up (flow in the same direction inside the core), then it can be interpreted as M being a negative value:

$$v_{w1} = L_{L1}\frac{d}{dt}i_1 + L_1\frac{d}{dt}i_1 + M\frac{d}{dt}i_2 \tag{C.17}$$

C.2.2 Magnetizing Inductance

Consider the result derived in Eq. (C.11):

$$v_{w1} = N_1\frac{d}{dt}(\frac{N_1 i_1}{\Re_{L1}}) + N_1\frac{d}{dt}(\frac{N_1 i_1 - N_2 i_2}{\Re_C})$$

The term $\frac{N_1 i_1 - N_2 i_2}{\Re_C}$ represents the overall (or resultant or mutual) flux $\Phi_M = \Phi_{M1} - \Phi_{M2}$: this is what magnetizes the magnetic core (due to the effect of both windings). Therefore, Φ_M is defined as the *Magnetizing Flux* (or the *Resultant* mutual flux) [76]. If it is assumed that the magnetizing flux is effectively caused by winding 1 only, then the equivalent winding 1 current that is creating this flux in winding 1 is defined as the *Magnetizing Current*, i_M:

$$\frac{N_1 i_1 - N_2 i_2}{\Re_C} = \frac{N_1 i_M}{\Re_C} \qquad \longrightarrow \qquad i_M = i_1 - \frac{N_2 i_2}{N_1} \tag{C.18}$$

Now, using this result in Eq. (C.11), we get a different perspective on the voltage expression for winding 1:

$$v_{w1} = \frac{N_1^2}{\Re_{L1}}\frac{d}{dt}i_1 + \frac{N_1^2}{\Re_C}\frac{d}{dt}i_M \tag{C.19}$$

The coefficient of the second term on the right hand side (RHS) is actually the self inductance of winding 1; however, since it is associated with the magnetizing current, let us

define it as the *Magnetizing Inductance*, L_M:

$$Magnetizing\ Inductance = L_M = \frac{N_1^2}{\Re_C} \tag{C.20}$$

And now, Eq. (C.19) can be rewritten as:

$$v_{w1} = L_{L1}\frac{d}{dt}i_1 + L_M\frac{d}{dt}i_M \tag{C.21}$$

If the result from Eq. (C.21) is taken and i_M is replaced according to Eq. (C.18), another perspective is presented:

$$\begin{aligned} v_{w1} &= L_{L1}\frac{d}{dt}i_1 + L_M\frac{d}{dt}(i_1 - \frac{N_2 i_2}{N_1}) \\ v_{w1} &= L_{L1}\frac{d}{dt}i_1 + L_M\frac{d}{dt}i_1 - L_M\frac{N_2}{N_1}\frac{d}{dt}i_2 \end{aligned} \tag{C.22}$$

Compare this result with Eq. (C.16). We can conclude that, by considering the coefficients of the second term of the RHS of the two equations, the magnetizing inductance is same as the self inductance of winding 1 (i.e. $L_M = L_1$). However, we can see that, by considering the coefficients of the third set of terms on the RHS of the two equations, that mutual inductance and magnetizing inductance expressions are not the same.

$$M = L_M\frac{N_2}{N_1} \tag{C.23}$$

And if we substitute that $L_M = N_1^2\Re_C$ in Eq. (C.23), we find the result $M = N_1N_2/\Re_C$ which agrees with the result $M = \sqrt{L_1L_2}$ derived in Appendix C.2.1. This is true because, as $L_M(= L_1 = N_1^2/\Re_C)$ is defined as a quantity of winding 1, the term N_2/N_1 has to be there in the expression for M in Eq. (C.23) in order to make expression valid for both windings. In summary, it can be stated that the magnetizing inductance is associated with the resultant flux in the core caused by individual windings, but expressed effectively as caused by winding 1 only.

Note that, the mutual flux is usually not a combined parameter and refers to original mutual fluxes between windings. For example, the flux linking with winding 1 due to the flux caused by winding 2 current, is due to the mutual inductance M_{21}. Similarly, the flux

linking with winding 2 due to the flux caused by winding 1 current, is due to the mutual inductance M_{12}.

It is quite notable in common literature that the terms magnetizing inductance and mutual inductance are used interchangeably. Conceptually, both terms refer to the magnetization of the core. But, as long as the number of windings are different, their mathematical expressions are not the same. If the number of windings are the same, i.e. $N_1 = N_2$, then:

1. $L_1 = L_2$ due to the same number of turns. Also, since L_M is also equal to L_1 by definition, $L_1 = L_2 = L_M$.
2. From Eq. (C.23), $M = L_M$.

Usually, in coupled inductor topologies, the condition $N_1 = N_2$ is valid as the topology requires the two windings to have same number of windings (ex: for symmetrical operation of two parallelly connected inverter legs which are coupled with inductors). On the other hand, in transformers, this condition is not valid, unless it is a 1:1 transformer. Therefore, it makes more sense to use the term mutual inductance when coupled inductor circuits are concerned, and op to magnetizing inductance expressions with equivalent circuits when transformers are in the picture.

C.2.3 Coupled Inductors

As their name implies, coupled inductors are two or more windings who have mutual coupling that usually wound on a common magnetic core. The basic equations of mutual coupling are as derived in the previous sections (i.e. $M = \sqrt{L_1 L_2}$). One practical aspect of coupled inductors is the fact that coupling between two windings are not always perfect. This means Φ_{M1} would not couple 100% with winding 2 (see Fig. C.4). In order to account for this fact, a coupling coefficient k is defined for the two windings as follows;

$$M = k\sqrt{L_1 L_2} \qquad where \quad 0 < k < 1 \tag{C.24}$$

Usually with tight coupling on a single core, coupling coefficients up to 0.999 are possible [11]. This definition makes it clear why self (L) and mutual (M) inductances can differ. On the other hand, magnetizing inductance (L_M) is always defined as equal to the self inductance (L) of the considered winding (see Eq. (C.20)).

Appendix D

Design Files and Notes on the Developed Hardware Units

Some important design files are included to provide additional information on the hardware development and control of the experimental system. The following files are appended:

- VisSim/ECD control interface used for controlling the DSP.
- VisSim/ECD block-level design of the system program.
- Eagle schematic file of the SiC based MOSFET inverter leg.
- Eagle layout file of the SiC based MOSFET inverter leg.
- Component list for the SiC based MOSFET inverter leg design.
- Eagle schematic file of the main control board (includes 5 design pages).
- Eagle schematic file of the analogue sensor box board.
- Eagle schematic file of the split-power supply unit for the analogue sensor box boards.

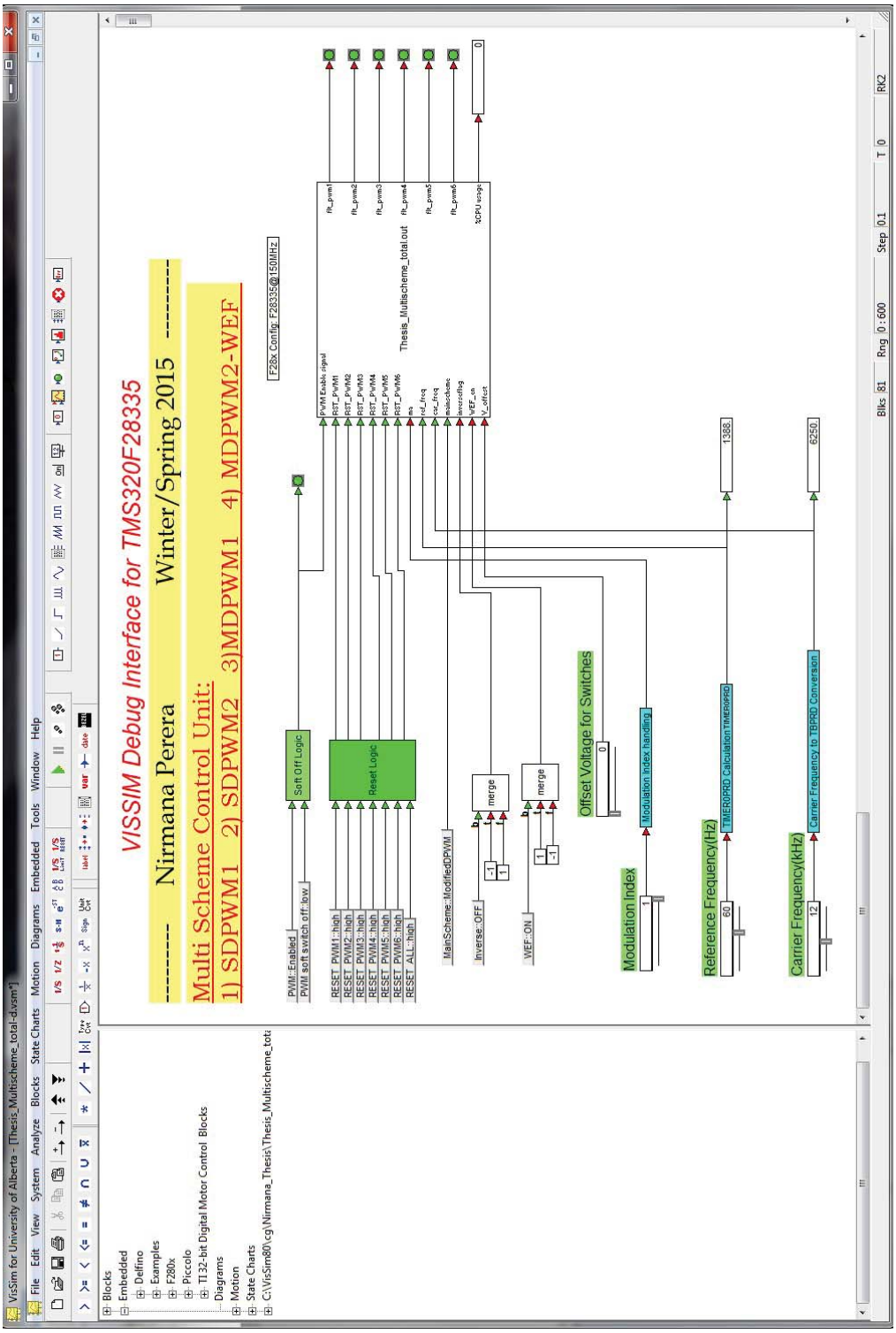


FIGURE D.1: VisSim/ECD control interface used for controlling the DSP

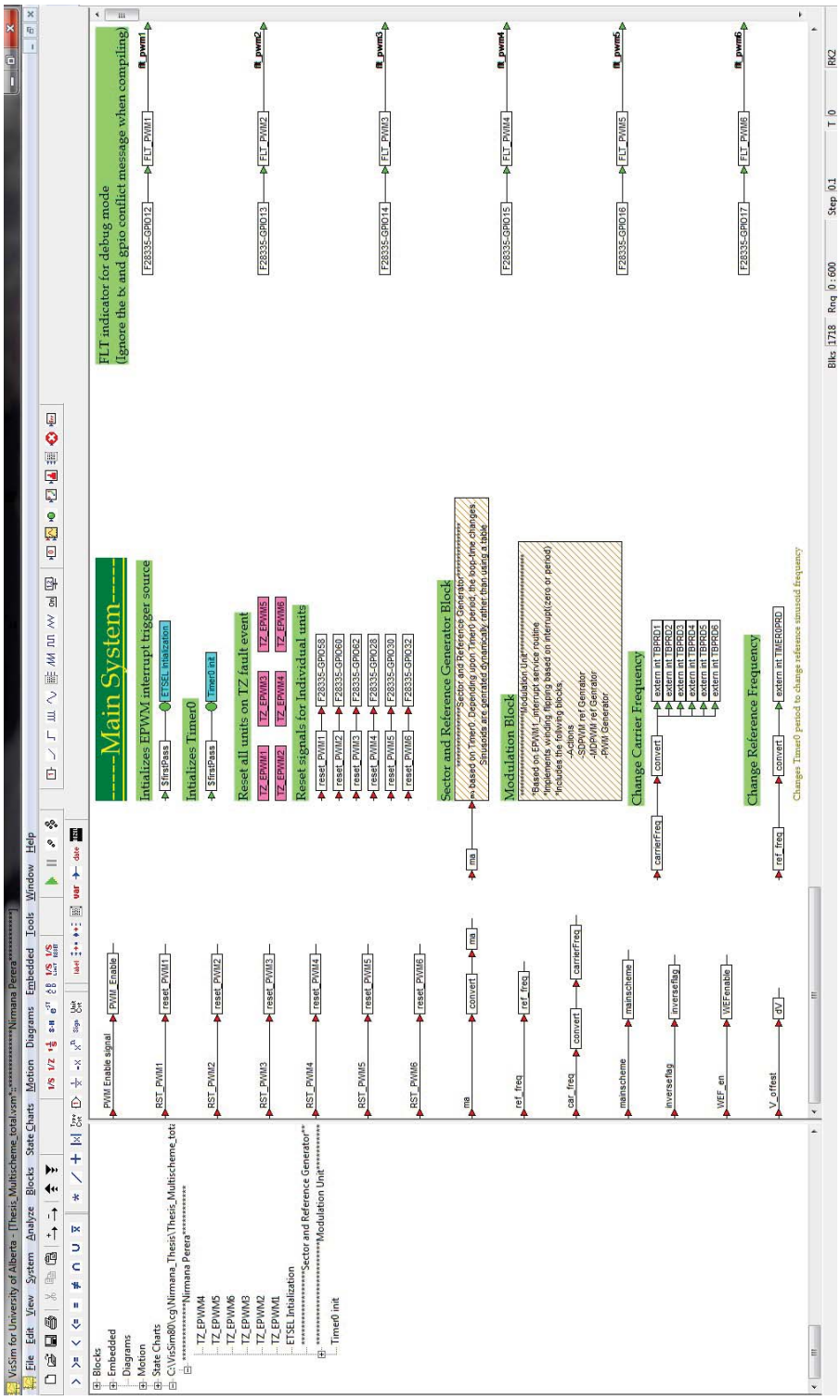


FIGURE D.2: VisSim/ECD block-level design of the system program

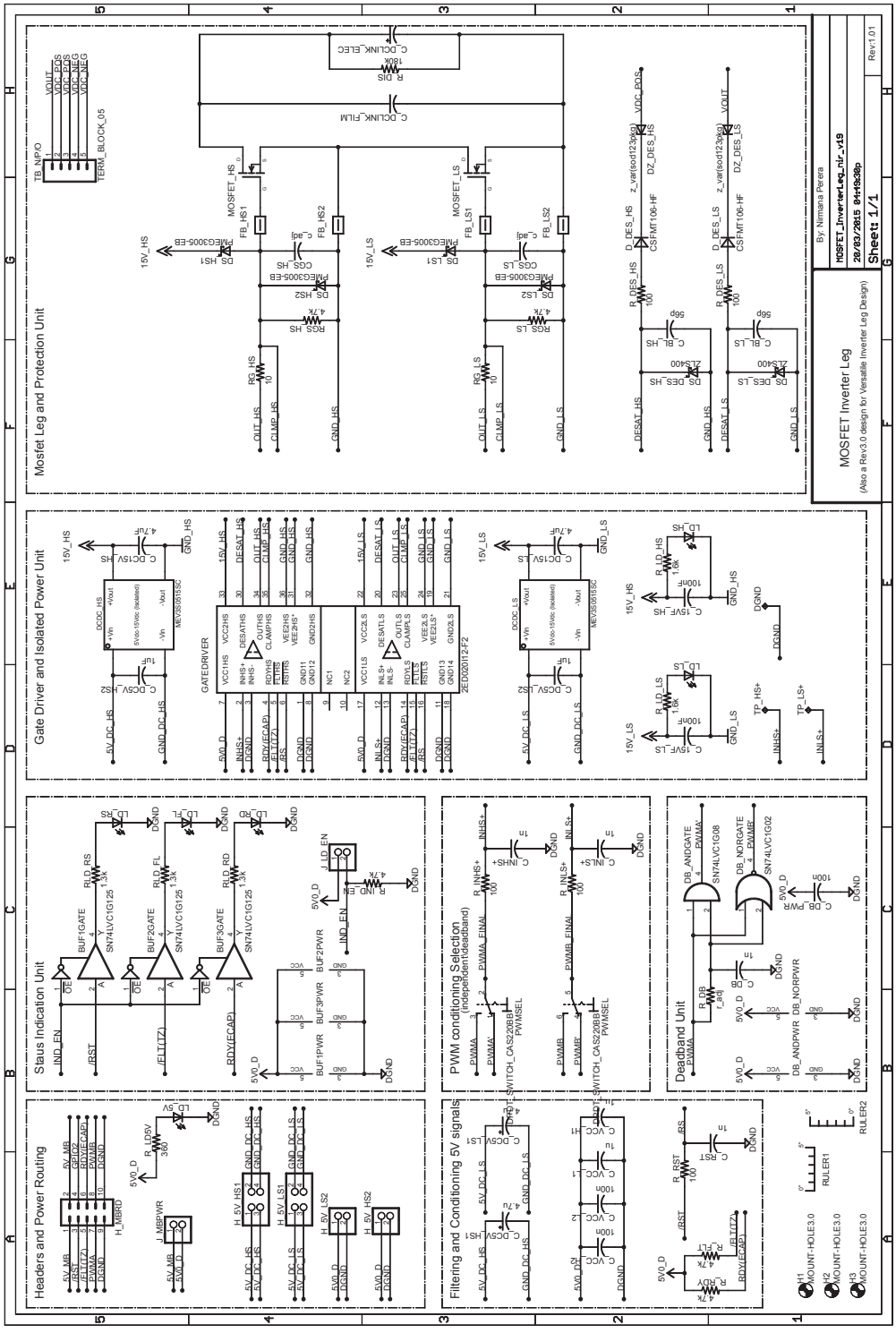


FIGURE D.3: Eagle schematic file: MOSFET inverter leg

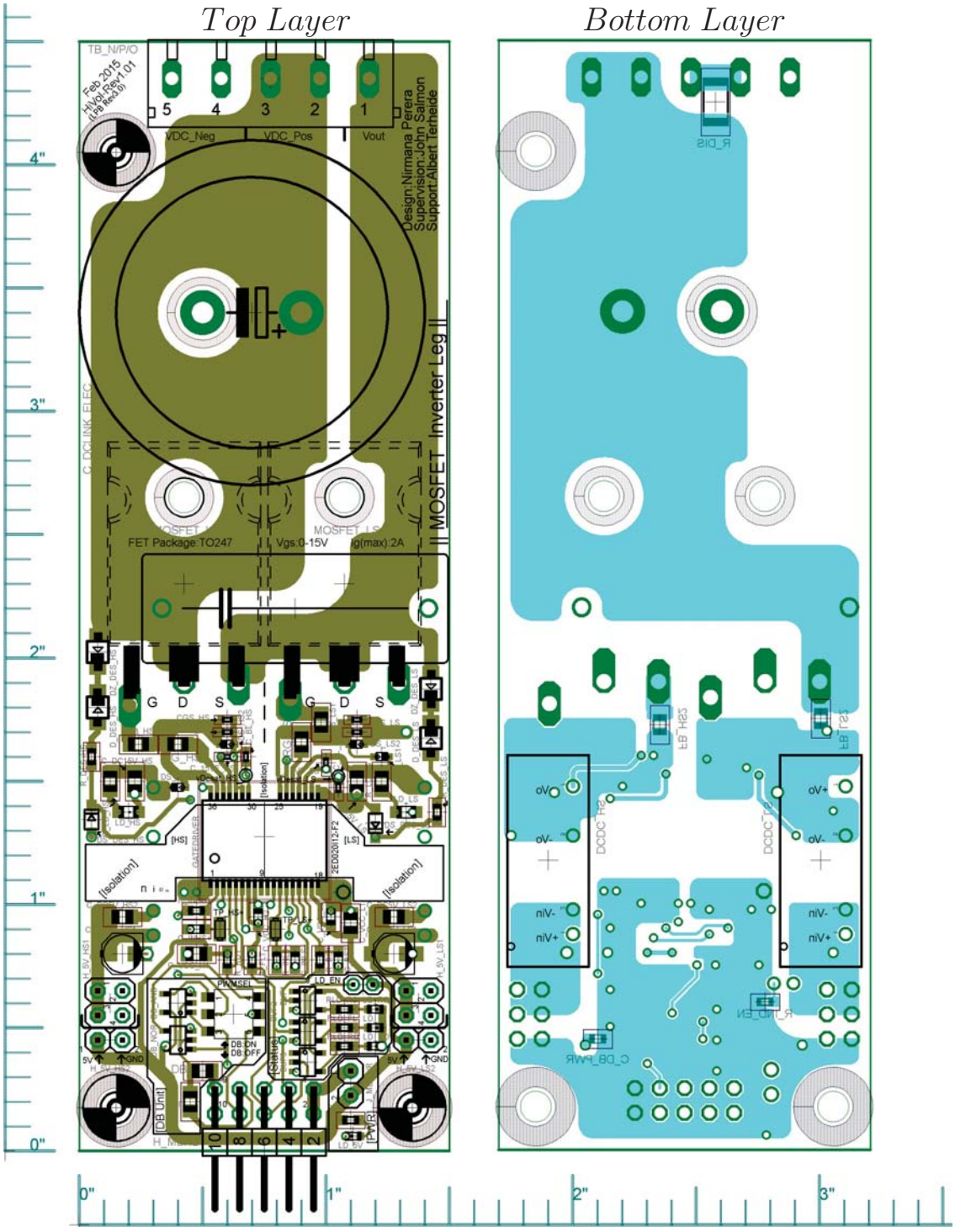


FIGURE D.4: Eagle layout file: MOSFET inverter leg - top and bottom layers

TABLE D.1: Component List for the Inverter Leg Design: Main Information

index	Qty	Device	Value	Package Remarks	Parts(1-6)
Power Side					
1	2	MOSFET	1200V/ 40A	TO-247-3 / Through Hole	MOSFET_HS, MOSFET_LS
2	2	Thermal Pad	Thermal Pad	TO-218, TO-220, TO-247	
3	1	Capacitor	5.0uF / 450V	Film / Through Hole	C_DCLINK_FILM
4	1	Capacitor	330uF / 400V	Snap-In / Through Hole	C_DCLINK_ELEC
5	1	Resistor	180k / 0.75W	SMD 2010	R_DIS
6	1	Terminal Block	5(1x5) pins	200mil pitch / Through Hole	TB_N/P/O
7	4	FERRITE Bead	60 Ohm @ 100MHz	SMD 0805	FB_HS1, FB_HS2, FB_LS1, FB_LS2
8	2	Capacitor	100nF /50V	SMD 0402	C_15VF_HS, C_15VF_LS
9	2	Capacitor	4.7uF / 50V	SMD 0805	C_DC15V_HS, C_DC15V_LS
10	2	Capacitor	56pF / 50V	SMD 0402	C_BL_HS, C_BL_LS
11	2	Capacitor	4.7nF / 50V	SMD 0402	CGS_HS, CGS_LS
12	2	Resistor	10 / 0.5W	SMD 0805	RG_HS, RG_LS
13	2	Resistor	2.2k / 0.2W	SMD 0402	RGS_HS, RGS_LS
14	5	Resistor	100 / 0.25W	SMD 0603	R_DES_HS, R_DES_LS, R_INHS+, R_INLS+, R_RST
15	2	Diode-Rectifier	400V / 1A	SOD-123 (SMD)	D_DES_HS, D_DES_LS
16	4	Diode-Shottky	Shottky- 30V / 500mA	SOD-523 (SMD)	DS_HS1, DS_HS2, DS_LS1, DS_LS2
17	2	Diode-Shottky	Shottky- 40V / 520mA	SOD-323 (SMD)	DS_DES_HS, DS_DES_LS
18	2	Diode-Zener	Zener- 8.2V / 500mW	SOD-123 (SMD)	DZ_DES_HS, DZ_DES_LS
19	2	LED	orange	SMD 0603	LD_HS, LD_LS
Gate Interface					
20	1		2ED020I12-F2	DSO-36 (36 pin SMD)	GATEDRIVER
21	2	DC-DC Conveter	15V / 200mA /3W	7-SIP (4 Leads) / Through Hole	DCDC_HS, DCDC_LS
Control Side					
22	3	Capacitor	1nF / 50V	SMD 0603	C_INHS+, C_INLS+, C_RST
23	1	Capacitor	100pF / 50V	SMD 0805	C_DB
24	4	Capacitor	1uF / 50V	SMD 0805	C_VCC_H1, C_VCC_L1 C_DC5V_HS2, C_DC5V_LS2
25	2	Capacitor	4.7uF / 35V	SMD/ Panasonic B / VS series	C_DC5V_HS1, C_DC5V_LS1
26	3	Capacitor	100nF / 25V	SMD 0603	C_DB_PWR, C_VCC_H2, C_VCC_L2
27	3	Resistor	1.3k / 0.25W	SMD 0603	RLD_FL, RLD_RD, RLD_RS
28	2	Resistor	1.6k / 0.5W	SMD 0805	R_LD_HS, R_LD_LS
29	3	Resistor	4.7k / 0.25W	SMD 0603	R_FLT, R_IND_EN, R_RDY
30	1	Resistor	360 / 0.25W	SMD 0603	R_LD5V
31	1	Resistor	510 / 0.5W	SMD 0805	R_DB
32	1	LED	green	SMD 0603	LD_5V,
33	3	LED	red	SMD 0603	LD_FL, LD_RD, LD_RD,
34	1	10-pin Header	10(2x5) pins	100mil pitch / Through Hole / Right Angle	H_MBRD
35	1	2-pin Header	2 pins	0.079" pitch / Through Hole	J_LD_EN

36	1	2-pin Jumper	2-pin Jumper	0.079" pitch	
37	4	2-pin Jumper	2-pin Jumper	100mil pitch	
38	2	6-pin Header	6(2x3) pins	100mil pitch / Through Hole	H_5V_HS1,H_5V_HS2 H_5V_LS1,H_5V_LS2
39	1	2-pin Jumper	2 pins	100mil pitch / Through Hole	J_MBPWR
40	1	Test Point	TESTPIN	0.040"Diameter / Through Hole	DGND
41	2	Test Pad	TESTPAD	SMD 0805	TP_HS+, TP_LS+
42	1	DPDT Switch	DPDT 2-position Switch	Surface Mount Dip Switch	PWMSEL
43	1	NOR Gate	1 gate / 5V / 32mA/ 4ns	SOT-23-5 (SMD-5pin)	DB_NOR
44	1	AND Gate	1 gate / 5V / 32mA/ 4.5ns	SOT-23-5 (SMD-5pin)	DB_AND
45	3	Tri-State Buffer	1 gate / 5V / 32mA	SOT-23-5 (SMD-5pin)	BUF1, BUF2, BUF3
Other					
46	3	Standoff	Threaded,Female-Female	4-40 / 0.5"	
47	3	Standoff	Threaded,Male-Female	4-40 / 0.375" / Aluminium	
49	1	Standoff	Threaded,Male-Female	4-40 / 0.375" / Nylon	

TABLE D.2: Component List for the Inverter Leg Design: Manufacturer and Distributor Information

index	Manufacturer	Manufacturer Part #	Digikey Part #	Digikey Description
Power Side				
1	Rohm Semiconductor	SCH2080KEC	SCH2080KEC-ND	MOSFET N-CH 1200V 40A TO-247
2	Bergquist	SP600-104	BER109-ND	THERMAL PAD TO-220 .009" SP600
3	EPCOS Inc	B32774D4505K	495-4828-ND	CAP FILM 5.0UF 10% 450V RAD
4	Cornell Dubilier Electronics (CDE)	380LQ331M400A012	338-3503-ND	CAP ALUM 330UF 400V 20% SNAP
5	Vishay Dale	CRCW2010180KJNEF	445-5932-1-ND	RES SMD 180K OHM 5% 3/4W 2010
6	FCI	20020316-H051B01LF	609-3939-ND	TERM BLOCK 5POS 5.08MM PCB HORIZ
7	Murata Electronics	BLM21PG600SN1D	490-1053-1-ND	FERRITE CHIP 60 OHM 0805
8	Murata Electronics	C1005X7R1H104K050BB	490-1519-1-ND	CAP CER 0.1UF 50V 10% X7R 0402
9	Samsung Electro-Mechanics America, Inc	CL21A475KBQNNNE	1276-1248-1-ND	CAP CER 4.7UF 50V 10% X5R 0805
10	TDK Corporation	C1005C0G1H560J050BA	445-1244-1-ND	CAP CER 56PF 50V 5% C0G 0402
11	Samsung Electro-Mechanics America, Inc	CL05B472KB5NNNC	1276-1125-1-ND	CAP CER 4700PF 50V 10% X7R 0402
12	Panasonic Electronic Components	ERJ-P06J100V	P10ADCT-ND	RES SMD 10 OHM 5% 1/2W 0805
13	Rohm Semiconductor	ESR01MZPJ222	RHM1014CT-ND	RES SMD 2.2K OHM 5% 1/5W 0402
14	Rohm Semiconductor	ESR03EZPJ101	RHM100DCT-ND	RES SMD 100 OHM 5% 1/4W 0603

15	Comchip Technology	CSFMT106-HF	641-1439-1-ND	DIODE GEN PURP 400V 1A SOD123H
16	NXP Semiconductors	PMEG3005EB,115	568-7397-1-ND	DIODE SCHOTTKY 30V 500MA SOD523
17	Diodes Incorporated	ZLLS400TA	ZLLS400TACT-ND	DIODE SCHOTTKY 40V 520MA SOD323
18	NXP Semiconductors	NZH8V2B,115	568-6375-1-ND	DIODE ZENER 8.2V 500MW SOD123F
19	Kingbright	APT2012SECK	754-1130-1-ND	LED 2X1.2MM 601NM OR WTR CLR SMD
Gate Interface				
20	Infineon	2ED020I12-F2	MOUSER:641-2ED020I12-F2	
21	Murata Power Solutions Inc	MEV3S0515SC	811-2119-5-ND	CONV DC/DC 3W 5V IN 15V OUT SIP
Control Side				
22	Murata Electronics	GRM188R71H102KA01D	490-1494-1-ND	CAP CER 1000PF 50V 10% X7R 0603
23	Samsung Electro-Mechanics America, Inc	CL21C101JBANNNC	1276-1014-1-ND	CAP CER 100PF 50V 5% NP0 0805
24	Taiyo Yuden	UMK212BJ105KG-T	587-2229-1-ND	CAP CER 1UF 50V 10% X5R 0805
25	Panasonic Electronic Components	EEE-1VA4R7SR	PCE3962CT-ND	CAP ALUM 4.7UF 35V 20% SMD
26	Samsung Electro-Mechanics America, Inc	CL10B104JA8NNNC	1276-1929-1-ND	CAP CER 0.1UF 25V 5% X7R 0603
27	Rohm Semiconductor	ESR03EZPJ132	RHM1.3KDCT-ND	RES SMD 1.3K OHM 5% 1/4W 0603
28	Panasonic Electronic Components	ERJ-P06J162V	P1.6KADCT-ND	RES SMD 1.6K OHM 5% 1/2W 0805
29	Rohm Semiconductor	ESR03EZPJ472	RHM4.7KDCT-ND	RES SMD 4.7K OHM 5% 1/4W 0603
30	Rohm Semiconductor	ESR03EZPJ361	RHM360DCT-ND	RES SMD 360 OHM 5% 1/4W 0603
31	Panasonic Electronic Components	ERJ-P06J511V	P510ADCT-ND	RES SMD 510 OHM 5% 1/2W 0805
32	Lite-On Inc	LTST-C190GKT	160-1183-1-ND	LED GREEN CLEAR 0603 SMD
33	Lite-On Inc	LTST-C190EKT	160-1182-1-ND	LED RED ORANGE CLEAR 0603 SMD
34	FCI	68021-210HLF	609-3410-ND	CONN HEADER 10POS .100 R/A 15AU
35	Harwin Inc	M22-2510205	952-1311-ND	CONN HEADER 2MM VERT AU 2POS
36	Harwin Inc	M22-1920005	952-1309-ND	CONN JUMPER SHORTING GOLD RED
37	Sullins Connector Solutions	SPC02SYAN	S9001-ND	CONN JUMPER SHORTING GOLD FLASH
38	TE Connectivity	826925-3	A106478-ND	CONN HEADER BRKWY 6POS VERT TIN
39	FCI	68001-202HLF	609-3469-ND	BERGSTIK II .100" SR STRAIGHT
40	Keystone Electronics	5116	5116K-ND	TEST POINT PC MINIATURE T/H GRN
41	TE Connectivity	1625854-2	A106144CT-ND	0805 PROBE PAD
42	Copal Electronics Inc	CAS-220TB	CAS220GCT-ND	SLIDE SWITCH DPDT GULL-WING 6V

43	Texas Instruments	SN74LVC1G02DBVR	296-11597-1-ND	IC GATE NOR 1CH 2-INP SOT-23-5
44	Texas Instruments	SN74LVC1G08DBVR	296-11601-1-ND	IC GATE AND 1CH 2-INP SOT-23-5
45	Texas Instruments	SN74LVC1G125DBVR	296-11603-1-ND	IC BUS BUFF TRI-ST N-INV SOT23-5
Other				
46	Keystone Electronics	2203	2203K-ND	HEX STANDOFF 4-40 ALUMINUM 1/2”
47	Keystone Electronics	8400	8400K-ND	HEX STANDOFF 4-40 ALUMINUM 3/8”
49	Keystone Electronics	4801	4801K-ND	HEX STANDOFF 4-40 NYLON 3/8”

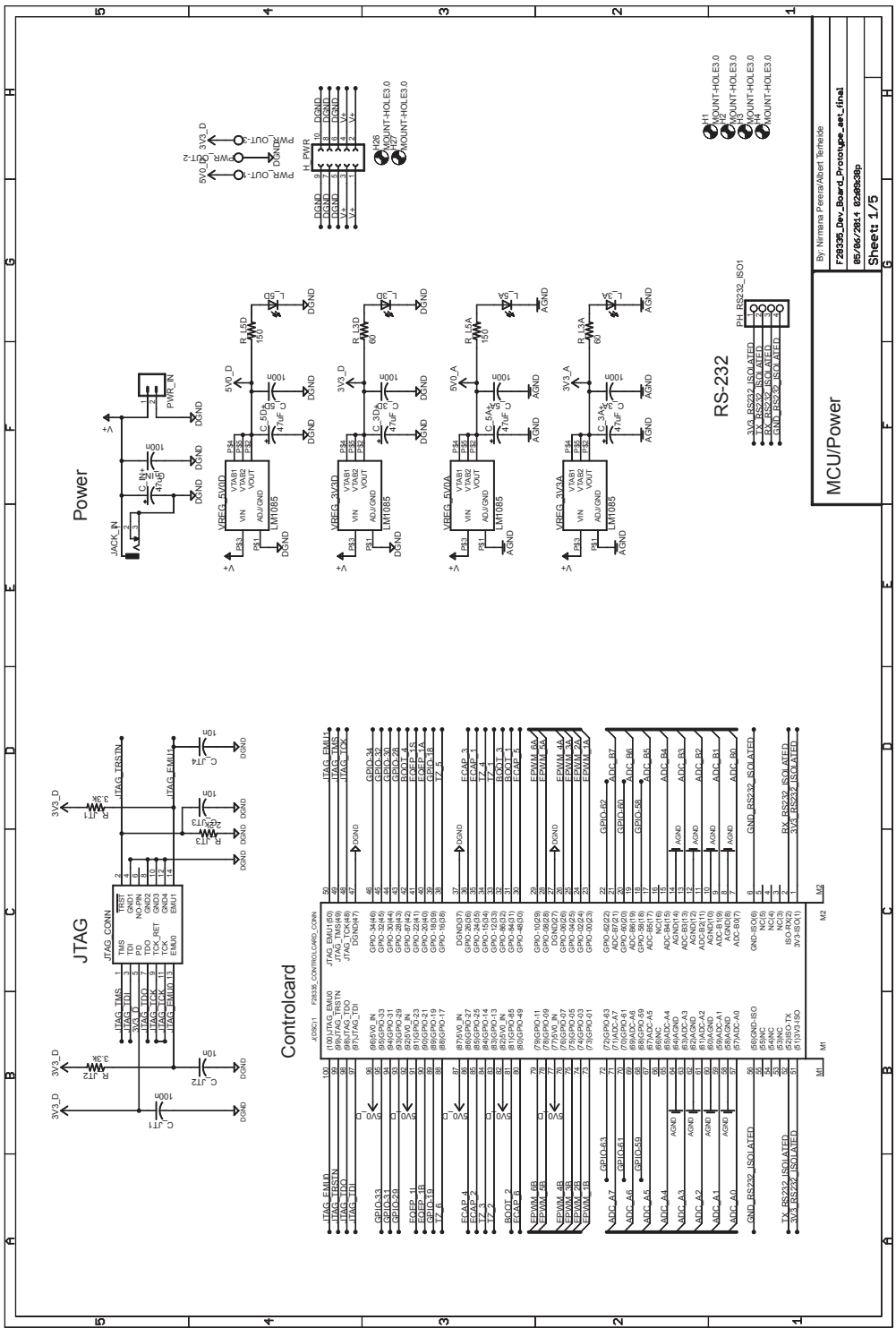


FIGURE D.5: Eagle schematic file: main control board - schematic page 1

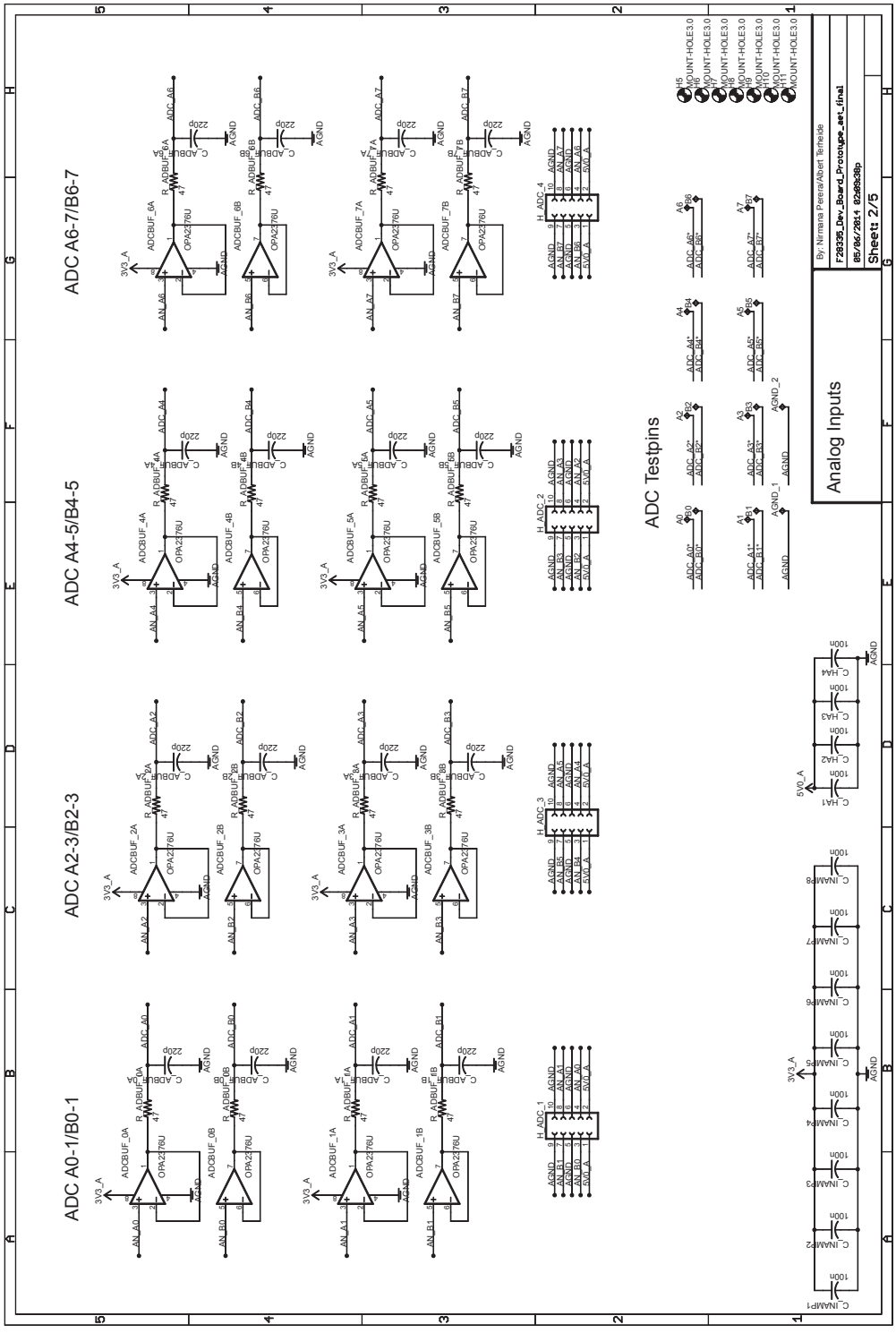


FIGURE D.6: Eagle schematic file: main control board - schematic page 2

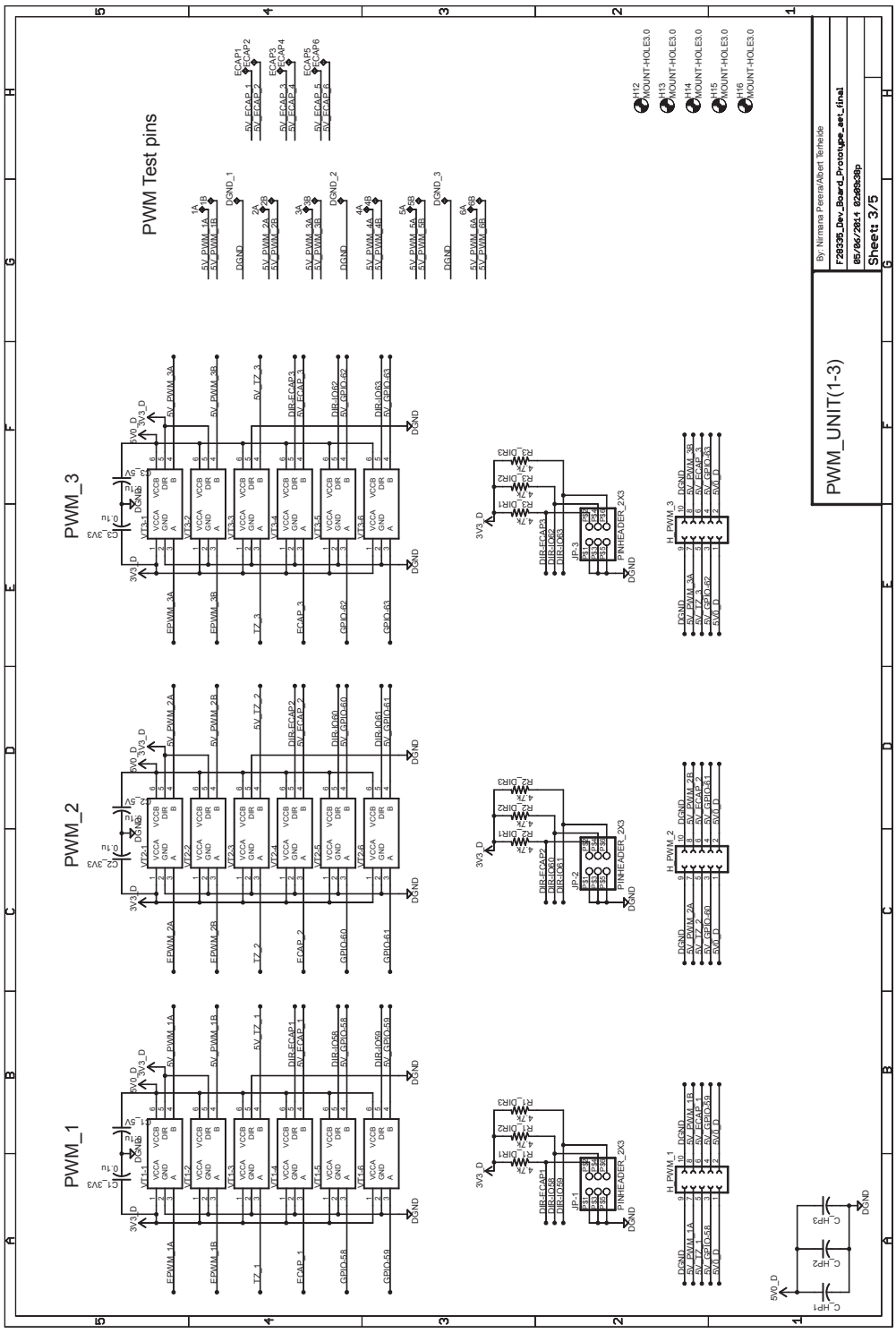


FIGURE D.7: Eagle schematic file: main control board - schematic page 3

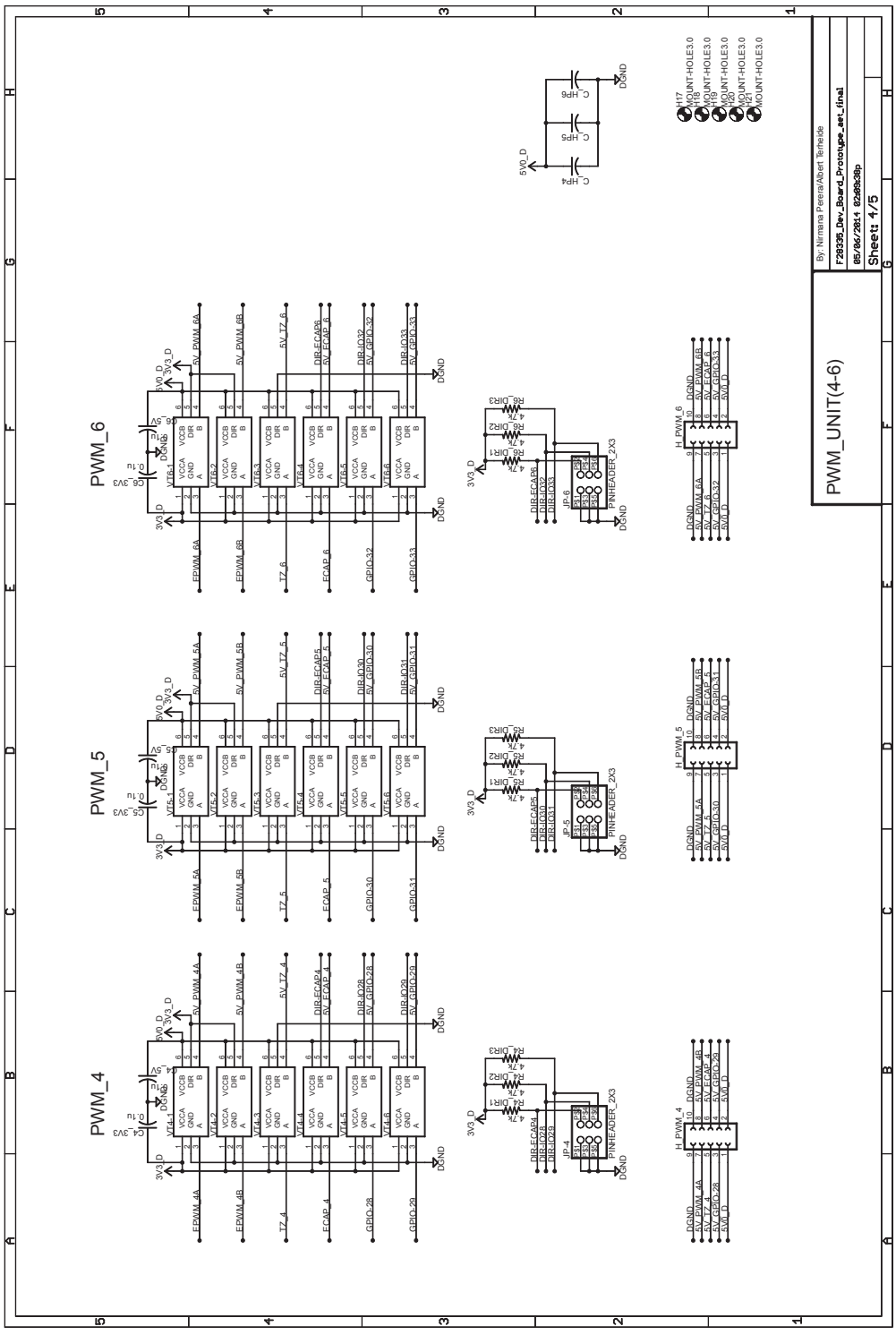


FIGURE D.8: Eagle schematic file: main control board - schematic page 4

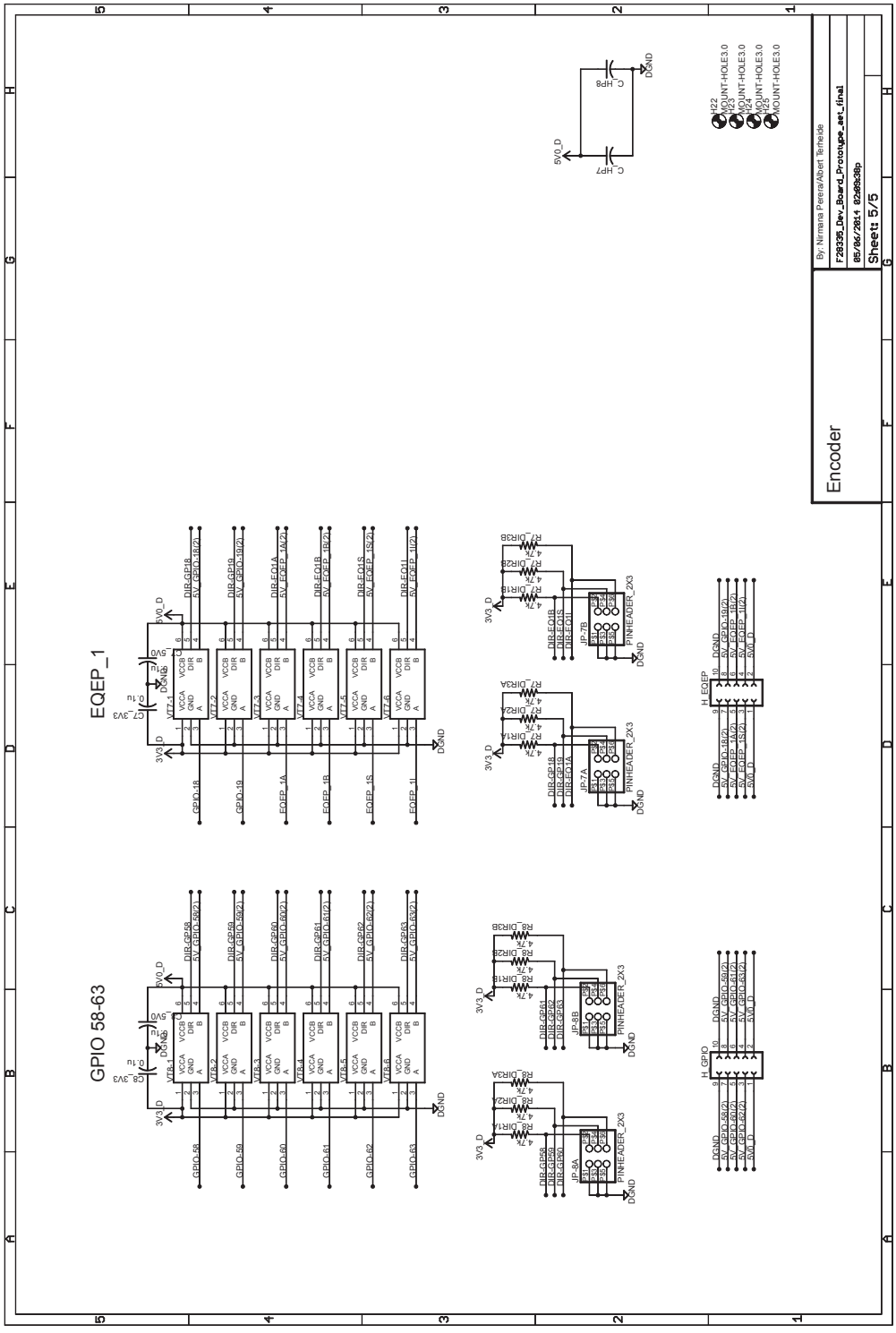


FIGURE D.9: Eagle schematic file: main control board - schematic page 5

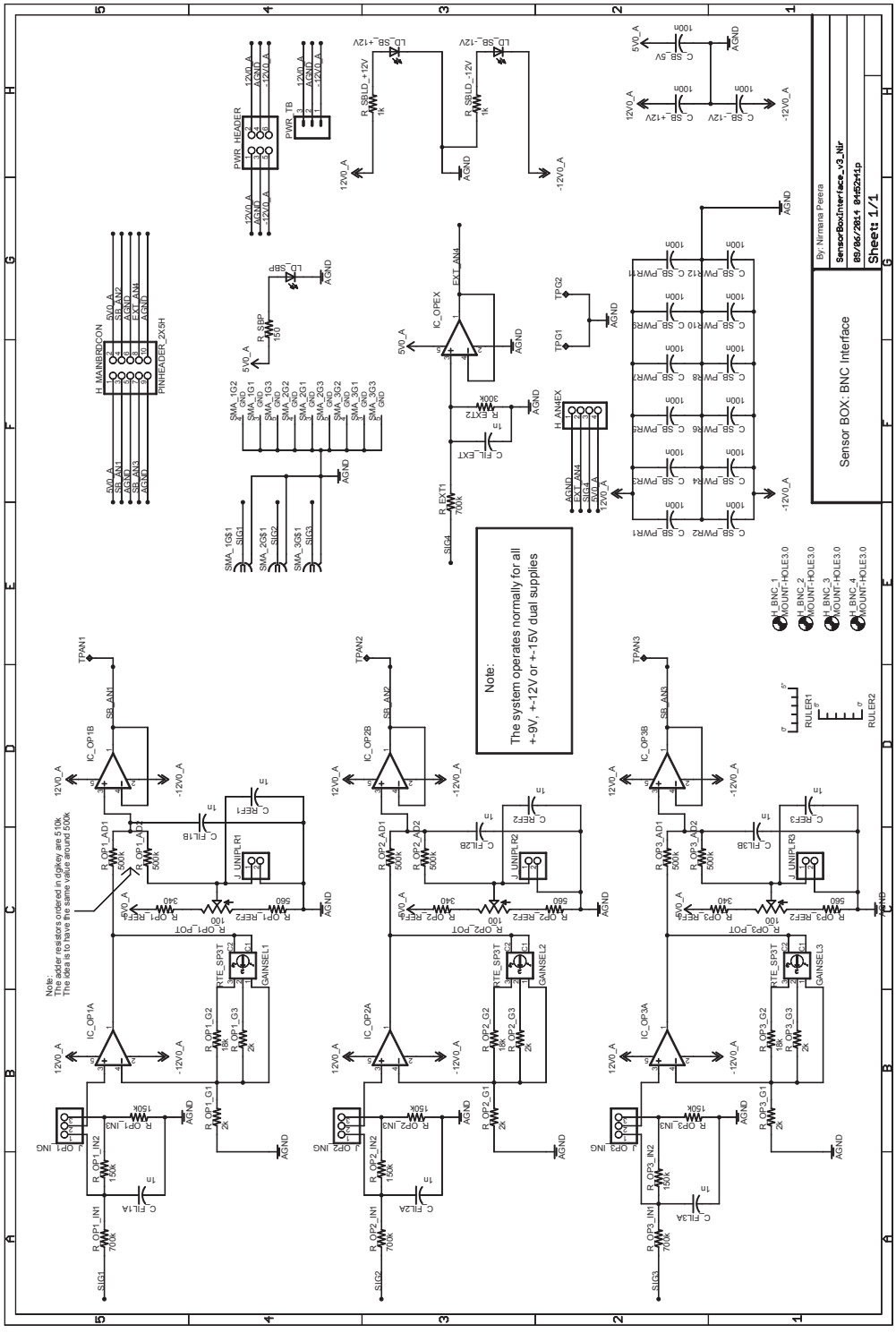


FIGURE D.10: Eagle schematic file: analogue sensor box board

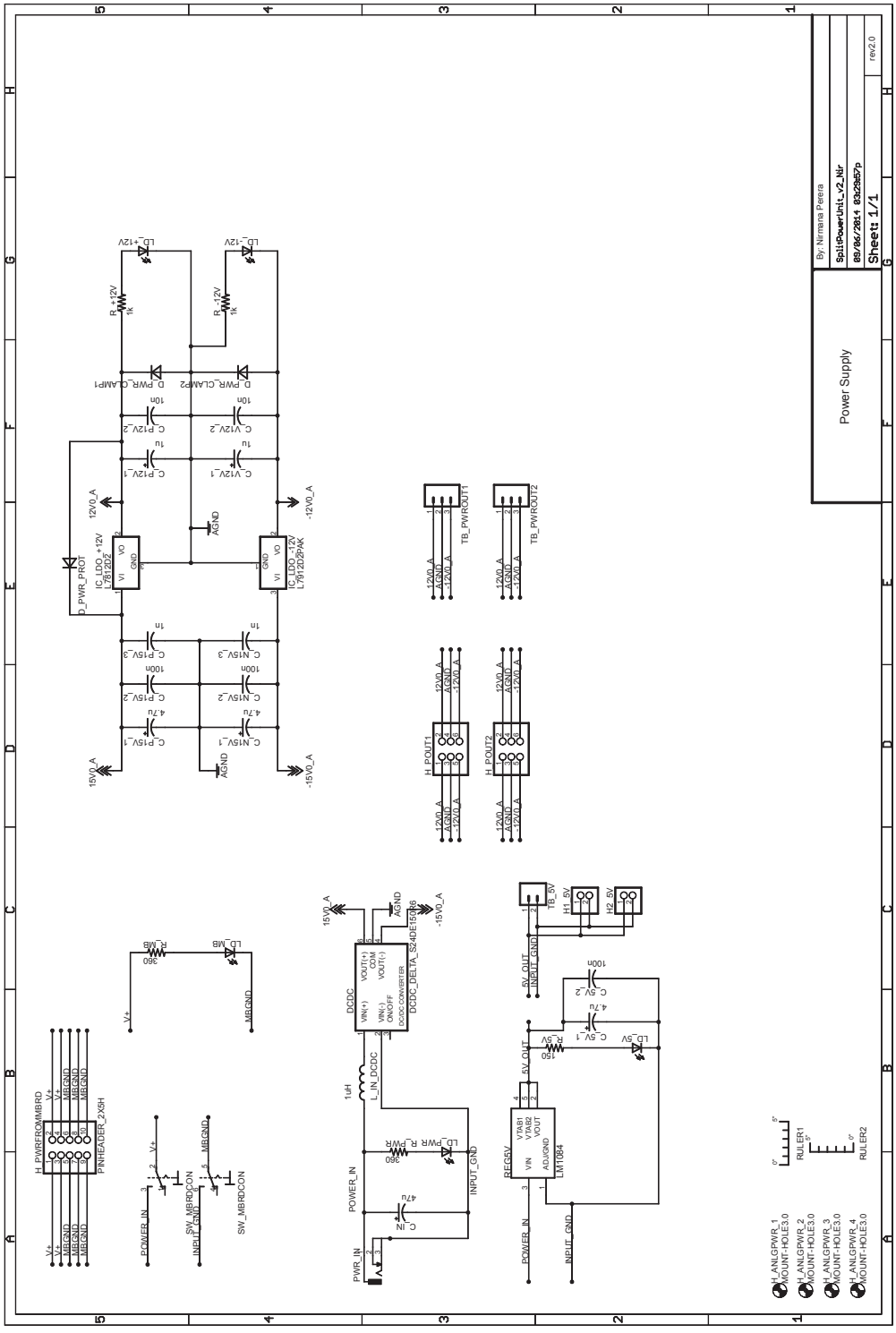


FIGURE D.11: Eagle schematic file: split-power supply unit for analogue sensor box boards

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