# Parallel Tapping LCC-HVDC Systems with Multiple Modular Multilevel Converters

by

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# Abstract

The idea of tapping is to extract a small amount of power from existing high voltage direct current (HVDC) transmission lines to minimize the infrastructure cost in electrifying rural communities. The vast majority of the previous research has focused on tapping schemes utilizing line commutated converter (LCC) based technologies that have operational limitations. With recent advancement of semiconductor devices and the introduction of new converter topologies, in particular, the full-bridge modular multilevel converter (FB-MMC) with direct current (DC) fault blocking capability, HVDC line tapping has regained attention.

This thesis presents a detailed hybrid multi-tapping study system developed in PSCAD/EMTDC that comprises two independently controlled FB-MMC-based HVDC tapping stations interfaced to the 1000 MW CIGRÉ LCC-HVDC benchmark model. The feasibility and system performance of the multi-tap stations is verified through extensive simulations that investigate the impact of changes in tapping power flows and varying fault locations at AC side of FB-MMCs. Simulation results reveal the majority of fault scenarios incite undesirable disturbances to the DC current/voltage of the LCC-HVDC system. This thesis develops i) a tap station current modulation method that transiently adjusts the current set-point of the healthy MMC tap, and ii) three supplementary controllers attached to the rectifier/inverter stations to reduce the impact of the tap AC side fault on the main LCC-HVDC system. Both fault mitigating schemes utilize only local measurements and are verified through extensive simulations at various operating points.

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# List of Acronyms

| | |
|---|---|
| AC | Alternating Current |
| DC | Direct Current |
| RES | Renewable Energy Source |
| HVDC | High-Voltage DC Transmission |
| MTDC | Multi-Terminal DC Transmission |
| LCC | Line-Commutated Converter |
| VSC | Voltage-Sourced Converter |
| CSI | Current-Sourced Inverter |
| MMC | Modular Multilevel Converter |
| FB | Full-Bridge |
| HB | Half-Bridge |
| FB-MMC | Full-Bridge Modular Multilevel Converter |
| HB-MMC | Half-Bridge Modular Multilevel Converter |
| IGBT | Insulated Gate Bipolar Transistor |
| SM | Submodule |
| CO | Current Order |
| CC | Constant Current |
| CEA | Constant Extinction Angle |
| VDCOL | Voltage Dependant Current Order Limit |
| CM | Current Margin |
| PLL | Phase-Locked Loop |
| PI | Proportional-Integral |

# Chapter 1

# Introduction

## 1.1 Background

Nowadays, global electricity generation relies heavily on the burning of non-renewable resources including fossil fuels such as coal and natural gas. In 2014, it was estimated that 77.2% of the electricity generation came from fossil fuels and nuclear energy, and 22.8% from renewable energy sources (RESs) [1]. To comply with the European Union goal of reducing greenhouse gas emission to 5-20% of 1990 level by 2050 [2], it is foreseeable that the increasing number of RESs such as solar farms and wind farms will replace the conventional means of centralized power generation.

As RESs are usually located far away from major consumption sites, grid integration of RESs through lengthy alternating current (AC) transmission lines is subjected to operational limitations and requires intermediate compensation devices. In particular, integrating offshore wind farms through underwater AC cables is limited to about 30 km due to the high capacitance of the cable [3]. Therefore, high voltage direct transmission (HVDC) has proven to be an effective technology for the transfer of power with various advantages over conventional AC transmission including [3], [4]:

1. Efficient delivery of power over long distances
2. Ability to interconnect systems with different frequencies
3. Capability to prevent propagation of power system faults
4. Power transfer capability over long submarine cables
5. Rapid and precise control of power flow
6. A narrower right of way

Fig. 1.1 shows a simple schematic of a classical point-to-point HVDC link with a power converter at each end of the HVDC line. The converter at the sending end of the line (denoted rectifier) converts AC to direct current (DC) power whereas the converter at the receiving end of the line (denoted inverter) converts DC to AC power.

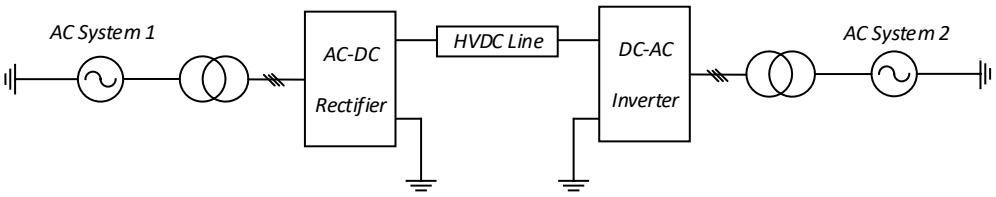



Figure 1.1: Point-to-point HVDC system

The first commercial application of the HVDC transmission was commissioned in 1954 utilizing mercury-arc valves to power the Swedish island of Gotland from shore by a 90 km underwater link [5]. However, due to the potential environmental hazard associated with mercury compounds and the introduction of more reliable converter technologies, the last mercury-arc valve based HVDC system was decommissioned in 2012.

With the advent of thyristor valves, line-commutated converter (LCC) employing thyristor valves with controlled turn-on ability offers higher reliability, larger transmission capacity, and lower maintenance compared to the mercury-arc valves. The first LCC-based back-to-back HVDC system was commissioned in 1972 to interconnect the power system of New Brunswick and Quebec [6]. The drawback of LCC includes a large footprint, requirement of reactive power compensation devices, large harmonic filters, and the inconvenient power reversal by changing the DC voltage polarity. In addition, as the commutation of LCC relies on the strength of the AC system, AC voltage disturbances or AC weak systems make LCC inverters more prone to commutation failure which would lead to the shutdown of the entire HVDC system. As of today, LCC is still the most established and widespread HVDC converter technology that is capable of transferring bulk power.

With the advancement of semiconductor devices, voltage-sourced converter (VSC) utilizing Insulated-Gate Bipolar Transistors (IGBTs) with controlled turn-on/off ability is an emerging HVDC converter technology featuring a smaller station footprint, independent control of active/reactive powers, ability to connect to a weak AC system, black start capability, and no risk

of commutation failure. Moreover, DC power reversal can be achieved by simply reversing the direction of the DC current. The traditional two-level VSC is limited to low-voltage and medium-voltage applications due to the low voltage rating of IGBT valves. Although it is possible to utilize series-stacking of switches to realize a higher voltage rating, the cost and the risk of unequal distribution of voltage among switches make it an unfavorable option. As the two-level VSC is only capable of generating two voltage levels at its AC terminal, its associated disadvantages include high switching losses, high derivative in voltage with respect to time, and high total harmonics distortion. Multilevel converters such as the cascaded H-bridge and the flying capacitor converter feature better waveform quality and lower switching losses by generating multiple voltage levels. However, the cost and control complexity of these topologies increase exponentially as the number of voltage levels increases.

The modular multilevel converter (MMC), introduced in the early 2000s, belongs to the family of VSCs and is widely popular due to its low harmonics, and high efficiency for high voltage and power applications [7]. The highly modular MMC employs a large number of low voltage switching cells (submodules) stacked in series to build up to the desired operating voltage, which increases the number of voltage output levels and the quality of the output voltage. Two common submodule (SM) topologies are the half-bridge (HB) SM and the full-bridge (FB) SM shown in Figs. 1.2(a) and (b), respectively. The SM output voltage ($V_{SM}$) of an HBSM containing two IGBTs can be either the capacitor voltage ($V_{cap}$) or zero. The FBSM consists of four IGBTs and is capable of producing an SM voltage equal to $\pm V_{cap}$ or zero. As each SM contains an individual capacitor, the large DC link capacitor required for the two-level VSC is no longer needed. However, the control system required for an MMC is more complicated than other converter topologies due to the necessity of balancing a large number of cell capacitors, and the suppression of internal circulating currents.

Traditionally, the converters of a point-to-point HVDC system adopt the same type of technology, namely LCC or VSC. However, a hybrid two-terminal HVDC system with an LCC rectifier and a VSC inverter would combine the advantages of both types of converters. With the rapid development of the DC grids and RESs, multi-terminal DC (MTDC) systems composed of three or more terminals are established to increase the power exchange among HVDC systems.

Moreover, the addition of a VSC to a conventional LCC-based HVDC system to facilitate the integration of offshore wind farms [8] opens up the prospect of hybrid MTDC systems.

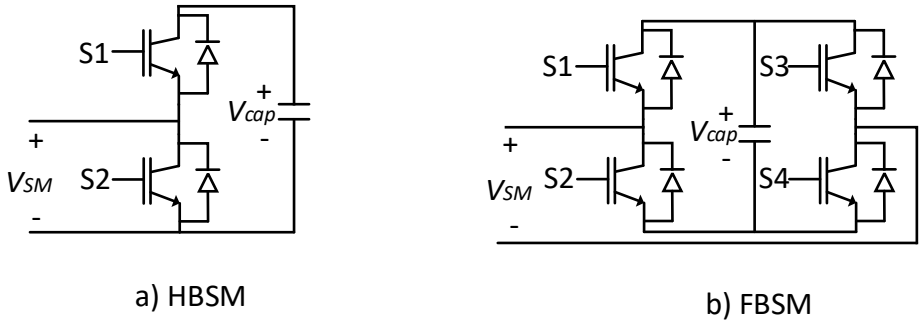



Figure 1.2: SM topologies

## 1.2 HVDC System Tapping

With the increasing number of HVDC lines commissioned around the world, many small communities located close to HVDC lines still rely on self-generation or have no access to electricity. Therefore, the HVDC infrastructure enables the prospect of "tapping" small amounts of AC power from the DC line using power electronic converters to electrify nearby communities at reduced cost and complexity, and to assist nearby communities in meeting the load growth demand. For example, the Manitoba Hydro Nelson River Bipole III project is expected to pass by as many as seven communities serviced by diesel generations or have limited access to electricity [9]. Thus, the idea of a tap can be applied by installing power electronic converters to extract a small amount of power to feed the communities located in the vicinity of the HVDC line. The general consensus is that the tap power rating should be restricted to 2-5% of the main HVDC system [10]. In addition, tapping can be further extended to inject power into the main HVDC system to facilitate integration of RESs. Since there is no theoretical limit on the number of tap stations attached to an HVDC line, multiple tapping stations can be added to an HVDC link and the number of tap stations attached to an HVDC system must be carefully selected based on the cost-benefit analysis. However, one of the main design requirements of power system tapping is that the addition of the tap should not jeopardize the operation of the main HVDC system at any time. An analytical method for calculating the power tapping limit to comply with the voltage regulation of HVDC systems is developed in [11], [12]. Series and parallel tappings are the main tap configurations with the latter being more suitable to extract a larger amount of power.

### 1.2.1 Series Tap

Series-connected taps that carry the same amount of DC current as the main HVDC system are illustrated in Fig. 1.3. Power tapping is realized by varying $v_{tapi}$ described in (1.1) for *i = 1 to N*. The lower cost of semiconductor switches rated for high current and low voltage makes series tapping an economic solution.

$$P_{tapi} = v_{tapi} \times I_d. \tag{1.1}$$

As series tapping introduces voltage drops to the main HVDC system, it is mainly considered for low power applications to avoid the need for DC voltage compensation devices. Moreover, the power tapping ability of series taps is highly dependent on the magnitude of the DC link current. For example, a reduction in the DC link current will cause the already fully-loaded series tapping station to further increase its DC voltage and risking to exceed the converter voltage rating in order to meet the scheduled tapping power. Another disadvantage of series tapping is that the extremely high DC voltage isolation needed between the AC transformer windings leads to costly and challenging transformer design and manufacturing.

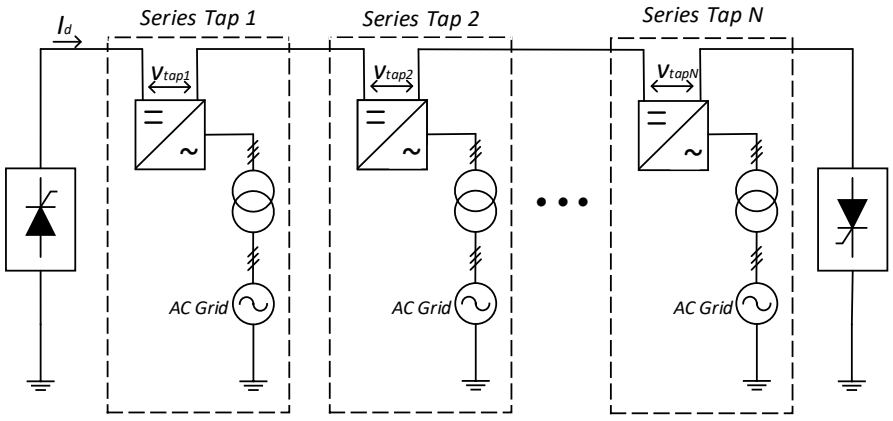



Figure 1.3: Series tap

As a series tapped converter operates at the DC line potential, the converter, valve arrester, and bridge arrester must be located on an insulated platform to avoid short circuits with the ground. In addition, the converter must be rated for the maximum transient overcurrent in case of main HVDC system faults or commutation failure. Auxiliary control and protection schemes should be

adapted to isolate the converter should HVDC line fault persists. For faults at the tap, bypass switches should operate to prevent the faulty converter from imposing additional impacts on the HVDC system.

### 1.2.2 Parallel Tap

The configuration of parallel connected taps that operate at the same DC voltage level as the main HVDC system is shown in Fig. 1.4. The power change is achieved by varying $I_{tapi}$ as indicated in (1.2) for *i = 1 to N*. The requirement of higher voltage and lower current rated switches, compared to series-connected taps, results in a higher installation cost.

$$P_{tapi} = v_d \times I_{tapi}. \tag{1.2}$$

The parallel tapping offers better power tapping ability as the DC link voltage of an HVDC system remains relatively constant regardless of the amount of transferred power. Thus, parallel tapping is considered as a more reliable solution for high power applications.

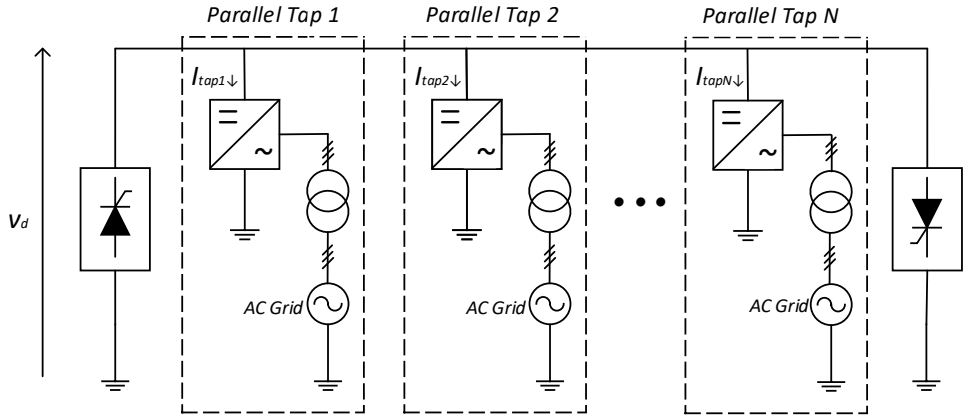



Figure 1.4: Parallel tap

A parallel tapped converter must be rated for the maximum transient overvoltage. Moreover, the converter may be exposed to transient overcurrents up to 20 times of the nominal current during main HVDC system faults and commutation failure. Thus, DC breakers along with proper protection and control measures should be implemented to prevent damages to tap converters that have no DC fault blocking capability.

### 1.2.3 Converter Selection

At present, most of the existing HVDC transmission networks are point-to-point systems based on LCC technology. Tapping LCC-HVDC systems with LCC-based converters is subjected to operational limitations. In particular, a weak AC grid which is typically the case for remote communities makes the LCC inverter more susceptible to commutation failure. This is especially true in case of AC faults on the load side of the tap, which could cause the shut down of the entire main HVDC line. Tapping with a multilevel current-source inverter (CSI) employing thyristors that are immune to commutation failure is explored in [13]; however, power reversal at the CSI requires interchanging its points of connection via mechanical switches which is undesirable. Therefore, the LCC-based converter is considered a less favorable candidate for tapping applications.

The capability of VSCs to operate in a weak AC system makes it a great candidate to deliver power to remote communities and to facilitate the integration of RESs. The incorporation of VSCs into an LCC-HVDC system in forming a hybrid MTDC system combines the advantage of both types of converter [14]. Such a hybrid system can also be extended to facilitate tapping to fully utilize the high power transferring capability of LCC-HVDC systems and the ability of VSC tap stations to operate under weak grid conditions. A hybrid two-stage series tapping scheme consisting of an LCC and two cascaded two-level VSCs is utilized to deliver power to a weak AC system [9]. The LCC inverter converts DC to AC power and the inverted AC voltage is stepped down via an AC transformer, which is then fed to a VSC-based DC-DC converter to supply power to a weak AC system. The main drawback of this scheme is the cost associated with the three converters and the control complexity. A parallel tapping scheme consisting of a two-level VSC with an intermediate DC-DC stage to reduce the number of high voltage equipment is proposed [15]. However, the additional DC-DC stage increases the system complexity and introduces a new potential point of failure. The ability of FB-MMCs to facilitate high voltage applications to block DC faults makes it a suitable candidate for tapping stations. The AC/DC fault response of an FB-MMC tapping station for an LCC-HVDC system is analyzed in [16]; however, it is limited to studying only one tapping station and therefore provides no insight into systems with multiple taps that can interact with one another. Similarly, the performance of an FB-MMC and an HB-MMC tapping station is evaluated in [17]. As there is no limit on the number of tap stations attached to

an LCC-HVDC system, a case study of an LCC-HVDC system with two VSC tapping stations is presented in [18]. However, the capacity of each of the taps is about 25% of the main system power rating which is well beyond the rated capacity of a tap, and therefore may be more accurately considered as low power-rated DC terminals. A review of recent HVDC system tapping converter topologies for both series and parallel configurations is presented in [23].

### 1.2.4 Supplementary Controllers

As the operation of taps may lead to disturbances to the HVDC system especially in the event of tap-side AC faults, supplementary controllers can be adopted to mitigate the stress on the HVDC system.

HVDC modulation controllers are utilized that transiently adjust the power/current reference signals to add synchronizing and damping torque to reduce the inter-area oscillations within multi-infeed HVDC systems [19], [20]. These controllers result in a better dynamic and fault recovery performance of multi-infeed HVDC systems. The idea of adopting global supplementary controllers to enhance the stability of a DC-segmented AC power system following AC system faults is presented in [21]. The supplementary controller dynamically modifies the reference values of the HVDC system controllers that can either confine the oscillatory disturbances within the faulted segment or transfer the oscillatory disturbances to other segments in a controlled manner. In addition, the idea of adopting a decentralized control scheme for multiple LCC-HVDC links with minimal communication infrastructure to prevent interactions between HVDC systems and to reduce the inter-area oscillations is proposed in [22]. To date, no work has employed HVDC supplementary controls as a solution to mitigating undesirable disturbances arising due to tapping stations.

## 1.3 Thesis Motivation

The vast majority of previous research has focused on HVDC tapping with one tap station using classical LCC-based technology schemes that have operational limitations and can be challenging to implement. This thesis proposes the tapping of existing LCC-HVDC systems with multiple FB-MMC converters to form a hybrid system that utilizes the benefits of both LCC and MMC topologies. As the operation of tap stations should not interfere with the main HVDC system, extensive simulations need to be conducted during both normal and abnormal conditions to verify the performance of the tap stations. Should the tap stations pose a detrimental impact on the main HVDC system performance, mitigation measures must be adopted to ensure the performance of the entire system.

## 1.4 Thesis Contribution

A hybrid study system comprised of two FB-MMC-based tapping stations interfaced to the well-known 1000 MW CIGRÉ LCC-HVDC benchmark model is developed in PSCAD/EMTDC to verify the technical feasibility of multiple tapping. The ability of taps to extract/inject power is verified through current set-point variations. This thesis further analyzes the impact of AC side faults at tapping stations on the operation of the main LCC-HVDC system. In addition, the impact of fault location on the severity of the resulting disturbances to the LCC-HVDC system is studied. Simulation results reveal undesirable disturbances in the DC link voltage/current of the main LCC-HVDC system due to AC side faults at tapping stations. Therefore, a tap station current modulation method that is based on local measurements is proposed to damp the oscillations. When an AC side fault occurs at one of the tap stations, the developed control method transiently adjusts the current set-point of the opposite MMC tap to reduce the resulting disturbances in the main HVDC system. The idea of supplementary controllers is also adopted at the LCC-HVDC rectifier and inverter stations to alleviate the impact of transients at tap stations on the main HVDC system.

# Chapter 2

# Modeling and Control of an LCC-HVDC System with Multiple Tapping Stations

This chapter introduces the basics of LCCs and MMCs, the developed hybrid LCC-MMC multi-tapping study system, converter controllers, and system parameters.

## 2.1 Converter Structure

This section provides an overview of the structure, operation, and control of the LCC and MMC HVDC systems.

### 2.1.1 Line Commutated Converter (LCC)

The basic structure of an LCC converter is a three-phase full-wave bridge (also known as the Graetz bridge), as shown in Fig. 2.1. The Graetz bridge consists of three single-phase legs each with an upper and a lower thyristor valve, and a large smoothing reactor ($L_d$) placed on the DC link to maintain a constant DC current. Since the control of a thyristor has only one degree of freedom (controlled turn-on capability), the magnitude of the instantaneous voltage ($v_d$) measured at the converter DC terminal is controlled by varying the firing instant of the thyristor valve. The switching of the DC current between AC phases from one thyristor valve to another on the same DC pole is referred to as commutation. Ideally, only one upper and one lower thyristor valves from the three legs conduct at the same time during commutation. Due to the unidirectional current conducting capability of the thyristor valves, the DC power reversal of a point-to-point LCC-HVDC system is achieved by reversing the polarity of the DC link voltage.

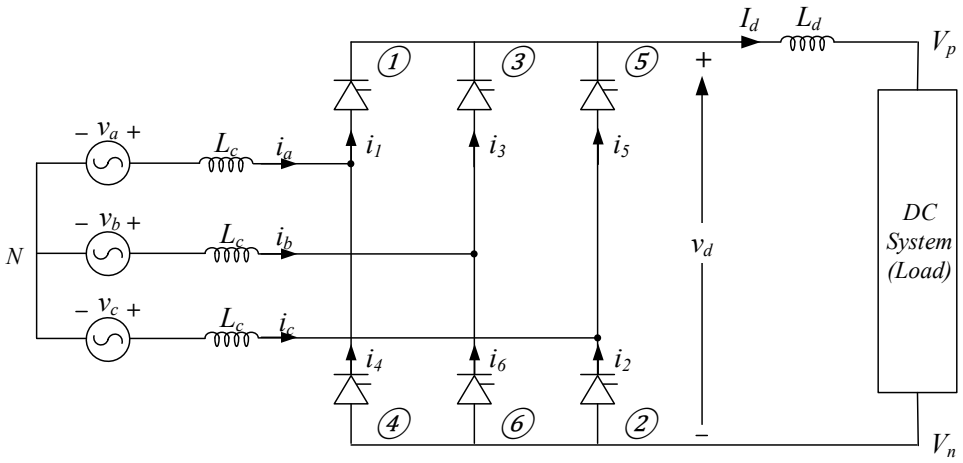



Figure 2.1: Graetz bridge

Fig. 2.2 depicts the operation of an LCC and the switching sequence of thyristor valves. Each thyristor valve conducts for 120°; therefore, six ripples are created in the DC voltage each AC cycle. The firing angle ($\alpha$) determines the firing instant of the thyristor valve, where $0° \leq \alpha \leq 90°$ (rectifier operation) and $90° \leq \alpha \leq 180°$ (inverter operation). With no ignition delay, the ideal no-load DC voltage ($V_{d0}$) is defined by (2.1) as a function of the AC line-to-line voltage. For rectifier operation, increasing $\alpha$ delays the ignition of the thyristor valve and reduces the rectifier average direct voltage ($V_{dr}$), as shown in (2.2). For inverter operation, increasing $\alpha$ increases the magnitude of the inverter average direct voltage ($V_{di}$) in the reverse polarity, as shown in (2.3). Due to the presence of the AC source inductance ($L_c$), the commutation between valves cannot be completed instantly and takes a finite time. Thus, the average DC voltage reduction during commutation can be modeled as a virtual commutating resistance ($R_c$) that consumes zero real power. The magnitude of the voltage drop depends on the DC link current ($I_d$).

$$V_{d0} = \frac{3\sqrt{2}}{\pi} E_{LL}, \tag{2.1}$$

$$V_{dr} = V_{d0r} cos\alpha_r - R_{cr} I_{dr}, \tag{2.2}$$

$$V_{di} = V_{d0i} cos\alpha_i - R_{ci} I_{di}, \tag{2.3}$$

where

$$R_{cr} = \frac{3}{\pi}\omega L_{cr} \text{ and } R_{ci} = \frac{3}{\pi}\omega L_{ci}. \tag{2.4}$$

The common practice of describing inverter operation is to use the extinction advance angle ($\gamma$). Thus, (2.3) can be represented as a function of $\gamma$. A similar equation for the inverter average voltage is defined by (2.5).

$$V_{di} = V_{d0i}\frac{(cos\alpha+cos\delta)}{2}. \tag{2.5}$$

(2.5) can be represented by (2.6).

$$V_{di} = -V_{d0i}\frac{(cos\beta+cos\gamma)}{2}, \tag{2.6}$$

where

$$cos\alpha = -cos\beta, \tag{2.7}$$

$$cos\delta = -cos\gamma. \tag{2.8}$$

The commutating current relation expressed by (2.9) is then substituted into (2.6) to derive the inverter average direct voltage as a function of $\gamma$, as shown in (2.10).

$$I_{di} = \frac{\sqrt{3}E_{LL}}{2\omega L_{ci}}(cos\gamma - cos\beta), \tag{2.9}$$

$$V_{di} = V_{d0i}cos\gamma - R_{ci}I_{di}. \tag{2.10}$$

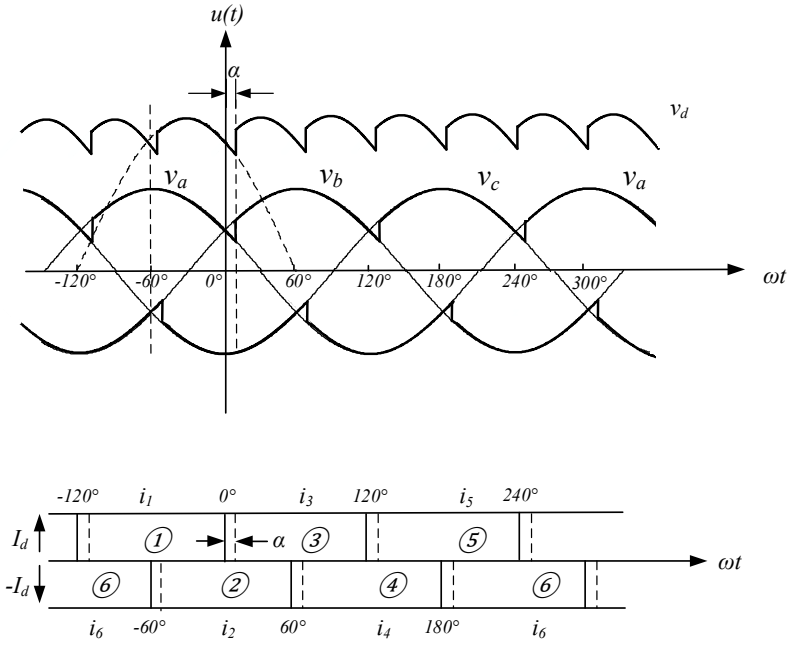



Figure 2.2: LCC operation

In practice, two Graetz bridges are connected in series to form a 12-pulse bridge, as seen in Fig. 2.3, to increase the DC link voltage and to reduce the AC side and DC side harmonics. By phase shifting the AC voltage supplied to the two bridges by 30° through the use of *Y*-Δ and *Y*-*Y* transformers, the odd multiples of the sixth harmonic in the DC voltage, and the $6n \pm 1^{th}$ voltage harmonics on the AC side are effectively eliminated for $n \in \{Z^+\}$. This improves the quality of the output waveform and reduces the need for harmonic filters.

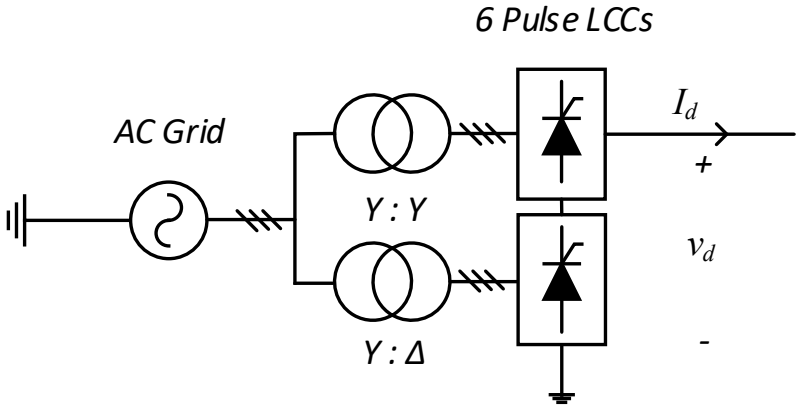



Figure 2.3: 12 pulse bridge

### 2.1.2 Modular Multilevel Converter (MMC)

The basic structure of an MMC consisting of three phase legs, each containing an upper and a lower arm (i.e., valve), is shown in Fig. 2.4. Each arm contains N number of series stacked SMs. The number of SMs dictates the number of output voltage steps and may vary from tens to hundreds depending on the power rating and the specific application. With N number of SMs, the MMC is capable of producing N+1 output voltage levels. Each arm also consists of an arm inductor ($L_s$) to facilitate the flow of current and to limit the rate of change of the arm current. $R_s$ models the arm inductor resistance. The sum of voltage drop across the two arm inductors as well as the associated inductor resistances plus the upper and lower arm voltages ($v_{uj}$, $v_{lj}$) equals to the DC link voltage ($v_d$) applied across each phase leg for $j \in \{a, b, c\}$. The AC terminal is attached to the mid-point of each phase leg ($v_{toj}$), and the AC output voltage is measured with respect to the ground. The MMC model in this thesis adopts a monopole configuration with the negative DC pole grounded, thus, creating a DC offset in the AC output voltage which is eliminated through the AC transformer.

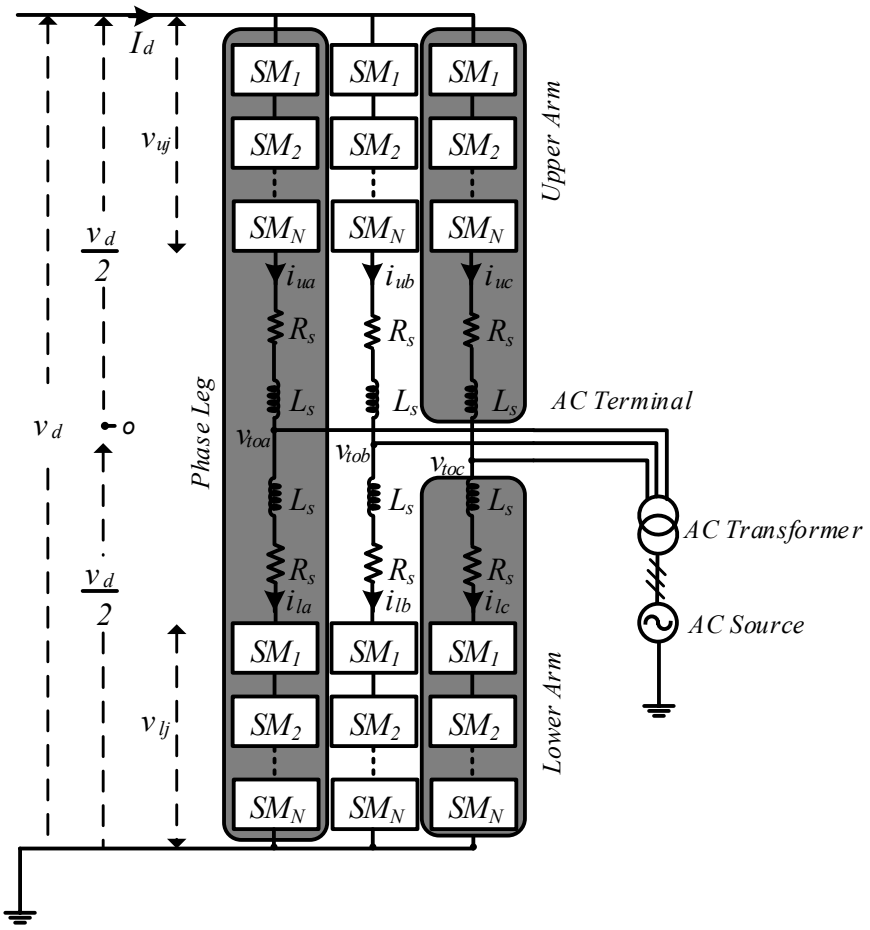



Figure 2.4: Three phase MMC structure

The HBSMs and FBSMs are the two common SM topologies consisting of different number of IGBTs and a cell capacitor to generate the desired DC and AC voltages. The HBSM is only capable of generating two voltage levels including the $+V_{cap}$ and zero. The FBSM can produce three voltage levels, namely the $\pm V_{cap}$ and zero. FBSMs also accommodate for DC link voltage reversal by generating a negative output voltage and are capable of blocking DC faults. Therefore, FBSMs are used in tapping stations in this thesis. The SM is "inserted" when it outputs $\pm V_{cap}$ and is "bypassed" when its output voltage is zero. The switching states of the FBSM are outlined in Table 2.1 and the current path for each of the switching states is displayed in Fig. 2.5. Similar switching states and current paths can be derived for reversed arm current conditions.

Table 2.1: FBSM switch states

| S1 | S2 | S3 | S4 | $V_{SM}$ |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 | $V_{cap}$ |
| 0 | 1 | 1 | 0 | $-V_{cap}$ |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |

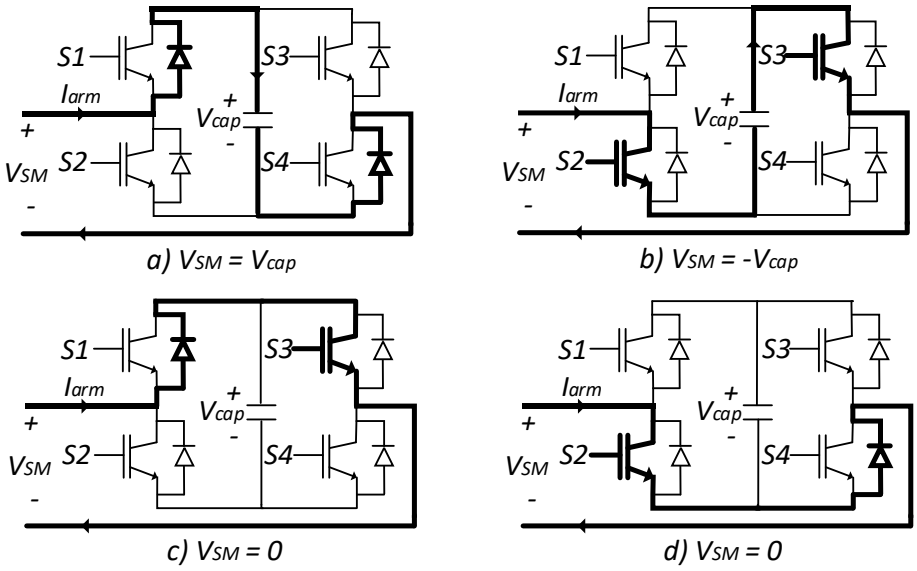



Figure 2.5: FBSM switching states (drawn for positive arm currents)

As the cell capacitor voltage directly affects the output voltage, the cell capacitance should be selected such that it is large enough to limit the DC voltage ripple under normal/transient conditions and to reduce the magnitude of DC current harmonics, yet not too large to ensure fast control of DC voltage at a reasonable cost [24]. A practical formula for selecting capacitor size is given in (2.11) where $C_{SM}$ is the capacitance for each individual cell capacitor, *EP* is the energy to power ratio which is typically between 30-40 kJ/MVA, *S* is the nominal power rating of the converter, *p* is the number of phases, *N* is the number of SMs per arm, and $V_{SM}$ is the nominal voltage for each individual cell capacitor.

$$C_{SM} = \frac{EP*S}{p*N*{V_{SM}}^2}. \tag{2.11}$$

Each arm current is composed of a DC component, an AC fundamental component, and harmonic components. The DC component current flows through each phase leg and is of the same polarity for both the upper and lower arms. Since the DC component current is common for both arms, it can be represented by the common mode current ($I_{comj}$) and calculated from the upper arm and the lower arm currents ($i_{uj}$, $i_{lj}$) in Fig. 2.4, as shown in (2.12). The sum of the common mode current from all three phase legs is the DC link current. The AC fundamental component of the upper and the lower arms are of the same magnitude but 180° out of phase, which can be represented by the differential mode current ($I_{diffj}$), as defined in (2.13).

$$I_{comj} = \frac{i_{uj}+i_{lj}}{2}, \tag{2.12}$$

$$I_{diffj} = \frac{i_{uj}-i_{lj}}{2}. \tag{2.13}$$

A general assumption in performing MMC analysis is that the voltage of all the cell capacitors is well-balanced and similar in magnitude. To fully utilize the functionalities of an FB-MMC, the sum of the cell capacitor voltages of each upper and lower arm within a phase leg must be equal or greater than the DC link voltage to ensure adequate headroom. Since each phase leg has to support the full DC link voltage, the sum of the number of SMs inserted from the upper arm and the lower arm within a phase leg must equal to N at all times. The MMC AC output voltage is achieved by varying the number of inserted and bypassed SMs within a phase leg. For example, to increase the AC output voltage, additional SMs in the lower arm may be inserted and the same number of SMs in the upper arm must be bypassed to change the voltage at the AC terminal yet maintaining the total number of inserted SMs equal to N. The upper and lower arm voltages are defined in (2.14) and (2.15), respectively, where $v_{uj}$ and $v_{lj}$ are the upper and lower arm voltages, $V_{rated}$ is the sum of the cell capacitor voltage within an arm, $d_{comj}$ is the DC offset, and $d_{diffj}$ is the AC duty cycle for $j \in \{a, b, c\}$.

$$v_{uj} = V_{rated} * (d_{comj} - d_{diffj}), \tag{2.14}$$

$$v_{lj} = V_{rated} * (d_{comj} + d_{diffj}). \tag{2.15}$$

$d_{diffj}$ is mainly a sinusoidal function, as represented by (2.16). $d_{1j}$ and $\theta_j$ are generated by the AC current control loop to achieve the desired AC voltage magnitude and phase. $d_{comj}$ is the

summation of the offset signal ($D_{comj}$) and minor variation terms to achieve specific control goals, as shown in (2.17). $D_{comj}$ is often a constant whereas the variation term in this case ($d_{com2j}$) is a sinusoidal function at twice the AC system frequency with parameters ($d_{2j}$ and $\theta_{2j}$) to reduce the circulating current within MMC legs, as shown in (2.18). $D_{comj}$ is generated by the arm sum capacitor voltage controller such that the sum of the upper and lower arm voltages plus the voltage drop of the two arm inductors equals to the DC link voltage. Under reduced DC voltage conditions, $D_{comj}$ is reduced to decrease the total number of inserted SMs within a phase leg. For reversed DC voltage conditions, $D_{comj}$ is reversed to command the SMs to produce negative voltages.

$$d_{diffj} = d_{1j} * sin(\omega t + \theta_j), \tag{2.16}$$

$$d_{comj} = D_{comj} + d_{com2j}, \tag{2.17}$$

where

$$d_{com2j} = d_{2j} * sin(2\omega t + \theta_{2j}). \tag{2.18}$$

Several common modulation schemes for MMCs include sinusoidal pulse-width modulation (PWM), carrier-disposition PWM, phase-shift carrier-based PWM, and nearest level modulation (NLM) [25]. The NLM directly calculates the number of SMs to be inserted from the modulation signal which is easy to implement and especially suitable for MMCs with a large number of SMs; thus, NLM is adopted in the MMC model presented in this thesis.

As the arm SMs are constantly inserted and bypassed, a capacitor voltage balancing algorithm is essential to ensure the even distribution of cell capacitor voltages. Failure to balance the capacitor voltages will lead to output voltage distortions and equipment damages. The voltage deviation in a cell capacitor depends on its switching states and the direction of the arm current. When a cell capacitor is bypassed, its voltage remains constant. On the other hand, when a cell capacitor is inserted, a positive (negative) arm current will charge (discharge) the capacitor and increase (decrease) the capacitor voltage. Thus, a capacitor voltage balancing algorithm constantly sorts cell capacitor voltages within an arm and inserts the cell capacitors with lower (higher) voltages when the arm current is positive (negative) based on the calculated number of SMs to be inserted. Reference [26] presents a detailed analysis of MMC operation and modeling, capacitor voltage balancing algorithms, and switching strategies.

## 2.2 Hybrid Study System

Fig. 2.6 shows the configuration of the proposed test system consisting of two FB-MMC-based parallel taps incorporated into the well-known CIGRÉ LCC benchmark model [27]. The developed system in PSCAD/EMTDC with two MMC stations tapped to the LCC-HVDC system constitutes a hybrid LCC-MMC multi-tapping study system. The two MMC taps denoted as MMC-1, MMC-2 are shunt connected to the DC line at distances 75 km and 25 km away from the LCC rectifier station. Each MMC tap is connected to its local system by a 5 km AC overhead line. Fig. 2.7 depicts the control structure of the study system. The LCC rectifier/inverter controller, MMC tap controller, and master controller enclosed in the red dotted boxes are discussed in detail in this section. The blue dashed lines represent the signals that need to be communicated between converter stations.

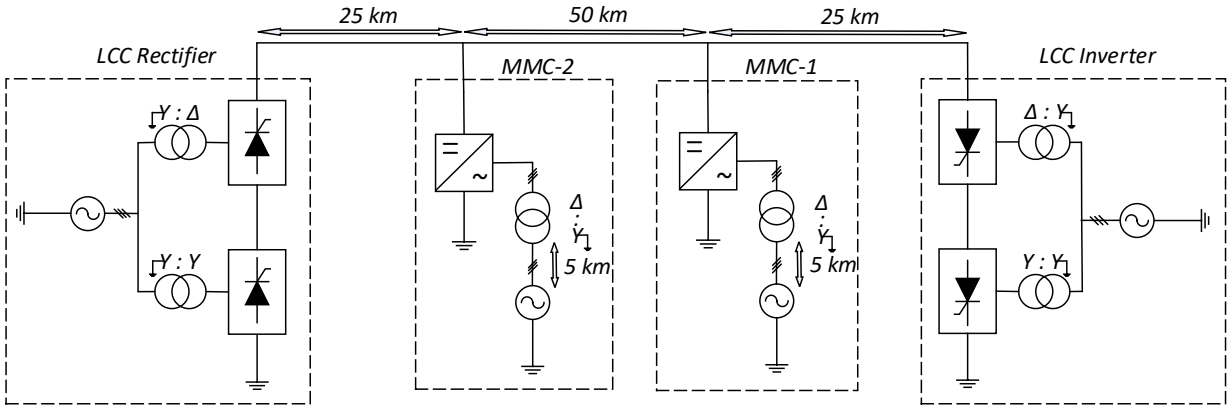



Figure 2.6: System configuration

### 2.2.1 CIGRÉ LCC Benchmark Model and Control

The CIGRÉ LCC benchmark model features a monopole asymmetrical network based on the 12-pulse bridge configuration for 1000 MVA at 500 kV. The current order (CO) at the inverter side generates the DC link current reference for both LCC stations. Under normal operation, the LCC rectifier operates in constant current (CC) mode to regulate the DC current and the inverter adopts the constant extinction angle mode (CEA) to set the DC link voltage. An LCC normally operates at low rectifier ignition angle and inverter extinction angle to maintain a high power factor, thus reducing the amount of reactive compensation. The rectifier ignition angle is typically maintained between 10° and 20°, and the inverter extinction angle reference is set to 15°. The

LCC-HVDC system also utilizes the voltage-dependent current order limit (VDCOL) control and the mode stabilizer to prevent excessive reactive power demand and oscillations between operating modes when a disturbance causes a sag in either the DC link voltage or the AC side voltage. If the LCC rectifier fails to regulate the DC current and reaches the minimum ignition angle (CIA), the inverter will take over the current controlling role as the DC link current falls below the rectifier current order by the current margin (CM). The LCC-HVDC system control characteristic is depicted in Fig. 2.8. The detailed system parameters of the benchmark model and the associated control characteristics can be found in [27].

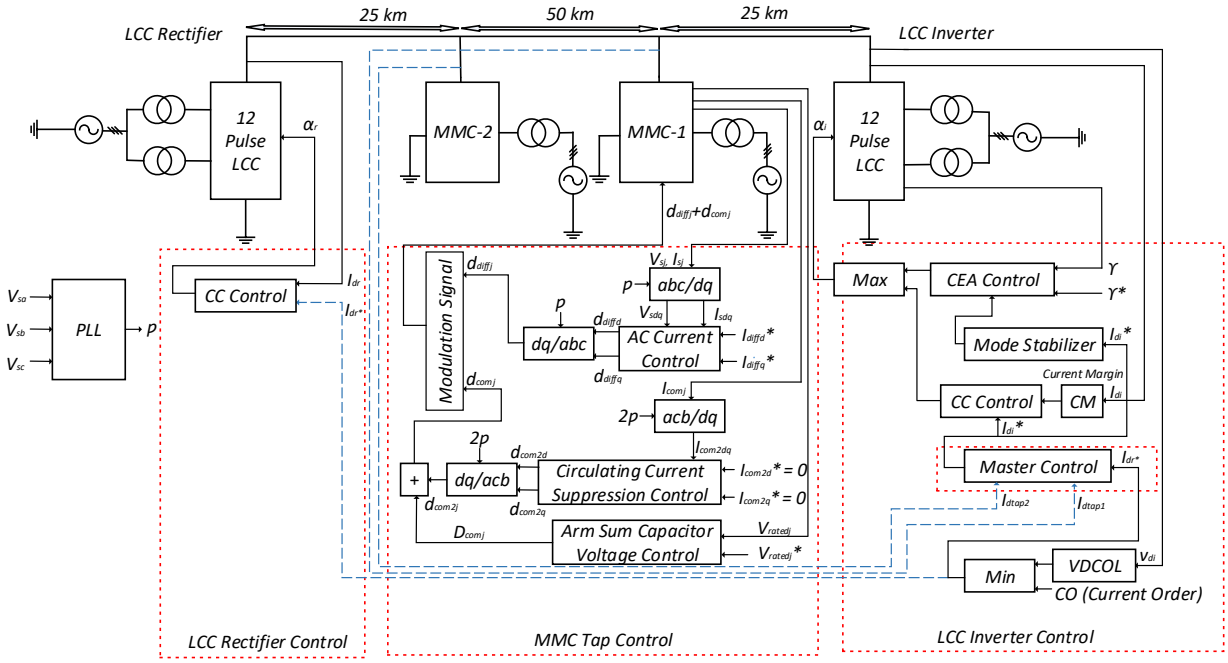



Figure 2.7: Study system control structure

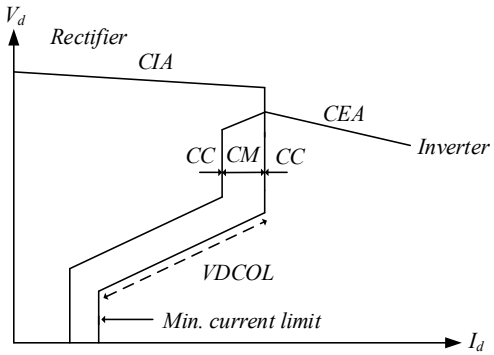



Figure 2.8: LCC-HVDC system control characteristic [27]

### 2.2.2 MMC Model and Control

As the power rating of a tap should be limited to around 5% of the main HVDC system rating, the power rating of each of the two asymmetric MMC taps are restricted to 50 MVA at 500 kV, but are designed for 100 MVA to maximize the flexibility of future studies. The MMC model in PSCAD/EMTDC adopts the detailed equivalent circuit model proposed in [28]. This circuit model simplifies each MMC arm to an equivalent Thevenin circuit to reduce the simulation time yet maintaining accurate system responses under AC and DC faults. The MMC parameters are given in Table 2.2. The MMC adopts the AC current control loop, the circulating current suppression controller (CCSC), and the arm sum capacitor voltage controller.

Table 2.2: MMC specification

| **Parameter** | **Value** |
|---|---|
| AC source voltage (L-L,rms), frequency | 42 kV, 50 Hz |
| Transformer winding configuration, voltage ratio (L-L rms) | Yg / Δ, 42:270 kV |
| Transformer rating, leakage reactance | 100 MVA, 15% |
| Number of submodules per arm, submodule capacitance | 312, 2.8 mF |
| Nominal submodule capacitor voltage | 1.6 kV |
| Arm inductance, arm resistance | 50 mH, 0.5 Ω |
| Rated DC voltage and Power | 500 kV, 100 MVA |

#### 2.2.2.1 AC Current Control Loop

The AC current control loop regulates the current injection into the local AC grid in the synchronous rotating frame (dq frame) to reduce the number of control variables and to achieve decoupled power flow control as shown in Fig. 2.9 [29]. The conversion between the natural frame (abc frame) and dq frame quantities are achieved by the embedded Park's transformation in the abc/dq and dq/abc blocks. The system synchronization of the dq quantities to the AC system frequency and phase is done by a phase-locked loop (PLL) that measures the instantaneous phase angle ($\rho$) of the AC system. The PLL is designed to align the space phasors to the d-axis resulting in a zero q-axis quantity to decouple the active and reactive power controls. The two control references ($I_{diffd}{}^{*}$, $I_{diffq}{}^{*}$) are used to set the desired flow of real and reactive power, respectively.

The outputs of the proportional-integral (PI) controllers are compensated with cross-decoupling feed-forward terms ($I_{sd}\omega_0 L$ and $I_{sq}\omega_0 L$) and feed-forward voltages ($V_{sd}$ and $V_{sq}$) to improve the dynamic performance of the controllers. The resulting dq frame AC duty cycles ($d_{diffd}, d_{diffq}$) are then converted back to the natural frame quantities ($d_{diffa}, d_{diffb}, d_{diffc}$) to generate the desired MMC AC voltages ($V_a, V_b, V_c$) based on the AC peak voltage ($v_{s_{peak}}$) and the DC link voltage ($v_d$). The MMC AC system dynamic is also shown in Fig. 2.9 to demonstrate the relationship between the MMC AC output voltages and the AC phase currents in the dq frame.

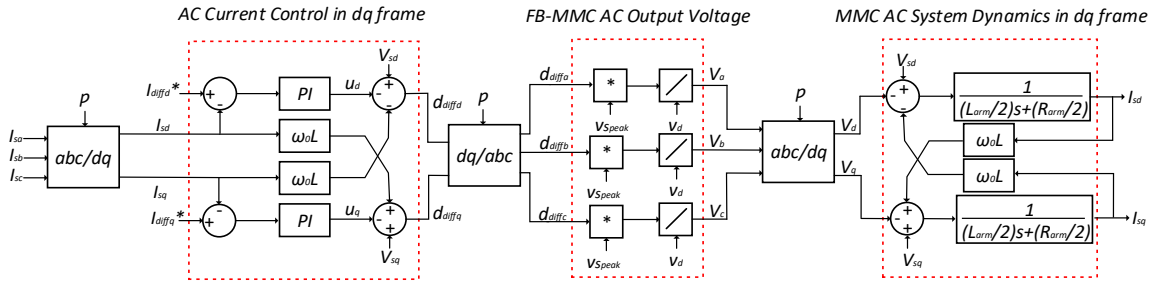



Figure 2.9: AC current controller [29]

### 2.2.2.2 Circulating Current Suppression Controller (CCSC)

During normal operation, the instantaneous imbalance of cell capacitor voltages causes circulating currents to flow through the three-phase legs. Such a current flow increases the magnitude of arm currents, capacitor voltage ripples, converter losses, and distorts the arm currents. Thus, the CCSC proposed in [30] (Fig. 2.10) is utilized to mitigate the negative sequence second harmonic current inherently induced in MMC legs. The dq frame common mode currents ($I_{com2d}, I_{com2q}$) are regulated to zero through PI controllers and compensated with cross-decoupling feed-forward terms ($I_{comd}2\omega_0 L$ and $I_{comq}2\omega_0 L$) to improve the dynamic performance. The generated natural frame CCSC modulation signals ($d_{com2j}$) are then utilized to generate the MMC DC offset.

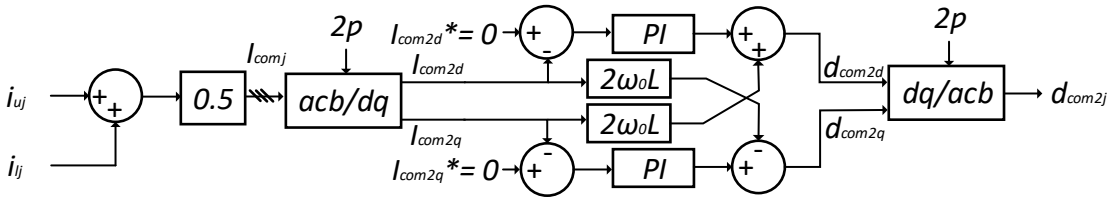



Figure 2.10: CCSC controller [30]

### 2.2.2.3 Arm Sum Capacitor Voltage Controller

The arm sum capacitor voltage controller regulates the sum of the arm capacitor voltages within an arm to its nominal value, as shown in Fig. 2.11. The arm capacitor voltage reference ($V_{ratedj}{}^{*}$) is set to the nominal DC voltage (500 kV) for all phases. The average arm voltage ($V_{ratedj}$) is calculated from the upper/lower arm capacitor voltages ($V_{rated\_uj}$, $V_{rated\_lj}$). The PI controller regulates the average arm voltage error ($V_{error}$) to generate a common mode current reference ($I_{comj}{}^{*}$) such that a positive error would increase the common mode current reference to charge the capacitor whereas a negative error would decrease the common mode current reference to discharge the capacitor. The measured common mode current is then regulated by a PI controller to the common mode current reference and compensated by the measured DC voltage and the arm capacitor voltage reference to generate the offset signal ($D_{comj}$).

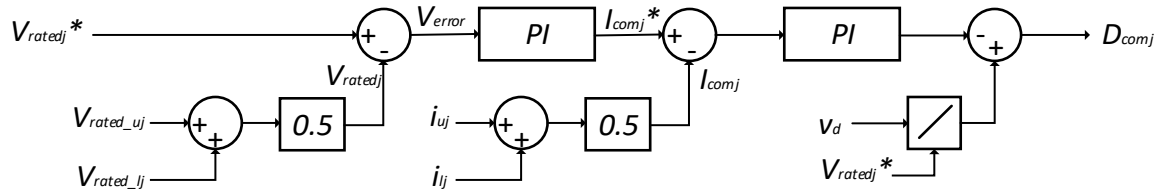



Figure 2.11: Arm sum capacitor voltage controller

The offset signals ($D_{coma}$ , $D_{comb}$ , $D_{comc}$) and the CCSC modulation signals ($d_{com2a}$ , $d_{com2b}$ , $d_{com2c}$) are then summed to generate the MMC DC offsets ($d_{coma}, d_{comb}, d_{comc}$).

### 2.2.3 Master Controller

As the current extracted/injected by the taps causes a current imbalance in the LCC rectifier and inverter stations, a master controller is implemented to adjust the current order of the inverter station taking the tap currents into consideration as shown in Fig. 2.12. The inverter current margin may be further adjusted to accommodate the current contribution from the taps and to prevent unnecessary switching oscillations between primary CEA and backup CC modes within the inverter.

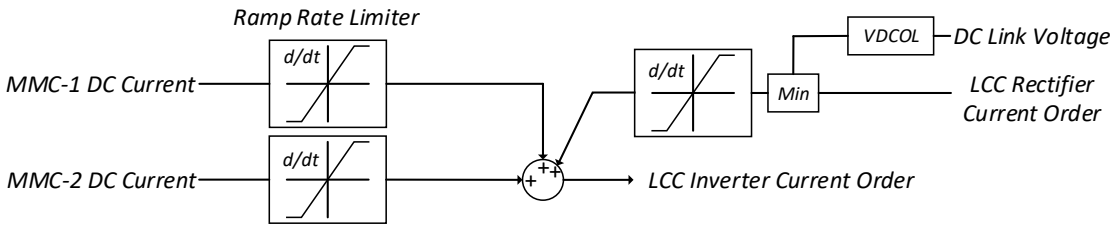



Figure 2.12: Master controller

## 2.3 Summary

This chapter provides an overview of the operation and control of LCCs and MMCs and introduces the developed hybrid study system and the associated system parameters. The developed study system will be used in chapters 3 and 4 to carry out technical feasibility studies and performance analysis of the LCC-HVDC system with multiple tap stations as well as to verify the effectiveness of the developed fault mitigating schemes.

# Chapter 3

# Analysis and Simulation of Tap Stations Operation

This chapter analyzes the technical feasibility of multi-converter tapping and the impact of MMC taps on the main LCC-HVDC system during both normal and fault conditions, through extensive simulations in PSCAD/EMTDC. The configuration of the study system is shown in Fig. 3.1. The conformity of the LCC-HVDC system dynamic performance to the main design goals of tapping with multiple stations operating simultaneously is studied with selected cases. The per unit system is adopted with base values of $S_{b3\emptyset}$ =1000 MVA and $V_{bLL}$ = 500 kV.

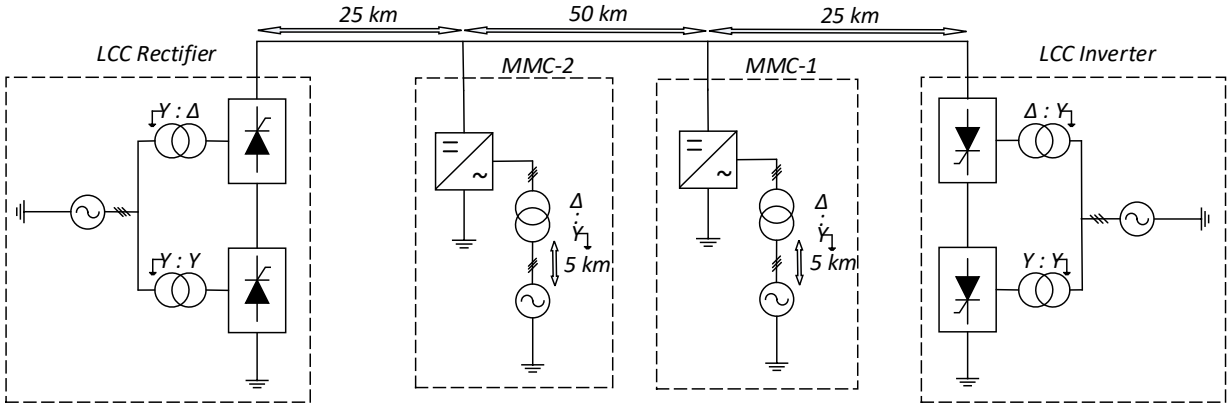



Figure 3.1: System configuration

## 3.1 Normal Operation

The operation of MMC taps under various disturbances such as variations in the tap station DC current set-point, AC grid reactive power compensation, current reversal, and different current ramp rates is evaluated. The performance of the tap stations and their associated impact on the LCC-HVDC system are discussed. As the energization of MMC taps has been reported in the literature [18], the MMC taps in this section are assumed to be pre-charged to the nominal voltage (500 kV) before the disturbances are applied.

### 3.1.1 MMC Tapping Current Set-point Change (Power Extraction)

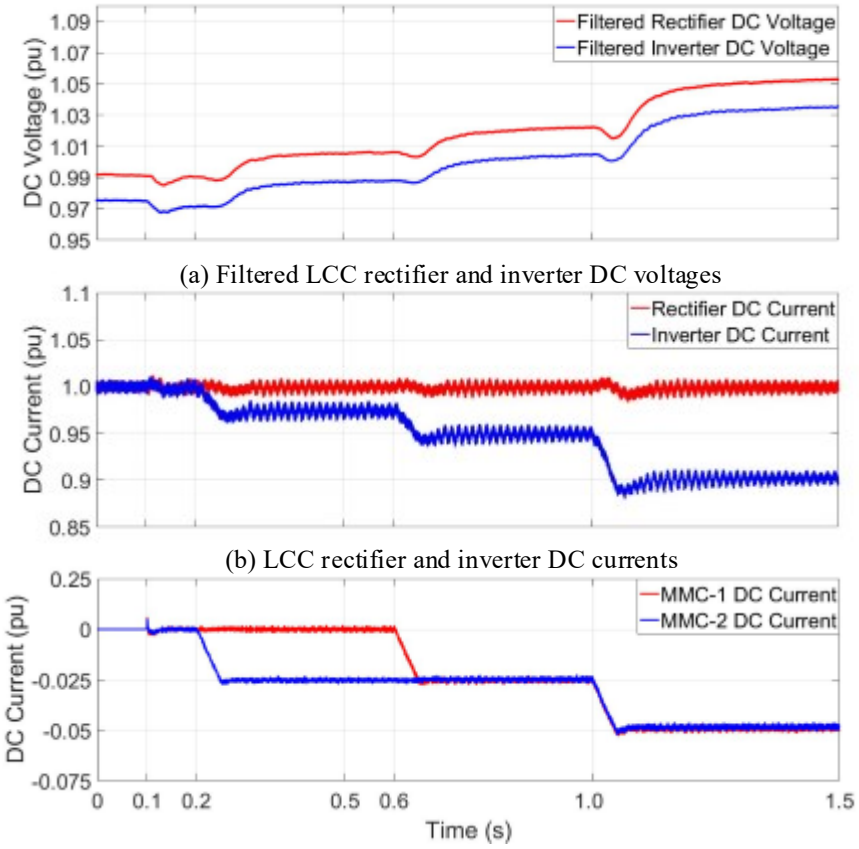
Simulation results shown in Fig. 3.2 demonstrate the current tapping capability of multiple tap stations when the DC current reference of i) each of the taps individually, or ii) two taps simultaneously is changed.

The sequence of operations is listed below:

- Initially, 1 pu of DC current is transferred from the LCC rectifier to the inverter.
- MMC-1 and MMC-2 are de-blocked at t = 0.1 s. The initial current reference of each tap is 0 pu.
- At t = 0.2 s, current reference of MMC-2 is changed to -0.025 pu such that the tap extracts about 25 MW from the DC system.
- At t = 0.6 s, current reference of MMC-1 is changed to -0.025 pu such that the tap extracts about 25 MW from the DC system.
- At t = 1.0 s, current reference of both MMC-1 and MMC-2 are set to -0.05 pu to extract 100 MW in total from the DC system.

At t = 0.1 s, the de-blocking of the taps results in no significant disturbances on the LCC-HVDC system currents, but leads to a temporary 0.5% DC voltage dip in the LCC rectifier and inverter that lasts for 70 ms. At t = 0.2 s, MMC-2 current ramps down at a rate of 0.5 pu/s to -0.025 pu, as shown in Fig. 3.2(c). The inverter DC current also drops to 0.975 pu whereas the rectifier DC current remains at 1pu, Fig. 3.2(b). A current oscillation of about 2% appears in the LCC rectifier and inverter currents, which is due to the mode stabilizer embedded in the inverter. The steady-state rectifier and inverter DC voltages also increase by approximately 1.7%, as

depicted in Fig. 3.2(a). As the LCC inverter operates in the CEA control mode, the commutating resistive voltage drop reduces as the inverter current decreases; therefore, the DC link voltage increases as the extinction angle is held constant. Thus, the voltage swell is not considered as a disturbance caused solely by the MMC taps. At t = 0.6 s, the current reference of MMC-1 ramps down to -0.025 pu. The operation of MMC-1 does not affect MMC-2, Fig. 3.2(c). No noticeable adverse effect on the LCC-HVDC system is observed apart from the 1% dip in the LCC inverter DC current to 0.94 pu. As a consequence of the reduction in steady-state LCC inverter current to 0.95 pu, the LCC rectifier and inverter DC voltages are further increased to 1.02 pu and 1.005 pu, respectively. At t = 1.0 s, the current reference of both MMCs is reduced simultaneously, and a marginally higher DC current dip occurs at the LCC inverter due to the combined current extraction from two MMC taps. The LCC inverter steady-state DC current is reduced to 0.9 pu whereas the rectifier current remains at 1 pu. The further reduction in the inverter DC current causes a 3% increase in the LCC rectifier and inverter DC voltages.




(a) Filtered LCC rectifier and inverter DC voltages

(b) LCC rectifier and inverter DC currents

(c) MMC-1 and MMC-2 DC currents

Figure 3.2: System performance under current set-point variation (power extraction)

It can be concluded that de-blocking and current set-point variations (power extraction) of MMC tap stations do not lead to LCC-HVDC system oscillations or instability, thus the feasibility of using double tap stations to extract a limited range of power (up to 5% of the LCC link capacity per tap station) from the LCC-HVDC system is verified.

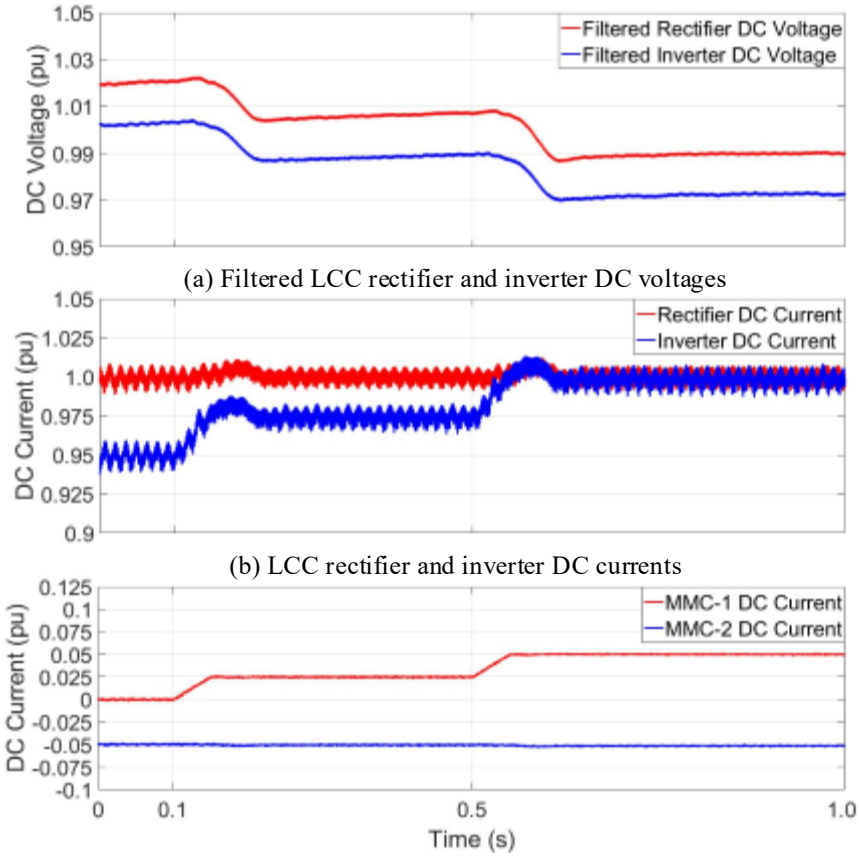
### 3.1.2 MMC Tapping Current Set-point Change (Power Injection)

The results in section 3.1.1 focused on extracting DC current from an existing LCC-HVDC system via taps. However, considering the potential for RESs commissioned around the taps, the bidirectional power flow capability of MMC-based taps can be utilized to inject the surplus power back into the LCC-HVDC system. This section examines the notion of injecting DC current into an existing LCC-HVDC system via MMC taps to facilitate future integration of RESs.

The sequence of operation of MMC taps during this test is listed below:

- Initially, the LCC rectifier and MMC-1 inject 1 pu and 0 pu of DC current, respectively; the LCC inverter and MMC-2 extract 0.95 pu and 0.05 pu of DC current, respectively.
- At t = 0.1 s, MMC-1 current reference is changed to 0.025 pu to inject about 25 MW to the DC system, and to mimic the integration of RESs.
- At t = 0.5 s, MMC-1 current reference is changed to 0.05 pu to inject about 50 MW to the DC system, and to supply MMC-2 total power.

At t = 0.1 s, MMC-1 DC current is increased to 0.025 pu at a ramp rate of 0.5 pu/s, Fig. 3.3(c). The injected tap current leads to an increase in the LCC inverter DC current from 0.95 pu to 0.975 pu, and negligible impact is imposed on the LCC-HVDC system currents as shown in Fig. 3.3(b). As a result of the increase in the inverter current, a DC voltage reduction is observed in Fig. 3.3(a), which can be counteracted by the operation of inverter AC side tap changer. At t = 0.5 s, as the MMC-1 current ramps up to the same value as the current drawn by MMC-2, the current transferred between the MMC taps is independent of the LCC-HVDC system, and the transferred current does not affect the operation of the LCC-HVDC system. The ability of MMC taps to facilitate the integration of RESs by injecting DC current into the LCC-HVDC system is therefore verified.




(a) Filtered LCC rectifier and inverter DC voltages

(b) LCC rectifier and inverter DC currents

(c) MMC-1 and MMC-2 DC currents

Figure 3.3: System performance under current set-point variation (power injection)

### 3.1.3 MMC Reactive Power Compensation

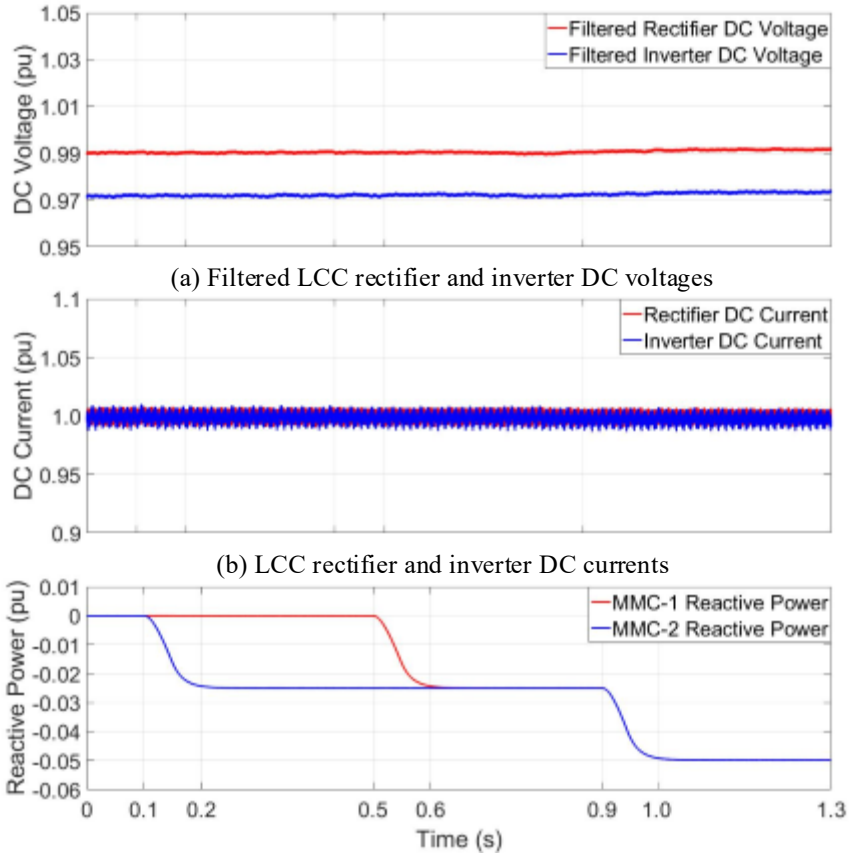
One of the main advantages of MMCs over LCCs is the ability to independently regulate active and reactive power outputs. Thus, an MMC tap can also operate as a static synchronous compensator (STATCOM) to inject or extract reactive power to the tap station AC grid to provide voltage regulation. In this section, the ability of MMC taps to inject reactive power into its associated AC grid is verified.

The sequence of operations is as follows:

- Initially, 1 pu of DC current is transferred from the LCC rectifier to the inverter with the MMC taps current reference set to 0 pu.
- At t = 0.1 s, current reference of MMC-2 is adjusted such that the tap injects about 25 MVar to its AC grid.

- At t = 0.5 s, current reference of MMC-1 is adjusted such that the tap injects about 25 MVar to its AC grid.
- At t = 0.9 s, current reference of both MMC-1 and MMC-2 are adjusted such that each tap injects 50 MVar to its AC grid.

At t = 0.1 s, MMC-2 current ramps down at a rate of 0.5pu/s to -0.025 pu to inject 25 MVar to the local AC grid, Fig. 3.4(c). From Fig. 3.4(b), it is observed that the LCC rectifier and inverter DC currents remain at 1 pu regardless of the amount of reactive power compensation provided to the grid. The magnitude of the rectifier and inverter DC voltages also remain unchanged, as shown in Fig. 3.4(a). At t = 0.9 s, the current reference of both MMCs ramps down to -0.05 pu simultaneously with each tap injecting 50 MVar into its AC grid, Fig. 3.4(c). No adverse effect is observed in the LCC-HVDC system operation, thus demonstrating the reactive power compensating capability of MMC taps.




(a) Filtered LCC rectifier and inverter DC voltages

(b) LCC rectifier and inverter DC currents

(c) MMC-1 and MMC-2 reactive power

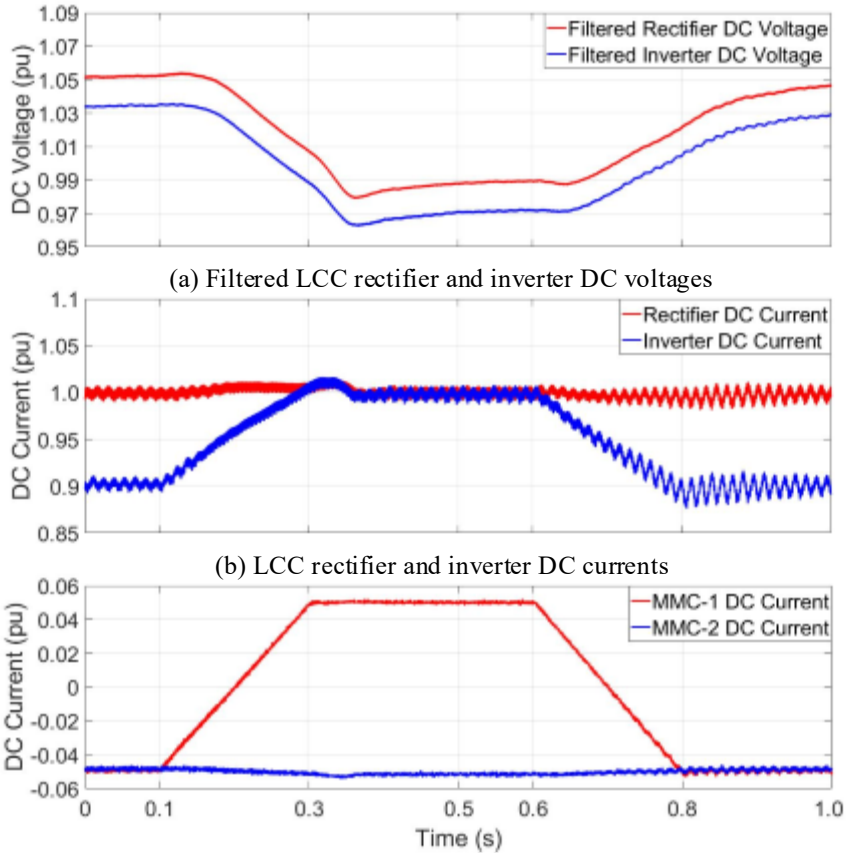
Figure 3.4: System performance in STATCOM mode

### 3.1.4 MMC Tap Current Reversal

With the increasing number of installed distributed energy resources (DERs), the transfer of electric power in the near future will be highly flexible, and power reversals in taps may occur frequently to meet the scheduled power dispatch. This section focuses on verifying the ability of the taps to switch between current injection and current extraction modes. The impact of such tap station current reversals on the LCC-HVDC system is shown in Fig. 3.5.

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, and MMC-2 extract 0.9 pu, 0.05 pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, MMC-1 current reference is changed to 0.05 pu to inject about 50 MW to the DC system.
- At t = 0.6 s, MMC-1 current reference is changed to -0.05 pu to extract about 50 MW from the DC system.

At t = 0.1 s, the current reference of MMC-1 ramps up from -0.05 to 0.05 pu at a rate of 0.5 pu/s to switch from the power extraction mode to power injection mode. The process of current reversal is completed at t = 0.3 s, when the LCC inverter and MMC-1 currents reach 1 pu and 0.05 pu, respectively. A current overshoot of 1% is observed at the LCC inverter station, as shown in Fig. 3.5(b). As a result of the increase in the LCC inverter current and the CEA control mode adopted by the inverter, the rectifier and inverter DC voltages are reduced, as shown in Fig. 3.5(a). At t = 0.6 s, the current reference of MMC-1 ramps down from 0.05 to -0.05 pu at 0.5 pu/s to change the power flow direction. As the LCC inverter current is decreased, a high-frequency oscillation of 3% occurs in both the LCC rectifier and inverter currents. The oscillation is mainly caused by the implementation of the mode stabilizer in the inverter, which can be significantly improved by redesigning of the mode stabilizer. The ability of MMC taps to provide bidirectional power/current is verified via the aforementioned test. The power reversal does not result in significant disturbances in the LCC-HVDC system operation.




(a) Filtered LCC rectifier and inverter DC voltages

(b) LCC rectifier and inverter DC currents

(c) MMC-1 and MMC-2 DC currents

Figure 3.5: System performance during power reversal

### 3.1.5 Current Ramp Rate

This section explores the impact of different MMC tap current ramp rates on the performance of LCC-HVDC systems. A typical HVDC system start-up power ramp rate of 600 MW/s is suggested in [31], which is equivalent to a current ramp rate of 0.6 pu/s. However, during contingencies, the ramp rate may be higher to assist the recovery of HVDC systems. Therefore, four current ramp rates 0.25 pu/s (case 1, about 250 MW/s), 0.5 pu/s (case 2, about 500 MW/s), 1 pu/s (case 3, about 1000 MW/s), and 2 pu/s (case 4, about 2000 MW/s), are studied.

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, and MMC-2 extract 0.9 pu, 0 pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, current reference of MMC-1 is changed to -0.05 pu to extract about 50 MW from the DC system.

Fig. 3.6(e) shows that a faster ramp rate results in a larger temporary tap current dip. From Figs. 3.6(a) and (b), it is observed that a faster current ramp allows for the LCC rectifier and inverter stations to quickly reach steady-state, but at the cost of higher initial DC voltage dips due to the limited response speed of the LCC rectifier and inverter controllers. The DC voltage dip leads to an overshoot in the current of the LCC rectifier as shown in Fig. 3.6(c). Moreover, the magnitude of the current overshoot is directly related to the extent of the voltage dip which increases with the ramp rate. Referring to Fig. 3.6(d), the LCC inverter DC current reaches steady-state faster with a higher ramp rate; however, this results in a larger current dip at the inverter station.

It is concluded that higher ramp rates allow the LCC-HVDC system to reach the steady-state faster, but will negatively affect the transient response of the system. Thus, it is important to select a ramp rate which results in a fast system response and acceptable transients.

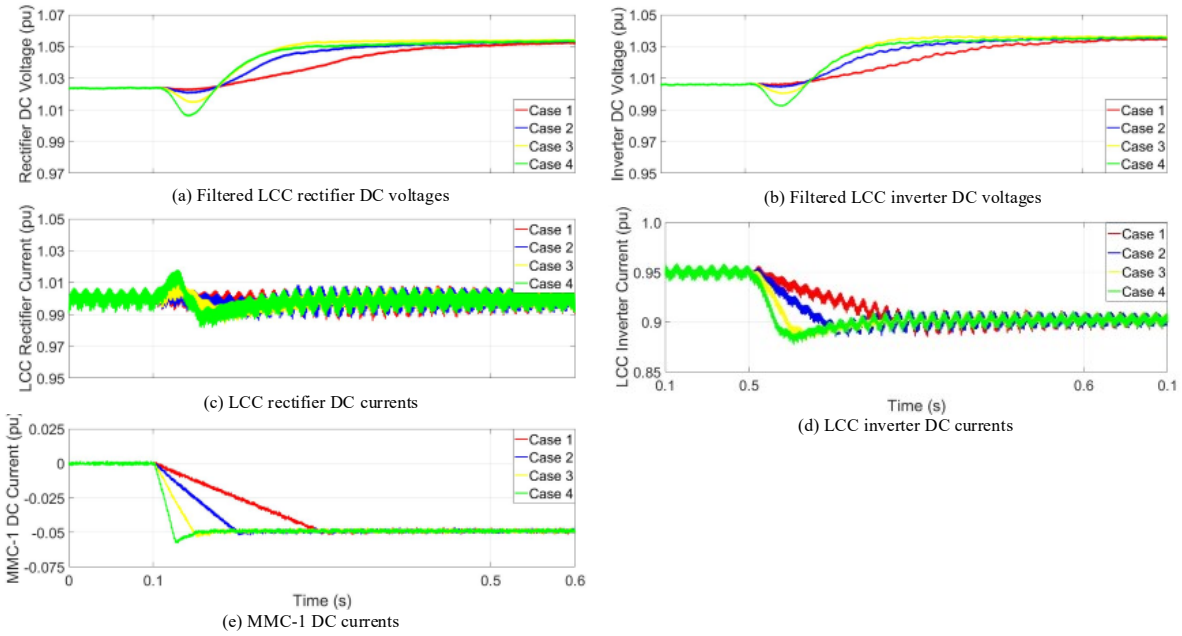



Figure 3.6: System performance under various current ramp rates

## 3.2 Fault Condition

A potential point of failure for the LCC-HVDC system is a fault on the AC side of the taps. This section evaluates the impact of single-line to ground (SLG), double-line to ground, and three-phase to ground faults at the AC side of the taps on the LCC-HVDC system under different tap pre-fault loading conditions. In this section, comparisons between fault response of taps located at several points along the LCC-HVDC line, for various fault locations along the AC overhead line are presented. As the simulation result is identical for all three fault types, only LCC-HVDC system response under tap station AC SLG fault is presented in this section.

### 3.2.1 MMC-1 AC Side Fault with High Loading Level

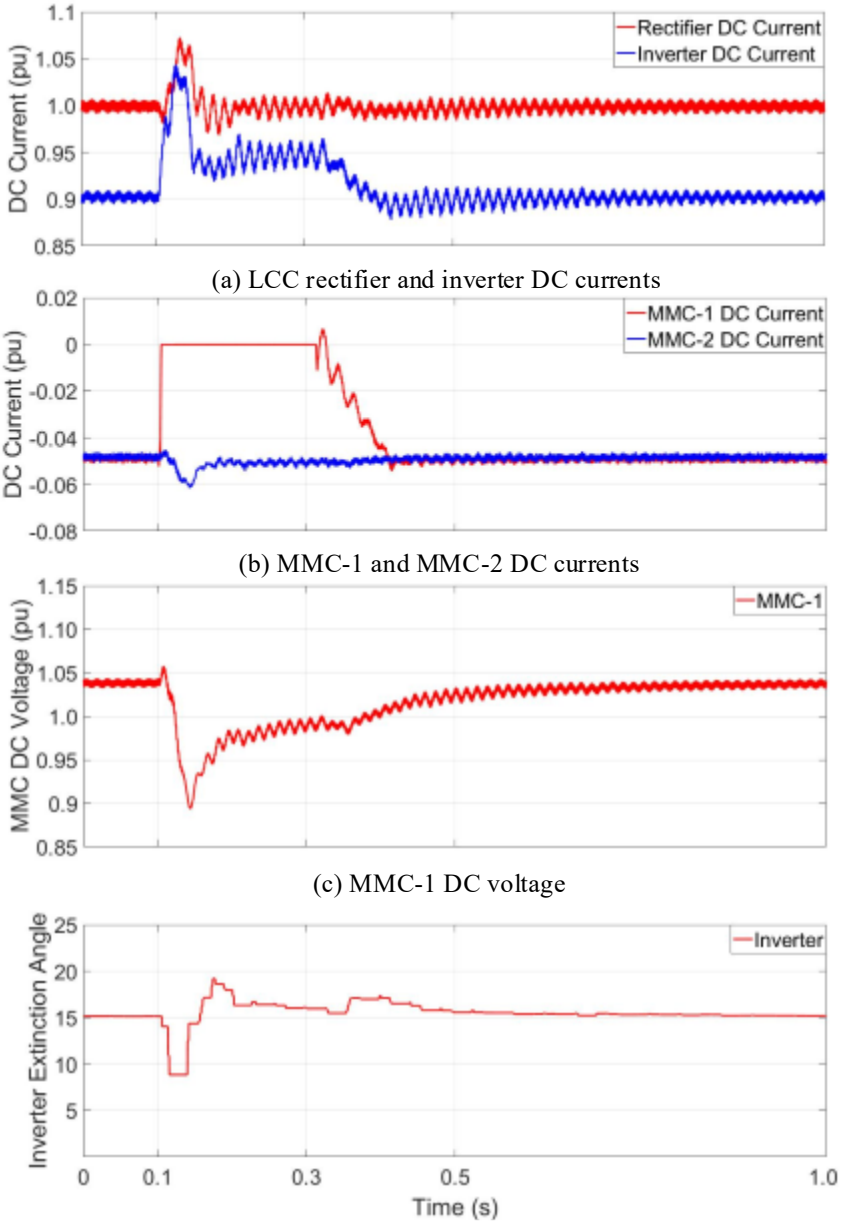
A temporary SLG fault (200 ms) is applied to the AC terminal of MMC-1. The pre-fault current reference of MMC-1 is -0.05 pu such that the tap extracts 50 MW from the DC system.

The test procedure is as follows:

- Initially, the LCC rectifier injects 1 pu and the LCC inverter, MMC-1, and MMC-2 extract 0.9 pu, 0.05 pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, the SLG fault is applied to the AC terminal of MMC-1.
- At t = 0.3 s, the fault is cleared.
- At t = 0.4 s, the system resumes its pre-fault operating condition.

4 ms after the fault instant, the AC side protection system detects an overcurrent in the AC system. The MMC-1 AC breaker and MMC-1 tap are immediately tripped and blocked to stop the flow of current to the fault location. The blocking of the faulted tap results in the converter DC current to drop to zero within 2 ms, as shown in Fig. 3.7(b). The sudden change of the tap current leads to a temporary current imbalance of 0.05 pu in the LCC-HVDC system, where the current entering the HVDC system is greater than the current leaving the system. This causes an instantaneous DC voltage swell of 2%, as depicted in Fig. 3.7(c). Due to the voltage swell, the LCC rectifier current temporarily decreases by 2% whereas the flow of the imbalanced current leads to an increase in the LCC inverter current as shown in Fig. 3.7(a). The increasing LCC inverter current prolongs the commutation overlap and results in a reduction of inverter extinction angle to 8.8° which is well below the acceptable minimum extinction angle of 15°, as seen in Fig. 3.7(d). As the inverter operates in CEA control mode, the inverter firing angle is quickly

reduced to restore the extinction angle back to its reference. The reduction in inverter firing angle causes a temporary DC voltage sag of roughly 14% (measured at the faulted tap), Fig. 3.7(c). This further leads to rapid current overshoots of 1.075 pu and 1.04 pu in the LCC rectifier and inverter, respectively.




(a) LCC rectifier and inverter DC currents

(b) MMC-1 and MMC-2 DC currents

(c) MMC-1 DC voltage

(d) LCC inverter extinction angle

Figure 3.7: System performance during faults on the AC side of the tap (highly-loaded tap)

According to Fig. 3.7(b), the unfaulted MMC tap current suffers from minor oscillations due to the DC voltage variation. At t = 0.15 s, the DC voltage starts ramping back to its nominal value

as the inverter extinction angle is brought back to 15°. The LCC-HVDC system also reaches a new operating point, where the LCC rectifier injects 1 pu, and the inverter, MMC-1, and MMC-2 extract 0.95 pu, 0 pu, and 0.05 pu of DC current, respectively. Minor post-fault oscillations, which slowly damp out, are observed in the LCC rectifier and inverter currents. When the fault is cleared at t = 0.3 s, MMC-1 starts ramping down its current reference to restore its pre-fault operating condition. No significant system disturbance is observed at the LCC-HVDC system during the restoration period.

Since the operation of taps should not interfere with the operation of the LCC-HVDC system, the DC current overshoot and DC voltage sag on the LCC-HVDC system during MMC tap AC SLG faults should be mitigated. These undesirable transients result in rapid changes in the LCC-HVDC system power flow. In addition, the temporary drop in the extinction angle at the inverter station may lead to commutation failure.

### 3.2.2 MMC-1 AC Side Fault with Medium Loading Level

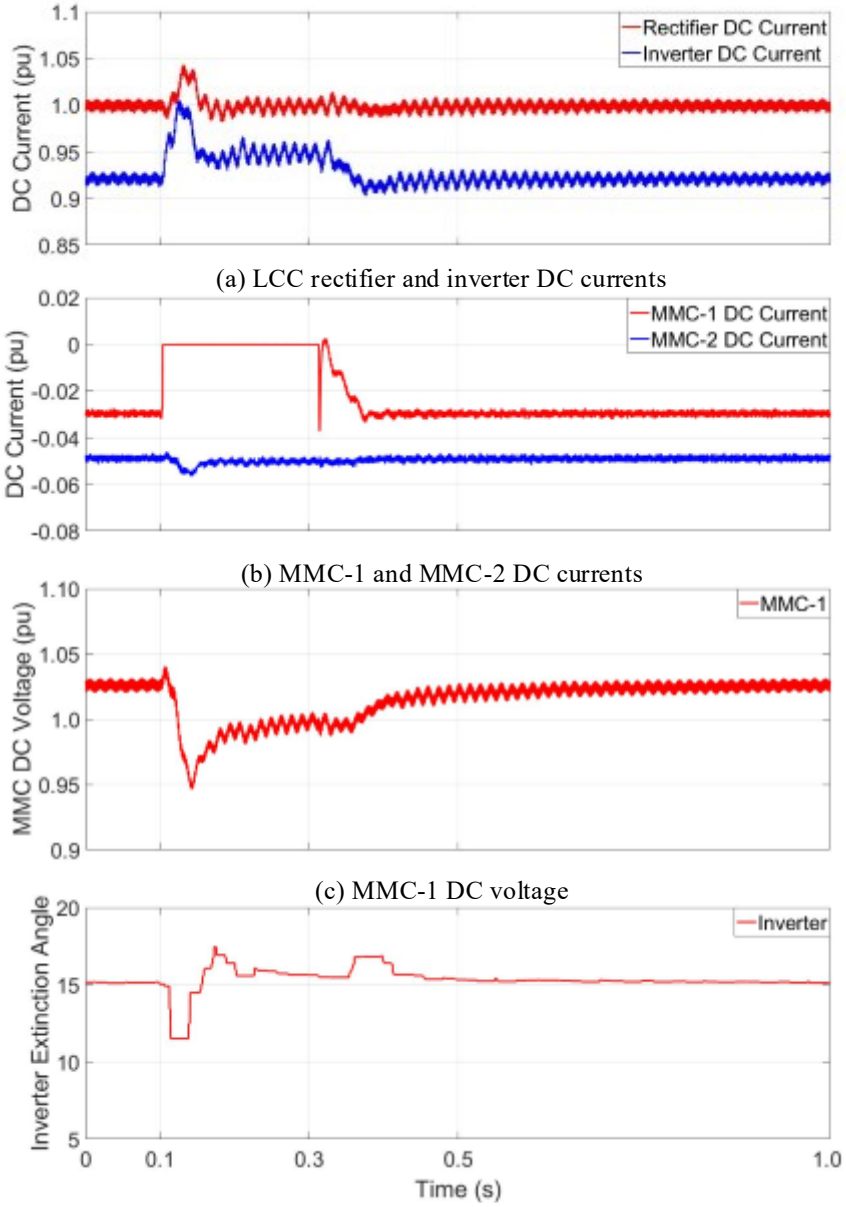
The impact of AC faults at the tap station on the performance of the LCC-HVDC system is investigated under various pre-fault loading levels of the tap station. A temporary SLG fault of 200 ms duration is applied to the AC terminal of MMC-1, while the pre-fault current reference of MMC-1 is -0.03 pu such that the tap extracts 30 MW from the DC system.

The test procedure is as follows:

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, and MMC-2 extract 0.92 pu, 0.03 pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, the SLG fault is applied to the AC terminal of MMC-1.
- At t = 0.3 s, the fault is cleared.
- At t = 0.4 s, the system resumes its pre-fault operating condition.

4 ms after the fault occurrence, the fault is detected and the blocking signal is sent to MMC-1 tap station. A fault transient response similar to the previous test is observed in the LCC rectifier and inverter currents and voltages but with reduced magnitudes. As shown in Fig. 3.8(b), MMC-1 DC current drops to 0 pu, 2 ms after the blocking of the faulted tap. The sudden change of the tap current leads to LCC rectifier and inverter DC current overshoots of 1.04 pu and 1.0 pu, respectively, Fig. 3.8(a). A DC voltage sag of about 7% is observed at the faulted tap, Fig. 3.8(c).

At the instant of the fault, the inverter extinction angle also reduces to 11.8°, which is below the minimum extinction angle of 15°, Fig. 3.8(d). Similar to the previous test, minor current oscillations are observed at the unfaulted MMC tap as a result of the DC link voltage fluctuations.




(a) LCC rectifier and inverter DC currents

(b) MMC-1 and MMC-2 DC currents

(c) MMC-1 DC voltage

(d) LCC inverter extinction angle

Figure 3.8: System performance during faults on the AC side of the tap (medium-loaded tap)

### 3.2.3 MMC-1 AC Side Fault with Light Loading Level

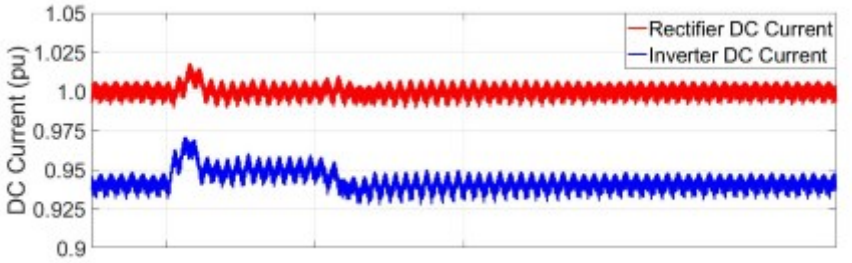
A SLG fault with a 200 ms duration is applied to the AC terminal of MMC-1. The pre-fault current reference of MMC-1 is -0.1 pu such that the tap extracts 10 MW from the DC system.

The test procedure is as follows:

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, and MMC-2 extract 0.94 pu, 0.01 pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, the SLG fault is applied to the AC terminal of MMC-1.
- At t = 0.3 s, the fault is cleared.
- At t = 0.4 s, the system resumes its pre-fault operating condition.

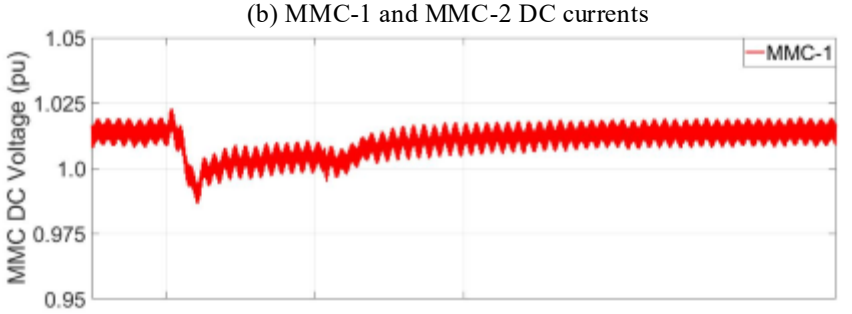
At t = 0.1 s, the tripping of the AC breaker along with the blocking of MMC-1 tap, upon the detection of the fault, causes the tap DC current to instantly drop to zero. Slight current overshoots of 1.02 pu and 0.97 pu and minor oscillations are observed in the LCC rectifier and inverter stations, respectively, Fig. 3.9(a). The current overshoots lead to a DC voltage sag of 2%, Fig. 3.9(c), which temporarily reduces the extinction angle to 13.9°. Since the DC voltage variation is relatively insignificant under the light load condition, no noticeable current oscillations are observed at the healthy MMC tap.

The simulation results from the three previous sections suggest that the transient response of the LCC-HVDC system during tap AC faults under various loading levels of taps remains the same. However, the magnitude of the disturbances on the LCC rectifier and inverter currents, DC link voltage, inverter extinction angle, and healthy MMC current is directly related to the faulted tap pre-fault current contribution.

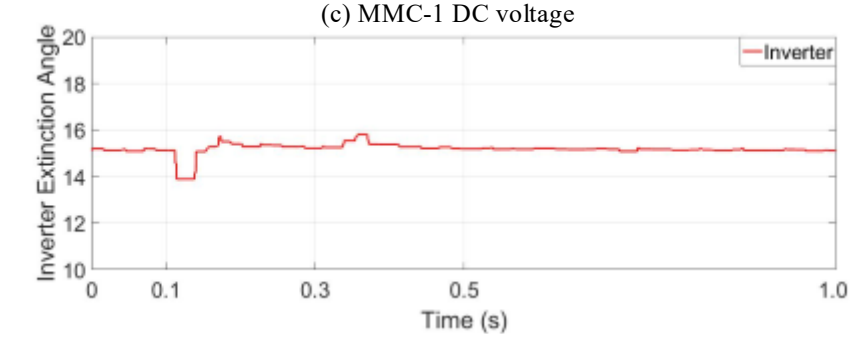



(a) LCC rectifier and inverter DC currents


(b) MMC-1 and MMC-2 DC currents




(c) MMC-1 DC voltage




(d) LCC inverter extinction angle

Figure 3.9: System performance during faults on the AC side of the tap (lightly-loaded tap)

### 3.2.4 Various Locations of the Faulted Tap

This section compares the LCC-HVDC system performance under different faulted tap station locations along the LCC-HVDC line. Table 3.1 outlines four selected locations for the faulted tap along the HVDC line.

The sequence of operation is listed below:

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, MMC-2 extract 0.95 pu, 0.05pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, the SLG fault with a 200 ms duration is applied to the faulted tap as indicated in Table. 3.1.
- At t = 0.3 s, the fault is cleared.
- At t = 0.4 s, the system resumes its pre-fault operating condition.

Table 3.1 Tap locations along the LCC-HVDC system

| | **Tap location away from rectifier (km)** | | **Faulted tap** | |
|---|---|---|---|---|
| | MMC-1 Tap | MMC-2 Tap | MMC-1 Tap | MMC-2 Tap |
| **Case 1** | 75 | 20 | | ✓ |
| **Case 2** | 75 | 40 | | ✓ |
| **Case 3** | 60 | 25 | ✓ | |
| **Case 4** | 80 | 25 | ✓ | |

During tap AC side faults, the filtered LCC rectifier DC voltages are similar in all cases; however, the magnitude of the voltage sags tends to be slightly lower as the location of the faulted tap is further away from the LCC rectifier. Identical transient behaviors are observed in the LCC rectifier and inverter currents (Figs. 3.10(b) and (c)), and MMC tap currents (Figs. 3.10(d) and (e)). The reduction of inverter extinction angle in all cases is of the same magnitude, Fig. 3.10(f).

The four case studies suggest that the LCC-HVDC system response to the tap AC faults does not depend on the location of the faulted tap.

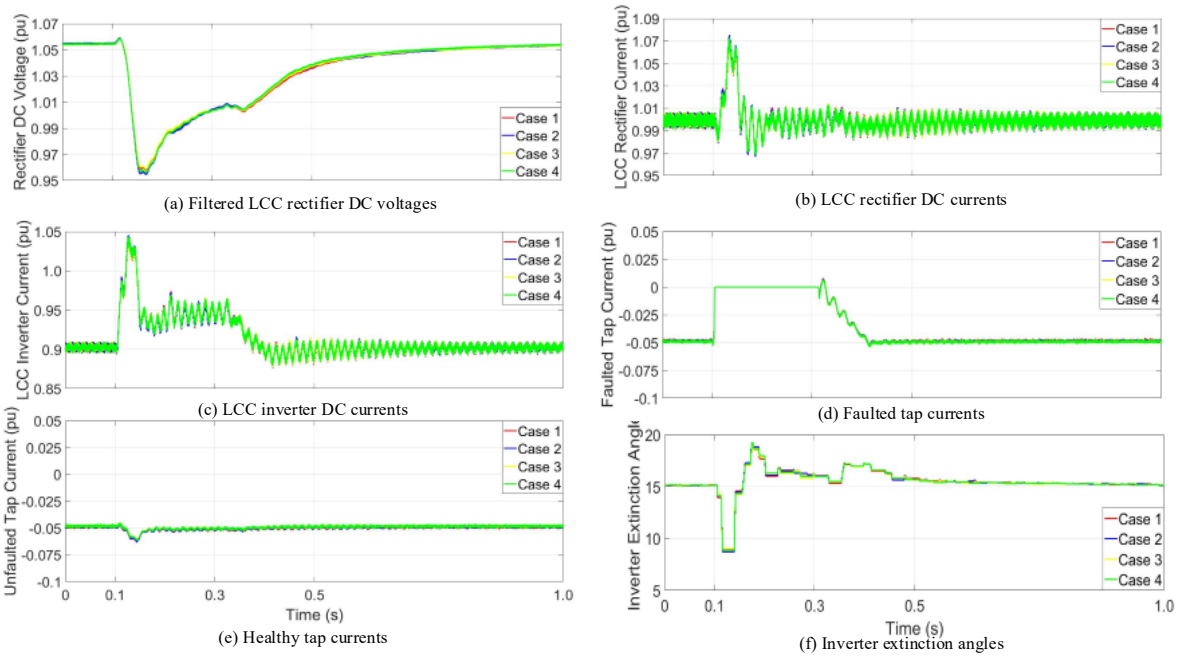



Figure 3.10: System performance during AC faults on the tap station at various locations

### 3.2.5 Various Locations of the Fault along MMC-1 AC Overhead Line

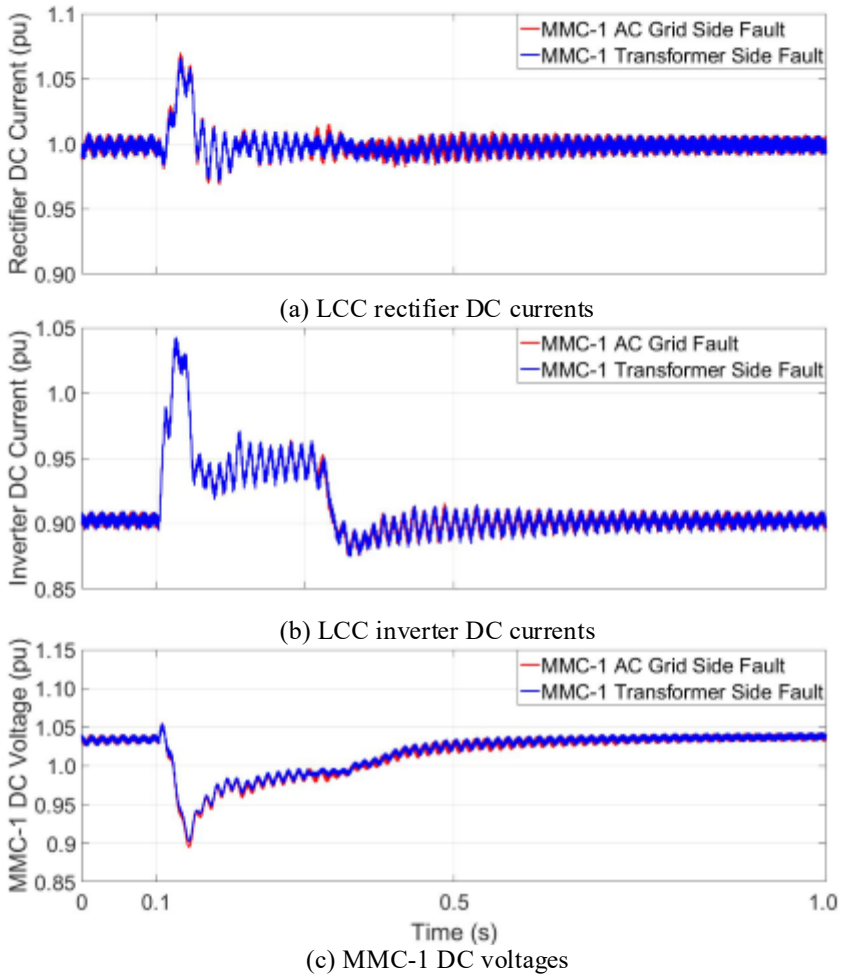
Extensive simulations have been performed to evaluate the impact of the AC fault location on the operation of the LCC-HVDC system. Two fault scenarios are selected for demonstration in this section including faults at i) MMC-1 AC grid terminal, which is the furthest location away from the tap converter, and ii) MMC-1 transformer terminal which is the closest location to the converter. SLG faults with 200 ms duration are applied to the two selected locations.

The sequence of operations is listed below:

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, and MMC-2 extract 0.9 pu, 0.05 pu, and 0.05 pu of DC current, respectively.
- At t = 0.1 s, the SLG fault is applied to the AC grid /transformer terminal of MMC-1 tap.
- At t = 0.3 s, the fault is cleared.
- At t = 0.4 s, the system resumes its pre-fault operating condition.

As shown in Figs. 3.11(a) and (b), the LCC rectifier and inverter DC currents variations for both fault locations are identical. At the instant of the fault, the magnitude of the DC voltage sag at MMC-1 is also similar for both cases, Fig. 3.11(c).

Similar LCC-HVDC system behavior is observed under both fault conditions, which indicates the location of the fault along the tap AC line does not significantly alter the LCC-HVDC system response during tap AC side faults.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) MMC-1 DC voltages

Figure 3.11: System performance during faults at different locations on the AC side of the tap

## 3.3 Summary

This chapter verified the power tapping capability of MMC taps and analyzed the system performance under both normal and abnormal conditions. Under normal operation, the ability of MMC taps to inject/extract current at different ramp rates, to provide reactive power compensation, and to perform power reversal is verified; such operations had a negligible impact on the operation of the LCC-HVDC system. On the other hand, simulation results revealed undesirable disturbances in the DC current/voltage of the LCC-HVDC system in case of AC side faults at the tap stations. The severity of the disturbance imposed on the LCC-HVDC system gets worse as the magnitude of the pre-fault DC tapping current extracted from the system increases. It is noted that the blocking of MMCs leads to a transient reduction in the inverter extinction angle, which risks the operation of the entire LCC-HVDC system. Tap AC side fault studies have also been performed for a current injecting tap; however, the simulation plots are not explicitly shown in this chapter as the resulting disturbances in the LCC-HVDC system is not as severe as compared to the case with a current extracting tap. Simulation results also revealed that the location of the faulted tap along the LCC-HVDC system, as well as the location of the AC side fault along the AC overhead line, do not significantly impact the severity of the resulting disturbances on the LCC-HVDC system. Thus, disturbance mitigation methods are proposed and discussed in chapter 4 to enhance the LCC-HVDC system response in case of tap AC side faults. The developed methods are capable of damping out the undesired transients to ensure the smooth fault ride-through of tap AC line faults such that the integration of taps does not impose additional operational risks on the LCC-HVDC system.

# Chapter 4

# Tap Station Current Modulation and Supplementary Controllers

Disturbances such as HVDC line current overshoot, HVDC line voltage dip, and inverter extinction angle reduction imposed on LCC-HVDC systems as a result of tap AC side faults are deemed to be unacceptable as discussed in chapter 3. A tap station current modulation method and three different supplementary controller configurations that utilize local measurements are therefore proposed to enhance the overall LCC-HVDC system performance in case of tap-side AC faults. The tap station current modulation method involves dynamically adjusting the current reference of the healthy MMC tap to counteract the momentary LCC-HVDC current imbalance caused by the blocking of the faulted MMC tap. In comparison, the three supplementary controller configurations dynamically vary the reference signals of the LCC rectifier and inverter stations to improve the response of the main LCC-HVDC system controllers. In this chapter, the validity of the proposed methods is discussed and verified through extensive simulations in PSCAD/EMTDC. In subsequent sections, SLG faults are applied to the AC terminal of the MMC-1 tap which is also referred to as the faulted tap. On the other hand, the unfaulted MMC-2 tap is referred to as the healthy MMC tap.

The effectiveness of the tap station current modulation method and three different supplementary controller configurations are verified at two pre-fault loading conditions of the faulted tap including extracting 50 MW (highly-loaded tap) and 30 MW (medium-loaded tap) from the DC system.

The simulation sequence of operation for the faulted tap station extracting 50 MW (and 30 MW) from the DC system is listed below and will be used in the rest of this chapter:

- Initially, the LCC rectifier injects 1 pu of DC current and the LCC inverter, MMC-1, and MMC-2 extract 0.9 pu (0.92 pu), 0.05 pu (0.03 pu), and 0.05 pu (0.05 pu) of DC current, respectively.
- At t = 0.1 s, the SLG fault is applied to the AC terminal of MMC-1 tap.
- At t = 0.3 s, the fault is cleared.
- At t = 0.4 s, the system resumes its pre-fault operating condition.

## 4.1 Tap Station Current Modulation

As seen in section 3.2.1, the blocking of the faulted MMC-1 tap caused its current to drop to zero in a few milliseconds. The rapid reduction in the tap current leads to a temporary current imbalance in the LCC-HVDC system, which results in system parameter oscillations due to the finite response speed of the LCC rectifier and inverter controllers. Therefore, if the rapid reduction of tap current for the LCC rectifier and inverter controllers can somehow be counteracted by control measures, the LCC-HVDC system disturbance and oscillation can be significantly alleviated.

Simulation results in section 3.1.2 suggest that the interaction between the two MMC taps functioned nearly independently from the main LCC-HVDC system. Thus, the idea of temporarily increasing the current reference of the healthy tap by the pre-fault current contribution of the faulted tap at the fault instant to cancel out the effect of the rapid current reduction of the faulted tap is proposed. The increased portion of the healthy tap current reference then rapidly damps out such that its current reference returns to the pre-fault value. By doing so, adequate time will be left for the LCC-HVDC system controllers to gradually settle at a new operating point. In this method, no communication between the two MMC tap stations is required. Therefore, the proposed tap station current modulation method utilizes local measurements and is applied to each of the two MMC taps. The activation algorithm and the current estimating scheme are the two main components of the method, which will be discussed in detail. The feasibility of the proposed method is subjected to certain limitations and is only applicable to LCC-HVDC systems with two tap stations.

The current estimating scheme is embedded in each of the MMC taps and it estimates the current contribution of the opposite MMC tap based on the locally measured DC link voltage and MMC tap DC current, along with the scheduled rectifier current order received from control centers. During normal operation, the LCC-HVDC system current balance is achieved when the summation of the LCC inverter, and MMC-1 and MMC-2 currents is equal to the LCC rectifier current; thus, by knowing the LCC rectifier, inverter, and local MMC tap currents, the magnitude of the current contribution from the opposite MMC tap can be estimated. As the LCC inverter adopts constant extinction angle control, the magnitude of the DC link voltage will vary with changes in the LCC inverter current. For example, an increase of the LCC inverter current prolongs the commutation overlap, thus reducing the inverter average voltage since the extinction angle is maintained constant. Therefore, the magnitude of the LCC inverter current can be approximated from the DC link voltage from the relation represented by (4.1) where $V_{di}$ is the inverter average direct voltage, $V_{d0i}$ is the inverter ideal no-load direct voltage, $I_{di}$ is the inverter current, $\gamma$ is the inverter extinction angle, and $R_{ci}$ is the inverter commutating resistance.

$$V_{di} = V_{d0i}cos\gamma - R_{ci}I_{di}. \tag{4.1}$$

The measured DC link voltage at each tap with respect to different magnitudes of the inverter current is plotted in Fig. 4.1. Note the LCC inverter current and DC link voltage relation of MMC-1 is slightly lower than that of MMC-2, which is due to the DC line resistive voltage drop as the two taps are located at different locations along the LCC-HVDC line, as represented by (4.2)-(4.3) where $V_{dMMC1}$ and $V_{dMMC2}$ are the DC link voltage at MMC taps, $R_1$ is the DC line resistance between the LCC inverter and MMC-1 tap station, $R_2$ is DC line resistance between MMC-1 and MMC-2 tap stations, and $I_1$ is MMC-1 DC current. During steady-state, the current estimating scheme of each of the taps continuously estimates the current contribution of the opposite MMC tap. The calculated current contribution of the opposite MMC tap then serves as the pre-fault current reference which will be added to the healthy MMC tap when AC side faults occur at the opposite MMC tap.

$$V_{dMMC1} = V_{di} + I_{di}R_1, \tag{4.2}$$

$$V_{dMMC2} = V_{di} + I_{di}R_1 + (I_{di} + I_1)R_2. \tag{4.3}$$

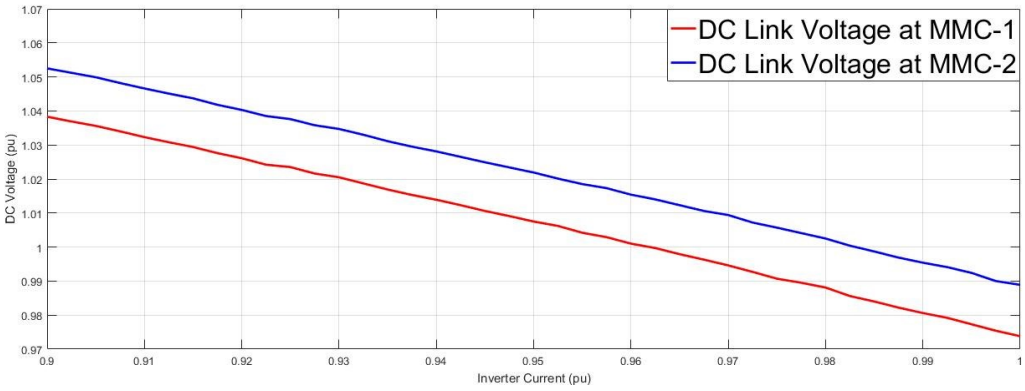



Figure 4.1: Relationship of inverter current and DC link voltage

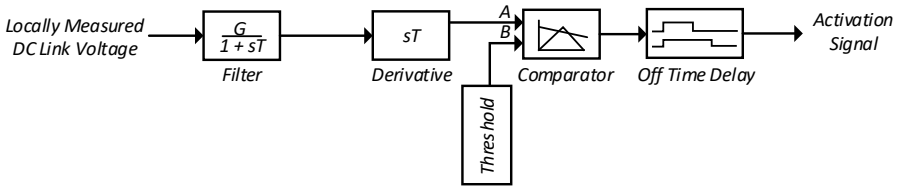



Figure 4.2: Activation algorithm

An activation algorithm is implemented in each tap, shown in Fig. 4.2, to trigger the current reference adjustment of the healthy MMC tap upon detecting the DC link voltage fluctuation caused by the blocking of the faulted MMC tap and its associated rapid current reduction. The derivative of the locally measured DC link voltage is continuously monitored and compared to a threshold. When the derivative of the measured DC link voltage exceeds the threshold, the activation signal goes high (i.e., logic 1). As the magnitude of the DC link voltage fluctuation depends on the pre-fault current contribution of the faulted MMC tap, the threshold should be selected such that it is small enough to be able to detect the tap AC side fault at low pre-fault current contributions, yet large enough to avoid misoperation during normal operation such as scheduled current set-point changes. A 0.9 s off-time delay is implemented to leave adequate time for fault clearance and for the LCC-HVDC system to settle at steady-state before the activation signal can be activated again, therefore avoiding the re-triggering of the current estimating controller. The off-time delay has no impact on the signal turn-on time.

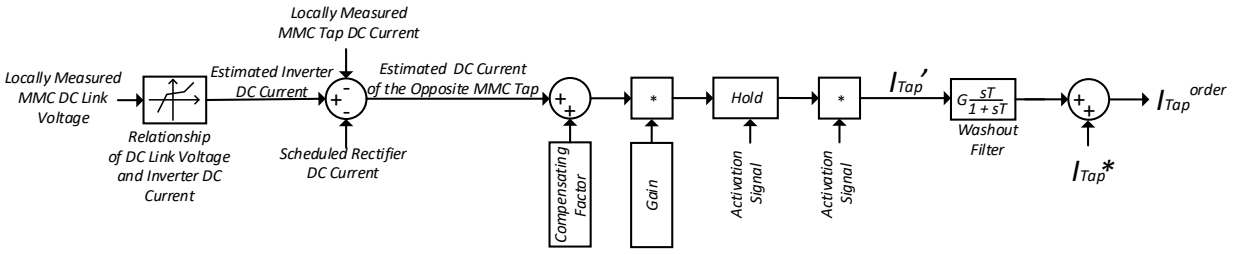


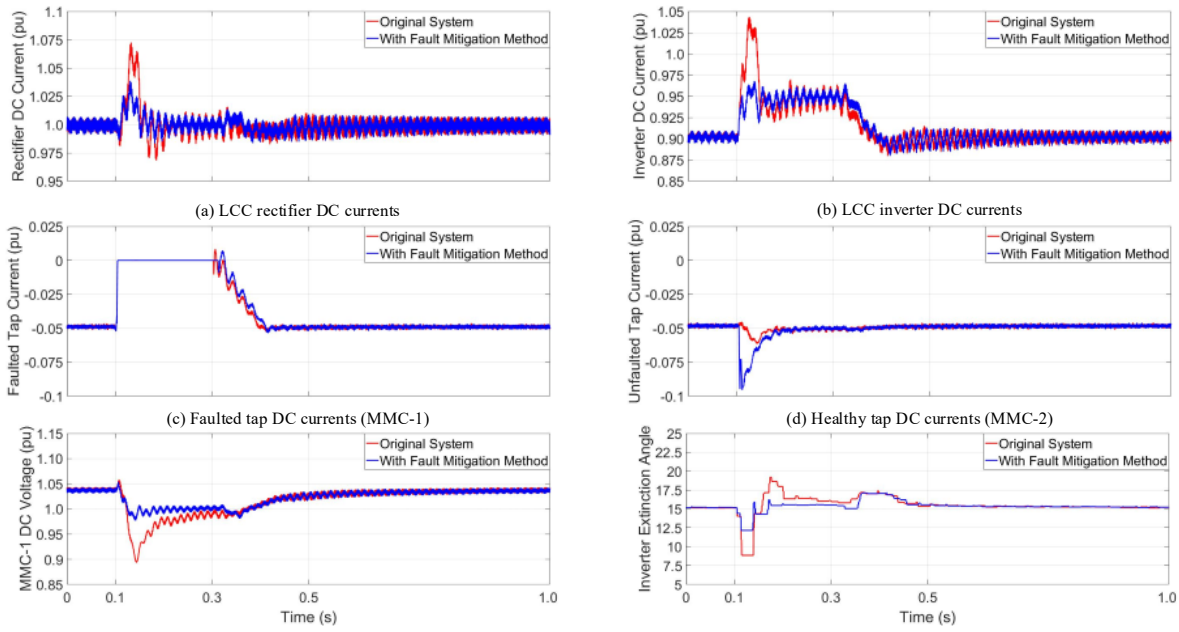

Figure 4.3: Current estimating controller

The current estimating controller, as shown in Fig. 4.3, is implemented in each of the two taps. First, the locally measured DC link voltage at the MMC tap is sent to a transfer function block to estimate the inverter current from the relation illustrated in Fig. 4.1. Next, the locally measured MMC tap current and the scheduled rectifier current are subtracted from the estimated inverter current to approximate the DC current of the opposite MMC tap. The estimated current of the opposite MMC tap is then corrected with the compensating factor and gain terms to form the supplementary current reference ($I_{Tap}{}'$). The compensating factor and gain terms convert the real value of the estimated current of the opposite MMC tap to per unit value and account for the different DC line resistive drop for the estimated current at each tap. During normal operation, the activation signal generated from the activation algorithm is set to zero. When an AC side fault occurs at the opposite MMC tap, the activation signal of the healthy MMC tap goes high to activate the supplementary current reference. The supplementary current reference is then added to the nominal tap current reference ($I_{Tap}{}^{*}$) to generate the adjusted current reference ($I_{Tap}{}^{order}$). The hold block temporarily holds the pre-fault current contribution of the faulted MMC tap such that the washout filter can quickly reduce the supplementary current reference of the healthy MMC to zero at a rate of 0.5 pu/s which is also the nominal current ramp rate of the MMC taps. Thus, the current reference of the healthy MMC tap can be restored to its pre-fault operating condition without causing the LCC-HVDC system unstable. After the rate of change of the DC link voltage reduces to below the threshold for 0.9 s, the activation signal returns to zero, and de-activates the hold block and the current estimating controller. The 0.9 s off-time delay is selected based on the settling time of the LCC-HVDC system to a new steady-state operating point following tap AC side faults as previously discussed.

### 4.1.1 Tap AC Side Faults with High Loading Level

A temporary SLG fault of 200 ms duration is applied to the AC terminal of MMC-1 tap to verify the effectiveness of the tap station current modulation method. The pre-fault current reference of MMC-1 tap is set to -0.05 pu to extract the rated power of 50 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.

At t = 0.1 s, the fault is initiated, and the blocking of MMC-1 tap causes its DC current to drop to zero, as shown in Fig. 4.4(c). Due to the rapid current reduction of the faulted MMC tap, a current imbalance of 0.05 pu occurs in the LCC-HVDC system, which leads to an instantaneous DC link voltage swell of 2%, Fig. 4.4(e). Upon sensing the rapid change in the DC link voltage, an activation signal is issued to the current estimating controller of MMC-2 to adjust its current reference from -0.05 pu to -0.098 pu to compensate for the impact of MMC-1 current reduction on the LCC rectifier and inverter controllers. As shown in Fig. 4.4(d), MMC-2 current is momentarily adjusted to -0.0975 pu, which greatly reduces the transient current imbalance and assists the LCC-HVDC system to reach a new operating point. The LCC rectifier current overshoot also reduces from 1.075 pu to 1.04 pu, Fig. 4.4(a). Moreover, a significant improvement is observed in the LCC inverter current with its overshoot reducing from 1.044 pu to 0.97 pu, Fig. 4.4(b). As a result of the reduction in the LCC inverter current overshoot, the magnitude of the DC link voltage dip is also significantly reduced as compared to the case without the tap station current modulation method, as shown in Fig. 4.4(e). As depicted in Fig. 4.4(f), the transient extinction angle reduction is also improved from 8.8° to 12.15°, which reduces the possibility of inverter commutation failure. MMC-2 supplementary current reference reduces to zero after 100 ms at t = 0.2 s to leave adequate response time for the LCC rectifier and inverter controllers and to allow MMC-2 to return to its pre-fault operating condition. The LCC-HVDC system reaches a new operating point, where the LCC rectifier injects 1 pu, and the inverter, MMC-1, and MMC-2 extract 0.95 pu, 0 pu, and 0.05 pu of DC current, respectively. Minor post-fault oscillations are observed in the LCC rectifier and inverter currents for both cases with and without the tap station current modulation method. At t = 0.3 s, the fault is cleared and MMC-1 current reference ramps back to -0.05 pu to restore the pre-fault operating condition. As the scope of this simulation is to verify the impact of restoring the pre-fault current reference of the faulted tap, the current reference of the faulted tap ramps back to its pre-fault value as soon as the SLG fault enabling signal is removed.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

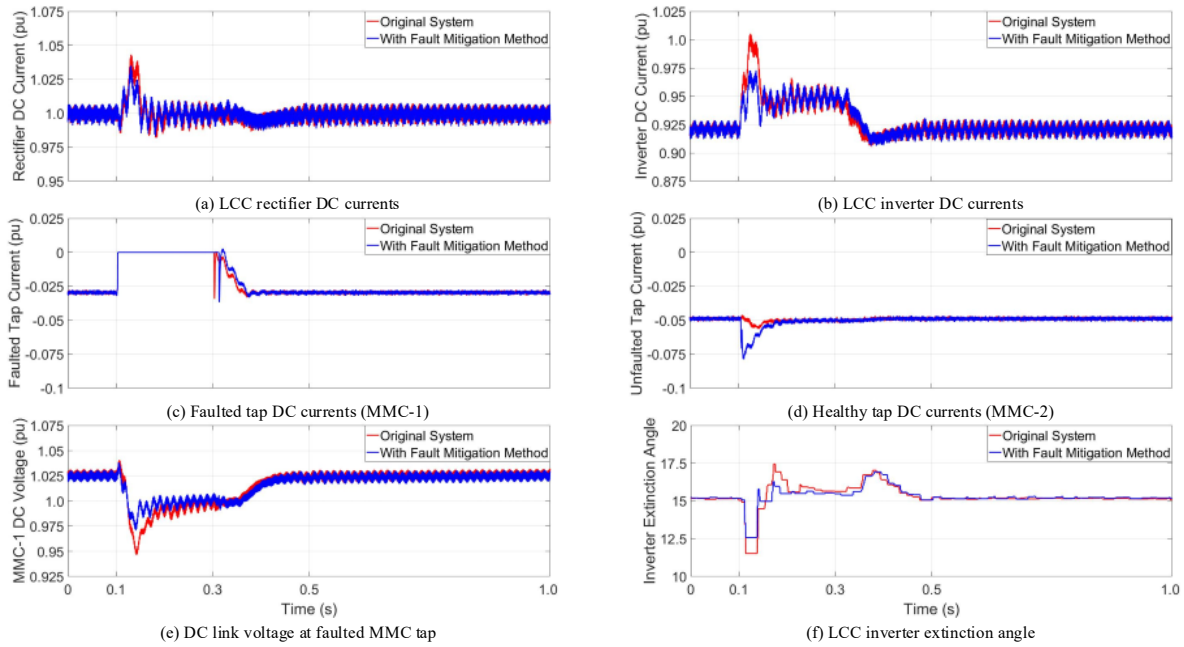
(f) LCC inverter extinction angle

Figure 4.4: System performance during faults with tap station current modulation controller (highly-loaded tap)

### 4.1.2 Tap AC Side Faults with Medium Loading Level

A SLG fault with a duration of 200 ms is applied to the AC side of MMC-1 tap. The pre-fault current contribution of MMC-1 tap is set to -0.03 pu to extract 30 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.

At t = 0.1 s, the tripping of MMC-1 AC side breaker and the blocking of MMC-1 tap cause its DC current to drop to zero approximately 6 ms after the occurrence of the fault. Upon detecting the rapid change of the DC link voltage, the fault mitigation controller dynamically adjusts the current reference of MMC-2 from -0.05 pu to -0.079 pu. At t = 0.11 s, MMC-2 current reaches -0.078 pu, as seen in Fig. 4.5(d). Similar improvements in the system performance are observed as compared to section 4.1.1. The LCC rectifier and inverter current overshoots reduce from 1.045 pu to 1.035 pu and 1.006 pu to 0.97 pu, respectively, as shown in Figs. 4.5(a) and (b). The improved LCC inverter current response also reduces the variations of the commutation overlap, thus reducing the magnitude of the DC link voltage dip and the fluctuations of the inverter extinction angle, as displayed in Figs. 4.5(e) and (f).




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

(f) LCC inverter extinction angle

Figure 4.5: System performance during faults with tap station current modulation controller (medium-loaded tap)

The ability of the tap station current modulation controller to improve the LCC-HVDC system performance during tap AC side faults is verified. The tap station current modulation method effectively alleviates the disturbance imposed on the LCC-HVDC system such as the LCC rectifier and inverter currents, the DC link voltage, and the inverter extinction angle.

For HVDC systems with more than two tap stations, droop control may be added to the tap station current modulation method to divide the temporary current adjustments among tap stations based on criteria such as the power rating and the operating status of tap stations.

With the rapid development of the 5G network, information exchange between tap stations can be achieved with a transmission delay of less than 1 ms. The availability of a communication channel between tap stations will further enhance the LCC-HVDC system response as the exact tap station currents can be transferred between tap stations. In addition, the blocking signal of the faulted tap can replace the existing activation algorithm to enhance reliability and to reduce the fault detection time. Nevertheless, the proposed current estimating controller and the activation algorithm are more cost-effective than communication-based option and can serve as a reliable backup plan in the case of communication failure between tap stations.

### 4.1.3 Technical Feasibility of Tap Station Current Modulation

The tap station current modulation involves temporarily adjusting the current reference of MMC taps, which overloads the healthy MMC tap converter, albeit for a very short amount of time. Therefore, two technical feasibility criteria are discussed including i) the surge current handling capability of IGBT switches, and ii) the dissipation of the excess power.

Under normal operation, each MMC tap may carry up to 100 A of DC current at 500 kV to achieve the rated real power exchange of 50 MW. However, with the tap station current modulation method, MMC taps may be commanded to operate at 200 A for a short period of time to alleviate the LCC-HVDC system disturbance. As most of the market available IGBT switches utilized for high power applications are designed with voltage and current ratings over 1 kV and 500 A, the temporary current surge of 200 A will not cause any thermal damage to the converter IGBT switches in practice.

With conventional MMC control schemes, the temporary current reference adjustment will lead to additional energy entering its associated AC system. As the tap AC grid is usually weak, direct transfer of the excess energy into the AC system will likely lead to frequency deviations and system instability. Therefore, three potential solutions are outlined and discussed below.

1. Storing the excess energy in MMC tap SM capacitors. Under the worst case scenario of temporarily increasing the current reference by 0.05 pu, a total energy of 2,250 kJ that is evenly distributed between all SMs will lead to approximately 15% increase in SM capacitor voltages. A dedicated MMC control scheme that is capable of absorbing and storing the excess energy in SM capacitors yet maintaining a constant real power exchange with the AC grid is a topic for future research.
2. The dynamic braking system (DBS) is originally designed to enhance the disturbance ride-through capability of off-shore wind farms by dissipating the excess energy through a combination of dummy resistors and power electronic devices. The same idea could be applied to tap stations to dissipate the excess energy.
3. The excess energy may also be stored in local energy storage systems; however, the feasibility of such a method is highly dependent on the capacity and the availability of energy storage devices.

## 4.2 Supplementary Controllers

This section presents three supplementary controller configurations implemented in the LCC converter controllers, namely the rectifier supplementary controller, the inverter supplementary controller, and the combined rectifier and inverter supplementary controllers. As the LCC rectifier adopts CC mode during normal operation, the rectifier supplementary controller is set to dynamically adjust the rectifier current order. On the other hand, as the LCC inverter adopts CEA mode and sets the DC link voltage, the inverter supplementary controller dynamically varies the inverter extinction angle set-point in case of tap AC side faults.

As previously seen in section 3.2, the mode stabilizer embedded in the LCC inverter causes minor LCC rectifier and inverter currents oscillation both at the fault instant and during the post-fault restoration period. The purpose of the mode stabilizer is to ensure the smooth transferring of CC mode from the LCC rectifier to the inverter in case of rectifier AC voltage depression. When the rectifier fails to regulate the DC current, the mode stabilizer increases the inverter extinction angle set-point to reduce the inverter average direct voltage, therefore assisting the rectifier to restore the nominal current order. For example, when a voltage depression occurs at the rectifier AC terminal, the DC link current reduces; therefore, the rectifier increases its average direct voltage in an attempt to maintain CC. Should the rectifier fail to regulate the DC link current, the mode stabilizer starts to increase the inverter extinction angle set-point, which in turn reduces the inverter average direct voltage to assist the restoration of the DC link current back to the nominal rectifier current order.

During tap AC side faults, the mode stabilizer operates to respond to the transient current imbalance and results in undesirable system oscillations. Thus, a mode stabilizer disabling scheme is proposed to temporarily disable the mode stabilizer for 0.5 s upon detecting tap AC side faults. This will leave enough time for the LCC-HVDC system to settle at a new operating point before the mode stabilizer is re-enabled. The triggering conditions of the mode stabilizer disabling scheme are mainly selected based on the LCC-HVDC system response to tapping station AC side faults. The disabling signal is triggered when the positive rate of change of the DC link voltage is greater than a threshold or when the extinction angle falls below 14.5°. The feasibility and the operation of the mode stabilizer disabling scheme are proved not to hinder the normal operation of the mode stabilizer. As the mode stabilizer is targeted to alleviate the impact of rectifier AC voltage

fluctuations, in the case of rectifier AC voltage depression, the rate of change of the DC link voltage will not be positive and the reduction in the DC link current would only increase the extinction angle to above its reference value of 15°.

### 4.2.1 Rectifier Supplementary Controller

The voltage difference of the LCC rectifier and inverter dictates the magnitude of the DC link current. Thus, when the LCC-HVDC system is subjected to disturbances, the response of the rectifier CC controller to variations of the DC link voltage (in an effort to regulate the DC link current) will result in coupled interactions between the LCC rectifier and inverter controllers. In addition, the presence of the large DC link smoothing reactor delays the current response to DC link voltage fluctuations, which further increases system-wide oscillations during tap AC faults. Therefore, the rectifier real power is selected as the input of the controller to reflect the dynamics of the DC link voltage and the rectifier current, and to generate the supplementary current reference.

The proposed rectifier supplementary controller is shown in Fig. 4.6. The rectifier real power is first filtered and passed to a derivative block. Under steady-state operation, the filtered real power is relatively constant such that its derivative equals nearly zero. On the other hand, when tap AC side faults occur, the fast-changing derivative of the rectifier real power will be converted to a current order to enhance the LCC-HVDC system performance. Next, the derivative of the filtered rectifier real power is passed to a PI controller and a washout filter to generate the supplementary current reference ($I_r{}'$), which is then subtracted from the nominal rectifier current order ($I_r{}^*$) to form the modified rectifier current order ($I_r{}^{order}$). The purpose of the washout filter is to gradually reduce the supplementary current reference and to restore the pre-fault current reference of the rectifier. The magnitude of the supplementary current reference is limited to $\pm 0.01$ pu to prevent large variations in power injection/absorption of the MMC taps and potential LCC-HVDC system stability issues.

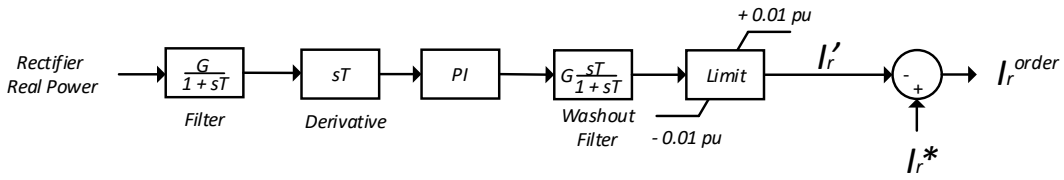
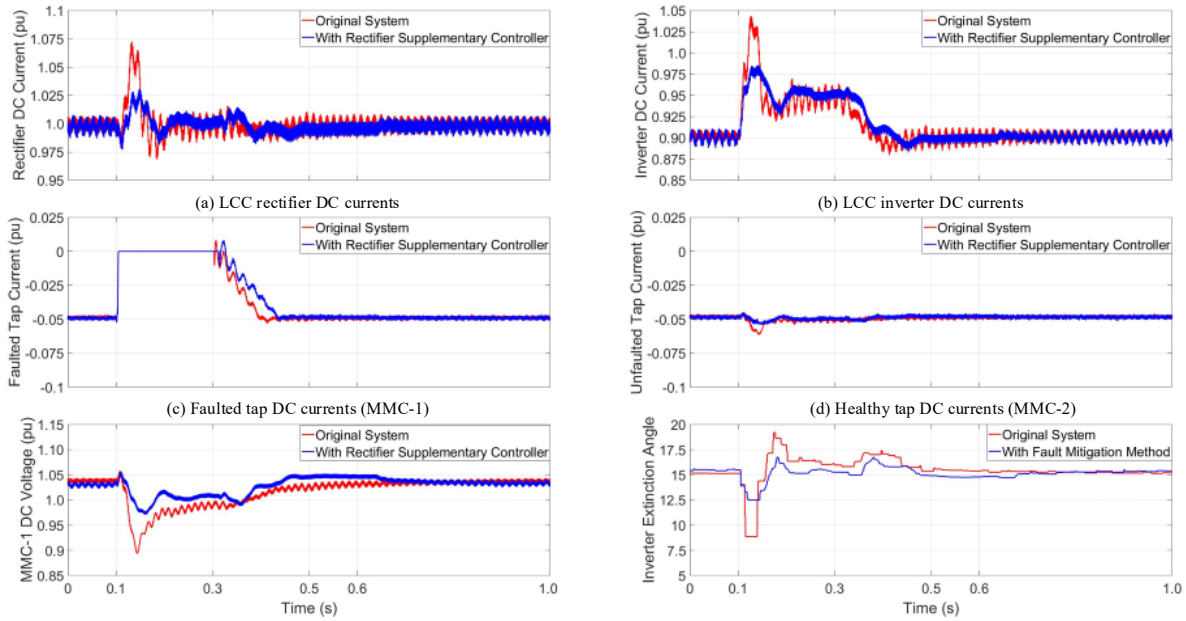



Figure 4.6: Rectifier supplementary controller

#### 4.2.1.1 Tap AC Side Faults with High Loading Level

A SLG fault with 200 ms duration is applied to MMC-1 tap AC terminal. The pre-fault current reference of MMC-1 tap is set to -0.05 pu to extract 50 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

(f) LCC inverter extinction angle

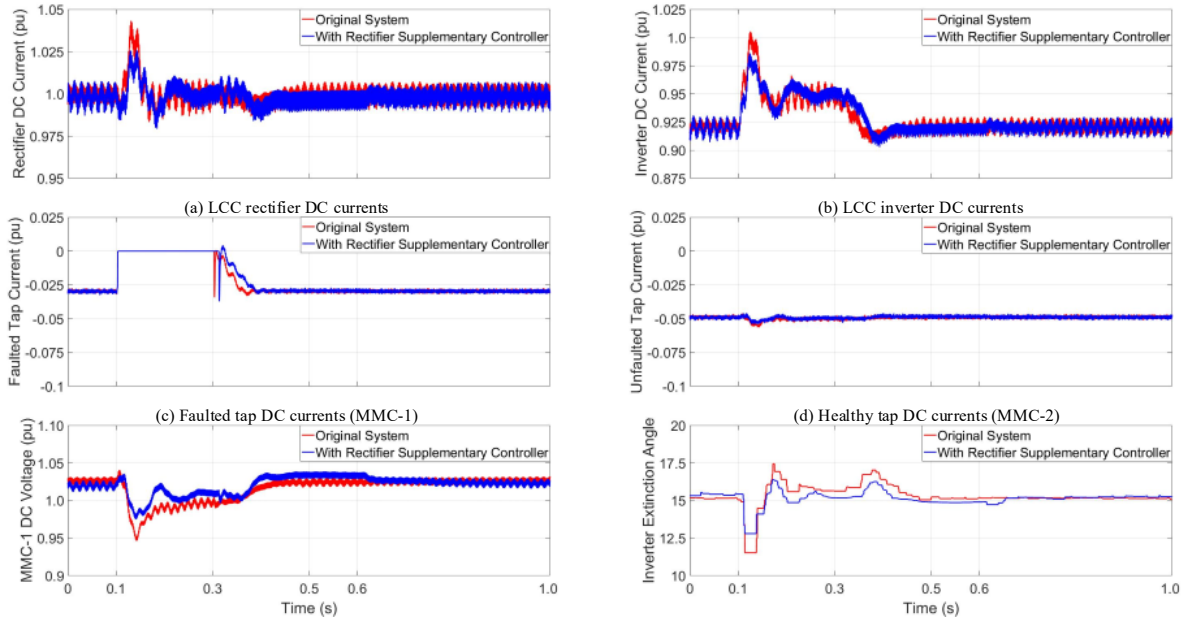
Figure 4.7: System performance during faults with rectifier supplementary controller (highly-loaded tap)

Prior to the fault occurrence, the LCC-HVDC system operates at steady-state with the rectifier supplementary controller generating a supplementary current reference that is almost zero. At t = 0.1 s, after the fault occurrence, the fault detection algorithm trips the MMC-1 AC breaker and blocks MMC-1 tap 4 ms into the fault. The rapid reduction of MMC-1 current leads to a transient current imbalance within the LCC-HVDC system, which further results in a DC link voltage swell of 2%, as shown in Fig. 4.7(e). As the positive rate of change of the DC link voltage exceeds the threshold, a disabling signal is issued by the mode stabilizer disabling scheme to disable the mode stabilizer at t = 0.106 s. The magnitude of the supplementary current reference varies with the fluctuations of the rectifier real power. As seen in Figs. 4.7(a) and (b), with the rectifier supplementary controller, the LCC rectifier and inverter current overshoots reduce significantly from 1.075 pu to 1.03 pu and 1.044 pu to 0.985 pu, respectively. The DC link voltage

sag also improves from 0.89 pu to 0.97 pu, as shown in Fig. 4.7(e), which in turn reduces the impact on the healthy tap DC current. Fig. 4.7(f) shows the improved inverter extinction angle response (minimum) from 8.8° to 12.5°. With the implementation of the rectifier supplementary controller, it can be observed that the LCC-HVDC system oscillations at both the fault instant and during the restoration period are much lower as compared to the original system. At t = 0.64 s, the mode stabilizer is re-enabled and minor oscillations once again appear in the LCC rectifier and inverter currents.

#### 4.2.1.2 Tap AC Side Faults with Medium Loading Level

A temporary SLG fault of 200 ms duration is applied to the AC terminal of MMC-1 tap. The pre-fault current contribution of MMC-1 tap is set to -0.03 pu to extract 30 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

(f) LCC inverter extinction angle

Figure 4.8: System performance during faults with rectifier supplementary controller (medium-loaded tap)

Similar LCC-HVDC system performance improvements are observed as compared to the case with the pre-fault contribution of -0.05 pu. As shown in Figs. 4.8(a) and (b), the magnitudes of the LCC rectifier and inverter current overshoots reduce from 1.045 pu to 1.025 pu and 1.01 pu to 0.98 pu, respectively. The impact on the DC link voltage and the inverter extinction angle also

improves from 0.946 pu to 0.975 pu and 11.5° to 12.8°, respectively, as seen in Figs. 4.8(e) and (f).

Simulation results from sections 4.2.1.1 and 4.2.1.2 demonstrate the effectiveness of the proposed rectifier supplementary controller to improve the LCC-HVDC system response under tap AC side faults at different pre-fault loading conditions. The LCC-HVDC system disturbance decreases as the faulted tap pre-fault current distribution decreases, which in turn reduces the magnitude of the supplementary current reference.

### 4.2.2 Inverter Supplementary Controller

As both the DC link voltage and the inverter current affect the magnitude of the inverter extinction angle, the inverter extinction angle controller is more prone to oscillations during system disturbances. For example, the LCC-HVDC current imbalance caused by the blocking of the faulted tap increases the inverter current, which in turn increases the commutation overlap and reduces the inverter extinction angle. As the extinction angle decreases, the inverter DC voltage also decreases which further increases the inverter current. The LCC-HVDC system will not settle at a new operating point until the interaction between the rectifier current controller and the inverter extinction angle controller is mitigated. Thus, the inverter DC voltage is selected as the input of the inverter supplementary controller to mitigate oscillations between controllers to enhance the LCC-HVDC system performance.

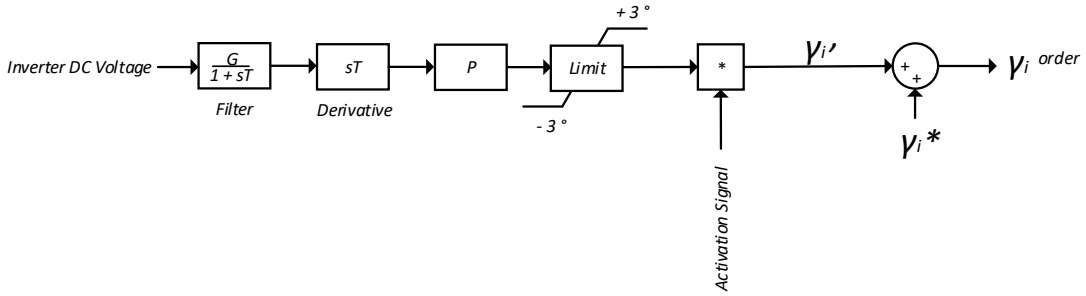


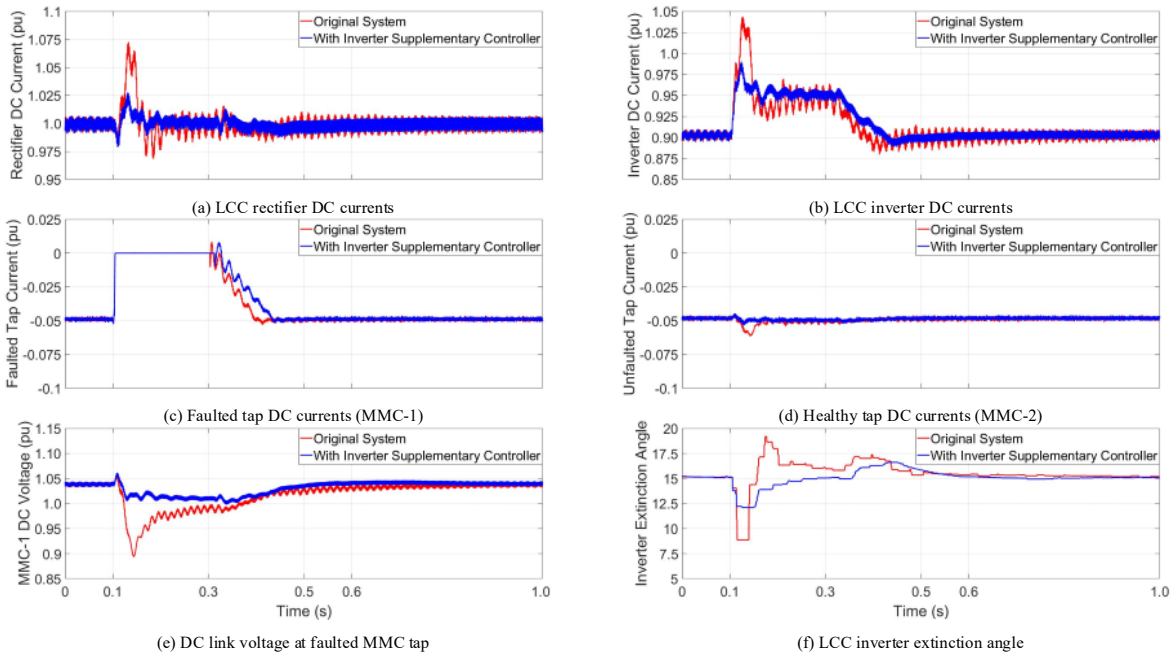

Figure 4.9: Inverter supplementary controller

The proposed inverter supplementary controller is shown in Fig. 4.9. The inverter DC voltage is first filtered and sent to a derivative block. The derivative of the filtered inverter DC voltage is then passed to a proportional controller and added to the inverter extinction angle reference ($\gamma_i{}^*$) to generate the modified extinction angle reference ($\gamma_i{}^{order}$). The supplementary

reference ($\gamma_i'$) is limited to $\pm 3°$ to prevent excessive variations in the reference signal. Under normal operation, the inverter supplementary controller is out of service with the activation signal equal to zero. The activation signal adopts the same logic as the mode stabilizer disabling scheme, therefore, the inverter supplementary controller is only activated in case of tap AC side faults.

#### 4.2.2.1 Tap AC Side Faults with High Loading Level

A SLG fault of 200 ms duration is applied to the AC terminal of MMC-1 tap. The pre-fault current reference of MMC-1 tap is set to -0.05 pu to extract 50 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

(f) LCC inverter extinction angle

Figure 4.10: System performance during faults with inverter supplementary controller (highly-loaded tap)

MMC-1 tap is blocked 4 ms after the occurrence of the SLG fault at t = 0.1 s. The rapid reduction of MMC-1 current leads to a current imbalance in the LCC-HVDC system, which further causes a momentary DC link voltage swell, as shown in Fig. 4.10(e). Upon detecting the rapid positive change in the DC link voltage at t = 0.106 s, the mode stabilizer is disabled and the inverter supplementary controller is activated to adjust the inverter extinction angle reference with respect to the rate of change of the DC link voltage. As seen in Fig. 4.10(e), with the inverter supplementary controller, the DC link voltage dip significantly improves from 0.89 pu to 1.01 pu.

The LCC rectifier and inverter current overshoots are also reduced from 1.075 pu to 1.028 pu and 1.044 pu to 0.99 pu, respectively, as shown in Figs. 4.10(a) and (b). With reduced DC link voltage fluctuations, the healthy tap is also subjected to less current oscillations, as shown in Fig. 4.10(d). Moreover, the minimum value of the inverter extinction angle is also improved from 8.8° to 12.1°, which significantly reduces the chance of commutation failure. At t = 0.3 s, the fault is cleared and MMC-1 current reference ramps back to its pre-fault value. It is observed that the LCC rectifier and inverter currents oscillations are much lower as compared to the original system. At t = 0.72 s, the mode stabilizer is re-activated as the inverter supplementary controller is disabled.

#### 4.2.2.2 Tap AC Side Faults with Medium Loading Level

A temporary SLG fault of 200 ms duration is applied to the AC terminal of MMC-1 tap. The pre-fault current reference of MMC-1 tap is set to -0.03 pu to extract 30 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.

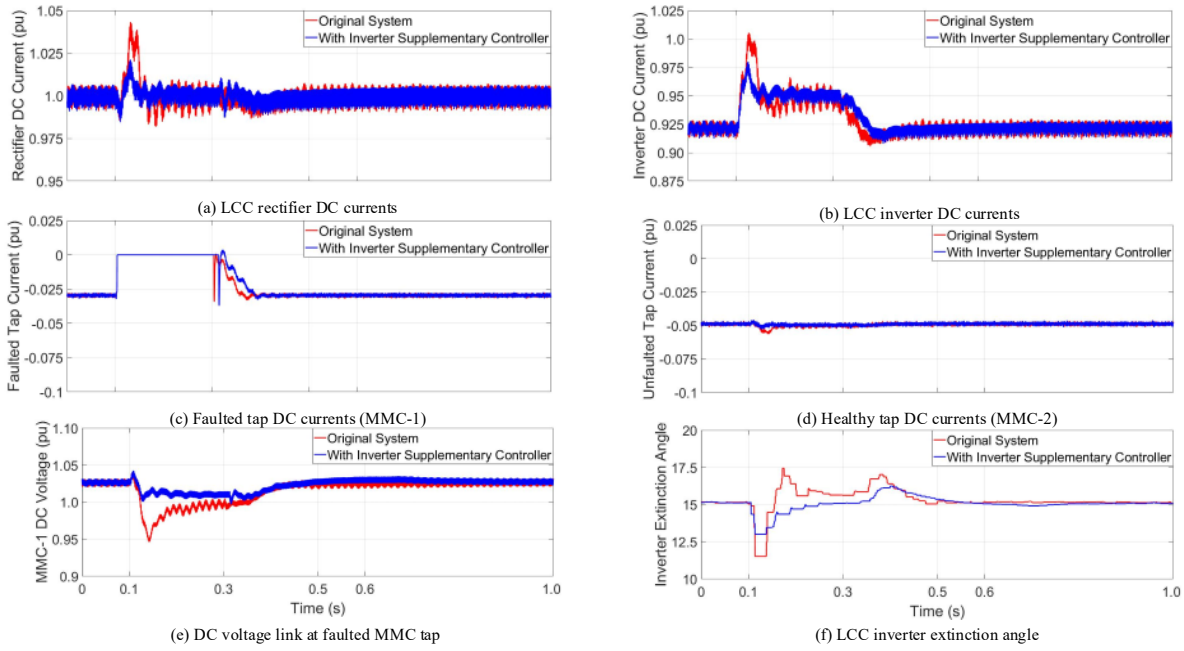



Figure 4.11: System performance during faults with inverter supplementary controller (medium-loaded tap)

The LCC-HVDC system performance improvement is similar to section 4.2.2.1. With the inverter supplementary controller, the magnitudes of the LCC rectifier and inverter current overshoots, the DC link voltage fluctuations, the transient inverter extinction angle reduction, and the healthy tap current oscillation are much lower as compared to the original system, Fig. 4.11.

Simulation results from sections 4.2.2.1 and 4.2.2.2 reveal the ability of the inverter supplementary control to enhance the LCC-HVDC system performance in the case of tap station AC side fault. The effectiveness of the inverter supplementary controller under different pre-fault operating conditions is verified. In particular, as the inverter supplementary controller is implemented at the DC link voltage regulating converter station, its ability to improve the DC link voltage is more significant as compared to the case with the rectifier supplementary controller. On the other hand, as the rectifier supplementary controller is adopted at the DC link current regulating station, its ability to improve the LCC-HVDC system DC link current is more significant.

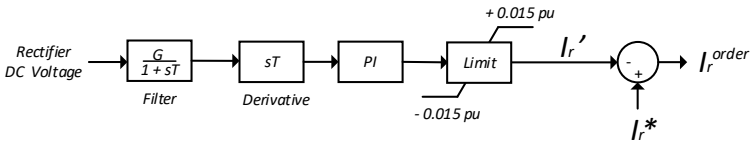
### 4.2.3 Combined Rectifier and Inverter Supplementary Controllers

As discussed in sections 4.2.1 and 4.2.2, the rectifier supplementary controller is more effective in improving the current response of the LCC-HVDC system whereas the inverter supplementary controller is more effective in enhancing the stability of the DC link voltage. This section explores the combination of the two supplementary controllers at the rectifier and inverter stations.

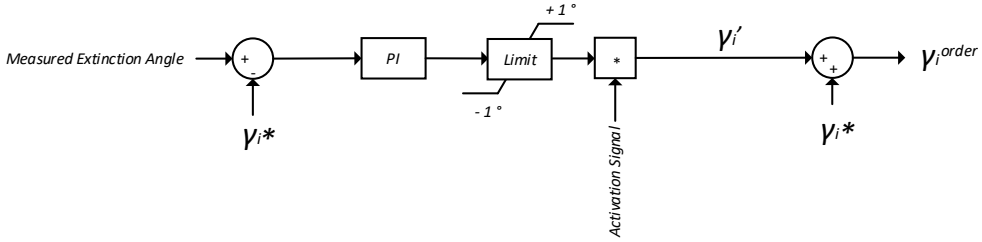
Directly incorporating the rectifier supplementary controller and the inverter supplementary controller proposed in sections 4.2.1 and 4.2.2 in the LCC-HVDC system would lead to undesirable interactions between the two supplementary controllers. The presence of the large DC smoothing reactors delays the rate of change of the DC link current and the speed of the current response with respect to changes in the DC link voltage. As a result, the response of the rectifier supplementary controller that utilizes the rectifier real power lags behind the inverter supplementary controller and causes LCC-HVDC system oscillations. Thus, changes are made to each of the supplementary controllers to enhance their coordination when used simultaneously.

The rectifier side supplementary controller proposed in this section takes the rectifier DC voltage as the input instead of the rectifier real power to minimize the delay of the system response, as shown in Fig. 4.12(a). The filtered rectifier DC voltage is first sent to a derivative block. The derivative of the filtered rectifier DC voltage is then passed to a PI controller to generate the

supplementary current reference ($I_r{}'$), which is then subtracted from the rectifier current order ($I_r{}^*$) to generate the modified rectifier current order ($I_r{}^{order}$). The magnitude of the supplementary current reference is limited to $\pm 0.015$ pu. The inverter side supplementary controller is also redesigned such that it takes the measured extinction angle as its input instead of the inverter DC voltage, as seen in Fig. 4.12(b). The calculated extinction angle error is first sent to a PI controller to generate the supplementary extinction angle reference ($\gamma_i{}'$), which is then added to the extinction angle reference ($\gamma_i{}^*$) to generate the modified extinction angle reference ($\gamma_i{}^{order}$). The magnitude of the supplementary extinction angle reference is limited to $\pm 1°$. Under normal operation, the inverter supplementary controller is out of service with the activation signal equal to zero. The inverter supplementary controller is deactivated when the supplementary extinction angle reference reaches zero, which is an indicator of polarity reversal of the extinction angle with respect to its initial value.




(a) Rectifier supplementary controller




(b) Inverter supplementary controller

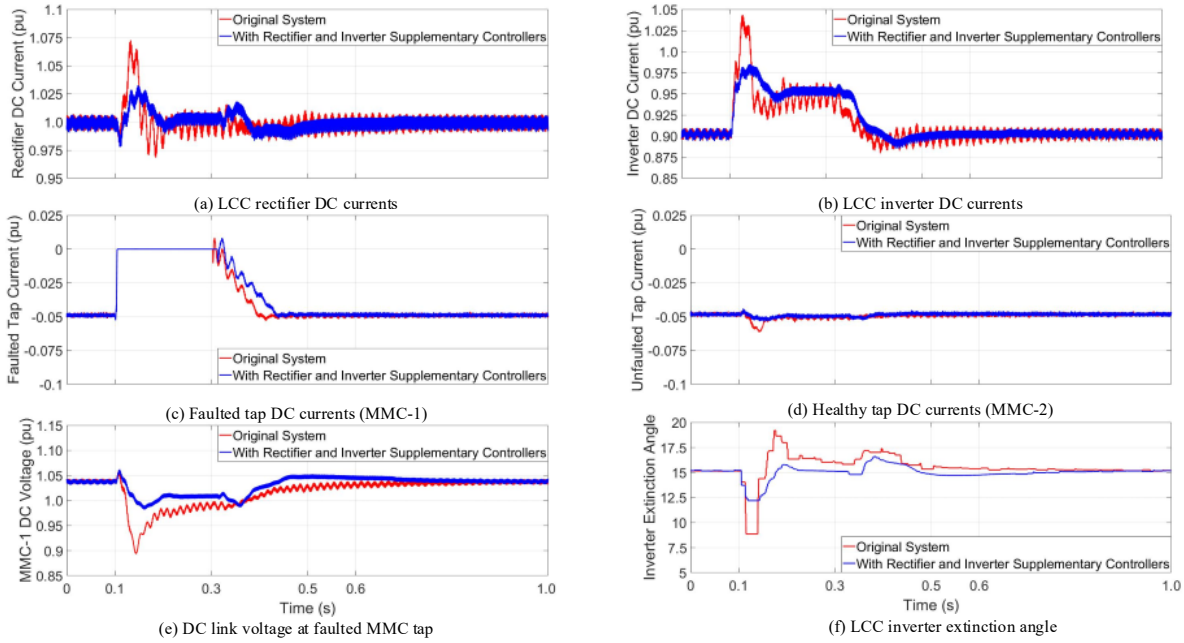
Figure 4.12: Combined rectifier and inverter supplementary controllers

#### 4.2.3.1 Tap AC Side Faults with High Loading Level

A SLG fault for 200 ms duration is applied to the AC terminal of MMC-1 tap. The pre-fault current contribution of MMC-1 tap is set to -0.05 pu to extract 50 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.

Prior to the occurrence of the fault, the supplementary current reference is nearly zero. After the fault occurrence, the tap AC side protection algorithm detects the SLG fault 4 ms into the fault and blocks MMC-1 tap causing its DC current to drop to zero within 2 ms, as shown in Fig. 4.13(c).

At t = 0.1055 s, the positive rate of change in the DC link voltage triggers the mode stabilizer disabling signal and activates the inverter supplementary controller. As seen in Figs. 4.13(a) and (b), with the combined rectifier and inverter supplementary controllers, the LCC rectifier and inverter current overshoots are reduced from 1.075 pu to 1.032 pu and 1.044 pu to 0.987 pu, respectively. As shown in Fig. 4.13(e), the DC link voltage dip is also improved from 0.893 pu to 0.982 pu. As a result of the reduced DC link voltage fluctuation, less current oscillation is observed at the healthy tap, as shown in Fig. 4.13(d). The transient extinction angle response is also improved from 8.8° to 12.2°, as depicted in Fig. 4.13(f). At t = 0.3 s, the fault is cleared with MMC-1 ramping its current reference back to its pre-fault operating condition. At t = 0.375 s, the supplementary extinction angle reference reaches zero and the inverter supplementary controller is thus disabled. The mode stabilizer is re-activated at t = 0.674 s. With the combined rectifier and inverter supplementary controllers, the LCC-HVDC system response during both the fault instant and the restoration period is improved significantly.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

(f) LCC inverter extinction angle

Figure 4.13: System performance during faults with combined rectifier and inverter supplementary controllers (highly-loaded tap)

### 4.2.3.2 Tap AC Side Faults with Medium Loading Level

A SLG fault for 200 ms duration is applied to the AC terminal of MMC-1 tap. The pre-fault current contribution of MMC-1 tap is set to -0.03 pu to extract 30 MW from the DC system. The detailed simulation sequence of operation can be found at the beginning of this chapter.

Similar LCC-HVDC system performance improvements are observed as compared to section 4.2.3.1. The magnitude of the LCC rectifier and inverter currents, the DC link voltage dip, the transient reduction of inverter extinction angle, and the current oscillation of the healthy tap are much lower with the combined rectifier and inverter supplementary controllers, as shown in Fig. 4.14.

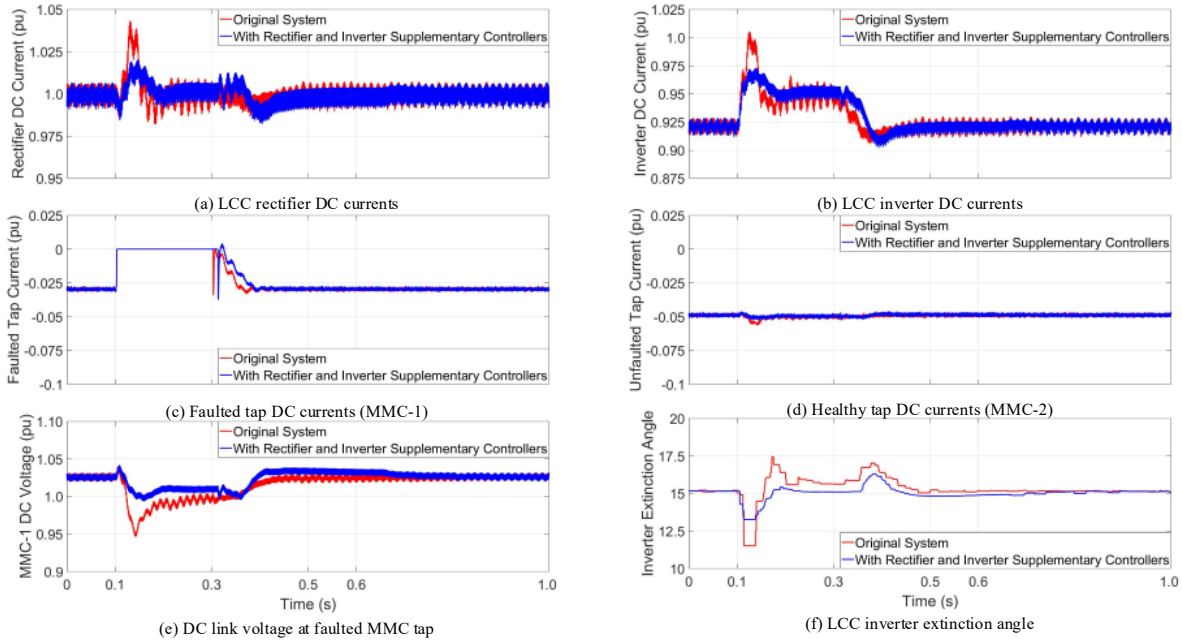



Figure 4.14: System performance during faults with combined rectifier and inverter supplementary controllers (medium-loaded tap)

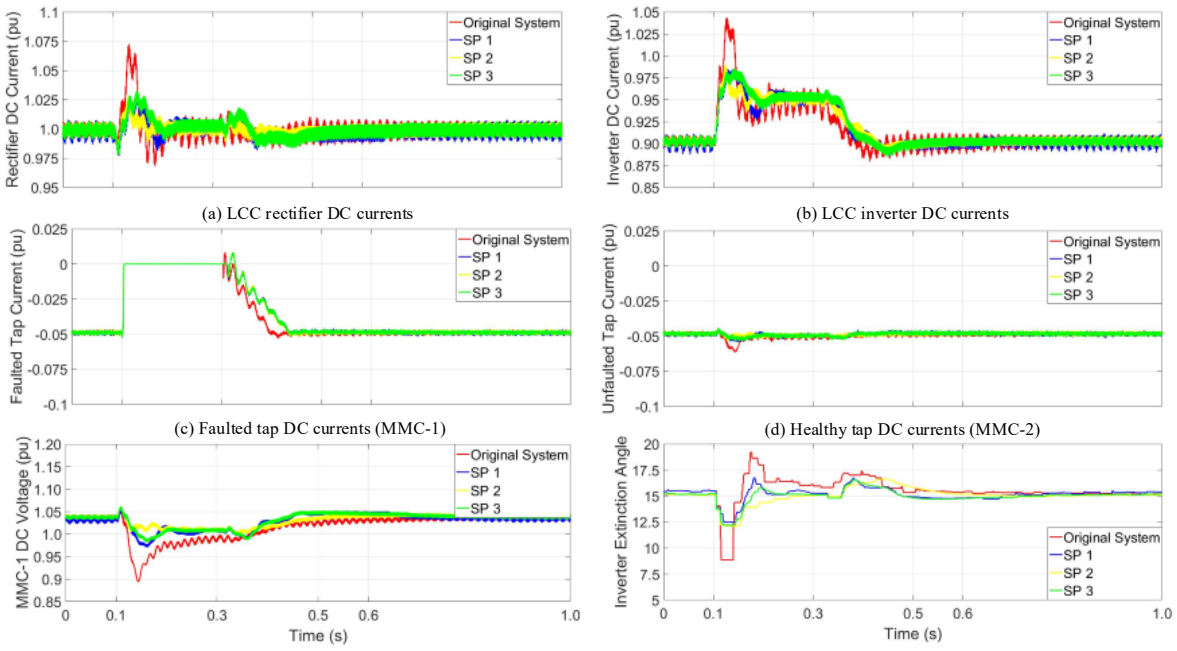
The rectifier and inverter supplementary controllers combine the advantages of each of the individual supplementary controllers to enhance the LCC-HVDC system performance. The effectiveness of the combined supplementary controller configuration is verified at two different pre-fault operating conditions reflective of high and medium loading levels. It is also noted that the combined rectifier and inverter controller configuration offers a better overall system

performance as compared to each of the rectifier supplementary controller and the inverter supplementary controller operating alone.

### 4.2.4 Comparison of Supplementary Controller Configurations

This section compares the LCC-HVDC system performance with each of the three different supplementary controller configurations in case of tap AC side faults. The rectifier, inverter, and combined rectifier and inverter supplementary controllers are denoted SP1, SP2, and SP3, respectively. As seen in Fig. 4.15(a), the magnitude of the LCC rectifier current overshoot is the highest with SP3 and the lowest with SP1. As SP1 is implemented in the current regulating station, it offers the highest current regulating capability. The LCC inverter current overshoot with SP3 is slightly lower than SP2 and SP1, as observed in Fig. 4.15(b). It is evident that the current response speed is the fastest with SP2 and consequently the associated system oscillation is the highest. On the other hand, SP3 has the slowest current controlling speed but features the smoothest current response as compared to SP1 and SP2. The faulted and healthy taps DC current responses, as shown in Figs. 4.15(c) and (d), are identical for all three supplementary controller configurations. The DC link voltage dip is the least severe with SP2 and the most severe with SP1, as seen in Fig. 4.15(e). As depicted in Fig. 4.15(f), the inverter extinction angle dip is the lowest with SP1 and the highest with SP2.

A brief comparison of the three supplementary controller configurations is shown in Table 4.1. SP1 offers the best performance in regulating the LCC rectifier and inverter currents. Conversely, SP2 implemented at the voltage regulating station features the best DC line voltage regulating capability. SP3 provides the most balanced current and voltage system performance enhancement by combining the advantages of both SP1 and SP2.




(a) LCC rectifier DC currents

(b) LCC inverter DC currents

(c) Faulted tap DC currents (MMC-1)

(d) Healthy tap DC currents (MMC-2)

(e) DC link voltage at faulted MMC tap

(f) LCC inverter extinction angle

Figure 4.15: System performance with different supplementary controller configurations during faults (highly-loaded tap)

Table 4.1: Performance comparison of supplementary controller configurations

| | **SP1 (rectifier)** | **SP2 (inverter)** | **SP3 (rectifier + inverter)** |
|---|---|---|---|
| **Rectifier current overshoot** | Lowest | Normal | Highest |
| **Inverter current overshoot** | Normal | Highest | Lowest |
| **DC link voltage dip** | Highest | Lowest | Normal |
| **Inverter extinction angle dip** | Lowest | Highest | Normal |
| **Controller response speed** | Normal | Highest | Lowest |
| **Smoothness of system response** | Normal | Lowest | Highest |

## 4.3 Summary

This chapter verifies the ability of the proposed tap station current modulation controller and the three supplementary controller configurations to enhance the LCC-HVDC system performance in case of tap AC side faults via extensive simulations. The tap station current modulation method is proved to be an effective approach to reduce the DC link current overshoot, the transient DC link voltage fluctuation, and the inverter station extinction angle sag; however, the proposed method is limited to LCC-HVDC systems with two taps. The triggering threshold of the controller has to be carefully selected to avoid misoperation yet maintaining adequate fault detecting sensitivity. The tap station current modulation method requires additional devices or control measures implemented at the tap stations to deal with the excess energy (albeit for a short time). On the other hand, the three supplementary controller configurations that utilize only local measurements do not require any additional device and are easy to implement. The rectifier supplementary controller is more effective in regulating the LCC-HVDC currents whereas the DC voltage regulating capability of the inverter supplementary controller is more superior. The combination of rectifier and inverter supplementary controllers offers the most balanced performance enhancement of the LCC-HVDC system.

# Chapter 5

# Conclusion

With the increasing number of HVDC systems commissioned around the world and the recent advancement of power electronic devices, the idea of tapping to extract a small amount of power from existing HVDC lines to minimize the infrastructure cost and the control complexity in electrifying rural communities is experiencing renewed attention. Tapping schemes utilizing classical LCC-based technology are subjected to operational limitations and can be challenging to implement. The recently introduced MMC has many advantages over the conventional LCC technology and therefore is a favorable candidate for tapping applications.

This thesis analyzes the operation and control of the hybrid LCC-MMC multi-tapping study system comprised of the CIGRÉ LCC benchmark model and two FB-MMC taps. The impacts of tap stations on the main LCC-HVDC system during both normal and abnormal conditions are studied. In particular, special attention is paid to the MMC tap AC side fault as it introduces a new point of failure to the LCC-HVDC system. Simulation results revealed that undesirable disturbances are imposed on the LCC-HVDC system as a result of tap station AC side faults, thus fault mitigation methods are developed to improve the LCC-HVDC system response.

## 5.1 Thesis Contribution

The contributions of this thesis are summarized as follows:

1. The feasibility of tapping an LCC-HVDC system with two FB-MMC taps under both normal and abnormal operating conditions are evaluated through extensive simulations at different current set-points. Under normal condition, the ability of tap stations to

extract/inject power is verified. Moreover, it is revealed the LCC-HVDC system response in case of tap station AC side faults is similar regardless of the location of the tap station along the LCC-HVDC line or the fault location along the tap station AC line. However, it is observed that the blocking of an MMC tap due to its AC line SLG fault imposes undesirable disturbances on the main LCC-HVDC system, which may result in the failure of the entire HVDC system.

2. The proposed tap station current modulation method is implemented in each of the MMC taps to improve the transient response of the LCC-HVDC system in case of tap AC side faults. The current contribution of the opposite MMC tap is continuously estimated based on local measurements at tap stations. When the opposite MMC tap is subjected to an AC side fault, the healthy MMC transiently adjusts its current reference to minimize the current imbalance experienced by the LCC rectifier and inverter controllers. Simulation results verified the ability of the tap station current modulation method to improve the LCC-HVDC system response in case of tap AC side faults.
3. Three different supplementary controller configurations are designed to alleviate the system disturbance imposed on the LCC-HVDC system in case of tap AC side faults. The rectifier supplementary controller adopted at the DC link current regulating station features the most improved current response. On the other hand, the inverter supplementary controller implemented at the DC link voltage setting station offers the most improved DC link voltage response. The combined rectifier and inverter supplementary controller configuration provides the most balanced DC link voltage and current improvements. The effectiveness of the three supplementary controller configurations is verified at different pre-fault operating conditions through extensive simulations.
4. The development of the detailed hybrid multi-tapping study system in PSCAD/EMTDC forms the basis of a comprehensive study system to evaluate tapping of LCC-HVDC systems with MMCs. The study system also provides a convenient testing environment for research into fault behavior of tapping stations and the development of new supplementary control schemes and fault mitigation methods.

## 5.2 Future Work

A list of future works is as follows:

1. Analyze the response of MMC taps under DC pole-to-ground faults, LCC rectifier and inverter AC voltage depressions, and HVDC line power flow reversals.
2. Development of alternative supplementary controllers using analytical methods.
3. Development of new fault mitigation methods assuming availability of a communication channel between tap stations.
4. Feasibility and cost-benefit analysis of HVDC systems with more than two tap stations.
5. Revision of the tap station current modulations method to accommodate for HVDC systems with more than two tap stations.
6. Feasibility analysis of tapping with MMCs utilizing mixed cells or a combination of half-bridge and full-bridge submodules to reduce conduction losses and to achieve cost savings.
7. Control hardware-in-the-loop testing of supplementary controllers via real-time digital simulation.

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