SMALLER/FASTER DELTA-SIGMA DIGITAL PIXEL SENSORS

by

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Abstract

A digital pixel sensor (DPS) array is an image sensor where each pixel has an analog-to-digital converter (ADC). Recently, a logarithmic delta-sigma ($\Delta\Sigma$) DPS array, using first-order $\Delta\Sigma$ ADCs, achieved wide dynamic range and high signal-to-noise-and-distortion ratios at video rates, requirements that are difficult to meet using conventional image sensors. However, this state-of-the-art $\Delta\Sigma$ DPS design is either too large for some applications, such as optical imaging, or too slow for others, such as gamma imaging. Consequently, this master's thesis investigates smaller or faster $\Delta\Sigma$ DPS designs, relative to the state of the art. All designs are validated through simulations. Commercial image sensors, for optical and gamma imaging, are used as targeted baselines to establish competitive specifications. To achieve a smaller pixel, process scaling is exploited. Three logarithmic $\Delta\Sigma$ DPS designs are presented for 180, 130, and $65\,\mathrm{nm}$ fabrication processes, demonstrating a path to competitiveness for the optical imaging market. Decimator and readout circuits are improved, compared to previous work, while reducing area, and capacitors in the modulator prove to be the limiting factor in deep-submicron processes. Area trends are used to construct a roadmap to even smaller pixels. To achieve a faster pixel, a higher-order $\Delta\Sigma$ architecture is exploited. A complete image sensor, encompassing a logarithmic $\Delta\Sigma$ DPS array and peripheral circuits, such as bond pads, is designed, where each DPS uses a second-order $\Delta\Sigma$ ADC. To maximize fill factor, the image sensor is developed for a two-tier $130\,\mathrm{nm}$ fabrication process, a 3D integrated circuit process. Done in collaboration with an industry partner, this fourth design helps to establish the feasibility of a fully-integrated gamma image sensor. Gamma imaging requirements, such as high frame rate, are taken into account. The thesis finishes by examining technology readiness levels, and offering maturation

plans, for the four presented designs. In conclusion, the thesis helps to make logarithmic $\Delta\Sigma$ DPS arrays competitive for targeted applications.

Preface

Chapter 2 gives the design of a delta-sigma digital pixel sensor in the 180, 130, and $65\,\mathrm{nm}$ technology nodes. Part of this work, related to the decimator circuit, was published as follows:

- Erika Azabache Villar, Orit Skorka, and Dileepan Joseph, "Small-area decimators for delta-sigma video sensors," *Proceedings of the SPIE NBIT Sensors and Systems Conference*, vol. 9060, pp. 1–11, Apr. 2014.

Furthermore, Chapter 3 presents the initial design of a fully-integrated gamma image sensor. It was developed using the Tezzaron two-tier $130\,\mathrm{nm}$ process, a 3D integrated circuit process. This work was included in a technical report as follows:

- Erika Azabache, Shuang Xie, Vitaliy Degtyaryov, and Dileepan Joseph,"Digital Pixel Sensor Design for a Gamma Ray Image Sensor," Tech. Rep., University of Alberta and Phantom Motion, pp. i–viii 1–32, Apr. 2015.

For the conference proceeding, I was responsible for manuscript writing and editing, as well as schematic design, simulation, verification, and layout of all circuits. Also, I was responsible for data processing and analysis. Orit Skorka contributed to the creation of original figures and to concept formation. Dileepan Joseph was the supervisory author and contributed to concept formation, manuscript composition and editing, and data analysis.

For the technical report, which contains four chapters, I was responsible for the writing and editing of Chapters 2 and 4. Also, I was responsible for the complete design of the image sensor, which included schematic design, simulation, verification, and layout of all circuits. Shuang Xie contributed to writing and editing of Chapters 3 and 4 and data analysis. Vitaliy Degtyaryov contributed to concept formation. Dileepan Joseph was the supervisory author and, apart from writing Chapter 1, contributed to concept formation, manuscript composition and editing, and data analysis.

To Lalo,
who always keeps me moving forward.

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My gratitude also goes to Victor for being by my side through this phase of my life. This adventure began the day he jokingly said "Brazil is just too warm, we should start looking for colder places to live." We never thought those words would change our lives in a wonderful way. Thanks for the encouragement and for being willing to catch planes and meet at airports for almost three years. Though it is sad this phase is ending, I am ecstatic about starting a new chapter of our lives together.

I would also like to thank Dr. Joseph for his supervision and support but, above all, for his patience. I'm grateful for the innumerable hours he has committed to reading my thesis and, in general, for his dedication to his students. It was only until I started working under his supervision that I truly understood the importance of effectively presenting research results. With him I learned more than just technical skills, I learned skills that I can apply in my everyday life. His guidance and insights played a great part in the completion of this thesis.

This thesis would not have been possible without the encouragement and support from friends and family from here, there, and everywhere. I'm thankful for the friendships I forged here and that I hope are for life. Thanks Geoff, Rodrigo, and Jorge for the coffee breaks, for the great times, and for your friendship. I would like to especially thank Patty for being a sister to me and for being caring and kind. You and Jeremiah made me feel as if I had a family here in Edmonton. Thanks to Cesar, Tal, Eli, and Gaby, who always cheer for me from different parts of the world. I'm lucky to have you as my friends despite the distance. Also, thanks to my family, the one I grew up with and the one I won when I married Victor, who have been with me in every step of this journey.

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Chapter 1

Introduction

Among the different types of modern electronic image sensors, digital pixel sensors are of interest because they convert luminance information, sensed by a photodetector, into a corresponding digital value at pixel level. By realizing the analog-to-digital conversion at pixel level, they enable lower noise, *i.e.*, better image quality, at higher frame rates, because analog signals are not carried outside the pixel for subsequent conversion at either column, chip, or board level.

Recently, Mahmoodi and Joseph [1] introduced a novel digital pixel sensor (DPS) architecture, which integrates a logarithmic sensor, a delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC), and readout circuitry in each pixel. The $\Delta\Sigma$ ADC in this architecture includes a first-order modulator and a bit-serial decimator. A DPS array of this kind achieved both high dynamic range (DR), *i.e.*, over $110\,\mathrm{dB}$, and high peak SNDR (PSNDR), *i.e.*, $45\,\mathrm{dB}$, at video rates, *i.e.*, $30\,\mathrm{fps}$, which is difficult to do according to a recent review of modern electronic image sensors [2].

Although the $\Delta\Sigma$ DPS design was intended for visible-band imaging, its pixel size was above the typical value for that band [3]. Larger pixels are acceptable for imaging in bands outside the visible spectrum, like for instance gamma imaging, which is a lens-less application. However, there are other application requirements to consider with other bands.

In short, for Mahmoodi and Joseph's $\Delta\Sigma$ DPS architecture to be practical for optical imaging, the pixel size has to be significantly reduced. Though improvements to the design can be made to make it smaller, this design could also benefit from process scaling and vertical integration, two trends in the semiconductor industry that enable area reduction.

While applications other than optical imaging, such as gamma imaging, have a more relaxed pixel pitch requirement, they may be required to work at much higher frame rates (on the order of MHz), compared to visible-band applications, due to application requirements. A first-order $\Delta\Sigma$ ADC, used in Mahmoodi and Joseph's architecture, is far less suitable for these

rates due to its need for a high oversampling ratio (OSR). A second-order $\Delta\Sigma$ ADC offers a good means to reduce the OSR without compromising image quality.

Therefore, the objectives of this thesis are to develop $\Delta\Sigma$ DPS designs that are smaller or faster than the state of the art. Toward that end, the rest of this chapter is organized as follows. Section 1.1 reviews the background for this work. It justifies our interest in DPS technology, in general, and in Mahmoodi and Joseph's $\Delta\Sigma$ DPS design, in particular, analyzing its strengths and current limitations. Section 1.2 explains the methodology used for the design of smaller pixels, by dual trend exploitation, and for faster ones, by using a higher-order architecture. Finally, Section 1.3 defines the scope of this work by establishing the targeted applications as well as the chosen method of verification. It also outlines the subsequent chapters of this thesis.

1.1 Background

This section reviews relevant background for the realization of this thesis. It discusses DPS architectures and, in particular, $\Delta\Sigma$ DPS architectures. Furthermore, it gives an overview of the $\Delta\Sigma$ DPS architecture that was chosen to design both smaller area and faster rate pixels. Also, it points out the limitations that have to be overcome with the chosen architecture.

Section 1.1.1 describes the options that have been explored to implement analog-to-digital conversion at pixel level, from approaches limited to imaging to the ones known in classical data conversion. Also, it lists the many advantages that the DPS architecture has over passive pixel sensor (PPS) and especially over active pixel sensor (APS) ones. The APS architecture is the most adopted one.

Section 1.1.2 explains the principles behind $\Delta\Sigma$ data conversion and how when applied to a DPS it could be beneficial in terms of performance, compared to other classical conversion methods. Also, the section reviews work done on $\Delta\Sigma$ DPS designs. Furthermore, it highlights in particular the benefits of using the $\Delta\Sigma$ DPS proposed by Mahmoodi and Joseph.

Finally, Section 1.1.3 points out the limitations of the $\Delta\Sigma$ DPS proposed by Mahmoodi and Joseph. These limitations are related to commercial applications in visible and invisible bands.

1.1.1 Digital Pixel Sensor (DPS)

CMOS image sensors are composed of an array of pixel sensors, which can be of PPS, APS, or DPS type. In addition to a photodiode, PPS image sensors have a single readout transistor per pixel, thus achieving small pixel size and high fill factor; however, they are slow and have low signal-to-noise ratio (SNR). APS image sensors add an amplifier to the PPS circuit, improving its speed and SNR, so they trade fill factor for performance. The PPS and APS architectures

Table 1.1: Sources of noise in APS and DPS image sensors. Because analog-to-digital conversion is done at pixel level, DPS image sensors present less noise than APS image sensors with column level ADCs. Inspired by Chi *et al.* [6].

Type of Noise	APS	DPS
Detector Noise	✓✓	✓✓
Readout	✓	
Pixel FPN	✓✓	✓
Column FPN	✓✓	
Amplifier Noise	✓	✓

can be considered "analog pixel sensor" architectures because their circuitry and pixel outputs are analog, even when used as part of a digital camera.

Newer technology nodes are being continuously developed, facilitating transistor miniaturization, thereby making pixels with a larger number of transistors per unit area viable. However, this trend also has a negative effect on the performance of analog circuits [4], especially in submicron complementary metal-oxide-semiconductor (CMOS) processes. The APS output depends on the supply voltage and the threshold voltage. Because in newer technologies supply voltage reduction is faster than threshold voltage reduction and due to the APS output range dependence on technology node parameters, the DR of the APS output is negatively affected in nanoscale processes [5]. Therefore, although currently the APS architecture is widely adopted, the impact that nanoscale processes would have on APS image sensor performance could make it difficult to maintain their advantages over other options [6].

Furthermore, from the noise performance point of view, there are two types of noise that affect image sensors: temporal (random) noise and fixed pattern noise (FPN) [6]. Temporal noise varies from frame to frame. It is composed of detector (shot), amplifier, and readout noise. In addition to integration time, detector noise depends on the photocurrent, dark current, and capacitance at the node connected to the photodetector, which in turn depend on the physical characteristics of the photodetector. Amplifier noise depends on the physical characteristics of CMOS devices such as transistors, resistors, and capacitors and can manifest as thermal and flicker noise. Readout noise is generated when carrying analog signals outside the pixel array to an ADC.

FPN is present due to component mismatch, so it varies spatially rather than temporally. It is composed of pixel FPN and column FPN. There are methods developed to counteract the effects of pixel and column FPN [7]. However, if digitization were done at pixel level, the sources of FPN noise that could affect the image sensor may be reduced, improving its signal-to-noise-and-distortion ratio (SNDR), as summarized in Table 1.1.

Image sensor performance can be measured in terms of SNDR and DR. Higher SNDR is related to better image quality while wider DR means that the range of brightness that can be captured without causing saturation is increased [3]. One potential pathway to achieve image sensors with higher performance is to go from APS to DPS architectures.

DPS image sensors include an ADC in each pixel, having digital outputs rather than analog ones. Because all pixels operate in parallel, high-speed readout and, consequently, video applications with higher rates are enabled. Furthermore, techniques for DR extension, such as multiple capture, can be applied [8].

Several DPS architectures can be found in the literature. As established by Skorka and Joseph [3], we can classify DPS architectures in two groups, depending on the in-pixel analog-to-digital conversion method used, as non-classical and classical ADC architectures. Non-classical ADC architectures provide a digitized output by taking advantage of device-specific properties of the photodetectors, such as its capacitance. Classical ADC architectures, on the other hand, use conventional ADCs, which may be optimized for imaging applications, to produce a digitized output from an intermediate analog signal produced after photodetection and preamplification.

Non-classical ADC architectures can be classified into two subgroups: photodiode-based and single-photon avalanche diode (SPAD)-based [3]. Photodiode-based DPS image sensors take their name from the fact that the photodetector is a p-n junction operating in the photodiode region, which uses reverse-bias voltages well below the breakdown voltage. Depending on the method used for the digital conversion, this subgroup can be further divided into two categories: time to first spike (TTFS) and pulse-frequency modulation (PFM) [3].

The TTFS DPS is shown in Fig. 1.1(a). At the beginning of a frame, the control unit resets the cathode voltage of the photodiode, V_{PD}, to its initial value, which is approximately the supply voltage. This voltage charges the photodiode capacitance. After the brief reset, the reset transistor is turned off and the photodiode discharges. The comparator senses the cathode voltage and compares it to a reference voltage, V_{ref}. When V_{PD} is lower than V_{ref} the comparator sends a pulse signal to the memory unit to store the digital integration time, provided by a global counter. This pulse also causes the control unit to reset V_{PD} and a new conversion starts. Under brighter light, less discharge time is required, so a lower value is stored in the memory. Similarly, under dimmer light, more discharge time is required, so a higher value is stored in the memory.

The PFM DPS is shown in Fig. 1.1(b). It works similarly to the TTFS DPS except that the output is a frequency rather than a number that represents the brightness level of the pixel. When V_{PD} is lower than V_{ref} the comparator sends a pulse signal to the counter and causes a reset of the photodiode cathode voltage. The counter gives the number of times V_{comp} was

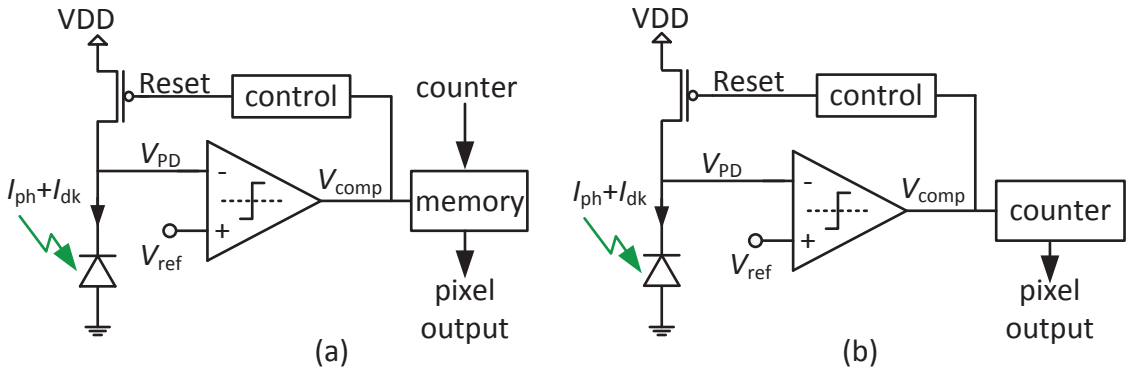


Figure 1.1: Photodiode-based DPS architectures. Schematic diagrams of (a) TTFS and (b) PFM DPS circuits. Taken from Skorka and Joseph [3].

pulsed high in a fixed period, *i.e.*, the frame time. At the end of the frame time a converted value is available at the output of the pixel and then the counter is reset to zero. Under brighter light, less discharge time is required, so higher pulse frequencies are registered at the output. Similarly, under dimmer light, more discharge time is required, so lower pulse frequencies are registered at the output.

SPAD-based DPSs employ p-n junctions that operate in the avalanche region, which requires reverse-bias voltages well above the breakdown voltage. Under this condition, the electric field is so high that a single carrier injected into the depletion layer can trigger a self-sustained avalanche. Because they work at such high voltages isolation is necessary, which means pixels require more area for guard-ring placement. Therefore, SPAD-based DPSs are more suitable for applications where large pixels are acceptable [3]. Depending on the method used for digital conversion, they can be divided mainly into two categories: passive quenching (PQ) and active quenching (AQ).

The PQ DPS is shown in Fig. 1.2(a). Once a photon is detected by the photodetector, *i.e.*, the SPAD, the avalanche effect produced by this detection increases the current through the photodetector abruptly. In order to detect subsequent photons, the avalanche effect needs to be stopped, *i.e.*, quenched. This can be done by putting a resistor in series with the photodetector that will create enough voltage drop across it, due to generated photocurrent, so the cathode voltage drops below the breakdown voltage. Every time a photon is detected the comparator, which works as an edge pulse detector, increases the photon count.

The main drawback of the PQ approach is that it presents slow voltage reset and ill-defined dead time [9]. The AQ DPS, shown in Fig. 1.2(b), was introduced to overcome these issues. Basically, the pulse generator sets the bias voltage to a value higher than the breakdown voltage, between photon detection events, and below the breakdown voltage, when detection happens. This method is faster than the PQ technique because it depends less on the characteristics of

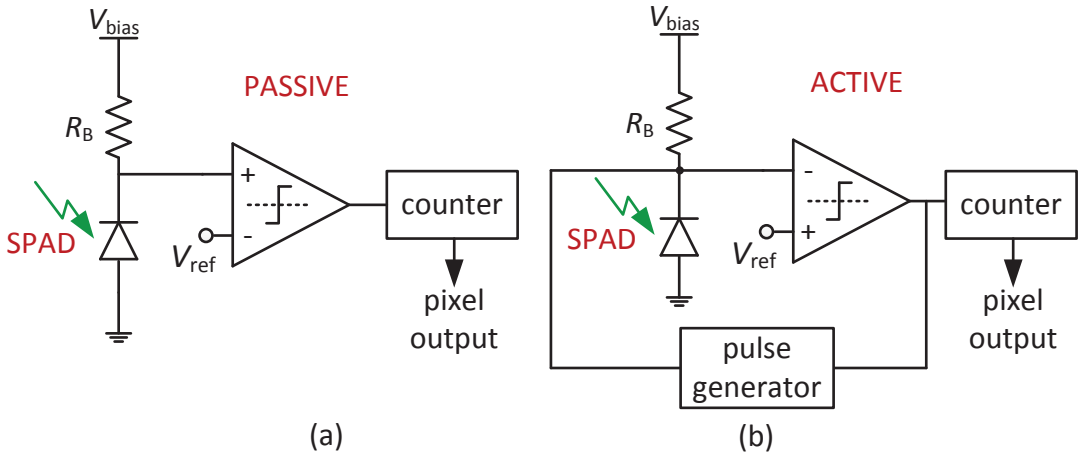


Figure 1.2: SPAD-based DPS architectures. Schematic diagrams of (a) PQ and (b) AQ DPS circuits. Taken from Gallivanoni *et al.* [9].

passive elements, which are also subject to process variation. Still, the quenching time can be significant because in order to quench it has to detect the avalanche current first, among other factors [9]. The AQ approach trades quenching time for complexity.

As mentioned before, a DPS can also be designed by including a classical (conventional) ADC in the pixel. As summarized in Table 1.2, several attempts to find the most suitable ADC architecture to be included in an image sensor, at pixel level, have been undertaken [10, 11, 12, 13, 14, 15, 16, 17, 2]. Most of these attempts have been done by the Information Systems Laboratory at Stanford University, where three generations of DPS designs were developed.

The ADCs used can be divided into Nyquist-rate and oversampling ADCs. The second CMOS DPS developed used a $\Delta\Sigma$ modulator per colour pixel, *i.e.*, per 2×2 pixels. This was done, partly to reduce the effective size of an earlier $\Delta\Sigma$ modulator pixel sensor. Even though this architecture had good performance in terms of DR and peak SNR (PSNR), the fill factor was greatly reduced, compared to APS approaches, due to a greater number of transistors included in a pixel. To solve this problem, Nyquist-rate architectures were explored [8]. The approach presented by Bidermann *et al.* [16] is the only one in Table 1.2 that has been commercialized. This approach presented good performance in terms of DR and SNR, comparable to the last DPS listed.

1.1.2 Delta-Sigma ($\Delta\Sigma$) DPS

Section 1.1.1 described the different options that have been explored to implement a DPS. Also, it listed the many advantages that the DPS architecture has over its analog counterparts. Here, the interest of this thesis in $\Delta\Sigma$ DPSs over other types of DPS is justified. Concepts

Table 1.2: Summary of classical-ADC DPS designs. Whereas most DPS designs use one ADC per pixel, Yang *et al.*'s and Bidermann *et al.*'s designs share one ADC over four pixels.

CMOS DPS	Node (μm)	Area (μm^2)	ADC type	Transistors (per pixel)	Application
Fowler *et al.* [10]	1.2	60×60	$\Delta\Sigma$ modulator	22/1	Optical
Yang *et al.* [11]	0.8	20.8×20.8	$\Delta\Sigma$ modulator	17/4	Optical
Yang *et al.* [12]	0.35	10.5×10.5	MCBS	18/4	Optical
Joo *et al.* [13]	0.8	125×125	$\Delta\Sigma$ modulator	35/1	Optical
McIlrath [14]	0.5	30×30	$\Delta\Sigma$ modulator	19/1	Optical
Kleinfelder *et al.* [15]	0.18	9.4×9.4	Ramp-compare	37/1	Optical
Bidermann *et al.* [16]	0.18	7×7	MCBS	22/4	Optical
Rocha *et al.* [17]		36×36	$\Delta\Sigma$ modulator	19/1	X-ray
Mahmoodi *et al.* [2]	0.18	38×38	$\Delta\Sigma$ ADC	275/1	Optical

behind $\Delta\Sigma$ data conversion and its relevance in the context of image sensors are explained.

As mentioned in Section 1.1.1, a DPS can be implemented by including a classical ADC at pixel level. There are several options for implementing classical ADCs, as shown in Fig. 1.3. These options can be divided into two main groups: Nyquist-rate and oversampling ADCs. Each ADC type is suitable for a certain application depending on its sampling rate and bit resolution requirements. For target applications that require high bit-resolution for low sampling rate, which is the case of pixel-level ADCs for image sensors, oversampling ADCs are a good choice in comparison to Nyquist-rate ones.

Oversampling ADCs, at the same time, can be divided into predictive and noise-shaping oversampling ADCs. Predictive oversampling ADCs use the present value of the signal to predict its future value. The difference between the actual and predicted values, called the error, is quantized, integrated, and returned to its analog form to generate a new prediction [19]. Both the signal and quantization noise spectrums are shaped. Noise-shaping oversampling ADCs, also known as $\Delta\Sigma$ ADCs, use a feedback loop to achieve their noise-shaping capability. Unlike predictive oversampling ADCs, only the quantization noise spectrum is shaped.

In order to understand the concept behind oversampling, the quantization noise, which is the noise (error) generated in the process of converting an analog value into a corresponding digital value, is assumed to be additive white noise having a uniform distribution. This approximation is good provided the signal at the input of the ADC includes random analog noise on the order of (or greater than) the quantization step size. Therefore, the quantization noise is assumed to be uncorrelated with the input signal and its power spectral density is white [20].

The quantization noise power, or noise variance, can be calculated by integrating the power

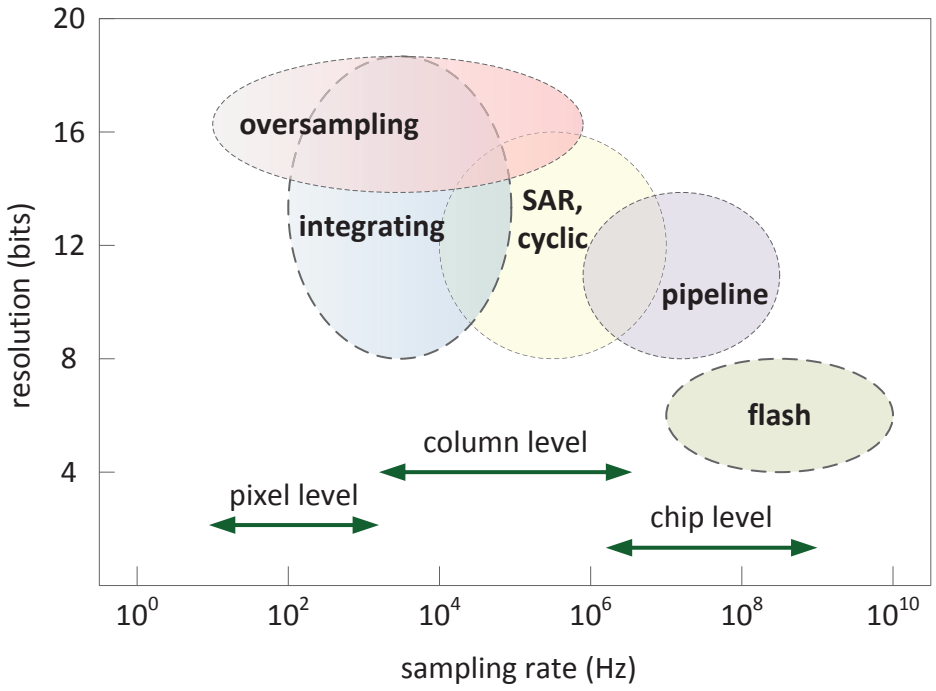


Figure 1.3: Design space of various ADC types. Depending on desired bit resolution and sampling rate, different types are ideal. A $\Delta\Sigma$ ADC is suitable for pixel-level data conversion. Adapted from Mahmoodi [18] by Skorka.

spectral density over the ADC bandwidth. But this value must equal $\Delta^2/12$, where Δ is the quantization step size. Because bandwidth depends on sampling rate, when the ADC bandwidth is extended by oversampling the signal several times the Nyquist rate, the power spectral density (PSD) drops to keep the power constant. In other words, oversampling redistributes the same noise power over a wider spectrum, as illustrated in Fig. 1.4. This allows overall noise reduction by using a digital low-pass filter designed to pass the Nyquist bandwidth while filtering out higher-frequency components.

To understand the concept behind noise shaping, we must realize that it is not desirable for the noise PSD to be white. A non-flat PSD, with most of the noise power outside the signal band, is preferable. This kind of PSD can be achieved with a $\Delta\Sigma$ modulator. Here, to illustrate noise-shaping, a first-order $\Delta\Sigma$ modulator is used, as shown in Fig. 1.5, but the same concept can be applied to higher-order $\Delta\Sigma$ modulators.

The output, $y_u[n]$, produced by a first-order $\Delta\Sigma$ modulator can be expressed as [21]

$$y_u[n] = x[n-1] + e[n] - e[n-1], \tag{1.1}$$

where $x[n-1]$ is the input signal and $e[n]$ is the quantization noise signal. Taking the z-

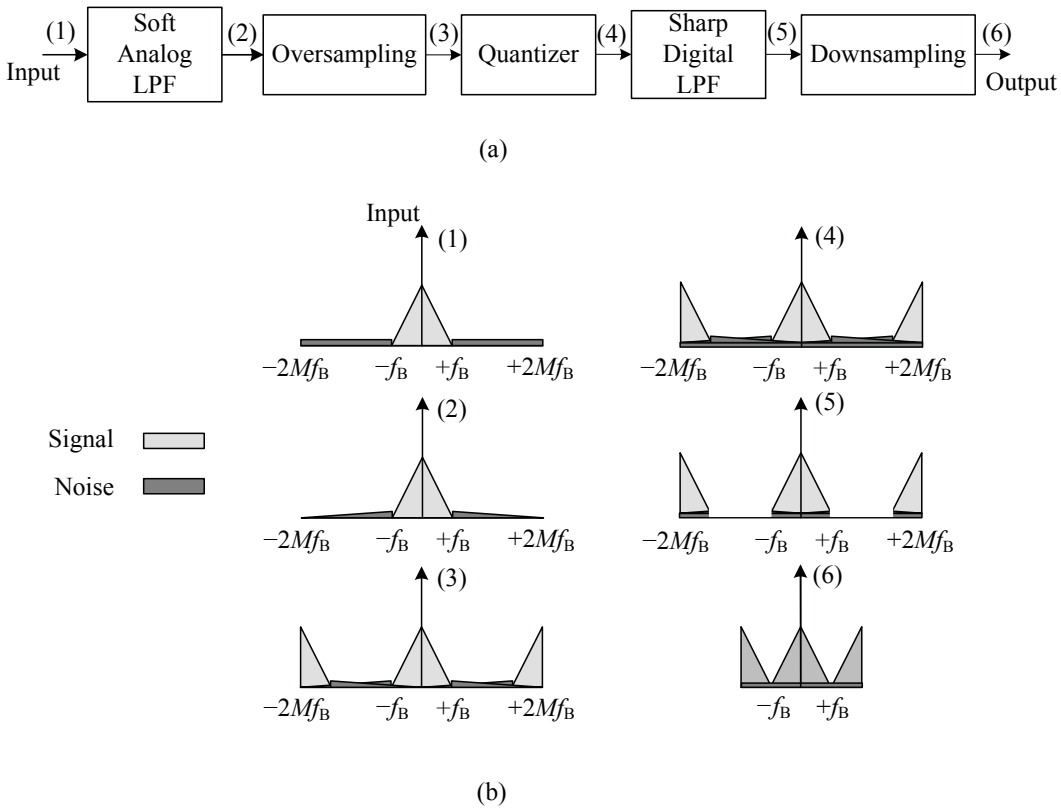


Figure 1.4: Oversampling ADC. (a) Block diagram and (b) signal and noise power spectrums at each stage of the ADC, taken from Mahmoodi [18].

transform, (1.1) may be rewritten as follows:

$$Y_u(z) = z^{-1}X(z) + (1 - z^{-1})E(z). \tag{1.2}$$

From (1.2) we can see that the $\Delta\Sigma$ modulator acts as a unit delay to the input signal while acting as a high-pass filter to the quantization noise. Therefore, most of the quantization noise power is pushed into higher frequencies, as shown in Fig. 1.5(c).

Another important part of $\Delta\Sigma$ analog-to-digital conversion is the decimation process, which is performed after modulation. The output of the decimator represents the analog signal at the modulator input using a lower bit rate than the stream that comes from the modulator output, but with more bits per sample. The decimator filters out-of-band components and quantization noise, as shaped by the $\Delta\Sigma$ modulator. Also, it downsamples the filtered signal to the Nyquist rate [20].

Reviewing the established theory for standalone ADCs [22], given a modulator of order l, a decimator based on a comb filter of order $l + 1$ offers a near-optimal response in terms of noise filtering. This means that for a first-order modulator, it is desirable to use a second-order

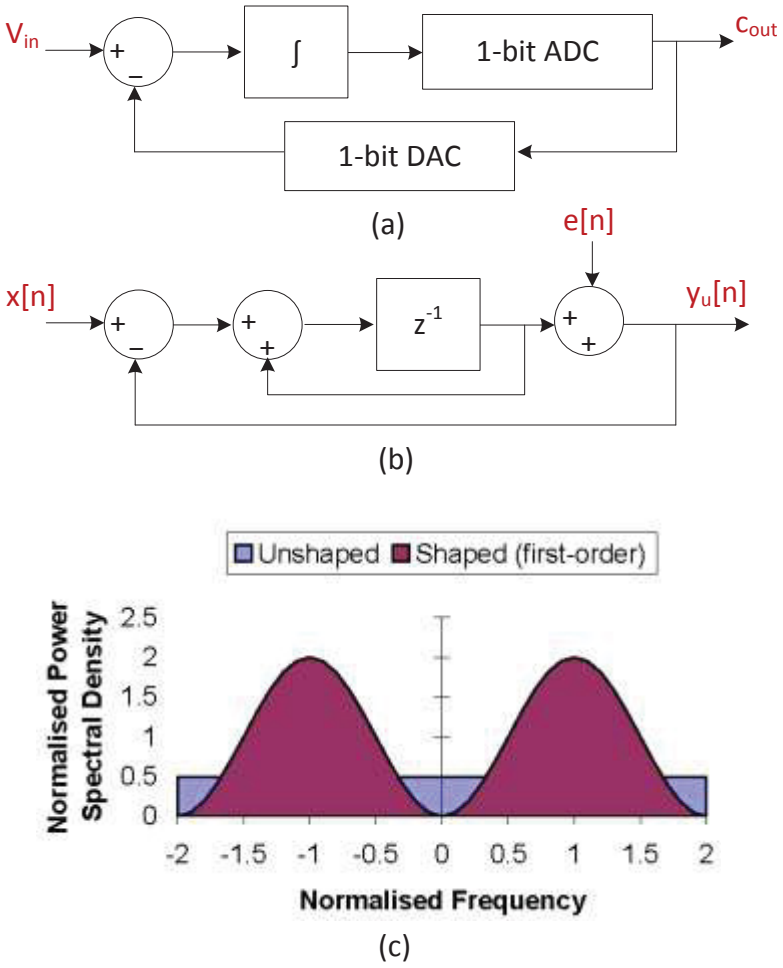


Figure 1.5: First-order $\Delta\Sigma$ modulator. (a) Block diagram and (b) linear discrete-time model of a first-order $\Delta\Sigma$ modulator. (c) Noise power spectrum of first-order $\Delta\Sigma$ modulator, taken from Joseph [23].

comb filter, having a triangular impulse response.

After oversampling and noise shaping, the quantization noise power after decimation, using an ideal low-pass filter, would be

$$\sigma_q^2 = \frac{\Delta^2 \pi^2}{36 M^3}. \tag{1.3}$$

So, the quantization noise is reduced by $9\,\mathrm{dB}$, equivalent to 1.5 extra bits of resolution, with every doubling of the OSR [20].

It is because of these and other properties that the $\Delta\Sigma$ ADC architecture is preferred over the predictive oversampling one, and, in general, over Nyquist-rate architectures. In particular, temporal noise filtering is possible without using a sharp low-pass analog filter at the input of

the ADC [20]. Also, $\Delta\Sigma$ ADCs have flexibility to trade effective number of bits with OSR using the same ADC implementation. OSR is varied either by changing the Nyquist sampling rate or the oversampling rate, or by changing both. In addition, $\Delta\Sigma$ ADCs are more robust to analog imperfections [24].

The above discussion concerns the features of $\Delta\Sigma$ ADCs in general. Let us now consider their use for DPS arrays in particular. The primary motivation has been either to increase the DR or the PSNDR of image sensors [2]. Indeed, Skorka and Joseph [25] have shown that most image sensor architectures are unable to achieve a wide DR and high PSNDR simultaneously at video rates, although such specifications are valuable. DR indicates the range from the brightest to the darkest light level that the imaging system can capture, in one frame, with SNDR greater than $0\,\mathrm{dB}$. PSNDR, which considers both temporal noise and residual FPN, is a measure of image quality.

Table 1.2 summarized DPS approaches. Except the last one, all of the $\Delta\Sigma$ solutions listed in the table realize only modulation at pixel level. Decimation was performed off-chip. The last CMOS DPS listed was demonstrated by the University of Alberta's Electronic Imaging Lab [18, 2]. This $\Delta\Sigma$ DPS achieved high values for both DR and PSNDR. It presents a true $\Delta\Sigma$ ADC, *i.e.*, where the decimator is included at pixel level. This was possible by, besides optimizing the number of transistors in the modulator, designing a low-area serial decimator. By including the decimator at pixel level high output data rate, as opposed to the other $\Delta\Sigma$ DPS approaches explored, is no longer a problem.

This image sensor, based on a $\Delta\Sigma$ ADC, is illustrated in Fig. 1.6. Each DPS, of the DPS array includes: a logarithmic APS, with a diode-connected transistor working in the sub-threshold region; a modulator, whose output is a bit stream that represents a sampled analog signal at its input; a decimator, whose output represents the bit stream coming from the modulator but with a lower rate; and a readout circuit, whose function is to allow the output of the $\Delta\Sigma$ ADC to be available at the output bus of the DPS.

Depending on the behavior of the signal generated by the photocurrent, the sensor circuit can be either linear or logarithmic. Though linear sensors easily present high PSNDR, their DR is limited by technology parameters such as voltage supply and transistor noise. Also, they need to be reset at the end of every sampling interval. Logarithmic sensors, on the other hand, achieve wide DR easily by compressing a large range of light intensity into a small voltage range. However, their PSNDR is limited due to the lack of temporal noise filtering via integration. By using a logarithmic sensor with a $\Delta\Sigma$ ADC, Mahmoodi *et al.* achieve both wide DR and high PSNDR [2].

Though including the decimator at pixel level increases the area usage, the obtained pixel size is comparable to other solutions that perform decimation off-chip, as shown in Table 1.2.

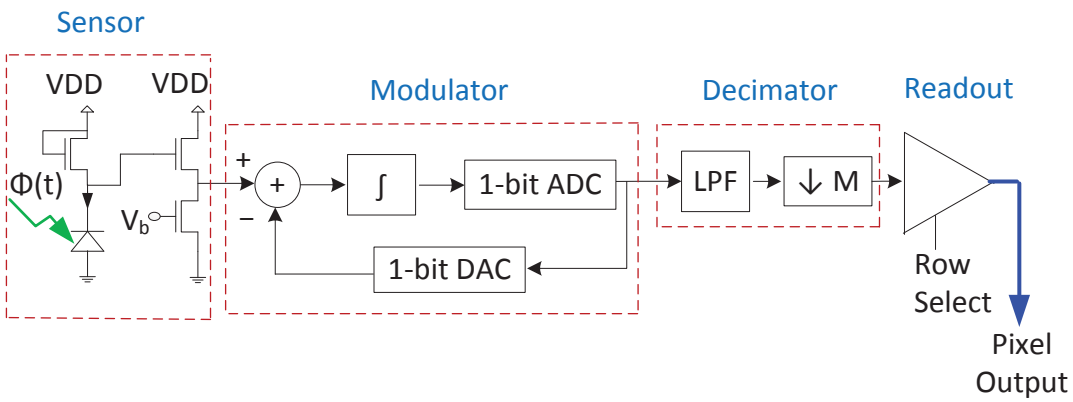


Figure 1.6: $\Delta\Sigma$ DPS for visible band applications. It is composed of a logarithmic APS, a $\Delta\Sigma$ ADC, and a readout circuit.

Therefore, compared to other $\Delta\Sigma$ DPS approaches proposed, the approach introduced by Mahmoodi *et al.* offers the advantages of in-pixel decimation while not critically worsening the pixel area, which makes it promising.

1.1.3 $\Delta\Sigma$ DPS Limitations

As explained in Section 1.1.2, the $\Delta\Sigma$ DPS invented by Mahmoodi and Joseph [26] is a promising approach. However, considering that its intended application was optical imaging, it presents some limitations. Keeping these limitations in mind can lead to a discussion about other applications in the electromagnetic spectrum where this $\Delta\Sigma$ DPS can be applied.

Work done on DPS designs for optical applications that include a classical ADC, such as a $\Delta\Sigma$ ADC, at pixel level has focused on keeping the number of transistors per pixel to the minimum necessary. This is done because, seeing it in a simplified way, a higher number of transistors can be related to a higher pixel pitch. Fig. 1.7 shows the variation of typical pitch for image sensors along the section of the electromagnetic spectrum used for imaging. As can be seen, optical imaging presents the smallest typical pixel pitch.

It could seem that the smaller we make the pitch of the image sensor, the better. However, pitch specifications are often determined by the wavelengths of interest. Whether photons in a certain spectral band can be focused, and the type of photodetectors available, are factors that affect how small the pitch can be. For optical applications, pixel pitch could vary from 1 to 8 μm, as shown in Table 1.3. So, it is expected that an image sensor for optical applications satisfies this, among other performance-related requirements.

Though the $\Delta\Sigma$ DPS array presented by Mahmoodi *et al.* [2] has several advantages over other approaches, it exhibits mainly three limitations, which are large area, low fill-factor, and high dark limit. Large area is the main disadvantage of the $\Delta\Sigma$ DPS approach, and certainly is

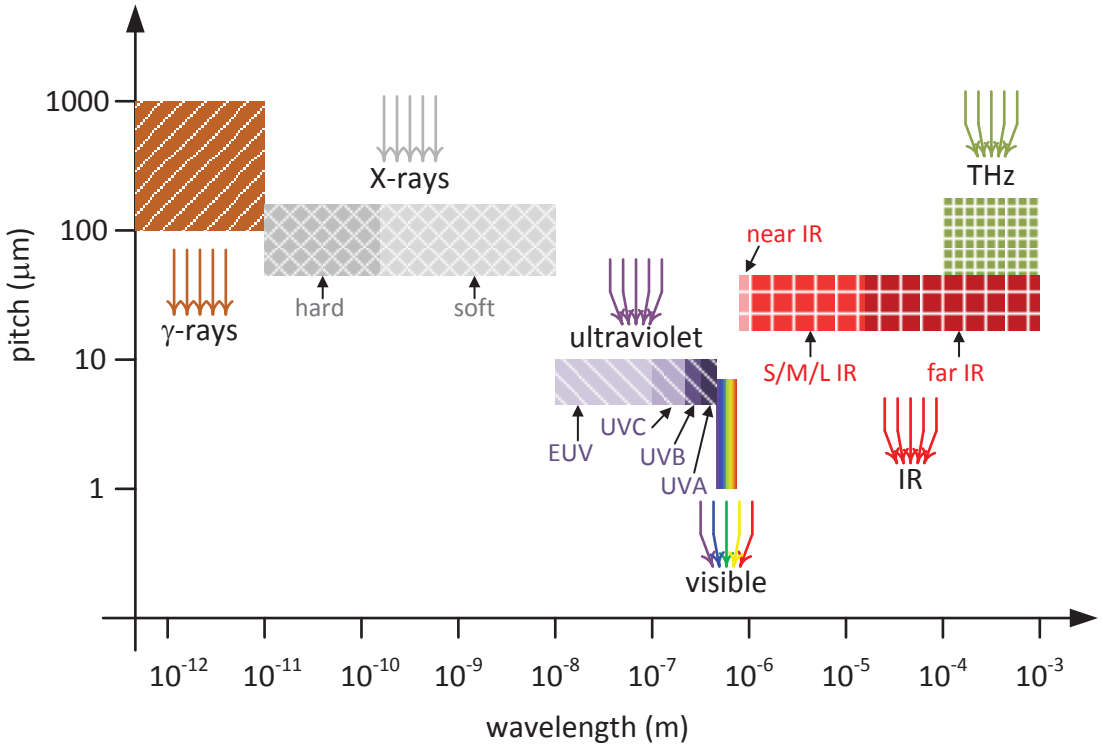


Figure 1.7: Typical pixel pitch in different imaging bands. Depending on the image band of interest, different area restrictions apply. Taken from Skorka *et al.* [3].

the reason why, despite its many advantages, other in-pixel ADC architectures are being considered. However, using the pixel size information from Table 1.2, it is evident that achieving an acceptable pixel size for optical imaging is not only an issue for Mahmoodi and Joseph's approach, but for most of the works listed, including for approaches using only a $\Delta\Sigma$ modulator in the pixel.

Fill factor can be defined as the ratio of the light-*sensitive* area of a pixel to its total area. The light-*insensitive* area of a pixel corresponds, in this case, to the part that is occupied by devices other than the photodiode, such as by transistors, capacitors, etc. In general, with a current-based photodetector, all devices involved in the photocurrent-to-digital conversion of the DPS take away from the fill factor. The low fill-factor reported by Mahmoodi *et al.* [2], *i.e.*, $2.3\,\%$, is due to the great number of devices included within the planar pixel architecture and that share pixel area with the photodiode.

The dark limit, expressed in $\mathrm{cd/m^2}$, can be defined as the lowest luminance level at which the SNDR, which depends on temporal noise and residual FPN, exceeds $0\,\mathrm{dB}$, *i.e.*, where signal and noise powers are equal [25]. It is affected by physical characteristics of the photodiode and can be improved by increasing the fill factor. Nevertheless, the reported dark limit was $0.28\,\mathrm{cd/m^2}$, which is comparable to reported values of other image sensors, as pointed out by

Table 1.3: Pitch characteristics in different imaging bands. Pitch is determined mainly by a set of characteristics such as focusing ability, and type of detector. Taken from Skorka and Joseph [3].

Band	Wavelength	Focus	Pitch (μm)	Detectors
γ-ray	< 0.01 nm	No	$100 - 1000$	Indirect: Scintillator and c-Si devices Direct: CdZnTe devices
X-ray	$0.01 - 10$ nm	No	$48 - 160$	Indirect: Scintillator and c-Si devices Direct: a-Si:H, CdZnTe, or a-Se devices
UV	$10 - 400$ nm	Yes	$5 - 10$	c-Si devices
Visible	$400 - 700$ nm	Yes	$1 - 8$	c-Si devices
Near IR	$0.7 - 1$ μm	Yes	$17 - 47$	c-Si devices
IR	$1 - 1000$ μm	Yes	$17 - 52$	Microbolometers or HgCdTe devices
THz	$100 - 1000$ μm	Yes	$50 - 180$	Microbolometers or c-Si antennas

a survey that includes 26 image sensor designs [2].

From Fig. 1.7 we can see that, although the pixel pitch of Mahmoodi and Joseph's $\Delta\Sigma$ DPS needs to be improved for optical (visible spectrum) imaging, it is within the expected range for some bands in the invisible spectrum, which is comprised of γ-ray, X-ray, UV, IR, and THz bands. Thus, provided the current architecture could be adapted to meet the requirements of these other bands, it could prove viable for an invisible-band application.

Due to a similar restriction on pixel size as in the visible band, the current $\Delta\Sigma$ DPS design appears unsuitable for UV imaging. On the other hand, γ-ray, X-ray, IR, and THz bands allow greater pixel pitch. IR and THz imaging involve the use of microbolometers or HgCdTe devices, for the IR imaging case, and c-Si antennas, for the THz case, as detectors. With microbolometers, there are specific assembly requirements due to their structure. With HgCdTe devices, cooling is needed for correct operation. For these and other reasons, we did not choose to adapt the $\Delta\Sigma$ DPS architecture to these bands.

In the case of γ-rays and X-rays, both allow the use of regular c-Si devices as detectors in the indirect approach, and both have relaxed pixel size requirements. Consequently, they enable a design flow that is performance rather than size driven. However, both applications are pulse-based rather than flux-based high-energy applications. Photons low in number but high in energy are converted by a scintillator to photons high in number but low in energy, *i.e.*, a short pulse of optical light. To properly detect this pulse, a high time resolution, or frame rate, is needed. In contrast, a regular visible-band application involves a relatively continuous flux of optical light due to continuous illumintion sources, such as the sun or artificial lighting.

Therefore, γ-ray and X-ray imaging have different speed requirements compared to optical

imaging. While optical imaging requires a minimum video rate of $30\,\mathrm{fps}$, according to the National Television System Committee (NTSC), this rate is not appropriate for the pulse-based applications. In particular, the frame rate for gamma imaging is related to the decay time of the scintillator used, which is the time it takes for the emission to decrease by a factor of e. Frame rates could be on the order of MHz [27].

The faster rates required by pulse-based applications need to be addressed without affecting the image sensor performance negatively. In order to allow faster rates, the OSR needs to be decreased, but this alone could decrease the SNR of the $\Delta\Sigma$ ADC and, consequently, the image quality of the imaging system. This is the main issue that needs to be addressed for the $\Delta\Sigma$ DPS technology to be viable for γ-ray or X-ray imaging.

In conclusion, besides the high DR and high SNDR requirements of optical imaging, small-area $\Delta\Sigma$ DPS designs are desirable for visible-band applications. Besides the particular requirements that a particular application in the invisible band may have, fast-rate $\Delta\Sigma$ DPS designs are generally desirable for γ-ray and X-ray applications.

1.2 Methodology

Work done by Mahmoodi and Joseph demonstrated a $\Delta\Sigma$ DPS that is competitive with the human eye in terms of DR and PSNDR. The main objective of this thesis is to overcome the problems that keep this technology from being commercially competitive. In order to do so, a methodology is presented here. This methodology uses targeted baselines, based on commercial image sensors for optical and gamma imaging, to define specifications and assess competitiveness. If the assessment reveals that the designs developed in this thesis do not meet the baselines, a plan is developed to do so.

To meet said targeted baselines, for applications where pixel area is the limiting factor, such as optical imaging, the dual trend of the semiconductor industry, *i.e.*, the "More Moore" and "More than Moore" trends, is investigated. For applications, such as gamma imaging, where frame rate is the limiting factor, higher-order $\Delta\Sigma$ ADC architectures are investigated. For both cases, this section discusses the trade-offs and challenges that may arise when applying the proposed approaches.

1.2.1 Targeted Baselines

Image sensors have been developed for a diversity of bands found in the electromagnetic spectrum. Optical imaging, which concerns wavelengths between 400 and $700\,\mathrm{nm}$, has been widely explored for consumer electronics, such as digital still and video cameras. Gamma imaging,

which concerns wavelengths below $0.01\,\mathrm{nm}$ is being explored for medical applications such as lymphoscintigraphy.

For optical imaging, as mentioned earlier in this chapter, several DPS architectures have been developed, as shown in Table 1.2. They focus on improving different properties of the image sensor, and one of them has proved to be competitive to the point of being commercialized. This is the case of Pixim's DPS, an architecture that uses a multichannel bit-serial (MCBS) ADC per colour pixel, which is a two-by-two subarray of pixels, each having a pitch of $7\,\mu\mathrm{m}$. Sharing an ADC between multiple pixels is part of the competitive advantage of Pixim's design. Using reported values for area and fill factor [16], Pixim's pixel pitch without ADC-sharing would be approximately $11\,\mu\mathrm{m}$.

Pixim's pixel circuit is shown in Fig. 1.8. In this design, each photodiode of the four belonging to one colour pixel is connected to a transistor to ensure non-destructive readout, another transistor for resetting the photodiode to the current value of an external ramp voltage, and further transistors for multiplexing the photodiode outputs to the shared MCBS ADC. Because the external ramp needs to be compared n times, n being the resolution of the ADC, in a single frame, speed is a major drawback of this architecture.

This architecture presents a wide dynamic range, which is greater than $100\,\mathrm{dB}$, and a high PSNR, which is greater than $45\,\mathrm{dB}$, while keeping the pixel size within a competitive range for the application. Pixim do not report PSNDR. In comparison, Mahmoodi and Joseph's $\Delta\Sigma$ DPS reported values for DR and PSNR of over $110\,\mathrm{dB}$ and $46\,\mathrm{dB}$, respectively, which is already competitive with Pixim's architecture in terms of performance. However, an approach to reduce area needs to be developed for the $\Delta\Sigma$ DPS to be also competitive in terms of pixel size.

For gamma imaging, although several ways to implement an image sensor for this application have been reported [28, 29], the design adopted by Cubresa, presented by Goertzen *et al.* [27], is considered in this thesis as the baseline. This is because the Electronic Imaging Lab at the University of Alberta was engaged by Phantom Motion, Cubresa's partner, to investigate improvements to the Cubresa technology.

Currently, gamma cameras have an analog head, an external ADC module, and another external processing module. The analog head includes a collimator, a scintillator, and a small array of silicon photomultiplier (SiPM) detectors, built from avalanche photodiodes, which together convert gamma rays into analog signals, one at each SiPM output. Although they provide high signal gain, compared to standard photodiodes, SiPMs require higher voltages (*i.e.*, $30\,\mathrm{V}$) than what is possible with mainstream, and cost-efficient, CMOS technology. The external ADC module is an array of off-the-shelf ADCs, which have standard CMOS voltage requirements [30].

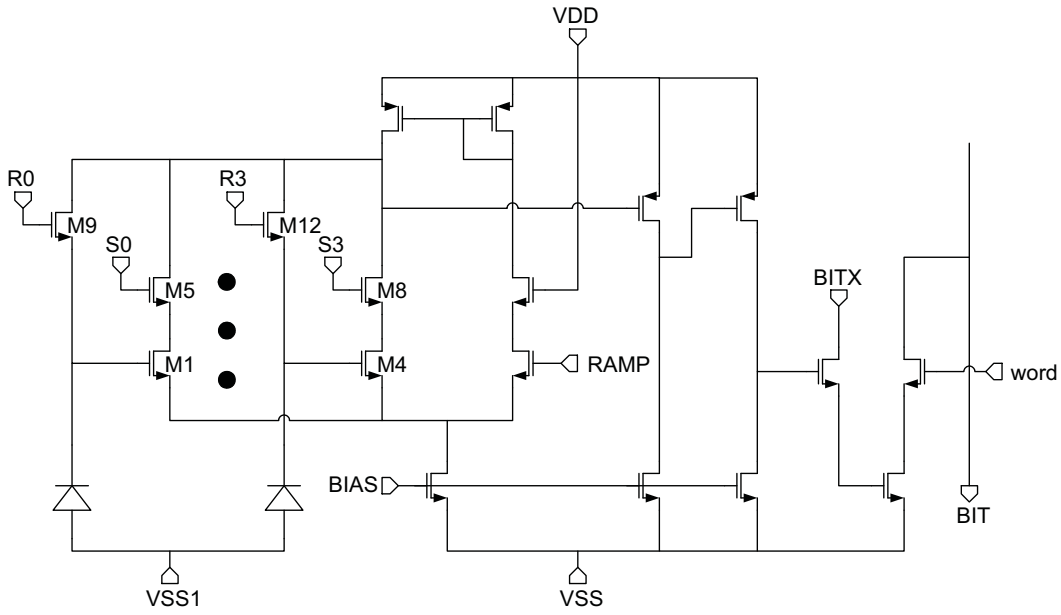


Figure 1.8: Circuit diagram of Pixim's pixel design. One MCBS ADC is shared among four pixels to form a colour pixel. Taken from Bidermann *et al.* [16].

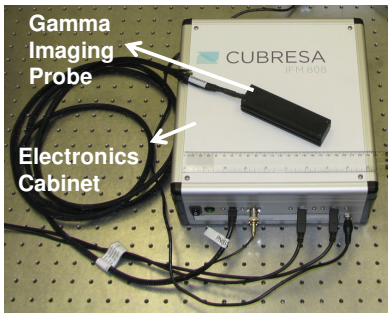


Figure 1.9: Diagram of a gamma imaging system. It is composed of a hand-held probe containing a SiPM detector, CsI:Tl scintillator, collimator; and a data acquisition system.

Whereas current gamma cameras offer high detection efficiency, which is the probability of detecting a gamma event, Phantom Motion and Cubresa were seeking a more compact system design. University of Alberta expertise was engaged for the purpose of integrating photodetection and data conversion at pixel level. Therefore, alternatives to make the detector and ADC arrays compatible, in terms of manufacturability, need to be found without affecting the camera's performance.

Current gamma sensors present incompatible voltage sources between the photon capture (high voltage) and digital conversion (low voltage) stages. In order to obtain an integrated image sensor, compatible voltage sources on one chip need to be used. One possibility is to employ a non-standard CMOS process that supports higher voltages and to integrate SiPMs at

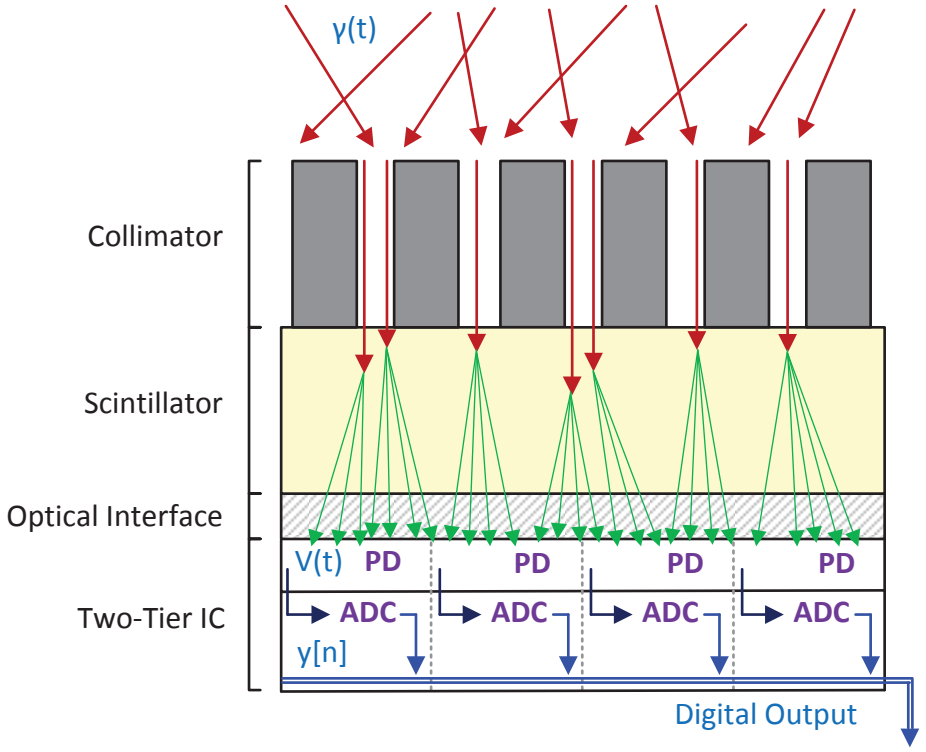


Figure 1.10: Diagram of the proposed gamma imaging system. Through multiple stages, gamma rays, $\gamma(t)$, are transformed into photon flux, $\Phi(t)$, then into voltages, $V(t)$, and finally into digital signals, $y[n]$. The latter two stages are the focus of this work.

chip level.

Alternatively, to ease manufacturability, the photodetection should be done with standard CMOS photodetectors, *i.e.*, photodiodes. Because photodiodes have lower signal than SiPMs, circuits that significantly reduce noise need to be included to maintain SNR, which is a good justification for using a $\Delta\Sigma$ DPS, provided it could meet the speed requirements of the application. The idea is that, by taking advantage of the noise filtering properties of the $\Delta\Sigma$ ADC, and by performing digital conversion at pixel level instead of in an external module, photodiodes can be used in lieu of SiPMs [30].

Additionally, because a $\Delta\Sigma$ ADC per pixel should to be included while keeping a high fill factor, for better photon capture, a vertically-integrated (3D) structure rather than a planar (1D) one needs to be used. Vertical integration, as defined by Garrou *et al.*, is "a structure composed of two or more layers of active electronic components, integrated both vertically and horizontally" [31].

Fig. 1.10 illustrates the gamma image sensor proposed to meet the integration requirement using vertical integration. Gamma rays, which come from different directions, pass through a collimator that only passes the gamma rays that are parallel to the collimator direction. The

aligned high-energy gamma rays are then transformed into low energy photons via a scintillator. The number of photons that leave the scintillator depend on the quantum efficiency of the scintillator, as well as the input and output wavelengths. In general, a pulse of many optical photons is emitted for each gamma ray that is absorbed, due to energy conservation. After passing through an optical interface, the photons are collected by photodiodes and transformed to an analog electrical signal that is then digitized with a $\Delta\Sigma$ ADC. These last processes are performed by a two-tier integrated circuit (IC) and are the focus of this work.

Summing up, a methodology based on targeted baselines needs to be followed so the $\Delta\Sigma$ DPS can be a competitive technology. To pursue competitiveness in optical imaging, Pixim's pixel size is used as the baseline. In this case, approaches need to be proposed for pixel size reduction. Also, to pursue competitiveness in gamma imaging, Cubresa's image sensor is used as the baseline. In this case, approaches need to be proposed to integrate an image sensor, while maintaining its performance. By following appropriate approaches to meet each targeted baseline, the $\Delta\Sigma$ DPS architecture can be used to design smaller/faster $\Delta\Sigma$ DPS circuits.

1.2.2 More Moore and More than Moore

As discussed in Section 1.2.1, the $\Delta\Sigma$ DPS technology is advantageous and recommended, for optical imaging, provided the area needed to accommodate more transistors can be reduced. Therefore, in this section, approaches are proposed to achieve a competitive pixel size, where there is one $\Delta\Sigma$ ADC per pixel, while maintaining performance advantages.

There is a dual trend roadmap for the semiconductor industry [32], presented in the International Technology Roadmap for Semiconductors (ITRS). The first trend is called "More Moore" and focuses on device miniaturization. This means that as technology scales down and physical feature sizes shrink, following Dennard's scaling theory [33], the overall area of a circuit in a newer technology is expected to decrease. This way, the $\Delta\Sigma$ DPS pixel pitch could be reduced by using newer technology nodes along with process-dependent improvements in the circuit design.

Digital circuits, unlike analog ones, benefit directly from scaling in compliance with Moore's Law. Given that the digital part of the DPS presented by Mahmoodi and Joseph, designed for a $180\,\mathrm{nm}$ CMOS process, represents about 50% of the total pixel area [2], size reduction of this part could lead to overall area reduction. However, following the "More Moore" trend alone may not make the DPS technology competitive for optical applications.

Besides the classic Moore's Law trend in the semiconductor industry, there is a second trend called the "More-than-Moore" trend, related to the combining of circuits with different functions, such as digital circuits and non-digital ones (analog/RF, sensors, etc) on the same

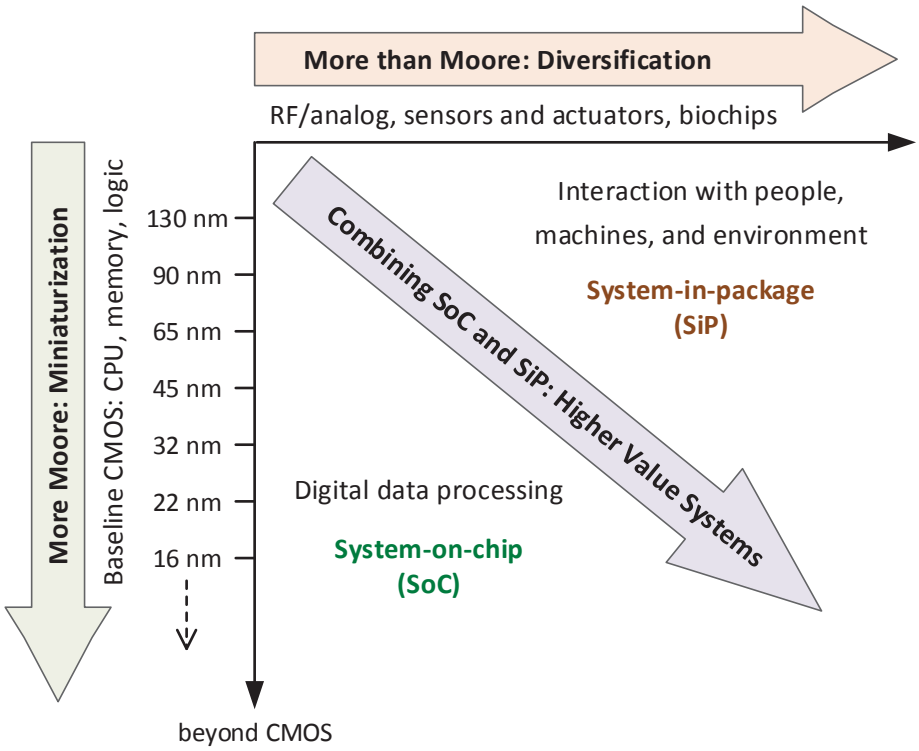


Figure 1.11: Dual trend in the semiconductor industry. The "More Moore" trend refers to miniaturization by using newer processes. The "More than Moore" trend refers to functional diversification through heterogeneous integration. Adapted from the ITRS [32] by Skorka.

integrated circuit by exploiting the functional diversification of semiconductor devices to form a compact system. A graphical representation of this dual trend is shown in Fig. 1.11.

Each pixel of a $\Delta\Sigma$ DPS array is composed of a detector, to convert an optical signal to an electrical one, and analog and digital circuits, for conditioning and pre-processing. Because of the inherent functional diversification of the $\Delta\Sigma$ DPS technology, "More than Moore" techniques can be applied to it. Improvements in performance and further reduction in terms of area could be achieved by applying system-in-package (SiP) fabrication techniques, such as vertical integration. Analog/digital and detector circuits of the image sensor can be fabricated in multiple tiers, so each part of the DPS design is properly placed in a different tier. This way, the detectors can be placed on top of the other circuitry, improving the fill factor and the spatial resolution of the camera, while data conversion and readout can be placed in a different layer.

Also, because photodiode properties do not scale well, vertical integration offers a dual-trend means to combine the benefits of scaling while not degrading performance. Vertical integration also offers a solution to the low dark limit (DL) problem by having a photodiode design dedicated to improve DL behavior while the other tiers scale accordingly.

Therefore, the "More Moore" and "More than Moore" approaches can be used together to exploit the advantages of in-pixel $\Delta\Sigma$ ADCs while counteracting their disadvantages. With the "More Moore" trend, however, careful sizing of the transistors that are part of the circuit needs to be done. Two-dimensional scaling works in a straightforward way when it comes to digital circuits, such as memory and logic circuits, which can be sized to minimum channel-length values, and whose performance, measured in terms of delay and frequency, benefits from the miniaturization process.

Non-digital circuits, such as analog/RF and power supply circuits, on the other hand, do not necessarily scale at the same rate as the digital ones, in terms of area and power, and represent a challenge due to the fact that performance parameters, measured in terms of noise, mismatch, leakage current, etc, do not necessarily improve for newer technologies [4]. Since many microelectronic systems, including DPS arrays, are composed of digital and non-digital circuits, efforts for decreasing the area, while not degrading the performance, do not only rely on the process technology alone but also on the design techniques applied in said technology.

An area-conscious architecture is the first step to achieve a small area. It is for this reason that a first-order $\Delta\Sigma$ ADC is preferable over higher-order implementations for optical imaging. However, the first-order $\Delta\Sigma$ ADC needs a greater oversampling ratio to achieve the same bit resolution, so it may be expected that the circuit consumes too much power because power consumption increases with switching frequency. Fortunately, Mahmoodi [18] has shown that the power consumption of this architecture, with good design, is comparable to other architectures. Thus, with scaling, Mahmoodi *et al.*'s design flow needs to be adapted to enjoy the power savings expected from lower supply voltages. Lower power consumption is always desirable as it makes the DPS technology more scalable, *i.e.*, the lower the power per pixel, for a given power budget, the greater the number of pixels that could be included.

The approach followed for reducing pixel size, so it is competitive with the targeted baseline for optical imaging, is process scaling. To see the roadmap of the $\Delta\Sigma$ DPS technology in terms of pixel pitch, the pixel is designed for three different technology nodes: 180, 130, and $65\,\mathrm{nm}$. Also, considerations for the application of vertical integration, by using a 3D IC process, such as the $130\,\mathrm{nm}$ Tezzaron process, are made. It is important to point out that applying the dual trend to the $\Delta\Sigma$ DPS technology could lead to pixel size reduction provided the pixel circuit is designed area-consciously. Finally, exploiting "More Moore" and "More than Moore" would give us an idea of what is needed to make the $\Delta\Sigma$ DPS more competitive.

1.2.3 Higher-Order Architecture

As discussed in Section 1.1.3, the pixel area restriction for gamma imaging is much more relaxed. Therefore, for such an application, device miniaturization is not a useful tool for pixel design improvement. On the other hand, as explained in Section 1.2.1, integration between photon capture and digital conversion as well as faster rate are the most important requirements that need to be satisfied. Therefore, in this section, a method to design an integrated gamma image sensor that includes a $\Delta\Sigma$ ADC per pixel, as shown in Fig. 1.10, that is capable of meeting the gamma speed requirements is proposed.

To meet the speed requirement of the pulse-based application, the rate at which the optical signal is converted to a digital signal needs to increase, which means the speed of the DPS architecture needs to increase. The DPS architecture adopted for optical applications uses a first-order $\Delta\Sigma$ ADC. DPS designs using higher-order $\Delta\Sigma$ ADCs can be also explored due to the lack of pixel area restrictions in gamma imaging. A second-order $\Delta\Sigma$ ADC, which is similar to the first-order one, is shown in Fig. 1.12(a). To justify the interest in higher-order $\Delta\Sigma$ architectures, we can analyze the ADC output of such architectures from a noise versus OSR perspective.

Similar to the noise shaping analysis for a first-order $\Delta\Sigma$ modulator in Section 1.1.2, we can obtain an expression for the second-order one. The z-transform of the output, $Y_u(z)$, produced by a second-order $\Delta\Sigma$ modulator can be expressed as

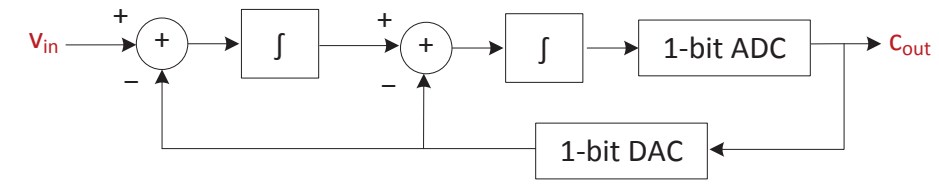
$$Y_u(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z), \tag{1.4}$$

where $e[n]$, in Fig. 1.12(b), is the quantization noise and $E(z)$ its z-transform. From (1.4), again we can see that the modulator simply delays the input signal while acting as a high-pass filter for the quantization noise. Furthermore, compared to the first-order modulator, having only one integrator and feedback differencer, a more efficient noise shaping is obtained by using two instead, as can be seen in Fig. 1.12(c). This way, the noise depends on the previous two error samples instead of just the previous one.

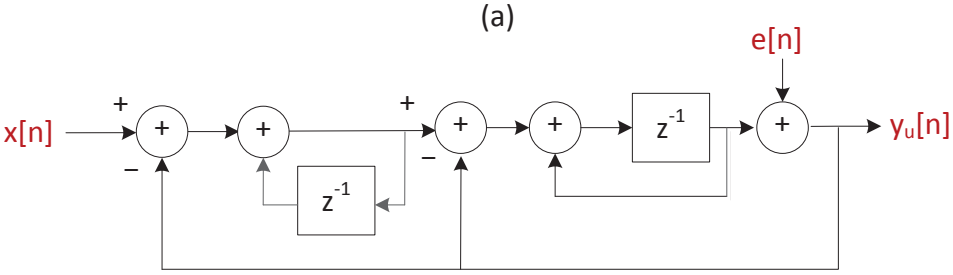
For the second-order modulator, the quantization noise power after decimation using an ideal low-pass filter can be expressed as

$$\sigma_q^2 = \frac{\Delta^2 \pi^4}{60 M^5}. \tag{1.5}$$

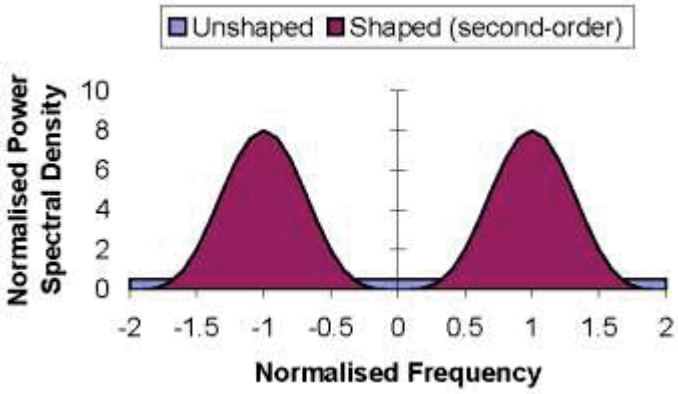
So, the quantization noise is reduced by $15\,\mathrm{dB}$, equivalent to 2.5 extra bits of resolution, with every doubling of the OSR [20]. In general, for an L-order $\Delta\Sigma$ ADC, the output of the modu-



(a)



(b)



(c)

Figure 1.12: Second-order $\Delta\Sigma$ modulator. (a) Block diagram and (b) linear discrete-time model of a second-order $\Delta\Sigma$ modulator, based on Norsworthy *et al.* [20]. (c) Noise power spectrum of the second-order $\Delta\Sigma$ modulator, taken from Joseph [23].

lator can be expressed as

$$Y_u(z) = z^{-1}X(z) + (1 - z^{-1})^L E(z), \tag{1.6}$$

and the quantization noise power can be expressed as

$$\sigma_q^2 = \frac{\Delta^2 \pi^{2L}}{(2L+1)M^{(2L+1)}}. \tag{1.7}$$

In general, the quantization noise is reduced by $6L + 3\,\mathrm{dB}$, equivalent to $L + 0.5$ extra bits of resolution, with every doubling of the OSR [34].

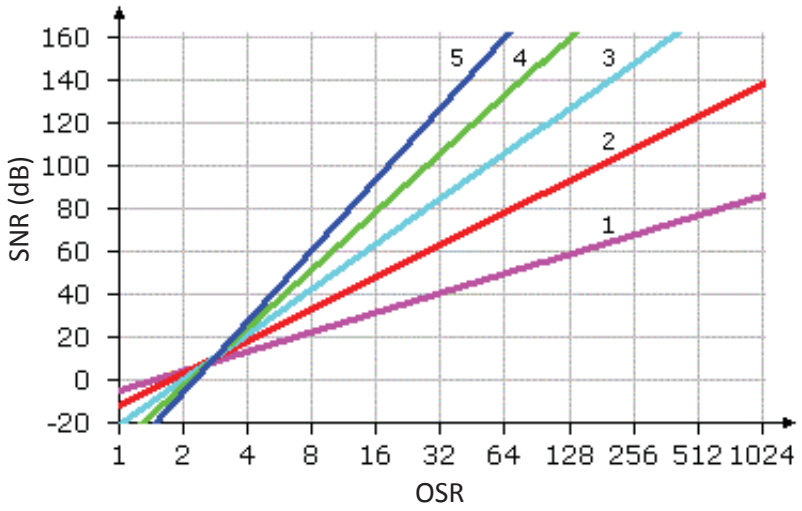


Figure 1.13: Impact of modulator order on SNR. The SNR versus OSR for different modulator orders assuming ideal decimation, taken from Beis [35], shows that, for the same target SNR, the higher the order of the modulator, the lower the needed OSR to achieve it.

Comparing the quantization noise powers obtained for the first and second-order $\Delta\Sigma$ modulators, as indicated in (1.3) and (1.5) respectively, it is plain to see that for a fixed OSR, we have less quantization noise with a second-order modulator than with a first-order one. The same is true for a third-order modulator and so on. However, higher-order modulators can suffer from stability issues [20] and present more complexity. So a second-order $\Delta\Sigma$ modulator, provided it meets noise and speed requirements, is preferred.

From the speed point of view, with the assistance of Fig. 1.13 we can see that, for instance, for a target SNR of $60\,\mathrm{dB}$ for the ADC, *i.e.*, for an effective number of bits (ENOB) of 10 bits, using a first-order $\Delta\Sigma$ modulator, an OSR of 200 would be needed. Considering that the frame rate for gamma ray imaging is $1\,\mathrm{MHz}$ [27], the oversampling period would be $5\,\mathrm{ns}$, which would require a modulator with very fast response. If we consider the same target SNR value, but choose a second-order modulator instead, the needed OSR would be 50 which would require an oversampling period of $20\,\mathrm{ns}$, which is more feasible than the one needed in the first case.

1.3 Scope

Logarithmic DPS arrays present better noise behavior than logarithmic APS arrays by realizing in-pixel analog-to-digital conversion. The analog-to-digital conversion can be done by using (non-classical) imaging-specific or (classical) conventional ADCs. $\Delta\Sigma$ ADCs offer several advantages over other architectures such as temporal noise filtering without using a sharp low-

pass analog filter at the input of the ADC, flexibility to trade bit resolution (SNR) with frame rate, and being more robust to analog imperfections. The $\Delta\Sigma$ DPS architecture is adopted in this thesis due to its wide DR and high PSNDR capability.

Although the $\Delta\Sigma$ DPS, based on a first-order $\Delta\Sigma$ ADC, introduced by Mahmoodi and Joseph [18, 2] serves to prove the feasibility of this technology and its promising advantages, it is not yet ready for commercialization due to either its pixel size or frame rate. To overcome its limitations, a methodology based on targeted baselines is proposed to establish specifications and assess the competitiveness of the $\Delta\Sigma$ DPS technology for small-area DPS designs and fast-rate image sensors.

Smaller $\Delta\Sigma$ DPS designs, meant for optical imaging, are realized having Pixim's commercial DPS as the targeted baseline for performance. Toward this end, process scaling is explored taking into account the challenges inherent to technology nodes that may arise, such as effects on the performance of analog circuits. $\Delta\Sigma$ DPS designs are made in 180, 130, and $65\,\mathrm{nm}$ fabrication processes. The $180\,\mathrm{nm}$ design presents design improvements to Mahmoodi and Joseph's $180\,\mathrm{nm}$ design. The $130\,\mathrm{nm}$ design is selected as it is the next technology node and also having in mind that $3\mathrm{D}$ IC integration in the same node would be desirable and possible in the future. The $65\,\mathrm{nm}$ design is selected to push the fabrication node towards nanoscale technologies and experience the problems that arise as the feature size further reduces.

Also, a faster $\Delta\Sigma$ DPS, meant for gamma imaging, is designed having Cubresa's gamma image sensor as the targeted baseline for performance. Gamma imaging requires high frame rates, where area usage is not an issue. For this application, a second-order, rather than a first-order, modulator is explored. Furthermore, the $\Delta\Sigma$ DPS is used as part of a complete image sensor and is designed for a two-tier $130\,\mathrm{nm}$ process, *i.e.*, a $3\mathrm{D}$ IC process. This fabrication process was selected to provide a fully integrated gamma imaging system. Also by using $3\mathrm{D}$ IC integration, fill factor specifications could be essentially satisfied.

The rest of this thesis is organized as follows. Chapter 2 shows a first-order $\Delta\Sigma$ DPS, designed in three different technology nodes, intended for optical imaging. Area trends for the $\Delta\Sigma$ DPS are shown to establish a path to competitiveness of this architecture for the consumer electronics market. Chapter 3 shows a complete image sensor based on an array of second-order $\Delta\Sigma$ DPSs, intended for gamma imaging. This design serves to study the feasibility of developing a fully-integrated gamma image sensor. In Chapter 4, the main contributions are presented. Also the optical and gamma imaging designs are assessed to determine their technology readiness levels (TRLs). Finally, a maturation plan is proposed based on this assessment.

Chapter 2

Smaller Area Designs

Pixel-level analog-to-digital converters (ADCs) counteract one of the main disadvantages of nonlinear complementary metal-oxide-semiconductor (CMOS) image sensors, *i.e.*, their low signal-to-noise-and-distortion ratio (SNDR) relative to linear CMOS image sensors. In particular, the oversampling, noise-shaping, and anti-aliasing properties of the delta-sigma ($\Delta\Sigma$) ADC makes it a great choice for pixel-level data conversion.

Using a logarithmic sensor with an in-pixel $\Delta\Sigma$ ADC, as demonstrated by Mahmoodi *et al.* [2], enables a competitive peak SNDR (PSNDR), compared to conventional linear active pixel sensor (APS) designs, while easily achieving wide dynamic range (DR) at video rates. However, the main disadvantage of this nonlinear digital pixel sensor (DPS) design is the pixel area, which is too large for optical applications, its original target.

Fortunately, the dual trend in the semiconductor industry, *i.e.*, scaling and functional diversification combined, promises to help mitigate the pixel size problem of Mahmoodi *et al.*'s architecture. By using newer technology nodes, the pixel size may eventually be small enough to be competitive with commercial DPS-based image sensors for optical imaging. Furthermore, by exploring vertical integration, the area reduction could be accelerated, while improving other specifications, such as fill factor and dark limit (DL). Vertical integration involves the stacking of integrated circuit (IC) tiers differentiated by functionality.

To these ends, novel designs of a $\Delta\Sigma$ DPS are presented in this chapter. The same fundamental circuit is designed for three different processes, at the 180, 130, and $65\,\mathrm{nm}$ technology nodes, in each case applying 3D IC principles. All three designs, including the $180\,\mathrm{nm}$ one, involve schematic and layout modifications of Mahmoodi's original $180\,\mathrm{nm}$ design [18] to improve its operation and reduce area.

Technology scaling considerations have to be taken into account in order to successfully design the $\Delta\Sigma$ DPS for the three nodes mentioned. Before doing so, however, we first summarize the requirements imposed by the application, *i.e.*, optical imaging. This is necessary

because the way the circuit is designed strongly depends on its requirements, which are given in Table 2.1. Of these requirements, the most important change, compared to previous work, concerns pixel pitch.

The DR reported by Mahmoodi and Joseph is over $110\,\mathrm{dB}$ [1], while Pixim's reported value is over $100\,\mathrm{dB}$ [16]. Moreover, the human eye's DR covers $126\,\mathrm{dB}$ [25]. With that in mind, by choosing a DR of $126\,\mathrm{dB}$, the designs in this work are set to outperform Pixim's commercial DPS.

The PSNDR reported by Mahmoodi and Joseph is $45\,\mathrm{dB}$ [1], while Pixim reports a signal-to-noise ratio (SNR) of over $45\,\mathrm{dB}$ [16], although it is not clear whether Pixim's reported value accounts for distortion. Moreover, the human eye has a PSNDR of $36\,\mathrm{dB}$ [25]. Both approaches, *i.e.*, the $\Delta\Sigma$ DPS and the multichannel bit-serial (MCBS), appear to surpass this value. In this work, a PSNDR of $36\,\mathrm{dB}$ is specified.

Also, the minimum frame rate specified for video is $30\,\mathrm{Hz}$, according to the National Television System Committee (NTSC). Therefore, this is the value that is used in this thesis for the three $\Delta\Sigma$ DPS designs.

The pixel pitch is based on Pixim's DPS design [16], which is considered the baseline pitch for optical applications in this thesis. Pixim's pixel pitch , assuming one ADC per pixel and excluding photodiodes, is calculated to be $11\,\mu\mathrm{m}$, so the objective is to obtain a pixel pitch of comparable magnitude, also assuming one ADC per pixel and excluding photodiodes, which would be placed in a separate tier.

Subsequent sections, in this chapter, provide an overview of the circuit considerations related to technology scaling and give details about the circuit design of every block comprising the DPS. These details include circuit selection criteria, schematic diagrams, and floorplanning considerations for physical design. Also, simulation and layout results obtained for all three DPS designs are presented, providing functional verification, performance evaluation, and area measures. Finally, area projections for the $\Delta\Sigma$ DPS technology, obtained from these results, are presented.

Table 2.1: Specifications of a DPS for optical imaging. These values are comparable to the specifications reported in the literature for the competing design and standard television.

Parameter	Value
DR (dB)	126
PSNDR (dB)	36
Frame Rate (Hz)	30
Pixel pitch ($\mu\mathrm{m}$)	11

2.1 Technology Scaling

As mentioned earlier, in order to reduce the pitch of $\Delta\Sigma$ pixels for optical imaging, the dual trend in the semiconductor industry, *i.e.*, the More Moore and More than Moore trends combined, is applied. This means that scaling, by using three different nodes, and considerations for vertical integration, by assuming a 3D IC process, are exploited.

Previous work related to the scaling of analog and mixed-signal circuits [4, 36, 37, 38] have shown the problems to overcome when going from one process to another. These works also predict further complications specific to nanoscale processes, *i.e.*, the $65\,\mathrm{nm}$ node and below. As transistor dimensions shrink, supply voltage and gate-oxide thickness also decrease, so transistor parameters are expected to change as well. Also, the pitch of metal interconnections and options for metallization and capacitors vary from one technology to another. In this section, the most important considerations when scaling down, in general, any design, from 180 to 130 and $65\,\mathrm{nm}$, and, in particular, a DPS that includes a $\Delta\Sigma$ ADC, are described.

2.1.1 Supply Voltages

As dimensions shrink from one technology to a newer one, voltage supply and gate-oxide thickness must also decrease according to Dennard's scaling theory [33]. In the nanoscale regime, a reduction of the supply voltage increases leakage current due to thermal diffusion of electrons, while a reduction of the gate-oxide thickness shifts down the threshold voltage, increasing gate leakage due to tunneling [39]. An increment in leakage currents results in an increment in static power, which was considered negligible, in older technologies, compared to dynamic power. However, both are becoming comparable for nanoscale technologies, possibly increasing the total power consumption. This goes against one of the semiconductor industry's drive for scaling down transistor sizes, which is to produce smaller and more efficient circuits.

From another point of view, the performance of an analog (or mixed-signal) circuit can be measured in terms of its SNDR. There is a trade-off between performance and power consumption, that is, the former decreases with reduction of the latter. Therefore, as stated by Annema *et al.* [38], we can conclude that, "for a given power budget the performance drops when migrating to newer technologies, simply because of their lower supply voltages." This represents one of the challenges when passing from a technology node to a newer one.

The current DPS design that will be scaled down was originally made in the Taiwan Semiconductor Manufacturing Corporation (TSMC) $0.18\,\mu\mathrm{m}$ process, where the supply voltage available for the core design is $1.8\,\mathrm{V}$. For the International Business Machines (IBM) $130\,\mathrm{nm}$ process, the supply voltage is $1.2\,\mathrm{V}$, which represents a $0.6\,\mathrm{V}$ or 33% reduction. Finally, for the TSMC $65\,\mathrm{nm}$ process the supply voltage is $1.0\,\mathrm{V}$ for the core design which, compared to

Table 2.2: Parameters of a CMOS transistor. These parameters, as reported by Baschirotto *et al.* [41], have a dependence on process parameters, so they also vary from one technology node to another. For reference, supply voltage, as reported publicly by CMC [42, 43, 44], is also shown.

Parameter	180 nm	130 nm	90 nm	65 nm
Oxide thickness (nm)	4.45	3.12	2.20	1.80
Threshold voltage (V)	0.43	0.34	0.36	0.24
Transconductance ($\mu S/\mu m$)	500	720	1060	1400
Conductance ($\mu S/\mu m$)	40	65	100	230
Intrinsic gain (A/A)	12.5	11.1	10.6	6.1
Supply voltage (V)	1.8	1.2	1.0	1.0

the $0.18\,\mu m$ supply voltage, represents a $0.8\,V$ or 44% reduction. So, it is critical to account for the effects of inherent supply voltage decrease to avoid performance degradation. Although Table 2.2 focuses on transistor parameters, it also gives the supply voltages for reference.

2.1.2 Transistor Parameters

The benefits of migrating to newer technologies are area reduction (or putting more transistors in the space available) and, at least for digital circuits, dynamic power reduction by scaling of supply voltage. As newer processes appear, the minimum channel length and width and the gate-oxide thickness shrink. Also, several physical characteristics, such as doping, are scaled in the same proportion as the supply voltage to keep electrical characteristics similar while having a smaller device [33].

Therefore, it is important to take into account that important transistor parameters are being scaled, when migrating to newer technology nodes. Knowing the values of these parameters, given a certain technology, helps the designer determine the transistor's behavior and estimate its performance as part of a more complex circuit or system.

Table 2.2 shows some important parameters of the NMOS transistor for four consecutive technology nodes [40]. To show the transition between 130 and $65\,nm$ nodes, which were actually used for this thesis, the $90\,nm$ node is also included in this table. The reported transconductances are the peak values, under velocity saturation conditions. Moreover, reported conductance and intrinsic gain values were taken at peak transconductance conditions.

As mentioned earlier, as newer technologies appear, values for oxide thickness tend to reduce, and so does the threshold voltage, V_t. Nevertheless, this tendency slows down as channel lengths reach nanoscale proportions and the effects of leakage currents, and consequently power consumption, start to cause concern [39]. To overcome this problem, process

techniques are being developed to increase transistor performance while maintaining the gate-oxide thickness at around the same value, *i.e.*, without following Dennard's classical metal-oxide-semiconductor field-effect transistor (MOSFET) scaling method [45].

An important parameter of the MOSFET transistor is its transconductance, g_{m}, which indicates the sensitivity of the device to changes in its gate voltage or, in other words, how well the device trades gate voltage changes into changes in current. Under regular conditions it is given by

$$g_{\mathrm{m}} \approx \frac{W}{L} C_{\mathrm{ox}} \mu (V_{\mathrm{gs}} - V_{\mathrm{t}}), \tag{2.1}$$

where the mobility of the carriers, μ, is a function of the electric field. For short-channel devices, the mobility saturates with high electric fields ($\geq 10^4\,\mathrm{V/cm}$ for electrons) [46]. Because the supply voltage does not scale as fast as the channel length, the electric field across the channel increases in newer technologies, which predisposes the transistor to velocity saturation. Under velocity saturation conditions, g_{m} is given by

$$g_{\mathrm{m-peak}} \approx W C_{\mathrm{ox}} v_{\mathrm{sat}}, \tag{2.2}$$

where v_{sat} is the velocity saturation of the carriers, which is relatively independent of the technology node. As a result, for a fixed W, (peak) g_{m} is proportional to C_{ox}, which in turn is proportional to $1/t_{\mathrm{ox}}$. Since t_{ox} decreases in newer technologies, g_{m} simultaneously increases.

The conductance, g_{ds}, is the slope of the drain-to-source I-V curve of the transistor. It grows faster than g_{m}, at peak conditions, so the intrinsic gain of the transistor, which is $g_{\mathrm{m}}/g_{\mathrm{ds}}$, shrinks [40]. Knowing the intrinsic gain of the transistor is essential because this parameter is directly involved in the overall gain of more complex circuits. Because it decreases for newer technology nodes, other circuit techniques need to be explored in order to have the same performance in the scaled circuits. Fig. 2.1 shows the g_{m}, g_{ds}, and $g_{\mathrm{m}}/g_{\mathrm{ds}}$ trends.

Summing up, there are relationships between technology node, process parameters, and transistor performance. Being aware of these relationships should lead to a more careful design process to avoid overall performance decline when scaling the DPS.

2.1.3 Metal Layers

At the $180\,\mathrm{nm}$ node, we can find that there are six metal layers available with the same thickness [42]. However, at the 130 and $65\,\mathrm{nm}$ nodes, the number and kind of metal layers offered may differ, as can be confirmed by public information provided by the Canadian Microelectronics Corporation (CMC) [43, 44]. It is expected that physical characteristics, such as thickness and

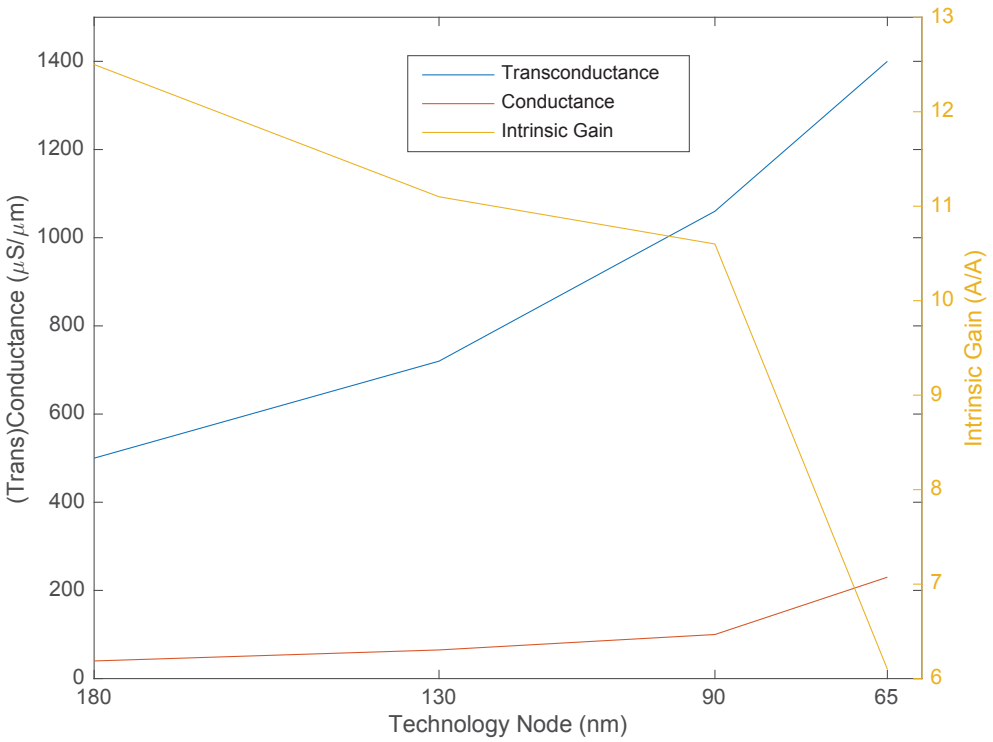


Figure 2.1: (Trans)conductance and intrinsic gain trends. Note that the intrinsic gain of a transistor, which is the ratio of transconductance to conductance, decreases in newer technologies.

spacing between metal layers, change from one process to another.

Also, in order to appropriately choose one metal layer over another, their electrical parameters should be reviewed first. With differentiation in thickness comes functional differentiation of the metal layers. Thus, thin metal layers are used for local interconnections, while thick ones, because of their lower resistance, are used for global interconnections and power distribution to minimize voltage drops.

Moreover, the differentiation of metal layers in the same technology node and the variation in thickness and availability of metal layers between different technology nodes, affect the optical properties of the sensor from node to node. In fact, scaling can be detrimental to the optical properties of an image sensor. As the number and thicknesses of metal layers increase, the distance that light must travel to reach the photodiodes also increases [8]. This must happen through increasingly narrow tunnels if the pixels also get smaller with scaling.

Fortunately, an advantage of using functional diversification through vertical integration, besides potentially reducing pixel size, is that the number and thicknesses of metal layers no longer affect the optical properties of the image sensor. This is due to the fact that photodiodes and related devices are placed in a dedicated semiconductor tier, where light enters from the back of the substrate, avoiding metal layers altogether.

Table 2.3: Capacitor parameters in a $130\,\mathrm{nm}$ process. The capacitance density of VNCAPs depends on the number of thin metals stacked. On the other hand, single and dual MIM capacitors have a fixed density because the top and bottom plates, and their separation, is fixed. Taken from IBM [48].

Specification	VNCAP	Single MIM	Dual MIM
Density ($\mathrm{fF}/\mu\mathrm{m}^2$)	0.17–1.3	2.05	4.10
Min. capacitance (fF)	6	60	680

2.1.4 Capacitors

For the DPS circuit made in the TSMC $180\,\mathrm{nm}$ process, metal-insulator-metal (MIM) capacitors were used. They are fabricated using two metals: a special capacitor top metal (CTM) layer, used as the top plate; and the ordinary metal layer just below it, used as the bottom plate of the capacitor. Both plates are separated by an insulator [47].

It is expected that for different processes, given the fact that physical characteristics are scaling, the same kind of capacitor does not have the same electrical characteristics. Also, different processes may or may not offer certain kinds of capacitors. This means that, for each design in a different process, the selection of the most suitable capacitor has to be reevaluated.

For instance, for the IBM $130\,\mathrm{nm}$ process, the kind of capacitors permitted for implementation depends on the different design kit options within the process. The option that is supported, for fabrication through CMC, allows the implementation of MIM capacitors and/or vertical natural capacitors (VNCAPs). MIM capacitors can be either single or dual depending on the layer selected to be the bottom and top plates. On the other hand, VNCAPs are formed using two or more consecutive thin metal layers. Values of the capacitance density for these three types are shown in Table 2.3 [48]. The table also gives the minimum capacitances possible.

Once the type of capacitor has been selected, the oversampling ratio (OSR) and the capacitor sizes, used in the $\Delta\Sigma$ ADC of the DPS, should be set to the minimum values needed, to meet the ADC specifications, so that power consumption is kept at an appropriate level [18]. Though smaller capacitors occupy less area, they present higher mismatch, which produces higher gain error in the integrator, and more thermal noise (kTC). Therefore, capacitor sizing should be handled carefully to avoid performance degradation.

As we can see in Table 2.3, the dual MIM capacitor has the highest density, which means that, for a given capacitance not limited to the minimum, the area needed would be the smallest one possible with the three capacitor types in the table. Nevertheless, what matters for the capacitors that are used in the $\Delta\Sigma$ DPS, as shown later in Section 2.2, are the ratios of various capacitances rather than the absolute value of each capacitance. Thus, using the mini-

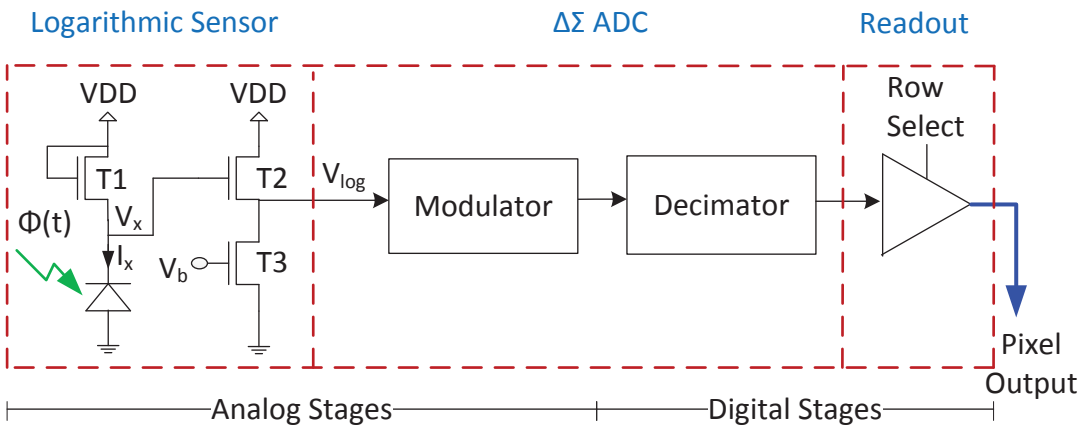


Figure 2.2: Simplified diagram of the $\Delta\Sigma$ DPS. It is composed of a logarithmic APS, a $\Delta\Sigma$ ADC, and a readout circuit.

mum allowed capacitance for this technology will suffice, provided its layout uses the smallest possible area.

The TSMC $65\,\mathrm{nm}$ process has two main capacitor options: MIM and metal-oxide-metal (MOM) capacitors. The latter are formed by stacking metal layers and their minimum dimensions, allowed by this technology, are smaller than for MIM capacitors. Thus MOM capacitors are becoming more attractive in technologies beyond $65\,\mathrm{nm}$ [49]. However, depending on the number of stacked metals, the MOM capacitor would need to be placed beside other devices in the same tier, while the MIM capacitor could be placed on top, not contributing to the total area usage.

2.2 Analog Stages

As mentioned earlier in this thesis, prior to this work, a $\Delta\Sigma$ DPS array was developed by Mahmoodi and Joseph [2] for a $180\,\mathrm{nm}$ CMOS process and validated experimentally. Fig. 2.2 shows the simplified block diagram of a pixel in said $\Delta\Sigma$ DPS array, where the light signal is transformed to a digital output by passing through different stages: sensor, $\Delta\Sigma$ ADC, which includes modulator and decimator at pixel level, and readout. Fig. 2.2 also shows, though at a high level, the topologies chosen to implement each stage. This section encompasses the circuit design of the analog stages of the $\Delta\Sigma$ DPS, *i.e.*, sensor and modulator.

2.2.1 Sensor

The first stage of a $\Delta\Sigma$ DPS, *i.e.*, the sensor, is formed by two main elements: a photodiode and a logarithmic circuit. The photodiode is responsible for the light-to-current signal

conversion. There are three ways to implement a CMOS photodiode [50], *i.e.*, n-diff/p-sub, p-diff/n-well/p-sub, and n-well/p-sub. The latter was used because, compared to the other two options, it presents better sensitivity, noise behavior, and SNR due to higher quantum and collection efficiency and smaller capacitance [50]. However, high dark-current is expected in this type of photodiode, unless dark-current reduction techniques are applied [51].

Back-illuminated pixels with substrate thinning, which can use either planar or 3D (two or more tier) technologies, offer a means to avoid the undesirable effects that scaling has on the photodiode's optical properties. In this case, because we would like to investigate the effect of using 3D technologies to make the $\Delta\Sigma$ DPS competitive in terms of pixel size, we assume two-tier technology processes are available for the three technologies used in this chapter. For this, the photodiode is left unplaced when laying out the circuit because it is assumed that it will be placed in a different tier than the rest of the circuits in the $\Delta\Sigma$ DPS.

The logarithmic circuit is responsible for the (photo)current-to-voltage signal conversion. The output voltage, as the name of the circuit suggests, is logarithmic. In fact, subjective brightness, which is the intensity as perceived by the human visual system, is also a logarithmic function of the light intensity incident on the eye [52]. So, logarithmic sensors and the human eye behave in a similar manner.

Work on logarithmic sensors, based on current-to-voltage conversion using a CMOS transistor in sub-threshold mode, can be found in the literature [53, 54, 55]. For a transistor to operate in sub-threshold mode, both

$$V_{\mathrm{g}} - V_{\mathrm{s}} \leq V_{\mathrm{t}} + nkT/q \tag{2.3}$$

and

$$V_{\mathrm{d}} - V_{\mathrm{s}} \gg kT/q \tag{2.4}$$

need to be satisfied. Here V_{g}, V_{s}, and V_{d} are the voltages at the gate, source, and drain of a transistor, respectively.

Under these conditions, from Fig. 2.2, the voltage-current relationship of transistor T1 is given by

$$V_{\mathrm{x}} = \mathrm{VDD} - V_{\mathrm{t}} - \frac{q}{nkT} \ln\left(\frac{I_{\mathrm{x}}}{I_{\mathrm{d0}}}\right), \tag{2.5}$$

where

$$I_{\mathrm{d0}} = \frac{W}{L}\mu_{\mathrm{n}}C_{\mathrm{ox}}\frac{1}{n}\left(\frac{nkT}{q}\right)^2 \exp(-1). \tag{2.6}$$

V_{x} and I_{x} are the output voltage and input current of the diode-connected transistor, as indicated in the figure. Also, V_{t} and kT/q are the threshold and thermal voltages respectively, while n represents a relationship between the capacitances of the gate oxide and depletion layers. W, L, and μ_{n} represent the MOSFET's width, length, and electron mobility, respectively.

Again with the assistance of Fig. 2.2, the logarithmic circuit, which can be found in the sensor block, is formed by three transistors. Transistor $\mathrm{T1}$ gives the circuit its logarithmic behavior, while transistors $\mathrm{T2}$ and $\mathrm{T3}$ work as a source follower, which is used as a voltage buffer to feed the next stage of the DPS, *i.e.*, the modulator.

Fig. 2.3 shows typical and corner DC responses of the logarithmic sensor for 180, 130, and $65\,\mathrm{nm}$ processes using the 3T circuit described. From this figure, the logarithmic sensor responses can be modeled as [7]

$$V_{\log} \approx a + b_0 \log(c + x), \tag{2.7}$$

where a, b_0, and c can be calculated by using nonlinear regression. The slope of the DC response of the logarithmic sensors, b_0, can help us estimate important parameters such as the PSNDR of each DPS design, as will be shown in Section 2.4.1.

Another parameter to consider is the range at the output of the logarithmic sensor, $V_{\log-\mathrm{PP}}$. It can be expressed as

$$V_{\log-\mathrm{PP}} \approx DR \cdot b_0 + \Delta V_{\max}, \tag{2.8}$$

where DR is the dynamic range of the pixel and $\Delta V_{\max}$ is the maximum voltage difference between two extreme corners, as seen in Fig. 2.3. The design parameters of the logarithmic sensor can be adjusted to obtain a voltage range that is within the expected values for the next stage, *i.e.*, the $\Delta\Sigma$ modulator.

2.2.2 Modulator

The second stage of a $\Delta\Sigma$ DPS is the $\Delta\Sigma$ modulator. As stated earlier in this thesis, for target applications with high bit-resolution at low sampling rates, $\Delta\Sigma$ ADCs are preferred because they do not demand high-accuracy analog components and are less vulnerable to noise [20]. The $\Delta\Sigma$ modulator can use either a continuous-time or a switched-capacitor design. While

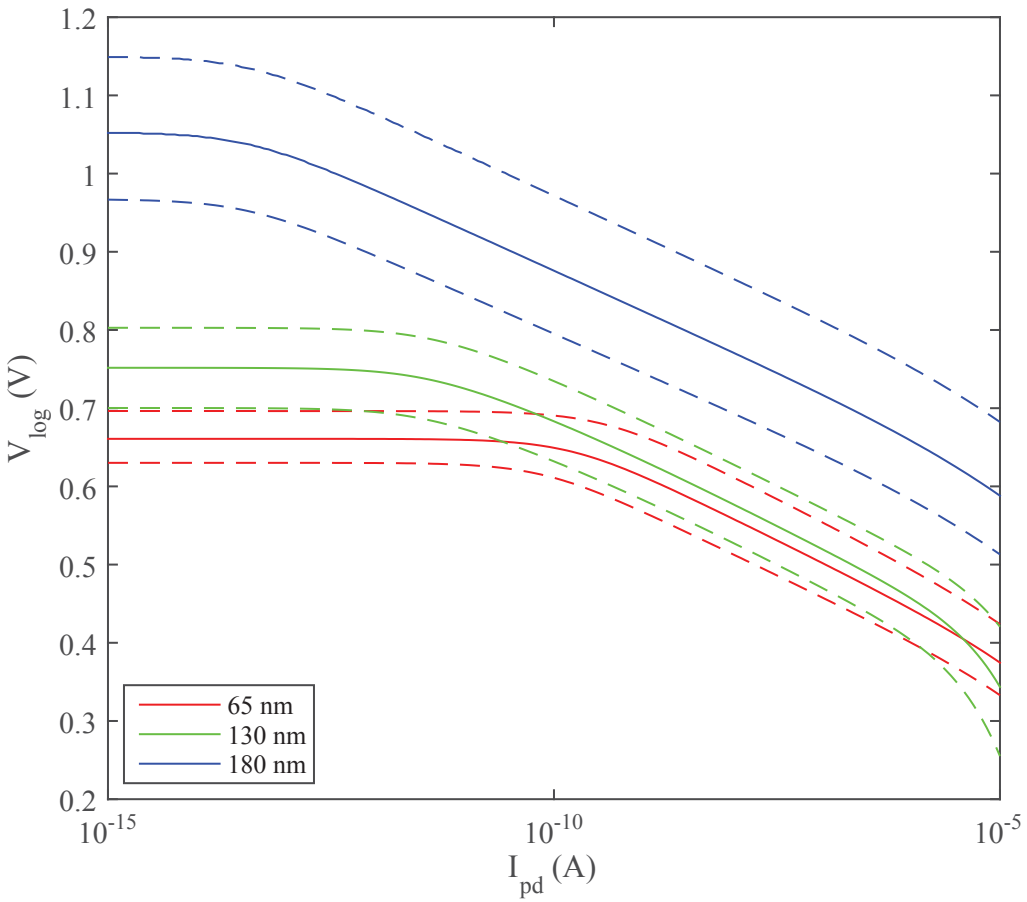


Figure 2.3: DC responses of the logarithmic sensor for three processes. Typical (solid lines) and corner (dashed lines) simulation results are given for 180, 130, and 65 nm processes using the 3T NMOS logarithmic circuit, including diode. A current source placed in parallel with the reverse-biased diode is used to represent the photocurrent generated by the incident light. Worst-case corners are shown (fast-fast and slow-slow).

continuous-time modulators behave better in terms of power consumption and speed, they are more complicated to design, are more sensitive to clock jitter, and present excessive loop delay. It is for these reasons, and because the latter can be more efficiently realized in standard CMOS technology, that switched-capacitor modulators are preferred [56, 57]. In addition, Mahmoodi and Joseph [26] also chose it over its continuous-time counterpart.

From a functional point of view, the switched-capacitor first-order modulator is formed by four main blocks: a differencer, an accumulator, a one-bit embedded ADC, and a one-bit embedded digital-to-analog converter (DAC), as shown in Fig. 2.4(a). Following Mahmoodi and Joseph [26], the differencer and one-bit embedded DAC blocks can be combined to form a new block, illustrated in Fig. 2.4(b), called the embedded DAC and differencer (EDD) in this thesis. Also, the accumulator, a switched-capacitor circuit shown in the functional diagram,

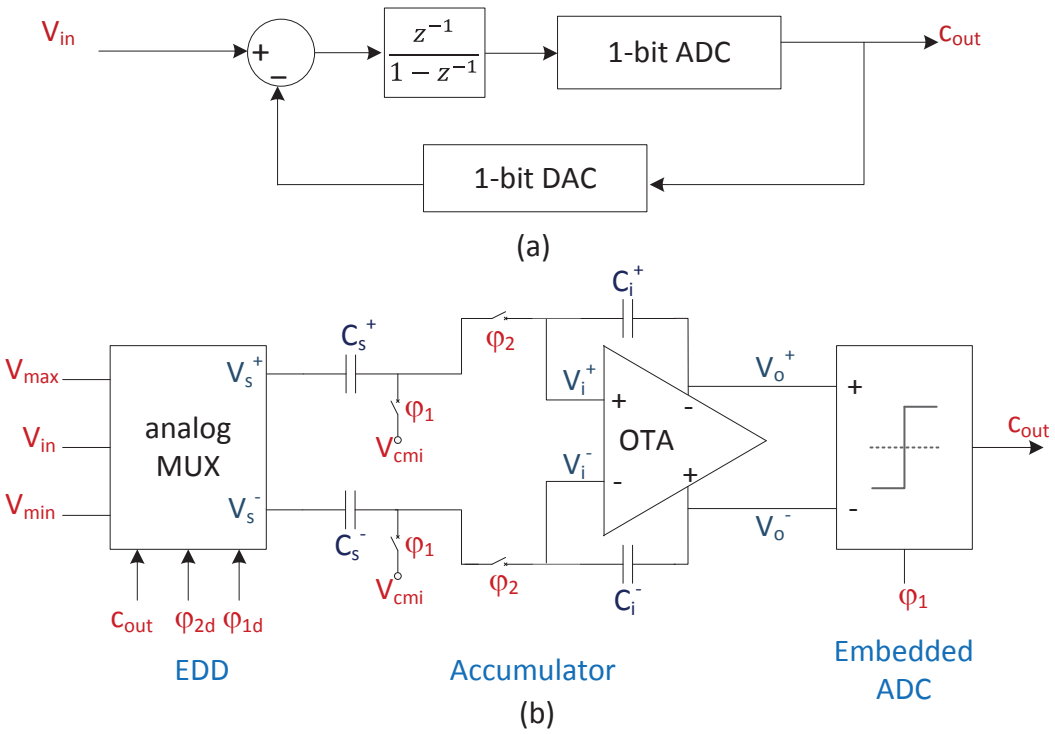


Figure 2.4: Diagrams of the first-order modulator. (a) Functional diagram, which shows that the modulator is composed of a differencer (summation block), an accumulator, a one-bit ADC, and a one-bit DAC. (b) Implementation diagram, which shows that the differencer and DAC represent one block, realized with an analog MUX, that the accumulator is realized with an OTA-based switched-capacitor circuit, and that the ADC is realized with a comparator

is actually implemented using an operational transconductance amplifier (OTA), a continuous-time circuit as can be seen in the implementation diagram.

Table 2.4 shows the component count, *i.e.*, the number of transistors and capacitors, per block of the first-order $\Delta\Sigma$ modulator. As can be seen, the accumulator uses a few more transistors compared to the other blocks, *i.e.*, the EDD and the one-bit ADC. Moreover, the accumulator is the only block that includes capacitors besides transistors. The capacitors could have a significant impact on the area usage of the block unless they are placed on top of the $\Delta\Sigma$ ADC, which can be done in the same tier using metal layers appropriately.

Even though the transistor counts of blocks in the first-order modulator are not significantly different, it is important to point out that transistors in the EDD and the one-bit ADC blocks can be sized to minimum width, as in a fully digital circuit, without causing performance degradation. This is not the case for the accumulator, which is composed of an OTA, switches, and capacitors and whose performance depends on a careful selection of the width and length of each transistor. It is for this reason that we can safely assume that the accumulator will have a greater impact on area usage than the other blocks that form the modulator. Hence,

it dominates the area usage of the first-order modulator. The subsequent parts of this section elaborate more on the schematics of each block contained in the $\Delta\Sigma$ modulator.

Embedded DAC and Differencer

Because the EDD block has the single-ended output of the logarithmic sensor as its input, it is designed to have a single-ended input. Also, in order to exploit the advantages a differential circuit offers, differential outputs are needed. Moreover, by doing this, the next stages can further enjoy the advantages of fully-differential circuits, such as the reduction of common-mode noise due to power supply disturbances.

The circuit used to implement the EDD sub-block is essentially an analog multiplexer, as shown in Fig. 2.5. Table 2.5 summarizes its operation. Its main purpose is to pass an analog voltage (either V_{min}, V_{max}, or V_{in}) depending on the state of c_{out}, which is the output of the ADC sub-block inside the modulator.

V_{min} and V_{max} are reference voltages, where $V_{\mathrm{min}} \leq V_{\mathrm{in}} \leq V_{\mathrm{max}}$. V_{in} is the output of the logarithmic sensor and, therefore, the input of the $\Delta\Sigma$ ADC. Clocks $\phi_{2\mathrm{d}}$ and $\phi_{1\mathrm{d}}$ are the delayed versions of ϕ_2 and ϕ_1, where the latter are used to control the switched capacitors.

Operational Transconductance Amplifier

When choosing the topology of the OTA to be used in the switched-capacitor circuit, speed is an important parameter to take into account given that SNR increases as the OSR increases. Therefore, an OTA with high gain and large bandwidth is desirable. In order to reduce pixel area while obtaining a high enough DC gain, a one-stage OTA is preferable. Also, since it will be driving capacitive loads, the chosen OTA should have a high output impedance. For these reasons, a folded-cascode OTA is used in the accumulator sub-block.

Fig. 2.6 shows the schematic diagram of the OTA, which is a part of the accumulator sub-block. The current through transistors $\mathrm{P2}$ and $\mathrm{P3}$, I_3, is assumed to be $1.5I_{\mathrm{b}}$. Also, the current

Table 2.4: Blocks and component counts of the first-order modulator. According to component count, the accumulator is the dominant block of the first-order modulator.

Quantity	Block(s)	Transistors	Capacitors
1	1-bit EDD	24	0
1	Accumulator	27	4
1	1-bit ADC	25	0
	All	76	4

Table 2.5: Truth table of the analog multiplexer. Depending on the state of c_{out}, $\phi_{2\mathrm{d}}$, and $\phi_{1\mathrm{d}}$, V_s^+ and V_s^- can be V_{min}, V_{in}, V_{max}, or high impedance (Z). Taken from Mahmoodi [18].

c_{out}	$\phi_{2\mathrm{d}}$	$\phi_{1\mathrm{d}}$	V_s^+	V_s^-
0	0	0	Z	Z
0	0	1	V_{in}	V_{min}
0	1	0	V_{min}	V_{in}
0	1	1	$-$	$-$
1	0	0	Z	Z
1	0	1	V_{in}	V_{max}
1	1	0	V_{max}	V_{in}
1	1	1	$-$	$-$

through transistors $\mathrm{N2}$, $\mathrm{N3}$, $\mathrm{N4}$, and $\mathrm{N5}$, I_4, is assumed to be equal to I_{b}. Currents that flow through $\mathrm{P4}$ and $\mathrm{P5}$ depend on the currents that flow trough $\mathrm{N8}$ and $\mathrm{N9}$. Therefore, the output currents, I_{out}^+ and I_{out}^-, are controlled by the voltage difference of the inputs of the differential pair formed by transistors $\mathrm{N8}$ and $\mathrm{N9}$.

A common-mode feedback (CMFB) circuit was added in order to set the common mode of the outputs to a controlled value. This is possible using negative feedback, *i.e.*, by converting the output voltage of the CMFB circuit to a current flowing through the transistor $\mathrm{N7}$ to adjust the current flowing through the input branch.

Accumulator

The discrete-time accumulator sub-block, which approximates a continuous-time integrator, has the differential output of the multiplexer as its differential inputs. Since its outputs are also differential, this is a fully-differential block that takes advantage of the superior power supply rejection ratio (PSRR) characteristic of this kind of circuit over the single-ended version. Its main purpose is to sample and accumulate the outputs of the multiplexer in the previous stage.

The output of the accumulator sub-block can be expressed as

$$V_{\mathrm{o}}[n+1] = \begin{cases} V_{\mathrm{o}}[n] + 2gV_{\mathrm{A}}[n], & c_{\mathrm{out}}[n] = 0, \\ V_{\mathrm{o}}[n] + 2gV_{\mathrm{B}}[n], & c_{\mathrm{out}}[n] = 1, \end{cases} \tag{2.9}$$

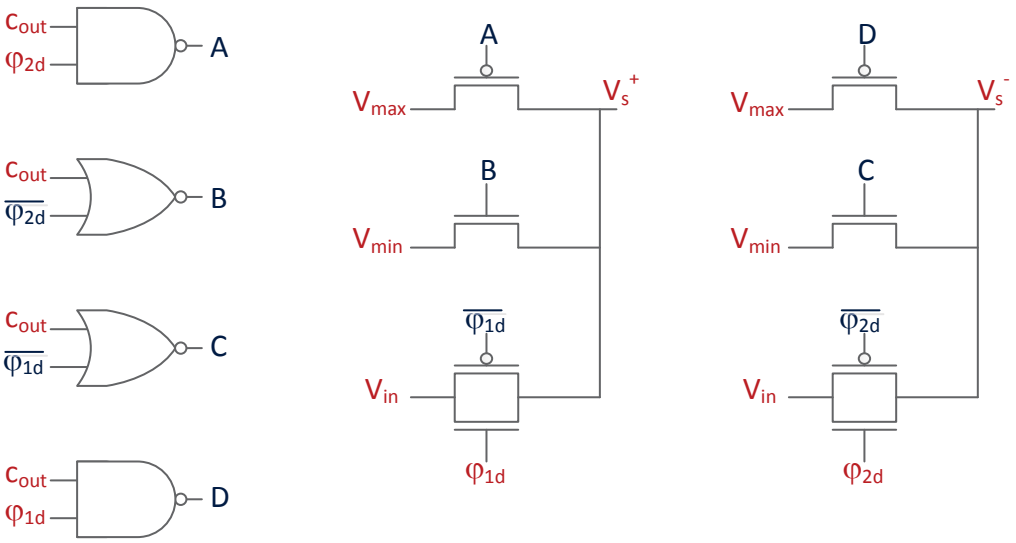


Figure 2.5: Schematic of the embedded DAC and differencer. An analog multiplexer is used to implement the EDD sub-block. Taken from Skorka *et al.* [58].

where

$$V_{\mathrm{o}}[n] = V_{\mathrm{o}}^{+}[n] - V_{\mathrm{o}}^{-}[n], \tag{2.10}$$

$$V_{\mathrm{A}}[n] = V_{\mathrm{in}}[n] - V_{\mathrm{min}}, \tag{2.11}$$

$$V_{\mathrm{B}}[n] = V_{\mathrm{in}}[n] - V_{\mathrm{max}}, \tag{2.12}$$

$$g = C_{\mathrm{s}}/C_{\mathrm{i}}. \tag{2.13}$$

The capacitor ratio in (2.13) is computed from

$$V_{\mathrm{o-PP}} = 4V_{\mathrm{in-PP}} \cdot g. \tag{2.14}$$

It is well known that smaller capacitors present a larger mismatch, and this is reflected in the inaccuracy of the gain. However, first-order structures are not sensitive to capacitor mismatch [18]. Thus, it is desirable to size C_{s} and C_{i} to be the minimum capacitances permitted by the technology. Nevertheless, according to

$$\sigma_{\mathrm{n}}^2 = \frac{24kT}{C_{\mathrm{i}}}, \tag{2.15}$$

the smaller the capacitor, the greater the kTC noise, so the latter also becomes a limiting factor when choosing C_{s} and C_{i}.

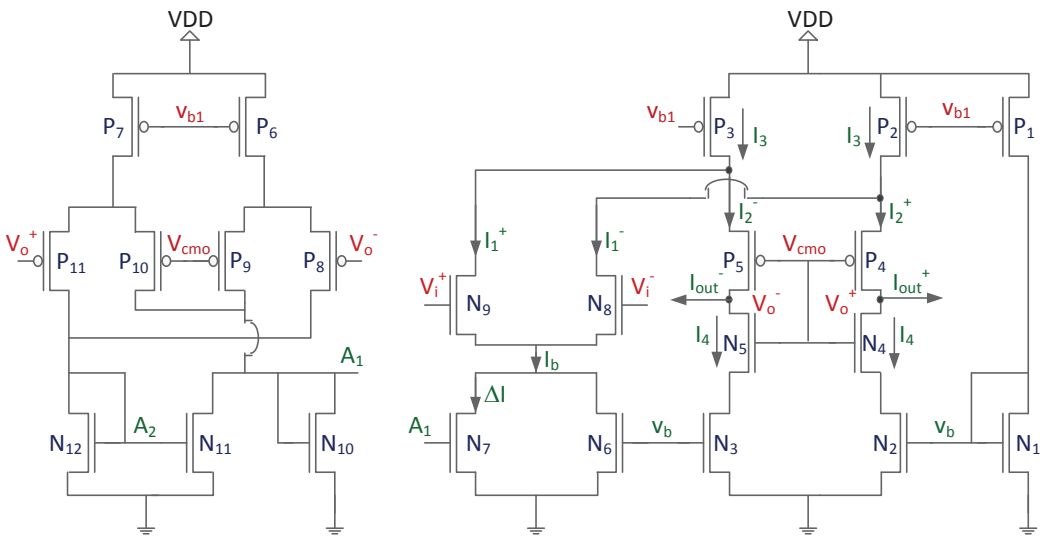


Figure 2.6: Schematic of the folded-cascode OTA. A fully-differential topology was chosen because of its rejection of common-mode noise. Voltages V_{b1} and V_{b2} are generated at board level, *i.e.*, externally. Taken from Skorka *et al.* [58].

Embedded ADC

The embedded ADC sub-block takes the differential outputs of the accumulator as its inputs and compares them while ϕ_1 is asserted. It follows the behavior of a comparator, *i.e.*, the output, c_{out}, is '1' when V_o^+ is greater than V_o^-; otherwise, it is '0'. Fig. 2.7 shows the topology chosen to implement the comparator. While the accumulator integrates during each ϕ_2 pulse, the embedded ADC takes its differential outputs to compare them during each ϕ_1 pulse.

2.3 Digital Stages

After the light signal has been transformed to a high-rate bitstream by the $\Delta\Sigma$ modulator, the next stage, *i.e.*, the decimator, has the objective of down-sampling the modulator output, while the readout makes available the down-sampled decimator output outside the pixel, at chip level. This section focuses on the circuit design of these two digital blocks.

2.3.1 Decimator

The main tasks of a $\Delta\Sigma$ decimator are to filter out-of-band components and quantization noise, shaped by the $\Delta\Sigma$ modulator, and to down-sample the filtered signal to the Nyquist rate [20]. The output of the decimator represents the analog signal at the modulator input using a lower bit rate than the stream that comes from the modulator output, but with more bits per sample.

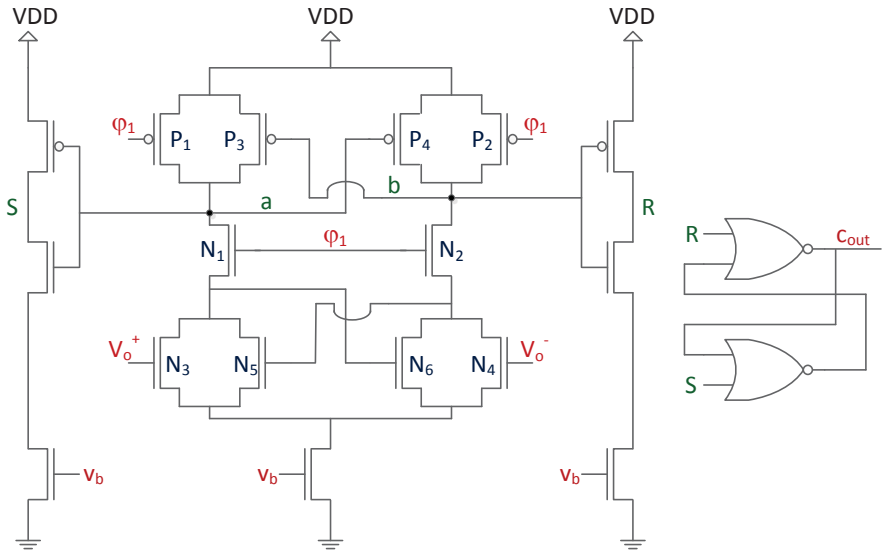


Figure 2.7: Schematic of the embedded ADC. A one-bit comparator has been used to implement this block. Taken from Skorka *et al.* [58].

The decimator circuit presented here is based on the decimator patented by Mahmoodi and Joseph [26]. Moreover, this decimator has been chosen because it is a simpler way, *i.e.*, using less area per ADC, to implement an array of decimators for an array of in-pixel $\Delta\Sigma$ modulators. These parallel decimators are based on a second-order finite-duration impulse response (FIR) filter having exactly M taps, M being the OSR of the modulator [18]. The coefficients of the decimation filter are generated at chip level and are shared by all the $\Delta\Sigma$ ADCs in the DPS array. The input of the decimator, *i.e.*, the output of the modulator, and the coefficients are then efficiently multiplied in a serial manner. Serial multiplication is chosen over a parallel one to reduce circuit area. Finally, the output of the accumulator is read out every M samples.

For a first-order modulator, the decimator can be configured as a parabolic FIR filter as follows [26]:

$$h_{\text{dec}}[n] = \frac{1}{S}\begin{cases} h[n], & 0 \leq n \leq M-1; \\ 0, & \text{otherwise;} \end{cases} \tag{2.16}$$

$$h[n] = M + n(M-1) - n^2; \tag{2.17}$$

$$S = \frac{M(M+1)(M+2)}{6}. \tag{2.18}$$

Here, $h_{\text{dec}}[n]$ represents the normalized coefficients of the filter's impulse response, $h[n]$ represents the de-normalized (integer) coefficients, and S, which is the coefficient sum, is the coefficient normalization. The coefficients for the FIR filter are associated with the OSR, M,

of the modulator according to (2.17).

Generation of de-normalized coefficients is also straightforward to implement. This is because the de-normalized coefficients $h[n]$ are of the form

$$h[n+1] = 2h[n] - h[n-1] - 2, \tag{2.19}$$

a recurrence relation that can be easily implemented. The coefficient generation can be done at chip level on the image sensor die or off-chip in an FPGA.

Fig. 2.8 shows the decimator circuit. It includes a one-bit full adder, a one-bit register, *i.e.*, a flip flop, an N-bit shift register, two NOR gates, and three inverters, which are all basic digital sub-blocks. Modifications to Joseph and Mahmoodi's patented circuit were done in order to reduce the transistor count and, consequently, the area. In digital circuits, the transistor count normally gives an idea of the area usage, assuming all transistors are sized to the minimum area allowed by the technology node.

Table 2.6 breaks down the transistor count for the decimator circuit. As can be seen, most of the transistors are used by the N-bit shift register, which suggests that efforts to reduce the overall area of the decimator have to focus on reducing the area of the shift register. For convenience, the rest of the pixel-level circuit is called a *macro* block.

As explained earlier, the decimator receives the modulator output, which is a one-bit signal at the oversampling rate. This rate determines the frequency at which the digital circuits in the decimator must work to guarantee proper operation of the ADC. Each value at the output of the modulator must be multiplied to an N-bit serial coefficient of the parabolic filter, N being the number of bits in the accumulator, and then accumulated. The process occurs for M coefficient values. Because both the output of the modulator and the coefficients are serial, the multiplication function can be easily implemented by an AND gate. In order to use the minimum number of transistors, a NOR gate is used instead. In this case, the inputs of the decimator will be inverted versions of the modulator output and serial coefficients.

The one-bit full adder performs the arithmetic sum of the bit-serial accumulator. By performing the addition operation serially rather than in parallel only a one-bit adder is needed instead of an N-bit one, therefore reducing the area usage. Fig. 2.9(a) shows the schematic used to implement the one-bit full adder. Since timing constraints are not the limiting parameter for the decimator, for optical image sensors, skewed gates are used to minimize the width of the PMOS transistors, *i.e.*, the PMOS and NMOS transistors have a $1:1$ size ratio even though the respective carrier mobilities do not have a $1:1$ ratio.

The one-bit register, *i.e.*, a flip flop, is used to store and feed back the carry out of the one-bit full adder. Flip flops, being part of the N-bit shift register, are also used to store

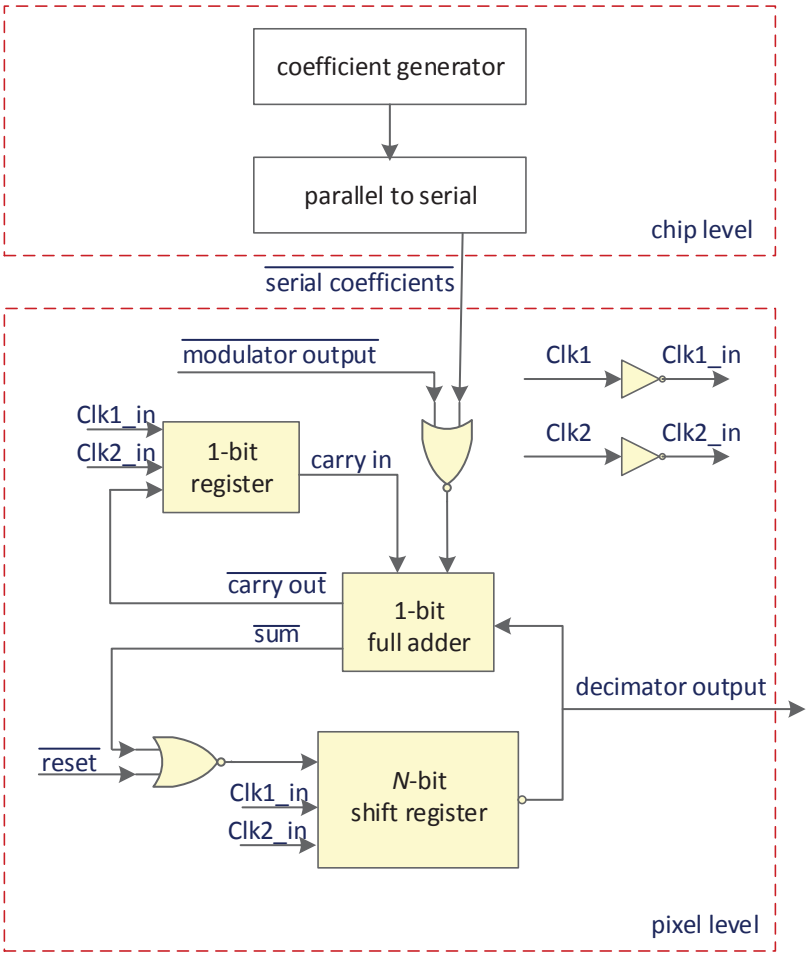


Figure 2.8: Block diagram of the small-area decimator. It is based on the decimator introduced by Mahmoodi and Joseph [26] and it is more compact than conventional decimators. Modifications were made to further reduce area.

the accumulator data. As described in Mahmoodi and Joseph's patent [26], and in Mahmoodi's PhD thesis [18], two pulsed latches were chosen to implement each flip flop, which utilizes only eight transistors. Though this approach works well, proper operation under more restrictive conditions, *i.e.*, lower supply voltage, higher leakage current, etc, needs to be ensured. The circuit is shown in Fig. 2.9(b).

Among the technology nodes considered in this thesis, the $65\,\mathrm{nm}$ one presents a higher leakage current that considerably affects the behavior of the flip flop. Switches in the two pulsed latches cause undesirable behavior in the flip flop, shift register, and the entire decimator. In order to avoid this, low leakage transistors were considered with the 130 and, especially, the $65\,\mathrm{nm}$ processes. However, the extra layer needed to lay-out the low-leakage transistors generates more restrictions in device closeness, increasing the flip-flop area considerably. It is for this reason that, instead, greater transistor sizes were considered instead to avoid the

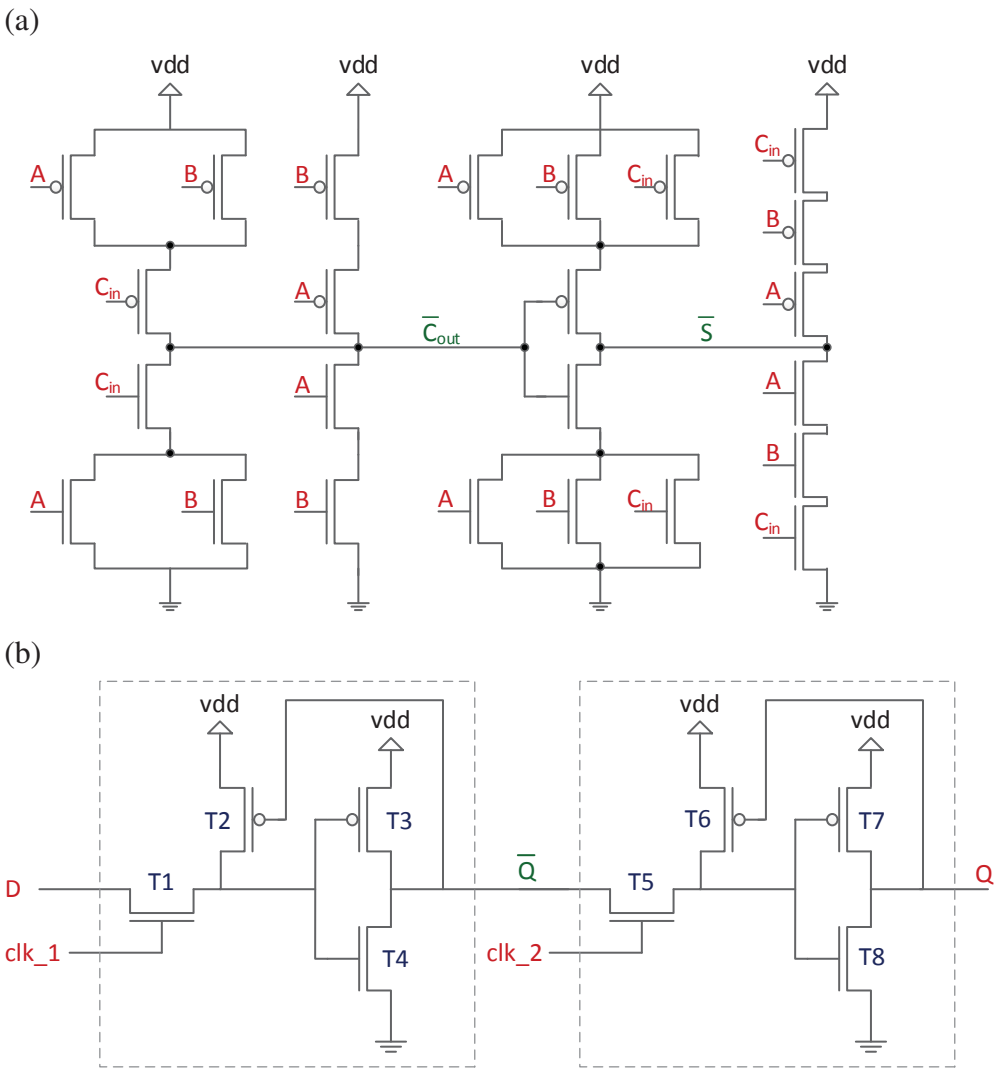


Figure 2.9: Schematics of the full adder and the flip flop. (a) This one-bit full adder, along with a shift register, implements bit serially the accumulator of the $\Delta\Sigma$ decimator. Inverted outputs, $\bar{S}$ and $\bar{C}_{\text{out}}$, suffice. (b) This flip flop, using two pulsed latches, is the building block of the shift register.

leakage issue.

Another thing to take into account is the effect of the clock slope on the operation of the circuit. Because it is well-known that this kind of flip flop might be sensitive to the clock slope, an inverter (buffer) per decimator per clock is included in order to sharpen the clock signal coming from the chip level.

The total number of transistors in the decimator circuit is $46 + 8N$. Assuming the number of bits of the N-bit register is 16, 128 transistors per decimator are needed. It can be noticed that the decimator concentrates most of the transistors in the N-bit shift register. It is for this reason that its basic cell, *i.e.*, the flip flop, has to be carefully laid out in order to reduce the total area usage of the decimator. Also, because the accumulator needs to be reset after the accumulation is done, a second NOR gate is listed in Table 2.6 to implement the reset function.

2.3.2 Readout

So far, all circuits and operations have been explained focusing only on the data conversion mode of the $\Delta\Sigma$ DPS, which converts an analog stimulus at the input of the photodiode to a digital value that appears at the output of the decimator. In fact, the $\Delta\Sigma$ DPS has two operation modes, *i.e.*, conversion and readout. Both operation modes happen in a frame period that starts with parallel data conversion and ends with sequential data readout.

Fig. 2.10 shows these modes of operation. The conversion time depends on the OSR and the oversampling period. It does not depend on the number of pixels in the DPS array because the analog-to-digital conversion of each pixel is done simultaneously. After the conversion phase has been completed, the digital data, of as many bits as the shift register in the decimator has, is available to be read. This operation, as presented by Mahmoodi *et al.* [2], is done sequentially. Therefore, the readout time does depend on the number of pixels in the DPS array.

Table 2.6: Blocks and transistor counts of the decimator. Here, N is assumed to be a multiple of 4, *i.e.*, an integer number of nibbles. Assuming $N \geq 16$, the shift register dominates the transistor count of the decimator.

Quantity	Block(s)	Transistors
3	Inverters	6
2	NORs	8
1	1-bit register	8
1	1-bit full adder	24
1	N-bit shift register	$8N$
	Total	$46 + 8N$

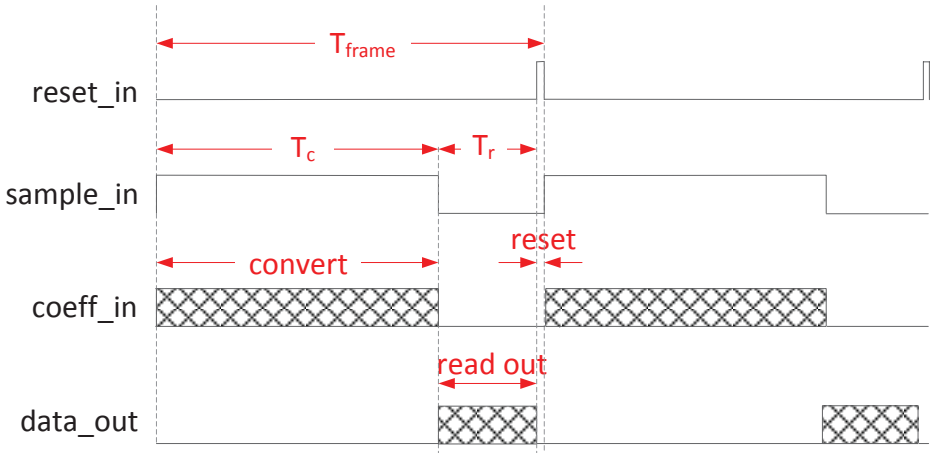


Figure 2.10: Modes of operation for a DPS. First, the inputs of all pixels are converted, at the same time, to a digital value during conversion mode. Afterward, the output of each pixel is read out, one pixel at a time. Once all pixels have been read out, a reset signal is activated to clear all registers. Based on Li's figure [59].

Clocks for conversion and readout may be provided off-chip by an FPGA. In the design presented by Mahmoodi *et al.* [2], two clocks are used in the $\Delta\Sigma$ decimator, as seen in Section 2.3. These two clocks work at a given frequency when in conversion mode and at a different one, a higher frequency, when in readout mode to reduce the time needed to read an individual pixel. Because readout time depends on the size of the array, reading one pixel after the other one is inefficient because it limits the frame rate.

The frame rate achieves its maximum value for a given conversion time when the readout time tends to zero. Because the conversion and readout times, in the mentioned readout circuit, are comparable, the major bottleneck when trying to increment the frame rate (or increase the array size) is to decrease the readout time. Also, as reported by the authors, the readout circuit presents high digital power consumption, even higher than the analog one. The digital power consumption, which includes decimation and readout, is way too high because of unnecessary active circuitry. In readout mode, only the shift register of the pixel to be read should "shift" while the shift registers of the remaining pixels should not. By having all shift registers shift in readout mode, a considerable amount of power is wasted. It is for these reasons that improvements to the readout circuit described by Mahmoodi *et al.* [2] were necessary.

In order to reduce the readout time, instead of reading each pixel sequentially by selecting one row and one column at a time, an entire row should be selected and then stored outside the pixel array to be read thereafter. This could be possible by having two registers arranged in a double-buffer manner with buffers at the base of each column of the array. The size of each register should be the number of bits of the shift register in the decimator. This way, the

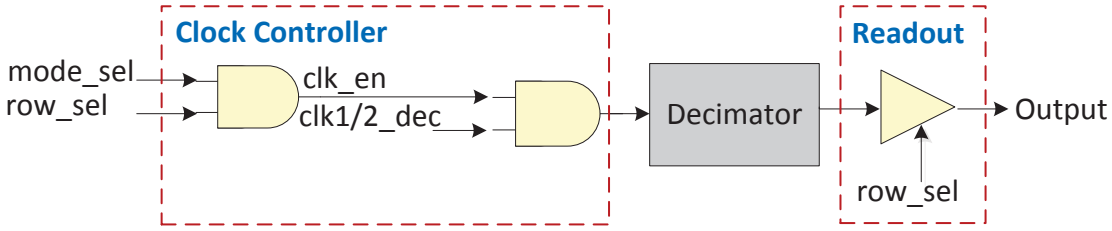


Figure 2.11: Readout circuit diagram. The clock controller, that is not part of the DPS design, deactivates the decimator clock of the pixels in a row that was not selected for readout. The readout connects the output of the decimator to the output of the pixel array.

readout time would depend on the number of rows rather than the number of pixels.

To select only one row at a time to shift the outputs of each DPS into the proposed column ping-pong buffer, there should be R row selectors, $\mathrm{row\_sel}$, in an array of $R \times C$ pixels, R and C being the number of rows and columns respectively. These selectors should come from the output of an address decoder and are meant to indicate whether a specific row has been selected, when it is "1", or not, when it is "0". These selectors would enable/disable a tristate buffer at the output of each decimator to close/open the path that connects this output to an appropriate column bus.

It is worth noticing that the capacitance contribution of the unselected pixels should be taken into account when sizing the row drivers and should not be assumed to be zero. In fact, the effect of the capacitance of the unselected pixels becomes more notorious for arrays with a great number of pixels. Because this chapter concerns the $\Delta\Sigma$ DPS itself, not a $\Delta\Sigma$ DPS array, the design of the double buffers, address decoder, and row drivers are not considered here.

In order to considerably reduce the power consumption of the digital part of the DPS, the shift registers of the unselected rows should be disabled [2]. In conversion mode, the decimator clock, $\mathrm{clock\_dec}$, should be activated for all rows, so all pixels work in parallel, shifting and storing ADC values in the shift register of each decimator. In readout mode, on the other hand, only one row is selected. To read an entire row, the outputs of each one of the C pixels in that row are exported to column-level double buffers. Therefore, only for that specific row, the decimator clock is active, while for the other rows it is not. This is possible by including a selector in each DPS that depends on the state of the mode selector and the row selector.

The mode selector, $\mathrm{mode\_sel}$, indicates in which mode the DPS array is working. When $\mathrm{mode\_sel}$ is "0", it is working in readout mode, otherwise, it is in conversion mode. Using a 3-input NOR gate with $\mathrm{mode\_sel}$, $\mathrm{row\_sel}$, and $\mathrm{clock\_dec}$ we can obtain a decimator clock $\mathrm{clock\_in}$ that satisfies the above mentioned requirements. Fig. 2.11 shows the block diagram of the readout approach explained here.

2.4 Results

This section presents the results obtained in this chapter when designing the $\Delta\Sigma$ DPS for three different technology nodes. These results can be divided into three main parts: verification, layouts, and projections.

The verification part shows qualitative results, which assess the correct operation of the DPS, and quantitative results, which indicate whether the DPS specifications were met. The layouts part, which involves floorplanning, gives us information about how the DPS circuits look in each technology node. Finally the projections part shows how close to the target pixel pitch the $\Delta\Sigma$ DPS technology is.

2.4.1 Verification

Here, qualitative results to determine the correct operation of the $\Delta\Sigma$ DPS are shown. This includes transient simulations and power consumption analysis of the $\Delta\Sigma$ DPS. Also, simulations that determine the quantitative performance of the $\Delta\Sigma$ ADC, which is the *heart* of the $\Delta\Sigma$ DPS circuit, in terms of signal-to-distortion ratio (SDR), are shown and used to characterize the entire DPS, including its DR.

In order to properly simulate the $\Delta\Sigma$ DPS operation, each one of its stages needs to be represented in the testbench. Recall that, the $\Delta\Sigma$ DPS is formed by a logarithmic sensor, which includes a photodiode, followed by a $\Delta\Sigma$ ADC, which includes a modulator and a decimator, and a readout circuit. For simulation purposes, the photodiode is modeled as a current source, which represents the photocurrent, in parallel with an n-well/p-sub diode. It represents the input of the DPS.

From the photodiode's perspective, the lower the current coming from the parallel current source, the lower the luminance and vice versa. The same applies to the input of a camera made out of a $\Delta\Sigma$ ADC array. This current range is translated, by the logarithmic circuit, into voltages within minimum and maximum allowed values at the input of the ADC. From the $\Delta\Sigma$ ADC's perspective, this range of allowed voltages depends on the technology node due to differences in the supply voltages, which restricts the output ranges of the sensor circuits in turn.

Because the modulator performance has great influence on the overall performance of the ADC, and the DPS in general, simulations were conducted to verify the adequate operation of this block. Fig. 2.12 shows the transient simulation results performed for the three technology nodes chosen in this chapter, *i.e.*, 180, 130, and $65\,\mathrm{nm}$, for a frame period. Each simulation shows the modulator outputs for three different steady (DC) inputs, *i.e.*, the corresponding minimum, half-scale, and maximum values for the technology node used. Analog signals at

the output of the accumulator ($V_{\mathrm{o}}^{+} - V_{\mathrm{o}}^{-}$) and at the output of the comparator, which is also the output of the modulator, are reported.

On the other hand, because decimator and readout are fully digital, even though supply voltages and output swing ranges vary between one technology to another, they should not affect the behavior of the circuit. Fig. 2.13 shows transient simulations performed for the three technology nodes chosen in this chapter, for a frame period. Each simulation shows the output of the decimators for a simple modulator output, *i.e.*, a constant '1', when the bit-serial coefficients are assumed to be uniformly 1 every time, M times, M being 16 in this case. These inputs make the output of the decimator easy to predict, that is, it should behave as a counter.

Although reducing the power consumption of the $\Delta\Sigma$ DPS was not an objective of this thesis, it is important to record this parameter to foresee its impact in a megapixel array. Table. 2.7 shows the average power consumption of the $\Delta\Sigma$ ADC for the 180, 130, and $65\,\mathrm{nm}$ designs. The total average power consumption is given by the average power consumption contributions of both modulator and decimator.

The average power of the modulator is given by the average for 10 different inputs of the average power consumed by the $\Delta\Sigma$ modulator when using the same testbench as in Fig. 2.12 for an entire frame ($20\,\mathrm{ms}$ out of $33\,\mathrm{ms}$ dedicated for conversion). The average power of the decimator is given by the average power consumed by the decimator when using the same testbench as in Fig. 2.13.

As reported by Mahmoodi [18], the power consumption of the modulator at the chosen working point, *i.e.*, at low root mean square (RMS) noise-and-distortion and with less variation of this parameter, is $4\,\mu\mathrm{W}$. As can be seen in Table 2.7, the $180\,\mathrm{nm}$ design presented in this thesis, which uses the same technology node as Mahmoodi, consumes 10 times more power. As expected, most of the excessive power consumption was found in the switched-capacitor circuit, more specifically, in the OTA. This is explained by the fact that, although this block is working, it was not optimized for power consumption, which needs to be addressed.

Also, Mahmoodi's reported decimator power consumption is $3\,\mathrm{nW}$, which is greater when compared to the approximately $16\,\mathrm{nW}$ reported in this thesis for the same technology node. This power reduction is due to the circuit and system (CAS) improvements applied to the decimator by reducing the number of transistors in the circuit. Also, further power reduction in an array level could be possible using the decimator design presented in this thesis, provided a clock controller is designed as specified in Section 2.3.2.

Power reduction is expected for smaller technology nodes, as was the case for the 130 and $65\,\mathrm{nm}$ designs when compared to the $180\,\mathrm{nm}$ design in this thesis and to Mahmoodi's design [18]. However, this is not the case for the $65\,\mathrm{nm}$ design when compared to the $130\,\mathrm{nm}$ design. Like the other designs, the $65\,\mathrm{nm}$ circuit was not optimized for power consumption. However,

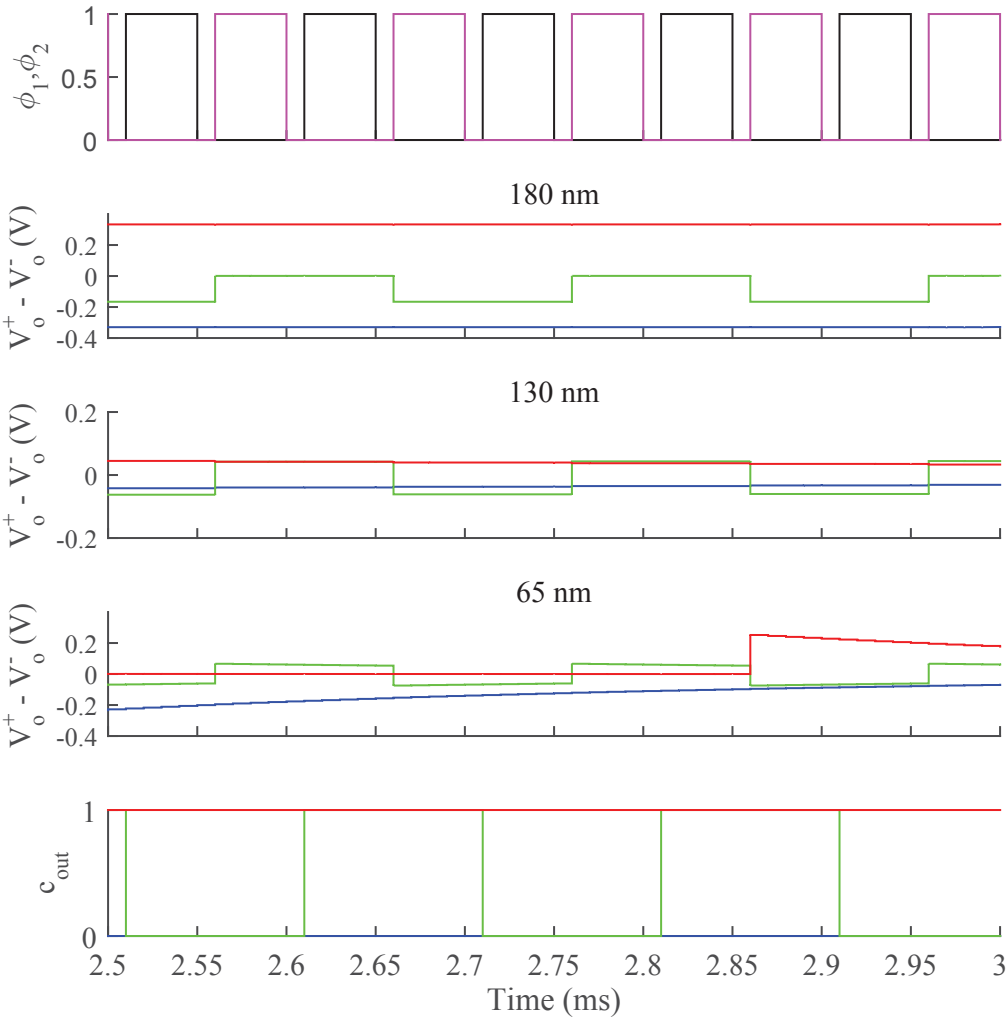


Figure 2.12: Transient simulation results for the modulators. It was obtained using the schematic view of the modulator for the 180, 130, and 65 nm designs. The differential output of the accumulator for each design, $V_o^+ - V_o^-$ (in Volts), and the modulator output, c_{out} (in bits), are shown for the minimum, maximum, and half-scale voltages at the input of the $\Delta\Sigma$ ADC.

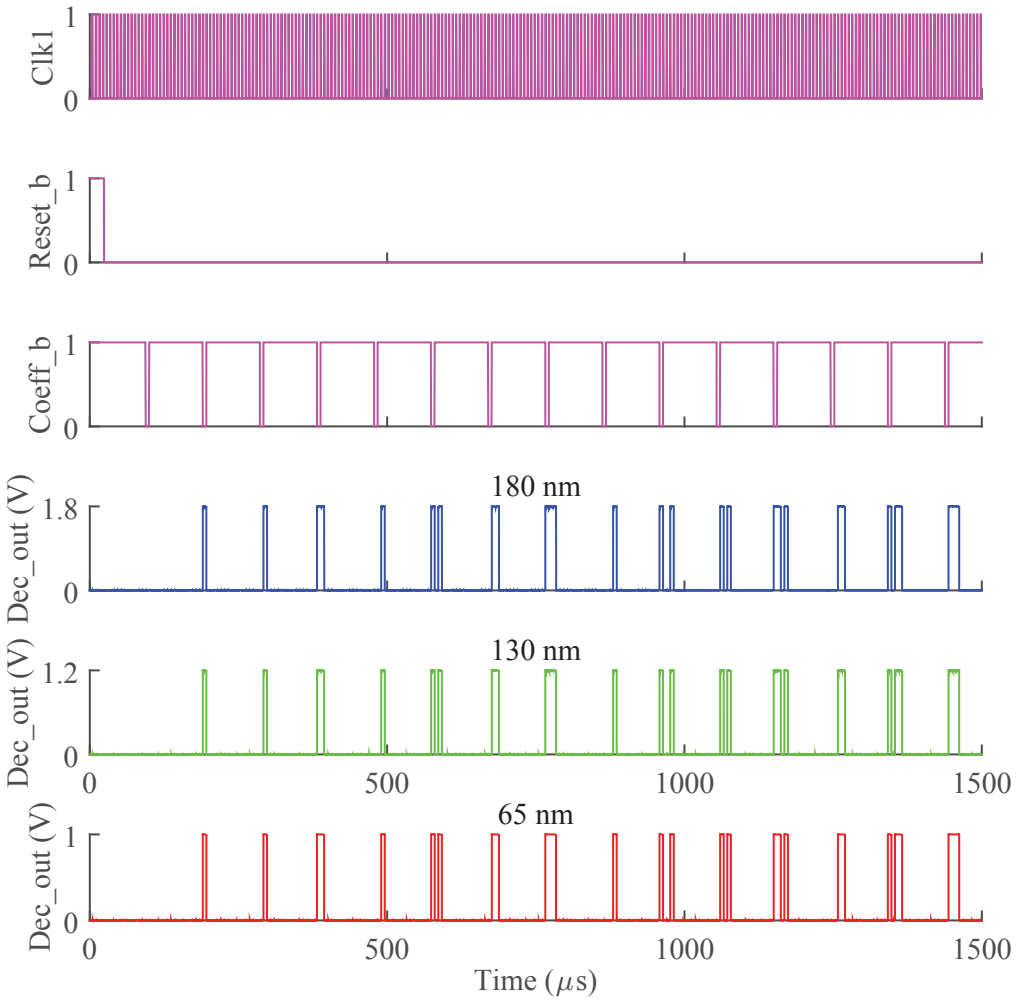


Figure 2.13: Transient simulation results for the decimators. These results were obtained using the schematic view of the decimator. Because the same testbench was applied to the 180, 130, and 65 nm designs, the coefficient inputs shown are normalized (logic '0' and '1').

Table 2.7: Power consumption for each technology node. Overall average power consumption for the 180, 130, and 65 nm designs are shown. Also, partial contributions made by the modulator and decimator, and main blocks are shown.

Parameter	180 nm	130 nm	65 nm
EDD (μW)	6.58×10^{-4}	8.67×10^{-4}	1.00×10^{-2}
OTA (μW)	41.10	2.79	4.43
Comparator (μW)	0.19	6.40×10^{-3}	0.95
Total modulator (μW)	41.30	2.80	5.38
Register (μW)	3.95×10^{-4}	9.73×10^{-4}	0.35
Shift register (μW)	1.45×10^{-2}	2.71×10^{-2}	0.87
Total decimator (μW)	1.65×10^{-2}	2.91×10^{-2}	1.33×10^{-3}
Total (μW)	41.30	2.79	6.71

other factors such as higher leakage of the technology node might be contributing to the overall higher than expected power consumption.

Once the qualitative behavior of the design is verified, it is necessary to characterize it to evaluate its performance. Quantitatively speaking, one important parameter to evaluate the performance of the DPS is its SDR, which is connected to the precision of the data conversion. Fig. 2.14 shows the normalized ADC outputs for a given input that varies from the minimum to the maximum value allowed in each one of the technology nodes used. The deviations from a straight line define the imprecision of the $\Delta\Sigma$ ADC, which varies with technology node.

It is important to verify that the specifications for the $\Delta\Sigma$ DPS, shown earlier in this chapter in Table 2.1, have been met. In order to do so, parameters such as PSNDR and DR are hand-calculated with the assistance of simulation results.

The logarithmic pixel response can be modeled as [7]

$$y = a + b\log(c + x) + \epsilon, \tag{2.20}$$

where y is the output of a logarithmic pixel, given in LSBs, due to a stimulus x, given here in Amperes. Also, a, b, and c represent the offset, gain, and bias values of the pixel. Because the logarithmic pixel is formed of a logarithmic sensor followed by an ADC, a, b, and c values are affected by both stages.

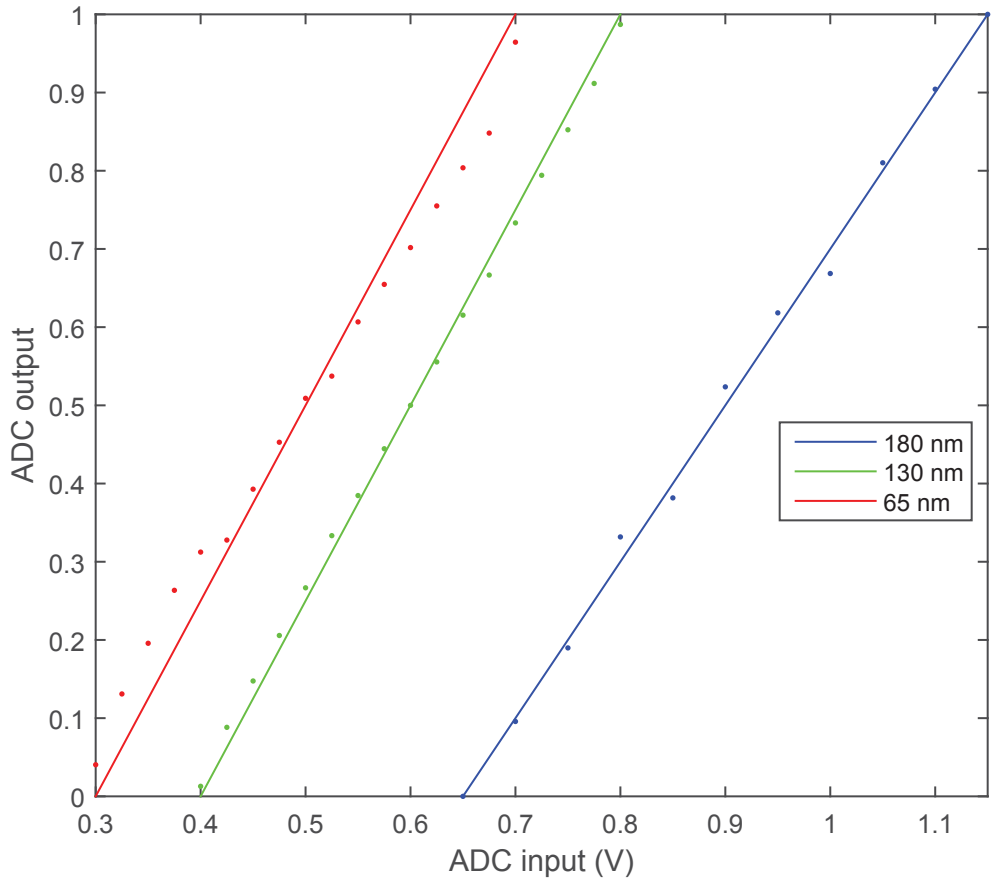


Figure 2.14: Output of the $\Delta\Sigma$ ADCs. The dots represent the actual data while continuous lines represent the best fit results. They were obtained for designs done at the 180, 130, and $65\,\mathrm{nm}$ technology nodes, using parametric and transient simulations of the modulator schematic, while the decimation was done using MATLAB.

The SNDR can be expressed as

$$SNDR = \frac{x}{\sigma_x} \cong \frac{x}{\sigma_y} \cdot \frac{dy}{dx} \tag{2.21}$$

$$= \frac{x}{\sigma_\epsilon} \cdot \frac{b}{\ln(10)(c+x)}, \tag{2.22}$$

where σ_x and σ_y represent the noise at the pixel's input and output, respectively. From this expression, when $x \gg c$, the PSNDR of the pixel can be expressed as

$$PSNDR = \frac{b}{\ln(10)\sigma_\epsilon}. \tag{2.23}$$

The DL is defined as the stimulus at which the noise and signal powers are equal, *i.e.*, the

SNDR at that condition is equal to $0\,\mathrm{dB}$. This can be expressed, using (2.22), as

$$0\,\mathrm{dB} = \frac{x_{\mathrm{DL}}}{\sigma_\epsilon} \cdot \frac{b}{\ln(10)(c + x_{\mathrm{DL}})}. \tag{2.24}$$

Using (2.23), this can be rewritten as

$$x_{\mathrm{DL}} = \frac{c}{PSNDR - 1}, \tag{2.25}$$

where c can be determined with the assistance of Fig. 2.3.

Also, the PSNDR of the DPS is always lower than its peak SDR (PSDR) because the latter excludes temporal noise contributions. Because

$$PSNDR \leq PSDR \leq PSDR_{\mathrm{ADC}}, \tag{2.26}$$

the PSNDR of the entire $\Delta\Sigma$ DPS can be estimated from the PSDR of the ADC, which can be obtained from Fig. 2.14 as follows.

First, b, given in LSB/dec, can be expressed as

$$b = b_0 \cdot G_{\mathrm{ADC}}, \tag{2.27}$$

where b_0 is the slope of the logarithmic sensor's DC response (in $\mathrm{V/dec}$), which can be found with the assistance of Fig. 2.3, while G_{ADC} is the gain of the $\Delta\Sigma$ ADC (in $\mathrm{LSB/V}$), which can be determined with the assistance of Fig. 2.14.

In addition, σ_ϵ due to the entire DPS can be approximated to its value due to the ADC, which can be found using the input/output response of the ADC shown in Fig. 2.14. This way, the calculated PSDR of the DPS represents the maximum PSNDR of the DPS that could be achieved. Parameters used for the estimation of the PSNDR of the DPS are shown in Table 2.8.

The DR is the difference in decibels between the highest, bright limit (BL), and lowest, DL, stimuli that can be detected at which the SNDR exceeds $0\,\mathrm{dB}$. The DL of the $\Delta\Sigma$ DPS can be estimated using (2.25) and the calculated PSNDR. The BL can be determined with the assistance of Fig. 2.3 by finding the largest non-saturating current for each logarithmic sensor within the ADC range, shown in Fig. 2.14. Parameters used for the estimation of the DR of the DPS are shown in Table 2.8. Also, Table 2.9 summarizes the calculated values for PSNDR and DR of the $\Delta\Sigma$ DPS designs for the three technology nodes used in this chapter.

From Table 2.9 we can conclude that performance parameters such as DR, PSNDR, and frame rate are at least comparable to the baselines shown in Table 2.1, in most cases. The DR of the $180\,\mathrm{nm}$ design needs to be improved by $5\,\mathrm{dB}$. Thus, a way to increase this value is

addressed in Section 2.4.3. Also, reported pitch values are explained in the following section.

2.4.2 Layout

A full-custom layout is desirable because it can be optimized for area as much as possible, which is not the case for automatically-generated layouts or even semi-custom layouts made from standard cells [60]. Also, a hierarchical layout creation is preferred over a flat one because it is easier to debug and, most importantly, because it enables reuse of sub-blocks to form major blocks and facilitates scaling. In order to plan and create the layout of the $\Delta\Sigma$ DPS, a combination between top-down and bottom-up organization was used.

The top-down organization was necessary to properly place the different cells and determine the way they will interact, spatially and functionally, between each other in the layout. For this, it is assumed that the photodiode is placed in its own tier, which from now on will be called the bottom tier, while the rest of the $\Delta\Sigma$ DPS, including the three transistors that are part of the logarithmic sensor and the readout circuitry, are placed in a different one, which from now on will be called the top tier.

This section concerns the layout of the top tier for each technology node, shown in Fig. 2.15, which represents the highest hierarchy, while the completion of the layout of each sub-block represents the lowest hierarchy. In order to successfully complete the highest hierarchy layout, placement of inputs and outputs of sub-blocks, prior to low-hierarchy layout, became necessary.

Fig. 2.16 shows the floorplan followed to create the layouts of the top tier, for each of the technology nodes used in this chapter, indicating main inputs, outputs, and main blocks that form it. Each floorplan offers the smallest area usage conceived for the $\Delta\Sigma$ DPS in that particular technology node.

Table 2.8: Parameters for PSNDR and DR of the DPS designs. Using these model parameters of the logarithmic sensor, the ADC, and the entire DPS, characterization of the $\Delta\Sigma$ DPS for three technology nodes is possible.

Parameter	180 nm	130 nm	65 nm
b_0 (V/dec)	0.054	0.060	0.060
G_{ADC} (LSB/V)	51.3	145.2	51.1
b (LSB/dec)	2.77	8.71	3.07
c (A)	5.30×10^{-14}	1.11×10^{-11}	1.92×10^{-10}
σ_ϵ (LSB)	0.019	0.0069	0.020
x_{BL} (A)	9×10^{-8}	10^{-6}	10^{-5}

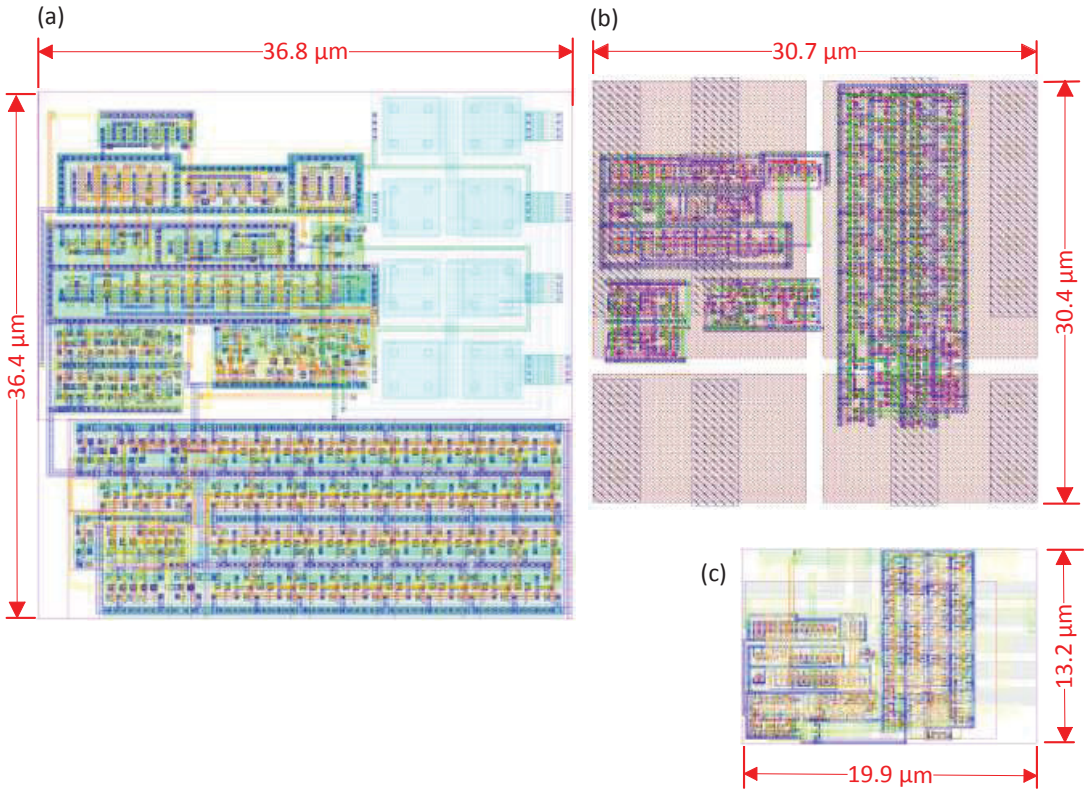


Figure 2.15: Top-tier layouts of the ΔΣ DPS. Layouts for (a) 180, (b) 130, and (c) 65 nm technology nodes.

Because it is expected that top and bottom tiers have the same area, we can safely state that the ΔΣ DPS area, A_{DPS}, can be calculated as the area of the top tier. The area calculation depends on the dominant blocks within the DPS. For instance, in the 180 design, A_{DPS} can be expressed by products of the sums of heights and widths, as shown in Fig. 2.16(a). This is due to the fact that all blocks are laid out side by side, each one contributing to the total area.

In the 130 nm design case, there are thin and thick (higher) metal layers. The thin ones were used for interconnections while the thick ones were left for dedicated devices, such as

Table 2.9: Characterization parameters for the ΔΣ DPS. DR and PSNDR values are calculated from simulation results for a fixed frame rate. Also, the measured pixel pitch is reported.

Parameter	180 nm	130 nm	65 nm
DR ($\geq$ dB)	121	154	131
PSNDR ($\leq$ dB)	36	55	36
Frame Rate (Hz)	30	30	30
Pitch (µm)	36.8	30.7	19.9

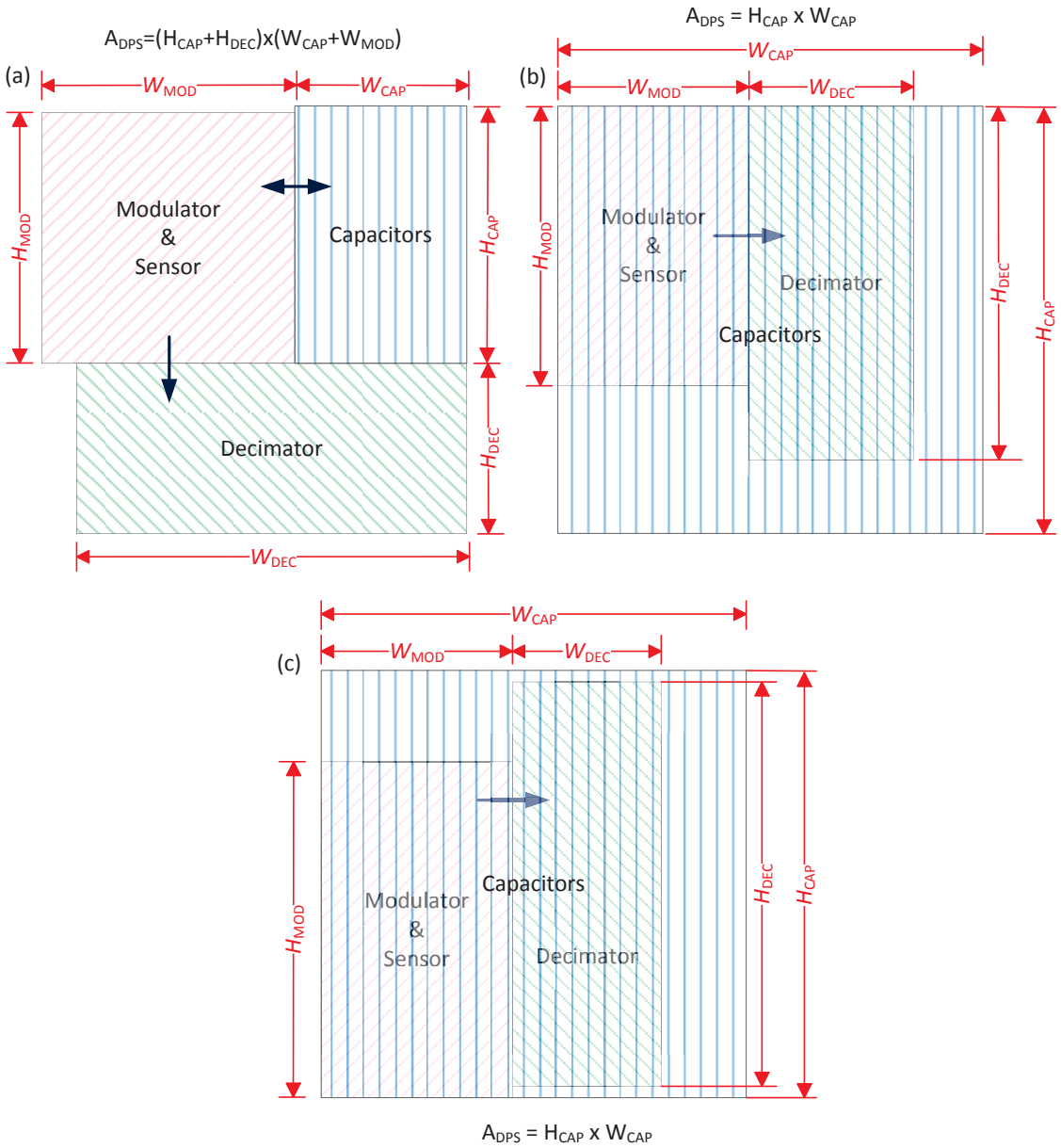


Figure 2.16: Floorplan of the $\Delta\Sigma$ DPS designs. Floorplan for (a) 180, (b) 130, and (c) 65 nm technology nodes, showing the distribution of the blocks in each technology node.

Table 2.10: Layout parameters of the DPS designs in three processes. Height, H, and width, W, parameters are used to calculate the DPS area of each design. Relative area, A, is given to show the area occupied by the block itself compared to the area of the DPS, A_{DPS}, in a given technology.

Parameters	$180\,\mathrm{nm}$	$130\,\mathrm{nm}$	$65\,\mathrm{nm}$
H_{MOD} (μm)	21.4	20.2	9.9
H_{DEC} (μm)	13.7	24.9	13.0
H_{CAP} (μm)	22.7	30.4	13.2
W_{MOD} (μm)	22.4	15.9	9.3
W_{DEC} (μm)	34.8	9.1	6.5
W_{CAP} (μm)	14.4	30.7	19.9
A_{MOD} (%)	36	34	35
A_{DEC} (%)	36	24	32
A_{CAP} (%)	24	100	100
A_{DPS} (μm^2)	36.4×36.8	30.4×30.7	13.2×19.9

capacitors. This was done to allow the capacitors to be placed on top of other devices. Because of this differentiation, there are fewer metals for interconnections, compared to the $180\,\mathrm{nm}$ node. This would increase the layout area of certain blocks that required more metals in the $180\,\mathrm{nm}$ node, more specifically, the layout area of the modulator block (without capacitors).

As shown in Fig. 2.16(b) and Table 2.10, the total area of the $130\,\mathrm{nm}$ $\Delta\Sigma$ DPS is dominated by the capacitors, *i.e.*, the DPS area is given by the capacitor area, $H_{\mathrm{CAP}} \times W_{\mathrm{CAP}}$. Therefore, the impact of fewer metal layers on the area of the modulator did not have an effect on the overall area of the DPS for that node, but instead enabled overall area reduction.

The $65\,\mathrm{nm}$ technology node, compared to the 180 and $130\,\mathrm{nm}$ nodes, has more metals available for interconnections. Therefore, capacitors, such as MIM capacitors, could be put on top of the other main blocks of the DPS without interfering with the devices below, thus saving area. As in the $130\,\mathrm{nm}$ node case, the capacitors dominate the pixel. Therefore, the DPS area is given by the capacitor area, $H_{\mathrm{CAP}} \times W_{\mathrm{CAP}}$, as shown in Fig. 2.16(c).

Table 2.10 shows the dimensions of each main block and how much area each one occupies compared to the top-level DPS area, A_{DPS}. It should be noted that the sum of the area contributions of each main block does not give 100%. This is because, from the top-level DPS perspective, main blocks may overlap. Interconnections between main blocks also contribute to the total area, as is the case for the $180\,\mathrm{nm}$ design. In the 130 and $65\,\mathrm{nm}$ designs, although modulator, decimator, and their interconnections occupy around 70% of the total area, they do not define the total area. The capacitors block occupies 100% of the total area.

With the assistance of Fig. 2.16 we can calculate the DPS total area for each technology

node. These values are also shown in Table 2.10. Compared to the $180\,\mathrm{nm}$ design, the 130 and $65\,\mathrm{nm}$ designs present a reduction of 30.3% and 80.4%, respectively, which is considerable. It should be noted that as the DPS circuit scales down, the modulator and decimator blocks shrink more considerably than the capacitors block, which could slow down the overall area reduction as smaller technology nodes are used.

2.4.3 Projections

In the previous subsections, verification and layout results for the $\Delta\Sigma$ DPS in three technology nodes were shown. These results are now used to develop a roadmap for the $\Delta\Sigma$ DPS technology and determine when it may become competitive with commercial DPS technologies for optical applications, such as Pixim's.

Specifications, shown in Table 2.1, can be compared against characterization values for the three technologies, shown in Table 2.9. As can be seen, the PSNDR is met at each node. In particular, the $130\,\mathrm{nm}$ design has a PSNDR that is well above the specified value. The DR values for the 130 and $65\,\mathrm{nm}$ designs surpass the specified target. However, the corresponding value for the $180\,\mathrm{nm}$ design is short by $5\,\mathrm{dB}$.

The calculated DR is affected by the input voltage range of the ADC. So, although the $180\,\mathrm{nm}$ sensor operates with currents up to $10\,\mu\mathrm{A}$ at $0.5\,\mathrm{V}$, as shown in Fig. 2.3, the maximum current allowed by the ADC, which corresponds to its minimum input voltage, is $90\,\mathrm{nA}$ at $0.65\,\mathrm{V}$. So, to improve the DR of the $180\,\mathrm{nm}$ design, the input voltage range of the $\Delta\Sigma$ ADC needs to be extended at its lower limit.

As explained in Section 1.2.1, the DPS design developed by the baseline, *i.e.*, Pixim, includes a MCBS ADC. This kind of ADC presents mostly analog components, which makes scaling to newer technology nodes more complex and less beneficial. The $\Delta\Sigma$ DPS architecture based on a $\Delta\Sigma$ ADC does not have this problem.

Also, speed is a major drawback of Pixim's architecture because a ramp is used to compare a sensed voltage, which represents the luminance at the pixel. This comparison is done multiple times, each time to determine one bit. Though the $\Delta\Sigma$ DPS architecture trades speed with bit resolution, overall it achieves a higher frame rate.

Because of its advantages over Pixim's approach, the $\Delta\Sigma$ DPS could be considered as competitive for commercial applications, provided the pixel pitch can be comparable to Pixim's, *i.e.*, $11\,\mu\mathrm{m}$, assuming that pixels do not share ADCs. As could have been concluded from the pixel pitch reported in Table 2.9, the $\Delta\Sigma$ DPS is still larger than the target baseline.

Fig. 2.17 shows the trend for pixel pitch of the $\Delta\Sigma$ DPS. Although it could be desirable to have more than three points to create a trendline, it is important to remember that each

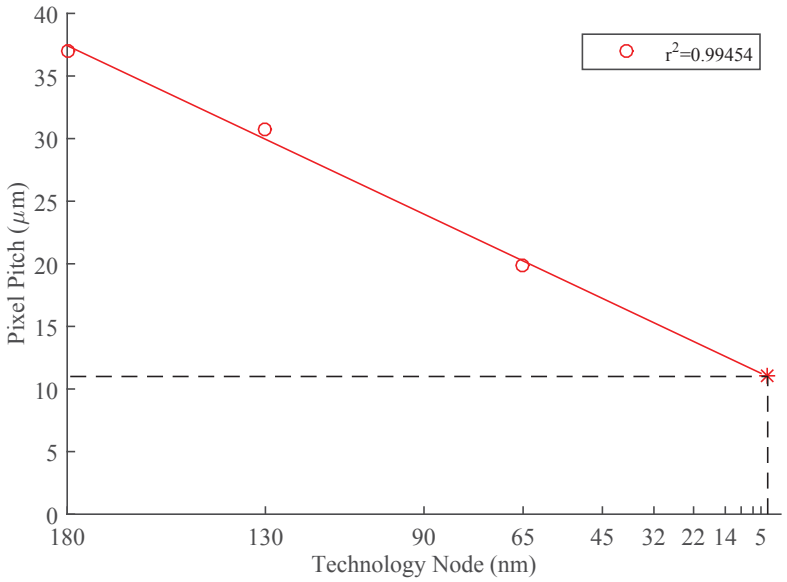


Figure 2.17: Pixel pitch versus technology node. Extrapolating from the 180, 130, and 65 nm layouts, by the 5 nm technology node a pixel pitch around 11 µm is expected, matching the baseline.

point was obtained by designing and laying out an entire DPS. Below 65 nm, the feature size reduction between one node and the next one decreases more slowly. This makes the scaling less and less beneficial under 14 nm.

Following the trendline shown in Fig. 2.17, using the 14 nm node we could expect a pixel pitch smaller than 13 µm. If we were to go further than 14 nm, scaling at 5 nm could match the baseline provided analog devices such as the capacitors do not slow down or even stop the scaling from reducing the pixel pitch.

2.5 Summary

This chapter presents a first-order $\Delta\Sigma$ DPS design developed for three different technology nodes, *i.e.*, 180, 130, and 65 nm. The $\Delta\Sigma$ DPS, based on Mahmoodi *et al.*'s work [2], is formed of a logarithmic sensor and a first-order $\Delta\Sigma$ ADC. The logarithmic sensor is a classic three-transistor (3T) circuit. The ADC is composed of a first-order $\Delta\Sigma$ modulator and a corresponding one-stage FIR decimator.

Full-custom layouts were done, assuming two-tier processes were available for each chosen technology node, where the photodiode could be placed in a different tier than the rest of the $\Delta\Sigma$ DPS. Each design was floorplanned to use the minimum area envisioned while, in most cases, fairly satisfying other performance parameters, such as DR and PSNDR.

The 130 and $65\,\mathrm{nm}$ designs meet, or even surpass, the target values for DR and PSNDR. However, the $180\,\mathrm{nm}$ DPS does not meet the DR specified by $5\,\mathrm{dB}$. In order to meet the DR specified, the minimum voltage allowed at the input of its ADC needs to be lowered.

While the power consumption of the $180\,\mathrm{nm}$ design is higher than the one reported by Mahmoodi [18], the 130 and $65\,\mathrm{nm}$ designs present lower total average power. A more power-conscious design flow is needed for nanometric nodes, *i.e.*, $65\,\mathrm{nm}$ and below, in order to mitigate the effects of static power in the overall power consumed by the circuit.

Finally, 80.4% area reduction was achieved for the $65\,\mathrm{nm}$ design, compared to the $180\,\mathrm{nm}$ design. Projections show that, relying on scaling and CAS improvements, the $11\,\mu\mathrm{m}$ pixel pitch can be achieved using a $5\,\mathrm{nm}$ process.

Chapter 3

Faster Rate Design

Current gamma image sensors present incompatible voltage sources between the photon capture stage (high voltage), done by an array of silicon photomultiplier (SiPM) detectors, and the digital conversion stage (low voltage), done by an external array of analog-to-digital converters (ADCs). However, compact and easy-to-manufacture gamma image sensors, with compatible voltage sources, are preferable for their practicality and lower cost.

Unlike some other invisible-band applications, gamma imaging allows the use of regular c-Si devices, *i.e.*, photodiodes, as detectors. Because photodiodes have lower signal than SiPMs, circuits that significantly reduce noise need to be included to maintain the signal-to-noise ratio (SNR). By taking advantage of the noise performance of the delta-sigma ($\Delta\Sigma$) digital pixel sensor (DPS) presented by Mahmoodi and Joseph [1], photodiodes can be used instead of SiPMs [30]. This means that, provided the $\Delta\Sigma$ DPS design could be adapted to meet other gamma imaging requirements, it could be considered over the current approach for gamma imaging.

Due to the high-in-energy low-in-number nature of the particles going through the imaging system, every photon reaching the imaging system at any time needs to be captured, so a high time resolution is needed. While optical imaging requires a minimum frame rate of $30\,\mathrm{fps}$ for video, the frame rate for gamma imaging is related to the decay time of the scintillator used, and could be on the order of M fps [27].

The faster rates required by gamma imaging need to be addressed without affecting the image sensor performance negatively. Therefore, higher-order $\Delta\Sigma$ ADC architectures need to be investigated. For this application, a second-order, rather than a first-order, modulator is explored. Furthermore, the $\Delta\Sigma$ DPS, which is the main component of an image sensor, uses a two-tier $130\,\mathrm{nm}$ process, *i.e.*, a $3\mathrm{D}$ integrated circuit (IC) process.

To this end, the initial design of a fully-integrated gamma image sensor is presented in this chapter. Subsequent sections provide details on the floorplan, architecture, and circuit design of

the image sensor. These details include circuit selection criteria, schematic diagrams, physical implementation attributes, and simulation results.

The circuit design depends on the requirements imposed by the application. Main gamma image sensor requirements are shown in Table 3.1. The most important requirement, however, is that ADCs are integrated with sensors at pixel level, on the same chip, to form a DPS array.

The specification for array size is based on the one adopted by Cubresa in its gamma camera, presented by Goertzen *et al.* [27]. Cubresa's camera is considered the baseline against which the performance of the proposed gamma camera can be evaluated. It uses an array of 4×4 pixels and it has proven to be sufficient for some commercial applications.

Another important specification is the frame rate of the gamma camera. This value depends on the duration of the pulse of light coming from the scintillator. This duration depends highly on the type of scintillator being used. Assuming we will be using the same scintillator used by Goertzen *et al.*, which has a reported decay constant of about $1\,\mu\mathrm{s}$ [27], we are choosing a frame rate of $1\,\mathrm{MHz}$ for this initial design.

The dynamic range (DR) should also be specified because it gives us an idea of the relationship between the largest and smallest signals that can be represented. This specification is reported by Cubresa under "number of bits," as the range reported is limited by the ADC used. It was converted to decibels for this work. Values vary between $48\,\mathrm{dB}$ (8 bits) [61] and $84\,\mathrm{dB}$ (14 bits) [27].

High fill factor, which affects sensitivity, is another requirement of the gamma camera. The fill factor is the ratio of the area of the pixel that collects light to the total pixel area. As it is clearly desirable, and proves essentially feasible, a fill factor of 100% is specified.

3.1 Floorplan and Architecture

Given that we would like to have an ADC in each pixel and at the same time have near 100% fill factor, a different approach from the typical planar IC technology needs to be used for the

Table 3.1: Specifications of the gamma image sensor. These values are comparable to the specifications reported in the literature for competing designs.

Parameter	Value
Array Size	4×4
Frame Rate (MHz)	1
DR (dB)	48–84
Fill Factor ($\%$)	100

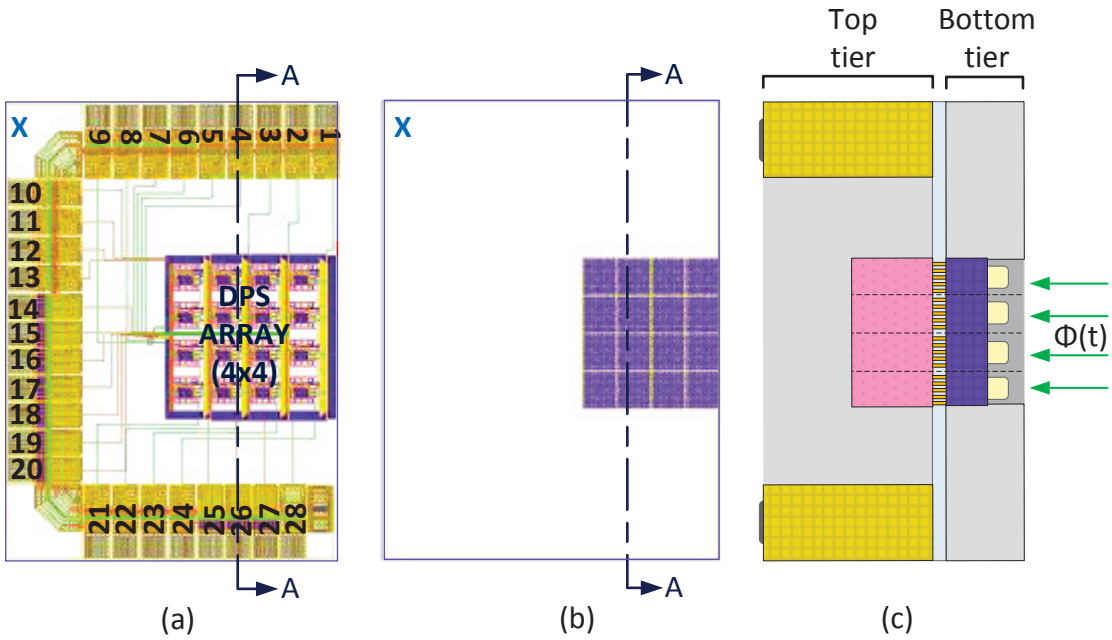


Figure 3.1: Floorplan of the gamma image sensor. (a) Top tier, (b) bottom tier, and (c) both tiers (cross section) of the initial IC design for a two-tier Tezzaron 130 nm CMOS process. The back side of the bottom tier faces the illumination.

gamma image sensor. It is for this reason that the Tezzaron 3D IC technology was selected [62]. It offers face-to-face wafer bonding of two tiers, each fabricated in 130 nm complementary metal-oxide-semiconductor (CMOS) technology. In one tier, called the *bottom* tier, we place the photodetectors. In the other one, called the *top* tier, we place the rest of the circuits required by the image sensor.

In the following sections, we first present the whole image sensor before giving an overview of each pixel. Finally, we discuss the operating modes of the chip, providing associated timing diagrams.

3.1.1 Image Sensor

Fig. 3.1 presents the layout of the image sensor. As can be seen, it comprises mainly bond pads and a DPS array. Interface circuits include an address decoder to select the DPS row that will be read out at a given time, one row at a time. A clock interface at chip level is used to provide clocks required by the ADC circuits at pixel level. Internal clocks are generated from external 64 and 800 MHz clocks.

Bond pads are used to connect the inputs and outputs of the DPS array to the outside world. These bond pads can be different depending on the type of signal to be carried. Digital input cells, which include input buffers, are used for pads 1 to 13. Analog cells, which include elec-

trostatic discharge (ESD) protection, are used for pads 14 to 20. Digital output cells, designed for high slew rate, are used for pads 21 to 24, while pads 25 to 28 use cells for analog supply, analog ground, digital supply, and digital ground, respectively. Corner and fill bond pads are also used. Although needed for completeness, they do not interface to the DPS array. Table 3.2 lists all bond pads.

Top and bottom tiers are connected through direct bond interfaces (DBIs), which are bond points between the top metals of each tier. These bond points are aligned for the connections to be done correctly. Because the bond pads are placed in the top tier, the bias voltage (*i.e.*, analog ground) of the photodiodes in the bottom tier are wired up from the top tier through bond points. Similarly, the photodiode outputs, which are the inputs for circuits in the top tier, are also wired up through bond points. For reliability purposes, multiple bond points are used for each connection.

Even though the initial design is done for a 4×4 DPS array, the floorplan is set up to enable a bigger DPS array through chip tiling. As only three of the chip's four sides have bond pads, the DPS array itself is placed at the edge of the fourth side. Furthermore, as shown in Fig. 3.1, the IC area is limited by the bond pads, not the 4×4 DPS array. Thus, a larger DPS array per chip is possible with no increment to the IC area.

3.1.2 Pixel Sensor

An image sensor is also an array of pixel sensors, in this case a DPS array. Fig. 3.2 shows the different blocks of one DPS and their position in the two-tier IC. Each DPS is composed of a photodiode that receives an optical signal, coming from a scintillator, and transforms it into an electrical signal, *i.e.*, a current. After a logarithmic current-to-voltage conversion, using a three-transistor (3T) circuit, the output voltage becomes the input voltage of an ADC, which functions to digitize the response. The final stage of the DPS is readout circuitry, which helps to make the digital response of the pixel available outside the chip.

A logarithmic sensor was chosen for several reasons. Most importantly, the Electronic Imaging Lab has the most experience working with logarithmic DPS arrays. But there are other reasons. Firstly, logarithmic sensors have higher DR compared to linear ones. Although linear sensors present higher SNR than logarithmic ones, the SNR of logarithmic sensors is high enough with a $\Delta\Sigma$ ADC in each pixel [2]. Secondly, logarithmic sensors work in continuous mode. This means that, unlike linear sensors, logarithmic sensors need not reset at the beginning of each frame. This is an important characteristic because, with gamma imaging, an event could happen while a linear sensor is being reset, given the high-speed requirements of the application.

Table 3.2: Bond pads of the gamma image sensor. Pad numbers correspond to Fig. 3.1. Bond pads are available for electrical connections on the back side of the top tier.

Pad	Pin name	Symbol	Type	Description
1	COEFF	$h[n]$	digital	coefficients for decimators
2	Reset_b	$\overline{reset}$	digital	reset for shift registers
3	SA	SA	digital	mode A selection for shift registers
4	Clk64M_1	Clk_{read1}	digital	first clock (64 MHz) for readout
5	Clk64M_2	Clk_{read2}	digital	second clock (64 MHz) for readout
6	Clk800M_1	Clk_{conv1}	digital	first clock (800 MHz) for conversion
7	Clk800M_2	Clk_{conv2}	digital	second clock (800 MHz) for conversion
8	Addr⟨1⟩	$Addr[1]$	digital	first row-selection bit for address decoder
9	Addr⟨0⟩	$Addr[0]$	digital	second row-selection bit for address decoder
10	Phi_1	ϕ_1	digital	first non-overlapping clock for modulators
11	Phi_1d	$\phi_{1\mathrm{d}}$	digital	first non-overlapping clock, delayed
12	Phi_2	ϕ_2	digital	second non-overlapping clock
13	Phi_2d	$\phi_{2\mathrm{d}}$	digital	second non-overlapping clock, delayed
14	Vbn	V_{bn}	bias	bias voltage for logarithmic sensors
15	Vcmi	V_{cmi}	bias	input common-mode voltage for OTAs
16	Vcmo	V_{cmo}	bias	output common-mode voltage for OTAs
17	Vmin	V_{min}	reference	low reference voltage for modulators
18	Vmax	V_{max}	reference	high reference voltage for modulators
19	Vb	V_{b}	bias	bias voltage for OTAs
20	Vb1	V_{b1}	bias	bias voltage for comparators
21	Data⟨0⟩	$Data[0]$	digital	serial output of first DPS column
22	Data⟨1⟩	$Data[1]$	digital	serial output of second DPS column
23	Data⟨2⟩	$Data[2]$	digital	serial output of third DPS column
24	Data⟨3⟩	$Data[3]$	digital	serial output of fourth DPS column
25	AVDD	V_{DD}	power	analog supply voltage
26	AVSS	V_{SS}	power	analog ground voltage
27	DVDD	V_{DD}	power	digital supply voltage
28	DVSS	V_{SS}	power	digital ground voltage

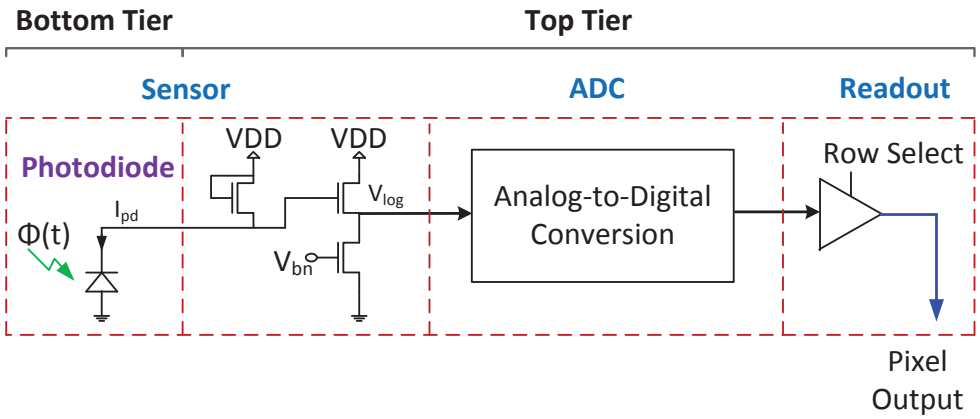


Figure 3.2: DPS architecture of the gamma image sensor. Each DPS comprises a logarithmic sensor, including a photodiode, an ADC, and readout circuitry. Apart from the photodiode, which is in the bottom tier, the rest of the DPS is in the top tier of the IC.

The photodiode, a part of the logarithmic sensor, is placed in the bottom tier, as mentioned earlier. Because top and bottom tiers are connected to each other through their top metal layers (face to face), as shown in Fig. 3.1(c), the resulting image sensor is of the back-illuminated type. As explained by Skorka and Joseph [3], the market for back-side illuminated CMOS image sensors is growing, while the traditional front-side illuminated approach is declining. So this is a competitive aspect of the approach.

A p-sub/n-well photodiode was chosen for the logarithmic sensor, to be consistent with the n-type 3T circuit. Photons are received through the p-substrate (anode) while the n-well (cathode) is connected to a diode-connected transistor, as shown in Fig. 3.2. As explained earlier, AVSS and I_{pd} are wired up to the top tier through DBIs. Transverse currents between neighboring photodiodes are not expected to be significant with logarithmic sensors.

Fig. 3.3 shows typical and corner DC responses of the logarithmic sensor. Each curve gives the output voltage for a given stimulus, represented by a photocurrent. The current range used in this simulation is expected to exceed those caused by luminances between the dark and bright limits of the DPS. The dark (bright) limit is the lowest (highest) luminance at which signal and noise power are the same [25].

These curves are important because from them we can calculate other parameters such as the minimum and maximum voltages possible at the output of each logarithmic sensor. This information is necessary for the design of the next stage, *i.e.*, the ADC. Moreover, it determines the value of voltage references applied to two pads (see Table 3.2) of the image sensor. Section 3.2 discusses the ADC, which is a $\Delta\Sigma$ ADC, in more detail.

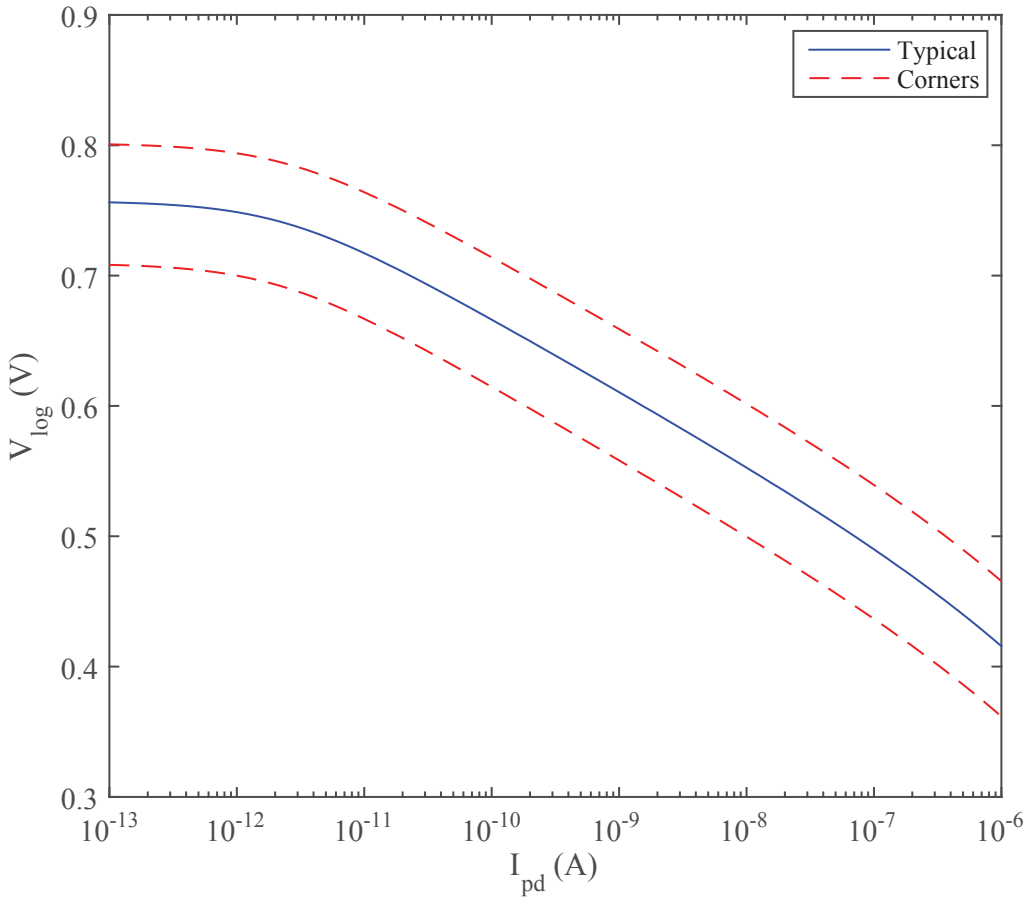


Figure 3.3: Simulated DC response of the logarithmic sensor. Typical and corner cases are given for the 3T circuit, including diode, shown in Fig. 3.2. To simulate photocurrent, a current source was placed in parallel with the reverse-biased diode.

3.1.3 Operating Modes

The gamma image sensor works in two modes of operation: conversion and readout. Circuits to support each mode are found in the ADC of each pixel, as explained in Section 3.2.

The image sensor's readout scheme is shown in Fig. 3.4(a). To limit the number of bond pads, bit-serial output was chosen. However, due to the relatively high frame rate, instead of outputting $256\,\mathrm{Mbps}$ (16 bits at $1\,\mathrm{MHz}$ for 16 pixels) on one serial output line, four serial output lines are used, one for each column. This reduces the bit rate to $64\,\mathrm{Mbps}$.

Conversion happens in parallel, for all 16 pixels in the gamma image sensor, within a $1\,\mu\mathrm{s}$ period, as shown in Fig. 3.4(b). After conversion, the data is available at the output of each pixel. All DPS outputs in the same column share a data line. When the address decoder selects one row, the output of the DPS in the selected row, for each one of the four columns, is placed on the data line, which is a one-bit output line.

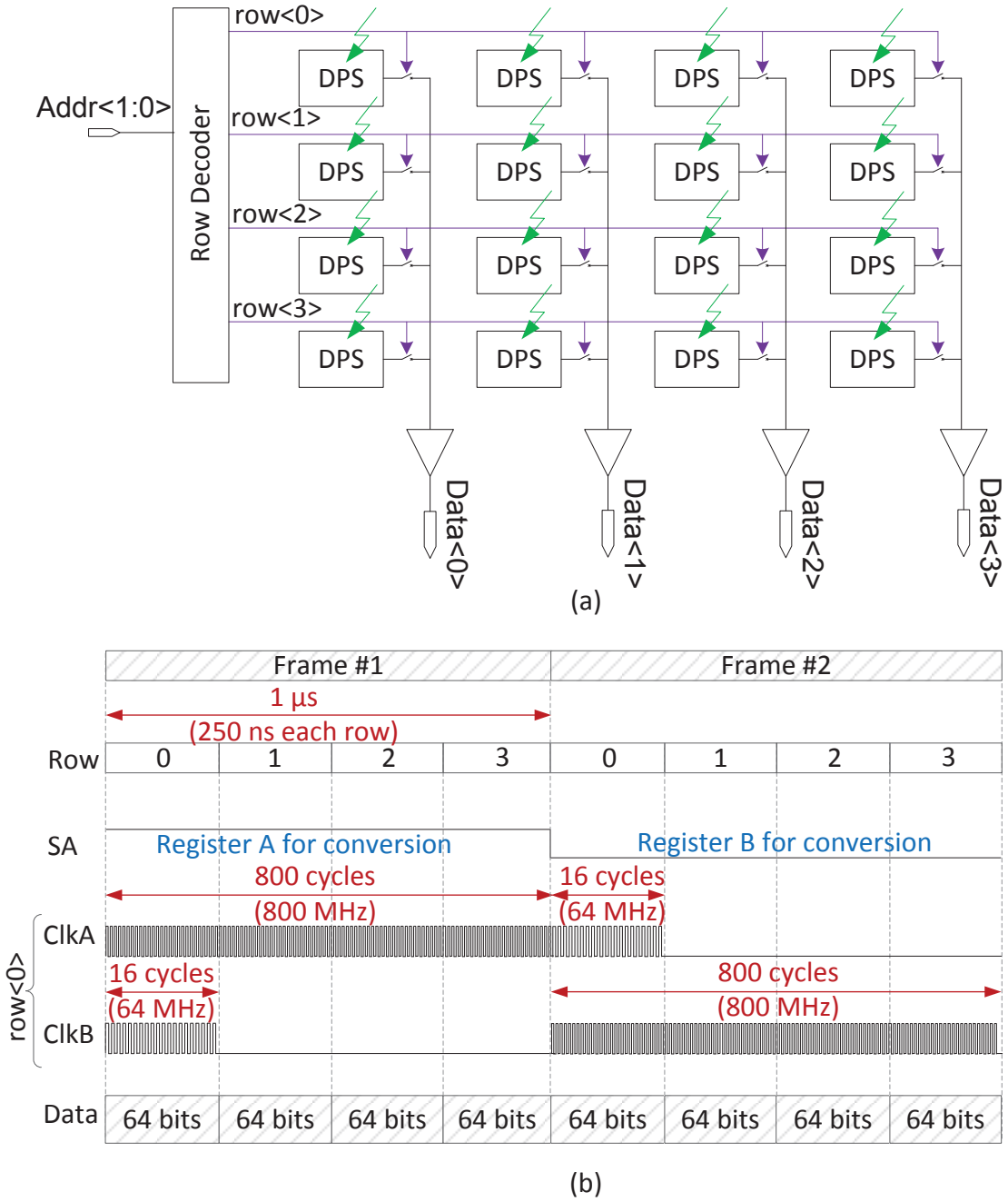


Figure 3.4: Conversion and readout modes. (a) Schematic and (b) timing diagram of operating modes. Conversion and readout happen at the same time, with the readout having a one-frame (1 µs) latency. Such performance is possible because each DPS has a ping-pong buffer, *i.e.*, two registers.

Readout happens in parallel for all four columns. Because each data line is shared by four rows, each row has to take turns to use the one-bit data line. A maximum latency of one frame period, as shown in Fig 3.4(b), is allowed for the digital conversion and readout of a complete frame. Each row is read out in one quarter of the frame period.

Because we are interested in not missing a gamma event, the gamma camera is sampling and converting, without interruption, the continuous-time signal that comes from the logarithmic sensor. In order to do this, the conversion of a frame and the readout of the previous one happens simultaneously. This means the ADC does not wait for readout of one frame before starting the conversion of the next frame.

The converted (digital) data is placed at the output of the pixel sensor to be read while the conversion of the next frame is happening. This is achieved by using a ping-pong buffer within the pixel, more specifically in the register that accumulates the final digital output of the ADC. The ping-pong buffer consists of two 16-bit data registers that we will call registers A and B. These registers will assist either the part of the DPS that is converting or the one that is reading the data out of the pixel.

The timing of the operating modes is illustrated in Fig. 3.4(b) for two consecutive frames. When high, the ping-pong status signal, SA, selects register A for conversion and register B for readout. When it is low, register B is selected for conversion and register A is selected for readout. This happens simultaneously across all rows of the DPS array.

As explained in Section 3.2 below, the required clock frequency for conversion is $800\,\mathrm{MHz}$, implemented by Clk_{conv1} and Clk_{conv2}. The required clock for column-parallel bit-serial readout is $64\,\mathrm{MHz}$, implemented by Clk_{read1} and Clk_{read2}. Thus, depending on the status of SA, the clocks of registers A and B change from one frame to another, a function performed by the clock interface at chip level. Because, in readout mode, each output line is only available one quarter of the frame time per row, the clock of the register performing readout is stopped three quarters of the frame time, using the row-selection signal. This reduces unnecessary switching, thereby decreasing power consumption.

3.2 ADC Schematics

The advantages of $\Delta\Sigma$ ADCs over other alternatives were described in Section 1.1.2. A $\Delta\Sigma$ ADC is composed of two parts: a modulator and a decimator. These parts will be explained in more detail in the next subsections. For the $\Delta\Sigma$ ADC to correctly fulfill its purpose, it is important to first compute its specifications based on the data in Table 3.1 and Fig. 3.3.

The specifications presented in Table 3.3 below correspond to the second-order modulator design. These specifications are reasonable values for the application. Optimizing the specifi-

cations was not a priority because the main objective of this project was the system integration.

In the sections below, procedures and choices are presented for the modulator and decimator circuits. Also, schematics for the main sub-blocks of each are provided.

3.2.1 Modulator

The main tasks of the modulator circuit are to oversample, noise shape, and quantize. The modulator oversamples the output produced by the logarithmic sensor in order to obtain better antialiasing, which is one of the advantages of oversampling ADCs over Nyquist-rate ones. Also, it uses feedback and integration to shape the noise to higher frequencies. Furthermore, it quantizes the noise-shaped signal to obtain a high-rate bit stream.

A second-order architecture was chosen over a first-order one because it offers a higher effective number of bits (ENOB) for a given oversampling ratio (OSR), M. Because of the high frame rate specification for the gamma image sensor (see Table 3.1), the OSR is limited by the maximum switching frequency allowed in the technology in use ($130\,\mathrm{nm}$ Tezzaron process in this work). Also, the second-order architecture is preferred over higher-order implementations because it offers a good compromise between circuit complexity and ENOB.

Fig. 3.5(a) shows the functional implementation of the $\Delta\Sigma$ modulator, which is implemented at schematic level as shown in Fig. 3.5(b). The modulator circuit is composed of two embedded digital-to-analog converters (DACs), two corresponding differencers, two integrators, and an embedded ADC. Each block is timed by clocks, coming from chip level, that are used only for conversion, which happens continuously. These clocks are ϕ_1, ϕ_2, and their delayed versions ($\phi_{1\mathrm{d}}$ and $\phi_{2\mathrm{d}}$).

The first embedded DAC and differencer (EDD) block has the output of the sensor as its input, so it has a single-ended input. To implement this sub-block we use an analog multiplexer, as shown in Fig. 2.5, found in Section 2.2.2. In order to exploit the advantages that a differential circuit offers, differential outputs are needed. Table 3.4 summarizes the operation of this sub-

Table 3.3: Specifications of the second-order $\Delta\Sigma$ ADC. Although they are not optimized, these specifications are calculated from the system requirements.

Parameter	Value
Input Voltage Range (V)	0.4
Nyquist Rate (MHz)	1
Oversampling Rate (MHz)	50
Register Size (bits)	16

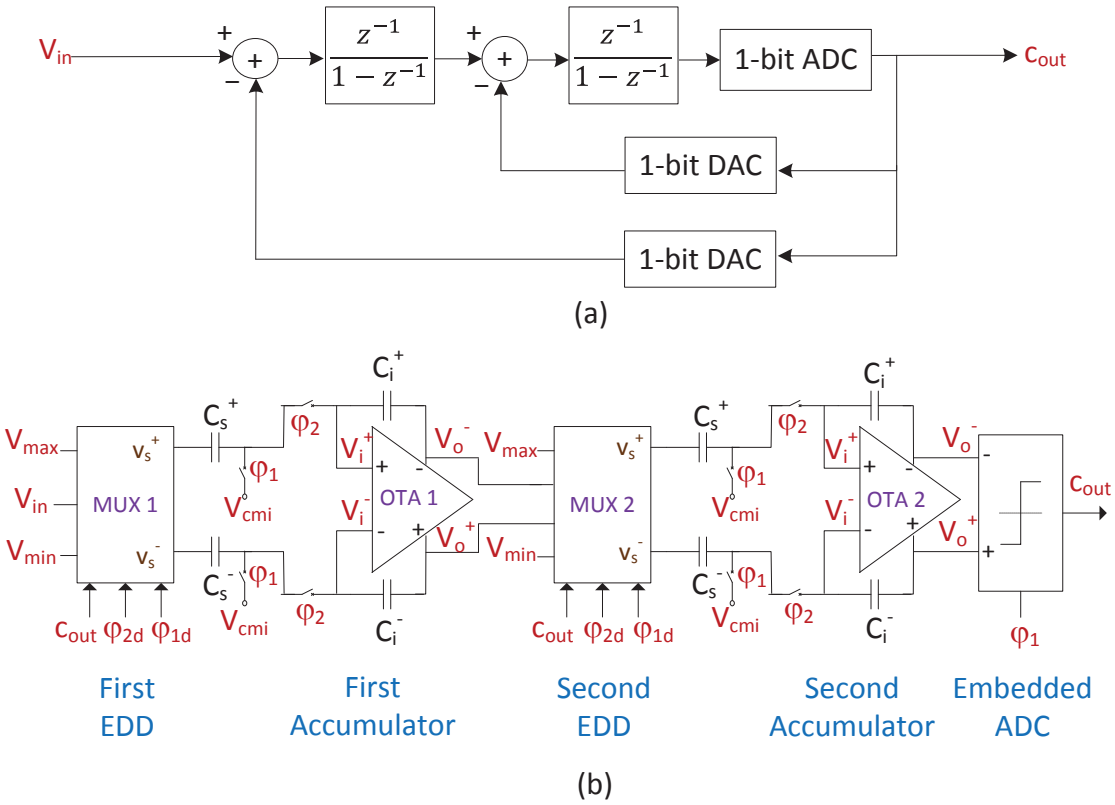


Figure 3.5: Diagram of the second-order modulator. Modulator diagrams showing (a) its functional structure, which is composed of two differencer (summation) blocks, two integrators, two one-bit DACs, and two one-bit ADCs, and (b) its switched-capacitor implementation, where differencer and DAC blocks are combined to form two EDD blocks.

block. Its main purpose is to pass an analog voltage (either $V_{\min}$, $V_{\max}$, or V_{in}) depending on the state of c_{out}, which is the output of the ADC sub-block inside the modulator. $V_{\min}$ and $V_{\max}$ are reference voltages, where $V_{\min} \leq V_{\text{in}} \leq V_{\max}$. V_{in} is both the output of the logarithmic sensor and the input of the second-order $\Delta\Sigma$ ADC.

The second EDD block has the output of the first integrator as its input, so it has differential inputs. As with the first EDD, differential outputs are needed. To implement this sub-block we use a fully differential analog multiplexer, as shown in Fig. 3.6. Table 3.4 summarizes its operation. It works similarly to the first EDD. The only difference is that instead of passing a single input, it passes a differential input.

While choosing a topology of the operational transconductance amplifier (OTA) to be used in a switched-capacitor circuit, speed is an important parameter to take into account given that it increases as the oversampling rate increases. Because the bandwidth of the OTA is directly related to the sampling frequency of the modulator, an OTA with high gain and most importantly large bandwidth is desirable.

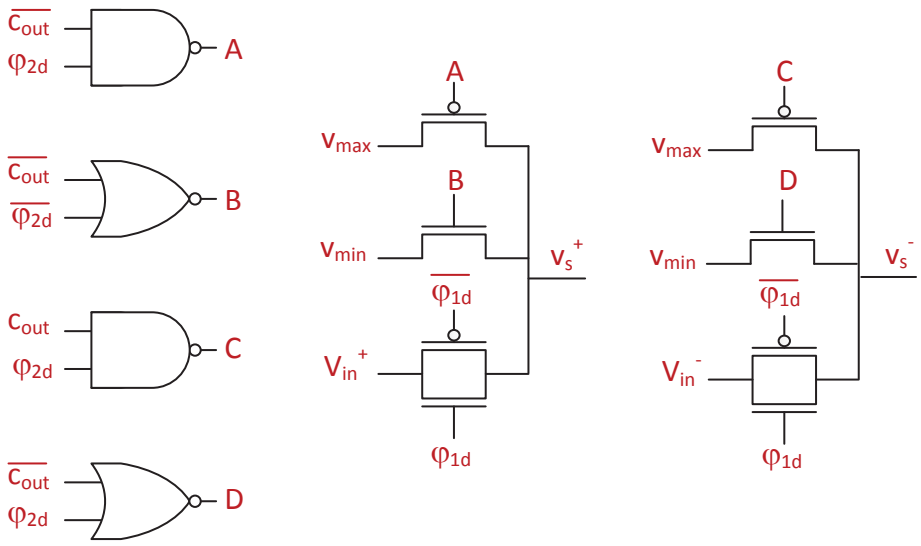


Figure 3.6: Schematic of the embedded DAC and differencer. A modified analog multiplexer is used to implement the second EDD sub-block.

Also, because settling time and slew rate requirements are very important for the correct functionality of the integrator, a fast response OTA is necessary for this application. For in-pixel ADCs, a one-stage OTA is preferable provided we obtain a high enough DC gain with a wide bandwidth. Also, since it will be driving capacitive loads, the chosen OTA should have a high output impedance. For these reasons, a folded-cascode OTA is used in the integrator sub-block.

Fig. 2.6, shown in Section 2.2.2, gives the schematic diagram of the OTA, which is also used in the integrator sub-block of the second-order modulator. As with the OTA designed in 2.2.2, the current through transistors P2 and P3, I_3, is assumed to be $1.5I_{\rm b}$. Also, the current through transistors N2, N3, N4, and N5, I_4, is assumed to be equal to $I_{\rm b}$. Currents that flow through P4 and P5, depend on the currents that flow through N8 and N9. Therefore, the output currents, $I_{\rm out}^+$ and $I_{\rm out}^-$, are controlled by the voltage difference of the inputs of the differential pair formed by transistors N8 and N9.

For the OTA described in this chapter, a common-mode feedback (CMFB) circuit was also added in order to set the common mode of the outputs to a controlled value. This is possible by converting the output voltage of the CMFB circuit to a current flowing through the transistor N7 to adjust the current flowing through the input branch.

Two integrators (technically, they are discrete-time accumulators) are needed in the second-order $\Delta\Sigma$ modulator. They each have the differential output of a multiplexer as their differential inputs. Since their outputs are also differential, each integrator is a fully-differential block that takes advantage of the superior power supply rejection ratio (PSRR) characteristic of this kind

Table 3.4: Truth table of the analog multiplexers. Depending on the state of c_{out}, $\phi_{2\mathrm{d}}$, and $\phi_{1\mathrm{d}}$, V_s^+ and V_s^- can be $V_{\min}$, $V_{\mathrm{in}}^{(+/-)}$, $V_{\max}$, or high impedance (Z).

			First EDD		Second EDD	
c_{out}	$\phi_{2\mathrm{d}}$	$\phi_{1\mathrm{d}}$	V_s^+	V_s^-	V_s^+	V_s^-
0	0	0	Z	Z	Z	Z
0	0	1	V_{in}	$V_{\min}$	V_{in}^+	V_{in}^-
0	1	0	$V_{\min}$	V_{in}	$V_{\max}$	$V_{\min}$
0	1	1	$-$	$-$	$-$	$-$
1	0	0	Z	Z	Z	Z
1	0	1	V_{in}	$V_{\max}$	V_{in}^+	V_{in}^-
1	1	0	$V_{\max}$	V_{in}	$V_{\min}$	$V_{\max}$
1	1	1	$-$	$-$	$-$	$-$

of circuit over the single-ended version.

The main purpose of each integrator is to sample and accumulate the outputs of the multiplexer in the previous stage. The sampling phase occurs when ϕ_1 is '1' (and ϕ_2 is '0'), while the accumulation occurs when ϕ_2 is '1' (and ϕ_1 is '0'). Over one Nyquist (1 µs) period, M samples are taken. The amount of time that the input is actually sampled is M times the time ϕ_1 is '1'. Because of this, tiny parts of events will be ignored if they happen in the time windows at which ϕ_1 is '0'. This issue could be alleviated by using a ping-pong sampling scheme, where the input is sampled while either ϕ_1 or ϕ_2 is '1'. By doing this, the amount of time the sampling clock is '0' is significantly reduced (non-overlapping time).

The output of the integrator sub-block can be expressed as follows:

$$V_{\mathrm{o}}[n+1] = \begin{cases} V_{\mathrm{o}}[n] + 2gV_{\mathrm{A}}[n], & c_{\mathrm{out}}[n] = 0, \\ V_{\mathrm{o}}[n] + 2gV_{\mathrm{B}}[n], & c_{\mathrm{out}}[n] = 1, \end{cases} \tag{3.1}$$

where

$$V_{\mathrm{o}}[n] = V_{\mathrm{o}}^+[n] - V_{\mathrm{o}}^-[n], \tag{3.2}$$

$$V_{\mathrm{A}}[n] = V_{\mathrm{in}}[n] - V_{\min}, \tag{3.3}$$

$$V_{\mathrm{B}}[n] = V_{\mathrm{in}}[n] - V_{\max}, \tag{3.4}$$

$$g = C_{\mathrm{s}}/C_{\mathrm{i}}, \tag{3.5}$$

and where the capacitor ratio in (3.5) is computed from

$$V_{\mathrm{o-PP}} = 4V_{\mathrm{in-PP}} \cdot g. \tag{3.6}$$

As in the case of the $\Delta\Sigma$ modulator for optical imaging shown in Section 2.2.2, the embedded ADC sub-block works as a two-level one-bit quantizer to get great tolerance to component matching. In the particular case of the second-order modulator, it takes the differential outputs of the second integrator as its inputs and compares them while ϕ_1 is asserted. It follows the behavior of a comparator, *i.e.*, the output, c_{out}, is '1' when V_o^+ is greater than V_o^-; otherwise, it is '0'. Fig. 2.7, which can be found in Section 2.2.2, gives the topology chosen to implement the comparator. While the integrator operates during each ϕ_2 pulse, the embedded ADC takes the differential outputs and compares them during each ϕ_1 pulse.

3.2.2 Decimator

The decimator circuit receives the bitstream generated by the second-order $\Delta\Sigma$ modulator, filters out-of-band components and quantization noise, and down-samples the filtered signal to the Nyquist rate. Several decimation methods exist in the literature. However, they are not meant for standalone ADCs, and although pixel area is not a concern for this application, all circuitry involved in the DPS should be able to fit within a reasonably small area.

For a given a modulator of order l, a decimator based on a comb filter of order $l+1$ offers a near-optimal response in terms of noise filtering. This means that for a second-order modulator, it is desirable to use a third-order comb filter. Here, the decimator patented by Mahmoodi and Joseph [26] is used instead. However, changes have been done to the patented design to further reduce area and introduce blocks to facilitate fast readout, as can be seen in Fig. 3.7.

Using a similar method for the calculation of the optimum decimator filter, shown in chapter 2.3.1, the denormalized coefficients of the decimation filter are as follows:

$$h[n] = \begin{cases} n^4 + an^3 + bn^2 + cn + d, & 0 \leq n \leq M-1, \\ 0, & \text{otherwise}, \end{cases} \tag{3.7}$$

where

$$a = -2(M-1), \tag{3.8}$$

$$b = M^2 - 5M - 1, \tag{3.9}$$

$$c = 3M^2 - M - 2, \tag{3.10}$$

$$d = 2M(M+1). \tag{3.11}$$

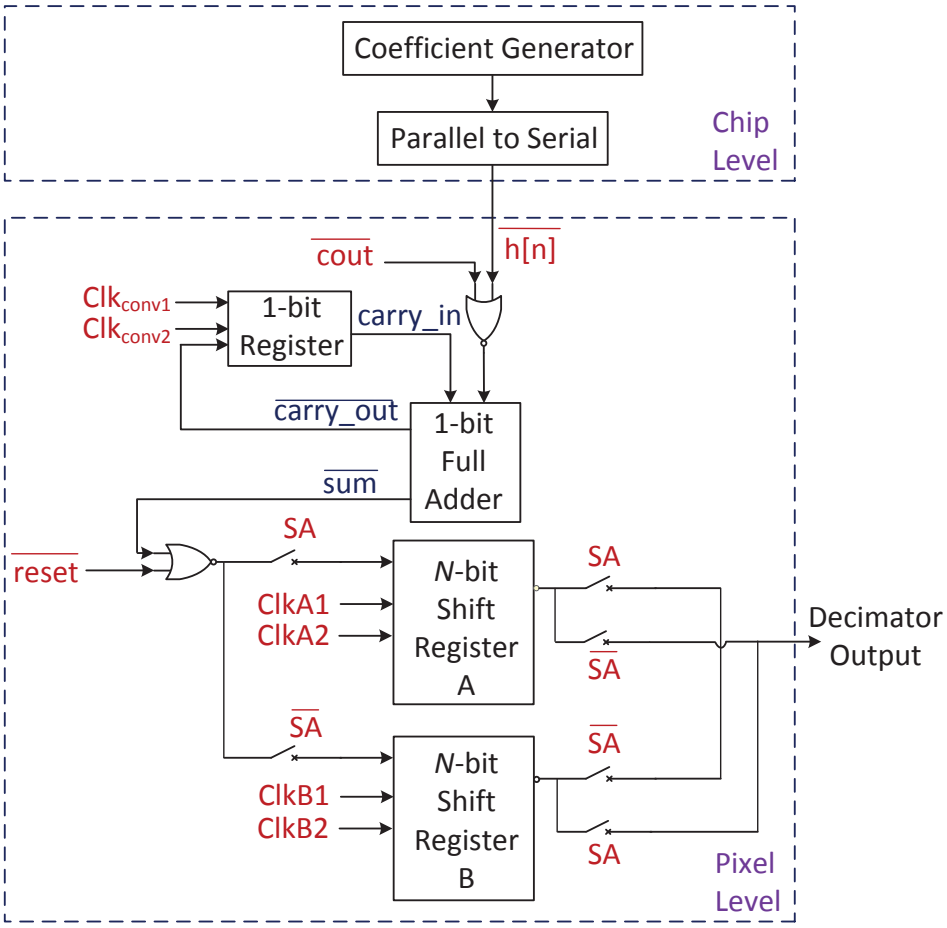


Figure 3.7: Schematic of the fast-rate decimator. It is composed of a bit-serial multiplier implemented by a NOR gate and a bit-serial accumulator implemented by a one-bit adder, a one-bit register, and an N-bit shift register. A second N-bit register (in parallel to the first one) is introduced to implement ping-pong buffering.

However, they are easier to calculate using the following recurrences:

$$h[n+1] = 4h[n] - 6h[n-1] + 4h[n-2] - h[n-3] + 24, \tag{3.12}$$

$$h[-3] = 2(M+3)(M+4), \tag{3.13}$$

$$h[-2] = 0, \tag{3.14}$$

$$h[-1] = 0, \tag{3.15}$$

$$h[0] = 2M(M+1). \tag{3.16}$$

Once $h[M-1]$ is computed and used, the decimation of one Nyquist interval is completed. The recurrence process is then re-initialized for the next Nyquist interval. Currently performed off-chip, (3.12) operates at $50\,\mathrm{MHz}$, the modulator frequency. However, because the coefficients

are fed bit-serially into the chip, and then bit-serially into all pixels, an off-chip parallel-to-serial converter, operating at $800\,\mathrm{MHz}$ for 16-bit coefficients, is also needed.

Because the application requires high-speed conversion and readout per frame, these two operations should happen in a pipelined fashion, *e.g.*, when the second frame is being converted, the first one is available at the output and so on. This way the DPS can be converting and reading data at the same time without "dead times". Modifications to the original circuit [26] were made in order to implement ping-pong buffering.

Three pairs of clocks are needed instead of one pair. Two of them are wired-up to the registers in the ping-pong buffer while the third one is connected to the 1-bit register exclusively involved in the conversion. The clocks for the registers A and B are controlled by a clock interface placed beside the DPS array, shown in Fig 3.1, that will provide the external clocks appropriately depending on the operating mode. One of the registers in the ping-pong buffer will be working on conversion while the other one will be working to read out the data from the previous frame.

In conversion mode, one of the registers (either A or B) works in a closed loop with the rest of the circuitry to obtain the final decimated value. This register stores intermediate values of the accumulation process. When the accumulation is complete, after the Mth coefficient has been multiplied to the output of the modulator, the control signal, SA, which comes from a global input, changes so now this register is used for readout, while the other one is used for conversion. The register responsible for readout is not used by the conversion loop. It provides the last frame's output of the decimator, ADC, and DPS. A timing diagram of the conversion mode is shown in Fig. 3.8.

3.3 Results

This section presents the results obtained in this chapter after designing a fully-integrated gamma image sensor in a Tezzaron 3D IC process. These results can be divided in two main parts: verification and layout. The verification part shows qualitative results, which assess the correct operation of the $\Delta\Sigma$ DPS, and quantitative results, which indicate whether the image sensor specifications were met. The layout gives us information about how the two-tier DPS would look.

3.3.1 Verification

Here, qualitative results to determine the correct operation of the $\Delta\Sigma$ DPS, which includes transient simulations of the second-order $\Delta\Sigma$ ADC, are shown. Also, simulations that deter-

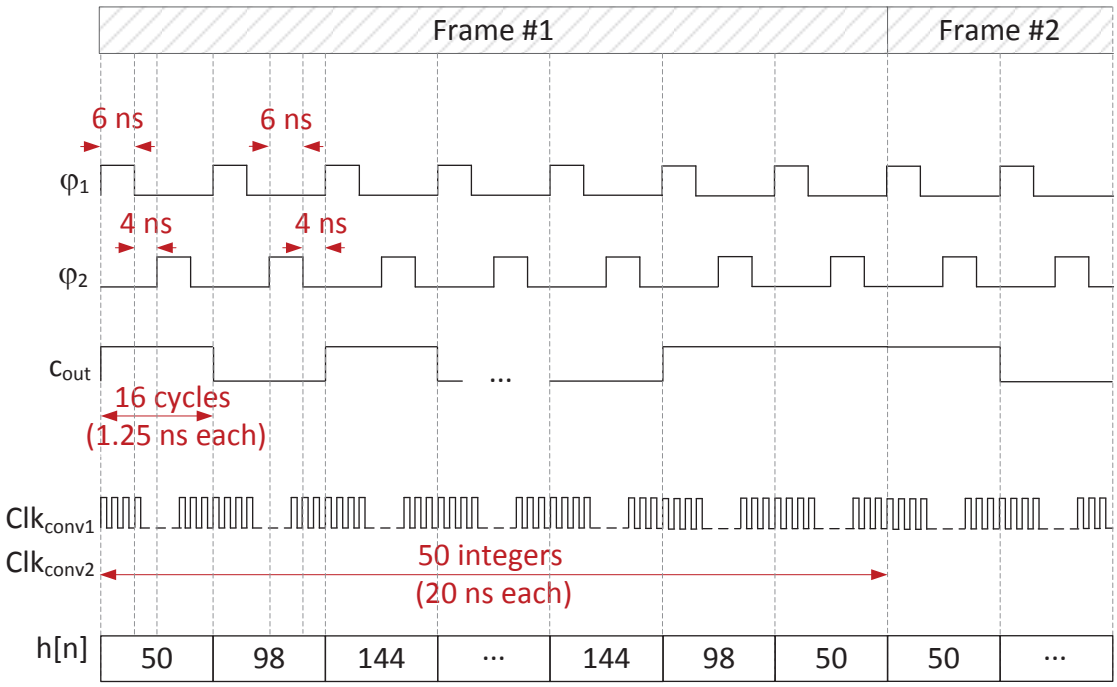


Figure 3.8: Timing diagram for conversion mode. The $50\,\mathrm{MHz}$ one-bit signal $c_{\mathrm{out}}[n]$, coming from the modulator, and 50 16-bit coefficients $h[n]$, coming from chip level, are convolved to generate the output of the ADC, which defines the output of the DPS.

mine the quantitative performance of the $\Delta\Sigma$ ADC, which is the *heart* of the $\Delta\Sigma$ DPS circuit, in terms of signal-to-distortion ratio (SDR) and DR are shown and used to characterize the entire DPS.

The modulator performance has great influence on the performance of the ADC and the image sensor in general. Because of it, simulations were conducted to verify the adequate operation of this block. Fig. 3.9 shows the transient simulation results for two frame periods. For simplicity, only ϕ_1 is shown in Fig. 3.9. However, there is another clock, ϕ_2, that does not overlap with ϕ_1. There are also two delayed versions of these clocks, $\phi_{1\mathrm{d}}$ and $\phi_{2\mathrm{d}}$. The testbench used has three different steady (DC) inputs that were set within the working voltage range of the ADC, which was 400 to $800\,\mathrm{mV}$ for this simulation. The minimum ($400\,\mathrm{mV}$), half-range ($600\,\mathrm{mV}$), and maximum ($800\,\mathrm{mV}$) inputs were selected.

Once the qualitative behavior of the most important part of the design is verified, it is necessary to characterize the design to evaluate its performance. Quantitatively speaking, one important parameter to evaluate the performance of the second-order $\Delta\Sigma$ ADC (and DPS) is its peak SDR (PSDR), which is a way to measure the quality of the data conversion. Fig. 3.10 shows the normalized ADC output for a given input that varies from $0.4\,\mathrm{V}$, the minimum value, to $0.8\,\mathrm{V}$, the maximum value.

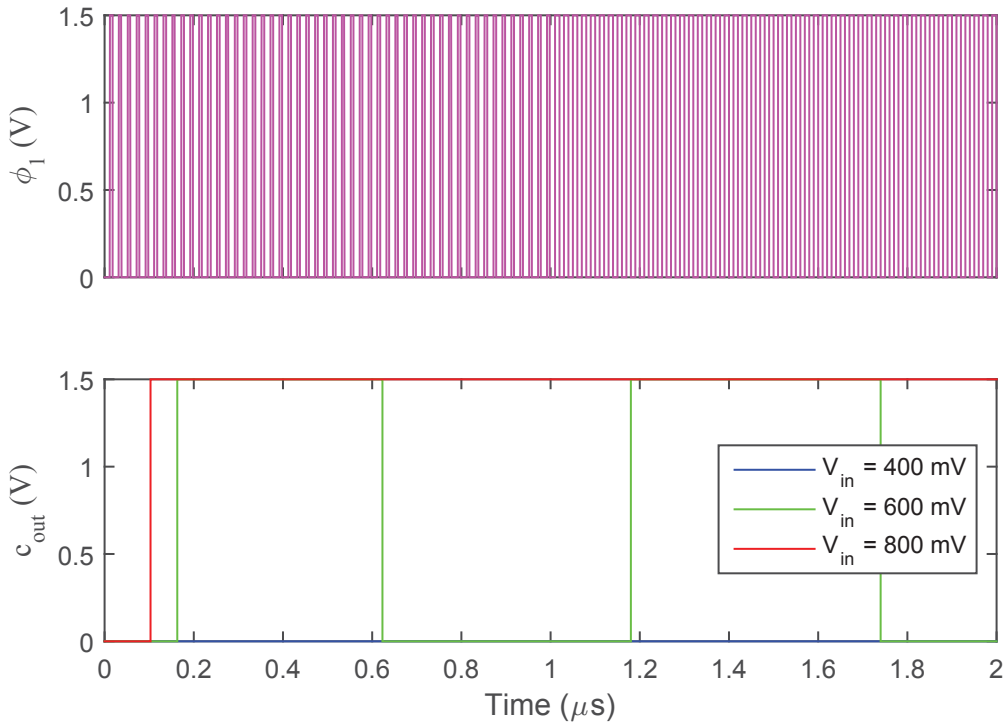


Figure 3.9: Transient simulation results. This simulation used the schematic view of the modulator and shows the modulator output, c_{out} for minimum, half-range, and maximum input values.

Fig. 3.10 was obtained by running multiple analog simulations of the modulator schematic and taking the output, c_{out}, to MATLAB to perform the decimation part of the ADC. Results of the decimation were normalized by the following value:

$$S = \sum_{n=0}^{M-1} h[n] = \frac{M(M+1)(M+2)(M+3)(M+4)}{30}. \tag{3.17}$$

This value, the sum of all filter coefficients, is the maximum possible output, before normalization, of the decimator, ADC, and DPS. After finding the best fit line, for the data in Fig. 3.10, using linear regression, the root mean square (RMS) value of the residual error is computed. This information is employed to calculate a PSDR of $29\,\text{dB}$ for the ADC.

Also, it is important to verify that the specifications for the image sensor, shown earlier in this Chapter in Table 3.1, have been met. In order to do so, parameters such as DR and fill factor are hand-calculated. The DR of the $\Delta\Sigma$ DPS is calculated using an estimated peak SNDR (PSNDR), as described below. The fill factor is calculated with the assistance of the layout of the image sensor.

As explained earlier in this chapter, the DR gives us an idea of the range between the

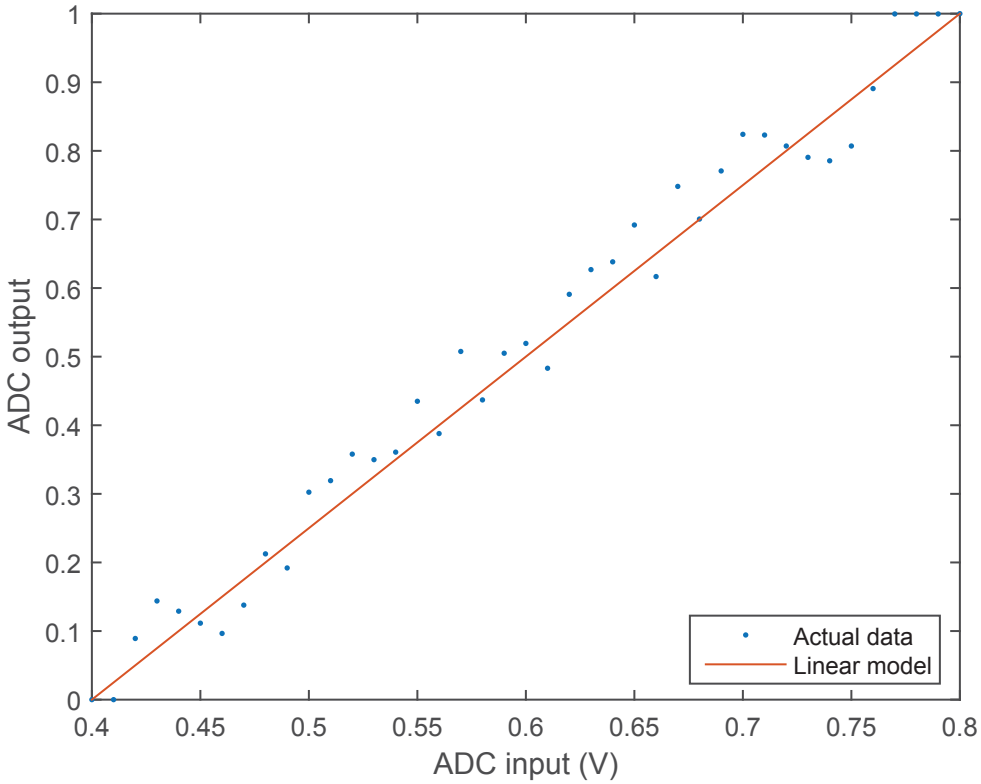


Figure 3.10: ADC simulation results. These results were obtained using parametric and transient simulations of the modulator schematic, while the decimation was done using MATLAB.

largest (bright limit (BL)) and smallest (dark limit (DL)) non-saturating signals that can be represented. A high DR indicates a wide range of detectable signals. The PSNDR, on the other hand, gives us an idea of the quality of the signal within the detectable range [8]. A high PSNDR indicates the precision of the detected signal.

To calculate the PSNDR of the $\Delta\Sigma$ DPS, a similar process used in Section 2.4.1 will be followed. Recalling, the PSNDR of the pixel can be expressed as

$$PSNDR = \frac{b}{\ln(10)\sigma_\epsilon}. \tag{3.18}$$

Here, b is the product of b_0 and G_{ADC}.

Also, b_0 is the slope of the logarithmic sensor's DC response (in $\mathrm{V/dec}$), which can be found with the assistance of Fig. 3.3. Meanwhile, G_{ADC} is the gain of the $\Delta\Sigma$ ADC (in $\mathrm{LSB/V}$), which can be determined with the assistance of Fig. 3.10.

As in Section 2.4.1, σ_ϵ due to the entire DPS can be approximated by its value due to the ADC, which can be found using the input/output response of the ADC shown in Fig. 3.10. So, the calculated PSDR of the DPS represents the maximum PSNDR of the DPS that could be

achieved.

In order to estimate the DR, the BL and DL need to be estimated first. Using the previously estimated PSNDR, the DL of the $\Delta\Sigma$ DPS can be calculated by

$$x_{\mathrm{DL}} = \frac{c}{PSNDR - 1}, \tag{3.19}$$

where c can be determined with the assistance of Fig. 3.3. The BL can be also determined with the assistance of Fig. 3.3 by finding the largest non-saturating current for the logarithmic sensor, which in this case is $0.36\,\mu\mathrm{A}$.

Parameters used for the estimation of the PSNDR of the DPS are shown in Table 3.5. The obtained PSNDR was $25\,\mathrm{dB}$, which is low compared to other DPS designs shown in this thesis. A low PSNDR translates into low precision for the computation of gamma photon energy. However, high energy resolution was not a specification given for this initial design.

Table 3.6 includes the value for DR of the $\Delta\Sigma$ DPS design used in this chapter. From Table 3.6 we can conclude that performance parameters such as array size, frame rate, and fill factor are comparable to the baselines shown in Table 3.1, while the DR specified was surpassed. Also, a fully-integrated image sensor was obtained.

3.3.2 Layout

The layout of both tiers of the initial DPS design was completed in accordance with what was explained in Section 3.1. This is shown in Fig. 3.11. The "x" in the top left corner is an alignment mark, as in Fig. 3.1, that indicates the way both tiers are supposed to be placed together. In the drawings prepared for chip fabrication, the top tier is mirrored because both tiers are assembled together, through their top metals, facing each other.

The bottom tier is composed entirely of the photodiode. The photodiode was meant to

Table 3.5: Parameters to calculate the PSNDR of the DPS. Using these model parameters of the logarithmic sensor, ADC, and the entire DPS, characterization of the $\Delta\Sigma$ DPS is possible.

Parameter	Value
b_0 (V/dec)	0.064
G_{ADC} (LSB/V)	28.18
b (LSB/dec)	1.80
c (A)	3.619×10^{-12}
σ_ϵ (LSB)	0.0423
x_{BL} (A)	3.6×10^{-7}

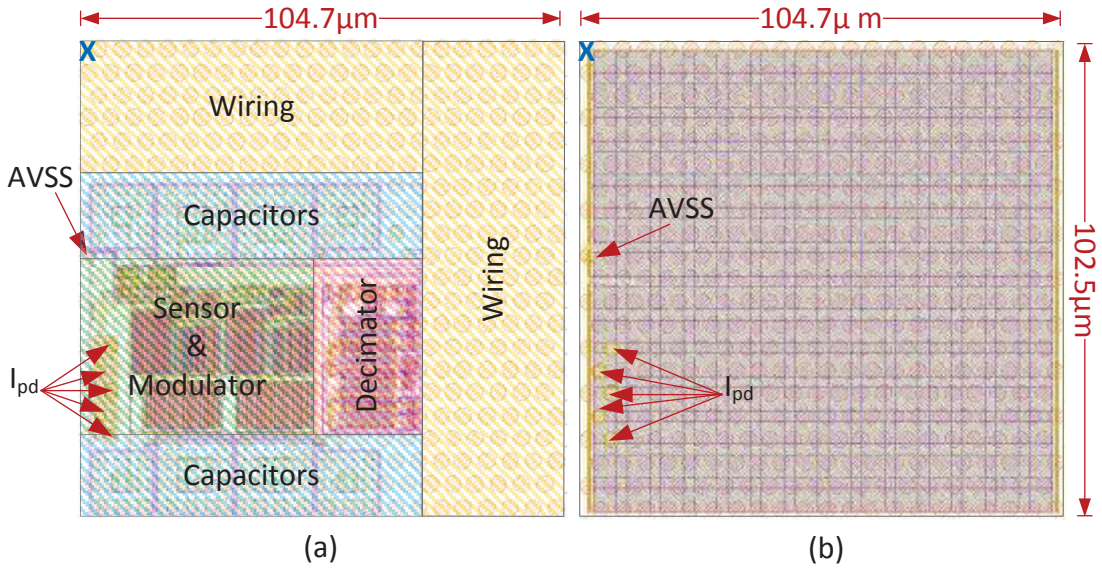


Figure 3.11: Two-tier layout of a DPS. Physical design showing: (a) the DPS in the top tier, including sensor & modulator, decimator, and capacitors, which represent 16.3, 6.5, and 22.8% of the pixel area; and (b) the photodiode, in the bottom tier.

occupy $100 \times 100\,\mu m^2$. However, the actual total area of the photodiode includes the space between photodiodes in a 4×4 array. Consequently, the photodiode area is $102.5 \times 104.7\,\mu m^2$ instead, making the fill factor slightly below 100%, *i.e.*, 93%.

The top tier contains all circuits and devices except the photodiode. These circuits have to be placed in such manner that they fit in the same area intended for the photodiode. Besides the designed circuits included in the DPS, plenty of space is allocated for local and global interconnections. The area occupied by the DPS circuits is $70 \times 70\,\mu m^2$, so, to match the area of the photodiode, the remaining area was used for the interconnections, for a total pixel area of $102.5 \times 104.7\,\mu m^2$.

The logarithmic sensor, excluding photodiode, and $\Delta\Sigma$ modulator, excluding capacitors,

Table 3.6: Characterization parameters for the image sensor. PSNDR is calculated from simulation results of the $\Delta\Sigma$ DPS for a fixed frame rate. Fill factor is calculated from the layout results of the bottom tier, which contains the photodiodes

Parameter	Value
Array Size	4×4
Frame Rate (MHz)	1
DR ($\geq$ dB)	125
Fill Factor (%)	93

occupy $35 \times 50\,\mu\mathrm{m}^2$, which represents 16.3% of the pixel area. This area includes the DBIs to and from the photodiode in the bottom tier. The $\Delta\Sigma$ decimator occupies $35 \times 20\,\mu\mathrm{m}^2$, which represents 6.5% of the pixel area. Finally, the eight capacitors used in the modulator occupy $35 \times 70\,\mu\mathrm{m}^2$, which represents 22.8% of the pixel area.

Shared signals between tiers, such as I_{pd} (internal interconnection) and AVSS (external pad) are connected through DBIs. These bond points have to be carefully placed in each tier of the design so they can be properly connected during the fabrication process. Because it is desirable that the shared connections are bonded at more than one point to ensure the connection, I_{pd} has five bond points. Though the same should have been done for the AVSS connection, there was enough space for only one bond point in this preliminary layout.

3.4 Summary

This chapter presented a novel gamma image sensor developed for the Tezzaron two-tier 3D IC process. The image sensor is formed of a DPS array with 4×4 pixels. The full layout was done for bottom and top tiers. The bottom tier contains an array of photodiodes while the top tier contains the rest of the circuits for conversion and readout, including bond pads. Both tiers are tied together using DBIs.

The DPS circuit is formed of a logarithmic sensor, a second-order $\Delta\Sigma$ ADC, and a simple column-parallel bit-serial readout scheme. The logarithmic sensor is a classic 3T circuit, whose input is photon flux and whose output is a voltage that is then digitized by the ADC. The ADC is composed of a second-order $\Delta\Sigma$ modulator and a corresponding one-stage finite-duration impulse response (FIR) decimator.

The modulator is designed for an OSR of 50. Its switched-capacitor circuit operates at $50\,\mathrm{MHz}$. The decimator, which reduces the sampling rate back to the Nyquist rate of $1\,\mathrm{MHz}$, includes a ping-pong buffer to implement the readout of frame i when conversion of the frame $i + 1$ is happening. Readout has a latency of one frame. The architecture, circuit schematics, and physical design for each of these blocks are explained in this chapter.

Results show that a DR of $125\,\mathrm{dB}$ was obtained for a fully-integrated gamma image sensor. The resultant pixel size was $102.5 \times 104.7\,\mu\mathrm{m}^2$, which is the size of the photodiode in the bottom tier. The ADC and readout circuits occupied $70 \times 70\,\mu\mathrm{m}^2$ of the pixel while the rest of the pixel area available, was used for interconnections.

Chapter 4

Conclusion

At present, complementary metal-oxide-semiconductor (CMOS) image sensors can be divided into three groups, *i.e.*, passive pixel sensor (PPS) architectures, active pixel sensor (APS) architectures, and digital pixel sensor (DPS) architectures, depending on the level at which the analog-to-digital conversion is implemented. Currently, APS architectures are the most accepted. By using a DPS architecture, noise reduction is achieved due to the elimination of analog noise at column and/or chip level.

There are several ways to implement an array of digital pixels. Researchers have investigated ways to perform analog-to-digital conversion taking advantage of photodetector properties. Even more, the inclusion of classical analog-to-digital converters (ADCs) at pixel level has also been investigated. Among them, delta-sigma ($\Delta\Sigma$) ADCs have appeared as a promising choice for low-to-medium speed pixel-level conversion.

Prior work related to $\Delta\Sigma$ DPS architectures mainly included only modulation at pixel level. Work done by Mahmoodi and Joseph [2], at the University of Alberta, introduced a true $\Delta\Sigma$ DPS architecture, which integrates a logarithmic sensor, a $\Delta\Sigma$ ADC with bit-serial decimation, and readout circuitry in each pixel. The logarithmic part of the circuit increased the dynamic range (DR) of the image sensor, while more effective noise reduction was performed by the $\Delta\Sigma$ ADC, which improves signal-to-noise ratio (SNR) due to its oversampling, noise shaping, and antialiasing operations. Therefore, the $\Delta\Sigma$ DPS architecture seemed to be a good alternative to the widely accepted linear APS for optical imaging, which suffers from low DR.

Though that particular $\Delta\Sigma$ DPS design was intended for optical imaging, its pixel pitch is above the value expected for that application, which could range from 1 to $8\,\mu\mathrm{m}$. Larger pixels are acceptable for gamma imaging and photodetection by c-Si devices is possible after scintillation, which could make the $\Delta\Sigma$ DPS a good candidate for this application. However, there are other requirements to consider such as the pulse-based nature of gamma imaging, which requires a high time resolution or frame rate. Therefore, provided the $\Delta\Sigma$ DPS design

could be adapted to meet these requirements, it can be considered for gamma imaging.

For optical imaging, a commercialized DPS developed by Pixim was used as a baseline for the $\Delta\Sigma$ DPS approach. The $\Delta\Sigma$ DPS is already competitive with Pixim's approach in terms of SNR and DR. However, its pixel size needs to be reduced to the order of Pixim's $11\,\mu\mathrm{m}$ pitch, assuming ADCs are not shared among neighboring pixels. For gamma imaging, the baseline is set by a handheld camera developed by Cubresa. In this case, the objective is to maintain the imaging performance while achieving a compact fully-integrated camera.

In order to reduce the pixel size to make it competitive for optical imaging, process scaling and simplified vertical integration were investigated. Also, a pixel pitch roadmap for the $\Delta\Sigma$ DPS technology was created by designing $\Delta\Sigma$ pixels for the 180, 130, and $65\,\mathrm{nm}$ technology nodes. The purpose of obtaining this roadmap was to have a better knowledge of whether it is possible for the $\Delta\Sigma$ DPS to achieve a pixel size within the desired range for optical imaging or, if it is not, to know how far from the baseline this technology stands, so further steps can be planned.

To integrate the photodetection and conversion parts of the gamma imaging system, while not degrading its performance, vertical integration was explored by using the two-tier Tezzaron $130\,\mathrm{nm}$ CMOS process. In one of the tiers, photodetectors were placed while, in the other one, all circuits involved in the photocurrent-to-digital conversion and digital readout can be found. To maintain its performance in terms of pulse detection and compensate for the noise that might be added to the system by avoiding high-voltage photodetectors, a second-order $\Delta\Sigma$ ADC was used instead of a first-order one.

In this chapter, the contributions, main conclusions, and maturation plan of this thesis are presented. Section 4.1 covers the main contributions of this thesis. Section 4.2 introduces the concept of technology readiness level (TRL) and assesses the TRLs for the optical and gamma imaging applications. Finally, Section 4.3 discusses ways to improve and extend the work presented here, based on the assessment performed in the previous section.

4.1 Contributions

The contributions of this thesis are highlighted in the following sections. Section 4.1.1 summarizes the specifications, design flow, layout and results of a small-area $\Delta\Sigma$ DPS for optical imaging. It also summarizes area trends of $\Delta\Sigma$ DPS designs done in three different processes, *i.e.*, 180, 130, and $65\,\mathrm{nm}$. Part of this work, related to the decimator in particular, was published in a proceeding [63] of the Society of Photo-Optical Instrumentation Engineers (SPIE). It was also presented at an SPIE conference.

Section 4.1.2 summarizes the initial design of a fully-integrated gamma image sensor that

includes an array of fast-rate $\Delta\Sigma$ DPSs. The gamma image sensor was developed for the Tezzaron two-tier 3D integrated circuit (IC) process. This work was included in a technical report [30] presented to Phantom Motion, a company that works with Cubresa, as one of the deliverables of a joint university-industry project.

4.1.1 Smaller Area Designs

Chapter 2 addressed the design of smaller $\Delta\Sigma$ DPS circuits based on Mahmoodi and Joseph's architecture [1]. The $\Delta\Sigma$ DPS performs several functions, each carried out by a different part, *i.e.*, sensing done by a detector and simple analog circuits, analog-to-digital conversion done by complex analog and complex digital circuits, and readout done by simple digital circuits. The conversion part includes digital storage. All these functions are performed at pixel level, while the goal for pixel pitch is a value less than or equal to $11\ \mu\mathrm{m}$. The digital circuits of the DPS benefit from Dennard's scaling theory in compliance to Moore's Law, while the detector and analog circuits do not, so not only scaling but also functional diversification, known as the dual trend in the semiconductor industry, were exploited to shrink the $\Delta\Sigma$ DPS.

As transistor dimensions shrink, process parameters, such as supply voltage and gate-oxide thickness, also decrease. This increases leakage current, which may become a significant issue in deep-submicron processes, and lead to higher-than-expected power consumption per pixel and, consequently, of a DPS array. Also, transistor parameters, such as transconductance and conductance, are expected to worsen for a given power (current) budget. Furthermore, the number of metal layers, types of capacitors, and minimum capacitances available vary from one technology to another, and affect how small the DPS could be made. All these technology considerations were taking into account to get a good performance-area trade-off when shrinking the $\Delta\Sigma$ DPS.

The $\Delta\Sigma$ DPS is formed by a logarithmic sensor, a first-order $\Delta\Sigma$ ADC (modulator and decimator), and a readout circuit. The logarithmic sensor transforms optical flux to a voltage signal and enables the wide DR of the image sensor. The first-order $\Delta\Sigma$ ADC converts the voltage signal into a digital signal, and in doing so enables the high peak SNDR (PSNDR) of the image sensor. Finally, the readout circuit allows the digital signal to be efficiently transported outside the image sensor and in doing so impacts the maximum frame rate achievable.

The logarithmic sensor was designed so that its optical requirements have minimal impact on pixel area. This is possible by using a two-tier process, where the photodiode is placed in one tier, while the rest of the logarithmic sensor, the $\Delta\Sigma$ ADC, and the readout are placed in the other tier. Although all designed circuits were, in practice, simulated and laid out for a one-tier process, with the photodiode simply omitted, conclusions that were drawn are expected

to apply also to two-tier processes at similar technology nodes. This is because, in practice, two-tier processes entail post-processing of fabricated one-tier wafers.

The modulator was composed of an embedded DAC and differencer (EDD), an accumulator, and a 1-bit ADC. The EDD efficiently integrates a 1-bit digital-to-analog converter (DAC) and a differencer. Special attention was given to the accumulator because, besides including more transistors than the other blocks, it is the only analog block of the modulator and it involves area-consuming capacitors. All of this makes it, a switched-capacitor circuit with an operational transconductance amplifier (OTA), the dominant modulator block in terms of area and performance.

The decimator was based on the bit-serial circuit invented by Mahmoodi and Joseph [26]. Each decimator in the array of $\Delta\Sigma$ pixels implements an finite-duration impulse response (FIR) parabolic filter, which offers optimal noise filtering for a first-order modulator, using serial coefficients generated at chip level or off-chip. This decimator uses less area than other decimators, such as comb filters, found in the literature. Some improvements were made to the original circuit to further reduce its number of transistors.

The readout circuit ensures the converted data is available off-chip. The circuit presented by Mahmoodi *et al.* [2] had two main problems: it did not use power efficiently; and frame rate (or maximum number of pixels in an array) was limited by readout time, which was comparable to conversion time. Conversion and readout are done sequentially. The first issue was solved by disabling the shifting of all unaddressed shift registers when in readout mode. The second issue was solved by proposing a double buffer for each column, so the readout time is reduced from depending on the number of pixels to depending on the number of rows. Although this thesis does not concern an *array* of pixels for optical imaging, the DPS circuit design depends on these array-level considerations. The total area of the decimator and readout, *i.e.*, the all-digital parts of the $\Delta\Sigma$ DPS, mainly depends on the number of bits in the accumulator. Therefore, a method was devised to efficiently design and lay out this block, in particular.

The $\Delta\Sigma$ DPS designs were verified qualitatively and quantitatively. Transient simulations were performed, as well as AC/DC and performance simulations, especially of the blocks that have more influence on the overall performance, such as the OTA and, in general, the modulator. Also, average power consumption was verified for the designs in all three processes. Furthermore, the DR and peak SDR (PSDR) characteristics of the three in-pixel $\Delta\Sigma$ DPS designs were obtained, where the latter affects the PSNDR of the image sensor.

Finally, three full-custom layouts were made, each for the technology nodes encompassed in Chapter 2, *i.e.*, 180, 130, and $65\,\mathrm{nm}$. The pixel pitches obtained were 36.8, 30.7, and $19.9\,\mu\mathrm{m}$, respectively. Compared to the $180\,\mathrm{nm}$ design, the pixel layout area was reduced by 80.4% with the $65\,\mathrm{nm}$ technology node. The three data points that were realized, one for

each technology node, form approximately a straight trendline. Extrapolating, we can predict that the target $11\,\mu\mathrm{m}$ pitch would be reached by the $5\,\mathrm{nm}$ technology node.

4.1.2 Faster Rate Design

Chapter 3 addressed the design of a fully-integrated gamma image sensor, based on faster pixel-level $\Delta\Sigma$ ADCs, intended for a compact gamma camera. This was done as an alternative to conventional gamma cameras, which are composed of many more parts designed for independent fabrication. None of these parts, *i.e.*, scintillator, photodetector (photomultiplier) array, and ADC array, can be easily integrated, based on current designs, due to manufacturability and compatibility reasons.

In particular, integration of photodetection and analog-to-digital conversion stages is not currently done because photodetectors, such as silicon photomultipliers (SiPMs), require voltages that are well above the maximum allowed by standard CMOS technology, which is ideal for ADCs. One possibility is to employ a non-standard CMOS process that supports higher voltages to integrate both parts. However, Chapter 3 addressed the use of standard CMOS photodetectors, *i.e.*, photodiodes, with low-noise $\Delta\Sigma$ ADCs [2], so high-signal SiPMs are not needed.

To meet the integration requirement of the application, the two-tier $130\,\mathrm{nm}$ Tezzaron process was used. This allowed vertical integration of the photodetectors with the rest of the image sensor. In one tier, called the *bottom* tier, the c-Si photodiodes were placed while, in the *top* tier, the rest of the circuits required by the image sensor, including bond pads, were placed. Both tiers were connected face-to-face by their top metals through direct bond interfaces (DBIs), forming a 3D IC image sensor where the back of one tier faces the illumination.

To meet the high-speed requirement, a logarithmic sensor along with a second-order $\Delta\Sigma$ ADC was used. Logarithmic sensors work in continuous mode, so no reset is needed at the beginning of each frame, which is important given the high-speed requirements of the application. However, on their own, logarithmic sensors present higher DR but lower SNR compared to linear sensors. The SNR problem is solved by integrating a logarithmic sensor with a $\Delta\Sigma$ ADC at pixel level. A second-order $\Delta\Sigma$ ADC enables a fast enough modulator that also has sufficient SNR, restrictions that are difficult or impossible to achieve with a first-order modulator.

Because speed was a priority for gamma imaging, conversion and readout happen at the same time, with the readout having a one-frame latency, in contrast to the optical imaging case, where conversion and readout happen sequentially. This was possible by including a ping-pong buffer in each DPS, *i.e.*, at pixel level. As a result, conversion happens, in parallel for all pixels,

while readout happens, in parallel for all columns, simultaneously.

The second-order modulator was composed of two EDDs made out of two multiplexers, two accumulators made out of two switched-capacitor integrators, and one 1-bit ADC made out of a clocked comparator. Special attention was given to both accumulators, each one including a fast-response wide-bandwidth OTA, because their correct operation greatly affects the performance of the entire ADC, and hence the image sensor.

The decimator, as in the optical imaging case, was based on the bit-serial circuit invented by Mahmoodi and Joseph [26]. It was designed from a bit-serial multiplier, implemented by a NOR gate, and a bit-serial accumulator, implemented by a 1-bit adder, a 1-bit register, and an N-bit shift register. Some improvements were done to the original circuit to allow simultaneous conversion and readout. That is, a second N-bit register was included in the pixel to implement ping-pong buffering. Though serial coefficients also come from outside the pixel array, as with optical imaging, these are different coefficients, specifically calculated for the second-order modulator.

The $\Delta\Sigma$ DPS for gamma imaging was verified qualitatively and quantitatively. Transient simulations were performed, as well as AC/DC and performance simulations, especially of the blocks that have more influence on the overall performance, such as the OTA and, in general, the modulator. Furthermore, the PSDR characteristic of the in-pixel $\Delta\Sigma$ ADC was obtained, which limits the PSNDR of the image sensor. Also, a layout of the entire gamma image sensor was done, including bondpads, for the Tezzaron two-tier process.

The gamma image sensor involved an array of 4×4 pixels, which is the same array size as Cubresa's current gamma image sensor. The design allows a bigger array because it was floorplanned to be scalable. The resultant pixel size was $102.5 \times 104.7\,\mu\mathrm{m}^2$ achieving a fill factor of 93%. The verification and layout results show that the gamma image sensor, based on a second-order $\Delta\Sigma$ DPS array, is feasible. It also represents an innovative design.

4.2 Technology Readiness

The technology readiness assessment (TRA) is a method developed to estimate the state of a technology at a given instant, evaluate the requirements that could make that technology advance in maturity, and establish a plan of how to do so. As described by the US Department of Energy (DOE) in its TRA guide [64] "it is not a pass/fail exercise and is not intended to provide a value judgment of the technology developers or the technology development program. It is a review process to ensure that critical technologies reflected in a project design have been demonstrated to work as intended (technology readiness) before committing to construction expenses."

To carry out a TRA, three phases must be completed [64]. First of all, critical technology elements (CTEs) need to be identified. CTEs are elements that either are new, are being used in a novel way, or are applied in an area in which they present high technological risk, and whose involvement is essential to the successful operation of the system [65]. After that, the TRL of the project being evaluated needs to be determined. TRLs are discrete levels, on a scale from 1 to 9, used to measure the maturity of a technology, where the higher the level the technology achieves, the more mature the technology is. Finally, once the TRL of a project has been assessed, a technology maturation plan (TMP) needs to be developed. A TMP helps identify the activities required to further advance the maturity level of the technology to a desired TRL.

Because the long-term goals of the Electronic Imaging Lab are to develop commercially-viable $\Delta\Sigma$ DPS designs, for optical and gamma imaging, a method is needed to properly assess how the work presented in this thesis contributes to these goals. Toward this end, the TRA method was chosen. Consequently, this section first explains the TRL definitions and reviews tools available for TRL calculation. Also, it examines the TRA concepts in relation to both goals. Finally, the TRLs of the optical pixel sensors and gamma image sensor developed in this thesis are determined.

4.2.1 Levels and Tools

TRLs are levels that were originally created by the National Aeronautics and Space Administration (NASA), in 1980, to assist in the development process of new space technologies. Initially, there were fewer levels, from 1 to 7 only. The first three levels represented the degree of research and development, while the last four represented the degree of testing and demonstration. Levels 8 and 9 were later added to include the degree of production and deployment [66].

Revisions to the original NASA TRLs can be found in the literature [67, 68, 64]. These works adapted the definitions given by NASA for applicability, in a general manner, to a broader suite of technologies. Table 4.1 presents the TRLs as defined by the Science and Technology Directorate (S&T) of the Department of Homeland Security (DHS) [69]. Later in this section, it will become obvious why these definitions were chosen, instead of others in the literature.

One thing that should be understood before evaluating TRLs is that the TRL scale only provides information of the maturity of a technology at a given time. Because projects, especially at early stages, may be evolving, doing so even in nonlinear ways, it is important to bear in mind that the TRL may increase or decrease with time [64].

Moreover, TRLs are neither predictive tools, metrics for program risks or health, nor a

Table 4.1: Levels of technology readiness. These TRL descriptions are taken from a department of the US government [69] that adapted definitions originally created by NASA.

Level	Description
TRL 1	Basic principles observed and reported.
TRL 2	Technology concept and/or application formulated.
TRL 3	Analytical and experimental critical function and/or characteristic proof-of-concept.
TRL 4	Component and/or breadboard validation in laboratory environment.
TRL 5	Component and/or breadboard validation in relevant environment.
TRL 6	System/subsystem model or prototype demonstration in a relevant environment.
TRL 7	System prototype demonstration in an operational environment.
TRL 8	Actual system completed and qualified through test and demonstration.
TRL 9	Actual system proven through successful mission operations.

complete measure of system readiness [68]. They only indicate how many stages in the maturation process have been completed and how many are remaining to be completed. Because the methodology assumes the final "product" will include all parts of a system, TRLs are not useful for assessing parts of a system, unless those parts can meaningfully be defined as independent "products", to which independent TRLs may be assigned.

Though it is considered a good practice to determine TRLs, assessing a technology through this method presents limitations. One of these limitations, highlighted by Smith [70], is the blurriness of the contributions to readiness. In determining the TRL, all contributors to the technology are combined, which makes it difficult to understand how any of those contributors affect the overall readiness. Also, a lack of context in the readiness assessment means that different elements of a technology, at different times, contribute differently to the risk.

There is plenty of literature about what the TRA methodology is and how the TRLs are defined. However, not long ago the methodology was lacking a tool to consistently assess the TRLs of specific non-system technologies [71], as is the case with the pixel and image sensor designs presented in this thesis. To address this issue a "Readiness Level Calculator" was developed, in 2002, at the Air Force Research Laboratory (AFRL) by Nolte [66], with improved versions that refined the TRL calculation using additional indicators.

Because the TRL by itself does not offer a complete analysis of the state of a technology, other readiness levels, such as manufacturing readiness levels (MRLs) and programmatic readiness levels (PRLs), were combined with TRLs to provide a more complete assessment, *i.e.*, one that considers manufacturability and programmaticity. The AFRL calculator contains groups of questions related to each type of readiness level. An overall TRL is calculated by averaging the TRL, PRL, and MRL, which could lead to a lower overall TRL as compared to

the TRL itself.

In 2008, DHS S&T also developed a readiness level calculator [69]. Unlike the AFRL calculator, it is possible to assess any one of the three readiness levels independently. This evidently is because the averaging of TRLs, PRLs, and MRLs was not universally accepted as a way to quantitatively represent their dependence, and no suitable alternative was found. As we are interested in determining only the technology readiness of pixel and image sensor designs, and because it is the most recently developed calculator, we use the DHS S&T calculator to assess only TRL, as reported in Sections 4.2.2 and 4.2.3 below.

The DHS S&T calculator lists activities for each TRL that are seen as milestones that need to be completed for completion of the project, *i.e.*, to reach TRL 9. The inputs are percentages assigned to each activity, which represent the percentage of completion of that activity. The output is a TRL report that indicates the TRL achieved and how close the developers are to achieve the next TRL. This is done using a color key. If a TRL is marked in red, it means said TRL has not been achieved. Yellow means that many of the tasks required for the TRL are justifiably (each over 75% complete) achieved. Green means most, if not all, tasks required for the marked TRL have been achieved [69].

A useful feature of the DHS S&T calculator is that it includes an applicability option. By default, it is set to "yes" for all milestones. This feature allows a user to disregard milestones that are not relevant to the technology being evaluated.

4.2.2 Optical Imaging Assessment

As explained earlier in this chapter, the first step to realize the TRA of a technology is to identify its CTEs. Overlooking CTEs may compromise the technology development while labeling too many elements as CTEs may create a misuse of available resources, which otherwise could have been allocated to focus on the true CTEs [65]. Looking retrospectively at the $\Delta\Sigma$ DPS technology for optical imaging, the identified CTE was the inclusion of a $\Delta\Sigma$ ADC at pixel level, along with a logarithmic sensor. This represented a novel way, requiring innovative circuits, to use a previously-established technology, *i.e.*, the classical $\Delta\Sigma$ ADC.

If we take the development of a commercially-viable camera, which works at video rates, as the long-term project, the work previously done by Mahmoodi and Joseph, hereafter called the initial design, and the work presented here, hereafter called the iteration, are milestones toward that end, although ones that represent nonlinear progress. The former can be seen as a hypotheses-proving achievement while the latter helps to lift a roadblock to further advancement of technology readiness.

In hindsight, when the initial design had completed milestones up to the TRL 3, it became

evident that an iteration was needed to enable completion of all the requirements of a commercial video camera. The main objective of this iteration was to correct the area usage, an important attribute that was not fulfilled. Without this correction, the initial design could go on to complete other milestones but in the end, the final product would not be commercially viable, *i.e.*, TRL 7 would be a ceiling for that technology.

Even though power consumption optimization was not an objective of this thesis, in particular for the optical imaging design, this does not mean that it is not another factor that could stop the initial design (and, consequently, the iteration) from becoming commercially-viable. In fact, power consumption, in the context of large DPS arrays, should be addressed to eventually pass TRL 7.

As mentioned previously, the TRL was determined with the assistance of the DHS S&T calculator. Fig. 4.1 shows (part of) the outputs obtained from the calculator when assessing the TRL of the initial design and of the iteration. For the former, the TRL achieved was 4 because, after level 3 was completed, leading to a patent [26], further laboratory validation was performed, leading to a publication [2]. For the latter, the TRL achieved was 3. Modeling and simulation activities were repeated in different ways, owing to process changes. Furthermore, experimental validation was not in the scope of this master's thesis so, logically, the TRL after the iteration could not advance further than level 3.

Notwithstanding, the iteration helped evaluate a hypothesis, *i.e.*, whether scaling and basic vertical integration alone could reduce the pixel pitch to be competitive with Pixim's (estimated) $11\ \mu\mathrm{m}$ pitch. Without this iteration, it would not have been possible to know that other strategies, complementary to the ones applied in this thesis, need to be investigated to achieve our goal, as part of a maturation plan. This work has given us insight in what needs to be done next, hence the significance of this work. Moreover, this work shows that process scaling and vertical integration will be essential parts of any final solution.

4.2.3 Gamma Imaging Assessment

For assessing the readiness of the $\Delta\Sigma$ DPS technology for gamma imaging, CTEs need to be identified first. As for the optical case, one of the CTEs was the inclusion of a $\Delta\Sigma$ ADC at pixel level, along with a logarithmic sensor. Another one was to design the photodetector and readout circuits of a complete two-tier image sensor. These CTEs make the work done in this thesis a novel approach for gamma imaging.

Unlike the optical case, there is no previous example of $\Delta\Sigma$ DPS technology for gamma imaging. Fig. 4.1(c) shows (part of) the outputs obtained from the calculator when assessing the TRL of the initial design documented in this thesis. TRL 2 received a green colour, while

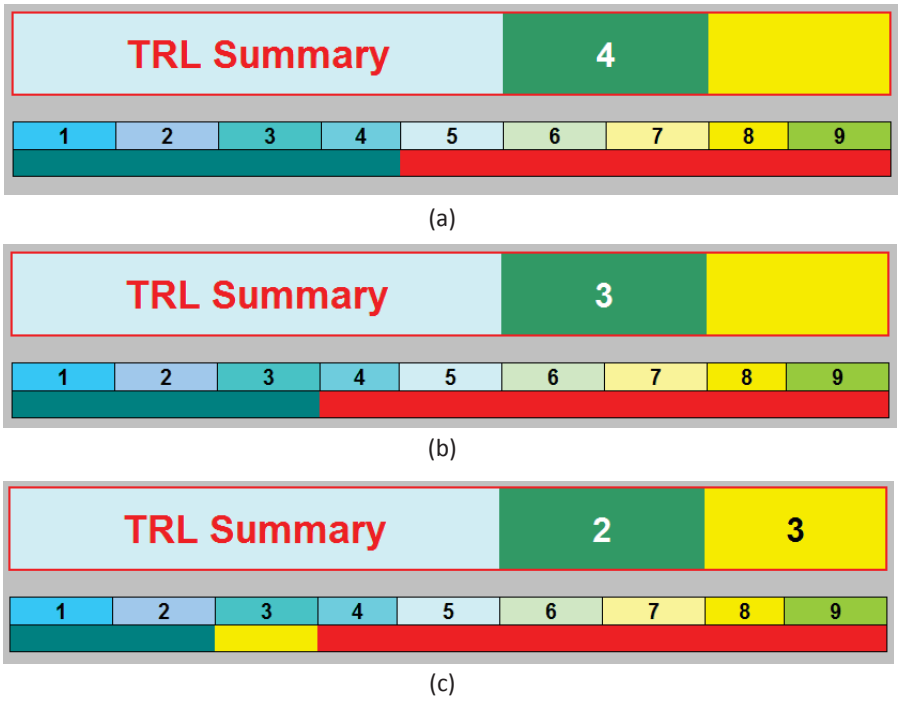


Figure 4.1: TRLs of $\Delta\Sigma$ DPS technologies. For the optical imaging, although the TRL after (a) Mahmoodi's doctoral thesis is higher than after (b) after this master's thesis, the later helps to lift the ceiling on highest-possible TRL. For gamma imaging the TRL after (c) This master's thesis represents the initial design. They were obtained using an Excel calculator [66].

TRL 3 received a yellow one. This means that 100% of the required activities were completed up to TRL 2, while TRL 3 was completed up to at least 75% of required activities. This gives an idea of how close the gamma imaging project is to the higher TRL.

TRL 3 was not entirely completed because there are pending modeling and simulation activities, more precisely at a physical level, that need to be completed to verify the performance of the entire image sensor and its individual components. The modeling and simulation phase, in the case of IC design, is not linear but iterative. In most cases, a first set of behavioral models are used to start drafting the specifications of each individual component. Then, electrical models are used for the electrical design stage and, after that, physical models are used to ensure the designed circuit is likely to match the fabricated circuit [72].

As in the case of optical imaging, experimental validation was not in the scope of this master's thesis. Because of this, the TRL could have never been above level 3 at the time of completion of this thesis. Nevertheless, the initial design helped demonstrate the feasibility of designing a fully-integrated gamma image sensor based on a $\Delta\Sigma$ DPS array. In addition, this work is the first known example of a second-order $\Delta\Sigma$ DPS, which includes both modulator and decimator at pixel level.

4.3 Maturation Plan

After identifying the current readiness level of the technologies developed in this thesis, the next step is to plan activities that can be done to further advance their readiness levels, *i.e.*, to elaborate a maturation plan. The pixel and image sensor designs presented in this master's thesis can be improved by completing certain activities that were not the main objective of this work but that are necessary for the successful completion of very-large-scale integration (VLSI) projects. Furthermore, they can also be improved by exploring options that were not considered necessary at the beginning, but which can improve the designs of both applications by complementing the approaches used in this thesis. Sections 4.3.1 and 4.3.2 elaborate on those activities, for the optical and gamma applications covered in this thesis, respectively.

4.3.1 Optical Imaging

Chapter 2 presented the design of three $\Delta\Sigma$ DPS circuits. All three designs were used to obtain a roadmap for the $\Delta\Sigma$ DPS technology for optical imaging and to know how far from the baseline for pixel pitch, *i.e.*, $11\,\mu\mathrm{m}$, this technology is. Results shown in that chapter suggest that the desirable pixel pitch could be achieved at the $5\,\mathrm{nm}$ node.

In Section 4.2.2 the first two stages of a TRA for the $\Delta\Sigma$ DPS technology for optical imaging were completed. So far, the CTEs and TRL of this technology were determined. This section concerns the third (last) stage of a TRA, *i.e.*, the elaboration of a maturation plan.

First of all, in terms of the VLSI validation, there are activities related to circuit verification that need to be completed before the design can be sent for fabrication to start physical test and experiments, *i.e.*, to pass from TRL 3 to TRL 4. These activities include thorough schematic simulation for all corners, design rule checking (DRC) of the layout, layout-versus-schematic (LVS) verification, and post-layout simulations.

Although schematic simulation, using Cadence tools, was performed for all three designs at all corners, not all circuits performed as expected on some corners, especially the fast-fast corner. Thus, the results shown in this work are based on the typical case, excluding the logarithmic sensor circuit, which did consider process variation. Consequently, the device sizing, *i.e.*, the widths and lengths of transistors and capacitors, done in this work needs to be adjusted to work properly for all corners.

Moreover, established fixed pattern noise (FPN) correction methods [7] could be applied to minimize the effects of mismatch on the overall performance of the $\Delta\Sigma$ DPS designs. Though simulations that consider temporal noise should be performed, Mahmoodi's work [18] showed that ADC distortion was the limiting factor instead.

Also, layout validation was performed for all three designs. However, only the $180\,\mathrm{nm}$

layout completely passed the DRC. This is because the 130 and $65\,\mathrm{nm}$ layouts include metal-insulator-metal (MIM) capacitors on top of other devices, which is technically not allowed but that in practice should not represent an issue. Consequently, LVS verification and post-layout simulations were only thoroughly completed for the $180\,\mathrm{nm}$ design, at the time of thesis completion.

Even though the $180\,\mathrm{nm}$ design of the iteration presented higher power consumption compared to the initial design, which was done in the same technology node, the power consumption for the iterations in the 130 and $65\,\mathrm{nm}$ processes remained within the power budget established by Mahmoodi and Joseph's approach. This means that although it is preferable to optimize the $180\,\mathrm{nm}$ iteration for power consumption, this does not stop the 130 and $65\,\mathrm{nm}$ iterations from completing other milestones to advance in technology readiness. However, it should be noted that, besides pixel pitch, power consumption should also be addressed for the initial design and, hence, the iterations. Consequently, more comprehensive low-power design techniques should be included in the design process of the $\Delta\Sigma$ DPS.

Work done in this thesis concerning the $\Delta\Sigma$ DPS has shown that the dual trend in the semiconductor industry alone will not suffice to reach the targeted pixel pitch with currently available technology processes. This means that other approaches, besides the ones applied in this work, need to be explored to reach the target pitch earlier. One alternative to reduce the pixel pitch is to change the architecture so that the modulator could be shared between four pixels in a sub-array of two-by-two pixels (*i.e.*, a color pixel).

A similar approach has already been used by several authors [11, 12, 16]. In fact, Pixim's commercialized DPS uses this approach to achieve a small pixel size. Calculations, using reported values by Bidermann *et al.*, show that Pixim's pixel pitch goes from $11\,\mu\mathrm{m}$ to $7\,\mu\mathrm{m}$ largely by sharing one ADC among 4 neighboring pixels. However, by following this approach, the new pitch target would become $7\,\mu\mathrm{m}$, in order for a fair comparison to be made between the $\Delta\Sigma$ DPS and Pixim's DPS.

Because the light-sensitive part of the pixel, *i.e.*, the photodiode, is considered to be placed in a different tier than the light-insensitive part of the pixel, sharing the latter could save (ideally) up to 75% of the current occupied area, making the pixel pitch around $10\,\mu\mathrm{m}$, for the $65\,\mathrm{nm}$ node, which is closer to the pixel pitch range for optical imaging (between 1 and $8\,\mu\mathrm{m}$), shown in Fig. 1.7. However, to avoid performance degradation it is important to account for an increment in the speed requirement of the multiplexed modulator, so that frame rate remains reasonable for optical applications. Due to the specified low rate of the optical application, *i.e.*, $30\,\mathrm{fps}$, this is unlikely to be a problem for a two-by-two pixel sub-array.

Because the pixel area begins to be limited by the capacitor area, as was shown by the 130 and $65\,\mathrm{nm}$ layouts, other approaches, such as the use of multiple-tier (more than two) 3D IC

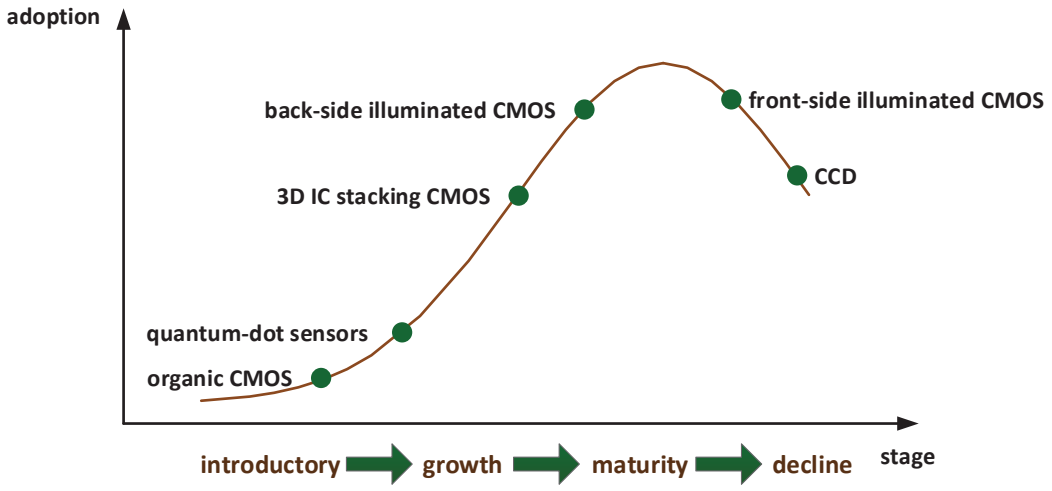


Figure 4.2: Technology adoption cycle of electronic image sensors. Front-illuminated technology is currently declining while back-illuminated technologies, which may or may not involve 3D ICs, are ascending. Taken from a presentation related to a proceeding by Skorka and Joseph [3].

processes, need to be investigated. This would allow the photodiode, the capacitors, and the rest of the pixel circuit to be placed in different tiers. By placing the capacitors in an individual tier, other types of capacitors, such as vertical natural capacitors (VNCAPs), or metal-oxide-semiconductor capacitors (MOSCAPs), can be considered as more suitable alternatives to the MIM capacitors used in this work, so overall area can be reduced. However, it is important to remember that in 3D processes there are other requirements that affect the pixel area, such as tier-to-tier connections and design rules, which could make the overall design more complicated.

Two-tier or multiple-tier 3D processes enable higher fill factor and lower dark limit (DL) [2]. The lower DL is possible due to the higher fill factor, but also to back illumination with substrate thinning. Back illumination happens because the tiers in a multiple-tier process are connected top-metal to top-metal, so only the backside is exposed to light. This means that light need not pass through multiple metal and dielectric layers before reaching the photosensitive silicon substrate. As indicated by technology and market trends of electronic image sensors, the front-illuminated approach is declining while the back-illuminated CMOS approach is ascending [3], as shown in Fig. 4.2. This suggests that, by adopting back-illuminated enabling processes, the $\Delta\Sigma$ DPS could remain a relevant technology through all maturation stages.

4.3.2 Gamma Imaging

Chapter 3 presented the prototype of the gamma image sensor where all parts were fully-integrated in an IC. Due to the fill factor requirement, the gamma imager was designed in the Tezzaron two-tier 3D IC process, where only the photodiode was placed in one tier, allowing back-side illumination, while the rest of the circuits, among them a second-order $\Delta\Sigma$ ADC, were placed in the other tier.

In Section 4.2.3, the first and second stages of the TRA for a $\Delta\Sigma$ DPS imager for gamma imaging were completed, *i.e.*, the CTEs were identified and the TRL was determined. This section concerns the elaboration of a maturation plan.

First of all, there are certain activities that need to be completed for the gamma imager to advance from TRL 2 to 3. These activities are related to further layout validation and verification through simulation. More specifically, thorough schematic simulation for all corners, DRC of the layout, LVS verification, and post-layout simulations need further work.

Though schematic simulation, using Cadence tools, was performed for all corners for the three-transistor (3T) logarithmic sensor, that was not the case for the second-order $\Delta\Sigma$ ADC and readout circuits, which were only simulated for the typical case. Consequently, the device sizing, *i.e.*, the widths and lengths of transistors and capacitors, done in this work needs to be adjusted so the gamma image sensor works properly for all corners. Moreover, established FPN correction methods [7] could be applied to minimize the effects of mismatch on the overall performance of the gamma image sensor.

Also, scalability of pixels is always preferable. Because the $\Delta\Sigma$ ADC included in each pixel of the gamma imager is already working at high frequencies, a more comprehensive timing analysis needs to be performed if a bigger array of pixels were to be included. This analysis should pay particular attention to sensitive circuits, such as the switched-capacitor accumulators, in the modulator, and shift-registers, in the decimator and readout.

Moreover, the readout scheme for an array of 4×4 pixels, shown in Chapter 3, presents four columns that are read out in parallel, one row at a time, through four one-bit data lines, *i.e.*, a column-parallel bit-serial approach. This means that four pixels needed to be multiplexed to use each data line, each row taking a quarter of the frame period for readout. Although this scheme is simple and suited for a small array of pixels, other alternatives for readout that are more scalable need to be studied for larger arrays and/or faster rates.

Another alternative that does not change the main circuit, *i.e.*, the $\Delta\Sigma$ ADC, considerably is to implement a column-parallel bit-parallel approach for readout. This requires, within the decimator, the use of serial-input parallel-output registers to implement the ping-pong buffers. As a result, there is no need to clock N times (N being the number of bits in the register) the register to have an N-bit output, which will relax the speed requirement of the readout clock

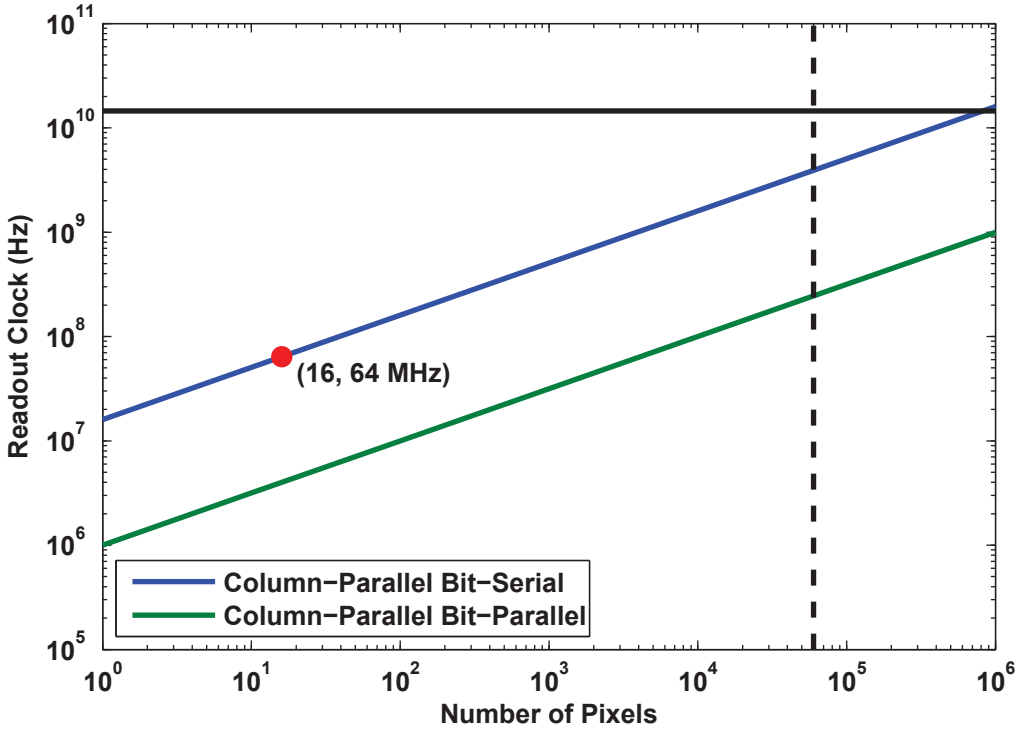


Figure 4.3: Readout clock frequency versus array size. Readout clock requirements for column-parallel bit-serial (this thesis) and bit-parallel (alternative solution) schemes as the pixel array reaches megapixel size. Figure made by Xie and taken from Azabache *et al* [30].

by N.

Fig. 4.3 compares both approaches, *i.e.*, column-parallel bit-serial and bit-parallel, in terms of clock frequency and scalability. The horizontal (bold) line represents the maximum clock frequency allowed by the CMOS technology used for this circuit. The vertical (dashed) line represents the maximum number of pixels allowed by the technology taking into account the maximum die size ($30\,\mathrm{mm} \times 20\,\mathrm{mm}$) and the nominal pixel size ($100\,\mu\mathrm{m}$) set for the gamma imager.

For the particular case of this thesis, using a column-parallel bit-serial approach, for a 4×4 pixel array with a frame rate of $1\,\mathrm{MHz}$, the required readout clock frequency is $64\,\mathrm{MHz}$, while for a column-parallel bit-parallel approach it would be $4\,\mathrm{MHz}$. For an array containing the maximum number of pixels that can be placed on a die (approximately 60,000 pixels), the column-parallel bit-serial approach surpasses the GHz clock frequency, which is undesirable. In any case, the column-parallel bit-parallel approach appears preferable, given that pixel area was not a limiting factor for the application.

References

[1] A. Mahmoodi and D. Joseph, "Pixel-Level Delta-Sigma ADC with Optimized Area and Power for Vertically-Integrated Image Sensors," in *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, pp. 41–44, 2008.

[2] A. Mahmoodi, J. Li, and D. Joseph, "Digital Pixel Sensor Array with Logarithmic Delta-Sigma Architecture," *Sensors*, vol. 13, pp. 10765–10782, Aug. 2013.

[3] O. Skorka and D. Joseph, "CMOS digital pixel sensors: technology and applications," *Proceedings of the SPIE*, vol. 9060, pp. 90600G–90600G–14, 2014.

[4] A.-J. Annema, "Analog Circuit Performance and Process Scaling," *IEEE Transactions on Circuits and Systems*, vol. 46, pp. 711–725, June 1999.

[5] X. Wang, W. Wong, and R. Hornsey, "A High Dynamic Range CMOS Image Sensor With Inpixel Light-to-Frequency Conversion," *IEEE Transactions on Electron Devices*, vol. 53, pp. 2988–2992, December 2006.

[6] Z. Chi, Y. Suying, and X. Jiangtao, "Noise in a CMOS digital pixel sensor," *Journal of Semiconductors*, vol. 32, pp. 1–5, November 2011.

[7] D. Joseph and S. Collins, "Modeling, calibration, and correction of nonlinear illumination-dependent fixed pattern noise in logarithmic CMOS image sensors," *IEEE Transactions on Instrumentation and Measurement*, vol. 51, pp. 996–1001, Oct 2002.

[8] A. El Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits and Devices Magazine*, vol. 21, pp. 6–20, May-June 2005.

[9] A. Gallivanoni, I. Rech, and M. Ghioni, "Progress in Quenching Circuits for Single Photon Avalanche Diodes," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 3815–3826, December 2010.

[10] B. Fowler, A. El Gamal, and D. X.-D. Yang, "A CMOS Area Image Sensor with Pixel-Level A/D Conversion," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 226–227, Feb. 1994.

[11] D. Yang, B. Fowler, and A. El Gamal, "A 128x128 Pixel CMOS Area Image Sensor with Multiplexed Pixel Level A/D Conversion," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 303–306, 1996.

[12] D. X.-D. Yang, B.Fowler, and A. E. Gamal, "A Nyquist-Rate Pixel-Level ADC for CMOS Image Sensors," *IEEE Journal of Solid-State Circuits*, vol. 34, p. 348, 1999.

[13] Y. Joo, J. Park, M. Thomas, K. S. Chung, M. A. Brooke, N. M. Jokerst, and D. S. Wills, "Smart CMOS Focal Plane Arrays: A Si CMOS Detector Array and Sigma-Delta Analog-to-Digital Converter Imaging System," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 5, pp. 296–305, March 1999.

[14] L. G. McIlrath, "A Low-Power Low-Noise Ultrawide-Dynamic-Range CMOS Imager with Pixel-Parallel A/D Conversion," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 846–853, May 2001.

[15] S. Kleinfelder, S. Lim, X. Liu, and A. E. Gamal, "A 10000 Frames/s CMOS Digital Pixel Sensor," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 2049–2059, Dec. 2001.

[16] W. Bidermann, A. E. Gamal, S. Ewedemi, J. Reyneri, H. Tian, D. Wile, and D. Yang, "A 0.18um High Dynamic Range NTSC/PAL Imaging System-on-Chip with Embedded DRAM Frame Buffer," in *IEEE International Solid-State Circuits Conference Technical Digest*, 2003.

[17] J. G. Rocha, G. Minas, and S. Lanceros-Mendez, "Pixel Readout Circuit for X-Ray Imagers," *IEEE Sensors Journal*, vol. 10, pp. 1740–1745, November 2010.

[18] A. Mahmoodi, *Low-Area Low-Power Delta-Sigma Column and Pixel Sensors*. PhD thesis, University of Alberta, Edmonton, AB, Canada, 2011.

[19] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. Oxford University Press, 2002.

[20] S. Norsworthy, R. Schreier, and G. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. IEEE Press, 1996.

[21] J. Candy and G. Temes, "Oversampling methods for data conversion," *IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, vol. 2, pp. 498–502, May 1991.

[22] J. Candy, "Decimation for Sigma Delta Modulation," *IEEE Transactions on Communications*, vol. 34, pp. 72–76, Jan. 1986.

[23] D. Joseph, "VLSI source coding for efficient analogue-to-digital conversion," tech. rep., University of Oxford, Dec 1998.

[24] G. C. Temes and J. C. Candy, "A Tutorial Discussion of The Oversampling Method for A/D and D/A Conversion," *Proceesings of IEEE International Symposium of Circuits and Systems*, vol. 2, pp. 910–913, 1990.

[25] O. Skorka and D. Joseph, "Toward a Digital Camera to Rival the Human Eye," *SPIE Journal of Electronic Imaging*, vol. 20, pp. 1–18, Aug. 2011.

[26] D. Joseph and A. Mahmoodi, "Pixel Sensor Converters and Associated Apparatus and Methods," *United States Patent*, pp. 1–22, June 2014. US 8745115 B2.

[27] A. L. Goertzen, J. D. Thiessen, B. McIntosh, M. J. Simpson, and J. Schellenberg, "Characterization of a Handheld Gamma Camera for Intraoperative Use for Sentinel Lymph Node Biopsy," in *IEEE Nuclear Science Symposium & Medical Imaging Conference*, pp. 1–4, 2013.

[28] K. Spartiotis, A. Leppanen, T. Pantsar, J. Pyyhtia, P. Laukka, K. Muukkonen, O. Mannisto, J. Kinnari, and T. Schulman, "A photon counting CdTe gamma- and X-ray camera," *Nuclear Instruments and Methods in Physics Research Section A-accelerators Spectrometers Detectors and Associated Equipment*, vol. 550, no. 1, pp. 267–277, 2005.

[29] P. Russo, A. S. Curion, G. Mettivier, L. Aloj, C. Caraco, and S. Lastoria, "The mediprobe cdte based compact gamma camera," in *International Federation of Medical and Biological Engineering Proceedings*, pp. 556–558, 2009.

[30] E. Azabache Villar, S. Xie, V. Degtyaryov, and D. Joseph, "Digital pixel sensor design for a gamma ray image sensor," tech. rep., University of Alberta and Phantom Motion, 2015.

[31] P. Garrou, C.Bower, and P.Ramm, *Handbook of 3D Integration, Technology and Applications of 3D Integrated Circuits*. Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, 2008.

[32] W. Arden, M. Brillouet, P. Cogez, M. Graef, B. Huizing, and R. R. Mahnkopf, "More-than-Moore," tech. rep., International Technology Roadmap of Semiconductors, 2010.

[33] R. Dennard, F. Gaensslen, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. SC-9, pp. 256–268, Jan. 1974.

[34] J. B. da Silva, *High-Performance Delta-Sigma Analog-to-Digital Converters*. PhD thesis, Oregon State University, 2004.

[35] U. Beis, "An introduction to delta sigma converters." http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma.html, 2016.

[36] M. J. M. Pelgrom and M. Vertregt, "CMOS Technology for Mixed Signal ICs," *Solid-State Electronics*, vol. 41, pp. 967–974, July 1997.

[37] W. Sansen, "Analog Circuit Design in Scaled CMOS Technology," in *VLSI Circuits Digest of Technical Papers*, pp. 8–11, June 1996.

[38] A.-J. Annema, B. Nauta, R. L. van, and H. Tuinhout, "Analog Circuits in Ultra-Deep-Submicron CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 132–143, Jan. 2005.

[39] Y. Taur, "CMOS design near the limit of scaling," *IBM Journal of Research and Development*, vol. 46, pp. 213–222, Mar.-May 2002.

[40] J. Pekarik, D. Greenberg, B. Jagannathan, R. Groves, J. R. Jones, R. Singh, A. Chinthakindi, X. Wang, M. Breitwisch, D. Coolbaugh, P. Cottrell, J. Florkey, G. Freeman, and R. Krishnasamy, "RFCMOS technology from $0.25\,\mu\mathrm{m}$ to $65\,\mathrm{nm}$: The state of the art," in *IEEE Custom Integrated Circuits Conference*, pp. 217–224, Oct. 2004.

[41] A. Baschirotto, V. Chironi, G. Cocciolo, S. Dmico, M. D. Matteis, and P. Delizia, "Low power analog design in scaled technologies," in *Proceedings of Topical Workshop on Electronics for Particle Physics*, pp. 103–110, Sept 2009.

[42] CMC, "Design Kit: TSMC $0.18\mu\mathrm{m}$ CMOS Process." https://www.cmc.ca/WhatWeOffer/Products/CMC-00000-48823.aspx.

[43] CMC, "Design Kit: GF (IBM) $0.13\mu\mathrm{m}$ CMOS." https://www.cmc.ca/WhatWeOffer/Products/CMC-00000-48598.aspx.

[44] CMC, "Design Kit: TSMC 65nm CMOS LP (CRN65LP)." https://www.cmc.ca/en/WhatWeOffer/Products/CMC-00131-53461.aspx.

[45] M. Bohr, "The New Era of Scaling in an SoC World.," in *IEEE International Solid-State Circuits Conference: Digest of Technical Papers*, pp. 23–28, Feb. 2009.

[46] W. Muller and I. Eisele, "Velocity saturation in short channel field effect transistors," *Solid State Communications*, vol. 34, pp. 447–449, 1980.

[47] TSMC, *TSMC* $0.18\,\mu\mathrm{m}$ *Mixed Signal/RF* $1\mathrm{P}6\mathrm{M}$ *Salicide* $1.8V/3.3V$ *Design Rule*. Taiwan Semiconductor Manufacturing Co., LTD, June 2006.

[48] IBM, *CMOS8RF (CMRF8SF) Design Manual*. International Business Machines Corporation, Nov. 2010.

[49] ITRS, "International Technology Roadmap for Semiconductors: Interconnect," tech. rep., International Technology Roadmap for Semiconductors, 2009.

[50] K. Murari, R. Etienne-Cummings, N. Thakor, and G. Cauwenberghs, "Which photodiode to use: A comparison of CMOS-compatible structures," *IEEE Sensors Journal*, vol. 9, pp. 752–760, July 2009.

[51] H. Tian, X. Liu, S. Lim, S. Kleinfelder, and A. El Gamal, "Active pixel sensors fabricated in a standard 0.18-$\mu\mathrm{m}$ CMOS technology," in *Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications II*, vol. 4306, 2001.

[52] R. C. Gonzalez and R. E. Woods, *Digital Image Processing*. Prentice Hall, 2007.

[53] N. Ricquier and B. Dierickx, "Pixel structure with logarithmic response for intelligent and flexible imager architectures," in *Proceedings of the 22nd European Solid State Device Research Conference*, pp. 631–634, 1992.

[54] K. Takada and S. Miyatake, "Logarithmic-converting CCD line sensor and its noise characteristics," tech. rep., Research and development headquarters, Minolta Co., Ltd., 1997.

[55] M. Loose, K. Meier, and J. Schemmel, "A self-calibrating single-chip CMOS camera with logarithmic response," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 586–596, April 2001.

[56] H. Zare-Hoseini, I. Kale, and O. Shoaei, "Modeling of switched-capacitor delta-sigma modulators in SIMULINK," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, pp. 1646–1654, Aug 2005.

[57] T. Ndjountche and R. Unbehauen, "Design techniques for high-speed sigma delta modulators," in *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, vol. 2, pp. 916–919, 2000.

[58] O. Skorka, J. Li, A. Harrison, M. Alexiuk., and D. Joseph, "Design of a low-dose X-ray imaging system using vertically-integrated CMOS circuits," tech. rep., Electrical and Computer Engineering, University of Alberta, IMRIS, Winnipeg, Manitoba, 2013.

[59] O. Skorka, J. Li, and D. Joseph, "Nonlinear Digital Pixels: Idea to Innovation (Phase I)," tech. rep., University of Alberta, 2013.

[60] A. Chang and W. J. Dally, "The role of custom design in ASIC chips," in *Proceedings of the 37th Annual Design Automation Conference*, pp. 643–647, 2000.

[61] D. F. Tapia and J. Schellenberg, "Review of gamma event detection architectures," tech. rep., Cubresa, 2012.

[62] Global Foundries, *0.13* μm *CMOS Logic/Mixed Signal/RF Technology Design Rules*, Oct. 2010.

[63] E. Azabache Villar, O. Skorka, and D. Joseph, "Small-area decimators for delta-sigma video sensors," *Proceedings of the SPIE*, vol. 9060, pp. 1–11, 2014.

[64] U.S. Department of Energy, *Technology Readiness Assessment Guide*. U.S. Department of Energy, 2011.

[65] Director and Research Directorate (DRD) Office of the Director and Defense Research and Engineering (DDR&E) , "Technology Readiness Assessment (TRA) Deskbook," tech. rep., Department of Defense, 2009.

[66] W. L. Nolte, B. C. Kennedy, and J. Roger J. Dziegiel, "Technology readiness calculator," tech. rep., Air Force Research Laboratory, 2003.

[67] J. C. Mankins, "Technology readiness levels," tech. rep., NASA, 1995.

[68] Assistant Secretary of Defense for Research and Engineering, "Technology Readiness Assessment (TRA) Guidance," tech. rep., Department of Defense, 2011.

[69] D. McGarvey, J. Olson, S. Savitz, G. Diaz, and G. Thompson, "Department of homeland security science and technology readiness level calculator," tech. rep., Homeland Security Studies and Analysis Institute, 2009.

[70] James D. Smith II, "An Alternative to Technology Readiness Levels for Non-Developmental Item (NDI) Software," in *Proceesings of the 38th Hawaii International Conference on System Sciences*, 2005.

[71] C. P. Graettinger, S. Garcia, and J. Siviy, "Using the Technology Readiness Levels Scale to Support Technology Management in the DoD's ATD/STO Environments," tech. rep., Army CECOM, 2002.

[72] A. J. L. Martin, *Tutorial of Cadence Design Environment*. Klipsch School of Electrical and Computer Engineering New Mexico State University, October 2002.

Appendix A

Device Sizing

This appendix presents the dimensions of the devices and bias voltages values used in the designs presented in this thesis. The corresponding values for the smaller-area designs, covered in Chapter 2, are shown in section A.1 while the ones for the faster-rate design, covered in Chapter 3, are shown in section A.2. Device sizing is broken down into the main blocks of each design.

A.1 Smaller Area Designs

This section refers to the designs of three smaller-area delta-sigma ($\Delta\Sigma$) digital pixel sensor (DPS), that can be found in Chapter 2. Device sizing and voltage biasing, for each technology node used, is shown for each main block.

First of all, all transistors included in logic gates were dimensioned such as they use the minimum channel length possible in the technology used. Also, their widths are $420\,\mathrm{nm}$, $280\,\mathrm{nm}$, and $150\,\mathrm{nm}$ for the 180, 130, and $65\,\mathrm{nm}$ processes. Because the embedded DAC and differencer (EDD) is mainly made out of logic gates, it can be kept small enough compared to other blocks in the modulator. Table A.1 shows the devices sizes for the EDD included in a $\Delta\Sigma$ modulator for optical applications.

For the accumulator, switches and capacitors are sized such as they occupy as little area as possible, as can be seen in Table. A.2. The operational transconductance amplifier (OTA), that is part of the accumulator circuit, is sized for performance taking into account the area restrictions of the optical imaging application.

Here, the transistor sizes have been chosen such as the OTA can have a DC gain of over $55\,\mathrm{dB}$, phase margin around 60 degrees, and over $50\,\mathrm{kHz}$. In this case, the transistor length is not necessarily the minimum allowed by the technology. Table A.3 shows the devices sizes and bias voltages of the OTA for optical imaging.

Table A.1: Device sizes of the EDD for smaller area. The widths and lengths are listed for this block, that was built using a MUX, for the three technology processes used for smaller DPS designs.

Device	180 nm	130 nm	65 nm
W (nm)	420	360	150
L (nm)	180	120	60
V_{cmi} (V)	0.9	0.6	0.5
V_{max} (V)	1.15	0.8	0.7
V_{min} (V)	0.65	0.4	0.3

Table A.2: Device sizes of the accumulator for smaller area. The widths and lengths and capacitance values are listed for this block for the three technology processes used in for smaller DPS designs.

Device	180 nm	130 nm	65 nm
W (nm)	420	360	150
L (nm)	180	120	60
C_i (fF)	60	60	30
C_s (fF)	20	20	10

The next circuit in the modulator is the embedded analog-to-digital converter (ADC). This block is implemented using a clocked comparator. Because saving area is the most important concern for the $\Delta\Sigma$ DPS for optical applications, width and length dimensions are kept to the minimum necessary. Table A.4 shows these values.

For the decimator, all transistors were set to minimum size, including logic gates, as shown in Table A.5. The $65\,\mathrm{nm}$ D flip flop was size differently. Its width and length are $200\,\mathrm{nm}$ and $60\,\mathrm{nm}$, respectively .

A.2 Faster Rate Design

This section refers to the design that can be found in Chapter 3. Device sizing and voltage biasing is shown for each main block of the second-order $\Delta\Sigma$ ADC.

Here, all transistors included in logic gates were dimensioned such as they use the minimum channel length possible in $130\,\mathrm{nm}$ Tezzaron technology. Also, the transistors widths in the logic gates are $360\,\mathrm{nm}$ except for the ones carrying bigger loads. Table A.6 shows the devices sizes for both EDDs included in the second-order $\Delta\Sigma$ modulator for gamma applications.

Table A.3: Device sizes of the OTA for smaller area. Aspect ratios are listed for this block for the three technology processes used in for smaller DPS designs.

Device	180 nm	130 nm	65 nm
N1	2µm/500nm	2µm/300nm	0.9µm/160nm
N2	1µm/500nm	1µm/300nm	0.45µm/160nm
N3	1µm/500nm	1µm/300nm	0.45µm/160nm
N4, N5	1µm/500nm	1µm/300nm	0.45µm/160nm
N6	1µm/500nm	0.3µm/300nm	0.45µm/160nm
N7	1µm/180nm	0.75µm/300nm	0.40µm/60nm
N8, N9	8µm/500nm	6µm/300nm	4µm/160nm
P1	4µm/500nm	1.5µm/300nm	1.6µm/200nm
P2	4µm/500nm	1.5µm/300nm	2µm/160nm
P3	4µm/500nm	1.5µm/300nm	2µm/160nm
P4, P5	2µm/500nm	2µm/300nm	1µm/160nm
V_{b1} (V)	1.2	0.9	0.7

Table A.4: Device sizes of the embedded ADC for smaller area. The widths and lengths of this block, that was built using an clocked comparator, are listed for this block for the three technology processes used in for smaller DPS designs.

Device	180 nm	130 nm	65 nm
W (nm)	420	360	150
L (nm)	180	120	60
V_b (V)	0.4	0.3	0.3

Two accumulators are included in the in-pixel second-order $\Delta\Sigma$ ADC. The OTAs, that are part of the accumulator circuits, are sized for wide bandwidth taking into account the rate restrictions of the gamma imaging application.

Table A.7 and A.8 show the sizes of the devices and bias voltages of the accumulators and OTAs for gamma imaging.

The last circuit in the modulator is the embedded ADC. This block is implemented using a clocked comparator. Table A.9 shows values for width, length and capacitance for this block.

For the decimator, all transistors were set for fast settling. Transistors in critical paths were dimensioned to 720 nm width. Actual sizes are shown for those transistors are shown in Table A.10.

Table A.5: Device sizes of the flip flop for smaller area. The widths and lengths of this block, that was built using two pulsed latches, are listed for this block for the three technology processes used in for smaller DPS designs.

Device	180 nm	130 nm	65 nm
W (nm)	420	280	150
L (nm)	180	120	60

Table A.6: Device sizes of the EDDs for faster rate. The width and length of transistors of this block, that was built using a MUX, are listed.

Device	Value
W (nm)	720
L (nm)	130
V_{cmi} (V)	0.7
V_{max} (V)	0.8
V_{min} (V)	0.4

Table A.7: Device sizes of the accumulators for faster rate. The width and length of transistors and capacitance values are listed for this block.

Device	Value
W (nm)	360
L (nm)	130
C_i (fF)	60
C_s (fF)	20

Table A.8: Device sizes of the OTAs for faster rate. Aspect ratios are listed for these blocks.

Device	Value
N1	20µm/300nm
N2	10µm/300nm
N3	10µm/300nm
N4, N5	30µm/300nm
N6, N7	10µm/300nm
N8, N9	2µm/300nm
P1	54µm/300nm
P2	54µm/300nm
P3	54µm/300nm
P4, P5	10µm/600nm
V_{b1} (V)	1

Table A.9: Device sizes of the embedded ADC for faster rate. The width and length of transistors for this block, that was built using a clocked comparator, are listed.

Device	Value
W (nm)	360
L (nm)	130
V_b (V)	0.4

Table A.10: Device sizes of the flip flop for faster rate. The width and length of the transistors for this block, that was built using two pulsed latches, are listed.

Device	Value
W (nm)	360
L (nm)	130