PWM and Control Strategies for AC-DC Matrix Converters

by

Fanxiu Fang

A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
ENERGY SYSTEMS

Department of Electrical and Computer Engineering
University of Alberta

Abstract

Alternating Current (AC)-Direct Current (DC) matrix converters can realize buck type rectifying and boost type inverting without bulky and vulnerable intermediate DC link capacitors. Thus, the topology shows great advances in applications like vehicle to grid, DC microgrid, data center, and telecom equipment, etc. According to the applications' requirements, AC-DC matrix converters can be built with or without a high frequency transformer (HFT) for isolation. The non-isolated AC-DC matrix converter has a simple structure and can effectively reduce the system size and cost, while the isolated AC-DC matrix converter can provide galvanic isolation for safety. However, both types of AC-DC matrix converter face some challenges, such as reliability of commutation, current distortions, and control complexity.

The purpose of this thesis is to develop modulation and control strategies for AC-DC matrix converters; therefore, current qualities can be improved while reliable commutation is ensured.

Firstly, the challenges in non-isolated AC-DC matrix converters are addressed. The multiple objectives control of the non-isolated AC-DC matrix converter is a major challenge since the single-stage converter shall regulate both AC current and DC current. To improve the quality of both currents and avoid narrow pulses, the finite control set model predictive control (FCS-MPC) with virtual space vectors, featuring multiple objectives capabilities and direct generation of gating signals without the pulse width modulation (PWM) scheme, is proposed.

Secondly, the challenges of isolated AC-DC matrix converters are addressed.

To enhance the commutation safety while achieving sinusoidal AC current, a 9-segment space vector modulation (SVM) strategy is proposed to avoid the commutation between two phases with close voltage magnitudes. The strategy can achieve high current quality even under a relatively large commutation duty ratio (commutation time divided by switching period). Generally, the commutation between bidirectional switches will require a long commutation time; however, with the development of fast-switching devices, the commutation time is reduced significantly. When the switching frequency is not very high, the commutation impact becomes smaller. In this case, another SVM method is developed to reduce low order harmonics with a reduced number of switching actions for higher efficiency and high quality AC current. To further improve the performance under light load condition based on the proposed SVM method, a new control method to coordinate modulation index and phase-shift angle is proposed to reduce current stress and improve system efficiency.

Finally, with the galvanic isolation provided by the HFT, isolated AC-DC matrix converters can be operated in parallel with increased power rating and mitigated circulating current. To achieve high performance for paralleled configuration, an interleaved sine pulse width modulation (SPWM) strategy is developed for unidirectional isolated AC-DC matrix converters. The interleaved SPWM can significantly suppress DC current ripples and it has good scalability and ease of implementation. Also, the duty cycle loss is compensated to reduce low order harmonics. As a result, the converters can achieve better current quality at both the AC and DC sides.

Acknowledgments

I would like to express my deepest gratitude to my supervisor, Yunwei (Ryan) Li, for providing me the opportunity to work in his research group and work on this project. I have a deep respect for his expertise and enthusiasm for research. Thanks for his continuous support and encouragement during my study at the University of Alberta.

I would like to thank Hao Tian for his assistance in laboratory experiments. Besides, a special thanks to Yuzhuo Li for his valuable advice on my research work. Thanks also to all the other colleagues at the lab for their help or accompany during my PhD program.

I would also like to thank the China Scholarship Council for providing me the scholarship.

Finally, I am immensely grateful to my parents, my sister, and my husband for supporting me spiritually throughout my PhD program and my life in general.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

AC	Alternating Current
CSC	Current Source Converter
DC	Direct Current
DSP	Digital Signal Processor
EMIF	External Memory Interface
FCS-MPC	Finite Control Set Model Predictive Control
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
GTO	Gate Turn-Off Thyristor
HFT	High Frequency Transformer
IGBT	Insulated Gate Bipolar Transistor
IMC	Indirect Matrix Converter
IPOP	Input-Parallel-Output-Parallel
IPOS	Input-Parallel-Output-Series
ILMC	Inverting Link Matrix Converter
LFT	Low Frequency Transformer
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPC	Model Predictive Control
PWM	Pulse Width Modulation
PI	Proportional Integral
RMS	Root Mean Square
SVM	Space Vector Modulation
SPWM	Sinusoidal Pulse Width Modulation
SiC	Silicon Carbide
SCR	Silicon Controlled Rectifier
THD	Total Harmonic Distortion
UPS	Uninterrupted Power Supplies
USMC	Ultra Sparse Matrix Converter

VSC	Voltage Source Converter
VSMC	Very Sparse Matrix Converter
WBG	Wide Bandgap
3-1 MC	Three-phase to Single-phase Matrix Converter

Chapter 1

Introduction

AC-DC power conversion has wide applications due to the high demand to supply DC components with a utility grid [1-2]. In AC-DC power conversions that interface a low DC voltage, AC-DC matrix converters show advances as they can realize buck type rectifying and boost type inverting in single-stage [3]. Compared to the voltage source converter (VSC) or current source converter (CSC) which holds a constant voltage or current on the DC link, the AC-DC matrix converters do not require any large energy storage component. The elimination of the intermediate energy component permits a compact implementation and increases the system lifetime [4]. Moreover, when galvanic isolation is required for safety concerns, the HFT can be easily integrated by adding an H-bridge constructed by diodes or active switches.

Due to these advantages and the development of power semiconductors, particularly the commercialization of the wide bandgap (WBG) devices, AC-DC matrix converters are increasingly researched in industrial applications where sizes, weights, and long-term reliability are important. Typical examples include power supply for data center, on-board electric vehicle charger, energy storage system, etc. [5-7].

1.1 AC-DC Converters with Low Voltage DC Bus

In the past few decades, VSCs are the most popular solutions for AC-DC conversion. However, the inherent feature of VSC, boost-type rectifying and buck-type inverting, requires that the DC voltage shall be higher than the line-to-line voltage. However, in practice, lots of DC components require lower DC voltage than AC line-to-line voltage. Typical applications include uninterrupted power supplies (UPS) for communication base station, server, and data center, 48V battery/fuel cell charger, etc. Specifically, a converter for the data center connects

a 400/480V AC to a 400V DC. Besides, the DC fast charger generally converts a 480V AC to a 250-450V DC [8-9]. As shown in Figure 1.1(a), with the VSCs, the AC is first converted to a high DC voltage, and then adjusted to the desired voltage level by a DC-DC converter. In other words, an extra DC-DC conversion stage shall be inserted between the DC bus and AC-DC converter. Another drawback of VSC based AC-DC converters is the bulky electrolytic capacitors for the intermediate DC link. This leads to the high volume and weight of the whole converter. Besides, the electrolytic capacitor is one of the most vulnerable components with a short lifespan, degrading the reliability and lifetime of the whole system.

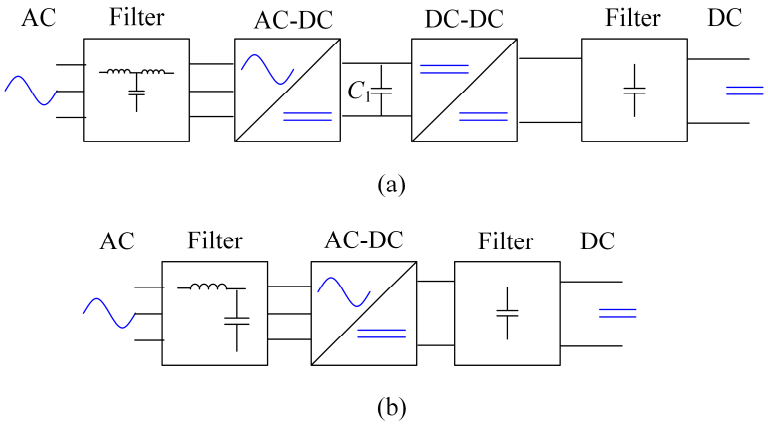


Figure 1.1 Topologies of buck type AC-DC conversion (a) two-stage (b) single-stage

To overcome the disadvantages of VSC-based multiple-stage converters, buck type rectifiers have been researched to allow a single-stage energy conversion (as shown in Figure 1.1(b)) between the grid and a DC bus with lower voltage, such as CSC [10], Z-source converter [11], and bidirectional swiss rectifier [12].

Figure 1.2 (a) shows the topology of CSC. It is constructed by six switches to allow unidirectional current flow and bidirectional voltage blocking. The switch can be constructed by a gate turn-off thyristor (GTO) / silicon controlled rectifier (SCR) that has reverse block capability, or an insulated gate bipolar transistor (IGBT) in series with a diode to block reverse voltage. The output voltage is synthesized by AC line-to-line voltage, so the DC voltage is smaller than the AC voltage. However, this topology only allows for unidirectional power flow.

A Z-source structure is proposed by F.Z Peng [13] in 2002 to achieve AC-DC

conversion in single-stage conversion, as shown in Figure 1.2(b). In this topology, two inductors and two capacitors are connected in X shape between the converter and DC source/load. The converter can be a VSC or CSC, and the DC source can be a voltage source or current source. The Z-source converter has a buck-boost characteristic, but it requires many passive components. Also, high voltage capacitors are required, which leads to a higher volume and cost. Furthermore, the inductor and capacitor may cause resonance when the converter starts up, which may cause large voltage, inrush current and destroy switching devices [14].

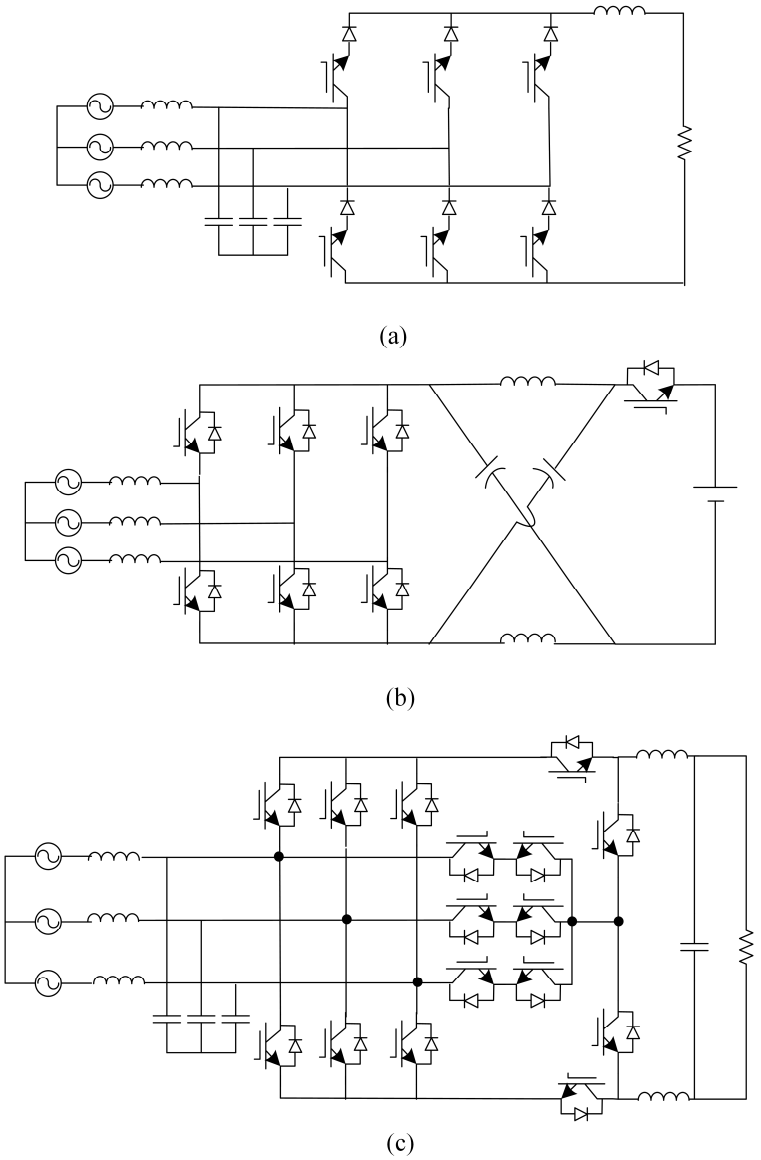


Figure 1.2 Topologies of single-stage buck type conversion (a) CSC (b) Z-source converter (c) bidirectional swiss rectifier

Swiss rectifier is proposed in 2012, as shown in Figure 1.2(c) [15]. It is constructed by a bidirectional input voltage selector and two DC-DC converters. The input voltage sector uses a three-phase bridge and three bidirectional switches to select maximum, medium, and minimum voltage on three output ports. The two DC-DC converters are controlled to achieve sinusoidal AC current, but the current is distorted at the intersections of the grid voltages. Also, this topology requires more power semiconductors and thus can be of a high cost.

As can be seen, the abovementioned topologies have their limitations. Therefore, it is necessary to find a topology with the buck-type rectifying / boost-type inverting ability with bidirectional power flow, low device count, and good waveform quality. A non-isolated AC-DC matrix converter is a promising option.

A similar problem also exists in isolated AC-DC conversions. When galvanic isolation is required to ensure safe operation and eliminate circulating current in paralleled systems, the low frequency transformer (LFT) can be connected to converters. To achieve reduced weight and volume without compromising efficiency, cost, and reliability, the LFT is increasingly replaced by an HFT [16]. Generally, the HFT is included in the DC-DC conversion, as shown in Figure 1.3(a). In isolated AC-DC converters, VSC based solutions also require extra stages with bulky DC link capacitors to smoothen the DC voltage, resulting in a relatively large physical volume and shorter lifetime.

The isolated AC-DC converter has an opportunity to reduce the DC link capacitor without using alternative topologies—relaxing the DC link voltage regulation as it is not directly connected to the DC output. Many works have been researched on the DC link capacitor elimination or reduction [17-22], shown in Figure 1.3 (b). A solution is to remove the intermediate DC link capacitor, the pulsating DC link voltage is generated. But overvoltage will be generated due to the energy stored in the leakage inductance has no conduction path. To absorb the energy, the conventional dissipative RCD snubber can be connected to the HFT, or an improved snubber circuit with reduced components can be connected to the intermediate DC link. However, both the two types snubber circuits can bring in losses and reduce the power efficiency. To reduce the loss, an active clamp snubber

circuit which is constructed by an active switch in series with one capacitor can be connected to the intermediate DC link [20]. Another solution is using a small film capacitor to replace the large electrolytic capacitor [21], but the DC link voltage is less stable due to the capability of storing energy is reduced, and overvoltage or undervoltage faults may cause once the source inductance is large compared to the DC link capacitance [22].

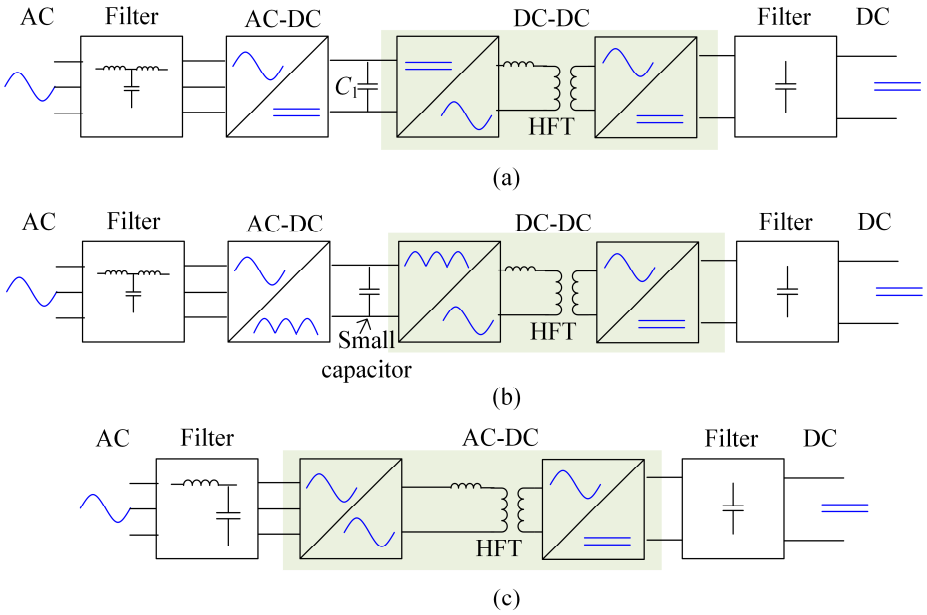


Figure 1.3 Topologies of different isolated AC-DC converters (a) two-stage conversion (b) quasi single-stage conversion (c) single-stage conversion

For the isolated AC-DC conversion, the matrix converter also shows great potential as it naturally does not need the DC link capacitor for the first-stage AC-AC conversion. Meanwhile, the matrix converter can convert line frequency AC to a high frequency AC, which can be directly applied to an HFT to further reduce required switches by omitting the converter circuit for HFT's primary side. The topology is shown in Figure 1.3 (c) [23].

To sum up, both the non-isolated AC-DC matrix converter and the isolated AC-DC matrix converter are promising in AC-DC conversions.

1.2 Structures of AC-DC Matrix Converters

AC-DC matrix converters are considered a promising solution for AC-DC conversions with low voltage DC bus. It can be classified into two categories: non-isolated AC-DC matrix converter and isolated AC-DC matrix converter [24-26]. Since single-stage buck type conversion can lower down weight/volume, and increase reliability, the AC-DC matrix converters show advantages in applications where variable DC voltage is required, or the DC voltage is lower than AC voltage. When galvanic isolation is required between the load and grid for safety concerns or when different grounding schemes are needed in applications, the isolated AC-DC matrix converter can be explored.

In the following subsections, the topology evolution of the two types of AC-DC matrix converter will be illustrated.

1.2.1 Non-isolated AC-DC Matrix Converter

The AC-DC matrix converters are derived from the AC-AC matrix converter; therefore, they share some features. To better illustrate the AC-DC matrix converters, the AC-AC matrix converter topology will be illustrated first.

The basic configuration of the AC-AC matrix converter is proposed by Venturini and Alesina in 1980 [27]. It uses an array of controlled bidirectional switches to enable three-phase AC-AC conversion without any intermediate energy storage component, as shown in Figure 1.4. It shows that the input side of the converter is connected to the power supply through a CL filter, while the output side is connected to the load through an inductor. When the power supply and the load of are swapped, another type matrix converter is introduced in [28]. However, the latter type is not often considered due to the realization requires a large inductance. Moreover, the energy accumulated in source inductors is dangerous when all switches are turned off. Hence, the matrix converter topology in Figure 1.4 is widely researched, and the derived AC-DC matrix converter are considered in this thesis. The matrix converter topology enables higher power density than back to back VSC (2.5 times), and it shows advantages when small size or weight is required [4, 29].

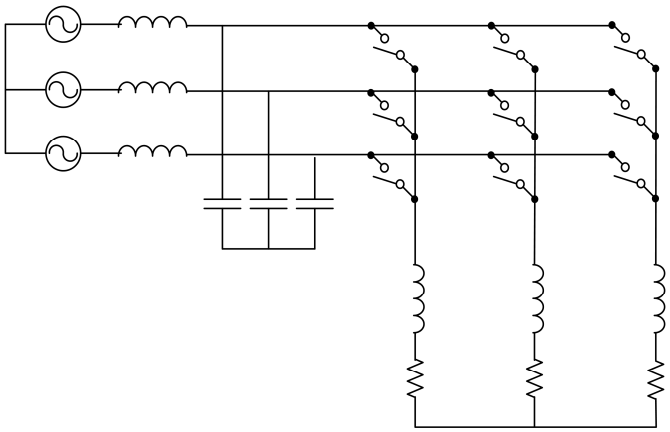


Figure 1.4 Topology of AC-AC matrix converter

The matrix converter requires bidirectional switches to block voltage and conduct current in both directions. However, no such device is available, instead, unidirectional devices are used to construct a bidirectional switch cell. Generally, there are four different ways to build bidirectional switch cells, as shown in Figure 1.5. A diode bridge bidirectional switch cell is presented in Figure 1.5(a) which contains an IGBT that connects with four diodes [30-31]. The same active switch can conduct the current in two directions, so only one switching signal is needed. However, the conduction loss is high because one active switch and two diodes are conducted in any current direction. Moreover, the current direction is uncontrolled in this switch cell. As an alternative, the configuration of the anti-parallel reverse blocking IGBT is given in Figure 1.5(b). It can control the current while the rising slope of the collector current and collector to emitter voltage is relatively high during switching transition due to the lack of fast recovery diode [32-33]. Another solution is to use a common-emitter anti-parallel IGBT bidirectional switch cell shown in Figure 1.5(c). Two IGBTs are used to provide the current path and two diodes are connected to provide the reverse blocking capability. The current direction can be controlled, and only one IGBT and one diode are conducted at each conduction path. The conduction loss is reduced compared with the diode bridge bidirectional switch cell. The last bidirectional switch type is a common collector bidirectional switch cell, as presented in Figure 1.5(d). The conduction loss is the same as the common emitter. However, the common emitter anti-parallel IGBT

configuration has the potential to use one isolated power supply for two IGBT gate drivers. Therefore, the common-emitter configuration is preferable for a matrix converter.

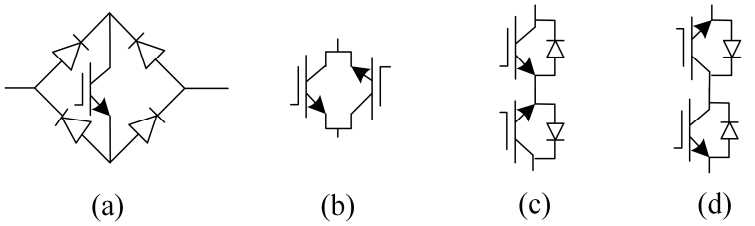


Figure 1.5 Different bidirectional switch cell (a) diode bridge bidirectional switch cell (b) anti-parallel reverse blocking IGBT (c) common emitter anti-parallel IGBT (d) common collector anti-parallel IGBT

Utilizing similar bidirectional switches, in 2001, L. Wei et al., propose the indirect matrix converter (IMC) topology [34], as shown in Figure 1.6. It contains two parts, a voltage-fed rectifier on the input side and a voltage source inverter on the output side. The two parts are directly connected on the fictitious DC link, and the fictitious link can be operated with both positive and negative link voltage while only the positive voltage is required in IMC. By limiting the fictitious DC link voltage to unipolar, the number of active switches can be reduced in sparse matrix converter (SMC), ultra sparse matrix converter (USMC), very sparse matrix converter (VSMC), and inverting link matrix converter (ILMC) [35-36].

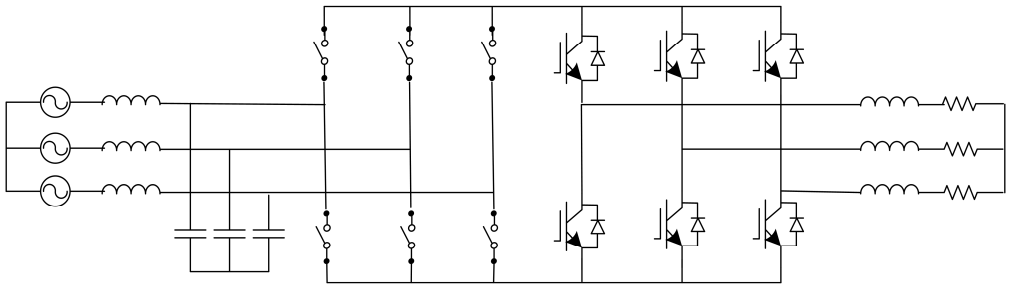


Figure 1.6 Topology of indirect AC-AC matrix converter

By setting the output frequency to zero, and connecting the load between two phases, the non-isolated AC-DC matrix converter is derived. The topology is shown in Figure 1.7, which is proposed by Holmes and Lipo in 1989 [37]. As can be seen, the non-isolated AC-DC matrix converter shares the same phase-legs with

bidirectional switches in IMC. By controlling the bidirectional switches properly, AC current can be synthesized by DC current, and the output DC voltage is constructed by filter capacitor voltages. To mitigate the current ripples on the DC side, an inductor is added so that the DC loads can see a relatively smooth DC current. In literature, this topology can also be called bidirectional CSC [38]. Compared to conventional CSC, the bidirectional switch can ensure bidirectional power flow and reduce conduction loss.

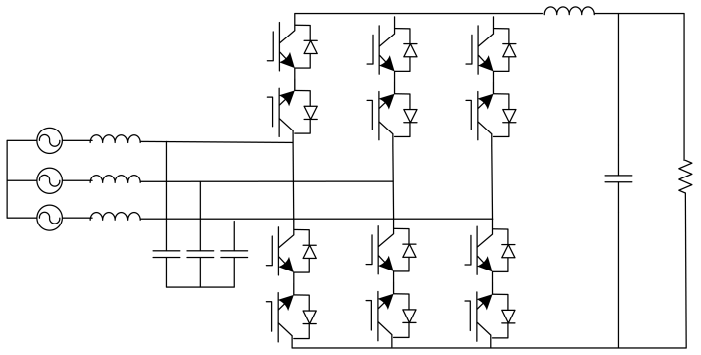


Figure 1.7 Topology of non-isolated AC-DC matrix converter

1.2.2 Isolated AC-DC Matrix Converter

In 1985, the unidirectional isolated AC-DC matrix converter is proposed by Stefanos Manias, and the topology is given in Figure 1.8 [39]. It utilizes a three-phase to single-phase matrix converter (3-1 MC) for selecting line-to-line voltages, and then they are applied to the primary side of the transformer. After the isolation, the high frequency voltage is rectified to a DC voltage by an H-bridge diode, followed by an inductor to smooth the DC output current. Since the secondary side is an H-bridge diode, the converter can only transfer power from the AC side to the DC side. To achieve bidirectional power flow capability, the diodes are replaced by active switches in [40], as shown in Figure 1.9. Unlike the unidirectional isolated matrix converter, this topology depends on a leakage inductor to transfer power between the primary side and the secondary side. Moreover, the DC side is connected to a capacitor instead of an inductor.

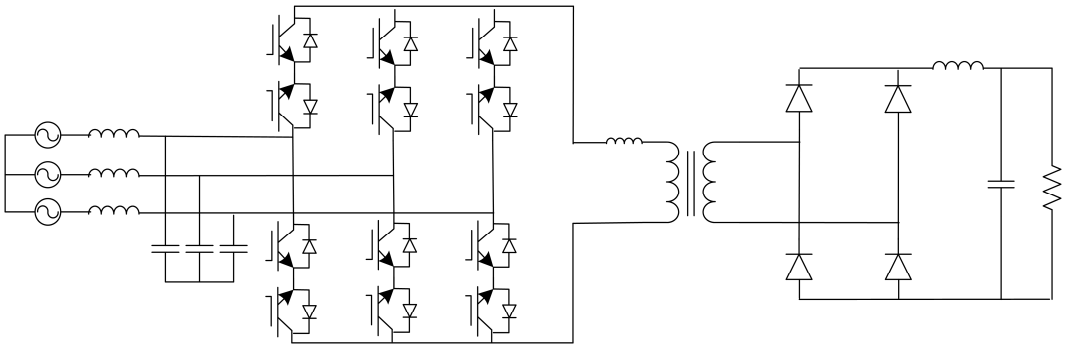


Figure 1.8 Topology of unidirectional isolated AC-DC matrix converter

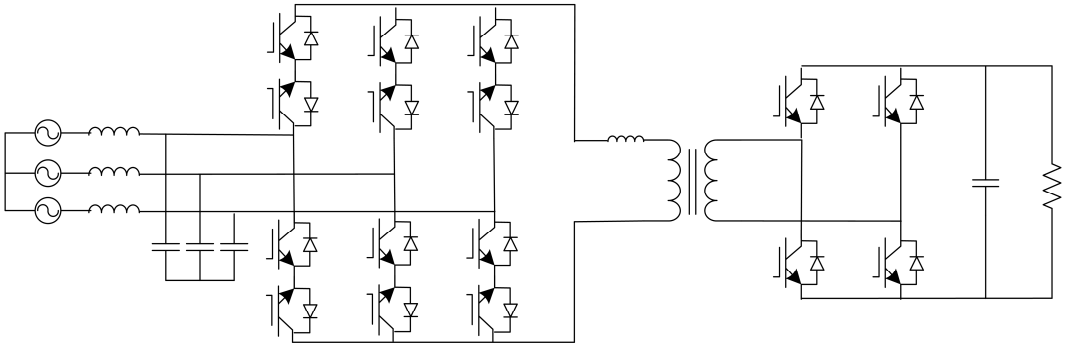


Figure 1.9 Topology of isolated AC-DC matrix converter

1.3 Commutation and PWM Methods of AC-DC Matrix Converters

1.3.1 Commutation of the Bidirectional Switches

Although the matrix converter has some advantages, it is not a popular commercialized topology in industrial applications due to the challenges of the commutation between bidirectional switches [41]. Different from switches in VSCs, the bidirectional switches in matrix converter cannot naturally form freewheeling paths. As a result, if the bidirectional switch is completely turned off, the circuit will see a significant *di/dt*, inducing a high voltage which may damage the switches. Therefore, the bidirectional switches must be properly controlled to provide the freewheeling path for inductive currents. Besides, considering the capacitors on the input side, the commutation should not cause a short circuit between two input phases.

Unlike the VSC, simply inserting dead time during the transition cannot guarantee safe operation, taking S_{ap} switch to S_{bp} as an example in Figure 1.10. If S_{ap} is turned off before S_{bp} is turned on, there is no current path for the inductor; therefore, voltage spikes will be caused, and switches will be destroyed. If S_{bp} is turned on before S_{ap} is turned off, the capacitors in phase A and phase B will be short circuit, overcurrent will be generated.

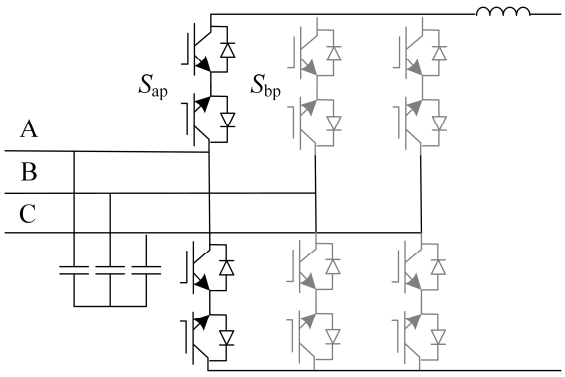


Figure 1.10 Commutation between S_{ap} and S_{bp}

Therefore, the commutation sequence must be carefully designed and properly executed. Various methods have been developed for a matrix converter to fulfill the commutation requirements. In [42], with the help of snubbers or clamping circuits, the dead time is inserted during the transition. This method is unpreferable because it can cause high commutation losses, and the snubber design is complicated. In 1989, Nandor Burany proposes a four-step commutation strategy for bidirectional switches [43], which selects the commutation sequence depends on the load current direction. Besides, the commutation sequence can be determined by the relative input voltage magnitude [44-45]. After that, multiple-step commutation strategies are widely used, and many improvements are made. The commutation sequences in current-based commutation strategy and voltage-based commutation strategy are illustrated in detail as follows.

(1) Current -based Commutation Strategy

The current based commutation strategy relies on the current direction to determine the switching sequence [46]. Figure 1.11 shows the schematic of

bidirectional switches and switching state sequence when S_{ap} (constructed by S_{ap1} and S_{ap2}) switches to S_{bp} (constructed by S_{bp1} and S_{bp2}). Each step is illustrated in detail by assuming the current direction is positive.

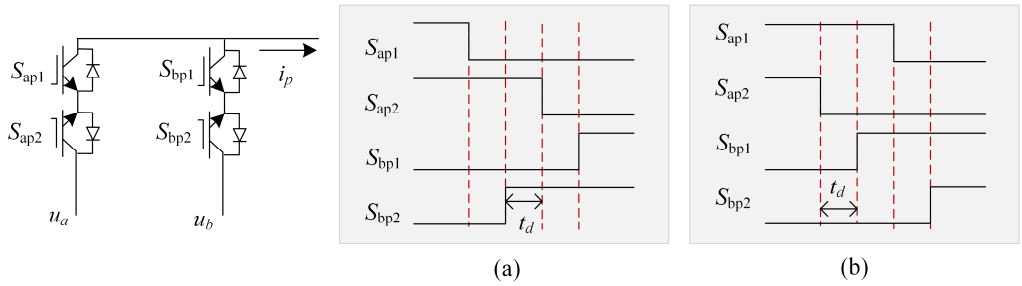


Figure 1.11 The four-step current based commutation strategy (a) i_p>0 (b) i_p<0

Step 1: In a steady state, both S_{ap1} and S_{ap2} are turned on to allow current flow. When S_{ap} switch to S_{bp} is required, S_{ap1} is turned off and the current flows through S_{ap2} and the diode of S_{ap1}.

Step 2: The S_{bp2} is turned on without causing a phase-to-phase short circuit. Depending on the voltage sign, the current flows through S_{ap2} and the diode of S_{ap1} or S_{bp2} and the diode of S_{bp1}.

Step 3: The S_{ap2} is turned off without causing overvoltage due to the current flows through S_{bp} now.

Step 4: The S_{bp1} is turned on to finish the process.

This process allows the current to commutate from one switch to another without generating overcurrent and overvoltage. The delay time between each switching state is determined by the device characteristics, and an interval time t_d is inserted between each commutation step. Hence, the commutation time (T_c) is equal to $3t_d$.

(2) Voltage-based Commutation Strategy

In the voltage-based commutation strategy, the relative magnitude of AC voltages is used to determine the commutation sequence [47]. Figure 1.12 shows the switching sequences of the four-step voltage-based commutation strategy when S_{ap} switches to S_{bp}.

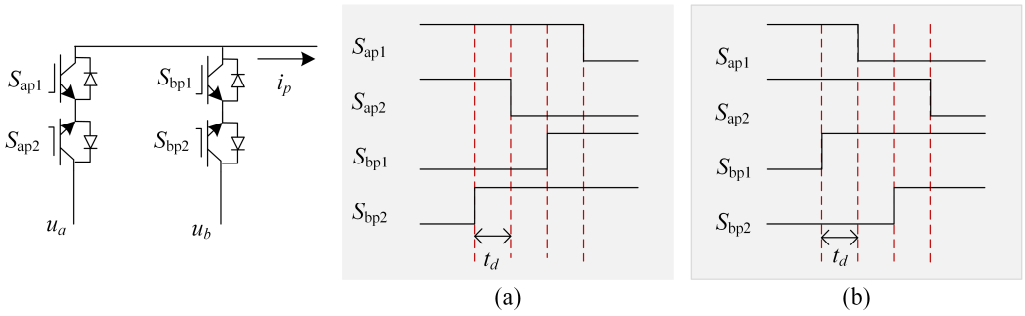


Figure 1.12 The four-step voltage-based commutation strategy (a) $u_a > u_b$ (b) $u_a < u_b$

Initially, S_{ap1} and S_{ap2} are turned on to allow current flow, while the S_{bp1} and S_{bp2} are turned off. The step detail is given as follows when $u_a > u_b$.

Step 1: The S_{bp2} is turned on due to this switch is not required to block voltage to avoid a phase-to-phase short circuit. The current is flowing through S_{ap1} and S_{ap2}.

Step 2: S_{ap2} is turned off. Depending on the current direction, it can flow through the S_{ap1} and the diode of S_{ap2} or S_{bp2} and the diode of S_{bp1}.

Step 3: The third step is to turn on S_{bp1}. The current flows through S_{bp}.

Step 4: At last, S_{ap1} is turned off to complete the commutation process.

By removing the first and last steps, a two-step voltage-based commutation strategy is achieved to reduce the commutation time [48]. In a steady state, the redundant switches are turned on, these switches will not cause a short circuit of input phases and provide a freewheeling path for the inductor.

(3) Hybrid Commutation Strategy

A hybrid commutation strategy that rotates the voltage-based commutation strategy and current-based commutation strategy in one fundamental period is proposed in [49-50]. This strategy relies on both the current direction and relative magnitude of input voltages to realize a three-step commutation strategy or one step commutation strategy [51].

1.3.2 PWM Methods

(1) Non-isolated AC-DC Matrix Converter

The non-isolated AC-DC matrix converter is reduced from a three-phase to three-phase matrix converter. Therefore, some conventional three-phase to three-

phase modulation strategies can be reduced into three-to-single and they can be applied in non-isolated AC-DC matrix converter, such as AlesinaVenturini [52], SPWM [53], and SVM modulation methods [54]. Among them, the SVM method is the most widely used strategy due to additional freedom in optimizing zero state placement. These modulation strategies focus on improving AC current quality or reducing DC current ripple. As harmonics may harm the lifetime of the power components and reduce conversion efficiency, they are constrained by grid codes. Also, the DC current ripples can impact AC current harmonics in the non-isolated AC-DC matrix converter and the DC ripples are harmful to the loads or DC sources as well. Considering double-sided symmetric switching patterns has better performance than single-sided switching pattern, seven SVM strategies are introduced in [55] to ensure AC current quality. Also, the DC current ripples are analyzed with different zero vector arrangement. [56] proposes an SVM strategy to reduce the current ripple by selecting properly active vectors based on the output voltage range. [57-58] use three line-to-line voltages in each switching cycle to synthesize the DC voltage, the DC current ripple is reduced by reducing the longest duty cycle of the largest active vector. However, these methods are applicable when the power factor is unity.

(2) Isolated AC-DC Matrix Converter

Except for the 3-1 MC in the non-isolated AC-DC matrix converter, the isolated AC-DC matrix converter contains an HFT and an H-bridge rectifier constructed by active switches or diodes. Due to different structures and operation principles, the modulation strategies are different from the non-isolated AC-DC matrix converter.

The isolated AC-DC matrix converter has extra four active switches in the H-bridge and the DC side output is connected to the filter capacitor. The primary voltage of HFT is constructed by line-to-line voltage, while the secondary voltage is made up of the DC voltage. Moreover, the voltages of the two sides should have a phase shift angle to transfer power. Simultaneously, the 3-1 MC and H-bridge are coupled due to the omittance of the intermediate energy storage component. In [59], the authors propose a modulation strategy for an isolated AC-DC matrix converter.

However, the duty cycle is calculated based on the rectangular approximation. Significant harmonic distortions present in the AC current. To reduce the low order harmonics, [60-61] use a trapezoidal current approximation for duty compensation. The harmonics distortions are reduced (for example, the seventh-order harmonic is reduced from 11% to 5.2%) but the current waveform still fails to meet the grid codes [62]. To improve the AC current quality, an SVM strategy is proposed in [63]. High quality current can be achieved, but the number of switching actions in both 3-1 MC and H-bridge is increased without soft switching features. This leads to low efficiency. To achieve higher efficiency with soft switching, [64] presents a new modulation method, which loses the buck type rectifying feature. In other words, the peak value of the line-to-line voltage must be smaller than the DC voltage. In this case, the matrix converter will lose one of its important advantage -- the voltage step down ability at the 3-1 MC stage. Making it worse, the transferred power is limited in a small range to ensure soft switching.

For unidirectional isolated AC-DC matrix converter, the active switches in the H-bridge rectifier are replaced by four diodes, and the DC side output is connected to a filter inductor instead of a capacitor. There is no phase shift angle between the two sides of HFT, but the duty cycle loss is a significant challenge in such topology. [65] introduces a six-segment SVM strategy, but the AC current is distorted by duty cycle loss. Because the leakage inductor existence requires transition time to allow the primary current to change polarity. To improve the AC current quality, duty cycle loss is compensated in [66]. Besides, many modulation methods focus on reducing DC current ripple in unidirectional isolated AC-DC matrix converters. [67] uses an eight-segment SVM strategy for unidirectional isolated matrix converter to achieve soft switching. However, at each sector broader, the DC current ripple is higher than that in the six-segment SVM strategy. Through optimizing the distribution time of the zero vector in the eight-segment SVM strategy, the DC current ripple can be reduced in [68]. Comparing these SVM sequences, [69] proposes an optimal six-segment SVM strategy for unidirectional isolated AC-DC matrix converter considering the DC current ripple and number of switching actions.

1.4 Challenges in AC-DC Matrix Converters

1.4.1 Communication Challenge in AC-DC Matrix Converter

The major challenges for the AC-DC matrix converter are the commutation safety and the current quality.

As illustrated, the commutation process is essential in AC-DC matrix converters for safety operation. When a different switching vector is applied to the converter, multi-step commutation must be performed to avoid short circuits of the AC side and open circuits of the DC side. Since the widely used multi-step commutation methods usually require a long commutation time, the possibility of narrow pulse, which is narrower than the commutation time, is increased. Hence, commutation failure is a significant concern. To ensure successful commutations, the narrow pulses in PWM should be extended to be long enough to finish commutation or directly eliminated. Hence, the extra procedure is needed for the PWM schemes to cope with the narrow pulses. Besides, the long commutation time itself can cause the current distortion due to the mismatch of the expected duty cycle and the actual duty cycle. Through extending or eliminating the narrow pulses, the actual duty cycle is greater or smaller than expected while the expected duty cycle is calculated to produce sinusoidal currents. This also worsens the current distortions.

Besides the common challenges, each converter has its challenge which is illustrated as follows.

1.4.2 Multiple Objectives Control Challenge in Non-isolated AC-DC Matrix Converter

In addition to the commutation challenge, multiple objectives control is another challenge for a non-isolated AC-DC matrix converter. The AC and DC sides are connected by switches, so the AC and DC currents are coupled directly. In such a converter, the control strategy of the non-isolated AC-DC matrix converter should simultaneously regulate the AC current and DC current, achieve sinusoidal current waveform, unity power factor, and desired DC current. However, realizing these targets simultaneously is not easy. [56] employs the widely used proportional

integral (PI) controller to regulate DC current while the power factor is uncontrolled. As a result, the CL filter of the converter induces an inherent phase shift between the grid currents and grid voltages, which results in a non-unity power factor. To control the power factor directly, besides the DC current control loop, a PI controller is added in [70] and [71] to control the phase angle of the grid current. However, the angle is sensitive to errors caused by the digital sampling process, and the control strategy is complex due to the need of designing multiple controllers.

1.4.3 Modulation Challenges in Isolated AC-DC Matrix Converters

Except for the 3-1 MC, the isolated AC-DC matrix converter contains an H-bridge which is built by four active switches or diodes. Therefore, both the operation principles and modulation strategies are different from the non-isolated AC-DC matrix converter.

An important challenge of isolated AC-DC matrix converter is to design proper commutation schemes for the 3-1 MC. Generally, multiple-step commutation strategies based on the knowledge of the current direction or relative magnitude of filter capacitor voltages can be used. As the isolated AC-DC matrix converter has a high frequency AC current at the HFT side, only the voltage-based commutation method is suitable. However, when the voltage magnitudes of the two phases are close, the relative magnitude is difficult to discriminate in practice due to the sensor errors and sampling noises. Therefore, the wrong commutation sequence may be selected and result in current distortion or even device damage.

The PWM design is another challenge due to the functional complexity of 3-1 MC. The 3-1 MC part combines the functions of an AC-DC matrix converter and an H-bridge. Therefore, it needs to regulate the AC current quality while performing power transfer control. To transfer power between two sides of HFT, the primary voltage and secondary voltage must be phase-shifted. As a result, the PWM methods developed for the AC-AC matrix converter or non-isolated AC-DC matrix converter cannot be directly applied for this topology. Coordination is required among PWM signals for H-bridge and 3-1 MC. Moreover, due to the omittance of

intermediate energy storage components, the phase currents are not synthesized by constant DC current, requiring a well designed PWM scheme to avoid distortions.

The isolated AC-DC matrix converter is easy to be scaled up by parallel connections without circulating current issues. In addition to the increased power capacity or wide voltage level, the modular structures can be interleaved to achieve good current quality. However, it is not so straight forward to do so and requires some research to best utilize the circuit modularity and achieve better performance. To realize the modularity in both circuit and control levels, a modular PWM scheme shall be developed. Taking the parallel unidirectional isolated AC-DC matrix converters as an example, the DC current ripple minimization can reduce the filter inductor size and then reduce the converter weight. There are two methods to reduce the DC current ripple- increasing the switching frequency or optimizing the modulation method. However, the former way has constraints as switching frequency is limited by the commutation duty ratio (higher commutation duty ratio, higher current distortion), or by thermal requirements (higher switching frequency, higher switching losses). Therefore, optimizing modulation is preferable. Furthermore, due to interleaved PWM can well mitigate the current ripples, the carrier-based modulation strategy should be researched. To design a modular interleaved PWM for unidirectional isolated AC-DC matrix converters, the PWM shall have the following features: firstly, the PWM pattern cannot be symmetrical in one PWM cycle, as a symmetrical pattern can lead to the same sequence when two converters are interleaving, losing the benefits of the interleaved operation; secondly, the duty cycle loss should be compensated because the necessary change of primary current's direction can lead to duty cycle loss, degrading the current quality.

1.5 Thesis Objectives

The overall objective of this thesis is to deal with the challenges in modulation and control strategies for AC-DC matrix converters.

Firstly, the multiple objectives control challenge in non-isolated AC-DC matrix converters is addressed. Considering the difficulties in multiple objectives

control and narrow pulse issue, the FCS-MPC is proposed for the non-isolated AC-DC matrix converter. This method does not need a modulation scheme and can directly control the AC and DC current at the same time.

Then, the challenges in isolated AC-DC matrix converters are addressed. As the AC current is no longer synthesized by constant DC current, the AC current is distorted in conventional modulation methods. To improve AC current quality, two modulation strategies are proposed for the isolated AC-DC matrix converter which can be used in different commutation duty ratio conditions. Moreover, a coordinated control scheme is proposed to reduce current stress and improve efficiency. Finally, an interleaved PWM method is proposed to reduce DC current ripples for parallel unidirectional isolated AC-DC matrix converters. Due to the HFT can eliminate the circulating current path, unidirectional isolated AC-DC matrix converters are easy to be operated in parallel. Thus, an interleaved SPWM is developed for easy implementation of parallel converters.

A summary of the research objectives addressed in each chapter is listed here.

Chapter 2 proposes an FCS-MPC for the non-isolated AC-DC matrix converter. Considering the coupling of AC current and DC current, and the requirement on safe commutation, the FCS-MPC, featuring multiple objectives capability and direct generation of gating signals without PWM scheme, is very suitable for this topology. With the proposed method, fast transient performance can be obtained. Besides, several virtual space vectors (formed by real space vectors) are used to improve the current quality without increasing sampling frequency.

Chapter 3 proposes a new SVM strategy for isolated AC-DC matrix converter. The commutation strategy relies on the relative magnitude of the filter capacitor's voltage to determine the commutation sequence. However, sensor errors and sampling noises can lead to wrong selections of the commutation sequences, leading to commutation failure. In the proposed SVM, the commutation will always happen between two phases with significant differences in magnitude. Meanwhile, a two-step commutation strategy and optimized zero vectors are used to reduce

narrow PWM pulses, ensuring the gating signals are long enough to finish the commutation procedures and the phase current quality is improved. The proposed modulation method can reduce the effect of commutation time on current quality, so it can achieve sinusoidal current even the commutation duty ratio is relatively large.

Chapter 4 focuses on reducing the low order harmonics of conventional modulation methods for isolated AC-DC matrix converter. With the development of fast switching semiconductors, the switching time is reduced significantly, and the switching frequency is not very high to avoid high switching losses. Therefore, the commutation effect on current quality is reduced. Under this condition, this chapter proposes an SVM strategy with reduced switching actions. Through improving the switching sequence and the distribution of zero vectors, the low order harmonics in conventional modulation strategies are reduced. Moreover, the existing control schemes fail to coordinate the modulation index and phase shift angle, and instead focus on optimizing one of the two variables. This can cause high current stress on the HFT, leading to low efficiency under a light load condition. Therefore, a coordination control of the modulation index and phase shift angle is proposed in this chapter to reduce the current stress.

Chapter 5 introduces a modular structure of unidirectional isolated AC-DC matrix converter to increase power rating and proposes an interleaved SPWM to reduce DC current ripples. In this chapter, a new SPWM strategy is proposed to obtain all the benefits from the interleaving of converters. The PWM pattern is carefully designed and duty cycle loss is compensated. As a carrier-based modulation method, it has good scalability for parallel converters.

Chapter 6 concludes the thesis and discusses future work.

Chapter 2

FCS-MPC for Non-isolated AC-DC Matrix Converter with Virtual Space Vectors

Considering long commutation time is required to ensure safe commutation, and the AC current and DC current is coupled, multiple objectives controllers are more suitable for the non-isolated AC-DC matrix converter. Model predictive control (MPC) is a promising option as it is easy to implement, and has fast dynamic responses [72-74]. In particular, the FCS-MPC [75-76] can select the optimal switching vector and apply it for one sampling period. The PWM scheme is no longer needed. The safe commutation can always be ensured without any extra procedures to check if the pulse duration is long enough for commutation, which is mandatory for PWM modulator based control methods [77]. Also, the errors of all the control variables can be taken into account when selecting the switching vector. In this case, the requirements of both the AC side and DC side can be fulfilled without using multiple controllers.

In conventional FCS-MPC, based on the minimum cost of the cost function, the optimal vector is applied in each sampling period. Generally, high sampling frequencies are required to achieve high performance. However, high sampling frequencies can lead to a high computation burden, expensive hardware devices, and a higher possibility to sample unexpected noises, which might be limited in practice [78]. To improve the performance of conventional FCS-MPC, virtual space vectors with duty cycle control is applied in [79-80]. By combining zero vectors and active vectors with different duty cycles, the virtual space vectors with different

---

Publication out of this Chapter:

F. Fang, H. Tian and Y. Li, "Finite Control Set Model Predictive Control for AC−DC Matrix Converter with Virtual Space Vectors," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 616-628, Feb. 2021.

amplitudes are generated. However, these methods cannot be applied to the non-isolated AC-DC matrix converter as the variable duty cycle can lead to narrow pulses, causing commutation failure. Also, large numbers of virtual space vectors (>100 in [81-82], >100000 in [83]) synthesized by discrete space vector modulation (DSVM) are used to balance neutral point voltage or obtain fixed switching frequency. These methods are not applicable to the non-isolated AC-DC matrix converter as well. On one hand, the computation burden is heavy, and the deadbeat technique based vector preselection method cannot be applied in the non-isolated AC-DC matrix converter. On the other hand, with the high number of virtual space vectors, narrow pulses are caused. The numbers of virtual space vectors are reduced (<36) in [84-87], where the sign of current reference is used to preselect vectors. The narrow pulses may be avoided in this method, but the vector preselection method is not suitable for the non-isolated AC-DC matrix converter, whose AC current and DC current should both be considered.

In this chapter, an FCS-MPC with virtual space vectors for non-isolated AC-DC matrix converter is proposed, which has the following advantages: (1) both the AC current and DC current quality are considered in the cost function, making it possible to simultaneously achieve sinusoidal AC current and smooth DC current; (2) the virtual space vectors are used to further enhance the power quality without increasing the sampling frequency; (3) as the optimal switching vector is directly selected, narrow pulses can be avoided without using complicated PWM method; (4) fast transient can be obtained. Besides, considering the FCS-MPC is usually sensitive to model errors, the effects of parameter mismatch are investigated in this chapter. The design guidance to enhance the robustness is provided.

2.1 Modeling of Non-isolated AC-DC Matrix Converter

2.1.1 Operation of Non-isolated AC-DC Matrix Converter

The detailed topology of the non-isolated AC-DC matrix converter is shown in Figure 2.1. It is made up of six bi-directional switches, which can conduct current in both directions. The bidirectional switches are built by IGBTs connected in common-emitter (common-E). For example, S_{ap} is made up of S_{ap1} and S_{ap2}.

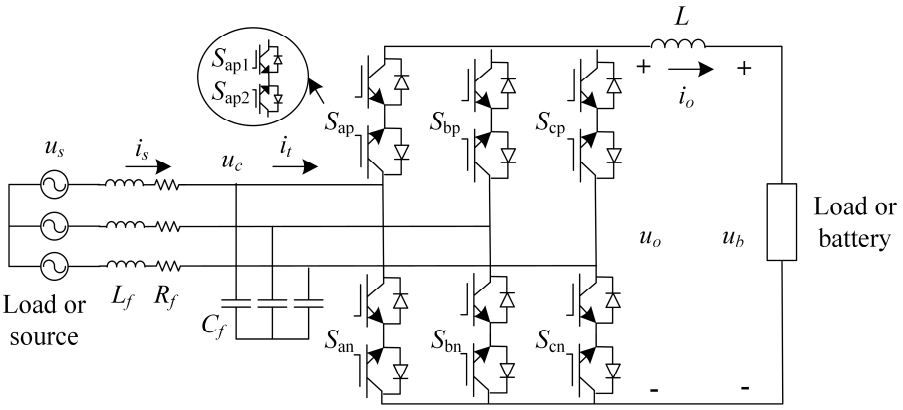


Figure 2.1 Topology of the non-isolated AC-DC matrix converter

At any time, only one bidirectional switch must be turned on in the three upper-arms and only one bidirectional switch must be turned on in the three lower-arms to avoid overvoltage and overcurrent. The switching function of each bidirectional switch is defined in (2.1) and the constraints are presented in (2.2).

$$S_{xy} = \begin{cases} 1 & \text{turn on} \\ 0 & \text{turn off} \end{cases} \quad x = \{\text{a,b,c}\} \quad y = \{\text{p,n}\} \tag{2.1}$$

$$\begin{aligned} S_{ap} + S_{bp} + S_{cp} &= 0 \\ S_{an} + S_{bn} + S_{cn} &= 0 \end{aligned} \tag{2.2}$$

Based on the constraints, there are nine vectors for the non-isolated AC-DC matrix converter, as shown in Table 2.1.

Table 2.1 Real Space Vectors in Non-isolated AC-DC Matrix Converter

Space vectors	Switching states						DC voltage u_o
	S_{ap}	S_{an}	S_{bp}	S_{bn}	S_{cp}	S_{cn}	
I_1	1	0	0	1	0	0	u_{ab}
I_2	1	0	0	0	0	1	u_{ac}
I_3	0	0	1	0	0	1	u_{bc}
I_4	0	1	1	0	0	0	u_{ba}
I_5	0	1	0	0	1	0	u_{ca}
I_6	0	0	0	1	1	0	u_{cb}
I_7	1	1	0	0	0	0	0
I_8	0	0	0	0	1	1	0
I_9	0	0	1	1	0	0	0

In practice, the rising/falling time and delay of the switching action should be considered. To achieve a reliable commutation operation, a four-step current-based

commutation strategy is applied in the non-isolated AC-DC matrix converter. However, it requires $3t_d$ to complete the commutation process. When the PWM pulse width is narrower than $3t_d$, the commutation will fail. To solve this problem, the narrow pulse can be either eliminated or extended to $3t_d$ to complete the commutation. To avoid the narrow pulse, FCS-MPC is a promising option for a non-isolated AC-DC matrix converter as the vectors can be designed and directly generated by FCS-MPC.

2.1.2 Discrete-time Model of the Converter

To develop FCS-MPC for the non-isolated AC-DC matrix converter, the system model should be built to predict the behavior and select the proper switching vector. In this section, the continuous time model of the non-isolated AC-DC matrix converter will be built and then be discretized. In the modeling procedure, the non-isolated AC-DC matrix converter is assumed to be time invariant.

In Figure 2.1, u_s denotes the grid voltage, i_s denotes the grid current, u_c denotes the filter capacitor voltage, and i_t denotes the current of the converter. These voltages and currents are three-phase variables and presented as

$$\begin{aligned} \mathbf{u_s} &= [u_{sa}, u_{sb}, u_{sc}]^T \\ \mathbf{i_s} &= [i_{sa}, i_{sb}, i_{sc}]^T \\ \mathbf{u_c} &= [u_{ca}, u_{cb}, u_{cc}]^T \\ \mathbf{i_t} &= [i_{ta}, i_{tb}, i_{tc}]^T \end{aligned} \tag{2.3}$$

The CL filter is used to prevent overvoltage and eliminate high order harmonics of the grid current. The dynamic model is

$$\begin{aligned} L_f \frac{d\mathbf{i}_s}{dt} &= \mathbf{u_s} - \mathbf{u_c} - R_f \mathbf{i_s} \\ C_f \frac{d\mathbf{u_c}}{dt} &= \mathbf{i_s} - \mathbf{i_t} \end{aligned} \tag{2.4}$$

where L_f, R_f, and C_f are the filter inductor, parasitic resistor, and capacitor.

For the non-isolated AC-DC matrix converter, DC voltage of the converter u_o is obtained as a function of switching states and u_c,

$$u_o = \begin{bmatrix} S_{ap} - S_{an} & S_{bp} - S_{bn} & S_{cp} - S_{cn} \end{bmatrix} \mathbf{u_c} \tag{2.5}$$

Also, the current i_t can be expressed by DC current i_o and switching states

$$\mathbf{i_t} = \begin{bmatrix} S_{ap} - S_{an} & S_{bp} - S_{bn} & S_{cp} - S_{cn} \end{bmatrix}^T i_o \quad (2.6)$$

The dynamic model of the DC side filter is shown in (2.7).

$$L\frac{di_o}{dt} = u_o - u_b \quad (2.7)$$

where L is the filter inductor on the DC side; u_b is the DC load voltage or battery voltage.

Using the forward Euler method, the continuous time model of the CL filter can be discretized as

$$\begin{aligned} \mathbf{i_s}(k+1) &= \frac{T_S}{L_f}\left(\mathbf{u_s}(k) - \mathbf{u_c}(k) - R_f\mathbf{i_s}(k)\right) + \mathbf{i_s}(k) \\ \mathbf{u_c}(k+1) &= \frac{T_S}{C_f}\left(\mathbf{i_s}(k) - \mathbf{i_t}(k)\right) + \mathbf{u_c}(k) \end{aligned} \quad (2.8)$$

where $i_s(k+1)$ and $u_c(k+1)$ are predicted values at $(k+1)^{th}$ sampling step, $u_s(k)$, $u_c(k)$, $i_s(k)$, $i_t(k)$ are values at k^{th} sampling step, T_S is the sampling time.

Similarly, (2.7) can be discretized as

$$i_o(k+1) = \frac{T_S}{L}\left(u_o(k) - u_b(k)\right) + i_o(k) \quad (2.9)$$

where, $i_o(k+1)$ is the predicted value; $i_o(k)$, $u_o(k)$ are the values at k^{th} sampling step;

Based on (2.8) and (2.9), the grid current i_s and DC current i_o in the next step can be predicted for given switching states and measured values.

2.2 FCS-MPC for Non-isolated AC-DC Matrix Converter

2.2.1 Virtual Space Vectors

Generally, FCS-MPC only utilizes nine switching vectors to calculate the cost function in one sampling period. Based on the minimum cost, the optimal switching vector can be selected and applied in the next sampling step. Due to the limited number of switching vectors, a high sampling frequency is typically needed to improve the performance. However, the sampling frequency is limited in practice. Instead of using only nine switching states to calculate the cost function, virtual space vectors can be taken into consideration when FCS-MPC searches the optimal

switching vector in each sampling period. Each virtual space vector is formed by two (or more) real space vectors with corresponding application time. Combining two different real space vectors with different dwell times in each PWM period, several virtual space vectors can be generated.

Considering two real space vectors form each virtual space vector, the general form of the virtual space vector is

$$\begin{aligned} I_{virtual} &= T_x I_x + T_y I_y \\ T_S &= T_x + T_y \\ I_x, I_y &\in \{I_1, I_2 \ldots I_9\} \, (I_x \neq I_y) \end{aligned} \tag{2.10}$$

where I_{virtual} is the virtual space vector; I_{x}, I_{y} are real space vectors; T_{x} and T_{y} are dwell times of I_{x} and I_{y}, respectively.

The more virtual space vectors are applied, the better performance can be achieved. However, using too many virtual space vectors can also contribute to large computation burdens, making it hard to implement in commercial digital controllers, such as a digital signal processor (DSP). In this chapter, virtual space vectors are formed by only two real space vectors with $0.5T_S$ dwell time. As a result, 12 virtual space vectors and 9 real space vectors are applied, as shown in Figure 2.2.

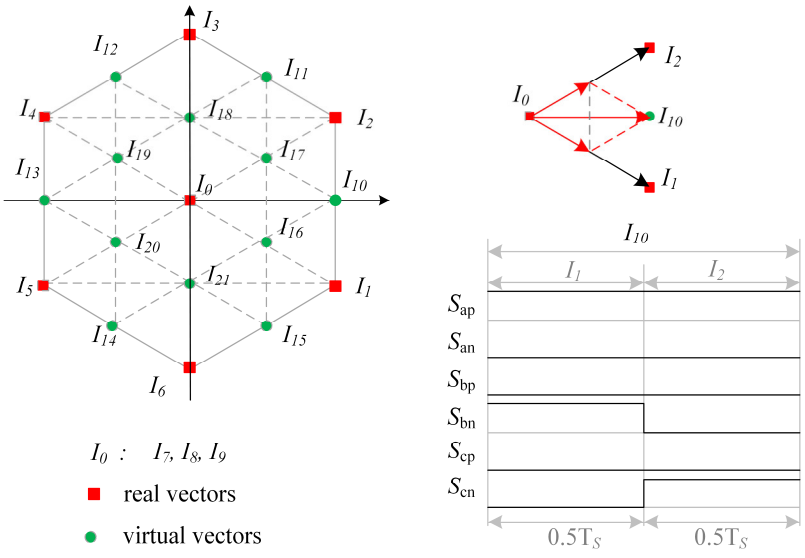


Figure 2.2 Space vectors for non-isolated AC-DC matrix converter

The virtual space vector formation and corresponding average DC voltage are shown in Table 2.2, where I_1 to I_9 are real space vectors and I_{10} to I_{21} are virtual

space vectors. For example, I_{10} is formed by I_1 and I_2 with the dwell times are $0.5T_S$. When I_{10} is selected, the switching vectors I_1 and I_2 are applied for half of the sampling period, respectively.

Table 2.2 Virtual Space Vectors Formation

Virtual space vectors	Formation	DC voltage u_o
I_{10}	$0.5I_1+0.5\ I_2$	$1.5u_a$
I_{11}	$0.5I_2+0.5\ I_3$	$-1.5u_c$
I_{12}	$0.5I_3+0.5\ I_4$	$1.5u_b$
I_{13}	$0.5I_4+0.5\ I_5$	$-1.5u_a$
I_{14}	$0.5I_5+0.5\ I_6$	$1.5u_c$
I_{15}	$0.5I_6+0.5\ I_1$	$-1.5u_b$
I_{16}	$0.5I_1+0.5\ I_0$	$0.5u_{ab}$
I_{17}	$0.5I_2+0.5\ I_0$	$0.5u_{ac}$
I_{18}	$0.5I_3+0.5\ I_0$	$0.5u_{bc}$
I_{19}	$0.5I_4+0.5\ I_0$	$0.5u_{ba}$
I_{20}	$0.5I_5+0.5\ I_0$	$0.5u_{ca}$
I_{21}	$0.5I_6+0.5\ I_0$	$0.5u_{cb}$

The cost function represents the evaluation criteria used to select the optimal switching vector in the next sampling step. For every sampling step, the cost function is calculated for each possible switching vector. The one with the minimum cost is the optimal switching vector and will be applied in the next sampling step.

The cost function is formed by the desired references and predicted values, defined as (2.11).

$$\begin{aligned} g &= \lambda_1 g_1 + \lambda_2 g_2 + ... + \lambda_n g_n \\ g_i &= f\left(x^*\left(k+1\right), x\left(k+1\right)\right) \end{aligned} \qquad (2.11)$$

where i=1,2…n. n is the number of control objectives; $x^*(k+1)$ is the future reference value and $x(k+1)$ is the predicted value; λ_n is the weighting factor, which presents the relative importance of each control objective.

For the non-isolated AC-DC matrix converter, the grid current and DC current should be controlled simultaneously. To eliminate the steady state errors, the grid current and DC current should track their references as close as possible. The cost function is presented in (2.12).

$$g=\lambda_1\left(\left(i_{s\alpha}^{*}\left(k+1\right)-i_{s\alpha}\left(k+1\right)\right)^2+\left(i_{s\beta}^{*}\left(k+1\right)-i_{s\beta}\left(k+1\right)\right)^2\right)+\lambda_2\left|i_o^{*}\left(k+1\right)-i_o\left(k+1\right)\right| \tag{2.12}$$

where i_s*(k+1) is grid current reference and i_s(k+1) is predicted grid current; i_o*(k+1) is DC current reference and i_o(k+1) is predicted DC current;

In FCS-MPC, both grid current and DC current are considered to obtain satisfactory results. Their weighting factors are therefore designed to present their priority. In different applications, the weighting factor can be adjusted according to different requirements.

The input active power, reactive power, and output active power can be calculated as (2.13). When the power flows from the AC side to the DC side, the input active power and output active power has the following relationship, as (2.14)

$$\begin{aligned} P_{in}^{*}&=\frac{3}{2}\left(u_\alpha i_\alpha^{*}+u_\beta i_\beta^{*}-R_f i_\alpha^{*2}-R_f i_\beta^{*2}\right)\\ Q^{*}&=\frac{3}{2}\left(-u_\alpha i_\beta^{*}+u_\beta i_\alpha^{*}\right)\\ P_o^{*}&=i_o^{*2}R \end{aligned} \tag{2.13}$$

$$P_o^{*}=\eta P_{in}^{*} \tag{2.14}$$

where i_o* is the DC current reference, R is the DC load resistor, and Q* is the reactive power reference, η is the efficiency of the converter. If the DC side is connected to a DC source or battery, the active power reference in (2.14) needs to be modified as P_o*=$u_b i_o$*. Therefore, the reference current can be calculated as (2.15).

$$\begin{aligned} i_\alpha^{*}&=\frac{2Q^{*}u_\beta}{3\left(u_\alpha^2+u_\beta^2\right)}+\frac{u_\alpha}{2R_f}-\frac{u_\alpha\sqrt{9\left(u_\alpha^2+u_\beta^2\right)^2-16Q^{*2}R_f^2-24\left(u_\alpha^2+u_\beta^2\right)R_f u_{dc}P_o^{*}/\eta}}{6R_f\left(u_\alpha^2+u_\beta^2\right)}\\ i_\beta^{*}&=\frac{-2Q^{*}u_\alpha}{3\left(u_\alpha^2+u_\beta^2\right)}+\frac{u_\beta}{2R_f}-\frac{u_\beta\sqrt{9\left(u_\alpha^2+u_\beta^2\right)^2-16Q^{*2}R_f^2-24\left(u_\alpha^2+u_\beta^2\right)R_f u_{dc}P_o^{*}/\eta}}{6R_f\left(u_\alpha^2+u_\beta^2\right)} \end{aligned} \tag{2.15}$$

It can be found that the grid current reference is related to converter efficiency and the resistance of the input filter. When the efficiency is high and the parasitic

resistor is small, the effect can be neglected. The reference can also be calculated as (2.16).

$$P^* = i_o^{*2} R$$
$$i_{s\alpha}^* = \frac{P^* u_{s\alpha} + Q^* u_{s\beta}}{1.5\left(u_{s\alpha}^2 + u_{s\beta}^2\right)}; \quad i_{s\beta}^* = \frac{P^* u_{s\beta} - Q^* u_{s\alpha}}{1.5\left(u_{s\alpha}^2 + u_{s\beta}^2\right)} \qquad (2.16)$$

When the sampling time is sufficiently small compared with the dynamic behavior of the current reference, the current reference value $i_s^*(k+1)$ equal to $i_s^*(k)$ and $i_o^*(k+1)=i_o^*(k)$. Or the future reference can be estimated via an appropriate extrapolation method, described as $i^*(k+1)=2i^*(k)-i^*(k-1)$.

2.2.2 Delay Compensation

Based on the above analysis, it shows that each switching vector should be used to evaluate the cost function with their corresponding predicted values. Theoretically, the optimal switching vector with minimum cost can be selected instantly and applied, as shown in Figure 2.3(a). However, in real digital controllers, both the sampling process and control computation are not finished instantly. For example, if the controller samples the voltage and current at the k^{th} step, it needs one step to generate control signals. As a result, the control signal can only be applied at the $(k+1)^{th}$ step—introducing one step delay. During the one step delay, the previous switching vector is still used (as shown in Figure 2.3(b)), and control errors will be caused [88]. To compensate the one step control delay, the model predictive control shall predict system output at the $(k+2)^{th}$ step, not $(k+1)^{th}$ step, as shown in Figure 2.3(c). The first step predicts the status at $(k+1)^{th}$ sampling step based on the measured values and the applied switching vector at the k^{th} sampling step; the second step predicts the results at $(k+2)^{th}$ sampling step of every applicable vector based on the predicted values at $(k+1)^{th}$ sampling step, then the corresponding cost can be obtained. The optimal switching vector for $(k+2)^{th}$ sampling step is selected and applied at the $(k+1)^{th}$ sampling step. After compensating for the delay, the cost function is rewritten as (2.17).

$$g = \lambda_1 \left(\left(i^*_{s\alpha}(k+2) - i_{s\alpha}(k+2) \right)^2 + \left(i^*_{s\beta}(k+2) - i_{s\beta}(k+2) \right)^2 \right) + \lambda_2 \left| i^*_o(k+2) - i_o(k+2) \right| \quad (2.17)$$

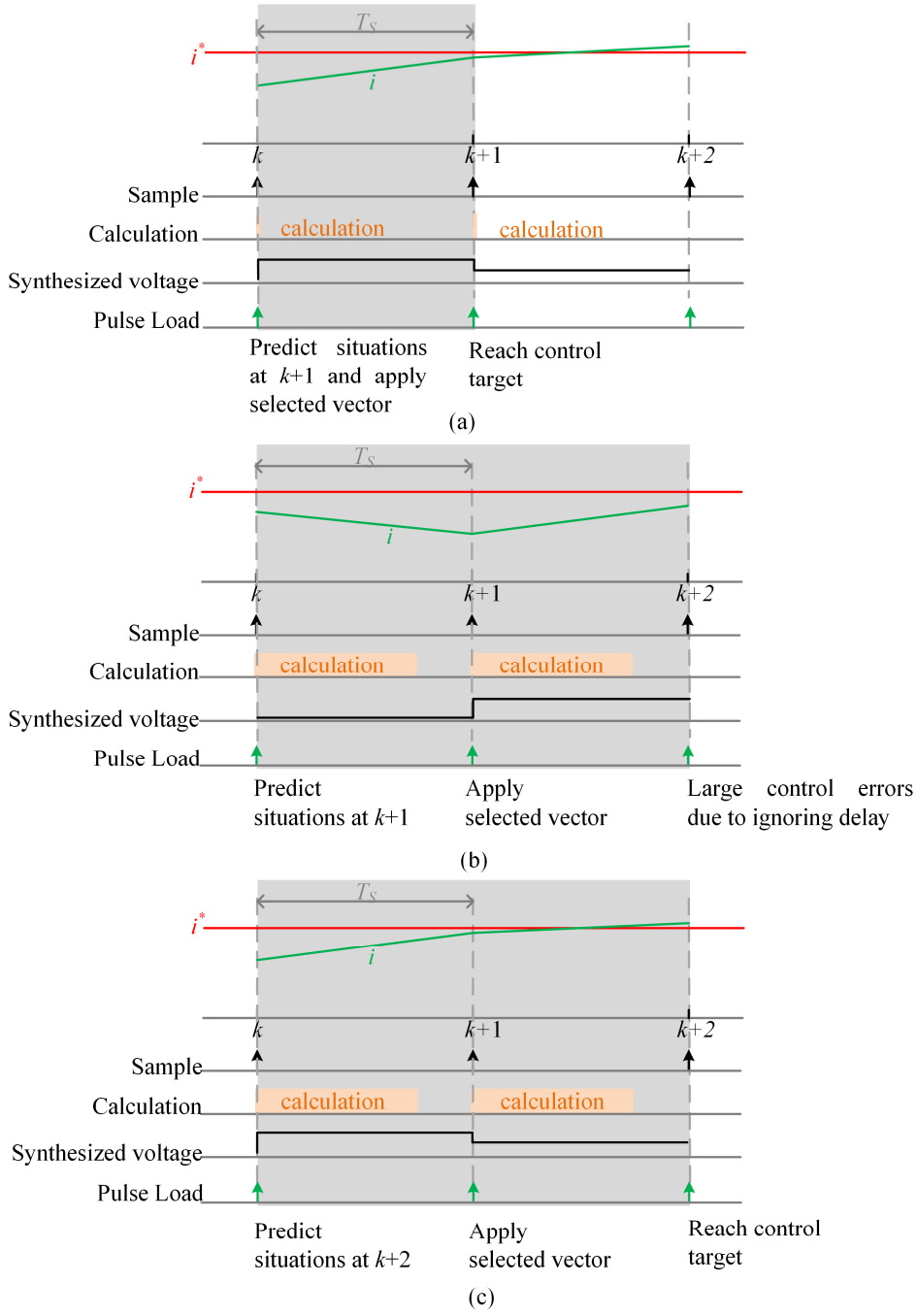


Figure 2.3 FCS-MPC operation (a) without delay (b) with delay and without compensation (c) with delay and with compensation

2.2.3 Vector Preselection

It is worth noting that the switching vectors can be preselected to reduce the computation burden. In the non-isolated AC-DC matrix converter, the DC voltage u_b is positive, in normal condition the output voltage of the converter u_o is not negative due to large DC current ripple and voltage ripple will be generated. Hence, these vectors which lead to negative u_o shall be excluded from the optimal vector as the voltage polarity shall not be inverted under any condition. It is unnecessary to evaluate AC current, DC current, and cost function yielded by 18 active vectors. Instead, by simply calculating the output voltage u_o, 8 out of 18 active vectors can be preselected. The computation burden is thus reduced significantly.

To demonstrate the procedure, an example is given in Figure 2.2, (1) calculate the output voltage of 6 real active vectors; (2) assuming the output voltages of I_1, I_2 and I_3 are positive; (3) therefore, the output voltage of I_{10}, I_{11}, I_{16}, $I_{17,}$ and I_{18} are positive (because they are constructed by the output voltages of I_1, $I_{2,}$ and I_3 or zero voltage); (4) finally, only 8 active vectors and zero vector are used to predict the AC and DC current values and then calculate the cost function. The vector with the lowest cost will be applied in each sampling period. When a virtual space vector is selected, two real space vectors will be applied in one switching period, e.g., I_2 and I_0 are applied for half-cycle to synthesize I_{17}. In this case, as the real space vectors will always be used for one cycle or half a cycle, the narrow pulses are avoided without sacrificing the output waveform quality.

2.2.4 Active Damping

The input CL filter can cause resonance and lead to distorted current. To suppress the resonance, a physical damping resistor can be added while it will bring extra power loss. Hence, active damping is applied in this section. The virtual damping resistor is assumed to be added in parallel with the input filter capacitor [89]. Because active damping only damping the harmonics without influencing the fundamental components, only the harmonic components of the filter capacitor are needed to calculate damping current, as (2.18).

$$i_{damp\_h} = \frac{u_{c\_h}}{\mathrm{R}_{damp}} \quad (2.18)$$

where u_{c_h} is the harmonic capacitor voltage of the input filter; R_{damp} is a virtual resistor in parallel with a filter capacitor.

The capacitor voltage contains a fundamental component and harmonic components, as shown in (2.19). Due to the grid voltage are provided by the AC source, it only contains the fundamental component. Therefore, the fundamental component of the filter capacitor voltage is calculated by (2.20).

$$u_c = u_{c\_1} + u_{c\_h} \quad (2.19)$$

$$u_{c\_1} = u_s - \left(R_f i_s + j\omega L_f i_s\right) \quad (2.20)$$

Based on (2.19) (2.20), the harmonic components of the filter capacitor voltage can be calculated by (2.21). The components are presented in αβ-frame as (2.22).

$$u_{c\_h} = u_c - \left(u_s - R_f i_s - j\omega L_f i_s\right) \quad (2.21)$$

$$\begin{aligned} u_{c\_h\alpha} &= u_{c\alpha} - \left(u_{s\alpha} - R_f i_{s\alpha} + \omega L_f i_{s\beta}\right) \\ u_{c\_h\beta} &= u_{c\beta} - \left(u_{s\beta} - R_f i_{s\beta} - \omega L_f i_{s\alpha}\right) \end{aligned} \quad (2.22)$$

Therefore, the new current references with active damping are expressed

$$\begin{aligned} i^*_{s\alpha\_d} &= i^*_{s\alpha} + \frac{u_{c\alpha} - \left(u_{s\alpha} - R_f i^*_{s\alpha} + \omega L_f i^*_{s\beta}\right)}{R_{damp}} \\ i^*_{s\beta\_d} &= i^*_{s\beta} + \frac{u_{c\beta} - \left(u_{s\beta} - R_f i^*_{s\beta} - \omega L_f i^*_{s\alpha}\right)}{R_{damp}} \end{aligned} \quad (2.23)$$

where $i^*_{s\alpha\_d}$ and $i^*_{s\beta\_d}$ are grid current references after adding a virtual resistor parallel with filter capacitor; $i^*_{s\alpha}$and $i^*_{s\beta}$ are calculated grid current reference based on (2.15) or (2.16);

2.2.5 Flowchart of the Proposed FCS-MPC Method

The proposed FCS-MPC with virtual space vectors control diagram of the non-isolated AC-DC matrix converter is shown in Figure 2.4. In this control scheme, the current control references for grid current are calculated by (2.15) or (2.16). With delay considered, the cost function will evaluate the cost of each applicable

vector. The optimal vector will be applied after the commutation sequence is inserted. The control scheme can also be concluded in detail as a flowchart shown in Figure 2.5.

At the beginning of the k^{th} sampling time, the grid voltage $u_s(k)$, grid current $i_s(k)$, filter capacitor voltage $u_c(k)$, DC current $i_o(k)$, DC voltage $u_b(k)$ are measured, and the switching vector at k^{th} sampling time is saved in memory. Then the grid current reference can be calculated in the second step. With the measured values and switching vector, the values of $i_o(k+1)$, $u_c(k+1)$, and $i_s(k+1)$ are predicted in the first step. To reduce the computation burden, the switching vectors are preselected--the switching vector to generate negative u_o will be neglected in the cost calculation. Then, the grid current and DC current at $(k+2)^{th}$ sampling step are predicted for each of the preselected switching vectors, which is the second step. Subsequently, the cost function can be calculated. The optimal switching vector which generates the minimum cost is selected and applied in the next sampling step after the commutation strategy.

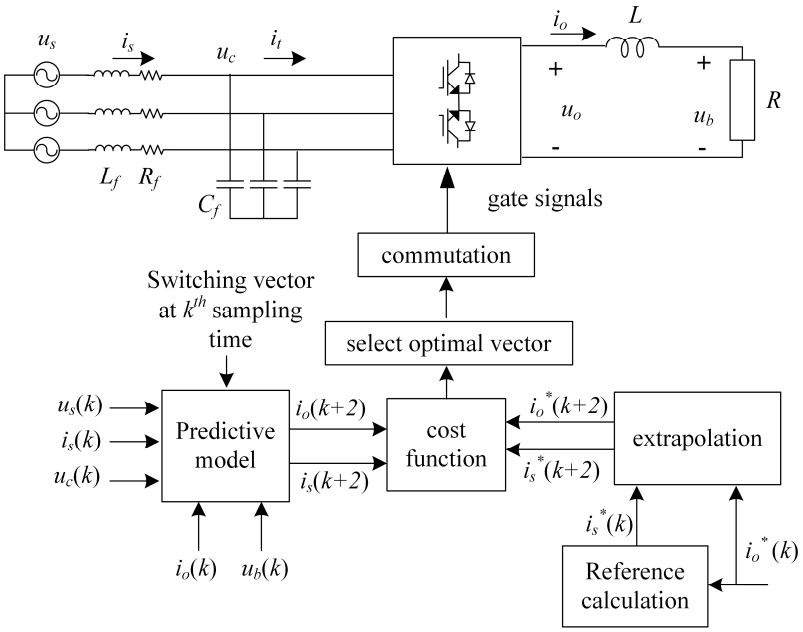


Figure 2.4 Control diagram of the proposed FCS-MPC with virtual space vectors for non-isolated AC-DC matrix converter

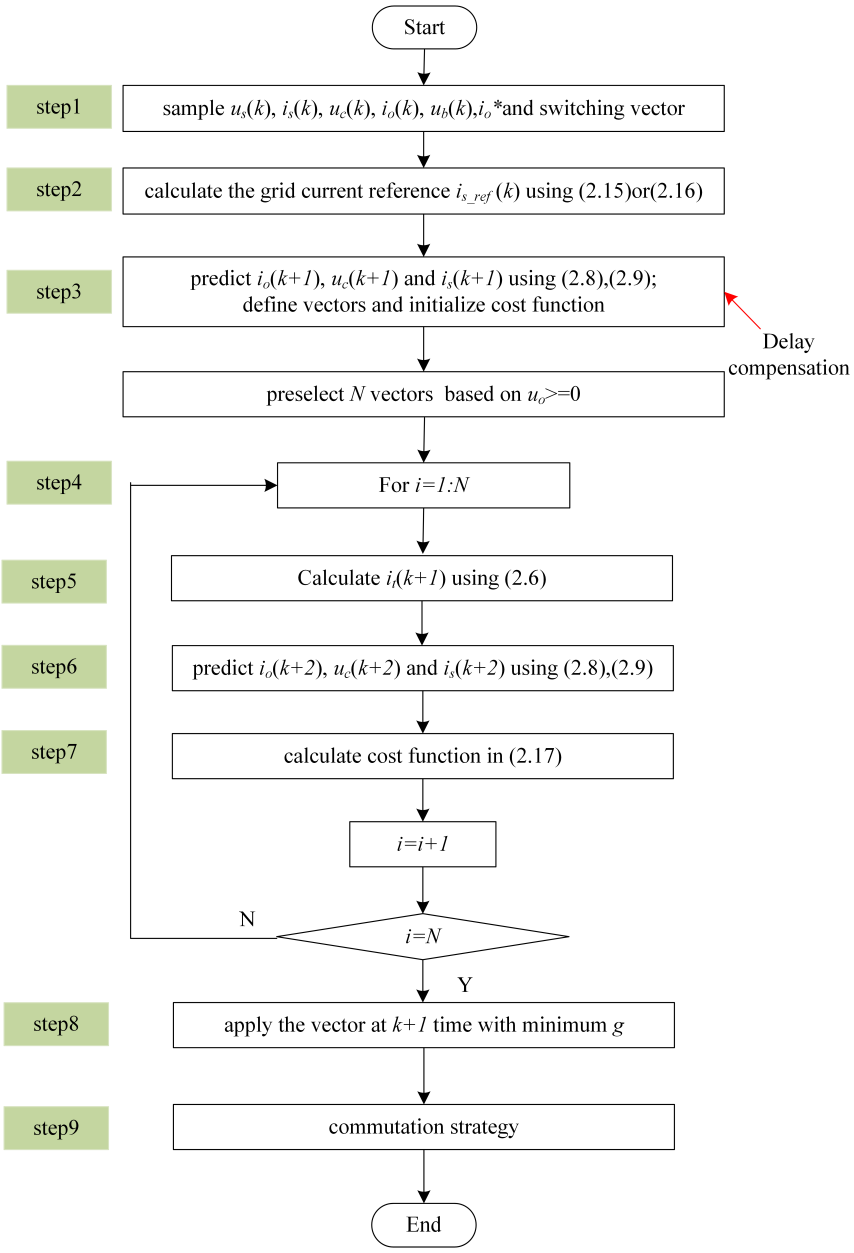


Figure 2.5 Flowchart diagram of the proposed FCS-MPC with virtual space vectors for non-isolated AC-DC matrix converter

Generally, control methods require a verification of the stability in close loop operation. However, the established methods used for linear systems cannot be applied for FCS-MPC methods. Moreover, the close loop stability analysis of FCS-MPC is difficult. To evaluate the FCS-MPC can prevent small disturbance can cause large variations, the most widely used method is analyzing the parameters mismatch performance to observe the response to model uncertainties. [90-91]. In FCS-MPC, the control variables are predicted based on modeled parameter values.

In practical application, the actual system parameter values may be different from the modeled parameter values, also these parameters can change under different conditions. The parameter variation can lead to concerns of control accuracy. Analyzing the effect of parameter mismatch is important for evaluating the control system's robustness.

In a non-isolated AC-DC matrix converter, the predicted grid current is related to the CL filter inductor, resistor, and capacitor. The DC current is influenced by the L filter inductor and load resistor. The modeled parameter values are L_f, R_f, C_f, L, and R. The actual system parameter values can be presented as $L_f+\Delta L_f$, $R_f+\Delta R_f$, $C_f+\Delta C_f$, $L+\Delta L$, and $R+\Delta R$ respectively, where Δ represents the uncertain component of each parameter.

With actual system parameter values, the predicted grid current and DC current are obtained,

$$\mathbf{i}_{\mathbf{s\_\,real}}\left(k+1\right)=\frac{T_S}{L_f+\Delta L_f}\left\{\begin{matrix}\mathbf{u}_{\mathbf{s}}\left(k\right)-\dfrac{T_S\left(\mathbf{i}_{\mathbf{s}}\left(k\right)-\mathbf{i}_{\mathbf{t}}\left(k\right)\right)}{C_f+\Delta C_f}\\ -\mathbf{u}_{\mathbf{c}}\left(k\right)-\left(R_f+\Delta R_f\right)\mathbf{i}_{\mathbf{s}}\left(k\right)\end{matrix}\right\}+\mathbf{i}_{\mathbf{s}}\left(k\right) \qquad (2.24)$$

$$i_{o\_real}\left(k+1\right)=\frac{T_S}{L+\Delta L}\left\{u_o\left(k\right)-i_o\left(k\right)\left(R+\Delta R\right)\right\}+i_o\left(k\right) \qquad (2.25)$$

The error is defined as the difference between the predicted values based on the modeled parameters and the actual values. The error of the grid current is shown in (2.26). The error of DC current is defined in (2.27).

$$\Delta\mathbf{i}_{\mathbf{s}}\Big|_{\Delta L_f}/\mathbf{i}_{\mathbf{s}}=\left|\left(\frac{T_S^2}{L_fC_f}+\frac{T_SR_f}{L_f}\right)\frac{\Delta L_f/L_f}{1+\Delta L_f/L_f}\right|\times100\% \qquad (2.26)$$

$$\Delta\mathbf{i}_{\mathbf{s}}\Big|_{\Delta C_f}/\mathbf{i}_{\mathbf{s}}=\left|\frac{T_S^2}{L_fC_f}\frac{\Delta C_f/C_f}{1+\Delta C_f/C_f}\right|\times100\% \qquad (2.27)$$

The grid current error, shown in (2.26), depends on three parts: (1) the measured grid voltage $u_s(k)$, capacitor voltage $u_c(k)$ and grid current $i_s(k)$; while the current $i_t(k)$ depends on the switching vector at k^{th} sampling step and measured DC current value $i_o(k)$; (2) sampling time T_S and modeled values of filter inductor L_f, resistor R_f, and capacitor C_f; (3) uncertain components of CL filter parameters, such

as ΔL_f, ΔR_f, and ΔC_f. To analyze the effect of the parameter mismatch of the CL filter, only the third part is considered. The errors (in percentage) of predicted grid current with respect to the CL filter inductor, filter capacitor, and parasitic resistor are presented in (2.28-2.30) respectively. The errors (in percentage) of predicted DC current with respect to the L filter inductor and load resistor are presented in (2.31-2.32) respectively.

$$\Delta \mathbf{i_s}\Big|_{\Delta R_f} / \mathbf{i_s} = \left| \frac{T_S R_f}{L_f} \frac{\Delta R_f}{R_f} \right| \times 100\% \tag{2.28}$$

$$\Delta i_o\Big|_{\Delta L} / i_o = \left| \frac{T_S R \Delta L}{L\left(L + \Delta L\right)} \right| \times 100\% \tag{2.29}$$

$$\Delta i_o\Big|_{\Delta R} / i_o = \left| \frac{T_S \Delta R}{L} \right| \times 100\% \tag{2.30}$$

$$\begin{aligned} \Delta \mathbf{i_s}\left(k+1\right) &= \left| \mathbf{i_s}\left(k+1\right) - \mathbf{i_{s\_real}}\left(k+1\right) \right| \\ &= \left| \begin{aligned} &-\left(\frac{T_S^2\left(L_f \Delta C_f + \Delta L_f C_f + \Delta L_f \Delta C_f\right)}{L_f C_f \left(L_f + \Delta L_f\right)\left(C_f + \Delta C_f\right)} + \frac{T_S\left(\Delta L_f R_f - L_f \Delta R_f\right)}{L_f\left(L_f + \Delta L_f\right)} \right) \mathbf{i_s}\left(k\right) \\ &+ \frac{T_S \Delta L_f \left(\mathbf{u_s}\left(k\right) \text{-} \mathbf{u_c}\left(k\right)\right)}{L_f\left(L_f + \Delta L_f\right)} + \frac{T_S^2\left(L_f \Delta C_f + \Delta L_f C_f + \Delta L_f \Delta C_f\right)}{L_f C_f \left(L_f + \Delta L_f\right)\left(C_f + \Delta C_f\right)} \mathbf{i_t}\left(k\right) \end{aligned} \right| \end{aligned} \tag{2.31}$$

$$\begin{aligned} \Delta i_o\left(k+1\right) &= \left| i_o\left(k+1\right) - i_{o\_real}\left(k+1\right) \right| \\ &= \left| \frac{T_S \Delta L}{L\left(L + \Delta L\right)} u_o\left(k\right) - \frac{T_S\left(R\Delta L - L\Delta R\right)}{L\left(L + \Delta L\right)} i_o\left(k\right) \right| \end{aligned} \tag{2.32}$$

Using the parameters in Table 2.3, Figure 2.6 shows the error of predicted grid current under the variation of filter inductor ($\Delta L_f / L_f$), capacitor ($\Delta C_f / C_f$), and resistor ($\Delta R_f / R_f$) respectively. It shows that the error is zero when $\Delta L_f / L_f$=0, $\Delta C_f / C_f$=0, and $\Delta R_f / R_f$=0. While, when the variation ratio is the same, the error of predicted grid current with respect to the filter inductor is higher than that of the capacitor. Additionally, with the variation of the resistor, the error stays small, which can be neglected. Moreover, when the actual capacitor or inductor is smaller than the modeled value, the impacts are more severe, i.e., overestimate of the inductor or capacitor will lead to larger errors. Hence, when applying the FCS-

MPC, the modeled values of the filter inductor or capacitor should be equal or slightly smaller than the actual system values.

Figure 2.7 shows the error of predicted DC current under the variation of inductor L and DC load. The overestimate of the filter inductor can also result in a greater error of predicted DC current than the underestimate condition. Moreover, when the actual system values are smaller than the modeled value, the effect of the filter inductor is more severe than the load resistor. On the contrary, the effect of the load resistor is more severe than the filter inductor when they are underestimated. Besides, compared with the grid current errors are shown in Figure 2.6, the error of DC current is smaller under parameter variation.

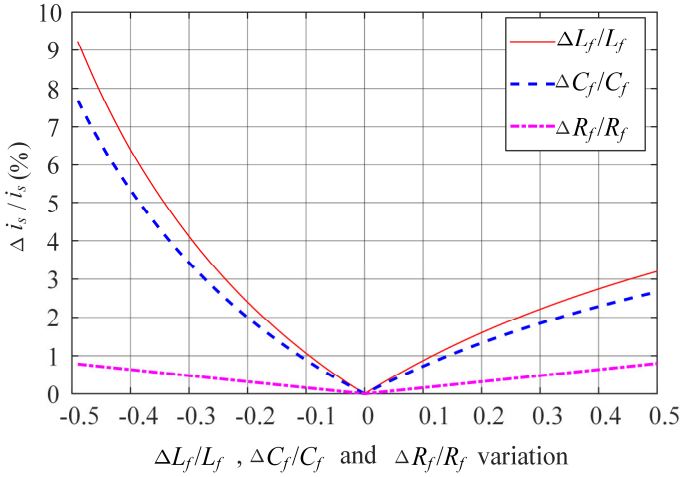


Figure 2.6 The error of grid current (in percentage) with CL filter parameter variation

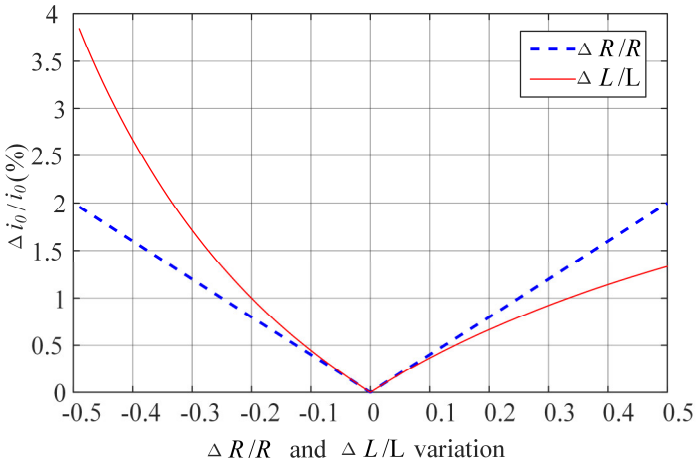


Figure 2.7 The error of DC current (in percentage) with L filter and DC load variation

According to the analysis, the following conclusions can be made:

(1) The proposed FCS-MPC can ensure good control accuracy if the components are within general tolerance, e.g. +/- 10%. Even within +/-20%, both the grid current and DC current can still have errors as small as 2%.

(2) The system is robust to the parasitic resistors.

(3) The AC inductance is more important than other parameters.

(4) If the system parameters cannot be accurately obtained, underestimate them is better than overestimate in terms of control accuracy.

2.3 Simulation and Experimental Verification

2.3.1 Simulation Verification

To validate the proposed control strategy and its advantages, both the proposed FCS-MPC (with 12 virtual space vectors) and the conventional FCS-MPC are implemented and simulated in Matlab/Simulink. The parameters are shown in Table 2.3. The four-step current-based commutation is implemented to ensure safe commutation, so the commutation time is 6*us* (the switching time for each IGBT is 2*us*).

Table 2.3 Model Parameters

Parameter	Values	p.u values
AC source	60V (u_{ll})	1
Rated power	400W	1
CL filter inductor (L_f, R_f)	0.5*mH*,0.2Ω	0.021,0.0222
CL filter Capacitor (C_f)	40*uF*	7.3667
L filter(L)	5*mH*	0.21
DC load (R)	5Ω	0.5556
Sampling time T_S	40*us*	-
One step interval time t_d	2*us*	-
Weighting factors for grid current	1	-
Weighting factor for DC current	1	-

This part compares the performance of conventional FCS-MPC with the proposed FCS-MPC for the non-isolated AC-DC matrix converter. In both control strategies, the system parameters and the cost functions are the same. Figure 2.8 shows the simulation results of conventional FCS-MPC and proposed FCS-MPC,

which includes the grid voltage, grid current, and DC current waveforms. The DC current reference is set to 6.5A, and the reactive power is 0Var.

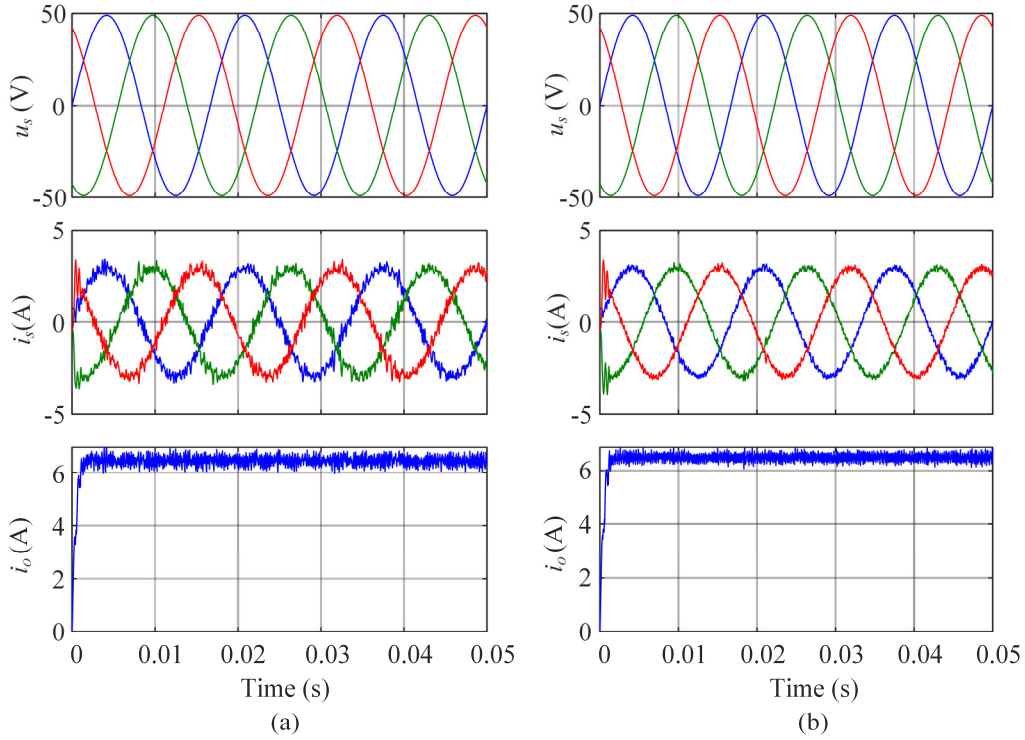


Figure 2.8 Waveforms of grid voltage, grid current, and DC current (a) conventional FCS-MPC (b) proposed FCS-MPC with virtual space vectors

Both control strategies can eliminate steady state errors in DC current and grid current. Unity power factor is achieved as the grid current is in phase with the grid phase voltage. However, it still can be observed that the performance of the proposed control strategy is better than the conventional one. The ripples in grid current and DC current are smaller in the proposed method. The total harmonic distortion (THD) of the grid current is 4.8% when the proposed FCS-MPC is applied, while the THD is 9.71% under the conventional FCS-MPC control strategy. The phase current fast Fourier transform (FFT) is presented in Figure 2.9. The spectrum is widely spread as the actual switching frequency is not constant in FCS-MPC -- the switching states change only when necessary. This is different from PWM based control. However, it still can be found that the harmonic of each order is smaller in the proposed FCS-MPC. Therefore, with the same model parameters and sampling time, the performance of the proposed FCS-MPC with

virtual space vectors is better than conventional FCS-MPC.

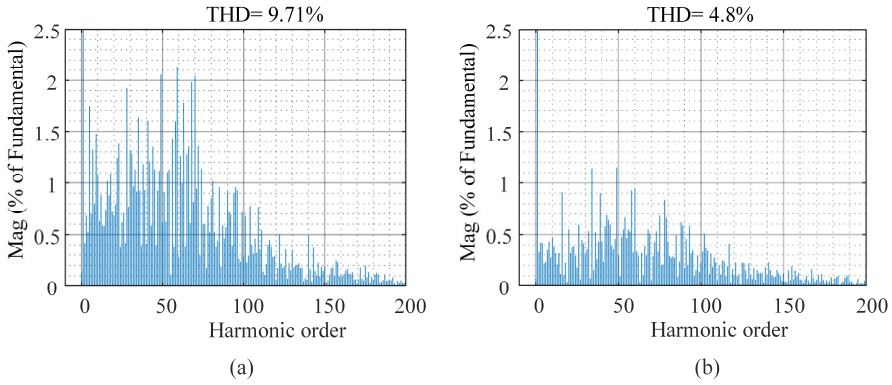


Figure 2.9 FFT analysis of grid current (a) conventional FCS-MPC (b) proposed FCS-MPC with virtual space vectors

For better visualization of the performance improvement, Figure 2.10 and Figure 2.11 present the simulation results for both control strategies.

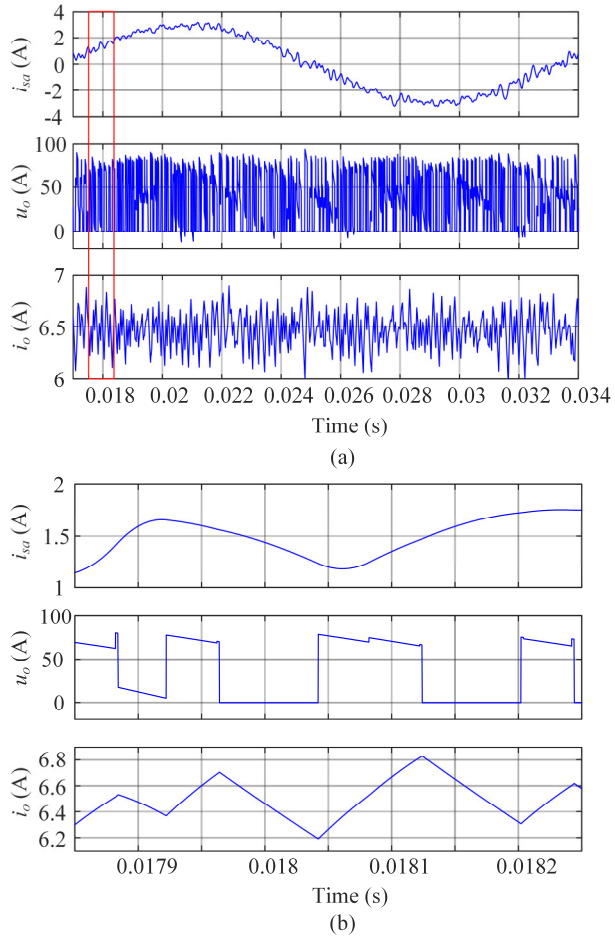


Figure 2.10 (a) i_s, u_o, i_o waveforms in one fundamental period when applying conventional FCS-MPC (b) zoom in the waveforms for ten sampling periods

Figure 2.10(a) shows the grid current i_s, DC voltage of the converter u_o, and DC current i_o waveforms in one fundamental period while Figure 2.10 (b) shows these waveforms in ten sampling periods under conventional FCS-MPC. The same waveforms are presented in Figure 2.11 with the proposed FCS-MPC. Both the control strategies can track the DC current reference and achieve sinusoidal grid current waveforms. However, the DC current ripples and grid current ripples are significantly reduced in the proposed FCS-MPC. To be specific, the DC current ripple is 0.6A in conventional FCS-MPC while the ripple is 0.3A in proposed FCS-MPC.

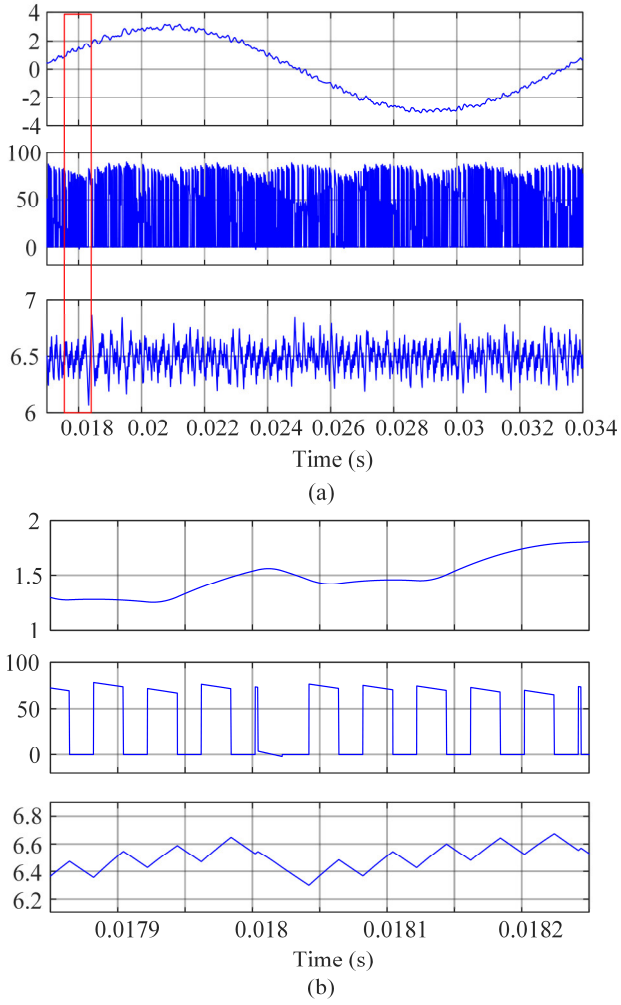


Figure 2.11 (a) i_s, u_o, i_o in one fundamental period when applying proposed FCS-MPC with virtual space vectors (b) zoom in the waveforms for ten sampling periods

From the above analysis, it shows that the CL filter parameter mismatch induces error, reducing the quality of the grid current. When the actual CL filter parameters mismatch with modeled parameters, both the proposed FCS-MPC and the conventional FCS-MPC can still track the reference, but the ripples of the grid current will be different, i.e, THD will be changed. Therefore, to evaluate the effect of parameter mismatch, the THD of grid currents are compared.

Figure 2.12 shows the THD of the grid current with different CL filter parameter mismatches under the conventional FCS-MPC and the proposed FCS-MPC. The modeled values are L_f =0.5mH, R_f =0.2Ω and C_f =40uF. The uncertain part of the parameters is changed from -50% to 50%. The changes of inductance and capacitance will lead to different resonant frequencies of the CL filter, resulting in the change of THD. However, the FCS-MPC can play an important role in the change of THD, as the THD is different under the same condition but with different control methods: when the parameter changes, the THD of the proposed method is always lower than that of conventional FCS-MPC because the proposed FCS-MPC can better mitigate ripples in the current.

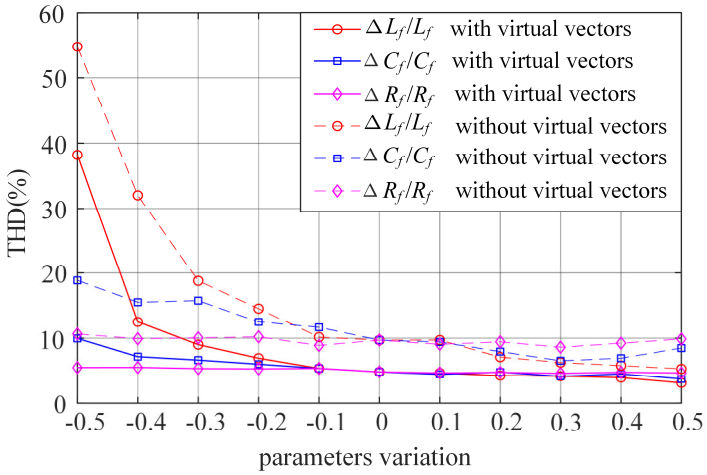


Figure 2.12 Phase current THD performance of conventional FCS-MPC and proposed FCS-MPC with virtual space vectors when filter parameters are mismatched

Besides, the conclusions made in Section 2.2.5 can also be validated with the results in Figure 2.12. With the proposed FCS-MPC method, the THD almost keeps constant when the parameters, including inductors, capacitor, and parasitic resistor,

changes within +/-10%. When the actual values increase by 20% (parameters are underestimated in the controller), the change of THD is still negligible. However, when the actual values decrease by 20% (parameters are overestimated in the controller), the impacts are observable and different parameters show different impacts: the decrease of inductance induces a larger increase of THD than the decrease of capacitance while the impacts of the parasitic resistor are negligible. Besides, the current can still track the reference accurately, and the transient performance (the response time is the same without overshoot) is not changed when the parameters are changes within +/- 20%.

2.3.2 Experimental Verification

The non-isolated AC-DC matrix converter prototype is built for experimental verification, as shown in Figure 2.13. The common emitter connected IGBTs are used as bidirectional switches. The control algorithm was implemented on Texas Instruments DSP TMS320F28379. The commutation strategy is implemented in the Xilinx field programmable gate array (FPGA) XC3S500E, which is connected to DSP by an external memory interface (EMIF) port. The sampling time is 40*us*. The AC power supply is the programmable source AMETEK 4500Lx. The parameters are the same as the simulation model, as shown in Table 2.3.

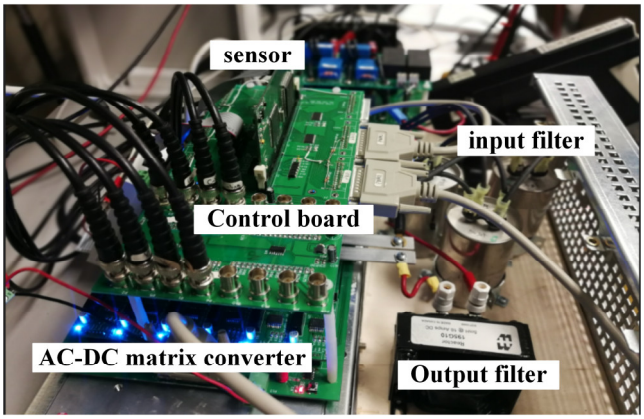


Figure 2.13 Experimental setup of non-isolated AC-DC matrix converter

Figure 2.14 shows the experimental results of both control strategies, Figure 2.14(a)(b)(c) are experimental results of conventional FCS-MPC with DC current reference is 4A, 7A, and 9A respectively. While Figure 2.14(d)(e)(f) are experimental results of proposed FCS-MPC with virtual space vectors under

different DC current reference (4A, 7A, and 9A). The experimental waveforms include phase A grid voltage, phase A grid current, and DC current. Here, with different DC current reference unity power factor is expected.

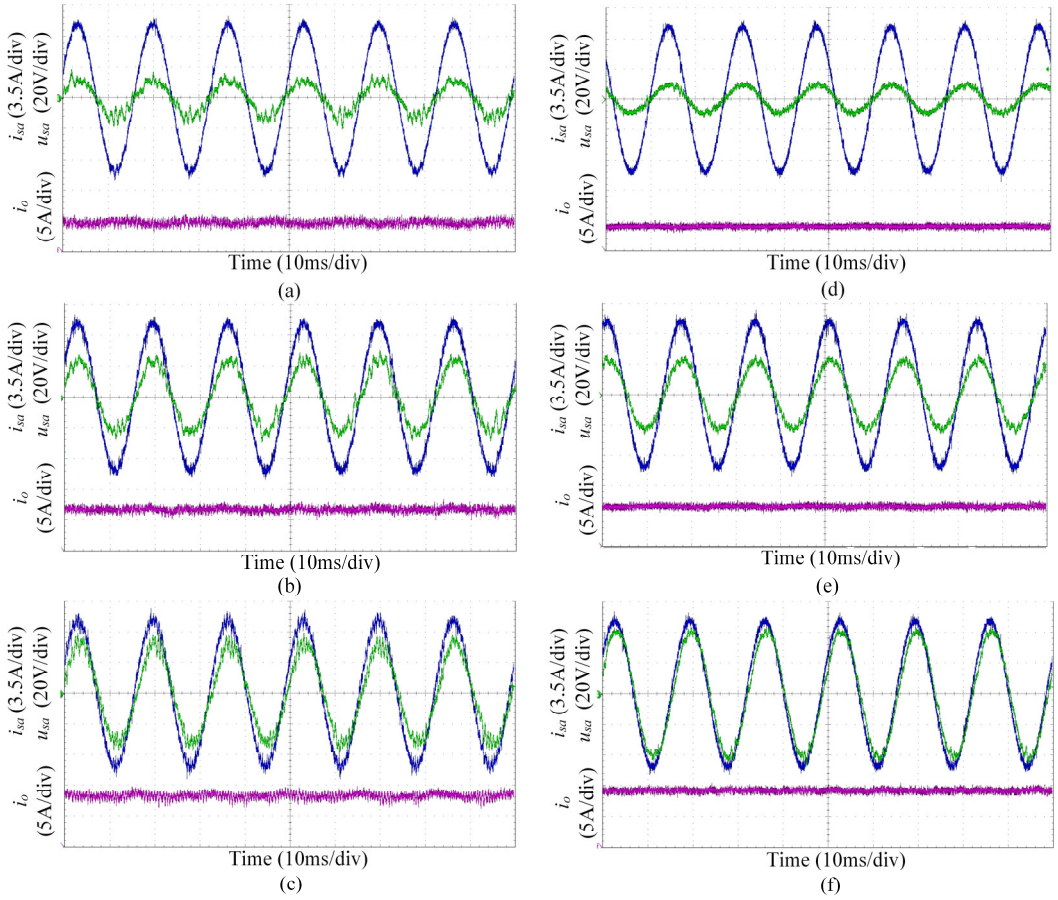


Figure 2.14 Waveforms of phase A grid voltage, phase A grid current and DC current, (a)(b)(c) are experimental results of conventional FCS-MPC with DC current reference are 4A, 7A, and 9A respectively;(d)(e)(f) are experimental results of the proposed FCS-MPC with virtual space vectors with DC current reference are 4A, 7A, and 9A respectively

From Figure 2.14, it can be seen, the grid current ripples and DC current ripples in the proposed method are always lower than the conventional method under the same sampling frequency – 25kHz. To comprehensively compare the proposed FCS-MPC method and the conventional FCS-MPC method, Table 2.4 is given to compare the DC current error, THD of grid current, power factor, and the average switching frequency.

Table 2.4 Switching Frequency and Control Performance under Different Conditions

	Conventional FCS-MPC			Proposed FCS-MPC		
i_o*/ A	4	7	9	4	7	9
Δi_o*/ A	0.4	0.4	0.4	0.2	0.15	0.15
THD / %	18.86%	11.45%	9.5%	11%	5.67%	4.39%
Power factor	0.999	0.992	0.99	0.999	0.994	0.99
f_a / kHz	4.2	4.8	4.65	8.3	8.7	8.2

Figure 2.14 shows that the grid current can be controlled to be in phase with the voltage, the sinusoidal current can be obtained under both control methods. Table 2.4 shows that the average switching frequency ranges from 4.2 to 4.8 *k*Hz in conventional FCS-MPC. The average switching frequency ranges from 8.2 to 8.7 kHz in the proposed FCS-MPC, which is higher than the conventional FCS-MPC. However, the proposed control strategy has a lower ripple in both grid and DC current than the conventional FCS-MPC. The DC current error of the proposed control strategy is around 0.15A, while the DC current error is 0.4A in conventional FCS-MPC. Moreover, thanks to the usage of virtual space vectors, the THD is reduced from 18.86%, 11.45%, and 9.5% to 11%, 5.67%, and 4.39% with the proposed FCS-MPC (DC current is 4A or 7A is not rated power, thus the THD higher than 5% is acceptable). Also, in both conventional FCS-MPC and proposed control strategy, the power factor is greater than 0.99. Therefore, compared with the conventional method under the same sampling frequency, the proposed method increases the equivalent switching frequency, but it can obtain better control performance.

Figure 2.15 shows the transient response of the proposed FCS-MPC with the DC current reference changes from 3A to 5A. The grid current can track the reference in 0.5*ms* without overshoot and the DC current can reach the desired value in 1.5*ms*. The DC current and grid current can track the reference accurately and the transient is fast without overshoot.

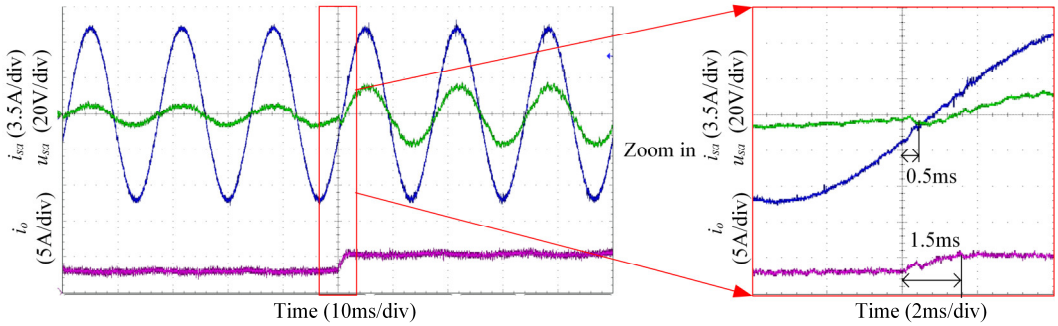


Figure 2.15 Waveforms of phase A voltage, phase A current, and DC current when applying proposed FCS-MPC with virtual space vectors, the DC current reference changes from 3A to 5A

2.4 Summary

This chapter proposes an FCS-MPC scheme with virtual space vectors for non-isolated AC-DC matrix converter to simultaneously achieve high-quality AC and DC currents and ensures successful commutation without a complex PWM scheme. Due to the usage of virtual space vectors, the performance of the proposed FCS-MPC is improved compared with the conventional FCS-MPC, which can effectively reduce the THD of the grid current and the DC current errors. Also, the proposed control strategy has a fast dynamic response without overshoot. Moreover, through the analysis of the impacts of parameter mismatch in FCS-MPC, the design guidelines to achieve robustness against parameter uncertainty are given. To validate the advantages of the proposed method, a thorough comparison between FCS-MPC without virtual space vectors and with virtual space vectors is performed in both simulation and experimental results.

Chapter 3

9-segment SVM for Isolated AC-DC Matrix Converter

Compared to the non-isolated AC-DC matrix converter, the isolated AC-DC matrix converter has extra four active switches in H-bridge. Therefore, the isolated AC-DC matrix converter has 36 vector combinations, more vector combinations would be formed if virtual space vectors are required. Also, unlike multiple objectives control in a non-isolated AC-DC matrix converter, only the AC current is required to be controlled in an isolated AC-DC matrix converter. Hence, the implementation of FCS-MPC is suitable for non-isolated AC-DC matrix converter, but it is too complex for the isolated AC-DC matrix converter. Instead, the modulation or control methods shall be studied to achieve high performance.

In an isolated AC-DC matrix converter, the commutation requires three times the switching time of the semiconductor to ensure safe commutation. When the switching time is long, the current will be distorted as numerous narrow pulses are generated. Besides, the commutation sequence is determined by the relative voltage magnitude, so it's difficult to determine the switching sequence when two phases have close voltage magnitude. To solve these challenges, this chapter proposes a 9-segment SVM strategy to avoid the commutation between two phases with close voltage magnitude. Moreover, the two-step commutation strategy can be applied in each switching cycle, and the zero vectors are optimized to reduce narrow pulse. Therefore, the high current quality can be achieved even the switching time of the semiconductor is relatively long.

Publications out of this Chapter:

F. Fang, H. Tian and Y. Li, "A New Space Vector Modulation Strategy to Enhance AC Current Quality of Isolated DC-AC Matrix Converter," in *IEEE Transactions on Industry Application*, in press.

Besides, the 3-1 MC and H-bridge should have a phase shift angle to transfer power. The AC current is synthesized by the primary current of HFT instead of constant DC current, leading to a different modulation design from the non-isolated AC-DC matrix converter. Therefore, the modulation strategy should be designed properly to achieve a sinusoidal current specifically for isolated AC-DC matrix converter.

3.1 Commutation Issue in Isolated AC-DC Matrix Converter

As illustrated, commutation is vital for the safe operation of matrix converter. This also applies to isolated AC-DC matrix converter. Due to the current is a high frequency waveform, the voltage-based, instead of current-based, commutation strategy is suitable for the isolated AC-DC matrix converter. As a result, the commutation sequence is selected based on the relationship between capacitor voltages, commutation can only be reliable when the relative voltage magnitude of two phases is clear. However, when the voltage magnitudes of the two phases are close (as shown in Figure 3.1), the relative magnitude is difficult to discriminate in practice due to the sensor errors and sampling noises. Therefore, the wrong commutation sequence may be selected and result in the current distortion or even device damage.

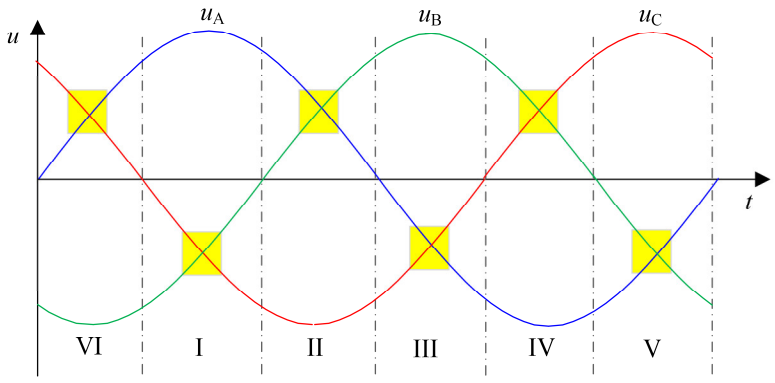


Figure 3.1 Critical area

Considering the harmonics in capacitor voltages, the critical area should be wide enough. However, the wider the critical area, the more distortions will be generated in the AC current due to nonequal commutation time in the critical area

and uncritical area. To solve the commutation problem in a critical area, many solutions have been researched. The first option is not executing the commutation sequence in a critical area [92]. Due to the small difference between the two phases, the effect on the output voltage is small, but distortions are generated in the input current. Alternatively, the current direction can be used to determine the commutation sequence in the critical area [93]. This is hard to implement due to the difficulty of sampling high frequency current in a power electronic converter, where the electromagnetic environment is complicated. The third solution is to avoid a short circuit between two phases when their voltage magnitudes are close. The current can switch to the third phase firstly, and then switch to the desired phase. But the transition doubles the commutation time. This may be a significant problem when the commutation time is long. Otherwise, the current distortion will be generated because of nonequal commutation in the critical area and uncritical area.

Considering the above challenge, a new SVM strategy is proposed for isolated AC-DC matrix converter with high current quality, reliable commutation scheme, relatively low number of switching actions. Firstly, through calculating the duty cycles of each vector, a high quality AC side current can be achieved in the proposed method. Secondly, the commutation will always happen between phases with detectable differences in instantaneous voltage amplitude. Thirdly, two approaches are applied to reduce the impact of the narrow pulses. On one hand, a two-step commutation is used to shorten the required commutation time. On the other hand, the SVM optimizes the usage of the zero vectors to further reduce the narrow pulses. As a result, the isolated AC-DC matrix converter can always perform safe commutation and the current distortions related to commutation are also minimized.

3.2 Basic Operation Principles

The detailed topology of the isolated AC-DC matrix converter is shown in Figure 3.2. The converter is connected to the grid through a CL filter which is applied to mitigate the current ripple and ensures a sinusoidal AC current. The 3-1 MC is used to convert the line frequency AC voltage to high frequency AC voltage.

The HFT can provide galvanic isolation and its turn ratio can be designed to step up/down the voltage according to the DC side requirement. Due to different voltages on the leakage inductor (L_k), the power can be transferred between the primary side and secondary side. On the secondary side, the H-bridge can perform a bidirectional conversion between the DC bus voltage and the high frequency AC voltage of the HFT.

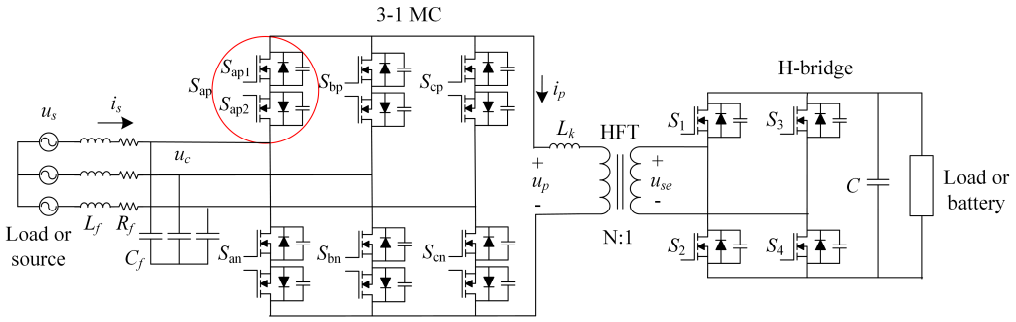


Figure 3.2 Topology of isolated AC-DC matrix converter

To properly operate the 3-1 MC, a simultaneous connection of two AC phases to the same high frequency phase must be avoided as this can lead to a short circuit of the load side. Meanwhile, due to the existence of the leakage inductor, the open circuit shall be avoided at the HFT side to provide freewheeling paths for the leakage inductor current. Therefore, at any time, only one bidirectional switch shall be turned on in the three-upper arms, and only one bidirectional switch must be turned on in the three-lower arms.

Therefore, there are six active vectors and three zero vectors in 3-1 MC. To obtain high frequency alternating voltage at the secondary side of the HFT, the switching vectors should produce both positive and negative voltages at the transformer side. Therefore, there are two switching states for each vector that generate the same voltage amplitude in the opposite direction, as shown in Figure 3.3. I_1 contains I_{1+} and I_{1-}, where I_{1+} generates u_{ab} voltage while I_{1-} generates u_{ba} voltage. The corresponding switching states and the output voltage of each vector are listed in Table 3.1.

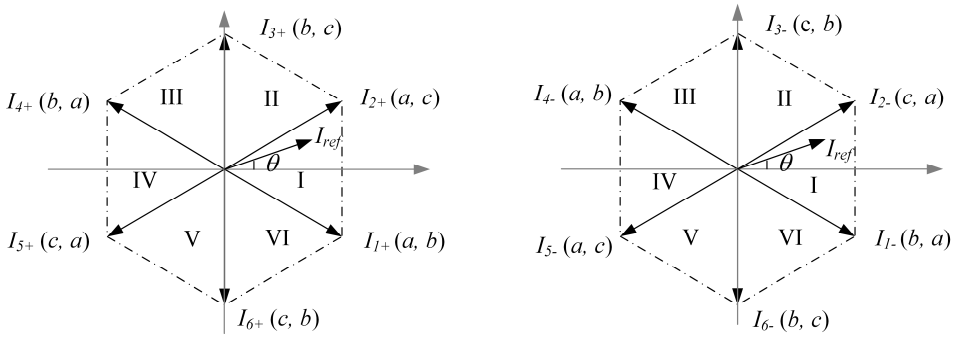


Figure 3.3 Space vector hexagon for 3-1 MC

Table 3.1 Space Vectors in 3-1 MC

Space vectors	Switching states						output voltage
	S_{ap}	S_{an}	S_{bp}	S_{bn}	S_{cp}	S_{cn}	
I_{1+}/I_{4-}	1	0	0	1	0	0	u_{ab}
I_{2+}/I_{5-}	1	0	0	0	0	1	u_{ac}
I_{3+}/I_{6-}	0	0	1	0	0	1	u_{bc}
I_{4+}/I_{1-}	0	1	1	0	0	0	u_{ba}
I_{5+}/I_{2-}	0	1	0	0	1	0	u_{ca}
I_{6+}/I_{3-}	0	0	0	1	1	0	u_{cb}
I_7	1	1	0	0	0	0	0
I_8	0	0	0	0	1	1	0
I_9	0	0	1	1	0	0	0

3.3 9-segment SVM Strategy

To explain the proposed SVM strategy, the current reference is assumed to be in sector I (when the desired input current is in other sectors, the corresponding analysis is similar). The reference can be synthesized by two adjacent active vectors (I_1 and I_2) and a zero vector I_0. In the proposed 9-segment SVM strategy, the switching sequence and corresponding duty ratio are illustrated in detail as follows.

3.3.1 Switching Sequence

To avoid the commutation between two phases with unclear relative magnitude, the switching signals and voltage waveforms of the proposed SVM strategy are presented in Figure 3.4. For 3-1 MC, the switching sequence is I_0, I_{1+}, I_0, I_{1-}, I_0, I_{2+}, I_0, I_{2-}, I_0. Corresponding to each vector, the duty ratios are $d_{01}/4$, $d_1/2$,

$d_{01}/2$, $d_1/2$, $(d_{01}+d_{02})/4$, $d_2/2$, $d_{02}/2$, $d_2/2$, $d_{02}/4$. The transition happens between active vector and zero vector, and the sequence in the upper arm is S_{ap}-S_{bp}-S_{ap}-S_{cp}-S_{ap}, the sequence in the lower arm is S_{an}-S_{bn}-S_{an}-S_{cn}-S_{an}. All the commutation occurs between phase A and phase B, or between phase A and phases C. In sector I, the relative magnitude of phase B and phase C is unclear. However, in the proposed SVM strategy, the commutation between phase B and phase C is not required. Therefore, the two-step commutation is always applicable.

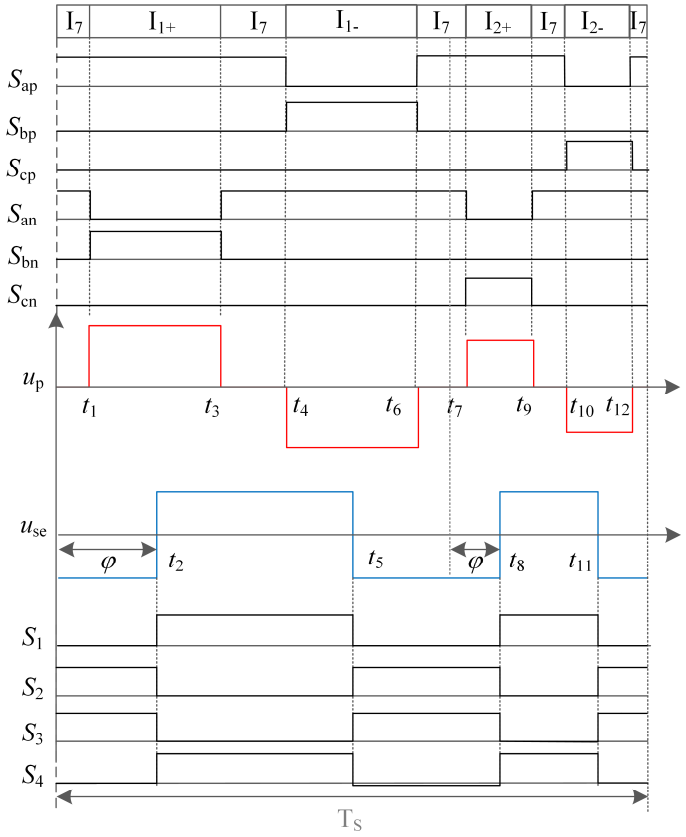


Figure 3.4 Waveforms of primary voltage, secondary voltage, and corresponding switching states of the 9-segment SVM strategy

With high frequency voltage applied to the 3-1 MC, the H-bridge should cooperate with the 3-1 MC to transfer power. All switches (S_1-S_4) are driven by square wave gate signals with a 50% duty ratio. The switches in one bridge have complementary gate signals. While a phase shift angle φ should be applied between the primary voltage and secondary voltage to transfer power. Therefore, the

alternative voltage produced by 3-1 MC must have a phase difference of φ compared with the AC voltage of the H-bridge converter.

3.3.2 Duty Cycle Calculation

After selecting the vectors and determining the switching sequence in one switching cycle, the two-step commutation scheme can be used. Moreover, it is worth noting that the corresponding duty ratio is critical to implement this SVM strategy to achieve sinusoidal current. The phase current is constructed by the primary current, and the primary current is determined by the primary voltage and secondary voltage. To track the current reference, the average current of each phase should be calculated. Taking sector I as an example, the switching sequence, primary voltage, secondary voltage, primary current, and AC phase current waveforms are presented in Figure 3.5.

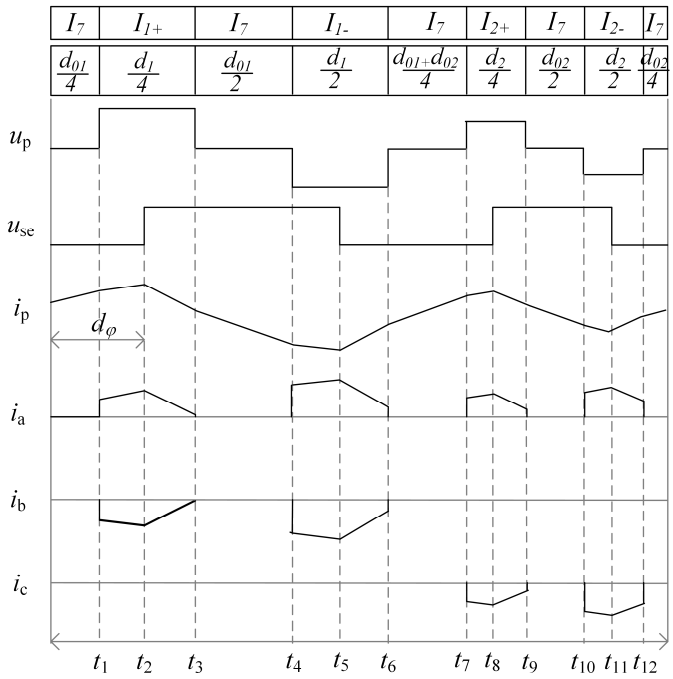


Figure 3.5 Phase current waveforms in one switching cycle

Figure 3.5 shows that the phase current waveforms are constructed by the primary current. The distribution of the zero vector has the following relationship, $d_{01}/d_{02}=d_1/d_2$. With the distribution time relationship, the average current can be calculated easily due to it can be seen as partition extended phase shift angle

strategy in dual active bridge [94-95]. In one switching cycle, the average value of each phase can be calculated as (3.1-3.3).

$$i_a = \frac{1}{T_S}\left(\int_{t_1}^{t_3} i_p dt + \int_{t_4}^{t_6} -i_p dt + \int_{t_7}^{t_9} i_p dt + \int_{t_{10}}^{t_{12}} -i_p dt\right) \tag{3.1}$$

$$i_b = \frac{1}{T_S}\left(\int_{t_1}^{t_3} -i_p dt + \int_{t_4}^{t_6} i_p dt\right) \tag{3.2}$$

$$i_c = \frac{1}{T_S}\left(\int_{t_7}^{t_9} -i_p dt + \int_{t_{10}}^{t_{12}} i_p dt\right) \tag{3.3}$$

With the calculated three phases current, the synthesized current can be achieved as

$$\begin{aligned} i &= \frac{2}{3}\left(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}}\right) \\ &= \frac{-\left(d_1^2 + d_2^2\right)}{8\left(d_1 + d_2\right)^2}\left\{\left(d_1 + d_2\right)^2 - 2\left(d_1 + d_2\right) + \left(4d_\varphi - 1\right)^2\right\}\frac{Nu_{dc}}{f_s L_k} \\ &+ j\frac{1}{\sqrt{3}}\frac{\left(d_1^2 - d_2^2\right)}{8\left(d_1 + d_2\right)^2}\left\{\left(d_1 + d_2\right)^2 - 2\left(d_1 + d_2\right) + \left(4d_\varphi - 1\right)^2\right\}\frac{Nu_{dc}}{f_s L_k} \end{aligned} \tag{3.4}$$

When the phase shift angle is 90°, the AC current can be achieved as

$$i = \frac{-\left(d_1^2 + d_2^2\right)}{8}\left\{1 - \frac{2}{d_1 + d_2}\right\}\frac{Nu_{dc}}{f_s L_k} + j\frac{1}{\sqrt{3}}\frac{\left(d_1^2 - d_2^2\right)}{8}\left\{1 - \frac{2}{d_1 + d_2}\right\}\frac{Nu_{dc}}{f_s L_k} \tag{3.5}$$

To track the current reference, the synthesized current should be equal to the reference, as (3.6).

$$\begin{aligned} I_{ref}\cos\theta &= \left(d_1^2 + d_2^2\right)\left(\frac{2}{d_1 + d_2} - 1\right)\frac{Nu_{dc}}{8f_s L_k} \\ I_{ref}\sin\theta &= \frac{1}{\sqrt{3}}\left(-d_1^2 + d_2^2\right)\left(\frac{2}{d_1 + d_2} - 1\right)\frac{Nu_{dc}}{8f_s L_k} \end{aligned} \tag{3.6}$$

where N is turns ratio of HFT, u_{dc} is DC voltage, f_s is switching frequency and L_k is leakage inductor.

By solving (3.6), the duty ratio of active vectors can be calculated as

$$
\begin{aligned}
d_1 &= \frac{\sqrt{\sin\left(\frac{\pi}{6}-\theta\right)}}{\sqrt{\sin\left(\frac{\pi}{6}-\theta\right)}+\sqrt{\sin\left(\frac{\pi}{6}+\theta\right)}}\left\{1-k\right\};\\
d_2 &= \frac{\sqrt{\sin\left(\frac{\pi}{6}+\theta\right)}}{\sqrt{\sin\left(\frac{\pi}{6}-\theta\right)}+\sqrt{\sin\left(\frac{\pi}{6}+\theta\right)}}\left\{1-k\right\};\\
d_{01} &= \frac{d_1}{d_1+d_2}\left(1-d_1-d_2\right);\\
d_{02} &= \frac{d_2}{d_1+d_2}\left(1-d_1-d_2\right);
\end{aligned}
\tag{3.7}
$$

where

$$
k = \sqrt{1-0.5m\left(\cos\theta+\sqrt{1-4\sin^2\theta}\right)}; \tag{3.8}
$$

$$
m = \frac{I_{ref}}{Nu_{dc}/\left(16f_sL_k\right)} \tag{3.9}
$$

where m is the modulation index, θ is the angle of current reference $\theta\in[-\pi/6,\pi/6)$. It can be observed that the modulation index and current reference has a linear relationship. Therefore, the conventional PI controller can be applied directly to this converter.

3.3.3 Narrow Pulses Reduction

To ensure the safe commutation of bidirectional switches, the pulse width is required to be larger than the commutation time. In the proposed SVM strategy (Figure 3.4), the requirements are shown in (3.10).

$$
\begin{aligned}
&0.5d_1 > d_c;\\
&0.5d_2 > d_c;\\
&0.25d_{01} > d_c;\\
&0.25d_{02} > d_c;
\end{aligned}
\tag{3.10}
$$

where d_c is commutation ratio, which equals to commutation time divides switching period.

To ensure safe commutation, the duty ratios of active vectors are required to be larger than two times the commutation ratio. At each sector boundary, either d_1 or d_2 is nearly zero, the duty ratio of the active vector must be extended to $2d_c$ mandatory to finish the commutation process. Eventually, the synthesized current is not equal to the current reference, increasing current distortions. To avoid changing the duty ratios of active vectors, the zero vector is optimized in this chapter. Figure 3.6 shows three different zero vectors (I_7, I_8, I_9) that are applied in each switching cycle to extend the pulse width of switches in active vectors. For example, I_9 is applied between I_{1+} and I_{1-} instead of I_7, therefore, the pulse width of S_{bn} changes from $0.5d_1$ to $(0.5d_1+0.5d_{01})$.

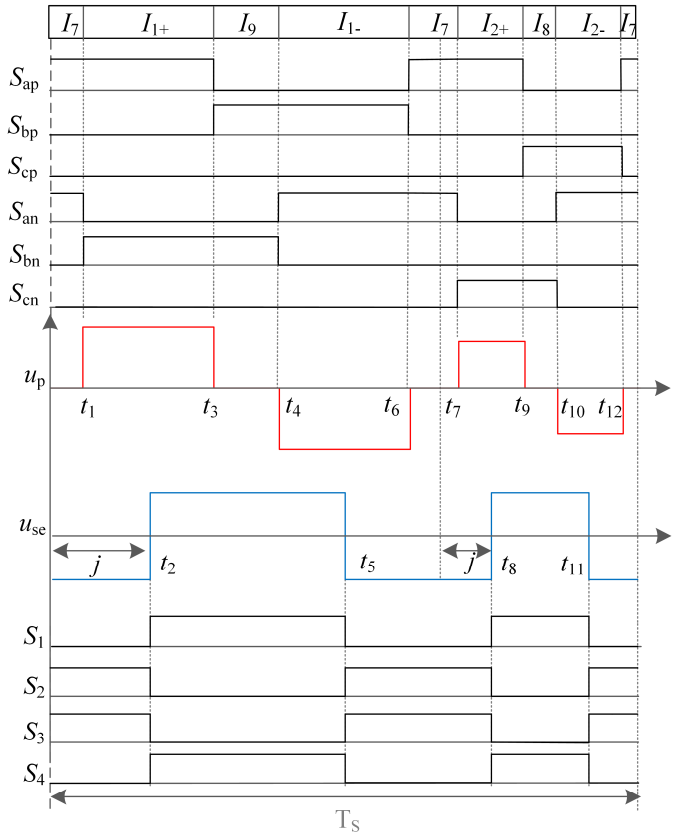


Figure 3.6 Waveforms of primary voltage, secondary voltage, and corresponding switching states of the proposed 9-segment SVM strategy with zero vector optimization

Finally, the constraints are given in (3.11). It can be observed that only the duty ratios of zero vectors are required to be larger than $4d_c$, the duty ratios of active vectors are not changed anymore. Therefore, the synthesized current can track the

current reference accurately.

$$0.25d_{01} > d_c;$$
$$0.25d_{02} > d_c; \tag{3.11}$$

According to the requirements in (3.10), the shaded area of narrow pulses with different modulation index and current angle is shown in Figure 3.7(a) and (b) when assuming d_c is 0.01 and 0.02, respectively. It can be observed that (1) with the increase of d_c, more narrow pulses are generated; (2) the area of narrow pulses increases with the decrease of modulation index. Therefore, at a low modulation index, the number of narrow pulses is higher and causes more current distortions. However, after optimizing zero vector, the narrow pulses are reduced significantly respectively in Figure 3.7(c) and (d).

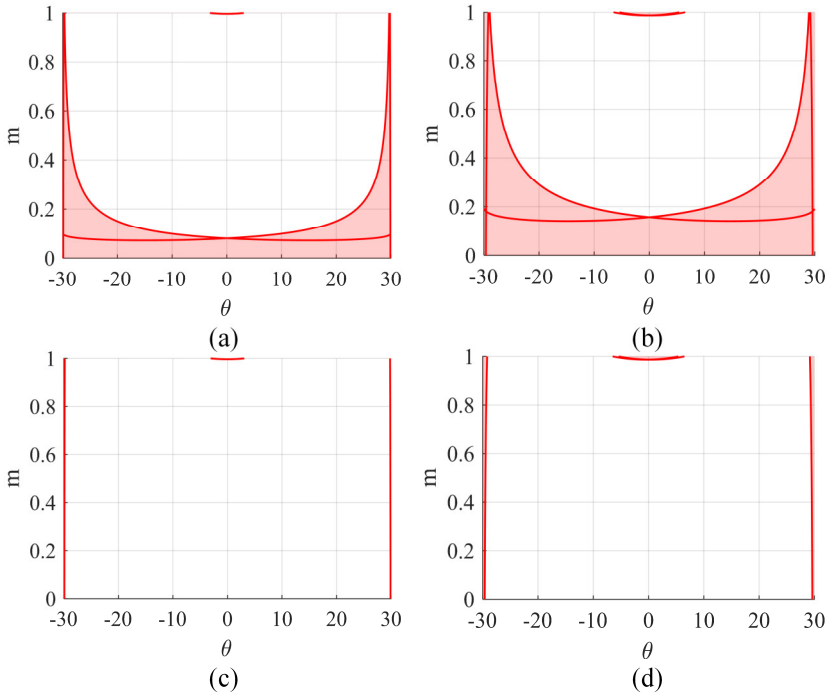


Figure 3.7 Narrow pluses are occurred in shaded area (a) without zero vector optimization when d_c =0.01 (b) without zero vector optimization when d_c =0.02 (c) with zero vector optimization when d_c =0.01 (d) with zero vector optimization when d_c =0.02

3.3.4 Two-step Commutation Process

To achieve a two-step commutation, some unidirectional switches can be turned on to provide freewheeling paths. The steady states of each switching vector

can be determined by the relative magnitude of filter capacitor voltages. Table 3.2 lists the switching states of each vector in sector I whose voltage condition is $u_a > u_c \approx u_b$.

Once the switching states are determined, the commutation sequence from one bidirectional switch to another bidirectional switch can be achieved. Taking the commutation process between S_{an} and S_{bn} as an example, the detailed switching states and the corresponding commutation schematics are given in Figure 3.8 and Figure 3.9. The transistors on a black background are in the ON-state, and those plotted by a gray line are in the OFF-state.

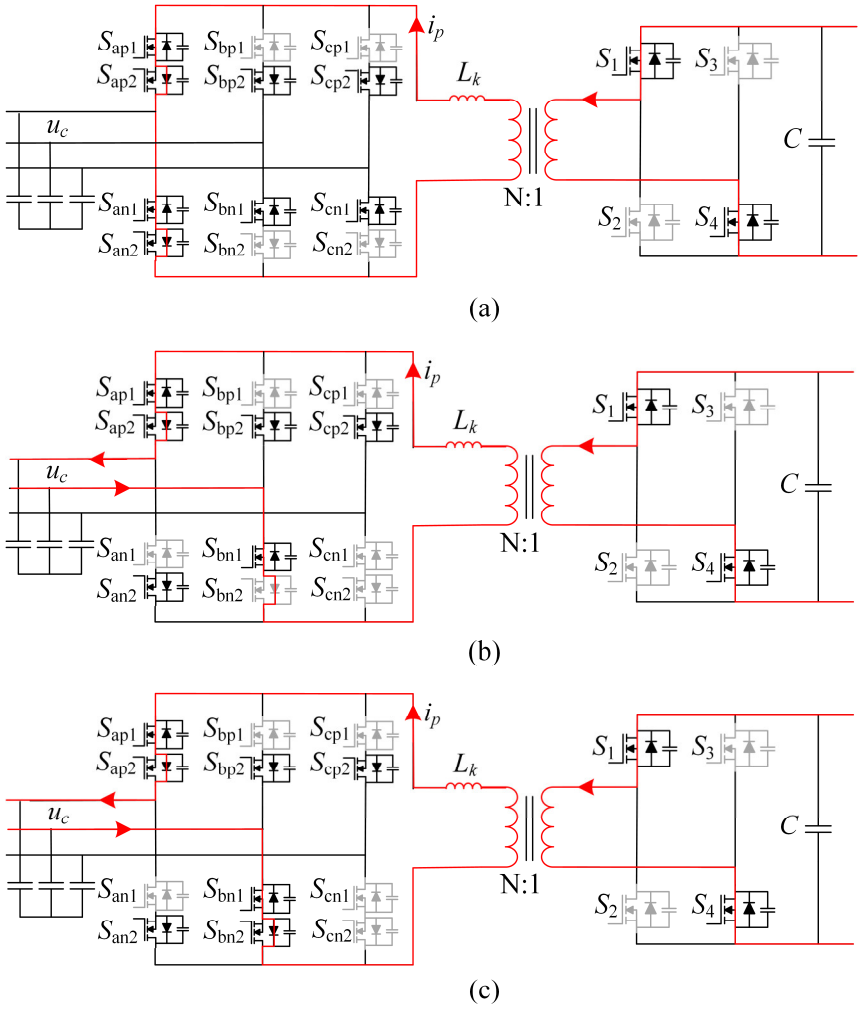


Figure 3.8 The commutation process of S_{an} to S_{bn} (I_7 to I_{1+}) (a) switching states of I_7 (b) first step (c) second step

Figure 3.8 (a) shows the switching states of I_7. At this state, S_{ap1}, S_{ap2}, S_{an1}, and S_{an2} are turned on. To facilitate a smooth transition from one switch to another, the redundant unidirectional switches are turned on to provide a freewheeling path without causing short circuits of filter capacitor voltages, such as S_{bp2}, S_{cp2}, S_{bn1}, and S_{cn1}. The primary current is circulating in phase A; therefore, the secondary voltage is zero. When I_7 transit to I_{1+}, the first step is to turn off S_{an1}. Since the S_{bn1} is turned on and the secondary current is negative, the current flows through S_{bn1} and the diode of S_{bn2}. After an interval time, S_{bn2} is turned on to finish the commutation process. Using the same procedure, the commutation process of S_{bn} to S_{an} is shown in Figure 3.9. Similarly, the switching states of each vector and the commutation sequence in any transition can be achieved.

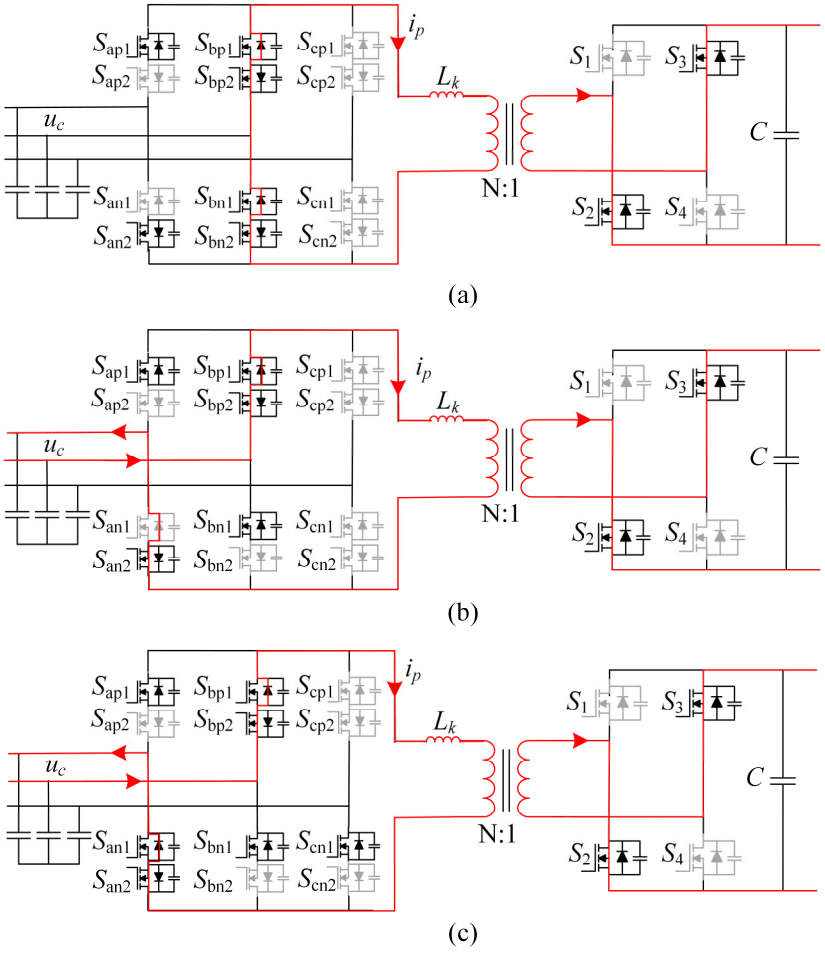


Figure 3.9 The commutation process of S_{bn} to S_{an} (I_9 to I_{1-}) (a) switching states of I_9 (b) first step (c) second step

Table 3.2 Switching States of Each Vector

	I_{1+}	I_{2+}	I_{1-}	I_{2-}	I_7	I_8	I_9
S_{ap1}	1	1	1	1	1	1	1
S_{ap2}	1	1	0	0	1	0	0
S_{an1}	0	0	1	1	1	0	0
S_{an2}	1	1	1	1	1	1	1
S_{bp1}	0	0	1	0	0	0	1
S_{bp2}	1	1	1	0	1	0	1
S_{bn1}	1	0	1	1	1	0	1
S_{bn2}	1	0	0	0	0	0	1
S_{cp1}	0	0	0	1	0	1	0
S_{cp2}	1	1	0	1	1	1	0
S_{cn1}	0	1	1	1	1	1	0
S_{cn2}	0	1	0	0	0	1	0

3.4 Simulation and Experimental Verification

3.4.1 Simulation Verification

The proposed SVM strategy for isolated AC-DC matrix converter is verified by the simulation model in MATLAB/Simulink. To achieve efficiency, the losses of isolated matrix converter with 600V 41A CoolMOS (IXKF 40N60SCD1) are measured by PLECS. The model parameters are given in Table 3.3.

Table 3.3 Model Parameters

Parameters	Values
DC capacitor C	110uF
Switching frequency	10kHz
Turns ratio N	2
Leakage inductor	220uF
Filter inductor L_f , R_f	0.3mH, 0.01Ω
Filter capacitor C_f	30uF

The DC side is connected to a 120V DC source, and the AC side is connected to a 208V, 60Hz AC source. Figure 3.10 shows the simulation waveforms of the proposed SVM strategy when the modulation index is 0.8. It includes phase current, primary voltage, secondary voltage, and primary current waveforms. It shows that the proposed SVM strategy can obtain a sinusoidal phase current with the calculated duty cycle (Figure 3.11 shows the phase current THD). To see the high frequency waveforms and observe the switching sequence, the primary voltage, secondary

voltage, and primary current waveforms in one switching cycle are given in Figure 3.12. The polarity of the primary voltage and secondary voltage changes twice in one switching cycle and the primary voltage lags the secondary voltage 90°.

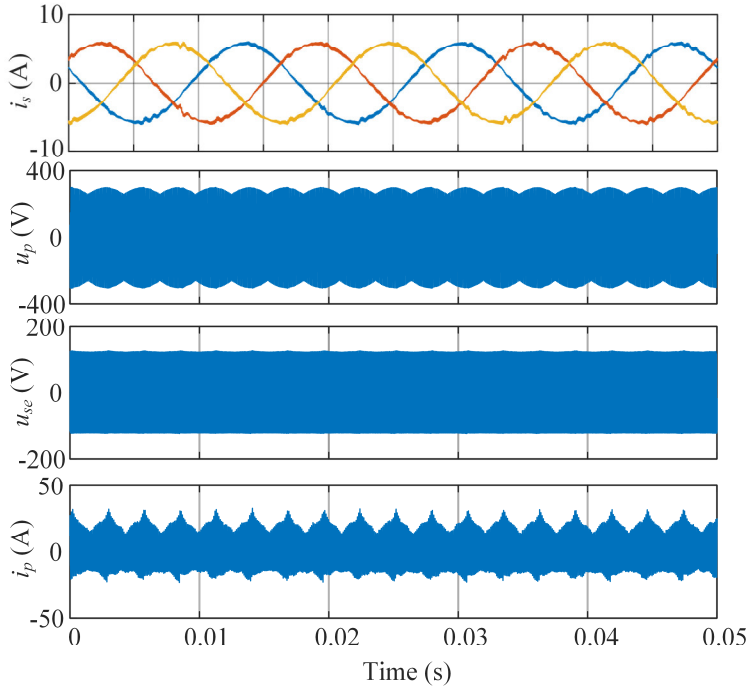


Figure 3.10 The waveforms of phase current, primary voltage, secondary voltage, and primary current

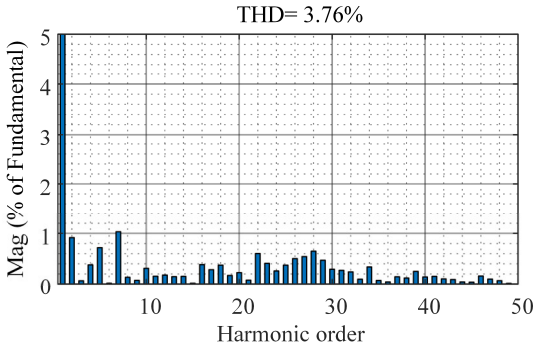


Figure 3.11 The FFT analysis of phase current

Under different active power, the power losses of the converter are measured in PLECS and the corresponding efficiency can be calculated. Figure 3.13 shows the efficiency of the converter for different active power. Under a light load condition, the power efficiency is 82%. However, as the active power increases, the efficiency increases and reaches its maximum value of 94%.

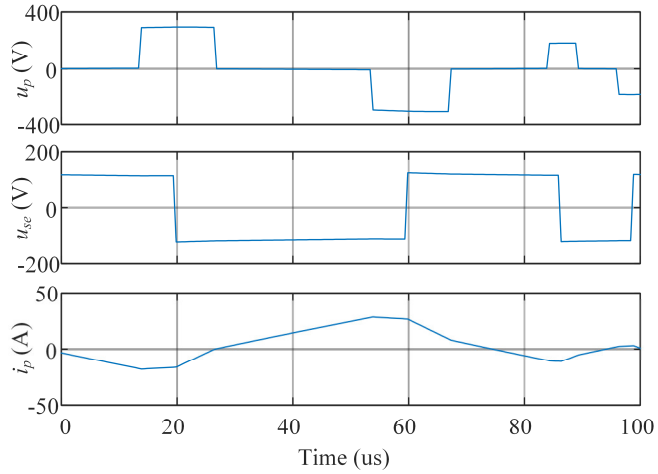


Figure 3.12 The waveforms of primary voltage, secondary voltage, and primary current

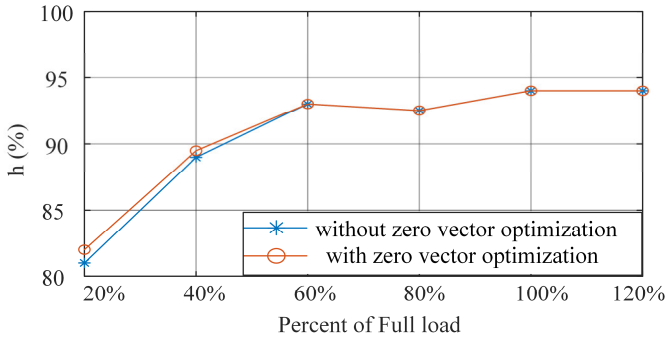


Figure 3.13 Efficiency of the proposed SVM strategy under different load conditions

Figure 3.14 shows the simulation results of the proposed SVM strategy without and with zero vector optimization under m=0.3. It turns that the current quality is improved after the zero vector is optimized, the THD is reduced from 5.89% to 3.48%, as shown in Figure 3.15. The 5^{th}, 7^{th}, 11^{th}, 13^{th} order harmonics are reduced significantly.

To verify the narrow pulse is reduced after zero vector optimization, the THD of the proposed method without zero vector optimization are compared in Figure 3.16. It shows that the THD is high without zero vector optimization at a low modulation index. Besides, as the modulation index increase, the THD is reduced. These conclusions are coordinate with the analysis. After zero vector optimization, the narrow pulses are reduced significantly. Therefore, the THD is improved especially at a low modulation index.

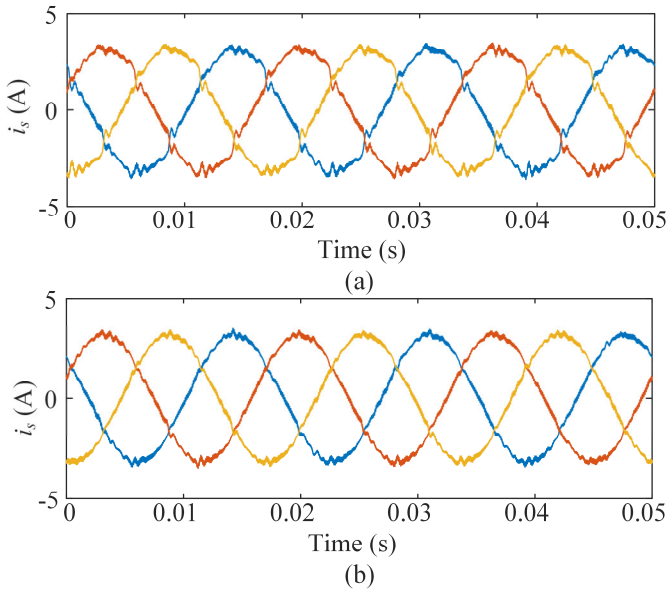


Figure 3.14 Phase current (a) without zero vector optimization (b) with zero vector optimization

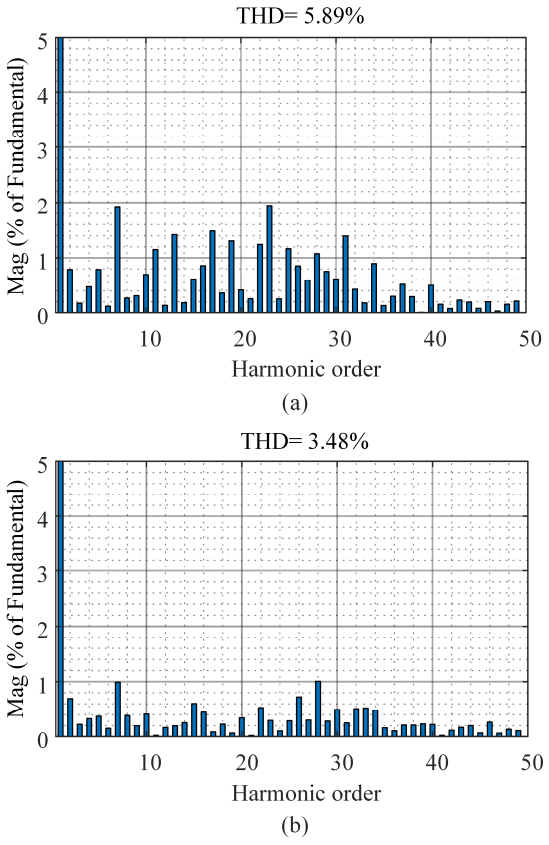


Figure 3.15 Corresponding FFT analysis of phase current (a) without zero vector optimization (b) with zero vector optimization

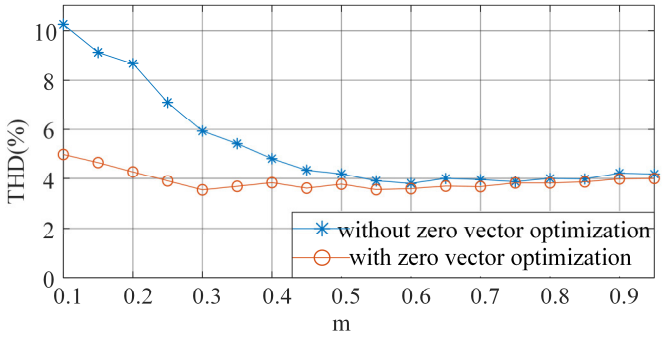


Figure 3.16 THD comparison of phase current without and with zero vector optimization under different modulation index

3.4.2 Experimental Verification

To verify the proposed SVM strategy for an isolated AC-DC matrix converter, a lab prototype is built. The super-junction metal oxide semiconductor field effect transistor (MOSFET) is used to build bidirectional switches. Texas Instruments DSP TMS320F28379 and the Xilinx FPGA XC3S500E are used to implement the SVM strategy. The prototype is presented in Figure 3.17 and the model parameters are the same as the simulation, as listed in Table 3.3. The DC side is connected to a 48V voltage, and the AC side is a three-phase load (20Ω).

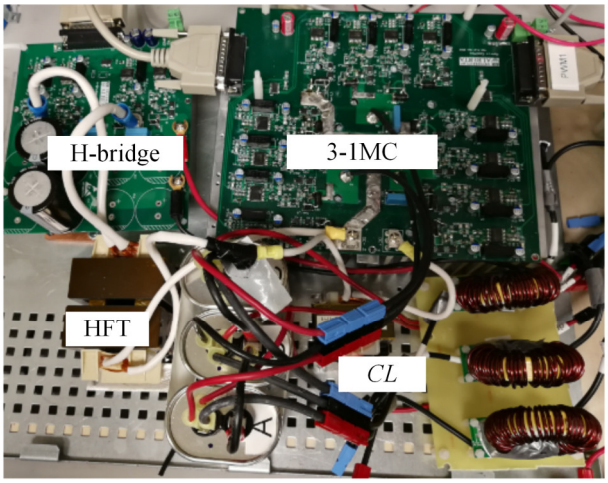


Figure 3.17 Experimental prototype of isolated AC-DC matrix converter

Figure 3.18 shows the experimental results of the proposed SVM strategy under m=0.8. It consists of the line-to-line voltage, phase current, primary voltage, secondary voltage, and primary current (from upper to lower). It can be observed that both the voltage and the current are sinusoidal, while the primary voltage,

secondary voltage, and primary current are high frequency waveforms. To see them clearly, Figure 3.19 shows the zoomed-in waveforms in two switching cycles. The secondary voltage contains 5 levels, and these levels are the positive and negative envelopes of the line-to-line voltages and zero voltage level. While the primary voltage is a square wave, the positive and negative DC bus voltage.

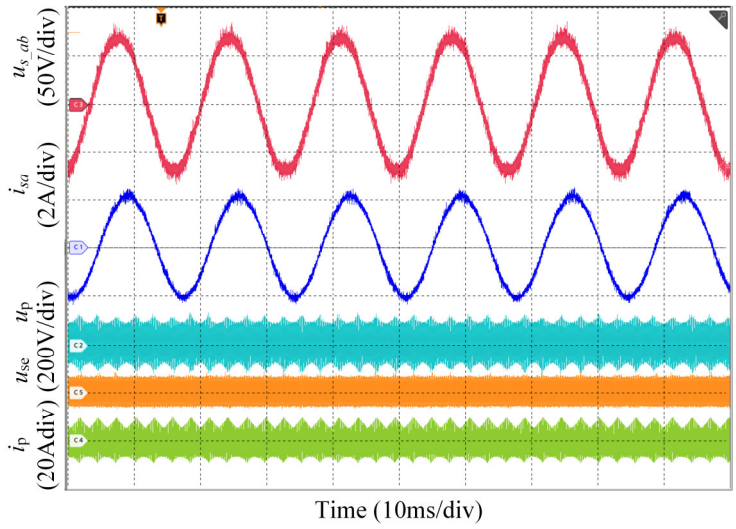


Figure 3.18 Waveforms of line-to-line voltage, phase current, primary voltage, secondary voltage, and primary current of HFT

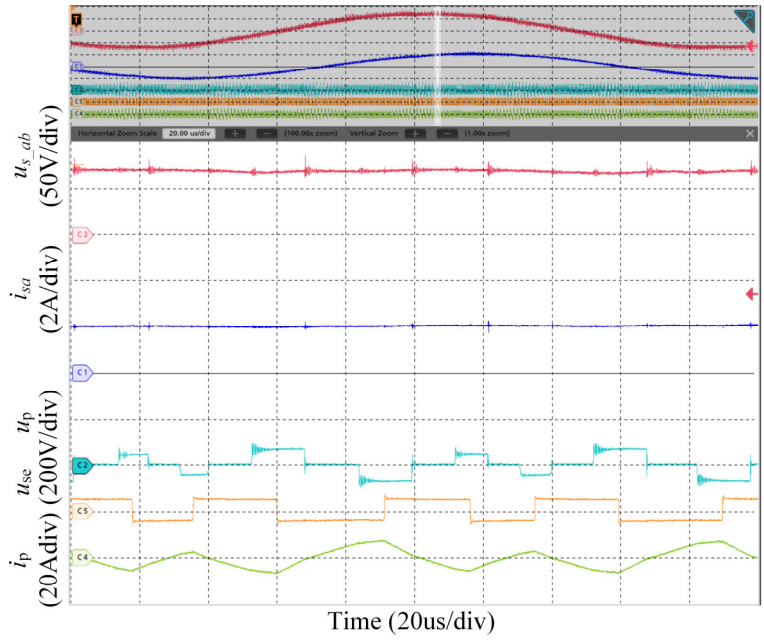


Figure 3.19 Zoom-in waveforms in two switching cycles

The smooth running of the converter indicates the proposed SVM ensures safe commutation. To further verify the commutation process, the primary voltage waveform, and corresponding gating signals for S_{an1}, S_{an2}, S_{bn1}, S_{bn2} are presented in Figure 3.20. When I_7 is applied, S_{an} is turned on and S_{bn} is turned off. In bidirectional switch S_{an}, both the S_{an1} and S_{an2} are turned on, while in S_{bn}, S_{bn1} is turned on while S_{bn2} is turned off. When I_7 transit to I_{1+}, the gating signals for S_{an2} and S_{bn1} are keeping constant. However, S_{an1} is turned off. After 1us, S_{bn2} is turned on, which is coordinated with the theoretical analysis. It takes 1us to finish the commutation process and a two-step commutation is achieved. Similarly, when I_9 transit to I_{1-}, the S_{bn2} is turned off, and then after 1us, S_{an1} is turned on. The sequence is the same as the designed sequence shown in Figure 3.9.

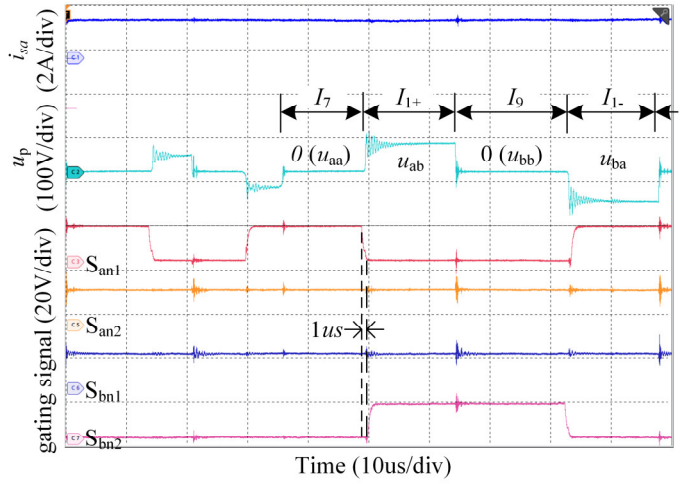


Figure 3.20 The primary voltage waveform and corresponding gating signals for S_{an1}, S_{an2}, S_{bn1}, and S_{bn2}

Figure 3.21 (a) and (b) show the performance comparison of the proposed SVM strategy without and with zero vector optimization (m=0.3). The corresponding low order harmonics and THD of phase current are presented in Table 3.4. The THD of the proposed SVM strategy without optimizing the zero vector is 5.937%. After optimizing the zero vector, the narrow pulses are significantly reduced, and the THD is reduced to 1.445% (the 5^{th}, 7^{th}, 11^{th}, 13^{th} order harmonics are reduced significantly). It can be verified that the modification allows the elimination of narrow pulses and then improve the current quality.

Table 3.4 THD of AC Current with and without Zero Vector Optimization

m=0.3	Without optimization	With optimization
5th	2.996%	0.227%
7th	3.299%	0.278%
11th	2.947%	0.07%
13th	1.255%	0.246%
THD	5.937%	1.445%

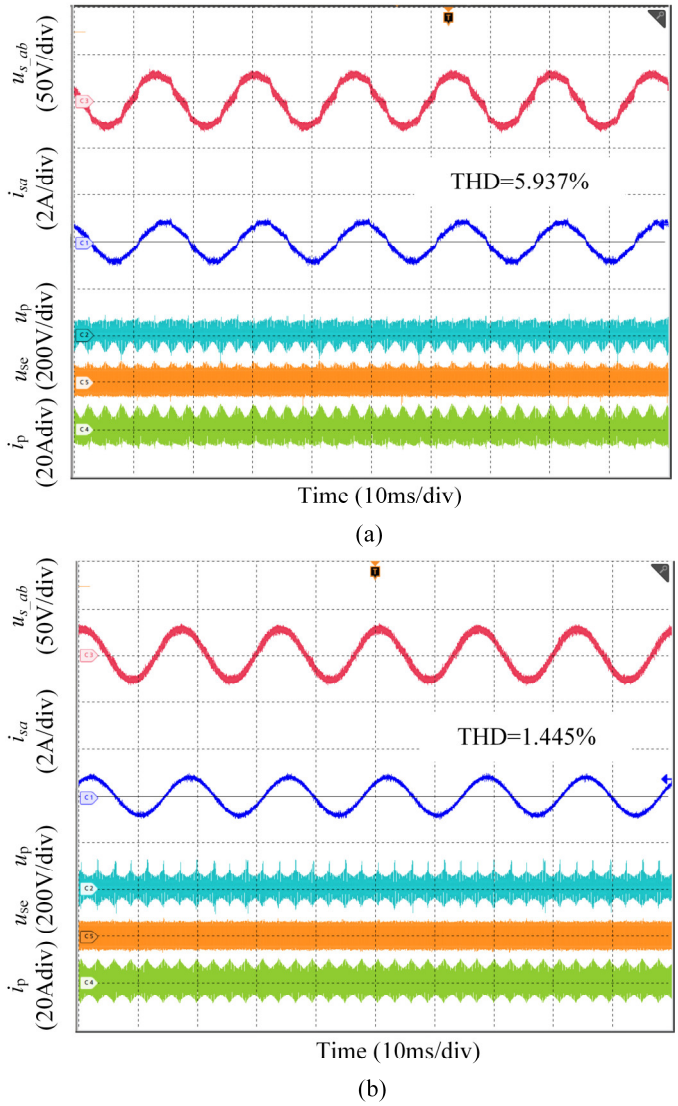


Figure 3.21 Experimental results when *m*=0.3, line-to-line voltage, phase current, primary voltage, secondary voltage, and primary current (from upper to lower) (a) without zero vector optimization (b) with zero vector optimization

3.5 Summary

In this chapter, a new SVM method for isolated AC-DC matrix converter is proposed. The commutation will always happen between two phases with significant differences in magnitude so that sampling errors will not result in the wrong commutation sequence. As narrow pulses can still lead to commutation failure, the impact of narrow pulses is minimized from two aspects: firstly, the two-step commutation sequence is applied to shorten the required commutation time; secondly, the zero vector is optimized in this method to further reduce the possibility of narrow pulses. As a result, the distortion related to narrow pulse processing is also mitigated. Also, the corresponding duty cycles of each vector is calculated to track the current reference. The proposed SVM strategy is preferable in applications where the commutation duty ratio is relatively large.

Chapter 4

An SVM with Reduced Switching Actions and Control Strategy for Isolated AC-DC Matrix Converter

Chapter 3 proposes a 9-segment SVM strategy for the isolated AC-DC matrix converter. It can obtain sinusoidal current even when the commutation duty ratio is large. This method is very effective to traditional MOSFET/IGBT based converters where the switching time requires several *us*. On the other hand, with the development of fast-switching semiconductors (like silicon carbide (SiC) or GaN), the commutation time is reduced significantly. When the switching frequency is not very high (high switching frequency bring in high switching losses and thus result in low efficiency) for WBG based converters, the commutation duty ratio becomes smaller, and the number of switching actions as well as the switching sequence impact on low order harmonics is relatively more important.

Under this condition, an SVM with reduced switching actions is proposed for an isolated AC-DC matrix converter. The number of switching actions is less than the 9-segment SVM strategy. Moreover, both the phase shift angle and modulation index can be regulated, so the peak value of the primary current (current stress) can be optimized with more control variables freedom. The conventional PWM methods can lead to AC current distortions in the isolated AC-DC matrix converter with excessive low order harmonics. To improve the current quality and maintain

---

Publications out of this Chapter:

F. Fang, H. Tian and Y. Li, "SVM Strategy for Mitigating Low-Order Harmonics in Isolated AC–DC Matrix Converter," in *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 583-596, Jan. 2021.

F. Fang, H. Tian and Y. Li, "Coordination Control of Modulation Index and Phase Shift Angle for Current Stress Reduction in Isolated AC–DC Matrix Converter," in *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4585-4596, April 2021.

a low number of switching actions, an improved SVM strategy is proposed in this chapter. The SVM switching sequence and the distribution of zero vectors are designed properly.

Besides, existing control schemes fail to coordinate the modulation index and phase shift angle, and instead focusing on optimizing one of the two variables. This can cause a high peak current on the HFT, leading to high current stress and low efficiency under a light load. To optimize the operation of the isolated AC-DC matrix converter, the coordination control of the modulation index and phase shift angle is proposed in this chapter to reduce the peak current of the transformer.

4.1 Conventional Modulation and Control Methods

The PWM signals should coordinate the 3-1 MC and H-bridge to transfer power because no intermediate energy storage component is used to decouple them. Also, considering the converter contains six bidirectional and four unidirectional switches, reducing the number of switching actions is also important for efficiency. However, in the existing method, high power quality and low switching actions are hard to be simultaneously achieved. The number of switching actions of different modulation strategies is presented in Table 4.1. [59] has six switching actions in 3-1 MC, and four switching actions in H-bridge in one PWM period, but numerous low order harmonics are generated. To achieve high quality current, more switching actions are needed in [63,64]. Therefore, it is very important to develop a PWM strategy to simultaneously obtain a low number of switching actions and high quality current.

Table 4.1 Number of Switching On/Off Actions

Method / Number	Method in Chapter 4	Method in [59]	Method in [63]	Method in [64]	Method in Chapter 3
3-1 MC	6	6	8	11	8
H-bridge	4	4	10	12	8

Besides PWM methods, the control approaches shall also coordinate the operation of 3-1 MC and H-bridge. There are two control variables in the isolated AC-DC matrix converter, the modulation index, and the phase shift angle between the primary side and the secondary side of HFT. However, the existing methods

generally focus on one of the two control variables. For example, a PI controller is used to control the phase shift angle and regulate DC current in [59]. While the modulation index keeps constant based on the grid voltage and DC voltage ratio. In [63], the modulation index is set as 0.707, and the phase shift angle is controlled by a PI controller. Alternatively, a control scheme fixes the phase shift angle as 90° and focuses on controlling the modulation index, so that the power factor and AC current can be regulated [96]. The above control methods for isolated AC-DC matrix converter focus on regulating one control variable, the modulation index, or the phase shift angle between two sides of HFT. The required transferred power can be achieved, but the current stress will be quite significant in a light load condition. The large current stress reduces the utilization rate of the converter hardware, increases the electromagnetic interference, and increases the conduction loss of power switches, and then result in low efficiency [97]. Therefore, it is necessary to develop a new method for isolated AC-DC matrix converter to minimize the HFT current stress.

Targeting a low number of switching actions and high quality waveforms, this chapter proposes an SVM strategy for isolated AC-DC matrix converter. Compared with SPWM methods, SVM can obtain additional degrees of freedom, i.e, the switching sequence and vector distribution, to improve the performance. Firstly, the conventional PWM strategy in [59], which can achieve a low number of switching actions, is introduced. The cause of low order harmonics is analyzed by a mathematical model based on Fourier transform. To mitigate the low order harmonics, the switching sequence is properly designed in the proposed SVM strategy. The low order harmonics can be significantly reduced in most conditions. However, when both the modulation index and phase shift angle are large, the harmonic distortions will appear. To solve this problem, the proposed SVM strategy redistributes the zero vector. As a result, the harmonic distortions can be maintained at a low level in any combinations of modulation index and phase shift angle.

Moreover, this chapter optimizes both the modulation index and phase shift angle to reduce current stress and improve the efficiency of the isolated AC-DC matrix converter. Since the number of modulation index and phase shift angle

combinations can be infinite, developing the method to find out the combination to reduce current stress is necessary. Based on the proposed SVM strategy, the peak current and transferred power can be calculated, and the optimal combination of the modulation index and phase shift angle is achieved to reduce current stress.

4.2 SVM Strategy for Isolated AC-DC Matrix Converter

4.2.1 Improved Switching Sequence

The isolated converter topology, switching vectors, and switching states are the same as in Chapter 3. To ensure the performance of the converter, the proposed SVM strategy improves the sequence and the distribution of zero vectors. The current reference can be synthesized by two adjacent active vectors and one zero vector. Assuming the current reference in sector I, the vectors I_1, I_2, and I_0 will be used. Applying the Ampere-second balance equation in (4.1), the duty cycle of each vector can be calculated by (4.2).

$$I_{ref}\, T_s = I_0 T_0 + I_1\, T_1 + I_2 T_2 \tag{4.1}$$

$$\begin{aligned} T_1 &= m T_s \sin(\pi/6 - \theta); \\ T_2 &= m T_s \sin(\pi/6 + \theta); \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{4.2}$$

where m is the modulation index, T_S is the switching cycle, θ is the current reference angle $\theta \in [-\pi/6, \pi/6)$.

The switching states and voltage waveforms of the conventional SVM strategy and proposed SVM strategy are shown in Figure 4.1. It shows that the sequence of $I_{1\text{-}}$ and $I_{2\text{-}}$ are swapped in the proposed method. The different sequences are named sequence 1 (sequence of conventional SVM strategy) and sequence 2 (sequence of proposed SVM strategy). With the different sequences, the 3-1 MC can produce different voltage waveforms and apply them to the primary side of HFT. However, the secondary voltages are still the same. Also, the proposed SVM strategy has the same number of switching actions as conventional SVM, the number of switching actions in 3-1 MC is 6, and the number in H-bridge is 4 in one switching cycle.

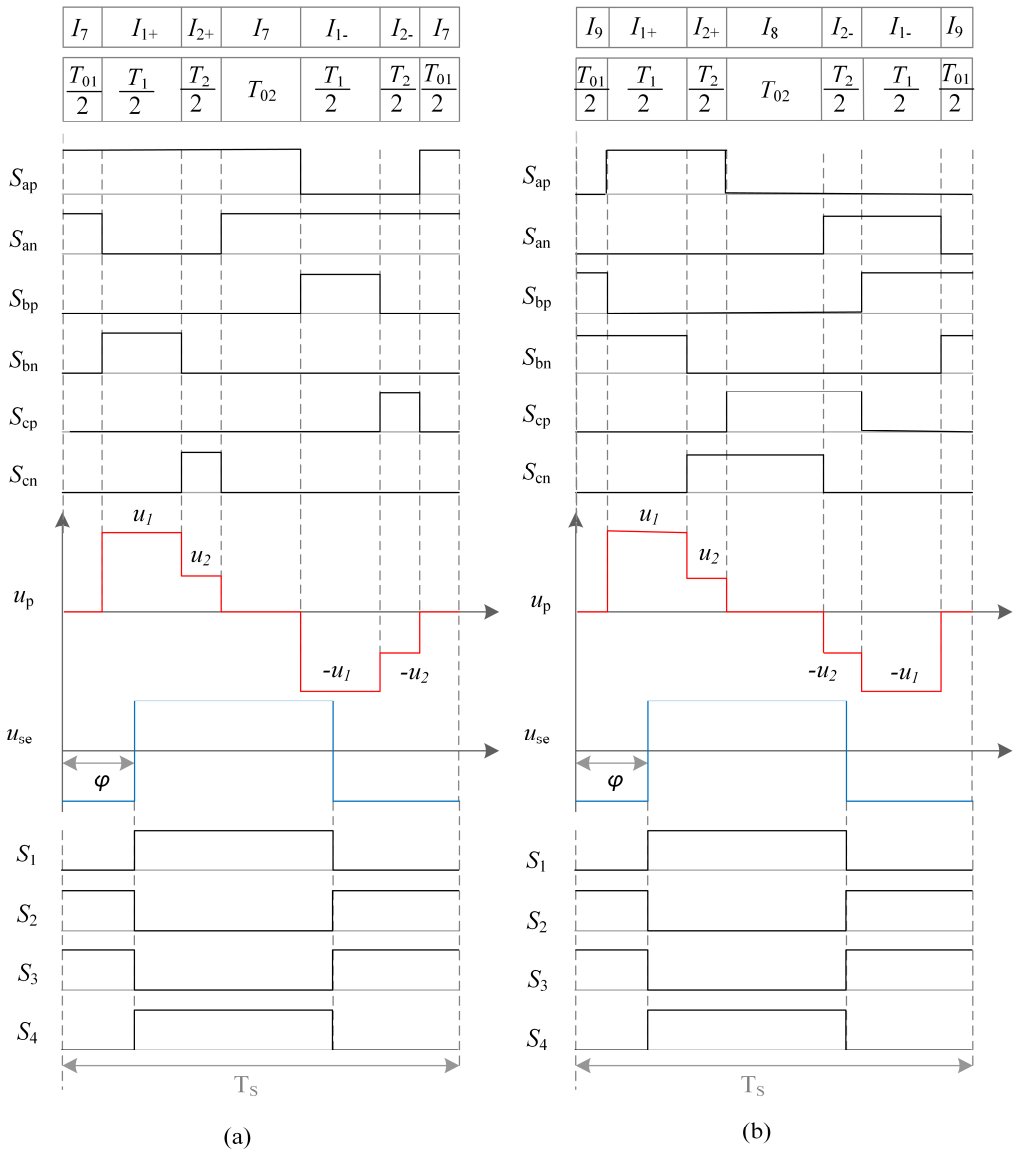


Figure 4.1 Waveforms of the primary voltage (u_p) and secondary voltage (u_{se}) of HFT (a) sequence 1 in conventional SVM (b) sequence 2 in proposed SVM

Besides the difference in switching sequence, the distribution of zero vector in the proposed SVM strategy is different from the conventional SVM strategy. On one hand, the distribution time of the zero vector is different. Although the total duty cycle of the zero vector is still the same, the distribution of the zero vector in the proposed method is changed to improve the current quality. In the conventional SVM, the duty cycle of zero vector in each switching period is simply distributed equally (T_{01}=T_{02}). However, the duty cycle of T_{01} and T_{02} are not equal anymore in the proposed SVM strategy, which can be calculated by (4.3).

$$T_{01} = \left\{ \frac{1}{2} + \frac{m}{\sqrt{3}} \sin\left(\theta - \frac{\pi}{3} \right) \right\} T_s$$
$$T_{02} = \left\{ \frac{1}{2} - \frac{m}{\sqrt{3}} \sin\left(\theta + \frac{\pi}{3} \right) \right\} T_s \qquad (4.3)$$

where $m \leq 0.866$.

On the other hand, the applied zero vector is different in each sector. For example, in sector I, only zero vector I_7 is used in the conventional SVM strategy. While I_8 and I_9 are applied in the proposed SVM strategy. To ensure the safe commutation of bidirectional switches, the pulse width is required to be larger than the commutation time. In the conventional SVM strategy, the requirement is shown in (4.4).

$$\frac{1}{2} T_{01} > T_c$$
$$\frac{1}{2} T_1 > T_c \qquad (4.4)$$
$$\frac{1}{2} T_2 > T_c$$

where T_c is commutation time.

However, to ensure safe commutation in the proposed SVM strategy, the requirement of pulse width is

$$\frac{1}{2} T_{01} > T_c$$
$$\frac{1}{2} \left(T_1 + T_2 \right) > T_c \qquad (4.5)$$
$$\frac{1}{2} T_2 + T_{02} > T_c$$

The pulse which is narrower than the commutation time should be extended or discarded to avoid commutation failure. However, either extending or discarding the narrow pulse can result in distortion. In the conventional SVM strategy, narrow pulses occur in the shaded area in Figure 4.2(a). It can be observed that the area of narrow pulses increases with the decrease of the modulation index. However, after optimizing the zero vector, the narrow pulse can be reduced significantly in the proposed SVM strategy, as shown in Figure 4.2(b). The remaining narrow pulses are extended to ensure safe commutation.

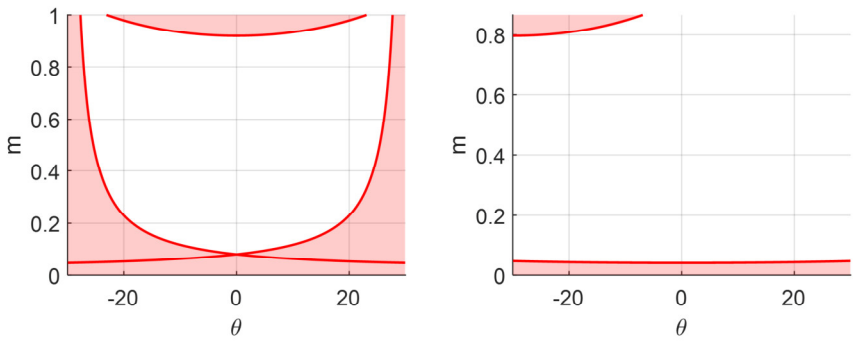


Figure 4.2 Narrow pulse varies with modulation index and current angle (d_c=0.02) (a) conventional SVM method (b) proposed SVM method

To comprehensively compare the performance of conventional SVM strategy and proposed SVM strategy, three cases are used in the comparison in this section, which is shown in Table 4.2. Case 1 represents the conventional SVM strategy. While Case 2 is used to verify the effectiveness of improved switching sequences in the proposed SVM strategy. Case 3 represents the proposed SVM strategy which improves not only the switching sequence but also the distribution of zero vector.

Table 4.2 Different Cases Used for Comparisons

	Case 1	Case 2	Case 3
Sequence	Sequence 1	Sequence 2	Sequence 2
Zero Vector Distribution	T_{01}=T_{02}	T_{01}=T_{02}	T_{01}≠T_{02} (4.3)

4.2.2 6th Order Harmonics in Transferred Power

To verify the proposed SVM strategy, the power quality of the three cases are compared in this section. As discussed, the distribution of zero vectors can be improved to reduce current distortions. To do this, it is necessary to build the mathematical model and find out the factors to cause harmonic distortions. In this section, the principle of the current distortions will be derived.

As can be seen from Figure 4.1, the primary voltage of HFT is an alternating staircase wave. The stair voltage u_1 and u_2 are line-to-line voltages, which can be described as

$$\begin{aligned} u_1 &= \sqrt{2}u_{ll}\sin\left(\theta+\frac{2\pi}{3}+\psi\right) \\ u_2 &= \sqrt{2}u_{ll}\sin\left(\theta+\frac{\pi}{3}+\psi\right) \end{aligned} \tag{4.6}$$

where u_{ll} is the root mean square (RMS) value of the line-to-line voltage of the grid, ψ is the power factor angle.

From the above analysis, both the amplitude of the stairs and their duty cycles vary as the θ changes from cycle to cycle. Hence, it is difficult to calculate the transferred power directly. According to the Fourier series theorem, any periodic waveform can be described as the sum of sine and cosine functions, which provides an alternative way to calculate the transferred power.

The Fourier series and the calculation of coefficients are given in (4.7).

$$\begin{aligned} x(t) &= a_0 + \sum_{n=1}^{\infty}\left(a_n \cos n\omega t + b_n \sin n\omega t\right) \\ a_0 &= \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} x(\mathrm{t})dt \\ a_n &= \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} x(\mathrm{t})\cos n\omega t dt \\ b_n &= \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} x(\mathrm{t})\sin n\omega t dt \end{aligned} \tag{4.7}$$

where x(t) is the periodic waveform, a_0, a_n and b_n are coefficients.

$$\begin{aligned} a_{1n} &= \frac{1}{n\pi}\left\{\begin{array}{l} u_1\left(1-\cos n\pi\right)\left[\sin\left(n\omega_s\frac{0.5T_0+T_1}{2}\right)-\sin\left(n\omega_s\frac{0.5T_0}{2}\right)\right] \\ +u_2\left(1-\cos n\pi\right)\left[\sin\left(n\omega_s\frac{0.5T_0+T_1+T_2}{2}\right)-\sin\left(n\omega_s\frac{0.5T_0+T_1}{2}\right)\right] \end{array}\right\} \\ b_{1n} &= \frac{1}{n\pi}\left\{\begin{array}{l} u_1\left(1-\cos n\pi\right)\left[-\cos\left(n\omega_s\frac{0.5T_0+T_1}{2}\right)+\cos\left(n\omega_s\frac{0.5T_0}{2}\right)\right] \\ +u_2\left(1-\cos n\pi\right)\left[-\cos\left(n\omega_s\frac{0.5T_0+T_1+T_2}{2}\right)+\cos\left(n\omega_s\frac{0.5T_0+T_1}{2}\right)\right] \end{array}\right\} \end{aligned} \tag{4.8}$$

$$\begin{aligned} a_{2n} &= 0 \\ b_{2n} &= \frac{2\cos n\pi}{n\pi}\left\{\begin{array}{l} u_1\left[-\cos\left(n\omega_s\frac{0.5T_0+T_2}{2}\right)+\cos\left(n\omega_s\frac{0.5T_0+T_2+T_1}{2}\right)\right] \\ +u_2\left[-\cos\left(n\omega_s\frac{0.5T_0}{2}\right)+\cos\left(n\omega_s\frac{0.5T_0+t_2}{2}\right)\right] \end{array}\right\} \end{aligned} \tag{4.9}$$

$$a_{3n}=0$$

$$b_{3n}=\frac{2\cos n\pi}{n\pi}\begin{Bmatrix}u_1\left[-\cos\left(n\omega_s\frac{T_{02}+T_2}{2}\right)+\cos\left(n\omega_s\frac{T_{02}+T_2+T_1}{2}\right)\right]\\+u_2\left[-\cos\left(n\omega_s\frac{T_{02}}{2}\right)+\cos\left(n\omega_s\frac{T_{02}+T_2}{2}\right)\right]\end{Bmatrix} \quad (4.10)$$

Hence, the primary voltage of Case 1, Case 2, and Case 3 are calculated as (4.11-4.13).

$$u_{1p}=\sum_{n=1,3\ldots}^{\infty}\left[a_{1n}\cos\left(n\omega_s t\right)+b_{1n}\sin\left(n\omega_s t\right)\right] \quad (4.11)$$

$$u_{2p}=\sum_{n=1}^{\infty}b_{2n}\sin\left(n\omega_s t\right) \quad (4.12)$$

$$u_{3p}=\sum_{n=1}^{\infty}b_{3n}\sin\left(n\omega_s t\right) \quad (4.13)$$

where $\omega_s=2\pi f_s$ and f_s is the switching frequency, n is harmonic order, the coefficients a_{1n}, b_{1n}, b_{2n} and b_{3n} are given in (4.14-4.16).

$$\begin{aligned}a_{1n}&=\frac{2\sqrt{6}u_{ll}}{n\pi}\sin\left(\frac{1}{2}n\pi\right)A_n\\b_{1n}&=\frac{2\sqrt{6}u_{ll}}{n\pi}\sin\left(\frac{1}{2}n\pi\right)B_n\end{aligned} \quad (4.14)$$

$$b_{2n}=\frac{-2\sqrt{6}\,\mathrm{u}_{ll}\cos\left(n\pi\right)}{n\pi}\left\{\cos\left(\frac{n\pi}{2}\right)A_n+\sin\left(\frac{n\pi}{2}\right)B_n\right\} \quad (4.15)$$

$$b_{3n}=\frac{-2\sqrt{6}u_{ll}\cos\left(n\pi\right)}{n\pi}\left\{\cos\left(\frac{1}{2}n\pi\right)C_n+\sin\left(\frac{1}{2}n\pi\right)D_n\right\} \quad (4.16)$$

where A_n, B_n, C_n, and D_n are given in (4.17-4.18).

$$\begin{aligned}A_n&=\frac{\sin\left(\theta+\psi\right)}{\sqrt{3}}\left(\cos\left(\frac{n\pi m\cos\theta}{2}\right)-\cos\left(\frac{\sqrt{3}n\pi m\sin\theta}{2}\right)\right)\\B_n&=\frac{\sin\left(\theta+\psi\right)}{\sqrt{3}}\sin\left(\frac{\sqrt{3}n\pi m\sin\theta}{2}\right)+\cos\left(\theta+\psi\right)\sin\left(\frac{n\pi m\cos\theta}{2}\right)\end{aligned} \quad (4.17)$$

$$C_n = -\cos(\theta+\psi)\sin\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\sin\left(\frac{mn\pi\cos\theta}{2}\right) + \frac{\sin(\theta+\psi)}{\sqrt{3}}\left\{\cos\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\cos\left(\frac{mn\pi\cos\theta}{2}\right) - \cos\left(\frac{mn\pi\sin\theta}{\sqrt{3}}\right)\right\} \quad (4.18)$$

$$D_n = \cos(\theta+\psi)\cos\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\sin\left(\frac{mn\pi\cos\theta}{2}\right) + \frac{\sin(\theta+\psi)}{\sqrt{3}}\left\{\sin\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\cos\left(\frac{mn\pi\cos\theta}{2}\right) + \sin\left(\frac{mn\pi\sin\theta}{\sqrt{3}}\right)\right\}$$

The secondary voltage of the three cases is the same, which can be described as (4.19).

$$u_{se} = \sum_{n=1,3...}^{\infty}\left\{b_{4n}\sin\left(n\omega_s t - n\pi\frac{\varphi}{180}\right)\right\} \quad (4.19)$$

where

$$b_{4n} = 4u_{dc}/(n\pi) \quad (4.20)$$

where u_{dc} is the DC voltage.

It can be found that the amplitude of the primary voltage is determined by u_{ll}, m, θ, ψ and n. However, the amplitude of the secondary voltage is only determined by u_{dc} and n. Because only the same order voltage and current can produce active power, the transferred active power of three cases in one switching cycle can be calculated as (4.21-4.23).

$$P_1 = \sum_{n=1,3...}^{\infty}\frac{P_b}{n^3}\sin\left(\frac{1}{2}n\pi\right)\left\{A_n\cos(n\varphi) + B_n\sin(n\varphi)\right\} \quad (4.21)$$

$$P_2 = \sum_{n=1,3...}^{\infty}\frac{P_b}{n^3}\sin\left(\frac{n\pi}{2}\right)B_n\sin n\varphi \quad (4.22)$$

$$P_3 = \sum_{n=1,3..}^{\infty}\frac{P_b}{n^3}\sin\left(\frac{n\pi}{2}\right)D_n\sin n\varphi \quad (4.23)$$

where P_b is the based power, shown in (4.24).

$$P_b = \frac{4\sqrt{6}u_{ll}Nu_{dc}}{\pi^2\omega_s L_k} \quad (4.24)$$

All the components of transferred power can be normalized by P_b. The P_b is the based power, which is determined by u_{ll}, N, u_{dc}, f_s, and L_k. The normalized transferred power contains infinite components and is determined by n, m, θ, ψ and φ. In one switching cycle, the transferred power is affected by the current reference

angle θ. Therefore, the transferred power contains 6th order harmonic in one grid frequency cycle.

Assuming the power factor is unity (ψ=0), the 6th order power ripple of Case 1 and Case 2 can be calculated and depicted in Figure 4.3(a) and Figure 4.3(b). The power ripple increases with the increase of m and φ. Under the same combination, the power ripple of Case 2 is smaller than that in Case 1. In Case 1, when m increases, the power ripple increase significantly. While for Case 2, the power ripple is large only when both m and φ are high.

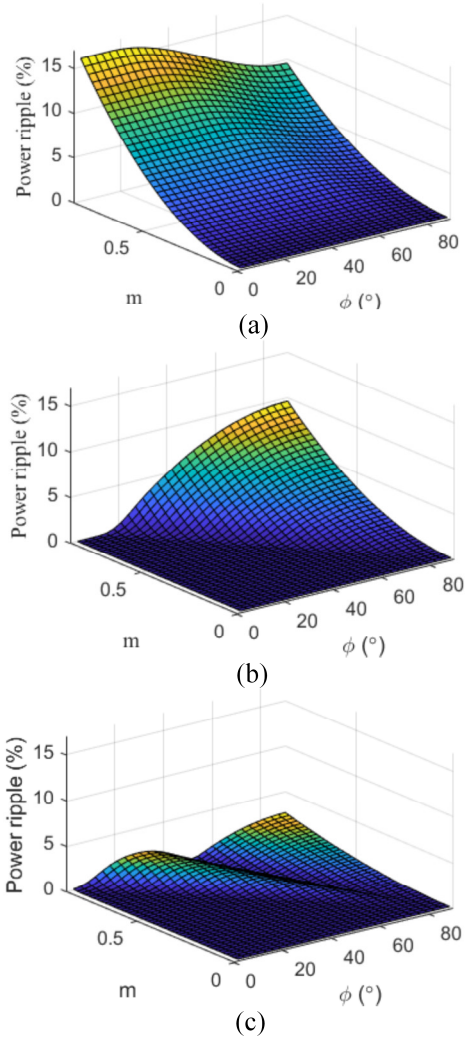


Figure 4.3 Transferred power ripple (in percentage) (a) Case 1 (b) Case 2 (c) Case 3

Through the above analysis, it shows that Case 2 has better performance than Case 1. The reason for the 6th order harmonic in transferred power is that the

primary voltage is affected by the current reference angle. To reduce the distortion in transferred power and thus improve the input current quality further, the zero vector can be redistributed. After redistributing the zero vector, the power ripple is kept at a very low level in the wide operation range, as shown in Figure 4.3(c). In particular, the power ripple is reduced when both m and φ are of high values. Hence, the 6th order ripple of transferred power can be significantly reduced with the method in Case 3. Besides, though the modulation index is smaller than 0.866, the maximum power is only reduced from P_b to $0.978P_b$.

4.2.3 Low Order Harmonics in Phase Current

Considering the 6th order harmonic in transferred power would result in 5th and 7th order harmonics in AC current, the current will be distorted. To verify this, the 5th and 7th order harmonics of three cases are calculated based on a double Fourier analysis. The double control variables function $f(x, y)$ can be expressed as (4.25), the coefficient is calculated by (4.26) [98].

$$\begin{aligned} f(x,y) = \frac{A_{00}}{2} &+ \sum_{q=1}^{\infty}\left(A_{0q}\cos qy + B_{0q}\sin qy\right) \\ &+ \sum_{p=1}^{\infty}\left(A_{p0}\cos px + B_{p0}\sin px\right) \\ &+ \sum_{p=1}^{\infty}\sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty}\left\{A_{pq}\cos(px+qy) + B_{pq}\sin(px+qy)\right\} \end{aligned} \tag{4.25}$$

$$A_{pq} + jB_{pq} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} f(x,y)\,\mathrm{e}^{j(\mathrm{p}x+qy)}\,dxdy \tag{4.26}$$

where $x(t)=\omega_s t+\theta_s$, $y(t)=\omega_0 t+\theta_0$, ω_s and ω_0 are the switching frequency and the modulating frequency, θ_s and θ_0 are the initial phase shift angles, and p, q are multiples. A_{00} represents the DC component of the PWM waveform, the second term represents the fundamental and low order harmonics components. While the third and fourth terms represent the switching frequency and sideband switching frequency harmonics.

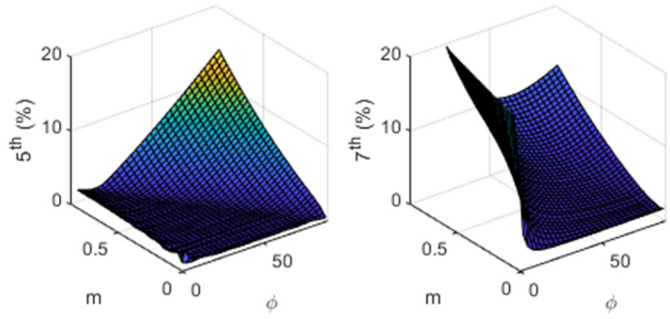
Under three-phase current is the symmetrical condition, taking phase A current as an example to calculate the 5th and 7th order harmonics. Figure 4.4 shows the 5th and 7th order harmonics of Case 1. It can be observed that the 5th order harmonic is

high when both m and φ are high. While the 7th order harmonic increases with the increase of m. Both the 5th and 7th order harmonics are greater than 4% of the rated current (the rated current is achieved when m and φ are high), which cannot meet the requirement in the IEEE standard [62] (as shown in Table 4.3).

After improving the switching sequence in Case 2, the 7th order harmonic can be reduced significantly, as shown in Figure 4.5. However, the 5th order harmonic is still higher than 4% when m and φ are high. Therefore, at rated current, the 5th order harmonic cannot meet the requirement in Table 4.3. In Case 3, both 5th and 7th order harmonics are lower than 4% with any combination of m and φ, as shown in Figure 4.6. Even though the value of 5th and 7th order harmonics are related to the model parameters, the trend of 5th and 7th order harmonics are similar to the trend of power ripple.

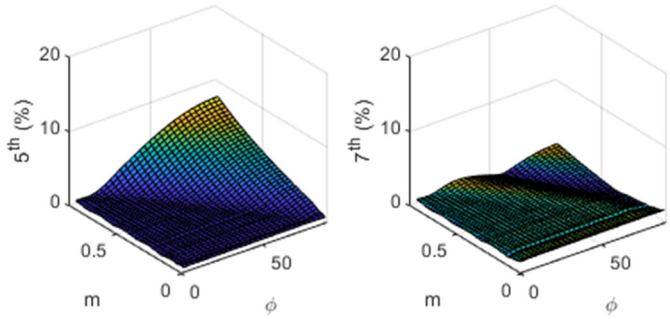
Table 4.3 Maximum Odd Harmonic Current Distortion in Percent of Rated Current

Individual odd harmonic order	h<11	h<17	h<23	h<35	h>35	THD
Limit	4%	2%	1.5%	0.6%	0.3%	5%



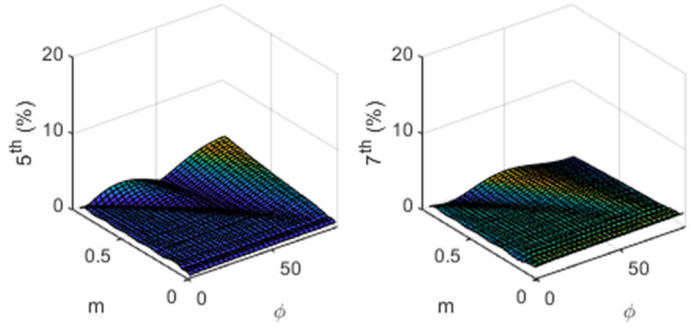
(a) **(b)**

Figure 4.4 Low order harmonics with different m and φ combination of Case 1 (a) 5th order harmonic (b) 7th order harmonic



(a) **(b)**

Figure 4.5 Low order harmonics with different m and φ combination of Case 2 (a) 5th order harmonic (b) 7th order harmonic



(a) **(b)**

Figure 4.6 Low order harmonics with different *m* and *φ* combination of Case 3 (a) 5th order harmonic (b) 7th order harmonic

4.3 Coordination Control of Modulation Index and Phase Shift Angle for Current Stress Reduction

4.3.1 Transferred Power and Peak Current Calculation

As shown in Figure 4.1, the primary voltage waveform of HFT is not a square wave. The duty cycles of each vector and the magnitude of line-to-line voltage are changed with different current reference angle, therefore, the transferred power and primary current cannot be calculated directly. In this section, the multi-frequency component approximation is used to analyze the voltage waveforms.

The primary voltage can be expressed by Fourier series,

$$u_p = \sum_{n=1}^{\infty} \left\{ a_n \sin\left(n\omega_s t\right) \right\} \tag{4.27}$$

where, $\omega_s = 2\pi f_s$, f_s is the switching frequency, n is harmonic order.

The amplitude of each order component of primary voltage can be rewritten as:

$$a_n = \frac{-2\sqrt{6}u_{ll}}{n\pi}\cos\left(n\pi\right)\left\{\sin\left(\frac{n\pi}{2}\right)A_n + \cos\left(\frac{n\pi}{2}\right)B_n\right\} \tag{4.28}$$

where A_n, B_n are given in (4.29).

$$
\begin{aligned}
A_n &= \cos(\theta+\psi)\cos\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\sin\left(\frac{mn\pi\cos\theta}{2}\right) \\
&\quad + \frac{\sin(\theta+\psi)}{\sqrt{3}}\left[\sin\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\cos\left(\frac{mn\pi\cos\theta}{2}\right)+\sin\left(\frac{mn\pi\sin\theta}{\sqrt{3}}\right)\right] \\
B_n &= -\cos(\theta+\psi)\sin\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\sin\left(\frac{mn\pi\cos\theta}{2}\right) \\
&\quad + \frac{\sin(\theta+\psi)}{\sqrt{3}}\left[\cos\left(\frac{mn\pi\sin\theta}{2\sqrt{3}}\right)\cos\left(\frac{mn\pi\cos\theta}{2}\right)-\cos\left(\frac{mn\pi\sin\theta}{\sqrt{3}}\right)\right]
\end{aligned}
\tag{4.29}
$$

According to the Fourier series, the secondary voltage of HFT can be written as

$$
\begin{aligned}
u_{se} &= \sum_{n=1,3,5\ldots}^{\infty}\left\{b_n\sin(n\omega_s t - n\varphi)\right\} \\
b_n &= \frac{4u_{dc}}{n\pi}
\end{aligned}
\tag{4.30}
$$

The primary voltage and secondary voltage are connected through L_k, the primary current can be presented as

$$
L_k\frac{i_p(t)-i_p(0)}{dt} = u_p(t) - Nu_{se}(t) \tag{4.31}
$$

Based on the current symmetry and the average current is zero in one switching period, the primary current can be calculated as (4.32).

$$
i_p(t) = \sum_{n=1,3..}^{\infty} c_n\sin\left(n\omega_s t + \operatorname{atan}\left(\frac{Nb_n\cos(n\varphi)-a_n}{Nb_n\sin(n\varphi)}\right)\right) \tag{4.32}
$$

$$
c_n = \frac{\sqrt{\left(Nb_n\cos(n\varphi)-a_n\right)^2+\left(Nb_n\sin(n\varphi)\right)^2}}{n\omega_s L_k} \tag{4.33}
$$

where c_n represent each order amplitude of the primary current.

The primary voltage of HFT can be described as a combination of series harmonics components, while the secondary voltage only contains odd order harmonics. For the same order component, the primary voltage is the leading secondary voltage φ degree. Due to the primary voltage and secondary voltage contain periodic components, they can be rewritten into phasor expressions as

$$U_P = \sum_{n=1,2,3\ldots} \frac{a_n}{\sqrt{2}}$$
$$U_{Se} = \sum_{n=1,3,5\ldots} \frac{b_n \left\{\cos\left(n\varphi\right) - j\sin\left(n\varphi\right)\right\}}{\sqrt{2}} \quad (4.34)$$

The primary voltage and secondary voltage are connected through L_k. The primary current I_P and apparent power S of the HFT can be calculated by the primary voltage and primary current, as (4.35), (4.36). In one switching cycle the peak current square and the transferred power can be obtained. The peak current square is normalized by I_{pb} (presented in (4.39)) and shown in (4.37). The transferred power can be normalized by P_b and the normalized power is presented in (4.38).

$$I_p = \sum_{n=1,3,5\ldots}^{\infty} \frac{U_P - NU_{Se}}{jn\omega_s L_k} = \sum_{n=1,3,5\ldots}^{\infty} \frac{\frac{a_n}{\sqrt{2}} - \frac{Nb_n}{\sqrt{2}}\left(\cos n\varphi - j\sin n\varphi\right)}{jn\omega_s L_k}$$
$$= \sum_{n=1,3,5\ldots}^{\infty} \frac{j\left(Nb_n\cos n\varphi - a_n\right) + Nb_n \sin n\varphi}{\sqrt{2}n\omega_s L_k} \quad (4.35)$$

$$S = U_P \frac{U_P - NU_{Se}}{j\omega_s L_k} = \sum_{n=1,3,5\ldots}^{\infty} a_n \frac{a_n - Nb_n\left\{\cos\left(n\varphi\right) - j\sin\left(n\varphi\right)\right\}}{j2n\omega_s L_k}$$
$$= \sum_{n=1,3,5\ldots}^{\infty} a_n \frac{a_n - Nb_n\left\{\cos\left(n\varphi\right) - j\sin\left(n\varphi\right)\right\}}{j2n\omega_s L_k} \quad (4.36)$$
$$= \sum_{n=1,3,5\ldots}^{\infty} \frac{a_n Nb_n \sin\left(n\varphi\right)}{2n\omega_s L_k} + j\frac{a_n\left\{Nb_n\cos\left(n\varphi\right) - a_n\right\}}{2n\omega_s L_k} = P + jQ$$

$$I_{pu}^2 = \frac{I_{peak}^2}{I_{pb}^2} = \sum_{n=1,3..}^{\infty} \frac{1}{n^4}\left\{3A_n^2 + 2\left(\frac{Nu_{dc}}{u_{ll}}\right)^2 - 2\sqrt{6}\left(\frac{Nu_{dc}}{u_{ll}}\right)\sin\left(\frac{n\pi}{2}\right)\cos\left(n\varphi\right)A_n\right\} \quad (4.37)$$

$$P_u = \frac{P}{P_b} = \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^3}\sin\left(\frac{n\pi}{2}\right)\sin n\varphi A_n \quad (4.38)$$

$$I_{pb} = \frac{2\sqrt{2}u_{ll}}{\pi\omega_s L_k} \quad (4.39)$$

$$P_b = \frac{4\sqrt{6}u_{ll}Nu_{dc}}{\pi^2\omega_s L_k} \quad (4.40)$$

The converter is used to achieve conversion between AC side and the DC side, only active power is transferred between the two sides. The transferred power is theoretically equal to active power at the AC side. For the primary voltage and the secondary voltage with different order harmonic components, the transferred power is zero. Only the same order components of the primary voltage and secondary voltage can generate primary current and transferred power. I_{pu}^2 represents the peak current square of primary current and P_u is the normalized transferred power, which contains infinite order components. I_{pu1}^2, I_{pu3}^2, and I_{pu5}^2 are the fundamental, 3rd, and 5th order components of peak current square. P_{u1}, P_{u3}, and P_{u5} are the fundamental, 3rd, and 5th order components.

Figure 4.7 illustrates how the total normalized peak current square, the fundamental, 3rd, and 5th order components vary with the phase shift angle. Besides, Figure 4.8 depicts how the normalized transferred power varies with the phase shift angle, where P_u, P_{u1}, P_{u3}, and P_{u5} represent the total normalized transferred power, fundamental, 3rd, and 5th order transferred power components (assuming the power factor angle is 0, m=0.8, and Nu_{dc}/u_{ll}=0.8).

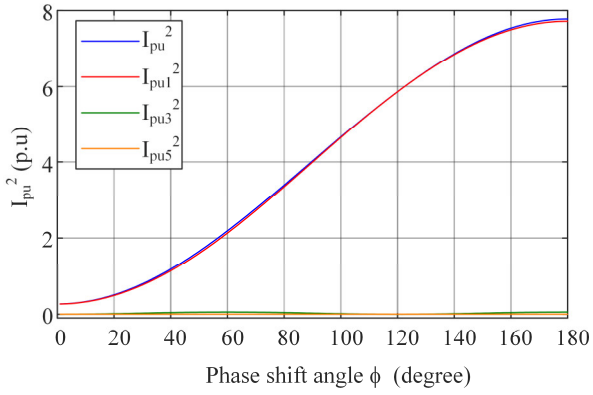


Figure 4.7 Normalized peak current square under different phase shift angle

It shows that the peak current square increase with phase shift angle increases, while the transferred power is axis symmetry at φ=90°. Secondly, the fundamental components have the largest proportion and are consistent with the whole total transferred power and peak current. Hence, it can be concluded that the fundamental component is the majority part of the peak current or transferred power, which can be used to represent the peak current or transferred power with a negligible error.

Besides, to obtain a small peak current, the phase shift angle is limited in [0°,90°] when power flows from the AC side to the DC side.

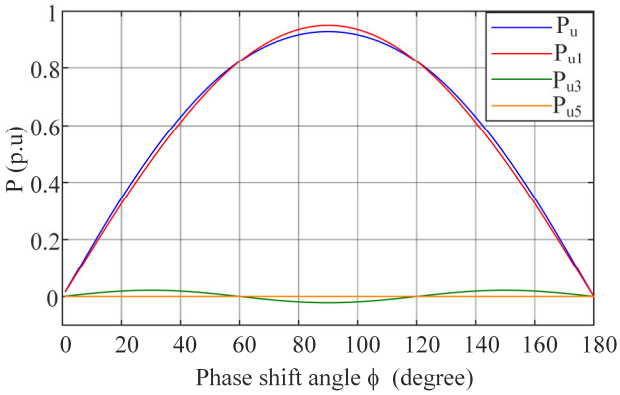


Figure 4.8 Normalized transferred power under different phase shift angle

The fundamental transferred power and the square of peak current are presented in (4.41), (4.42).

$$P = P_b \sin\left(\frac{m\pi}{2}\right)\sin\varphi\cos\psi \tag{4.41}$$

$$I_{peak}^2 = I_{pb}^2\left(3\sin^2\left(\frac{m\pi}{2}\right)\cos^2\psi + 2\left(\frac{Nu_{dc}}{u_{ll}}\right)^2 - 2\sqrt{6}\left(\frac{Nu_{dc}}{u_{ll}}\right)\sin\left(\frac{m\pi}{2}\right)\cos\psi\cos\varphi\right) \tag{4.42}$$

The transferred power flows from the bridge with a leading phase angle to the bridge with a lagging phase angle. Moreover, the transferred power is related to two controllable variables, one is a modulation signal which determines the primary voltage. The other is the phase shift angle φ. To minimize current stress with the required transferred power, the relationship of two control variables should be researched.

4.3.2 Control Variables Combination

The current stress optimization problem can be described as finding an improved parameter that minimizes the current stress with the required transferred power. The optimization problem is formulated in the standard form (4.43).

$$\min I_{peak}^2 \quad \text{, subject to } P^* = P \tag{4.43}$$

In mathematics, the Lagrange multiplier method [99] is used to solve this

problem.

$$L = I_{peak}^2 + \lambda\left(P - P^*\right) \tag{4.44}$$

where L is the Lagrangian function, λ is the Lagrangian multiplier and $\lambda \neq 0$, P^* is a transferred power reference.

To track the transferred power reference and minimum peak current, the function should be minimized,

$$\frac{\partial L}{\partial m} = 0; \quad \frac{\partial L}{\partial \varphi} = 0 \tag{4.45}$$

Solving (4.46), the minimum current stress and the improved control parameters can be derived as

$$Nu_{dc} = 1.2247 u_{ll} \sin\left(0.5m\pi\right)\cos\psi\cos\varphi \tag{4.46}$$

The relationship of the phase shift angle and modulation index can be presented by (4.48).

$$\varphi = ar\cos\left(\frac{Nu_{dc}}{1.2247 u_{ll}\sin\left(0.5m\pi\right)\cos\psi}\right) \tag{4.47}$$

The Lagrange multipliers yields the necessary condition for optimality in constrained problems. To verify the local optimal solution is the global solution, the sufficient condition should be added. The Hessian of the peak current square (*f* represents the peak current square function in (4.42)) is given as

$$\nabla^2 f = \begin{bmatrix} \dfrac{\partial^2 f}{\partial m^2} & \dfrac{\partial^2 f}{\partial m \partial \varphi} \\ \dfrac{\partial^2 f}{\partial \varphi \partial m} & \dfrac{\partial^2 f}{\partial \varphi^2} \end{bmatrix} = \begin{bmatrix} A_1 & A_2 \\ A_3 & A_4 \end{bmatrix} \tag{4.48}$$

where

$$A_1 = I_{pb}^2 \left\{ 1.5\pi^2 \cos\left(m\pi\right)\cos^2\psi + \frac{\sqrt{6}\pi^2}{2}\frac{Nu_{dc}}{u_{ll}}\sin\left(\frac{m\pi}{2}\right)\cos\psi\cos\varphi \right\}$$

$$A_2 = A_3 = \sqrt{6}\pi\frac{Nu_{dc}}{u_{ll}}\cos\left(\frac{m\pi}{2}\right)\cos\psi\sin\varphi$$

$$A_4 = 2\sqrt{6}\frac{Nu_{dc}}{u_{ll}}\sin\left(\frac{m\pi}{2}\right)\cos\psi\cos\varphi$$

In feasible region, with the relationship of modulation index and phase shift angle in (4.47), the matrix in (4.48) is positive definite. Therefore, the achieved peak current square is the optimal minimum value [100].

With the relationship in (4.48), the optimum combination is achieved [101]. The primary voltage of HFT is synthesized by the capacitor voltages with corresponding duty cycles. In one switching cycle, the average value can be calculated as (4.49).

$$u_{\mathrm{p\_}average} = u_{ab}T_1 / \mathrm{T_S} + u_{ac}T_2 / \mathrm{T_S} = 1.2247 m u_{ll} \cos\psi \tag{4.49}$$

where u_{ll} is line-to-line voltage, ψ is the phase angle.

Assuming k is the voltage conversion ratio of the primary side and secondary side, as presented in (4.50).

$$k = \frac{N u_{dc}}{1.2247 u_{ll} \cos\psi} \tag{4.50}$$

In (4.49), the average voltage of the primary side is always smaller than $1.2247 u_{ll}\cos\psi$. Therefore, to ensure the voltages between the two sides can be matched, Nu_{dc} should be smaller than $1.22 u_{ll}\cos\psi$, in other words, k<1. Therefore, the calculation of the phase shift angle can be rewritten as (4.51).

$$\varphi = \begin{cases} ar\cos\left(\dfrac{k}{\sin(0.5m\pi)}\right); & \dfrac{k}{\sin(0.5m\pi)} < 1 \\ 0; & \dfrac{k}{\sin(0.5m\pi)} \geq 1 \end{cases} \tag{4.51}$$

4.3.1 Comparative Analysis of Current Stress

To simplify the control complexity, the fundamental components (the switching frequency component) of the peak current square and transferred power are used to reduce current stress with negligible error. However, to verify the performance of the coordinate control, this section compares the actual peak current (not only contains the fundamental component but also contains the numerous order harmonics). The current characteristics of different combination parameters are compared. In the first combination parameters, the modulation index is 0.866, while the phase shift angle is changed from 0° to 90°, defined as Method I. In Method II,

the phase shift angle is 90°, and the modulation index is controllable. In Method III, the improved parameter combination is applied. Figure 4.9 shows the relation curves of the normalized current stress to the normalized transferred power of three methods.

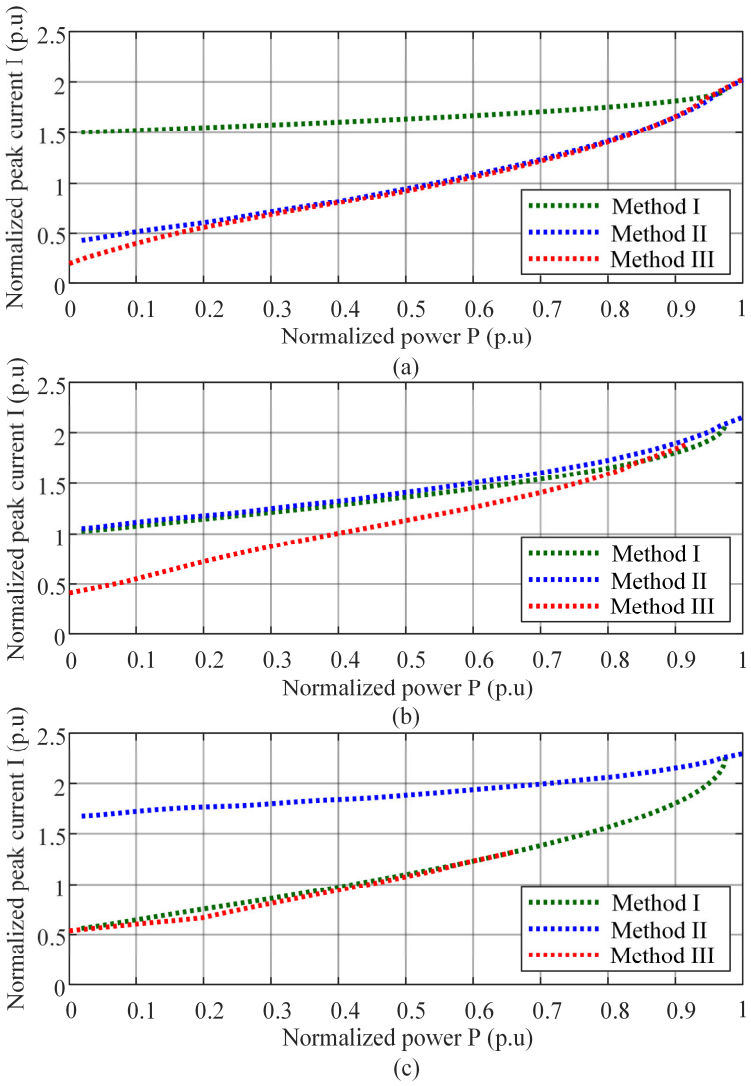


Figure 4.9 Relation curves of normalized peak current and normalized transferred power under different voltage conversion ratio (a) k=0.2 (b) k=0.5 (c) k=0.8

Figure 4.9(a) illustrates the normalized peak current varied with the normalized transferred power under the voltage conversion ratio is 0.2. When the voltage conversion ratio is changed to 0.5, the relationship between normalized peak current and normalized transferred the power of three methods are presented

in Figure 4.9(b). It shows that the current difference between the proposed method and the conventional methods decreases as the power increase. Moreover, Figure 4.9(c) presents the relation curves of normalized peak current to normalized transferred power when the voltage conversion ratio is 0.8.

Through observing these figures, we can see that the normalized peak current is increased with the increase of the transferred power. The normalized peak current of Method I decrease with the increase of the voltage conversion ratio, the larger the conversion ratio, the lower the current stress. However, as the conversion ratio increases, the normalized peak current is increasing in Method II. The lower the voltage conversion ratio is, the better the performance can be. When the voltage ratio is higher than 0.5, Method I and Method III have lower current stress than Method II. Besides, Method I achieve the highest current stress among the three methods once the voltage conversion ratio is smaller than 0.5. The comparison among the three methods indicates that Method III has the lowest current stress under the same normalized transferred power at any voltage conversion ratio. Moreover, the peak current is reduced significantly at light load conditions.

From the above analysis, the improved parameter combination can reduce current stress in an isolated AC-DC matrix converter. To realize the coordination control of the modulation index and phase shift angle in the converter, the control strategy implementation is proposed in Figure 4.10.

The inner current loop is in the *dq* frame, two PI controllers are applied in the *dq* axis to control i_d and i_q. The control outputs are transformed back to the *abc* frame and supplied for the SVM modulator. Then the phase shift angle is regulated by a slow loop which is the integration links with a large time constant. The dynamic response of the phase shift angle is slower than the modulation index. Hence, the phase shift angle is considered as constant when the modulation index is regulated by PI controllers. There are three control modes for isolated AC-DC matrix converter, power control mode, AC voltage control mode, and DC voltage control mode. In the power control mode, the current references are calculated based on power reference, and the AC voltage and DC voltage are constant values. In AC voltage control mode, the AC voltage is controlled by the PI controller and

the output is feed to the current reference. At the same time, the line-to-line voltage in (4.50) is the AC voltage reference. Similarly, the DC voltage is controlled by a PI controller and the output is i_d reference in DC voltage control mode and the DC voltage reference is used to calculate (4.50).

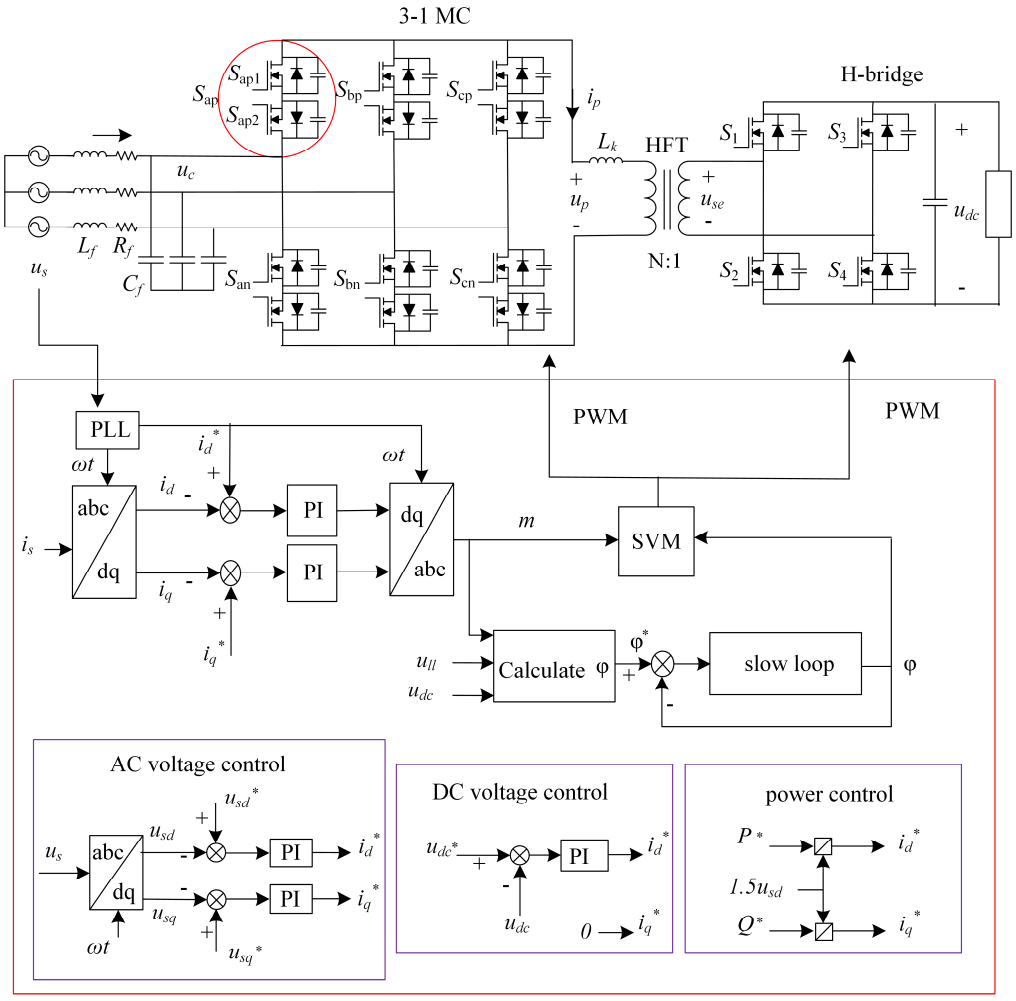


Figure 4.10 Implementation of optimal control variables for isolated AC-DC matrix converter

4.4 Experimental Verification

4.4.1 SVM Strategy Verification

To validate the proposed SVM strategy, the isolated AC-DC matrix converter prototype is built for experimental verification. The SiC MOSFETs are used to build bidirectional switches. Texas Instruments DSP TMS320F28379 and the

Xilinx FPGA XC3S500E platform are used to implement the proposed method. The prototype is given in Figure 4.11. The three cases (conventional SVM strategy, the proposed SVM strategy with improving the switching sequence, and the proposed SVM strategy with improving the switching sequence and zero vectors) are conducted to verify the performance. The model parameters are given in Table 4.4. The DC side is connected to a 48V DC source, while the AC side is connected to a three-phase resistor load (28.6 Ω).

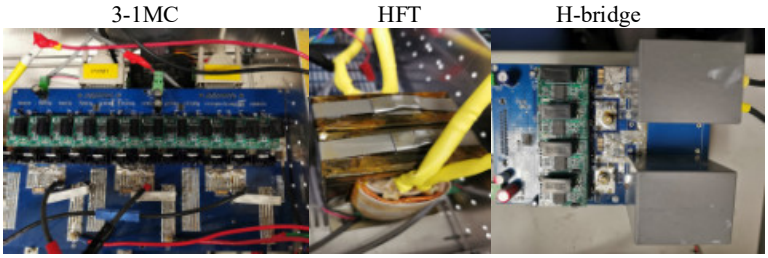


Figure 4.11 The experimental setup of isolated AC-DC matrix converter

Table 4.4 Model Parameters

Parameter	Value
Filter inductor L_f	0.3mH
Filter capacitor C_f	20uF
Turns ratio N	1
Leakage inductor L_k	80uH
Switching frequency f_s	20kHz
DC capacitor	200uF

Figure 4.12 shows the results of three cases when m=0.5, φ=-50°. The waveforms are line-to-line voltage, phase current, primary voltage, secondary voltage, and primary current of HFT respectively (from upper to lower). To observe the high-frequency waveforms, the primary voltage, secondary voltage, and primary current are zoomed in (d)(c)(e), respectively. It shows that the AC current of Case2 and Case3 are of high quality while distortions can be observed from Case1. To compare them directly, the corresponding FFT analysis is given in Figure 4.13. The phase current THD of three cases is 11.39%, 3.91%, and 3.87%. Compared with Case1, 5^{th}, 7^{th} order harmonics, and THD are reduced in Case2 and Case3. This indicates that only changing the switching sequence can improve the current quality.

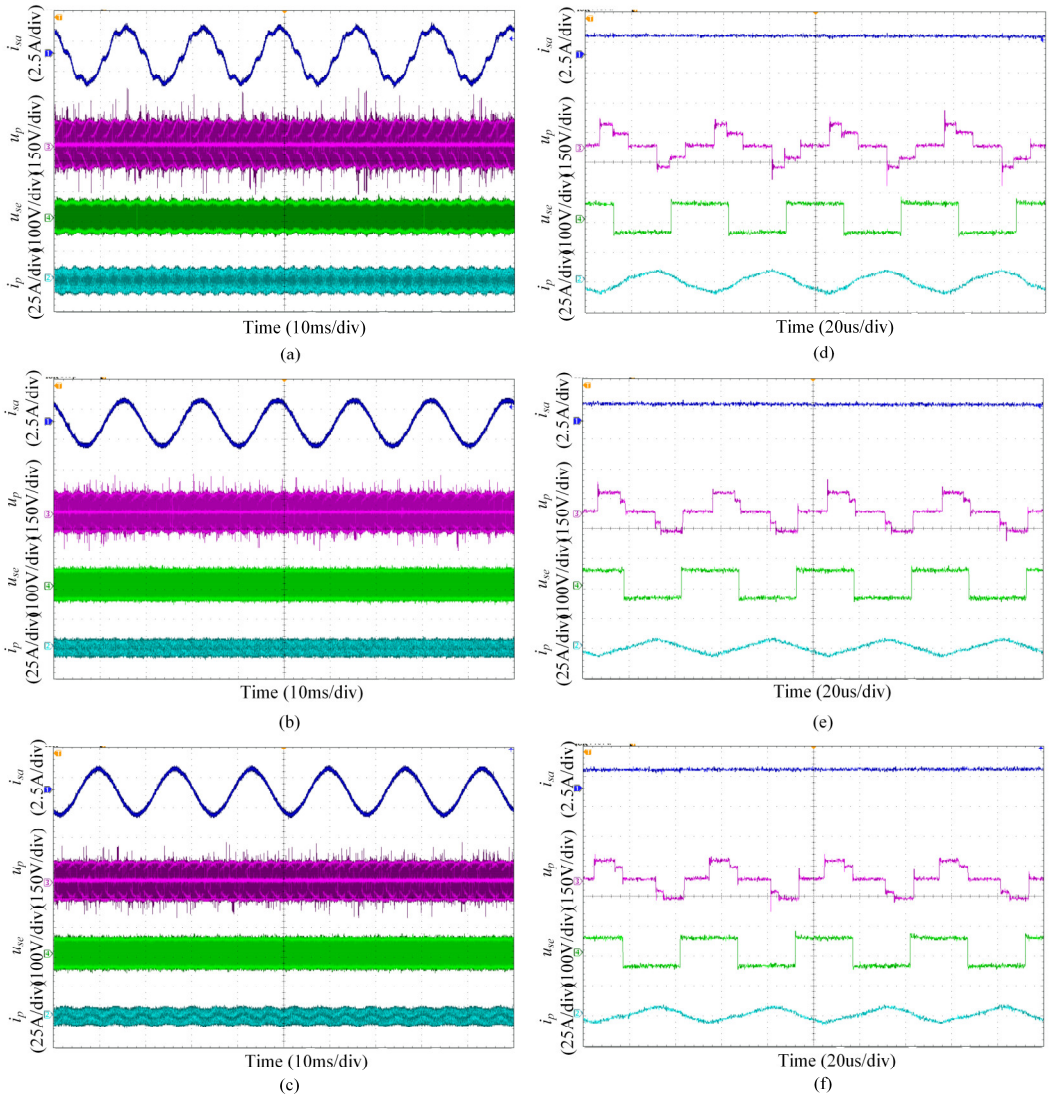


Figure 4.12 Experimental results of three cases, phase current, primary voltage, secondary voltage and primary current when m=0.5, φ=-50° (a) Case1 (b) Case2 (c) Case3 (d) zoom in of Case1 (e) zoom in of Case2 (f) zoom in of Case3

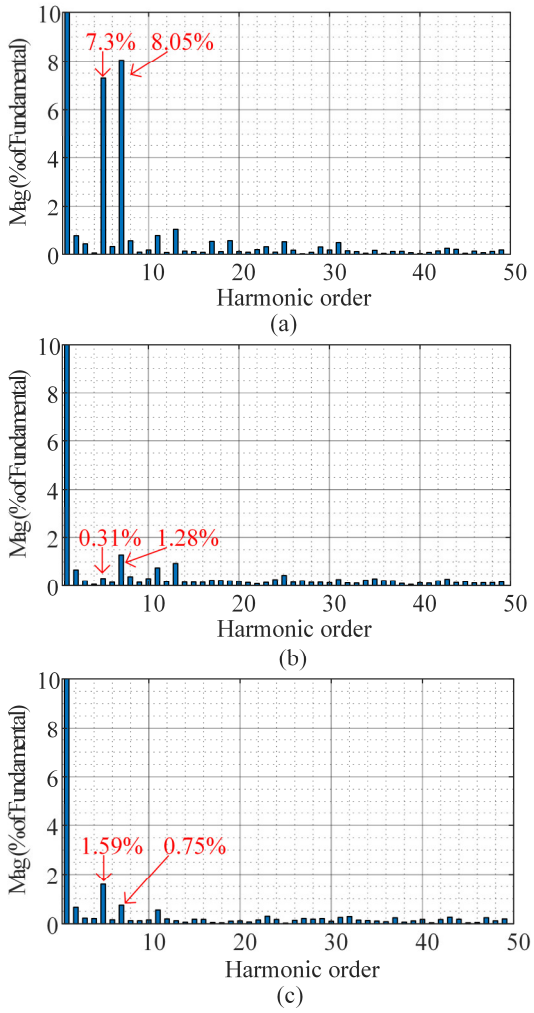


Figure 4.13 The phase current FFT analysis of three cases when m=0.5, φ=-50° (a) Case1 (b) Case2 (c) Case3

When the modulation index is 0.8 and the phase shift angle is -90°, the experimental results of the three cases are given in Figure 4.14. It can be observed that the current is distorted in Case1 and Case2. The corresponding FFT analysis is presented in Figure 4.15.

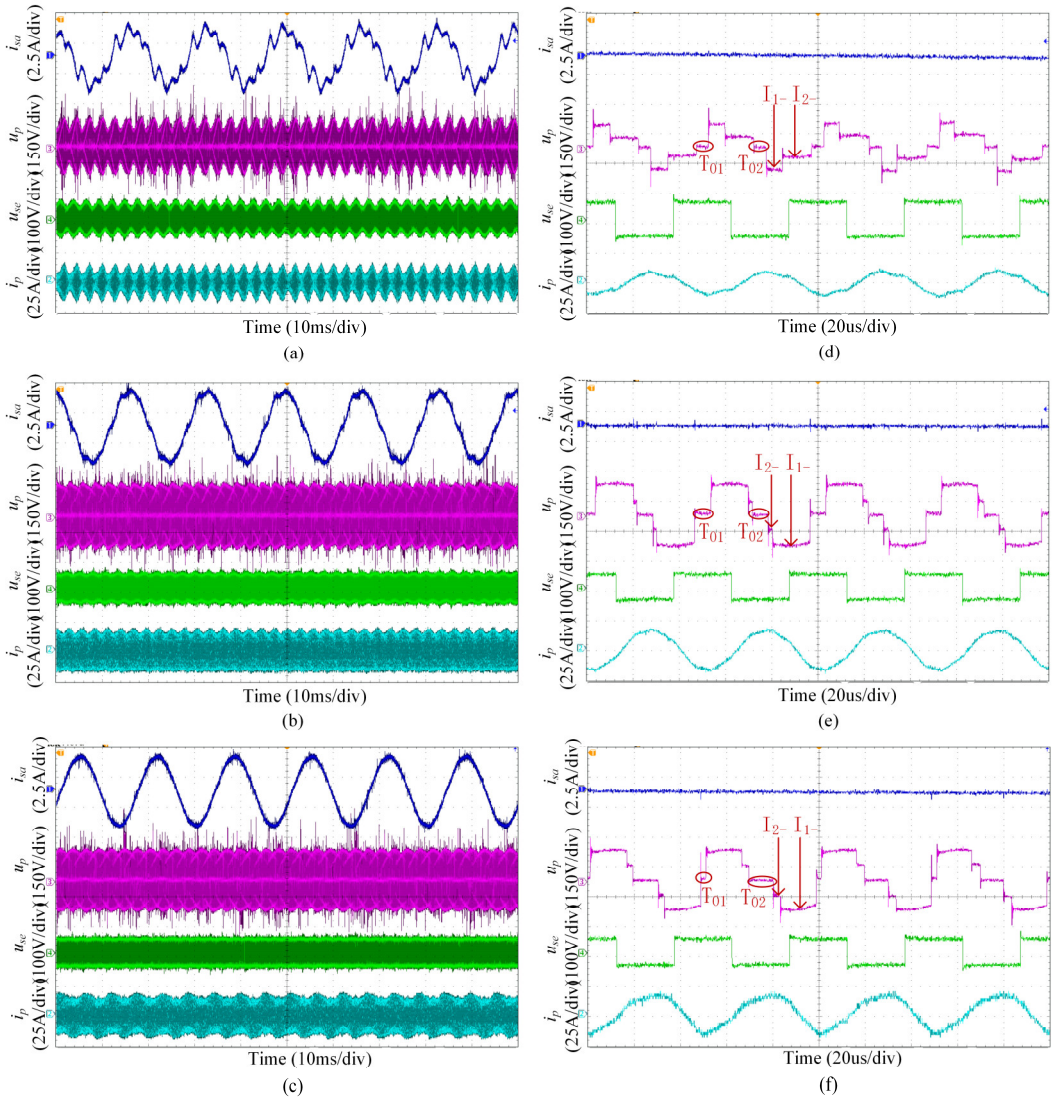


Figure 4.14 Experimental results of three cases, phase current, primary voltage, secondary voltage and primary current when m=0.8, φ=-90° (a) Case1 (b) Case2 (c) Case3 (d) zoom in of Case1 (e) zoom in of Case2 (f) zoom in of Case3

The phase current THD in Case2 is lower than Case1; however, the THD and 5th order harmonic still fail to meet the requirements in Table 4.3. Besides the new sequence in Case 2, the zero vectors are redistributed in Case 3. As a result, the THD is further reduced in Case 3. Meanwhile, both the 5th and 7th order harmonics are lower than 4%. The current quality can meet the IEEE 519 in this case.

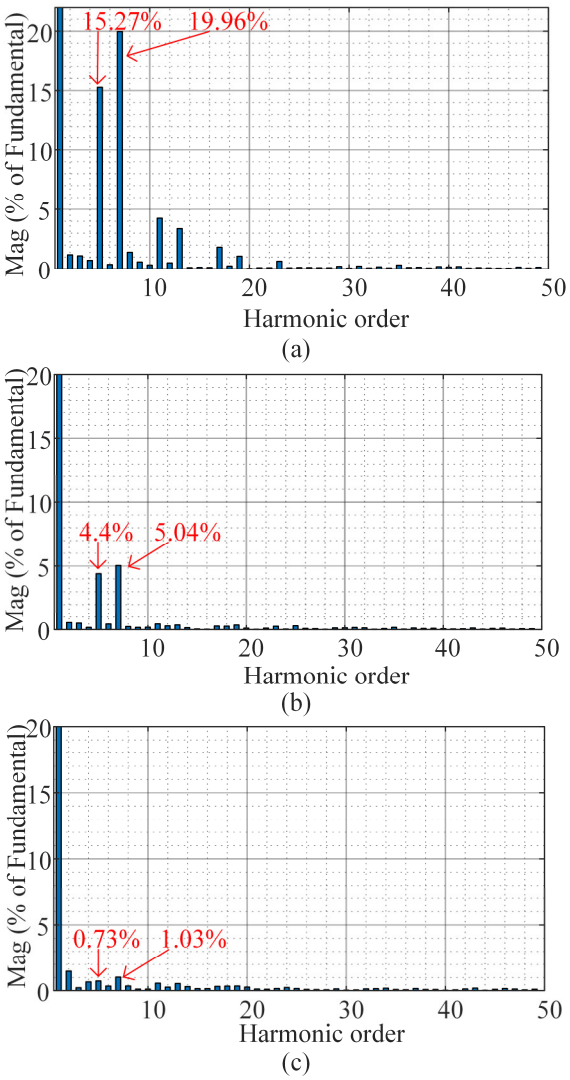


Figure 4.15 The phase current FFT analysis of three cases when m=0.8, φ=-90° (a) Case1 (b) Case2 (c) Case3

The differences in sequence and zero vector distribution, which leads to the differences in power quality. To observe the PWM sequence and distribution time in detail, the high frequency waveforms are provided in Figure 4.14. From upper to lower, the waveforms are primary voltage, secondary voltage, primary current, and secondary current within four switching cycles. Due to the different switching sequence, the primary voltage waveforms in Figure 4.14(d) and Figure 4.14(e) are different, where the two negative voltages are swapped. But the zero vectors' duty cycles are still equal (T_{01}=T_{02}). After redistributing the zero vectors in Case 3, the duty cycles of zero vectors are now different ($T_{01}\neq T_{02}$), as shown in Figure 4.14(f).

The different primary voltage waveforms can lead to different primary current and then affect the AC current quality.

4.4.2 Current Stress Reduction Verification

To validate the proposed control variables combination, three different control variables are defined as Method I, Method II, and Method III, and their performance is compared under the same conditions. The model parameters are the same as Table 4.4, and the WT5000 Yokogawa precision power analyzer is used to measure power efficiency. The experimental part includes two aspects, the first part compares the performance of three methods under the same voltage ratio. While the second part presents the comparison of three methods with different voltage ratio.

(1) Performance Comparison under Varying Load with Same Constant Voltage Ratio

The DC voltage is supported by a 48V DC source, and the AC side is connected to a three-phase AC load. Two different loads are conducted (28.6 Ω and 57.2Ω) to achieve a 0.5 voltage ratio. The experimental results of three different methods are presented in Figure 4.16 when the load is 28.6 Ω. Where i_a is phase current, u_p is primary voltage, u_{se} is secondary voltage and i_p represents primary current. The envelope of the primary voltage is line-to-line voltage, and the secondary voltage is constructed by positive and negative DC voltage. It shows that the amplitude of primary voltage (same loads, same voltage ratio) in three methods are almost the same but the peak-to-peak values of primary current are different. The peak value of the primary current of Method I and Method II are similar, while the proposed Method III has the lowest peak-peak primary current value, therefore, the current stress is reduced. To observe the primary current clearly, the high frequency waveforms are zoomed in, as Figure 4.16(d)-(f). With different modulation index and phase shift angle combinations in three methods, the primary voltage and primary currents are different. Table 4.5 lists the parameters combination, peak current, efficiency, and THD of phase current in three methods.

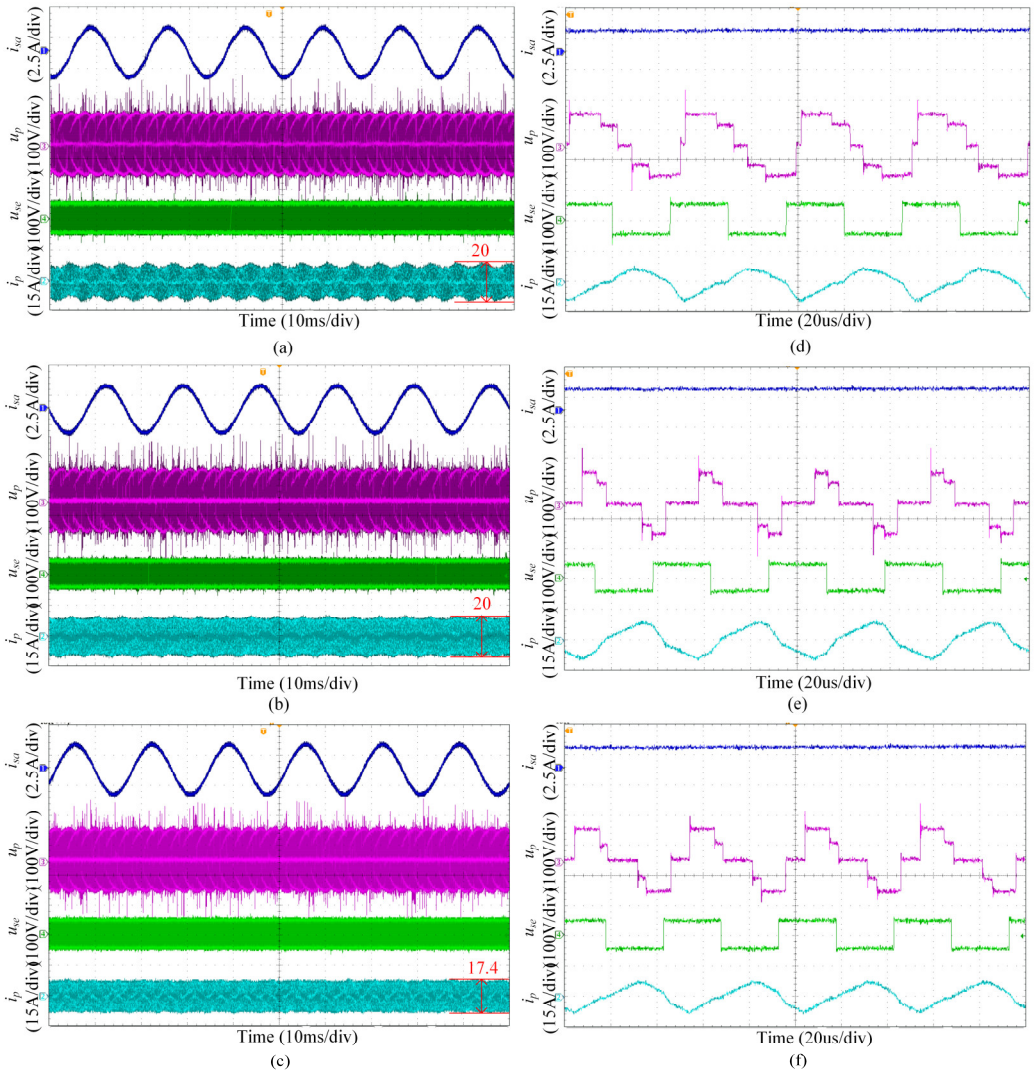


Figure 4.16 Phase current, primary voltage, secondary voltage, and primary current waveforms when k=0.5, R=28.6Ω (a) Method I (b) Method II (c) Method III (d) zoom in waveforms of Method I (e) zoom in waveforms of Method II (f) zoom in waveforms of Method III

Table 4.5 Parameters of Three Methods When k=0.5, R=28.6Ω

	m	φ(°)	i_{p_peak} (A)	η(%)	THD (%)
Method I	0.866	40	10	90.9	3.17
Method II	0.416	90	10	87.74	2.4
Method III	0.6	52	8.7	91.2	2.36

Table 4.5 shows that with the improved control combination, the proposed Method III achieves the minimum current stress, and the power efficiency is improved correspondingly. To compare the performance of three methods in

different loads and the same voltage conversion ratio, Figure 4.17 shows the experimental results when the AC load is 57.2Ω. Three different methods can achieve the same amplitudes of phase current, but the peak values of primary current are different.

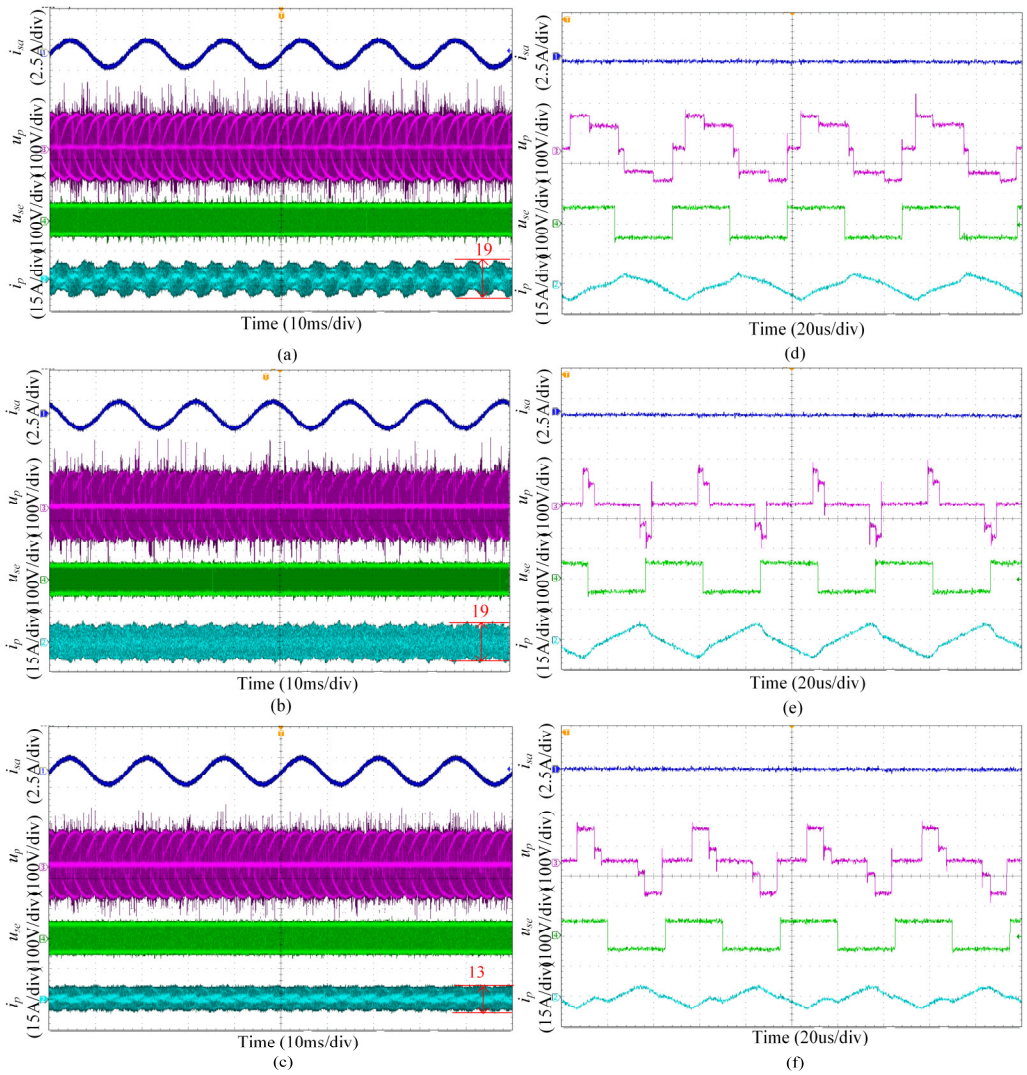


Figure 4.17 Phase current, primary voltage, secondary voltage, and primary current waveforms when k=0.5, R=57.2Ω (a) Method I (b) Method II (c) Method III (d) zoom in waveforms of Method I (e) zoom in waveforms of Method II (f) zoom in waveforms of Method III

Under the same condition, Method III achieves the lowest current stress, while Method I and Method II have the same current stress. Since the modulation index is different in the three methods, the primary voltage waveforms are different. Also, the phase shift angle is different to transfer the same power. The control variables

combinations, current stress, efficiency, and THD are listed in Table 4.6. The current stress in Method I and Method II are the same, and Method I have higher efficiency than Method II. Moreover, it shows that the proposed Method III has the lowest current stress and highest power efficiency.

Table 4.6 Parameters of Three Methods When k=0.5, R=57.2Ω

	m	φ(°)	ip_peak (A)	η(%)	THD (%)
Method I	0.866	22	9.5	88.9	3.22
Method II	0.186	90	9.5	86	3.13
Method III	0.426	36	6.5	92.4	2.56

From the above analysis, it can be concluded that Method I and Method II can achieve similar current stress under different load conditions when the voltage ratio is 0.5. However, the proposed Method III reduces the current stress significantly, especially in a light load condition. The conclusions are coordinate with the analysis. Moreover, the proposed Method III has the highest power efficiency among the three methods due to the power loss is reduced with decreased current stress.

(2) Performance Comparison under Varying Voltage Ratio with the Same Load

To validate the proposed Method III and demonstrate its advantage over the other two methods under different voltage ratio, three methods are implemented respectively for the same load condition (57.2Ω). Figure 4.18 shows the experimental results when the voltage ratio is 0.3. The envelope of the primary voltage is line-to-line voltage, and the secondary voltage is constructed by positive and negative DC voltage. It shows that the DC voltage is still 48V, while the amplitude of the line-to-line voltage is higher than that in Figure 4.17 due to the voltage ratio is reduced from 0.5 to 0.3. Also, it shows that the amplitudes of phase current in the three methods are almost the same, but the peak-to-peak values of the primary current are different.

Method I have the highest current stress, the peak value of the primary current is 17.85A, followed by Method II. While the proposed Method III has the lowest current stress, the peak value of the primary current is 11.5A. The zoomed-in high-

frequency waveforms are shown in Figure 4.18(d)-(f), it can be observed that the control variable combinations are different in three methods.

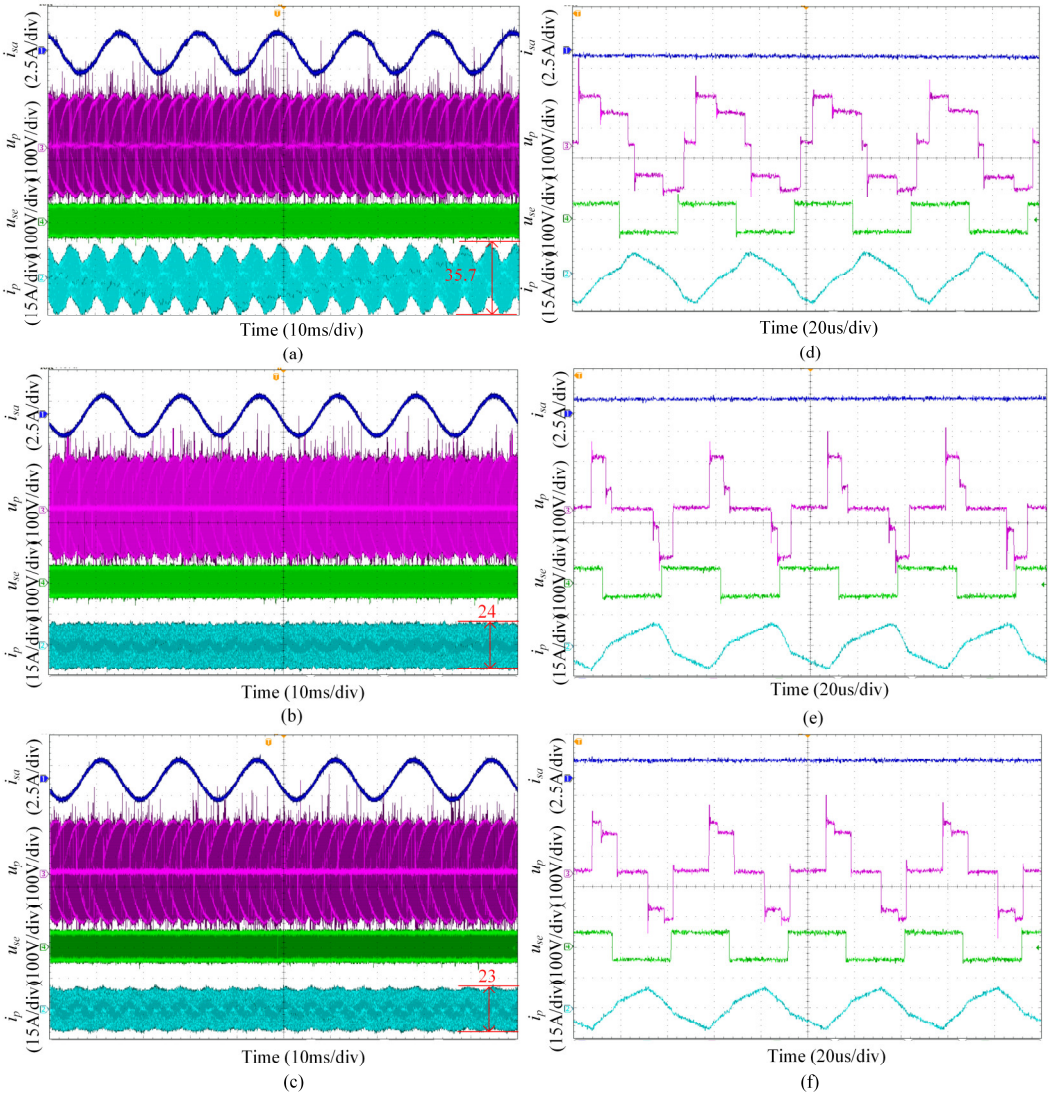


Figure 4.18 Phase current, primary voltage, secondary voltage, and primary current waveforms when k=0.3, R=57.2Ω (a) Method I (b) Method II (c) Method III (d) zoom in waveforms of Method I (e) zoom in waveforms of Method II (f) zoom in waveforms of Method III

Figure 4.19 gives the experimental results of three methods when the voltage ratio is 0.6, including the phase current primary voltage, secondary voltage, and primary current waveforms. Since the voltage ratio is increased to 0.6, the line-to-line voltage is decreased. Under this condition, the current stress in Method II is higher than that in Method I, which is different from Figure 4.18. However, the

proposed Method III achieves the lowest current stress among them, the peak current is 5.375A.

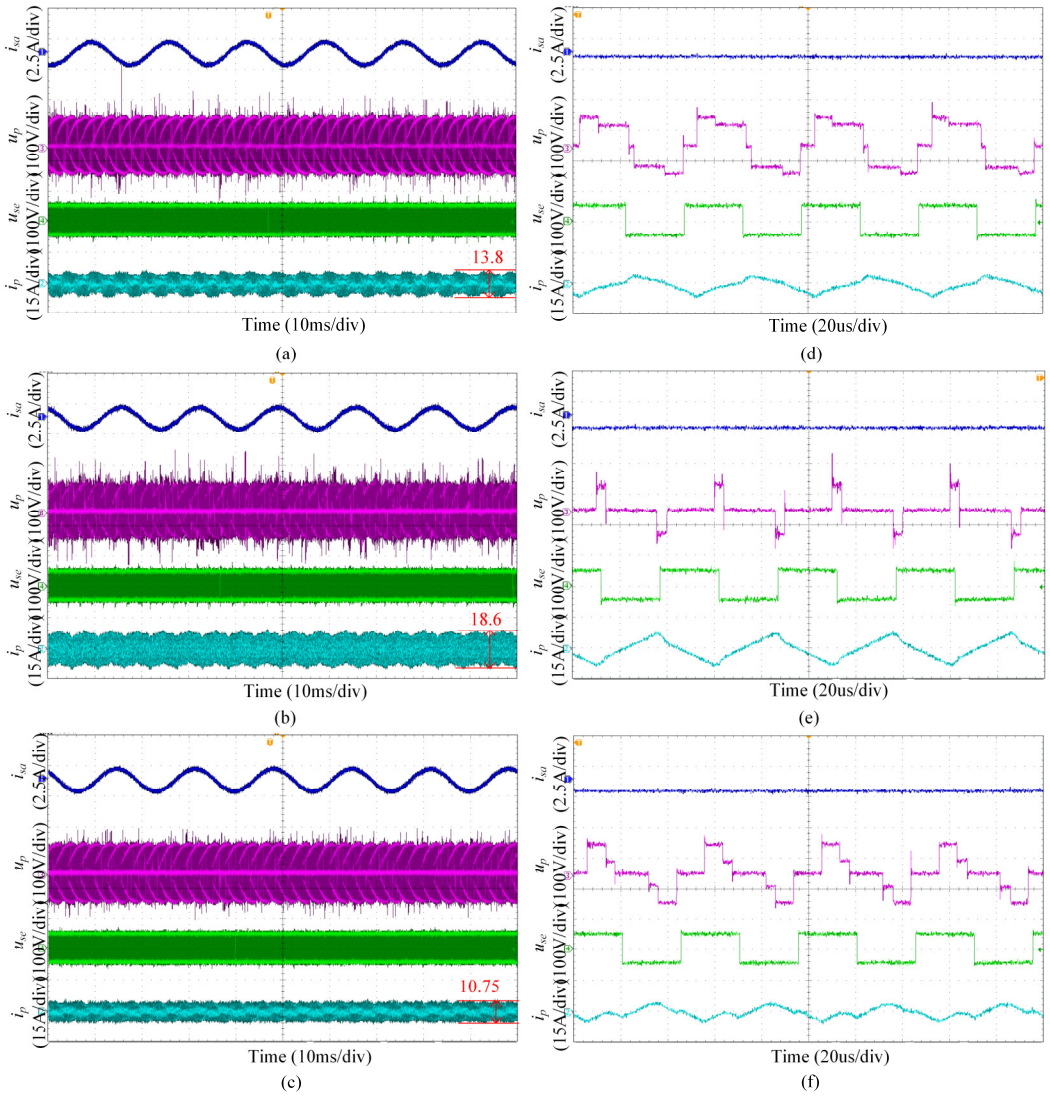


Figure 4.19 Phase current, primary voltage, secondary voltage, and primary current waveforms when k=0.6, R=57.2Ω (a) Method I (b) Method II (c) Method III (d) zoom in waveforms of Method I (e) zoom in waveforms of Method II (f) zoom in waveforms of Method III

To observe the performance of three methods under different voltage ratio, the peak value of the primary current is given in Figure 4.20. With the increase of voltage ratio, the peak currents of the three methods are decreased. When the voltage ratio is smaller than 0.5, Method I has the highest current stress, followed by Method II. As the voltage ratio increase to 0.5, the current stress of Method I

and Method II are similar. When the voltage ratio greater than 0.5, the current stress in method II is higher than that in Method I. However, the proposed Method III achieves the lowest current stress at any voltage ratio, which agrees with the theoretical analysis. The measured power efficiency and THD of the three methods are presented in Figure 4.21 and Figure 4.22 respectively. It can be observed that the proposed Method III can improve power efficiency without decreasing AC current quality.

To sum up, the proposed coordination control of the modulation index and phase shift angle method achieves the lowest current stress under different loads, especially in light load conditions. Moreover, compared with the other two methods, the proposed method reduces the current stress under different voltage ratios. The above experimental results are coordinate with the theoretical analysis.

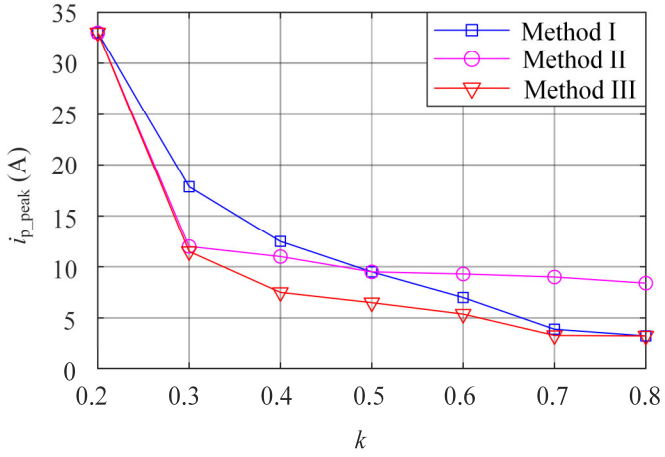


Figure 4.20 Measured peak current of three methods varied with voltage ratio

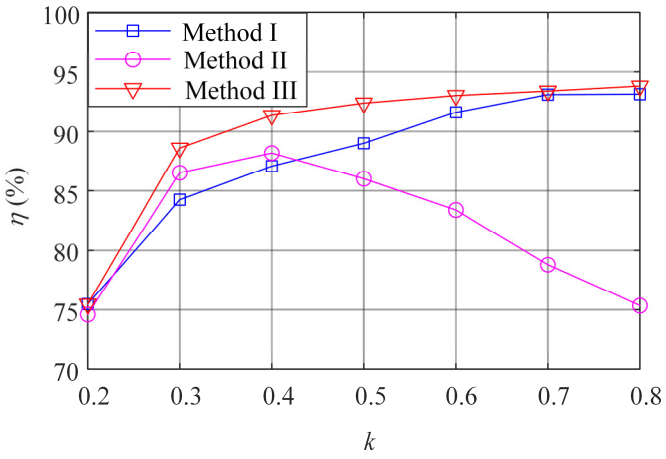


Figure 4.21 Measured power efficiency of three methods varied with voltage ratio

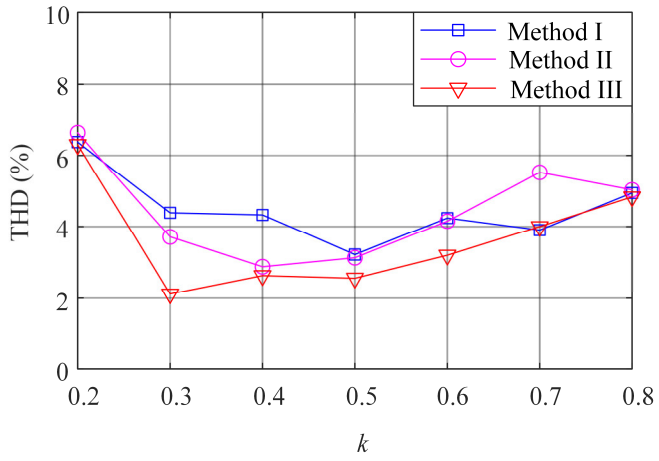


Figure 4.22 Phase current THD of three methods varied with voltage ratio

4.5 Summary

With the development of fast switching devices, the commutation duty ratio can be reduced, and the effect on the current quality is reduced. Under this condition, the 9-segment SVM in Chapter 3 cannot ensure the best performance. In this chapter, an SVM strategy with a low number of switching actions is proposed. Moreover, this method reduces the low order harmonics by improving both the switching sequence and zero vector distribution.

Based on the proposed modulation method, two control variables are optimized to reduced current stress. This chapter calculates the transferred power and peak value of the primary current by establishing the mathematical model based

on the Fourier series. Then, using the Lagrange multiplier method to optimize two control variables to reduce current stress. With the proposed control variables combination, the current stress is reduced, and the converter efficiency is improved especially at the light load condition.

Chapter 5

Modular Modulation Strategy for Parallel Unidirectional Isolated AC-DC Matrix Converters

Due to the galvanic isolation, the isolated AC-DC matrix converters are easy to parallel as circulating current can be avoided. The isolated AC-DC matrix converters can be operated in input-parallel-output-parallel (IPOP) to increase power rating or operated in input-parallel-output-series (IPOS) to increase voltage level. However, the modular structure and corresponding modular modulation strategy have not been researched. For modular isolated AC-DC converters, the SPWM strategy is preferable because it has good scalability compared to the multilevel SVM strategy. By interleaving the carriers, advanced performance can be achieved. Taking the unidirectional isolated AC-DC matrix converter as an example, this chapter proposes an interleaved SPWM strategy for the parallel structure to reduce DC current ripple.

In parallel unidirectional isolated AC-DC matrix converter topology, the DC current ripple, particularly the high frequency ripple, is a concern to be addressed. Applying a large filter inductor to reduce the ripple can lead to higher cost, volume, and weight. Fortunately, the DC current ripple can be mitigated by interleaving multiple unidirectional isolated AC-DC matrix converters. However, the PWM design can be challenging: firstly, the PWM pattern must be asymmetry to realize interleaving for even number of converters in parallel while ensure good current quality; secondly, the necessary changing primary current direction for converter can lead to duty cycle loss, degrading the current quality; thirdly, the widely used

---

Publication out of this chapter:

F. Fang, Y. Li and Y. Li, "A New Modular SPWM Strategy for Parallel Isolated Matrix Rectifiers to Improve Current Quality," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 1577-1582.

SVM is not straightforward for modular design. In this chapter, a new SPWM strategy is proposed to obtain all the benefits from the interleaving of unidirectional isolated AC-DC matrix converters. The PWM pattern is carefully designed and duty cycle loss is compensated. As a carrier-based modulation method, it has good scalability for paralleled converters. Simulation and experimental results are provided to validate the feasibility and performance of the interleaved SPWM.

5.1 Topology and Conventional Modulation Strategies for Unidirectional Isolated Matrix Converter

Figure 5.1(a) shows the topology of a unidirectional isolated AC-DC matrix converter, which contains a 3-1 MC, an HFT, and a diode bridge. The 3-1 MC converts three-phase AC voltage to a high frequency voltage at the primary side of HFT. While the diode bridge converts the secondary side voltage of HFT to a DC voltage. Then, the output side is connected to the filter inductor to smooth DC current and reduce phase current THD in the AC side [102-103]. The adoption of an HFT can provide galvanic isolation and avoid circulating current in parallel systems. Therefore, it is easy to achieve modular design when multiple unidirectional isolated AC-DC matrix converters are used.

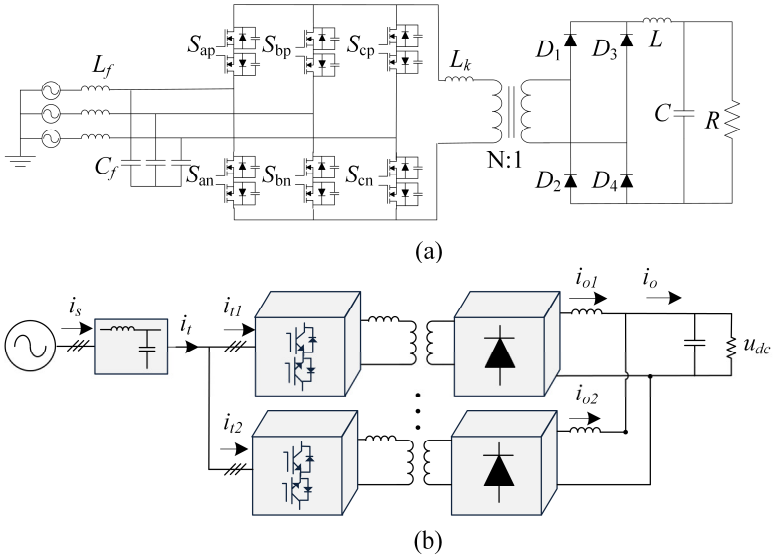


Figure 5.1 (a) the topology of unidirectional isolated AC-DC matrix converter (b) parallel structure

The switching vectors of 3-1 MC are the same as the isolated AC-DC matrix converter. Also, the current reference can be synthesized by two adjacent active vectors and one zero vector. Assuming the current reference in sector I, I_1, I_2, and I_0 (I_7) will be used. The dwell time of each vector can be calculated by (5.1).

$$\begin{aligned} T_1 &= mT_s \sin(\frac{\pi}{6} - \theta) \\ T_2 &= mT_s \sin(\frac{\pi}{6} + \theta) \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{5.1}$$

where m is the modulation index, θ is the current reference angle, $\theta \in [-\pi/6, \pi/6)$.

Based on the active vectors and zero vector, different switching patterns can be formed, the widely researched switching patterns are six-segment and eight-segment strategies. The switching sequence and primary voltage of the two strategies are given in Figure 5.2. Compared with the eight-segment SVM strategy, the six-segment SVM strategy has a lower DC current ripple and smaller duty cycle loss [69].

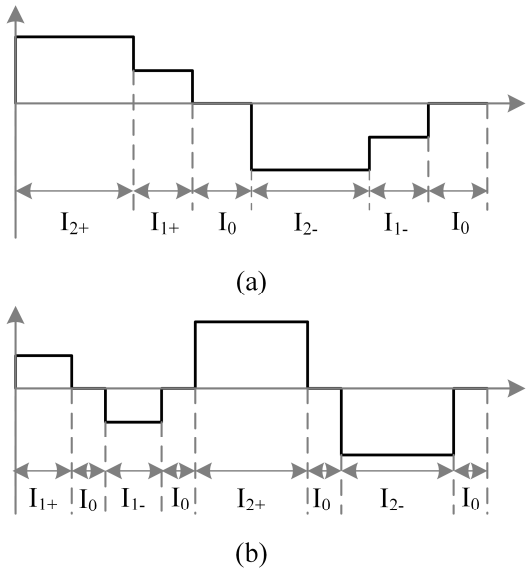


Figure 5.2 Primary voltage waveforms of different SVM strategies (a) six-segment SVM strategy (b) eight-segment SVM strategy

To increase power capacity and better utilize the modular feature of this converter, multiple unidirectional isolated matrix converters can be paralleled and interleaved to improve current quality, as shown in Figure 5.1(b). The interleaved

strategy is already well proved in VSC and CSC [104-107]. However, due to the unique operation principle of this converter, the interleaved PWM patterns for VSC and CSC are not applicable for this topology. In this converter, the 3-1 MC shall convert line frequency AC to a high frequency AC. As a result, even PWM for a single unidirectional isolated AC-DC matrix converter needs to be different from the other topologies.

Furthermore, the above mentioned SVM methods for a single unidirectional isolated AC-DC matrix converter are not always applicable to the interleaving operation of parallel converters. Firstly, the PWM should ensure the current quality and avoid significant AC distortion as the low order harmonics caused by each converter can superposition when they are paralleled. The low order harmonics not only harm the other connected devices but also endanger the safe operation of this converter. Besides, the unidirectional isolated AC-DC matrix converter utilizes bidirectional switches and multi-step commutation must be performed to ensure the freewheeling of inductive current. The pulse should be larger than the commutation time to ensure safe commutation, distortions will be caused by improper PWM design. Secondly, the PWM pattern cannot be symmetrical in one PWM cycle, as a symmetrical pattern can lead to the same sequence when two converters are paralleled, losing the benefits of the interleaved operation. Besides, the primary current of HFT requires a finite time to change the current direction, the duty cycle loss is caused and degraded current quality.

Up till now, the modular structure of unidirectional isolated AC-DC converter has not been researched. To fill this gap, this chapter focuses on the design of interleaved PWM for such a system. The PWM pattern is carefully designed to ensure low AC distortion and with an asymmetrical pattern to obtain benefits of interleaving under an arbitrary number of paralleled converters. Considering the modularity of paralleled unidirectional isolated AC-DC matrix converters, this chapter also targets a modular PWM design, which leads to a carrier-based PWM implementation. Besides, the duty cycle loss is compensated to improve the performance of the paralleled converters.

5.2 Modular Structure and Proposed SPWM

The modular structure is given in Figure 5.3. The converters are fed by a common AC voltage after a common CL filter, while the DC sides are connected to load after their filter inductor, respectively. The input current of each converter and total input current are i_{t1}, i_{t2} and i_t respectively. While the output current of each converter and total output current is i_{o1}, i_{o2}, and i_o.

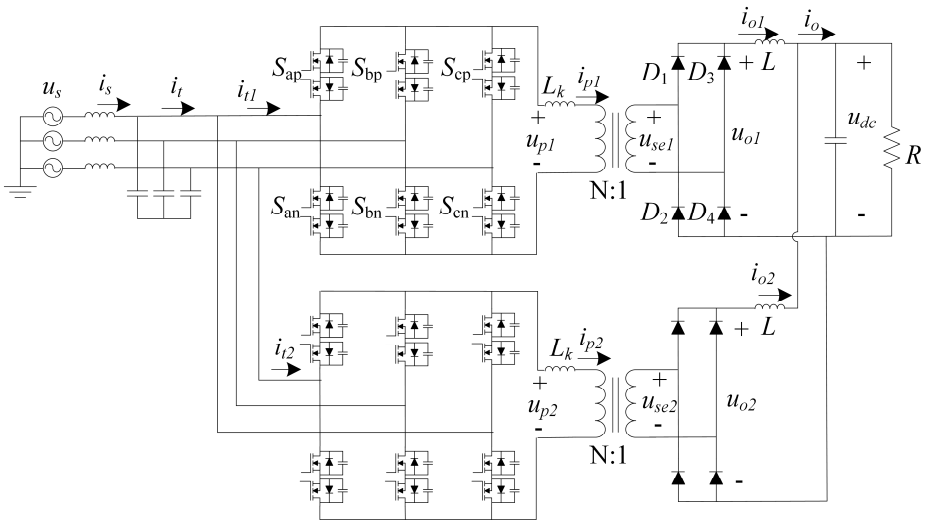


Figure 5.3 Modular structure of unidirectional isolated AC-DC matrix converters

The proposed carrier-based modulation strategy for unidirectional isolated matrix converters is given in Figure 5.4.

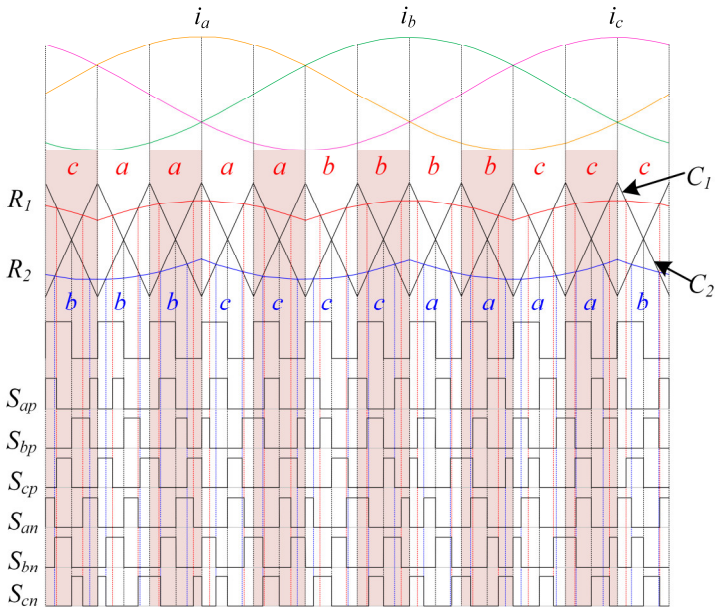


Figure 5.4 The gating signals generation of the proposed SPWM strategy

By comparing the three-phase current references, the maximum current i_{max} and minimum current i_{min} can be selected, defined as R_1 and R_2. The corresponding phase is defined as Max, Min, and the third phase is defined as Med. Two triangular waveforms are used as carriers, each carrier amplitude is equal to one, while C_1 ranges [0, 1] and C_2 ranges [-1, 0]. Due to the 3-1 MC is connected to HFT, the gating signals should produce a positive and negative voltage in each switching cycle. Therefore, the carriers can be divided into two parts, the first half cycle is named a positive half cycle and the second half cycle is named the negative half cycle. After that, the references are compared with two high frequency triangle waveforms to obtain the gating signals for bidirectional switches.

When R_1 is larger than C_1, the switch in the Max phase is turned on; otherwise, the switch in Med phase is turned on. In a positive half cycle, the gating signals are for the upper-arms and lower-arms in a negative half-cycle. When R_2 is smaller than C_2, the switch in the Min phase is turned on; otherwise, the switch in Med phase is turned on. In a positive half cycle, the gating signals are for lower-arms and upper-arms in the negative half cycle. The gating signals are generated based on the principles, as shown in Table 5.1.

Table 5.1 Gating Signals for Each Switch

	Positive Half Cycle	Negative Half Cycle
Upper arm	$R_{1p}>C_1$ $S_{Maxp}=1$	$R_{2n}>C_2$ $S_{Medp}=1$
	$R_{1p}\leq C_1$ $S_{Medp}=1$	$R_{2n}\leq C_2$ $S_{Minp}=1$
Lower arm	$R_{2p}>C_2$ $S_{Medn}=1$	$R_{1n}>C_1$ $S_{Maxn}=1$
	$R_{2p}\leq C_2$ $S_{Minn}=1$	$R_{1n}\leq C_1$ $S_{Medn}=1$

Note: R_{1p} and R_{2p} present the maximum and minimum current in the positive half cycle, R_{1n} and R_{2n} present the maximum and minimum current in the negative half cycle. S_{xp} presents the switch of phase x in the upper arm, S_{xn} presents the switch of phase x in the lower arm. $x\in\{a,b,c\}$.

To illustrate the SPWM in detail, Figure 5.5 shows an example when $i_a>i_c>i_b$. The Max phase is phase *a*, the Med phase is phase *c*, and the Min phase is phase *b*. In a positive half cycle when i_a is larger than C_1, S_{ap} is turned on, otherwise, S_{cp} is turned on. When i_b is larger than C_2, $S_{cn}=1$, else $S_{bn}=1$. In a negative half cycle, when i_a is larger than C_1, S_{an} is turned on; otherwise, S_{cn} is turned on. When i_b is larger than C_2, $S_{cp}=1$, else $S_{bp}=1$. Figure 5.5 shows that the primary voltage in

positive and negative half cycles are centrosymmetric and the voltage-second can be achieved.

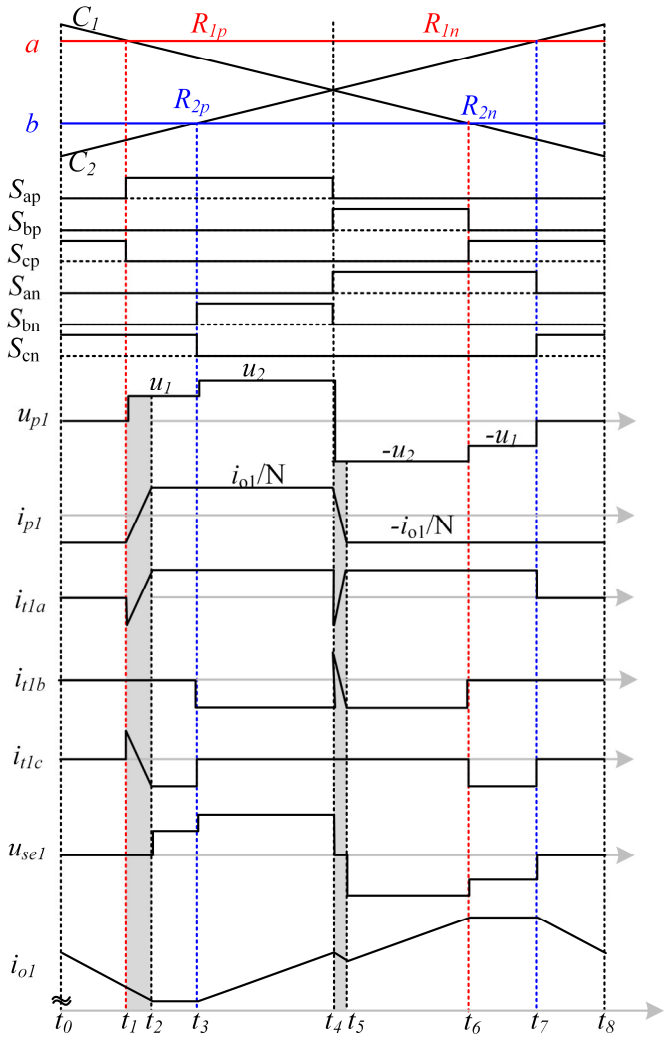


Figure 5.5 Comparison results when $i_a>i_c>i_b$ ($|i_a|>|i_b|$), current references, carriers, gating signals, primary voltage, primary current, i_{ta}, i_{tb}, i_{tc}, secondary voltage, and DC current waveforms (from upper to lower)

According to relative current reference magnitudes, there are twelve sectors in each fundamental frequency. The Max, Min current reference, and the corresponding primary voltages are presented in Table 5.2.

Figure 5.5 shows that the primary voltage has six switching states, and the corresponding duty ratios are given as follows.

$$d_1 = \frac{1}{2}\left(1 - R_{1p}\right); d_2 = \frac{1}{2}\left(R_{1p} + R_{2p}\right); d_3 = -\frac{1}{2}R_{2p}$$
$$d_4 = -\frac{1}{2}R_{2n}; d_5 = \frac{1}{2}\left(R_{1n} + R_{2n}\right); d_6 = \frac{1}{2}\left(1 - R_{1n}\right) \tag{5.2}$$

Table 5.2 Switching Sequence under Different Conditions

	Max	Min	Med	Primary voltage					
1	*a*	*b*	c<0	u_{cc}	u_{ac}	u_{ab}	u_{ba}	u_{ca}	u_{cc}
2	*a*	*c*	b<0	u_{bb}	u_{ab}	u_{ac}	u_{ca}	u_{ba}	u_{bb}
3	*a*	*c*	b>0	u_{bb}	u_{bc}	u_{ac}	u_{ca}	u_{cb}	u_{bb}
4	*b*	*c*	a>0	u_{aa}	u_{ac}	u_{bc}	u_{cb}	u_{ca}	u_{aa}
5	*b*	*c*	a<0	u_{aa}	u_{ba}	u_{bc}	u_{cb}	u_{ab}	u_{aa}
6	*b*	*a*	c<0	u_{cc}	u_{bc}	u_{ba}	u_{ab}	u_{cb}	u_{cc}
7	*b*	*a*	c>0	u_{cc}	u_{ca}	u_{ba}	u_{ab}	u_{ac}	u_{cc}
8	*c*	*a*	b>0	u_{bb}	u_{ba}	u_{ca}	u_{ac}	u_{ab}	u_{bb}
9	*c*	*a*	b<0	u_{bb}	u_{cb}	u_{ca}	u_{ac}	u_{bc}	u_{bb}
10	*c*	*b*	a<0	u_{aa}	u_{ca}	u_{cb}	u_{bc}	u_{ac}	u_{aa}
11	*c*	*b*	a>0	u_{aa}	u_{ab}	u_{cb}	u_{bc}	u_{ba}	u_{aa}
12	*a*	*b*	c>0	u_{cc}	u_{cb}	u_{ab}	u_{ba}	u_{bc}	u_{cc}

Through selecting appropriate current reference, the duty cycle of each switching state can vary in a sinusoidal way. However, the current reference changes small in each switching cycle. Therefore, the output voltage is seen as a constant value in each switching cycle, as shown in Figure 5.5 (the output voltage u_1 and u_2 are assumed as constant). Due to the leakage inductor, the transition time of the current change direction is finite. At this time, the secondary voltage is clamped to zero voltage mandatory. The transition time in the shaded area can be calculated based on (5.3)

$$L_k \frac{di_p}{dt} = u_p - N u_{se} \tag{5.3}$$

The input current of the converter is constructed by the primary current, the effective duty cycles of each phase are less than expected due to the interval time in the shaded area. Therefore, the synthesized current is not equal to the current reference, so the current is distorted, and the value is reduced. The duty cycle losses (the shaded area) in the positive half cycle and negative half-cycle are calculated as (5.4), (5.5).

$$\Delta D_p = \frac{2i_{o1}L_k f_s}{Nu_1} \tag{5.4}$$

$$\Delta D_n = \frac{2i_{o1}L_k f_s}{Nu_2} \tag{5.5}$$

The duty cycle loss is related to the leakage inductor, switching frequency, output current, and the voltage magnitude of primary voltage. Once the switching frequency or the leakage inductor is high, the duty cycle loss cannot be neglected; therefore, the current will be distorted. Otherwise, the duty cycle loss is very low, and it can be ignored.

To compensate for the duty cycle loss without changing the duty cycle of d_3 and d_5, the current reference should be revised, as

$$\begin{aligned} R'_{1p} &= R_{1p} + 2\Delta D_p; \\ R'_{2p} &= R_{2p} \end{aligned} \tag{5.6}$$

$$\begin{aligned} R'_{1n} &= R_{1n} + 2\Delta D_n; \\ R'_{2n} &= R_{2n} - 2\Delta D_n \end{aligned} \tag{5.7}$$

When $i_a > i_c > i_b$ ($|i_a| \le |i_b|$), the waveforms are shown in Figure 5.6. The duty cycle of each switching state is presented as

$$\begin{aligned} d_1 &= \frac{1}{2}\left(1 + R_{2p}\right); d_2 = -\frac{1}{2}\left(R_{1p} + R_{2p}\right); d_3 = \frac{1}{2}R_{1p} \\ d_4 &= \frac{1}{2}R_{1n}; d_5 = -\frac{1}{2}\left(R_{1n} + R_{2n}\right); d_6 = \frac{1}{2}\left(1 + R_{2n}\right) \end{aligned} \tag{5.8}$$

The current references are changed as

$$\begin{aligned} R'_{1p} &= R_{1p} \\ R'_{2p} &= R_{2p} - 2\Delta D_p \end{aligned} \tag{5.9}$$

$$\begin{aligned} R'_{1n} &= R_{1n} + 2\Delta D_n \\ R'_{2n} &= R_{2n} - 2\Delta D_n \end{aligned} \tag{5.10}$$

Similarly, the duty cycle loss can be compensated in one fundamental cycle. Besides, the values of each reference are limited in [$2d_c$, 1-$2d_c$] to ensure each PWM pulse is longer than commutation time.

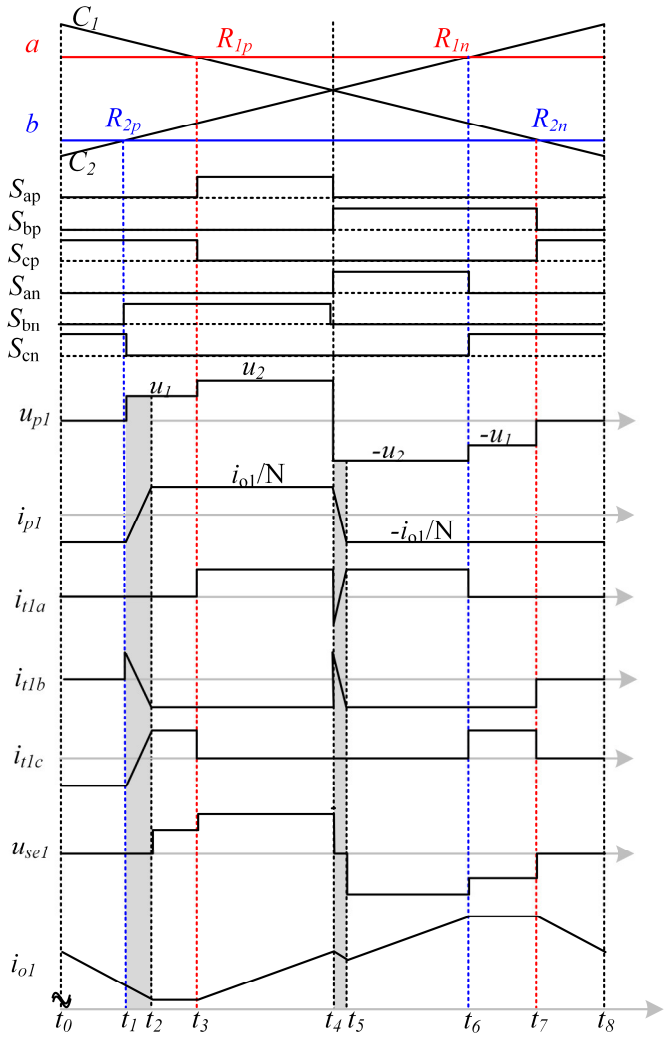


Figure 5.6 Comparison results when i_a>i_c>i_b ($|i_a| \leqslant |i_b|$), current references, carriers, gating signals, primary voltage, primary current, i_{ta}, i_{tb}, i_{tc}, secondary voltage, and DC current waveforms (from upper to lower)

5.3 Interleaved SPWM Strategy for Parallel Structure

Both the unidirectional isolated AC-DC matrix converters are designed to have the same rated power, the current reference for each converter is the same. The above proposed SPWM strategy is applied for each converter. However, the high-frequency carrier signals are interleaved, and the interleaved angle is determined by the number of the parallel converter ($360°/N$). The interleaved angle of the N^{th} converter is given as (5.11).

$$\varphi_N = \frac{360°}{N}\left(N-1\right) \tag{5.11}$$

With the interleaved carriers for two converters in a modular structure, the input phase current of each converter and total input phase current (i_{t1_a}, $i_{t2\_a,}$ and i_{t_a}), the output current of each converter and total output current (i_{o1}, $i_{o2,}$ and i_o) are presented in Figure 5.7. Through shifting carriers, the input phase current becomes a multilevel waveform. Therefore, the AC current quality can be improved. Moreover, the DC current ripple can be reduced significantly.

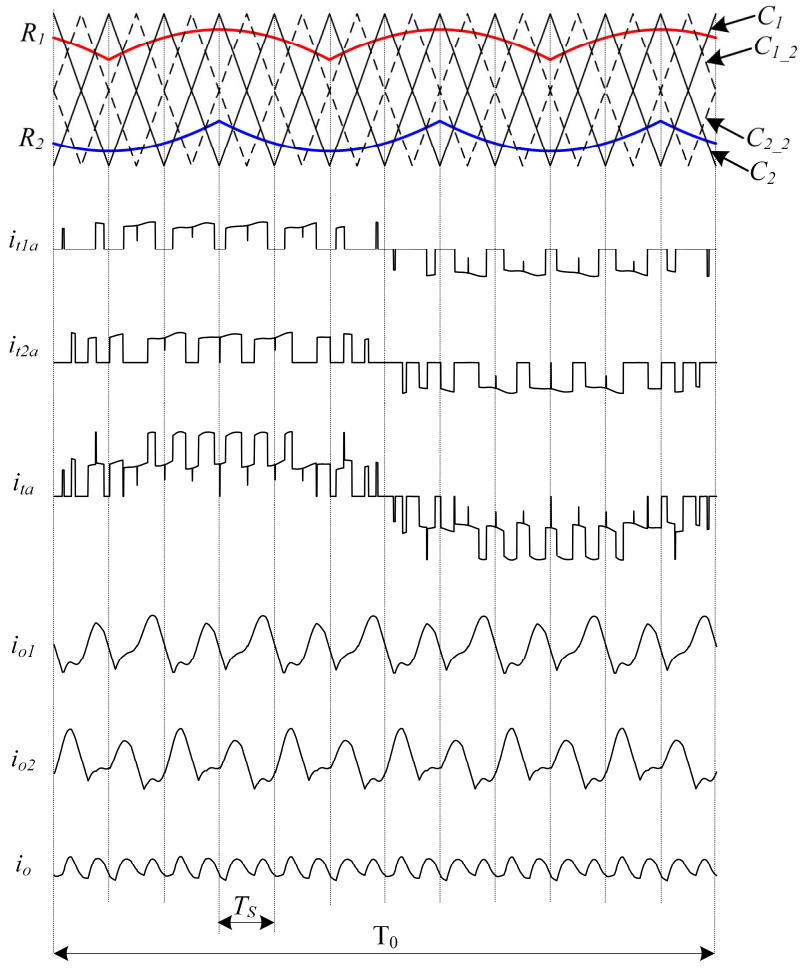


Figure 5.7 Two sets carriers for modular structure, input phase current of each converter and total input phase current, output DC current ripple of each converter and total output current ripple

The DC current depends on the voltage drop of the inductor filter, which can be calculated at any time.

$$L\frac{di_{o1}}{dt} = u_{o1} - u_{dc} \tag{5.12}$$

The current ripple can be normalized by based current (5.13), which is determined by switching frequency, filter inductor, and line-to-line voltage.

$$i_{dc\_based} = \frac{u_{ll}}{f_s L} \tag{5.13}$$

where f_s is the switching frequency and L is the DC filter inductor.

To verify the performance of the proposed interleaved SPWM strategy, the normalized maximum DC current ripple of non-interleaved SPWM, interleaved six-segment SVM strategy are calculated and presented in Figure 5.8. It shows that the non-interleaved SPWM has a higher DC current ripple than the other two methods, the maximum normalized current is 0.35. After interleaving the carriers, the maximum normalized DC current ripple is reduced to 0.0875. Furthermore, the normalized DC current ripple of the proposed interleaved SPWM method is lower than that in the interleaved six-segment SVM strategy.

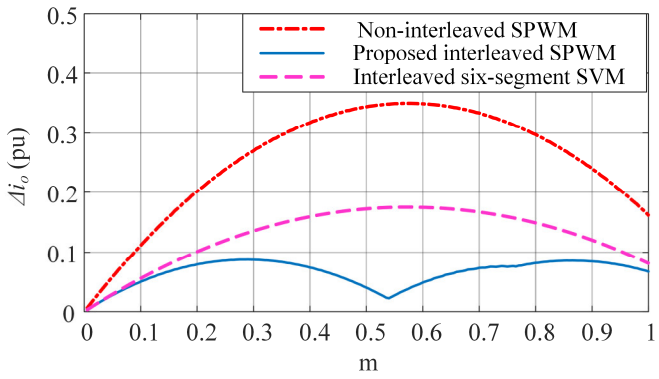


Figure 5.8 The normalized DC current ripple of non-interleaved SPWM, interleaved six-segment SVM strategy, and interleaved SPWM strategy when two unidirectional isolated AC-DC matrix converters are paralleled

5.4 Simulation and Experimental Verification

5.4.1 Simulation Verification

To verify the performance of the proposed SPWM method, a modular isolated matrix converter is simulated in MATLAB/Simulink. Table 5.3 lists the simulation

model parameters. Besides, the AC side is connected to the AC source (208V, 60Hz), and the DC side is connected to a resistor.

Table 5.3 Model Parameters

Parameters	Values
Filter inductor L_f	0.3mH
Filter capacitor C_f	30uF
Switching frequency	10kHz
Turns ratio	1:1
Leakage inductor L_k	2.6uH
Output filter inductor L	2.4mH
DC load, R	11.4Ω

Figure 5.9 shows the simulation results by applying the non-interleaved SPWM method when the modulation index is 0.8. The waveforms include the phase current, the primary voltage of the first converter, the primary voltage of the second converter, total DC current. It shows that the DC current ripple is 8.8A.

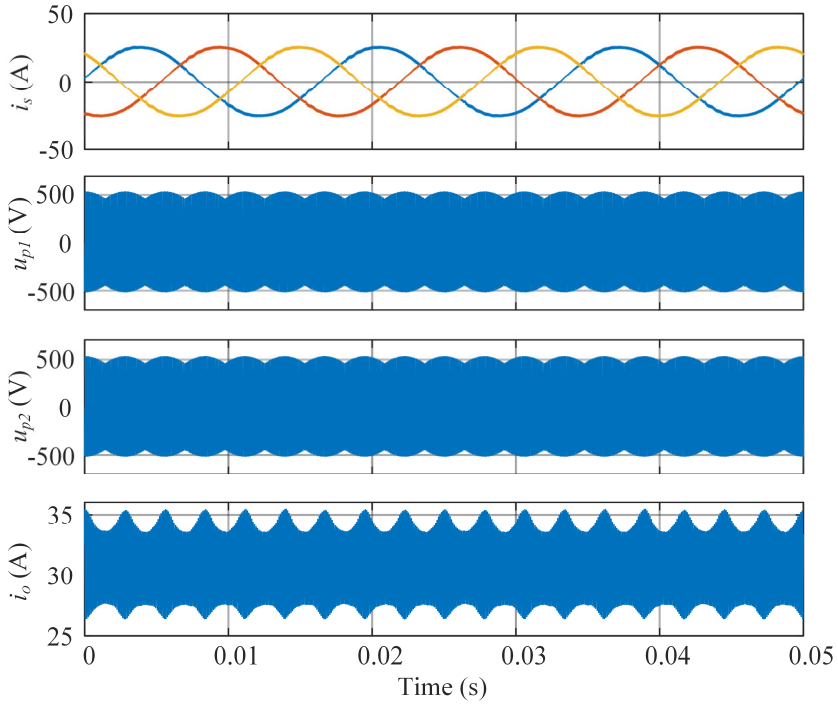


Figure 5.9 Simulation results of non-interleaved SPWM, phase current, the primary voltage of two converters, and DC current

To observe the high frequency waveforms, the primary voltages and DC current ripples are presented in Figure 5.10 in one switching cycle. It shows that the

primary voltage of the two converters are the same, and the DC current ripple is 7.5A.

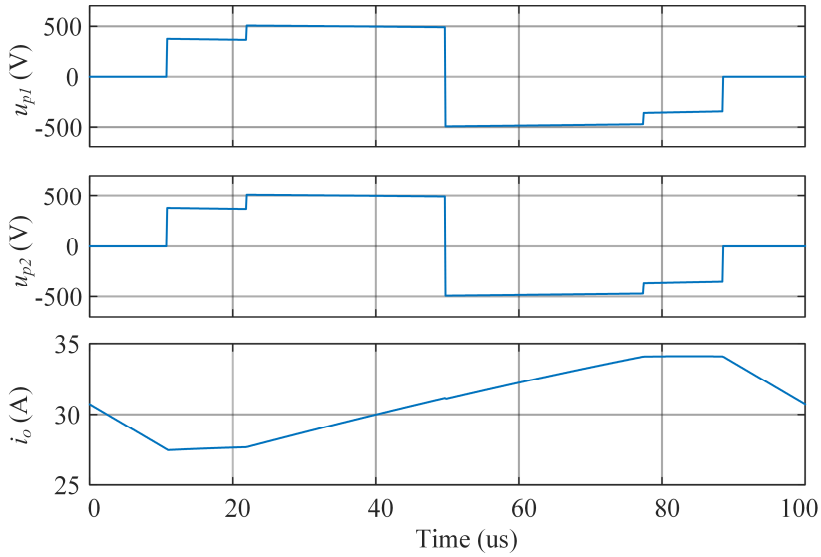


Figure 5.10 Simulation results of non-interleaved SPWM, the primary voltage of two converters, and DC current in one switching cycle

Applying the proposed interleaved SPWM strategy, the simulation results are given in Figure 5.11 (the modulation index is 0.8). From top to bottom, the waveforms are phase current, the primary voltage of the first converter, the primary voltage of the second converter, total DC current. The phase current value is the same as in Figure 5.9; however, the DC current ripple is reduced from 8.8A to 3A. In one switching cycle, the primary voltages of two converters and the DC current waveforms are presented in Figure 5.12. It can be found that the primary voltages of the two converters are interleaved 180°. Also, compared with Figure 5.10 the DC current is ripple is reduced from 7.5A to 2A in the proposed interleaved SPWM strategy.

The DC current FFT analysis of non-interleaved SPWM and proposed interleaved SPWM methods are compared in Figure 5.13. With the proposed interleaved SPWM strategy, the equivalent switching frequency is increased to 20kHz. Moreover, the THD of the DC current is reduced from 10.51% to 3.26%.

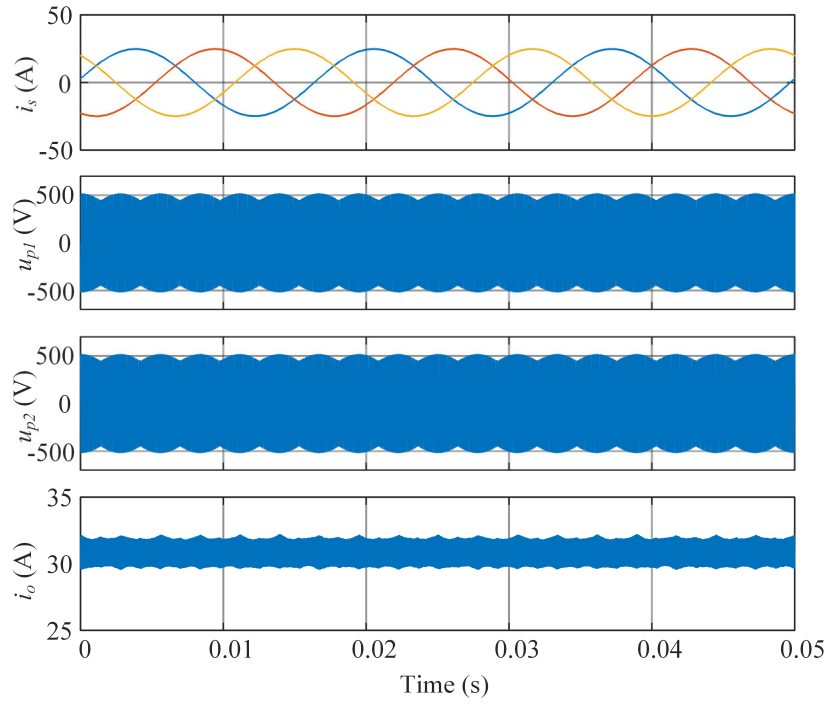


Figure 5.11 Simulation results of the proposed interleaved SPWM, phase current, the primary voltage of two converters, and DC current

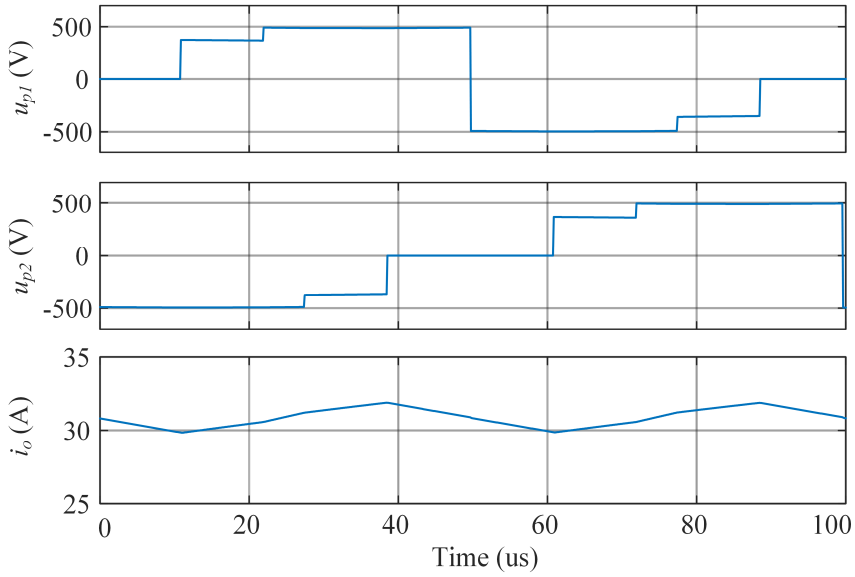


Figure 5.12 Simulation results of the proposed interleaved SPWM, the primary voltage of two converters, and DC current in one switching cycle

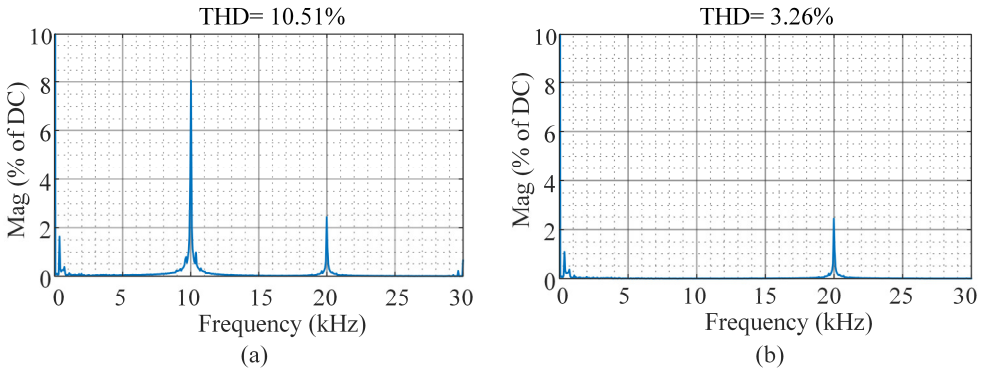


Figure 5.13 DC current THD of two methods (a) non-interleaved SPWM (b) proposed interleaved SPWM

Figure 5.14 and Figure 5.15 show the DC current ripple and phase current THD of non-interleaved SPWM, proposed interleaved SPWM strategy, and the interleaved six-segment SVM under different modulation index. Figure 5.14 shows that the proposed interleaved SPWM achieves the lowest DC current ripple and the conclusion is coordinated with Figure 5.8. Besides, the phase current THD is reduced in the interleaved SPWM strategy, as shown in Figure 5.15.

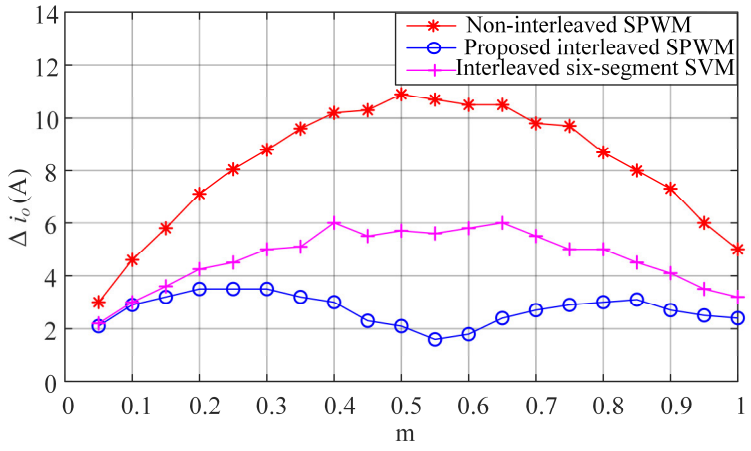


Figure 5.14 DC current ripple of non-interleaved SPWM, proposed interleaved SPWM strategy, and interleaved six-segment SVM strategy

Compared with the non-interleaved SPWM strategy, the interleaved SPWM strategy can improve both AC and DC current qualities. Furthermore, compared with the interleaved six-segment SVM strategy, the proposed interleaved SPWM strategy has a lower DC current ripple and lower phase current THD.

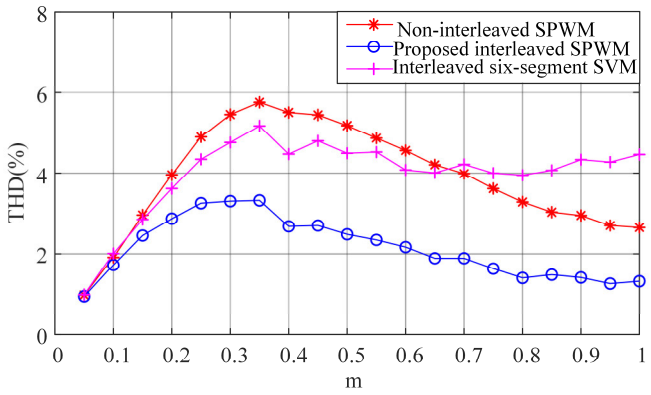


Figure 5.15 Phase current THD of non-interleaved SPWM, interleaved six-segment SVM strategy, and proposed interleaved SPWM strategy

5.4.2 Experimental Verification

The parallel unidirectional isolated AC-DC matrix converter prototype is built for experimental verification, as shown in Figure 5.16. The SiC MOSFETs are used to build bidirectional switches. Texas Instruments DSP TMS320F28379 and the Xilinx FPGA XC3S500E platform are used to implement the proposed SPWM method. The AC power supply is the programmable source AMETEK 4500Lx. The parameters are the same as the simulation model in Table 5.3. A voltage-based commutation strategy is applied to ensure the safe commutation of bidirectional switches.

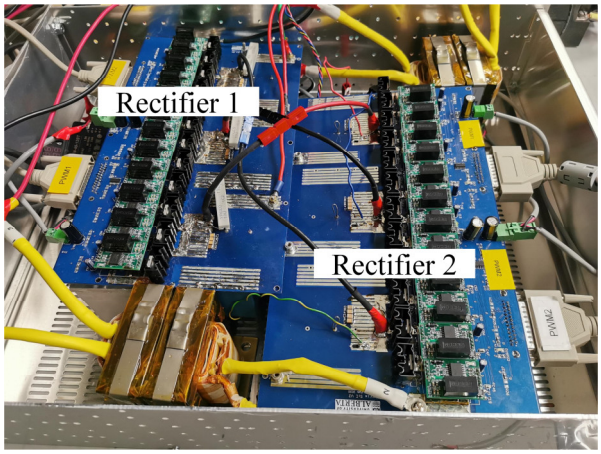


Figure 5.16 Experimental prototype of the parallel unidirectional isolated AC-DC matrix converter

Figure 5.17(a) and Figure 5.17(b) show the steady state experimental results of non-interleaved SPWM and proposed interleaved SPWM strategies under the

modulation index is 0.8. From top to bottom, waveforms are phase current, the primary voltage of the first converter, the primary voltage of the second converter, and DC current, respectively. The corresponding zoomed-in waveforms are presented in Figure 5.18(a) and (b), where the DC current is the current ripple waveforms.

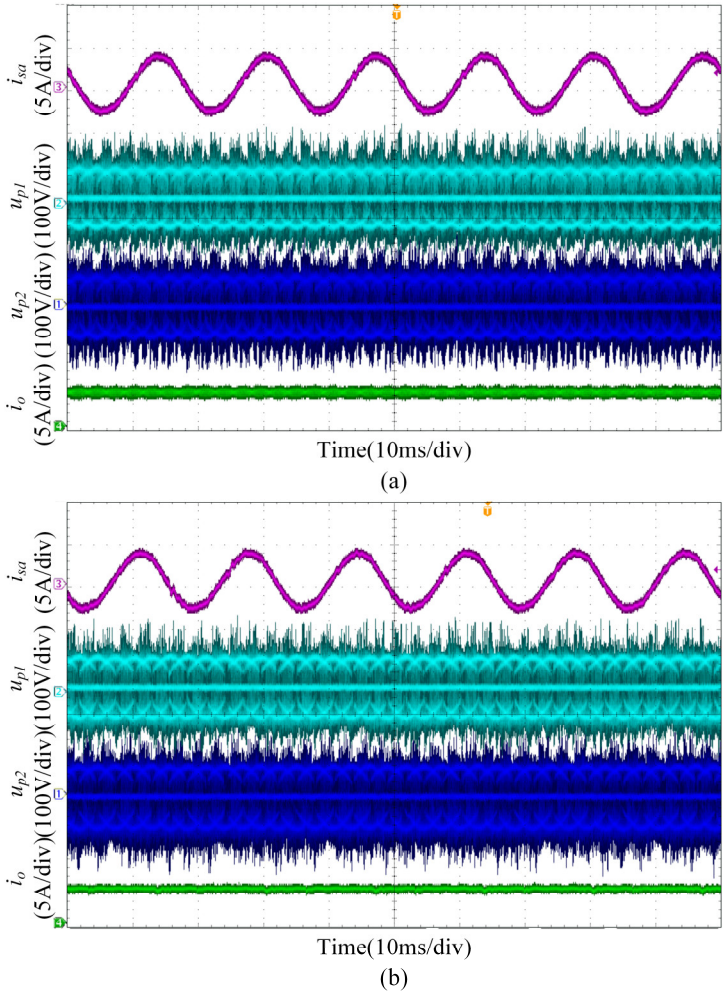


Figure 5.17 Experimental waveforms, phase current, the primary voltage of the first converter, the primary voltage of the second converter, and DC current (a) non-interleaved SPWM strategy (b) proposed interleaved SPWM strategy

The non-interleaved SPWM strategy has the same primary voltages of two converters which cause a high DC current ripple. By applying the proposed interleaved SPWM strategy, the primary voltages of two converters are interleaved, and the DC current ripple is reduced significantly. The FFT analysis of the two strategies is shown in Figure 5.19(a) and (b), respectively. It shows that after

applying the interleaved SPWM strategy, the equivalent switching frequency is increased from 10kHz to 20kHz, and the THD is reduced from 9.83% to 3.26%.

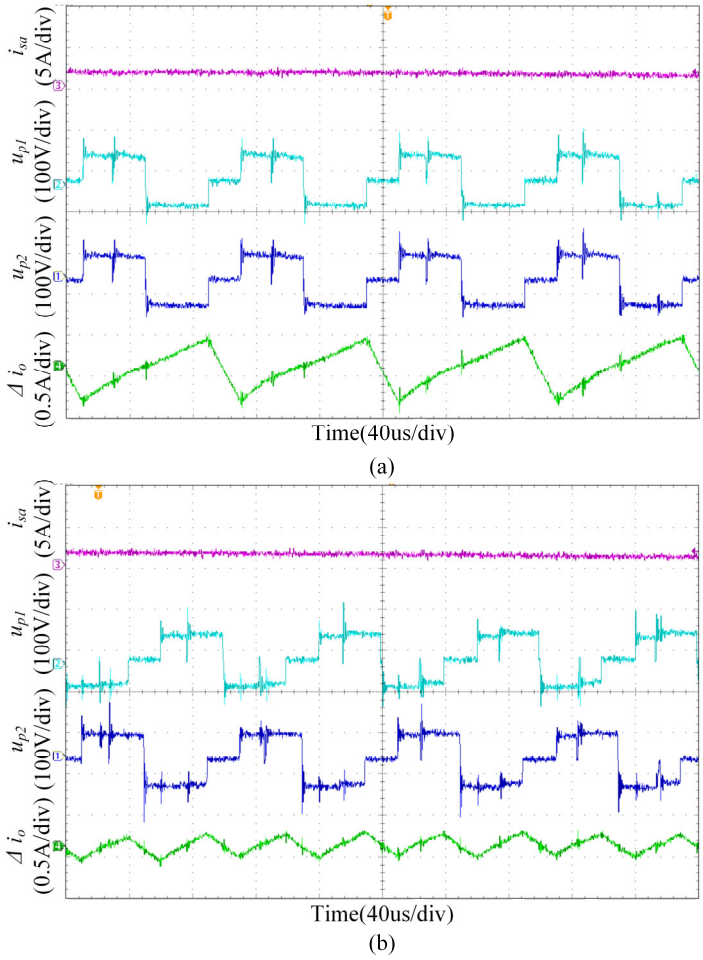


Figure 5.18 Zoom in Figure 5.17 (a) non-interleaved SPWM strategy (b) proposed interleaved SPWM strategy

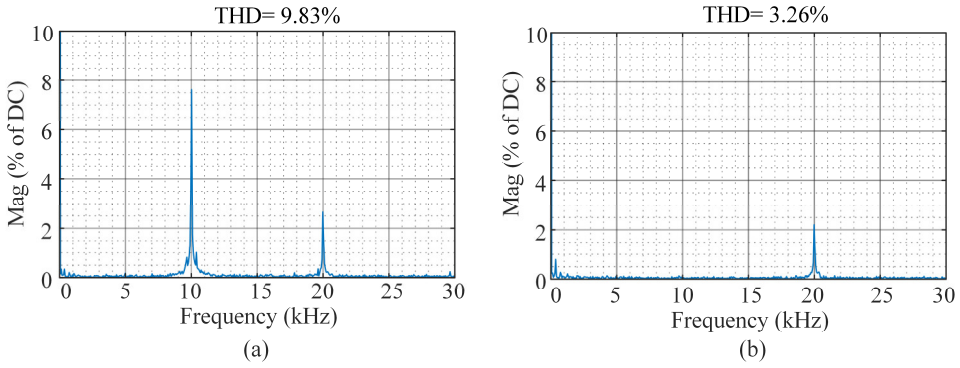


Figure 5.19 FFT analysis of DC current (a) non-interleaved SPWM strategy (b) proposed interleaved SPWM strategy

Figure 5.20 shows the transient experimental results when the load is changed from 11.4Ω to 15.2Ω. It can be found that the proposed interleaved SPWM strategy can reduce the DC current ripple at any load conditions.

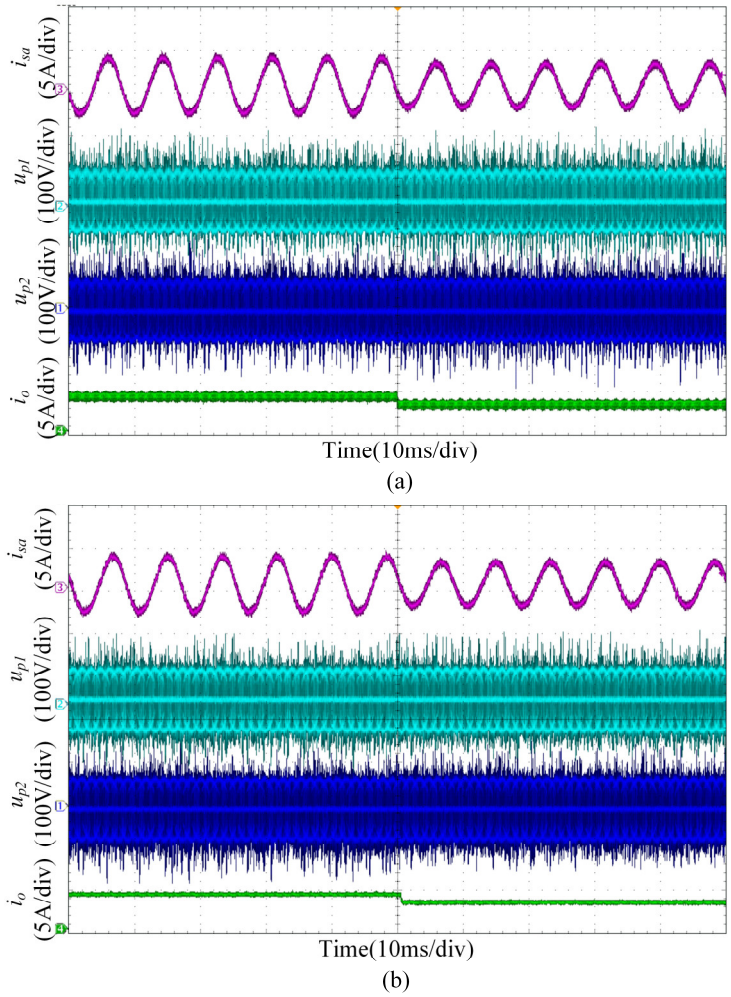


Figure 5.20 Experimental results when load changed from 11.4 Ω to 15.2 Ω, from top to bottom waveforms are phase current, the primary voltage of the first converter, the primary voltage of the second converter, and DC current (a) non-interleaved SPWM strategy (b) proposed interleaved SPWM strategy

5.5 Summary

Due to the galvanic isolation in the isolated AC-DC matrix converter, it is easy to parallel the converters to increase power rating or voltage level without generating a circulating current. With good scalability, the SPWM is preferable

than the multilevel SVM strategy for modular structures. This chapter takes a modular unidirectional isolated AC-DC matrix converter as an example and proposes a modular SPWM strategy for such topology to improve current quality. The proposed SPWM strategy is simple and easy to implement for modular converters. With the help of interleaved SPWM, multilevel AC current can be achieved, and the DC current ripple is reduced significantly.

Chapter 6

Conclusions and Future Work

6.1 Thesis Conclusions and Contributions

This thesis addressed the challenges in AC-DC matrix converters. Using improved modulation and control strategies, the commutation safety, AC current waveforms, and DC current ripple are improved. The main contributions of this thesis are listed as follows.

(1) Multiple Objectives Control in a non-isolated AC-DC matrix converter

To ensure commutation safety and control both AC and DC current simultaneously, an FCS-MPC method is proposed for the non-isolated AC-DC matrix converter. This method selects the optimal switching vector and applies it for one PWM period; therefore, the conventional modulation method is not needed. It also avoids pulses that are narrower than the required time for commutation. Thus, safe commutation can always be ensured without any extra procedures to check the pulse width. To improve the current qualities, virtual space vectors are designed and added. The proposed method has the following advantages: (1) both the AC current and DC current quality are considered in the cost function, which makes it possible to simultaneously achieve sinusoidal AC current and smooth DC current; (2) the virtual space vectors are used to further enhance the power quality without increasing the sampling frequency; (3) as the optimal switching vector is directly selected, narrow pulses can be avoided without using complicated PWM method; (4) fast transient can be obtained. Besides, considering the FCS-MPC is usually sensitive to model errors, the effects of parameter mismatch are investigated in this thesis. The design guidance to enhance the robustness is provided.

(2) Low order harmonics reduction in isolated AC-DC matrix converter

In an isolated AC-DC matrix converter, the low order harmonics are caused by commutation issues or modulation strategy. While the bidirectional switch's commutation has two challenges. Firstly, the narrow pulses shall be processed to ensure safe commutation. This leads to the mismatch between the synthesized current and the current reference, generating current distortions. Secondly, the commutation sequence during two bidirectional switches is determined by the relative magnitude of capacitor voltages. However, when the voltage of the two phases is close, it is difficult to distinguish the relative voltage magnitude. To solve these problems, a 9-segment SVM strategy is proposed. This strategy can avoid commutation between two phases with close voltage magnitude. Besides, the narrow pulses are reduced significantly by optimizing the zero vectors. This method can achieve high quality current even when the commutation duty ratio is relatively large.

However, with the development of the switching devices, the commutation time is reduced significantly. When the switching frequency is not very high (higher switching losses lower efficiency), the effect of the commutation time on the current distortion becomes smaller. Under this condition, another SVM strategy is proposed for the isolated AC-DC matrix converter. This method can reduce the number of switching actions while ensuring high current quality.

(3) Reduced current stress of HFT in isolated AC-DC matrix converter

In the isolated AC-DC matrix converter, the HFT can play an important role to transfer power between the AC side and DC side. The current stress on the transformer can be optimized by coordinating the modulation index and the phase-shift angle between 3-1 MC and the H-bridge. However, the conventional methods either set the modulation index or phase shift angle as a constant value. In this thesis, based on the proposed SVM method with reduced switching actions, coordinate control is developed to reduce the current stress of HFT. It optimizes the combination of modulation index and phase shift angle to produce the desired output power while keeping the current stress low on HFT. Moreover, with the proposed method, the power efficiency is increased.

(4) Interleaved SPWM to reduce DC current ripple for parallel unidirectional isolated AC-DC matrix converter

To best utilize the modularity of isolated AC-DC matrix converters, the performance enhancement is studied for parallel converters. A modular SPWM strategy is proposed to do interleave among paralleled unidirectional isolated AC-DC matrix converters. On one hand, multilevel AC current is achieved, and the equivalent switching frequency is increased. On the other hand, the DC current ripple is reduced, relaxing the constraints on the size of the filter inductor. More importantly, as a carrier-based modulation method, it has good scalability for paralleled converters.

6.2 Future Work

The suggestions for extending this research are as follows:

(1) Multi-rate Sampling MPC for non-isolated AC-DC matrix converter

In theory, applying a higher sampling frequency for MPC in a non-isolated AC-DC converter can achieve satisfying performance. However, in power converters, using a high sampling rate can import switching ripples of power semiconductors to the control system and degrade the control performance. A potential solution is to virtually increase the sampling rate—perform the sampling rate in a proper range while using a multi-rate model to calculate the control variables in a much smaller time step than the sampling period. This can create virtual sampling results in a high frequency without sampling switching noises. Then the traditional MPC can be applied but the switching frequency can be much higher.

(2) Soft switching of isolated AC-DC matrix converter

The soft switching technique can be applied to reduce the switching losses. By reducing the switching losses, the power efficiency can be improved. Also, the switching frequency can increase to achieve high performance with reduced switching losses. Among the three soft switching techniques, e.g. adding auxiliary switch, natural soft switching, adding passive components, the third solution

attracts attention these years. In future, the soft switching would be researched for isolated AC-DC matrix converter by adding capacitor in series with leakage inductor.

(3) Modular operation of isolated AC-DC matrix converter

To increase power rating or voltage level, a modular isolated AC-DC matrix converter is preferable due to simple connection, reliability improvement, enable low power rating switch devices, and simplicity of maintenance, etc. The modular operation of unidirectional isolated AC-DC matrix converter is researched in Chapter 5. However, the proposed interleaved SPWM method for unidirectional isolated AC-DC matrix converter can not be used for bidirectional isolated AC-DC matrix converter because numerous low order harmonics would be caused. For the modular bidirectional isolated AC-DC matrix converter, the interleaved SPWM should be researched. For example, the proposed SVM strategy in Chapter 4 can be converted to an SPWM strategy and applied in modular converters.

Besides, in a bidirectional isolated AC-DC matrix converter, the transferred power is related to leakage inductance. Therefore, the inevitable mismatch of the circuit parameters among module converters should be considered to share power among each module. Moreover, when converters plug-in or plug-out in the modular structure to increase or decrease the power capacity, the seamless operation should be studied to share power among them.

References

[1] H. Kakigano, Y. Miura and T. Ise, "Low-Voltage Bipolar-Type DC Microgrid for Super High Quality Distribution," in *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3066-3075, Dec. 2010.

[2] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues," in *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3528-3549, May 2016.

[3] D. G. Holmes, "A unified modulation algorithm for voltage and current source inverters based on AC-AC matrix converter theory," in *IEEE Transactions on Industry Applications*, vol. 28, no. 1, pp. 31-40, Jan.-Feb. 1992.

[4] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative Evaluation of Three-Phase AC–AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 12, pp. 4487-4510, Dec. 2012.

[5] P. Cortes, D. Bortis, R. Pittini, and J. W. Kolar, "Comparative evaluation of three-phase isolated matrix-type PFC rectifier concepts for high efficiency 380VDC supplies of future telco and data centers," *2014 16th European Conference on Power Electronics and Applications*, Lappeenranta, 2014, pp. 1-10.

[6] G. Rizzoli *et al*., "Comparison between an AC-DC matrix converter and an interleaved DC-dc converter with power factor corrector for plug-in electric vehicles," *2014 IEEE International Electric Vehicle Conference (IEVC)*, Florence, 2014, pp. 1-6.

[7] P. Drabek, Z. Peroutka, M. Pittermann and M. Cedl, "New Configuration of Traction Converter With Medium-Frequency Transformer Using Matrix Converters," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 11, pp. 5041-5048, Nov. 2011.

[8] S. Anand and B. G. Fernandes, "Optimal voltage level for DC microgrids," IECON 2010 - *36th Annual Conference on IEEE Industrial Electronics Society*, Glendale, AZ, 2010, pp. 3034-3039.

[9] A. Sannino, G. Postiglione and M. H. J. Bollen, "Feasibility of a DC network for commercial facilities," in *IEEE Transactions on Industry Applications*, vol. 39, no. 5, pp. 1499-1507, Sept.-Oct. 2003.

[10] R. J. Hill and F. L. Luo, "Current Source Optimization in AC-DC GTO Thyristor Converters," in *IEEE Transactions on Industrial Electronics*, vol. IE-34, no. 4, pp. 475-

482, Nov. 1987.

[11] Fang Zheng Peng, "Z-source inverter," in *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504-510, March-April 2003.

[12] L. Schrittwieser, J. W. Kolar and T. B. Soeiro, "Novel SWISS Rectifier Modulation Scheme Preventing Input Current Distortions at Sector Boundaries," in *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5771-5785, July 2017.

[13] F. Z. Peng, "Z-source inverter," *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, Pittsburgh, PA, USA, 2002, pp. 775-781 vol.2.

[14] Y. Tang, S. Xie, C. Zhang and Z. Xu, "Improved Z-Source Inverter With Reduced Z-Source Capacitor Voltage Stress and Soft-Start Capability," in *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 409-415, Feb. 2009.

[15] L. Schrittwieser, M. F. Vancu, J. W. Kolar and T. B. Soeiro, "Control of the input characteristic and the displacement factor of uni- and bidirectional SWISS rectifier for symmetrical and unsymmetrical three-phase mains," *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Seoul, 2015, pp. 40-47.

[16] M. Leibl, G. Ortiz and J. W. Kolar, "Design and Experimental Analysis of a Medium-Frequency Transformer for Solid-State Transformer Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 110-123, March 2017.

[17] A. Mallik and A. Khaligh, "Intermediate DC-Link Capacitor Reduction in a Two-Stage Cascaded AC/DC Converter for More Electric Aircrafts," in *IEEE Transactions on Vehicular Technology*, vol. 67, no. 2, pp. 935-947, Feb. 2018.

[18] Y. Son and J. Ha, "Direct Power Control of a Three-Phase Inverter for Grid Input Current Shaping of a Single-Phase Diode Rectifier With a Small DC-Link Capacitor," in *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3794-3803, July 2015.

[19] E. Koutroulis, J. Chatzakis, K. Kalaitzakis and N. C. Voulgaris, "A bidirectional, sinusoidal, high-frequency inverter design," in *IEE Proceedings - Electric Power Applications*, vol. 148, no. 4, pp. 315-321, July 2001.

[20] D. De and V. Ramanarayanan, "Analysis, Design, Modeling, and Implementation of an Active Clamp HF Link Converter," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 6, pp. 1446-1455, June 2011.

[21] V. K. Kanakesh, D. B. Yelaverthi, A. Ghoshal, A. K. Rathore and R. Mahanty,

"Analysis and Implementation of Closed-Loop Control of Electrolytic Capacitor-Less Six-Pulse DC-Link Bidirectional Three-Phase Grid-Tied Inverter," in *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 539-550, Jan.-Feb. 2018.

[22] W. Lee and S. Sul, "DC-Link Voltage Stabilization for Reduced DC-Link Capacitor Inverter," in *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 404-414, Jan.-Feb. 2014.

[23] V. Vlatkovic, D. Borojevic and F. C. Lee, "A zero-voltage switched, three-phase isolated PWM buck rectifier," in *IEEE Transactions on Power Electronics*, vol. 10, no. 2, pp. 148-157, March 1995.

[24] T. -L. Nguyen and H. -H. Lee, "Simplified Model Predictive Control for AC/DC Matrix Converters With Active Damping Function Under Unbalanced Grid Voltage," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2907-2917, Sept. 2020.

[25] Kunrong Wang, F. C. Lee, D. Boroyevich and Xinxiang Yan, "A new quasi-single-stage isolated three-phase ZVZCS buck PWM rectifier," *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, Baveno, Italy, 1996, pp. 449-455 vol.1.

[26] R. Garcia-Gil, J. M. Espi, E. J. Dede and E. Sanchis-Kilders, "A bidirectional and isolated three-phase rectifier with soft-switching operation," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 765-773, June 2005.

[27] M. Venturini and A. Alesina, "The generalised transformer: A new bidirectional, sinusoidal waveform frequency converter with continuously adjustable input power factor,"*1980 IEEE Power Electronics Specialists Conference*, Atlanta, Georgia, USA, 1980, pp. 242-252.

[28] H. Nikkhajoei, "A Current Source Matrix Converter for High-Power Applications," *2007 IEEE Power Electronics Specialists Conference*, Orlando, FL, USA, 2007, pp. 2516-2521.

[29] S. Bernet, S. Ponnaluri and R. Teichmann, "Design and loss comparison of matrix converters, and voltage-source converters for modern AC drives," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 304-314, April 2002.

[30] C. Klumpner, P. Nielsen, I. Boldea and F. Blaabjerg, "New solutions for a low-cost power electronic building block for matrix converters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 336-344, April 2002.

[31] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham and A. Weinstein,

"Matrix converters: a technology review," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 276-288, April 2002.

[32] C. Klumpner and F. Blaabjerg, "Using reverse-blocking IGBTs in power converters for adjustable-speed drives," in *IEEE Transactions on Industry Applications*, vol. 42, no. 3, pp. 807-816, May-June 2006.

[33] M. Takei, T. Naito and K. Ueno, "The reverse blocking IGBT for matrix converter with ultra-thin wafer technology," *ISPSD '03. 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, 2003. Proceedings.*, Cambridge, UK, 2003, pp. 156-159.

[34] L. Wei and T. A. Lipo, "A novel matrix converter topology with simple commutation," *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*, Chicago, IL, USA, 2001, pp. 1749-1754 vol.3.

[35] J. W. Kolar, F. Schafmeister, S. D. Round and H. Ertl, "Novel Three-Phase AC–AC Sparse Matrix Converters," in *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1649-1661, Sept. 2007.

[36] J. Schonberger, T. Friedli, S. D. Round and J. W. Kolar, "An Ultra Sparse Matrix Converter with a Novel Active Clamp Circuit," *2007 Power Conversion Conference - Nagoya*, Nagoya, 2007, pp. 784-791.

[37] D. G. Holmes and T. A. Lipo, "Implementation of a controlled rectifier using AC-AC matrix converter theory," *20th Annual IEEE Power Electronics Specialists Conference, Milwaukee*, WI, USA, 1989, pp. 353-359 vol.1.

[38] H. Dai, R. A. Torres, W. Lee, T. M. Jahns and B. Sarlioglu, "Integrated Motor Drive using Soft-Switching Current-Source Inverters with SiC- and GaN-based Bidirectional Switches," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 2372-2378.

[39] S. Manias and P. D. Ziogas, "A Novel Sinewave in AC to DC Converter with High-Frequency Transformer Isolation," in *IEEE Transactions on Industrial Electronics*, vol. IE-32, no. 4, pp. 430-438, Nov. 1985.

[40] N. D. Weise, K. K. Mohapatra and N. Mohan, "Universal utility interface for Plug-in Hybrid electric vehicles with vehicle-to-grid functionality," *IEEE PES General Meeting*, Providence, RI, 2010, pp. 1-8.

[41] L. Empringham, J. W. Kolar, J. Rodriguez, P. W. Wheeler and J. C. Clare, "Technological Issues and Industrial Application of Matrix Converters: A Review," in

IEEE Transactions on Industrial Electronics, vol. 60, no. 10, pp. 4260-4271, Oct. 2013.

[42] L. Empringham, P. W. Wheeler and J. C. Clare, "Intelligent commutation of matrix converter bi-directional switch cells using novel gate drive techniques," *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, Fukuoka, 1998, pp. 707-713 vol.1.

[43] N. Burany, "Safe control of four-quadrant switches," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, San Diego, CA, USA, 1989, pp. 1190-1194 vol.1.

[44] A. Ecklebe, A. Lindemann and S. Schulz, "Bidirectional Switch Commutation for a Matrix Converter Supplying a Series Resonant Load," in *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1173-1181, May 2009.

[45] A. Alesina and M. G. B. Venturini, "Analysis and design of optimum-amplitude nine-switch direct AC-AC converters," in *IEEE Transactions on Power Electronics*, vol. 4, no. 1, pp. 101-112, Jan. 1989.

[46] P. W. Wheeler, J. C. Clare, L. Empringharn, M. Bland and M. Apap, "Gate drive level intelligence and current sensing for matrix converter current commutation," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 382-389, April 2002.

[47] Jang-Hyoun Youm and Bong-Hwan Kwon, "Switching technique for current-controlled AC-to-AC converters," in *IEEE Transactions on Industrial Electronics*, vol. 46, no. 2, pp. 309-318, April 1999.

[48] H. She, H. Lin, B. He, X. Wang, L. Yue and X. An, "Implementation of Voltage-Based Commutation in Space-Vector-Modulated Matrix Converter," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 154-166, Jan. 2012.

[49] K. Kato and J. Itoh, "Improvement of Input Current Waveforms for a Matrix Converter Using a Novel Hybrid Commutation Method," *2007 Power Conversion Conference - Nagoya*, Nagoya, 2007, pp. 763-768.

[50] S. Takuma and J. Itoh, "Hybrid commutation method with current direction estimation for three-phase-to-single-phase matrix converter," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 672-679.

[51] M. Ziegler and W. Hofmann, "New one-step commutation strategies in matrix converters," *4th IEEE International Conference on Power Electronics and Drive Systems. IEEE PEDS 2001 - Indonesia. Proceedings (Cat. No.01TH8594)*, Denpasar,

Indonesia, 2001, pp. 560-564 vol.2.

[52] S. M. A. Cruz, A. M. S. Mendes and A. J. M. Cardoso, "A New Fault Diagnosis Method and a Fault-Tolerant Switching Strategy for Matrix Converters Operating With Optimum Alesina-Venturini Modulation," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 269-280, Jan. 2012.

[53] P. C. Loh, R. Rong, F. Blaabjerg and P. Wang, "Digital Carrier Modulation and Sampling Issues of Matrix Converters," in *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1690-1700, July 2009.

[54] B. Feng, H. Lin, X. Wang, X. An and B. Liu, "Optimal zero-vector configuration for space vector modulated AC-DC matrix converter," 2012 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, 2012, pp. 291-297.

[55] M. Mengoni, L. Zarri, A. Tani, G. Rizzoli, G. Serra, and D. Casadei, "Modulation strategies for three-phase AC-DC matrix converters: A comparison, "2016 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-7.

[56] M. Su, H. Wang, Y. Sun, J. Yang, W. Xiong, and Y. Liu, "AC/DC Matrix Converter With an Optimized Modulation Strategy for V2G Applications," in *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5736-5745, Dec. 2013.

[57] T. Nguyen and H. Lee, "A Space Vector Modulation Method to Reduce Output Current Ripple at Unity Grid Power Factor for AC/DC Matrix Converters," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, Lisbon, Portugal, 2019, pp. 1561-1566.

[58] H. Long Dang, Eun-Su Jun, Sangshin Kwak, " Reduction of DC Current Ripples by Virtual Space Vector Modulation for Three Phase AC-DC Matrix Converters," in *Energies* 2019, 12(22), 4319.

[59] M. A. Sayed, K. Suzuki, T. Takeshita, and W. Kitagawa, “PWM switching technique for three-phase bidirectional grid-tie DC–AC–AC converter with high-frequency isolation,” *IEEE Trans. Power Electron*., vol. 33, no. 1, pp. 845–858, Jan. 2018.

[60] M. A. Sayed, K. Suzuki, T. Takeshita, and W. Kitagawa, “Grid-tie isolated bidirectional DC-AC-AC converter based on high frequency transformer with high efficiency and low THD,” in *Proc. 19th Eur. Conf. Power Electron*. Appl., Warsaw, Poland, 2017, pp. P.1–P.10.

[61] M. A. Sayed, T. Takeshita, and W. Kitagawa, “Steady-state analysis of soft switched three-phase grid-tie DC-AC converter isolated by high-frequency transformer

for high efficiency and low THD," in *Proc. 20th Eur. Conf. Power Electron*. Appl., Riga, Latvia, 2018, pp. P.1–P.10.

[62] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems-Redline, *IEEE Standard 519-2014* (Revision of IEEE Standard 519-1992)—Redline, pp. 1–213, Jun. 11, 2014.

[63] D. Varajão, R. E. Araújo, L. M. Miranda, and J. A. P. Lopes, "Modulation strategy for a single-stage bidirectional and isolated AC–DC matrix converter for energy storage systems," *IEEE Trans. Ind. Electron*., vol. 65, no. 4, pp. 3458–3468, Apr. 2018.

[64] D. Das, N. Weise, K. Basu, R. Baranwal, and N. Mohan, "A bidirectional soft-switched DAB-based single-stage three-phase AC–DC converter for V2G application," *IEEE Trans. Transp. Electrific*., vol. 5, no. 1, pp. 186–199, Mar. 2019.

[65] J. Afsharian, D. David Xu, B. Gong, and Z. Yang, "Space vector demonstration and analysis of zero-voltage switching transitions in three-phase isolated PWM rectifier," 2015 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 2477-2484.

[66] J. Afsharian, D. Xu, T. Zhao, B. Gong, and Z. Yang, "Reduced duty-cycle loss and output inductor current ripple in a ZVS switched three-phase isolated PWM rectifier," 2016 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 33-37.

[67] T. Zhao, X. Guo, J. Su and D. Xu, "Improved space vector modulation for matrix converter based isolated rectifiers," *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Dallas, TX, 2014, pp. 1532-1536.

[68] J. Afsharian, D. David Xu, B. Wu, B. Gong and Z. Yang, "Improved eight-segment PWM scheme with non-equally distributed zero-vector intervals for a three-phase isolated buck matrix-type rectifier," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 3415-3419.

[69] J. Afsharian, D. Xu, B. Wu, B. Gong, and Z. Yang, "The Optimal PWM Modulation and Commutation Scheme for a Three-Phase Isolated Buck Matrix-Type Rectifier," in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 110-124, Jan. 2018.

[70] K. You, D. Xiao, M. F. Rahman, and M. N. Uddin, "Applying Reduced General Direct Space Vector Modulation Approach of AC-AC Matrix Converter Theory to Achieve Direct Power Factor Controlled Three-Phase AC-DC Matrix Rectifier," in *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 2243-2257, May-June

2014.

[71] B. Feng, H. Lin, S. Hu, X. An and X. Wang, "Control strategy of AC-DC matrix converter in battery energy storage system," 2012 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, 2012, pp. 2128-2134.

[72] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo and J. Rodriguez, "Predictive Control in Power Electronics and Drives," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4312-4324, Dec. 2008.

[73] Rodriguez et al., "State of the Art of Finite Control Set Model Predictive Control in Power Electronics," in *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 1003-1016, May 2013.

[74] A. A. Ahmed, B. K. Koh and Y. I. Lee, "A Comparison of Finite Control Set and Continuous Control Set Model Predictive Control Schemes for Speed Control of Induction Motors," in *IEEE Transactions on Industrial Informatics*, vol. 14, no. 4, pp. 1334-1346, April 2018.

[75] B. Stellato, T. Geyer and P. J. Goulart, "High-Speed Finite Control Set Model Predictive Control for Power Electronics," in *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 4007-4020, May 2017.

[76] P. Falkowski and A. Sikorski, "Finite Control Set Model Predictive Control for Grid-Connected AC–DC Converters With LCL Filter," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 2844-2852, April 2018.

[77] H. Eskandari-Torbati, D. Arab Khaburi and V. Eskandari-Torbati, "Virtual flux based Direct Power Control (DPC) of three phase PWM rectifier using Model Predictive Control (MPC) and Space Vector Modulation (SVM)," The *5th Annual International Power Electronics, Drive Systems and Technologies Conference (PEDSTC 2014)*, Tehran, 2014, pp. 242-248.

[78] S. Vazquez et al., "Model Predictive Control with constant switching frequency using a Discrete Space Vector Modulation with virtual state vectors," *2009 IEEE International Conference on Industrial Technology, Gippsland*, VIC, 2009, pp. 1-6.

[79] Y. Zhang, W. Xie, Z. Li and Y. Zhang, "Low-Complexity Model Predictive Power Control: Double-Vector-Based Approach," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 11, pp. 5871-5880, Nov. 2014.

[80] Z.Zhou, C. Xia, Y. Yan, Z. Wang and T. Shi, "Torque Ripple Minimization of Predictive Torque Control for PMSM With Extended Control Set," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 6930-6939, Sept. 2017.

[81] J. Lee, J. Lee, H. Moon and K. Lee, "An Improved Finite-Set Model Predictive Control Based on Discrete Space Vector Modulation Methods for Grid-Connected Three-Level Voltage Source Inverter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 1744-1760, Dec. 2018.

[82] H. Moon, J. Lee and K. Lee, "A Robust Deadbeat Finite Set Model Predictive Current Control Based on Discrete Space Vector Modulation for a Grid-Connected Voltage Source Inverter," in *IEEE Transactions on Energy Conversion*, vol. 33, no. 4, pp. 1719-1728, Dec. 2018.

[83] C. Jiang, G. Du, F. Du and Y. Lei, "A Fast Model Predictive Control with Fixed Switching Frequency Based on Virtual Space Vector for Three-Phase Inverters," 2018 *IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, 2018, pp. 1-7.

[84] T. Wang, Y. Guo and J. Zhu, "Finite-control-set model predictive direct torque control of PMSMs with virtual space vectors," 2017 *12th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Siem Reap, 2017, pp. 1427-1430.

[85] W. Alhosaini and Y. Zhao, "A Model Predictive Voltage Control using Virtual Space Vectors for Grid-Forming Energy Storage Converters," 2019 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 1466-1471.

[86] T. He, J. Zhu, D. D. Lu and L. Zheng, "Modified Model Predictive Control for Bidirectional Four-Quadrant EV Chargers With Extended Set of Voltage Vectors," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 274-281, March 2019.

[87] K. S. Alam, D. Xiao, M. Parvez Akter, D. Zhang, J. Fletcher and M. F. Rahman, "Modified MPC with extended VVs for grid-connected rectifier," in *IET Power Electronics*, vol. 11, no. 12, pp. 1926-1936, 16 10 2018.

[88] P. Cortes, J. Rodriguez, C. Silva and A. Flores, "Delay Compensation in Model Predictive Current Control of a Three-Phase Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 1323-1325, Feb. 2012.

[89] H. Gao, B. Wu, D. Xu and N. R. Zargari, "A Model Predictive Power Factor Control Scheme With Active Damping Function for Current Source Rectifiers," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2655-2667, March 2018.

[90] R. N. Fard, H. Nademi and L. Norum, "Analysis of a Modular Multilevel inverter under the predicted current control based on Finite-Control-Set strategy," *2013 3rd*

International Conference on Electric Power and Energy Conversion Systems, Istanbul, Turkey, 2013, pp. 1-6..

[91] M. Novak, U. M. Nyman, T. Dragicevic and F. Blaabjerg, "Analytical Design and Performance Validation of Finite Set MPC Regulated Power Converters," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2004-2014, March 2019.

[92] M. Ziegler and W. Hofmann, "Implementation of a two steps commutated matrix converter," *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, Charleston, SC, USA, 1999, pp. 175-180 vol.1.

[93] J. Mahlein, J. Igney, J. Weigold, M. Braun and O. Simon, "Matrix converter commutation strategies with and without explicit input voltage sign measurement," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 407-414, April 2002.

[94] B. Zhao, Q. Song, W. Liu and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091-4106, Aug. 2014.

[95] Y. Mei, Q. Lu and Z. Liu, "A Novel partition-phase-shift Control Strategy for the Isolated Bidirectional AC/DC Matrix Converter," *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, Nanjing, China, 2020, pp. 2490-2494.

[96] F. Fang and Y. W. Li, "Modulation and control method for bidirectional isolated AC/DC matrix-based converter in hybrid AC/DC microgrid," 2017 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 37-43.

[97] F. Wu, F. Feng, and H. B. Gooi, "Cooperative Triple-Phase-Shift Control for Isolated DAB DC-DC Converter to Improve Current Characteristics," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 7022- 7031, Sept. 2019.

[98] R. Wang, J. Zhao, and Y. Liu, "A comprehensive investigation of four switch three-phase voltage source inverter based on double fourier integral analysis," *IEEE Trans. Power Electron*., vol. 26, no. 10, pp. 2774–2787, Oct. 2011.

[99] W. Kuo, H. Lin, Z. Xu and W. Zhang, "Reliability Optimization with the Lagrange-Multiplier and Branch-and-Bound Technique," in *IEEE Transactions on Reliability*, vol. R-36, no. 5, pp. 624-630, Dec. 1987.

[100] Stephen Boyd, Lieven Vandenberghe, Convex Optimization, *Cambridge University Press*, New York, United States, 2004.

[101] M. Li, "Generalized Lagrange Multiplier Method and KKT Conditions With an

Application to Distributed Optimization," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 2, pp. 252-256, Feb. 2019.

[102] D. Lan, P. Das, and S. K. Sahoo, “A high-frequency link matrix rectifier with a pure capacitive output filter in a discontinuous conduction mode,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 4–15, Jan. 2020.

[103] W. Hu, Y. Xie, Y. Guan, Z. Wang, Z. Zhang, and J. Xu, "A Novel Volt-Second Self-Balancing SVPWM Scheme to Eliminate Steady-State DC Bias for a Three-Phase Isolated AC–DC Matrix Converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11518-11532, Nov. 2020.

[104] J. S. Siva Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 76-91, Jan. 2014.

[105] D. Zhang, F. Fred Wang, R. Burgos and D. Boroyevich, "Common-Mode Circulating Current Control of Paralleled Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation," in *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3925-3935, Dec. 2011.

[106] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich, "Total Flux Minimization Control for Integrated Inter-Phase Inductors in Paralleled, Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation," in *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1679-1688, April 2012.

[107] L. Ding and Y. W. Li, "Simultaneous DC Current Balance and CMV Reduction for Parallel CSC System with Interleaved Carrier-Based SPWM," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8495-8505, Oct. 2020.