**University of Alberta**

# Design of Active CMOS Multiband Ultra-Wideband Receiver Front-End

by

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## Abstract

Inductors are extensively used in the design of radio-frequency circuits. In the last decade, the integration of passive components, especially inductors on silicon chips, has led to the widespread development and implementation of Radio Frequency Integrated Circuits (RFICs) in CMOS technologies. However, on-chip passive inductors occupy a large silicon chip area and hardly scale down with technology scaling. Therefore, on-chip passive inductors become formidable obstacles to the realization of highly dense RFICs to be integrated with other highly dense digital circuits on a single chip using a common fabrication process. In recent years, researchers have focused on replacing passive inductors with transistor-only active circuits, namely active inductors. Active inductors can be realized with only a few transistors, which scale down with technology scaling. Therefore, they occupy a fraction of the chip area of their passive counterparts, and can be implemented densely in CMOS processes. Unlike passive inductors, bias dependent operations of active inductors allow for the tuning of their inductance and quality factor ($Q$), and in turn, tuning the performance parameters of RFICs.

This thesis focuses on the design and development of passive inductorless CMOS RFICs for ultra-wideband (UWB) receiver front-ends using active inductors. A new $Q$-enhanced and a new bandwidth-extended tunable active inductors are designed. Using the $Q$-enhanced active inductor, two tunable UWB low-noise amplifiers (LNAs) (two-stage and three-stage UWB LNAs), a UWB mixer and a wideband local-oscillator (LO) driver are designed. Active inductors are utilized to develop a novel wideband active shunt-peaking tech-

nique that decreases high-frequency losses to yield a flat gain over a wide bandwidth. A tunable multiband-UWB front-end integrating a two-stage UWB LNA, and a pair of UWB mixers driven by a pair of wideband LO drivers, is fabricated in a 90nm digital CMOS process. The passive inductorless two-stage UWB LNA, three-stage UWB LNA and UWB front-end occupy chip areas of only 0.0114mm$^2$, 0.0227mm$^2$, and 0.1485mm$^2$, respectively. The active CMOS UWB front-end exhibits a measured flat gain of 22.5dB over 2.5-8.8 GHz bandwidth, and its tunability allows for varying the gain and bandwidth.

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For my wife Tanzina,
my daughter Nojhat, and my son Taanish.

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# List of Abbreviations

| | |
|---|---|
| RF | Radio frequency |
| RFIC | Radio frequency integrated circuit |
| CMOS | Complementary metal oxide semiconductor |
| UWB | Ultra-wideband |
| LNA | Low-noise amplifier |
| LO | Local oscillator |
| Hz | Hertz |
| GHz | Giga hertz |
| MHz | Megahertz |
| dB | decibel |
| m | Meter |
| mm | Millimeter |
| cm | Centimeter |
| $\mu$m | Micrometer |
| nm | Nanometer |
| mV | Millivolt |
| mA | Milliampere |
| MOS | Metal-oxide semiconductor |
| MOSFET | Metal-oxide semiconductor field-effect transistor |
| DSP | Digital signal processing |
| AI | Active inductor |
| H | Henry |
| nH | Nanohenry |
| DC | Direct current |

| | |
|---|---|
| AC | Alternate current |
| Mb | Megabit |
| s | Second |
| Mb/s | Megabit per second |
| ns | Nanosecond |
| WPAN | Wireless personal area network |
| MB | Multiband |
| FCC | Federal Communications Commission |
| IF | Intermediate frequency |
| 3D | Three dimensional |
| W | Transistor's width |
| L | Transistor's length |
| MMIC | Monolithic microwave integrated circuit |
| GaAs | Gallium arsenide |
| GIC | Generalized impedance converter |
| DUT | Device under test |
| LF | Low frequency |
| HF | High frequency |
| MF | Mid frequency |
| Re | Real |
| Im | Imaginary |
| S-parameter | Scattering parameter |
| SNR | Signal-to-noise ratio |
| NF | Noise figure |
| log | Logarithm |
| IM | Intermodulation |
| CP | Compression point |
| IP3 | Third-order intercept-point |
| IIP3 | Input third-order intercept-point |
| VNA | Vector network analyzer |
| BW | Bandwidth |
| BPF | Bandpass filter |

| | |
|---|---|
| MIM | Metal-insulator-metal |
| DSB | Double sideband |
| CG | Conversion gain |
| VCO | Voltage-controlled oscillator |

# List of Symbols

| | |
|---|---|
| $Q$ | Quality factor |
| $\omega$ | Angular frequency rad/s |
| $\Omega$ | Ohm |
| $L$ | Inductance |
| $C$ | Capacitance |
| $V$ | DC Voltage |
| $P$ | Power |
| $v$ | AC Voltage |
| $I$ | DC current |
| $i$ | AC current |
| $f$ | Frequency in Hz |
| $R$ | Resistance |
| $G$ | Conductance |
| $Z$ | Impedance |
| $Y$ | Admittance |
| $B$ | Magnetic field |
| $E$ | Electric field |
| M | Transistor |
| $A_v$ | Voltage gain |
| $A_i$ | Current gain |
| $\mu$ | micro |
| $\pi$ | pi |
| $\alpha$ | alpha |
| $\beta$ | beta |

| | |
|---|---|
| $\gamma$ | gamma |
| $\lambda$ | lambda |
| $\Delta$ | delta |
| $\Gamma$ | Gamma |
| $\approx$ | Approximately |
| $\infty$ | Infinity |
| $>$ | Greater than |
| $<$ | Less than |
| $\geqslant$ | Greater than or equal |
| $\leqslant$ | Less than or equal |
| $f_0$ | Resonance frequency (Hz) |
| $\omega_0$ | Angular resonance frequency (rad/s) |
| $f_t$ | Unity-gain cut-off frequency |
| $f_{sr}$ | Self-resonance frequency |
| $RLC$ | Resistance-inductance-capacitance |
| $\triangle\ \omega$ | Angular -3dB bandwidth |
| $V_{DD}$ | DC power supply voltage |
| $V_{SS}$ | Ground |
| $V_{TN}$ | NMOS transistor's threshold voltage |
| $C_{ox}$ | Transistor's gate-oxide capacitance in Farad/cm$^2$ |
| $\mu_n$ | Electron mobility in cm$^2$/V-s |
| $g_m$ | Transistor's transconductance |
| $g_d$ | Transistor's drain conductance |
| $S_{11}$ | Input return loss |
| $S_{12}$ | Reverse isolation |
| $S_{21}$ | Forward gain |
| $S_{22}$ | Output return loss |
| $F$ | Noise factor |
| $F_{min}$ | Minimum noise factor |

# Chapter 1

# Introduction

## 1.1 Motivation for Active CMOS RFIC Design

The ever increasing demand for wireless technologies is continuously calling for the development of high bandwidth, low power, small size and low cost radio-frequency (RF) transceivers. In reducing the size and cost of transceiver chipsets, designers in the late 1990's started using CMOS technologies to integrate RF, analog, and digital circuits of transceivers on a single-chip. CMOS processes offer the highest level of device integration and the lowest fabrication cost among all of the process technologies available in the semiconductor industry. Importantly, the aggressive scaling (shrinking) of active devices (MOS transistors) in deep submicron CMOS processes allows for integration of more transistors per unit area of silicon die going from one technology node to the next one. However, passive devices such as resistors, capacitors and inductors, which are widely used in RF integrated circuits (RFICs), hardly scale down (shrink) with technology scaling. Among all of these passive components, inductors are the most bulky as they occupy a large percentage of the chip area to obtain required inductance values. Consequently, RFICs using passive inductors occupy a large chip (or die) area with increased cost. Hence, it is highly desirable to replace area-inefficient (occupying a costly large die area) on-chip passive inductors with transistor-only active circuits to reduce the die sizes of RFICs and integrate them densely for low cost high volume production of RF transceivers.

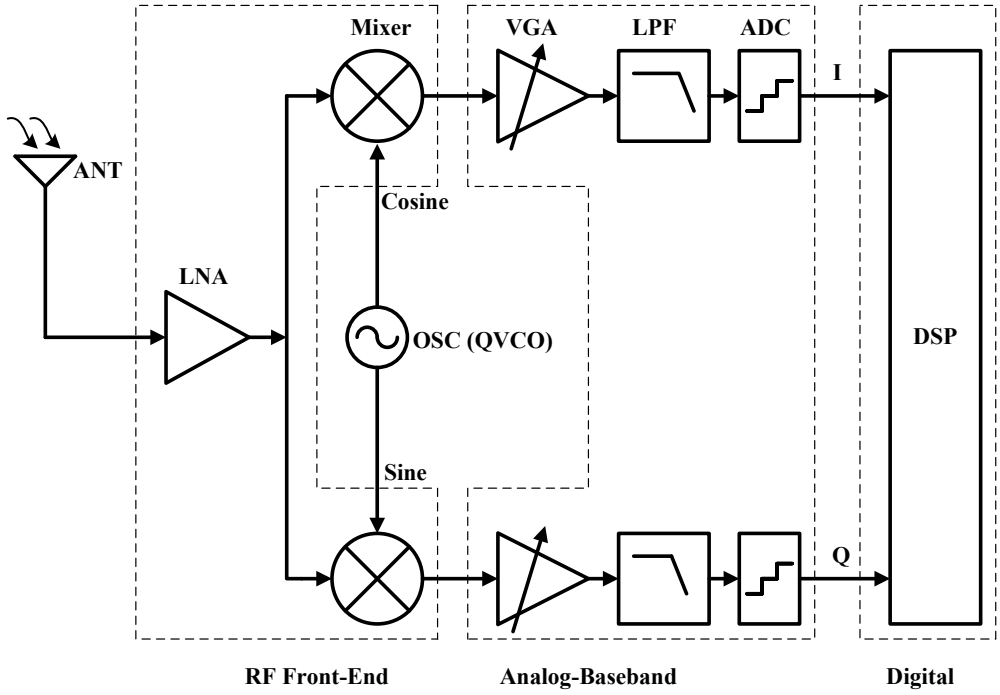


Figure 1.1: Direct conversion receiver architecture.

Figure 1.1 shows a typical RF receiver architecture, which has three main sections: an RF front-end, an analog baseband circuitry, and a digital signal processing (DSP) unit [1]. The RF front-end includes a low-noise amplifier (LNA), and a pair of mixers driven by a quadrature oscillator. Inductors are essential components in the design of LNAs, mixers and oscillators (using $LC$ resonators), and are used for impedance matching, inductive peaking, bias feeding, load tuning, signal filtering, frequency resonating, and source degeneration [2]. However, the extensive use of on-chip passive inductors make these RFICs area-inefficient, non-scalable, and incompatible with other highly-integrated analog and digital circuits (of receivers) implemented in inexpensive digital CMOS processes.

In CMOS processes, on-chip passive inductors are built on silicon substrates as planar structures of metal wires in the form of a spiral [2, 3]. They require a large chip area to obtain a high inductance value because the higher the induc-

tance, the longer the spiral. Moreover, on-chip passive inductors are typically implemented using thick metal wires and tripple-well process. These lead to the use of RF CMOS processes, which are more expensive than standard digital CMOS processes. Electrical and magnetic couplings of an on-chip passive inductor to the substrate and other nearby large structures (other inductors and circuits) also make it difficult to obtain an accurate model of the inductor. On-chip passive inductors have low quality factors and low self-resonant frequencies, which limit the performance of RFICs. The high resistivity of metal wires, and lossy silicon substrates provide a low quality factor ($Q$) [2]. The large physical size of inductors causes a low self-resonant frequency because of increased parasitic capacitances (due to close proximity of inductors to silicon substrates) that resonate with inductance at low frequency [2]. A low self-resonant frequency reduces the operating range and bandwidth of inductors. Moreover, through large physical dimensions of on-chip inductors, noise from substrates is coupled to sensitive RF circuits, and degrades their noise performance. Hence, on-chip passive inductors have a number of limitations and disadvantages. Therefore, designers are looking for alternative methods of designing inductorless RF circuits. Fortunately, inductors can be constructed with active circuits known as active inductors consisting of only transistors; the most suitably available devices in MOSFET technologies.

An active inductor is realized with a circuit configuration consisting of only a few transistors [4]. Therefore, an active inductor requires a fraction of the area of an on-chip passive inductor. The inductance of an active inductor depends on small-signal transconductances and conductances, and capacitances of transistors. These are bias dependent parameters; therefore, a high inductance can be achieved for an active inductor by suitably biasing the circuit. An active inductor exhibits no substrate and metallic or ohmic losses, and due to its small size, it also exhibits low parasitic capacitances to the substrate. Therefore, an active inductor provides a high $Q$ due to low losses, and exhibits a high self-resonant frequency due to its small size. Moreover, an active inductor can be tuned widely to vary its inductance, $Q$, and resonant-frequency by changing bias conditions. In summary, the advantages of active inductors over

passive ones are: a small chip area (or die area), a high inductance value (over 10nH) with higher self-resonance frequency, a high $Q$ factor (over 30), wide tunability, and compatibility with standard digital CMOS processes [4, 5, 6]. While active inductors have many advantages over their passive counterparts, they also have a few shortcomings. Theoretically, passive inductors do not consume DC power while active inductors require DC biasing that consumes a small amount of power. However, the power consumption of an active inductor is significantly low compared to the overall power consumption of an RF circuit, where it is intended to be used. Transistors in active inductors add an extra noise that degrades the overall noise performance of RF circuits. The inherent noise of transistors can not be eliminated completely. However, using circuit design techniques, the overall noise contribution of an active inductor to the core RF circuit can be minimized. Thus, many advantages but a few shortcomings of active inductors over passive inductors render that they are viable candidates in implementing area-efficient (occupying low-cost small die area), scalable, tunable and low-cost active (passive inductorless) CMOS RFICs for RF receiver front-ends.

## 1.2 Active CMOS MB-UWB Receiver Front-End

This thesis focuses on the design of an area-efficient active CMOS ultra-wideband (UWB) receiver front-end using active inductors instead of passive inductors in the RFICs of the front-end. UWB radio technology, using the bandwidth of 3.1-10.6 GHz, enables high data-rate (up to 480Mb/s) communications for short ranges (less than 10 meters), and sees its rapid growth and applications in multimedia-rich wireless personal area networks (WPANs) [7, 8]. Among different approaches of using the 7.5GHz UWB spectrum, the multiband (MB) system is being widely adopted to reduce the design complexity and ease the operation of UWB receivers [9]. In MB-UWB systems, the 7.5GHz spectrum is divided into fourteen bands of 528MHz each, as shown in Figure 1.2 [9]. These bands are grouped into five distinct band groups, and a MB-UWB system can operate in one or more band groups. With this re-

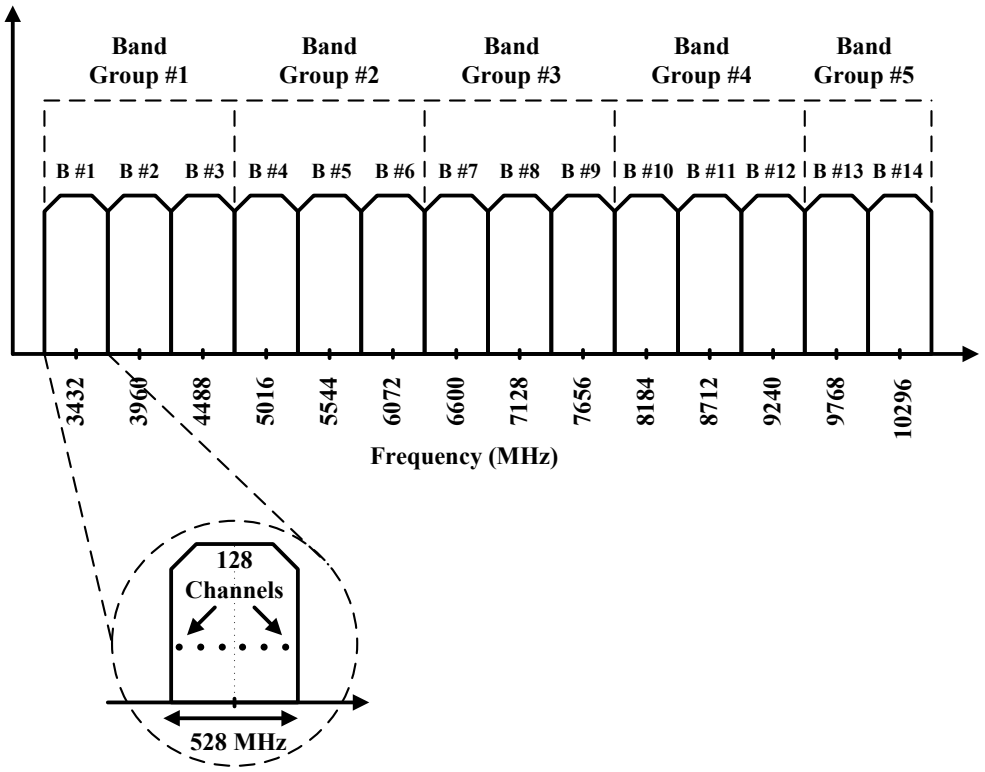


Figure 1.2: Frequency bands and band groups of MB-UWB systems.

duced operating bandwidth, MB-UWB systems still meet the minimum signal bandwidth requirement of 500MHz for UWB systems mandated by the Federal Communications Commission (FCC) [9]. Hence, instead of employing a UWB system of 7.5GHz bandwidth, MB-UWB systems of reduced bandwidth ease the design complexity of the RFICs of receiver front-ends, and overall receivers. In this thesis, an active (passive inductorless) CMOS UWB front-end operating in the range of 2.5-8.8 GHz that covers three lower band groups of MB-UWB systems (Figure 1.2) is designed.

In the design of UWB receiver front-ends, the direct-conversion architecture is typically used as shown in Figure 1.1 where the LNA is directly connected to a pair of mixers [1, 10]. A direct-conversion architecture ensures a high level of device integration and compact design for the front-end because an off-chip and

power-hungry bulk, large-size image-reject(IR) filter is not required between the LNA and mixer. In a direct conversion front-end, RF signals are directly converted into baseband signals using local oscillator (LO) signals of the same frequency of RF signals. A direct-conversion front-end also requires a simple LO scheme and consumes a small amount of DC power [10]. This thesis focuses on the design of a fully-integrated on-chip direct-conversion UWB receiver front-end.

The LNA, the first building block in a receiver front-end (Figure 1.1), amplifies RF signals received by the antenna. It needs to be designed with a high gain and a low noise figure while achieving a broadband (50Ω) input matching over the desired bandwidth. The high gain of the LNA amplifies very weak RF signals adequately and reduces the noise contribution of the subsequent stages (mixers and IF amplifiers) to the overall noise figure of the receiver. As the first circuit block in a receiver chain, the noise figure of the LNA is directly added to the system noise figure. Therefore, the LNA needs to be designed with maximum gain and minimum noise-figure. To maximize the gain and minimize the noise figure, the input impedance of the LNA should be matched to the impedance of the antenna (typically 50Ω). The design challenge for UWB LNAs is to achieve the input matching over a wide bandwidth while keeping the gain flat and high, and noise figure low. The most common approach of achieving the wideband input matching for UWB LNAs is to use higher order $LC$ filters, which require several passive inductors, and consequently, occupy a large chip area. For enhanced flat gain and extended bandwidth, inductive peakings (series, shunt or series-shunt peakings) are used in LNAs [3]. Moreover, for linearity improvement, an inductive source-degeneration (of transistors) technique is employed [3]. Thus, an LNA requires the most number of passive inductors among all of the RFICs of the front-end. In this thesis, active CMOS UWB LNAs are designed using active inductors instead of passive inductors to reduce chip area significantly while keeping gain flat for extending bandwidth. Moreover, the tunability of active inductors allows for tuning (or varying) the gain and bandwidth of the UWB LNAs over desired band group or band groups of MB-UWB systems.

The mixer, the next stage in the front-end after the LNA, switched by local oscillator (LO) signals, converts RF signals to zero intermediate-frequency (zero-IF) or baseband signals. Typically, LO signals generated from the oscillator are weak and need to be amplified by LO drivers before feeding to the mixer. In the RF front-end, the mixer generates the most of noise because of the switching of large signals (LO signals) in frequency conversion. Due to the constraint on transmitted power of UWB signals regulated by the FCC, the received UWB signals are typically very weak and may not be sufficiently amplified by the UWB LNA alone. Therefore, UWB mixers also need to be designed with a high conversion gain (RF-to-IF) and a low noise figure to reduce the noise contribution of the following stages (after the mixer) while adding a low noise to the overall receiver by itself. Like UWB LNA, the design challenge for UWB mixers is to achieve a flat conversion gain (RF-to-IF), and flat noise figure over a wide bandwidth. Note that the minimum IF bandwidth of MB-UWB systems is above 500MHz. To obtain a flat conversion gain for the wide IF bandwidth, along with a flat gain of the LNA, the frequency response (gain over frequency) of the LO driver should also be flat over the desired UWB bandwidth.

In the direct-conversion front-end of Figure 1.1, the capacitance at the node between the output of the LNA and the input of the mixer, reduces high-frequency gain due to diminishing capactive impedance, and in turn, reduces the bandwidth of the front-end. The LO driver is typically a multistage amplifier. The nodal capacitances in the multiple stages of the LO driver reduce the bandwidth significantly, yielding the reduction of high-frequency gain. Hence, the overall challenge in the design of the UWB mixer is to cancel out or minimize the effects of nodal capacitances in obtaining a flat conversion gain. This thesis focuses on the design of an active CMOS UWB mixer and an active CMOS LO driver using active inductors to cancel the effects of nodal capacitances and keep the gain flat in increasing the bandwidth. Moreover, the tunability of active inductors is exploited to tune (or vary) the overall gain-bandwidth of the front-end.

In summary, the capacitances at different nodes in RF signal paths of the

RFICs reduce the overall bandwidth of the front-end. The frequency response (gain over frequency) of the front-end rolls off fast at high frequencies due to diminishing capacitive impedances contributed by nodal capacitances. Active inductors introduced at different nodes parallel to RF signal paths can counter (compensate for) the diminishing capacitive impedances with their increasing inductive impedance. In this thesis, new CMOS tunable active inductors for UWB applications are designed. The tunability of active inductors allows for varying inductance, inductive bandwidth and $Q$ factor leading to vary the gain-bandwidth of the LNA, mixers, and the overall front-end. Overall, this thesis emphasizes developing area-efficient (occupying low-cost small die area) RFICs using active inductors for implementing a compact UWB front-end, which can be compatibly integrated with analog, mixed-signal, baseband and digital circuits on a single chip using an inexpensive standard digital CMOS process. The use of ultra-compact active inductors instead of area-inefficient (occupying high-cost large die area) passive inductors will lead to achieve very low chip-area (or low die-area) active CMOS front-ends, and consequently will reduce the cost of wireless transceiver chipsets in high volume production.

## 1.3 Thesis Organization

This thesis is organized into six chapters that include an introduction, CMOS on-chip inductors, $Q$-enhanced and bandwidth-extended tunable CMOS active inductors, CMOS UWB low-noise amplifiers, active CMOS MB-UWB receiver front-end including a UWB LNA, UWB mixers, LO drivers, and conclusion. The introductory chapter discusses the motivation and benefits of using active inductors instead of passive inductors in the design of active (passive inductorless) CMOS RFICs for RF receiver front-ends

Chapter 2 begins with an overview of applications, structures, parameters, frequency characteristics, and the advantages and disadvantages of CMOS on-chip passive inductors. This is followed by an overview of the evolution, theory of operation, design implementation, parameters and frequency characteristics of CMOS active inductors.

Chapter 3 presents two new CMOS configurations of tunable active inductors for enhanced quality factor ($Q$) and extended bandwidth. The design of these active inductors with theoretical analysis is described in detail. The implementation and measurement results of the fabricated new active inductors are presented.

Chapter 4 begins with an overview of the performance parameters of low-noise amplifiers (LNAs), and designs of CMOS UWB LNAs. Two new area-efficient tunable CMOS UWB LNAs using active inductors instead of passive inductors are presented. The LNAs are described in detail with theoretical analysis and mathematical development of their performance parameters. The design implementation, and measurement results of the fabricated UWB LNAs are presented.

Chapter 5 presents a new area-efficient, active CMOS MB-UWB receiver front-end that includes passive inductorless RFICs, namely active CMOS RFICs, a low-noise amplifier (LNA), mixers, and local oscillator (LO) drivers. Beginning with an overview of CMOS mixers and front-ends, Chapter 5 presents an active CMOS UWB mixer, and an active CMOS LO driver using very low chip-area tunable active inductors, which are used to exploit wideband active shunt peaking for bandwidth extension. Then, two identical UWB mixers, and two identical wideband LO drivers are integrated with a two-stage area-efficient CMOS UWB LNA to implement the proposed direct conversion UWB receiver front-end. Fabricated in a 90nm digital CMOS process, the measurement results of the active CMOS (passive inductorless) UWB receiver front-end are presented.

Finally, the thesis is concluded in Chapter 6. The future research toward the improvement of the noise performance and linearity of UWB receivers using active inductors is presented. The future research plan also includes the design and development of wide-tunable CMOS voltage-controlled oscillators using active inductors and covering all the bands of MB-UWB systems spreading over 3.1-10.6 GHz UWB frequency range.

# Chapter 2

# CMOS On-Chip Inductors

This chapter presents an overview of on-chip inductors in CMOS technologies. First, the structures, parameters and frequency characteristics of CMOS passive inductors are described in Section 2.1. The evolution, theory of operation, design implementation, parameters and frequency characteristics of CMOS active inductors are presented in Section 2.2.

## 2.1 CMOS On-Chip Passive Inductors

Inductors are essential components in the design of RF circuits and systems. They are used for many important applications including impedance matching, bias feeding, load tuning, signal filtering, frequency resonating and phase shifting [2, 3]. Figure 2.1 shows a CMOS ultra-wideband (UWB) low-noise amplifier (LNA) using several on-chip passive inductors. In this LNA, a third-order $LC$ network (inside the dashed box) employing three inductors ($L_1$, $L_2$ and $L_G$) along with inductor $L_S$ is used for broadband input impedance matching to maximize the amplifier's power gain and minimize its noise figure [11]. Inductors exhibit low impedance at low frequency (theoretically short at DC) but very high impedance to AC signals as inductive impedance increases with frequency. Therefore, inductors are used to feed DC bias voltages to signal paths in RF circuits while preventing RF signals to be leaked through their high impedances. In the LNA of Figure 2.1, bias voltage $V_{bias}$ is applied to the input of the LNA through inductor $L_2$. The inductive source-degeneration

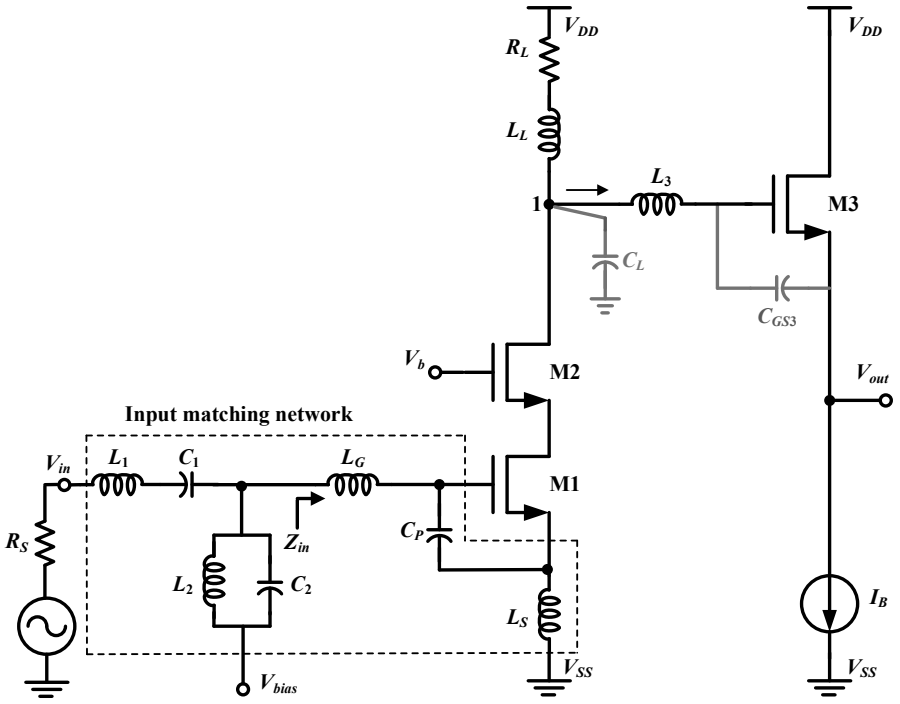


Figure 2.1: UWB LNA using on-chip passive inductors.

of transistor M1 using inductor $L_S$ increases the linearity of the LNA by exploiting negative feedback [3]. Inductive peaking, achieved by shunt and series inductors $L_L$ and $L_3$, respectively is used in the LNA to enhance its gain and extend bandwidth [3]. With shunt peaking, inductor $L_L$ parallel to the output RF signal path (shown by arrow) compensates for the effect of total nodal capacitance $C_L$ (shaded) at Node 1, and increases the high-frequency gain of the amplifier. With series peaking, inductor $L_3$ in series with the output signal path, cancels the effect of input capacitance $C_{GS3}$ (gate-source capacitance of transistor M3) of the next-stage output buffer of the LNA, and keeps the frequency response (gain over frequency) of the amplifier flat at high frequency. Thus, inductive peaking increases the bandwidth of amplifiers by increasing high-frequency gain, and by keeping frequency response flat up to a very high frequency.

Inductors are widely used in the design of $LC$ filters (or resonators). A

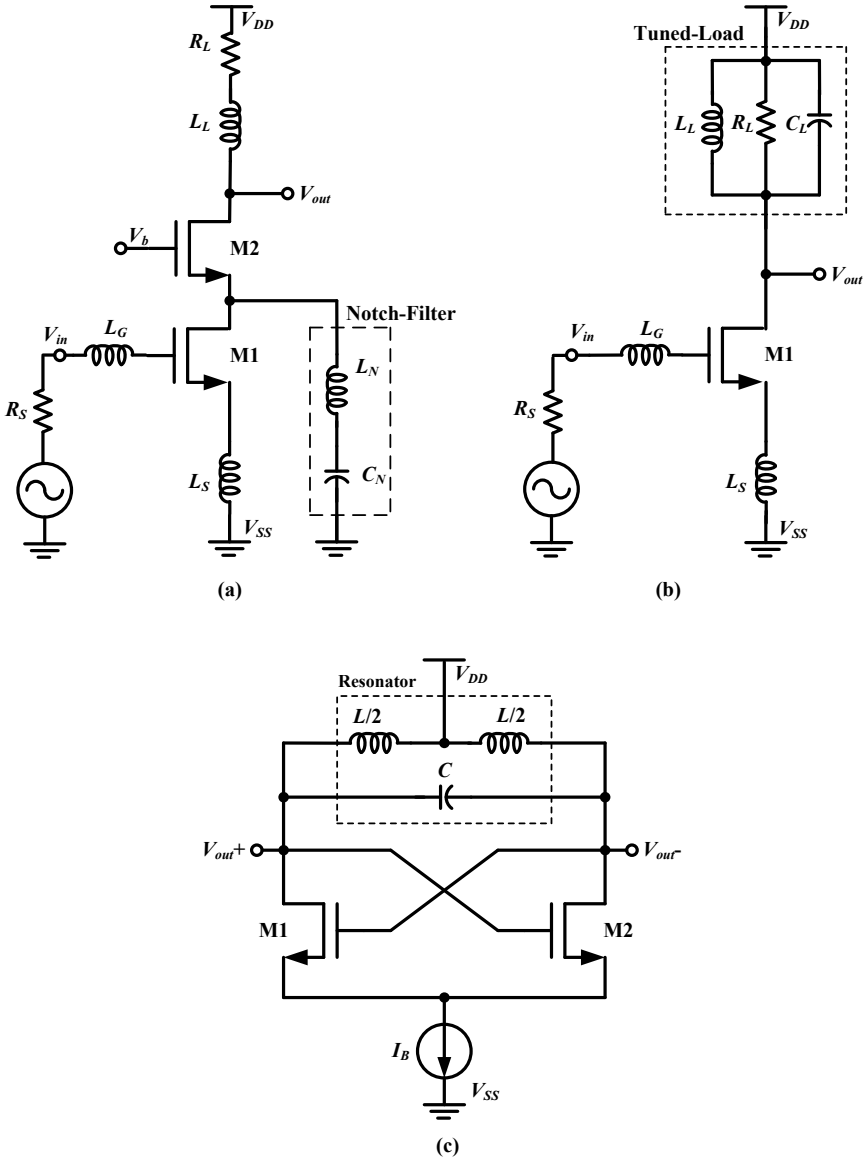


Figure 2.2: (a) Series resonator as the notch filter in amplifier, (b) parallel resonator as the tuned load in amplifier, (c) oscillator using $LC$ resonator.

series $LC$ resonator provides the minimum resistance at resonance frequency, and filters out undesired signals. Thus, a series resonator tapped at the RF signal path of the amplifier, is used as the notch-filter as shown in Figure 2.2(a). On the other hand, a shunt $LC$ resonator exhibits the maximum

resistance at resonance-frequency, and is used as the tuned load at the desired frequency as shown in Figure 2.2(b) [3]. An $LC$ resonator also determines the frequency of oscillation ($f_{osc} = 1/\sqrt{LC}$) of an oscillator as shown in Figure 2.2(c) [2]. Thus, passive inductors are widely and essentially used in the design of radio-frequency integrated circuits (RFICs).

### 2.1.1 Structures of On-Chip Passive Inductors

In CMOS process technologies, metal wires in the form of a spiral are laid on the plane of a silicon substrate to form an inductor. Figure 2.3(a) shows the top view of a planar square-spiral inductor. Planar structures for inductors are widely used because of the availability of compatible design tools, and the ease of modeling and fabrication. The inductance of a spiral inductor depends on the number of turns in the spiral, the inner and outer diameters ($d_{in}$ and $d_{out}$) of the spiral, the metal width ($W$), and the spacing ($S$) between the adjacent metal traces [2, 3]. The important design consideration for on-chip passive inductors is the occupied chip-area. The higher the inductance required, the larger the area of an inductor becomes because inductance increases with the length of the spiral. Besides inductance ($L_s$), the important design parameters of inductors are quality factor ($Q$) and self-resonant frequency ($f_{sr}$) [2, 3]. To achieve a high $L_s$, a high $Q$ and a high $f_{sr}$ for on-chip inductors, many shapes and structures such as circular, hexagonal, octagonal, multilayered stacked-metal and miniature 3-D inductors have been proposed using specialized CMOS process technologies (RF CMOS processes)[12, 13]. However, on-chip inductors rarely scale down (or do not shrink) whether using improved structures or deep sub-micron advanced CMOS technologies. Figure 2.3(b) shows the 3D cross-section view of the square-spiral inductor of Figure 2.3(a) exhibiting magnetic field, current, and passive elements (inductance, resistance and capacitance).

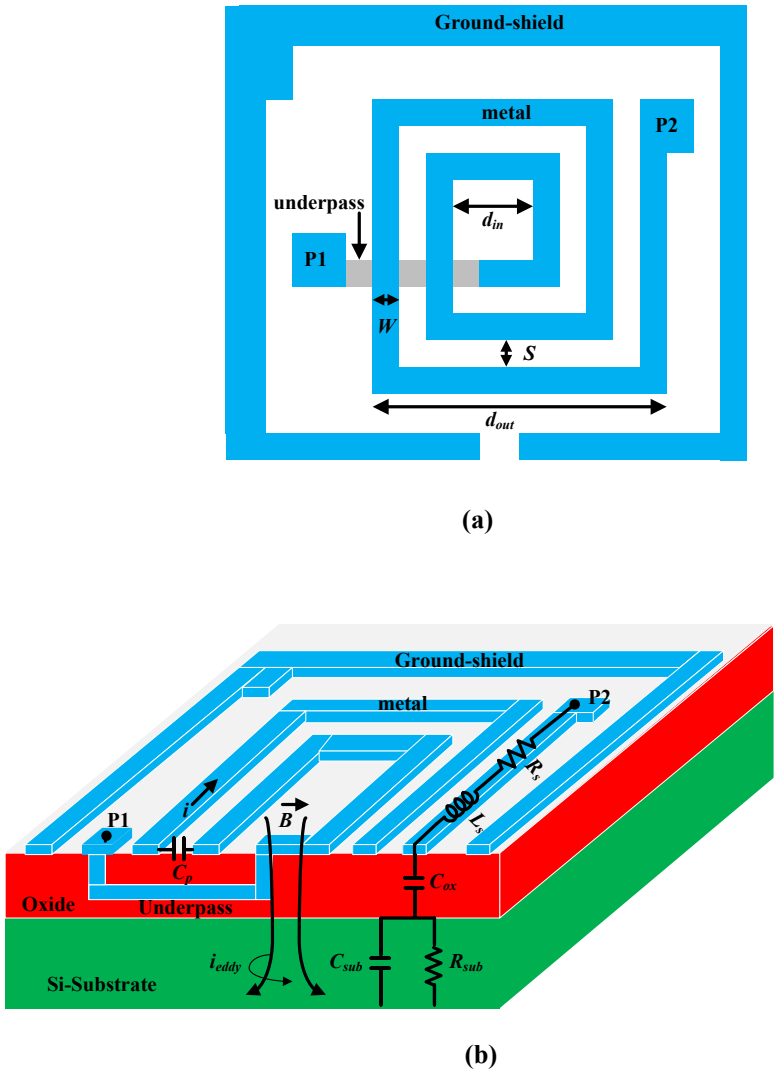


Figure 2.3: (a) Top view of square spiral inductor, (b) 3-D cross-section view of spiral inductor.

### 2.1.2 Lumped-Element Model of On-Chip Passive Inductors

Describing an on-chip passive inductor employed in an RF circuit, it is useful to model the structure of the inductor of Figure 2.3 with an equivalent circuit. The presence of magnetic and electric fields in the inductor, and their couplings to the nearby substrate, generate parasitic elements (resistance $R_{sub}$,

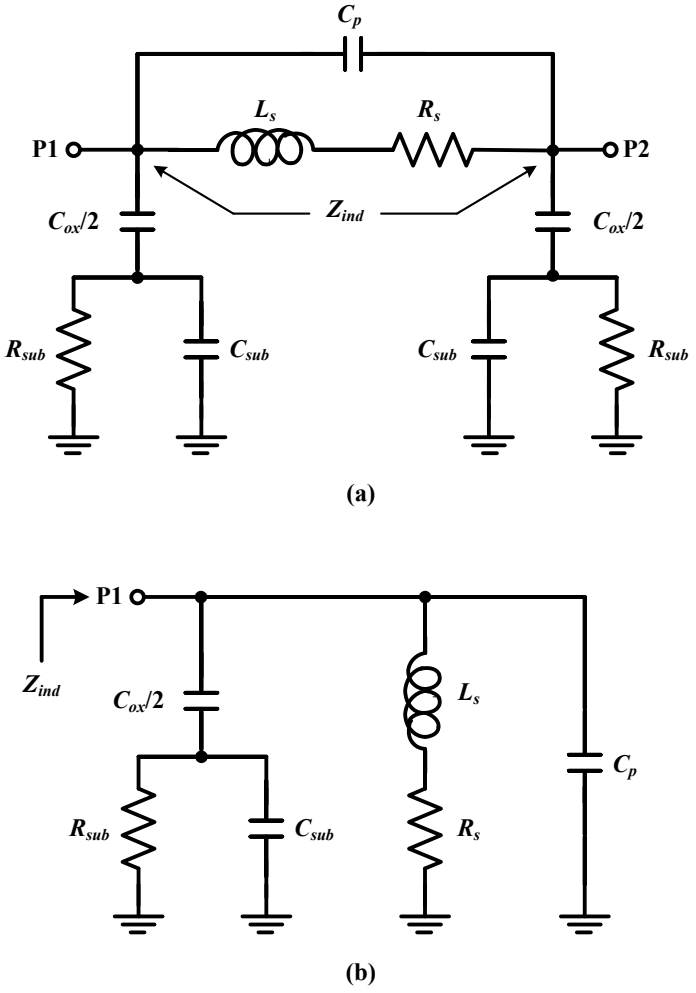


Figure 2.4: (a) Double-ended on-chip passive inductor's model ($\pi$-mode), (b) single-ended on-chip passive inductor's model (reproduced from [2]).

and capacitances, $C_{ox}$, $C_{sub}$) as shown in Figure 2.3(b). Many of such elements distributed all over the inductor's structure result in a complex circuit model. Figure 2.4(a) shows a basic lumped-element equivalent circuit model called the pi-model ($\pi$-model) of the square-spiral inductor derived from the elements as shown in Figure 2.3(b)[2]. In this equivalent circuit, $L_s$ represents the total inductance of the inductor between ports P1 and P2, $R_s$ is the total resistance of metal lines in series with $L_s$, $C_p$ is the total capacitance between

adjacent parallel lines of the spiral, $C_{ox}$ is the capacitance formed between metal lines and the substrate through the oxide. Elements $C_{sub}$ and $R_{sub}$ are the capacitance and resistance (or conductance) of the substrate respectively due to electromagnetic effects, and represents the total substrate losses. The $\pi$-model in Figure 2.4(a) exhibits inductive impedance $Z_{ind}$ between two ports (P1 and P2) of a double-ended inductor. For a single-ended inductor or one-port grounded (port P2 is grounded) inductor, the simplified model is shown in Figure 2.4(b), which is a parallel $RLC$ circuit. From the lumped elements of an on-chip inductor model, parameters $Q$ and $f_{sr}$ are derived.

### 2.1.3 Parameters of On-Chip Passive Inductors

Inductors are characterized by quality factor $Q$ and self-resonant frequency $f_{sr}$. The parameter $Q$ determines losses in an inductor, and the $f_{sr}$ determines its impedance characteristics (inductive or capactive) over frequency [2]. The impedance of an inductor becomes capacitive when the operating frequency exceeds $f_{sr}$. The factors that are involved in determining the $Q$ and $f_{sr}$ of an inductor are: the physical size (small or large) and shape (square, circular, hexagonal or octagonal), the conductivity of the metal wire (copper or aluminum), the resistivity of the silicon substrate, and the proximity of the inductor to the substrate. When energized, the presence of magnetic ($B$) and electrical fields causes losses in an inductor. The physical losses in an on-chip inductor can be determined from the following definition of $Q$ [14].

$$Q = 2\pi \frac{Peak\ magnetic\ energy}{Energy\ loss\ in\ one\ oscillation\ cycle}. \tag{2.1}$$

Note that electrical energy and electrical loss are counter productive to magnetic energy, and hence, these two need to be minimized to maximize $Q$. As shown in Figure 2.3(b), current $i$ in the metal wire causes ohmic losses (electrical losses) due to the resistivity of the metal wire. The magnetic field $B$ generated by current $i$ in the metal wire induces eddy current ($i_{eddy}$) in the substrate and causes eddy-current losses. The electric field created by current $i$ in the metal wire makes capacitive-coupling between the metal wire and the

substrate through dielectric material (insulating material). Thus, magnetic and electric fields in the inductor create parasitic effects and introduce parasitic resistances ($R_{sub}$) and capacitances ($C_{sub}$) to the substrate as shown in Figure 2.3. In the substrate, resistances cause ohmic losses and capacitances store electrical energy. Both of them are counter productive to magnetic energy, and together, they are called substrate losses. In summary, losses in an inductor can be grouped as ohmic (losses due to the resistivity of the metal wire) and substrate losses (due to parasitic elements of the substrate). At low frequencies, ohmic losses limit $Q$ and at high frequencies, substrate losses limit $Q$. Moreover, due to the skin-effect, the resistance of the metal wire increases at high frequencies, and this further reduces the $Q$ of an inductor[2]. For circuit analysis, $Q$ is defined with a simple expression as [2]

$$Q = \frac{Img(Z_{ind})}{Real(Z_{ind})} = \frac{\omega L_s}{R_s}, \tag{2.2}$$

where $Z_{ind}$ is the impedance of the inductor consisting of $L_s$ in series with $R_s$ (Figure 2.4) and $\omega$ is the angular frequency in rad/sec. Note that $R_s$ representing ohmic losses needs to be reduced to have a high $Q$.

Parasitic capacitances ($C_p$, $C_{sub}$, $C_{ox}/2$) resonate with the inductance of the inductor at $f_{sr}$, which decreases with the increased size of the inductor that contribute increased parasitic capacitances. Before $f_{sr}$, the inductive impedance of the inductance dominates the capacitive impedance of the parasitic capacitances, and the overall impedance of the inductor becomes inductive. At $f_{sr}$, the impedance of the inductor becomes pure resistive, and $Q$ becomes zero. After $f_{sr}$, the impedance of the parasitic capacitances dominate the impedance of the inductance, and the overall impedance of the inductor becomes capacitive. Thus, a high self-resonant frequency increases the inductive operating range or bandwidth of inductors. The close proximity of the large structure of an inductor to the substrate, contributing more parasitic capacitances, reduces $f_{sr}$ [2]. Therefore, in CMOS processes, passive inductors are constructed using the top-level metal layer of multilevel layers, which are placed one above other on the silicon substrate. The increased distance

between the top metal layer and the silicon substrate contributes less parasitic capacitances.

### 2.1.4 Frequency Characteristics of On-Chip Passive Inductors

The lumped-element model of an on-chip passive inductor indicates that inductance $L_s$ and quality factor $Q$ are frequency-dependent parameters [2]. Typical simulation and measurement tools for inductors can provide inductive impedance, $Z_{ind}$ and its imaginary part $\mathrm{Im}(Z_{ind})$ and real part $\mathrm{Re}(Z_{ind})$ over frequency. Note that $\mathrm{Im}(Z_{ind})$ is pure reactive ($=X_L$), and $\mathrm{Re}(Z_{ind})$ is pure resistive ($=R$). Hence, $L_s$ and $Q$ are determined as

$$L_s = \frac{Im(Z_{ind})}{\omega} = \frac{X_L}{\omega} = \frac{X_L}{2\pi f}, \tag{2.3}$$

and

$$Q = \frac{Im(Z_{ind})}{Re(Z_{ind})} = \frac{X_L}{R}, \tag{2.4}$$

where $\omega$ ($=2\pi f$) is the angular frequency in rad/s and $f$ is the frequency in Hz.

Figure 2.5 shows the simulated frequency characteristics of $Z_{ind}$, $\mathrm{Im}(Z_{ind})$, $\mathrm{Re}(Z_{ind})$ and $\mathrm{Phase}(Z_{ind})$ of a 5.0nH single-ended CMOS passive inductor whose physical dimensions are: metal width ($W$) of 15$\mu$m, number of turns ($n$) of 4.5, metal spacing ($S$) of 3$\mu$m, inner diameter ($d_{in}$) of 60$\mu$m, outer diameter of 285$\mu$m, and the occupied area of 285$\mu$m $\times$ 285$\mu$m. $Z_{ind}$ is the magnitude of the inductive impedance of the inductor. The resonant peaks of $Z_{ind}$ and $\mathrm{Re}(Z_{ind})$ occur at 9.6GHz, which is the resonance frequency ($f_{sr}$) or zero-crossing frequency ($f_0$) of $\mathrm{Im}(Z_{ind})$. $Z_{ind}$ and $\mathrm{Im}(Z_{ind})$ increase with frequency starting from low frequency but $\mathrm{Re}(Z_{ind})$ remains constant up to 5.6GHz. At $f_{sr}$ ( or $f_0$), $\mathrm{Im}(Z_{ind})$ is zero but $Z_{ind}$ is purely resistive with maximum $\mathrm{Re}(Z_{ind})$. After $f_{sr}$, $\mathrm{Im}(Z_{ind})$ becomes negative, and the magnitude of $Z_{ind}$ decreases with the decreasing of $\mathrm{Im}(Z_{ind})$. The phase angle of $Z_{ind}$, $\mathrm{Phase}(Z_{ind})$ is positive before $f_{sr}$ indicating the inductive impedance region.

Figure 2.6 shows the frequency characteristics of inductances $L_s$ and $Q$ of

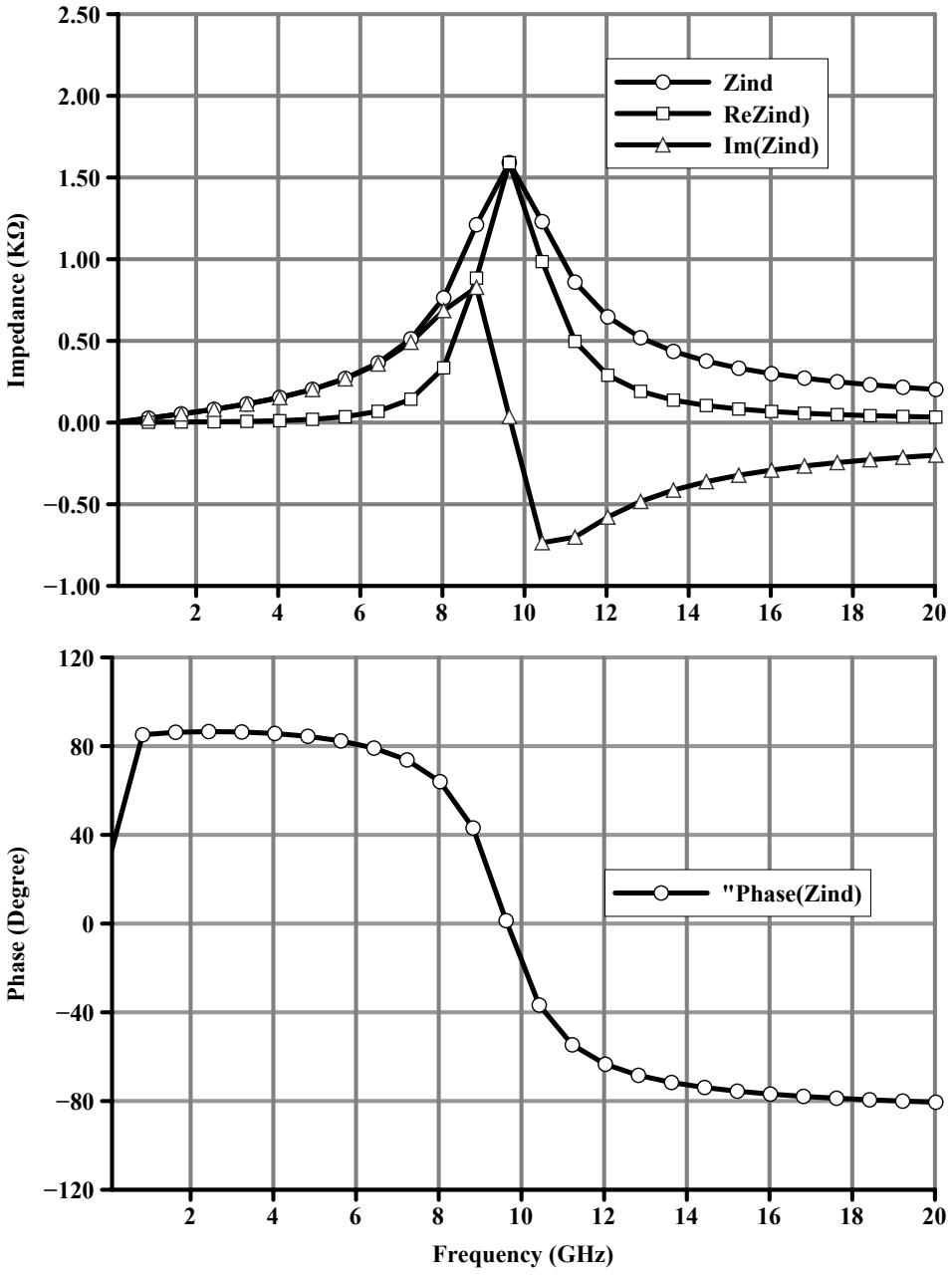


Figure 2.5: Impedances and phase of 5nH CMOS passive inductor over frequency.

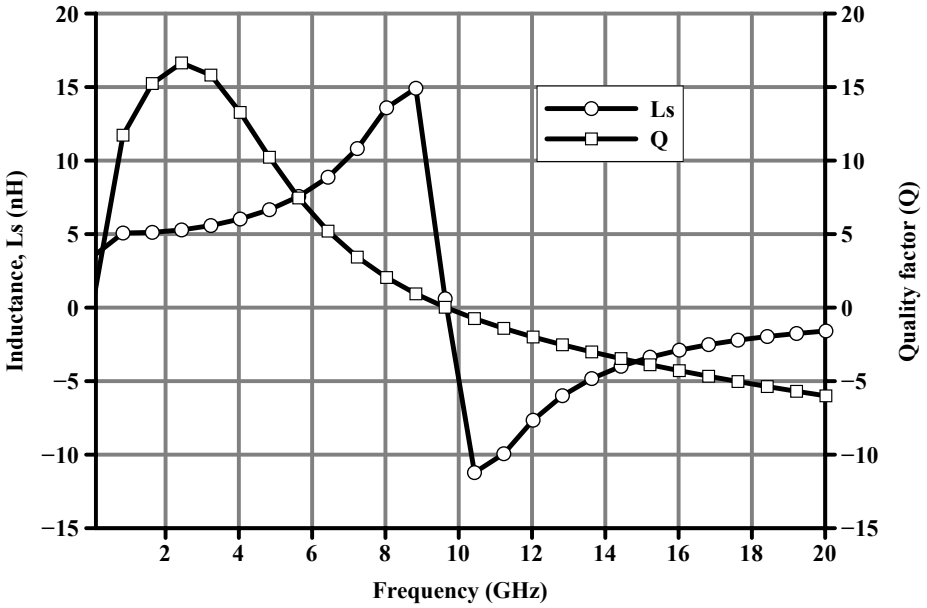


Figure 2.6: Inductance and $Q$ of 5nH CMOS passive inductor over frequency.

the 5.0nH single-ended passive inductor. $L_s$ exhibits 5.0nH over DC-to-3.0GHz range, and the maximum $Q$ of 17.0 is obtained at 2.8GHz. At $f_{sr}$ both $Q$ and $L_s$ are zero, and after $f_{sr}$, $L_s$ becomes negative and decreasing with frequency. This also indicates the capacitive characteristic of the inductor after $f_{sr}$.

Figure 2.7 shows the frequency characteristics a 5.0nH and a 1.75nH inductors with different physical dimensions. With wide metal width ($W$=15$\mu$m) and 4.5 turns of the spiral, the 5.0nH (≈5.1nH) inductor occupies a chip area of 285$\mu$m × 285$\mu$m and exhibits $f_{sr}$ of 9.6GHz. With narrow metal width ($W$=6$\mu$m) and 4.5 turns of the spiral, the 5.0nH (≈5.0nH) inductor occupies an area of 200$\mu$m × 200$\mu$m and exhibits an $f_{sr}$ of 14.0GHz. On the other hand, the small-structure 1.74nH inductor with wide metal width ($W$=15$\mu$m) and 2.5 turns of the spiral exhibits an $f_{sr}$ of 22.7GHz. Hence, with increased metal width, and increased spiral length (increasing number of turn), parasitic capacitances increase significantly, and $f_{sr}$ decreases drastically. It is also evident that even for the same inductance value of 5.0nH, the inductor with wide metal width (15$\mu$m) has an $f_{sr}$ of 9.6GHz, which is far below the $f_{sr}$

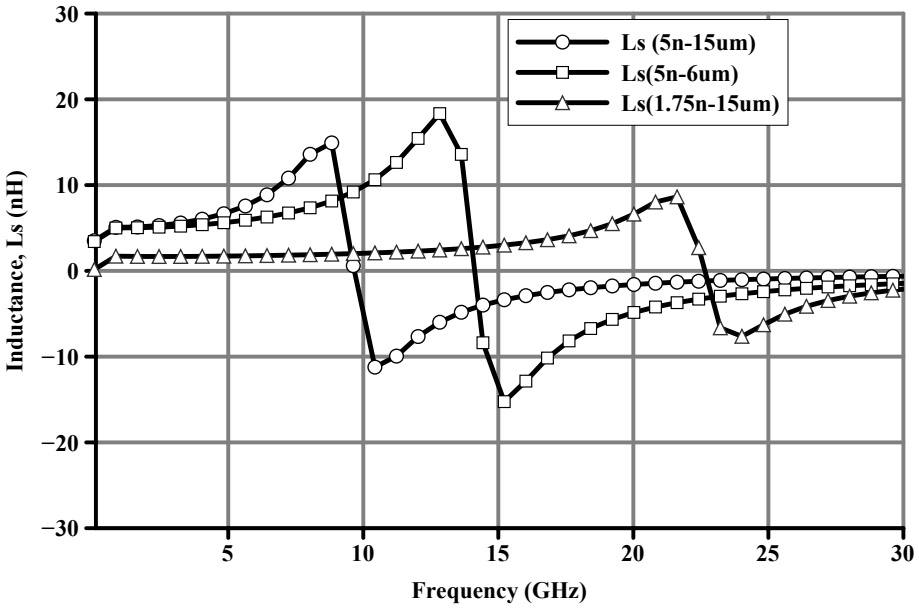


Figure 2.7: Inductances of 5nH and 1.75nH CMOS passive inductors over frequency.

(14.0GHz) of the narrow metal width (6$\mu$m) inductor. Note that large-width inductors are required in RFICs to carry a large amount of DC current.

### 2.1.5 Advantages and Disadvantages of Passive Inductors

Theoretically, passive inductors do not consume power assuming a negligible resistance of metal wires. Thus, in low-power design environments, a high DC voltage headroom is available for output signals with inductive loads that lead to increased linearity. Because of negligible resistance, passive inductors are not considered significant sources of noise in RF circuits.

The main drawback of using on-chip passive inductors is their large chip areas as long traces of wide metal wires are used in their structures. Physical sizes of inductors increase with increased inductances, and increased current-carrying capabilities. High inductances with large structures (long spirals and wide metal widths) reduce both $Q$ and resonance frequency of inductors. Long spiral wires increase losses (ohmic and substrate losses), and in turn, decrease

$Q$. Increased parasitic capacitances of large-structure inductors decrease resonance frequency, and in turn, limit operating bandwidths of inductors. Moreover, due to the fixed structures, passive inductors can not be tuned with varying values of inductance and $Q$.

To prevent magnetic coupling between an inductor and the nearby large structures such as other inductors and circuits, it needs to be isolated from them with a large physical spacing. Hence, for improved performance, on-chip passive inductors require an additional chip area. Through large structures of on-chip passive inductors, noise from the substrate is coupled to RF circuits and degrades the noise performance of sensitive RF circuits. To reduce substrate noise-coupling, the additional protection schemes (ground-shields and metal-shields) are used for on-chip inductors. These require additional processing and masking steps that lead to the use of specialized CMOS fabrication processes, namely RF CMOS processes. Hence, many of these disadvantages of on-chip passive inductors have led to the use of on-chip active inductors in the design of RF and microwave integrated circuits.

## 2.2 CMOS On-Chip Active Inductors

### 2.2.1 Evolution of Active Inductors

Active inductors evolved in the mid 60's when intensive efforts were going on to realize inductorless filters or active filters [15]. However, a number of development of electric circuits and theories during the late 40's to mid 50's led to the concept of active inductors. In 1948, the new electric network element, namely the gyrator, a positive impedance inverter, was created [16]. Subsequently, from the mid 50's to mid 60's, the development of gyrator-based impedance inverter circuits, and the realization of transistor gyrators and gyrators with operational amplifiers, advanced the development of active inductors. Another concept of active inductors originated from the theory of the negative impedance converter in the early 50's followed by the subsequent development of $RC$ active filters in the mid 50's [17, 18]. The core of the negative impedance converter is an operational amplifier that converts a

capacitance into a negative capacitance, which provides inductive impedance.

In the late 60's, gyrator-based active filters were being popularly developed for microwave and ultra high-frequency (UHF) applications [19]. The gyrator is a two-port network and transforms a load impedance into an input impedance, which is proportional to the inverse of the load impedance. Thus, the gyrator loaded with a capacitance provided a virtual inductance. Depending on the applications, the development of active inductors continued using both gyrators and operational amplifiers. From the early 80's to late 80's, monolithic microwave integrated circuit (MMIC) active inductors for GHz-range operation were developed using GaAs technology. In 1988, a fully integrated broadband MMIC active inductor operating over 5.0GHz was reported [20]. From the early to the mid 90's, submicron CMOS technologies have boosted the development of gyrator-based CMOS active inductors for high-frequency applications. In 1990, a fully-integrated CMOS active filter based on gyrator was reported in the literature [21]. Today, CMOS active inductors are being considered and developed for designing area-efficient RF and microwave integrated circuits.

### 2.2.2 Theory of Active Inductors

Active inductors are realized using a well-known gyrator-capacitor (gyrator-$C$) configuration. Figure 2.8(a) shows a gyrator, which is a two-port network and consists of two transconductors (voltage-to-current converters) ($G_{m1}$ and $G_{m2}$) connected back-to-back in a feedback configuration [21]. A load impedance connected at node 2 is transformed into an input impedance at node 1, which is inverse to the load impedance. Figure 2.8(b) shows the gyrator loaded with a capacitor $C$. The transconductors provide currents $i_1$ and $i_2$ from their respective input voltages of $V_{in}$ (=$V_1$) and $V_2$). Hence, input impedance $Z_{in}$ is calculated as

$$Z_{in}(s) = \frac{sC}{G_{m1}G_{m2}} = sL_s. \tag{2.5}$$

Thus, inductance ($L_s$) is obtained as

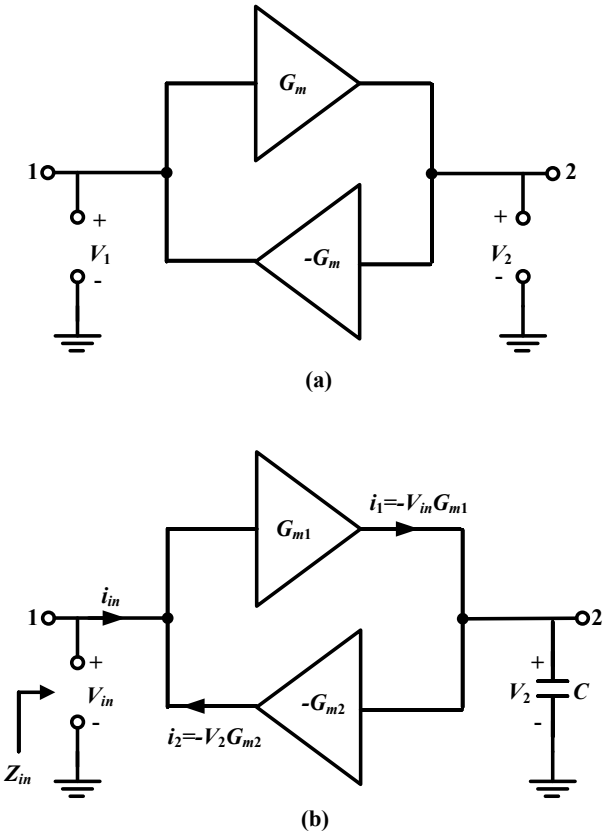


Figure 2.8: (a) Two-port gyrator network, (b) gyrator-$C$ configuration.

$$L_s = \frac{C}{G_{m1}G_{m2}}. \tag{2.6}$$

Note that $Z_{in}$ is inductive impedance and $L_s$ is the inductance. Hence, a capacitance $C$ at the output has been gyrated into an inductance $L_s$ at the input. Here, the gyrator-$C$ inductor is a one-port grounded active-inductor because $Z_{in}$ is defined with respect to ground. For gyrator-$C$ active inductors, transconductors with opposite signs can be realized with transistors or amplifiers. For a MOSFET transistor, its transconductance is defined as the ratio of the change of its drain (or source) current to the change of its input voltage at a constant DC voltage level (DC bias voltage) [22]. Thus, transcon-

ductance $G_{m1}$ and $G_{m2}$ can be realized with a single-transistor amplifier of common-source or common-gate or common-drain configuration [22].

### 2.2.3 CMOS Implementation of Active Inductors

Using two single-transistor amplifiers of common-source and common-drain configurations, the implemented CMOS active inductor is shown in Figure 2.9(a), which is known as the Generalized Impedance Converter (GIC) [23]. Transistors M1 and M2 form two back-to-back connected transconductors of $g_{m1}$ and $g_{m2}$ respectively, and gate-source capacitance, $C_{gs2}$ of transistor M2 is the capacitance that transformed into an inductance. Here, the GIC resembles the gyrator-$C$ configuration of Figure 2.8(b) except that capacitance $C_{gs2}$ is connected between two ports of the gyrator instead of its one port to be grounded. Gate-source capacitance $C_{gs1}$ of M1 comes in parallel with inductance. Using transistor models that take into account gate-source capacitance $C_{gs}$, gate-drain capacitance $C_{gd}$, transconductance $g_m$ and output conductance $g_{ds}$, the simplified small-signal model of the CMOS active is shown in Figure 2.9(b). Here, input impedance $Z_{in}$ or admittance $Y_{in}(=1/Z_{in})$ of the active inductor as shown in Figure 2.9(b) can be expressed as

$$Y_{in}(s) = sC_{gs1} + g_{ds2} + \frac{(g_{ds1} + g_{m1} + sC_{gd2})[g_{m2} + s(C_{gs2} + C_{gd1})]}{g_{ds1} + s(C_{gs2} + C_{gd1} + C_{gd2})}. \quad (2.7)$$

At very low frequency (LF) and very high frequency (HF), $Z_{in}$ can be approximated as follows:

$$Z_{in,LF}(s) \approx \frac{g_{ds1}}{g_{m1}(g_{ds1} + g_{m1})}. \quad (2.8)$$

$$Z_{in,HF}(s) \approx \frac{C_{gs2} + C_{gd1} + C_{gd2}}{C_{gd2}(C_{gs2} + C_{gd1})}. \quad (2.9)$$

Note that $Z_{in}$ is resistive at LF but capacitive at HF. Over the mid-

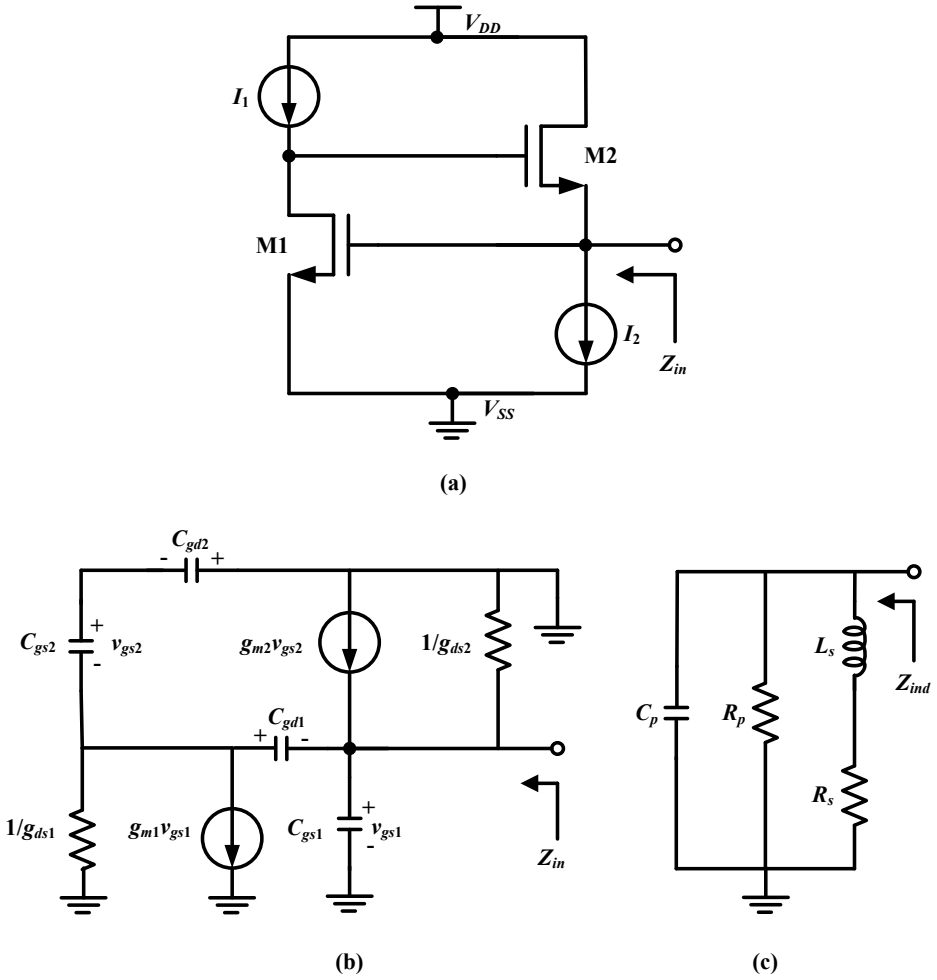


Figure 2.9: (a) CMOS GIC active inductor (reproduced from [23]), (b) small-signal equivalent model of active inductor, (c) equivalent $RLC$ circuit of inductive impedance, $Z_{ind}$.

frequency (MF) range, $Z_{in}$ is inductive and can be expressed as

$$Z_{in,ind}(s) = \frac{g_{ds1} + s(C_{gs2} + C_{gd1} + C_{gd2})}{(g_{ds1} + g_{m1} + sC_{gd2})[g_{m2} + s(C_{gs2} + C_{gd1})]}. \tag{2.10}$$

Note that, inductive impedance $Z_{in,ind}$ is a second-order transfer function, and can be modeled with an equivalent $RLC$ circuit of Figure 2.9(c), where $L_s$

represents the inductance of the active inductor, $R_s$ is the resistance in series with $L_s$, $C_p$ is the parallel capacitance and $R_p$ is the parallel resistance. These elements are derived as follows:

$$L_s = \frac{C_{gs2}}{g_{m1}g_{m2}}. \tag{2.11}$$

$$R_s = \frac{g_{ds1}}{g_{m1}g_{m2}}. \tag{2.12}$$

$$C_p = C_{gs1}. \tag{2.13}$$

$$R_p = \frac{1}{g_{m2}}. \tag{2.14}$$

The parameters of the active inductor, $Q$ and resonance frequency ($\omega_0$ rad/s) are derived using the elements of the $RLC$ model as

$$\omega_0^2 = \frac{1}{L_s C_p} = \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}, \tag{2.15}$$

and

$$Q = \omega_0 \frac{L_s}{R_s} = \omega_0 \frac{C_{gs2}}{g_{ds1}}. \tag{2.16}$$

In deriving $Q$, the effects of $C_p$ and $R_p$ are neglected. Note that in the active inductor of Figure 2.9, the output conductance $g_{ds1}$ of transistor M1 limits $Q$. With a high $g_{ds1}$, series resistance $R_s$ increases, which in turn increases losses in the inductor and decreases $Q$. The low output resistance ($r_{ds1}$) or high conductance ($g_{ds1}$) provides a low gain for the common-source amplifier (consisting of transistor M1 and current-source $I_1$). The low gain ($g_{m1}r_{ds1}$ or $g_{m1}/g_{ds1}$) reduces the amount of negative feedback at the input of the active inductor (Figure 2.9) and reduces the inductive operating bandwidth. Note that in the expression of inductive impedance $Z_{in,ind}$ (Equation 2.10), there are two poles ($\omega_{p1}$ and $\omega_{p2}$) and one zero ($\omega_z$). The inductive operating bandwidth is limited within the range starting from zero ($\omega_z$) at $g_{ds1}/(C_{gs2} + C_{gd1} + C_{gd2})$ to the dominant pole ($\omega_{p1}$) at $g_{m2}/(C_{gs2} + C_{gd1})$. The upper limit of

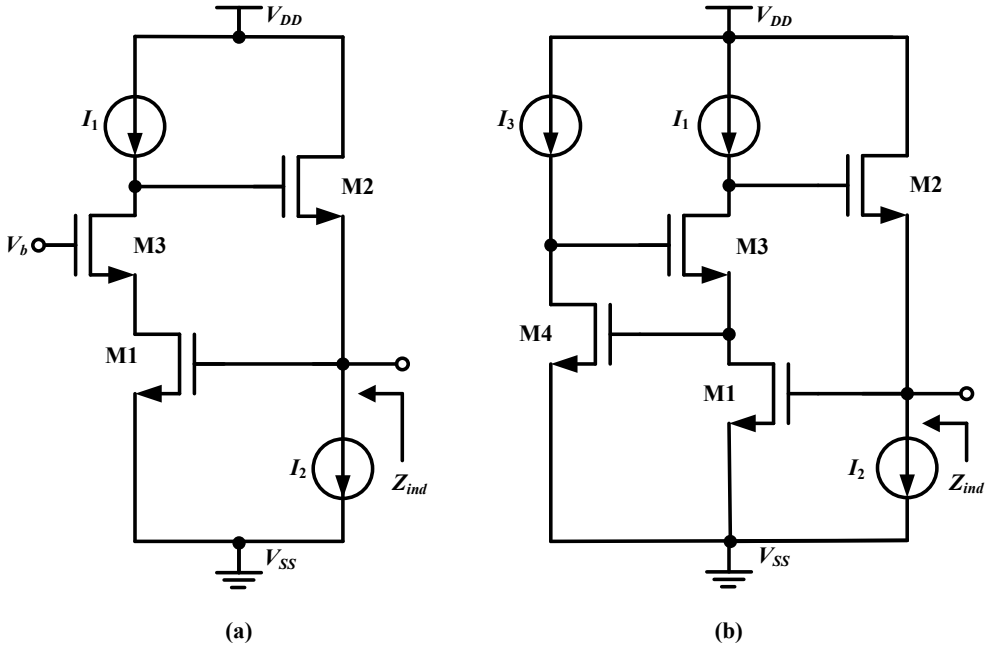


Figure 2.10: (a) Cascode active inductors, (b) regulated cascode inductors. (reproduced from [4])

inductance operating bandwidth reaches the unity-gain-cut-off frequency ($f_t$) of transistor M2 ($f_t \cong \frac{g_{m2}}{C_{gs2}}$) but the lower end of the bandwidth is limited by zero $\omega_z$, which depends on $g_{ds1}$. Thus, a low output resistance ($r_{ds1}$) or a high conductance ($g_{ds1}$) of transistor M1 reduces both $Q$ and the inductance operating bandwidth.

To improve $Q$ and widen inductive operating range, the modified cascode active inductor is proposed as shown in Figure 2.10(a) [4], where cascode transistor M3 sits on transistor M1 of the GIC (Figure 2.9). The cascode transistor M3 reduces the conductance or increases the output resistance of M1, and in turn, increases the gain of the cascode amplifier. Note the increased output resistance of transistor M1 and the increased gain of the cascode amplifier are $g_{m3}r_{ds1}r_{ds2}$ and $g_{m1}g_{m3}r_{ds1}r_{ds2}$, respectively. Like GIC, the inductive impedance of cascode active inductor is also modelled by an $RLC$ circuit and its elements are derived as follows:

$$L_s = \frac{C_{gs2}}{g_{m1}g_{m2}}. \tag{2.17}$$

$$R_s = \frac{g_{ds1}g_{ds3}}{g_{m1}g_{m2}g_{m3}}. \tag{2.18}$$

$$R_p = \frac{1}{g_{m2}}. \tag{2.19}$$

$$C_p = C_{gs1}. \tag{2.20}$$

Neglecting the effect of $R_p$, the $Q$ and $\omega_o$ of the cascode active inductor are expressed as follows:

$$Q = \omega_0 \frac{L_s}{R_s} = \omega_0 \frac{C_{gs2}g_{m3}}{g_{ds1}g_{ds3}}. \tag{2.21}$$

$$\omega_0^2 = \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}, \tag{2.22}$$

Note that, reduced $R_s$ due to the increased output resistance and the enhanced gain of the cascode amplifier (M1, M3 and $I_1$) increases $Q$. In other words, the increased gain of the cascode stage reduces losses in the inductor leading to a high $Q$. To further increase the gain of the cascode stage, the cascode transistor M3 is regulated by a feedback amplifier (common-source amplifier) consisting of transistor M4 and current-source $I_3$ as shown in Figure 2.10(b), which is called the regulated cascode configuration [4]. The feedback amplifer does not affect the inductive bandwidth and the operation of the core cascode inductor because it is not located in the main signal path (via transistors M1, M3 and M2).

The inductance ($L_s$), quality factor ($Q$) and resonance frequency $\omega_0$ of CMOS active inductors (Figures 2.9 and 2.10) depend on small-signal and device parameters: transconductance $g_m$, output conductance $g_{ds}$, gate-source capacitance $C_{gs}$, and gate-drain capacitance $C_{gd}$. These parameters are bias-dependent parameters and vary with the changing biasing conditions of induc-

tor circuits. Thus, active inductors become tunable with varying values for $L_s$, $Q$ and $\omega_0$. Hence, by controlling current sources ($I_1$, $I_2$ and $I_3$) with external voltages, CMOS active inductors of Figures 2.9 and 2.10 can be tuned.

### 2.2.4 Frequency Characteristics of CMOS Active Inductors

Note that the expressions of $L_s$, $Q$ and $\omega_0$ of CMOS active inductors (Figures 2.9 and 2.10) contain capacitances ($C_{gs}$ and $C_{gd}$) whose impedances are frequency dependent. Therefore, like on-chip passive inductors, the parameters of active inductors also depend on operating frequencies. The cascode active inductor in Figure 2.10(a) is simulated in a deep submicron CMOS process (STMicroelectronics 90nm CMOS process). Figure 2.11 shows the frequency responses of $Z_{ind}$, Re($Z_{ind}$) (real or resistive part), Im($Z_{ind}$) (imaginary or reactive part) and Phase($Z_{ind}$) (Phase angle) of the cascode active inductor. Like CMOS passive inductors, $Z_{ind}$ and Im($Z_{ind}$) increases with frequency while Re($Z_{ind}$) remains constant up to a very high frequency (over 10.0GHz). At a certain frequency, $Z_{ind}$ and Re($Z_{ind}$) exhibit peak values while Im($Z_{in}$) becomes zero, and this is the resonance frequency, $f_0$ (around 13.7GHz) for the CMOS cascode active inductor. Starting from a low frequency to the $f_0$, the positive Phase($Z_{ind}$) (phase angle) indicates the inductive operating region. Note that in the lower frequency region (below 6.0GHz) of inductive impedance, Phase($Z_{ind}$) is less than $90^0$. Although active inductors exhibit phase angle less than $90^0$ in the lower frequency part of the inductive region, they still can be used in an application like inductive peaking. After resonance frequency, Im($Z_{ind}$) becomes negative while both $Z_{ind}$ and Re($Z_{ind}$) continuously decrease. The frequency characteristics of CMOS cascode active inductor (Figure 2.11) are similar to those of an on-chip passive inductor (Figure 2.5).

Figure 2.12 shows the simulated frequency responses of inductance ($L_s$) and quality factor ($Q$) of CMOS cascode active inductor. Note that at resonance frequency (zero-crossing frequency), both $Q$ and $L_s$ are zero, and they becomes negative after resonance frequency. Hence, the frequency characteristics of ($L_s$) and $Q$ of CMOS cascode active inductor resemble those (Figure 2.6) of the passive inductor. The CMOS cascode active inductor achieves an inductance

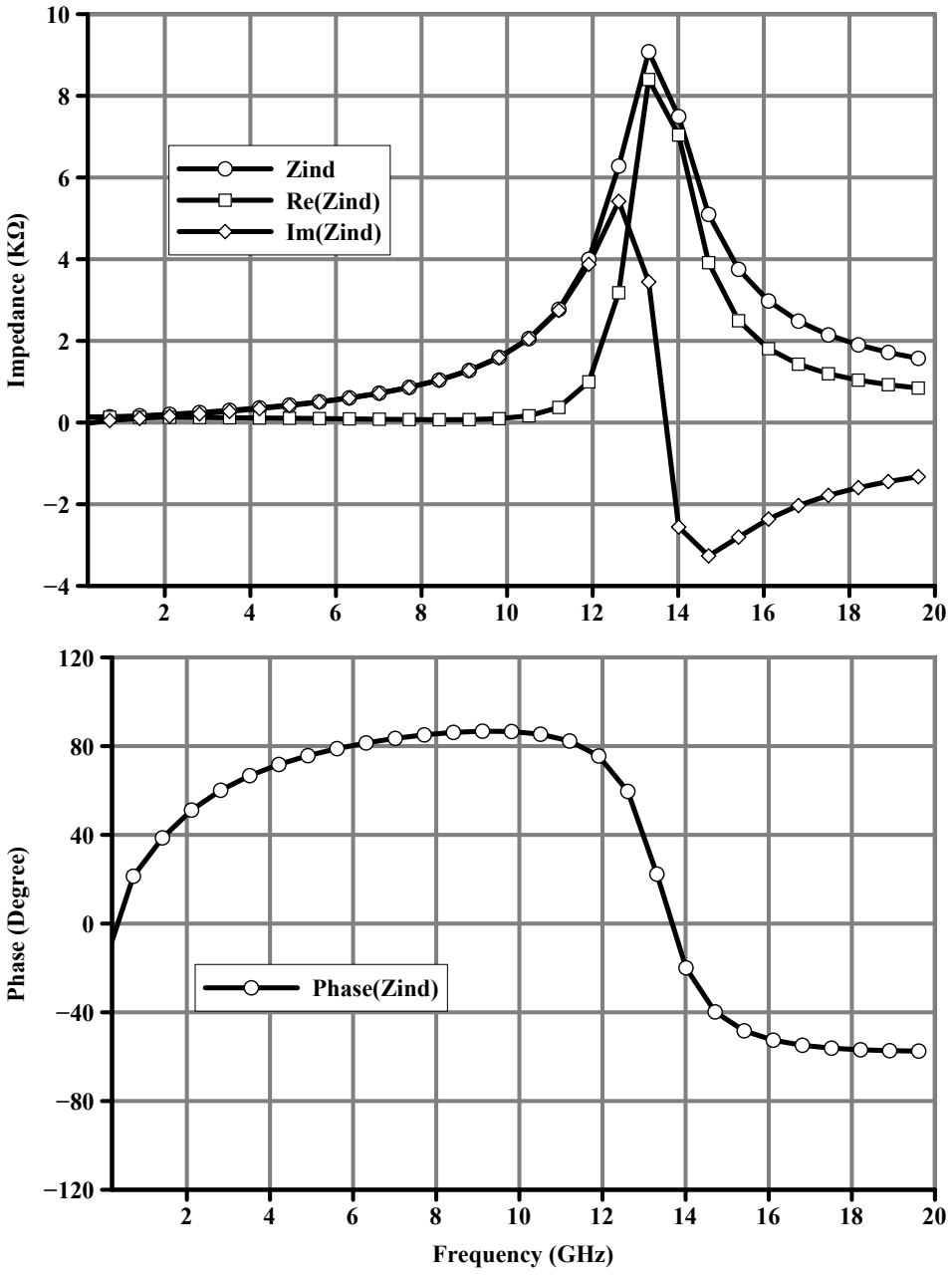


Figure 2.11: Impedances and phase of CMOS cascode active inductor over frequency.

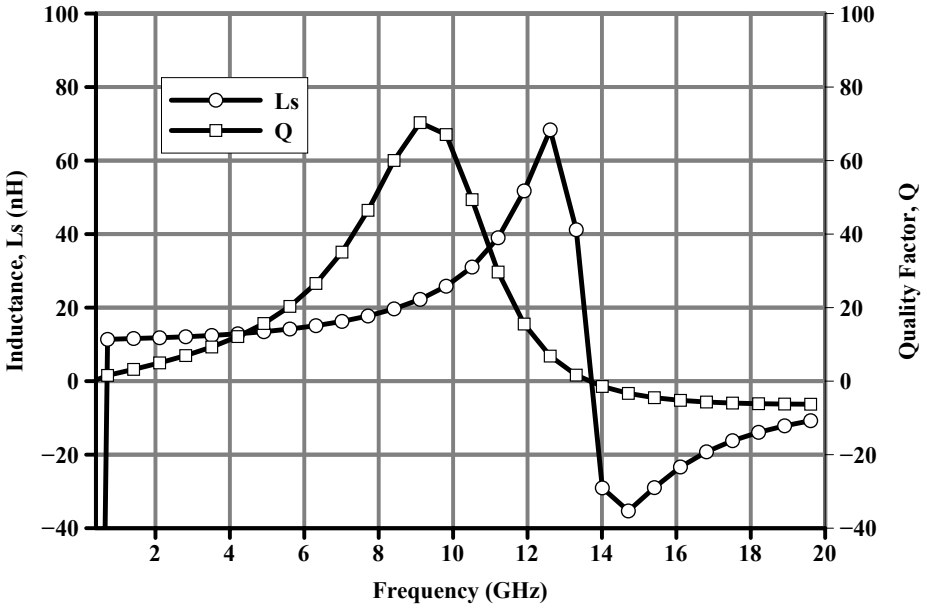


Figure 2.12: Inductance and $Q$ of CMOS cascode active inductor over frequency.

of 14.0nH (at DC) and a maximum $Q$ of 70.0 whereas a 5.0nH (at DC) CMOS passive inductor achieves a maximum $Q$ of 17.0 (Figure 2.6). A 5.0nH passive inductor reaches $f_0$ below 10.0GHz, whereas a cascode active inductor with a 14.0nH value reaches $f_0$ of 13.8GHz. Hence, the CMOS active inductor has relatively higher resonance frequency with high inductance values. The 5.0nH passive inductor occupies a chip area of $285\mu$m $\times$ $285\mu$m (0.08mm$^2$), whereas the estimated chip area of the CMOS cascode active inductor is $30\mu$m $\times$ $20\mu$m (0.0006mm$^2$). Thus, a 14.0nH CMOS cascode active inductor is almost 133 times smaller than that of a 5.0nH on-chip passive inductor.

### 2.2.5 Previous Designs of CMOS Active Inductors

Depending on their applications, many configurations for CMOS one-port active inductors have been proposed. CMOS cascode active inductors in Figure 2.10 require a minimum supply voltage ($V_{DD}$) of twice the gate-source voltage ($V_{GS}$) plus one overdrive voltage (or gate drain-voltage $V_{DS,sat}$) (=$2V_{GS}$+$V_{DS,sat}$)

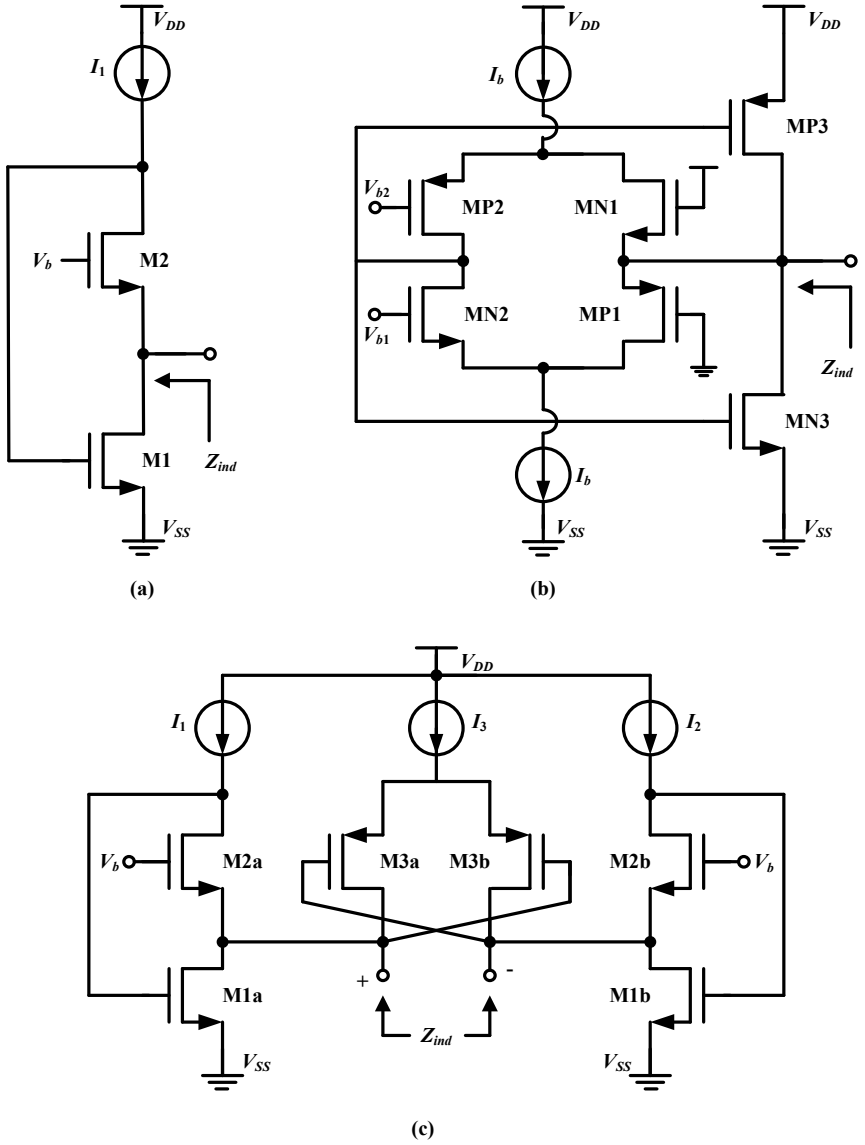


Figure 2.13: (a) Low-voltage active inductor, (b) class AB active inductor, (c) two-port floating active inductor (reproduced from [24],[25] and [26]).

of transistors. For a low voltage operation, the active inductor in Figure 2.13(a) has been proposed [24], and it requires a minimum $V_{DD}$ of $V_{GS}$ plus $V_{DS,sat}$ ($V_{GS}$+ $V_{DS,sat}$) only. This active inductor exhibits better noise performance because of using only a few transitors. However, with a low parallel resistance

$R_p$ of its $RLC$ model, the active inductor in Figure 2.13(a) exhibits a low $Q$ ($Q = R_p/\omega L_s$).

For increased signal handling capability along with low voltage operation, the CMOS active inductor of class AB configuration has been proposed as shown in Figure 2.13(b) [25]. This circuit consists of two complementary folded-cascode amplifiers and a push-pull stage. The signals at the input of the inductor swing between $V_{DD}$ plus $V_{THN}$ ($V_{DD}$+$V_{THN}$) and $V_{SS}$ plus $V_{THP}$ ($V_{DD}$+$V_{THN}$) where $V_{THN}$ and $V_{THP}$ are the threshold voltages of NMOS and PMOS transistors, respectively. With complementary power supplies (+$V_{DD}$ or -$V_{SS}$), the maximum swing can be obtained as $2V_{DD}$ or $2V_{SS}$ but still the circuit can operate with a minimum supply of $V_{GS}$+ $V_{DS,sat}$. One of the limitations of this active inductor is that with increased dynamic range, the inductance varies widely. Moreover, an increased number of transistors degrades the noise performance of the inductor. Besides one-port CMOS active inductors, a two-port floating active inductor is shown in Figure 2.13(c) [26]. This double-ended active inductor is obtained by connecting two active inductors of Figure 2.13(a) through a pair of cross-coupled transitors M3a and M3b. The inductive Impedance $Z_{ind}$ is obtained between nodes ($\pm$) and therefore, this inductor is called the differential or floating inductor. One common feature of all CMOS active inductors in Figure 2.13 is that they can be made tunable by controlling current sources using external voltages.

### 2.2.6 Comparison between Passive and Active Inductors

Comparisons between passive and active inductors allow for choosing one over others with the most favorable advantages in the design of RFICs. The most practical advantage of using active inductors over passive inductors is the substantial reduction of the chip real estate leading to the low-cost development of RFICs. CMOS on-chip passive inductors are constructed using metal wires on silicon substrates. When energized, the magnetic and electric fields are created in passive inductors, and energy is stored in them. As a stand-alone element, a passive inductor exhibits inductance, often called the self-inductance but with two or more closely placed inductors, they also exhibit mutual inductance be-

tween them. Hence, it is difficult to model and analyze an on-chip passive inductor in presence of other closely spaced inductors and circuits because of the electro-magnetic coupling among them. Moreover, mutual inductances affect the performances of core RF circuits. Inductance, quality factor $Q$, and resonance frequency of passive inductors depend on their physical shapes and sizes. The higher the inductance required, the larger the size of the inductor. The larger size inductor with long wires reduces $Q$ because of higher amounts of resistive and substrate losses. The large size of inductors also reduces resonance frequency because of increased parasitic components, and in turn, reduces the inductance operating frequency range. Theoretically, there is no voltage drop across passive inductors as the resistance of the metal wires is considered negligible. Therefore, a high DC voltage headroom is available with inductive loads allowing for large signal swing across them, and this leads to the development of highly linear RF and analog circuits [2, 3]. Theoretically, passive inductors do not contribute noise to core RF circuits because of negligible resistances. However, noise from other noisy circuits is coupled to them via the substrate and penetrates to noise-sensitive RF and analog circuits. Because of fixed metal structures, passive inductors can not be tuned.

CMOS active inductors are impedance-converter circuits, mimicking inductive behavior. The positive impedance converter circuits (using gyrator) of active inductors transforms a capacitance into a virtual inductance. There is no real existence of magnetic field, and the node capacitances (of transistors) work as energy-storage devices. Thus, in absence of real magnetic fields, closely-spaced active inductors do not interact with each other; hence, there is no existence of mutual inductance. The inductance of active inductors depend on the intrinsic capacitances and transconductances of transistors. Using small size devices, and spending a small amount of power for CMOS active inductors, high and tunable inductances can be obtained. Moreover, lower losses (resistive and substrate losses) of small size devices cause a high $Q$ for active inductors. Small areas of active inductors contribute less parasitic components (resistances and capacitances) to the substrate leading to high resonance frequency. Unlike passive inductors, one of the important advantages of active

Table 2.1: Typical parameters of active and passive inductors.

| Item | Passive inductors | Active inductors |
|---|---|---|
| Inductance(nH) | $\leqslant$5.0 | 5.0-100.0 |
| Quality factor ($Q$) | 5.0-30.0 | 10.0-1000.0 |
| Tunability | No | Yes |

inductors is their tunability. Since active inductors are circuits, they consume a certain amount of DC power depending on device sizes and bias conditions. Because of the inherent noise of transistors, active inductors are noisy. Therefore, active inductors are not suitable to be used in the input matching network of RFICs as they directly contribute noise to the input-referred noise of the RFICs. Depending on their configurations, active inductors also require a certain supply voltage to be operated. With a low supply voltage, a low voltage headroom is available at the their inputs. This causes the limited swing of signals at the inputs of active inductors that results into a low linearity. Hence, active inductors can not be suitably used for power amplifiers where output signal can swing above the supply voltage.

Whether using active or passive inductors, the achievable inductance ($L_s$), $Q$, resonance frequency ($f_0$), and chip-area need to be considered. In CMOS process technologies, passive inductors can achieve inductance of a few nH ($\leqslant$5.0nH) because of the practical limitation of the required chip area (greater than 300$\mu$m $\times$ 300$\mu$m for 5.0nH inductance). On the other hand, an active inductor can achieve tens of nH (10.0nH to 100.0nH and over) while requiring a small chip area. With advanced process technologies and design techniques, CMOS passive inductors can have $Q$ of 5.0 to 30.0, whereas active inductors can have $Q$ of 100.0-1000.0 and over. For sub-nH to nH inductance, $f_0$ of passive inductors drops from tens of GHz to a few GHz but $f_0$ of active inductors does not decrease drastically because the sizes of the passive inductors remain almost the same and do not contribute to increased parasitics. The tuning of active inductors also allow for varying $L_s$, $Q$, and $f_0$. Table 2.1 summarizes typical values for the parameters of active and passive inductors.

# Chapter 3

# Q-Enhanced and Bandwidth-Extended Tunable CMOS Active Inductors

This chapter presents two new CMOS configurations for quality factor ($Q$) enhancement and bandwidth extension of tunable active inductors. A $Q$-enhanced active inductor employing positive and negative feedbacks is introduced and described in Sections 3.1 to 3.3. Then, an extended-bandwidth active inductor using dual negative feedbacks is presented in Sections 3.4 to 3.5. The proposed inductors are designed and fabricated in a 90nm digital CMOS process. The measurement results along with simulation results are presented to evaluate the performances of the fabricated active inductors.

## 3.1 Proposed $Q$-Enhanced CMOS Active Inductor

CMOS active inductors based on classical gyrator-$C$ configuration emulate an inductive input impedance by gyrating a load capacitance into an inductance. This inductive input impedance can be modelled by a parallel $RLC$ circuit, whose equivalent impedance is expressed with a second-order transfer function as described in Chapter 2. The first CMOS implementation of an active inductor resembling gyrator-$C$ configuration, and its inductive input-impedance ($Z_{ind}$) modelled by an $RLC$ circuit are shown in Figure 3.1 [23]. In the $RLC$ circuit of Figure 3.1(b), $L_s$ represents the inductance of the active inductor in series with a resistance $R_s$, $R_p$ is the parallel resistance and $C_p$ is the parallel

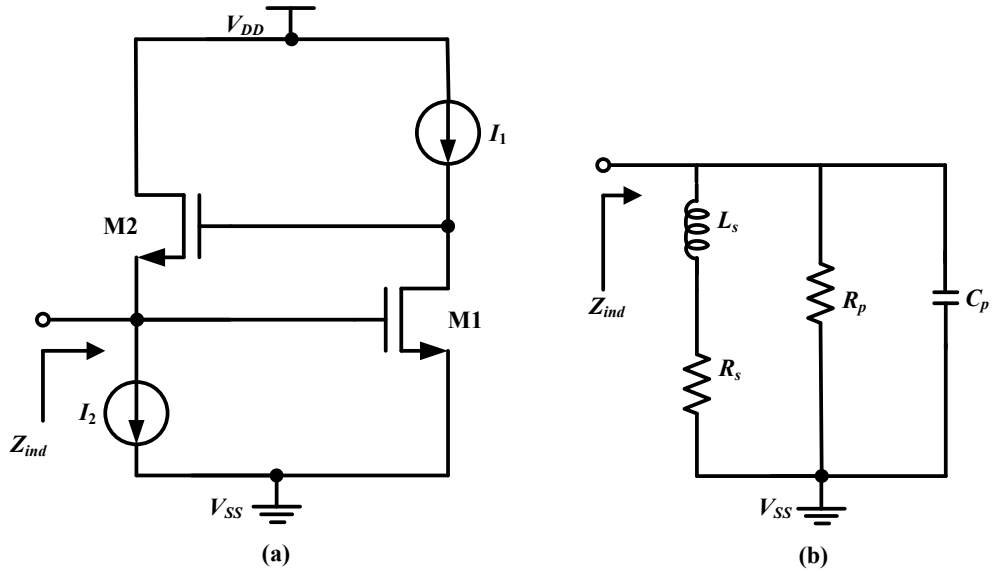


Figure 3.1: (a) CMOS active inductor resembling gyrator-$C$ configuration, (b) equivalent $RLC$ model of inductive impedance, $Z_{ind}$.

capacitance. $R_s$ and $R_p$ represent losses (series and parallel) of the inductor. $R_s$ and $Q$ of this active inductor (Figure 3.1) are derived in Chapter 2 as

$$Q = \omega_0 \frac{C_{gs2}}{g_{ds1}} \tag{3.1}$$

and

$$R_s = \frac{g_{ds1}}{g_{m1} g_{m2}}, \tag{3.2}$$

where $g_{ds}$, $g_m$ and $C_{gs}$ with subscript notations (1, 2) represent conductance, transconductance and gate-source capacitance of the corresponding transistor respectively. In deriving $Q$, the effect of $R_p$ is neglected. Note that $Q$ decreases with a high output conductance $g_{ds1}$ (or a low ourput resistance $r_{ds1}$) of transistor M1. A high $g_{ds1}$ ($=1/r_{ds1}$) causes a high loss in the inductor, yielding a high series resistance $R_s$ with inductance $L_s$. In other words, the low-gain ($g_{m1} r_{ds1}$) of the common-source amplifier (consisting of transistor M1 and current-source $I_1$) in the inductor (Figure 3.1) caused by a low $r_{ds1}$ (or a

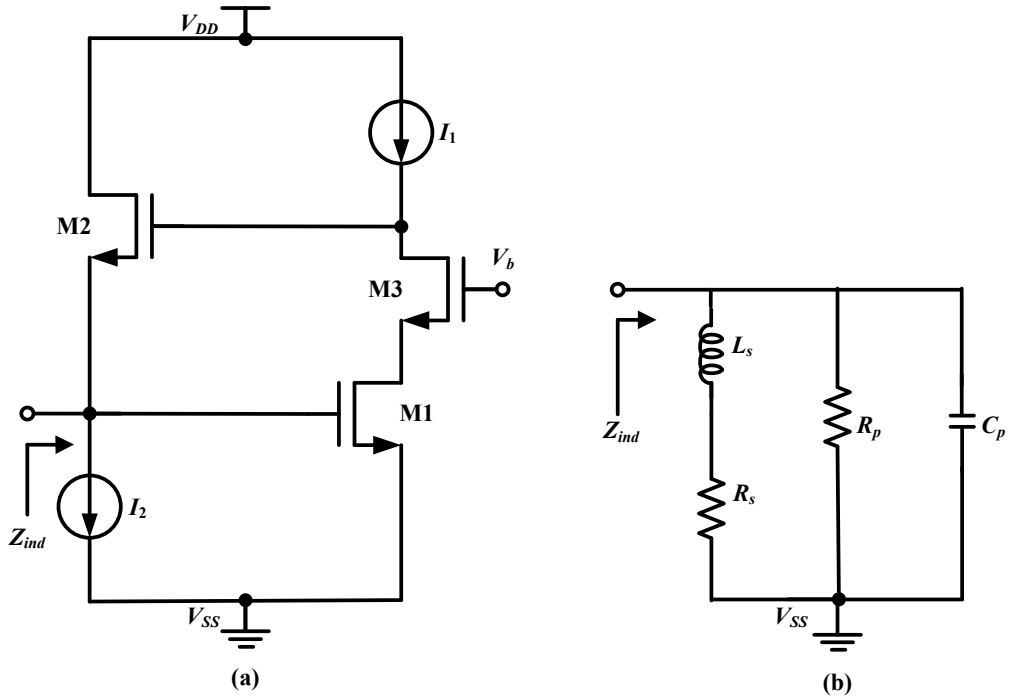


Figure 3.2: (a) CMOS cascode active inductor, (b) equivalent $RLC$ model of inductive impedance, $Z_{ind}$.

high $g_{ds1}$) reduces the amount of negative feedback at the input of the inductor (Node 1). This reduced negative feedback results in an increased $R_s$, and in turn, results in a low $Q$ for the active inductor.

To improve the $Q$ factor, a CMOS cascode active inductor is proposed as shown in Figure 3.2(a), where a cascode transistor M3 tops on transistor M1 [4]. The $RLC$ model of the inductive impedance ($Z_{ind}$) of the cascode active inductor is shown in Figure 3.2(b), and its elements $L_s$, $R_s$, $R_p$ and $C_p$ are derived as follows:

$$L_s = \frac{C_{gs2}}{g_{m1}g_{m2}}. \tag{3.3}$$

$$R_s = \frac{g_{ds1}g_{ds3}}{g_{m1}g_{m2}g_{m3}}. \tag{3.4}$$

$$R_p = \frac{1}{g_{m2}}. \tag{3.5}$$

$$C_p = C_{gs1}. \tag{3.6}$$

Neglecting the effect of $R_p$, the $Q$ of the cascode active inductor is expressed as

$$Q = \omega_0 \frac{L_s}{R_s} = \omega_0 \frac{C_{gs2} g_{m3}}{g_{ds1} g_{ds3}}. \tag{3.7}$$

Note that conductance $g_{ds3}$ (in the order of $10^{-6}$) of transistor M3 is much smaller than its transconductance $g_{m3}$ (in the order of $10^{-3}$). Hence, $R_s$ is significantly reduced due to the induction of $g_{ds3}$ in the numerator of the expression of $R_s$, and thus, series losses in the inductor is reduced leading to a very high $Q$. It is also evident from the expression of $Q$ (Equation 3.7) that $g_{ds3}$ appears in its denominator and this causes $Q$ to be much higher than that of the active inductor of Figure 3.1. In other words, the output resistance ($g_{m3} r_{ds1} r_{ds2}$) and gain ($g_{m1} g_{m1} r_{ds1} r_{ds2}$) of the cascode amplifier (consisting of M1, M3 and $I_1$) of the active inductor (Figure 3.2) are much higher than those of the common-source amplifier of the active inductor (Figure 3.1). The increased output resistance (or the reduced conductance) of the cascode amplifier enhances $Q$, yielding a low loss caused by a low series resistance $R_s$. However, the increased output resistance and gain of the cascode amplifier do not have any effect on $R_p$ that causes parallel losses; these are comparable to series losses caused by $R_s$. In deriving $Q$ of the cascode inductor as expressed by Equation 3.7, the effect of $R_p$ is neglected. Taking $R_p$ into account, the effective quality factor ($Q_{eff}$) of the cascode active inductor can be expressed as

$$Q_{eff} \approx \omega_0 \frac{1}{L_s(\frac{1}{R_p} + \frac{R_s C_p}{L_s})}. \tag{3.8}$$

Thus, $Q_{eff}$ of the cascode active is lower than the $Q$ obtained by Equation

3.7. Hence, parallel losses caused by $R_p$ contribute to the reduction of the overall or effective $Q$ ($Q_{eff}$) of the cascode active inductor.

For further enhancement of $Q$, along with series losses, parallel losses of active inductors need to be reduced. In general, the inductive impedance ($Z_{ind}$) of CMOS one-port active inductors, including the cascode inductor, can be modeled by a typical parallel resonance circuit of Figure 3.3(a) where resistances $R_{sL}$ and $R_{sC}$ appear in series with $L_s$ and $C_p$, respectively, and $R_p$ is the parallel resistance. For CMOS active inductors, such an $RLC$ model of Figure 3.3(a) represents a combination of losses (series and parallel) appearing in series or parallel with $L_s$ (or $C_p$). To enhance the $Q$ of active inductors, here, a new $RLC$ model is proposed as shown in Figure 3.3(b) where a negative resistance $R_n$ is introduced in parallel with $R_p$. $R_n$ compensates the effects of $R_p$, $R_{sL}$ and $R_{sC}$ to minimize active inductor's overall losses. With narrowband approximations [27], the $RLC$ circuit of Figure 3.3(b) can be transformed into an equivalent $RLC$ circuit of Figure 3.3(c). In Figure 3.3(c), series losses caused by $R_{sL}$ and $R_{sC}$ appear as parallel losses $R_{pL}$ and $R_{pC}$, respectively. $R_{pL}$ and $R_{pC}$ are approximately expressed as follows:

$$R_{pL} \cong \frac{L_s}{R_{sL}C_p}. \tag{3.9}$$

$$R_{pC} \cong \frac{L_s}{R_{sC}C_p}. \tag{3.10}$$

The circuit in Figure 3.3(c) can be transformed into an equivalent $RLC$ circuit of Figure 3.3(d) where lumped parallel element $R_{eq}$ represents the total losses of the active inductor and expressed as

$$R_{eq} = (R_{pL} \| R_{pC} \| R_p). \tag{3.11}$$

In terms of conductances ($G$=1/R), Equation 3.11 can be rewritten as

$$G_{eq} = G_{pL} + G_{pC} + G_p. \tag{3.12}$$

Negative resistance $R_n$ ($1/G_n$) parallel with $R_{eq}$ ($1/G_{eq}$) increases the ef-

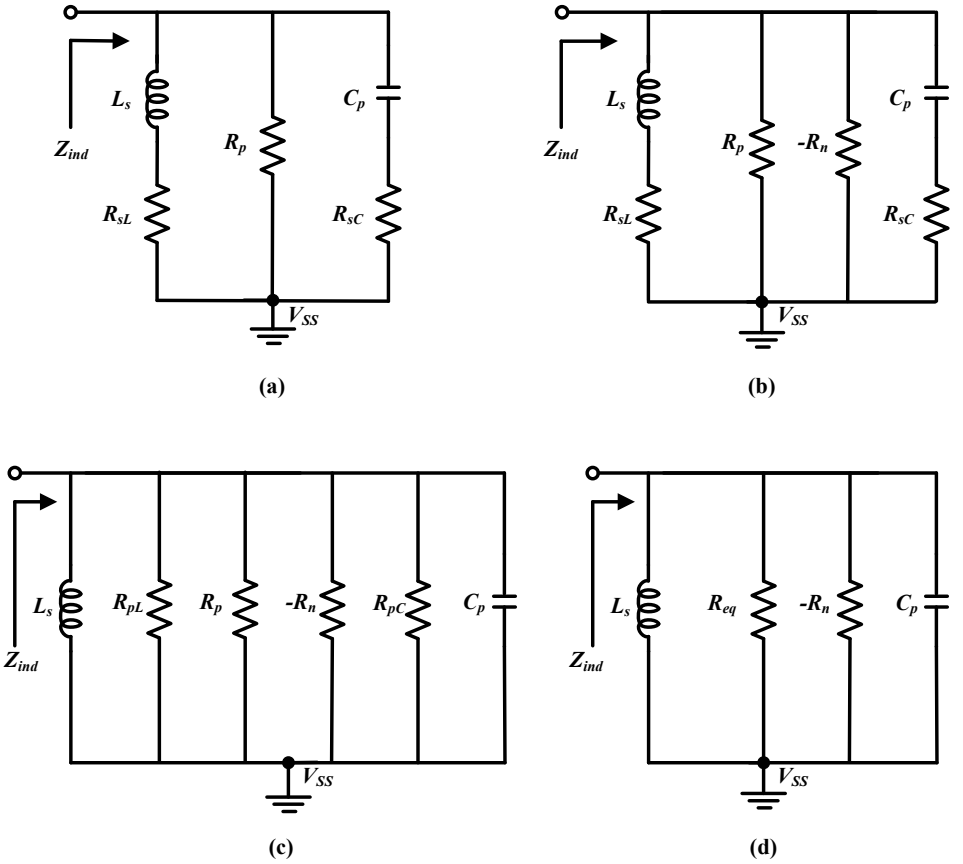


Figure 3.3: (a) Typical $RLC$ model of inductive impedance, $Z_{ind}$ of CMOS active inductors, (b) $RLC$ model of $Z_{ind}$ for proposed new $Q$-enhanced active inductor, (c) equivalent$RLC$ circuit of (b) with narrowband approximations, (d) equivalent parallel $RLC$ circuit of (c).

fective parallel resistance or decreases the effective parallel conductance ($G_{eq}$) as

$$G_{eff} = G_{eq} - G_n, \tag{3.13}$$

where $G_{eq}$ and $G_n$ are the conductances of resistances $R_{eq}$ and $R_n$, respectively. Hence, this decreased parallel conductance or increased parallel resistance will reduce losses in the proposed new inductor, and in turn, will enhance $Q$. Mathematically, the $Q$ of the proposed new active inductor based on the $RLC$ model of inductive-impedance $Z_{ind}$ of Figure 3.3(b) can be expressed as

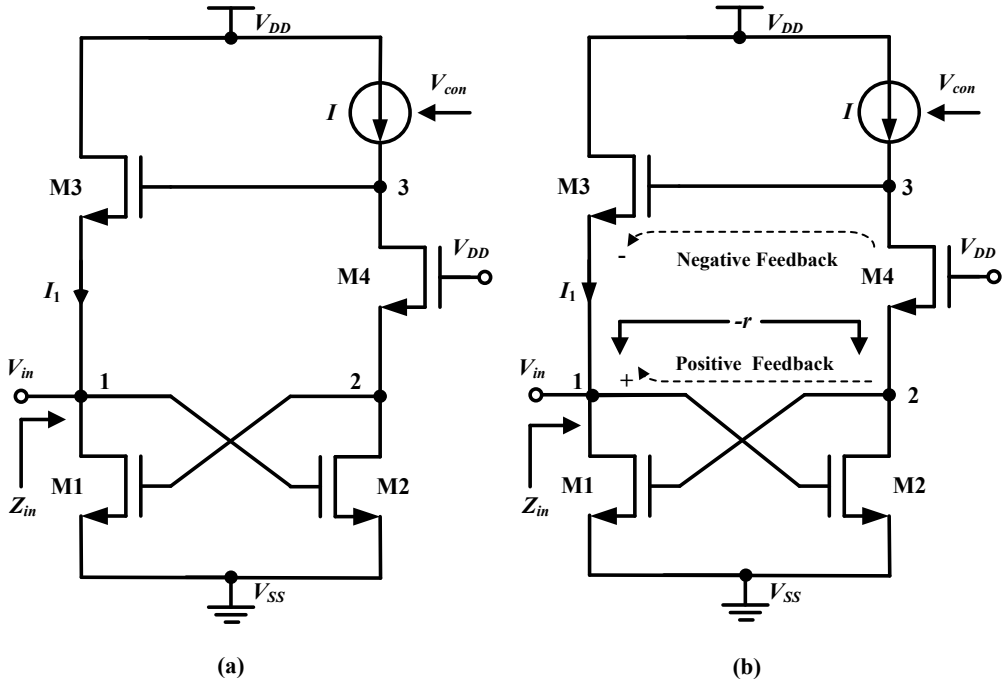


Figure 3.4: (a) Circuit of proposed $Q$-enhanced active inductor, (b) proposed $Q$-enhanced active inductor with negative and positive feedbacks.

$$Q_{enhanced} = \frac{1}{\omega_0 L_s (G_{eq} - G_n)} = \frac{\omega_0 C_p}{G_{eq} - G_n}. \tag{3.14}$$

Hence, by choosing $R_n$ (=$1/G_n$) very close to $R_{eq}$ (=$1/G_{eq}$), theoretically, an infinite $Q$ for the proposed new active inductor can be achieved.

### 3.1.1 Design of *Q*-Enhanced Active Inductor

Based on the new $RLC$ model of Figure 3.3(b), a new $Q$-enhanced active inductor is proposed as shown in Figure 3.4(a) [28], which embeds a pair of cross-coupled transistors (M1 and M2) into a cascode configuration to create a negative resistance for $Q$ enhancement. Due to negative resistance, concurrent positive and negative feedbacks occur in the proposed active inductor as shown in Figure 3.4(b). The negative feedback at the input (Node 1) through transistors M2, M4 and M3 creates the inductive impedance by exploiting a

CMOS gyrator-$C$ configuration. The cross-coupled transistors M1 and M2 form a negative-impedance circuit (NIC) to provide positive feedback at the input (Node 1). The positive feedback creates negative resistance (-$r$), which increases the equivalent parallel resistance of the $RLC$ circuit of the inductive impedance ($Z_{ind}$) of the proposed inductor, and in turn, enhances $Q$ yielding low losses.

With negative feedback as shown in Figure 3.4(b), transistors M2 and M3 form two back-to-back connected transconductors ($g_{m2}$ and $g_{m3}$) resembling two transconductors of a gyrator-$C$ configuration. Input voltage $V_{in}$ (at Node 1) is converted to a current by transistor M2. This current flows through cascode transistor M4 and charge integration capacitance $C_{gs3}$ (gate-source capacitance) of transistor M3, which converts charging voltage across $C_{gs3}$ into a current flowing through Node 1. Thus, input impedance $Z_{in}$ looking at Node 1 becomes inductive yielding the gyrator-$C$ configuration that includes capacitance $C_{gs3}$ as the load, and two transconductors: $g_{m2}$ and $g_{m3}$. Cascode device M4 increases DC gain, and in turn, increases the loop gain. The increased loop gain reduces the series resistance of the inductance that reduces series losses, and in turn, enhances the $Q$ of the proposed active inductor.

With positive feedback, transistors M1 and M2 form negative resistance -$r$ between nodes 1 and 2 as

$$r = -\frac{(g_{m1} + g_{m2})}{g_{m1} . g_{m2}}, \tag{3.15}$$

where $g_{m1}$ and $g_{m2}$ represent the transconductances of transistors M1 and M2 respectively. As input voltage $V_{in}$ is converted to a drain current by transistor M2, it also charges combined gate-source capacitance ($C_{gs1}$ plus $C_{gs4}$) of transistors M1 and M4. This charging voltage at Node 2 is fed back to the input (Node 1) as a current converted by transistor M1. Thus, positive feedback occurs at the input through negative resistance -$r$. Positive feedback also reduces the coupling of signals to the ground through gate-source capacitance $C_{gs4}$ of cascode device M4. In summary, the negative and positive feedbacks at the input (Node 1) reduce overall losses (both series and parallel losses) of

the proposed new $Q$-enhanced inductor, and in turn, increase $Q$.

### 3.1.2 Large-Signal Analysis of *Q*-Enhanced Active Inductor

In the proposed new $Q$-enhanced active inductor (Figure 3.4), DC operating points and nodal voltages are defined by a single current $I$. Indeed, if $I$ is the drain current of M2 (and M4), then the drain current of M1 (and M3) is defined as a function of gate-source voltage $V_{GS1}$ of M1, which is obtained by subtracting gate-source voltage $V_{GS4}$ of M4 from power supply voltage $V_{DD}$. Assuming all the transistors of the proposed active inductor are long-channel devices, and they operate in saturation, then, neglecting their body effects, the following equations for current $I$ and supply voltage $V_{DD}$ are obtained using MOSFET large-signal analysis of the proposed active inductor (Figure 3.4).

$$V_{DD} = V_{GS4} + V_{GS1}. \tag{3.16}$$

$$I = \frac{1}{2}\mu_n C_{ox}.(\frac{W}{L})_4(V_{GS4} - V_{TN})^2 = \frac{1}{2}\mu_n C_{ox}.(\frac{W}{L})_2(V_{GS2} - V_{TN})^2, \tag{3.17}$$

where $\mu_n$, $C_{ox}$ and $V_{TN}$ (threshold voltage of NMOS transistor) are process parameters, and $W/L$ (=*Width/Length*) with subscript notations (1, 2, 3, and 4) is the aspect ratio of the corresponding transistor. For a known value of $I$, gate-source voltages ($V_{GS2}$ and $V_{GS4}$) of transistors M2 and M4 are obtained using equation 3.17, and voltage at Node 1 ($V_1$) is calculated from $V_{GS2}$. The voltage at Node 2 ($V_2$) equals gate-source voltage ($V_{GS1}$) of M1, which defines current $I_1$ through transistor M1 or M3 (Figure 3.4). Hence, the following equations are obtained as

$$V_1 = V_{GS2} = V_{TN} + \sqrt{\frac{2I}{\mu_n C_{ox}(\frac{W}{L})_2}}, \tag{3.18}$$

$$V_2 = V_{GS1} = V_{DD} - V_{GS4} = V_{DD} - (V_{TN} + \sqrt{\frac{2I}{\mu_n C_{ox}(\frac{W}{L})_4}}), \tag{3.19}$$

and

$$I_1 = \frac{1}{2}\mu_n C_{ox}.(\frac{W}{L})_1(V_{GS1} - V_{TN})^2. \tag{3.20}$$

One can find gate-source voltage $V_{GS3}$ of M3 as

$$V_{GS3} = V_{TN} + \sqrt{\frac{2I_1}{\mu_n C_{ox}(\frac{W}{L})_3}}. \tag{3.21}$$

Hence, the voltage at Node 3 ($V_3$) is equal to

$$V_3 = V_{GS3} + V_{GS2}. \tag{3.22}$$

Thus, for a known value of current $I$ controlled by $V_{con}$ (Figure 3.4), and for known process parameters of transistors ($\mu_n$, $C_{ox}$ and $V_{TN}$), currents in all the transistors, and voltages at all the nodes of the proposed active inductor can be defined. Varying $I$ by control voltage $V_{con}$ changes the biasing conditions of the proposed inductor circuit, and in turn, changes device parameters ($C_{gs}$ and $C_{gd}$), and small-signal parameters ($g_m$ and $g_{ds}$) of transistors. The changing of these parameters leads to the tuning of inductance $L_s$, resonance frequency $\omega_0$ (in rad/s) and quality factor $Q$ of the proposed active inductor.

### 3.1.3 Small-Signal Analysis of *Q*-Enhanced Active Inductor

In the proposed $Q$-enhanced active inductor (Figure 3.4), considering transistor M4 simply transports the current of transistor M2, the small-signal model including transistors M2 and M3 is shown in Figure 3.5(a), where input current ($i_{in}$) is obtained as

$$i_{in} = -g_{m3}v_{cgs3} + g_{m2}v_{in}, \tag{3.23}$$

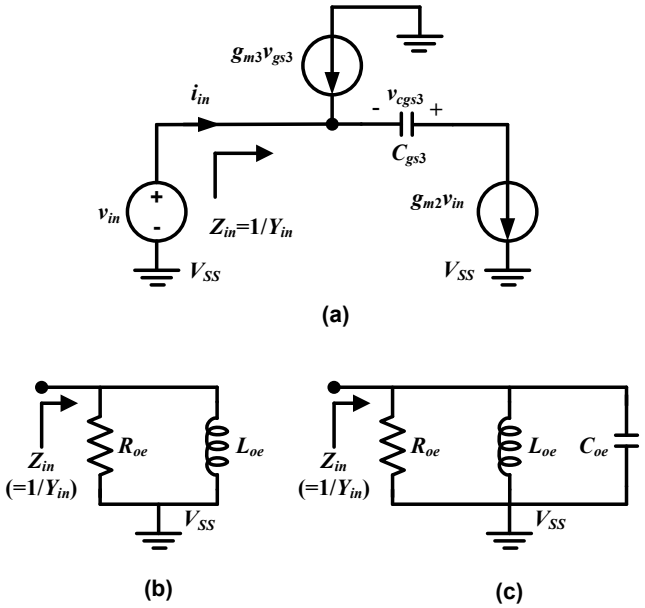


Figure 3.5: (a) Developing small-signal model of $Q$-enhanced active inductor, (b) equivalent $RL$ circuit, (c) equivalent $RLC$ circuit.

where

$$v_{cgs3} = -g_{m2}v_{in}.\frac{1}{sC_{gs3}}. \tag{3.24}$$

Hence, input admittance $Y_{in}$ (=$1/Z_{in}$) is obtained as

$$Y_{in}(s) = \frac{i_{in}}{v_{in}} = \frac{g_{m2}g_{m3}}{sC_{gs3}} + g_{m2} = \frac{1}{sL_{oe}} + \frac{1}{R_{oe}}, \tag{3.25}$$

where

$$L_{oe} = \frac{C_{gs3}}{g_{m2}g_{m3}}. \tag{3.26}$$

$$R_{oe} = \frac{1}{g_{m2}}. \tag{3.27}$$

Thus, $Y_{in}$ is a parallel connection of inductance $L_{oe}$ and resistance $R_{oe}$ as shown in Figure 3.5(b). The capacitances of transistors contribute to an equivalent capacitance ($C_{oe}$) that appears in parallel with $L_{oe}$ and resistance $R_{oe}$ as shown in Figure 3.5(c). The resonant frequency ($\omega_0$) and quality factor

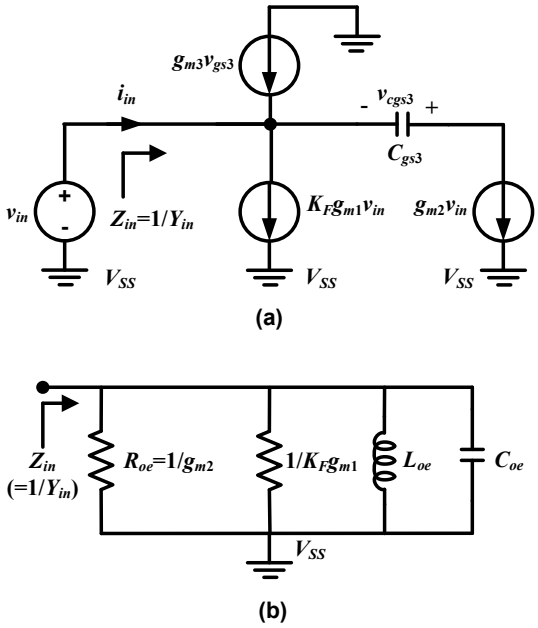


Figure 3.6: (a) Small-signal modeling of Q-enhanced active inductor introducing feedback, (b) equivalent $RLC$ circuit.

($Q$) factor of this parallel $RLC$ circuit can be obtained as

$$\omega_0 = \frac{1}{\sqrt{L_{oe}C_{oe}}} = \sqrt{\frac{g_{m2}g_{m3}}{C_{gs3}C_{oe}}}. \tag{3.28}$$

$$Q = \omega_0 C_{oe} R_{oe} = \sqrt{\frac{C_{oe}}{C_{gs3}}}.\sqrt{\frac{g_{m3}}{g_{m2}}}. \tag{3.29}$$

Changing $g_{m2}$ and $g_{m3}$ will change both $Q$ and $\omega_0$. This can be achieved with feedback at the input through transistor M1 (Figure 3.4), which can be modeled by a current source ($K_F g_{m1} v_{in}$) appearing in the small-signal model as shown in Figure 3.6(a). This gives $Y_{in}$ as

$$Y_{in}(s) = K_F g_{m1} + g_{m2} + \frac{g_{m2}g_{m3}}{sC_{gs3}}. \tag{3.30}$$

Here, $Y_{in}$ ($=1/Z_{in}$) can be modeled by the equivalent circuit of Figure 3.6(b) where an additional resistance $1/K_F g_{m1}$ appear in parallel with $1/g_{m2}$.

A negative value for $K_F$ increases overall parallel resistance, and thus $Q$ can be made infinitely large by choosing as

$$\frac{1}{g_{m2}} = -\frac{1}{K_F g_{m1}}. \tag{3.31}$$

The factor $K_F$ is expressed as

$$K_F = -\frac{g_{m2}}{g_{m1}}. \tag{3.32}$$

Now, for negative gain from the source to the drain of the cascode transistor M4 (Figure 3.4), and for negative factor $K_F$ (=-1), the overall feedback at the input of the active inductor through transistor M1 becomes positive. Thus, admittance $Y_{in}$ is obtained as

$$Y_{in}(s) = sC_{gs2} + g_{m2}(1 - \frac{g_{m1}}{gm_4}) + \frac{g_{m2}g_{m3}}{sC_{gs3}}. \tag{3.33}$$

If the term $g_{m2}(1 - g_{m1}/g_{m4})$ is small, then the active inductor can provide a very high $Q$ factor. Thus, the small-signal analysis can be used to model the active with an equivalent $RLC$ circuit that can determine its parameters.

### 3.1.4 Parameters of *Q*-Enhanced Active Inductor

The parameters of the proposed $Q$-enhanced active inductor, $L_s$, $\omega_0$ and $Q$, can be determined from the expression of the input-impedance $Z_{in}$, looking at Node 1 of the active inductor (Figure 3.4). Figure 3.7 shows the complete small-signal model of the proposed inductor to determine $Z_{in}$. As a first approximation, taking $g_m$ and $C_{gs}$ of transistors into account only while neglecting gate-drain capacitance $C_{gd}$ ($C_{gs} > C_{gd}$) and drain-source conductance $g_{ds}$ ($g_m > g_{ds}$), $Z_{in}$ can be expressed as

$$Z_{in}(s) = \frac{C_{gs3}(C_{gs1} + C_{gs4})s^2 + C_{gs3}g_{m4}s}{C_{gs2}C_{gs3}(C_{gs1} + C_{gs4})s^3 + C_{gs2}C_{gs3}g_{m4}s^2 + C_{gs3}g_{m2}(g_{m4} - g_{m1})s + g_{m2}g_{m3}g_{m4}}, \tag{3.34}$$

where $g_m$ and $C_{gs}$ with subscripts 1,2,3 and 4 are the parameters of transistors M1, M2, M3 and M4 respectively. Neglecting the non-dominant terms, at very

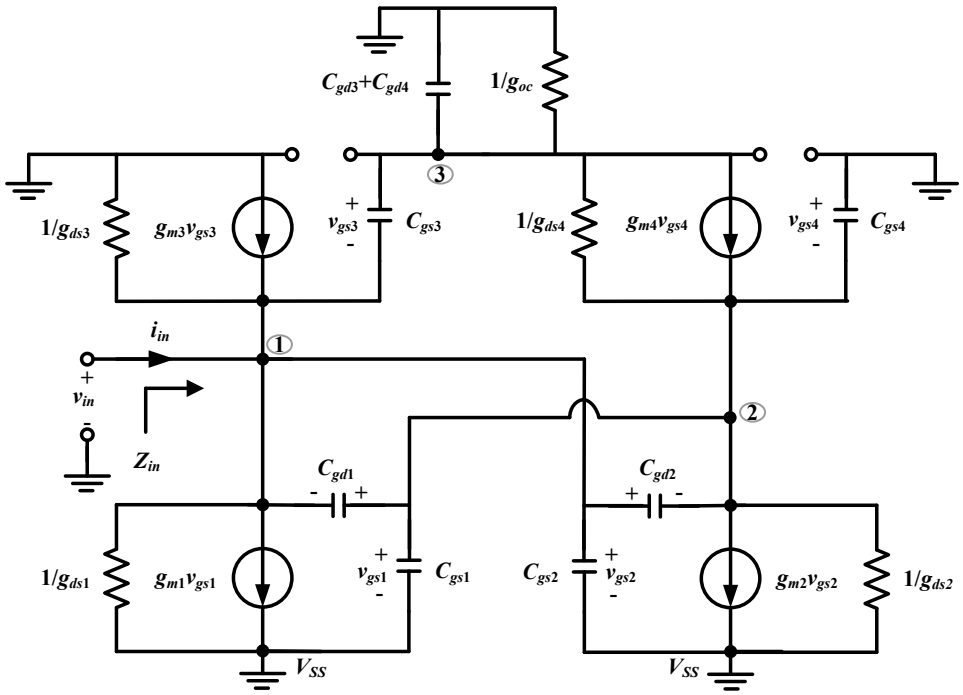


Figure 3.7: Small-signal model of $Q$-enhanced active inductor.

low-frequency (LF), and at very high-frequency (HF), $Z_{in}$ can be expressed as

$$Z_{in,LF}(s) \approx \frac{sC_{gs3}}{g_{m2}g_{m3}}, \tag{3.35}$$

and

$$Z_{in,HF}(s) \approx \frac{1}{sC_{gs2}}. \tag{3.36}$$

Note that at LF and HF, $Z_{in}$ is inductive and capacitive respectively. Hence, inductive impedance starts from low frequency. Neglecting the non-dominant terms, $Z_{in}$ over mid-frequency (MF) range can be expressed as follows:

$$Z_{in,MF}(s) \approx \frac{s^2C_{gs3}(C_{gs1}+C_{gs4}) + sC_{gs3}g_{m4}}{C_{gs2}C_{gs3}g_{m4}s^2 + C_{gs3}g_{m2}(g_{m4}-g_{m1})s + g_{m2}g_{m3}g_{m4}} \tag{3.37}$$

or

$$Z_{in,MF}(s)(or Z_{ind}) \approx \frac{s^2\frac{C_{gs1}+C_{gs4}}{g_{m4}C_{gs2}} + s\frac{1}{C_{gs2}}}{s^2 + s\frac{g_{m2}(g_{m4}-g_{m1})}{g_{m4}C_{gs2}} + \frac{g_{m2}.g_{m3}}{C_{gs2}.C_{gs3}}}. \tag{3.38}$$

Note that the expression of $Z_{in,MF}$ in Equation 3.38 is a second-order transfer function, which indicates the existence of an inductive element as described in Chapter 2. Here, $Z_{in,MF}$ (or $Z_{ind}$) can be compared with a second-order transfer function of Equation 3.39.

$$Z(s) = \frac{s^2R_s + s\frac{1}{C_p}}{s^2 + s\frac{1}{R_pC_p} + \frac{1}{L_sC_p}}. \tag{3.39}$$

As a second-order expression, *Z(s)* represents the equivalent impedance of a parallel $RLC$ circuit where $L_s$ represents inductance, $C_p$ is the capacitance in series with resistance $R_s$ and $R_p$ is in parallel $L_s$. Comparing $Z_{in,MF}(s)$ of Equation 3.38 with *Z(s)* of Equation 3.39, $Z_{ind}$ of the proposed $Q$-enhanced active inductor can be modeled by an $RLC$ circuit of Figure 3.8(a), and the elements of this $RLC$ circuit are obtained as follows:

$$L_s = \frac{C_{gs3}}{g_{m2}g_{m3}}. \tag{3.40}$$

$$R_s = \frac{C_{gs1}+C_{gs4}}{g_{m4}C_{gs2}}. \tag{3.41}$$

$$C_p = C_{gs2}. \tag{3.42}$$

$$R_p = -\frac{g_{m4}}{g_{m2}(g_{m1}-g_{m4})}. \tag{3.43}$$

Here, $R_s$ represents a series loss of the proposed new active inductor that

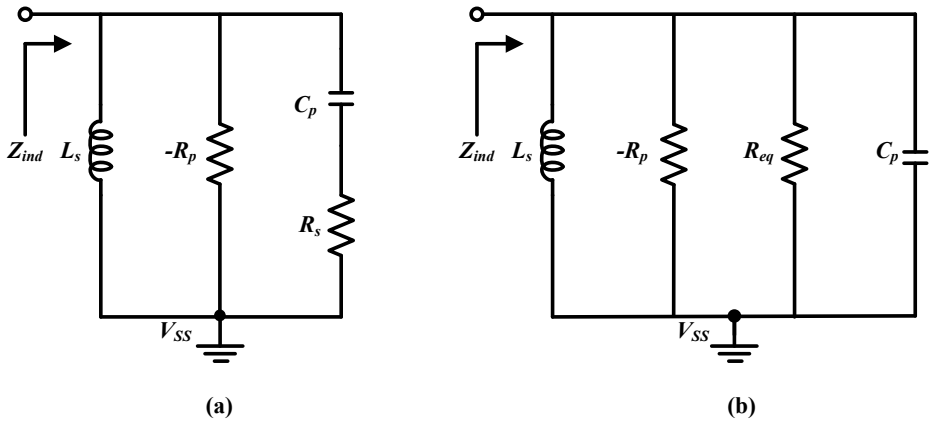


Figure 3.8: (a) $RLC$ circuit of inductive impedance $Z_{ind}$ of $Q$-enhanced active inductor, (b) equivalent parallel $RLC$ circuit of (a) with narrowband approximations.

appears in series with $C_p$ instead of $L_s$. $R_p$ is negative for $g_{m1}$ greater than $g_{m4}$. Note that negative resistance $R_p$ appears in parallel with $L_s$ and $C_p$. With narrowband approximations, the circuit in Figure 3.8(a) can be transformed into a parallel $RLC$ circuit of Figure 3.8(b) where $R_{eq}$ is equal to

$$R_{eq} = R_s + \frac{1}{\omega_0^2 C_p R_s} \cong R_s(1 + Q_C^2) \cong \frac{L_s}{C_p R_s}. \tag{3.44}$$

where $Q_C$ is the quality factor of the capacitor $C_p$ at $\omega_0$ and is expressed as

$$Q_C = \frac{1}{\omega_0 R_s C_p}. \tag{3.45}$$

Here, overall $Q$ ($Q_{eff}$) and $\omega_0$ of the proposed active inductor are expressed as

$$Q_{eff} = \frac{\omega_0 C_p}{\frac{1}{R_{eq}} - \frac{1}{R_p}} = \frac{\omega_0 C_{gs2}}{\frac{L_s}{C_p R_s} - (\frac{g_{m1} - g_{m4}}{g_{m2} g_{m4}})}, \tag{3.46}$$

and

$$\omega_0^2 = \frac{1}{L_s C_p} = \frac{g_{m2} g_{m3}}{C_{gs2} C_{gs3}}. \tag{3.47}$$

Note that $Q_{eff}$ increases due to the subtraction term $1/R_p$ in the denominator of Equation 3.46 and $\omega_0$ reaches close to unity-gain-cutoff-frequency $f_t$ $(g_m/C_{gs})$ of a transistor.

More accurate parameters for the proposed $Q$-enhanced active inductor can be obtained using complex models of transistors that also take into account $g_{ds}$ and $C_{gd}$ along with $g_m$ and $C_{gs}$. However, deriving $Z_{in}$ using the complete small-signal model of Figure 3.7 becomes a complex task; therefore, some non-significant elements can be ignored. Because of small-size devices and low-bias currents, $C_{gd4}$ and $g_{ds4}$ of transistor M4 can be neglected. $C_{gd3}$ and $g_{ds3}$ of transistor M3 can also be neglected because they are very small compared with $C_{gs3}$ and $g_{m3}$ respectively. Conductance $g_{oc}$ looking into the current-source $I$ is also neglected as it is very low due to a low $I$. Thus, inductive input impedance $Z_{ind,cor}$ over MF range can be approximated as

$$Z_{ind,cor}(s) \approx \frac{s^2 fk + sek}{s_2[k(be + af) + (cg + dh)] + s[ake - (ch + id) + ci}. \tag{3.48}$$

where coefficients a,b,c.....are obtained as follows:

$$a = g_{ds1}. \tag{3.49}$$

$$b = C_{gd1} + C_{gd2} + C_{gs1}. \tag{3.50}$$

$$c = g_{m2}. \tag{3.51}$$

$$d = C_{gd1} + C_{gd2}. \tag{3.52}$$

$$e = g_{ds2} + g_{m4}. \tag{3.53}$$

$$f = C_{gs1} + C_{gs4} + C_{gd1} + C_{gd2}. \tag{3.54}$$

$$g = C_{gs3}(C_{gd1} + C_{gd2}). \tag{3.55}$$

$$h = C_{gs3}(g_{m1} + g_{m4}). \tag{3.56}$$

$$i = g_{m3}g_{m4}. \tag{3.57}$$

$$k = C_{gs3}. \tag{3.58}$$

Equation 3.48 is also a second-order transfer function, and more accurate or corrected (cor) elements of the proposed active inductor are obtained as

$$L_{s,cor} = \frac{C_{gs3}(g_{ds2} + g_{m4})}{g_{m2}g_{m3}g_{m4}} \tag{3.59}$$

and

$$R_{s,cor} = \frac{C_{gs1} + C_{gs4} + C_{gd1} + C_{gd2}}{D_{cor}}, \tag{3.60}$$

where $D_{cor}$ is

$$\begin{aligned} D_{cor} &= C_{gs3}[(C_{gs2} + C_{gd1} + C_{gd2})(g_{ds2} + g_{m4})] + g_{ds1}[(C_{gs1} + C_{gs4}) \\ &+ C_{gd1} + Cgd2)] + C_{gs3}(C_{gd1} + C_{gd2})(g_{m2} + g_{m1} - g_{m4}). \end{aligned} \tag{3.61}$$

$$R_{p,cor} = \frac{C_{gs3}(g_{ds2} + g_{m4})}{g_{ds1}C_{gs3}(g_{ds2} + g_{m4}) - [g_{m2}C_{gs3}(g_{m1} - g_{m4}) + g_{m3}g_{m4}(C_{gd1} + C_{gd2})]}. \tag{3.62}$$

$$C_{p,cor} = (C_{gs2}+C_{gd1}+C_{gd2})+K_1(C_{gs1}+C_{gs4}+C_{gd1}+C_{gd1})+K_2(C_{gd1}+C_{gd2}), \tag{3.63}$$

where

$$K_1 = \frac{g_{ds1}}{g_{ds2} + g_{m4}}, \tag{3.64}$$

and

$$K_2 = \frac{g_{m2} + (g_{m1} - g_{m4})}{g_{ds2} + g_{m4}}. \tag{3.65}$$

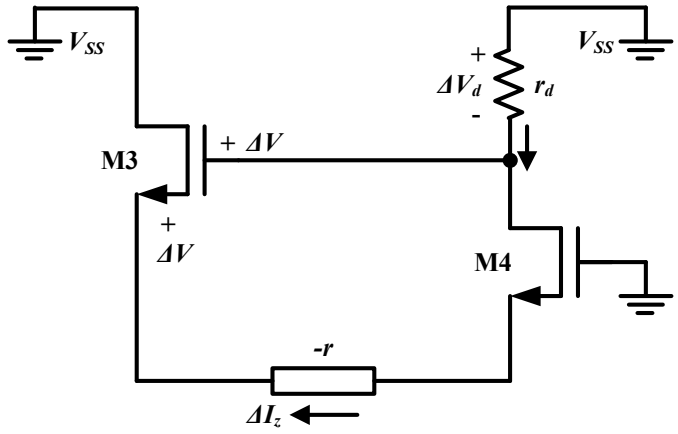


Figure 3.9: Small-signal circuit of $Q$-enhanced inductor for stability analysis.

Note that if $g_{ds1}$, $g_{ds2}$, $C_{gd1}$ and $C_{gd2}$ are neglected, then corrected equations of the elements match with those obtained using simple transistor models.

## 3.2 Inductance and Stability Analysis of *Q*-Enhanced Active Inductor

As an active circuit incorporating both positive and negative feedbacks, the development of inductance, and the stability of the proposed inductor are important design considerations. Using more general approaches, the development of inductance for the proposed $Q$-enhanced active inductor can be explained with a small-signal model of Figure 3.9. The cross-coupled transistor pair (M1 and M2) creates negative impedance (or resistance) -$Z$ (or -$r$). Assuming the potential at the gate of transistor M3 increases by $\triangle V$, it will be repeated at the source of transistor M4, and will provide current $\triangle I_Z$ flowing into the source of transistor M3, which acts as the source-follower. Current $\triangle I_Z$ is approximately equal to -$\triangle V/r$ where $r$ is expressed as

$$r = -\frac{g_{m1} + g_{m2}}{g_{m1} \cdot g_{m2}}. \tag{3.66}$$

Current $\triangle I_Z$ will be repeated in the drain of M4, and a voltage-drop of $\triangle V_d$

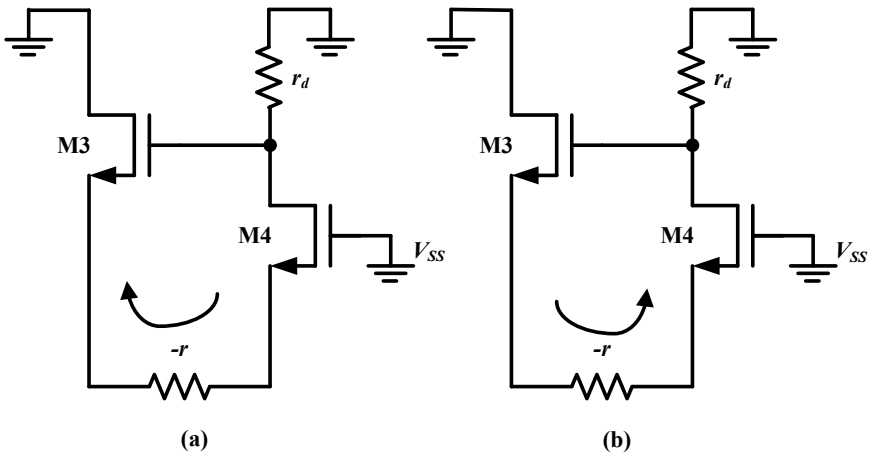


Figure 3.10: (a) Positive feedback loop, (b) negative feedback loop.

will occur across $r_d$, the total node resistance with a negative sign at the drain of M4. $\triangle V_d$ tries to cancel $\triangle V$, and this implies that there exists a negative feedback. Negative resistance -$r$ between the sources of M3 and M4 provide a positive feedback loop as shown in Figure 3.10 (a). This negative-resistance also creates a negative feedback loop that includes transistors M3 and M4 as shown in Figure 3.10 (b). One can find the loop gain, $A_{loop}$,

$$A_{loop} \approx -\frac{r_d}{r}. \tag{3.67}$$

Hence, the operation of this circuit as an inductor where inductance seen from the source of M3 is explained in the following way with figure 3.11(a). The existence of node capacitance $C_d$ parallel with $r_d$ gives impedance $Z_d$ as

$$Z_d(s) = \frac{r_d}{1 + C_d r_d s}. \tag{3.68}$$

Now, source-current $i$ sees the impedance $Z_i$ as

$$Z_i(s) \cong \frac{1}{g_{m3}} \frac{1}{1 + \frac{Z_d}{r}}. \tag{3.69}$$

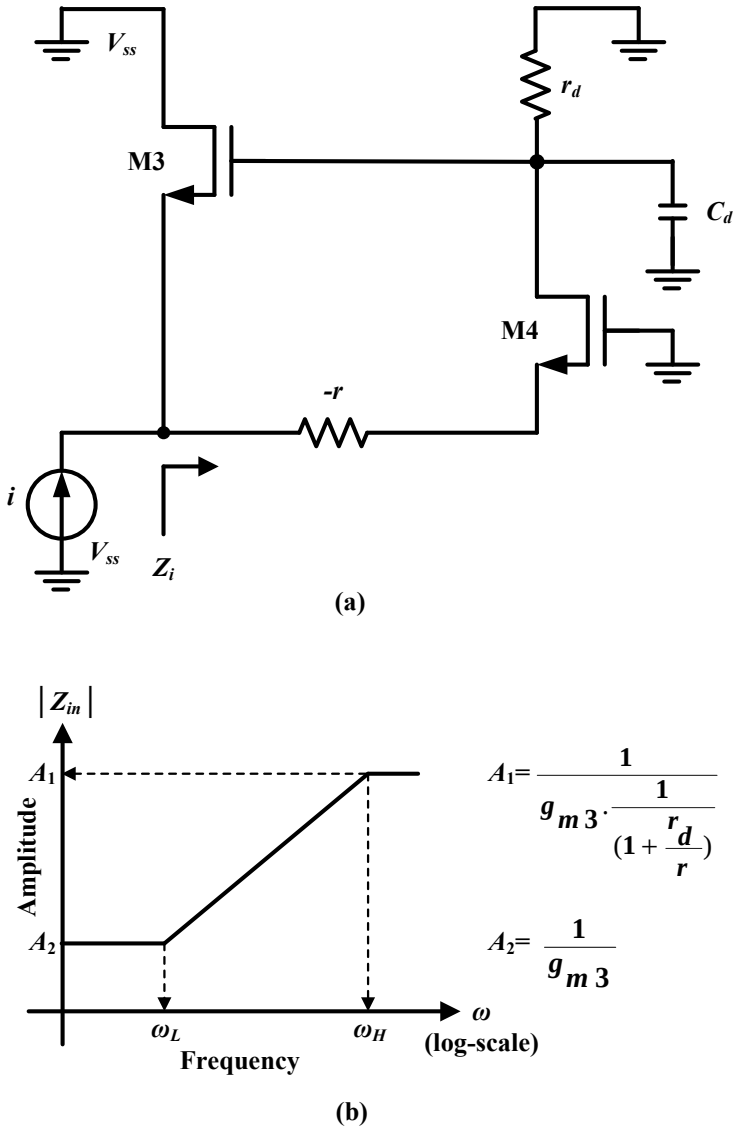


Figure 3.11: (a) Small-signal circuit for input impedance $Z_{in}$ of active inductor, (b) bode plot of $Z_{in}$.

$$Z_i(s) = \frac{1}{g_{m3}} . \frac{1 + C_d r_d s}{(1 + \frac{r_d}{r}) + C_d r_d s}. \tag{3.70}$$

The bode plot of 4.16 is shown in Figure 3.11(b). Note that at LF and

HF, $Z_i$ is resistive because it remains constant. Over MF range, $Z_i$ increases with frequency and hence, it is inductive. The lower and upper limits of the inductive impedance are set by $\omega_L$=$1/C_d r_d$ and $\omega_H$=$1/C_d r$ respectively. In inductive region, $Z_{i,ind}$ is obtained as

$$Z_{i,ind}(s) \approx \frac{1}{g_{m3}}.\frac{C_d r_d s}{1+\frac{r_d}{r}} = sC_d r.\frac{1}{g_{m3}}, \tag{3.71}$$

and

$$Z_{i,ind}(s) \approx \frac{sC_d(g_{m1}+g_{m2})}{g_{m1}g_{m2}g_{m3}}. \tag{3.72}$$

Hence, equivalent inductance $L_{eq}$ is

$$L_{eq} \approx \frac{C_d(g_{m1}+g_{m2})}{g_{m1}g_{m2}g_{m3}}. \tag{3.73}$$

For $g_{m1}$ is to be significantly greater than $g_{m2}$, $L_{eq}$ is approximated as

$$L_{eq} \approx \frac{C_d}{g_{m2}g_{m3}}. \tag{3.74}$$

Here, the expression of $L_{eq}$ yields the classical gyrator-$C$ configuration, and in case of the proposed $Q$-enhanced active inductor, $C_d$ is replaced with $C_{gs3}$, which is gate-source capacitance of transistor M3.

For stability analysis, consider the circuit of Figure 3.12(a) which represents the elements of $Z_i$. Here, a unity-gain voltage-amplifier ($A_v$=1) and a unity-gain current-amplifier ($A_i$)=1) are used. At node 1, the nodal equations of currents gives

$$v_d.(1+r_d C_d s) = ir_d v_d + r_d C_d.\frac{dv_d}{dt} = ir_d. \tag{3.75}$$

Since $i$ also equals -$v_d/r$ and this gives

$$v_d(1+\frac{r_d}{r}) + r_d C_d.\frac{dv_d}{dt} = 0. \tag{3.76}$$

Hence, from equations 3.75 and 3.76, the characteristic equation is obtained

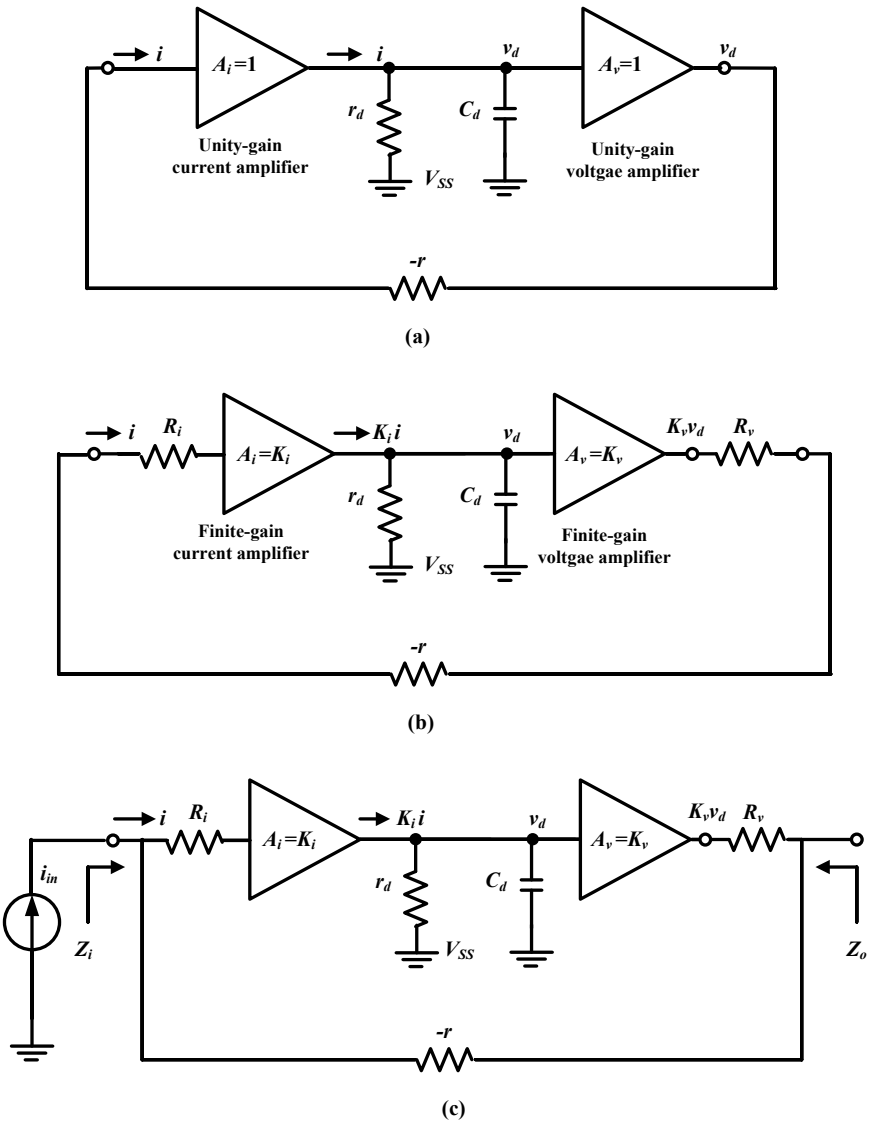


Figure 3.12: (a) Circuit with an ideal amplifier, (b) circuit with a finite-gain amplifier, (c) circuit for input and output impedances.

as

$$(1 + \frac{r_d}{r}) + r_d C_d s = 0. \tag{3.77}$$

Solving of Equation 3.77 for $s$ gives

$$s = -\frac{1 + \frac{r_d}{r}}{r_d C_d}. \tag{3.78}$$

Note that $s$ remains in the left half plane, and hence, the system is stable. The use of such a stable system with finite-gain amplifiers, which have finite input or output impedances, is explained with modified Figure of 3.12(b). $K_i$ and $K_v$ are current and voltage gain of current and voltage amplifiers respectively. $R_i$ is the input resistance of the current amplifier and $R_v$ is the output resistance of the voltage amplifier. Hence, voltage $v_d$ and current $i$ can be expressed as

$$v_d + r_d C_d \frac{dv_d}{dt} = k_i r_d . i, \tag{3.79}$$

and

$$i = \frac{k_v v_d}{R_v + R_i - r}. \tag{3.80}$$

Replacing $i$ in Equation 3.79 gives

$$v_d(1 + \frac{K_i K_v r_d}{r - R_v - R_i}) + r_d C_d \frac{dv_d}{dt} = 0. \tag{3.81}$$

Solving of Equation 3.81 for $s$ gives

$$s = -\frac{1}{r_d C_d}(1 + \frac{K_i K_v r_d}{r - R_v - R_i}). \tag{3.82}$$

Note that $s$ will be negative if $r>(R_v+R_i)$, and this is the design condition for the stable operation of the proposed active inductor. For $r \gg (R_v+R_i)$ and r$\gg r_d$,

$$s \approx -\frac{K_i K_v}{r C_d}. \tag{3.83}$$

For the condition of $r>(R_v+R_i)$, the characteristics of input and putput impedances using Figure 3.12(c) can be explained. Input impedance $Z_i$ is expressed as

$$Z_i(s) \cong \frac{R_i}{1 + \frac{K_i K_v}{r - R_v - R_i} . \frac{1}{C_d s}}. \tag{3.84}$$

At LF, $Z_i$ becomes

$$Z_{i,LF}(s) \approx \frac{R_i(r - R_v - R_i C_d)s}{K_i K_v}. \tag{3.85}$$

Hence, $Z_{i,LF}$ has the inductive component, and the equivalent inductance is

$$L_{ei} \approx \frac{R_i(r - R_v - R_i)C_d}{K_i K_v}. \tag{3.86}$$

## 3.3 Implementation and Measurement of *Q*-Enhanced Active Inductor

### 3.3.1 Design Implementation

The proposed $Q$-enhanced tunable active inductor (Figure 3.4) is designed and implemented using STMicroelectronics 90nm CMOS digital CMOS process. The current-source $I$ is replaced with a PMOS device, whose gate is driven by an external control voltage, $V_{con}$. Small width ($W$) minimum length ($L$) transistors contribute low capacitances (gate-source, gate-drain and other parasitic capacitances) that ensure an increased operating frequency for active inductors while consuming a small-amount of power. Therefore, the proposed $Q$-enhanced active inductor is optimized using small-width and minimum-length transistors with $W$ in the range of 1.5$\mu$m to 5.0$\mu$m while all of them have $L$ of 100nm. Typically, these sizes of transistors provide transconductances, conductances and capacitances with units of mS(mA/V), $\mu$S ($\mu$A/V) and fF (femto Farad) respectively. Table 3.1 summarizes the widths and lengths of the transistors of the proposed active inductor (Figure 3.4), which is optimized for enhanced $Q$ and increased operating frequency. The PMOS transistor, namely transistor MI for the current-source $I$ is chosen with $W$ and $L$ of 1.2$\mu$m and

Table 3.1: Device sizes for $Q$-enhanced active inductor

| | M1 | M2 | M3 | M4 | MI |
|---|---|---|---|---|---|
| $W$ ($\mu$m) | 2.5 | 5 | 2.5 | 1.5 | 1.2 |
| $L$ (nm) | 100 | 100 | 100 | 100 | 100 |

100nm, respectively.

Fabricated in STMicroelectronics 90nm CMOS digital process, the die photo of the proposed $Q$-enhanced active inductor (Figure 3.4) with testing (or bonding) pads is shown in Figure 3.13. The core chip-area of the active inductor (AI-the black rectangular box in Figure 3.13), excluding bonding pads is 0.00036mm$^2$ (14$\mu$m $\times$ 26$\mu$m).

### 3.3.2 Measurement Techniques, Setups and Results

Typically, inductors are measured for scattering parameters (S-parameters) using a Vector Network Analyzer (VNA), a two-port RF measuring equipment. Then, measured S-parameters are converted into impedance parameters (Z-parameter) or admittance parameters (Y-parameter) for the extraction of inductance values. Here, the fabricated active inductor is a one-port circuit. Therefore, the VNA measures input-return loss ($S_{11}$) which is the reflection due to the mismatch between the impedance of the VNA (typically 50$\Omega$), and the input impedance of the active inductor. $S_{11}$ in terms of Z-parameter is mathematically expressed as [29]

$$S_{11} = \frac{Z_{11} - Z_0}{Z_{11} + Z_0}, \tag{3.87}$$

$Z_0$ is the characteristics impedance, which is 50$\Omega$ in the measurement system. $Z_{11}$ is the impedance looking into the input of the active inductor, and is expressed in terms of $S_{11}$ as

$$Z_{11} = Z_0.\frac{1 + S_{11}}{1 - S_{11}}. \tag{3.88}$$

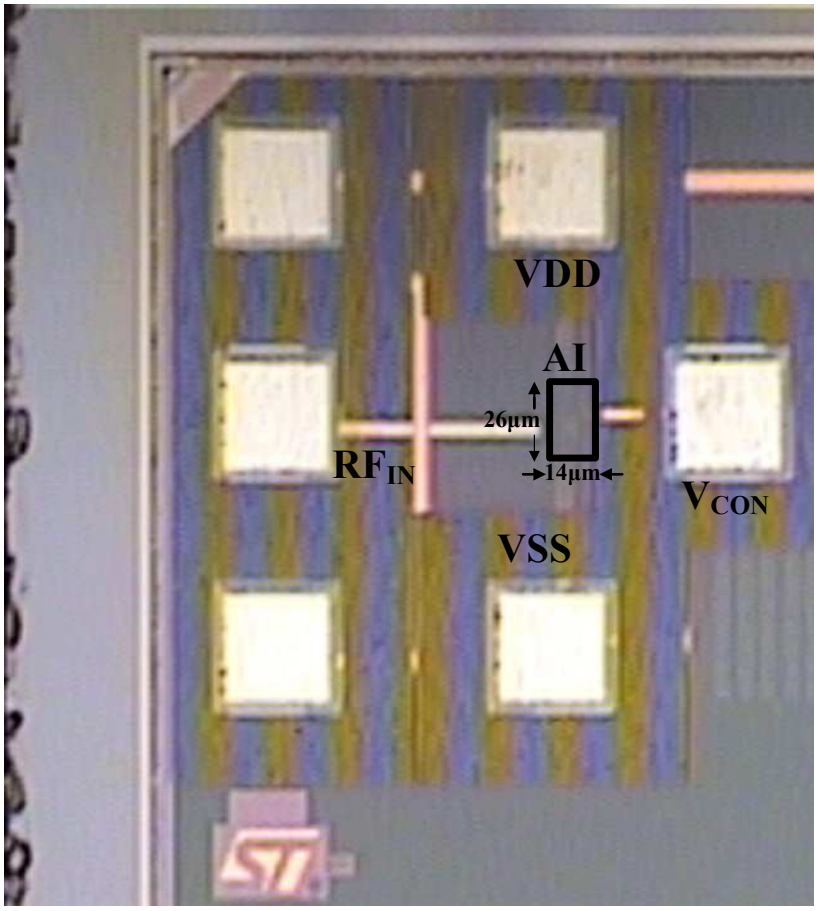


Figure 3.13: Microphotograph of fabricated $Q$-enhanced active inductor.

Impedance $Z_{11}$ has reactive and real parts where the reactive part $\mathrm{Im}(Z_{ind})$ is inductive, and the real part $\mathrm{Re}(Z_{ind})$ is resistive. Inductance ($L_s$) and quality factor $Q$ are calculated using $\mathrm{Im}(Z_{ind})$ and $\mathrm{Re}(Z_{ind})$ as

$$L_s = \frac{Im(Z_{11})}{\omega} = \frac{Im(Z_{11})}{2\pi f}, \tag{3.89}$$

and

$$Q = \frac{Im(Z_{11})}{Re(Z_{11})}, \tag{3.90}$$

where $\omega$ is the angular frequency in rad/sec and $f$ is the frequency in Hz.

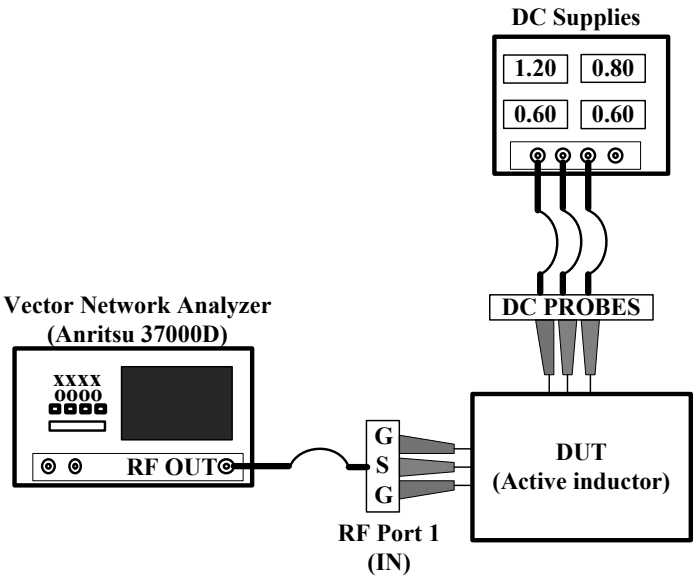


Figure 3.14: Measurement setup for measuring S-parameter ($S_{11}$) of active inductors.

Figure 3.14 shows the on-wafer measurement setup for the fabricated one-port active inductor as the DUT (device under test) to obtain input-return loss $S_{11}$ at port 1 (input RF port). The inductor is measured using a GSG (ground-signal-ground) probe touching down the input RF port of the active inductor (Figure 3.14). Operated with a 1.2V supply, the fabricated tunable active inductor draws a current of 365$\mu$A for control-voltage $V_{con}$ of 600mV while it draws a current of 380$\mu$A in simulation. For the tuning of the active inductor, $V_{con}$ is varied from 400mV to 700mV.

Figure 3.15 shows the measured and simulated frequency responses of magnitude and phase angle of inductive impedance ($Z_{ind}$) of the active inductor for $V_{con}$ of 600mV. The measured peak amplitude of magnitude($Z_{ind}$) is 14.8k$\Omega$ at 12.85GHz whereas the simulated peak amplitude is 15.8k$\Omega$ at 13.4GHz. The positive phase angle starting from a few hundred MHz to 12.5GHz and over ensures the existence of inductive impedance over a wide frequency range. Figure 3.16 shows the measured frequency responses of real and reactive parts of $Z_{ind}$ along with the simulated responses. The real part Re($Z_{ind}$) is resistive,

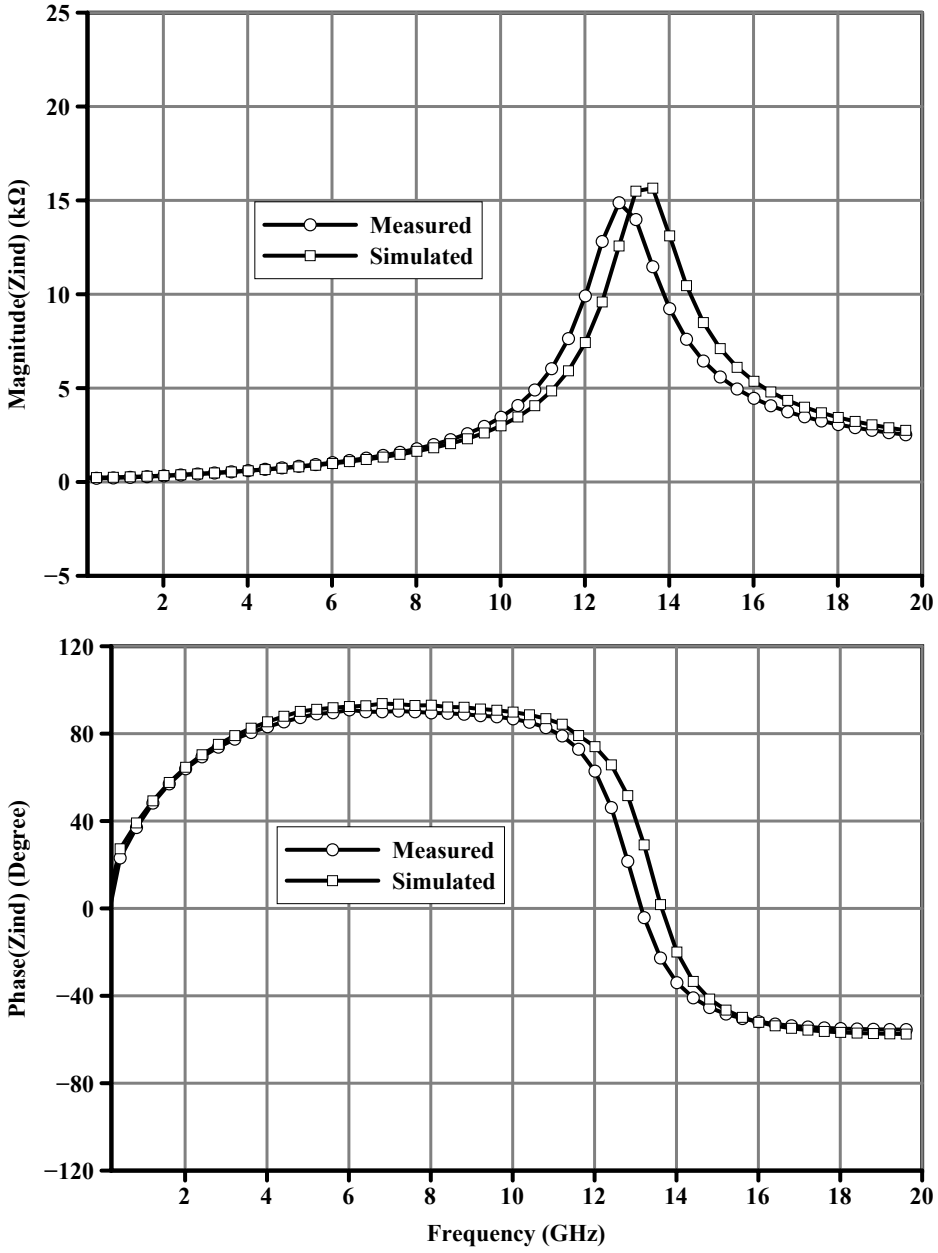


Figure 3.15: Measured magnitude and phase of inductive impedance ($Z_{ind}$) over frequency.

and remains relatively constant up to 10.5GHz. Positive resistance ensures the stable operation of the inductor. The imaginary part Im($Z_{ind}$) increases slowly with frequency indicating the wide inductive operating range in excess of 10.0GHz. The zero-crossing frequency of Im($Z_{ind}$) (=0) is the resonance frequency ($f_0$) and here, the measured $f_0$ is 13.7GHz

Figure 3.17 shows the measured frequency characteristics of inductance ($L_s$) and $Q$ of the active inductor along with the simulated results. Starting from a low frequency, the inductance changes slowly and linearly up to 10.0GHz, and the maximum inductance obtained is 120.0nH at 12.2GHz (measured). The $Q$ of the active inductor also increases with frequency, and the maximum $Q$ is obtained over 220.0 at the frequency of 8.7GHz, which is well below the resonance frequency, $f_0$ (=13.7GHz). Around $f_0$, the rising and falling of the inductance are sharp. As inductance approaches resonance frequency, the active inductor exhibits a low $Q$ yielding a high resistance of Re($Z_{ind}$) (Fig. 3.16). At $f_0$, both $Q$ and $L_s$ are zero (zero crossing line) indicating Re($Z_{ind}$) (resistance) is very high and Im($Z_{ind}$) is very low. Thus, the $Q$ of the active inductor becomes very small (almost zero) at $f_0$. Above $f_0$, inductance exhibits capacitive characteristics (negative inductance)indicating the capacitance of the active inductor dominates the inductance. Note that the measured $Q$ is higher than the simulated ones. This is because the measured $L_s$ has a higher value with a reduced $f_0$.

Figure 3.18 shows the measured inductance ($L_s$) of the $Q$-enhanced active inductor over frequency for different voltages (400mV to 700mV) of $V_{con}$. Note that the resonance frequency (the zero-crossing frequency of the inductances) is tuned from 11.4GHz to 14.2GHz for $V_{con}$ of 400mV to 700mV. It is also note that the $Q$-enhanced inductor achieve a wide inductance bandwidth ($BW$) (linear region of inductance variation) of 300MHz to 12.1GHz for $V_{con}$ of 400mV.

Figure 3.19 shows the tuning of the measured $L_s$ and $f_0$ as a function of control voltage $V_{con}$ (350mV to 800mV). Note that $L_s$ varies from 17.0nH to 40.0nH at 5.0GHz, and with increasing operating frequency, the variation of $L_s$ increases further. At 10.0GHz, $L_s$ varies from 33.0nH to 93.0nH. The

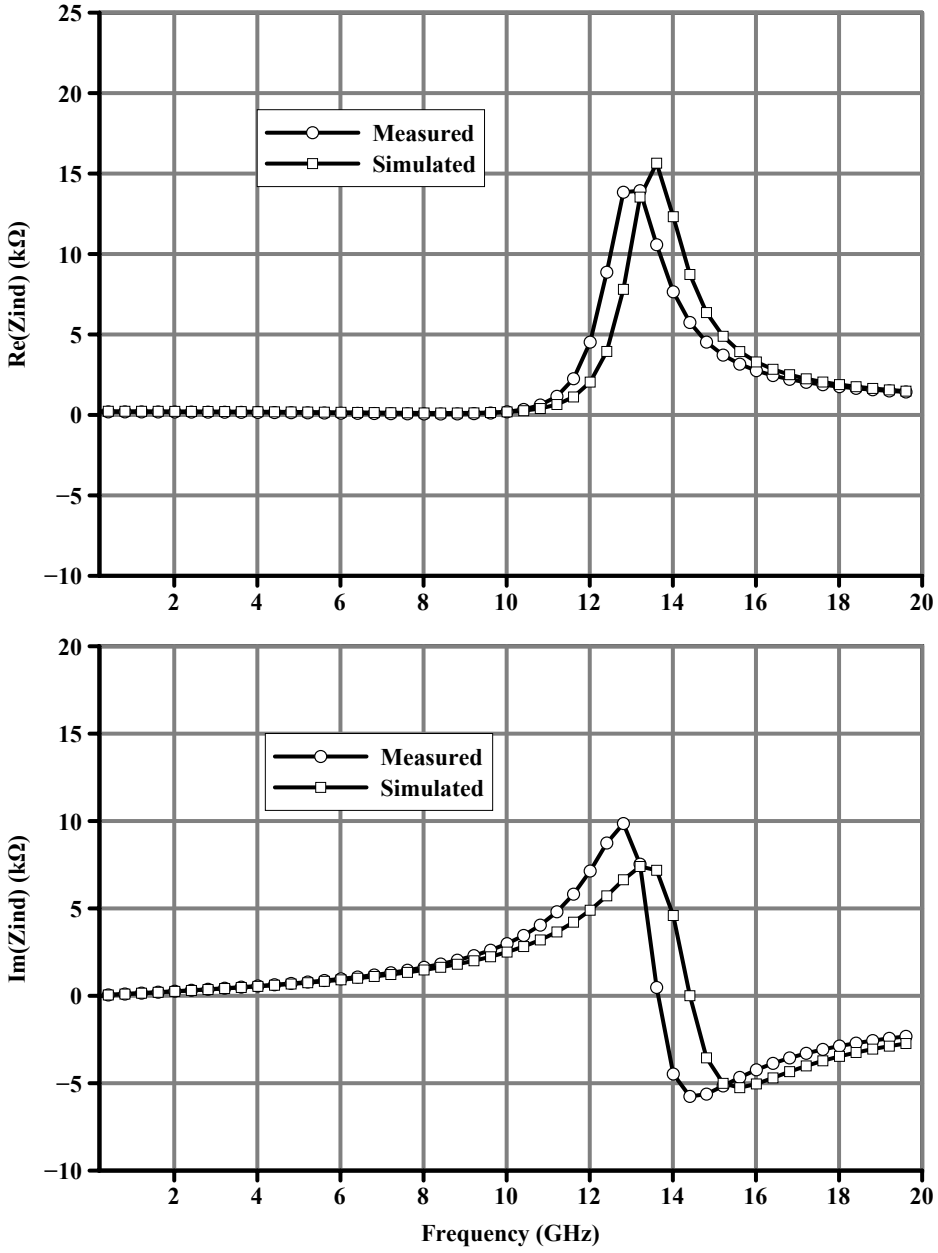


Figure 3.16: Measured real and imaginary parts of inductive impedance ($Z_{ind}$) over frequency.

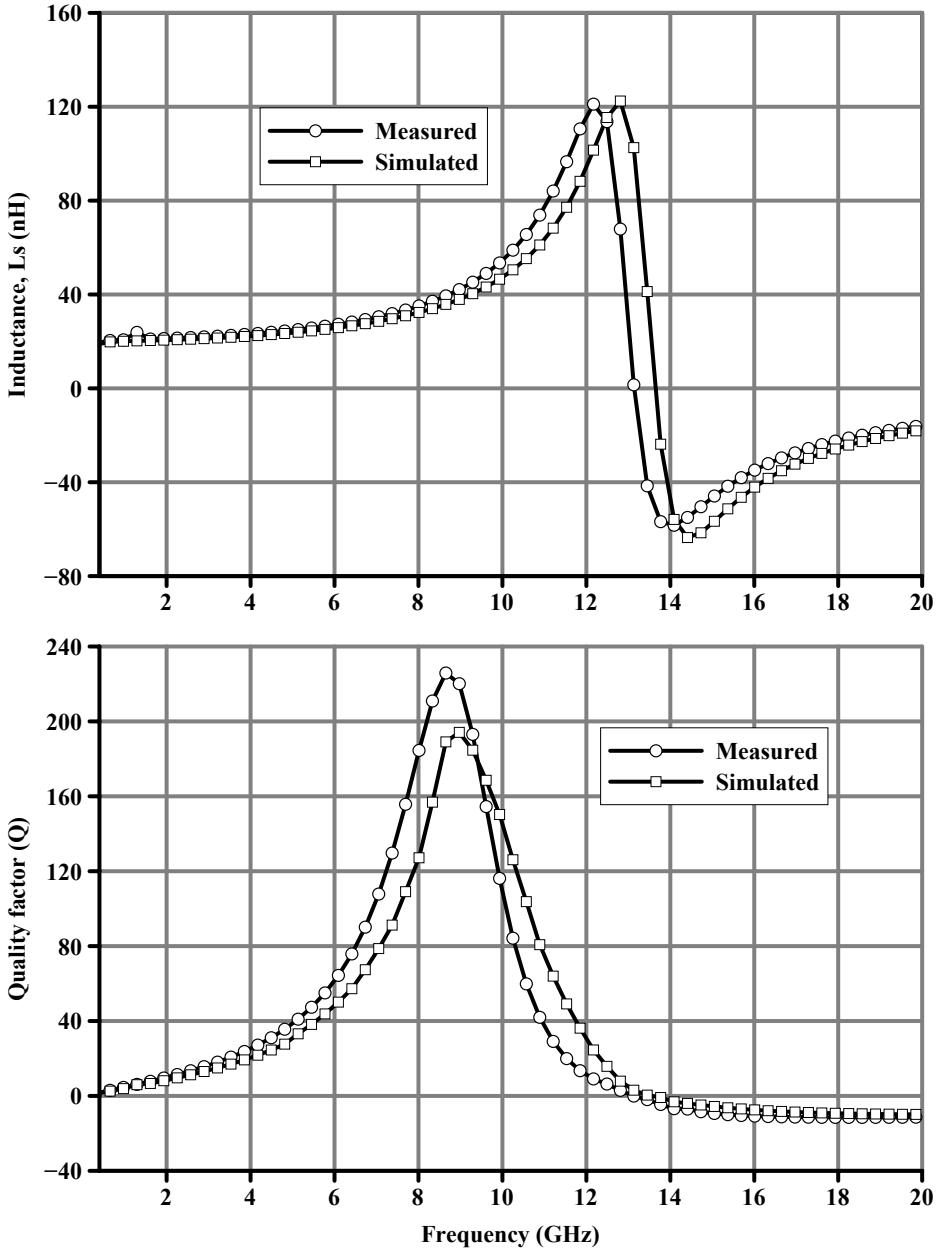


Figure 3.17: Measured inductance ($L_s$) and $Q$ over frequency.

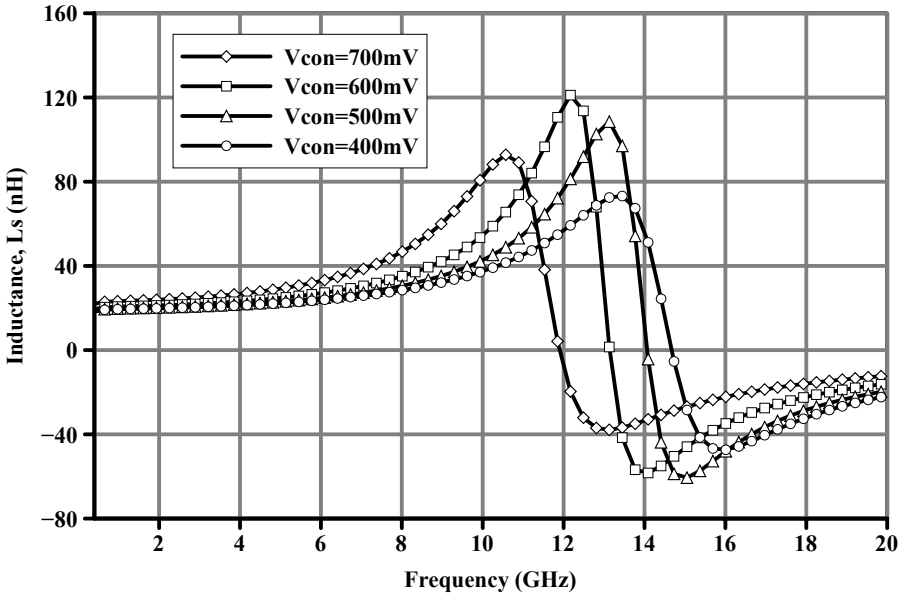


Figure 3.18: Measured inductance ($L_s$) over frequency for different control voltages ($V_{con}$).

measured resonance-frequency $f_0$ is tuned from 8.9GHz to 14.3GHz (Fig. 3.19). Figure 3.20 shows the measured $Q$ as a function of control voltage $V_{con}$, and the maximum $Q$ (220.0) is obtained at 600mV. Table 3.2 summarizes the measured and simulated results of the proposed $Q$-enhanced active inductor (Ind.).

There are discrepancies between measured and simulated results. The $Q$-enhanced active inductor is designed and simulated using the normal digital transistors. One of the discrepancies between measured and simulated results is due to model inaccuracies at high RF frequencies. The measurement errors (de-embedding errors) over a wide frequency-range (200MHz-20.0GHz) also causes discrepancies between measured and simulated results. In measurement, a slightly reduced amount of current is drawn than it is drawn in simulation because of the contact resistances between probe-tips and bonding pads (power supply pads $V_{DD}$ and $V_{SS}$), and the resistances of interconnects wires inside the active inductor. This also causes the measured results to be deviated from the simulated ones.

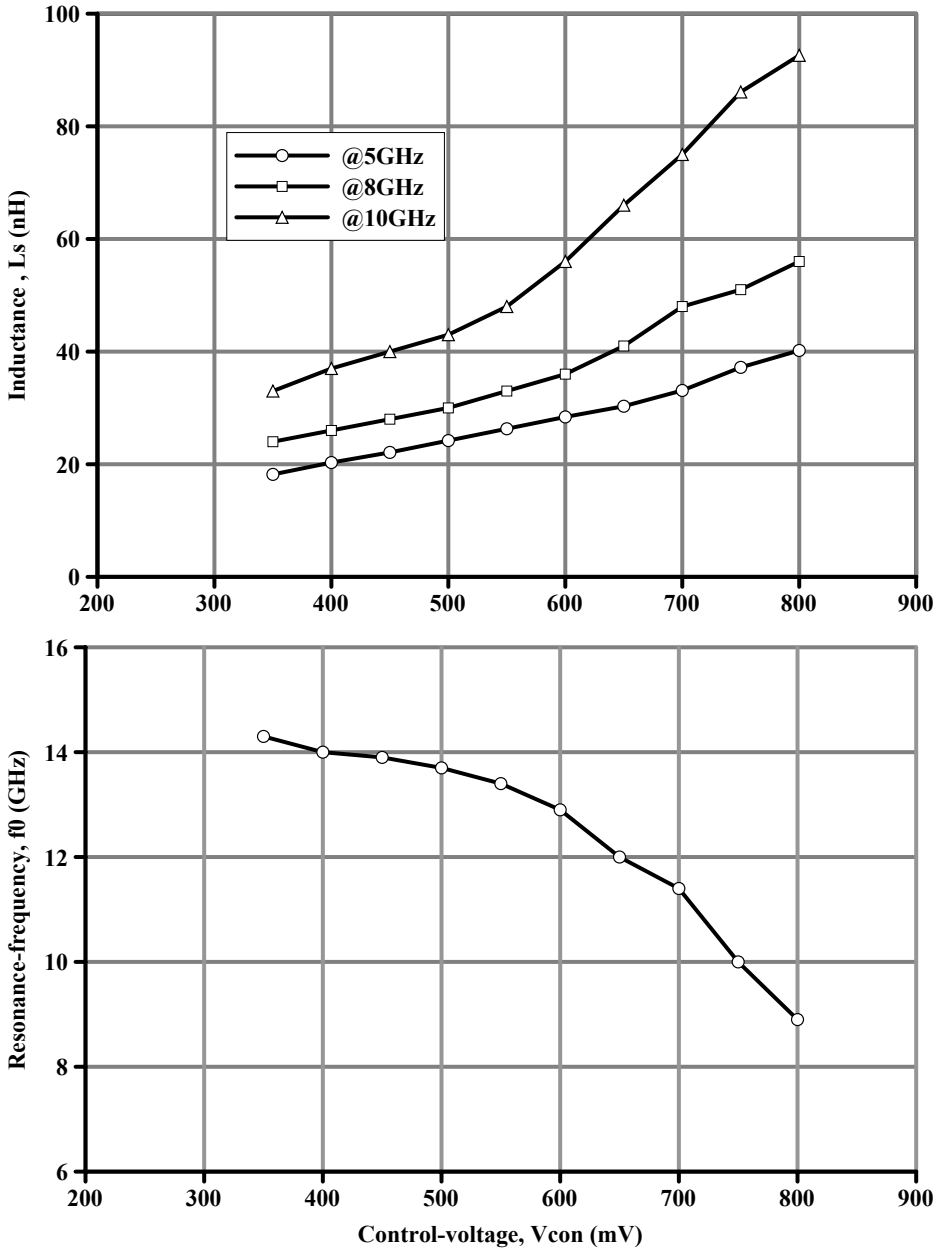


Figure 3.19: Measured inductance ($L_s$) and resonance-frequency ($f_0$) over control voltage ($V_{con}$).

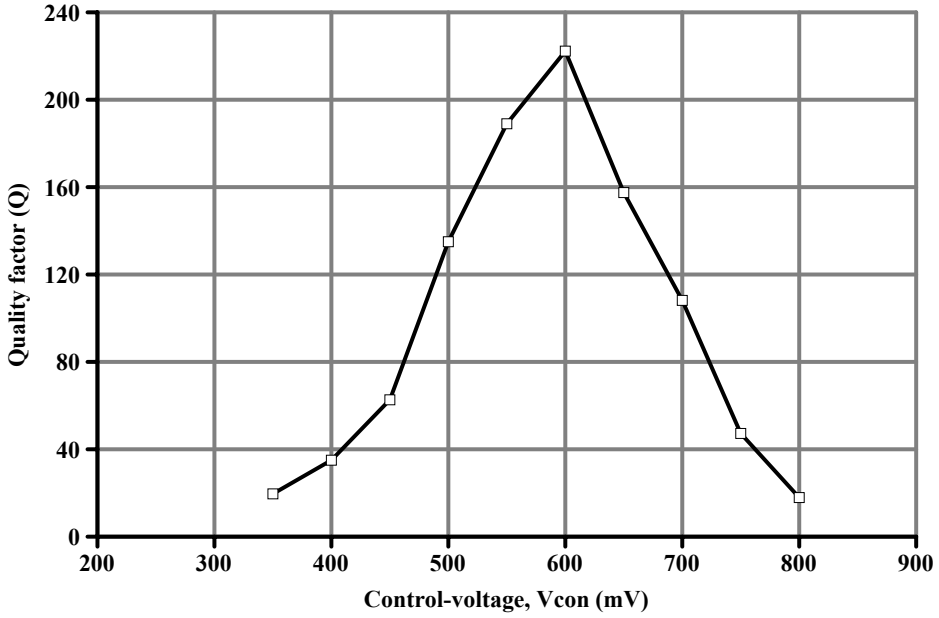


Figure 3.20: Measured $Q$ over control voltage ($V_{con}$).

Table 3.2: Simulated and measured results of $Q$-enhanced inductor.

| | Ind. tuning range (nH) | Max. Ind. $BW$ (GHz) | $Q_{max}$ | $f_0$ tuning range (GHz) |
|---|---|---|---|---|
| Simulated | 14.0-118.0 | 0.2-14.0 | 190.0 | 9.0-15.2 |
| Measured | 16.0-120.0 | 0.2-13.1 | 220.0 | 8.8-14.3 |

## 3.4 Proposed Bandwidth-Extended CMOS Active Inductor

The proposed $Q$-enhanced active inductor (Figure 3.4) employing negative and positive feedbacks exhibits high $Q$ (over 220.0), high inductance ($L_s$) (over 100.0nH) and limited inductive bandwidth (from a few hundred MHz to over 10.0 GHz). In this active inductor, the combined gate-source capacitance ($C_{gs1}$+$C_{gs4}$) of transistor M1 and M4 at the output node of transistor M2 limits the operating bandwidth and reduces the amount of negative feedback. The

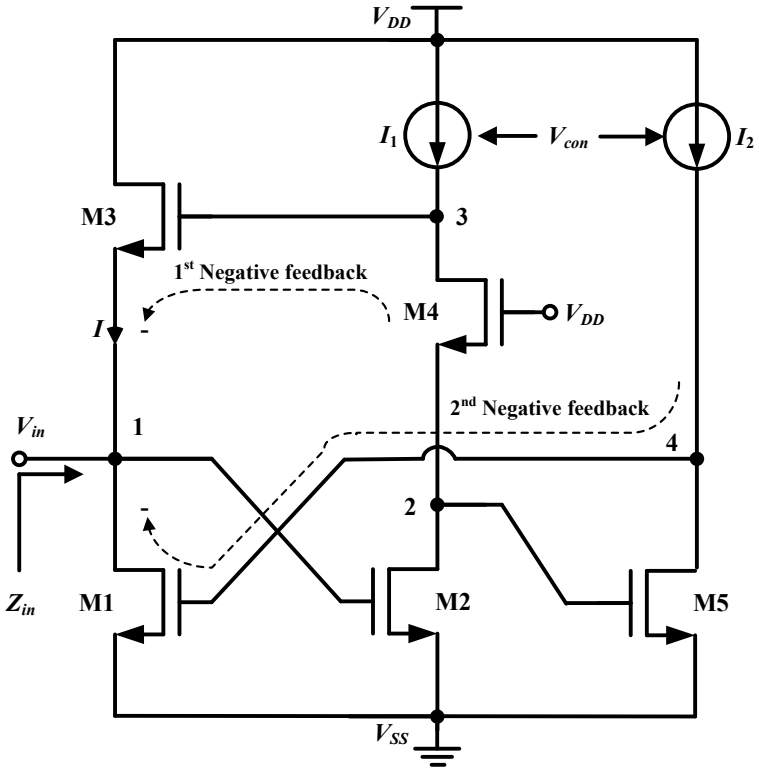


Figure 3.21: Proposed bandwidth-extended tunable CMOS active inductor.

reduced negative feedback increases inductance but decreases the operating bandwidth of the $Q$-enhanced active inductor. Here, a new active inductor for an extended bandwidth is proposed as shown in Figure 3.21 [30] where the amount of negative feedback is increased to increase the inductive bandwidth. In the proposed bandwidth-extended active inductor, instead of using a direct cross-coupled pair of transistors M1 and M2, an additional common-source (consisting of transistor M5 and current source $I_2$) gain-stage is incorporated. This creates the second negative-feedback loop at the input (Node 1) of the active inductor (Figure 3.21). The second feedback loop minimizes the effect of combined gate-source capacitance ($C_{gs1}$ plus $C_{gs4}$) of transistor M1 and M4, and further extends the inductive bandwidth.

As shown in the bandwidth-extended active inductor (Figure 3.21), input voltage $V_{in}$ at Node 1 is converted to a current by transistor M2. This current

flowing through Node 2 charges gate-source capacitance $C_{gs3}$ of transistor M3, and the first negative feedback at the input (Node 1) occurs through transistors M4 and M3. Thus, the inductance is formed resembling the gyrator-$C$ configuration where transistors M2 and M3 form two transconductors ($g_{m2}$ and $g_{m3}$) and $C_{gs3}$ is the required capacitance. The signal from the drain of transistor M2 of the cascode stage is also fed to the gate of transistor M5 of the common-source amplifier and charges the gate-source capacitance $C_{gs5}$ of transistor M5. The charging voltage across $C_{gs5}$ is converted to a current following through Node 4. The drain current of M5 charges gate-source capacitance, $C_{gs1}$ of transistor M1. This charging voltage is converted to a current by transistor M1 appearing as the negative feedback at the input (Node 1). The second negative feedback minimizes the effect of the pole created by the gate-source capacitance $C_{gs4}$ (of transistor M4) and gate-drain conductance $g_{ds2}$, and hence, it increases the inductive bandwidth.

### 3.4.1 Large-Signal Analysis of Bandwidth-Extended Inductor

In the proposed bandwidth-extended active inductor (Figure 3.21), DC operating points and nodal voltages are defined by currents $I_1$ and $I_2$. Assuming all the transistors of the inductor are long-channel devices, and neglecting their body effects, the currents and voltages can obtained using MOSFET large-signal or static analysis. It is assumed that transistors M1, M2, M3 and M4 operate in saturation , and transistor M2 operates in triode. The drain currents ($I_{D2}$ and $I_{D4}$) of transistors M2 and M4 are equal to $I_1$.

$$I_{D2} = I_{D4} = I_1. \tag{3.91}$$

Hence, gate-source voltages of M2 and M4 ($V_{GS2}$ and $V_{GS4}$) are obtained as follows:

$$V_{GS2} = V_{TN} + \sqrt{\frac{2I_1}{K_2}}, \tag{3.92}$$

and

$$V_{GS4} = V_{TN} + \sqrt{\frac{2I_1}{K_4}}, \tag{3.93}$$

where $K_{2,4}$ is

$$K_{2,4} = \mu_n C_{ox}(\frac{W}{L})_{2,4}. \tag{3.94}$$

Thus, gate-source voltage of M5 ($V_{GS5}$) is obtained as

$$V_{GS5} = V_{DD} - V_{GS4} = V_{DD} - V_{TN} - \sqrt{\frac{2I_1}{K_4}}. \tag{3.95}$$

With the assumption of transistor M5 operating in deep triode, current $I_2$ is calculated as

$$I_2 = \mu_n C_{ox}(\frac{W}{L})_5(V_{GS5} - V_{TN}).V_{DS5} = K_5(V_{GS5} - V_{TN}).V_{DS5}. \tag{3.96}$$

Thus, the gate-source voltage of M1 ($V_{GS1}$) is obtained as

$$V_{GS1} = V_{DS5} = \frac{I_2}{K_5(V_{GS9} - V_{TN})} \tag{3.97}$$

This will allow one to find current through transistors M1 and M3 as

$$I_{D1} = I_{D3} = \mu_n C_{ox}(\frac{W}{L})_1(V_{GS1} - V_{TN})^2 = K_1(V_{GS1} - V_{TN})^2. \tag{3.98}$$

Hence, all the currents and voltages in the proposed bandwidth-extended active inductors are defined.

### 3.4.2 Small-Signal Analysis of Bandwidth-Extended Inductor

Using the similar approach of small-signal analysis for $Q$-enhanced active inductor, the bandwidth-extended active inductor can be modeled. Here, in the proposed bandwidth-extended inductor, the additional gain stage (consisting of transistor M5 and current source $I_2$) provides positive gain, and in turn, negative feedback at the input through transistor M1. The small-signal gain

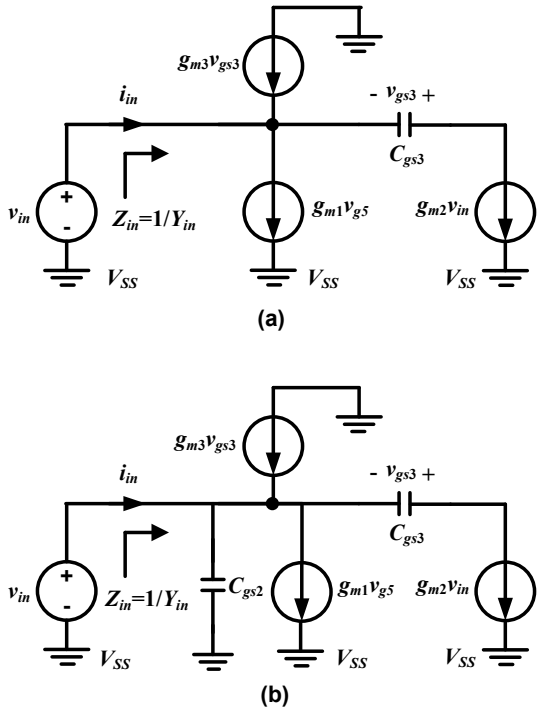


Figure 3.22: (a) Developing small-signal model of bandwidth-extended active inductor, (b) small-signal model with parallel equivalent capacitance.

($A_{v5}$) of this gain stage can be obtained by differentiating Equation 3.96, and equating the result zero. The part of the small-signal model of the active inductor is shown in Figure 3.22 where voltage $v_{g5}$ for the current-source $g_{m1}v_{g5}$ is obtained as

$$v_{g5} = (-\frac{g_{m2}}{g_{m4}}A_{v5})v_{in} \tag{3.99}$$

where $-\frac{g_{m2}}{g_{m4}}$ is the gain of the cascode stage. The input current $i_{in}$ is

$$i_{in} = g_{m1}v_{g5} + g_{m2}v_{in} - g_{m3}v_{gs3}. \tag{3.100}$$

Replacing $v_{g5}$, $i_{in}$ is obtained as

$$i_{in} = [g_{m1}.\frac{g_{m2}}{g_{m4}}(\frac{V_{DS5}}{V_{GS5} - V_{TN}}) + g_{m2} + \frac{g_{m2}g_{m3}}{sC_{gs3}}]v_{in} \tag{3.101}$$

Thus, input admittance $Y_{in}$ is obtained as

$$Y_{in}(s) = \frac{1}{Z_{in}(s)} = \frac{i_{in}}{v_{in}} = G_{oe} + \frac{1}{sL_{oe}} \tag{3.102}$$

where conductance $G_{oe}$ and inductance $L_{oe}$ are

$$G_{oe} = g_{m2}[1 + \frac{g_{m1}}{g_{m4}}.\frac{V_{DS5}}{V_{GS5} - V_{TN}}] \approx g_{m2}, \tag{3.103}$$

and

$$L_{oe} = \frac{C_{gs3}}{g_{m2}g_{m3}}. \tag{3.104}$$

Changing $I_1$ and $I_2$ by external control voltages causes changing of inductance $L_{oe}$. If the effects of gate-source capacitances of transistor M1 and M4 ($C_{gs1}$ and $C_{gs4}$) are neglected, then considering the gate-source capacitance of M2 ($C_{gs2}$), $Y_{in}$ is obtained as

$$Y_{in}(s) = G_{oe} + \frac{1}{sL_{oe}} + sC_{oe} \tag{3.105}$$

where $C_{oe}$ equals $C_{gs2}$. Hence, $Y_{in}$ is parallel $RLC$ circuit. The $Q$ is obtained as

$$Q = \omega_0 C_{oe} R_{oe} = \sqrt{\frac{C_{gs2}}{C_{gs3}}}.\sqrt{\frac{g_{m3}}{g_{m2}}} \tag{3.106}$$

Like $Q$-enhanced active inductor, the bandwith-extended active inductor is also modelled with an equivalent $RLC$ circuit that can provide its parameters.

### 3.4.3 Parameters of Bandwidth-Extended Active Inductor

Taking $C_{gs}$ and $g_m$ ($g_m >> g_{ds}$ and $C_{gs} >> C_{gs}$) into account only, the simplified small-signal circuit of the bandwidth-extended (be) active inductor is shown in Figure 3.23. The input impedance, $Z_{in,be}$ is expressed as

$$Z_{in,be}(s) = \frac{sC_{gs1}C_{gs3}[g_{m4} + (C_{gs4} + C_{gs5})s]}{D_{mai}(s)}, \tag{3.107}$$

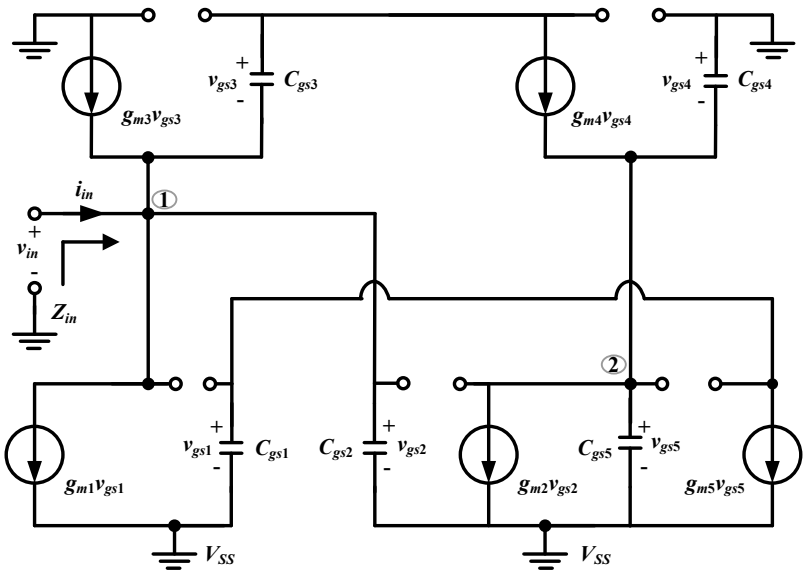


Figure 3.23: Small-signal model of bandwidth-extended active inductor.

where

$$\begin{aligned} D_{be}(s) &= s^3 C_{gs1}C_{gs2}C_{gs3}(C_{gs4}+C_{gs5}) + s^2 C_{gs1}C_{gs2}C_{gs3}g_{m4} + \\ &+ sC_{gs1}C_{gs3}g_{gm2}g_{m4} + g_{m2}(C_{gs1}g_{m3}g_{m4} + C_{gs3}g_{m1}g_{m5}). \end{aligned} \quad (3.108)$$

Neglecting non-dominant terms in the numerator and denominator of $Z_{in,be}$, over mid-frequency (MF) range, $Z_{ind,be}$ can be expressed as

$$\begin{aligned} Z_{ind,be}(s) &\approx \frac{sC_{gs1}C_{gs3}g_{m4}}{s^2 C_{gs1}C_{gs2}C_{gs3}g_{m4} + sC_{gs1}C_{gs3}g_{m2}g_{m4} + g_{m2}(C_{gs1}g_{m3}g_{m4} + C_{gs3}g_{m1}g_{m5})}, \\ &\approx \frac{\frac{s}{C_{gs2}}}{s^2 + s\frac{g_{m2}}{C_{gs2}} + \frac{1}{C_{gs2}}.\frac{g_{m2}(C_{gs1}g_{m3}g_{m4} + C_{gs3}g_{m1}g_{m5})}{g_{m4}C_{gs1}C_{gs3}}}. \end{aligned} \quad (3.109)$$

Here, $Z_{ind,be}$ of the proposed active inductor is also a second-order transfer function representing the impedance of a parallel $RLC$ circuit, and its elements are obtained as follows:

$$L_{s,be} = \frac{C_{gs1}C_{gs3}}{(C_{gs1}g_{m3}g_{m4} + C_{gs3}g_{m1}g_{m5})}.\frac{g_{m4}}{g_{m2}}. \quad (3.110)$$

$$C_{p,be} = C_{gs2}. \tag{3.111}$$

$$R_{p,be} = \frac{1}{g_{m2}}. \tag{3.112}$$

For $C_{gs1}$ equals $C_{gs3}$, the inductance $L_s$ is simplified as

$$L_{s,be} \approx \frac{C_{gs3}}{(g_{m3}g_{m4} + g_{m1}g_{m5})}.\frac{g_{m4}}{g_{m2}}. \tag{3.113}$$

Note that $L_{s,be}$ of the proposed bandwidth-extended inductor is reduced due to the summation term of transcondutances in the denominator. Due to the second feedback loop in the proposed bandwidth extended inductor, the term, $\frac{g_{m4}}{g_{m2}}$ appears in the expression of inductance $L_{s,be}$ (Equation 3.113). Here, for the condition of $g_{m2} > g_{m4}$, $L_{s,be}$ is reduced. Modeling the inductive impedance of the bandwidth-extended active inductor with an equivalent parallel $RLC$ circuit, the resonance frequency ($\omega_{0,be}$) and quality factor ($Q_{be}$) are obtained as

$$\omega_{0,be}^2 = \frac{1}{L_{s,be}C_{p,be}} = \frac{(g_{m3}g_{m4} + g_{m1}g_{m5})}{C_{gs2}C_{gs3}}.\frac{g_{m2}}{g_{m4}}, \tag{3.114}$$

and

$$Q_{be} = \omega_0 R_{p,be}C_{p,be} = \omega_0 \frac{C_{gs2}}{g_{m2}}. \tag{3.115}$$

Here, in the expression of $\omega_{0,be}$, the term $\frac{g_{m2}}{g_{m4}}$ is appeared, and for the condition of $g_{m2} > g_{m4}$, $\omega_{0,be}$ is increased. If $g_{m2}$ becomes two times (2) larger than $g_{m4}$, then $\omega_{0,be}$ is increased by almost one and a half times (1.5). Note that $\omega_{0,be}$ is inversely proportional to the square root of $L_{s,be}$. With the decreasing of $L_{s,be}$, $Q_{be}$ decreases but a high $\omega_{0,be}$ is obtained. Unlike the parameters of the $Q$-enhanced active inductor (Figure 3.4), the parameters of the bandwidth-extended active inductor do not contain the subtraction term of the transconductances ($g_{m1} - g_{m4}$).

Table 3.3: Device sizes for proposed bandwidth-extended active inductor.

| | M1 | M2 | M3 | M4 | M5 |
|---|---|---|---|---|---|
| $W$ ($\mu$m) | 2.5 | 5 | 2.5 | 1.5 | 2.5 |
| $L$ (nm) | 100 | 100 | 100 | 100 | 100 |

## 3.5 Implementation and Measurement of Bandwidth Extended Active Inductor

### 3.5.1 Design Implementation

The proposed bandwidth-extended tunable active inductor (Figure 3.21) is also designed and implemented using STMicroelectronics 90nm CMOS digital CMOS process. Current sources $I_1$ and $I_2$ are implemented using two PMOS transistors, namely transistors MI1 and MI2 with the width ($W$) of 1.0$\mu$m and length ($L$) of 100nm, respectively. Optimized for the extended inductive bandwidth with an increasing operating frequency, the smaller width and the minimum length transistors are chosen. Table 3.3 summarizes $W$ and $L$ of the transistors of the proposed bandwidth-extended active inductor.

Fabricated in STMicroelectronics 90nm CMOS digital process, the bandwidth-extended inductor (Figure 3.21) almost occupies the same chip-area as the $Q$-enhanced inductor because two additional transistors in the modified inductor do not increase its area significantly. The measurement setup and techniques are the same as those of the $Q$-enhanced active inductor.

### 3.5.2 Measurement Results

Operated with a 1.2V supply, the proposed extended broadband active inductor draws a current of 490$\mu$A while it draws a current of 510$\mu$A in simulation. Figure 3.24 shows the measured and simulated frequency responses of the magnitude and phase of the inductive impedance ($Z_{ind}$) of the fabricated bandwidth-extended active inductor for $V_{con}$ of 500mV. Note that the peak amplitude of magnitude($Z_{ind}$) is 12.7k$\Omega$ at 19.4GHz, whereas the simulated peak

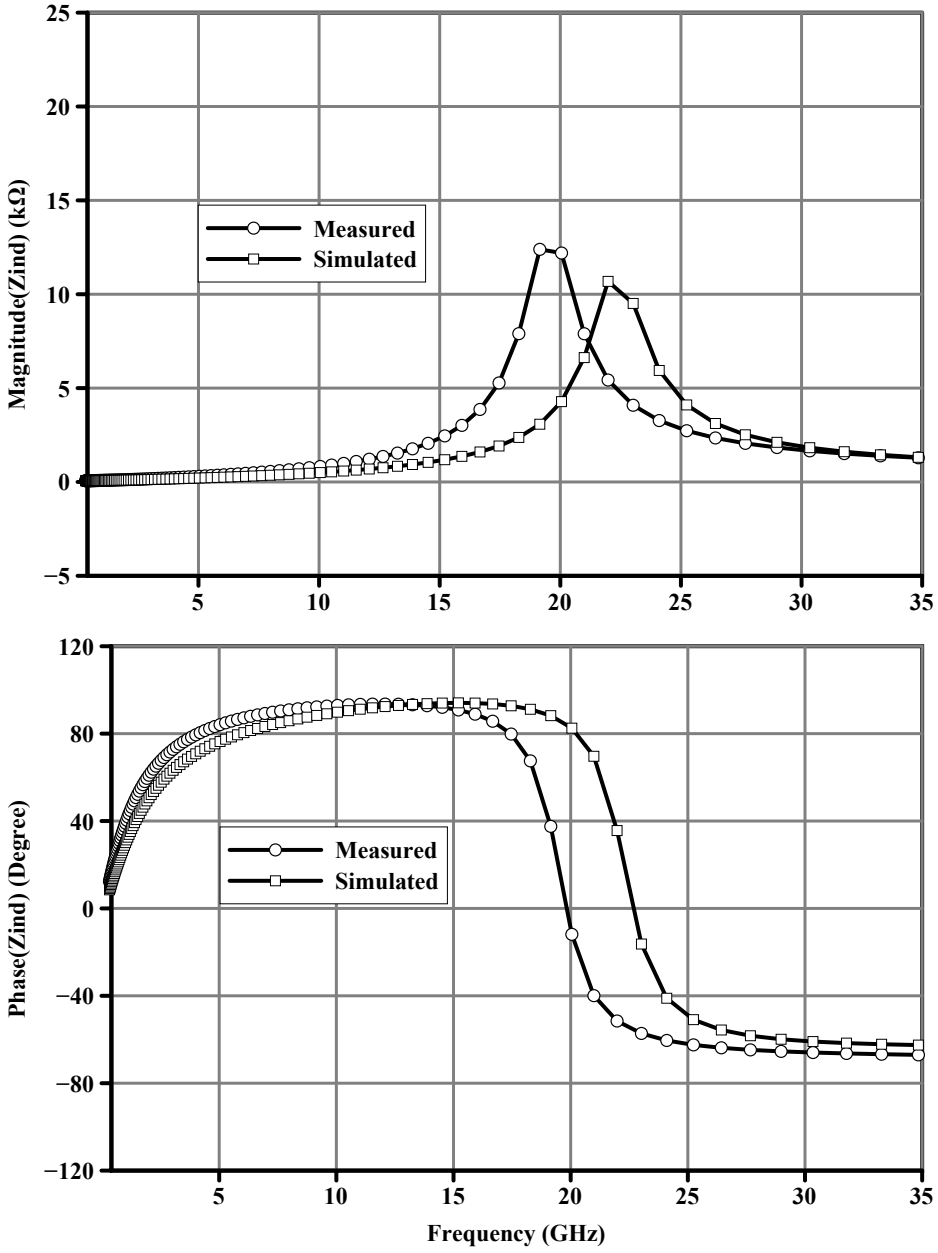


Figure 3.24: Measured magnitude and phase of inductive impedance ($Z_{ind}$) over frequency.

amplitude is 11.0kΩ at 23.0GHz. Hence, the modified active inductor achieves the extended bandwidth but a reduced peak amplitude compared to those of the $Q$-enhanced active inductor. The positive phase-angle Phase($Z_{ind}$) up to the peak amplitude of $Z_{ind}$ ensures the inductive behavior of the active inductor over a wide-frequency range. The measured and simulated resistive and reactive parts of $Z_{ind}$ are shown in Figure 3.25. The measured resistive part, Re($Z_{ind}$) remains very low and constant up to 16.2GHz. The measured reactive part, Im($Z_{ind}$) increases slowly and linearly with frequency up to 15.0GHz, and the resonance frequency ($f_0$) or zero-crossing frequency is 19.9GHz. With increased $f_0$, a wide operating bandwidth for the bandwidth-extended active inductor is obtained.

Figures 3.26 shows the measured frequency characteristics of inductance $L_s$ and $Q$ of the bandwidth-extended inductor for $V_{con}$ of 500mV. At low frequency, $L_s$ remain almost the same but slowly increases with frequency over mid-frequency region. Around resonant peak, the variations of $L_s$ are sharp. Note that at $f_0$, $Q$ is zero, and afterwards, inductance exhibits capacitance (negative inductance) characteristics. Like the $Q$-enhanced active inductor, the measured $Q$ of the bandwidth extended active is also higher than the simulated one because it exhibits higher inductance in measurement with a reduced resonance frequency, $f_0$. Overall, The reasons for the discrepancies between measured and simulated results have already been explained for the $Q$-enhanced active inductor.

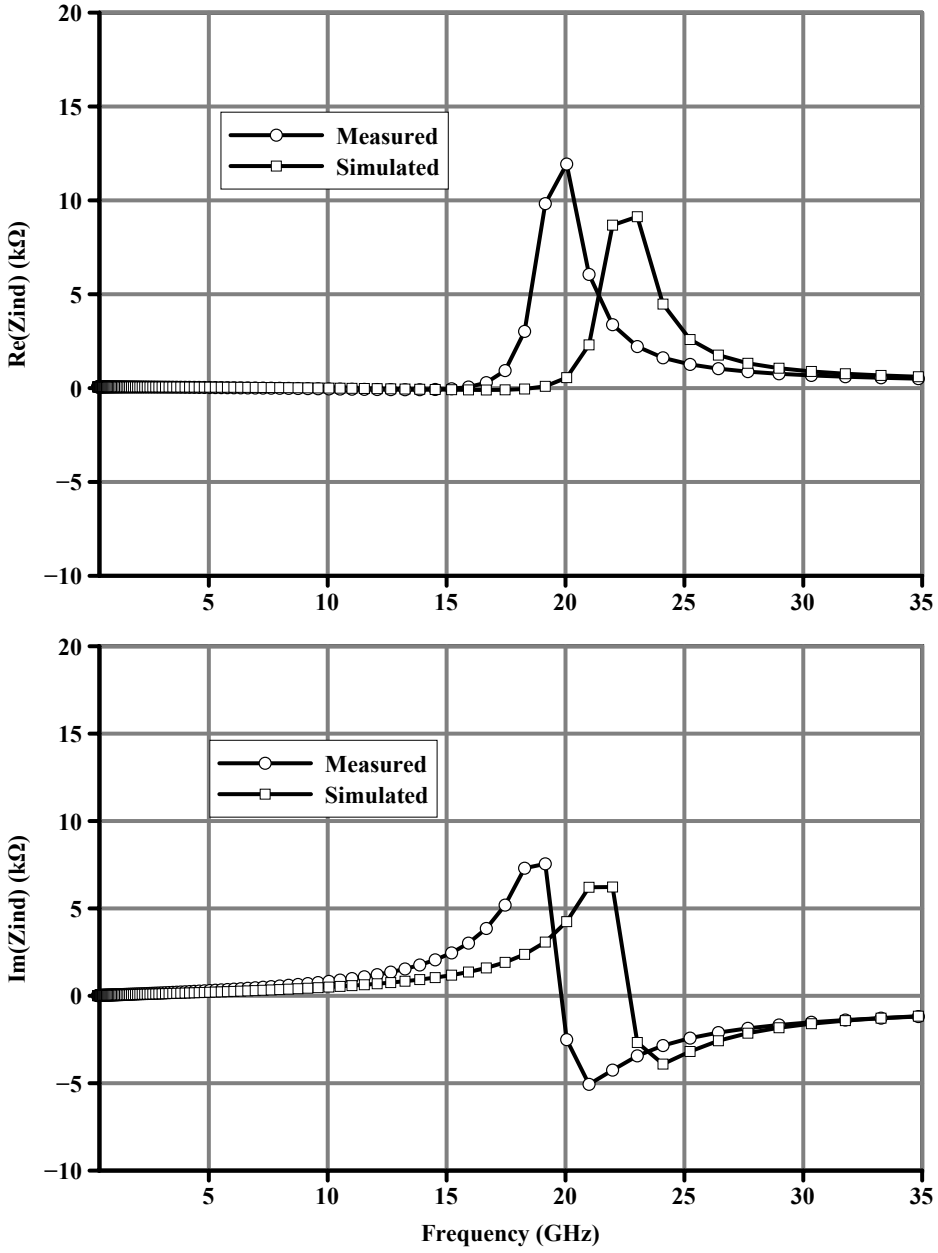


Figure 3.25: Measured real and imaginary parts of inductive impedance ($Z_{ind}$) over frequency.

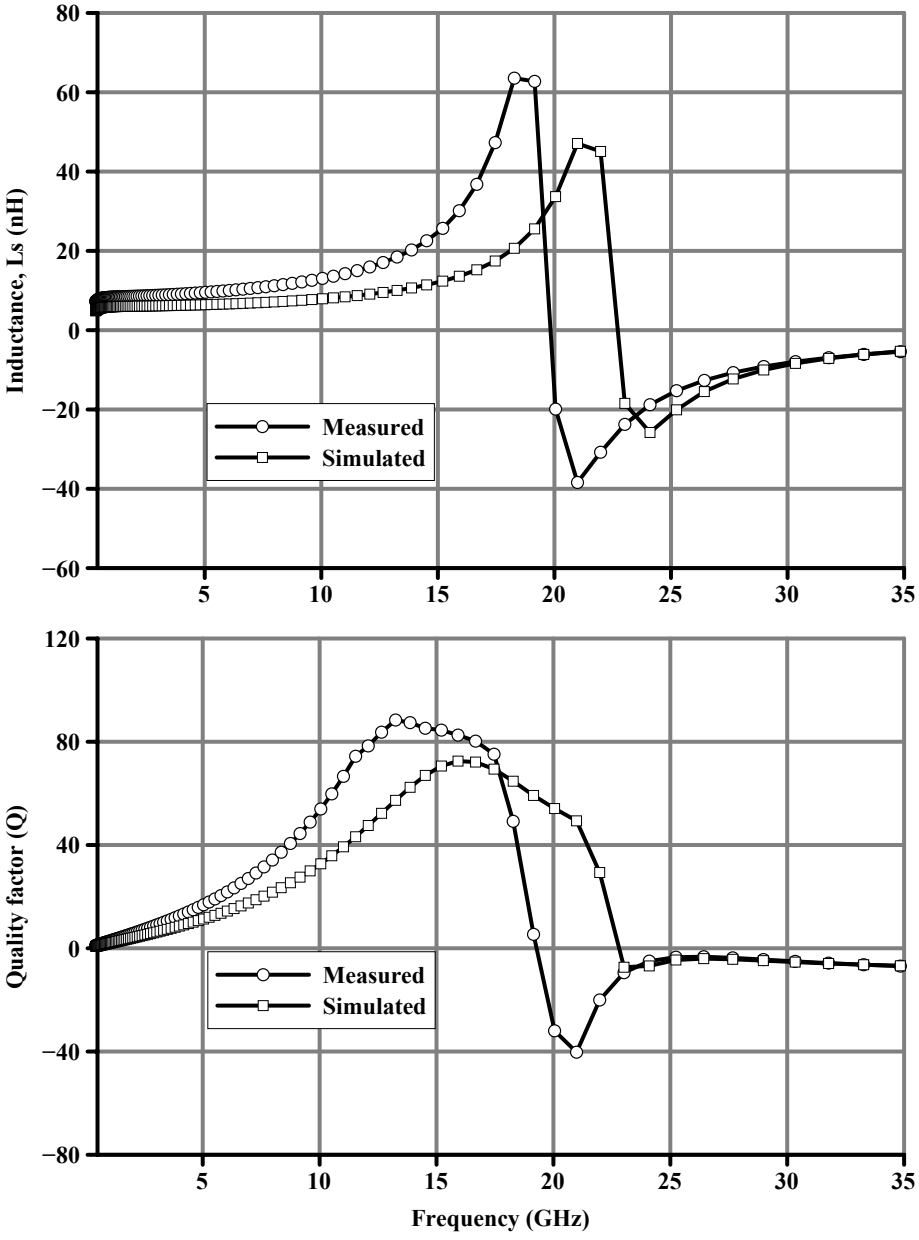


Figure 3.26: Measured inductance ($L_s$) and $Q$ over frequency.

# Chapter 4

# CMOS UWB Low-Noise Amplifiers

In this chapter, two new area-efficient CMOS UWB low-noise amplifiers (LNAs) using very small-area tunable active inductors instead of bulk large-area passive inductors are presented. The proposed LNAs are two-stage and three-stage amplifiers using active inductors to exploit wideband active shunt peaking for bandwidth extension. Fabricated in 90nm digital CMOS processes, the measurement results of the UWB LNAs along with simulated results are presented. In the beginning of the chapter (Section 4.1), an overview of the performance or design parameters of low-noise amplifiers (LNAs) followed by design considerations for, and design examples of ultra-wideband (UWB) LNAs are presented.

## 4.1 Design of UWB Low-Noise Amplifiers

### 4.1.1 Design Parameters of Low-Noise Amplifiers

A low-noise amplifier (LNA) is the first RF building block in a receiver chain to amplify very weak signals with a high gain while contributing a little amount of noise to the system. A low noise for the LNA increases the sensitivity of the receiver [2]. Besides achieving a high gain and contributing a low noise, an LNA also should have a good linearity to accommodate large signals with minimal distortion. Thus, a number of design parameters including gain, noise-figure, bandwidth and linearity, specify the performance of the LNA [2]. These

parameters are also commonly used in describing the performances of other RF circuits in receivers such as mixers and front-ends. Some of the performance parameters as described in the following trade off with each other making it challenging to optimize them simultaneously.

- Gain: Gain (voltage or power gain) is one of the most important performance parameters of RF amplifiers. At RF frequencies, the efficient transmission of signal power is of great importance, and therefore, RF circuits are often specified with power gain instead of voltage gain. For a two-port network with an input impedance of $Z_i$ and an output impedance of $Z_o$, the maximum power transfer occurs when the load impedance ($Z_l$) is conjugate of the source impedance $Z_s$ that is $Z_s$=$Z_i^*$ and $Z_l$=$Z_o^*$ at the input and output ports, respectively [31]. This condition of maximum power-transfer is called the impedance matching. The overall performance of two-port RF circuits are defined using scattering parameters (S-parameters): $S_{11}$, $S_{12}$, $S_{21}$, and $S_{22}$ [29]. $S_{11}$ and $S_{22}$ are the input and output reflection coefficients respectively because of the impedance mismatch at the respective port while the other port is matched. $S_{21}$ and $S_{12}$ represent forward and reverse transmission coefficients respectively with output and input impedances are matched. The forward transmission coefficient $S_{21}$ represents the gain of a two-port network.

- Noise Factor and Noise Figure: Noise limits the level of the minimum detectable signal that a circuit can process with acceptable quality. In analog and RF circuits, the quality of a signal in presence of noise is described by a parameter called Signal-to-Noise Ratio ($SNR$), which is defined as the ratio of the signal power to the total noise power. Quantitatively, the performance of a noisy system is described by *noise factor* ($F$), which is defined as [2]

$$F = \frac{SNR_i}{SNR_o}, \tag{4.1}$$

where $SNR_i$ is the $SNR$ at the input, and $SNR_o$ is the $SNR$ at the output

of a system. The physical meaning of $F$ is how much $SNR$ degrades when a signal passes through a noisy system. For an added noise of $N_a$ from the electronics of the system, and for an input noise power of $N_i$ (noise source), the $F$ is obtained as [1, 2]

$$F = 1 + \frac{N_a}{N_i}. \tag{4.2}$$

Note that the minimum value of $F$ can be 1 when the system adds no noise ($N_a$=0). In circuit design, $F$ is expressed in logarithmic scale (dB) and is referred to as the noise figure ($NF$),

$$NF = 10log_{10}F. \tag{4.3}$$

In a cascaded system of three stages with different gains ($G_1$, $G_2$, $G_3$ ) and noise factors ($F_1$, $F_2$, $F_3$), the overall noise factor $F$- is expressed as [2]

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}. \tag{4.4}$$

Note that in a cascaded system, the $F_1$ of the first-stage is directly added to the overall system $F$ but noise contribution from any stage except the first stage is reduced by the gain of its preceding stage or stages. Therefore, for better noise performance of a cascaded system, along with a high gain the first stage should have the minimum possible $F$.

- Linearity: Aside from gain and $NF$, linearity is an important design consideration for RF circuits and systems because the nonlinearities of RF circuits and systems cause gain compression, cross modulation and intermodulation distortion [10]. A large swing of signal amplitudes at the input of RF circuits causes output signals reaching the saturation level that results in gain compression exhibiting clipped outputs (in case of a sinusoidal input). Cross modulation causes the modulation of a desired signal (weak signal) with an undesired carrier (strong interferer). When

two signals of different frequencies are applied to a nonlinear system, the output contain some frequency components, which are not the harmonics of the input frequencies and cause intermodulation distortion. Typically, the linearity of RF circuits or systems is measured by 1-dB compression point (1-dB $CP$) and third-order intercept point ($IP3$) [2, 3]. The 1-dB $CP$ is defined as the input signal-level for which the small-signal gain (due to fundamental frequency) of RF circuits is decreased by 1-dB in comparison to linear gain. For a single-tone signal (one frequency $\omega_1$) applied to a nonlinear system, the 1-dB $CP$ in logarithmic scale is expressed with the ratio of the actual output voltage $V_o$ to the ideal output (without gain compression) voltage $V_{oi}$ as [2]

$$20log_{10}(\frac{V_o}{V_{oi}}) = -1dB. \tag{4.5}$$

For a two-tone signal containing fundamental frequencies of $\omega_1$ and $\omega_2$, the intermodulation products or tones (due to mixing) are: $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$. $IP3$ is a theoretical point at which the amplitudes of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitudes of $\omega_1$ and $\omega_2$. If $V_i$ is the amplitude of $\omega_1$ (and $\omega_2$), then the linear fundamental term and the intermodulation term are given by $c_1V_i$ and $(3/4)c_3v_i^3$, respectively. Considering the first three terms of a nonlinear transfer function are sufficient to characterize a nonlinear system dealing with a two-tone signal, $c_1$ and $c_3$ are the coefficients of the first-order and third-order terms of the transfer function. Theoretically, the input voltage ($V_{IP3}$), at which intermodulation and fundamental tones are equal, can be defined as [2]

$$\frac{\frac{3}{4}c_3V_I}{c_1V_{IP3}^3} = 1, \tag{4.6}$$

where $V_{IP3}$ is obtained as

$$V_{IP3} = 2\sqrt{\frac{c_1}{4c_3}}. \tag{4.7}$$

For a cascaded system of two or more stages, the overall $IP3$ voltage ($V_{IP3,ov}$) can be expressed as[10]

$$\frac{1}{V_{IP3,ov}^2} = \frac{1}{V_{IP3,1}^2} + \frac{\alpha_1^2}{V_{IP3,2}^2} + \frac{\alpha_1^2\beta_1^2}{V_{IP3,3}^2} + ..., \tag{4.8}$$

where $V_{IP3,1}$, $V_{IP3,2}$ and $V_{IP3,3}$ represent the input $IP3$ voltage of the first, second and third stages, respectively. $\alpha_1$ and $\beta_1$ are the small-signal gains of the first and second stages respectively. Note that increasing the gain of the first and second stages decreases the over all input $IP3$ ($V_{IP3,Nov}$) of the cascaded system because the third stage experiences the signal with large amplitude causing the larger $IM3$ products. From equation 4.8, it can be stated that for each stage of the cascaded system with gain greater than unity increases the nonlinearities of the later stages. Thus, unlike the noise figure, the $IP3$ of the cascaded system is limited by the $IP3$ of the last stage.

### 4.1.2 LNA Design Specifications for UWB Applications

Among different UWB systems, impuse-radio UWB systems cover the entire UWB bandwidth of 3.1-10.6 GHz and multiband (MB) UWB systems may operate over a band-group (three bands) or a number of band-groups: there are five band-groups and fourteen bands over 3.1-10.6 GHz UWB bandwidth. Importantly, LNAs for UWB systems need to cover a very wide bandwidth while they should provide a high gain and a low noise figure. UWB systems are used for short range (<10m) and high rate data (up to 480Mb/s) communications where channel capacities are increased by high bandwidth in accordance with the Shannon's channel capacity formula as [32]

$$C = Blog_2(1 + SNR), \tag{4.9}$$

where $C$ is the channel capacity and $B$ is the system bandwidth. Unlike narrowband systems, for short-range UWB systems, $SNR$ requirement is not strict because channel capacity is generally increased by high bandwidth. This

Table 4.1: Typical values of performance parameters for UWB LNAs

| Parameters | Values |
|---|---|
| $S_{21}$ (dB) | $> 10.0$ |
| $BW$ (GHz) | 3.1-10.6 |
| $NF$ (dB) | $< 6.0$ |
| $IIP3$ (dBm) | $> -15.0$ |
| 1-dB $CP$ (dBm) | $> -21.0$ |
| $S_{11}$, $S_{22}$ (dB) | $< -10.0$ |

allows for designing UWB LNAs with a higher noise figure. To maximize power gain, UWB LNAs should achieve broadband (50Ω) impedance matchings (at the input and output) over a wide bandwidth. The broadband input matching with antenna can be achieved with higher-order lossless $LC$ networks that use a number of passive inductors, which require a large chip area. However, the input matching for LNAs also depends on the configurations of amplifiers such as common-source and common-gate configurations.

Common-source configurations for UWB LNAs use lossless $LC$ filters to resonate reactive components (capacitive) at the input of the LNAs, and achieve broadband matching. Common-gate configurations provide direct broadband matching at the cost of higher power consumption, reduced gain and increased noise-figure. Broadband matching conditions are measured with input and output return losses ($S_{11}$ and $S_{22}$), which should be below $< -10dB$ over the desired UWB bandwidth. Along with high gain and low noise figure, the gain flatness in UWB LNAs over the desired UWB bandwidth is critically important because the flat gain ensures a low dynamic range for UWB signals. A low-dynamic range makes the designs of the wideband baseband circuits (variable gain amplifier, filter and analog-to-digital converter) of UWB receivers simple. For UWB LNAs, typical values of performance or design parameters including power gain ($S_{21}$), bandwidth ($BW$), noise figure ($NF$), input and output return losses ($S_{11}$ and $S_{22}$), 1-dB $CP$, and $IIP3$ are given in Table 4.1.

### 4.1.3 CMOS UWB Low-Noise Amplifiers

Several CMOS UWB LNAs have been reported in the literature [11, 33, 34, 35, 36]. Since UWB LNAs deals with very weak signals, most of these LNAs have been optimized for gain, bandwidth and noise figure with moderate $IIP3$ for linearity. Among different amplifier configurations, cascode common-source configurations for UWB LNAs exhibit excellent gain-noise performance. However, in these amplifiers, the broadband input matching requires higher-order ($3^{rd}$ order) $LC$ networks because RF signals are applied to the gate of a large transistor, which exhibits capacitive impedance. A 3.1-10.0 GHz UWB LNA using a cascode amplifier followed by a source-follower is presented in [11]. Optimized for flat gain, low noise figure and bandwidth, this LNA achieves broadband input matching using a three-section Chebyshave $LC$ passband filter that resonates with the input reactive component (capacitive) over the entire UWB bandwidth. Moreover, for enhanced and flat gain over the desired bandwidth, the cascode amplifier uses inductive load to exploit shunt peaking. Overall, the LNA in [11] uses five inductors (1.2-3.0 nH) and three capacitors 0.5-1.5 pF. These inductors require a large chip area leading to the overall area of the LNA to be 1.2mm$^2$.

Using a common-gate amplifier at the input stage, multistage CMOS UWB LNAs are reported in the literature [33, 34]. These LNAs achieve direct broadband matching with an input impedance which is inversely proportional to the transconductance ($g_m$) of the input transistor. The LNAs also employ inductors at the input to resonate the input reactive component over UWB bandwidth. The LNA in [33] is the cascading of a common-gate and a cascode amplifiers, followed by a source-follower. Because of low-gain of the input-stage common-gate amplifier, this LNA employs the second-stage cascode amplifier that uses shunt-peaked inductive load to enhance gain and improve gain flatness. The LNA in [34] is a four-stage amplifier including the output buffer stage. This LNA employs two shunt-peaked cascode amplifiers after the first-stage common-gate amplifier. The LNA exhibits a simulated bandwidth of 3.1-10.6 GHz, and simulated gain of 15.0-17.5 dB while occupying a large chip area because of using several passive inductors, and also consuming a large

amount of power(32.0mW).

CMOS UWB distributed amplifiers reported in the literature exhibit very wide bandwidth, flat gain and low *NF* [35, 36]. These LNAs comprise multiple amplifying stages in cascade with *LC* ladders at the outputs (at the drains) and inputs (at the gates) of the amplifiers. The *LC* ladder provides 50Ω broadband input and output matchings. However, because of using passive inductors in the amplifying stages, the distributed amplifiers occupy a large chip and consumes a large amount of power. The three-stage distributed LNA in [35] exhibits 0.1-11.0 GHz bandwidth and an average power gain of 8.0dB while it consumes 21.6mW and occupies a chip area of 0.7mm$^2$. Increasing the number of stages in distributed amplifiers increases both gain and bandwidth but chip area and power consumption increases proportionally. The LNA in [36] is a eight-stage distributed amplifier that provides an average gain of 10.0dB over the bandwidth of DC-44.0GHz but it consumes a large amount of power (over 90.0mW) while occupying a chip area of 1.5mm$^2$.

In summary, UWB LNAs using cascode configurations require passive *LC* input matching circuits, and therefore, they occupy a large chip area. UWB LNAs using common-gate configurations provide direct input matching using a few inductors but consume a large amount of power and also use inductors for gain-bandwidth enhancement. UWB distributed amplifiers exhibit flat gain with flat frequency response but use many area-inefficient inductors while consuming a large amount of power. In these LNAs, passive inductors occupy a significant portion of the chip area. Besides occupying a large chip area, the passive-inductor LNAs also have a common functional limitation that their gain-bandwidth cannot be tuned with fixed-structure inductors and capacitors.

Here, two new area-efficient CMOS UWB LNAs using ultra-compact tunable active inductors instead of bulk large-area passive inductors, are proposed. The tuning of active inductors with varying inductance and operating bandwidth makes these proposed LNAs tunable: varying gain and bandwidth, or trading gain with bandwidth of the LNAs. The tunability of the proposed UWB LNAs can be exploited further to adjust the variation of the desired gain-bandwidth caused by the variations of supply, process and temperature. Im-

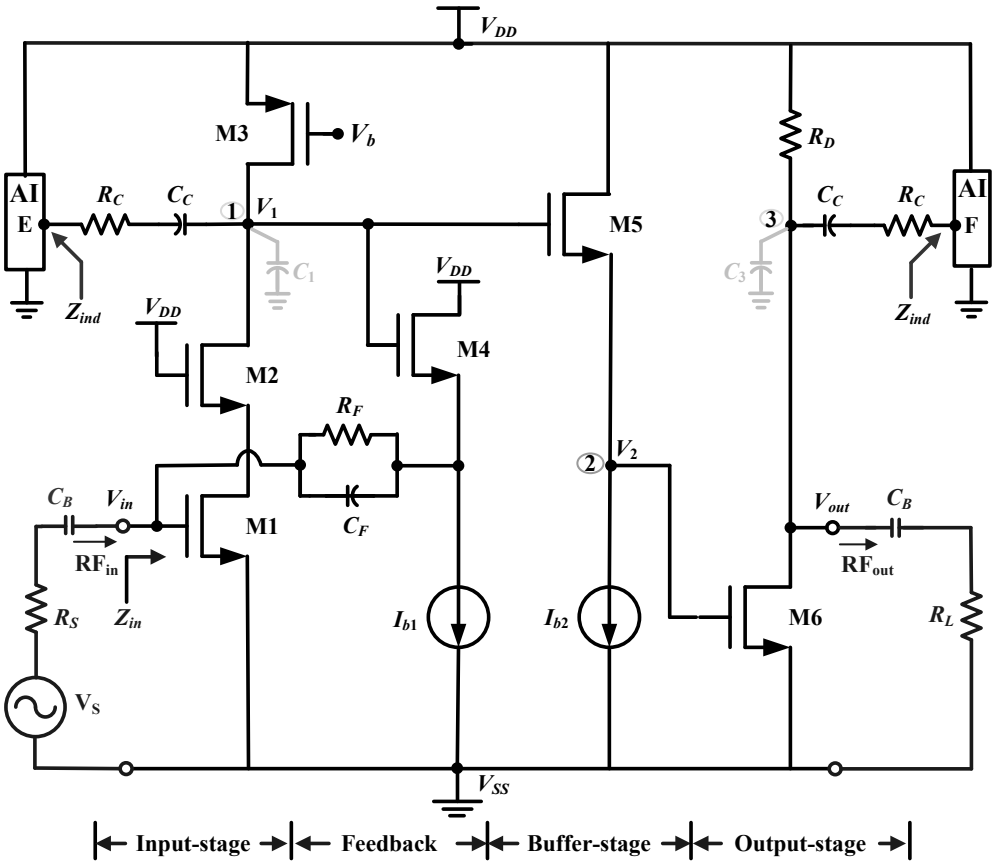


Figure 4.1: Proposed tunable three-stage UWB LNA.

portantly, to reduce cost, design considerations for the proposed UWB LNAs are: ultra-low chip area with a high level of device integration, and using standard digital CMOS processes. The performances of the proposed UWB LNAs are optimized for gain, bandwidth and noise figure.

## 4.2 Proposed Three-Stage Tunable UWB LNA

Figure 4.1 shows the schematic of a proposed three-stage UWB LNA terminated with source and load impedances ($R_S$=$R_L$=50Ω) [37]. This three-stage amplifier uses active inductors in the input and output stages. The input-stage

is a cascode amplifier (consisting of transistors M1, M2 and M3), and it is connected to the output-stage common-source amplifier (consisting of transistor M6 and resistor $R_D$) through a buffer amplifier or source follower (consisting of transistor M5 and $I_{b2}$). At the output node (Node 1) of the cascode amplifier, an active inductor is connected through a resistor $R_C$ in series with a coupling capacitor $C_C$ to cancel the effect of overall node capacitance ($C_1$). The active inductor is used to exploit inductive shunt peaking in improving the amplifier's gain flatness and extending its bandwidth [3]. The feedback resistor $R_F$, through a source-follower (transistor M4 and current source $I_{b1}$), providing local feedback, is used to achieve 50Ω input matching. A small capacitor $C_F$ (=25fF) in parallel with $R_F$ is used to improve input matching. It also increases feedback at high frequencies and eliminates peaking in the amplifier's frequency response [38].

The common-source amplifier boosts the gain of the overall LNA and provides 50Ω output matching. Here, another active inductor is connected to the load resistor $R_D$ at Node 3 to cancel the effect of overall node capacitance ($C_3$) and keep the frequency response (gain over frequency) flat at high frequencies, and in turn, enhance the bandwidth. The inter-stage buffer circuit provides isolation between input cascode and output common-source amplifiers making input and output matchings of the LNA independent of each other. The circuit of the identical active inductors used in the proposed LNA is shown in Figure 4.2 where a common control-voltage $V_{tune}$ is applied to control current $I$ of the active inductors, and in turn, tune the gain and bandwidth of the LNA. $C_B$ is the external DC blocking capacitor for simulation and measurement purposes only. The following subsections describe the tunable active inductor, input matching, gain-bandwidth, and noise figure of the proposed LNA.

### 4.2.1 Tunable Active Inductor

The design and analysis of the proposed one-port tunable active inductor of Figure 4.2 are presented in Chapter 3. The equivalent $RLC$ circuit of the inductive impedance $Z_{ind}$ of the active inductor along with series $RC$ network ($R_C$ and $C_C$) connected at Node 1 or 3 (with nodal capacitance $C_1$ or $C_3$) of

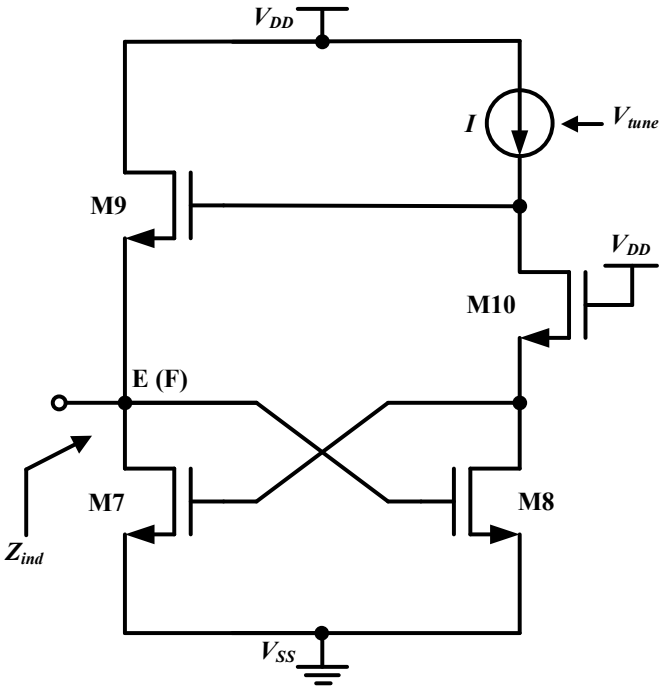


Figure 4.2: Tunable CMOS active inductor.

the LNA is shown in Figure 4.3(a) where $L_s$ is the inductance of the active inductor, and capacitance $C_p$ in series with resistance $R_s$ is parallel to $L_s$. Using simple transistor models, the elements of the equivalent $RLC$ circuit of $Z_{ind}$ are derived in Chapter 3 as follows:

$$L_s \approx \frac{C_{gs9}}{g_{m8}g_{m9}}. \tag{4.10}$$

$$R_s = \frac{C_{gs7} + C_{gs10}}{g_{m10}C_{gs8}}. \tag{4.11}$$

$$C_p = C_{gs8}. \tag{4.12}$$

$$R_p = \frac{g_{m10}}{g_{m8}(g_{m10} - g_{m7})}. \tag{4.13}$$

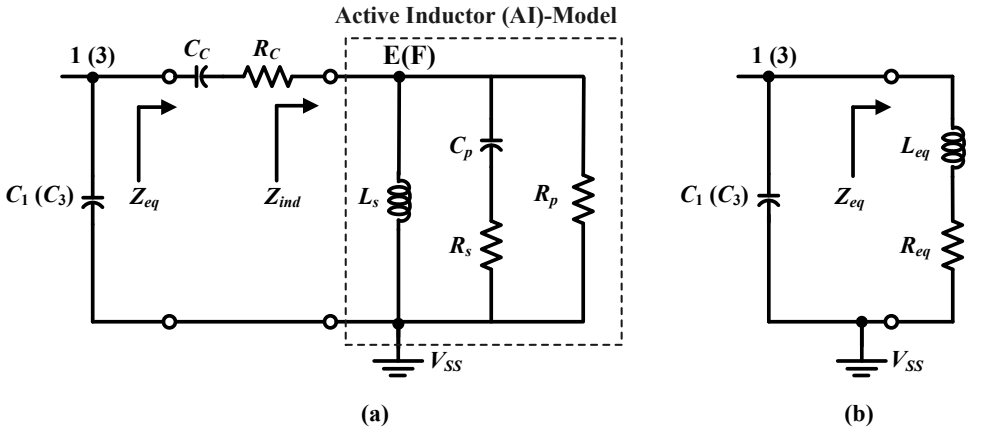


Figure 4.3: (a) Equivalent $RLC$ circuit of inductor in series with $R_C$ and $C_C$; (b) equivalent $RL$ circuit comprising $R_C$ and $C_C$.

In the above equations, $C_{gs}$ and $g_m$ with subscripts (7,8,9,10) represent gate-source capacitances and transconductance of matching number transistors (M7-M10) respectively. Neglecting the loading effects of $C_p$ and $R_p$ due to small device sizes, and low transconductance ($g_m$) and conductances($g_{ds}$), $L_s$ comes in series with $R_C$ and $C_C$. The coupling capacitor $C_C$ has negligible effect because it exhibits low impedance over the frequency of interest. Thus, the equivalent $RLC$ circuit of Figure 4.3(a) can be transformed into an equivalent $RL$ circuit of Figure 4.3(b). Hence, equivalent inductive-impedance $Z_{eq}$ is simply a series connection of $L_{eq}$ and $R_{eq}$ where $L_{eq}$ equals $L_s$, and $R_{eq}$ equals $R_C$. Note that $C_1$ is the total nodal capacitance at Node 1 (output node) of the input cascode stage. The series resistance of inductance $L_s$ increases by $R_C$, and this reduces loaded $Q$ of the active inductor. The low $Q$ of the inductor reduces the frequency selectivity, and consequently, makes the active inductor suitable for wideband applications.

Replacing the one-port grounded active inductor (AI) with inductance $L_s$ in series with resistance $R_s$ (here $R_s$ is zero), the upper part of the proposed UWB LNA circuit is shown in Figure 4.4(a). Coupling capacitor $C_C$ exhibits low impedance over the desired UWB frequency range. Hence, neglecting the effect of $C_C$ (considering to be shorted), the circuit in Figure 4.4(a) can be

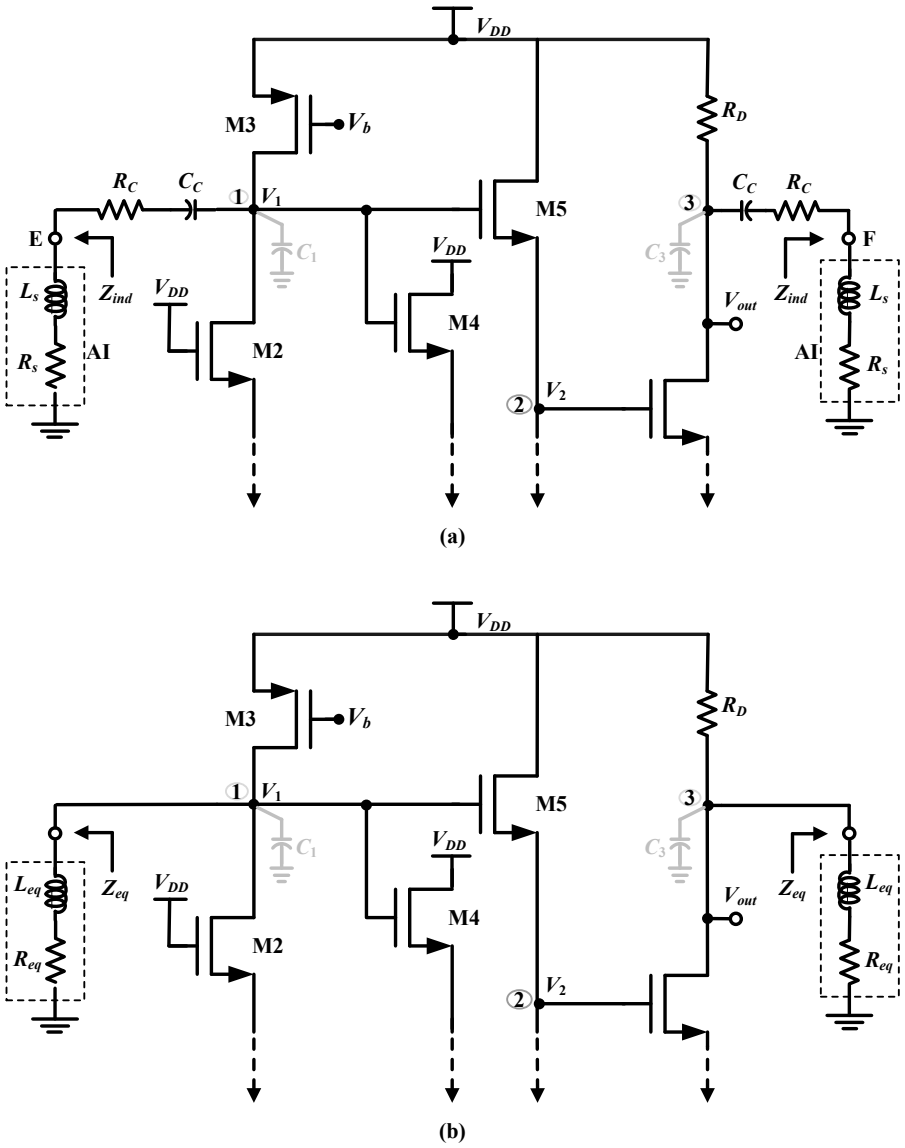


Figure 4.4: (a) Upper part of UWB LNA with inductor equivalent circuit excluding $R_C$ and $C_C$; (b) Upper part of UWB LNA with equivalent $Z_{eq}$.

replaced with the circuit in Figure 4.4(b) where $Z_{eq}$ is the equivalent inductive impedance looking at Node 1 (or 3). Here, $L_{eq}$ in series with $R_{eq}$ connected at the outputs (Nodes 1 and 3) of the amplifying stages becomes parallel to the signal path and nodal capacitance ($C_1$ or $C_3$). With increasing frequency, the

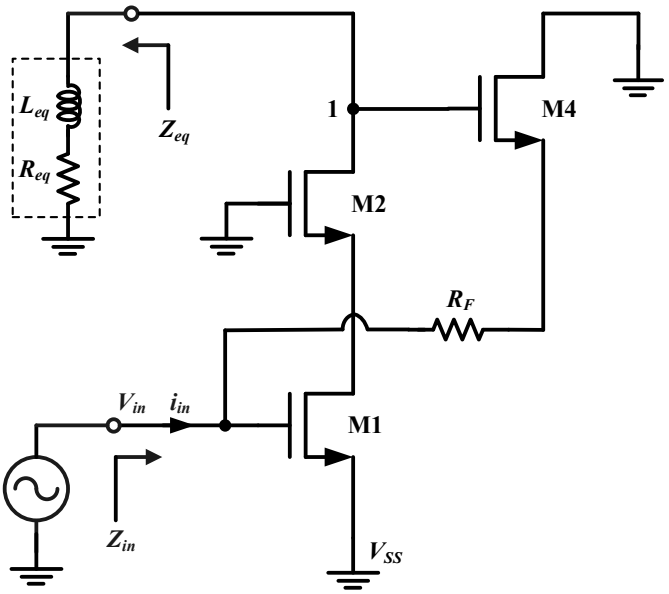


Figure 4.5: Small-signal circuit for input impedance of three-stage LNA.

diminishing capacitive impedance of $C_1$ or $C_3$ increases losses, and causes the frequency response (gain over frequency) of the amplifier falling of sharply that reduces the bandwidth. However, at high frequencies, the increasing inductive impedance of $L_{eq}$ of the active inductor counters the diminishing capacitive impedance of $C_1$ or $C_3$, and keeps the frequency response flat that increases the bandwidth. Here, the active inductor is used to provide shunt peaking, namely active shunt peaking.

### 4.2.2 Input Matching

Neglecting the loading effects of load transistor M3 and inter-stage buffer circuit (M5 and $I_{b2}$), the small-signal circuit for determining the input impedance ($Z_{in}$) of the proposed three-stage LNA is shown in Figure 4.5. At low frequencies, the input impedance, $Z_{in}$ ($= R_{in}$) of the LNA is

$$R_{in} = (R_F + \frac{1}{g_{m4}}).(\frac{g_{m2}}{g_{m2} + g_{m1}}) \approx R_F.\frac{g_{m2}}{g_{m1} + g_{m2}}, \tag{4.14}$$

where $g_m$ with subscripts 1,2 and 4 represents the transconductance of transistor M1, M2 and M4, respectively. For $R_F g_{m4} \gg 1$ ($R_F$ of around 200Ω and $g_{m4}$ of 60mS (mA/V), $R_{in}$ is approximated as

$$R_{in} = R_F . \frac{g_{m2}}{g_{m1} + g_{m2}}. \tag{4.15}$$

Hence, in order to achieve the input matching condition of $R_{in} = R_S$=50Ω, feedback resistor $R_F$ needs to be 200Ω with $g_{m1} = 3g_{m2}$. This requires transistor M1 to be approximately three times larger than transistor M2 for the same overdrive voltage. At high frequencies, the input impedance without considering $C_F$ (=20-25 fF) is expressed as

$$\begin{aligned} Z_{in} &= \frac{R_F}{1 + Z_{eq} g_{m1} + s R_F C_{gs1}} \\ &= \frac{R_F}{(1 + g_{m1} R_{eq}) + s(g_{m1} L_{eq} + R_F C_{gs1})} \\ &\approx \frac{R_F}{(g_{m1} R_{eq}) + s(g_{m1} L_{eq} + R_F C_{gs1})}, \end{aligned} \tag{4.16}$$

where $C_{gs1}$ is the gate-source capacitance of transistor M1, and $Z_{eq}$ is the equivalent impedance looking at the output node (node 1) of the cascode amplifier. In deriving Equation 4.16, gate-drain capacitance of M1, $C_{gd1}$ was neglected because the Miller effect was cancelled due to cascode device M2. The gate-source capacitance of M4, $C_{gs4}$ is also neglected due to small device sizes. It is also assumed that $R_F g_{m4} \gg 1$. At low frequencies, $Z_{in}$ is approximated as

$$Z_{in} = \frac{1}{1 + g_{m1} R_{eq}} \approx \frac{R_F}{g_{m1} R_{eq}}, \tag{4.17}$$

Since, it is assumed that $C_C$ is shorted as it exhibits negligible impedance over the frequency of interest, at low frequencies, $R_{eq}$ only appears in the expression of input impedance.

### 4.2.3 Gain-Bandwidth

The overall voltage gain $A_v$ of the proposed three-stage LNA is $A_{v1}A_{v2}A_{v3}$, where $A_v$ with subscripts 1,2, and 3 represents the gain of the first-stage cascode amplifier, the inter-stage source-follower (buffer), and the output-stage common-source amplifier, respectively. The cascode amplifier provides reasonable gain but the overall node capacitance $C_1$ at Node 1 of the LNA adds a pole in the frequency response, and reduces the bandwidth for UWB signals. The inter-stage buffer circuit reduces the gain slightly without affecting the bandwidth. The common-source stage boosts the gain but the frequency response of the overall amplifier rolls off very fast at high frequencies due to capacitance $C_3$ at the output node (at Node 3). In deriving the expression for voltage gain, the active inductor along with $R_C$ is replaced with the equivalent impedance $Z_{eq}$ of $L_{eq}$ in series with $R_{eq}$ as shown in Figure 4.5. The voltage gain of the first-stage cascode amplifier is expressed as

$$A_{v1} = \frac{v_1}{v_{in}} = -g_{m1}\{(r_{o3}) \parallel (\frac{R_{eq} + L_{eq}s}{L_{eq}C_1s^2 + R_{eq}C_1s + 1})\}, \tag{4.18}$$

where $r_{03}$ is the output resistance of load transistor M3. The total output resistance of the cascode amplifier at node 1 is $(g_m r_{01} r_{o2}) \parallel r_{03}$, where $r_{01}$ and $r_{02}$ are the output resistances of transistor M1 and M2, respectively. For a large current-source load device M3, providing a current of around 4.0mA with $g_{m2}$ of 20.0 mS(mA/V), $g_{m2}r_{o1}r_{o2}$ is much higher than $r_{o3}$ ($g_{m2}r_{o1}r_{o2} >> r_{o3}$). Hence, the small-signal gain of the cascode amplifier (without taking the active inductor into effect) is simply equal to $-g_{m1}r_{o3}$. However, from Equation 4.18, it is observed that low-frequency gain is $-g_{m1}R_{eq}$ assuming $r_{o3} >> R_{eq}$ because $C_C$ is shorted as it exhibits negligible impedance. For $g_{m1}$ of 60.0 mS and $R_{eq}$ (RC) of 170Ω, the absolute gain (≈10) obtained from the cascode stage is reasonably high. However, under input-matching condition, with a load of $R_{eq}$ (taking the active inductor into effect) for the amplifier, input resistor $R_{in}$ is approximately equal to $R_F/(g_{m1}R_{eq})$. Therefore, the gain of the input-stage can be simplified as $A_{v1} - g_{m1}R_{eq} = -R_F/R_{in}$ (≈4), which is low due to satisfying the input matching condition of $R_{in} = R_S = 50\Omega$. Thus, the gain

of the input cascode stage is traded off with input matching.

With increasing frequency, the diminishing capacitive impedance of capacitance $C_1$ at Node 1 causes the frequency response of the amplifier to fall off sharply at high frequencies due to increased signal losses. Here, at Node 1, increasing inductive impedance of inductance $L_{eq}$ (of the active inductor) counters decreasing capacitive impedance of $C_1$ and keeps the frequency response of the amplifier flat up to a very high frequency. Thus, gain remains flat up to very high frequency and bandwidth increases. The gain of the interstage source-follower (consisting of transistor M5) is expressed as

$$A_{v2} = \frac{v_2}{v_1} = \frac{C_{gs5}s + g_{m5}}{(C_2 + C_{gs5})s + g_{m5}}, \tag{4.19}$$

where $C_2$ is the total load capacitance including the gate-source capacitance of M6 ($C_{gs6}$) at node 2, and $g_{m5}$ and $C_{gs5}$ are the transconductance and gate-source capacitance of transistor M5 respectively. Note that the source follower has a unity gain at low-frequency. For low values of $C_{gs5}$ and $C_2$, the pole $-g_{m5}/(C_2 + C_{gs5})$ and the left-half plane zero $-g_{m5}/C_{gs5}$ provide some degree of cancellation with each other. This broadens the frequency response and keeps the bandwidth of the cascode-stage intact. The voltage gain of the output-stage common-source amplifier is

$$A_{v3} = \frac{v_{out}}{v_2} = -\frac{(g_{m6} - C_{gd6}s).R_D \parallel (R_{eq} + L_{eq}s)}{1 + R_D \parallel (R_{eq} + L_{eq}s).(C_3 + C_{gd6})s}, \tag{4.20}$$

where $g_{m6}$ and $C_{gd6}$ are the transconductance and the gate-drain capacitance of transistor M6 respectively, and $C_3$ is total node capacitance at Node 3. At low-frequency, the gain is $g_{m6}(R_D \parallel R_{eq})$. With $g_{m6}$ of 110mS/V, $R_D$ of 75Ω and $R_{eq}(R_C)$ of 170Ω, the amplifier provides a good low-frequency small-signal gain ($\approx 5.7$). Moreover, $R_D \parallel R_{eq}$ ($\approx 52\Omega$) ensures direct 50Ω broadband output matching (with $R_L = 50\Omega$). Like input-stage cascode amplifier, diminishing capacitive impedance of capacitance $C_3$ causes the frequency response of the amplifier to fall off (gain drops sharply at high frequencies) and decreases overall bandwidth of the LNA as gain drops. Here, inductance $L_{eq}$ (of the

active inductor) keeps the frequency response flat ensuring flat gain and wide bandwidth by countering $C_3$.

### 4.2.4 Noise Factor

The noise factor ($F$) of the proposed three-stage LNA is mainly determined by the noise factor of the first-stage cascode amplifier. The significant thermal noise sources in the circuit are: input device M1, load device M3, feedback resistor $R_F$, source-follower device M4, transistor Mb1 (not shown in Figure 4.2) of current-source $I_{b1}$, and the equivalent resistor $R_{eq}$ of the active inductor. The noise factors of these noise-sources with respect to source resistance $R_S$ are as follows:

$$F_{M1} \approx \frac{\gamma_1}{g_{m1} R_S}. \tag{4.21}$$

$$F_{M2} \approx \frac{\gamma_2}{g_{m2} R_S}.\frac{1}{(g_{m1}.r_{03})^2}. \tag{4.22}$$

$$F_{M3} \approx \frac{\gamma_3 g_{m3}}{g_{m1}^2.R_S}. \tag{4.23}$$

$$F_{M4} \approx \frac{\gamma_4 g_{m4}}{g_{m4}^2.R_S.(g_{m1}r_{03})^2}. \tag{4.24}$$

$$F_{R_{I_{b1}}} = \frac{\gamma_{I_{b1}}}{g_{m4}^2.R_S.(g_{m1}r_{03})^2}. \tag{4.25}$$

$$F_{R_{eq}} = \frac{R_{eq}}{R_S(g_{m1}r_{o3})^2}. \tag{4.26}$$

$$F_{R_F} = \frac{R_S}{R_F}. \tag{4.27}$$

In the above equations, $\gamma_1$, $\gamma_2$, $\gamma_3$, $\gamma_4$ and $\gamma_{Ib1}$ are the noise factors (or fitting parameters for the noise models) of transistors M1, M2, M3, M4 and Mb1 (of $I_{b1}$)respectively. Hence, using the analysis of the input-referred noise of a two-

port network [3, 22], the $(F)$ of the LNA with respect to source-resistance $R_S$ under matching condition $(R_S = R_{in})$ is expressed as

$$F = 1 + F_{M1} + F_{M2} + F_{M3} + F_{M4} + F_{R_{I_{b1}}} + F_{R_{eq}} + F_{R_F}, \tag{4.28}$$

or

$$\begin{aligned} F &= 1 + \frac{\gamma_1}{g_{m1}R_S} + \frac{\gamma_2}{g_{m2}R_S}.\frac{1}{(g_{m1}.r_{03})^2} + \frac{\gamma_3 g_{m3}}{g_{m1}^2.R_S} + \frac{\gamma_4 g_{m4}}{g_{m4}^2.R_S.(g_{m1}r_{03})^2} \\ &+ \frac{\gamma_{I_{b1}}}{g_{m4}^2.R_S.(g_{m1}r_{03})^2} + \frac{R_{eq}}{R_S(g_{m1}r_{o3})^2} + \frac{R_S}{R_F}, \end{aligned} \tag{4.29}$$

Note that a large $g_{m1}$, and a high gain $(g_{m1}r_{o3})$ for the input cascode-stage are required to reduce overall $F$ of the LNA. The lower limit of $F$ is bounded by the last term $(R_S/R_F)$. Thus, the minimum noise factor $F_{min}$ of the LNA is approximated as

$$F_{min} = 1 + \frac{R_S}{R_F}. \tag{4.30}$$

Note that for $R_F = 200\Omega$ and $R_S = 50\Omega$, minimum noise figure $(NF)$ is approximately 1.0dB $(10\log F_{min})$. In equation 4.29, the third term from the last is associated with the noise contribution of the active inductor to the core LNA. With increasing gain $(g_{m1}r_{o3})$, noise contributed by the active inductor decreases. Here, noise added from the input stage active inductor to the core LNA can be explained with a negative feedback system of Figure 4.6.

In Figure 4.6, $X_{noise,AI}$ is the noise signal from the active inductor (AI), $X_{in}$ is the input RF signal and $X_{o,sf}$ is the output signal at the source-follower of the feedback loop around the first-stage cascode amplifier. For the gain of $A_{v1}(= v_1/v_{in})$ of the cascode stage, if $A_{v,sf}$ represents the gain of the feedback source-follower (consisting of M4 and $I_{B1}$), then the following expression with a feedback factor $\beta$ (determined by $R_F$) is obtained as

$$X_{o,sf}(t) = X_{in}(t)\frac{A_{v1}A_{v,sf}}{1 + \beta A_{v1}A_{v,sf}} + X_{noise,AI}(t)\frac{A_{v1}A_{v,sf}}{1 + \beta A_{v1}A_{v,sf}}. \tag{4.31}$$

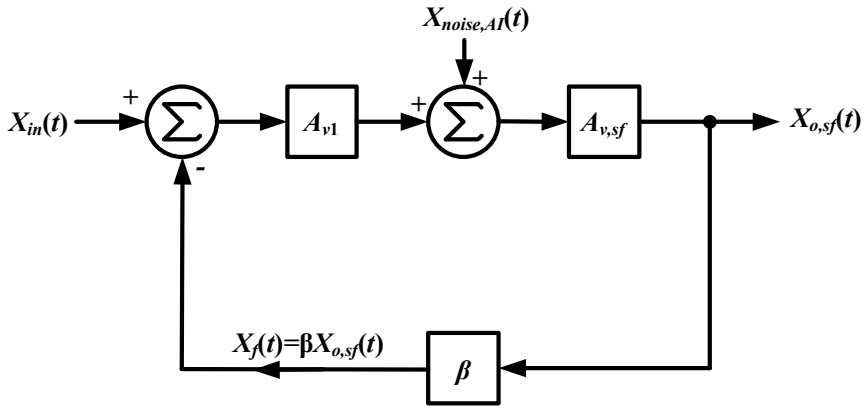


Figure 4.6: Addition of noise in negative feedback system.

Note that the fraction of noise, $X_{noise,AI}(t)$ contributed by the active inductor fedback to the input of the LNA is $\beta X_{o,sf}$. For a high loop gain of $\beta A_{v1} A_{v,sf}$, the input referred noise is not much affected by the active inductor embedded in the negative feedback loop. Notably, the high gain of the cascode stage reduces the noise contribution of the input-stage active inductor. Moreover, the local feedback-loop through a source follower further reduces the noise contribution. Since the active inductor connected at the output node (node 3) of the common-source amplifier is physically far apart from RF input, and the signal is not amplified in the subsequent-stages, its noise contribution to the core LNA is negligible.

### 4.2.5 Effects of Series $R_C C_C$

Active inductors are connected to the outputs of the amplifiers through $RC$ ($R_C$ and $C_C$) networks where $C_C$ is used as the coupling capacitor that keeps the DC operating points of the active inductors independent of those of the core LNA. $R_C$ and $C_C$ have significant effects on the gain and linearity of the LNA. For a fixed $R_C$, with increasing $C_C$, the gain decreases as the losses of the signals to the ground increase through the active inductor. Thus, the signal amplitude is reduced due to the reduced gain. Consequently, the re-

duced signal-amplitude causes the improvement of the linearity measured by $IIP3$ and 1-dB $CP$. Note that the active inductor along with the $RC$ network is represented by an equivalent inductance $L_{eq}$ in series with the equivalent resistance $R_{eq}$ that also includes $R_C$. With increasing $R_C$, $R_{eq}$ also increases, that in turn causes the effective factor quality factor ($Q_{eq}$) of the active inductor (a series $RLC$ circuit) to be decreased yielding the equation as

$$Q_{eq} = \omega_0 \frac{L_{eq}}{R_{eq}}. \tag{4.32}$$

The decreased $Q_{eq}$ causes the effective output resistance ($R_{o,eff}$) to be increased at Node 1 of the cascode amplifier yielding the equation as

$$R_{o,eff} = \frac{1}{\omega_0 L_{eq} Q_{eq}}. \tag{4.33}$$

Thus, the signal amplitude at the output of the cascode stage is increased as it is multiplied by the increased effective load resistor. Hence, the following inter-stage source follower and the common-source amplifier experience the increased signal amplitude at their inputs.

The increased input signals decrease both 1-dB $CP$ and input $IIP3$ of the inter-stage buffer, and the final-stage common-source amplifier. Note that in the cascaded system of the LNA, the $IIP3$ of the LNA is limited by the $IIP3$ of the final-stage common-source amplifier, yielding Equation 4.8. Hence, with increasing $R_C$, the overall linearity of the LNA is decreased. Note that the increasing of $R_C$ reduces the losses of the signals to ground through the active inductor, which in turn increases the gain. However, with a very large $R_C$, the active inductor loses its effectiveness because the series resistance dominates over the inductance of the active inductor.

### 4.2.6 Design Implementation

Figure 4.7(a) shows the complete circuit of the proposed three-stage UWB LNA including the bias circuit and active inductor. The current sources $I_{b1}$ and $I_{b2}$ are realized with two NMOS transistors Mb1 and Mb2, respectively, whose

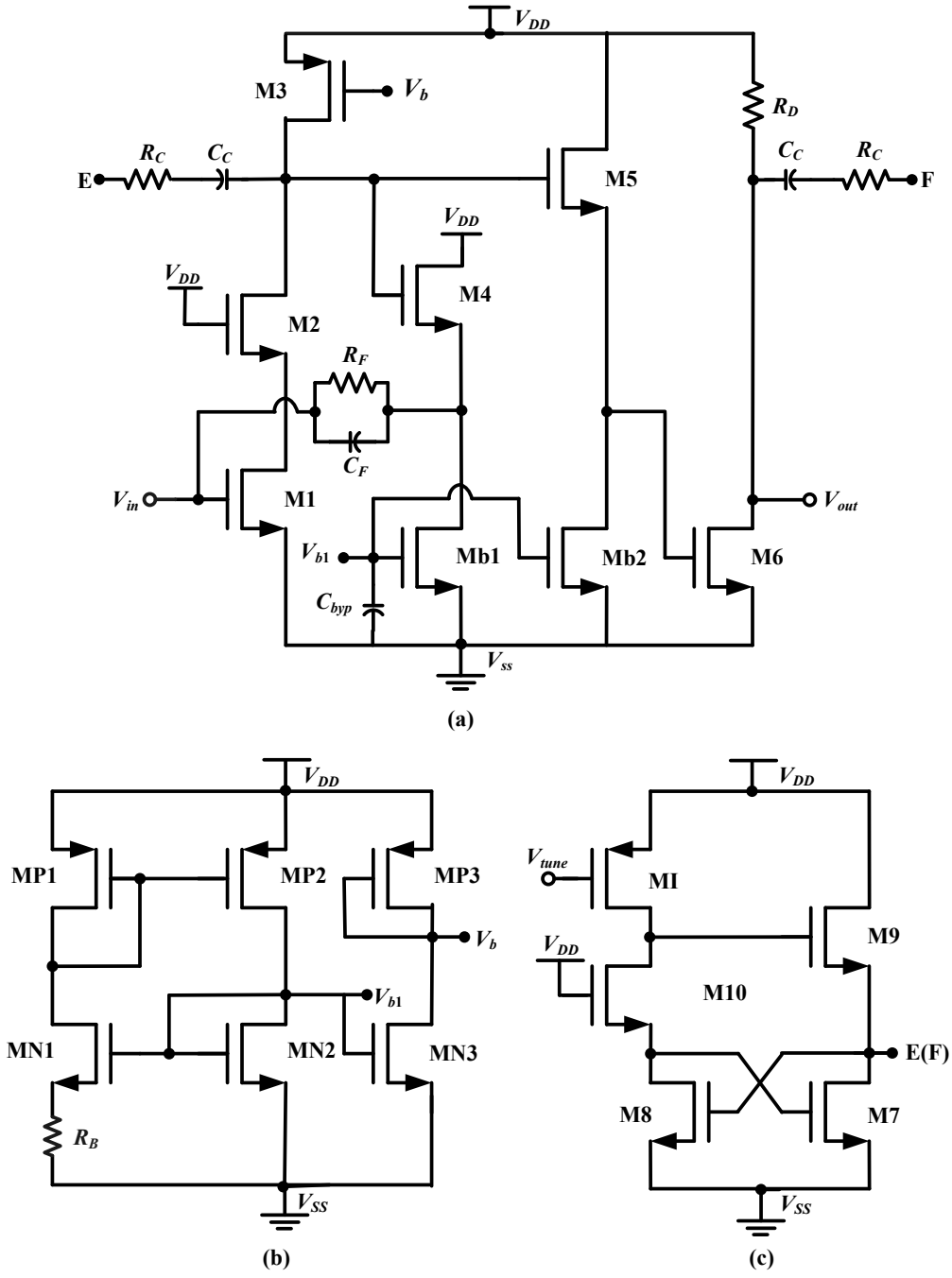


Figure 4.7: Complete circuit of proposed three-stage UWB LNA.

gates are biased with a DC voltage $V_{b1}$. A single bias circuit as shown in Figure 4.7(b) generates bias voltages, $V_{b1}$ and $V_b$. The active inductor in Figure 4.7(c) is connected to the core LNA through nodes E and F. Current-source $I$ in the active inductors is replaced with a PMOS device. The proposed three-stage UWB LNA in Figure 4.7 is designed and implemented in STMicroelectronics 90nm CMOS digital CMOS process. Device sizes (width$=W$ and length $=L$) of and bias voltages for transistors are chosen to achieve desired gain-$BW$, $NF$, and $IIP3$ for the proposed LNA.

The aspect ratio ($=W/L$) of transistors along with bias and supply voltages establishes DC current, and in turn, determines small-signal parameters such as transconductances ($g_m$) and conductances ($g_d$), which determine the gain of the LNA. On the other hand, capacitances ($C_{gs}$ and $C_{gd}$) of transistors limit the operating bandwidth of the amplifier. In the proposed UWB LNAs, transistors have different roles as some of them (transistors M1, M2, M4, M5, M6) are used in signal paths, some are used as loading devices parallel to the signal paths (transistor M3, Mb1, Mb2) and some are used as biasing devices (transistors MN1-MN3 and MP1-MP3). Hence, transistors are sized and biased depending on their applications.

1. Length($L$): Transistors with minimum feature size (minimum $L$) contribute minimum parasitic capacitances that result in a higher operating frequency. The minimum $L$ also provides a high transconductance ($g_m$) for a given $W$ and an overdrive voltage (gate-source voltage minus threshold voltage). On the other hand, a high $L$ for transistors reduces thermal and flicker noises [22]. However, these two advantages of noise reduction with a high $L$ are overlooked due to the requirement of high $g_m$ (for high gain), and increased operating frequency with minimum $L$. Therefore, transistors M1 to M6, Mb1 and Mb2 of the core LNA, and transistors M7 to M10 and MI of the active inductors of the proposed three-stage LNA (Figure 4.7)are chosen with the minimum $L$ of 100nm. On the other hand, all bias transistors (MN1 to MN3 and MP1 to MP3) are chosen with a $L$ of 200nm to reduce thermal and flicker noise.

2. Width ($W$): Transistors with a large $W$ provide high transconductances ($g_m$) for a given $L$ and an overdrive voltage. A high $g_m$ is necessary for a high gain because the gain of an amplifier is obtained by multiplying $g_m$ with the load resistor. On the other hand transistors with a small $W$ contribute low noise and low parasitics resulting in increased operating frequency. However, high gain requirement of RF amplifiers forgoes the advantages of using small-width transistors. In the proposed three-stage LNA, transistors M1 and M6 are used for input matching, and gain boosting, respectively. Therefore, M1 and M6 are chosen with a large $W$ to provide a high current, and in turn, to provide a high $g_m$. With increased current consumption, large widths for M1 and M6 also provide high output $IP3$ ($OIP3$) yielding high input $IP3$ ($IIP3$), and hence, the linearity of the LNA is improved. Transistor M4 of the buffer source-follower is optimized for input matching while keeping its gain below unity so that a lower amount of noise is fed back from the active inductor to the input of the core LNA. Transistor M5 of the inter-stage source-follower is chosen to keep its gain close to unity so that the final-stage common-source amplifier does not require to provide a high gain. Load device M3 (PMOS transistor) is also chosen large to obtain a high current in the cascode amplifier so that $g_{m1}$ of M1 remains high in order to provide input matching and a moderate gain. The sizes of transistors (Mb1 and Mb2) of current-sources ($I_{b1}$ and $I_{b2}$) are chosen smaller to contribute less noise. The widths of the transistors of active inductors are kept small to reduce power consumption, increase inductive operating bandwidth, and reduce noise contribution to the core LNA.

3. Multi-fingered transistor: At RF frequencies, the gate resistance ($R_G$) of a transistor contributes significant thermal noise. Therefore, transistors with a large width are realized using folded structures, where instead of using a single-gate large width transistor, multiple-gate small width transistors are folded together to achieve the same width of a single-gate large width transistor. In folded-structure transistors, the gates are connected together at both ends so that gate resistance $R_G$ is reduced by a

factor of $2N$ ($R_G/2N$) for an $N$ number of gate fingers. Moreover, for RF amplifications, transistors need to carry a large amount of current, but limited widths of metal lines in source and drain diffusion areas cannot carry a high current. Here, multi-fingered transistors create multiple parallel paths in source and drain diffusion areas allowing to carry a large amount of current. For the proposed LNA, all the transistors in the core LNA are sized with a minimum width ($W$) of $1.5\mu m$. Thus, a transistor with a $W$ of $60\mu m$ is realized with a folded structure of 40(N)x$1.5\mu m$ where 40 is the number of fingers.

4. Resistors and capacitors: In the proposed three-stage UWB LNAs (Figure 4.7), resistors are used as biasing ($R_B$), loading ($R_D$) and feedback ($R_F$) devices. The wider resistors with shorter length are subjected to less process and temperature variations, which are necessary to generate stable bias voltages (with $R_B$) in the bias circuit, and stable DC operating points (with $R_D$) in the core LNA. Since load device $R_D$ has to carry a large amount of current, it is designed with parallel connections of multiple resistors having shorter wider width ($W$) compared to a single resistor. The bias resistor $R_B$ is realized with a width greater than $2\mu m$ while keeping the ratio of the length to width equal to or less than five (5), as recommended in the process technology documentations. For example, the load resistor $R_D$ of $75\Omega$ is realized with ten parallel resistors with a width of $2.5\mu m$ and an length of $5\mu m$, and it is designed with twenty percent overload capacity. Besides resistors, coupling capacitors, $C_c$ (0.85-1.200 pF) and feedback capacitor $C_F$ (25fF) are used. Capacitors are intended to provide high capacitance per unit area to reduce the chip area; therefore, all capacitors are realized with fringe capacitors (lateral flux capacitors) using multilevel interdigitated metal structures, which increase per unit capacitance to $2.2\text{fF}/\mu\text{m}^2$. These types of capacitors are also useful to meet metal density requirements for fabrication over the full chip. In a seven-metal 90nm CMOS process, the fringe capacitors are realized using metal-3 to metal-7 layers to keep more isolation between bottom plates of capacitors and the silicon substrate in

Table 4.2: Device sizes for three-stage UWB LNA

| | M1 | M2 | M3 | M4 | M5 | M6 | Mb1 | Mb2 |
|---|---|---|---|---|---|---|---|---|
| $W$ ($\mu$m) | 120 | 39 | 45 | 15 | 60 | 81 | 27 | 39 |
| $L$ (nm) | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 |

order to minimize losses of signals at high frequencies.

5. DC bias voltages: Once device sizes are chosen, bias voltages are generated to keep all transistors in saturation. The overdrive voltage of a transistor ($V_{GS} - V_{TH}$) determines its drain current where $V_{GS}$ is the gate-source voltage and $V_{TH}$ is the threshold voltage of the transistor. In the proposed three-stage UWB LNA, for input transistor M1, the choice of DC level for $V_{GS1}$ is critical because the required transconductance ($g_{m1}$) for power and noise matching (for maximum gain and minimum noise figure) is to be achieved at the input cascode stage. Moreover, stable DC operating points of the following stages (source-follower and common-source amplifier) also depend on the DC operating points of the input cascode stage. Using a local feedback ($R_F$, Mb1), $V_{GS1}$ is kept around 400mV. With a $V_b$ of 380mV, the current in the cascode stage is set around 4.5mA. Bias voltage $V_{b1}$ is chosen as 450mV to obtain 1.2mA and 2.5mA in the respective source followers. The DC level of $V_{GS6}$ for M6 is required to be around 500mV to have a current of around 6.0mA that provides direct output matching and enough voltage headroom for a large signal-swing. Note that the DC level shifting is caused by the source follower consisting of transistors M5 and Mb1 to obtain $V_{GS6}$ of 500mV. It is also noted that the core LNA and active inductors are independently biased as they are separated by a coupling capacitor $C_C$.

Table 4.2 summarizes widths and lengths of transistors of the core LNA.

Fabricated in STMicroelectronics seven-metal 90nm CMOS digital process, the die photo of the proposed three-stage LNA (Figure 4.7) is shown in Figure 4.8. The LNA occupies a core chip or active chip area (excluding testing bond

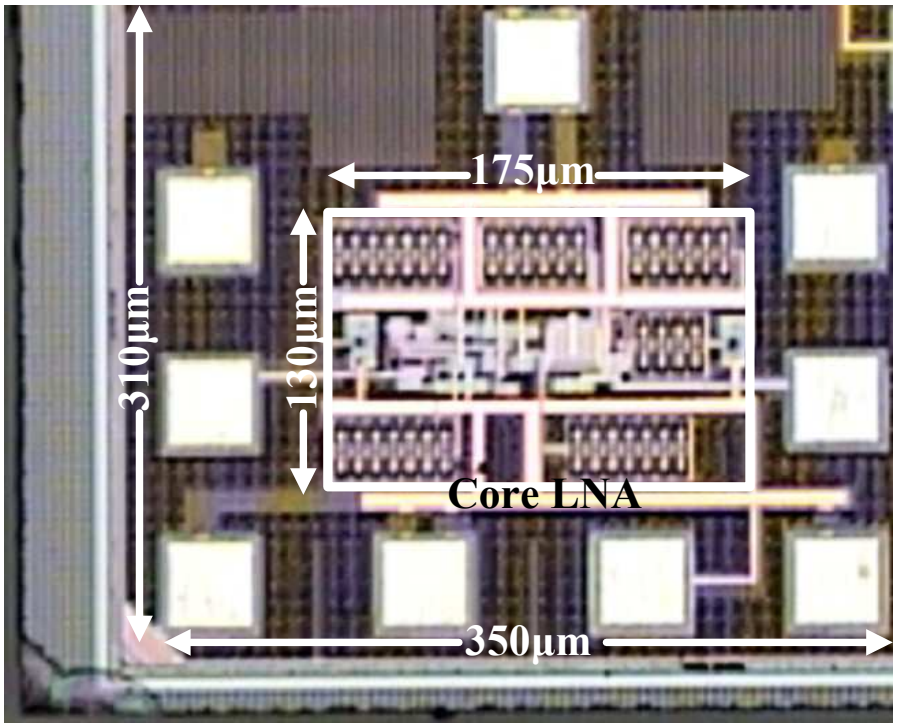


Figure 4.8: Microphotograph of fabricated three-stage LNA.

pads) of only 0.022mm$^2$ (180$\mu$m $\times$ 125$\mu$m). The overall chip-area including all the bonding pads is 0.08mm$^2$ (320$\mu$m $\times$ 250$\mu$m).

### 4.2.7 Measurement Setups

The fabricated three-stage LNA is measured on-wafer using GSG (ground-signal-ground) probes for RF signals and DC probes for DC power supplies and control voltages. The LNA is measured for S-parameters and *NF* using a Vector Network Analyzer (VNA) and an Agilent noise-figure meter N8975A, respectively. Figure 4.9 shows the on-wafer measurement setup for the fabricated LNA to measure S-parameters using VNA. The measurement setup for input return-loss ($S_{11}$) and reverse isolation ($S_{12}$) is shown in Figure 4.9(a). Forward-gain or power gain ($S_{21}$) and output return-loss ($S_{22}$) are measured

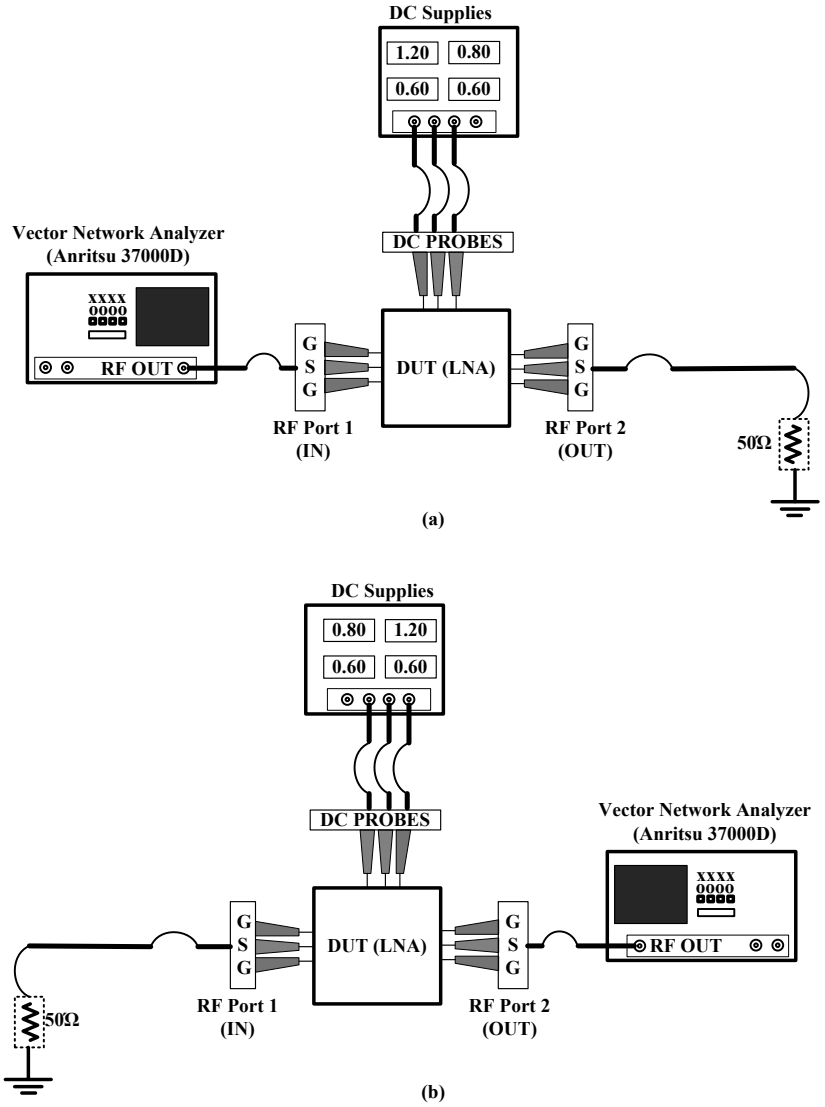


Figure 4.9: (a) Measurement setup for input return loss ($S_{11}$) and reverse isolation ($S_{12}$); (b) measurement setup for power gain ($S_{21}$) and output return loss ($S_{22}$).

using the setup as shown in Figure 4.9(b).

The measurement setup for *NF* is shown in Figure 4.10(a) where a noise-source is connected at the input RF port and *NF* is measured at the output RF port using the noise-figure meter. An internal DC voltage source drive

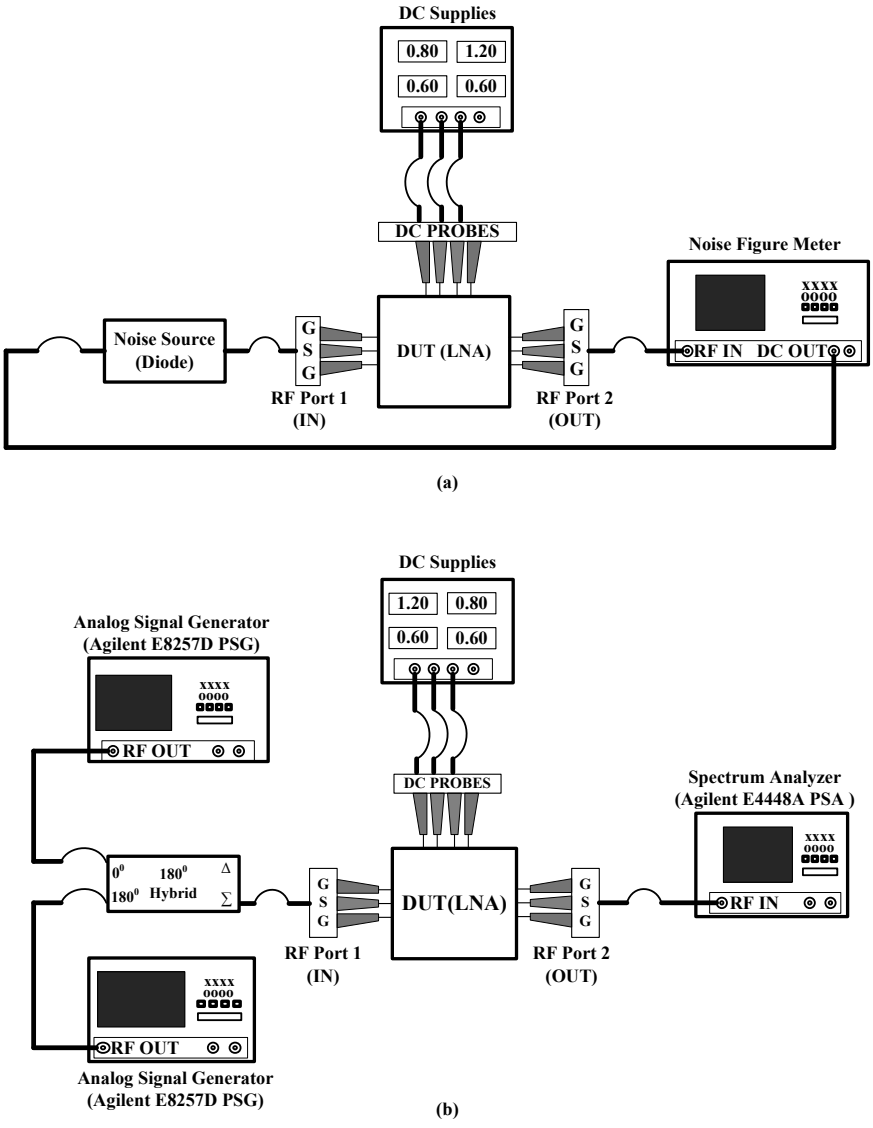


Figure 4.10: (a) Measurement setup for *NF*; (b) Measurement setup for *IIP3*.

the noise-source. The measurement setup for the linearity measurement of the LNA ($IIP3$) and 1-dB $CP$) is shown in Figure 4.10(b) where two closely spaced RF tones are combined using a power combiner (Hybrid) and are applied to the input RF port. With varying input RF power, the power of the fundamental tones and IM terms are measured using the spectrum analyzer at the output

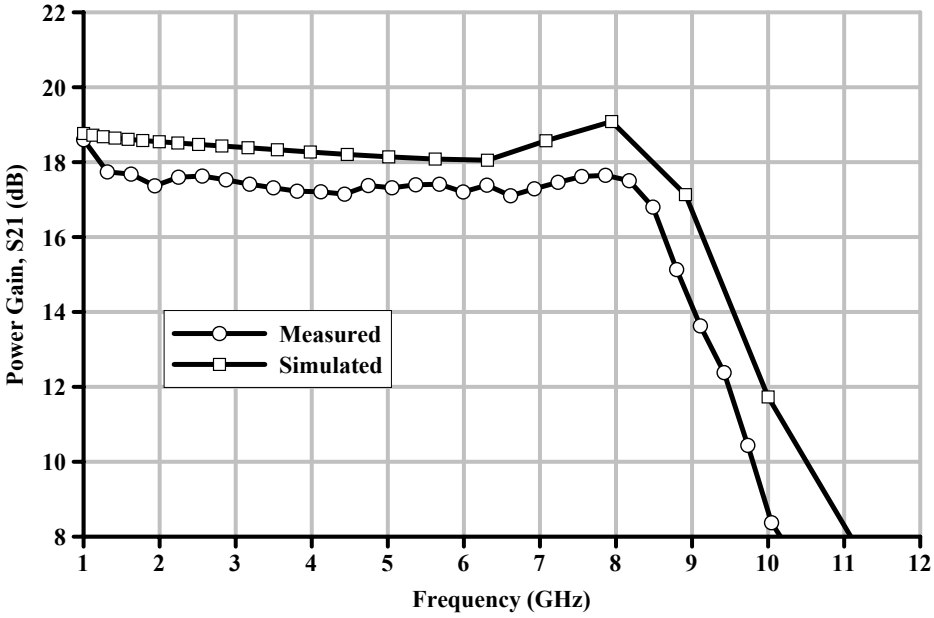


Figure 4.11: Measured and simulated gain of three-stage LNA.

RF port.

### 4.2.8 Measurement Results

Operated with a 1.2V power supply, the fabricated three-stage LNA draws a current of 13.8mA with a $V_{tune}$ of 600mV for the active inductors. In simulation, the three-stage LNA draws a total current of 14.1mA including the currents of active inductors where each active inductor draws a current of 340$\mu$A for a $V_{tune}$ of 600mV. The measured power gain ($S_{21}$) of the LNA along with the simulated $S_{21}$ is shown in Figure 4.11. The LNA exhibits a measured flat $S_{21}$ of 17.6dB and its 3dB bandwidth ($BW$) spans over 3.0-8.8 GHz band. Note that the measured $S_{21}$ is reduced by 1.2dB from the simulated $S_{21}$ (18.8dB), and the measured $BW$ (3.0-8.8 GHz) is reduced by 300MHz from the simulated $BW$ (3.0-9.1 GHz).

Figure 4.12 exhibits the measured and simulated noise figure ($NF$) of the LNA. The LNA exhibits a measured $NF$ of 3.6-5.1 dB over 3.0-8.8 GHz band,

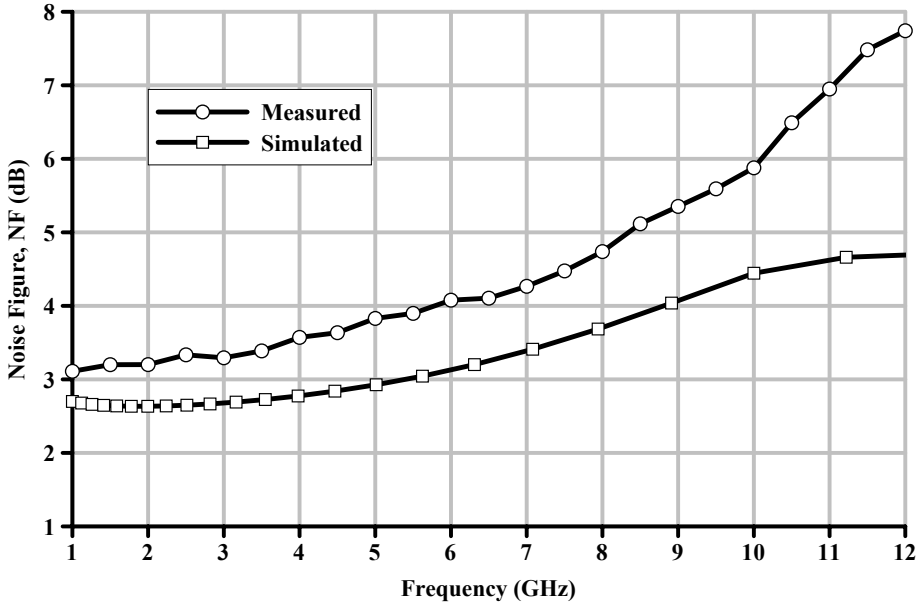


Figure 4.12: Measured and simulated noise figure of three-stage LNA.

whereas the simulated *NF* is (2.8-4.0 dB). Hence, the measured *NF* (3.6-5.1 dB) is increased by an average of 0.9dB from the simulated *NF*. Figure 4.13 shows the measured and simulated input ($S_{11}$) and output ($S_{22}$) return losses of the three-stage LNA. Measured $S_{11}$ and $S_{22}$ are below -10.0dB over 2.0-10.5 GHz indicating the perfect broadband matching of the input or output impedance of the LNA with source or load impedance. The measured $S_{11}$ and $S_{22}$ exhibit excessive deep at a comparatively lower frequency ($<$ 2.0GHz. This is because of the small-signal substrate resistance effect caused by the increasing body resistance ($R_{body}$) of transistors due to a larger distance to the body contact [39]. In case of measured $S_{22}$, the output impedance also decreases with increased $R_{body}$, and the dipping effect becomes more evident. However, the small-signal substrate resistance effect might not be identified in simulation, and therefore, the measured $S_{11}$ and $S_{22}$ exhibit large deviation from the simulated ones. Figure 4.14 shows the measured and simulated reverse isolation ($S_{12}$ of the fabricated three-stage LNA. The measured $S_{12}$ is below -30.0dB over the frequency range of 2.0-10.0 GHz and follows the

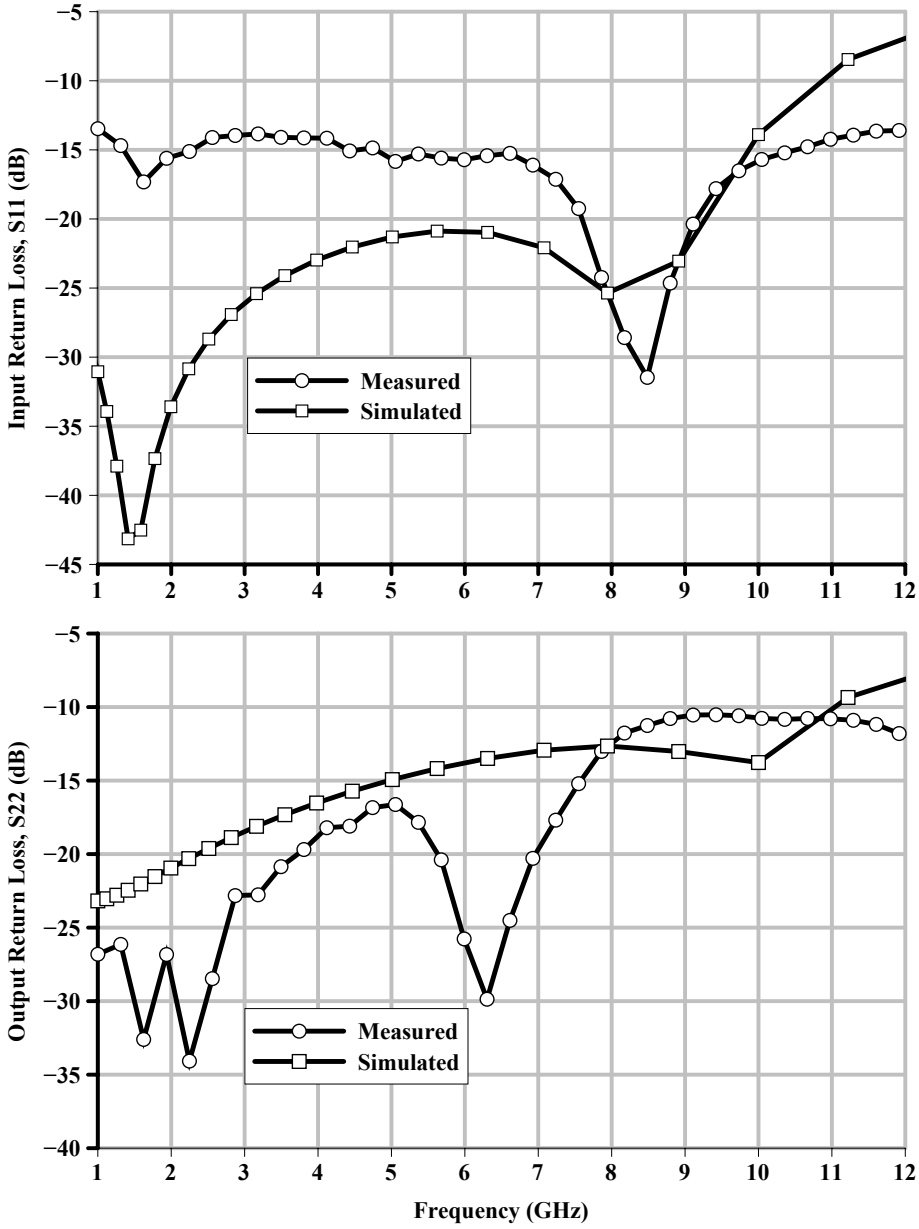


Figure 4.13: Measured and simulated return losses of three-stage LNA.

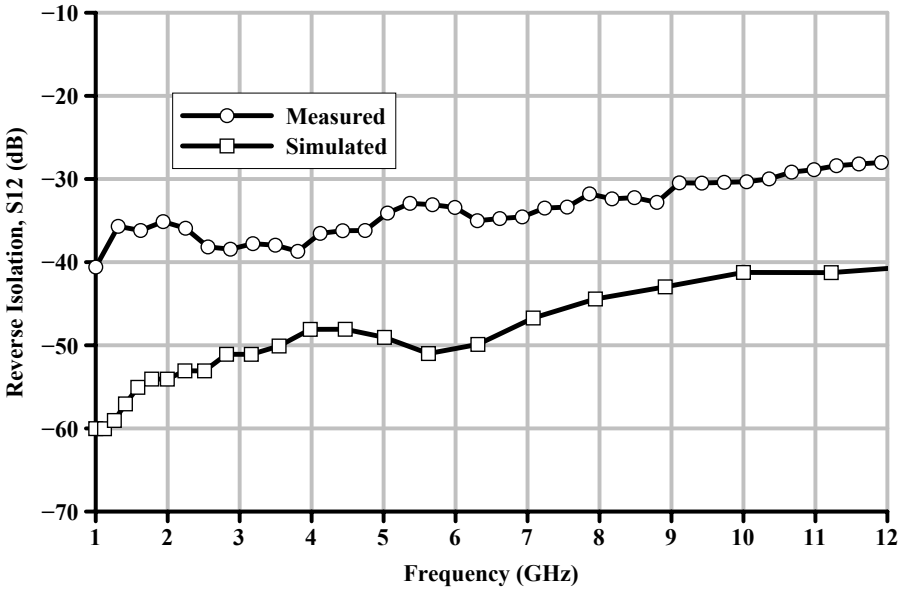


Figure 4.14: Measured and simulated reverse isolation of three-stage LNA.

pattern of the simulated $S_{12}$ with a reduced value.

Note that measured gain ($S_{21}$), $BW$ and $NF$ differ from simulated ones. As the RF LNA is designed and implemented using normal transistors of digital CMOS technology, one of the possible causes behind the difference between measured and simulated results is the inaccuracy in high-frequency modeling of transistors and metal interconnects. The fabricated LNAs also draw less current than they do in simulation. The reduction of current occurs due to the resistances of interconnects, and the contact resistance between probe tips and bonding pads (power supply pads, $V_{DD}$ and $V_{SS}$). Here, the reduced current decreases gain and increases $NF$ slightly. Note that the measured $NF$ degrades by almost 1.0dB from the simulated $NF$. This is possibly for the lack of high-frequency noise model for transistors available in simulation. The noisy measurement environment (noisy power supply, and noise contributed by external wires) also causes the discrepancy between simulated and measured noise figures.

Figure 4.15 shows the tuning of three-stage LNA with control voltage $V_{tune}$

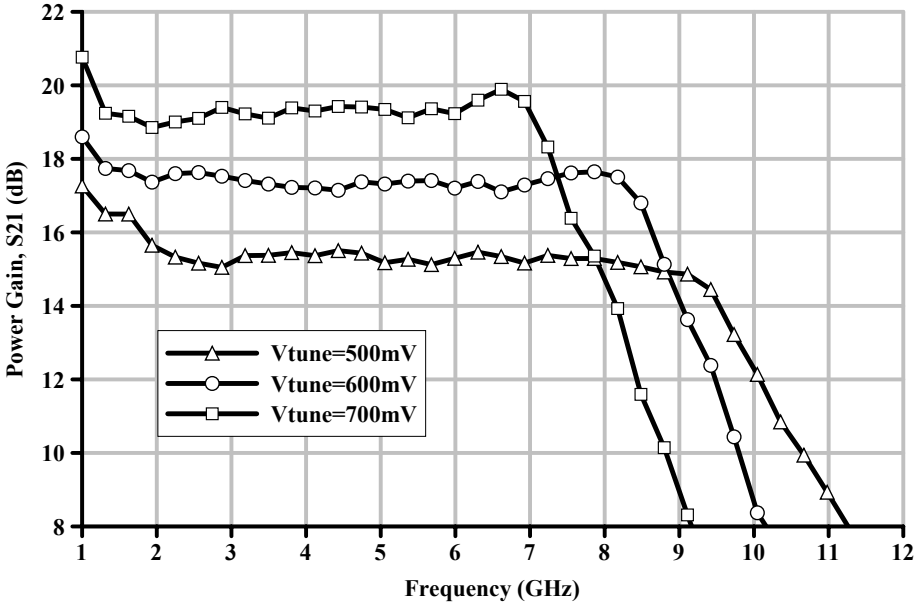


Figure 4.15: Tuning of measured gain-bandwidth of three-stage LNA.

of 500mV, 600mV and 700mV for the active inductors indicating the trade off between gain and bandwidth. With $V_{tune}$ of 700mV, the measured gain ($S_{21}$) obtained is 19.4dB but the bandwidth ($BW$) is reduced to 3.0-7.6 GHz. At high $V_{tune}$, the inductance of the active inductor increases but its useable operating bandwidth decrease with a lower resonance frequency. Here, with an increased inductance, the gain of the LNA increases but its bandwidth decreases. On the other hand for $V_{tune}$ of 500mV, $BW$ is extended over 3.0-9.8 GHz but $S_{21}$ is reduced to 15.3dB. In case of low $V_{tune}$, the inductance of the active inductor decreases but its useable operating bandwith increases. This causes the reduced gain but the increased bandwidth for the LNA.

The measurement setup for $IIP3$ and 1-dB $CP$ of the fabricated three-stage LNA is shown in Figure 4.10(b). For 1-dB $CP$ measurement, a single-tone test is performed with a 5.0GHz signal. The LNA exhibits measured 1-dB $CP$ of -16.2dBm as shown in Figure 4.16. For $IIP3$ measurement, a two-tone test with two signals at 1.0MHz apart (one is at 5.0GHz and another one is at 5.001 GHz) is performed. Three-stage LNA exhibits measured $IIP3$ of -6.3dBm as

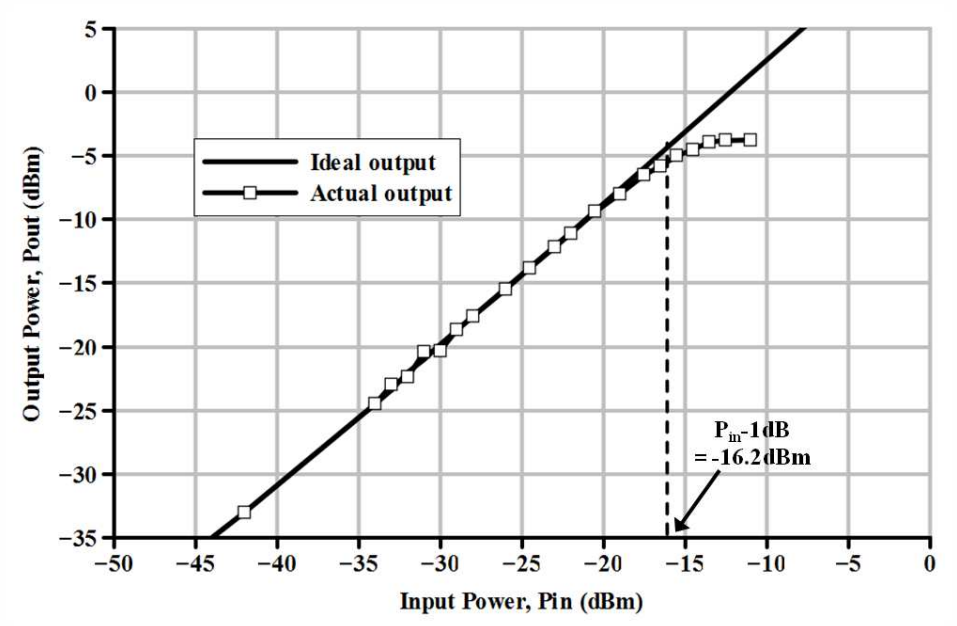


Figure 4.16: Measured 1-dB *CP* of three-stage LNA.

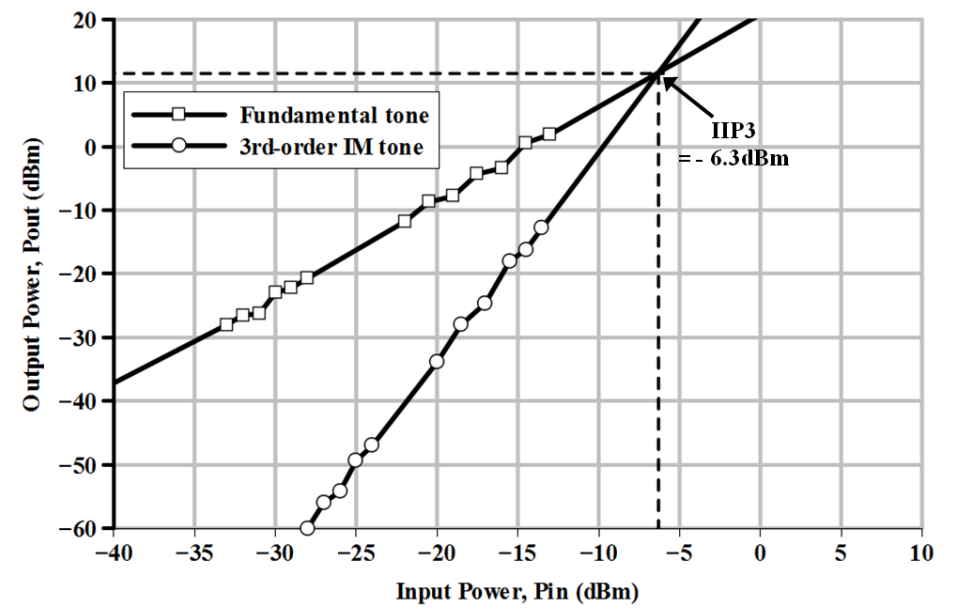


Figure 4.17: Measured input-*IP*3 (*IIP*3) of three-stage LNA.

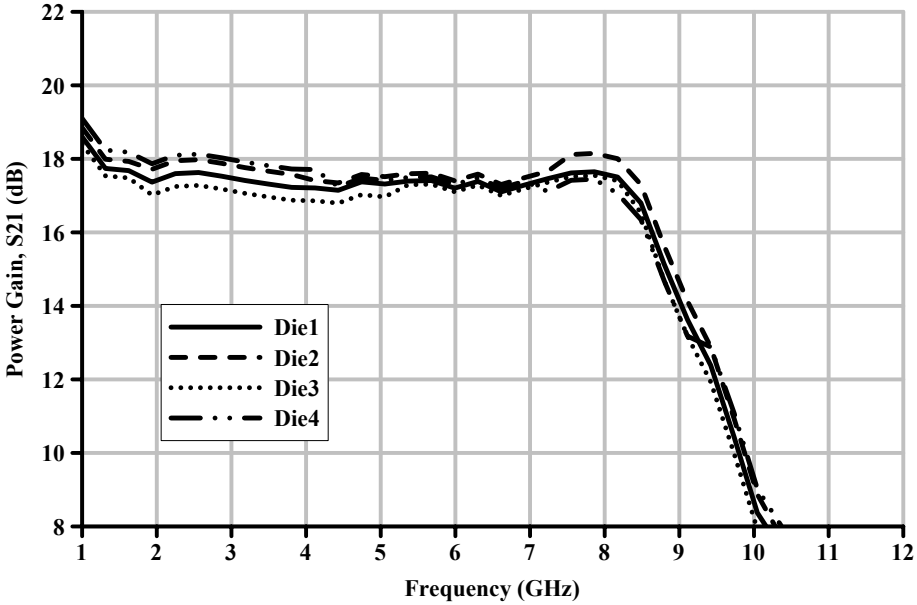


Figure 4.18: Measured gain of three-stage LNA on different samples

shown in Figure 4.17.

The fabricated three-stage LNAs are measured on different samples to investigate design robustness and die yield. Figure 4.18 shows the gain ($S_{21}$) of the three-stage LNA measured on five different samples. The LNA shows a variation of $S_{21}$ within 0.5dB among the measured dies. This indicates the good repeatability of the performances of the LNA on different samples as well as good yield of the fabrication process.

## 4.3 Proposed Two-Stage Tunable UWB LNA

The proposed three-stage UWB LNA in Figure 4.7 employs two source-followers. One source-follower (M4 and $I_{b1}$) around the input cascode-stage is used for input-matching. Another inter-stage source-follower (M5 and $I_{b2}$) (buffer) provides isolation between input and output amplifying stages, and it is also used for DC level shifting to keep the output-stage common-source amplifier in saturation. A reasonable amount of current is consumed in the inter-stage buffer to

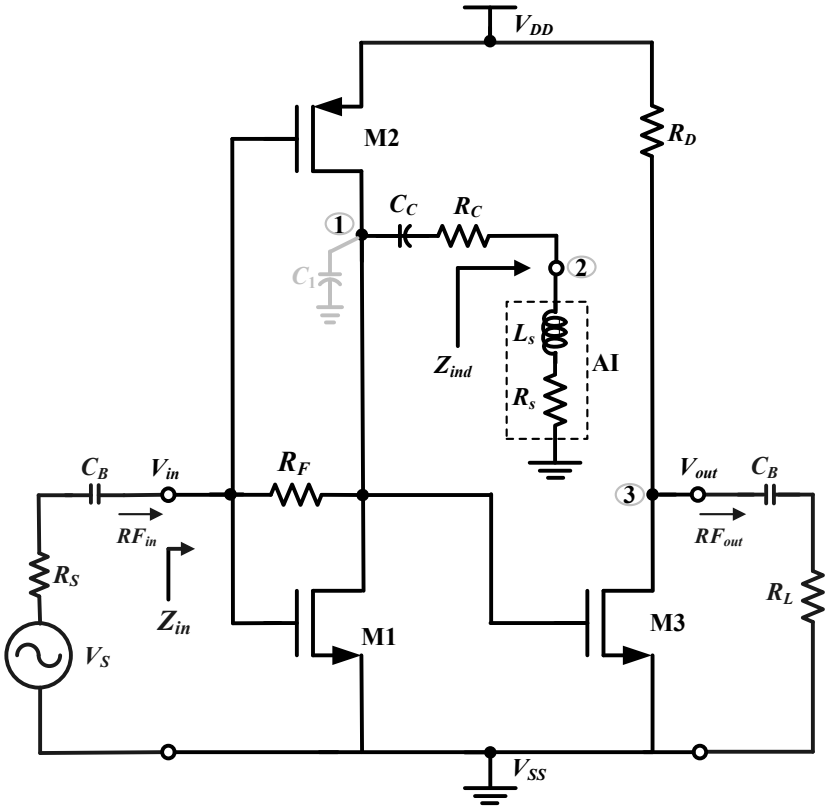


Figure 4.19: Proposed new two-stage UWB LNA.

keep gain close to unity without affecting the bandwidth. Hence, two source-followers require additional biasing circuits that consume power and occupy additional chip area. Moreover, the increasing number of transistors of source-followers also contribute more noise to the LNA. Here, for further reduction of chip area, power consumption and noise, a new two-stage simple-architecture UWB LNA using an active inductor is proposed as shown in Figure 4.19.

The first stage of the new LNA is a resistive-feedback inverter amplifier (consisting of transistors M1 and M2, and resistor $R_F$). The resistive shunt-feedback (with $R_F$) establishes the DC biasing voltage for the inverter amplifier around the mid-point of the supply voltage ($V_{DD}$) and provides stable DC operating points for the entire LNA. The second-stage is a resistive-load common-source amplifier (consisting of M3 and $R_D$). A tunable active in-

ductor (Figure 4.2) is connected at the output node (at Node 1) of the inverter amplifier in exploiting the active shunt-peaking. The input matching is achieved using the combined transconductances ($g_{m1}$ plus $g_{m2}$) of transistors M1 (NMOS) and M2 (PMOS) while feedback resistor $R_F$ sets the DC bias voltage. At Node 1, the overall capacitance $C_1$ includes the gate-source capacitance of transistor M3 ($C_{gs3}$), which is significantly high for the large size of transistor M3). Therefore, the frequency response of the amplifier rolls-off fast at high frequency due to the diminishing capacitive impedance of $C_1$. Here, at node 1, with increasing frequency, the increasing inductive impedance of the active inductor compensates the losses of the signals through the diminishing capacitive impedance. Thus, the bandwidth is increased in exploiting the shunt peaking caused by the active inductor. The inverter amplifier works as a transresistance amplifier and exhibits a low input impedance and this makes the input matching simpler at the cost of reduced gain. Like three-stage LNA, the gain is also traded with input matching. The output common-source amplifier stage boosts the overall gain, and provides the output matching. An additional active inductor at the output node (Node 2) of common-source amplifier further enhances the bandwidth by cancelling capacitance at this node. The input impedance, gain and noise-figure of the proposed two-stage LNA are described in the following sections.

### 4.3.1 Input Impedance

For the derivation of the expression for input impedance ($Z_{in}$), the small-signal equivalent circuit of the two-stage LNA is shown in Figure 4.20. At low-frequencies, the input impedance, $Z_{in}$ ($= R_{in}$) of the LNA is expressed as

$$R_{in} \approx \frac{1}{g_{m1} + g_{m2}}, \tag{4.34}$$

where $g_m$ with subscripts 1 and 2 represents the transconductance of transistor M1 and M2, respectively. Hence, in order to achieve the broadband input matching ($R_{in} = R_S$=50Ω), the sum of $g_{m1}$ and $g_{m2}$ needs to be equal to 20.0 mS (mA/V). Using small sizes of transistors, and spending a reasonable

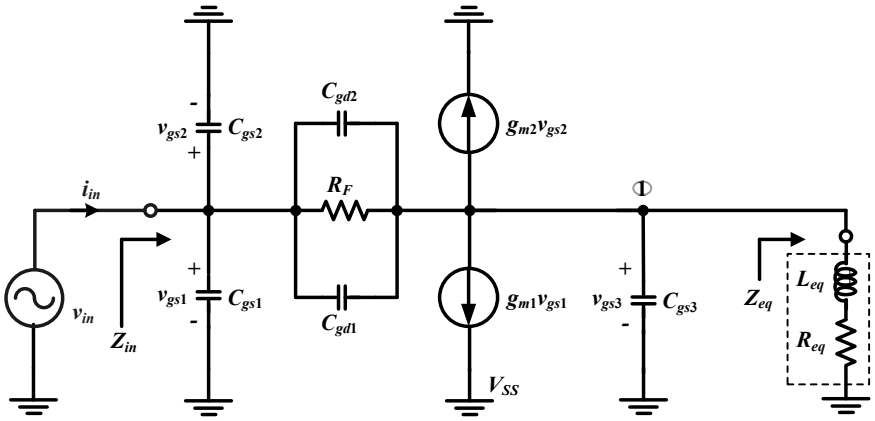


Figure 4.20: Small-signal circuit for input-impedance of two-stage LNA.

amount of current, the required $g_{m1}$ and $g_{m2}$ can be obtained to achieve the input matching. Alternatively, large sizes of transistors and a small amount of current can also provide input matching. However, the input matching using the smaller transistors are preferable because of the increased operating frequency caused by the low capacitances of small-size transistors. Note that the resistive-feedback amplifier exhibits low input resistance and can be considered as a translinear amplifier where transresistance is approximately equal to $R_F$.

At high frequency, all the capacitances of the transistors in the LNA need to be considered. The input impedance $Z_{in}$ at high frequency can be expressed as

$$Z_{in} = \frac{1 + (\frac{1}{Z_{eq}} + sC_1).\frac{R_F}{1 + sR_FC_{gd}}}{(g_{m1} + g_{m2}) + sC_{gs} + (\frac{1}{Z_{eq}} + sC_1).\frac{1 + sR_F(C_{gs} + C_{gd})}{1 + R_FC_{gd}}}, \qquad (4.35)$$

where $C_{gd}$ (=$C_{gd1} + C_{gd2}$) and $C_{gs}$ (=$C_{gs1} + C_{gs2}$) are the combined gate and drain capacitances of transistor M1 and M2 respectively. $C_1$ is the total capacitance at node 1 including the gate-source capacitance ($C_{gs3}$) of transistor M3. $Z_{eq}$ is the equivalent inductive impedance looking toward the active inductor.

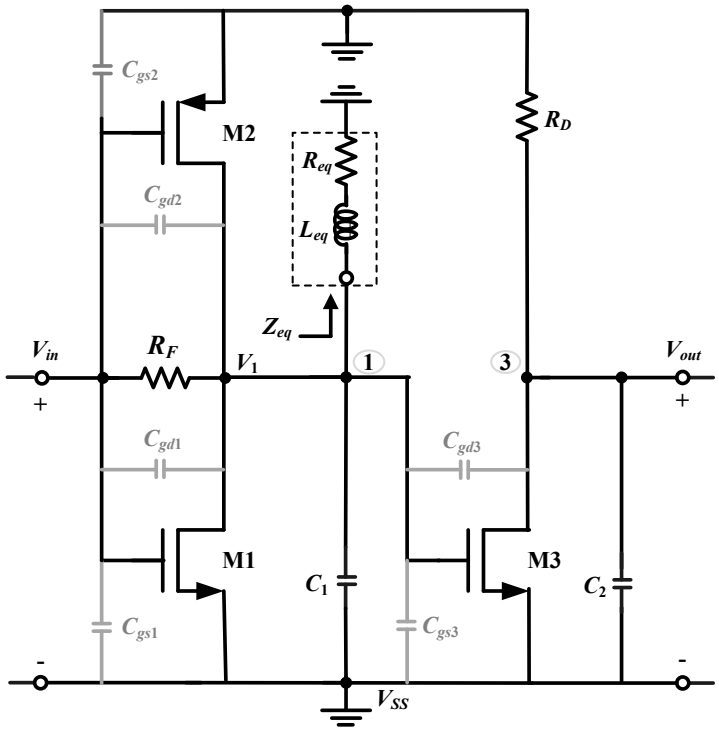


Figure 4.21: Small-signal circuit of two-stage LNA for gain.

Note that at low frequency, $Z_{in}$ equals the resistance as expressed by Equation 4.34. Assuming $Z_{eq}$ is purely inductive ($\approx sL_{eq}$) and it is intended to cancel the node capacitance $C_1$, the input impedance is simplified to

$$Z_{in} \approx \frac{1}{(g_{m1} + g_{m2}) + s(C_{gs1} + C_{gs2})}. \tag{4.36}$$

### 4.3.2 Gain-Bandwidth

The voltage gain, $A_v(s)$ of the proposed two-stage amplifier is $A_{v1}(s).A_{v2}(s)$ where $A_{v1}(s)$ and $A_{v2}(s)$ are the gain of the first stage and the second stage, respectively. Figure 4.21 shows the small-signal circuit of the proposed two-stage LNA to obtain the expression for gain. The capacitances of the transistors taken into consideration are shown with shaded parts. The gain of the

first-stage shunt-feedback amplifier is

$$A_{v1}(s) = \frac{v_1}{v_{in}} \approx -\frac{(g_{m1} + g_{m2}) - s(C_{gd1} + C_{gd2})}{\frac{1}{R_F} + \frac{1}{R_{eq} + sL_{eq}} + sR_F(C_{gd1} + C_{gd2} + C_1)}, \tag{4.37}$$

where $C_1$ is the overall node capacitance at node 1 including the gate-source capacitance $C_{gs3}$ of M3. The above equation 4.37 is approximated with $(g_{m1} + g_{m2})R_F \gg 1$. At low frequencies, the gain is

$$A_{v01} \approx -(R_F \parallel R_{eq})(g_{m1} + g_{m2}). \tag{4.38}$$

Because of the coupling capacitor $C_c$, $R_{eq}$ does not come into effect, the low frequency gain becomes:

$$A_{v01} \approx -R_F(g_{m1} + g_{m2}). \tag{4.39}$$

Hence, taking $R_F$ in the range of 180-200 $\Omega$ and $(g_{m1} + g_{m2})$ of 20.0mS, the gain obtained is 3.6-4.0 (or 5.0-6.0 dB in logarithmic scale), which is not high enough. The gain of the second stage common-source amplifier is

$$A_{v2}(s) = \frac{v_0}{v_1} \approx -\frac{R_D(g_{m3} - sC_{gd3})}{1 + sR_D(C_{gd3} + C_2)}, \tag{4.40}$$

where $C_2$ is the output node capacitance. At low frequencies, the gain $A_{v02}$ is

$$A_{v02} \approx -R_D g_{m3}. \tag{4.41}$$

Choosing $R_D$ of 120$\Omega$ and creating $g_{m3}$ of 80.0 mS, the gain can be obtained as 9.6 (or 9.8dB in logarithmic scale) which is high and thus, two stages together can provide a low-frequency gain of approximately 15.0dB.

With increasing frequency, increasing inductive impedance of $L_{eq}$ at Node 1 compensates for diminishing capacitive impedance of $C_1$. This keeps the frequency response of the amplifier flat up to a very high frequency by reducing losses at high frequencies. Thus, the bandwidth of the LNA is increased due

to flat frequency response up to an extended frequency range.

### 4.3.3 Noise Factor

Like the three-stage LNA, the noise factor ($F$) of the proposed two-stage LNA is mainly determined by the noise factor of the first-stage shunt-feedback amplifier. Unlike the three-stage amplifier, a few components contribute to the overall noise-figure ($NF$) of the two-stage LNA. Considering the thermal noise is the significant only, the important thermal noise sources are input transistors M1 and M2, feedback resistor $R_F$, and the equivalent resistor $R_{eq}$ of the active inductor. The $F$s of these noise-sources with respect to the source resistance $R_S$ are:

$$F_{M1} \approx \frac{\gamma_1}{g_{m1}R_S}. \tag{4.42}$$

$$F_{R_{eq}} = \frac{R_{eq}}{R_S(g_{m1}+g_{m2})_2R_F^2}. \tag{4.43}$$

$$F_{R_F} = \frac{R_S}{R_F}. \tag{4.44}$$

Hence, Using the analysis of the input-referred noise of the two-port network, the $F$ of the LNA with respect to the source-resistance $R_S$ under matching condition ($R_S = R_{in}$) can be expressed as

$$F = 1 + F_{M1} + F_{M2} + F_{R_{eq}} + F_{R_F}, \tag{4.45}$$

or

$$F = 1 + \frac{\gamma_1}{g_{m1}R_S} + \frac{\gamma_2}{g_{m2}R_S} + \frac{R_{eq}}{R_S(g_{m1}+g_{m2})^2R_F^2} + \frac{R_S}{R_F}, \tag{4.46}$$

Note that large transconductances ($g_{m1}$ and $g_{m2}$) reduce the noise factor $F$, and the lower limit of the $F$ is bounded by the term $R_s/R_F$. The minimum $NF$ ($NF_{min}$) is still the same range as in the three-stage LNA. The third term in Equation 4.46 defines the noise contribution of the active inductor to the core LNA. Here, $R_F$ reduces the $NF$ but the reduction is less than that of Equation

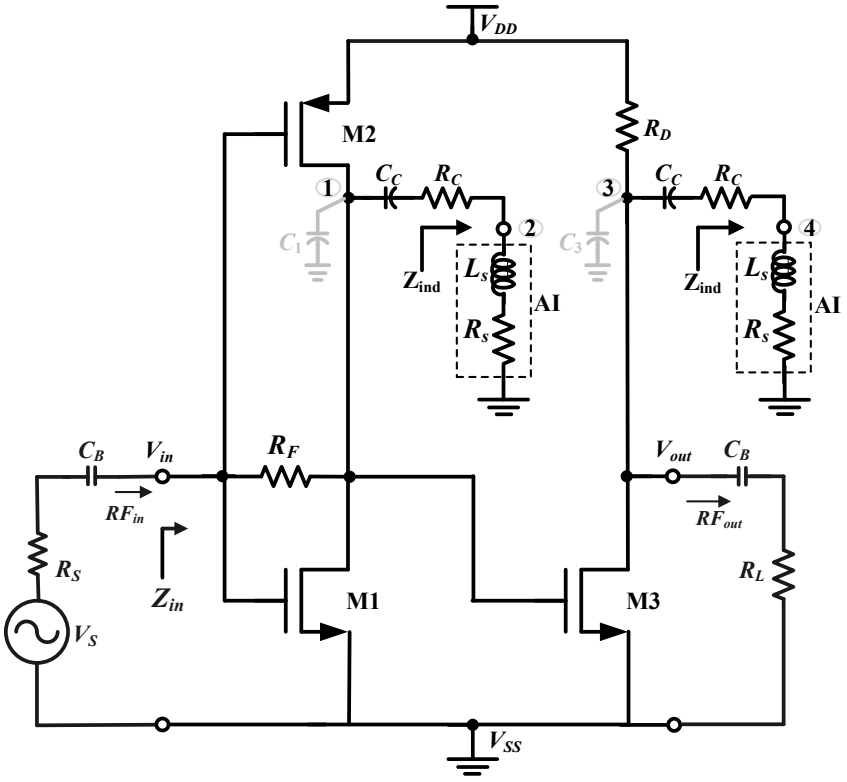


Figure 4.22: Proposed two-stage LNA using two active inductors.

4.29 because $R_F$ is smaller than the output resistance $r_{03}$ of transistor M3 in the three-stage LNA. Overall, a smaller number of components in the two-stage LNA contribute less noise, and it is easily predictable that the overall *NF* of the LNA will be lower than that of the three-stage LNA.

### 4.3.4 Bandwidth Extension

In the proposed two-stage LNA of Figure 4.19, the upper limit of the overall bandwidth is also limited by capacitance $C_2$ as obtained in gain expression of $A_{v2}$ (Equation 4.40). Note that $C_2$ is the output node capacitance of the second-stage common-source amplifier. As in the three-stage LNA, another active inductor is connected at the output node (at Node 2) of the common-source amplifier resulting in the modified two-stage LNA of Figure 4.22. Here,

the inductive impedance of the active inductor compensates for the diminishing capacitive-impedance of $C_2$ at high frequencies and extends the bandwidth.

### 4.3.5 Design and Simulation of Two-Stage LNA

The proposed two-stage UWB LNA in Figure 4.19 is designed in TSMC 90nm CMOS digital CMOS process. Device sizes (width$=W$ and length $=L$) are chosen based on their applications. The core two-stage LNA consists of only three transistors (M1, M2 and M3), and all of them are in signal paths. As the transistors used for signal-amplification, M1 to M3 are chosen with large widths of 60$\mu$m, 60$\mu$m and 81$\mu$m respectively while all of them have the length ($L$) of 100nm. These transistors are also multi-fingered structures of 40(N) $\times$ 1.5$\mu$m ($W$) $\times$ 100nm($L$) for 60$\mu$m width and 54(N) $\times$ 1.5$\mu$m($W$) $\times$ 100nm($L$) for 81$\mu$m. $N$ is the number of fingers of the transistors.

The LNA is simulated with with 50$\Omega$ ($R_S$=$R_L$=50$\Omega$) terminations. With a supply voltage of 1.2V and $V_{tune}$ of 650mV for the active inductor, the LNA draws a total current of 11.5mA including a current of 320$\mu$A consumed by the active inductor.

The effects of active inductors on the proposed two-stage UWB LNAs can be observed more vividly with simulation results. Figure 4.23 shows the simulated gain ($S_{21}$) of the two-stage LNA with active inductor (WI-AI), and without active inductor (WO-AI) for $V_{DD}$ of 1.2V and $V_{tune}$ of 650mV. Without the active inductor, the core LNA exhibits simulated $S_{21}$ (plot of WO-AI) of 17.0dB at 2.0GHz and 13.0dB at 10.0GHz. Hence, there is a 4.0dB variation of gain (not flat gain) over 2.0-10.0 GHz, and the -3dB bandwidth is reduced to 2.0-8.8 GHz. On the other hand, with an inductor at the input stage, the LNA shows a flat $S_{21}$ (plot of WI-AI) of 15.0dB over 2.0-9.9 GHz, and the -3dB $BW$ extends over 2.0-14.2 GHz.

Figure 4.24 shows the simulated noise figure ($NF$) of the two-stage LNA without active inductors and with active inductors (one and two inductors) for $V_{DD}$ of 1.2V and $V_{tune}$ of 650mV. Without active inductor (WO-AI), the LNA shows a $NF$ of 2.7-3.0 dB over 2.0-12.5 GHz bandwidth but with one active inductor (WI-1AI), a $NF$ of 3.2-3.8 dB is obtained over the same band-

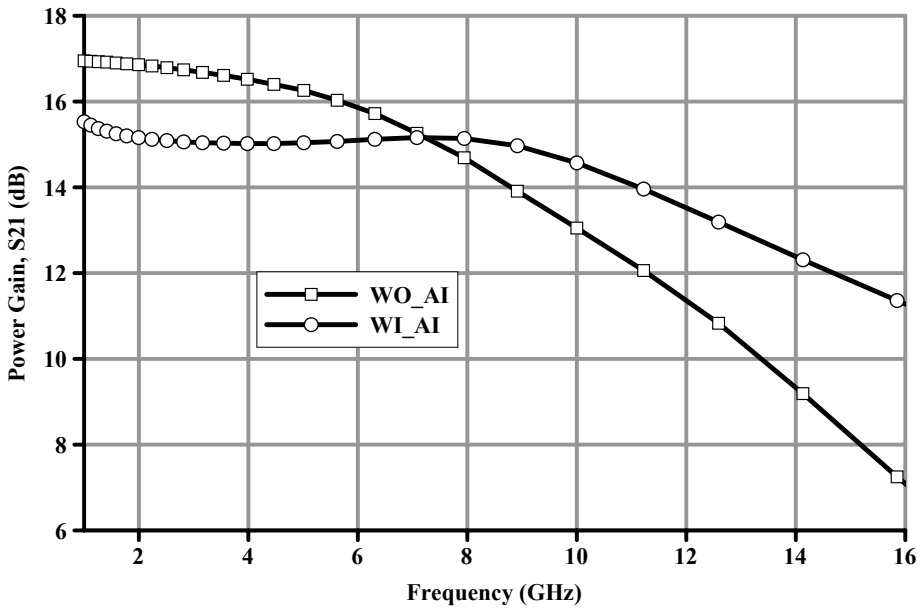


Figure 4.23: Simulated gain of two-stage LNA with and without inductors.

width. Using two inductors (WI-2AI) (the second inductor at the output of the second-stage common-source amplifier), the *NF* of the LNA slightly degrades (increases by 0.2dB) from that of using one inductor. The second active inductor at the final output of the LNA is physically apart from its input and therefore, it does not contribute a significant amount of noise to the overall *NF* of the LNA.

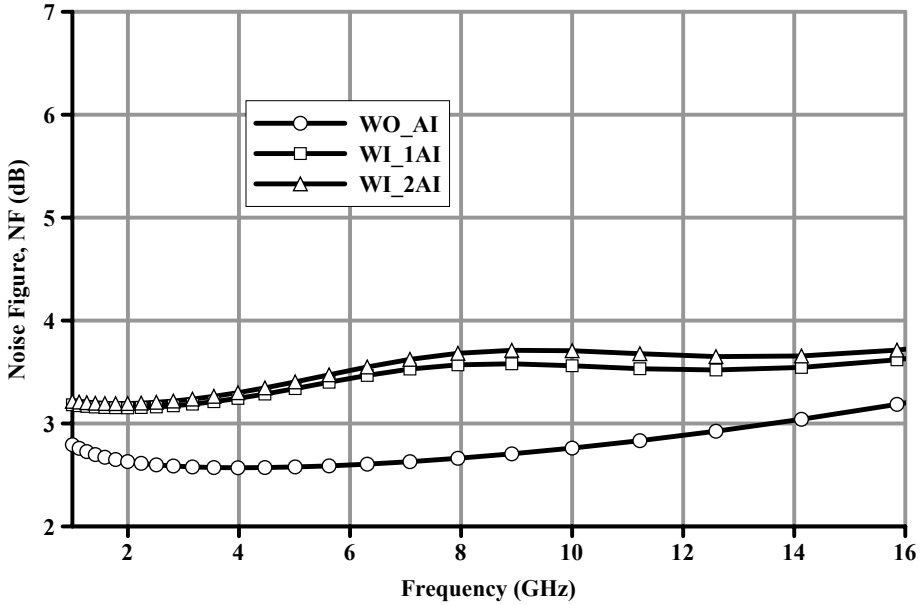


Figure 4.24: Simulated noise figure of two-stage LNA with and without inductors.

## 4.4 Measurement of Two-Stage UWB LNA

The proposed two-stage UWB LNA in Figure 4.19 is implemented in a nine metal TSMC 90nm CMOS digital CMOS process. The die photo of the fabricated two-stage LNA is shown in Figure 4.25. The core LNA occupies an active chip area of 0.011mm$^2$ (110$\mu$m $\times$ 100$\mu$m) and the overall chip-area including all the bonding pads is 0.06mm$^2$.

### 4.4.1 Measurement Results

The measurement setup has been described earlier for the three-stage LNA. The fabricated two-stage LNA is also measured on-wafer using G-S-G (ground-signal-ground) probes for RF signals, and is measured for S-parameters, *IIP*3 and 1-dB *CP*.

Operated with a 1.2V power supply, the fabricated two-stage LNA draws a current of 10.8mA with a $V_{tune}$ of 650mV for the active inductor. In simula-

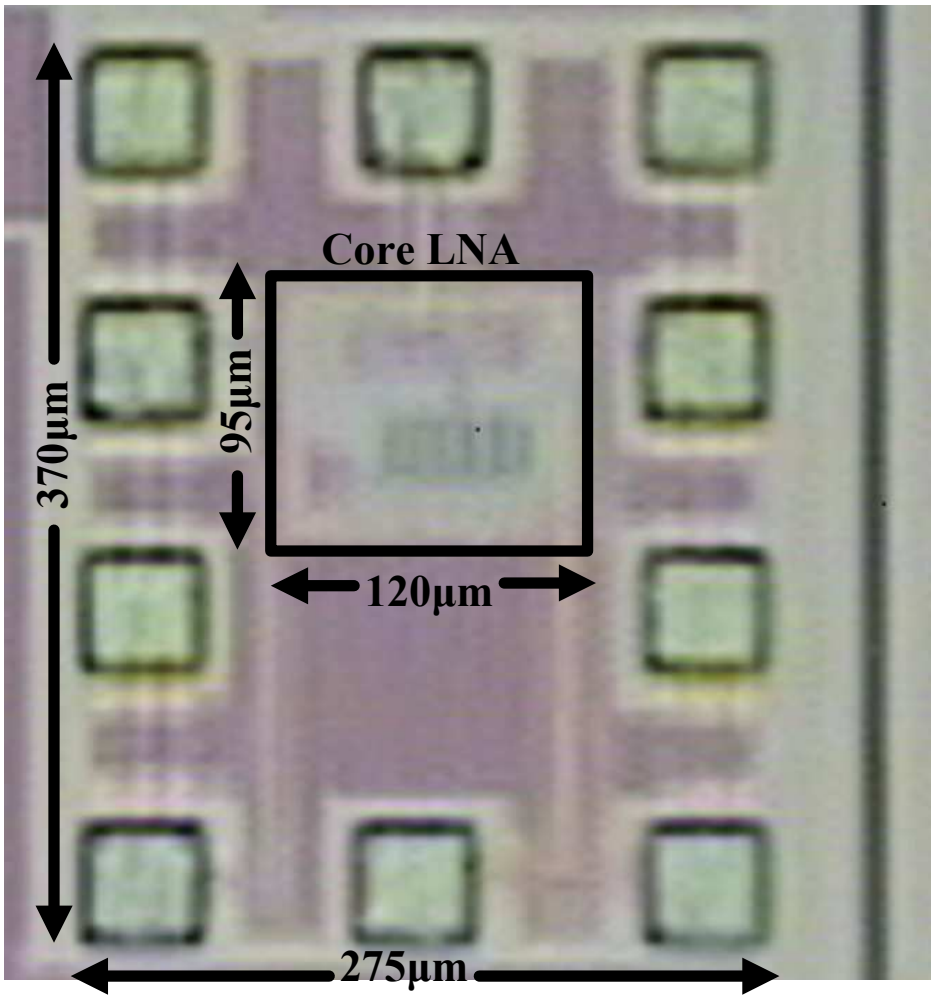


Figure 4.25: Microphotograph of fabricated two-stage LNA.

tion, the LNA draws a total current of 11.5mA including a current of 320$\mu$A consumed by the active inductor. Figure 4.26 exhibits the measured and simulated power gain ($S_{21}$) of the two-stage LNA. The measured $S_{21}$ is 13.4dB with a 3dB $BW$ of 2.5-11.2 GHz. Note that the measured $S_{21}$ and $BW$ are reduced by 1.0dB and 400 MHz from the simulated $S_{21}$ and $BW$ of 14.4dB and 2.5-11.6 GHz, respectively. The two-stage LNA exhibits a measured $NF$ of 3.4-5.0 dB over 2.5-11.0 GHz whereas the simulated $NF$ is 3.1-3.6 dB as shown

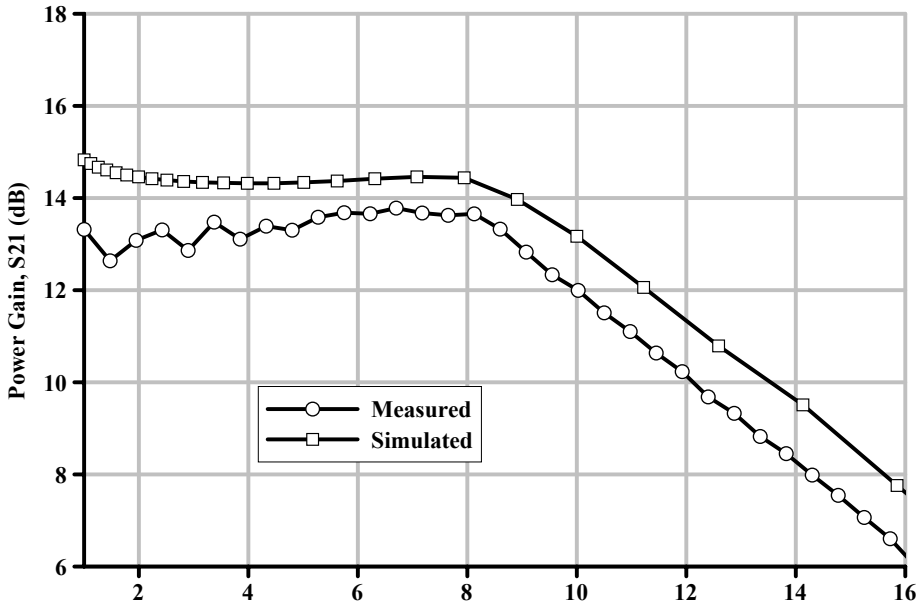


Figure 4.26: Measured and simulated gain of two-stage LNA.

in Figure 4.27. The measured *NF* of the two-stage LNA degrades by 1.1dB from the simulated *NF*. Figure 4.28 shows the measured and simulated input ($S_{11}$) and output ($S_{22}$) return losses of two-stage LNA. The measured $S_{11}$ and $S_{22}$ are less than -15.0dB and -19.0dB, respectively over the frequency range of 2.5-11.0 GHz. Both measured $S_{11}$ and $S_{22}$ are below -10.0dB over the desired bandwidth. Hence, the input and output impedances achieve broadband matching with the source and load impedances. For $S_{11}$ and $S_{22}$, the discrepancies between measured and simulated results have already been described for the three-stage LNA. Figure 4.29 shows the measured and simulated reverse isolation ($S_{12}$) of the fabricated two-stage LNA. The measured $S_{12}$ is below -28.0dB over 2.5-11.0 GHz and follows the pattern of the simulated $S_{12}$ with a reduced value.

Figure 4.30 shows the gain-$BW$ tuning of the two-stage LNA with $V_{tune}$ of 550mV, 650mV and 750mV for the active inductors. With $V_{tune}$ of 750mV, the measured gain ($S_{21}$) obtained is 15.4dB but the bandwidth ($BW$) is reduced to 2.5-8.6 GHz. On the other hand for $V_{tune}$ of 500mV, the $BW$ is extended over

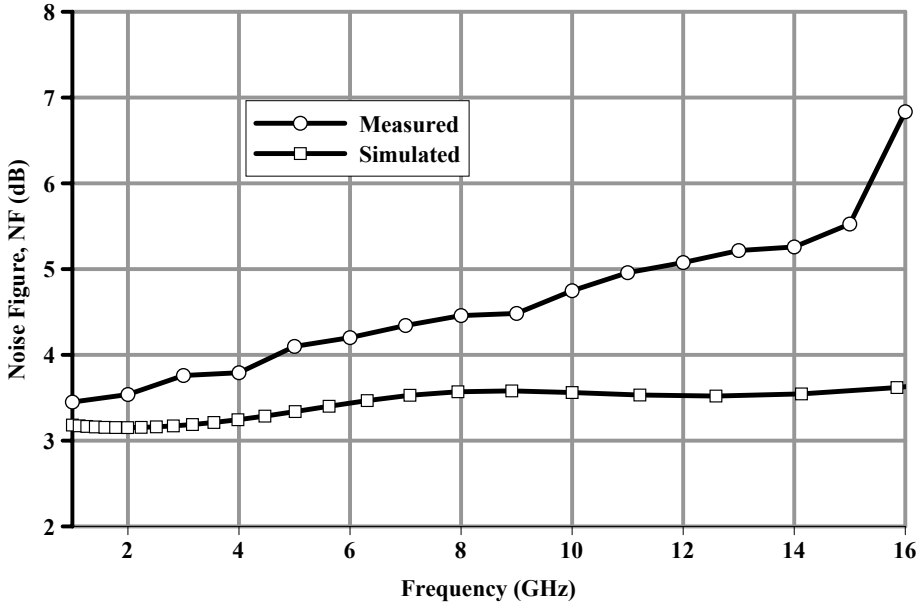


Figure 4.27: Measured and simulated noise figure of two-stage LNA.

2.5-13.4 GHz but $S_{21}$ is reduced to 11.6dB. The reasons for the variation of the gain and bandwidth with different values of $V_{tune}$ has been earlier described for the three-stage LNA.

The two-stage LNA exhibits measured 1-dB *CP* of -13.7dBm as shown in Figure 4.31. Like three-stage LNA, input *IP*3 (*IIP*3) of the fabricated two-stage-LNA is also measured with a two-tone test of applying two signals at 1.0MHz apart (one is at 5.0GHz and another one is at 5.001GHz). The LNA exhibit measured *IIP*3 of -4.2dBm as shown in Figure 4.32.

The possible causes of discrepancies between measured and simulated results are similar to those as described earlier for the three-stage UWB LNA. The fabricated two-stage LNA is also measured on different samples to observe the design robustness of the LNA and die yield. Figure 4.33 shows the gain ($S_{21}$) of the two-stage LNA measured on four (4) different dies. Note that the variation of the measured $S_{21}$ on different samples is within 0.5dB. Here, the results of the LNA are well repeated on different samples, and the process exhibits a good yield.

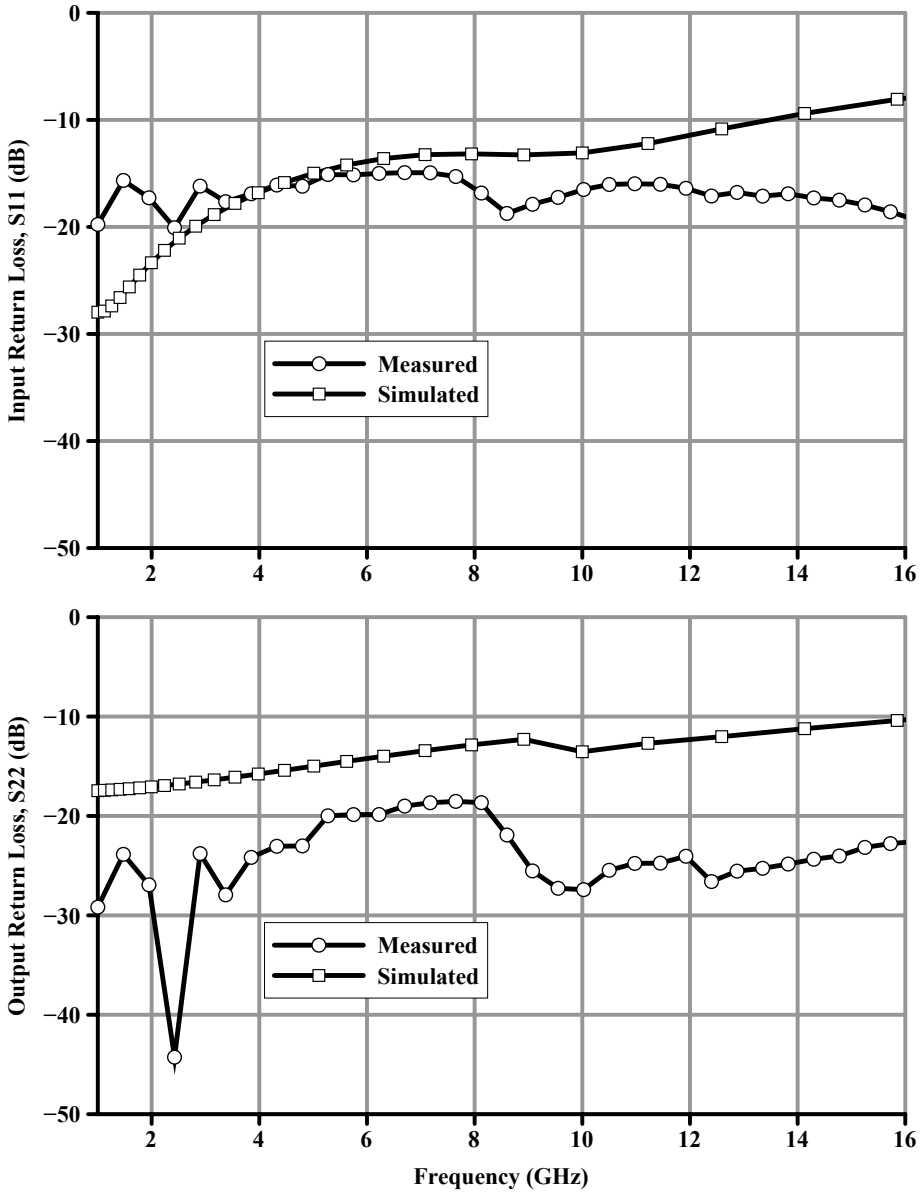


Figure 4.28: Measured and simulated return losses of two-stage LNA

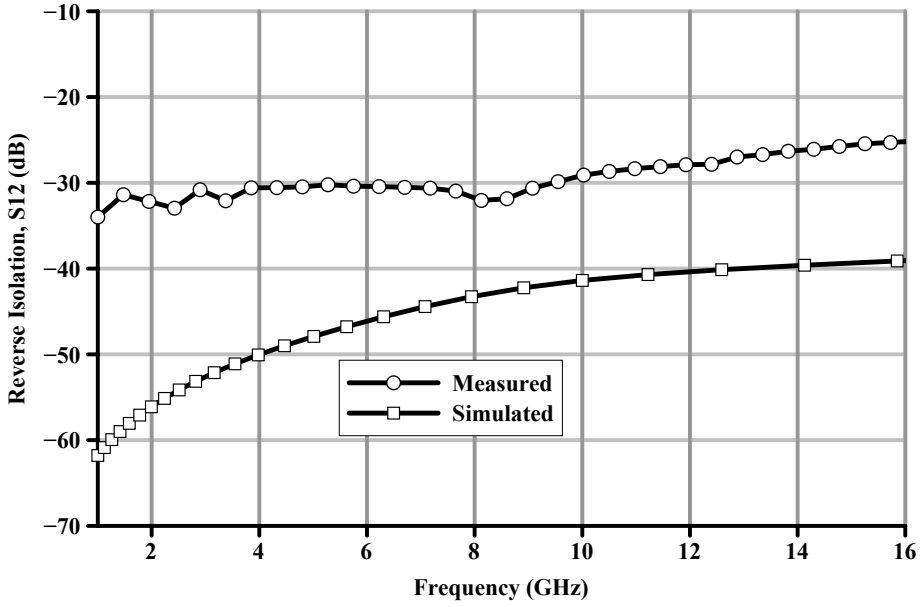


Figure 4.29: Measured and simulated reverse isolation of two-stage LNA.

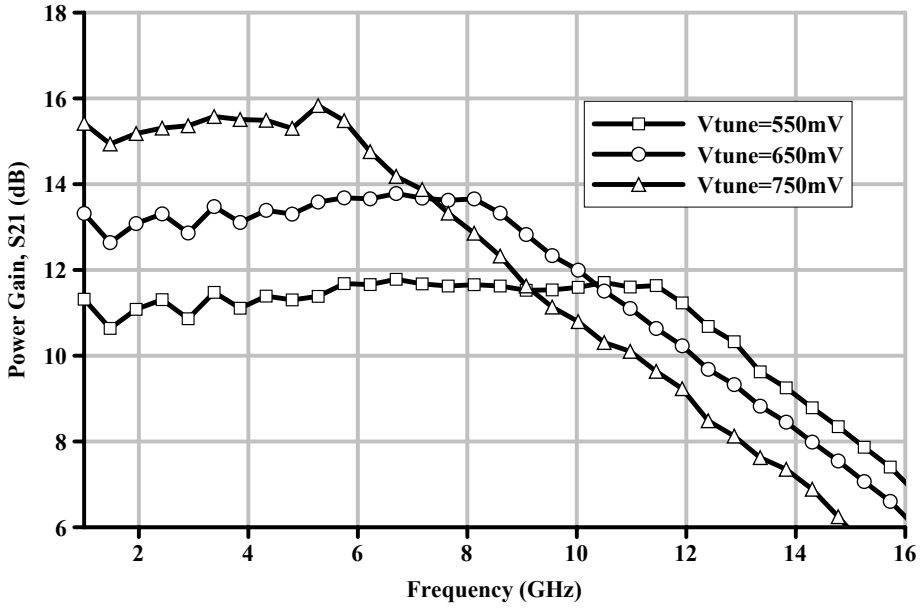


Figure 4.30: Tuning of measured gain-bandwidth of two-stage LNA.

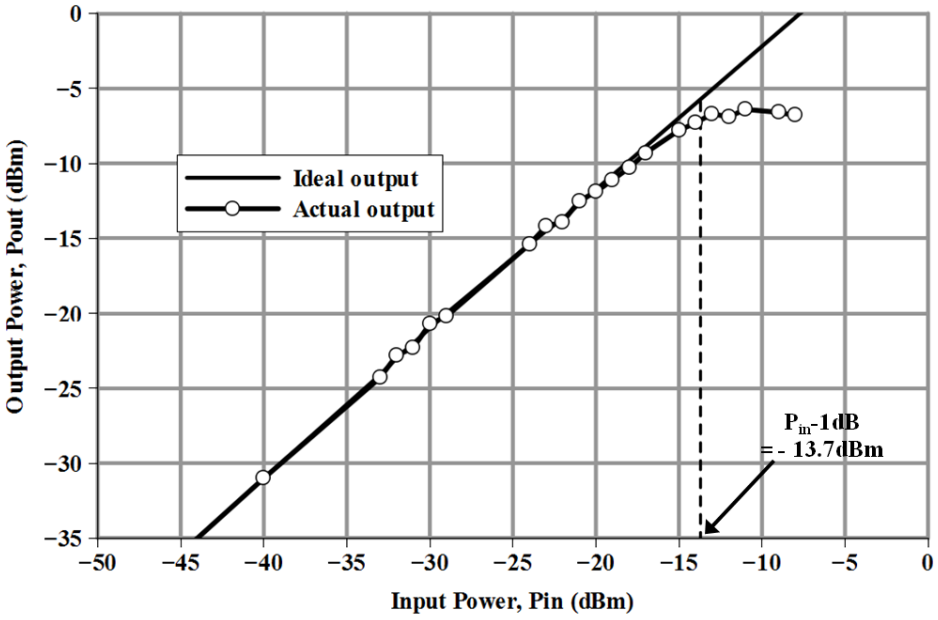


Figure 4.31: Measured 1-dB *CP* of two-stage LNA.

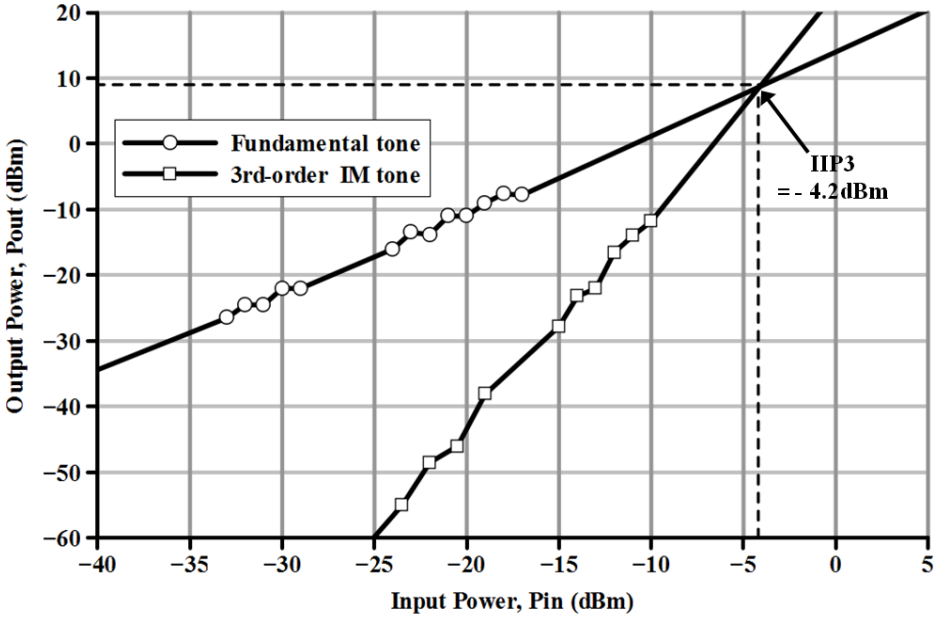


Figure 4.32: Measured input *IP*3 (*IIP*3) of two-stage LNA.

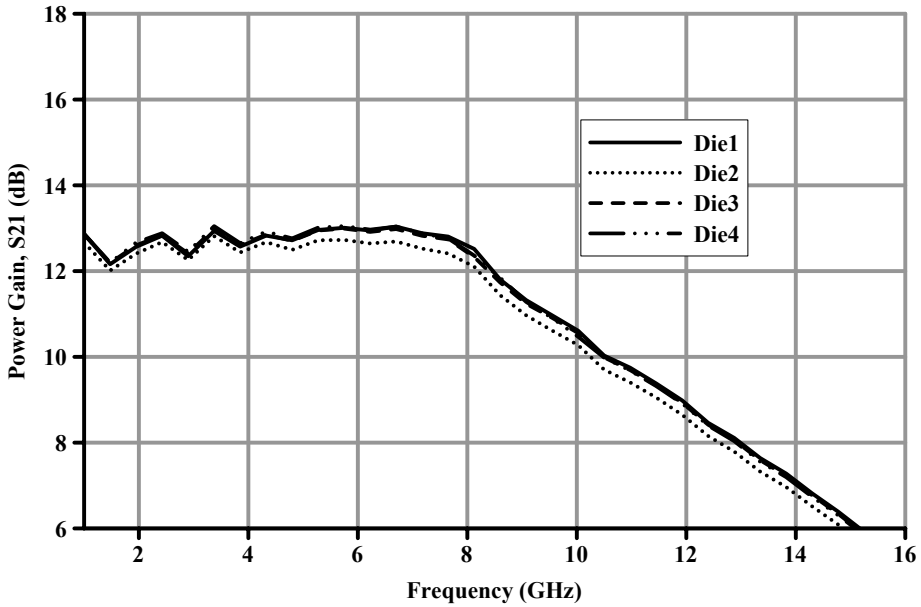


Figure 4.33: Measured gain of two stage LNA on different dies.

### 4.4.2 Performance Summary and Comparison

The performances of our proposed two-stage ($LNA_2$) and three-stage ($LNA_3$) UWB LNAs are summarized in Table 4.3, and are compared with those of the recently published UWB LNAs in the literature. The LNA in [40] exhibits a higher gain with a higher power consumption but our proposed LNAs exhibit wider bandwidth at lower power consumption. Although the proposed UWB LNAs in this thesis use active inductors, they exhibit relatively low noise figures over the desired UWB bandwidth. The active inductors are connected at the outputs of the amplifying stages in our proposed UWB LNAs and therefore, they do not contribute to the significant increase of the noise figures. The UWB LNAs in the literature [35, 41, 42] do not achieve broadband input matchings as their input-return losses ($S_{11}$) are higher than -10.0dB. Although using active inductor, the proposed two-stage LNA ($LNA_2$) in this thesis has relatively higher $IIP3$ because in this two-stage LNA, $IIP3$ is bounded by the second-stage common-source amplifier, which do not use an active inductor.

Table 4.3: Performance summary and comparison of UWB LNAs.

| REF. | Technology [CMOS] | $BW$ [GHz] | $S_{21}$ [dB] | $NF$ [dB] | $S_{11}$ [dB] | $IIP3$ [dBm] | $P_{Diss}$ [mW] | Core area $mm^2$ |
|---|---|---|---|---|---|---|---|---|
| [11] | 0.18$\mu$m | 2.3-9.2 | 9.3 | 4.0-9.2 | <-9.9 | -6.7 | 18.0 | 0.66 |
| [33] | 0.18$\mu$m | 0.4-10.0 | 12.4 | 4.4-6.5 | <-10.0 | -6.0 | 12.5 | 0.42 |
| [35] | 0.18$\mu$m | 0.1-11.0 | 8.0 | 2.9- | <-5.0 | -3.5 | 21.6 | 0.76 |
| [44] | 0.18$\mu$m | 1.2-11.9 | 9.7 | 4.5-5.1 | <-11.0 | -6.2 | 20.0 | 0.59 |
| [45] | 0.13$\mu$m | 2.0-5.2 | 16.0 | 4.7-5.7 | <-9.0 | n/a | 38.0 | 0.24 |
| [41] | 0.13$\mu$m | 2.0-9.6 | 11.0 | 3.6-4.8 | <-8.3 | -7.2 | 19.0 | 0.05 |
| [42] | 0.13$\mu$m | 1.5-8.1 | 11.7 | 3.6-6.0 | <-9.0 | -6.7 | 11.62 | 0.58 |
| [43] | 90nm | 2.0-11.0 | 12.0 | 5.2-5.9 | <-10.0 | -4.0 | 17.0 | 0.696 |
| [40] | 90nm | 3.5-8.4 | 22.7 | 6.0-6.4 | <-10.5 | n/a | 34.8 | 0.685 |
| [$LNA_2$] | 90nm | 2.5-11.2 | 13.4 | 3.1-5.0 | <-15.0 | -4.2 | 12.96 | 0.0114 |
| [$LNA_3$] | 90nm | 3.0-8.8 | 17.6 | 3.6-5.1 | <-11.5 | -6.4 | 16.56 | 0.0227 |

The UWB LNAs in [41, 43] exhibits improved linearity with a slightly higher $IIP3$ than that of our proposed two-stage UWB LNA ($LNA_2$). Note that the $LNA_2$ consumes a lower amount of power (12.96mW) than the those of the LNAs in [41] (17.0mW) and [43] (22.0mW) leading to a lower $IIP3$.

All the LNAs but the one in [41] use on-chip passive inductors leading to occupying a larger chip areas. Our proposed UWB LNAs use active inductors and exhibit moderate performance but occupy the lowest chip areas. Moreover, these LNAs ($LNA_2$ and $LNA_3$) are tunable with varying gain and bandwidth. The two-stage UWB LNA can be tuned with a varying gain of 13.4dB to 15.4dB, and the upper limit of its bandwidth can be tuned from 8.6GHz to 11.2GHz. The upper limit of the bandwidth of the three-stage UWB LNA can be tuned in the range of 7.6GHz to 9.8 GHz, and the gain can be varied from 17.6dB to 19.4dB. Hence, with tunability, our proposed UWB LNAs ($LNA_2$ and $LNA_3$) are overtaking the performances of the UWB LNAs in the literature.

# Chapter 5

# Active CMOS Multiband UWB Receiver Front-End

This chapter presents a new area-efficient CMOS multiband (MB) ultra-wideband (UWB) receiver front-end that does not use any passive inductors. This active CMOS UWB receiver front-end consists of passive inductorless RFICs, namely active CMOS RFICs, a low-noise amplifier (LNA), mixers, and local oscillator (LO) drivers. First, an area-efficient UWB mixer and a wideband LO driver are designed using very low chip-area tunable active inductors, which exploit wideband active shunt peaking for bandwidth extension. Then, two identical UWB mixers driven by two identical wideband LO drivers are integrated with a two-stage area-efficient CMOS UWB LNA (presented in Chapter 4) to implement the proposed UWB front-end with a direct-conversion architecture. Fabricated in a 90nm digital CMOS process, the measurement results of the passive inductorless area-efficient tunable UWB receiver front-end are presented.

## 5.1 Design of CMOS UWB Mixers

### 5.1.1 Mixer Basics

In a receiver chain, just after the antenna, the LNA and mixer mainly deal with RF signals; therefore, they are considered as the core circuits of the RF

front-end of the receiver. The LNA amplifies very weak RF signals received by the antenna, and the mixer switched by LO signals, converts amplified RF signals to intermediate-frequency (IF) signals. The frequency translation or conversion (RF-to-IF) in a mixing operation can be achieved by multiplying an RF signal with a frequency of $\omega_{RF}$ by a square-wave LO signal alternating between $\pm 1$ at a frequency of $\omega_{LO}$. With this mixing technique, the IF output voltage $V_{IF}$ is proportional to the input RF voltage $V_{RF}$ only. Expanding the square-wave LO signal $square(\omega_{LO}t)$ with Fourier series, mathematically, the IF signal can be expressed as [46]

$$\begin{aligned} V_{IF} &= V_{RF}cos(\omega_{RF}t) \times Square(\omega_{LO}) \\ &= V_{RF}cos(\omega_{RF}t) \times \frac{4}{\pi}[cos(\omega_{LO}t) + \frac{1}{3}cos(3\omega_{LO}t)t + ...] \\ &= \frac{2V_{RF}}{\pi}cos(\omega_{RF}t - \omega_{LO}t) + ..., \\ &= \frac{2V_{RF}}{\pi}cos(\omega_{IF}t) + ..., \end{aligned} \tag{5.1}$$

where $V_{RF}$ is the peak amplitude of the RF signal and the down converted IF frequency ($\omega_{IF}$) is $\omega_{RF} - \omega_{LO}$. The higher-order terms other than IF term in Equation 5.1 are typically filtered out. If the ratio of the r.m.s voltage of the IF signal to the r.m.s voltage of the RF signal is greater than unity, then mixers provide voltage conversion gain (in logarithmic scale), and they are called active mixers.

A typical active mixer consists of a transconductance stage for converting the input RF voltage to an RF current, and a switching stage for translating the RF current to an IF voltage. To obtain a high conversion gain and a low noise figure, large-amplitude LO signals are applied for switching. However, they are highly unwanted at the output of a mixer because large-amplitude LO signals can saturate the stages following the mixer, and can also reduce the linearity of the mixer itself [46]. Therefore, to prevent direct feedthrough of LO frequencies to the IF output, double-balanced mixers using a Gilbert cell core as shown in Figure 5.1 are widely used [46]. Here, the Gilbert cell, an analog multiplier, consists of two identical RF transistors M1 to M2 (RF transconduc-

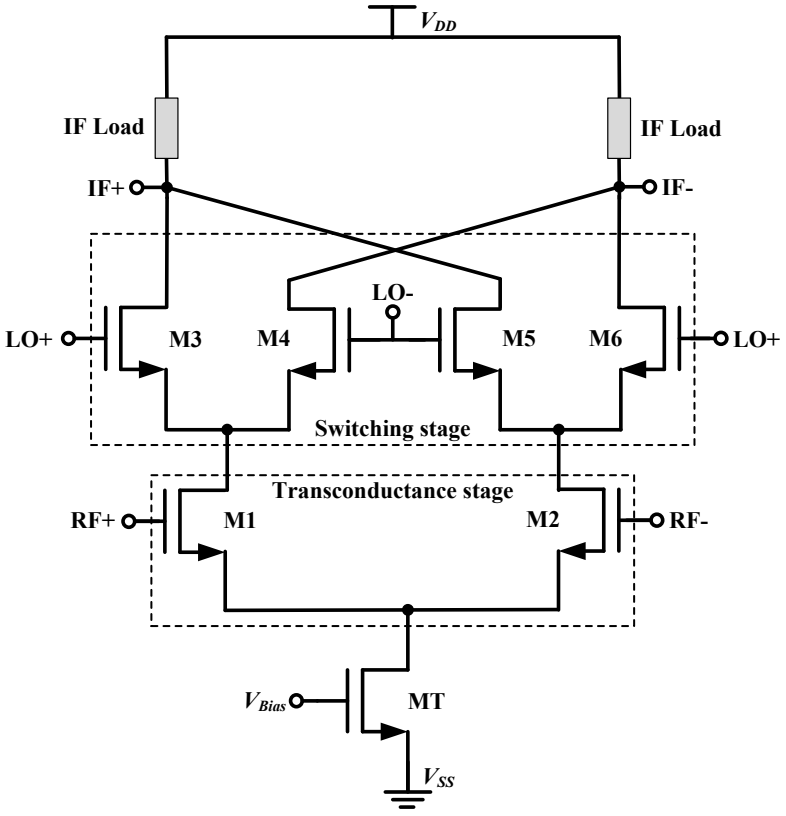


Figure 5.1: Double-balanced Gilbert cell mixer.

tance stage) and four identical LO transistors (M3-M6) (LO switching stage) [47]. The switching of balanced (differential) RF signals ($V_{RF}$+ and $V_{RF}$-) with balanced (differential) LO signals ($V_{LO}$+ and $V_{LO}$-) causes LO signals to be absent at the mixer output [46]. Here, +LO feedthrough from transistor M3 is cancelled by -LO feedthrough from transistor M5, and -LO feedthrough from transistor M4 is cancelled by +LO feedthrough from transistor M6. In the double-balance mixer of Figure 5.1, there is a cascode connection of four devices between power rails (between $V_{DD}$ and $V_{SS}$): an IF load device (a resistor or a transistor), an LO transistor (M3 or M4 or M5 or M6), an RF input transistor (M1 or M2), and a tail-current transistor (MT). Thus, the switching stage sitting on the transconductance stage, double-balanced Gilbert-cell mixers become unsuitable for a low-voltage operation, and also a low DC voltage

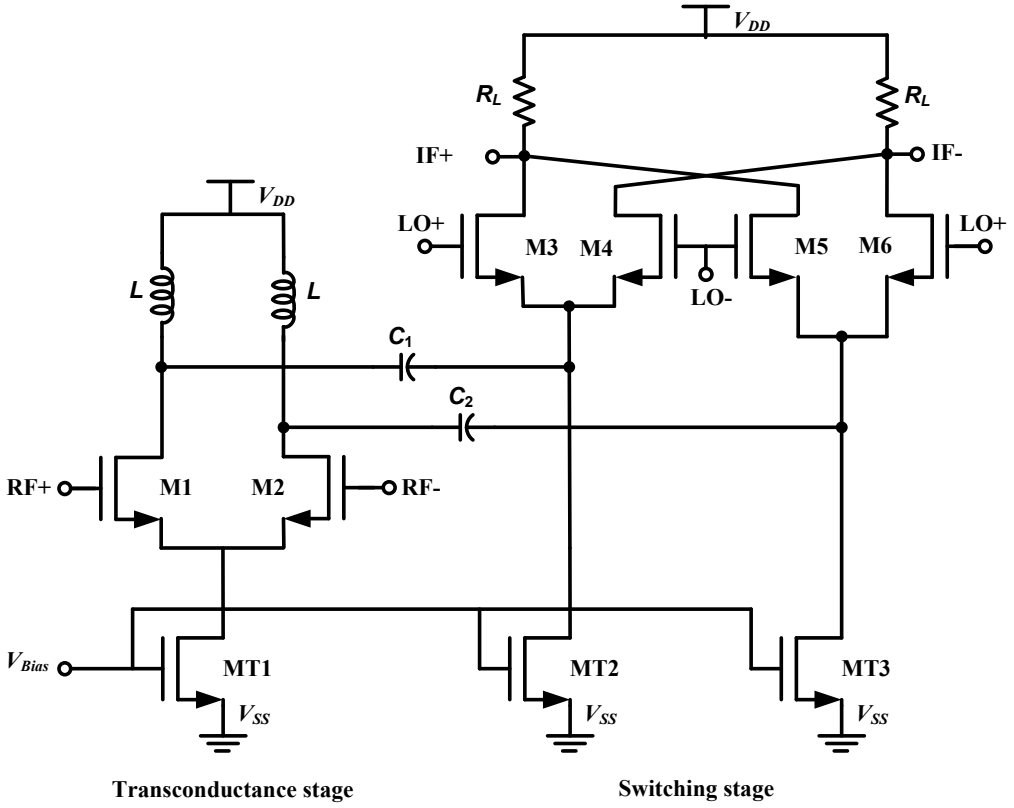


Figure 5.2: Folded switching mixer.

headroom is available at the outputs of mixers for the swing of IF signals.

For a low voltage operation, and for a high DC voltage headroom at the IF output, a CMOS folded switching mixer is shown in Figure 5.2, where the switching stage is folded with respect to the transconductance stage [2]. Note the transconductance stage is AC coupled to the switching stage through coupling capacitors ($C_1$ and $C_2$), and there are three devices between power rails ($V_{DD}$ and $V_{SS}$). Because of inductive loads (no significant voltage drop occurs across it), the transconductance stage can operate even with a lower supply voltage than the switching stage. The CMOS folded switching mixer in the literature [48] uses inverting transconductors for RF inputs (RF+ and RF-), and RF currents from the transconductors are directly (without coupling capacitors) folded to the sources of NMOS switching transistors followed by

resistive IF loads. This folded mixer has only two devices between power rails, and can operate with a lower supply voltage than the folded mixer in Figure 5.2. Another low-voltage folded mixer is reported in the literature [49], where RF currents from the transconductance stage are folded to the sources of PMOS switching transistors followed by resistive IF loads.

RF mixers are also characterized by a set of parameters, similar to those of LNAs: conversion gain (RF to IF gain), noise figure, 1-dB compression point ($CP$) and $IIP3$ (linearity measurement), and port-to-port isolation (RF-to-LO, LO-to-RF and RF or LO to IF). In mixers, the gain is referred as the conversion gain due to the frequency conversion. Because of the switching of the signals, mixers are the most noisy blocks in RF receiver chains. Therefore, besides reducing noise figures of mixers, high gain LNAs are required to reduce overall noise figures of RF front-ends.

In mixers, port to port isolations are critical. LO-to-RF isolation measures how much leakage of LO signals occur at the RF port. In a direct conversion front-end, LO leakages to the RF input port can cause DC offsets because LO and RF frequencies are the same. DC offsets due to self-mixing can corrupt the output of a direct conversion receiver. A symmetric design (physical design) for mixers can cause cancellation of RF and LO signals with each other [46]. A good reverse isolation in LNAs can prevent LO signals reaching the antenna to be radiated [46]. In a direct conversion front-end, LO-to-IF and RF-to-IF leakages are not critical because they are far apart from the IF signals and can easily be filtered out. However, excessive RF and LO leakages to IF port can saturate the circuits that follow the mixer. For UWB applications, RF mixers are mainly optimized for gain and noise figure over a wide bandwidth while having moderate linearity (1-dB $CP$ and $IIP3$).

### 5.1.2 CMOS UWB Mixers

For UWB applications, mixers need to keep their frequency responses (gain over frequency) flat to provide flat conversion gain over a wide bandwidth. Note that for MB-UWB systems, the 7.5GHz UWB spectrum is divided into fourteen bands of 528 MHz each, and these bands are grouped into five dis-

tinct band groups. UWB mixers for MB-UWB systems need to provide flat gain over one or more band groups. The flat conversion gain for UWB mixers allows for designing wideband baseband circuits (post IF circuits) including filters, variable-gain amplifiers, and analog-to-digital converters in receiver chains with lower dynamic range. A low dynamic range for wideband baseband (post IF) circuits makes their implementations less complex using simple circuitry.

Mixers are switched or driven by LO signals, which are typically amplified by LO drivers before feeding to mixers. Along with flat frequency responses of UWB LNAs, the frequency responses of LO drivers also need to be flat to obtain flat conversion gain for UWB mixers over a wide bandwidth. LO drivers are typically two-stage or three-stage amplifiers. Like two-stage or three-stage UWB LNAs as described in Chapter 4, the wideband active shunt-peaking techniques using active inductors can be employed in the transconductance stage of the mixer and the amplifying stages of the wideband LO drivers.

A UWB folded-mixer, exhibiting a conversion gain ($CG$) that drops from 8.0dB to 5.0dB over 0.2-16.0 GHz RF frequency range for a fixed LO power of -2.0dBm, is reported in [50]. This stand-alone mode UWB mixer uses $LC$ matching circuits at LO and RF ports and requires a large chip area because of using passive inductors. Another folded UWB mixer uses two RF chokes of 5.4nH each in the transconductance stage for enhanced conversion gain and extended bandwidth [51]. This UWB mixer exhibits a 2.8dB variation of $CG$ over 3.0-7.0 GHz bandwidth. Two RF chokes of 5.4nH each occupy a large chip area, which is almost seventy (70) percent of the overall chip area. A pair of single-balanced mixers integrated into a direct conversion front-end is presented in [52], and the overall $CG$ of this front-end exhibits a 10.0dB variation over 2.0GHz RF bandwidth. The UWB mixer reported in [51] uses on-chip passive inductors in the transconductance stage and switching stages to increase bandwidth. This mixer exhibits reasonable flat $CG$ of 2.8dB variation over 3.0-7.0 GHz bandwidth. On the other hand, the mixers in [50, 52] do not employ a shunt-peaking technique; and therefore, these mixers experience a wide variation in their conversion gains. Besides occupying large

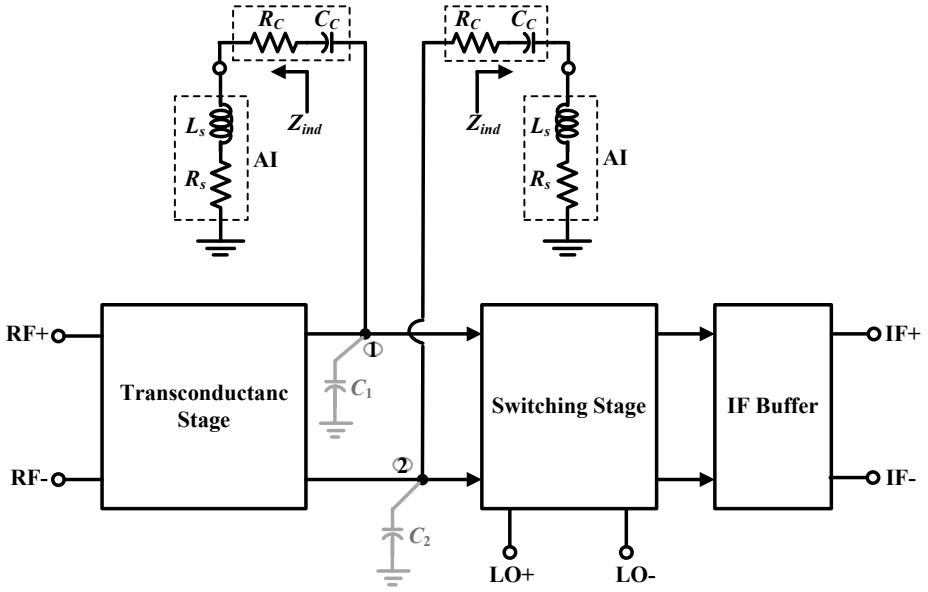


Figure 5.3: Architecture of proposed UWB mixer.

chip areas, all these mixers have a common limitation that they are non-tunable. The tunability of mixers allows for tuning (varying) the gain and bandwidth of the front-end. Here, to achieve a flat conversion gain over a wide bandwidth with tunability, a new architecture for area-efficient UWB mixers is proposed as shown in Figure 5.3. Like area-efficient UWB LNAs as described in Chapter 4, the proposed UWB mixer uses active inductors (AIs) between the transconductance and switching stages to cancel the effects of diminishing capacitive impedances of node capacitances $C_1$ and $C_2$ by exploiting wideband active shunt-peaking for bandwidth extension.

## 5.2 Proposed Tunable UWB Mixer

### 5.2.1 Design of Tunable UWB Mixer

Figure 5.4 shows the schematic of the proposed UWB mixer using active inductors. This is a folded double-balanced mixer consisting of transconductance

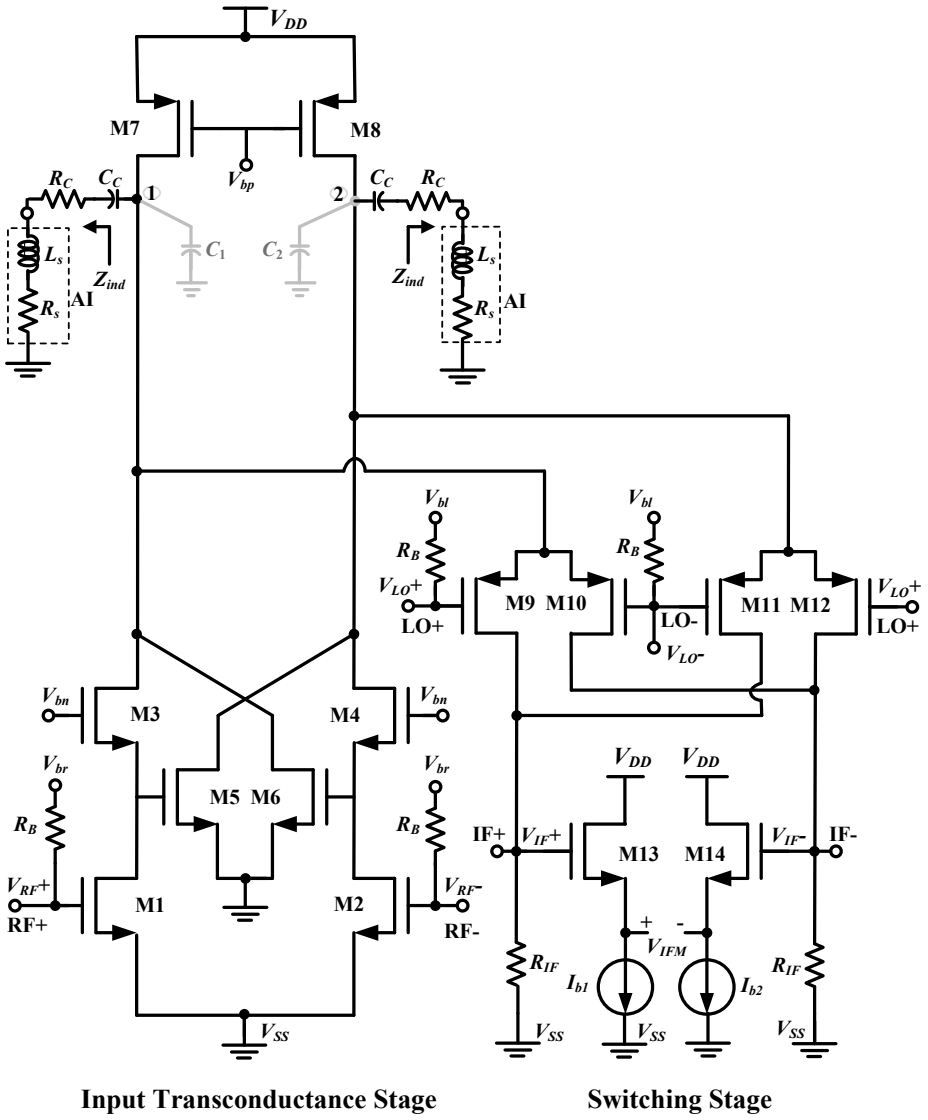


Figure 5.4: Proposed folded-cascode mixer for MB-UWB front-end.

and switching stages followed by a pair of IF buffers (or source-followers). The source-followers are used for measurement purpose only. Like the UWB LNAs as described in Chapter 4, the tunability of active inductors allows for the tuning of the proposed mixer.

The transconductance stage consists of a source-coupled cascoded differ-

ential pair and provides a high gain using large input transistors M1 and M2 (width $W1{=}W2{=}81\mu$m) and current-source loads of PMOS transistors M7 and M8 ($W7{=}W8{=}39\mu$m). Cascode transistors M3 and M4 ($W3{=}W4{=}39\mu$m) provide better isolation between the input and output of the transconductance stage, and improved noise performance. They also provide better isolation between RF and LO signal ports. The cross-coupled pair of transistors M5 and M6 is used for linearity enhancement, and this is similar to the approach of using the MOSFET cascomp configuration in the mixer for linearity improvement [3]. Transistors M5 and M6 subtract RF currents from the main RF paths of the transconductance stage and increase the linearity. The cross-coupled connection of the drains of transistors M5 and M6 compensate for errors in two branches of RF signals, and also increase DC voltage headroom at Nodes 1 and 2 (output nodes).

At the output nodes (Nodes 1 and 2) of the differential transconductance stage, there exist substantial capacitances ($C_1$ and $C_2$) contributed by transistors. Therefore, the frequency response (gain over frequency) of the transconductance stage rolls off fast at high frequencies due to diminishing capacitive impedances of nodal capacitances $C_1$ and $C_2$, and thus, the bandwidth is reduced significantly. Like UWB LNAs as presented in Chapter 4, here in the UWB mixer, the active shunt-peaking technique is exploited by connecting two active inductors (dashed boxes of AI represented by series $L_sR_s$) at node 1 and 2 through $RC$ networks. With increasing frequency, the increasing inductive impedances of active inductors cancel the effects of diminishing capacitive impedances. Thus, the frequency response of the transconductance stage remains flat over a wide bandwidth. Here, the active inductors used in the proposed new mixer are identical to those used for the proposed UWB LNAs as described in Chapter 4. The equivalent $RLC$ model of the active inductor along with series $RC$ network ($R_C$ and $C_C$) connected at Node 1 (or Node 2) of the mixer is shown in Figure 5.5(a) where $L_s$ is the inductance of the active inductor. Neglecting the impedance of coupling capacitor $C_C$ over the frequency of interest, the equivalent $RL$ circuit of Figure 5.5(b) replaces the active inductor and $R_C$ at Node 1 (or Node 2) where $L_{eq}$ and $R_{eq}$ are equal

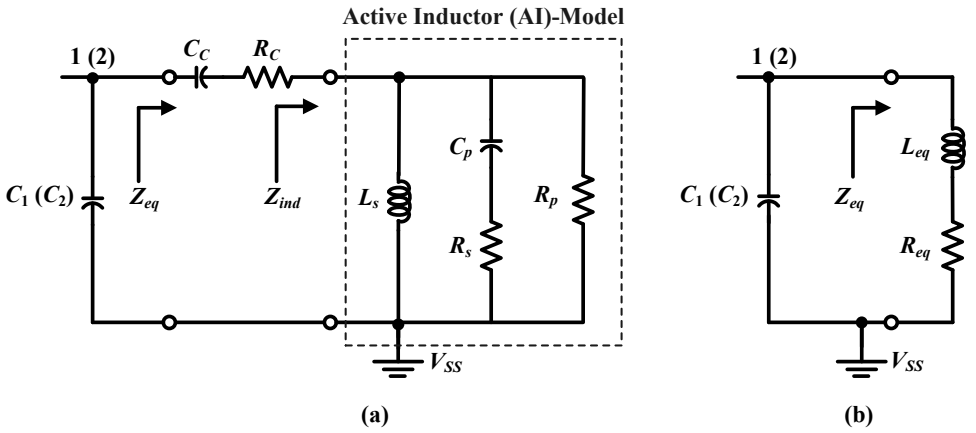


Figure 5.5: (a) Equivalent $RLC$ model of inductive impedance of active inductor in series with $R_C$ and $C_C$, (b) equivalent $RL$ circuit of (a).

to $L_s$ and $R_C$, respectively.

RF input voltages ($V_{RF}+$, $V_{RF}-$) is converted to currents by the source-coupled transistor pair M1 and M2. Then, RF currents at Nodes 1 and 2 from the transconductance stage are folded into the sources of PMOS transistors M9 to M12 of the switching stage. The PMOS switching transistors M9 to M12 are chosen as large (width, $W9$-$W12$=54$\mu$m) to reduce flicker noise [3, 46]. The large amplitude LO signals ($V_{LO}+$, $V_{LO}-$) convert RF currents into IF voltages of ($V_{IF}+$ and $V_{IF}$-) across load resistors ($R_{IF}$) of 400Ω.

### 5.2.2 IF buffer

For the measurement of the mixer with a 50Ω external load, a buffer stage is required at the IF output ($V_{IF}+$ and $V_{IF}-$). The buffer circuit should not load the IF stage, and should have minimum impact on the gain, bandwidth and linearity of the core mixer. Typically a differential common-source amplifier or a source follower is used as the IF buffer. A differential common-source amplifier with 100Ω load resistors can provide 50Ω output impedance to match with 50Ω of the measuring system. However, a large amount of current is required to keep the linearity of the mixer intact. However, a large current requires

large input transistors that boost the gain but decreases the bandwidth of the mixer. Large transistors load the IF output and affect the overall performance of the mixer.

Here in the proposed mixer, two single-ended source followers consisting of transistors M13 and M14 with two identical current-source loads ($I_{b1} = I_{b2}$) take differential IF outputs ($V_{IF}+$ and $V_{IF}-$) from the core mixer (Figure 5.4). A source-follower exhibits a high input impedance and a low output impedance [10]. Therefore. it does not load the IF-stage of the mixer. By increasing current in the source follower, the gain of the IF buffer is kept close to unity, and therefore, the overall gain of the core mixer remains unchanged. Moreover, to keep the linearity of the core mixer unaffected, the transistors of the current-source loads ($I_{b1} = I_{b2}$) are kept in linear mode of operation at the cost of having a slightly increased noise figure.

## 5.3 Proposed Wideband LO driver

### 5.3.1 LO Driver Architecture

To obtain flat conversion gain for UWB mixers, along with even amplitudes of RF signals, the amplitudes of LO signals should also be even over the desired UWB bandwidth. Note that LO signals are amplified for increased driving capability to switch transistors M9-M12 perfectly for increased conversion gain and better linearity [46]. The perfect switching of transistors M9-M12 requires LO signals alike rectangular waves [46]. Typically, LO signals generated from oscillators are sinusoidal and weak, and have poor switching capability. Therefore, LO signals from oscillators are amplified by drive amplifiers before feeding to mixers. The level of sinusoidal LO signals is elevated to the saturation level of drive amplifiers that provides signals alike rectangular waves.

Typically, LO drivers are a two-stage or three-stage amplifiers where each amplifying stage introduces pole at its output due to output node capacitance. The multiple poles in a multistage driving amplifier causes the frequency response rolling off fast at high high frequencies and reduces the bandwidth of the LO driver significantly. Thus, a wide variation in the gain of the driver

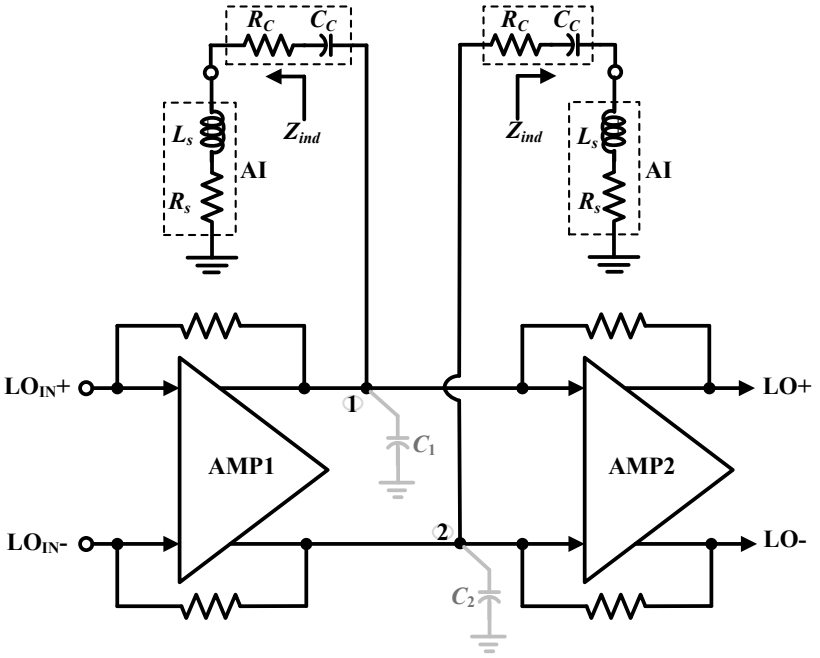


Figure 5.6: Proposed architecture of LO driver.

occurs over the desired bandwidth; and consequently, conversion gain of the mixer also varies widely. Figure 5.6 shows the architecture of the proposed LO driver, which is a two-stage differential amplifer. Like passive inductorless UWB LNA and mixer using active inductors, here, in the proposed LO driver, two active inductors (AIs) are connected to the output nodes (Nodes 1 and 2) in between amplifying stages (AMP1 and AMP2) to cancel the effects of diminishing capactive impedances of node capacitances $C_1$ and $C_2$ at high frequency in increasing bandwidth.

### 5.3.2 LO Driver Circuit Description

Figure 5.7 shows the schematic of the proposed two-stage wideband LO driver. which is a cascading of two shunt-feedback differential amplifiers. Like the new two-stage UWB LNA in Chapter 4, the broadband input matching is achieved using the combined transconductances of transistors M1 (or M2) and M3 (or M4) at the cost of a large amount of current because the input impedance of

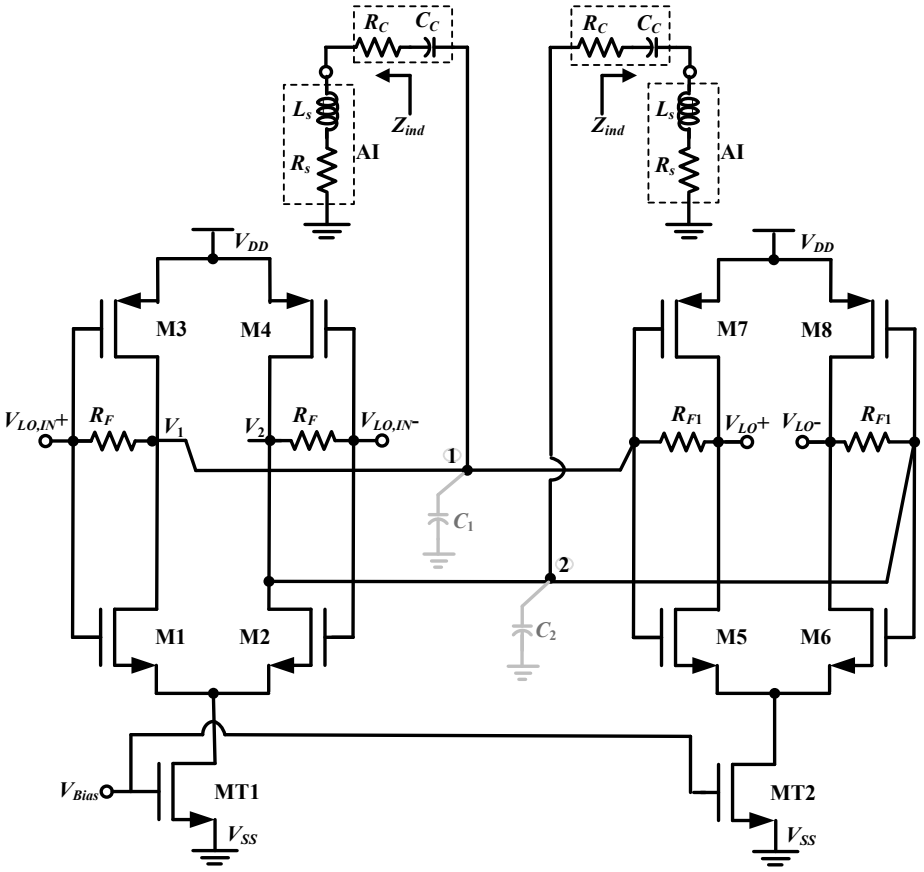


Figure 5.7: Proposed two-stage wideband LO driver circuit.

the LO driver depends on transconductances of transistors. Here two active inductors are connected at the output nodes (Nodes 1 and 2) of the first-stage shunt-feedback amplifier through $RC$ ($R_C$, $C_C$) networks to cancel the effects of diminishing capactive impedances of node capacitances ($C_1$ and $C_2$) and keep the frequency response (gain over frequency) of the LO driver flat to increase the bandwidth. The active inductors along with $R_C$ and $C_C$ at Nodes 1 and 2 are replaced with the equivalent $RL$ circuit of Figure 5.5(b), which models the equivalent inductive impedance ($Z_{eq}$) of the active inductor along with resistor $R_C$. The differential sinusoidal LO signals ($V_{LO,IN}$+ and

$V_{LO,IN}-$) are fed to the differential input of the driver. The broadband input matching (50Ω) for the LO driver is important, and the first-stage transresistance amplifier (transistors M1 to M4 and MT1) requires a large current (6.0mA) to achieve required transconductances of M1 (or M2) and M3 (or M4) for input matching. The second-stage transresistance amplifier (transistors M5 to M8 and MT2) draws a significant amount of current (9.0mA) to drive the gates of the switching transistors of the mixer. A transimpedance (or transresistance) amplifier takes current as the input and provides voltage as the output. Neglecting the loading effect of the $Z_{ind}$ of the active inductor, the transimpedance transfer function derived using the half-circuit of the first-stage differential can be expressed as

$$Z_{im} = \frac{s(C_{gd1,2} + C_{gd3,4}) - (g_{m1,2} + g_{m3,4} - \frac{1}{R_F})}{D_{im}}. \tag{5.2}$$

$D_{im}$ is expressed as

$$D_{im} = s^2 C_{1,2}(C_{gd1} + C_{gd2}) + s[\frac{C_{1,2}}{R_F} + (g_{m1,2} + g_{m3,4})(C_{gd1,2} + Cg_{d3,4})] + \frac{(g_{m1,2} + g_{m3,4})}{R_F}, \tag{5.3}$$

where $C_{gd}$ and $g_m$, with subscripts 1,2, 3 and 4 represent gate-drain capacitances and transconductances of transistors M1 (or M2) and M3 (or M4), respectively. At low frequencies, the transimpedance, $Z_{im}(0)$ (or transresistance, $R_{im}$) is

$$R_{im} = Z_{im}(0) = -\frac{R_F(g_{m1,2} + g_{m3,4}) - 1}{(g_{m1,2} + g_{m3,4})} \approx -R_F. \tag{5.4}$$

Here, the design goal is to reduce $R_F$ to increase current for enhanced driving capability of the driver. In the first-stage amplifier, the feedback resistor $R_F$ is chosen larger (200Ω) but in the second-stage, the feedback resistor $R_{F1}$ is chosen smaller (100Ω).

## 5.4 Design of UWB RF Front-End

### 5.4.1 RF Front-End Basics

The front-end is a cascaded connection of the LNA and mixer. In a direct-conversion front-end, the LNA is directly coupled to the mixer and therefore, it does not need to drive a 50Ω load. This allows for making the LNA design simpler because no 50Ω output impedance matching is required. The relaxed requirement of the output impedance matching eliminates the necessity of the inter-stage impedance matching circuit between the LNA and mixer. The important performance parameters of the front-end are gain, noise figure, 1-dB compression point ($CP$) (linearity measurement for gain compression), and $IIP3$ (linearity measurement for intermodulation terms). Because the front-end is a cascaded system, the overall performance parameters depend on the performance parameters of the LNA and mixer. The overall gain of the front-end (FE) is the summation of the gain ($G$) of the LNA and mixer as

$$G_{FE}(dB) = G_{LNA}(dB) + G_{Mixer}(dB) \tag{5.5}$$

The noise factor ($F$) and $IIP3$ of a cascaded system are described in Chapter 4. Here, for the front-end, the $F$ is expressed as

$$F_{FE} = F_{LNA} + \frac{F_{Mixer} - 1}{G_{LNA}}, \tag{5.6}$$

where $F_{LNA}$ and $G_{LNA}$ are noise factor and gain of the LNA, respectively, and $F_{Mixer}$ is the noise factor of the mixer. Note that the noise factor of the LNA is directly added to the noise factor of the front-end, and the noise factor of the mixer is divided by the gain of the LNA. Therefore, to reduce the overall noise factor of the front-end, the LNA should be designed with minimum noise factor and maximum gain. The overall $IIP3$ of the front-end is expressed as [10]

$$\frac{1}{V_{IP3,FE}^2} \approx \frac{1}{V_{IP3,LNA}^2} + \frac{\alpha_1^2}{V_{IP3,Mixer}^2}, \tag{5.7}$$

where $V_{IIP3}$ with subscripts (FE, LNA and Mixer) is the input signal amplitude (of the front-end, LNA, and mixer) at which amplitude of the fundamental terms equal intermodulation terms. Unlike the noise factor, the overall $IIP3$ of the front-end is limited by the $IIP3$ of the mixer.

### 5.4.2 CMOS UWB Front-End

For MB-UWB applications, RF front-ends operate over a band-group or a number of band-groups within 3.1-10.6 GHz frequency range. Note that in the MB-UWB systems, the 7.5GHz UWB spectrum is divided into fourteen bands of 528 MHz each, and these bands are grouped into five distinct band-groups. Along with a high level of device integration, a UWB front-end needs to be designed and implemented in standard digital CMOS processes to be compatible with the rest of the receiver system, which is usually integrated in inexpensive digital CMOS processes. Note that a high level of device integration leads to a low chip area, and inexpensive standard digital CMOS processes reduce cost of the overall front-end. However, the extensive use of area-inefficient on-chip passive inductors in conventional UWB front-ends leads to the use of a costly large chip area.

CMOS UWB front-ends using on-chip passive inductors occupy large chip areas [52, 53]. A 3.1-8.0 GHz UWB RF front-end where the LNA uses a number passive inductors, which are realized using off-chip bondwires [54]. Although, the active part of this front-end is inductorless, and occupies only $0.35\text{mm}^2$, this approach does not provide a fully-integrated solution. Moreover, the conversion gains of these front-ends are not flat over the desired UWB bandwidth. Here, a new passive inductorless UWB front-end that uses an area-efficient UWB LNA and a UWB mixer using ultra compact tunable active inductors, and provides a flat conversion gain, is proposed. The tunability of active inductors allows for tuning the gain and bandwidth of the proposed active CMOS (passive inductorless) UWB front-end.

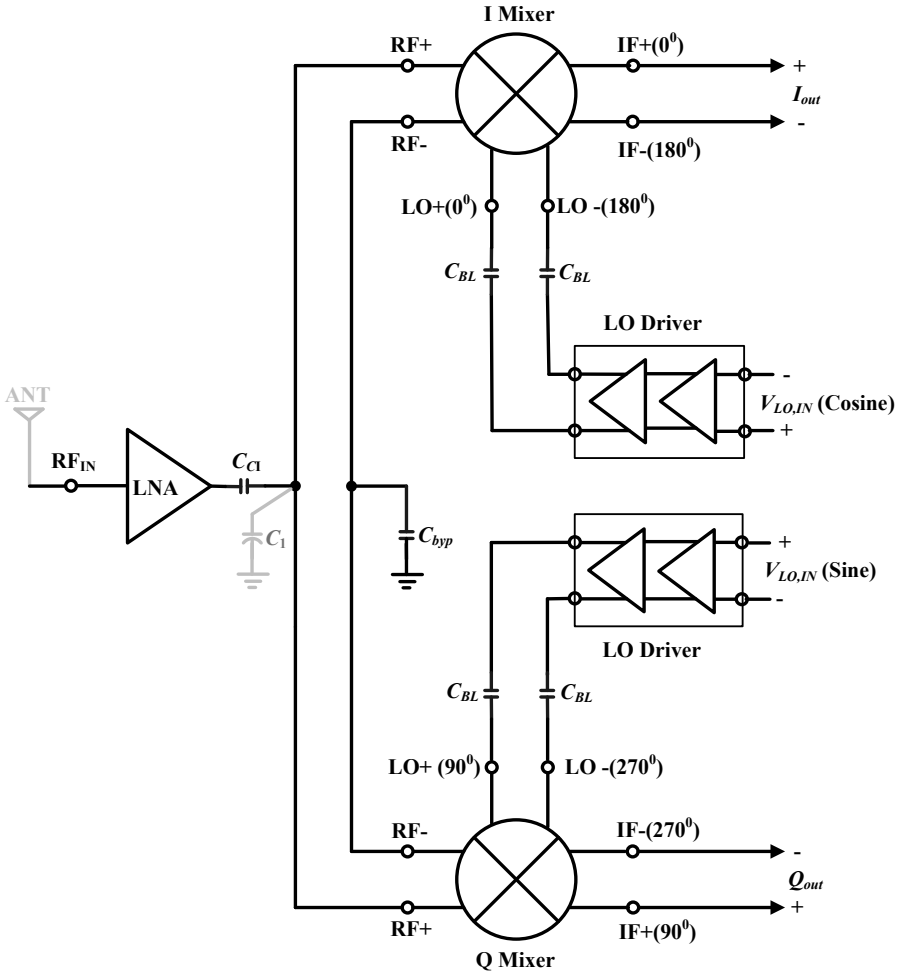


Figure 5.8: Proposed MB-UWB front-end architecture.

## 5.5 Proposed Active CMOS MB-UWB Front-End

Figure 5.8 shows the architecture of the proposed active CMOS UWB receiver front-end where the LNA is directly coupled to a pair of mixers (I and Q mixers) through a coupling-capacitor, $C_{C1}$ (=2.5pF). RF signals from the single-ended UWB LNA are fed to one port (RF+) of each of the UWB mixers. The other port (RF-) of each of the mixers is grounded through a common bypass capacitor, $C_{byp}$ (=2.5pF). Thus, single-ended RF signals from the LNA

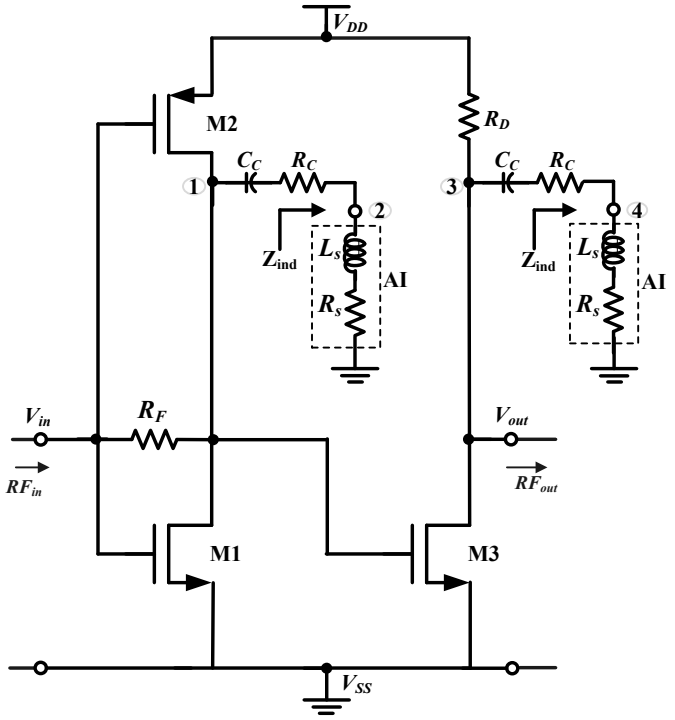


Figure 5.9: Two-stage LNA used in UWB front-end.

are applied to the mixer as the differential signals. Differential quadrature ($90^0$ out of phases) LO signals, $V_{LO,IN}$ ($0^0$) and $V_{LO,IN}$ ($90^0$) are fed to the LO ports (LO+ and LO-) of the mixers through LO drivers followed by DC blocking capacitors $C_{BL}$ (=2.0pF). Thus, differential zero-IF or baseband signals, $I$ and $Q$ ($90^0$ out of phases) are obtained at the IF ports (IF+ and IF-). Mixers are used in a quadrature configuration to obtain quadrature IF signals by applying quadrature LO signals.

For the proposed UWB front-end, a two-stage area-efficient UWB LNA using tunable active inductors is shown in Figure 5.9. The design of this active (passive-inductorless) CMOS LNA is described in Chapter 4. Here, the proposed UWB LNA uses active inductors at the outputs of amplifying stages. The output of the LNA is directly coupled to the transconductance or gain stages of two mixers (I and Q mixers) through a coupling capacitor $C_{C1}$. The input transistors M1 and M2 of the UWB mixer (Figure 5.4) for the

proposed front-end have large gate-source capacitances ($C_{gs1,2}$), which reduce the bandwidth due to diminishing capacitive impedances at high frequencies. Here, the second active inductor connected at the output node of the LNA (Figure 5.9) cancels the effects of total nodal capacitances of input transistors (M1 and M2) of the transconductance stages of quadrature I and Q mixers. As described in Chapter 4, the bandwidth of the UWB LNA (Figure 5.9) using two active inductors is increased at the cost of reduced gain while having a minimum impact on noise figure. The circuit of LO drivers for the proposed front-end is also previously shown in Figure 5.7.

### 5.5.1 Design Realization and Simulation

The proposed front-end is designed and implemented in TSMC 90nm digital CMOS process. For the two-stage UWB LNA of the front-end (Figure 5.9), widths ($W$) of transistor M1 (and M2) is chosen as 60$\mu$m to achieve a combined transconductance of 20.0mS(mA/V) that provides 50$\Omega$ input matching over the desired bandwidth. Transistor M3 with $W$ of 64$\mu$m provides high transconductance (80mS) to boost the overall gain of the UWB LNA. Feedback resistor $R_F$, coupling resistor $R_C$ and load resistor $R_L$ are chosen as 180$\Omega$, 170$\Omega$ and 112$\Omega$, respectively. The coupling capacitor $C_C$ is 1.2pF, and the transistors of the active inductors of the LNA have widths in the range of 1$\mu$m-7.5$\mu$m while all of them have the length of 100nm. The simulation and measurement results of the two-stage UWB LNA are presented in Chapter 4.

Mixers and front-ends are characterized using similar parameters of conversion gain ($CG$), noise figure ($NF$), 1-dB $CP$ and $IIP3$. In the wideband LO driver (Figure 5.7), the first-stage transresistance amplifier provides input matching with moderate gain. The second-stage amplifier boosts the gain and provide 50$\Omega$ output impedance. The widths of transistors M1 to M4 and M5 to M8 are chosen as 30$\mu$m and 60$\mu$m, respectively. Feedback resistor $R_F$ and $R_{F1}$ are chosen as 200$\Omega$ and 100$\Omega$, respectively.

Figure 5.10 shows the simulated frequency response (gain as a function of frequency) of the LO driver with active inductor (W-AI) and without active inductor (WO-AI) for control voltage $V_{tune}$ of 600mV. With active inductors,

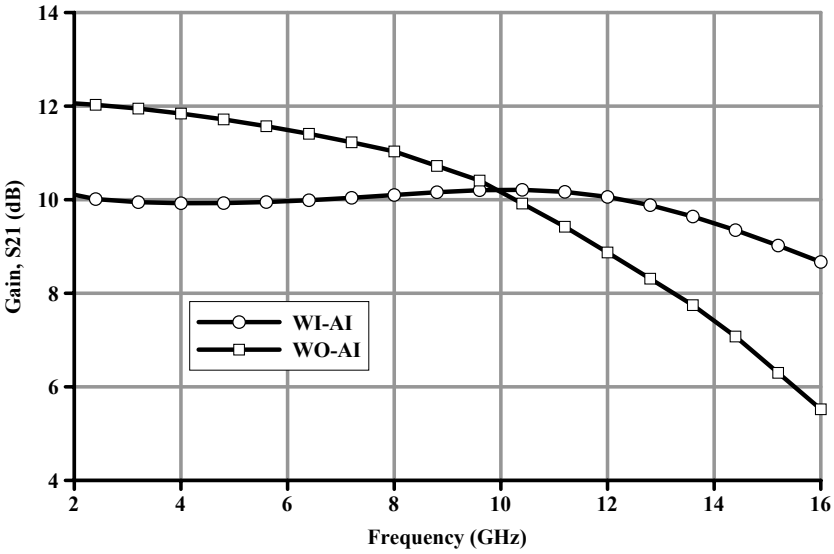


Figure 5.10: Simulated frequency responses of LO driver.

the LO driver exhibits a flat gain of 10.0dB over 2.0-12.0 GHz (plot of W-AI). On the other hand, without active inductors, the gain of the LO driver rolls off sharply at high frequencies (above 8.0GHz), and gain drops from 12.0dB to 8.7dB over 2.0-12.0 GHz band (plot of WO-AI). Note that at high frequencies, the diminishing capacitive impedances of node capacitances cause the reduction of high-frequency gain, and in turn, cause the reduction of bandwidth. With active inductors, the gain of the LO driver drops by 1.8dB (from 12.0-10.2dB) at lower frequencies (below 8.0GHz) because of the signal losses through the low impedances of active inductors. On the other hand, at high frequencies, the increasing inductive impedances of the active inductors compensate for the losses caused by the diminishing capacitive impedances and keep gain flat for the extended bandwidth.

The performance of RF circuits depend significantly on physical layouts. All large transistors are realized using multi-fingered gate transistors with a maximum width ($W$) of 1.5$\mu$m per finger. This reduces gate resistances of large transistors. Resistors are realized using poly-silicon resistors with maximum ratio of the length to the width of 5. The widths of resistors are chosen

greater than 2.0$\mu$m that results in less variations of resistances due to process and temperature variations. For a large amount of current to be carried out by resistors, a number of parallel devices are used. Coupling capacitor ($C_{C1}$) and blocking capacitors ($C_{BL}$) are implemented using area-efficient MIM capacitors with a unit value of 2fF/$\mu$m$^2$. Bypass capacitor ($C_{byp}$) is realized with interdigitated multilevel metal structures. This gives a higher unit capacitance of 2.2fF/$\mu$m$^2$. The use of interdigitated capacitors also fulfills the metal density requirement across the full chip of the front-end.

## 5.6 Implementation and Measurement of UWB Front-End

The proposed MB-UWB front-end that includes all the circuits and components of Figure 5.8 is implemented in a nine-metal TSMC 90nm CMOS digital CMOS process. The die photo of the fabricated front-end is shown in Figure 5.11. The complete front-end (excluding bonding pads and IF buffer) occupies a chip area of 0.261mm$^2$ (450$\mu$m $\times$ 580$\mu$m), and the overall front-end (including bonding pads) occupies an area of 0.66mm$^2$ (750$\mu$m $\times$ 880$\mu$m). The core front-end (LNA and quadrature I and Q mixers) occupies only 0.148mm$^2$ (450$\mu$m $\times$ 330$\mu$m) as shown in the dashed box of Figure 5.12.

The front-end is measured on-wafer for gain, gain-bandwidth tuning, input return loss ($S_{11}$), noise figure ($NF$), 1-dB $CP$ and $IIP3$. Figure 5.13 shows the measurement setup for the $CG$ of the front-end. The single-ended RF signal is applied through a GSG (ground-signal-ground) probe. The LO signal is converted to differential signals using a 0-180$^0$ hybrid and is applied through a GSSG probe. The differential IF signals are converted to a single-ended one (by using external hybrid coupler), which is measured using the spectrum analyzer. The front-end is measured for a fixed IF frequency of 500MHz over the RF frequency range of 2.5-11.0 GHz. Thus, RF and LO frequencies are chosen accordingly to obtain the 500MHz downconverted IF frequency ($\omega_{IF}$=$\omega_{RF}$-$\omega_{LO}$). Active inductors for LO drivers are biased with a fixed control voltage, $V_{tune}$ of 600mV. Operated with a 1.2V and using control voltages $V_{tune}$ of

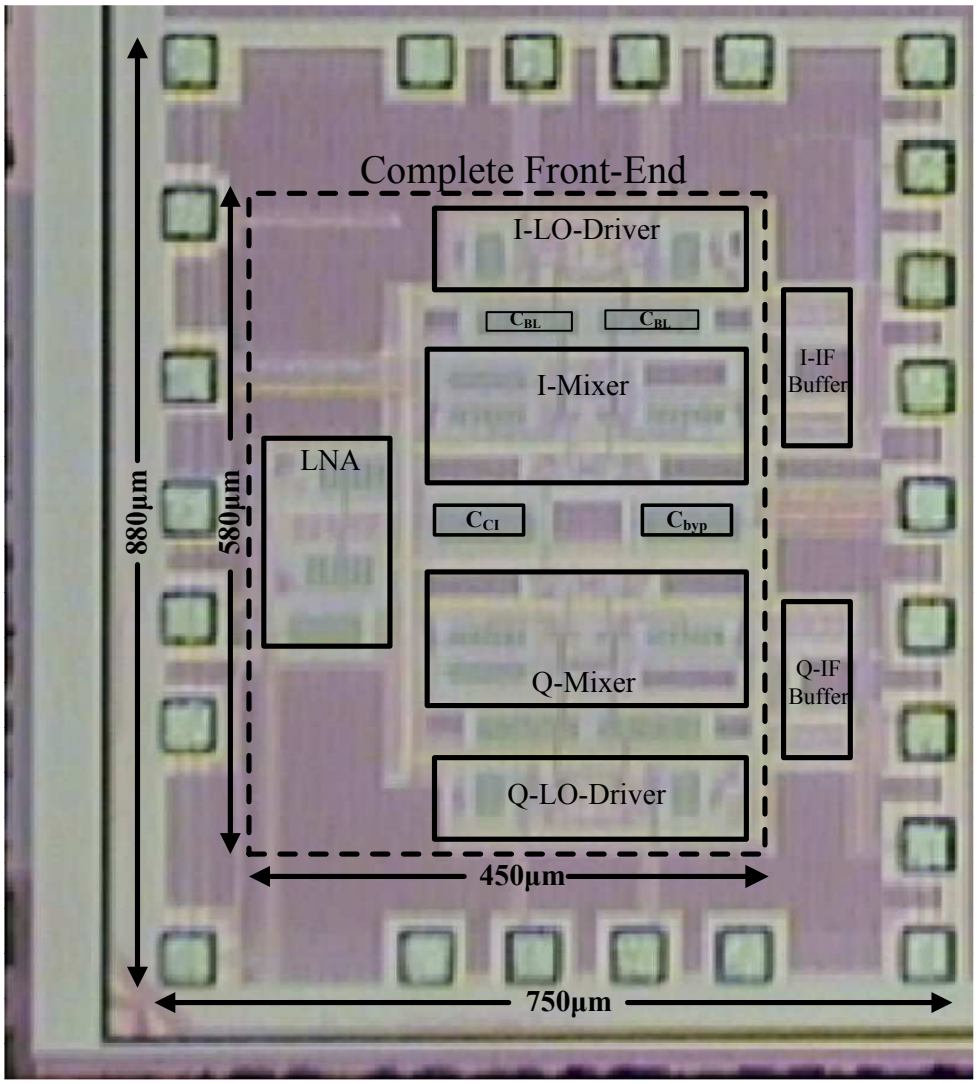


Figure 5.11: Microphotograph of fabricated front-end.

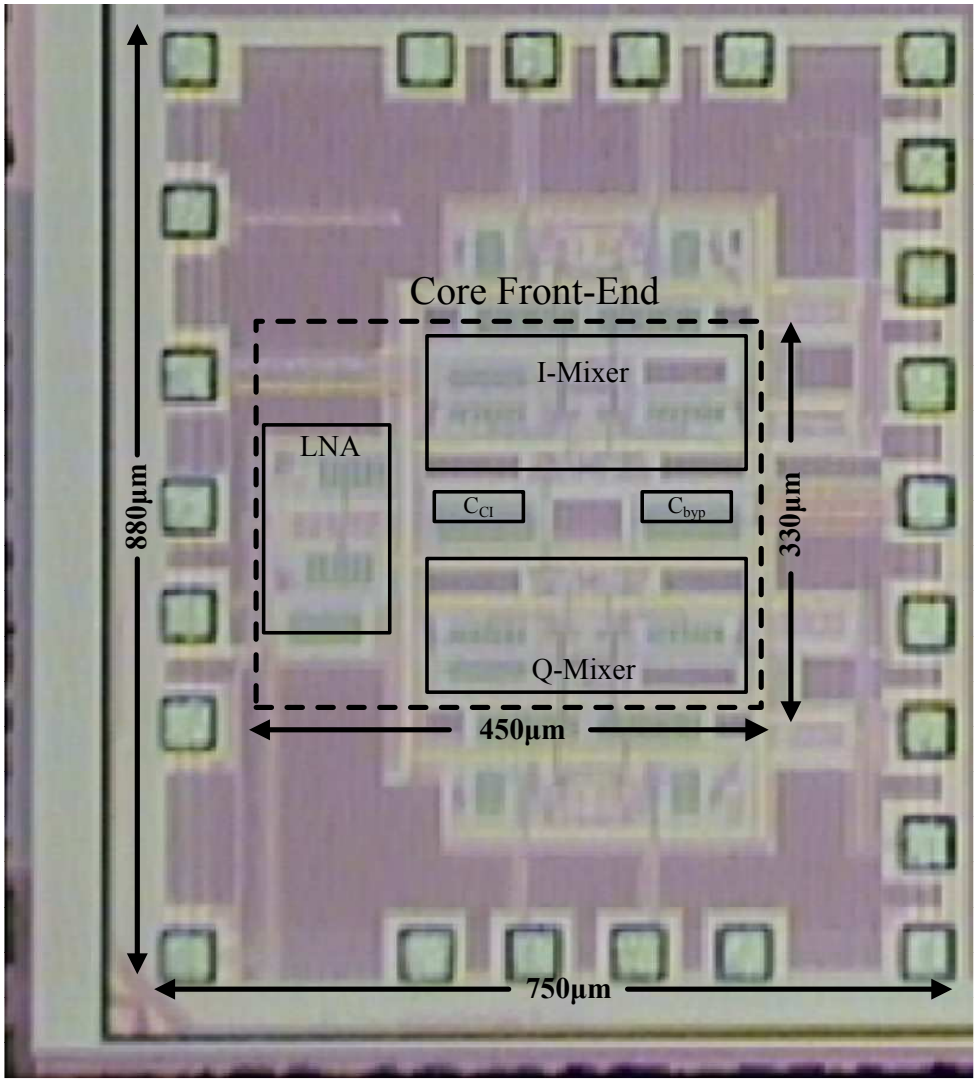


Figure 5.12: Microphotograph showing fabricated front-end core.

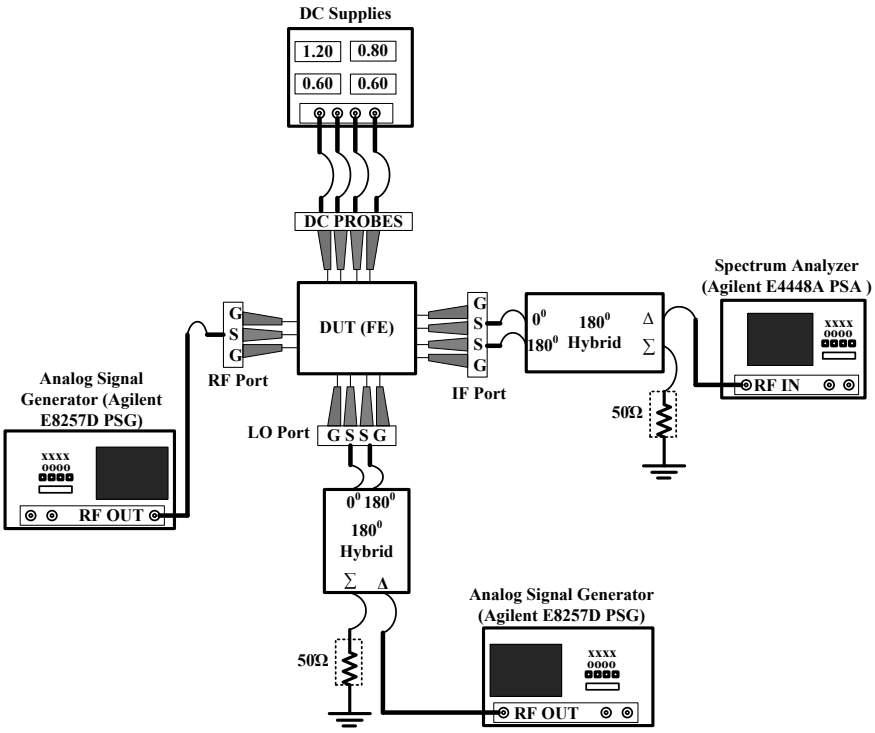


Figure 5.13: Measurement setup for front-end gain.

650mV for the LNA and mixers, the fabricated front-end draws a total current of 74.8mA. In simulation, the front-draws a current of 76.2mA at 1.2V supply with $V_{tune}$ of 650mV. The core front-end (the LNA, and I and Q mixers) draws a current of 30.2mA but the LNA and one mixer (I or Q) mixer draw 22.1mA.

Figure 5.14 shows the measured and simulated gains of the proposed UWB receiver front-end over input RF frequency with a $V_{tune}$ of 650mV for controlling the active inductors of the LNA and mixers. The measured gain varies from 22.6dB (at 2.5GHz) to 21.8dB (at 8.9GHz) exhibiting only 0.8dB variation of gain over 6.4GHz UWB spectrum. On the other hand, the simulated gain varies from 23.8dB (2.5GHz) to 23.2dB (at 9.3GHz). Note that the measured gain and bandwidth are reduced by 1.3dB and 400 MHz, respectively, compared to the simulated ones. Figure 5.15 shows the measured gain of the front-end along with the simulated gain over output IF frequency of DC-500MHz where the LO frequency is selected in the range of 3.4-3.9 GHz. The

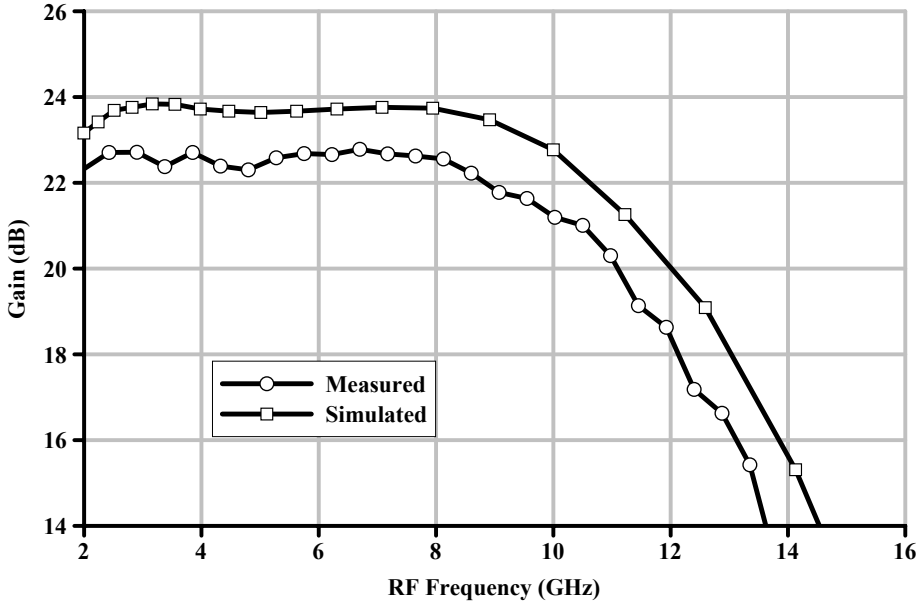


Figure 5.14: Measured and simulated gain of UWB front-end.

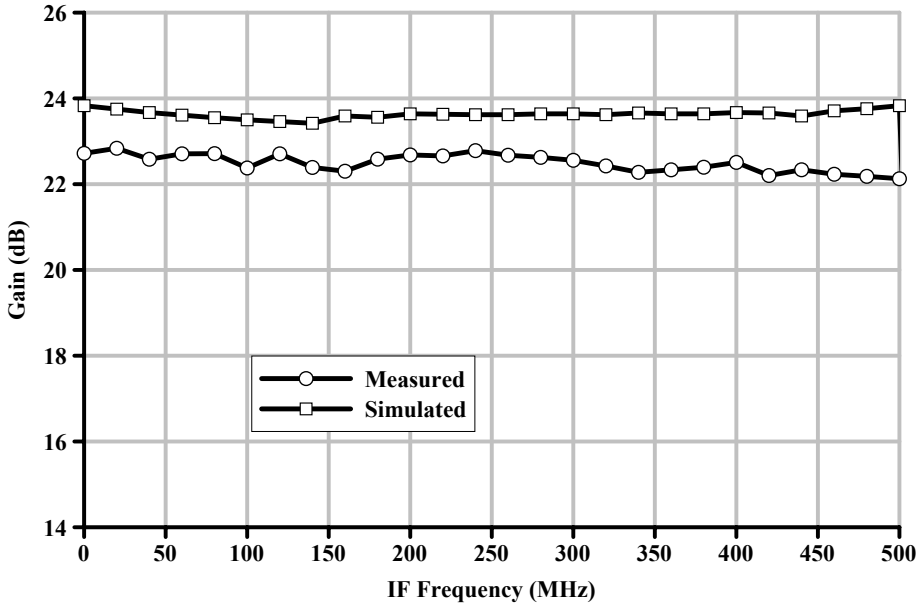


Figure 5.15: Measured and simulated gain of UWB front-end.

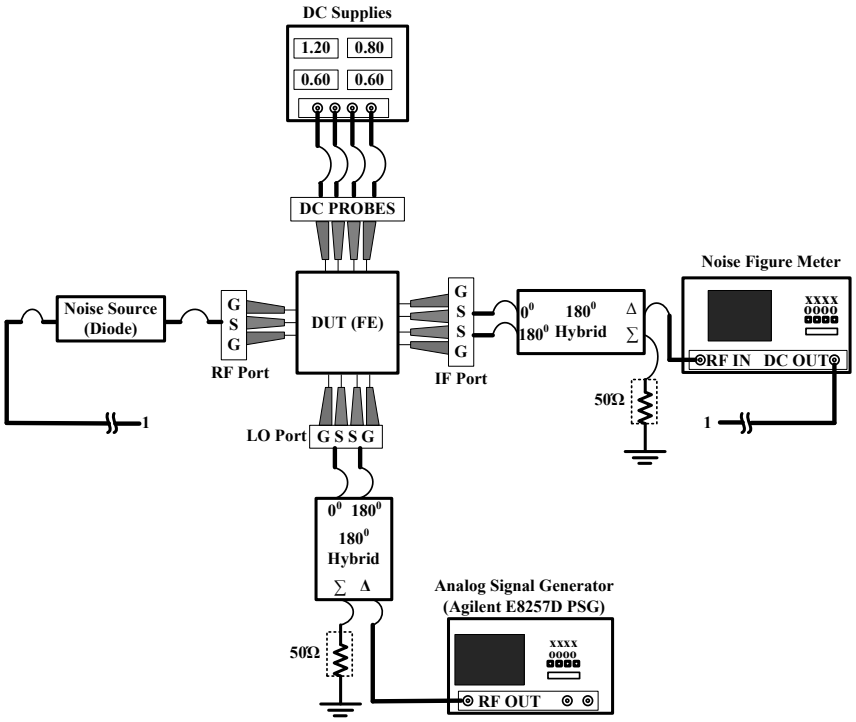


Figure 5.16: Measurement setup for front-end noise figure.

measured results differ from the simulated ones due to the lack of accurate RF modeling of digital transistors used in simulation, and there is a also possibility of errors in measurement. Moreover, in measurement, the front-end draws less current than it does in simulation due to the resistances of interconnects and the contact resistances between pads and probe tips. This also causes the reduction of the measured gain and bandwidth of the fabricated front-end.

Figure 5.16 shows the measurement setup for the *NF* of the UWB front-end where a noise signal is applied to the input RF port and the *NF* is measured at the IF port using a noise-figure meter. Figure 5.17 shows the measured and simulated *NF* of the fabricated front-end. The measured double-sideband (DSB) *NF* is 5.4-7.2 dB over 2.5-11.0 GHz whereas the simulated DSB *NF* is 4.3-4.7 dB. The measured *NF* differs by 1.2 to 2.5dB from the simulated *NF*. This is because of the lack of an accurate noise model for digital transistors

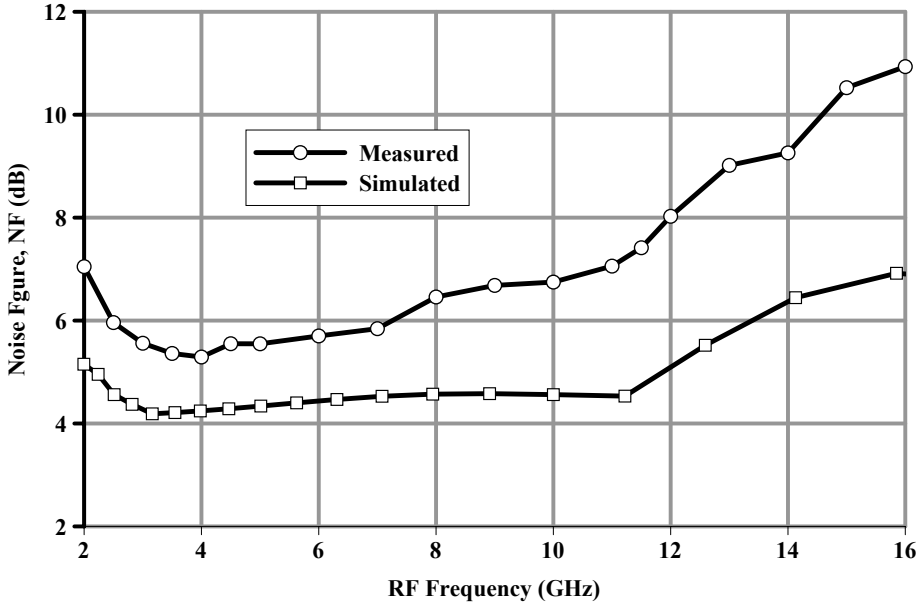


Figure 5.17: Measured and simulated noise figure of UWB front-end.

used in simulation. The noisy measurement environment also contribute to the increased *NF*. To measure input return loss $S_{11}$, the IF port is terminated with a 50Ω load, and the VNA is connected at the input RF port of Figure 5.13. Figure 5.18 shows the measured and simulated $S_{11}$ of the front-end, and the measured $S_{11}$ remains below -14.0dB over 2.5-11.0 GHz indicating the broadband input matching. The causes of discrepancies between measured and simulated $S_{11}$ are already described for the UWB LNAs in Chapter 4

Figure 5.19 shows the tuning of the gain-bandwidth of the front-end for a $V_{tune}$ of 550mV, 650mV and 750mV. For a $V_{tune}$ of 750mV, the gain variation is limited within 0.9dB (24.2-23.3 dB) over 2.5-7.8 GHZ bandwidth. On the other hand, for a $V_{tune}$ of 550mV, the measured gain is obtained 20.7-20.1 dB over 2.5-9.5 GHz exhibiting only 0.6dB variation of gain over the bandwidth of 7.0GHz. With a high $V_{tune}$, the inductance of active inductors increases but their inductive operating range decreases. Therefore, the active inductors cannot cancel the effects of nodal capacitances at high frequencies, and the frequency response of the front-end falls of sharply resulting into a reduced

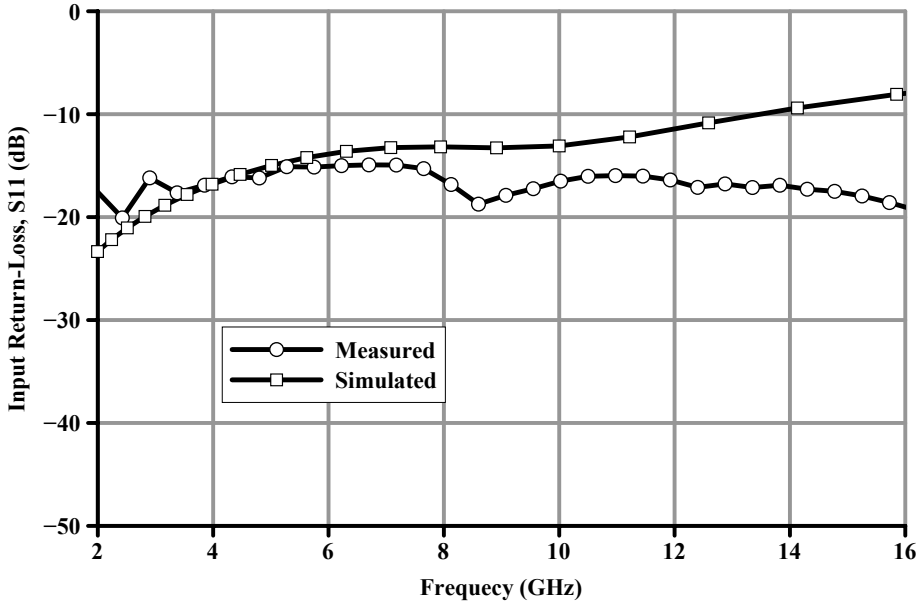


Figure 5.18: Measured and simulated input return-losses of UWB front-end.

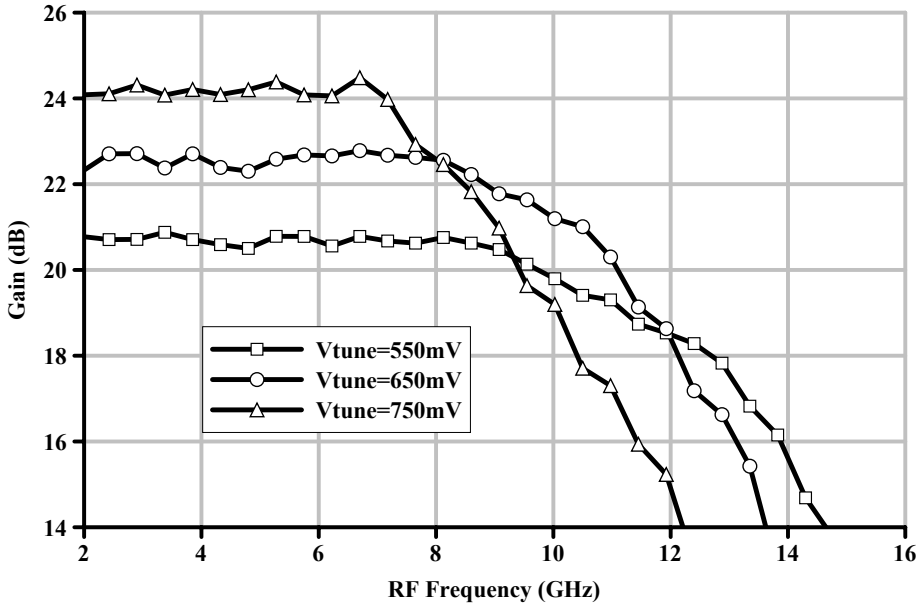


Figure 5.19: Tuning of measured gain-bandwidth of UWB front-end.

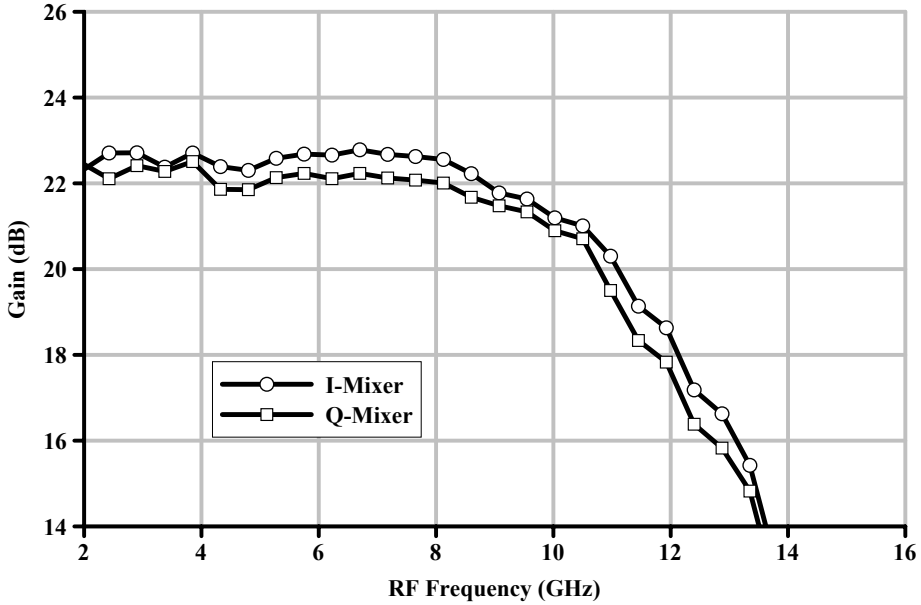


Figure 5.20: Measured gain of UWB front-end with I and Q mixers.

bandwidth. With a low $V_{tune}$, the inductance of active inductors decreases but their inductive operating range extends to an increased frequency. The reduced inductances of active inductors increase losses and reduce the gain of the front-end. However, the increased inductive operating range cancel the effects of nodal capacitances at high frequencies, and keep gain flat over an extended bandwidth. Figure 5.20 shows the measured gain of the front-end for I and Q mixers. Note that there is a 0.4-0.6 dB variation of gain between I and Q mixers, and there is also a slight variation in bandwidth. This gain-bandwidth mismatches can be adjusted by controlling active inductors of I and Q mixers separately with $V_{tune}$.

The measurement setup to measure 1-dB *CP* of the front-end is similar to that of the gain measurement setup, where the IF signal power is measured using a spectrum analyzer while varying the input RF power. Figure 5.21 shows the measured 1-dB *CP* of -18.1dBm, which is the input RF power where the gain of the front-end drops by 1-dB from the expected linear gain.

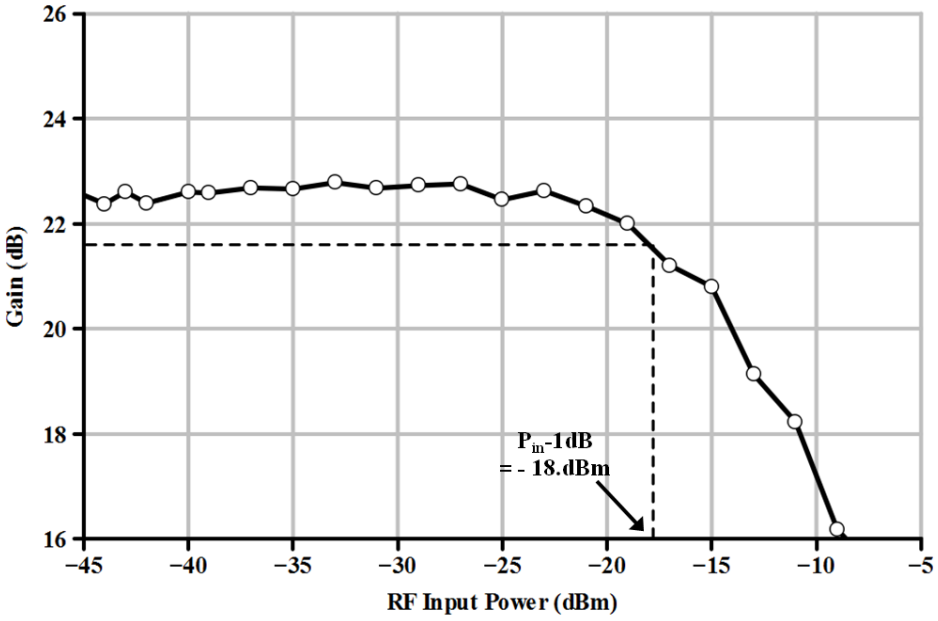


Figure 5.21: Measured 1-dB *CP* of UWB front-end.

The measurement setup for measuring the *IIP*3 of the front is shown in Figure 5.22. Two RF tones at 1.0MHz apart (5.0GHz and 5.001GHz) are applied through a power combiner to the RF port of the front-end. The front-end exhibits measured *IIP*3 of -8.3dBm as shown in Figure 5.23.

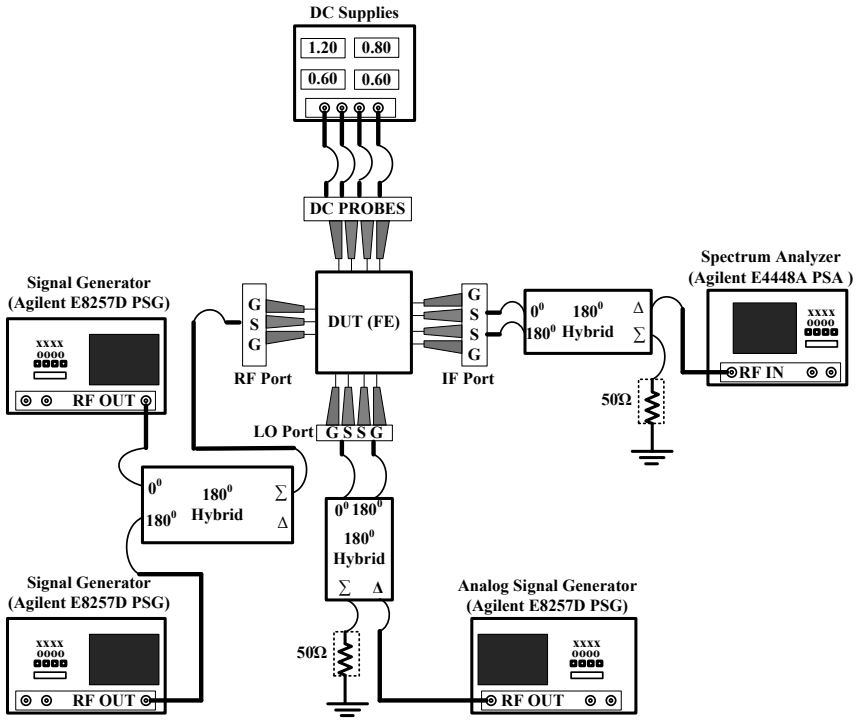


Figure 5.22: Measurement setup for front-end *IIP*3.

The performances of the fabricated UWB front-end are summarized in Table 5.1, and are compared with those of the recently published UWB front-ends in the literature. The front-ends in [55, 56] exhibit higher gain. These front-end occupy large areas as they use passive inductors. Although the front-end in [56] consumes lower power, its bandwidth is only 3.24-4.75 GHz. The front-end in [57] occupies a small chip area (0.2mm$^2$) excluding the area of an on-chip balun transformer used for input matching. Hence, the area of this front-end is much higher than the core area of our proposed UWB front-end (0.1485mm$^2$). In [54], off-chip bond-wires are the integral parts of the front-end. Although using active inductors, the proposed front-end in this thesis exhibits relatively a low NF over the desired bandwidth (2.5-8.9 GHz) because active inductors are connected at the outputs of the amplifying stages in the RF signal paths and they are physically apart from the input of front-end.

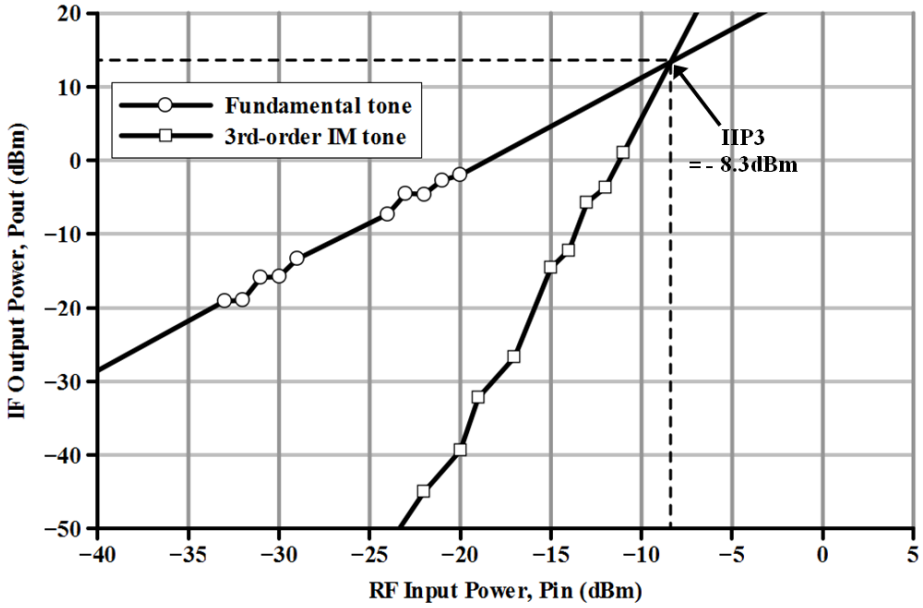


Figure 5.23: Measured input $IP3$ ($IIP3$) of UWB front-end.

The complete area (0.261mm$^2$) of our proposed front-end (in this thesis) is smaller than any of the LNAs of the front-ends in the Table.

Table 5.1: Performance summary and comparison of UWB Front-ends.

| [REF.] | [55] | [54] | [58] | [56] | [57] | [This work] |
|---|---|---|---|---|---|---|
| Tech. [CMOS] | 0.18$\mu$m | 0.18$\mu$m | 0.13$\mu$m | 90nm | 45nm | 90nm |
| $BW$ [GHz] | 3.1-8.0 | 3.1-8.0 | 3.1-10.6 | 3.25-4.75 | 0.6-10.0 | 2.5-8.9 |
| $Gain$ [dB] | 29.0 | 21.0 | 23.3 | 29.5 | 14.0 | 22.6 |
| $NF$ [dB] | 6.5-8.1 | 5.0-6.5 | 5.2-9.1 | <5.2 | 6.0-7.8 | 5.4-6.6 |
| $S_{11}$ [dB] | <-13.0 | <-10.0 | <-5.0 | <-10.0 | <-10.0 | <-14.5 |
| 1-dB $CP$ [dBm] | -21.8 | -22.7 | -22.7 | -26.0 | n/a | -18.1 |
| $IIP3$ [dBm] | -11.1 | -5.6 | -10.4 | n/a | 0.0 | -8.3 |
| Tunability | No | No | No | No | No | Yes |
| $P_{Diss}$ [mW] | 33.8 | 44.85 | 42.0 | 9.6 | 30.0 | 36.0 |
| Core Area [mm$^2$] | >2.0 | 0.35 | 0.9 | >1.0 | 0.20 | 0.1485 |

# Chapter 6

# Conclusion and Future Research

## 6.1 Conclusion

In this thesis, we presented a new active CMOS design for a UWB receiver front-end that uses area-efficient transistor-only active inductors instead of bulk area-inefficient passive inductors. Although passive inductors are essential components for the design of RF circuits, this work showed the possibility of design and implementation of active (passive inductorless) CMOS RFICs; LNA, mixer and LO driver for UWB front-ends. The use of active inductors led the UWB RFICs to occupy a small fraction of the area of conventional RFICs. Moreover, the tunability of active inductors allowed for tuning the UWB RFICs, and in turn, tuning the performance of the UWB front-end with varying gain and bandwidth. For UWB applications, the tunability of the front-end can be widely exploited to obtain the desired gain and bandwidth over a band or band groups of MB-UWB systems. Although active inductors are noisy, this work exhibited that using them at the outputs can minimize their noise contributions to the core RFICs. Overall, passive inductorless designs can lead to integrate RF, analog and digital circuits of transceivers on a low-cost small die area while using inexpensive digital CMOS processes.

In developing area-efficient RFICs for the UWB front-end, first of all, we proposed and designed two new configurations of CMOS tunable active inductors for $Q$ enhancement and bandwidth extension. In the $Q$-enhanced active inductor, simultaneous positive and negative feedbacks were created to

reduce series and parallel losses in the inductor to enhance the quality factor ($Q$). The proposed $Q$-enhanced active inductor exhibited an inductance of 15.0nH to 20.0nH (at DC), a $Q$ in excess of 200.0, and an inductive impedance range over 12.0GHz. To extend the inductive operating range, we proposed a bandwidth-extended active inductor employing double negative feedbacks. One negative feedback mainly contributed to the development of inductance, and the other negative feedback increased the inductive operating bandwidth by cancelling non-dominant poles in the RF signal path. The bandwidth-extended active inductor exhibited inductive operating bandwidth from a few hundred MHz to over 22.0GHz. The wide inductive-operating range of the active inductors made them suitable for UWB applications and beyond. The active inductors occupied a chip area of 0.000364mm$^2$, which is more than 100 times smaller than a typical 3.0nH passive inductor.

Using the $Q$-enhanced active inductor, we proposed, designed and implemented two new CMOS tunable UWB LNAs. The active inductor in series with a resistor were utilized to exploit wideband active shunt peaking. Identical UWB active inductors were employed at different nodes parallel to RF signal paths to compensate for the losses of diminishing capactive impedances at high frequencies. This technique kept the frequency responses (gain over frequency) of the LNAs flat over a wide bandwidth. A new three-stage UWB LNA using active inductors at the outputs of the input and output stages was fabricated in a 90nm CMOS digital process, and it exhibited a flat gain of 17.5dB over 3.0-8.8 GHz band. Using a simple configuration, we presented a new two-stage UWB LNA that used one active inductor at the output of the input stage. The two-stage UWB LNA was implemented in a different 90nm digital CMOS process, and it exhibited flat gain of 13.5dB over an extended bandwidth of 2.5-9.5 GHz. The three-stage and two-stage UWB LNAs occupied areas of 0.0227mm$^2$ and 0.0114mm$^2$, respectively, which are more than 20 times smaller than conventional UWB LNAs using passive inductors.

We extended the use of active inductors in exploiting the wideband active shunt-peaking to the design and implementation of UWB mixers and wideband LO drive amplifiers. The active inductors were employed in the transconduc-

tance stage of the mixer to keep the frequency response (gain over frequency) flat and extend the bandwidth. In the LO driver, a two-stage amplifier, active inductors were used at the differential outputs of the input stage, and the overall bandwidth of the LO driver was extended to over 2.0-11.0 GHz.

Finally, we designed and implemented the new active (passive inductorless) CMOS UWB receiver front-end by integrating active CMOS RFICs; a two-stage UWB LNA, two identical UWB mixers in quadrature configuration, and the respective wideband LO driver for the respective mixer. The complete UWB front-end occupied a chip area of 0.261mm$^2$, which is more than 10 times smaller than conventional UWB front-ends. The core front-end (an LNA and a pair of mixers) occupied an area of only 0.149mm$^2$, which is close to the area of a single passive inductor of a few nH. The tunable front-end exhibited a measured flat gain of 22.5dB over 2.5-8.8 GHz bandwidth. The gain can be tuned with ±1.5dB variation around 22.5dB, and the bandwidth can be tuned with ±1.1GHz variation around 8.8GHz. The tunability of the front-end can also allow for adjusting the mismatches between I and Q signals (IF signals) due to process, temperature and supply variations.

## 6.2 Future Research

In this thesis, we showed the advantages of using active inductors instead of passive inductors in the design of RFICs. However, we suggest further research to improve the functionality and decrease the form factor of RFICs and transceivers

1. In this thesis, we emphasize reducing chip areas of RFICs and obtaining tunability using active inductors. For further reduction of chip areas some of the passive resistors and capacitors can be replaced by MOSFET resistors and capacitors, respectively. Active inductors are noisy because of the noise of transistors. Using circuit techniques, noise contribution of active inductors to core RFICs are reduced. The future research will focus on embedding noise cancellation techniques in active inductors.

2. Active inductors also have poor linearity because of nonlinear characteristics of transistors. Moreover, a low-voltage headroom with a low-supply voltage reduces the swing of the signals in active inductors. Hence, the future research will include improving linearity, and increasing signal handling capacity of active inductors.

3. In this thesis, wideband LO drivers were integrated in the UWB front-end without using on-chip oscillators. One of the major challenges is to design an oscillator that can be tuned to the center frequencies of all the bands of the MB-UWB systems, which means to design a voltage controlled oscillator (VCO) that can be tuned over the whole system bandwidth of 7.5GHz. Limited tuning range of passive $LC$ tank VCOs make them unsuitable for MB-UWB applications. Hence, a wide tunable CMOS VCO using tunable active inductors needs to be designed that can cover all the bands of the MB-UWB system. The phase noise of these kinds of active-inductor oscillators are high. The future research will focus on design and development of active CMOS VCOs with reduced phase noise.

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