University of Alberta

Nonlinear Control of a Voltage Source Converter

by

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Abstract

Due to its unique features such as controllable power factor, controllable bi-directional power flow, and rapid dynamic response, Voltage Source Converters (VSCs) have been widely used in various industrial applications such as distributed generation systems, power distribution systems, uninterruptible power supplies (UPS), AC motor drives, etc. To optimize the performance of the VSC, many control algorithms have been proposed. This thesis investigates development of nonlinear controls for the VSC in two applications: power factor control and active power filtering. A detailed description of the dynamic model of the VSC system is presented in different reference frames. An exact linearization-based control scheme is presented for power factor regulation. This control is verified by switched simulation and real-time experiment on a test stand constructed at the Applied Nonlinear Control Lab (ANCL), University of Alberta. In addition, an internal model-based control scheme is introduced to perform active power filtering. This algorithm is verified by simulation.

Acknowledgements

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Chapter 1

Introduction

Voltage Source Converters (VSCs) have been widely used in many industrial applications such as distributed generation systems [14], power distribution systems [10], uninterruptible power supplies (UPS) [7], AC motor drives [3], etc. Given this wide range of applicability, the control of VSCs has become an important research topic, and many control methods have been proposed to optimize its performance. This thesis investigates the control law development for two applications of the VSC: power factor control and active power filtering. A main contribution of this thesis is the development of an experimental test stand for validating the control for these two applications. The control laws considered in this thesis are *nonlinear* in that they account directly for the nonlinear dependence in the model used for control.

1.1 Overview of the Voltage Source Converter (VSC)

With the development of power electronics and pulse width modulation (PWM) techniques, the VSC has led to large improvements in performance of power conversion and transmission applications. It provides unique features such as controllable power factor, controllable bi-directional power flow, and rapid dynamic response [2]. A basic circuit structure of a three-phase VSC is shown in Figure 1.1. Three inductors on the AC side are included to boost the DC voltage and to filter the current ripple due to switching AC terminal voltage [3]. The system has three-phase legs connected in parallel; each leg includes two

switching devices in series and each switch has a free-wheeling diode in parallel. The switching devices can be Gate Turn-Off Thyristors (GTOs), Bipolar Junction Transistors (BJTs), Insulated Gate Bipolar Transistors (IGBTs), power MOSFETs, or Integrated Gate-Commutated Thyristors (IGCTs). Since the IGBTs have high input impedance, like MOSFETs, low conduction losses, like BJTs, and relatively low cost, they are commonly used and adopted in our test stand. The IGBT is turned on when the gating signal is high and the IGBT is turned off when the gating signal is low. With all the IGBTs turned off, the VSC becomes an uncontrolled diode rectifier, and this mode of operation is useful for startup.

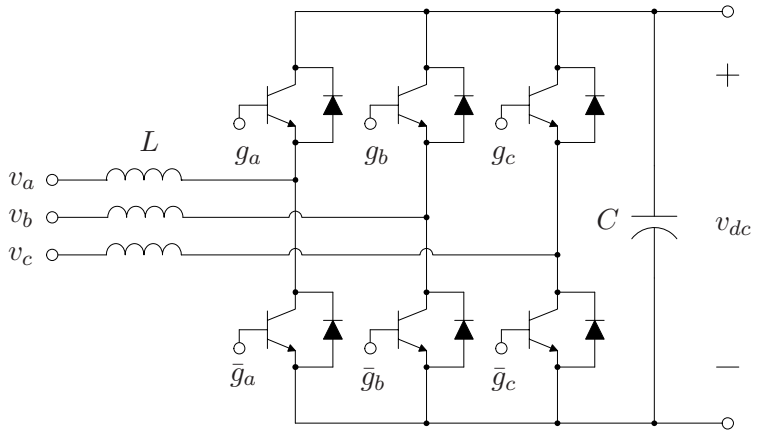
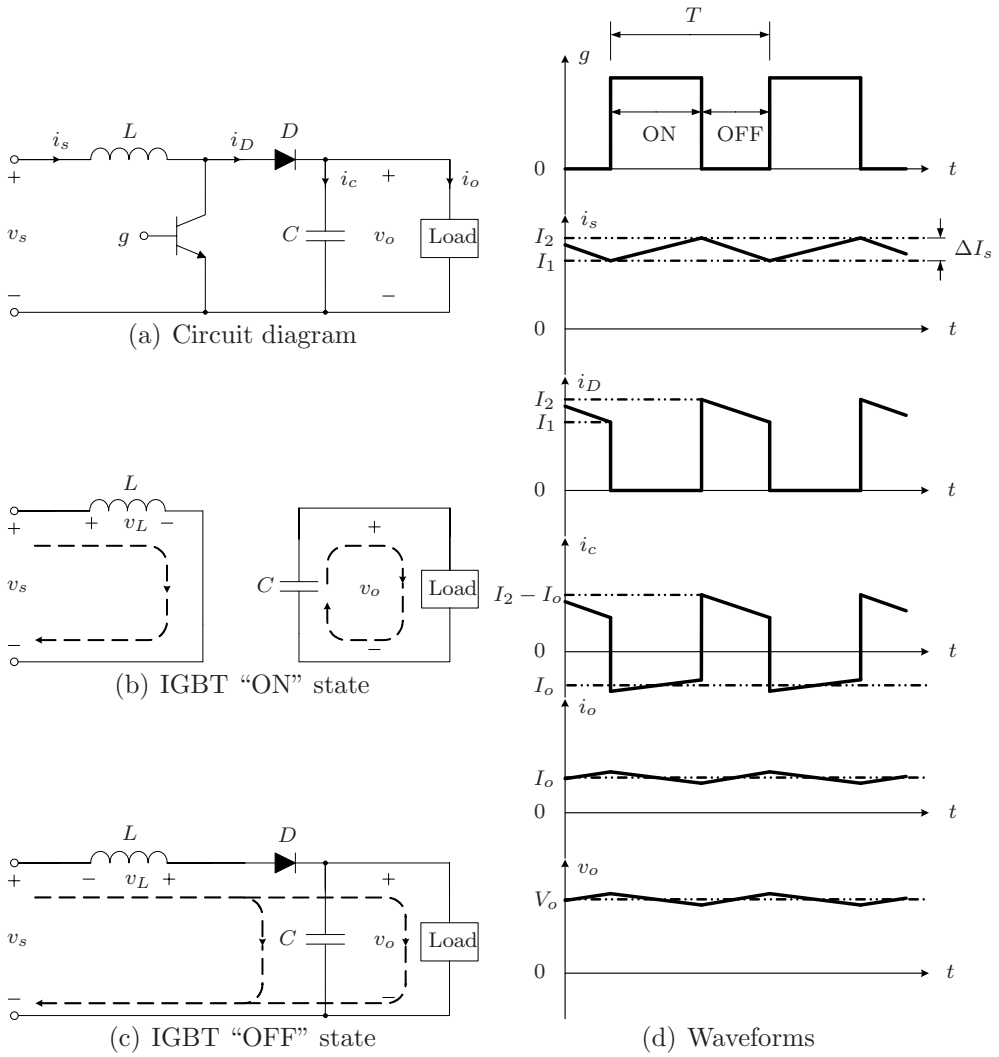


Figure 1.1: Typical circuit diagram of the VSC. The gating signals $g_a, g_b, g_c, \bar{g}_a, \bar{g}_b, \bar{g}_c$ determine the switching states of the IGBTs.

Insight into the operation of the VSC converter can be obtained by considering a DC-DC boost converter [3, 26]. We first review the operation of the boost converter shown in Figure 1.2. We assume continuous conduction to simplify the discussion. That is, the current through the inductor L never falls to zero. Figure 1.2(a) indicates a typical circuit of the boost converter using an IGBT. The input voltage v_s is a positive DC voltage and the load is assumed to be resistive. Based on the state of the IGBT, the operation of the converter can be divided into two modes illustrated in Figure 1.2(b) and 1.2(c). The dashed lines shown in the figures denote the direction of current flow. Typical waveforms of the voltages and currents are shown in



(a) Circuit diagram

(b) IGBT "ON" state

(c) IGBT "OFF" state

(d) Waveforms

Figure 1.2: Operation principles of the DC-DC boost converter. The converter operates in two modes during each gating signal period. When the IGBT is on, the inductor is charging and the capacitor is discharging. When the IGBT is off, the inductor is discharging and the capacitor is charging.

Figure 1.2(d) [25]. When the IGBT is turned *on*, as shown in Figure 1.2(b), the input voltage v_s is directly across the inductor and the input current i_s, which flows though inductor and IGBT, increases from I_1 to I_2. Meanwhile, the capacitor C discharges providing current i_o to the load so that the output voltage v_o decreases. When the IGBT is *off*, as shown in Figure 1.2(c), the diode D conducts and the current which was flowing through the inductor and IGBT now flows through the inductor, diode, capacitor, and load. The capacitor current i_c becomes positive leading to an increase in v_o until the

IGBT is turned on. In addition, the energy stored in the inductor is directed to the capacitor and load. This causes the input current i_s to decrease. For a large C, the peak-to-peak ripple voltage of the capacitor is negligible and v_o is approximately a constant value V_o. Hence, the output current has an approximately constant value of I_o.

The change in input current during the two modes can be derived as

$$\Delta i_{i,ON} \approx \frac{v_s}{L} dT, \quad \Delta i_{i,OFF} \approx \frac{v_o - v_s}{L}(1-d)T$$

where $\Delta i_{i,ON}$ is the change in input current when the IGBT is on, $\Delta i_{i,OFF}$ is the change in input current when the IGBT is off, d is the duty cycle of the gating signal, and T is the time period of the gating signal. Since the current changes during both period are identical, we obtain

$$\frac{v_s}{L} dT = \frac{v_o - v_s}{L}(1-d)T$$

or

$$\frac{v_o}{v_s} = \frac{1}{1-d}$$

Therefore, the output voltage v_o is always larger than input voltage v_s.

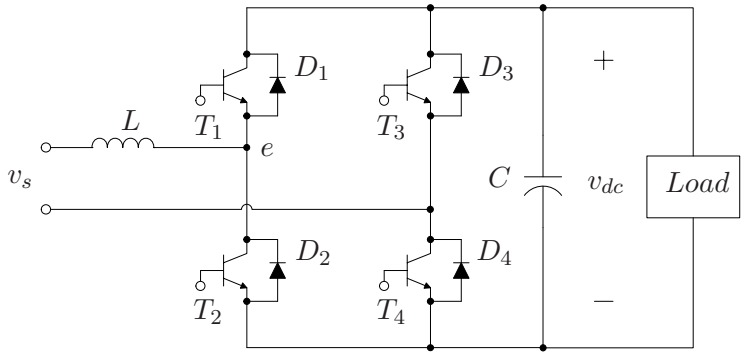


Figure 1.3: Circuit diagram of a single-phase VSC with a pure resistive load.

Now, we extend the discussion to a single-phase VSC shown in Figure 1.3. This system contains four IGBTs T_1, T_2, T_3, T_4 and four diodes D_1, D_2, D_3, D_4. The input v_s is assumed sinusoidal and the load is purely resistive. Figure 1.4 illustrates the operating principles of the single-phase VSC when the input v_s is greater than zero. The dashed lines denote the directions of current flow. In

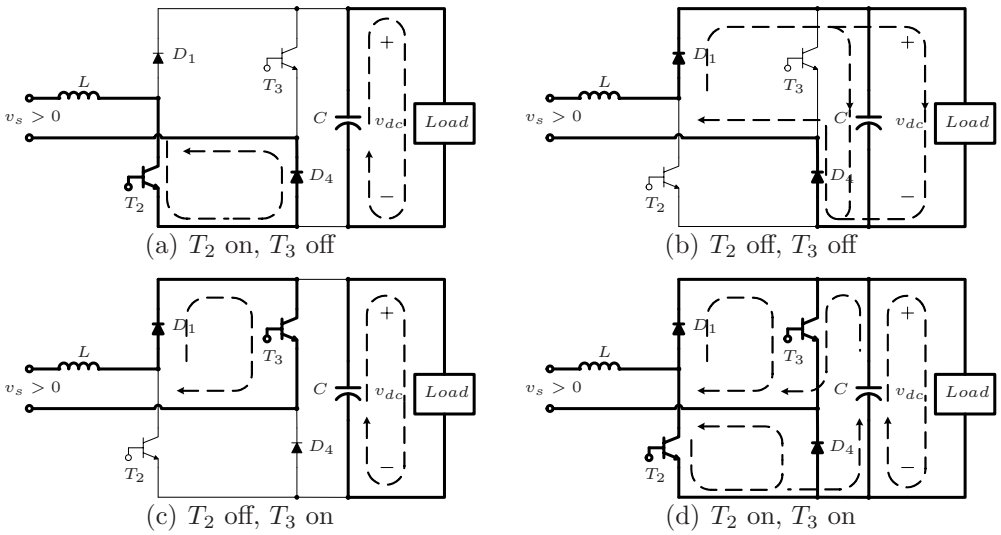


Figure 1.4: Operating principle of the single-phase VSC for positive input voltage. Based on the states of the IGBTs, the VSC operates in four modes in a similar way to the boost converter.

this case, the diodes D_1 and D_4 always conduct regardless of the state of T_1 and T_4. Thus, the components T_2, D_1, D_4, L and T_3, D_1, D_4, L consist of two boost converters in parallel, respectively, shown in Figure 1.4. The case when T_2 is on and T_3 is off is shown in Figure 1.4(a); the VSC operates similar to the boost converter in the first mode shown in Figure 1.2(b). The line inductor L is charged by the input voltage v_s and the input current flows through L, T_2 and D_4. The capacitor provides energy to the load and the DC link voltage v_{dc} decreases. When T_2 and T_3 are both turned off as in Figure 1.4(b), the VSC operates similar to the boost converter in the second mode shown in Figure 1.2(c). The capacitor and load are excited by the input current and the DC link voltage v_{dc} increases. During this period, the energy stored in the inductor is transferred to the capacitor and load. When T_2 is off and T_3 is on as in Figure 1.4(c), the VSC operates similar to the case when T_2 is on and T_3 is off. The line inductor is charged by v_s, the input current flows through L, D_1 and T_3, and the capacitor discharges. When T_2 and T_3 are both on, the VSC is equivalent to that in Figure 1.5. Both the input voltage and DC link voltage are charging the inductor in this period and energy stored in the capacitor is transferred to the inductor and load.

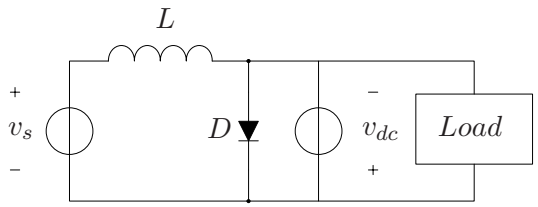


Figure 1.5: Equivalent circuit of the single-phase VSC when both T_2 and T_3 are turned on. In this case, the system is equivalent to two voltage sources, a diode, and a inductor. The diode conducts the current generated by input voltage. Thus, the input voltage does not provide power to the capacitor; the energy stored on the capacitor is transferred to the inductor during this period.

If the input voltage v_s is less than zero, D_2 and D_3 conduct. Thus, T_1, D_2, D_3, L and T_4, D_2, D_3, L consist of two boost choppers in parallel. The operating principle is similar to the $v_s > 0$ case. The single-phase VSC provides the basis to understanding the three-phase case. The three-phase VSC contains three equivalent boost converters in parallel instead of two and has eight operating modes based on different switching states of the IGBTs. Note that, since the VSC operates as a boost converter, the DC link voltage is boosted and should be greater than twice peak phase voltage [3].

Define the counter electromagnetic force (CEMF) voltage as the VSC AC terminal voltage. This voltage is shown as e in Figure 1.3 for the single-phase VSC. And for the three-phase case, the CEMF of phase a is denoted e_a in Figure 1.6. It is important to note that the magnitude and phase angle of the fundamental component of the CEMF voltage can be controlled by the VSC gating signals. This control will be described in Section 2.1.4. In Figure 1.6, assuming the signals v_{sa}, v_{La}, e_a, and i_a are sinusoidal, they can be represented as phasors $\mathbf{V}_{sa}, \mathbf{V}_{La}, \mathbf{E}_a$ and $\mathbf{I}_a$, respectively. We have

$$\mathbf{V}_{sa} = V_{sa}\angle\phi_{v_{sa}}, \quad \mathbf{V}_{La} = V_{La}\angle\phi_{v_{La}}, \quad \mathbf{E}_a = E_a\angle\phi_{e_a}, \quad \mathbf{I}_a = I_a\angle\phi_{i_a}$$

where V_{sa}, V_{La}, E_a, I_a are the amplitudes and $\phi_{v_{sa}}, \phi_{v_{La}}, \phi_{e_a}, \phi_{i_a}$ are the phase angles of the sinusoidal variables v_{sa}, v_{La}, e_a, i_a, respectively. Figure 1.7 shows phasor diagram of the circuit in Figure 1.3 [3]. From the figure we have

$$\mathbf{V}_{sa} = V_{sa}\angle 0, \quad \mathbf{V}_{La} = V_{La}\angle(\phi + \pi/2), \quad \mathbf{E}_a = E_a\angle -\delta, \quad \mathbf{I}_a = I_a\angle\phi$$

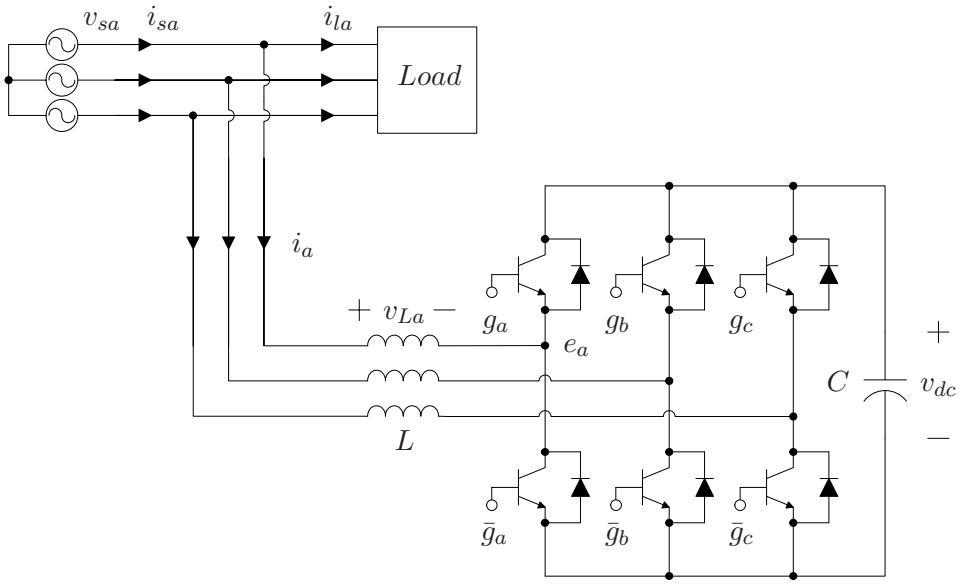


Figure 1.6: Configuration for power factor control using a VSC. The VSC is connected in parallel with the load and controlled to absorb or inject reactive power. A VSC which provides this functionality is called a static VAR compensator (SVC). When the VSC compensates for active current harmonics, the system is called a shunt active filter (SAF).

where ϕ is the phase angle between the i_a and v_{sa}, and δ is the phase angle between v_{sa} and e_a.

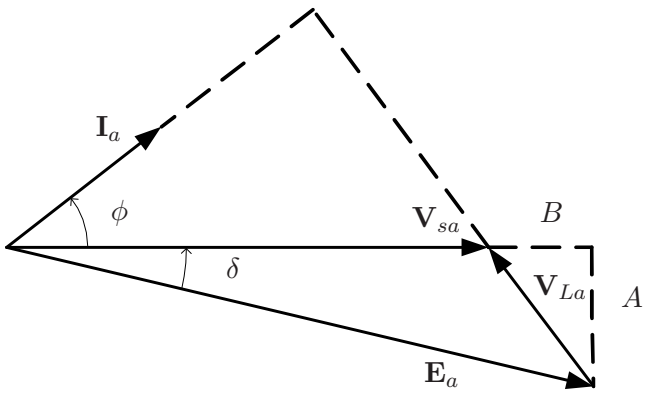


Figure 1.7: Phasor diagram of the AC side variables. $\mathbf{V}_{La} = \mathbf{V}_{sa} - \mathbf{E}_a$ and the input current phasor $\mathbf{I}_a$ is perpendicular with $\mathbf{V}_{La}$.

The active power P and reactive power Q on the AC side of the VSC can

be expressed as

$$P = \mathrm{Re}\{\frac{3}{2}\mathbf{V}_{sa}\mathbf{I}_a^*\} = \frac{3}{2}V_{sa}I_a\cos\phi$$
$$Q = \mathrm{Im}\{\frac{3}{2}\mathbf{V}_{sa}\mathbf{I}_a^*\} = \frac{3}{2}V_{sa}I_a\sin\phi$$

where $\mathbf{I}_a^* = I_a\angle -\phi$, is the complex conjugate of $\mathbf{I}_a$. From Figure 1.7, we have

$$I_a = \frac{V_{La}}{\omega L}$$
$$V_{La}\cos\phi = A = E_a\sin\delta$$
$$V_{La}\sin\phi = B = E_a\cos\delta - V_{sa}$$

Then, we can obtain

$$P = \frac{3V_{sa}E_a}{2\omega L}\sin\delta$$
$$Q = \frac{3V_{sa}}{2\omega L}(E_a\cos\delta - V_{sa})$$

The equations above indicate that P and Q can be controlled by the amplitude of CEMF phasor $\mathbf{E}_a$ and the phase angle δ between $\mathbf{V}_{sa}$ and $\mathbf{E}_a$. Hence, the VSC enjoys a wide range of applications where power factor needs to be regulated. In the next section, some typical VSC applications are introduced; some of which exploit the circuit's ability to control reactive power.

1.2 VSC Applications

In this section we briefly describe various applications of a VSC:

- a Flexible AC Transmission System (FACTS) uses VSCs as static VAR compensators (SVC) (volt-ampere reactive (VAR) is a unit used to measure reactive power in an AC electric power system) or active power filters (APFs),
- AC and DC motor drive system to provide four quadrant operation,
- uninterruptible power supplies (UPS) and battery chargers which perform power factor correction.

1.2.1 Power Transmission System

The widespread use of diode and thyristor rectifiers have negatively affected the power quality of the electrical utility. This is because these nonlinear loads inject harmonic currents into the grid. The distorted currents can cause serious power quality problems. Distorted voltage is generated when current flows through the power line. The highly distorted bus voltage may damage equipment connected on the same bus. In addition, the harmonic currents increase losses during power distribution [3]. VSCs can be used to construct APFs and SVCs which solve grid power quality problems.

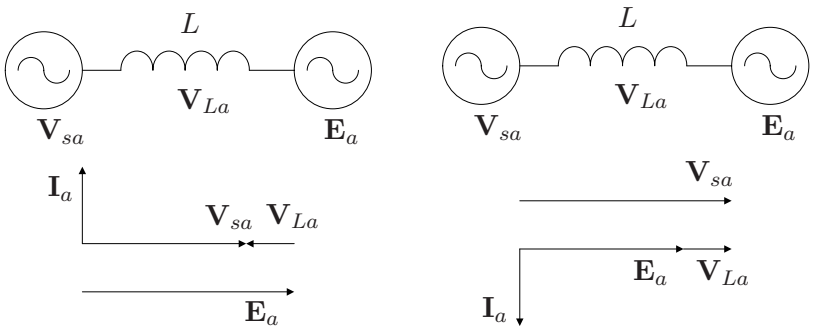
Static VAR Compensators (SVC)

The circuit configuration of a VSC-based SVC is shown in Figure 1.6 [11]. Since the VSC can operate at a programmable lagging or leading power factor, it is able to absorb or generate desired reactive power to achieve VAR compensation. If we assume the active power P is zero, the reactive power on the AC side of the SVC can be expressed as

$$Q = \frac{3}{2} V_{sa} I_a = \frac{3V_{sa}}{2\omega L}(E_a - V_{sa})$$

This means the SVC can be seen as a controllable reactive power source that compensates the grid reactive power via properly steering the AC terminal voltage e_a. Actually, since the SVC is not lossless, the active power $P \neq 0$. Additionally, the only source in the SVC that provides reactive power to achieve VAR compensation is the energy stored in the DC link capacitor. Therefore, a certain amount of real power is also required to charge the capacitor and regulate the DC voltage level. The operation principle of the SVC is shown in Figure 1.8. In Figure 1.8(a), the SVC operates as a leading VAR compensator. The SVC possesses positive reactive power on the AC side and absorbs reactive power from the grid. In Figure 1.8(b), the SVC operates as a lagging VAR compensator. The reactive power of the SVC is negative and it injects reactive power to the grid.

To control the output reactive power Q, the reactive component of the three-phase load current i_{labc} is measured and fed back to the controller of



(a) Leading Power Factor (b) Lagging Power Factor

Figure 1.8: Equivalent circuit and phasor diagram of the SVC. When the current $\mathbf{I}_a$ leads $\mathbf{V}_{sa}$, the SVC operates as a leading VAR compensator. When the current $\mathbf{I}_a$ lags $\mathbf{V}_{sa}$, the SVC operates as a lagging VAR compensator.

SVC as a reference. The negative value of the reactive component of the SVC three-phase current i_{abc} is driven to track this reference. Therefore, the reactive component of the three-phase line current i_{sabc} becomes zero and power factor is regulated to unity.

Shunt Active Filters

The system in Figure 1.6 can also be operated as a shunt active filter (SAF). Although the system configuration is the same as SVC, the control objectives of the SAF are not only to compensate the reactive current, but also to reduce the harmonic components of the active current [23]. The input current i_{labc} of a nonlinear load can be expressed as a sum of a constant DC term, a fundamental term and harmonic terms [21], i.e.,

$$i_{la} = I_{la0} + I_{la1}\cos(\omega t + \varphi_{la1}) + \sum_{n=2}^{N} I_{lan}\cos(n\omega t + \varphi_{lan})$$

$$i_{lb} = I_{lb0} + I_{lb1}\cos(\omega t + \varphi_{lb1}) + \sum_{n=2}^{N} I_{lbn}\cos(n\omega t + \varphi_{lbn})$$

$$i_{lc} = I_{lc0} + I_{lc1}\cos(\omega t + \varphi_{lc1}) + \sum_{n=2}^{N} I_{lcn}\cos(n\omega t + \varphi_{lcn})$$

The instantaneous real power can also be expressed as a sum of a constant and harmonic terms

$$p_l = P_{l0} + \sum_{n=1}^{N} P_{ln} \cos(n\omega t + \psi_n)$$

Note that only the constant term P_{l0} is useful and the harmonic components $\sum_{n=1}^{N} P_{ln} \cos(n\omega t + \psi_n)$ should be compensated by the SAF. In order to achieve VAR compensation the instantaneous reactive load power q_l should be compensated. Therefore, the reference signals for the SAF are

$$\begin{bmatrix} P_{l0} - p_l \\ -q_l \end{bmatrix} \tag{1.1}$$

Another essential control objective for the SAF is to maintain DC voltage in a region $[V_m, V_M]$ to avoid discharge and overcharge of the DC link capacitor [22]. This objective is highly coupled with the first one. Since only the active current delivers energy to charge the capacitor, v_{dc} is indirectly controlled by active power. On the other hand, the DC voltage is the main power source of the SAF. When v_{dc} drops to a minimum value of twice the peak phase voltage, the free-wheeling diodes take over the current conduction. At this point the controller cannot reduce v_{dc} any lower. In addition, the SAF is not actually lossless. Therefore, the actual active power should compensate the power losses on the SAF and the power required to maintain v_{dc}. The detailed control of the SAF is discussed in Chapter 4.

1.2.2 AC Motor Drives

Since the VSC provides bi-directional power transmission and is capable of four-quadrant operation, it can be used to form a double-sided AC-DC-AC converter to drive synchronous motors as shown in Figure 1.9 [3]. The motor velocity, torque, and the direction of the motor's rotation are regulated by the load-side VSC. Four quadrant operation of the motor is performed with properly designed gating signals of the load-side VSC [20]. In motoring mode, the load-side VSC delivers energy to the motor and determines the direction of rotation. In regenerative braking mode, the motor operates as a generator,

the kinetic energy in the machine is transferred to the dc link source and the motor speed decreases. Traditionally, this regenerated energy is dissipated in a resistive load and transformed to heat. However, the line-side VSC not only provides VAR compensation and active filtering but also can deliver the regenerated energy to the AC source. This energy can be stored in a DC battery or flywheel for future use.

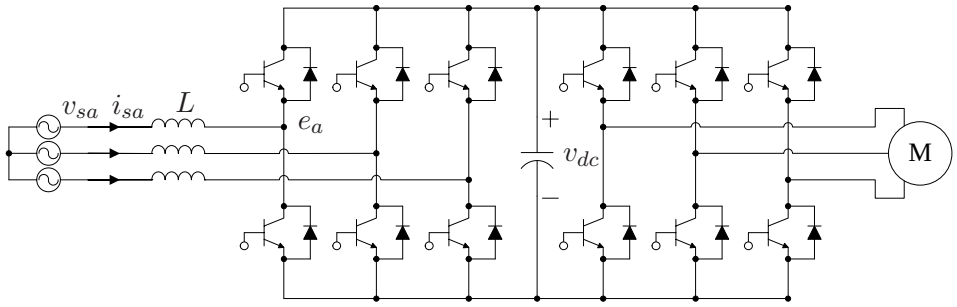


Figure 1.9: Double-sided AC-DC-AC converter used in a motor drive. Batteries or flywheels are not shown in this figure.

1.2.3 Uninterruptible Power Supply (UPS)

Figure 1.10 shows a traditional configuration of an uninterruptible power supply (UPS) with isolation transformer [7]. The transformer increases system weight and cost. And the rectifier draws harmonics from the grid and reduces the power quality. Alternatively, a VSC can replace the rectifier and transformer as shown in Figure 1.11. This is because the VSC can compensate the current harmonics, correct the line-side power factor, and provide the required DC voltage.

1.3 Thesis Outline and Contributions

Chapter 2 gives a detailed derivation of an averaged bilinear model for the VSC in three reference frames. We present the identification of the model parameters for the test stand considered. We describe the Sine Pulse Width Modulation (SPWM) scheme used and derive the relation between modulation parameters, gating signals, and VSC AC terminal voltage. We present

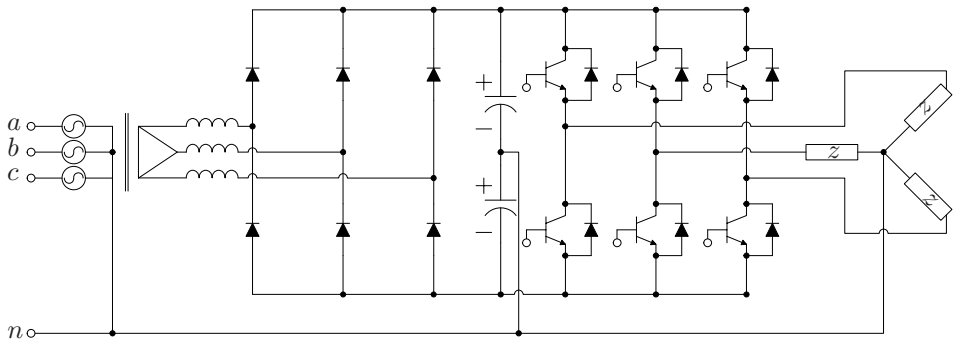


Figure 1.10: Typical UPS circuit diagram with line-side rectifier. The neutral of the power supply, the mid point of the DC bus, and the neutral of the load are connected.

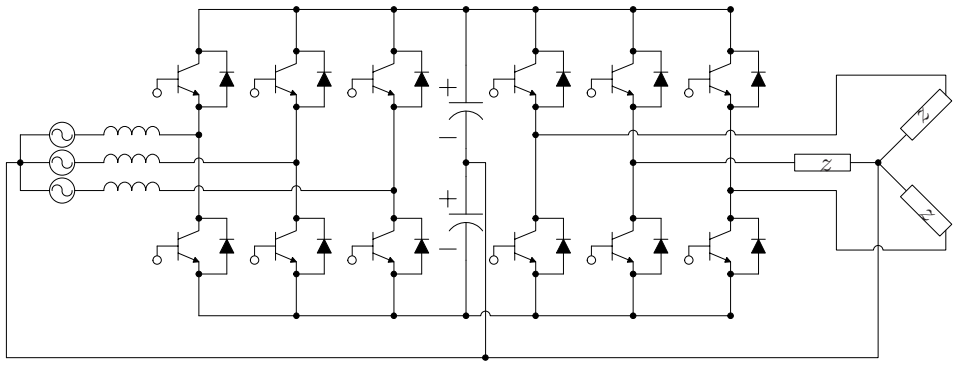


Figure 1.11: UPS circuit diagram with line-side VSC to provide VAR compensation and harmonic cancelation.

a nonlinear control method also derived in [29] and modify it to include nonzero d-axis current at equilibrium. Finally we present Simulink simulation results for this control. The contribution of this chapter involves a number of improvements relative to existing work: we present details on the model parameter identification, compensate the nonlinear controller for nonzero d-axis current in steady-state, and provide more accurate simulations which account for switching behaviour.

Chapter 3 provides detailed discussion on experimental implementation of power factor control. A Semiteach VSC module is interfaced by a dSPACE control system to implement the control algorithm introduced in Chapter 2. Sensor boards are built to provide a measurement of the system state. Level shift-

ing boards are constructed for interfacing the VSC drivers and the dSPACE system. Detailed information of each component of the test stand is provided and and how they are interconnected. Several tests are described to validate the functionality of the components and system. The nonlinear control scheme introduced in Chapter 2 is implemented with the test stand and the results are analyzed. The contribution of this chapter is to establish the experimental test stand and implement the control scheme to achieve power factor control. These achievements involve efforts on parameter identification, circuit boards design and fabrication, experiment design and implementation.

Chapter 4 discusses the application of the VSC as an SAF. First a dynamic model of the VSC-based APF is presented. This model differs from that given in Chapter 2. We transform this model's state representation to power variables and review the required power theory. We present fundamental results on internal model control (IMC) for LTI systems. This theory is applied to solve a robust current tracking problem and an additional DC voltage feedback is added to ensure tracking error is bounded. The work here is based on recent results in [22] and the contribution provided is to demonstrate this approach's functionality in simulation.

Chapter 5 summarizes the thesis and discusses future research direction.

Chapter 2

Averaged Model and Power Factor Control

2.1 VSC System Modelling

Using basic circuit analysis and a power balance, a three-dimensional two-input mathematical model for the VSC system shown in Figure 2.1 is derived. The phase angle and magnitude of the VSC AC terminal voltage relative to the AC supply voltage directly relate to the power factor of the system. In order to establish a sinusoidal voltage at the AC terminal of the VSC with appropriate phase angle and magnitude, a three-phase Sine PWM (SPWM) is chosen to drive the switches. Using the fundamental component of the VSC AC terminal voltages, an averaged model is obtained which is forced by two SPWM parameters. A commonly used reference frame transformation is then used to obtain a state representation in which the dynamics has a relatively simple form.

An equivalent three-wire circuit of the VSC system is shown in Figure 2.1. The AC voltage supply is assumed balanced throughout this thesis and generates three-phase voltages with identical amplitude and $2\pi/3$ offset in phase. The phase voltages are denoted v_a, v_b, v_c, the phase currents are denoted i_a, i_b, i_c, and the phase voltages of the VSC AC terminals are denoted e_a, e_b, e_c. The switching signals $g_a, g_b, g_c, \bar{g}_a, \bar{g}_b, \bar{g}_c$ are the physical control inputs of the VSC. A PWM strategy is applied to generate these signals, and they are binary-valued. The signals $\bar{g}_a, \bar{g}_b, \bar{g}_c$ are complements of g_a, g_b, g_c, respectively.

An IGBT is turned on when its gate signal is high and turned off when it is low. The DC terminal voltage is denoted v_{dc} and current is denoted i_{dc}.

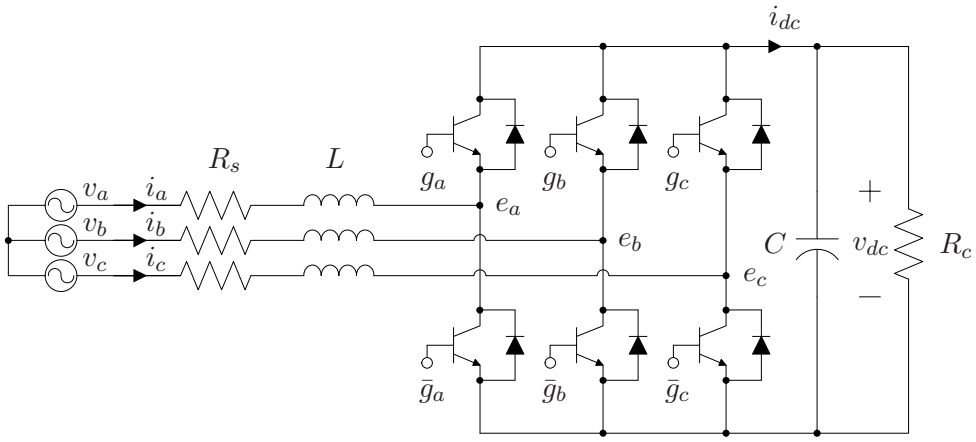


Figure 2.1: A typical circuit of the three-phase VSC. Four parameter are used and the IGBTs and diodes are lossless.

In our experimental setup an AC supply provides a balanced three-phase 120 V root mean square (RMS) voltage which is fed to a variable transformer to obtain v_a, v_b, v_c. This transformer allows the amplitudes of v_a, v_b, v_c to be gradually increased to avoid large inrush currents while charging the capacitor. The transformer is manually adjusted such that the peak phase voltage is 60 V. Based on the application note of the IGBT module [9], the RMS values of i_a, i_b, i_c should be limited to 30 A and e_a, e_b, e_c should be less than 440 V. The DC link voltage v_{dc} is always higher than twice the peak phase voltage as mentioned in Chapter 1 and lower than 500 V due to the measuring capability of the sensor boards. This means that 120 V $\leq v_{dc} \leq$ 500 V.

The VSC system includes four parameters L, C, R_s, and R_c. The parameter L models a three-phase inductor which is designed to boost the DC voltage and to reduce the current harmonics caused by the IGBTs switching. We assume the inductance of each phase is identical and equal to its nominal value of 2 mH. The parameter C models the capacitance which is connected in parallel with VSC DC terminal. There are two identical DC bank filtering capacitors integrated in the Semiteach system. Each one has rated value 2200 μF/400 V. Connected in series, the equivalent capacitance on the DC

bus is 1100 μF/800 V. The main sources of R_s are the conduction losses on the wires and the reactor. This resistance is directly measured to be about 0.18 Ω for each phase. Another important source of R_s are the conduction losses of the IGBTs. Figure 2.2 shows the typical output characteristics of the collector current i_{ce} versus the collector-emitter voltage v_{ce} [25]. There are two regions of the operation: saturation region and active region. In the saturation region, the collector current i_{ce} increases with increasing collector-emitter voltage v_{ce}. In the active region, the collector current i_{ce} remains almost constant as a function of v_{ce}. When the IGBT is switching, it operates in the saturation region since the voltage across the IBGT is relevantly low. The slope of the steep region of the output characteristic determines the resistance R_{ce} which models the conduction losses of the IGBT. From the output characteristics of the Semiteach IGBT module data sheet, the value of R_{ce} is obtained as 0.03 Ω. Therefore, the nominal value of R_s is the sum of the two parts and taken as 0.21 Ω.

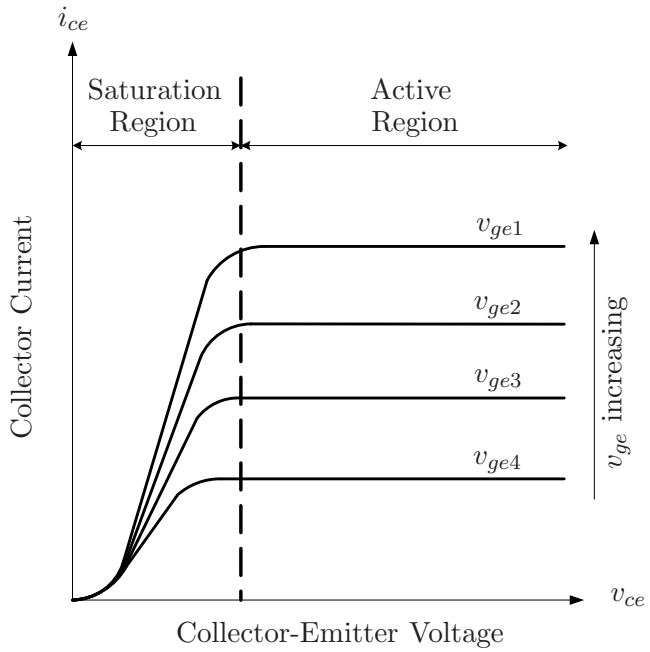


Figure 2.2: Output characteristic of IGBTs. The transistor can operate in two regions. With increasing gating voltage v_{ge}, i.e., $v_{ge1} > v_{ge2} > v_{ge3} > v_{ge4}$, the collector current i_{ce} can reach higher values in the active region.

The switching loss of the IGBT is modeled by R_c. Each SKM50GB123D IGBT module contains two IGBTs and their switching losses can be expressed as $P = f_t(E_{on} + E_{off})$ [25], where f_t is the switching frequency, E_{on} and E_{off} is the energy dissipated during turning on and off, respectively. From the data sheet of the IGBT module, E_{on} is 7 mJ and E_{off} is 4.5 mJ at $i_{ce} =$ 30 A and $v_{dc} =$ 500 V. With $f_t = 5$ kHz, the switching loss P is 57.5 W. Since the VSC includes three IGBT modules, the total switching loss of the converter is $3P$ which is 172.5 W. Therefore, we take a nominal value of $R_c = v_{dc}^2/3P = 1.45\,\text{k}\Omega$. Since the actual power losses on IGBTs and diodes are decoupled from the components and modeled as parts of R_s, R_c, the IGBTs and diodes in Figure 2.1 are regarded as lossless. Table 2.1 summarizes the model's parameters. Evidently, the values of these parameters are only nominal since in practice their values are affected by temperature and the assumptions under which they are derived.

Parameter	Values
L	$2mH$
C	$1100\mu F$
R_s	0.21Ω
R_c	$1.45k\Omega$

Table 2.1: The values of the parameters used in the model. The values are directly measured or calculated approximately. In practice temperature and operating conditions can affect the parameters.

Using Kirchoff's voltage law on the AC side of the converter we obtain

$$L\frac{d}{dt}i_{abc} = v_{abc} - R_s i_{abc} - e_{abc}$$

where

$$v_{abc} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_m \cos(\omega t) \\ V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_m \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix}, \quad i_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad e_{abc} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

The angular frequency $\omega = 2\pi f_i$ where f_i is the fundamental frequency of the AC source and equals to 60 Hz in our case. With the assumption of

lossless IGBTs and diodes, the instantaneous power at the VSC's AC and DC terminals is balanced, which means

$$i_a e_a + i_b e_b + i_c e_c = i_{dc} v_{dc} \tag{2.1}$$

Since i_{dc} can be expressed in terms of v_{dc}

$$i_{dc} = C\frac{dv_{dc}}{dt} + \frac{v_{dc}}{R_c}$$

the DC voltage dynamics can be derived as

$$\frac{dv_{dc}}{dt} = \frac{i_a e_a + i_b e_b + i_c e_c}{C v_{dc}} - \frac{v_{dc}}{C R_c}$$

Therefore, we have

$$\begin{aligned} \frac{d}{dt} i_{abc} &= -\frac{R_s}{L} i_{abc} + \frac{1}{L} v_{abc} - \frac{1}{L} e_{abc} \\ \frac{dv_{dc}}{dt} &= \frac{i_a e_a + i_b e_b + i_c e_c}{C v_{dc}} - \frac{v_{dc}}{C R_c} \end{aligned} \tag{2.2}$$

We remark that since $i_a + i_b + i_c = 0$ only two of the three differential equations for current are independent. Hence, the dynamics has three states. We remark that since we assume $v_a + v_b + v_c = 0$, then $e_a + e_b + e_c = 0$ and if we treat the AC terminal voltages as system inputs, the dynamics has two inputs.

2.1.1 Other Configurations and Models

The literature contains various VSC models. For example, a model is derived under the assumption of negligible input resistance loss and switching device loss [12]. With this assumption, the input power is identical with the AC terminal power and (2.1) becomes

$$i_a v_a + i_b v_b + i_c v_c = i_{dc} v_{dc} \tag{2.3}$$

and the VSC system model is

$$\begin{aligned} \frac{d}{dt} i_{abc} &= -\frac{R_s}{L} i_{abc} + \frac{1}{L} v_{abc} - \frac{1}{L} e_{abc} \\ \frac{dv_{dc}}{dt} &= \frac{i_a v_a + i_b v_b + i_c v_c}{C v_{dc}} - \frac{v_{dc}}{C R_c} \end{aligned}$$

We apply a change of coordinates to transform the last dynamic to v_{dc}^2-coordinates. The model becomes

$$\begin{aligned}\frac{d}{dt}i_{abc} &= -\frac{R_s}{L}i_{abc} + \frac{1}{L}v_{abc} - \frac{1}{L}e_{abc}\\ \frac{dv_{dc}^2}{dt} &= \frac{2(i_a v_a + i_b v_b + i_c v_c)}{C} - \frac{2v_{dc}^2}{CR_c}\end{aligned}$$

which is a LTI system which simplifies its control [24].

The model described by (2.2) can also be simplified by taking the parameter $R_c = \infty$ [21]. This assumption leads to a system which contains three parameters, i.e., L, R, and C. Only one resistance R is utilized to model power losses. The resulting model is given by

$$\begin{aligned}\frac{d}{dt}i_{abc} &= -\frac{R}{L}i_{abc} + \frac{1}{L}v_{abc} - \frac{1}{L}e_{abc}\\ \frac{dv_{dc}}{dt} &= \frac{1}{Cv_{dc}}i_{abc}^T e_{abc}\end{aligned} \tag{2.4}$$

This model assumption reduces the complexity of the control law analysis and used in Chapter 4 on active filtering. However, In power factor control section, we choose to keep two resistive components since R_c is a function of IGBT switching frequency whereas R_s is affected by heat. Separating the losses into two parts isolates two distinct physical phenomenon and allows, for example, an analysis of controller sensitivity to these effects.

The four-wire VSC system is another common configuration which appears in the literature. This system appears in uninterruptible power supply (UPS) applications [7]. Figure 2.3 shows the typical four-wire system [8]. The star point of the power source and the middle point of the two capacitors are connected by an extra wire. Therefore, the sum of the AC currents is not necessarily zero and the voltage drop on the two capacitors are not equal. The corresponding dynamic model of this configuration is

$$\begin{aligned}\frac{d}{dt}i_{abc} &= -\frac{R}{L}i_{abc} + \frac{1}{L}v_{abc} - \frac{1}{L}e_{abc} + z_2\\ \frac{dz_1}{dt} &= \frac{1}{Cz_1}i_{abc}^T e_{abc}\\ \frac{dz_2}{dt} &= -\frac{i_a + i_b + i_c}{C}\end{aligned}$$

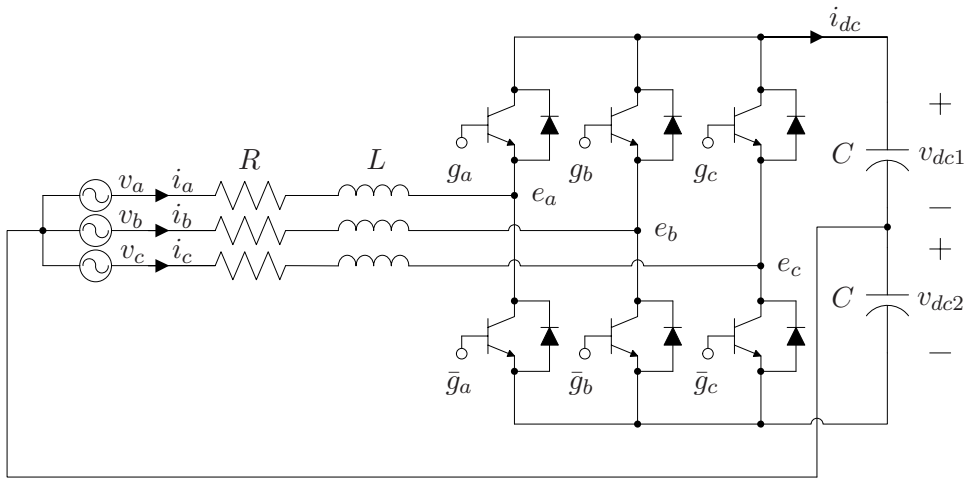


Figure 2.3: Typical four-wire configuration of the VSC used in UPS applications. Since the neutral point is connected to the mid point of the DC link, the voltages across the capacitors is not necessarily equal.

Where $z_1 = v_{dc1} + v_{dc2}$ and $z_2 = v_{dc2} - v_{dc1}$. The four-wire configuration increases the complexity of the model and control algorithm. In UPS applications the star point of the supply is not only connected to the middle point of the two capacitors, but also connected to the neutral point of the load. Therefore, the load neutral point is prevented from floating and a current path is provided to release fault currents.

2.1.2 Sinusoidal Pulse Width Modulation (SPWM)

A number of PWM techniques exist to drive the VSC gates, e.g. SPWM, space-vector PWM (SVPWM), selected harmonic elimination PWM, and delta modulation [3]. In this thesis we adopt the commonly used SPWM; this technique is relatively simple conceptually and easy to implement. The principle of SPWM generation is illustrated in Figure 2.4. The control generates three-phase sinusoidal modulating signals v_{ma}, v_{mb}, v_{mc} which are compared with a triangular carrier wave v_t which has constant amplitude 1 and frequency f_t.

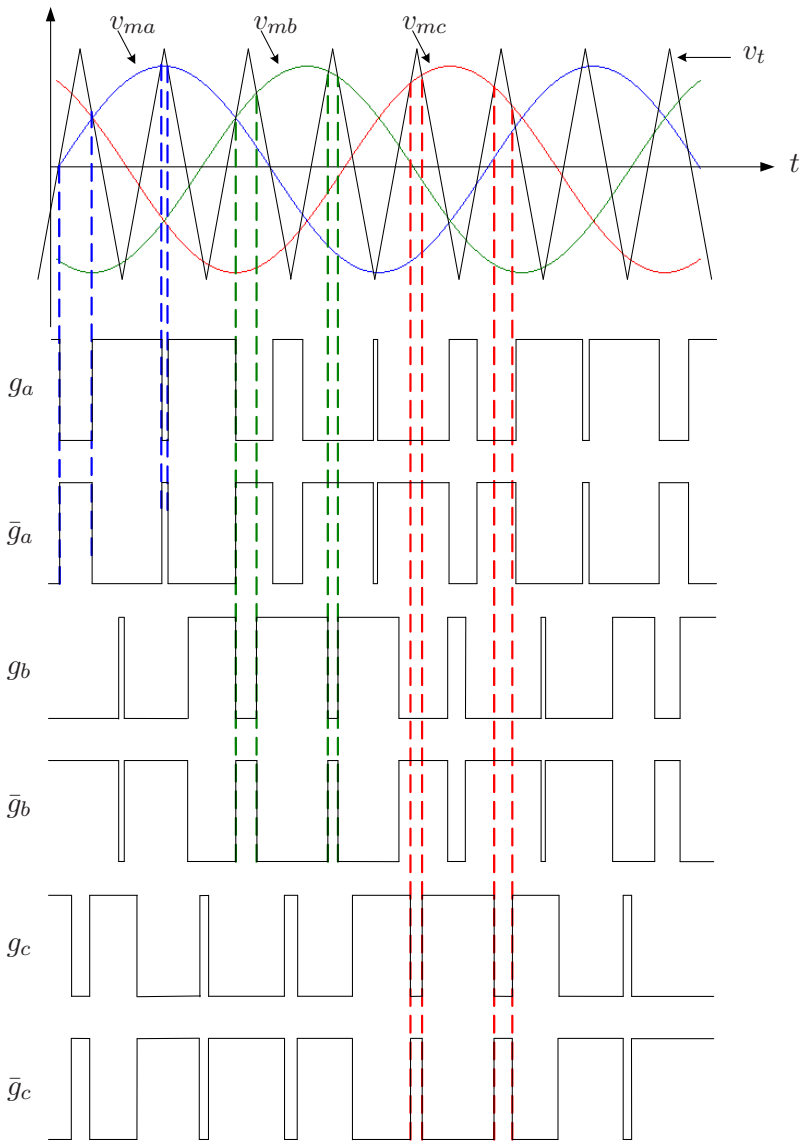


Figure 2.4: Three-phase SPWM is generated by comparing three-phase modulation signals with a carrier signal. When the modulation signal is greater than the carrier signal, the corresponding SPWM is at high level; when the modulation signal is lower than the carrier signal, the corresponding SPWM is at low level. In order to excite three-phase VSC, each modulation signal generates a pair of complementary SPWM signals.

The three-phase modulating signals are defined as

$$\begin{aligned} v_{ma} &= m_a \cos(\omega t + \delta) \\ v_{mb} &= m_a \cos(\omega t + \delta - \frac{2\pi}{3}) \\ v_{mc} &= m_a \cos(\omega t + \delta + \frac{2\pi}{3}) \end{aligned} \tag{2.5}$$

where m_a is the modulation index and δ is the phase shift. Let 1 denote "closed" or ON state of the switch and 0 denote "open" of OFF state of the switch. The states of gating signals are given by

$$g_a = \begin{cases} 1, & v_{ma} > v_{th} \\ 0, & v_{ma} < v_{th} \end{cases} \quad g_b = \begin{cases} 1, & v_{mb} > v_{th} \\ 0, & v_{mb} < v_{th} \end{cases} \quad g_c = \begin{cases} 1, & v_{mc} > v_{th} \\ 0, & v_{mc} < v_{th} \end{cases}$$

where v_{th} is the threshold voltage of the IGBTs. It is clear that the duty cycles of the generated SPWM waves are determined by m_a and δ which are the two inputs determined by the control. The inputs are constrained by the saturations

$$0 \leq m_a \leq 1, \quad -\frac{\pi}{2} \leq \delta \leq \frac{\pi}{2} \tag{2.6}$$

The frequency of the modulating signals is chosen equal to the desired fundamental component of the VSC terminal voltages e_{abc} which in our case is line angular frequency ω. So-called over-modulation occurs when $m_a > 1$ and will not be considered in this thesis. In our test stand we take $f_t = 5$ kHz which corresponds to a constant frequency modulation ratio of $f_t/f_i = 83$.

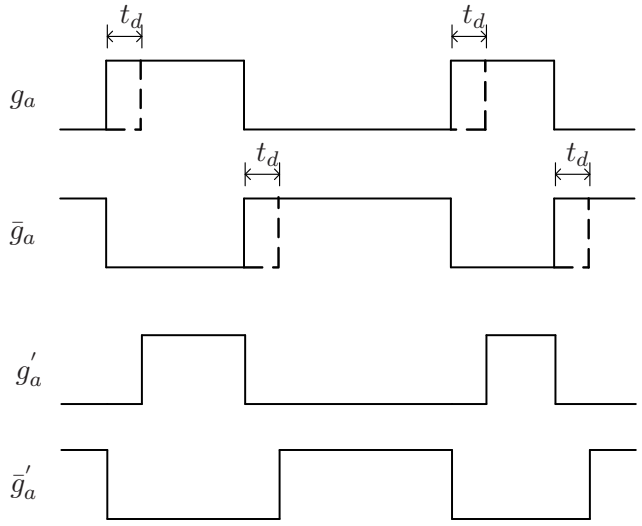


Figure 2.5: Implementation of the dead-time is achieved by delaying the raising edges of the SPWM to avoid the IGBTs on the same leg being turned on simultaneously.

To avoid short circuiting the capacitor voltage during the switching, a dead-time or blank-time is introduced into the SPWM signals. Figure 2.5 indicates

the implementation of the dead-time. $g_a^{'}$ and $\bar{g}_a^{'}$ are the shifted signals of g_a and $\bar{g}_a$. Note that only the raising edges are delayed by a time period t_d.

2.1.3 Reference Frame Theory

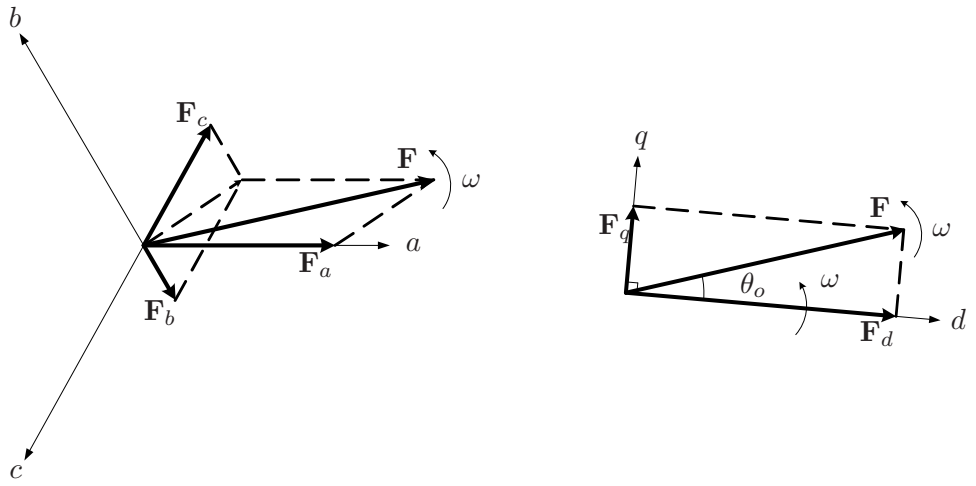
To simplify the analysis of three-phase circuits, reference frame transformations are often applied to change the variables from the original *a*-*b*-*c* coordinates. There are a number of transformations possible, such as a synchronous reference frame transformation (also referred to as *d*-*q* transformation), arbitrary reference frame transformation. In this thesis, we use the synchronous and stationary reference frames. The synchronous reference frame transformation is applied in power factor control and the stationary reference frame transformation is used for active filtering discussed in Chapter 4.

Synchronous Reference Frame Transformation The three-phase sinusoidal variables f_a, f_b, f_c can be represented as phasors $\mathbf{F}_a = F_a\angle 0, \mathbf{F}_b = F_b\angle 3\pi/2, \mathbf{F}_c = F_c\angle -3\pi/2$ in *a*-*b*-*c* coordinates, where F_a, F_b, F_c are the amplitudes of f_a, f_b, f_c and ω is the fundamental angular frequency of f_a, f_b, f_c. We can define a phasor $\mathbf{F} = \mathbf{F}_a + \mathbf{F}_b + \mathbf{F}_c$ which is rotating in the *a*-*b*-*c* coordinates with an angular velocity ω shown in Figure 2.6(a). Then, the synchronous reference frame (or *d*-*q* reference frame) is defined so that the *d* axis lags $\mathbf{F}$ with a constant phase shift θ_o and the *q* axis leads 90° ahead to the *d* axis, as shown in Figure 2.6(b) [18]. Because the *d*-*q* coordinates rotates synchronously with $\mathbf{F}$ in the *a*-*b*-*c* coordinates, it is called the synchronous reference frame. The phasor $\mathbf{F}$ can be mapped to the *d*-*q* coordinates using the linear transformation

$$\mathbf{F}_d = \mathbf{F}\cos\theta_o, \quad \mathbf{F}_q = \mathbf{F}\sin\theta_o \tag{2.7}$$

Therefore, we define a transformation that maps the phasors from *a*-*b*-*c* coordinates to *d*-*q* coordinates using [3]

$$\begin{bmatrix} \mathbf{F}_d \\ \mathbf{F}_q \\ \mathbf{F}_o \end{bmatrix} = K \begin{bmatrix} \mathbf{F}_a \\ \mathbf{F}_b \\ \mathbf{F}_c \end{bmatrix}$$



(a) a-b-c coordinates (b) d-q coordinates

Figure 2.6: Fundamental principle of the synchronous reference frame transformation. The d-q coordinates rotates synchronously with the $\mathbf{F}$ which is the sum of the phasors $\mathbf{F}_a, \mathbf{F}_b, \mathbf{F}_c$.

where

$$K = \frac{2}{3}\begin{bmatrix} \cos(\omega t + \theta_o) & \cos(\omega t + \theta_o - \frac{2\pi}{3}) & \cos(\omega t + \theta_o + \frac{2\pi}{3}) \\ \sin(\omega t + \theta_o) & \sin(\omega t + \theta_o - \frac{2\pi}{3}) & \sin(\omega t + \theta_o + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

To simplify the transformation, we define the d axis to be in phase with $\mathbf{F}$, which means $\theta_o = 0$. This implies (2.7) becomes $\mathbf{F}_d = \mathbf{F}, \mathbf{F}_q = 0$, K is

$$K = \frac{2}{3}\begin{bmatrix} \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin\omega t & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.8}$$

and

$$K^{-1} = \begin{bmatrix} \cos\omega t & \sin\omega t & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & \sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{2.9}$$

One important property of the d-q transformation is that balanced variables take a simple form. We have

$$f_a = F\cos(\omega t), \quad f_b = F\cos(\omega t - \frac{3\pi}{2}), \quad f_c = F\cos(\omega t + \frac{3\pi}{2})$$

the corresponding f_d, f_q are constant quantities and can be derived as

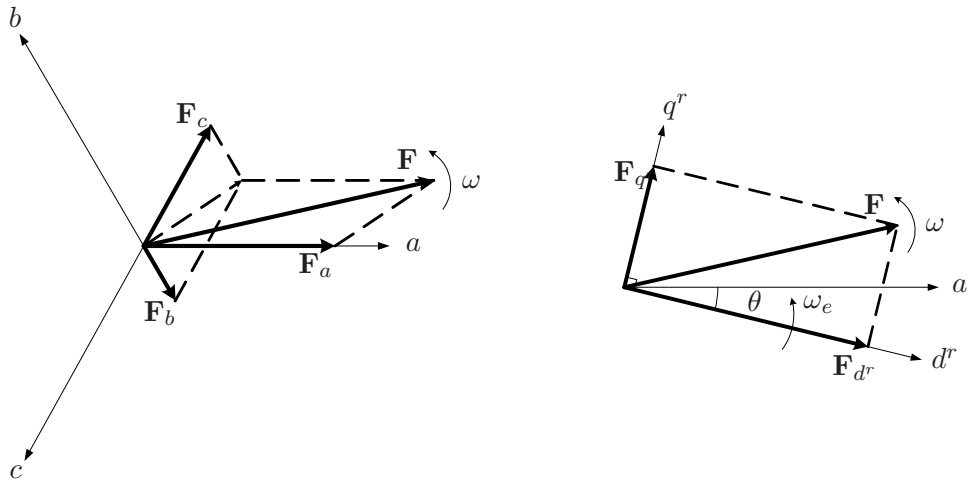
$$\begin{aligned}
f_d =& \frac{2}{3}\left(f_a\cos(\omega t+\theta_o)+f_b\cos\left(\omega t+\theta_o-\frac{2\pi}{3}\right)+f_c\cos\left(\omega t+\theta_o+\frac{2\pi}{3}\right)\right)\\
=& \frac{2}{3}\left(F\cos(\omega t)\cos(\omega t+\theta_o)+F\cos(\omega t-\frac{2\pi}{3})\cos\left(\omega t+\theta_o-\frac{2\pi}{3}\right)\right.\\
&\left.+F\cos(\omega t+\frac{2\pi}{3})\cos\left(\omega t+\theta_o+\frac{2\pi}{3}\right)\right)\\
=& \frac{2}{3}F\cos\theta_o\left(\cos^2\omega t+\cos^2\left(\omega t-\frac{2\pi}{3}\right)+\cos^2\left(\omega t+\frac{2\pi}{3}\right)\right)\\
&-\frac{2}{3}F\sin\theta_o\left(\cos\omega t\sin\omega t+\cos\left(\omega t-\frac{2\pi}{3}\right)\sin\left(\omega t-\frac{2\pi}{3}\right)\right.\\
&\left.+\cos\left(\omega t+\frac{2\pi}{3}\right)\sin\left(\omega t+\frac{2\pi}{3}\right)\right)\\
=& F\cos\theta_o
\end{aligned}$$

$$\begin{aligned}
f_q =& \frac{2}{3}\left(f_a\sin(\omega t+\theta_o)+f_b\sin\left(\omega t+\theta_o-\frac{2\pi}{3}\right)+f_c\sin\left(\omega t+\theta_o+\frac{2\pi}{3}\right)\right)\\
=& \frac{2}{3}\left(F\cos(\omega t)\sin(\omega t+\theta_o)+F\cos(\omega t-\frac{2\pi}{3})\sin\left(\omega t+\theta_o-\frac{2\pi}{3}\right)\right.\\
&\left.+F\cos(\omega t+\frac{2\pi}{3})\sin\left(\omega t+\theta_o+\frac{2\pi}{3}\right)\right)\\
=& \frac{2}{3}F\sin\theta_o\left(\cos^2\omega t+\cos^2\left(\omega t-\frac{2\pi}{3}\right)+\cos^2\left(\omega t+\frac{2\pi}{3}\right)\right)\\
&+\frac{2}{3}F\cos\theta_o\left(\cos\omega t\sin\omega t+\cos\left(\omega t-\frac{2\pi}{3}\right)\sin\left(\omega t-\frac{2\pi}{3}\right)\right.\\
&\left.+\cos\left(\omega t+\frac{2\pi}{3}\right)\sin\left(\omega t+\frac{2\pi}{3}\right)\right)\\
=& F\sin\theta_o
\end{aligned}$$

Note that when $\theta_o = 0$, the d component is identical with the amplitude of the variable in the *a*-*b*-*c* coordinates and the q component is identically zero. This fact is exploited to simplify the model and derivation of the control for the VSC for power factor control. Applying the synchronous reference frame transformation (2.8) to (2.2), we obtain

$$\begin{aligned}
\frac{di_d}{dt} &= -\frac{R_s}{L}i_d+\omega i_q+\frac{v_d}{L}-\frac{e_d}{L}\\
\frac{di_q}{dt} &= -\frac{R_s}{L}i_q-\omega i_d+\frac{v_q}{L}-\frac{e_q}{L}\\
\frac{dv_{dc}}{dt} &= \frac{3}{2}\frac{e_di_d+e_qi_q}{Cv_{dc}}-\frac{v_{dc}}{CR_c}.
\end{aligned} \tag{2.10}$$

Since the AC supply is assumed balanced, v_d is constant and $v_q = 0$.



(a) a-b-c coordinates (b) d^r-q^r coordinates

Figure 2.7: Fundamental principle of the arbitrary reference frame transformation. The d^r-q^r coordinates rotates arbitrarily.

Arbitrary Reference Frame Transformation Different from the synchronous reference frame transformation, the arbitrary reference frame transformation maps $\mathbf{F}$ to d^r-q^r coordinates which is similar to the d-q coordinates but an arbitrary angular velocity is used. Shown in Figure 2.7(b), the angular velocity ω_e is arbitrary and angle $\theta = \omega_e t$ [19]. The transformation matrix K can be expressed as

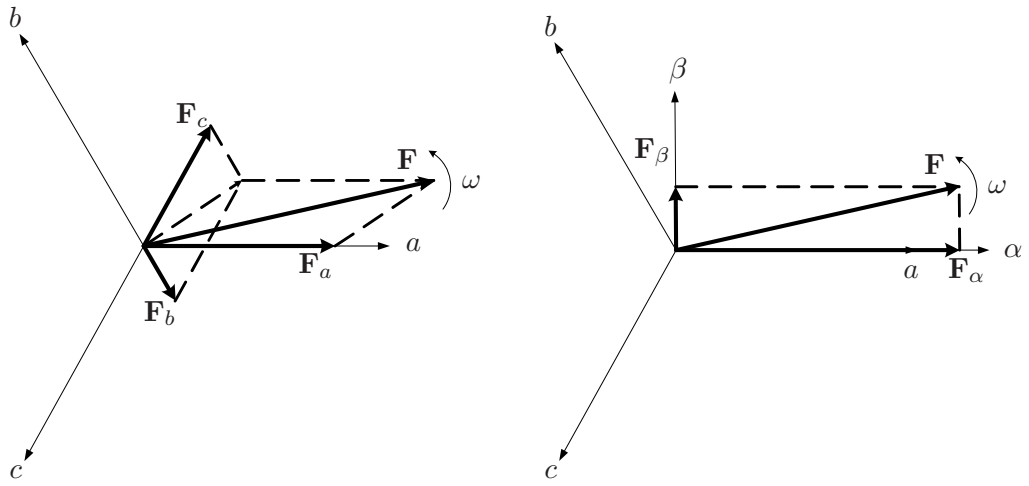
$$K = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & +\sin\left(\theta - \frac{2\pi}{3}\right) & +\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

Stationary Reference Frame Transformation If the arbitrary reference frame is set to be stationary in the a-b-c coordinates, i.e., the angular velocity $\omega_e = 0$ and the angle θ is constant, it is defined as stationary reference frame which is also referred to as the α-β reference frame. To simplify the discussion, the angle θ is also set to zero. Therefore, the α-β coordinates are defined in Figure 2.8(b) where the α axis is in phase with the a axis and the β axis leads

90° ahead to the α axis [1]. The transformation is given as

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}$$

This transformation is applied in Chapter 4.



(a) a-b-c coordinates (b) α-β coordinates

Figure 2.8: The stationary reference frame transformation. The α-β frame is fixed to the a-b-c frame. The α-axis is in phase with the a-axis.

2.1.4 Averaged VSC Model

In this section we relate the fundamental component of e_a, e_b, e_c to the amplitude m_a and phase δ of the SPWM modulating signals (2.5). We consider the eight possible switch configurations for g_a, g_b, g_c. When $g_a = g_b = g_c$ we have $e_a = e_b = e_c = 0$. When $g_a = 1, g_b = 1, g_c = 0$, the following equations can be obtained $e_a = e_b$, $e_a - e_c = v_{dc}$, and $e_a + e_b + e_c = 0$, which leads to $e_a = v_{dc}/3$, $e_b = v_{dc}/3$ and $e_c = -2v_{dc}/3$. After analyzing all 8 switching states, the relationship between e_a, e_b, e_c and v_{dc} is shown in Table 2.2.

Since the triangular carrier wave v_t has a constant amplitude and frequency, the states of the switches are determined by m_a and δ. Therefore, the average values of e_a, e_b, e_c can be derived in terms of m_a and δ based on the discussion above. In the experimental setup, the sampling frequency f_s is set to be twice of the carrier wave frequency f_t. This means that during half period of

(g_a, g_b, g_c)	e_a	e_b	e_c
(1,1,1)	0	0	0
(1,1,0)	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$	$-\frac{2}{3}v_{dc}$
(1,0,1)	$\frac{1}{3}v_{dc}$	$-\frac{2}{3}v_{dc}$	$\frac{1}{3}v_{dc}$
(1,0,0)	$\frac{2}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$
(0,1,1)	$-\frac{2}{3}v_{dc}$	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$
(0,1,0)	$-\frac{1}{3}v_{dc}$	$\frac{2}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$
(0,0,1)	$-\frac{1}{3}v_{dc}$	$-\frac{1}{3}v_{dc}$	$\frac{2}{3}v_{dc}$
(0,0,0)	0	0	0

Table 2.2: The relationship between gating signals g_a, g_b, g_c and the AC terminal voltages e_{abc}. Based on different IGBT states, the values of e_{abc} takes the value of $-\frac{2}{3}v_{dc}, -\frac{1}{3}v_{dc}, 0, \frac{1}{3}v_{dc}$, and $\frac{2}{3}v_{dc}$.

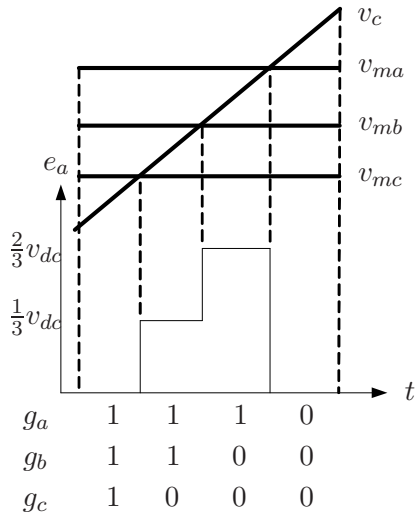


Figure 2.9: Values of e_a in half a switching period when $v_{ma} \geq v_{mb} \geq v_{mc}$. During half a switching period, there exist four sets of IGBT states and the values of AC terminal voltages varying with the IGBT states.

the carrier wave, the modulating signals are constant. In the case shown in Figure 2.9, the modulating signals are arranged as $v_{ma} > v_{mb} > v_{mc}$.

Therefore, four switching states are carried out during half period of v_c. Based on a simple geometric argument, the average values of the e_a, e_b, e_c over

the half period is

$$\begin{aligned} e_a &= \frac{v_{mc}+1}{2}\cdot 0 + \frac{v_{mb}-v_{mc}}{2}\cdot\frac{v_{dc}}{3} + \frac{v_{ma}-v_{mb}}{2}\cdot\frac{2v_{dc}}{3} \\ &= \frac{v_{dc}}{6}(2v_{ma}-v_{mb}-v_{mc}) \end{aligned}$$

$$\begin{aligned} e_b &= \frac{v_{mc}+1}{2}\cdot 0 + \frac{v_{mb}-v_{mc}}{2}\cdot\frac{v_{dc}}{3} - \frac{v_{ma}-v_{mb}}{2}\cdot\frac{v_{dc}}{3} \\ &= \frac{v_{dc}}{6}(-v_{ma}+2v_{mb}-v_{mc}) \end{aligned}$$

$$\begin{aligned} e_c &= \frac{v_{mc}+1}{2}\cdot 0 - \frac{v_{mb}-v_{mc}}{2}\cdot\frac{2v_{dc}}{3} - \frac{v_{ma}-v_{mb}}{2}\cdot\frac{v_{dc}}{3} \\ &= \frac{v_{dc}}{6}(-v_{ma}-v_{mb}+2v_{mc}) \end{aligned}$$

Substituting the expressions for modulating signals in Equation (2.5) into the above equations gives the average values for e_a, e_b, e_c:

$$\begin{aligned} e_a &= \frac{1}{2}v_{dc}m_a\cos(\omega t+\delta) \\ e_b &= \frac{1}{2}v_{dc}m_a\cos(\omega t+\delta-\frac{2\pi}{3}) \\ e_c &= \frac{1}{2}v_{dc}m_a\cos(\omega t+\delta+\frac{2\pi}{3}) \end{aligned} \tag{2.11}$$

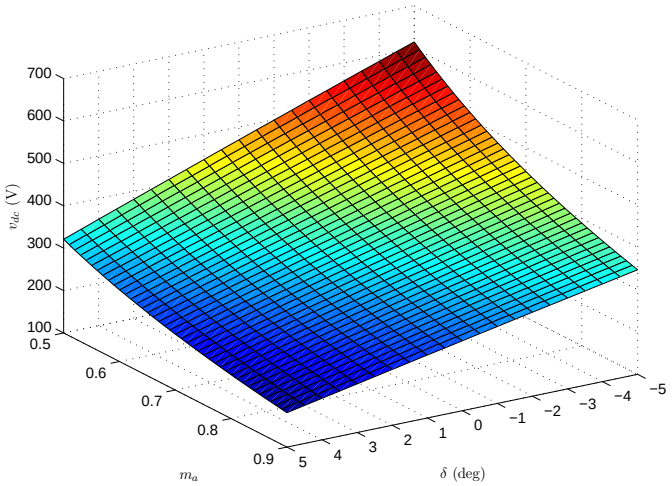
These expressions are valid for general values of v_{ma}, v_{mb}, and v_{mc} and a detailed proof is presented in [29].

If we substitute (2.11) into system model (2.2) and apply the synchronous reference frame transformation (2.8) we get

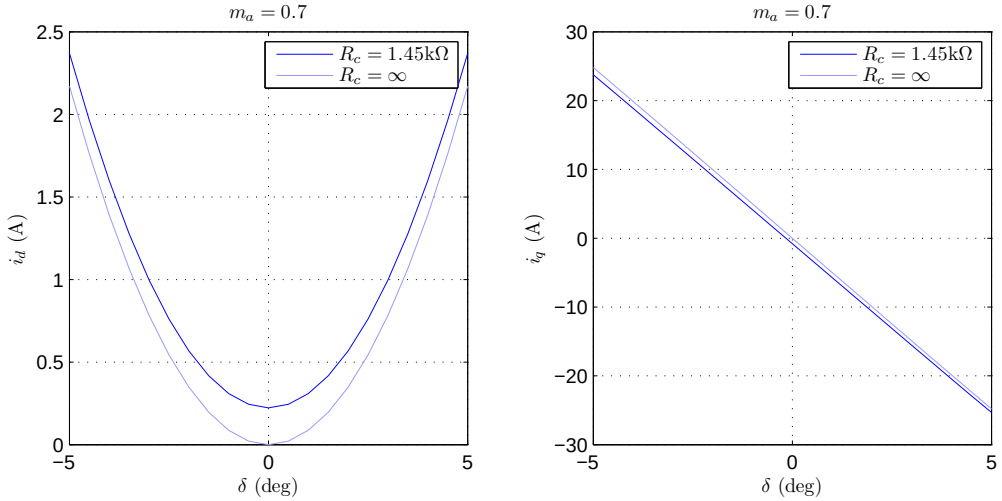
$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L}i_d + \omega i_q + \frac{v_d}{L} - \frac{1}{2L}v_{dc}m_a\cos\delta \\ \frac{di_q}{dt} &= -\omega i_d - \frac{R_s}{L}i_q + \frac{v_q}{L} - \frac{1}{2L}v_{dc}m_a\sin\delta \\ \frac{dv_{dc}}{dt} &= \frac{3(i_d m_a\cos\delta + i_q m_a\sin\delta)}{4C} - \frac{v_{dc}}{CR_c} \end{aligned} \tag{2.12}$$

Therefore, we obtain a bilinear model which shows a clear relationship between the actual modulating signals and the AC currents and DC voltage dynamics. It contains three states, i_d, i_q, v_{dc}, and two inputs, m_a, δ. This model will be

used in next section to derive a linearization-based nonlinear control algorithm. From the open-loop equilibrium relation, the relation between states and inputs is shown in Figure 2.10. From the figure, the DC voltage v_{dc} increases while either m_a or δ decreases. The current i_d, i_q have very little dependence on m_a and Figure 2.10(b) was generated with $m_a = 0.7$. If we take $R_c = \infty$, the values of i_d, i_q drop slightly and v_{dc} remains roughly unchanged.



(a) Equilibriums of v_{dc}



(b) Equilibriums of i_d and i_q

Figure 2.10: Equilibriums values of the system state. Since i_d and i_q have little dependence on m_a, only variation in δ is shown with $m_a = 0.7$. The light lines for currents were obtained for $R_c = \infty$. Since v_{dc} remains unchanged as we vary R_c, it is plotted for $R_c = 1.45$ kΩ.

2.2 Feedback Linearization-based Power Factor Control

This section derives a state feedback control which achieves power factor control. We remark that the system in Figure 2.1 contains no load which makes the need for control of power factor not obvious. However, the ability to track reactive current references desired properly is equivalent to achieving power factor control. Hence, we omit the load only to simplify presentation. In this section we use a feedback linearization technique to control the bilinear model (2.12) expressed in the d-q frame. To simplify the control law eventually, we renotate this model into the standard control affine form

$$\dot{x} = f(x) + g_1(x)u_1 + g_2(x)u_2 \tag{2.13}$$

where

$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} i_d \\ i_q \\ v_{dc}^2 \end{bmatrix}, \quad u = \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} \frac{v_{dc} m_a \cos\delta}{2L} \\ \frac{v_{dc} m_a \sin\delta}{2L} \end{bmatrix}$$

and

$$f(x) = \begin{bmatrix} -\frac{R_s}{L}x_1 + \omega x_2 + \frac{v_d}{L} \\ -\omega x_1 - \frac{R_s}{L}x_2 \\ -\frac{2x_3}{CR_c} \end{bmatrix}, \quad g_1(x) = \begin{bmatrix} -1 \\ 0 \\ \frac{3Lx_1}{C} \end{bmatrix}, \quad g_2(x) = \begin{bmatrix} 0 \\ -1 \\ \frac{3Lx_2}{C} \end{bmatrix}$$

2.2.1 Feedback Linearization

Feedback linearization is a control technique that linearizes a nonlinear system with state feedback in new state coordinates [15, 17]. The feedback linearizability of (2.12) has been verified in [29] and we review the details here. First of all, we recall the definition of Lie derivative of a smooth function $h(x)$ along the vector field $f(x)$ which is defined as

$$f(x) = f_1(x)\frac{\partial}{\partial x_1} + \cdots + f_n(x)\frac{\partial}{\partial x_n}$$

The Lie derivative is normally denoted as

$$L_f h = f(h)(x) = \sum_{i=1}^{n} f_i(x)\left(\frac{\partial h(x)}{\partial x_i}\right)$$

and its iterated form is defined as

$$L_{f_1}L_{f_2}L_{f_3}\dots L_{f_j}h(x) = f_1(f_2(f_3(\dots f_j(h)(x)\dots)))$$

The feedback linearizing coordinates are defined as

$$\begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} = \begin{bmatrix} \phi_1(x) \\ L_f\phi_1(x) \\ \phi_2(x) \end{bmatrix}$$

with the nonunique smooth functions ϕ_1 and ϕ_2 taken as

$$\begin{aligned} \phi_1 =& z_1 = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3 \\ \phi_2 =& z_3 = x_2 \end{aligned} \tag{2.14}$$

and

$$L_f\phi_1 = \frac{3R_c(v_d x_1 - R_s(x_1^2 + x_2^2)) - 2x_3}{2R_c} \tag{2.15}$$

Note that ϕ_1 is actually the total energy stored in the inductors and capacitors and ϕ_2 is the reactive current of the VSC. These coordinateare are well-defined on

$$\mathbf{S} = \{x \in \mathbb{R}^3 : x_1 < \frac{CR_cV_m}{2(CR_cR_s - L)}; x_3 > 4V_m^2\} \tag{2.16}$$

and the linearizing state feedback is defined by

$$w = \begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \begin{bmatrix} L_f^2\phi_1 \\ L_f\phi_2 \end{bmatrix} + F \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}$$

where

$$F = \begin{bmatrix} L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix} \tag{2.17}$$

and w denotes the auxiliary input. Therefore, the system dynamics in z-coordinates is

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \\ \dot{z}_3 \end{bmatrix} = \begin{bmatrix} L_f\phi_1 \\ L_f^2\phi_1 \\ L_f\phi_2 \end{bmatrix} + \begin{bmatrix} L_{g_1}\phi_1 & L_{g_2}\phi_1 \\ L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}$$

Since ϕ_1 was chosen such that $L_{g_1}\phi_1 = 0, L_{g_2}\phi_1 = 0$, the dynamics become

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \\ \dot{z}_3 \end{bmatrix} = \begin{bmatrix} L_f\phi_1 \\ L_f^2\phi_1 \\ L_f\phi_2 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ L_{g_1}L_f\phi_1 & L_{g_2}L_f\phi_1 \\ L_{g_1}\phi_2 & L_{g_2}\phi_2 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{2.18}$$

The condition for choosing ϕ_2 is that the matrix F is nonsingular on $\mathbf{S}$. Hence, the state feedback control is

$$u = \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = F^{-1} \begin{bmatrix} w_1 - L_f^2 \phi_1 \\ w_2 - L_f \phi_2 \end{bmatrix} \tag{2.19}$$

With these inputs, the system dynamics (2.18) becomes a controllable LTI system in the z-coordinates and input w:

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \\ \dot{z}_3 \end{bmatrix} = \begin{bmatrix} z_2 \\ w_1 \\ w_2 \end{bmatrix}$$

if we choose $w_1 = -k_1 z_1 - k_2 z_2, w_2 = -k_3 z_3$, then we have

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \\ \dot{z}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -k_1 & -k_2 & 0 \\ 0 & 0 & -k_3 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix}$$

with gains k_1, k_2, k_3 chosen for stability. From (2.19) the state feedback is presented as a function of states, system parameters, and control gains,shown as

$$\begin{aligned} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} =& F^{-1}(x) \begin{bmatrix} w_1 - L_f^2 \phi_1(x) \\ w_2 - L_f \phi_2(x) \end{bmatrix} \\ =& \begin{bmatrix} \frac{2CR_c}{3(2CR_c R_s x_1 - CR_c v_d - 2Lx_1)} & \frac{2(L - CR_c R_s)x_2}{2Lx_1 + CR_c(v_d - 2R_s x_1)} \\ 0 & -1 \end{bmatrix} \\ & \begin{bmatrix} -k_1 z_1 - k_2 z_2 - \frac{3(v_d^2 + v_d(\omega L x_2 - 3R_s x_1) + 2R_s^2(x_1^2 + x_2^2))}{2L} - \frac{2x_3}{CR_c^2} \\ -k_3 z_3 + \omega x_1 + \frac{R_s}{L} x_2 \end{bmatrix} \end{aligned} \tag{2.20}$$

with $z_1 = \frac{3}{4}L(x_1^2 + x_2^2) + \frac{1}{2}Cx_3, z_2 = (3R_c(v_d x_1 - R_s(x_1^2 + x_2^2)) - 2x_3)/(2R_c)$, and $z_3 = x_2$. If we assume the system is lossless, i.e., $R_s = 0$ and $R_c = \infty$, the control law is represented in a simpler form

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} \frac{2}{3v_d}(k_1 z_1 + k_2 z_2 + \frac{3(v_d^2 + v_d \omega L z_3)}{2L}) \\ k_3 z_3 - \omega x_1 \end{bmatrix}$$

2.2.2 Power Factor Control Using Feedback Linearization

In this section we explain how tracking of constant references i_q^* and v_{dc}^* can be obtained using the feedback linearizing control in the previous section.

The constant references have to be chosen inside the equilibrium set of the system (2.13) to ensure the states are able to converge to the references. The equilibrium set of a differential equation $\dot{x} = f(x,t)$ is defined as

$$\{x^* \in \mathbb{R}^n : f(x^*,t) = 0, \forall t\}$$

Based on this definition, we set the left hand side of system model (2.13) to be zero and shown as

$$\begin{aligned} 0 &= -\frac{R_s}{L}x_1^* + \omega x_2^* + \frac{v_d}{L} - \frac{e_d^*}{L} \\ 0 &= -\frac{R_s}{L}x_2^* - \omega x_1^* + \frac{v_q}{L} - \frac{e_q^*}{L} \\ 0 &= \frac{3(e_d^* x_1^* + e_q^* x_2^*)}{C} - \frac{2x_3^*}{CR_c} \end{aligned} \tag{2.21}$$

where x_1^*, x_2^*, x_3^* are the constant references of the states and e_d^*, e_q^* are corresponding constant inputs of the system. Note that v_d is constant and $v_q = 0$ since the AC voltage is balanced. By solving Equation (2.21) the references can be derived as

$$\begin{aligned} x_1^* =& \frac{R_s v_d - e_d^* R_s - e_q^* L w}{R_s^2 + L^2 w^2}, \\ x_2^* =& \frac{L(e_d^* - v_d)w - e_q^* R_s}{R_s^2 + L^2 w^2}, \\ x_3^* =& \frac{3R_c(e_d^* R_s v_d - e_d^{*2} R_s - e_d^{*2} R_s - e_q^* L v_d w)}{2(R_s^2 + L^2 w^2)}. \end{aligned} \tag{2.22}$$

With x_2^* and x_3^* given, we obtain x_1^* as a function of the system parameters and x_2^*, x_3^*.

$$x_1^* = \frac{v_d}{2R_s} \pm \sqrt{\frac{v_d^2}{4R_s^2} - x_2^{*2} - \frac{2x_3^*}{3R_s R_c}} \tag{2.23}$$

Note that i_d is practically very small since losses are relatively small. Therefore, the smaller value of (2.23) is the practically relevant solution of (2.23), i.e.,

$$x_1^* = \frac{v_d}{2R_s} - \sqrt{\frac{v_d^2}{4R_s^2} - x_2^{*2} - \frac{2x_3^*}{3R_s R_c}} \tag{2.24}$$

Now, we define the tacking errors of the system in (2.25). Two integral states are added to improve the robustness of steady-state tracking:

$$\begin{aligned} e_1(t) &= \int_0^t (z_1(\tau) - z_1^*(\tau))d\tau \\ e_2(t) &= z_1(t) - z_1^*(t) \\ e_3(t) &= \frac{dz_1(t)}{dt} \\ e_4(t) &= \int_0^t (z_3(\tau) - z_3^*(\tau))d\tau \\ e_5(t) &= z_3(t) - z_3^*(t) \end{aligned} \tag{2.25}$$

where $z_1^*(t), z_3^*(t)$ represent references $x_2^*(t), x_3^*(t)$ in z-coordinates and are denoted as

$$\begin{aligned} z_1^*(t) =& \frac{3}{4}L(x_1^{*2} + x_2^{*2}(t)) + \frac{1}{2}Cx_3^*(t) \\ =& \frac{3}{4}L\left(\left(\frac{v_d}{2R_s} - \sqrt{\frac{v_d^2}{4R_s^2} - x_2^{*2}(t) - \frac{2x_3^*(t)}{3R_sR_c}}\right)^2 + x_2^{*2}(t)\right) + \frac{1}{2}Cx_3^*(t), \\ =& \frac{3}{4}L\left(\frac{v_d^2}{2R_s^2} - \frac{2x_3^*(t)}{3R_sR_c} - \frac{v_d}{R_s}\sqrt{\frac{v_d^2}{4R_s^2} - x_2^{*2}(t) - \frac{2x_3^*(t)}{3R_sR_c}}\right) + \frac{1}{2}Cx_3^*(t), \\ z_3^*(t) =& x_2^*(t) \end{aligned} \tag{2.26}$$

and the corresponding error dynamics is derived as

$$\begin{aligned} \dot{e}_1 &= e_2 \\ \dot{e}_2 &= e_3 \\ \dot{e}_3 &= L_f^2\phi_1 + L_{g_1}L_f\phi_1 u_1 + L_{g_2}L_f\phi_1 u_2 - \ddot{z}_1^* \\ \dot{e}_4 &= e_5 \\ \dot{e}_5 &= L_f\phi_2 + L_{g_1}\phi_2 u_1 + L_{g_2}\phi_2 u_2 - \dot{z}_3^* \end{aligned}$$

By taking inputs u_1, u_2 as

$$\begin{aligned} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} =& F^{-1}(x)\begin{bmatrix} -k_1e_1 - k_2e_2 - k_3e_3 - L_f^2\phi_1 + \ddot{z}_1^* \\ -k_4e_4 - k_5e_5 - L_f\phi_2 + \dot{z}_3^* \end{bmatrix} \\ =& \begin{bmatrix} \frac{2CR_c}{3(2CR_cR_sx_1 - CR_cv_d - 2Lx_1)} & \frac{2(L - CR_cR_s)x_2}{2Lx_1 + CR_c(v_d - 2R_sx_1)} \\ 0 & -1 \end{bmatrix} \\ & \begin{bmatrix} -k_1e_1 - k_2e_2 - k_3e_3 - \frac{3(v_d^2 + v_d(\omega Lx_2 - 3R_sx_1) + 2R_s^2(x_1^2 + x_2^2))}{2L} - \frac{2x_3}{CR_c^2} \\ -k_4e_4 - k_5e_5 + \omega x_1 + \frac{R_s}{L}x_2 \end{bmatrix} \end{aligned} \tag{2.27}$$

with positive constant k_1, k_2, k_3, k_4, k_5, and $k_2k_3 - k_1 > 0$, it yields a stable error dynamics with controllable transient performance:

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \\ \dot{e}_4 \\ \dot{e}_5 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ -k_1 & -k_2 & -k_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -k_4 & -k_5 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \\ e_5 \end{bmatrix}.$$

Step Trajectories Derivation

In this section we derive piecewise smooth reference trajectories which provide asymptotic tracking of constant reference signals. The transition starts at time point t_0 and ends at time point t_1. The transition interval is defined as $\Delta t = t_1 - t_0$. In order to provide a smooth transition, the trajectories are taken as polynomials:

$$z_1^*(t) = \begin{cases} z_1^*(t_0) & : \quad t \le t_0 \\ z_1^*(t - t_0) & : \quad t_0 < t < t_1 \\ z_1^*(t_1) & : \quad t \ge t_1 \end{cases} \qquad z_3^*(t) = \begin{cases} z_3^*(t_0) & : \quad t \le t_0 \\ z_3^*(t - t_0) & : \quad t_0 < t < t_1 \\ z_3^*(t_1) & : \quad t \ge t_1 \end{cases} \tag{2.28}$$

where

$$\begin{aligned} z_1^*(t_0) =& \frac{3}{4}L\left(\frac{v_d^2}{2R_s^2} - \frac{2x_3^*(t_0)}{3R_sR_c} - \frac{v_d}{R_s}\sqrt{\frac{v_d^2}{4R_s^2} - x_2^{*2}(t_0) - \frac{2x_3^*(t_0)}{3R_sR_c}}\right) \\ &+ \frac{1}{2}Cx_3^*(t_0), \\ z_1^*(t_1) =& \frac{3}{4}L\left(\frac{v_d^2}{2R_s^2} - \frac{2x_3^*(t_1)}{3R_sR_c} - \frac{v_d}{R_s}\sqrt{\frac{v_d^2}{4R_s^2} - x_2^{*2}(t_1) - \frac{2x_3^*(t_1)}{3R_sR_c}}\right) \\ &+ \frac{1}{2}Cx_3^*(t_1), \\ z_1^*(t - t_0) =& z_1^*(t_0) + \left(-10\frac{z_1^*(t_0) - z_1^*(t_1)}{\Delta t^3}\right)(t - t_0)^3 \\ &+ \left(15\frac{z_1^*(t_0) - z_1^*(t_1)}{\Delta t^4}\right)(t - t_0)^4 + \left(-6\frac{z_1^*(t_0) - z_1^*(t_1)}{\Delta t^5}\right)(t - t_0)^5 \end{aligned}$$

and

$$\begin{aligned} z_3^*(t_0) =& x_2^*(t_0), \\ z_3^*(t_1) =& x_2^*(t_1), \\ z_3^*(t - t_0) =& z_3^*(t_0) + \left(-3\frac{z_3^*(t_0) - z_3^*(t_1)}{\Delta t^2}\right)(t - t_0)^2 + \left(2\frac{z_3^*(t_0) - z_3^*(t_1)}{\Delta t^3}\right)(t - t_0)^3. \end{aligned}$$

2.2.3 Simulation Results

We set the steady-state trajectories of i_q, v_{dc} before the transition as $i_q^*(t_0) = -5$ A, $v_{dc}^*(t_0) = 150$ V and after transition as $i_q^*(t_1) = 5$ A, $v_{dc}^*(t_1) = 200$ V. The value of i_d^* can be calculated as discussed in previous section as: $i_d^*(t_0) = 0.31$ A before transition and $i_d^*(t_1) = 0.45$ A after transition. Thus, we remark that before and after the transition z_1^*, z_3^* have the following values.

$$\begin{aligned}
z_1^*(t_0) =& \frac{3}{4}L\left(i_d^{*2}(t_0) + i_q^{*2}(t_0)\right) + \frac{1}{2}Cv_{dc}^{*2}(t_0) = 12.4126,\\
z_1^*(t_1) =& \frac{3}{4}L\left(i_d^{*2}(t_1) + i_q^{*2}(t_1)\right) + \frac{1}{2}Cv_{dc}^{*2}(t_1) = 22.0378,\\
z_3^*(t_0) =& i_q^*(t_0) = -5,\\
z_3^*(t_1) =& i_q^*(t_1) = 5
\end{aligned}$$

where t_0 is the start time point of the transition and t_1 is the end time point of the transition. To avoid large inrush currents, the transition time Δt is chosen to be 100 ms. Based on the discussion in the last part of previous section, the tracking trajectories are designed and shown in Figure 2.11.

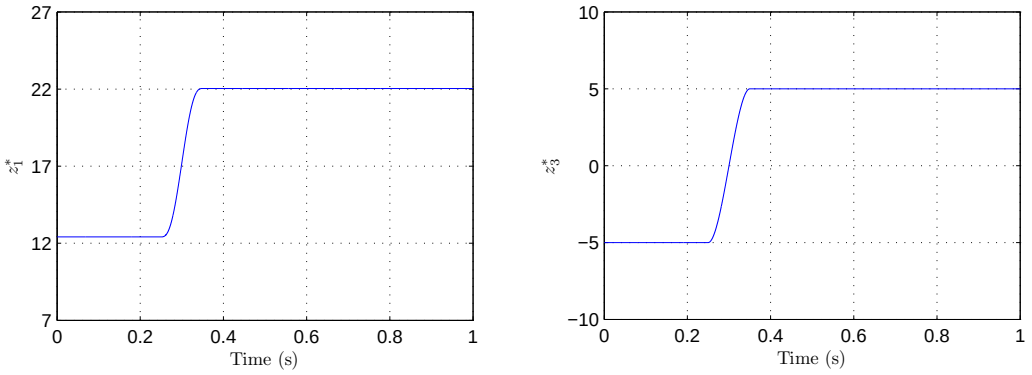


Figure 2.11: Tracking Trajectories

We verify the feedback linearization-based controller via simulation to track the desired trajectories given in Figure 2.11. In order to avoid large transient overshoots at the beginning of the simulation, the initial states of the system are set at $(x_1, x_2, x_3) = (0, 0, 150)$. The feedback gains are chosen as $k_1 = 5 \times 10^4\ s^{-3}, k_2 = 1.2 \times 10^8\ s^{-2}, k_3 = 10^4\ s^{-1}, k_4 = 10^4\ s^{-2}, k_5 = 5.6 \times 10^3\ s^{-1}$. Figure 2.12 shows the simulation results based on a mathematical model which

is implemented in a S-function and governed by (2.12). Figure 2.13 shows the simulation results based on a more realistic model which contains a three-phase VSC block from the SimPowerSystems library. Both plants in simulation adopt identical parameters identified from the experimental test stand (see Table 2.1). The results in Figure 2.12 are approximately equivalent to the average values of the results in Figure 2.13.

Both Figure 2.12 and Figure 2.13 indicate that the linearization-based control provides good constant reference tracking. Besides the tracking performance, another important criterion of the control algorithm is the robustness. We take a twenty percent uncertainty for each model parameter $R_s, R_c, L, C$and investigate the effect of model error in simulation. The results indicate that only C has a noticeable effect on performance and that tuning the control gains reduces the steady state error to a negligible amount.

2.3 Summary

In this chapter we have derived a model (2.12) for the three-phase VSC system in the synchronous reference frame. The parameters of the model are identified for the test stand considered. We describe the Sine Pulse Width Modulation (SPWM) scheme used and derive the relation between modulation parameters, gating signals, and VSC AC terminal voltage. We present a nonlinear control method also considered in [29] and modify it to compensate for non-zero d-axis current at equilibrium. The simulation results of the scheme are presented and robustness verified.

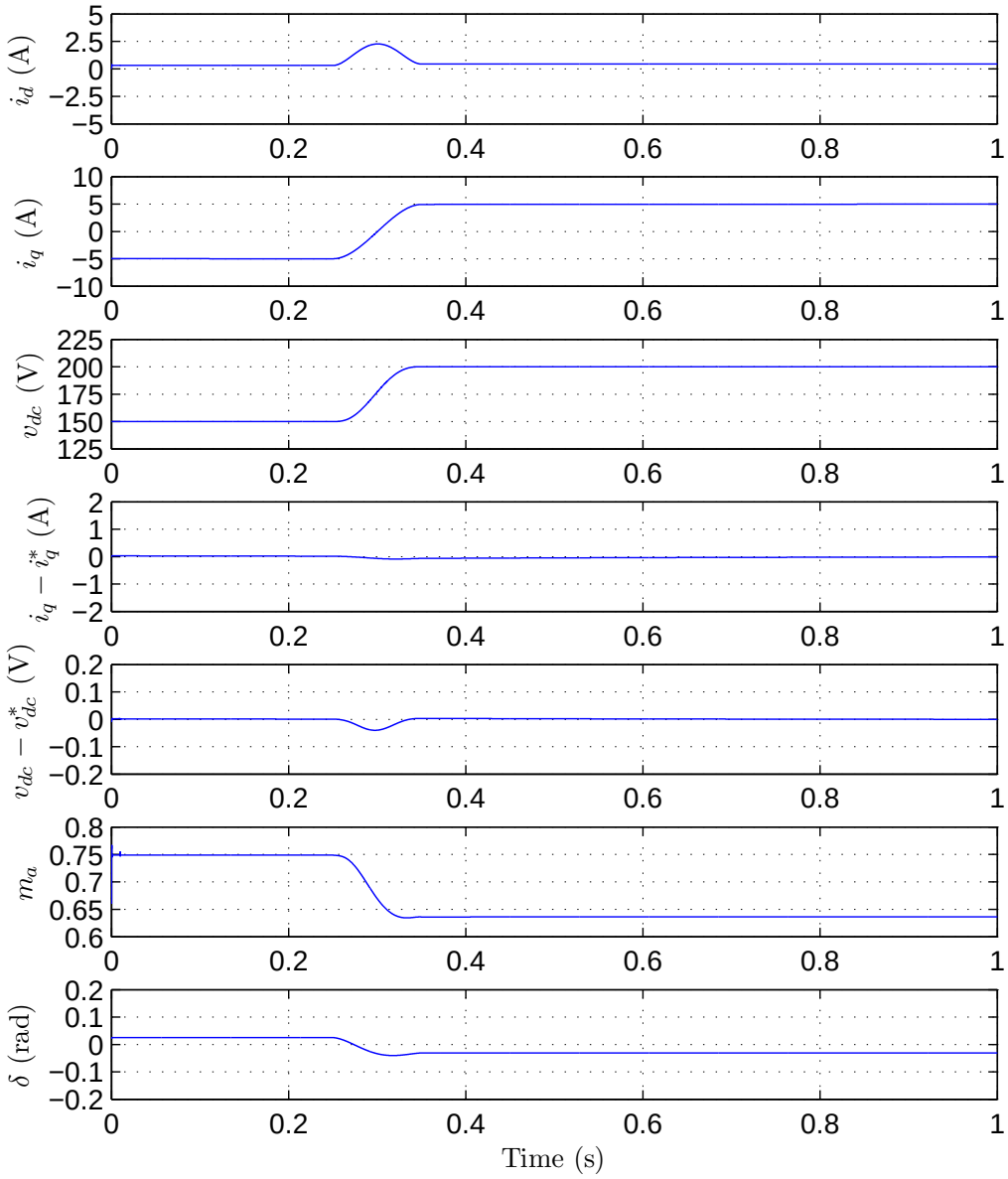


Figure 2.12: Simulation results of the linearization-based control algorithm with an averaged model. The plant is a S-function which presents the model given as Equation (2.12).

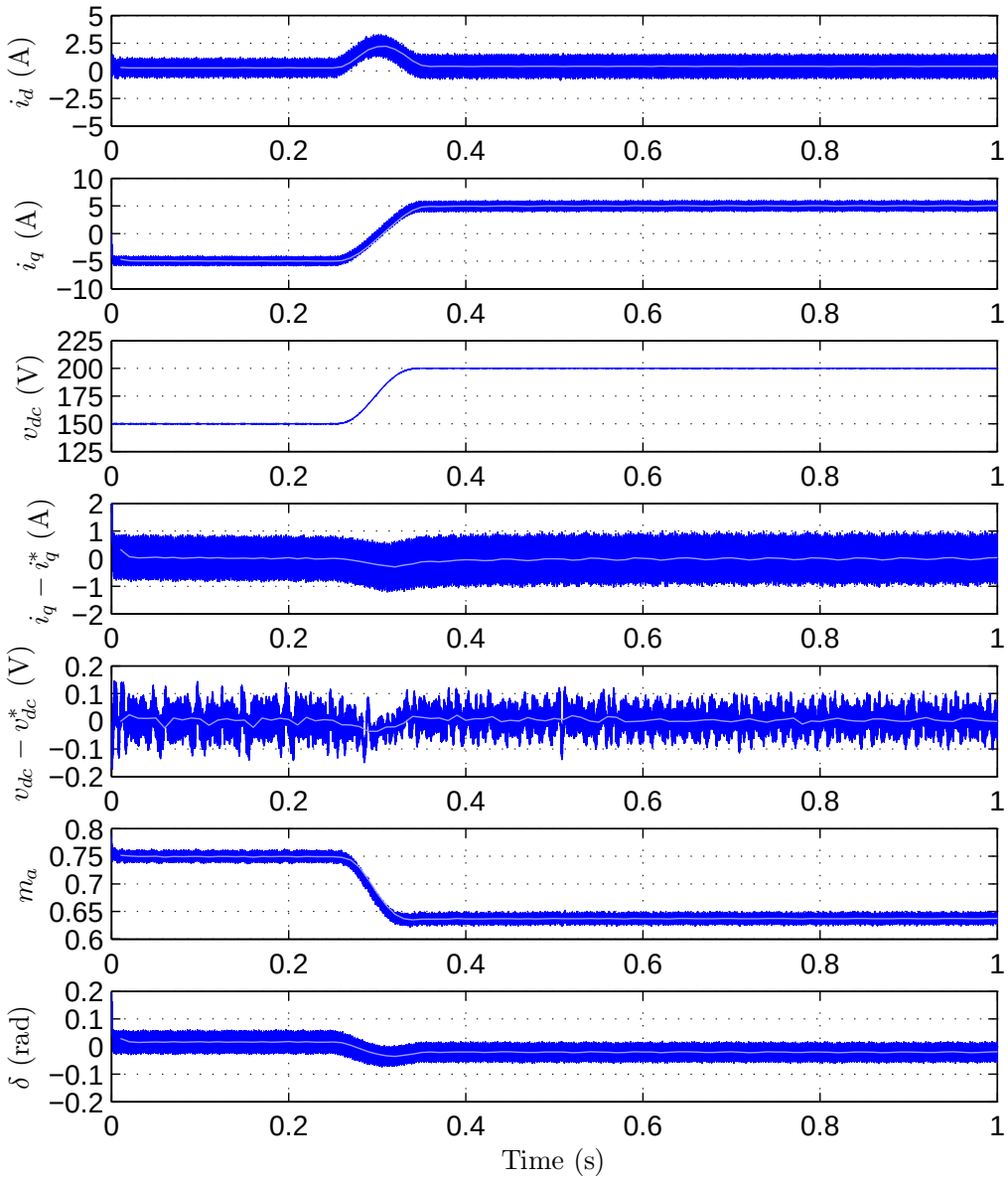


Figure 2.13: Simulation results of the linearization-based control algorithm with a switched model. The plant of the simulation contains a VSC-based power electronics block from the Simulink SimPowerSystems library using parameters given in Table 2.1. The lighter lines are the averaged values of the results. The switching frequency is $f_t = 5kHz$. In order to provide sufficient PWM pulses in each switching period, the simulation frequency is $500kHz$, which means there are one hundred integration steps in each switching period.

Chapter 3

Experimental Verification

In this chapter, the feedback linearization-based control algorithm to achieve power factor control is implemented on an actual experimental test stand at the Applied Nonlinear Control Lab (ANCL), University of Alberta. All the elements of the setup and their interconnections are introduced in detail. A number of components were built to enable the test stand's operation; a testing procedure for these components is described. The experimental results of the control are presented and compared with the traditional vector control scheme.

3.1 Experimental Test Stand

Figure 3.1 shows the complete experiment setup. The main components include a Semiteach power electronics teaching module, a dSPACE control system (connector panel is shown), a connector box to the three-phase power source, a three-phase variable transformer, a three-phase choke, a ± 15 V DC supply, two sensor boards, two level shifting boards, and a host computer which is used for software development and monitoring the experiment. This section describes these components in detail.

3.1.1 Semiteach Power Electronics Teaching Module

The Semiteach module is manufactured by SEMIKRON International GmbH. As shown in Figure 3.2, it is covered by a transparent enclosure which provides safety to the operator and a view of the internal components for learning purposes. The module includes an uncontrolled rectifier (which is not used

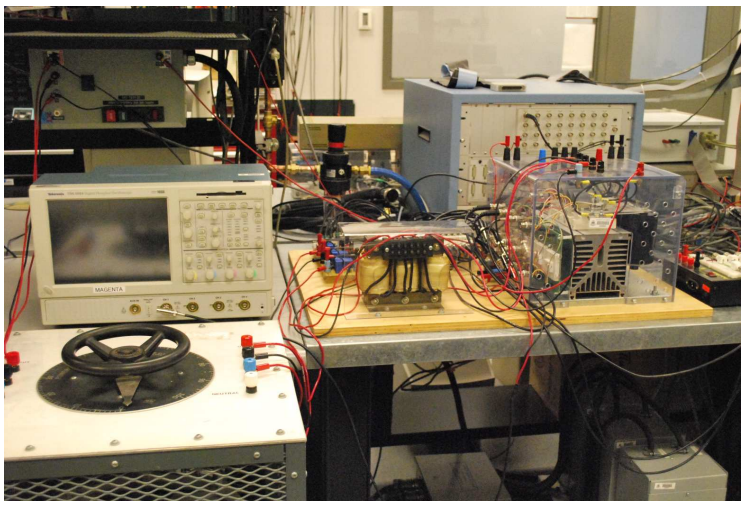


Figure 3.1: Main components of the experimental test stand. The figure shows the Semiteach module, the connector panel of the dSPACE control system, the connector box to the three-phase power source, the three-phase variable transformer, the three-phase choke, and two sensor boards.

in this experiment), a three-phase IGBT-based VSC, drivers for the IGBTs, DC bank capacitors, a cooling system, and external banana/BNC connectors. Unfortunately, there are no voltage or current sensors in the Semiteach. To measure voltage and current required by the the controller, external sensor boards were constructed and will be introduced later.

IGBT modules

The core part of the Semiteach module is a VSC unit which contains three IGBT modules in parallel. Each IGBT module, model number is SKM50GB-123D, becomes a leg of the VSC and includes two IGBTs in series with free-wheeling diodes. Figure 3.3 shows the actual IGBT module and equivalent circuit. The top IGBT collector is connected at terminal 3 which is wired to the positive terminal of the DC side and the bottom IGBT emitter is connected at terminal 2 which is wired to the negative terminal of the DC side. The mid-point of two IGBTs is labeled 1 and connected to the AC terminal. The IGBTs are forced on by a 15 V voltage between the Gates (terminals 4 and 6, respectively) and the associated Emitters (terminals 5 and 7, respectively), and forced off by a -15 V voltage. These voltages are delivered by the IGBT driver

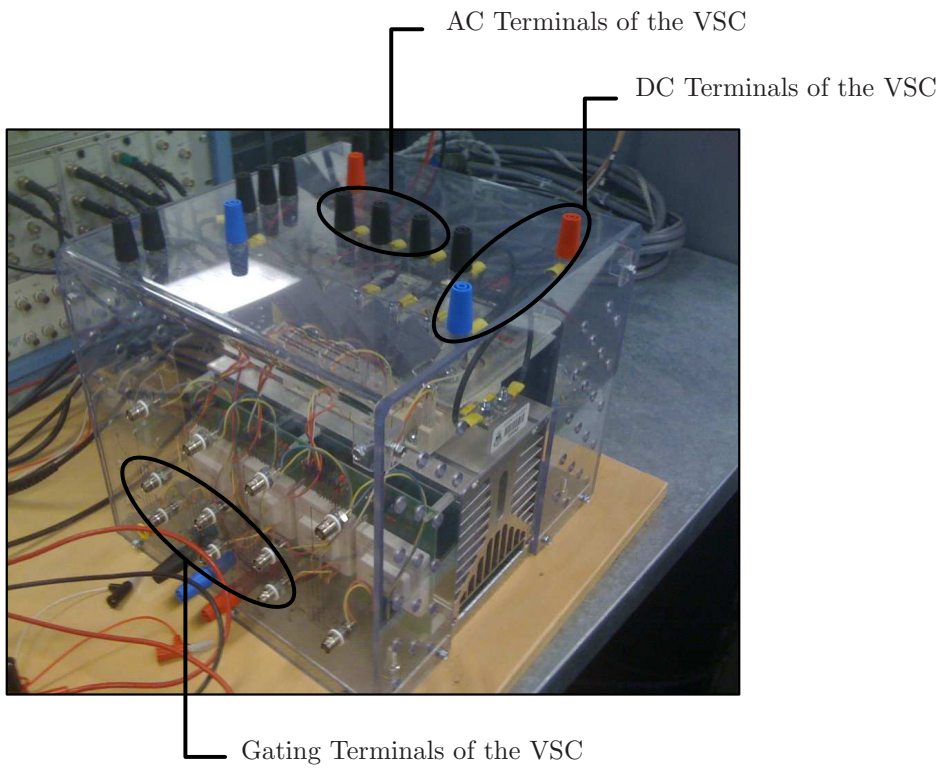


Figure 3.2: SEMIKRON Semiteach power electronics teaching module. The polarity of the DC terminals is denoted with color. The red terminal is anode and the black one is cathode.

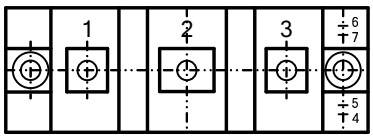
SKHI22AR which will be introduced next. Due to the physical constrains of the devices, the maximum AC current of the VSC is 30 A and the maximum DC voltage is 750 V. To keep within these current and voltage ranges, the system is monitored by the controller and the six IGBTs are forced off before the limits are reached.

IGBT Drivers

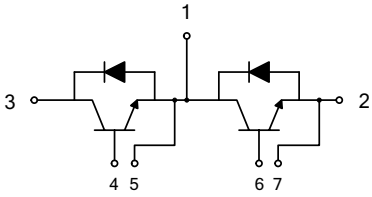
Each IGBT module is driven by one IGBT driver SKHI22AR, shown in Figure 3.4, which has two inverted PWM signals as inputs. The maximum switching frequency of the PWM inputs is 50 kHz. The drive is able to provide a 3.8 μs dead-time for each IGBT module, thus there is no need to implement dead-time in control algorithm. The detailed circuit diagram can be found in [27].

The driver is designed to amplify the PWM signals and deliver high peak

(a) SEMIKRON IGBT module



(b) Top view of the module



(c) Equivalent circuit

Figure 3.3: SEMIKRON IGBT module SKM50GB123D. The actual connections are labeled in the top view and the corresponding internal circuit is shown in the bottom. Each module includes two pairs of IGBT and free-wheeling diode.

current during the signal transition periods to trigger the IGBTs. The high and low input threshold voltages are 11.7 V and 5.5 V, respectively. This means the driver takes any input voltage higher than 11.7 V as "HIGH" and delivers a +15 V voltage to close the IGBT, and any input voltage lower than 5.5 V as "LOW" and delivers a −15 V voltage to open the IGBT. These two levels are important for designing the PWM signal output from the controller.

Another function of this driver is to detect short-circuits and under-voltage to its DC power. The driver responds to these situations by forcing both IGBTs open. The detection is implemented by monitoring the voltage drop between collector and emitter of an IGBT (v_{ce}). Since v_{ce} significantly increases when the current flows through the IGBT becomes very high, a fault is detected based on an significant increase of the v_{ce}. Therefore, not only the short-

Figure 3.4: IGBT driver SKHI22AR. Each driver drives one IGBT module and provides a fault detection.

circuit situation, but also large transient current can trigger the protection and generate an error signal to open the IGBTs. This error signal is negative logic, which means it stays high (15 V) when there is no error occurs and low (0 V) when an error is detected. It can be reset by setting both gate signals to "LOW". To further reduce the chance of equipment damage, all three error signals are also monitored by the dSPACE controller and six null gating signals are generated when errors are detected. In addition, the driver interfaces and isolates the PWM signal generation from high voltage.

Other Components

Two filtering capacitors are connected in series at the DC terminal of the VSC. Their individual capacitance is 2200 μF, thus the equivalent capacitance of the DC bus is 1100 μF. Since the capacitors are polarized, the polarity of the DC terminal should be respected to avoid capacitor explosion.

Dissipating the power losses generated in the VSC is critical to its operation. A fan and heat sink are provided in the Semiteach to control device temperature. To protect the devices from being damaged by overheating, a thermal switch is connected in series with the DC power supply of the IGBT drivers. In this configuration, the thermal switch will shut down the drivers, which leads to a null voltage generated by the drivers and opens all six IGBTs. The protection occurs when heat sink temperature is higher than 71° C.

3.1.2 dSPACE Control System

The dSPACE system is a real-time controller which provides rapid prototyping functionality. Although controllers can be handcoded in C using a dSPACE environment, it is often more convenient to use MATLAB/Simulink to accelerate development and facilitate controller testing in a simulation environment. dSPACE provides an interface development software called ControlDesk which can be used to monitor any signal in the Simulink, change parameters of the Simulink model, and save the experimental data. The test stand uses a modular dSPACE system which has an extremely wide range of high performance I/O which can be used in various configurations for different applications.

The dSPACE system is housed in a PX10 expansion box which contains one DS1005 processor board, three DS2001 high-speed analog-to-digital (A/D) boards, one DS2103 multichannel digital-to-analog (D/A) board, one DS3002 encoder interface board, one DS5101 digital waveform output board, and one DS814 link board. There is a companion DS817 link board installed in the host computer. The function of each board used in the experiment is provided in this section and further detailed technical information is in [4]. The interconnection of the boards is show in Figure 3.5.

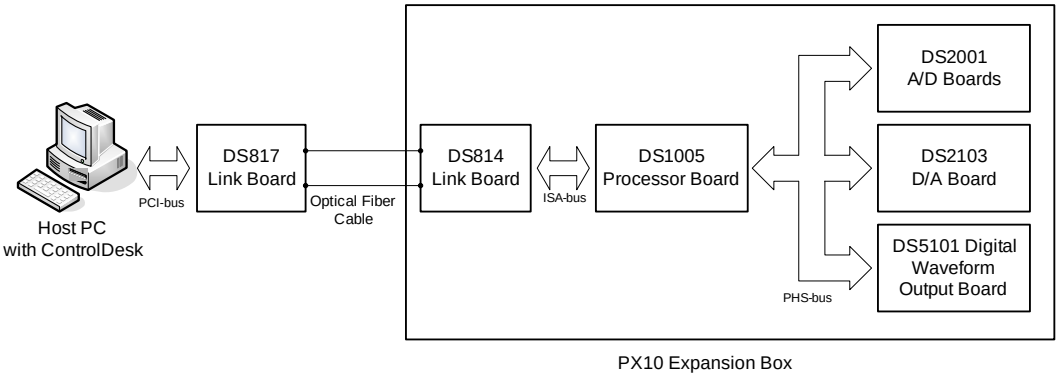


Figure 3.5: Interconnections of dSPACE boards. The I/O boards and processor board communicate with each other via PHS-bus and the processor board talks with DS814 link board via ISA-bus. An optical fiber cable is used to interface two link boards and enables data commutation.

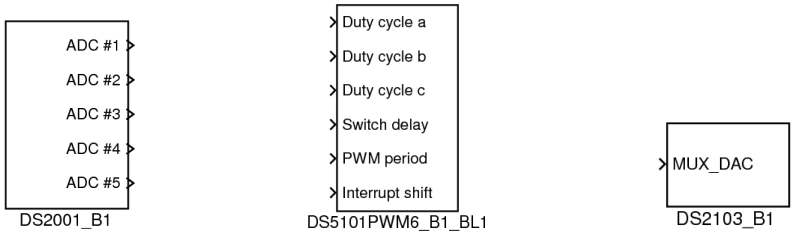
All the boards in the expansion box are installed on ISA-bus which pro-

vides power and a data connection between the DS1005 and DS814. In order to provide fast communication between the DS1005 and the I/O boards, a dedicated PHS-bus is provided which is not connected to the DS814. In addition, fast and convenient I/O access to the boards are provided by an external connector panel. Figure 3.6(a) shows the expansion box and Figure 3.6(b) shows the connector panel. dSPACE provides a library of MATLAB/Simulink blocks to interface with its boards. The blocks used in the experiment are shown in Figure 3.7. With this feature, the process of input data collection and output signal generation becomes straightforward.

(a) Expansion box of the dSPACE

(b) Connector panel of the dSPACE

Figure 3.6: dSPACE Expansion Box and Connector Panel. The expansion box provides ten ISA slots and most dSPACE boards are installed in it. The connector panel provides convenient connections to I/O boards.



(a) DS2001

(b) DS5101

(c) DS2103

Figure 3.7: Simulink blocks of the I/O boards.

DS2001 Analog-to-Digital Board

The function of the DS2001 A/D board is to digitize analog input signals with 16-bit resolution. Each board provides five parallel A/D channels. Since the control algorithm requires five measurements, i.e., v_{ab}, v_{bc}, i_a, i_b, and v_{dc}, and three error signals generated by the IGBT drivers, two boards and eight channels in total are used. The input voltage range of the board is programable between ± 5 V and ± 10 V for each channel individually. In our experiment, the ranges of all eight channels are set to ± 10 V. Figure 3.7(a) is the Simulink block of DS2001 board. This block allows the input voltage range to be specified, and the five block outputs are scaled to ± 1.

DS2103 Multichannel Digital-to-Analog Board

This board provides 32 D/A channels. The output voltage range is programable between ± 5 V and ± 10 V for each channel individually and set to ± 10 V in our experiment. One channel is used to deliver a reset signal to stop DS5101 from generating PWM signals when an error is detected. Figure 3.7(c) shows a single channel Simulink block for the board. The channel number can be specified in block parameter. The range of the output signal is scaled from ± 1 to ± 5 V or ± 10 V.

DS5101 Digital Waveform Output Board

The DS5101 digital waveform output board is designed to generate complex high-frequency digital signals. It is perfect choice for generating PWM signals and is capable of generating single-phase PWM signals, three-phase PWM signals, and three-phase inverted and non-inverted PWM signals. In our experiment, the board is used to generate three-phase inverted and non-inverted PWM signals. On the connector panel, channel 1, 3, and 5 deliver non-inverted signals and channel 2, 4, and 6 deliver inverted signals. The generated PWM signals has a Transistor-Transistor logic (TTL) voltage level, which means the high level of the signals is greater than 3.3 V and the low level is less than 0.35 V [13]. To be compatible with the IGBT drivers, a voltage level shifting

board is designed and built; it is introduced later in this section. Besides the output terminals, an external reset terminal is provided with TTL input voltage levels. When this signal is set to high and held for 100 ns, signal generation outputs are zero.

Figure 3.7(c) shows the Simulink block of DS5101 in the mode of three-phase inverted and non-inverted PWM signal generation. Six inputs need to be specified: the first three inputs are the duty cycles (using $0-1$ to map $0\%-100\%$) of the PWM signals. The other three are switch delay, PWM period, and interrupt shift of the signals. Since the IGBT drivers add dead-time into driving signals, the switch delay can be set to 0. The switching frequency of IGBTs is chosen as 5 kHz in the experiment. The interrupt shifting depends on PWM period and must be in the range 0.25 μs $\sim$ $(0.5 * 200 - 0.25)$ μs. This signal determines where the signal generation is stopped by reset signal. In our test stand it is set to 0.25 μs.

Other Boards

Besides the boards discussed above, there are DS1005 processor board, DS814 and DS817 link boards are integrated in the system. The DS1005 processor board performs the controller calculations in real-time. This board uses a sampling frequency of 10 kHz. The DS814 and DS817 link boards provide an interface to connect the expansion box to the host PC and enable the communication between them. DS814 is installed on an ISA slot in expansion box and DS817 is installed on a PCI slot in host PC. They are connected by a fiber-optic cable.

3.1.3 Voltage-Current Sensor Boards

Since the Semiteach module does not provide any voltage-current measurement, the system state required by the control algorithm is obtained using sensor boards. These boards are designed by Dr. Yunwei Li and built in ANCL. Each board provides two channels of voltage measurements and three channels of current measurements. The boards are powered by $\pm$15 V DC voltages. The boards can measure current in the range $\pm$50 A and voltage

in the range ±500 V. Since the board outputs are constrained to ±10 V to be compatible with DS2001, the current measurements need to be scaled by a factor of 5 and the voltage measurements by a factor of 10. Board#1 is connected between the transformer and the reactor to measure i_a, i_b, v_{ab}, and v_{bc}. Board#2 is connected at the DC terminal of the VSC to measure v_{dc}. Figure 3.8 shows the actual setup of the boards.

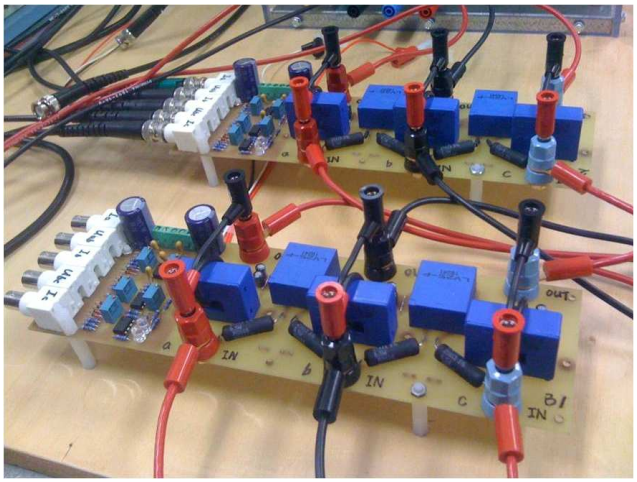


Figure 3.8: Voltage current sensor boards. Each board provides three channels of current measurement and two channels of voltage measurement.

The figure shows that the connectors can be identified via colors. Each of these connectors are actually a combination of two, an upper banana connector and a lower binding post. The binding posts denote phase a, b, and c of the power line by red, black, and blue, respectively. The banana connectors denote the direction of the current measurement. The current measurement is defined as positive when the current flows from the red banana connector to the black banana connector. The measurements of the boards are delivered by standard 50 Ω BNC connectors and labeled with corresponding channel.

Voltage Sensors

The voltage is sensed by voltage transducer LV25-P which is manufactured by LEM Components and shown in Figure 3.9. It is able to measure any DC, AC, or pulsed voltage with nominal value between 10 V – 500 V and provide

galvanic isolation between the primary and secondary circuits.

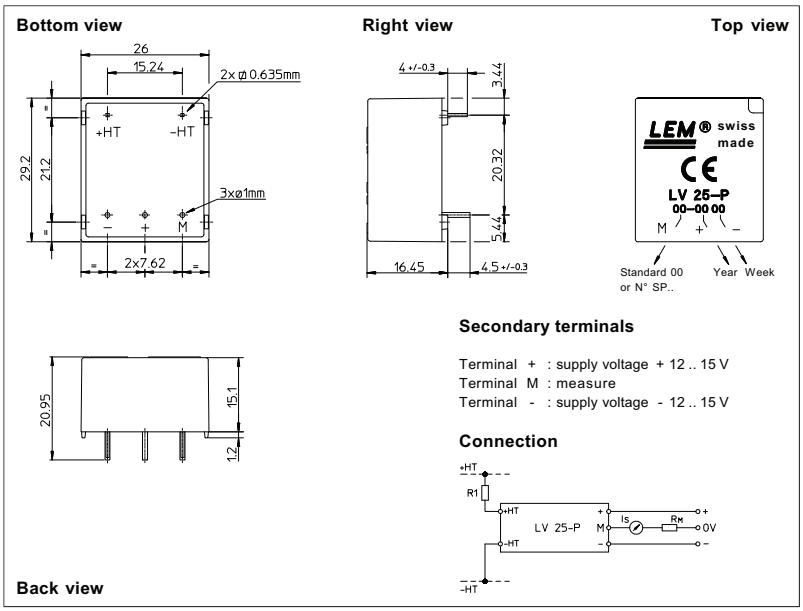


Figure 3.9: LEM voltage transducer LV25-P. The device is powered by ±15 V DC voltage. The voltage signal to be measured should be applied across terminal "+HT" and "−HT". The measurement signal is delivered from terminal "M".

For measuring voltage, the input is connected to the primary terminals "+HT" and "-HT", and the voltage measurement from terminal "M" is positive when the voltage is applied on terminal "+HT". The primary current I_p which flows into the primary side of the component should be in the nominal range of -10 mA $\sim +10$ mA. In order to achieve this requirement, an external resistor R_1 is connected in series with the primary circuit of the transducer as shown in fundamental operating circuit. Therefore, the ratio of maximum input voltage and maximum input current, $50k\ \Omega$, is selected for R_1. The measure current I_s is rated at 25 mA, with a measuring resistor R_M, this measurement can be transformed to voltage and delivered to the board's output terminal. R_M should be between 100 $\Omega \sim 350\ \Omega$ when the maximum absolute primary current is ±10 mA and is picked as 200 Ω in the actual boards.

Current Sensors

The current is measured by current transducer LA55-P which is manufactured by LEM Components and shown in Figure 3.10. It is capable to measure any DC, AC, or pulsed current whose nominal value is between -50 A $\sim +50$ A and provide galvanic isolation between the primary and secondary circuits.

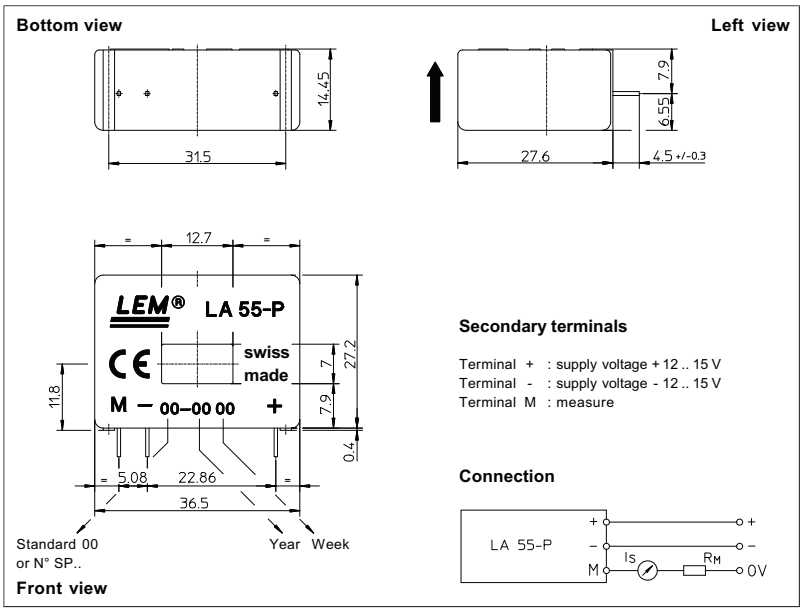


Figure 3.10: LEM current transducer LA55-P. Similar with LV25-P, the device is powered by ± 15 V DC voltage and the measurement signal is delivered from terminal "M". The current signal to be measured should be arranged to flow though the hole of the unit.

Since the Hall Effect is used to measure the current, wires which are carrying the current should be mounted through the primary hole of the component. To achieve best performance, single wire is used and wound over the top edge of the unit. The measurement I_s is positive when the current flows in the direction of the arrow which is printed on the top of the device and has a nominal RMS value as 50 mA. With a measuring resistor R_M, a proportional voltage is developed and delivered to board output terminal. R_M should be between 50 $\Omega \sim 160$ Ω when the maximum absolute value of the input current is ± 50 A. In the actual boards, R_M is picked as 100 Ω.

Board Testing

To test the performance of the boards, they are connected with a three-phase AC power supply and a resistive load. The power supply generates 120 V/60 Hz AC voltages to the load which provides a approximately 10.4 Ω resistance for each phase. Therefore, the phase currents should have sinusoidal waveform with 16.3 A amplitude and the phase voltages should have a sinusoidal waveform with 196.7 V peak voltage. Since the measurements of the two boards are identical, only the results of board one are shown in Figure 3.11. We took $\tilde{v}_a = v_a - 10.4 i_a$ which can be treated as a rough measurement error of phase a. Since our power supply is not exactly balanced, the three-phase resistance is not balanced, the value of resistance is not accurate, and the sensors have measurement errors, our $\tilde{v}_a$ is not zero. However, it is relatively small with respect to phase voltage v_a and negligible. Therefore, the sensor boards are functional and valid for operating.

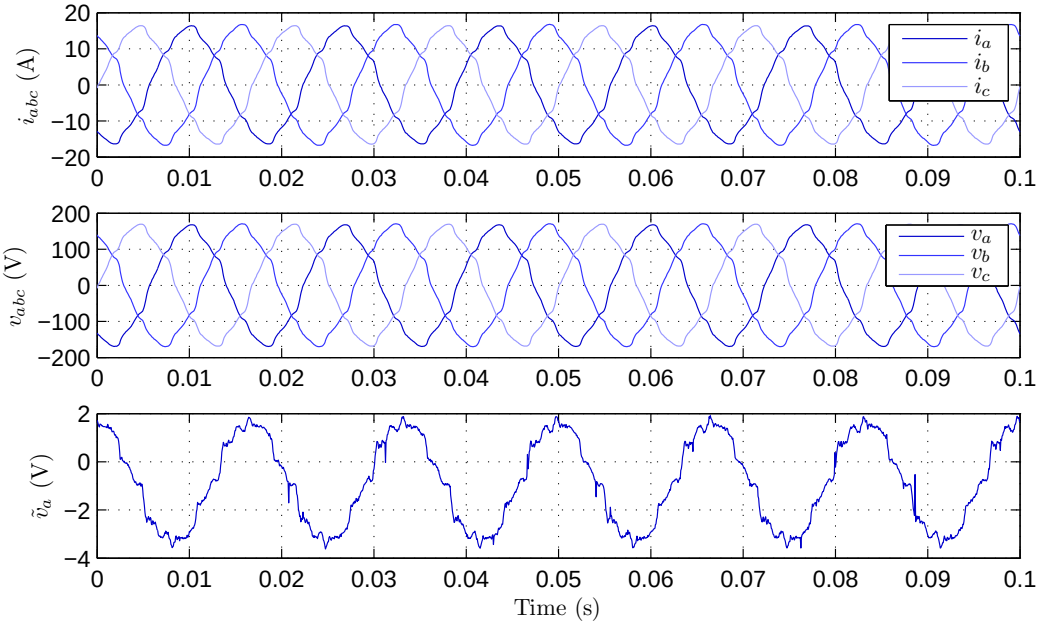
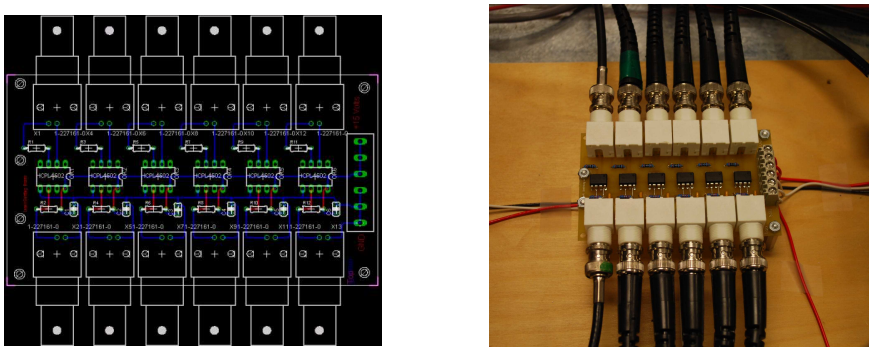


Figure 3.11: Testing results of the sensor board. The three-phase voltages were applied on the resistive load and the results fulfill our expectation. The voltage and current measurements are notated with different color depth for phase a (dark), b (medium), and c (light).

3.1.4 Level Shifting Boards

The DS5101 board is only able to generate TTL output, on the other hand, the VSC requires at least 11.7 V voltage at gates to close the IGBTs. Therefore, a level shifting board is designed and built. The EAGLE layout editor is used to design the printed circuit board. The board includes six identical channels and is power by +15 V DC voltage. Figure 3.12 show the layout and actual setup of the level shifting board. The key component of the board is



(a) EAGLE layout of the level shifting board

(b) Actual level shifting board

Figure 3.12: Level shifting board. The board contains six identical channels. Each channel is consisted of two BNC connectors, a HCPL-4504 chip, two metal film resistors, and one ceramic capacitor.

the HCPL-4504 chip in each channel. It needs to be powered by +15 V at terminal 8 and grounded at terminal 5. Each HCPL-4504 contains a GaAsP LED which is optically coupled to an integrated high gain photodetector with an insolating layer between them. The schematic diagram of the device is shown in Figure 3.12(a) and Figure 3.12(b) indicates the first channel of the board. The chip uses negative logic. When a TTL high level voltage is applied on terminal 2 of the chip, the LED is turned on, then the optically coupled photodetector starts conducting and turns on the transistor. Thus, the chip pin 6 is shorted with pin 5 and the BNC2 terminal of the channel is shorted to GND. When a TTL low level voltage is applied on terminal 2, the LED is turned off and the transistor is turned off. Assume there is no load. Thus, R_2 does not drain any voltage and voltage of the BNC2 terminal is identical to DC supply voltage +15 V. With the external circuit configured as shown

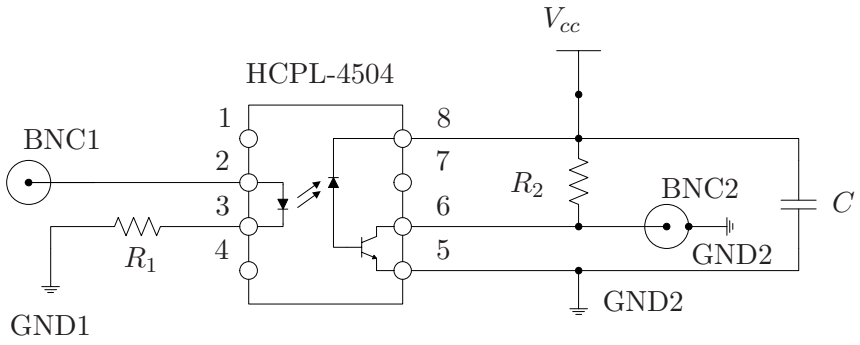


Figure 3.13: Single channel schematics of level shifting board. The six channels are identical and all have negative logic.

in Figure 3.12(b), R_1 is chosen as 200 Ω to ensure the input current is lower than the rated input current. The high level output voltage equals to 15 V when there is no load. When a load is connected, its value depends on the value of R_2 and the input impedance of the load. Since the input impedance of the IGBT driver is 10 kΩ, R_2 is chosen as 2.21 kΩ so that the voltage at the BNC2 terminal is 15 V × 10 kΩ/(10 kΩ + 2.21 kΩ) = 12.3 V which is higher than the high threshold voltage of the driver.

Since the input impedance of the device connected to the secondary side of the board can significantly affect the board output, performing any board test with no load is meaningless. Therefore, the board was verified by applying the board outputs to drive the VSC while the VSC was operated as an inverter and monitoring the voltage between each AC terminal and the negative DC terminal. This voltage is supposed to be in phase with the corresponding PWM signal. The VSC was powered by a 10 V DC supply and the PWM gating signals are generated based the modulating signals with $m_a = 0.8$, and $\delta = 0$. The result of phase a is shown in Figure 3.14. Channel 1 displays the PWM signal and Channel 2 displays the voltage between each AC terminal and the negative DC terminal. It is clear that the voltage is in phase with corresponding PWM signals. Therefore, we can conclude that the level shifting board is functional.

Since the maximum input of DS2001 board is 10 V, another very simple level shifting board is used to shift the 15 V error signals to 5 V. The board has

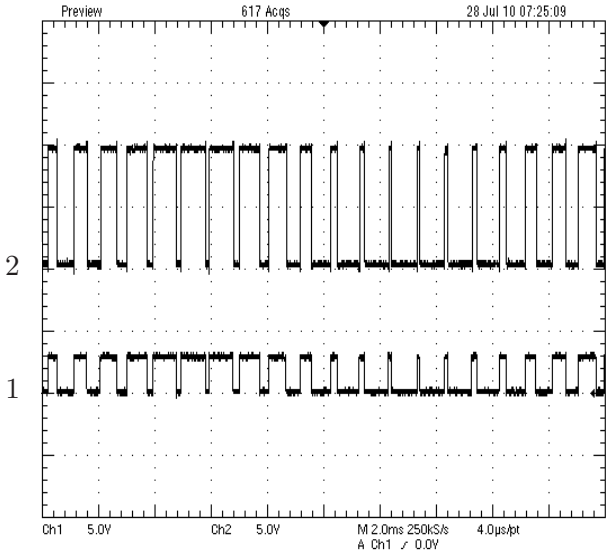


Figure 3.14: Test result of the level shifting board. Channel 1 displays the PWM signal and Channel 2 displays the voltage between each AC terminal and the negative DC terminal.

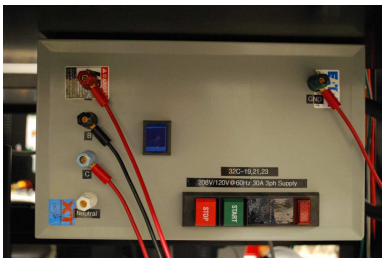
three channels and does not require power. Only one resistor is used together with the output impedance of the error signal ports to divide the voltage.

3.1.5 Other Hardware

Besides the components discussed above, the system includes an AC power supply, a DC power supply, and a three-phase choke.

AC Power Supply

The AC power source of the system is actually a combination of a three-phase power supply module, shown in Figure 3.15(a), and a standard three-phase variable transformer, shown in Figure 3.15(b). This power supply module provides 120 V/60 Hz three-phase AC voltage and its rated output current is 30 A. Actually, the AC currents are sightly distorted and not exact sinusoidal. There are five connectors denoted by different colors on the module. Red, black and blue denote phase a, b, c, respectively, a white connector is neutral, and green is ground. On the lower right, there are two push buttons; the green one is for turning on the power supply and the red one is for shutting it down.



(a) Connector box to the three-phase power source

(b) Three-phase manually variable transformer

Figure 3.15: The AC power supply of the system. It is a combination of a three-phase power source and a three-phase manually adjustable transformer. The power source has rated AC voltage 120 V/60 Hz and the transformer provides flexibility to manually adjust the output voltage used to excite the VSC.

The variable transformer is used for facilitating the startup procedure. It allows the amplitude of the AC supply to be continuously varied between 0 V $\sim$ 120 V.

DC Power Supply

The DC power supply is manufactured by Condor DC Power Supplies Inc. This unit is able to convert a single-phase 120 V AC voltage to four different DC voltage, i.e., 5.1 V, +24 V, +15 V, and −15 V. It is used to power the IGBT drivers with 15 V, voltage-current sensor board with ±15 V, and the level shifting board with 15 V. Since the 5.1 V and +24 V outputs require non-zero minimum output currents which are 1 A and 0.5 A, respectively, two power resistors are connected as loads as these two outputs are not used. The device is shown in Figure 3.16.

Three-Phase Reactor

The three-phase line reactor is manufactured by Hammond Power Solutions Inc. It is connected between the AC power supply and the sensor boards in order to reduce the current harmonics caused by IGBT switching and improve

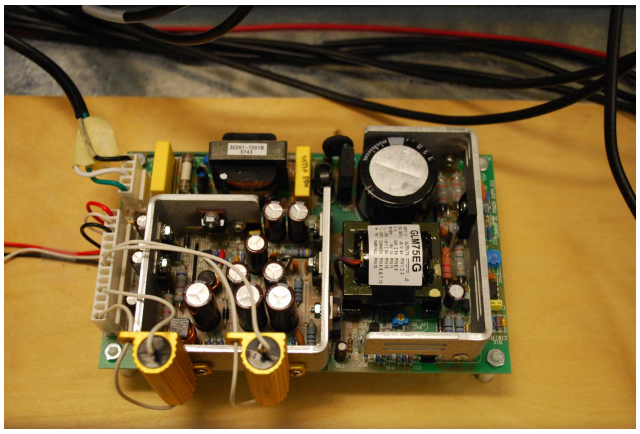


Figure 3.16: Condor DC power supply. It provides various DC voltages and only ±15 V and ground are used in our test stand.

the power factor of the VSC. The reactor has a 1 mH static inductance for each phase and 1 mH mutual inductance when currents flow. The actual unit is shown in Figure 3.17.

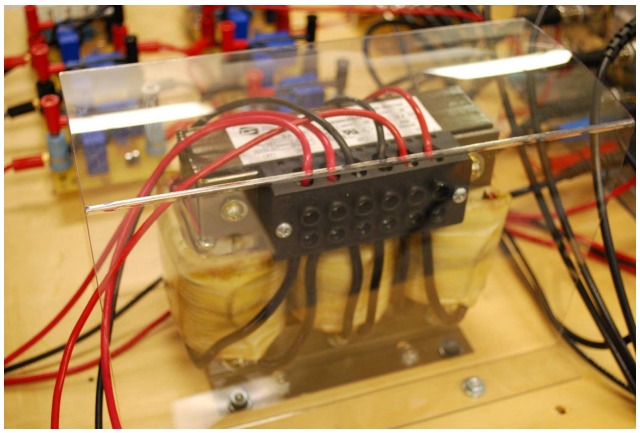


Figure 3.17: Hammond three-phase reactor. It has a 1 mH static inductance for each phase and 1 mH mutual inductance when currents flow.

3.1.6 Experiment Software

The dSPACE control system uses MATLAB/Simulink to implement the control algorithm and the ControlDesk software to monitor and interface with the controller.

Control Algorithm Implementation

The dSPACE system provides a Real-Time Interface (RTI) which provides a library in Simulink. RTI provides easy use of the dSPACE I/O boards in Simulink. The Simulink model of the controller is shown in Figure 3.18, and the controller's structure is described in the following.

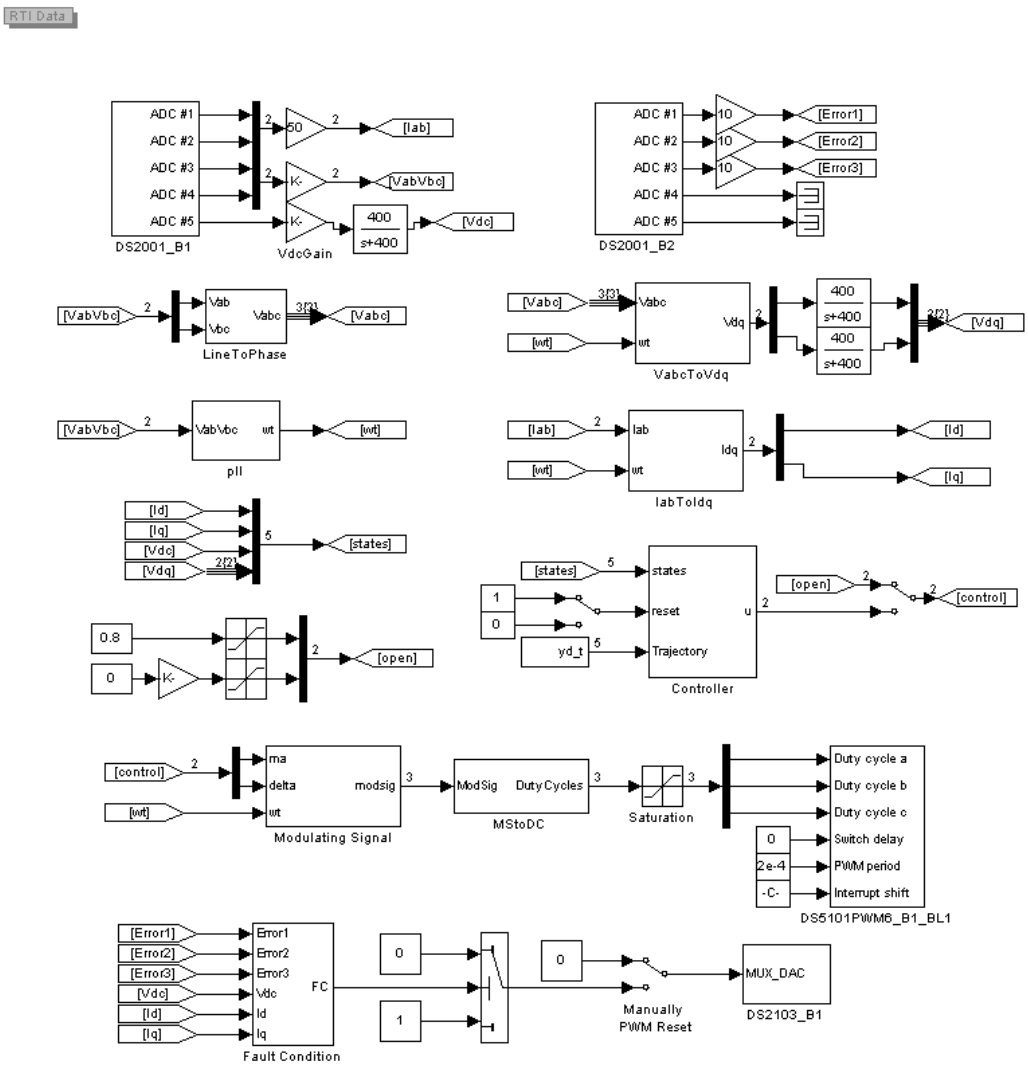


Figure 3.18: Simulation model of the control scheme.

The sensor boards scale the actual current values down to 1/5 and the voltage values down to 1/50, and then these measurements are scaled again and down to 1/10 by the Simulink block of the DS2001. Therefore, the scale

factor of the current outputs of the block is 50 and the scale factor of the voltage outputs of the block is 500. To reduce the disturbance and harmonics fed into controller by noise on v_{dc}, a low-pass filter is included. With these scaled and filtered signals, i_c is calculated based on i_a and i_b, phase voltage v_a, v_b, and v_c are calculated from line voltages v_{ab} and v_{bc}, and the reference angle ωt. Based on the assumption of balanced AC power supply,

$$v_a + v_b + v_c = 0, \quad i_a + i_b + i_c = 0$$

Therefore, we have

$$i_c = -i_a - i_b, \quad v_a = \frac{2v_{ab} + v_{bc}}{3}, \quad v_b = \frac{-v_{ab} + v_{bc}}{3}, \quad v_c = \frac{-v_{ab} - 2v_{bc}}{3}$$

To calculate ωt, we recall that

$$\begin{aligned} v_a(t) &= V_m \cos(\omega t) \\ v_b(t) &= V_m \cos(\omega t - \frac{2\pi}{3}) \\ v_c(t) &= V_m \cos(\omega t + \frac{2\pi}{3}) \end{aligned}$$

Hence

$$\begin{aligned} v_{ab}(t) &= V_m \cos(\omega t) \\ &\quad - V_m \left(\cos(\omega t) \cos(\frac{2\pi}{3}) + \sin(\omega t) \sin(\frac{2\pi}{3}) \right) \\ &= V_m \left(\frac{3}{2} \cos(\omega t) - \frac{\sqrt{3}}{2} \sin(\omega t) \right) \end{aligned}$$

and

$$\begin{aligned} v_{bc}(t) &= V_m \left(\cos(\omega t) \cos(\frac{2\pi}{3}) + \sin(\omega t) \sin(\frac{2\pi}{3}) \right) \\ &\quad - V_m \left(\cos(\omega t) \cos(\frac{2\pi}{3}) - \sin(\omega t) \sin(\frac{2\pi}{3}) \right) \\ &= V_m(\sqrt{3} \sin(\omega t)) \end{aligned}$$

which results in

$$\begin{aligned} V_m \sin(\omega t) &= \frac{1}{\sqrt{3}} v_{bc}(t) \\ V_m \cos(\omega t) &= \frac{1}{3}(2v_{ab}(t) + v_{bc}(t)) \end{aligned}$$

Hence, the reference angle is computed by

$$\omega t = \tan^{-1}\left(\frac{\sin(\omega t)}{\cos(\omega t)}\right) = \tan^{-1}\left(\frac{3v_{bc}(t)}{\sqrt{3}(2v_{ab}(t)+v_{bc}(t))}\right)$$

Furthermore, the synchronous reference transformation (2.8) is performed to both currents and voltages to generate i_d, i_q, v_d, and v_q. These four signals are fed in the feedback control (2.27) together with v_{dc}. The outputs of the feedback control law and ωt can be used to generate three-phase modulating signals which are transformed to duty cycles of the desired PWM signals. Figure 3.19 illustrates the relationship between the duty cycle d of phase a PWM and the associated modulating signal.

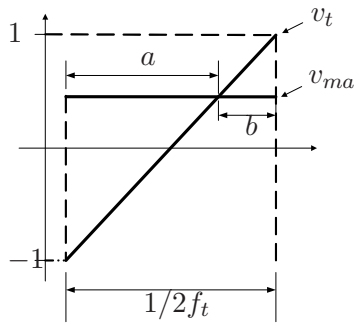


Figure 3.19: Relation between duty cycle and modulating signal.

Although the sampling frequency f_s is twice of switching frequency f_t, the duty cycle during one switching period dose not change. Therefore, to simplify the discussion, we assume the value of phase a modulating signal v_{ma} does not change during the switching period. From simple geometry we have

$$\frac{b}{1/2f_t} = \frac{1-v_{ma}}{2}$$

Hence,

$$d = 1 - \frac{b}{1/2f_t} = 1 - \frac{1-v_{ma}}{2} = \frac{v_{ma}+1}{2}$$

The duty cycles are input to the DS5101 block to generate the gating signals. Open-loop control is also provided in this Simulink model and an internal protection algorithm is implemented to deliver reset signal to DS5101 via DS2103 D/A board when an IGBT driver error occurs or states leave and acceptable region.

To build the model, the start time of the simulation is set at zero and the end time is set at "inf". Only fixed-step single-tasking solvers are allowed to compile RTI model. After compiling the model, MATLAB generates a *.sdf (standard data file) file which is used by ControlDesk to monitor and control the experiment.

Interface Software

ControlDesk allows us to control and monitor the status of the experiment. The main window of the ControlDesk development environment is shown in Figure 3.20.

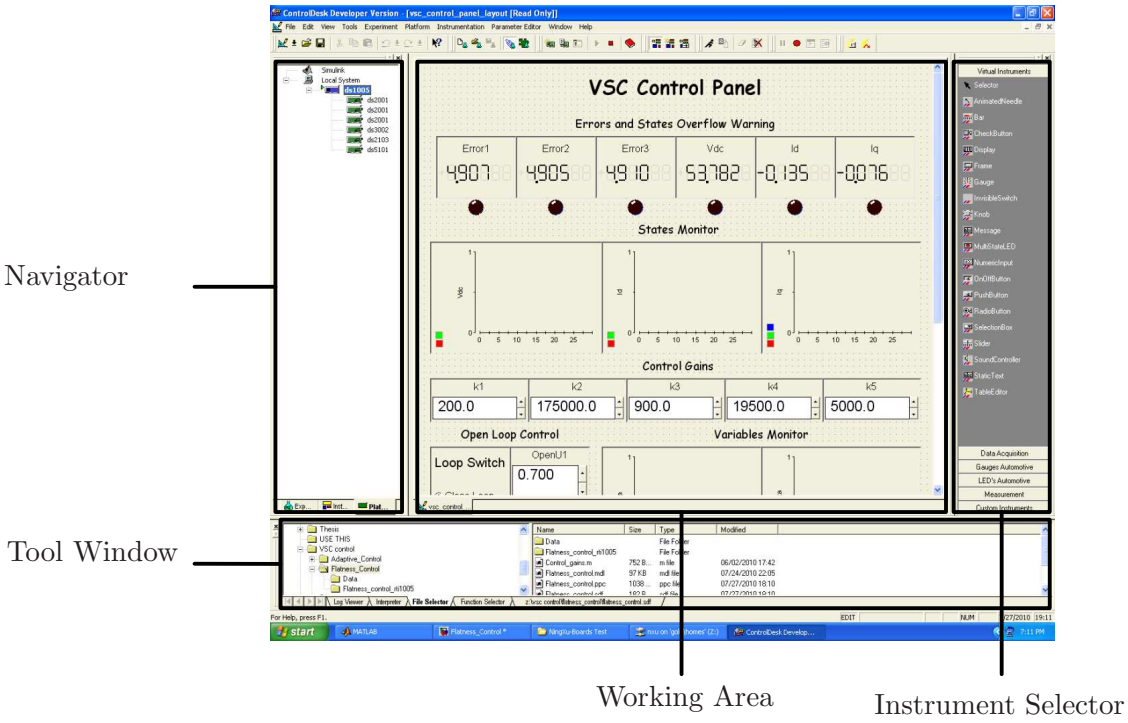


Figure 3.20: Main window of the ControlDesk. It contains four major parts: navigator, tool window, working area, and instrument selector.

The navigator displays all files and functions of the open experiment, all the variables of the model, all platforms registered in your system, and all functions needed for advanced test. The working area is normally used to build instrument panels to monitor and interact with the real-time experiment. The instrument selector provides virtual instruments which can be dragged into

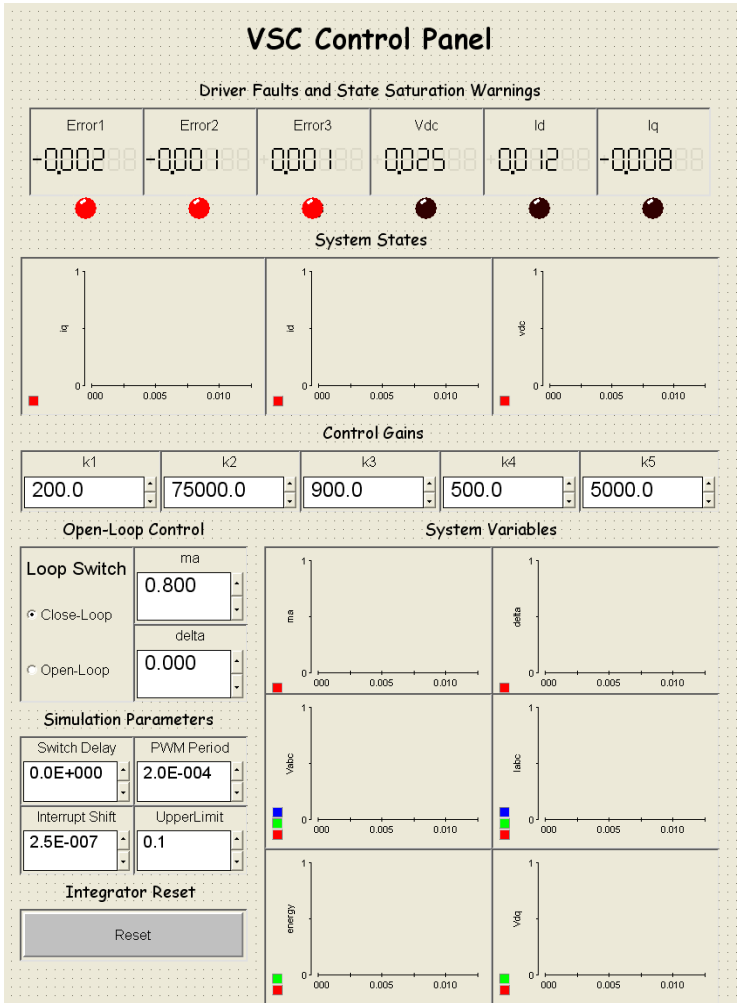


Figure 3.21: ControlDesk instrument panel of the linearization-based controller.

the working area to build instrument panels. The tool window provides access to all the signals and parameters of the Simulink model. All the variables and parameters can be easily dragged to various instruments to associate with them. With different instruments, the data and parameters can be set, displayed, and stored. The instrument panel used in this experiment is shown in Figure 3.21.

In the "Driver Faults and State Saturation Warnings" section indicate driver error signals and out of range system states using warning LEDs which light when an abnormal situation arises. Numerical values of the the signals are also displayed. The "System States" section displays time trajectories of

the system states i_d, i_q, v_{dc}. Five control gains of the control algorithm can be tuned individually in the "Control Gains" section. The "Open-loop Control" section provides a switch to select between open-loop and closed-loop operation. Open-loop values of m_a and δ can be assigned. "System Variables" plots trajectories of control inputs m_a and δ, three-phase AC currents i_{abc}, three-phase AC voltages v_{abc}, voltages in synchronous reference frame v_d and v_q, and the energy stored in the VSC. Several important parameters of DS5101 are provided to modify the PWM generation in real-time. A button resets the internal integrator of the controller.

3.2 System Interconnection

The system interconnection is illustrated in Figure 3.22 and described in this section. The three-phase AC power supply is connected with the variable transformer to work as a variable power source. Sensor board one is connected on the secondary side of the transformer to measure v_{ab}, v_{bc}, i_a, and i_b. The three-phase reactor is connected between the first sensor board and the VSC AC terminal. The second sensor board is connected on the DC terminal of the VSC to measure v_{dc}. Only one channel is used on this board. Using a distinct colour for each phase of the AC voltage on the power supply, transformer, sensor boards, and AC terminal of the VSC simplifies interconnection.

The first six channels of DS5101 are connected to the primary side of the level shifting board. Since the board shifts signals with negative logic, all the PWM input signals become their inverted signals. Therefore, the shifted signals of channel 1, 3, and 5 are used to drive the bottom IGBTs and the shifted signals of channel 2, 4, and 6 are used to drive the top IGBTs. The error signals of the IGBT drivers are connected to the first three channel of the DS2001 Board #2. The measurements of five quantities i_a, i_b, v_{ab}, v_{bc}, and v_{dc} are sent to the DS2001 Board #1 as shown in Figure 3.22.

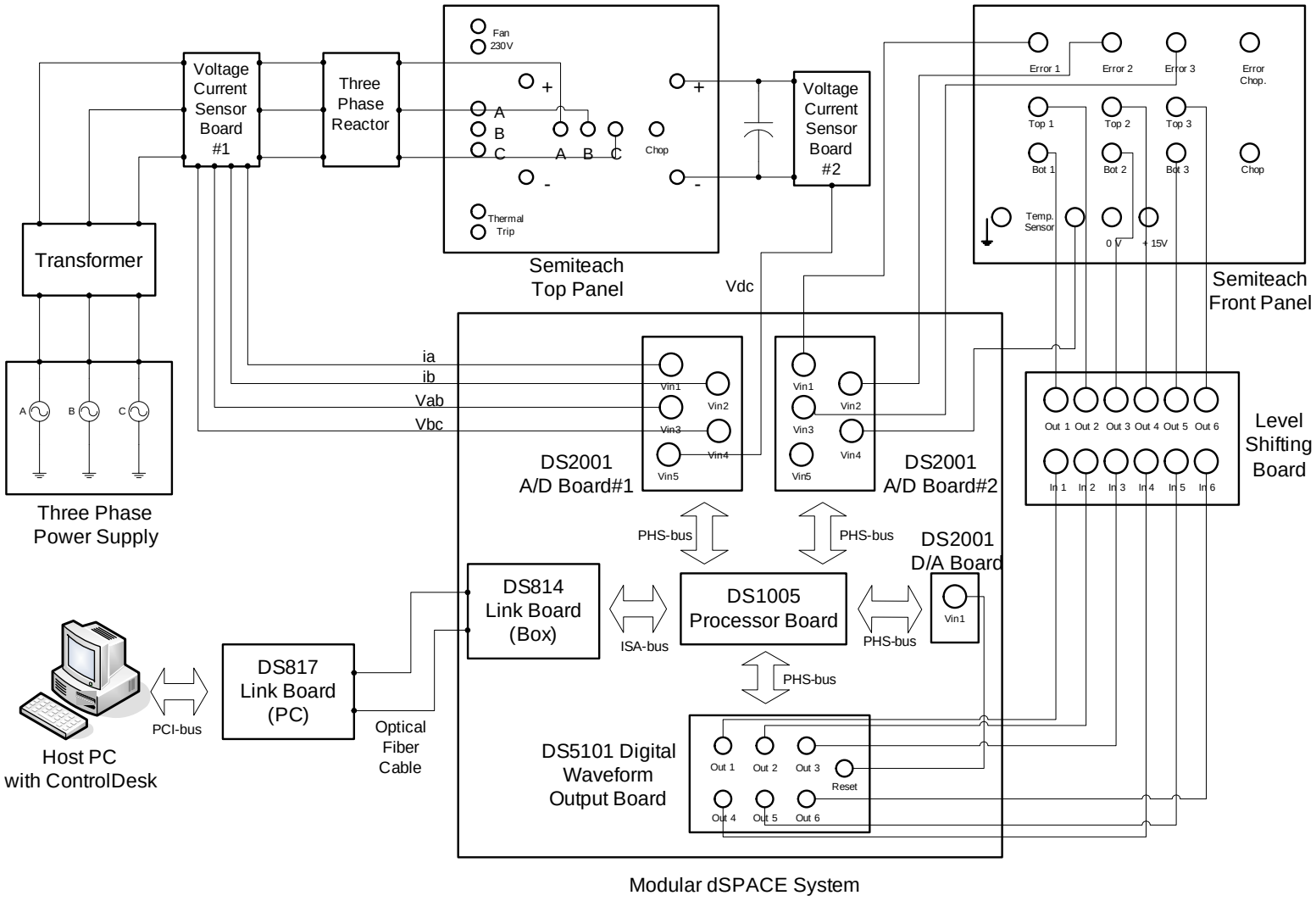


Figure 3.22: Interconnections of most components of the test stand. For better view, the top panel and the front panel of the VSC are displayed in the same plane. All the components are labeled as same as the actual.

3.3 System Tests

Before operating the test stand, a number of tests were performed to verify it's operation. One test was performed when testing the level shifting board. This test is performed to ensure that the PWM signals are capable of driving the IGBTs properly. We applied 10 V DC voltage to the VSC DC terminal and monitored the voltage between AC terminals and DC negative terminal. If the gating signal is able to switch the corresponding IGBT properly, e_o should switch between 0 to 10 V. Figure 3.23 demonstrates the expected result and indicates perfect gating signal generation. Since e_o is the function of gating signal g and DC voltage v_{dc}, we can determine the fault when the IGBT switching fails. For example, when the upper IGBT cannot be closed appropriately, the high level value of the voltage between the AC terminal and the negative DC terminal will be $v_{dc}/2$ rather than v_{dc}; when the lower IGBT cannot be closed appropriately, the voltage will switch from $v_{dc}/2$ to v_{dc} instead of 0 to v_{dc}.

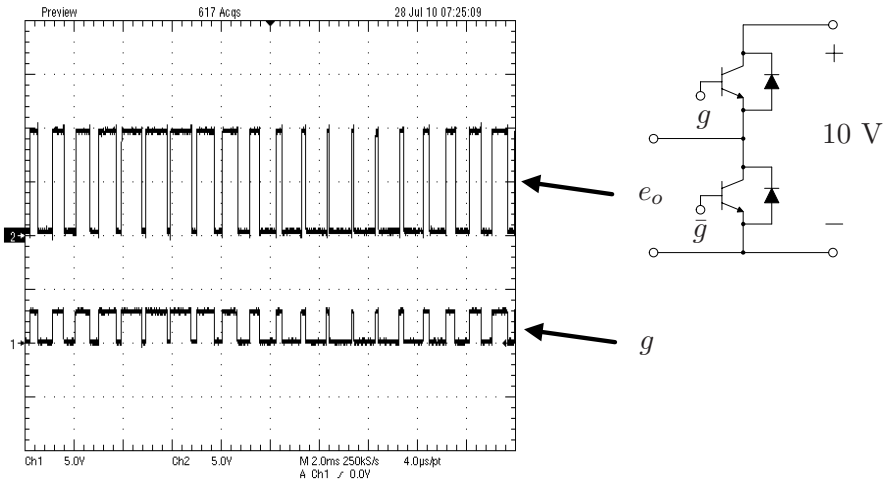


Figure 3.23: IGBT Switching Status Test. The output voltage e_o is the function of gating signal g and DC voltage v_{dc}. By monitoring e_o, we can determine whether the gating signals are able to switch the IGBTs properly.

Another important test was performed to make sure the generated PWM signal is in phase with the corresponding AC voltage when $\delta = 0$. If there is a phase shift between these two signals, the response of the VSC will be delayed

or advanced and control performance can suffer. To address this concern, the non-inverted PWM and AC voltage of phase a are displayed together and shown in Figure 3.24. From the figure, it is clear that the duty cycle of the

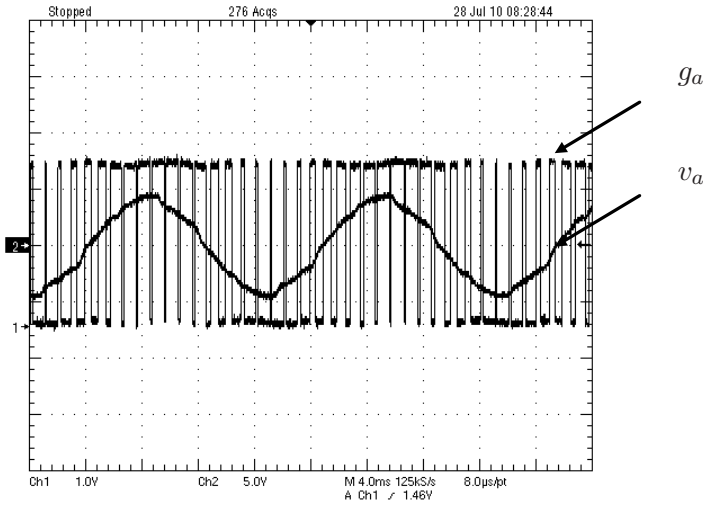


Figure 3.24: Test result of the phase angle. The AC voltage of the VSC share same phase angle with their associated gating signals. This test is to ensure that the PWM gating signals are properly generated. Channel 1 displays the phase a PWM signal and channel 2 displays AC voltage of phase a.

PWM signal becomes maximum when the AC voltage reaches peak so that the generated PWM signals are in phase with the corresponding AC voltage signals.

3.4 Startup Operation

When the control algorithm was simulated in the previous chapter, initial states were assigned to avoid large transients. In order to establish suitable initial conditions in experiment, we forced all IGBT open and let the VSC operate as a rectifier to charge the capacitor. After v_{dc} reaches is maximum voltage, the closed-loop controller was activated. However, this approach failed on our test stand. As mentioned before, the IGBT drivers provide voltage monitoring between the collectors and emitters of the IGBTs. When the current though any IGBT increases significantly, an abnormally high voltage is detected and

the protection is triggered. Unfortunately, high transient current always occurs when the duty cycle of the PWM signal changes significantly in a very short period, which means any controller switch, e.g. , from open-loop control to closed-loop control, is not acceptable. And the protections of the drivers are extremely sensitive to this type of pulse currents and detect them as fault signals.

Without initial states and any controller switching, the controller should be able to stabilize the system with very low three-phase AC voltages and maintain the performance as the amplitude of the AC voltages are ramped up. This is basically a tuning issue and can be achieved with properly chosen control gains. The control gains used during start up operation were selected as $k_1 = 2 \times 10^2 \mathrm{s}^{-3},\ k_2 = 7.5 \times 10^4 \mathrm{s}^{-2},\ k_3 = 9 \times 10^2 \mathrm{s}^{-1},\ k_4 = 5 \times 10^2 \mathrm{s}^{-2},\ k_5 = 6 \times 10^3 \mathrm{s}^{-1}$. After the system operates in steady state, the controller was further tuned to improve its performance.

3.5 Experiment Results

In this section, the experiment results are presented based on the feedback linearization-based control algorithm. The trajectories are well defined in previews chapter. The system should operate from one equilibrium point $v_{dc} = 150$ V, $i_q = -5$ A to another equilibrium point $v_{dc} = 200$ V, $i_q = 5$ A. To avoid large signal overshoots during the transition, the transition time $t_1 - t_0$ is chosen to be 100 ms. Since the twice of peak AC voltage needs to be lower than the DC link voltage of the VSC, the amplitude of the three-phase voltage is chosen as 60 V.

3.5.1 Trajectory Tracking Performance

The tracking performance of i_q and v_{dc} are shown in Figure 3.25. All the signals are captured unfiltered. Good tracking of i_q is achieved; transition time is around 100 ms and no overshoot occurs. The ripples in the signal is caused by IGBT switching. The DC voltage signal tracks the reference with a small steady state error which may be due to modeling error or disturbances.

Transient performance is excellent. i_d is not zero in steady state due to the losses of the system, and a pulse occurs for charging the DC link capacitors when v_{dc} is increased. The two control outputs m_a and δ do not saturate during the transition. The control gains were chosen as $k_1 = 5 \times 10^2 \mathrm{s}^{-3}$, $k_2 = 8.5 \times 10^5 \mathrm{s}^{-2}$, $k_3 = 10^3 \mathrm{s}^{-1}$, $k_4 = 2 \times 10^4 \mathrm{s}^{-2}$, $k_5 = 5 \times 10^3 \mathrm{s}^{-1}$.

3.5.2 Vector Control Scheme and results

A traditional vector control method presented in [28] is implemented to allow a comparison of performance. As discussed previously, the current dynamics in the synchronous reference frame are

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L} i_d + \omega i_q + \frac{v_d}{L} - \frac{e_d}{L} \\ \frac{di_q}{dt} &= -\frac{R_s}{L} i_q - \omega i_d - \frac{e_q}{L} \end{aligned} \tag{3.1}$$

In this subsystem, e_d and e_q are taken as control inputs. If e_d and e_q are chosen as

$$\begin{aligned} e_d &= v_d + L(\omega i_q - p_1) \\ e_q &= L(-\omega i_d - p_2) \end{aligned} \tag{3.2}$$

where

$$\begin{aligned} p_1 &= k_{id}^p (i_d^* - i_d) + k_{id}^i \int_0^\tau (i_d^* - i_d) d\tau \\ p_2 &= k_{iq}^p (i_q^* - i_q) + k_{iq}^i \int_0^\tau (i_q^* - i_q) d\tau \end{aligned}$$

Substituting (3.2) into (3.1) leads to

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_s}{L} i_d + k_{id}^p (i_d^* - i_d) + k_{id}^i \int_0^\tau (i_d^* - i_d) d\tau \\ \frac{di_q}{dt} &= -\frac{R_s}{L} i_q + k_{iq}^p (i_q^* - i_q) + k_{iq}^i \int_0^\tau (i_q^* - i_q) d\tau \end{aligned}$$

Clearly, the closed-loop dynamics for i_d and i_q are decoupled and tracking error can be controlled by tuning $k_{id}^p, k_{id}^i, k_{iq}^p$, and k_{iq}^i.

The voltage v_{dc} is coupled with i_d since only the real current charges the capacitor. Therefore, v_{dc} is indirectly controlled by i_d. An inner-outer loop control scheme is presented. i_d is controlled by a relatively faster inner loop controller and v_{dc} is controlled by the outer loop controller. The error between

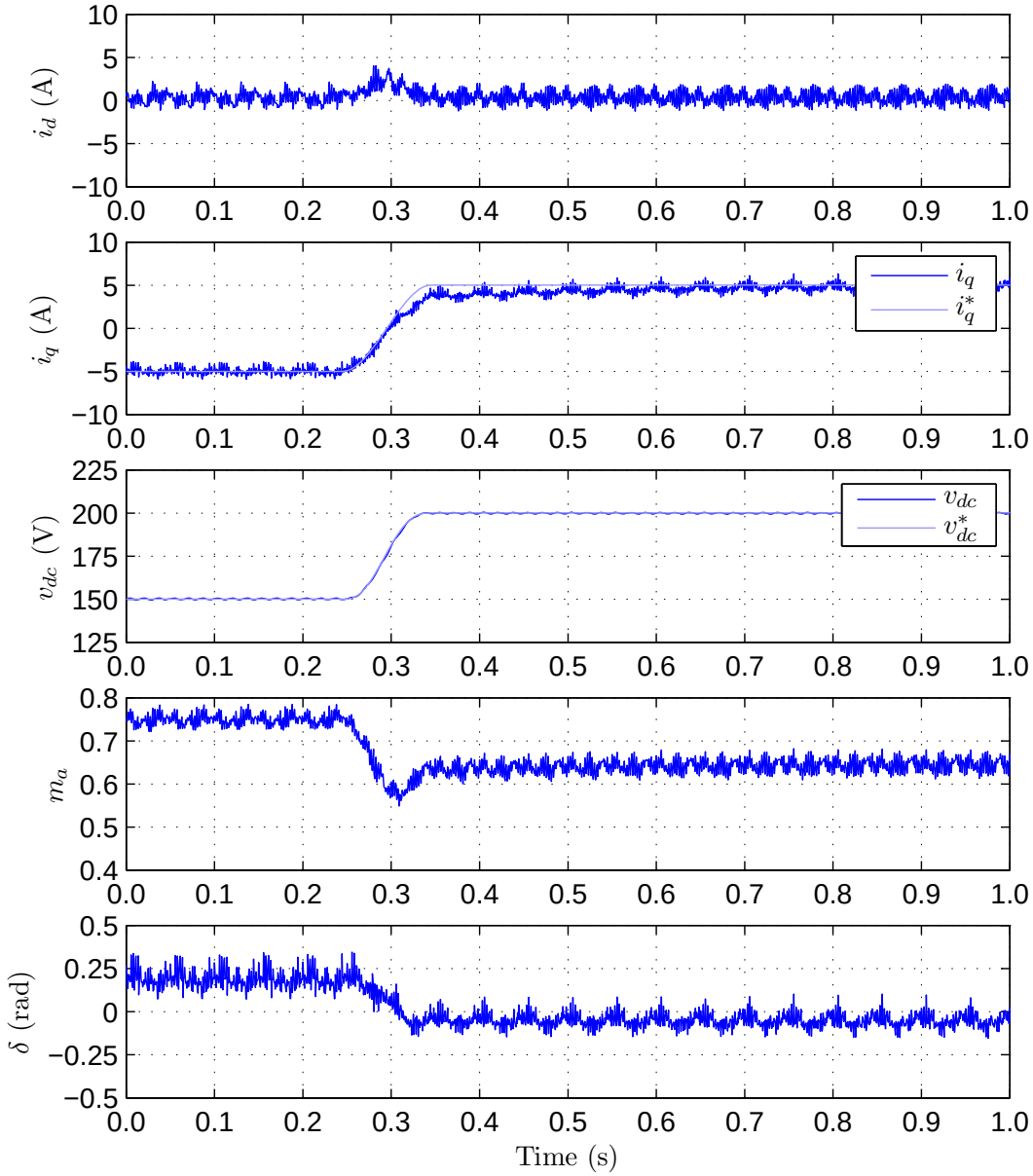


Figure 3.25: The experiment results of the linearization-base control scheme. The references of i_q and v_{dc} are shown by the lighter lines. The ripples in the current are caused by the IGBT switching and can be reduced by applying a low-pass filter.

v_{dc} and its reference v_{dc}^* is used to generate i_d^* so that enough i_d is delivered to maintain the DC voltage. We have

$$I_d^*(s) = \left(k_v^p + \frac{k_v^i}{s}\right)(V_{dc}^* - V_{dc})$$

A block diagram of this controller is illustrated in Figure 3.26.

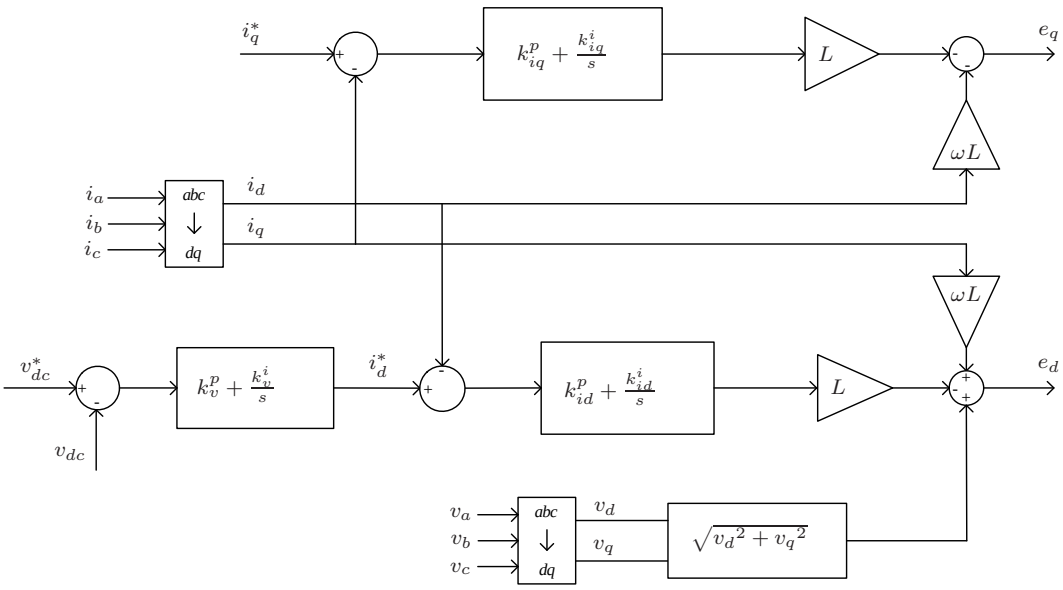


Figure 3.26: Block diagram of vector control algorithm. Three P-I compensators are included. Two references i_q^* and v_{dc}^* are directly assigned and the reference of i_d is generated by the v_{dc} compensator.

This control scheme was implemented on the test stand and the control gains were chosen as $k_{id}^p = 5000$ V/A, $k_{id}^i = 20000$ V/(A· s), $k_{iq}^p = 5000$ V/A, $k_{iq}^i = 20000$ V/(A·s), $k_v^p = 50$ A/V, $k_v^i = 200$ A/(V·s). The experimental results based on filtered states are shown in Figure 3.27.

Compared to feedback linearization, the ripples in currents and control inputs are sightly larger. This means the vector controller is less sensitive to the undesired disturbances and less efficient to remove the disturbances. However, acceptable tracking performance is achieved.

3.6 Summary

In this chapter, the entire experiment test stand has been described. A feedback linearization-based control and a vector control were implemented on the system. Both approaches demonstrated good tracking performance for tracking constant reference for i_q and v_{dc}.

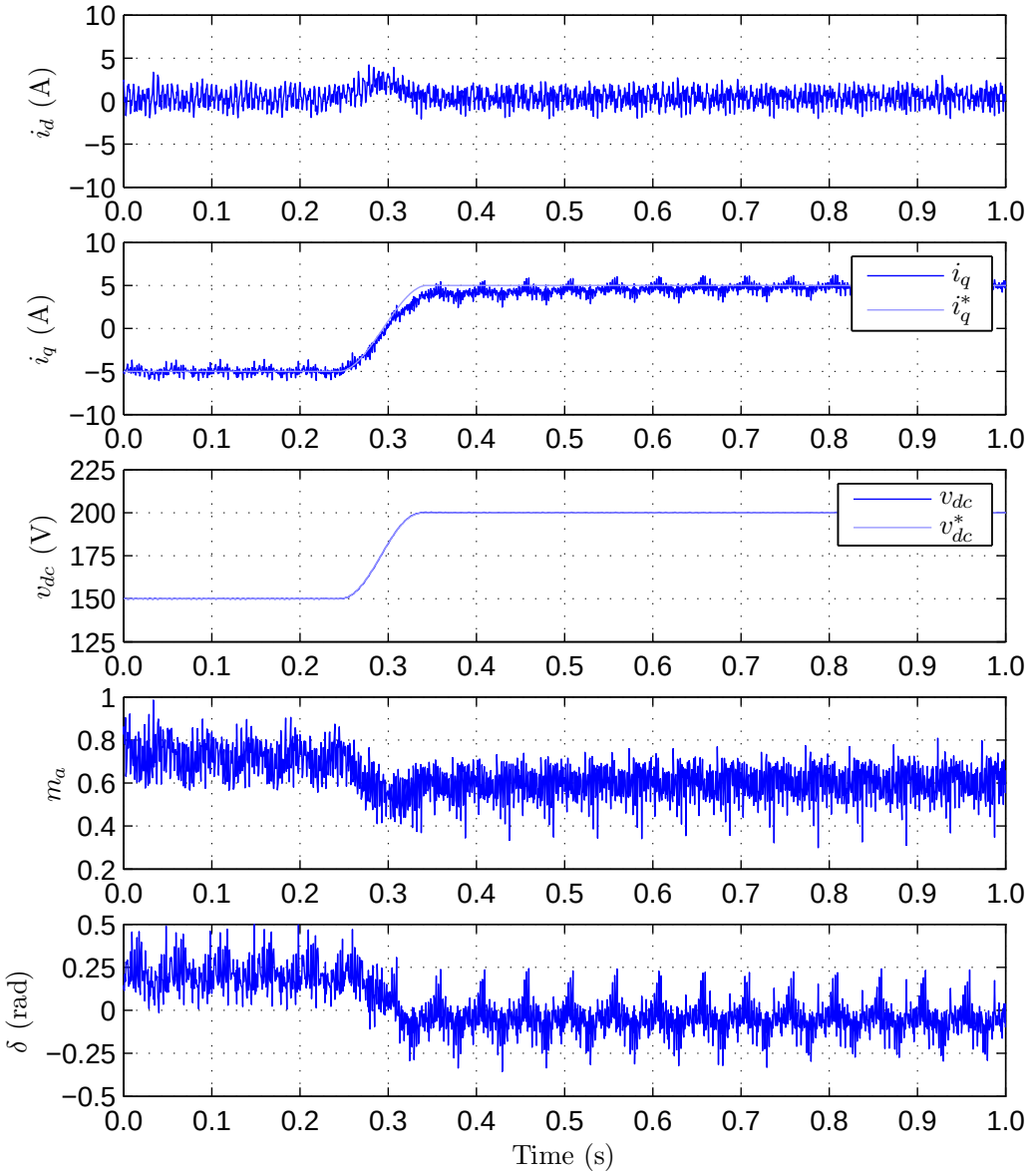


Figure 3.27: Experimental results of the vector control algorithm. Compare with the results of linearization-based controller, the current signals contains more ripples which means the controller is less capable of tolerant disturbances and system errors.

Chapter 4

Harmonic Cancelation

As introduced in Chapter 1, SAF is an important application of the VSC. In this chapter, a mathematical model of the SAF is derived with power states instead of currents and an internal model-based control algorithm is introduced. The controller is verified by simulation using the parameters of the model presented in Chapter 2.

4.1 Mathematical Model Derivation

The configuration of the SAF used in this chapter is in Figure 4.1 [21]. The source voltages v_a, v_b, and v_c are assumed balanced, e_a, e_b, and e_c are the AC terminal voltages of the filter, v_{dc} is the DC terminal voltage of the filter, i_{sa}, i_{sb}, and i_{sc} are the AC source currents, i_{la}, i_{lb}, and i_{lc} are the load currents, and i_a, i_b, and i_c are the filter currents. The model of VSC system in this configuration was introduced in Section 2.1.1. It contains three parameters L, R, and C and is given by

$$\begin{aligned} \frac{di_{abc}}{dt} &= -\frac{R}{L} i_{abc} + \frac{1}{L} v_{abc} - \frac{1}{L} e_{abc} \\ \frac{dv_{dc}}{dt} &= \frac{1}{C v_{dc}} e_{abc}^T i_{abc} \end{aligned} \tag{4.1}$$

where

$$v_{abc} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_m \cos(\omega t) \\ V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_m \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix}, \quad i_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad e_{abc} = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

Since having three current states are redundant, we apply the stationary reference frame transformation discussed in Section 2.1.3. We introduce

$$T_{abc}^{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{4.2}$$

and define the transformed variables

$$i_{\alpha\beta} = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_{abc}^{\alpha\beta} i_{abc}, \quad e_{\alpha\beta} = \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = T_{abc}^{\alpha\beta} e_{abc}, \quad v_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{abc}^{\alpha\beta} v_{abc}$$

which leads to

$$v_{\alpha\beta} = V_m \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix}$$

Therefore, the SAF model in α-β reference frame is expressed as

$$\begin{aligned} \frac{di_{\alpha\beta}}{dt} &= -\frac{R}{L} i_{\alpha\beta} + \frac{1}{L} v_{\alpha\beta} - \frac{1}{L} e_{\alpha\beta} \\ \frac{dv_{dc}}{dt} &= \frac{3}{2Cv_{dc}} e_{\alpha\beta}^T i_{\alpha\beta} \end{aligned} \tag{4.3}$$

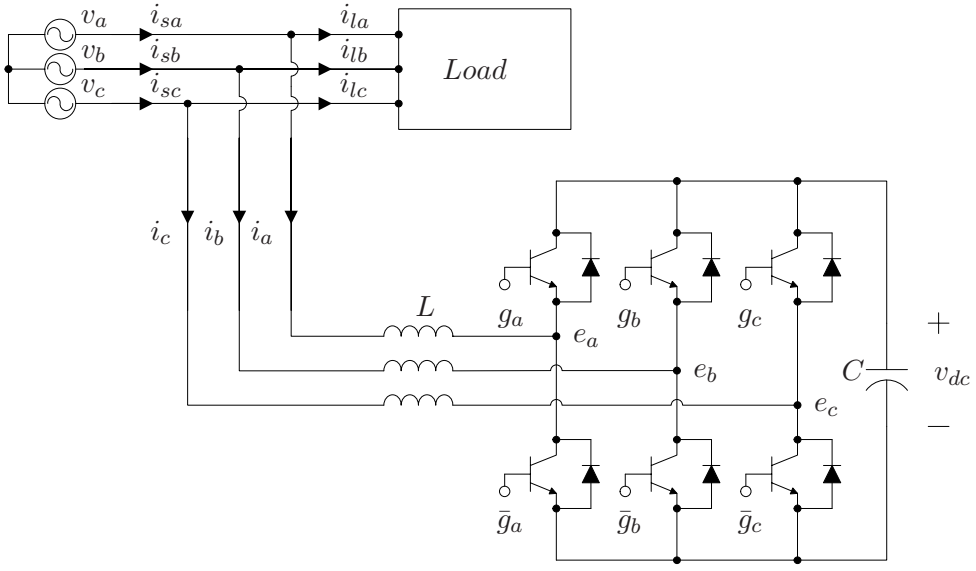


Figure 4.1: Shunt active filtering using a VSC. In this configuration, the VSC acts as a shunt active filter to compensate both active current harmonics and reactive current.

4.2 Power States Based Model

The control objectives discussed in Chapter 1 are that the SAF compensates the harmonic components of the real power and entire imaginary power of the

source while maintaining v_{dc} in a desired interval. The definitions of the instantaneous real and imaginary powers are reviewed here. Recall the definition of the conventional instantaneous real power of the three-phase system, it is expressed as

$$p = v_a i_a + v_b i_b + v_c i_c$$

and it can be transformed into α-β coordinates as

$$p = v_\alpha i_\alpha + v_\beta i_\beta$$

where $v_\alpha i_\alpha$ and $v_\beta i_\beta$ are the instantaneous real powers of the three-phase system on the α and β-axes.

The instantaneous imaginary power is introduced in [1]. The phasor of the instantaneous imaginary power is defined as

$$\mathbf{Q} = \mathbf{V}_\alpha \times \mathbf{I}_\beta + \mathbf{V}_\beta \times \mathbf{I}_\alpha$$

From the space vector diagram in Figure 4.2, the imaginary axis is perpen-

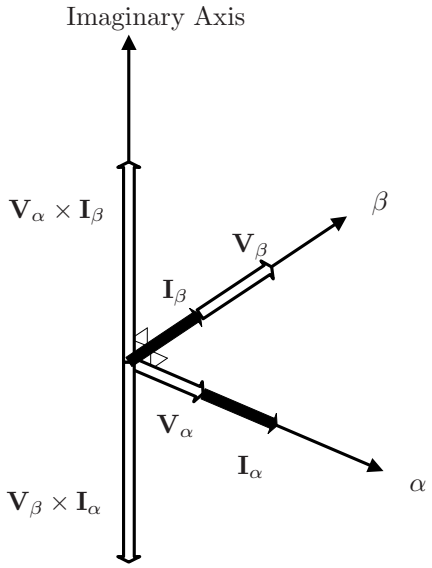


Figure 4.2: Phasor diagram of the instantaneous imaginary power in α-β coordinates. The imaginary axis is perpendicular to the α-β plane and respects the right-hand rule.

dicular to the plane of α-β coordinates and its direction is determined by the

right-hand rule. The instantaneous imaginary power is the amplitude of the phasor **Q**. Therefore, we have

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$
$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ q \end{bmatrix}$$

The currents in α-β coordinates, i_α and i_β, can be divided into active current and reactive current components on each axis. This means

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ 0 \end{bmatrix} + \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ q \end{bmatrix} = \begin{bmatrix} i_{\alpha p} + i_{\alpha q} \\ i_{\beta p} + i_{\beta q} \end{bmatrix}$$

where $i_{\alpha p}$ is the active current component in the α-axis, $i_{\alpha q}$ is the reactive current component in the α-axis, $i_{\beta p}$ is the active current component in the β-axis, and $i_{\beta q}$ is the reactive current component in the β-axis. Expanding the above equation gives

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} p, \quad i_{\alpha q} = -\frac{v_\beta}{v_\alpha^2 + v_\beta^2} q, \quad i_{\beta p} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2} p, \quad i_{\beta q} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} q$$

Then, p can be presented as

$$p = v_\alpha\, i_{\alpha p} + v_\alpha\, i_{\alpha q} + v_\beta\, i_{\beta p} + v_\beta\, i_{\beta q} = p_{\alpha p} + p_{\alpha q} + p_{\beta p} + p_{\beta q}$$

where $p_{\alpha p}$ is the active power in the α-axis, $p_{\alpha q}$ is the reactive power in the α-axis, $p_{\beta p}$ is the active power in the β-axis, $p_{\beta q}$ is the reactive power in the β-axis. And

$$p_{\alpha p} = \frac{v_\alpha^2}{v_\alpha^2 + v_\beta^2} p, \quad p_{\alpha q} = -\frac{v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2} q, \quad p_{\beta p} = \frac{v_\beta^2}{v_\alpha^2 + v_\beta^2} p, \quad p_{\beta q} = \frac{v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2} q$$

Note that

$$p = p_{\alpha p} + p_{\beta p}$$
$$0 = p_{\alpha q} + p_{\beta q}$$

Therefore, the instantaneous real power p is the sum of the active powers $p_{\alpha p}$ and $p_{\beta p}$, and the reactive powers $p_{\alpha q}$ and $p_{\beta q}$ are complementary and determined by the instantaneous imaginary power q.

In order to compensate the harmonic components of instantaneous real power p and the instantaneous imaginary power q of the source, the states of

the model (4.3) are transformed from current coordinates to power coordinates. The power variables are defined as

$$x = \begin{bmatrix} x_p \\ x_q \end{bmatrix} = T \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$

where

$$T = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}$$

whose inverse is

$$T^{-1} = \frac{1}{E_{mp}} \begin{bmatrix} V_m \cos(\omega t) & -V_m \sin(\omega t) \\ V_m \sin(\omega t) & V_m \cos(\omega t) \end{bmatrix}$$

where $E_{mp} := v_\alpha^2 + v_\beta^2 = V_m^2$. Thus, the final model of SAF in power coordinates is

$$\begin{aligned} \frac{dx}{dt} &= M(R, L)x - \frac{1}{L}u + d_o \\ \frac{dv_{dc}^2}{dt} &= \epsilon u^T x \end{aligned} \tag{4.4}$$

where

$$M(R, L) = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix}, \quad d_o = \begin{bmatrix} \frac{E_{mp}}{L} \\ 0 \end{bmatrix}, \quad \epsilon = \frac{3}{CE_{mp}}$$

and $u = T^{-1}e_{\alpha\beta}$ is a new control input designed to achieve both control objectives. Note that the first objective can be defined as a tracking problem that requires x_p and x_q to track prescribed reference signals. With an ideal lossless VSC, the tracking reference was justified in (1.1) and recalled here

$$x^* = \begin{bmatrix} x_p^* \\ x_q^* \end{bmatrix} = \begin{bmatrix} P_{l0} - p_l \\ -q_l \end{bmatrix}$$

However, in reality, the real power compensated by the SAF also includes the power loss of the SAF itself and the energy required to maintain v_{dc} in a reasonable interval $[V_{dc,m}, V_{dc,M}]$. Therefore, the actual reference has been designed in [22] as

$$x_\eta^* = x^* - N_1 q(\tilde{z}) + N_1 \eta \tag{4.5}$$

Where $N_1 = [1, 0]^T$, $\tilde{z}$ is the voltage error variable which is defined as

$$\tilde{z} := v_{dc}^2 - \bar{V}^2, \text{ with } \bar{V}^2 = \frac{V_{dc,m}^2 + V_{dc,M}^2}{2} \tag{4.6}$$

Note that $\tilde{z}$ has to belong to $[-l^*, l^*]$ for all time, where $l^* = (V_{dc,M}^2 - V_{dc,m}^2)/2$, to ensure v_{dc} in the region $[V_{dc,m}, V_{dc,M}]$. The function $q(\cdot) : \mathbb{R} \to \mathbb{R}$ is a

deadzone function to keep v_{dc} in the desired range. When v_{dc} is far away from the boundary, which means the absolute value of $\tilde{z}$ is less than a positive value l and $l < l^*$, then $q(\tilde{z}) \equiv 0$. When v_{dc} approaches the upper boundary, $q(\tilde{z})$ becomes larger to decrease the power reference and keep v_{dc} within the region. When v_{dc} approaches the lower boundary, $q(\tilde{z})$ becomes smaller to enhance the power compensation of the SAF and charge the DC link capacitor. The extra control state η asymptotically estimates the power losses of the SAF. Its dynamics are given as

$$\dot{\eta} = -\epsilon h(\tilde{z}) \tag{4.7}$$

where $h(\cdot) : \mathbb{R} \to \mathbb{R}$ satisfies $h(s) = 0$ for all $s \in \mathbb{R}$ and $|s| < l$.

Based on this power reference, the power error variable can be defined as

$$\tilde{x} = x - x^*_\eta = x - x^* + N_1 q(\tilde{z}) - N_1 \eta \tag{4.8}$$

and the error variable of η is $\tilde{\eta} = \eta - \varphi_o$ where φ_o is the power loss of the system. Therefore, based on the error variables defined in (4.6) and (4.8), the error dynamics of the system is

$$\begin{aligned} \dot{\tilde{x}} &= M(R, L)\tilde{x} - \frac{1}{L}u + d(t) + I(\tilde{\eta}, \tilde{z}, \dot{\tilde{\eta}}, \dot{\tilde{z}}), \\ \dot{\tilde{z}} &= \epsilon u^T(\tilde{x} + x^* - N_1 q(\tilde{z}) + N_1 \tilde{\eta}), \\ \dot{\tilde{\eta}} &= -\epsilon h(\tilde{z}) \end{aligned} \tag{4.9}$$

where

$$d(t) := d_o + M(R, L)x^*(t) - \dot{x}^*(t) + M(R, L)N_1\varphi_o$$

and

$$I(\tilde{\eta}, \tilde{z}, \dot{\tilde{\eta}}, \dot{\tilde{z}}) := M(R, L)N_1(\tilde{\eta} - q(\tilde{z})) - N_1\left(\dot{\tilde{\eta}} - \frac{dq(\tilde{z})}{d\tilde{z}}\dot{\tilde{z}}\right)$$

Since the power loss of the VSC φ_o is unknown and the parameters are uncertain, the periodic signal $d(t)$ is unknown and cannot be compensated directly by a state feedback. In order to compensate for d, an internal model-based controller can be developed using the theory in [16] and the references therein.

4.3 Output Regulation Theory

Consider a finite-dimensional, time-invariant, linear system which is modeled as

$$\begin{aligned} \dot{x} &= Pw + Ax + Bu \\ e &= Qw + Cx \end{aligned} \tag{4.10}$$

where $x \in \mathbb{R}^n$ is a vector of state variables, $u \in \mathbb{R}$ is a vector of control inputs, $e \in \mathbb{R}$ is a vector of tracking errors and the trajectories of the system are always bounded. Additionally, $w \in \mathbb{R}^s$ is a vector of disturbances and uncertainties governed by

$$\dot{w} = Sw \tag{4.11}$$

where S is a matrix with suitable dimension having all its eigenvalues on the imaginary axis. The controller can be modeled in a general form

$$\begin{aligned} \dot{x_c} &= A_c x_c + B_c e \\ u &= C_c x_c + D_c e \end{aligned} \tag{4.12}$$

where $x_c \in \mathbb{R}^v$ is a vector of controller states. Therefore, the associated closed-loop system is expressed as

$$\begin{bmatrix} \dot{w} \\ \dot{x} \\ \dot{x_c} \end{bmatrix} = \begin{bmatrix} S & 0 & 0 \\ P + BD_cQ & A + BD_cD & BC_c \\ B_cQ & B_cC & A_c \end{bmatrix} \begin{bmatrix} w \\ x \\ x_c \end{bmatrix} \tag{4.13}$$

with output

$$e = Qw + Cx$$

The problem of output regulation is to design a feedback controller to guarantee the closed-loop system is asymptotically stable [16]. If we assume the controller (4.12) is able to solve the problem of output regulation, the real parts of all the eigenvalues of the matrix (4.14) are negative.

$$\begin{bmatrix} A + BD_cD & BC_c \\ B_cC & A_c \end{bmatrix} \tag{4.14}$$

And since the eigenvalues of S are all located on the imaginary axis, the system (4.13) possesses a stable invariant subspace and a center invariant subspace [16]. The center invariant subspace represents a linear map

$$w \mapsto \begin{bmatrix} x \\ x_c \end{bmatrix} = \begin{bmatrix} \Pi \\ \Pi_c \end{bmatrix} w$$

where Π and Π_c are solutions of the Sylvester equation

$$\begin{bmatrix} \Pi \\ \Pi_c \end{bmatrix} S = \begin{bmatrix} A + BD_cD & BC_c \\ B_cC & A_c \end{bmatrix} \begin{bmatrix} \Pi \\ \Pi_c \end{bmatrix} + \begin{bmatrix} P + BD_cQ \\ B_cQ \end{bmatrix} \tag{4.15}$$

Since the controller (4.12) solves the output regulation problem, it is necessary that the pair (Π, Π_c) satisfies $e = Qw + Cx = Qw + C\Pi w = 0$, which leads to $Q + C\Pi = 0$. With this constraint, the Sylvester equation becomes

$$\begin{aligned} \Pi S &= A\Pi + BC_c\Pi_c + P \\ \Pi_c S &= A_c\Pi_c \\ 0 &= C\Pi + Q \end{aligned}$$

Let $\Psi = C_c\Pi_c$, the above equations can be divided into a controller-independent form

$$\begin{aligned} \Pi S &= A\Pi + B\Psi + P \\ 0 &= C\Pi + Q \end{aligned} \tag{4.16}$$

and a controller-dependent form

$$\begin{aligned} \Psi &= C_c\Pi_c \\ \Pi_c S &= A_c\Pi_c \end{aligned} \tag{4.17}$$

The linear equations (4.16) are named as Francis' equation and the existence of a solution (Π, Ψ) is a necessary condition for the solution of the output regulation problem [5].

Let equation (4.18) denote the minimal polynomial of S,

$$d(\lambda) = s_0 + s_1\lambda + \cdots + s_{d-1}\lambda^{d-1} + \lambda^d \tag{4.18}$$

and set

$$T = \begin{bmatrix} \Psi \\ \Psi S \\ \vdots \\ \Psi S^{d-2} \\ \Psi S^{d-1} \end{bmatrix}, \ \Phi = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -s_0 & -s_1 & -s_2 & \cdots & -s_{d-1} \end{bmatrix}, \ \Gamma = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \end{bmatrix}$$

where (Φ, Γ) is an observable pair. Then, T, Φ, and Γ satisfy the equations (4.17) and are expressed as

$$\begin{aligned} \Psi &= \Gamma T \\ TS &= \Phi T \end{aligned} \tag{4.19}$$

The constraints (4.17) guarantee the controller regulate the error to zero in steady-state. And from Francis' equations, the states of the system satisfy the form $x(t) = \Pi w(t)$ as long as the controller solves the output regulation problem. Therefore, this is refereed to the internal model property: any controller that solves the problem of output regulation necessarily embeds a model of the feedforward inputs needed to keep $e(t)$ identically zero [6].

Now, consider a controller formed as

$$\begin{aligned} u &= \Gamma\xi + v \\ \dot{\xi} &= \Phi\xi + Gv \end{aligned} \tag{4.20}$$

where Γ and Φ satisfy (4.19) for certain T, G is a vector that makes $\Phi - G\Gamma$ as a Hurwitz matrix, and v is an additional control. Then, the closed-loop system with plant (4.10) is obtained as

$$\begin{aligned} \dot{w} &= Sw \\ \dot{x} &= Pw + Ax + B(\Gamma\xi + v) \\ \dot{\xi} &= \Phi\xi + Gv \\ e &= Qw + Cx \end{aligned} \tag{4.21}$$

If the controller (4.20) solves the problem of output regulation, there exists a graph of the linear map

$$w \mapsto \begin{bmatrix} x \\ \xi \end{bmatrix} = \begin{bmatrix} \Pi \\ T \end{bmatrix} w$$

If the additional control v is able to drive the states of the system to this graph, the problem of output regulation is solved.

Replacing the states of system (4.21) by their differences

$$\tilde{x} = x - \Pi w, \quad \tilde{\xi} = \xi - Tw$$

then (4.21) becomes

$$\begin{aligned} \dot{\tilde{x}} &= A\tilde{x} + B\Gamma\tilde{\xi} + Bv \\ \dot{\tilde{\xi}} &= \Phi\tilde{\xi} + Gv \\ e &= C\tilde{x} \end{aligned} \tag{4.22}$$

Therefore, to drive the states of the system to the graph is equivalent to stabilizing (4.22) to the equilibrium $(\tilde{x}, \tilde{\xi}) = (0, 0)$. And it is easy to show

that there is always a robust control v to stabilize (4.22) when all zeros of the system (4.23)

$$\begin{aligned} \dot{x} &= Ax + Bu \\ e &= Cx \end{aligned} \tag{4.23}$$

have negative real parts [16].

4.4 Internal Model-Based Controller

Based on the theory discussed above, assume the unknown $d(t)$ is a disturbance and generated by an exosystem. Its dynamic model can be defined as

$$\begin{aligned} \dot{w}(t) = \Phi w(t) &= \begin{bmatrix} S & 0 \\ 0 & S \end{bmatrix} w(t), \\ d(t) = \Gamma w(t) &= \begin{bmatrix} \Gamma_d & 0 \\ 0 & \Gamma_q \end{bmatrix} w(t) \end{aligned}$$

where $w \in \mathbb{R}^{4N+2}$, N denotes the total number of harmonic components to be compensated by the SAF, $\Gamma_d, \Gamma_q \in \mathbb{R}^{1\times(2N+1)}$ are well defined vectors, and $S = blkdiag(S_r) \in \mathbb{R}^{(2N+1)\times(2N+1)}$ with $S_0 = 0$ and

$$S_r = \begin{bmatrix} 0 & r\omega \\ -r\omega & 0 \end{bmatrix}, \quad r \in \{1, \ldots, n\}$$

where r denotes the orders of the harmonic components to be compensated.

Then, an internal model-based controller is defined as

$$\begin{aligned} \dot{\xi} &= \Phi\xi + Q\tilde{x} \\ u &= \Gamma\xi + K\tilde{x} \end{aligned} \tag{4.24}$$

where Q and K are the control gains to be chosen. The variable ξ estimates the disturbance $d(t)$ and its error variable is defined as $\tilde{\xi} = \xi - Lw$. Therefore, the overall error dynamics of the system can be expressed as

$$\begin{aligned} \dot{\tilde{x}} &= \left(M(R, L) - \frac{1}{L}K\right)\tilde{x} - \frac{1}{L}\Gamma\tilde{\xi} + I(\tilde{\eta}, \tilde{z}, \dot{\tilde{\eta}}, \dot{\tilde{z}}) \\ \dot{\tilde{\xi}} &= \Phi\tilde{\xi} + Q\tilde{x} \\ \dot{\tilde{z}} &= \epsilon(\Gamma(\tilde{\xi} + Lw) + K\tilde{x})^T(\tilde{x} + x^* - N_1 q(\tilde{z}) + N_1\tilde{\eta}) \\ \dot{\tilde{\eta}} &= -\epsilon h(\tilde{z}) \end{aligned}$$

With suitably chosen Q and K, the error dynamics should be asymptotically stable. The detailed discussion on calculating Q and K can be found in [22].

4.5 Simulation Results

The introduced control algorithm was simulated with MATLAB/Sumilink. The SAF uses the same values of L and C as our experimental test stand and an uncertain R around 0.21 Ω. The limits on v_{dc} are $V_{dc,m} = 300$ V and $V_{dc,M} = 500$ V which respect the constrains of the physical system. The voltage source generates three-phase voltage with 120 V RMS phase voltage and 60 Hz frequency.

A balanced nonlinear load which is a parallel combination of a rectifier with resistive load and a three-phase RL load is applied to generate current harmonics to the grid. The major harmonic components of the load power are the $6th$ and $12th$.

The control parameters discussed in Section 4.4 have been selected as [22]

$$S = \begin{bmatrix} S_0 & 0 & 0 \\ 0 & S_6 & 0 \\ 0 & 0 & S_{12} \end{bmatrix}, \quad \Gamma_d = \Gamma_q = [1,1,0,1,0]^T, \quad K = \begin{bmatrix} 35 & 0 \\ 0 & 70 \end{bmatrix},$$
$$Q = 10^3 \times \begin{bmatrix} Q_d & 0 \\ 0 & Q_q \end{bmatrix}, \text{ with } Q_d = Q_q = [40.6, 80.7, 7.15, 78.7, 17.6]^T$$

The deadzone function is defined as

$$q(s) = \begin{cases} l_M - l_m & : & s > l_m \\ s - l_m & : & l_m < s \leq l_M \\ 0 & : & |s| \leq l_m \\ s + l_m & : & -l_M \leq s < -l_m \\ l_m - l_M & : & s < -l_M \end{cases}$$

and

$$h(s) = E_{sp} q(s) \frac{dq(s)}{8ds}$$

The line grid current and load current of phase a are presented in Figure 4.3 where i_{la} is the load current and i_{sa} is the line grid current. It is clear that the load current distortion has been greatly reduced and the $6th$ and $12th$ harmonic components have been compensated. The wave form of the compensated grid current is close to being sinusoidal. The tracking performance of the power states x_1 and x_2 is presented in Figure 4.4. The offset between the real power of the SAF and the real power of load is due to the extra power drawn

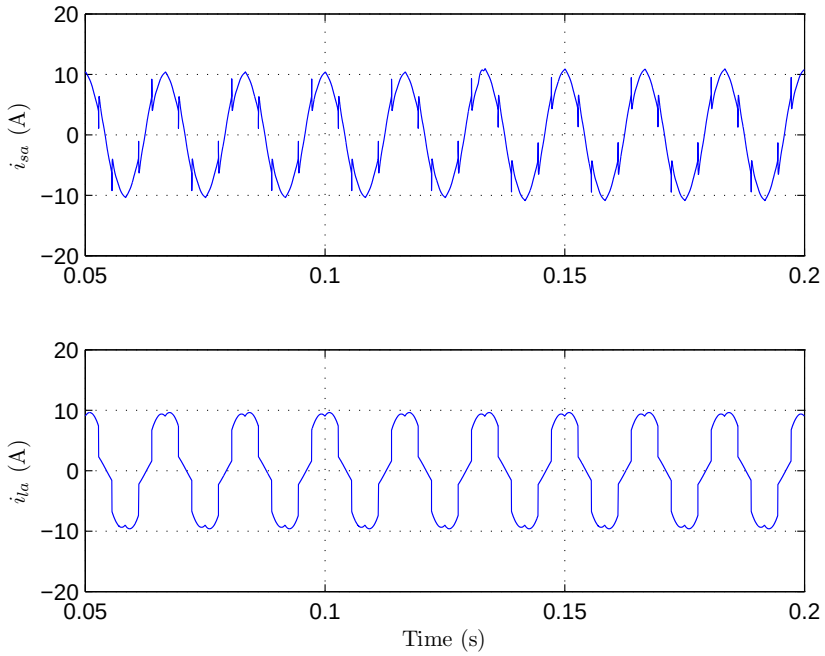


Figure 4.3: Line current and load current of phase a. Although the load current is highly distorted, the compensated main current is almost sinusoidal. The harmonics are successfully compensated by the SAF.

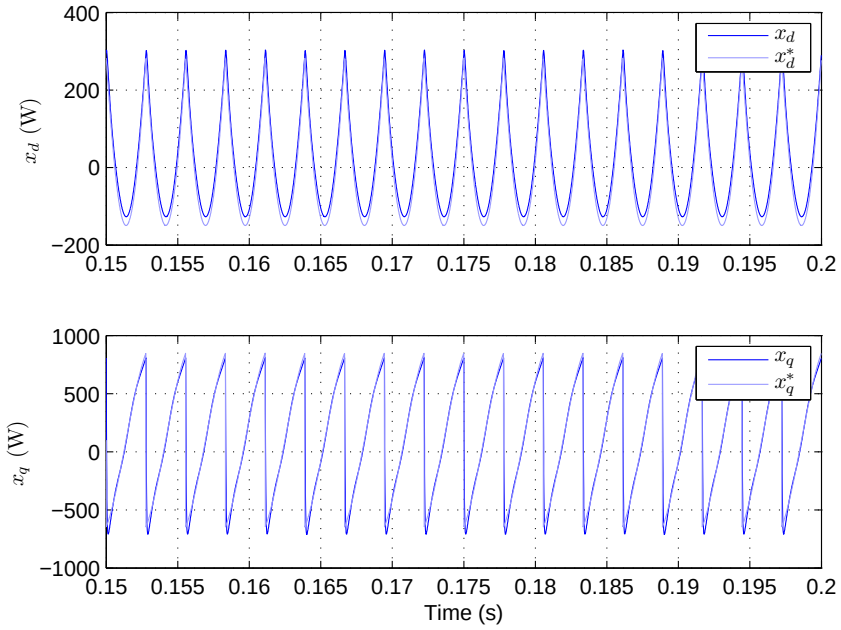


Figure 4.4: Real power and imaginary power of the SAF. The lighter lines are reference signals.

to compensate the SAF losses and maintain v_{dc}. The tracking error of the reactive power of the SAF is negligible, and it still can be reduced by compensating additional harmonic components. Figure 4.5 plots v_{dc}^2. The boundary of squared DC voltage value is set as $V_{dc,m}^2 = 9 \times 10^4$ V and $V_{dc,M}^2 = 2.5 \times 10^5$ V. From the figure, v_{dc}^2 stays in this boundary. Therefore, we conclude the active filtering is achieved using the internal model-based control algorithm.

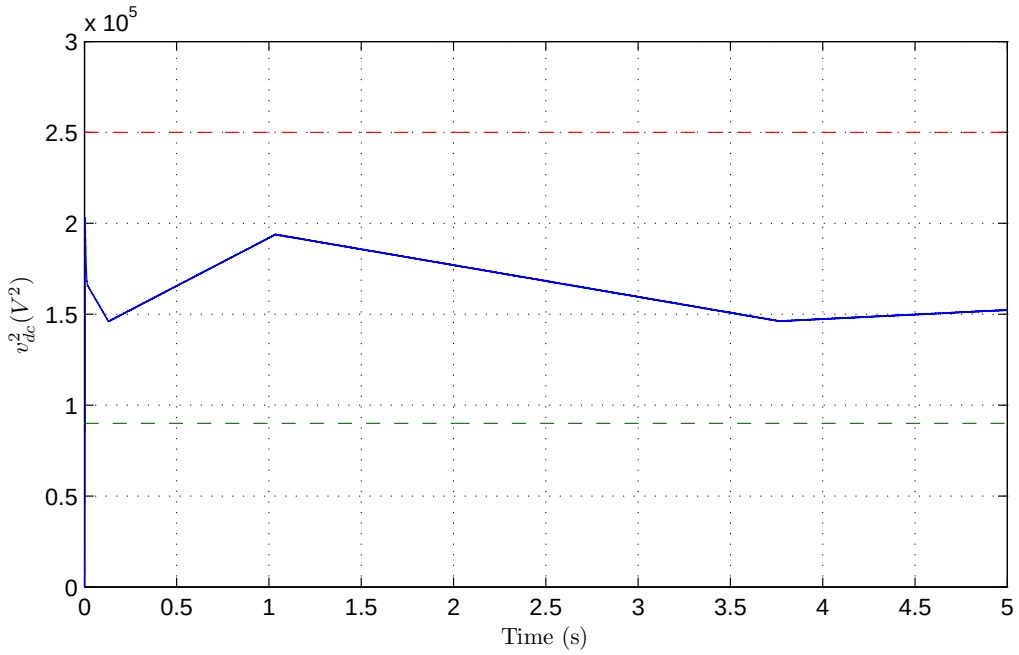


Figure 4.5: Square value of the DC terminal voltage v_{dc}^2. The dashed lines are the boundaries of v_{dc}^2 and it is obvious that v_{dc}^2 fluctuates inside its boundary.

4.6 Summary

In this chapter the VSC system has been used as a SAF to compensate load current harmonics. An internal model-based control algorithm was introduced based on output regulation theory. The controller has been verified via simulation.

Chapter 5

Conclusions

5.1 Summary of Research

This thesis focusses on the implementation of controllers for a three-phase VSC system. For the application of power factor control, the reactive current and DC voltage of the VSC are considered as tracking outputs. A nonlinear control is derived which asymptotically tracks these outputs. A traditional industrial Proportional-Integral (PI) control scheme is implemented on the test stand to compare the performance of the nonlinear control. In addition, we consider the problem of operating the VSC as a shunt active filter to perform VAR compensation and harmonic cancelation.

In chapter two we have derived a mathematical model for the three-phase VSC system in a synchronous reference frame. The nonlinear model possesses 3 states and 2 inputs. A feedback linearization-based control algorithm was introduced. In chapter three, a detailed description of the development and operation of the experimental test stand was provided. Both the feedback linearization-based control algorithm and vector control algorithm are implemented on the system. Based on the experimental performance of the controllers, we conclude that the nonlinear control can effectively be used for power factor control. In the fourth chapter, the VSC has been considered as a SAF to compensate load current harmonics. A VSC system model which uses real and imaginary power coordinates was derived and an internal model-based control algorithm was introduced. The control algorithm was verified by simulation based using parameters for the test stand.

5.2 Future Work

With the established experimental test stand, the system can be used to compensate VAR and harmonics. Since the issue of control input saturation was not explicitly addressed, appropriate theory could be developed to account for this effect. The test stand is ready to be used as a benchmark for control algorithm development. For example, an adaptive backstepping-based control under development would be a natural choice [24]. Although the system operates properly, the test stand can still be further optimized by modifying external circuit boards and the rewriting certain parts of the controller software. These modifications could lead to better performance through faster sampling times, for example.

Bibliography

[1] H. Akagi, Y. Kanazawa, and A. Nabae. Instantaneous reactive power compensators comprising switching devices without energy storage components. *IEEE Transactions on Industry Applications*, 20(3):625–630, May 1984.

[2] B. M. Bird, K. G. King, and D. A. G. Pedder. *An Introduction to Power Electronics*. John Wiley and Sons, New York, 1993.

[3] B. K. Bose. *Modern Power Electronics and AC Drives*. Prentice Hall, Upper Saddle River, New Jersey, 2002.

[4] dSPACE GmbH. *Installation and Configuration Reference for Hardware Components of a Modular System*. dSPACE GmbH, Paderborn, Germany, 2003.

[5] B. A. Francis. The linear multivariable regulator problem. *SIAM Journal on Control and Optimization*, 15(3):486–505, Nov. 1976.

[6] B. A. Francis and W. M. Wonham. The internal model principle of control theory. *Automatica*, 12(5):457–465, Sept. 1976.

[7] M. E. Fraser, C. D. Manning, and B. M. Wells. Transformerless four-wire pwm rectifier and its application in ac-dc-ac converters. *IEE Proceedings - Electric Power Applications*, 142(6):410–416, Nov. 1995.

[8] A. Gensior, J. Rudolph, and H. Güldner. Flatness based control of three-phase boost rectifiers. In *11th European Conference on Power Electronics and Applications Rec., EPE 2005*, Dresden, Germany, Sep. 2005.

[9] S. I. GmbH. *Application Note of SEMISTACK-IGBT*. SEMIKRON International GmbH, Germany, 2005.

[10] R. Grunbaum. Voltage source converters for maintaining of power quality and stability in power distribution. *2005 European Conference on Power Electronics and Applications*, pages 10–20, Aug. 2005.

[11] L. Gyugyi. Unified power-flow control concept for flexible AC transmission systems. *Generation, Transmission and Distribution, IEE Proceedings C*, 139(4):323–331, Jul. 1992.

[12] A. Hadri-Hamidaa, A. Allagb, M. Y. Hammoudib, S. M. Mimouneb, S. Zeroualib, M. Ayadc, M. Becherifc, E. Milianic, and A. Miraouic. A nonlinear adaptive backstepping approach applied to a three phase pwm accdc converter feeding induction heating. *Communications in Nonlinear Science and Numerical Simulation*, 14(4):1515–1525, Apri. 2009.

[13] P. Horowitz and W. Hill. *The Art of Electronics*. Cambridge University Press, Cambridge, 1989.

[14] Y. Hu, C. Zhe, and H. McKenzie. Voltage source converters in distributed generation systems. *Third International Conference on Electric Utility Deregulation and Restructuring and Power Technologies*, pages 2775–2780, May 2008.

[15] L. R. Hunt and R. Su. Linear equivalents of nonlinear time-varying systems. In *International Symposium on the Mathematical Theory of Networks and Systems*, pages 119–123, Santa Monica, CA, 1981.

[16] A. Isidori and L. Marconi. *Lecture Notes of Short Course on Asymptotic Tracking and Disturbance Rejection*. University of Stuttgart, Stuttgart, 2010.

[17] B. Jakubczyk and W. Respondek. On linearization of control systems. *Bulletin de L'Academie Polonaise des Sciences, Série des Sciences mathématiques*, 28(1):517–522, 1980.

[18] P. Krause, O. Wasynczuk, and S. Sudhoff. *Analysis of Electric Machinery and Drive Systems*. John Wiley and Sons, New York, 2002.

[19] P. C. Krause and C. H. Thomas. Simulation of symmetrical induction machinery. *IEEE Transactions on Power Apparatus and Systems*, 84(11):1038–1053, Nov. 1965.

[20] R. Krishnan, S. Y. Park, and K. Ha. Theory and operation of a four-quadrant switched reluctance motor drive with a single controllable switch. 41(4):1047–1055, Aug. 2005.

[21] L. Marconi, F. Ronchi, and A. Tilli. Robust control of shunt active filter based on the internal model principle. *Proceedings of American Control Conference*, 5:3943–3948, Jun. 2003.

[22] L. Marconi, F. Ronchi, and A. Tilli. Robust nonlinear control of shunt active filters for harmonic current compensation. *Automatica*, 43(2):252–263, Aug. 2006.

[23] P. Mattavelli. A closed-loop selective harmonic compensation for active filter. *IEEE Transactions on Industry Applications*, 37(1):81–89, Aug. 2001.

[24] R. Milasi, A. Lynch, and Y. Li. Adaptive control of a voltage source converter. *Proceedings of the 23rd Canadian Conference on Electrical and Computer Engineering*, May 2010.

[25] M. H. Rashid. *Power Electronics Circuits, Devices, and Applications*. Prentice Hall, New York, 2003.

[26] J. Salmon. *Power Electronics Notes*. University of Alberta, Edmonton, 2009.

[27] F. Sargos. Application note of igbt power electronics teaching system principle for sizing power converters. *Semikron*, Sept. 2008.

[28] C. Schauder and H. Mehta. Vector analysis and control of advanced static var compensators. *Generation, Transmission and Distribution, IEE Proceedings C*, 140(4):299–306, Jul. 1993.

[29] E. Song, A. F. Lynch, and V. Dinavahi. Experimental validation of nonlinear control for a voltage source converter. *IEEE Transactions on Control System Technology*, 17(5):1135–1144, Sept. 2009.