Nanofabrication of a CMOS Compatible Device For Macro-to-Atom Interfacing

by

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Abstract

Advancements in scanning tunneling microscopy (STM) have enabled atomic-scale lithographic patterning of logic gates, memory, and wires, by selectively passivating hydrogen (H) atoms on a H-terminated silicon (Si) surface. However, atomically fabricated systems encounter challenges of developing from research labs into commercial applications. This thesis focuses on developing a complementary metal-oxide semiconductor (CMOS) compatible process flow to nanofabricate a device capable of injecting and making signal measurements between CMOS and atomic circuitry; a macro-to-atom device.

The design of the macro-to-atom device is capable of withstanding the high-temperature flashing required to prepare an area of H-terminated Si. By isolating the high-temperature flashing to a small area at the center of the device, damage to any prefabricated CMOS circuitry can be prevented. An initial design utilized tungsten-silicide (W-Si) conduction lines on a heavily-doped Si substrate to connect between the atomic and CMOS circuitry. However, the high-temperature surface preparation caused metal particulates to contaminate the center region where atomic circuitry would be fabricated, which could impede atomic circuit functionality. The high-temperature surface preparation also caused thin conduction lines to coagulate causing discontinuities. Another disadvantage to the initial device was that deposited W-Si on the Si surface increases the risk of STM tip crashing, as the surface is no longer flat. This would also make patterning continuous DB wires closely connecting to the W-Si conduction wires difficult.

To circumvent these issues, a device using heavily-doped arsenic (As) conduction lines on a lightly-doped silicon substrate is to be utilized instead. Fabrication and testing of the device has been separated into three individual components to isolate and address development issues. The first component focuses on the main design and nanofabrication process flow of the bulk of the macro-to-atom device, and ensuring the process flow remains contaminant free. The second component focuses on the contact junctions that would directly interface with

the atomic circuitry. By patterning atomic circuitry between the junctions, transport measurements are enabled that help further understand how the conductive contacts interact with the atomic circuitry and perturb the transmission spectra. The third component focuses on implanting a heavily-doped antimony (Sb) reservoir under the surface where atomic-scale lithography would occur, to provide the STM with the required carriers for low temperature operation and surface dangling bonds (DBs) with the required charge state. Once all components of the device are further realized, the three components can then be implemented together as a single macro-to-atom device.

Preface

The thesis presented was performed under the supervision of Dr. Robert Wolkow between September 2018 and August 2020 in the Department of Physics at the University of Alberta, Canada. The work presented is an extension and refinement of a device designed and developed by Dr. Bruno Martins; I developed and fabricated the ion implanted arsenic (As) version of the device. I performed all device nanofabrication except ion implantation using available tools from the nanofabs located in the National Research Council of Canada Nanotechnology Research Centre and the Electrical and Computer Engineering Research Facility at the University of Alberta. Ion implantation was done externally at CuttingEdge Ions, a specialized semiconductor ion implantation company based in California.

With copyright permission, Fig. 1.1d, 3.8a, and 3.13b have been reproduced or adapted from references [1], [2], and [3] respectively. All other figures are originally created or photographed. With copyright permission, Tab. 4.2 has been adapted from reference [4].

Experimental scanning tunneling microscope (STM) analysis and images for identifying surface contamination on the macro-to-atom device in Fig. 4.13a, 4.13b, 4.14a, and 4.14b was collected by Dr. Hedieh Hosseinzadeh. Experimental STM analysis and imaging in patterning a dangling bond (DB) wire between two titanium (Ti) contacts on Si in Fig. 4.15b,c was collected by Dr. Jo Onoda. Parameters for ion implantation and annealing of the macro-to-atom device were calculated by Dr. Gregory Snider. Secondary ion mass spectroscopy (SIMS) data used in the analysis of Fig. 4.19 were collected by the University of Alberta Nanofab characterization/sample analysis team.

"I have not failed.
I've just found 10,000
ways that won't work."

Thomas A. Edison

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Lastly, I could not be where I am today without the love and support of my friends and family. To my mom, who has demonstrated to be the very definition of hard work and sacrifice. Although after all these years you still think I am studying "phys-ed", I hope I have made you proud. To my sister, who has provided me with unending support and most importantly, many great meals. To my uncle, who has been at the forefront of supporting and encouraging my interests and career my entire life. To my friends, thank you for the laughter, a shoulder to cry on, and everything in between. Thank you for the unforgettable memories created and making this journey an absolute joy.

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List of Symbols and Abbreviations

Symbols and Units

α	Fitting parameter for determining band gap	eV/K
β	Fitting parameter for determining band gap	K
ΔR	Straggle	nm
$\hbar$	Planck's constant	$4.136 \cdot 10^{-15} eV \cdot s$
Φ_B	Built-in potential	eV
Φ_M	Metal work function	eV
ρ	Resistivity	$\Omega \cdot cm$
d	Length	m
E_B	Binding energy	eV
E_C/E_V	Lowest/highest energy level of the conduction/valence band	eV
E_D/E_A	Donor/acceptor energy level	eV
$E_{F,i}$	Fermi energy of an intrinsic semiconductor	eV
E_F	Fermi energy	eV
E_G	Band gap	eV
$f_{FD}(E)$	Fermi-Dirac distribution function	
$g_C(E)/g_v(E)$	Density of states in the conduction/valence band in 3D	$m^{-3} eV^{-}1$
k_B	Boltzmann constant	$8.617 \cdot 10^{-5} eV \cdot K^{-1}$
m_e^*/m_h^*	Electron/hole effective mass	kg

$n(E)/p(E)$	Electron/hole concentration	cm^{-3}
n_0/p_0	Electron/hole concentration at thermal equilibrium	m^{-3}
N_C/N_V	Effective density of states in the conduction/valence band	m^{-3}
N_D/N_A	Concentration of donor/acceptor atoms	$ions \cdot cm^{-3}$
n_i	Intrinsic electron/hole concentration	cm^{-3}
P	Pressure	$Torr$
R_P	Projected range	nm
T	Temperature	K, $°C$
X_{Si}	Electron affinity for silicon	eV

Element Abbreviations

Ar	Argon
As	Arsenic
B	Boron
C	Carbon
Cr	Chromium
Ge	Germanium
H	Hydrogen
Hg	Mercury
O	Oxygen
P	Phosphorous

Pt	Platinum
Sb	Antimony
Si	Silicon
Ti	Titanium
W	Tungsten

Compound Abbreviations

C_4F_8	Octafluorocyclobutane
CO_2	Carbon dioxide
DNQ	Diazonaphthoquinone
H_2	Molecular hydrogen
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
HF	Hydrofluoric acid
$HMDS$	Hexamethyldisilazane
N_2	Dinitrogen
NH_3	Ammonia
NH_4F	Ammonium fluoride
O_2	Molecular oxygen
OH	Hydroxyl
$PMMA$	Polymethyl methacrylate

SF_6	Sulfur hexafluoride
$Si(100)2x1:H$	Hydrogen-terminated silicon (100) with a 2x1 reconstruction
SiH_4	Silane
SiO_2	Silicon dioxide
$SiOH$	Silanol
$W-Si$	Tungsten-silicide

Abbreviations

(D)RIE	(Deep) reactive ion etching
(E)UV	(Extreme) ultraviolet
(LT-)/(MP-) STM	(Low Temperature-)/(Multi-probe-) Scanning tunneling microscope
(PE)CVD	(Plasma enhanced) chemical vapour deposition
AFM	Atomic force microscope
BOE	Buffered oxide etch
BOX	Buried oxide
CAD	Computer-aided design
CB	Conduction band
CMOS	Complementary metal oxide semiconductor
DB	Dangling bond
DOS	Density of states
EBL	Electron beam lithography

FA	Furnace anneal
IC	Integrated circuit
IR	Infrared
LOR	Liftoff resist
MEIS	Medium energy ion scattering
MEMS	micro-electromechanical systems
PVD	Physical vapour depositon
RTA	Rapid thermal anneal
SEM	Scanning electron microscope
SIMS	Secondary ion mass spectroscopy
SOI	Silicon-on-insulator
UHV	Ultra-high vacuum
VB	Valence band

01
Introduction

1.1 Background and Motivation

The 1930 patent and design of Lilienfeld and Heil's transistor is regarded as one of the most revolutionary inventions of the 20th century, the backbone of progress and advancements in modern scientific research [5, 6]. Jack Kilby created the first printed circuit in 1958, and alongside the emergence of optical lithographic and dopant diffusion techniques, enabled the mass production and commercialization of integrated circuits (ICs), which then initiated the information age [7]. Optical lithography provided an economical method to fabricate ICs, providing a high wafer throughput with minimal defects [8]. Although initially motivated by militaristic demands in achieving satellite and missile superiority, the miniaturization of complex electronic systems has now been assimilated into every aspect of society and everyday living [7]. ICs of the '60s contained less than a hundred components. However, in following Moore's law of doubling transistor density on an IC every 18 - 24 months, devices of today, such as an average smartphone, have transistor counts in the billions [9].

The miniaturization of electronics was seemingly straightforward; IC performance and speed increased while simultaneously decreasing material and fabrication costs [6]. The increasingly smaller nanoscale dimensions of transistors have been directly attributed to advancing lithographic patterning techniques, such as immersion lithography and exposure with shorter

and shorter wavelengths, to extreme ultraviolet (EUV) [6, 9]. However, as scaling trends entered the nanoscale regime, electron tunneling and short channel effects hindered the momentum previously sustained by Moore's law. Over the last several years, components on an IC are doubling every 24 - 36 months, rather than every 18 - 24 months as was previously accomplished. As the semiconductor industry struggles to preserve Moore's law due to the bottleneck of physical limitations, alternative technologies beyond complementary-metal-oxide-semiconductor (CMOS) has surged in interest.

Our understanding of many scientific fields relies on our tools to observe and characterize samples. A major limitation of optical microscopes was the diffraction limit of light, which limited the imaging of features to no larger than 1 μm [10, 11]. However, this was mitigated with Gerd Binnig and Heinrich Rohrer's 1981 invention of the scanning tunneling microscope (STM), which awarded them the 1986 Nobel Prize in Physics [10, 11]. This also enabled the emergence of other scanning probe techniques such as the atomic force microscope (AFM), which together propelled our understanding and advancements achieved in surface physics. The STM was initially used to image a sample's surface topography and resolve the surface's electronic states with atomic resolution, but it now has the capability to manipulate and move surface atoms [12, 13]. Here in the Wolkow group, we perform atomic-scale lithographic patterning to manipulate individual atoms on a hydrogen (H)-terminated silicon (Si) surface to fabricate atomic wires, logic gates, and memory [1, 14]. Atomic circuitry is revolutionary in its ability to potentially continue Moore's Law in that they utilize the smallest spatial resolution physically achievable of a single atom [1, 14, 15]. This provides the benefits of fabricating significantly denser circuitry, while having the possibility of being more energy efficient [1, 14].

However, despite the control achieved with STMs, there are several challenges for atomic circuitry [16, 17]. In order for a transition to occur from research labs to industry, we must overcome the challenge of making reliable connections between the atomic circuitry and current CMOS technologies [15]. Si provides an avenue for the direct integration of atomic circuitry into

CMOS technologies, as Si is already the most utilized material in semiconductor technologies and allows a process flow compatible with typical nanofabrication facilities [9].

One consideration in the process flow is contamination, which could hinder the intended function of the atomic circuitry when working in the nanoscale regime [9, 18]. The nanofabrication facilities we work in are classified as class 100 cleanrooms, which means that less than 100 particles larger than 0.5 µm, and less than 3500 particles larger than 0.1 µm are airborne in one cubic foot [3, 19]. Although fabrication inside a class 100 cleanroom ensures minimal environmental contamination, contamination comes mainly from fabrication processes [3]. The many steps required for fabricating the device inherently yields defects, with contamination arising from limitations in equipment performance, materials evaporating from chamber walls, or chemical vapours from wet benches. Process flow design for the nanofabrication of the device must therefore be robust and optimized to minimize surface contamination.

Another consideration for the fabrication process flow is the power the device would use. Although transistors have reduced in size, power per transistor has not commensurately lowered [6]. As a result, overall power density which is proportional to thermal energy has been steadily increasing. The majority of device failure mechanisms hindering performance and reliability are thermally activated. This includes dopant diffusion between layers, creep, and fatigue of interconnects. Therefore, to take full advantage of the low power consumption capability of atomic circuitry, power dissipation within the bulk of the device must also be minimized.

Therefore, our challenge is to create a unique device design that allows for signal measurements to be made between CMOS and atomic circuitry; a macro-to-atom device. The design and process flow must be compatible with fabrication in a conventional cleanroom while keeping the surface free of contamination. Any prefabricated CMOS circuitry must also be able to survive the harsh surface preparations required to prepare an area of pristine H-terminated Si surface for atom-scale lithographic patterning [1, 14, 20].

1.2 Initial Device

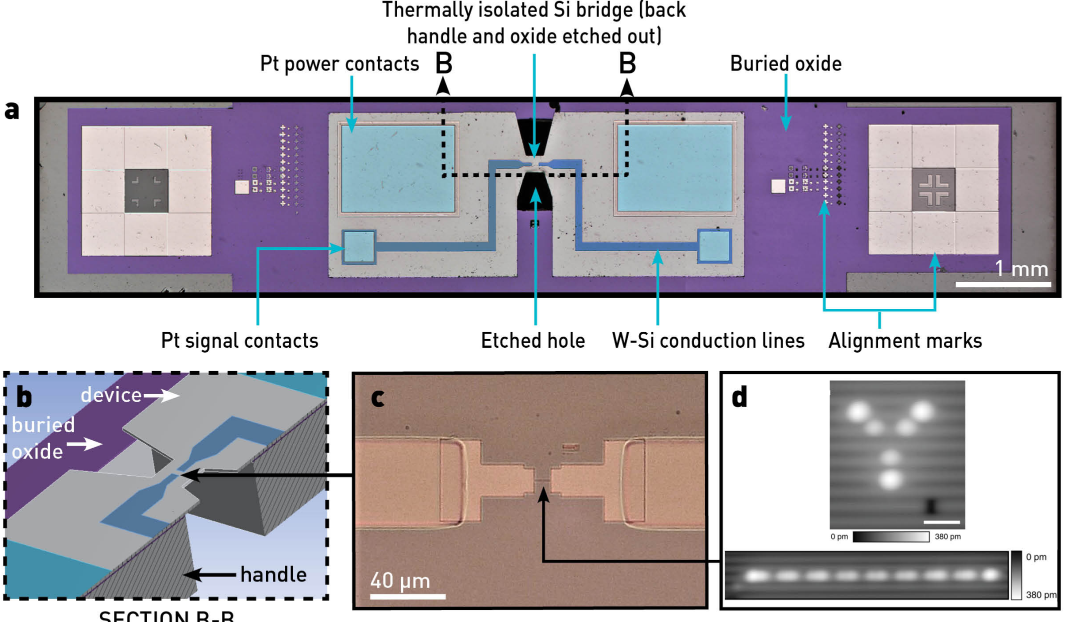
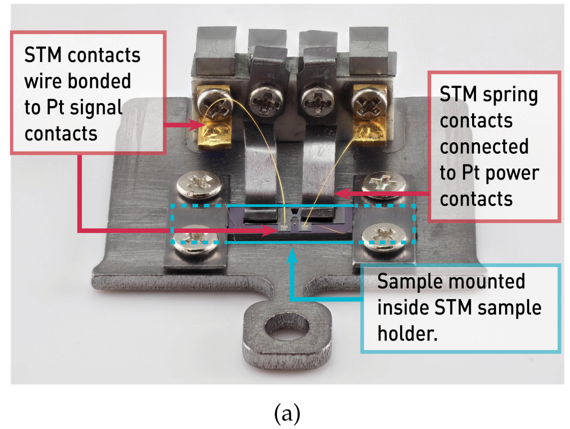
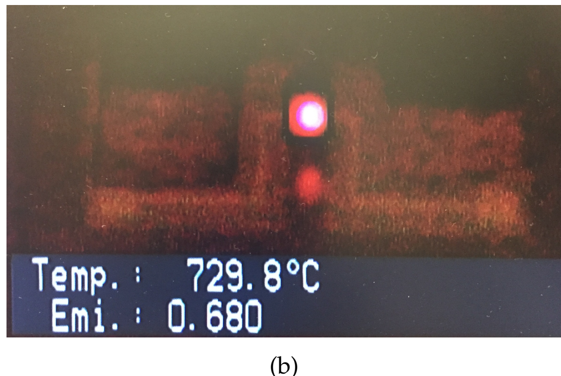


Figure 1.1 – **(a)** Schematic of the initial tungsten-silicide (W-Si) macro-to-atom device. The photo is colourized to differentiate the materials on the device. **(b)** Cross-section cutout of the thermally isolated Si bridge from (a). **(c)** Zoom in of the center of the W-Si conduction lines. Between the W-Si contacts is a 300 nm gap. **(d)** Atomic circuitry is planned to be fabricated on a hydrogen (H)-terminated Si surface between the 300 nm gap. Adapted from "Binary atomic silicon logic" by Huff et al., 2018, Nature Electronics 9. Copyright 2018, by permission of Springer Nature [1].

An initial prototype of the macro-to-atom device was designed by a postdoctoral fellow in the Wolkow group, which has since been refined into the device shown in Fig. 1.1a. The device is fabricated on a heavily-doped n-type silicon-on-insulator (SOI) substrate, which consists of a buried oxide (BOX) layer bonded between a heavily-doped device (top) and handle (bottom) layer as shown in the cross-section cutout in Fig. 1.1b. With traditional bulk Si substrates, metal silicide on the surface can react with the Si and leak into the bulk, causing unwanted



(a)



(b)

Figure 1.2 – **(a)** Tungsten-silicide (W-Si) macro-to-atom device clipped in and wire bonded to a scanning tunneling microscope (STM) sample holder. **(b)** STM surface preparation of the W-Si macro-to-atom device via high temperature flashing. Heating is isolated at the center as indicated by the bright red glow. The dimmer red glow below is a reflection.

leakage currents [21]. The advantage of utilizing SOI is that the BOX layer minimizes leakage currents to those through the thin active device layer [21, 22]. Other properties of SOI wafers, such as decreased parasitic capacitance and increased output conductance, provides increased device performance over traditional Si wafers, making them more widely adopted for use in semiconductor devices [21]. Most importantly for the macro-to-atom device, the thick back handle layer of Si conducts away heat, and provides support and robustness to the ultra-thin BOX and device layers [23].

The dimensions of the device (2.55 mm x 12.05 mm, thickness of 250 µm) were specified to fit inside an STM sample holder as shown in Fig. 1.2a. As seen in the figure, the spring connections of the STM sample holder are in direct contact with the device's large platinum (Pt) power contacts. In applying a bias voltage to the Pt power contacts using the spring connections, the current is concentrated in the thermally isolated Si bridge of high resistance at the center of the device. This results in local heating to temperatures as high as 1050 °C for only approximately

1 second. Heating is isolated in the center as shown in Fig. 1.1c while the rest of the device remains virtually unheated as observed in Fig. 1.2b. The tapered center area is a free-standing Si bridge where the back handle and oxide layers are etched out behind, preventing thermal dissipation to the bulk substrate. Far less power is required to reach high temperatures locally while also avoiding heating of surrounding areas. This allows for CMOS circuitry that would be fabricated at a later stage to remain undamaged during surface preparation for atomic-scale lithography. The local high-temperature cleaning of the bridge yields a pristine center such that the surface can be readily passivated with H, and atomic-scale lithographic patterning can be subsequently performed [1, 14].

The center region as shown in Fig. 1.1c contains tungsten-silicide (W-Si) conduction lines that taper down to 200 nm wide contacts. Two such conduction lines converge in the center interface leaving a 300 nm gap where atomic circuitry such as that shown in Fig. 1.1c,d would be fabricated. The smaller contacts (Fig. 1.1c) are the intermediate contacts that allow for the "macro-to-atom scale" connection; scaling between atomic circuitry and larger conduction lines. Narrowing the gap to 300 nm also helps accommodate the STM patterning window for efficient atomic patterning [16]. Pt signal contacts sit overtop the ends of the W-Si conduction lines, such that they can be wire bonded to external contacts for signal injection and measurements as shown in Fig. 1.2a. Pt is utilized as the contact electrodes as it allows for direct wire bonding, allowing connections between CMOS and atom-scale portions of the hybrid circuit [24]. Additionally, Pt has good resistance to corrosion and oxidation, making it a reliable material choice for metallic interconnects in semiconductor devices.

1.3 The Scanning Tunneling Microscope

In an STM, a scanning tip is attached to three orthogonal piezoelectric transducers, one for each directional axis [10]. While applying a bias voltage to the sample, the tip is brought within picometers of the surface to be imaged such that the overlap of surface and tip wave functions generate tunneling conductance. Images can be obtained through two different scanning modes [10, 25].

In scanning with "constant height mode" as illustrated in Fig. 1.3a, the lateral distance between the tip and sample is fixed. As the tip scans in a plane parallel to the sample at a constant bias, the tunneling current varies as surface topography varies and is recorded to build the STM image. Due to a lack of feedback control, scanning can be done with much higher speeds. However, this also increases the probability of STM tip crashes, reserving this imaging mode for very flat and small areas.

In "constant current mode" as illustrated in Fig. 1.3b, a feedback loop uses the tunneling current to apply voltage to drive the z-piezo, allowing a contour plot of the surface to be obtained as the STM scans the plane for variations in local state density. STM operation is most commonly utilized in this scanning mode, as it can be used on any surface topography [10].

1.3.1 Sample Preparation for Scanning Tunneling Microscopy

To prepare a sample in the STM for atomic-scale lithographic patterning, the STM sample chamber is first brought to ultra-high vacuum (UHV) [1, 12, 14, 20]. The sample can be exposed to UV activated ozone to deteriorate organic contaminants on the surface into volatile compounds, resulting in a cleaner surface. The sample is then brought to 300 °C and left to degas, removing adsorbed water from the sample's surface and from the holder. Degassing is typically done overnight for regular samples. However, because the area of interest on the macro-to-atom device is so small, it only takes approximately 15 min. In applying a bias voltage to the large Pt

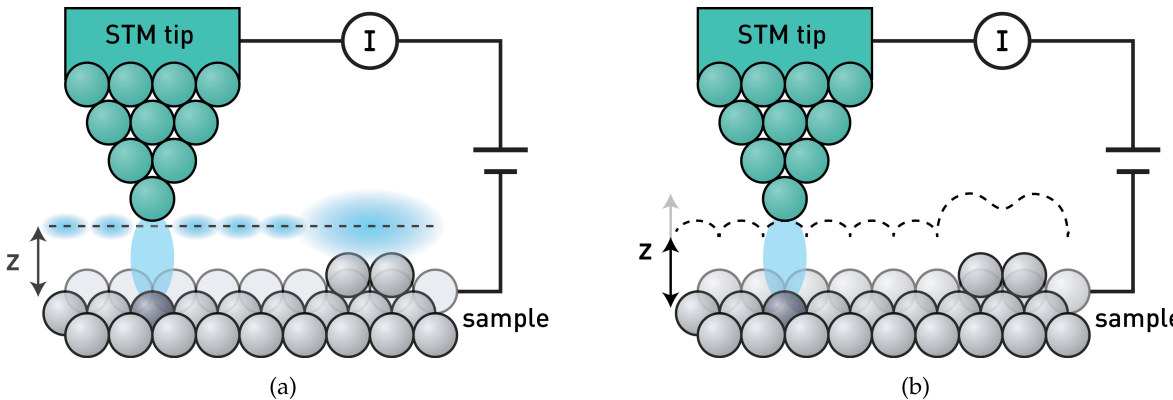


Figure 1.3 – Scanning tunneling microscope (STM): **(a)** In constant height mode. **(b)** In constant current mode.

contact pads connected to the sample holder's spring connections, the sample is flashed several times to heat the surface at very high temperatures measured with a calibrated pyrometer. The sample reaches temperatures as high as ~800 to 1050 °C to remove the native protective oxide from the Si surface. Heating is isolated at the center as observed in Fig. 1.2b. Each surface Si atom has one dangling bond (DB), and through a subsequent H-termination process, each DB becomes the attachment point for one H atom [1, 12, 14, 20]. To accomplish H-termination, the chamber is filled with pure molecular H_2 gas. A W filament heated to 1900 °C cracks the molecular H_2 to form atomic H that reacts with DBs on the bare Si surface, forming a H monolayer.

Atomic-scale lithographic patterning is accomplished by selectively depassivating the H-terminated Si (100) surface (Si (100) 2x1: H) with an atomically sharp tip of a UHV-STM or AFM [1, 14, 15]. A voltage pulse applied to the STM tip dissociates the Si-H bond. The H atom attaches to the tip and a DB remains on the Si surface. That tip-attached H atom can be subsequently controllably deposited to repassivate an unoccupied DB site. In creating a DB, a well-defined energy state is introduced into the Si (100) 2x1: H band gap (E_G) [16]. The DB's energy level lies approximately at the midpoint of Si's E_G, allowing it to be substantially isolated from the conduction band (CB) and valence band (VB), and exhibit zero-dimensional properties like a quantum dot [16, 26]. A linear array of DBs can be utilized as a conducting

wire. The electronic states are localized to the surface DBs, allowing electrons to hop from one DB to the next, preventing contact with the Si's bulk states [17].

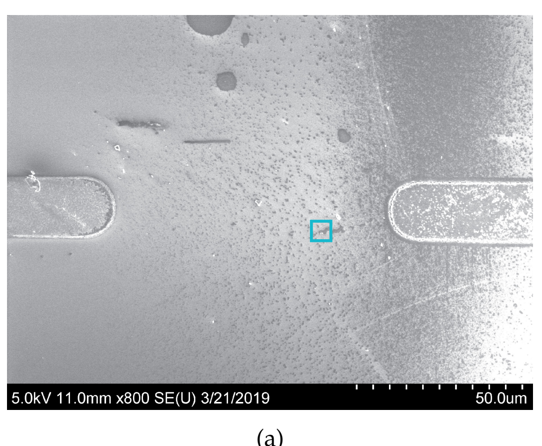
While H atoms can be removed from the surface at room temperature, employing cryogenic conditions in a low-temperature (LT)-UHV STM decreases the thermal drift between the tip and sample [1, 14]. This allows for far greater control to be achieved. These advancements in STM capability and efficiency have been enormously enhanced by implementing machine learning methods in enabling the automation of tip reconditioning following damage sustained on the tip from atomic-scale lithographic patterning [27]. The controlled creation and passivation of DBs have together allowed writing and editing of the desired atom defined patterns.

1.4 Initial Device Issues

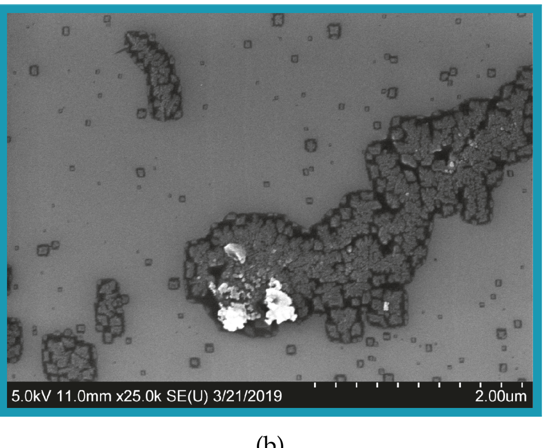
1.4.1 Tungsten-Silicide Contacts

W is superior to other metals in high-temperature applications, due to its high-temperature stability and high melting point [28]. W-Si thin films are also widely used in microelectronics due to the formation of a protective surface layer, preventing damaging oxidation at high temperatures [29]. Despite these attractive properties and the sufficiency of W in many standard applications, scanning electron microscope (SEM) images showed that high-temperature surface preparation caused W particulates to contaminate the center where atomic circuitry would be fabricated as shown in Fig. 1.4. Such defects may well exist in larger scale applications, but because of the scale of the defects, be insignificant in these other applications. The W contaminants several orders of magnitudes larger in size than a single DB could severely impede circuit functionality or cause STM tip crashes when performing atomic-scale lithography [16].

To accommodate the small STM patterning window, the gap between the two W-Si conduction lines is narrowed down to 300 nm. To scale between the atomic circuitry and larger



(a)

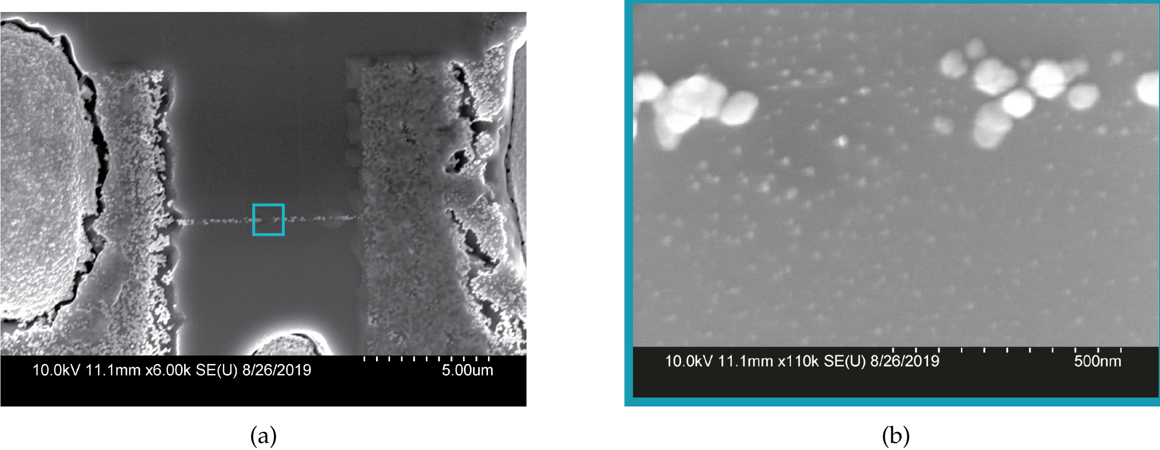


(b)

Figure 1.4 – Scanning electron microscope (SEM) images of the tungsten-silicide (W-Si) macro-to-atom device after after several ~1000 °C flashes. **(a)** At the center of the macro-to-atom device, the W-Si conduction lines narrow down to 20 µm in width and leaves a 75 µm gap in between. **(b)** Zoom in of the center of (a). Metal islands contaminate the center region of interest where atomic circuitry would be fabricated.

conduction lines, the W-Si conduction lines taper down to contact wires that are 200 nm in width. Upon flashing the sample, these thin W-Si contact wires coagulate into metal islands causing discontinuities in the contact wires as shown in Fig. 1.5.

Another big challenge lies in the interface between the DB circuitry and electrical contacts [16, 17]. The interface of two different materials will inherently yield unavoidable defects [30]. Due to Fermi level pinning at the metal-semiconductor junction, localized states are created which traps charges. In the nanoscale regime, these non-uniformities of the surface could have a critical effect on the surrounding circuitry and can disturb the behavior of electron transport.



(a) (b)

Figure 1.5 – Scanning electron microscope (SEM) images of the tungsten-silicide (W-Si) macro-to-atom device's 300 nm gap after several ~1000 °C flashes. **(a)** At the center of the macro-to-atom device, the W-Si conduction lines narrow down to 300 nm in width and leaves a 300 nm gap in between. **(b)** Zoom in of the center of (a). Metal contamination pollutes the center region of interest where atomic circuitry would be fabricated. Additionally, the W-Si contact wires no longer appear continuous due to the coagulation of metal particles from high temperature flashing.

1.4.2 Current Leakages

Although atomic circuitry would utilize minimal power to operate, the bulk of the heavily-doped Si is conductive and creates undesired pathways [1, 14]. However, a heavily-doped substrate is required for low-temperature STM (LT-STM) operation such that there are sufficient carriers for tunneling between the sample and tip [10]. The low resistivity (ρ) of the Si bulk poses a challenge in limiting leakage currents and power dissipation. Considering the large circuit density that could be made possible through atomic-scale lithographic patterning, the issue of power density and dissipation perpetuates even more critically [14].

1.4.3 Scanning Tunneling Microscope Tip Landing

While STM imaging, the tip has a risk of crashing into the Si surface which could damage or deform the tip [31]. Lateral positioning of the STM tip on a sample is very challenging, and tip crashing can occur during the coarse approach. An added benefit of the W-Si conduction lines is visibility. With the W-Si device, the metal reflections as shown in Fig. 1.6 help an operator guide manual STM tip landing, allowing the STM tip to get very close to the sample's surface relatively quickly. Without any guidance or fiducial marks, the process could be very troublesome in risking tip crashes, or very time consuming if the automated tip landing is initialized too soon with the tip still substantially distant from the surface.

However, the 35 nm thick layer of deposited W-Si increases the risk of STM tip crashes. As the atomic circuitry needs to be patterned closely to the W-Si conduction lines for electrical homogeneity, the STM tip has a high risk of crashing into the edges of the W-Si conduction lines as it approaches. As a result of tip damage, images can no longer be accurately produced with atomic resolution, and we can no longer accomplish atomically precise lithographic patterning [31].

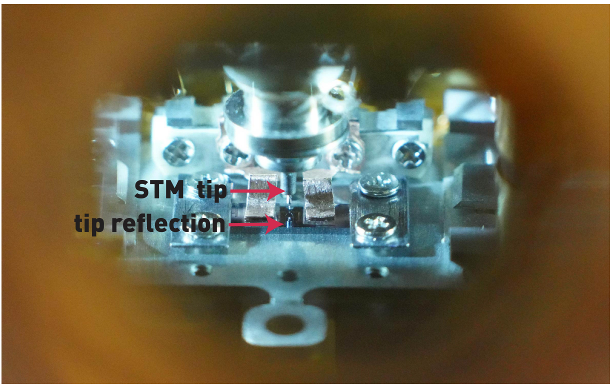


Figure 1.6 – Scanning tunneling microscope (STM) tip approaching the surface of the tungsten-silicide (W-Si) macro-to-atom device. The reflection of the tip on the W-Si conduction lines aid the operator in centering and coarse approaching with the STM tip towards the surface.

1.5 The Focus of This Thesis

To circumvent the current limitations of the macro-to-atom device, heavily-doped implanted arsenic (As) conduction lines (n-type) on a lightly-doped n-type SOI substrate are planned as a replacement for the W-Si conduction lines on a heavily-doped n-type SOI substrate. As the dopants are implanted into the Si substrate itself, and no additional materials are present around the center area subjected to high-temperature flashing, the presence of metal contaminants would be eliminated. The Pt power and signal contacts remain sufficiently distant from where high temperature heating is concentrated to prevent metal contamination. The majority of previous STM experiments utilize bare, unfabricated heavily-doped Si for atomic-scale lithographic patterning, ensuring surface contamination should not be present upon flashing the heavily-doped contacts [1, 14]. As no additional material sits above the surface plane, this could also help minimize STM tip crashes from scanning across the planar surface, as was always an obstacle with the topography created by the deposited metal contacts [25].

Greatly reducing the dopant concentration from a heavily-doped to lightly-doped bulk of the device also greatly reduces undesired current pathways. Lightly-doped Si experiences "carrier-freezeout" at LT-STM operation, with liquid nitrogen (N) (77.2 K), or liquid helium (He) (4.2 K) [1, 32]. The STM operates at cryogenic temperatures to provide the thermal stability required for precision in atomic-scale lithographic patterning. As the bulk becomes non-conductive due to the lack of free carriers, only the conduction lines carry current, denying leakage currents in the bulk. However, this benefit also poses a disadvantage, in that STM operation requires tunneling of free carriers between tip and substrate to operate [25]. Additional modifications to the device must be made to provide the free carriers required for STM operation.

This thesis is devoted to describing the technologies and processes used in developing a macro-to-atom device, and subsequent challenges experienced by fabricating the prototype. By introducing the fundamentals of semiconductor physics (Ch. 2) and the fundamentals of nanofabrication techniques (Ch. 3), the thesis then collects the described methods into a refined process flow used in prototyping the device (Ch. 4). The chapter also presents the shortcomings in the design of the macro-to-atom device and fabrication in the first prototype. The final chapter (Ch. 5) describes the remaining obstacles on the project and the future outlook on overcoming the challenges of realizing a fully functioning macro-to-atom device.

02 Physics of Semiconductors

2.1 Semiconductor Properties

The advent of semiconductor technologies has been attributed to revolutionary processing techniques, which allowed for the ultra-refinement of semiconductors such as germanium (Ge) and Si [6, 33]. Refining other materials to contain very low impurity and defect concentrations were difficult to achieve. Solid-state devices were initially fabricated by diffusing dopants into ultra-pure Ge crystals but were replaced by Si for its more attractive material properties. Si's wider E_G means conductivity from thermal carriers is not as much of an interference compared to Ge, allowing Si to have a larger range in operating temperatures [34]. Additionally, Si's ability to easily form silicon dioxide (SiO_2), a high-quality native insulator, could be utilized as an effective dopant mask unlike Ge's water soluble oxide [34–36]. The ability to incorporate impurities to methodically tailor a semiconductors' electronic properties over a wide range has allowed the continual miniaturization of Si technology.

2.1.1 Intrinsic Semiconductors

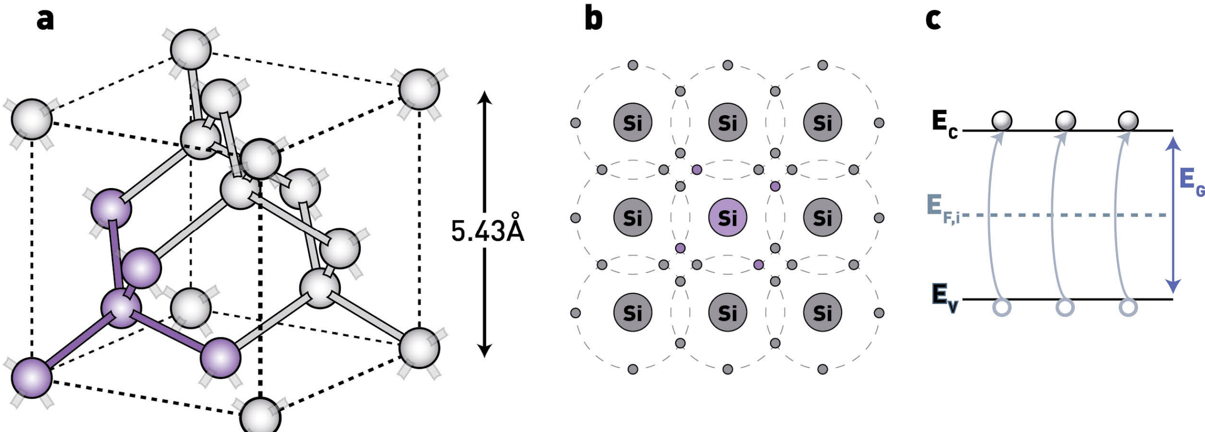


Figure 2.1 – Intrinsic silicon (Si). **(a)** Crystal lattice: each Si atom is covalently bonded to each of its four nearest neighbors. **(b)** 2D representation of (a). **(c)** Energy diagram; electrons with sufficient thermal energy are promoted across the band gap (E_G) leaving behind a hole in the valence band (VB).

When a semiconductor's properties are exclusively characterized by its band structure, and its impurity concentration is so low that those do not contribute to its electrical properties, it is classified as an intrinsic semiconductor [32, 33, 37]. The tetrahedral diamond structure of Si as illustrated in Fig. 2.1a allows each atom to have four nearest neighbors, where it shares its four valence electrons to form stable covalent bonds as illustrated in Fig. 2.1b. The stability of these covalent bonds gives rise to a substantial E_G, making it difficult for electrons to be excited into the CB from the VB at low temperatures. As shown in Fig. 2.1c, the Fermi energy for an intrinsic semiconductor ($E_{F,i}$) sits approximately halfway between the highest energy level of the VB (E_V) and the lowest energy level of the CB (E_C), showing that no electrons at 0 K will have sufficient thermal energy to jump across E_G. However, as temperatures increase, some electrons are thermally excited across E_G into the CB, leaving behind holes in the VB and allowing electrical conduction [38].

E_G of Si at room temperature is 1.12 eV, however, E_G decreases as temperature increases [37]. The temperature dependence of E_G can be expressed as

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta} \tag{2.1}$$

where $E_G(0)$ is E_G at 0 K, and α and β are experimentally determined fitting parameters, which for Si are determined in Tab. 2.1 [37, 38].

Table 2.1 – Experimentally determined parameters to calculate the band gap (E_G) of silicon (Si) as a function of temperature.

$E_G(0)(eV)$	$\alpha(eV/K)$	$\beta(K)$
1.1695	4.73 E-04	636

⋆ **Data obtained from [38].**

2.1.2 Extrinsic Semiconductors

The conductivity of a semiconductor can be altered with the addition of acceptor group III (boron (B)) or donor group V (phosphorous (P), As, antimony (Sb)) elements [33]. In substituting a Si atom with a group V element that has five valence electrons, only four electrons are used for covalent bonding as shown in Fig. 2.2a. The extra electron is loosely bound to its nucleus with a binding energy (E_B) at least several orders of magnitude smaller than E_G as illustrated in Fig. 2.2b. The electron is thus ionized easily, promoting it from its donor energy level (E_D) into the CB and assisting in electrical conduction. The excess electrons from the donor atoms characterize it as an n-type semiconductor.

In the same regard, substituting with a group III atom that has only three valence electrons, creates a localized vacancy or hole as shown in Fig. 2.2c [33]. If sufficient thermal energy is provided to promote an electron from VB to acceptor energy level (E_A), a mobile hole is created in the VB, and assists in hole conduction as shown in Fig. 2.2d. The excess holes created from the acceptor atoms characterize it as a p-type semiconductor.

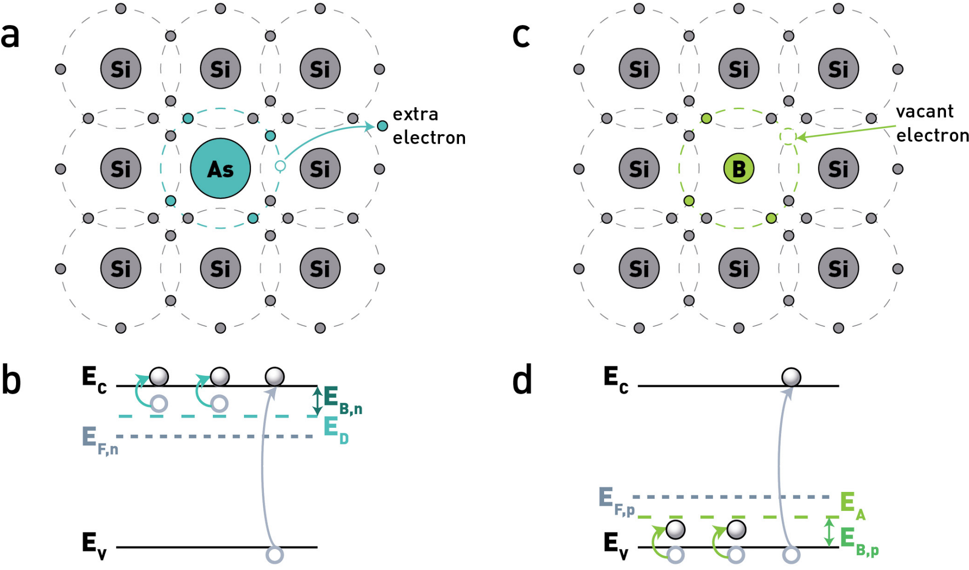


Figure 2.2 – **(a)** 2D illustration of an n-type silicon (Si) crystal. The arsenic (As) atom has five valence electrons, only four of which are covalently bonded with Si. **(b)** Energy diagram of an n-type semiconductor. Extra electrons from donor atoms occupy donor energy levels (E_D). As this is near the lowest energy level of the conduction band (E_C), the electrons are only loosely bound with a small binding energy ($E_{B,n}$). Electrons can be easily promoted from E_D into E_C, providing an excess of electrons for conduction. **(c)** 2D illustration of a p-type Si crystal. The boron (B) atom only has three valence electrons, leaving a vacancy. **(d)** Energy diagram of a p-type semiconductor. Extra electrons from acceptor atoms occupy acceptor energy levels (E_A). As this is near the highest energy level of the valence band (E_V), the electrons are only loosely bound with a small binding energy ($E_{B,p}$). Electrons can be easily promoted from E_V into E_A, leaving behind excess holes for conduction.

2.2 Carrier Concentrations in Equilibrium

Pivotal to understanding how semiconductor devices operate is in first obtaining its current-voltage characteristics, which are defined by the concentration of free carriers present [33]. The concentration of electrons ($n(E)$) occupied in the CB is defined by

$$\begin{aligned} n(E) &= g_c(E) f_{FD}(E) \\ &= \left(\frac{\sqrt{2} {m_e^*}^{\frac{3}{2}} \sqrt{E - E_C}}{\hbar^3 \pi^2} \right) \left(\frac{1}{1 + e^{(E-E_F)/k_B T}} \right) \end{aligned} \tag{2.2}$$

where $g_c(E)$ is the CB's density of states (DOS), $f_{FD}(E)$ is the Fermi-Dirac distribution function which defines the probability of quantum state occupancy, m_e^* is the electron's effective mass, and E_F is the Fermi energy which defines the energy at which there is a 50% probability of finding an electron at any given temperature [37, 38].

Similarly, the concentration of holes ($p(E)$) occupied in the VB can be calculated to be

$$\begin{aligned} p(E) &= g_v(E)(1 - f_{FD}(E)) \\ &= \left(\frac{\sqrt{2} {m_h^*}^{\frac{3}{2}} \sqrt{E_V - E}}{\hbar^3 \pi^2} \right) \left(1 - \frac{1}{1 + e^{(E-E_F)/k_B T}} \right) \end{aligned} \tag{2.3}$$

where g_v is the VB's DOS, and m_h^* is the hole's effective mass [37].

2.2.1 Non-Degenerate Semiconductors

When a semiconductor is lightly- to moderately-doped, the electrons in the CB and holes in the VB act as non-degenerate carrier gases; classifying the semiconductor as non degenerate [32]. In n-type non-degenerate semiconductors, this is when E_F is more than $3k_BT$ below E_C [32, 38]. Therefore the $f_{FD}(E)$ can be approximated with Boltzmann statistics and the concentration of

electrons in the CB at thermal equilibrium (n_0) can then be evaluated as

$$\begin{aligned} n_0 &\approx \int_{E_C}^{\infty} \left(\frac{\sqrt{2} {m_e^*}^{\frac{3}{2}} \sqrt{E - E_C}}{\hbar^3 \pi^2} \right) \left(\frac{1}{e^{(E_F - E)/k_B T}} \right) dE \\ &= N_C \cdot exp \left(\frac{E_F - E_C}{k_B T} \right) \end{aligned} \tag{2.4}$$

where N_C is defined as the effective DOS for the CB, and is described by [32, 33, 37]

$$N_C = 2 \left(\frac{2 \pi m_e^* k_B T}{h^2} \right)^{3/2} \tag{2.5}$$

Rewriting Eq. 2.4, E_F can be defined as [37]

$$E_F = E_C + k_B T ln \frac{n_0}{N_C} \tag{2.6}$$

Likewise, a p-type non-degenerate semiconductor is when E_F is more than $3k_B T$ above E_V. The concentration of holes in the VB at thermal equilibrium (p_0) is found to be

$$\begin{aligned} p_0 &\approx \int_{-\infty}^{E_V} \left(\frac{\sqrt{2} {m_h^*}^{\frac{3}{2}} \sqrt{E_V - E}}{\hbar^3 \pi^2} \right) \left(1 - \frac{1}{e^{(E_F - E)/k_B T}} \right) dE \\ &= N_V \cdot exp \left(\frac{E_V - E_F}{k_B T} \right) \end{aligned} \tag{2.7}$$

where N_V is defined as the effective DOS for the VB, and is described by [32, 33, 37]

$$N_V = 2 \left(\frac{2 \pi m_h^* k_B T}{h^2} \right)^{3/2} \tag{2.8}$$

Rewriting Eq. 2.7, E_F can be defined as [37]

$$E_F = E_V - k_B T ln \frac{p_0}{N_V} \tag{2.9}$$

2.2.2 Degenerate Semiconductors

In degenerate semiconductors where carrier concentrations are greater than the effective DOS, $f_{FD}(E)$ can no longer viably be approximated with Boltzmann statistics [32]. The Joyce-Dixon approximation can be used instead, defining E_F for degenerate n-type semiconductors as [37].

$$E_F \approx E_C + k_B T \left(ln \frac{n_0}{N_C} + \frac{1}{\sqrt{8}} \frac{n_0}{N_C} \right) \tag{2.10}$$

Similarly for degenerate p-type semiconductors, E_F is defined as [37].

$$E_F \approx E_V - k_B T \left(ln \frac{p_0}{N_V} + \frac{1}{\sqrt{8}} \frac{p_0}{N_V} \right) \tag{2.11}$$

If the last term for Eq. 2.10 and Eq. 2.11 is neglected, then the results are respectively identical to Eq. 2.6 and Eq. 2.9; E_F for non-degenerate semiconductors using the Boltzmann approximation [37].

2.2.3 Intrinsic Semiconductors

For undoped semiconductors, E_F lies approximately halfway between E_G [37]. By equating the E_F for non-degenerate semiconductors, Eq. 2.6 and Eq. 2.9

$$E_F = E_{F,i} = \frac{E_C + E_V}{2} + \frac{k_B T}{2} ln \frac{N_V}{N_C} \tag{2.12}$$

E_F for intrinsic semiconductors can be found [37].

The intrinsic carrier concentration (n_i) can also be inferred with the mass action law [37]

$$n_0 \cdot p_0 = N_c N_v e^{(E_v - E_c)/k_B T} = n_i^2 \tag{2.13}$$

2.2.4 Charge Neutrality

Carriers can be redistributed between energy bands and dopant levels, but their concentration must be conserved [32]. By equating the density of negative charges which include n_0 and ionized acceptor atoms (N_A^-), with the density of positive charges which include p_0 and ionized donor atoms (N_D^+), we can define the charge neutrality condition as [37].

$$n_0 + N_A^- = p_0 + N_D^+ \tag{2.14}$$

2.2.5 Temperature Dependence of Carrier Concentrations

All doped components of the device under study here including the substrate itself is n-type. Thus, the following analysis of the temperature dependence of carrier concentrations focuses on the case of $N_A = 0$, and $N_D \neq 0$. The concentration of N_D^+ is then defined as [32]

$$N_D^+ = N_D(1 - f_{FD}^*(E_D)) \tag{2.15}$$

As the energy for E_D and E_F become closer together, the Fermi distribution function for donor levels ($f_{FD}^*(E_D)$) has to be factored in since its degeneracy has to be accounted for. $f_{FD}^*(E_D)$ can be defined by [32]

$$f_{FD}^*(E_D) = \frac{1}{\frac{1}{2} \cdot e^{\left(\frac{E_G - E_B - E_F}{k_B T}\right)} + 1} \tag{2.16}$$

Eq. 2.15 can then be expressed as [32]

$$N_D^+ = N_D \frac{n_1}{n_0 + n_1} \tag{2.17}$$

where

$$n_1 = \frac{1}{2} N_C \cdot e^{\left(\frac{-E_B}{k_B T}\right)} \tag{2.18}$$

Using Eq. 2.13 and Eq. 2.17, Eq. 2.14 can then be rewritten to [32]

$$\begin{aligned} n_0 + N_A^- &= p_0 + N_D^+ \\ n_0 + 0 &= \frac{n_i^2}{n_0} + N_D \frac{n_1}{n_0 + n_1} \end{aligned} \tag{2.19}$$

By multiplying Eq. 2.19 by n_0^2, we can turn it into the homogeneous equation [32]

$$n_0^3 + n_1 n_0^2 - (n_i^2 + n_1 N_D) n_0 - n_i^2 n_1 = 0 \tag{2.20}$$

Three real solutions can be obtained from considering the limiting cases of Eq. 2.20. In establishing three distinct regions as shown in Fig. 2.3, the temperature limits for ideal semiconductor device operation can be identified [32, 37, 38].

1. **Intrinsic Region** $(\mathbf{N_D \ll n_i})$:

   This condition applies to significantly high temperatures well over 1000 °C, and thus the only real solution to Eq. 2.20 is if $n_0 = n_i$ [32]. At high temperatures, thermally excited carriers outnumber carriers liberated from dopants, therefore the doped semiconductor behaves identically to an intrinsic semiconductor [37].

2. **Saturation Region** $(\mathbf{N_D \gg n_i, N_D \ll n_1})$:

   This condition applies to lightly- or moderately-doped semiconductors at relatively high temperatures [32]. Eq. 2.20 shows at these conditions, $n_0 = N_D$; almost all donor atoms are ionized, and the carrier concentration is maximized in the CB. Conductivity in this

region is independent of temperature, thus most semiconductor devices operate within this region.

3. **Freeze-out Region** $(\mathbf{N_D \gg n_i, N_D \gg n_1})$:

   This condition applies to lightly- or moderately-doped semiconductors at low temperatures. At low temperatures, there is insufficient thermal energy to fully ionize dopants, therefore carrier concentration is no longer equivalent to the dopant concentration [32]. As previously mentioned, a non-degenerate semiconductor is defined as having E_F less than $3k_BT$ from an allowed band [38]. This is because the change from $f_{FD}(E) = 0$ to $f_{FD}(E) = 1$ arises within an energy range of $+3k_BT$ to $-3k_BT$. Therefore, in lightly- or moderately-doped semiconductors ($\sim 1.45 \cdot 1 \cdot 10^{10}$ - 10^{18} $ions \cdot cm^{-3}$) where E_F is more than $3k_BT$ from an allowed energy band, there is a very small probability that some states are filled in the CB, and some states are vacant in the VB at low temperatures. Carriers remain bound to donors, thus provides no carrier contribution to the CB.

   In increasing dopant concentration, E_F is brought closer to either the CB or VB depending on dopant species [32]. Further increasing the dopant concentration can bring E_F into an allowed band, defining the semiconductor as degenerate or heavily-doped [38]. At large dopant concentrations, the interatomic spacing between dopant atoms is so close that the wave functions of individual dopant levels overlap and combine into one single impurity band. As the distinction between allowed bands and localized states are blurred, n_0 becomes independent of temperature, and $E_B = 0$. The carriers do not experience a freeze-out, and the semiconductor remains conductive even at low temperatures.

Temperature Dependence of Carrier Concentrations in the Macro-to-Atom Device

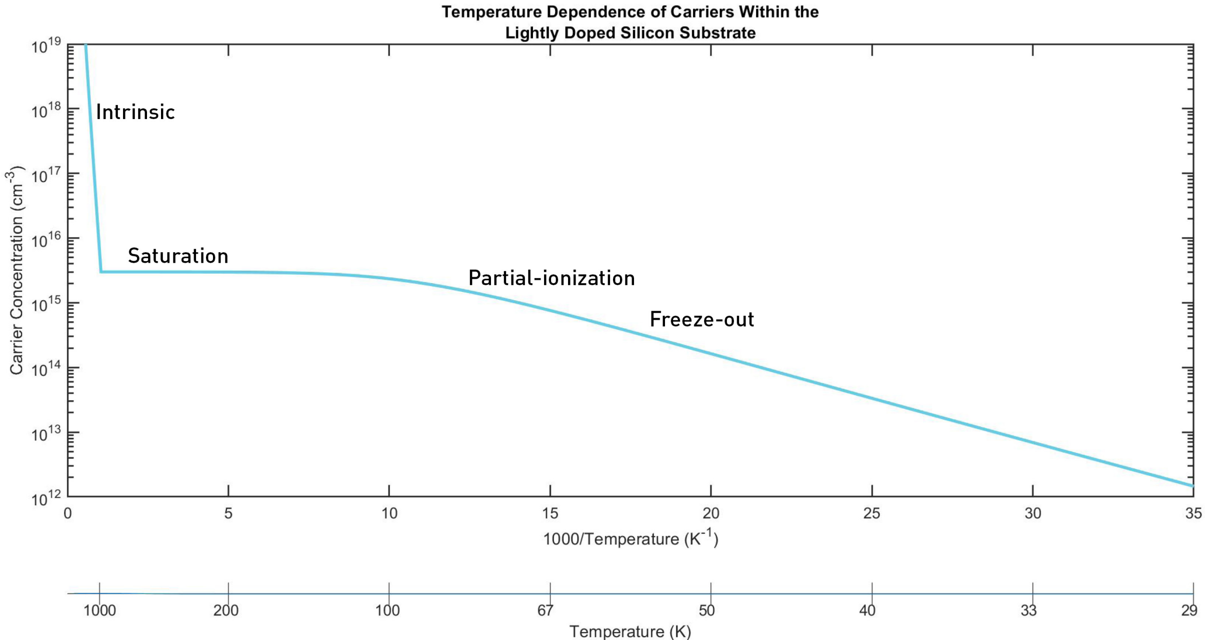


Figure 2.3 – The carrier concentration of the lightly-doped n-type silicon (Si) substrate (bulk of the macro-to-atom device) with a dopant concentration (N_D) of $3 \cdot 10^{15}$ $ions \cdot cm^{-3}$ as a function of temperature.

Selected properties of various n-type regions of the the macro-to-atom device are presented in Tab. 2.2. Using the values for the lightly-doped Si bulk of the device from Tab. 2.2, the temperature dependence of the carrier concentration is calculated, with the results presented in Fig. 2.3. Details of the function and purpose of each dopant region will be explained in detail in Ch. 4. Although the saturation region is the focus of most semiconductor manufacturers, this project focuses on device operation in the freeze-out region [32]. This is because STM operation at the cryogenic temperatures of liquid He (4.5K) and liquid N (77.2K) provides the thermal stability required for atomic-scale lithographic patterning [1, 14].

From Fig. 2.3, it can be seen that the substrate experiences carrier freeze-out at temperatures below ~100 K. As the surface of the macro-to-atom device will no longer be conductive, this

Table 2.2 – The concentration of donor atoms (N_D) on various n-type regions of the macro-to-atom device.

Dopant	**Area of Device**	$N_D(ions \cdot cm^{-3})$	$E_B(meV)$
P	Bulk substrate	$3 \cdot 10^{15}$ (lightly-doped)	45.5*
As	Conduction lines	$3 \cdot 10^{19}$ (heavily-doped)	–
Sb	Embedded center region	~$1 \cdot 10^{19}$ (heavily-doped)	–

* **Only the lightly-doped region has a value for its binding energy (E_B) as the heavily-doped regions have $E_B = 0$. Data for E_B of P obtained from [39].**

poses an obstacle for the STM operating at cryogenic temperatures. Using the temperature dependence of E_G from Eq. 2.1, alongside the E_F of degenerately and non-degenerately doped semiconductors from Eq. 2.6 and Eq. 2.10, E_F for each doped region on the device as a function of temperature is calculated with the data provided in Tab. 2.2 and shown in Fig. 2.4. The heavily-doped As and Sb regions show E_F within the CB at temperatures nearing 0 K, allowing these regions to be conductive for STM operation at cryogenic temperatures [38]. E_F is also shown to decrease as temperature increases, due to the doped areas becoming increasingly intrinsic.

Only n-type semiconductors are handled within the project, however, analogous results can be similarly inferred and applied to p-type semiconductors [33, 37].

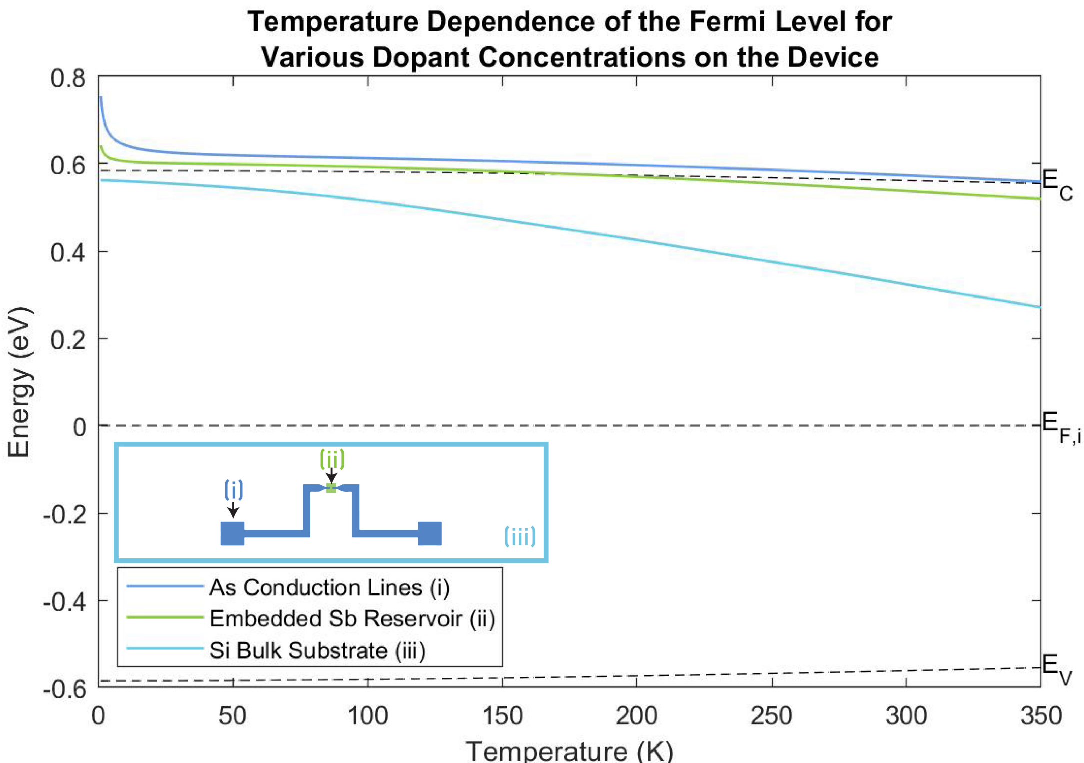


Figure 2.4 – Fermi energies (E_F) of the various n-type doped regions on the macro-to-atom device as a function of temperature. Heavily-doped regions have E_F above the lowest energy level of the conduction band (E_C) of silicon (Si), providing electrical conductance even near 0 K temperatures.

03

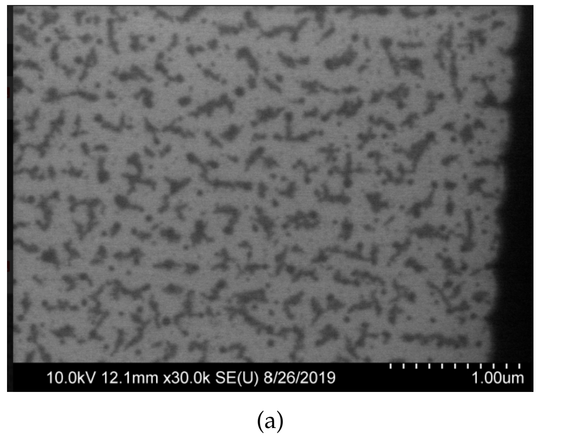
Fundamentals of Nanofabrication

3.1 Introduction

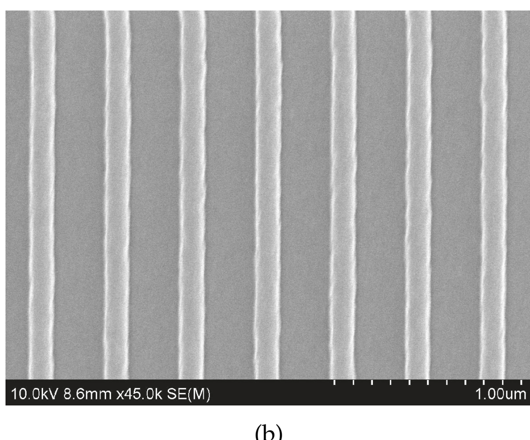
Although nanofabrication has tremendous capabilities, it also has many practical industry limitations, which are only better understood in obtaining hands-on experience for every step and technique used within the device process flow. Many obstacles of the process flow are overlooked during the design stage, as each lithographic step has to accommodate previous and subsequent layers in material and fabrication tool compatibility [19]. Rarely does the conceptualized design translate flawlessly into a final product, but experience and understanding with each nanofabrication technique allow for the concept design to be best completed.

An example of the deviation of concept to successful fabrication is highlighted in the nanofabrication of a simple 200 nm striped pattern using electron-beam lithography (EBL) as shown in Fig. 3.1. Although not a part of the macro-to-atom device, it was fabricated to aid in adjusting creep from the piezoelectric actuators used in the STM [10]. EBL had been previously successful in patterning 200 nm features on the metal-silicide devices and even has the capabilities for patterning sub-10 nm features [40]. However, it could not create the desired pattern due to a common issue known as an "electron-beam proximity effect" which is further described in Sec. 3.5.7 [40–42]. Backscattered electrons caused unwanted exposure of areas meant to remain exposure-free. This occurred in regions where the pattern features were too closely spaced

together, which caused features to merge together and thus rendering the striped pattern completely illegible after development as shown in Fig. 3.1a. After nine design iterations and trials in adjusting EBL parameters, such as increasing the accelerating voltage of the beam from 10 kV to 15 kV and decreasing the exposure dosage from 100 $\mu C \cdot cm^{-2}$ to 60 $\mu C \cdot cm^{-2}$, the deceptively simple pattern was at last successfully fabricated as shown in Fig. 3.1b. Understanding the limitations of each lithographic technique also helps in overcoming its shortcomings. The nanofabrication techniques highlighted in this chapter encompass the methods used in the prototyping of the macro-to-atom device.



(a)



(b)

Figure 3.1 – Scanning electron microscope (SEM) images of electron-beam lithography (EBL) fabricated samples. **(a)** The intended pattern design was stripes of 100 nm lines. However, electron-beam proximity effects rendered the pattern illegible after pattern development. **(b)** Same design as (a), but with 200 nm stripes instead. Additional calibration of EBL parameters helped resolve the pattern.

3.2 Cleanroom

Due to the nanoscale of our device features, even the most minimal amount of contamination can be very detrimental [19]. Nanofabrication is performed in a meticulously controlled environment known as a cleanroom as shown in Fig. 3.2. The nanofabs at the University of Alberta are class 100 cleanrooms, meaning less than 100 particles larger than 0.5 µm and less than 3500 particles larger than 0.1 µm are airborne in one cubic foot [3, 19]. Disturbances of any kind are minimized by eliminating mechanical vibrations, fluctuations in humidity and temperature, and having personnel wear protective gowns and equipment. Environmental cleanliness is so exceptional, that the main contamination sources are contributed by the fabrication processes and equipment themselves.

Figure 3.2 – Workers in the University of Alberta Nanofab's class 100 cleanroom.

The pattern development section inside the cleanroom is akin to a darkroom for photography, but because the photoresist is sensitive to wavelengths below 450 nm, yellow light is used

in place of red safe light [3].

3.3 Lithography

Lithography first requires a spin coating of resist sensitive to the type of radiation used for exposure onto the substrate. Optical lithography is performed by exposing the photosensitive resist to UV light through a photomask, where opaque regions of the mask block incoming light and creates a pattern in the exposed areas of photoresist [3, 43]. EBL is a maskless lithography method that exposes resist with a highly focused electron-beam [40, 44]. In any university nanofab, EBL has a much higher resolution than optical lithography. In state of the art commercial nanofabs, high-resolution optical lithography methods are used, but those capabilities are beyond the budget of any university. Although EBL has a significantly higher resolution and smaller feature size capability in comparison to optical lithography, it is slower in production efficiency, making the prevailing patterning method for large-scale production still optical lithography [5]. The multiple steps required in performing lithography are illustrated and summarized in Fig. 3.3.

The limitations of lithographic feature sizes are determined by the wavelength of exposing radiation; shorter wavelengths provide higher resolution features [9]. Mercury (Hg)-vapour lamps providing near-UV light radiation with spectral peaks at 365, 405, and 436 nm, have been the dominant radiation source of lithography for several decades, and is the radiation source available at our nanofab [3, 9, 43]. However, in commercial nanofabs, they have been replaced over the years by deeper UV radiation sources and immersion lithography, which involves replacing the gap of air between the lens and wafer in an optical lithography aligner with a high refractive index fluid [44]. Advancing lithographic techniques remains the prominent driving force for sustaining Moore's law, which is one of the biggest infrastructure costs in nanofabrication [9]. A single current state of the art optical lithography aligner capable of exposing and

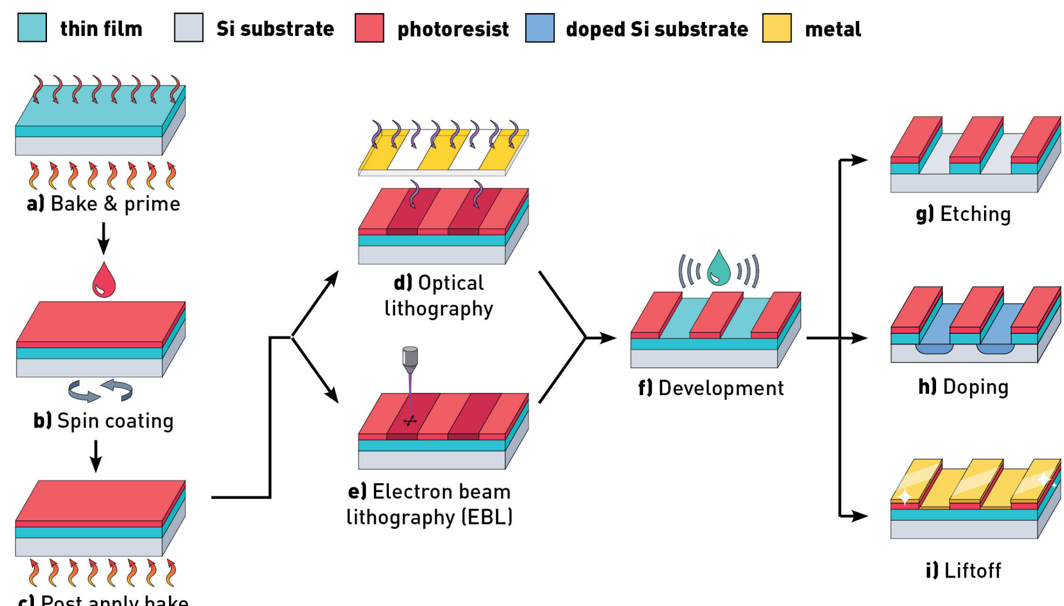


Figure 3.3 – Schematic illustration of the basic steps performed to achieve a positive lithographic pattern transfer onto a thin film covered substrate.

patterning wafers with features smaller than 16 nm is reported to range around \$ 90 million USD [9].

3.4 Piranha Cleaning

Upon receiving a new wafer and before any fabrication steps, a piranha clean is performed to remove contaminants residing on the wafer's surface [19]. A piranha clean is a 3:1 mixture of sulfuric acid (H_2SO_4): hydrogen peroxide (H_2O_2), and is an extremely exothermic, aggressive method to remove organic materials, hence the derivation of its name [19, 45]. The reaction first acts by dehydrating organic residue on the surface by removing its oxygen (O)- and H-containing molecules in the form of water [45, 46]. The second mechanism is oxidation by dissolving any remaining carbon (C) based molecules and producing carbon dioxide (CO_2). After rinsing the wafer with deionized water, the hydroxyl (OH)-terminated surface becomes

hydrophilic. [19]. Piranha cleaning is usually only performed once at the very beginning of the entire process flow, as the volatility of the solution would deteriorate any subsequent materials deposited onto the surface.

3.5 Pattern Development

3.5.1 Bake and Prime

Although piranha cleaning removes most contaminants on the bare wafer, further surface preparation is the first step required for any lithography process [19]. Contaminants contribute to defects in the photoresist pattern, as well as prohibit photoresist adhesion to the substrate. When the hydrophilic surface is exposed to environmental moisture, tough to remove OH- are produced on the surface [5]. A dehydration bake of the substrate at 150 - 200 °C in vacuum removes most of the adsorbed water but leaves behind a monolayer of silanol ($SiOH$) groups on the surface [44, 47]. Photoresist has poor adhesion to the baked dehydrated surface, and it is necessary to subsequently deposit an additional coating to promote photoresist adhesion [47]. Therefore, immediately following the dehydration bake is vapour priming (Fig. 3.3a), where an adhesion promoter such as hexamethyldisilazane (HMDS) vapour is applied. An organic functional group replaces the $OH-$ group on the surface as shown in Fig. 3.4, which then provides adequate surface adhesion to the subsequent application of photoresist [47, 48].

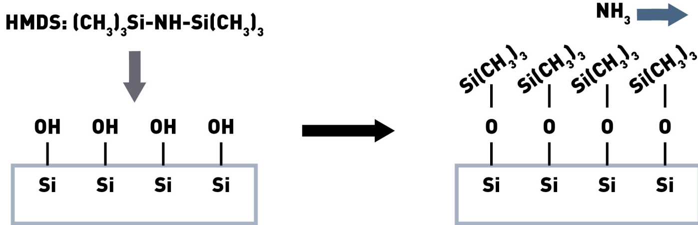


Figure 3.4 – Hexamethyldisilazane (HMDS) process in priming a substrate to promote photoresist adhesion.

3.5.2 Photoresist Chemistry

The photoresist is a solution composed of an organic polymer, solvent, and photoactive compound that is designed to be sensitive to the type of radiation used for exposure [3, 5, 9]. There are two types of resist as shown in Fig. 3.5. Upon utilizing the same photomask, a negative photoresist leaves the inverse of the positive resist pattern [5, 35]. Exposed radiation in positive resist causes polymer chain-scission, such that the cleaved polymer chains result in an increase in the solubility of resist in a developer [5, 35]. While exposed radiation in negative resist causes polymer cross-linking, rendering the photoresist less soluble in a developer. The type of resist used usually depends on the patterns that need resolving [35]. Patterning an isolated line is best suited for negative resists, and additionally, negative resists are less expensive than their counterparts. However, positive resists are usually preferred because they utilize less toxic developers and provide a better overall resolution. Therefore, the project consists of lithographic steps utilizing only positive photoresists.

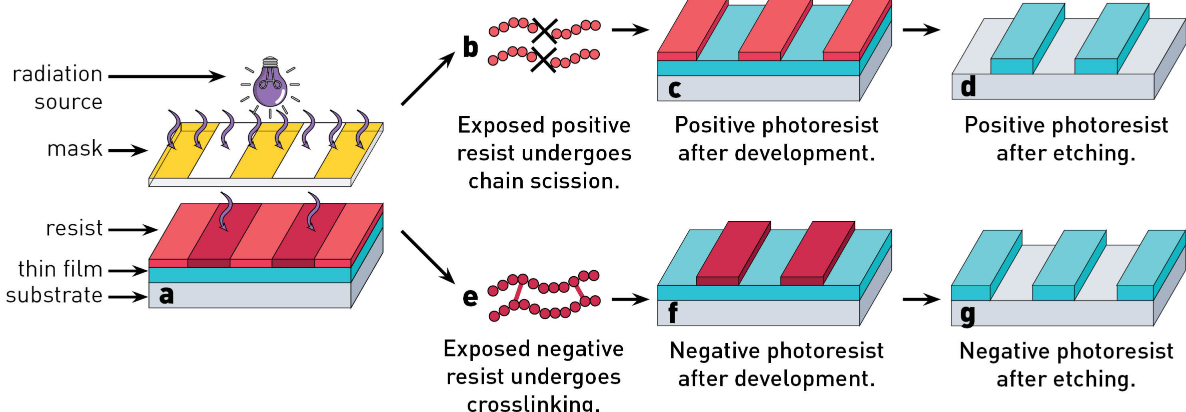


Figure 3.5 – Comparison between utilizing positive and negative photoresists under the same photomask pattern.

DNQ-Novolac positive resists are the most commonly used resist for optical lithography, and is comprised of three main components [3, 35, 49]:

1. **Base Novolac resin:** Establishes the resist's thermal and structural properties.
2. **Diazonaphthoquinone (DNQ) photoactive compound:** A strong inhibitor which is not soluble in a base developer. Upon exposure to UV light between 310 - 450 nm, DNQ reacts and is converted into carboxylic acid, allowing the resist to be soluble in an alkaline developer.
3. **Solvent:** Determines viscosity and allows the resist to be in liquid form for easy application.

EBL resists such as polymethyl methacrylate (PMMA) have similar components to DNQ-Novolac, but are sensitive to wavelengths below 240 nm, and polymer chain-scission reacts significantly slower [3, 35, 50]. Although PMMA can be used in optical lithography utilizing DUV radiation, it is usually used solely for EBL. When PMMA is exposed to an electron-beam, the solubility of the PMMA resist increases, which can be subsequently developed in a solvent.

3.5.3 Spin Coating

Following a bake and prime with HMDS is spin coating of photoresist (Fig. 3.3b) [3, 49, 51]. The photoresist is applied to the center of a slowly rotating substrate held in place by a vacuum chuck, allowing the resist to uniformly dispense across the wafer [3, 49, 51]. The substrate then rapidly accelerates for a given amount of time, which determines the final resist thickness due to its centrifugal force [35]. A faster spin speed provides a thinner resist layer, where the standard thickness varies between 0.1 - 500 µm.

3.5.4 Post Apply Bake

To stabilize and harden the resist layer, the substrate is baked between 100 - 180 °C on a hot plate to drive out any remaining solvent (Fig. 3.3c) [3, 49]. Over baking the resist can break down the photoactive compound, leading to problematic exposure.

3.5.5 Optical Lithography

Although other radiation sources such as electron or ion beam lithography have superior feature resolution, they are severely handicapped by low throughput [2, 43, 47]. Therefore, the majority of patterning in the semiconductor industry is still done with optical lithography (Fig. 3.3d). As the entire pattern for a wafer is exposed in one step, patterning is produced with very high throughput. However, the resolution of feature sizes in optical lithography is diffraction limited [2, 47]. For contact optical lithography aligners used in most university fabs, this is in the sub-micron regime. State of the art optical lithography aligners circumvent the diffraction limit by employing complex and expensive lithographic systems, and clever tricks utilizing elaborate mask designs [2, 47].

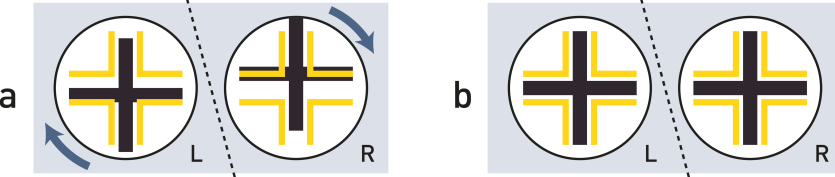


Figure 3.6 – Alignment between a photomask (yellow alignment marks) and substrate (black alignment marks). **(a)** The substrate is first translated such that its alignment marks are within spatial proximity of the photomask's alignment marks. **(b)** The substrate is then rotated such that alignments marks on both substrate and photomask are superimposed.

Most devices consist of multiple lithographic layers that must be precisely aligned to ensure proper functionality [3]. Previously lithographed alignment marks are superimposed with alignment marks of the new mask to ensure proper positioning and angle within the mask aligner as shown in Fig. 3.6. Photomasks are composed of a UV transparent material such as soda-lime glass, with a computer-aided design (CAD) pattern drawn out with an opaque 100 nm thick chromium (Cr) layer [3, 47]. As the resist is sensitive to wavelengths below 450 nm, patterns are exposed for several seconds to a Hg-vapour lamp, providing distinct peaks

at wavelengths of 365, 405, and 436 nm [3, 47]. There are three main techniques for pattern exposure as presented in Fig. 3.7:

1. **Contact lithography (Fig. 3.7a):** The simplest of three techniques; a 1:1 scale of the mask is placed in direct contact with the coated substrate [5, 47]. This technique is not as popular in the industry, as defects can be caused by mask contamination. Additionally, the intimate contact of the mask and substrate can cause photoresist to tear off onto the mask. However, as it is the most economical method, it is widely used in academic research [2].

2. **Proximity lithography (Fig. 3.7b):** Very similar to contact lithography, but a small gap of several microns is left between the mask and substrate, avoiding the issues of defects that were present with contact lithography [5, 47].

3. **Projection lithography (Fig. 3.7c):** A complex and expensive lens system projects the mask pattern onto the substrate [5, 47]. Although rare in academic research, it is the most widely used technique in the industry as it avoids mask contamination issues and most importantly, can reduce the scale of the mask pattern [2, 5, 47].

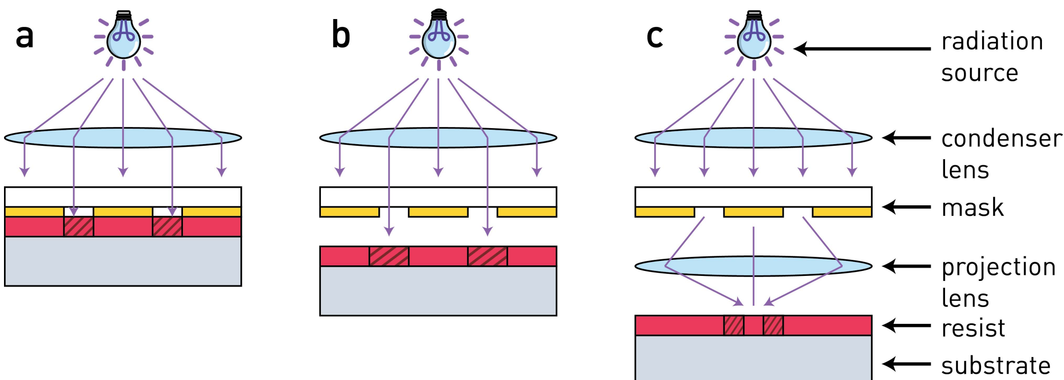


Figure 3.7 – The three main types of optical lithography aligners. **(a)** Contact lithography projects a 1:1 ratio of the pattern onto the resist. **(b)** Proximity lithography projects a slightly larger pattern onto the resist. **(c)** Projection lithography projects a reduced pattern onto the resist.

3.5.6 Electron-Beam Lithography

Evolving from SEM technology; maskless, direct-write lithography options such as EBL (Fig. 3.3e) can be used as an alternative [2]. As its resolution is mainly limited by optical aberrations and electron scattering in the resist, which is on the order of tens of nanometers, its resolution is a dramatic improvement over basic optical techniques as are available at a university fab [47]. However, the low throughput of EBL has kept its use outside larger-scale manufacturing, limiting its use in mainly research and development [2, 47].

To perform EBL, a PMMA resist coated substrate is fixed onto a sample holder and loaded into the EBL's vacuum chamber [40, 50]. To obtain the correct exposure parameters, meticulous calibrations such as alignment of the gun and column, correction of beam astigmatism, focus and current, and write-field alignment are performed. Alignment marks similar to those utilized in optical lithography are used for positioning and angle alignment. The tool is then automated to expose the sample to a preloaded pattern, where exposure of the electron-beam increases the solubility of the PMMA resist, which is subsequently developed in a solvent.

Optical lithography is analogous to a printing press; although it has a high starting cost, it is the most economical and efficient option for large-scale production [3]. While EBL and other maskless lithographic methods are like writing with a pen; smaller-scale patterning can be produced and altered very quickly but is not efficient at producing multiple copies, restricting it to mostly academic research.

3.5.7 Proximity Effects

Proximity effects are the deviation of pattern features due to other nearby features and are the primary hindrances in resolution limits for both optical and electron-beam lithography [35, 47]. These can include variations in line width, rounding of corners, and most evidently in the deviation in the appearance of an isolated line as opposed to an array of lines. Proximity effects

can even cause neighboring features in close packing densities to merge or vanish altogether as was previously shown with the EBL patterned stripes in Fig. 3.1 [42].

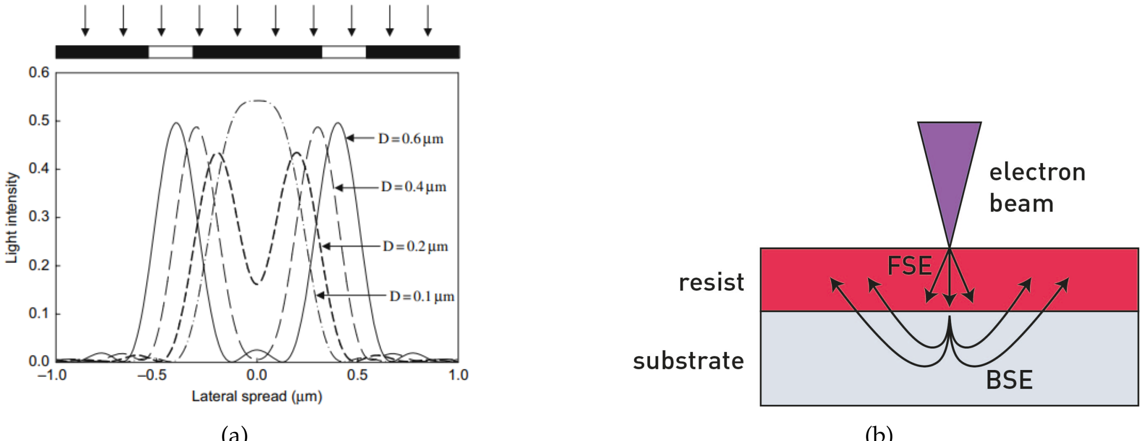


Figure 3.8 – Lithographic proximity effects: **a)** Optical proximity effect: Resulting light intensities of illumination through a photomask with two 0.2 μm wide line features separated by a gap of distance ’D’. Given a half-pitch of 0.2 μm, when the gap is half this distance (D = 0.1 μm), the two features merge into one, and the original pattern can not be resolved. Reproduced from "Nanofabrication: Principles, Capabilities and Limits" by Cui, Z., 2008. Copyright 2008, by permission of Springer Nature [2]. **b)** Electron proximity effect: Forward scattered electrons and backscattered electrons leads to a loss in pattern fidelity; backscattered electrons are far more detrimental, as electrons scatter with wider angles and larger deviations from their original position.

Optical proximity effects are caused by optical diffraction as shown in Fig. 3.8a, where decaying evanescent waves expose undesired areas of photoresist [52]. A common method to circumvent optical proximity effects and maintain pattern fidelity is to modify the dimensions and design of patterns to compensate for nonuniform areas of exposures on the resist as shown in Fig. 3.9 [35, 47, 52].

Electron-beam proximity effects are the main culprit in limiting EBL resolution and are caused by electron scattering in the photoresist and the substrate [41, 42]. Forward scattered electrons are deflected with small angles, while backscattered electrons deflect back into the

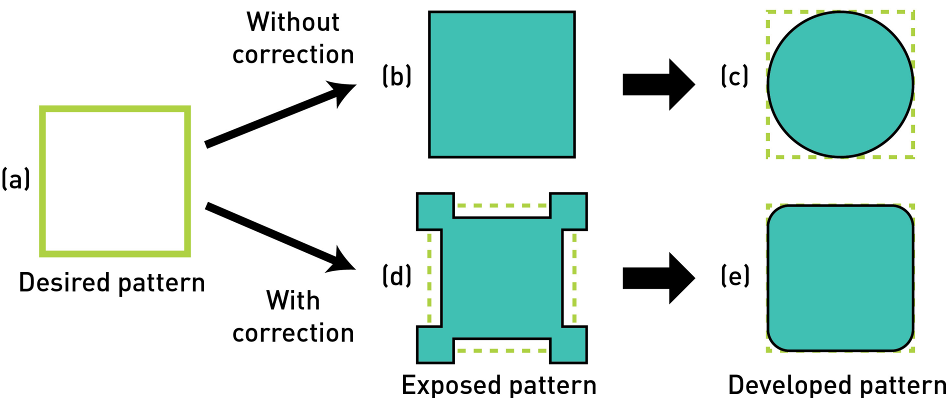


Figure 3.9 – A square feature on a photomask produces a rounded feature due to optical proximity effects. Optical proximity corrected patterns maintain pattern fidelity by accounting for neighboring features and developer behavior.

resist with broader angles, and travel quite far from the electron's point of entry as shown in Fig. 3.8b, making backscattered electrons much more detrimental than forward scattered electrons [41, 42]. Electron-beam proximity effects can be minimized by optimizing EBL processing parameters and adjusting pattern designs.

3.5.8 Development

After pattern exposure alters the resist chemistry, a developer bath removes the soluble resist areas away (Fig. 3.3f) [3, 47, 49]. Following the development of the patterned photoresist, the pattern is then transferred to the substrate through a variety of fabrication methods, such as etching (Fig. 3.3g), doping (Fig. 3.3h), or liftoff (Fig. 3.3i).

3.6 Etching

The most common process following lithography is etching the underlying material from exposed and unprotected regions of the pattern [3, 44]. Etching is categorized as either chemical

(wet), physical (dry) or plasma etching, with their differences in the phase of etchants used and by-products of the reaction [3, 44].

Chemical (wet) etching consists of the substrate submerged in a liquid chemical bath, where the exposed areas chemically react to produce soluble by-products [3, 44]. Physical (dry) etching is analogous to nanoscale sandblasting, and no chemical processes are involved [3, 44]. Plasma etching utilizes a vacuum chamber with reactive gases to perform a combination of both physical and chemical processes to produce volatile products, that are then dissociated and pumped away [3]. Parameters used in determining the performance of an etching process include the selectivity between the etching mask and underlying material, the etch rate, and anisotropy [44].

3.6.1 Chemical Etching

Chemical etching is typically isotropic, even undercutting underneath the protective photoresist mask as shown in Fig. 3.10 [44]. Although its high etch rate typically makes it difficult to control and reproduce, it is highly desirable for large-scale manufacturing where processes can be highly automated.

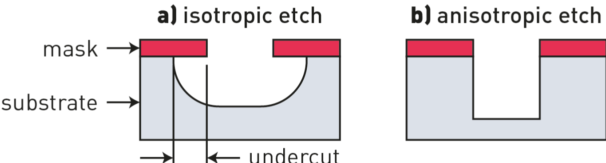


Figure 3.10 – Substrate profiles following etching. **(a)** Chemical etching generally isotropically etches the substrate, undercutting the photomask. **(b)** Physical and plasma etching generally anisotropically etches the substrate.

One of the most commonly used thin film materials in nanofabrication is silicon dioxide

(SiO_2) [3, 9]. Hydrofluoric acid (HF) is a common chemical etchant for SiO_2, as it has an exceedingly high selectivity for SiO_2 to Si [19]. The etching reaction is [44]

$$SiO_2 + 6HF \rightarrow H_2 + SiF_6 + 2H_2O \tag{3.1}$$

HF is commonly buffered with its conjugate base, ammonium fluoride (NH_4F), to form a buffered oxide etchant (BOE) [44, 53]. As HF is consumed with the reaction, NH_4F aids in maintaining a constant supply of fluorine ions described by [44]

$$NH_4F \rightleftharpoons NH_3 + HF \tag{3.2}$$

This ensures the pH of the solution is maintained, and a constant supply of HF is present for a consistent etch rate [44]. The characteristic indicator that all oxide is removed is when the surface changes from hydrophilic to hydrophobic.

3.6.2 Physical Etching

Ion milling is a purely physical process that uses inert gases, such that no chemical reactions are involved [44]. Ion milling achieves high anisotropy by employing a strong electric field to accelerate ions in a low pressure chamber. This allows ion-ion collisions to rarely occur, such that ion impact on the substrate's surface remains vertical for a high degree of anisotropic etching. The benefit of being independent of any chemical reaction is that anisotropic etching can be performed on any material. However, this also poses as an obstacle, as the selectivity to any masking layer will also be roughly 1:1.

3.6.3 Plasma Etching

Reactive ion etching (RIE) is the general plasma etching process [44, 54]. The process utilizes an RF field to produce a plasma that ionizes reactive gases into neutrals and ions within a low pressure vacuum chamber, incorporating a combination of both physical (ion bombardment) and chemical (reactive) etching processes. Reactants diffuse and adsorb onto the substrate's surface where they chemically react, and the by-products are desorbed and diffused out of the chamber [44]. While ions physically bombard the surface to provide energy for etching mechanisms such as adsorption, desorption, and surface reactions as shown in Fig. 3.11.

RIE allows for more control and provides less sensitivity to environmental temperature and humidity changes, thus allowing it to be significantly more repeatable than a wet etch bath [3]. However, the most attractive capability of RIE comes from its capability in vertical ion bombardment, allowing anisotropic etching of small features with aspect ratios of 100:1.

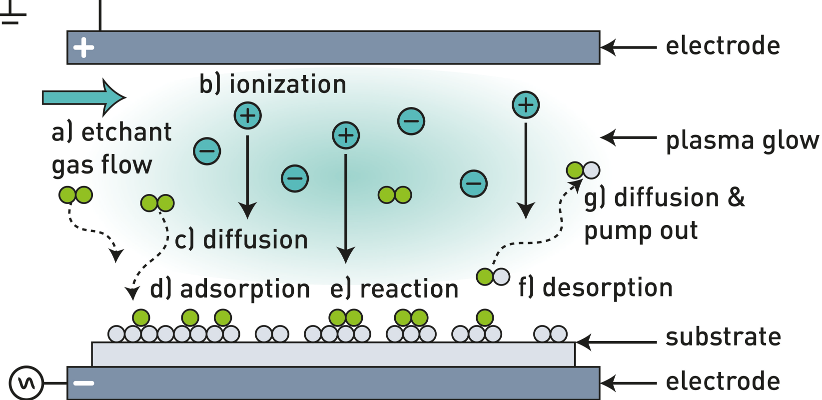


Figure 3.11 – Reactive ion etching (RIE) process showing a combination of the physical and chemical processes involved.

Deep Reactive Ion Etching

Deep reactive ion etching (DRIE) is an enhanced variation of RIE, allowing for features of even larger aspect ratio [3, 55]. The Bosch process is a variant of DRIE and is illustrated in Fig. 3.12. Alternating pulses of sulfur hexafluoride (SF_6) and octafluorocyclobutane (C_4F_8) are applied; a pulse of SF_6 isotropically etches Si (Fig. 3.12a) but is followed by a pulse of C_4F_8 to deposit a thin protective film (Fig. 3.12b). The next pulse of SF_6 uses ion bombardment to etch the protective film, but only at the bottom of the trench, while the sidewalls remain passivated (Fig. 3.12c). With the protective film removed, SF_6 continues etching the substrate and parts of the passivated walls (Fig. 3.12d), continuing the cycle.

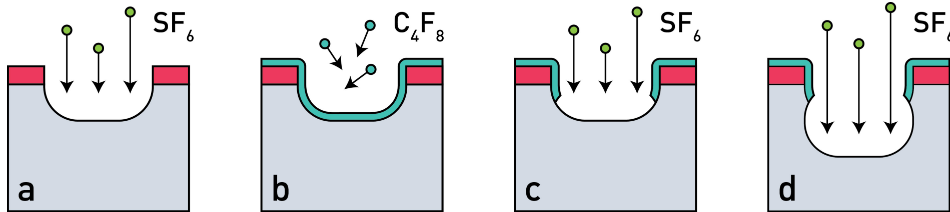


Figure 3.12 – Bosch etching process: **(a)** Sulfur hexafluoride (SF_6) isotropically etches the substrate. **(b)** Deposition of octafluorocyclobutane (C_4F_8) passivates the surfaces with a protective layer. **(c)** Directionality of SF_6 bombardent etches the bottom protective layer. **(d)** SF_6 continues to isotropically etch the substrate. Thus the process repeats until the desired etch depth is reached.

3.6.4 Summary

Table 3.1 – Advantages and disadvantages of various etching methods.

	Wet	Dry	Plasma
Selectivity	Good	Poor	Moderate
Etch Rate	Good	Poor	Good
Anisotropy	Poor (Isotropic)	Good	Good
Costs	Low	High	High

The advantages and disadvantages of each etching method is compared and highlighted in Tab. 3.1 [3, 19, 44].

3.7 Ion Implantation

The capability to dope Si and precisely alter its electronic properties has lead to the advancements made in semiconductor technology [33]. Dopants can be introduced to the substrate through thermal diffusion, however, since the '80s, doping has almost been exclusively done through ion implantation due to the isotropic profile of thermal diffusion [34]. Another shortcoming of thermal diffusion is the peak dopant concentration resides on the surface, while ion implantation can implant the peak concentration deep within the substrate by increasing implantation energy [19].

To perform ion implantation, dopants are first ionized in a vacuum. Then using an electric field, ions are accelerated towards a Si substrate with typical energies between 10 - 200keV [3, 44, 56]. The ions penetrate the bulk with doses between 10^{11} - 10^{16} $ions \cdot cm^{-2}$, which are decelerated through stochastic collisions as shown in Fig. 3.13a. Higher implantation energies provide a deeper projected range (R_P), and the deviation in range of ion distribution under the surface is referred to as straggle (ΔR) [3, 56]. The dopant profile is approximated with a Gaussian distribution, where 10% of the dopant profile peak lies at a distance of $R_P \pm 2\Delta R$, while 1% of the dopant profile peak lies at a distance of $R_P \pm 3\Delta R$. As shown in Fig. 3.13b, lighter elements travel through the substrate with a larger R_P, as well as a larger ΔR. Additionally, heavier elements have lower diffusion during annealing, making As and Sb preferable over conventionally used P for n-type ion implantation [4].

There are several drawbacks of ion implantation; the high energies required during processing, eject atoms within the lattice, which subsequently undergo further collisions, displacing more atoms as shown in Fig. 3.13a, and damaging the substrate's crystal lattice [3, 44].

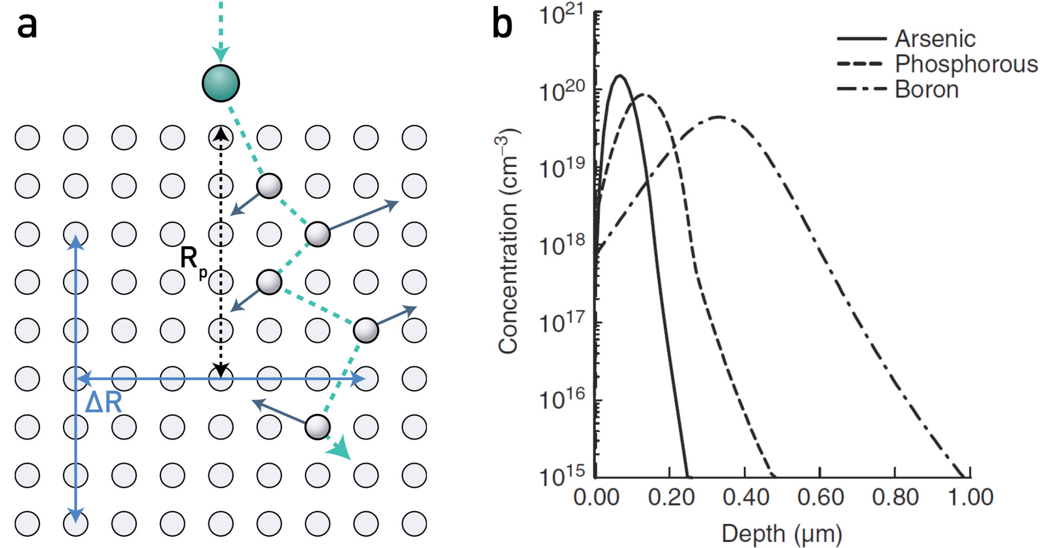


Figure 3.13 – **(a)** Ions implanted into a substrate are decelerated through colliding and displacing other atoms in the lattice. On average, the ion stops at a projected range (R_P), which deviates by the straggle (ΔR). **(b)** Dopant distribution of various elements implanted with 50 keV. Heavier ions implanted with the same energies have a smaller R_P and ΔR. Reproduced from "Introduction to Microfabrication" by Franssila, S., 2010. Copyright 1969, by permission of John Wiley and Sons [3].

The extent of damage depends on implant energy, dose, and dopant species, as heavier ions are more damaging. The resist used to pattern implanted regions also forms a very difficult to remove carbonized layer following ion implantation.

3.7.1 Annealing

As mentioned, the high energies of ion implantation can damage the Si crystalline structure [3, 44]. A Si atom can be displaced from the lattice with only 20 eV, so when barraging the surface with ions of 100 keV during implantation, one ion could potentially displace around 5000 Si atoms [19]. The dopants are also implanted at interstitial lattice sites and need to be positioned in substitutional lattice sites to perform intended electrical operations. To repair the crystalline

damage and to reposition the implanted dopants, diffusion through high-temperature annealing at temperatures greater than 800 °C is required [3].

Annealing can be done through rapid thermal annealing (RTA), which rapidly heats a wafer enclosed in a highly reflective chamber through high-intensity infrared (IR) lamps at high temperatures for tens of seconds [57]. In an industrial setting, furnace annealing (FA) is performed for batch processing [57]. Hundreds of wafers are loaded into a hot furnace to anneal for around an hour. Although RTA systems can only process a single wafer at a time, it can be advantageous over FA for small batches of several wafers due to the significant decrease in processing time. RTA is also attractive in addressing the substrate's thermal budget and minimizing diffusion, especially critical in shallow junctions [3].

3.8 Deposition

Thin film deposition is widely used to modify surfaces to tailor mechanical, electrical, optical, or chemical properties [19, 58]. The emergence of deposition techniques can be credited to its wide use in consumer products, from food insulation and packaging, to decorative coatings in automobiles and jewelry [58]. In nanofabrication, deposition techniques use either physical (PVD) or chemical vapour deposition (CVD), with a focus on depositing dielectric or metal thin films [19]. The two techniques are differentiated by the phase of starting materials and deposition pressure. PVD liberates atoms from a solid target to deposit its material onto the substrate, while CVD utilizes the chemical reaction of gaseous precursors to form a thin film [44]. PVD deposition pressure is also no more than a few mTorr, while CVD operates at pressures as high as several Torrs [19].

3.8.1 Physical Vapour Deposition

PVD vapourizes the solid target material to be deposited, to liberate target atoms to be ejected towards a substrate [19]. Different methods of PVD are determined by the target vapourization method, which is usually done by heating or ion bombardment of the target material. The different methods of PVD also provide different thin film qualities. PVD is performed in vacuum at pressures of no more than a few mTorr, such that ejected atoms do not undergo collision, providing a direct line of sight towards the substrate [3].

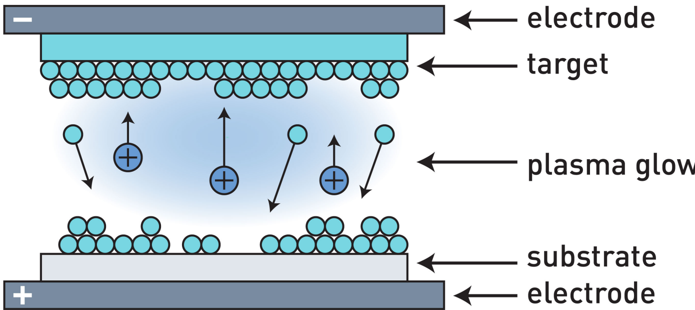


Figure 3.14 – The process of sputtering: a plasma creates argon (Ar) ions to bombard the biased target material, ejecting target atoms that are deposited on a substrate.

Sputtering

In the semiconductor industry, PVD was initially done solely through thermal evaporation, which is done by heating the target material until it evaporates [44]. However, thermal evaporation has now been mostly replaced with sputtering due to sputtering's improved step coverage and ability to deposit a vast array of materials [44]. The sputtering system is almost identical to the RIE system, utilizing parallel plates to produce a plasma within a vacuum chamber [3]. However, in the case of sputtering, argon ions (Ar+) from the plasma strike the negatively biased target material, ejecting its atoms towards the substrate to be deposited on the surface as shown in Fig. 3.14. Although DC sputtering has a better sputtering rate, in using an RF plasma, even insulating materials can be deposited.

Liftoff

Deposited metal films can be hard to etch, therefore to overcome these difficulties, 'liftoff' can be performed instead [44]. To perform liftoff, metal is first deposited overtop patterned photoresist using PVD [44]. When the resist is dissolved, the metal overtop of the sacrificial resist also simultaneously lifts off, leaving behind metal in the exposed regions as illustrated in Fig. 3.15. Bi-layer lithography is performed to ensure an angled resist profile, which includes an additional lift-off resist (LOR) to be spin-coated before the traditional positive resist (Fig. 3.15a) [59, 60]. The top layer of positive resist is exposed to a mask pattern (Fig. 3.15b), which then acts as an etching mask for the LOR layer underneath. The LOR is subsequently isotropically developed to form an undercut profile (Fig. 3.15c). When metal is sputtered overtop, the undercut profile allows for discontinuity within the film (Fig. 3.15d), such that the sacrificial resist lifts off without intruding the desired pattern (Fig. 3.15e).

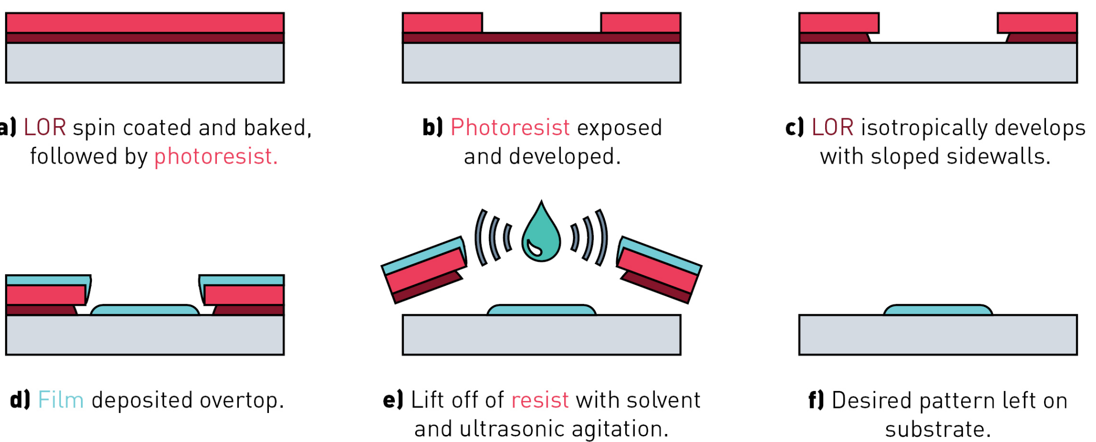


Figure 3.15 – Substrate profile during liftoff when using an additional liftoff resist (LOR).

3.8.2 Chemical Vapour Deposition

In CVD, volatile gases chemically react with the substrate's surface to produce a solid thin film [44]. For electronic nanofabrication, CVD is usually utilized for dielectric materials such as nitrides and oxides. The process for producing an oxide layer (SiO_2) on top of a Si substrate is [44].

$$SiH_4(g) + O_2(g) \rightarrow SiO_2(s) + 2H_2(g) \tag{3.3}$$

Although it is possible to use sputtering for some non-conductive materials, CVD remains the ideal process for insulating materials. Due to the isotropy of precursor gases, CVD offers conformal step coverage, opposite that of PVD, where target deposition generally follows a straight path.

Plasma Enhanced Physical Vapour Deposition

CVD systems typically utilize high temperatures, but in CMOS electronics where layers of metal contacts are woven between insulating dielectric material, most CVD systems are not suitable as this could be detrimental to lower melting point metals and cause dopant diffusion [19, 44]. To circumvent this, plasma-enhanced CVD (PECVD) utilizes an RF plasma so that free radicals from the plasma bombard the surface, providing the needed energy for adspecies diffusion, and increasing reaction rate, without the use of high temperatures.

3.9 Photoresist Removal

The last step involved in the lithography sequence is removing the resist without damaging any underlying material [3]. Solvent strippers are much easier and quicker to utilize, but are less controllable and involve more toxic chemicals in comparison to an oxygen plasma [35].

3.9.1 Solvent Stripper

Piranha solution as mentioned previously, is very efficient in removing organic material such as photoresist from a substrate [35]. However, due to their volatility in the presence of a substantial amount of organic material, they are commonly prohibited from laboratories outside of use in initial surface preparation [19, 45]. Additionally, H_2SO_4 from the piranha solution will also etch metals, prohibiting its use if the substrate has been previously metallized [3].

A chemical bath of a mild alkaline solvent stripper or acetone alongside ultrasonic agitation is more commonly used in removing the photoresist, but is incapable of removing resist if the resist has been altered by ion bombardment [3].

3.9.2 Oxygen Plasma Clean

A gas plasma is frequently used for etching, but can also be used to clean surface contamination [19]. Molecular oxygen (O_2) is commonly used to clean organic contamination such as photoresist, without disturbing any inorganic material on the substrate. Within the plasma, O_2 is broken into neutral radicals and ions which then react with organic surfaces, producing organic species such as H_2O and CO_2 to be pumped out. UV light emissions can also be incorporated to further dissociate organic material, allowing for more efficient cleaning [19, 35].

04

Nanofabrication of the Macro-to-Atom Device

4.1 Device Overview

All device fabrication except ion implantation was performed using available tools from the nanofabs located in the National Research Council of Canada Nanotechnology Research Centre and the Electrical and Computer Engineering Research Facility at the University of Alberta. Ion implantation was done externally at CuttingEdge Ions, a specialized semiconductor ion implantation company based in California. The basic fabrication process is described in Fig. 4.3 - 4.9, while the mask patterns and parameters for the nanofabrication processes in detail is described in Appx. A. Although the process flow for fabricating the device has been designed and planned out, fabrication of the device has been divided into three components which are separated at the three different implantation steps required as shown in Fig. 4.1. Each of the three components of the device is fabricated and experimented upon independently of each other for the time being. This aids in simplifying individual concerns and circumvents time limitations of outsourcing ion implantation.

The bulk of the macro-to-atom device (Fig. 4.1a) is fabricated following the processes described in Fig. 4.3, 4.4, 4.7, 4.8 and 4.9 (lithography steps # 1, 2, 5, 6, 7). The device has Pt

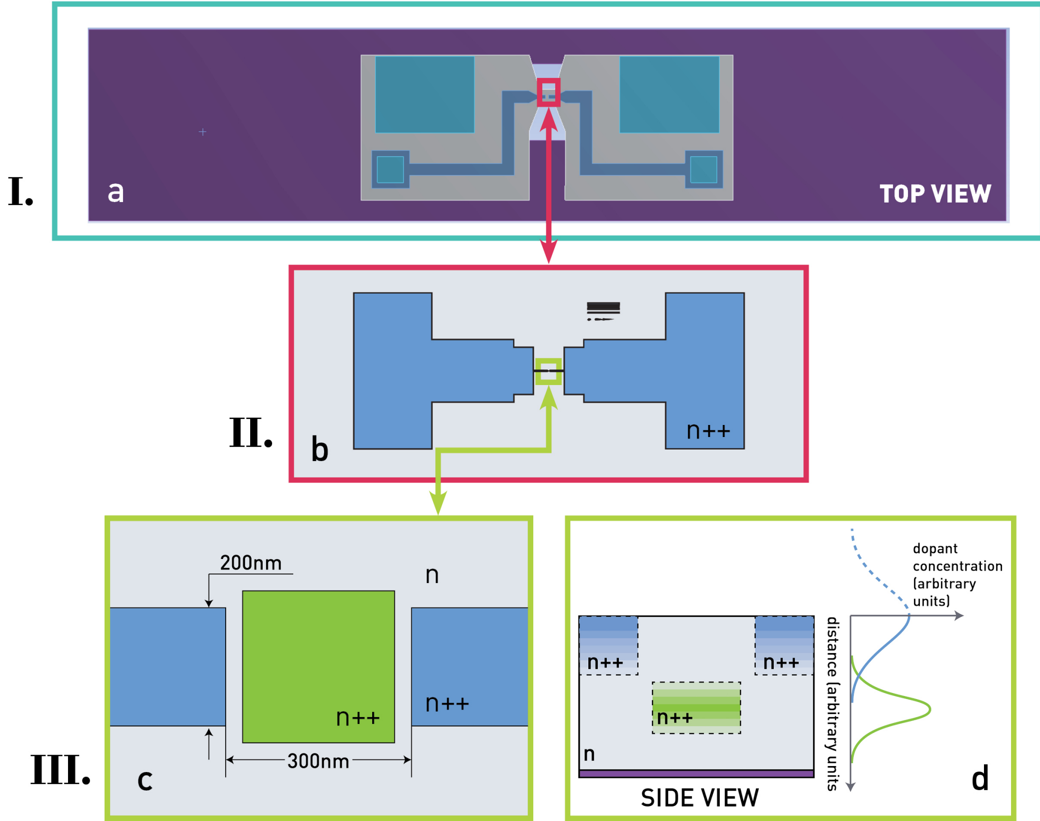


Figure 4.1 – The three main components of the macro-to-atom device: **(a)** Project I focuses on the nanofabrication of the bulk of the macro-to-atom device, including the ion implanted arsenic (As) conduction lines. **(b)** Project II focuses on the electron-beam lithography (EBL) patterned contacts, where narrower electrodes interface with the atomic circuitry patterned in between the gap. **(c)** Project III focuses further center where atomic-scale lithographic patterning occurs. A heavily-doped antimony (Sb) region is embedded under the surface, to provide carriers for low-temperature scanning tunneling microscope (LT-STM) operation and for the surface dangling bonds (DBs) to be negatively charged. **(d)** Side view of (c): heavily-doped areas are implanted with a Gaussian distribution. The embedded Sb reservoir (green) utilizes a heavier dopant than the As contacts (blue), thus it has a narrower and sharper dopant profile.

power pads required for STM surface preparation, Pt signal pads for wire bonding to external CMOS circuitry, and heavily implanted As conduction lines connecting the Pt signal contacts to the center of the device. Between two such As conduction lines is a 2 - 4 μm gap, which is the resolution limit of optical lithography. To narrow down the width of the contacts and size of the gap, EBL is utilized to pattern smaller contacts (Fig. 4.1b). Fabrication for the EBL contacts are described in Fig. 4.5 (lithography step # 3). Narrowing the contacts and gap is required to help accommodate the STM patterning window, as well as being able to scale between the larger conduction lines and atomic circuitry.

The cryogenic temperatures used for atomic-scale lithographic patterning causes a carrier freeze-out of the lightly-doped bulk. Therefore, a heavily-doped Sb embedded reservoir (Fig. 4.1c,d) is required to provide a sufficient amount of free carriers for STM imaging to be possible [10]. The heavily-doped Sb reservoir could also provide the surface DBs with the required charge state for use in computing [61]. Fabrication for the doped reservoir is described in Fig. 4.6 (lithography step # 4).

4.2 Substrate

Unless otherwise specified, a default Si wafer has a <100> orientation. The <100> orientation offers higher electron mobility compared to <110> wafers and has less trapped charges produced during oxidation compared to <111> wafers, allowing for a better interface quality [35]. Another benefit is that the lower activation energy of a <100> surface allows it to etch significantly faster than the <111> surface. This anisotropic etch is commonly taken advantage of in etching large V-grooves and membrane structures, a signature character in micro-electromechanical systems (MEMS) [3].

SOI wafers offer better performance over traditional Si wafers and are widely adopted in current semiconductor technologies [22]. An SOI wafer is comprised of a thin insulating BOX

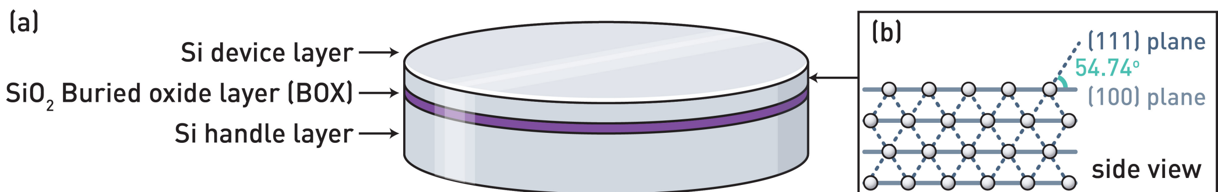


Figure 4.2 – (100) silicon-on-insulator (SOI) wafer. **(a)** Layer schematic. **(b)** Side view of the silicon (Si) crystal planes.

layer bonded between two Si layers as shown in Fig. 4.2. Device circuitry is mostly fabricated on the top Si device layer, and the bottom supporting Si substrate is the handle layer. The biggest advantages of using SOI wafers is in reducing parasitic capacitance, and the junction area being magnitudes smaller decreases leakage currents.

For the macro-to-atom device, an SOI wafer is required because the BOX layer is used as an etching mask for the thermally isolated Si bridge. The macro-to-atom device is fabricated on an SOI substrate with a lightly-doped n-type Si (100) device and handle layer with the substrate parameters listed in Tab. 4.1. The discrepancy in wafer thickness between the two prototypes was not intentional and was simply due to available wafers in stock.

Table 4.1 – Properties of the silicon-on-insulator (SOI) wafers used in the ion implanted macro-to-atom device prototypes.

	Layer	**Thickness (μm)**	**ρ ($\Omega \cdot cm$)**
Prototype #1	Device	20 ± 1	1-10
	BOX	2	
	Handle	400 ± 25	1-10
Prototype #2	Device	25 ± 1	1-10
	BOX	2	
	Handle	600 ± 15	1-10

* **Discrepancy between thickness in the two wafers was not intentional; the wafer for prototype #2 was the only available wafer most similar to prototype #1.**

4.3 Nanofabrication Process

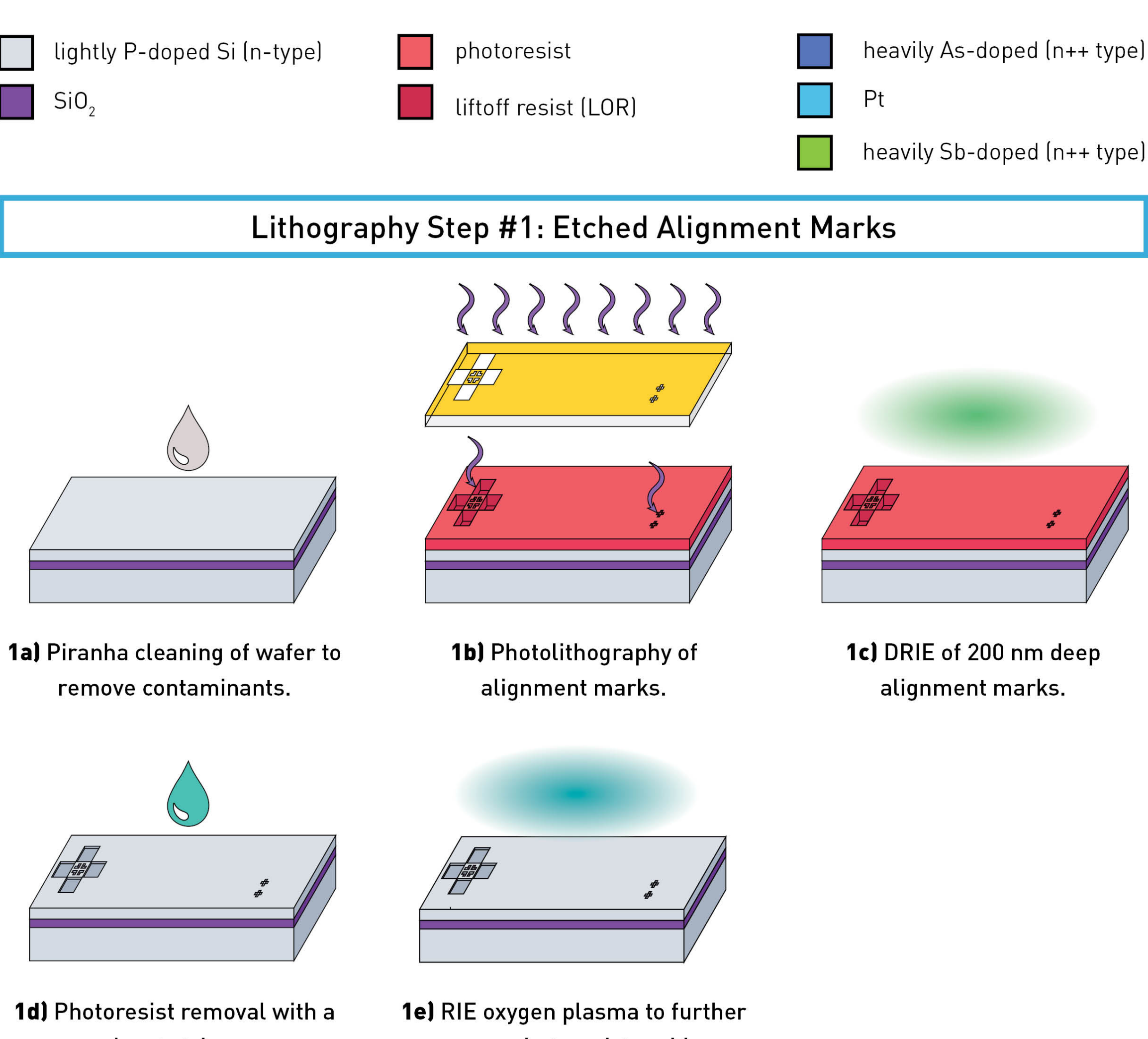
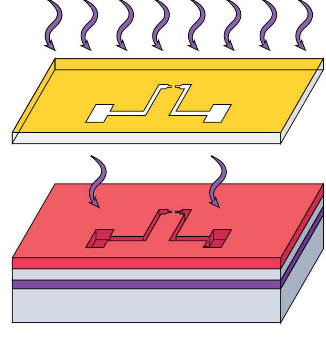
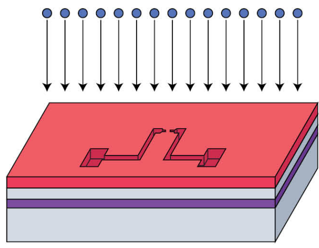


Figure 4.3 – Lithography step # 1: Schematic illustration of the nanofabrication processes for etching alignment marks.

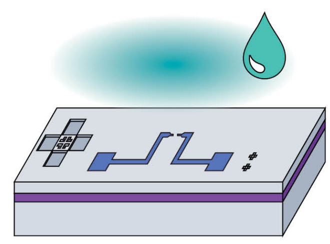
Lithography Step #2: Arsenic Conduction Lines



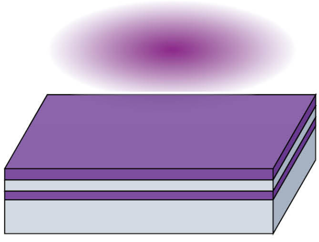
2a) Photolithography of conduction lines.



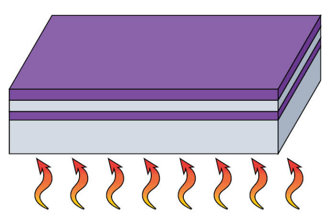
2b) Ion implantation of 100 keV 75As+ ions with a dose of $3.00{\cdot}10^{14}$ ions · cm^{-2}.



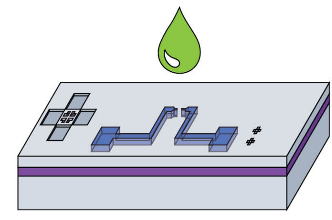
2c) Removal of the carbonized photoresist using a RIE ozone cleaning and a solvent stripper.



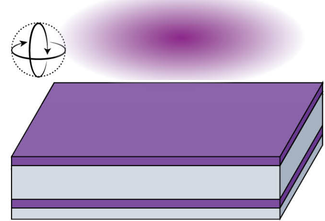
2d) PECVD deposition of a 500 nm thick layer of oxide to be used as a diffusion barrier for the subsequent annealing.



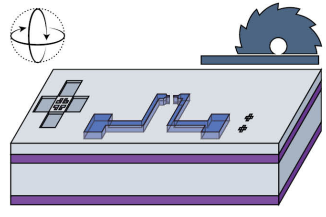
2e) Furnace annealing at 1050 °C for 60 min, dopants are driven down 650 nm into the substrate with a dopant density of $4.2{\cdot}10^{19}$ ions · cm^{-3}.



2f) BOE to remove the 500 nm oxide diffusion barrier.



2g) PECVD deposition of a 500 nm layer of oxide on the handle (back) side to be used as an etching mask for the thermally isolated Si bridge later.



2h) Dicing of the wafer into thirty 12.05mm x 12.55mm blocks (5 devices per block).

Figure 4.4 – Lithography step # 2: Schematic illustration of the nanofabrication processes for implanting heavily-doped arsenic (As) conduction lines.

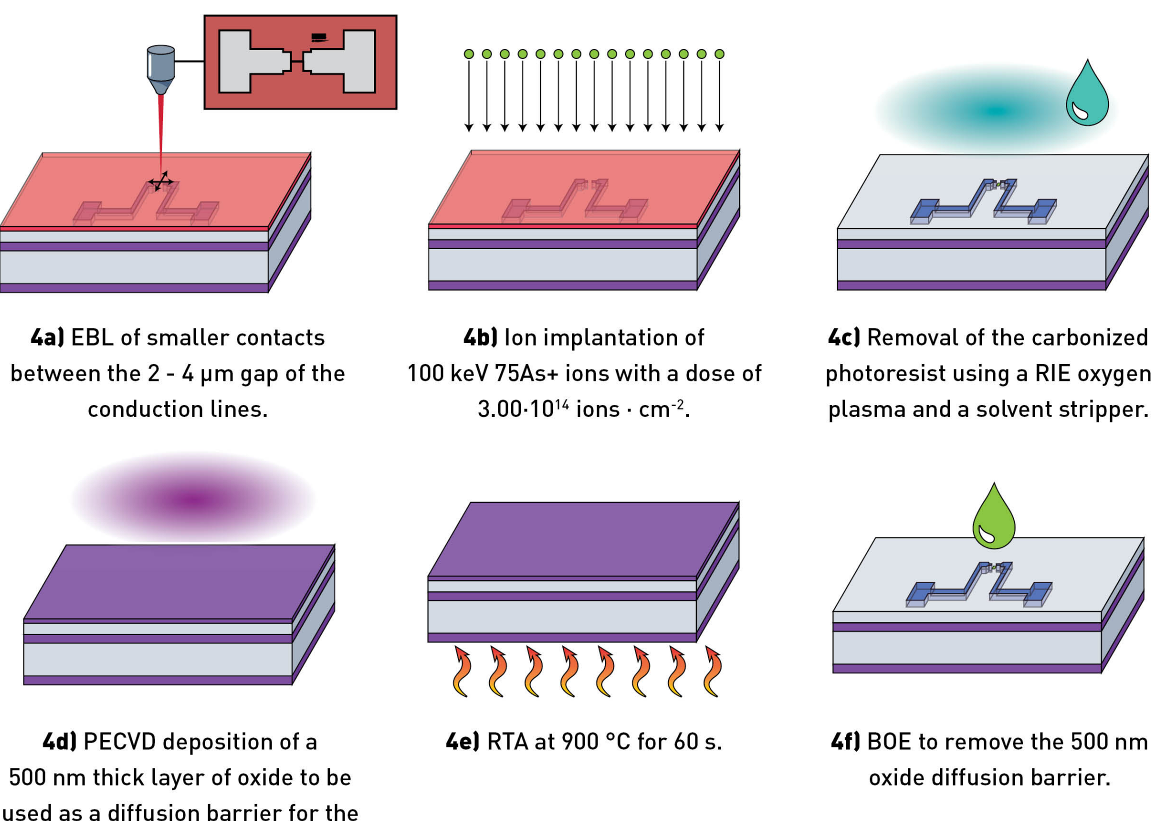


Figure 4.5 – Lithography step # 3: Schematic illustration of the nanofabrication processes for implanting smaller electron-beam lithography (EBL) patterned heavily doped arsenic (As) contacts between the 2 - 4 µm gap in the center of the previously implanted As conduction lines. Although this is where implantation of the As contacts would occur within the process flow of the final macro-to-atom device, it is omitted in fabrication of prototype # 1 and # 2 of the main device, and fabricated and tested on individually.

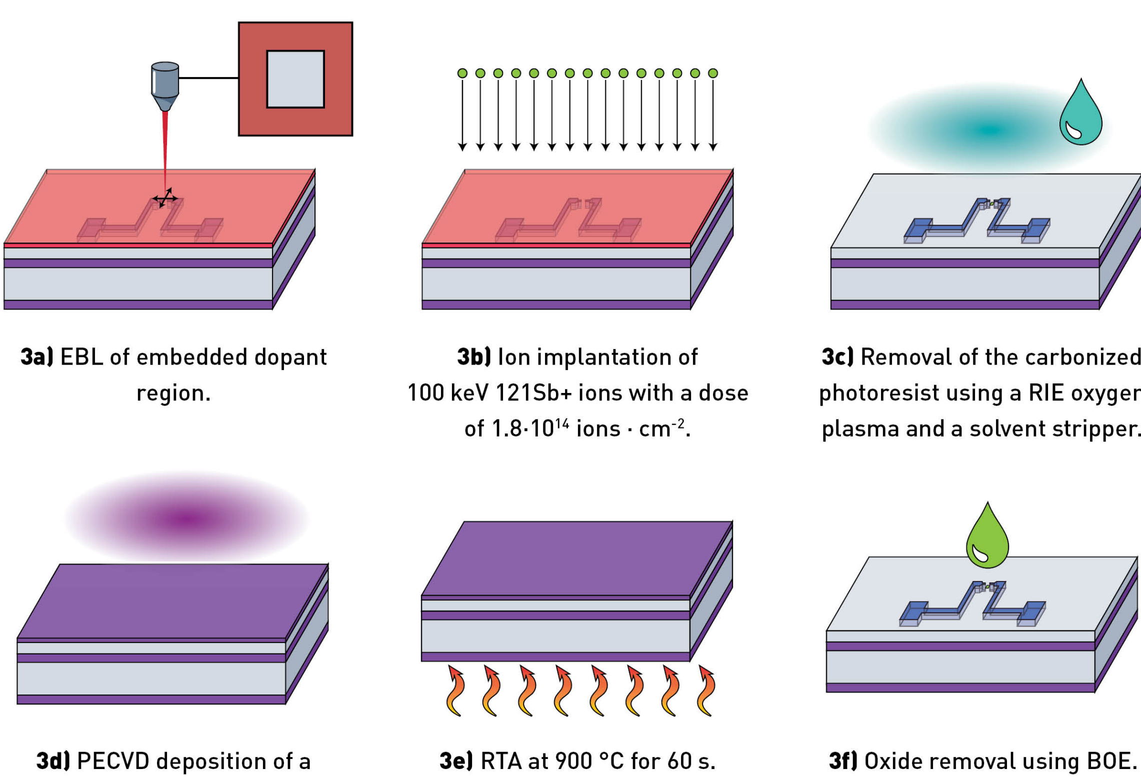
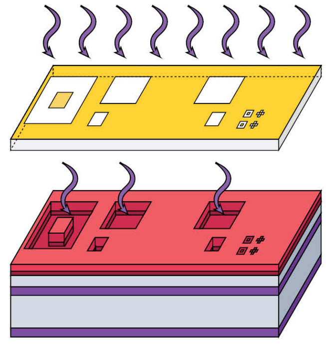
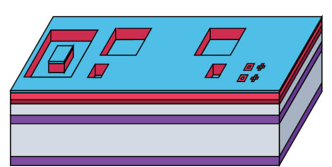


Figure 4.6 – Lithography step # 4: Schematic illustration of the nanofabrication processes for implanting a heavily-doped embedded antimony (Sb) reservoir between the 300 nm gap in the center of the previously implanted arsenic (As) contacts. The Sb reservoir is implanted with the dopant profile peak ~45 nm under the surface. Although this is where implantation of the embedded Sb reservoir would occur within the process flow of the final macro-to-atom device, it is omitted in fabrication of prototype # 1 and # 2 of the main device, and fabricated and tested on individually.

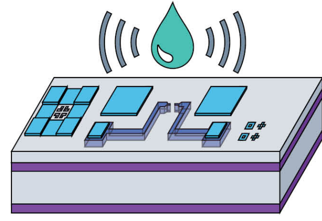
Lithography Step #5: Platinum Contact and Signal Contacts



5a) Bilayer photolithography of Pt power and signal contact pads.



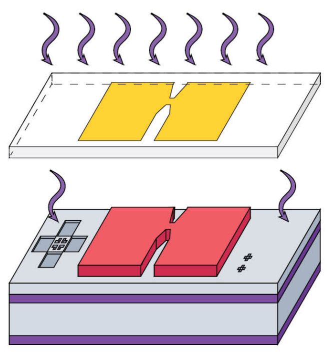
5b) Sputtering of a 35 nm layer of Ti and a 315 nm layer of Pt. Ti is used as an adhesive between the Pt and Si substrate.



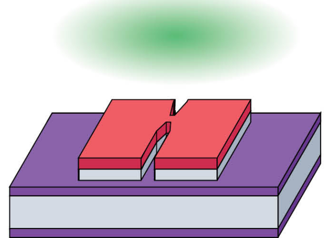
5c) Liftoff using a solvent stripper and ultrasonication.

Figure 4.7 – Lithography step # 5: Schematic illustration of the nanofabrication processes for depositing platinum (Pt) power and signal contacts.

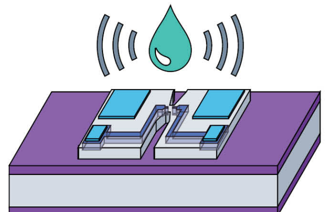
Lithography Step #6: Silicon Mesa



6a) Photolithography of the Si mesa.



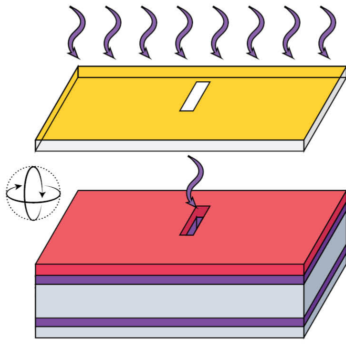
6b) DRIE of the Si mesa.



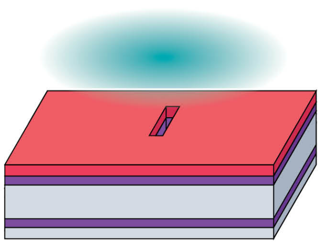
6c) Photoresist removal using a solvent stripper and ultrasonication.

Figure 4.8 – Lithography step # 6: Schematic illustration of the nanofabrication processes for etching the silicon (Si) mesa.

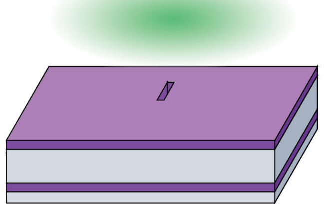
Lithography Step #7: Thermally Isolated Silicon Bridge



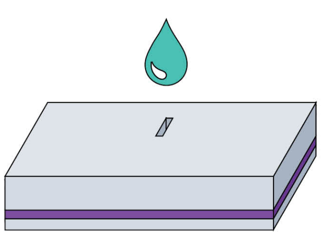
7a) Photolithography of a hole on the handle side for the thermally isolated Si bridge.



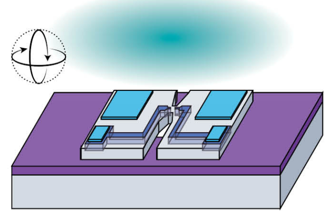
7b) RIE of the handle side oxide to be used as a mask for DRIE.



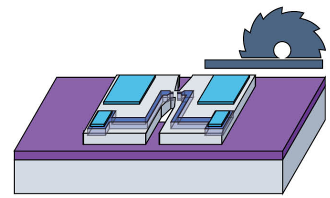
7c) DRIE etching of the handle layer, and BOX layer. Photoresist and most of the handle oxide is also etched away in the process.



7d) Removal of the crystal bond used in DRIE using hot water, and removal of photoresist residue using a hot solvent stripper.



7e) RIE oxygen plasma to clean any remaining photoresist residue.



7f) Dicing the blocks (5 devices per block) into individual 12.05mm x 2.55mm devices.

Figure 4.9 – Lithography step # 7: Schematic illustration of the nanofabrication processes for etching out a hole for the thermally isolated silicon (Si) bridge. Processes take place on the handle (back) layer of the sample block to etch out the handle and buried oxide (BOX) layers of the device.

4.4 Bulk of the Macro-to-Atom Device (I)

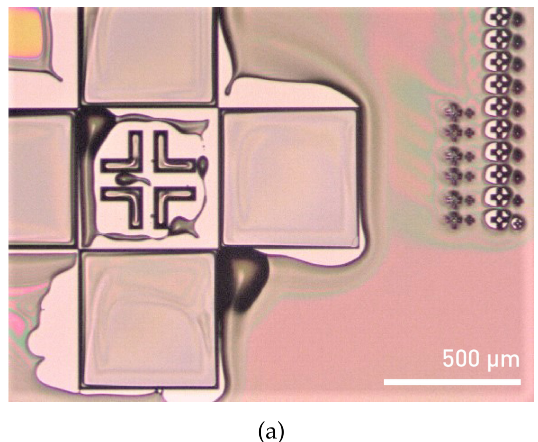
A first prototype of the bulk of the macro-to-atom device (Fig. 4.1a) has been successfully fabricated. Most revisions in the process flow for the second prototype were simply overlooked design flaws that were discovered from fabricating the first prototype. However, one of the more problematic issues was in surface contamination found through STM imaging and required extensive testing to solve. Upon improving the process flow and design, fabrication for a second prototype has started but has not been completed.

4.4.1 Design Revisions

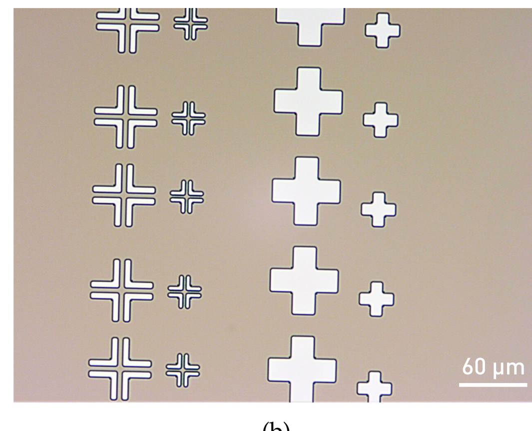
Alignment Marks

Alignment marks are utilized to align subsequent layers of lithography to the correct pattern layout [3]. Because conduction lines are implanted and not optically visible, alignment marks are even more critical to ensure proper pattern positioning. In "lithography step # 1 (Fig. 4.3)" for the first prototype, the alignment marks were etched down 20 µm to the middle oxide layer of the substrate. Upon applying the next lithography step, the photoresist struggled to evenly spin-coat around the deep alignment features as shown in Fig. 4.10a. Although the alignment marks had uneven resist coverage, the primary patterning of the conduction lines remained mostly sharp and fabrication proceeded.

For the second prototype, alignment marks were only etched down ~243 nm compared to the previously etched 20 µm alignment marks. As shown in Fig. 4.10b, this alleviated the issue of spin coating uneven photoresist in subsequent lithography steps. Although the alignment marks are more difficult to see optically due to a lack of contrast in depth, the following lithography step is still successfully performed using the alignment marks.



(a)

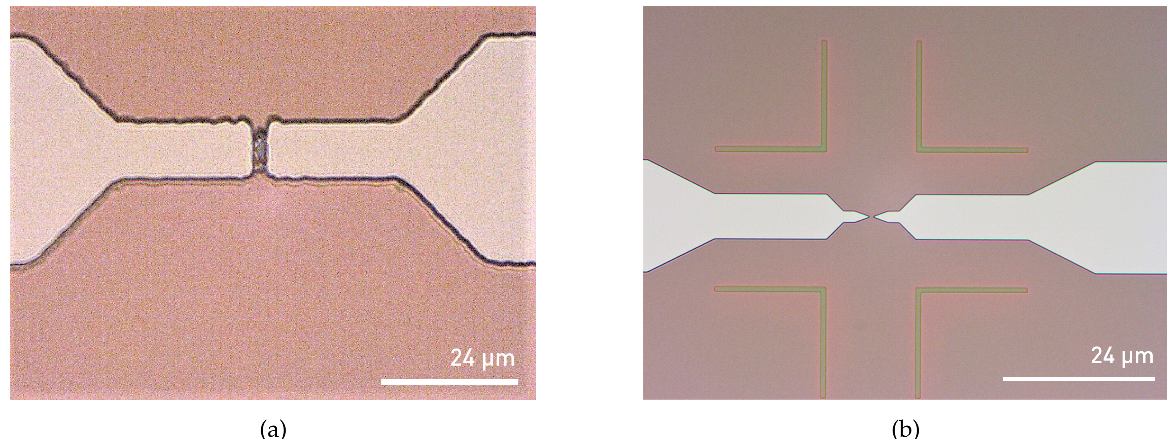


(b)

Figure 4.10 – **(a)** Prototype # 1: Spin coating photoresist evenly around deeply etched alignment marks (~20 µm) is difficult to achieve. **(b)** Prototype # 2: In only etching 243 nm deep alignment marks, photoresist in the subsequent lithography step is evenly spin coated.

Device Gap

In the first prototype, the majority of patterning in "lithography step # 2 (Fig. 4.4)" maintained pattern fidelity. However, the flat ends of the conduction lines seemed to cause an uneven spin-coating of resist in the gap between the two conduction lines as shown in Fig. 4.11a. This is caused by an optical proximity effect due to the flat contacts being too close in proximity [47, 52]. Ion implantation has a minimum required resist thickness of 0.5 µm to successfully block out incoming high energy ions [44]. The device's 2 - 4 µm gap between the flat contacts is too small to accurately pinpoint with an ellipsometer to get an accurate measurement of the resist thickness. If the resist is too thin, ions during implantation can penetrate through the resist and into the substrate. This could cause issues for the atomic circuitry sitting on the surface. In sharpening the ends of the contacts to a point in the second prototype, the photoresist is evenly spin-coated as shown in Fig. 4.11b.



(a) (b)

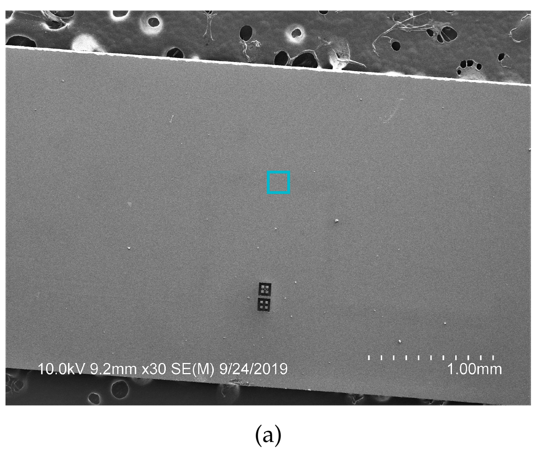
Figure 4.11 – **(a)** Prototype # 1: An optical proximity effect causes uneven spin coating of photoresist in the 2 μm gap between the two flat ends of the conduction lines at the center of the macro-to-atom device. **(b)** Prototype # 2: In tapering the contacts to a point, the optical proximity effect is circumvented, and resist is evenly spin coated.

Guiding Marks

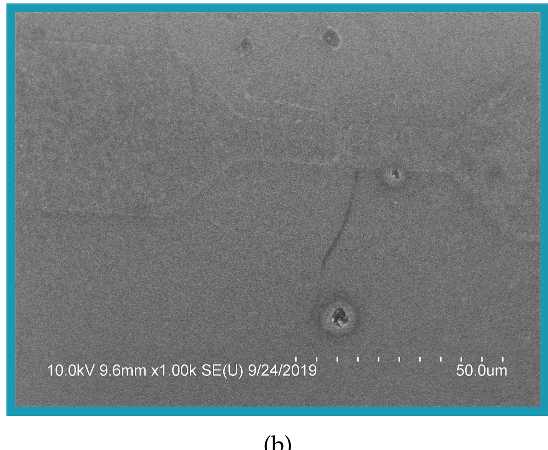
As previously mentioned, the ion implantation pattern is difficult to see optically. As shown in Fig. 4.12, even with SEM imaging using backscattered electrons, which typically allows for deeper substrate imaging, the As conduction lines are still difficult to observe [62]. To pinpoint the center region where the gap is, crosshair guiding marks are etched in for the second prototype as shown in Fig. 4.11b.

4.4.2 Process Flow Revisions

Upon STM imaging an ion implanted sample, contamination covering the entire surface was found, preventing any legible STM images. Although the original W-Si macro-to-atom device had metal particulates contaminating the center region, good STM images displaying the Si step edges were still obtainable. To isolate the source of contamination, each nanofabrication process performed on the implanted macro-to-atom device but not on the W-Si macro-to-atom device, were individually performed and followed with STM imaging.



(a)



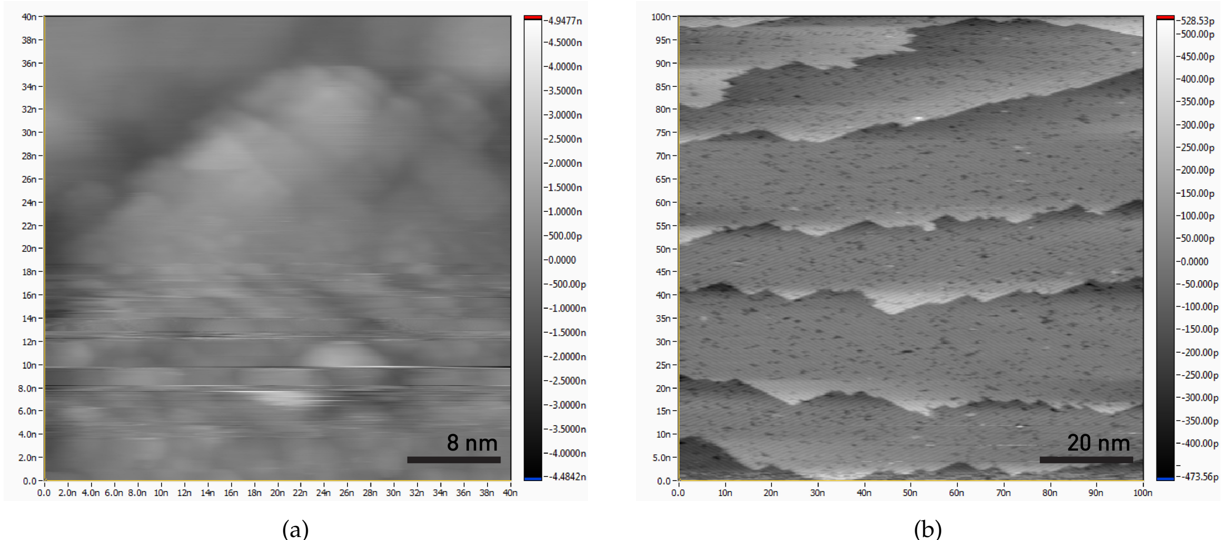
(b)

Figure 4.12 – Scanning electron microscope (SEM) images of the first completed prototype. **(a)** The heavily-doped arsenic (As) conduction lines can faintly be seen. **(b)** Zoom in of (a).

Removal of Carbonized Photoresist

Typically, photoresist is easily removed with a solvent stripper alongside ultrasonic agitation [3]. However, after implantation, the resist remained uncompromised using the same methods. The high energies used in ion implantation carbonized the resist, forming extremely durable polymer bonds [44].

In the first implanted prototype, an oxygen plasma was used for 10 min to ash the resist off. In measuring with an ellipsometer, the measurement showed no signs of photoresist suggesting all resist had been removed. However, upon STM imaging, the images appeared contaminated as shown in Fig. 4.13a. It is a strong possibility that a minuscule amount of resist residue remained and could not be read with the ellipsometer. In a second test, the oxygen plasma cleaning was doubled in time and a solvent stripper introduced halfway between plasma cleaning. In STM imaging the sample as shown in Fig. 4.13b, the Si step edges are seen, ensuring that the resist has been successfully stripped off the surface.



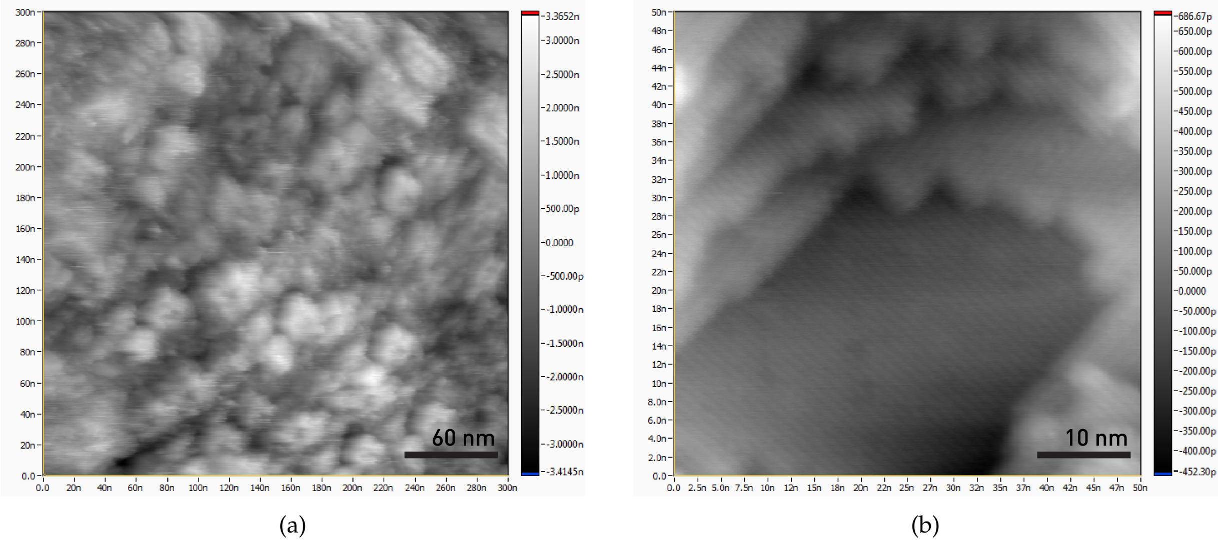
(a) (b)

Figure 4.13 – Scanning tunneling microscope (STM) images of samples flashed at 1050 - 1200 °C following different processes to remove carbonized photoresist: **(a)** 10 min of an oxygen plasma clean is not sufficient in cleaning the carbonized photoresist, as a clear STM image of the silicon (Si) surface could not be resolved following several 1050 °C flashes due to contaminants. **(b)** 10 min of an oxygen plasma clean, followed by a 10 min bath of a solvent stripper, and then another 10 min of an oxygen plasma clean is sufficient in cleaning the carbonized photoresist. Following several 1200 °C flashes, the step edges of a clean Si surface can be seen in the 100 nm window. (STM experimentation and imaging in (a) and (b) courtesy of Hedieh Hosseinzadeh, QSi.)

Removal of Oxide

Following implantation, annealing is performed to repair the substrate's crystalline structure and reposition the dopants into substitutional lattice sites. [3, 56]. Using PECVD, a layer of SiO_2 is deposited on the wafer's surface to act as a diffusion barrier, protecting dopants from escaping during annealing. Following annealing, the oxide is etched away with HF. The tool used for vapour HF etching was also a strong candidate as the contamination source, as the chamber used for etching is also used by others in fabricating MEMS. The chamber walls may have been contaminated with other materials, which may flake off when etching the oxide and

attach onto the Si surface. As shown in Fig. 4.14a, the Si step edges can not be seen in the STM following a vapour HF etch in removing the SiO_2 layer.



(a) (b)

Figure 4.14 – Scanning tunneling microscope (STM) images of samples flashed five times at 1050 °C following different processes to remove a 500 nm layer of silicon dioxide (SiO_2): **(a)** Vapour hydrofluoric acid (HF) etching is not sufficient, as a clear STM image of the silicon (Si) surface could not be resolved due to contaminants. **(b)** Liquid HF etching is sufficient, as the step edges of a clean Si surface can be seen in the 50 nm window. (STM experimentation and imaging in (a) and (b) courtesy of Hedieh Hosseinzadeh, QSi.)

Vapour HF etching is often preferred over a liquid HF bath, as the automation of the tool is easier and safer to operate, and allows for a significantly higher degree of control and reproducibility [63]. For comparison, an implanted sample with a 500 nm layer of SiO_2 was wet etched in a chemical bath of 10:1 BOE, which is composed of 10% liquid HF [53]. With an etch rate of 510 - 580 Å/min, the substrate was left in the bath for 15 min to remove the 500 nm SiO_2 layer. Upon STM imaging the sample as shown in Fig. 4.14b, the Si step edges are seen, suggesting the switch to a chemical bath solved the contamination issue.

Summary

Using methods of a longer oxygen plasma cleaning followed by a bath of solvent stripper and ultrasonic agitation to remove the carbonized photoresist, and using BOE to remove the SiO_2 mask, seem to be sufficient in resolving a clean Si surface. However, the longevity of the clean Si surface still needs to be looked into. As the remaining steps will require more than a month of processing, there are still questions on how long the surface can remain clean and contaminant-free idly sitting within the nanofab cleanroom.

4.5 Center Electron-Beam Lithography Patterned Contacts (II)

One of the greatest challenges in utilizing atomic circuitry is in making a reliable interconnection between the electrical contacts and atomic wires [17, 30]. EBL is utilized when feature sizes are too small for optical lithography. The diffraction limit of the nanofab's optical aligners do not allow for feature sizes smaller than ~1 - 2 µm [3, 43]. At the center of the macro-to-atom device, the conduction lines narrow down from 50 µm to 200 nm in width, and the gap is further decreased from 2 µm to a 300 nm gap (Fig. 4.1). These smaller contacts are the intermediate contacts to scale between atomic circuitry and implanted As conduction lines. Additionally, narrowing the gap helps accommodate the STM patterning window as the 2 µm gap is too wide for efficient atomic-scale lithographic patterning [16].

Samples of just the central EBL patterned contacts that would scale between the wider As conduction lines and atomic-scale lithographic patterns fabricated between the center gap on the macro-to-atom device were independently fabricated as shown in Fig. 4.15a. Using a multi-probe STM (MP-STM) with a built-in SEM, the samples were tested, bypassing the conduction lines connecting to Pt signal contacts of the larger device, thus omitting the majority of device fabrication required. The advantage of MP-STMs is that they typically have four probes that are independently operated, allowing the measurement of a sample's electronic transport

properties [15]. Samples of EBL patterned 20 nm thick Ti on heavily-doped n-type Si were first tested, and further tests involving 20 nm deposited on lightly-doped n-type Si are currently being conducted. Although the EBL contacts would be implanted with heavily-doped As on a lightly-doped substrate on the final macro-to-atom device, the contacts are fabricated with a 20 nm thick Ti for current experimentation. This is due to the contrast that Ti provides on the Si surface, allowing the SEM within the MP-STM to find the area of interest to land on. As was shown previously in Fig. 4.12, even a much more capable SEM had difficulty in locating the large implanted contacts. Although the EBL contacts were patterned to have a 300 nm gap, following development and lift off, the resulting gap is ~600 nm as shown in Fig. 4.15b.

4.5.1 Patterning of Dangling Bond Wires

In applying voltage pulses with the STM tip to locally desorb a H atom off of the Si surface, a DB forms, creating a surface state within the E_G of the passivated Si substrate [1, 16, 64]. DB wires can then be fabricated by selectively removing a series of H atoms parallel or perpendicular to dimer rows [16, 65]. Although the DBs in both cases have their energy states lie within the E_G, DB coupling differs in each case. DB wires perpendicular to dimer rows exhibits very little coupling between DB dimers, in contrast with DB wires parallel to the dimer rows which demonstrate substantial through-lattice and through-space coupling [16, 65]. Therefore, DB wires parallel to the dimer rows experience higher conductance and can behave as a 1D quasi-ballistic wire. DB wires perpendicular to the dimer rows can still be utilized for purposes such as logic gates, as the smaller coupling between dimers allows for better control of current [16].

Direct coupling between DBs is thought to be what allows transmission through the wires, however, the host substrate is also critical in effecting electronic transport [16]. Additionally, as the goal for the device is for CMOS compatibility, the DB wires need to be connected to external circuitry via the center EBL contacts. One of the biggest challenges in interfacing between atomic and CMOS circuitry is in fabricating direct contacts to the DB wires with the correct transport properties [30].

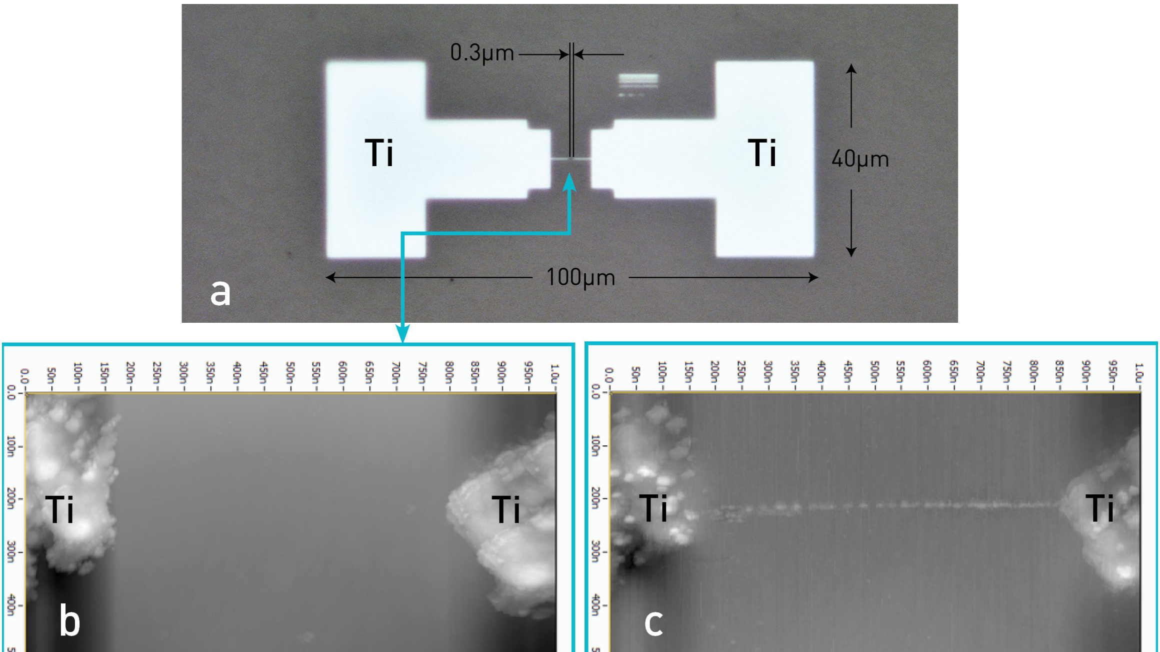


Figure 4.15 – **(a)** Electron-beam lithography (EBL) patterned contacts. The contacts are 20 nm thick titanium (Ti) contacts with an intended gap of 300 nm, fabricated on a lightly-doped n-type substrate (1 - 5 $\Omega \cdot$ cm) . **(b)** 1.0 µm x 500 nm scanning tunneling microscope (STM) image of the gap between the two Ti contacts. Although the gap was fabricated to be 300 nm wide, the gap appears ~300 nm wider. This could be attributed to material loss from liftoff, or a slight over development of photoresist after EBL patterning. **(c)** Using field emission (10 V, 2 nA) of the STM tip, a dangling bond (DB) wire is patterned between the two Ti contacts. (STM experimentation and imaging in (b) and (c) courtesy of Jo Onoda, University of Alberta.)

Many proposed methods suggest simply connecting the fabricated DB wires with metallic nanopads [17]. Having a good contact between the metallic contacts and DB wire is required to maximize conductance, but is more challenging to make in practice. Using field emission (2V, 2nA) of the STM tip, the MP-STM patterned a coarse DB wire between the two Ti electrodes as shown in Fig. 4.15c, d. One challenge in patterning the DB wire was that the bluntness of the STM tip would interfere with the Ti contacts, making DB patterning near the edge of the raised Ti contacts extremely difficult as shown in Fig. 4.16. If the DB wire does not meet the edge of the contacts, the DB wire is no longer continuous. The future device of solely implanted As contacts would be able to circumvent this issue, with patterning capable even over top the doped contacts to ensure continuity for maximum conductance.

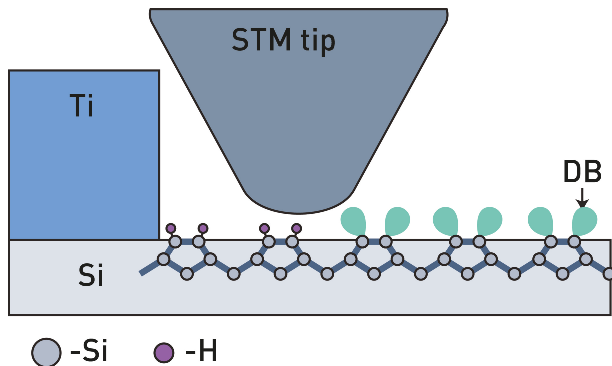


Figure 4.16 – Scanning tunneling microscope (STM) patterning of a dangling bond (DB) wire to connect to a titanium (Ti) contact. The raised Ti contact makes it difficult for the STM tip to pattern a continuous DB wire connecting to the Ti contact.

Electronic homogeneity is also disrupted with the introduction of electrodes such as the center EBL contacts [16]. By applying a bias voltage to the contact junction, a tunneling current passes through the DB wire. Ballistic electrons propagating from the contacts to the DB wire will experience a built-in potential (Φ_B) as shown in Fig. 4.17. Theoretically, Φ_B is calculated by subtracting the metal work function (Φ_M) by Si's electron affinity (X_{Si}) [37]. Thus, by increasing N_D, a very low barrier height can be achieved, which in turn reduces contact resistivity. However, the experimentally determined Φ_B is mostly independent of Φ_M and X_{Si} due to Fermi

surface level pinning near the VB, making a low Φ_B difficult to achieve [66, 67]. Even if the Si electron affinity is larger than the metal work function, a negative Φ_B can not be achieved.

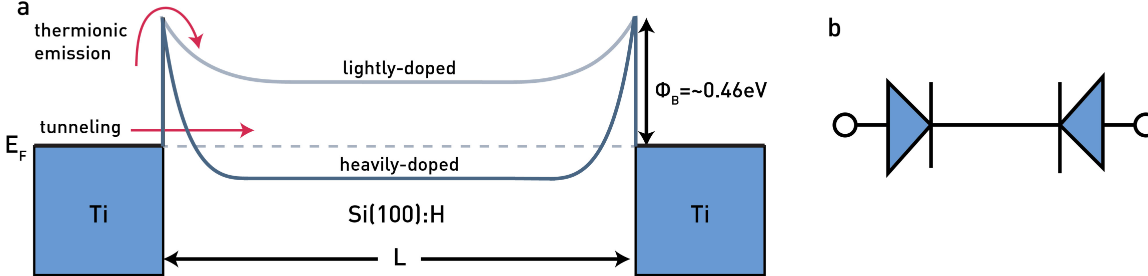


Figure 4.17 – **(a)** Energy diagram of electron-beam lithography (EBL) patterned diagram (Ti) contacts on an n-type silicon (Si) surface. Φ_M is ~0.46 eV for any value of dopant concentration (N_D). However, (N_D) affects the barrier width, which in turn affects the mechanism for electron transport. Conduction through a lightly-doped n-type Si interface is through thermionic emissions, while conduction through a heavily-doped n-type Si interface is mostly through tunneling. **(b)** The contacts are treated as back-to-back diodes.

A Ti/n-Si interface has been found to have a Φ_B of ~0.46 eV, independent of the N_D [67]. However, N_D affects the width of Φ_B, which affects the mechanism for electrical conduction through the contacts. Conduction through a lightly-doped n-type Si interface is through thermionic emissions, while conduction through a heavily-doped n-type Si interface is largely through field emission as shown in Fig. 4.17.

The DB wires, Si substrate, and contacts must all be accounted for in designing a complete circuit. Understanding how the conductive contacts interact with the atomic circuitry and perturb the transmission spectra will be required before designing a fully functioning device [16].

4.6 Embedded Antimony Reservoir (III)

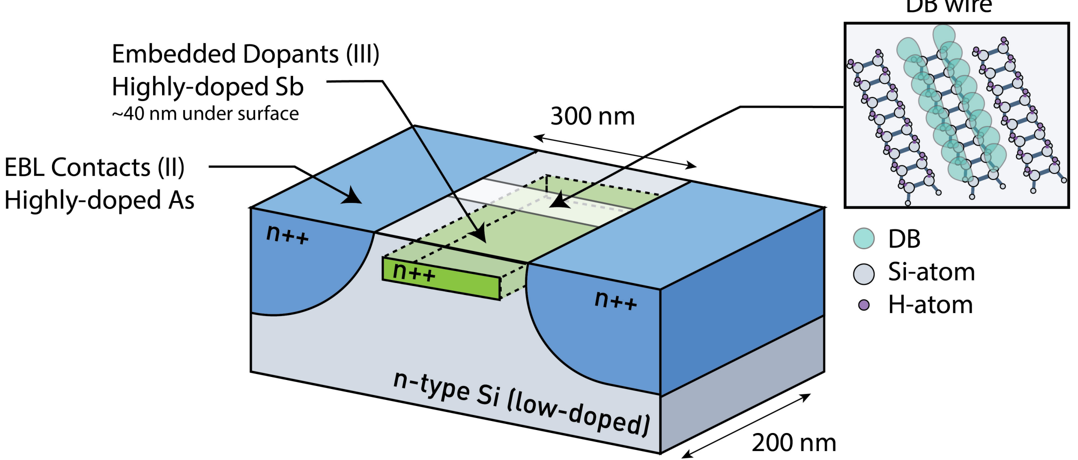


Figure 4.18 – Illustration of the embedded heavily-doped antimony (Sb) region that sits 40 nm under the surface of the macro-to-atom device. Dangling bond (DB) wires are patterned between the device's 300 nm center gap and above the embedded heavily-doped Sb region. The heavily-doped Sb region sits 40 nm under the surface, and is not connected to the heavily-doped EBL contacts.

The basis of STM operation uses electron tunneling between a tip and sample, therefore, the sample needs a sufficient amount of free carriers for imaging to be possible, which the heavily-doped substrate of the initial W-Si device provided [10]. However, the implanted device is fabricated on lightly-doped Si to avoid large body currents and to contrast the heavily-doped implanted conduction lines. At the low temperatures of STM operation, carriers experience a freeze-out due to the lack of thermal energy available to ionize impurities [32, 37, 38]. Increasing semiconductor doping increases the threshold before experiencing carrier freeze-out, and degenerately doped semiconductors do not experience carrier freeze-out at all [38]. Therefore the center of the device requires a reservoir of carriers provided from heavily-doped impurities embedded within the lightly-doped bulk for STM operation as shown in Fig. 4.18. The exact

placement and dimensions of the heavily-doped reservoir are not fully resolved yet. Surfaces without the heavily-doped reservoir underneath to provide carriers would be seen as a blind-spot in the STM, creating a possibility for tip crashes. However, the embedded reservoir should not be electrically connected to either electrode or be too close to the surface, as that could create a short in the device for the atomic circuitry sitting above on the surface [16]. However, the reservoir still needs to be sufficiently close to the surface to cause DBs to be negatively charged [61].

A neutral DB (DB^0) inherently hosts a single electron but is capable of hosting another electron of opposite spin and allowing the DB to be negatively charged (DB^-) [61]. Due to Coulomb repulsion, two DB^-s in close proximity can not form a $DB^- - DB^-$ pair. Instead, the two DBs can share an extra electron which tunnels between the coupled $DB - DB^-$ pair and could be ideal for use in computing. This extra electron is easily provided by a donor atom in heavily-doped n-type Si due to the substrate's high E_F even at low temperatures. In addition to serving as a classical bit, Livadaru et al. (2010) have demonstrated that a $DB - DB^-$ pair shows strong potential as a charge qubit due to the proximity of DBs leading to high tunneling rates, prompting excellent coherence properties.

4.6.1 Effects of Rapid Thermal Annealing on the Antimony Dopant Profile

Sb is chosen as the dopant for the embedded doped reservoir, as a heavier element such as Sb provides a sharper and narrower dopant profile (smaller ΔR) compared to a more conventionally used dopant such as P or As [3]. Another attractive property of Sb is its low diffusivity during annealing [4]. Anytime a substrate undergoes high energy ion implantation, it must be annealed at high temperatures to activate the dopants and to repair the substrate's crystalline structure [3, 44]. The applied heat can cause diffusion of dopants, causing the dopants to migrate and accumulate too closely to the surface. However, a larger element such as Sb has been shown to have lower diffusion during annealing compared to P or As [4].

Dalponte et al. (2009) performed a study using medium energy ion scattering (MEIS) to compare the dopant profiles of ion implanted As and Sb in (100) SOI and p-type Si substrates with a ρ of 2 - 10 Ω·cm (lightly-doped) following different annealing processes [4]. The pre-annealing implantation profiles for both As and Sb appear very similar, but substantially diverge following both RTA and FA processes. The dopant concentration profiles following RTA and FA of ion implanted As and Sb in a (100) SOI wafer are compared and summarized in Tab. 4.2. In employing RTA at 1000 °C for 10 s, As showed considerable diffusion with a strong accumulation of As at the SiO_2 surface interface which is used as a diffusion barrier. While Sb displayed very little diffusion under the same RTA process with the annealed dopant profile remaining nearly identical to the original as-implanted distribution. With FA at 1000 °C for 15 min, diffusion is even more apparent in As. The dopant distribution profile in the Si bulk is almost entirely flattened with no visible peak, but with a strong accumulation of dopants at the SiO_2 surface interface, and a considerable amount of dopant loss through the SiO_2 surface interface. Sb under the same FA parameters experienced yet again very little diffusion. With its annealed dopant profile comparable to the original as-implanted profile, with the exception of a decrease in its overall concentration and small accumulation at the surface oxide.

4.6.2 Secondary Ion Mass Spectroscopy Analysis on the Embedded Antimony Profile

Due to the proximity of the embedded dopant reservoir to the Si surface, RTA is utilized over FA to minimize dopant diffusion. Through analysis with secondary ion mass spectroscopy (SIMS), the effects of RTA on the sample at various temperatures and durations can be investigated. SIMS utilizes an ion beam directed onto the sample's surface to emit atoms known as secondary ions from the surface, to be extracted into a mass spectrometer to identify the element [68].

Sample #1 is used as a control sample, with no annealing performed. In implanting Sb with a dose of $1.8 \cdot 10^{14}$ $ions \cdot cm^{-2}$ at 100 keV, the as-implanted dopant profile shows the dopant peak between ~45 - 55 nm from the surface as shown in Fig. 4.19. Sample #2 was annealed at 900 °C

Table 4.2 – Distribution of dopants in a (100) silicon-on-insulator (SOI) wafer following rapid thermal annealing (RTA) and furnace annealing (FA) as a percentage of the original implanted dose ($5 \cdot 10^{14}\ cm^{-2}$).

Dopant	Annealing Process	Overall % of Retained Dose	% of Accumulated Dose at the Surface Oxide Interface	% of Non-accumulated Dose in the Bulk
As	RTA (1000 °C for 10 s)	92	20	72
	FA (1000 °C for 15 min)	64	32	32
Sb	RTA (1000 °C for 10 s)	94	10	84
	FA (1000 °C for 15 min)	94	28	66

Note. * **Data adapted from "Effect of excess vacancy concentration on As and Sb doping in Si" by Dalponte et al., 2009, Journal of Physics D: Applied Physics 42. Copyright 1969, by permission of IOP Publishing [4].**

for 90 s, and shows the peak has shifted to ~8 nm from the surface, which is unexpected. As evident in Dalponte et al.'s (2009) study, the Sb profile on a lightly-doped (100) SOI substrate is not expected to dramatically diverge from the original as-implanted profile following RTA or even a longer FA [4]. It is not too unexpected to observe a slight broadening of the dopant distribution peak, but to obtain a narrower distribution and have a significant shift in depth of the peak is contradictory to literature [4, 56]. A second sample that has undergone the same anneal steps has been sent in for reanalysis.

A possible solution to circumvent further diffusion with RTA, is that the flashing involved with STM sample preparation could suffice in activating the dopants and repairing the crystal structure [69]. A sample has been prepared in the STM with 5 flashes of 800 °C, but will not be submitted for further analysis until the previous RTA reanalysis is completed.

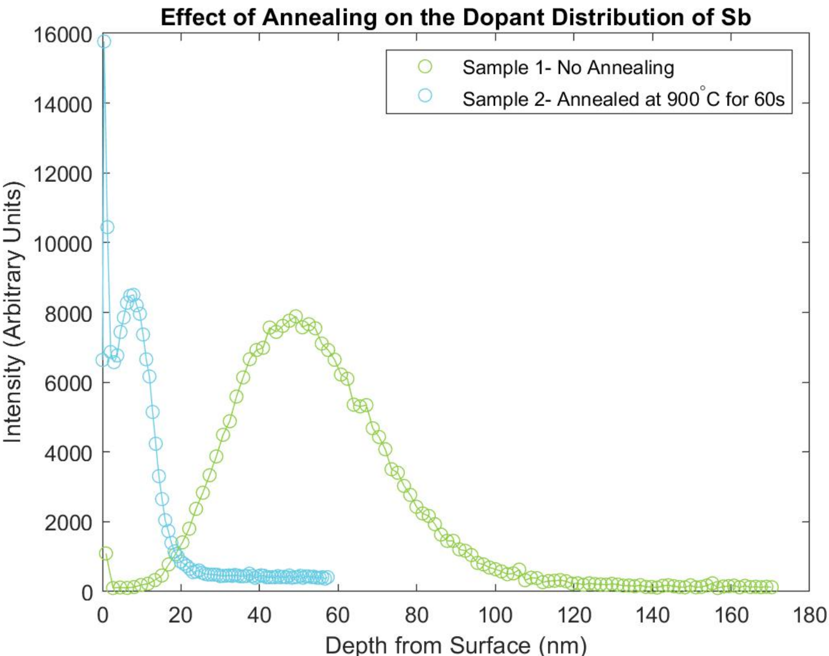


Figure 4.19 – Change in dopant distribution profile following rapid thermal annealing (RTA). Secondary ion mass spectroscopy (SIMS) data collected and used in the plot is courtesy of the University of Alberta Nanofab characterization/sample analysis team.

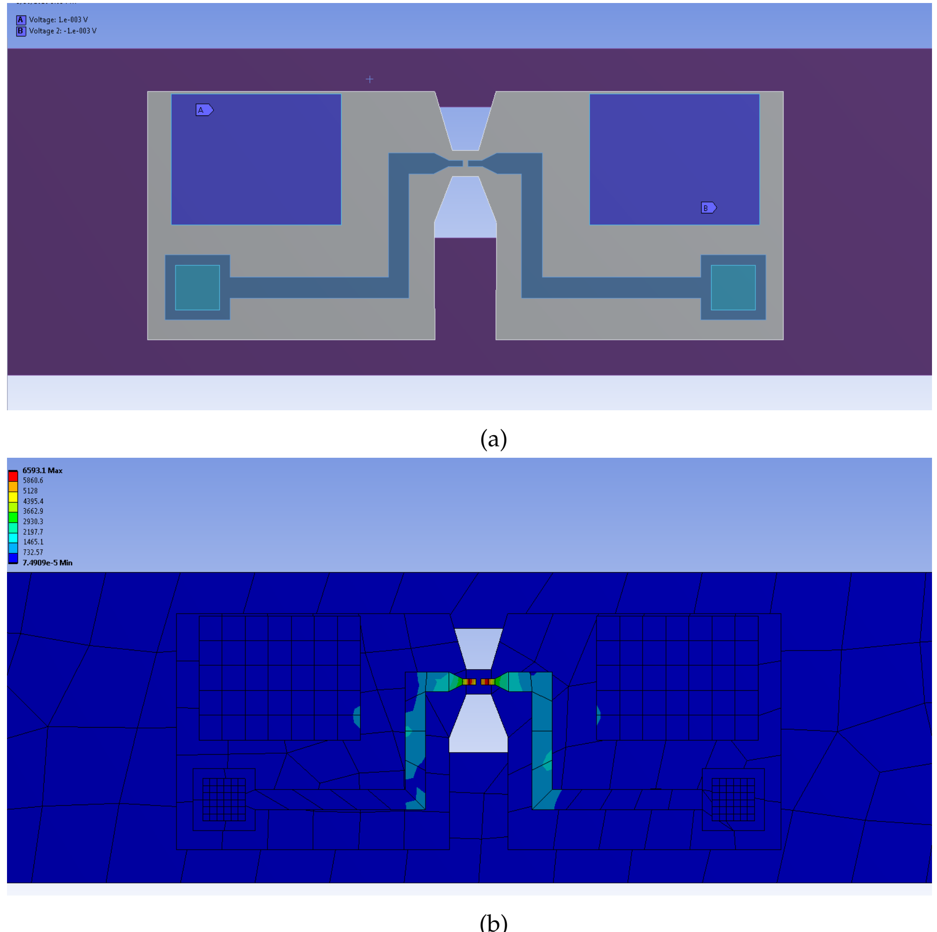
05

Future Outlook

Ch. 4 demonstrates the progress made in realizing a fully functioning macro-to-atom device. However, as mentioned, significant challenges remain that are still currently being addressed through experimentation and further prototyping. Several other issues integral to understanding and completing the macro-to-atom device but have not received proper attention due to time constraints are highlighted below.

5.1 Finite Element Simulations

The original W-Si macro-to-atom device has been tested and prepared in an LT-STM. The heat density upon flashing can partially be seen through the STM camera as was previously shown in Fig. 1.2b (Ch. 1), where the center region glows increasingly red, indicating the heat is concentrated only at the center. However, obtaining a detailed evaluation of the current density could help provide insight to help optimize device geometry and design parameters. Ansys Student, a finite element analysis software was employed in an attempt to simulate the device and analyze its electrical and thermal properties. The original macro-to-atom W-Si device is used as an initial benchmark, as the device had been previously prepared in the STM and we understand some of the device's behaviors. Material properties such as ρ are applied to a CAD model of the device as shown in Fig. 5.1a. A bias voltage of 0.1 V and -0.1 V is applied to each



(a)

(b)

Figure 5.1 – Finite element simulations using Ansys Student. **(a)** CAD model of the tungsten-silicide (W-Si) macro-to-atom device with applied material properties. Bias voltages are applied to the large platinum (Pt) power pads. **(b)** Simulation of the current density of the W-Si macro-to-atom device during high temperature scanning tunneling microscope (STM) flashing.

of the Pt power contacts in the simulation to emulate the high-temperature surface preparation. The current density during a single high-temperature flash is shown in Fig. 5.1b. However, the simulations do not seem entirely accurate as greater current flow through the bulk is expected. This error could be attributed to the treatment of the thin 35 nm conduction lines as a 2D surface over the Si bulk in the simulation. The simulations require more refinement, but due to time

constraints, other members of the Wolkow group will continue with the finite element analysis of the macro-to-atom device.

Another useful analysis would be in measuring current leakage upon using the Pt signal pads for signal injection and measurement. The next steps following a successful analysis of the current leakage in the W-Si macro-to-atom device, would be to perform a comparison of leakage currents in the implanted sample at the different temperatures of STM operation (4 K - 300 K). The previously calculated behavior of carrier concentrations as a function of temperature (Ch. 2) can be utilized to infer the ρ at different temperatures of the lightly-doped bulk and heavily-doped conduction lines. The thermal stress from flashing could also then be calculated. Each subsequent flash provides a cleaner surface, but a trade-off is that an excess of flashes can fracture the thermally isolated Si bridge and deteriorate the bridge completely. Analyzing the thermal stress can provide insight to an optimal number of 1000 °C flashes without risking damage to the device.

5.2 Further Prototyping

Each iteration of device fabrication aids in gaining further insight into overlooked challenges and flaws in the design and process flow, which are then improved upon in the next prototype. Fully completing a second prototype with the current improvements on minimizing surface contamination should be the next step moving forward in further refining the implanted macro-to-atom device. The university nanofab has recently acquired a direct-write lithographic tool with a resolution similar to EBL but with higher throughput. This could allow for the As conduction lines and EBL contacts to be combined and patterned simultaneously, saving time and resources by reducing an entire lithographic and implantation step.

Another possibility is to explore the use of the same heavily-doped As conduction lines, but in a heavily-doped p-type SOI substrate. Many parameters for the heavily-doped embedded

reservoir still need to be further refined; area dimensions and annealing parameters require more extensive analysis. Once the EBL contacts and embedded dopant reservoir of the device are further realized, all three portions can then be implemented together in fabrication on a single device.

5.3 Scanning Tunneling Microscopy Testing and Tip Guiding

As the main objective of the device is to be able to successfully STM pattern atomic circuitry on the surface, the device needs to be thoroughly tested in the STM. The W-Si macro-to-atom device has been previously prepared and imaged in STMs operating at room temperature, however LT-STM operation which is required for atomic-scale lithographic patterning is another challenge. Landing the STM tip on the W-Si macro-to-atom device is challenging enough even with the aid of the reflections from the W-Si conduction lines. Without any metal reflections or other landing guides, this could prove extremely challenging. Several ideas have been proposed to aid STM tip landing, including implanting heavily-doped guiding marks as shown in Fig. 5.2. The guiding marks would consist of concentric rings of increasing width and diameter. Upon landing on any quadrant of the device, the concentric rings could provide directions for the STM tip. In measuring the arc and thickness of the ring, the distance from the center could be determined. However, as the general design and process flow of the device already faced a substantial amount of challenges, the basic macro-to-atom device design and process flow was the priority. Implementing additional implantation steps for guiding marks into the design would further complicate the process flow. In successfully fabricating the basic macro-to-atom device, can guidance marks then be implemented.

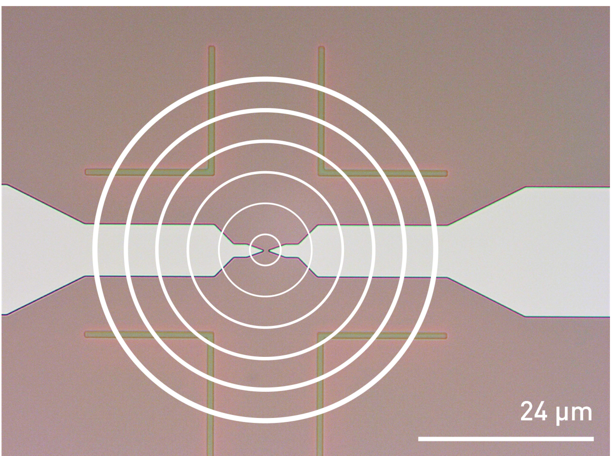


Figure 5.2 – Illustration of implanted guiding marks to aid in scanning tunneling microscope (STM) tip landing. Measuring the arc and thickness of the ring would determine the distance from the center.

5.4 Summary

The electronic properties of DB structures allow it to be utilized as atomic-scale memory, logic gates, and wires; creating a strong candidate for beyond-CMOS technology. However, DB circuitry awaits completion of the macro-to-atom interface. This thesis presents a design and nanofabrication process for a device capable of injecting and making signal measurements between CMOS and atomic circuitry. Atomic scale lithography is performed in an LT-STM, where part of the device is subjected to harsh conditions to prepare a pristine surface to be passivated with H. Due to the geometry of the device, the signal contacts where CMOS circuitry would later be fabricated could remain virtually unheated and undamaged while the center of the device reaches very high temperatures [1, 14]. By selectively removing H from the Si (100) 2x1: H surface and revealing a DB, patterns such as logic gates and conductive wires can be fabricated. Although the STM can operate at room temperature, working with cryogenic temperatures provide the thermal stability and precision required for selectively depassivating H.

The initial design of the device utilized a heavily-doped SOI substrate with W-Si conduction lines to interface between the CMOS and atomic circuitry, however, the design faced several challenges. The conductivity of the heavily-doped substrate would suffer from leakage currents. There were plans to minimize leakage currents by isolating the W-Si conduction lines from the Si bulk with a layer of oxide in between the two materials. However, the STM would still suffer in patterning continuous DB wires connecting to the W-Si contacts, as well as risk STM tip crashes. In heating the center region where atomic circuitry would be fabricated, the high temperatures also caused severe W-Si particle contamination in the center and the coagulation of W-Si particles caused a discontinuity in the conduction lines. Altogether, these issues could impede circuit functionality.

To circumvent the issues of the initial device, heavily implanted As would replace the W-Si conduction lines, and a lightly-doped substrate would be used in place of the heavily-doped substrate. However, in altering the device, other issues have been introduced. The processes involved in ion implantation introduced surface contamination issues but has been mitigated by modifying the nanofabrication process flow. In utilizing a lightly-doped substrate, not enough carriers would be present at low temperatures for the LT-STM to operate. A heavily-doped implanted region embedded below the surface is introduced to provide such carriers for STM operation, as well as provide the surface DBs with the required charge state.

Another big challenge was in interfacing between the atomic and CMOS circuitry and making transport measurements that have yet to be completed. Gaining insight into how the conductive contacts will interact with the DB wires and affect transmission will be required before designing a fully functioning device.

A preliminary design and prototype of the device demonstrates the feasibility of a device capable of macro-to-atom scale integration. Although there are still significant obstacles to overcomes there is substantial room for progress to be made in fully realizing the macro-to-atom device.

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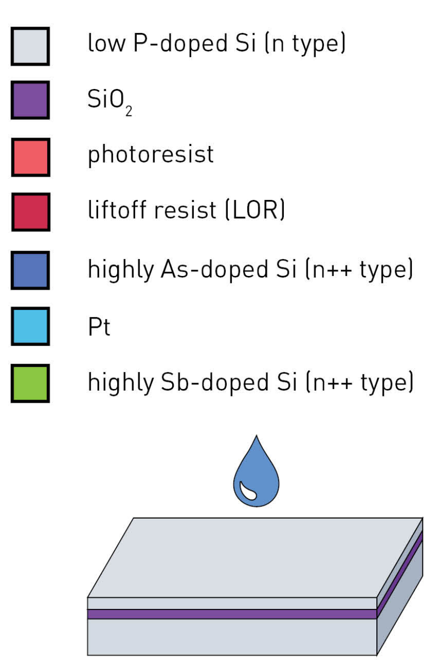
Appendix A

Detailed Nanofabrication Process for the Macro-to-Atom Device

Photomask #1: Etched Alignment Marks

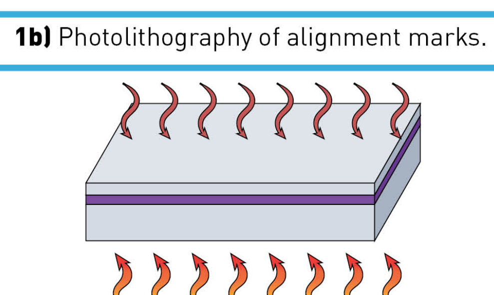
Figure A.1 – CAD drawing for the photomask used in etching alignment marks on a 4" wafer in lithography step # 1.

Lithography Step #1: Etched Alignment Marks

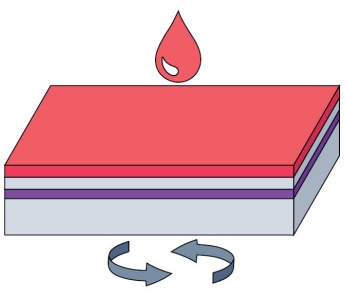


1a) Piranha clean a 4” SOI wafer:
Submerge in a chemical bath of 600 mL H_2SO_4 (96%) + 200 mL of H_2O_2 (30%) for a minimum of 15 min.

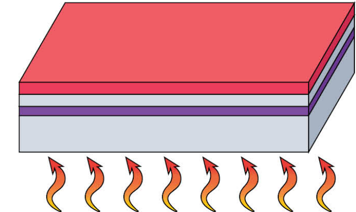
1b) Photolithography of alignment marks.



1b.1) HMDS bake and prime:
i. Dehydrate at 150 °C and purge O_2 from the chamber.
ii. Prime with HMDS vapour to increase the wafer’s adhesion to resist.



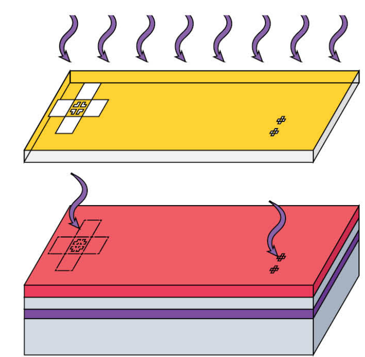
1b.2) Spincoat photoresist:
i. Apply 5 mL of “AZ1512” resist to the center of the wafer.
ii. Spincoat wafer for 10 s @ 500 RPM, then increase the speed to 40 s @ 5000 RPM.



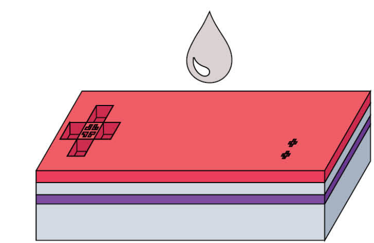
1b.3) Softbake:
Bake for 60 s @ 100°C to drive off solvents and harden the resist.

Figure A.2 – Lithography step # 1: Schematic illustration of the nanofabrication processes for etching alignment marks.

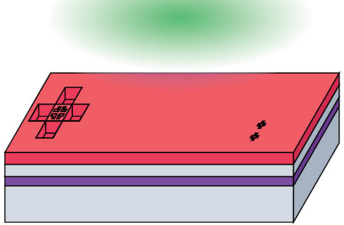
Lithography Step #1: Etched Alignment Marks (Continued)



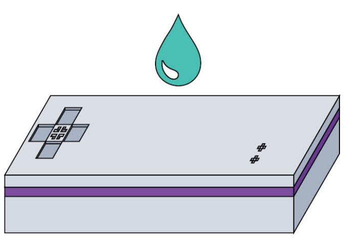
1b.4) Alignment and exposure:
Expose wafer to MASK#1 for 2.8 s under a Hg-vapour lamp.



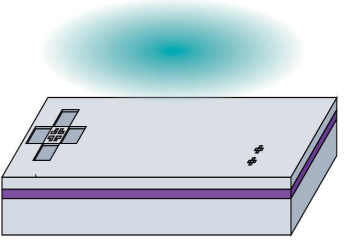
1b.5) Develop:
Develop in "AZ400K 1:4" developer for 45 s.



1c) DRIE (Bosch Process):
Using the recipe "Unswitched Process" with an etch rate of 7.3 μm/min:
i. Condition the chamber with a dummy wafer for 4 min.
ii. Process with the wafer (crystal bonded to another wafer that fits in the chamber) for 20 s to etch 243 nm alignment marks.



1d) Strip resist:
i. Soak in boiling water for 5 min to remove the crystal bond used from DRIE to bond the wafer.
ii. Soak in "Remover PG" for 10 min to strip the resist and reveal etched pattern.



1e) RIE to further clean any remaining residue:
i. Run recipe "Clean" on an empty chamber for 15 min.
ii. Run recipe "Descum/Strip" on the wafer for 5 min.

Figure A.2 – (Continued) Lithography step # 1: Schematic illustration of the nanofabrication processes for etching alignment marks.

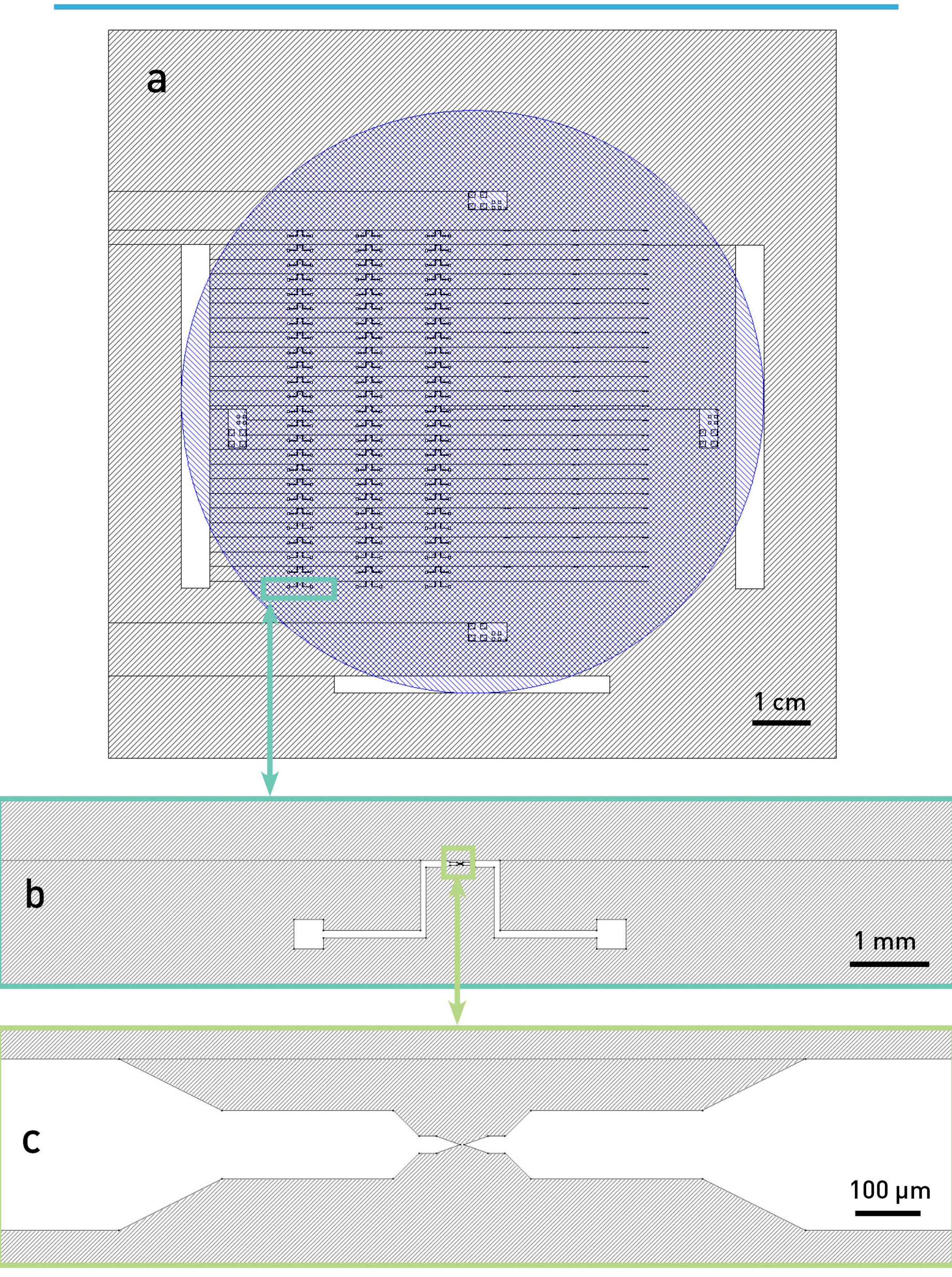
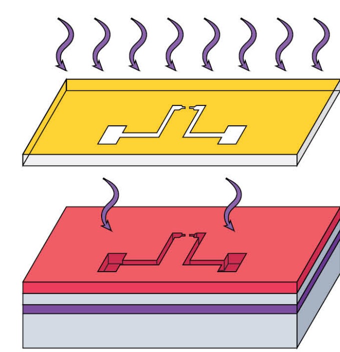


Figure A.3 – CAD drawings for the photomask used in implanting arsenic (As) conduction lines on a 4" wafer in lithography step # 2.

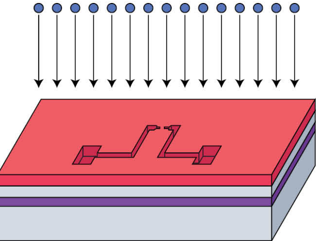
Lithography Step #2: Arsenic Conduction Lines



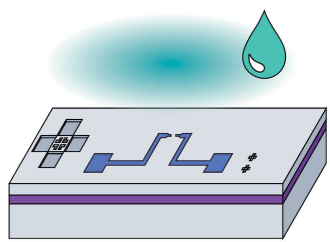
2a) Lithography:
i. HMDS bake and prime.

ii. Apply 5 mL of "AZ1512" resist at the center of the wafer.
iii. Spincoat wafer for 10 s @ 500 RPM, then increase to 40 s @ 5000 RPM.
iv. Softbake for 1 min @ 100 °C.
v. Expose to MASK #2 for 2.8 s.

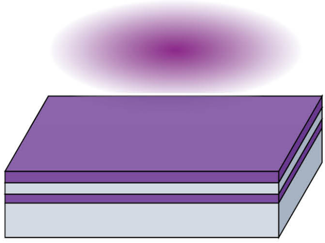
vi. Develop in "AZ400k 1:4" developer for 45 s.



2b) Ion implantation of 100 keV 75As+ ions with a dose of $3.00 \cdot 10^{14}$ ions · cm^{-2}. Outsourced to CuttingEdge Ions.



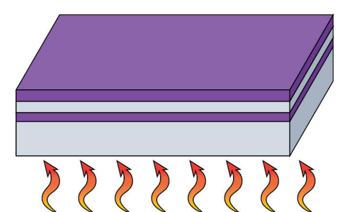
2c) Strip carbonized resist:
i. Run RIE recipe "Clean" on empty chamber for 15 min.
ii. Run RIE recipe "Descum/Strip" for 30 min.
iii. Soak in a chemical bath of "Remover PG" for 5 min.



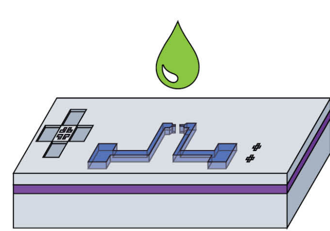
2d) PECVD to grow SiO_2 diffusion barrier to prevent dopants from escaping during annealing.
i. For better uniformity, deposit a 1 µm oxide film in the chamber by "oxide conditioning" for 500 s.
ii. Deposit 500 nm of "new oxide" on the device side by processing for 350 s.
iii. "Clean" the chamber for 1700 s.

Figure A.4 – Lithography step # 2: Schematic illustration of the nanofabrication processes for implanting heavily-doped arsenic (As) conduction lines.

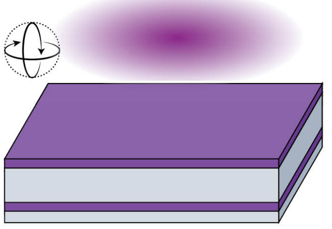
Lithography Step #2: Arsenic Conduction Lines (Continued)



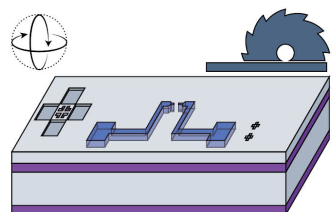
2e) FA to activate and drive in dopants:
Annealing with a N_2 carrier gas for 60 min @ 1050 °C with a 6 hr ramp down time, provides a junction depth of 0.65 um and dopant density of $4.2 \cdot 10^{19}$ ions · cm^{-3}.



2f) Oxide removal:
BOE 10:1 (NH_4F + HF) etches at 51-58 nm/min, therefore, a chemical bath of ~15 min is required to etch the 500 nm oxide.



2g) PECVD on handle (back) side:
To be used as an etch mask later on when etching out the hole for the thermal ly isolated Si bridge.
i. For better uniformity, deposit a 1 µm oxide film in the chamber by "oxide conditioning" for 500 s.
ii. Deposit 500 nm of "new oxide" on the device side by processing for 350 s.
iii. "Clean" the chamber for 1700 s.



2h) Dicing wafer into blocks:
MASK #1 etched dicing marks on the device side to guide where to dice.
Using the DISCO DAD 321 with the following settings: Ch1: 12.05 mm, Ch2: 12.55 mm, Speed: 2 mm/s to dice the wafer into 30 blocks. Any further processing is done on individual blocks. Each block contains 5 individual devices.

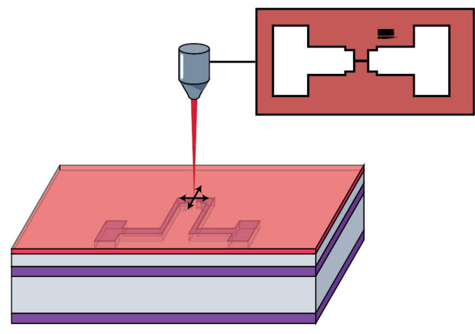
Figure A.4 – (Continued) Lithography step # 2: Schematic illustration of the nanofabrication processes for implanting heavily-doped arsenic (As) conduction lines.

EBL CAD Pattern #3: Arsenic Center Contacts

100 µm
200 nm
40 µm
300 nm

Figure A.5 – CAD drawing for the electron-beam lithography (EBL) design used in patterning heavily doped arsenic (As) contacts between the 2 - 4 µm gap in the center of the previously implanted As conduction lines in lithography step # 3.

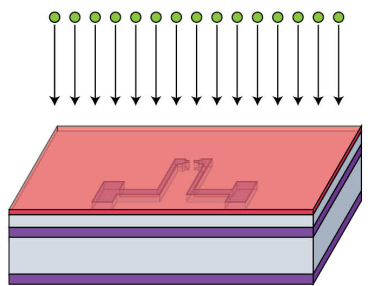
Lithography Step #3: Arsenic Center Contacts



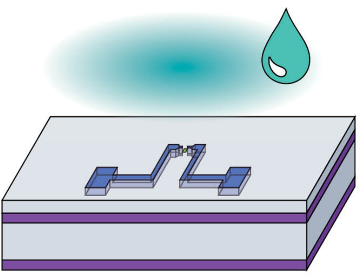
3a) Brewer spinner and hotplate:
i. Dehydrate substrate on a hot plate for 5 min @ 180 ºC.
ii. Cool down for 2 min.
iii. Coat with 5 drops of "950k PMMA A2" resist.
iv. Spincoat for 5 s @ 500 RPM, then increase to 40 s @ 4000 RPM.
v. Softbake for 90 s @ 180 ºC.

vi. EBL (10kV, 15um aperture) patterning: The pattern leaves an open square in the center where Sb dopants would be implanted.

vii. Develop in "MIBK:IPA 1:3" developer for 45 s, followed by IPA for 15 s.



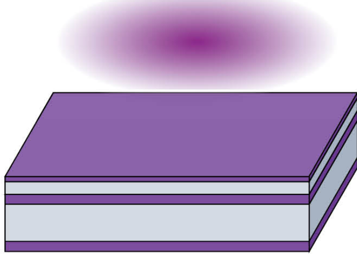
3b) Ion implantation of 100 keV 75As+ ions with a dose of $3.00 \cdot 10^{14}$ ions · cm^{-2}. Outsourced to CuttingEdge Ions.



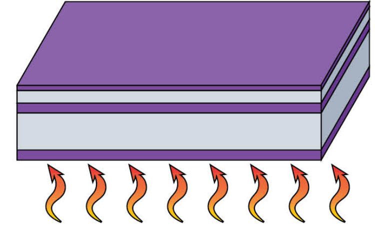
3c) Strip carbonized resist:
i. Run RIE recipe "Clean" on the empty chamber for 15 min.
ii. Run RIE recipe "Descum/Strip" for 30 min.
iii. Soak in "Remover PG" for 5 min.

Figure A.6 – Lithography step # 3: Schematic illustration of the nanofabrication processes for implanting smaller electron-beam lithography (EBL) patterned heavily doped arsenic (As) contacts between the 2 - 4 µm gap in the center of the previously implanted As conduction lines.

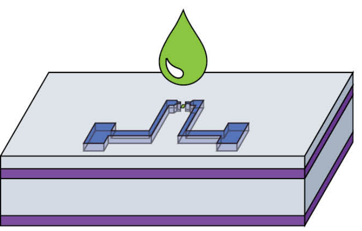
Lithography Step #2: Arsenic Center Contacts (Continued)



3d) PECVD to grow SiO_2 diffusion barrier to prevent dopants from escaping during annealing.
i. For better uniformity, deposit a 1 µm oxide film in the chamber by “oxide conditioning” for 500 s.
ii. Deposit 500 nm of “new oxide” on the device side by processing for 350 s.
iii. “Clean” the chamber for 1700 s.



3e) RTA:
90 s @ 900 ºC in a gas atmosphere of Ar.



3f) Oxide removal:
BOE 10:1 (NH_4F + HF) etches at 51-58 nm/min, therefore, a chemical bath of ~15 min is required to etch the 500 nm oxide.

Figure A.6 – (Continued)Lithography step # 3: Schematic illustration of the nanofabrication processes for implanting smaller electron-beam lithography (EBL) patterned heavily doped arsenic (As) contacts between the 2 - 4 µm gap in the center of the previously implanted As conduction lines.

Electron-Beam Lithography CAD Pattern #4: Embedded Antimony Reservoir

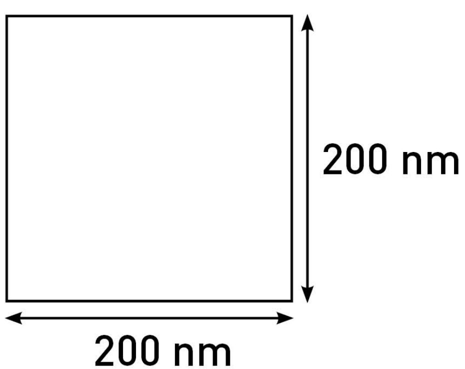
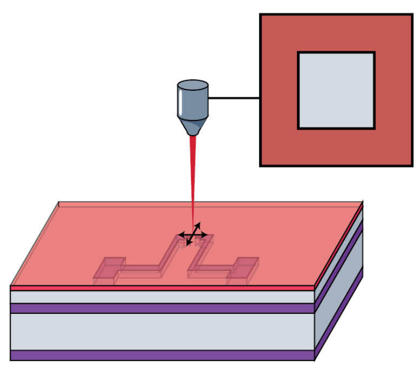


Figure A.7 – CAD drawing for the electron-beam lithography (EBL) design used in patterning an embedded antimony (Sb) reservoir between the 300 nm gap of the previously EBL patterned contacts for lithography step # 4.

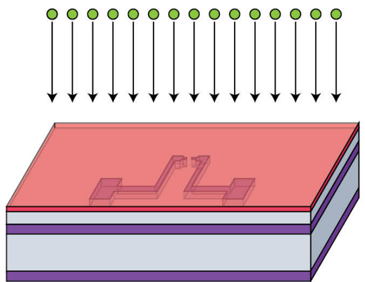
Lithography Step #4: Embedded Antimony Reservoir



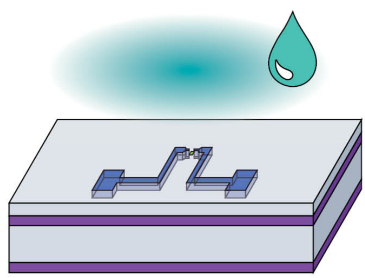
3a) Brewer spinner and hotplate:
i. Dehydrate substrate on a hot plate for 5 min @ 180 °C.
ii. Cool down for 2 min.
iii. Coat with 5 drops of “950k PMMA A2” resist.
iv. Spincoat for 5 s @ 500 RPM, then increase to 40 s @ 4000 RPM.
v. Softbake for 90 s @ 180 °C.

vi. EBL (10kV, 15um aperture) patterning: The pattern leaves an open square in the center where Sb dopants would be implanted.

vii. Develop in “MIBK:IPA 1:3” developer for 45 s, followed by IPA for 15 s.



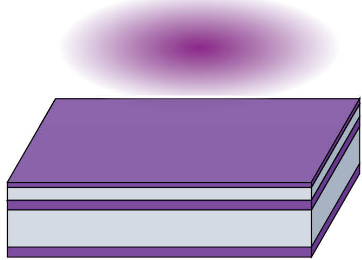
3b) Ion implantation of 100 keV 121Sb+ ions with a dose of $1.8{\cdot}10^{14}$ ions · cm^{-2}. Outsourced to CuttingEdge Ions.



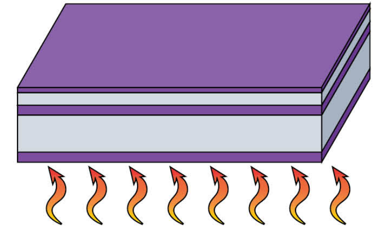
3c) Strip carbonized photoresist:
i. Run RIE recipe “Clean” on empty chamber for 15 min.
ii. Run RIE recipe “Descum/Strip” for 30 min.
iii. Soak in “Remover PG” for 5 min.

Figure A.8 – Lithography step # 4: Schematic illustration of the nanofabrication processes for implanting a heavily-doped embedded antimony (Sb) reservoir between the 300 nm gap in the center of the previously implanted arsenic (As) contacts. The Sb reservoir is implanted with the dopant profile peak ~45 nm under the surface.

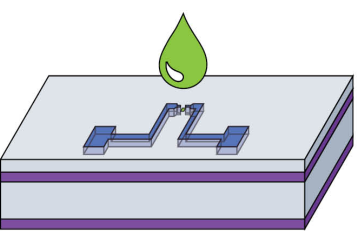
Lithography Step #4: Embedded Antimony Reservoir (Continued)



3d) PECVD to grow SiO_2 diffusion barrier to prevent dopants from escaping during annealing.
i. For better uniformity, deposit a 1 µm oxide film in the chamber by "oxide conditioning" for 500 s.
ii. Deposit 500 nm of "new oxide" on the device side by processing for 350 s.
iii. "Clean" the chamber for 1700 s.



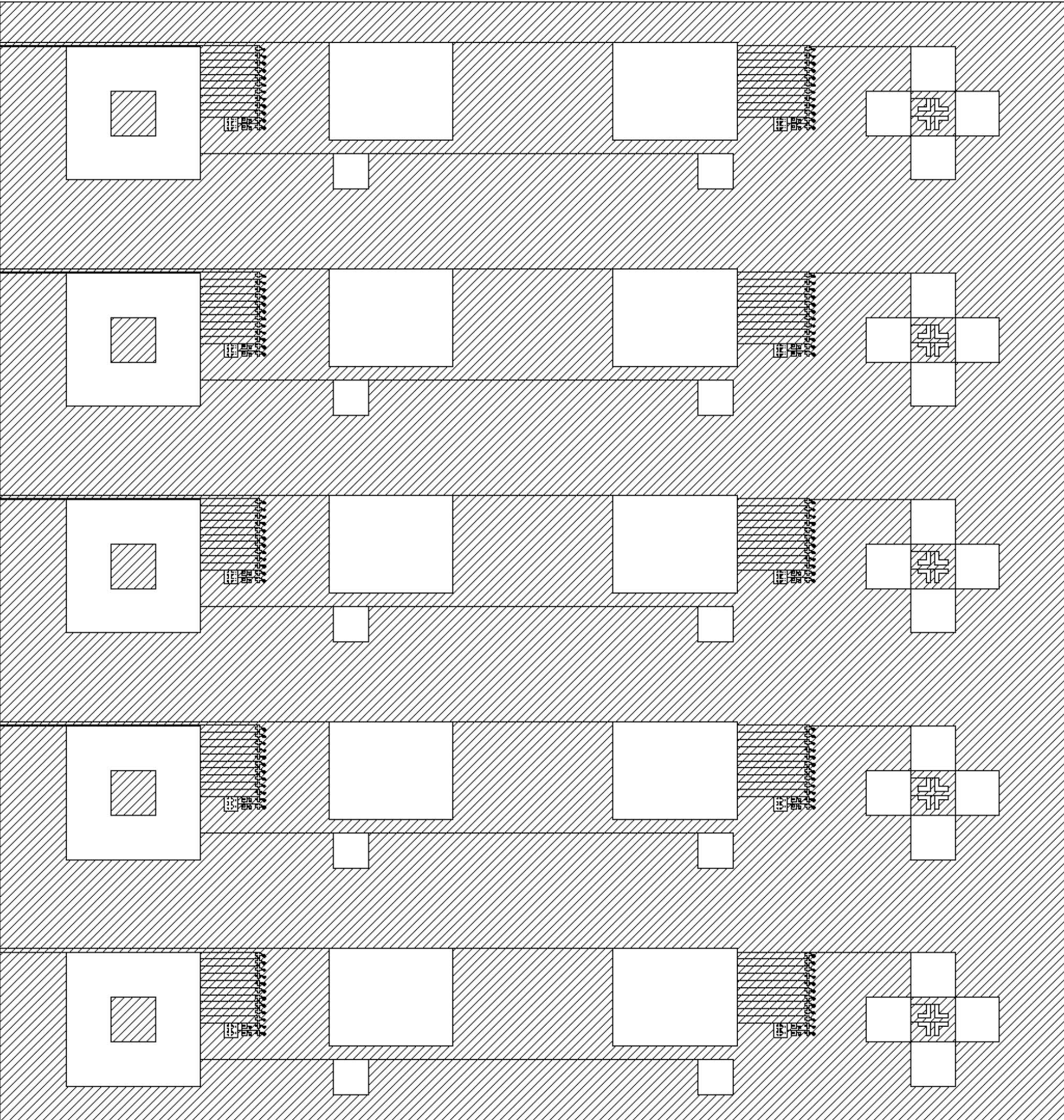
3e) RTA:
90s @ 900ºC in a gas atmosphere of Ar.



3f) Oxide removal:
BOE 10:1 (NH_4F + HF) etches at 51-58 nm/min, therefore, a chemical bath of ~15 min is required to etch the 500 nm oxide.

Figure A.8 – (Continued) Lithography step # 4: Schematic illustration of the nanofabrication processes for implanting a heavily-doped embedded antimony (Sb) reservoir between the 300 nm gap in the center of the previously implanted arsenic (As) contacts. The Sb reservoir is implanted with the dopant profile peak ~45 nm under the surface.

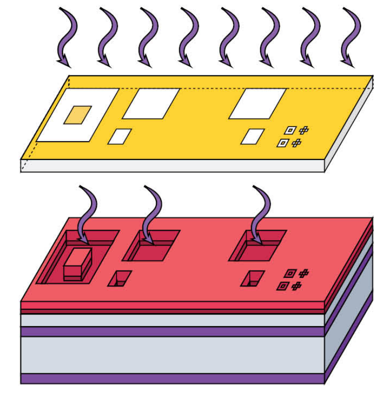
Photomask #5: Platinum Power & Signal Contacts



1 mm

Figure A.9 – CAD drawing for the photomask used in depositing platinum (Pt) power and signal contacts onto a sample block in lithography step # 5. Five devices fit inside one sample block.

Lithography Step #5: Platinum Power & Signal Contacts

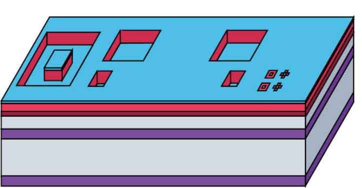


5a) 18. Bi-layer Lithography:
i. HMDS bake and prime.

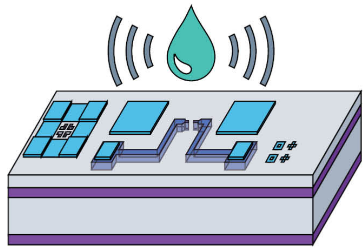
ii. Apply 5 drops of "LOR5B" on device.
iii. Spincoat wafer for 10 s @ 500 RPM, then increase to 40 s @ 3000 RPM.
iv. Softbake for 5 min @ 150 ºC.

v. Apply 5 drops of "AZ1512" resist on the device.
vi. Spincoat wafer for 10 s @ 500 RPM, then increase to 40 s @ 5000 RPM.
vii. Softbake for 1 min @ 100 ºC.

viii. Expose to MASK #3 for 2.8 s.
ix. Develop "AZ1512" resist in "AZ400k 1:4" developer for 45 s.
x. Bake for 120 s @ 115 ºC.
xi. Develop "LOR5B" in "MF319" developer for 15 s.



5b) Sputtering of Ti, Pt:
i. Pump down chamber to ~10^{-6} Torr.
ii. Activate Ar gas @ 50 sccm.
iii. Sputter at 7 mTorr.
iv. AC sputter @ 100 W for 30 s to clean substrate.
v. DC sputter Ti @ 300 W for 1 min to ramp up target, then sputter for 1 min for a 15 nm layer of Ti to be used as an adhesive between the Si substrate and Pt pads.
vi. DC sputter Pt @ 75 W for 1 min to ramp up target, then sputter for 20 min for a 315 nm layer.



5c) Liftoff:
Sonicate in Remover PG for ~50 min.

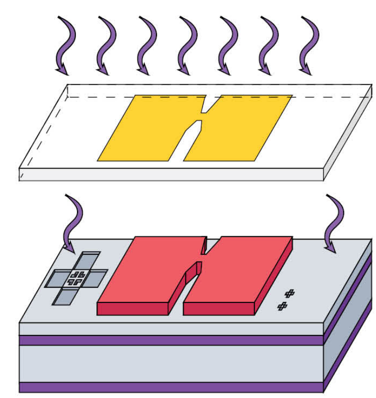
Figure A.10 – Lithography step # 5: Schematic illustration of the nanofabrication processes for depositing platinum (Pt) power and signal contacts.

Photomask #6: Etched Silicon Mesa

1 mm

Figure A.11 – CAD drawing for the photomask used in etching the silicon (Si) mesa onto a sample block in lithography step # 6. Five devices fit inside one sample block.

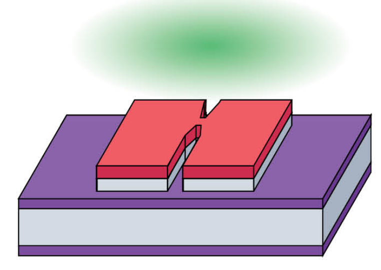
Lithography Step #6: Silicon Mesa



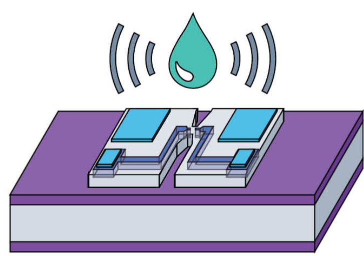
6a) Lithography:
i. HMDS bake and prime.

ii. Apply 5 mL of “AZ1512” resist at the center of the wafer.
iii. Spincoat wafer for 10 s @ 500 RPM, then increase to 40 s @ 5000 RPM.
iv. Softbake for 1 min @ 100 °C.
v. Expose to MASK #2 for 2.8 s.

vi. Develop in “AZ400k 1:4” developer for 45 s.



6b) DRIE:
Using recipe: “ECE 457”:
i. Condition for 50 cycles on a blank wafer.
ii. Process on substrate for 150 cycles to etch out Si mesas, where the BOX layer acts as an etch stop.



6c) Clean resist:
i. Sonicate in hot water for 5 min.
ii. Sonicate in Remover PG for ~25 min.

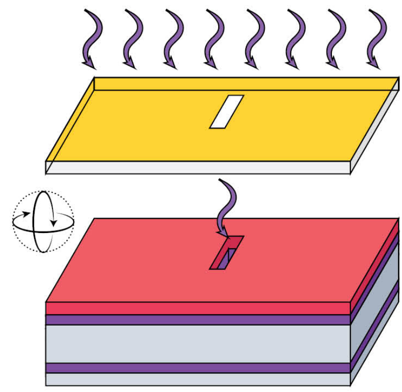
Figure A.12 – Lithography step # 6: Schematic illustration of the nanofabrication processes for etching the silicon (Si) mesa.

Photomask #7: Thermally Isolated Silicon Bridge

1 mm

Figure A.13 – CAD drawing for the photomask used in etching out a hole for the thermally isolated silicon (Si) bridge on a sample block in lithography step # 7. Five devices fit inside one sample block.

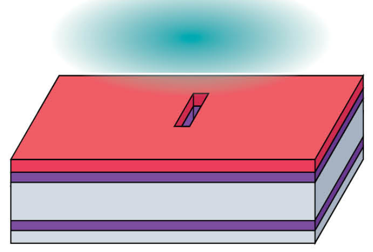
Lithography Step #7: Thermally Isolated Silicon Bridge



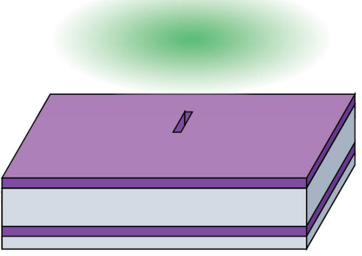
7a) Lithography:
i. HMDS bake and prime.

ii. Apply 5 mL of “AZ1512” resist at the center of the wafer.
iii. Spincoat wafer for 10 s @ 500 RPM, then increase to 40 s @ 5000 RPM.
iv. Softbake for 1 min @ 100 °C.
v. Expose to MASK #2 for 2.8 s.

vi. Develop in “AZ400k 1:4” developer for 45 s.



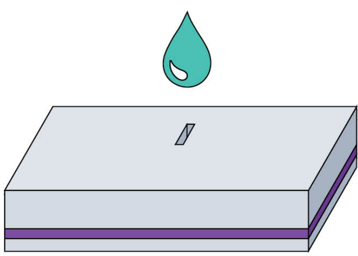
7b) RIE:
i. Run “Clean” on an empty chamber for 10 min.
ii. Process substrate with “SiO_2 Etched Martins” for 2 cycles of 10 min (20 min total) to etch the back handle oxide to be used as an etch mask for the following Bosch etch.



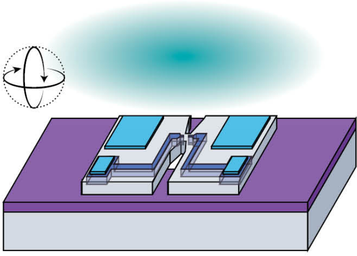
7c) DRIE:
Using recipe: “Bosch High Rate Stage 1 150mm”:
i. Condition for 50 cycles on a blank wafer.
ii. Process with 150 + 150 + 100 cycles (400 total cycles), or until hole is etched through. The process etches at a rate of 0.24 μm/min, with a 300:1 selectivity of $Si:SiO_2$.

Figure A.14 – Lithography step # 7: Schematic illustration of the nanofabrication processes for etching out a hole for the thermally isolated silicon (Si) bridge. Processes take place on the handle (back) layer of the sample block to etch out the handle and oxide layers of the device.

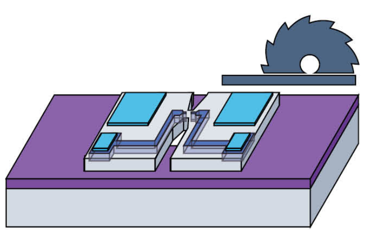
Lithography Step #7: Thermally Isolated Silicon Bridge (Continued)



7d) Clean resist residue and crystal bond:
i. Clean with boiling water for ~5 min.
ii. Clean with "remover PG" @ 70 ºC for ~5 min. Sonication is not used, as the Si bridge is too fragile.



7e) RIE for oxygen cleaning:
i. Run "Clean" on an empty chamber for 12 min.
ii. Process on substrate with "O_2 Descum" for 2 min to clean any remaining residue off the device side.



7f) Dicing blocks:
Using the DISCO DAD 321 with the following settings: Ch1: 2.55 mm, Speed: 2 mm/s to dice blocks into 5 individual devices to fit inside the STM sample holders.

Figure A.14 – (Continued) Lithography step # 7: Schematic illustration of the nanofabrication processes for etching out a hole for the thermally isolated silicon (Si) bridge. Processes take place on the handle (back) layer of the sample block to etch out the handle and oxide layers of the device.