On Faster-Than-Real-Time Dynamic Simulation of AC-DC Grids

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Energy Systems

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Abstract

The proportion of renewable energy versus conventional generation has been increasing significantly worldwide due to enhanced environmental standards, bringing with it a host of technical and operational challenges. Restrictions on available transfer capacities leading to severe congestion of major transmission and distribution corridors have been the most common problem, with severe consequences related to voltage and frequency regulation, and transient stability and reliability of the grid. Building new transmission facilities is the only viable long-term solution to assuage the impacts of renewable energy penetration, and increasingly electric utilities are opting to construct new direct current (DC) transmission lines. With modular multi-level converter (MMC) technology as the foundation, multi-terminal DC grids have enabled the transfer of large amounts of power, and interconnection of asynchronous alternating current (AC) systems. In this scenario, real-time dynamic simulation of integrated AC-DC networks is indispensable for maintaining system stability and resiliency. Currently, available dynamic simulation tools adopt sequential compute hardware and therefore turn out to be time-consuming. On the other hand, field-programmable gate arrays (FPGAs) with large hardware resource capacity allow parallel processing of various components. As a result, they shorten the process of finding the whole network solution by optimizing the hardware latency, which is why they are the ideal platform to attain faster-than-real-time (FTRT) execution. In this thesis, practical modeling techniques, numerical solution strategies, and hardware implementation schemes are proposed for FTRT dynamic emulation of integrated AC-DC grids on FPGAs.

The FPGA-based hardware emulation platform is suitable for the energy control center for dynamic security assessment (DSA), which is necessary for analyzing the ability of a power system to withstand cascading failures or contingencies in a specified time span to ensure that the power grid is at a secure operating point. The proposed FTRT dynamic emulation can enable the prediction of system state following severe disturbance and provides recommendations for taking preventive and remedial actions. The increasing scale

of a power system also demands that more contingency scenarios be taken into consideration during DSA. The FPGA-based DSA platform is able to provide fast and accurate contingency screening data for a large-scale AC/DC grid in FTRT mode. The reconfigurability and the sufficient hardware resources allow the entire grid to be deployed on the platform after proper system partitioning and allocation.

In the meantime, widely adopted for boosting the transmission capacity of a line, capacitive series compensation induces the potential risk of subsynchronous resonance (SSR) which is one of the most severe security issues that the power system may encounter, which makes its expansion with multi-terminal HVDC transmission system and renewable energy installations leading into a hybrid grid more vulnerable. As a precautionary measure, the FTRT simulation is able to mitigate the SSR once it happens following the occurrence of a serious contingency like a three-phase fault or a sudden load change. It has the ability of reproducing the phenomenon and then learning in advance the system's responses under various scenarios to find a proper strategy. The proposed FTRT simulation in the energy control center can predict how much active power should be injected into or extracted from the AC grid by regulating the HVDC grid, as well as how long should the process last before real actions take place in the actual system.

In the last few decades, dynamic equivalents were put forward to deal with the challenge of modeling large-scale systems for transient stability (TS) simulation. Meanwhile, artificial intelligence (AI) has caught a lot of attention in current industry practice. A practical method for power control center with the machine learning based synchronous generator model (SGM) and dynamic equivalent model (DEM) is proposed to reduce the computational burden of the traditional TS simulation. Hardware emulation is also investigated to accelerate the proposed machine learning based models deployed on the FPGAs for FTRT execution.

Preface

The contents of this thesis are based on original work by Shiqi Cao. As detailed below, material from some chapters of the thesis has been published as journal articles under the supervision of Dr. Venkata Dinavahi in concept formation, writing the manuscript text, and by providing comments and corrections to the article manuscript.

Chapter 2 includes the results published in the following papers:

- S. Cao, N. Lin, and V. Dinavahi, "Faster-than-real-time dynamic simulation of AC/DC grids on reconfigurable hardware", *IEEE Transactions on Power Systems*, vol. 35, no. 2, pp. 1539-1548, Mar. 2020.

- S. Cao, N. Lin, and V. Dinavahi, "Flexible time-stepping dynamic emulation of AC/DC grid for faster-than-SCADA applications", *IEEE Transactions on Power Systems*, vol. 36, no. 3, pp. 2674-2683, May 2021.

Chapter 3 contains contents from the following papers:

- S. Cao, N. Lin, and V. Dinavahi, "Mitigation of subsynchronous interactions in hybrid AC/DC grid with renewable energy using faster-than-real-time dynamic simulation", *IEEE Transactions on Power Systems*, vol. 36, no. 1, pp. 670-679, Jan. 2021.

- S. Cao, N. Lin, and V. Dinavahi, "Damping of subsynchronous control interactions in large-scale PV installations through faster-than-real-time dynamic emulation", *IEEE Access*, vol. 9, pp. 128481-128493, Sept. 2021.

The contents from the following paper is included in Chapter 4:

- S. Cao, N. Lin, and V. Dinavahi, "Faster-than-real-time hardware emulation of extensive contingencies for dynamic security analysis of large-scale integrated AC/DC grid", *IEEE Transactions on Power Systems*, accepted, pp. 1-11, DOI: 10.1109/TPWRS.2022.3161561.

The materials presented in Chapter 5 have been submitted:

- S. Cao, N. Lin, and V. Dinavahi, "Faster-than-real-time hardware emulation of dynamics of a grid of microgrids", *under review, IEEE Open Access Journal of Power and Energy.*, pp. 1-10, 2022 (No. OAJPE-00063-2022).

Chapter 6 is based on the following paper that is currently under peer review:

- S. Cao, V. Dinavahi, and N. Lin, "Machine learning based transient stability emulation and dynamic system equivalencing of large-scale AC-DC grid for FTRT digital twin", *under review, IEEE Transactions on Power Systems*, pp.1-10, 2022 (No. TPWRS-00592-2022).

To my parents for your unconditional love,
especially to my mother who always supported me.

Acknowledgements

I would like to express my genuine gratitude to my supervisor *Dr. Venkata Dinavahi* for his support, encouragement, and inspiring guidance through my study at the University of Alberta. His passion, patience, and positive attitude towards research is a tremendous impetus to me.

In the meantime, I wish to deliver thanks to members of the RTX-Lab, particularly *Dr. Ning Lin*, who helped me a lot at the beginning of my research. Many thanks to my friends and colleagues, especially *Songyang Zhang* for providing me with the latest industrial information, and the support whenever I needed it.

I want to express my sincere appreciation for the greatest support and understanding from my family: my father, *Lixin Cao*, and my mother, *Jing Shi*. During my studies at the University of Alberta, even though my mother faced health challenges, she still gave me a lot of psychological help and emotional support which made me feel warm all the time.

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List of Acronyms

AC	Alternating Current
AI	Artificial Intelligence
ANN	Artificial Neural Network
ASM	Angle-Based Stability Margin
AVM	Averaged Value Model
AVR	Automatic Voltage Regulator
BESS	Battery Energy Storage System
CCT	Critical Clearing Time
CNN	Convolutional Neural Network
CPU	Central Processing Unit
CRNN	Convolutional Recurrent Neural Network
CUDA	Compute Unified Device Architecture
DAC	Digital Analog Converter
DAE	Differential Algebraic Equations
DC	Direct Current
DEM	Dynamic Equivalent Model
DFIG	Doubly-Fed Induction Machine
DLQR	Discrete Linear Quadratic Regulator
DSA	Dynamic Security Assessment
EMT	Electromagnetic Transient
ESS	Energy Storage System
FACTS	Flexible AC Transmission Systems
FBM	First Benchmark Model
FF	Flip-Flop
FFT	Fast Fourier Transform
FGRA	Fine-Grained Relaxation Algorithm
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
FTRT	Faster-Than-Real-Time
FTS	Flexible Time-Stepping
GCSC	Gate-Controlled Series Capacitor
GPU	Graphics Processing Unit
GRU	Gated Recurrent Unit
GS	Gauss-Seidel
HIL	Hardware-in-the-loop
HLS	High-Level Synthesis
HVDC	High-voltage Direct Current

IGBT	Insulated-Gate Bipolar Transistor
IGE	Induction Generator Effect
JTAG	Joint Test Action Group
LCS	Load Commutation Switch
LSTM	Long Short-Term Memory
LTE	Local Error Truncation
LUT	Look-Up Table
MG	Microgrid
MIMO	Multi-Input-Multi-Output
ML	Machine Learning
MMC	Modular Multi-level Converter
MOV	Metal-Oxide Varistor
MTDC	Multi-terminal DC
NERC	North American Electric Reliability Corporation
NLP	Natural Language Processing
NR	Newton-Raphson
OWF	Offshore Wind Farm
PCC	Point of Common Coupling
PMU	Phasor Measurement Unit
PSS	Power System Stabilizer
PV	Photovoltaic
QSFP	Quad Small Form-factor Pluggable
RK	Rung Kutta
RNN	Recurrent Neural Network
RT	Real-Time
SCADA	Supervisory Control and Data Acquisition
SCR	Short Circuit Ratio
SGM	Synchronous Generator Model
SIMD	Single-Instruction-Multiple-Data
SM	Submodule
SSCI	Subsynchronous Control Interaction
SSI	Subsynchronous Interaction
SSR	Subsynchronous Resonance
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TI	Torsional Interaction
TLM	Transmission Line Modeling
TS	Transient Stability
TSSM	Two-State Switch Model
UART	Universal Asynchronous Receiver Transmitter
UPFC	Unified Power Flow Controller
VDHN	Very Dishonest Newton
VHDL	Very-high-speed-integrated-circuit Hardware Description Language
VSC	Voltage Source Converter
VTS	Variable Time-Stepping

1 Introduction

Transient stability (TS) simulation of integrated AC and DC grids is paramount to address real-time operation challenges in energy control centers, such as available transfer capacities, relieving grid congestion, and taking effective control actions for improving the integrated grid system stability and security. Conventionally, transient stability simulation of AC systems involves the time-domain solution of a set of nonlinear differential algebraic equations (DAEs). The differential equations correspond to the synchronous machine models, and the algebraic equations correspond to the network. For dynamic security assessment (DSA) these simulations are run for a set of critical contingencies [1–3]. The differential equations may be discretized by either explicit and implicit numerical integration methods, resulting respectively in a separate (iterated) or simultaneous solution of the machine and network equation sets. The iterative schemes commonly employed are the Gauss-Seidel (GS), the Newton-Raphson (NR), or the Very Dishonest Newton (VDHN) methods with their corresponding pros and cons influencing the accuracy, convergence rate, and computational burden of the overall simulation [4–6]. For large-scale systems, invariably, the computation is distributed over parallel processors by employing domain decomposition and relaxation schemes in space, time, or both dimensions [7–9]. Hitherto, large-scale transient stability implementations have been carried out on clusters of CPUs and GPUs for efficient simulation or even real-time execution [10–12], and dense or sparse libraries are utilized for matrix equation solution in the simulation.

As the multi-terminal HVDC systems are introduced into the traditional AC systems, transient stability simulation cannot meet the requirements of revealing the dynamic process of converter stations. The electromagnetic transient (EMT) simulation is applied to the DC side. With varying submodule topologies, MMCs offer faster controllability, higher redundancies, and better fault-tolerant capability [13, 14]. Due to the complexity of inte-

grated AC and DC grid, an FTRT dynamic simulation tool is therefore put forward. The proposed FTRT emulation deployed in the energy control center can accelerate planning schedules, assess the impact of excessive energy penetration at critical locations, predict destabilizing outages, devise newer control strategies, and enhance the overall security and reliability of the grid.

Over the last 10 years, there has been tremendous development in reconfigurable hardware logic devices that are FPGAs, in both their VLSI architecture and CAD software tools, that have enabled them to become mainstream processors in many industrial areas. Currently, available Ultrascale+ FPGAs from Xilinx® are 16nm devices with a maximum of 3.8M system and programmable logic cells, up to 12,288 DSP slices, and 32.75 GB/s maximum transceiver speed. These features are expected to grow even more in the future. For power systems and power electronic systems, FPGAs have been used in real-time hardware-in-the-loop (HIL) application for detailed device-level modeling of various equipment [15, 16].

Based on the above observations, this research is aiming to conduct fast and parallel dynamic simulation for hybrid AC-DC grid to accelerate the simulation process by proposing new computational methods and implementation architectures:

- At the computational level: a fine-grained relaxation algorithm (FGRA) and flexible time-stepping (FTS) method are proposed for calculating the non-linear DAEs in the TS simulation. Meanwhile, with the development of artificial intelligence (AI) technologies, the machine learning based synchronous generator model and dynamic equivalent model (DEM) are proposed to reduce the computational burden of the traditional TS simulation.

- At the hardware implementation level: the FPGA boards which have abundant hardware resources are applied in conducting TS-EMT co-simulation, and its parallelism and reconfigurability features indicate that it is suitable for simulating a large power system at high speed.

With an achievable high speedup ratio over real-time, the FPGA-based FTRT emulation could enable the energy control center to have sufficient time to predict the future states, improve dynamic response analysis speed, yield an optimal solution to mitigating the subsynchronous oscillations, as well as provide a large number of contingencies screening results for DSA.

1.1 Literature Review

In this section, a review of previous studies related to this research are conducted.

1.1.1 Transient Stability Problem

A practical power transmission system includes synchronous generators, buses, transmission lines, as well as various loads. The differential equation (1.1) describes the dynamic process of the synchronous machines and will be explained in detail in the following section. And the remaining components contribute to the algebraic equations which solve the network in conjunction with stator voltages of the generators.

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{u}, \mathbf{t}), \tag{1.1}$$

$$\mathbf{g}(\mathbf{x}, \mathbf{u}, t) = 0, \tag{1.2}$$

where **x** refers to the vector of state variables, and **u** represents the bus voltages of a typical power system. The initial conditions can be written as:

$$\mathbf{x}_0 = \mathbf{x}(t_0), \tag{1.3}$$

The researchers are dedicated to speeding up the transient stability simulation and reducing the computational burden, which benefits the dynamic security assessment in the energy control center. Currently, the methodologies of solving the transient stability problem can be classified into two categories: 1) Developing new parallel numerical integration algorithms, 2) Utilizing high-performance processors. Notice that the main challenge of emulating a power transmission system is basically solving a series of differential algebraic equations (DAEs). The traditional proceeding of solving the differential equation is given as follows [11]:

1) Discretization: The continuous differential equation should be discretized prior to its solution, e.g., the corresponding time-discrete nonlinear algebraic equation can be obtained after applying the Trapezoidal rule:

$$\mathbf{F}(\mathbf{z}) = \frac{\Delta t}{2}[\mathbf{f}(\mathbf{x}, \mathbf{u}, t) + \mathbf{f}(\mathbf{x}, \mathbf{u}, t + \Delta t)] - [\mathbf{x}(t + \Delta t) - \mathbf{x}(t)], \tag{1.4}$$

where $\mathbf{z} = [\mathbf{x}, \mathbf{u}]$, and Δt is the simulation time-step.

2) Nonlinear Algebraic Equation Formation: The N-R iteration method is applied to the aforementioned nonlinear algebraic equation and consequently leads to

$$\mathbf{J}(\mathbf{z}_i) \cdot \Delta\mathbf{z} = -\mathbf{F}(\mathbf{z}_i), \tag{1.5}$$

where the subscription i is the iteration time, **J** refers to the Jacobian matrix whose elements are obtained by the partial derivative of the 9th-order state variable functions, and $\Delta\mathbf{z} = \mathbf{z}_{i+1} - \mathbf{z}_i$.

3) Linear Algebraic Equation Solution: The formation of (1.5) allows deriving the state variables using traditional linear equation solvers such as Gaussian Elimination and LU decomposition. The simulation speed is deeply affected by the type of solver employed, especially considering the scale of power system always results in a huge matrix equation which often causes a heavy computational burden.

4) Update of Jacobian Matrix: Following the solution, the Jacobian matrix which is changing in every iteration can be updated for the preparation of next iteration or – if the results are convergent – the next time-step.

Meanwhile, some improved integration methods are proposed, such as relaxation methods, and parallel in time methods [4, 17]. The principle of these methods is calculating several time-steps simultaneously to shrink the simulation time, which will sacrifice accuracy for higher efficiency. Furthermore, most of the commercial dynamic simulation tools commit to reducing power consumption rather than optimizing hardware platforms. With the significant progress being made in parallel processing, utilizing the high-performance hardware comes to be another direction of speeding up transient stability analysis. The improvement includes applying supercomputers [18], multiprocessors [19], and GPUs [10, 11]. Although these hardware-based platforms help to accelerate the operation speed, they still have their drawbacks. For instance, the cost of a supercomputer, the communication issues of multiprocessors, as well as the difficulties in programming on GPUs are the main factors that limit their widespread application.

1.1.2 Dynamic Security Assessment

Modern power systems are increasingly complex due to the interconnection between high voltage direct current (HVDC) and renewable energy, which makes the simulating, analyzing, and controlling the network difficult. Dynamic security assessment (DSA) is applied in power systems to ensure their stability and security. A complete DSA is composed of five stages [20]: measurements, modeling, computing, visualization, and control. The real-time measurements are captured by the supervisory control and data acquisition (SCADA) for basic state estimation, and then a detailed time-domain simulation is carried out for imminent contingencies. The obtained security indices are delivered to the system operators in the energy control center. The entire DSA cycle is conducted within 10-30 minutes to ensure that the operators have sufficient time to take remedial actions.

Due to the enormous computational burden in DSA systems and the expansion of power system scale, the hardware resources are stretched. For instance, to realize near real-time simulation of a power transmission system with more than 50,000 nodes and 3000 generators, the DSA is conducted on the supercomputer with more than 24,000 CPU cores for power system parallel simulation [18], which occupies a lot of hardware resources. On the other hand, the SCADA system collects data from the field every 2-5s [21], this may be sufficient for steady-state tasks such as online power flow or state estimation, how-

ever, it falls short of predicting system stability and conducting online dynamic security assessment. The phasor measurement unit (PMU) technology provides a faster refresh rate (50/60 samples per second [21]) which is at least two orders of magnitude faster than SCADA, however, PMUs are expensive and cannot be installed on a wide-area to gather system dynamic situational awareness. Moreover, even if PMUs were widely deployed, communication delays to the energy control center would still exist.

In a real power system, the distributed and multi-input-multi-output (MIMO) wide-area damping controllers are also applied to mitigate the inter-area oscillations and reduce the computational burden. The MIMO controller of the power system can be estimated directly without the need for having a detailed model of the power system. Once the changing dynamics/operating points of the system are captured in the measured data, the MIMO model can be used for mode and control loop estimation. However, the MIMO identification of the power system, estimation of the control loops, and the design of the discrete linear quadratic regulator (DLQR) are done every 4s [22], and due to the slow rate of state estimation, MIMO identification is insufficient for real-time or faster-than-real-time estimation. The PMU based wide-area control of static synchronous compensator [23], on the other hand, has main restrictions such as the communication time-delay and the synchronization issues of wide-area controllers, which make them unsuitable for the FTRT emulation.

1.1.3 Variable Time-Stepping Methods

To provide fast, accurate, and time-synchronized data for the complex AC-DC grids, a high-fidelity simulation strategy is also needed. Traditional off-line dynamic simulation tools such as PSS®/E, and DSATools™/TSAT® apply fixed time-steps, and so do all commercial real-time simulators, which, as noticed, will require more hardware resources and prolong the simulation when the system scale becomes larger. A complex matrix solution is inevitable during the transient stability simulation and the admittance matrix will increase along with the system scale. Although the real-time simulation can be reached with the help of the high-performance processors [2,12,19,24] and the parallel algorithms [9,25,26], the execution time will increase along with the dimension of the admittance matrix. Some improved numerical methods are thereby put forward for accelerating the simulation, such as parallel-in-time [10,17,27], and parallel-in-space methods [8,28,29]. Although these methods help to accelerate the operation speed, the excessive iteration requirement of the parallel-in-time algorithm, as well as the difficulties in the programming of the parallel-in-space algorithm limit their widespread application.

It is noticed that fixed time-stepping is not always mandatory for the large-scale AC-DC grids as the various equipment have different dynamic responses to time-step. The variable time-steps (VTS) algorithms are also proposed for speeding up time-domain simulations [30–33]. Using various criteria such as local truncation error (LTE), or event-

correlated criterion [30], the VTS scheme was successfully applied on a few occasions where the system is relatively simple, but its application to a larger and more complex nonlinear system such as the hybrid AC-DC grid has yet to be explored.

1.1.4 Subsynchrnous Interactions

Subsynchrnous interaction (SSI) is largely defined as the interaction between the series compensator and turbine generator, which has 3 major categories [35], i.e., the induction generator effect (IGE), the torsional interaction (TI), and the torsional amplification (TA) which generally refers to the immediate oscillations in the shaft torque following large disturbances, such as faults or switching operations. This phenomenon could linger for a long period of time in a series-compensated system, and it may cause disconnection of the generators and damages to the shaft [35,36]. Therefore, TA mitigation becomes imperative once it appears to avoid a deeper negative impact on the AC-DC grid.

A detailed multi-mass turbine-shaft-generator model compulsory to produce the torsional amplification is developed for transient stability analysis in the dynamic simulation. In a typical power transmission system which includes series compensation on transmission lines, torsional interactions among each turbine shaft may arise when system faults and sudden load changes occur. Following a disturbance, the transient power oscillation may emerge. If the resonance frequency corresponds to one of the torsional oscillation frequencies, the electrical power may interact with the T-G shaft, resulting in subsynchronous resonance [37].

1.1.5 Subsynchronous Control Interaction

In a grid with massive inverter-based renewable generations, subsynchronous resonance (SSR) due to subsynchronous control interaction (SSCI) has become increasingly common [38]. As a phenomenon of resonance between a power electronic device and neighboring series compensated transmission lines [39], the SSCI is distinct from torsional interaction which involves the mechanical system of a synchronous generator [40], and therefore, it may grow more rapidly and subsequently present a severe threat to the security and reliability of the overall power system.

First seen in a doubly-fed induction generator (DFIG) based wind farm in Texas in 2009 [39], tremendous efforts have since been endeavored in mitigating the SSCI in wind farms [41–43]. However, the inverter-based photovoltaic (PV) station is not exempted from the same phenomenon and needs investigation. The power generated by large-scale PV farms has to be transmitted over a long distance since the plants are usually far away from load centers. Therefore, the PV source in conjunction with the transmission links constitutes a weak grid that faces many stability issues, including the SSCI [44–48]. Considering that in an interactive network, the oscillations between a PV converter and the line will

soon spread to the AC grid, analysis and mitigation of the PV oscillation become crucial in the transient stability analysis.

Among prevalent SSR analysis methods, frequency scanning is an approximate linear method that calculates the equivalent impedance of the whole system seen from the rotor at a specific frequency [49]. Its main drawback is relatively low accuracy, albeit little calculation effort is required. Time-domain simulation and eigenvalue analysis are more suitable for analyzing the SSCI in PV farms [37]. The former method takes the linear and nonlinear characteristics of the system into account, and it provides a variety of time-varying curves that reflect a real SSCI scenario under the circumstance of accurate modeling.

Traditional SSR mitigation strategies can be classified as: 1) Bypass the oscillation region [50]; 2) Utilize flexible AC transmission systems (FACTS) devices, such as static var compensator (SVC) [51,52], static synchronous compensator (STATCOM) [53,54], unified power flow controller (UPFC) [55], and gate-controlled series capacitor (GCSC) [56]. Since bypass or cutting off the abnormal components may influence the overall stability of the integrated network, the utilization of FACTS devices plays a crucial role in mitigating SSR on the thermal turbine generator connected to the series compensated power systems. The working principle of the FACTS devices is to alert the series compensated factor by the reactive power change. However, the complex control strategies and costs of FACTS devices are the main restrictions of their wide spread deployment.

1.1.6 Contingency Screening

The increasing scale of a power system demands that more contingency scenarios be taken into consideration during DSA. To mitigate the adverse impacts of a variety of disturbances on the actual power system, online DSA is widely utilized to continuously monitor the grid and take remedial actions [20,57]. The contingency screening type is a major factor that influences the speed of DSA. A typical contingency analysis applies the power flow calculation or state estimation, which only provides a single-state security index for contingency ranking [57,58]. Due to the relatively low computational burden, the power-flow based contingency analysis methods are widely utilized in high-speed DSA [2,59,60]. However, more stringent criteria have been proposed by the North American Electric Reliability Corporation (NERC) [61], which brings many challenges to conducting fast contingency analysis. Since it is computational onerous to evaluate all the contingencies at a time, a subset is usually selected for analysis in traditional contingency screening methods such as the performance index contingency ranking [62]. However, when a larger subset is required for the contingency analysis of a large-scale grid, it is difficult to achieve real-time execution. Meanwhile, the power-flow based contingency ranking methods fall short of provision of subsequent dynamic processes after a disturbance, and are hence excluded for predictive control in an energy control center. The TS simulation is therefore adopted for DSA purpose. It enables the representation of the dynamic characteristics of all power

system components in time-domain, which is a direct and precise method attributing to the utilization of detailed dynamic models [36, 63, 64].

The processing hardware is another aspect that limits the performance of contingency screening, which nowadays is usually supported by high-performance CPUs or multiprocessors for efficient simulation or even real-time execution [18, 65, 66]. Although presently CPU-based commercial DSA simulators are prevalent in stability analysis, the massive scale of the target power system, as well as the huge number of contingencies to be analyzed, always poses a significant challenge to the simulation efficiency. The utilization of the multiprocessors or supercomputers is a straightforward solution for real-time DSA due to the sufficient hardware resources and high processing frequency [12]. However, as many as 24,000 CPU cores may be needed to realize a near real-time simulation of a real power grid containing 3,000 generators [18], which is inconvenient and expensive for commercial use. Although parallel algorithms are utilized for accelerating transient stability simulation [8, 10, 17, 25, 26, 29], the execution time will still increase along with the dimension of the admittance matrix [67, 136].

1.1.7 Microgrid Simulation

The penetration of microgrids (MGs) with renewable energy resources has been increasing in the power system to alleviate the energy crisis and environmental issues. The traditional centralized structure of the power systems is not efficient to meet the growing electricity demand due to the power loss in the transmission network [68]. Therefore, modern power systems are experiencing a shift from centralized generation to distributed generation [69, 70]. The distributed generation with multiple MGs integrated may bring new challenges including designing, operating, and coordinating the complex system. Considering that in such an integrated network a small disturbance may spread to other areas and cause severe damage to the whole system, it further increases the complexity of controlling the microgrid cluster.

To deal with the complexity caused by the integration of MGs, a variety of models and control strategies have been developed and investigated in the literature. Most of the existing microgrid technologies focus on one specific aspect, such as energy management [71, 73, 74], control methods [70], [75–77], optimal power flow [78], or protection schemes [79, 80]. Meanwhile, some simulation models for analyzing the microgrids are also investigated, e.g., the detailed and simplified models for the energy storage system (ESS) in MGs are presented in [81–83]. Although significant progress has been made, these research results lack hardware support and the simulation models mentioned above are hard to realize in real-time, which is insufficient for modern energy control center that requires taking remedial actions immediately after a disturbance. Furthermore, it falls short of revealing the impact of multiple MGs on the AC grid with which they are integrated.

While there is still further research needed related to real-time simulation of the MGs,

significant progress has been made in the literature which can be categorized into four aspects: 1) the design and modeling of MG components to achieve real-time simulation [84]- [91]; 2) the utilization of existing commercial real-time simulators [92]- [95]; 3) the development of real-time virtual test bed for MGs [96]- [98]; 4) novel computational approaches for distribution grids [100], [101]. Real-time simulation prefers the models with lower computational burden, and therefore, the relatively simpler models or equivalent dynamic models have been developed. Machine learning (ML) based models have also been investigated to selectively model and simulate MG components [86], [87], which significantly reduced the hardware consumption; however, the ML-based models may ignore some dynamics of the MG components to obtain a higher simulation speed. Thus, these modeling approaches still require further research to meet the requirements of modern power systems for dynamic security assessment. Commercial real-time simulators are usually executed on high-performance processors or supercomputers to realize the high-speed simulation for microgrids [18], which are able to conduct the simulation of MG components in real-time. Although their accuracy and efficiency can be guaranteed due to the high processing frequency, the cost of the computing equipment is the main factor that limits their widespread application. Meanwhile, the hardware-in-the-loop (HIL) simulation is also utilized in modern power systems and has also been applied to investigating microgrids [102], [103]. The hardware resources of the existing simulators restricts the scale of MG or MG clusters. Only a relatively small scale microgrid is tested and neither power dispatch nor interactions among grid components are investigated in the above papers. Virtual testbeds for cyber and physical data acquisition have caught a lot of attention in MG simulation, which can also coordinate with other unconventional modeling methods to realize real-time simulation [98]. Due to their flexibility and scalability, virtual testbeds are convenient to reconfigure and adapt to various systems without depending on specialized hardware; however, they have limited real-time simulation capabilities, especially in applications that require deterministic, low-latency feedback loops for real hardware [98]. The lack of efficient physical interfaces is also another one of their drawbacks. Furthermore, some novel approaches were also proposed for real-time simulation of MGs. Commonly, EMT simulation method is adopted for detailed representation of MG components described by non-linear differential algebraic equations. Parallel solution approaches were therefore put forward to gain a high-speed execution. These methods usually require sufficient hardware resources for parallel processing, and multiple FPGA boards are utilized to realize real-time simulation [101], [104].

1.1.8 Dynamic System Equivalents for Transient Stability Simulation

With the system scale becoming larger, despite the availability of high-performance hardware, the most time-consuming part of TS simulation is still solving the nonlinear DAEs of the synchronous generator. The dynamic equivalencing is therefore proposed to reduce

the execution time, which is achieved by reducing the number of generator and network nodes. Currently, the main approaches to the dynamic equivalencing are largely classified into the following three directions.

- **Coherency Methods**
  For a given perturbation, if a group of generators oscillates with the same angular speed, these generating units are identified as a coherent group, which can be attached to a common bus [105–107]. The aggregation of the generating units consists of replacing a coherent group of machines with an equivalent generator. The approach of dynamic equivalencing involves the following steps [108–110]: 1) identification of the coherent group, 2) aggregation of generator buses, 3) aggregation of the generator models and control devices, 4) reduction of the load buses.

  The coherency-based dynamic equivalents still remain the nonlinear physical characteristics of the generators in an equivalent form, which may have a high accuracy if the equivalent model is properly designed. However, the accuracy of these methods cannot be guaranteed with the number of generators growing up in a coherent group. Furthermore, the coherent methods can significantly reduce the dimension of network equations due to the nodes inside the coherent group have been eliminated.

- **Modal Methods**
  The detailed models of complicated physical systems usually consist of a large number of nonlinear time-varying equations as given in (1.1) and (1.2), which makes analyzing the basic dynamic interactions extremely difficult by using the nonlinear model [111–113]. To reduce the computational burden, a linearized state-space model derived from (1.1) is proposed for analyzing the low frequency oscillations for dynamic simulation, given as:

  $$\dot{\mathbf{X}} = \mathbf{A} \cdot \mathbf{X}(\mathbf{t}) + \mathbf{B} \cdot \mathbf{u}(\mathbf{t}), \tag{1.6}$$

  where $\mathbf{A}$ refers to the state-space matrix, which provides the oscillation information of a specific system.

  When a disturbance occurs, the system undergoes a transient subsequent with high damped modes and low damped modes. The modal methods focus on the less damped modes which are represented by the eigenvalues closer to the origin. The linear equivalents are achieved by applying reduction techniques that eliminate the high damped modes. Meanwhile, the modal methods are also corporate with the coherency methods to identify the coherent groups [113].

- **Estimation Methods**
  Although valuable contributions have been made, the computational requirements are still heavy by one of the aforementioned approaches, such as the eigenvalue analysis and diagonalization of the modal approach, and the transient stability analysis

for various contingencies of the coherency methods. The estimation methods are basically utilizing the measurement or simulation-based results to estimate the parameters of the equivalent model [115–118]. The advantage of these methods is that no information of the original system is required. The main challenge is to find the best parameters of the equivalent model which have the minimum error between the measured outputs and calculated outputs. Due to the development of high-performance simulation tools, these methods are widely used in dynamic equivalents of large power systems.

1.2 Motivation and Objectives

This research focuses on developing a practical method which can be implemented in the power/energy control center to reduce the computational burden and accelerate the emulation speed for dynamic security assessment of hybrid AC-DC grid. The two main factors which impact the emulation efficiency are the computational method and the hardware platform.

The major tasks and specific research objectives for this work are listed as following:

- **A novel relaxation algorithm for dynamic simulation**
  Current off-line commercial DSA tools such as TSAT®, and PSS®/e are using series calculation scheme. Meanwhile, taking the TSAT® solver package for example, only the Forward Euler (FE), Runge Kutta (RK), and Newton Raphson (NR) methods can be selected for solving the DAEs, which is insufficient for modern power systems with a large number of synchronous generators. Therefore, a novel relaxation algorithm is needed for a more efficient solution of the nonlinear differential algebraic equations of the integrated system model. Besides, the proposed algorithm should be massively parallelized and pipelined in hardware to realize the lowest latencies and minimum utilization of hardware resources.

- **Flexible time-stepping algorithm for dynamic simulation**
  In the traditional VTS algorithms, the time-step needs to be halved or double several times before reaching the proper time-step, and the process prolongs the simulation. For instance, after a disturbance is detected, the time-step is expected to shrink from 10 ms to 1 ms. The time-step will need to be halved 4 times by the traditional VTS algorithm. Meanwhile, each time-step adjustment results in the solution of the nonlinear system's differential equations to make sure the consequent LTE is smaller than the predefined threshold; otherwise, the time-step should be halved again until a proper time-step is found. Due to the relatively low sample frequency of the governor control system and the various time-steps adopted in AC and DC systems, the goal of this work is to propose a local equipment based flexible time-stepping scheme to realize FTRT emulation. The proposed flexible time-stepping algorithm is able to

find the proper time-step instantly and thus significantly reduce the computational burden, which is of ultra-importance in realizing FTRT.

- **Multi-mass synchronous generator model**
  In TS simulation, the synchronous generators are represented by several DAEs, which include mechanical equations, rotor electrical equations, and excitation system equations. Usually, the mechanical equations only contain one generator shaft, however, in practice, the mechanical part is driven by several steam turbines in conjunction with a governor system. The SSI emerges when the electrical oscillation frequency corresponds to one of the torsional oscillation frequencies. Therefore, a multi-mass torsional shaft model needs to be considered for analyzing the SSI, which provides detailed information of the torsional oscillation frequencies of a synchronous generator. Meanwhile, a corresponding governor system with four-stage steam turbines is also needed to provide mechanical torque to each shaft. With the properly designed multi-mass synchronous machine model, the SSI can be simulated under some specific faults.

- **SSCI phenomenon of PV plants**
  SSCI involves the interactions between a weak transmission system and a power electronics control system (such as HVDC links, SVC, or wind turbine control system) [40], which may induce serious damage to the power system. According to the literature review, SSCI and its mitigation techniques for conventional wind farm systems are well documented, however, not as much literature is available regarding the SSCI phenomenon in the context of series compensated PV farm systems. Due to the PV inverter and its control system, the PV stations and their neighboring transmission system are a potential source of SSCI.

  Supplementary damping controller techniques for mitigating SSCI have been reported recently. The controls and parameters have substantial impacts on defining the negative resistance of wind generators, which can significantly damp SSCI. Since the converter controllers are originally designed to compensate currents or voltages at the fundamental frequency, their control capability can be considerably reduced if they are used to inject the compensation signals only at the concerned subsynchronous frequency instead of fundamental. Meanwhile, for the commissioned large-scale wind farms, it is sophisticated and economically unviable to individually implement the control schemes on the existing converters of diversely located hundreds of WTGs that could be of different make and/or type. It is evident that both the RSC and GSC auxiliary damping controllers are specifically suitable for wind farms. There is not enough literature to support that supplementary damping controller techniques can be applied to photovoltaic power plants. Further, the utilization of FACTS devices or converter-based damping controllers is not an eco-

nomical solution to mitigate the SSCI in the real-world. Therefore, this work analyzes the oscillation modes of a typical PV farm and its transmission system by eigenvalue analysis, which provides the theoretical basis for the subsequent research on the SSCI phenomenon of PV plants. The FTRT based hardware emulation is also applied to provide optimal control strategies for damping the SSCI in the AC-DC grid with PV installations.

- **FPGA-based FTRT emulation for DSA**
  Driven by increasingly higher demands such as online dynamic security assessment, control and protection algorithm test, and system performance preview, the real-time systems have witnessed an explosive growth in these applications for being able to interact with real power system secondary devices. Currently, commercial simulators such as the TSAT®, and PSS®/e have been popular in the industry for factory acceptance tests as well as user training. However, the above mentioned products are basically off-line simulation tools, which are unable to provide real-time control data to an operating system when a disturbance occurs. The equipped high-speed communication interfaces in Xilinx Virtex® UltraScale+™ series FPGA boards can realize the real-time communication between FPGAs and external devices, which is suitable for energy control centers to realize predictive control. Furthermore, The reconfigurability of the FPGA enables each circuit part to program its function according to the application, which makes hardware-in-the-loop (HIL) emulation can be achieved. The enormous hardware resources make it suitable for emulating large-scale power systems, and eventually, the hybrid AC-DC grid is expected to be deployed on the FPGA boards.

- **Deep learning based dynamic equivalent model for TS simulation**
  The current industry practice is able to accelerate the TS simulation by adopting the dynamic equivalent methods to large-scale power systems. The dynamic equivalencing is achieved by reducing the number of generators and the network nodes, which requires a lot of computation to obtain a proper equivalent model. Most classical approaches require a complete input parameter, but available measurements may be insufficient to reliably identify all the model parameters. Thus, there is a need to develop an accurate dynamic equivalencing method with lower computational requirements. The deep learning technology has a high capability to deal with complicated nonlinear problems and to resemble the behavior of the original systems in a general frame, and therefore, it is suitable for the dynamic equivalent model. By selecting proper training datasets, the trained machine learning based dynamic equivalent model is able to provide detailed dynamic results according to the disturbance in the study zone.

1.3 Contributions of the Thesis

This work targets both FTRT hardware emulation and its applications for DSA of AC-DC grid, as given in Fig.1.1 The main contributions are briefly summarized in the following:

- The proposal of a fine-grained relaxation algorithm (FGRA) for calculating the nonlinear DAEs of the synchronous generators. The proposed algorithm enables the DAEs being solved in parallel and is suitable for hardware design.
- Proposal of the AC-DC grid interface and its synchronization strategy. The proposed strategy enables the EMT and TS simulation types compatible in one program.
- FPGA-based hardware design methodology for realization of FTRT emulation. The proposed FTRT emulation platform can be utilized in the energy control center for dynamic security analysis.
- Proposal of a local-equipment-based flexible time-stepping algorithm and its synchronization strategy for computation efficiency improvement.
- Coordinated communication and emulation among several FPGA boards. The data communication among the FPGA boards is realized, which improves the scalability of the FTRT emulation.
- Introduction of the multi-mass synchronous machine model in TS simulation. The detailed machine model enables emulating and analyzing the SSI phenomenon possible in TS emulation.
- Detailed eigenvalue analysis to investigate the SSCI between a PV inverter and neighboring weak transmission system.
- A dynamic active/reactive power injection strategy for mitigating the SSI and SSCI using FTRT hardware emulation.
- Hardware emulation of contingency screening for DSA of large-scale AC-DC grid. The properly designed hardware platform enables extensive contingencies running simultaneously in FTRT mode.
- Improvement of the AC-DC grid interface using dynamic voltage injection. The novel interface strategy is able to maintain a constant admittance matrix despite the HVDC converter outputs being time-varying, which consequently reduces hardware resource utilization and expedites the emulation.
- Proposal of the Gated Recurrent Unit (GRU)-based synchronous generator model and dynamic equivalent model in TS simulation for further acceleration of FTRT emulation.

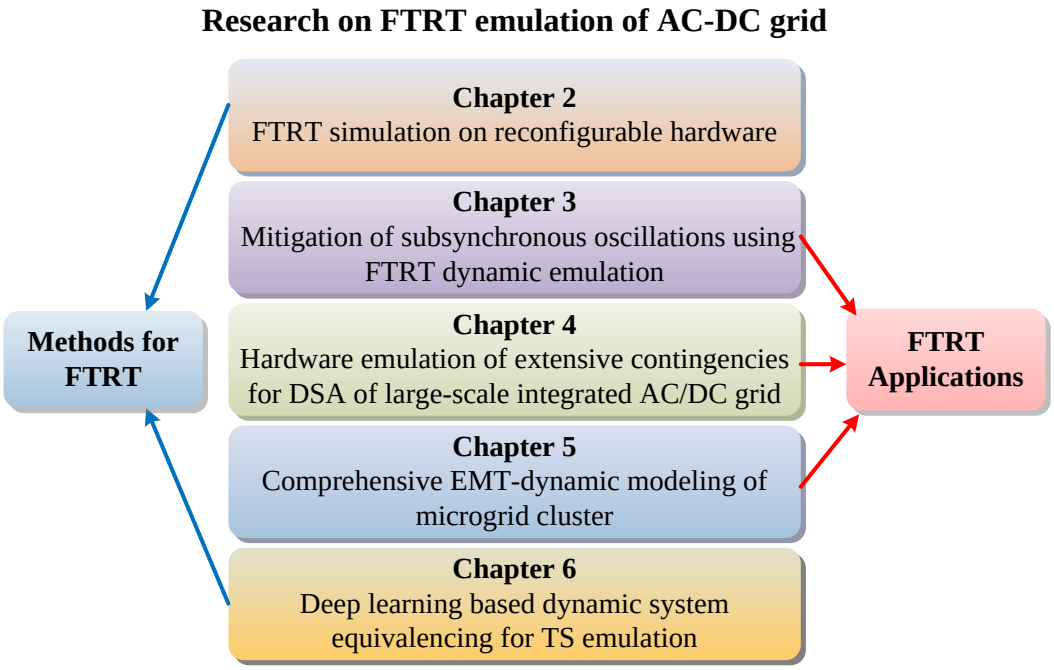

Figure 1.1: Contributions of the proposed research.

1.4 Thesis Outline

This thesis consists of eight chapters and is organized as follows:

- **Chapter 1: Introduction** - The background of this work is briefly introduced. The motivation and contributions are also summarized.

- **Chapter 2: FTRT simulation on reconfigurable hardware** - This chapter proposes a faster-than-real-time (FTRT) dynamic simulation of integrated AC-DC grids on the reconfigurable parallel hardware architecture of the field programmable gate array (FPGA). A fine-grained relaxation algorithm (FGRA) is proposed for a more efficient solution of the nonlinear DAEs of the integrated AC-DC grid, including the detailed nonlinear models of the synchronous generators in the AC system which can be solved in parallel on the FPGA. Two case studies are used to illustrate the efficacy of the proposed algorithm and demonstrated a closed-loop prediction scenario for improving grid stability.

  Meanwhile, a faster-than-SCADA/real-time (FT-SCADA/RT) emulation based on flexible time-stepping (FTS) algorithm is also proposed for the energy control center to predict and mitigate the impacts after serious disturbances using FPGAs. To gain a high acceleration over SCADA/RT, the FTS-based dynamic emulation is applied to

the AC grid.

- **Chapter 3: Mitigation of subsynchronous oscillations using FTRT dynamic emulation** - As the FTRT hardware emulation can be achieved by the methods proposed in Chapter 2, this part focuses on the applications of the proposed FTRT emulation, which can be utilized to the energy control center for mitigating the subsynchronous oscillations. The multi-mass generator model is applied to TS simulation for analyzing the SSI in a hybrid AC-DC grid integrated with wind farms. Meanwhile, the oscillation modes of a typical PV network are also analyzed, and the FTRT emulation is utilized for predicting the SSCI and consequently mitigating its impacts on AC grid by taking the effective active/reactive power control action.

- **Chapter 4: Hardware emulation of extensive contingencies for DSA of large-scale integrated AC-DC grid** - In addition to the SSR problems, the system may encounter several kinds of contingencies. In this chapter, the hardware emulation is investigated to accelerate the dynamic security assessment (DSA) solution of a large-scale AC-DC system deployed on the FPGAs. An emulation platform containing multiple FPGA boards is established so that with a proper allocation it has a sufficient capacity to accommodate the system under study which has 6 ACTIVSg 500-bus systems interconnected by a 6-terminal DC grid. The efficacy of the proposed FTRT hardware emulation platform is demonstrated by 2 case studies with more than 5500 contingencies analyzed in total, where an FTRT ratio of more than 208 is achieved for the hybrid AC-DC grid, while it is over 277 times for a single 500-bus system.

- **Chapter 5: FTRT hardware emulation of dynamics of a grid of microgrids** - The increasing proportion of MGs brings new challenges to online dynamic security assessment. In this chapter, comprehensive modeling of a grid of MGs for FTRT emulation is proposed, which can be utilized in the energy control center for contingencies analysis. Electromagnetic transient (EMT) modeling is applied to the microgrid in order to reflect the detailed device processes of the converter and renewable energy sources, while the AC grid utilizes transient stability modeling to reduce the computational burden and obtain a high acceleration value over real-time. Consequently, a dynamic power injection interface is proposed for the coexistence of the two simulation types.

- **Chapter 6: Machine learning based dynamic system equivalencing for FTRT digital twin** - Although an achievable high speedup ratio can be obtained by the proposed methods and the hardware design strategies, the scalability of the FPGA-based FTRT emulation seems to be insufficient. Machine learning based synchronous generator model (SGM) and dynamic equivalent model (DEM) are proposed in this chapter, which are able to significantly reduce the computational burden of the traditional TS simulation. For the experiments, the Gated Recurrent Unit (GRU) algo-

rithm is adopted to train the synchronous generators and DEM, where the training and testing dataset are obtained from the off-line simulation tool TSAT®. A testing system containing 15 ACTIVSg 500-bus systems interconnected by a 15 terminal DC grid is built for validating the accuracy of the proposed FTRT emulation platform. Due to the complexity of emulating a large-scale AC-DC grid, multiple FPGA boards are also applied.

- **Chapter 7: Conclusions** - The research conclusions are provided and future work is discussed.

2

FTRT Emulation of AC-DC Network on Reconfigurable Hardware

In this chapter, a fine-grained relaxation algorithm (FGRA) is proposed for FTRT dynamic simulation of integrated AC-DC networks on the massively parallel reconfigurable hardware architecture of the FPGA. The floating point operations carried out at the smallest resolution of the proposed algorithm are scalar in nature and any matrix operations are completely avoided. The AC-DC system component models undergo a fully decoupled parallel solution. High parallelism and pipelining is achieved for the FTRT hardware emulation on the Xilinx Virtex® UltraScale+™ XCVU9P FPGA. Two case studies are emulated to provide insight into the performance of the proposed algorithm.

Meanwhile, as various equipment have different dynamic responses to time-steps, the local equipment based flexible time-stepping for FT-SCADA/RT emulation is also proposed in this chapter, which is able to decide a proper time-step for each circuit part. The proposed flexible time-stepping algorithm is applied on the integrated AC-DC network for FT-SCADA/RT emulation. The multi-terminal HVDC grids undergoing electromagnetic transient (EMT) simulation are utilized to enhance the stability of the traditional AC transmission system. Various contingencies, such as three-phase-to-ground fault, generator outage, and sudden load change are emulated to reveal the efficiency of the proposed local equipment based flexible time-stepping algorithm. The FT-SCADA/RT hardware emulation is suitable for a real power control center to predict the system's stability, as well as to select an optimal control strategy after a serious disturbance occurs.

2.1 Fine-grained Relaxation Algorithm for FTRT Emulation on Reconfigurable Hardware

2.1.1 AC Grid Modeling

The main components in the AC grid are synchronous generators and networks. The synchronous generator model contains the mechanical part, electrical part, and excitation system. The transmission lines, compensators, as well as loads, contribute to the network.

2.1.1.1 Synchronous Machine Model

As mentioned in Chapter 1, the differential equation (1.1) containing the dynamics of a synchronous generator has 9 types of state variables. Among the 9^{th}-order differential algebraic equations (DAEs), the mechanical equations which refer to the derivative of rotor angle and angular velocity are given below:

$$\dot{\delta} = \omega_R \cdot \Delta\omega(t), \tag{2.1}$$

$$\dot{\Delta\omega}(t) = \frac{1}{2H}[T_e + T_m - D \cdot \Delta\omega(t)], \tag{2.2}$$

The rotor electrical circuit equations adopt 2 windings on the d-axis and 2 damping windings on the q-axis, which can be expressed as:

$$\dot{\psi}_{fd}(t) = \omega_R \cdot [e_{fd}(t) - R_{fd} i_{fd}(t)], \tag{2.3}$$

$$\dot{\psi}_{1d}(t) = -\omega_R \cdot R_{1d} i_{1d}(t), \tag{2.4}$$

$$\dot{\psi}_{1q}(t) = -\omega_R \cdot R_{1q} i_{1q}(t), \tag{2.5}$$

$$\dot{\psi}_{2q}(t) = -\omega_R \cdot R_{2q} i_{2q}(t), \tag{2.6}$$

Meanwhile, the control system of the synchronous generator includes automatic voltage regulator (AVR) and power system stabilizer (PSS) as given in Fig. 2.1, and the differential equations have the following expression:

$$\dot{v}_1(t) = \frac{1}{T_R} \cdot [v_t(t) - v_1(t)], \tag{2.7}$$

$$\dot{v}_2(t) = K_{stab} \cdot \dot{\Delta\omega}(t) - \frac{1}{T_\omega} v_2(t), \tag{2.8}$$

$$\dot{v}_3(t) = \frac{1}{T_2} \cdot [T_1 \dot{v}_2(t) + v_2(t) - v_3(t)]. \tag{2.9}$$

Therefore, the vector $\mathbf{x}$ is repetitive when multiple synchronous generators exist in the power system, with a basic 9-D unit for a single generator as

$$\mathbf{x} = [\delta, \Delta\omega, \psi_{fd}, \psi_{1d}, \psi_{1q}, \psi_{2q}, v_1, v_2, v_3], \tag{2.10}$$

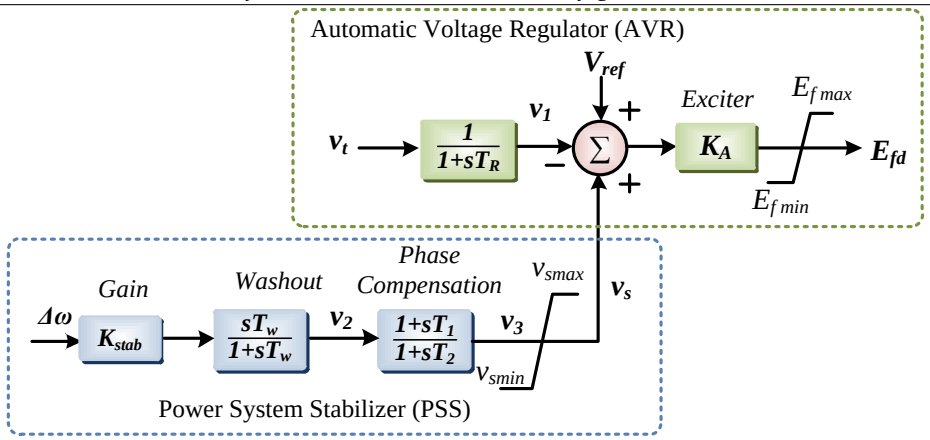

Figure 2.1: Excitation system of the synchronous generator.

where the meanings of the constant values in (2.7)-(2.15), such as ω_R, H, D, R_{fd}, R_{1d}, R_{1q}, R_{2q}, T_R, K_{stab}, T_ω, T_1, and T_2 can be found in [36]. Meanwhile, the generator field voltage e_{fd} in the reciprocal per unit system is related to the exciter output voltage E_{fd}, which can be expressed as the following equation:

$$e_{fd}(t) = \frac{R_{fd} \cdot K_A \cdot (V_{ref} - v_1(t) + v_s(t))}{L_{ad}}, \tag{2.11}$$

where R_{fd} and L_{ad} are constant values, and the coefficient K_A is given in Fig. 2.1.

2.1.1.2 AC Network Model

The AC network mainly comprises transmission lines, transformers, loads, and shunt capacitors. The transmission lines and the transformers are represented as lumped π models. The fixed loads and shunt capacitors are treated as the admittance which is associated with the buses, given as

$$Y_{Load} = \frac{P_{Load} + jQ_{Load}}{V_{Bus}^2}, \tag{2.12}$$

where V_{Bus} refers to the voltage of the local bus, P_{Load} is the active power of the load, and Q_{Load} represents the reactive power of the load or the shunt capacitor. Following the derivation of the admittance matrix of the AC network, the output current of the generators can be solved by the following matrix equations:

$$\begin{bmatrix} \mathbf{I_m} \\ \mathbf{I_r} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{mm}} & \mathbf{Y_{mr}} \\ \mathbf{Y_{rm}} & \mathbf{Y_{rr}} \end{bmatrix} \begin{bmatrix} \mathbf{V_m} \\ \mathbf{V_r} \end{bmatrix}, \tag{2.13}$$

where m is the number of synchronous generator nodes, r is the number of remaining nodes. Absence of current injection into the non-generator buses means $I_r = [\mathbf{0}]$ and

$$\mathbf{I_m} = \mathbf{Y_R V_m}, \tag{2.14}$$

where $\mathbf{Y_R} = \mathbf{Y_{mm}} - \mathbf{Y_{mr}}\mathbf{Y_{rr}^{-1}}\mathbf{Y_{rm}}$ is the reduced admittance matrix of $m \times m$ dimension. Under the D-Q frame,

$$\begin{aligned} \mathbf{I_{Dm}} &= \mathbf{G_m}\mathbf{V_{Dm}} - \mathbf{B_m}\mathbf{V_{Qm}}, \\ \mathbf{I_{Qm}} &= \mathbf{G_m}\mathbf{V_{Qm}} + \mathbf{B_m}\mathbf{V_{Dm}}, \end{aligned} \tag{2.15}$$

where $\mathbf{G_m}$ and $\mathbf{B_m}$ are the real and imaginary part of the reduced admittance matrix, respectively. The relationship between the voltage and current is

$$\begin{aligned} V_D &= I_D \cdot u_1 + I_Q \cdot u_2 + u_5, \\ V_Q &= I_D \cdot u_3 + I_Q \cdot u_4 + u_6, \end{aligned} \tag{2.16}$$

where u_{1-6} can be calculated from the state variables, given as:

$$u_1 = -R_a, \tag{2.17}$$

$$u_2 = X''_{ad}sin^2(\delta) + X''_{aq}cos^2(\delta) + X_l, \tag{2.18}$$

$$u_3 = -(X''_{ad}cos^2(\delta) + X''_{aq}sin^2(\delta) + X_l), \tag{2.19}$$

$$u_4 = -R_a, \tag{2.20}$$

$$u_5 = -cos(\delta)E''_d - sin(\delta)E''_q, \tag{2.21}$$

$$u_6 = cos(\delta)E''_q - sin(\delta)E''_d, \tag{2.22}$$

$$E''_d = X''_{aq}(\frac{\psi_{q1}(t)}{X_{q1}} + \frac{\psi_{q2}(t)}{X_{q2}}), \tag{2.23}$$

$$E''_q = X''_{ad}(\frac{\psi_{fd(t)}}{X_{fd}} + \frac{\psi_{d1}(t)}{X_{d1}}), \tag{2.24}$$

$$X''_{ad} = X_l + \frac{L_{ad} \cdot L_{fd} \cdot L_{d1}}{L_{ad} \cdot L_{fd} + L_{ad} \cdot L_{d1} + L_{fd} \cdot L_{d1}}, \tag{2.25}$$

$$X''_{aq} = X_l + \frac{L_{aq} \cdot L_{q1} \cdot L_{q2}}{L_{aq} \cdot L_{q1} + L_{aq} \cdot L_{q2} + L_{q1} \cdot L_{q2}}, \tag{2.26}$$

where R_a, X_l, X_{q1}, X_{q2}, X_{fd}, X_{d1}, L_{ad}, L_{fd}, L_{d1}, L_{aq}, L_{q1}, and L_{q2} refer to stator resistance, stator leakage reactance, reactance of damper winding $q1$, reactance of damper winding $q2$, field winding reactance, reactance of damper winding $d1$, d-axis mutual inductance, field winding inductance, inductance of damper winding $d1$, q-axis mutual inductance, inductance of damper winding $q1$, inductance of damper winding $q2$, respectively, which are constant values of the synchronous generator. Meanwhile, the variables with superscription $''$ represent the subtransient reactance and electromotive force, and the variables in time-domain are the synchronous state variables solved from (2.1)-(2.6). Following the acquirement of new state variables the relationship between $\mathbf{I_m}$ and $\mathbf{V_m}$ can be ascertained. Meanwhile, the matrix $\mathbf{Y_R}$ can be obtained from the original admittance matrix, and only $\mathbf{I_m}$ is yet to be solved in (2.14). Then, the rotor current and voltage in d-q frame can be derived according to their D-Q common frame counterparts, i.e.,

$$\begin{aligned} i_{dq} &= I_{DQ} \cdot e^{-j\delta}, \\ e_{dq} &= V_{DQ} \cdot e^{-j\delta}, \end{aligned} \tag{2.27}$$

The variables i_{dq} and e_{dq} lay foundation for calculating the voltages including their phases at non-generator nodes, the power flow, etc.

2.1.2 Proposed Fine-grained Relaxation Algorithm

The adoption of a traditional linear solver for nonlinear equation solution falls short of efficiency, particularly in utilizing the processor's parallelism. The FGRA is thereby proposed to fully exploit the FPGA's parallel hardware architecture by introducing concurrency in solving the $9m$-D matrix equation.

Congregating the 9 state variables of all the synchronous generators as a basic vector unit $\mathbf{x_i}$ in an m-machine system where each one is connected to an individual bus will lead to a diagonal matrix equation expressed as

$$\begin{bmatrix} \Delta\mathbf{x_1} \\ \Delta\mathbf{x_2} \\ \Delta\mathbf{x_3} \\ \vdots \\ \Delta\mathbf{x_m} \end{bmatrix} = \begin{bmatrix} \mathbf{J_1} & \mathbf{0} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{J_2} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{J_3} & \cdots & \mathbf{0} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{J_m} \end{bmatrix}^{-1} \begin{bmatrix} -\mathbf{F_1} \\ -\mathbf{F_2} \\ -\mathbf{F_3} \\ \vdots \\ -\mathbf{F_m} \end{bmatrix}, \tag{2.28}$$

where $\Delta\mathbf{x_i}$ and $-\mathbf{F_i}$ are 9×1 vectors, and $\mathbf{J_i}$ is a 9×9 matrix. In typical dynamic simulations, all synchronous generators are located on different buses, i.e., one swing bus and the remaining are PV buses, which means the generators are fully independent from each other resulting in non-diagonal elements in the Jacobian matrix are all 0, and therefore the equation can be decomposed into m 9-D matrix equations.

The second level of parallelism is achieved by further decomposing the 9-D matrix equation which solves the state variables of a single generator. Taking the form of

$$\begin{bmatrix} \Delta x_1^{n+1} \\ \Delta x_2^{n+1} \\ \Delta x_3^{n+1} \\ \vdots \\ \Delta x_9^{n+1} \end{bmatrix} = \begin{bmatrix} J_{11}^n & J_{12}^n & J_{13}^n & \cdots & J_{19}^n \\ J_{21}^n & J_{22}^n & J_{23}^n & \cdots & J_{29}^n \\ J_{31}^n & J_{32}^n & J_{33}^n & \cdots & J_{39}^n \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ J_{91}^n & J_{92}^n & J_{93}^n & \cdots & J_{99}^n \end{bmatrix}^{-1} \begin{bmatrix} -f_1^n \\ -f_2^n \\ -f_3^n \\ \vdots \\ -f_9^n \end{bmatrix}, \tag{2.29}$$

In a specific iteration the Jacobian matrix and function f_i are constant. As mentioned above, the traditional methodology has to calculate at least m times of 9×9 matrix inversion, which poses a severe challenge to realizing the fast-than-real-time simulation. An arbitrary state Δx_i can be derived as

$$\begin{aligned} J_{11}^n \Delta x_1^{n+1} + J_{12}^n \Delta x_2^n + \cdots + J_{19}^n \Delta x_9^n &= -f_1^n, \\ J_{21}^n \Delta x_1^n + J_{22}^n \Delta x_2^{n+1} + \cdots + J_{29}^n \Delta x_9^n &= -f_2^n, \\ &\vdots \\ J_{91}^n \Delta x_1^n + J_{92}^n \Delta x_2^n + \cdots + J_{99}^n \Delta x_9^{n+1} &= -f_9^n, \end{aligned} \tag{2.30}$$

$$\Delta x_i^{n+1} = \frac{-f_i^{n-1} - \sum_{j\neq i}^{j=1-9} J_{ij}^n \Delta x_j^n}{J_{ii}^n}, \tag{2.31}$$

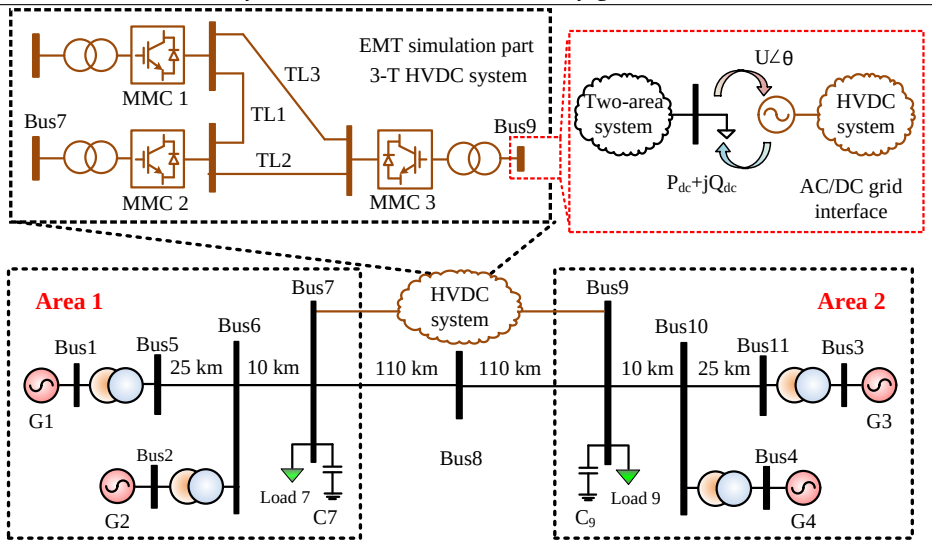

Figure 2.2: Case 1: Integrated AC-DC grid for dynamic-EMT co-simulation based on Kundur's two-area system.

where the superscription n denotes the count of Newton-Raphson iteration which is required since the state variable to be solved is built upon the history values of its counterparts, but no extra N-R iteration loop should be introduced since it already existed due to the nonlinear characteristic of the DAE. (2.31) shows that every arbitrary Δx_i is only related to the i^{th} row in the Jacobian matrix **J**. Generally, the Jacobian matrix is sparse; therefore, we can further substitute (2.31) via eliminating the zero coefficients. This approach can significantly shrink the calculation time and reduce the hardware resources. Moreover, the fact that the synchronous generator is a nonlinear component means that the coefficients have to be updated within every iteration. The terms with superscription n+1 can be set as initial values or updated from the last iteration.

Compared with traditional waveform relaxation [121] and its evolutive algorithms [10, 26], FGRA has the advantages of low iteration and usage of hardware resource. The proposal of (2.31) enhances parallelism as it can be seen that the original matrix equation with a dimension of $9m$ solved using traditional matrix solution methods is decomposed into $9m$ algebraic equations which, due to mutual independence, is suitable for hardware parallelism on the FPGA board.

2.1.3 AC-DC Grid Interface

Fig. 2.2 shows a typical integrated AC-DC grid as the 1^{st} case of dynamic-electromagnetic transient (EMT) co-simulation for analyzing system stability. The 3-terminal HVDC system that undergoes EMT simulation is linked to its AC counterpart via Bus 7 and 9, and considering that it is EMT simulation, a time-step of 200μs is adopted to reveal more details as well as to keep the computation convergent; whilst the AC grid subjected to sta-

bility analysis is based on Kundur's two-area system which has 4 synchronous generators in addition to 11 buses. The dynamic simulation focuses on the transient stability of the synchronous machines and network data with a large time-step of $10ms$, 50 times that of the EMT simulation. Therefore, in order to establish the co-simulation with a unified time scheme, the AC system synchronizes the active power data with the DC side after the EMT simulation calculates 50 steps. Therefore the AC system solves a new admittance matrix before the iteration in every time-step.

Since different simulation algorithms are applied to the AC and DC systems, an interface is introduced to enable the two types of simulation compatible in one program. However, the HVDC stations denoted by $MMC_1 \sim MMC_3$ are dynamic processes, regardless of the type, i.e., rectifier or inverter, which can be modeled as time-varying P+jQ loads, or to be more specific, both P and Q values are updated in every time-step to reflect the real dynamic process on the point of common coupling (PCC), as shown in Fig. 2.2. The mechanism of the interface is as follows, after the introduction of the AC-DC grid interface, the AC grid dynamic simulation is concurrent with its EMT counterpart with the former type of simulation yields the PCC voltage in every time-step for the latter to proceed. In return, the DC grid undergoing EMT simulation provides the power P+jQ to the AC grid in the same manner. Therefore, both the PCC voltage and the power are not constant and the dynamic processes is enabled. Furthermore, in dynamic simulation, the HVDC stations are taken as loads so that the bus phase voltages $U\angle\theta$ can be obtained; on the other hand, the instantaneous bus voltages are calculated to keep the EMT simulation going on and consequently the power of each station can be derived and returned to the AC grid.

2.1.4 Modular Multilevel Converters

Fig. 2.3(a) shows a 3-phase (N+1)-level MMC operating as an HVDC grid terminal. Within a half-bridge submodule, there are 2 IGBTs and a DC capacitor. When the upper switch S_1 is turned on, the capacitor is inserted; otherwise, it is bypassed. Therefore, the Thévenin equivalent circuit of a submodule can be expressed by

$$v_{SM} = \int (V_{g1} \cdot \frac{i_{arm}}{C})dt + i_{arm} \cdot r_{on}, \tag{2.32}$$

where i_{arm} means the MMC arm current, V_{g1} is a binary denoting the gate signal of the upper switch S_1, and r_{on} represents the on-state resistance of the switch [122].

2.1.4.1 MMC Average Value Model

The FTRT simulation prefers models that induce the least computational burden whilst ensuring sufficient accuracy, and adopting the average value model (AVM) for a modular multilevel converter (MMC) [123], [124] is justified by the type of study, where power flow, instead of converter details, is the main concern. Compared with its detailed coun-

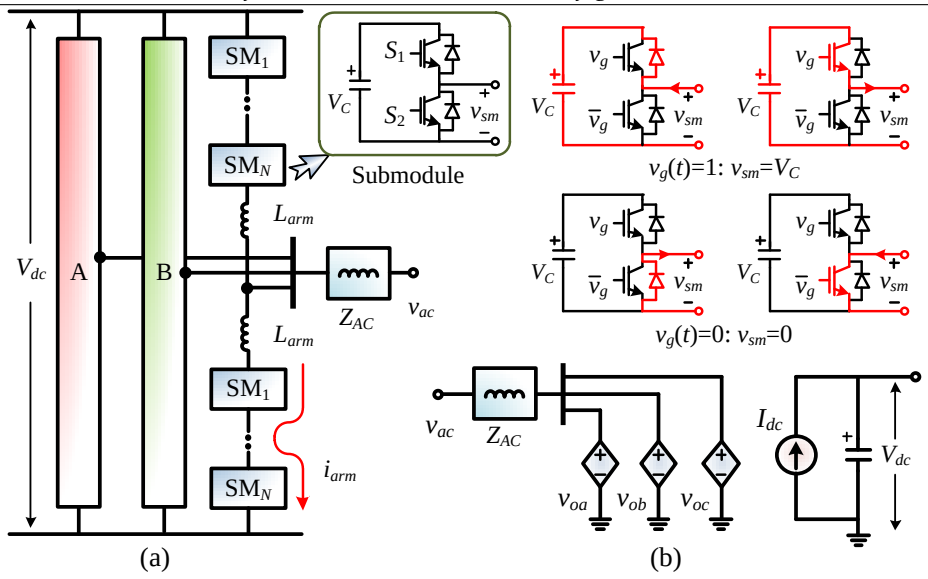

Figure 2.3: Illustration of modular multilevel converter modeling: (a) Three-phase topology, (b) average value model.

terpart [122] shown in Fig. 2.3(a), the hardware latency of AVM is much lower, while it retains the capability to provide power flow under the influence of a controller.

Assuming that the MMC is internally balanced, each submodule can then be deemed as a voltage pulse source whose width is determined by the gate signal of the upper switch, as it is obvious from Fig. 2.3(b) that the submodule capacitor is inserted under ON-state, whilst the OFF-state indicates that it is bypassed.

Since the voltage of an arbitrary SM capacitor equals to the DC bus voltage divided by the total number of submodules in an arm, denoted as N, the equivalent voltage source can be expressed as

$$v_{sm(i)}(t) = \frac{V_{dc}}{N} \cdot sgn[sgn(v_{g(i)}(t) - V_{th}) + 1], \tag{2.33}$$

where $v_{g(i)}(t)$ represents a time-varying gate signal of the upper IGBT, whose threshold voltage is V_{th}, and the sign function sgn yields +1, 0, and -1 when the expression inside it is greater than, equal to, or less than 0, respectively. As a result, the arm voltage equals to

$$v_{arm} = \sum_{i=1}^{N} v_{sm(i)} + L_{arm}\frac{di_{arm}}{dt}, \tag{2.34}$$

where L_{arm} denotes the arm inductance.

The well-balanced condition in the AVM yields no circulating current, meaning that the differential term in the above equation can be omitted and the AC side output voltage becomes a vector sum of voltages of the two arms,

$$v_o = \frac{V_{dc}}{N}(\sum_{i=1}^{N} S_{SM(i)} - \sum_{i=N+1}^{2N} S_{SM(i)}), \tag{2.35}$$

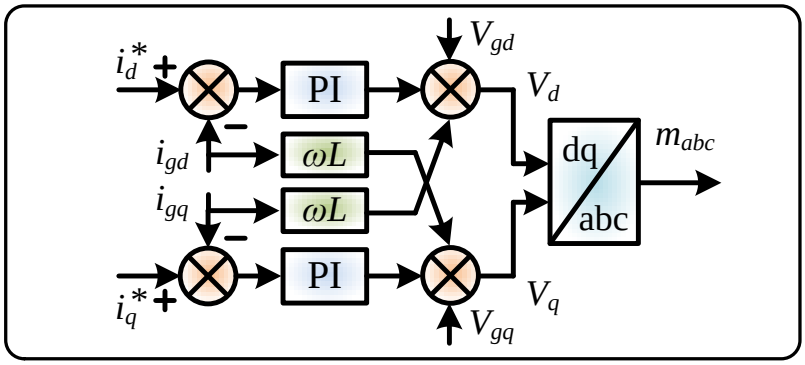

Figure 2.4: MMC current controller in d-q frame

where

$$S_{SM(i)} = sgn[sgn(v_{g(i)}(t) - V_{th}) + 1], \tag{2.36}$$

denotes the ON-OFF state of a submodule. Then, the two-arm structure can be simplified into a single-arm equivalence, as demonstrated in Fig. 2.3(b), so that the corresponding hardware design on FPGA reduces to the minimum to achieve the fastest response to contingencies in the external power grid.

2.1.4.2 MMC Controller

The MMC adopts a two-loop control scheme in which the outer-loop controller is in charge of converter functions, e.g., regulation of the active/reactive power and the AC bus voltage, which yields the reference current $i^*_{d,q}$ under the d-q frame:

$$i^*_{d,q} = K_p(T^*_{ar} - T_{ar}) + K_i \int (T^*_{ar} - T_{ar})dt, \tag{2.37}$$

where K_p and K_i are constants, T^*_{ar} and T_{ar} represent the control target and the actual output, respectively. The current controller given in Fig. 2.4(c) is the core part which amplifies the current error to gain the voltage $V_{d,q}$, which is then converted to the 3-phase signals m_{abc} that are sent to the MMC inner-loop controller employing phase-shift strategy [124].

2.1.4.3 DC Network Model

The MMC DC side is represented by a current source in parallel with a capacitor. The injected DC current is

$$I_{dc} = \frac{\eta P_{ac}}{V_{dc}} = \frac{3\eta(V_d I_d + V_q I_q)}{2V_{dc}}. \tag{2.38}$$

where η is the converter efficiency, and $V_{d,q}$, $I_{d,q}$ are the AC side voltage and current in d-q frame.

The DC transmission lines are represented by the π model, the parasitic capacitance is merged with the MMC DC side capacitor, while the internal node in the series R-L is

eliminated by expressing the Norton equivalent circuit as

$$G_{TL} = (\frac{2L_{dc}}{dt} + R_{dc})^{-1}, \tag{2.39}$$

$$J_{TL} = 2v_L^i \cdot (\frac{2L_{dc}}{dt} + R_{dc})^{-1}, \tag{2.40}$$

where v_L^i is the incident pulse of the inductor modeled as a section of lossless transmission line [126].

2.1.5 Hardware Emulation on FPGA

The emulation of integrated AC-DC grids is conducted on the Xilinx Virtex® UltraScale+™ XCVU9P FPGA board which has 1182240 look-up tables (LUTs), 2364480 flip-flops (FFs), and 6840 DSP slices to accommodate various hardware designs. The parallelism and pipelined designed approach enables a high FTRT ratio for system performance prediction and subsequently appropriate regulations which help to stabilize the power system. The package Xilinx Vivado allows designing hardware modules by coding in C/C++ in its high-level synthesis (HLS) tool to shorten the design cycle, and the AC-DC grid given in Fig. 2.2 is taken as an example since other configurations also conform to the same hardware design principle, i.e., the modularity, which means each of the power system components, or functions such as the FGRA, is written as an individual C/C++ function and then transformed into a hardware module in HLS that can be imported into Vivado® to form the top-level using the hardware description language VHDL. Fig. 2.5 shows the hardware configuration for the FTRT simulation.

In this work, we emulated the two-area system and IEEE 39-bus system with various contingencies. The data and the program in VHDL language were downloaded from the host computer via the JTAG interface, which has the ability of in-circuit-debug, in-circuit-emulator, and in-system-program. The digital output of the FPGA board was transferred into analog data by the digital-and-analogic-converter (DAC) board through the FPGA Mezzanine Card (FMC) connector so that the waveforms can be displayed on the oscilloscope. However, in a power grid control center, the data from the real system can be delivered to the FPGA board running a virtual grid via Samtec® FireFly connector, Quad Small Form-factor Pluggable (QSFP) interface which has dual cages with a maximum transmission speed of up to $4\times28\ Gbps$, and the Ethernet interface, and vice visa for the output since all these three ports are bidirectional regarding data transmission. The QSFP interface is constructed with fiber optic material, which can significantly reduce the signal attenuation, and therefore, in the power grid control center, it is applied for data exchange with external devices, including other FPGAs. In the meantime, a significantly reduced data communication delay of the QSFP connector helps maintain FTRT simulation. It is also available for transferring data through Ethernet jack as a backup since the Ethernet connector can reach a maximum speed of 1000 $Mbps$. On the other hand, the FireFly connector

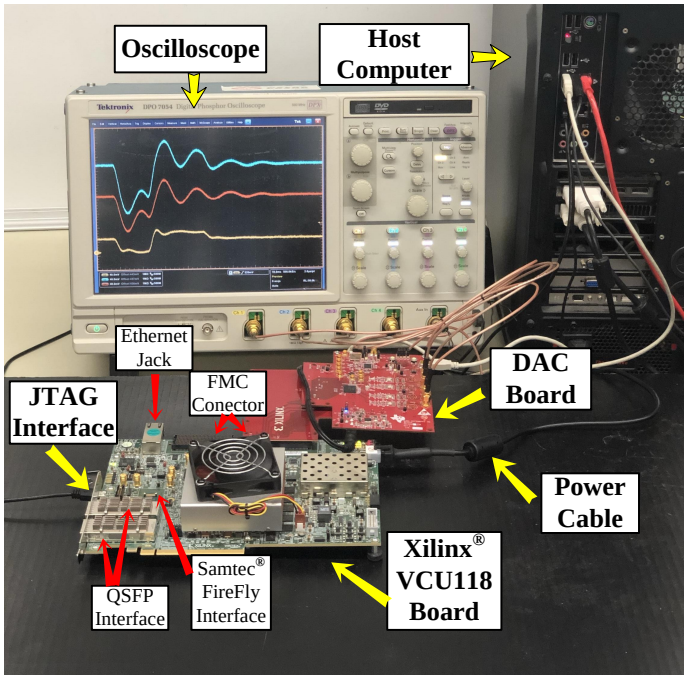

Figure 2.5: Hardware setup for FTRT simulation.

is the latest on-board data communication interface with both copper and optical modules. Nowadays, the QSFP interface and FireFly connector have the same transmission speed of 28 $Gbps$ per lane and similar features. However, the FireFly connector will be widely used in the future with the advantages such as small size and low power consumption. When an actual contingency occurs, the FTRT hardware platform in the control center can yield several solutions to mitigate the frequency rise and other damage. Therefore, the control center may have sufficient time to deal with the faults as well as make an optimal decision.

Fig. 2.6 shows a concise hardware architecture of the integrated AC-DC grid. The solution of the discretized form of the differential equation is conducted with parallelism due to the proposed FGRA, which, along with the nonlinear nature of the differential equation, requires iteration until the maximum error among all state variables and those caused by fine-grained relaxation algorithm is less than the tolerance δ_{max}. Meanwhile, the EMT simulation mainly involves 3 modules: the MMC including the AVM and its controller (CNT), and the HVDC network is conducted simultaneously. As the only type of signal that the dynamic simulation needs from the DC grid is the dynamic active power, which is converted into admittance according to the voltage of the bus the HVDC station connects to, the admittance matrix of the AC system can be formed in the module $GMatrix$. The iterative solution of (1.1) may yield the state variables multiple times in a single time-step, forcing the hardware module Network Solution to follow the same procedure. Once the dynamic simulation results converge, the AC bus voltages are fed back to the DC grid so

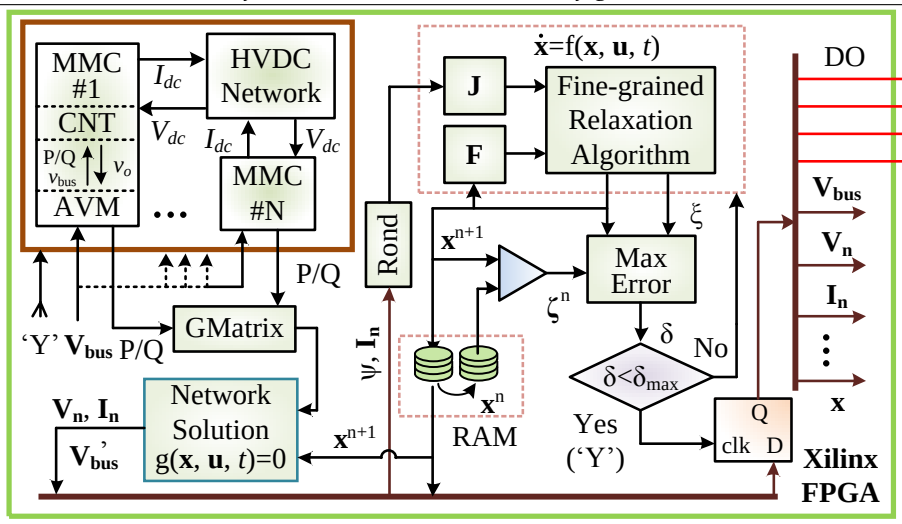

Figure 2.6: Integrated AC-DC grid top-level hardware design scheme and signal flow routes.

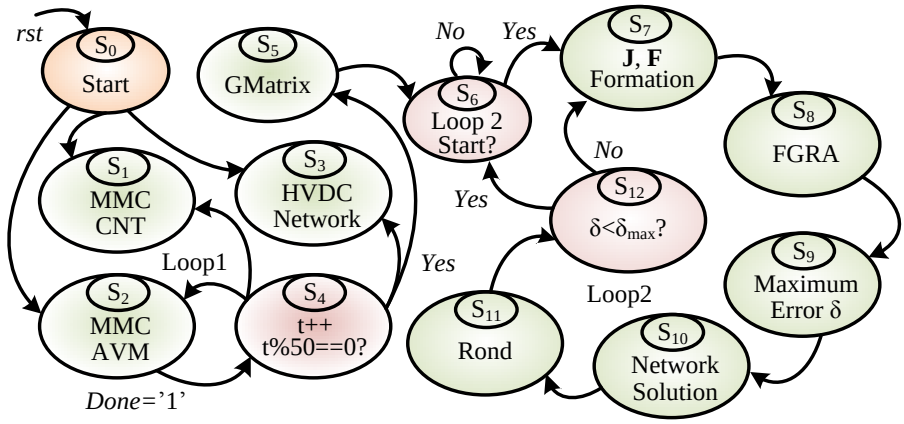

Figure 2.7: Top-level finite state machine for the coordination of hardware modules of the integrated AC-DC grid.

that the EMT simulation can move forward to the next time-step. Any results produced during the co-simulation, denoted as *DO* in the figure, can be exported and displayed on the oscilloscope.

Noticing that the time-step required by EMT simulation should be much smaller than that of dynamic simulation in addition to a correct sequence that all the hardware modules need to follow, a top-level finite state machine (FSM) is required, as shown in Fig. 2.7. The co-simulation starts once the reset order is issued, and the EMT simulation of the DC grid starts in $Loop1$. A time-step of $10ms$ used in the dynamic simulation means that the DC grid is computed 50 times more frequent than its AC counterpart. In $Loop2$, the discretized differential equation is first solved to obtain the state variables using the proposed FGRA. The calculation of the maximum error of the results is followed by solving the network

Table 2.1: Specifics of major AC-DC grid hardware modules

Module	BRAM	DSP	FF	LUT	Latency
Case 1	28	3819	416284	535773	7462 T_{clk}
	0.6%	55.8%	17.6%	45.3%	–
Case 2	32	4127	560929	866576	7462 T_{clk}
	0.7%	60.3%	23.7%	73.3%	–
XCVU9P	4320	6840	2364480	1182240	–
MMCCNT	0	54	5733	11085	85 T_{clk}
MMCAVM	16	208	8292	19277	90 T_{clk}
DCGrid	0	17	2209	2868	73 T_{clk}
GMatrix	12	1045	123388	126767	1313 T_{clk}
JMatrix	0	53	5045	4984	30 T_{clk}
FVector	0	87	8376	8219	32 T_{clk}
Maxerror	0	4	3874	4570	394 T_{clk}
ACNet	16	534	43928	57664	269 T_{clk}
Rond	16	402	27032	42750	98 T_{clk}
FGRA	0	8	1010	1596	35 T_{clk}
Gauss	0	4807	554584	925577	1464 T_{clk}
LU	$\geq$78	$\geq$480	$\geq$157849	$\geq$225383	$>$1805 T_{clk}

equation, and the results are used to update the synchronous generators. The necessity of FGRA iteration in computing the overall loop is determined by the maximum error δ and its threshold δ_{max}: repetition of the loop is mandatory if the results are not sufficiently accurate; on the other hand, a convergence does not guarantee a new start of the dynamic simulation unless – as mentioned above – the DC grid has proceeded to another $50m$s.

Table 2.1 gives the design specifics of major hardware modules, where the "MMC-CNT," "MMVAVM," and "DCGrid" denote the functions in DC system. The "Gmatrix," "JMatrix," and "FVector" refer to the modules of calculating admittance matrix, Jacobian matrix, and the F vector in (2.29), respectively. The "Rond" function presents the function of updating of the Jacobian matrix elements. All the modules except for the "GMatrix" are inside the iteration loop. Since there is nearly no time-delay of values assignment in hardware simulation, the new state variables updating function is not shown in Table 2.1. With the latencies above, it can calculate the accelerator factor theoretically, then validate in hardware emulation. The DC grid parts are fully parallelized with the largest latency of 90 T_{clk}, i.e., 90 clock cycles, under an FPGA clock frequency of $10n$s, meaning with an EMT simulation time-step of 200μs, the FTRT ratio is over 222 times. Meanwhile, in a TS time-step, the latencies inside the iteration can be calculated as $32 + 35 + 394 + 98 = 559$ T_{clk}, where the "FVector" and "JMatrix" can be parallelized, similarly, the "MaxError" and "ACNet" functions should be synchronized, therefore we choose the maximum latency between the parallel parts.

Nevertheless, it is not the actual latency since the iteration is not taken into account.

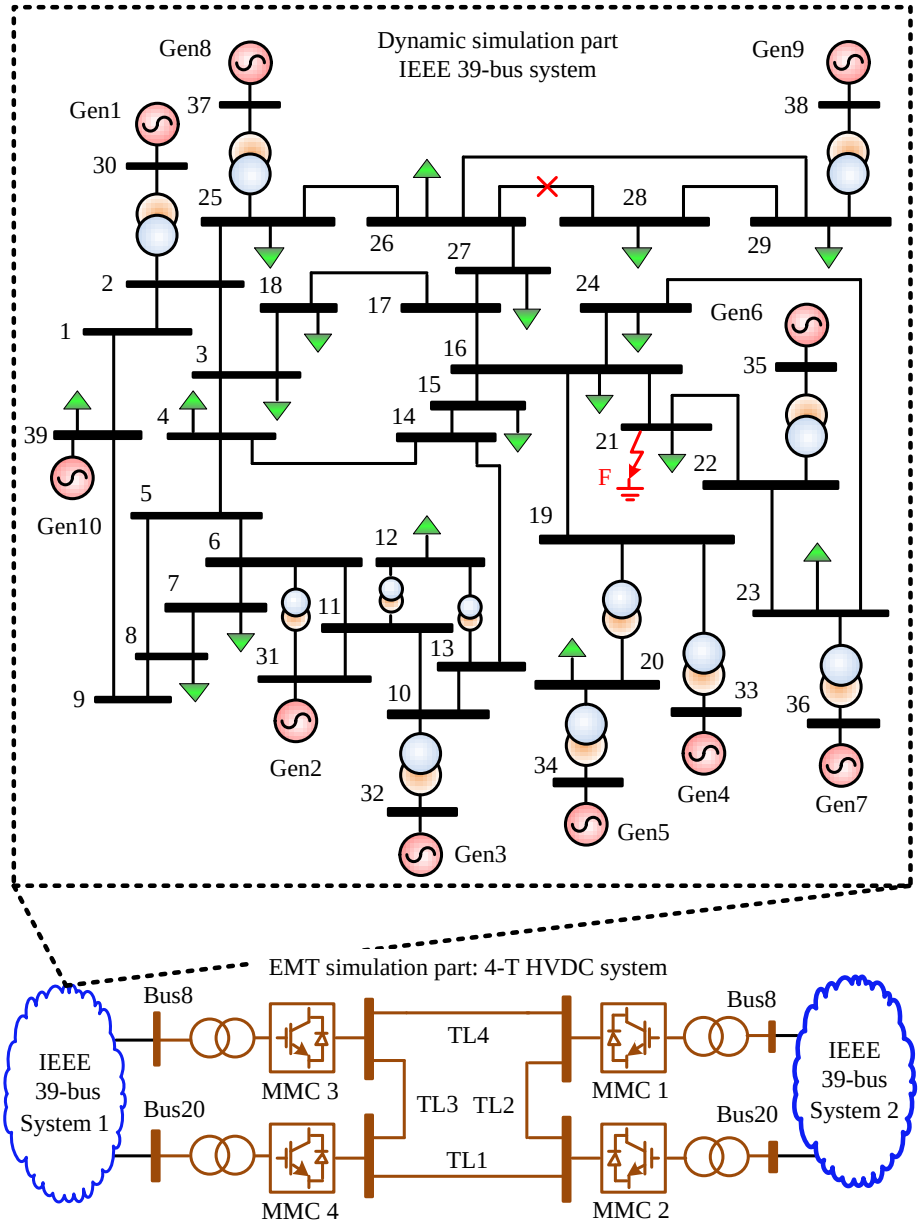

Figure 2.8: Case 2: integrated large-scale AC-DC grid based on 2 IEEE 39-bus systems interconnected with a 4-terminal HVDC grid.

Take the hybrid two-area AC-DC system as an example, the maximum iteration is 11. Since the number of iterations in every time-step varies significantly, the FGRA function may need to calculate 11 times in every time-step on the FPGA, or calculate with less than 11 times and wait idly till an equivalent amount of time expires. With a maximum FGRA iteration of 11, the estimated overall latency of the dynamic simulation is $559 \times 11 + 1313 = 7462$ clock cycles, where the "GMatrix" with a latency of 1313 T_{clk} is only calculated outside of the iteration loop, meaning with a time-step of $10ms$, the FTRT ratio reaches

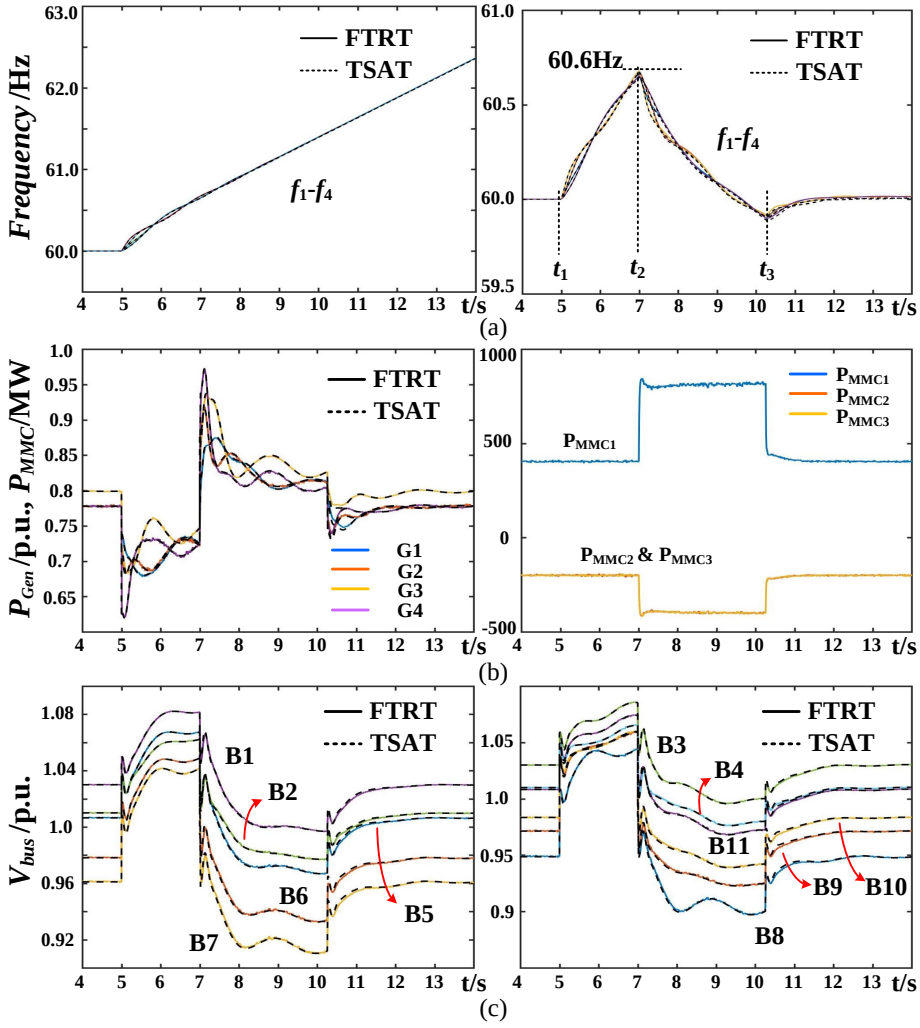

Figure 2.9: Predictive control based on FTRT co-simulation for power system stability analysis: (a) AC grid frequency, (b) output power of synchronous generators and MMCs, and (c) AC bus voltages.

over $\frac{10ms}{7462\times10ns} \approx 134$. Meanwhile, the EMT model can be solved in parallel with the TS model which is the AC grid, i.e., the DC grid will send data to the AC system in every 50 steps, considering that the DC part is 222 times faster than real-time which is faster than AC grid, the DC grid needs to "wait" the AC grid in every 50 EMT time-steps. So we can estimate that the hardware emulation is 134 times faster than real-time. By comparison, if the traditional matrix-based method is adopted, with a maximum iteration number of 5, the overall latency would be 11253 clock cycles – larger than the proposed FGRA method. In addition to Case 1, the HVDC grid is also integrated into two IEEE 39-bus systems for the study of a more practical scenario, given as Case 2 in Fig. 2.8. It shows that the chosen FPGA board has sufficient hardware resources for the final designs of both cases.

2.1.6 FTRT Simulation Results and Validation

The two dynamic-EMT co-simulation cases are tested to showcase the predictive regulation of FTRT in stabilizing the power system following various contingencies, and the results based on FPGA are validated by the off-line transient stability simulation tool TSAT in the DSATools^{TM} suite.

2.1.6.1 Two-Area System

In the two-area system, the 2 MMCs connected to Bus 7 and 9 operate as inverter stations, while the remaining one as the rectifier station is linked to an infinite bus. At t=5s, a load of 183.5MW and 383.5MW are removed temporarily from Bus 7 and 9 respectively, causing instability to the AC system which cannot be restored even the loads are recovered 2s later to its original capacity of 767MW and 1567MW, as can be seen from Fig. 2.9(a), the frequency keeps rising and eventually it is far beyond the maximum allowed 1% threshold, i.e., 60.6Hz. On the contrary, the integration of HVDC system greatly improves the stability issue by doubling the rectifier's output power to 800MW following the detection of the grid frequency exceeding the threshold at around 7s, and it lasts till the frequency is restored to the standard 60Hz at t=10s, as Fig. 2.9(b) shows. Meanwhile, when Bus 7 and 9 are unloaded, the output power of the 4 synchronous generators, as expected, decrease, accompanied by a severe rise of all AC bus voltages given in Fig. 2.9(c). The intervention of HVDC suppresses all the voltages, which are finally restored, and so are the output powers of the synchronous generators.

2.1.6.2 Large-scale AC-DC grid

In Fig. 2.8, $MMC3$ and $MMC4$ operate as the rectifiers while the other two operate as inverters. At t=5s, a ground fault lasting 270ms occurs at Bus 21 in $System$ 1. The imminent impacts are severe disturbances to the AC system, including the synchronous generators' rotor angle, the bus voltage, and the frequency, as shown in Fig. 2.10, e.g., the rotor angle of $G5$ surges to over 200° in less than 0.3s, the voltage of the synchronous generator $G6$ plummet to below 0.5 p.u., and the frequencies rise beyond the 60.6Hz threshold. An initial test by the dynamic-EMT co-simulation proved that the AC system cannot restore its frequency to below 60.6Hz even when the fault is cleared, which is why the HVDC grid participates in stabilizing the AC power system by maintaining a continuous injection of an additional 200MW and 100MW from the two rectifiers respectively into the DC grid between t=5.2s and t=9s. Therefore, the FTRT simulation is able to help tackle power system stability issues by providing necessary solutions as well as quantifying the exact change to be made such as the amount of power to be injected in this case prior to action from the actual system.

The inter-area oscillation test is also conducted to further demonstrate the predictive

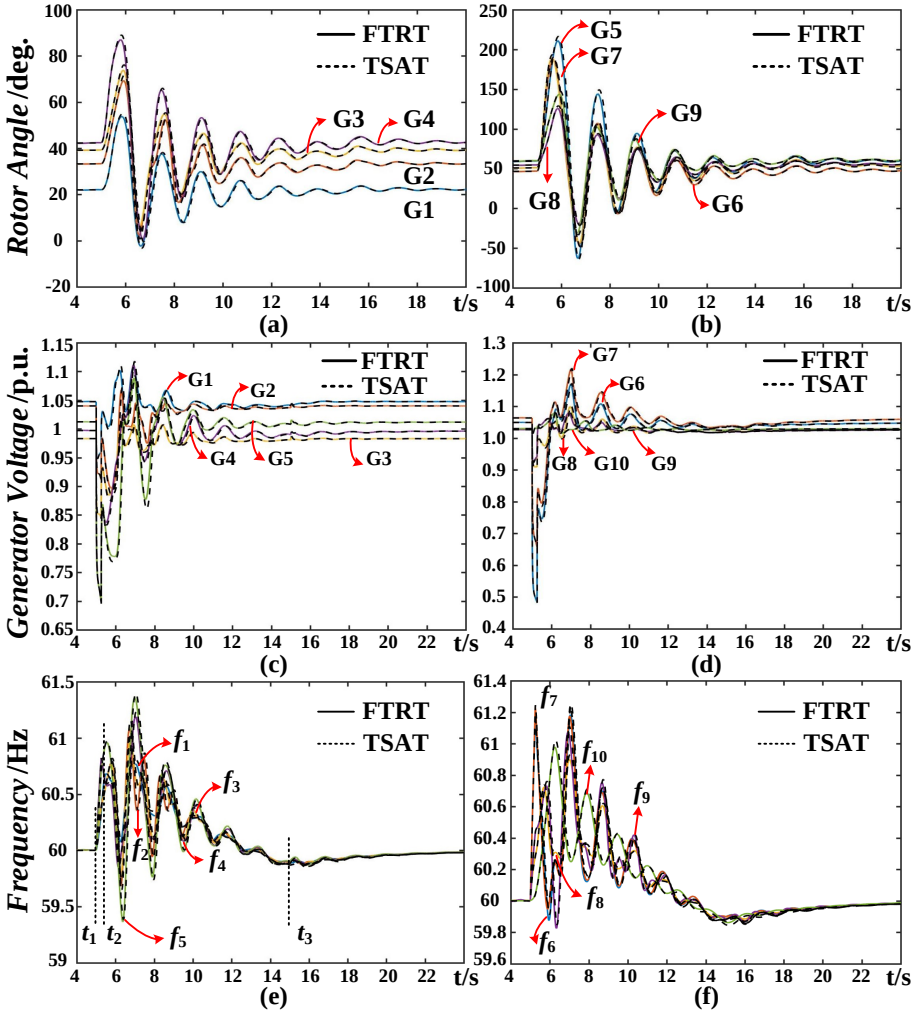

Figure 2.10: FTRT co-simulation for preview of generator behaviors under AC system ground fault: (a) Rotor angles, (b) voltages, and (c) frequencies.

regulation function of FTRT in stabilizing the power system, and the results are given in Fig. 2.11. At t=5s, the transmission line between Bus 26 and Bus 28 in the $System$ 1 is temporarily removed, so that the normal operation of the load on Bus 28 is mainly sustained by the 9^{th} generator. At t=10s, the line is recovered while the one between Bus 28 and 29 is disconnected. It can be seen that the system starts to oscillate, e.g., rotor angles of the generators, and the output powers of many of them, as given in Fig. 2.11(a)-(c). At t=15s, the connection between Bus 28 and 29 is restored, and the two rectifiers begins to deliver more power from the AC system subjected to inter-area oscillation, i.e., an additional extraction of 100MW and 50MW from Bus 8 and Bus 20, respectively. The benefit of FTRT is thoroughly demonstrated by the fact that the all artificial interventions, including that by the HVDC system, can stop at t=17.5s even when the system is still undergoing severe oscillations since the power system is able to recover gradually by itself at around t=25s, as shown in Fig. 2.11(d)-(f), and the actual system action can follow suit

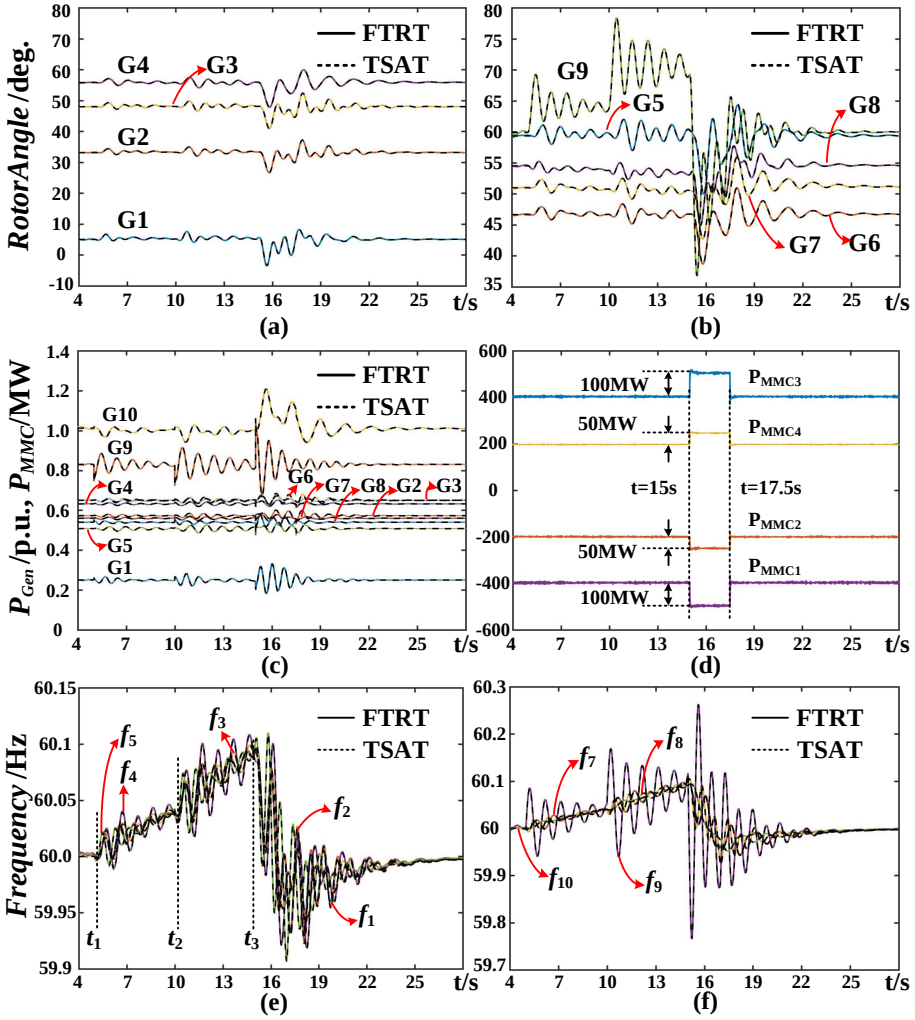

Figure 2.11: FTRT co-simulation for preview of AC-DC grid behavior under inter-area oscillation: (a) Generator rotor angles, (b) output power of generators and MMCs, and (c) generator frequencies.

since this scenario has already been simulated in advance and proven to be effective. It should be pointed out that representing the HVDC converter by the time-varying P+jQ load plays a significant role in stabilizing the AC grid frequency, as shown in Fig. 2.9(b) and Fig. 2.11(d); on the contrary, the AC grid will not stabilize if the equivalent load is kept constant.

With its results proven to be correct, the FTRT ratio that the hardware emulation can achieve in both cases is validated by the oscilloscope waveforms. The 4 synchronous generators' voltages and their relative angles to generator $G4$ are given in Fig. 2.12(a), and the former waveforms show an identical trend to that of AC buses in Case 1. Similarly, the generator waveforms under inter-area oscillation of Case 2 are shown in Fig. 2.12(b). It should be particularly pointed out that both of the waveforms in Fig. 2.12(a) have the time interval in real-time of 13.4s. Meanwhile, 1 division in the oscilloscope presents $10ms$

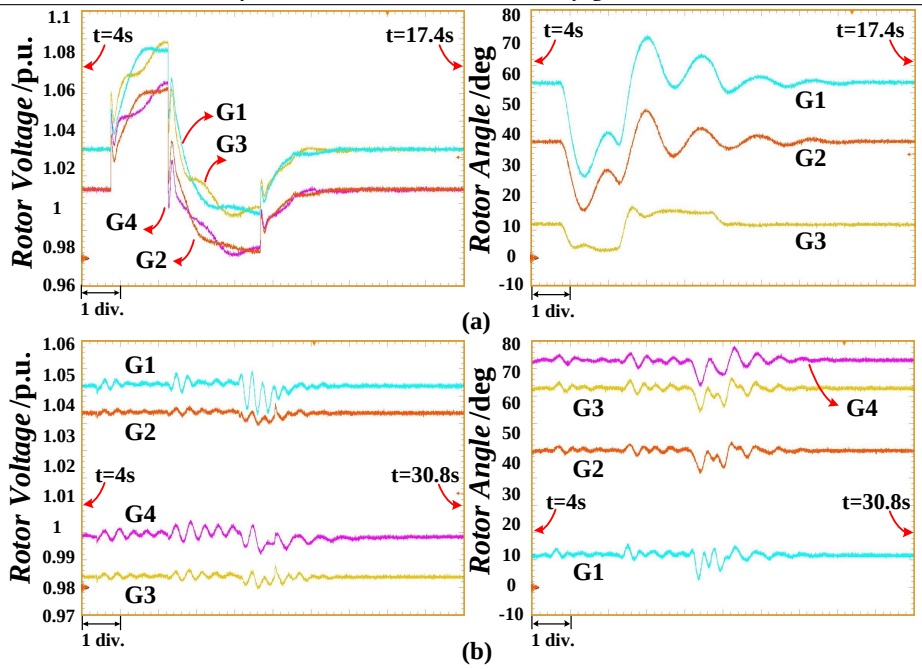

Figure 2.12: FTRT co-simulation results displayed in the oscilloscope from: (a) Case 1 (x-axis: 10ms/div.), and (b) Case 2 (x-axis: 20ms/div.).

which refers to 100ms on the x-axis. The discrepancy between the oscilloscope scan time and the duration that these waveforms actually denote indicates that the proposed FTRT co-simulation is approximately 134 times faster than real-time, meaning it leaves a sufficient margin for the actual power system to react and adopt the strategy tested in advance by the hardware emulation on FPGA.

2.2 Flexible Time-Stepping Dynamic Emulation of AC-DC Grid for Faster-Than-SCADA Applications

As mentioned the main challenge of emulating a power transmission system is basically solving a series of differential algebraic equations (DAEs). Due to the non-linear nature of the equations, the Newton-Raphson (NR) algorithm is required. The NR method is essentially an iterative method, which is not ideally suited for parallel design in FPGAs due to the inherently sequentially of iterations until convergence. The explicit methods such as Forward Euler, or 4^{th}-order Runge-Kutta (RK4) are applied in this section due to the low resource usage. In a trade-off between emulation efficiency and the accuracy, RK4 is adopted as the solution for calculating the non-linear DAEs, as given below:

$$RK_1 = dt \cdot f(t_n, x_n), \tag{2.41}$$

$$RK_2 = dt \cdot f(t_n + \frac{dt}{2}, x_n + \frac{RK_1}{2}), \tag{2.42}$$

$$RK_3 = dt \cdot f(t_n + \frac{dt}{2}, x_n + \frac{RK_2}{2}), \tag{2.43}$$

$$RK_4 = dt \cdot f(t_n + dt, x_n + RK_3), \tag{2.44}$$

$$x_{n+1} = x_n + \frac{1}{6}(RK_1 + 2RK_2 + 2RK_3 + RK_4), \tag{2.45}$$

where x_n refers to the state variables of the synchronous generator, dt is the emulation time-step.

2.2.1 Flexible Time-Stepping

As mentioned above, all the DAEs should be discretized into numerical equations. The local truncation error is an estimate of the error introduced in a single time-step. Assuming that x_{n+1} is the calculated state variable, and $x(t_{n+1})$ refers to the corresponding exact value, the LTE can be expressed in the following equation:

$$LTE = x(t_{n+1}) - x_{n+1}, \tag{2.46}$$

Theoretically, LTE exists in both implicit and explicit numerical integration methods. However, it is difficult to find the exact value which is $x(t_{n+1})$ in a non-linear system. The approximate values can be solved by iterative methods or explicit integration methods using the results of the previous time-step, which means the exact state variables cannot be obtained directly in a non-linear system due to the time-varying state equations. Multi-step integration approximations have higher precision than low-order integration methods. The results from the higher-order integration methods are treated as the exact values, the time-step can be resolved according to the true values. Taking the 5^{th}-order Adams-Bashforth (AB5) for example, the predicted value of the next time-step can be expressed as follows:

$$\dot{x} = F(t, x(t)), \tag{2.47}$$

$$\bar{x}_{n+1} = x_n + \frac{dt}{720} \cdot (1901F_n - 2774F_{n-1} + 2616F_{n-2} - 1274F_{n-3} + 251F_{n-4}), \tag{2.48}$$

where $\bar{x}_{n+1}$ is the predicted state variable of the next time-step, dt refers to the time-step. As the exact values are solved from AB5, the adaptive time-step ($\widetilde{dt}$) can be obtained as:

$$\widetilde{dt} = \frac{6\,|\bar{x}_{n+1} - x_{n+1}|}{(RK_1 + 2RK_2 + 2RK_3 + RK_4)}, \tag{2.49}$$

The principle of LTE-based variable time-stepping algorithm is as follows: if the LTE is larger than the predefined threshold ϵ, which is given in (2.50), the time-step is decreased to obtain higher accuracy and vice versa.

$$\epsilon = \left| \frac{\bar{x}_{n+1} - x_{n+1}}{\bar{x}_{n+1}} \right| \times 100\%, \tag{2.50}$$

As can be seen, traditional LTE-based variable time-stepping algorithms are discrete. The time-step is doubled or halved until it reaches the upper or lower limit. With discrete

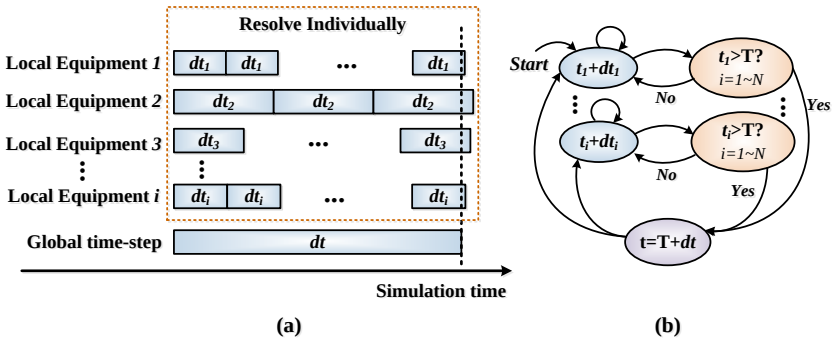

Figure 2.13: Local equipment based flexible time-stepping for hybrid AC-DC grid emulation: (a) principle of the proposed algorithm, (b) time instant synchronization.

time-steps, the calculated values may not be perfectly suitable for the specific step. The proposed flexible time-stepping strategy is able to yield a proper time-step instantly. In the traditional variable time-stepping (VTS) algorithm, the time-step will be halved or doubled several times; in the meantime, the DAEs solved by the numerical integration method will also be calculated in each iteration until a suitable time-step is found. Therefore, the proposed flexible time-stepping algorithm can significantly reduce the computational burden and execution time.

2.2.2 Event-Based Flexible Time-Stepping

This algorithm is relative to the contingencies taking place in the system, such as three-phase-to-ground fault, generator outage, or sudden load change. In a dynamic transient emulation system, after a serious disturbance, the synchronous generators may lose synchronism, resulting in a rapid change of output voltages and generator rotor angles. Therefore, the rate of change voltage and rotor angle (dv/dt, $d\delta/dt$) can be treated as the main time-step control indices. When dv/dt or $d\delta/dt$ in a specific time-step change significantly, the time-step can be reduced or increased to ensure accuracy. This method has lower sensitivity than the flexible time-stepping algorithm, it is usually executed in a relatively large time-step, and therefore can significantly reduce the emulation time.

2.2.3 Local Equipment Based Flexible Time-Stepping

According to the sensitivity and stability of the various components in the power transmission system, different time-stepping control strategies are applied, which is beneficial to reduce the computational burden in low sensitivity parts. While the utilization of various time-stepping strategies may lead to an asynchronous time instant at the interface, which may lead to emulation unstable. Therefore, a hybrid time-steps control algorithm should be generated. For instance, the output mechanical torque (T_m) of the governor

system in the synchronous generator has a low sensitivity to time-step variation; in other words, a relatively large time-step will not influence the stability of the governor system. The event-based variable time-stepping method which provides time-steps ranging from 5-10ms is employed in the generator control system as shown in Fig. 2.13(a). To ensure the accuracy of the mechanical and electrical parts, the flexible time-stepping strategy should be adopted, which is usually executed in small time-steps after a disturbance occurs.

The local equipment based flexible time-stepping algorithm contributes a localized time-step dt_i produced in each component. Once a disparity emerges among them, the emulation goes forward only when the time instants of all variable time-stepping systems exceed the global time-step which is determined by the largest time-step of the subsystems. In the proposed emulation platform, the generator control systems are always computed with the largest time-step, which is therefore chosen as the global time-step. The synchronization mechanism works as follows: the control systems proceed at a much lower sample frequency, and they enter the next time-step only when the time instants of all local equipment reach beyond their current value; otherwise, all the components compute individually while the global system waits for them to finish. The time instant synchronization of the local equipment based flexible time-stepping algorithm is given in Fig. 2.13(b).

2.2.4 Large-Scale AC-DC Grid Test System

2.2.4.1 AC-DC Grid Interface

Fig. 2.14 shows a typical integrated AC-DC grid, where the IEEE 118-bus test systems [127, 128] are connected with 4-terminal HVDC system at Bus 25 and Bus 54. *MMC*3 and *MMC*4 act as rectifier stations, while *MMC*1 and *MMC*2 are treated as inverter stations. The IEEE 118-bus systems undergoing the transient stability analysis have a flexible time-step ranging from 1ms to 10ms. On the other hand, to reveal the dynamic process of the 4-terminal HVDC, the electromagnetic transient (EMT) emulation is adopted for the DC grid, which has a fixed time-step of 200μs. The local equipment based flexible time-stepping is applied for establishing an integrated co-emulation time-step scheme. Due to the distinct emulation strategies of the AC and DC grid, a proper interface should be designed.

In this case, the converter stations are utilized for delivering power among IEEE 118-bus systems. The converters can be treated as time-varying P+jQ loads, which means both P and Q values are updated in every time-step to reveal the dynamic process of the converter stations. At the point of common coupling (PCC), the power injections of MMC stations can be calculated in (2.12) and introduced in the admittance matrix of the AC network.

In the proposed EMT and transient stability co-simulation of the hybrid AC-DC grid, the bus voltage angle can be directly obtained from the solution of the AC network equations, and therefore, the PLL is not used in the converter controller. Due to parallelism in the DC grid, the PLL has no impact on the emulation speed, albeit the hardware resource

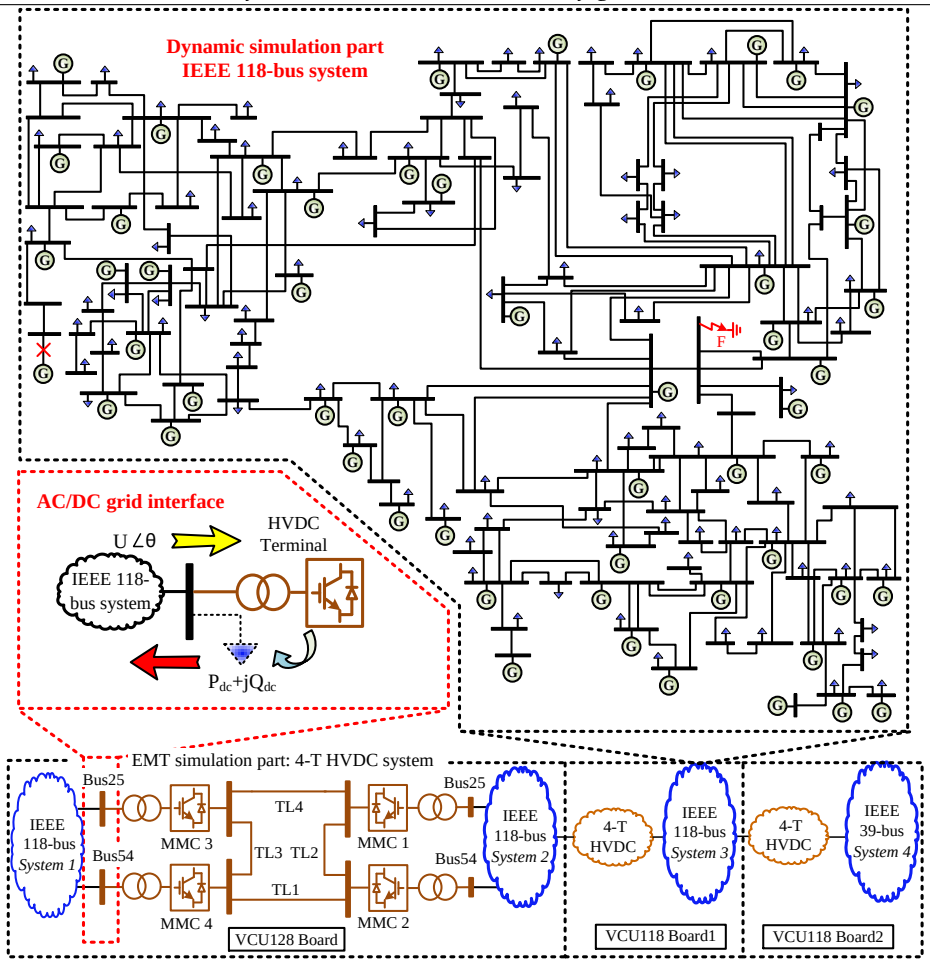

Figure 2.14: Integrated AC-DC grid for dynamic-EMT co-emulation.

utilization increases slightly, as shown in Table 2.3. To emulate the integrated AC-DC grid with high accuracy and low hardware resource burden, and also due to the fact that the PLL can trace the PCC phase angle instantly, it is reasonable to adopt the calculated phase angle.

2.2.4.2 AC-DC Grid Components Modeling

The AC grid undergoes the TS simulation and the 9^{th}-order synchronous generator model is also adopted. The detailed synchronous generator and network equations are given in 2.1.1. Meanwhile, the fully detailed model is also tested on the Xilinx Virtex® UltraScale+™ VCU118 FPGA board, and the AVM is still chosen as the simulation method for the converters in the 4-T HVDC grid. The conventional method considering the IGBT and its anti-parallel diode as a gate-signal-controlled two-state resistor falls short of revealing correct system performance when the DC line fault occurs. To avoid that, the unidirectional feature of the diode is taken into account, i.e., when the anode potential is higher than

Table 2.2: Specifics of detailed MMC hardware modules

Module	Latency	BRAM	DSP	FF	LUT
MMCDetailed	170 T_{clk}	0	75	25418	40960
MMCCNT	185 T_{clk}	0	58	10013	19077
HVDCNetwork	107 T_{clk}	0	20	2958	4098

that of the cathode, the diode conducts, otherwise, it is under OFF state. The improvement in the switch model is accompanied by adopting the N-R iteration, which makes the computation more burdensome than the AVM.

Based on the proposed interface, regardless of the MMC model, the HVDC part can always be deemed as a time-varying complex power P+jQ injection to the AC system, and the dynamic simulation provides a converter station with AC bus voltage amplitude and phase angle in complex domain for the EMT simulation. Meanwhile, the d-q frame-based control schemes in both AVM and detailed model are largely the same and the impact of the controller on the HVDC can be reflected in both cases. Therefore, there is no significant difference in power injection by using AVM and a detailed model. Regarding model validation, in order to make a reasonable and fair comparison for the FTRT simulation results, the MMC AVM is also applied to the AC-DC grid. In Table 2.2, we provide the latencies and resources of the MMC detailed model. Comparing with the AVM, the latencies and hardware resources of a detailed model are a little larger. With a maximum time-step of 50μs, the detailed model has an FTRT ratio of $\frac{50\mu s}{185 \cdot 10ns} \approx 27$, which is slower than the AVM. Therefore, the AVM was chosen for FTRT simulation without compromising the simulation accuracy.

2.2.5 FT-SCADA/RT Emulation Platform on FPGAs

The hardware emulation of the hybrid AC-DC grids was conducted on Xilinx Virtex® UltraScale+™ FPGAs. The integrated hardware platform includes three FPGA boards: two VCU118 evaluation boards featuring the XCVU9P FPGAs and a VCU128 board with XCVU37P FPGA. Each XCVU9P FPGA includes 1182240 look-up tables (LUTs), 2364480 flip-flops (FFs), and 6840 DSP slices. The XCVU37P FPGA contains 9024 DSP slices, 1303680 LUTs, and 2607360 FFs. Two IEEE 118-bus systems connecting with one 4-T HVDC system are accommodated on the VCU128 board. The remaining parts are emulated on the two VCU118 boards, as shown in Fig.2.14. The mechanism of the hardware design is as follows: the Xilinx Vivado® package enables designing hardware modules by coding in C/C++ in its high-level synthesis (HLS) tool to shorten the design cycle; The components or functions which consist of the integrated AC-DC grid in Fig. 2.14 are transformed into a hardware module in HLS that can be imported into Vivado® to form the top-level using the hardware description language VHDL. Fig. 2.15 shows the hardware configuration for the FT-SCADA/RT emulation.

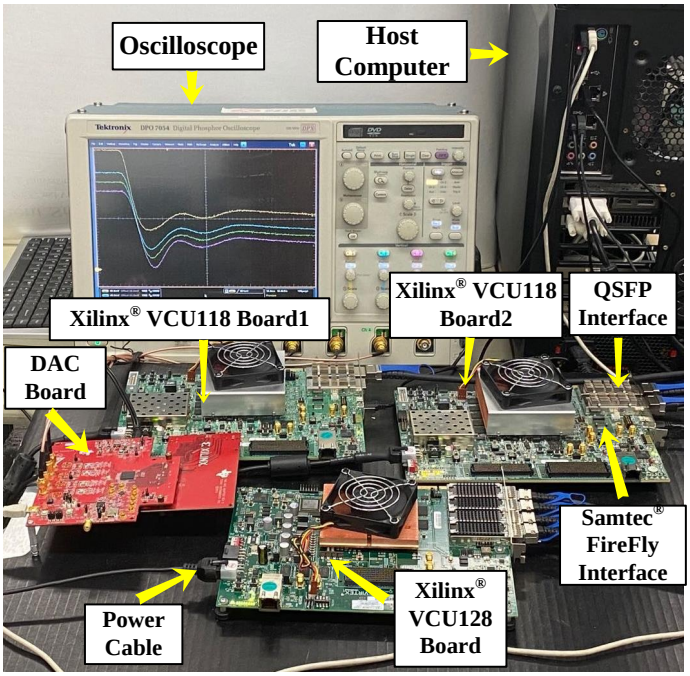

Figure 2.15: Hardware setup for FT-SCADA/RT emulation.

In the integrated AC-DC grid, each subsystem and function can be designed as a reconfigurable hardware module, and the HIL emulation is achieved following proper connection of these modules and deployment onto the FPGA boards. For the FT-SCADA/RT emulation, the initial conditions and the functions are downloaded from the host computer via the Joint Test Action Group (JTAG) interface. The current operating conditions could be emulated on the FTRT platform based on the signals it receives. Each module reserves one or several input data channels for receiving real-time data. If a disturbance occurs, the received current operating conditions will be sent to the relative subsystems, such as the dynamic power injection data will be delivered to *Ymatrix* module and the output mechanical torque of steam turbine will be calculated in the module which represents the synchronous generator. With the required real-time data of the gird and the emulation model downloaded from the host computer, the FTRT predictive regulation control can be realized.

The main challenge of emulating such a complex hybrid AC-DC grid is data communication among the three boards. A communication strategy among the FPGA boards should be properly designed. The communication delay has always been a time-consuming part of DSA systems. The Xilinx® Ultrascale+™ series FPGA board provides more efficient communication ports, such as Quad Small Form-factor Pluggable (QSFP) and Samtec® FireFly interfaces, for large data exchange with external devices or other FPGA boards. A maximum bidirectional data transmission speed of 4×28 *Gbps* provided by the dual QSFP cages accommodates delivering the current operating conditions from the real power trans-

mission system or other FPGA boards. The Samtec® FireFly connector provides up to 4×28 $Gbps$ full-duplex bandwidth in 4 channels and realizes data communication from an FPGA to an industry-standard multi-mode fiber optic cable, which can be used for optical data communication as well as support cable lengths up to $100m$.

The proposed interface strategy with less data transfer and the utilization of the QSFP interface will significantly shorten the communication delay. The VCU118 Board1 sends time-varying P and Q values calculated from the 4-terminal HVDC system to the VCU128 Board, and the instantaneous phase voltages are in turn delivered to VCU118 Board1 via the bidirectional QSFP interface, as given in Fig. 2.15. From each board's point of view, the P and Q values and the phase voltages are real-time measurements. In addition, the constantly updated P and Q values act as the inputs of the AC grid for calculating the admittance matrix, which can be treated as changing the network topology or dynamic conditions in every time-step.

Table 2.3: Specifics of major AC-DC grid hardware modules

Module	BRAM	DSP	FF	LUT	Latency
MMCCNT	0	54	5733	11085	85 T_{clk}
MMCAVM	16	208	8292	19277	90 T_{clk}
DCGrid	0	17	2209	2868	73 T_{clk}
PLL	0	8	892	1357	18 T_{clk}
YMatrix	12	1045	123388	126767	1470 T_{clk}
RK4	0	36	6970	7520	83 T_{clk}
AB5	0	98	12013	21077	135 T_{clk}
FTS	0	12	521	780	18 T_{clk}
Network	16	534	43928	57664	269 T_{clk}
Governor	0	17	3783	4598	29 T_{clk}
Update	0	38	4951	6875	33 T_{clk}
Total	44	4758	753450	848458	1873 T_{clk}
	1.02%	69.56%	31.87%	71.76%	–
XCVU9P	4320	6840	2364480	1182240	–

Table 2.3 gives the hardware resources and the latencies of major modules on the VCU118 Board1, where the *MMCCNT* refers to the control system of MMC stations, *MMCAVM* represents the functions of MMC average value model, and *DCGrid* denotes the network equations of the DC grid. The modules in the 4-T HVDC system can be calculated in parallel. The latency of the DC grid is 90 T_{clk}, meaning with an EMT emulation time-step of $200\mu s$, the FT-SCADA/RT ratio is over 222 times under an FPGA clock cycle of $10ns$. Meanwhile, the *YMatrix*, *RK4*, *Network*, *Governor*, and *Update* denote the components in IEEE 118-bus system, where *YMatrix* refers to the functions for calculating the admittance matrix, *RK4* is the non-linear differential equation solver, *Network* represents the AC network equations given in (2.27), and *Governor* is the governor control system of

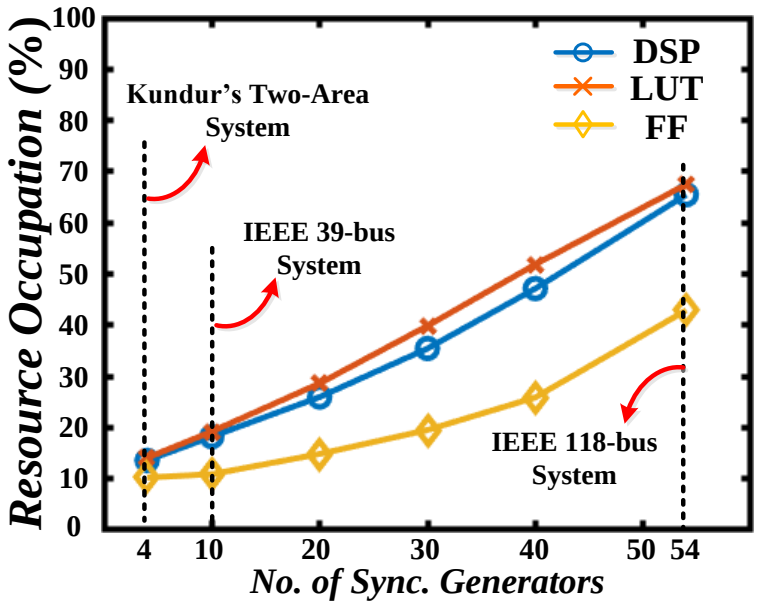

Figure 2.16: Relationship between hardware resources and synchronous generators.

synchronous generators. The proposed local equipment based flexible time-stepping algorithm is applied to the AC grids. The performances of the proposed flexible time-stepping are relative to the contingencies. For instance, a severe fault may lead to a long-term oscillation until the system retains to steady-state, and the proposed algorithm will operate in a small time-step for a long period. Therefore, the total time-steps are different under various disturbances.

Table 2.4 provides the FT-SCADA/RT ratio, and the total time-steps in the AC system under various conditions. Although a relatively small time-step is adopted during or after the fault, and a minimum FT-SCADA/RT ratio of 101 can be achieved by utilizing the proposed flexible time-stepping method. If the EMT emulation time-step is reduced to 50μs, the FT-SCADA/RT emulation can still be realized. However, the FT-SCADA/RT ratio could be highly dependent on the DC circuits, only 27 times faster than SCADA/real-time can be reached. Similarly, if the method of solving the DAEs switches to AB5 under a time-step of 1ms during or after the disturbance, the accuracy can be guaranteed. However, the latencies of AB5 increase to 135 clock cycles as given in Table 2.3, which are larger than RK4. To solve the DAEs during or after the occurrence of a fault, the RK4 is still chosen as the main method.

It is noticed that the hardware resources such as *DSP* and *LUT* are nearly full. The relationship between hardware resources and the number of synchronous generators is given in Fig. 2.16, where the synchronous machines are modeled in a set of 9^{th} order DAEs,

Table 2.4: Time-steps under various contingencies

Contingencies	Time-steps in proposed algorithm	Time-steps in fixed time-step of $1ms$
Load Change	14664	30000
3-Phase Fault	14478	30000
Outage	15967	30000
Hardware execution time of proposed algorithm	Emulation time span	FT-SCADA/RT ratio
274.56ms	30s	109.23
271.17ms	30s	110.63
296.18ms	30s	101.29

and each generator has a governor system. The governor is mainly responsible for providing mechanical power P_m (the same as T_m in per unit) to the synchronous generator. Meanwhile, the control of mechanical power is regulated by the steam turbine, which is a relatively slow process. The input of T_m in *RK4* is provided by the results of *Governor* from the previous time-step, and thereby *RK4* and *Governor* modules can be calculated in parallel. Taking the IEEE 118-bus system as an example, the DSP utilization can be calculated as $(36+17)\times 54+1045+534+38=4479$, where the 54 refers to the number of generators. The DSP utilization of *RK4* and *Governor* modules are proportional to the synchronous machines. The remaining modules are solved in series in a specific time-step, such as *YMatrix* and *Network*. The hardware resources of those modules are directly related to the bus numbers, which increases along with grid nodes. Therefore, the hardware resources are nearly proportional to the synchronous machines, and a single VCU118 FPGA board is able to accommodate about 70 synchronous generators in parallel.

2.2.6 FT-SCADA/RT Emulation Results and Validation

Various contingencies of the integrated AC-DC grid in Fig. 2.2 are emulated in the FT-SCADA/RT platform, and the results are validated by the off-line transient stability simulation tool TSAT® in the DSATools™ suite.

2.2.6.1 Three-Phase-to-Ground Fault

At the time of 5s, a three-phase-to-ground fault occurs at Bus 68 in *System 1*, as shown in Fig. 2.2. The impacts after the disturbance are severe to the AC system, including the generators' rotor angles, bus voltages, and the frequencies, as shown in Fig. 2.17. The synchronous generators lose synchronism after the ground fault as the relative rotor angles rise significantly as shown in Fig. 2.17 (a) and (b). Meanwhile, in Fig. 2.17 (c) and (d) the

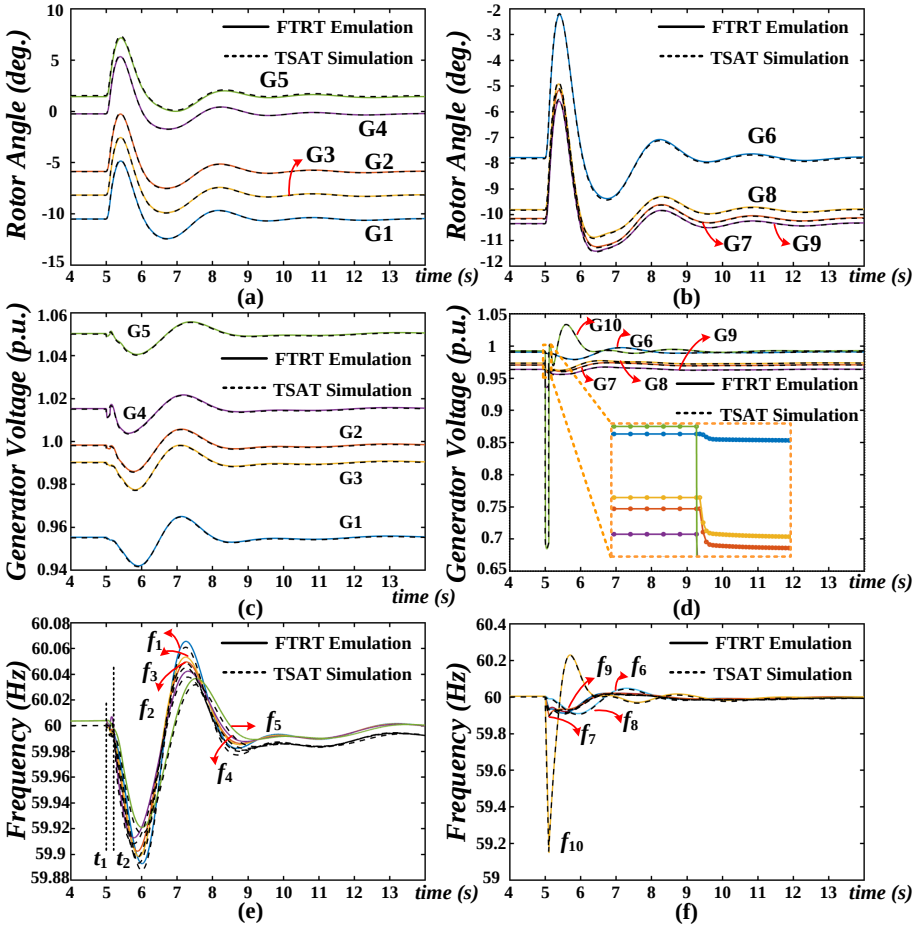

Figure 2.17: FT-SCADA/RT emulation using FTS algorithm for preview of generator behaviours under AC system ground fault: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

bus voltage of G5 decreases to $0.67p.u.$ in less than $0.1s$. The frequency of G10 plummets to $59.2Hz$ which is beyond the threshold of $\pm 1\%$ as shown in Fig. 2.17 (e) and (f). At t_2=$5.1s$, the three-phase-to-ground fault is cleared, and the system returns to the steady-state in about $5s$ as given in Fig. 2.17.

In a real power transmission system, a more than $100ms$ ground fault is unwanted in a power control center. The long-term ground fault may lead to generator damage or subsynchronous resonance in a series compensated transmission system. Therefore, the flexible time-stepping based FT-SCADA/RT emulation is applied to the control center to predict or mitigate the oscillations after a severe disturbance. The zoomed-in plots in Fig. 2.17 (d) and Fig. 2.20 (a) demonstrate that the time-steps shrink right after the bus voltages drop. At steady-state the time-step is $10ms$, once the fault occurs, the time-step reduces to the lower limit to maintain accuracy.

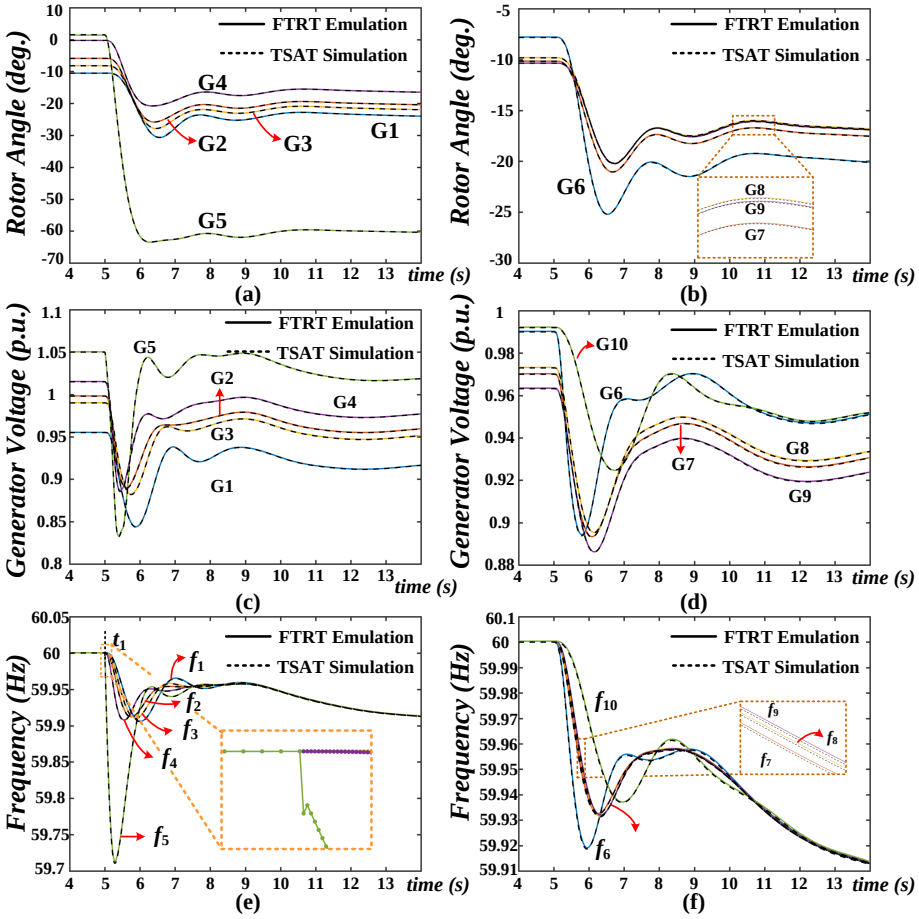

Figure 2.18: FT-SCADA/RT emulation using FTS algorithm for preview of AC-DC grid behaviours under generator outage: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

2.2.6.2 Generator Outage and Sudden Load Change

At the time of $5s$, the generator outage occurs at the generator G5. Fig. 2.18 shows the results of the rotor angles, generator voltages, and the frequencies before and after the contingency. The rotor angles of the generators decrease significantly after t_1, especially in G5, which is shown in Fig. 2.18 (a) and (b). Meanwhile, the generator voltages decrease to $0.83p.u.$ in less than $0.2s$ as shown in Fig. 2.18 (c) and (d). Due to the robustness in a large power transmission system, the generator voltages and rotor angles may transfer to a new steady-state. The main impact of the generator outage contingency is the divisions on the frequencies. Fig. 2.18 (e) and (f) present the frequencies drop to $59.7Hz$, which may cause the whole system to operate in a long-term unstable state. The zoomed-in plots in Fig. 2.18 (e) and Fig. 2.20 (b) illustrate the proposed flexible time-stepping algorithm can significantly change time-steps after the occurrence of a disturbance to ensure the emulation accuracy. Meanwhile, a relatively large time-step is applied to accelerate the emulation.

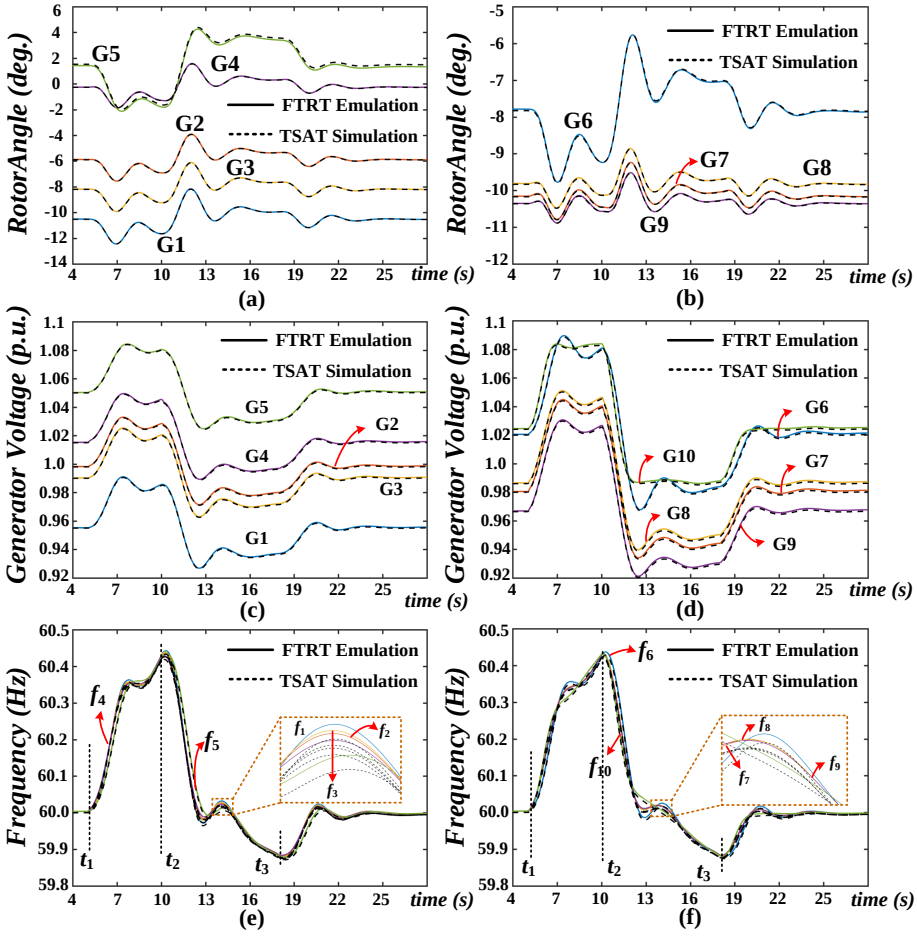

Figure 2.19: FT-SCADA/RT based predictive control for power system stability analysis: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

The sudden load change disturbance happens at the load Buses 25 and 54 in IEEE 118-bus *System 1*. At t_1=5.0s, a load of 200MW and 100MW are removed from Buses 25 and 54 respectively, causing the disturbance of the AC system which can not be restored even the loads are recovered at t_2=10s to its original capacity of 277MW and 184MW. The load change factor is relatively small in the large power transmission system, resulting in the slight changes in rotor angles and generator output voltages, as shown in Fig. 2.19 (a)-(d). However, the main impacts of the load change contingency are the frequencies, which reach the maximum allowed threshold of 1%. The power control center should select a proper strategy to mitigate the impacts after the load change. At t_2=10.0s, *MMC*3 and *MMC*4 deliver extra 100MW and 50MW active power to Buses 25 and 54 respectively from IEEE 118-bus *System 1* to *System 2*. At t_3=18.0s, the extra power injection is removed, and the whole system is therefore restored stable gradually in about 7s. As a result, the introduction of the HVDC system improves the stability of the integrated AC-DC

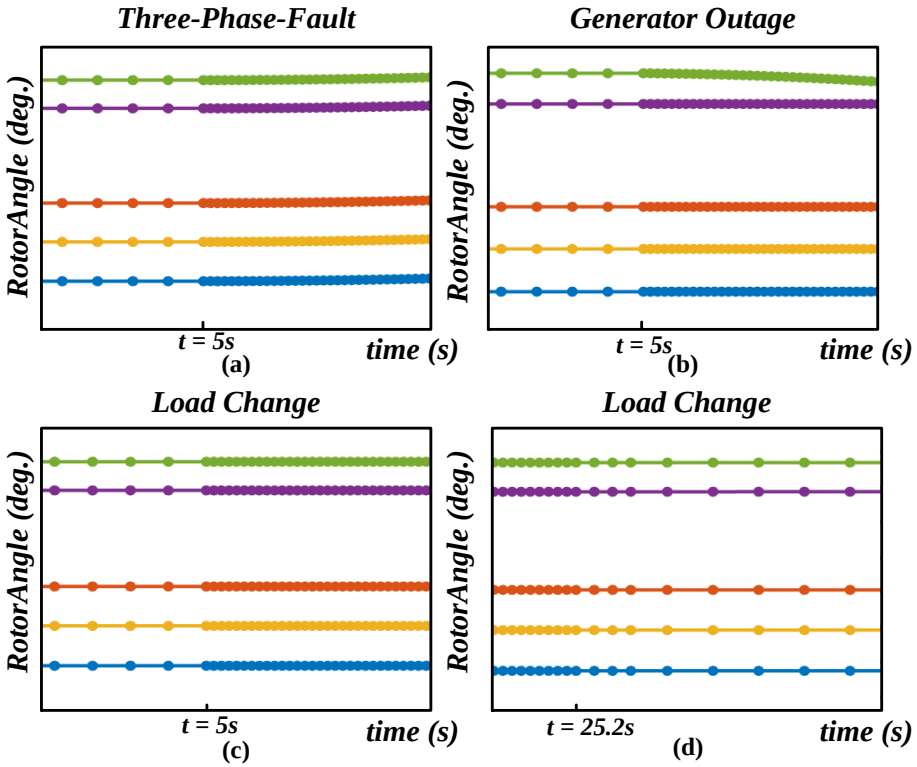

Figure 2.20: Zoomed-in plots of rotor angles for three contingencies: (a) three-phase-to-ground fault (G1-G5), (b) generator outage (G1-G5), (c), and (d) sudden load change (G1-G5).

grid by injecting active power into the AC grid or absorbing power from the AC system. The zoomed-in plots in Fig. 2.20 (c) demonstrate that the proposed flexible time-stepping reduced the time-step to the lower limit for higher accuracy, and the time-step increases gradually when the system restores to steady-state after the power injection, as shown in Fig. 2.20 (d).

2.2.6.3 AC-DC Interface Results and Error Analysis

As mentioned before, the HVDC stations denoted by *MMC1* to *MMC4*, regardless of the type, i.e., rectifier or inverter, can be modeled as time-varying P+jQ loads. The active power of each converter station in the 4-terminal HVDC between IEEE 118-bus *System 1* and *System 2* is given in Fig. 2.21.

Under steady-state, IEEE 118-bus *System 1* delivers $200MW$ and $100MW$ to *System 2* from Bus 25 and Bus 54, respectively. The dashed lines in Fig. 2.21 (a) and (b) refer to the received active power in the AC grid, in the meantime, dashed lines in Fig. 2.21 (c) and (d) represent the input bus voltages of the DC system. The solid lines in Fig. 2.21 (a)-(b) and (c)-(d) are the calculated active power and bus voltages in DC and AC grids, respectively. In the hardware emulation program, the DC part is calculated with the voltages and

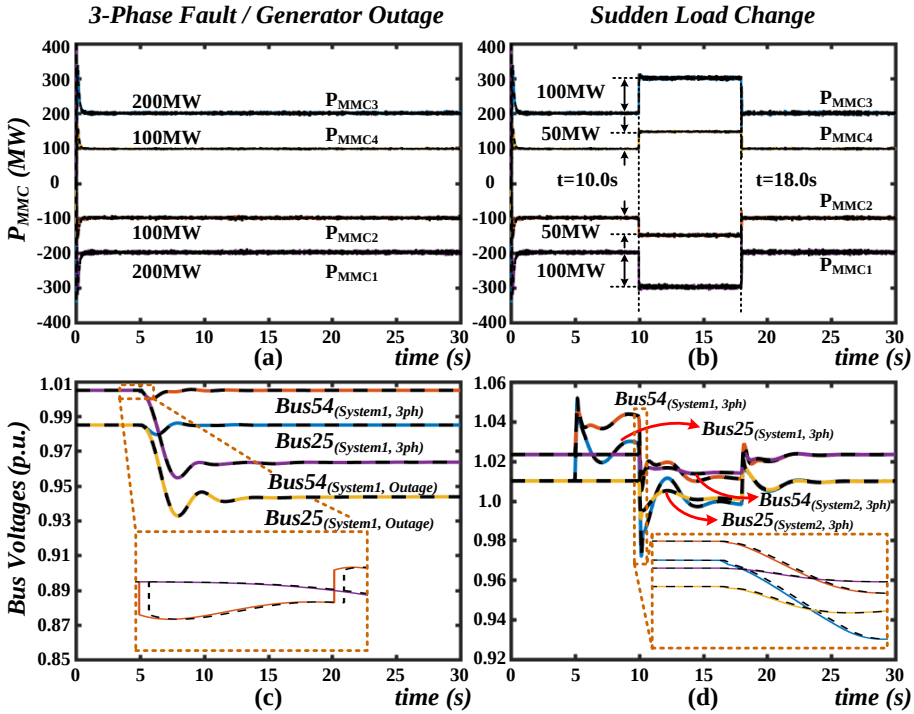

Figure 2.21: AC-DC grid interface results.

phase angles solved from the previous time-step in the AC system. The zoomed-in plots in Fig. 2.21 (c) and (d) indicate that the receiving bus voltages of the DC system are always lagging the calculated voltages in the AC grid by one time-step.

During the three-phase to ground fault and generator outage, the output power of IEEE 118-bus *System 1* remains stable, as given in Fig. 2.21 (a). The calculated interface bus voltages under the above two contingencies in *System 1* are provided in Fig. 2.21 (c). After the sudden load change occurs, with the 109 times faster than real-time ratio, the power control center has sufficient time to come up with an optimum solution that helps maintain the synchronism of the generators and select the proper power that should be delivered by the HVDC system as given in Fig. 2.21 (b). Meanwhile, Fig. 2.21 (d) provides the interface bus voltages calculated in the AC grid in both *System 1* and *System 2*. Since in Fig. 2.21 (a) and (b) the MMC stations undergo a dynamic process, the admittance matrix should be updated in every time-step to obtain practical emulation results.

In order to validate the accuracy and performance of the proposed method, Fig. 2.22 (a)-(c) provide the relative errors of the rotor angle in Generator 1 under various contingencies, where the relative errors are calculated by the following equation:

$$\epsilon = \frac{V_{Calculated} - V_{TSAT}}{V_{TSAT}} \times 100\%, \tag{2.51}$$

Fig. 2.22 (a)-(c) indicate that the maximum error appears when a serious contingency occurs. The maximum error among these three contingencies is merely 0.81%, which thor-

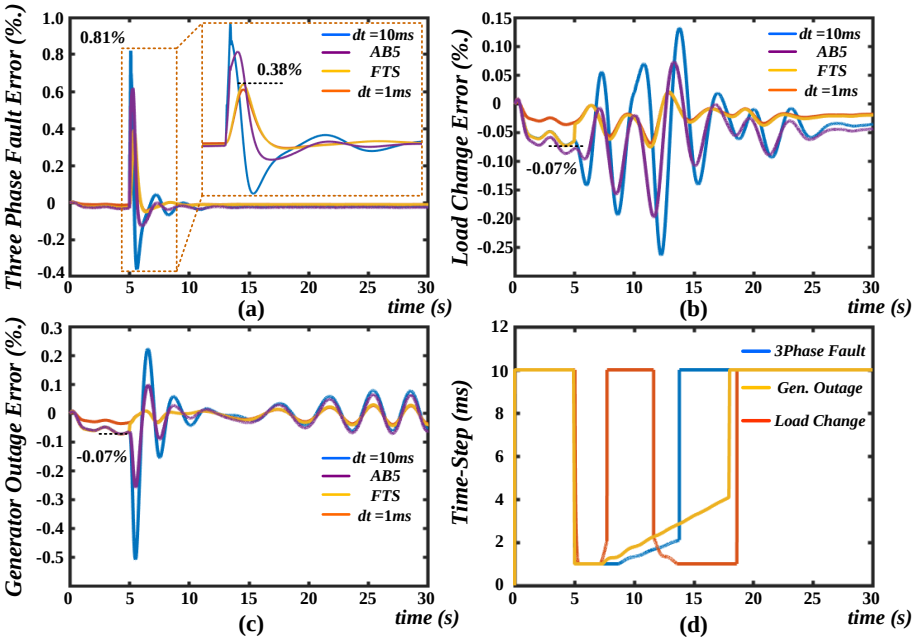

Figure 2.22: (a)-(c) Relative errors compared with TSAT under various contingencies, (d) time-steps under various contingencies.

oughly demonstrates the accuracy of the proposed method. Fig. 2.22 (d) provides the adaptive time-steps of the synchronous machine model during the emulation. It shows that the time-step will shrink after the occurrence of a serious disturbance. Furthermore, the updated time-step avoids being halved or doubled several times according to (2.49), which means the proposed flexible time-stepping method is able to find a proper time-step instantly compared with the traditional variable time-stepping strategy.

2.3 Summary

This chapter provided two methods to achieve the FTRT emulation for large-scale AC-DC grid. The proposed FGRA is iterative and is completely devoid of matrix operations; as such it is perfectly suited for mapping to the massively paralleled and pipelined hardware architecture of the FPGA. The emulated dynamic network model achieved a factor of 134 faster than real-time execution. The time-domain results from the case studies of integrated AC-DC methods demonstrate, in comparison with a commercial transient stability simulation tool, that the proposed algorithm is numerically stable and highly accurate in computing system states. Furthermore, the closed-loop HVDC grid control demonstrated the efficiency of the FTRT in predicting future system dynamic performance and taking effective control action to mitigate unforeseen contingencies with the potential to adversely impact grid stability. While the emulation of FGRA-based FTRT dynamic studies was carried out on a single Xilinx Virtex® UltraScale+™ XCVU9P FPGA, the proposed FGRA is

fully scalable for execution on multiple FPGAs interfaced with high speed data communication links.

Meanwhile, a novel local equipment based flexible time-stepping algorithm is also proposed for FTRT emulation of AC-DC grid, which is conducted on multiple FPGA boards. Compared with the traditional variable time-stepping methods, the proposed algorithm can significantly reduce the computational burden by utilizing large time-steps under steady-state and small time-steps during or after a disturbance. Traditional variable time-step algorithms need several stages to find the appropriate time-step; in contrast, the proposed FTS scheme can achieve this instantly, and thus helps to further reduce the computational burden. On the other hand, the parallel architecture of the hardware platform makes transient stability emulation more efficient than traditional CPU based simulators. With the minimum FT-SCADA/RT ratio of 101, the energy control center has sufficient time to select an optimal solution to maintain the system stable. The results of flexible time-stepping based FT-SCADA/RT dynamic emulation are highly matched with the off-line dynamic simulation tool TSAT®. Therefore, the FT-SCADA/RT emulation can help mitigate the adverse impacts after a serious disturbance rapidly, which ensures the stability of the complex power transmission system. When more system contingencies need to be considered, the FT-SCADA/RT platform can be applied to accelerate contingencies screening and ranking in dynamic security assessment systems.

3

Mitigation of Subsynchronous Oscillations in AC-DC Grid

The HVDC has seen significant inroads into modern power systems, for purposes such as economic long-distance electricity transmission, the connection of different grids with distinct frequencies, and renewable energy integration where a few DC stations are routinely linked by transmission lines to enable flexible power flow [2]. The formation of a complex network of the hybrid AC-DC grid as a result of the integration of intermittent renewable energies such as the wind farm makes it more challenging to maintain a stable power system operating safely [129], considering that in such an interactive network any unexpected contingency in a small region will soon spread to other areas via various paths while during the process its severity may also increase.

Transmission line capacity enhancement by series compensation is commonly used in power systems, which consequently faces potential subsynchronous interaction (SSI). In this chapter, FTRT simulation based on the field-programmable gate arrays is proposed to mitigate the disastrous SSI in a hybrid AC-DC grid integrated with wind farms. Dynamic simulation is applied to the AC system to gain a high speedup over real-time, and a detailed multi-mass model is specifically introduced to the synchronous generator to show the electrical-mechanical interaction. Meanwhile, the DC grid undergoes electromagnetic transient simulation to reflect the impact of power converters' control on the overall grid, and consequently, the EMT-dynamic co-simulation running concurrently due to FPGA's hardware parallelism is formed.

Furthermore, less restricted by geographical conditions and higher flexibility in terms of installation compared with other forms of renewable energies, the solar power system is deemed as one of the most effective solutions to the environmental problem and energy crisis [130–132]. Although the integration of photovoltaic (PV) generation sys-

tems eases energy demand on the modern power system, their connection to the utility network can lead to grid instability or even failure, if the converters are not properly controlled [133, 134]. Traditionally, the transient stability simulation for SSCI analysis is conducted on the CPU-based off-line simulators, such as PSS®/e, PowerWorld®, and DSATools™/TSAT®. However, the CPU-based simulation is implemented sequentially, which is insufficient for real-time control in the energy control center. The reconfigurability of FPGA enables the power system components running in parallel to realize real-time or even FTRT emulation [135,136]. With the hardware emulation, the energy control center may have sufficient time to select an optimal solution for mitigating the SSCI in PV farm.

In this chapter, a hardware-based FTRT emulation is proposed for damping SSCI in PV farms. The integrated voltage source converter (VSC) and PV plant can be treated as a PV-STATCOM, which can realize dynamic active/reactive power control. Therefore, the power injection method for mitigating the SSCI in PV farm is utilized. As mentioned, the SSCI may induce serious damage to the power system. An extremely fast time-domain emulation platform is required to determine the proper power injection values to mitigate the oscillations.

3.1 Mitigation of Subsynchronous Interactions in Hybrid AC-DC Grid

3.1.1 Multi-Mass Torsional Shaft Model

Although the detailed electrical circuits and the mechanical equations of a synchronous generator are given above, in reality, the mechanical part is driven by a steam turbine in conjunction with a governor system. In this paper, we apply a five-mass torsional shaft system composed of the four-mass-turbine shaft connecting with the generator rotating shaft to the dynamic simulation, as shown in Fig. 3.1, where δ_n means the relative rotor angle of each turbine, and specifically, δ_1 is the generator rotor angle. K_{45} presents the stiffness coefficient between $Mass5$ and $Mass4$, so as to K_{34}, K_{23}, and K_{12}. D_n and H_n refer to the damping factor and inertia constant of each torsional shaft, respectively.

Therefore, the set of mechanical equations for the multi-mass torsional shaft model can be written as [139]:

$$\dot{\delta_1} = \omega_R \cdot \Delta\omega_1, \tag{3.1}$$

$$\Delta\dot{\omega}_1 = \frac{1}{2H_1}[K_{12}(\delta_2 - \delta_1) - T_e - D_1 \cdot \Delta\omega_1], \tag{3.2}$$

$$\dot{\delta_n} = \omega_R \cdot \Delta\omega_n, \tag{3.3}$$

$$\Delta\dot{\omega}_n = \frac{[T_n + K_n^{n+1}(\delta_{n+1} - \delta_n) - K_{n-1}^{n}(\delta_n - \delta_{n-1}) - D_n\Delta\omega_n]}{2H_n}, \tag{3.4}$$

$$\dot{\delta_5} = \omega_R \cdot \Delta\omega_5, \tag{3.5}$$

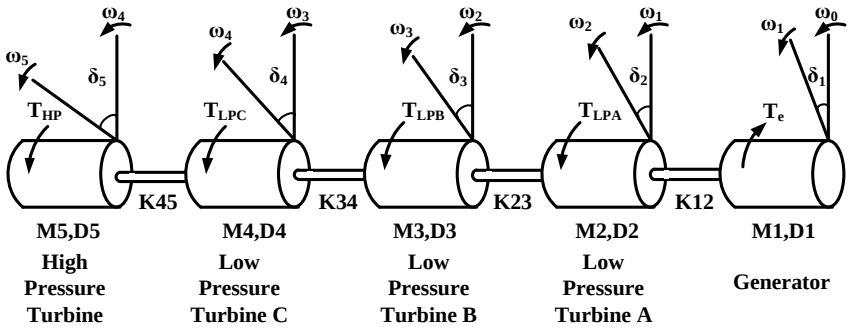

Figure 3.1: Five-Mass torsional shaft system.

$$\Delta\dot{\omega}_5 = \frac{1}{2H_1}[T_5 - K_{45}(\delta_5 - \delta_4) - D_5 \cdot \Delta\omega_5], \tag{3.6}$$

where the subscript n in (3.3) and (3.4) refers to $Mass2$-4, and variables with subscript 1 constitute the mechanical functions of the generator shaft. T_1, T_5, and T_n are the mechanical torque of each steam turbine. Therefore, the five masses Turbine-Generator (T-G) shaft has five modes of torsional oscillation frequencies that typically range from 10 to 35 Hz.

3.1.2 Torsional Interaction

Take the IEEE First Benchmark Model (FBM) in Fig. 3.2 for example, the torsional oscillation frequencies can be calculated by eigenvalues and verified from fast Fourier transform (FFT) analysis. Fig. 3.2 shows the topology of FBM in Matlab/Simulink®, which contains two steam-turbine shafts and one generator shaft. Therefore, the three-mass shaft model has three pairs of eigenvalues theoretically. Meanwhile, the eigenvalue analysis can be obtained from the linearized state-space form of (3.1)-(3.4). However, there is an input T_e in (3.4) which should be related to the state variables. For a small disturbance, the electromagnetic torque deviation is proportional to the generator rotor angle deviation, which can be expressed as $\Delta T_e = K_s \cdot \Delta\delta_1$, where K_s is the synchronizing torque coefficient [36,49,140]. The linearized state-space equations can be expressed by the following function:

$$\begin{bmatrix} \Delta\dot{\omega}_n \\ \Delta\dot{\delta}_n \end{bmatrix} = \mathbf{A} \cdot \begin{bmatrix} \Delta\omega_n \\ \Delta\delta_n \end{bmatrix}, \tag{3.7}$$

where $\mathbf{A}$ refers to the state-space matrix, which, for a specific system, is generated from the constant parameters H_n, D_n, K_n, and K_s. Therefore, the state matrix is constant and the eigenvalues can be obtained, along with the FFT analysis results, as listed in Table 3.1.

The results of FFT analysis come from a three-phase to ground fault at the high voltage side of the transformer, as shown in Fig. 3.2. As mentioned above, a disturbance in a series compensated transmission system may excite transient power oscillations at subsynchronous frequencies which are mainly dependent on the degree of line compensation,

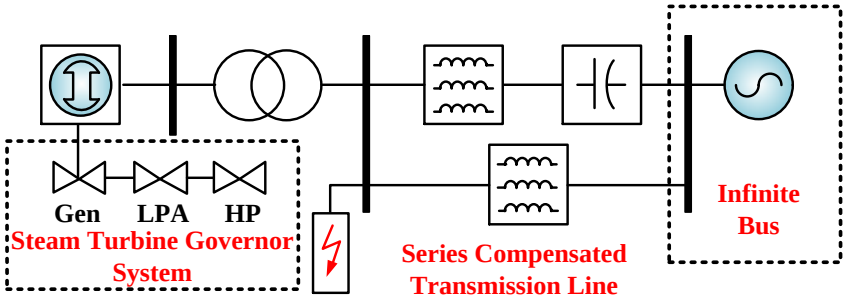

Figure 3.2: IEEE First Benchmark Test System.

Table 3.1: Torsional Oscillation Frequencies and FFT Analysis

Eigenvalues	Frequency (Hz)	Torsional Mode
-0.4971743430807 $\pm$ 226.0003376339336i	35.9691	3
-0.3627485375639 $\pm$ 162.5259229903647i	25.8668	2
-0.3943003150324 $\pm$ 11.3366105040643i	1.8043	1

Frequency (Hz)	Percentage (%)	Frequency (Hz)	Percentage (%)
24	1.16	40	2.29
28	1.49	44	1.44
32	2.13	48	1.31
36	4.91	60	100.00

e.g., 55% in this FBM. As Table 3.1 shows, the subsynchronous resonance after the three-phase fault is $36Hz$ from FFT analysis which is almost the same as one of the natural frequencies ($35.9691Hz$) from eigenvalue analysis.

3.1.3 Hybrid AC-DC Grid Modeling

3.1.3.1 Numerical Method for AC System Simulation

Traditional dynamic simulation of a single-mass synchronous generator model contains 9^{th} order differential equations, which can be solved by Newton-Raphson or other iterative methods. However, a higher order differential equations may lead to more iterations in every single time-step; Furthermore, the iterative method is entirely sequential which is time consuming in FTRT emulation. Since the multi-mass torsional shaft model includes 17 state variables, the iterative methods are inappropriate for hardware design. Therefore, the 4^{th}-order Runge-Kutta (RK4) method is applied to solve the nonlinear differential equations of synchronous generators.

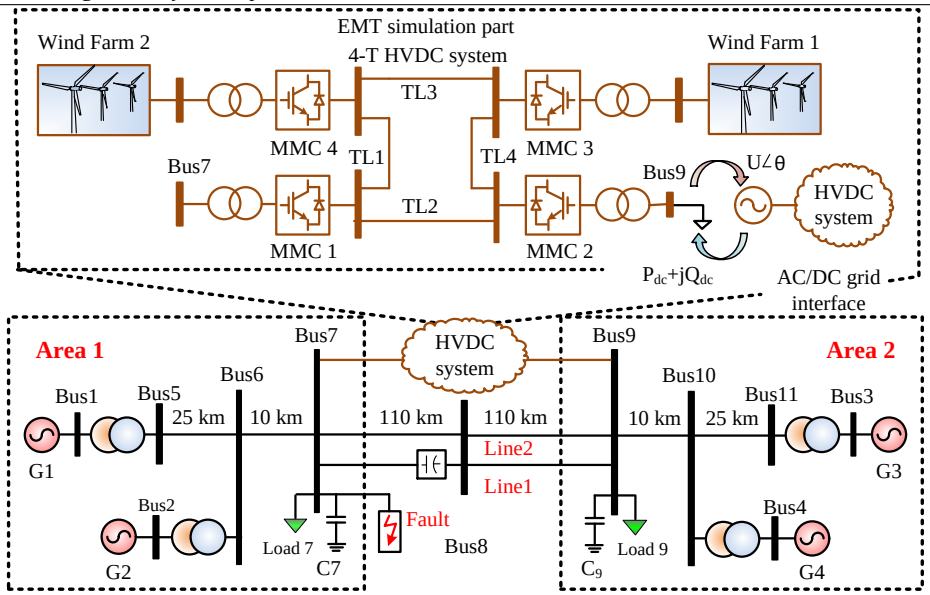

Figure 3.3: Topology of hybrid AC-DC grid.

3.1.3.2 MMC AVM for Power Flow Analysis

The FTRT simulation prefers models that induce the least computational burden whilst ensuring sufficient accuracy, and adopting the average value model (AVM) for a modular multilevel converter (MMC) [123, 124] is justified by the type of study, where power flow, instead of converter details, is the main concern. Compared with its detailed counterpart [122], the hardware latency of AVM is much lower, while it retains the capability to provide power flow under the influence of a controller. The MMC provides a stable voltage on the AC side to the wind farm composing of a number of wind turbines, whose output power takes the form of

$$P_{WT} = \frac{1}{2}\rho\pi R^2 v_w^3 C_p, \tag{3.8}$$

where ρ means the air density, R the wind turbine radius, v_w the wind speed, and C_p indicates the wind turbine's capability of converting kinetic energy into mechanical energy [141]. In the wind farm, some wind turbines are operating while the others remain standby in order to maintain a stable power system. Therefore, the total output power of a wind farm can be roughly regulated by either changing the power command or adjusting the number of wind turbines in service.

3.1.3.3 AC-DC Grid Interface

The topology of a hybrid AC-DC grid is shown in Fig. 3.3, where the two-area system connects with the 4-terminal HVDC via Bus 7 and Bus 9. Meanwhile, MMC 1 and MMC 2 operate as inverter stations, and the remaining two terminals connected with two individual wind farms act as rectifier stations. The two areas are connected by two parallel

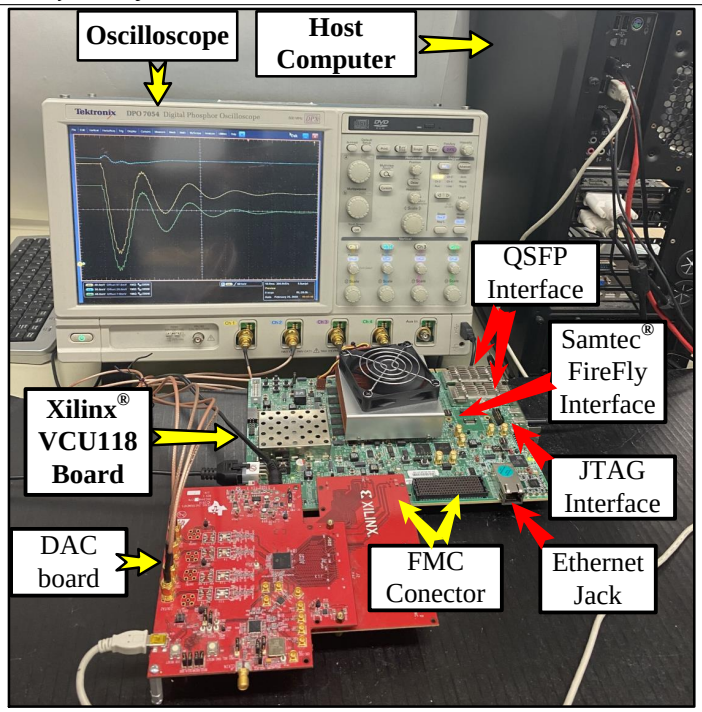

Figure 3.4: Hardware design scheme of hybrid AC-DC grid.

transmission lines, in which *Line* 1 has a series compensator and the compensated factor is 80%, and *Line* 2 is a traditional π model transmission line. To reveal the dynamic process of the HVDC system, a time-step of 200μs is adopted in the EMT simulation. However, the two-area Kundur's system undergoing the stability analysis has a time-step of 3ms, which is 15 times larger. Therefore, in order to establish an integrated co-simulation time-step scheme, the DC system should send data to the AC grid in every 15 time steps. Moreover, to keep the accuracy, an updated admittance matrix of the AC network should be solved in every time-step.

3.1.4 Hardware Emulation on FPGA

The embedded FTRT algorithm is implemented on the Xilinx Virtex® UltraScale+™ XCVU9P FPGA board which features 1182240 look-up tables (LUTs), 2364480 flip-flops (FFs), 6840 DSP slices, and a maximum transceiver speed of 32.75 Gb/s. Fig. 3.4 shows the hardware setup used in this work. The highly parallel hardware architecture of the FPGA greatly shortens the latency induced by mathematical operations and thus enables conducting the real-time as well as FTRT emulation of a variety of converter-integrated power systems. The Xilinx® HLS tool which enables VHDL code auto-generation ensures reliable delivery of hardware design in addition to being able to significantly shorten the design stage, and therefore, it was adopted [12]. Then, Xilinx® Vivado can synthesize the generated IP package from the HLS tool into the overall hardware design. In a practical power system,

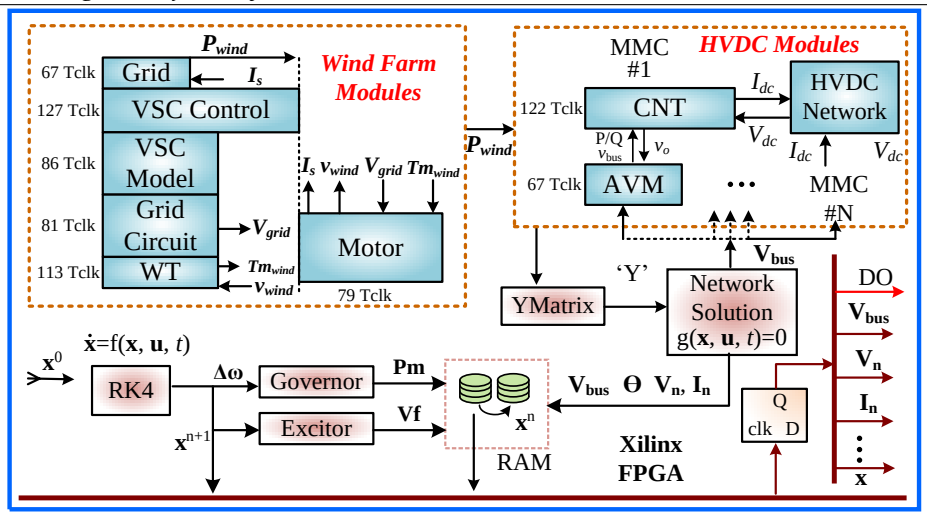

Figure 3.5: Hardware design scheme of hybrid AC-DC grid.

the Joint Test Action Group (JTAG) and the Universal Asynchronous Receiver Transmitter (UART) interfaces enable the interconnection of host computer and the FPGA board. With an in-circuit-emulator, in-circuit-debug, and in-system-program capability, the JTAG connector can be utilized for hardware-in-loop (HIL) simulation of the desired power system. The UART, on the other hand, is a general-purpose serial data bus, which can write and debug programs to the device. Meanwhile, the data from the real power transmission system is delivered to the FPGA board running a virtual grid via Samtec® FireFly connector, Quad Small Form-factor Pluggable (QSFP) interface or Ethernet connector. The dual-QSFP cages are a bidirectional communication and networking interface, which has a maximum transmission speed of up to 4×28 $Gbps$. Therefore, they are mainly used for communication among FPGAs. The FireFly connector from Samtec® provides up to 4×28 $Gbps$ full-duplex bandwidth in 4 channels from an FPGA to an industry-standard multi-mode fiber optic cable, which can be used for optical data communication as well as support cable lengths up to 100 m. The traditional Ethernet port can be applied as a backup since it can only reach a maximum speed of 1000 $Mbps$. Hence, with a significant reduction in communication delay, the QSFP and Samtec® FireFly interfaces are suitable for data exchange with external devices or other FPGA devices. Then, the grid status data is transmitted to the corresponding FTRT-algorithm-embedded FPGA in the control center where the optimal solution to the system contingency is emulated prior to mitigating and eliminating the hazardous impact by the actual equipment.

Fig. 3.5 shows the mechanism of the hardware design strategy for the hybrid AC-DC grid, where blocks grouped together refer to the EMT simulation of the wind farm as well as the 4-terminal HVDC grid. The modules inside the wind farm can be solved in parallel using pipeline design, albeit the *Grid Circuit* provides the mechanical torque to *Motor*. Theoretically, both the wind farm and the HVDC should calculate 15 times before

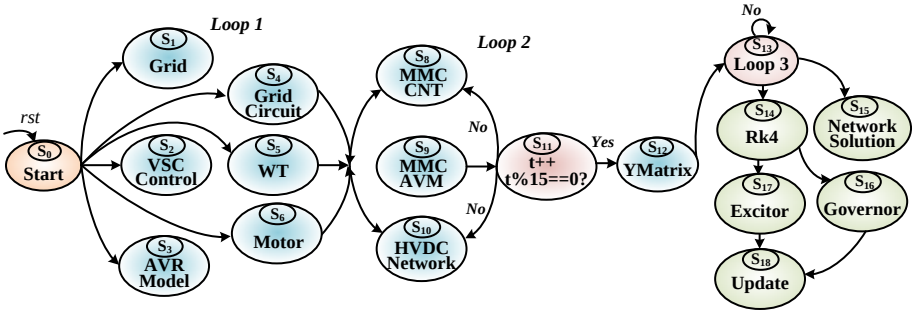

Figure 3.6: Top-level finite state machine for the hardware modules.

synchronization with the AC grid. However, the wind farm power is nearly constant in 15 time-steps, which is $3ms$. Considering the EMT simulation will diverge as long as the time-step is larger than $200\mu s$, the wind speed remains unchanged in a duration of $3ms$ in order to keep convergence and improve the simulation efficiency. Therefore, the virtual time-step for the wind farm is treated as $3ms$.

The HVDC grid is comprised of three modules, where the *CNT*, *AVM*, and the HVDC network can be pipelined and computed concurrently. As the dynamic simulation needs the power supply from the DC grid, the module *YMatrix* receives instantaneous P and Q value to calculate the new admittance matrix. Then, the dynamic simulation comes to AC modules, where only *Governor* and *Excitor* can be solved in parallel. Once the dynamic simulation completes in one time-step, the AC bus voltage provides U and θ to the DC grid. Meanwhile, the results of the co-simulation can be displayed on the oscilloscope.

As has been mentioned, the time-step of EMT simulation is much smaller than that of its dynamic counterpart, therefore a top-level finite state machine (FSM) should be generated, as shown in Fig. 3.6, to maintain a proper sequence of each hardware module. In a specific power transmission system, the data is delivered to the FPGA board through the QSFP interface. The emulation starts once the data is successfully received, $Loop$ 1 refers to the wind farm EMT simulation, where all the modules are solved concurrently. The fact that the HVDC grid utilizes $200\mu s$ as the time-step means that the DC grid should be computed 15 times more frequent than the AC side. Afterward, the new admittance matrix can be obtained in *YMatrix*. In $Loop$ 3, the nonlinear differential equations are solved in $RK4$, which targets the control systems of the synchronous generator, followed by the network equations. The results of control systems will be applied in the next time-step. Table 3.2 is a summary of hardware design specifics, where the latency is defined in clock cycles and the main hardware resource utilization is listed. Due to parallelism, the wind farm latency is deemed as 127 T_{clk}, and thus, its FTRT ratio reaches over $\frac{200\mu s}{127 \cdot 10ns} \approx 157$. Similarly, the *MMCAVM*, *MMCCNT*, and *HVDCNetwork* are fully parallelized, and among them, the largest latency is 122 T_{clk}, under an FPGA clock frequency of $10ns$, the FTRT ratio is calculated as $\frac{200\mu s}{122 \cdot 10ns} \approx 164$. In the meantime, the dynamic simulation has a total latency calculated

Table 3.2: Specifics of major AC-DC grid hardware modules

Module	Latency	BRAM	DSP	FF	LUT
Grid	67 T_{clk}	24	338	9672	22574
VSCcontrol	127 T_{clk}	20	240	18825	40046
VSCmodel	86 T_{clk}	0	38	3454	3752
Gridcircuit	81 T_{clk}	0	7	1475	2169
WT	113 T_{clk}	0	43	5085	8929
Motor	79 T_{clk}	0	66	5128	9219
MMCAVM	67 T_{clk}	0	24	6637	10604
MMCCNT	122 T_{clk}	0	68	7406	13526
HVDCNetwork	107 T_{clk}	0	20	2958	4098
Ymatrix	1470 T_{clk}	6	1106	133972	129108
RK4	199 T_{clk}	16	315	29709	45721
Network	269 T_{clk}	16	534	43928	57664
Excitor	29 T_{clk}	0	17	3783	6598
Governor	188 T_{clk}	0	22	6105	10666
Update	33 T_{clk}	0	38	4951	6875
Total	4174 T_{clk}	82	2876	283079	371549
	–	1.90%	42.05%	11.97%	31.43%
XCVU9P	–	4320	6840	2364480	1182240

by $1479 + 199 + 269 + 188 + 33 = 2138\ T_{clk}$, which is $\frac{3ms}{2138 \cdot 10ns} \approx 138$ times faster than real-time. Although the EMT simulation has a higher FTRT ratio, in hardware design, the EMT simulation should wait for the AC grid to complete in order to keep synchronization, meaning the total FTRT ratio is about 138.

It is noted that the *Ymatrix* module has the largest latency among other modules. For the testing system, the converter stations are treated as the time-varying complex power P+jQ. The main task of *Ymatix* module is calculating the admittance matrix. Although this module performs calculation in every time-step, the only changes are the components at the PCC in the admittance matrix (**Y**). In this case, to reveal the dynamic process of MMCs, the element $Y(7,7)$ and $Y(9,9)$ in the admittance matrix should be resolved in every time-step. Since the transmission line or the fixed shunt capacitors remain stable in a specific power transmission system, the latency of the *Ymatrix* module will not increase with the system size, it only related to the interfaces between the HVDC part and the AC system. Similarly, due to the fact that network equations and DAEs of each synchronous machine can be solved in parallel, the increase of the generators challenges the hardware resources rather than the latency. For example, the Ultrascale+ FPGA VCU118 evaluation board can accommodate large systems such as the IEEE 39-bus system with a maximum hardware resource utilization of 73.3%, and the same latency as in the Kundur's two-area case. As a result, the FTRT ratio can be maintained even though the AC system expands. Moreover, the hardware resource burden can be alleviated by interconnecting multiple FPGA boards when the AC-DC system is enlarged, or with a sufficient FTRT ratio, a trade-off can be

made between simulation speed and hardware resources without adding another FPGA board.

3.1.5 Hardware Emulation Results and Validation

3.1.5.1 Eigenvalue Analysis

In the proposed AC-DC hybrid simulation, each synchronous machine has a five-mass shaft, whose model corresponds to five pairs of eigenvalues. The eigenvalue analysis results and the FFT analysis are given in Table 3.3, based on a three-phase to ground fault on Bus 7, where the fault period is 90 ms. Due to the aforementioned series capacitor compensation between Bus 7 and Bus 9, a major contingency like the fault may cause the instantaneous power oscillations in the AC system. Furthermore, if the electrical oscillation frequency is close to or the same as one of the shaft natural frequencies, the torsional interaction will occur. As Table 3.3 shows, the subsynchronous resonance frequency after the three-phase to ground fault is about 27Hz from the FFT analysis results, which is matched with one of the natural frequencies, i.e., 26.587Hz.

Table 3.3: Eigenvalue Analysis of Five-Mass Torsional Shaft and FFT Analysis

Eigenvalues	Frequency (Hz)	Torsional Mode
-0.0617913744225 $\pm$ 777.4154871513625i	123.730	5
-0.0398957979074 $\pm$ 280.1332882191073i	44.585	4
-0.0812398973282 $\pm$ 167.0512211097699i	**26.587(≈27)**	3
-0.0348365892891 $\pm$ 83.7505682682303i	13.329	2
-0.0584038300879 $\pm$ 9.7600253406880i	1.553	1

Frequency (Hz)	Percentage (%)	Frequency (Hz)	Percentage (%)
18	1.17	**27**	2.98
21	1.48	33	0.89
24	2.72	36	0.70

3.1.5.2 Case 1: Three-Phase-to-Ground Fault

The three-phase-to-ground fault test is based on the system configuration in Fig. 2.6, which is a combination of the two-area system and a four-terminal HVDC grid connecting with offshore wind farms. Under steady-state, the HVDC link between Bus 7 and Bus 9 delivers 100MW from Area 1 to Area 2 via the DC transmission line TL 2 whilst the total transmitted power of the other two links, i.e., the compensated *Line* 1 and the uncompensated *Line* 2, is 300MW, which means that Area 2 has a net power inflow of 400MW. At the time of 3.0s, a three-phase ground fault takes place at Bus 7 with a duration of 90ms. When the fault encounters, the transmission power of the HVDC system remains stable at 100MW while *Line* 1 and *Line* 2 are considered to connect to the power grid all the time. As a result,

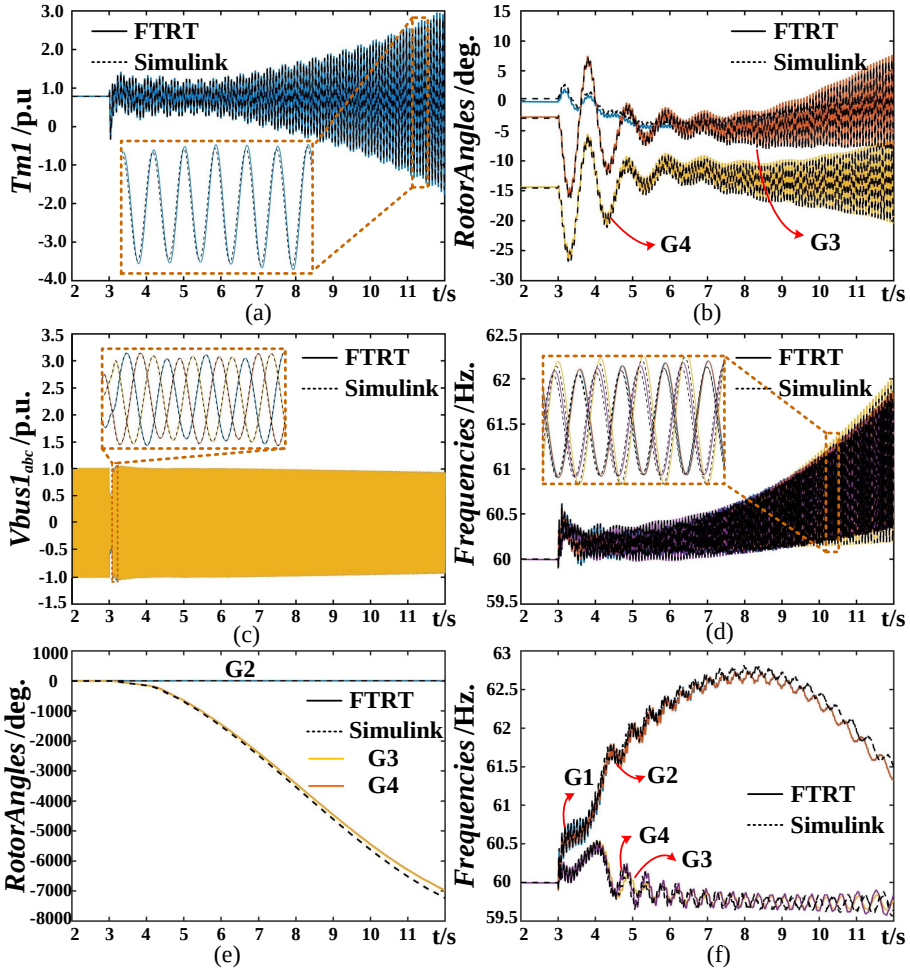

Figure 3.7: Torsional interaction phenomenon under FTRT co-simulation: (a) Mechanical torque of generator 1, (b) relative rotor angles, (c) three-phase voltage of Bus 1, (d) generator frequencies, (e) relative rotor angles after remove the compensated line, and (f) frequencies after remove the compensated line.

in Fig. 3.7 (a), the torque experiences a drastic oscillation that keeps amplifying during the process and at the time of 12s, it reaches approximately 3.0 p.u. Consequently, the rotor angles, as that of $G3$ and $G4$ given in Fig. 3.7 (b) for instance, are no longer stable. In the meantime, the envelope of three-phase generator terminal voltage starts to oscillate and introduces a noticeable SSR phenomenon, shown in Fig. 3.7 (c)-(d). In Fig. 3.7 (e)-(f), the investigation of cutting off the compensated line (*Line* 1) is conducted at the time of 3.09s with the same grid topology. As a result, the rotor angle decreases enormously to -8000 p.u. and loses synchrony while its frequency can not maintain at the same level as prior to the fault. Thus, it is proposed that the HVDC transmission system should play the role of delivering more power to alleviate the burden of Line 2. The FTRT emulation results match up with that of the Simulink accurately in Fig. 3.7 which proves the correctness of proposed modeling and hardware implementation methods and the AC grid dynamic

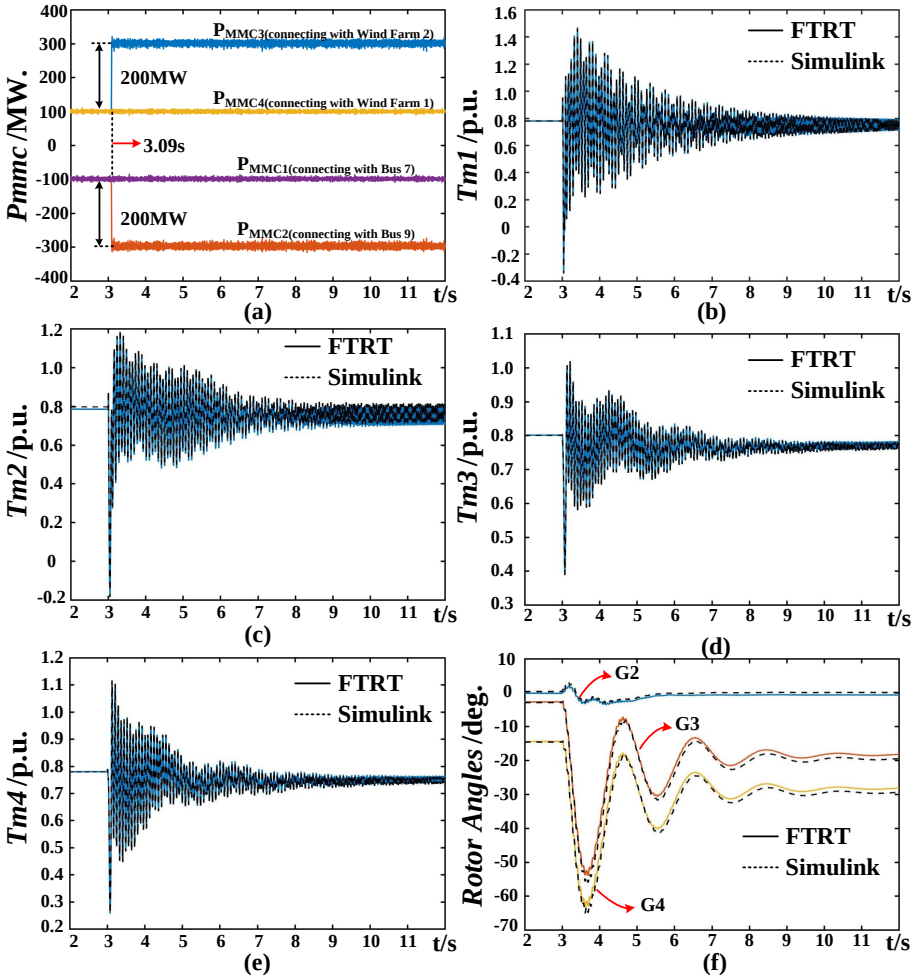

Figure 3.8: The results of power injection for mitigation the torsional interaction: (a), (b) , (c) and (d) Mechanical torques, (e) relative rotor angles compared with generator 1, (f) active power resulting from FTRT co-simulation

simulation part is as accurate as the EMT simulation in Matlab/Simulink® following the introduction of the multi-mass model.

1) Mitigation Strategies:

The mitigation of SSR can be conducted in two ways: 1) Install a Flexible AC Transmission Systems (FACTS) device to dynamically change the series compensation factor; 2) Change of the transmission grid configuration by utilizing the bypass topology. In this work, the second one is employed to reduce the burden of *Line* 2. In Fig. 3.8 (a), it shows the remedial effect of cutting off *Line* 1 and increasing the HVDC transmission power from $100MW$ to $300MW$. The oscillating torques of four generators in the two-area system steadily converge to the static operation value, as given in Fig. 3.8(b)-(e) while the rotor angle in Fig. 3.8(f) can be synchronized at the new static state eventually. Hence, it is reasonable to apply such a strategy to mitigate the SSR phenomenon in this case where the emulation results in concrete lines are also highly consistent with the Simulink® simulation

results drawn in dashed lines.

In a practical power system, once a serious contingency occurs and is detected, the peripheral devices would deliver the recorded data to the FPGA boards running a virtual grid via Samtec® FireFly connector or QSFP interface. In the control center, there could be a number of FTRT hardware platforms running the scenario with various potential solutions simultaneously and then they come up with an optimum one that helps maintain the synchronism of the generators and mitigate the torsional oscillation. Scanning the power that should be delivered by the HVDC is performed. In addition, other control actions and the consequent system response could also be simulated on several FPGA boards in the control center. Nevertheless, as power scanning is sufficient to demonstrate how FTRT is developed and used to maintain a stable system, those additional control strategies requiring multiple FPGA boards are not carried out in this work. Instead, only the effective solution is given, since other control actions that are unable to stabilize the system will be automatically bypassed and not implemented. With a sufficient response margin over real-time, the control center would have enough time to deal with the contingencies as well as make an optimal decision.

2) FTRT Justification:

The fact that the electro-mechanical phenomenon lasts dozens of seconds or even longer justifies the feasibility of using FTRT for the power system stability maintenance. Once the signals are delivered to the control center after some delay, the FPGA based emulator can study the system and give proper strategies and quantified regulations instantly, whilst the electro-mechanical oscillation is still at its initial stage. So, a high FTRT ratio leaves the control center sufficient time to maintain a stable system.

Therefore, the difference between FTRT and real-time simulation is significant, as the latter type of simulation would never be able to catch up with the real system when the communication delay is taken into account since they are synchronized in the time axis, let alone giving predictive system results to stabilize the power system. In stark contrast, with a dramatic 138 times faster than real-time and an electro-mechanical process lasting much longer than the communication latency, the FTRT simulation can make up for the delay and consequently give the proper strategy in advance for the real system to follow to mitigate the SSI.

3.1.5.3 Case 2: Long-Term Overload

In Case 2, both MMC 3 and MMC 4 respectively transmits $100MW$ power to the two-area system under steady-state. A $200MW$ overload on Bus 9 is simulated at t=3.0s. In Fig. 3.9 (a)-(b), the torsional interaction can be observed for all four generators with a grid configuration given in Fig. 3.3. Under this circumstance, the compensated *Line* 1 induces the electrical oscillation on the grid side and the torsional interaction on the mechanical side of the generators. Cutting off the compensated line (*Line* 1) when the grid side experiences

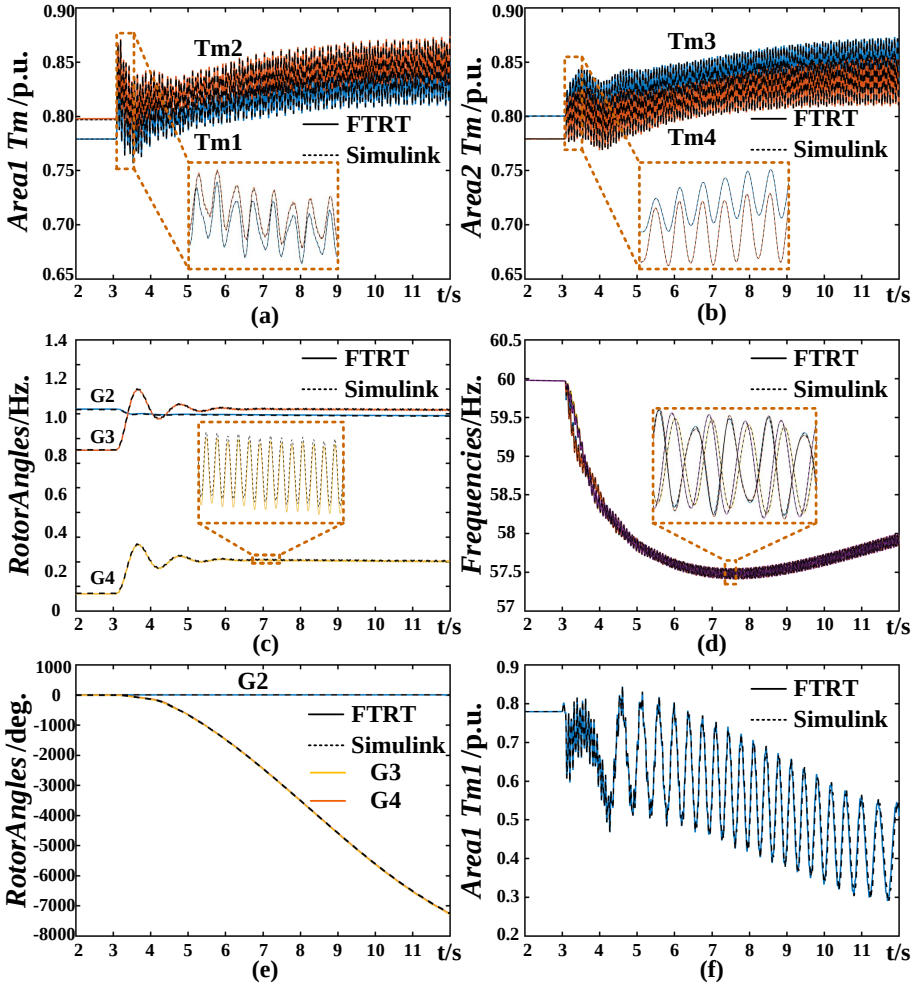

Figure 3.9: Torsional interaction for hybrid AC-DC grid under long term over load on bus 9: (a) Mechanical torques for area 1, (b) mechanical torques for area 2, (c) relative rotor angles compared with generator 1, (d) frequencies under long term over load, (e) and (f) rotor angles and mechanical torques of generator 1 for only bypass the compensated Line 1, respectively.

SSR phenomenon can be adopted as the normal operation for Case 2. However, this strategy significantly debilitates the synchronization capability of the four generators system because *Line* 2 is inadequate to solely deliver an extra power of $600MW$ to Area 2, as shown in Fig. 3.9 (e)-(f). To alleviate the stress of *Line* 2, power injection from the wind farm can be a promising answer to reduce the SSR and increase the synchronization capability of the generators, suppose there is a sufficient number of standby wind turbines. Due to the instability of regional wind speed, Wind Farm 1 (WF1) and Wind Farm 2 (WF2) transmit around 380-420MW power to Bus 9 and 90-110MW power to Bus 7 at 3.09s, respectively. As can be seen in Fig. 3.10 (a) and (b), all the oscillated generator torques attenuate and eventually restore to the steady-state operation value which validates the efficacy of proposed power injection method. Meanwhile, the rotor angles can be synchronized at the

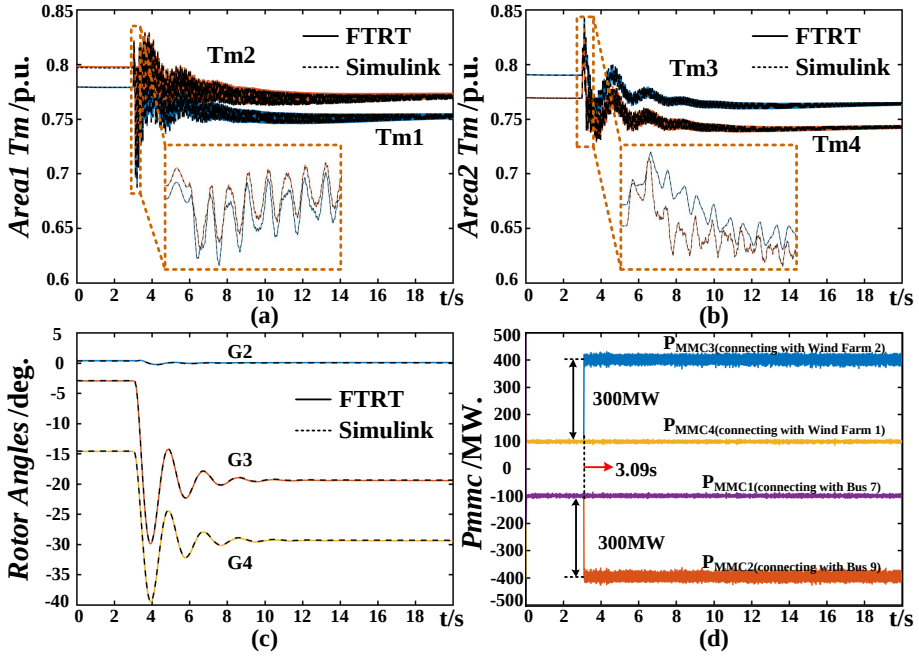

Figure 3.10: FTRT co-simulation results of mitigation the torsional interaction during long term over load: (a) (b) Mechanical torques of Area1 and Area 2, (c) relative rotor angles, (d) active power of MMCs.

Table 3.4: Maximum relative errors under different contingencies

Contingencies	Tm	RotorAngle	Frequency
Three Phase Fault	0.26%	-0.95%	-0.11%
Mitigation after Fault	0.24%	-0.97%	-0.12%
Overload	0.22%	-0.24%	-0.18%
Mitigation after Overload	0.20%	-0.35%	-0.15%

new steady-state ultimately, as shown in Fig. 3.10 (c). Fig. 3.10 (d) gives the results of the MMC transmission power trend under the overload scenario.

3.1.5.4 Error Analysis

Fig. 3.7 (a)-(d) illustrate the torsional oscillation phenomenon as a consequence of the three-phase-to-ground fault at Bus 7. In order to validate the accuracy of the proposed algorithm, the waveforms are zoomed-in. Among them, the solid lines refer to the results from FTRT simulation, and the dash lines represent the offline simulation results from Simulink® with the same grid configuration. From the zoomed-in plots in Fig. 3.7, the maximum relative error of the FTRT simulation is -0.95%, according to the formula below:

$$\epsilon = \frac{V_{FTRT} - V_{Simulink}}{V_{Simulink}} \times 100\%, \tag{3.9}$$

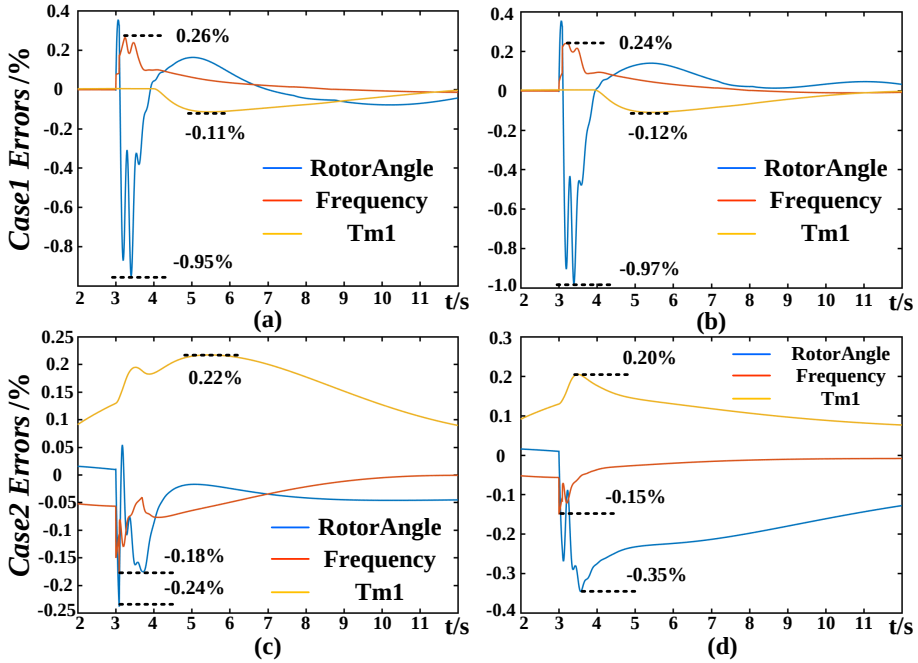

Figure 3.11: Relative errors under different contingencies: (a) Three phase fault, (b) Mitigation after fault, (c) Overload, (d) Mitigation after Overload.

where V_{FTRT} and $V_{Simulink}$ refer to the results from FTRT simulation and Simulink® respectively. Similarly, according to the zoomed-in plots in Fig. 3.9 and Fig. 3.10, the maximum relative errors are -0.24% under the long-term overload circumstance and -0.35% after mitigation. Table 3.4 provides the maximum relative errors under various contingencies.

In Fig. 3.11, the relative errors of rotor angle, frequency, and mechanical torque of G1 are drawn. It shows that the maximum error appears when a serious contingency occurs. The maximum error among these four contingencies is -0.97%, which thoroughly demonstrates the accuracy of the proposed method. Due to a trade-off between the accuracy and simulation speed, the FTRT simulation adopts the 32-bit single-precision data type. On the contrary, the inherent data type in Simulink® is 64-bit double-precision. Therefore, during the hardware emulation, the single-precision data type may result in a small fraction of data loss, which in turn leads to errors that could be neglected in the figure. Therefore, we can conclude that it is reasonable to apply the single-precision data type in FTRT simulation since the accuracy can be guaranteed.

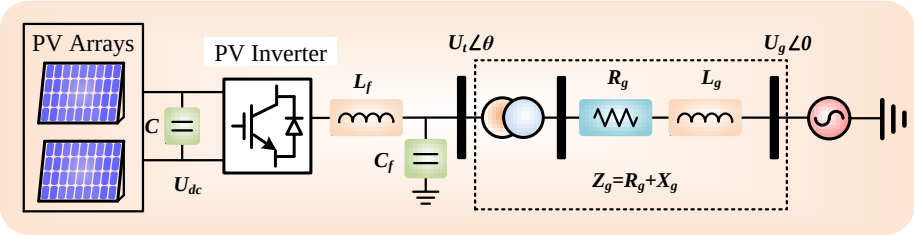

Figure 3.12: Configuration of a PV plant connected with AC grid.

3.2 Damping of Subsynchronous Control Interactions in Large-Scale PV Installations

3.2.1 PV Farm Subsynchronous Oscillation and Eigenvalue Analysis

The increasing demand for renewable energy and FACTS devices with voltage source converters (VSCs) induces the potential risk of subsynchronous control interaction. In order to investigate the principle of SSCI in PV farm, eigenvalue analysis is applied and the results are validated in Matlab/Simulink®.

3.2.1.1 Subsynchronous Control Interaction

The subsynchronous resonance (SSR) is one of the major issues that the traditional power systems encounter [34], and the inclusion of grid-connected VSC and its control system leads the hybrid grid more vulnerable. The IEEE SSR Working Group conducted a general classification of SSR/SSO [35]. SSO including subsynchronous control interaction (SSCI) is defined as the subsynchronous oscillation problems caused by the interaction between the turbine generator and other equipment in the system (VSC, HVDC, variable speed drive converter, etc.).

Usually, large-scale renewable power plants locate far away from the main grid and VSCs are needed. The PV farm SSCI may emerge when a long transmission line is connected, which will influence the overall security and stability of the power system. The AC grid strength is typically described by the short circuit ratio (SCR), which is defined as (3.10).

$$SCR = \frac{U_N^2}{Z_g \cdot S_N}, \tag{3.10}$$

where Z_g represents the grid impedance, U_N and S_N refer to the rated grid line voltage and the rated power of PV generation, respectively. A real power transmission system is treated as a weak AC system when SCR is less than 3. According to (3.10), the PV farm connected with a long transmission line is more likely to be regarded as a weak system due to the large impedance.

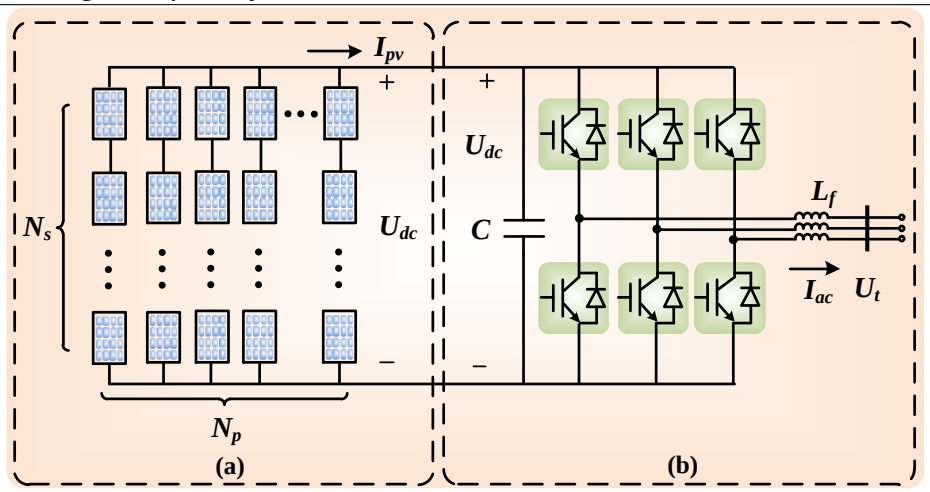

Figure 3.13: Detailed topology of (a) PV arrays and (b) PV inverter.

3.2.2 Structure of PV Farm

Fig. 3.12 provides the configuration of a PV farm connected with an infinite bus. U_{dc} is the output DC voltage of the PV station, C refers to the DC filter capacitor, C_f and L_f represent the filter capacitor and inductor of the PV inverter, R_g and L_g are the resistance and inductance of transmission line, U_t and U_g are voltages at the point of common coupling (PCC) and grid voltage, respectively. The detailed PV cell equivalent circuit and the subsequent PV inverter is provided in Fig. 3.13.

In a typical PV power plant, a large number of PV panels are arranged in an array in order to provide sufficient energy to the inverter. An arbitrary PV array is composed of N_p parallel strings and each string includes N_s PV panels in series, as shown in Fig. 3.13 (a). The I_{PV}-U_{dc} characteristic can be expressed as following equation [142]:

$$I_{PV} = N_p I_s [1 - C_1 (e^{\frac{U_{dc}}{C_2 N_s U_T}} - 1)], \tag{3.11}$$

where I_s refers to the saturation current, U_T denotes the thermal voltage, C_1 and C_2 are constant values. According to Fig. 3.13 (b) the differential equation related to PV voltage U_{dc} can be derived as:

$$U_{dc} \cdot C \frac{dU_{dc}}{dt} = U_{dc} \cdot I_{PV} - U_{td} \cdot I_d, \tag{3.12}$$

where U_{td} and I_d represent the grid connection point voltage and current in d-q frame.

3.2.3 Control System of PV Inverter

As mentioned, the introduction of VSCs may lead to the SSCI, which is largely dependent on the choice of control parameters and the network strength. A common PV inverter control strategy is provided in Fig. 3.14, where the signals with superscript '*' are the reference

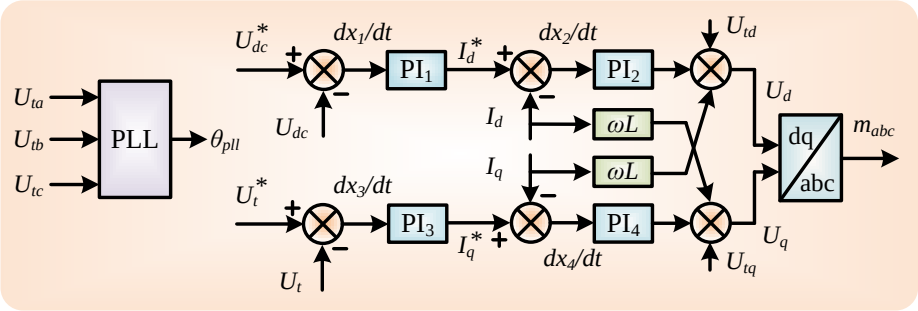

Figure 3.14: PV inverter controller.

values. Then, the transfer function of the voltage control loop can be expressed as:

$$\frac{dx_1}{dt} = U_{dc} - U_{dc}^*, \tag{3.13}$$

$$\frac{dx_2}{dt} = K_{p1} \cdot (U_{dc} - U_{dc}^*) + K_{i1} \cdot x_1 - I_d, \tag{3.14}$$

$$\frac{dx_3}{dt} = U_t - U_t^*, \tag{3.15}$$

$$\frac{dx_4}{dt} = K_{p3} \cdot (U_t - U_t^*) + K_{i3} \cdot x_3 - I_q, \tag{3.16}$$

where x_1, x_2, x_3, and x_4 are state variables; K_{p1} and K_{p3} refer to the gains of the controllers; K_{i1} and K_{i3} represent the integral coefficients.

Meanwhile, the control system of the PV inverter includes phase locked loop (PLL) to provide the fundamental frequency and phase information of the AC grid, and the differential equations have the following expression:

$$\frac{dx_{pll}}{dt} = U_{tq}, \tag{3.17}$$

$$\frac{d\theta_{pll}}{dt} = K_{p4} \cdot U_{tq} + K_{i4} \cdot x_{pll} + \omega_0, \tag{3.18}$$

where θ_{pll} is the angle produced by PLL.

3.2.3.1 Eigenvalue Analysis

In power system stability and dynamic assessment, the eigenvalue analysis is commonly used for obtaining the modal frequencies, which can be validated by fast Fourier transform (FFT). As mentioned above, not only the parameters in VSC control system may induce SSCI, the grid strength is an equally important factor to induce oscillations. Take the equivalent circuit given in Fig. 3.12 for example, the circuit equations can be obtained as:

$$L_g \frac{dI_d}{dt} = U_{td} - U_{gd} + \omega L_g I_q, \tag{3.19}$$

$$L_g \frac{dI_q}{dt} = U_{tq} - U_{gq} - \omega L_g I_d, \tag{3.20}$$

In order to calculate the eigenvalues of the proposed system, the differential algebraic equations (DAEs) (3.12)-(3.20) should be linearized at the operating point. The calculated

Table 3.5: Eigenvalues of the PV system

Eigenvalues	Frequency (Hz)	Mode
-3887.07127	0	1
-5772.03268	0	2
-12.6235382 $\pm$ 74.2719266i	11.8207	3,4
-8.5620138 $\pm$ 25.3479526i	4.034	5,6
-20.4770033	0	7
-30.0851799	0	8
-50.4943053	0	9

Frequency (Hz)	Percentage (%)	Frequency (Hz)	Percentage (%)
6	0.93	14	2.72
8	1.42	16	1.44
10	3.13	18	1.08
12	**4.91**	60	100.00

state-space equations can be expressed by the following function:

$$\Delta\dot{\mathbf{x}} = \mathbf{A} \cdot \mathbf{\Delta x} + \mathbf{B} \cdot \mathbf{\Delta u}, \tag{3.21}$$

$$\Delta\mathbf{x} = [\Delta x_1, \Delta x_2, \Delta x_3, \Delta x_4, \Delta x_{pll}, \Delta\theta_{pll}, \Delta I_d, \Delta I_q, , \Delta U_{dc}]^T, \tag{3.22}$$

where $\Delta\mathbf{x}$ denotes the vector of state variables, which is selected as (3.22), $\Delta\mathbf{u}$ refers to the input quantity, $\mathbf{A}$ and $\mathbf{B}$ are state-space matrix and input matrix, respectively. For a specific system, the state-space matrix $\mathbf{A}$ is constant at the equilibrium point and the eigenvalues can be obtained, along with the FFT results, as listed in Table 3.5. Meanwhile, the main parameters of the PV power plant are given in Table D in the appendix.

The calculated mode frequencies are validated by FFT analysis when SSCI occurs in the proposed weak grid, as shown in Fig. 3.12. The oscillation frequencies are highly dependent on the SCR, e.g. SCR=1.8 in this system. Table 3.5 indicates that, the oscillation frequency is about 12 Hz from FFT analysis, which is almost the same as one of the modal frequencies (11.8207 Hz) calculated from space-state matrix. Meanwhile, Fig. 3.15 (a), (b) provide the eigenvalue locus as the SCR varies from 3.5 to 1. The arrows in Fig. 3.15 (a) and (b) refer to decreasing grid stiffness, which indicates that λ_1, λ_8, and λ_9 change slightly, λ_2, λ_3, λ_4, and λ_7 move further to the left, while λ_5, and λ_6 move to the right-half plane (unstable region) eventually. Therefore, the SSCI is more likely to occur in a weaker grid.

Furthermore, the relation between factors such as varying PI parameters and PLL control parameters and SSCI can be analyzed using the eigenvalues. The eigenvalue results of various PI parameters and PLL control parameters are calculated and analyzed. It shows that the PLL control parameters (especially the proportional gain) have a significant impact on the damping characteristic of the system. Therefore, the eigenvalue locus for various PLL control parameters is given in Fig. 3.15 (c), (d). The SSCI in the PV plants could be also induced by the PLL control parameters, the eigenvalue locus of the PLL proportional

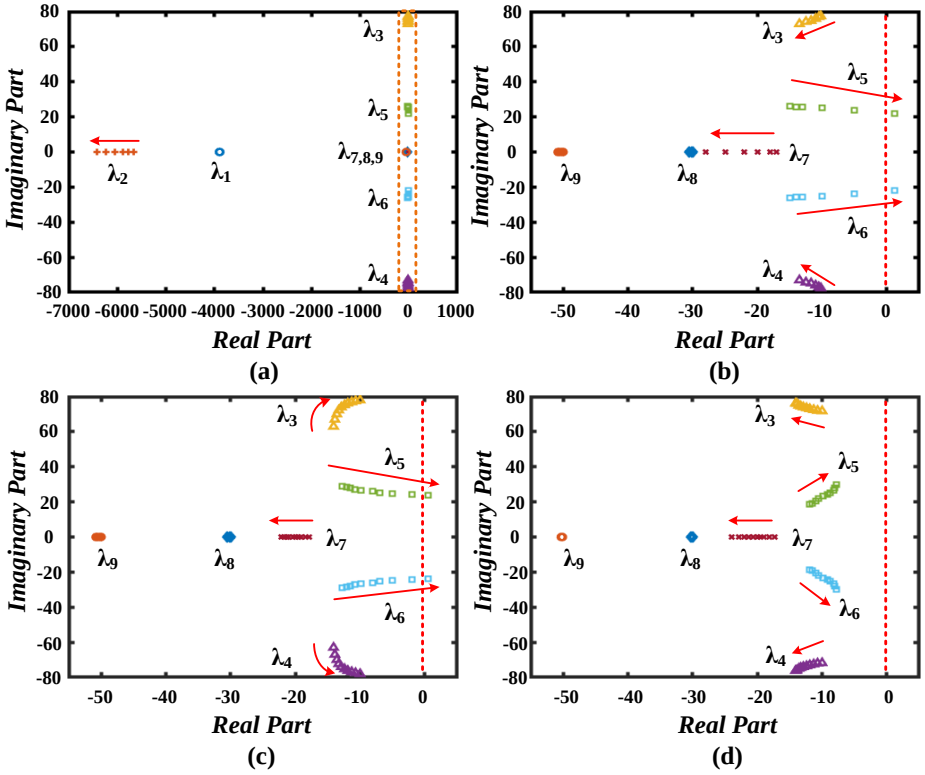

Figure 3.15: Eigenvalue locus: (a) eigenvalue locus for varying SCR, (b) zoomed-in plots for varying SCR, (c) eigenvalue locus for varying K_{p_pll}, (d) eigenvalue locus for varying K_{i_pll}.

gain varying from 100 to 10 (indicated by the direction of the arrows) is given in Fig. 3.15 (c), where the SCR is fixed at 1.8. It indicates that the λ_3, λ_4, λ_5, and λ_6 move further to the right as K_{p_pll} decreases, while λ_7 moves towards the left-half plane. The system becomes unstable when K_{p_pll} = 10, since λ_5 and λ_6 are located in the unstable region. Meanwhile, the eigenvalue locus for varying K_{i_pll} is also provided in Fig. 3.15 (d), where the SCR and K_{p_pll} are fixed at 1.8 and 50, respectively. As K_{i_pll} increases from 500 to 1500, although λ_5 and λ_6 move towards the unstable side, the system is still stable when K_{i_pll} = 1500. As a result, decreasing the grid strength and the proportional gains of PLL controller would reduce the system damping significantly. The eigenvalue locus for varying PI parameters is also provided in Fig. 3.16. It indicates that the varying PI parameters of the converter control have little impact on the stability of the system, meanwhile, the eigenvalues are always located in the left side (stable region) with varying PI parameters.

3.2.4 Equivalent Circuit of PV Cells

In order to reveal the dynamic process of the subsynchronous transient, the EMT simulation is utilized for the PV cells and the corresponding inverter station. The equivalent circuit of a PV unit is provided in Fig. 3.17 (a), which consists of the irradiance-dependent

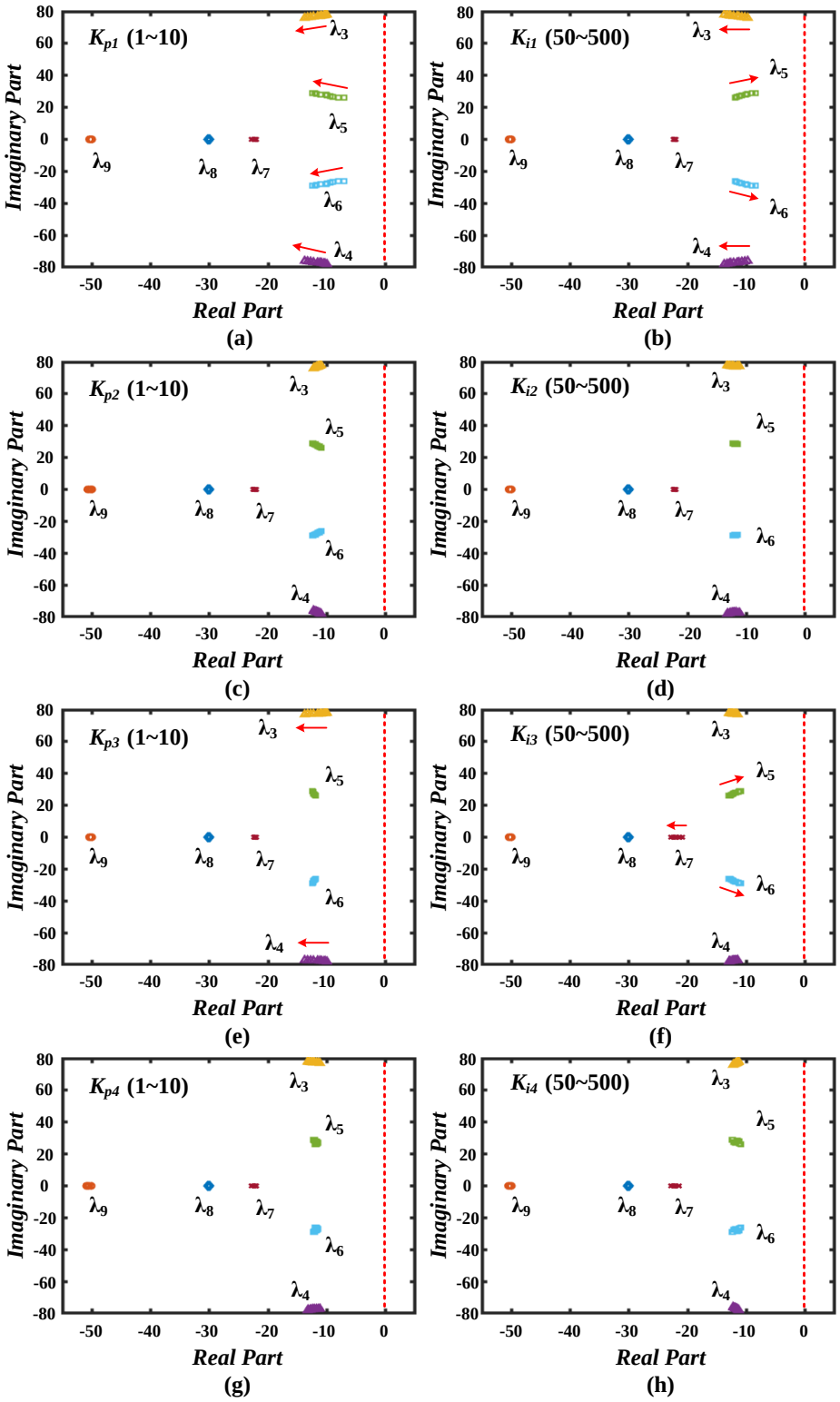

Figure 3.16: Eigenvalue locus for varying PI parameters.

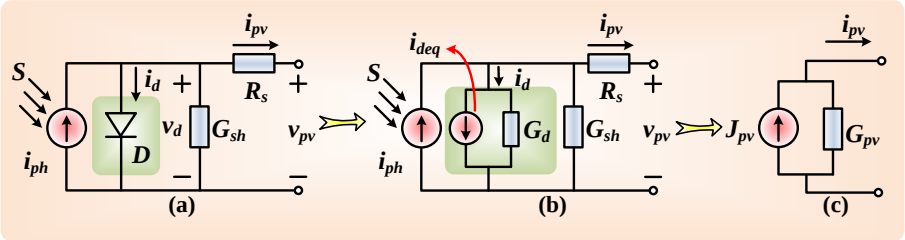

Figure 3.17: PV cell model: (a) equivalent circuit, (b) diode discretized circuit, and (c) two-node EMT model.

current source, an anti-parallel diode as well as shunt and series resistors. The working principle of the irradiance dependent current source is given as [143]:

$$i_{ph} = \frac{S}{S_{ref}} \cdot i_{ref}(1 + \alpha_T \cdot (T_k - T_{ref})), \tag{3.23}$$

where the variables with subscription ref are reference values, S refers to the solar irradiance, α_T denotes the temperature coefficient, and T_k is the environment temperature. In hardware emulation, the nonlinear component, anti-parallel diode is linearized using partial derivatives for EMT emulation, as shown in Fig. 3.17 (b). The equivalent conductance and current which represents the nonlinear diode are expressed as:

$$G_d = \frac{I_s}{V_T} \cdot e^{\frac{v_d}{V_T}}, \tag{3.24}$$

$$i_{deq} = i_d - G_d v_d, \tag{3.25}$$

where I_s and V_T are the saturation current and thermal voltage, respectively. The fact that all the components in the PV cell equivalent circuit implies that the PV cell can be expressed by current sources and resistors. The PV unit can be further simplified into two-node EMT model by Norton's theorem, as shown in Fig. 3.17 (c), where

$$J_{pv} = \frac{I_{ph} - i_{deq}}{G_d R_s + R_s G_{sh} + 1}, \tag{3.26}$$

$$G_{pv} = \frac{G_d + G_{sh}}{G_d R_s + R_s G_{sh} + 1}. \tag{3.27}$$

3.2.5 EMT and Transient Stability Co-emulation Interface

The integrated AC-DC grid with PV farm is given in Fig. 3.18, where the four-terminal (4-T) HVDC system is connected with IEEE 39-bus system at Bus 20 and Bus 39 for delivering extra active or reactive power to the AC grid, while the PV farm with a capacity of 400 MW is connected directly to the AC grid at Bus 39 through a long transmission line, which is represented as the blue circle in Fig. 3.18 (a). *MMC* 1 and *MMC* 2 act as rectifier stations,

while *MMC* 3 and *MMC* 4 are treated as inverter stations. For effective coordination of the various emulation strategies, the interface between EMT and transient stability co-emulation should be designed properly.

3.2.5.1 Data Synchronization

The PV arrays as well as VSC stations can be treated as time-varying P+jQ loads from the AC side point of view, which means both of the P and Q values are updated in every time-step to maintain the emulation accuracy. The power injection of the MMC stations can be derived as (3.28) and introduced into the admittance matrix,

$$Y = \frac{(P_{mmc} + j \cdot Q_{mmc})}{V_{Bus}^2}, \tag{3.28}$$

Meanwhile, the instantaneous voltages represented by a combination of amplitude U and phase angle θ at PCC are the inputs of the EMT simulation. The data synchronization of the AC-DC interface is simultaneous, i.e., the output time-varying P+jQ loads calculated from MMC stations are delivered to the AC gird and solved together with the admittance matrix. After solving the network equations, the resulting PCC bus phase voltages $U\angle\theta$ are in turn sent to the control systems of MMC stations.

3.2.5.2 Time-Step Synchronization

As mentioned above, a time-step of 5 ms is applied on the transient stability emulation of the IEEE 39-bus system, while the 4-T HVDC system, as well as PV farms adopt EMT emulation with the time-step of 200 μs. The emulation goes forward only when the time instant of all subsystems exceed the global time-step. In the proposed testing system, the DC system is calculated 25 times individually until it reaches the same time instant of AC grid. Then the DC system sends the instantaneous P+jQ values to the AC grid, and the calculated PCC voltages $U\angle\theta$ are delivered to the control systems of MMC stations.

3.2.6 FTRT Emulation on FPGA

The hardware emulation of the hybrid AC-DC grids with PV installation was conducted on Xilinx Virtex® UltraScale+™ VCU118 board containing XCVU9P FPGA, which includes 1182240 look-up tables (LUTs), 2364480 flip-flops (FFs), and 6840 DSP slices. The abundant hardware resources enable the large-scale AC-DC grid to be emulated on FPGA board. The reconfigurability of FPGA, i.e., enables programming hardware according to the application, allows the hardware resources can be adjusted to accommodate and represent a practical system, and results in each component or subsystem could be designed as a hardware module. After linking the hardware modules properly, the integrated AC-DC grid can be executed on the hardware.

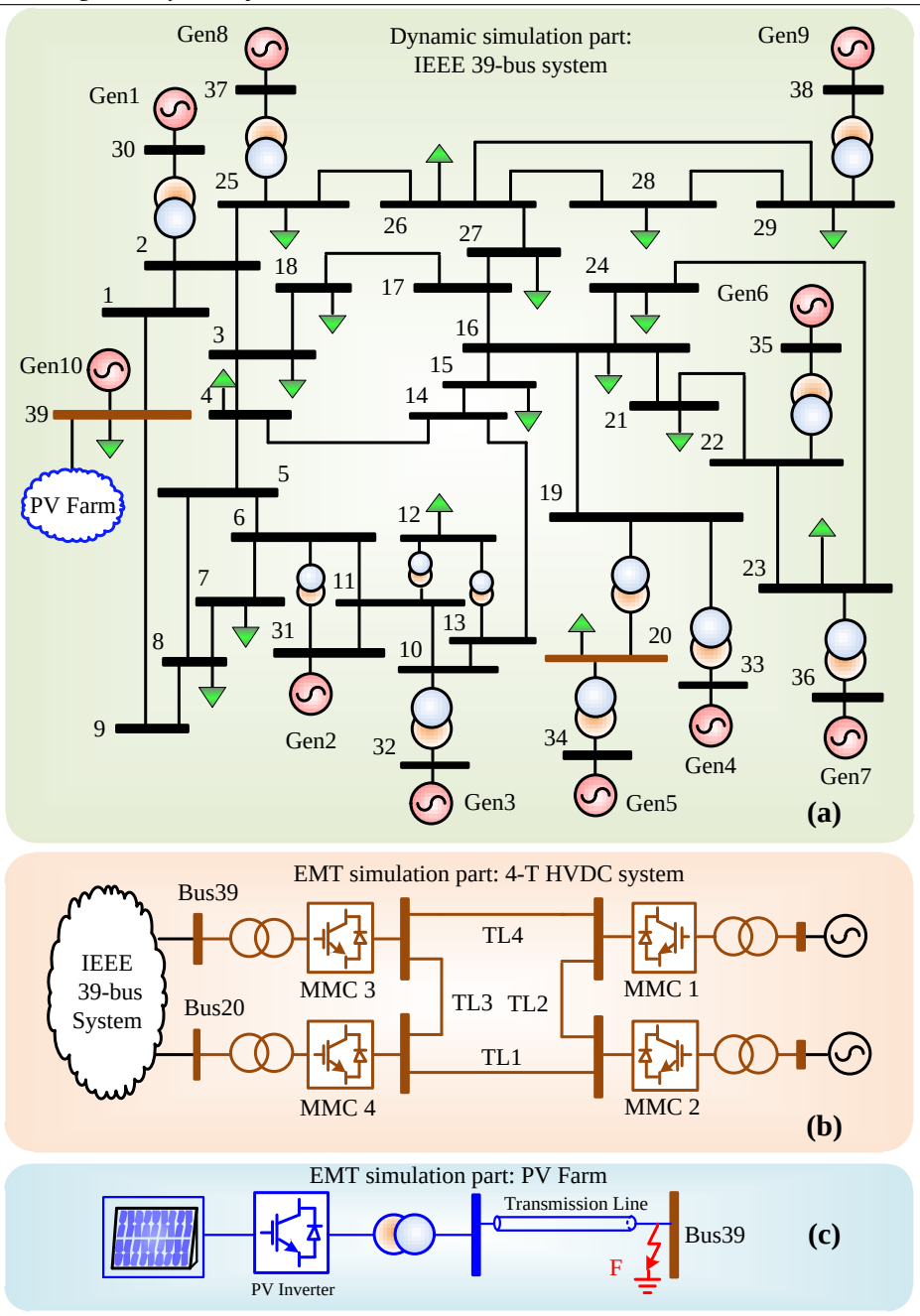

Figure 3.18: Topology of the integrated AC-DC grid with PV farm: (a) IEEE 39-bus system, (b) four terminal (4-T) HVDC system, (c) PV farm and its inverter station.

3.2.6.1 FTRT emulation Platform

Fig. 3.19 provides the hardware setup for the FTRT emulation. The initial conditions as well as the functions which represent the AC-DC grid are downloaded from the host computer via the JTAG interface, then the HIL emulation can be achieved in the FPGA board. Meanwhile, the Xilinx Virtex® UltraScale+™ VCU118 board is equipped with three

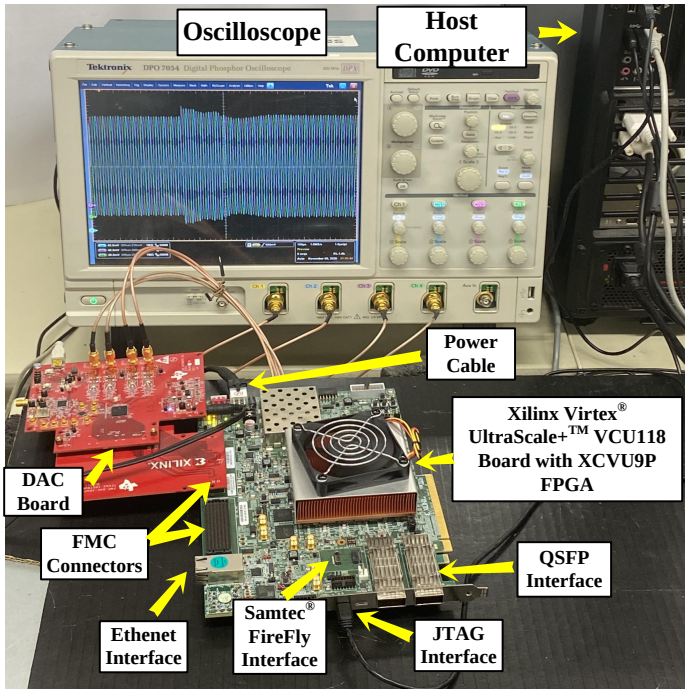

Figure 3.19: Hardware setup for FTRT emulation.

high-speed real-time communication interfaces for data transfer, which are QSFP, Samtec® FireFly and Ethernet interfaces. The received current operation conditions will be delivered to the relative hardware module. In practical, both of the QSFP and Samtec® FireFly interfaces provide up to 4×28 *Gbps* bidirectional data communication speed, which are widely utilized for receiving current operation conditions from a real power control center or other FPGA boards. Due to the relatively slow transmission speed, the Ethernet interface is treated as the backup solution for data communication. With the emulation functions downloaded from the host computer and the real-time condition signals, the hardware emulation can go forward in time domain. The output of the FPGA is digital data, which is inconvenient for following analysis. The VCU118 FPGA board provides the FMC interface to connect the DAC board, so that the output signals can be displayed on the oscilloscope.

3.2.6.2 Hardware Design Process

Recently, Xilinx Vivado® toolset provided the high-level synthesis (HLS) tool to shorten the design cycle, which enables designing hardware modules by coding in C/C++. After synthesis in the HLS tool, each circuit part written in C++ program generates an IP core for block design. The hardware block diagram along with the data steam is given in Fig. 3.20, where each block represents an IP core generated by HLS®. The discretized differential equations are calculated by *RK4*. Due to the fully independent state variables, the ten

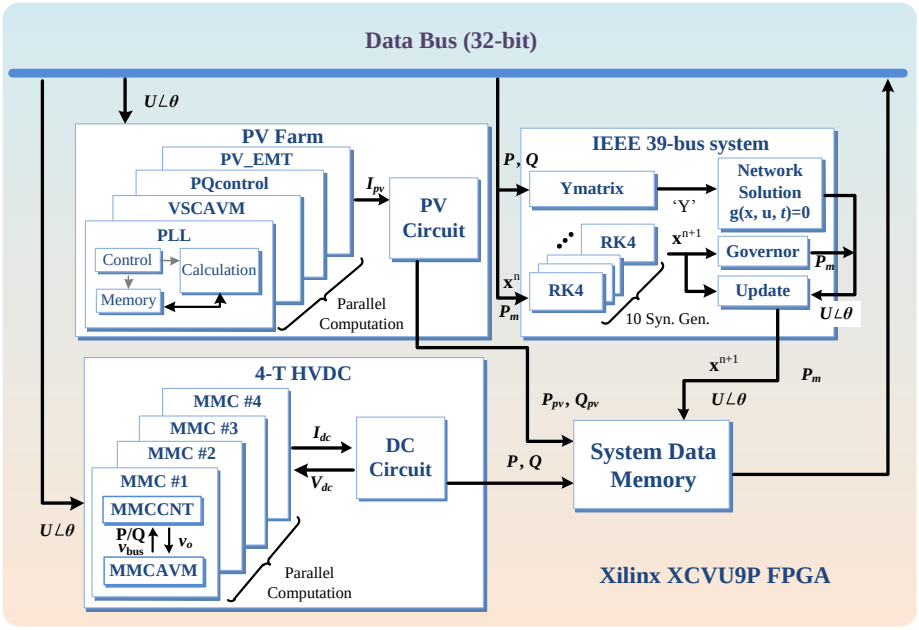

Figure 3.20: Block design for FTRT emulation.

generators in IEEE 39-bus system can be solved in parallel. The calculated admittance matrix $\mathbf{Y}$ and state variables $\mathbf{x^{n+1}}$ are delivered to *Network* and *Governor*, respectively. The 4-T HVDC system mainly involves three concurrently computed modules: the MMC average value model (AVM), its controller (CNT), and the DC grid network. The only signal that the transient stability simulation needs from the HVDC system is the dynamic active and reactive power, which are calculated in the DC grid and converted into the admittance matrix according to the PCC voltages. Meanwhile, the PV Farm also requires the PCC voltage for *PLL* module and provides the time-varying P+jQ load to IEEE 39-bus system. The external data exchange mechanism of PV Farm is the same as that of 4-T HVDC system.

Table 3.6 gives the latencies and hardware resource utilization of the proposed integrated AC-DC system. The PV stations are fully parallelized except the *PVCircuit* part, and therefore, the total latency can be calculated as $41 + 119 = 160T_{clk}$. Under an FPGA clock cycle of $10ns$, the FTRT ratio can be expressed as $\frac{200\mu s}{160\times 10ns} = 125$. Similarly, due to the parallelism, with the EMT emulation time-step of $200\mu s$ the FTRT ratio of the 4-T HVDC system is over $\frac{200\mu s}{(90+73)\times 10ns} = 122$. Meanwhile, the estimated latency in a transient stability time-step is $1470 + 269 + 33 = 1529T_{clk}$, where *YMatrix* and *RK4* should be synchronized, and the maximum latency of parallel parts is chosen. According to the proposed co-emulation interface, although the FTRT ratio of $\frac{5ms}{1529\times 10ns} = 327$ can be reached in the AC grid, the overall FTRT ratio of the hybrid AC-DC grid is dependent on the EMT emulation parts, which is about 122 times faster than real-time. With more than 122 FTRT ratio, the power control center has sufficient time to predict the adverse impacts, take remedial

Table 3.6: Specifics of major AC-DC grid hardware modules

Module	BRAM	DSP	FF	LUT	Latency
PQcontrol	0	22	3497	8418	32 T_{clk}
PVEMT	0	19	3329	11493	39 T_{clk}
VSCAVM	0	33	4489	9447	41 T_{clk}
PVCircuit	0	1109	112733	127455	119 T_{clk}
PLL	0	8	892	1357	18 T_{clk}
MMCCNT	0	54	5733	11085	85 T_{clk}
MMCAVM	16	208	8292	19277	90 T_{clk}
DCGrid	0	17	2209	2868	73 T_{clk}
YMatrix	12	1045	123388	126767	1470 T_{clk}
RK4	0	36	6970	7520	83 T_{clk}
Network	16	534	43928	57664	269 T_{clk}
Governor	0	17	3783	4598	29 T_{clk}
Update	0	38	4951	6875	33 T_{clk}
Total	92	4454	465217	603576	1692 T_{clk}
	2.13%	65.12%	19.68%	51.05%	–
XCVU37P	4320	6840	2364480	1182240	–

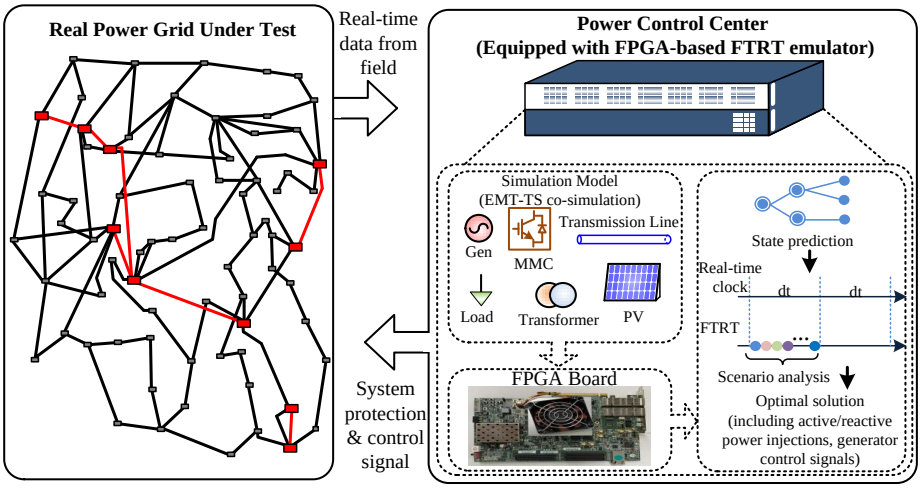

Figure 3.21: Design process of the FTRT emulation for mitigating SSCI.

actions, or decide an optimal power injection solution for damping SSCI.

3.2.6.3 Design Process for Damping SSCI

The proposed FTRT emulation can be utilized by the power control center in a real power transmission system, as given in Fig. 3.21. Once the SSCI occurs and is detected, the peripheral devices delivered the recorded data to the FPGA boards running a virtual grid via the high-speed interfaces of the FPGA board, including QSFP, Samtec® FireFly, and

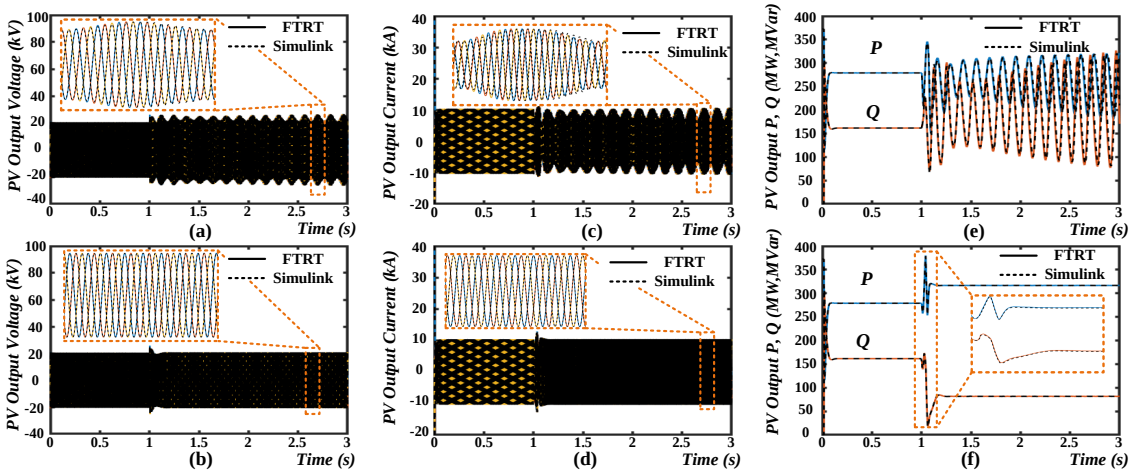

Figure 3.22: FTRT emulation results: (a) PV voltage under SSCI, (b) PV voltage after FTRT power control strategy, (c) PV current under SSCI, (d) PV current after FTRT power control strategy, (e) active/reactive power output under SSCI, and (f) active/reactive power output after FTRT power control strategy.

Ethernet interfaces. Meanwhile, in the control center, there could be several power injection scenarios being emulated in the FTRT hardware platforms. With a 122 FTRT ratio, the control center has sufficient time to come up with an optimum solution that helps maintain the synchronism of the generators and mitigate the SSCI, such as those shown in the manuscript. In addition to determining the proper power that should be delivered by the HVDC and PV stations by scanning a wide power range on the FTRT hardware, other control actions and the consequent system response could also be simulated simultaneously on the boards in the control center. However, it should be pointed out that since the focus of this work is to demonstrate how FTRT being developed and used to maintain a stable system, only an effective solution is demonstrated, and other control actions that are unable to stabilize the system will be automatically disregarded. The sufficient margin over real-time, i.e., the high FTRT ratio, leaves the control center enough time to predict the impact of a remedial action following a contingency as well as make an optimal decision.

3.2.7 FTRT Emulation Results and Validation

The subsynchronous oscillation and its mitigation strategy are emulated in the FTRT platform, and the results are validated by the Matlab/Simulink® and the off-line transient stability simulation tool TSAT® in the DSATools™ suite.

3.2.7.1 Case 1

In steady state, the PV farm delivers 287 MW active power and 170 $MVar$ reactive power to the AC grid, the total inductance of the AC transmission line is 0.1 H and the system is stable. At the time of 1 s, fixed the inductance to 1.1 H, resulting in the SCR of the AC

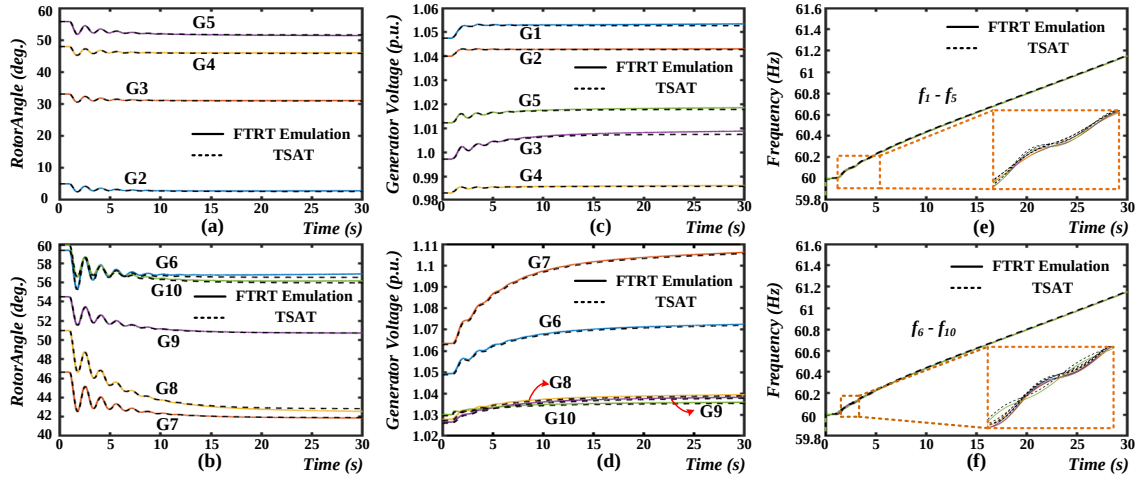

Figure 3.23: The impacts on the AC grid after power injection: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator voltages (G1-G5), (d) generator voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

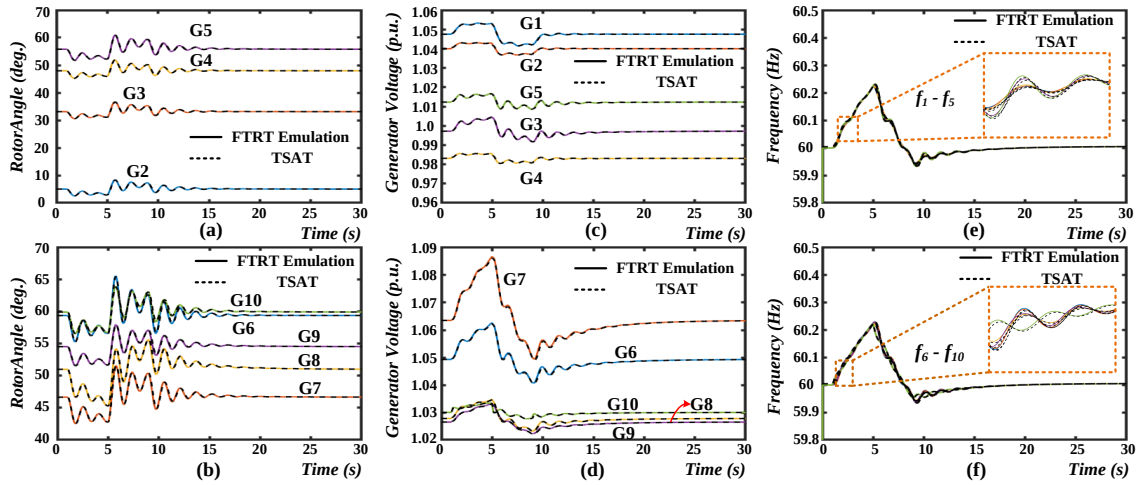

Figure 3.24: FTRT based predictive control for power system stability analysis: (a) generator relative rotor angles (G1-G5), (b) generator relative rotor angles (G6-G9), (c) generator voltages (G1-G5), (d) generator voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

transmission line reach to 1.2. Generally, the SCR of an AC transmission line below 3.0 is treated as a weak grid. After changing the inductance, the oscillation occurs, as shown in Fig. 3.22 (a), (c), and (e). Fig. 3.22 (a) and (c) imply that the oscillation frequency is below 60 Hz, which means the oscillation is in subsynchronous mode. Fig. 3.22 (e) indicates that the PV farm SSCI is diverging, which may cause serious impacts on the generator shaft if it spreads to the AC grid. In order to limit the disturbances caused by SSCI, the power control center should take remedial actions immediately.

In this work, PV farm with VSC stations has the ability of dynamically changing ac-

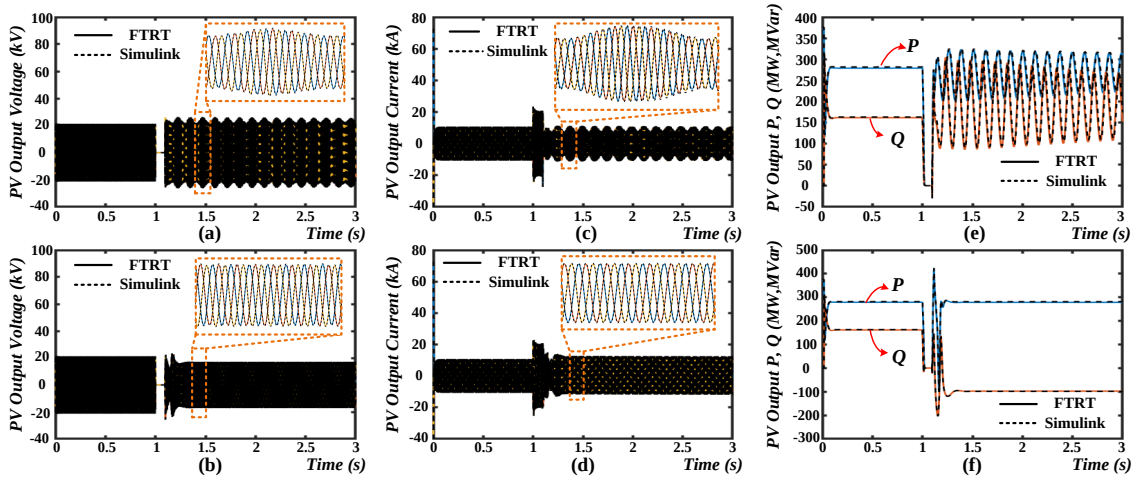

Figure 3.25: FTRT emulation results and validation: (a) PV voltage under three-phase-to-ground fault, (b) PV voltage after power control strategy, (c) PV current under three-phase-to-ground fault, (d) PV current after power control strategy, (e) active/reactive power in PV farm under three-phase-to-ground fault, and (f) active/reactive power in PV farm after power control strategy.

tive/reactive power, which has similar effects with FACTS devices. Meanwhile, with the introduction of FTRT emulation, the power control center has sufficient time to decide an optimal solution before the SSCI causes more disruption. At t=1.09 s, PV farm provides extra 48 MW active power to AC grid and reduces the reactive power to 75 $MVar$, as shown in Fig. 3.22 (f). After changing the power injection, the output voltage and current of the PV station restored stable. Meanwhile, the zoomed-in plots in Fig. 3.22 prove that the proposed FTRT hardware implementation method is as accurate as the EMT simulation in Matlab/Simulink®.

Although the power injection method can mitigate the SSCI in PV farm and the integrated weak grid significantly, the extra power may cause instability of the integrated AC gird, as given in Fig. 3.23. Due to the power injection from the PV farm, the rotor angles and voltages of the synchronous generators start to oscillate and then stabilize in a new state, as shown in Fig. 3.23 (a)-(d). However, the abnormal power injection causes the instability of the generator frequency, which cannot be restored. As can be seen in Fig. 3.23 (e)-(f), the frequency keeps rising, and eventually it is far beyond the maximum 1% threshold. The integration of the 4-T HVDC system increases the overall stability by changing the inverter's active power from 400 MW to 300 MW at around 5 s, it lasts until the frequency is recovered to 60 Hz at t=9.5 s, as Fig. 3.24 (e)-(f) shows. Meanwhile, the output voltages and rotor angles of the generators, as expected, restore to the previous state given in Fig. 3.24 (a)-(d).

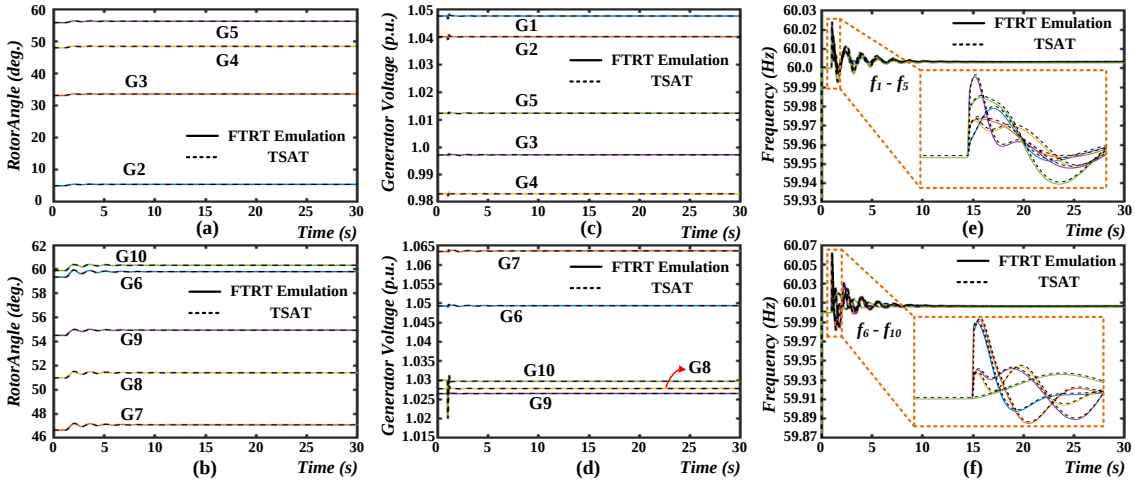

Figure 3.26: FTRT emulation results and validation: (a) generator relative rotor angles (G2-G5), (b) generator relative rotor angles (G6-G9), (c) generator voltages (G1-G5), (d) generator voltages (G6-G10), (e) frequencies (G1-G5), and (f) frequencies (G6-G10).

3.2.7.2 Case 2

In this case, series compensator is used for reducing the voltage drop and maintaining system stability since the impedance cannot be ignored in a long transmission line, which may also induce the PV SSCI after the occurrence of a serious disturbance. At the time of 1 s, a three-phase-to-ground fault lasting 90 ms happens at the remote end of the transmission line (near *Bus* 39) in PV farm, where the transmission line is 65% compensated. Fig. 3.25 (a), (c), and (e) indicate that SSCI emerges in PV farm after the fault is cleared. The FTRT emulation platform equipped in the energy control center forecasts different scenarios and then adopts a proper active/reactive power injection strategy to mitigate the SSCI induced by the series compensator. At t=1.09 s, the PV farm begins to change the output reactive power from 170 $MVar$ to -100 $MVar$, as given in Fig. 3.25 (f). With the reactive power control, the output voltage and current maintain stable as shown in Fig. 3.25 (b) and (d).

Although the PV farm absorbs reactive power for mitigating SSCI, the impacts after the reactive power change will not induce significant disturbance in IEEE 39-bus system since active power remain stable. The instability of the bus voltages, current and frequencies in AC grid can be damped by the exciter and governor system of synchronous machine, as given in Fig. 3.26. The integrated 4-T HVDC maintains the same power injection values as before the fault. Based on the emulation results, the power control strategy is able to mitigate the SSCI in PV farms, and the FTRT emulation helps tackle power system stability issues by reducing the reaction time for providing an optimal solution.

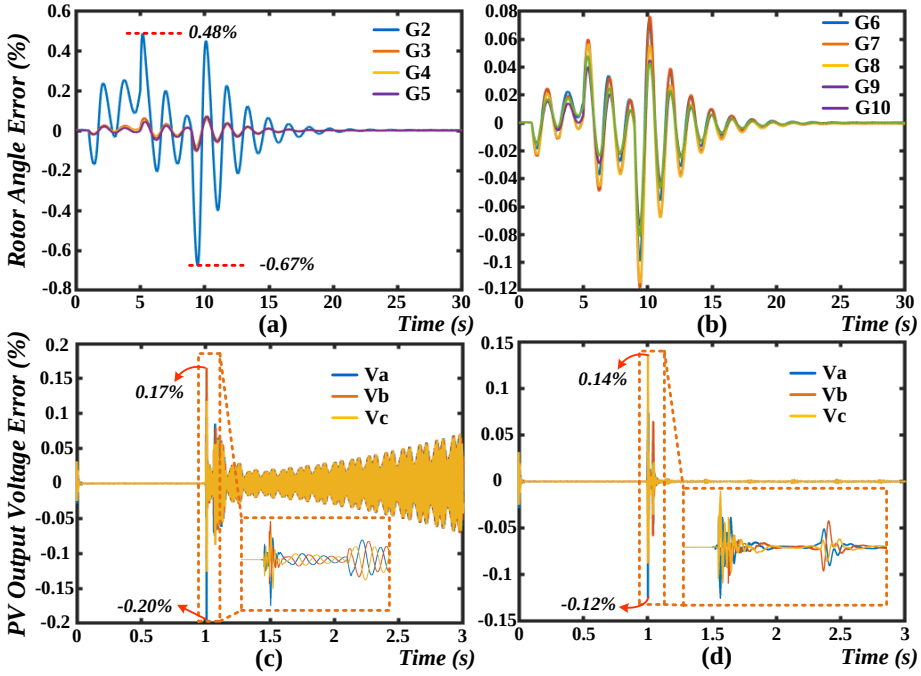

Figure 3.27: Relative errors: (a) generator relative rotor angle errors (G2-G5), (b) generator relative rotor angle errors (G6-G10), (c) PV output voltage errors under SSCI, (d) PV output voltage errors after mitigation.

3.2.7.3 Error Analysis

In order to validate the accuracy and performance of the proposed FTRT platform, Fig. 3.27 provides the relative errors of the transient stability emulation part and EMT emulation part, where the relative errors are calculated as:

$$\epsilon = \frac{V_{FTRT} - V_{Simulink/TSAT}}{V_{Simulink/TSAT}} \times 100\%, \tag{3.29}$$

Fig. 3.27 (a) and (b) provide the relative errors of rotor angles in Fig. 3.24, where the 4-T HVDC system takes actions to maintain the overall stability. Under this contingency, the AC system experience three times active/reactive power injection, which induces the maximum computational error. Fig 3.27 (a)-(b) indicate that the maximum error appears right after the occurrence of serious disturbances, e.g., at t=9.5s, the maximum error of -0.67% appears when the HVDC system changes to the normal operation stage. Fig. 3.27 (c) and (d) provide the EMT emulation part errors of PV output voltage under SSCI and after mitigation, respectively. Due to a dramatic voltage oscillation, the maximum relative error appears when the SSCI occurs. The relative errors of the EMT emulation range from 0.17% to -0.20%. After the mitigation of SSCI, the relative errors restore to stable gradually as shown in Fig. 3.27 (d). Compared with the TS emulation part, the EMT emulation has higher accuracy since a relatively small time-step is applied, and the overall relative errors of the proposed FTRT based system are within $\pm 1\%$.

3.3 Summary

An active power control method to mitigate the subsynchronous interaction using FTRT emulation of hybrid AC-DC grid is proposed. The introduction of the multi-mass torsional shaft into a dynamic simulation can demonstrate the SSR phenomenon under three-phase fault and long-term overload. Compared with EMT simulation, the proposed model applied a larger time-step of $3ms$, which is convenient to achieve FTRT in hardware emulation. Furthermore, the proposed algorithm is suitable for the energy control center to eliminate the influence of torsional interaction after a serious disturbance. With the 138 times FTRT execution, the energy control center has enough time to predict the power system stabilities and selecting a proper power injection factor to maintain the system stable.

Furthermore, this chapter also presented the subsynchronous control interaction issue induced by the operation modes of PV converters integrated into transmission and distribution systems and a new solution combining hardware parallelism, the FTRT algorithm, and consequently the predictive functionality of the platform. Taking the inherent advantages of reconfigurability and parallelism, the FPGA allows emulating the integrated system in FTRT mode. Meanwhile, the eigenvalue analysis on the PV farm and its control system provided theoretical basis for the SSCI phenomenon in PV plants connected to a weak grid. The time-domain results from the FTRT emulation demonstrate that the EMT and transient stability co-emulation are numerically stable and accurate in comparison with the off-line simulation tools Matlab/Simlink® and TSAT®. Therefore, the FTRT co-simulation can help mitigate the contingencies in an extremely small time span, which is significantly meaningful in a practical power transmission system.

4

Hardware Emulation of Extensive Contingencies for Dynamic Security Analysis

The rapid expansion of modern power systems has brought a tremendous computational challenge to dynamic security analysis (DSA) tools which consequently need to process extensive contingencies. A multi-FPGA-based DSA platform is proposed to provide fast and accurate contingency screening data for a large-scale AC-DC grid by faster-than-real-time (FTRT) emulation. Compared with currently available commercial real-time (RT) simulation tools, the FPGA-based platform has the following advantages. The most straightforward difference between an FTRT emulation platform and RT simulators is the computation speed. RT simulation implies that the hardware must solve the model equations within an interval of the time-step. On the other hand, FTRT is stricter in terms of hardware latency, and the platform runs at least several times faster than a RT simulator. FTRT emulation can meet all the requirements of RT simulation, while the RT simulation tools are unable to reach FTRT due to their scalability and computational speed limits.

Secondly, the capability and scalability of the FPGA-based FTRT emulation platform are better than RT simulators. For example, the 141-bus system with 38 generators is simulated using the RTDS® simulator, and 4 PB5 racks were needed [144]. In order to reduce the hardware resources and reduce the cost, only 5 buses and 2 generators were simulated on RTDS®, while the rest of the system parts were simulated on FPGA boards. As shown later in this paper, two 500-bus systems with 180 generators in total can be executed on a single Xilinx® VCU128 board, which demonstrates the FPGA's capability in emulating a large power system. The reconfigurability and the sufficient hardware resources allow the entire grid to be deployed on the platform after proper system partitioning and allocation. Meanwhile, a specific AC-DC grid interface using dynamic voltage injection is proposed to maintain a constant admittance matrix despite the HVDC converter outputs

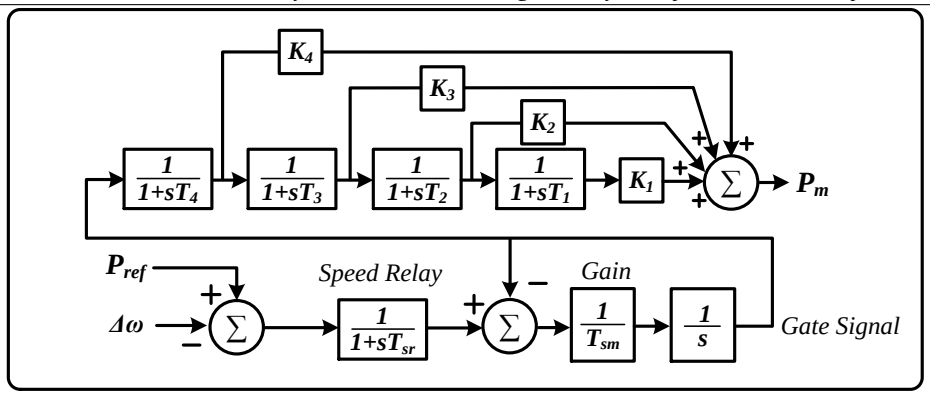

Figure 4.1: Turbine governor system of the synchronous generator.

being time-varying, which consequently reduces hardware resources utilization and expedite the emulation.

Since the FTRT emulation enables a high computation speed above real-time, the grid can be emulated much faster and therefore it can accelerate planning schedules, predict the upcoming disturbances, and help in devising new control strategies. The proposed FTRT emulation can also be used in the energy control center to provide sufficient time to take remedial actions, recommend an optimal control strategy to mitigate adverse impacts, and enhance the overall stability and security of the system.

4.1 AC Grid Model for Dynamic Security Analysis

4.1.1 Transient Stability Problem

As mentioned in Section 2.1.1, the transient stability simulation for DSA is based on a set of differential algebraic equations (DAEs). The 9^{th}-order DAEs are also applied to solve the synchronous generators in AC grid. Meanwhile, The detailed mechanical equations and swing equations of a synchronous machine are also included. In a practical power transmission system, the mechanical power is provided by the turbine governing system. In order to obtain a higher accuracy of the dynamic security analysis results, a four-stage governor system is also included as given in Fig. 4.1. To reduce the computational burden and execution time of the hardware emulation, the governor system equations are solved by Forward Euler with a time-step of 1 ms, which are not included in the 9^{th}-order DAEs.

The accuracy of the transient stability simulation is highly dependent on the solution strategies of the DAEs, which can be roughly classified into two categories: implicit and explicit integration methods. The former is essentially iterative methods such as Newton-Raphson, which has a higher accuracy under large time-steps. However, a large dimension of the DAEs may lead to more iterations in every single time-step and consequently extra execution time. Furthermore, due to the inherently sequential iterations until convergence, the iterative method is not suitable for parallel processing in FPGAs. Therefore, the explicit

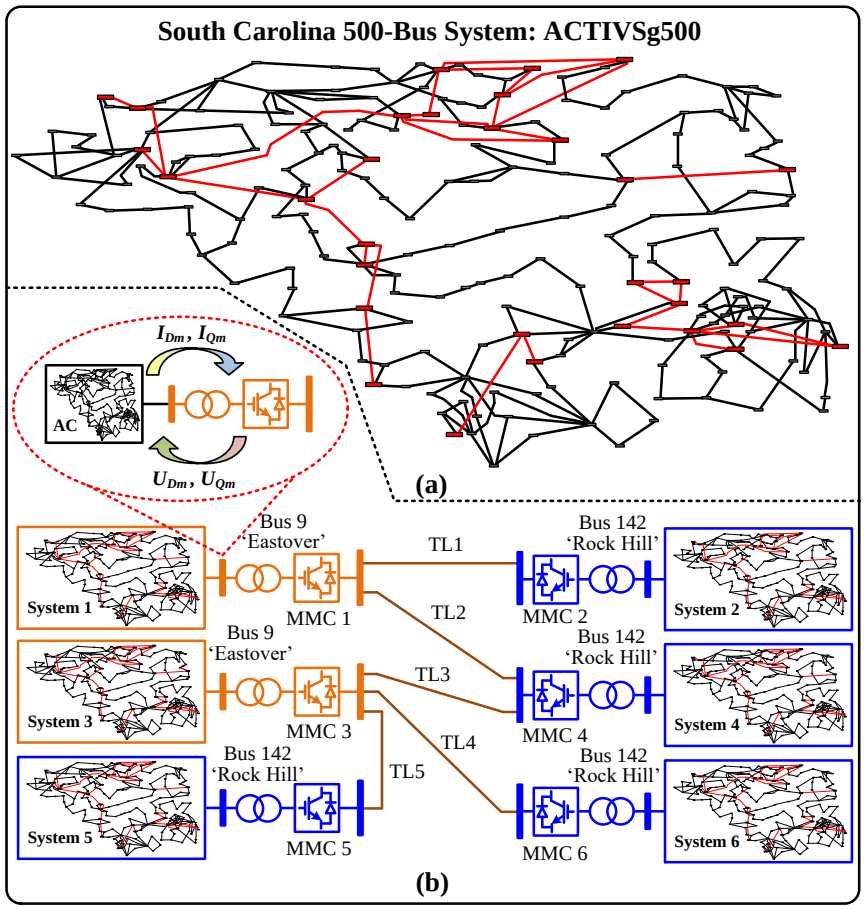

Figure 4.2: Topology of hybrid AC-DC grid: (a) transient stability simulation part: South Carolina 500-bus system (ACTIVSg500), (b) EMT simulation part: six-terminal HVDC grid.

method 4th-order Runge-Kutta (RK4) is adopted in the hardware emulation for the high efficiency and low hardware resource demand.

4.1.2 AC-DC Grid Interface

The single-line diagram of the hybrid AC-DC grid is shown in Fig. 4.2, where the 6 AC-TIVSg 500-bus systems [145] connect with a 6-terminal (6-T) HVDC system. MMC 1 and MMC 2 operate as inverter stations and connect with AC System 1 and 2 via Bus 9, respectively, while the remaining four terminals, all acting as rectifier stations, each delivers 100 MW active power from the connected AC grid via Bus 142. Since the AC grid undergoes transient stability simulation with a time-step of 1 ms, and the EMT emulation with a time-step of 200 μs is applied to the HVDC system, the latter part should be calculated five times more frequent than the former before data synchronization to keep numerical stability. Furthermore, the distinct emulation strategies prompts an interface based on dynamic

voltage injection strategy which enables the two types of simulations to be compatible in one program, in addition to maintaining a constant admittance matrix that results in acceleration of the hardware emulation.

The synchronous machines can not only be represented in detail by Park's equation as given in (2.1)-(2.6), but also constant voltage sources in the D-Q frame when their dynamics are not concerned. The HVDC converter stations in the EMT simulation can be treated as time-varying voltage injections to the AC grid, which are equivalent to the non-detailed machines in transient stability simulation. The dynamic voltages $\mathbf{U_{Dm}}$ and $\mathbf{U_{Qm}}$ in Fig. 4.2 (b) of the HVDC converter stations are directly delivered to the AC grid and integrated with the AC network equations without updating the admittance matrix. Due to the voltage injection method, (2.14) can be expanded as:

$$\begin{bmatrix} \mathbf{I_n} \\ \mathbf{I_m} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{nn}} & \mathbf{Y_{nm}} \\ \mathbf{Y_{mn}} & \mathbf{Y_{mm}} \end{bmatrix} \begin{bmatrix} \mathbf{U_n} \\ \mathbf{U_m} \end{bmatrix}, \tag{4.1}$$

where the subscription n refers to the synchronous machine nodes represented by the detailed Park's equations, m are the nodes where converter stations locate, and $n+m$ denotes the N generator nodes.

As the voltages calculated by the HVDC system are in D- and Q- axis, (4.1) which is based on complex numbers yields 4 real matrix equations:

$$\mathbf{I_{Dn}} = \mathbf{G_{nn}U_{Dn}} - \mathbf{B_{nn}U_{Qn}} + \mathbf{G_{nm}U_{Dm}} - \mathbf{B_{nm}U_{Qm}}, \tag{4.2}$$

$$\mathbf{I_{Qn}} = \mathbf{G_{nn}U_{Qn}} + \mathbf{B_{nn}U_{Dn}} + \mathbf{G_{nm}U_{Qm}} - \mathbf{B_{nm}U_{Dm}}, \tag{4.3}$$

$$\mathbf{I_{Dm}} = \mathbf{G_{mn}U_{Dn}} - \mathbf{B_{mn}U_{Qn}} + \mathbf{G_{mm}U_{Dm}} - \mathbf{B_{mm}U_{Qm}}, \tag{4.4}$$

$$\mathbf{I_{Qm}} = \mathbf{G_{mn}U_{Qn}} + \mathbf{B_{mn}U_{Dn}} + \mathbf{G_{mm}U_{Qm}} - \mathbf{B_{mm}U_{Dm}}, \tag{4.5}$$

where $\mathbf{G}$ and $\mathbf{B}$ refer to the real part and the imaginary part of the corresponding $\mathbf{Y}$ matrix. Following the solution of DC grid, the components $\mathbf{U_{Dm}}$ and $\mathbf{U_{Qm}}$ in the above equations are known, while the values of $\mathbf{U_{Dn}}$ and $\mathbf{U_{Qn}}$ associated with the detailed synchronous machines are not directly known. After each step of integration, the synchronous voltages can be evaluated by the state variables. Since the values of $\mathbf{U_{Dn}}$ and $\mathbf{U_{Qn}}$ are available after (4.2) and (4.3) are solved, the subsequent equation (4.4) and (4.5) can then be solved. Meanwhile, the calculated current vectors $\mathbf{I_{Dm}}$ and $\mathbf{I_{Qm}}$ in D-Q frame are sent to the HVDC system for its next time-step emulation, as given in Fig. 4.2 (b).

4.2 Hardware Emulation on Multi-FPGA Platform

The proposed hybrid AC-DC grid is implemented on the integrated Xilinx Virtex® UltraScale+™ FPGA platform, which includes 2 VCU118 boards equipped with XCVU9P FPGA and 2 VCU128 boards containing XCVU37P FPGA. System 1 and 2 in Fig. 4.2(b) are deployed on the 2 VCU118 boards, respectively. Due to abundant hardware resources of VCU128

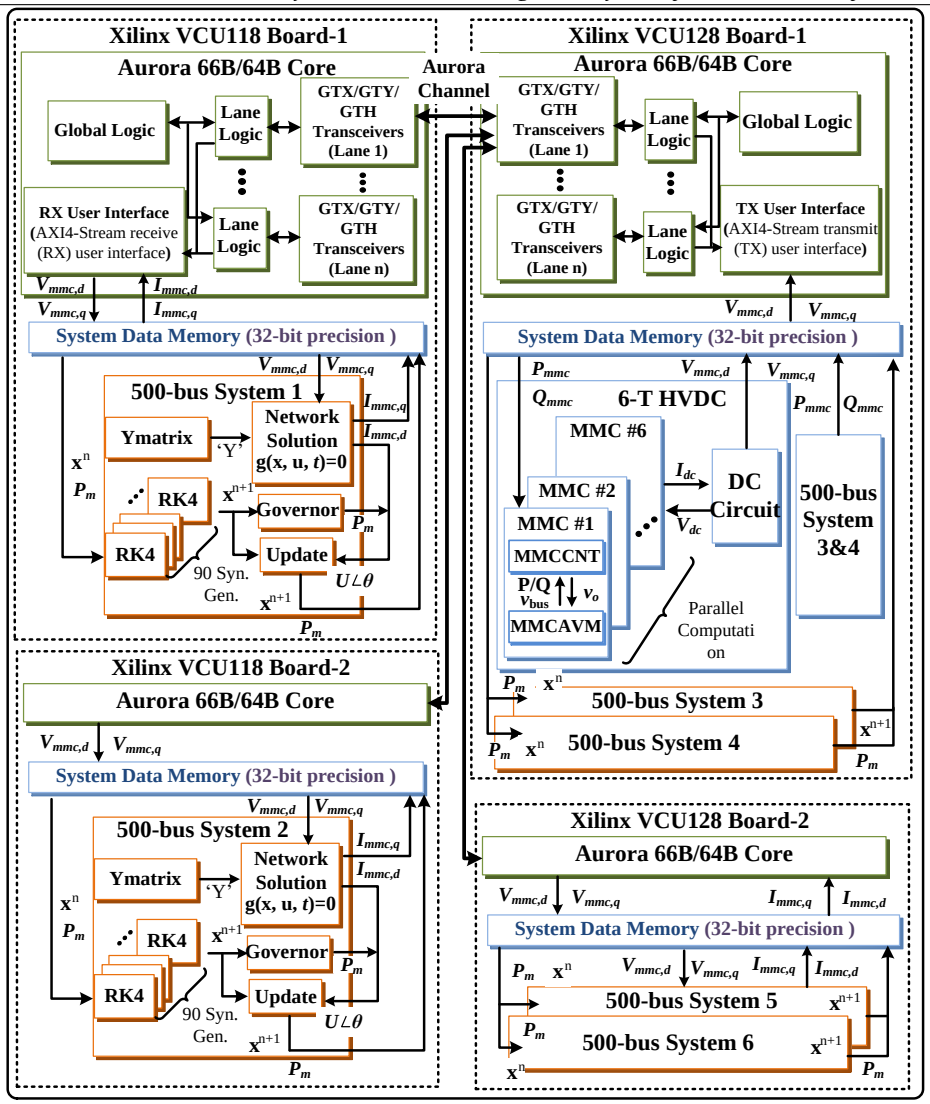

Figure 4.3: Hardware implementation block design for the proposed FTRT DSA platform.

boards, System 3 and 4 including the 6-T HVDC system are implemented on VCU128 Board 1, while the remaining 2 AC systems (System 5 and 6) are calculated on VCU128 Board-2. The reconfigurability of the FPGAs enables each circuit part or subsystem to be designed as a hardware module, and allows programming its function according to the application. After linking the hardware modules and designing the parallel components properly, the integrated AC-DC grid can be executed on the proposed platform.

The subsystems and functions which consist of the proposed integrated AC-DC grid written in C/C++ code are transformed into hardware modules by Xilinx Vivado® high-level synthesis (HLS) tool. Then they, termed as IP cores, are imported into Vivado® for block-level design. Due to the dynamic voltage injection strategy, the PCC voltages in the *D-Q* frame are chosen as the communication data among different FPGA boards, which is

Table 4.1: Specifics of major AC-DC grid hardware modules

Module	Latency	BRAM	DSP	FF	LUT
ACTIVSg 500-bus system on VCU128 ($100MHz$)					
RK4	29 T_{clk}	0	18	1939	2045
Network	196 T_{clk}	16	678	48921	54732
Governor	114 T_{clk}	0	19	4046	4132
Update	21 T_{clk}	0	35	3639	3970
HVDC system on VCU128 ($100MHz$)					
PQcontrol	45 T_{clk}	0	62	4398	5372
MMCAVM	96 T_{clk}	0	16	2582	5270
MMCCNT	86 T_{clk}	0	62	5829	6320
HVDCNetwork	73 T_{clk}	0	20	2488	3710
Total_VCU128	–	0.79%	93.15%	42.82%	97.46%
Total_VCU118	–	0.37%	59.11%	25.00%	51.99%
Available hardware resources					
VCU128	–	4032	9024	2607360	1303680
VCU118	–	4320	6840	2364480	1182240

realized by the build-in IP Aurora 66B/64B core. The hardware block diagram along with the data stream is given in Fig. 4.3.

Table 4.1 provides the latency and the hardware resource utilization of each circuit part in the proposed integrated AC-DC system, where the latency is defined in clock cycles which is 10 ns under the FPGA frequency of 100 MHz. The total latency of the AC grid can be calculated as $29 + 196 + 114 + 21 = 360T_{clk}$, with a transient stability time-step of 1 ms, the FTRT ratio of the AC system is over $\frac{1ms}{360\times10ns} = 277$. Since the hardware modules *PQcontrol*, *MMCAVM*, and *MMCCNT* can be solved in parallel, the overall hardware delay is determined by their maximum latency which is 96 $Tclk$, resulting in an FTRT ratio of $\frac{200\mu s}{96\times10ns} = 208$. Thus, the overall FTRT ratio of the hybrid AC-DC grid as Case I is determined by the EMT emulation part, which gives a final 208 times speedup over real-time. In contrast, if a single ACTIVSg 500-bus system without DC grid is analyzed as Case II, the FTRT ratio of the pure AC grid is more than 277, where six 500-bus systems can be executed concurrently in the integrated FPGA boards.

Fig. 4.4 provides the hardware platform for FTRT emulation. The functions which represent the target power transmission system and the initial conditions of the synchronous generators are downloaded from the host computer via the Joint Test Action Group (JTAG) interface. Since multiple FPGA boards are assembled, data communication among them is also a challenge in emulating such a complex system. The Xilinx Virtex® UltraScale+™ series FPGA boards provide efficient communication ports, such as Quad Small Form-factor Pluggable (QSFP), Samtec® FireFly interfaces, which can significantly accelerate the communication speed, since both interfaces can provide a maximum bidirectional communication rate of 4×28 $Gbps$, which can be utilized for delivering the current operating con-

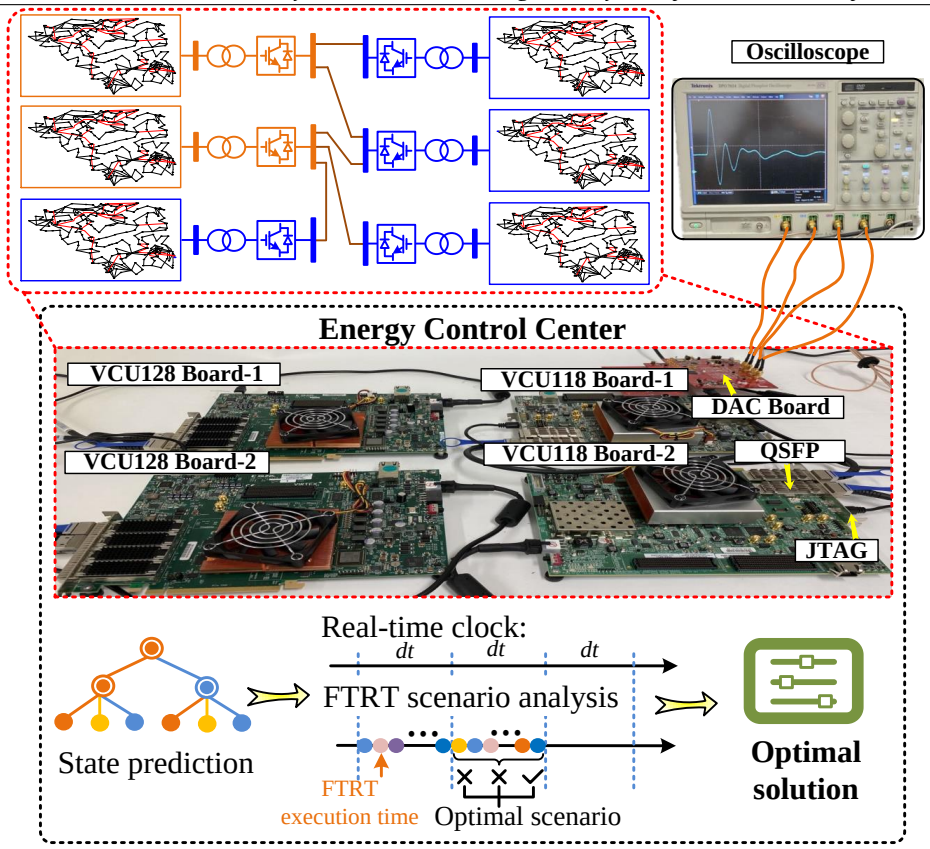

Figure 4.4: Hardware implementation platform for FTRT DSA emulation and scenario analysis in the energy control center.

ditions from real power transmission system or other FPGA boards, making the proposed FTRT emulation suitable for online DSA in the energy control center. Once a disturbance is detected, the real-time operation data from the field will be delivered to the control center. Meanwhile, there could be hundreds of scenarios being emulated in the FTRT emulation platform for a comprehensive study. Since a more than 208 FTRT ratio can be achieved, the power control center has sufficient time to come up with optimal strategies for contingencies in various subsystems that help maintain the stability of the entire system.

The scalability of the proposed FTRT emulation is demonstrated by interconnecting four FPGA boards in realizing the FTRT emulation, and more FPGA boards can be connected along with a further expansion of the AC-DC grid. Table 4.1 indicates that the hardware resources such as DSP and LUT of VCU128 board are nearly full for two 500-bus systems with 180 generators. Although the *Network* module will increase along with the size of the system, its influence can be neglected if multiple synchronous generators are included since the *Network* module is only calculated once in a single time-step. The hardware resource utilization is proportional to the synchronous generators, and therefore, a Xilinx® VCU128 board is able to accommodate about 180 generators with excitation and governor system in parallel. With a larger power system scale, the multiple FTRT emula-

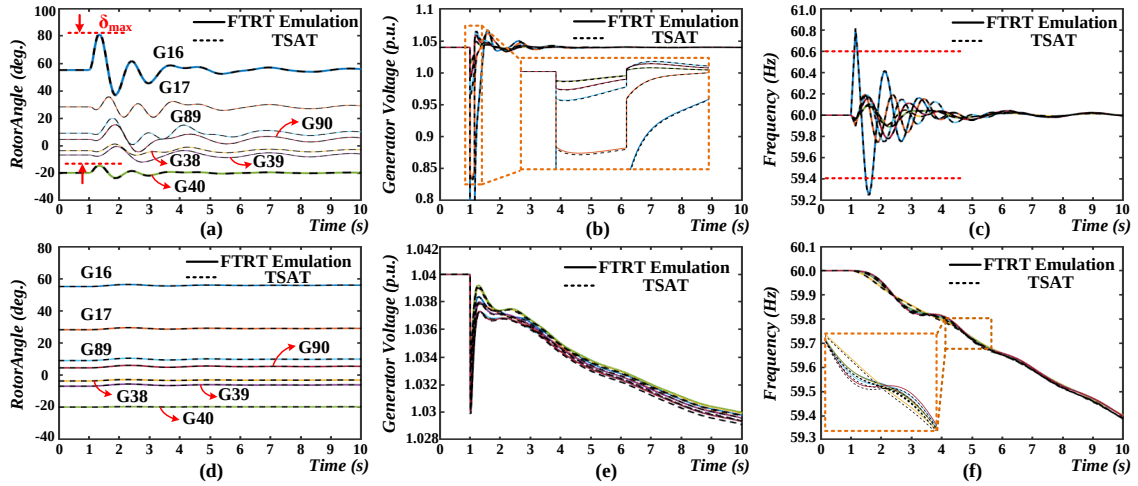

Figure 4.5: FTRT emulation results: (a) generator rotor angles under three phase fault, (b) generator output voltages under three phase fault, (c) generator frequencies under three phase fault, (d) generator rotor angles under long term over-load, (e) generator output voltages under long term over-load, (f) generator frequencies under long term over-load.

tors can be employed in the dynamic security assessment for HIL emulation or predictive control.

4.3 Contingency Screening Results and Validation

4.3.1 Dynamic Security Index

The contingency screening for dynamic security analysis is based on the system in Fig. 4.2. The transient stability analysis focuses on the rotor angle stability, voltage stability, and frequency stability, and the rotor angle stability is described as the power angle-based stability margin (ASM), which is defined as follows for each AC grid in the system.

$$ASM = \frac{360 - \delta_{max}}{360 + \delta_{max}} \times 100, \tag{4.6}$$

where δ_{max} is the maximum angle separation of any two generators in the same AC subsystem at the same time in the post-fault response, which is illustrated in Fig. 4.5 (a). The transient stability index of a contingency is chosen as the smallest index among all 6 AC grids. ASM is directly proportional to rotor angle separation so it provides an indication of severity of a disturbance. A smaller-than-zero ASM indicates that the δ_{max} is larger than 360 unit, which means the generators lose synchronism and the system is under unstable condition, while ASM>0 corresponds to a secure system status.

4.3.2 Case 1: Hybrid AC-DC Grid

At t = 1 s a three-phase-to-ground fault lasting 180 ms occurs at *Bus* 16 in *System 1*, the imminent impacts including severe disturbances to the rotor angles, bus voltages, and

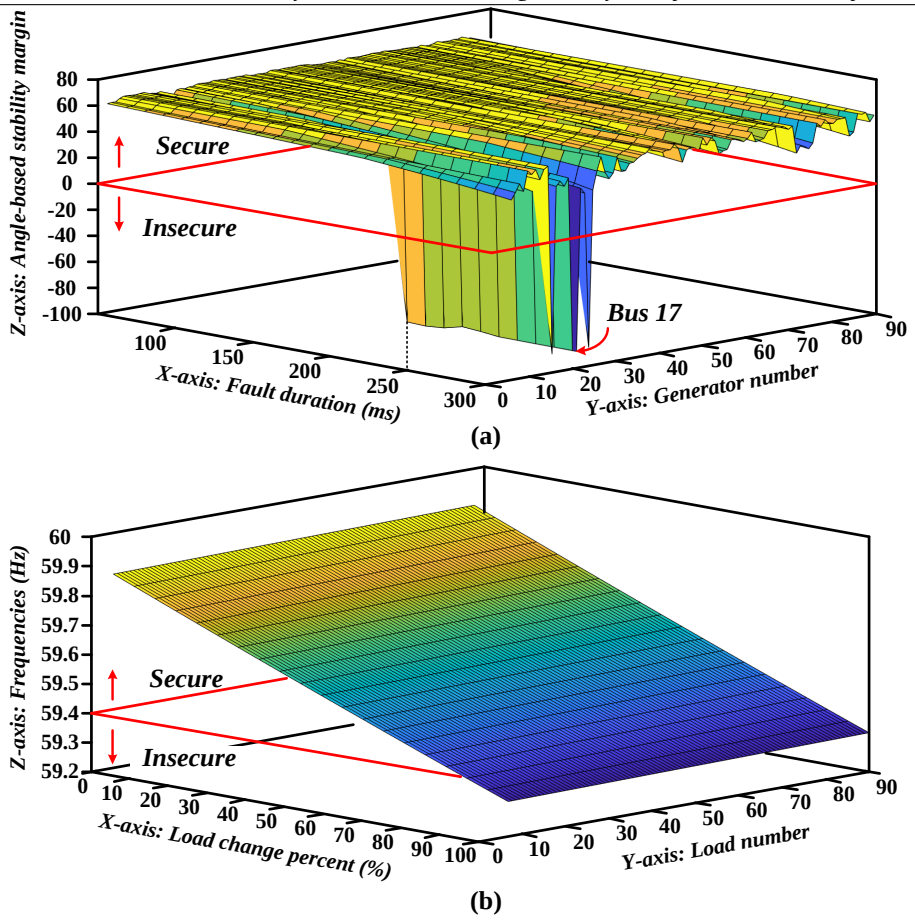

Figure 4.6: Dynamic security indices of extensive contingencies: (a) ASM results of three phase fault contingencies, (b) frequencies of long term over-load contingencies.

frequencies, as shown in Fig. 4.5 (a)-(c). Fig. 4.5 (a) demonstrates that the maximum angle separation (δ_{max}) is less than 360 unit, and therefore, the system is under secure condition. Although one of the frequencies exceeds the $\pm 1\%$ threshold after the three-phase fault, it restores to the normal operation eventually. Fig. 4.5 (d)-(f) provide the emulation results after a long-term over-load. At 1 s, a 90% over-load occurs to the load at *Bus* 392 in *System 1*. There are no significant impacts on the rotor angles of the synchronous generators as given in Fig. 4.5 (d). However, the bus voltages and the frequencies of the generators keep decreasing after the over-load disturbance and cannot be recovered by the generators' control system. The whole system enters the unstable condition at around 9 s when the frequencies reach below 59.4 Hz. The dashed lines represent the results calculated from the simulation tool TSAT®, while the solid lines refer to the FTRT emulation results from FPGA boards. The zoomed-in plots in Fig. 4.5 (b) and (f) demonstrate that the accuracy of the proposed FTRT emulation since the waveforms of the hardware emulation are identical to TSAT® off-line simulation results.

Fig. 4.6 (a) provides ASM results calculated from FTRT emulation under 1890 three-

Table 4.2: Contingency screening results and errors for 300ms three-phase-to-ground faults in System 1

Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)
17	-86.64	-86.52	0.14	22	52.40	52.34	0.11	37	59.06	58.92	0.24
11	-85.42	-85.31	0.13	61	52.78	52.80	0.04	45	59.60	59.48	0.2
20	-85.34	-85.27	0.08	30	53.37	53.24	0.24	76	59.72	59.60	0.2
16	-85.23	-85.16	0.08	47	53.45	53.41	0.07	51	59.75	59.63	0.2
19	36.42	36.55	0.36	3	53.50	53.58	0.15	81	59.77	59.68	0.15
21	37.75	37.91	0.42	8	53.77	53.80	0.06	46	60.07	59.81	0.43
71	38.89	39.00	0.28	62	53.91	53.96	0.09	34	60.13	59.99	0.23
74	40.64	40.72	0.2	89	54.09	54.08	0.02	36	60.15	60.13	0.03
18	40.92	40.96	0.1	63	54.29	54.17	0.22	65	60.40	60.26	0.23
1	41.16	41.22	0.15	58	55.10	55.10	0.00	64	60.55	60.29	0.43
73	43.05	43.05	0.00	31	55.27	55.23	0.07	87	60.56	60.48	0.13
72	44.56	44.56	0.00	77	56.62	56.47	0.27	70	60.61	60.53	0.13
25	44.57	44.63	0.13	**32**	**56.86**	**56.58**	**0.49**	78	60.87	60.80	0.12
75	44.64	44.70	0.13	38	56.93	56.71	0.39	82	60.89	60.81	0.13
14	44.74	44.73	0.02	59	57.26	57.14	0.21	68	60.98	60.83	0.25
84	45.06	45.12	0.13	56	57.31	57.21	0.17	60	61.38	61.30	0.13
12	45.76	45.81	0.11	57	57.41	57.27	0.24	67	61.39	61.32	0.11
4	46.27	46.30	0.06	55	57.53	57.36	0.3	9	61.50	61.38	0.2
2	46.59	46.58	0.02	80	57.67	57.57	0.17	27	61.59	61.44	0.24
43	47.56	47.52	0.08	49	57.71	57.63	0.14	86	61.64	61.50	0.23
85	47.57	47.63	0.13	79	57.92	57.92	0.00	7	61.74	61.66	0.13
26	48.38	48.39	0.02	69	58.19	57.96	0.40	66	61.80	61.72	0.13
29	48.54	48.57	0.06	90	58.26	58.20	0.10	88	61.96	61.78	0.29
28	48.55	48.59	0.08	40	58.31	58.24	0.12	50	62.45	62.40	0.08
52	48.92	48.96	0.08	39	58.38	58.31	0.12	23	62.68	62.55	0.21
13	49.24	49.21	0.06	6	58.60	58.43	0.29	5	62.82	62.78	0.06
24	50.04	50.03	0.02	33	58.78	58.65	0.22	35	62.87	62.80	0.11
53	50.71	50.73	0.04	44	58.83	58.75	0.14	10	62.96	62.82	0.22
15	50.77	50.75	0.04	83	58.84	58.85	0.02	41	63.04	62.86	0.29
54	51.39	51.44	0.10	42	58.92	58.92	0.00	48	63.91	63.90	0.02

phase-to-ground fault contingencies in *System* 1. The x-axis denotes the fault duration ranging from 100 ms to 300 ms, and the y-axis is the fault locations at *Bus* 1 to 90, which are generator buses. As mentioned, the ASM results below zero represent the unstable conditions, and therefore, the whole system may come to an insecure state if a three-phase-to-ground fault lasting more than 250 ms occurs at *Bus* 17. Fig. 4.6 (b) demonstrates the frequencies after 9 s of the overload happening on the load number 1 to 90 with various overload percentages. It shows that the entire system is insecure regardless of which bus is overloaded by more than 80% for 9 s.

Aiming at demonstrating the accuracy of the proposed FTRT emulation, Table 4.2 gives the contingency screening results and errors for 90 300-ms three-phase-to-ground faults at each generator bus. The relative errors given in Table 4.2 are calculated by the following

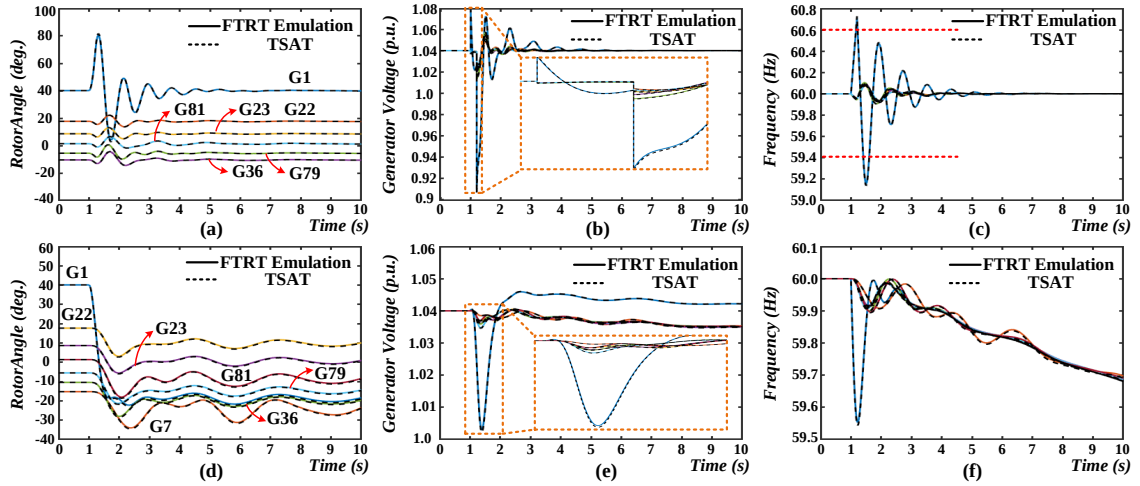

Figure 4.7: FTRT emulation results: (a) generator rotor angles under open circuit on *Bus* 1, (b) generator output voltages under open circuit on *Bus* 1, (c) generator frequencies under open circuit on *Bus* 1, (d) generator rotor angles under generation reduction on *Generator* 1, (e) generator output voltages under generation reduction on *Generator* 1, (f) generator frequencies under generation reduction on *Generator* 1.

formula:

$$\epsilon = \frac{abs(ASM_{FTRT} - ASM_{TSAT})}{abs(ASM_{TSAT})} \times 100\%, \tag{4.7}$$

The maximum relative error among the 90 contingencies is 0.49 %, which thoroughly demonstrates the accuracy of the proposed method.

4.3.3 Case 2: Purely AC grid

In Case 2, the 6-T HVDC system is omitted, and a single ACTIVSg 500-bus system is taken into consideration. The utilization of the integrated FPGA platform enable six contingencies to run concurrently in the FTRT emulation platform with 277 FTRT ratios. The dynamic emulation results are provided in Fig. 4.7, where Fig. 4.7 (a)-(c) refer to an open circuit lasting 180 ms occurs at 1 s on generator *Bus* 1. The emulation results indicate that the system is under stable condition after the fault is cleared. Meanwhile, Fig. 4.7 (d)-(f) show the emulation results of 90% generation reduction on *Generator* 1. Fig. 4.7 (f) indicates that the frequencies of synchronous generators keep decreasing and cannot be restored.

Fig. 4.8 (a) gives the ASM results for 1890 open circuit contingencies that occur on each generator bus under various fault duration, which demonstrates that the entire system is more likely to be insecure with a longer fault. Fig. 4.8 (b) provides 900 ASM results for various generation reduction percentages of each generator. Although the ASM results show that the system is secure, the frequencies after the generation reduction will not be restored without extra power injection as given in Fig. 4.7 (f). It indicates that the proposed DSA platform may reveal more potential risks with the utilization of time-domain emulation. The contingency screening results for 90 open circuit faults are given in Table 4.3.

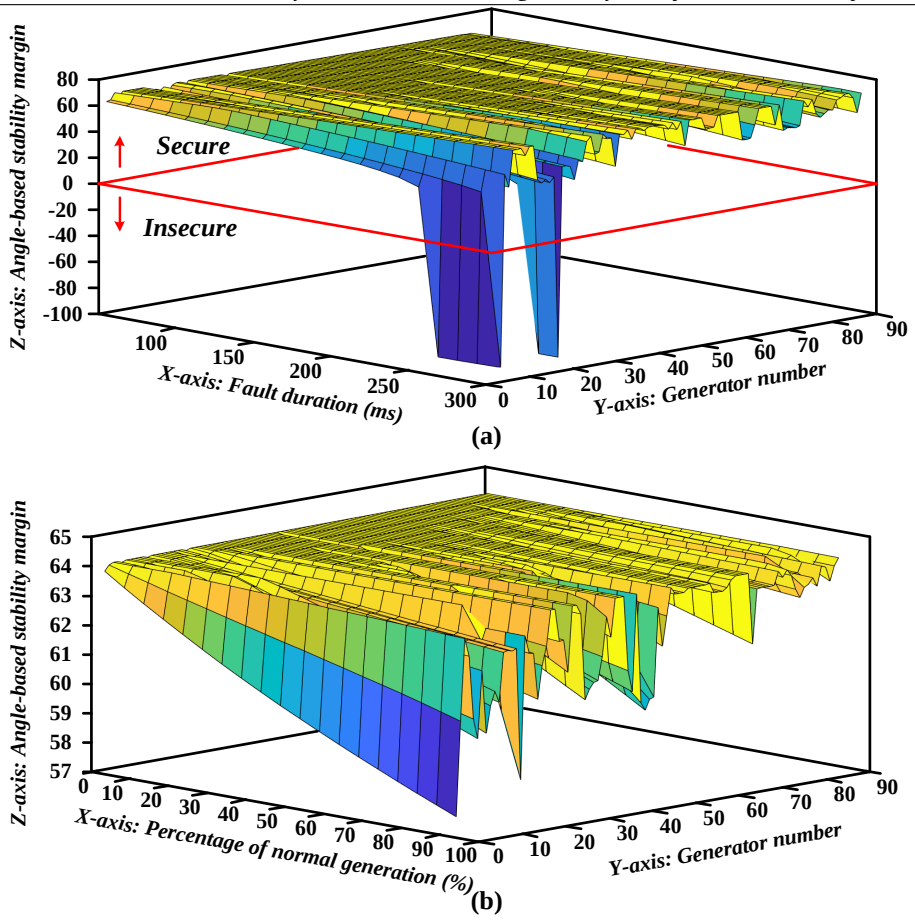

Figure 4.8: Dynamic security indices of extensive contingencies: (a) ASM results of open circuit contingencies, (b) frequencies of generation reduction contingencies.

The maximum relative error is merely 0.81%, which demonstrates that the accuracy of the proposed FTRT emulation is suitable for online DSA in the energy control center.

4.3.4 Accuracy Validation

In order to validate the the accuracy of the proposed modeling and hardware implementation approaches, an underdamped case is emulated. Fig. 4.9 (a)-(c) provide the emulation results for an underdamped excitation system, where the PSSs for all synchronous generators have been removed. At $t = 1s$, a three-phase-to-ground fault lasting 180 ms occurs on *Bus* 17, the generator rotor angles start to oscillate without recovery. The zoomed-in plots in Fig. 4.9 (a)-(c) demonstrate that the FTRT emulation results are matched well with the results calculated from TSAT in an underdamped system.

Furthermore, the emulation results are also provided to validate the accuracy of the proposed FTRT emulation under a three-phase-to-ground fault which is cleared near the critical clearing time (CCT), as given in Fig. 4.9 (d)-(f). As Fig. 4.6 (a) shows the CCT of the three-phase-to-ground fault at the bus of *Bus* 17 is 250 ms. Therefore, Fig. 4.9 (d)-(f)

Table 4.3: Contingency screening results and errors for 300ms open circuit faults on generators in System 1

Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)	Fault Gen.	ASM FTRT	ASM TSAT®	Error (%)
2	-88.18	-87.66	0.59	26	55.46	55.48	0.04	38	67.52	67.53	0.01
16	-86.96	-87.34	0.44	81	56.32	56.16	0.28	58	67.52	67.54	0.03
1	**-86.17**	**-86.88**	**0.82**	64	56.41	56.34	0.12	56	67.54	67.56	0.03
20	38.51	38.61	0.26	79	56.85	56.8	0.09	55	67.54	67.56	0.03
14	39.42	39.36	0.15	83	57.53	57.55	0.03	57	67.54	67.57	0.04
12	40.07	40.11	0.10	82	58.35	58.23	0.21	59	67.55	67.57	0.03
4	40.99	41.03	0.10	52	59.06	58.83	0.39	65	67.56	67.59	0.04
13	42.25	42.13	0.28	53	59.65	59.39	0.44	76	67.59	67.61	0.03
11	42.67	42.73	0.14	54	59.88	59.6	0.47	60	67.6	67.61	0.01
15	43.09	42.96	0.30	34	60.54	60.8	0.43	87	67.64	67.66	0.03
30	43.32	43.25	0.16	8	61.68	61.82	0.23	40	67.66	67.67	0.01
62	46.85	46.79	0.13	45	62.17	62.36	0.30	86	67.67	67.67	0.00
61	46.99	46.91	0.17	77	63.0	62.88	0.19	39	67.67	67.67	0.00
63	47.29	47.26	0.06	43	63.54	63.56	0.03	44	67.67	67.7	0.04
19	48.48	48.41	0.14	88	63.63	63.96	0.52	46	67.7	67.7	0.00
71	48.95	48.92	0.06	28	64.24	64.03	0.33	27	67.7	67.71	0.01
74	49.28	49.29	0.02	29	64.25	64.03	0.34	36	67.74	67.74	0.00
17	49.37	49.37	0.00	84	64.46	64.43	0.05	78	67.74	67.75	0.01
18	49.57	49.58	0.02	23	64.74	64.54	0.31	9	67.75	67.75	0.00
47	49.83	49.8	0.06	32	64.97	65.07	0.15	50	67.75	67.75	0.00
73	49.86	49.87	0.02	37	65.41	65.56	0.23	51	67.75	67.75	0.00
72	50.29	50.3	0.02	85	65.56	65.66	0.15	24	67.75	67.75	0.00
75	50.31	50.33	0.04	31	65.72	65.74	0.03	70	67.75	67.75	0.00
22	50.51	50.45	0.12	90	66.5	66.48	0.03	33	67.76	67.75	0.01
3	50.62	50.58	0.08	42	66.94	66.88	0.09	10	67.76	67.76	0.00
21	52.67	52.58	0.17	5	67.01	67.15	0.21	35	67.76	67.76	0.00
89	52.84	52.85	0.02	6	67.1	67.19	0.13	48	67.76	67.76	0.00
69	53.9	53.82	0.15	41	67.23	67.32	0.13	68	67.76	67.76	0.00
80	54.01	53.92	0.17	49	67.27	67.4	0.19	67	67.76	67.76	0.00
25	54.44	54.42	0.04	7	67.51	67.49	0.03	66	67.77	67.77	0.00

provides the emulation results of a three-phase-to-ground fault lasting 249 ms at *Bus* 17. Fig. 4.9 (d)-(f) indicate that the fault causes a severe oscillation including rotor angles, bus voltages, and frequencies. The zoomed-in plots demonstrated the accuracy of the proposed FTRT emulation can still be guaranteed even when the fault is cleared near the CCT. Meanwhile, the ASM results for two serious three-phase-to-ground faults calculated from FTRT emulation and TSAT are provided in Table 4.4, which indicates that the accuracy of the proposed method can be guaranteed for the contingencies that are cleared around the CCT.

The emulation time-step Δt is another important factor, which could influence the performance and accuracy of the FTRT emulation. As mentioned, 1 ms is utilized in the AC grid for DSA, while the time-step of 200 μs is adopted in the HVDC part for EMT emulation. The adoption of 200 μs is justified by the type of study in this work, where the

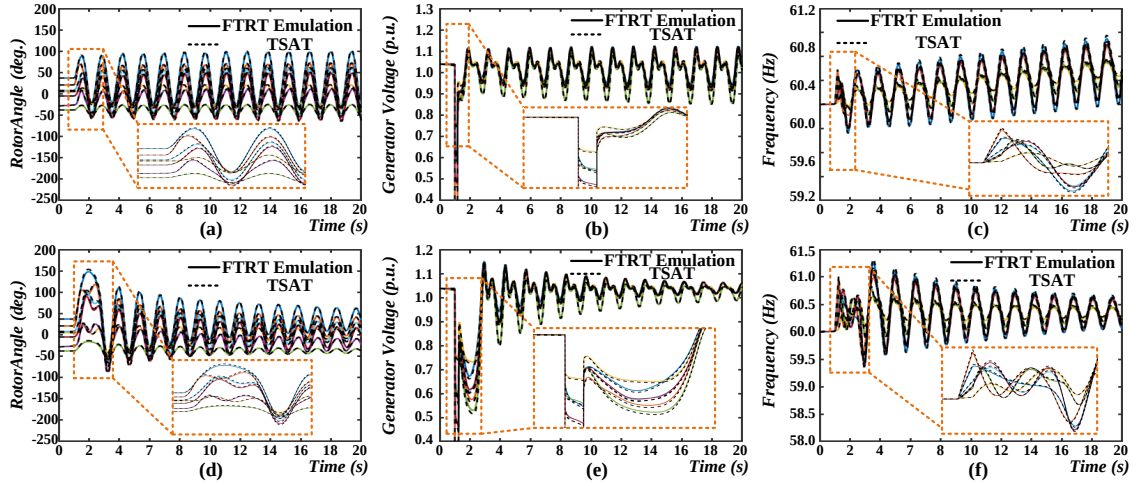

Figure 4.9: Three-phase-to-ground fault for underdamped synchronous generators: (a) generator rotor angles, (b) generator output voltages, (c) generator frequencies; FTRT emulation results of three-phase-to-ground fault lasting 249 ms: (d) generator rotor angles, (e) generator output voltages, (f) generator frequencies.

Table 4.4: ASM results for three-phase-to-ground faults cleared near the CCT.

Fault Bus (*Bus* 17)				Fault Bus (*Bus* 20)			
Fault Dur.	ASM FTRT	ASM TSAT®	Error (%)	Fault Dur.	ASM FTRT	ASM TSAT®	Error (%)
248 ms	39.09	39.15	-0.10	295 ms	39.22	39.22	0.00
249 ms	36.22	36.28	-0.16	296 ms	36.62	36.61	0.03
250 ms	**-83.92**	**-83.78**	**0.17**	297 ms	-85.16	-85.12	0.05
251 ms	-85.41	-85.35	0.07	298 ms	-86.12	-86.07	0.07

converter system-level dynamics such as output power and reactive power, instead of the converter electromagnetic transient details, are the main focus. In the dynamic security assessment, the commonly used time-step ranges from 1 ms to 10 ms. A dramatic computational advantage can be achieved with the time-step of 200 μs, and a $\frac{200\mu s}{96\times 10ns} = 208$ FTRT ratio can be obtained. On the other hand, with the time-step of 50 μs, the FTRT emulation can still be achieved, given as $\frac{50\mu s}{96\times 10ns} = 52$. The emulation results of output active power of the *MMC* 1 and 3 under various time-steps and relative errors are given in Fig. 4.10.

Fig. 4.10 (b) indicates that there is no significant improvement in emulation accuracy under the time-step of 50 μs. However, the acceleration has a significant drop if 50 μs is adopted. Therefore, after a trade-off between the emulation accuracy and computational speed, the 200 μs is selected as the emulation time-step of the HVDC grid.

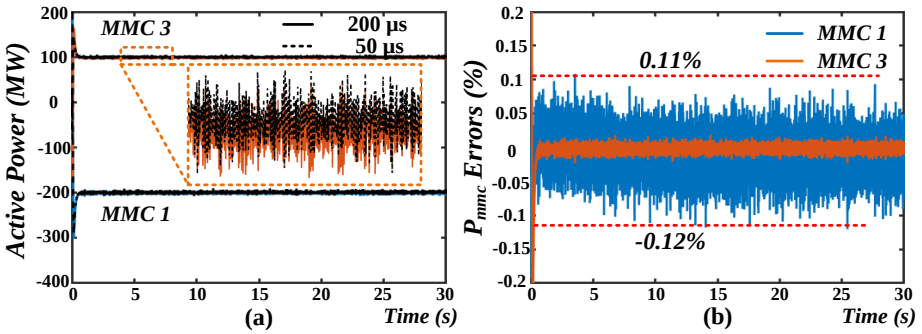

Figure 4.10: FTRT emulation results: (a) active power of MMC 1 and 3 under different time-steps, (b) relative errors.

4.4 Summary

A screening strategy of extensive contingencies in FTRT mode of execution for a comprehensive dynamic security analysis of large-scale integrated AC-DC grid is proposed in this chapter. Due to the pipelined hardware design method and parallelism of AC-DC grid modules, the EMT and TS co-simulation is introduced to provide more detailed operation conditions of the integrated AC-DC grid for dynamic security analysis. A dynamic voltage injection interface for AC-DC grid is proposed, which enables the EMT and TS co-simulation executing as one program without updating the admittance matrix in every time-step. The proposed interface strategy is also suitable for the data communication among FPGA boards as its less data transferred, which can further accelerate the FTRT emulation by reducing the communication delay. An FTRT ratio of 208 can be obtained for the hybrid AC-DC grid, while the FTRT ratio is over 277 times for a pure AC system. The contingency screening results of the more than 5500 contingencies from the FTRT DSA hardware emulation platform are well matched with those of TSAT® off-line simulation. Therefore, a guaranteed accuracy and execution speed of the proposed FTRT emulation methodology suggest its importance in planning and operation of a practical power system in scenarios such as online DSA.

5

FTRT Hardware Emulation of Dynamics of a Grid of Microgrids

Enhanced environmental standards are leading to an increasing proportion of microgrids (MGs) being integrated with renewable energy resources in modern power systems, which brings new challenges to simulate such a complex system. In this chapter, the comprehensive modeling of microgrids for faster-than-real-time (FTRT) emulation on FPGA boards is proposed, which can not only provide real-time HIL simulation services for testing local MG control and protection functions, but also enable the energy control center with effective strategies to improve the stability and security of the larger grid. It is quite challenging, even for real-time HIL simulation, to model and emulate a microgrid cluster. Due to its accelerated mode of execution, an FTRT emulator can conduct traditional control center functions such as dynamic state estimation, power flow, and contingency analysis much faster to predict the system condition in response to adverse events. It can then run multiple scenarios in parallel to devise and recommend viable solutions to dynamically restore the voltages and frequencies to nominal values.

For a realistic power system, the role of the FTRT emulation might be more prominent, as it is able to collect real-time data from the field and provide an optimal solution without cutting off the fault area. FTRT emulation improves the grid stability by predicting the grid performance, which is beyond the capability of real-time (RT) simulation tools [146]. Furthermore, the FPGAs require lower cost and power consumption compared with RT tools, enabling them to be of service in dynamic security assessment (DSA). With the help of creative solution algorithm and efficient parallel implementation, FTRT emulation can provide sufficient time for DSA to take remedial actions [67].

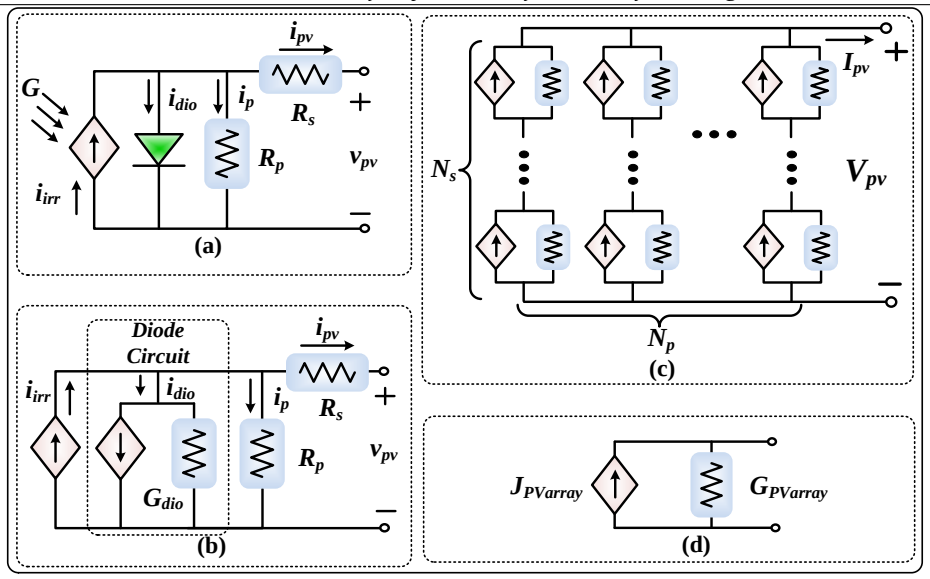

Figure 5.1: Configuration of a PV array model.

5.1 Detailed EMT Modeling of Microgrid Components

5.1.1 Photovoltaic (PV) and Battery Energy Storage System (BESS) EMT Model

Fig. 5.1 (a) provides the equivalent circuit representation of a solar cell, which consists of an irradiance-dependent current source, an anti-parallel diode, shunt resistor (R_p), and series resistor (R_s) [147]. The output current of the single solar cell can be expressed based on Kirchhoff's Current Law as:

$$i_{pv} = i_{irr} - i_{dio} - i_p, \tag{5.1}$$

where i_{irr} and i_{dio} refer to the irradiance current and the current flowing through the anti-parallel diode as given in (5.2) and (5.3), respectively.

$$i_{irr} = i_{irr,ref} \cdot \frac{G}{G_{ref}}[1 + \alpha_T \cdot (T - Tref)], \tag{5.2}$$

$$i_{dio}(t) = I_0 \cdot (e^{\frac{v_{dio}(t)}{V_T}} - 1), \tag{5.3}$$

where the variables with the subscription ref are the reference values, G denotes the solar irradiance, α_T refers to the temperature coefficient, V_T is the thermal voltage, and T represents the absolute temperature. Meanwhile, I_0 is the diode saturation current.

In a practical PV array, a large amount of PV panels are arranged in an array to provide sufficient energy. The topology of a typical PV array with N_p parallel strings and each of them containing N_s series panels is given in Fig. 5.1 (c). The equivalent circuit is still

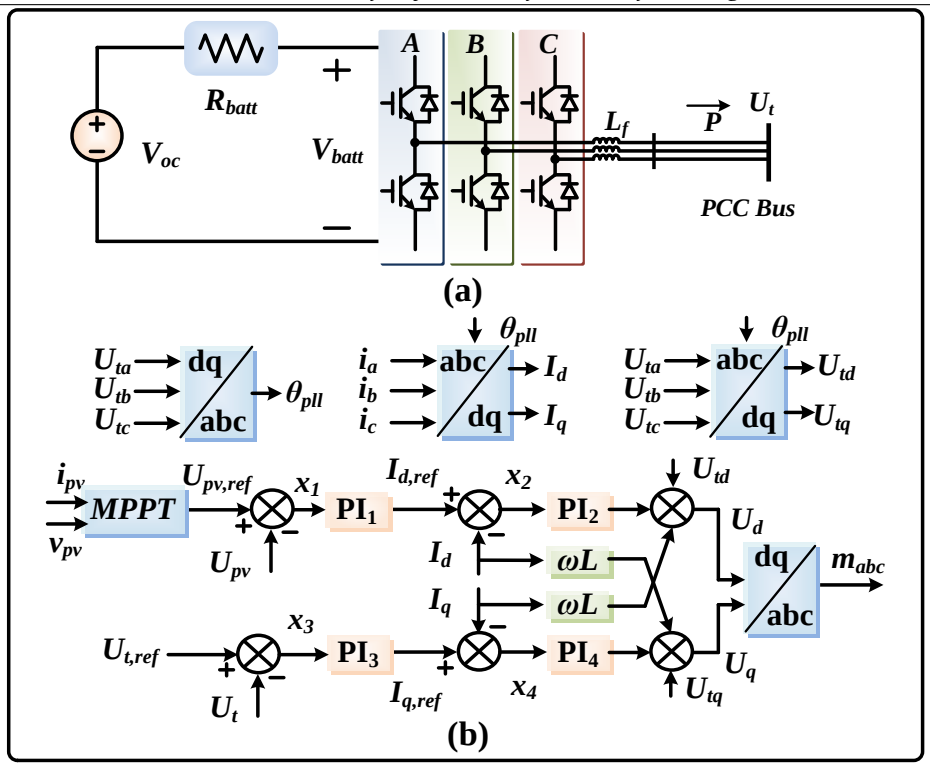

Figure 5.2: (a) Equivalent circuit of BESS, and (b) control strategy of PV&BESS inverter.

available in a PV array, where the (5.1) can be expanded as

$$I_{pv} = N_p i_{irr} - N_p I_0 (e^{\frac{V_{pv}(t)+N_s N_p^{-1} R_s I_{pv}(t)}{N_s V_T}} - 1) - \frac{I_{pv}(t) R_s + N_p N_s^{-1} V_{pv}(t)}{R_p}. \tag{5.4}$$

The non-linear nature of the anti-parallel diode makes the emulation of the solar cell complex. To reduce the computational burden as well as shrink the emulation time. The equivalent circuit in Fig. 5.1 (c) can be further simplified by Norton's Theorem, resulting in a two-node circuit as given in Fig. 5.1 (d), where

$$G_{PVarray} = \frac{N_p(G_{dio}+G_p)}{N_s(G_{dio}R_s+R_sG_p)+N_s}, \tag{5.5}$$

$$J_{PVarray} = \frac{N_p(i_{irr}-I_{Deq})}{G_{dio}R_s+R_sG_p+1}, \tag{5.6}$$

where G_p refers to the conductance of the parallel resistor, the G_{dio} and I_{Deq} are given as follows:

$$G_{dio} = \frac{\partial i_{dio}}{\partial v_{dio}} = \frac{I_0 \cdot e^{\frac{v_{dio}(t)}{V_T}}}{V_T}, \tag{5.7}$$

$$I_{Deq} = i_{dio} - G_{dio} \cdot v_{dio}. \tag{5.8}$$

The operation of a microgrid under the islanded mode requires energy storage system to balance the generation and demand as well as regulate the grid voltage. A battery energy storage system (BESS) is applied in each microgrid, which contains a battery system,

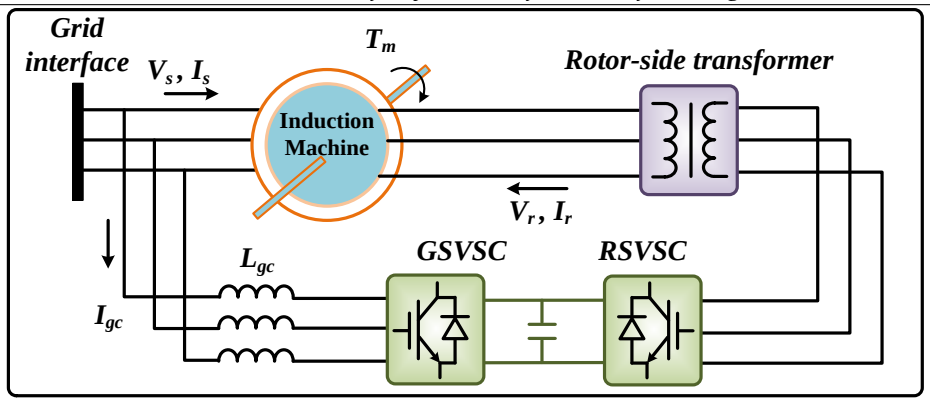

Figure 5.3: Topology of a typical DFIG.

and a DC/AC converter. To emulate the non-linear part of the battery system, the EMT simulation is applied for calculating BESS. The battery is modeled [83] as an ideal controllable voltage source in series with an equivalent internal resistance R_{batt}, as given in Fig. 5.2 (a). The open-circuit voltage of the battery V_{oc} can be represented based on the actual battery charge (it) by a non-linear equation expressed as follows.

$$V_{oc} = V_0 - K\frac{Q}{Q - it} \cdot it + A \cdot exp(-B(it)), \tag{5.9}$$

where V_0 refers to the battery constant voltage, K is the polarisation voltage, Q represents the battery capacity, and A and B denote exponential zone amplitude and exponential zone time constant inverse, respectively. According to Kirchhoff's laws, the battery voltage (V_{batt}) can be derived as:

$$V_{batt} = V_{oc} - I_{batt}R_{batt}, \tag{5.10}$$

The controllers of the PV system and BESS also share some similarities since they are both based on the d-q frame, as given in Fig. 5.2 (b). For a PV converter, the controller regulates the DC voltage on the d-axis according to the reference voltage which is generated by the maximum power point tracking (MPPT) algorithm, while in BESS, the DC voltage or the active power is the control target. On the q-axis, depending on the grid condition, the converters can control either the PCC voltage or its reactive power.

5.1.2 EMT Model of Wind Turbine

A typical doubly-fed induction generator (DFIG) is applied in the microgrid as shown in Fig. 5.3, which includes an induction machine, a grid side voltage source converter (GSVSC), and a rotor side voltage source converter (RSVSC). The principle of the DFIG is that the rotor windings are fed with a back-to-back voltage source converter which controls the rotor and grid currents, while the stator windings are connected to the grid. The converter controls the rotor currents, which is possible to adjust the active and reactive power fed to the gird under various wind speed and grid conditions.

For FTRT hardware emulation, the induction machine in the DFIG is represented by 5^{th} order differential algebraic equations (DAEs). The state-space equation of the induction machine can be expressed as:

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A} \cdot \mathbf{x}(t) + \mathbf{B} \cdot \mathbf{u}(t), \tag{5.11}$$

$$\mathbf{y}(t) = \mathbf{C} \cdot \mathbf{x}(t), \tag{5.12}$$

where $\mathbf{x}$, $\mathbf{y}$, and $\mathbf{u}$ are vectors that refer to the fluxes, currents, and input voltages, respectively. The DAEs of the induction machine contains 4 rotor and stator circuit equations in the α-β frame [148], given as:

$$\dot{\lambda_{\alpha s}}(t) = \frac{-L_r R_s \lambda_{\alpha s}(t)}{L_s L_r - L_m^2} + \frac{L_m R_s \lambda_{\alpha r}(t)}{L_s L_r - L_m^2} + V_{\beta s}, \tag{5.13}$$

$$\dot{\lambda_{\beta s}}(t) = \frac{-L_r R_s \lambda_{\beta s}(t)}{L_s L_r - L_m^2} + \frac{L_m R_s \lambda_{\beta r}(t)}{L_s L_r - L_m^2} + V_{\alpha s}, \tag{5.14}$$

$$\dot{\lambda_{\alpha r}}(t) = \frac{L_m R_r \lambda_{\alpha s}(t)}{L_s L_r - L_m^2} + \frac{-L_s R_r \lambda_{\alpha r}(t)}{L_s L_r - L_m^2} - \omega_r \lambda_{\beta r}(t), \tag{5.15}$$

$$\dot{\lambda_{\beta r}}(t) = \frac{L_m R_r \lambda_{\beta s}(t)}{L_s L_r - L_m^2} + \frac{-L_s R_r \lambda_{\beta r}(t)}{L_s L_r - L_m^2} + \omega_r \lambda_{\alpha r}(t), \tag{5.16}$$

where the $\lambda_{\alpha s}$, $\lambda_{\beta s}$, $\lambda_{\alpha r}$, and $\lambda_{\beta r}$ refer to the fluxes of stator and rotor in α-β frame, respectively, $V_{\alpha s}$ and $V_{\beta s}$ are the input voltages, R_s and R_r are the stator and rotor resistance, and L_s, L_r, and L_m represent the stator, rotor, and magnetizing inductance, respectively.

The 5th differential equation which describes the mechanical dynamics is given as

$$\dot{\omega_r}(t) = \frac{P}{2J} \cdot (T_e(t) - T_m(t)), \tag{5.17}$$

where P and J are constant values which refer to the poles and inertia of the induction machine, ω_r refers to the electrical angular velocity. The electromagnetic torque T_e and mechanical torque T_m can be obtained by

$$T_e(t) = \frac{3}{2} P (i_{\beta s}(t) \lambda_{\alpha s}(t) - i_{\alpha s}(t) \lambda_{\beta s}(t)), \tag{5.18}$$

$$T_m(t) = \frac{1}{2} \rho \pi r_T^3 v_w^2 F(r_T, v_w, \omega_r), \tag{5.19}$$

where ρ represents the air density, r_T is the wind turbine radius, and F refers to a non-linear function of ω_r, r_T, and the wind speed v_w, where the detailed function F can be found in [141]. The stator currents $i_{\alpha s}$ and $i_{\beta s}$ are calculated from (5.12), where the vector $\mathbf{y}$ can be expanded as

$$\mathbf{y} = [i_{\alpha s}(t), i_{\beta s}(t), i_{\alpha r}(t), i_{\beta r}(t)]^T, \tag{5.20}$$

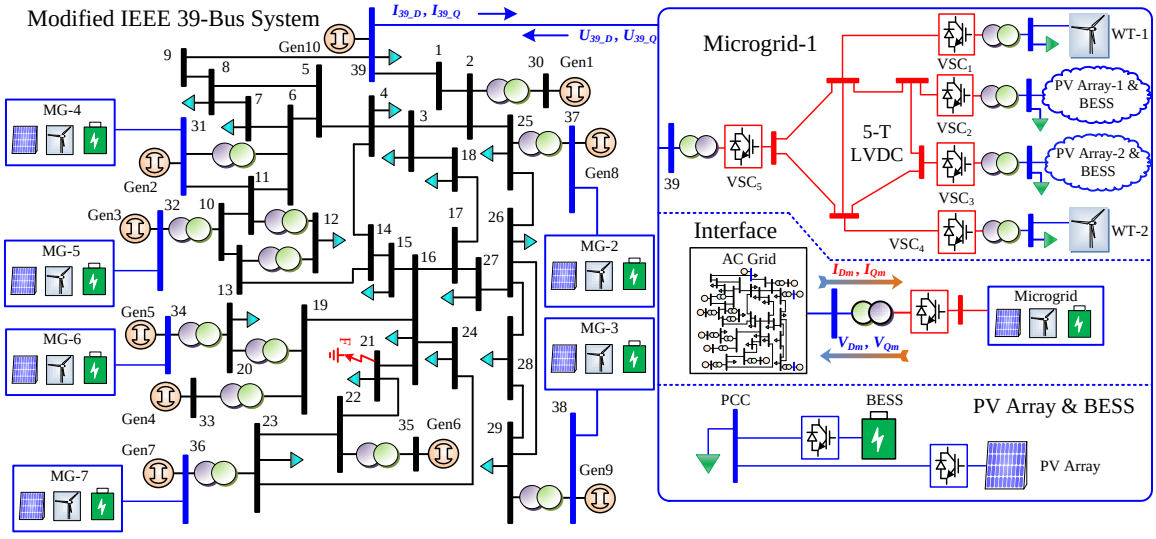

Figure 5.4: Topology of the host grid connected with multiple microgrids.

the corresponding coefficient matrix $\mathbf{C}$ can be expressed as

$$\mathbf{C} = \begin{bmatrix} \frac{L_r}{L_s L_r - L_m^2} & 0 & \frac{-L_m}{L_s L_r - L_m^2} & 0 \\ 0 & \frac{L_r}{L_s L_r - L_m^2} & 0 & \frac{-L_m}{L_s L_r - L_m^2} \\ \frac{-L_m}{L_s L_r - L_m^2} & 0 & \frac{L_s}{L_s L_r - L_m^2} & 0 \\ 0 & \frac{-L_m}{L_s L_r - L_m^2} & 0 & \frac{L_s}{L_s L_r - L_m^2} \end{bmatrix}, \tag{5.21}$$

The continuous differential equations should be discretized before the numerical calculation. The corresponding time-discrete for (5.11) can be obtained after utilizing the trapezoidal rule:

$$\mathbf{x}(t+\Delta t) = (\mathbf{I} - \mathbf{A}\frac{\Delta t}{2})^{-1}[(\mathbf{I} + \mathbf{A}\frac{\Delta t}{2})\mathbf{x}(t)] + \mathbf{B}\frac{\Delta t}{2}(\mathbf{u}(t+\Delta t) + \mathbf{u}(t))], \tag{5.22}$$

where Δt refers to the time-step of the EMT emulation utilized in the wind turbine, which is defined as 50 μs, and $\mathbf{x}(t+\Delta t)$ denotes the vector of state variables of next time-step.

5.2 AC Grid Modeling and Interface Strategy

Fig. 5.4 shows a modified IEEE 39-bus system [145] integrated with seven DC microgrids, where the wind turbine (WT) and PV-BESS system in each microgrid are linked to a five terminal (5-T) MVDC system. Under a base power of 1 MVA for the host grid, each wind turbine has a rated 2 $p.u.$ active power, both PV and BESS have a standard 1 $p.u.$ rated power, and local loads of 500 kW and 1 MW are connected with the PV-BESS system and WT, respectively. When a microgrid operates under the islanded mode, the generated power from the renewable energy is utilized for supporting the local loads, while the extra active power is stored in the batteries. On the other hand, in the grid-connected mode, each microgrid provides up to 3 MW active power to the host system.

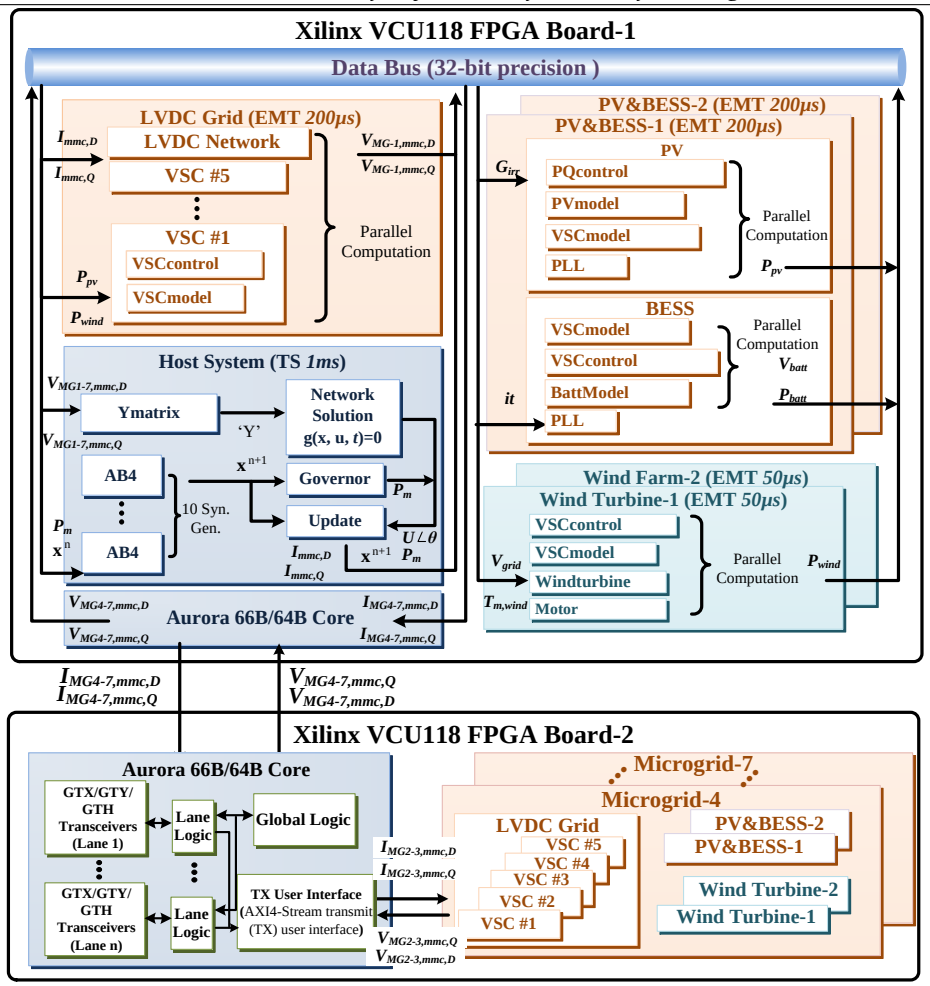

Figure 5.5: Hardware block design for FTRT emulation of the host system integrated with 7 microgrids.

TS simulation is also adopted to solve the AC grid. The 9^{th}-order DAEs are utilized for representing the synchronous generators of the proposed AC system, which are solved by the explicit 4^{th}-order Adams-Bashforth (AB4) given as:

$$x(t+h) = x(t) + \frac{h}{24} \cdot [55F(t) - 59F(t-h) + 37F(t-2h) - 9F(t-3h)], \tag{5.23}$$

where h refers to the time-step of AC grid, which is defined as 1 ms. Meanwhile, the voltage injection strategy between microgrids and AC grid is adopted, which is given in 4.1.2.

5.3 FTRT Hardware Emulation of Grid of Microgrids on FPGAs

The full deployment of the AC system integrated with the microgrid cluster requires two Xilinx Virtex® UltraScale+™ VCU118 boards containing XCVU9P FPGA which includes

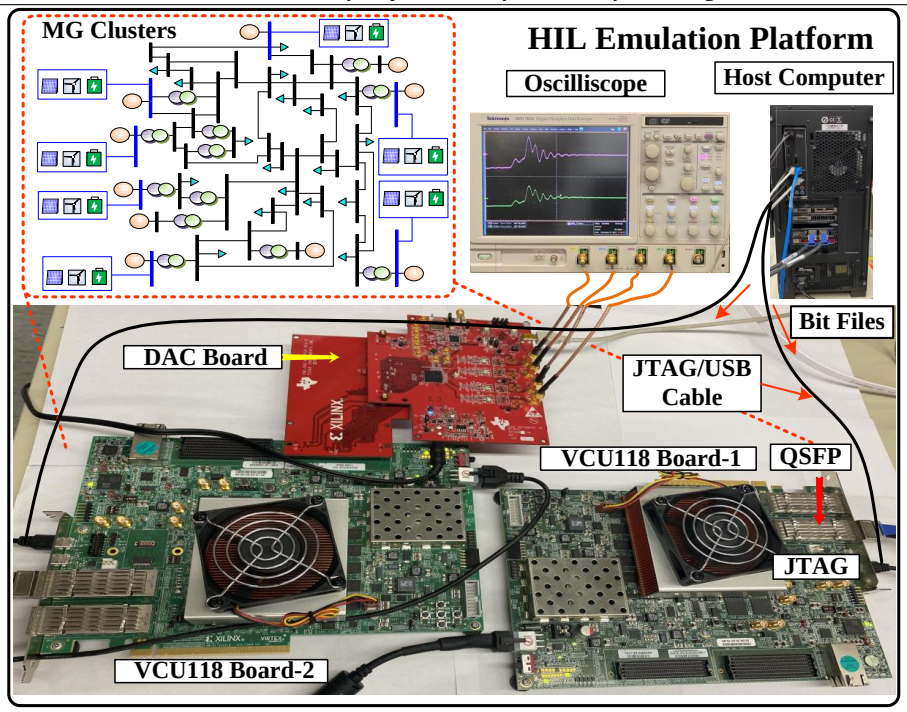

Figure 5.6: Experimental hardware-in-the-loop (HIL) emulation platform.

6840 DSP slices, 1182240 look-up tables (LUTs), and 2364480 flip-flops (FFs). The host system as well as the microgrid-1 (MG-1) to MG-3 in Fig. 5.4 are deployed on the VCU118 Board-1, and the remaining four microgrids are implemented on the VCU118 Board-2. The sufficient hardware resources enable the MGs to be executed on the FPGA board in FTRT mode. The reconfigurability of FPGAs allows the hardware resources to be adjusted to accommodate and represent practical systems [136], and therefore it is suitable for the hardware-in-the-loop (HIL) emulation and dynamic security assessment in the energy control center.

The circuit parts and subsystems which consist of the microgrid cluster are programmed in C/C++ code before the hardware design. The Xilinx® high-level synthesis software Vivado HLS® is able to transform the C/C++ code into intellectual property (IP) which contains corresponding input/output ports in VHDL format. After IP generation, each circuit component is converted to a hardware module and exported to Vivado® for block design. In a practical real-time application, data exchange is realized by connecting the input/output ports among the hardware modules. According to the correlation among the subfunctions, the hardware modules are designed to be calculated in parallel or series. The hardware block design and the data stream are provided in Fig. 5.5. After design synthesis and device mapping, the bitstreams were downloaded to the target FPGA boards via the Joint Test Action Group (JTAG) interface as given in Fig. 5.6. The Quad Small Form Pluggable (QSFP) interfaces are connected with cable and the build-in IP Aurora 66B/64B

Table 5.1: Details of major microgrid cluster hardware modules

Module	Latency	BRAM	DSP	FF	LUT
PV array on VCU118 ($100MHz$)					
PVmodel	39 T_{clk}	0	19	3329	11493
PQcontrol	32 T_{clk}	0	22	3497	8418
VSCmodel	41 T_{clk}	0	33	4489	9447
PLL	18 T_{clk}	0	8	892	1357
BESS on VCU118 ($100MHz$)					
BattModel	73 T_{clk}	0	44	2923	7497
VSCmodel	31 T_{clk}	0	34	3244	4673
VSCcontrol	28 T_{clk}	0	32	3450	5931
PLL	18 T_{clk}	0	8	892	1357
Wind turbine on VCU118 ($100MHz$)					
Windturbine	83 T_{clk}	0	43	5085	8929
Motor	79 T_{clk}	0	66	5128	9219
VSCcontrol	97 T_{clk}	18	196	13255	30652
VSCmodel	86 T_{clk}	0	38	3454	3752
LVDC system on VCU118 ($100MHz$)					
PQcontrol	45 T_{clk}	0	62	4398	5372
VSCmodel	96 T_{clk}	0	16	2582	5270
LVDCNetwork	73 T_{clk}	0	17	2209	2868
IEEE 39-bus system on VCU118 ($100MHz$)					
AB4	33 T_{clk}	0	36	2048	2547
Network	196 T_{clk}	16	678	48921	54732
Governor	29 T_{clk}	0	17	3783	4598
Update	21 T_{clk}	0	35	3639	3970
VCU118 Board-1	–	2.87%	82.16%	22.57%	82.52%
VCU118 Board-2	–	3.33%	85.32%	23.84%	95.35%
Available hardware resources					
VCU118	–	4320	6840	2364480	1182240

core is utilized to realize the data communication. Due to the little data required of the proposed AC/Microgrid interface, the PCC voltages and currents in D-Q frame are chosen as the communication data between the FPGA boards. Meanwhile, the output digital data is transferred to analog data via the digital-to-analogic converter (DAC) board, so that the waveforms can be displayed on the oscilloscope.

Table 5.1 provides the hardware resource utilization and the latencies of the hardware modules in the FTRT emulation. As mentioned, the components in the microgrid including the PV array, wind turbine, and LVDC system are modeled by EMT emulation. The hardware modules of PV stations are fully parallelized, and therefore, the total latency of a PV system is 41 $Tclk$. The execution time of the PV array is calculated as $41 \times 10ns = 0.41\mu s$, where the clock cycle is defined as 10 ns under the FPGA frequency of 100 MHz. Then the FTRT ratio can be expressed as $\frac{200\mu s}{0.41\mu s} = 487$. Similarly, due to the parallelism, the

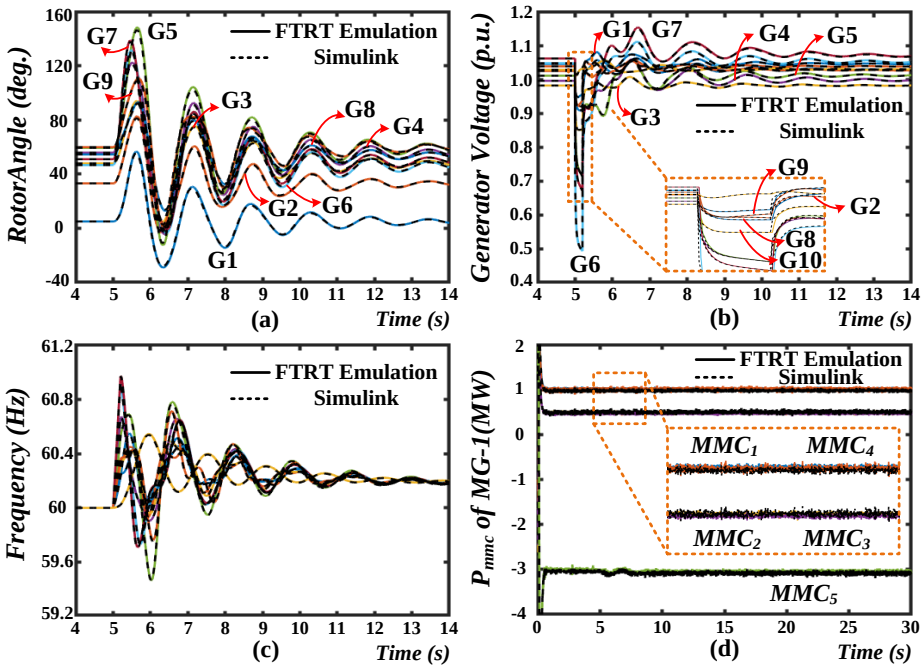

Figure 5.7: FTRT emulation results of three-phase-to-ground fault: (a) rotor angles, (b) generator voltages (G6-G9), (c) generator frequencies, (d) output power of MMCs in MG-1.

FTRT ratios of the BESS, wind turbine, and DC system can be solved as $\frac{200\mu s}{73\times 10ns} = 273$, $\frac{50\mu s}{97\times 10ns} = 51$, and $\frac{200\mu s}{96\times 10ns} = 208$, respectively. Meanwhile, the latency of the AC system is $33+196+29+21 = 279Tclk$, thus the FTRT ratio reaches over $\frac{1ms}{279\times 10ns} = 358$. Although a 358 FTRT ratio can be achieved in the transient stability emulation, the overall FTRT ratio is determined by the EMT emulation part, since the AC system should wait for the wind turbine part to finish computation to keep data synchronization. Therefore, the total FTRT ratio of the proposed microgrid cluster is about 51.

5.4 FTRT Emulation Results and Validation

The hardware emulation of the AC grid integrated with microgrid cluster is conducted on the FPGA-based FTRT platform (Fig. 5.6), and the proposed FTRT emulation and the interface strategy are validated by comparing the results with those of the off-line simulation tool Matlab/Simulink®.

5.4.1 Case 1: Three-Phase-to-Ground Fault

At $t = 5s$, the three-phase-to-ground fault lasting 200 ms occurs at *Bus* 21 as given in Fig. 5.4. The rotor angles, output voltages, and frequencies of the synchronous generators start to oscillate immediately, as given in Fig. 5.7 (a)-(c), where the dashed lines refer to the results from Simulink® and the solid lines represent the FTRT emulation results. Fig. 5.7

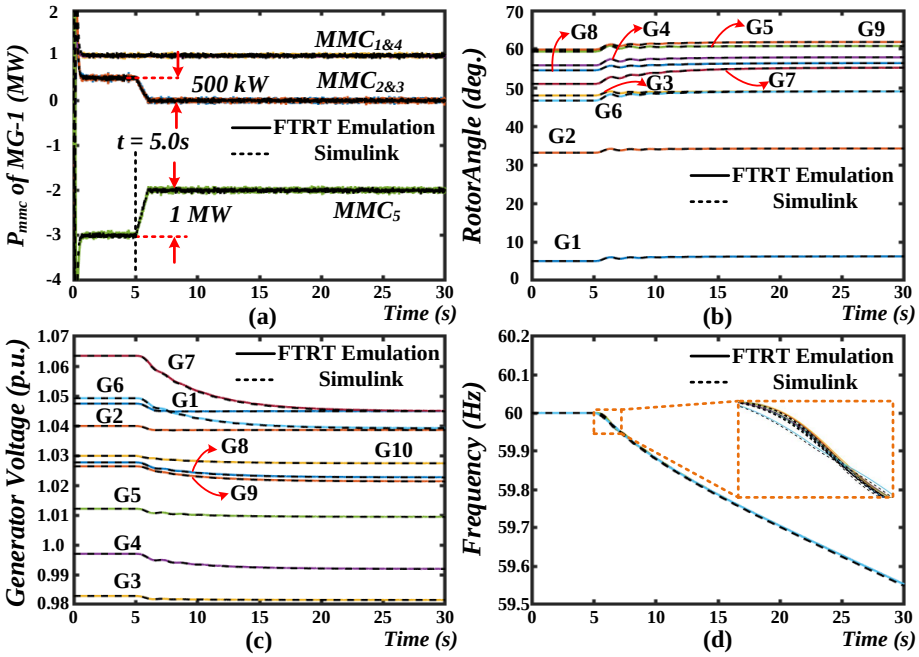

Figure 5.8: Impact of lack of power generation in PV array: (a) generator relative rotor angles, (b) generator voltages, (c) frequencies, (d) output power of MMCs in MG-1.

(d) provides the output power of the VSCs in MG-1, which indicates that the waveforms from the FTRT emulation match with those obtained from the off-line simulation. Since the output power of the PV-BESS systems and wind turbines maintain stability, there is no significant change of the active power injections at the PCC, as given in Fig. 5.7 (d).

5.4.2 Case 2: Microgrid Internal Power Balance

Since the output power of renewable energy is highly dependent on the environment, such as irradiations or wind speed, low power generation may occur and last for a long period in the microgrids. This case study focuses on the microgrid internal balance and the predictive control of the proposed FTRT emulation. At the time of $5s$, the output power of each PV array in MG-1 decreases by 500 kW, which induces a lack of power injection at *Bus* 39, as given in Fig. 5.8 (a). Although the rotor angles can restore to a new steady-state as given in Fig. 5.8 (b), the impacts of reduced generation are severe, including the significant drop of the generator voltages and the unrecoverable generator frequencies as shown in Fig. 5.8 (c) and (d).

With the 51 times faster than real-time execution, the FTRT emulation equipped in the energy control center comes up with an optimal power control strategy following the detection of the abnormal condition to mitigate the adverse impacts, as given in Fig. 5.9 (a). At $t = 7.8s$, each BESS in MG-1 provides extra 1 MW active power to the AC grid in $1s$ and lasts $1.2s$ until $t = 10.0s$, resulting in an extra active power injection of 2 MW

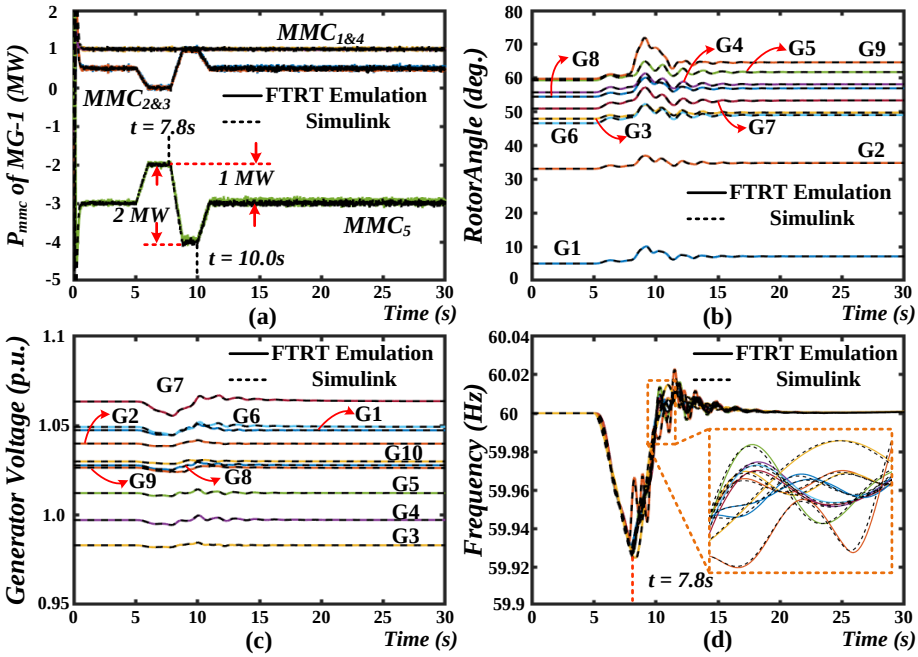

Figure 5.9: Microgrid internal power balance results: (a) generator relative rotor angles, (b) generator voltages, (c) frequencies, (d) output power of MMCs in MG-1.

from MG-1 to *Bus* 39. As a result, the frequencies start to recover as given in Fig. 5.9 (d). After 10s, MG-1 reduces the power injection from 4 MW to 3 MW, then the generator frequencies restore to 60 Hz, meanwhile, the rotor angles and generator voltages recover to the previous working conditions. The zoomed-in plots in Fig. 5.8 and 5.9 (d) indicate that the FTRT emulation results matched with the off-line simulation tool.

5.4.3 Case 3: Inter-MG Coordination

In this case, assuming that the BESS in MG-1 is fully charged and cannot store the extra power generated from the PV array, so that the MG-1 injects 1 MW into the AC grid, as given in Fig. 5.10 (a). It brings significant impacts on the stability of the host grid, including the rotor angles, bus voltages, especially the increasing generator frequencies, as shown in Fig. 5.10 (b)-(d). After the detection of the abnormal frequency, the energy control center emulates several power control contingencies and provides an optimal solution to mitigate the increasing frequencies.

At t=8.0s, both MG-2 and MG-3 start to take action, and each microgrid absorbs 1 MW active power, As a result, the generator frequencies start to decrease as given in Fig. 5.11 (a) and (d). At the time of 15.2s, MG-2 and MG-3 reduce the absorption power to 0.5 MW, and the frequencies start to recover and return to 60 Hz. Meanwhile, the rotor angles and the bus voltages of the AC grids stabilize in a new steady-state as shown in Fig. 5.11 (b) and (c). Meanwhile, the zoomed-in plots are also provided in Fig. 5.10 and 5.11 (d), which

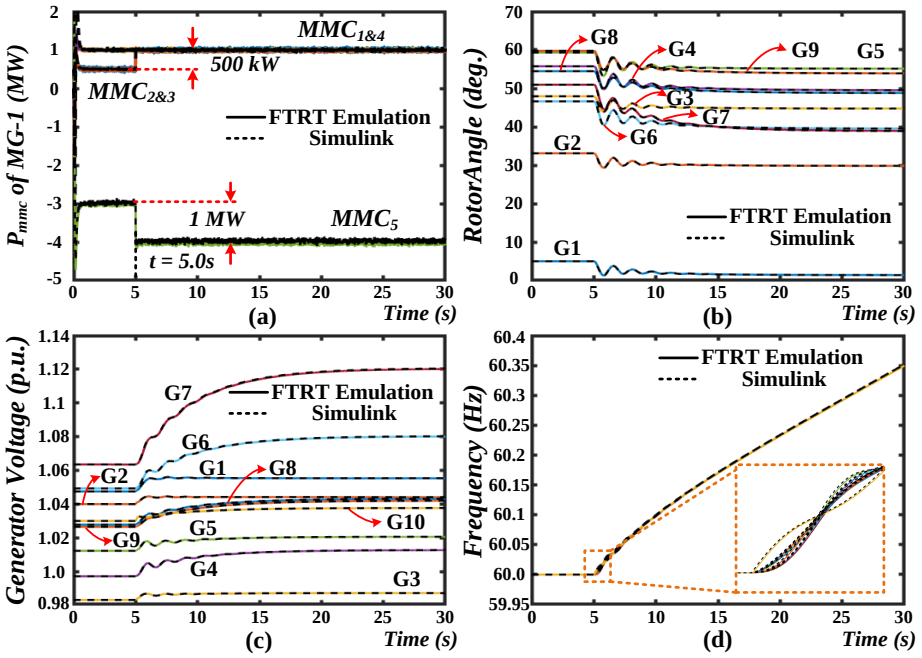

Figure 5.10: Impacts of excess power injection to the host grid: (a) generator relative rotor angles, (b) generator voltages, (c) frequencies, (d) output power of MMCs in MG-1.

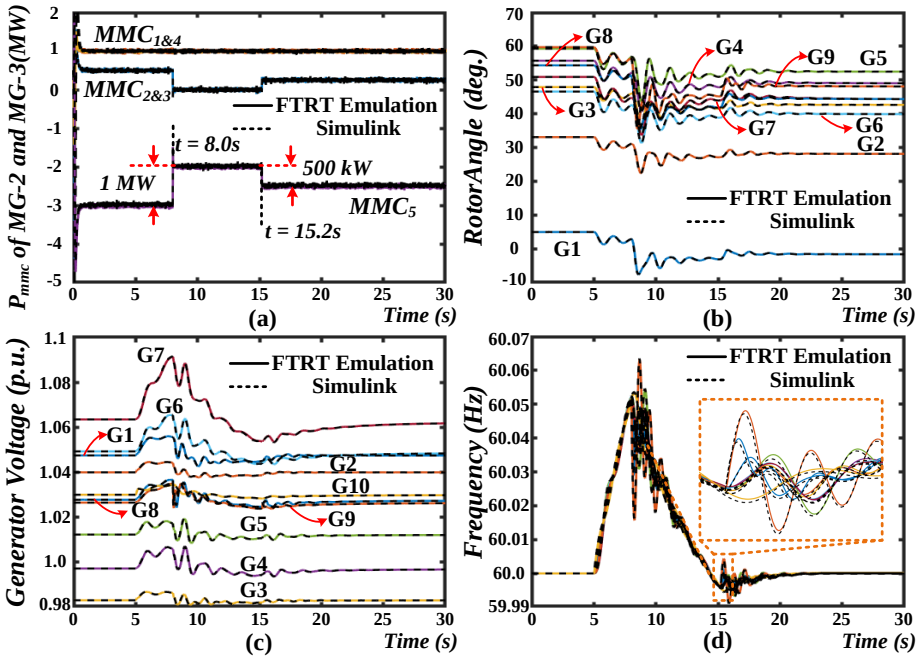

Figure 5.11: Inter-MG coordination results: (a) generator relative rotor angles, (b) generator voltages, (c) frequencies, (d) output power of MMCs in MG-1.

thoroughly demonstrates the accuracy of the proposed method.

5.5 Summary

This chapter proposed a comprehensive hardware-based faster-than-real-time dynamic emulation of a grid of microgrids to study the impact of their integration on the host system. Since different emulation types and time-steps are adopted for the AC grid and microgrids, a dynamic voltage injection interface strategy with less hardware utilization and lower latency is therefore proposed to enable the compatibility of EMT and TS models. Taking its inherent advantages of reconfigurability and parallelism, the FPGA-based hardware platform allows emulating the integrated microgrid cluster with an execution speed over 51 times faster than real-time. Meanwhile, an active power dispatch is emulated to deal with the various working conditions of the microgrids. The time-domain results indicate that the proposed FTRT emulation is numerically stable and accurate compared with the off-line simulation. Furthermore, the dynamic security assessment can be carried out on the proposed FPGA-based FTRT platform with significant acceleration. The detailed comprehensive FTRT emulation is also suitable for analyzing other severe disturbances, which is meaningful for modern power systems with high penetration of renewable energy.

6

Machine Learning Based Dynamic System Equivalencing for FTRT Digital Twin

With the increasing size and complexity of modern power systems, the TS simulation requires considerable computational effort [105]. The commonly used security indices for a large-scale transmission network are obtained from TS simulations, which provide critical data for analyzing the system stability such as rotor angles, bus voltages, and frequencies. The current industry practice is able to accelerate the TS simulation in real-time execution due to the availability of the high-performance hardware [106]. However, the existing solutions for TS simulation are based on the numerical solutions of model equations that represent the dynamic process of the nonlinear system components.

In the last few decades, dynamic equivalencing has been adopted for dealing with the large-scale systems for TS simulation, which divides the system into "study zone" where the dynamic phenomena occur and "external system" where the system part needs to be replaced [106]. The dynamic equivalent model is obtained by reducing the number of generator and the network nodes. Currently, the main approaches of dynamic equivalencing are largely classified into the following three directions: 1) Coherency methods [105], [107]-[110], which are achieved by replacing a coherent group of machines in the external system with an equivalent generator and attaching it to a common bus. 2) Modal methods [111]-[113], which focus on the less damped modes. The linear equivalents are obtained by applying reduction techniques that eliminate the high damped modes. Meanwhile, the modal methods are also cooperated with the coherency methods to identify the coherent groups [113]. 3) Estimation methods [115]- [118], which basically utilize measurements or simulation based results to estimate the parameters of the equivalent model.

Although valuable contributions have been made, the computational requirements are still heavy by the aforementioned approaches, such as the eigenvalue analysis, diagonal-

ization of the modal approach, or identification of the coherency groups. In this work, machine learning (ML) based dynamic equivalent models are proposed for both synchronous generator and external networks for TS emulation. Artificial neural network (ANN) based power system dynamic equivalencing has been previously proposed in [149]; however, traditional ANN-based equivalent models are relatively simple, and cannot meet the requirements for long-term prediction for a large-scale network. Therefore, the Gated Recurrent Unit (GRU) algorithm is utilized, which is a variant of the Long Short-Term Memory (LSTM) network that has a higher accuracy in representing the non-linear parts for dynamic equivalencing [150]. Although compared with ANN-based algorithms, the GRU-based dynamic equivalent model requires more hardware resources and inferencing time, these shortcomings can be effectively minimized by the FPGA. The reconfigurability of FPGAs enables each system component to be designed according to its function [136]. The proposed FTRT emulation can therefore operate as a digital twin of the real power system to predict its performance and provide remedial solutions after detection of a disturbance.

6.1 Part I: Machine Learning Based Modeling of Synchronous Generator

6.1.1 Transient Stability Problem

TS simulation is essentially analyzing the rotor-angle, voltage, and frequency stability of synchronous generators as stated in Section 2.1.1. The dynamics of generators and their auxiliary controllers are represented by a set of nonlinear differential-algebraic equations (DAEs), as given in (1.1) and (1.2).

To achieve a high accuracy, a detailed 17^{th}-order multi-mass synchronous generator model (SGM) is chosen as the training target for the ML-based SGM, which includes ten mechanical equations, four electrical equations consisting two windings on d-axis and two damping windings on q-axis. Meanwhile, an excitation system with three DAEs is also included. In addition to a five-mass torsional shaft system composed of the four-mass-turbine shaft connecting with the generator rotating shaft is applied for training the ML-based SGM.

6.1.2 Machine Learning Strategy

The most commonly used ML strategies can be largely classified into recurrent neural network (RNN) and convolutional neural network (CNN). The former has better performance than CNN regarding ML modeling of time-series signals because of its effectiveness and long-term prediction ability. Even though many newer applications of transform in natural language processing (NLP) have emerged in recent years, considering the features of the power system, hardware resource consumption, and latency, it is more efficient to utilize RNN with a more straightforward structure for ML modeling in this paper. The

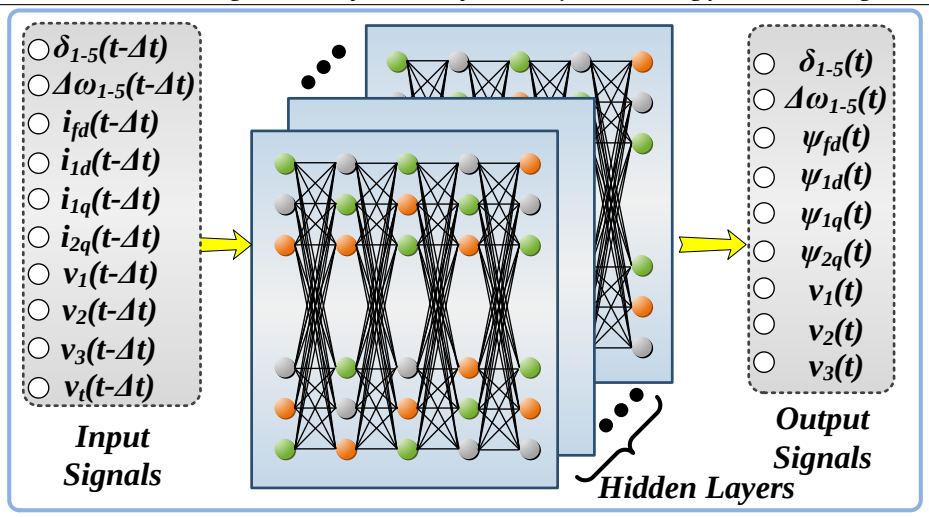

Figure 6.1: Lumped GRU model of synchronous generator.

complexity and accuracy of ANN, convolutional recurrent neural network (CRNN), GRU, and long short-term memory (LSTM) for modeling power electronic devices are compared in the literature [151]. GRU is a low-resource-consumption RNN with reasonably high accuracy, which is more accurate than ANN and CRNN, close to LSTM, but the resource consumption is much smaller than LSTM. There are four processes within GRU:

1) Update process: the update matrix $\mathbf{Z}$ is calculated by input $\mathbf{X}$ and previous state $\mathbf{H}^{t-1}$, as given below:

$$\mathbf{Z} = \sigma(\mathbf{W}_z[\mathbf{X}, \mathbf{H}^{t-1}] + \mathbf{B}_z). \tag{6.1}$$

GRU is assisted by the update gate in determining how much information from the previous and the present time-step should be transmitted into current state. It is quite important since the GRU may choose to replicate all previous information to minimize the risk of disappearing gradients.

2) Reset process:

$$\mathbf{R} = \sigma(\mathbf{W}_r[\mathbf{X}, \mathbf{H}^{t-1}] + \mathbf{B}_r), \tag{6.2}$$

where the reset matrix $\mathbf{R}$ is obtained from input $\mathbf{X}$ and previous state $\mathbf{H}^{t-1}$. This matrix $\mathbf{R}$ has the same equation as the update gate matrix $\mathbf{Z}$, but its parameters and applications are different. This gate is used to select how much of the past or current information to forget.

3) Current memory process:

$$\mathbf{H}_r^{t-1} = \mathbf{H}^{t-1}\mathbf{R}, \tag{6.3}$$

$$\mathbf{H}' = tanh(\mathbf{W}_h[\mathbf{X}, \mathbf{H}_r^{t-1}] + \mathbf{B}). \tag{6.4}$$

The previously acquired reset gate processes the historical information $\mathbf{H}^{t-1}$ to get $\mathbf{H}_r^{t-1}$, which determines the past information to be maintained and abandoned. Then, the current memory $\mathbf{H}'$ is constructed by the processed historical information and the current input $\mathbf{X}$, as shown in (6.4) where the hyperbolic tangent activation function is used.

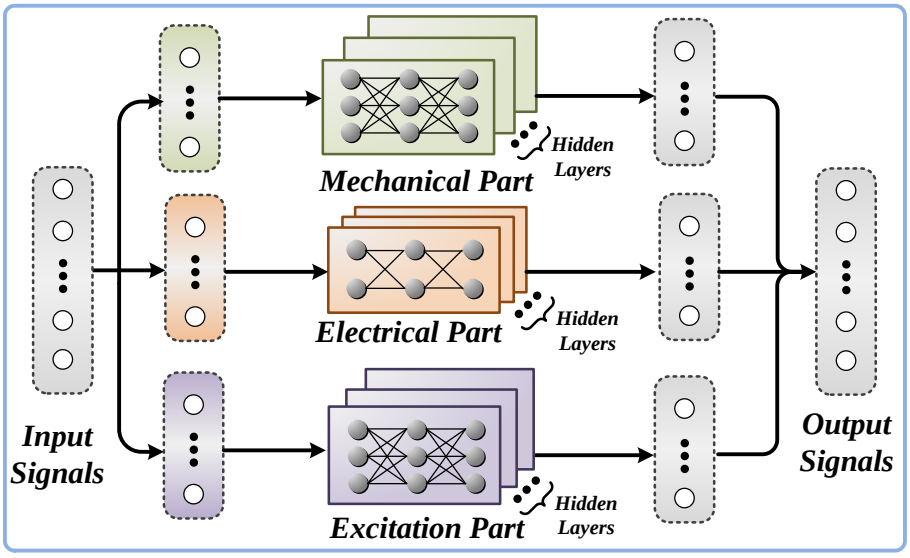

Figure 6.2: Partitioned GRU model of synchronous generator.

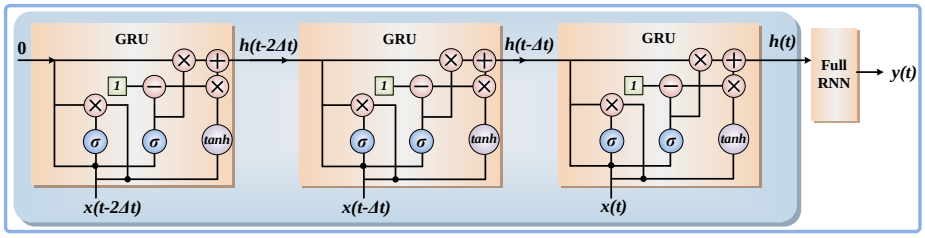

Figure 6.3: GRU structure for each part (mechanical, electrical, and excitation) of synchronous generator.

4) Final transfer memory process:

$$\mathbf{H}^t = \mathbf{Z}\mathbf{H}^{t-1} + (\mathbf{I} - \mathbf{Z})\mathbf{H}'. \tag{6.5}$$

$\mathbf{H}^t$, a vector that stores information from the current unit, is computed and passed on to the next unit. The update gate matrix $\mathbf{Z}$, which decides what information needs to be gathered in the current memory content $\mathbf{H}'$ and the prior time step $\mathbf{H}^{t-1}$, must be used in this procedure.

A lumped GRU model with inputs and outputs is depicted in Fig. 6.1, which may be developed without specific expertise. According to 3.1.1, the input vector $\mathbf{X}$ can be defined as:

$$\mathbf{X} = [\delta_{1-5}, \Delta\omega_{1-5}, i_{fd}, i_{1d}, i_{1q}, i_{2q}, v_1, v_2, v_3, v_t]^T. \tag{6.6}$$

Since the proposed GRU-SGM is conducted on the FPGA boards, the sequence length, hidden size, and layers that may influence the hardware resource consumption should be properly defined. In this work, the lumped model is divided into three parts depending on machine operation knowledge, as illustrated in Fig. 6.2. As for the three partitioned

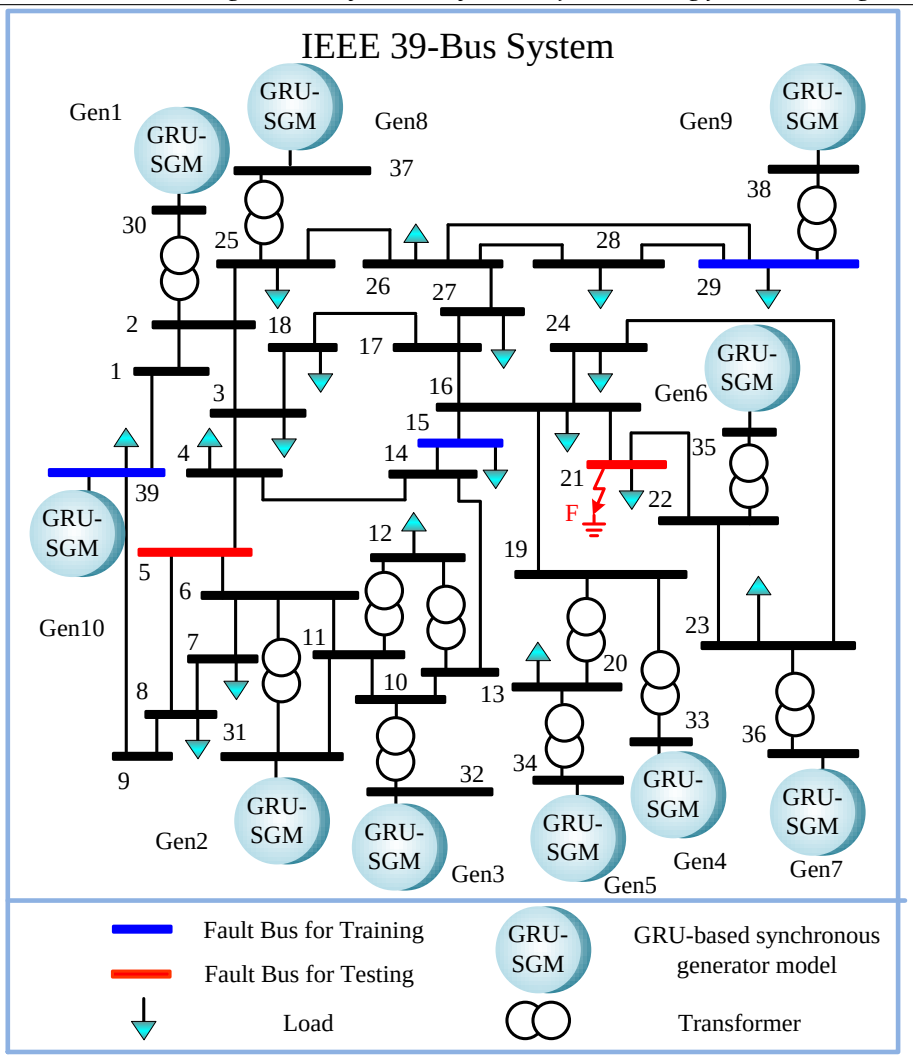

Figure 6.4: Topology of IEEE 39-bus system with ML-based synchronous generator models.

GRU parts of the SGM, Fig. 6.3 shows the structure of an unrolled GRU model, the layer number is one, and the sequence length is three for GRU-SGM.

The partitioned model enables the three portions to be calculated in parallel and thus lower the hide size, saving hardware resource usage and speeding up execution without compromising accuracy. And this division is based on expertise and has no bearing on accuracy. The GRU model of the mechanical part of the machine can be trained based on the input and output variables of (3.1)-(3.6). The GRU can then represent the current and flux linkage parts, in the same way as (2.3)-(2.6). In terms of excitation system, the effect of the third GRU model is similar to that of (2.7)-(2.9).

Table 6.1: Relative errors of rotor angles under various systems

System	Gen.	25 Epoch	50 Epoch	75 Epoch	100 Epoch
IEEE 39-bus	10	11.43%	5.93%	1.36%	**0.65%**
IEEE 118-bus	54	16.13%	8.03%	1.50%	0.94%
ACTIVSg 500-bus	90	13.35%	6.69%	1.39%	0.84%

6.1.3 Datasets and Training

Taking the IEEE 39-bus system for example, the training data is obtained from several three-phased to ground faults, as given in Fig. 6.4. Since the fault locations have significant impacts on the dynamics of generator state variables, the fault buses are chosen from closest to furthest, which are located at *Bus* 39, 15, and 29 for training the *Gen* 10.

The training data set comprises data on both normal and abnormal operating circumstances since the system includes a fault state. The model's input and output contain substantial variations; therefore, a data set with a wide range of variations is highly essential for GRU model training. In practice, 1 ms is chosen as the timestep, and a 20-second data set is captured. 70% of it is utilized for training, while the remaining 30% is used for testing. For the training of the GRU model, it is not necessary to input all the training data obtained into the program, which will result in the training time being too long. After shuffling the training data, the data processing program samples the data set at regular intervals and sends it to the training program so that the obtained data set ensures generality and dramatically reduces the size. Meanwhile, Adam algorithm [152] is chosen as an adaptive learning rate optimization method to minimize the errors during training processes.

The proposed models are trained in a 196-node cluster after GRU parameter design, where each node contains two Intel® Silver 4216 Cascade Lake central processing units (CPUs). The GRU models for each part of the synchronous machine cost about 8 h training on a cluster node requiring within 10 GB memory. Then, the training results, weights and bias of the GRU models, are obtained and saved in Pytorch framework.

6.1.4 Inferencing from the Trained Model

As mentioned, some tests have been done in the training process. Although these GRU models are optimized and elevated by the test datasets, they should be further tested by the practical application operation. The trained GRU-SGM is tested on a standard IEEE 39-bus system containing ten generators and validated by the offline simulation tool TSAT®. The accuracy of the proposed model is related to the epoch of training. Fig. 6.5 (a)-(c) provides the rotor angles of *Gen* 10 of a three-phase-to-ground fault at *Bus* 5, and 21 lasting 150 ms of various epoch numbers. The state variables $\Delta\omega_1$, ψ_{fd}, ψ_{1d}, ψ_{1q}, ψ_{2q}, and v_3 are also illustrated in Fig. 6.5 (c)-(h). The zoomed-in plots in Fig. 6.5 indicate that with

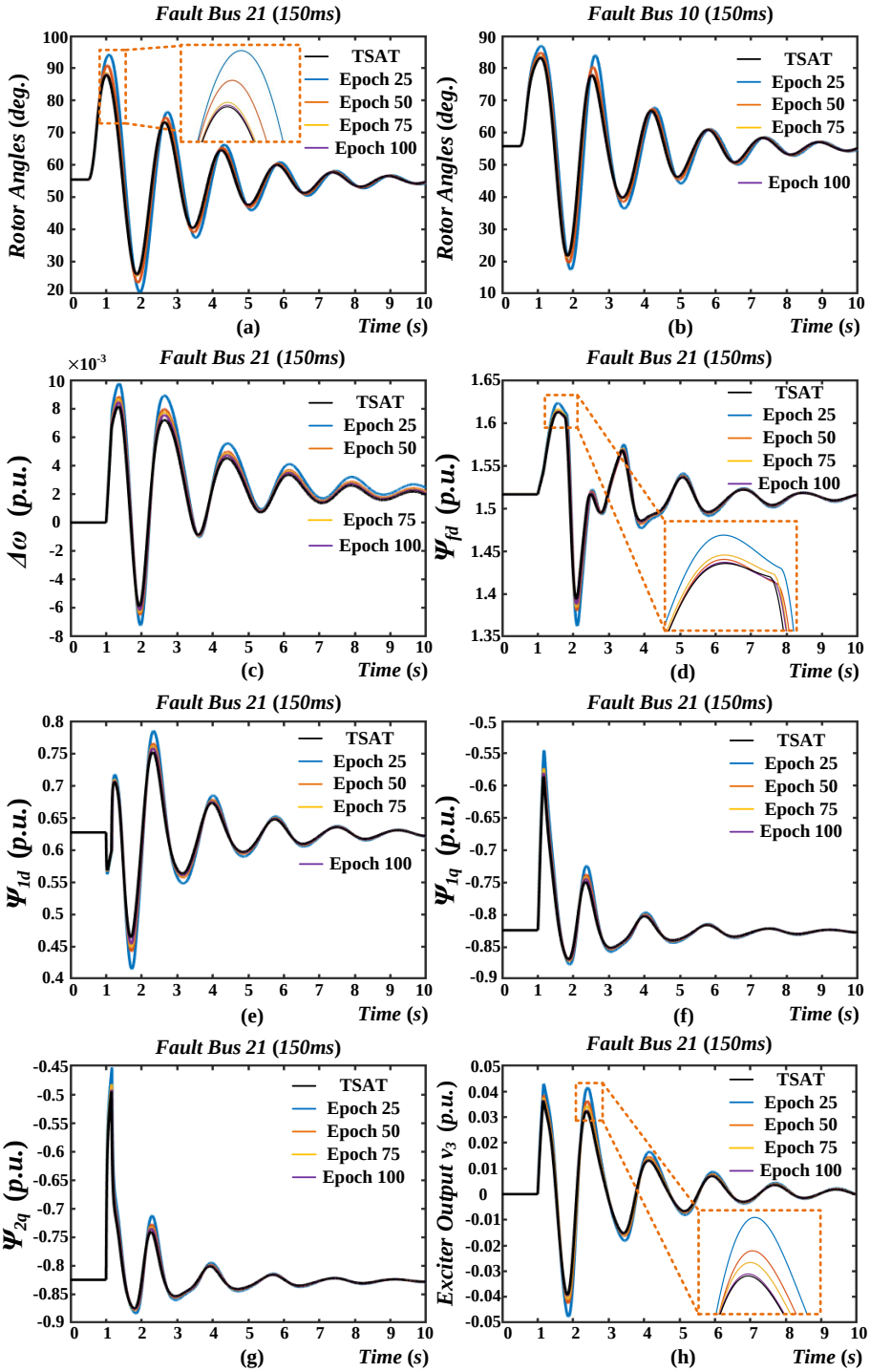

Figure 6.5: Outputs of *Gen* 10 under various epoch numbers: (a) rotor angles of a 150 ms fault at *Bus* 21, (b) rotor angles of a 150 ms fault at *Bus* 10, and results of a 150 ms fault at *Bus* 21: (c) $\Delta\omega_1$, (d) ψ_{fd}, (e) ψ_{1d}, (f) ψ_{1q}, (h) ψ_{2q}, and (f) v_3.

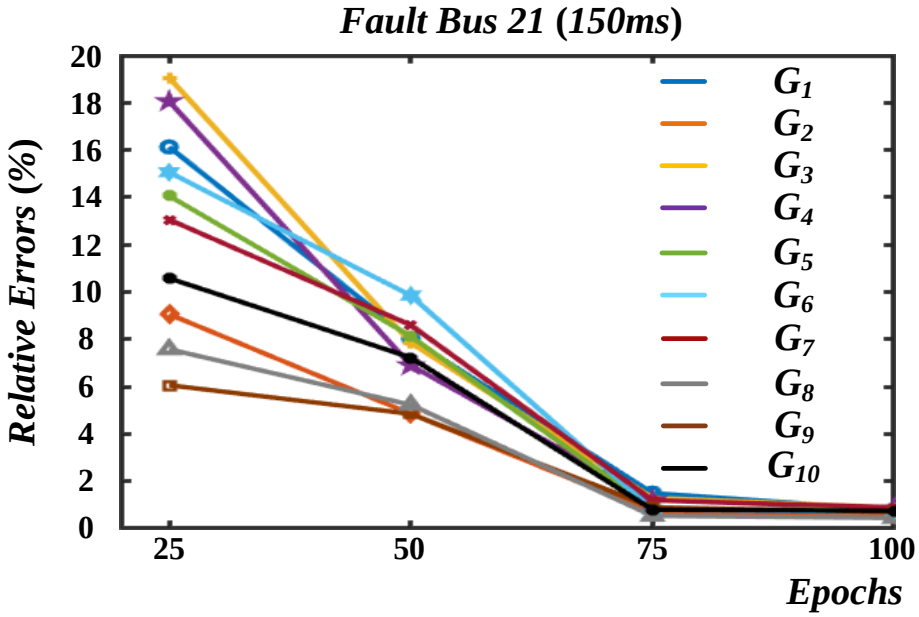

Figure 6.6: Relative errors of various training epochs.

the epoch number increasing the higher accuracy can be obtained. Meanwhile, to further demonstrate the accuracy of GRU-SGM for TS emulation, the relative errors of rotor angles from various generators under different epoch numbers are given in Fig. 6.6. The accuracy of the proposed model is illustrated by the relative errors which are calculated by the following formula:

$$\epsilon = \frac{|\delta_{GRU} - \delta_{TSAT}|}{\delta_{TSAT}} \times 100\%. \tag{6.7}$$

Fig. 6.6 and zoomed-in plots in Fig. 6.5 (a), (e), and (f) indicate that with the epoch number increasing the higher accuracy can be obtained. In order to test the generalization ability, the proposed SGM is also applied on other power transmission systems under various evaluation conditions that differ from the training datasets, as given in Table 6.1. Although the epoch number, and the subsequent networks would influence the accuracy of the trained model, the relative errors of GRU-SGM in various power systems are less than 1% after 100 epoch. And a minimum error of 0.65% can be obtained on the IEEE 39-bus system. Therefore, the accuracy can be guaranteed by the GRU method for dynamic security analysis.

Meanwhile, the GRU-based synchronous models are also executed on the Xilinx Virtex® UltraScale+™ VCU118 board containing XCVU9P FPGA to validated the efficiency of the proposed model. For the computational model, both the implicit Newton-Raphson (NR) method and explicit 4^{th}-order Runge-Kutta (RK4) method are adopted for calculating the 17^{th}-order DAEs. The hardware resource utilization and the latencies of various calculation strategies are provided in Table 6.2. The proposed GRU-SGM has significant advantages in resource consumption and execution time compared with NR method and RK4.

Table 6.2: Hardware resource occupation of various methods

Module	Latency	BRAM	DSP	FF	LUT
NR	1526 T_{clk}	18	1296	287589	338067
RK4	199 T_{clk}	16	315	29709	45721
GRU-SGM	146 T_{clk}	42	116	13058	17064
Network	269 T_{clk}	16	534	43928	57664
XCVU9P	–	4320	6840	2364480	1182240

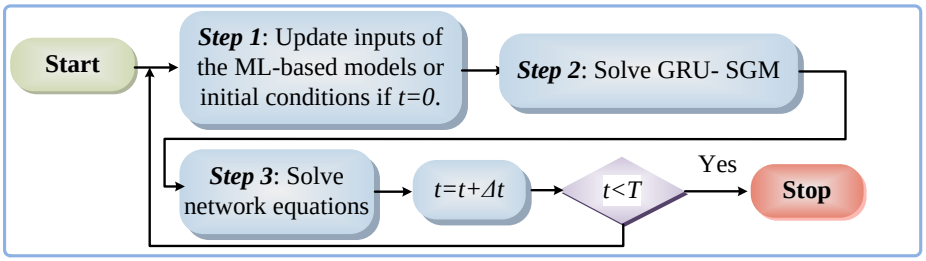

Figure 6.7: Procedure for the hybrid computational-ML based TS emulation.

Under the FPGA frequency of 100 MHz, the latency is defined in clock cycles which is 10 ns. An FTRT ratio of $\frac{1ms}{146\times10ns} = 684$ can be reached by applying the GRU-SGM. Then, the emulation procedure for the hybrid computational-ML based AC-DC grid is illustrated in Fig. 6.7.

6.2 Part II: Machine Learning Based Dynamic Equivalencing for Hybrid AC-DC Grid

The basic idea of dynamic equivalents for TS simulation is through the dynamic respond measurements to create an equivalent system that replaces a part of original system, where the equivalent models can be linear or nonlinear. In this section, an GRU-based dynamic equivalents is proposed, which replaces the conventional procedures of dynamic equivalencing.

The external system refers to a nonlinear dynamic system with generators, excitors, and loads, which is replaced by the dynamic equivalent model (DEM) using machine learning techniques. The internal system represents the area that need to be analyzed in details, which is also called as study zone. The key issues of the proposed GRU-based dynamic equivalents are the quality of selected input/output signals, and the interface strategy between external area and study zone.

6.2.1 Datasets and Training

The proposed GRU-based dynamic equivalent model is applied to a hybrid AC-DC grid, which contains fifteen ACTIVSg 500-bus systems and a fifteen terminal (15-T) HVDC grid,

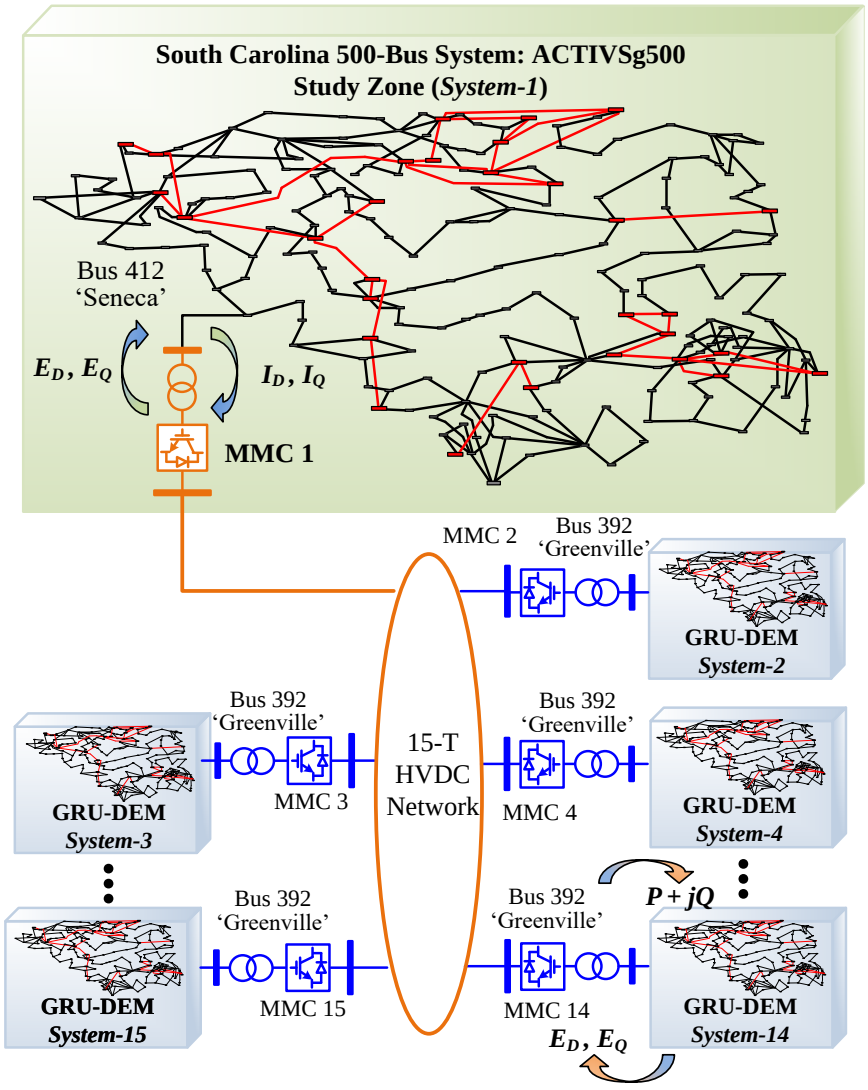

Figure 6.8: Hybrid computational-ML based test system of large-scale AC-DC grid.

as given in Fig. 6.8 (a). The modular multilevel converter (MMC) 1 is treated as rectifier station, which provides the dynamic power to the 15-T HVDC grid and the external systems. The 500-bus *System-1* is defined as the study zone, while the remaining fourteen 500-bus systems are replaced by the GRU-based dynamic equivalent model, as shown in Fig. 6.8. After a disturbance in study zone, the output current at *Bus* 412 starts to oscillate, and the oscillation will spread to the following external systems through the HVDC grid. Fig. 6.8 illustrates that the inverter stations provide dynamic $P+jQ$ loads to the external systems at the boundary buses. In return, the external systems modeled by GRU-DEM provide the point of common coupling (PCC) voltages to the DC grid in the same manner.

Due to the relatively small size of the measurement values at the boundary buses be-

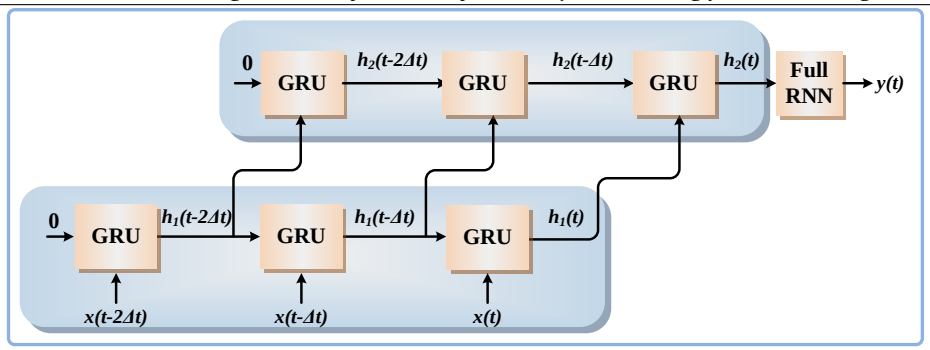

Figure 6.9: GRU structure for dynamic equivalent model of the external system.

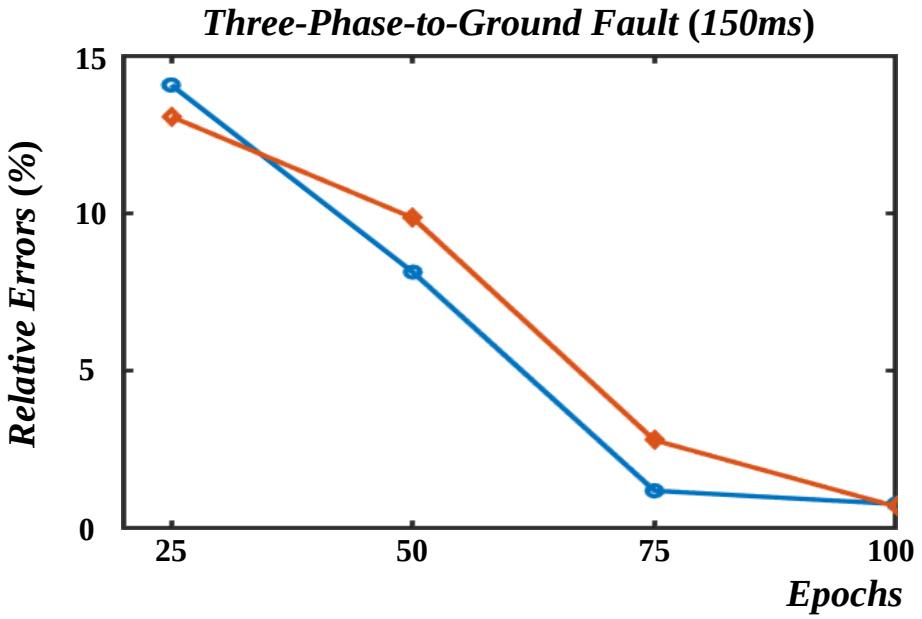

Figure 6.10: Relative errors of GRU-DEM under various training epochs.

tween the DC grid and DEM, the datasets have significant impacts on the accuracy of the equivalent results, and therefore, a large number of contingencies in the study zone need to be included. In this work, the three-phase-to-ground faults occur at 90 buses are simulated off-line to obtain the real and imaginary components of the boundary nodes power and voltages. Meanwhile, for those contingencies that are cleared around the critical clearing time (CCT), the simulation result is highly sensitive to the error. The fault durations ranging from 50 ms-240 ms are simulated for training GRU to guarantee the accuracy of the proposed dynamic equivalent model, which means there are 20 various fault durations are simulated on each bus with a step of 10 ms. Therefore, the results of 1800 contingencies are collected from the off-line simulation tool for training the GRU-DEM.

Although the structure of GRU-DEM is similar to that of the GRU-SGM, the hyperparameters (hidden size, the number of layers, etc.) are different. The GRU structure for

Table 6.3: Relative errors of GRU-DEM

Output Variables	25 Epoch	50 Epoch	75 Epoch	100 Epoch
E_D	14.06%	8.13%	1.21%	0.78%
E_Q	13.13%	9.85%	2.81%	0.70%

DEM is illustrated in Fig. 6.9, where the input vector $\mathbf{X}$ for GRU-DEM can be defined as:

$$\mathbf{X} = [P(t), Q(t), P(t-\Delta t), Q(t-\Delta t), P(t-2\Delta t), Q(t-2\Delta t)]^T. \tag{6.8}$$

Due to the complexity of the 500-bus system and the relatively small size of input data, the GRU-based model for DEM should increase much more hidden neurons (100 for DEM system), and the number of layers is two instead. With this comes increased data requirements. Nevertheless, the chosen auto-learning-rate optimization method, Adam algorithm [152], still works for this GRU-based model, and the training process costs about 30 h in one cluster node. Once one GRU-DEM system is trained and tested, other GRU-DEM systems can be trained simultaneously in the cluster. In order to further demonstrated the accuracy of GRU-DEM, the relative errors under various epochs are illustrated in Fig. 6.10. Meanwhile, Table 6.3 indicates that the accuracy of proposed GRU-DEM can be guaranteed after 100 epochs.

6.2.2 Interface Strategy of Hybrid Computational-ML based Dynamic System Equivalencing

Since the DC grid undergoes the EMT simulation and the TS simulation is applied on the 500-bus *System-1* in the study zone, it would be impractical to take the two types of simulation model running compatible instantly. Meanwhile, the generators of *System-1* applies the GRU-SGM while the remaining 500-bus systems are represented by the GRU-DEM. An interface strategy should be designed properly at the boundary buses. As illustrated in Fig. 6.8, the DC grid provide PCC voltage in D-Q frame to the AC system, while the TS simulation part provide current to the rectifier station. Therefore, from the AC system point of view, the DC grid can be simplified as a dynamic voltage source interconnecting with the network equations. The DC grid provide the PCC voltage to the network, resulting in the non-zero value at the boundary bus. The network equation can be expanded as

$$\begin{bmatrix} \mathbf{I_i^{ML}} \\ I_b^{DC} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{ii}} & \mathbf{Y_{ib}} \\ \mathbf{Y_{bi}} & Y_{bb} \end{bmatrix} \begin{bmatrix} \mathbf{E_i^{ML}} \\ E_b^{DC} \end{bmatrix}, \tag{6.9}$$

where the subscript i is the generator nodes that are represented by the ML-based SGM, the superscript DC represents the variables coming from DC grid, and b refers to the boundary node of AC and DC grids which is *Bus* 412 in the study zone. As the PCC voltage calculated by the HVDC grid in D- and Q- axis are already known, the current injection at the boundary bus can be derived as a complex matrix equations.

$$I_b^{DC} = \mathbf{Y_{bi}} \mathbf{E_i^{ML}} + Y_{bb} E_b^{DC}. \tag{6.10}$$

As mentioned, the generator voltages $\mathbf{E_i^{ML}}$ are not directly known after solving the GRU-DEM, the relationship between generator voltages and currents can be expressed in (2.16). Obviously, the only unknown vector in (6.9) is I_b^{DC}, and therefore, the output current at the boundary bus can be solved and is sent to DC grid to keep the EMT emulation going on. The hardware emulation procedure of the AC-DC grid digital twin is similar to that of the IEEE 39-bus system as given in Fig. 6.7, where the *Step 2* is replaced by solving the MMC AVM and GRU-DEM/SGM.

6.3 Digital Twin Hardware Emulation for Hybrid AC-DC Grid

The FTRT emulation of the large-scale AC-DC grid with proposed GRU-DEM is realized on the integrated Xilinx Virtex® UltraScale+™ FPGA platform as shown in Fig. 6.11, which includes two VCU118 boards containing XCVU9P FPGA, two VCU128 boards featuring XCVU37P FPGA, and a Xilinx Alveo U250 acceleration card equipped with Alveo U250 FPGA. The detailed computational model of the study zone and the 15-T HVDC grid are executed on U250 FPGA. Four GRU-based dynamic equivalent systems can be executed in parallel on a VCU128 board, meanwhile, each VCU118 board is able to accommodate 3 dynamic equivalent systems.

The reconfigurability of FPGAs allows the hardware resources to be adjusted to accommodate and represent a practical system, and enables each circuit part or subsystem to be designed as a hardware module. Recently, the Xilinx Vivado® packages provide the high-level sysnthesis (HLS) tool to simplify the hardware design cycle, which transforms the system functions written in C/C++ code to intellectual property (IP) which contains corresponding input/output ports in hardware design language (HDL) format. After IP generation, each circuit part is converted to a hardware module and exported to Vivado® for block-level design. According to the correlation among the subsystems, the hardware modules are designed to be calculated in parallel or series, and the data exchange is realized by connecting the input/output ports among hardware modules.

As illustrated in Fig. 6.11, after synthesis and block design, the bit files are generated and downloaded to the target FPGAs via the PCIe or the Joint Test Action Group (JTAG) interface. Since multiple FPGA boards are assembled, data communication is required for emulating such a complex testing system. Several communication ports are provided on the Xilinx Virtex® UltraScale+ series FPGA boards/card, such as Quad Small Form-factor Pluggable (QSFP), Samtec® FireFly interfaces and traditional Ethernet jacks. Both the QSFP and FireFly interfaces can provide maximum bidirectional communication rate of 4×28 $Gbps$. Due to the absence of Samtec® FireFly interface on the Alveo U250 acceleration card, the QSFP interface is applied to the FTRT emulation platform. Owing to the fewer data required of the proposed DEM-DC grid interface, the PCC voltages and dynamic power are chosen as the communication data. Meanwhile, the calculated data from the FPGA boards is in digital format, which is transferred to analog data through the digital-

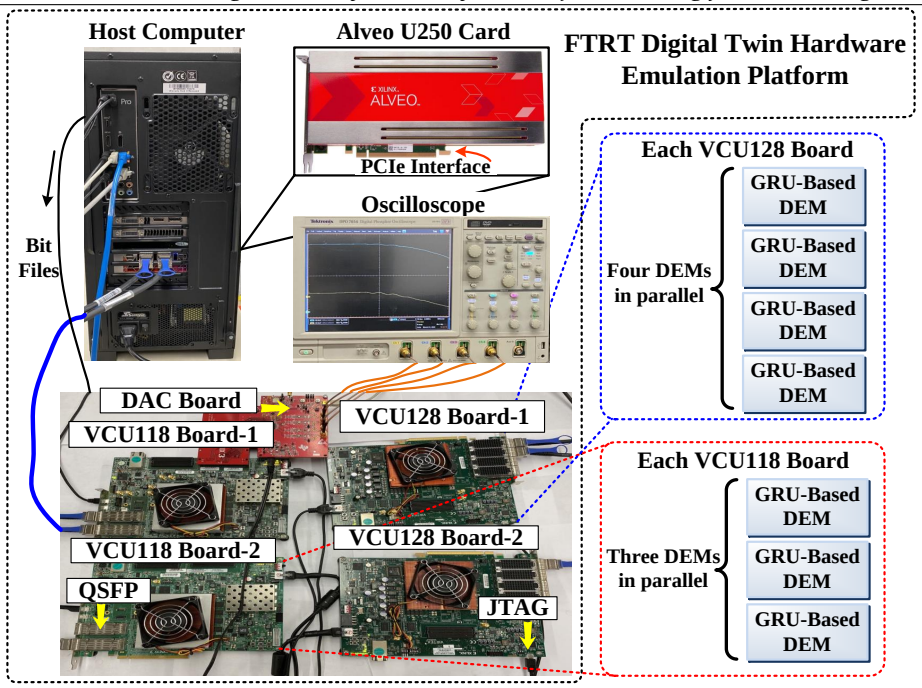

Figure 6.11: FTRT digital twin hardware for hybrid computational-ML based TS emulation.

to-analogic (DAC) board and displayed on the oscilloscope.

The latency and hardware resource utilization of each hardware module are provided in Table 6.4, where the latency is given in clock cycles which are defined as 10 ns under the FPGA frequency of 100 MHz. Since the similar UltraScale+ series FPGAs are equipped on the aforementioned boards/card, the proposed *DEM* module has the same latency and hardware resource occupation on them. The execution time of *DEM* is calculated as $937 \times 10ns = 9.37\mu s$. As the time-step of the AC system is chosen as 1 ms, the FTRT ratio can be expressed as $\frac{1ms}{9.37\mu s} = 106.72$. The *RK4*, *GRU*, *Network*, and *Update* modules denote the functions in study zone. The *GRU* can be solved in parallel with the latency of $167Tclk$, and the overall latency of the study zone is $146 + 196 + 21 = 363Tclk$. Then the FTRT ratio of the study zone is over $\frac{1ms}{363\times 10ns} = 275$. Similarly, the DC grid part are fully parallelized with the largest latency of $96Tclk$, meaning with an EMT emulation time-step of 200 μs, the FTRT ratio reaches over $\frac{200\mu s}{96\times 10ns} = 208$. Although an FTRT ratio of 260 can be achieved in the study zone, the overall FTRT ratio is determined by the EMT part, since the AC grids should wait for the DC grid to finish to update the communication data at the interfaces. Therefore, the total FTRT ratio of the testing system is over 208.

6.4 Hardware Emulation Results and Validation

The hardware emulation of the integrated AC-DC grid was conducted on the FPGA-based FTRT digital twin platform as mentioned above, and the emulation results of the pro-

Table 6.4: Details of major hardware modules of the large-scale AC-DC grid

Module	Latency	BRAM	DSP	FF	LUT
Available hardware resources					
VCU118	–	4320	6840	2364480	1182240
VCU128	–	4032	9024	2607360	1303680
U250	–	5376	12288	3456000	1728000
DEM on FPGA ($100MHz$)					
GRU-DEM	937 T_{clk}	116	1872	233467	273579
ACTIVSg 500-bus system on FPGA ($100MHz$)					
GRU-SGM	146 T_{clk}	42	116	13058	17064
Network	196 T_{clk}	16	678	48921	54732
Update	21 T_{clk}	0	35	5635	6185
HVDC system on FPGA ($100MHz$)					
MMCmodel	96 T_{clk}	0	16	2582	3270
PQcontrol	86 T_{clk}	0	62	5829	6320
HVDCNetwork	93 T_{clk}	0	30	3675	4830
Total_VCU118	–	8.06%	82.11%	29.62%	69.42%
Total_VCU128	–	11.51%	82.98%	35.82%	83.94%
Total_U250	–	12.95%	90.48%	35.42%	92.04%

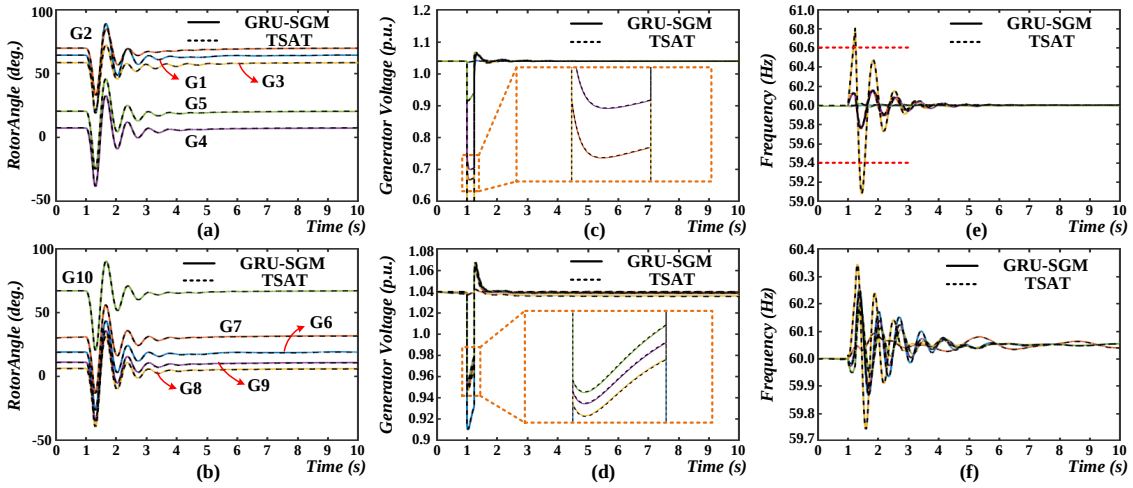

Figure 6.12: Comparison of GRU-SGM and TSAT® results under three-phase-to-ground fault: (a) generator rotor angles (G1-G5), (b) generator rotor angles (G6-G10), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) generator frequencies (G1-G5), and (f) generator frequencies (G6-G10).

posed GRU-based synchronous generator and dynamic equivalent model were validated by comparing with the results from the off-line simulation tool DSATools™/TSAT®.

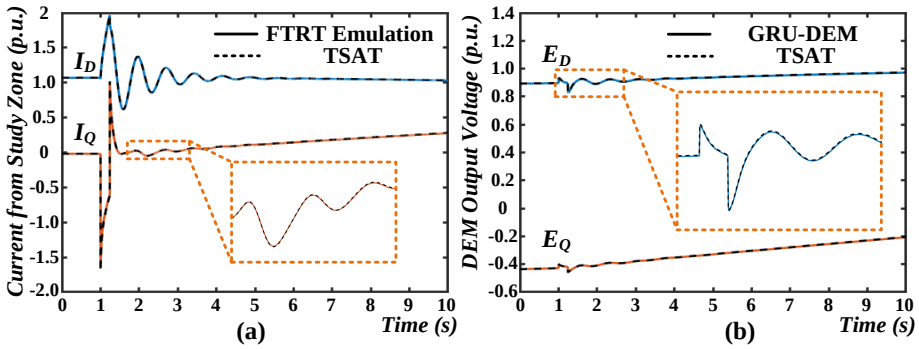

Figure 6.13: FTRT emulation results of interface data: (a) output currents at *Bus* 412 of study zone, (b) output voltages of GRU-DEM.

6.4.1 Case 1: Three-Phase-to-Ground Fault

In dynamic security analysis, the three-phase-to-ground faults usually induce the most severe disturbances. Meanwhile, the emulation results for those contingencies that are cleared around the CCT are usually highly sensitive to the error, and therefore, a three-phase-to-ground fault on the study zone lasting 300 ms is taken into considered in this part. Under steady-state, the study zone delivers 850 MW to the remaining 500-bus systems via the 15-T HVDC grid, and each system receives about 50 MW. At the time of 1 s, a three-phase fault takes place at *Bus* 413 with a duration of 300 ms. Since the fault location is close to the PCC *Bus* 412, the fault will cause serious oscillation and spread to the following systems. The emulation results of G1 to G10 are provided in Fig. 6.12. When the fault encounters, the generator rotor angles experience a drastic oscillation lasting about 3 s. A significant voltage drop occurs right after the occurrence the three-phase fault as given in Fig. 6.12 (c) and (d). In the meantime, the abnormal rotor angles induce a severe oscillation on the generator frequencies, and the frequency of G3 exceed the $\pm 1\%$ threshold as shown in Fig. 6.12 (e) and (f).

To further demonstrate the accuracy of the proposed GRU-DEM, the interface data is also provided in Fig. 6.13. The oscillating currents in D-Q frame at *Bus* 412 are send to the rectifier station and delivered to the subsystems that are emulated by DEM. Due to the 14 subsystems connected to the HVDC grid, the output voltage of each DEM system is not as severe as the output current from the study zone as shown in Fig. 6.13 (b). The zoomed-in plots in Fig. 6.13 and Fig. 6.12 (c)-(d) indicate that the FTRT emulation results match up with that of the TSAT®, which proves that the proposed GRU-SGM and DEM is as accurate as the transient stability simulation of the full system in TSAT®.

6.4.2 Case 2: Generation Reduction

The proposed dynamic equivalent model was trained by several three-phase faults, and the accuracy can be guaranteed as mentioned above. In the dynamic security analysis, the

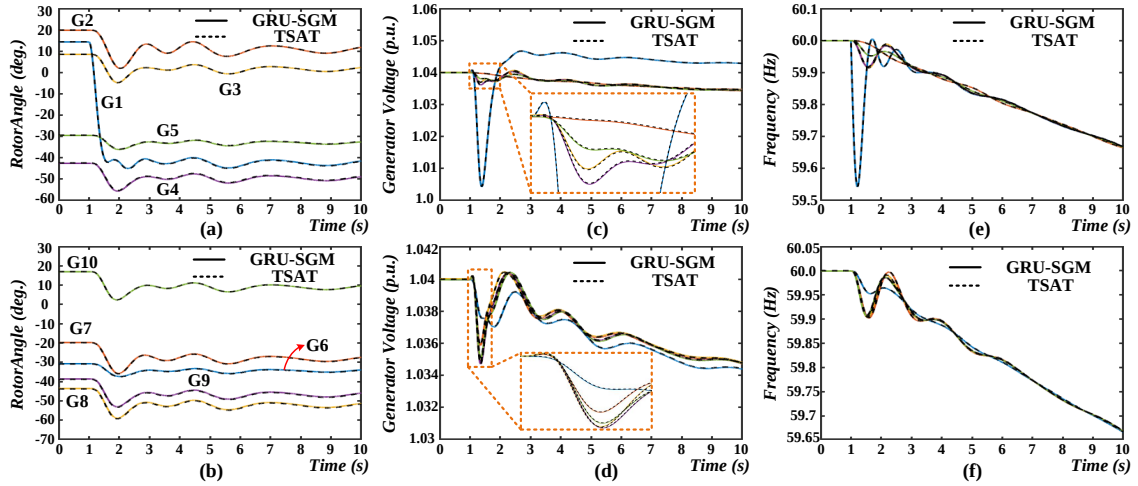

Figure 6.14: Comparison of GRU-SGM and TSAT® results under generation reduction on G1: (a) generator rotor angles (G1-G5), (b) generator rotor angles (G6-G10), (c) generator output voltages (G1-G5), (d) generator output voltages (G6-G10), (e) generator frequencies (G1-G5), and (f) generator frequencies (G6-G10).

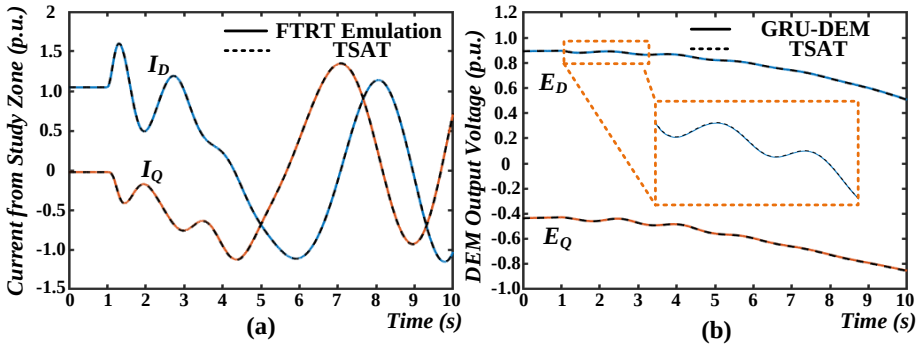

Figure 6.15: FTRT emulation results of interface data: (a) output currents at *Bus* 412 of study zone, (b) output voltages of GRU-DEM.

system may encounter several kinds of contingencies. In this section, a long-term generation reduction is emulated on the FTRT platform and validated by the off-line simulation tool. At the time of 1 s, the generator G1 suddenly reduce 90% of its normal generation without recovered. The imminent impacts including serious disturbance to the rotor angles, generator voltages, and frequencies, as given in Fig. 6.14. The frequencies of synchronous generators keep decreasing and cannot be restored. Due to the $\pm 1\%$ threshold of the frequencies in dynamic security assessment, the abnormal frequencies are detected after 10 s, which may cause serious impacts on the system. With the 208 FTRT ratio, the hardware emulation platform is able to predict the upcoming disturbance and take remedial actions.

Similarly, the interface data is also provided to validate the accuracy of the proposed DEM under generation reduction, as given in Fig. 6.15. Fig. 6.15 (a) indicates that the

reduced generation causes output current at *Bus* 412 unstable. The zoomed-in plots in Fig. 6.15 (b) proves that the proposed DEM still has high accuracy under the contingencies except three-phase faults. Therefore, the proposed GRU-SGM and DEM executed on the FTRT emulation platform can be utilized on large-scale AC-DC grid for dynamic security analysis.

6.5 Summary

This chapter proposed the ML based synchronous generator model and dynamic equivalent model for implementing an FTRT digital twin of a large-scale AC-DC grid. The GRU-based ML strategy is able to emulate the multi-mass synchronous machine with high accuracy. Compared with traditional iterative method, the GRU-based machine model has significant advantages in resource consumption and execution time during hardware implementation. Meanwhile, the GRU-based ML method is also applied to create a dynamic equivalent system. Since the GRU-DEM replaces the complex computational model in the external system, the execution time of emulating the hybrid AC-DC grid is accelerated. The utilization of the FPGA boards containing the high-speed communication interfaces enabled emulating a large-scale power system in parallel, and a 208 FTRT ratio was achieved. Furthermore, two case studies were emulated to validate the accuracy of the proposed model with contingencies that differ from the training datasets. The FTRT hardware emulation results of the integrated AC-DC grid are highly matched with those of the off-line simulation results from TSAT®. Therefore, the GRU-SGM and DEM executed on the FPGA-based FTRT emulation platform can help predict upcoming disturbances and initiate remedial actions, which is significantly meaningful in an energy control center application.

7 Conclusions

There has been increasing integration of HVDC grids and renewable energy into modern power system in recent years, which drew attention from both academia and industry. The expansion of power systems has brought a tremendous computational challenge to dynamic security analysis. Transient stability simulation is the main approach for investigating the stability and security of hybrid AC-DC grids. Currently, the commercial DSA tools are executed on the CPU-based platforms, which occupies a lot of hardware resources. Nevertheless, due to sequential calculation scheme, only real-time results can be obtained from the currently available DSA tools. Therefore, a practical method for energy control center with FPGA-based faster-than-real-time hardware platform is proposed to reduce the computational burden of DSA.

FPGAs are selected as prime compute devices for FTRT hardware-in-the-loop emulation of the integrated AC-DC grids in this thesis. Their intrinsic parallelism and pipeline architecture enable each system part to be programmed according to its function and application, and therefore the FTRT emulation could be achieved with high speed-up ratio even though the FPGA clock frequency was lower than other processors. Meanwhile, with a rapid growth in logic gates and higher clock frequency due to maturing fabrication technology, sufficient hardware resources are available to model more complex power systems. The development of corresponding hardware design tools further shortened the design cycle by enabling programming in advanced languages.

7.1 Contributions of Thesis

The main contributions of this thesis are summarized as follows:

- The proposal of a fine-grained relaxation algorithm for FTRT emulation of hybrid

AC-DC grid on the FPGA. FTRT emulation implies that the platform runs several times faster than an RT platform so that it is able to predict system performance after contingencies and consequently yield useful information for system operation guidance. The most time-consuming part for a TS problem is solving the synchronous generators which is represented by DAEs. The proposed FGRA enables the DAEs being solved in parallel. Meanwhile, due to the parallelism and pipeline architecture of FPGA, the proposed algorithm can be executed perfectly on it after properly hardware design. Thus, a 134 times FTRT ratio could be obtained, which is suitable for the energy control center to provide sufficient time to take remedial actions, provide an optimal control strategy to mitigate adverse impacts, and enhance the overall stability and security of the system.

- A local-equipment-based FTS algorithm and its synchronization strategy (including EMT and transient stability co-simulation interface) were proposed for computation efficiency improvement. Compared with the traditional LTE-based variable time-stepping strategy, the proposed FTS method is able to find the proper time-step instantly and thus significantly reduce the computational burden, which is of ultra-importance in realizing FTRT. Besides, the time-step synchronization strategy enables various time-steps of circuit parts to run compatible in one program.

- The introduction of multi-mass synchronous generator model in the transient stability simulation for SSI analysis. Single mass generator shaft mode is inefficient for SSI investigation. The SSI phenomenon emerges when the electrical oscillation frequency after a severe disturbance matches with one of the shaft natural frequencies. Thus, eigenvalue analysis was adopted to verify the accuracy of the multi-mass machine model. Meanwhile, the FTRT hardware emulation being able to enhance the stability of AC transmission and distribution system was also utilized.

- Investigating and mitigating the SSCI between a PV inverter and neighboring weak transmission system. The detailed eigenvalue analysis was applied for analyzing the PV farm and its control system, which provides theoretical basis for the SSCI phenomenon in PV plants connected to a weak grid. Meanwhile, an active/reactive power control strategy is proposed for mitigating the SSCI. With the help of FTRT emulation, the energy control center have sufficient time to predict the future states, and yield an optimal power injection solution to maintain the system stability.

- Coordinated communication and emulation among several FPGA boards. Single FPGA board is insufficient to accommodate a large power grid which contains hundreds of synchronous generators, and therefore, multiple FPGA boards are utilized for FTRT emulation. With the 4×28 $Gbps$ full-duplex bandwidth in 4 channels of QSFP connector, communication delay can be neglected and the efficient data ex-

change among FPGAs can be realized, which significantly improves the scalability of the FTRT hardware emulation.

- Hardware emulation of contingency screening for DSA of large-scale AC-DC grid. Since the FTRT emulation enables a high computation speed above real-time, the grid can be emulated much faster and therefore it can accelerate planning schedules, predict the upcoming disturbances, and devise new control strategies. The proposed FTRT emulation could also be applied to the energy control center to provide real-time security index after the occurrence of a disturbance. Meanwhile, the properly designed hardware platform enables extensive contingencies running simultaneously in FTRT mode.

- Improvement of the AC-DC grid interface using dynamic voltage injection. Traditional P-Q load based interface requires the admittance matrix to be updated in every time-step. The novel interface strategy was able to maintain a constant admittance matrix despite the HVDC converter outputs being time-varying, which consequently reduced hardware resource utilization and expedited the emulation.

- The GRU-based synchronous generator model and dynamic equivalent model are applied to TS simulation for further acceleration of FTRT emulation. Dynamic equivalencing strategies are commonly used in dealing with the large-scale systems for TS simulation. Although valuable contributions have been made, the computational requirements are still heavy. The ML-based dynamic equivalencing method is able to significantly reduce the computational burden of large-scale AC-DC grids for TS simulation. Meanwhile, the hardware designs for the GRU-based SGM and DEM were also demonstrated, and a remarkable speedup was attained on multiple FPGA boards.

7.2 Directions for Future Work

The following topics are proposed for future work:

- Hardware resource is the main factor that restricts the scale of a power system deployed to the FPGA boards. The scalability is demonstrated by cascading multiple FPGA boards in realizing the FTRT emulation, and more FPGA boards can be connected along with a further expansion of the AC-DC grid. Furthermore, the FTRT hardware emulation for large-scale AC-DC grid can also be achieved by leveraging the fast and parallel computing capabilities of FPGA/GPU/Multi-Processor System-on-Chip (MPSoC) hardware platforms, which can distribute the computational burden based on their advantages.

  A fully detailed MTDC grid could be developed on GPU by using high fidelity models of power system components such as the transmission line and the transformer,

rather than the lumped model in current EMT simulation parts. Moreover, the network equations with matrix multiplication can be executed on MPSoC, due to its high calculation frequency. The FTRT emulation platform with multiple kinds of hardware can be also treated as a digital twin of a real large-scale AC-DC grid and applied to the energy control center.

- The flexible time-stepping schemes could be applied to other power system configurations for FTRT emulation on FPGA. In this work, it has been applied to transient stability simulation. Nevertheless, the algorithm for complex systems such as the wind farm with DFIG whose mathematical equations take the matrix form has not been developed. New criteria for time-stepping judgment and control can also be investigated.

- In this work, the GRU-DEM is adopted to represent the ACTIVSg 500-bus system with dynamic P+jQ interface. Due to the significant acceleration in execution time and low hardware resource occupation in ML-based model, the proposed GRU-DEM is also suitable for other large-scale power systems, which enables emulating a complex power system in FTRT mode. Furthermore, the ML-based equivalent model can be applied to the EMT simulation part such as PV grids. Each PV cell can be modeled by either an ML-based model or a detailed computational model, and therefore a multi-domain mixed-solver architecture can be established for FTRT emulation.

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A

Chapter 1 Appendix: Kundur's Two-Area System Parameters

Table A.1: Bus data

Bus	Type (0 = P-Q) (1 = P-V)	Volts	Load MW	Load MVar	Gen MW	Gen MVar
1	1	1.03	0.00	0.00	700.00	185.00
2	1	1.01	0.00	0.00	700.00	235.00
3	1	1.03	0.00	0.00	719.00	176.00
4	1	1.01	0.00	0.00	700.00	202.00
5	0	-	0.00	0.00	0.00	0.00
6	0	-	0.00	0.00	0.00	0.00
7	0	-	967.00	-100.00	0.00	0.00
8	0	-	0.00	0.00	0.00	0.00
9	0	-	1767.00	-250.00	0.00	0.00
10	0	-	0.00	0.00	0.00	0.00
11	0	-	0.00	0.00	0.00	0.00

Table A.2: Line data

Bus	Bus	Resistance	Reactance	Susceptance	Transformer Magnitude	Transformer Angle
1	5	0.0000	0.0167	0.0000	0.0000	0.0
2	6	0.0000	0.0167	0.0000	0.0000	0.0
3	11	0.0000	0.0167	0.0000	0.0000	0.0
4	10	0.0000	0.0167	0.0000	0.0000	0.0
5	6	0.0025	0.0250	0.0000	0.0000	0.0
6	7	0.0010	0.0100	0.0175	0.0000	0.0
7	8	0.0110	0.1100	0.1925	0.0000	0.0
8	9	0.0110	0.1100	0.1925	0.0000	0.0
9	10	0.0010	0.0100	0.0175	0.0000	0.0
10	11	0.0025	0.0250	0.0000	0.0000	0.0

Table A.3: Generator data

X_d=1.8	X_q=1.7	X_l=0.2	X'_d=0.3	X'_q=0.55
X''_d=0.25	X''_q=0.25	R_a=0.0025	T'_{d0}=8.0 s	T'_{q0}=0.4 s
T''_{d0}=0.03 s	T''_{q0}=0.05 s	A_{sat}=0.015	B_{sat}=9.6	ψ_{T1}=0.9
H=6.5 (for G1)	H=6.175 (for G2)	H=6.5 (for G3)	H=6.175 (for G4)	K_D=0.0

B

Chapter 1 Appendix: IEEE 39-Bus Parameters

Table B.1: Bus data

Bus	Type (0 = P-Q) (1 = P-V)	Volts	Load MW	Load MVar	Gen MW	Gen MVar
1	0	-	0.0000	0.0000	0.0000	0.0000
2	0	-	0.0000	0.0000	0.0000	0.0000
3	0	-	322.000	2.400	0.0000	0.0000
4	0	-	500.000	184.000	0.0000	0.0000
5	0	-	0.0000	0.0000	0.0000	0.0000
6	0	-	0.0000	0.0000	0.0000	0.0000
7	0	-	233.800	84.000	0.0000	0.0000
8	0	-	522.000	176.000	0.0000	0.0000
9	0	-	0.0000	0.0000	0.0000	0.0000
10	0	-	0.0000	0.0000	0.0000	0.0000
11	0	-	0.0000	0.0000	0.0000	0.0000
12	0	-	7.500	88.000	0.0000	0.0000
13	0	-	0.0000	0.0000	0.0000	0.0000
14	0	-	0.0000	0.0000	0.0000	0.0000
15	0	-	320.000	153.000	0.0000	0.0000
16	0	-	329.000	32.300	0.0000	0.0000
17	0	-	0.0000	0.0000	0.0000	0.0000
18	0	-	158.000	30.000	0.0000	0.0000
19	0	-	0.0000	0.0000	0.0000	0.0000
20	0	-	628.000	103.000	0.0000	0.0000
21	0	-	274.000	115.000	0.0000	0.0000
22	0	-	0.0000	0.0000	0.0000	0.0000
23	0	-	247.500	84.600	0.0000	0.0000
24	0	-	308.600	-92.200	0.0000	0.0000
25	0	-	224.000	47.200	0.0000	0.0000
26	0	-	139.000	17.000	0.0000	0.0000
27	0	-	281.000	75.500	0.0000	0.0000

Table B.2: Bus data

Bus	Type (0 = P-Q) (1 = P-V)	Volts	Load MW	Load MVar	Gen MW	Gen MVar
28	0	-	206.00	27.60	0.00	0.00
29	0	-	283.50	26.90	0.00	0.00
30	1	1.0475	0.00	0.00	250.00	-
31	1	0.982	9.20	4.60	-	-
32	1	0.9831	0.00	0.00	650.00	-
33	1	0.9972	0.00	0.00	632.00	-
34	1	1.01235	0.00	0.00	508.00	-
35	1	1.0493	0.00	0.00	650.00	-
36	1	1.0635	0.00	0.00	560.00	-
37	1	1.0278	0.00	0.00	540.00	-
38	1	1.0265	0.00	0.00	830.00	-
39	1	1.03	1104.0	250.0	1000.0	-

Table B.3: Line data

Bus	Bus	Resistance	Reactance	Susceptance	Transformer Magnitude	Transformer Angle
1	2	0.0035	0.0411	0.6987	0.000	0.0
1	39	0.0010	0.0250	0.7500	0.000	0.0
2	3	0.0013	0.0151	0.2572	0.000	0.0
2	25	0.0070	0.0086	0.1460	0.000	0.0
3	4	0.0013	0.0213	0.2214	0.000	0.0
3	18	0.0011	0.0133	0.2138	0.000	0.0
4	5	0.0008	0.0128	0.1342	0.000	0.0
4	14	0.0008	0.0129	0.1382	0.000	0.0
5	6	0.0002	0.0026	0.0434	0.000	0.0
5	8	0.0008	0.0112	0.1476	0.000	0.0
6	7	0.0006	0.0092	0.1130	0.000	0.0
6	11	0.0007	0.0082	0.1389	0.000	0.0
7	8	0.0004	0.0046	0.0780	0.000	0.0
8	9	0.0023	0.0363	0.3804	0.000	0.0
9	39	0.0010	0.0250	1.2000	0.000	0.0

Table B.4: Line data

Bus	Bus	Resistance	Reactance	Susceptance	Transformer Magnitude	Transformer Angle
10	11	0.0004	0.0043	0.0729	0.000	0.0
10	13	0.0004	0.0043	0.0729	0.000	0.0
13	14	0.0009	0.0101	0.1723	0.000	0.0
14	15	0.0018	0.0217	0.3660	0.000	0.0
15	16	0.0009	0.0094	0.1710	0.000	0.0
16	17	0.0007	0.0089	0.1342	0.000	0.0
16	19	0.0016	0.0195	0.3040	0.000	0.0
16	21	0.0008	0.0135	0.2548	0.000	0.0
16	24	0.0003	0.0059	0.0680	0.000	0.0
17	18	0.0007	0.0082	0.1319	0.000	0.0
17	27	0.0013	0.0173	0.3216	0.000	0.0
21	22	0.0008	0.0140	0.2565	0.000	0.0
22	23	0.0006	0.0096	0.1846	0.000	0.0
23	24	0.0022	0.0350	0.3610	0.000	0.0
25	26	0.0032	0.0323	0.5130	0.000	0.0
26	27	0.0014	0.0147	0.2396	0.000	0.0
26	28	0.0043	0.0474	0.7802	0.000	0.0
26	29	0.0057	0.0625	1.0290	0.000	0.0
28	29	0.0014	0.0151	0.2490	0.000	0.0
12	11	0.0016	0.0435	0.0000	1.006	0.0
12	13	0.0016	0.0435	0.0000	1.006	0.0
6	31	0.0000	0.0250	0.0000	1.070	0.0
10	32	0.0000	0.0200	0.0000	1.070	0.0
19	33	0.0007	0.0142	0.0000	1.070	0.0
20	34	0.0009	0.0180	0.0000	1.009	0.0
22	35	0.0000	0.0143	0.0000	1.025	0.0
23	36	0.0005	0.0272	0.0000	1.000	0.0
25	37	0.0006	0.0232	0.0000	1.025	0.0
2	30	0.0000	0.0181	0.0000	1.025	0.0
29	38	0.0008	0.0156	0.0000	1.025	0.0
19	20	0.0007	0.0138	0.0000	1.060	0.0

Table B.5: Detailed model generator data

Gen No.	H ((sec))	T'_{d0}	T''_{d0}	T'_{q0}	T''_{q0}	D
G1	50.0	7.00	0.03	0.70	0.04	0
G2	3.03	6.56	0.03	1.50	0.04	0
G3	3.58	5.70	0.03	1.50	0.04	0
G4	2.86	5.69	0.03	1.50	0.04	0
G5	2.60	5.40	0.03	0.44	0.04	0
G6	3.48	7.30	0.03	0.40	0.04	0
G7	2.64	5.66	0.03	1.50	0.04	0
G8	2.43	6.70	0.03	0.41	0.04	0
G9	3.45	4.79	0.03	1.96	0.04	0
G10	4.20	10.20	0.03	1.50	0.04	0
X_d	X_q	X'_d	X'_q	X''_d	X_l	R_a
0.200	0.19	0.06	0.06	0.02	0.0125	0
2.950	2.82	0.697	0.697	0.20	0.125	0
2.495	2.37	0.531	0.531	0.20	0.125	0
2.620	2.58	0.436	0.436	0.20	0.125	0
6.700	6.20	1.320	1.320	0.20	0.125	0
2.540	2.41	0.500	0.500	0.20	0.125	0
2.950	2.92	0.490	0.490	0.20	0.125	0
2.900	2.80	0.570	0.570	0.20	0.125	0
2.106	2.05	0.570	0.570	0.20	0.125	0
1.000	0.69	0.310	0.310	0.20	0.125	0

Table B.6: Detailed model control system data

Gen No.	KA	TR	Kstab	TW	T1	T2	Efd_{max}	Efd_{min}
G1	200	0.01	1.0	10	1.0	0.05	5	-5
G2	200	0.01	0.5	10	5.0	0.40	5	-5
G3	200	0.01	0.5	10	3.0	0.20	5	-5
G4	200	0.01	2.0	10	1.0	0.10	5	-5
G5	200	0.01	1.0	10	1.5	0.20	5	-5
G6	200	0.01	4.0	10	0.5	0.10	5	-5
G7	200	0.01	7.5	10	0.2	0.02	5	-5
G8	200	0.01	2.0	10	1.0	0.20	5	-5
G9	200	0.01	2.0	10	1.0	0.50	5	-5
G10	200	0.01	1.0	10	5.0	0.60	5	-5

C

Chapter 2 Appendix: IEEE 118-Bus System Parameters

Table C.1: Load data

Bus	P	Q	Q_{comp}	Bus	P	Q	Q_{comp}
1	52.0	27.0	-24.0	31	44.0	27.0	-12.0
2	20.0	9.0	0.0	32	60.0	23.0	0.0
3	40.0	10.0	0.0	33	23.0	9.0	0.0
4	31.0	12.0	0.0	34	60.0	26.0	0.0
5	0.0	0.0	40.0	35	34.0	9.0	0.0
6	53.0	22.0	0.0	36	32.0	17.0	0.0
7	19.0	2.0	0.0	37	0.0	0.0	25.0
8	0.0	0.0	0.0	38	0.0	0.0	0.0
9	0.0	0.0	0.0	39	28.0	11.0	0.0
10	0.0	0.0	0.0	40	20.0	23.0	-12.0
11	71.0	23.0	0.0	41	38.0	10.0	0.0
12	48.0	10.0	0.0	42	38.0	23.0	0.0
13	35.0	16.0	-12.0	43	18.0	7.0	0.0
14	14.0	1.0	0.0	44	16.0	8.0	0.0
15	92.0	30.0	0.0	45	54.0	22.0	-12.0
16	26.0	10.0	0.0	46	29.0	10.0	0.0
17	11.0	3.0	0.0	47	35.0	0.0	0.0
18	61.0	34.0	0.0	48	20.0	11.0	0.0
19	46.0	25.0	0.0	49	89.0	30.0	0.0
20	18.0	3.0	0.0	50	17.0	4.0	0.0
21	14.0	8.0	-12.0	51	17.0	8.0	0.0
22	10.0	5.0	0.0	52	18.0	5.0	0.0
23	7.0	3.0	0.0	53	23.0	11.0	-12.0
24	0.0	0.0	0.0	54	115.0	32.0	0.0
25	0.0	0.0	0.0	55	64.0	22.0	0.0
26	0.0	0.0	0.0	56	86.0	18.0	-12.0
27	63.0	13.0	0.0	57	12.0	3.0	0.0
28	17.0	7.0	0.0	58	12.0	3.0	0.0
29	24.0	4.0	-12.0	59	283.0	113.0	0.0
30	0.0	0.0	0.0	60	80.0	3.0	0.0

Table C.2: Load data

Bus	P	Q	Q_{comp}	Bus	P	Q	Q_{comp}
61	0.0	0.0	0.0	90	80.0	42.0	0.0
62	79.0	14.0	0.0	91	0.0	0.0	0.0
63	0.0	0.0	0.0	92	66.0	10.0	0.0
64	0.0	0.0	0.0	93	12.0	7.0	0.0
65	0.0	0.0	0.0	94	31.0	16.0	0.0
66	40.0	18.0	0.0	95	43.0	31.0	-12.0
67	29.0	7.0	0.0	96	39.0	15.0	0.0
68	0.0	0.0	0.0	97	15.0	9.0	0.0
69	0.0	0.0	0.0	98	35.0	8.0	0.0
70	67.0	20.0	0.0	99	0.0	0.0	0.0
71	0.0	0.0	0.0	100	38.0	18.0	0.0
72	0.0	0.0	0.0	101	22.0	15.0	0.0
73	0.0	0.0	0.0	102	5.0	3.0	0.0
74	69.0	27.0	-24.0	103	23.0	16.0	0.0
75	48.0	11.0	0.0	104	39.0	25.0	0.0
76	69.0	36.0	-36.0	105	32.0	26.0	-24.0
77	62.0	28.0	-12.0	106	44.0	16.0	-12.0
78	72.0	26.0	-24.0	107	29.0	12.0	-12.0
79	40.0	32.0	0.0	108	2.0	1.0	0.0
80	133.0	26.0	0.0	109	8.0	3.0	0.0
81	0.0	0.0	0.0	110	40.0	30.0	0.0
82	55.0	27.0	-24.0	111	0.0	0.0	0.0
83	20.0	10.0	-10.0	112	26.0	13.0	-8.0
84	11.0	7.0	0.0	113	0.0	0.0	0.0
85	24.0	15.0	0.0	114	8.0	3.0	0.0
86	21.0	10.0	0.0	115	22.0	7.0	0.0
87	0.0	0.0	0.0	116	0.0	0.0	0.0
88	49.0	10.0	0.0	117	20.0	8.0	-8.0
89	0.0	0.0	0.0	118	34.0	15.0	-12.0

Table C.3: Line data

From Bus	To Bus	Resistance [Ω]	Reactance [Ω]	Susceptance[μS]
1	2	2.14	42.77	100.59
1	3	0.91	18.16	42.68
2	12	1.60	32.04	75.33
3	5	2.31	46.23	108.75
3	12	3.42	68.42	161.20
4	5	0.33	6.66	15.66
4	11	1.73	34.50	81.11
5	6	1.16	23.13	54.36
5	11	1.73	34.50	81.11
6	7	0.45	8.91	20.93
7	12	1.62	32.28	75.88
8	9	4.85	136.02	348.01
8	30	5.87	165.07	424.76
9	10	5.91	166.38	428.26
11	12	0.72	14.31	33.61
11	13	1.91	38.12	89.65
12	14	1.80	35.93	84.49
12	16	5.01	100.36	237.21
12	117	0.12	2.48	5.84
13	15	5.20	104.26	246.53
14	15	4.51	90.29	213.15
15	17	1.49	29.75	69.94
15	19	1.90	37.91	89.14
15	33	2.66	53.24	125.29
16	17	0.95	18.88	44.36
17	18	1.08	21.63	50.83
17	31	3.34	66.84	157.46
17	113	2.92	58.26	137.16
18	19	1.79	35.75	84.06
19	20	2.51	50.12	117.74
19	34	3.16	63.23	148.91
20	21	1.82	36.35	85.48
21	22	2.08	41.53	97.67
22	23	3.95	79.10	186.53
23	24	1.88	37.63	88.48
23	25	3.07	61.45	144.69
23	32	7.00	140.82	334.79

Table C.4: Line data

From Bus	To Bus	Resistance [Ω]	Reactance [Ω]	Susceptance[μS]
24	70	9.83	199.35	479.83
24	72	5.06	101.33	239.53
25	27	7.26	146.20	347.91
26	30	10.24	285.05	720.43
27	28	1.83	36.61	86.09
27	32	4.47	89.56	211.42
27	115	5.17	103.65	245.07
28	29	2.02	40.38	94.95
29	31	0.71	14.18	33.32
30	38	6.26	176.54	455.49
31	32	2.11	42.17	99.17
32	113	4.33	86.70	204.61
32	114	0.54	10.79	25.35
33	37	3.04	60.75	143.04
34	36	0.58	11.48	26.97
34	37	0.27	5.32	12.51
34	43	1.62	32.26	75.83
35	36	0.22	4.37	10.28
35	37	1.07	21.28	50.02
37	39	2.27	45.38	106.74
37	40	7.77	156.63	373.46
38	65	10.71	312.26	845.18
39	40	7.34	147.74	351.67
40	41	4.62	92.60	218.66
40	42	3.91	78.21	184.41
41	42	2.89	57.76	135.97
42	49	6.93	137.33	326.32
42	49	6.93	137.33	326.32
43	44	5.22	104.67	247.53
44	45	1.93	38.58	90.71
45	46	2.90	58.02	136.58
45	49	3.97	79.48	187.44
46	47	2.72	54.35	127.91
46	48	4.04	80.76	190.47
47	49	1.34	26.77	62.91
47	69	5.90	118.34	280.37

Table C.5: Line data

From Bus	To Bus	Resistance [Ω]	Reactance [Ω]	Susceptance[μS]
48	49	1.08	21.63	50.83
49	50	1.92	38.40	90.31
49	51	2.93	58.61	137.98
49	54	7.49	150.83	359.23
49	54	7.49	150.83	359.23
49	66	1.97	39.34	92.52
49	66	1.97	39.34	92.52
49	69	6.85	137.76	327.34
50	57	2.87	57.33	134.95
51	52	1.26	25.18	59.18
51	58	1.54	30.79	72.38
52	53	3.50	69.91	164.73
53	54	2.61	52.20	122.85
54	55	1.81	36.13	84.95
54	56	3.21	64.19	151.17
54	59	5.26	105.40	249.26
55	56	1.52	30.25	71.11
55	59	3.10	62.03	146.06
56	57	0.65	13.05	30.65
56	58	0.65	13.05	30.65
56	59	5.34	107.04	253.20
56	59	5.09	101.96	241.04
59	60	3.10	62.03	146.06
59	61	3.21	64.15	151.10
60	61	0.76	15.22	35.75
60	62	1.28	25.47	59.86
61	62	1.99	39.74	93.46
62	66	4.65	93.07	219.78
62	67	2.51	50.07	117.82
63	64	2.37	66.15	167.71
64	65	3.57	99.65	253.54
65	68	2.81	78.47	199.17
66	67	2.18	43.45	102.19
68	81	3.73	104.30	265.53
68	116	0.85	23.51	59.45
69	70	6.85	137.76	327.34
69	75	5.30	106.31	251.46
69	77	4.21	84.35	199.01

Table C.6: Line data

From Bus	To Bus	Resistance [Ω]	Reactance [Ω]	Susceptance[μS]
70	71	2.36	47.12	110.86
70	74	2.83	56.61	133.25
70	75	3.24	64.84	152.73
71	72	3.86	77.11	181.14
71	73	1.87	37.35	87.82
74	75	0.87	17.39	40.85
75	77	16.91	114.21	163.29
75	118	1.24	24.69	58.04
76	77	12.54	84.56	120.89
76	118	1.43	28.52	67.05
77	78	3.11	62.21	146.49
77	80	4.45	89.05	210.20
77	80	4.45	89.05	210.20
77	82	3.73	74.58	175.81
78	79	0.62	12.34	28.99
79	80	1.51	30.15	70.88
80	96	3.89	77.78	183.39
80	97	2.00	39.99	94.04
80	98	2.31	46.23	108.75
80	99	17.42	117.69	168.27
82	83	1.50	29.89	70.27
82	96	1.83	36.57	85.99
83	84	1.28	25.61	60.19
83	85	3.17	63.31	149.09
84	85	1.38	27.46	64.54
85	86	0.95	18.91	44.43
85	88	2.83	56.48	132.94
85	89	3.70	73.95	174.30
86	87	4.42	88.58	209.08
88	89	0.50	10.01	23.52
89	90	0.82	16.32	38.34
89	90	0.82	16.32	38.34
89	92	4.29	28.85	129.14
89	92	1.61	32.16	75.60
90	91	0.70	13.98	32.86
91	92	1.16	23.25	54.64
92	93	1.83	36.53	85.89
92	94	13.38	90.27	129.06

Table C.7: Line data

From Bus	To Bus	Resistance [Ω]	Reactance [Ω]	Susceptance[μS]
92	100	6.25	125.59	297.86
92	102	3.25	65.07	153.26
93	94	6.21	41.82	59.79
94	95	3.68	24.80	35.45
94	96	1.86	37.21	87.49
94	100	0.29	5.83	13.70
95	96	1.17	23.43	55.07
96	97	1.90	37.90	89.11
98	100	15.15	102.27	146.21
99	100	1.91	38.13	89.67
100	101	1.16	23.25	54.64
100	103	1.88	37.50	88.17
100	104	4.35	87.13	205.63
100	106	0.49	9.74	22.89
101	102	2.40	47.94	112.79
103	104	3.39	67.73	159.57
103	105	3.47	69.48	163.72
103	110	3.87	77.49	182.71
104	105	1.71	34.11	80.20
105	106	1.17	23.43	55.07
105	107	1.79	35.72	83.98
105	108	1.51	30.11	70.78
106	107	1.16	23.21	54.56
108	109	0.83	16.58	38.95
109	110	1.92	38.40	90.31
110	111	2.14	42.77	100.59
110	112	2.25	44.86	105.52
114	115	0.22	4.46	10.48

Table C.8: Generator Transformers

Bus	R [pu]	X [pu]	X/R	S [MVA]	U1 [kV]	U2 [kV]
1	0.0025	0.1	40	115	138	10.5
4	0.0025	0.1	40	115	138	10.5
6	0.0025	0.1	40	115	138	10.5
8	0.0033	0.1	30	50	138	10.5
10	0.0020	0.1	50	250	345	20
12	0.0040	0.1	25	25	138	10.5
15	0.0025	0.1	40	115	138	10.5
18	0.0025	0.1	40	115	138	10.5
19	0.0025	0.1	40	115	138	10.5
24	0.0020	0.1	50	470	138	10.5
25	0.0022	0.1	45	215	138	15
26	0.0025	0.1	40	153	345	15
27	0.0020	0.1	50	450	138	10.5
31	0.0067	0.1	15	8	138	10.5
32	0.0025	0.1	40	115	138	10.5
34	0.0025	0.1	40	115	138	10.5
36	0.0025	0.1	40	115	138	10.5
40	0.0025	0.1	40	115	138	10.5
42	0.0040	0.1	25	37.5	138	10.5
46	0.0067	0.1	15	12	138	15
49	0.0025	0.1	40	150	138	15
54	0.0033	0.1	30	50	138	15
55	0.0025	0.1	40	115	138	10.5
56	0.0040	0.1	25	20	138	10.5
59	0.0025	0.1	40	115	138	15
61	0.0022	0.1	45	240	138	15
62	0.0025	0.1	40	115	138	10.5
65	0.0022	0.1	45	220	345	20
66	0.0022	0.1	45	240	138	20
69	0.0022	0.1	45	155	138	20
70	0.0025	0.1	40	115	138	10.5
72	0.0025	0.1	40	115	138	10.5
73	0.0025	0.1	40	115	138	10.5
74	0.0025	0.1	40	115	138	10.5
76	0.0025	0.1	40	115	138	10.5
77	0.0025	0.1	40	115	138	10.5
80	0.0022	0.1	45	165	138	20
85	0.0038	0.1	40	115	138	10.5
87	0.0056	0.1	18	15	138	15

Table C.9: Generator Transformers

Bus	R [pu]	X [pu]	X/R	S [MVA]	U1 [kV]	U2 [kV]
89	0.0022	0.1	45	240	138	20
90	0.0025	0.1	40	115	138	10.5
91	0.0040	0.1	25	37.5	138	10.5
92	0.0025	0.1	40	115	138	10.5
99	0.0025	0.1	40	115	138	10.5
100	0.0025	0.1	40	100	138	15
100	0.0022	0.1	45	240	138	15
103	0.0029	0.1	35	75	138	10.5
104	0.0025	0.1	40	115	138	10.5
105	0.0025	0.1	40	115	138	10.5
107	0.0050	0.1	20	15	138	10.5
110	0.0025	0.1	40	115	138	10.5
111	0.0029	0.1	35	75	138	15
112	0.0067	0.1	15	10	138	10.5
113	0.0067	0.1	15	7.5	138	10.5
116	0.0022	0.1	45	220	345	10.5

Table C.10: Generator Data

Bus	S [MVA]	P [MW]	Q_{min} [MVar]	Q_{max} [MVar]	U [kV]
1	115	0	-15	48	10.4
4	115	0	-100	100	11.03
6	115	0	-13	50	10.4
8	42	0	-37.5	37.5	10.71
10	248	210.8	-73.5	100	21
12	23.5	20	-8.75	12.5	10.61
15	115	0	-10	30	10.29
18	115	0	-16	50	10.19
19	115	0	-8	24	10.08
24	470	0	-42.5	42.5	10.5
25	215	183	-47	110	15.75
26	153	130	-80	80	15.75
27	440	0	-300	300	10.29
31	8	7	-4	4	10.29
32	115	0	-14	42	10.19
34	115	0	-8	24	10.5
36	115	0	-8	24	10.5
40	115	0	-100	100	10.4

Table C.11: Generator Data

Bus	S [MVA]	P [MW]	Q_{min} [MVar]	Q_{max} [MVar]	U [kV]
42	35	0	-29.75	29.75	10.61
46	10.9	9.2	-4	6	15.15
49	150	106.5	-45	90	15.75
54	40	34	-20	20	15
55	115	0	-8	23	10.19
56	20	0	-8	15	10.61
59	115	95	-30	65	15.45
61	238	200	-100	130	15.75
62	115	0	-50	50	10.82
65	220	187	-33.5	100	21
66	238	196	-33.5	100	20.6
69	115	Slack	n.a.	n.a.	21
70	115	0	-10	32	10.29
72	110	0	-100	100	10.5
73	115	0	-100	100	10.4
74	115	0	-6	9	10.08
76	115	0	-50	50	10.08
77	115	0	-20	70	11.03
80	162	137.7	-82.5	140	20.8
85	115	0	-8	23	10.29
87	12.5	10	-5	7.5	14.85
89	238	202	-70	100	21
90	38.5	0	-32.73	32.73	10.4
91	35	0	-29.75	29.75	10.5
92	115	0	-3	21	10.5
99	115	0	-100	100	10.61
100	238	200	-90	130	15.3
103	75	60	-15	40	10.5
104	115	0	-8	23	10.19
105	115	0	-8	23	10.19
107	12.5	0	-10.63	10.63	10.29
110	115	0	-8	23	10.19
111	67	57	-30	35	15.3
112	10	0	-8.5	8.5	10.29
113	6	0	-5	5	10.61
116	217	184	-184.4	184.4	10.61

D

Chapter 3 Appendix: PV Farm Parameters

Table D.1: Main parameters of the PV power plant in Chapter 3

Parameter	Value
Rating power P	400 kW
Grid voltage U_g	260 V
DC voltage U_{dc}	500 V
Input filter capacitor C	0.02 F
Output filter inductor L_f	0.5 mH
Output filter capacitor C_f	100 μF
DC voltage control loop (K_{p1}, K_{i1})	(2, 150)
Active current control loop (K_{p2}, K_{i2})	(3, 200)
AC voltage control loop (K_{p3}, K_{i3})	(2, 150)
Reactive current control loop (K_{p4}, K_{i4})	(3, 200)
PLL (K_{p_pll}, K_{i_pll})	(50, 1000)