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INVESTIGATION OF A NEW CONFIGURATION OF A TWO-STAGE CMOS WIDEBAND AMPLIFIER AND A NEW CMOS WIDEBAND RF FRONT-END FOR MULTISTANDARD LOW-IF WIRELESS RECEIVERS

by

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A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science**

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To
Tanzina and Nojhat for their love and encouragement

Abstract

A front-end, a combination of a low noise amplifier and a frequency converter, is an important building block in a radio receiver system. Very weak radio frequency signals need to be amplified before they are translated to the intermediate frequency or baseband signals. For multistandard wireless communication systems operating at different carrier frequencies, one of the important requirements is wideband receiver front-end capable of handling all these frequencies. Therefore, attention is made to design wideband amplifier and front-end circuit for the multistandard low intermediate-frequency wireless receiver.

In this thesis, a new configuration of a two-stage wideband amplifier is proposed and designed in CMOS 0.18 μm technology. Dual loop negative feedback is used to achieve the input/output wideband matching with –3 dB bandwidth of larger than 2.5 GHz.

Using the new configuration of the proposed wideband amplifier as the low noise amplifier, a new wideband front-end is proposed and designed in CMOS 0.18 μm technology. The overall front-end circuit is highly linear with input bandwidth of larger than 3 GHz. All the designs are mathematically analyzed and the simulation results justify the functionality of the circuits.

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I will be always remembering my late Dad on my way of life. From thousands of miles way my Mom is always praying for me to be successful. The encouragement from my father-in-law and mother-in-law is invaluable.

I am extremely grateful to my loving wife and little lovely daughter for their sacrifice, love, encouragement and happiness. Without my wife support and sacrifice, I would never be able to finish my studies.

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Acronyms

AC	alternating current
BB	baseband
BJT	bipolar junction transistor
BW	bandwidth
CMRR	common mode rejection ratio
CMOS	complementary metal oxide semiconductor transistor
CG	common gate
CS	common source
DC	direct current
DECT	Digital European Cordless Telecommunications
DR	dynamic range
DSB	double sideband
FET	field-effect transistor
GaAs	gallium arsenide
GBW	gain-bandwidth
GHz	gigahertz
GPS	global positioning system

GSM	global system for mobile communications
GX	gain crossover
Hz	hertz
IC	integrated circuit
IF	intermediate frequency
IR	image rejection
kHz	kilohertz
LNA	low noise amplifier
LNC	low-noise converter
LO	local oscillator
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field-effect transistor
MIM	metal-insulator-metal
MHz	megahertz
NF	noise figure
NF_{min}	minimum noise figure
NMOS	N-type metal oxide semiconductor
Op-Amp	operational amplifier
PDF	probability density function
PSD	probability spectral density
PX	phase cross-over
RF	radio frequency
SiGe	silicon germanium

SNR	signal-to-noise ratio
SSB	single sideband
VLSI	very large scale integration
WCDMA	wide code division multiple access
WLAN	wireless local area network

List of Symbols

A	Ampere
Cgd	Gate-drain capacitance
Cgs	Gate-source capacitance
C_{OX}	Gate oxide capacitor
dB	Decibel
f	frequency in Hz
f_T	Unity gain cut-off frequency
G_m	Equivalent transconductance
g_m	Transconductance
g_{mb}	Body transconductance (when source is not connected to the bulk)
I_{DC}	DC current
i_d	Drain current
k	Boltzman constant
kf	stability factor
kT	Thermal energy
kΩ	Kilo-ohm
L	Length of the transistor gate

mA	milli-ampere
Q	Quality factor
q	Electron charge
R	Resistance
r_{ds}	Drain-source resistance
$S_{v(f)}$	Spectral density function
T	Absolute temperature
tox	Gate-oxide thickness
V	Voltage
VDD	DC power supply voltage
VSS	DC ground voltage
V_{DS}	The drain-source voltage
V_{GS}	The gate-source voltage
V_{SB}	The source-bulk potential
V_{TH}	Threshold voltage
V_{THN}	Threshold voltage of NMOS transistor
W	Width of the transistor gate
β	Feedback factor
γ	Body-effect coefficient
φ	Fermi level
λ	Channel-length modulation coefficient
μ	Carrier mobility
μ_n	Carrier mobility of N-type material

μm	Micro-meter
ω	Frequency in radian/sec
Ω	Ohm

Chapter 1

Introduction

1.1 Motivation

Wireless communications are expanding in many directions with tremendous growth of numerous standards and applications such as WLAN, WCDMA, GSM, GPS and DECT, operating at different carrier frequencies and bands [1], [2]. When hardware aspects are considered there is a persistent demand for a single-chip, light, inexpensive, low-power, hand-held portable terminal compatible with different standards and applications. Thus, in the future, radio frequency circuits for wireless communications need to be fully integrated on-chip, having the capability of covering a very wide rang of frequencies.

The majority of radio-frequency integrated-circuits (RFICs) are still implemented in GaAs or silicon bipolar technologies because of the higher speed of BJT and GaAs devices, which have higher unity-gain-cut-off frequency (f_t) [3], [4]. However, the continuous scaling of CMOS technology has driven toward the deep-submicron minimum feature size, reducing the minimum channel length of the MOS devices, and thereby increasing the f_t of the transistor [5]-[7]. Thus, with high f_t and high level of

integration, CMOS is becoming a viable technology for RFICs used in wireless communication systems. Again, in scaled CMOS process, a higher level of integration ensures higher degree of functionality with lower costs. Therefore, the rapid evolution of the wireless communication world has resulted in tremendous amount of research on building high performance radio frequency (RF) circuits in CMOS technology because of its very-large scale-integration (VLSI) features that lead to low power, small size and low cost solution for portable devices, equipments and systems.

In the last few years, various CMOS RF chips have been implemented with the ultimate goal of integrating an entire radio transceiver (combined transmitter and receiver) on a single chip [8], [9]. Again, with the increasing number of wireless standards operating at different carrier frequencies, the need for multiple standards (multistandard) transceiver systems is increasing [10]. Thus, an RF receiver front-end, a combination of a low noise amplifier (LNA) and a downconversion mixer needs to be able to cover a huge range of different carrier frequencies. Using one RF front-end for each standard and then, combining a number of such front-ends to cover all the frequency range will be very area inefficient and costly. Therefore, the straightforward approach is to integrate a wideband RF front-end capable of handling all the different carrier frequencies for different standards. Hence, it will be a cost effective and area efficient solution. In this way, a wideband front-end can easily be reused to achieve maximum hardware sharing and to have a higher performance/price ratio in comparison to the one chip-set for each standard. Since the first stage of a receiver front-end is an LNA, a wideband front-end needs either a wideband LNA [11], or a narrowband LNA with multiple passbands [12], or a tunable LNA [13]. Narrowband LNAs with multiple passbands are only suitable when the

passbands are well separated and their number is not more than two [12]. Tunable LNAs are very attractive but hard to design for a large tuning range. Hence, the motivation is to design a wideband amplifier that can be used as an LNA in the RF (radio frequency) stage, or as an IF (intermediate frequency) amplifier at the output of the front-end. With the advancement of continuously scaled down CMOS technology the use of MOS transistors at RF frequencies where BJT and GaAs devices were previously dominating gives designers the possibility to integrate wideband amplifiers with bandwidths of several GHz.

Increased level of integration driven by the need for both a better portability and a lower cost price has been very attractive for wireless communications. Today, most of the wireless receivers (heterodyne receivers) [14], [15] work at high intermediate frequency (50 MHz to 200 MHz), and still, they need a lot of off-chip discrete components. In recent years, low IF (several hundreds kHz to few MHz) receivers [16]-[19] have been successfully adapted for certain applications such as GSM [16], DECT [17], WLAN [18] or Bluetooth [19]. Low intermediate frequency (low-IF) receivers [20]-[23] avoid the use of expensive discrete components such as image-rejection (IR) filters, and thus, allow a higher level of integration. However, low-IF receivers still have image problems, so a recent research has been done in low-IF receivers architectures to reject image fully [20]-[23]. In traditional heterodyne receiver, designers use LNA and downconversion mixer, keeping in mind impedance matching to an IR filter (IR filter is in between the LNA and the mixer). A little has been done to exploit the benefit, the increased overall linearity [24], of not having an IR filter between the LNA and the mixer in low-IF receivers. Here,

the motivation is to design a highly linear wideband RF front-end to improve the feasibility of low-IF wireless receivers.

1.2 Objectives

The objectives of this research work include a number of goals and implementations:

1. Investigation of wideband amplifiers in CMOS 0.18 μm process, which are already proposed in the papers [25]-[28]. One of these amplifiers has been investigated in SiGe bipolar process [25] but no detailed analysis has been done yet in a CMOS process.

2. Investigation of a new two-stage CMOS wideband amplifier [27] that can be used as an LNA in the RF front-end and as an IF amplifier after the front-end. A systematic design approach is followed to realize the wideband amplifier such that its performance parameters are independent of the process. The new wideband amplifier was designed, implemented and fabricated in CMOS 0.18 μm process.

3. Design and implementation of a CMOS wideband RF front-end for low-IF wireless receivers. The RF front-end is designed by directly combining an LNA and a downconversion switching mixer where LNA is the wideband amplifier configuration designed in step 2 with certain modifications. The front-end was designed, implemented and fabricated in CMOS 0.18 μm process.

All the designs in this research work are optimized with respect to their respective performance parameters such as linearity, noise, gain, and bandwidth etc. The fabricated ICs will be tested to compare the measured results with the computer simulation results to verify the functionality of the actual device and justify the necessity of the implementation.

1.3 Thesis Overview

Chapter 2 presents a review of general issues in analog and RF circuit design, making it related to the RF front-end and its building blocks such as wideband amplifier, LNA and mixer. In this chapter, design issues such as gain, linearity, bandwidth and noise are discussed in detail. The overall effect of these design parameters in a cascaded system of multiple stages is also discussed. Accurate device modeling is an important factor that characterizes the circuit behavior. The transistor high frequency characteristics are far different than its low frequency characteristics. A brief review of CMOS transistor, its noise behavior and high frequency model are presented in this chapter.

In Chapter 3, design considerations and requirements for wideband amplifiers are discussed in detail. Negative feedback is the most common technique to achieve wide bandwidth with stable gain and better linearity. A preliminary discussion of some of wideband amplifiers based on single and multi-loop negative feedback is presented in this chapter to have a basic idea of designing and implementing issues.

In Chapter 4, the wideband amplifiers based on negative feedback and realized in CMOS process are discussed as a step forward to the implementation of the proposed new

wideband amplifier. A new CMOS two-stage wideband amplifier, its design approach, circuit analysis, realization and implementation are presented in this chapter. A comparative performance analysis of different wideband amplifiers shows the simplicity and feasibility of the proposed CMOS wideband amplifier.

A radio receiver front-end is a combination of two separate building blocks: a low-noise-amplifier (LNA) and a downconversion mixer. The performance of the entire front-end depends on the combined performance of LNA and mixer. Therefore, the design issues for the RF front-end are related to the design issues of its individual building blocks. In Chapter 5, the design considerations and requirements for RF front-ends are discussed in detail.

In Chapter 6, a new configuration of CMOS wideband RF front-end for multistandard low-IF receivers is investigated. The first stage of the front-end is a LNA, which is designed using the amplifier investigated in Chapter 4. A folded-cascode mixer is selected to combine it with LNA, keeping in mind the low-voltage design technique.

Summary and conclusions of the thesis are given in Chapter 7, illustrating the feasibility, simplicity and systematic design approaches of the proposed ICs in CMOS process.

Chapter 2

Analog and RF Design: Issues and Technology

In this chapter we present a brief overview of some commonly used general concepts, issues and terminologies in analog and RF design. In addition, a deep understanding of the device process technology in which the circuits will be implemented is essential. The second part of this chapter presents a brief overview of CMOS transistor models and characteristics in realization of high frequency analog and RF circuits.

2.1 Design Issues and Specifications

The performance characteristics of the analog and RF circuits are gain, bandwidth, distortion (nonlinearity), noise and input/output impedance [26], [29]-[31]. Apart from these, supply voltage, power dissipation, voltage swing and performance stability are the factors that need to be considered in the overall circuit design. At the system level, the specifications for the most of the parameters (e.g. gain, noise) must be determined before the circuit is designed. Nonidealities such as noise and nonlinearity deviate the circuit

performance from its ideal behavior and give rise to need for optimization of other parameters [31]. Noise, which is inherently present in all active and passive devices, limits the minimum detectable signal. On the other hand, nonlinearities limit the maximum signal amplitude, and thereby cause the output signal distortion [31]. In practice, most of the parameters trade with each other as illustrated in the "analog design octagon" of Figure 2.1 [29]. Such trade offs make the design a multi-dimensional optimization problem, and present many challenges in the design of high performance circuits. Here, we will discuss some of these design parameters and issues in detail.

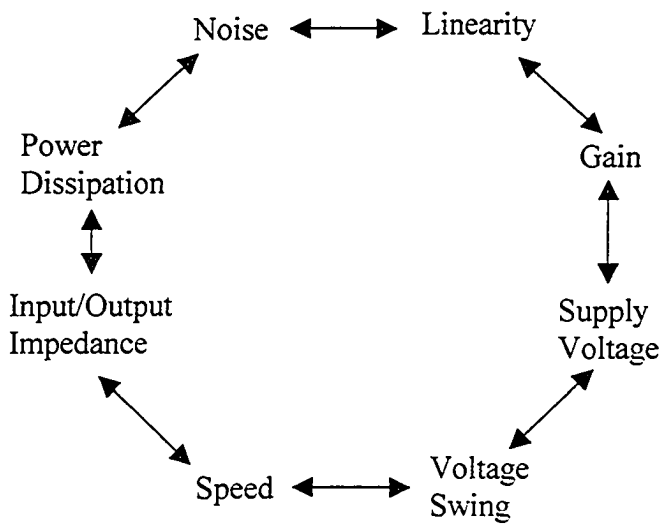


Figure 2.1 Analog design octagon [28].

2.1.1 Gain and Bandwidth

Typically, RF circuits have to deal with very weak signals. Input signals to a radio receiver system coming from antennas are very weak, while the output signals need to be

strong enough so that they can be processed in the following stages. It is therefore necessary to provide enough signal gain between input and output by amplifying stages (LNA, IF amplifier).

In analog and RF design, the most common terms used for "gain" are *voltage gain* and *power gain*. In low frequency analog design, the term *voltage gain* is commonly used. On the other hand, in high frequency applications (0.9 GHz – 5 GHz), RF designers use the broader term *power gain* that relates the signal powers. For a linear, memoryless and time-invariant system X in Figure 2.2, voltage gain A_V and power gain G_P can be expressed as

$$A_V = \frac{V_L}{V_S} \tag{2.1.1}$$

$$G_P = \frac{V_L^2 / R_L}{V_S^2 / R_S} = A_V^2 \frac{R_S}{R_L} \tag{2.1.2}$$

where the system X is driven by an external voltage source V_S with internal source impedance Z_S (= R_S Ω) and load voltage V_L is taken across load impedance Z_L (= R_L Ω).

Here, Z_i and Z_o are input and output impedance, respectively. To obtain maximum power transfer, the source and load impedances must be complex conjugate of the input and output impedances i.e. $Z_S = Z_i^*$ and $Z_L = Z_o^*$ [30]. Maximum gain for the system X occurs when matching is perfect. From equation (2.1.2) it is noted that power gain and voltage gain are related to each other. For $R_S = R_L$ (most of the RF systems are terminated with load and source impedance of 50 Ω [31]), power gain equals voltage gain when expressed in decibels (dB) as seen from equations (2.1.3) and (2.1.4).

$$A_V(dB) = 20\log_{10}\frac{V_L}{V_S}. \tag{2.1.3}$$

$$G_P(dB) = 10\log_{10}\frac{V_L^2/R_L}{V_S^2/R_S} = 20\log_{10}\frac{V_L}{V_S}. \tag{2.1.4}$$

However, in practice due to impedances mismatches, power gain hardly equals the voltage gain.

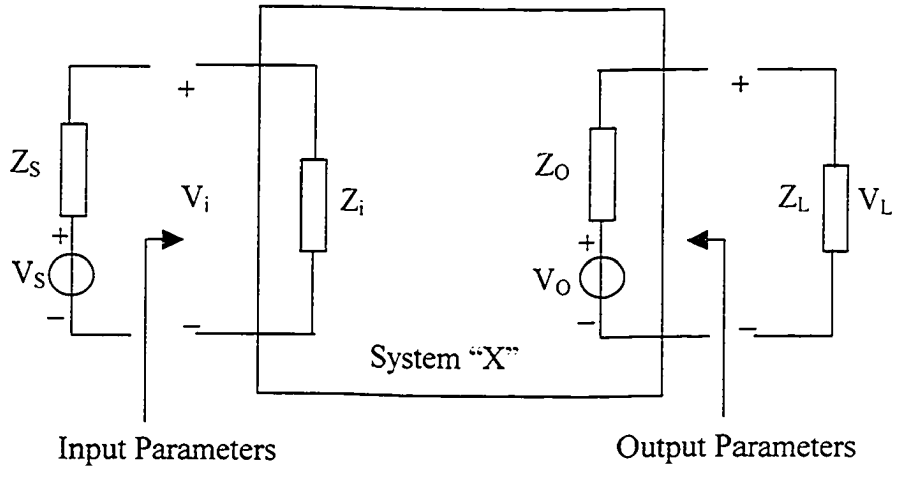


Figure 2.2 A linear, memoryless, and time-invariant two-port system.

Gain-bandwidth product is a useful measure of the amplifier performance. A transistor has a gain-bandwidth product that limits the gain-bandwidth product of the entire amplifier [26]. There are two typical high frequency figures of merit f_t (transistor's unity-gain-cut-off frequency) and f_{max} (maximum oscillation frequency) used to describe how fast a transistor will operate. f_t and f_{max} are the frequencies at which the current gain and

power gain of a transistor, respectively, become unity [32]. The voltage gain of an amplifier over a bandwidth wider than f_t can be not achieved i.e. the bandwidth of an amplifier is fundamentally limited by the transistor gain-bandwidth product [26]. On the circuit level, there are several ways to determine the gain-bandwidth product of an amplifier. To achieve higher gain, cascading of multiple stages is a popular method. In an N stage amplifier, the gain-bandwidth product is arbitrarily defined as [33]:

$$(GBW)_N = (Gain)^{1/N} BW \tag{2.1.5}$$

where N is the number of similar stages, *Gain* is the total midband gain (=N x gain of each stage), and BW is the overall bandwidth. The overall bandwidth of an N stage amplifier can be expressed as [33]

$$BW = B\sqrt{2^{1/N} - 1} \tag{2.1.6}$$

where B is the bandwidth of each stage. Note that bandwidth shrinks with increasing the number of stages. As N approaches infinity, the overall bandwidth tends toward zero. Thus, the overall gain-bandwidth product is

$$(GBW)_N = GB\sqrt{2^{1/N} - 1} \tag{2.1.7}$$

where G is the gain of each stage and *Gain* in (2.1.5) is replaced by G^N (*Gain*= N x G= G^N) . Note that as the number of stages increases, the amplifier gain-bandwidth is reduced. Thus, a reduction in the bandwidth by a factor increases the gain by the square of that factor. The gain-bandwidth of a simple single-stage amplifier is identical to the transistor gain-bandwidth product and the gain-bandwidth of a single-pole single-stage feedback amplifier is identical to that of the transistor gain-bandwidth product [26].

2.1.2 Noise and Noise Figure

Noise can be defined as any random interference and is inherently present in all physical systems [29]. It limits the minimum signal level that a circuit can process with acceptable quality [29]. Only signals larger than noise can be reliably detected. Thus, noise performance of a circuit is a primary concern when low-level signals need to be processed. Noise trades off with other design issues such as gain, bandwidth, linearity and power dissipation. Therefore, it is necessary for analog and RF designers to understand the impact of noise on circuit performance.

In analog signal processing, there are two different types of noise sources that can corrupt the desired signals. One is device electronic noise and the other one is "environmental noise" [29]. However, device electronic noise is the main concern for analog and RF designers (it is often said that if there were no noise, there would be no analog designers). Present in all resistors and active devices, noise can be classified as thermal noise, flicker noise and shot noise [29]. Like any other random process, noise is characterized by a PDF (probability density function) and a PSD (power spectral density) [14]. One of the most common thermal noise sources in a circuit is resistor. The thermal noise in a resistor is expressed with the spectral density function [29]

$$S_V(f) = 4kTR \tag{2.1.8}$$

where T is the Kelvin temperature of the resistor, k = 1.38x10^{-23} J/K is the Boltzmann constant and R is the value of resistor. Thus, $S_v(f)$ is expressed in V^2/Hz. Thermal noise is white noise as it has constant power spectral density with respect to frequency [29], [32].

Noise figure is one of the important parameters used to characterize the RF receiver front-end building blocks (LNA, mixer). As the signal is processed through a system, noise added from all the electronics is characterized by *Noise-Factor* (*F*) that can be expressed as [31]

$$F = 1 + \frac{N_{O(added)}}{N_{O(source)}} \tag{2.1.9}$$

where $N_{O(added)}$ is the noise at the output added by the electronics, and $N_{O(source)}$ is the noise at the output originating at the source. When expressed in decibels, the result is termed as the noise figure:

$$NF = 10\log_{10} F. \tag{2.1.10}$$

In RF design, the ultimate objective is to maximize the *SNR* because the higher the *SNR*, the higher the channel capacity of the circuit (the simplest form of Shannon's information theory is that the channel capacity increases logarithmically with the *SNR*)[31]. As the signal is processed through a system, *SNR* degrades due to the added noise. Again, the higher the added noise, the higher will be the noise figure. Thus, noise figure is a measure of how much the *SNR* degrades as the signal passes through a system and the most common definition for the noise figure is [14]

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{2.1.11}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output, respectively. For a system with number of cascaded stages (*N*) shown in Figure 2.3, the overall noise figure (or noise factor) can be expressed by the Friis equation [31], [32].

$$F_{N,Overall} = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + \ldots\ldots\ldots + \frac{(F_N - 1)}{\prod_{i=1}^{n} G_i} \tag{2.1.12}$$

Note that high gain of the preceding stage causes the effective noise figure in the later stage to be reduced.

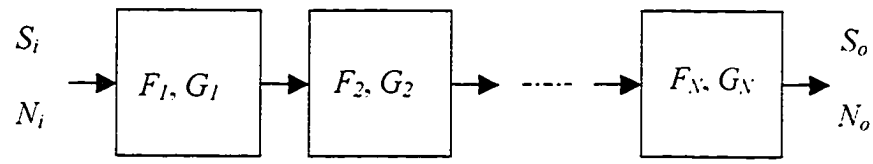


Figure 2.3 Noise figure in a cascaded system of N stages.

2.1.3 Linearity and Distortion

In an ideal system, the output signal is linearly proportional to the input signal. In practice, due to nonlinear distortion in actual devices, the output signal deviates from the expected signal based on linear transfer function. Nonlinearities often lead to phenomena such as harmonic distortion, gain compression, desensitization, blocking, and intermodulation [14]. Thus, the actual devices with nonlinear characteristics can approximate the linear behavior of an ideal device up to a certain level of the applied input signal [29] beyond which the output signal becomes distorted. Hence, the maximum tolerable signal power is determined by distortion. Nonlinearities set the upper bound or ceiling on the dynamic range of the receiver front-end (i.e. how large a signal can be processed in the receiver front-end without distortion) [32]. In analog and RF design,

linearity is characterized by the compression point (1-dB compression point) and the two-tone third-order intercept point [14], [31], [32].

The compression point is the value of an input signal to a system at which a calibrated departure from the ideal linear curve occurs as shown in Figure 2.4 [13], [31], [34]. In other words, the 1 dB compression point is defined as the input power level at which the actual output power level (large signal output) drops 1 dB below its ideal small signal value [34]. A memoryless, time-invariant system with nonlinearity up to the degree of three (3) can be expressed as [32], [34]

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1.13}$$

where α_1 is the linear or small signal gain of the system [34]. If a single-tone signal, $x(t) = A\cos\omega t$ is applied to a such system, then, after simplifying, equation (2.1.13) yields

$$y(t) \approx \left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right) A\cos\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \tag{2.1.14}$$

where the DC and 2nd order terms have been discarded. The fundamental-frequency coefficient $\alpha_1+(3\,\alpha_3 A^2)/4$ is the large signal gain [34]. Note that the small-signal gain α_1 is varied with the input signal amplitude due to the third order nonlinearity. In most systems, $\alpha_3<0$ and thus, the gain $(\alpha_1+(3\,\alpha_3 A^2)/4)$ of the system is a decreasing function of A (the input signal amplitude). From the definition of 1-dB compression point, the signal amplitude in volts at 1-dB point with single-tone applied can be written as [14]

$$A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.1.15}$$

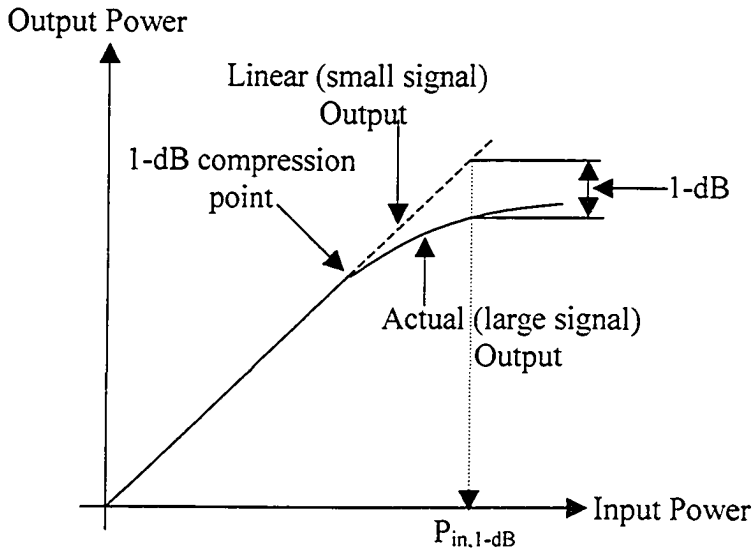


Figure 2.4 Definition of 1 dB compression point.

Besides of 1-dB compression point, nonlinear systems are characterized by the 3rd order intercept-point. It is derived when a two-tone signal, $x(t) = A\cos\omega_1 t + A\cos\omega_2 t$, is applied to a nonlinear system as depicted in Figure 2.5. This point results from intermodulation phenomena [14], [34].

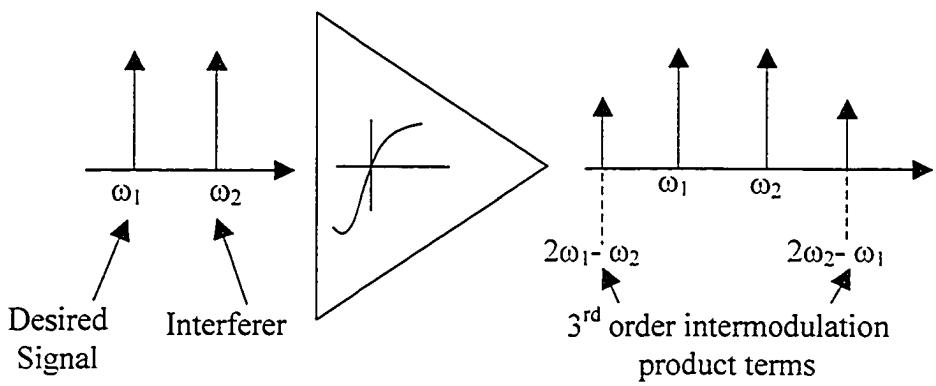


Figure-2.5 Intermodulation in a nonlinear system.

The first tone ($A\cos\omega_1 t$) represents the desired signal, whereas the second tone ($A\cos\omega_2 t$) represents the unwanted signal or interferer. Putting value of $x(t)$ in equation (2.1.13), and then, after expanding the right hand side and discarding all the DC terms and 2nd order harmonics, we obtain the intermodulation product terms, $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ [14]. The most unwanted terms are $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ because they fall in band of desired output (ω_1 and ω_2), if ω_1 is close to ω_2. The 3rd order intercept point is a fictitious point (or theoretical point) where the amplitudes of the intermodulation tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitudes of the fundamental tones at ω_1 and ω_2 [31]. Figure 2.6 shows the 3rd order intercept point graphically [14], [32] where the desired output and the 3rd order intermodulation output are plotted as a function of input power level in dBm [31], [32]. From the definition of 3rd intercept point, the signal amplitude in volts can be expressed as

$$A_{IP3} = \sqrt{\frac{4|\alpha_1|}{3|\alpha_3|}} \tag{2.1.16}$$

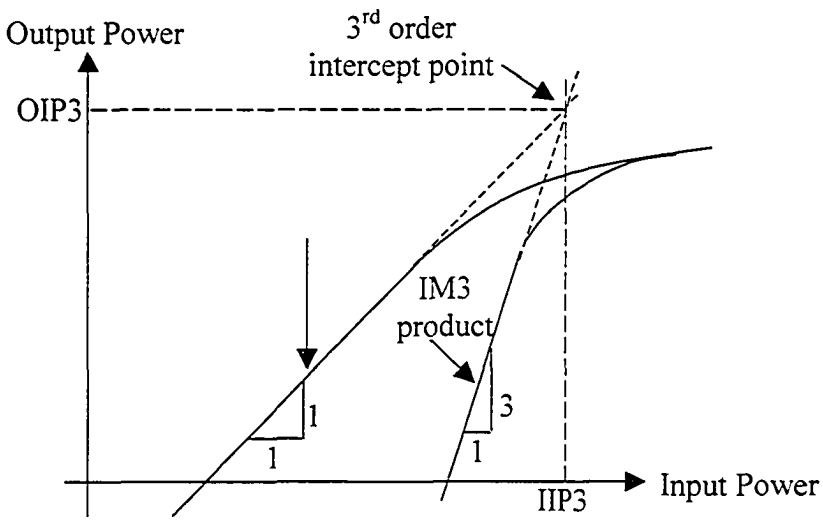


Figure 2.6 The graphical representation of 3rd order intercept point.

Customarily, 3rd order intercept point is quoted as *IP3*. When quoted as *IIP3*, it is called the input 3rd order intercept point referring to the input power and when quoted as *OIP3*, it is called the output 3rd order intercept point referring to the output power [32]. Note that there is a relationship between the 1-dB compression point and the *IP3* point. Thus from equation (2.1.15) and (2.1.16), $A_{1\text{-}dB}$ and A_{IP3} can be related as

$$\frac{A_{IP3}}{A_{1-dB}} = \frac{\sqrt{4/3}}{\sqrt{0.145}} = 3.04 \tag{2.1.17}$$

When expressed in decibels, (2.1.17) yields

$$20\left|\log_{10} A_{1-dB}\right| \approx 20\left|\log_{10} A_{IP3}\right| - 9.6. \tag{2.1.18}$$

Thus, one can estimate that the compression point is almost 10 dB below the intercept point with single-tone applied signal for $A_{1\text{-}dB}$ calculation. For a cascaded system of multiple stages shown in Figure 2.7, the overall *IP3* is approximated as [14]

$$\frac{1}{A_{IP3,O}^2} = \frac{1}{A_{IP3,1}^2} + \frac{\alpha_1^2}{A_{IP3,2}^2} + \frac{\alpha_1^2 \beta_1^2}{A_{IP3,3}^2} + \ldots \tag{2.1.19}$$

where $A_{IP3,i}$ represent the input *IP3* point of i^{th} stage. The coefficients α_1 and β_1 are the small signal gains of the first and the second stage, respectively.

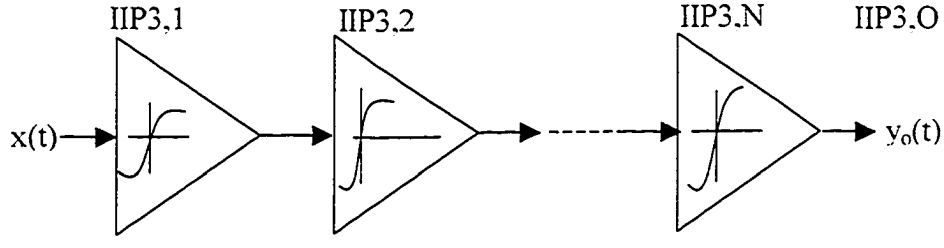


Figure 2.7 Overall *IIP3* (*IIP3,O*) in a cascaded system of multiple stages

Besides the above mentioned parameters, input/output impedance and their matching is an important factor in analog and RF design. Typically, most of the RF circuits are 50 Ω systems where external source and load impedances are 50 Ω (Z_S and Z_L in Figure 2.2). In matched condition, performance of the amplifiers becomes independent of the source and load impedances [29]. There are two types of matching, narrowband-matching (typically using inductors, capacitors) and wideband-matching. The most commonly used approach to the wideband matching is the use of resistive feedbacks, which makes input and output impedance of the circuit of interest equal to 50 Ω [26].

2.2 S-Parameters

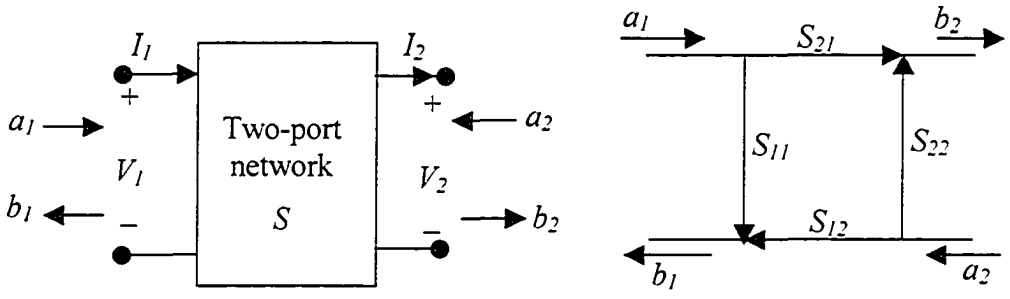
In analog and RF design, typically S parameters (scattering parameters) are used to specify the small signal performance of the circuits [30], [32] because it is quite difficult to provide adequate shorts or opens at very high frequencies to determine input/output impedance/admittance parameters that define signal amplitude at the respective terminals. For the two-port network as shown in Figure 2.8, incident and reflected power is calculated using S parameters. The S parameters are reflection or transmission coefficients and are defined by the following relationships [32].

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.2.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.2.2}$$

where a_1 is the input incident wave, b_1 is the input reflected wave, a_2 is the reverse transmitted wave and b_2 is the forward transmitted wave. S_{11} is the input reflection co-

efficient, S_{21} is the forward transmission coefficient, S_{22} is the output reflection coefficient and S_{12} is the reverse transmission coefficient. The additional information to determine these parameters can be obtained in [32]. S_{21} is the measure of forward gain and higher S_{21} indicates higher gain with impedance matching. For 50 Ω broadband matching, the values of S_{11} and S_{22} should be below –10 dB in the bandwidth of interest. S_{12} should be as low as possible (< -60 to –100 dB) [31], [32]. High reverse transmission reduces gain and increases noise.



(a) Reflected & transmitted waves with voltages and currents

(b) Reflected & transmitted waves with S parameters

Figure 2.8 Two-port networks and S-parameters.

2.3 CMOS Technology Review

Although the rapid progress of process technology has benefited RF fabrication, the design of analog and RF circuits in CMOS technology faces increasing challenges because of inadequate characterization and modeling of MOS transistors in deep-submicron CMOS process (0.5 μm – 0.09 μm) [1]. It becomes difficult to analyze and predict circuit behavior on transistor level without accurate models. At the present there

are substantial discrepancies between simulated and measured results. Therefore, it is necessary to have a good understanding of transistor models and parameters in the technology that is being used. In this section, a brief overview of MOS transistor models, and parameters will be presented.

2.3.1 MOS Small-Signal Models and Parameters

With long channel approximation ($L>4\mu m$ in 0.18 um technology), CMOS square-law equation for an NMOS transistor can be written as [29], [32].

$$i_{D,sat} = \frac{\mu_n C_{oxn}}{2}\frac{W}{L}(v_{GS} - V_{THN})^2 \tag{2.3.1}$$

In derivation of this equation, the second-order effects such as body effect (represented by coefficient, γ) and the channel-length modulation (represented by coefficient, λ) were neglected [29]. The body effect is significant in analog design when multiple transistors are stacked one upon another between the power rails because V_{THN} (threshold voltage) of the bottom transistor is different from that of the top transistor. V_{THN} is defined as [29]

$$V_{THN} = V_{THO} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{2.3.2}$$

V_{SB}, voltage between source and bulk, is different for the top and bottom transistor in the stack. In analog design, typically, transistors are kept in saturation with the condition that $V_{DS} \geq V_{GS}-V_{TH}$. Here, V_{DS} represents the voltage between drain and source of the transistor and V_{GS} is the voltage between the gate and source. $V_{GS}-V_{TH}$ is termed as overdrive voltage. Thus, V_{GS} must be sufficient enough to keep the transistor on with a correct

prediction of V_{TH}. In saturation, a MOSFET produces a current in response to its gate-source overdrive voltage, i.e. a change in the drain current occurs with a change in the gate-source voltage. Thus, the device "transconductance" g_m is defined as [29]

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{v_{DS,constant}} \tag{2.3.4}$$

$$= \mu_n C_{oxn} \frac{W}{L}(v_{GS} - V_{THN}) \tag{2.3.5}$$

For short-channel MOS transistors, more accurate and complex equations have been developed to realize the *I/V* characteristics and can be found in [29], [31], [32]. However, the circuit behavior with short-channel devices can be approximated with long-channel device characteristics as a first approximation [29].

Once the DC operating point (bias voltages and currents) of the transistor is determined, the small signal model of the transistor can be defined in terms of large signals (DC signals). A low-frequency small signal model of NMOS transistor is shown in Figure 2.9 [29], [35].

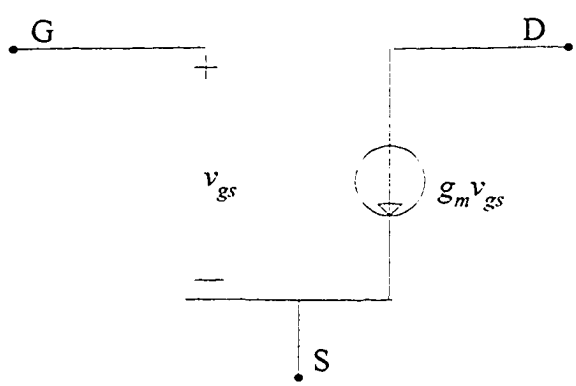


Figure: 2.9 MOS small-signal model.

At high frequencies (RF), the device capacitances become very significant in determining the circuit behavior. Besides, each terminal of the MOSFET exhibits a finite ohmic resistance due to the resistivity of the material. A more accurate transistor model with device capacitances and resistances can be found in [29], [35]. However, using the high frequency model, it is difficult to analyze any RF circuit consisting of two or more transistors.

2.4 Conclusion

In this chapter, a number of design issues and specifications that characterize the performance of analog and RF integrated circuits were discussed. A brief overview of CMOS transistor models and parameters was presented also. At the system level, specifications for gain-bandwidth, noise, linearity, input/output impedance, matching criteria and trades-off among these must be determined before the circuit can be designed. The impact of noise on minimum detectable signals and the effect of nonlinearity on distortion need to be understood to design high performance analog and RF integrated circuits with realistic specification.

On the other hand, it is necessary to have the accurate MOSFET device models, especially with respect to noise performance and nonlinear distortion. If they are at hand, the discrepancies between the simulated and the measured results are reduced.

Chapter 3

Wideband Amplifier

An amplifier is an important circuit in analog and RF design. For example, a signal coming from an antenna is very weak, and needs to be amplified at the first stage of a receiver front-end. Here, we need an amplifier with a bandwidth around several GHz because of high frequency RF signals. On the other hand, for baseband signals with bandwidth around several kHz or close to DC, we need a low-frequency amplifier. An amplifier should provide linear gain within this wide range of frequencies.

Feedback is a commonly used technique in the design of wideband amplifiers to provide stable gain over process and supply variations, wider bandwidth, lower distortion, and accurate control of input/output impedance [26]. The bandwidth of the amplifier is limited by the transistor's gain-bandwidth product as stated earlier in Section 2.1.1. Feedbacks allow the designer to trade gain for bandwidth for the transistor with the same gain-bandwidth product. In this chapter, we will discuss design issues and considerations for wideband amplifiers.

3.1 Design Considerations and Requirements

Apart from gain and bandwidth, the important characteristics of a wideband amplifier are noise, distortion (nonlinearity), accurate input/output impedances and stability. Feedback is in the heart of wideband amplification and frequency-independent feedback networks are employed to optimize the performance of wideband amplifiers. In the design of wideband amplifiers, one has to consider the following requirements [35]:

1. Accurate gain characteristics: One of the important requirements in wideband amplifier design is perfect gain characteristics, which must be maintained stable within a certain tolerance level over process, temperature and supply voltage variations. Gain also needs to be independent of device parameters, source and load impedance. This can be achieved effectively by using feedback [29], [35]. Normally, feedback reduces gain and increases bandwidth [26], [35]. However, improper feedback can drastically reduce gain with a little improvement in bandwidth.

2. Wide bandwidth: The frequency response of the amplifier is required to be flat within a certain level of tolerance over the entire bandwidth (frequency range from dc gain to –3 dB gain). This is also achieved by using feedback, which relocates the closed-loop transfer function pole position to modify bandwidth [29].

3. Low noise characteristics: Low noise and noise figure are among the key requirements of wideband amplifier design. To meet these criteria, active loads and high value resistances need to be eliminated in the signal paths because of

their poor noise characteristics [26] [29]. The high resistive loads reduce the bandwidth by increasing the time constants.

4. Linear signal transfer: The signal must be amplified with minimum distortion (suppression of nonlinearity) over its specified dynamic range and this also can be achieved by feedback in acquiring adequate loop gain [26], [29], [35].

5. Input and output impedance control: The amplifier needs to be interfaced with other circuits and systems, which have specific impedance requirements. In broadband design, resistive feedbacks are used to set input and output impedance to the required levels [26], [29].

6. Stability: Stability over gain, noise and bandwidth can be achieved by employing feedback properly [26].

The above requirements are intended in the design of wideband amplifiers to achieve optimum performance. However, the actual design requires a fair compromise between various conflicting requirements that determine the particular circuit configuration to be used. From the observation of above requirements, a new set of general considerations are formulated in the design of wideband amplifier [36]:

1. Feedback is indispensable to obtain well-defined value of gain and bandwidth.

2. Using multi-loop feedbacks to achieve accurate gain, increased linearity and minimized noise.

3. Applying feedback around individual amplifier stages in the multi-stage configurations for higher stability.

3.2 Two-Stage Amplifier Design

One-stage amplifiers often do not provide adequate gain because of the low transconductance (g_m) that can be achieved in a single stage. Again negative feedback is very common in amplifier design that allows high-precision signal processing. Two-stage amplifiers offer higher gain, and the straightforward way to create a two-stage amplifier is cascading of two single stage amplifiers as shown in Figure 3.1. Cascading more than two stages makes it extremely difficult to guarantee stability in the feedback system because each gain stage introduces at least one pole in the open-loop transfer function [29]. Therefore, amplifiers with more than two stages are rarely used.

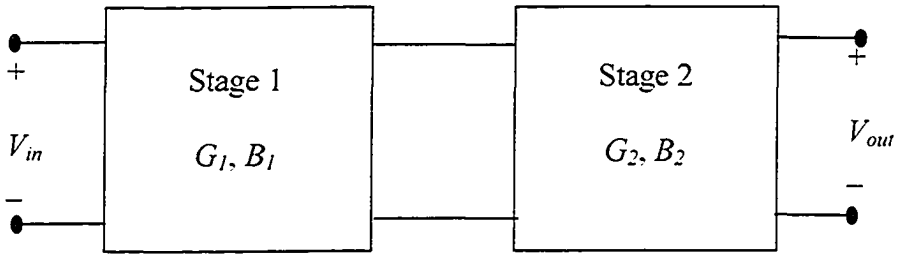


Figure 3.1 A two-stage cascaded amplifier.

The negative feedback [37] is widely used in the design of wideband amplifiers because of the following benefits [26], [29]:

1. Negative feedback desensitizes the gain, making closed-loop gain of the amplifier independent of the transistor parameters.

2. Negative feedback modifies input and output impedances, making wideband matching to the specific impedance without using inductive elements.
3. Negative feedback causes an increase in the bandwidth due to the gain desensitization property of the feedback.
4. Negative feedback suppresses the variation of the small-signal gain with input level, which can be viewed as reduction of nonlinearity.

3.2.1 Negative Feedback Amplifiers

As stated earlier, negative feedback is in the heart of wideband amplification and is frequently used in the design of wideband amplifiers. A basic amplifier (A_{OL}) along with a negative feedback (β) forms the negative feedback amplifier as shown in Figure 3.2 [38]. Here, A_{OL} is the open-loop forward gain of the basic amplifier, β is the frequency-independent feedback factor and $A_{OL}\beta$ is the loop gain. Z_i/Z_o is the open loop input/output impedance and $Z_{i,CL.}/Z_{oCL.}$ is the closed loop input/output impedance.

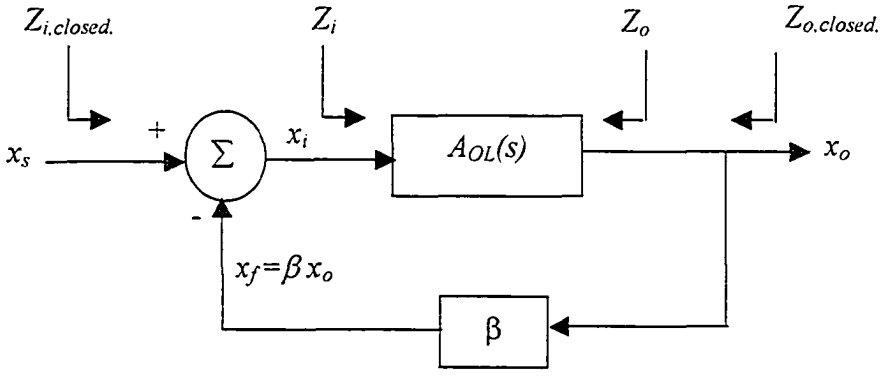


Figure 3.2 Negative feedback concepts.

The subtraction (x_s-x_f) is referred to as series/shunt if the variables (x_s, x_i, x_f) become voltage/current at the input of the amplifier. On the other hand, the measuring of output variable (x_o) is current/voltage. Based on different types of subtracting and measuring variables, the effects on the parameters (Z_i, Z_o and A_{OL}) of different negative feedback amplifiers can be found in [29], [38]. For the negative feedback system in Figure 3.2, the closed loop transfer function is

$$A_{CL}(s) = \frac{x_o}{x_s}(s) = \frac{A_{OL}(s)}{1 + \beta A_{OL}(s)} \tag{3.2.1}$$

Note that gain decreases with feedback and as it is possible to show bandwidth increases to preserve the constant gain-bandwidth product. If the loop gain becomes very high ($A_{OL}\beta$>>1), then gain and impedances depend only on the feedback factor (β). In this way, by feedback, gain can be desensitized and input/output impedance also can be modified. To achieve the prescribed gain and bandwidth along with input/output impedances matched to certain values, multiple feedbacks are often used. In the design of two-stage amplifiers, two single-stage feedbacks (local feedbacks) or two two-stage feedbacks (global feedbacks) or a combination of a single-stage feedback and a two-stage feedback can be used.

Stability is a critical concern when applying negative feedback because it may cause a phase shift in the input signal large enough so that the feedback becomes positive resulting in an unstable system [29], [38]. The stability of the system in Figure 3.2 can be defined with frequency responses as shown in Figure 3.3. To ensure stability with negative feedback, gain crossover (GX) must occur well before the phase crossover (PX), i.e. $|A_{OL}\beta|$ must drop to unity (0 dB) before $\angle\beta A_{OL}$ crosses -180^0 [29]. The greater the

distance between GX and PX, the more stable the feedback system becomes [29]. For smaller margin between GX and PX, the frequency response of the feedback system suffers from a sharp peaking at the GX point [29]. Thus, larger phase margin ensures stable system, while smaller phase margin results in peaking at the gain crossover frequency (ω_c) as shown in Figure 3.3. Therefore, frequency compensation techniques are needed to have optimum value of phase margin that results in "no peaking" or "negligible peaking" in the frequency response curve.

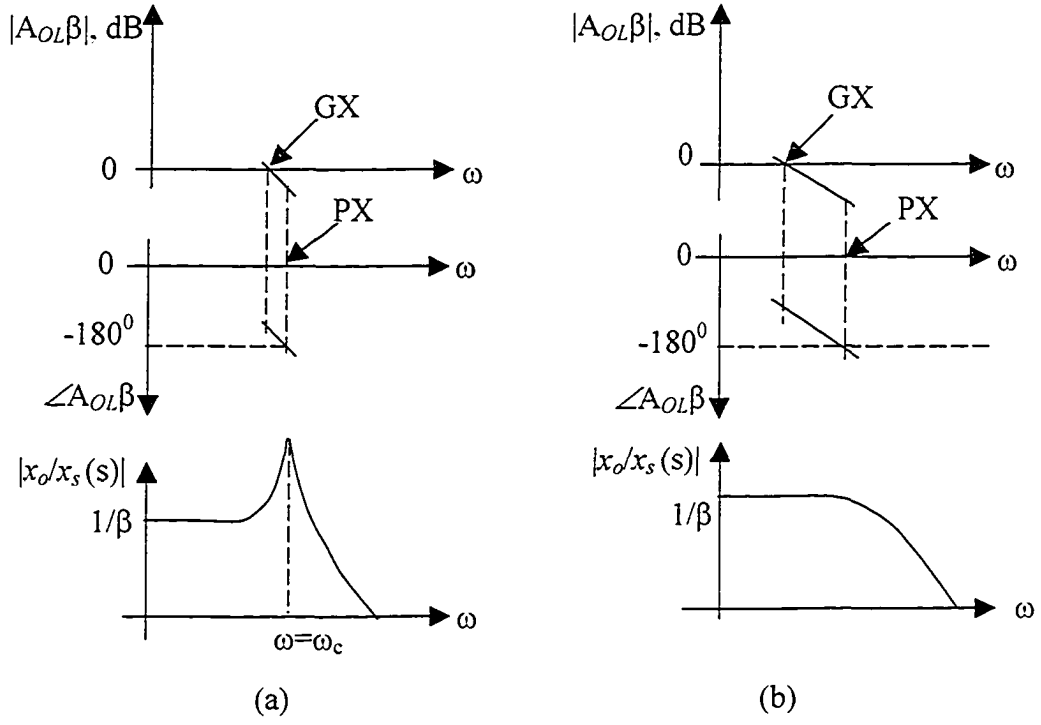


Figure 3.3 Closed-loop frequency responses for (a) small and (b) large margin between GX and PX point.

The stability problem due to the inadequate phase margin can be overcome either by dominant pole compensation or by introducing a *feedback zero* [26], [29]. The dominant-

pole compensation technique reduces gain-bandwidth significantly, and therefore, it is not suitable for wideband amplifier design [26]. On the other hand, feedback-zero technique does not affect the gain-bandwidth significantly, and therefore, it is very suitable for wideband amplification [26]. In feedback-zero compensation technique as shown in Figure 3.4, a capacitor is placed around the feedback element that increases feedback at high frequencies giving extra phase lead to compensate the phase lag in the amplifier [26], [39].

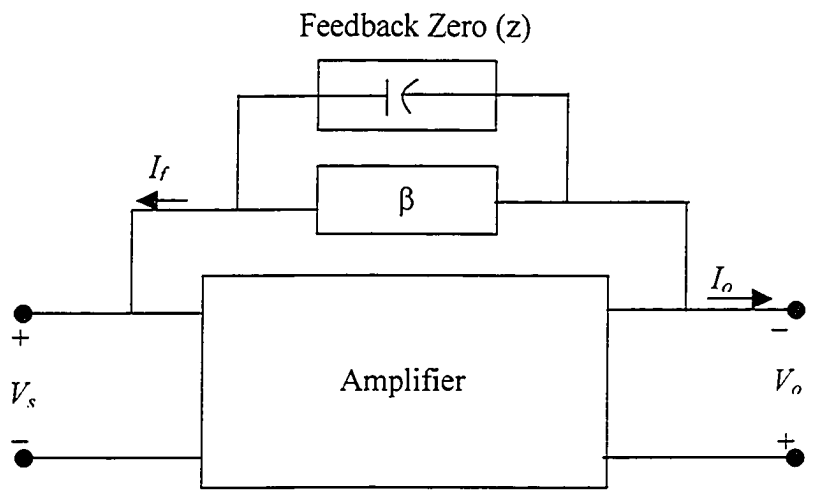


Figure 3.4 Frequency compensation technique by feedback zero.

As mentioned earlier, cascading more than two-stages complicates the stability problem due to having more than two poles that makes frequency compensation technique extremely difficult to get adequate bandwidth. Therefore, two-stage amplifier configuration is more commonly used and it also the choice for the wideband amplifier for this thesis.

3.3 Wideband Matched-Impedance Amplifiers

Here, the design issue is widening bandwidth along with impedance matching at the input/output terminals throughout the bandwidth. In high frequency amplifier design, some of the ways of increasing bandwidth are using inductors or resistors [32] by exploiting the negative feedback. In inductive broadbanding (using inductors), it is often required to use high values of inductors, which are impossible to integrate fully on chip. On the other hand, resistive broadbanding (using resistors only) has the advantage of requiring less chip area with the possibility of high level of integration. In addition to the bandwidth enhancement, resistive broadbanding can be simultaneously used to set terminal impedances matched to a specified system impedance (50 Ω). Thus, the matched impedance level internal to the chip using resistive broadbanding has the advantage of reduced sensitivity to parasitics. In this section, we will discuss resistive broadbanding that is simultaneously used for increasing bandwidth and impedance matching.

3.3.1 Resistive Broadbanding

As mentioned earlier, negative feedback (Fig. 3.2) modifies input and output impedances of different feedback amplifiers. Now, negative feedback increases bandwidth can be explained by the frequency-compensation behavior of the feedback circuit shown in Figure 3.5. As a first approximation, the frequency-dependant behavior of all the basic amplifiers can be characterized by one dominant pole, while neglecting other non-dominant poles. If the feedforward amplifier in Figure 3.2 has a one-pole transfer function, $A_{OL}(s)$ such that the close-loop transfer function is [29]

$$A_{CL}(s) = \frac{A_{o,n}}{1 + \frac{s}{\omega_{p,n}}} \tag{3.3.1}$$

where $\omega_{p,n}$ (= $\omega_p\{1+\beta A_o\}$) is the new dominant-pole location, and $A_{o,p}$ (= $A_o/\{1+\beta A_o\}$) is the new DC gain as shown in Figure 3.5. Note that new pole, $\omega_{p,n}$ has been shifted from the origin by the factor that is equal to the factor by which DC gain has been reduced. Thus, the new pole location $\omega_{p,n}$ shifts upward resulting in increased bandwidth and reduced gain. In this way, resistive broadbanding makes bandwidth wider by changing closed-loop pole location [34], [39]. Resistive broadbanding works on one pole only (i.e. a single-pole is shifted like in Figure 3.4).

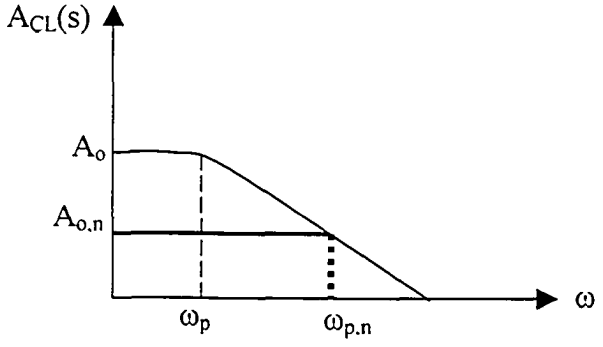


Figure 3.5 Bandwidth increase by negative feedback

Now, we will see how feedback works in two-stage or multistage amplifiers. In Section 2.1.1, it was shown in equations (2.1.6) and (2.1.7) that cascading identical stages in a system increase gain and decrease bandwidth. Therefore, multistage wideband amplifiers built up of several identical stages with nearly identical poles are not a good configuration due to significant bandwidth reduction. To compensate for the loss in

bandwidth in a cascaded system, the first approach is to reduce stage gain and increase bandwidth by local feedback (series or shunt feedback) around the stage as shown in Figure 3.6. In multistage amplifiers, there may be a number of poles. The poles should be distributed such that an optimum overall transfer function is obtained that leads to the maximally flat frequency response [39]. If stages contribute zeros they can be cancelled by poles in the other stages so that closed loop transfer function become an all-pole transfer function. As discussed earlier in this section, feedbacks can relocate the pole positions efficiently. Thus, in two-stage or multistage amplifiers, both local feedback and global feedback (or, overall feedback), shown in Figure 3.6, can be used to have the desired pole pattern. Local feedback ensures better stability, while global feedback with larger loop gain ensures better reduction of distortion, better accuracy, and better noise figure [39].

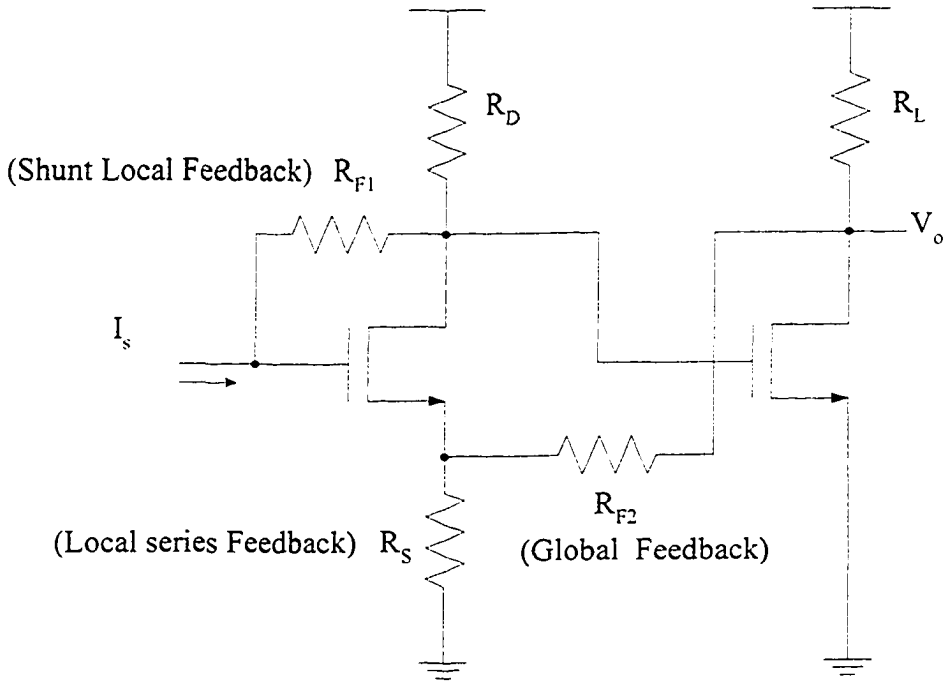


Figure 3.6 Global and local feedbacks in a two-stage amplifier

3.3.2 Stage Selection for the Two-stage Amplifiers

Typically, in the design of feedback amplifiers, the objective is to maximize the loop gain so that amplifier performances become independent of device parameters and DC operating points. In this case, common-source (CS) stage is natural choice because it gives very high gain to have high loop gain. On the other hand, common-gate (CG) or source-follower has gain close to unity. However, cascading CS stages are not unilateral and they are also interactive that hampers the designability. A CS gain stage has high input impedance and low output impedance. Therefore, there is impedance mismatching between the stages. Thus transfer of a stage is not independent of output impedance of the preceding stage and/or the input impedance of its successor. Therefore, a buffer stage is added between the CS stages that hardly contributes to the gain of the open-loop and provides the desired mutual isolation between the stages. The source-follower is the most common choice as a buffer stage because of its high input impedance and low output impedance. Therefore, it has no loading effect to the preceding stage or succeeding stage.

3.4 Conclusion

In this chapter, design issues and considerations for wideband amplifier were discussed in detail. Negative feedbacks were exploited for wideband amplifier design. A two-stage amplifier is the best choice for adequate gain, better stability and bandwidth with individual stage of common-source configuration. Matching, stability and bandwidth are optimized simultaneously using local and global feedbacks with adequate loop gain.

Chapter 4

Investigation of CMOS Wideband Amplifiers

In Chapter 3, a number of general design issues such as gain, bandwidth, stability and matching for wideband amplifiers were discussed in detail. The limitations of single-stage amplifiers and the restrictions for designing amplifiers including more than two stages have also been illustrated in Chapter 3. Two of the widely used circuits for wideband amplifiers are Kukielka configuration [40] and Meyer configuration [41]. These are two-stage amplifiers, and they were realized in Si bipolar processes.

The realization of wideband amplifiers in CMOS process needs new approaches and techniques due to different DC operating characteristics of CMOS transistors than those of bipolar transistors. On circuit level, the most difficulties arise in biasing CMOS transistors as no DC currents flow through the gates of MOS devices. Therefore, additional biasing networks need to be established in conjunction with the gain stages of the amplifiers. At the technology level, CMOS devices have low small-signal transconductance that lead to the lower value of loop-gain ($A_{OL}\beta$). With such a small-loop gain it is difficult to exploit the advantages of negative feedback in achieving stable gain, adequate bandwidth and perfect matching [26], [29], [41] ensuring these parameters are independent of process, device dimensions and DC operating points. As discussed

earlier in section 3.3.2, common-source (CS) configuration is the best suitable candidate for the implementation of individual stages of a two-stage amplifier.

In this chapter, the Kukielka [40] and Meyer configurations [41] are investigated in CMOS 0.18 μm process as a preliminary step to estimate the feasibility of the two-stage amplifiers in CMOS process. Then, a new configuration for a two-stage CMOS wideband amplifier is proposed that will be realized with systematic design approaches and techniques. The proposed wideband amplifier is analyzed and simulated in association with step-forward discussions of the amplifiers [40], [41] in CMOS process.

4 .1 CMOS Amplifier of Kukielka Configuration

The schematic of two stage CMOS wideband amplifier referred to as the Kukielka configuration is shown Figure 4.1 [26], [27]. The circuit is a cascaded connection of two source-degenerated common-source stages. The input stage consists of an NMOS transistor *M1* driving the output stage, which consists of NMOS transistor *M2*. A local series (series-series) feedback consisting of source-degenerated resistor R_{SS1} gives high input impedance at the first stage. On the other hand, a local shunt (shunt-shunt) feedback consisting of resistor R_{F2} gives a low-impedance at the input node of the second stage. Then, a global shunt (shunt-shunt) feedback with resistor R_{F1} brings overall input and output impedance of the circuit matched to the source (R_S=R) and load (R_{Load}=R) impedance respectively. C_B is the external DC blocking capacitor.

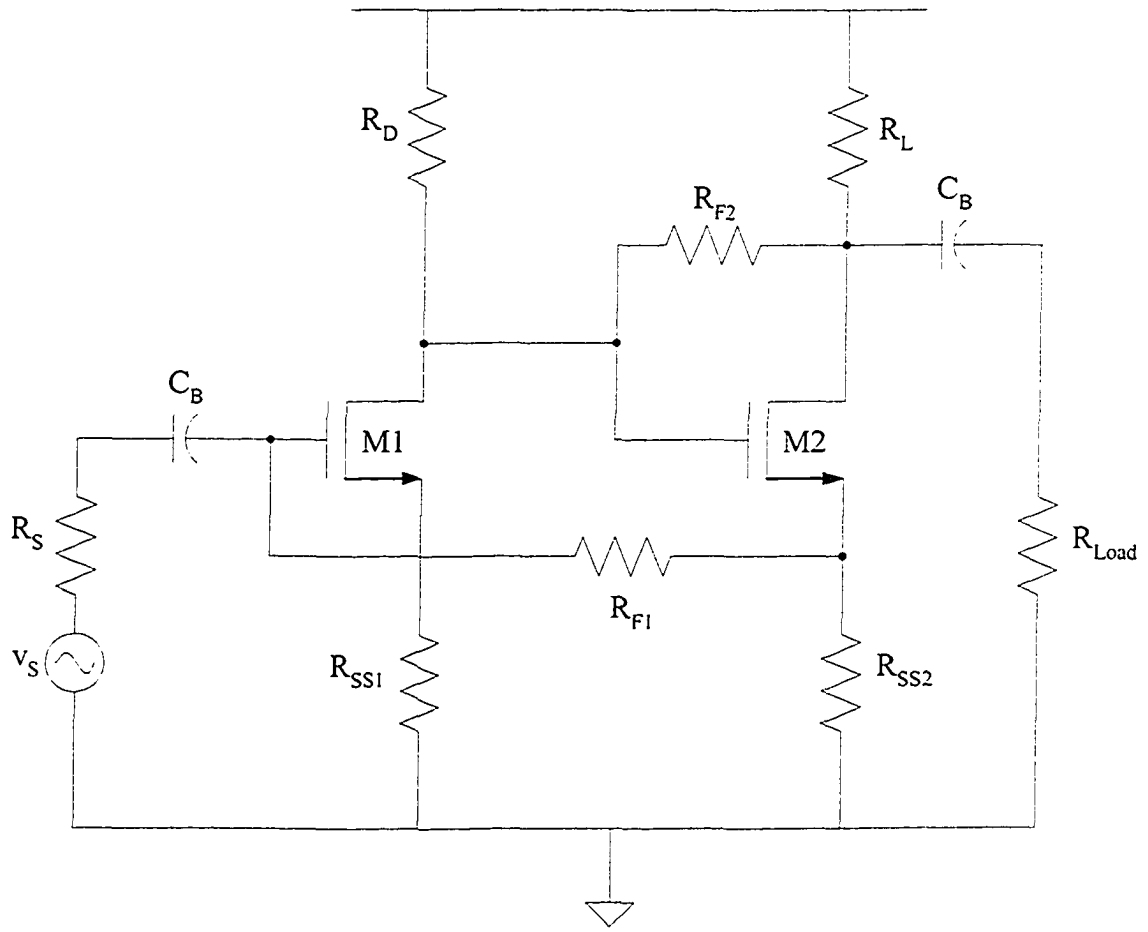


Figure 4.1 CMOS Kukielka configuration.

From a small-signal low-frequency analysis of the circuit in Figure 4.1, the expressions for voltage gain (A_V), input impedance (R_{in}) and output impedance (R_{out}) have been derived in [27]. Thus, with assumptions of $g_{m1}R_{SS1}>>1$, $g_{m2}R_{SS2}>>1$ and considering R_{F1}, R_{F2} are very large ($R_{F1}>>R_{SS1}$ and $R_{F2}>>R_{SS2}$, R_L), the voltage gain (A_V), input impedance (R_{in}) and output impedance (R_{out}) of this amplifier are approximated as [27]

$$A_V = -\frac{R_D}{R_{SS1}}. \tag{4.1.1}$$

$$R_{in} = \frac{R_{F1}}{1 + \frac{R_D}{R_{SS1}}}. \tag{4.1.2}$$

$$R_{out} = \frac{R_{F1} + R_D}{1 + \frac{R_D}{R_{SS2}}}. \tag{4.1.3}$$

For maximum gain and power transfer, the input and output impedance must be matched to the source and load impedance respectively. For the typical case of R_S=R_{Load}=R=R_{in}=R_{out}, the following condition in equation (4.1.4) needs to be satisfied.

$$\frac{R_{F1}}{1 + \frac{R_D}{R_{SS1}}} = \frac{R_{F1} + R_D}{1 + \frac{R_D}{R_{SS2}}} = R. \tag{4.1.4}$$

Now, for improved gain stability and maximally flat frequency responses, the circuit in Figure 4.1 is further modified as shown in Figure 4.2. In the open-loop transfer function for this two-stage amplifier of Kukielka configuration, there are two dominant poles (ω_{P1}, at the input node and ω_{P2}, at the output node). The local series feedback resistor, R_{SS1} is used to adjust ω_{P1}, while shunt feedback resistor R_{F2} and series resistor R_{SS2} is used to adjust ω_{P2}, so that two poles coincide with each other leaving only one dominant pole [28]. Then, the global feedback resistor R_{F1} in association with parallel capacitor C_{F1} provides the required loop gain to attain maximally flat frequency response. The capacitor C_{SS2} in parallel R_{SS2} is used to introduce peaking to compensate for the over-damped characteristics of this amplifier [26]. Thus, C_{SS2} assists in achieving large and improved bandwidth. However, large values of capacitance C_{SS2} create stability problem because at high frequencies, R_{SS2} is almost shorted out by C_{SS2} [26], [28], [32].

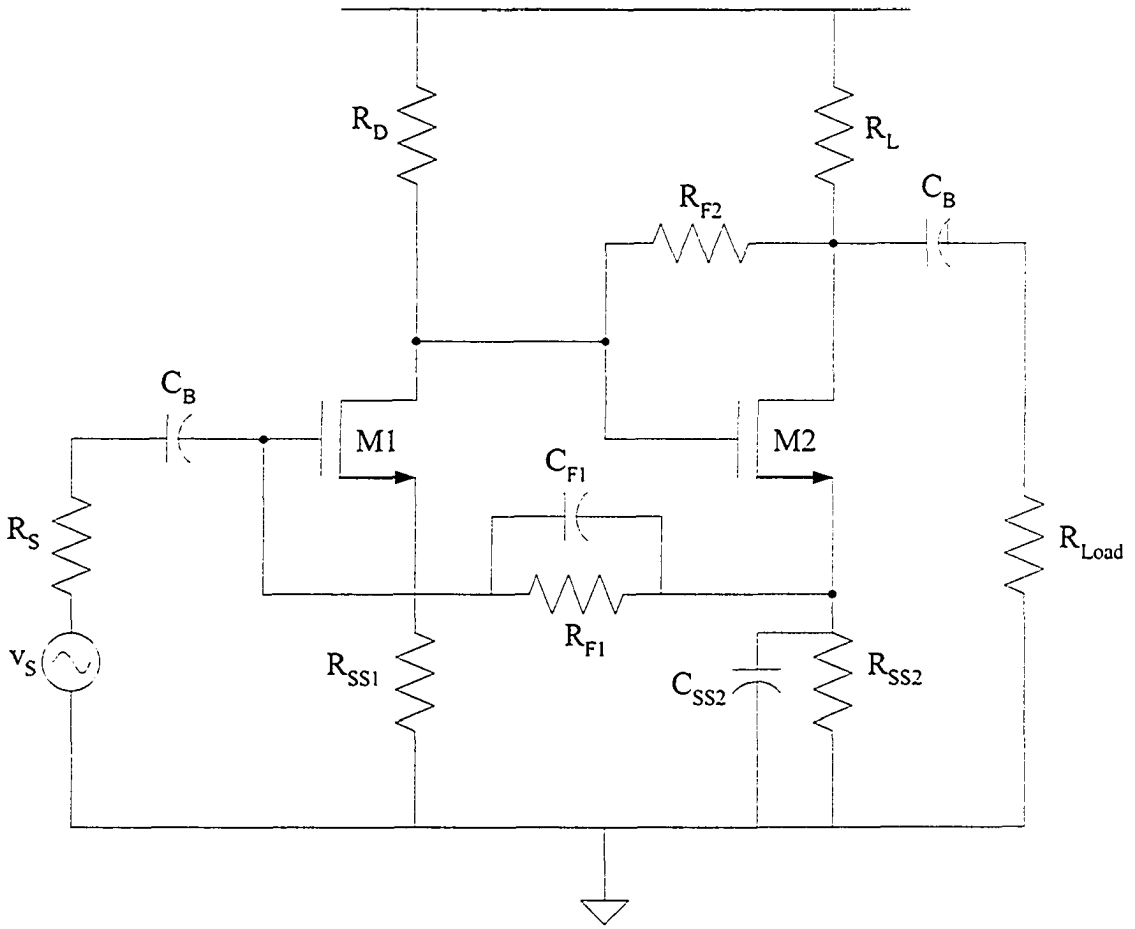


Figure 4.2 The modified Kukielka configuration for improved frequency response.

4 .1.1 Simulation: Results and Analysis

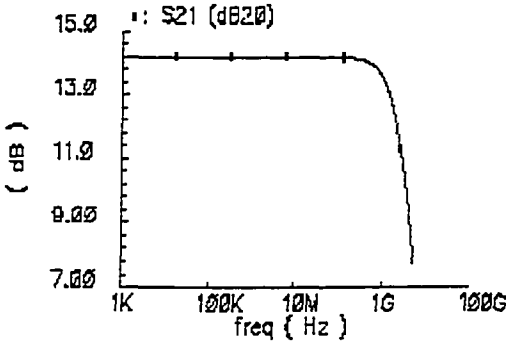
The circuit in Figure 4.2 is realized in CMOS 0.18 μm process and simulated using circuit simulator SpectreRF in *Cadence*, a suite of interactive CAD tools [42]. In simulation, performance parameters such as gain, bandwidth and noise figure are optimized keeping input/output matched to 50 Ω. The parametric values of all components of the circuit in Figure 4.2 are summarized in Table 4.1 of for an estimated

optimum performance. *M1* is biased externally with sufficient gate overdrive voltage (V_{GS}-V_{TH}) such that the condition, $V_{DS} > (V_{GS}-V_{TH})$ is satisfied.

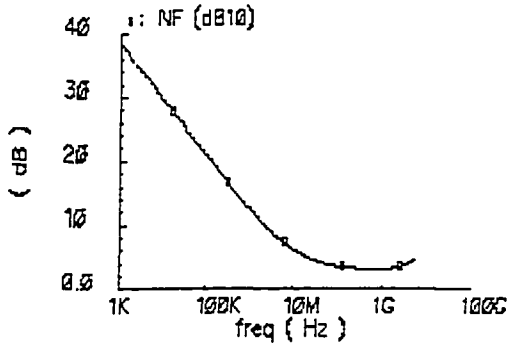
Table-4.1: Summary of the components of the circuit in Figure 4.2

Component	Component parameter	Value
M1	*W1/L*	450 µm/ 0.18 µm
M2	*W2/L*	250µm/ 0.18 µm
R_D	-	300 Ω
R_L	-	60 Ω
R_{SS1}	-	5 Ω
R_{SS2}	-	25 Ω
R_{F1}	-	300 Ω
R_{F2}	-	2.2 kΩ
C_{F1}	-	50 fF
C_{SS2}	-	3 pF

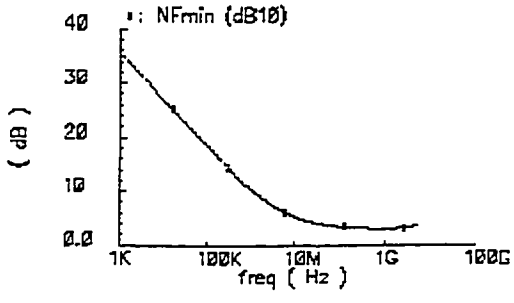
The simulation results for the chosen values of components in Table 4.1 are graphically depicted in Figure 4.3 and 4.4. Figure 4.3 shows frequency responses for S_{21} (gain), *NF* (noise figure), NF_{min} (minimum noise figure), and *kf* (stability factor). Frequency responses for Z_{11} (input impedance), Z_{22} (output impedance), S_{11} (input return loss) and S_{22} (output return loss) are shown in Figure 4.4.



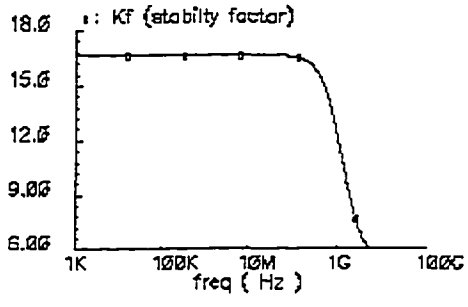
(a) Gain (S_{21})



(b) Noise figure (NF)

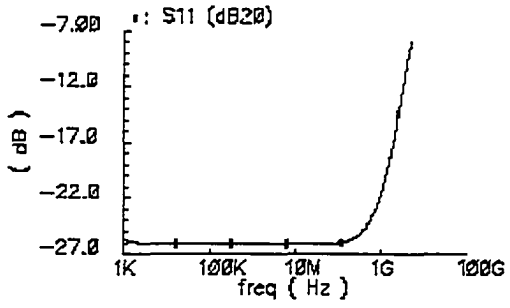


(c) Minimum noise figure (NF_{min})

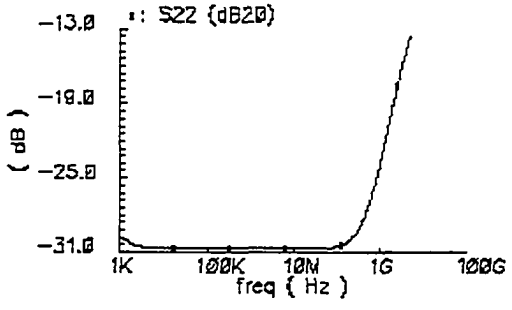


(d) Stability factor (kf)

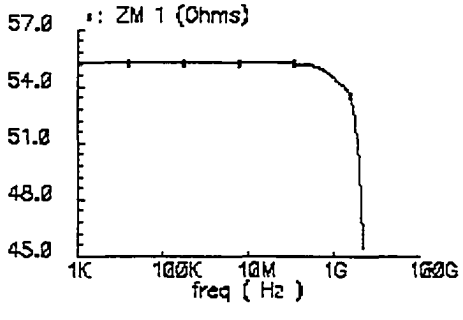
Figure 4.3 SpectreRF simulation results for Kukielka configuration



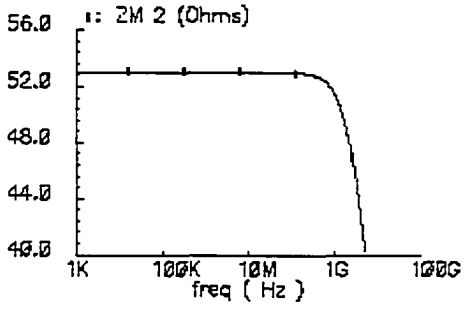
(a) Input return loss (S_{11})



(b) Output return loss (S_{22})



(c) Input impedance (Z_{11})



(d) Output impedance (Z_{22})

Figure 4.4 SpectreRF simulation results for Kukielka configuration

The simulation results measured from the graphs are summarized in Table 4.2. The measured S_{21} exhibits a very flat response with –3 dB bandwidth of 2.5 GHz and DC gain of 14.0 dB. Return loss S_{11} and S_{22} are less than –10 dB within the range of bandwidth (DC to 2.5 GHz). Input impedance, Z_{11} varies from 54 Ω to 49.5 Ω and output impedance, Z_{22} varies from 55 Ω to 49 Ω in the range of bandwidth. From the simulated results of input/output impedances and return losses (S_{11} and S_{22}), it can be said that input and output impedances of the amplifier circuit closely match to the system impedance (50 Ω).

Table 4.2: Summary of simulation results for Kukielka configuration in Figure 4.2

Performance parameters	Measured values (simulation)
Gain (S_{21}) in dB	14.0 dB
-3 dB bandwidth in GHz	2.5
Minimum noise figure (NF_{min}) in dB	3.0 dB
Input return loss (S_{11}) in dB	-26 to –14.5 (DC to 2.5 GHz)
Output return loss (S_{22}) in dB	-30 to –18 dB (DC to 2.5 GHz)
Input impedance (Z_{11}) in Ω	54 to 49.5 in 2.5 GHz bandwidth
Output impedance (Z_{22}) in Ω	55 to 49 in 2.5 GHz bandwidth
Stabilty factor (kf)	>3 (16.6 to 7.6) in 2.5 GHz bandwidth
DC current consumption (I_{DC}) in mA	12
DC Voltage in V	1.8

The calculated results for gain ($|20\log A_V|$=35 dB), input impedance (R_{in}=5 Ω) and output impedance (R_{out}=46 Ω) using equations 4.1.1 to 4.1.3 are apart from the simulated results. In calculation, the secondary effects such as channel-length-modulation (λ) and body effect (γ) of the transistors were not considered (λ=γ=0). Again, in calculation, we approximated the circuit behavior with low-frequency small signal model (Figure 2.9) that does not represent the actual device model with parasitic resistances and capacitances, which are significant at high frequencies. Therefore, simulation results are reasonably far from the calculated values.

4 .2 CMOS Amplifier of Meyer Configuration

The schematic of two-stage CMOS wideband amplifier referred to as the Meyer configuration is shown in Figure 4.5 [27], [41]. Like Kukielka configuration, this amplifier also consists of two source-degenerated common-source stages connected in cascade. Note that there are two global feedback pairs. The overall circuit can be viewed as a hybrid between series-shunt (voltage-voltage) feedback and shunt-series (current-current) feedback. The series-shunt feedback pair formed by resistors R_{F2} and R_{S1} reduces input impedance at the first stage and increases output impedance at the second stage. On the other hand, shunt-series feedback formed by resistors R_{F1} and R_{S2} increases input impedance and reduces output impedance. Thus, the combined effects of these two feedback pairs bring overall wideband matching at the output and input of the amplifier. A very small value of capacitor C_{F1} (fF) is employed to add a feedback zero that ensures maximally flat frequency response. As in Kukielka configuration of Figure 4.2, capacitor

C_{SS2} introduces peaking to compensate for the over-damped characteristics of Meyer configuration. The advantage of two global feedback pairs in Meyer configuration is larger loop gain, which ensures better stability in the frequency responses [39].

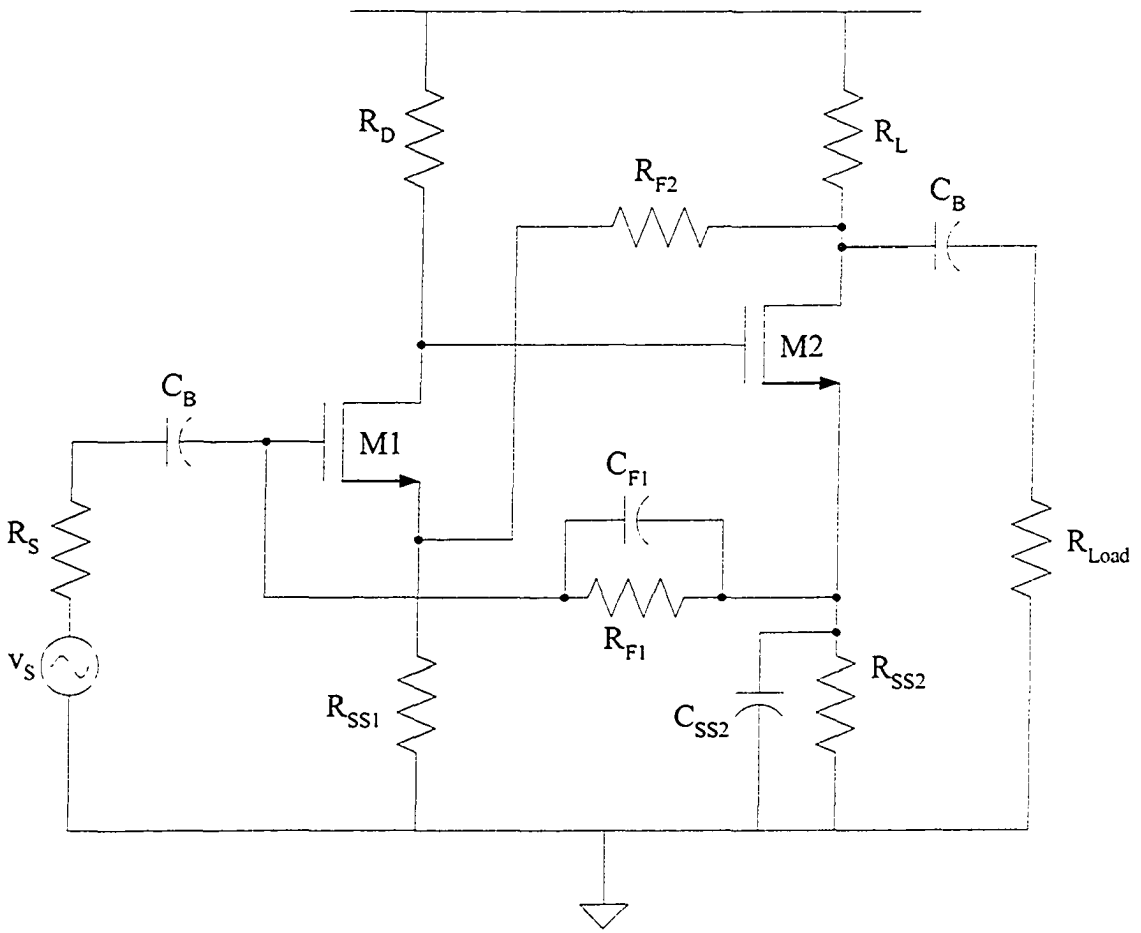


Figure 4.5 CMOS Meyer configuration.

Using low-frequency small-signals models of this circuit in Figure 4.5, the expressions for voltage gain (A_V), input impedance (R_{in}) and output impedance (R_{out}) have been derived in [27]. Thus, with similar assumptions of $g_{m1}R_{SS1}>>1$ and $g_{m2}R_{SS2}>>1$ and

considering that R_{F1}, R_{F2} are infinitely large (R_{F1}>>R_{SS1} and R_{F2}>>R_{SS2}, R_L) as mentioned earlier in section 4.1.1, the voltage gain (A_V), input impedance (R_{in}) and output impedance (R_{out}) of this amplifier are approximated as [27]

$$A_{V} = \frac{1}{2}(1+\frac{R_{F1}}{R_{SS1}}) \approx \frac{1}{2}\frac{R_{F1}}{R_{SS1}}. \tag{4.2.1}$$

$$R_{in} = \frac{R_{F1}}{1+\frac{R_D}{R_{SS1}}}. \tag{4.2.2}$$

$$R_{out} = \frac{R_{F2}}{1+\frac{R_D}{R_{SS2}}}. \tag{4.2.3}$$

Now, for typical requirements of impedance matching, R_S=R_{Load}=R_{in}=R_{out}=R, a generalized relationship is established as

$$\frac{R_{F1}}{1+\frac{R_D}{R_{SS1}}} = \frac{R_{F2}}{1+\frac{R_D}{R_{SS2}}}. \tag{4.2.4}$$

4 .2.1 Simulation: Results and Analysis

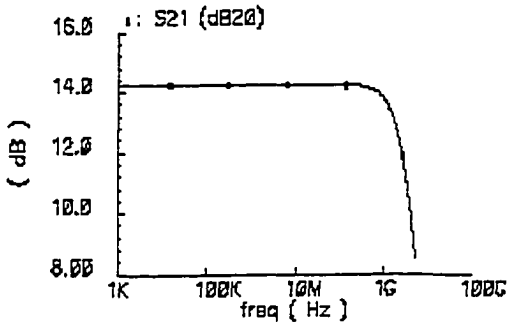
The circuit in Figure 4.5 also realized in CMOS 0.18 μm process and simulated using the SpectreRF simulator. In simulation, the performance parameters of the Meyer configuration are optimized keeping input/output matched to 50 Ω. The parametric values of all components of the circuit are summarized in Table 4.3 for an estimated optimum performance of the amplifier. The simulation results for these parameters are graphically

depicted in Figure 4.6 and 4.7. Figure 4.6 shows frequency responses for S_{21} (gain), *NF* (noise figure), NF_{min} (minimum noise figure), and *kf* (stability factor). Frequency responses for input impedance Z_{11}, output impedance Z_{22}, S_{11} (input return loss) and S_{22} (output return loss) are shown in Figure 4.7.

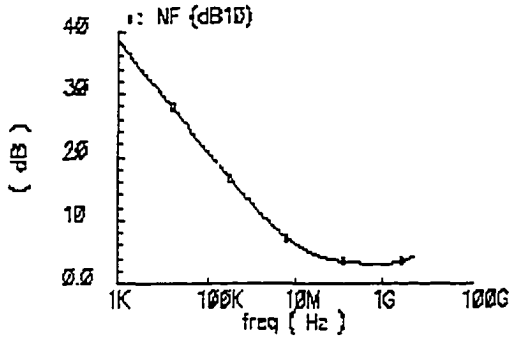
Table 4.3: Values of all the components of the circuit in Figure 4.5

Component	Component parameter	Value
M1	*W1/L*	430 μm/ 0.18 μm
M2	*W2/L*	200μm/ 0.18 μm
R_D	-	260 Ω
R_L	-	58 Ω
R_{SS1}	-	5 Ω
R_{SS2}	-	25 Ω
R_{F1}	-	300 Ω
R_{F2}	-	2 kΩ
C_{F1}	-	50 fF
C_{SS2}	-	3 pF

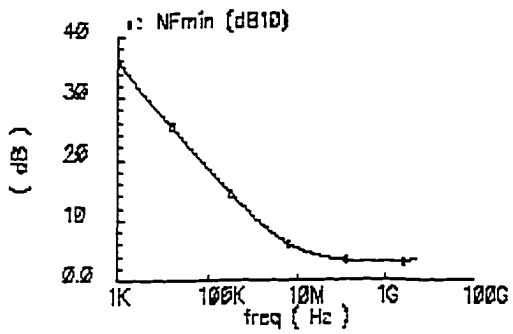
From the result of input and output impedances, it can be concluded that amplifier circuit is closely matched to the system impedance (R_S=R_{Load}=50 Ω). The calculated results for gain, input and output impedances using equations (4.2.1 to 4.2.3) are 25 dB, 56 Ω and 70 Ω respectively.



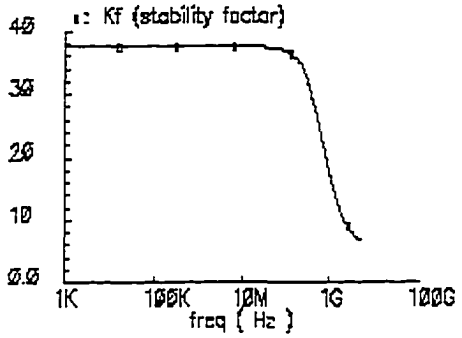
(a) Gain (S_{21})



(b) Noise figure (NF)

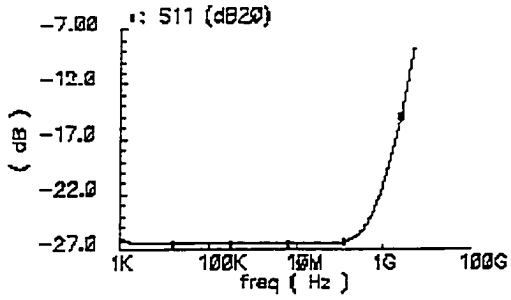


(c) Minimum noise figure (NF_{min})

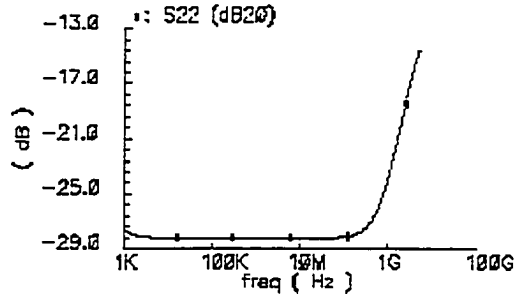


(d) Stability factor (kf)

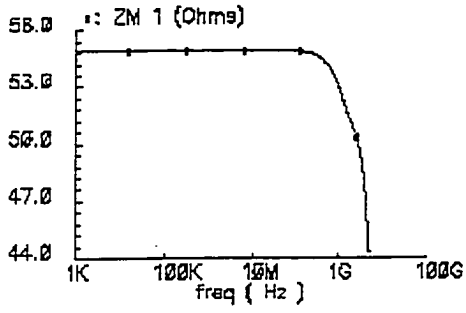
Figure 4.6 SpectreRF simulation results for Meyer configuration



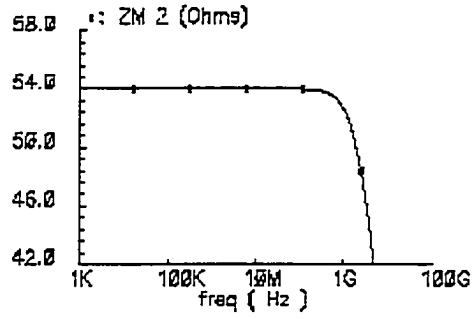
(a) Input return loss (S_{11})



(b) Output return loss (S_{22})



(c) Input impedance (Z_{11})



(d) Output impedance(Z_{22})

Figure 4.7 SpectreRF simulation results for Meyer configuration.

The simulation results measured from the graphs are summarized in Table 4.4 of. Note that the measured S_{21} exhibits a very flat response with –3 dB bandwidth of 3 GHz and DC gain of 14.2 dB. Return loss S_{11} and S_{22} are less than –10 dB within the range of bandwidth (DC to 3 GHz). Input impedance, Z_{11} varies from 55 Ω to 50 Ω and output impedance, Z_{22} varies from 54 Ω to 47 Ω in the range of bandwidth. From the simulated results of input/output impedances and return losses (S_{11} and S_{22}), it can be said that input and output impedances of the amplifier circuit closely match to the system impedance (50 Ω). However, discrepancies are also found here between the simulated results and the calculated results due to the cause as described in section 4.1.1.

Table 4.4: Summary of simulation results for Meyer Configuration in Fig. 4.5.

Performance parameters	Measured values (simulation)
Gain (S_{21}) in dB	14.2 dB
-3 dB bandwidth in GHz	3
Minimum noise figure (NF_{min}) in dB	3.0 dB
Input return loss (S_{11}) in dB	-26 to –13.3 (DC to 3 GHz)
Output return loss (S_{22}) in dB	-27 to –17 dB (DC to 3 GHz)
Input impedance (Z_{11}) in Ω	55 to 50 in 3 GHz bandwidth
Output impedance (Z_{22}) in Ω	54 to 47 in 3 GHz bandwidth
Stability factor (kf)	>3 (26 to 8) in 3 GHz bandwidth
DC current consumption (I_{DC}) in mA	13
DC Voltage in V	1.8

4.3 Proposed CMOS Two-Stage Wideband Amplifier

The CMOS wideband amplifiers for Kukielka (Fig. 4.2) and Meyer configurations (Fig. 4.5) are not complete circuits because external DC bias voltages were applied to the gate of the first-stage transistor (*M1*) in both cases. A new configuration of two-stage CMOS wideband amplifier first described in [27] is investigated here. The new configuration is a modified form of Meyer-Blauschild configuration [41].

In the proposed amplifier, one global feedback (shunt-series) is substituted by the local feedback (shunt-shunt) applied to the input stage. Then, in both local and global feedback loops, the isolating source followers are set up as buffer stages. The connection of resistive feedback loops via source followers allows one to establish a simple bias for the amplifier. These buffer stages, in addition to elimination of loading effects between the stages, provide also necessary DC level shifting and increase the loop gain. The design of the proposed amplifier becomes systematic and can easily be optimized independent of active device parameters and DC operating points.

In section 4.3.1, the modified circuit and the design objectives are outlined for the proposed two-stage CMOS wideband amplifier. Section 4.3.2 describes the design approaches for the proposed amplifier circuit. The detailed circuit analysis will be discussed in section 4.3.3. In section 4.3.4, the implementation of the proposed amplifier is described. A brief review of physical layouts of the circuit components are presented in section 4.3.5. The simulation results are discussed in section 4.3.6.

4 .3.1 Modified Circuit Description

The original Meyer configuration for two-stage CMOS wideband amplifier was shown in Figure 4.5. Now, the proposed modified version of Meyer configuration is shown in Figure 4.8 [27]. Alternatively, the proposed new configuration can also be viewed as the modification of Kukielka configuration in Figure 4.2, where local and global feedbacks have simply changed the position with each other.

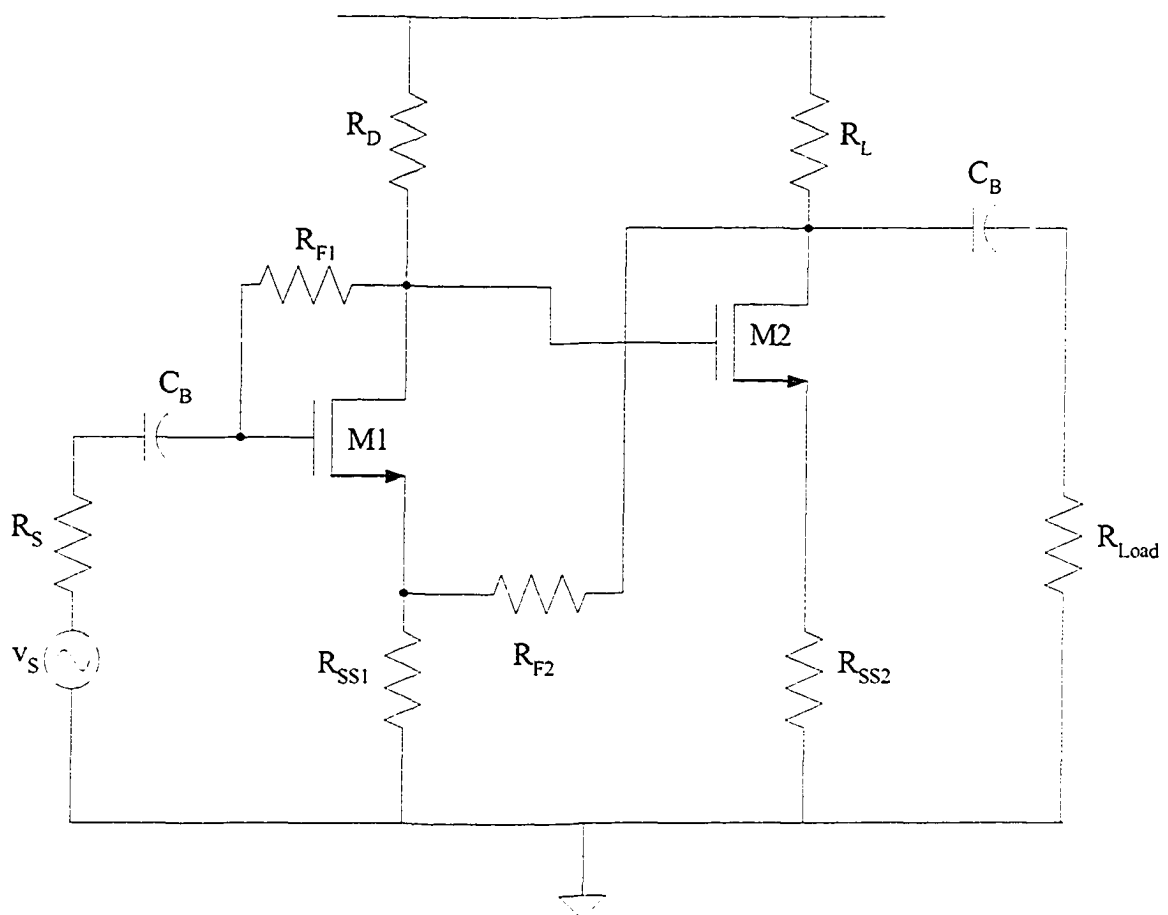


Figure 4.8 Proposed new configuration for two-stage CMOS wideband amplifier

The analysis of small signal low-frequency models with assumptions of $g_{m1}R_{SS1}>>1$ $g_{m4}R_{SS2}>>1$, R_{F1} & $R_D>>$ R_{SS1}, R_{F2} &R_L >>R_{SS2}, *and* $R_{SS1}=R_{SS2}$, give the expressions for amplifier parameters such as small-signal voltage gain, input impedance and output impedance as

$$R_{in} \approx R_{F1}\left(\frac{R_{SS1}}{R_D}+\frac{R_L}{R_{F2}}\right) \tag{4.3.1}$$

$$R_{out} \approx R_{F2}\|R_L \tag{4.3.2}$$

$$A_V \approx \frac{v_{out}}{v_s} \approx \frac{1}{2}\left(1+\frac{R_{F2}}{R_{SS1}}\right) \tag{4.3.3}$$

Here, the attempts to realize this amplifier with above approximated parameters show that it is not possible to satisfy the first two requirements ($g_{m1}R_{SS1}>>1$, $g_{m4}R_{SS2}>>1$). If the level of resistors R_{SS1} and R_{SS2} is chosen to keep amplifier noise at acceptable level, then the values of $g_{m1}R_{SS1}>>1$ and $g_{m4}R_{SS2}>>1$ reach around 1.2-1.5 only [27]. This results in a strong difference between the initial values of amplifier parameters by equations (4.3.1) to (4.3.2) and the design goals. To resolve this issue, further modifications in the circuit of Figure 4.12 are can be introduced. Thus, the modified circuit for the proposed amplifier is shown in Figure 4.9.

In the circuit of Figure 4.9, two additional source followers are introduced in each feedback loop. The source followers provide necessary DC level shifts in the feedback loops and allow the reduction of the level of R_{F1} and R_{F2}. As a result, the loop gains are increased and the loading effects in the loops are diminished. Again the source followers work as buffer stages between the gain stages and help in achieving internal DC levels.

The biasing of these two source followers is very simple, and due to weakened interaction between the loops, the bias of the whole amplifier can be obtained in a small number of iterations. The first source follower (*M3*) provides necessary DC voltages at the gate of gain stage transistors (*M1* and *M2*) and thus, the difficulties of biasing the gain stage transistors have been removed. In this way, a well-defined internal basing network is established for the whole wideband amplifier.

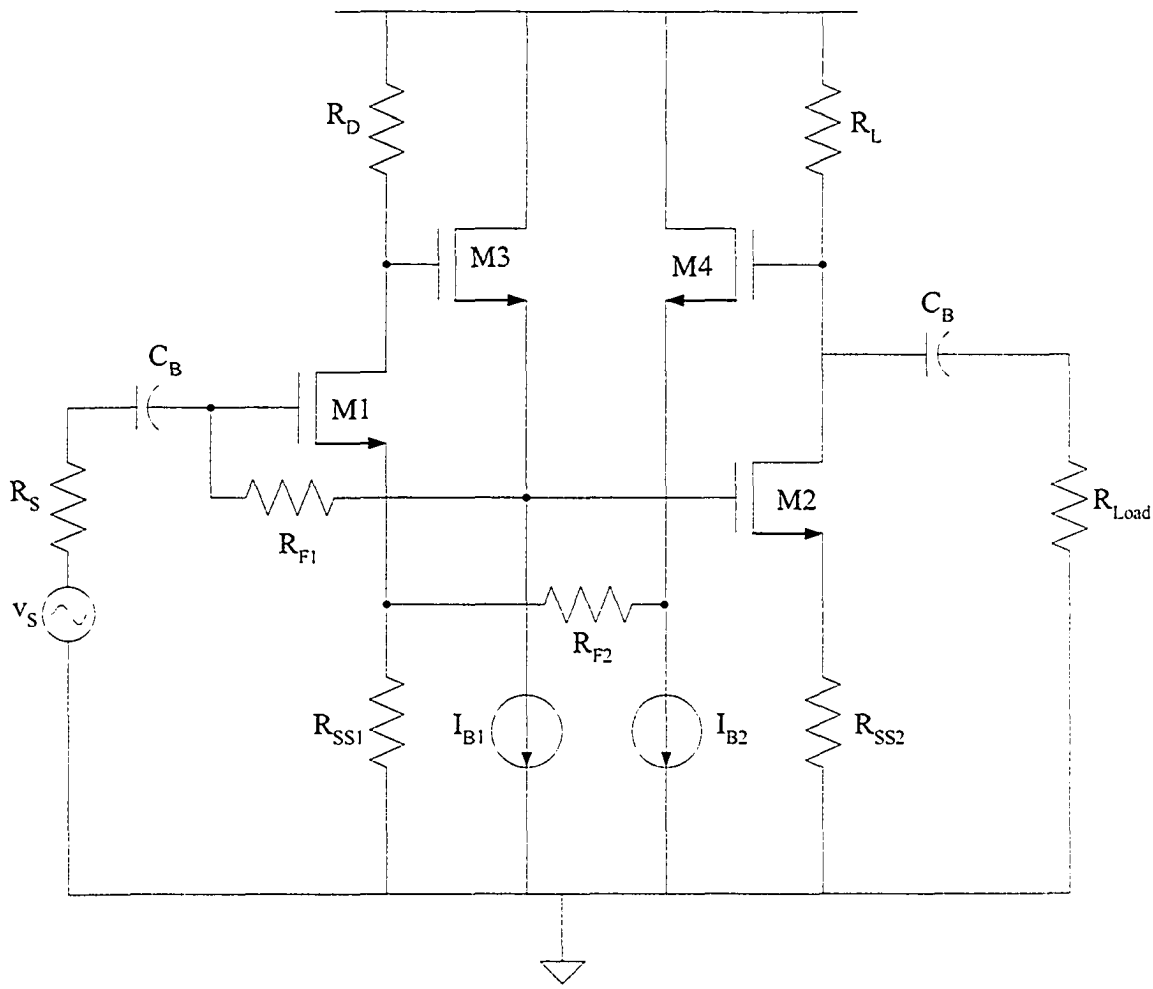


Figure 4. 9 The modified proposed wideband amplifier

4 .3.2 Design Approach

The modifications discussed in the previous section allow one to develop a new design approach for the wideband amplifier. The circuit now can be considered as a cascaded connection of two stages as shown in Figure 4.10, namely an operational amplifier, and an output nullor-based amplifier [43]. In overall circuit, these two stages have the common feedback from the output to the operational amplifier non-inverting input.

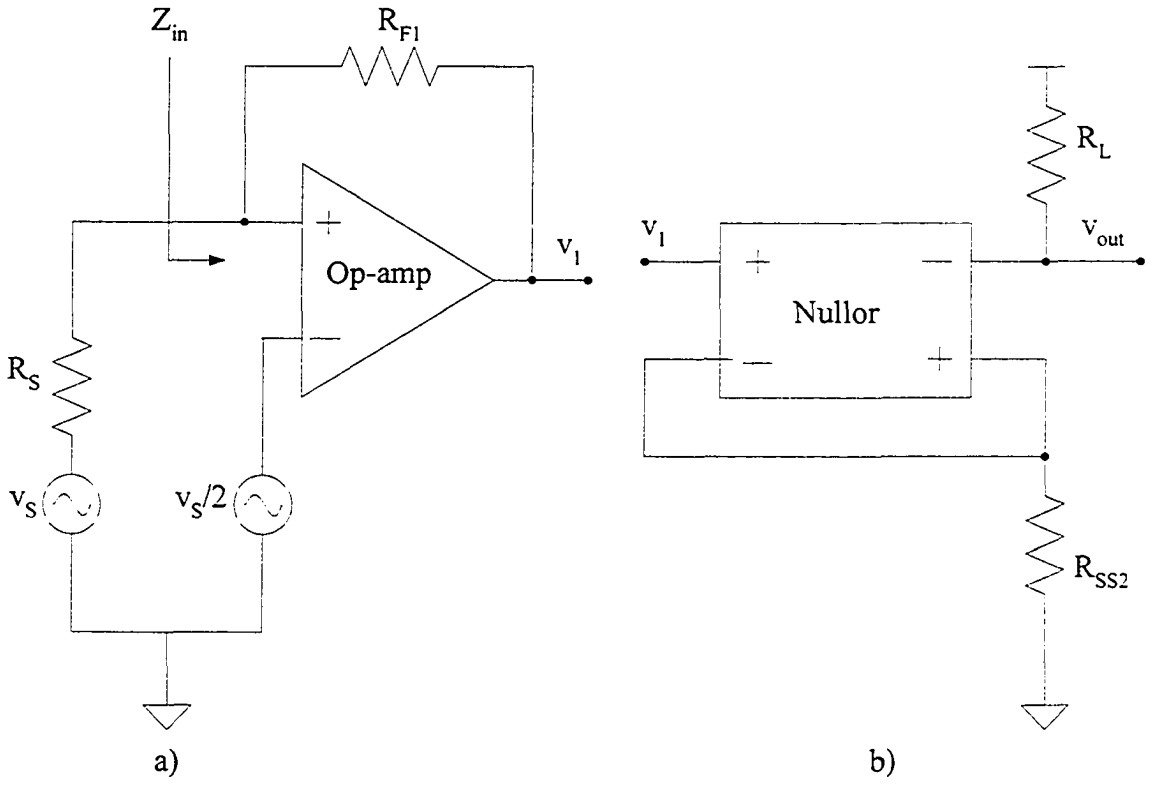


Figure 4.10 Basic design stages of the proposed amplifier

Let the signal source, v_s, with internal impedance R_s be connected to the input of the operational amplifier. If with the signal v_s, another signal of $v_s/2$ appears simultaneously at the operational amplifier non-inverting terminal (Fig.4.10.a). Then, the impedance Z_{in}

of the circuit is obliged to be equal to R_S. If the operational amplifier feedback resistance is equal to R_{F1}, the output voltage at the first stage is

$$v_1 = -(v_S / 2)\left[\frac{R_{F1}}{R_S} - 1\right]. \tag{4.3.4}$$

This amplification in the first stage operational amplifier may be insufficient. Therefore, it is increased by the gain of the second stage nullor as

$$\frac{v_{out}}{v_1} = -K = -\frac{R_L}{R_{SS2}}. \tag{4.3.5}$$

If the global feedback (β) is added as shown in Figure 4.11 to provide the required signal $v_s/2$ to the non-inverting input terminal of the operational amplifier, so that

$$v_1(-K\beta) = v_s / 2. \tag{4.3.6}$$

Then one obtains a two-stage amplifier with overall gain of

$$A_{V} = \frac{v_{out}}{v_s} = (2K)\left[\frac{R_{F1}}{R_S} - 1\right] \tag{4.3.7}$$

and the input impedance of

$$Z_{in} = R_S \frac{D}{2 - D} \tag{4.3.8}$$

where the factor D is

$$D = K\beta\,[(R_F/R_S)\text{-}1]. \tag{4.3.9}$$

Hence, if the condition $D = 1$ is satisfied, one obtains an amplifier with input impedance, $Z_{in} = R_S$ and overall voltage gain

$$A_{V} = \frac{1}{2\beta}. \tag{4.3.10}$$

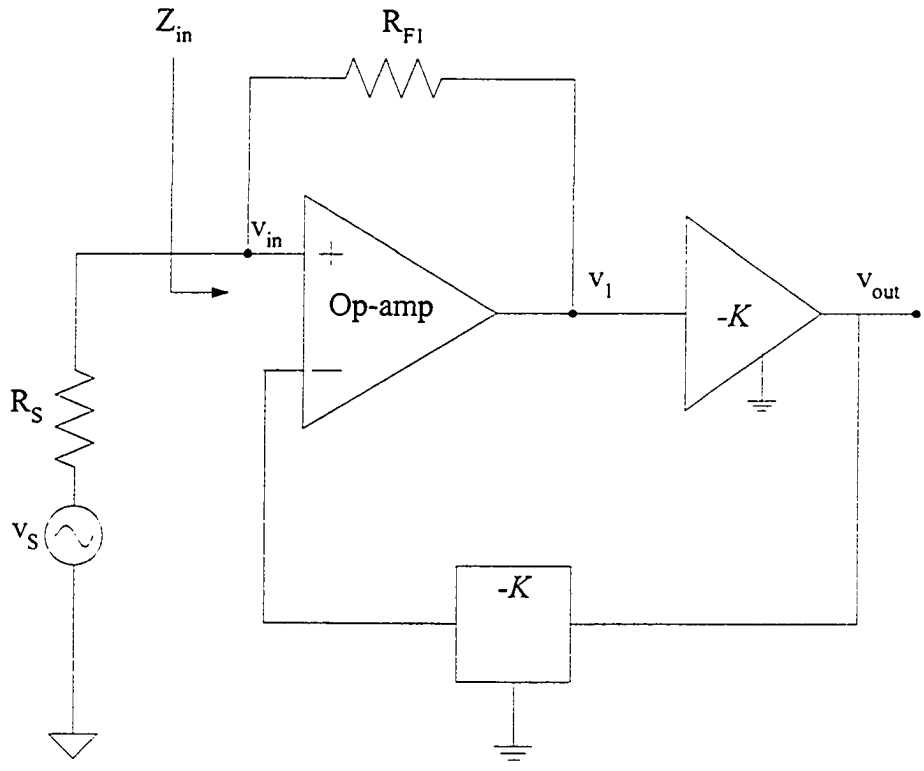


Figure 4.11 The addition of a global feedback from output to input in Fig. 4.10.

If the voltage at the inverting input of the operational amplifier in Figure 4.15 is equal to v_{in}, then one finds that

$$v_{in} = v_s \frac{R_{F1}}{R_S} \frac{\beta K}{1 + \beta K\left[1 + \frac{R_{F1}}{R_S}\right]} \tag{4.3.11}$$

and

$$v_1 = -v_s \frac{R_{F1}}{R_S} \frac{\beta K}{1+\beta K\left[1+\frac{R_{F1}}{R_S}\right]}. \tag{4.3.12}$$

From these results one can find that the voltage gain A_{v1} is

$$A_{V1} = \frac{v_{out}}{v_{in}} = \frac{1}{\beta} \tag{4.3.13}$$

and the overall voltage gain A_v is

$$A_V = \frac{v_{out}}{v_s} = \frac{v_1}{v_{in}} \frac{v_{out}}{v_s} = \frac{R_{F1}}{R_S} \frac{K}{1+\beta K\left[1+\frac{R_{F1}}{R_S}\right]}. \tag{4.3.14}$$

If the condition $D=1$ is satisfied in equation (4.3.9), then equation (4.3.14) verifies the overall gain voltage gain (A_V) in equation (4.3.10).

Using equation (4.3.11) one can find input impedance is

$$Z_{in} = R_{F1} \frac{\beta K}{1+\beta K} \tag{4.3.15}$$

and for the condition of $D=1$ in (4.3.9), one can verify that $Z_{in} = R_s$ is satisfied.

Finally, one can find the output impedance is

$$Z_{out} = \frac{R_L R_{SS2}}{R_{SS2}+\beta R_L\left[1+\frac{R_{F1}}{R_S}\right]}. \tag{4.3.16}$$

Hence, one can obtain an amplifier with desired gain, matched input and output impedance by following a sequence of steps that are usually used in the design of instrumentation systems with operational amplifiers and nullors [43].

4 .3.3 Design Realization and Circuit Analysis

The final and complete circuit of the proposed two-stage CMOS wideband amplifier is shown in Figure 4.12.

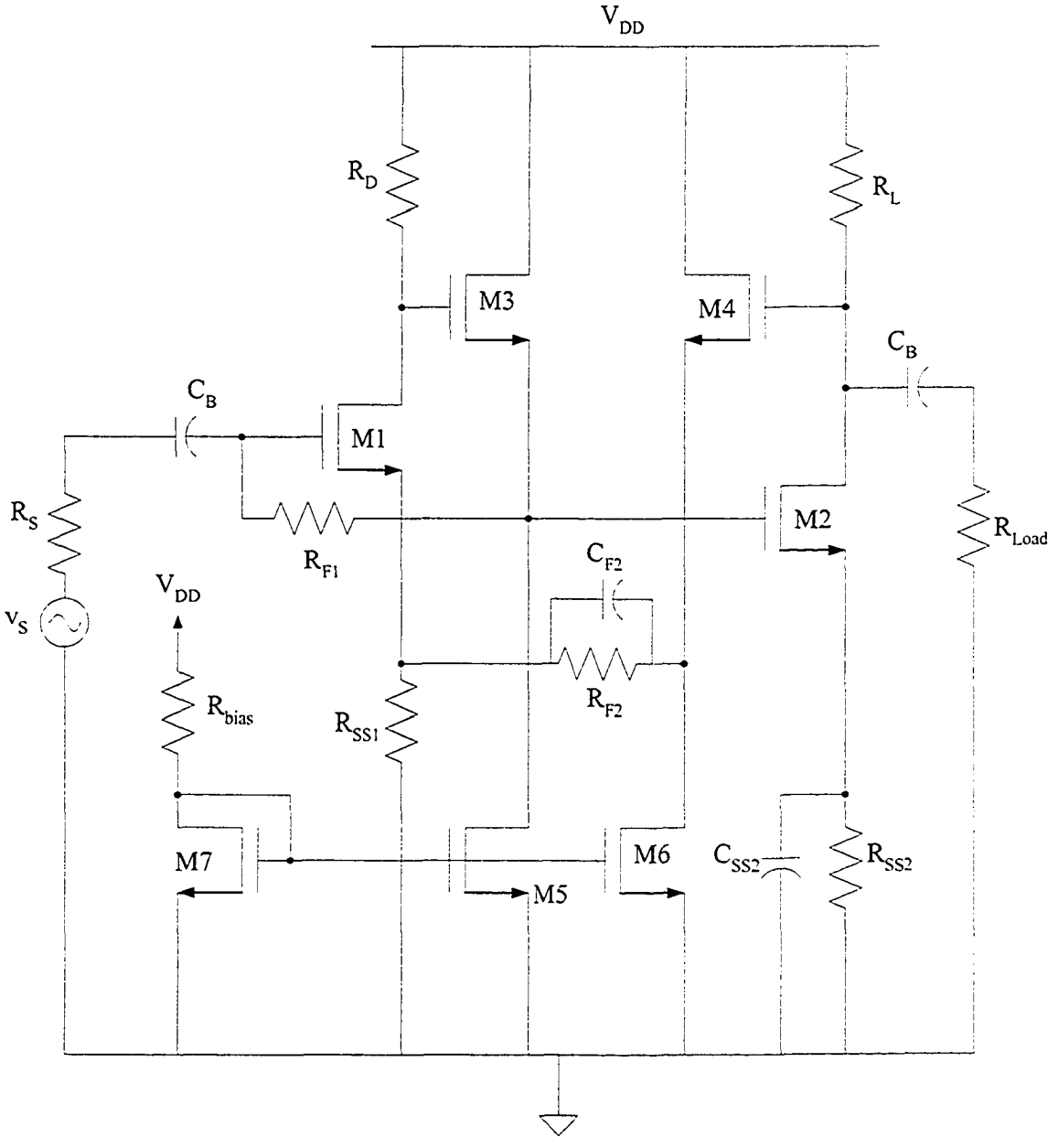


Figure 4.12 Final and complete circuit of the proposed two-stage CMOS wideband amplifier.

In this amplifier, transistors *M1*, *M2* realize approximately the mixed input operational amplifier (at the gate of *M1* is the voltage input and at the source is the current input). Resistor R_{F1} creates the first feedback loop via source follower (*M3* and *M5*). The second feedback loop is a series-shunt one, formed by resistor R_{F2} and R_{SS1} via source follower (*M4*, *M6*). Two current sources (I_{B1} and I_{B2} in Figure 4.12), have been replaced by a current mirror consisting of transistors *M5*, *M6*, and *M7*. The first inter-stage source follower consists of transistors *M3* and *M5* establishes DC gate voltages V_{G1} and V_{G2} for the gain stage transistors *M1* and *M2*. The second buffer stage source follower consisting of transistors *M3* and *M5*, shifts DC level at the source of transistor *M1* and eliminates the loading effect of the second stage nullor. These two distinct buffer stages compensate overdrive voltages V_{GS1}-V_{TH1} and V_{GS2}-V_{TH2} for transistors *M1* and *M2* in association with source resistors R_{SS1} and R_{SS2}, respectively. A small value of capacitor C_{F2} (fF) in parallel with R_{F2} is added to attain maximally flat frequency response (feedback zero). A capacitor, C_{SS2} (2-10 pF) enhances the bandwidth of the amplifier significantly with pole-zero cancellation technique [32], [39].

Assuming that the amplifier input impedance (Z_{in}) is equal to R_S, the voltage, v_{g1} at the gate of the input transistor *M1*

$$v_{g1} = \frac{v_s}{2} \tag{4.3.17}$$

and for overall voltage gain A_V in equations (4.3.3) and (4.3.10)

$$\frac{v_{out}}{v_{g1}} = 2A_V \approx 1 + \frac{R_{F2}}{R_{SS1}}. \tag{4.3.18}$$

From the output side of this amplifier one can find

$$v_{g3} \approx -v_{out}\frac{R_{SS2}}{R_L} = -\frac{R_2}{R_L}\left(1+\frac{R_{F2}}{R_{SS1}}\right)v_{g1}. \tag{4.3.19}$$

If the input impedance is matched to the signal source, then one can write

$$\frac{v_s}{2R_s} = \frac{\frac{v_s}{2} - v_{g3}}{R_{F1}}. \tag{4.3.20}$$

Then from equations (4.3.12) and (4.3.13) one can obtain the following relationship

$$\frac{R_L}{R_{SS2}}\left(\frac{R_{SS1}}{R_{SS1}+R_{F2}}\right)\left(\frac{R_{F1}}{R_S}-1\right)=1. \tag{4.3.21}$$

This relationship should be compared with equation (4.3.9) when *D=1*. From above analysis, it can be concluded that a systematic design approach can be followed in the design of the proposed wideband amplifier. Finally, for wideband amplifier realizations, it is useful to introduce an operational amplifier stage with one voltage and one current input. The conceptual realization of this amplifier is shown in Figure 4.13 [44].

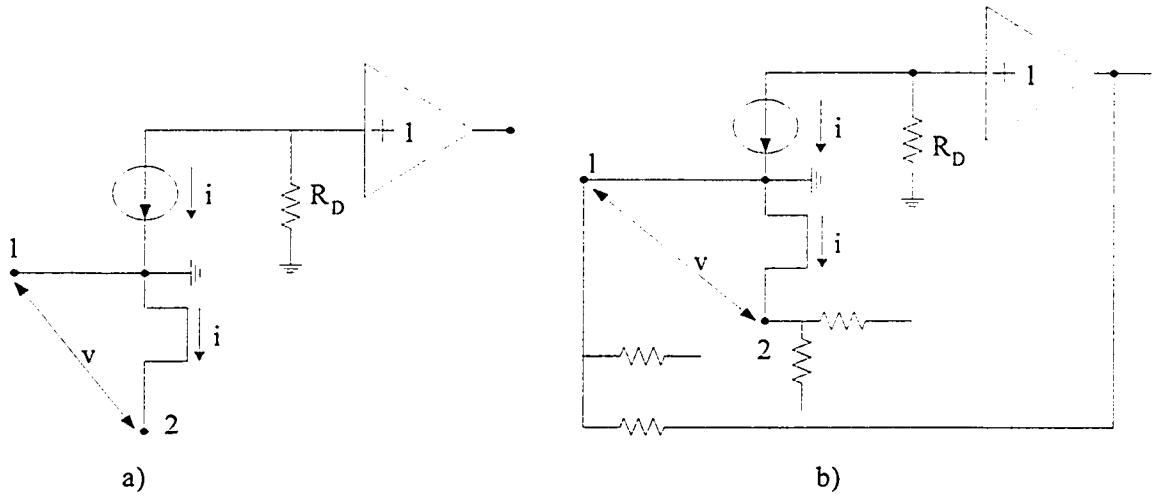


Figure: 4.13 Conceptual realization of the proposed amplifier [44].

It has high impedance at voltage input '1' and zero impedance at current input '2'. An important property of this amplifier is that it maintains the input terminals at the same AC voltage when part of a two feedback loops circuit, and at least one feedback path is preserved.

4 .3.4 Circuit Implementations

The proposed amplifier was implemented in a CMOS 0.18 μm process [45]. Note that small-signal parameters of the proposed wideband amplifier as given by equations (4.3.1) to (4.3.2) are independent of DC operating points and the active device dimensions (W/L). The circuit allows one to achieve 50 Ω input/output impedance matching and large gain with wide bandwidth. A large value of feedback resistor, R_{F2} gives very high gain as given by equation (4.3.3). Then, to achieve 50 Ω output impedance matching, R_L needs to be chosen with a value around 50 Ω ($R_{out} \approx R_L || R_{F2} \approx R_L$ for $R_{F2} >> R_L$). On the other hand, the small value of R_L reduces the gain of the second stage. Again, the large value of R_{F2} ($>>R_L$) nullifies the second term of equation (4.3.1). Then, to achieve input impedance matching to 50 Ω, a balanced selection among the values of R_{F1}, R_{SS1} and R_D are needed. If a large R_{F1} is connected between the drain and gate of the transistor in the first-stage of the amplifier, then it severely reduces the bandwidth by increasing the input stage time constant due to the Miller effect. On the other hand, a large value of R_{SS1} (or R_{SS2}) increases the noise contribution as it is connected in series with source of the transistor. Therefore, to keep noise at acceptable level, all resistors in series with drain and source of the transistors are kept as small as possible. The large value of R_D increases

the gain but reduces the bandwidth drastically. Here, a very small value of resistance is chosen for R_{SS1} (or R_{SS2}) to reduce noise contribution and a reasonable value of R_D is chosen to achieve moderate gain. Then, to fulfill the condition of $g_{m1}R_{SS1}>1$ and $g_{m2}R_{ss2}>1$, the transconductance g_{m1} and g_{m2} are made high with large transistor sizes ($=W/L$) and reduced overdrive ($=V_{GS}-V_{TH}$) voltages. For the proposed two-stage CMOS wideband amplifier, the values of all resistances, capacitances and transistor sizes are summarized in Table 4.5. These values were achieved after several iterations of computer simulations.

Table 4.5: Summary of all the components of the proposed amplifier in Fig.

Component	Component parameter	Value
M1	*W1/L*	400 μm/ 0.18 μm
M2	*W2/L*	520μm/ 0.18 μm
M5,6	*W5,6/L*	50 μm/ 0.18 μm
M3	*W3/L*	240 μm/0.18 μm
M4	*W4/L*	150 μm/ 0.18 μm
M7	*W7/L*	10 μm/0.18μm
R_{F1}	-	260 Ω
R_L	-	60 Ω
R_D	-	135 Ω
R_{bias}	-	2.7 kΩ
R_{SS1}	-	5 Ω
R_{SS2}	-	5 Ω
R_{F2}	-	550 Ω
C_{F1}	-	112 fF
C_{SS2}	-	5.2 pF

4 .3.5 Implementations of Physical Layouts

One has to implement all the passive and active devices as depicted in Table 4.5 physically in CMOS 0.18 μm process technology. In this scaled-down CMOS technology, the performance of high frequency analog and RF circuits significantly depends on the physical layouts of the devices (active and passive) [46], [47]. To achieve reduced parasitics, reduced noise and good isolation among the devices, special layout techniques should be adopted to have optimum performance so that a large degree of consistency remains between simulated and measured device performance [46], [47].

High frequency RF and analog layouts are concerned with matching accuracy and noise immunity rather than the minimizing area, which is the main focus on digital layouts [47]. In realization of analog and RF layouts, techniques such as interdigitized layouts and common centroid layouts are adopted to improve matching [47]. Layout also involves optimizing individual transistor layouts. To prevent leakages and reduce parasitics (parasitic capacitances and resistances) at high frequencies, the devices and wire lines are kept as far as possible.

In analog and RF design, large transistors are quite often used to achieve higher transconductance that leads to higher gain (in our design, maximum transistor width is 520 μm for *M2* and the maximum transistor width used in ESD protection circuit is 1800 μm). One important layout technique, which is often applied to improve the layout of large analog and RF transistors, is multi-fingered layout. This layout is used to minimize series gate resistance where ends of the gates are connected together. Moreover, guard bands surrounding the layout are used to reduce noise. However, to prevent antenna

effects, guard bands [47] are left open. The equivalent circuit model and scaling rule for implementing multi-fingered transistors can be obtained in [45]. A complete layout of a 520 μm (=*M2*) transistor, developed for the proposed wideband amplifier is shown in Figure 1 of Appendix.

In implementing RF resistors, two important factors such as current carrying capacity and noise need to be considered (typically, resistors in analog and RF design carry current in the range of 1-10 mA) in addition to the resistance values. The value of resistance of a layout shown in Figure 4.14 can be calculated from the following relationship

$$R = 2R_{contact} + N(L/W)R_{sh} \tag{4.3.21}$$

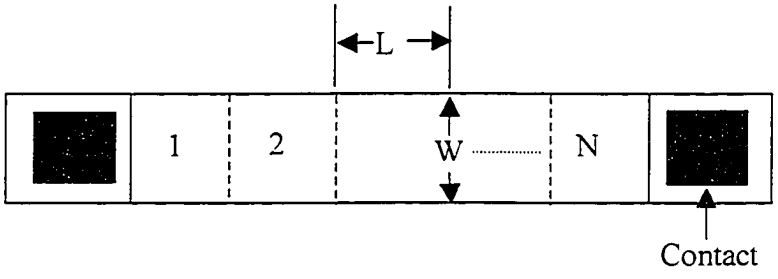


Figure 4.14 Resistor layout geometry.

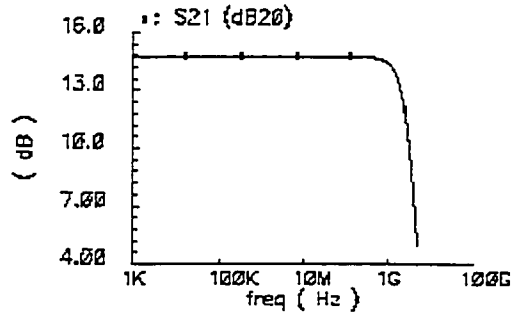
Since the resistive layer has a specific resistance value (sheet resistance, R_{sh}) its width (W) should be sufficient to carry the required current. To minimize the effects of boundary dependent etching, dummy resistors at the ends of the desired resistor are used as shown in Figure 2 of Appendix [45], [46]. The dummy resistors also work as guard-bands surrounding the resistor layout and reduce noise. For the proposed amplifier, the large value resistors (kΩ) are implemented using N+/poly layers and the low value resistors are implemented as P+/diffusion resistors [45]. A very small value resistor, 5 Ω

is implemented using metal layer [45]. The complete layout of a 5 Ω metal resistor for the proposed amplifier is shown in Figure 3 of Appendix.

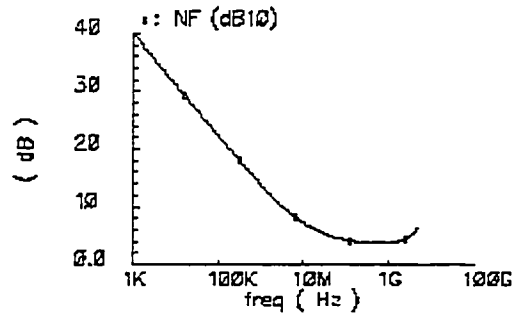
On-chip MIM (metal-insulator-metal) capacitors are implemented for the proposed amplifier. MIM capacitors are suitably used in CMOS RF integrated circuits due to their small area, high quality factor (Q) and small parasitic (capacitances and resistances) [45]. The structure, equivalent circuit model and scaling rule for MIM capacitor can be found in [45]. The input/output pads for the proposed amplifier are designed with ESD protection suitable for high frequency analog and RF design [48], [49]. The final layout for the proposed two-stage CMOS wideband amplifier in Figure 4.12 occupies a die area of 0.85 x 0.9mm^2.

4 .3.6 Simulation: Results and Analysis

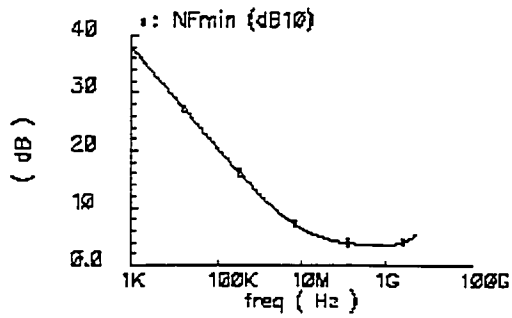
The post-layout pad-to-pad simulations were performed for gain, noise figure, input *IP3*, 1-dB compression point, return loss, input impedance and output impedance in a 50 Ω system (keeping input and output terminals of the proposed amplifier matched to 50 Ω). For the values of components in Table 4.5, the simulated results are graphically shown in Figures 4.15, 4.16 and 4.17. Figure 4.15 shows frequency responses for S_{21} (gain), NF (noise figure), NF_{min} (minimum noise figure), and kf (stability factor). Frequency responses for input impedance Z_{11}, output impedance Z_{22}, S_{11} (input return loss) and S_{22} (output return loss) are shown in Figure 4.16. Figure 4.17 shows *IIP3* and 1 dB compression point.



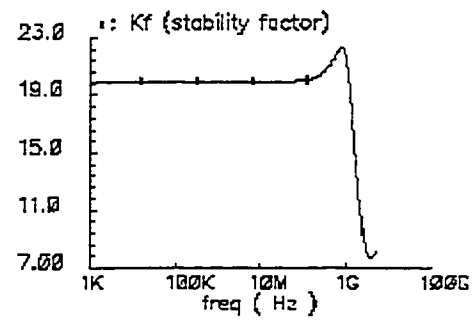
(a) Gain (S_{21})



(b) Noise figure (NF)

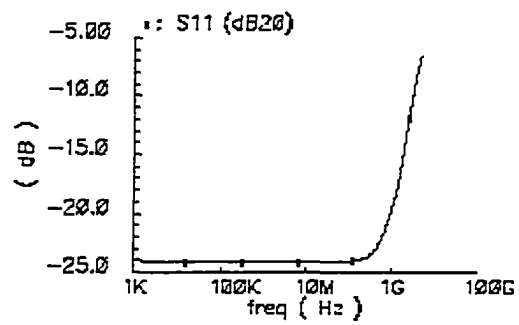


(c) Minimum noise figure (NF_{min})

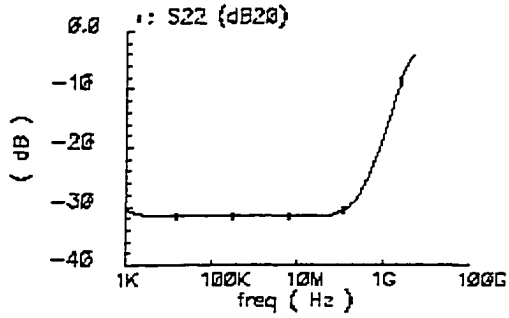


(d) Stability factor (kf)

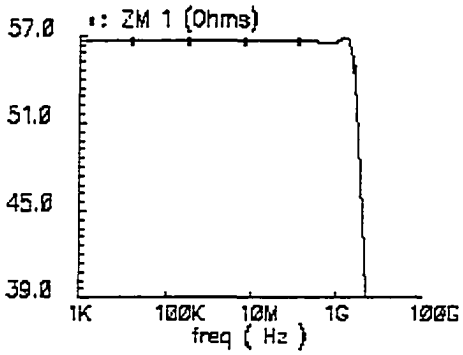
Figure 4.15 SpectreRF simulation results for the proposed wideband amplifier



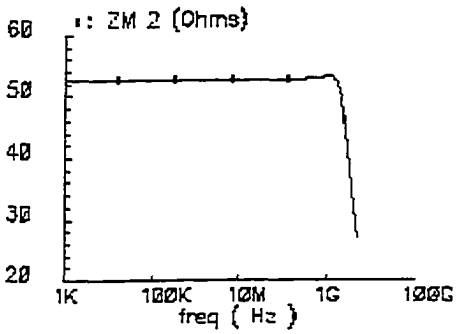
(a) Input return loss (S_{11})



(b) Output return loss (S_{22})

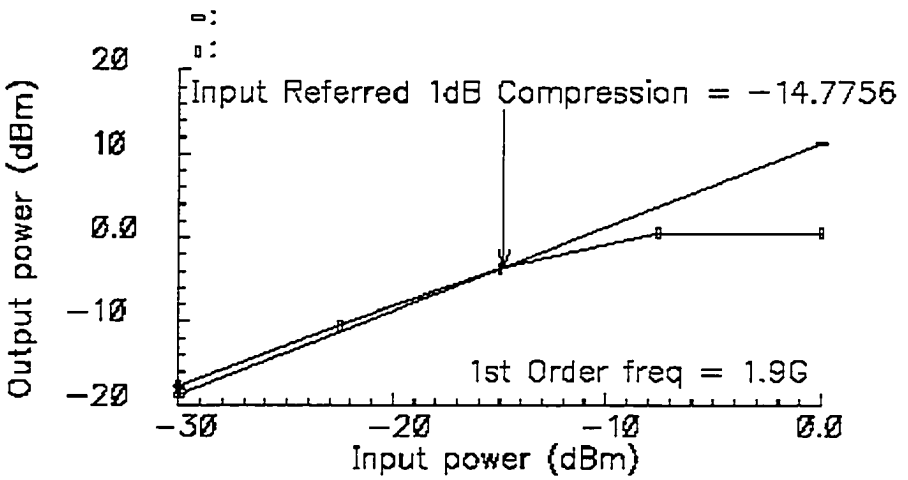


(c) Input impedance (Z_{11})

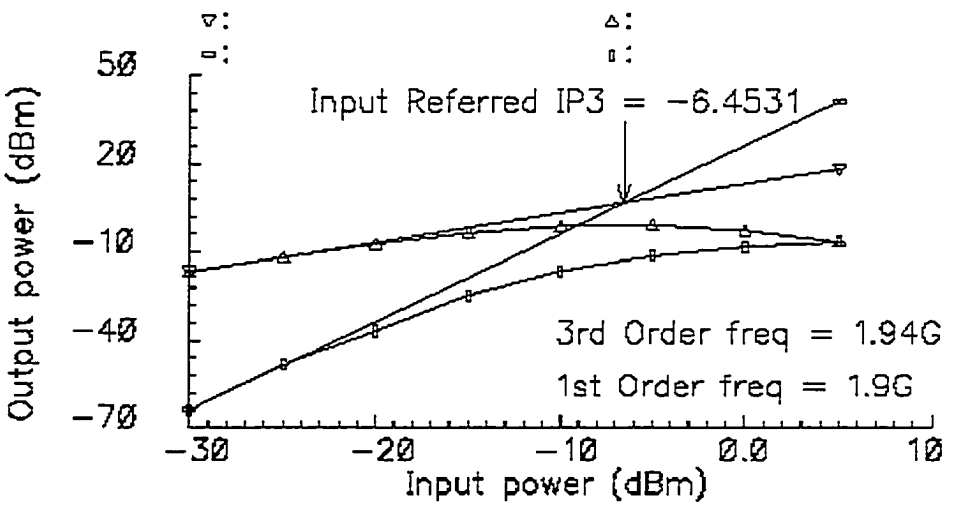


(d) Output impedance (Z_{22})

Figure 4.16 SpectreRF simulation results for the proposed wideband amplifier



(a) 1-dB compression point



(b) Input 3rd order intercept point (*IIP3*)

Figure 4.17 SpectreRF simulation results for the proposed wideband amplifier (input signal power –50 dBm).

The simulated results from the graphs for the proposed amplifier are summarized in Table 4.6.

Table 4.6: Summary of simulation results for the proposed amplifier in Fig. 4.12

Performance parameters	Measured values (simulation)
Gain (S_{21}) in dB	14.8
-3 dB bandwidth in GHz	2.6
Minimum noise figure (NF_{min}) in dB	3.4
Input return loss (S_{11}) in dB	-24 to –11 (DC to 2.6 GHz)
Output return loss (S_{22}) in dB	-30 to –10 dB (DC to 2.6 GHz)
Input impedance (Z_{11}) in Ω	55 to 51 in 2.6 GHz bandwidth
Output impedance (Z_{22}) in Ω	52 to 45 in 2.6 GHz bandwidth
Stability factor (kf)	>3 (24 to 9) in 2.6 GHz bandwidth
1-dB compression point in (dBm)	-14.7
Input 3rd order intercept point in (dBm)	-6.4
DC current consumption (I_{DC}) in mA	17.6
DC Voltage in V	1.8

S_{21} exhibits a very flat response with –3 dB bandwidth of 2.6 GHz and DC gain of almost 15.0 dB (loaded). Return losses S_{11}, and S_{22} are less than –10 dB in the range of –2.6 GHz bandwidth, that indicates the amplifier remains matched to system impedance, 50 Ω within the bandwidth. The frequency response characteristics of input and output impedance vary from 55 Ω to 51 Ω and from 53 Ω to 45 Ω respectively. Linearity measures such as *IIP3* and 1-dB compression point are –15 dBm and –4 dBm, respectively. The stability factor varies 24 to 6 (DC to 4 GHz), and thus the criteria for stability was achieved ($kf \geq 3$). The calculated results for gain, input and output impedance

are 34.8 dB, 40 Ω and 54 Ω, respectively using equations (4.3.1) to (4.3.3). Note that the calculated gain is more than 20 dB higher than the simulated gain. However, the calculated and the simulated input and output impedances are pretty close. Here, again it can be said that due to the same reasons as described in section 4.1.1, the calculated results differs from the simulated results.

To make a comparative study with the results of schematic simulation for Kukielka configuration and Meyer configuration in Table 4.2 and 4.4 respectively, the schematic simulation results for the proposed wideband amplifier in Figure 4.12 are summarized in Table 4.7.

Table 4.7: Schematic simulation results for the proposed amplifier in fig. 4.12

Performance parameters	Measured values (simulation)
Gain (S_{21}) in dB	15
-3 dB bandwidth in GHz	3.4 G
Minimum noise figure (NF_{min}) in dB	3.47
Input return loss (S_{11}) in dB	-26 to –12.5 (DC to 3.4 GHz)
Output return loss (S_{22}) in dB	-30 to –10.5 dB (DC to 3.4 GHz)
Input impedance (Z_{11}) in Ω	55 to 50 in 3.4 GHz bandwidth
Output impedance (Z_{22}) in Ω	52 to 48 in 3.4 GHz bandwidth
Stability factor (kf)	>3 (24 to 8) in 3.4 GHz bandwidth
1-dB compression point in dBm	-15.8 (at 1.9 GHz)
DC current consumption (I_{DC}) in mA	18
DC Voltage in V	1.8

4 .3.6 Comparative Study of Wideband Amplifiers

The simulation results for different types of wideband amplifiers are comparatively summarized in Table 4.8.

Table 4.8: Comparative simulation results for different wideband amplifiers.

	Kukielka Configuration	Meyer Configuration	Proposed New Configuration	Proposed New Configuration
Simulation type	Schematic simulation	Schematic simulation	Schematic simulation	Layout simulation
Gain	14.0 dB	14.2 dB	15 dB	14.8 dB
Min. noise-figure	3.3 dB	3 dB	3.4 dB	3.4 dB
-3 dB bandwidth	2.5 GHz	3 GHz	3.4 GHz	2.6 GHz
1 dB Compression point	-15.4 dBm (At 1.9 GHz)	-15.1 dBm (At 1.9 GHz)	-15.8 dBm (At 1.9 GHz)	-14.7 dBm (At 1.9 GHz)
DC current Consumption	12 mA	13.1 mA	18.2	17.6 mA
DC Voltage	1.8 V	1.8 V	1.8 V	1.8 V

Note that for the proposed new CMOS wideband amplifier, bandwidth obtained in layout simulation is by 800 MHz (3.4 GHz- 2.6 GHz) lower than that obtained in schematic simulation. The layout represents the actual physical device with its parasitic capacitances and resistances. The input and output pads increase the time constants by

contributing additional capacitances. Thus, overall bandwidth is decreased by a significant amount in post-layout pad-to-pad simulation. In this way, it is expected that the bandwidths obtained for Kukielka and Meyer configurations in schematic simulation would be decreased by significant amount in post-layout pad-to-pad simulation as well. If the bandwidth is reduced by the same amount of 800 MHz, then the bandwidths obtained for Kukielka and Meyer configurations will be far below the bandwidth of the proposed wideband amplifier in layout simulation. Here, the proposed CMOS amplifier exhibits improved performance with respect to the bandwidth. Other parameters such as gain, noise figure and linearity are close for all of the amplifiers.

4 .4 Conclusion

In this chapter, a number of wideband amplifiers have been evaluated for CMOS realization. The proposed new wideband amplifier has been analyzed theoretically as well. The simulation results further verify the theoretical analysis and establish the feasibility of the proposed two-stage CMOS wideband amplifier.

The proposed amplifier is a promising one. Introducing an independent and simple bias network allows one to use a systematic, nearly a stage-by-stage design approach for the proposed amplifier. The isolation of small signal AC and DC bias circuits makes design parameters to a first degree of approximation defined by resistors only (see 4.3.1 to 4.3.3).

Chapter 5

Wideband RF Receiver Front-End

Fully integrated system-on-chip CMOS implementations for low-power and high performance RF receivers are being explored [20], and a lot of research has been done to implement RF receiver building blocks such as LNA, mixer, and oscillator separately or integrate two or more of these blocks into subcells. A typical example of such an RFIC is the receiver front-end where a low noise amplifier (LNA) is combined with a downconversion mixer. Integrated RF front-ends are widely used because they often avoid the use of off-chip discrete components (filters) and all the RF signal processing is done on a single chip. An RF receiver front-end produces an amplified signal translated down to lower intermediate frequency (IF). Again, for multistandard receivers operating at different carrier frequencies, it is necessary to implement a front-end architecture that has enough flexibility to accommodate all these frequencies. Therefore, a wideband front-end architecture is inevitable for cost-effective single-chip solution.

In this chapter, the design issues, specifications and requirements for wideband RF front-ends in low-IF receivers [20]-[24], [50] are discussed. The front-end blocks, LNA and

mixer together determine the performance of the front-end. For instance, the gain of the LNA must be high enough to overcome fundamentally high noise of the mixer [14], [32]. On the other hand, very high gain of LNA may saturate (or, overload) the mixer and reduce the dynamic range of the front-end [14], [32]. It is very desirable to connect the LNA and mixer without any power consuming RF buffer stage [51]. Therefore, a careful co-design of the building blocks of an RF front-end is very essential to have optimum performance.

5.1 Front-End Basics

The front-end considered in this thesis is intended for low-IF receivers, and the architecture of a low-IF receiver is shown in Figure 5.1 [14], [20].

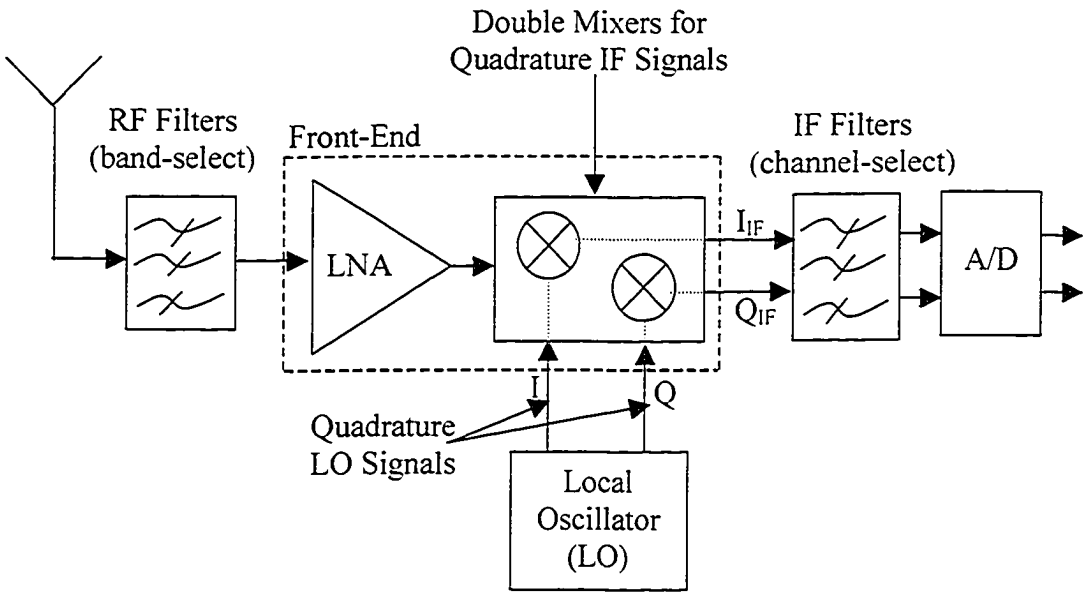


Figure 5.1 A low-IF receiver architecture (front-end is with dotted-line boundary).

A low-IF receiver has a number of advantages in comparison to the traditional superheterodyne receiver shown in Figure 5.2. In low-IF receivers, the output of the LNA is directly connected to the input of the mixer, and therefore, no image-reject (IR) filter is required. However, the image-problem in a low-IF receiver is solved by image-reject receiver architectures [14], [52]. Our interest of discussion is limited to the front-end part of the low-IF receiver.

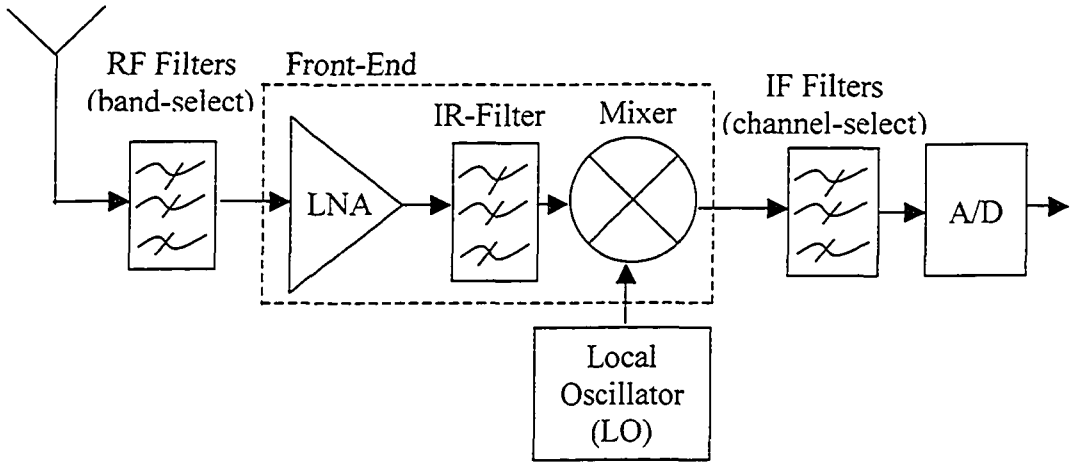


Figure 5.2 A typical superheterodyne receiver architecture

From the block diagram of the receiver front-end in Figure 5.3, it is noted that LNA and mixer are differential circuits where the inputs are applied to the LNA differentially and the outputs are taken from the mixer also differentially. Mixer translates the LNA output signal (900 MHz-3500 MHz) to Low IF signal (4 MHz–20 MHz). The front-end performance depends on the combined performance of LNA and mixer. Usually, the mixer performance defines the performance of the entire front-end (or, receiver) [34].

The performance parameters, which must be considered in the design of front-end are RF-to-IF gain, overall single-side-band (SSB) noise figure, RF-to-IF linearity, LO-to-RF and LO-to-IF isolations, wideband input matching and operating frequencies. All these issues will be discussed in the following.

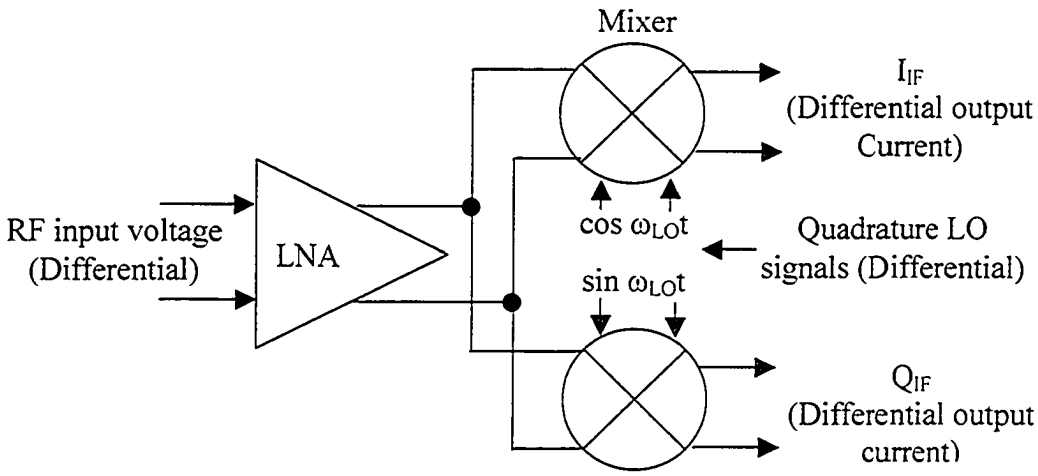


Figure 5.3 Compact notation of RF receiver front-end.

5.1.1 RF-to-IF Gain (Conversion Gain)

In the front-end, the input-signal to the LNA is RF signal and the output signal from the mixer is downconverted signal, i.e. the signal is converted to the intermediate frequency (IF). The gain from RF to IF is called the conversion gain. The RF-to-IF gain depends on many factors such as noise and nonlinearity in the cascaded stages. However, RF-to-IF gain must be sufficient enough to suppress noise contribution from all the stages being traded off with linearity so that the receiver sensitivity (dBm) increased well above the

noise-floor (dBm), the minimum detectable signal ($NF = kTB$). The overall gain of the front-end can be expressed as (in dB)

$$Gain_{Front-End}(dB) = Gain_{LNA}(dB) + Gain_{Mixer}(dB) \tag{5.1.1}$$

LNA needs to contribute most of the gain to the overall conversion gain because mixer is inherently noisy due to its switching action in frequency conversion, and the higher gain in the LNA stage will suppress the overall noise of the front-end as described by (2.1.22).

5.1.2 Noise-Figure

Noise and noise figure have been discussed in detail in section 2.1.2. For the cascaded connection of LNA and mixer in the front-end, the overall noise-figure (or noise-factor) can be expressed using equation (2.1.12) as

$$F_{Front-End} = F_{LNA} + \frac{F_{Mixer} - 1}{G_{LNA}}. \tag{5.1.2}$$

This formula shows that noise figure of the first stage, the LNA, is directly added to the noise-figure of the whole RF front-end. On the other hand, noise-figure of the 2nd stage, the mixer, is scaled down by the gain of the LNA. Therefore, to have a very low noise-figure for the whole front-end, the noise-figure of the LNA should be as low as possible, and simultaneously, gain of the LNA should be as high as possible. Two types of noise figure such as single-side-band (SSB) and double-side-band (DSB) noise figures are used for characterization of front-ends [32], [34].

5.1.3 RF-To-IF Linearity

As stated earlier in section 2.1.3, nonlinearities cause harmonic distortions, gain compression, desensitization, blocking, intermodulation, etc. [14]. In an RF front-end, signals are processed by a cascaded system of LNA and mixer. The overall linearity of the front-end can be expressed in terms of input *IP3* using equation (2.1.19) as

$$\frac{1}{A^2_{IP3,Overall}} \approx \frac{1}{A^2_{IP3,LNA}} + \frac{\alpha_{1,LNA}}{A^2_{IP3,Mixer}} \tag{5.1.3}$$

where $\alpha_{1,LNA}$ is the voltage gain of LNA for the first harmonic. This equation implies that the linearity of LNA and mixer should be maximized to achieve a highly linear front-end system. To achieve high linearity, gain (α_1) of the LNA stage should be minimized, which is contradictory to the requirement of low noise-figure as expressed by equation (5.1.1). A low gain in the LNA stage would lead to worse overall noise performance. Since the LNA and mixer are directly connected in the front-end, wideband matching at the input of the front-end with overall feedback (global) increase overall linearity [24]. However, fair trade-offs among overall gain, noise figure and linearity determine optimum performance.

5.1.4 Port-To-Port Isolation

Port-to-port isolation is a measure of how much power is coupled from one port to the other (i.e. amount of feedthrough from one port to the other) [14]. Isolations in the front-end are RF-to-IF, LO-to-IF, and LO-to-RF isolations. The first two indicate how much

RF and LO power leak through the output IF port, and the third one indicates how much LO power leaks through the input RF port. Strong presence of RF and LO signals at the IF port can saturate IF signals leading to poor linearity [14], [32], [34]. However, in low-IF receiver front-ends, both LO and RF signals (several hundred MHz) are far apart from IF signals (a few MHz) in the frequency domain. Therefore, RF and LO signals at the IF output port can easily be filtered out by high Q (quality fator) IF channel select filters. In addition, the use of a double-balanced switching mixer will further improve LO-to-IF isolation [34]. The most critical one is LO-to-RF isolation. In a low-IF receiver front-end, RF and LO signals are pretty close (separated by few MHz) and hard to remove by filtering. The low isolation between RF and LO port causes LO signals to leak through the RF port, corrupting input RF signals which results in DC off-sets due to self mixing. Moreover, LO leakage can re-radiate through the antenna, corrupting other RF signals of the same band in other systems. The LO-to-RF isolation can be maximized by designing mixer in the front-end to be as symmetrical as possible, thus hoping for two paths where any LO to RF leakage cancel each other out [34]. In addition, the LNA stage can be realized as high loop-gain feedback system to minimize this direct transfer from LO to RF port, i.e. to increase LO-to-RF isolation, [53]-[54].

5.1.5 Return-Loss and Wideband Matching

As discussed earlier in sections 2.1.1, impedance matching at the input/output terminals is absolutely necessary if the circuit is to yield optimum gain (maximum power transmitted) and return loss (minimum power reflected). Again, for wide bandwidth,

resistive feedbacks are promising, as stated earlier in section 3.3.1. In RF front-end, the input (RF port) and output (IF port) are at different frequencies. Therefore, no direct feedback between input and output is possible. Internal feedbacks around the first stage LNA can be employed. In this way, one feedback can be employed from the input of the mixer to the input of the LNA and the second one can be employed as local feedback around any part of the LNA for stability. For better inter-stage isolation, feedbacks are applied via buffer stages.

5.2 Topology Selection for Wideband LNA

Since LNA is the first block in the receiver front-end, its noise figure is directly adds to the noise figure of the entire front-end as described by equation (5.1.2). Therefore, the main function of the LNA would be to provide enough gain to overcome the noise of the subsequent stages contributing minimum noise figure by itself. In addition to high gain and very low noise figure, LNA should maintain high linearity to accommodate large signals without distortion and overloading the following stages. Finally, for maximum power transfer and minimum power reflections, its input impedance must be matched to the source impedance [32]. Again, for multistandard and wideband applications, the input matching would be such that its bandwidth extends to a few GHz.

For higher gain, the LNA can be implemented into two stages: the input stage and the output stage. The common-source (CS) configuration is the best suited for implementing stages of the amplifier because it offers the largest gain compared to the common-gate (CG) configuration [29], [31]. A common-drain configuration or source-follower makes

an excellent voltage buffer between two CS stages [29], [31] as discussed earlier in section 3.3.2. For better noise performance, single transistor CS topology is used and for improvement in linearity, resistive source-degeneration is used in the CS configuration that also helps in achieving wideband matching [29].

5.2.1 Input and Output Stages for Wideband LNA

The single-ended input stage for wideband LNA is chosen as a shunt-series amplifier as shown in Figure 5.4, which provides broadband matched real input. Hence, the circuit is a common-source amplifier with a resistive feedback via common-drain (source-follower).

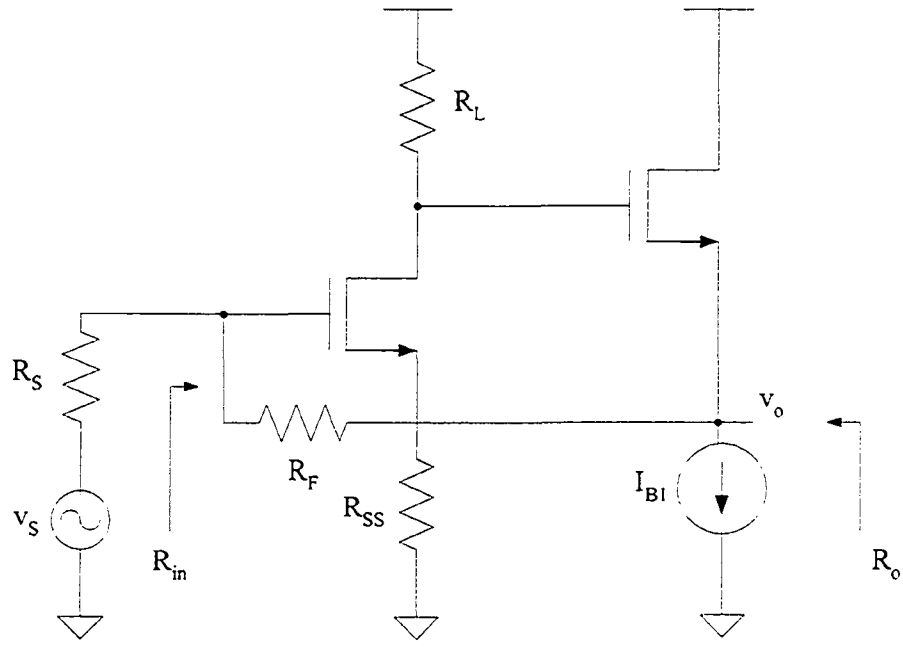


Figure 5.4 Modified input-stage of the LNA.

The source-follower feedback stage assists to optimize the noise performance [11] and acts as a buffer for the second stage amplifier. However, the wideband input stage exhibits a major trade-off between input impedance and noise figure [55]. For differential RF input signals, two single-ended input stages are connected in symmetric manner as shown in Figure 5.5.

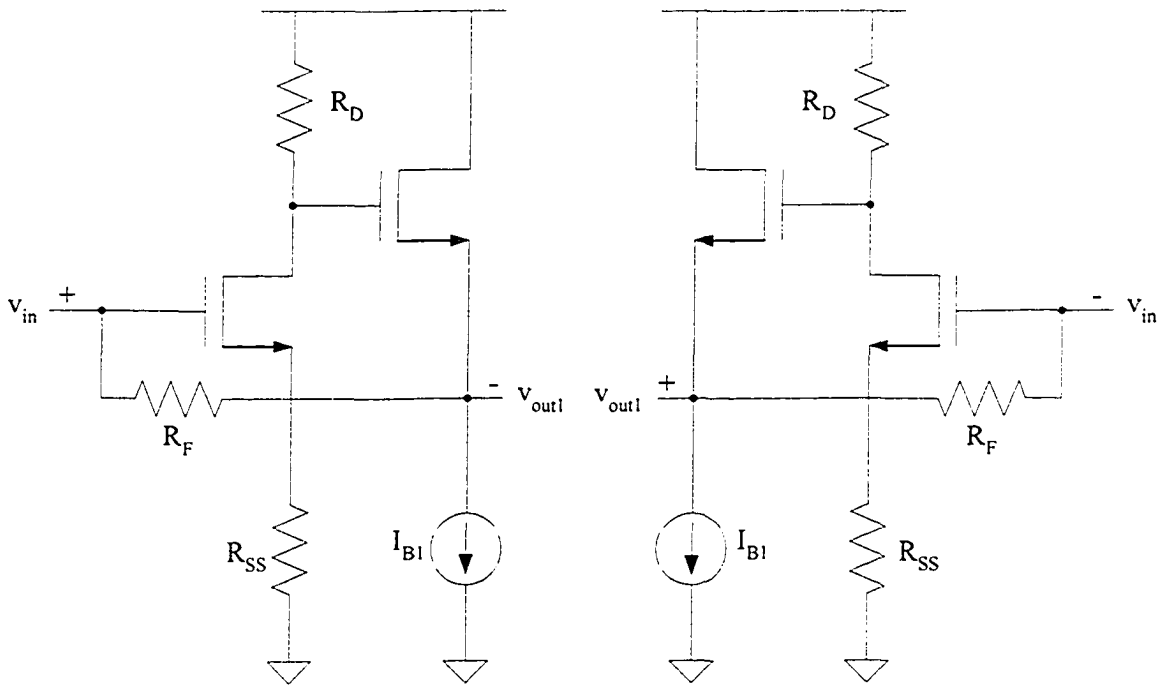


Figure 5.5 The overall differential input-stage.

The output stage for wideband LNA is chosen as differential amplifier as shown in Figure 5.6. The outputs $v_{outI}+$ and $v_{outI}-$ from two symmetric input stages are fed to the differential inputs $v_{inI}+$ and $v_{inI}-$ of the second stage, respectively. Note that due to the common-source configuration of the input stages, the polarity of the outputs ($v_{outI}+$ and

v_{out}-) is opposite to their respective inputs (v_{in}+ and v_{in}-). The differential stage has the advantages of improved linearity, the ability to reject common mode disturbances and increased dynamic range with increased power consumption and noise figure [32]. However, the main purpose of this differential stage is to generate differential signals for the next stage mixer.

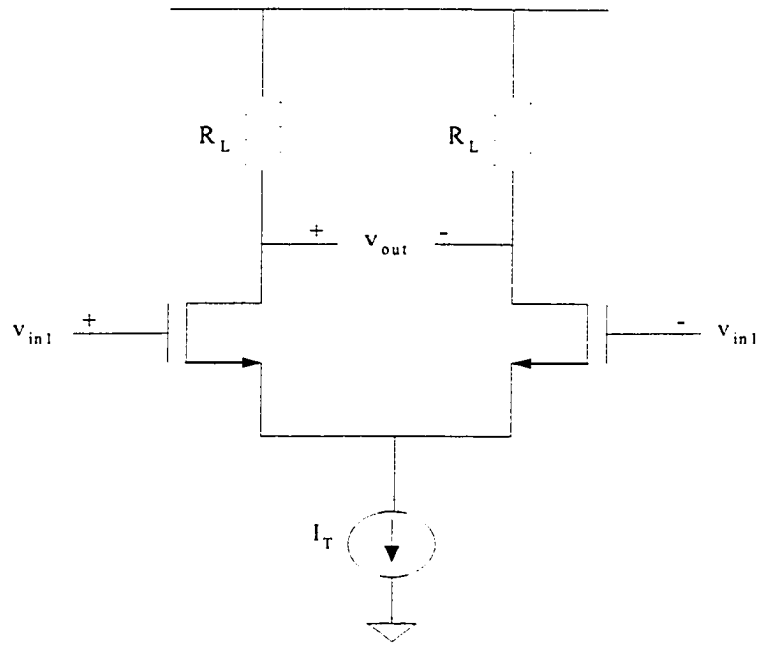


Figure 5.6 The differential amplifier in the output-stage of the LNA.

5.2.2 The Complete Wideband LNA

The complete wideband LNA circuit, combining input and output stages is shown in Figure 5.7. Note that the circuit in Figure 5.7 has been modified with additional feedback networks. A global feedback from each side of the differential output has been applied to the corresponding input via source follower. Thus, dual feedback loops are established in

each of the half circuit of the overall LNA. These dual feedback loops are used to achieve wideband matching at the input and they also help in increasing overall linearity. Indeed, this wideband LNA is a symmetric combination of two wideband amplifiers shown in Figure 4.9 of section 4.3.1. As a symmetric circuit, this LNA can be easily analyzed using half-circuit concept [29] with a resemblance to the analysis of wideband amplifier shown in Figure 4.9. A general discussion on performance parameters of the amplifier such as gain, bandwidth, linearity, noise, matching and return loss has already been done in Chapters 2, 3, and 4, which are also applicable to wideband LNA.

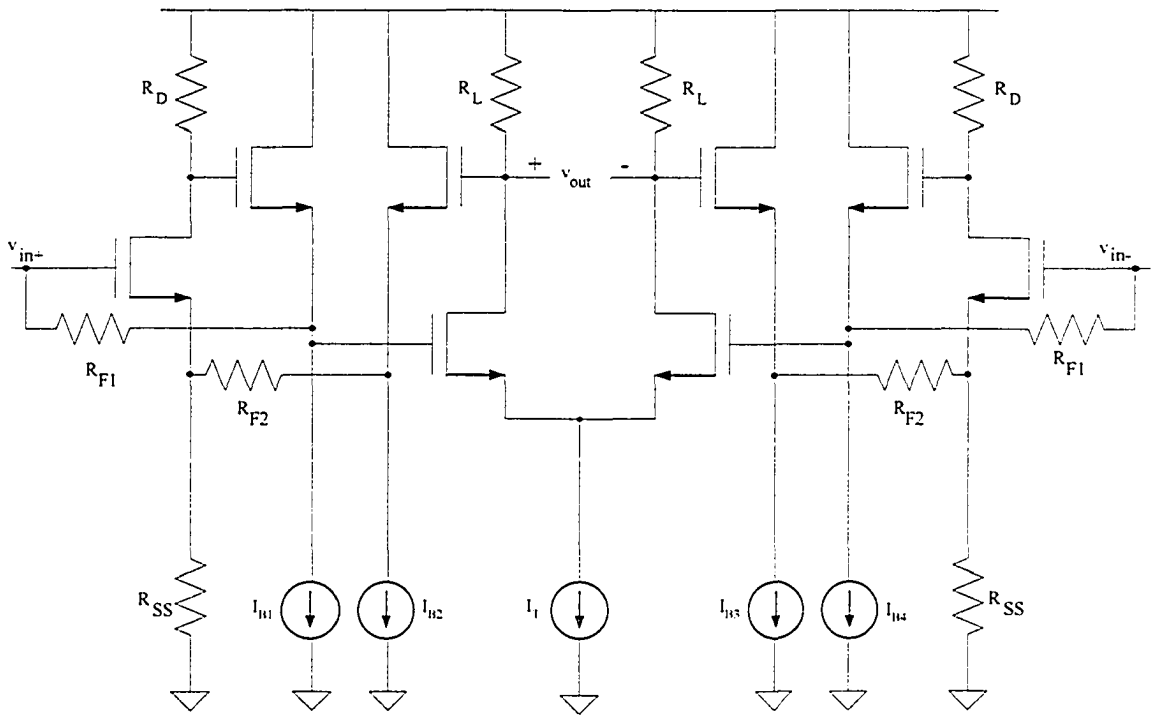


Figure 5.7 The complete wideband LNA

5.3 Topology Selection for Mixer

A mixer performs the crucial task of frequency conversion. In the receiver front-end, a mixer is called as downconversion one, and converts RF signal to IF signals (high IF, low IF, or Zero IF). The performance parameters of the front-end are defined by the performance parameters of the mixer: conversion gain, noise-figure, 1-dB compression point, third-order intercept point (*IP3*), port-to-port isolation and return loss as earlier discussed in section 5.1. The fundamental choice in MOSFET mixer design is whether to use an active or passive mixer. The passive mixers have better linearity and excellent intermodulation performance at the cost of local oscillator power, but the disadvantages of these mixers are conversion loss, higher noise figure and large LO power requirement [32], [56]-[57]. In contrast to passive mixers, the active mixers have better conversion gain, lower noise figure and higher linearity [32], [56]-[57]. Again, to suppress the noise in the following stages of the RF front-end after the mixer, it is desirable to achieve gain in the mixer. Therefore, active mixer is most widely used. The performance parameters of the active mixers depend on the mixer types. Active mixers can be loosely classified as single ended mixers, single balanced mixers, double balanced mixers and folded cascode mixers [32], [34], [56], [58]. Due to various limitations and demerits, single ended and single balanced mixers receive little attention in CMOS RF design, and are also rarely used in RF communication [32], [34], [57]-[59].

Double-balanced switching mixers (Figure 5.8) also called Gilbert cells are very commonly used ones [32], [58], [60].

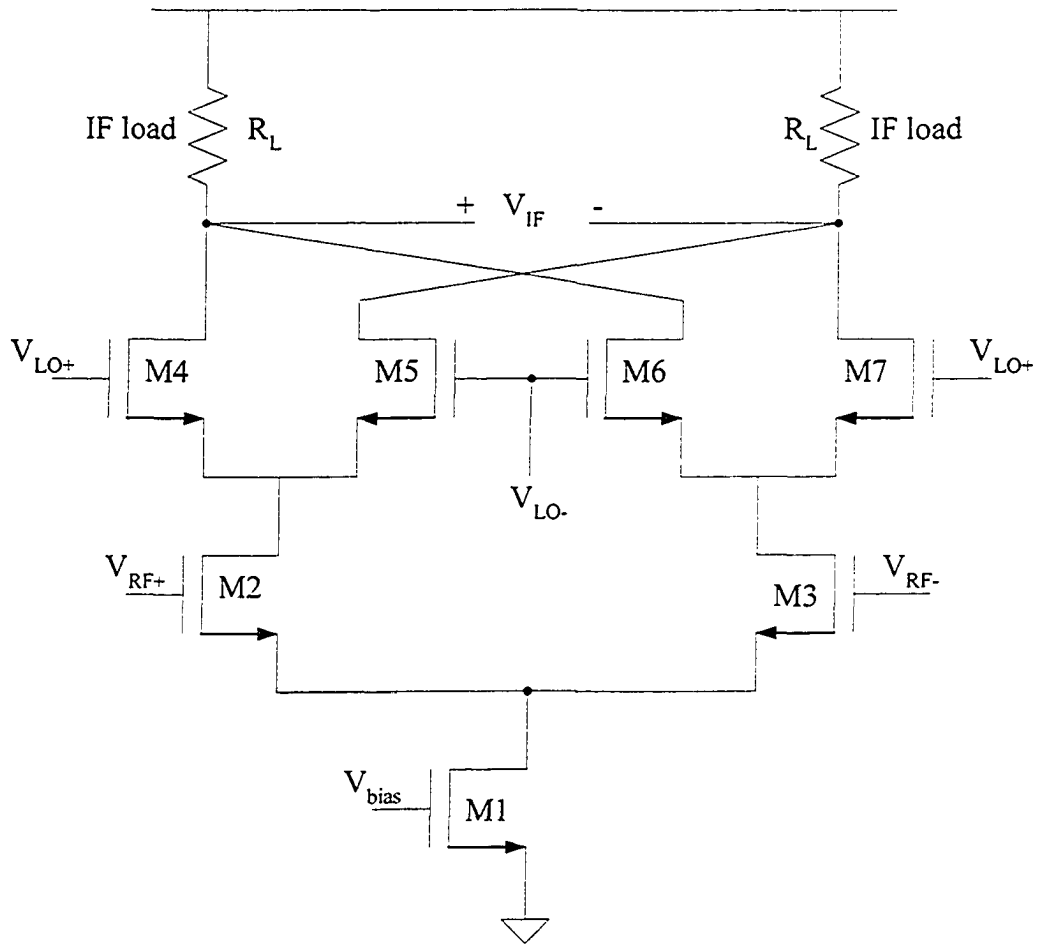


Figure 5.8 A double balanced Gilbert-cell mixer

The advantages of the Gilbert-cell double balanced mixers are the inherent high degree of isolation between all the ports (RF, LO and IF), the suppression of all even order products of the LO and/ or the RF signals, and good common mode rejection ratio (CMRR) due to fully differential nature with respect to the RF inputs and the IF outputs [32], [34]. However, in this architecture, there are three MOSFETS and one IF resistive load stacked on top of each other. This tall stack of elements now requires a higher supply voltage to keep all transistors in saturation with adequate overdrive voltages (V_{GS}-V_{TH}) so that it can provide conversion gain. With low supply voltage like 1.8 V in CMOS

0.18 μm process, it is hard to realize such a double balanced Gilbert-cell mixer with adequate conversion gain. Moreover, the overall voltage swing at the IF output port becomes low, limiting mixer (or, front-end) dynamic range [58]-[61]. The low-voltage versions of Gilbert-cell mixer have been described in [60] with the limitations of narrow-band applications because of the use of inductor-capacitor tanks in the signal path. Therefore, for low voltage operation, the trend is now turning to folded switching mixers (folded cascode architecture), which have less stacked on components [59], [61].

5.3.1 Folded Switching Mixer

Folded switching mixers have a higher voltage gain at low supply voltages compared to the double balanced Gilbert-cell mixers. The objective in designing folded switching mixer is to reduce the number of stacked on transistors between the power rails (supply and ground). To achieve this, a low-voltage design technique [60] can be applied where the transconductance and the switching stages are decoupled into cascaded stages instead of cascode configuration (switching stage sits on the transconductor stage) in the Gilbert-cell mixer. Moreover, the tail current source (M_1) is completely omitted. Thus, a folded switching mixer is built as shown in Figure 5.9 [61]. It provides high gain, low noise figure and moderate linearity at low supply voltages. The current distribution between transconductance and switching stage is shown in Figure 5.9. The transistors in the switching and transconductance stages are biased with DC gate voltages such that all the transistors remain in saturation.

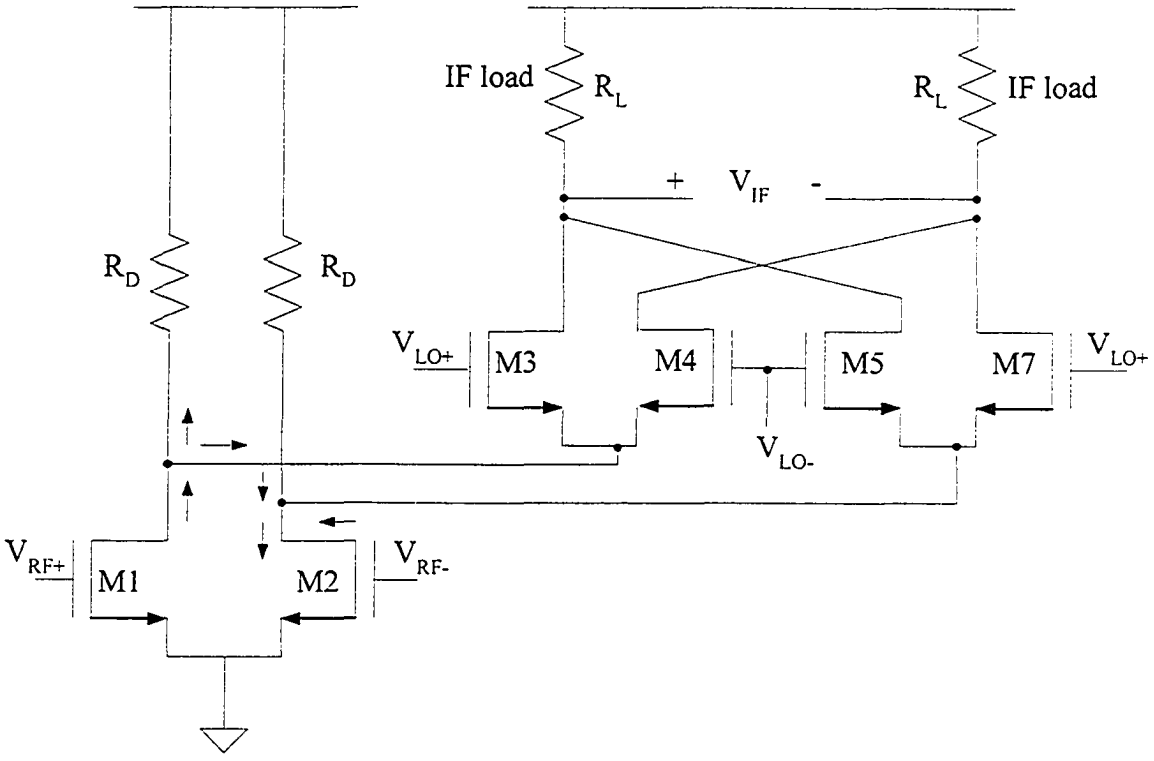


Figure 5.9 Folded switching mixer [66]

This folded switching mixer (Figure 5.9) can provide reasonable gain because low DC currents flow through the switching transistors, which results in low voltage drop across resistors R_L. The voltage conversion gain in dB of this mixer can be approximated as [61]

$$G_{C|Voltage}|dB = 20\log\left(\frac{2}{\pi}\frac{g_{m1,2}R_L}{1+\frac{1}{R_D(g_{ms}+g_{mbs})}}\right) \tag{5.3.1}$$

where $g_{m1,2}$ is the transconductance of the transistor *M1* or *M2*, g_{ms} is the transconductance of the switching transistors and g_{mbs} is the body transconductance of

the switching transistors. Note that if R_D (g_{ms} +g_{mbs}) >>1, then voltage conversion gain is reduced to

$$G_{C\|Voltage}|dB = 20\log\left(\frac{2}{\pi} g_{m1,2} R_L\right) \tag{5.3.2}$$

which is similar to the conversion gain of the double balanced Gilbert cell mixer in Figure 5.8 [34].

This mixer has some restrictions. Due to omitting tail current-source (*M1*), the input stage is no longer a differential pair, but rather a source-coupled pair. However, the folded mixer circuit is still balanced and will operate in differential manner if it driven by differential RF input signals [34]. Although, inputs and outputs are differential in nature, the circuit in Figure 5.9 has no common mode rejection ratio [34]. Therefore, either in the IF filter-stage or in the LNA stage, common mode rejection needs to be provided. In spite of these drawbacks, the folded switching mixer is the most attractive topology for its higher conversion gain over the Gilbert-cell mixer at low supply voltage [59], [61]. Therefore, in this thesis, folded switching mixer topology is chosen for the proposed wideband RF receiver front-end.

5.4 Conclusion

In this chapter, the design issues and requirements for the wideband receiver front-end have been discussed in detail. The performance of the front-end entirely depends on the combined performance of its building blocks, LNA and mixer. The good design strategies are needed to make the performance parameters of the building blocks

orthogonal to each other. Hence, at first, the performance parameters of the LNA can be optimized and then, a mixer is designed independently with optimized performance.

Topology selection for the building blocks of the front-end is an important issue. In this chapter, a detailed discussion explained what are the correct topologies of wideband LNA and mixer for the receiver front-end. In receiver front-end, a building block in the preceding stage (LNA) influences the performance of the later stage (mixer). Therefore, a number of trade-offs have to be made in obtaining overall better front-end performance. In the next chapter, it will be discussed how the proposed receiver front-end for this thesis is built using the wideband LNA (Fig. 5.7) and of folded switching mixer (Fig. 5.9).

Chapter 6

Investigation of CMOS Wideband RF Front-End

As mentioned earlier in Chapter 5, the combined performance of the front-end depends on the individual performance of LNA and mixer. Since LNA is the first block in the receive path, its noise is directly adds to the overall noise figure of the RF front-end and its gain reduces the noise contribution from the subsequent mixer stage. Therefore, LNA is expected to be designed with very low noise figure and high gain. On the other hand, a mixer is the noisiest one due to the switching action of MOSFET transistors. Here, the design objective with mixer is to keep its noise figure as low as possible and add a moderate gain. At the device level, attention needs to be employed so that noise in transistors and resistors is reduced significantly using special physical layout techniques [46], [47]. At the circuit level, DC operating points, device sizes and matching criteria are chosen such that gain and linearity are improved with acceptable noise levels.

In this Chapter, a wideband receiver front-end is designed in CMOS 0.18 μm process for low-voltage low-IF multistandard wireless receivers. This is a new configuration for CMOS RF front-end where dual feedback loops are employed for input wideband matching. A new linearization technique makes the front-end circuit suitable for operating at low supply voltages. Conceptually, LNA and mixer are realized separately

and then they are combined with modifications to build the complete front-end circuit. The performances of RF front-end are investigated both with theoretical analysis and computer simulations.

6 .1 Circuit Design for the Receiver Front-End

In this thesis, a new CMOS wideband front-end is designed. It includes a switching mixer stage cascaded with a two-stage LNA. The circuit is modified in such a way that only three components (active and passive) are stacked between the power rails, which makes the circuit suitable for operating with low DC supply voltage (1.8 V).

The first step towards an implementation is to find a front-end topology suitable for multistandard low-IF receivers. The front-end with two quadrature outputs (I, Q) in Figure 5.3 is the proposed architecture for the front-end in this thesis. However, the implementation of the front-end in this thesis work is limited to one IF output as shown in Figure 6.1 where a differential LNA is cascaded with a differential mixer, and can be called a double-balanced low-noise-converter (LNC).

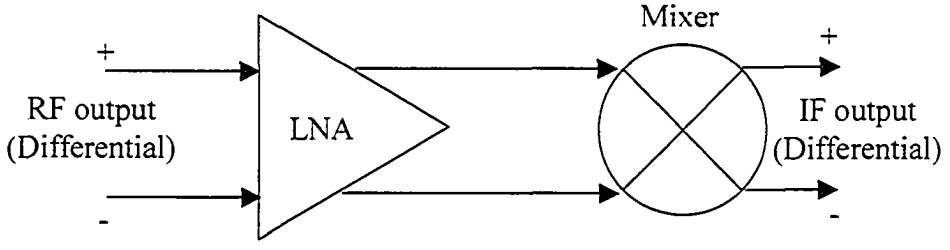


Figure 6.1 Implementation of the proposed wideband front-end.

Based on design strategies for LNA and mixer in (Sections 5.2 and 5.3), a preliminary CMOS circuit for the proposed front-end is shown in Figure 6.2. Here, the differential output of the LNA in Figure 5.7 has been connected to source-coupled pair of the switching transistors of the mixer in Figure 5.9.

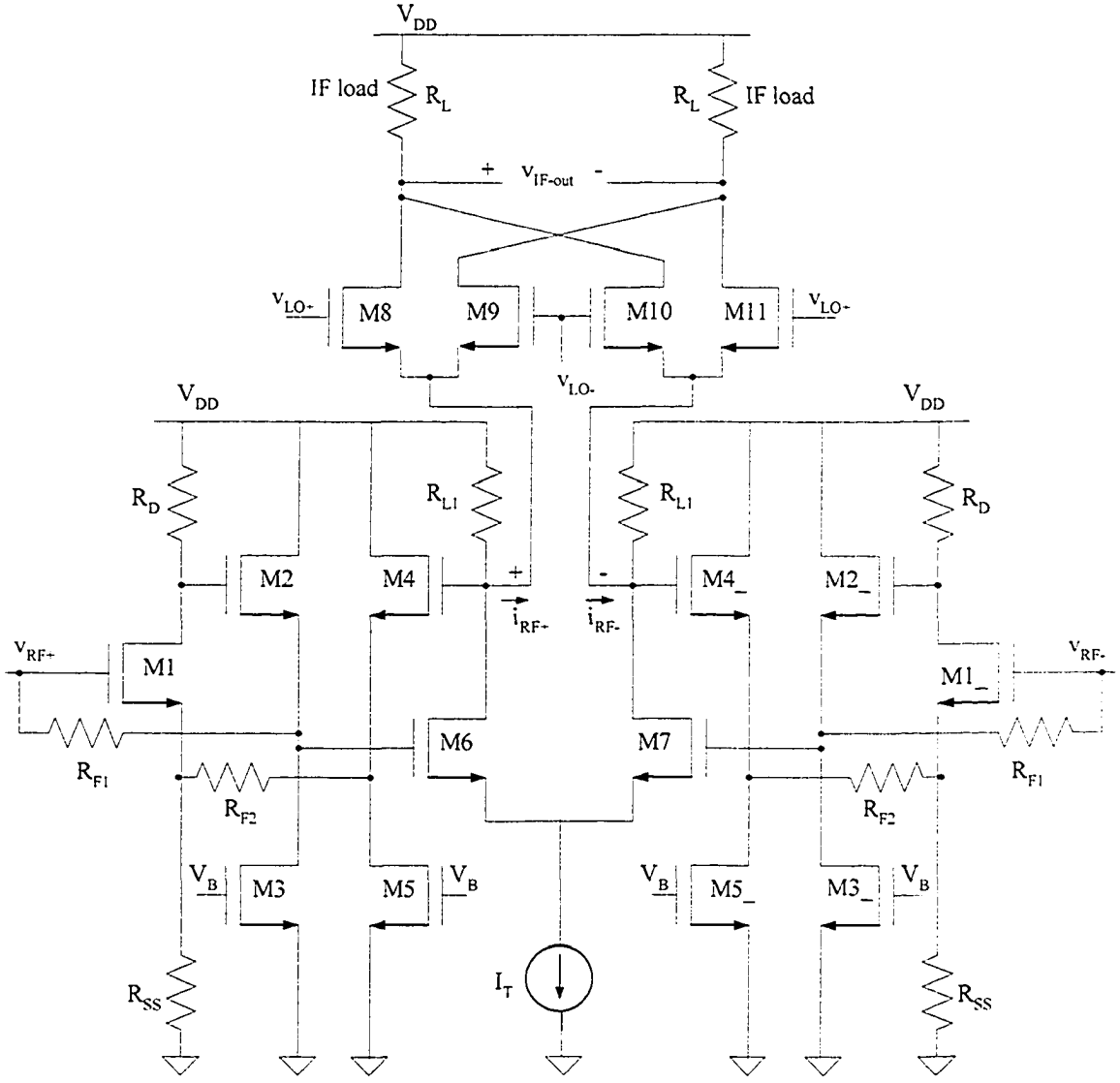


Figure 6.2 The preliminary proposed front-end circuit

With a first look in Figure 6.2, it is difficult to trace the blocks of the front-end as they were seen in Figures 5.10 and 5.16. Again, in this circuit there is a maximum of four elements stacked on top of each other between the power rails that make this circuit unsuitable for low voltage operation, especially with 1.8 V DC supply in a CMOS 0.18 μm process. Therefore, the circuit in Figure 6.2 needs modification. In the first step of modification, the tail current source, I_T is removed with restrictions of only balanced inputs to the source-coupled pair (*M6-M7*) [34]. Moreover, the circuit is rearranged such that LNA and mixer stages are distinctively present. The modified and rearranged circuit for the proposed front-end is shown in Figure 6.3.

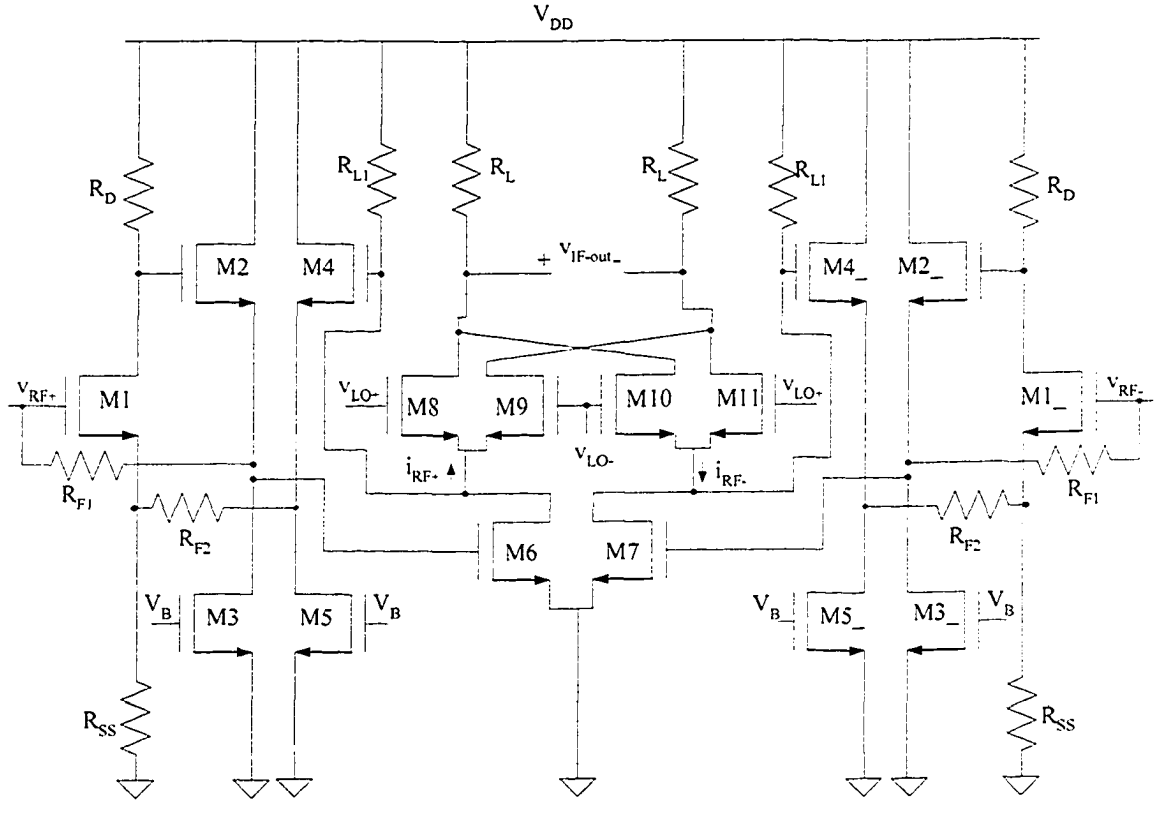


Figure 6.3 The modified front-end circuit

In the circuit of Figure 6.3, LNA and folded switching mixer have been separated in individual stages such that the differential output stage of the LNA has been moved to form the source-coupled pair transconductance stage of the mixer. In an alternative way, it can be said that two two-stage CMOS wideband amplifiers (Figure 4.14) are connected to the Gilbert cell source-coupled switching pairs (Figure 5.16) in a balanced way. For balanced inputs (V_{RF+} and V_{RF-}) (i.e. for fully differential input to the amplifiers) the IF output is also differential. Thus, the overall front-end circuit nature is differential. Moreover, there are maximum three elements between the power rails. Thus, this front-end circuit is suitable for operating with low supply voltage.

6 .2 Linearization Techniques for RF Front-End

In the front-end circuit in Figure 6.3, one can see three distinct stages: the low-noise amplifier of the first stage (*M1* or *M1_*) followed by the second stage transconductance pair (*M6-M7*), and two switching pairs (*M8-M11*) of the final stage. The linearity in the first amplifying stage is reasonably good due to the source degenerated common-source configuration [29]. If the perfect switching with adequate LO signal power is performed, then the transistors in the switching stages contribute a little to the non-linearity of the mixer (or front-end) [32], [34]. For the folded switching mixer in Figure 5.16, input differential RF voltage ($|v_{RF+}| = |v_{RF-}| = v_{RF}$) is converted to the differential current $i_{diff.RF}$ as

$$i_{diff|RF} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} + v_{RF} - V_{TH})^2 - \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} + v_{RF} - V_{TH})^2 \qquad (6.2.1)$$

or,

$$i_{diff|RF} = 2\beta(V_{GS} - V_{TH})v_{RF} \tag{6.2.2}$$

where $\beta = (W/L)\mathrm{x}(\mu_n C_{ox})/2$ is process parameter. From (6.2.2), it is noted that the linearity of the input differential pair in the transconductance stage depends only on the input RF voltage v_{RF} while gate-source overdrive voltage (V_{GS}-V_{TH}) sets the transconductance. In practice, the *V-I* conversion for the transconductance in the input stage is not fully linear [28]. Thus, the linearity of the entire front-end is limited by the linearity of input transconductance pair (*M6*, *M7*) of the mixer. Therefore, a linearization technique "feedforward" as shown in Figure 6.4 can be used [62].

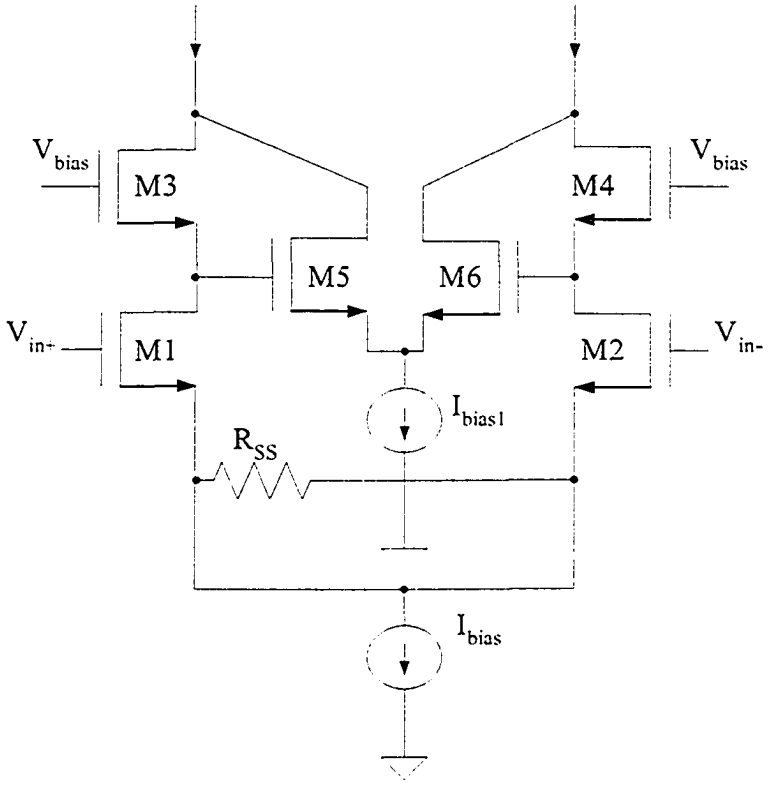


Figure 6.4 MOSFET "cascomp" [31]

The circuit in Figure 6.4 can be further modified as shown in Figure 6.5 where a source-coupled transistors pair is used instead of an inner differential pair and the drains of this transistor pair are connected in direct-mode instead of cross-mode. For a linear transconductance circuit, the output current should be precisely proportional to the input voltage. In this new linearization technique, the effective transconductance of the source-coupled pair (*M6-M7*) is reduced, which in turn, reduces the total harmonic distortion (THD) [29]. Thus, the third and higher order nonlinearities are suppressed significantly due to the reduced total harmonic distortion. This issue will be further analyzed in the Section 6.3.1. With adoption of the new linearization technique in Figure 6.5, the final and complete circuit for the proposed two-stage CMOS wideband front-end is shown in Figure 6.6.

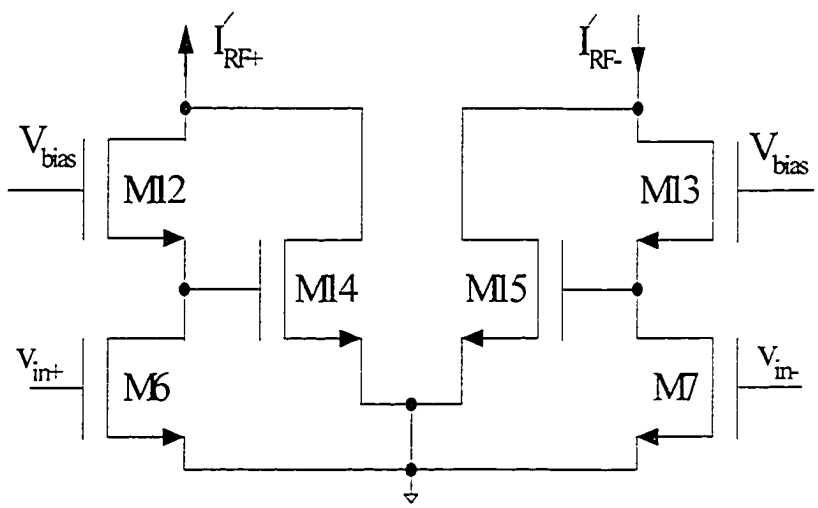


Figure 6.5 Modified linearization circuit from the concept of "cascomp".

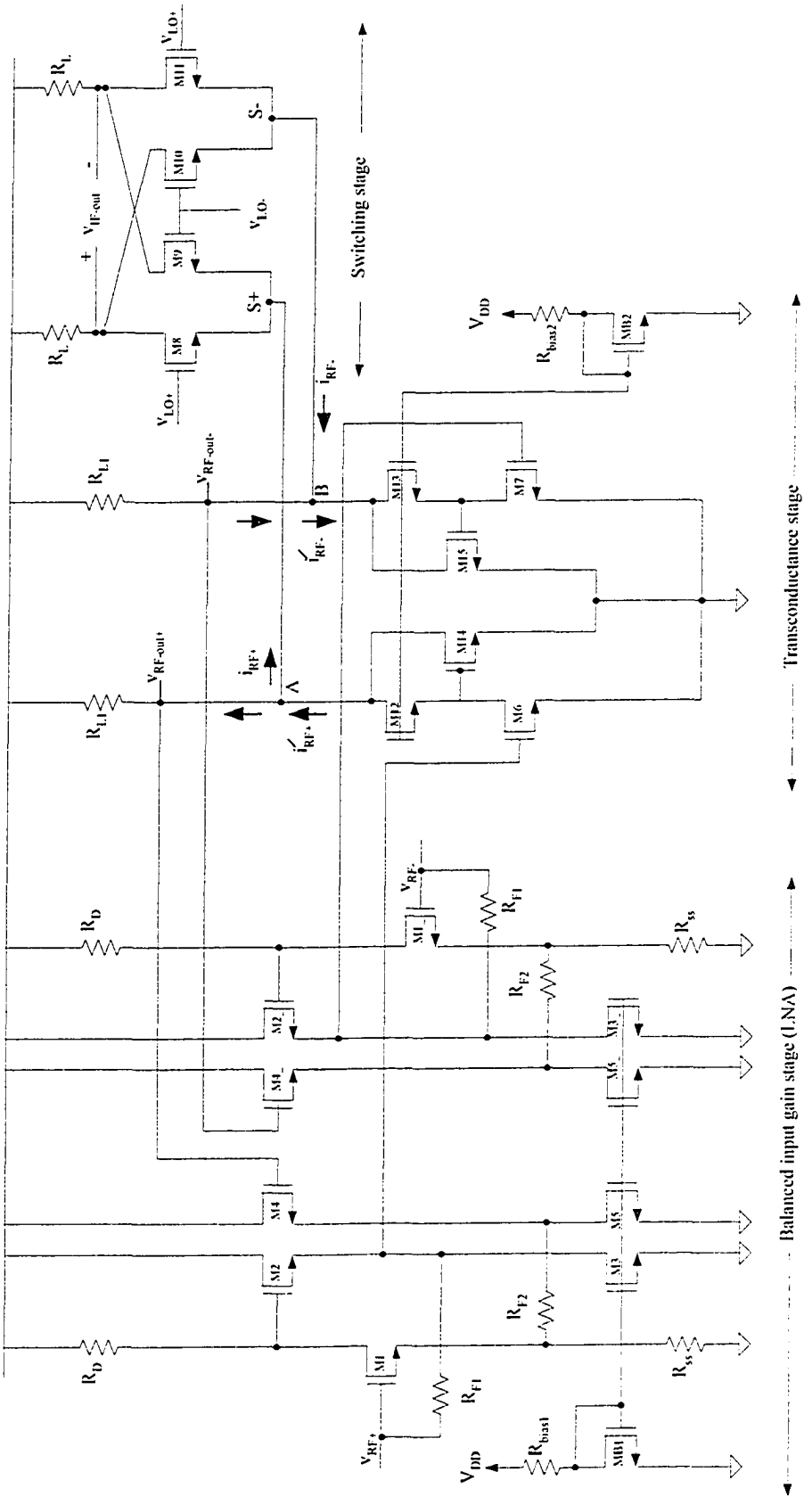


Figure 6.6 Final and complete circuit for the proposed wideband front-end

6 .3 Circuit Description and Analysis

The complete circuit of the proposed wideband front-end is shown in Figure 6.6. This circuit has been developed in a systematic and step-by-step approach as described in section 6.2. In the complete circuit, there are maximum three elements between the power rails (power supply and ground). Therefore, this circuit is suitable for low supply voltage operation by keeping all transistors in saturation with adequate gate overdrive voltages (V_{GS}-V_{TH}). The input wideband matching (to 50 Ω) is achieved by the combined effects of local series-series feedback (resistance R_{SS}) and shunt-series feedback (resistance R_{F1}) via source follower as described in chapter 3 and 4. From the output of the transconductance stage, a common-mode global feedback (resistance R_{F2}) to the input stage increases overall linearity [53]. A very high resistance (R_{F2}) in the global feedback path and a very low resistance ($<<R_{L1}$) looking in to the source-coupled pair of the switching transistors (*M8-M11*) drive maximum amount of RF current to the IF load resistors (R_L). DC biasing for the transistors (*M3*, *M3_*, *M5*, *M5_*, *M14* and *M15*) is a part of the circuit. The switching transistors (*M8-M11*) are biased externally (not shown). The circuit in Figure 6.6 is a fully symmetric circuit with respect to its input and output. Therefore, in theoretical analysis, half-circuit concept [29] is used. Moreover, stage-by-stage analysis can be performed

As mentioned earlier, the entire front-end can be considered as a mixer block with amplified RF inputs. Therefore, the performance parameters of such a front-end can be described in that of a mixer. The functionality of the proposed front-end circuit in Figure 6.6 is different from that of traditional Gilbert cell mixer. Due to the current distribution at node "A" (or "B"), only a part of the RF current passes to the IF load resistor, R_L.

Without the source-coupled pair, *M14-M15*, the transconductance stage neglecting body effect (γ=0) becomes a cascade configuration (for half circuit) with small-signal gain of $A_V=g_{m6,8}R_{L1}$. Thus, without transistors (*M14-M15*), the analysis of small-signal low-frequency models with the assumptions of $g_mR_{SS}>>1$, and $R_{F2}>>R_D$, R_{SS} gives the RF signal gain and input impedance as

$$A_v = \frac{v_{RF-out}}{v_{RF-in}} \approx (g_{m6,8}R_{L1}) \times \frac{R_D R_{F1}}{R_{SS}(R_{F1}+R_D)}. \tag{6.3.1}$$

$$Z_{in} \approx \frac{R_{F1} + R_D}{1 + \frac{R_D}{R_{SS}}}. \tag{6.3.2}$$

Again, with further assumption of $R_{F1}>>R_D$, the second factor in equation (6.3.1) is reduced to R_D/R_{F1}, the gain of the source-degenerated common-source stage (*M1*). Thus the gain in (6.3.1) is simplified to

$$A_v = \frac{v_{out-RF}}{v_{in-RF}} \approx \left(g_{m6,8}R_{L1}\right) \times \left(\frac{R_D}{R_{SS}}\right). \tag{6.3.3}$$

Note that RF signal gain is simply the multiplication of the gain in the input stage and the gain in the transconductance stage.

With (*M14-M15*) involved in linearization process, the equivalent transconductance of the source-coupled transistors (*M6-M7*) is reduced by the factor, $g_{m14,15}/g_{m12,13}$. Then, the gain in equation (6.3.1) is modified to

$$A_v = \frac{v_{RF-out}}{v_{RF-in}} \approx \left[g_{m6,8}\left(1 - \frac{g_{m14,15}}{g_{m12,13}}\right) \times R_{L1} \right] \times \frac{R_D R_{F1}}{R_{SS}(R_{F1}+R_D)}. \tag{6.3.4}$$

If we look at node "A" (or "B"), the RF current I'_{RF+} (or I'_{RF-}) is divided between R_D and resistance looking into the source-coupled point, $S+$ (or $S-$). Neglecting the body effect ($\gamma=0$) in the switching transistors, the impedance seen into the point $S+$ is $1/g_{m8,9}$. For maximum amount of RF power to be passed to the IF load resistor R_L, the condition $R_D \approx (1/g_{m8,9})$ needs to be satisfied. Thus, the part of RF current passing to the IF load resistor, R_L is

$$i_{RF+} = i'_{RF+} \times \frac{R_{L1}}{R_{L1} + \frac{1}{g_{m8,9}}}. \tag{6.3.5}$$

Hence, the conversion gain for the proposed wideband front-end is found as

$$G_C = \frac{v_{IF-out}}{v_{RF-in}} \approx \frac{2}{\pi}\left[g_{m6,8}\left(1 - \frac{g_{m14,15}}{g_{m12,13}}\right)\right] \times \frac{R_D R_{F1}}{R_{SS}(R_{F1} + R_D)} \times \frac{R_L}{1 + \frac{1}{R_{L1} g_{m8-10}}}. \tag{6.3.6}$$

For $R_{F1} >> R_D$ and $R_{L1}g_{m8-10} >> 1$, the conversion gain in (6.3.6) becomes

$$G_C \approx \frac{2}{\pi}\left[g_{m6,8}\left(1 - \frac{g_{m14,15}}{g_{m12,13}}\right) \times R_L\right] \times \frac{R_D}{R_{SS}}. \tag{6.3.7}$$

Note that overall front-end conversion gain is simply the multiplication of the conversion gain of the folded switching mixer and the gain in the input wideband LNA stage ($\approx R_D/R_{SS}$).

6 .4 Circuit Implementations

The proposed wideband front-end in Figure 6.6 was implemented in CMOS 0.18 μm process [45]. Two small-signal parameters for the proposed front-end circuit at first approximation are determined by equations (6.3.2) to (6.3.6). Note that input impedance given by (6.3.2) is independent of DC operating points and the active device dimensions (*W/L*). The circuit has a number of flexibilities to achieve 50 ohms input-impedance by a fair selection of resistance values in (6.3.2) that has be been discussed in Section 4.3.4. A large value of R_{SS} increases the noise contribution as it is connected in series with source of the transistor. Therefore, to keep noise at acceptable level, R_{SS} ($\approx 5\ \Omega$) in series with source of the transistors *M1* (or, *M1_*) is used. The large value of R_D and R_{F1} increases gain in LNA stage but reduces the input bandwidth drastically. Here, the reasonable values for R_D and R_F are chosen to achieve moderate gain. Then, to approximate the condition of $g_{m1}R_{SS1}>1$ and $g_{m2}R_{ss2}>1$, the transconductance g_{m1} (or $g_{m1\_}$) are made high with large transistor sizes ($=W/L$) and reduced overdrive ($=V_{GS}-V_{TH}$) voltages.

The overall conversion gain, G_C depends on many factors as depicted in equation (6.3.6) and (6.3.7). For increased linearity with reduced effective transconductance, the ratio ($g_{m14,15}/g_{m12,13}$) is kept as high as possible. On other hand, to maintain a reasonable conversion gain, this ratio is kept as low as possible. However, the conversion gain and the overall linearity are traded-off with each other. Here, the ratio ($g_{m14,15}/g_{m12,13}$) is basically governed by the transistor sizes(W/L). The RF current distribution at node "A" (or, "B") is shown in Figure 6.6. To have higher conversion gain, the maximum amount of RF power needs to be diverted to the IF load resistor, R_L. This can be done by

choosing a large value of resistor R_{L1} such that it satisfies the condition $R_{L1} \approx 1/g_{m8\text{-}11}$, the resistance looking into the source-coupled point *S*+ (or, *S*-) in the switching stage. For further increase in overall conversion gain, a large value IF load resistor R_L is chosen so that a small current flows through the switching stage transistors (*M8-M11*), which in turn reduces the overall noise contributions from the switching stage. The overall noise figure and linearity for the front-end circuit are governed by equations (5.1.2) and (5.1.3).

DC biasing for the proposed wideband front-end is mostly internal. All the current-source transistors (*M3*, *M3_*, *M5*, and *M5_*) are biased using a common voltage reference consisting of resistor R_{bias} and transistor *MB1*. To avoid transistor mismatches, the minimum transistor feature sizes are avoided, i.e. the length ($=L_{min}$) for the transistor gates (*M3*, *M3_*, *M5*, *M5_*, and *MB1*) are chosen 0.5 μm instead of the minimum feature length 0.18 μm. Transistors *M12* and *M13* are biased with another voltage reference that consists of transistor *MB2* and R_{bias2} so that they remain in saturation. The switching transistors (*M8-M11*) are biased with external DC gate voltage to keep them in saturation. This keeps the provision of trading conversion gain with linearity as required.

For the proposed CMOS wideband front-end in Figure 6.6, the values of all the resistances and transistor sizes are summarized in Table 6.1. The values of all the components are achieved after several iterations of computer simulations in optimizing the front-end performance with estimated parameters. The physical implementations of these components (resistors and transistors) for high-frequency RF applications have already been discussed earlier in section 4.3.5. To reduce series gate resistance and increase current carrying capacity of the active regions (source and drain) the multi-fingered-gates transistor layouts are used. The resistor layouts with dummy resistors

(guard-bands) are designed with added advantages as described in section 4.3.5. The complete layout for the proposed wideband front-end occupies a die area of 1.125 x 0.975 mm^2.

Table 6.1: The values of all the components for the proposed front-end in Fig. 6.6.

Component	Component parameter	Value
*M1, M1_*	*W/L*	250 µm/ 0.18 µm
*M2, M2_*	*W/L*	270µm/ 0.18 µm
*M3, M3_*	*W/L*	140 µm/ 0.5 µm
*M4, M4_*	*W/L*	50 µm/ 0.18 µm
*M5, M5_*	*W/L*	140 µm/0.5 µm
M6, M7	*W/L*	300 µm/ 0.18 µm
M8-M11	*W/L*	60 µm/ 0.18 µm
M12, M13	*W/L*	500 µm/0.18µm
M14, M15	*W/L*	100 µm/0.18µm
MB1	*W/L*	30 µm/ 0.5 µm
MB2	*W/L*	20 µm/ 0.5 µm
R_{F1}	-	350 Ω
R_{F2}	-	2 kΩ
R_D	-	170 Ω
R_{L1}	-	190 Ω
R_L	-	450 Ω
R_{SS}	-	5 Ω
R_{bias1}	-	14 kΩ
R_{bias2}	-	270 Ω

6 .5 Simulation: Results and Analysis

The proposed front-end circuit in Figure 6.6 was realized in CMOS 0.18 μm process and is now in the process of fabrication. The post layout pad-to-pad simulation was performed using circuit simulator SpectreRF in *Cadence*. The circuit was simulated at four different RF input frequencies of 900 MHz, 1.9 GHz, 2.5 GHz, and 3.5 GHz. For 4 MHz estimated IF frequency, the LO signals are applied with 889 MHz, 1.896 GHz, 2.496 GHz, and 3.496 GHz, respectively. In simulation, the two ideal balun transformers were used at the input and output for converting the input RF single-ended signal to the balanced differential-signal and the output IF differential signal to the single-ended signal respectively. Moreover, the output was matched to 50 Ω using external off-chip matching circuits at IF frequency of 4 MHz. The simulated results for different performance parameters as described in section 5.1 and DC operating points are summarized in Table 6.2. These results were taken from the various simulation plots as depicted in Figure 6.7 to Figure 6.12.

Figure 6.7 shows the simulation plot of overall conversion gain for different input RF frequencies. Here, the conversion gain is measured with respect to the input frequencies at 900 MHz, 1.9 GHz, 2.5 GHz, and 3.5 GHz. Since the frequency is converted to the IF frequency, the similar results can be measured by the forward S-parameter term S_{21} at the output frequency of 4 MHz as depicted in Figure 6.8. Figure 6.9 shows the noise figure measured with referred to the output IF frequency (at 4 MHz). The 1-dB compression point is depicted in Figure 6.10 for different input RF frequencies. The overall RF-to-IF *IIP3* for the input RF frequencies of 1.9 GHz and 2.5 GHz is shown in Figure 6.11. The input return loss (S_{11}) is shown in Figure 6.12

Table 6.2: Simulation results for the proposed front-end with IF 4 MHz

Input RF Frequency	900 MHz	1.9 GHz	2.5 GHz	3.5 GHz
Overall conversion Gain (G_C) in dB	17.6	15.6	13	7.5
Overall SSB noise figure (NF) in dB	6.8	7.1	8.0	10
Overall 1-dB compression point in dBm	-11.5	-11.2	-10.8	-8.5
3rd-order intercept point ($IIP3$) in dBm	-1.8	-1.2	+0	+2.6
Input Return Loss (S_{11}) in dB	-26.5	-16	-12	-10
LO-port DC bias voltage in V	1.45	1.45	1.45	1.45
Input RF power in dBm	-30	-30	-30	-30
LO power in dBm	0	0	0	0
DC current consumption in mA	22.3	22.3	22.3	22.3
DC Supply Voltage in V	1.8	1.8	1.8	1.8

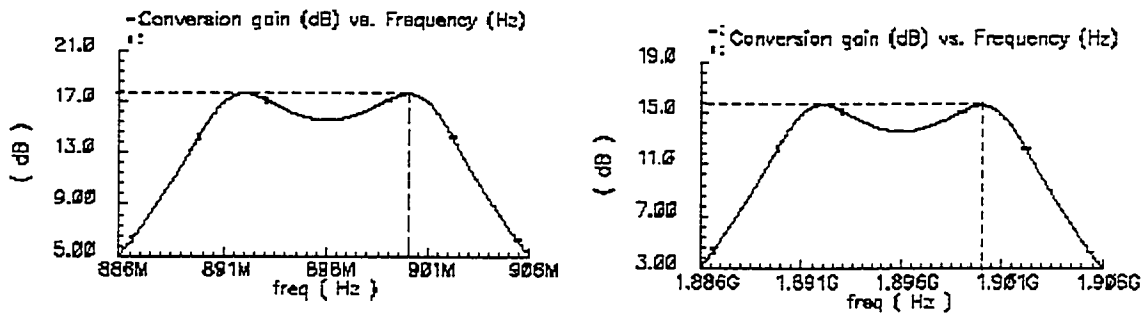
From the plots of conversion gain versus frequency (Figure 6.7), it is noted that the conversion gain peaks around the respective input RF frequencies (900 MHz, 1.9 GHz, 2.5 GHz, and 3.5 GHz). At these frequencies, maximum power transfer occurs from RF to IF with input and output impedances matched to 50 Ω. Again, conversion decreases at higher input RF frequencies. At higher RF frequencies, the effects of parasitic capacitances and resistances and secondary transistor effects come into consideration significantly, which degrades the input impedance matching of the circuit. Due to this increased mismatching at higher RF frequencies, the power transfer from RF to IF is

reduced and thus, the conversion gain decreases at higher input RF frequencies. Figure 6.8 shows the plot of conversion gains with respect to the output IF frequency of 4 MHz.

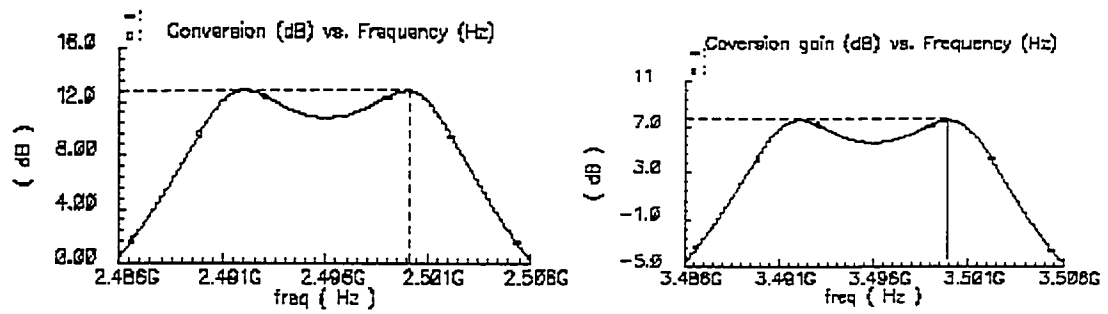
Figure 6.9 shows a plot of SSB noise figure versus output IF frequency. Here, all the noise folds to the output IF frequency of 4 MHz. With increasing input RF frequency, noise also increases due to the impedance mismatches. Besides, leakages and increased parasitics at higher frequency cause increased noise.

Figure 6.10 shows the plotting of 1-dB compression point, caused by harmonic distortion (one of the nonlinear effects), over a range of input RF power (dBm) at specific input frequency (900 MHz or 1.9 GHz or 2.5 GHz, or 3.5 GHz). Note that with increasing input RF frequency, 1 dB compression-point shifts upward. Due to the differential nature of the front-end circuit, even order harmonics are filtered out. At higher RF frequencies, the 3^{rd} order and other higher order odd harmonics are reduced significantly causing reduction of total harmonic distortion. Therefore, with increasing RF frequency, nonlinear effects due to the harmonic distortion are reduced, and thus the 1-dB compression becomes higher. Note that gain and linearity can be alternatively traded off with each other due to the opposite characteristics.

Figure 6.11 shows another nonlinearity measurement, *IIP3* against input RF power for the frequencies of 1.9 GHz and 2.5 GHz. Here, the 1-dB compression point plot in Figure 6.10 was obtained with single-tone applied. Thus, the *IIP3* measured from the plot in figure 6.11 closely satisfy equation (2.1.18), the relation between *IIP3* and 1-dB compression point (*IIP3* is almost 9.6 dB above the 1-dB compression point).

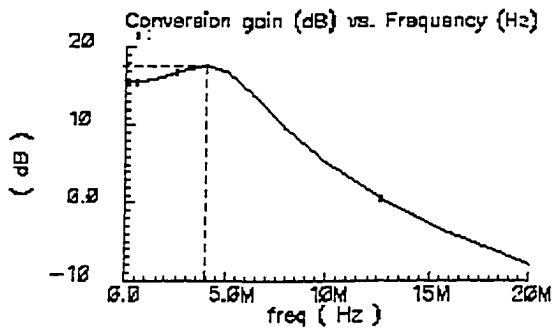


(a) Conversion gain at RF freq. 900 MHz (b) Conversion gain at RF freq. 1.9 GHz

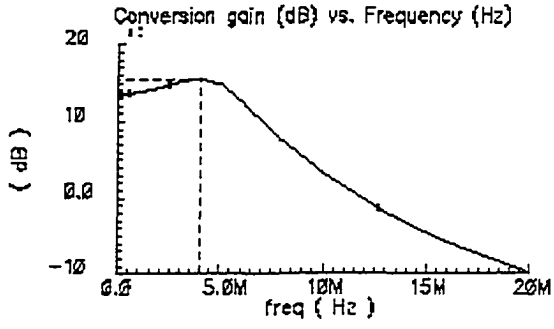


(c) Conversion gain at RF freq. 2.5 GHz (d) Conversion gain at RF freq. 3.5 GHz

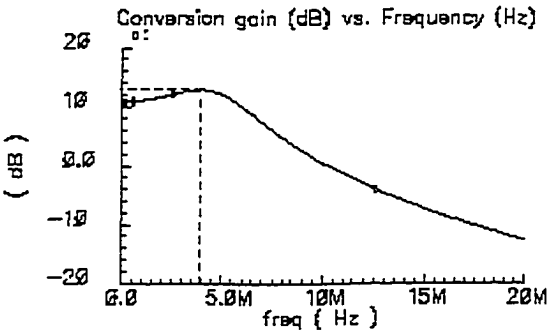
Figure 6.7 Conversion gain for different input RF frequencies (SpectreRF simulation).



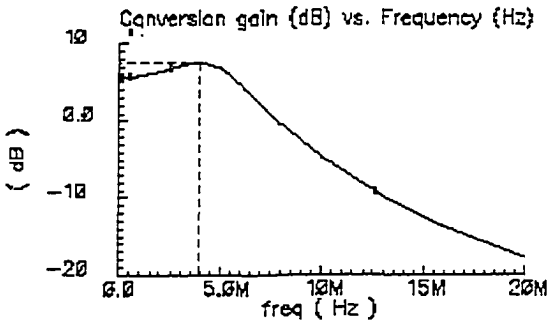
(a) Conversion gain at IF freq. 4 MHz



(b) Conversion gain at IF freq. 4 MHz

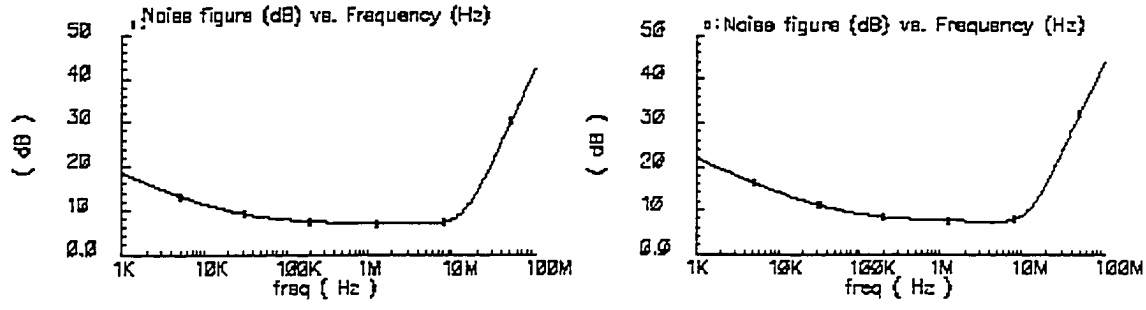


(c) Conversion gain at IF freq. 4 MHz

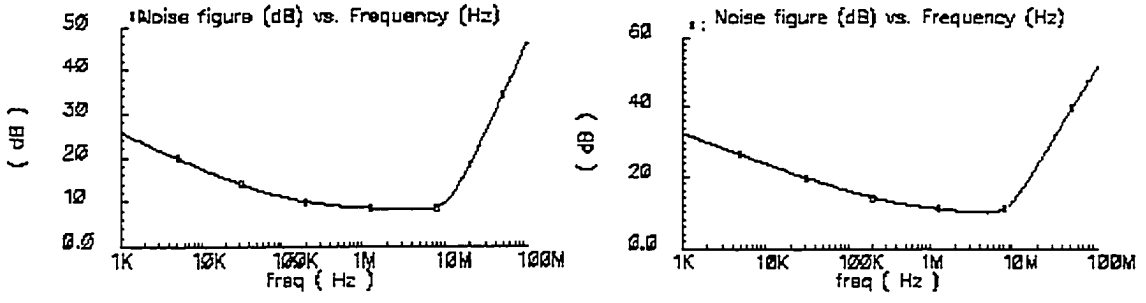


(d) Conversion gain at IF freq. 4 MHz

Figure 6.8 Conversion gain at output IF frequency (SpectreRF simulation)

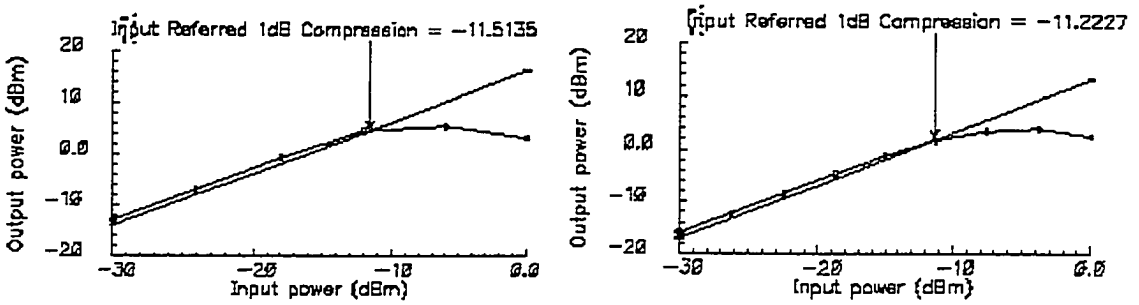


(a) Noise figure at RF freq. 900 MHz (b) Noise figure at RF freq. 1.9 GHz

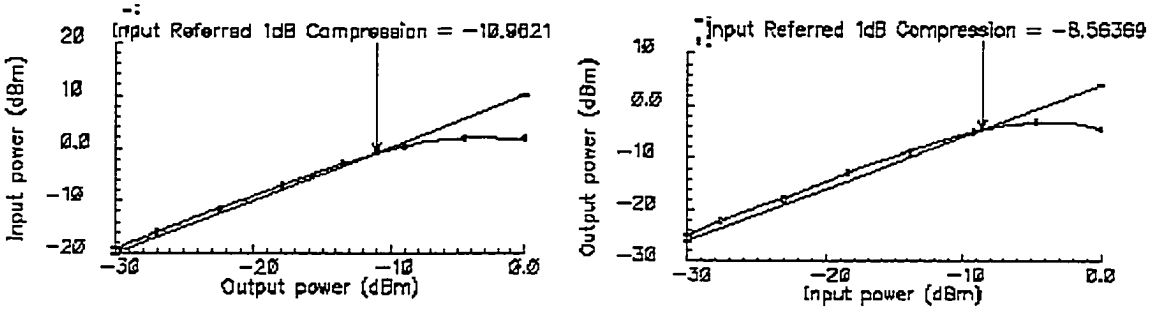


(c) Noise figure at RF freq. 2.5 GHz (d) Noise Figure at RF freq. 3.5 GHz

Figure 6.9 Noise figure at IF frequency for different input RF frequencies (SpectreRF Simulation)

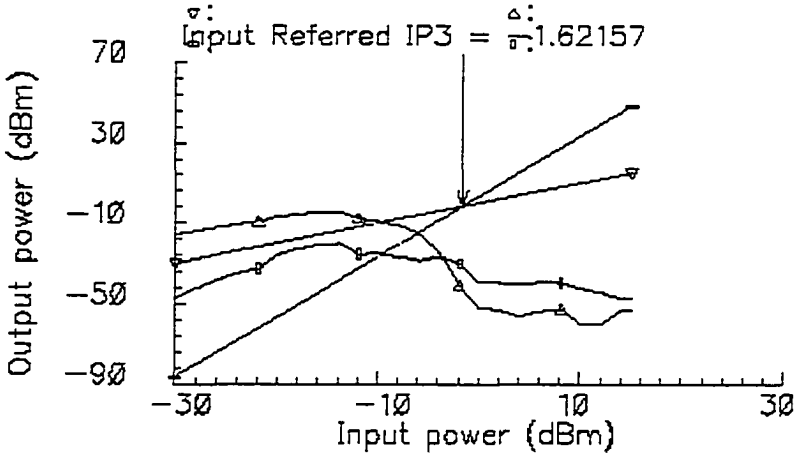


(a) 1-dB comp. point at RF freq. 900 MHz (b) 1-dB comp. point at RF freq. 1.9 GHz

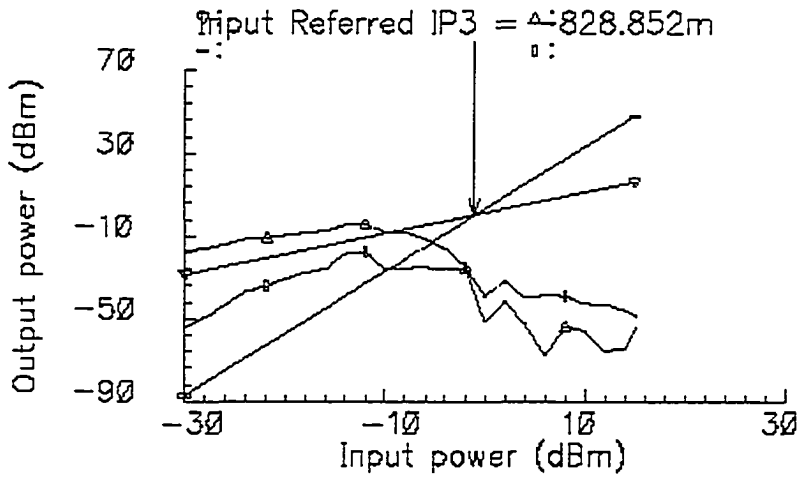


(c) 1-dB comp. point at RF freq. 2.5 GHz (d) 1-dB comp. point at RF freq. 3.5 GHz

Figure 6.10 1-dB compression point at different input RF frequencies (SpectreRF simulation)



(a) Input *IP3* (*IIP3*) for RF frequency of 1.9 GHz.



(b) Input *IP3* (*IIP3*) for RF frequency of 2.5 GHz

Figure 6.11 SpectreRF simulation results for input *IP3* (*IIP3*)

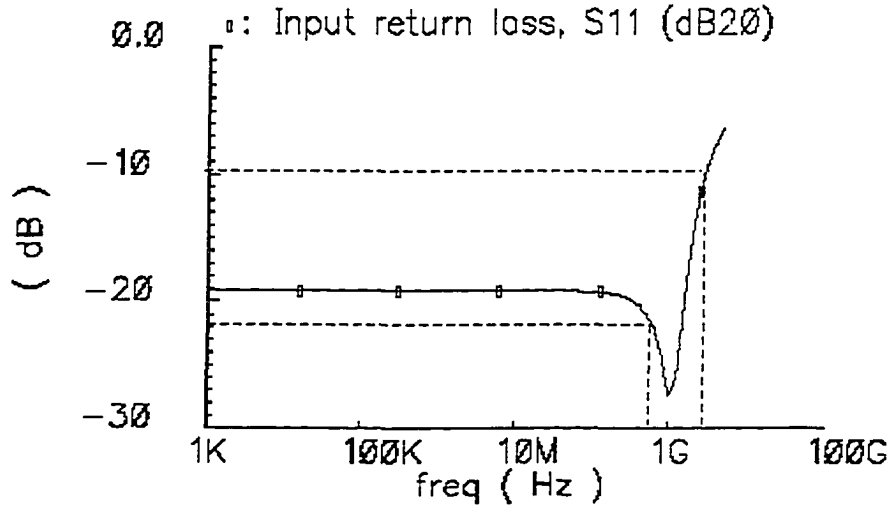


Figure 6.12 Input return loss (S_{11})

Figure 6.12 shows the input return loss (S_{11}) over the RF frequency, which varies from –26 dB to –10 dB in the range of 900 MHz to 3.5 GHz (as illustrated by the doted lines). At higher RF frequencies due to the input impedance mismatch, the reflection of the signal increases and forward transmission of the signal decreases. Thus, input return loss (*S11*) is increased and the gain is decreased with increasing frequency.

6 .6 Comparative Study of Wideband Front-Ends

The performance parameters of the proposed wideband front-end in this thesis and those of the front-ends as described in [24], [63] are compared in Table 6.3. The wideband front-end in [24] was implemented in SiGe bipolar process operating with DC supply voltage of 5 V. The CMOS version of the front-end in [24] was implemented in [63] operating with DC supply voltage of 3 V.

Table 6.3: Comparative results of different wideband front-ends

Front-End	Thesis Front-end			Front-end in [24]			Front-end in [63]		
Process	CMOS 0.18 μm			SiGe bipolar			CMOS 0.18 μm		
DC Voltage Supply	1.8 V			5 V			3 V		
Type of Results	Measured from Layout Simulation (pad-to-pad)			Measured from the device			Measured Schematic simulation		
RF Frequency	900 MHz	1.9 GHz	2.5 GHz	900 MHz	1.9 GHz	2.5 GHz	900 MHz	1.8 GHz	2.5 GHz
Conversion Gain (dB)	17.6	15.6	13	19.3	19.2	N/A	15	12.21	11.31
Noise Figure (dB)	6.8	7.1	8.0	3.7	3.8	N/A	4.4	6.3	7.5
Noise Figure type	SSB	SSB	SSB	DSB	DSB	DSB	DSB	DSB	DSB
1-dB Compression point (dBm)	-12	-11.2	-10.8	N/A	-20	N/A	N/A	-15	N/A
IIP3 (dBm)	-2.8	-1.5	+0	-3	-4.5	N/A	-3.2	+3	4.5
DC Current (mA)	22.3	22.3	22.3	13	13	13	14.4	14.4	14.4

Note that performance of the proposed front-end in this thesis is comparable to those of the front-ends in [23], [42].

The conversion gain of the proposed wideband front-end is higher than its CMOS counterpart in [63] at all input RF frequencies. The SSB noise figure is almost 3 dB higher than the DSB noise figure as described in section 5.3.2. Therefore, the noise performance of the proposed wideband front-end is better than that of in [63]. A linearity measure in terms of 1-dB compression point due to harmonic distortion is always better than that of in [24], [63]. As well, a linearity measure IIP3 due to intermodulation distortion in the proposed wideband front-end degrades at higher frequencies (1.9 GHz and 2.5 GHz) than its counter part in [63]. However, the overall performance of the front-end in [63] will be significantly degraded when the above parameters will be measured from post-layout pad-to-pad simulation. The average DC power consumption in the front-ends of [24] and [63] is 65 mW and 43 mW respectively whereas the proposed front-end consumes 40 mW power. Besides, due to the architectural differences, the front-ends in [24] and [63] are not suitable for operating with low DC supply of 1.8 V. Thus, the overall performance of the proposed CMOS-wideband front-end will be higher than the front-ends in the reference papers.

6 .7 Conclusion

In this chapter, a new CMOS wideband front-end has been designed with a new technique of linearization that makes the circuit suitable for operating with low supply voltage of 1.8 V. The overall front-end circuit has been designed in a systematic approach

that makes the circuit analysis simpler because the overall circuit has been partitioned into three distinctive stages of a wideband LNA, a transconductance stage and the final switching stages. The theoretical analysis for conversion gain and input impedance give first approximation of performance of the wideband front-end. From simulation results, it is noted that the performance of the proposed wideband front-end is comparable to the performance of the frond-ends in the referenced papers.

Chapter 7

Conclusion

In today's multiband, multistandard wireless communication systems, wideband amplifiers and wideband front-ends are inevitable for cost-effective single-chip solution. There are a number of factors that need to be considered for the optimum performance of these circuits so that they are compatible with different wireless standards. In addition to the wider bandwidth in the range of DC to GHz frequency range, moderate gain, minimum noise figure and increased linearity are the highly expected figures of merit in the design of wideband amplifier and wideband front-end. Avoiding the use of passive components such as inductors and capacitors in the design of CMOS RF ICs ensures high degree of integration leading to a cost-effective solution.

The first part of this thesis included the design, investigation and implementation of a two-stage CMOS wideband amplifier. Prior to the design of the proposed wideband amplifier, two other well-know wideband amplifiers, namely Kukielka and Meyer configurations have been investigated because little has been done to investigate these amplifiers in a CMOS 0.18 μm process. The proposed two-stage CMOS wideband amplifier is a new configuration, which can be realized using a systematic design

approach. The circuit for this amplifier is such that the DC biasing circuit is developed internally in an isolated manner from the AC signal path. The post-layout pad-to–pad simulation results that closely follow the actual circuit performance show that the proposed two-stage CMOS wideband front-end is a promising one with moderate gain, wide bandwidth and moderate linearity.

The second-part of this thesis included the design and implementation of a new CMOS wideband RF front-end for multistandard low-IF wireless receivers. The front-end design has been resolved into design of stages such that the circuit realization and analysis were simple. A new technique of enhancing linearity in reducing effective transconductance made the circuit suitable for operating with low DC supply voltage. The proposed two-stage CMOS wideband amplifier is used as a half circuit of the differential input stage LNA of the front-end, ensuring high conversion gain and low noise figure in overall. The overall linearity was better compared to the wideband front-ends designed in the references. The front-end is a new type of configuration in CMOS process without using off-chip IR filters between the LNA and mixer, suitable for low-IF applications. Again, the post-layout pad-to-pad simulation brings the circuit characteristics close to the actual device characteristics.

The performance of the RF ICs significantly depends on the physical layouts. To ensure high quality performance with reduced noise and leakages at high RF frequency applications, a number of techniques were employed in the implementation of physical layouts. In the design of transistors with wider widths, multi-fingered-gate layouts were used to reduce gate noise and increase the current carrying capacity of the source/drain active region. To reduce further noise level, non-closed loop substrate-contacted guard-

rings were used around all active and passive devices. In protecting the device against electro-static discharge, RF ESD protection circuit was implemented in the design of wideband amplifier.

In summary, the main contributions of this thesis are highlighted in the following.

1. A new CMOS two-stage wideband amplifier has been designed and implemented in a CMOS 0.18 μm process. The amplifier circuit exhibits bandwidth larger than 2.5 GHz with a DC gain of 14.8 dB and a minimum noise figure of 3.4 dB.
2. A new CMOS wideband front-end has been designed and implemented in a CMOS 0.18 μm process. The front-end circuit shows input bandwidth around 3 GHz with conversion gain of 15.6 dB, SSB noise figure of 7.1 dB, and *IIP3* of – 1.5 dBm at 1.9 GHz.

Both the wideband amplifier and the front-end circuits are in fabrication process. Future work will include testing the actual ICs to validate the theoretical analysis and the simulation results.

References

[1] Asad A. Abidi, "RF CMOS Comes of Age," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 4, pp. 549-561, Apr. 2004.

[2] Behzad Razavi, "RF CMOS Transceivers for Cellular Telephony," *IEEE Communications Magazine*, vol. 41, issue 8, pp. 144-149, Aug. 2003.

[3] Lawrence E. Larsen, "Integrated Circuit Technology Options for RFIC's – Present Status and Future Directions," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 387-399, Mar. 1998.

[4] Asad A. Abidi, "Low-power Radio-Frequency IC's for Portable Communications, *Proc. Of the IEEE*, vol. 83, no. 4, pp. 544-569, Apr. 1995.

[5] S.P. Voinigescu, S. W. Tarasewicz, T. MacElwee, and J. Lliowski, An assessment of the state-of-the-art 0.5μm bulk CMOS technology for RF applications." *Int. Electron Devices Meeting*, pp. 721-724, 10-13 Dec. 1995, Washington, DC USA.

[6] R. R. J. Vanoppen, L. M. F. de Maaijer, D. B. M. Klaassen, and L. F. Tiemeijer, "RF noise modeling of 0.25μm low power LNA's," *Int. Electron Devices Meeting*, Technical Digest, pp. 317-320, 7-10 Dec. 1997, Washington, DC USA

[7] Qiuting Huang, Francesco Piazza, Paolo Orsatti, and Tatsuya Ohguro, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits, " *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1023-1036, Jul. 1998.

[8] Asad A. Abidi, "The Future of CMOS Wireless Transceivers," *IEEE ISSCC Dig. Tech. Papers*, pp. 118-119, Feb. 1997, San Francisco, CA.

[9] J. Rudell et al., " A 1.9 GHz Wide-Band double conversion CMOS integrated receiver for cordless telephone applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 304-305, Feb. 1997, San Francisco.

[10] X. Li, and M. Ismail, *Multi-Standard CMOS Wireless Receivers: Analysis and Design*. Boston, MA: Kluwer, 2002

[11] H. Knapp, D. Zoschg, T Meister, K. Aufinger, S. Boguth, and L. Treitinger, "15 GHz Wideband Ampifier with 2.8 dB Noise Figure in SiGe Bipolar Technology," *IEEE Radio Frequency Integrated Circuits Symposium*, 2001, pp. 287-290, 20-22 May, 2001, Phoenix, AZ USA.

[12] H. Hashemi, and A. Hajimiri, "Concurrent Multiband Low-Noise Amplifiers-Theory, Design, and Applications," *IEEE Transactions on Microwave Theory and Tecchniques*, no. 1, vol. 50, pp. 288-301, Jan. 2002.

[13] S. Anderssom, P. Caputa, and C. Svensson, "A Tuned, Inductorless, Recursive Filter LNA in CMOS," *European Solid-State Circuit Conference*, 2002, pp. 351-354.

[14] Behzad Razavi, *RF Microelectronics*, Prentice Hall PTR, 2000.

[15] L. Lessing, *Man of High Fidelity: Edwin Howard Armstrong, A Biography*, New York: Bantam Books, 1969.

[16] ETSI, *GSM Technical Specification 05.05, v.5.2.0*, ETSI, Jul.1996.

[17] ETSI, Physical Layer v1.5.1, "Part 2, DECT, Common Interface," ETSI, Feb. 2001.

[18] *IEEE P802.11 Wireless LAN Medium Acess Control (MAC) and Physical layer (PHY) Specification,* 1999.

[19] *Bluetooth Specification v.1.0.B, Radio Specification,* www.bluetooth.com.

[20] Jan Crols and Michiel S.J. Steyaert, "Low-IF Topologies for High-Performance Analog Front-Ends of Fully Integrated Receivers," *IEEE Transactions on Circuits and Systems* – II: Analog and Digital Signal Processing, vol. 45, no. 3, pp. 269-282, Mar. 1998.

[21] Asad A. Abidi, "Direct Conversion Radio Transceivers for Digital Communications," *IEEE Journal of Solid-State Circuits*, vol. 30, no.12, pp. 1399-1410, Dec. 1995.

[22] Jan Crols and Michiel S. J. Steyaert, "A Single-chip 900 MHz CMOS Receiver Front-End with a High Performance Low-IF Topology," *IEEE Journal of Solid-State Circuits*, vol 30, no. 12, pp. 83-86, Feb. 1995.

[23] Farbod Behahani, John C. Leete, Yoji Kisigami, Andreas Roithmeier, Koichi Hoshino and Asad A. Abidi, " A 2.4 GHz Low-IF Receiver for Wideband WLAN in 0.6-um CMOS – Architecture and Front-End," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1908-1916, Dec. 2000.

[24] Adiseno, Mohammed. Ismail, and Hakan Olsson, "A Wide-Band Front-End for Multiband Multistandard High-Linearity Low-IF Wireless Receivers," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1162-1168, Sept. 2002.

[25] R. G. Meyer, and R. Blauschild, "A 4-Terminal Wideband Monolithic Amplifier, *IEEE Journal of Solid-State Circuits*, vol. SC-16, no. 6, pp. 634-638, Dec.1992.

[26] C. D. Hull, and R. G Meyer, "Principles of Monolithic Wideband Feedback Amplifier Design," *International Journal of High Speed Electronics*, vol. 3, no. 1, pp. 53-93, Feb. 1992.

[27] I. M. Filanovsky, "Gain-Controlled Resistors in Analysis of Amplifiers Featuring Accurate Input and Output Impedance," *Proc. 43rd Midwest Symposium on Circuits and Systems*, vol. 3, pp.1232-1235, Aug. 2000.

[28] Yu-chang Chen and Shey-Shi Lu, " Analysis and Design of CMOS Broadband Amplifier with Dual Feedback Loops," *Proc. IEEE Asia-Pacific Conference on ASIC*, pp. 245-248, Aug. 2002.

[29] Behzad Razavi, *Design of Analog CMOS Integrated Circuit,* McGraw-Hill Higher Education, New York, 2001.

[30] Domine Leenaerts, John Vander Tang, and Cicero Vaucher, *Circuit Design for RF Transceivers*, Kluwer Academic Publishers, Dordrect, The Netherlands, 2001

[31] John Rogers and Calvin Plett, *Radio Frequency Integrated Circuit Design*, Artech House Inc, Norwood, MA, 2003.

[32] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge, UK, 2002.

[33] Lawrence E. Larson, Editor, *RF and Microwave Circuit Design for Wireless Communications*, Artech House, Inc., Norwood, MA, USA, 1996.

[34] Chris Toumazou, George Moschytz, and Barrie Gilbert: Editors, *Trade-Offs in analog Circuit Design, The Designers Companion*, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2002.

[35] Alan B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley & Sons, Inc., New York 1984.

[36] Igor M. Filanovsky, " Design of Radio-Frequency Integrated Circuit: *EE 671 Course Lecture Note*, ECE, University of Alberta, 2001.

[37] H. S. Black, "Inventing the Negative Feedback Amplifier," *IEEE Spectrum*, Vol.14, pp. 55-60, December 1977.

[38] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Third edition, New York: Wiley, 1993.

[39] Jan Davidse, *Analog Electronic Design*, UK, Prentice Hall, 1991.

[40] J. Kukieilka and C. Snapp, "Wideband Monolithic Cascading Feedback Amplifiers Using Silicon Bipolar Technology," *Monolithic Microwave Integrated Circuits*, IEEE Press, 1985, pp. 330-331.

[41] R. G. Meyer, and R. A. Blauschild, " A 4-Terminal Wide-band Monolithich Amplifier, "*IEEE Journal of Solid-State Circuits*, vol. sc-16, no.6, pp. 634-638, Dec. 1992.

[42] *Cadence*: "*IC Design Tools, version 2002*," *Canadian Microelectronic Corporation*, Queens University, Kingston, Ontario, Canada.

[43] C.J.M. Verhoven, A. Van Staveren, Bert Monna, M.H.I. Kouwehoven and E. Yildiz, *Structred Electronic Design*, Kluwer Academic Publishers, Boston, 2003.

[44] Igor M. Filanovsky, Md. Mahbub Reja, and Ahmed Allam, A New Configuration of a Two-Stage CMOS Wideband Amplifier," *47th IEEE Midwest Sym. on Circuit and Systems*, Hiroshima, Japan, July 25-28, 2004, pp. III-13 – III-16.

[45] Taiwan Semiconductor Manufacturing Co. Ltd., "TSMC 0.18 um Mixed Signal 1P6M Salicide 1.8V/3.3V RF Spice Models," Taipei, Taiwan.

[46] Troels Emil Kolding, "Consistent Layout Techniques for Successful RF CMOS Design," RISC Group, Denmark.

[47] Mohammed Ismail, "Introduction to RF CMOS IC Design for Wireless Applications," eewww.ng.ohio-state.edu/VLSI, Analog VLSI Lab, The Ohio State University, U.S.A.

[48] Ming-Dou Ker, Tung-Yang Chen, Chung-Yu Wu, and Hun-Hsien Chang, "ESD Protection Design on Analog Pin with Very Low Input Capacitance for High-Frequency or Current-Mode Applications," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1194-1199, Aug. 2000.

[49] Ming-Dou Ker "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clam Circuits for Submicron CMOS VLSI," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 173-183, Jan. 1999.

[50] Behzad Razavi, "Architectures and Circuits for RF CMOS Receivers," *IEEE Custom Integrated Conference*, pp. 393-400, 1998.

[51] Ahmed Rofougaran, James Y. C. Chang, Maryam Rofourgan, and Asad Abidi, "A 1 GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 7, pp. 880-890, Jul. 1996.

[52] R. Montemayor, and Behzad Razavi, "A Self Calibrating 900 MHz CMOS Image-Reject Receiver," *Proc. European Solid-State Circuits Conference (ESSIRC) 2000*, pp. 292-295, Sept. 2000.

[53] E. H. Nordholt, " Classes and properties of Multiple Negative–Feedback amplifiers," *IEEE Transactions on Circuit Systems*, vol. CAS-28, pp. 203-211, Mar.1981.

[54] E. H. Nordholt, *Design of High Performance Negative–Feedback Amplifiers*. Amsterdam, The Netherlands: Elsevier, 1983.

[55] F. Bruccoleri, E.A.M. Klumperink, and B. Nauta, Noise Cancelling in Wideband CMOS LNAs, *IEEE International Solid-State Circuits Conference*, pp. 406-407, Feb. 2002.

[56] B. Gilbert, *Mixer Fundamentals and Active Mixer Design*, EPEL Electronic Laboratories.

[57] B. Gilbert, "A Precise Four Quardant Multiplier with Subnano-Second Response," *IEEE Journal of Solid-State Circuits*, vol. 45, SC-3, pp. 365-373, Dec. 1968.

[58] P. J. Sulivan, B. A. Xavier, and W. H. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, pp. 1151-1155, Jul.1997.

[59] Eyed Abou Allam, John J. Nisbet, and Michele C. Mailepaard, "Low-Voltage 1.9 GHz Front-End Receiver in 0.5μm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1424-1443, Oct. 2001.

[60] Tajinder Manku, Galen Beck and Etty J. Shin, "A Low Voltage Design Technique for RF Integrated Circuits," *IEEE Journal of Circuits and Systems II*, vol. 45, pp. 1408-1413, Oct. 1998.

[61] Vojkan Vidojkovic, John van der Tang, Arjan Leeuwenburgh, and Arthur van Roermund, "Mixer Topology Selection for 1.8-2.5 GHz Multistandard Front-End in

0.18μm CMOS," *International Symposium on Circuits and Systems (ISCAS)*, vol. II, pp. 300-303, 2003.

[62] Pat Quinn, "A Cascode Amplifier Nonlinearity Correction Technique," *Digest Technical Papers, ISSSC Conference*, 1981, Vol. XXIV.

[63] Adiseno, Mohammed Ismail, and Hakan Olsson, " Multiband High-Linearity Front-end Receivers for Wireless Applications," *Analog Integrated Circuits and Signal Processing*, vol. 30, no. 1, pp. 59-67, Jan. 2002.

Appendix: Physical Layouts

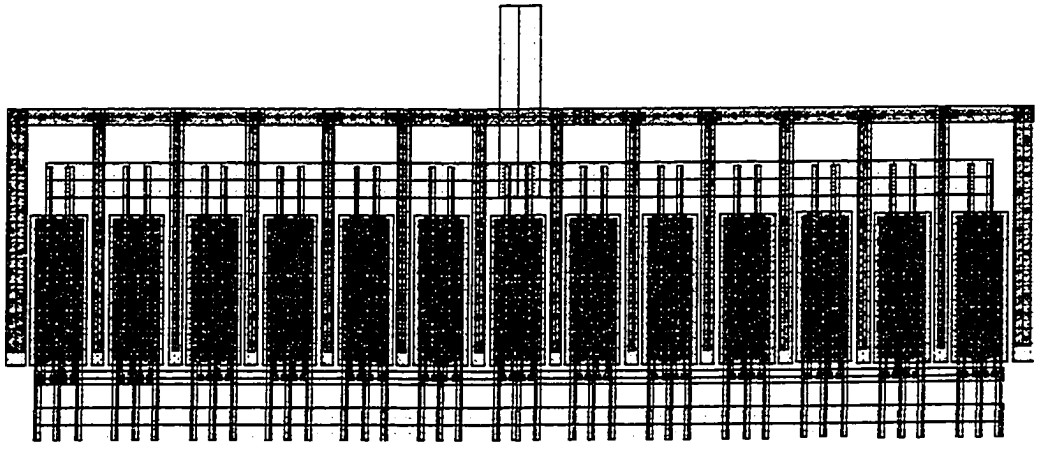


Figure 1 The layout of the multi-fingered, *W/L* (= 520 μm/ 0.18 μm) for the proposed wideband amplifier

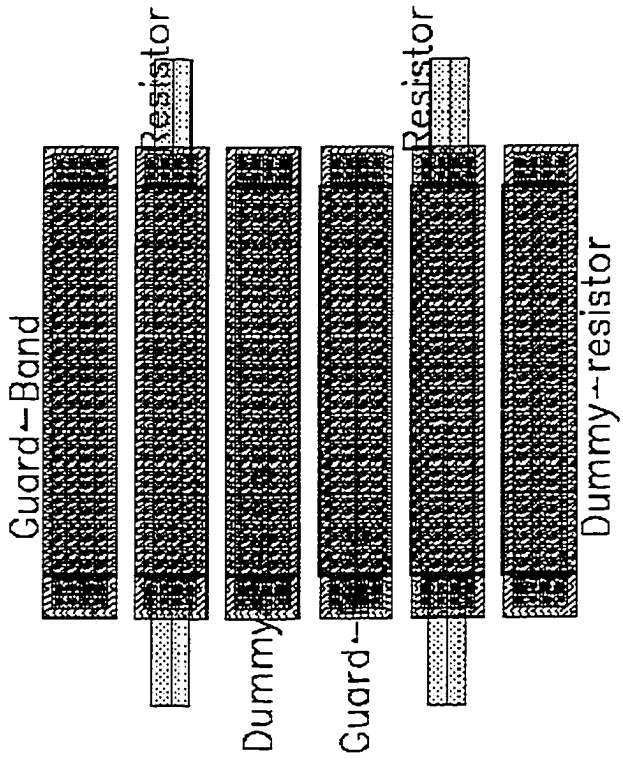


Figure 2 The layout of the resistor with dummy resistors as guard-band

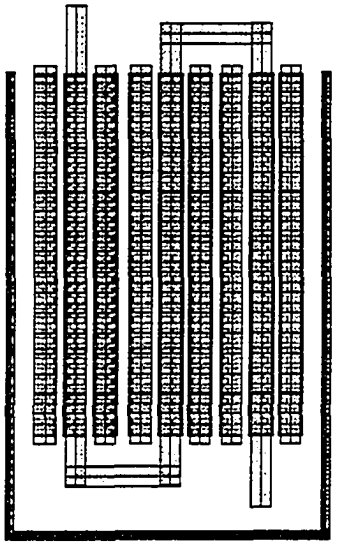


Figure 3 The layout of the 5 ohms metal resistor for the proposed wideband amplifier.