

A Real-Time Nonlinear Hysteretic Power Transformer Transient Model on FPGA

Jiadao Liu, *Student Member, IEEE*, and Venkata Dinavahi, *Senior Member, IEEE*

Abstract—A transformer is the most widely used equipment in power systems to transfer energy from one circuit to another. For real-time electromagnetic transient simulation, this paper presents a digital hardware emulation of the power transformer on a field programmable gate array. The linear model of the transformer is based on the admittance matrix approach. Detailed real-time modeling of the transient nonlinearities, including hysteresis phenomena, is carried out based on the Preisach theory. The nonlinear solution in real time is undertaken using a full Newton iteration. All the hardware modules for the transformer emulation were developed in VHDL. The model is fully parallelized and pipelined to achieve the lowest latency and the smallest hardware resource consumption. Real-time results on the oscilloscope are compared with off-line results from the ATP software.

Index Terms—Electromagnetic transient (EMT) analyses, embedded systems, field programmable gate arrays (FPGAs), hysteresis, real-time systems, saturation, transformer modeling.

I. INTRODUCTION

A REAL-TIME digital simulator is an important tool in the analysis of power systems for the design and development of new solutions to alleviate operational challenges of complex grids. Field programmable gate arrays (FPGAs) have been successfully and widely employed in digital industrial control systems for demanding applications [1]–[5]. FPGAs are also making inroads into real-time simulation due to their parallel hardwired architecture, which allows detailed modeling of power system components with very small time steps to capture transients with high fidelity. FPGA-based digital hardware models of several power system apparatus such as transmission lines, rotating machines, and power electronic equipment [6]–[14] have started to appear in the literature. When it comes to transient simulation, a transformer is the most ignored power system component. In real-time simulation, in particular, to achieve a small time step, as well as to accommodate a large system size on limited simulator hardware, the transformer model is either entirely omitted or represented using a simplified equivalent containing only the winding leakage impedance. Yet, power transformers have a great impact on the behavior of transient overvoltages and overcurrents; for example, phenomena, such as inrush current,

ferroresonance, and harmonics, present daunting technical and economic challenges to customer loads and to system operators.

Transformer models for electromagnetic transient (EMT) analysis can be broadly classified [15] into three groups: 1) admittance matrix representation for multiwinding and multiphase transformers, e.g., the BCTRAN model; 2) star-circuit representation based on the saturable transformer component (STC model); and 3) topology-based representation, e.g., the unified magnetic equivalent circuit (UMEC) model. All of these models are appropriate for low- and mid-frequency transient analysis (up to 10 kHz); however, each of them has inherent limitations, which influence their applicability in real-time simulation. In the BCTRAN model, mutual phase coupling is included; however, this model does not differentiate between different core designs or winding topologies [16]. The main limitation of the STC model is that it cannot be used to represent transformers with more than three windings because of its reliance on the star configuration [17]. The topology-based models, such as UMEC, can represent very accurately any type of core design as long as the design parameters are adequately available [18]. Due to their detailed nature, the computational time of such models can be much longer than the previous two models.

A computationally simple way to represent transformer core nonlinear behavior is to use a piecewise linear representation [19] with multiple slopes for the B – H curve, and implemented using switched linear inductors in several EMT programs. This method is currently employed in both off-line and real-time transient simulations. A more rigorous method is to solve the nonlinearity using an iterative Newton process, of course, at the expense of a higher computational cost. The accurate modeling of hysteresis with independent formation of major and minor loops, as well as the modeling of eddy currents, are paramount for analyzing ferroresonance transients, as well as transient recovery overvoltage [15]. Yet, hysteresis phenomena are usually represented by a constant resistance, or codependent loops, whereas the eddy currents are included as a constant resistor in shunt with the magnetizing inductance in transient programs. Nevertheless, there are detailed magnetic hysteresis models available in the literature, such as the Jiles–Atherton and Preisach models. A comprehensive treatment of hysteresis models can be found in [20]–[22]. Similarly, complex eddy current models are also available [23]–[25]. For real-time simulation, a detailed and accurate implementation of saturation, hysteresis, and eddy current phenomena is yet to be reported in the literature mainly due to their computational complexity.

This paper proposes a real-time nonlinear hysteretic power transformer model on the FPGA. The linear dynamics of

Manuscript received January 8, 2013; revised May 9, 2013, July 3, 2013, and August 9, 2013; accepted August 13, 2013. Date of publication August 22, 2013; date of current version January 31, 2014. This work was supported by the Natural Science and Engineering Research Council of Canada.

The authors are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: jiadao@ualberta.ca; dinavahi@ualberta.ca).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIE.2013.2279377

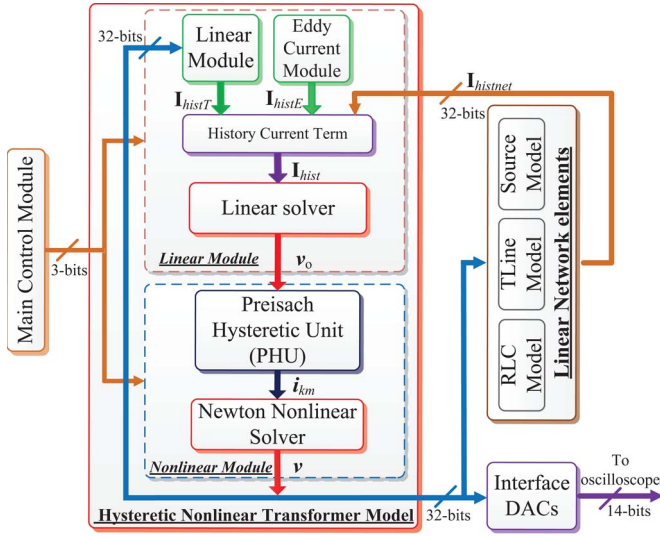


Fig. 1. Overall architecture of the real-time nonlinear hysteretic transformer model on FPGA.

the model are based on the admittance matrix representation. Nonlinear saturation is modeled by a fully iterative Newton-Raphson (N-R) method. The hysteresis phenomena are modeled based on the Preisach theory, whereas the eddy currents in the core are modeled using a frequency-dependent equivalent network. The entire power transformer nonlinear hardware model and the associated numerics were developed using the VHDL language, employing IEEE 32-bit floating-point precision. All the transformer modules employ full hardware parallelism and deep pipelining to optimize the hardware resources and model latency. The real-time simulation results are validated in off-line using the ATP software. The remainder of the paper is organized as follows: Section II provides the hardware design details of the power transformer. Section III provides various case studies and results to validate the emulated transformer model on the FPGA. Section IV gives the conclusion of the paper.

II. DIGITAL HARDWARE EMULATION OF THE POWER TRANSFORMER

The complete real-time transformer model hardware architecture is shown in Fig. 1. It can be divided into three parts: the linear module, the nonlinear module, and the main control module. The linear module is built up based on the admittance matrix approach after discretizing the transformer differential equations, and is used to update the transformer history current terms, and calculates the node voltages without the nonlinear elements according to the compensation method. The nonlinear module contains two parts, i.e., the Preisach hysteretic unit (PHU) and the N-R nonlinear solver unit, for finding the solution to the nonlinear equations. Further details regarding the nonlinear module are provided in Section II-C. The control module sends command signals to other modules to control which functions will be performed by each module and also waits for the signals sent back by each module, so that all modules can be operated either in parallel or sequentially, as

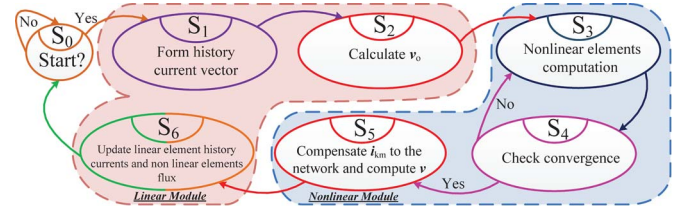


Fig. 2. FSM of the main control module.

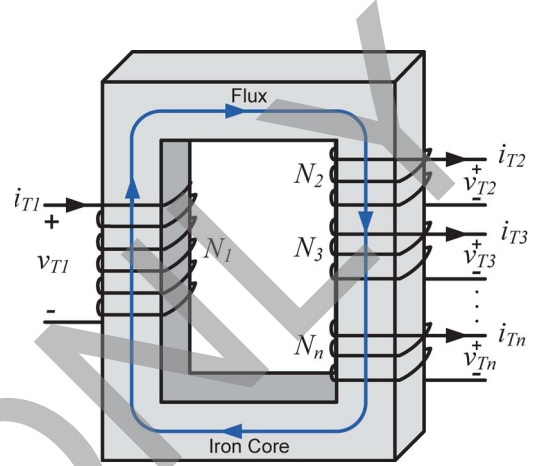


Fig. 3. Single-phase n -winding transformer.

required by the transient algorithm. Fig. 2 shows the detailed finite state machine (FSM) for the main control module. S_1 calculates the summation of all the history current terms (I_{hist}) received from the linear transformer module (I_{histT}), the eddy current module (I_{histE}), and the network components ($I_{histnet}$) that include the passive element (RLC) and transmission line (Tline) modules, which together constitute the linear part of a power system. S_2 computes the nodal voltages (v_o) without the nonlinear elements. S_3 evaluates the nonlinear functions of $f(i_{com})$ and their derivative $df(i_{km})$. S_4 performs the N-R procedure to compute the results in each iteration; if the result is converged, then the FSM goes to S_5 to calculate the nodal voltages (v); otherwise, it goes back to S_3 . In S_6 , the transformer linear module, the eddy current module, and the RLC and TLine modules update their history terms.

A. Admittance Matrix Transformer Representation

1) *Linear Model Formulation:* The admittance matrix formulation results from the concept of mutually coupled coils. Under transient conditions, the governing equations for a single-phase n -winding transformer (see Fig. 3) can be expressed as

$$\frac{d}{dt} i_T = L^{-1} v_T - L^{-1} R i_T \quad (1)$$

where v_T and i_T are $n \times 1$ vectors, which are expressed as $v_T = [v_{T1}(t) v_{T2}(t) \dots v_{Tn}(t)]^T$ and $i_T = [i_{T1}(t) i_{T2}(t) \dots i_{Tn}(t)]^T$, respectively. R is an $n \times n$ diagonal matrix of winding

resistance and \mathbf{L} is an $n \times n$ matrix of winding leakage inductances, which are given by

$$\mathbf{R} = \text{diag}\{R_1 \ R_2 \ \dots \ R_n\}, \mathbf{L} = \begin{bmatrix} L_{11} & L_{12} & \dots & L_{1n} \\ L_{21} & L_{22} & \dots & L_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n1} & L_{n2} & \dots & L_{nn} \end{bmatrix}. \quad (2)$$

The entries of \mathbf{R} and \mathbf{L} can be found directly from the short-circuit test data.

For a three-phase transformer, the governing equation is the same as (1), except each entry of \mathbf{R} and \mathbf{L} matrices is a 3×3 submatrix, i.e., \mathbf{R}_p and \mathbf{L}_{pq} , ($p, q = 1, 2, \dots, n$) given by

$$\mathbf{R}_p = \begin{bmatrix} R_{pa} & 0 & 0 \\ 0 & R_{pb} & 0 \\ 0 & 0 & R_{pc} \end{bmatrix}, \mathbf{L}_{pq} = \begin{bmatrix} L_{paqa} & L_{paqb} & L_{paqc} \\ L_{pbqa} & L_{pbqb} & L_{pbqc} \\ L_{pcqa} & L_{pcqb} & L_{pcqc} \end{bmatrix} \quad (3)$$

where a , b , and c stand for the three phases.

Using the trapezoidal rule to discretize (1), the discrete-time difference equation is given by

$$\mathbf{i}_T(t) = \mathbf{G}\mathbf{v}_T(t) + \mathbf{hist}(t - \Delta t) \quad (4)$$

where Δt is the simulation time step, with $\mathbf{hist}(t - \Delta t)$ being the $n \times 1$ vector containing history terms, which is given by

$$\mathbf{hist}(t - \Delta t) = \mathbf{H}\mathbf{v}_T(t - \Delta t) + (\mathbf{I} - 2\mathbf{G}\mathbf{R})\mathbf{hist}(t - 2\Delta t) \quad (5)$$

$$\mathbf{H} = 2(\mathbf{G} - \mathbf{G}\mathbf{R}\mathbf{G}) \quad (6)$$

$$\mathbf{G} = \left[\mathbf{I} + \frac{\Delta t}{2}\mathbf{L}^{-1}\mathbf{R} \right]^{-1} \frac{\Delta t}{2}\mathbf{L}^{-1} \quad (7)$$

with \mathbf{I} being the $n \times n$ identity matrix.

2) *Linear Module Hardware Design:* There are two main functions for this module: 1) calculate the history currents and send them to the linear solver; 2) save the updated history currents within this module to use them in the next iteration. The main control module sends a signal to this module to indicate which operation is to be executed.

As indicated by (5), the history current calculation can be carried out by matrix multiplication. A matrix vector multiplication (MVM) unit, which is part of the linear solver, has been developed for this purpose. Since the entries in \mathbf{R} , \mathbf{L} , \mathbf{G} , and \mathbf{H} are the properties of the transformer, which are unchanged, these parameters can be saved in memory before the real-time simulation begins. Furthermore, instead of saving \mathbf{R} and \mathbf{L} individually, the result of $2(\mathbf{G} - \mathbf{G}\mathbf{R}\mathbf{G})$ and $(\mathbf{I} - 2\mathbf{G}\mathbf{R})$ can be saved as \mathbf{H} and \mathbf{IGR} in the memory, respectively, to further reduce the computational complexity and latency. The matrix storage format consists of two RAMs defined to store the precalculated transformer matrices: a 32-bit RAM val , which stores the matrix entities row-wise, and a 9-bit RAM, consisting of the last 8-bit cid to store the column indexes and the first bit

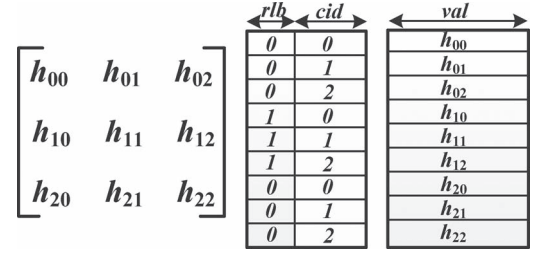
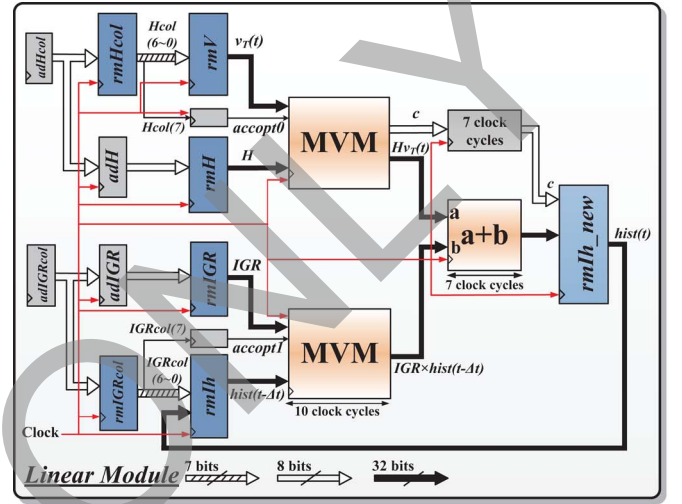
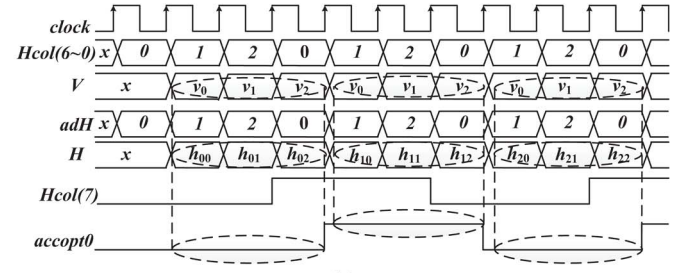


Fig. 4. Example matrix and its storage format.



(a)



(b)

Fig. 5. Pipelined scheme for the linear module. (a) Hardware design. (b) Timing diagram.

rlb to label the same row entities with “0” or “1.” Fig. 4 shows an example matrix and its storage format.

In Fig. 5(a), the RAMs ($rmHcol$, rmH , $rmIGRcol$, and IGR) containing the transformer parameters are generated by the aforementioned rule, and rmV stores the transformer nodal voltages calculated by the nonlinear solver, whereas $rmIh$ stores the history current terms calculated in the previous time step. When the linear module executes the updated function, the aforementioned memory devices are accessed sequentially by $adHcol$, adH , $adIGRcol$, and $adIGR$, and the data are sent to the MVM function unit. The timing diagram of this operation is shown in Fig. 5(b).

As shown in Fig. 6(a), the MVM hardware unit is comprised of one floating-point multiplier, one floating-to-fixed-point converter, one fixed-to-floating-point converter, and two fixed-point adders. The reason for a fixed-point adder in this module is that the floating-point adder needs much more logic resources and a higher clock latency, although the fixed-point adder only

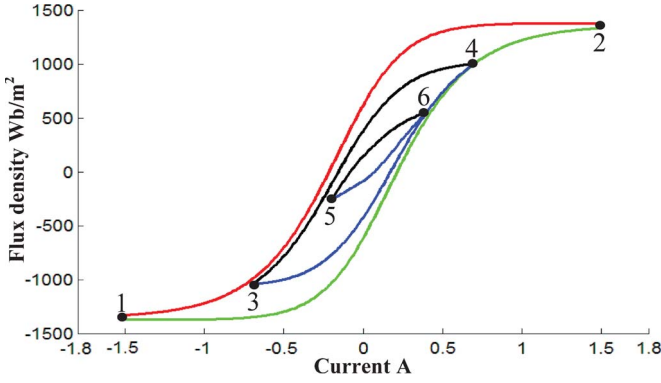


Fig. 9. Hysteresis characteristic with major and minor loops.

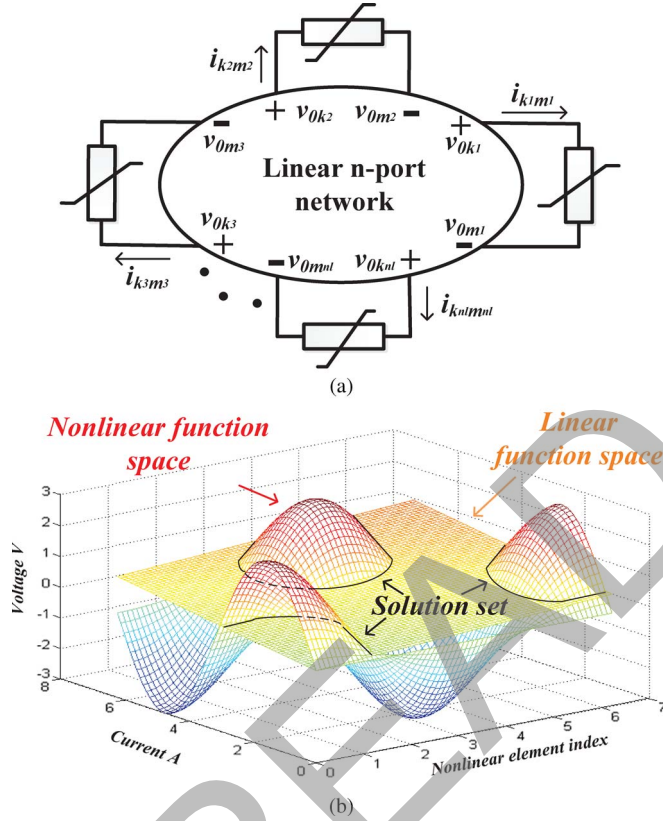


Fig. 10. (a) Linear network with external nonlinear elements. (b) Compensation method demonstration for multiple nonlinearities.

where \mathbf{Y} is the $n \times n$ admittance matrix without nonlinear elements; \mathbf{v}_0 and \mathbf{i} are $n \times 1$ vectors of unknown nodal voltages and known nodal currents, respectively, which are expressed as $\mathbf{v}_0 = [v_{01}(t) \ v_{02}(t) \ \dots \ v_{0n}(t)]^T$ and $\mathbf{i} = [i_1(t) \ i_2(t) \ \dots \ i_n(t)]^T$.

For the solution of the nonlinear part, the compensation method is employed. After the linear solution of a network is found, an n -node power system with n_l nonlinear elements is solved, as illustrated in Fig. 10(b) and in

$$\mathbf{f}(\mathbf{i}_{km}) = \mathbf{v}_{\text{open}} - \mathbf{r}_{\text{thev}} \mathbf{i}_{km} \quad (9)$$

where \mathbf{v}_{open} is the $n_l \times 1$ open-circuit voltage vector (a subset of \mathbf{v}_0) without the nonlinear elements, and \mathbf{i}_{km} is the $n_l \times 1$ nonlinear element current injection vector with k_l and

$m_l (l = 1, 2, \dots, n_l)$ being the node indexes to which the nonlinear elements are connected, which are expressed as

$$\mathbf{v}_{\text{open}} = [v_{0k_1}(t) - v_{0m_1}(t) \ v_{0k_2}(t) - v_{0m_2}(t) \ \dots \ v_{0k_{n_l}}(t) - v_{0m_{n_l}}(t)]^T \quad (10)$$

$$\mathbf{i}_{km} = [i_{k_1 m_1}(t) \ i_{k_2 m_2}(t) \ \dots \ i_{k_{n_l} m_{n_l}}(t)]^T. \quad (11)$$

\mathbf{r}_{thev} is the $n_l \times n_l$ Thevenin equivalent resistance matrix that can be found from \mathbf{Y} , and $\mathbf{f}(\mathbf{i}_{km})$ are the nonlinear functions. The intersection of linear and nonlinear spaces is the set of solution \mathbf{i}_{km} , as shown in Fig. 10(b). In the proposed module, these nonlinear functions are generated either by a five-segment piecewise nonlinear function to represent the saturation effect or the Preisach model, as detailed in the next section, to represent both of the saturation and the hysteresis effect. Equation (9) is solved simultaneously for \mathbf{i}_{km} using the N-R iteration. Linearizing (9) using the N-R iteration results in the following equation:

$$\mathbf{J}(\mathbf{i}_{km}^{j+1} - \mathbf{i}_{km}^j) = -\mathbf{F}(\mathbf{i}_{km}^j) \quad (12)$$

where \mathbf{J} is the Jacobian matrix; \mathbf{i}_{km}^{j+1} and \mathbf{i}_{km}^j are the current vectors at the $(j+1)$ th and j th iterations, respectively. \mathbf{J} and \mathbf{F} can be computed as

$$\begin{cases} \mathbf{J} = \frac{\partial \mathbf{F}(\mathbf{i}_{km}^j)}{\partial \mathbf{i}_{km}^j} = \mathbf{r}_{\text{thev}} + \frac{\partial \mathbf{f}(\mathbf{i}_{km}^j)}{\partial \mathbf{i}_{km}^j} \\ -\mathbf{F} = \mathbf{v}_{\text{open}} - \mathbf{r}_{\text{thev}} \mathbf{i}_{km} - \mathbf{f}(\mathbf{i}_{km}^j). \end{cases} \quad (13)$$

The convergence conditions, with small enough values of ϵ_1 and ϵ_2 , are defined as

$$\|\mathbf{i}_{km}^{j+1} - \mathbf{i}_{km}^j\| < \epsilon_1 \text{ and } \|\mathbf{F}(\mathbf{i}_{km}^j)\| < \epsilon_2. \quad (14)$$

The final network solution is found by superimposing the response of \mathbf{i}_{km} on the linear network solution

$$\mathbf{v} = \mathbf{v}_0 - \mathbf{R}_{\text{Thev}} \mathbf{i}_{km} \quad (15)$$

where \mathbf{v} is the $n \times 1$ node voltage vector with nonlinear branches, which is expressed as $\mathbf{v} = [v_1 \ v_2 \ \dots \ v_n]^T$, and \mathbf{R}_{Thev} is an $n \times n_l$ matrix obtained from \mathbf{Y} .

For example, for the nonlinear inductance, the characteristic function is provided in the form

$$\lambda(t) = \mathbf{f}_\lambda(\mathbf{i}_{km}(t)) \quad (16)$$

where the flux $\lambda(t)$ is the integral of node voltage over a time step, i.e.,

$$\lambda(t) = \lambda(t - \Delta t) + \int_{t-\Delta t}^t \mathbf{v}'(u) du. \quad (17)$$

Applying the trapezoidal rule results in

$$\lambda(t) = \frac{\Delta t}{2} \mathbf{v}'(t) + \lambda_{\text{hist}}(t - \Delta t) \quad (18)$$

where

$$\lambda_{\text{hist}}(t - \Delta t) = \lambda(t - \Delta t) + \frac{\Delta t}{2} \mathbf{v}'(t - \Delta t). \quad (19)$$

From (18) and (16), the set of nonlinear equations to determine i_{km} is given by

$$\mathbf{F}_\lambda \equiv \frac{2}{\Delta t} [\mathbf{f}_\lambda(i_{km}(t)) - \lambda_{\text{hist}}(t - \Delta t)] - \mathbf{v}_{\text{open}}(t) + \mathbf{r}_{\text{thev}} i_{km}(t). \quad (20)$$

Then, the Jacobian matrix and the nonlinear equations for this case can be rewritten as

$$\begin{cases} \mathbf{J}_\lambda = \frac{\mathbf{F}_\lambda(i_{km}^j(t))}{i_{km}^j(t)} = \mathbf{r}_{\text{thev}} + \frac{\mathbf{f}_\lambda(i_{km}^j(t))}{i_{km}^j(t)} \frac{2}{\Delta t} \\ -\mathbf{F}_\lambda = \mathbf{v}_{\text{open}}(t) - \mathbf{r}_{\text{thev}} i_{km}^j(t) - [\mathbf{f}_\lambda(i_{km}^j(t)) - \lambda_{\text{hist}}(t - \Delta t)] \frac{2}{\Delta t}. \end{cases} \quad (21)$$

2) PHU: The major loop hysteresis function is geometrically represented by the following hyperbolic function [26]:

$$\lambda_{p_m}(i_{km}) = \frac{1}{2} \sum_{u=1}^3 a_u [\tanh(b_u i_{km}) + c_u \sec h^2(b_u i_{km})] \quad (22)$$

where a_u , b_u , and c_u are the parameters to define this hyperbolic template; i_{km} is the current value vector flowing through the nonlinear inductances as before; and $\lambda_{p_m} = [\lambda_{p_m1} \ \lambda_{p_m2} \ \dots \ \lambda_{p_mn_l}]^T$ is the flux density corresponding to this current value vector on the major loop. The subscript “p_m” stands for Preisach major loop.

Once the major loop function is fixed, all the minor loop trajectories from a reversal point follow this uniform template. The reversal point can be captured when $\lambda_{p_ml}(t + \Delta t) > \lambda_{p_ml}(t)$ on a downward trajectory, or when $\lambda_{p_ml}(t + \Delta t) < \lambda_{p_ml}(t)$ on an upward trajectory ($l = 1, 2, \dots, n_l$). In general, Preisach upward and downward trajectories from a reversal point (i_{rl}, λ_{rl}) can be expressed as (23) and (24), respectively [27], where $i_r = [i_{r1} \ i_{r2} \ \dots \ i_{rn_l}]$ and $\lambda_r = [\lambda_{r1} \ \lambda_{r2} \ \dots \ \lambda_{rn_l}]$. The reversal points need to be recorded in a reversal point stack (RPS), while traveling the hysteresis loop; for example, when flux density starts increasing from point 5 and reaches point 6, the trajectory beyond the reversal point 6 is defined by the template beginning at point 3, as shown in Fig. 9. Thus, if the flux density increases or decreases out of the outer loop, the last two coordinates in the stack are removed. This example is initialized by saving the two major loop reversal points (1 and 2) in the stack; these two points cannot be removed since all the trajectories cannot be beyond the major loop, as illustrated in Fig. 11. The trajectory is processed by going through the following reversal points: 1–4–3–6–5, with the corresponding stack shown in Fig. 11(a). Once the trajectory increases beyond point 6, the reversal points 5 and 6 are removed due to the reason previously discussed, as shown in Fig. 11(b). The flux density trajectories corresponding to the instantaneous current in an upward λ_{p_u} minor loop or a downward λ_{p_d} minor loop are given by

$$\lambda_{p_u}(i_{km}) = -\lambda_{p_m}(-i_{km}) - \lambda_{p_m}(i_r) + \lambda_r + 2\mathbf{K}(-i_r)\mathbf{K}(i_{km}) \quad (23)$$

$$\lambda_{p_d}(i_{km}) = \lambda_{p_m}(i_{km}) + \lambda_{p_m}(-i_r) + \lambda_r - 2\mathbf{K}(i_r)\mathbf{K}(-i_{km}) \quad (24)$$

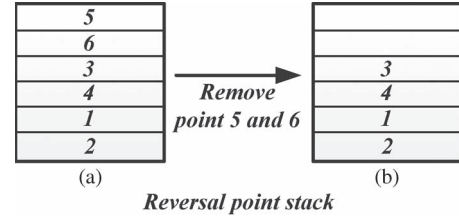


Fig. 11. Corresponding RPS (a) before and (b) after current increasing beyond the point 6.

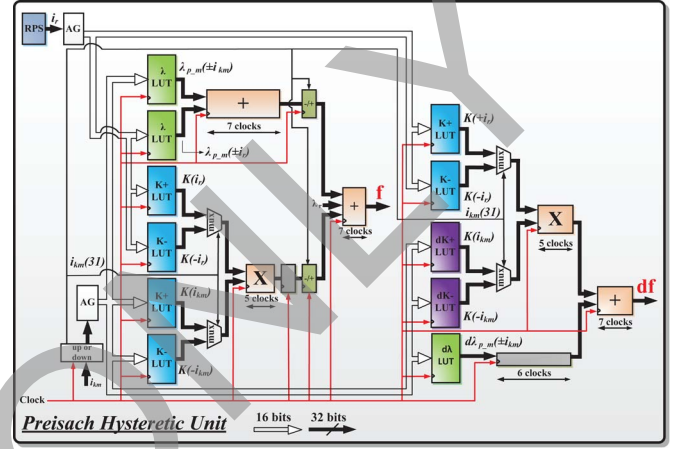


Fig. 12. PHU hardware design.

where

$$\mathbf{K} = [K_1 \ K_2 \ \dots \ K_{n_l}]$$

$$K_l(x) = \begin{cases} \sqrt{\lambda_{p_m}(-x)}, & x < 0 \\ \frac{\lambda_{p_m}(-x) + \lambda_{p_m}(x)}{2\sqrt{\lambda_{p_m}(x)}}, & x > 0 \end{cases}$$

$$l = 1, 2, \dots, n_l.$$

The functions $d/di_{km} \lambda_{p_u}(i_{km})$ and $d/di_{km} \lambda_{p_d}(i_{km})$ for upward and downward trajectories, respectively, can be expressed as

$$\frac{d}{di_{km}} \lambda_{p_u}(i_{km}) = d\lambda_{p_m}(-i_{km}) + 2\mathbf{K}(-i_r)d\mathbf{K}(i_{km}) \quad (25)$$

$$\frac{d}{di_{km}} \lambda_{p_d}(i_{km}) = d\lambda_{p_m}(i_{km}) + 2\mathbf{K}(i_r)d\mathbf{K}(-i_{km}). \quad (26)$$

Substituting (23) and (24) into (16), the Jacobian matrix can be computed by (21) using the differentials (25) and (26).

Nonlinear Module Hardware Design: Several hardware implementations are available, such as COordinate Rotation Digital Computer (CORDIC), to evaluate the nonlinear functions required in the N-R iteration. However, since the number of iterations executed is unknown, the computational burden and latency could be too high to achieve real-time execution. In the PHU, lookup tables (LUTs) are employed instead to compute the nonlinear functions.

As shown in Fig. 12, taking the advantage of parallelism of logic resources, the function $f(i_{km})$ and $d/di_{km} f(i_{km})$ can be evaluated simultaneously. The address generator (AG)

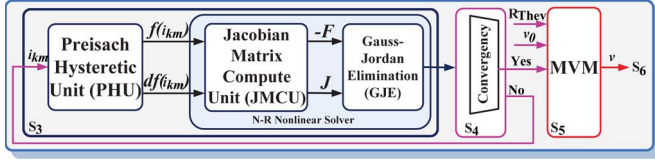


Fig. 13. Overall nonlinear module hardware architecture.

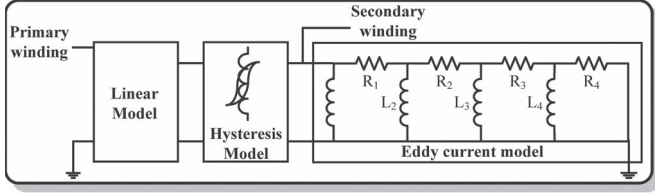


Fig. 14. Cauer equivalent circuit for the frequency-dependent eddy current model.

functional unit is used to convert the 32-bit floating-point i_{km} into integer numbers to address the LUTs. Equations (23)–(26) show that function $f(i_{km})$ and $d/i_{km}f(i_{km})$ can be evaluated with i_{km} or $-i_{km}$, i_r or $-i_r$, depending on the trajectory direction. Therefore, before i_{km} is input into the AG unit, its trajectory direction must be known. In addition, since the function $K(i_{km})$ is dependent on the sign of i_{km} (25), two $K(i_{km})$ LUTs ($K+$, $K-$) are precalculated, and the first bit of i_{km} (or $-i_{km}$) determines which value is involved in the calculation by using a multiplexer *mux*.

As shown in Fig. 13, after finding the values of $f(i_{km})$ and $d/i_{km}f(i_{km})$, the function Jacobian matrix compute unit (JMCU) computes the values of $-F$ and J , as given in (21), and then, the Gauss–Jordan elimination (GJE) unit is used to solve the algebraic equation (12). If the calculated i_{km} satisfies (14), then i_{km} is used to compensate the voltage v_0 to find the final result v (15). If the i_{km} has not converged, then it is used as an input for the next iteration until convergence or the maximum number of iterations is reached.

C. Frequency-Dependent Eddy Current Model

Eddy currents, a part of the transformer core losses, are induced by the change in the magnetic field. While they can be reduced by using a laminated core, previous works indicate that eddy current losses are frequency dependent. However, in transformer transient models, commonly, the eddy current phenomena are represented by a constant resistance in parallel with the magnetizing inductance. Thus, this representation is invalid over a wide frequency range.

A Cauer equivalent circuit has been developed to represent the frequency dependence as a cascade of RL lumped sections (see Fig. 14). The accuracy of this model over a wide frequency range depends on the number of RL sections. Four sections are required to represent the frequency up to 200 kHz with an error of less than 5% [25].

The parameters of the Cauer model can be derived as

$$\begin{aligned} L_0 &= \frac{N^2 A \mu}{l} \quad \text{and} \quad L_k = \frac{L_0}{(4k-3)} \\ R_0 &= \frac{4N^2 A}{ld^2 \gamma} \quad \text{and} \quad R_k = R_0(4k-1). \end{aligned} \quad (27)$$

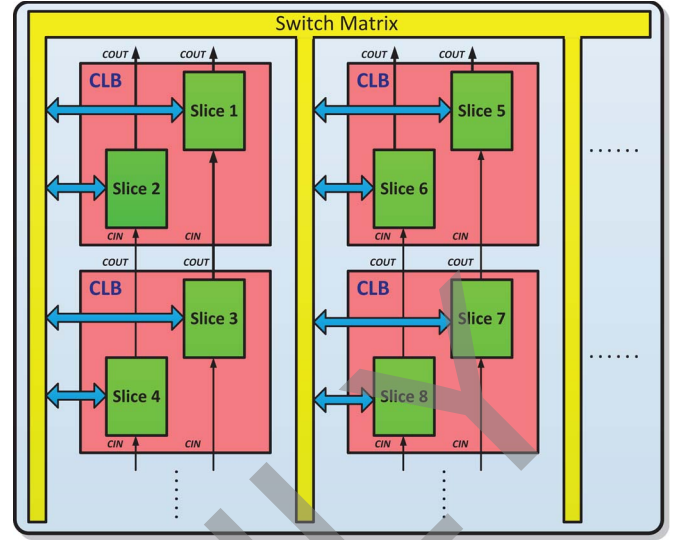


Fig. 15. Virtex-7 FPGA architecture.

The symbols μ , γ , A , d , l , and N stand for the magnetic permeability of the steel lamination, the electrical conductivity of the steel lamination, the total cross-sectional area of all laminations, the thickness of the lamination, the length of the core limb, and the number of coil turns, respectively.

The overall frequency-dependent nonlinear hysteretic transformer model is shown in Fig. 14.

III. CASE STUDY AND EXPERIMENTAL RESULTS

A. Experimental Setup

The real-time nonlinear hysteretic transformer EMT model is implemented on the Xilinx Virtex-7 VC707 XC7VX485T FPGA, which is featured as following: 485-K logic cells, 37-Mbit block RAMs, 2800 DSP slices, and 700 user input/output pins. User design functionality can be realized by configurable logic blocks (CLBs) and DSP slices. As shown in Fig. 15, each CLB contains two slices, and each slice is composed of four 6-input LUTs, eight flip-flops, multiplexers, and arithmetic carry logic. The two slices in each CLB are not connected, and each CLB, as well as each slice, is organized as a column. In each column, the slice is connected by an independent carry chain. A switch matrix connected to all slices is for accessing to the general routing matrix purpose. As shown in Fig. 16, the Virtex-7 FPGA outputs the real-time simulation results to a digital-to-analog converter (DAC) board through an FPGA Mezzanine Card (FMC) connector integrated on the board, and an FMC-to-DAC adapter, and the real-time data are captured by an oscilloscope. The Chipscope is a convenient tool provided by ISE software to visualize data. This tool can be used to analyze short transient periods; however, due to the limitation of the sampling number (up to 131 072), this tool cannot be used to trace the waveforms. The overall logic elements utilized by the nonlinear transformer model is 15%. The real-time simulation was carried out with a time step of 10 μ s on the FPGA input clock frequency of 100 MHz. The breakdown of model latencies in one simulation time step is shown in Fig. 17. The execution time for one time step is

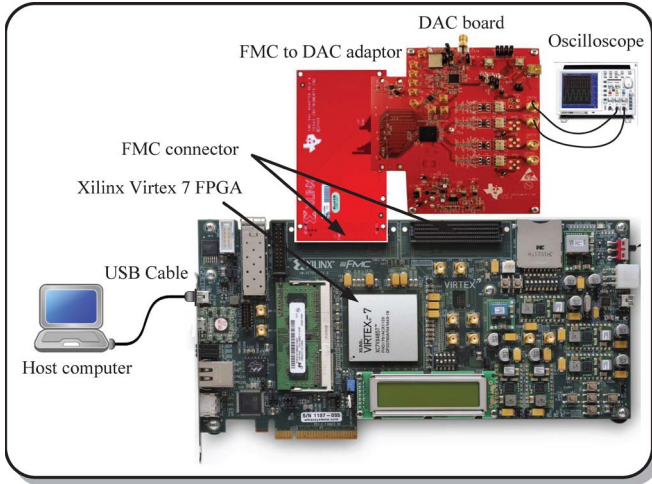


Fig. 16. Experimental setup.

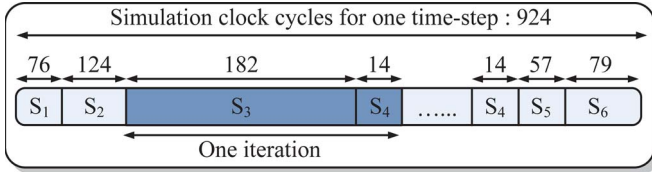


Fig. 17. Model latencies for one time step.

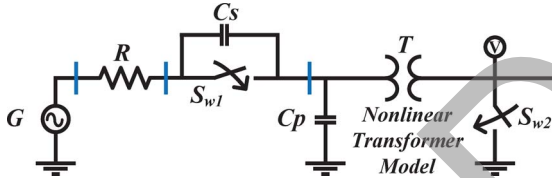


Fig. 18. Single-line diagram for case study I.

9.24 μs , with a maximum of three Newton iterations per time step. This means that, within a 50- μs time step, which is the acceptable time step for real-time transient simulation, this FPGA-based nonlinear transformer model can simulate five nonlinear transformers in real time with very small hardware resource consumption. Increasing the hardware utility or the clock frequency, it is also possible to simulate a larger power system with more transformer models, including the nonlinear and frequency-dependent phenomena.

B. Case Study I

Two power systems are studied to show the effectiveness and accuracy of the proposed FPGA-based real-time nonlinear transformer model. Fig. 18 shows the first case study: single-line diagram of a three-phase system. A transformer T is connected to a voltage source G through a circuit breaker S_{w1} . C_s is the breaker's grading capacitance, and C_p is the phase-to-earth capacitance, including transformer winding capacitance. The system data are listed in the Appendix. The real-time simulation results are validated by off-line software ATP.

1) *Inrush Current Transients*: In this inrush-current-transient case study, capacitors C_s and C_p are removed in Fig. 18, and a five-segment piecewise nonlinear function is employed to represent the saturation effect. When the breaker

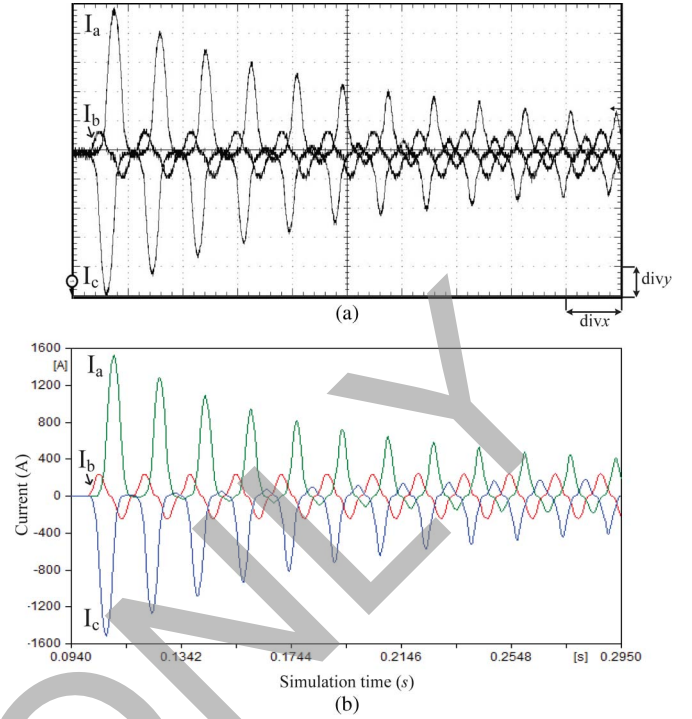


Fig. 19. Breaker current when the breaker closed at $t = 0$ s. (a) Real-time simulation results (1 div $x = 20$ ms; 1 div $y = 320$ A). (b) Off-line (ATP) simulation results.

S_{w1} is closed at 0.1 s, the real-time-captured three-phase breaker current waveforms are shown in Fig. 19(a). As shown in these waveforms, phases a and c have larger current amplitude, whereas the amplitude of phase b current is relatively small. These unbalanced current waveforms are caused due to the instantaneous voltage supply values being different in various phases when the breaker S_{w1} is closed. The peak magnitude inrush current value of phases a and c is 210% of the transformer rated current, and it decays to the steady state after 0.6 s. Similar inrush current behavior can be seen in the ATP off-line simulation results in Fig. 19(b).

2) *Hysteresis Behavior*: To investigate the hysteresis behavior in the magnetizing core, the PHU is used to model the saturation and hysteresis during the inrush current transient. The parameters to define the hysteresis trajectory are listed in the Appendix. The initial flux in the core is set on the downward major loop trajectory. Fig. 20 shows the real-time simulation results for the flux and magnetizing current of the nonlinear transformer. From $t = 0$ to 0.106 s, the power system is energized from a voltage source at a value of 0.65 p.u. As shown in Fig. 20, during the first cycle (1–2), the flux is nonsymmetrical due to the initial remanent flux, and the peak flux value is 1 p.u. After the first cycle, the flux is symmetrical and travels on the minor loop since the value of voltage is not high enough to drive the transformer working in the saturation region (3–4). From $t = 0.106$ to 0.15 s, the breaker is opened and the flux is locked at 0.62 p.u. From $t = 0.15$ s, the voltage rises to 1.25 p.u. and the breaker is reclosed, when the peak flux value reaches 1.25 p.u., and the high voltage value drives the flux into the saturation region, travelling on the major loop (5–6).

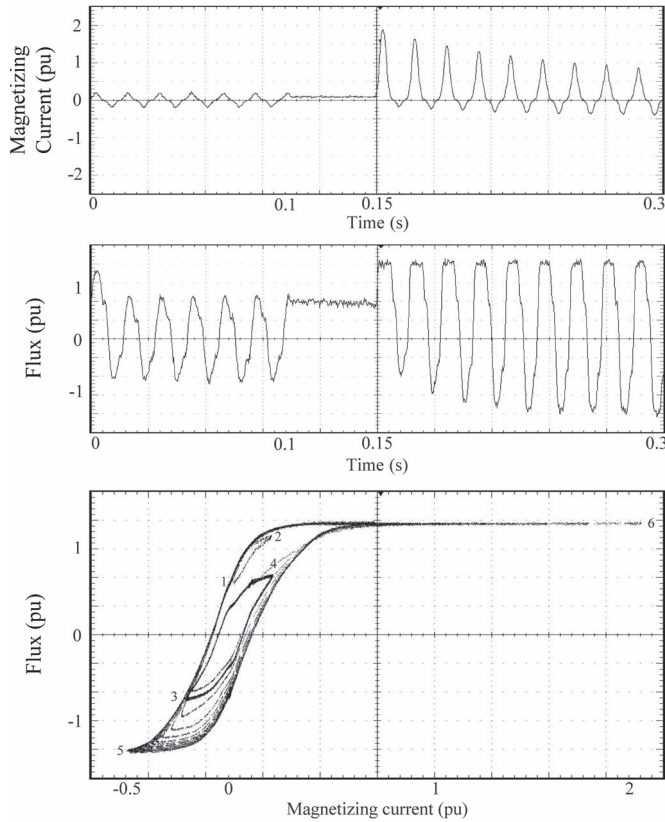


Fig. 20. Real-time simulation results for the flux, magnetizing current, and the hysteresis characteristic of the nonlinear transformer.

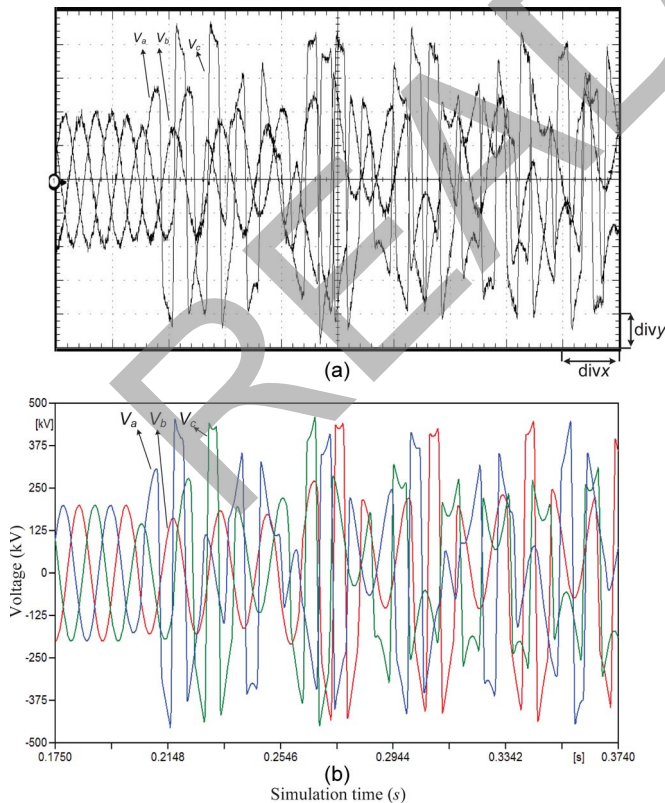


Fig. 21. Primary-side three-phase voltages when the breaker opened at $t = 0.2$ s. (a) Real-time simulation results (1 div $x = 20$ ms; 1 div $y = 100$ kV). (b) Off-line (ATP) simulation results.

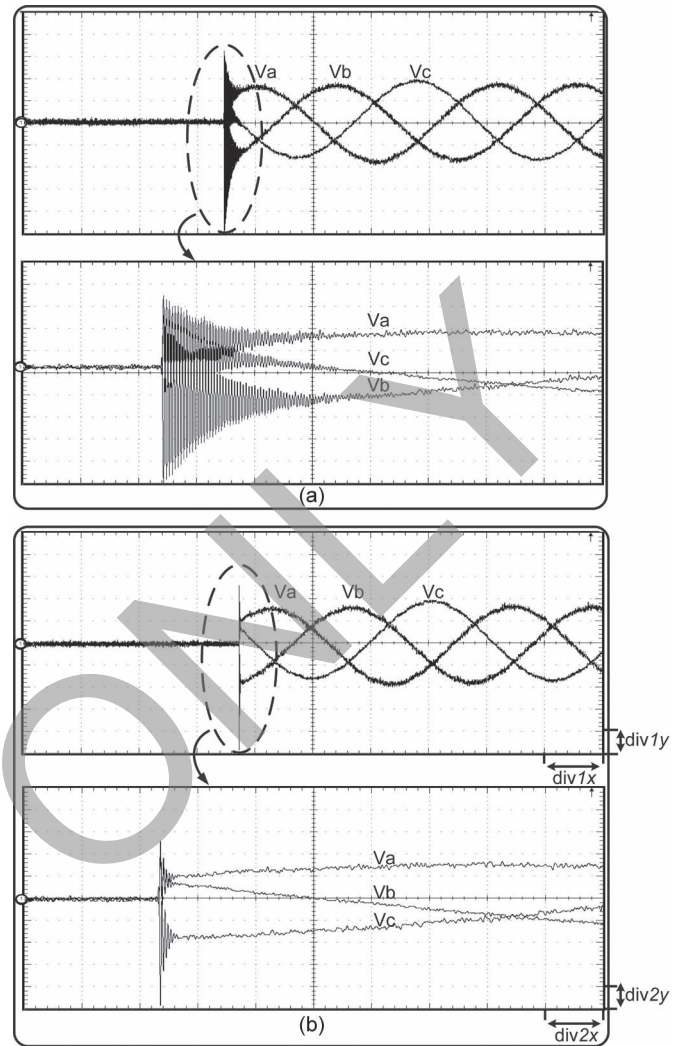


Fig. 22. TRV real-time simulation results at $t = 0.2$ s. (a) Cauer model. (b) Non-frequency-dependent model (constant resistor) (1 div $1x = 4$ ms; 1 div $1y = 84$ kV; 1 div $2x = 400$ μ s; 1 div $2y = 84$ kV).

3) *Ferroresonance Transients*: Ferroresonance is an electrical phenomenon, which can occur when a nonlinear inductance is fed from a sinusoidal source. It can cause overvoltages and overcurrents in the system, with the subsequent risk of damage to equipment. In Fig. 21, after opening S_{w1} while the breaker S_{w2} is closed at $t = 0.2$ s to simulate a three-phase ground fault, the voltage waveforms are highly distorted and have a higher peak value of 220% of the steady-state voltage value. Again, similar voltage behavior can be observed in the off-line simulation results in Fig. 21(b).

4) *Eddy Current Transient*: Transient recovery voltages (TRVs) manifest across any circuit breaker in power systems during fault clearance. This case study is initialized by closing S_{w2} to cause a ground fault and then reopening S_{w2} to clear this fault. The real-time simulation results of voltage across S_{w2} by using two different models, i.e., a Cauer equivalent circuit and a constant resistor, are captured. As shown in Fig. 22, the Cauer model simulation result shows a higher peak value and much longer damping time than that with a constant resistor model, this implies that the eddy currents increase the power losses in the transformer during the transient recovery period.

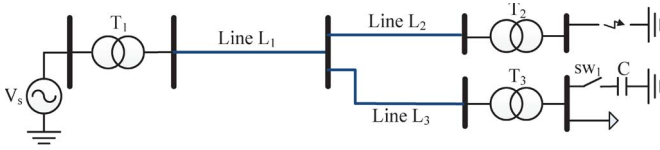
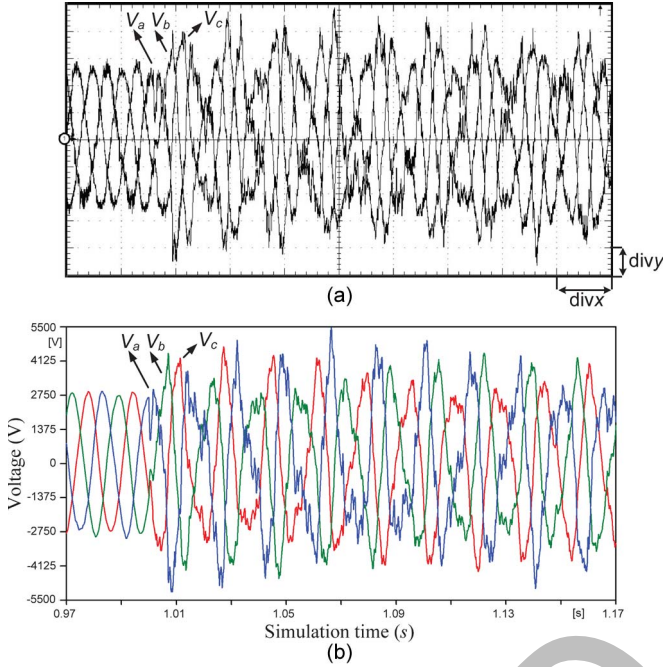


Fig. 23. Single-line diagram for case study II.

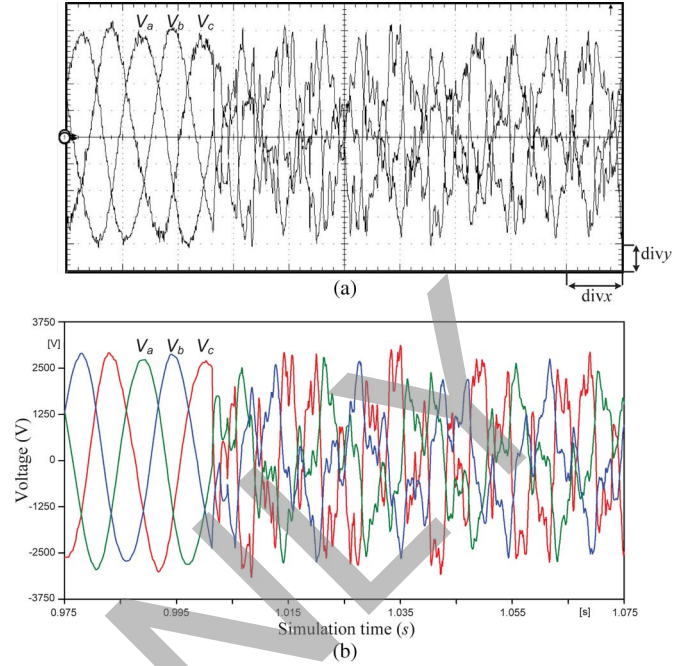
Fig. 24. Capacitor switch at $t = 1$ s. (a) Real-time simulation results (1 div $x = 10$ ms; 1 div $y = 1.06$ kV). (b) Off-line (ATP) simulation results.

C. Case Study II

In the second case study (see Fig. 23), the studied power system involves: 1) three transformers (T_1, T_2, T_3), all of them employing the full nonlinear modeling; 2) three transmission lines (L_1, L_2, L_3), which are modeled using a distributed parameter line model (Bergeron's model); 3) one ideal voltage source (V_s); 4) one switch (SW_1) and a capacitor C are used to model the capacitor switching. The parameters for this case study are also listed in the Appendix.

1) *Capacitor Switching Transients*: The entire power system is energized until $t = 1$ s, when the capacitor switching is initiated by closing SW_1 . Both real-time and off-line simulation results are captured to show the primary winding voltages at transformer T_3 (see Fig. 24). From the waveforms, after closing the switch, the voltage dropped to zero because the voltage of the capacitor at the secondary winding of this transformer cannot change immediately, and then, a fast voltage recovery is observed. The distorted recovery voltage is a maximum of 150% of the steady-state voltage value, and it decays to the steady state after 3 s.

2) *Ground Fault Transients*: This case study is achieved by initiating a three-phase-to-ground fault at $t = 1$ s at the secondary winding of transformer T_2 , and the voltage waveforms at the primary winding of transformer T_3 are captured in both real-time and off-line simulation results, as shown in Fig. 25. Compared with capacitor switching transients, the ground fault

Fig. 25. Ground fault at $t = 1$ s. (a) Real-time simulation results (1 div $x = 20$ ms; 1 div $y = 1.5$ kV). (b) Off-line (ATP) simulation results

transients behave in a highly distorted fashion; however, there is no overshoot in voltage, and the steady state is achieved after 4 s.

IV. CONCLUSION

A nonlinear hysteretic power transformer hardware model has been developed in real time on the FPGA. Taking the natural advantages of the hardwired architecture, parallelism, as well as pipelining, enabled us to achieve real-time simulation. This hardware power transformer model has the following features: linear model to update the history current terms; nonlinear phenomena, such as hysteresis, are included with a Newton iteration for solving the nonlinear equations; the Preisach model was used to define the hysteretic loop; and a frequency-dependent equivalent circuit was used to model the eddy current behavior. Two case studies have been analyzed to show the accuracy and efficiency of this proposed model under various transient conditions. The hardware utility and simulation time show that the FPGA-based model can still realize real-time simulation even if the power system is large.

APPENDIX

- I. Parameters of case study I, Inrush Current Transient: Three-phase Transformer T : 250 MVA, 200 kV/400 kV, Y-Y connection; Voltage source G : 20 kV; Resistance R : 1 Ω .
- II. Parameters of case study I, Ferroresonance and Eddy Current Transients: Three-phase Transformer T : 250 MVA, 125 kV/500 kV, Y-Y connection; Voltage source G : 50 kV; Capacitance C_s, C_p : 0.05 μ F, 0.0125 μ F; Resistance R : 500 Ω .
- III. Parameters of case study II: Three-phase Y-Y Transformers T_1, T_2, T_3 : 20 MVA, 15 kV/35 kV, 32 kV/14 kV, 32 kV/20 kV; Transmission line inductance: mode +: 1.556 mH/m,

mode 0: 5.819 mH/m; Transmission line capacitance: mode +: 0.0194 μ F/m, mode 0: 0.0120 μ F/m; Transmission line L1, L2, L3: 120 m, 140 m, 180 m.

- IV. Parameters of hysteresis trajectory: $a_1 = 0.7900$; $a_2 = 0.2430$; $a_3 = 200$; $b_1 = 0.0186$; $b_2 = 1.1236$; $b_3 = 0.0105$; $c_1 = 0.0214$; $c_2 = 0.5736$; $c_3 = 0.5203$.

REFERENCES

- [1] E. Monmasson, L. Idkhajine, M. N. Cirstea, I. Bahri, A. Tisan, and M. W. Naouar, "FPGAs in industrial control applications," *IEEE Trans. Ind. Informat.*, vol. 7, no. 2, pp. 224–243, May 2011.
- [2] T. J. Vyncke, S. Thielemans, and J. A. Melkebeek, "Finite-set model-based predictive control for flying-capacitor converters: Cost function design and efficient FPGA implementation," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1113–1121, May 2013.
- [3] H. Guo, H. Chen, F. Xu, F. Wang, and G. Lu, "Implementation of EKF for vehicle velocities estimation on FPGA," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3823–3835, Sep. 2013.
- [4] S. Kuo-Kai, C. Yun-Jen, L. Po-Lei, L. Ming-Huan, S. Jyun-Jie, W. Chi-Hsun, W. Yu-Te, and T. Pi-Cheng, "Total design of an FPGA-based brain-computer interface control hospital bed nursing system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2731–2739, Jul. 2013.
- [5] M. Curkovic, K. Jezernik, and R. Horvat, "FPGA-based predictive sliding mode controller of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 637–644, Feb. 2013.
- [6] Y. Chen and V. Dinavahi, "Multi-FPGA digital hardware design for detailed large-scale real-time electromagnetic transient simulation of power systems," *IET Gen., Transm., & Distrib.*, vol. 7, no. 5, pp. 451–463, May 2013.
- [7] A. Myaing and V. Dinavahi, "FPGA-based real-time emulation of power electronic systems with detailed representation of device characteristics," *IEEE Trans. on Industrial Electronics*, vol. 58, no. 1, pp. 358–368, Jan. 2011.
- [8] O. Lucia, L. A. Barragan, J. M. Burdio, O. Jimenez, D. Navarro, and I. Urriza, "A versatile power electronics test-bench architecture applied to domestic induction heating," *IEEE Trans. on Ind. Electron.*, vol. 58, no. 3, pp. 998–1007, Mar. 2011.
- [9] Y. Chen and V. Dinavahi, "Digital hardware emulation of universal machine and universal line models for real-time electromagnetic transient simulation," *IEEE Trans. on Industrial Electronics*, vol. 59, no. 2, pp. 1300–1309, Feb. 2012.
- [10] D. Majstorovic, I. Celanovic, N. D. Teslic, N. Celanovic, and V. A. Katic, "Ultralow-latency hardware-in-the-loop platform for rapid validation of power electronics designs," *IEEE Trans. on Ind. Electron.*, vol. 58, no. 10, pp. 4708–4816, Oct. 2011.
- [11] Y. Chen and V. Dinavahi, "FPGA-based real-time EMTF," *IEEE Trans. on Power Delivery*, vol. 24, no. 2, pp. 892–902, Apr. 2009.
- [12] Y. Chen and V. Dinavahi, "An iterative real-time nonlinear electromagnetic transient solver on FPGA," *IEEE Trans. on Industrial Electronics*, vol. 58, no. 6, pp. 2547–2555, Jun. 2011.
- [13] E. Adzic, M. Adzic, V. Katic, D. Marcetic, and N. Celanovic, "Development of high-reliability EV and HEV IM propulsion drive with ultra-low latency HIL environment," *IEEE Trans. on Ind. Informat.*, vol. 9, no. 2, pp. 630–639, May 2013.
- [14] Y. Chen and V. Dinavahi, "Hardware emulation building blocks for real-time simulation of large-scale power grids," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 373–381, Feb. 2014.
- [15] J. A. Martinez and B. A. Mork, "Transformer modeling for low- and mid-frequency transients—A review," *IEEE Trans. Power Del.*, vol. 22, no. 2, pp. 1235–1246, Apr. 2007.
- [16] V. Brandwajn, H. W. Dommel, and I. Dommel, "Matrix representation of three-phase n-winding transformers for steady-state and transient studies," *IEEE Trans. Power App. Syst.*, vol. PAS-101, no. 6, pp. 1369–1378, Jun. 1982.
- [17] H. W. Dommel, *EMTP Theory Book*. Portland, OR: BPA, 1985.
- [18] W. Enright, O. B. Nayak, G. D. Irwin, and J. Arrillaga, "An electromagnetic transients model of multi-limb transformers using normalized core concept," in *Proc. Int. Conf. Power System Transients*, Seattle, WA, Jun. 1997, pp. 93–98.
- [19] H. W. Dommel, "Nonlinear and time-varying elements in digital simulation of electromagnetic transients," *IEEE Trans. on Power App. Syst.*, vol. 90, no. 4, pp. 2561–2567, Jun. 1971.
- [20] M. A. Coulson, R. D. Slater, and R. R. S. Simpson, "Representation of magnetic characteristic, including hysteresis, using Preisach's theory," in *Proc. of IEE*, Oct. 1977, vol. 124, no. 10, pp. 895–898.
- [21] F. Liorzou, B. Phelps, and D. L. Atherton, "Macroscopic models of magnetization," *IEEE Trans. on Magn.*, vol. 36, no. 2, pp. 418–428, Mar. 2000.
- [22] A. Rezaei-Zare, R. Iravani, M. Sanaye-Pasand, H. Mohseni, and S. Farhangi, "An accurate hysteresis model for ferroresonance analysis of a transformer," *IEEE Trans. on Power Del.*, vol. 23, no. 3, pp. 1448–1456, Jul. 2008.
- [23] E. J. Tarasiewicz, A. S. Morched, A. Narang, and E. P. Dick, "Frequency dependent eddy current models for nonlinear iron cores," *IEEE Trans. on Power Syst.*, vol. 8, no. 2, pp. 588–597, May 1993.
- [24] F. de Leon and A. Semlyen, "Time domain modeling of eddy current effects for transformer transients," *IEEE Trans. on Power Del.*, vol. 8, no. 1, pp. 271–280, Jan. 1993.
- [25] J. Avila-Rosales and A. Semlyen, "Iron core modeling for electrical transients," *IEEE Trans. on Power App. Syst.*, vol. PAS-104, no. 11, pp. 3189–3194, Nov. 1985.
- [26] I. D. Mayergoyz, *Mathematical Models of Hysteresis*. Berlin, Germany: Springer-Verlag, 1991.
- [27] S. R. Naidu, "Simulation of the hysteresis phenomenon using Preisach's theory," *Proc. Inst. Elect. Eng. A*, vol. 137, no. 2, pp. 73–79, Mar. 1990.



Jiadai Liu (S'11) received the B.Sc. degree in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2008 and the M.Eng. degree from the University of Windsor, Windsor, ON, Canada, in 2010. He is currently working toward the Ph.D. degree at the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada.

His research interests include detailed power system transient modeling and simulation, and field programmable gate arrays.



Venkata Dinavahi (S'94–M'00–SM'08) received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 2000.

He is a Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. His research interests include real-time simulation of power systems and power electronic systems, large-scale system simulation, and parallel and distributed computing.