Enabling Flexible Electronics: Demonstration of the Tunneling Junction Transistor (TJT) and Flexible Circuit Elements

by

Lhing Gem K. Shoute

A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy
in
Solid-State Electronics

Department of Electrical and Computer Engineering

University of Alberta

ABSTRACT

Thin-film technology continues to evolve as it finds new technological spaces to fulfill that will inevitably lead to an increased integration between society and technology. The aims of this research are to push beyond the limits of thin film electronics to enable a new era of flexible innovation. First, a self-oscillating energy harvesting boosting circuit was designed to understand the demands of a flexible circuit used in this prospective application. The electrical elements of the circuit which would practically and fundamentally inhibit its realization was closely examined and investigated. In particular, these were the inductor and the transistor. The problem of the inductor was approached by developing a design technique that will allow for an increased inductance without increasing its effective occupied area. The theoretical and realized workings of a fractal loop inductor is developed in this work.

Another major problem to address was the transistor. Before exploring the transistor, a fundamental component of the thin-film transistor (TFT) was investigated: the metal-oxide-semiconductor (MOS) structure, the region where the channel is formed. It is shown in this work that, unlike in bulk semiconductor MOS structures, for ultrathin active layers that are used in TFTs, traditional capacitance-voltage (CV) modeling does not accurately capture measured behavior. In order to do so, the assumption that the thickness of semiconductor is greater than the theoretical depletion width must be cast aside because it does not hold true for very thin-films. At ultra-thin dimensions, the geometry of the film plays a crucial part in the observed output CV behavior. Starting from the Schrödinger-Poisson self-consistent model, modifications from the traditional CV extraction methods were made that included both incorporating non-uniform dopant concentration and changes in the charge centroid within the semiconductor active film. The development of the model was crucial in estimating the behavior of the MOS interface for more complex structures that were required to increase the performance of a novel TFT architecture explored here.

An exploration of a novel TFT architecture was required because TFTs have been fundamentally limited to low power applications due to its reliance on unipolar current transport and thus far have only played the role of a simple switch in its commercial realization. In order to integrate TFTs in high fidelity circuits, its power handling capabilities must be improved by utilizing bipolar current transport which itself cannot be achieved conventionally in thin-film materials. As a proof-of-principle, we demonstrated a bipolar tunneling junction thin-film transistor (TJT) achieved with hole-assisted enhanced electron tunneling in a thin metal/HfO2/n-ZnO/p-Si tri-heterojunction modulated by a two-dimensional (2D) referred base. We began with initially exploring the nature of the enhanced tunneling current observed by combining the modified CV model with the Schrödinger-Poisson transfer matrix method. Unlike in previous MOS tunneling models that investigated polysilicon gates, the MOS structure that made up the tunneling emitter used a true metal. The model developed was adapted to take this account. It was found that the hole-assisted enhanced tunneling current was a result of an effective barrier thinning of the barrier oxide layer. This itself was a direct result of the probabilistic distribution of the tunneling electrons at metal penetrating the oxide due to the presence of holes at the inverted semiconductor.

A basic compact model for the TJT was also developed to predict the output of a well-behaved prototype and was experimentally supported. The resulting electrical characteristics of the device include a maximum current density of at least 45 $mA \cdot mm^{-1}$ at 3 V up to 115 $mA \cdot mm^{-1}$ at 10 V, the combination thereof currently unmatched by modern TFTs.

PREFACE

This thesis is an original work by Gem Shoute structured in the traditional format. The work in Chapter 2 is work based on a patent fully disclosed in Barlage, Douglas, and Lhing Gem Kim Shoute. "Frequency dependent analog boost converter for low voltage applications." U.S. Patent 9,397,561, issued July 19, 2016. Chapter 3 is based on the work published in Shoute, Gem, and Douglas W. Barlage. "Fractal loop inductors." *IEEE Transactions on Magnetics* 51.6 (2015): 1-8. Both Chapter 4 and 5 are the extended work of Shoute, G., Afshar, A., Muneshwar, T., Cadien, K., & Barlage, D. (2016). "Sustained hole inversion layer in a wide-bandgap metal-oxide semiconductor with enhanced tunnel current." *Nature Communications*, 7. The analytical and proceeding works described in the aforementioned chapters will be submitted in the near time after the completion of the thesis. My contributions to these studies include device fabrication, data collection, data analysis and manuscript preparation, all of which I carried out or lead. I also received support for this work and its overall from my supervisor, Professor D. W. Barlage. Additional assistance was also provided when necessary by my research colleagues Dr. A. Ma, Dr. M. Shen, Dr. K. Bothe, M. Benlamri and Professor M. Gupta. The materials processing for the key materials were carried out by Professor K.C. Cadien and members of his group, Dr. T. P. Muneshwar and Dr. A. Afshar.

ACKNOWLEDGEMENTS

First, I would like to give my special thanks and appreciation to my supervisor Professor Douglas W. Barlage for guiding me throughout my graduate studies career. The creativity, worldliness and kindness he provided were invaluable to my growth not only as a scientist and engineer, but also as an individual. Not only did he push my limits as a professional, but he also enabled me to explore paths with full encouragement and support.

I am also indebted to the support from those who guided and provided the resources that were required to complete this long journey. Professor Kenneth C. Cadien and his group members, Dr. Triratna Muneshwar and Dr. Amir Afshar were instrumental in providing the materials and advice that were key to creating a solid body of work that will hopefully have lasting impact. Professor Ying Y. Tsui and Professor Manisha Gupta also supported me during those difficult early graduate student years, for which I am grateful for to this day. With Professor Tsui's encouragement in my later years, I took my first leap to be public communicator of research with unexpected success and which I find myself doing more and more!

My earnest thanks I also give to my colleagues (and now friends), Dr. Alex Ma, Dr. Mei Shen, Mourad Benlamri, Kevin Voon, Peter von Hauff and Dr. Kyle Bothe. The many hours we have spent intensely debating and discussing throughout the past five years was what made this experience much more fun and meaningful.

Finally, the support for my family and my dearest friends is one of the most important reasons I am here today.

Thank you.

CONTENTS

LIST OF FIGURES

Chapter 6

LIST OF TABLES

LIST OF ABBREVATIONS

General

ALD	atomic layer deposition
BJT	bipolar junction transistor
C_{DEN}	capacitance density
C_{MAX}	Maximum capacitance
C_{MIN}	minimum capacitance
CV	capacitance-voltage
CVU	capacitance-voltage unit
FSM	fractal scaling method
GND	ground
MCU	microcontroller
MISCAP	metal insulator semiconductor capacitor
MOS	metal oxide semiconductor
MOSCAP	metal oxide semiconductor capacitor
MOSFET	metal oxide semiconductor field effect transistor
TEFET	tunnelling emitter field effect transistor
TFT	thin-film transistor
TJT	tunneling junction transistor
V_{APP}	applied voltage

Materials

a-Si	amorphous silicon
Au	gold
Cr	chromium
HfO_2	hafnium oxide
IGZO	indium gallium zinc oxide
sc-Si	single crystalline silicon
Si	silicon
Si_3N_4	stochiometric silicon nitrde
ZnO	zinc oxide

1 INTRODUCTION

The impact of 20th century innovations in semiconductor electronics has lead to an extraordinary era of accelerated growth in technology. High-tech progression since the past century have been dictated by advancements in scaling silicon-based transistors, the dominant semiconductor material today. Silicon (Si) has also enabled the exploration of alternative materials for application which itself cannot fulfill satisfactorily. It is understood to be this way because, in order to meet the needs of the applications it serves, silicon electronics requires high material quality in terms of crystallinity and high manufacturing yield. The single crystal requirement to ensure how performance and manufacturing yield increases processing cost significantly. Consequently, the design and development of electronics as a whole is constrained by the non-conformal nature of the key semiconductor material. Additional essential steps before productization include planarization, back-end processing and packaging, the culmination of which can only be offset high extremely high-volume manufacturing.

Therefore, the space which sc-Si and other single crystalline materials cannot sufficiently compete are applications where 1) the electronic material need to be conformal and be able to grow in a consistent manner on a wide variety of substrates; and 2) the production volume need not be colossal proportions to be have a market that is sustainably profitable (i.e. on the scale of 100s of billions of dollars). Flexibility and substrate-independent material synthesis are often intertwined to mean electronics that can be built on any media, such as plastics, glass, etc., on which the electronic materials can conform, even when distorted. One such technology is the emerging field of thin-film electronics and its application space. The common thread between these applications is the absolute requirement of low-cost production that is not strongly dependent on the extremely high-volume production, as required with silicon electronics. In terms of manufacturing, this means that the cost of the

raw material must be reasonably low and the subsequent cost of the infrastructure to build the technology, starting from synthesizing the materials all the way to fabricating the circuit, must remain economical at both low- and high-volume production.

Candidate class of materials that have been proposed and explored to meet these demands are metal oxide semiconductors and organics. Both have shown recent commercial success in the flat display technology that today is driven by the mobile market. Inspired by this on-going success, metal oxides and organics are currently being highly pursued for other large area applications which encompasses conformal, biomedical and disposal electronics.

1.1 Towards a Highly Integrated World

The impetus of the research done here is to bring us closer to the post-modern vision of a deeper relationship between society and technology by pushing towards their more intimate integration. Biocompatible metal oxide semiconductors enable this push due to its abundance and ease of processibility. Metal oxides can be manufactured at low-cost due to compromises made with material crystallinity. By eliminated the need for single crystallinity, processes requiring high temperatures are circumvented resulting in much lower costs. It is under this context where metal oxides show promise: in comparison to non-sc-Si, non-single crystalline metal oxide semiconductors perform much better with key metrics such as mobility and stability [**1**].

This work was inspired by a vertical approach where the design of the electrical components were guided by the needs of the application. Figure **1.1** gives an illustrative overview of all the subjects of interest investigated and their relationship to each other within this body of work.

An aggressive goal was set with the intention advancing past the current limits of thin-film technology, particularly the thin-film transistor (TFT). Practically speaking, the first step was to

define a Level 3 (Lv. 3) category need. Here, a circuit function that thin-film devices can undeniably fulfill when pushed to its limits was chosen. The chosen technology was a signal boosting self-regulating circuit designed for an unstable input supply commonly found in alternative energy sources. A patent was also awarded for this work[1]. The second step was to examine all the electrical elements that make the circuit and deduce which was a challenging task to accomplish (Lv. 2). The third and what is really the true scientific and engineering purpose of this pursuit is to develop and realize the components demanded by this simple but potentially powerful circuit (Lv. 1).

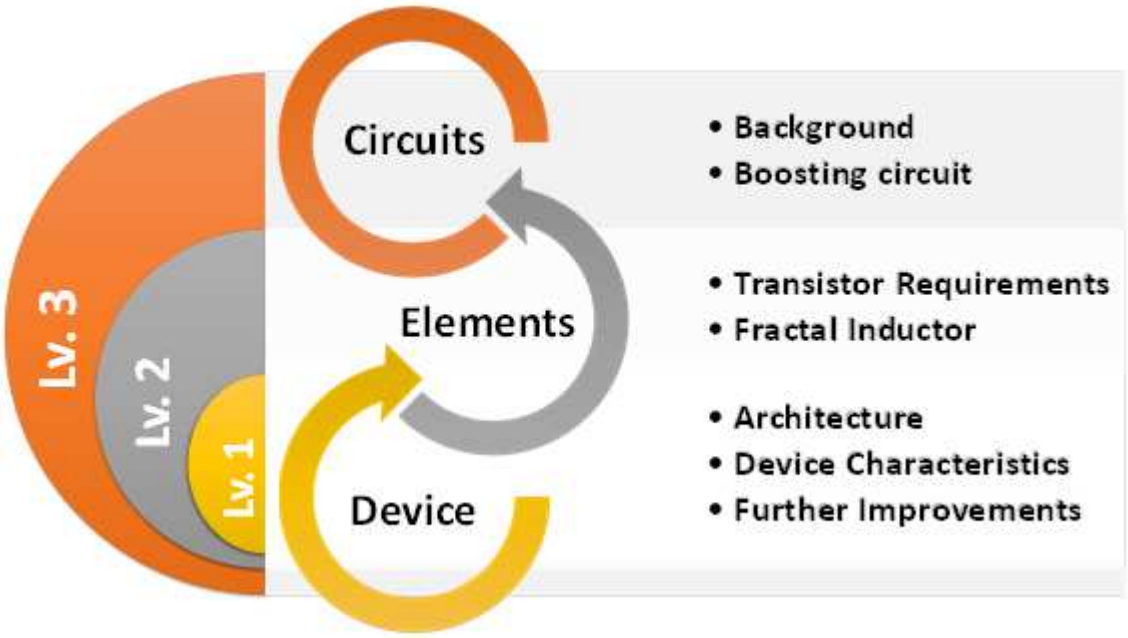


Figure 1.1: A schematic of the vertical approach from which the structure of this work was inspired. Beginning from the highest level, Lv. 3, the application space was defined by a boosting circuit. As we move down to Lv. 2, we consider the important constituent components that make up the circuit. The focus for Lv. 2 was the inductive element along the transistor requirements. The most basic level and the enabling level that is critical to the fidelity of the upper levels is Lv. 1, the device that serve as the key part to the overall circuit application function.

[1] Barlage, Douglas, and Lhing Gem Kim Shoute. "Frequency dependent analog boost converter for low voltage applications." U.S. Patent No. 9,397,561. 19 Jul. 2016.

In the end, the circuit under development in this work itself represents the vast multitudes of electronics, including other circuits, used ubiquitously in a increasing technically savvy world. These same technologies are now evolving flexible and printable capabilities and it is the aim of this research to find a technological space for it to thrive.

1.2 Low Cost & Flexible Circuits for Direct Integration

What is currently marketed as "flexible electronics" is an ambitious futuristic goal where electronics becomes even more integrated in our everyday lives. A proposed flexible device will only ever find success in the commercial space if it can achieve a balance a sustainable cost of manufacturing that can manage wide volume bandwidth. Critical to enabling this is low temperature processing of the constituent materials which in turn introduces significant cost-savings in the manufacturing infrastructure.

One practical and important feature of flexible electronics is its ability to directly integrate an entire circuit to an existing technology. Although flexible circuits are currently being pursued for application in bio-sensing on living mediums, some equally important applications are the amplification of electrical signals of established and emerging technologies such as acoustic imaging tools and alternative energy sources. For instance, capacitive and piezoelectric micromachined ultrasound transducers are emerging diagnostics tools which all require an external circuit of signal amplification. This is usually fulfilled by CMOS technology, but it remains expensive and is met with a multitude of issues related to, for example, bonding and signal routing. Similarly, energy sources, such as solar cells exhibit in principle the same problem [**2**].

These signal sources although having a promising future, suffer from a similar challenge: an unstable input source. DC-DC converters and amplifiers can be utilized as a stabilizing circuit; and, in the case of the well-known boosting topology, a low varying input voltage can be boosted to provide a stable output voltage capable of delivering the required potential for

a multitude of applications. The challenge in making a truly flexible circuit lies in creating an analog circuit that can self-regulate itself without the need of a digitally assisted modulation. Such a circuit was developed here.

1.3 Single Layer Fractal Inductor

The pursuit of simplification of monolithic circuitry, for integrated implementation in printed and flexible/stretchable circuits urges the need for renewed interest in single layer planar geometries for passive components. A comprehensive and insightful investigation of known, mathematically defined fractal space-filling curved geometries was carried out in [**4**]. In addition to fractals already studied by Lazarus, *et al.* (2014), we investigate merits of a loop-based fractal structure in obtaining an appreciable inductance given two important restrictions: that it occupies the same physical design space and, more critically, that it requires only a single fabrication layer.

While the spiral inductor is ubiquitously utilized for a multitude of applications, it nonetheless requires at least two layers or an air bridge to be used in a network [**5**], limiting its use for low-cost circuits. Previously examined alternative single layer planar geometries include the common "loop" and the "meander." However, adjacent electrodes and anti-parallel current pathway lead to an early resonance because of an overwhelming capacitive coupling [**6**]. The loop inductor, on the other hand, does not exhibit this disadvantage as strongly [**7**].

Nevertheless, as in most inductors, the major drawback is the surface area, arising mainly due to the planar structure's poor ability to couple magnetically for better inductive performance. For this reason, we implemented a simple geometrical strategy through fractalization to increase this parameter. Fractals have shown promise for novel transformers, antennas layouts, and even used in the metamaterials design space [**8**,**9**,**10**]. The most successful utilization was in the construction of fractal capacitors, which included design

and optimisation [11]. In this part of the research, sub-200 nm metal films for inductors are studied In order to ensure a satisfactory level of flexibility in related applications. In contrast to CMOS inductors, metal thicknesses of ≥3 μm are usually used. We report the quality factor at sub-200 nm thickness and also normalize them to thicknesses more commonly reported. The fractal loop inductor will be realized ultimately at the thin-film range since for deposition on flexible substrates, while 1 μm are possible with notable limitations [12], sub-200 nm metal films show higher cracking-resilience [13,14].

1.4 Thin-Film Bipolar Junction Transistor

The introduction of a nanocrystalline, disordered semiconductor paved way to the rapid emergence of a new generation of thin-film flexible devices [15]. To further enable thin-film flexible electronics to its maximum potential and beyond the low power limit, a high current density thin-film transistor (TFT) is essential. In order to so, a transistor with true bipolar junction transport must be developed due to the numerous advantages the bipolar junction transistor (BJT) has over the field-effect transistor (FET). An important advantage is that at more relaxed dimensions, the BJT can still have relatively high frequency performance, along with higher current density and transconductance. Furthermore, in contrast to today's TFTs, a BJT architecture provides better stand-off voltage due to the pn-junctions present between the base and emitter and the base and collector. Asymmetrical junctions, of course, are absent in present day TFTs.

Before this was explored, extensive work was dedicated to understanding the behavior of key parts of the device, namely the metal-oxide-semiconductor heterojunction. A model for the capacitance and tunneling characteristics is developed and explored using Schrödinger-Poisson self-consistency methods. The capacitance-voltage (CV) characteristics of the metal-oxide-semiconductor capacitor are modeled and compared with the experimental behavior of the majority carriers of the thin-film semiconductor. A

revision of traditional Schrödinger-Poisson CV extraction was required to consider the geometrical case where the thickness of the active layer is thinner than the theoretical depletion width for a given bias. The insight from the CV modeling is then used to understand the bias distribution of over the metal-oxide-semiconductor (MOS) heterojunction. With this understanding in hand, the workings of such a transistor is then introduced by taking advantage of a unique hole-assisted electron tunneling phenomena coupled with the unique interfacial properties of an ultrathin heterojunction. By using thin-film zinc oxide (ZnO), in conjunction with the p-type hole source and hafnium oxide (HfO_2) barrier layer and a metal as a source of carriers, we introduce a novel thin film bipolar transistor architecture: the thin-film tunneling junction transistor (TJT). A Schrödinger-Poisson interpretation of a true metal MOS tunneling characteristics is developed to understand this phenomenon based on Schottky barrier tunneling instead of the well-studied poly-silicon gate based MOS structures.

The TJT built experimentally was also rudimentarily modeled to extrapolate its potential. Several iterations of the TJT was built and measured based on the suggestions of the model leading to incremental improvements of the device. In particular, parameters affecting saturation characteristics and leakages resulting from the prototype structures are further improved to reach a more ideal electrical performance.

1.5 Market Potential

Displays are predominantly based on polysilicon and amorphous silicon switches but since 2013 indium gallium zinc oxide (IGZO) displays have become commercially available. IGZO since 2004 has been a widely researched amorphous semiconductor which has boosted the interest in flexible electronics[2]. The two major technology to take advantage of these

[2] Nomura, Kenji, *et al*. "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors." Nature 432.7016 (2004): 488-492.

properties are light-emitting diode based displays, which will eventually account for 35% of the market share and sensor applications, accounting for 32% of the share[3]. By 2018, it is predicted that the flexible, printable and organic market will reach up to $10 billion[4]. Although a significant figure, its commercial ceiling stems from the low power limit of all these devices. The work presented here is an attempt to break the low power limit and to further enable thin-film technology into new frontiers by introducing a novel TFT architecture with improved performance over conventional MOSFET-based TFTs.

To summarize the first step was to design a need—a circuit that serves a function in which thin-film devices can undeniably fulfill. In this case, the chosen technology was a signal boosting self-regulating circuit designed for an unstable input supply commonly found in alternative energy sources. The second step was to examine all the electrical elements that make the circuit and deduce which is the most difficult to solve or accomplish. The third and what is really the true scientific and engineering purpose of this pursuit is to develop and realize the components demanded by this simple but potentially powerful circuit.

Each chapter which investigated a component of the circuit followed a general format in spirit of the vertical approach. That is, the device of interest was both initially fabricated and experimentally measured. This was followed by a model dedicated to understanding its behavior and using the model to predict how future improvements could be made.

In the end, the circuit and its components under development in this work is a representation of the vast multitudes of electronics, including other circuits, used ubiquitously in a rapidly advancing society. These same technologies are now evolving flexible and printable capabilities and it is the aim of this research to find a technological space for it to thrive.

---

[3] http://www.electronics.ca/store/printed-organic-flexible-electronics-market-forecasts.html

[4] http://www.marketsandmarkets.com/PressReleases/thin-film-material.asp

2 CIRCUIT DESIGN FOR A SELF-OSCILLATING BOOST CONVERTER

2.1 BACKGROUND

Pulse-width modulation (PWM) converters dominate the field of power systems primarily due to its circuit simplicity and ability to offer a voltage gain greater than unity [16]. More specifically, this is offered by the boost converter topology. Typically, such a circuit consists of the inductor and a switch responsible for the voltage boost, with a rectifying device and a ripple-minimizing capacitor. The gain of the overall circuit is strictly dependent on the nature of the waveform fed to the switching semiconductor device—the transistor; two approaches in particular have been examined: the fixed-frequency/varying pulse-width or PWM converters, and the varying-frequency/fixed pulse-width or resonant converters. The most common method of dictating the switching behaviour of the boosting circuit's transistor is through an extrinsic source, usually in form of a digital microcontroller (MCU). The incompatibility between a digitally driven switch and the pursuit of circuits operational at higher frequencies lies in the latter's objective to minimize both the area employed by the circuit and its bulk costs [17]. To further elaborate, if localized boosting is required for an unstable source, large boosting arrays can be placed at on any compatible media at reduced costs if we eliminate the need for an MCU, thereby reducing the cost of fabrication.

The dependence of an external driver for the transistor is eliminated in a resonant converter. In such a converter, the LC network causing the self-oscillation at resonance is implemented within the circuit, which in turn determines the switching behaviour. It is also operable at higher frequencies which allows for the miniaturization of component size, making it ideal for integrated circuit applications [18]. Unfortunately, these class of converters poses the gain limitation of at most unity, which is achieved only at resonance.

In order to address both the problem of self-regulation and circuit compactness, the studied boost converter was designed for the frequency range designated "very high" (VHF) which spans from 30MHz to 300MHz. The frequency range of TFTs today range from 10 kHz to 1 MHz due to their low current throughput. Due to the low frequency of operation, the inductive component must be very large making more difficult to make large arrays of converters within a confined space. To address this transistor limitation, it is necessary to design a TFT architecture that pushes the current density, thus also increasing the frequency response, to minimize the size of reactive components such as inductors and capacitors.

2.2 CIRCUIT TOPOLOGY

In essence, a frequency-dependent gain boost converter is realized with the proposed topology (Figure **2.1**). As previously stated, it contains the cardinal DC-DC converter components including the inductor (L1), the switching semiconductor device (M_{SWITCH})—the field-effect transistor (FET), the rectifying diode (D1) and a ripple-free capacitor (C2). The output terminal (T_{OUT}) is taken at the positive terminal of C2 (5).

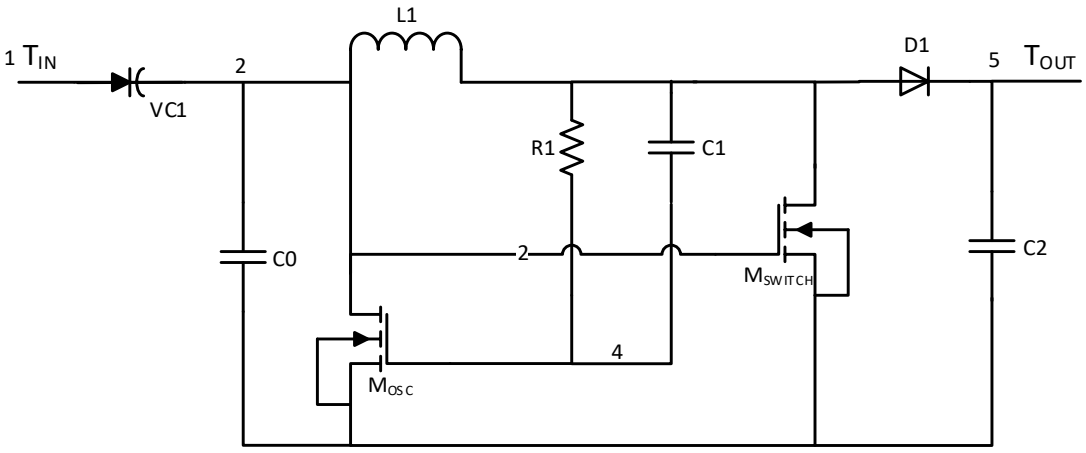


Figure 2.1: Proposed open-loop circuit schematic of a gain-varying self-oscillating boost converter. The inductive component L1 and the transistors M_{OSC} and M_{SWITCH} are of particular interest for realizing circuit using thin-film components.

The self-oscillating network comprises of a capacitor (C1) and resistor (R1) in parallel with their low-terminal (4) connected directly to the gate of the second switch (M_{OSC}), a third input capacitor (C0) placed in parallel with the input source and, finally, a varactor (VC1) situated between the onset of the inductor (2) and the circuit's input terminal (T_{IN}). The gate of M_{SWITCH} is tied to the drain of M_{OSC} (2). Introducing the varactor into the overall LC-network allows for the modulation of the self-oscillating frequency which dictates the gain of the circuit. It should be noted that the varactor is oriented such that a higher applied voltage results in an increase of capacitance, while a lower voltage exhibits the opposite effect. The varactor's capacitance is varied according to the voltage applied at (1) with respect to (2).

2.3 Operations and Performance Demands

2.3.1 Voltage Gain

At lower capacitance and therefore increased current coupling, the peak-voltage of the pulse applied at the gate of M_{SWITCH} is greater than at larger values. As a result, the variance of the gain of the boost converter is obtained because the bias of the M_{SWITCH} gate also varies, which in turn controls the current throughput. In general, if the signal feeds a higher peak-voltage, the greater the gain and vice versa for lower on-state-voltage values.

In the open-loop configuration, the varactor's value is determined by the variable input voltage source. It is oriented such that at higher input voltages, a higher capacitance value is adopted; the converse is true for lower input voltages. As shown in Figure **2.2**, capacitance and the corresponding frequency is positively correlated. The frequency was normalized to 30 MHz (lowest frequency) and the capacitance was normalized to 1 nF.

A detailed example of operation is as follows: the boost converter operates at some self-oscillating frequency and provides its corresponding gain at T_{OUT} when a certain voltage is experienced at T_{IN} at time t_0. When the varying input voltage source provides a higher potential at T_{IN} at a time t_1 greater than t_0, the depletion width of the varactor is subsequently

decreased, which in turn increases capacitance. This rise in the overall capacitance of the circuit at t_1 results in the increase of the self-oscillating frequency, causing T_{OUT} to experience a reduced gain.

Similarly, a lower input voltage at T_{IN} results in the narrowing of the depletion width of the varactor, leading to lower capacitance and operating frequency, which consequently increases the voltage gain. It is worth mentioning again that the operation of the varactor described above is the reverse of the behaviour that is traditionally expected given the external stimulus. However, the desired mechanism of operation is consistently observed even in conventional active devices and can be exploited accordingly.

This behavior also further elaborates on why the frequency of oscillation rose at larger capacitance values: the capacitance increase indicated the thinning of the depletion width of the varactor device. Understanding this as a diode, the decrease in the depletion width corresponds with the varactor turning on. Hence after approximately 1 nF, the frequency oscillation began to saturate due to the nigh short-circuit state which the varactor diode operates beyond this point.

Bias sensitivity in the varactor is, of course, advantageous. The variance of the varactor capacitance with respect to its bias requires the oscillation of the converter to be highly sensitive to miniscule capacitive changes to attain a wider range of achievable gain. Examination of gain versus capacitance shown in Figure **2.3**.

The domain representing capacitance spans from 0.5 nF at the highest gain to 10 nF at the lowest gain, with the most sensitive region spanning from 0.5 nF to 1 nF. At higher capacitance values, the varactor diode is turned on leading to the suggestion from Figure **2.2** that the highest frequency that the converter components need to operate at is approximately 110 MHz. The transistor must also be able to properly operate at 60 MHz to be able achieve the full gain range (from ~4.5 V/V to 2 V/V).

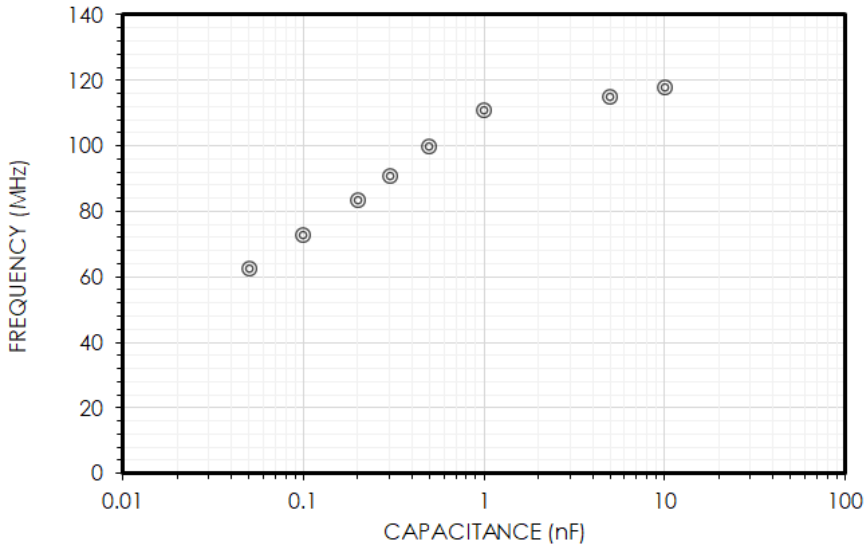


Figure 2.2: Frequency response of the open-loop circuit with varying capacitance. The frequency increases with capacitance due to critical coupling of the varactor diode as it approaches its turn-on voltage. At 1 pF, the varactor is nearly short-circuited leading to the saturation of the oscillation frequency.

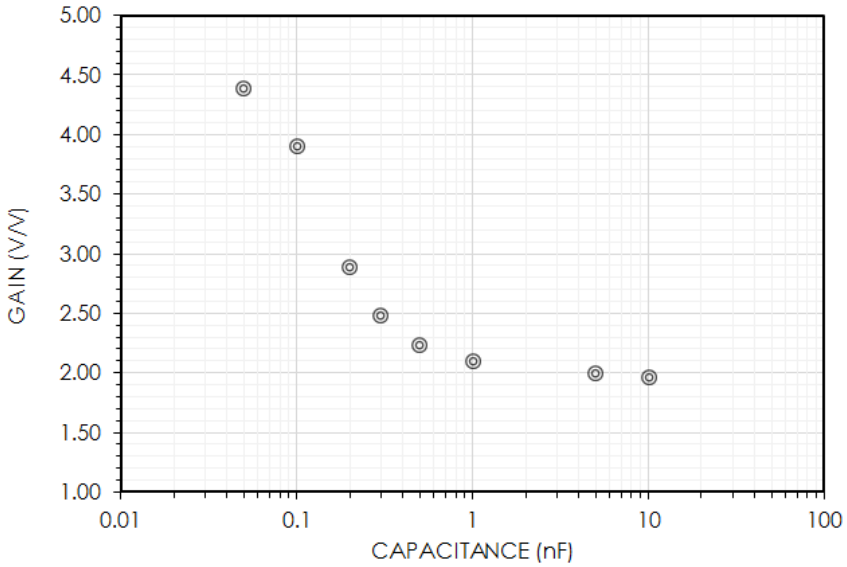


Figure 2.3: Gain response of an open-loop circuit with varying capacitance with a normalized scale. The cut-off frequency ~110 MHz corresponded with the 1 nF turn-on of the varactor capacitance where the gain only minimally varied.

2.3.2 ELEMENTAL METRICS

From simulations, particularly for the inductor and the transistor certain performance metrics were required in order to perform properly. For the inductor, the circuit required an inductance of at least 50 nH with a minimal resistance of at most 5 Ω. The minimal transistor requirements are transconductance of at least 15 $\mu A/V^2$, a drain resistance of 10 Ω, a junction capacitance of at least 1pF, and turn-on voltage of 0.2 V. Finally, because the gain improved at lower oscillating frequency and with gain variance being limited at beyond 110 MHz, we require a TFT that can operate from 60 MHz to 110 MHz to take advantage of the full gain range.

2.3.3 ALTERNATIVE GAIN MECHANISM: USING A TUNNELING EMITTER BIPOLAR TRANSISTOR

In principle, the MOSFETs M_{SWITCH} and M_{OSC} can easily be replaced by bipolar junction transistors, and their operations will be more or less the same. This solution may be favourable and more realistic since the key operations behind the voltage gain is the increased coupling of the inductor with the input source, as dictated by the capacitance between these two terminals. Because of this, the range of varying capacitance demanded of the varactor is very high, spanning just over an order..

2.4 CONCLUSION

The discrete systems illustrated above coalesce to provide the desired self-oscillating boost converter for low voltage applications. For example, it can be utilized to drive or charge a variety of devices requiring a specific voltage. It is also possible for use in the stabilization of variable input sources. By understanding the operations of the boosting circuit, we gained insight on the demands of its individual components. What is especially essential is the that the active transistor devices be able to manage the high current throughput and sustain the relatively large oscillating frequency ranging from 60 MHz to110 MHz. Moving forward, this study serves as a guidance for what the performance targets that key components must

reach in order to ensure the operation of the self-oscillating boost converter, and other potential high fidelity circuits.

In the next section, we developed the inductive component. Inductors are critical to the operation of the boost converter, but also in a variety of other applications, such as communication circuits. Consistent with the goal of this work, a planar fractal inductor was experimental developed and modeled to evaluate the performance of thin-film inductors.

3 PLANAR INDUCTOR DESIGN USING FRACTAL LOOP GEOMETRIES

3.1 BACKGROUND

We examined the fractal derivations of the original loop due to its space filling properties [19]; whilst the arrangement still essentially occupies the same space. The fractal loop was chosen due to its lower capacitance coupling of the adjacent electrodes relative to what was observed for meander geometries. All structures studied are compared against each other in an all-inclusive inductance versus resistance or "L and R" gain plot. The aim of this consolidation is to demonstrate which strategies are worth pursuing for further investigations within the loop-fractal family. We achieve this by introducing an "Inductance gain" Figure of merit (FOM). Because higher order fractals result in a lengthened conductive pathway, both self-inductance, the inductance from an individual loop, and mutual inductance, the inductance from interacting magnetic field of proximal electrodes is enhanced [20,21].Consequently, it is crucial that the signal's magnetic component is able to interact with the coupling features of the geometry.

3.2 FRACTAL DEFINITIONS

Naming conventions for fractal geometries are explicitly defined in accordance with mathematical definitions [22]. A simple loop inductor was used as the base geometry from which all fractal configurations are derived. The associated nomenclature of the fractal geometry is determined by the amount of recursion within the effective planar area of the original structure [23]. For instance, the "3O" fractal is equivalent to three base structures oriented such that the overall outline resembles the base. These configurations are studied to determine the optimal geometry to be set as the "first order" fractal; *i.e*. the first fractal derivative of the base structure. Furthermore, one of these structures is chosen for further recursion to create a 2nd order structure, and once more to yield a 3rd order structure. All

structures were fabricated on a borofloat glass substrate with an adhesion chrome layer of 30 nm, followed by a 150 nm gold layer. Figure 3.1a is an example of fabricated inductor taken with an optical microscope. The inductor layouts for the other realized structures are shown from Figure **3.1b** to **f**, with the Figure **3.1f** being an example of the simulated layout in KeySight's EM Design Tool, taken directly from the gds layout file used for the constructing the mask. The equivalent series layouts for each fractal order were also evaluated; an example is given in Figure **3.1g** for the 3rd order.

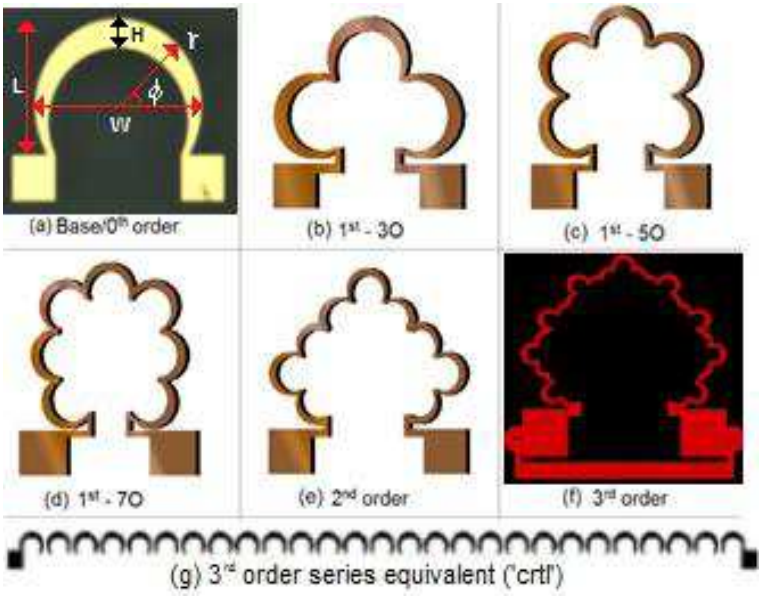


Figure 3.1: The (a) fabricated base inductor and dimensional definitions; the set of 1st order structures consisting of (b) 3 bases, (c) 5 bases, (d) 7 bases; (e) the 2nd-3O order fractal and (f) the 3rd -3O order simulated fractal; (g) an example of a control (ctrl) structure: shown is the 3rd order series equivalent.

3.3 Effect of Fractalization

Raw inductance measurements L are shown in Table **3.1**, with a margin of error dependent on probe placement. With respect to the base 0th order fractal, increasing both the amount of recursion (for the 1st order) and fractal order was met with an improved inductance but added resistance R. The raw values of inductance and resistance are normalized to the base loop value and shown in Figure **3.2**. Without any resistance reduction strategies, the

resistance from the base to the highest order amplifies more so than the inductance: 12.6 times in resistance, and 9.9 times in inductance. These trends are also revealed in Figure **3.3** connected by a dashed line.

Table 3.1: Raw inductance and resistance

Fractal Order	Inductance *L* ±1.0 nH	Resistance *R* ±0.5 Ω
Base/0th	4.6	5.0
1st		
3O	8.6	10.5
5O	11.0	11.6
7O	12.9	17.3
2nd	19.2	23.2
3rd	44.7	63.5

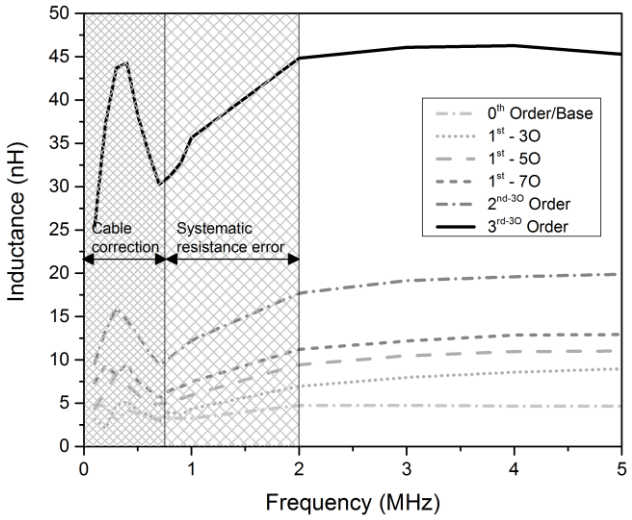


Figure 3.2: Raw inductance measurement of the loop inductor and its subsequent higher order fractal geometries using the Keithley 4200 SCS CVU.

When this trend is compared to other fractal geometries, for example the Hilbert fractal of [**24**] and [**25**] which adopted a meander configuration as its second order structure, from "2nd order" to "5th order" both the inductance and effective area occupied increased five times, where for the loop base structure studied here to the 3rd order, the inductance improved 9.9 times while essentially maintaining the same occupied space. These structures

also compare favorably to the extensive study done by Lazarus, *et al.* (2014) when the normalised for electrode thicknesses.

For example, the base inductance is measured at 4.6 nH with a resistance of 5 Ω; and, we observed a 3rd order inductance of 44.7 nH at 63.5 Ω. Self-inductance alone does not sufficiently explain the increase. Thus we must attribute the increase to the mutual inductance that the fractal oriented loops fosters and which the current simulation tool is unable to predict. To further investigate the extent of the mutual magnetic coupling and explain the discrepancies, we described the structure using known models for determining inductance. These models are summarized in the following.

Considering the contribution of the geometry's self-inductance to the overall inductance rating, with ϕ' being the angular limits of the loop and C being the full circumference of a single loop given a radius r, we can approximate it using the following model for circular loops, an example described by Clayton (2010):

$$L_{self} = \frac{\mu_0}{2\pi} \int_{\phi'=\frac{11\pi}{18}}^{2\pi} \int_{r=0}^{r-\frac{H}{2}} \frac{1}{r} \left[\int_{\phi=0}^{\pi} \frac{a^2 \cos\phi \, (a - r\cos\phi)}{(a^2 + r^2 - 2ar\cos\phi)^{\frac{3}{2}}} d\phi \right] r dr d\phi' \tag{3.1}$$

Which can be further approximated to [**19**]:

$$L_{self} = \frac{\mu_0 C}{2\pi} \left\{ \ln\left(\frac{8\pi r}{H}\right) - \frac{7}{18} \ln\left(\frac{8\pi r}{H}\right) \right\} \tag{3.2}$$

For higher order fractals, since each recursion is simply scaled accordingly, we can arrive at a rough estimate by first evaluating the self-inductance of a single scaled-down loop using (**3.2**), then multiplying by the number of copies within the structure. The rough mutual inductance estimate is then:

$$M = L - L_{self} \tag{3.3}$$

As previously mentioned, the non-linear increase suggested a mutual magnetic coupling which goes beyond simply the increase of the effective length as shown in Table **3.2**. To elaborate further, a possible reason for the discrepancy between the simulated and measured inductance can be explained in terms of the mode of field that interacts with structure. Because the EM simulation tool excites the planar structure in the transverse electric mode, we can still accurately arrive at the resistance values which closely match measurements. The discrepancy in the inductance between measurement and simulation is thought to be from the transverse magnetic field. Further to that, the capacitance-voltage unit (CVU) of the Keithley 4200 SCS tool is not obstructed by reflections and subsequent mis-measurement from unaccounted for modes. The advantage of this measurement technique being that the CVU forces current and measures the voltage with a phase differences in order to decouple both signals making it independent of load mismatches. Furthermore, the technique also does not discriminate any EM modes. Thus, the inductance measured from this unit can be considered to capture the true inductance of the element including fractal effects.

Table 3.2: Dimensional properties, self-inductance L_{self} and mutual inductance M

Order	$N^{\dagger}$	L×W×H* (mm)	r (μm)	Sim. L (nH)	L_{self} (nH)	M (nH)
0th	1	1.6×1.6×0.30	770	3.6	2.6	2.0
1st						
3O	3	1.6×2.2×0.13	365	4.2	3.6	5.0
5O	5	1.7×1.3×0.12	273	4.6	4.2	6.7
7O	7	1.8×1.9×0.10	208	5.0	4.4	8.4
2nd	9	1.7×2.3×0.06	171	5.3	5.0	14.1
3rd	27‡	1.8×2.4×0.03	100	6.8	9.2	35.5

*See Figure 1a for definitions

†N is the number loops for a given order if the loop were not a diluted fractal.

3.4 Inductance Quality Gain Figure of Merit

The quality factor Q must be improved at the thicknesses investigated here (180 nm). In order to more accurately compare Q with competing planar inductors, we needed decrease the resistance without compromising inductance.

$$R_{Scaled}t_{scaled} = R_{180\text{nm}}t_{180\text{nm}} \tag{3.4}$$

From equation (3.2), inductance does not heavily depend on electrode thickness t. Conversely, the resistance is inversely proportional to t as in equation (**3.4**). These claims were confirmed by simulation for all structures shown in Figure **3.1**, with the only modification being an order increase by t. The Q and scaled Q_{scaled} at 1 GHz are shown in Table **3.3**.

To determine which geometry provided a better relative inductance rating over its associated resistance, we define an "Inductance quality gain" figure of merit. A inductance quality gain is achieved when the normalized inductance rating falls in the lower diagonal

of the "Unity gain" or G = 1 line, while resistance gain will fall on the upper diagonal. Unity gain is defined as:

$$G = \frac{G_L}{G_R} = \frac{L}{L_0}\frac{R_0}{R} = 1 \tag{3.5}$$

Where:

$$G_L := G > 1 \; Inductance\ gain\ (Lower\ diagonal) \tag{3.6a}$$

$$G_R := G < 1 \; Resistance\ gain\ (Upper\ diagonal) \tag{b}$$

All geometries and configurations discussed in this study are compared with each other using this FOM in Figure **3.3** and evaluated for the original and doubled width structures in Table **3.3**.

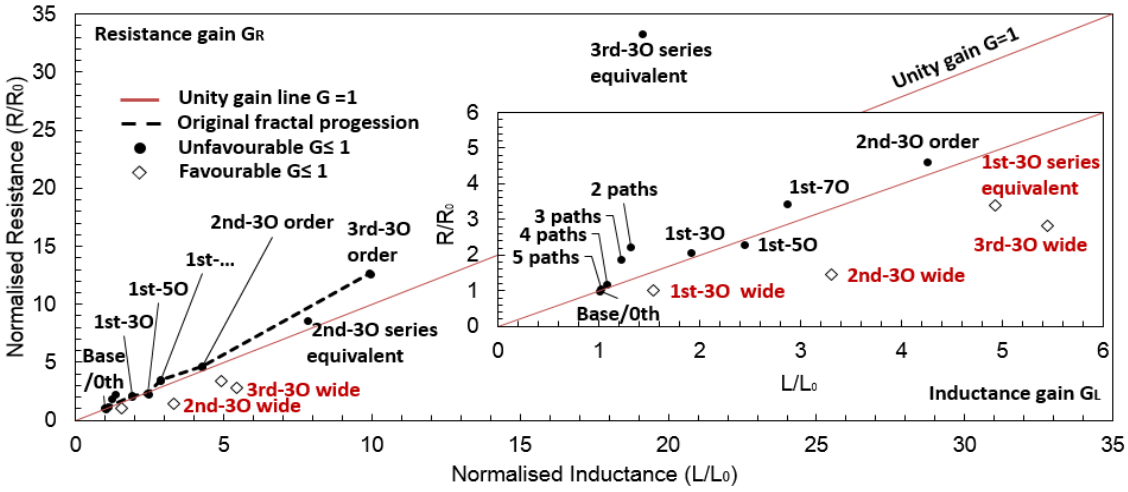


Figure 3.3: L and R gain plot of all structures studied comparing inductance to resistance normalised to the 0th/base loop. Here, the null gain line represents no tradeoffs between resistance and inductance; points that fall in the lower diagonal represents an inductance gain that is greater than resistance for a given structure. The dashed line emphasizes the L and R progression with respect to the original fractals. The inset magnifies and highlights the structures exhibiting an inductance gain; in particular, "wide" tag denotes that the electrode width was double (2H) that of the original fractal; the "paths" tag denotes the number of geometrically identical paths placed in parallel with each other.

Table 3.3: Quality Factor at 1 GHz at flexible thickness (180 nm) and scaled thickness (1.8 μm) and inductance gain FOM G for the original O and doubled-width W structures for 180 nm electrode thickness

Fractal Order	Q		G	
	Q_{scaled}			
	t = 180 nm	t_{scaled} = 1.8 μm	*O*	*W*
0th	5.8	57.8	1.0	
1st				
3O	5.2	51.5	0.9	1.5
5O	6.5	65.0	1.1	-
7O	4.7	46.5	0.8	-
2nd	5.2	52.0	0.9	2.3
3rd	4.4	44.2	0.8	1.9

We conclude that the 3rd wide inductor showed the most promise because it optimized both the inductance and resistance metrics, with the 2nd coming second. We posit that the nature of the 3rd order fractal, and the fractal strategy in general, is able to maintain a high inductance per sheet rating because the geometry which includes recursive loops in close proximity to each other is conducive to mutual magnetic coupling; and, though placing the loops in series also demonstrated excellent coupling, because its effective length is longer than its fractal equivalent and its electrode width is a fraction of the original loop, these structures showed much higher sheet resistance.

3.5 Sheet Resistance

Because we emphasize the planar aspect of the inductors examined here, especially in low-cost applications which would restrict the fabrication process to a single layer, the sheet properties of the inductors are examined. For applications where conductor consumption is a concern, we also examine the conductor area taken up by each structure.

Sheet resistance analysis at a thickness of 180 nm in Figure **3.4a** revealed that for the first two orders, the resistance per square was lower than the basic loop inductor, up until 3rd order fractal which exhibited a slight degradation. However, when comparing the sheet resistance to the measured inductance (inductance per square) for each geometry, a clear improvement is observed. In the same figure, the series configuration (control) was also contrasted with the equivalent series layout (Figure **3.4a**). The assessed sheet resistance was consistently higher with the series equivalents than its comparable fractal structure. In addition, the inductance per sheet resistance for the control also produced poorer ratings, with the exception of the 3rd order equivalent structure. Any observed improvements in the sheet resistance is a result of the effective lengthening and narrowing of the electrode as the fractal increases in order.

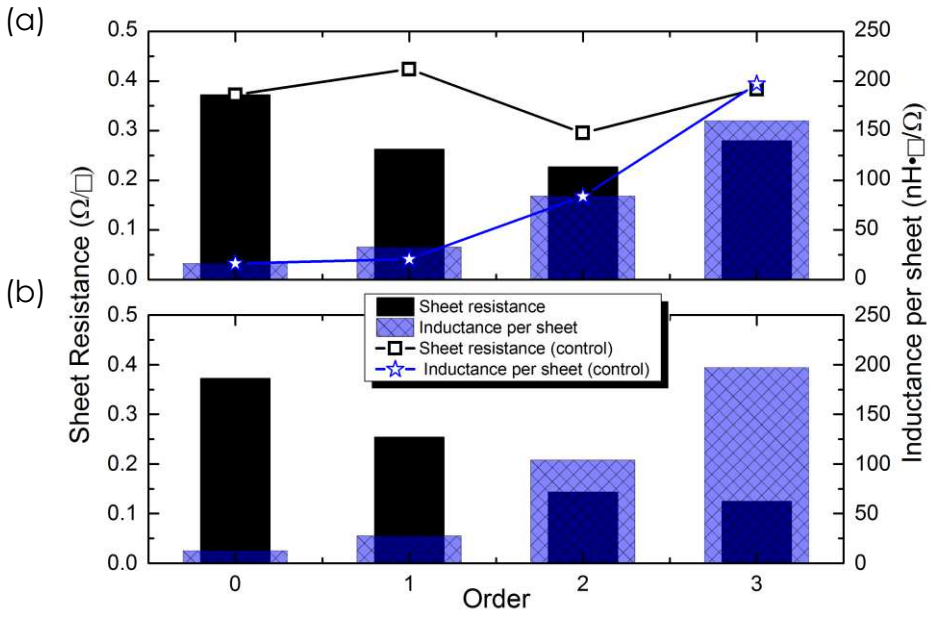


Figure 3.4: Measured sheet resistance and inductance per square analysis for each fractal order based on 1st-3O geometry extracted from (a) the original structures and its equivalent series layout (control); and, (b) with electrode width doubled from the original. Here, smaller black bars and larger checkered bars mean higher inductance per square area of resistance.

The effect of doubling the electrode width (from H to 2H) for all fractal orders higher than zero is also shown in Figure **3.4b**. While for the 3rd order the inductance decreased by approximately half of the original amount, the resistance fell to under a quarter of the original electrode width. Furthermore, we found that doubling the electrode width had dramatically reduced the effective sheet resistance at higher orders. In other words, the actual resistance reduced faster than the number of squares from a geometrical argument.

Combining Figure **3.3** and Figure **3.4** demonstrated that the major advantage of the fractal loop geometry was that the relative inductance rose faster than the relative resistance with increasing fractal order.

3.6 Analytical Model for Mutual Inductance

3.6.1 Extracting δ: The Fractal Scaling Approach

Scaling arising from the dimensionality of further fractilization has been previously observed and used to describe fractal capacitors [**26**] and even to explain the perlocation of electromagnetic particles [**27**]. In the work by Robin, *et al.* (2007), fractal scaling is used to model the electromagnetic properties, including inductance, of conductive grain boundaries resulting from fractal aggregates using generalised antenna equations. However, this method as a design technique and optimisation tool for inductors were not previously realized.

Here, we constructed a generalized expression for any arbitrary shaped loop-based fractal that depends on the fractal dimension of the geometry of interest with respect to the base/0th order of said loop.

An important difference between the classical approach and the fractal approach must be distinguished. The classical model considers the total inductance to be the sum of two key components: the self-inductance L_{self} and the mutual inductance M as expressed in

(**3.3**). In contrast, fractal dimensionality approach which, by the nature of fractals, considers the total inductance to be L_{self} scaled by some factor ζ_f as in (**3.7**).

$$L = \zeta_f L_{self} \tag{3.7}$$

Figure **3.5** provides an illustrative visual field interaction in a fractal loop structure for the following.

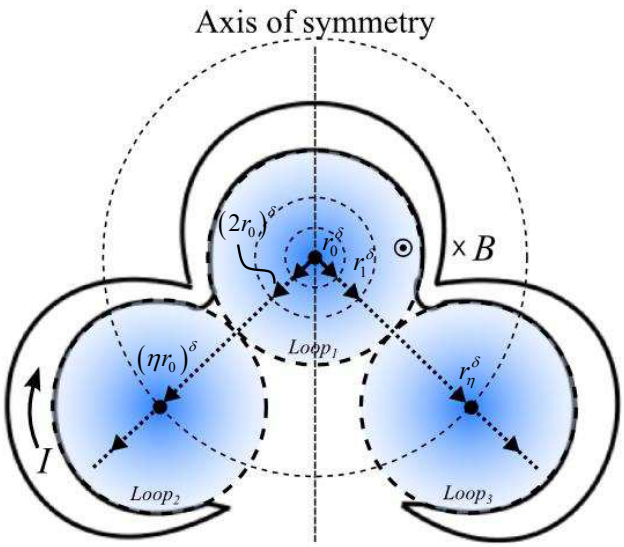


Figure 3.5: The essential geometrical parameters for the fractal dimensionality approach. Here, the 1st-3O order is used as an example.

The validity of the fractal scaling model is proven based on the assumptions:

i. L_{self} is classically modeled with some confidence using (**3.2**).
ii. The magnetic field B generated from one loop, which contributes to L_{self}, is also captured by the adjacent loop, contributing to the total inductance L.
iii. There exists at least one axis of symmetry with a complete absence of edges for all orders of the loop fractal taken to account in ζ_f.
iv. A single magnetic field line is captured by an infinitesimally small loop of radius r.
v. The inductance resulting from iii. can be summed together to capture the total inductance,
vi. The strength of the magnetic field in a loop is inversely proportional to the distance r of the point where B is evaluated according to Biot-Savart Law:

$$B = \frac{\mu_0 I}{2r^{\delta-1}} \tag{3.8}$$

Where δ is the dimension of the shape. For the base/0th order, δ = 2, which corresponds to the area in which the magnetic field is captured.

vii. Additional contribution to the total inductance can be scaled according to the dimensionality of the fractal with respect to the dimension of the base/0th order.

Taking to account to i to vii, equation (**3.7**) can be expanded further:

$$L = \left(L_{self_{loop1}} + L_{self_{loop2}} + \ldots + L_{self_{loopN}} \right) \frac{r_0^{\delta}}{r_1^{\delta}} + \left(L_{self_{loop1}} + L_{self_{loop2}} + \ldots + L_{self_{loopN}} \right) \frac{r_0^{\delta}}{r_2^{\delta}} + \ldots \tag{3.9a}$$

This can be simplified further if we only define the point of interests as integer multiples of r_0 away from the original point.

$$L = \left(L_{self_{loop1}} + L_{self_{loop2}} + \ldots + L_{self_{loopN}} \right) r_0^{\delta} \times \left(\frac{1}{r_0^{\delta}} + \frac{1}{(2r_0)^{\delta}} + \ldots + \frac{1}{(\eta r_0)^{\delta}} + \ldots \right) \tag{3.9b}$$

By factoring $1/r_0^{\delta}$ this can be further reduced to and compactly written as:

$$L = \sum_{\eta=1}^{\infty} \frac{1}{\eta^{\delta}} L_{self} \tag{3.10}$$

Where,

$$\zeta_f = \sum_{\eta=1}^{\infty} \frac{1}{\eta^{\delta}} \tag{3.11}$$

Which follows the same form as (**3.7**). We then use (**3.11**) as the fitting parameter to match L from (**3.10**) to the measured inductance. The results are summarized in Table **3.4**.

Table 3.4: Key metrics calculated from using the Fractal Scaling Method (FSM)

Fractal Order	$\zeta_{f\text{-}Experimental}$†	Quantities for and from Fractal Scaling Method†			
		N_{eff}	ζ_f	δ (FSM)	δ' (Geometric)
0th	1.8	1	1.64	2	2
1st					
3O	2.4	3	2.43	1.55	1.58
5O	2.6	5	2.61	1.5	1.46
7O	2.9	7	2.96	1.425	1.40
2nd	3.8	9	3.79	1.3	1.37
3rd	8.7	15	8.58	1.13	1.125

†These values were also used to calculate L_{self} using (3.2) for complete consistency.

Several crucial design implications and predictions stemming from the fractal scaling model arise as a consequence.

i. Since the base/0th order structure has a fractal dimension associated to it, there is a fractal scaling factor ζ_f associated to it as well. From [**16**], δ = 2 converges to:

$$\zeta_{f_{\delta=2}} = \frac{\pi^2}{6} \approx 1.64 \tag{3.12}$$

This is comparable to its experimental value of 1.8.

ii. The theoretical geometric fractal dimension is predicted by the number of effective new loops N_{eff} and the amount which they have been scaled down according to $\epsilon = 1/(r_{base}/r_{order})$ while occupying the same area as the original shape (**3.13**):

$$\delta' = -\frac{\log N_{eff}}{\log \epsilon} \tag{3.13}$$

iii. According to (3.15), as the fractal dimensionality approaches 1 ($\delta \rightarrow 1$): the inductance approaches infinity ($L \rightarrow \infty$), and (**3.8**) is no longer valid.

iv. Loop fractals can be optimised based on N_{eff} and ϵ.

3.6.2 OPTIMISATION BASED ON THE FRACTAL SCALING MODEL

Table **3.4** revealed that, although 3rd-3O order used ideally 27 loops as initially conceived, the effective number of loops is N_{eff} = 15 to obtain the same inductance rating (an effect of fractal dilution). Hence, the 3rd-3O order fractal could be optimized using just 15 loops while maintaining the same scaling factor ϵ, and the same inductance would be obtained. The alternative is a structure with 27 loops with scaling factor of ϵ = 1/19, which is the less ideal design optimisation approach. The manner in scaling ϵ is also at the behest of the designer. In this experiment, as previously mentioned, ϵ was scaled according to the radius of a particular fractal order with respect to the base/0th order structure. Scaling ϵ according to, for example, electrode width, or height, etc. are also perfectly valid parameters. Other more fundamental parameters can also be investigated like changing the electrode material or adding magnetic oxide at key layers to further enhance the inductance.

3.7 CONCLUSION

Planar loop-based fractal inductors built using thin metal films of 180 nm were fabricated to understand the trade-offs between inductance and resistance. Thin metal films were used because of the inductor's foreseeable application on flexible substrates.

Through fractalization of a basic loop structure, it was found that there is a measurable and fractally-scaled improvement of inductance per unit of space taken by the 0th order fractal or the original inductor, with the highest recorded fractal inductance value of 44.7 nH. The result suggests that the loop-based fractals have excellent magnetic coupling properties possibly explained by the proximity of each adjacent loop which encourages mutual

coupling leading to an enhancement of inductance. The projection of the quality factor Q was determined simply by scaling the electrode thickness from 180 nm to 1.8 μm at 1 GHz: the Q was found to be greater than 40 for all structures.

An analytical model for the gain in inductance for every increase in order was also constructed based on the established method of "Fractal Scaling" applied to loop fractal inductors for the first time. By determining the dimension of the fractal with respect to the base/0^{th} order fractal, the scaling factor ζ_f was extracted which closely matched the experimental scaling factor. Furthermore, the fractal dimension δ calculated using this method was in close agreement with the geometric fractal dimension commonly used to evaluate the dimension of all patterns considered to be fractal in nature. With this fractal loop model, a clear design and optimization path for maximal inductive output is presented.

Based on this study, we believe that the application in printed and flexible/stretchable circuits of the fractal strategy on a simple loop inductor is an effective method to maximally harness the magnetic energy for improving inductance ratings within a single planar layer.

4 CAPACITANCE-VOLTAGE MODELING FOR MOS CAPACITORS USING THIN-FILM SEMICONDUCTORS

4.1 BACKGROUND

Insight into the behavior of the carriers semiconductor in simple structures is important for designing future devices. Metal oxide/insulator semiconductor capacitors or MOSCAPs/MISCAPs are frequent subject of investigation because they simplify a full field-effect transistor (MOSFET) to perhaps its most vital part, the channel and its formation. Electrostatic modeling can give both material and device designers an understanding about the material and its charges which determine the characteristics of the structure. Models developed have long paid the most attention to the material and the material system in and of itself while paying little attention to geometrical affects. Such an oversight was allowed since majority of the models were developed for bulk semiconductors.

These approaches however are based upon the fundamental architectural assumption that the depletion width of the semiconductor is lower than the thickness of the bulk semiconductor. The big picture goal is to fill the knowledge gap of MOS structures that does not conform to the bulk architecture. In particular, for cases where the active semiconductor layer thickness is indeed less than the theoretical depletion width. This study can be directly applied to ultrathin films used for the MOS layers in all modern TFTs. It will further discuss how the geometrical dimensions and the structure of the film influences some of the relevant electrostatic behavior which in turn affects the overall CV. As the structures get more complex with additional junctions introduced in the following chapter, this analysis can also be used to predict the true capacitance at the MOS interface independent of parasitics such as leakages and defects.

The results and discussion of these findings are not meant to solely address the challenges of the material used here (ZnO). It is the intention of this study to be applicable to a multitude of semiconductors that are used as thin-films within the MOS capacitor architecture where there is sufficient isolation from other capacitive plates.

4.1.1 METAL OXIDE SEMICONDUCTOR CAPACITORS

The compact relationship for capacitance-voltage (CV) is that charge varying with varying voltage gives rise to capacitance. This same fundamental principle is also applied for models attempting to understand the CV characteristics of MOSCAPs.

$$C = {dQ}/{dV} \tag{4.1}$$

Equivalent circuit model of the MOSCAP consists of two capacitors placed in series and is described analytically in Eqn (**4.2**). Capacitance-based doping extraction methods also assume a classical distribution along uniform distributions [**28**,**29**,**30**]. In this simple description, C_T is the total capacitance of the structure. This can be further broken down into the oxide capacitance C_{OX} which is assumed to be constant in the frequency range of interest and the semiconductor capacitance C_S. This schematic is visually illustrated in Figure **4.1**.

$$\frac{1}{C_T} = \frac{1}{C_{OX}} + \frac{1}{C_S} \tag{4.2}$$

For bulk semiconductors, C_S is dictacted by the change in mobile charges as the potential in the semiconductor is modulated. If the active film is supplied with a sufficient amount of free carriers, a channel will be formed at the insulator-semiconductor (MOS or MIS) junction. When the channel is made up of the semiconductor's majority carriers, the MOSCAP is considered to be in the "accumulation" voltage region. From this region to the point where minimum capacitance is reached is the depletion region. If a channel formed by minority carriers is operating at the "inversion" voltage region with, a more critical caveat is that these

carriers are supplied in abundance. Invesrion capacitance is larger than the absolute minima, otherwise, if the semiconductor is unable to form an inverted channel, the MOSCAP is considered to be operating at the "deep-depletion" region.

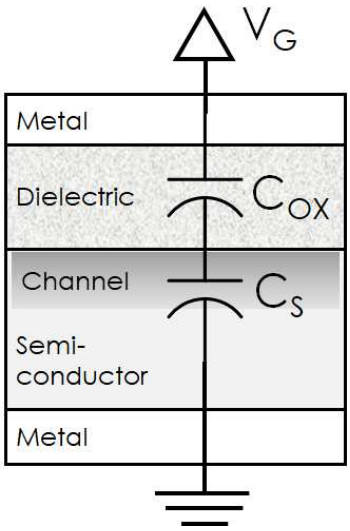


Figure 4.1: Equivalent circuit model of a MOSCAP containing two capacitors in series: C_{OX} which represents the capacitance arising for the insulator and is constant throughout the voltage range, and C_S representing the channel capacitance which does vary with the gate voltage V_G.

4.1.2 MOSCAP GEOMETRY

Planar MOSCAPs were evaluated within a circular geometry as illustrated in Figure **4.2a**. Figure **4.2b** breakdowns the constituent layers consisting of the substrate as the base layer, upon which the active layer of interest is deposited, followed by the insulator layer and ending with metal contacts at the upper most layer. The channel was formed underneath the inner metal contact when a bias V_{APP} or V_G (gate voltage) was applied. The outer contact is set as the common terminal and is labeled "GND". In this geometry, the electric field is radially symmetrical such that the raw capacitance C_{raw} can be normalized by the radius of the inner metal contact r to give the capacitance density as follows:

$$C_{den} = \frac{C_{raw}}{\pi \cdot r^2} \tag{4.3}$$

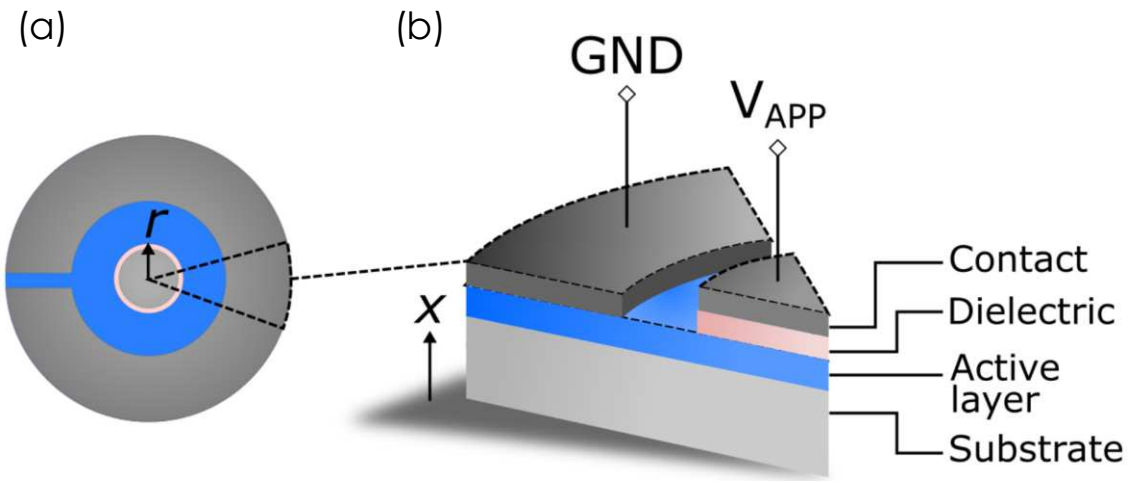


Figure 4.2: The structure of the circular MOSCAP (a) as in a top-down view; and a cross-section slice of showing its constituent layers. In this work, the substrate is sapphire, the active layer is a 30 nm of PEALD ZnO, followed by PEALD HfO_2 and Cr and the gate metal. The x direction trackes the thickness or depth of the structure, while the *r* tracks the lateral dimension.

4.1.3 LAYER DESCRIPTION

A thin ZnO-film was deposited on a sapphire substrate via plasma atomic layer deposition (PEALD) at a temperature of 200 °C. For the dielectric layer, PEALD high-κ hafnium oxide (HfO_2) grown at 100 °C was grown on top of the active film. The HfO_2 recipe used in this experimental setup has been well-characterized in previous studies where it has shown respectable behavior with gallium nitride MOSCAPs [**31**]. Sputtered chromium (Cr) was used as the gate contact with a total of 100 nm deposited, thus completing the MOSCAP.

4.1.4 EXPERIMENTAL RESULTS

The MOSCAPs were measured using the Capacitance-Voltage (CV) unit Keithley 4200 Semiconductor Characterization System (SCS). Both V_{APP} and small signal voltage 30 mV_{AC} at 10 kHz was applied at the inner contact where the channel was formed. Figure **4.3** shows the resulting area-normalized CV-sweeps for 58, 40 and 30 cycle HfO_2 on ZnO films.

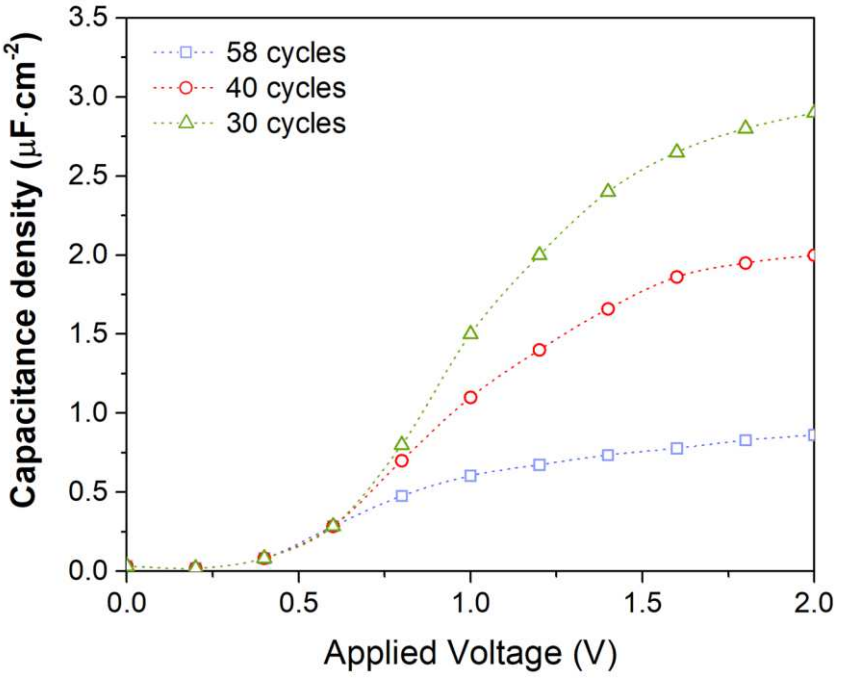


Figure 4.3: The CV measurement of 58, 40 and 30 cycles of HfO_2 measured from 0 V to 2 V at 10kHz frequency with an AC voltage of 30 mV_{AC}. All three cycles were grown on the same layer with the bottom adjacent layer being 30 nm of PEALD ZnO.

While the expected trend of increasing capacitance is observed as the insulator layer is thinned, a closer examination revealed thickness alone could not account for the changes in capacitance. Using the conventional depletion model, the dielectric constant ε_{ox} was extracted using Eqn (**4.2**) and listed in Table **4.1**. The dielectric parameter extraction revealed that higher number of deposition cycles degraded the electrical performance of the dielectric and the degradation was not directly inversely proportional to the thickness. In this study, at a 30 cycles dielectric constant ε_{ox} was reported at 22 with a capacitance density of 2.9 μm·cm^{-2}. An ε_{ox} = 18.5 was extracted at 40 cycles with a C_{den} = 2 μm·cm^{-2}, and finally 58 cycles yield an ε_{ox} = 10.1 with 0.86 μm·cm^{-2}. To put it in perspective, Table **4.1** also reveals the expected capacitance density if the electric permittivity was constant at ε_{ox} = 22. A rough estimation of the calculation was determined using the equation below:

$$\frac{1}{C_{den}} = \frac{\varepsilon_{OX}}{t_{OX}} + \frac{\varepsilon_{ZnO}}{t_{channel}} \tag{4.4}$$

Where $t_{channel}$ is the centroid of the electron gas channel distribution formed beneath the MIS interface and is approximated at 1 nm to 1.4 nm and an electric permittivity of 8.6 was used for ZnO ε_{ZnO}. In the later sections, the exact value for $t_{channel}$ will be explored and determined with the Schrödinger-Poisson model.

Previously reported studies of HfO_2 have provided evidence of crystallinity dependence on oxide film thickness for vacuum processes [**32**,**33**]. Regions of crystal order were formed as the thickness of the layer increased resulting in a mixture of an amorphous and polycrystalline film. Further to that, electric permittivity dependence on crystallinity of HfO_2 have been observed experimentally in other reports and thus our findings here are not unique [**34**,**36**,**37**,**38**]. Though in this work, the nature of this dynamic dielectric constant is not a subject of further interest, that may depend on the process parameters used to synthesize the oxide films. Nonetheless, its affect on the MOSCAP CV characteristics are clear.

Table 4.1: Extracted dielectric constant from measured capacitance values compared to expected values

Parameters	**58 cycles**	**40 cycles**	**30 cycles**
Thickness	8.7 nm	5.6 nm	4 nm
Measured Capacitance	0.86 μF·cm^{-2}	2 μF·cF^{-2}	2.9 μF·cm^{-2}
Extracted Dielectric† ε_{ox}	10.1	18.5	22
Expected Capacitance‡	1.59 μF·cm^{-2}	2.28 μF·cm^{-2}	2.9 μF·cm^{-2}

†These values are extracted using conventional techniques as described by Hilibrand and Gold/capacitance depletion model.

‡Assuming a dielectric constant of 22, the same as the 30 cycles.

4.1.5 1D SCHRÖDINGER-POISSON MODEL

When the MOSCAP operates in either strong accumulator or inversion, a high concentration of carriers populates the region near the interface between the insulator and semiconductor film. Classical models using the only the Poisson self-consistent equation assume a continuous energy spectrum and thus incorrectly predicts a distribution of the carriers along the film beginning at the onset of the interface and eventually tapering as the depths of the semiconductor's depletion region are reached [**40**]. However, because of the high barrier potential of the insulator, the carriers experience barrier confinement and as a result can exist only in quantized states (Figure **4.4**). This restriction is accounted for in the Schrödinger description [**41**,**42**]. Solving these two equations simultaneously analytically remains a significant challenge today, hence an iterative solution was developed based on previous work [**42**,**43**,**44**,**45**,**46**] and improved upon for ultrathin-film applications.

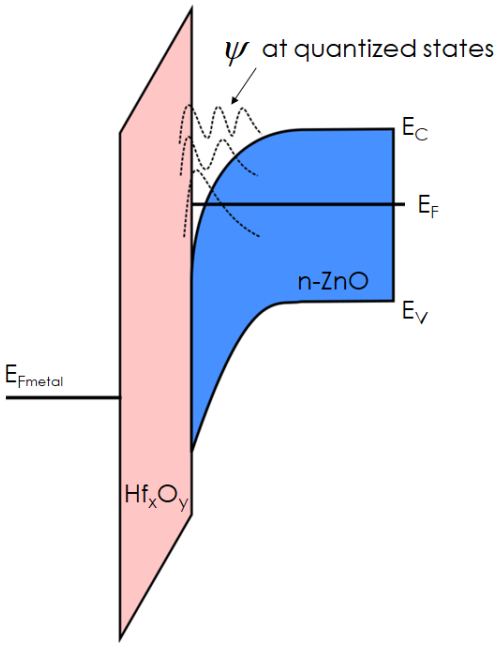


Figure 4.4: Band diagram of accumulation-biased MOSCAP. The wavefunction ψ exists in quantized energy states and dictate the distribution of carriers in the triangular well formed by the high barrier potential of the dielectric layer and surface band banding of ZnO.

The solver arrives at the solution by evaluating Fermi-Dirac statistics, Schrödinger and Poisson equation self-consistently. The two guiding expressions are given as follows.

For a single-electron one-dimensional the Schrödinger equation can be expressed as:

$$-\left(\frac{\hbar^2}{2}\frac{1}{m_e^*}\frac{d^2}{dx^2}-V(x)\right)\psi(x)=E\psi(x) \tag{4.5}$$

Where E is the energy, ψ is the wave function, an asterixis (*) denotation is simply the effective mass scalar multiplied by m_o and V is the potential.

Poisson's equation Eqn (**4.6**) relates the charge density ρ with potential V.

$$\frac{d^2}{dx^2}V(x)=-\frac{\rho(x)}{\varepsilon_S} \tag{4.6}$$

Beginning with the given ionized dopant concentration N_D, the equilibrium electron density n_o is calculated:

$$n_o=\frac{N_D}{2}+\sqrt{\left(\frac{N_D}{2}\right)^2+n_i^2} \tag{4.7}$$

Where n_i is the intrinsic carrier concentration within the semiconductor and is determined by the bandgap and the density of states at the conduction N_C and valance N_V band-edge of the active thin-film E_G. This is expressed below.

$$n_i^2=N_C N_V e^{E_G/k_B T} \tag{4.8}$$

Three-dimensional non-degenerate semiconductor description are given in Eqn (**4.9**) and (**4.10**) for N_C and N_V which depend on the effective mass of electrons m_e and holes m_h, respectively.

$$N_C = \frac{1}{\sqrt{2}}\left(\frac{m_o m_e k_B T}{\pi\hbar^2}\right)^{3/2} \tag{4.9}$$

$$N_V = \frac{1}{\sqrt{2}}\left(\frac{m_o m_h k_B T}{\pi\hbar^2}\right)^{3/2} \tag{4.10}$$

With the components calculated, the probabilistic carrier distribution over the energy states within the bandgap is derived from the Fermi-Dirac equation. With respect to the conduction E_C or valence band $-E_V$ this can be easily evaluated:

$$E_f = E_C + k_B T \ln\frac{n_o}{n_i} \tag{4.11}$$

After the determining the Fermi-level, we then proceed to solve the Schrodinger equation. The solution for Eqn (**4.5**) are the bound states E which are then used to evaluate the carrier density distribution within the film. As we are solving for the majority carriers in an n-type accumulation-mode MOSCAP, we correlate electron density $n(x)$ with a position along the semiconductor film for each bound state i as follows:

$$n(x) = \int_{E_C}^{\infty} \sum_v g_{v,n} \frac{m_{n,v}}{\hbar^2\pi} \sum_i \left(E_f - E_{n,i}\right)\left|\psi_{n,i}(x)\right|^2 \cdot f(E)\,dE \tag{4.12}$$

And for hole density *p(x)*:

$$p(x) = \int_{\infty}^{E_V} \sum_{v} g_{v,p} \frac{m_{p,v}}{\hbar^2 \pi} \sum_{i} \left(E_f - E_{p,i}\right) \left|\psi_{p,i}(x)\right|^2 \cdot \left[1 - f(E)\right] dE \tag{4.13}$$

Where g_v is the corresponding degeneracy for each valley *v* and *f(E)* is simply the Fermi-Dirac distribution:

$$f(E) = 1 + e^{\frac{E_f - E}{k_B T}} \tag{4.14}$$

To relate this back to Poisson equation, we began by further decomposing the charge density in Equation (**4.6**) to its two separate carriers, electrons *n* and holes *p*, and to the ionized dopants, donors $+N_D$ and acceptors $-N_D$.

$$\rho(x) = q\left[-n(x) + p(x) + N_D(x) - N_A(x)\right] \tag{4.15}$$

The ionized dopant distribution is a design parameter which is determined *a priori* to the behavior of the carriers. For most models, the dopant distribution is assumed to be independent of its position of x, i.e. uniform doping profile throughout the film. As it will be demonstrated later, this assumption fails to model some of the key regions in a CV-curve for thin-film semiconductors and the model is revised to consider non-uniform distributions.

What must first be determined is the manner in which the conduction and valence band edge are perturbed by the electrostatic potential *V(x)* distributed throughout the film. Beginning from the flatband case of both the conduction $E_{C,FB}$ and valence band edge $E_{V,FB}$ are affected by *V(x)* through the following relationship:

$$E_C(x) = E_{C,FB} - qV(x) \tag{4.16}$$

$$E_V(x) = E_{V,FB} - qV(x) \tag{4.17}$$

Using the parabolic band approximation for a volumetric density of states DOS^{3D} , both *n* and *p* are expressed as:

$$DOS_n^{3D} = \sum_v \frac{g_v m_{e,v}^{*3/2}}{\pi^2 \hbar^2} \sqrt{2\left(E - E_C(x)\right)} \tag{4.18}$$

$$DOS_p^{3D} = \sum_v \frac{g_v m_{p,v}^{*3/2}}{\pi^2 \hbar^2} \sqrt{2\left(E_V(x) - E\right)} \tag{4.19}$$

Subsequently, the location of the carriers can be determined by correlating the expressions above for *n* and *p* respectively.

$$n(x) = \int_{E_C}^{\infty} DOS_n^{3D}(E,x) f(E)\, dE \tag{4.20}$$

$$p(x) = \int_{\infty}^{E_V} DOS_p^{3D}(E,x)\left[1 - f(E)\right] dE \tag{4.21}$$

The Schrödinger solution for Eqn (**4.12**) or (**4.13**) are compared with the results of Eqn (**4.20**) or (**4.21**) of the Poisson equation, along with the potential *V*(x). Figure **4.5** shows the flowchart, with self-consistent solution accepted by applying Newton-Rhapson root method for *V*(x) guesses. Note that the ϵ is a very small number (chosen to be 1×10^{-12} here).

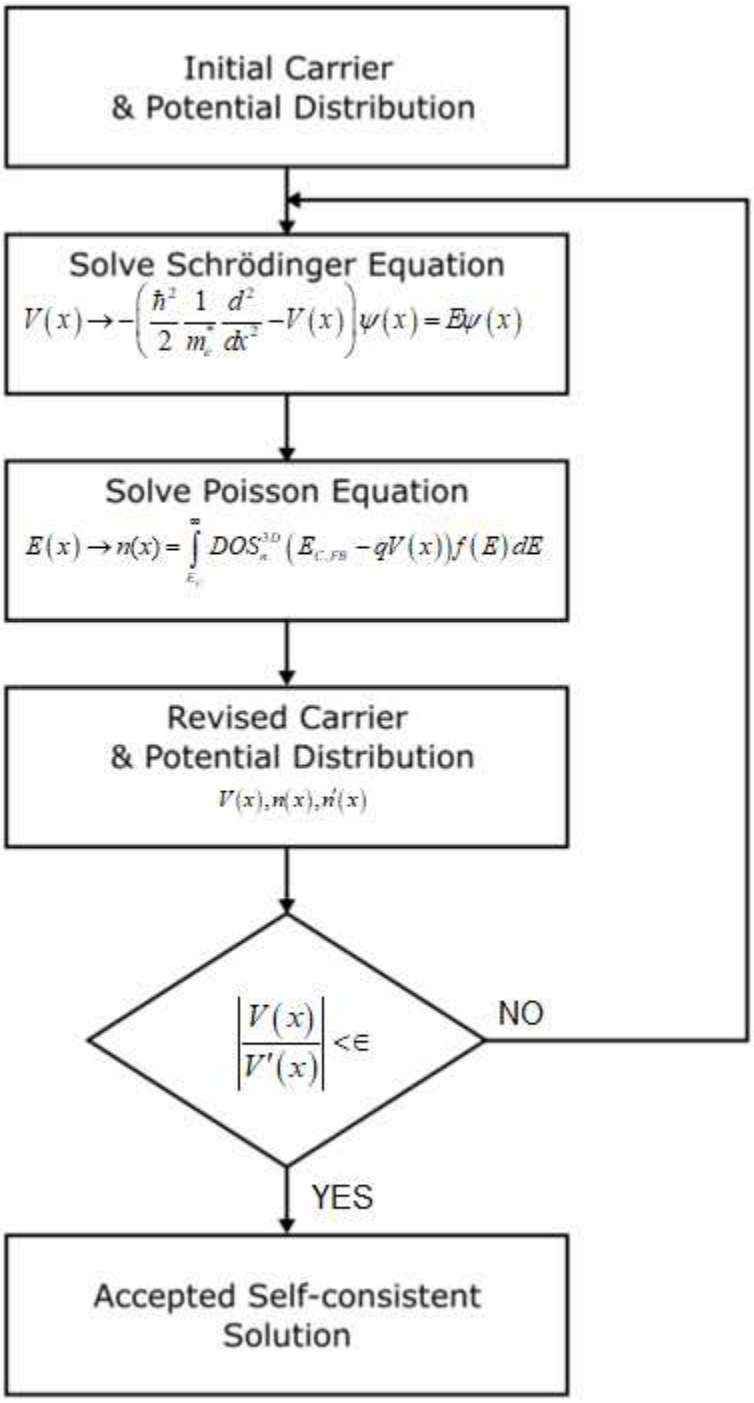


Figure 4.5: Schrödinger-Poisson self-consistent flow chart. Initial guesses are made for both initial carrier and potential distribution and calculated first with the Schrödinger equation. The solution is then applied to the Poisson-equation. The carrier and the potential solution are combined to give a revised solution. If the new potential correction is less that ϵ, then the solution is as accepted as self-consistent.

4.2 CAPACITANCE MODEL FOR THIN-FILM MOS

4.2.1 TRADTIONAL CAPACITANCE EXTRACTION

The traditional capacitance is evaluated based on the dynamic behavior of the carriers with respect to the changing gate potential. As all components of Eqn (**4.15**) have been solved, from the net charge ρ the total charge density Q_{TOT} can easily determined by taking the integral over the its distribution through the film.

$$Q_{TOT} = \int_0^{t_s} \rho \cdot dx \tag{4.22}$$

We also note that the voltage applied the gate terminal V_{APP} is composed of flatband voltage V_{FB}, the surface potential φ_S at the MIS interface and the drop in potential over the insulator itself V_{OX}.

$$V_{APP} = V_{FB} + \varphi_S + V_{OX} \tag{4.23}$$

Due to boundary conditions, both the potential and the electric field ξ at the onset of the semiconductor must be the same as the terminus of the oxide.

Therefore:

$$V_{OX} = \int_0^{t_{ox}} \xi_i \cdot dx \tag{4.24}$$

Both the change in Q_{TOT} is tracked as the potential is changed and satisfying eqn (**4.1**) and completing the extraction of the CV in an MIS structure.

When using the extracted dielectric constant provided in Table **4.1** and comparing the measured results versus the max capacitance at accumulation extracted via the traditional model, we found that the model underestimated the peak capacitance. This implied that

the dielectric values using equation (**4.4**) were lower than the actual values. However, what the value was not independent of the insulator thickness. As a first approach to resolve the difference with the model and experiment, we targeted an agreement between them with respect to the maximum capacitance at accumulation C_{ACC}.

The new values were 58, 40 and 30 cycles were 12, 25 and 29, respectively and are recorded in Table **4.2**. The decreasing dielectric constant, as explained in Section **4.1.4**, was due to the increase in regions of polycrystallinity in the oxide as the ALD cycle count became larger. These values were comparable with this group's previous work with a similar high-κ oxide showing better performance on the wide-bandgap semiconductor gallium nitride GaN [**31**]. The high-κ used was zirconium oxide with similar processing parameters as the HfO_2 used in this study. Because the oxide was deposited on a thick GaN film, the extracted dielectric constant from the measured capacitance were close to its true value because the depletion width was less than the thickness of the GaN body (~5 μm on sapphire).

For semiconductor films with thicknesses that are much less than its theoretical depletion width, traditional dielectric extraction methods are not valid, and are often underestimated as demonstrated in Table **4.1**. The ALD ZnO film deposited on sapphire which was only t_{ZnO} = 30 nm. In Table **4.2**, there is another parameter related to the ZnO thickness, t_{eff}. Due to the biasing scheme of the planar MOSCAP, the t_{eff} was not equal to the vertical thickness t_{ZnO}. The reason for this discrepancy is further explained in Section **4.2.5**. In brief, due to the planar biasing scheme of the MOSCAP, the electric field in ZnO contained both a vertical component which equaled t_{ZnO} and a horizontal component, which combined equaled t_{eff}.

Table 4.2: Full list of parameters used for simulation, including electrical environment, HfO_2 and ZnO material materials.

Parameters		58 cycles	40 cycles	30 cycles
Applied voltage range			0 V – 2 V	
Initial Doping Concentration			5×10^{16} cm^{-3}	
Temperature			300 K	
V_{FB}		0.59 V	0.65 V	0.65 V
	HfO_2			
	t_{ox}	8.7 nm	5.6 nm	4 nm
	ε_{OX}	12	25	29
	ZnO			
	t_{ZnO}	30 nm	30 nm	30 nm
	t_{eff}	50 nm	48 nm	45 nm
	ε_S		8.6	
	E_G		3.31 eV	
	$m_{e,\,low}$		0.21	
	$m_{e,high}$		0.23	
	$m_{d,low}$		0.04	
	$m_{d,high}$		0.55	
	g_1		1	
	g_2		6	

Despite the agreement in C_{ACC}, obvious problems in fitting remained and is shown clearly in Figure **4.6** for all three insulator thicknesses. The depletion region spanning the voltage range where the capacitance transitioned from its minimum to C_{ACC} increased at a much faster rate with the conventional model than the experimental measurements. We called the voltage when the depletion rate changes the 'pivot voltage'. Previously reported model-experimental comparisons at depletion regions have shown agreement in the rate of transition for high quality dielectrics and insulator-semiconductor interfaces [**47**,**48**,**49**]. Thus, we do not attribute it to a fundamental failure in the extraction. What the analysis did reveal was the incompleteness of the model as it stands. Thus, we further explored the potential affects of both a non-uniform dopant profile and the geometrical thinness of the film.

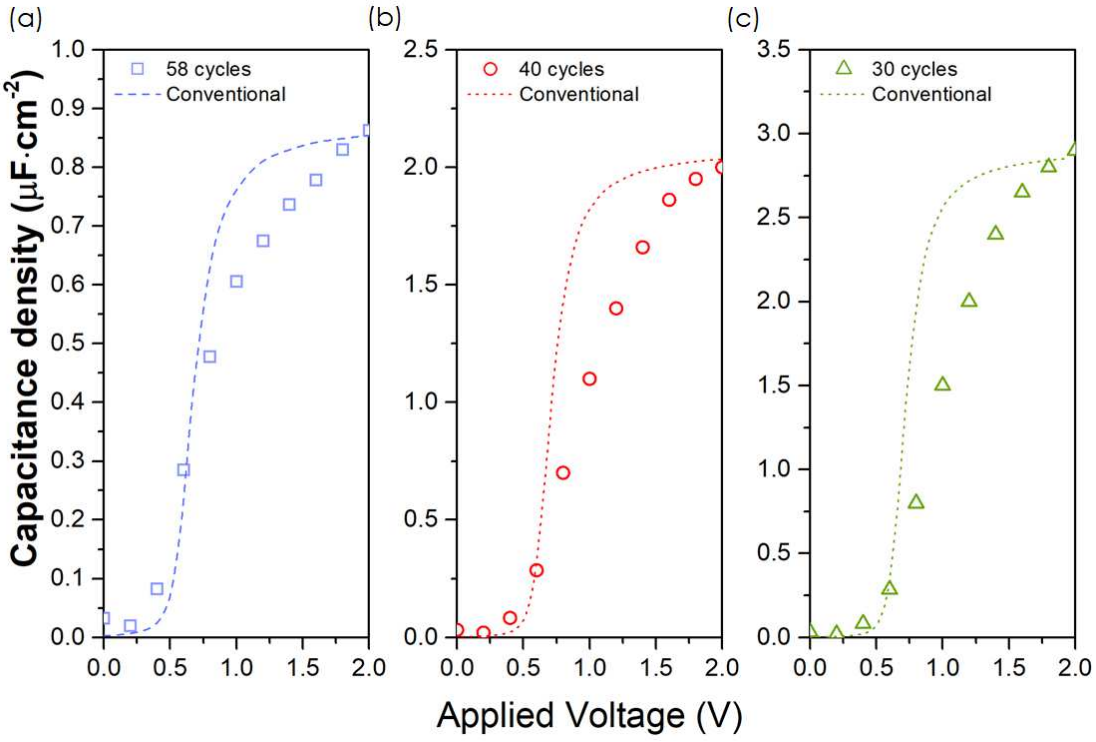


Figure 4.6: Comparison between measurement and conventional CV model for (a) 58 cycles of HfO_2; (b) 40 cycles; and (c) 30 cycles. Overall, the fitting is demonstrably poor, even with the dielectric constant corrected matching C_{ACC}. The main issue comes with the difference in rate of depletion which cannot be explained by defects or parasitic components alone.

Presence of defects has not shown to significantly decrease the depletion rate [50,51,52,53,54]. Interfacial defects D_{IT} have been shown to cause deviations from ideal CV characteristics in two ways depending on their distribution over the forbidden energy gap: for symmetrical distribution about the band edges, the minimum depletion capacitance C_{min} increases significantly implying that its behavior is analogous to capacitor parallel to C_S; non-uniformity in D_{IT} manifested as kinks or bumps at the depletion region, with a more rapid change from deep depletion to the defect-induced bump than the ideal CV, and thereafter rises at a similar rate with slight shift in voltage. Traps within the oxide itself D_{OT} causes slight increase in C_{MIN} compared to interfacial defects indicating a parallel capacitor component to C_{OX}. In addition, both defect species causes hysteresis in CV loop measurement. The rate of depletion, however, remain essentially the same. In contrast to the thin-film ZnO measured in this study, the slow depletion rate cannot be palpably explained by D_{IT} or D_{OT}, though capacitance-frequency measurements have shown the presence of D_{IT}. The possibility of a defect incorporated parallel capacitance component can be considered minimal since there is a general agreement at C_{MIN} for simulation and experimental (Figure 4.7). Hence other causes were explored.

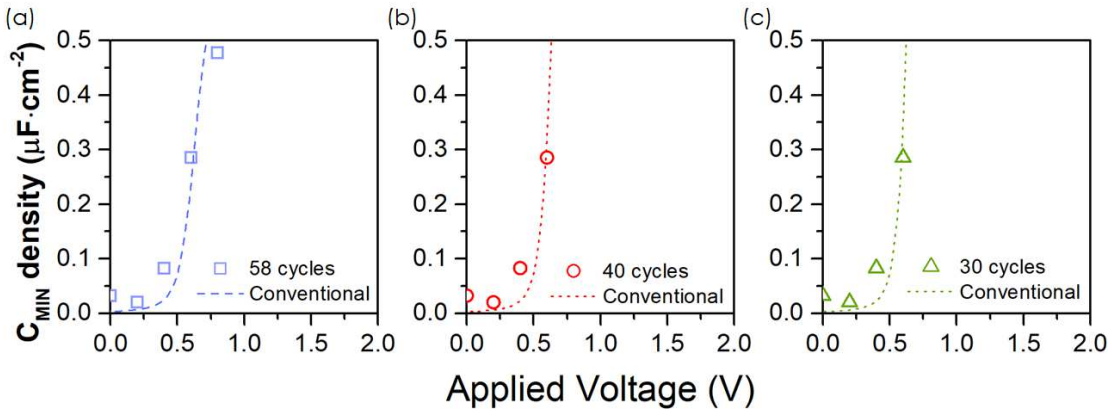


Figure 4.7: Deep depletion region comparison between measurement and conventional CV model for (a) 58 cycles of HfO_2; (b) 40 cycles; and (c) 30 cycles. The absolute C_{MIN} of both measured and model data are in respectable agreement, implying that the defect level are not heavily influencing the deep depletion region.

4.2.2 THIN-FILM GEOMETRICAL EFFECTS

A lower rate of depletion between C_{ACC} and C_{MIN} have been observed in the past. For instance, polysilicon gates in Si MOS exhibited slowed depletion transitions which could not be explained by detects or series resistance. The electrostatic cause was pinpointed to the depletion at the surface of the highly degenerate polysilicon gates interfacing with the insulator. The previous studies showed that when poly-depletion was accounted for in the Schrodinger-Poisson models, the overall CV of the MOS devices showed stronger agreement at the depletion region. Although slight variances were observed between models, this was due to the differences in the quantization or parameterizaton of the depleted gate material surface [**55**].

For true metal gates, this affect was not observed. Yet, in the ultrathin films measured in this study, the depletion rate is much more dramatic than what could be attributed to even a slight depletion at the opposing surface interfacing the insulator.

Capacitance-voltage modeling using conventional approaches do not consider geometrical constraints because they were developed for semiconductors whose body thickness far exceeded the maximum depletion thickness the applied electric field could achieve. This assumption yielded accurate MOS CV models which depended only on the insulator characteristics and the dynamic behavior of the charge, with the body of the semiconductor behaving effectively as a continuous contact to the ground terminal. This cannot be assumed in a thin-film semiconductor MOS because the potential is concentrated at such small lengths that the electric field is able to fully deplete the film.

Furthermore, from Figure **4.7** the voltage at which the capacitance 'pivots' from C_{MIN} is worth noting (around 0.6 V). The pivot voltage is the voltage where the capacitance transitioned from the deep-depletion to depletion region. For a uniformly distributed doping

profile assumed here, the modeled pivot voltage is slightly higher than what was measured experimentally. Tuning V_{FB} alone did not explain CV behavior as the MOS transitioned from C_{MIN} to C_{DEP}. The common assumption for depletion model behavior is the uniform distribution of dopants. In this analysis, we discard this assumption and incorporate non-uniform dopant profile with conventional modeling techniques. As it will be later demonstrated, dopant non-uniformity becomes an important factor of the overall CV behavior when the thickness of the film can no longer be ignored.

4.2.3 *IMPROVED SP MODEL*

Due to the dependence on the geometrical thickness of the active layer, the series capacitive components model of equation (**4.2**) and (**4.4**) have to be revisited.

Of interest in particular is $t_{channel}$ which was introduced to explain a C_{MAX} which did not equal the C_{OX} value as a result of non-classical effects at the interface in a basic circuit. The C_S value dependence was only tracked for either fully accumulated or fully inverted structures.

In the improved model, we observe the C_S through the depletion and accumulation voltage range. Since a channel is not necessarily fully formed, the centroid of the corresponding carriers t_C was tracked. Therefore, equation (**4.4**) for ZnO is revised as follows:

$$\frac{1}{C_{den}} = \frac{\varepsilon_{OX}}{t_{OX}} + \frac{\varepsilon_{ZnO}}{t_C} \tag{4.25}$$

The carrier centroids t_C are calculated based on the work of King, *et* al (1998) which was simply [**56**]:

$$t_C = \frac{\int \rho_e(x) \cdot x \, \mathrm{dx}}{\int \rho_e(x) \mathrm{dx}} \tag{4.26}$$

Where ρ_e is the electron distribution of the film as solved by the Schrödinger-Poisson self-consistent model. With this, the capacitance density C_{DEN} is modeled from 0 V to 2 V as the centroid varies with voltage.

The CV output was also impacted by the initial ionic charge distribution throughout the ultrathin semiconductor. Most models assumed an evenly distributed dopant profile, but in thin-films which do not normally exhibit predictable crystal order, such an assumption creates problems. For instance, there continues to be on-going debate with intrinsic ZnO and the source of its unintentional dopants. Numerous mechanisms have been proposed, including the relationship of oxygen with zinc and the atmosphere or the presence of hydrogen [**57**,**58**,**59**,**60**,**61**]. Work presented here will not attempt explain the presence of unintentionally dopants in thin-films such as ZnO but perhaps its distribution may give further insight into this on-going topic of research.

Three cases generally sketched out in Figure **4.8** were considered for the dopant profile: uniform, linear and exponential.

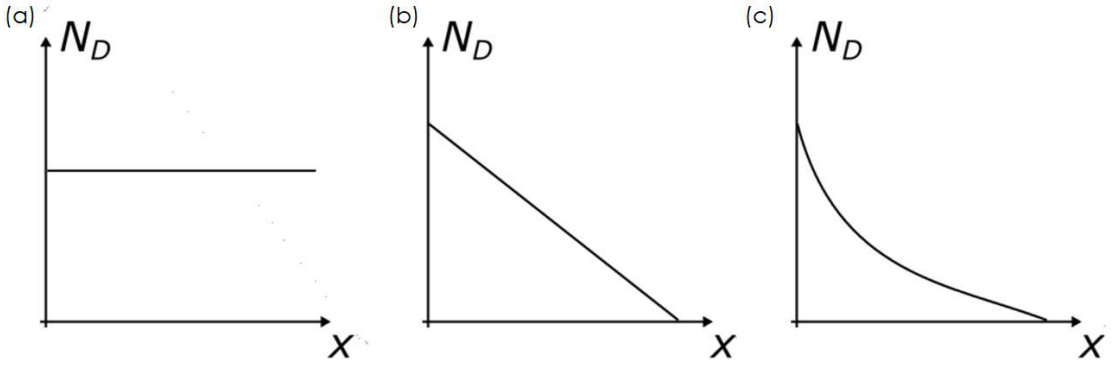


Figure 4.8: The dopant profile considered in this work include (a) uniform, which is the most common assumption, and the non-uniform profiles which are distributed (b) linearly and (c) exponentially. For the revised model, non-uniform distribution had to be considered in order to predict the CV behavior below 0.6V.

The linear and exponential profiles were predicted to be a more accurate portrayal of the equilibrium doping distribution due to several observations noted in literature that a higher concentration of unintentional dopants, particularly related to hydrogen, were located near the semiconductor surface [**62**,**63**,**64**]. In fact, further revisions were made with the non-uniform profiles which suggested that the surface of the ZnO was about an order higher in dopant concentration than throughout rest of the film. This will be discussed in later sections.

Within the revised model developed here, t_C played a crucial role in the CV characteristics of the MOSCAP. Moreover, the furthest that t_C can reach away from the insulator-semiconductor interface is the edge of the semiconductor. In other words, the full thickness of the active layer t_S. Thus, we can see how the dimensions of the ultrathin film plays a significant role in the output capacitance behavior.

We saw why the initial dopant profile could not be ignored when considering the consequence of assuming a uniform doping distribution: C_{MIN} increased substantially when film thickness was factored in and showed extremely poor agreement with the over all measured CV data. Figure **4.9** clearly illustrated that non-uniform dopant distribution is likely the cause of the behavior seen at lower voltages about the deep depletion region.

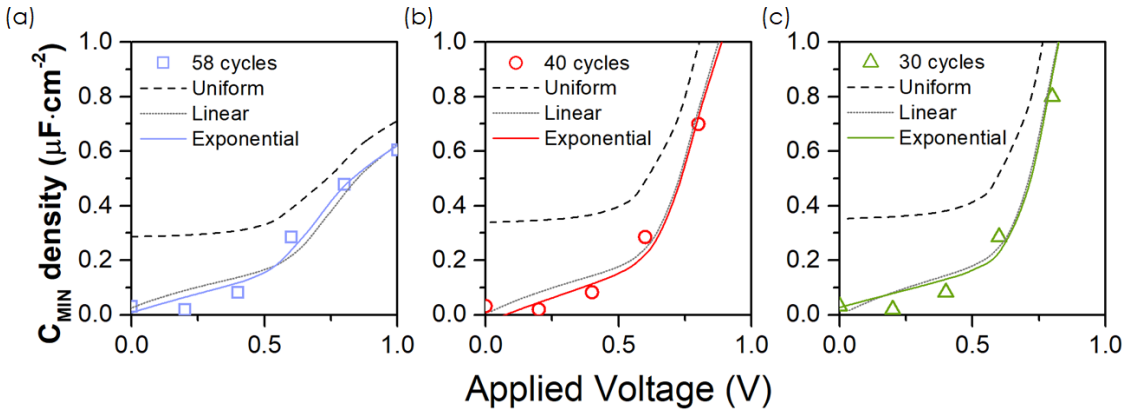


Figure 4.9: Using the modified model, various dopant profiles are simulated and compared with deep depletion region for (a) 58 cycles of HfO_2; (b) 40 cycles; and (c) 30 cycles measured data. Uniform distribution failed to match C_{MIN}, but a revised linear and exponential model showed better fits including predicting the correct pivot voltage. The revised non-uniform distributions are discussed in Section **4.2.5**.

Both non-uniform profiles showed much better fitting to the measured data: the linear and exponential cases were able to emulate the pivot voltage that distinguishes the floor capacitance region from the onset of depletion. As stated previously, both the non-uniformities were similarly profiled in that there was a higher concentration of dopants at the surface than along the rest of the semiconductor. Though the fit was not perfect, the exponential distribution showed slightly improved agreement than its linear counterpart. This simulation strongly suggests that the true dopant distribution must be non-uniform and non-linear and can be used to explain the true nature of unintentional doping in thin-films grown via ALD, and perhaps other growth techniques as well. Since the best fitting was found to be the exponential profile, it was used to extract the free electron distribution from the measured voltage range in a ZnO film. This is shown for all HfO_2 thicknesses from 0 V to 2 V in Figures **4.10** (58 cycles), **4.11** (40 cycles) and **4.12** (30 cycles).

Using equation (**4.26**), we could determine the centroid of the distribution and it was subsequently tracked throughout the simulated voltage range. This analysis revealed that the carrier distribution is not uniform even as we approach V_{FB} as one would observe for a uniformly distributed dopant profile. Instead, as can be inferred from Figures **4.10c**, **4.11c** and **4.12c** for 58, 40 and 40 cycles, the flatband free carrier distribution takes on a 'saddle' form where the concentration are highest but equal to the set doping concentration at the onset of the MOS interface and the edge of the semiconductor i.e. the semiconductor ground terminal. An example of this 'saddle' near-flatband distribution is shown for 30 cycles in Figure **4.13**.

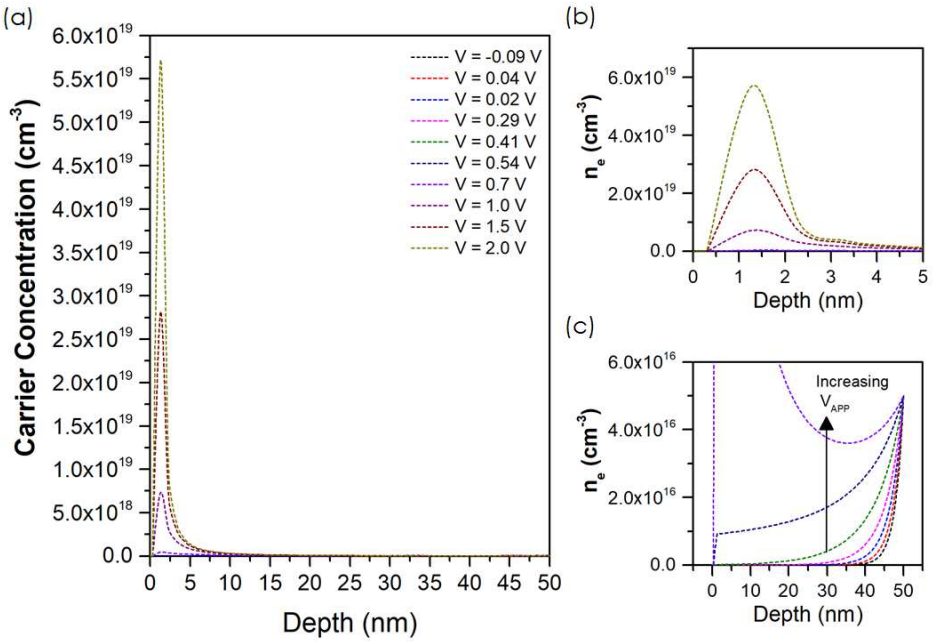


Figure 4.10: The 58 cycles HfO_2 electron distribution within the ZnO active layer at various applied biases V_{APP}. The overall distribution is shown in (a). A magnified view within the first 5 nm from the surface is shown in (b) at accumulation voltages and (c) is the overall distribution at voltages from depletion to the onset of accumulation. The centroid at 2V is ~1.5 nm for 58 cycles.

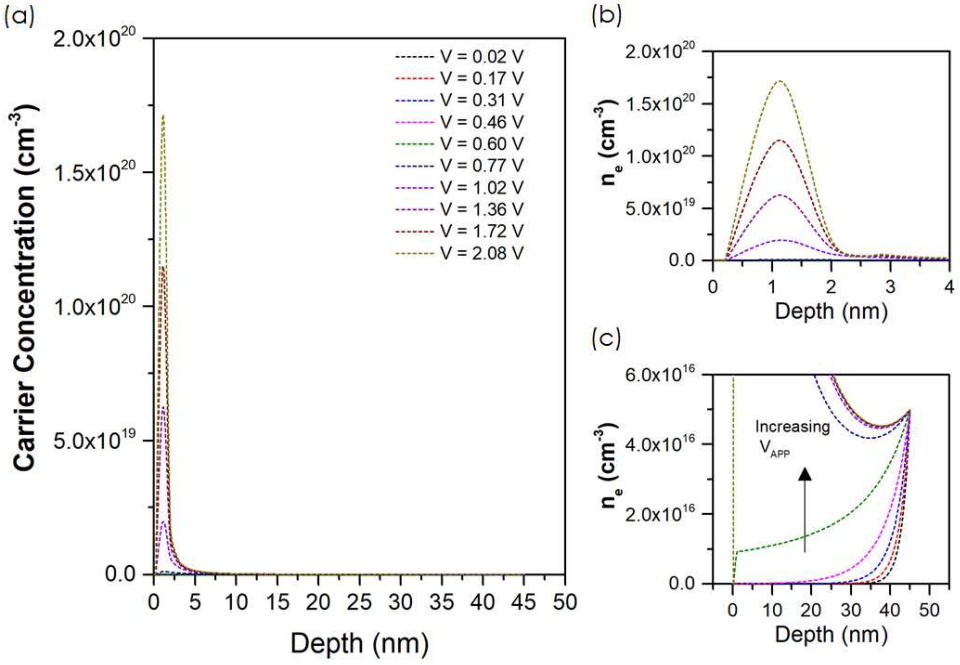


Figure 4.11: The 40 cycles HfO_2 electron distribution within the ZnO active layer at various applied biases V_{APP}. The overall distribution is shown in (a). A magnified view within the first 5 nm from the surface is shown in (b) at accumulation voltages and (c) is the overall distribution at voltages from depletion to the onset of accumulation. The centroid at 2V ~1.2 V for 40 cycles.

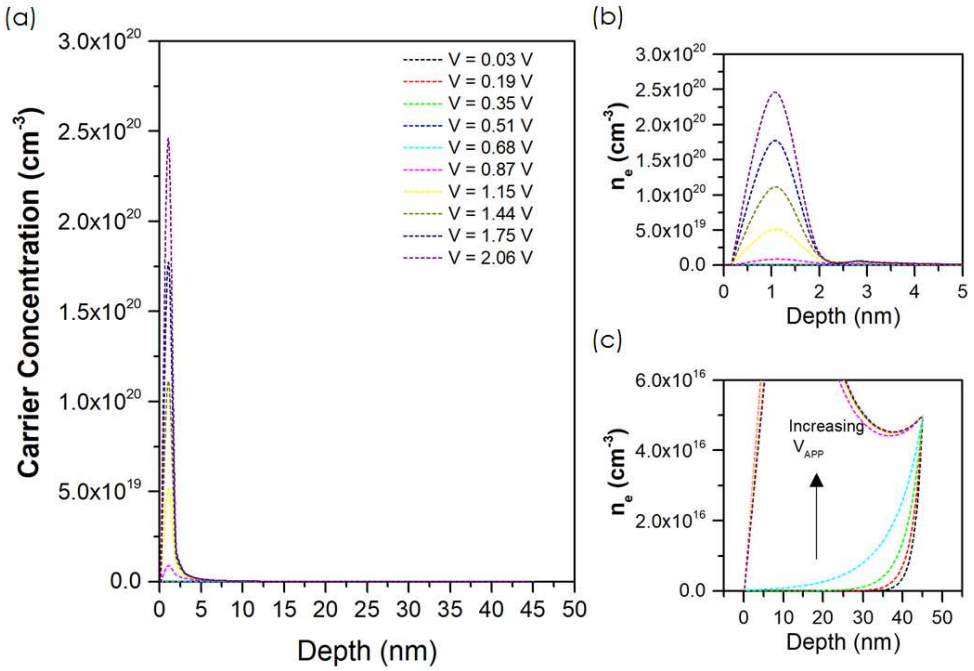


Figure 4.12: The 30 cycles HfO_2 electron distribution within the ZnO active layer at various applied biases V_{APP}. The overall distribution is shown in (a). A magnified view within the first 5 nm from the surface is shown in (b) at accumulation voltages and (c) is the overall distribution at voltages from depletion to the onset of accumulation. The centroid at 2V ~1.1 V for 30 cycles.

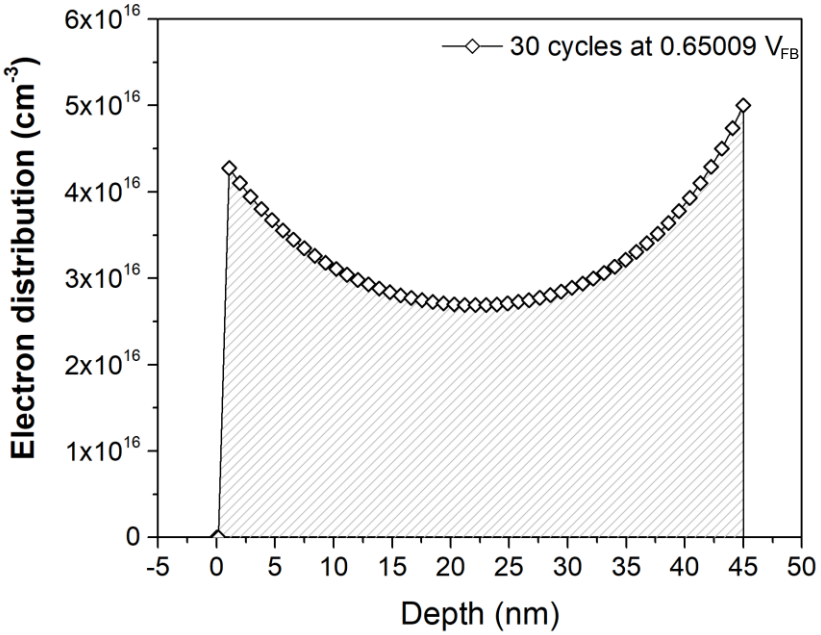


Figure 4.13: An example of the carrier distribution at flatband for 30 cycles HfO_2. In a uniform distribution, the carriers also be uniform, but in an exponentially-graded dopant profile, a 'saddle-like' electron distribution is revealed.

From Figure **4.14**, we see the centroid as a function of applied voltage. The flatband voltage for are indicated with the figures. Although 30 cycles and 40 cycles showed the same flatband voltage of V_{FB} = 0.65 V, 58 cycles was determined to be V_{FB} = 0.59 V. This is likely due to the additional ALD cycles changing the crystal properties of the HfO_2, as similarly reported in previous works for other processes [**32**,**33**]. The additional polycrystalline regions in the oxide changed the surface contact with the gate metal resulting in a lower flatband voltage.

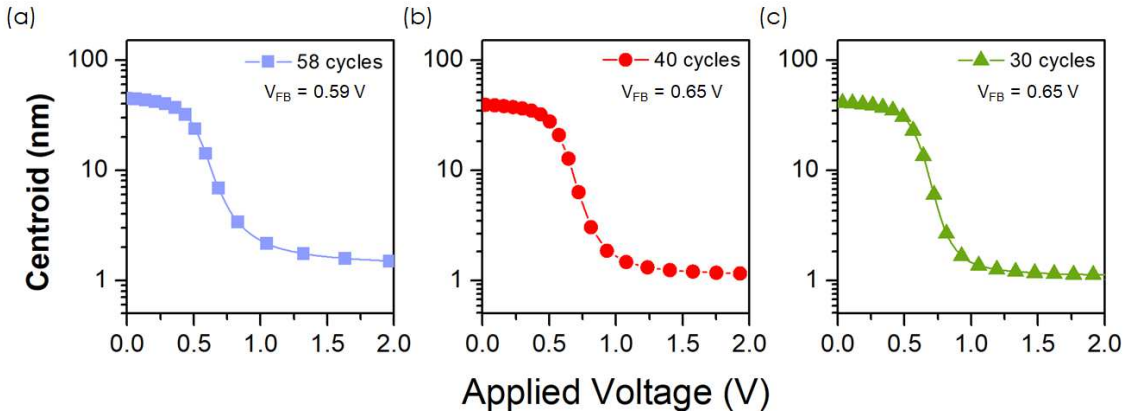


Figure 4.14: Calculated centroids for (a) 58 cycles of HfO_2; (b) 40 cycles; and (c) 30 cycles. As the voltage increases, the electrons become more concentrated at the insulator-semiconductor interface but does not reach interface due to quantum effects. The centroid location increases as the field reverse pushing the electrons to the opposite direction.

As expected, the above figures indicated that as we reach accumulation voltages, the carrier centroid approached the interface, but due to quantum mechanical effects as dictated by the wavefunction, it nevertheless does not reach the surface. The most dramatic change, of course, being at the depletion voltage range with the onset of the channel formation corresponding with flatband. An additional observation is that as the insulator thins in thickness, the centroid of the channel formed at accumulation approaches closer to the insulator-semiconductor interface. This behavior is expected as the strength of the field over the structure increases resulting in further confinement of the quantum. For ZnO, the electron concentration actually exceeded the density of states at the conduction band edge. As a

result, a portion of the total electron concentration must necessarily take up higher quantized energy levels. Its effects are revealed in the overall carrier distribution in Figures **4.10c**, **4.11c** and **4.12c**, where there exists a subtle secondary carrier 'bump' which follows the wavefunction of the second lowest energy level, and which only forms at higher fields when more carriers populate the accumulation layer.

The wavefunction and band bending for all three cycles are also shown in Figure **4.15** for an applied voltage of 2V.

At the accumulation voltage of about 2V, the channel centroid for 58 cycles was t_C = 1.4 nm, for 40 cycles t_C = 1.2 nm and for 30 cycles t_C = 1.1 nm. The depletion centroids about 0 V are also summarized in Table **4.3**. Compared to the accumulation channel centroid which was about <1.5 nm away from the insulator-semiconductor interface, the centroid at depletion voltage range was at least 4 nm to 5 nm away from the edge of the film but was modeled classically. Further improvements to the model would be needed to consider the non-classical physics that would effect at that region, such as an insulator, semiconductor or other non-ohmic substrates.

Table 4.3: Electron centroids at accumulation at the semiconductor surface and depletion centroids at the semiconductor edge

Parameters	**58 cycles**	**40 cycles**	**30 cycles**
Accumulation† t_C	1.4 nm	1.2 nm	1.1 nm
Depletion‡ t_C	45 nm	37.5 nm	41 nm

†Applied voltage was taken ~ 2 V.

‡Applied voltage was taken ~ 0V

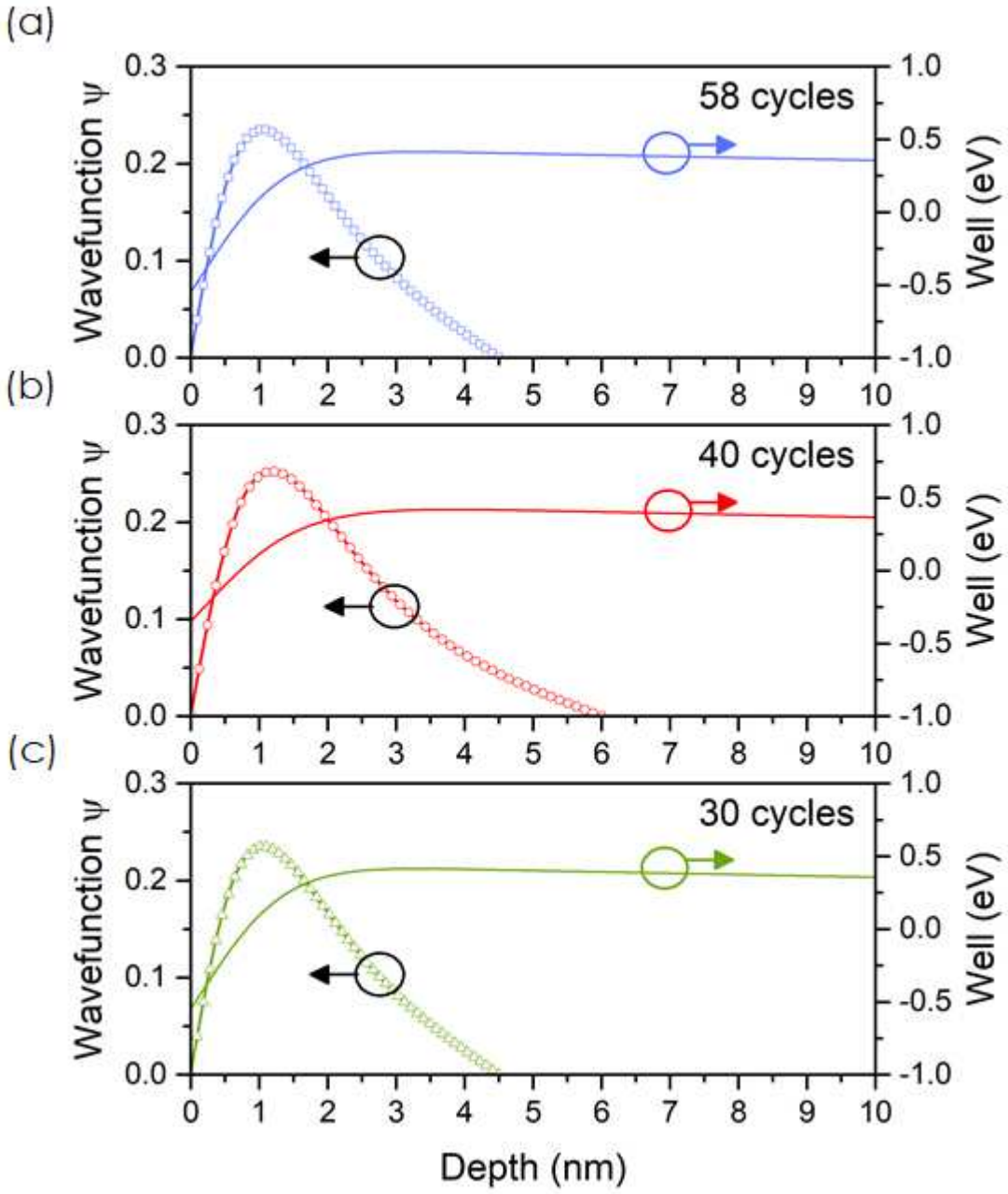


Figure 4.15: The lowest energy level wavefunction and the quantum well formed at 2V applied voltage for (a) 58 cycles of HfO_2; (b) 40 cycles; and (c) 30 cycles measured data with respect to applied voltage at the gate. Due to the quantum well formed from the band-bending of the conduction can, the corresponding electrons are distributed according to the wavefunction.

4.2.4 *MODEL COMPARISON*

The full measured voltage range from depletion to accumulation was assessed between the conventional CV extraction method and the modified method described in this work. Both methods were based on calculations constrained by a self-consistent Schrödinger-Poisson solution. From Figure **4.16**, it is clear, however, that the thickness of a film at ultrathin dimensions significantly shapes the capacitance-voltage characteristics of a MOS. More specifically, that the slower rate of transition of minimum capacitance to accumulation observed in the measured data cannot be explained by the charge reacting to a changing voltage. Unlike a bulk semiconductor, for a thin body, the electric field is strong enough to deplete the entire film. This means that at a high enough potential, the body of a very thin active layer will have a considerable effect on the capacitance response by mainly decreasing the rate of depletion by acting as another depleting component.

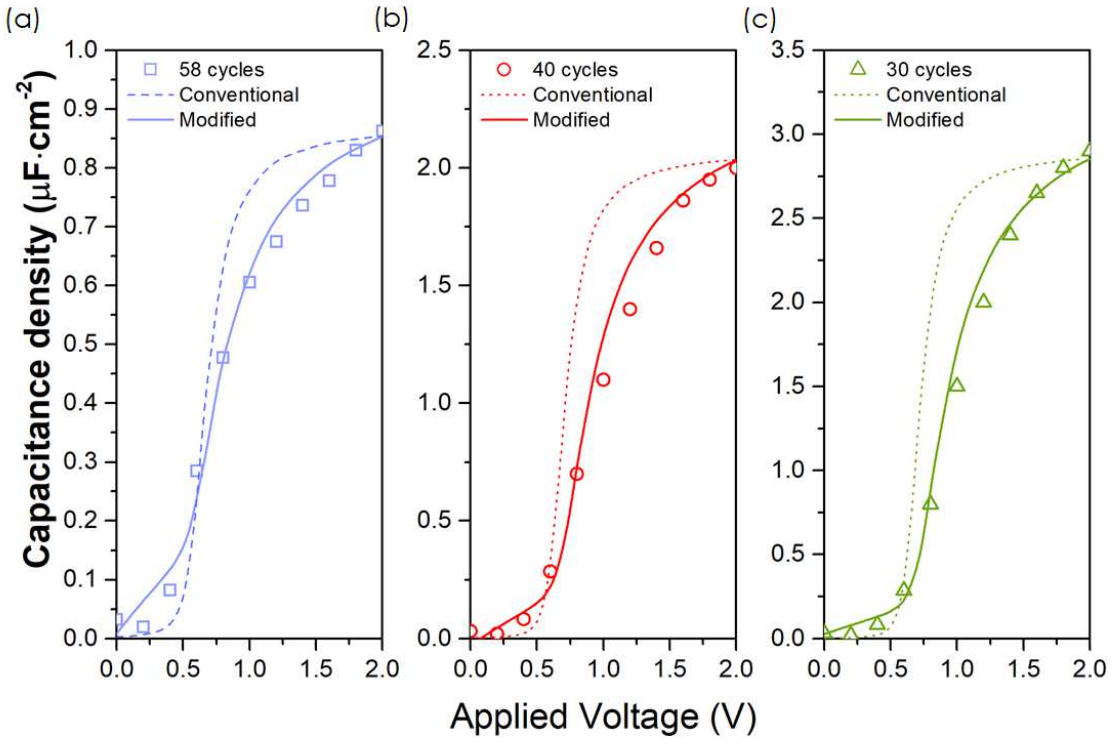


Figure 4.16: Comparison between measurement, conventional and modified CV model for (a) 58 cycles of HfO_2; (b) 40 cycles; and (c) 30 cycles. The modified which takes into consideration both the geometrical thickness of the film and an exponentially-graded doping shows a much improved measured-model matching than the conventional CV extraction method.

To understand which model showed better fitting, the CV curve was divided into two regions separated by the pivot voltage: 1) from the 0 V to the onset of depletion (deep-depletion reion) and 2) from the onset depletion to up to 2 V accumulation region. For the sake of analysis, for all three cycles, the pivot voltage was set at 0.6 V which is fairly consistent with measurement. At this voltage, the conventional model ('con.') underestimated the capacitance whereas the modified model ('mod.') slightly overestimated the response. Beyond the pivot voltage, both models to some extent overestimated the CV output, particularly in the depletion region. Table **4.4** shows the fitting break down of both regions and the strength of the accumulate fit for the full voltage range considered in this study as a percentage. The fit was evaluated such that the higher the percentage, the stronger the fit.

Table 4.4: Fitting comparison of conventional and modified models with measured data.

Voltage Region†	58 cycles		40 cycles		30 cycles	
	Con.	Mod.	Con.	Mod.	Con.	Mod.
≤ 0.6 V	72.3%	89.7%	58.1%	89.5%	54.3%	94.6%
≥ 0.6 V	82.5%	91.8%	67.4%	96.4%	60.7%	95.2%
Full	79.4%	91.1%	64%	94.3%	59.1%	95%

Fitting analysis revealed that for both voltage ranges bordering on 0.6 V and the full range, the modified model had a stronger agreement to the measured data than the conventional as expected. Furthermore, increase in insulator thickness t_{OX} and electric permittivity ε_{OX} corresponded with better agreement with the experimental and modified model data. These two parameters determine the electric field penetration into the semiconductor and played a role in the effective film thickness t_{eff} which will be discussed in the next section.

We also observed that overall the improved model fit better at voltages beyond the pivot than below. Although it resulted in poorer matching, this pattern was also observed for the conventional model. In fact, the fit at this region exceeded 90% for the modified model, with the mismatch mainly attributed to an overestimation of capacitance occurring at the depletion transition.

Conversely, at 0.6 V and below, the fit strength fell below 90% for both 58 cycles and 40 cycles. The comparison is even poorer for the conventional model, especially for thinner insulator dimensions (which fell below 60%). An assumption that was made in this revised model was that quantum effects were only present at the insulator-semiconductor interface, and thus the semiconductor-substrate end was dictated by classical mechanics. More technically speaking, the Schrödinger-Poisson self-consistency constraint was only applied to the active interface at biasing terminal and ignored at the semiconductor edge. This assumption is not fully valid, as indicated by the poorer fits prior to the pivot voltage.

In these cases where the active films are thinner than the expected depletion width, the electric field formed due to the applied bias influenced the entire film so that the equilibrium condition cannot be assumed at the edge of the thin body as it would for thick bodies where the electric field is negligible, such as MOSCAPS with semiconductor substrates. Therefore, just as both quantum and classical effects are considered due to the quantum well formed due to band-bending at the surface of the insulator's high potential barrier at the biasing edge, so must quantum/classical effects be considered at the semiconductor-insulator at the substrate edge of very thin films (grounding edge). The same constraints must also be considered for structures which have non-ohmic junctions, for instance in the case where the semiconductor is grown on Schottky metals. Compared to the insulator-semiconductor interface, centroids for classical centroid calculations would be higher. On the contrary, ultrathin active films grown on ohmic material layers would be subject to quantum effects only on the biasing side. Hence, a ground terminal connected directly to the bottom of the

semiconductor, instead of laterally, would only be bounded by classical effects as dictated by Poisson's equation. An example of such a structure will be demonstrated in Section **4.4**.

Finally, the fit for thinner and higher electric permittivity insulators show better agreement, as can be noted for the 30 cycles. This is consistent with a higher field strength becoming concentrated at the surface and thus carriers do not crowd the edge to the same extent as the lower dielectric cycle count within the same voltage.

4.2.5 DISCUSSION OF KEY PARAMETERS AND PARAMETERIZATION

EFFECTIVE THICKNESS

As recorded in Table **4.4**, in achieving a respectable fit with the experimental results and model discussed here, it was revealed that effective thickness of the semiconductor t_{eff} was larger than the actual thickness of the ZnO films t_{ZNO}. Closer examination of the MOSCAP structure shows that geometrically, t_{eff} can simply be broken down into two components: the depth component denoted in this work as t_x and the lateral component denoted t_r. A key assumption for this model is that the active film following the dimensional component parallel to the applied potential would be fully depleted by the corresponding component of the electric field. The 'additional' depth is accounted for as follows: due to the top lateral placement of the common terminal, a perpendicular component of the electric field must necessarily exist and it must end at said terminal. However, because the field strength dissipates at a rapid rate, the perpendicular component t_r can be simply approximated as follows:

$$t_{eff} = t_{\parallel}^2 + t_{\perp}^2 = t_x^2 + t_r^2 \tag{4.27}$$

A visual illustration is provided in Figure **4.17**. As an example, for 58 cycles, t_{eff} was found to be 50 nm. Knowing that the parallel component or, in other words, the ZnO film thickness, was 30 nm, the perpendicular component t_r was determined to be 40 nm. This means that

the field was significant up to 40 nm away from bias terminal in the direction towards ground. Table **4.5** summarized the calculated t_r for all cycles and shows a real pattern where as the dielectric became thinner, the field becames more concentrated at the surface hence the range of its penetration also became shorter.

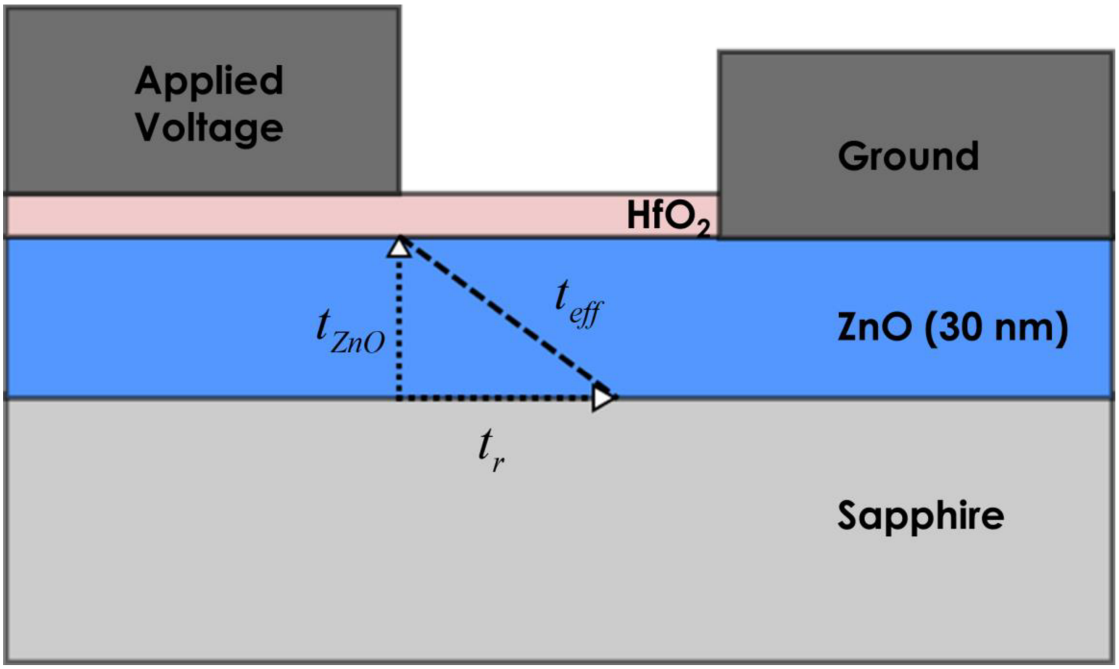


Figure 4.17: The geometrical interpretation of t_{eff}. The effective thickness for cases exceeded the actual thickness of the film. However, since the field as both a parallel t_z and a perpendicular t_r component, t_{eff} is interpreted as the Pythagoras sum of these two components.

Table 4.5: The calculated lateral component calculated from t_{eff}

Component	58 cycles	40 cycles	30 cycles
t_r †	40 nm	33.5 nm	33.5 nm

Parallel component $t_{||}$ or t_x was taken to the thickness of ZnO t_S = 30 nm

HIGHLY DOPED SURFACE AND QUANTUM CONFINEMENT

The semiconductor was parameterized into two separate regions: a region of high dopant concentration x_1 with the remainder of the film being relative moderately doped. As stated previously, the non-uniformly dopant profile were further refined to model the pivot voltage and the deep depletion region before it as seen in the measured CV. The pivot voltage being the voltage where the MOSCAP's capacitance transitioned from deep depletion region to the depletion region. It was found that the conventional approach could not simulate satisfactorily. To take into consideration the reports of ZnO's highly unintentionally doped surface, x_1 was chosen such that the linearly or exponentially graded dopant concentration was confined near the surface. Beyond x_1 to the edge of the semiconductor x_2, the tapering of the carrier concentration was at a much slower rate. The linear and exponential dopant profile are shown in Figure **4.18a** and Figure **4.18b**, respectively. This dopant distribution affected the overall carrier distribution of by increasing the voltage drop over the insulator and the about the insulator-semiconductor interface. As a result, the interface was more sensitive to the applied gate voltage V_{APP}.

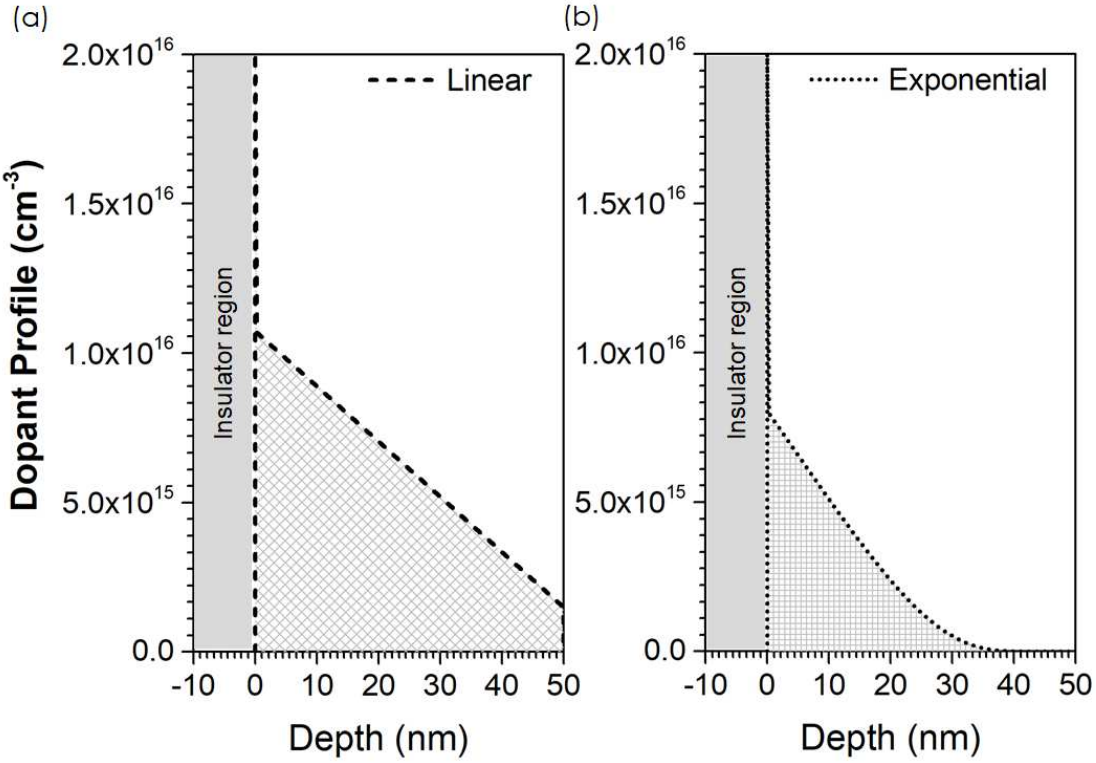


Figure 4.18: The revised dopant profile in PEALD ZnO that was distributed (a) linearly and (b) exponentially. Ultimately, exponentially-graded profile showed a better fit, but the important finding was that a highly doped surface relative to the rest of the film was necessary in order to resolve the CV behavior at lower voltages. The discontinuity x_1 represents the edge of the doped surface and the onset of the film's body. This surface depth was tuned until an acceptable fit was achieved.

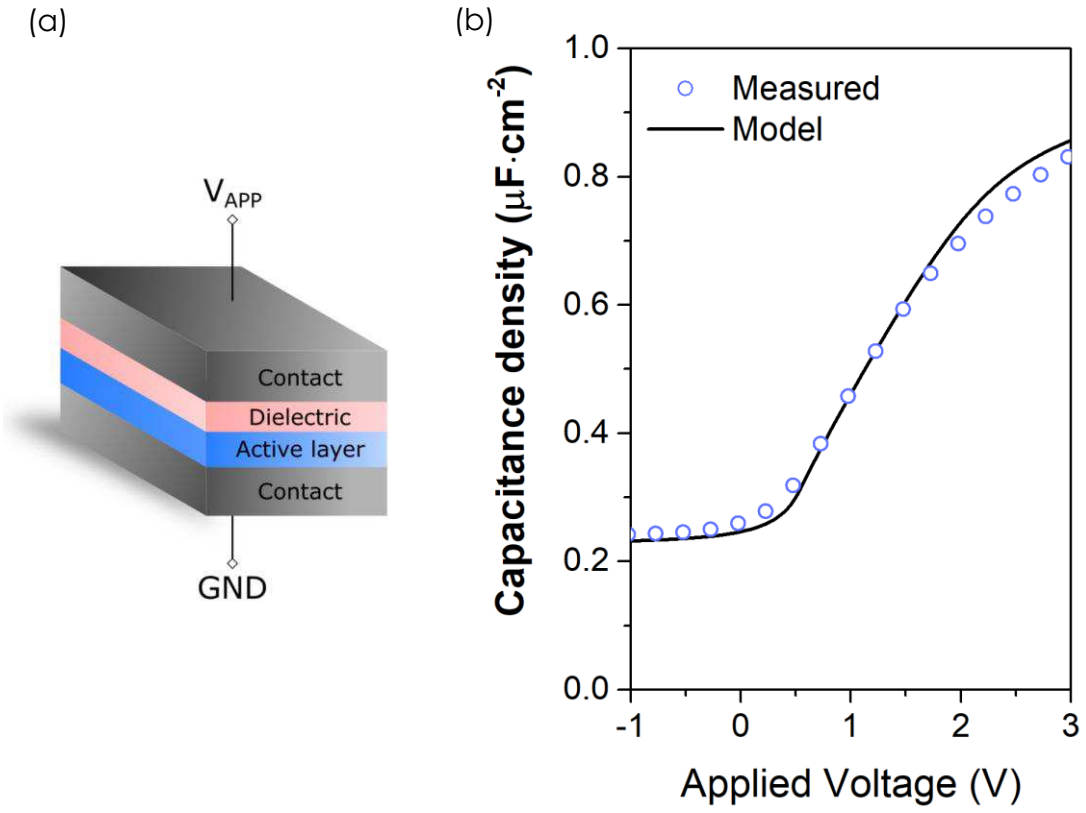
As expected, the non-uniformity exhibited in the doping distribution within ZnO played a critical role in resolving the capacitance at the deep depletion region when considering the geometry of the film in the overall CV characteristics. A uniformly distributed profile failed to reach the minima observed in the measured data by an order of magnitude of this ZnO MOSCAP structure when the geometry was incorporated. Further to that, a continuous linear and exponential profile also failed to emulate measured data, implying that there is a distinct surface chemistry at either the final synthesis steps of ZnO or it when it is exposed to ambient environment. This inference can be made due to the strong fitting evaluated for discontinuous non-uniform distributions that favour the surface and is validated by

experimental studies of intentionally hydrogen-doped ZnO studies showing similar distributions [**62**,**63**,**64**].

4.4 OHMIC SUBSTRATE MOS

In Section **4.2.4**, the models fit strength to the experimental results of fabricated film-on-insulator substrate MOSCAPs were discussed. Of particular interest was the poorer fitting observed in the deep depletion region before the pivot voltage, which was more prominent for thicker dielectrics with weaker electric permittivity. We suggested that because the semiconductor was grown on an insulating substrate, the carriers present on this edge must also follow the quantum confinement due to the formation of a well. On the other hand, for an ohmic substrate, the carrier distribution at the semiconductor edge would only have to obey Poisson's equation.

We tested this conjecture by building a vertical MOSCAP with a thermal ALD (TALD) ZnO film growth on an ohmic metal ruthenium (Ru). TALD ZnO was chosen because it has been previously reported that this deposition recipe formed an ohmic contact when grown on Ru by this group [**65**] and with other growths types as well [**66**]. A thick HfO_2 dielectric layer of 80 cycles was grown on the ZnO active layer (Figure **4.19a**) and the CV was experimental measured. The modified model developed here was then compared to the results and shown in Figure **4.19b**.



In this model, the non-uniform dopant distribution was also assumed. However, in stark contrast, the initial dopant profile for a TALD ZnO grown an ohmic metal showed higher concentration at the metal surface than the insulator surface. It therefore suggests that there has to be an high doped region present at the ohmic-semiconductor interface in order to achieve a good ohmic contact. The distribution of the non-mobile ionic specifies (here, donors) are shown in Figure **4.20**.

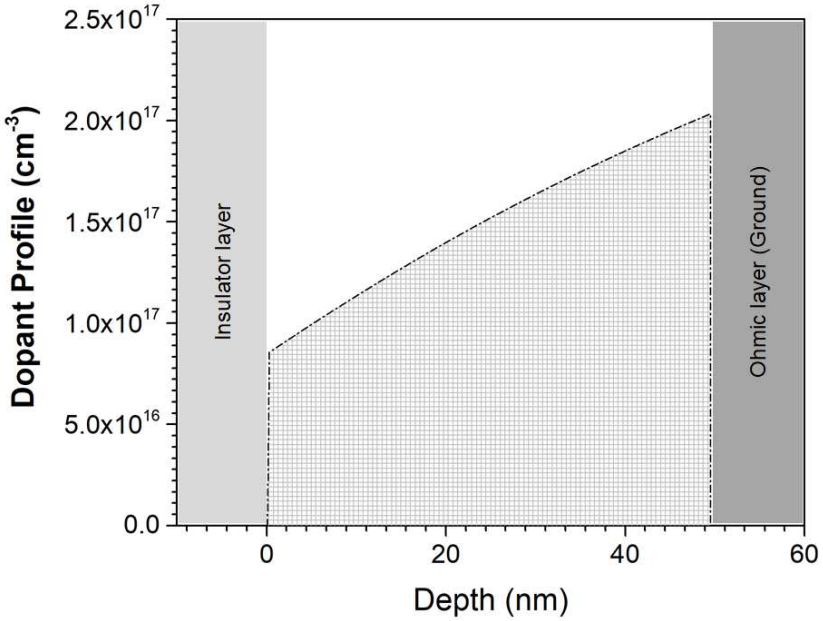


Figure 4.20: The dopant profile which yielded the best fit for the TALD ZnO grown ohmic substrate MOSCAP. At the Ohmic edge, the TALD ZnO film had higher dopant concentration than the insulator edge.

Analysis of the fit revealed a much improved for ohmic edge showing a 99.3% overall fit. The breakdown for below and above 0.4 V pivot are also summarized in Table **4.6**. The fit could be further improved by finely tuning t_{eff} and ε_{OX} .

Table 4.6: Fitting summary of vertical MOSCAP

Voltage Region†	**Fit**
≤ 0.4 V	96.1%
≥ 0.4 V	99.8%
Full	99.3%

4.5 Discussion and Conclusions

Conventional CV extraction via Schrödinger-Poisson equation was shown to be insufficient in capturing the behavior of thin-film MOSCAPs. The failure is attributed to the assumption that the thickness of the semiconductor is much greater maximum depletion width of the semiconductor. In thin active layers, such as those used in TFTs or the thin-film MOSCAP studies here, this is not the case. The modified model developed here incorporated the geometrical thickness of the thin film by considering the solutions of carrier centroids as solved by the Schrödinger-Poisson equation, instead of solely the dynamic of the net charge as function of voltage.

It was further found that, with the modified CV model, it was required that we remove the assumption that the distribution of the ionic charge (i.e. dopants) is uniform, which has been oft the default profile for many models. Instead, the dopant profile was approximated to be exponential in nature, with high concentration at the surface region which was rapidly exponentially decreasing, and beyond this region, a relatively slower exponentially decreasing doping concentration was assumed for the rest of the active layer. Such a profile was necessary in order to capture the behaviour at deep depletion at lower voltages and have been reported experimentally for controlled hydrogen doping in ZnO films, which are usually the unintentional dopant species in ultrathin growths.

The shortcomings of the model remain for cases when thin-film semiconductors are grown on substrates or base layers that are non-ohmic such as insulators, Schottky metals, or other semiconductors. For insulating base layers, potential quantum confinement affects are not considered when opposing potential to the carriers of interests are applied. For base materials which could form a junction with the thin-film, effects from such a formation is not taken into account. On the other hand, based on the aforementioned shortcomings, our hypothesis was that the model could properly model a vertical MOSCAP with the active

layer grown on an Ohmic metal. Indeed, the strongest fit was achieved with a fabricated and measured vertical MOSCAP and the model developed in this study.

The investigative nature of this work can potentially give electrical insight into thin-film materials other than ZnO, including dopant distribution and their nature, in addition to predicting CV behavior of thin-films.

5 TUNNELING JUNCTION TRANSISTOR: A NOVEL ARCHITECTURE FOR HIGH PERFORMANCE TFTS

5.1 BACKGROUND

5.1.1 UNIPOLAR TRANSPORT LIMITATIONS IN A TRANSISTOR

To enable thin-film flexible electronics to its maximum potential, a high current density thin-film transistor (TFT) is essential for many applications. The boost converter, for instance, deal with high current throughput which the switching transistor must be able to handle. The vast majority of modern TFTs however do not meet this requirement compared to traditional MOSFETs.

TFTs and traditional MOSFETs differ in whether their operations rely on a single carrier or both carriers. Thin-film field-effect transistor (FET) architectures, including the conventional metal-oxide semiconductor (MOS) TFT, are dictated by the treatment of a single carrier type, which in turn solely determines the output electrical characteristics of the device. Majority carriers are used to form the channel in the active region directly underneath the gate, whereas the traditional single-crystalline bulk MOSFETs use minority carriers. The bipolar nature of the traditional MOSFET allows the formation of both the accumulation and inversion region when extracting its CV characteristics. On the other hand, because the TFT is a monopolar device, only the accumulation capacitance is formed. This is made demonstrated for the n-MOSFET and the n-TFT in Figure **5.1**.

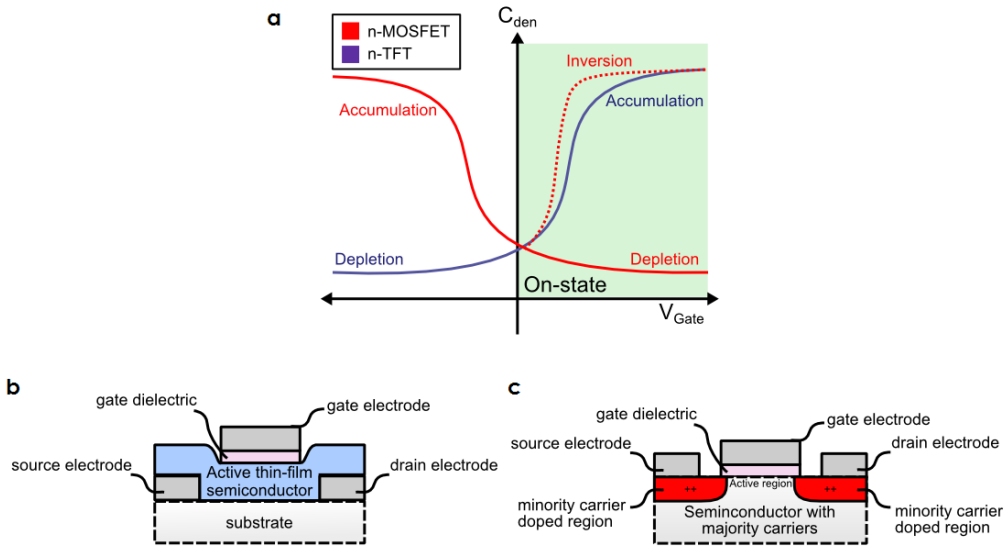


Figure 5.1: a) Shows the CV of n-TFT and n-MOSFET; b) the active thin-film of the TFT operated at accumulation region where the channel is made of majority carriers; and c) the n-MOSFET operates in the inversion region where the minority carrier doped regions at the source and drain supplies the channel with minority carriers.

For the TFT, majority carriers of the accumulation region are used. In Figure **5.1b**, these carriers are drawn from the body of the thin-film and forms the channel with the source and drain and the current path does not encounter any pn-junctions. In contrast, for traditional MOSFET architecture shown in Figure **5.1c**, the minority carriers of the inversion region formed the channel and these carriers are supplied by the source and is collected at the drain. Both the source and drain region are highly-doped and made up of the carrier species opposite of the lowly-doped semiconductor body. The current sees two pn-junctions as a result. By controlling conduction through minority carriers, traditional MOSFETs can be effectively scaled with respect to the gate capacitance (C_{OX}) simply by thinning the gate dielectric. This is because the turn-on voltage V_{ON} does not heavily depend on the thickness of the gate dielectric, but rather the minority charge channel formed at a certain voltage threshold V_{TH}. In contrast, TFTs can suffer from undesirable V_{ON} if the C_{OX} is not sufficiently thick, since an insufficiently depleted channel of majority carriers may exist during OFF-state voltages causing parasitic conduction.

As a result, monopolar enhancement devices based on these mechanisms fundamentally suffer from low current output, and rely heavily on the field-effect mobility μ of the active film for compensation eqn (**5.1**). The inescapable trade-off which limits unipolar accumulation-mode devices stems from the pursuit of a desirable turn-on voltage. To achieve this, either the gate oxide must be sufficiently thick or the active material must exhibit sufficiently low carrier concentrations to be fully depleted by the gate dielectric alone. Both of these options must be exercised to obtain a well-behaved transistor but ultimately result in low drain currents I_D due to a low maximum oxide-charge capacitance C_{OX} [**67**,**68**,**69**].

$$I_D \propto \mu C_{OX} \tag{5.1}$$

5.1.2 BIPOLAR TRANSPORT ADVANTAGES

For this reason, several advantages are immediately apparent in the use of bipolar devices. Electrical characteristics such as off-state behaviour, transconductance, cut-off frequency and current gain are intrinsically superior to the FET, making them generally preferable in amplifiers, an application which modern TFTs cannot sufficiently fulfill [**70**]. Furthermore, the mobility metric of the semiconductor is not as crucial in the output of these devices due to the diffusion based charge transport [**71**]. Monocrystallinity and reduction of lattice defects is crucial to minimize current loss to excessive carrier recombination [**72**,**73**]. Up to this point, due to the general disordered nature of the crystal lattice in thin-film semiconductors, true bipolar junction TFTs, in contrast to the ambipolar variant [**74**,**75**], have been largely non-existent.

5.2 THE THIN-FILM TUNNELING JUNCTION TRANSISTOR (TJT)

What is required for bipolar transport at low temperatures in non-crystalline wide-bandgap transistors is a p-type source that supplies holes in the inversion region of the device. A similar method is used for an asymmetrical TFT architecture, the source-gated field-effect transistor (SGT). In this device, a Schottky metal source supplies electrons into a depleted body at voltages corresponding to the accumulation region that forms the channel within the intrinsically n-type semiconductor [**76**,**77**].This method for injecting carriers from a metal to form an active channel proved successful in building an enhancement-mode ZnO-based TFT depleted of free carriers [**78**]. Hence, any material source of holes, for example, p-type Si at the appropriate bias can inject its majority carriers into an n-type wide-bandgap semiconductor bringing us a step closer to bipolar action in a ZnO-based transistor.

The workings of such a transistor is introduced here by incorporating the tunneling emitter bipolar design previously reported within a thin-film medium [**79**,**80**,**81**,**82**]. Active thin-film technologies to date have been limited to low power switching applications primarily because of low current density exhibited in TFTs. Beginning with a wide-bandgap oxide semiconductor, in this case zinc oxide (ZnO), we put in conjunction with the p-type hole source to form a pn-junction. We then combined the principals of the tunneling emitter and the base-inversion channel to demonstrate a novel thin film bipolar transistor architecture: the thin-film tunneling junction transistor (TJT).

5.3 HOLE INVERSION LAYER FORMATION

5.3.1 P-SOURCED N-TYPE MOSCAP: DEVELOPING THE REFERRED BASE

A npn BJT requires a p-type base. To achieve a similar bipolar action within a TJT, requires the same. However, this is especially difficult in thin-films that usually have large bandgaps are commonly either intrinsically n or p-type. In other words, thin-films are dominated by

majority carriers such that minority carriers are nigh undetectable. A consequence of this arises in CV measurements where inversion capacitances are instead replaced with deeper depletion capacitance at inverse voltages. It is hypothesized here that the crux of the problem is the absence of a source of minority carrier. In the case of n-ZnO, a p-type source is required.

To demonstrate that a p-type source will be able to inject its carriers into an intrinsically n-type wide-bandgap material and subsequently form an inversion layer, a n-ZnO MOSCAP built on a (100) p-Si was simulated using Crosslight TCAD with the bias scheme shown in Figure **5.2**. A 25 nm ultrathin PEALD n-ZnO mesa was layered on a (100) p-type silicon substrate to form a pn-junction. Above n-ZnO, a 4 nm HfO_2 layer was place and then finished with the emitter terminal and ground contact made up of aluminum and gold (Al/Au).

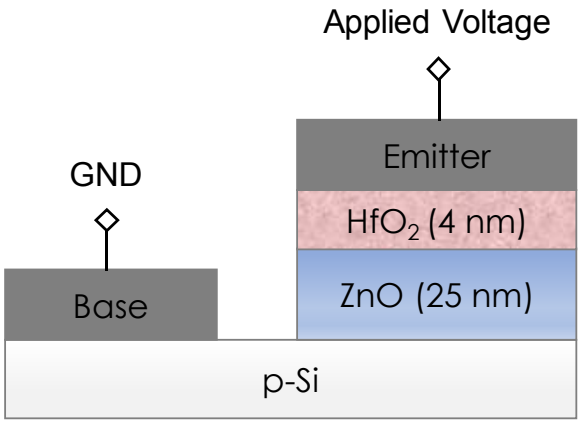


Figure 5.2: The MOSCAP structure simulated in Crosslight TCAD consisting of the active layer n-ZnO on top of a p-Si substrate that behaves as a supply for holes. A 4 nm HfO_2 is deposited on top of n-ZnO to form the barrier layer. The structure is completed with a base and emitter made of Al/Au.

During the early onset of the ON-state (V_{BE}, $\overline{V}_{EB} > 0$ V), holes injected from the p-Si conglomerate in ZnO directly underneath the HfO_2, forming the referred base or the p-type analogue in an NPN transistor. The accumulation of holes in the 2D inversion layer that serves as the referred base at the HfO_2-ZnO is evident in the simulation results using the classical Poisson model presented in Figure **5.3a**. Furthermore, the simulated results presented revealed a uniform hole distribution across the region where there is no direct contact with

the p-Si base. This study also predicted a significant hole gas concentration on the order of 10^{20} cm^{-3}.

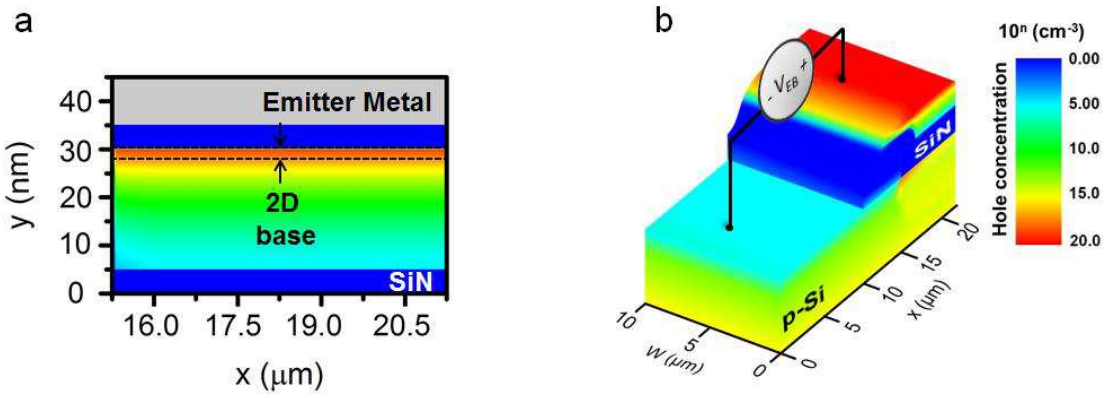


Figure 5.3: The distribution of holes at the a) HfO_2/ZnO region isolated from the p-Si holes source showing lateral uniformity and reaching hole concentration of up to 10^{20} cm^{-3} at the 2D referred base; b) the hole distribution of the full device from the onset of the p-Si control base to the edge of collector contact biased at V_{EB} = -5V.

In Figure **5.3b**, the full ON-state hole distribution *sans* the contacts and barrier layer of the device based on simulation from onset of the p-Si to the edge of the collector contact is given at V_{EB} , $\overline{V}_{BE}$ = -5 V. We can observe that the hole inversion uniformity directly underneath the barrier layer ceases at from the start of the p-n overlap to edge of the isolation layer (SiN) where it terminates. At the p-n junction itself, a large layer depleted of holes is formed. While a p-type substrate was used as a proof-of-principle of the TJT, a thin-film hole source can be be utilized and designed by considering the doping concentration of the p-type material. In this instance, the p-Si substrate was set with a doping concentration on the order of 10^{15} cm^{-3} which was then put in intimate contact with a 5×10^{16} cm^{-3} doped n-ZnO. At V_{BE} = 5 V, this resulted in a maximum "active charge region" of 80 nm at the valence band edge of the ON-state p-Si, the total hole-accumulation width, plus the additional 25 nm n-ZnO film. The relevance of this metric being that the remaining p-type carriers in p-Si beyond 80 nm do not participate in the injection of holes into ZnO.

A direct implication is that the thickness of any given p-type thin film chosen for use in a TJT can be made thinner if the material features higher acceptor doping or holes concentration, the ideal being intrinsically hole conducting materials [**83**]. Further implications also suggest that the only condition for the n-type film where the referred base forms is that its bandgap is sufficiently wide. Conversely, at OFF-state (V_{BE}, $\overline{V}_{EB} < 0$ V), the pn-junction becomes reversed biased wherein the n-ZnO film is almost fully depleted and the p-Si is depleted up to 50 nm, with a small accumulation of the remaining free electron carriers at the barrier interface.

To experimentally verify that an inversion layer can formed as suggested by simulations, a MOSCAP with the same structure as the model was fabricated and directly measured (see **Appendix**). The CV characteristics are shown in Figure **5.4**. The emitter was treated as the cathode (applied voltage terminal) and the p-substrate as the anode (ground terminal) as indicated in Figure **5.2**. A max capacitance density of 1.9 μF·cm^{-2} at the HfO_2/ZnO interface was detected at the negative voltages and is attributed to the corresponding holes injected into n-ZnO. Alongside the capacitance, the conductance density measured at this region also exhibited more dynamic behavior, indicating that control of the device via the control base terminal can be exercised at voltage V_{BE}, $\overline{V}_{EB} < 0$ V. In contrast, at OFF-state, a small ZnO electron accumulation capacitance density of 0.05 μF·cm^{-2} is detected, coupled with a conductance density that allowed almost indiscernible and eventually no control over charge after V_{BE}, $\overline{V}_{EB} = 2.2$ V.

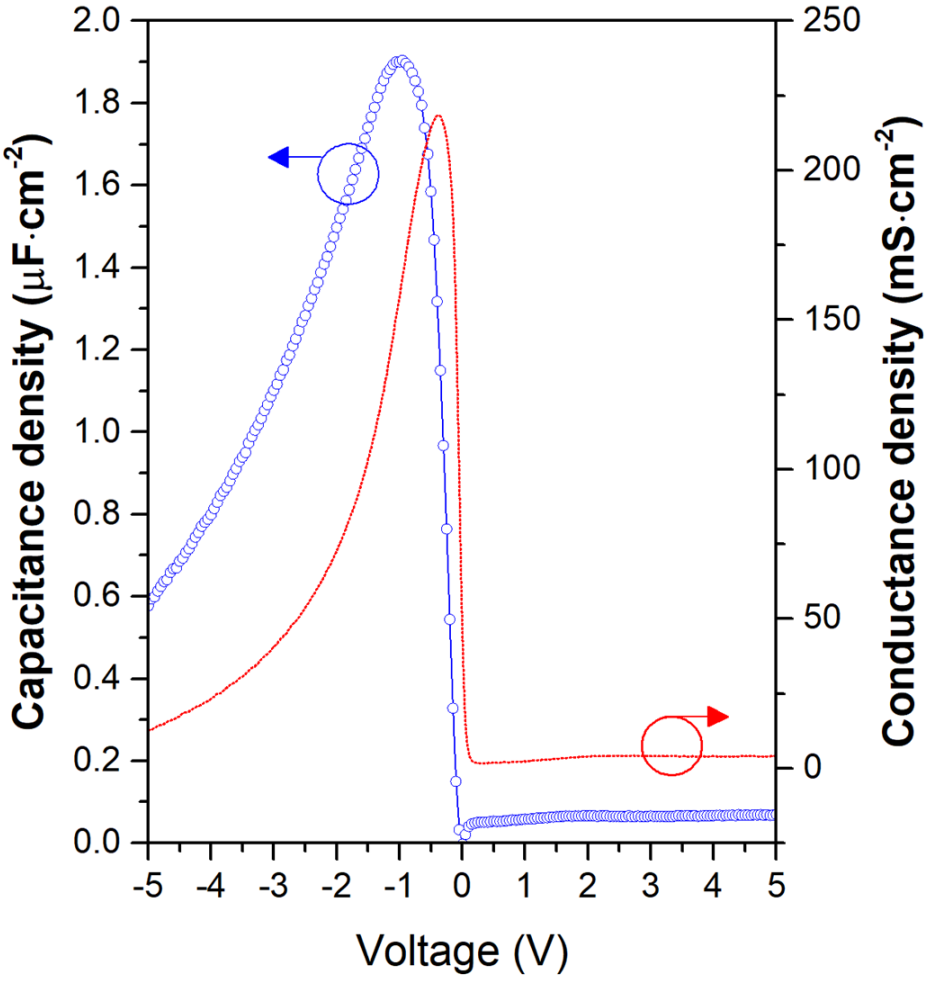


Figure 5.4: The HfO_2/n-ZnO/p-Si MOSCAP showing the (a) measured CV which is consistent with proposed electrical operations. Furthermore, conductance curve reveals that control over charge is maintained beyond $V_{EB} < 0$ V before leakage degrades the GV. At $V_{EB} > 2$ V, there is no control of charge during accumulation.

Due to the structure of the MOSCAP, we observed for the CV that below V_{BE} = -0.90 V, the maximum capacitance decreases at relatively rapid rate. Since the ground terminal was set on top of p-Si instead of the bottom, as the reverse bias increase, the pn-junction becomes fully forward bias and the capacitance detected at the interface begins to degrade. Much of the charge is lost into the p-Si substrate as it provided an alternative current path to the top ground terminal. A similar degradation behavior is also seen with the conductance when the p-Si/n-ZnO is turned on. This has been reported for Si MOSFETs with top source contacts, with a correction factor associated to compensate for leakages [**84**].

Nonetheless, it remains of interest the CV behavior of the reverse voltage as the p-Si substrate can be replaced with a viable thin-film p-type semiconductor film.

5.3.2 TRUE INVERSION CAPACITANCE

To understand the behavior of the emitter MOS interface operating at inversion, the modified Schrödinger-Poisson method, the CV was modeled to gain a true estimation capacitance behavior. Although the substrate leakage degraded the capacitance a beyond -0.95 V, the region from 0 V to the threshold voltage ('calibration region') can be used a guide knowing the general parameters of MOSCAPs prior. It is important to gain insight into the mechanics of the interface when tunneling at the MOS interface is investigated. In particular, the surface potential and the effect of the field at the oxide all play an important role in determining the tunneling current, a key to TJT device operations.

The estimation of the true inversion capacitance is shown in Figure ***5.5*** to be about 3.1 $\mu m \cdot cm^{-2}$ at 2V. At this voltage, the measured capacitance density was reduced to just 1.5 $\mu m \cdot cm^{-2}$. To note, the model and measured did not perfectly fit the calibration region, especially at the voltages about 0 V. A minimum capacitance of about 0.2 $\mu m \cdot cm^{-2}$ is predicted but the experimental results at the same voltage was much lower, even indicating slight leakage at 0 V. To explain the discrepancy, as stated before, the model makes the assumption that the active layer is on top of an ohmic contact. In reality, of course, being that n-ZnO was layered so as to form a junction with p-Si. Therefore, the additional depletion width contribution came from not just ZnO alone, but also from the p-Si substrate. As a result, this was detected as a lower minimum capacitance at about 0 V and above, as expected from a reversed biased pn-junction.

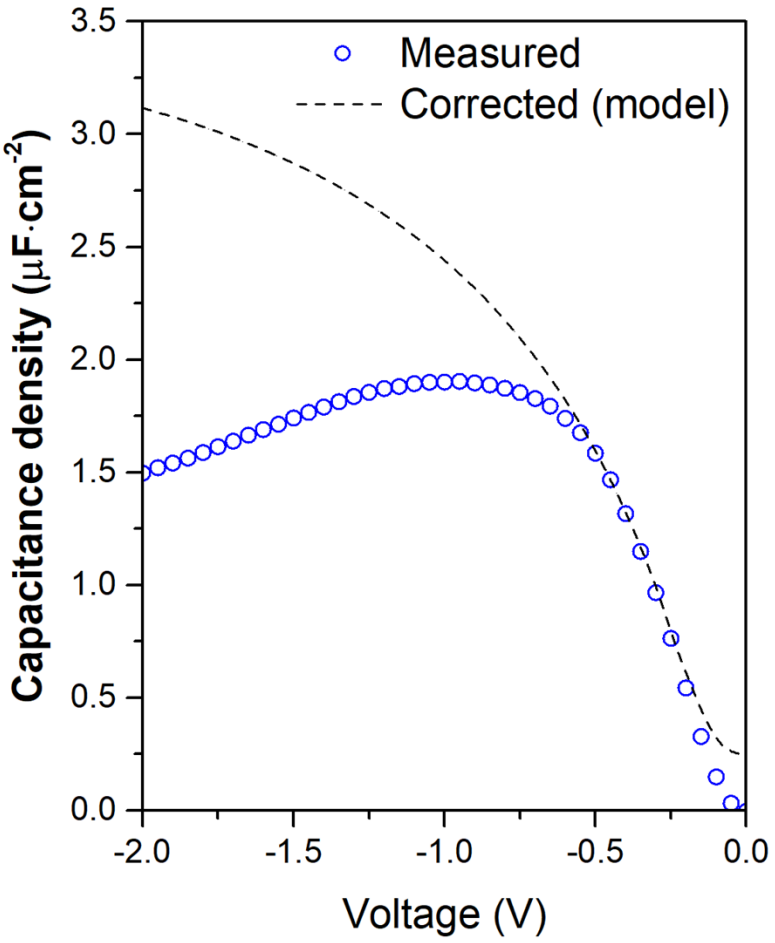


Figure 5.5: Simulated CV characteristics of the HfO_2/n-ZnO/p-Si MOSCAP. Using the modified Schrödinger-Poisson equation, the model predicted the corrected inversion capacitance to be 3.1 μF·cm^{-2}. The correction removed the additional junction effects contributing to the degradation of the inversion capacitance.

With the CV characteristics confirming that an inversion layer can be formed in a wide-bandgap semiconductor which is intrinsically n-type like ZnO, it is found that one of the key component a TJT, the tunneling emitter, can be realized and further enhanced.

5.4 TJT: TUNNELING EMITTER

Previous transistor designs featuring the tunneling emitter showed promise due to its intrinsic current gain properties resulting from the ratio of electron carriers versus hole carriers tunneling through the barrier layer [**85**,**86**,**87**]. However, the design was limited due to

insufficient volume of carriers participating in the overall current throughput, with the best reported current gain being 500-800 (A/A) with a low density of 0.07 mA/mm [**88**]. Most of these devices, however, used a silicon (Si)/silicon dioxide (SiO_2) material system which exclusively relies on direct tunneling of electrons and holes through a large barrier determined by the conduction ($E_{C\text{-}offset}$) and valance band-offsets ($E_{V\text{-}offset}$). Few wide-bandgap tunneling-emitter transistor were also studied, showing slightly better but still insufficient current output, such as AlAs/GaAs and AlGaAs/GaAs systems, which required high temperature (>500 °C) growth techniques [**89**] and are ultimately not flexible nor bio- or print- compatible.

5.4.1 FABRICATION OF THE TJT

Figure **5.6a** and Figure **5.6b** shows the layers and cross-section of the TJT. A top-down achromatic image was taken to highlight each constituent layers of the final device (Figure **5.6c**). Key dimensions are also labeled: in this device: the base-, emitter- and collector-width W was 10 µm, the Si/ZnO pn-junction overlap L_{OV} was 5 µm, and the emitter to collector length L_{EC} was 10 µm. On a p-Si substrate, 50 nm of PECVD silicon nitride (SiN) was deposited as the isolation layer. The plasma-enhanced atomic layer deposition (PEALD) and the plasma-enhanced ALD (PEALD) processes were performed at 200 °C and 100 °C, respectively. The first TALD process deposited a 25 nm ZnO blanket film over the entire substrate and patterned by wet etching with ferric chloride. Following this, the emitter was fashioned using lift-off with a 4 nm PEALD HfO_2 barrier layer on top of ZnO, thus forming the tunneling emitter. A more detailed fabrication steps is provided in the **Appendix**.

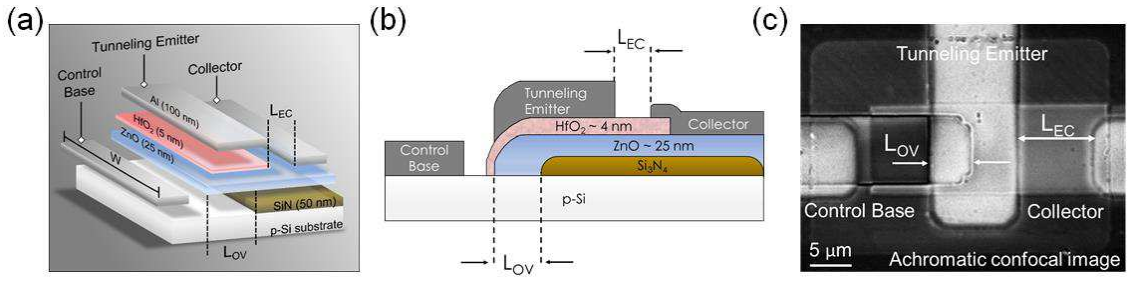


Figure 5.6: Overview of the thin tunneling junction transistor (TJT) based on p-Si/n-ZnO/HfO2 tri-heterojunction: a) the fabrication process layers beginning from a bare p-Si substrate to the final metal layer; b) cross-section of a completed device along with the key terminals including the control base, tunneling emitter and collector; c) achromatic confocal microscopic top-view of a sample completed device; L_{OV} = 5 µm, L_{EC} = 10 µm.

5.4.2 TUNNELING CURRENT IN TRUE METAL-INSULATOR-SEMICONDUCTORS

There are numerous literature that have described in detail the tunneling currents observed in Si-based MOS structures. Unlike the TJT studied here, the exact structure of the Si-based MOS consisted for Si of either n or p type, followed by a gate oxide and gate electrode being made of highly degenerate polysilicon [**90**,**91**,**92**,**93**]. Direct tunneling, as a result, was simply explained by a flow current resulting from carriers transporting from band-to-band through the gate oxide potential barrier. This model was successful in describing this phenomenon with great precision and is the basis for other tunneling emitter transistors. As these would not be valid for a structure utilizing a true metal instead polysilicon, classical models developed on the principles outlined by Richardson, O.W. (1912) [**94**] and corroborated by Sze, *et al* (1967) [95]. These works were exclusively based on the Poisson interpretation of metal-Schottky barriers [**96**,**97**,**98**,**99**]. After the wider acceptance of the Bardeen's (1964) proposed quantum mechanical description of tunneling [**100**], several MIS tunneling models combined the Schrödinger description with the classical solution to produce an approximate analytical or self-consistent solution [**101**,**102**].

In this work, the solution was self-consistently solved iteratively through the transfer matrix method [**103**,**104**,**105**]. The tunneling coefficients are determined by the reflection and transmission of the wavefunctions as it interacts at the metal-insulator interface and the

insulator-semiconductor interface. This was then compared with the measured current of the transistor biased TJT as in Figure **5.7a**. The voltage was applied from emitter-to-base and the current was taken at the collector as revealed in Figure **5.7b**. The voltage where the p-Si/n-ZnO junction is turned on is also indicated in the figure and it corresponded with the voltage where the CV clearly degraded and deviated from the theoretical CV (Figure **5.5**). The collector was set at V_C = 0 V to ensure that no additional fields were induced at the emitter.

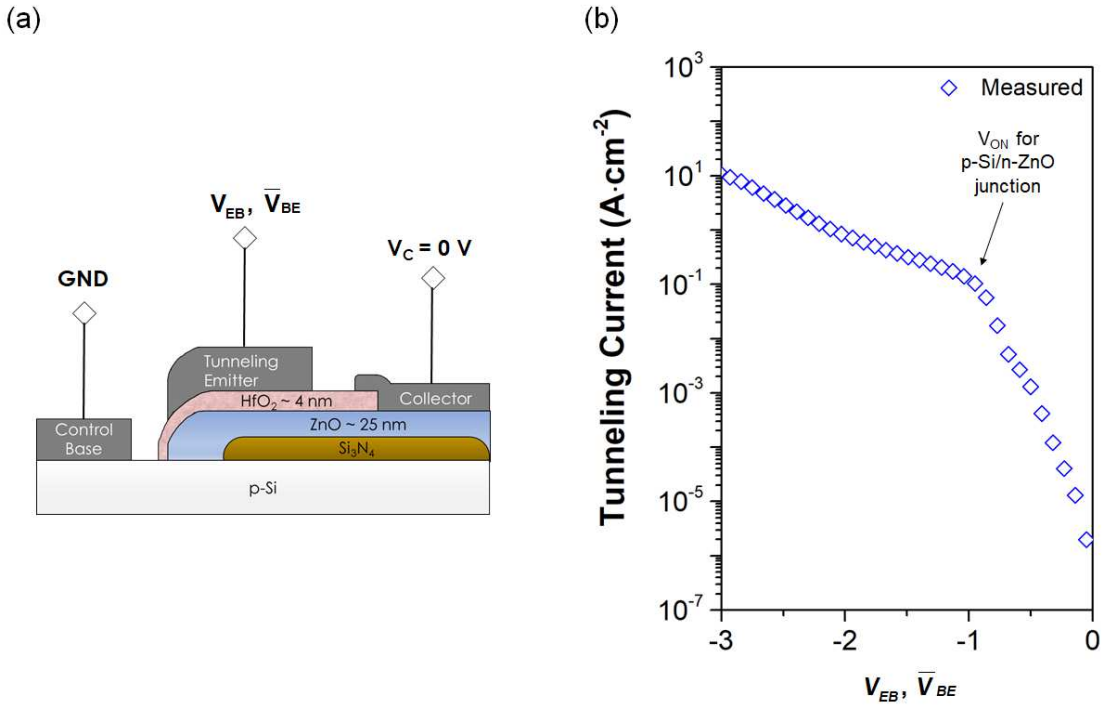


Figure 5.7: (a) The bias scheme of the TJT to measure the tunneling current at the emitter and, (b) the corresponding measured tunneling current density. The tunneling emitter was operating at inversion. The voltage where measured CV deviated from the expected CV is labeled as "V_{ON}" and is the point where the p-Si/n-ZnO junction is turned on.

The IV output of the TJT was consistent with other reported MOS junctions which have shown the same general IV form for highly degenerate p-type Si semiconductors with ultra-thin SiO_2 barriers for instance in the work of Sze *et al.* (1967). At the voltage beyond the 'knee' voltage about -0.9 V, the tunneling current's dependence on the applied voltage was weakened. It is worth noting that the knee voltage is a close match to the voltage at which the

capacitance density began to degrade rapidly as seen in Figure **5.7b**. Although this was observed in MOS with p++ Si substrate, the lower voltage dependencies occurred at higher potentials where the tunneling probability reaches its peak. This behavior may differ with the TJT because the interface region of interest was operating at inversion instead of accumulation. Though the exact nature cannot be known until further investigations. To determine whether this loss of control over current is predicted by the tunneling model or is caused by other factors, a comparison between model and measurement was made of a 4 nm HfO_2 barrier in an n-ZnO MOS structure.

The potential electron barrier height at equilibrium was assumed to be equivalent to the conduction band offset ($E_{C\text{-}offset}$) at the HfO_2/ZnO interface. The hole barrier height was determined by the valence band offset. X-ray photoelectron spectroscopy (XPS) determined $E_{V\text{-}offset}$ to be only 0.12±0.02 eV and $E_{C\text{-}offset}$ was calculated to be 2.27±0.02 eV. Similar values have been reported with single crystalline ZnO with HfO_2 [**106**]. The tunneling current taken beyond the onset of the semiconductor surface. Using the modified Schrödinger-Poisson, the potential drop over the 4 nm insulator HfO_2 was determined and applied to the tunneling model. The initial description of the dynamic behavior of the band diagrams are given Figure **5.8**. As the applied voltage decreases (becoming more negative), the oxide begins to bend down indicating a negative electric field.

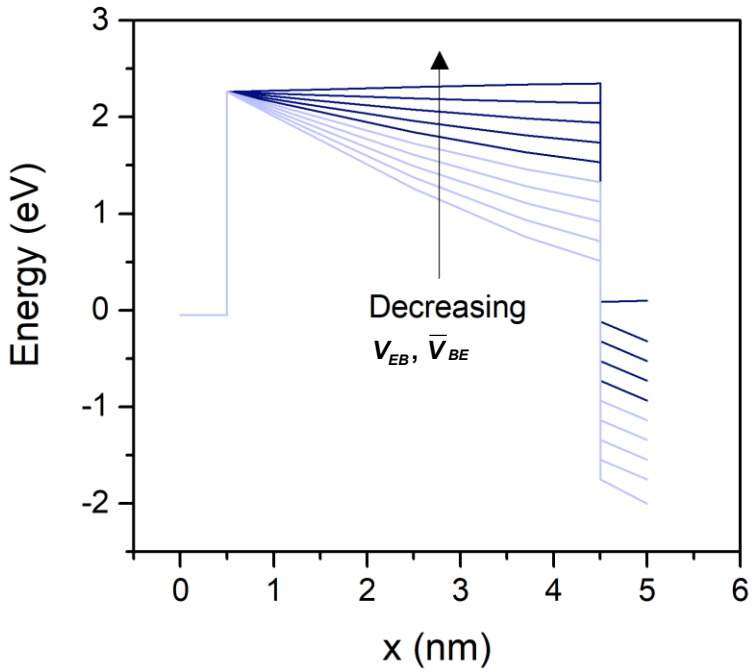


Figure 5.8: The dynamic band profile of the tunneling emitter as the applied voltage V_{EB} is varied from 0 V to 2 V. The barrier bends downward in response to the negative bias and the ZnO conduction band edge bends down as it gets further depleted.

In Figure **5.9**, the current-voltage (IV) of the measured reverse current at the tunneling emitter is compared with the model output. The results showed significant disagreements at both below the knee voltage and above. Differences in current density at higher negative biases can be attributed both series resistance and loss of electrons via recombination with the hole inversion layer as the measured current is taken at the collector terminal. On the other hand, discrepancies at voltages closer to 0 V merited a deeper investigation because the current measured was greater than the predicted output. Additional leakage paths as a result of defects within the oxide or the interface may explain it. However, a brief examination of the tunneling current for n-ZnO which could form an inversion layer showed that the current was consistent with direct tunneling of HfO_2 and n-Si. In Figure **5.9**, the PEALD HfO_2 used in this study had leakage performance comparable to the HfO_2 used in production at the same oxide thicknesses [**107**]. Thus the additional leakages cannot be

attributed to poor oxide performance. Another possibility that is eliminated is leakage current from the pn-junction, which if it were the case, the resulting current density would rise at a much faster rate than what was measured here.

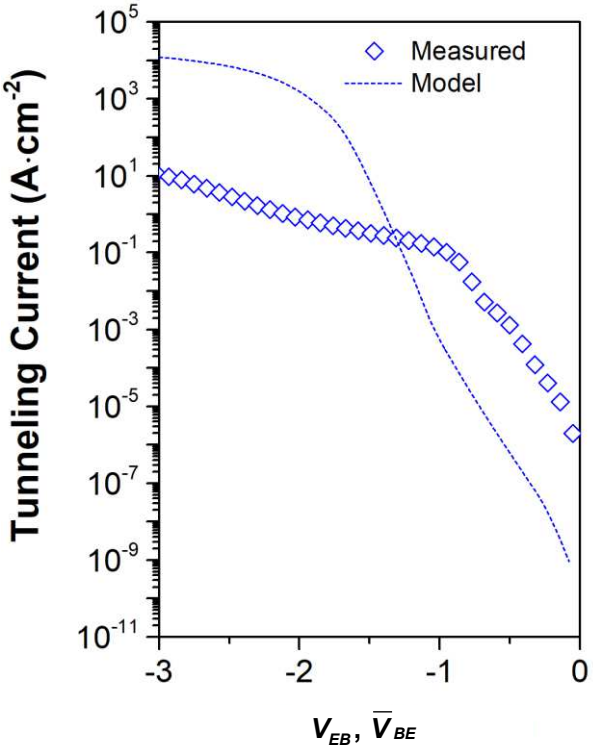


Figure 5.9: Tunneling current of the emitter was modeled using a Schrödinger-Poisson transfer matrix method. There is significant mismatch between measured and model at the calibration region (0V to -0.9 V) when considering a 4 nm barrier thickness (the physical barrier thickness of HfO_2 layer).

5.4.3 WAVE MECHANICS IN TUNNELING BEHAVIOR

Current density is extracted after the tunneling probability is determined using the transfer matrix method. For MOS using true metals, the current is determined using equation (**4.1**).

$$J_T = \frac{A^* T}{k_B} D\left(E_x, V_{bias}\right) \cdot \int \left[f_o\left(E\right) - f_{N+1}\left(E\right) \right] dE dE_x \tag{5.2}$$

Where A^* is the effective Richardson constant and E_x is the energy of the electron whose tunneling probability, D is evaluated. The tunneling coefficient as calculated from the connecting momentum eigenfunctions with the general description of the wavefunction as follows:

$$\psi(x) = Ae^{jkx} + Be^{-jkx} \tag{5.3}$$

ψ The wave vector k of the transmitted electron is calculated with respect to the barrier profile U simply by:

$$k = \sqrt{\frac{2m^*}{q\hbar^2}(E-U)} \tag{5.4}$$

In Equation (**5.4**), only the transmission waves are of interested and are detected in measurement. It is then acceptable to ignore the reflected waves about the insulator-semiconductor interface.

$$\psi_T(x) = Ae^{jkx} \tag{5.5}$$

Boundary conditions are set at the metal-insulator interface with A = 1 (source of the transmitted electrons) and the insulator-semiconductor interface B = 0 (no wave being reflected back into the semiconductor). In other words, at both interfaces the continuity of ψ and $(1/m^*)$ $(d\psi/dx)$ must be satisfied.

As there is the tunneling current is directly proportional to the transmission probability, the ratio of the model and measured current is related to the ratio of the probabilities simply as:

$$\eta = \frac{J_{Tmeas}}{J_{T\,\mathrm{mod}}} = \frac{D_{meas}}{D_{\mathrm{mod}}} \tag{5.6}$$

The solution of *D* for a single electron is proportionally related to the transmitted wave function by multiplying itself with its conjugate. By combining Equation (**5.5**) and (**5.6**), we arrive at:

$$\eta = \frac{e^{jk_{meas}x_{meas}}}{e^{jk_{\mathrm{mod}}x_{\mathrm{mod}}}} \tag{5.7}$$

To further simplify this relationship, we investigated the parameters influencing the wave vector and discuss its effect on the tunneling constant. Much like the measured model, the goal remains to find plausible method to match the measured data below the region where the output began to degrade. For the measured current, this region is defined as from about 0 V to the knee voltage of ~-0.9 V. The knee voltage also had a close correspondence to the voltage at which the capacitance in the CV measurement began to degrade due to leakage.

Limiting the study to the first order, from equation (**5.7**), that leaves the effective mass of the transmitting electron m^* as it traverses HfO_2 and enters ZnO and the band profile with which the electron interacts. Modifying m^* = 0.05 as it interacts with HfO_2 yielded a good match experimental data, but contradicts literature values, even at the lowest range of 0.1 to 0.18 [**108**,**109**,**110**,**111**]. For the sake of rigour, we maintained that m^*_{HfO} = 0.15 which is a widely reported value. Similarly, the effective mass for ZnO was not modified and set at m^*_{ZnO} = 0.15. The effects focusing on the barrier and the band bending behavior are plotted in Figure **5.10**. We considered the case where the conduction band offset to ZnO was halved resulting in lowered potential barrier in Figure **5.10a**. While it showed a better match than the original parameters, the match to the range of interest was not satisfactory. Increased barrier

bending shown in Figure **5.10b** also did not achieve a strong match. Both of the resultant tunneling currents are shown in Figure **5.10c**.

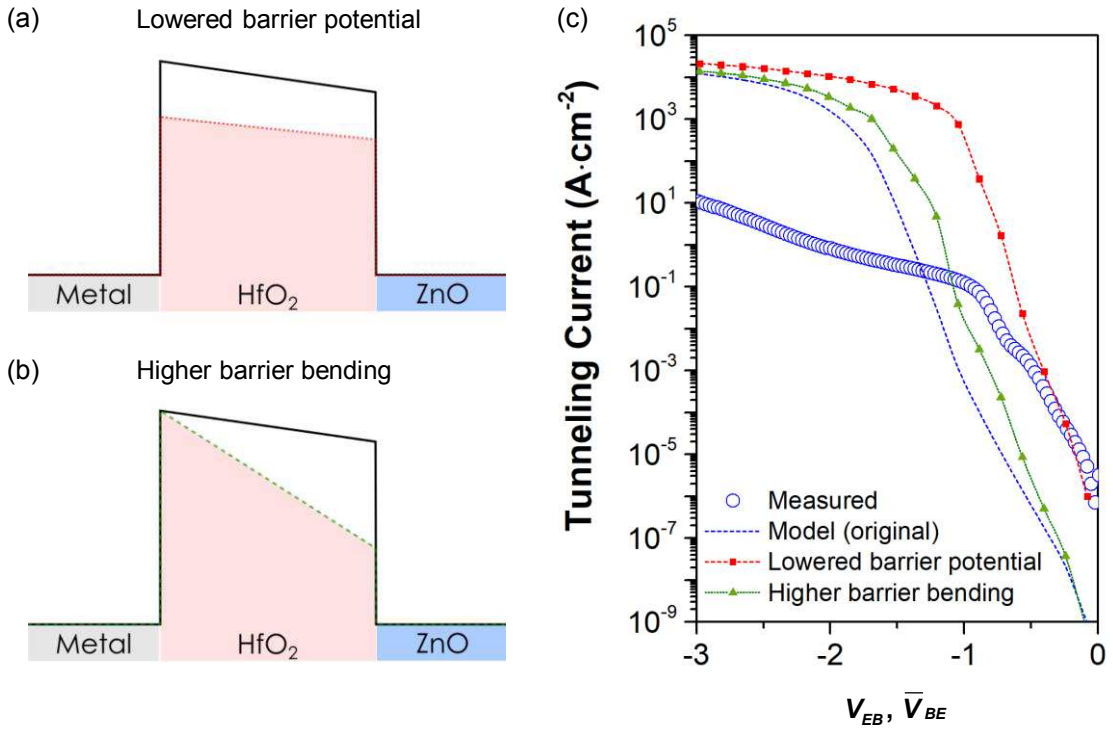


Figure 5.10: Measured vs. simulated tunneling current for parameters affecting the wave vector *k*. The original barrier profile (black line) was compared to two cases: (a) Lowering the barrier potential (filled red circles) showed a better fit but did not satisfactorily match the region of interest. (b) Increasing the amount of barrier band bending (green filled triangles) still underestimated the tunneling current at the calibration region. (c) The resultant tunneling current generated by the model.

Due to the general failure of achieving an acceptable match by modifying the parameters affecting *k* in the first order, the unaccounted for idiosyncrasies with the wave vector was concluded to be a minor contributor to the mismatch observed between the original model and measured data. By eliminating *k* as a factor, and setting $k_{meas} = k_{mod}$ we return to equation (**5.7**) and attribute the aberration solely on the distribution of the wave function which reduces the ratio η to:

$$\eta = e^{jk\cdot\Delta x} \tag{5.8}$$

An interesting consequence of this consideration is that the distribution of the wave function distribution of the metal ψ_m or that of ZnO ψ_{ZnO} (or both) either penetrate or is centered further away from their respective interfaces. Because the modeled current was lower than the measured above the knee voltage, the latter was not considered a possibility because it would result in a lower tunneling probability. If we consider that ψ_{ZnO} penetrates the barrier, instead of ceasing at the insulator-semiconductor interface, then only a portion of the onset of a wave would be able to do so. This portion may not be significant enough to influence Δx. For the sake of simplicity, the assumption for wave function of ZnO was upheld, thereby leaving the physical interpretation of Δx solely on the behavior of metal wave function ψ_m. This will be explored in Section **5.4.4**.

To reiterate, the goal of this analysis is to determine if whether there exists a single correction parameter that resolves the disagreement in the model and the measurement. This correction is identified through the difference described by η and associated with Δx while the calculated *k* is unchanged. For simplicity's sake, the wave vector *k* is assumed to be true because the individual components, such as effective mass or barrier potential, etc. that influenced it did not completely satisfactorily explain the difference. And the intention was to keep the degree of freedom of the parameters to a minimum.

The ratio η was evaluated at comparable voltages and the wave vector *k* was simply extracted from the model results. Higher ratios imply the largest discrepancy and is observed at -0.1 V with the largest revealed at Δx = 1.6 nm (Table **5.1**). As the voltage became more negative Δx decreased as the model begins to intercept the experimental data, converging at about 0.9 nm. Nonetheless, because the goal was to match the full voltage region of interest by minimizing the amount of parameters requiring adjustments, only the Δx associated with the largest extraction discrepancy ratio η was considered. The largest

η was associated at the V = -0.1 V, with a ratio of 5589. The dependence of η with respect to the voltage is also a strong indicator of a poor fit at the voltage range not influenced by structural factors (e.g. before the p-Si/n-ZnO junction is turned on). As demonstrated in Figure **5.10c**, the tunneling current for all cases converged around a maximum current on the order of 10^4 A·cm^{-2}. This suggests that the main influence of the parameters of the barrier and its interaction with an applied field, is over the behavior prior to reaching the theoretical maximum tunneling current. Consequently, the rate at which the tunneling current increases will be different depending on the how the barrier and its field-interaction are characterized. The η -V dependence is then a result of the difference in the rate of change of the insufficient model versus the measured results, and does not necessarily imply that many parameterization corrections need to be made. In fact, it is possible that only a single parameter may need to be adjusted in order to yield better model-measurement fits.

Table 5.1: Wave vector taken from model and ratio between the measured and model using 4 nm taken at the same voltage and the corresponding calculated Δx .

Voltage	***k*** (m^{-1})	η	Δx
-0.1	5.5×10^9	5589	1.6 nm
-0.2	5.9×10^9	1947	1.3 nm
-0.4	6.3×10^9	2336	1.2 nm
-0.6	6.7×10^9	1603	1.1 nm
-0.7	7.1×10^9	678	0.9 nm
-0.9	7.4×10^9	727	0.9 nm

As such, the purpose of this technique was to reduce the potential of a multitude of corrections into a single parameter which can be analytically extracted with ease. Its results are discussed in the next section.

5.4.4 EFFECTIVE BARRIER THINNING

Further elaboration on the meaning of Δx with its affect on ψ_m is illustratively depicted in Figure **5.11a**. In the original case, the probabilistic metal electron distribution $|\psi_m|^2$ is portrayed as almost wholly outside the barrier, thus implying that the wave function penetration is miniscule. In this situation, the barrier thickness which is equivalent to the electron's path of least resistance corresponds to the physical thickness of the insulator. Of course, as already discussed the physical barrier thickness resulted in a much lower current densities when taken into account in the model. Assuming the ZnO probabilistic distribution $|\psi_{ZnO}|^2$ is true as it is, what Δx suggests is the error in the distribution of ψ_m at the metal-insulator interface; to correct this the assumption, a revision was required to allow $|\psi_m|^2$ to penetrate into the barrier. Wave function penetration into the barrier have been reported [**112**,**113**,**114**]. Consequently, the path of least resistance for the emitting metal electron that is now allowed exist within the barrier is reduced by Δx effectively thinning the barrier the electron sees (Figure **5.11b**). For a Δx = 1.6 nm, the effective barrier $t_{Ox\text{-}eff}$ becomes 2.4 nm, which was corrected from the physical barrier thickness of 4 nm. In Figure **5.12**, with all other parameters remaining unchanged, the resulting model tunneling current was revealed.

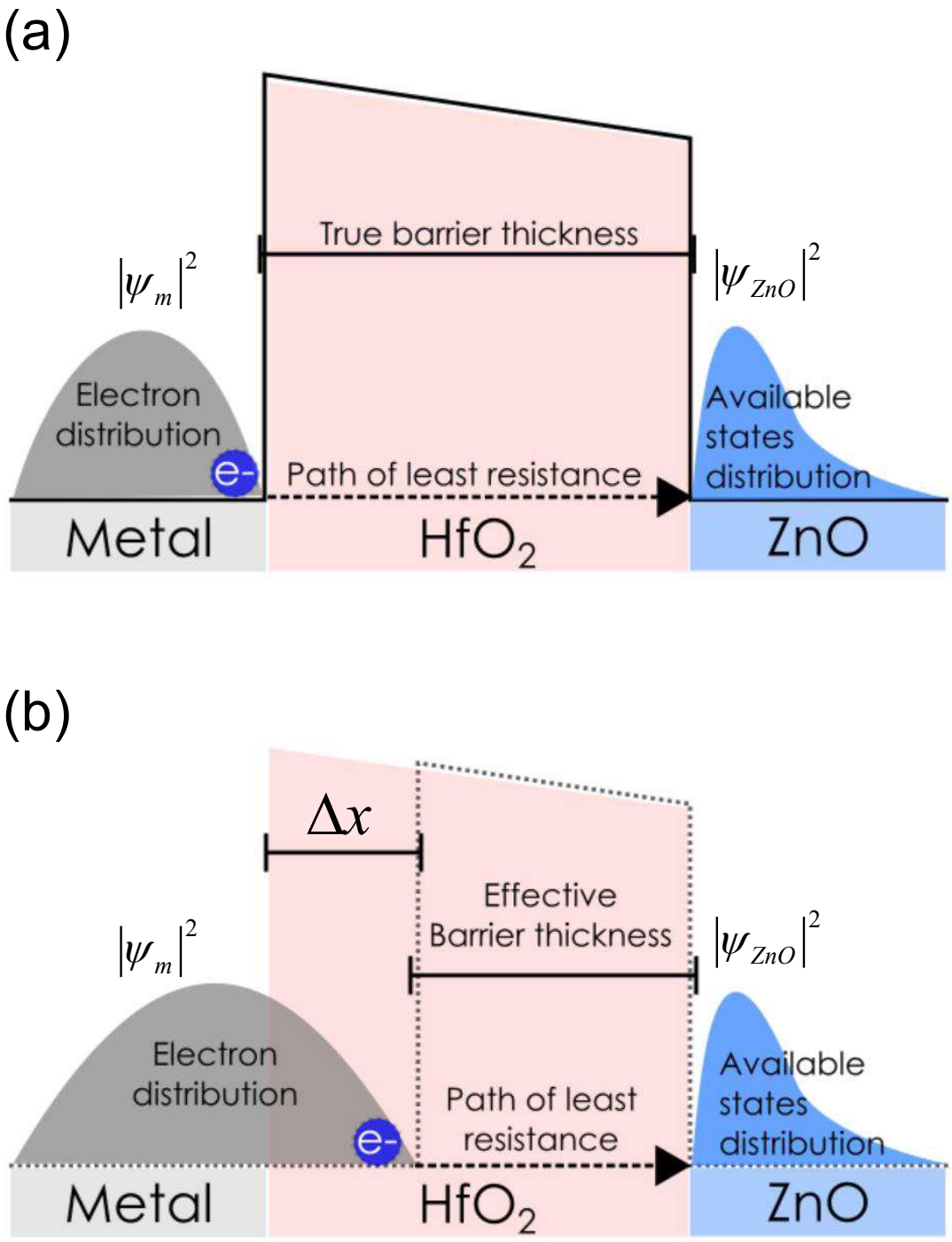


Figure 5.11: The proposed interpretation Δx and the effective barrier thickness. In (a), the barrier thickness is equal to the physical thickness of the HfO_2 layer. In this model, the wave function of the metal barely penetrates the barrier such that electrons primarily exist outside the barrier. On the other hand, the discrepancy in the measured and the initial model is rectified through Δx, it suggests that the metal electron wave function penetrates the barrier by that difference. As shown in (b), this leads to an effective thinning of the barrier.

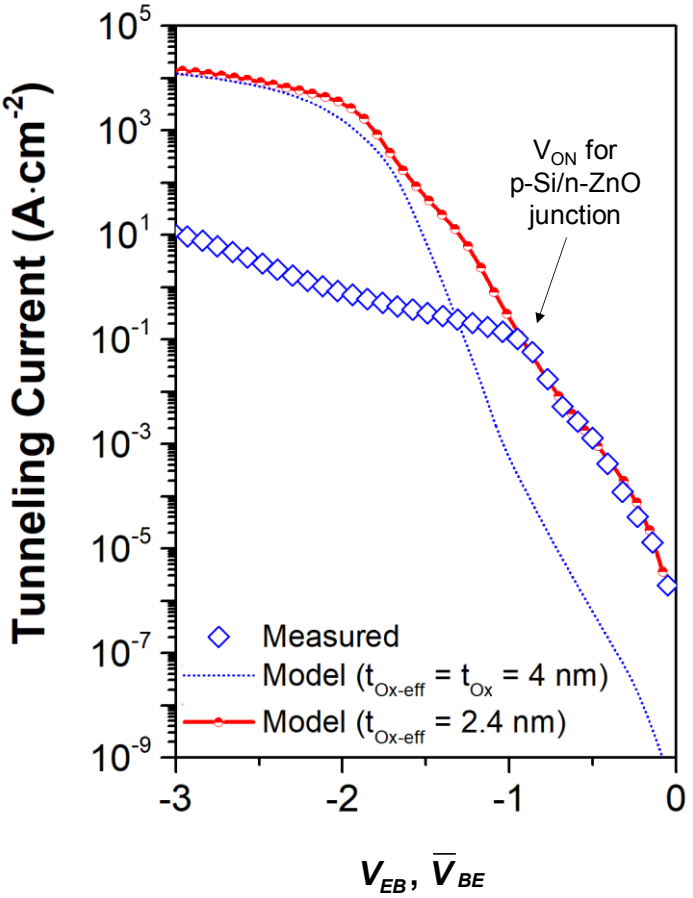


Figure 5.12: The revised model that compensates Δx by effective thinning of the barrier compared to the measured data and the previous models. With the compensation, the revised model provided a strong match with the calibration region. The model also predicts the tunneling current density at voltages below -0.9 V where the current and capacitance began to degrade. At 3 V, the current density reaches 10^4 mA·mm^{-1}.

With the correct applied to the model, we see a strong match at the region where other factors such as pn-junction leakages or series resistance have less impact on the overall output. More specifically, from ~0 V to ~-0.9 V, the fit is above 99% indicating the validity of an effective barrier thinning explanation. Furthermore, a potential design parameter is implied: if current losses can be reduced to nothing, a very high current density can be achieved. This prediction is particularly important because high fidelity circuits such as power converters and amplifiers require higher current throughout from TFTs in order to move past the switching space. In fact, this work proposes that the effective barrier thinning gives rise to an enhancement of tunneling current which is central to the gain mechanism of the TJT.

5.5 DEVICE OPERATIONS

5.5.1 ENERGY BAND PERSPECTIVE

The TJT's complete emitter-base band diagram consists of first the onset of HfO_2 at 0 nm (4 nm thick), followed by a 25 nm ZnO film and ending with the p-Si substrate. At equilibrium, the conduction band offset $E_{C\text{-}offset}$ of 2.26±0.05 eV and a valence band offset $E_{V\text{-}offset}$ of 0.14±0.05 eV as shown in Figure **5.13a**.

When the device is on, ZnO is completely depleted of its majority n-type carriers and is inverted. The p-Si partially accumulates its majority p-type carriers at the p-n junction, but most of the holes are injected into the inversion layer. This is depicted in the simulated band diagram in Figure **5.13b** and diagramed in Figure **5.13c**.

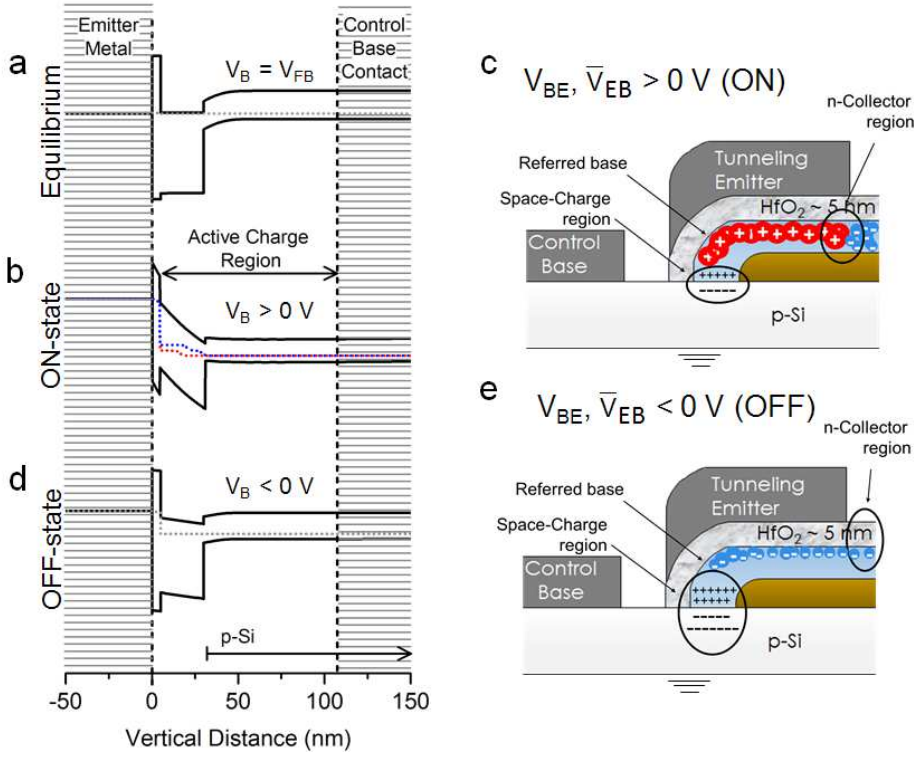


Figure 5.13: Band diagram elaborating on the of Al/HfO_2/ZnO/p-Si tri-heterojunction during a) Equilibrium voltage where V_B = 0 V; b) ON-state indicating the active charge region which determines the minimum film thickness required for a p-type carrier source; and c) the predicted carrier distributions showing the inversion layer or referred base; d) OFF-state and e) the almost fully depleted majority carriers of both ZnO and p-Si.

During OFF-state in Figure **5.13d** and Figure **5.13e**, both ZnO film and p-Si surface are depleted of their majority carriers. This results in a very limited amount of free electrons available to be collected, resulting in low current throughput at the $V_{BE} < V_{ON}$.

5.5.2 GAIN MECHANISM

A closer demonstration of the tunneling gain mechanism in the TJT is revealed in Figure **5.14a**. When the device is on, the bias at the control base with respect to the emitter terminal V_{BE} determines the accumulation of injected holes forming the 2D inversion layer at the n-ZnO valence band edge. Simultaneously, electrons tunnel through the MOS interface beginning from the metal and are subsequently injected into the collector region. The primary current gain mechanism arises from the exacerbation of the Columbic forces between metal electrons and injected holes separated by the barrier layer. In contrast to polysilicon metal gates, the tunneling holes into true metals are not known or reported. In gain mechanisms explored in polysilicon tunneling emitters, it is the effective differential between the electron and the hole that causes this effect. Here, from the band diagram at Figure **5.14b**, the holes do not tunneling across the barrier into metal. Instead, the wave function of metal electrons ψ_M is distorted by the ZnO inversion layer and forces the wave to significantly penetrate the barrier. Owing to this effect, the actual effective barrier experienced by the emitter metal electrons was shown to be $t_{OX\text{-}eff}$ = 2.4±0.5 nm and not the physical barrier of t_{Ox} = 4 nm. The incoming electrons in the ZnO conduction are then ideally swept to collector, completing the transistor action.

Tunneling enhancement leading to current gain at the emitter was only observed when a strong inversion layer was simultaneously present. When the hole channel was instead replaced with a highly depleted ZnO film which was not supplied with a source of holes, like p-Si, even when considering the degradation of current throughput, the measured tunneling current was at least two orders lower.

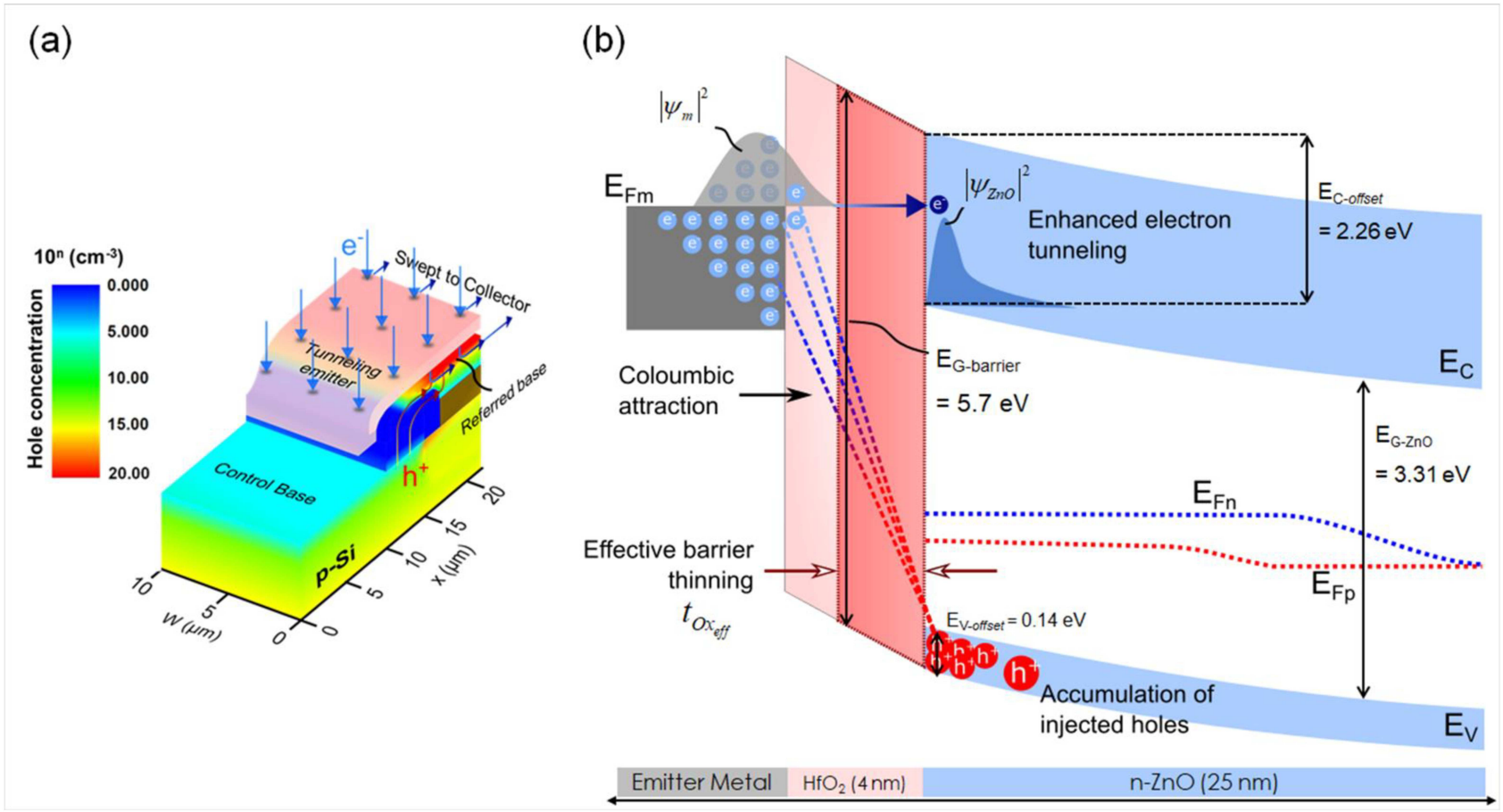


Figure 5.14: A demonstration of the (a) the device's operations where holes from p-Si accumulate underneath the barrier to form the 2D referred base and eventually inverting the ZnO, as a result, the subsequent enhancement in electrons from the metals tunneling through the HfO_2 barrier layer occurs, which is eventually swept to the collector (b) A band diagram illustration of the tunneling emitter at the HfO_2-ZnO interface during ON-state detailing the relevant parameters, the charge transport and the effective barrier thickness.

Figure **5.15** provides a much deeper view of the difference in tunneling currents when there is inversion layer present ("Holes") and without ("Depletion only"). The reason that the depletion-only model did not reveal as dramatic as a correction of current at high voltages compared to the holes case is because there were no additional current loss paths. In other words, for the depletion only MOS structure, which followed traditional tunneling behavior, the ZnO was deposited on top of an insulator and hence the current is primarily lost as series resistance from the emitter to the collector.

Nevertheless, even when comparing modeled tunneling currents in both cases, the theoretical ideal for the current arising with the presence of an inversion layer still showed a remarkable gain between 10^4 and 10^5.

The difference between the current characteristics for the holes measured and holes modeled cases below ~-0.9V corresponded to the junction leakage resulting from the turning-on of the p-Si/n-ZnO junction; this junction leakage also affected the structure's CV characteristics where the capacitance was observed to degrade at <~-0.9 V, hence also needed a CV correction. In fact, due to the turning-on of the pn-junction, the holes at the MOS interface are drawn towards pn-junction instead. With respect to the conductance-voltage curve, we saw this as a loss of charge control. It is for this reason that as the inverted MOS interface loses its holes to the forward biased pn-junction, we observed that the resultant current-voltage behavior of the tunneling emitter trended towards the shape of the depletion-only model and away from the holes model. This is consistent with the proposed mechanism where the presence of holes for a true metal MOS interface played a crucial role in enhancing the tunneling current from the metal to the semiconductor.

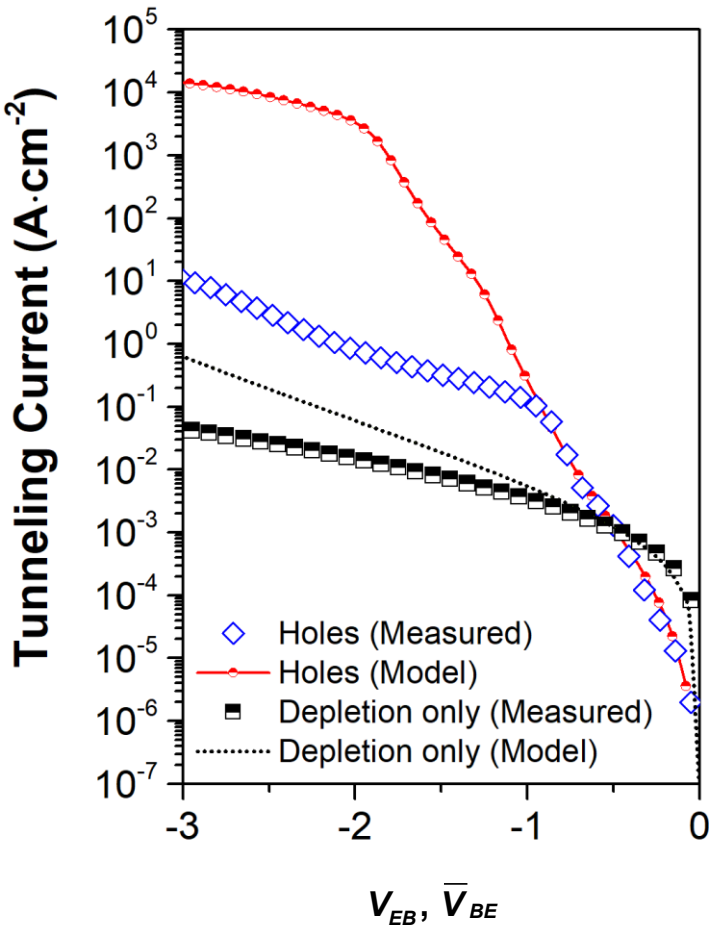


Figure 5.15: The emitter's tunneling current when n-ZnO is operating at inversion ('Holes') and when it is operating without inversion ('Depletion only'). There is a clear effect difference in both the measured and modeled case. In the former, the holes structure was almost 10^2 higher than the depletion only structure. The mode predicts a difference of almost 10^5. The cases with holes, the difference between the measured and the model is a result of a junction leakage at V_{EB} < ~-0.9V due to the turned-on p-Si/n-ZnO junction. This also effected the CV characteristics where the measured capacitance decreased rapidly below the same voltage.

5.5.3 TRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS

Like in a BJT, the tunneling electrons not lost to recombination are eventually swept to the collector. These collected electrons resulted in a characteristic transistor current-voltage (IV) family of curves dependent on the emitter voltage with respect to the base as shown in Figure **5.16a**. To further emphasis the influence of the tunneling emitter, the measurement was taken at the common-base mode and the high potential is taken from the base and grounded at the emitter (V_{BE}). As the field applied between base-to-emitter voltage was

strengthened, the collector current increased. The hole-assisted enhanced tunneling current at the emitter is a key reason why the throughput current density reached as high as ~45 A/mm at $3V_{BE}$ as have been reported [**115**]. electrical degradation of the ZnO film was observed under these power conditions. Consistent with the prior CV results, at >1 V emitter-to-base voltages, almost no current modulation is present and the device can be considered to be off. A clear distinction in the OFF-state and ON-state transconductance is also shown in Figure **5.16b**, indicating a turn on base voltage of around -1.5 V where the device can truly be said to be on. An immediate problem that is discerned is the high collector saturation voltage $V_{CE\text{-}SAT}$. Deeper insight into this issue was explored through a basic TJT compact circuit model and the behavior of the devices were compared at different values of L_{EC}.

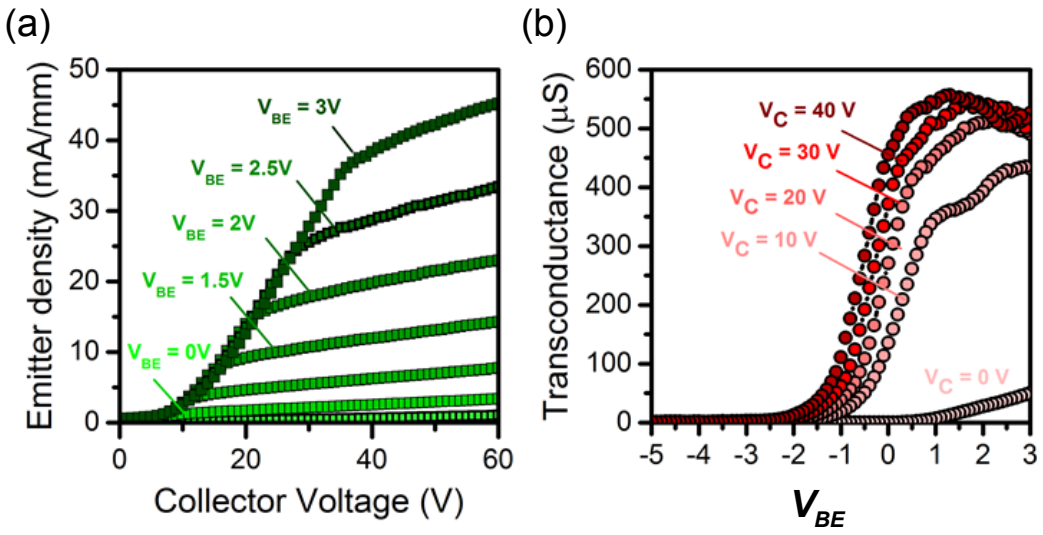


Figure 5.16: The measured TJT family curves in common-emitter mode from V_{BE} = 0V to 3V; (**c**) the transconductance of the TJT in the common-emitter mode.

5.5.4 TJT COMPACT MODEL

Due to the complexity involved with the multitude of junctions in the TJT, many of the parameters were extracted when applying the Ebers-Moll BJT compact model to the TJT

[116]. In Figure 5.17, we break down the elements to two tunneling diodes J_{DT1} and J_{DT2} representing the current at the collector J_{BC} and the emitter J_{BE}, respectively. Two dependent sources also contribute to the over current and is associate with BJT definition of gain. For the overall collector current J_C, the forward gain α_F is applied to the base-to-emitter current J_{BE}, and for the overall emitter current J_E, the reverse gain α_R is applied to the base-to-collector current J_{BC}. Additional parasitics are also identified including contact resistances at the collector R_C, the emitter R_E and most as it will be shown most significantly from emitter to collector R_{CE}.

Finally, another component, G_{leak}, was meant to represent holistically the loss in various junction currents related to the base. Because of the difficulty in capturing the full effects of G_{leak}, the motivation for the model was to elucidate the behavior of the TJT in its absence. In its entirety, G_{leak} is meant to represent the current lost between the base and collector through the silicon nitride substrate, the recombination current between the base and emitter and also the recombination current between the referred base and the collector. Many of these issues primarily arose from using a p-Si substrate and a silicon nitride layer at regions where isolation from ZnO to p-substrate were required. The emitter current was closely investigated because relatively speaking, its characteristics was least influenced by G_{leak}. Nevertheless, there were some effects that remained and could not be deconvoluted during measurements. As such, this served as the driving force behind the compact model analysis.

As we are most interested in the emitter current, from the Ebers-Moll's description of the TJT, we arrive at the full description of the emitter-to-collector current $\bar{J}_{EC}$ as follows:

$$\bar{J}_{EC} = \alpha_{F(V_{BE})} J_{ES} \left(e^{\frac{V_{BE}}{n_e(V_{BE})k_B T}} - 1 \right) - \alpha_{R(V_{BE})} J_{CS} \left(e^{\frac{V_{BE}}{n_e(V_{CE})k_B T}} - 1 \right) \qquad \text{for } V_{CE} \le V_{BE} \text{ V} \qquad (5.9)$$

$$\bar{J}_{EC} = \alpha_{F(V_{BE})} J_{ES} \left(e^{\frac{V_{BE}}{n_e(V_{BE})k_B T}} - 1 \right) - \alpha_{R(V_{BE})} J_{CS} \left(e^{\frac{V_{BE}}{n_c k_B T}} - 1 \right)(1+\lambda) \qquad \text{for } V_{CE} > V_{BE} \text{ V} \qquad (5.10)$$

In this compact model, the ideality factor between the base-emitter n_e was adjusted with respect to the base-emitter voltage to capture the combined effects of emitter tunneling and the junction leakages. Similarly, at $V_{CE} \le V_{BE}$, the ideality factor of the collector-emitter n_c junction was also adjusted with respect to the collector-emitter voltage.

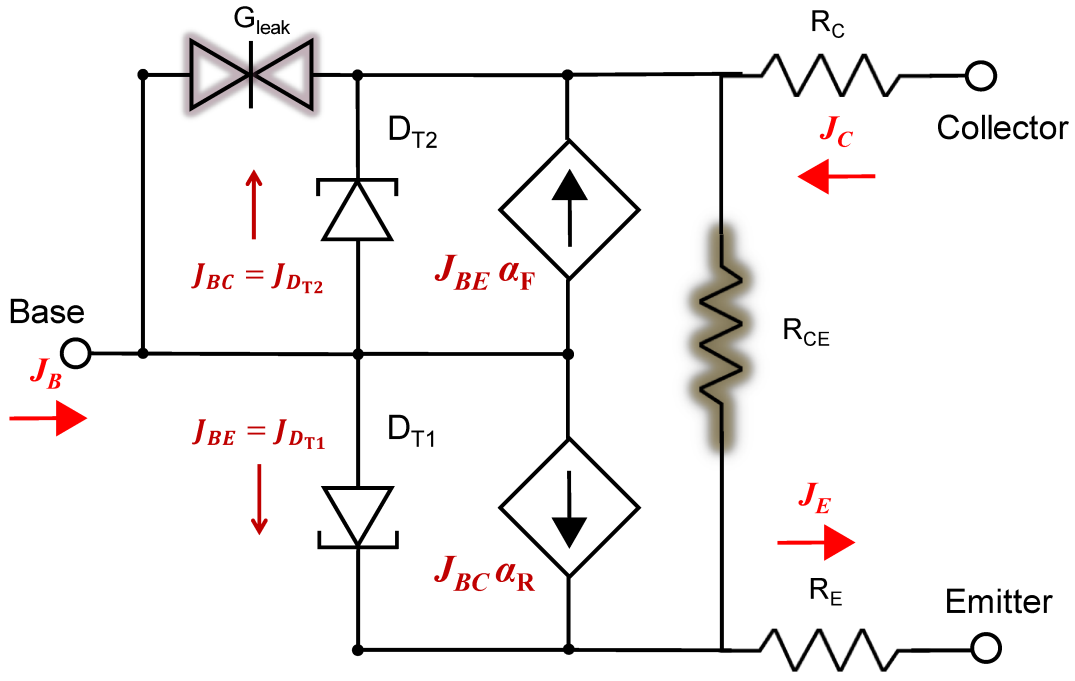


Figure 5.17: The TJT circuit model based on Ebers-Moll highlighting the major sources of non-idealities to be corrected. This includes G_{leak} which represents junction leakages at the base which are eventually collected at the collector. R_{CE} is the parasitic resistance between the emitter and collector. The diodes D_{T1} and D_{T2} represent the tunneling emitter and the referred-base-collector junctions, respectively.

For V_{CE} > V_{BE} V, an extracted parameter λ was applied to the overall output, which captures the voltage dependence on $I_{E,SAT}$. $V_{MOD,sat}$ must be selected such that the current does not explode in magnitude. The contact resistance are ignored as it is considered minor compared to the R_{CE}. In this compact description, D_{T1} and D_{T2} have both their anodes tied to the base dictated by the control base terminal, with the D_{T1} being simply tied to the tunneling emitter as the low potential (cathode), and the latter having the electron current at the tunneling emitter further dictated by the potential at the collector. Since the exact nature of the tunneling diodes are not fully understood, D_{T1} and D_{T2} were modeled using a general junction expression, with varying saturation current density (J_{ES} and J_{CS}) determined by the current at a particular base voltage. Furthermore, ideality factors n_E and n_C are modeled as showing dependence on their respective voltages V_E and V_C up to the ideal saturation knee voltage ($V_{CE,SAT}$ = V_{BE}).

It can be seen from Equation (**5.9**) and (**5.10**) that there are many dependencies on V_{BE} and V_{CE}. To capture some tangible parameters, we took the reverse differential emitter gain β_R which we say is about equivalent β_F and it corresponds to α_R as follows:

$$\beta_R = \frac{\alpha_R}{1-\alpha_R} \approx \beta_F \qquad)$$

To extract the reverse emitter current gain, the base current was taken at the low collector voltages and for each V_{BE} before it could be lost through G_{leak}. The differential gain was than extracted by taking the slope at the corresponding base-to-emitter voltages.

The true saturation emitter current $J_{E,SAT}$ was extracted through extrapolating the current at 0 V by tracing the emitter current that was measured. This value was estimation of the current with the effects of G_{leak}, at collector voltages before base-collector leakages took effect.

Both extracted β_R and $J_{E,SAT}$ are provided in Figure **5.18a** and Figure **5.18b**, respectively.

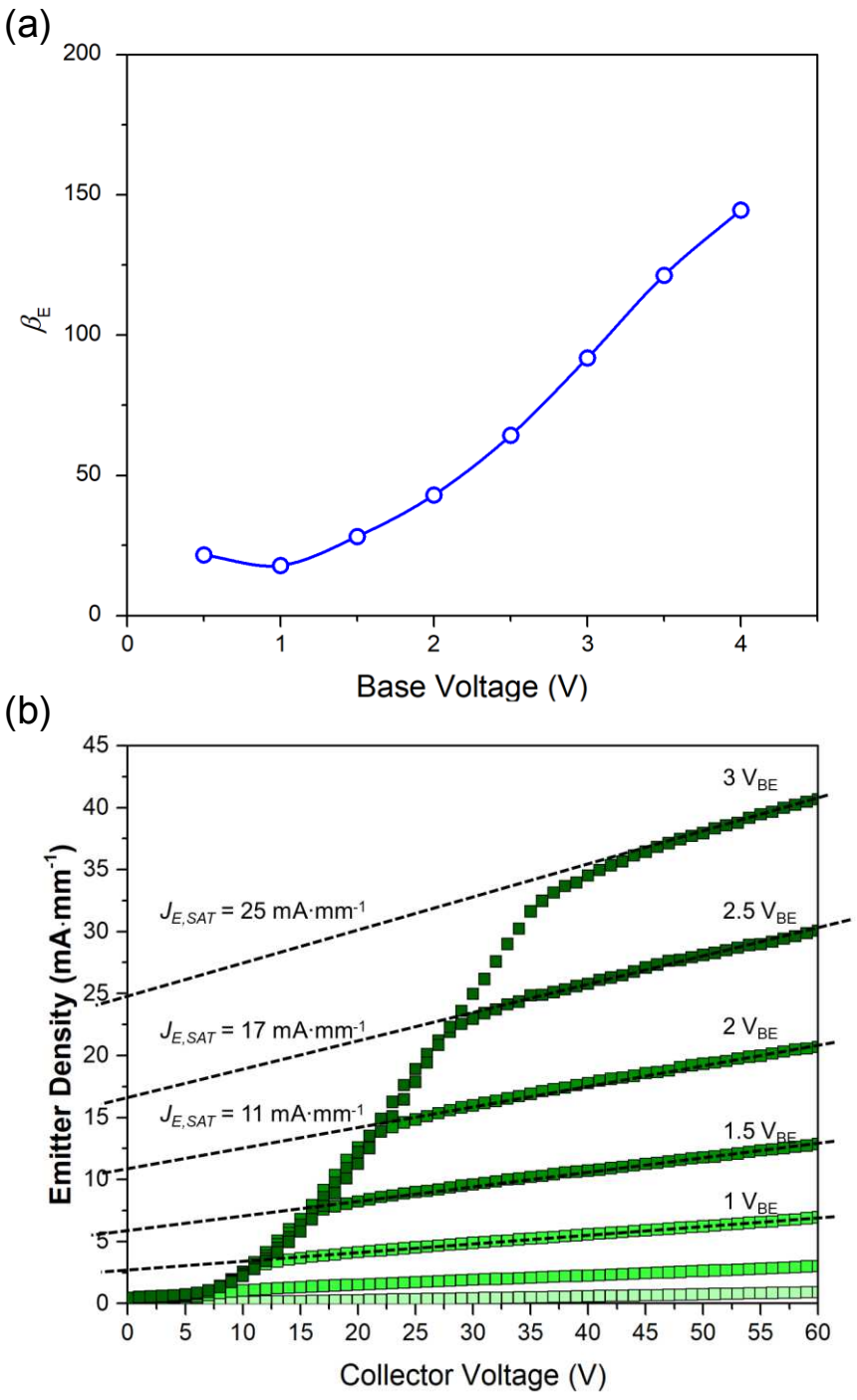


Figure 5.18: The TJT's (a) differential emitter gain for the TJT used to calculate α_R for the compact model and (b) the estimated saturation current independent of junction leakages extrapolated from the slope of the measured current to when V_C = 0 V.

Several other simplifications were made to reduce the complexity of the compact model. For VCE > VBE, nC = 1 and JES = JCS, since both components would have a similar dependence on the tunneling emitter. For all other regions, the parameters were adjusted to achieve a reasonable fit up to VCE = VBE. The goal of this model was to simulate the family of emitter current curves for the condition that VCE,SAT = VBE is true. The simulated curves are given in Figure **5.19** and compared with the measured family of curves.

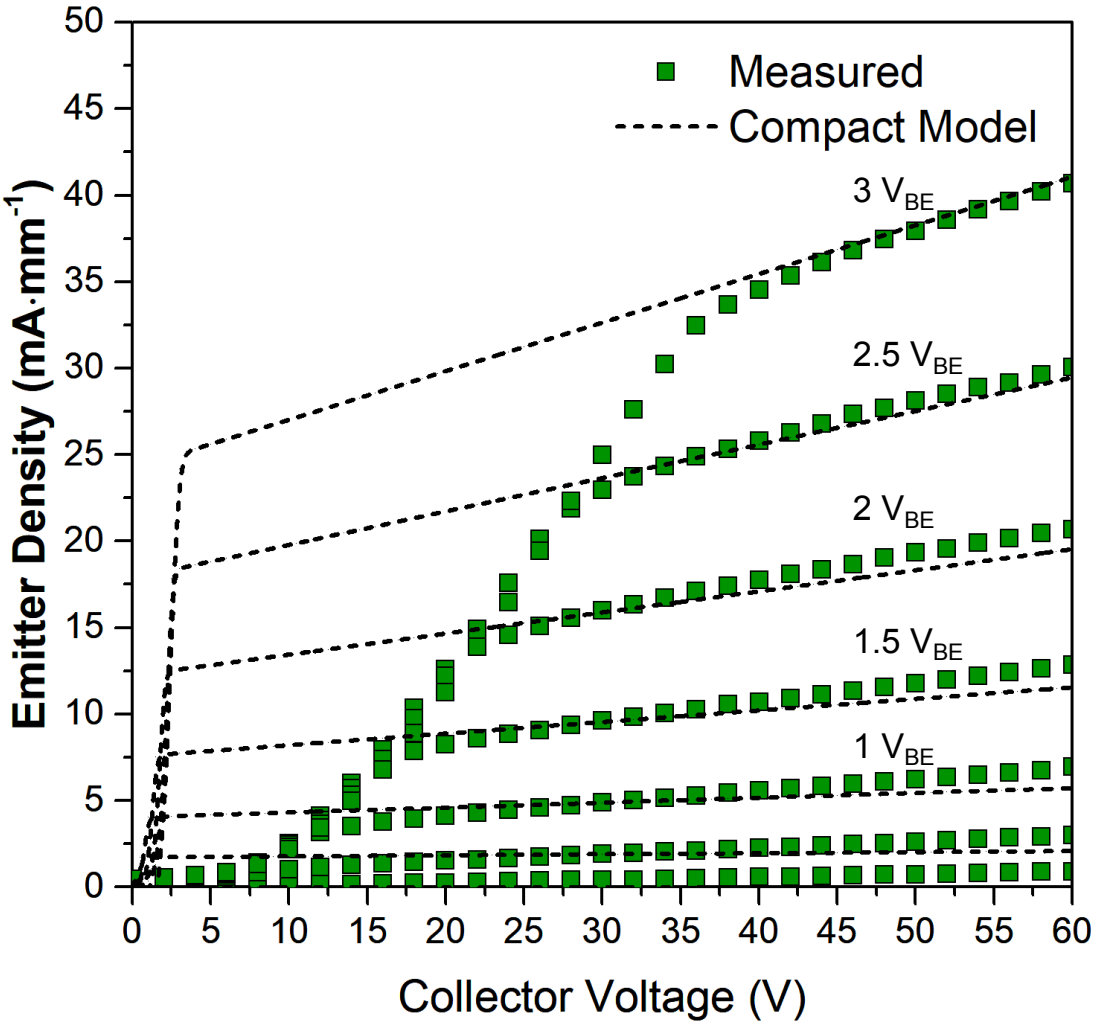


Figure 5.19: The simulated emitter family of curves based on the compact model compared to the L_{EC} = 10 µm TJT measured results. The goal of the compact model was understand the behaviour of the TJT without the affects of recombination affects of G_{leak} such that $V_{CE,SAT} = V_{BE}$.

At simulated voltages below the simulated saturation voltage $V_{CE,SAT} = V_{BE}$, the current behaved as expected for a BJT that is biased via voltage rather than current biasing, as is the convention. Unlike the measured data, the current at the triode region do not converge, suggesting that referred base does affect the emitter current at $V_C < V_{CE,SAT}$

We also considered that reducing L_{EC} would lead to an improvement to the experimental saturation voltage behavior because the recombination region would also by physically reduced. To verify this, a L_{EC} = 2 μm device was measured and compared with the same compact model (Figure **5.20**).

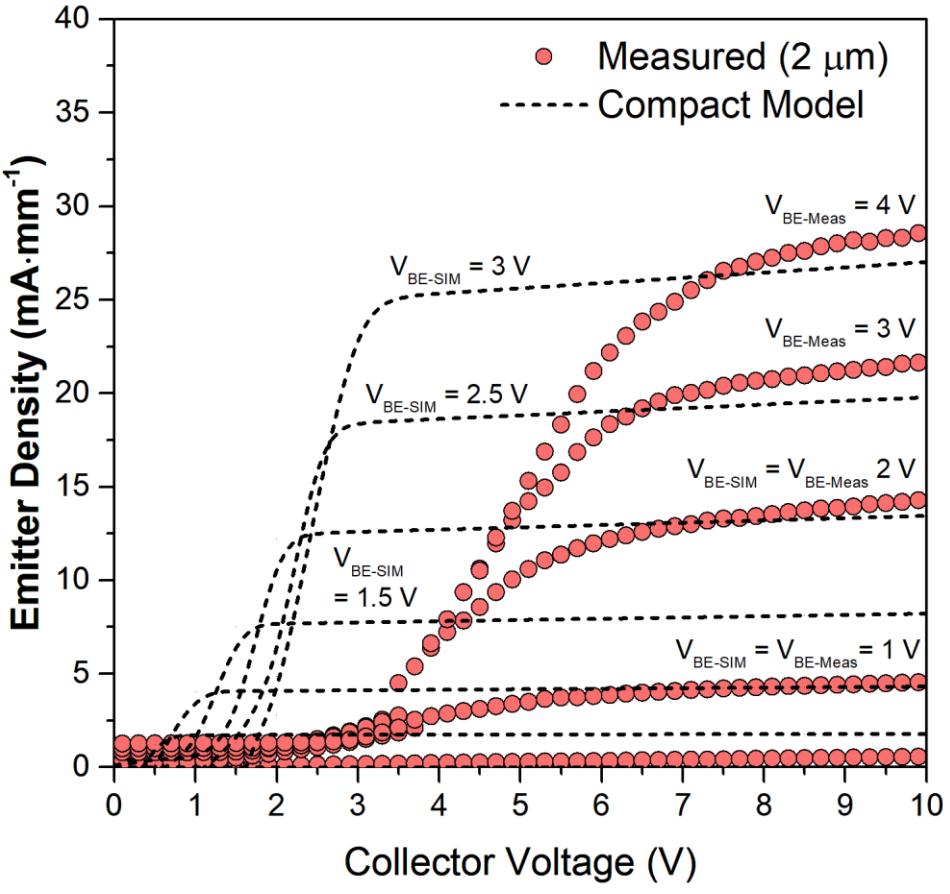


Figure 5.20: The measured results for a L_{EC} = 2 μm TJT with the compact model. Reducing the emitter to collector distance reduced both R_{EC} and the current lost due to recombination. As V_{BE} increases, the measured data revealed a lower transconductance than the predictions of the compact model, indicating that additional some degradation in current at higher base-emitter voltages.

The decreased L_{EC} diminished the electrons lost to recombination and the magnitude R_{EC} both which resulted in an extending linear region. Simulation of the hole and electron distribution for various lengths of L_{EC} starting from the onset of the emitter to the collector onset were also performed. In this simulation, L_{EC} (see Figure **5.6b**) was varied from 0.25 µm to 8 µm. Both the hole (green) and electron (purple) concentration was measured under the entire emitter region to the entire collector region. It is seen clearly in Figure **5.21a** (holes) and Figure **5.21b** (electrons) that the potential recombination path decreased in the high hole concentration area, which begins at emitter-edge facing the collector and terminates at the collector onset. This was especially critical because the concentration of both carrier species remain similarly high between L_{EC} with minimal tapering for longer emitter-to-collector distances.

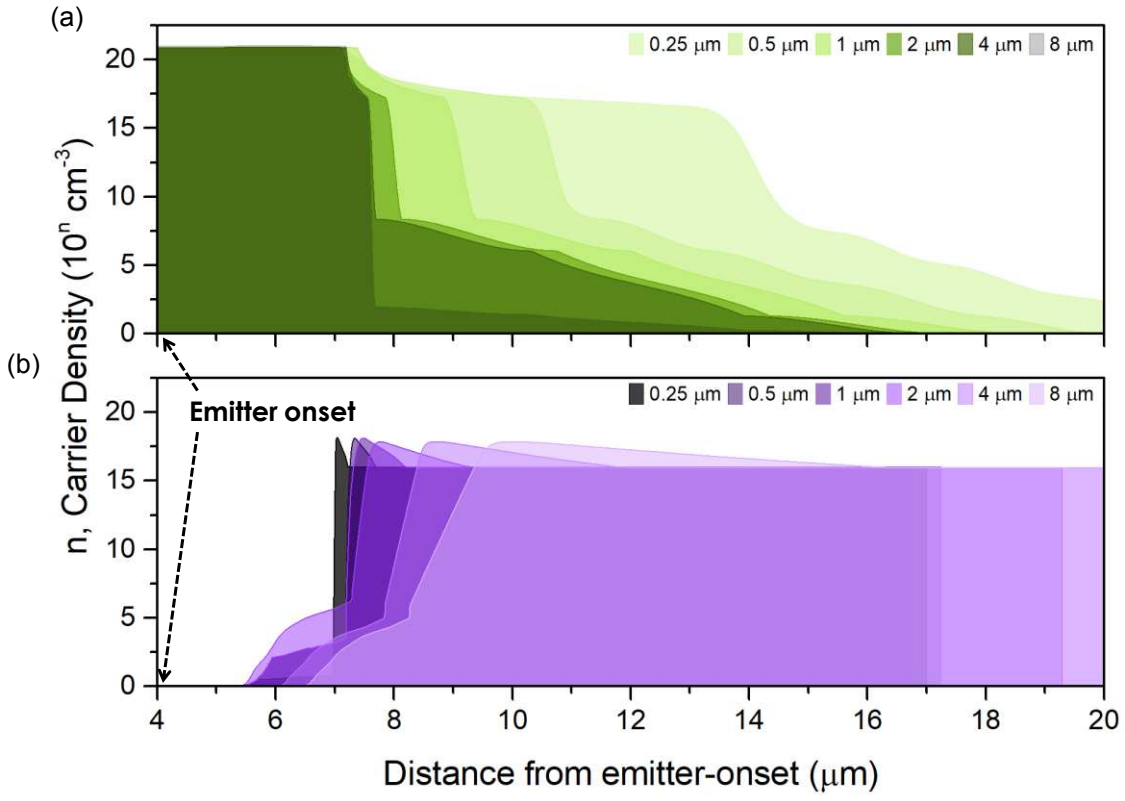


Figure 5.21: Simulated distribution of (a) holes and (b) electrons from the on-set of the emitter where the inversion channel is formed to the on-set of the collector for various emitter-collector distances L_{EC}. Some of the advantages of a scaled L_{EC} is a smaller recombination region and shorter resistance path.

While indeed the saturation voltage did improve, it observed that beyond 2 V, the transconductance of the measured device reduced as the matching base-to-emitter voltage V_{BE} was off about by about 0.5 V. This effect is similarly seen in the tunneling current analysis where, after a certain voltage (-0.9 V), the rate at which the tunneling current density increase was slowed. So in reducing the emitter-collector distance the recombination current between the referred base and the collector region is attenuated resulting in improved $V_{CE,SAT}$. On the other hand, the control over the transfer current with respect to V_{BE} either lessened due to loses in the base-to-emitter junction or additional current is gained beyond measured saturation voltages through silicon nitride isolation layer where the collector voltages are relatively high.

From results shown in Figure **5.22**, the isolation material of higher reliability was utilized to understand the effects of leakages at this isolation region where silicon nitride (Si_xN_y) was used. In these set of devices, an additional 5 nm of high quality ALD Si_xN_y on top of a 45 nm low pressure chemically vapor deposited (LPCVD) Si_xN_y was used between ZnO and p-Si at the non-overlapping regions. Since the current density reduced as the L_{EC} increased with an improved isolation material, we conclude that inadequate isolation of p-SI by the silicon isolation layer does increase the emitter current at higher collector voltages.

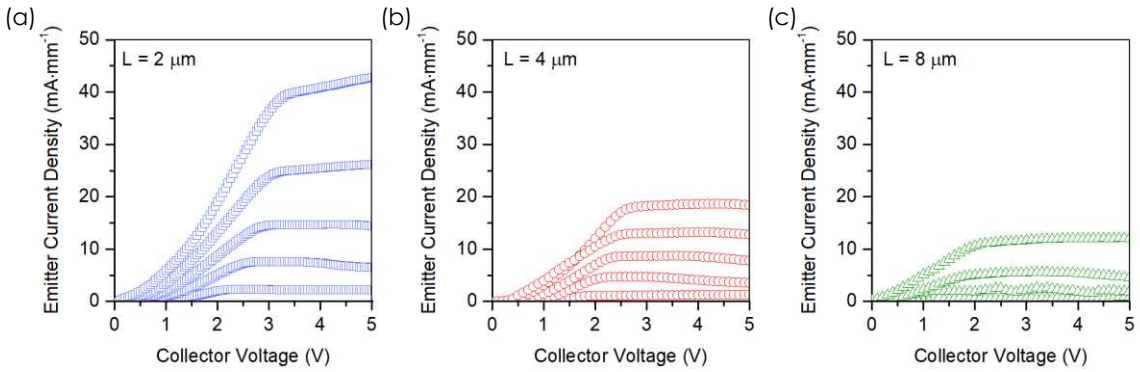


Figure 5.22: Measured family of emitter curves with improved isolation layer between n-ZnO and p-Si at non-overlapping region. The devices varied only in emitter-to-collector distances where (a) L_{EC} = 2 μm, (b) L_{EC} = 4 μm and (c) L_{EC} = 8 μm. V_{BE} was taken from 0 V to 5 V.

Figure **5.23** also suggests that scaling of L_{EC} will increase current density which is important for applications requiring high current transistors while simultaneously minimizing many of the shortcomings for longer dimensions.

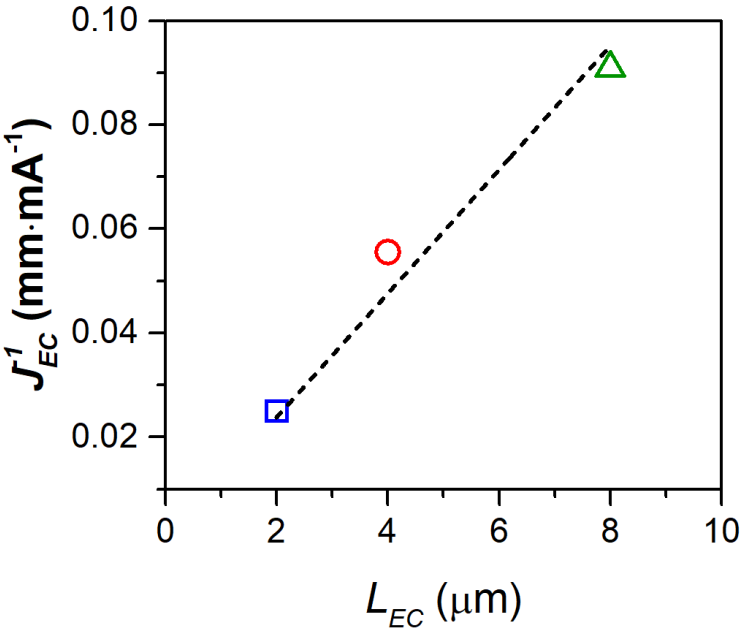


Figure 5.23: With an improved silicon nitride layer, current leakage from of the p-Si substrate to the collector electrode was minimized revealing increasing current densities as L_{EC} is shortened, suggesting that the device can improve its performance at scaled dimensions.

5.6 DISCUSSIONS & CONCLUSIONS

The TJT is a novel and very promising device that takes advantage of the tunneling emitter phenomena. By forming an inversion layer at MOS junction emitter, the TJT takes advantage of the enhancement of current from emitter as a result of effective barrier thinning. This thinning is explained by the penetration of the metal wave function into the barrier oxide and is increased due to the metal electrons attraction to the hole gas layer at the insulator-semiconductor interface. Such an effect is not observed in ZnO that is unable to invert.

The interpretation of Δx also has more than one valid manifestation. Some of additional interpretations of Δx are given in Figure **5.24** all of which are mathematically equivalent. For instance, instead of only being accounted for in $|\psi_M|^2$, the wave function distribution of ZnO $|\psi_{ZnO}|^2$ can also be the solely adjusted by Δx. Another case is that both $|\psi_M|^2$ and $|\psi_{ZnO}|^2$ share parts of the sum that total Δx as illustrated in Figure **5.24b**. In this instance, Δx_1 is associated with the distribution of $|\psi_M|^2$ and Δx_2 is associated with $|\psi_{ZnO}|^2$. The total Δx is simply $\Delta x_1 + \Delta x_2$.

All the proposed physical interpretations are mathematically equivalent according to the model used in this study and result in the same effective barrier thickness with respect to what is seen by the tunneling electron.

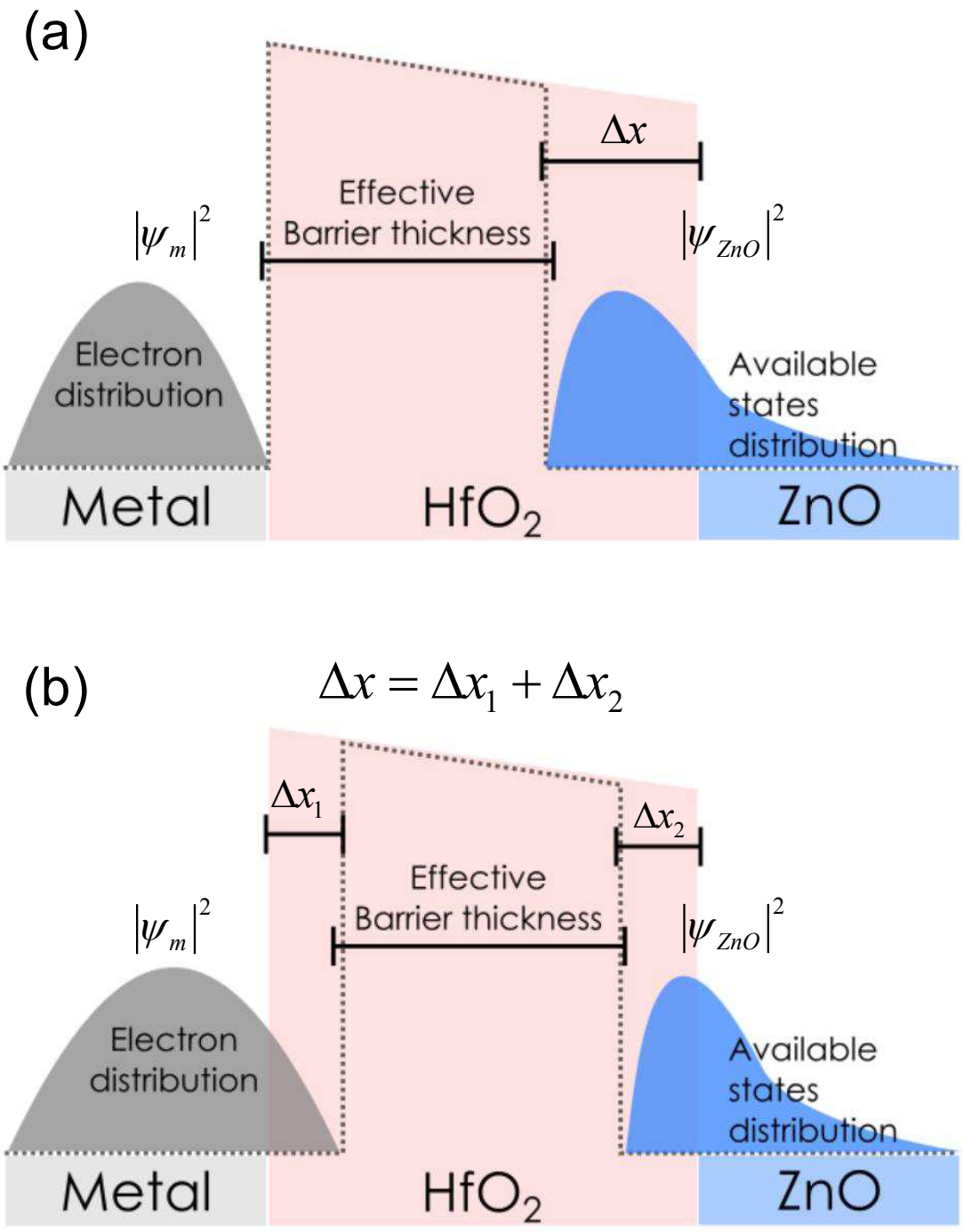


Figure 5.24: Alternative proposed interpretation of Δx and the effective barrier thickness. In (a) the ZnO electron wave function penetrates the barrier; and, (b) both the metal and the ZnO distribution penetrate the barrier by Δx_1 and Δx_2. The sum of which gives Δx. These cases also lead to an effective thinning of the barrier.

It is important to state that what is proposed here is not that the physical barrier thickness is actually thinner due to the presence of holes. Further to that, the effects of oxide defects were also considered to be miniscule. The reasons for this are two-fold: 1) the measured hysteresis of the CV curve was miniscule <50 meV, and 2) because we compared with the measured results of the MOSCAP without a hole supply (depletion only), we observed a higher current with the hole supplied MOSCAP, despite having the same ZnO and HfO_2 recipe and thicknesses. The conclusion that can be made are that:

I. Effective barrier thinning is able to account for the enhanced tunneling observed for a true metal MOS with a n-type wide-bandgap semiconductor supplied with holes at the interface operating at inversion
II. Effective barrier thinning is one physical explanation to the penetration of the probabilistic distribution by a total Δx into the barrier of either the metal electrons $|\psi_M|^2$, the ZnO available states $|\psi_{ZnO}|^2$ or a combination of both.
III. Mathematically, these interpretations are indistinguishable and the effective thinning cannot be explained solely due to defects in the oxide barrier.
IV. This model is effective at predicting the tunneling current if the charge is not lost due a forwarded biased pn-junction.

What this analysis provided was the high potential of the TJT's performance as predicted by the tunneling current with shortcomings of the prototype improved or entirely removed. As Through design improvements, the TJT can reach current densities as high as 10^5 A·cm^{-2} at $|V_{BE}|$ = 3 V opening up RF applications for flexible electronics.

There several methods to improve the current form TJT but two of particular importance are: 1) to replace a p-type substrate with a p-type mesa so as to eliminate the need for a high quality isolation layer; and, 2) to scale the traversing dimensions to reduce unwanted effects. Both of these solutions are aimed at minimizing and diminishing the undesirable affects of

recombination and leakages which ultimately degrade the performance of the TJT. Unlike in longer devices, widening the width of the devices did not suffer the same affects, as we expect. This can be inferred because all experimentally obtained raw currents were normalized to the widths of the emitter contacts varying from 10 μm to 50 μm, yet the extracted current densities showed consistency among the prototype design.

6 CONCLUSIONS & FUTURE WORK

6.1 BOOST CONVERTER REQUIREMENTS

We began by conceiving a self-oscillating boosting circuit. A circuit which was meant to fulfill the very real demand of energy harvesting electronics that is low in cost and is directly integrateable for immediate utilization. This boosting circuit had itself had demands from its constituent elements. What was attempted to build those elements with low cost materials from scratch. For instance, of the several elements that makes the circuit whole, we focused on those which are arguably the biggest problems in the field of electronics.

For instance, the first problem we approached is the matter of area and inductance. The inductor needed an inductance of at least 50 nH while still using a single-layer and should not consume an unreasonably large area. The solution was a fractal loop inductor which achieved an inductance ration of 44 nH with the third order iteration, a 9.9 times increase from its base/zeroth order iteration which consumed the same area.

The second problem was realizing a transistor which required a current density higher than what can be achieved by modern TFTs. Because of the monopolar nature of these thin-film FETs, there is a fundamental limitation in current output for this architecture. As such they cannot fulfill some of the power requirements of the boosting circuit. The TJT at its current form cannot fulfill the full current demands of a boost converter. The switching transistor M_{SWITCH} posses a particular challenge because its current density requirements are well into the power level on the order of 10^4 A·cm^{-2}. On the other hand, at 3 V the TJT reached a current density 2250 A·cm^{-2} which meets the requirements of M_{OSC}, the oscillating transistor of the self-oscillating power converter.

The TJT does nonetheless vastly outperform other TFTs (Figure 6.1), and shows promise converters and amplifying circuits requiring high performance thin-film transistors.

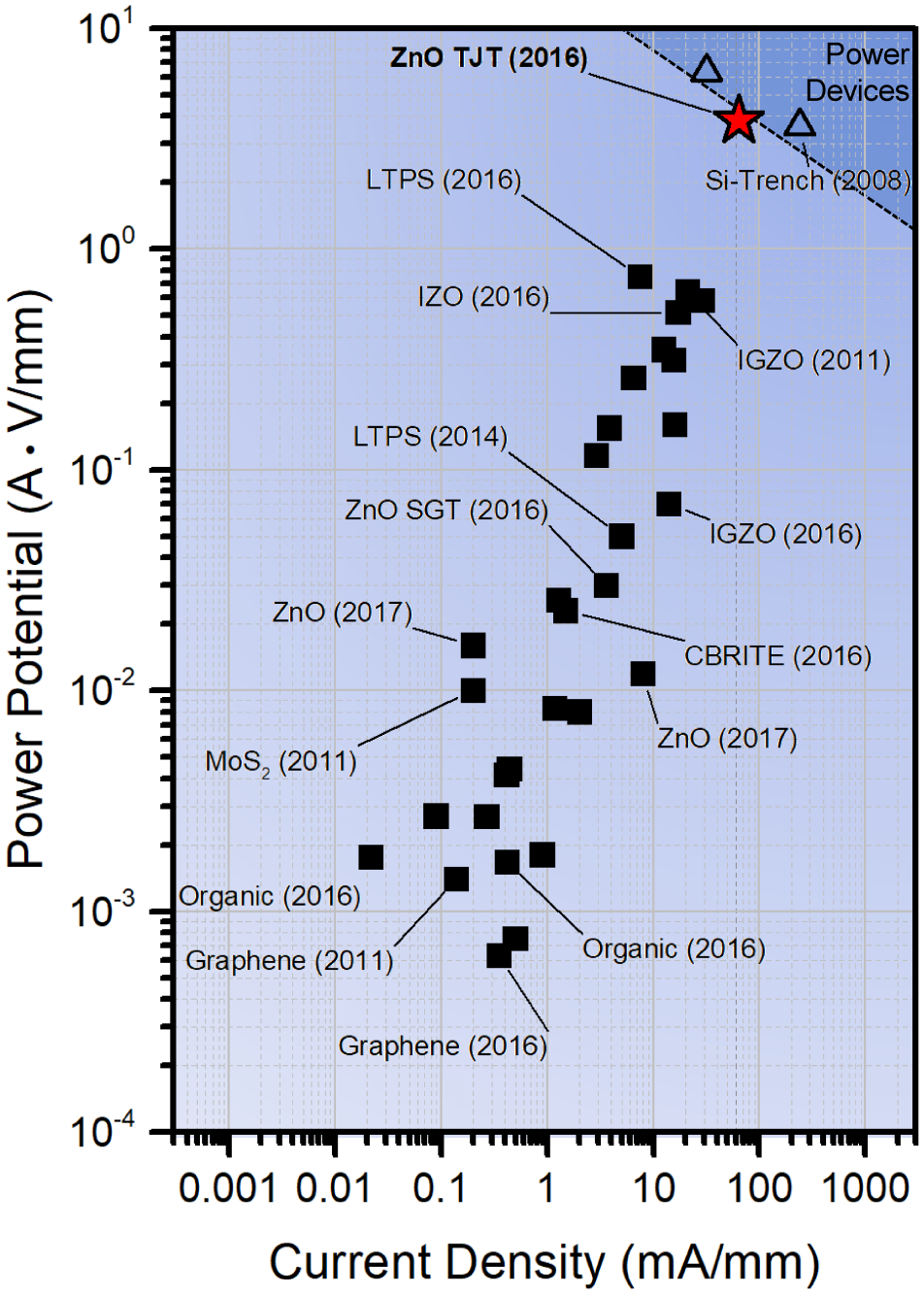


Figure 6.1: The TJT power rating density and current density performance comparison to other devices normalized to the gate/base width. The power rating was determined by extracting the highest drain/collector current density at the highest drain/collector voltage provided by the IV family curves of the corresponding literature. The ZnO/p-Si TJT is shown to have a power rating of 3.81 VA·mm^{-1} and a current density of 63.5 mA·mm^{-1}, which is the highest for any TFT to date.

6.2 FUTURE WORK

Simple power boost converters utilizing the TJT have been designed to be experimentally tested. The voltage applied at the base of the switching TJT can be controlled by an external signal generator. To increase the current throughput of the TJT, the base voltage could be further increased. At 10 V_{BE} the current density reached as high as 115 mA·mm^{-1} with a collector bias of 80 V without breakdown of the device (see Figure **6.2**).

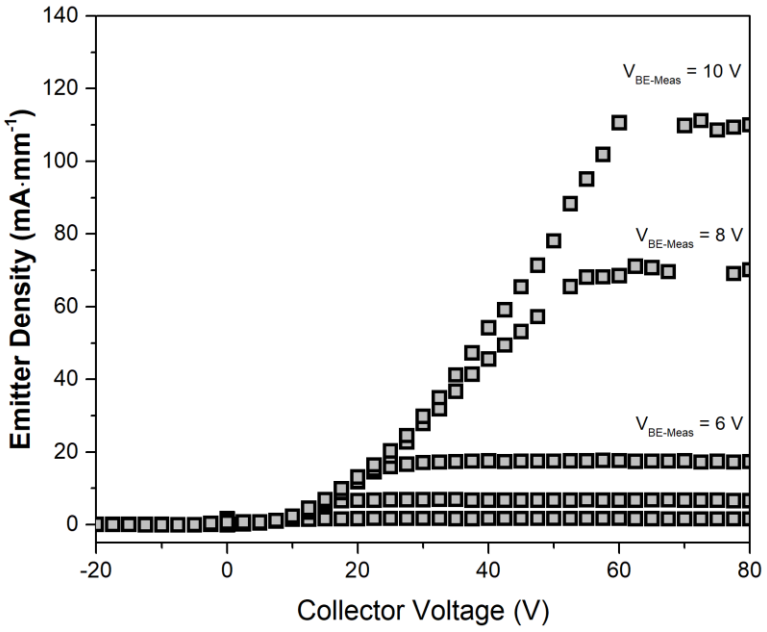


Figure 6.2: The TJT's current density can reach as high as 115 mA·mm^{-1} when biased at a higher base voltage. In this case, the high density was reached at a bias of 10 V_{BE} and 80 V_{CE}. The TJT did not exhibit breakdown at these operating values and thus can be used for applications requiring power tolerances.

A simple boost converter layout is given in Figure **6.3**. A very large TJT with a width of 1 mm and a length of 2 µm is used in order to reach high currents required for the boost converter. Due to limitations of the speed of the switch, a large spiral inductor was designed to achieve an inductance of ~450 nF. With future improvements of the TJT cut-off frequency, fractal inductors can be utilized instead of large spiral inductors. An alternate layout replaced the spiral inductor with two electrodes to accommodate 2 mm by 2.8 mm surface mount inductor with larger inductance ratings to ensure continuous current.

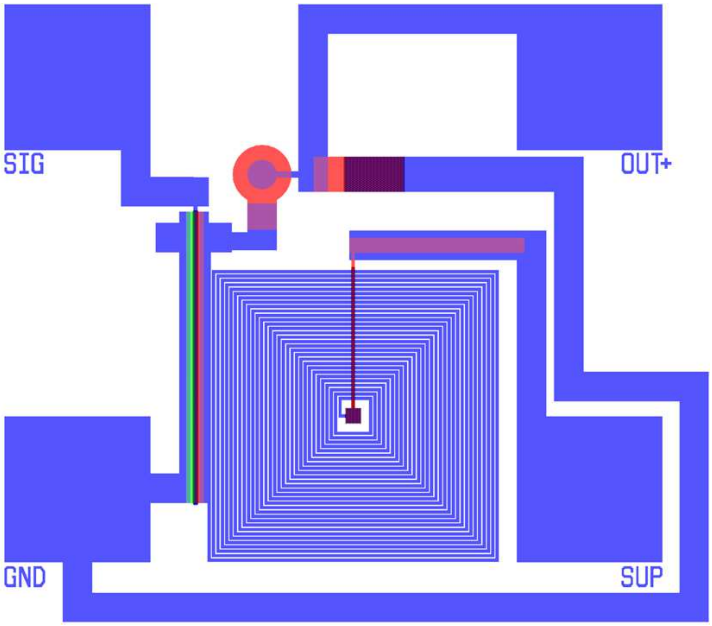


Figure 6.3: Simply single-TJT boost converter layout. The TJT has a W = 1 mm and a L_{EC} = 2 µm. In this design, the TJT acts as a switch to control the current through the inductor. An external signal generator must be used to apply a pulse signal to the base at "SIG". The spiral inductor was designed to provide an inductance of 0.4 µH, with 40 turns with 10 µm wide electrodes spaced apart by 5 µm. A ZnO Schottky diode and MOSCAP are used as the rectifier and the ripple-reduction capacitor.

Finally, it is crucial that a high p-type semiconductor that can self-align replaces a p-type silicon substrate used in this work. According to simulations, an 80 nm p-type doped at 10^{17} cm^{-3} is sufficient to form a highly doped base at the barrier-semiconductor interface of ZnO. What is shown in this work is the prototype of a high performing thin-film transistor which has the potential to reach densities rivaling devices used in high fidelity circuits usually saved of bulk semiconductor based transistors. This opens up fields where the current manifestations of TFTs have been largely unable to break due to the high electrical demands complex circuits such as power converters and complex amplifiers. With further boosting of the performance, the TJT can reach current densities that enable RF frequency operations as required in RFID circuits. For low temperature and biocompatible materials such as ZnO, the prospects for accelerating the fast growing market of additive electronics for applications in the internet of thin (IoT) are significant. Overall, the realization of the TJT's full potential will

ultimately substantial impact a rapidly expanding thin-film electronics industry and give rise to new renaissance of electronics in a largely unexplored space.

REFERENCES

CHAPTER 1

[1] Rim, Y. S., Chen, H., Zhu, B., Bae, S. H., Zhu, S., Li, P. J., ... & Yang, Y. (2017). Interface Engineering of Metal Oxide Semiconductors for Biosensing Applications. *Advanced Materials Interfaces*.

[2] Sun, Yugang, and John A. Rogers. "Inorganic semiconductors for flexible electronics." Advanced Materials 19, no. 15 (2007): 1897-1916.

[3] Forrest, Stephen R. "The path to ubiquitous and low-cost organic electronic appliances on plastic." *Nature* 428, no. 6986 (2004): 911-918.

[4] Lazarus, N., Meyer, C.D., & Bedair, S.S. (2014, April). Fractal Inductors. Magnetics, IEEE Transactions on, 50(4), 1-8.

[5] Burghartz, J. N., Edelstein, D. C., Jahnes, C. V., & Uzoh, C. E. (2000). U.S. Patent No. 6,114,937. Washington, DC: U.S. Patent and Trademark Office.

[6] Kawabe, K., Koyama, H., & Shirae, K. (1984). Planar inductor. Magnetics, IEEE Transactions on, 20(5), 1804-1806.

[7] Bahl, I. J. (2003). Lumped elements for RF and microwave circuits. Artech House Publishers.

[8] Stojanović, G., Radovanović, M., & Radonić, V. (2008). A new fractal-based design of stacked integrated transformers. Active and Passive Electronic Components, Hindawi Publishing Corp. 2008

[9] Werner, D. H., & Ganguly, S. (2003). An overview of fractal antenna engineering research. Antennas and Propagation Magazine, IEEE, 45, 38-57.

[10] Xu, H. X., Wang, G. M., & Liang, J. G. (2011). Novel CRLH TL metamaterial and compact microstrip branch-line coupler application. Progress In Electromagnetics Research C, 20, 173-186.

[11] Samavati, H., Hajimiri, A., Shahani, A. R., Nasserbakht, G. N., & Lee, T. H. (1998). Fractal capacitors. Solid-State Circuits, IEEE Journal of, 33(12), 2035-2041.

[12] Lacour, S. P., Chan, D., Wagner, S., Li, T., & Suo, Z. (2006). Mechanisms of reversible stretchability of thin metal films on elastomeric substrates. Applied Physics Letters, 88(20), 204103.

[13] Li, T., Huang, Z., Suo, Z., Lacour, S. P., & Wagner, S. (2004). Stretchability of thin metal films on elastomer substrates. Applied Physics Letters, 85(16), 3435-3437.

[14] Graz, I. M., Cotton, D. P., & Lacour, S. P. (2009). Extended cyclic uniaxial loading of stretchable gold thin-films on elastomeric substrates. Applied Physics Letters, 94(7), 071902.

[15] Nomura, K., et al. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. Nature 432, 488-492, (2004).

CHAPTER 2

[16] Kazimierczuk, Marian K. Pulse-width modulated DC-DC power converters. John Wiley & Sons, 2008.

[17] Nowakowski, R. and King, B. Challenges of designing high-frequency high-input-voltage DC/DC converters. *TI: Analog Applications Journal 215.* 28-31, (2011).

[18] Rivas, J. M., Jackson, D., Leitermann, O., Sagneri, A. D., Han, Y., & Perreault, D. J. (2006, June). Design considerations for very high frequency dc-dc converters. In Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE (pp. 1-11). IEEE.

CHAPTER 3

[19] Best, S. R., & Morrow, J. D. (2002). The effectiveness of space-filling fractal geometry in lowering resonant frequency. Antennas and Wireless Propagation Letters, IEEE, 1(1), 112-115.

[20] Robin, T., & Souillard, B. (2007). Electromagnetic properties of fractal aggregates. EPL (Europhysics Letters), 21(3), 273.

[21] Clayton, P. (2010). Inductance: loop and partial. Wiley-IEEE Press. 126-130.

[22] Falconer, K. (2003). Fractal geometry: mathematical foundations and applications. Wiley. 36-43

[23] Mandelbrot, B. B., Gefen, Y., Aharony, A., & Peyriere, J. (1985). Fractals, their transfer matrices and their eigen-dimensional sequences. Journal of Physics A: Mathematical and General, 18(2), 335.

[24] Maric, A., Radosavljevic, G., Zivanov, M., Zivanov, L., Stojanovic, G., Mayer, M., & Keplinger, F. (2008, October). Modelling and Characterisation of Fractal Based RF Inductors on Silicon Substrate. International Conference on Advanced Semiconductor Devices and Microsystems, 2008. ASDAM 2008. (pp 191-194).

[25] Wang, G., Xu, L., & Wang, T. (2012, November). A Novel MEMS Fractal Inductor Based on Hilbert Curve. 2012 Fourth International Conference on Computational Intelligence and Communication Networks (CICN), (pp. 241-244).

[26] Samavati, H., Hajimiri, A., Shahani, A. R., Nasserbakht, G. N., & Lee, T. H. (1998). Fractal capacitors. Solid-State Circuits, IEEE Journal of, 33(12), 2035-2041.

[27] Shalaev, V. M. (1996). Electromagnetic properties of small-particle composites. Physics Reports, 272(2), 61-137.

CHAPTER 4

[28] HLLIBRAND, J., and R. D. Gold. "Determination of the impurity distribution in junction diodes from capacitance-voltage measurements." Semiconductor Devices: Pioneering Papers. 1991. 191-198.

[29] Schroder, Dieter K. Semiconductor material and device characterization. John Wiley & Sons, 2006.

[30] Hu, Chenming. Modern semiconductor devices for integrated circuits. Prentice Hall, 2010.

[31] Von Hauff, P., et al. "ZrO2 on GaN metal oxide semiconductor capacitors via plasma assisted atomic layer deposition." *Applied Physics Letters* 102.25 (2013): 251601.

[32] Balog, M., et al. "Chemical vapor deposition and characterization of HfO2 films from organo-hafnium compounds." Thin Solid Films 41.3 (1977): 247-259.

[33] Kukli, Kaupo, et al. "Comparison of hafnium oxide films grown by atomic layer deposition from iodide and chloride precursors." Thin Solid Films 416.1 (2002): 72-79.

[34] Kim, Hyoungsub, Paul C. McIntyre, and Krishna C. Saraswat. "Effects of crystallization on the electrical properties of ultrathin HfO 2 dielectrics grown by atomic layer deposition." Applied physics letters 82.1 (2003): 106-108.

[35] Cho, M-H., et al. "Thermal stability and structural characteristics of HfO 2 films on Si (100) grown by atomic-layer deposition." Applied physics letters 81.3 (2002): 472-474.

[36] Sim, J. H., et al. "Effects of ALD HfO2 thickness on charge trapping and mobility." Microelectronic Engineering 80 (2005): 218-221.

[37] Senzaki, Yoshihide, et al. "Atomic layer deposition of hafnium oxide and hafnium silicate thin films using liquid precursors and ozone." Journal of

Vacuum Science & Technology A: Vacuum, Surfaces, and Films 22.4 (2004): 1175-1181.

[38] Liu, Xinye, et al. "ALD of hafnium oxide thin films from tetrakis (ethylmethylamino) hafnium and ozone." Journal of the electrochemical society 152.3 (2005): G213-G219.

[39] Seiwatz, Ruth, and Mino Green. "Space charge calculations for semiconductors." Journal of Applied Physics 29.7 (1958): 1034-1040.

[40] Kingston, Robert H., and Siegfried F. Neustadter. "Calculation of the space charge, electric field, and free carrier concentration at the surface of a semiconductor." Journal of Applied Physics 26.6 (1955): 718-720.

[41] Stern, Frank, and W. E. Howard. "Properties of semiconductor surface inversion layers in the electric quantum limit." Physical Review 163.3 (1967): 816.

[42] Stern, Frank. "Self-consistent results for n-type Si inversion layers." Physical Review B 5.12 (1972): 4891.

[43] Tan, I-H., et al. "A self-consistent solution of Schrödinger–Poisson equations using a nonuniform mesh." Journal of applied physics 68.8 (1990): 4071-4076.

[44] Hu, C-Y., et al. "Determining effective dielectric thicknesses of metal-oxide-semiconductor structures in accumulation mode." Applied physics letters 66.13 (1995): 1638-1640.

[45] Moglestue, C. "Self-consistent calculation of electron and hole inversion charges at silicon–silicon dioxide interfaces." Journal of applied physics 59.9 (1986): 3175-3183.

[46] Lee, Chien-Wei, and Jenn-Gwo Hwu. "Quantum-mechanical calculation of carrier distribution in MOS accumulation and strong inversion layers." AIP Advances 3.10 (2013): 102123.

[47] Yang, Nian, et al. "Modeling study of ultrathin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices." IEEE Transactions on Electron Devices 46.7 (1999): 1464-1471.

[48] Vogel, Eric M., Curt A. Richter, and Brian G. Rennex. "A capacitance–voltage model for polysilicon-gated MOS devices including substrate quantization effects based on modification of the total semiconductor charge." Solid-State Electronics 47.9 (2003): 1589-1596.

[49] Moreau, Mathieu, et al. "Investigation of capacitance–voltage characteristics in Ge/high-κ MOS devices." Journal of Non-Crystalline Solids 355.18 (2009): 1171-1175.

[50] Johnson, N. M., D. J. Bartelink, and M. Schulz. "Transient capacitance measurements of electronic states at the SiO 2-Si interface." Proc. Int. Topical Conf. Physics of SiO and Its Interface. 1978.

[51] Lang, D. V. "Space-charge spectroscopy in semiconductors." Thermally Stimulated Relaxation in Solids. Springer Berlin Heidelberg, 1979. 93-133.

[52] Mudanai, S., et al. "Interfacial defect states in HfO/sub 2/and ZrO/sub 2/nMOS capacitors." IEEE Electron Device Letters 23.12 (2002): 728-730.

[53] Sarwar, ATM Golam, et al. "Effects of interface traps and oxide traps on gate capacitance of MOS devices with ultrathin (EOT~ 1 nm) high-κ stacked gate dielectrics." TENCON 2009-2009 IEEE Region 10 Conference. IEEE, 2009

[54] Ouisse, T., et al. "Low-frequency, high-temperature conductance and capacitance measurements on metal-oxide-silicon carbide capacitors." Journal of applied physics 75.1 (1994): 604-607.

[55] Palestri, P., et al. "Comparison of modeling approaches for the capacitance–voltage and current–voltage characteristics of advanced gate stacks." IEEE Transactions on Electron Devices 54.1 (2007): 106-114.

[56] King, Ya-Chin, et al. "DC electrical oxide thickness model for quantization of the inversion layer in MOSFETs." Semiconductor science and technology 13.8 (1998): 963.

[57] Lyons, J. L., et al. "First-principles characterization of native-defect-related optical transitions in ZnO." Journal of Applied Physics 122.3 (2017): 035704.

[58] Djurišić, Aleksandra B., et al. "ZnO nanostructures: growth, properties and applications." Journal of Materials Chemistry 22.14 (2012): 6526-6535.

[59] McCluskey, M. D., and S. J. Jokela. "Defects in zno." Journal of Applied Physics 106.7 (2009): 10.

[60] Lee, Seungjun, et al. "The effect of oxygen remote plasma treatment on ZnO TFTs fabricated by atomic layer deposition." physica status solidi (a) 207.8 (2010): 1845-1849.

[61] Tsiarapas, C., D. Girginoudi, and N. Georgoulas. "Effect of hydrogen on ZnO films and Au/ZnO schottky contacts." Semiconductor Science and Technology 29.4 (2014): 045012.

[62] Theys, Bertrand, et al. "Effects of intentionally introduced hydrogen on the electrical properties of ZnO layers grown by metalorganic chemical vapor deposition." Journal of applied physics 91.6 (2002): 3922-3924.

[63] Ip, K., et al. "Hydrogen incorporation and diffusivity in plasma-exposed bulk ZnO." Applied physics letters 82.3 (2003): 385-387.

[64] Ohashi, Naoki, et al. "Passivation of active recombination centers in ZnO by hydrogen doping." Journal of applied physics 93.10 (2003): 6386-6392.

[65] Ma, Alex M., et al. "Interfacial Contact Effects in Top Gated Zinc Oxide Thin Film Transistors Grown by Atomic Layer Deposition." IEEE Transactions on Electron Devices 63.9 (2016): 3540-3546.

[66] Kim, Han-Ki, et al. "Thermally stable and low resistance Ru ohmic contacts to n-ZnO." Japanese journal of applied physics 41.5B (2002): L546.

CHAPTER 5

[67] Colinge, J. Conduction mechanisms in thin-film accumulation-mode SOI p-channel MOSFETs. IEEE Trans. Electron Devices 37, 718-723 (1990).

[68] Flandre, D. Problems in designing thin-film accumulation-mode p-channel SOI MOSFETs for CMOS digital circuit environment. IEEE Electronics Lett. 27, 1280-1282 (1991).

[69] Steele, G.A., Gotz, G. and Kouwenhoven, L.P. Tunable few-electron double quantum dots and Klein tunnelling in ultraclean carbon nanotubes. Nature Nanotech. 4, 363-367 (2009).

[70] Hofstein, S. R. An analysis of deep depletion thin-film MOS transistors. IEEE Trans. Electron Devices 13, 846-855 (1966).

[71] Pierret, R.F. Semiconductor device fundamentals. (1996).

[72] Kroemer, H. Heterostructure bipolar transistors and integrated circuits. IEEE Proceedings 70, 13-25 (1982).

[73] Ashizawa, Y., et al. Influence of lattice misfit on heterojunction bipolar transistors with lattice-mismatched InGaAs bases. Journal of Appl. Phys. 64, 4065-4074 (1988).

[74] Ohyama, H., et al. Degradation of Si 1-x Ge x epitaxial heterojunction bipolar transistors by 1-MeV fast neutrons. IEEE Trans. Nuclear Science 42, 1550-1557 (1995).

[75] Tada, K., Harada, H., and Yoshino, K.. Polymeric bipolar thin-film transistor utilizing conducting polymer containing electron transport dye. Japanese Journal of Appl. Phys. 35, L944 (1996).

[76] J.M. Shannon, E.G. Gerstner, IEEE Electron Device Lett., 2003, 24(6), 405-407.

[77] R.A. Sporea, M.J. Trainor, N.D. Young, J.M. Shannon, S.R.P. Silva, Scientific reports, 2014, 4.

[78] A.M. Ma, M. Gupta, A. Afshar, G. Shoute, Y.Y. Tsui, K.C. Cadien, D.W. Barlage,. Appl.Phys. Lett., 2013, 103, 253503.

[79] Simmons, J. G., & Taylor, G. W. (1986). Concepts of gain at an oxide-semiconductor interface and their application to the TETRAN—A tunnel emitter transistor—And to the MIS switching device. Solid-state electronics, 29(3), 287-303.

[80] Taylor, G. W., Lebby, M. S., Izabelle, A., Tell, B., Brown-Goebeler, K., Chang, T. Y., & Simmons, J. G. (1988). Demonstration of a p-channel GaAs/AlGaAs BICFET. Electron Device Letters, IEEE, 9(2), 84-86.

[81] Zhu W.J., et al. Current transport in metal/hafnium oxide/silicon structure. IEEE Electron Dev. Lett 23, 97-99 (2002).

[82] Vexler, M. I., et al. Determination of the hole effective mass in thin silicon dioxide film by means of an analysis of characteristics of a MOS tunnel emitter transistor. Journal of Phys. Cond. Mat. 17, 8057 (2005).

[83] Inzelt, G.. Conducting polymers. (2008)

[84] Barlage, Douglas W., et al. "Inversion MOS capacitance extraction for high-leakage dielectrics using a transmission line equivalent circuit." *IEEE Electron Device Letters* 21.9 (2000): 454-456.

[85] Shewchun, J., & Clarke, R. A. (1973). The surface oxide transistor (SOT). Solid-State Electronics, 16(2), 213-219.

[86] Xu, J., & Shur, M. (1986). A tunneling emitter bipolar transistor. IEEE electron device letters, 7, 416-418.

[87] K.K. Ng, Complete guide to semiconductor devices, J Wiley & Sons, Murray Hill, NJ, USA 2002.

[88] Aderstedt, E., Medugorac, I., & Lundgren, P. (2002). High-gain MOS tunnel emitter transistors. Solid-State Electronics, 46(4), 497-500.

[89] Matsumoto, K., Hayashi, Y., Hashizume, N., Yao, T., & Kato, M. (1986). GaAs inversion-base bipolar transistor (GaAs IBT). IEEE electron device letters, 7, 627.

[90] Lo, S-H., Douglas A. Buchanan, and Yuan Taur. "Modeling and characterization of quantization, polysilicon depletion, and direct tunneling effects in MOSFETs with ultrathin oxides." *IBM Journal of Research and Development* 43.3 (1999): 327-337.

[91] Lo, S-H., et al. "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's." *IEEE Electron Device Letters* 18.5 (1997): 209-211.

[92] Yang, Nian, et al. "Modeling study of ultrathin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices." *IEEE Transactions on Electron Devices* 46.7 (1999): 1464-1471.

[93] Register, Leonard F., Elyse Rosenbaum, and Kevin Yang. "Analytic model for direct tunneling current in polycrystalline silicon-gate metal–oxide–semiconductor devices." *Applied physics letters* 74.3 (1999): 457-459.

[94] Richardson, Owen Willans. "LI. Some applications of the electron theory of matter." *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science* 23.136 (1912): 594-627.

[95] Dahlke, W. E., and S. M. Sze. "Tunneling in metal-oxide-silicon structures." *Solid-State Electronics* 10.8 (1967): 865-873.

[96] Card, H. C., and E. H. Rhoderick. "Studies of tunnel MOS diodes II. Thermal equilibrium considerations." *Journal of Physics D: Applied Physics* 4.10 (1971): 1602.

[97] Doghish, MOHAMED YEHYA, and Fat Duen Ho. "A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices." *IEEE Transactions on Electron Devices* 39.12 (1992): 2771-2780.

[98] Chattopadhyay, P., and A. N. Daw. "On the current transport mechanism in a metal—insulator—semiconductor (MIS) diode." *Solid-state electronics* 29.5 (1986): 555-560.

[99] Tarr, N. Garry, D. L. Pulfrey, and D. S. Camporese. "An analytic model for the MIS tunnel junction." IEEE Transactions on Electron Devices 30.12 (1983): 1760-1770.

[100] Bardeen, John. "Tunnelling from a many-particle point of view." *Physical Review Letters* 6.2 (1961): 57.

[101] Schenk, Andreas, and Gernot Heiser. "Modeling and simulation of tunneling through ultra-thin gate dielectrics." *Journal of applied physics* 81.12 (1997): 7900-7908.

[102] Jiménez-Molinos, F., et al. "Physical model for trap-assisted inelastic tunneling in metal-oxide-semiconductor structures." *Journal of Applied Physics* 90.7 (2001): 3396-3404.

[103] Ando, Y., and Tomohiro I. Calculation of transmission tunneling current across arbitrary potential barriers. Journal of Appl. Phys. 61, 1497-1502 (1987).

[104] Ko, David Yuk Kei, and J. C. Inkson. "Matrix method for tunneling in heterostructures: Resonant tunneling in multilayer systems." *Physical Review B* 38.14 (1988): 9945.

[105] Jonsson, Björn, and Sverre T. Eng. "Solving the Schrodinger equation in arbitrary quantum-well potential profiles using the transfer matrix method." *IEEE journal of quantum electronics* 26.11 (1990): 2025-2035.

[106] Chen, Q., et al. Band offsets of HfO 2/ZnO interface: In situ x-ray photoelectron spectroscopy measurement and ab initio calculation. Appl. Phys. Lett. 95, 162104-162104 (2009).

[107] Doyle, B. and Barlage, D., *et al.* Transistor Elements for 30nm Physical Gate Lengths and Beyond. *Intel Tech. Jour.* 6, (2002).

[108] Zhu, W. J., et al. "Current transport in metal/hafnium oxide/silicon structure." *IEEE Electron Device Letters* 23.2 (2002): 97-99.

[109] Yeo, Yee-Chia, Tsu-Jae King, and Chenming Hu. "Direct tunneling leakage current and scalability of alternative gate dielectrics." *Applied Physics Letters* 81.11 (2002): 2091-2093.

[110] Hou, Y. T., et al. "Modeling of tunneling currents through HfO 2 and (HfO 2) x (Al 2 O 3)/sub 1-x/gate stacks." *IEEE Electron Device Letters* 24.2 (2003): 96-98.

[111] Monaghan, S., et al. "Determination of electron effective mass and electron affinity in HfO 2 using MOS and MOSFET structures." *Solid-State Electronics* 53.4 (2009): 438-444.

[112] Mudanai, S., et al. "Understanding the effects of wave function penetration on the inversion layer capacitance of NMOSFETs." *IEEE Electron Device Letters* 22.3 (2001): 145-147.

[113] Polishchuk, Igor, and Chenming Hu. "Electron wavefunction penetration into gate dielectric and interface scattering-an alternative to surface roughness scattering model." *VLSI Technology, 2001. Digest of Technical Papers. 2001 Symposium on*. IEEE, 2001.

[114] Haque, Anisul, and Mohammad Zahed Kauser. "A comparison of wave-function penetration effects on gate capacitance in deep submicron n-and p-MOSFETs." *IEEE Transactions on Electron Devices* 49.9 (2002): 1580-1587.

[115] Shoute, Gem, et al. "Sustained hole inversion layer in a wide-bandgap metal-oxide semiconductor with enhanced tunnel current." *Nature communications* 7 (2016).

[116] Ebers, J. J., and John L. Moll. "Large-signal behavior of junction transistors." *Proceedings of the IRE* 42.12 (1954): 1761-1772.

APPENDIX

FABRICATION STEPS: MOSCAP AND TJT

Below, the general fabrication steps for the majority of both the MOSCAP and the TJT are described sequentially.

1. Prime p-Si substrate was piranha cleaned. The mobility of the p-type Si substrate was measured at about 250 $cm \cdot V \cdot s^{-2}$. The substrate was then dipped into a HF bath for a total of 10 s to remove any native oxide.
2. PECVD silicon nitride (SiN) was deposited direct on top of the substrate at a temperature of 300 °C for 125 s. The target thickness was 50±5 nm.
3. The SiN was then patterned using HPR 504 positive photoresist (PR) was exposed forbaked for 115 s after spin-coating at 10 s spread at 500 rpm and 50 s spin at 4000 rpm. The patterned SiN was etched using reaction ion etch for 25 s.
4. A 25 nm plasma-enhanced ALD (PEALD) ZnO processed at 200 °C was blanket deposited onto the pattern SiN/p-Si substrate. Because the HPR504 developer, MF-354 was shown to etch ZnO, the PR AZ5214 was used. Here, AZ5214 was not converted into a negative resist by eliminating the second bake and exposure step. The PR was stripped using the MF-319 developer.
5. The ZnO mesa was formed by immersing the wafer into a ferric chloride bath for no greater than 3 s and immediately bathe in water. This was necessary to the rapid etching rate of ferric chloride with ZnO.
6. In order to prepare the substrate for dielectric lift-off the following HfO_2, AZ5214 was converted into negative resist and patterned. PEALD HfO_2 was deposited at temperature of 100 °C and a lifted off by sonication.

7. The final metalization layer was deposited using magnetron sputtering using 50 nm of Al and 5 nm Au. The 5 nm of Au was used as a capping layer to prevent oxidization of Al. The metal was also patterned via lift-off.