University of Alberta

A New Hybrid Current Controller for Single-phase Rectifier and DSP Implementation

By

Hao Zhang 

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List of Abbreviations

ADC	Analog-to-Digital Converter
ADCCLOCK	ADC clock rate
ADCCTRL	ADC control register
ADCSTATE	ADC status register
AGND	Analog ground
AH	Switching leg A high-side drive signal
AL	Switching leg A low-side drive signal
AUXSYNC	Auxiliary PWM synchronization signal
AUXPWM	Auxiliary PWM signals
BH	Switching leg B high-side drive signal
BL	Switching leg B low-side drive signal
CAN	Controller area network
CCLK	DSP core clock
CH	Switching leg C high-side drive signal
CL	Switching leg C low-side drive signal
DAC	Digital-to-analog converter
DGND	Digital ground
DM	Data memory
DMA	Data memory address
DSP	Digital Signal Process
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FPF	Fundamental power factor
HCLK	Peripheral clock
IGBT	Insulated Gate Bipolar Transistor
MIPS	Million instructions per second
MODSEL	ADC operating mode select
MOSFET	Metal-oxide semiconductor field-effect transistor
MSPS	Million samples per second
PF	Power factor
PLL	Phase locked loop
PM	Program memory
PMA	Program memory address
p.u.	Per unit
PWM	Pulse width Modulation
PWMCHA	PWM duty cycle control register
PWMCHB	PWM duty cycle control register
PWMCHC	PWM duty cycle control register
PWMCTRL	PWM control register
PWMDT	PWM dead time register
PWMSEG	PWM segment register
PWMSTAT	PWM status register

Chapter 1 Introduction

Single-phase and three-phase full-bridge switch-mode rectifiers are widely used to interface power electronics equipment with the utility grid to prevent supply voltage disturbances. Often the harmonic currents and the electromagnetic interference produced by power electronics equipment are major causes of concern because of their undesirable effects on other loads connected to the utility grid. Controlled-current PWM rectifiers, see Figure 1.1, generate a voltage PWM waveform by turning on or off the rectifier switches to control the current flowing through the supply inductance. These rectifiers can function as a stand-alone regulated voltage source with fast power reversal capability while feeding near sinusoidal input currents at unity power factor [1]. There are many ways for generating the switching signal for the PWM rectifiers to perform PWM current control. Two methods are introduced in this chapter: variable frequency hysteresis current control and fixed frequency carrier based current control. The new hybrid current controller examined in this thesis combines features from both methods to achieve a zero current error and unipolar PWM waveforms.

1.1 Single-phase PWM controlled IGBT rectifier

The major polluters of power system harmonics are the diode bridge rectifiers and phase-controlled thyristor bridge rectifiers [1]. Such converters have the inherent drawbacks that their power factors are low due to both phase angle displacement and the presence of harmonics in the line current [2]. Harmonic currents injected from the power electronics equipment into the ac voltage supply can also cause the supply voltage waveform distortion and other problems such as additional heating, electromagnetic interference and malfunction of other equipments, which

receives power from the same ac supply. In order to maintain a good power quality and to limit the harmonic current injection, single-phase and three-phase boost-type ac/dc PWM controlled converters are also used in industrial applications. In comparison with the diode rectifier, PWM controlled rectifiers are more expensive but can realize a unity input power factor, decrease the harmonic current injected from the power electronics equipment and permit bi-directional power flow. The basic scheme of a single-phase PWM controlled IGBT rectifier is shown in Figure 1.1.

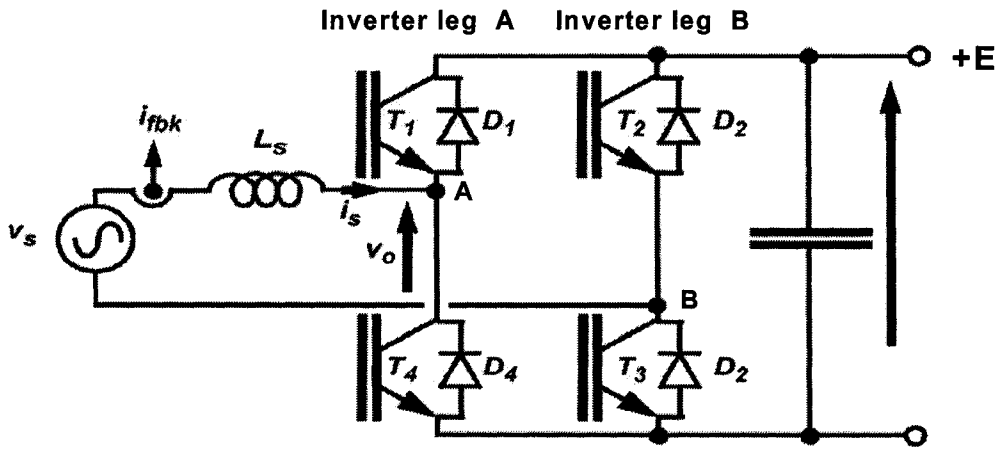


Figure 1.1 Single-phase PWM controlled IGBT rectifier

The supply current can be expressed in terms of its fundamental frequency component i_{s1} plus other harmonic components. If v_s is assumed to be purely sinusoidal, then only i_{s1} contribute to the average power flow. This is because the frequencies of the supply voltage and current must be the same to produce an average power flow. Power factor is used to measure how effectively the equipment draws the power from the ac supply and can be calculated by using the following formula (1.1). When the harmonic current i_h increases, the power factor will decrease. At a given voltage and power level, as the power factor decreases, the current drawn by the equipment will increase and may cause an overload of the power supply equipment.

$$PF = \frac{I_1}{\sqrt{I_1^2 + I_h^2}} FPF \qquad (1.1)$$

In formula (1.1), $FPF = \frac{I_{1r}}{I_1}$ and I_1 represents the rms value of fundamental harmonic current. $I_1 = \sqrt{I_{1r}^2 + I_{1i}^2}$. I_{1i} is the fundamental imaginary current, which is caused by the phase shift between the input voltage V_S and I_1. If I_1 can be controlled to be in the same phase as V_S, I_{1i} can be eliminated. Hence, the power quality can be improved by reducing the imaginary fundamental current and other harmonics. The main task of the new current controller is to try to shape the input current waveform to be sinusoidal and to achieve unity power factor by minimizing both I_{1i} and I_h.

1.1.1 Bipolar PWM switching pattern

The single-phase PWM controlled full-bridge rectifier consists of two inverter switch legs, A and B, see Figure 1.1. Each leg consists of one pair of switches (which can be MOSFET or IGBT) and every switch has a free-wheel diode. This kind of structure allows the full-bridge converter to operate in all four quadrants of the i_s-v_s plane and to permit bi-directional power flow. The magnitudes of the DC output voltage are also controllable. The two switches in each leg are never on simultaneously to prevent potentially destructive short-circuits. That means that when one switch is on, the other switch in the same leg must be off. When the on-state of the switch changes both switches must be off for a short time (dead time or blanking time). By switching the appropriate pair of switches, using a PWM controller, the input-current waveform is controlled to keep close to a sinusoidal template whose phase and magnitude can be set as desired [3]. An inductor L_s is included in the circuit to help reduce the ripple in i_s. The capacitor

C is used to help smooth the DC-link voltage.

The full-bridge PWM controlled rectifier has the capability to operate in all four quadrants, and the IGBT switches can be pulse-width modulated using two kinds of PWM switching strategies: PWM with bipolar voltage switching and PWM with unipolar voltage switching. Before starting to discuss the details of these switching schemes some fundamental definitions are reviewed first.

The amplitude modulation ratio m_a, shown in Figure 1.2, is defined as

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{1.2}$$

Where the $\hat{V}_{control}$ is the peak amplitude of the sinusoidal fundamental harmonic control signal and the $\hat{V}_{tri}$ is the peak amplitude of triangular carrier signal. m_a determines the peak amplitude of the rectifier input voltage at fundamental harmonic frequency. When $m_a \leq 1.0$, the controller operation is called linear modulation, which means that the magnitude of the voltage at fundamental harmonic frequency varies linearly with the amplitude modulation ratio m_a. When $m_a > 1.0$, the PWM rectifiers work in over-modulation mode. In this operation mode the magnitude of the voltage at fundamental harmonic frequency does not increase proportionally with m_a. As the harmonics are increased in this mode, normally m_a is controlled to operate in the linear modulation range from 0 to 1. In the DSP control system, the PWM duty cycle can be achieved by numerically calculating the m_a.

The order h of the harmonic voltages in the PWM waveform are normally odd harmonics and are also present in the current waveform, see formula (1.3). Even harmonics are normally not produced

$$h = \frac{f_h}{f_1} \tag{1.3}$$

In bipolar switching mode, the switching signals are generated by comparing the control voltage $\hat{V}_{control}$ with a triangular waveform whose frequency determines the device switching frequency. The switches (T_{A+}, T_{B-}) and (T_{A-}, T_{B+}), see Figure 1.1, are treated as two switch pairs and the switches in the same pair are turned on and off simultaneously. The detailed control logic waveforms are shown in Figure 1.2.

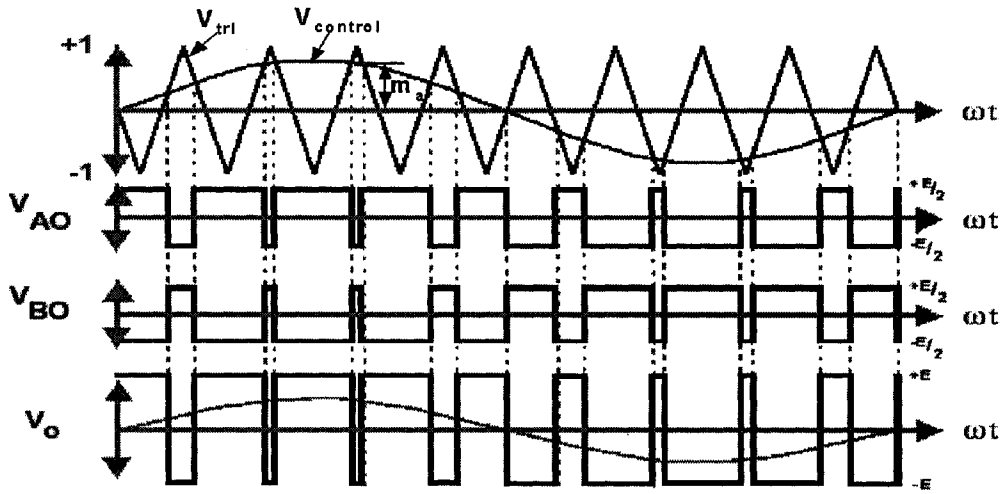


Figure 1.2 PWM with bipolar voltage switching

When $\hat{V}_{control} > \hat{V}_{tri}$, T_{A+}, T_{B-} are turned on.

When $\hat{V}_{control} < \hat{V}_{tri}$, T_{A-}, T_{B+} are turned on.

In theory the input and output voltages of the boost type converters have following relation:

$$E \geq \sqrt{2} \times V_s \tag{1.4}$$

The duty cycle D_1 and D_2 of V_{AO} and V_{BO} of bipolar voltage switching are defined:

$$D_1 = \frac{t_{ON}}{T_s} \tag{1.5}$$

$$D_2 = 1 - D_1 \tag{1.6}$$

t_{ON} is the on-time of the switch pair (T_{A+}, T_{B-}).

The voltage of V_{AO} and V_{BO} depend on the voltage E and duty cycles D_1 and D_2:

$$V_{AO} = E \times D_1 \tag{1.7}$$

$$V_{BO} = E \times D_2 = E \times (1 - D_1) \tag{1.8}$$

$$V_O = V_{AO} - V_{BO} = (2D_1 - 1)E \tag{1.9}$$

The rectifier input voltage V_o jumps between +E and –E and duty cycle can vary between 0 and 1, depending on the magnitude and polarity of $V_{control}$. This means that the average voltage can be varied in a range from +E to –E.

1.1.2 Unipolar PWM switching pattern

In unipolar switching mode, the switching signals are generated by comparing the control voltage $\hat{V}_{control}$ and $-\hat{V}_{control}$ with a triangular waveform whose frequency is the same as the inverter bridge switching frequency. The switches in each leg are controlled independently of the other leg. The detailed control logic is as follows and the waveforms are shown in Figure 1.3:

When $\hat{V}_{control} > \hat{V}_{tri}$, T_{A+}, is turned on.

When $-\hat{V}_{control} > \hat{V}_{tri}$, T_{B+} are turned on.

The formulas (1.5-1.9) are also valid in unipolar voltage switching. At the same switching frequency, when compared with bipolar voltage switching mode, unipolar voltage switching mode has higher frequency harmonics with lower voltage harmonic magnitudes. This

is because unipolar switching generates PWM voltage waveforms with a higher switching frequency, (ie. Doubled), and lower rms values. Hence the load current ripple is reduced. The proposed hybrid current controller being examined uses the unipolar voltage switching scheme to perform the intended current control.

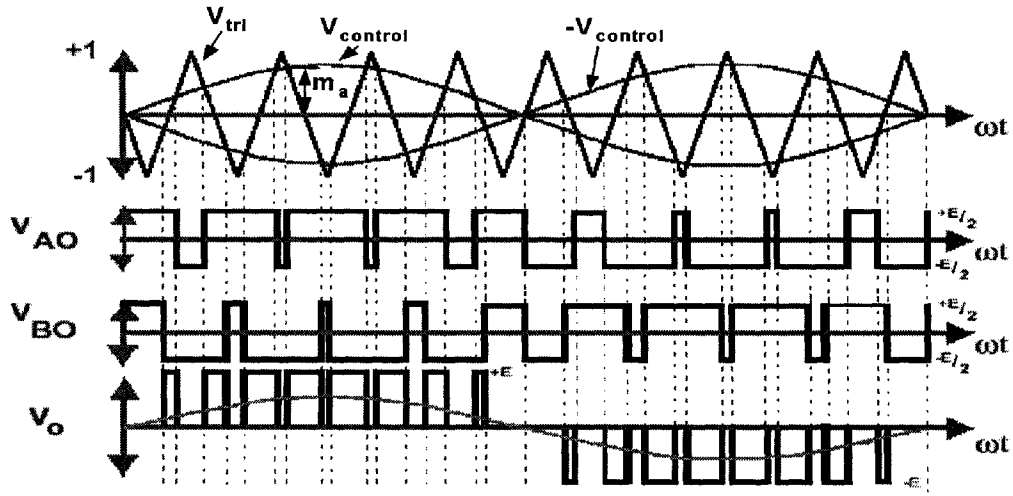


Figure 1.3 PWM with unipolar voltage switching

1.1.3 PWM current control

Most applications of voltage-source pulse-width modulated converters have a control structure comprising of an internal current feedback loop, e.g. ac motor drives, active filters, high power factor ac/dc converters, uninterruptible power supply systems and ac power supplies. Consequently the performance of the converter system largely depends on the quality of the applied current control strategy [4]. The current-controlled PWM converters have many desired advantages such as fast current control dynamics, peak current limitation with an intrinsic short-circuit protection.

A number of control techniques have been developed and widely used in many industrial applications to control the rectifier input current. The most common and basic control strategies to generate the switching signals are variable frequency hysteresis current control and fixed-frequency carrier-based current control. The proposed hybrid current controller for a single-phase PWM rectifier combines both methods to achieve a zero current error and unipolar PWM waveforms. The fundamentals of these concepts are now described.

1.2 Hysteresis current control

Hysteresis current control can also be referred to as "tolerance band current control" and is the basic control method used to control the input current [5]. The switching signals are derived from the comparison of the actual input current error with a fixed hystersis band. The center of the hysteresis band is the reference current and the magnitude of the hysteresis band is determined by the controller. One switch leg of the single-phase PWM rectifier (T_{A+} and T_{A-}) is used to illustrate how the hysteresis current control works in Figure 1.4. The switching frequency depends on the speed of the current changed between the upper limit and lower limit. When the current error tries to overpass the lower limit, the switch T_{A-} is turned on, and when the current error tries to overpass the upper limit, the switch T_{A+} is turned on.

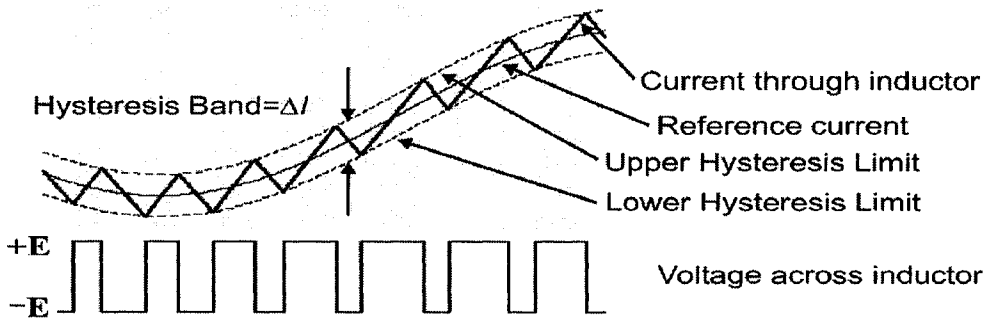


Figure 1.4 Fixed current ripple current control

There are two switching patterns in single-phase PWM rectifier hysteresis current control: "unipolar hysteresis control" and "bipolar hysteresis control". Figure 1.5 shows the unipolar hysteresis control scheme. The two rectifier inverter legs are controlled independently by comparing the current error with two hysteresis bands. Figure 1.6 shows the waveforms of simulated input current, reference current error with hysteresis band and switching signals.

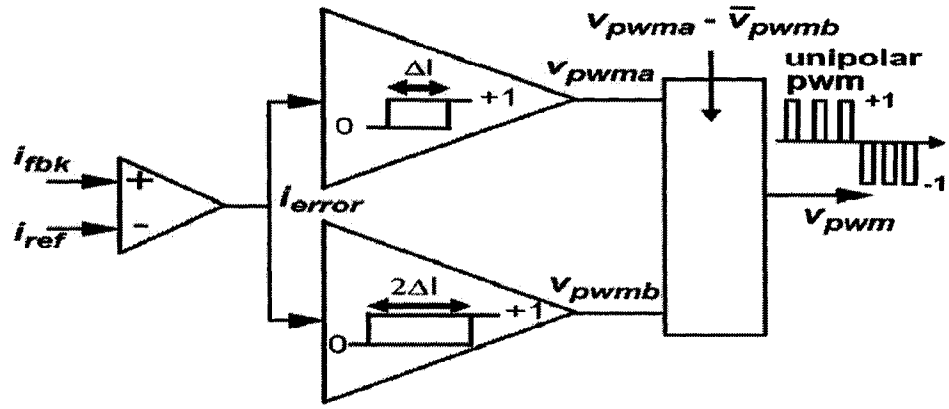


Figure 1.5 Unipolar hysteresis current control

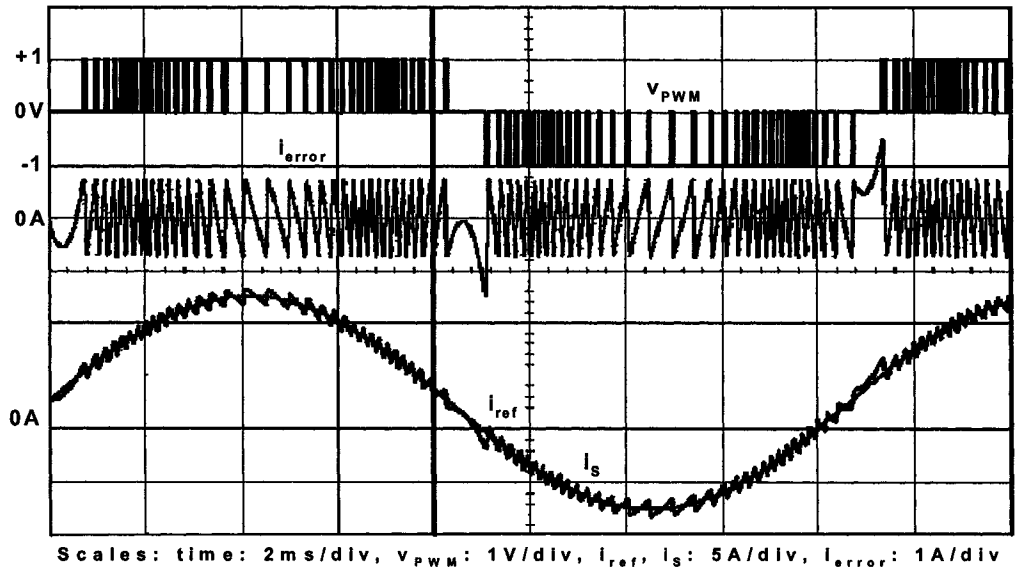


Figure 1.6 Unipolar hysteresis current control waveform

In bipolar voltage switching mode, T_{B-} has the same switching pattern as T_{A+} and the T_{B+} has the same switching pattern as T_{A-}. In unipolar voltage switching mode, the reference voltage used to generate PWM signals for leg B is the same one as leg A's, but two carrier signals are used to control leg A and leg B. The two carrier signals have an 180° phase shift.

The advantages of a hysteresis current controller are: simple implementation, fast current dynamics, excellent current wave-shaping ability, stable control, inherent peak-current limiting capability and close to zero average current error.

The main drawback of hysteresis current control is its variable switching frequency. The variable switching frequency produces a wide frequency spectrum, generates uneven and random switching patterns and sometimes can cause excessive stress on the rectifier switching devices. In hysteresis current control, the current error signal is essentially centered on the sinusoidal reference signal and the hysteresis band is fixed. The proposed new PWM control scheme combines the hysteresis and carrier-based current control scheme to achieve a zero centered current error signal where the switching frequency is fixed by a saw-tooth carrier waveform and the hysteresis band is allowed to change naturally.

1.3 Carrier-based current control

Carrier-based current control is also widely used for pulse-width modulation. In a single-phase or three-phase inverter, the PWM control switching signals can be derived from the comparison of the desired sinusoidal reference current amplitude depth m_a with a fixed-frequency triangular waveform to shape the input current to be sinusoidal. In single-phase or three-phase rectifier, the PWM control switching signals can be derived from the comparison of the current error signal $k_1 * i_{error}$ with a fixed-frequency saw tooth to shape the input current to follow its reference. Since in each triangular cycle, the relative switches are only turned on or off

once, the PWM switching frequency is the same as the triangular frequency and is fixed, conversely, this operation is associated with a variable peak-peak current ripple.

The Figure 1.6 shows a block diagram of the carrier based unipolar PWM controller and Figure 1.7 shows the relevant waveform.

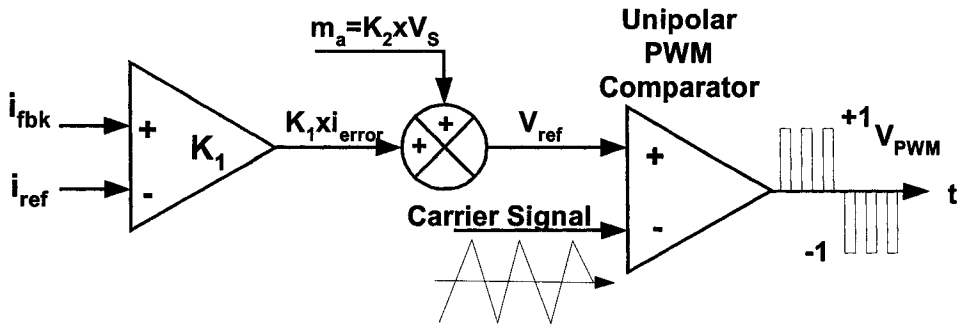


Figure 1.6 Control scheme of Carrier based unipolar PWM control

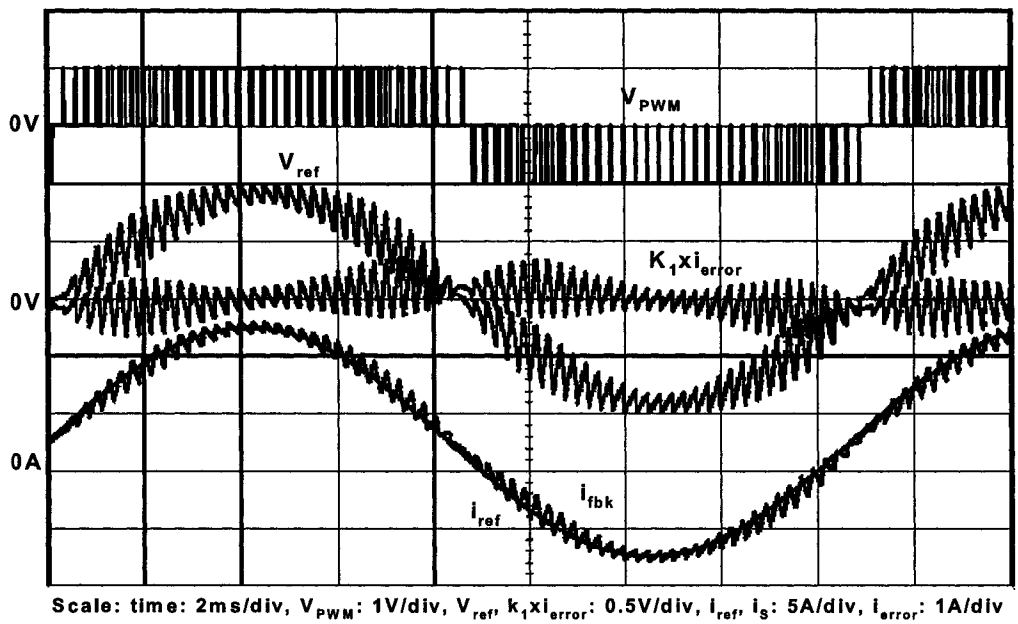


Figure 1.7 Waveform of carrier-based unipolar current control

The advantages of carrier-based current controllers scheme are their fixed switching frequency, simple implementation and low harmonics. By combining the excellent current-

shaping ability of hysteresis current control with the constant switching frequency of the carrier-based current control, the new control scheme for fixed frequency hysteresis current control has been developed to achieve zero current error.

1.4 Summary

The fundamental characteristic of PWM current control techniques in single-phase PWM rectifier have been reviewed. This thesis examines several fixed switching frequency PWM controllers using a signal integrator to demonstrate how the proposed new current controller operates and to compare the advantage and disadvantages of the various current controllers (See chapter 2).

Detail descriptions of the new current control techniques are given, see chapter 3. In order to demonstrate the experimental operation of the new current controller, a DSP test system is used that includes a DSP controller; an IGBT rectifier and a relative signal sampling and a isolation circuit (see chapter 5). An overview of the ADSP-21992 mixed signal DSP controller is given to help to understand how the DSP controller works (see chapter 4).

Experimental tests are undertaken on an IGBT rectifier using a 5mH supply inductance and a 60Hz supply with voltage range from 60 to 120V and the currents varying from 3 to 10A. The software development and experimental results are also given (see chapter 6).

1.5 Thesis contribution

In this thesis the development process of new current controller and DSP experimental implementation were described and the contributions of this thesis are list below.

- The new current controller shapes the input current by comparing the current error with modulated carrier signals m_a. The new control scheme has many advantages such as fixed frequency, close to zero current error per PWM cycle, easy implementation and no current phase shift.
- ADSP-21992 DSP controller is used to implement the current control scheme in real time.
- A signal sampling circuit and a signal isolation circuit are designed and tested to connect the DSP board with power electronics board.
- Experimental results obtained from the test verified the operation of the new control scheme.

Chapter 2 Survey of PWM Current-Control Techniques

The current controlled PWM rectifier is characterized as being a highly accurate and instantaneous current waveform controller, excellent peak current limiter, overload rejection with fast current dynamics. Many PWM current control methods have been developed to try to force a sinusoidal input current and to avoid the generation of additional harmonics. The performance of the PWM controlled converter system largely depends on the quality of the applied current controller strategy [4]. The application of digital signal processors (DSP) and high-performance processors can also bring significant improvement in the system design to ensure satisfactory performance, and to boost the reliability of designs and shortened the design cycle. This chapter describes various digital current control methods such as the digital deadbeat current control, predicted current control and zero average current error control. These controllers are used to place the proposed current controller into perspective.

2.1 General description

AC/DC converters are widely used in industrial application to supply the DC voltage. As the diode bridge rectifiers and phase-controlled thyristor bridge rectifiers can seriously pollute the power system, cause harmful electromagnetic interference to neighborhood appliance and overheat the power transformer. Many current control techniques have been developed for single-phase or three-phase rectifiers or active filters to force the ac input current to follow the sinusoidal waveform to improve the power quality and achieve the unity power factor. The basic

current control techniques can be classified into two kinds: one is the variable frequency current control and another one is fixed-frequency control. The control scheme can be implemented by using analog control circuit or digital control circuit. In practice, the analog control techniques, such as the linear current control, have faster response than digital control technique. But the fast development of digital signal processors (DSP) and high-performance processors has allowed the high-level program language application in power electronics control and the new software design methodologies and test procedures have significantly improved the system design to ensure satisfactory performance, boosted the reliability of designs and shortened the design cycle. Recently, most current control techniques for AC/DC power conversion are developed based on digital control to achieve the optimum current control that can accurately recreate the current reference waveform without causing the generation of additional harmonics [6].

The basic current control is hysteresis current control. It has many ideal current control features such as fast current dynamics, excellent current wave-shaping ability and inherent peak-current limiting capability. But it also has disadvantages: the main one is that it produces a varying modulation frequency for the power converters. This is responsible for various problems, from the difficulty in designing the input filters to the generation of unwanted resonance on the utility grid. These have limited the application of hysteresis current control especially in applications requiring co-ordination of switching between multi-PWM modules such as three-phase rectifiers. Many new control strategies were developed to keep the high dynamic features of hysteresis current control but operate at a fixed switching frequency [7]-[15]. So the first and the main design goal for the current controller was to combine the excellent current wave-shaping characteristics of hysteresis based controllers with the benefits associated with fixed switching frequency carrier based controller.

The second design goal for the current controller was to obtain a fixed PWM switching frequency that has an inherent variable current ripple, but that also achieves a zero average current error over a PWM switching cycle.

Several current control techniques are described in this chapter, such as fixed frequency delta-modulated hysteresis current control, predicted switching time current control [7]-[11], digital simulated integrator current control [12] [13] and adaptive hysteresis band current control [14][15]. These controllers are examined to see how these techniques meet the above mentioned design goals. The results are used to illustrate what kind of technique the new hybrid current controller developed uses, see chapter 3, and to demonstrate the advantages of the new current controller.

2.2 Fixed Frequency delta-modulated hysteresis PWM controller

This is a general PWM signal generator that creates unipolar PWM controller that using hysteresis comparator with a signal integrator, see Figure 2.1. This modulation is examined here as it mimics the structure of a hysteresis current controlled PWM rectifier. The signal waveforms produced can be analyzed to identify the relationship between the amplitude modulation depth m_a of the PWM waveform V_{PWM}, the hysteresis magnitude h and the integration constant R. The single-phase delta-modulated hysteresis current control scheme is shown in Figure 2.1.

The feedback of a unipolar PWM hysteresis comparator output signal V_{PWM} to a signal integrator input can produce a self-oscillating closed-loop system, where the ramping rate of the integrator output signal V_{ref} changes with the polarity of V_{PWM}. The signal V_{ref} can be considered as a delta-modulated signal. m_a is the amplitude modulation depth of the PWM modulator and

determines the average of the PWM output signal over a PWM cycle, $V_{PWM,\,av}$. V_{ref} ramps between the upper and lower bounds of the hysteresis band h. The ramping rate over time of V_{ref} is determined by the integration constant R, the signal m_a and V_{PWM}. The input signal m_a exists in the range ±1, and V_{PWM} has the states 0 and ±1.

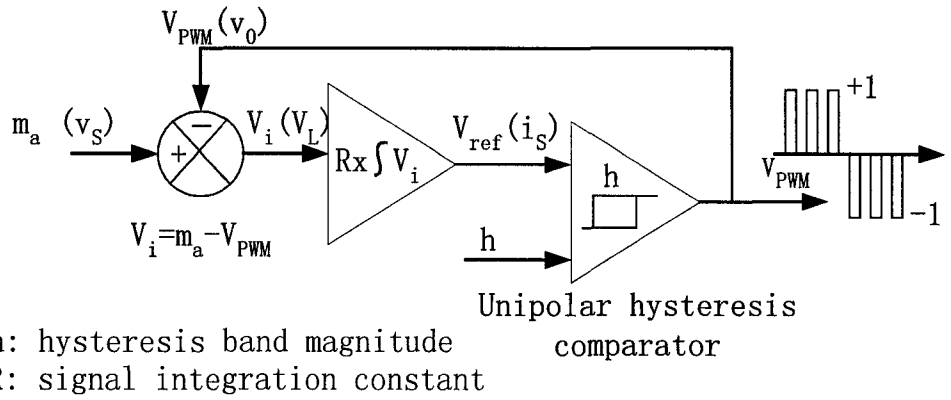


Figure 2.1 Single-phase delta-modulated hysteresis PWM controller

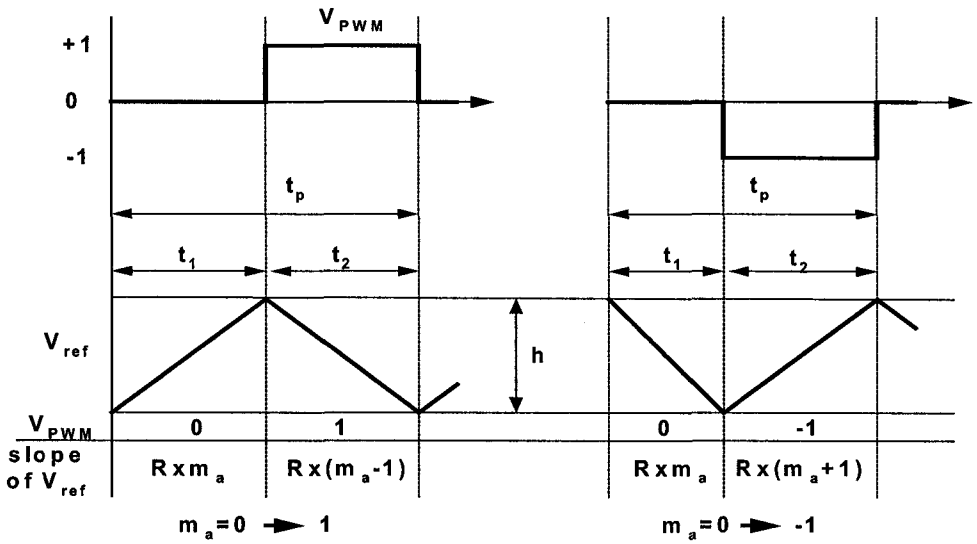


Figure 2.2 Delta Modulated hysteresis PWM controller

The ramping rate of V_{ref} for a positive m_a is given by:

$$t_1 : \frac{dv}{dt}(t_1) = R \times m_a, t_2 : \frac{dv}{dt}(t_2) = R \times (m_a - 1) \tag{2.1}$$

The periods t_1 and t_2 are derived from the above formula:

$$t_1 : t_1 = \frac{h}{R} \times \frac{1}{m_a}, t_2 : t_2 = \frac{h}{R} \times \frac{1}{1 - m_a} \tag{2.2}$$

And

$$t_p = t_1 + t_2 = \frac{h}{R} \times \frac{1}{m_a(1 - m_a)} \tag{2.3}$$

hence for a fixed m_a, the switching frequency f_{sw} of V_{PWM} is:

$$f_{sw} = \frac{R}{h} \times m_a(1 - m_a) \tag{2.4}$$

The average of V_{PWM} is related to m_a in this p.u. system by:

$$v_{PWM,av} = \frac{t_2}{t_p} = \frac{\frac{h}{R} \times \frac{1}{1 - m_a}}{\frac{h}{R} \times \frac{1}{m_a(1 - m_a)}} = m_a \tag{2.5}$$

The formula (2.5) states that the average of V_{PWM} is determined by m_a and is independent of the integration constant R and the hysteresis band magnitude h. The formula (2.4) states that m_a, R and h determine the PWM switching frequency. Since m_a is a sinusoidally varying signal in a PWM rectifier, the resultant PWM waveform v_{pwm} has a variable switching frequency with a wide varying frequency spectrum. This is considered undesirable and hard to filter. As the integration constant is hard to control, in order to fix the switching frequency, the usual control technique is to control the hysteresis band magnitude band h in real-time by linking h to the amplitude modulation depth m_a. Since m_a is directly linked to the resultant $V_{PWM, av}$, h could be determined by sampling V_{PWM} and determining a sampled value of m_a. For instance, putting:

$$h = m_a(1 - m_a) \tag{2.6}$$

and $$f_{sw} = R \qquad (2.7)$$

From formula (2.6) we can see the hysteresis band goes to zero at m_a=0 and has a maximum magnitude of h=0.25 at m_a=0.5. The waveform is shown in Figure 2.3 and the sampled switching frequency is shown in Figure 2.4.

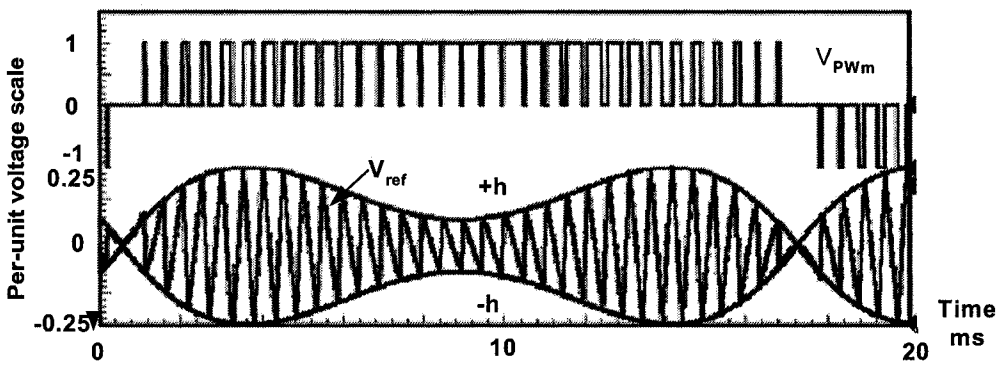


Figure 2.3 Waveform of current error

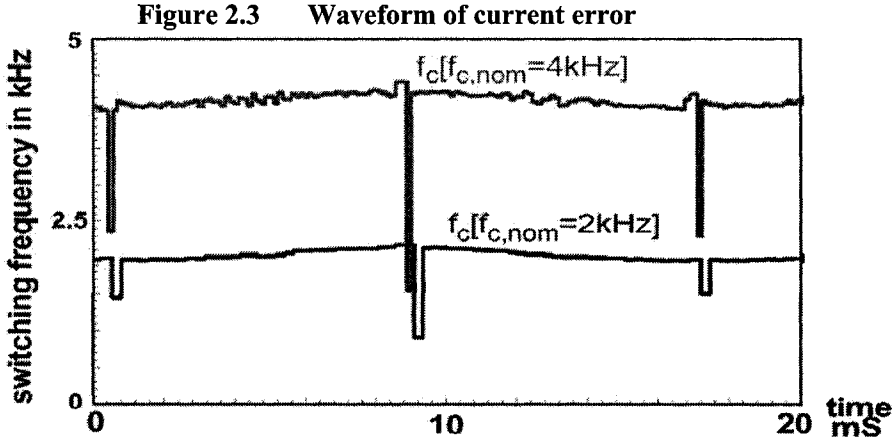


Figure 2.4 Switching frequency for the signal V_{PWM}

A variable hysteresis band can be used to try to fix the switching frequency, but generally a variable switching frequency is still obtained, see Figure 2.4. The advantages include simple calculation for DSP controller because the switching frequency can be controlled to generate the desired hysteresis band h by linking h to the amplitude modulation depth m_a; the average current

error per PWM cycle is centered at zero. All these advantages are attractive and are also features of the new current control technique development illustrated in chapter 3.

2.3 Dead-beat adaptive hysteresis current control

The hysteresis band can be calculated by using the amplitude modulation depth m_a. Another way to obtain the desired hysteresis band is referred to as a dead-beat adaptive hysteresis current control [14].

A hysteresis current controller is characterized by accurate current waveshaping, very fast response and good accuracy. But the variable switching frequency is also undesirable. Many research works have been done to eliminate this drawback. The "dead-beat adaptive hysteresis current controller"is one of the solutions to keep the advantage of hysteresis current control while maintaining a constant switching frequency.

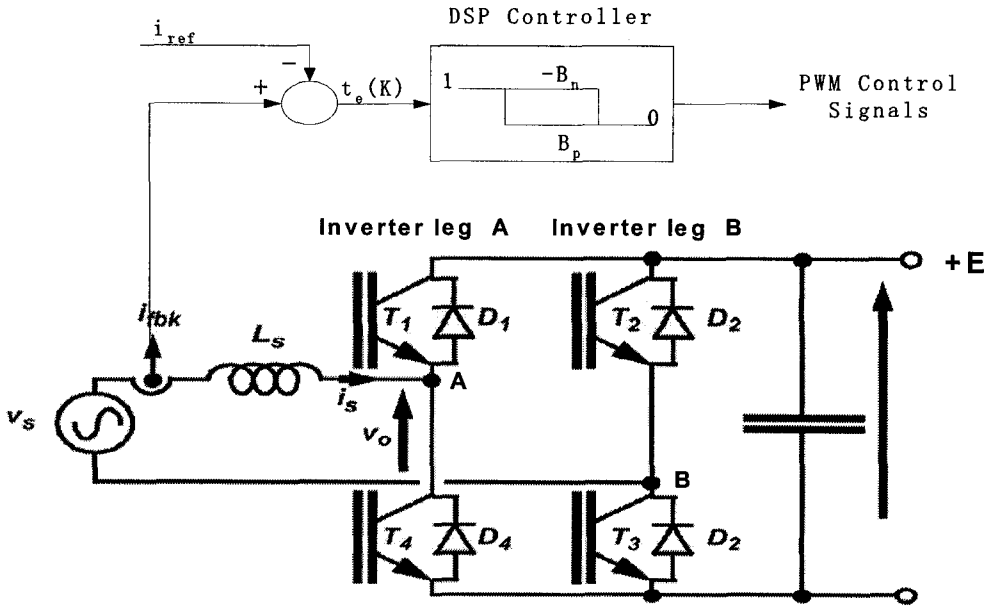


Figure 2.5 Diagram of dead-beat hysteresis current control

The main idea of this control is to change the input current error hysteresis band to keep the switching frequency constant. The block diagram of the dead-beat adaptive hysteresis current control is shown in Figure 2.5. The hardware setup is the same as the new current control scheme illustrated in chapter 3. The only difference is the current control method.

The control algorithm is explained in two steps: first, the ideal operating conditions are assumed, i.e. the converter dead time and signal delays are neglected. And then the operating condition with the converter dead time is added.

By comparing the input current with its reference, the current error is obtained. This current error is compared with the hysteresis bands to generate the switching signals. The stable switching frequency at the desired level can be achieved by adjusting the hysteresis band. The DSP controller performs the calculation for the new hysteresis band. The principle of control scheme is shown in Figure 2.6.

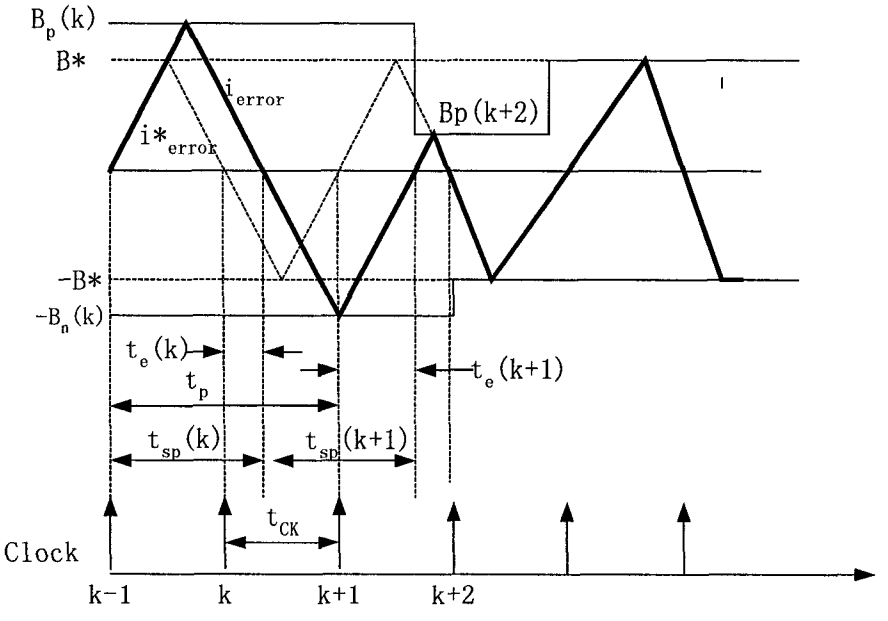


Figure 2.6 Diagram of control scheme

In the fixed switching frequency mode, the slope of the current error should be constant. That's the basic and key idea for dead-beat hysteresis current control. The DSP calculates the new amplitude of the hysteresis band for next cycle to keep the slope of current error constant and update the hysteresis band at current error zero crossing point. The detailed calculation is based on the formulas derived below. In Figure 2.6 the B* and –B* correspond to the desired hysteresis band. The $t_e(k)$ represents the time between the current error zero crossing and the last external synchronization clock pulse. The t_p is the desired modulation period and equal to $2t_{ck}$. From the Figure 2.6 we can get the following relations based on simple geometrical considerations:

$$B^*(k) = \frac{t_p}{2} * \frac{B_p(k)}{t_{sp}(k)} \tag{2.8}$$

and

$$\frac{B_p(k+2)}{B^*(k)} = \frac{\frac{t_p}{2} - t_e(k+1)}{\frac{t_p}{2}} \tag{2.9}$$

From the above formulas, the new amplitude of hysteresis band can be derived:

$$B_p(k+2) = B_p(k) * \frac{t_p - t_e(k) - t_{sp}(k) * \frac{B_n(k)}{B_p(k)}}{t_{sp}(k)} \tag{2.10}$$

All the calculations are based on the measurement or previous calculations. The calculation of opposite hysteresis band $B_n(k+2)$ uses the same technique. The DSP controller updates the upper hysteresis band at the zero crossing point when the current error continuously increase and updates the lower hysteresis band at the zero crossing point when the current error continuously decreases. That means that the DSP controller has the ability to get the correct bandwidth in two control cycles or in one modulation period. These two-cycle delays can permit

the current control to have a better dynamics response. In theory the dead-beat hysteresis current control can achieve the fixed switching frequency and keep the average current error to zero.

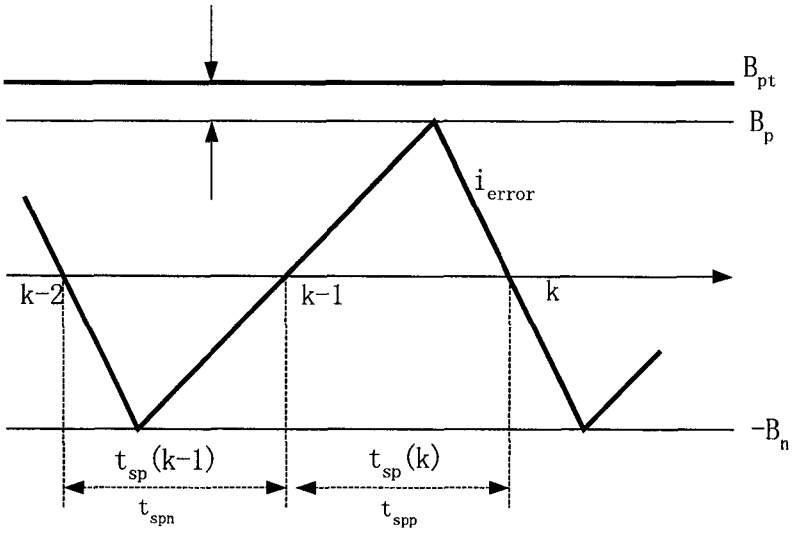


Figure 2.7 Control operation with deadtime

If the dead time is considered, the current control operation is shown in Figure 2.7. The control scheme is kept the same but the calculation becomes complicated. The new formula can be derived as above:

$$B_p(k+2) = [B_p(k) + \Delta B_p(k)] * \frac{t_p - t_e(k) - t_{sp}(k) * \dfrac{B_n(k) + \Delta B_n(k)}{B_p(k) + \Delta B_p(k)}}{t_{sp}(k)} - \Delta B_p(k) \quad (2.11)$$

The magnitude of the hysteresis band needs to be determined by the DSP controller in real time in order to track the changes in the operating conditions of the rectifier and to maintain a constant switching frequency. The current error is shown in Figure 2.3 and the current errors vary between hysteresis band $B_p(k)$ and $B_n(k)$ mentioned.

The main advantages of the "dead-beat adaptive hysteresis current controller" include

fixed switching frequency, zero average current error per PWM cycle and easy hardware implementation. The disadvantages are that the formulas used to calculate the hysteresis band are complicated, and mean that the DSP requires more time for calculation.

2.4 Predictive digital current control

"Predicted current controller" is another kind of fixed switching frequency current control, which combines the superior dynamics of the hysteresis current control and the advantages offered by constant frequency current control. The basic idea of this kind of control strategy is that the voltage required for controlling the line current is predicted first to determine a quasi-optimal switching pattern [2]. The duty cycle of the inverter legs of converter is controlled such that the input current reaches the value set by the reference current template at the end of the switching cycle [3].

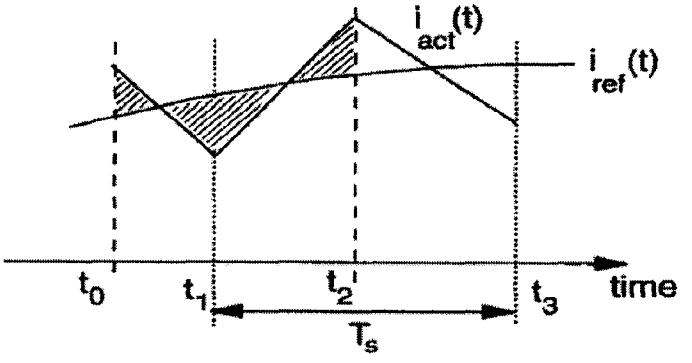


Figure 2.8 Current waveform in simple equal-charge criterion method

The predicted (on-time) equal-charge criterion scheme for constant-frequency control of single-phase boost-type AC/DC converter, shown in Figure 2.8, is one of the predicted current controllers which has the similar hardware setup as the new control scheme developed in chapter

3. The details of it are now presented below.

Figure 2.9 shows a single-phase boost type PWM control rectifier. The PWM controller uses two feedback signals to generate switching signals to force the input current follow the sinusoidal waveform. One of the feedback signals is the power supply voltage and used by the PWM controller generate the desired waveform. The second feedback signal is the current signal. The bipolar switching pattern is used here to explain the principal of predicted (on-time) equal-charge current control. The switch pairs (T_{A+}, T_{B-}) and (T_{A-}, T_{B+}) are turned on or off once in every period T: It making the switching frequency constant.

The DSP controller predicts the switch's turn-on time to make the average input current satisfy the following requirement:

$$\int_{A}^{C} i_{fbk}(t)dt = \int_{A}^{C} i_{ref}(t)dt \qquad (2.12)$$

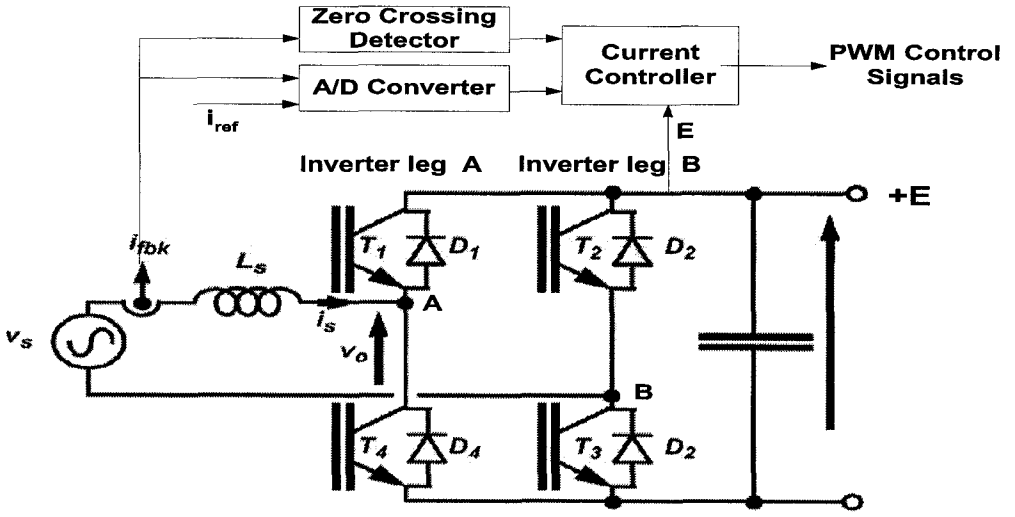


Figure 2.9 Single-phase Current Control PWM Rectifier

The start time of t_A can have two positions named mode A and mode B, the details are shown in Figure 2.10 and Figure 2.11. (Assume the carrier frequency is much higher than

fundamental frequency). With the mode A, during the time t_A-t_B, the switch T_{A-} is on. The voltage across the inductor is equal to:

$$V_{in} + V_{dc} = L\frac{di_{fbk}(t)}{dt} \tag{2.13}$$

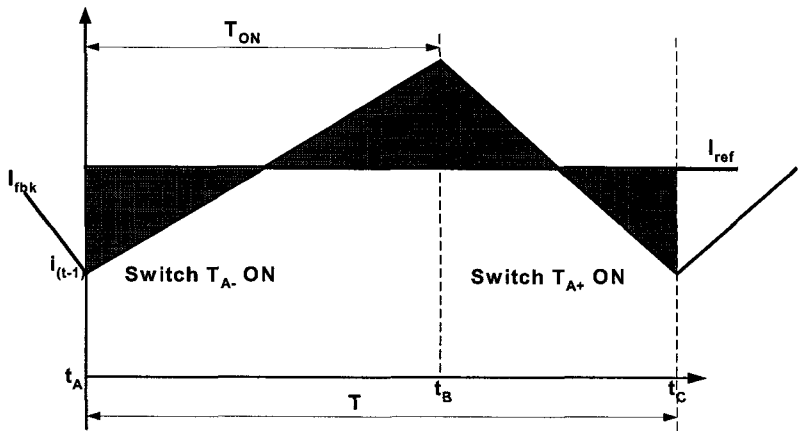


Figure 2.10 Predicted on-time current control mode A

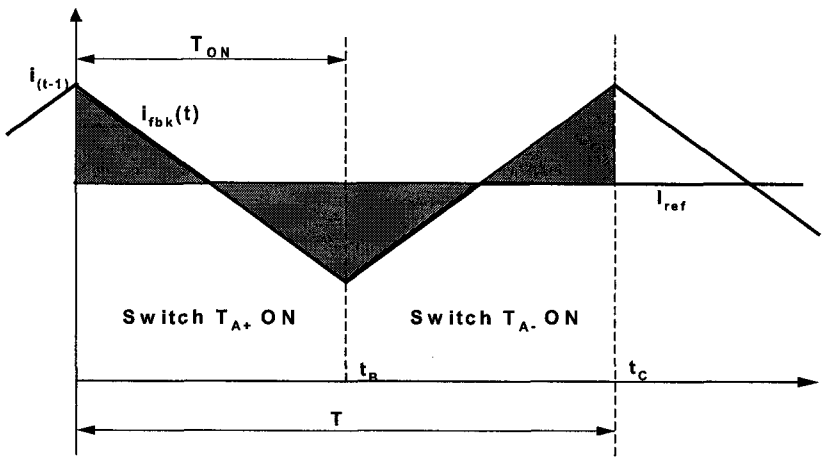


Figure 2.11 Predicted on-time current control mode B

Simplifying and integrating the formula (2.13):

$$i_{fek}(t) = i_{(t-1)} + \frac{V_{in} + V_{dc}}{L}(t - t_A) \tag{2.14}$$

Set the value of $i_{fek}(t)$ at $t=t_B$ is i_t, then i_t will equal to:

$$i_t = i_{(t-1)} + \frac{V_{in} + V_{dc}}{L} T_{ON} \tag{2.15}$$

At time $t=t_B$, the switch T_{A+} is on. The voltage across the inductor is equal to:

$$V_{in} - V_{dc} = L\frac{di_{fek}(t)}{dt} \tag{2.16}$$

Simplifying and integrating the formula (2.16):

$$i_{fek}(t) = i_{(t-1)} + \frac{V_{in} - V_{dc}}{L}(t - t_B) \tag{2.17}$$

Set the value of $i_{fek}(t)$ at $t=t_C$ is $I_{(t+1)}$, then $i_{(t+1)}$ will equal to:

$$i_{(t+1)} = i_t + \frac{V_{in} - V_{dc}}{L}(T - T_{ON}) \tag{2.18}$$

Combines the formulas (2.15) and (2.18) and simplifying:

$$i_{(t+1)} = i_{(t-1)} + \frac{V_{in}}{L}T + \frac{V_{dc}}{L}(2T_{ON} - T) \tag{2.19}$$

As during the time t_A to t_C, the average input current should equal to the reference current, the switch on-time can be solved:

$$aT_{ON}^2 + bT_{ON} + c = 0 \tag{2.20}$$

Where $a = -\frac{V_{dc}}{L}$, $b = \frac{2Vdc}{L}T$ and $c = T(i_{(t-1)} - I_{ref}) + \frac{T^2}{2L}(V_{in} - V_{dc})$.

The switch-on time in Mode B can also be obtained by using a similar approach. As Mode A can not operate stably in the negative half cycle and Mode B can not operate in the positive half cycle [6], the predicted on-time current control scheme combines two modes together, each

mode only works in a half cycle to keep the system stable. At each cycle, the DSP controller uses the above formulas to predict the switch-on time to force the average input current equal to the reference current at the time period t_A to t_C. The switching frequency will keep constant because the period T is a constant value in theory. But in the simulation and experimental test, the switching frequency changes a little during the switch mode changes between the mode A and the mode B. These changes are very small so the predicted on-time current control can be treat as fixed frequency current control. The average current error can be nearly zero.

Compare with the new hybrid current control scheme, which is described in the Chapter 3, the predicted on-time equal-charge current has follow disadvantages:

A: The hardware implementation is complex, more feedback signal (V_{dc}) and zero crossing detector circuit needed.

B: The calculation is more complex. DSP controller needs more time for calculation and this limits the switching frequency.

C: Dynamic response is lower. As the on-time of the switch is calculated in the prior period, the actual current may not be the same as the predicted one. All the predicted current control schemes have the same disadvantages.

D: The switching frequency is still variable, even though the changes are minor.

E: The system control has the delay time caused by A/D conversion and other response time.

2.5 A current control strategy to realize zero steady-state control error

This current control strategy can eliminate the steady-state control error completely without using the detected values of the supply voltage and ac-side circuit parameters and keep the

switching frequency constant [7]. The approach can also be said to "eliminate control error digital current control". i.e. to control the average current error (the control error between the actual input current and reference current) to be equal to zero.

As mentioned above, the hysteresis current is not suitable for directly application because of the variable switching frequency. But if combined with other current control techniques, the hysteresis control can be used to accurately control the input current waveform. The "eliminating control error digital current control" scheme is developed based on the combination of the hysteresis current control and carrier-based current control. In this method, the current error is obtained by instantaneously comparing the input current with its reference and then these current errors are applied to a lossless resonant element. As it has an infinite gain at the resonant frequency (will be the fundamental frequency of the supply voltage), the lossless resonant element exhibits a function similar to an integrator for the alternating current component, the frequency of which is equal to the resonant frequency [4]. The Figure 2.12 shows the equivalent circuit of lossless resonant element.

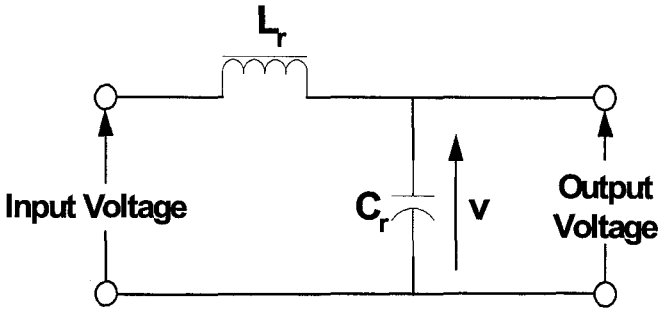


Figure 2.12 Equivalent circuit of lossless resonant element

The output of the lossless resonant element is sent to the carrier based PWM generator as the reference signal for the input voltage of the bridge circuit. A DSP controller is used as the

lossless resonant element because the power loss can't be avoided by using the analog circuit. The loss-less resonant element is introduced and the proposed diagram of feedback controller needed in eliminating control error digital current control scheme is shown in Figure 2.13.

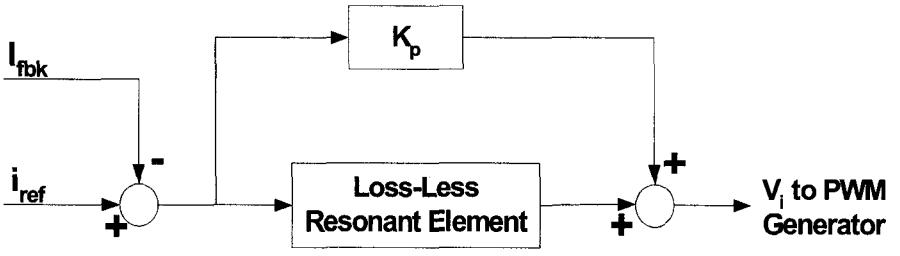


Figure 2.13 Basic resonant element feedback controller

The transfer function $G_r(S)$ of the loss-less resonant element shown in Figure 2.12 is given by following formula:

$$G_r(S) = \frac{K_r}{1+(s/\omega_1)^2} \qquad (2.21)$$

In the formula (2.21), the K_r is the DC gain and the ω_1 is the resonant angular frequency of the resonant element. Here the resonant angular frequency ω_1 is set to the angular frequency ω_s of the supply voltage. When the $s=j\omega_s$ the value of the $G_r(S)$ goes to infinity. In order to improve the transient response, a proportional controller K_p is connected in parallel with the resonant element.

The feedback controller will automatically adjust the output signal of the resonant element to make the fundamental frequency component of the ac input current coincide exactly with its reference. If the fundamental frequency component of the ac input current coincides exactly with its reference, the input control error signal becomes zero and the elimination of the steady-state error in the fundamental component of the supply current is achieved. The block diagram

for the whole control scheme is shown in Figure 2.14.

In Figure 2.13, the L_S and R_S are the inductance and resistance of the ac inductor. The transfer function from the reference current I_{ref} to the actual input current $F_{ii}(S)$ of the eliminating control error current controller shown in Figure 2.13 is given by following formula:

$$F_{ii}(s)=\frac{I_S(s)}{I_{ref}(s)}=\frac{-H(s)/(sL_S+R_S)}{1-H(s)/(sL_S+R_S)} \tag{2.22}$$

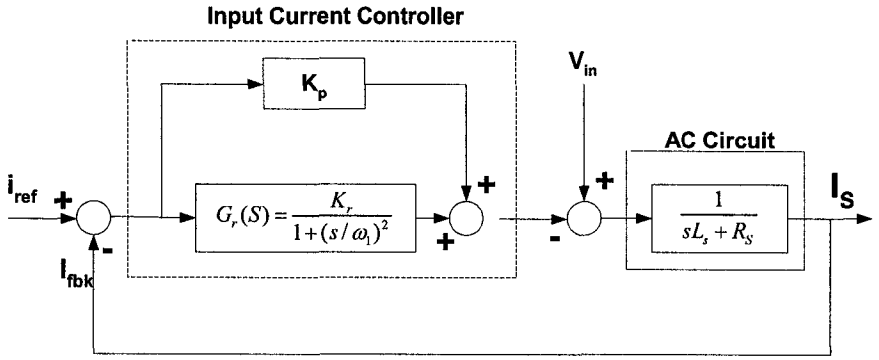


Figure 2.14 Eliminating control error current controller

Where the H(s) is the total transfer function of the feedback controller:

$$H(s)=\frac{K_r}{1+(s/\omega_1)^2}+K_p \tag{2.23}$$

The control characteristics at $s=j\omega_1$ can be obtained by substituting s and H(s) into formula (2.22).

$$F_{ii}(s)=\frac{I_S(j\omega 1)}{I_{ref}(j\omega 1)}=1 \tag{2.24}$$

As the transfer function value of $F_{ii}(s)$ in formula (2.24) is equal to 1, that means the actual input current coincides exactly with the reference current and the steady state controller error in the fundamental component is eliminated completely. The input current can be controlled without knowledge the control parameters K_p, K_r and the ac input circuit parameters

R_S and L_S.

Now the transfer function from the input voltage V_{in} to the actual input current $Fv_i(S)$ of the eliminating control error current controller shown in Figure 2.12 is investigated:

$$F_{vi}(s)=\frac{I_S(s)}{V_S(s)}=\frac{1/(sL_S+R_S)}{1-H(s)/(sL_S+R_S)} \tag{2.25}$$

The control characteristics at $s=j\omega_1$ can be obtained by substituting s and H(s) into formula (2.25).

$$F_{vi}(s)=\frac{I_S(j\omega_1)}{V_S(j\omega_1)}=0 \tag{2.26}$$

As the transfer function value of $F_{vi}(s)$ in formula (2.26) is equal to 0, that means the input ac fundamental frequency voltage does not affect the current control function. But the harmonics in the supply voltage has the effect on the input current control and cause the waveform distortion of the input current. In order to eliminate the waveform distortion due to the harmonics in the supply voltage, an additional lossless resonant element is added in parallel with the feedback controller. The resonant frequency is set to the harmonics frequency [4]. The new feedback controller is shown in Figure 2.15.

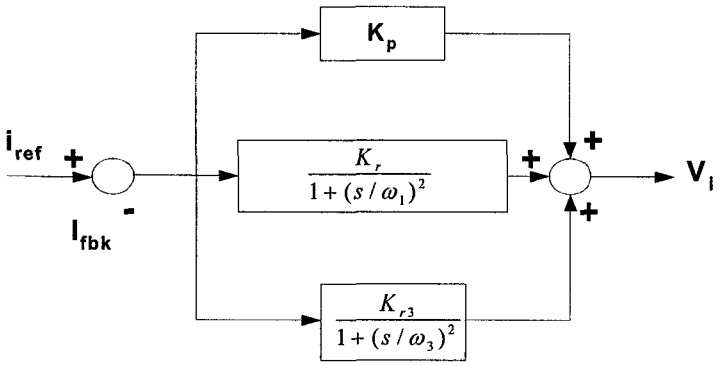


Figure 2.15 Resonant element feedback controller with harmonics elimination

The fundamental of eliminating control error current control scheme has been investigated above. A DSP processor is used as resonant element to simulate the function of proportional integral controller to eliminate the control error. The advantages of ac input current control strategy for the voltage type PWM rectifier include: it could eliminate the steady control error and keep the switching frequency constant, the ac input current could be controlled accurately without knowledge of the supply voltage and the AC side circuit parameters. (Note: the feedback voltage and current signal are still needed). The new control scheme described in chapter 3 has the same advantages, same hardware setup but different control method. It inputs the current errors directly into the carrier based PWM generator to obtain the switching signal. This made the DSP implementation easier.

This control scheme has following disadvantages: the DC gain K_r and the control gain K_p need to be selected deliberately to obtain the stable operation, the resonant element in eliminating control error current control usually is designed for specific frequency for example the fundamental frequency, if the input voltage has harmonics, the harmonics distorts the input current waveform. Extra resonant element needs to be added to the feedback controller to smooth the input current waveform. This makes the design more difficult and the DSP program more complicated. The spectrum of harmonics in the supply voltage is wide and uncertain; it makes it difficult for the eliminating control error current control to completely eliminate the effect of the input voltage harmonics to the input current. This may impede the current controller to achieve the zero control error if the harmonics exist in the supply voltage is too big. The system control has the delay time caused by A/D conversion and other response time.

2.6 Summary

Four current control methods are introduced in this chapter: "delta-modulated hysteresis current control"; "adaptive hysteresis current control"; "predict digital current control" and "realizing zero steady-state control error current control". All of these current control schemes have the same advantages such as fixed switching frequency and Zero steady-state control current error. But as the "adaptive hysteresis current control", "predict digital current control" and "realizing zero steady-state control error current control" need to predict the hysteresis band or switching on-time base on the feedback signals or previous PWM cycle data, many complicated calculation are involved. The DSP speed is slowed down and as the result the dynamic responses of these current controllers are low.

From above we can see that the fixed frequency hysteresis current control by linking the hysteresis band to the amplitude modulation depth m_a is the simplest way to implement. The new current control method that is introduced in the following chapter is developed based on that technique.

Chapter 3 A New Carrier Based Hysteresis Current Controller

The PWM current controller examined in this thesis was designed to combine a fixed switching frequency associated with using a carrier signal, together with good current wave-shaping characteristics, associated with using hysteresis based controllers. The controller was also designed to generate its own amplitude modulation depth without requiring a voltage feedback signal. This latter feature helps force the PWM-cycle average current error to be centered on zero. Four kinds of current-control techniques are investigated in chapter 2. This chapter describes a new unipolar carrier based hysteresis current-control technique for single-phase PWM rectifier based upon the delta-modulated and carrier based PWM signal generators described in chapter 3. The resultant PWM current controller achieves fixed switching frequency, excellent current tracking capability and zero average current error. Some background about the carrier based delta-modulated PWM controllers are introduced first.

3.1 Carrier based delta-modulated PWM controller

The proposed "carrier based delta-modulated PWM controller" is a fixed frequency carrier based PWM signal generator that combines the hysteresis-based and carrier-based current controllers together. Even though both the "carrier based delta-modulated PWM controller" and the "fixed frequency delta-modulated PWM signal generator" can achieve fixed switching frequency, the principles are different. In the fixed-frequency delta-modulated PWM controller

the hysteresis band h can be pre-determined by using the formula (2.6) and (2.7) to fix the switching frequency of V_{PWM} and here is compared V_{ref} with hysteresis band h to generate the PWM switching signal. In carrier-based delta-modulated PWM controller the V_{ref} is compared with the carrier sawtooth signals to generate the PWM switching signals. The switching frequency can still be fixed without calculating the hysteresis band h. Both PWM controllers have the same characteristic in that the signal V_{ref} ramps between a positive and negative maximum defined by band h and the average of the resultant PWM waveform $V_{PWM,\,av}$ is independent to the signal integration R and hysteresis band magnitude h.

In the proposed carrier based delta-modulated PWM current controller there are two ways to obtain the unipolar PWM switching signals to force the average current error per PWM cycle to zero: one is to compare the integrator output V_{ref} with the sawtooth carrier signals V_{C+} and V_{C-} and another one is to compare the integrator output V_{ref} with the sawtooth carrier signals subtracting the m_a (V_{C+}- m_a) and (V_{C-}- m_a). The detail schemes are shown in Figure 3.1 and 3.2.

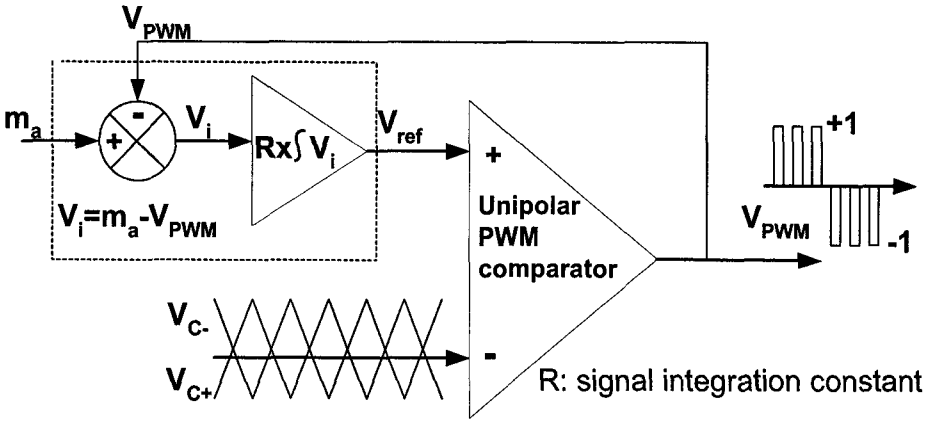


Figure 3.1 Type 1: v_{ref} compared with sawtooth V_{C+} and V_{C-}

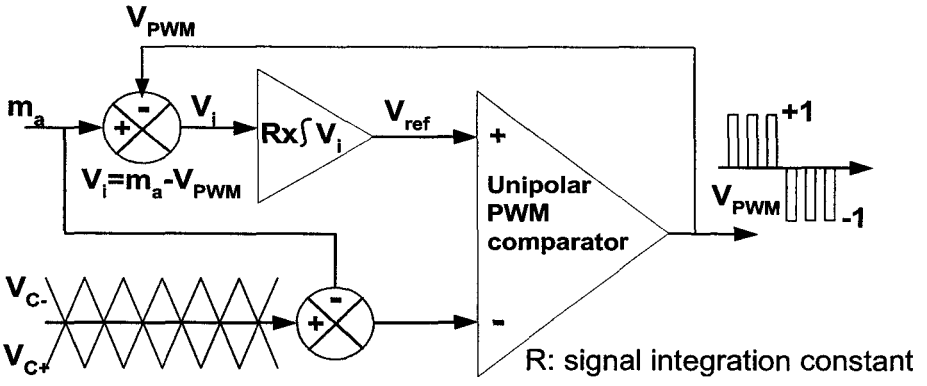


Figure 3.2 Type 2: v_{ref} compared with sawtooth (V_{C+} -m_a) and (V_{C-}-m_a)

The signal m_a in Figure 3.2 is a sine-wave amplitude modulated signal and represents the supply voltage. The unipolar PWM voltage signal V_{PWM} represents the rectifier input voltage. V_{ref} represents the rectifier input current or inductor current. $V_{ref} = K \times i_L$. The parts in the dotted rectangle shown in Figure 3.1 simulate a signal phase rectifier circuit with input inductor. The K_1 factor determines the value of input current ripple. It can be decided based on the rectifier circuit parameters. Detail description of the PWM generator is given in the following section.

3.2 Carrier based delta-modulated PWM controller simulation result

In the type 1 of the carrier based delta-modulated PWM controller shown in the Figure 3.1, V_{ref} is compared with two sawtooth carrier signals by using a unipolar PWM comparator to generate the PWM waveform V_{PWM}. Since V_{ref} is the integration result of (m_a-V_{PWM}), it varies naturally with the magnitude of m_a. An expanded waveform of V_{ref} is shown in Figure 3.3. V_{ref} follows the sine wave reference template and the average of the current error per PWM cycle can be maintained close to zero.

In the Figure 3.2, the signal V_{ref} is obtained as the same way as the type 1. The difference

between the type 1 and type 2 is the ways in which the PWM signal is created. In type 1 the V_{ref} is compared with two sawtooth carrier signals, the waveform of the sawtooth carrier signals will not vary. But in type 2, the V_{ref} is compared with sawtooth minus m_a. The waveform of the sawtooth carrier signals is modulated by the reference waveform m_a. The waveform for V_{ref} is centered on zero and does not vary to follow the sinusoidal m_a varing signal, see Figure 3.4..

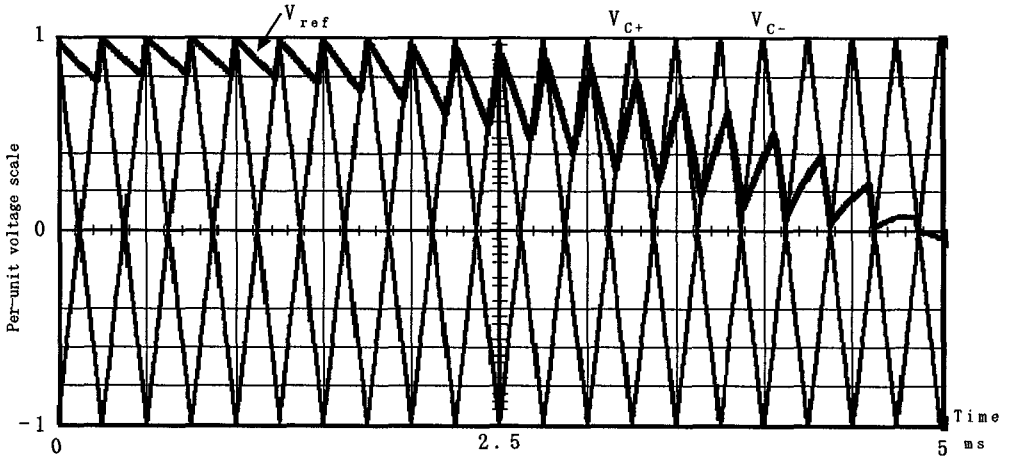


Figure 3.3 Waveform of v_{ref} compared with sawtooth V_{C+} and V_{C-}

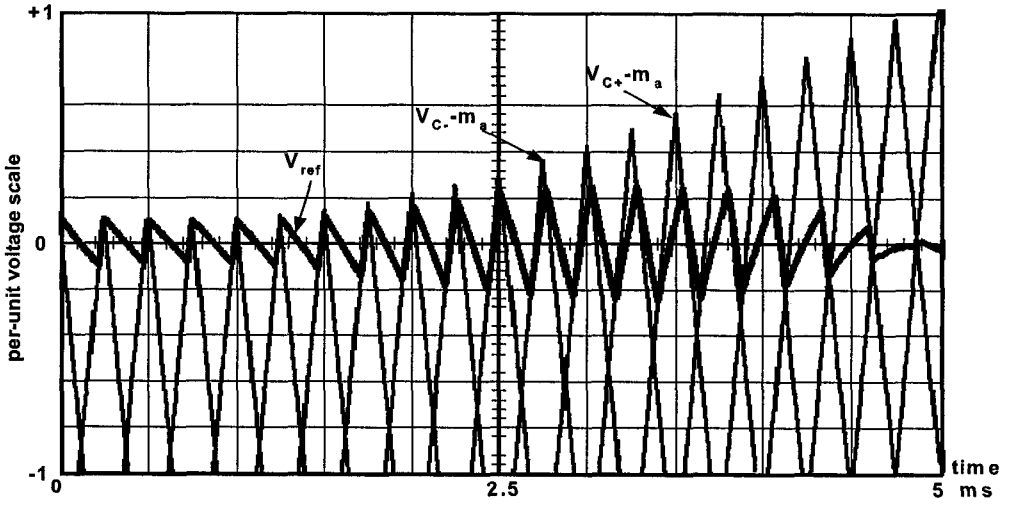


Figure 3.4 Waveform of v_{ref} compared with sawtooth (V_{C+} -m_a) and (V_{C-}-m_a)

The simulated waveform of type 2 carrier-based delta-modulated PWM controller is shown in Figure 3.4. The difference between the two approaches can be seen clearly by comparing the waveforms shown in Figure 3.3 and 3.4. In the type 2 the switching cycle average of V_{ref} is zero and is not required to follow the sinusoidal m_a. The detail waveforms of the saw-tooth minus m_a are also shown in Figure 3.5. As the type 2 can always maintain the current error centered at zero, that is the preferred method and the new hybrid current-control is developed based on this type.

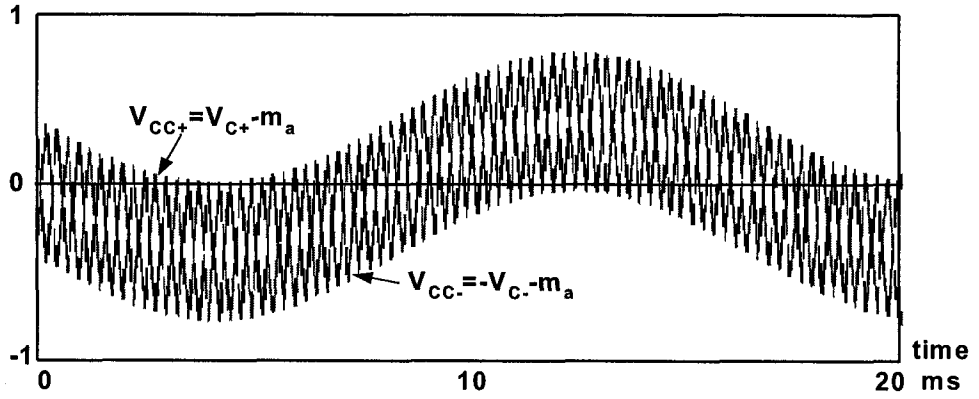


Figure 3.5 Waveform of carrier signal modulated by the m_a

The frequency spectrum of the unipolar PWM waveform for both type 1 and 2 are centered at twice the sawtooth carrier frequency f_C.

3.3 Investigation on the proposed PWM controller's parameter

The peak-to-peak value of V_{ref} is equivalent to hysteresis band h in the hysteresis current-control and the ΔV_{ref} can be derived from the formula (2.4):

$$\Delta V_{ref} = \frac{R}{2f_C} \times m_a(1-m_a) \qquad (3.1)$$

The formula (3.1) means the peak value of ΔV_{ref} is determined by the signal integration constant R and the amplitude modulation depth m_a. Note the carrier frequency is a constant value. V_{ref} represents the input current passed through the input inductance in type 1, see Figure 3.1, and the current error in type 2, see Figure 3.2, the ΔV_{ref} represent the current ripple and the current ripple can be affected by the size of the inductance. The signal integration constant R represents the size of the input inductance because $R \propto \frac{1}{L}$. A simulation waveform, produced using the type 1 scheme, (see Figure 3.6), shows the signal V_{ref} using fixed values of m_a and switching frequency f_C, but the integration constant R varied over a wide range. The result on current ripple ΔV_{ref} changes with R, but the average of the PWM waveform, v_{pwm}, does not change.

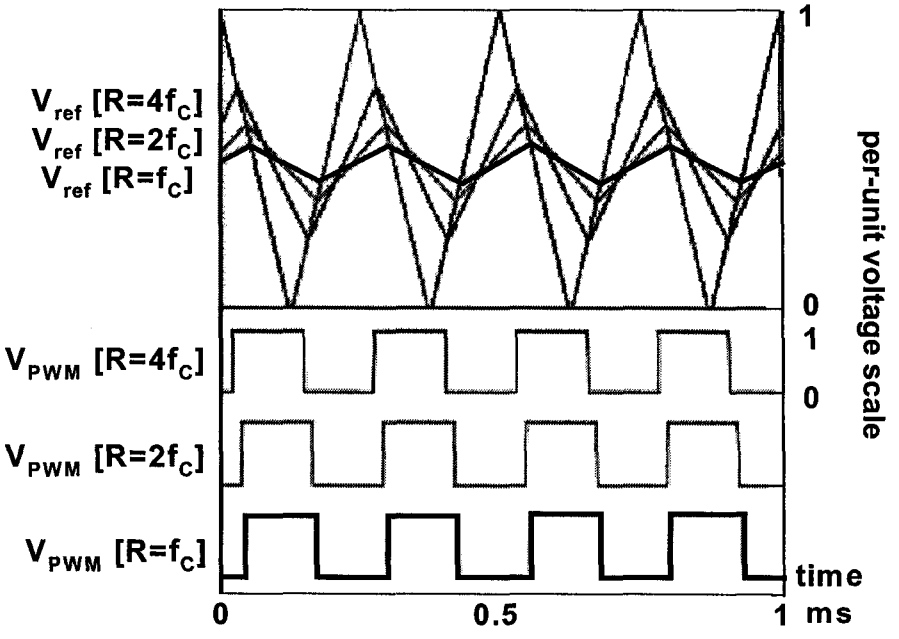


Figure 3.6 Type 1 V_{ref} Waveform for different R for m_a=0.5, f_C=2Khz

From the formula (2.4) we can see that the ΔV_{ref} varies following the m_a. The maximum value of $m_a(1-m_a)$ is at m_a=0.5 and the value is 0.25. If R=4f_C, the ΔV_{ref} (peak-to-peak ripple in the signal V_{ref}) can be obtained as following:

$$\Delta V_{ref} = 0.5 p.u. \qquad (3.2)$$

The simulation results show that the integration constant R can vary over a wide range and that the average of V_{ref} hence $V_{PWM,av}$, is still accurately determined by m_a. The main effect on V_{PWM} is a slight phase shift relative to the carrier signal. With R=4f_C and m_a=1 the maximum slope of V_{ref} matches the slope of the sawtooth carrier waveform. However with appropriate switching logic, R can exceed this value (R=4f_C), as illustrated in Figure 3.7. That is significant that the current controller has the capability of coping with a wide variation in R. This is a useful feature in a current controlled PWM rectifier because the integration constant R in proposed PWM controller is not required to be fixed accurately. The R is essentially determined by the circuit inductance size and DC link voltage. That means the proposed PWM controller is insensitive to circuit parameter variations such as inductance.

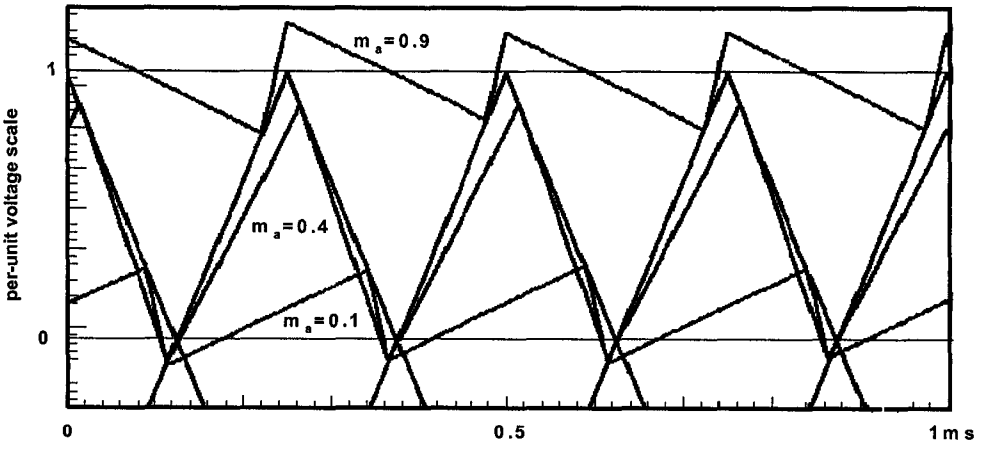


Figure 3.7 Type 1 V_{ref} waveform for R=8f_C

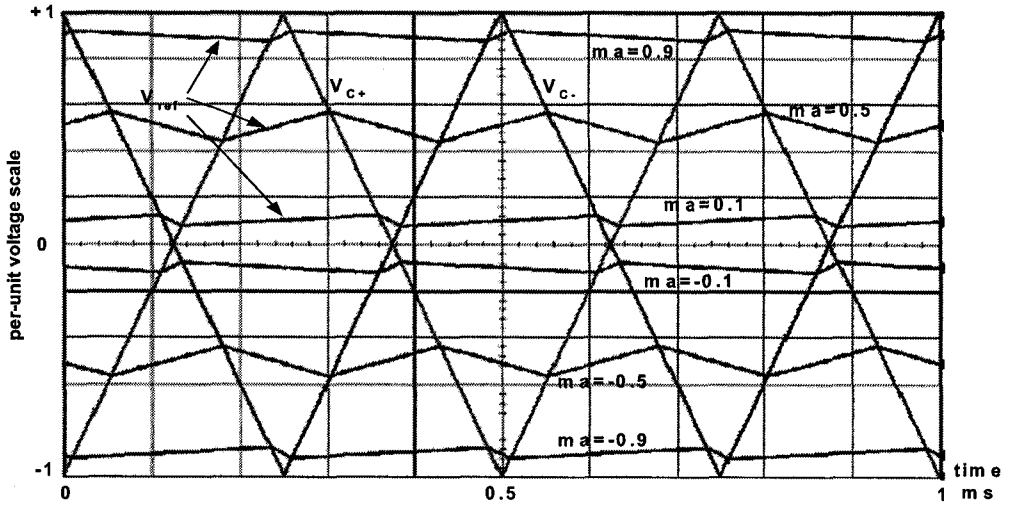


Figure 3.8 Type 1 V_{ref} waveform at different m_a

Figure 3.8 illustrates the type 1 control scheme simulation result of how V_{ref} changes when the m_a is set at different values. V_{ref} changes with m_a if m_a is changed in a sinusoidal pattern.

The differences between the type 1 controller and type 2 controller can be observed in waveforms where both schemes use the same value of m_a, carrier frequency f_C and integration constant R, see Figure 3.9 and 3.10. Both controllers generate the same waveform shape for V_{ref} and V_{PWM}. But in the type 2 PWM controller the V_{ref} is maintained at an average value of 0. Figure 3.11 and Figure 3.12 shown the V_{ref} and m_a waveform with $m_a=0.9\text{Sin}(2\pi f_C t)$, carrier frequency f_C=2KHz and $R=4f_C$/sec. In type 1 controller, V_{ref} varies sinusoidally with m_a and lags m_a due to the nature of the signal integrator. This also results in V_{PWM} lagging the m_a. This phase shift is the main cause for the skewing of the i_{error} signal in single-phase PWM rectifiers with current feedback.

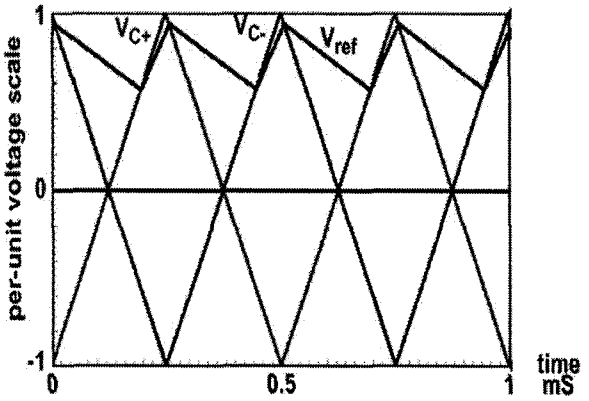


Figure 3.9 Type 1 with m_a=0.75, f_C=2KHz,R=4f_C/sec

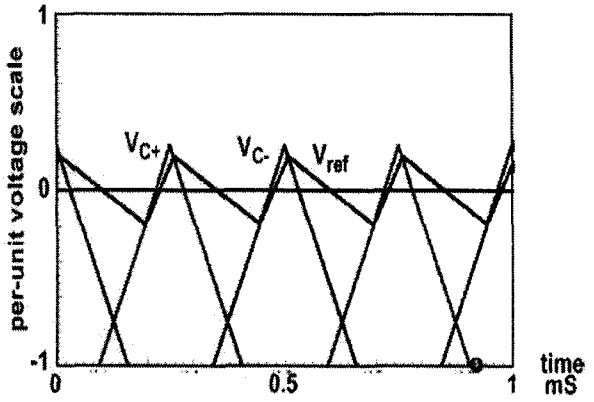


Figure 3.9 Type 2 with m_a=0.75, f_C=2KHz,R=4f_C/sec

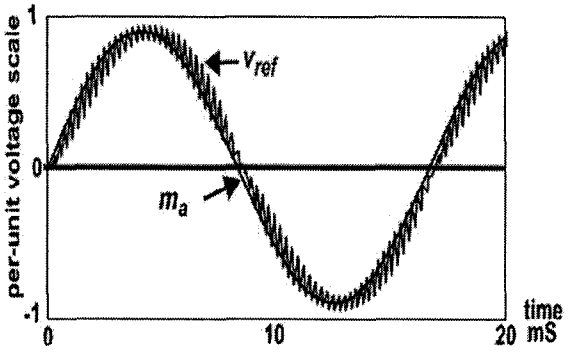


Figure 3.11 Type 1 waveform with m_a=0.9Sin(2πf_Ct), f_C=2KHz, R=4f_C/sec

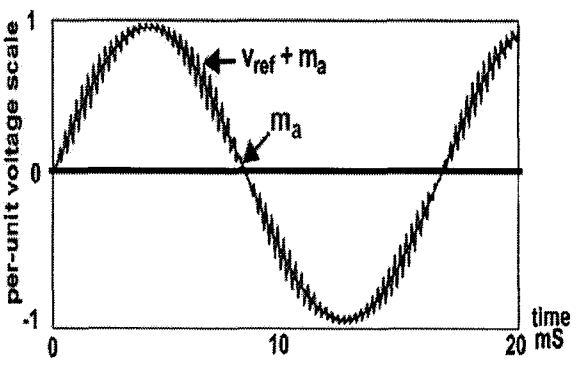


Figure 3.12 Type 2 waveform with m_a=0.9Sin(2πf_Ct), f_C=2KHz, R=4f_C/sec

For type 2 PWM controller, the V_{ref} is always maintained centered at zero while the m_a varies sinusoidally with no phase shift in V_{PWM}, or the reconstructed signal V_{ref}-m_a, because the sawtooth carrier signal is modulated by m_a. Figure 3.13 shows the type 2 unipolar PWM and integrator output signal waveforms. V_{ref} is maintained centered at zero which is a useful advantage for a current controller. This represents the current error signal being centered on zero, hence a close to zero PWM cycle average current error..

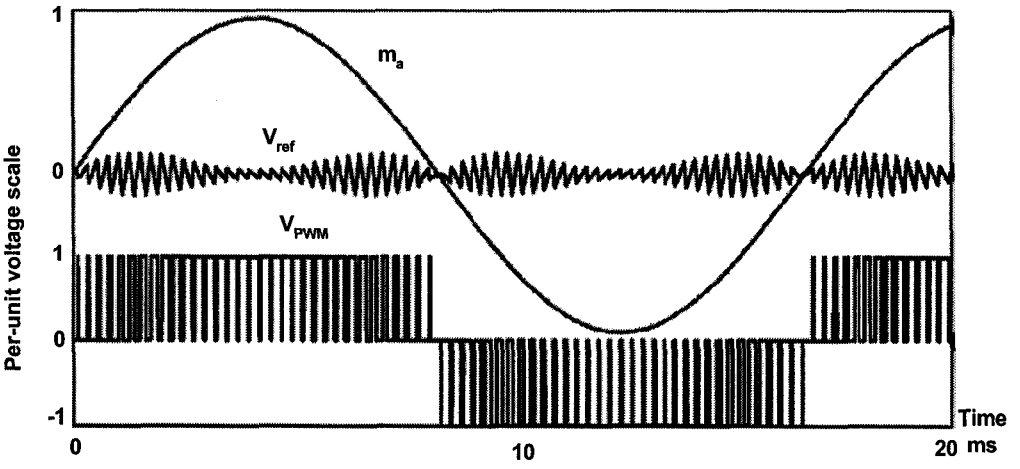


Figure 3.13 Type 2 unipolar PWM and integrator output signal waveform

3.4 New hybrid current controller

The type 2 PWM controller has an attractive operation advantage for a current controller as V_{ref} signal is always maintained centered at zero. This represents the current error signal to be centered at zero. The PWM cycle-average of V_{PWM} is unaffected by R and no phase shifts are introduced into V_{PWM} hence no skewing of the V_{ref} (or i_{error}) due to the sinusoidal modulation of V_{PWM}. Note that a design goal of the new hybrid current controller is to achieve fixed switching frequency with zero PWM cycle current error and no skewing.

The proposed new current controller based on type 2 requires a means for obtaining the signal m_a. Two possible ways to obtain the m_a include: one is obtained from the feedback signal of the supply voltage, or another one is to obtain m_a from the feedback signal of PWM output V_{PWM}. These schemes are illustrated in Figure 3.14 and 3.15.

The general structure of PWM controllers uses an integrator as described in this chapter

for unipolar PWM waveforms since this matches the function of the single-phase rectifier. The signal V_{ref} is equivalent to the current error signal with an appreciate feedback gain constant K_1:

$$V_{ref} = K1 \times i_{error} \tag{3.3}$$

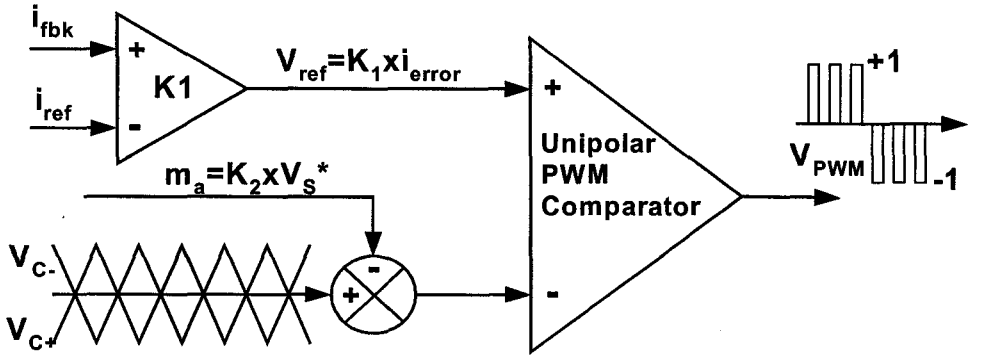


Figure 3.14 Current controller using supply voltage feedback to obtain m_a

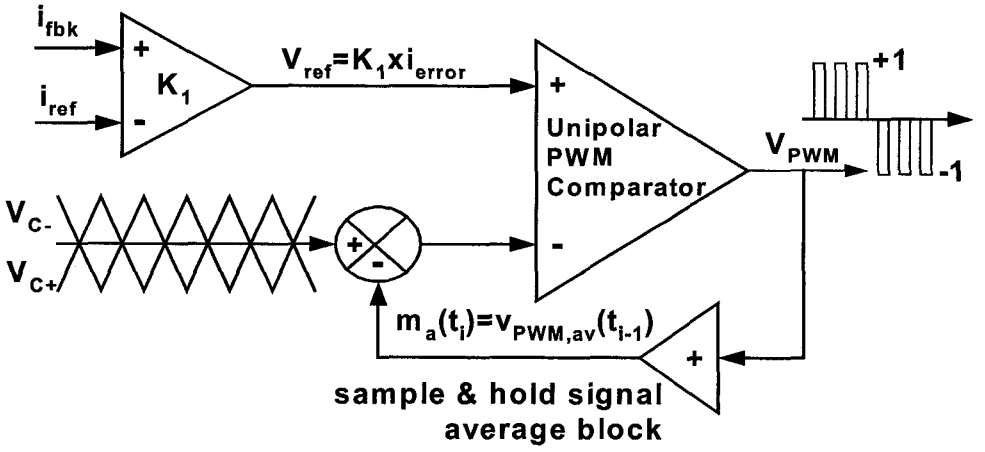


Figure 3.15 Current controller using sampled feedback of V_{PWM} to obtain m_a

We can derive the following formulas by comparing the expression for ΔV_{ref} in formula (3.1) with an expression that defines the current ripple Δi_{error} obtained in the PWM rectifier, and assuming that the feedback gain factor K_1 is used to obtain a per unit value for the signal i_{error}:

$$\Delta V_{ref} = m_a(1-m_a)\frac{E}{2f_C L_S}K_1 = \frac{R}{2f_C}\times m_a(1-m_a) \tag{3.4}$$

$$R = K_1\frac{E}{L_S} \tag{3.5}$$

Since the PWM generator is insensitive to variation in R, this is equivalent to the controller being insensitive to variations in the rectifier parameters such as the supply inductance L_S and the dc link voltage E. Now the design process is described below.

At first the current feedback loop is designed and the parameters are selected based on following formula:

$$\Delta I = m_a(1-m_a)\frac{E}{2f_C L_S} \tag{3.6}$$

which is maximum at m_a=0.5:

$$\Delta I_{max} = \frac{E}{8f_C L_S} \tag{3.7}$$

As the constant R is selected to allow the controller to respond rapidly during transients, the value $R=4f_C$, this produces ΔV_{ref}=0.5. So an appropriate design choice for K_1 based on formula (3.7) is equal:

$$K_1\Delta I_{max}=0.5 \Rightarrow K_1 = \frac{1}{2\Delta I_{max}} \tag{3.8}$$

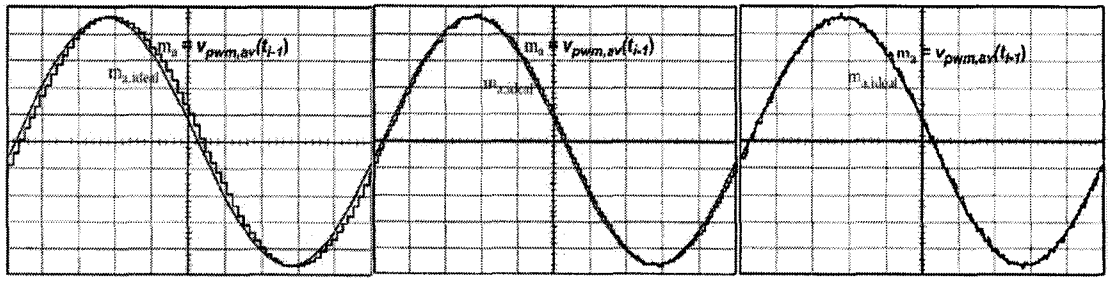
The current controller shown in Figure 3.14 requires a reference signal m_a that represents the ideal sinusoidal voltage. V_S^* required at the rectifier input terminals obtains a sinusoidal supply current in phase with the supply voltage V_S. This signal can be obtained from the feedback of the supply voltage. But the supply voltage cannot be used because V_S^* lags the supply voltage and it is difficult to predictly obtain an accurate value for K_2. So a modified

controller shown in Figure 3.15 is considered. In every half-cycle the second controller uses the m_a obtained from the previous half-cycle to modulate the carrier signals and is equal to:

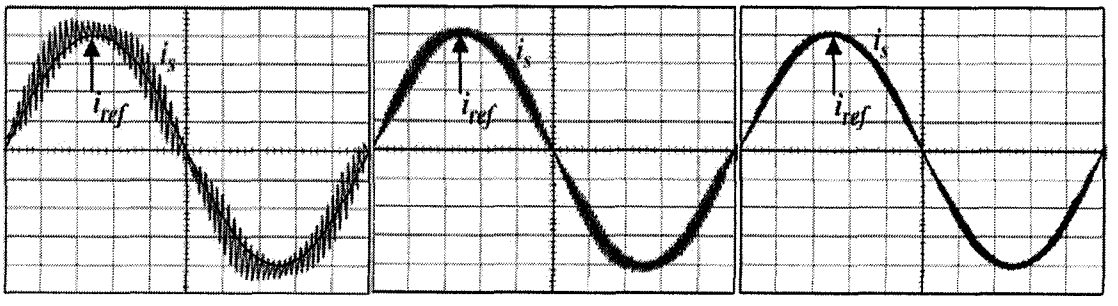
$$m_a(t_i) == v_{PWM}(t_{i-1}) \tag{3.9}$$

m_a at time t_i ($i=i^{th}$ carrier half-cycle) is determined from the average of V_{PWM} during the previous $(i-1)^{th}$ half-cycle. This modification makes it unnecessary to use the supply voltage in the generation of the PWM waveform.

Simulation tests were undertaken on the current controller structure shown in Figure 3.15 using a single-phase PWM rectifier and the results include real time generation of the amplitude modulation signal m_a as shown in Figure 3.16. The experimental test result by using ADSP-21992 DSP controller is given in chapter 6.



F_c=2Khz, K_I=0.215, L_S=7.5mH F_c=4Khz, K_I=0.43, L_S=7.5mH F_c=8Khz, K_I=0.86, L_S=7.5mH



F_c=2Khz, K_I=0.215, L_S=2.5mH F_c=4Khz, K_I=0.43, L_S=2.5mH F_c=8Khz, K_I=0.86, L_S=2.5mH

Figure 3.16 Simulation result for proposed current controller

3.5 Summary

In this chapter the development of a delta modulated carrier based current controller is described that generates PWM voltage waveforms for a single-phase PWM rectifier. Examination of generic PWM modulators using a signal integrator is undertaken to show how delta modulated signals can be used with carrier signals to produce output PWM waveforms that are independent of the integrator constant.

The result current controller uses a sinusoidal amplitude modulated reference signal that is internally generated from a unipolar PWM modulator output signal. The size of the high frequency ripples in the current error signal changes with the size of inductance but the average current error is always kept close to zero.

Chapter 4. DSP Current Controller: ADSP-21992

In order to demonstrate the experimental operation of the proposed current control, a DSP controller was selected. In this chapter a detail description of the ADSP-21992 DSP core is given including the PWM generator, ADC port and the evaluation board. The DSP software control program is described in chapter 6.

The ADSP-21992 is a mixed signal DSP controller based on the ADSP-219x DSP Core, suitable for a variety of high performance power electronics real time control (PWM) and digital signal processing applications that require the combination of a high performance DSP and the mixed signal integration of embedded control peripherals such as analog-to-digital conversion (ADC) and digital-to analog conversion (DAC).

4.1 PWM generator

The DSP controller is a versatile DSP that has a programmable PWM generator that can produce three pairs of PWM signals on the six PWM output: AH, AL, BH, BL, CH and CL. The duty cycles of these outputs can be controlled together with the signal polarity; dead time control to prevent potentially destructive short-circuit (dead time is a delay time added to the PWM signals to avoid the switches in the same inverter leg to be turned on at the same time, during this delay time both switches in the same inverter leg are both off); an internal synchronization pulse based on the PWMTM and PWMSYNCWT register values to synchronize the PWM switching frequency; shutdown of the PWM output signals in the event of external fault conditions. A block diagram of the PWM generation unit is illustrated in Figure 4.1[3].

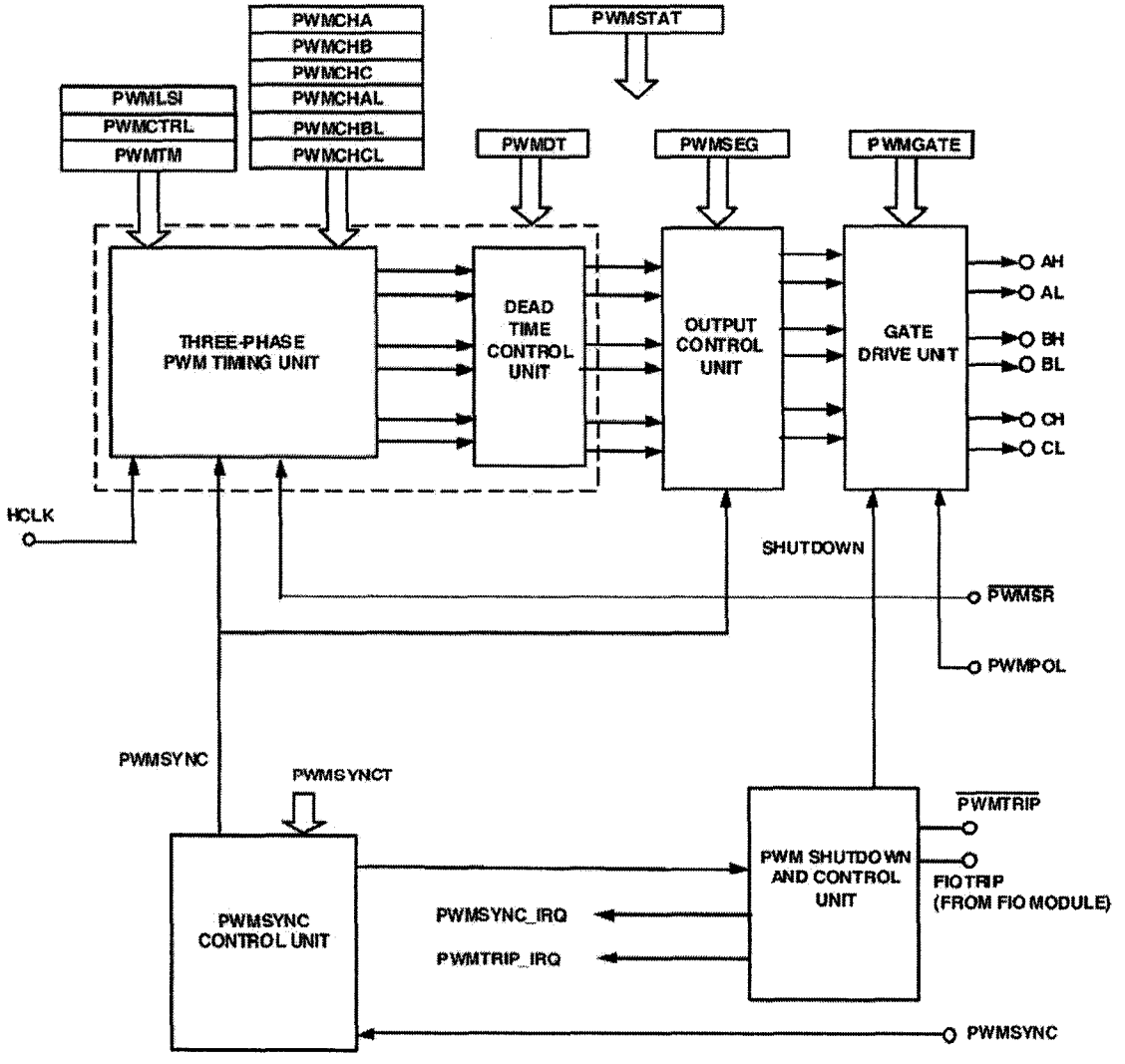


Figure 4.1 PWM Generation Units

The DSP PWM generation unit can be controlled in two ways: hardware and software. The hardware control is performed by tying the relative control pins to active high or active low. The software control can be completed by writing the correct value to relative registers.

The polarity of the PWM output signal is controlled by hardware. In order to generate the active HI patterns PWM output, tie the PWMPOL pin to active HI and tie the PWMPOL pin to

active LO when the active LO pattern PWM output needed. This setting had be set to active high before the control program starts.

The DSP PWM generation unit has following registers for the software control:

Register	Name
PWM control register	PWMCTRL
PWM status register	PWMSTAT
PWM period register	PWMTM
PWM duty cycle register	PWMCHA, PWMCHB, PWMCHC
PWM low side duty cycle register	PWMCHAL, PWMCHBL, PWMCHCL
PWM dead time register	PWMDT
PWM gate register	PWMGATE
PWM segment register	PWMSEG
PWM synchronization signal width register	PWMSYNCWT
PWM low side invert register	PWMLSI

These registers are put in the I/O memory page 8. Following program gives an example of how to go through these registers (the registers below are freely selected to illustrate how to go through the PWM register in C program):

```
sysreg_write (sysreg_IOPG, PWM0_Page);  /* go to I/O memory page 8
PWM_Period=io_space_read(PWM0_TM); /* read the PWM periodvalue from the register
                                        PWM0_TM.
io_space_write(PWM0_CHA,0); /* write the PWM duty cycle to the PWM control register
                                PWM0_CHA.
```

4.1.1 PWM operating mode

The PWM generation unit has two distinct operating modes, "single update mode" or "double update mode". In "single update mode" the duty cycle values are updated only once per PWM period and the PWM waveforms are symmetrical to the mid-point of the PWM period. In the "double update mode" the duty cycle values are updated twice per PWM period: one at the beginning of the PWM period and one at the midpoint of the PWM period, the waveform will be

asymmetrical to the mid-point of the PWM period. The operating mode can be selected by a control bit in PWM control register (PWMCTRL).

The PWM generator can also generate an internal synchronization pulse based on the value of PWMTM to synchronize the PWM switch frequency. The width of the In PWMSYNC pulse is controlled by synchronization signal width register (PWMSYNCWT). In single update mode a PWMSYNC pulse is generated at the start of each PWM period. In double update mode, two PWMSYNC pulse is generated: one at the start of each PWM period and one at the mid-point of each PWM period.

A faster control and lower response voltage harmonic in three-phase inverter application are the advantages of the double update mode. However, the higher switching losses and larger computational burden are also the obvious disadvantage of the double update mode.

4.1.2 PWM switching frequency control

The PWM switching frequency is controlled by writing the values to a 16-bit read/write PWM period register PWMTM. The basic timing unit of the PWM controller is t_{ck}, which is defined based on the DSP peripheral clock. When the peripheral clock f_{ck} is 80MHz, the basic time increment t_{ck} is 12.5ns. The value written to the PWMTM register is effectively the number of t_{ck} increments in half a PWM period. The value of the t_{ck} increment value can be calculated using the following formula:

$$PWMTM = \frac{f_{ck}}{2 \times f_{PWM}} \tag{4.1}$$

f_{PWM}: Desired PWM switching frequency

And the PWM switching period T_s can be written as:

$$T_S = 2 \times PWMTM \times t_{CK} \tag{4.2}$$

For example, for an 80MHZ HCLK and 2 KHz desired PWM frequency, the PWMTM is:

$$PWMTM = \frac{80 \times 10^6}{2 \times 2 \times 10^3} = 20000$$

As the maximum value of 16-bit PWMTM register is 0xFFFF (=65535), when the HCLK is 80 MHz, the minimum PWM switch frequency will be:

$$f_{\min PWM} = \frac{80 \times 10^6}{2 \times 65535} = 610Hz$$

4.1.3 Dead time control

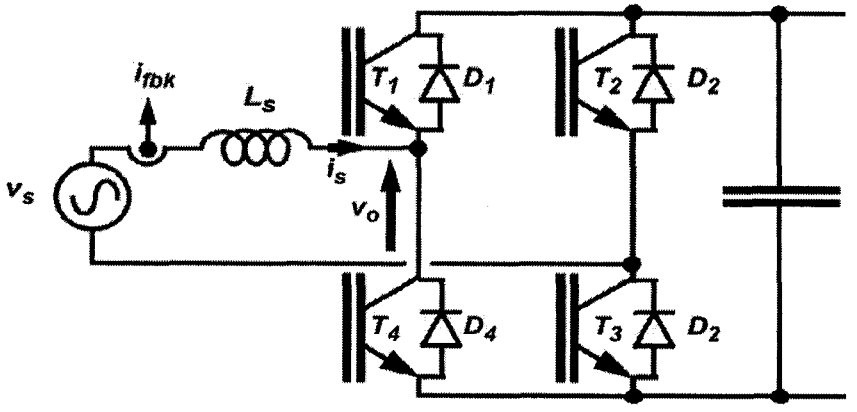


Figure 4.2 Diagram of single-phase H-bridge rectifier

Figure 4.2 show a diagram of single-phase H-bridge rectifier. In order to prevent the potentially destructive short circuit condition, the switcher in the same inverter leg (e.g. T_1, T_4 or T_2, T_3) should not be turned on at the same time. A short delay time is introduced to permit one power switch to be turn off completely before the complementary switch to be turn on. The value of the dead time inserted into the three pairs of PWM output is controlled by one 10-bit, read/write PWMDT register. The value written to the PWMDT register determines the dead time T_d:

$$T_d = PWMDT \times 2 \times t_{CK} \qquad (4.3)$$

For example, the value in PWMDT register is 0x028 (=40), the dead time T_d equal:

$$T_d = 40 \times 2 \times 12.5ns = 1us$$

As the maximum value of 10-bit PWMDT register is 0x3FF (=1023), when the HCLK is 80 MHz, the maximum dead time will be:

$$T_{d,Max} = 1023 \times 2 \times 12.5ns = 25.6us$$

The Figure 4.3 shows how the dead time is inserted into the PWM signals[3].

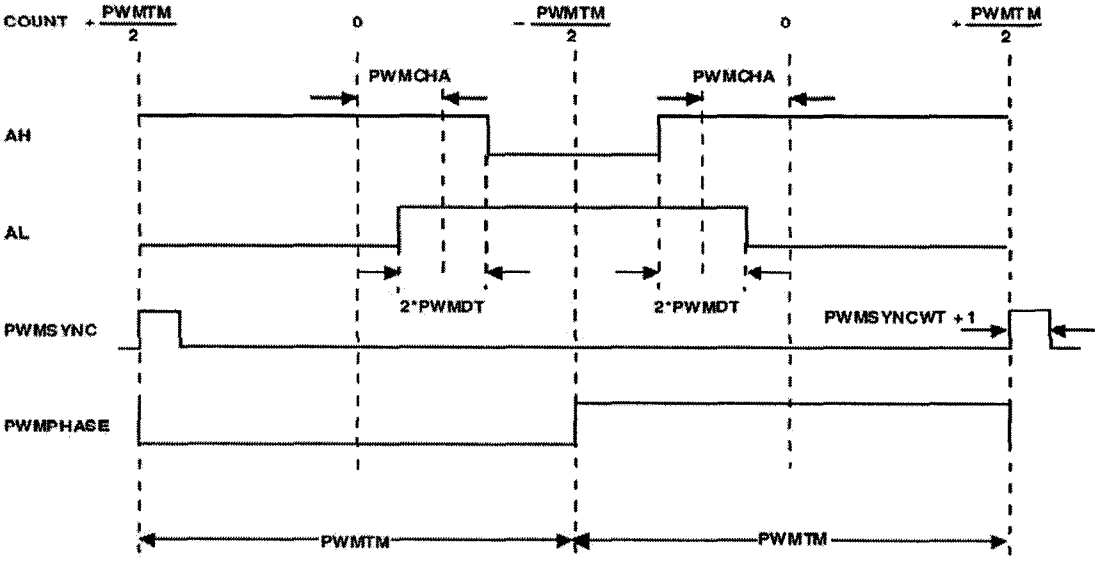


Figure 4.3 PWM output signal with dead time

The duty cycle range is from $(\frac{-PWMTM}{2} - PWMDT)$ to $(\frac{PWMTM}{2} + PWMDT)$ and the value of 0 represents a 50% PWM duty cycle.

4.1.4 Other PWM control

In the event of external fault condition, all six PWM output are placed in the OFF state. A falling edge on the $\overline{\text{PWMTRIP}}$ pin provides an instantaneous shutdown of the PWM controller. The PWM generator permit independent crossover of the two signals of a PWM pairs by set or clear the three control bits of the PWM segment register (PWMSEG). In crossover mode, the PWM signal high side switch is diverted to complementary low side output and the complementary low side switch is diverted to complementary high side output.

The three pairs of PWM output can be enabled or disabled by set or clear corresponding bit of PWM segment register (PWMSEG).

The status information about the PWM system is available to the user in the PWMSTAT register. When the interrupt occurs, the PWMSYNCINT and PWMTRIPINT bits in the PWMSTAT register are latched and held on the interrupt event and must be cleared by the control software during the interrupt service routine.

4.2 Analog to digital converter system

The ADSP-21992 contains a fast, high accuracy, multiple input analog to digital conversion system [22]. The maximum data sampling speed for one DAC channel is 2.5 MSPS at 20MHz ADCCLOCK. The ADC system can simultaneously sample two input signals in DMA-assisted data sampling mode. The ADC system contains a precision internal 1.0V voltage reference, which can be enable or disable by using the jumper JP3 and JP4. In this experimental test the internal reference was enabled. The input signals were centered at 1.0V and the maximum analog input voltage is 2V peak-to-peak.

The DSP ADC system has the following registers for the software control:

Register	Name
ADC control register	ADCCTRL
ADC status register	ADCSTAT
ADC software convert start register	SOFTCONVST
ADC data registers	ADC0 to ADC7
ADC latched data registers	ADCLATCHA, ADCLATCHB
ADC timer register	ADCTIMER

These registers are defined and arranged in the I/O memory page 13. Following program gives an example of how to go through these registers (the registers below are freely selected to illustrate how to go through the PWM register in C program):

```
sysreg_write (sysreg_IOPG, ADC_Page);  /* go to I/O memory page 13
data_read=io_space_read(ADC_DATA0); /* read the converter channel 0 value from
                                       the register ADC_DATA0.
io_space_write(ADC_CTRL,0); /* write the value to the ADC control register ADCCTRL.
```

4.2.1 ADC converter general description

The ADSP-21992 ADC converter system is a 14-bit pipeline (6-stage) flash analog to digital converter with 8 analog inputs. The functional block diagram of the ADC system is shown in Figure 4.4[3]. The input signals are divided into two banks: VIN0-VIN3 makes up one bank and VIN4-VIN7 make up the second bank. Each bank has an output to the corresponding sample & hold amplifier and the input signals can be correctly biased to the nominal operating range of the ADC. The various analog inputs can be switched to sample & hold amplifier by the internal multiplexers. The value of internal or external voltage reference determines the maximum input voltage range. In this experimental test, the internal 1.0V reference voltage is predefined by using jumper JP3 an JP4, so the maximum input analog voltage is 2V peak-to – peak.

The maximum ADC clock rate is 20MHz. The ADC clock rate ADCCLOCK is programmable by the user via the 4-bit field ADCCLKSEL in the ADC control register ADCCTRL [11:8]. The value 0 and 1 in ADCCLKSEL are not allowed and writing 0 or 1 to ADCCLKSEL will disable the ADC CLOCK.

$$ADCCLOCK = \frac{HCLK}{2 \times ADCCLKSEL} \tag{4.4}$$

$$ADCCLKSEL \in [2,15]$$

When ADCCLKSEL=2, the ADC clock rate is equal to its maximum value 20MHz.

At 20MHz clock rate the ADC can convert all 8 channel input signals in approximately 725ns, the first data value is available approximately 375ns after the convert start command.

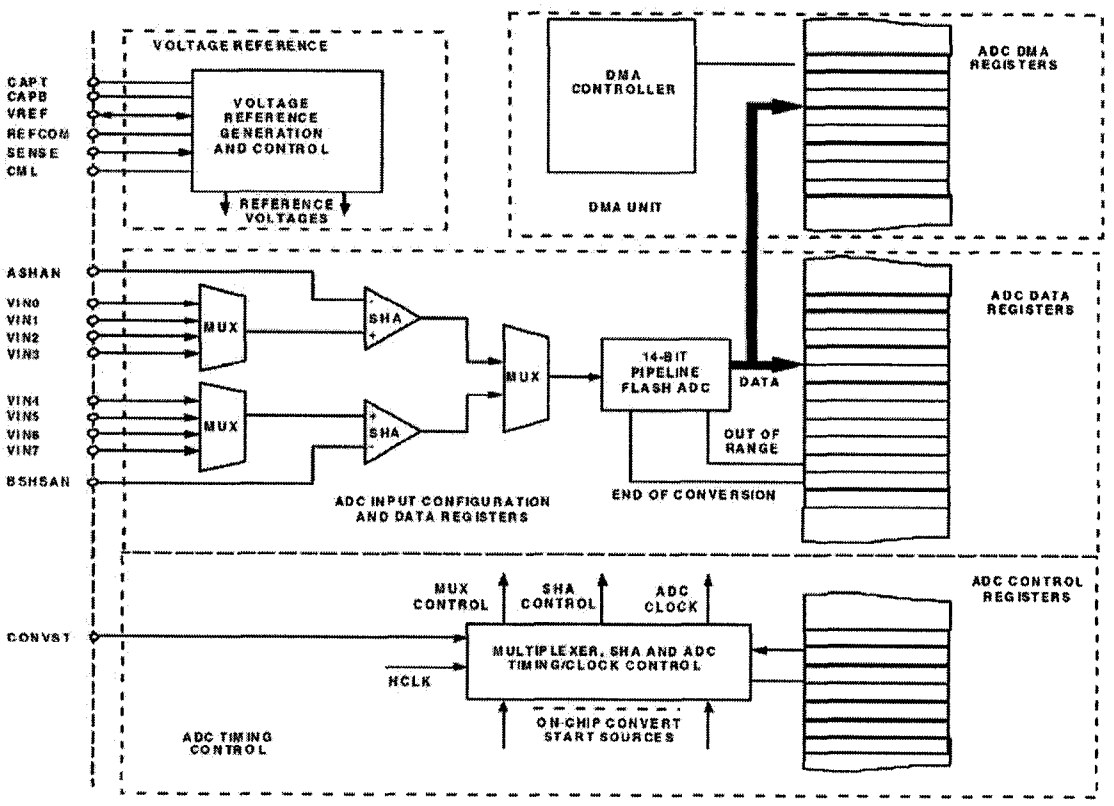


Figure 4.4 Functional block diagram of the ADSP-21992 ADC system

4.2.2 ADC control

The ADC conversion process can be started by four different ways and the TRIGSRC bit field in the ADC control register ADCCTRL [2:0] is used to select the way in which to start the conversion process. The conversion start trigger events include:

- Rising edge of the internally derived PWM synchronization pulse PWMSYNC.
- Rising edge of the external CONVST pin.
- Writing to the SOFTCONVST register.
- Rising edge of the internally derived auxiliary PWM synchronization pulse AUXSYNC.

The ADC system has two basic conversion modes, "timed conversion" and "DMA-assisted" data sampling mode. And within each of the two modes, there are a number of different operating modes.

In a "timed conversion" mode there are 3 different operation modes:

- Simultaneous sampling mode (default mode).
- Latch mode.
- Offset calibration mode.

In a "DMA-assisted" mode there are 4 different operation modes:

- DMA signal channel acquisition.
- DMA dual channel acquisition.
- DMA quad channel acquisition.
- DMA all channel acquisition.

The operating mode is selected by the MODSEL bit field in the ADCCTRL Register [6:4]. In this experimental test, the "DMA-assisted" dual channel acquisition mode was selected to fast the data conversion speed because we had more than one feedback signals.

4.3 ADSP-21992 core microprocessor

The most useful parts in this experimental test, PWM generator and ADC system, have been introduced section 4.1 and 4.2. This section gives a brief description of the ADSP-21992 core microprocessor to explain how the DSP works.

4.3.1 General description.

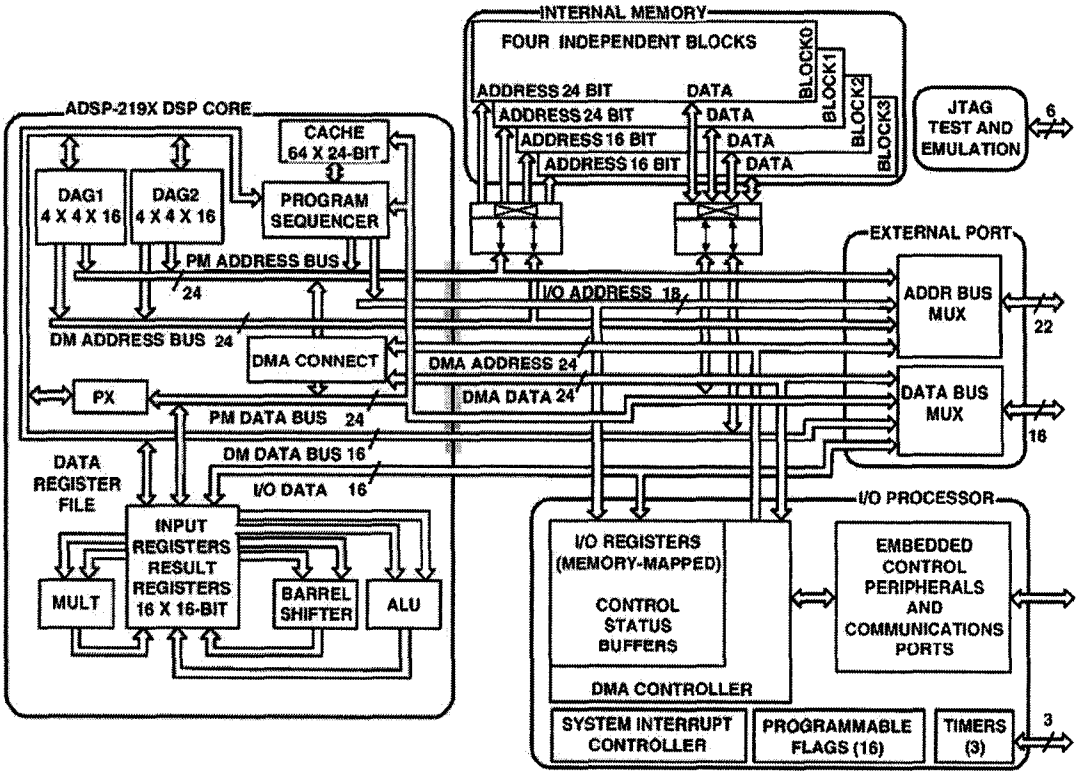


Figure 4.5 ADSP-21992 Block Diagram

The ADSP-21992 mixed signal DSP core integrates the 160 MIPS, fixed point ADSP-219x family base architecture with a complete set of embedded control peripherals such as ADC ports, a DMA controller, three programmable timers, on-chip program and data memory spaces. The architecture of the embedded ADSP-21992 is shown in Figure 4.5[3]. The program memory

(PM) bus, data memory (DM) bus and directly memory accessing (DMA) bus make the DSP operated more efficiency. During a single cycle, these buses let the processor access two data operands (one from PM and one from DM), access an instruction and write up to three values back to the register file. The DSP core architecture includes:

6.25 ns instruction cycle time (internal), for up to 160 MIPS sustained performance.
ADSP-218x family code compatible with the same easy to use algebraic syntax.
Single cycle instruction execution.
Up to 1M words of addressable memory space with 24 bits of addressing width.
Dual purposes program memory for both instruction and data storage.
Fully transparent instruction cache allows dual operand fetches in every instruction cycle.
Unified memory space permits flexible address generation, using two independent DAG units.
Independent ALU, multiplier/accumulator, and barrel shifter computational units with dual 40-bit accumulators.
Single cycle context switch between two sets of computational and DAG registers.
Pipelined architecture supports efficient code execution at speeds up to 160 MIPS.
Register file computations with all non-conditional, nonparallel computational instructions.
Power program sequencer provides zero overhead looping and conditional instruction execution.
Architectural enhancements for compiled C code efficiency.
Architecture enhancements beyond ADSP-218x family are supported with instruction set extensions for added registers, ports, and peripherals.

The clock generator module generates two output clocks: the DSP core clock, CCLK; and the peripheral clock, HCLK. The clock values of CCLK can be up to 160MHZ, and HCLK can be up to 80MHz at the 160MHz CCLK rate.

At any time the ADSP-21992 core can respond up to seventeen interrupts and the priority of the 12 user defined interrupts is determined by the programmers.

4.3.2 Memory Access

The memory structure of ADSP-21992 includes internal on-chip memory, external off-chip memory, I/O off-chip memory and off-chip boot memory and is shown in Figure 4.6[3].

The program and data memory spaces are accessible through 24-bit PMA (Program memory address) and DMA (Data memory address) address buses.

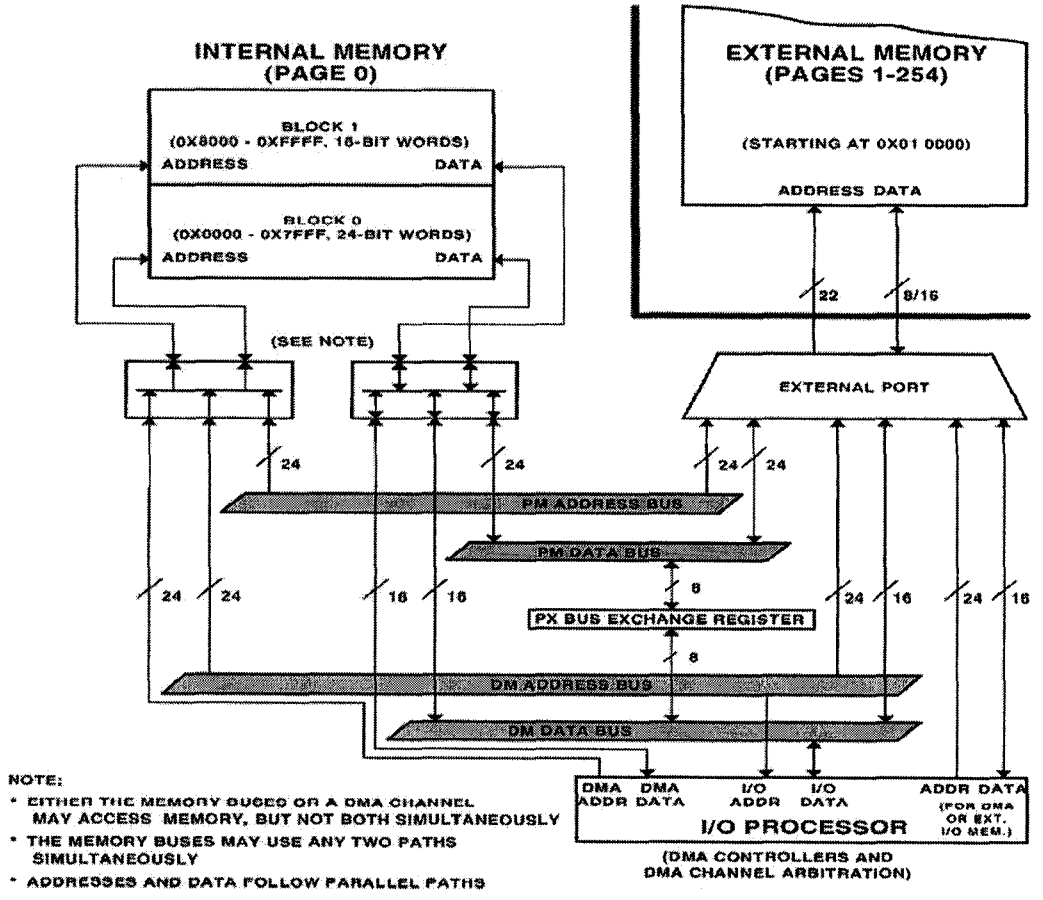


Figure 4.6 ADSP-21992 Memory structure

The I/O memory is an additional external memory, which consists 256 pages and each page contains 1024 addresses. The I/O memory is designed to support simple connections to

peripherals (such as data converters and externals registers) or to bus interface ASIC data registers. The first 32 pages (32K addresses) are reserved for on-chip peripherals and remained 224 pages (224K addresses) are available for external peripheral devices. The Visual DSP provides instruction set to access I/O memory.

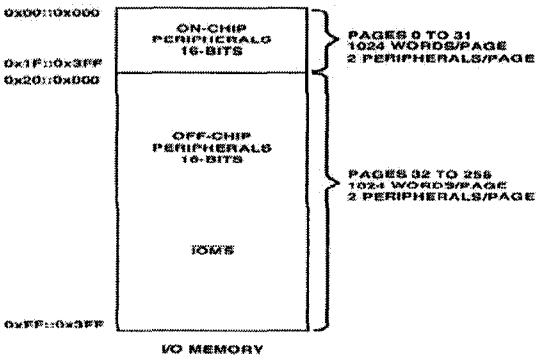


Figure 4.7 I/O Memory Map

During the control software development, the on-chip peripherals control registers such as the PWM generation control registers and ADC converter control registers are arranged in I/O memory first 32 pages.

4.3.3 DSP peripherals Architecture

The ADSP-21992 contains following embedded control peripherals shown in Figure 4.8[3]:

One 8-channel, 14-bit analog to digital converter system.
One 3-phase, 16-bit, center based PWM generation unit.
Two adjustable frequency auxiliary PWM output.
One 16-bit digital I/O.
One 16-bit watchdog timer.

Three general-purpose timers.
One controller area network (CAN) module.
One DSP serial Port (SPORT).
One serial peripheral interface (SPI) port.

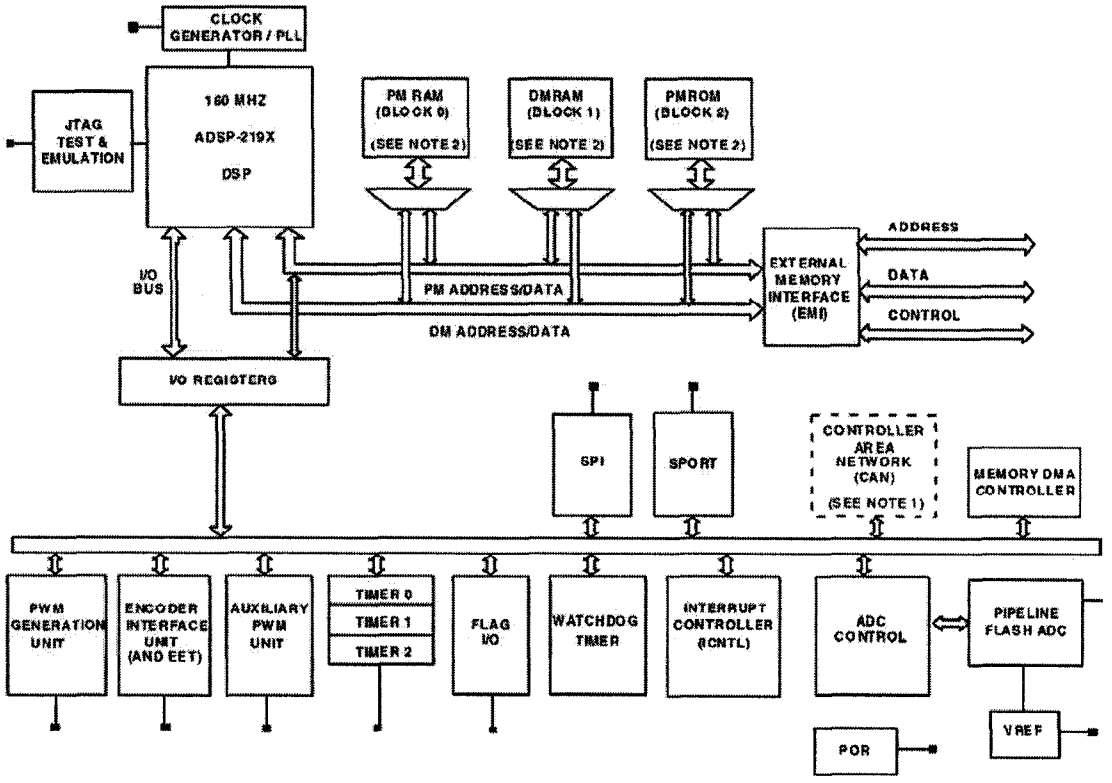


Figure 4.8 ADSP-21992 Functional Block Diagram

For the details please refer to the ADSP-21992 hardware reference data sheet [21].

4.4 ADSP-21992 EZ-KIT Lite Evaluation System

The ADSP-21992 EZ-KIT lite evaluation system includes an evaluation board and VisualDSP++ software. The evaluation board is designed to be compatible with the VisualDSP++ code development environment to test the capabilities of the ADSP-21992 fixed-

point, mixed-signal, digital signal processor (DSP). Via the expansion connectors, the ADSP-21992 can communicate with designed peripherals. The DSP evaluation board includes follow attributes:

Analog device ADSP-21992 160 MHz mixed-signal DSP.
USB debugging interface
Analog input circuitry.
8-channel 2-bit DAC (AD5328BRU) on SPI interfaces.
PWM output interface.
External memory interface.
Encoder interface circuitry.
General-purpose I/O interface.
UART interface (RS-232).
CAN interface circuitry.
Flash memory 512Kx8.
External SRAM 64Kx16.
14-pin emulator connector for JTAG interfaces.

4.4.1 Hardware description

The layout of the DSP evaluation board is shown in Figure 4.9. The DSP board is powered up using ±5V DC voltage supply on the connector P1. The control software can be downloaded from the PC to the DSP evaluation board through the USB connector P11. The PWM control signals are obtained at the output from the PWM, AUXPWM, Timer interface via connector P10. Analog input signals fed into the DSP board through the analog input connector P4. The outputs of the SPI DAC are brought out to the DAC output connector P5. The positions of all the connectors are also shown in Figure 4.9[21].

The DSP core voltage is 2.5V, and the external interface operates at 3.3V. These power supplies are provided by linear regulators supplied from the +5V source. The DSP evaluation board has three power supply inputs: VDD, +AVDD and –AVDD. For correct operation, the link JP1 between AGND and DGND must not be removed.

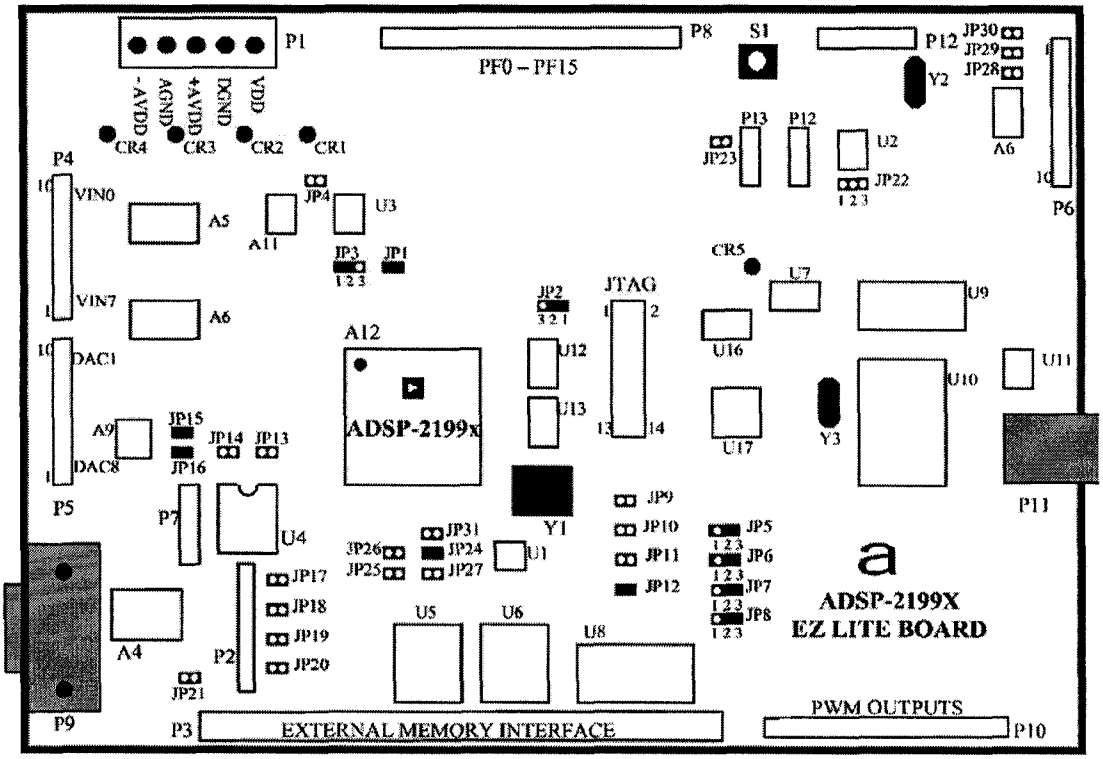


Figure 4.9. ADSP-21992 EZ-KIT Lite Board Layout

The DSP board is configured by a set of jumpers. Before starting to use the DSP board, the position of the jumpers must conform to the default configuration.

JP1 closed to link the analog and digital ground planes.
JP2 closed at 1-2 position to set the DSP board can be reset from pushbutton switch (S1), or external power-on reset IC (ADM708), or USB interface circuitry on the DSP board.
JP3 closed at 1-2 position and JP4 open to select the internal voltage reference for the ADC port.
JP5 is closed at 2-3 position to enable the PWM output and let the /PWMTRIP pin to be defined by the external circuitry.
JP6 closed at 2-3 position to disable the PWM switched reluctance mode.
JP7 closed at 2-3 position to enable the active HI PWM output.
JP8 closed at 2-3 position to enable the AUXPWM outputs.
JP12 closed to select the BYPASS boot mode.
JP15 closed to select the DAC as the SPI slave.
JP16 closed to select PF3 pin to update the DAC register.
JP24 closed to map the external SRAM to /MS0.

The detailed connections to the DSP board in the experimental setup are described in chapter 5. The detailed schematic of the ADSP-21992 board is attached at appendix B for completeness

4.4.2 VisualDSP++ software

VisualDSP++ software development and debug tools include C/C++ compiler, runtime library with over 100 math, DSP, and C runtime library routines, assembler, linker, loader, simulator, emulator and splitter.

The C/C++ compiler is designed to process ISO/ANSI standard C and C++ source files, produce machine level version of the source code and object files, provide re-locatable data and debugging information, provide relocatable data and program memory segments for placement by the linker in the processors' memory. A number of C language extension library developed by Analog Devices are also included to help the customer to develop the DSP application.

The VisualDSP++ has provided three tools to help the software developer to debug the code. The simulator is a kind of software that mimics the behavior of a DSP chip and is used to test and debug the DSP code. The simulator can be run without hardware. The evaluation system can enable the user to monitor DSP behavior by connecting the ADSP-21992 EZ-Kit Lite board to the PC via a USB connector. No power electronics hardware required at this stage. In emulation system the control target (power electronics board) is connected and application software to be debugged in real system. Emulator software performs the communications that enable the user to see how your DSP code affects the DSP performance. The control software can be debugged first using the simulator and evaluator. When the software is confirmed to work

properly, the user can go to the emulation stage to perform the real time control and to check the results.

In the visualDSP++ environment, program development consists of the following steps: create a project, configure project options, add and edit project source files, define project build options, build a debug version (executable file) of the project, create a debug session and load the executable file, run and debug the program, build a release version of the project. These steps can help to reduces the code development time and make the project consistent, accurate and with less project management.

For the process for installing the VisualDSP++ the user can refer to VisualDSP++ 3.0 user's guide for ADSp-21xx DSPs [22], VisualDSP++ 3.0 getting started guide for ADSP-21xx DSPs [23] and VisualDSP++ 3.0 C/C++ compiler and library manual for ADSP-219x DSPs [24].

Chapter 5 Experimental Setup Guidelines & Problems

The experimental DSP controlled single-phase IGBT rectifier system used to verify the proposed new current control scheme, see chapter 3, includes the ADSP-21992 EZ-KIT Lite board, power electronics board (include IGBT switches and relative drives), signal sampling (feedback) circuit and DSP output control signals isolation circuit. A personal computer (PC) was also used to develop the control software and download the source code to the ADSP-21992 EZ-KIT Lite DSP board to perform the function of the proposed PWM current controller. Each part of this experimental system is described in this chapter.

5.1 System hardware description

The experimental operation of the new hybrid current controller was tested using a DSP controlled single-phase IGBT rectifier test system. This system controls the single-phase IGBT rectifier in real time. Figure 5.1 gives a block diagram overview of the experimental system. The whole system includes a personal computer, ADSP-21992 EZ-KIT Lite board, optocoupler board (DSP output control signals isolation circuit), signal sampling board (feedback signal sampling and scaling circuit), power electronics board (IGBT bridge and relative drivers). An isolation transformer is also included in the system to avoid internal electrical short circuits during measurements. The power electronics board, signal sampling board and optocoupler board are built in the lab and the detail description are given in the following sections.

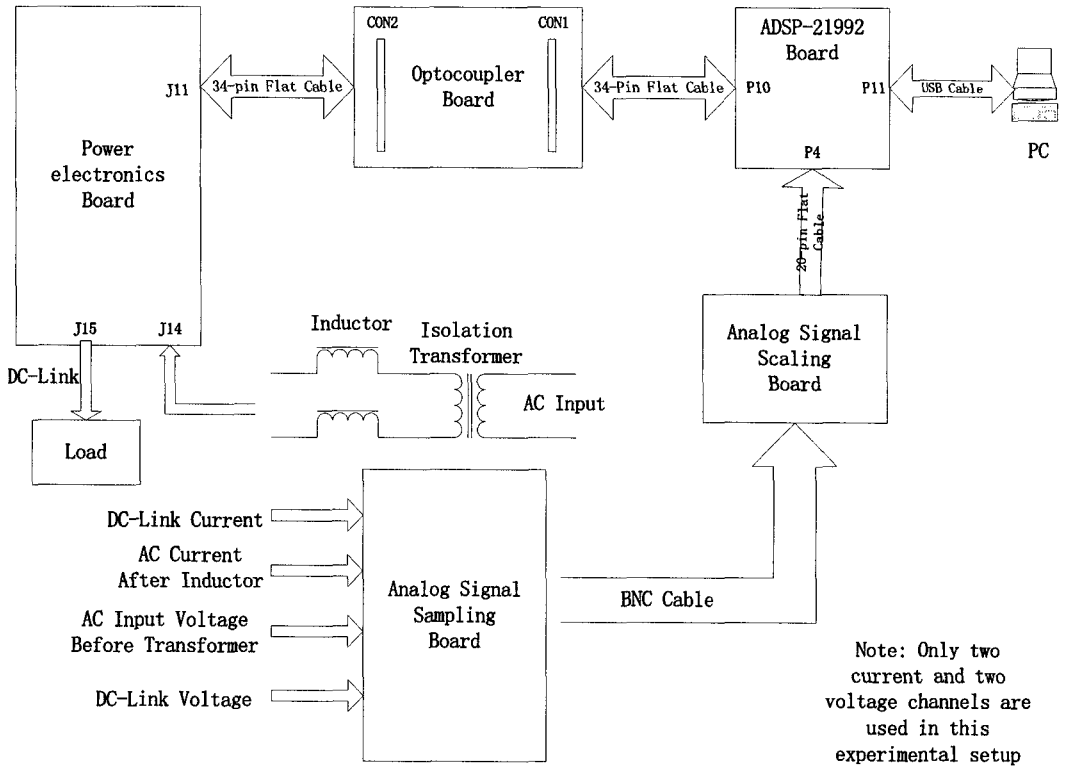


Figure 5.1 Layout of Experimental Setup

The components used in this experimental setup are also list in Table 5.1.

Isolation transformer	Single-phase VARIAC autotransformer
Power electronics board	Load box
ADSP-21992 EZ-KIT Lite evaluation board	±5V DC power supply
Signal sampling box	Optocoupler isolation box
34-pin flat cable connectors	Signal scaling box
BNC cables with ends	Banana cables
Tektronix TDS420 oscilloscope	Fluke 39 power meter
Brunelle digital multimeters	Personal computer

Table 5.1 Components list

Sections of the experimental system were tested for functionality and the relevant test results obtained are included in those sections when these parts are described. The detailed pin arrangements for the various connectors shown in Figure 5.1 are included in the relevant sections in this chapter.

Electrical noise interference on various signals in the test setup was a particular concern. If ignored, it can dramatically affect the test result and sometimes can cause the power electronics circuit trip on a fault. The electrical noises existing in the signals may also possible to be transferred to ADSP-21992 board through the long cables and cause the DSP controller to work improperly. In order to minimize the associated interference, the equipment layout was carefully arranged during the experimental setup. All the test equipment was put as near as possible to shorten the length of the cables. For instance, USB cable shipped together with ADSP-21992 EZ-KIT Lite evaluation board can not be used because of its excessive length. Ground loops can cause the electrical noise, so every circuit should have one and only one ground used and any ground loop should be avoided.

5.2 ADSP-21992 EZ-KIT Lite evaluation board

The ADSP-21992 ADSP-21992 EZ-KIT Lite evaluation board is the heart of the experimental setup. It is designed to be used in conjunction with the VisualDSP++ development environment to perform advanced application code development and debug task. The evaluation board uses the connectors to communicate with other peripheral circuits. These connectors are analog input connector P4, PWM, AUXPWM connector P10, USB connector P11 and power supply P1.

The DSP evaluation board has three power inputs: VDD, +AVDD and –AVDD. For correct operation, these power supplies are required to meet the following requirement: VDD +5V, 800mA; +AVDD +5V, 60mA, -AVDD –5V, 60mA. The pin arrangement of the power supply connector P1 is shown in Figure 5.2[21].

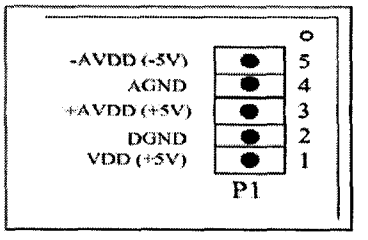


Figure 5.2 Power supply connector P1

Analog input signals to the DSP evaluation board are supplied at the analog input connector P4. The ADSP-21992 has 8 ADC input channels labeled from VIN0 to VIN7. Nominally the analog input signals should sit in the range –1V and +1V. The pin arrangement of analog input connector P4 is shown in Table 5.2.

Pins	Name	Signal
1	AGND	Analog ground
2	VIN0	Analog input channel 0
3	VIN1	Analog input channel 1
4	VIN2	Analog input channel 2
5	VIN3	Analog input channel 3
6	VIN4	Analog input channel 4
7	VIN5	Analog input channel 5
8	VIN6	Analog input channel 6
9	VIN7	Analog input channel 7
10	AGND	Receive clock

Table 5.2 Analog input connector P4

The connector P10 outputs the 6 PWM, 2 AUXPWM control signals and 3 general-purpose timer signals from the DSP board and inputs two error signals to the DSP to shut down the PWM and AUXPWM output. The pin arrangement of the PWM output connector P10 is shown in the Table 5.3.

Pin	Name	Signal
1	AH	PWM channel A high output
2	AL	PWM channel A low output
3	BH	PWM channel B high output
4	BL	PWM channel B low output
5	CH	PWM channel C high output
6	CL	PWM channel C low output
7	PWMTRIP	PWM trip input
8	PWMSYNC	PWM synchronization signal
9	DGND	Digital ground
10	AUX0	Auxiliary PWM output
11	AUX1	Auxiliary PWM output
12	DGND	Digital ground
13	AUXTRIP	Auxiliary PWM trip input
14	TMR0	General-purpose timer I/O
15	TMR1	General-purpose timer I/O
16	TMR2	General-purpose timer I/O

Table 5.3 PWM connector P10

The DSP evaluation board is configured by using the jumpers. Before connecting the evaluation board to the system, the jumpers' positions on the DSP evaluation board were checked to conform the board is set up in the default configuration. The detail jumper setting is shown in Table 5.4.

Reference	Jumper Settings	Description
JP1	Closed	AGND / DGND ground link
JP2	1-2 position	Choice of reset
JP3	1-2 position	Internal/external Vref source
JP4	Open	Internal/external Vref source
JP5	1-2 position	Disable/enable PWMTRIP
JP6	1-2 position	PWM SR mode selection
JP7	1-2 position	PWM polarity selection
JP8	1-2 position	Disable/enable AUXTRIP
JP12	Closed	PLL BYPASS mode
JP15	Closed	SPI DAC select
JP16	Closed	SPI DAC select
JP24	Closed	External SRAM memory IC select

Table 5.4 DSP Board Jumper Default configurations

The DSP evaluation board contains ESD sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent

damage may occur in devices subjected to high-energy discharges. Proper ESD precautions to avoid the discharge of static electricity are strongly recommended to avoid performance degradation or loss of functionality.

5.3 Power electronics board

The IGBT power electronics board contains two sets of power electronics circuits and one DC supply. The schematic of the power electronics board is attached in appendix B. A simplified circuit diagram is shown in Figure 5.3[25]. The DC supply is designed to power up the power electronics board. Each power electronics circuit includes one three-phase IGBT module (CPV364M4U), associated drive (IR2133J) circuit, PWM signal input and AC, DC link connectors. The IGBT power electronics board is mounted on a heat sink in order to ensure good thermal contact between the CPV364M4U module substrate and the heat sink, the two CPV364M4U modules are also mounted on the heat sink.

The IGBT module CPV364M4U has six IGBT switches and each IGBT switch has a paralleled free-wheel diode. The CPV364M4U can be used as a three-phase rectifier or a three-phase inverter depends on the need. By disabling any one pair of IGBT switches through the control software, the CPV364M4U can also be used as single-phase rectifier or single-phase inverter. The main ratings of CPV364M4U are list below:

- Maximum collector-to-emitter voltage is 600V.
- Maximum continuous collector current of each IGBT is 20A.
- Maximum pulsed collector current is 60A.

During the experimental test, the tester should always keep these in mind to make sure the voltage and current remain below these maximum values.

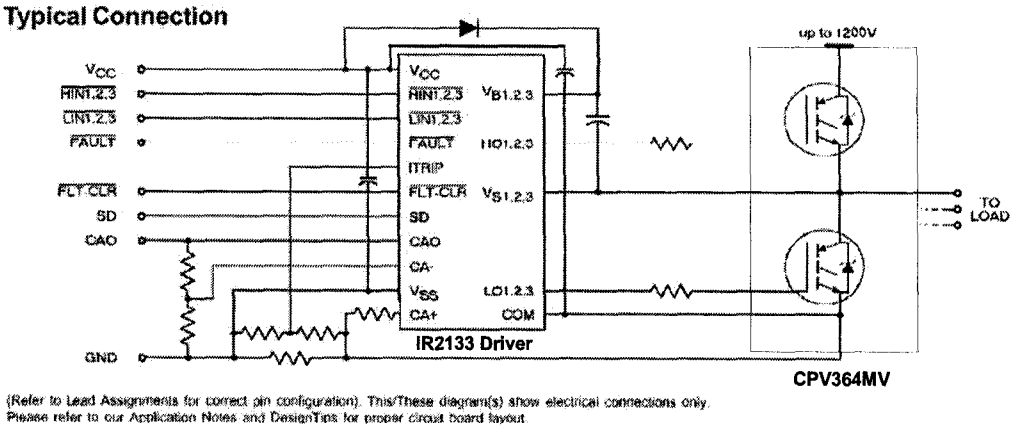


Figure 5.3 Simplified Circuit Diagram

The IR2133 are high voltage driver with three independent high side and low side referenced output channels for high-speed power MOSFET and IGBT circuit. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration, which operates up to 600V or 1200V. Through an external current sense resistor, the chip can provide an analog feedback of the inverter bridge dc-link current and voltage. A current trip function, which terminates all six outputs, can also be derived from this sense resistor. The open drain active low FAULT signal is provided to indicate that an over-current or under-voltage shutdown has occurred and the fault condition can be cleared by active low the FLT-CLR lead, see Figure 5.3.

The PWM control signals are input from the connector J11, see appendix B, and the J11 is connected to the optocoupler board CON2 connector through a 34-pin flat cable. The pin arrangement is shown in table 5.5.

Pin	Name	Signal
1	+5V_a	+5V power supply output
2	+15V_a	+15V power supply output
3	GND_a	Ground
4	IN1_a	PWM control signal AH
5	IN2_a	PWM control signal AL
6	IN3_a	PWM control signal BH

7	IN4_a	PWM control signal BL
8	IN5_a	PWM control signal CH
9	IN6_a	PWM control signal CL
10	Fault_a	Circuit error signal
11	N/A	
12	IFB_a	DC link current feedback
13	VFB_a	DC link voltage feedback
14	RESET_a	Circuit reset signal
15	STOP_a	Circuit stop signal
16	N/A	

Table 5.5 Power electronics control signal input connector J11

The power electronics board was carefully checked before use because it works under the high voltage and current. Before the electrical test, a visual check had been done to check if the power electronics board has any broken or burned damages, and if the IGBT module CPV364M4U has been mounted tightly on the heat sink. After that the power electronics board was powered up, it was checked for ±15V and +5V DC power supply. And then input a 2 kHz to 20 kHz square waveforms at PWM signal input pin and checked the waveform at IR2133 output to make sure the driver circuit worked properly. After passed this test, started to test the IGBT bridges. A VARIAC transformer, a series inductor and a diode rectifier were used. To verify the free-wheel diodes low AC voltage was applied to IGBT bridge A, B (and A, C and B, C) terminals and the DC-link voltage was measured to see if the $Vdc \geq \sqrt{2} * Vac$.

5.4 DSP output isolation Circuit

The PWM signals from DSP output pins are delivered to the power electronics control input pins using opto-coupler isolation circuit. This isolation avoids electrical short circuit and also can help to minimize the effects of noise to the DSP and digital circuit. A circuit diagram for the isolation of the signals AH and AL are shown in Figure 5.4. The circuit schematic is attached in the appendix B for detail reference.

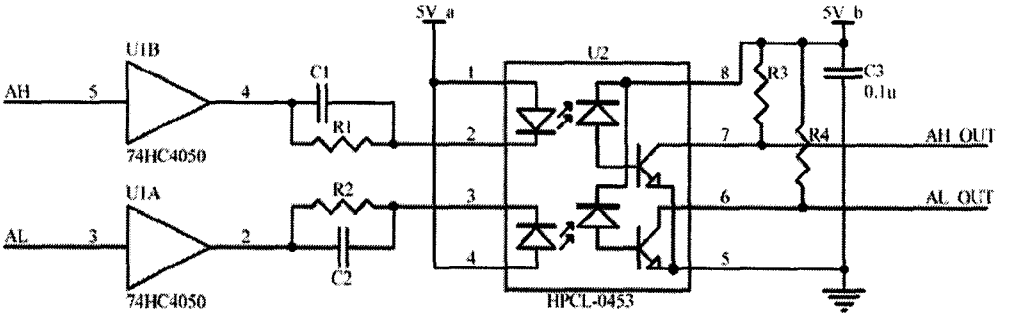


Figure 5.4 Optocoupler Circuit Block Diagram

An experimental test had been done to measure the delay time between the signal input and output. The suitable components' values were selected to control the delay time to be less than 1.5us.

To avoid any possible internal electrical connection between the digital control circuit and power electronics circuit the 5V_a and 5V-b, see Figure 5.4, are isolated and supplied separately from DSP board and power electronics board.

A manual start/stop and reset control functions are included; see Figure 5.5, which can let the experimental tester control the power electronics board easily and directly. Two red LEDs are used to indicate the working status of power electronics board, see Figure 5.5. These lights are turned on under the follow logic conditions:

- The power electronics circuit is stopped.
- An error occurs.
- The power electronics circuit needs to be reset.

The whole circuit is put in a metal box and can be connected to DSP board and power electronics board through two double-row 34-pin flat cable connectors. The detail panel layout is shown in Figure 5.5.

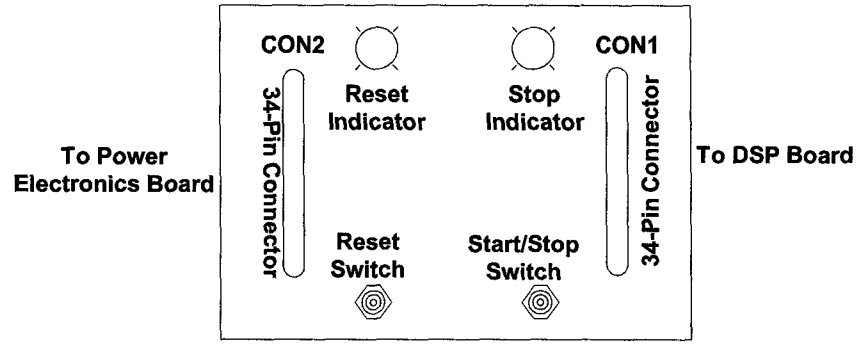


Figure 5.5 Optocoupler Box Panel Layout

The isolation box has two ribbon cable connectors (CON1, CON2); one start/stop control output channel and one fault feedback channel. The detailed pin arrangements for each connector are listed in Table 5.6 and 5.7.

Pin	Name	Signal
1	AH	PWM control signal AH
2	AL	PWM control signal AL
3	BH	PWM control signal BH
4	BL	PWM control signal BL
5	CH	PWM control signal CH
6	CL	PWM control signal CL
7	PWMTRIP	error signal to stop PWM output
8	N/A	N/A
9	GND	Ground
10	N/A	N/A
11	N/A	N/A
12	N/A	N/A
13	N/A	N/A
14	N/A	N/A
15	N/A	N/A
16	N/A	N/A
17	+5V	+5V power supply input

Table 5.6 CON1 pin arrangement

Pin	Name	Signal
1	+5V	+5V power supply input
2	N/A	N/A
3	GND	Ground
4	AH	PWM control signal AH
5	AL	PWM control signal AL
6	BH	PWM control signal BH
7	BL	PWM control signal BL
8	CH	PWM control signal CH

9	CL	PWM control signal CL
10	Fault	Circuit error signal
11	N/A	
12	N/A	N/A
13	N/A	N/A
14	RESET	Circuit reset signal
15	STOP	Circuit stop signal
16	N/A	

Table 5.7 CON2 pin arrangement

The most important parameter of the optocoupler circuit is its internal signal delay. In this experimental test, the signal delay from the input to output was less than 1.5us. A 2kHz to 20kHz square waveform test signals were applied to the optocoupler box input pin and a oscilloscope was used to record the waveforms at the optocoupler box input and output pins. The oscilloscope's cursor function was used to measure the response time. The experimental test results are shown in Figure 5.6.

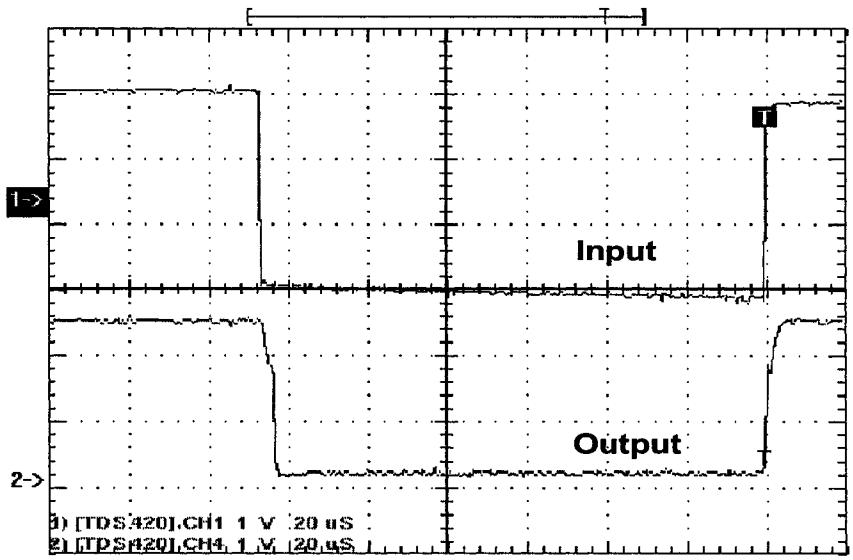


Figure 5.6 Experimental test result for the optocoupler board delay time

The reset and start function were also tested. For the Reset function, when the reset button is pressed, an active low signal should be output from the optocoupler box "RESET" pin.

For the start/stop function, the logic output from the optocoupler box "STOP" pin should change from low to high when the switch is turned from start position to stop position.

5.5 Signal sampling and scaling circuit

As the ADSP-21992 mixed signal DSP controller analog to digital conversion system input voltage range is 2V peak to peak, the feed back signals need to be scaled into this range. A signal sampling and scaling circuit is designed for this task. The signal feedback includes three voltage and three current channels, which can permit the DSP to receive up to six feedback signals at the same time.

The signal sampling circuit is put into one big metal box and signal-scaling circuit is put into another small metal box. As the output terminals use BNC connectors, the signal-sampling box can also be used as scope's inputs. It makes the experimental test measurement very convenient, simple and safe. The voltage input has two conversion ratios: 25:1 and 50:1, which can be selected by a switch. In the current conversion circuit, the current transducers are used. The output range of the current transducers is ±15V/±50A and the maximum input current is 50Arms. When the system was setup, the polarities of the applied feedback signals were checked to make sure they are the same.

As the signal-sampling box's maximum voltage convert ratio is 50:1, if the input peak to peak voltage exceeds 100V, the output feedback signal's peak-to-peak voltage will exceed 2V and can not be used directly by ADSP-21992. A signal scaling circuit is designed to help to solve this problem. The simple diagram of this circuit is shown in Figure 5.7. The scale factor is 5:1 and the circuit output is pulled down to -5V DC through a 100k resistor. This is helpful to make sure the center of the output scaling signal to the ADSP-21992 DSP ADC port will be at +1V.

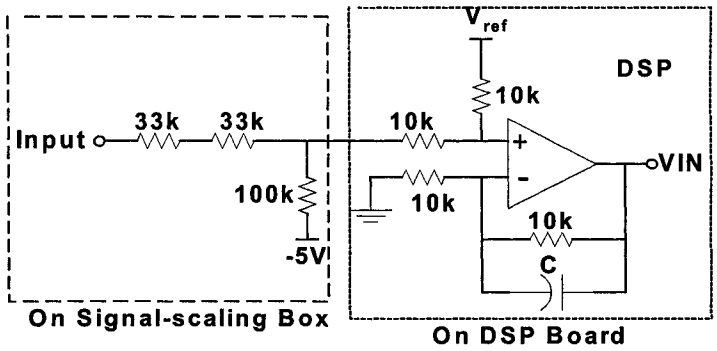


Figure 5.7 Signal Scaling Circuit

The signal-sampling box voltage feedback circuit has two converter ratios: 25:1 and 50:1 and they can be selected by changing switches. Before signal-sampling box was connected to the system, ratio test, switches test and polarity test had been done to make sure the ratio and the polarities were correct and the switches functioned as expected. For the voltage input, the red terminals represent positive polarity and black ones represent negative polarity. For the current input, the white terminals represent positive polarity and the black ones represent the negative polarity.

The signal-scaling box was also tested to make sure the signals applied to DSP ADC port were centered at +1V.

5.6 Experimental test after setup

After the whole experimental system is set up, a low AC voltage was applied to power electronics board AC input terminals from a VARIAC transformer to start to test the IGBT switch. A single-phase unipolar hysteresis current control PWM program was written for this purpose, power up the DSP and power electronics board, download the PWM control program into the ADSP-21992 board, start the program and observe the waveform at AB (AC and BC)

terminals. If the waveform shown in Figure 5.8 and Figure 5.9 can be observed, it means the power electronics board is ready to go. For the details of the circuit please refer to the appendix schematic.

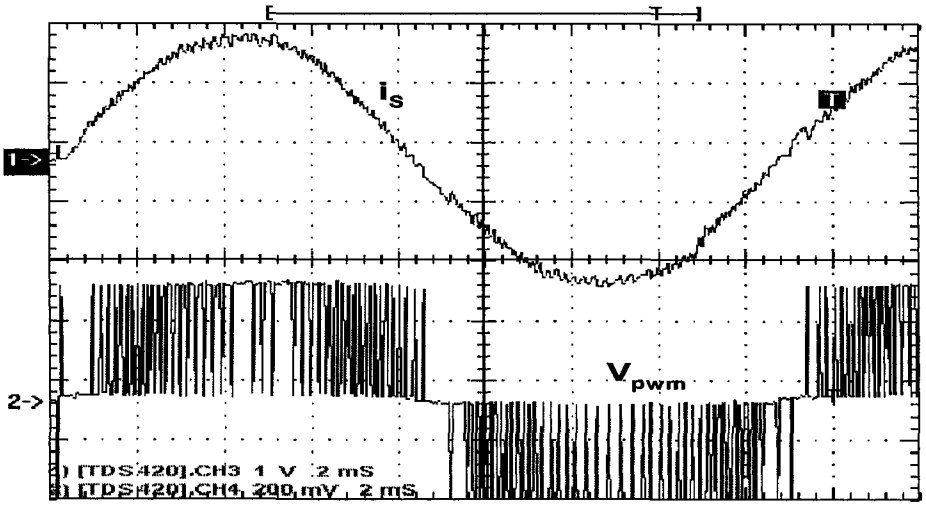


Figure 5.8 Unipolar hysteresis current control waveform (1)

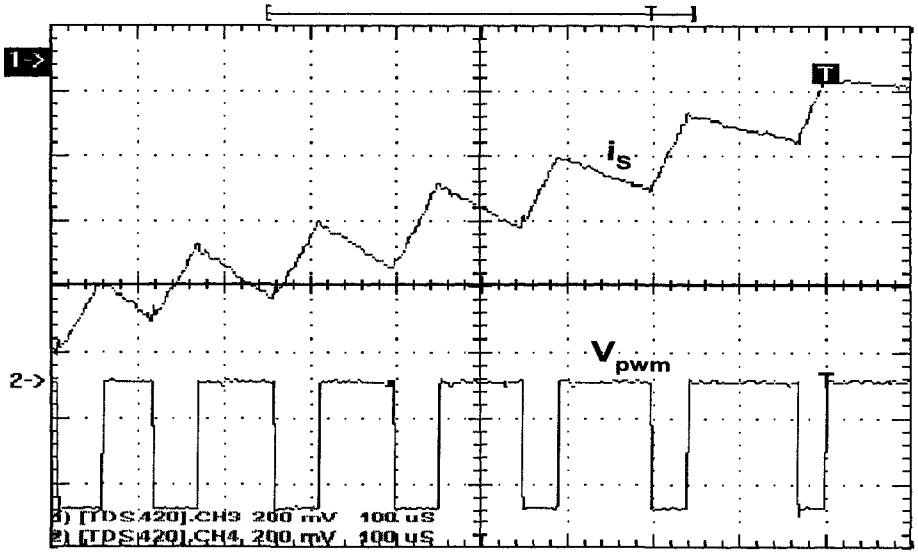


Figure 5.9 Unipolar hysteresis current control wavefore (2)

5.7 Summary

In this chapter an experimental setup for new current control scheme DSP application is described. The main parts of the experimental system include DSP evaluation board, power electronics board, signal feedback circuit and PWM output signals isolation circuit. The detail and the test procedures of each part are also given out.

The DSP evaluation board is designed to be used in conjunction with the VisualDSP++ development environment to perform advanced application code development and debug task. The board setup configuration should be check before use.

The signal isolation circuit is used to avoid the DSP board damage caused by any undesired surges or failures occurred in the power electronics circuit.

The signal feedback circuit is designed to sample the feedback signals from rectifier circuit and apply them to DSP ADC port.

Chapter 6 DSP Software Development

The PWM current control scheme presented in this thesis is verified by using DSP controller ADSP-21992 together with a single-phase IGBT rectifier and relevant signal sampling and isolation circuit. The experimental system setup is described in chapter 5. The DSP control software development described here implements the proposed PWM current control scheme. Details are given on how the ADC signal sampling is achieved, PWM signal generation and program initiation. The DSP control program is developed using C language software.

6.1 General description

The control program is an interrupt-oriented program because the ADC data sampling and PWM signal generation are controlled by the interrupt signals. The diagram of the program flow is shown in Figure 6.4.

The software program starts using a DSP controller initialization process. During this process the program writes predefined values to set the PLL clock, interrupt priority, sets the PWM generator and ADC converters to the desired working modes. The program sample is shown below:

```
sysreg_write(sysreg_IOPG,Clock_and_System_Control_Page);
temp=io_space_read(PLLCTL);
temp=temp|0x0100;                          /*bypass PLLCTL*/
io_space_write(PLLCTL,temp);
io_space_write(PLLCTL,0x0B50);
for (i=0;i<512;i++) j++;
io_space_write(PLLCTL,0xA50);        /*configure PLLCTL,
                                     HCLK=CCLK/2,CLKOUT=HCLK*/
```

The 0x0A50 in PLL control register means:

- The peripheral clock HCLK is equal one half the DSP core clock rate.
- The CLKOUT pin is enabled.
- The DSP core frequency is 160MHz.

After initialization, the program goes through an infinite loop to wait for interrupts to occur. Two basic interrupt routines are defined. They are the "PWM trip interrupt routine" and the "PWM generating interrupt routine". The "PWM trip interrupt routine" has higher priority than the "PWM generating interrupt routine" because of the safety issue. It is used to terminate the control program when an error occurrs in the power electronics circuit to protect the DSP and power electronics circuit.

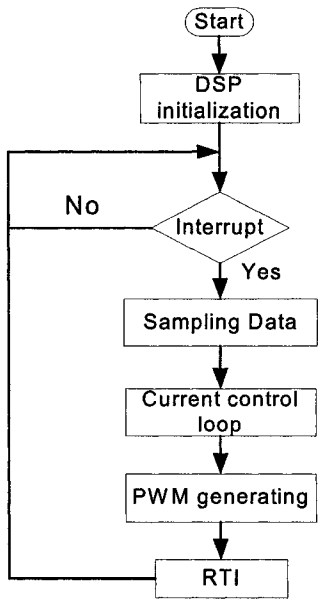


Figure 6.1 Flow chart of the Control program

The PWM generating interrupts are synchronized to the PWM synchronization pulse PWMYNC. During the PWM generating interrupt the DSP reads the feedback signals from the ADC port, calculates the current error, calculates the magnitude of the m_a modulated carrier signals, compares the current error with the m_a modulated carrier signals to obtain the duty cycle

values of the PWM switching signals, updates the PWM duty cycle control register and returns from the interrupt to wait for the next interrupt to happen.

The program details are described in the following section.

6.2 PWM generation unit

In the ADSP-21992 the duty cycle of the PWM signals are controlled by three 16-bit read/write duty-cycle control registers (PWMCHA, PWMCHB, PWMCHC). The two's complement integer value in the control register PWMCHA controls the duty cycle of the signals on AH, AL. Similarly for the PWMCHB and PWMCHC. The duty cycle control register range is from $(-\frac{PWM\_SAMP\_TM}{2} - PWMDT)$ to $(\frac{PWM\_SAMP\_TM}{2} + PWMDT)$. The PWM_SAMP_TM here mentioned is different from the PWM period. The PWM period is determined by the carrier frequency. The PWM_SAMP_TM is determined by data-sampling rate. The $(-\frac{PWM\_SAMP\_TM}{2} - PWMDT)$ here represent the 0% duty cycle (FULL OFF), the 0 in PWM duty cycle control register represent 50% PWM duty and $(\frac{PWM\_SAMP\_TM}{2} + PWMDT)$ represents 100% PWM duty cycle (FULL ON).

In normal modulation the duty cycle of the PWM signals vary from 0% to 100% between successive PWMSYNC pulses. In the proposed current controller implementation, the PWM registers only have two values, which represent FULL ON and FULL OFF. Figure 6.2 is shown the PWM waveforms transition from normal modulation to FULL ON and FULL OFF. How the dead time is added to the waveform is also shown in that Figure[3].

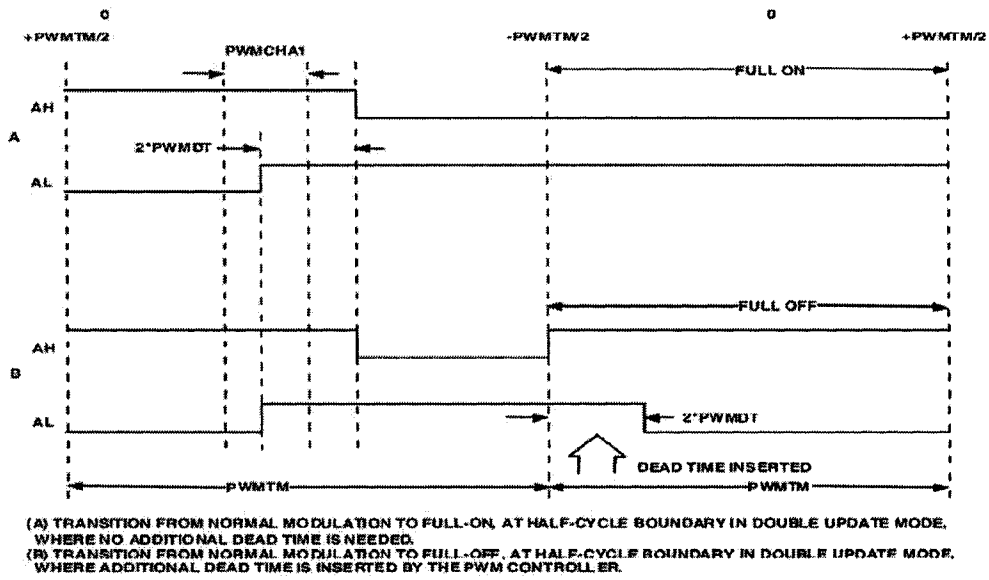


Figure 6.2 PWM signals in FULL ON and FULL OFF

6.2.1 PWM signal generation program

The proposed current controller work in the following ways to generate the PWM switching signals and is shown in Figure 6.3: Set the carrier signal frequency to 2KHz (For example); set the data sampling rate to 80KHz (for example), then each carrier period contains 40 data sampling periods (PWM_SAMP_TM). As a unipolar PWM switching pattern is used, the PWM switching frequency is twice the carrier signal frequency and is 4KHz. That means every PWM period contains 20 PWM signal-sampling periods (PWM_SAMP_TM). When a PWM generation interrupt occurss, the DSP samples the current feedback value, then calculates the current error and compare with the carrier signal, if the current error is smaller that the carrier signal, a value that represents the FULL OFF is written to the PWM duty cycle register; if the current error is bigger than the carrier signal, a value that represents the FULL ON is written to the PWM duty cycle register. So the region from point B to C shown in Figure 6.2, represents the actual "on-time" in the PWM switching signal, it contains several data sampling period and in

each data sampling period the PWM keeps FULL ON. The value written to the duty cycle control register can be determined by using the formula (5.1). In that formula the f_{ck}=80MHz, f_{PWM}=data sampling rate.

The values of PWM_ON and PWM_OFF can be calculated by using following formulas:

$$PWM\_ON = (\frac{PWM\_SAMP\_TM}{2}) - PWM\_DT \qquad (6.1)$$

$$PWM\_OFF = (\frac{PWM\_SAMP\_TM}{2}) + PWM\_DT \qquad (6.2)$$

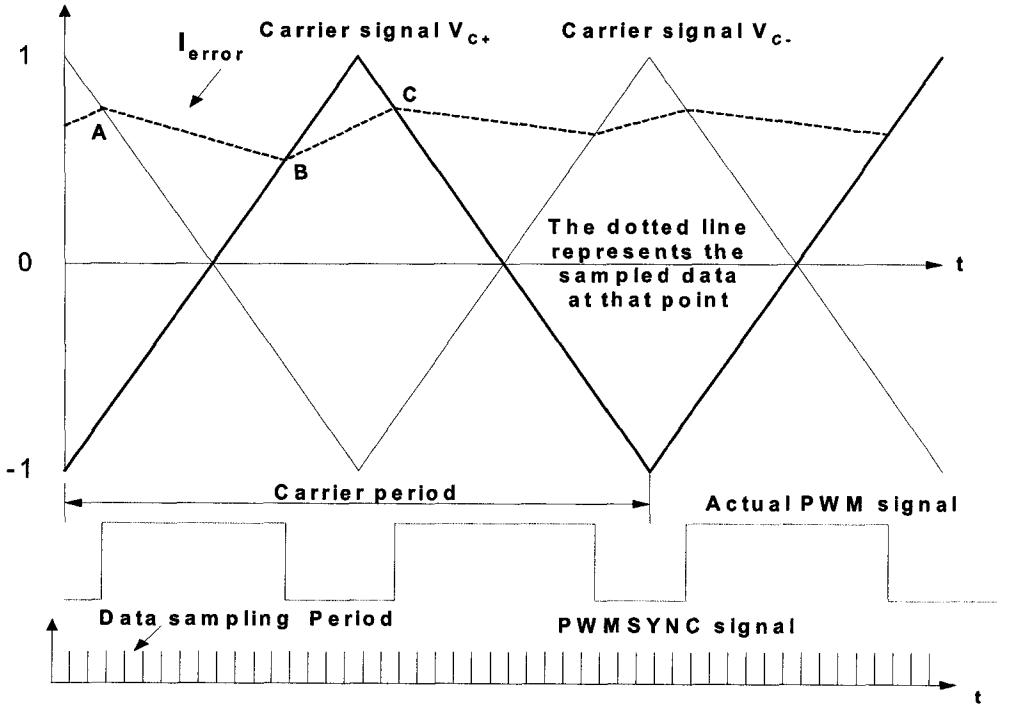


Figure 6.3 New current control diagram

The PWM_ON in formula (6.1) represents the value to control the switch FULL ON, and when the sampled current error is less than the carrier signal, this value will be written to the PWM duty cycle control register. The PWM_OFF in formula (6.2) represents the value to control the

switch FULL OFF, and when the sampled current error is higher than the carrier signal, this value will be written to the PWM duty cycle control register.

The carrier saw tooth signals are generated from the DSP and the values change step by step from +1 to –1. The step value can be determined by using the following formula:

$$STEP\_VALUE = \frac{4 \times f_{carrier}}{f_{sampling-rate}} \qquad (6.3)$$

For example, if carrier signal frequency $f_{carrier}$ is 2KHz, data sampling rate $f_{sampling\text{-}rate}$ is 40KHz, then the step value can be calculated as:

$$STEP\_VALUE = \frac{4 \times 2KHz}{40KHz} = 0.2$$

That means that in each data-sampling period, the magnitude of the saw tooth signal increases 0.2 until it reach 1 or decreases until reaches –1. In the proposed current control scheme, the carrier signals V_{C+} and V_{C-} are modulated by m_a.

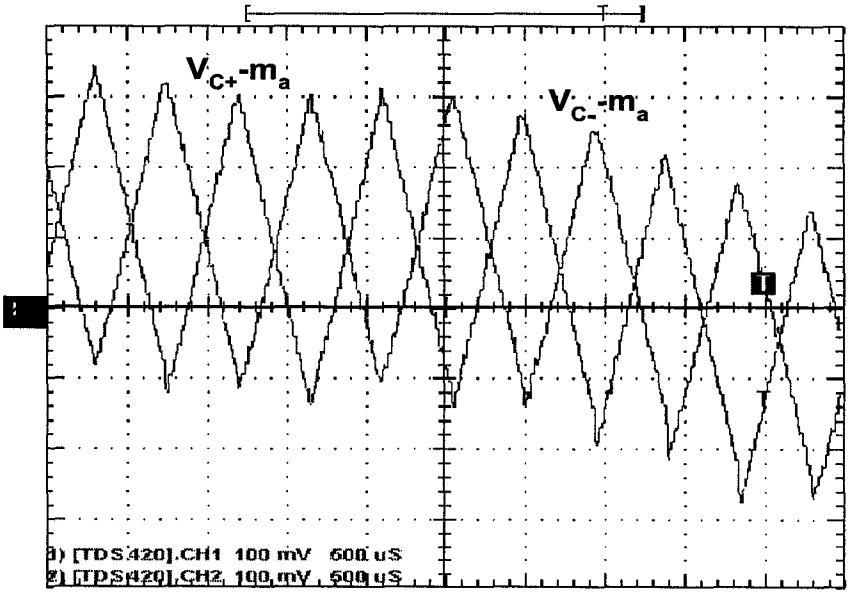


Figure 6.4 Carrier signal generated by DSP

The resultant analog waveforms representation of this process is shown in Figure 6.4. As the carrier signals V_{C+}-m_a and $V_{C-}$$m_a$ are generated inside the DSP, these waveforms were output to the DSP DAC port and recorded by a scope.

The PWM switching signals are generated by comparing the current error signal i_{error} with the modulated carrier signals. At the end of the PWM generation interrupt, the PWM duty cycle is determined: FULL_ON or FULL_OFF, the PWM duty cycle register is updated and then the program returns to the main routine to wait for the next interrupt. The following program performs this process:

```
sysreg_write(sysreg_IOPG,PWM0_Page);

io_space_write(PWM0_CHA,ma);      /* update PWM_CHA
io_space_write(PWM0_CHB,ma1);     /* update PWM_CHB

return;
```

6.2.2 PWM generator initialization

The PWM generate unit must be initialized before use it. Several registers need to be set by writing the user defined data such as the PWM period, dead time and PWM synchronization signal pulse wide. The detailed formulas for calculating PWM period and dead time had been given in chapter 4. The software use following command to update PWM period register, dead-time register and PWM synchronization signal width register:

```
sysreg_write(sysreg_IOPG, PWM0_Page);

io_space_write(PWM0_TM,PWM_Period);          /*PWM switching frequency is
                                             2kHz*/

io_space_write(PWM0_DT,PWM_DT);              /*set the dead time 2us*/

io_space_write(PWM0_SYNCWT,PWM_syncwidth);   /*set PWM synchronization signal
                                             width*/
```

As only four PWM output channels are used, the remaining two PWM output channels need to be disabled by setting the relevant bits in the PWM segment register. For example if the CH and CL channels need to be disable, the value 0x0003 is written to the PWM segment register.

*io_space_write(PWM0_SEG,0x0003); /*disable PWMC*/*

During the PWM generator initialization, bit PWM_EN and SYNC_EN in the PWM control register PWMCTRL need to be set to enable PWM generation PWMSYNC signal and continue interrupts. If the users want to use the double update mode to update the duty cycle twice per PWM period, the PWMDBL bit in PWMCTRL need to be set.

6.3 ADC data sampling program

The ADC converter in ADSP-21992 is fast and accurate. It has several conversion modes and can sample up to 8 analog inputs at same time. The User can set bit 4 to 6 in the ADC control register ADCCTRL to select these modes based on the number of the input signals. In this experimental test as only two feedback signals, the DMA dual-channel mode is selected. The data conversion can be trigged by four different trigger events. Bits 0 to 2 in the ADC control register ADCCTRL is used to select the trigger event and the rising edge of the internally derived PWM synchronization pulse PWMYNC is selected as the trigger event. The frequency of PWMSYNC is equal to the data-sampling rate mentioned in the last section.

The ADC data registers are 16-bit and the data format is left aligned 2's complement 14-bit word in the 16-bit field of the data registers. Bit 0 of the data registers may contain an OTR (Out of Range) bit depending on the state of the DATASEL bit of the ADCCTRL register. The OTR bit is cleared in this program to monitor if the input analog signals out of range.

The ADC clock also needs to be set in the ADCCLKSEL bits (bit 8 to 11) in the ADC control register ADCCTRL. A value of 0010 is written to ADCCLKSEL bits to select maximum ADC clock 20MHz in this program. All of above settings must be written to ADCCTRL in the program initialize process. The detail program is shown below:

```
void ADC_init()

{
        sysreg_write(sysreg_IOPG, ADC_Page);
        io_space_write(ADC_CTRL,0x0200);    //HCLK/4
}
```

During the PWM generating interrupt routine, the ADC converter is trigged to start converting the input analog signal to digital signals and the results are sent to the ADC data registers. The data stored in the ADC data registers can be read using the following commands by DSP controller:

```
sysreg_write(sysreg_IOPG, ADC_Page);
feedbackV=io_space_read(ADC_DATA4);      //obtain the current feedback
                                         from channel 4;
feedbackI=io_space_read(ADC_DATA0);      //obtain the voltage feedback
                                         from channel 0;
```

The ADC channel 0 and 4 are a pair of channels that the ADC port can sample the date simultaneous in the DMA Dual channel acquisition mode. Other pairs in this mode are channel 1 and 5, channel 2 and 6, channel 3 and 7.

The ADC digital output is 1.15 data format. It can represent the analog input voltage range ±1V: 0x7FFF equals +1V, 0x0000 equals 0V and 0x8000 equals –1V.

6.4 Summary

The detailed program development is described. The ADSP-21992 DSP controller, PWM generation unit and ADC converter port are used to perform the current control task. The control program is interrupt-oriented and the interrupts are controlled by the PWMSYNC signal pulses

(is same as the data sampling frequency). All the relevant units need to be initialized. In each signal-sampling period (PWM_SAMP_TM period), the switches are kept FULL_ON or FULL_OFF depend on the current control scheme. The actual frequency of the PWM switching signals is controlled by the carrier frequency. In next chapter the experiment result is given out to verify the control program.

Chapter 7 Experimental Result

The waveforms obtained from the experimental test circuit are presented in this chapter. These waveforms include two types of test results. One set of waveforms were obtained from the experiment hardware and used to demonstrate that every important part in the experimental setup was working properly. The details of the test methods are also described. Another set of waveform results demonstrates the operation of the DSP based proposed PWM current controller. These test were undertaken on a single-phase rectifier using a 5mH supply inductance and a 60Hz power supply. Analysis of the test results is also given.

7.1 Experimental hardware test

The Analog devices sample program was used to test the PWM generation unit and ADC port of ADSP-21992 EZ-KIT Lite board. The PWM signals generated by PWM generation unit were output to the connector P10. A channel by channel test had been done to make sure all six PWM channels work properly. The DSP ADC converter was also tested by applying a signal to each ADC channel. The DSP read that value and output to DAC port through connector P5. All the output signals are connected to a scope and the waveforms are recorded.

7.1.1 ADSP-21992 EZ-KIT Lite board test

Figure 7.1 shows the PWM output signals associated with the AH and AL channels. The AH and AL are a pair of PWM channels controlled by one PWM duty cycle control register. The

duty cycle of AH PWM channel is controlled by the value written to the PWM duty cycle control register and the duty cycle of AL PWM channel controlled by the complement integer value.

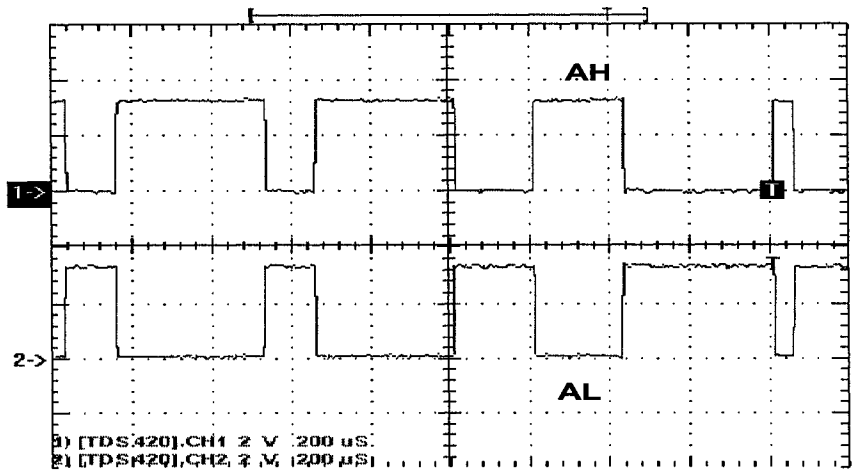


Figure 7.1 PWM switching signals in active low mode

The PWM signal dead time feature is added to permit the power switch being turned off to completely recover its block capability before the complementary switch is turned on. The expanded waveform is shown in Figure 7.2 and the dead time 2us is clearly displayed.

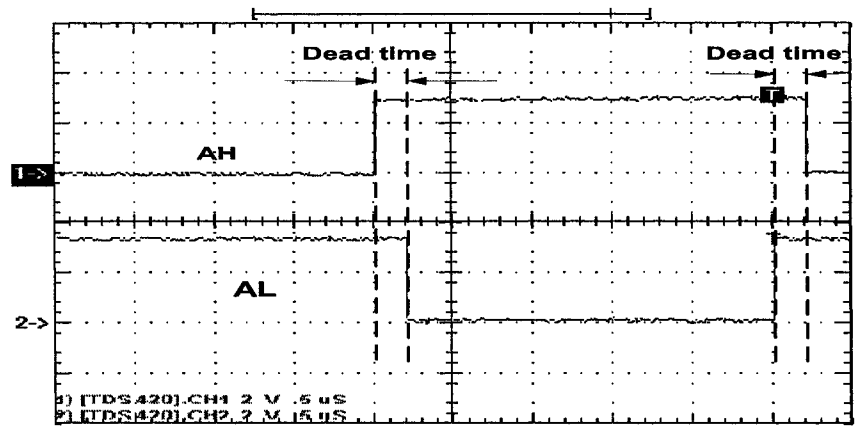


Figure 7.2 Detailed PWM control signals in active low mode

The PWM generator is capable of operating in two distinct modes, which are single update mode and double update mode. In single update mode the duty cycle values are programmable only once per PWM cycle and the PWM waveform are symmetrical to the mid-point of the PWM period, as illustrated by the PWMSYNC signal in Figure 7.3.

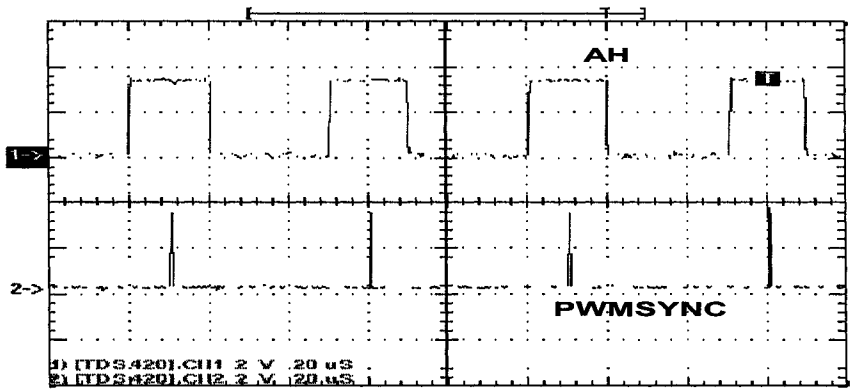


Figure 7.3 PWM waveforms in single update mode

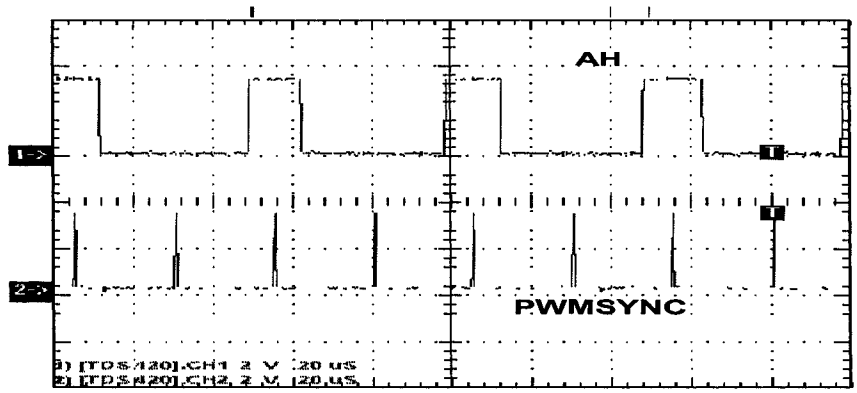


Figure 7.4 PWM waveforms in double update mode

In double update mode the duty cycle values are programmable twice per PWM period and the second update of the duty cycle register is implemented at the midpoint of the PWM period, as illustrated by the PWMSYNC signal. The PWM waveforms are asymmetrical to the mid-point of the PWM period and shown in Figure 7.4.

7.1.2 ADC converter test

A simple test program was written to test the ADSP-21992 ADC converter. The rectifier current feedback signal is applied to one of the ADC port and the test program read the data from the ADC port and output the waveform from the DAC port. The current waveforms before and after the PWM current controller was activated were different. It's a simple way to demonstrate the ADC port work properly. Figure 7.5 shows that the DSP controller can exactly sample the input analog signals and display them in DAC port.

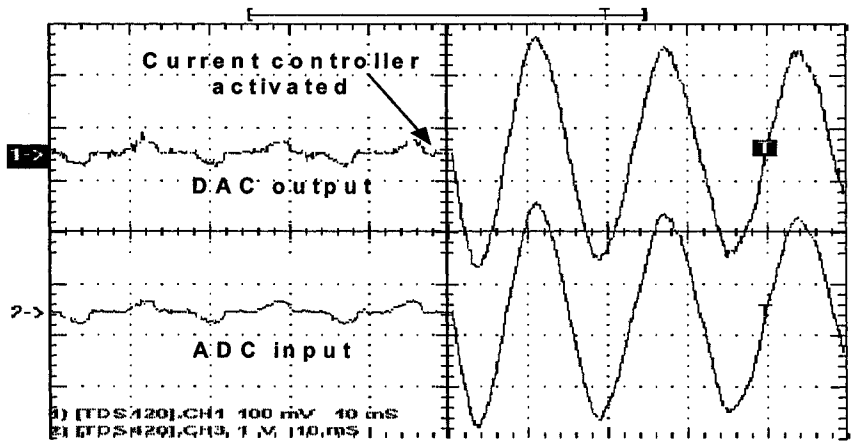


Figure 7.5 ADC –DAC test waveform

7.1.3 Isolation circuit test

Important test items in isolation circuit test include output delay time test and output signal voltage level test. The delay time between the input and output signals is measured to make sure the delay time in the accept range (say less than 2us). The Figure 7.6 and 7.7 shown the waveform recorded from the scope. The delay time is determined by the parameters of

isolation circuit. The circuit had been tested by adjust the values of R1 and C1 shown in Figure 4.4.

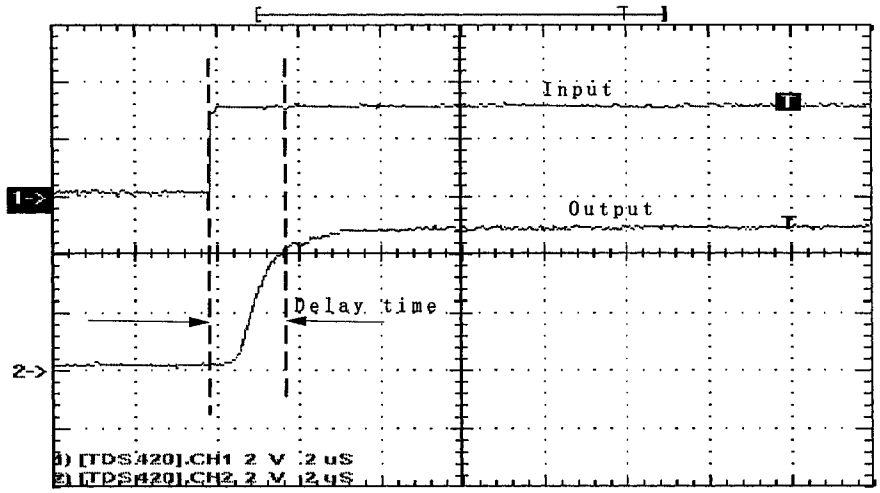


Figure 7.6 The isolation circuit delay time on a signal rising edge

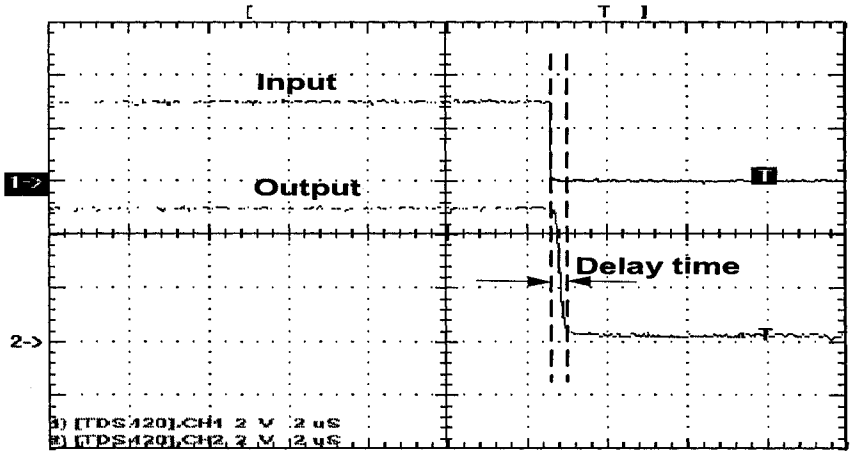


Figure 7.7 The isolation circuit delay time on a signal falling edge

The logic level test is to check the output signal waveform to make sure the voltage representing logic low in the output signal is below 0.1V. The value of R3 shown in Figure 4.4 had been adjusted in this test.

The delay time between the DSP PWM output and IGBT gate input were also measured. The waveforms are shown in Figure 7.8 and 7.9.

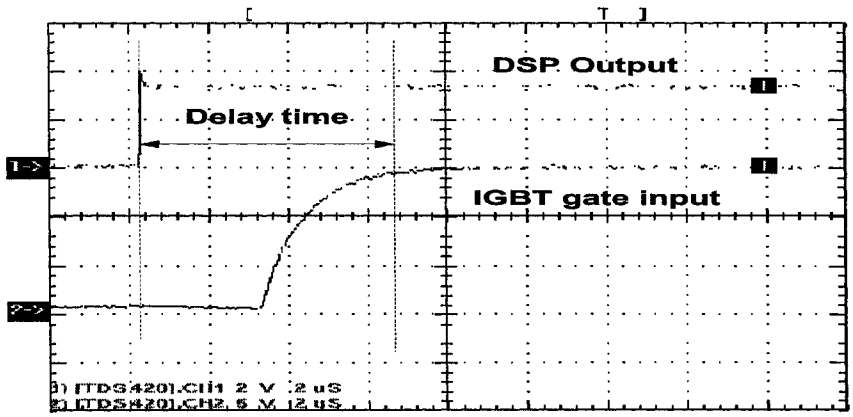


Figure 7.8 Delay on rising edge between the DSP output and IGBT gate input

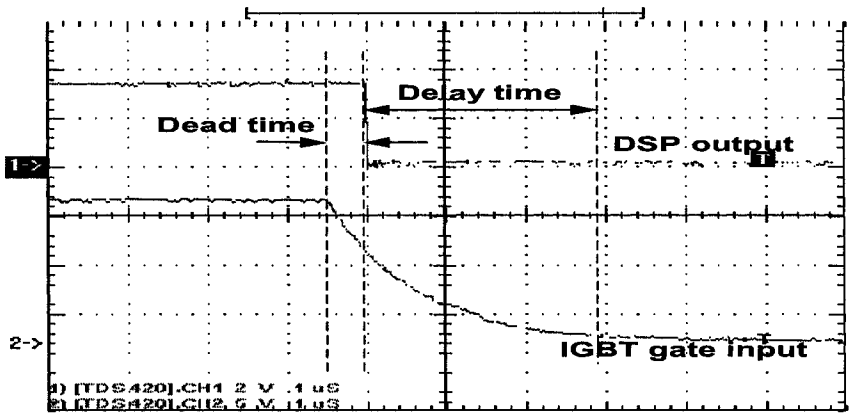


Figure 7.9 Delay on falling edge between the DSP output and IGBT gate input

7.2 New current control DSP implementation

The new current controller DSP implementation is undertaken on a signal-phase IGBT rectifier with 5mH supply inductance. The supply voltage range is from 60V to 120V and the current can vary from 3A to 10A.

The purposes of the test are to verify the operation of the DSP controlled single phase rectifier that should be similar as the simulation result; the new current controller can shape the rectifier input current into sinusoidal; achieve a zero current per PWM cycle and fixed switching frequency. The experimental results ware obtained under following test conditions:

* Supply voltage: 80Vrms
* DC link voltage: 120VDC
* Rectifier current: 3A
* PWM switching frequency: 2KHz
* Supply inductance: 5mH

The program was developed in C language and is described in chapter 6. Test results are shown below. The inverter bridge output voltage waveform is shown is Figure 7.10. It is a unipolar waveform.

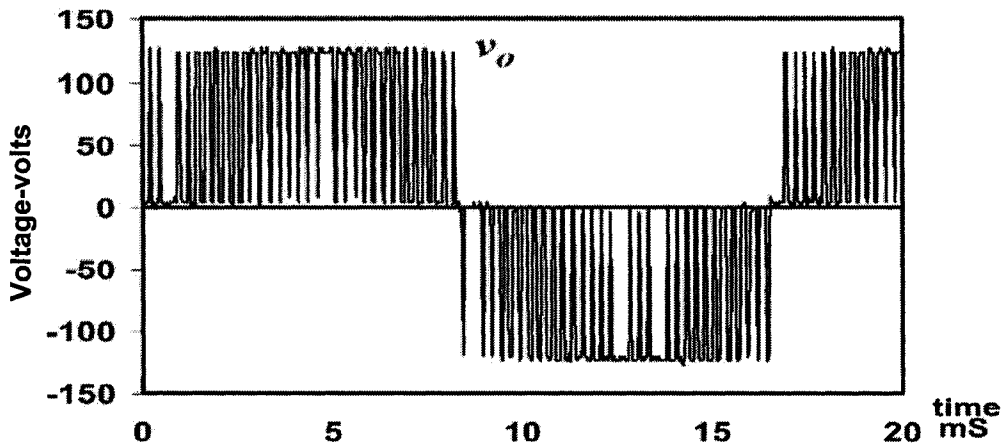


Figure 7.10 Rectifier bridge output voltage v_0

The Figure 7.11 shows the rectifier bridge output voltage v_0 expanded waveforms. This waveform is recorded in the negative cycle. The PWM pulses switch between 0V and -120V. If in positive cycle the PWM pulse switch between 0V and 120V.

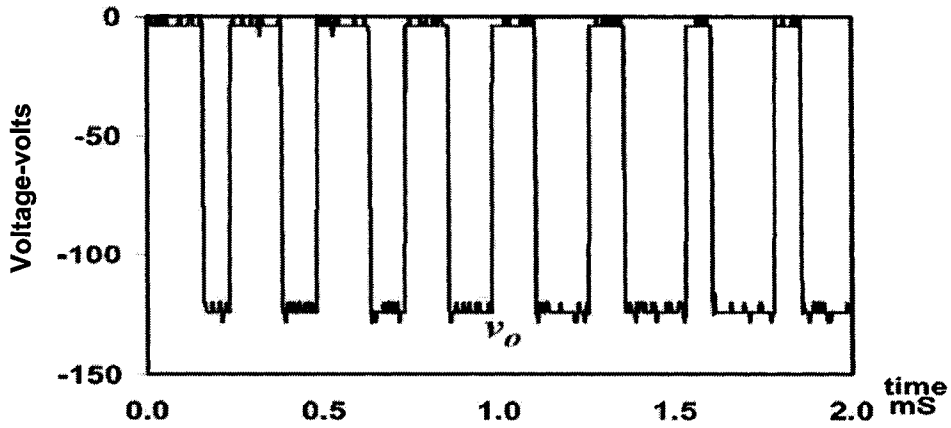


Figure 7.11 Rectifier bridge output voltage expend waveform

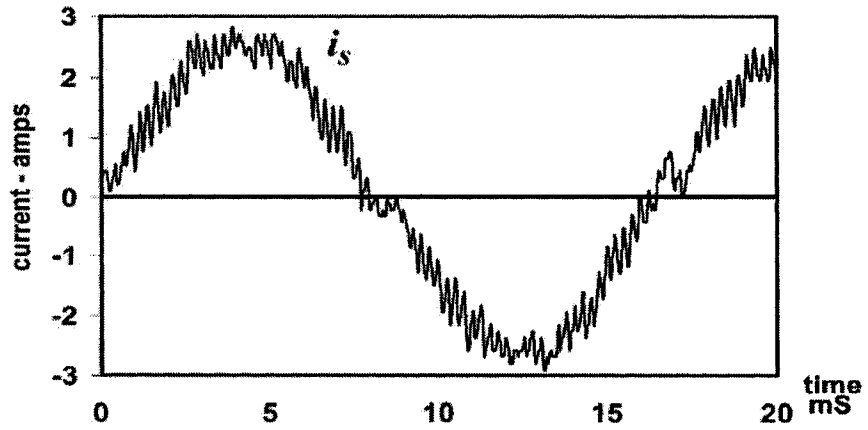


Figure 7.12 Rectifier bridge input current i_S

The sinusoidal rectifier input current waveform is shown in Figure 7.12. Some distortion in the input current waveform can also be observed. These could be caused by the following reasons: hardware and software delay time, switching noise and EMI. The circuit hardware delay time has been tested in the last section. That kind of delay is one of the reasons to cause the input current waveform distortion. The software delay is caused by C program and control scheme. In this proposed DSP current control scheme the duty cycle values can't be written to the duty cycle control registers until the next interrupt happens. In double update mode the waiting time is half

cycle. That delay time is big and can significantly affect the current waveform. The switching noise caused by IGBT switches can also have the affect to the DSP controller.

The Figure 7.13 shows the relation among the modulated carrier signal, current error and the PWM voltage signals. The modulated carrier signal and the current error were obtained from the DAC output. The PWM voltage waveform was obtained from the scope. The K_1*i_{error} signals are compared with m_a modulated carrier signals V_{C+}-m_a and V_{C-}-m_a. If the K_1*i_{error} signals are smaller than the carrier signals the switch is turned on, otherwise the switch is turned off.

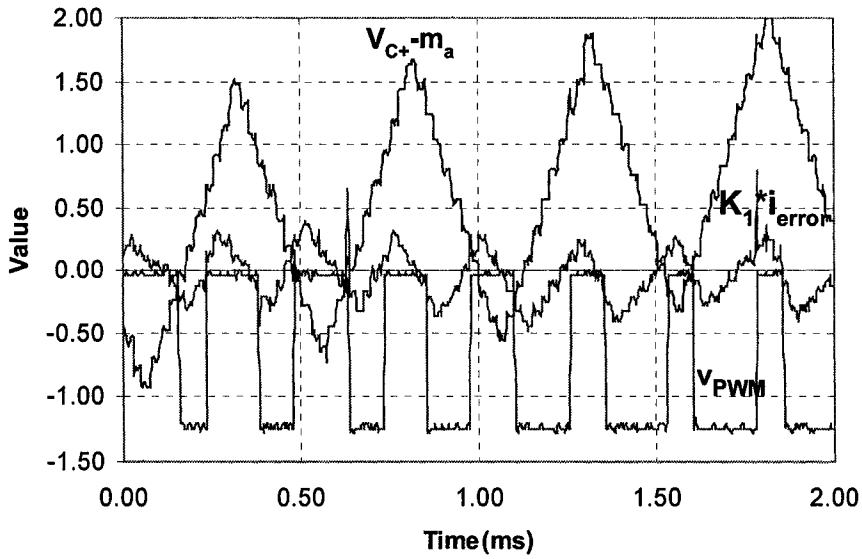


Figure 7.13 Carrier signal, current error and the PWM voltage signals.

From Figure 7.13 we also can observe that the average current error per half PWM cycle is centered nearly at zero. That means the DSP implementation of the new current controller is worked.

The Figure 7.14 shows the rectifier input current waveforms for different carrier frequencies. The carrier frequency can affect the rectifier bridge input current waveform. In

theory the higher the carrier frequency, the lower the current distortion. In experimental implementation the results are not similar as the simulation results. The current ripple is independent of the carrier frequency. There are many reasons could cause this kind problem such as hardware delay, noise and software limitations. The effect of the hardware delay has discussed above. The noise is always a problem in power electronics and sometimes may cause the system malfunction. The software limitations include a half PWM cycle delay; the DSP may not have enough calculation time in each interrupt to obtain the correct duty cycle values. The half cycle delay is unavoidable. As the DSP is used as a comparator in this test, lots of the DSP time is occupied. When the carrier frequency increases, the time period for each interrupt decreased and may not be enough for comparing the data and calculating the duty cycle values.

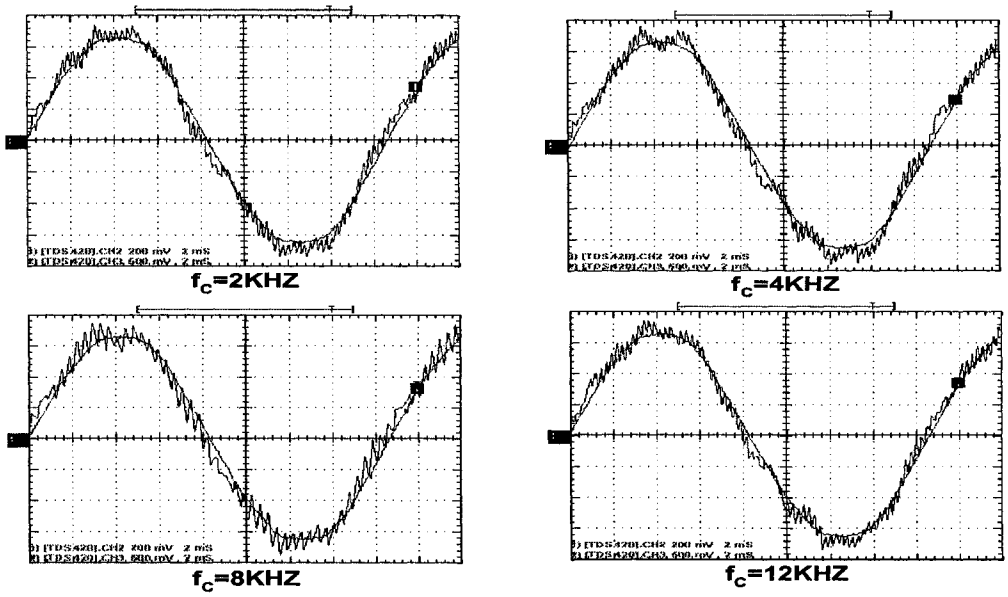


Figure 7.14 Rectifier input current in different carrier frequency

The Figure 7.15 shows the m_a waveform at different carrier frequency. The m_a was output from the DSP DAC port.

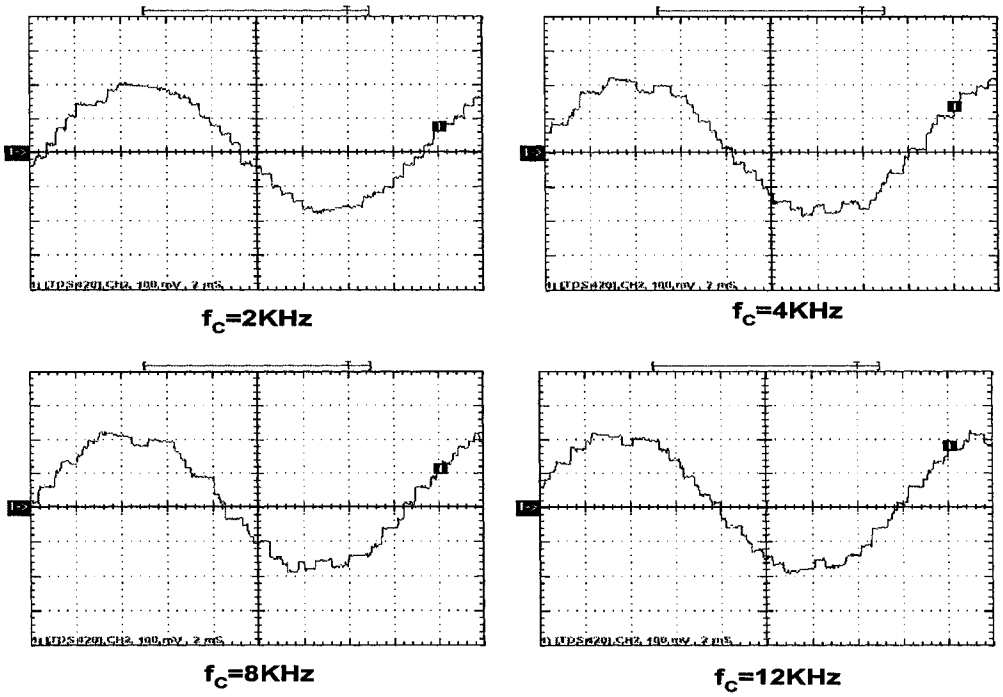


Figure 7.15 m_a in different carrier frequency

7.4 Summary

In this chapter the experimental result of the proposed current control scheme are given. By comparing the experimental result with theoretical simulation result, we can say that the new control scheme DSP application works but that the test results do not meet expectations. If in further work the delay time can be shorted, the switching frequency and EMI can be reduced, the DSP is not used as a comparator and the control C program is improved, better test results can be expected.

Chapter 8 Conclusion

A delta modulated carrier based current controller is described that generates PWM voltage waveforms for a single-phase PWM rectifier. A DSP experimental test system is used to implement the controller. The new current controller combines the excellent current wave shaping ability of hysteresis based controllers together with the constant switching frequency of carrier based controllers.

Examination of various current control methods such as "delta-modulated current control", "dead-beat adaptive hysteresis control", "predicted current control" and "Zero average current error control" is undertaken to show how relatively simple the proposed current controller is to implement. An investigation on generic PWM modulators using a signal integrator is also done to show how delta-modulated signals can be used with carrier signals to produce output PWM waveforms that are independent of the integrator constant. This examination is used to define the appropriate gain constant for the feedback current error signal in a PWM current controller.

The resultant current controller uses a sinusoidal amplitude modulated reference signal that is internally generated from the unipolar PWM modulator output signal. The size of the high frequency ripple in the current-error signal changes with the inductance size, but the average current error is always kept close to zero. The carrier half-cycle delay in generating the sinusoidal amplitude modulated reference signals, introduces an average current-error at low carrier frequencies, but these errors diminish rapidly as the carrier frequency is increased.

The new current controller is also implemented by using a ADSP-21992 DSP controller together with a single-phase IGBT rectifier. The DSP application has minimized the external hardware circuit to interface the DSP to the single-phase rectifier (no external ADC converter needed). The fast sampling rate has made it easier to perform the real-time current control and achieve fast current dynamics. The dead time that prevents potentially destructive short circuit can be automatically added to the PWM signals to increase the control system reliability.

Some drawbacks were observed in the experimental controller. The first drawback is associated with delays in the signals. Two major kinds of delay were experienced in experimental testing: the first delay is hardware delay and second is software delay. The hardware delay was caused by the isolation circuit. This is one factor but not a major one to cause the current waveform distortion. The major factor to cause the current waveform distortion was software delay. The PWM duty cycle control register can only be update once at the beginning of each interrupt. That means if the current changes during this interrupt cycle, the DSP cannot response to that change until the next interrupt coming. The longer the delay time, the more current distortion is experienced. The second major drawback experienced is switching noise caused by switching the higher power switched power supply. It can affect the DSP circuit.

The high sampling rate is also a concern. When DSP performs the proposed current control scheme, in order to pursue the fast current dynamics, the DSP samples the actual current as fast as possible to try to know the actual current change and generate the switching signals based on these feedback signals. The sampling rate can go up to 240KHz. This occupies a lot of the CPU time to read the data from ADC port and to do the operation to determine the status of the switch and limit the IGBT rectifier's switching frequency. Future research on reducing the sampling rate and increasing the program efficiency will be very helpful in reducing the current

waveform distortion. Using an analog simulator to perform the comparator function is a way to reduce the sampling rate and free the DSP CPU computation time.

A C program is used to develop the DSP control software. In the future it is also reasonable to write the DSP program by using assembly language and to compare the running result with the program using C language to see if there is any improvement on current waveform shaping ability, the signal sampling rate and current dynamics.

During the development of the new current controller, the K factor is set manually. This is because the main task of this test is to verify the waveform shaping ability of the new current control. In the future application, the K factor should be determined automatically by the program. There are many ways to perform this task. One is using the DC link voltage feedback signal. Further research should be done to verify it.

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Appendix A: Already published papers

A hybrid current controller for a 1-phase pwm rectifier combining hysteresis and carrier-based schemes to achieve a zero current error and unipolar pwm waveforms

John Salmon, Hao Zhang
Department of Electrical and Computer Engineering, University of Alberta, Edmonton, Alberta, Canada, T6G 2V4
ph: (780) 492 7037, email: salmon@ece.ualberta.ca

Abstract

A current controller is described for 1-phase pwm rectifiers that combines both the functionality of hysteresis-based and carrier based controllers. The development of this current controller is described with the aid of generic PWM controllers that use a sinusoidal modulating signal and a signal integrator. These controllers mimic the operation of the 1-phase pwm rectifier and are used to determine the optimal gain-constant associated the current-error feedback signal. The resultant current controller is relatively insensitive to variations in rectifier parameters such as the supply inductance and the dc link voltage magnitude. The controller combines the excellent current waveshaping ability of hysteresis-based controllers together with the constant switching frequency of carrier-based controllers. The main controller features include: real-time generation of the sinusoidal amplitude modulation signal from the pwm signal; elimination of phase-shifts caused by the limited rate-of-change of the rectifier current; a near zero current-error over a pwm half-cycle; no skewing effects in the current-error signal. Simulation results, using a per-unit system of values, are used to illustrate the step-by-step development of the current controller. A DSP-based controller is used, together with an IGBT rectifier, to demonstrate the experimental operation of the controller.

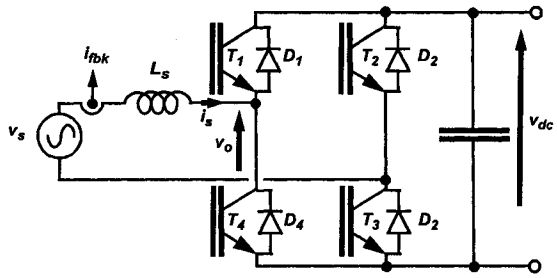
1 Introduction

Controlling the input current of a 1-phase pwm rectifier is a relatively easy task, see Fig. 1, but it is slightly more difficult to achieve an accurate high quality current control with minimal error under the normal operating conditions associated with a rectifier connected to the utility supply, [1-17]. A general classification for opposite controller types can be said to be those base upon a *"fixed current-ripple hysteresis current controller"*, see Fig. 1(b), versus a *"fixed frequency carrier-based pwm controller"*, see Fig. 1(c) [1-10]. Some systems have a *"hard-to-track"* current references with high frequency components, e.g. active filters [11-14]. PWM current controllers are also widely used in utility rectifiers [15-17]. [16] illustrates the difficulty of obtaining a zero current-error after each pwm cycle and [2] describes a scheme that can respond to a current-error after each pwm cycle.

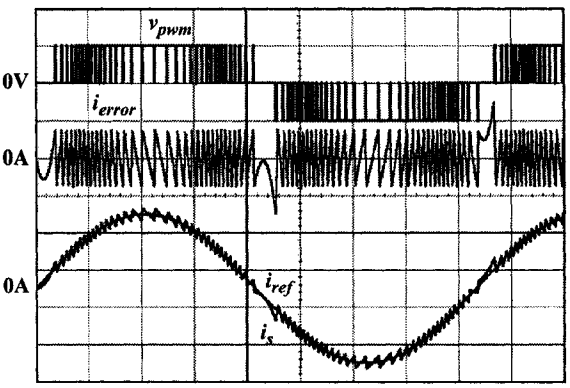
The first, and main, design goal for the current controller was to combine the excellent current waveshaping characteristics of hysteresis-based controllers with the benefits associated with fixed switching frequency carrier-based controllers.

The second design goal for the current controller, was to obtain a fixed pwm switching frequency that has an inherent variable current ripple, but that also achieves a zero average current-error over a pwm switching cycle.

Hysteresis controllers have a difficulty in controlling the switching frequency, see Fig. 1(b), but automatically generate the required amplitude modulation depth, or m_a, for the pwm signal generation, [7-10]. The third design goal for the current controller was to obtain a carrier-based pwm controller that can also automatically generate its own amplitude modulation depth for the generation of the pwm waveforms without requiring voltage feedback.

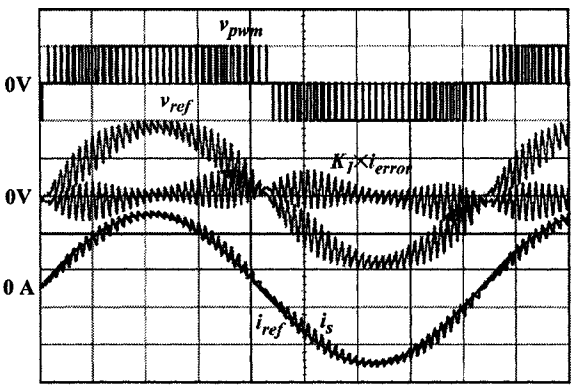


1(a) 1-phase IGBT H-bridge Pwm Rectifier



scales: time: 2 mS/div, v_{pwm}: 1 V/div, i_{ref}, i_s: 5A/div, i_{error}: 1 A/div

1(b) unipolar pwm hysteresis current controller: ΔI = 1.5 A



scales: time: 2 mS/div, v_{pwm}: 1V/div., v_{ref}, K_1*i_{error}: 0.5 V/div
i_{ref}, i_s: 5A/div, i_{error}: 1 A/div

1(c) unipolar pwm "carrier-based" current controller: f_c = 2kHz

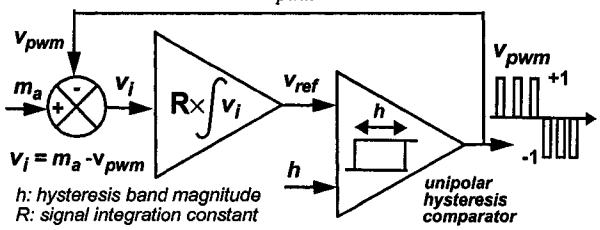
Fig. 1 1ϕ pwm rectifier I-controller waveforms: $I_{ref,pk}$ = 10A, V_{supply} = 120V

2 Delta-Modulated Hysteresis PWM Controllers

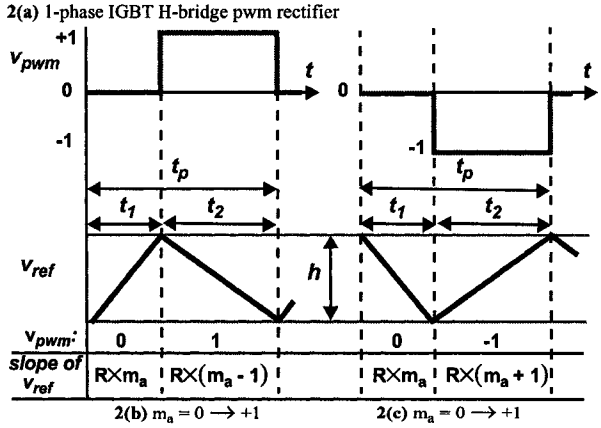
A unipolar pwm controller that uses a hysteresis comparator with a signal integrator is examined here as it best represents the structure of a hysteresis current-controlled pwm rectifier, see Figs. 1(a), 2(a). Examination of this controller identifies the relationship between the amplitude modulation depth m_a, of the pwm waveform v_{pwm}, the hysteresis magnitude h, and the integration constant, R. The results show that the relationship between m_a and $v_{pwm,av}$ is independent of R. This is significant for the final current controller as the generation of v_{pwm} can be made to be insensitive to variations in rectifier parameters such as the supply inductance.

2.1 Analysis of delta modulated waveforms

Feedback of a unipolar pwm hysteresis comparator output signal, see Fig. 2(a), to a signal integrator input can produce a self-oscillating closed-loop system, where the ramping rate of the integrator output signal v_{ref} changes with the polarity of v_{pwm}. The signal v_{ref} can be considered as a *delta modulated signal*, see Fig. 2(b). m_a is the amplitude modulation depth of the pwm modulator and determines the average of the pwm output signal over a pwm cycle, $v_{pwm,av}$. v_{ref} ramps between the upper and lower bounds of the hysteresis band h. The ramping rate over time of v_{ref} is determine by the integration constant R and both the signals m_a and v_{pwm}. The input signal m_a exists in the range ± 1, and v_{pwm} has the states 0 and ± 1.



2(a) 1-phase IGBT H-bridge pwm rectifier



2(b) $m_a = 0 \rightarrow +1$ 2(c) $m_a = 0 \rightarrow +1$

Fig. 2. Delta Modulated hysteresis pwm controller

The ramping rate of v_{ref} for a positive m_a is given by:

$$t_1: \frac{dv}{dt}(t_1) = R \times m_a, \; t_2: \frac{dv}{dt}(t_2) = R \times (m_a - 1) \quad \ldots\ldots (1)$$

Hence the periods t_1 and t_2 are given by:

$$t_1: t_1 = \frac{h}{R} \times \frac{1}{m_a}, \; t_2: t_2 = \frac{h}{R} \times \frac{1}{1 - m_a} \quad \ldots\ldots (2)$$

This the period of the pwm waveform $t_p = t_1 + t_2$ is given by:

$$t_p = \frac{h}{R} \times \frac{1}{m_a(1 - m_a)} \quad \ldots\ldots (3)$$

Hence for a fixed m_a, the switching frequency f_{sw} of v_{pwm} is:

$$f_{sw} = \frac{R}{h} \times m_a(1 - m_a) \quad \ldots\ldots (4)$$

The average of v_{pwm} is related to m_a in this p.u. system by:

$$v_{pwm,av} = \frac{t_2}{t_p} = \frac{\frac{h}{R} \times \frac{1}{1 - m_a}}{\frac{h}{R} \times \frac{1}{m_a(1 - m_a)}} = m_a \quad \ldots\ldots (5)$$

(5) States that the average of v_{pwm} is determined by m_a and is independent of the integration constant R and the hysteresis magnitude h. (4) states that the pwm switching frequency is determined by both the ratio of R/h and m_a. When considering the current controlled pwm rectifier both these relationships for f_{sw} are undesirable: m_a is sinusoidally varying and R is dependent on the circuit parameters, e.g. supply inductance, and their natural tolerance variations.

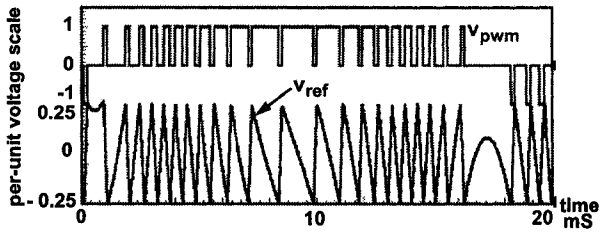
2.2 Fixing the switching frequency of a hysteresis controller

Since m_a is a sinusoidally varying signal in pwm rectifiers, the pwm switching frequency changes over the 60 Hz supply cycle. This produces a wide varying frequency spectrum which is considered undesirable and hard to filter. Since the integration constant is hard to control, the often used technique to fix the pwm switching frequency is to control the hysteresis band magnitude. For instance, putting:

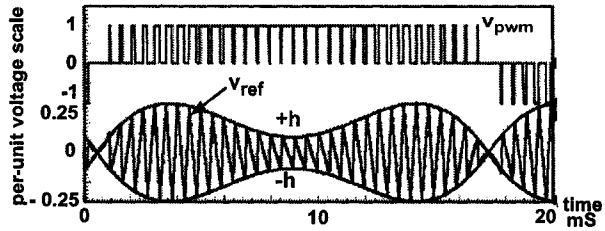
$$h = m_a(1 - m_a) \quad \ldots\ldots (6)$$

gives: $f_{sw} = R$ ..... (7)

The hysteresis band goes to zero at $m_a = 0$ and has a maximum magnitude of $h = 0.25$ at $m_a = 0.5$. Modulating signal waveforms for both "*fixed band hysteresis*" and "*variable band hysteresis*" control are shown in Fig. 3.



3(a) fixed band hysteresis



3(b) variable band hysteresis

Fig. 3 Comparison of fixed and variable band hysteresis pwm controllers

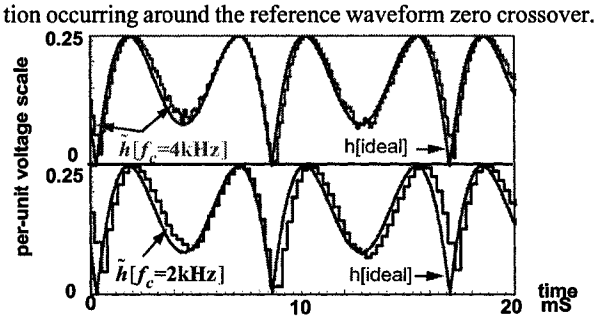
2.3 Constant switching frequency using adaptive hysteresis

A hysteresis-based current controller has difficulty in determining what current hysteresis band magnitude that is required to maintain a constant switching frequency. The magnitude of the hysteresis band h needs to be determined by the controller in real time in order to track the changes in the operating conditions of the rectifier: *adaptive hysteresis.*

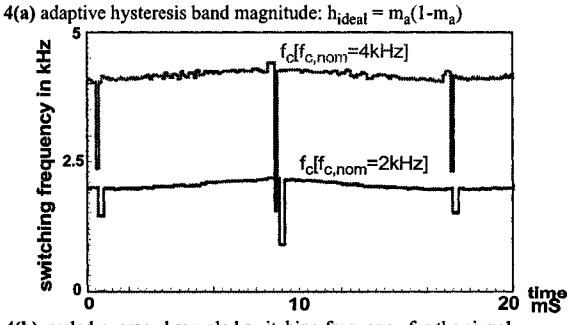
One feasible approach for an *adaptive hysteresis controller* to generate the desired hysteresis band h in real-time by linking h to the amplitude modulation depth m_a. Since m_a is directly linked to the resultant $v_{pwm,av}$, h could be determined by sampling v_{pwm} and determining a sampled value for m_a, $\tilde{m}_a$, from the sampled cycle average of v_{pwm}: $\tilde{v}_{pwm,av}$:

$$\tilde{h} = \tilde{m}_a(1-\tilde{m}_a)\ ,\ \tilde{m}_a = \text{sampled } m_a \text{ using } \tilde{m}_a = \tilde{v}_{pwm,av}\ .(8)$$

The hysteresis band generated in real time $\tilde{h}$, see Fig. 4(a), has a sampled stepped waveform characteristic with a refresh rate determined by the pwm switching frequency. The controllers ability to follow the "*ideal*" trajectory for h, improves the higher the switching frequency used, see Fig. 4(a). The real-time generation of the hysteresis band experiences jitter and lags the ideal when h is required to change rapidly. Real-time monitoring of the "*pwm cycle-average switching frequency*" can be difficult to obtain, but the results shown in Fig. 4(b) illustrate the switching frequency can experience fluctuations over the 60 Hz supply cycle, with some perturbation occurring around the reference waveform zero crossover.



4(a) adaptive hysteresis band magnitude: $h_{ideal} = m_a(1-m_a)$



4(b) cycled-averaged sampled switching frequency for the signal v_{pwm}

Fig. 4 Adaptive hysteresis pwm controller signals for $f_{c,nom}$=2 and 4 kHz.

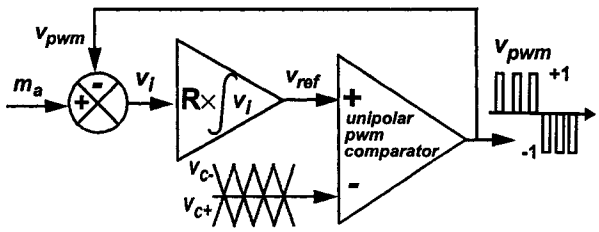
3 Delta-Modulated Carrier-Based PWM Controller

When using a delta modulated reference waveform v_{ref}, (5) illustrates that the average of the resultant pwm waveform, v_{pwm}, is independent of R and h. (6,8) illustrates that the switching frequency of v_{pwm} can be fixed by pre-determining the hysteresis band $\tilde{h}$. However, one can also conclude that the nett variation of the signal v_{ref} over a pwm-cycle should be forced to zero (for steady-state operation). This can be achieved by: (a) *fixing the pwm-cycle period using a carrier signal*, and (b) maintaining a *zero pwm-cycle average* for v_{ref}.

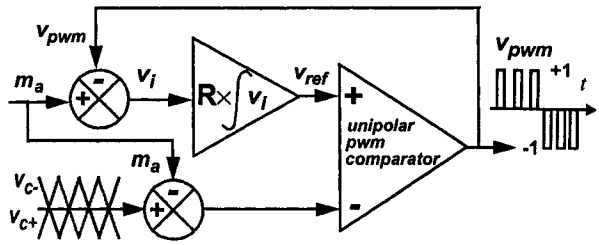
3.1 Fixed frequency pwm waveforms using a carrier signal

Carrier-based delta modulated pwm generators, see Fig. 5(a), do not pre-determine the hysteresis band magnitude but operate instead by fixing the pwm cyclic period using a sawtooth carrier waveform.

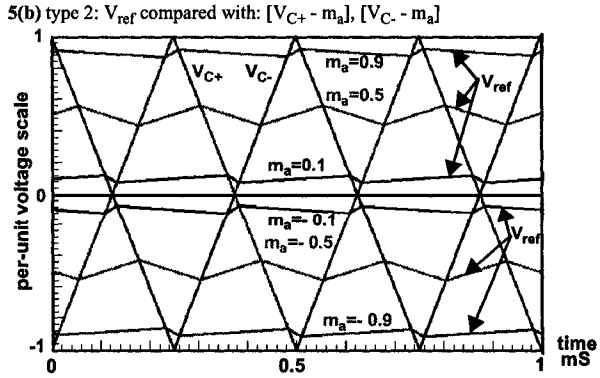
Identical to the hysteresis-based controller, the signal v_{ref} is still obtained from the result of integrating the difference between m_a and v_{pwm}, compare Figs. 5(a) and 2(a). However, here v_{ref} is compared with two sawtooth carrier signals using a *unipolar pwm comparator* to generate an output unipolar pwm waveform, v_{pwm}, see Fig. 5(a). The function of this *unipolar pwm comparator* is best described with the signal waveforms it creates, see Fig. 5(c). The peak-peak variation in the signal v_{ref} over a pwm cycle changes naturally with the magnitude of m_a, but its cyclic period is fixed at $^1/_{(2*fc)}$ with the waveform of the signal v_{ref} repeating every half-cycle.



5(a) type 1: V_{ref} compared with sawtooth carrier waveforms V_{C+}, V_{C-}



5(b) type 2: V_{ref} compared with: $[V_{C+} - m_a]$, $[V_{C-} - m_a]$



5(c) type 1 scheme: f_c = 2 kHz, R = 2*f_c, m_a = -0.9, -0.5,-0.1, 0.1, 0.5, 0.9.

Fig. 5 Delta-Modulated Carrier-Based PWM Controller

3.2 Design parameters for the pwm modulator

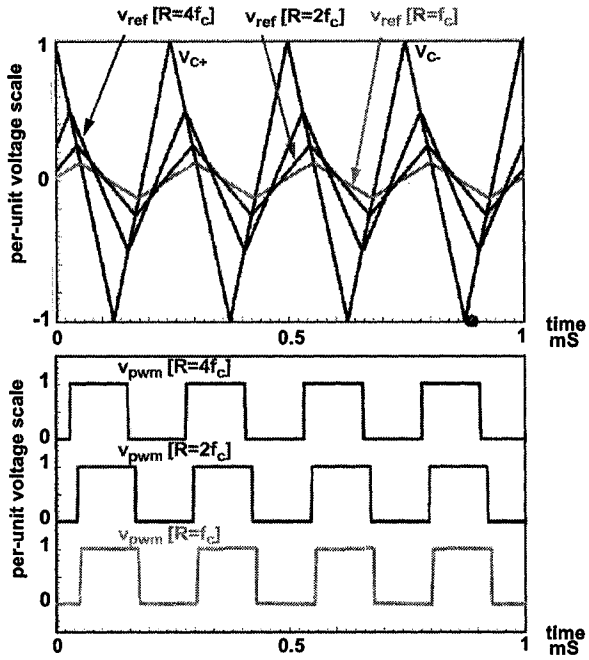
The pwm switching frequency f_{sw} is twice the carrier frequency, f_c. hence using (4) the pk-pk of v_{ref} is equivalent to h in hysteresis-based controllers and is given by:

$$\Delta V_{ref} = \frac{R}{2f_c} \times m_a(1 - m_a) \quad \text{.....(9)}$$

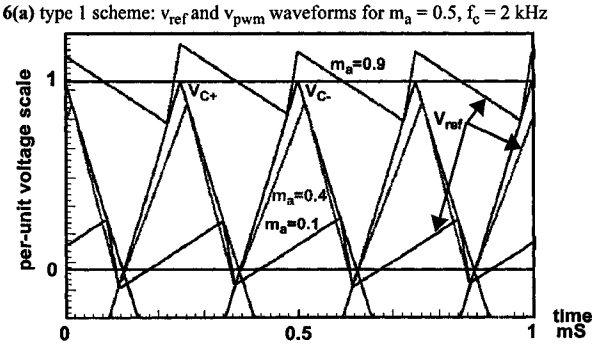
For instant, this is a maximum at $m_a = 0.5$ and if $R = 4f_c$:

$$\Delta V_{ref} = 0.5\text{p.u.} \quad \text{.....(10)}$$

(a) The integration constant R does not have to be fixed accurately for the signal m_a to accurately control the average of v_{pwm}. R can vary over a wide range, hence ΔV_{ref}, and the main effect on v_{pwm} is a ***slight*** phase shift relative to the carrier signal, see Fig. 6(a).



6(a) type 1 scheme: v_{ref} and v_{pwm} waveforms for $m_a = 0.5$, $f_c = 2$ kHz

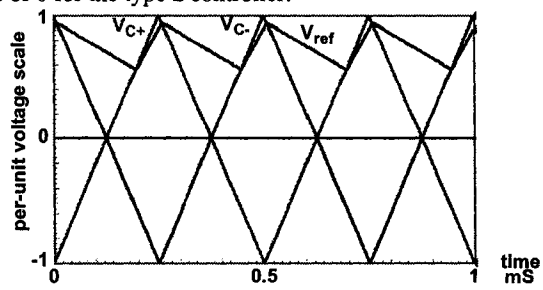


6(c) type 1 scheme: V_{ref} signal waveforms for $R = 8f_c$ V/sec, $f_c = 2$ kHz

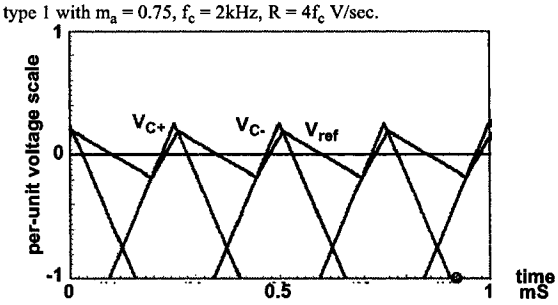
Fig. 6 Signals for type 1 delta-modulated carrier-based pwm controller

(b) With $R=4f_c$, & $m_a = 1$, the maximum slope of v_{ref} matches the slope of the sawtooth carrier waveform. However with appropriate switching logic, R can exceed this value, see Fig. 6(c). The controllers ability to cope with a wide variation in R is a useful feature in current-controlled pwm rectifiers.

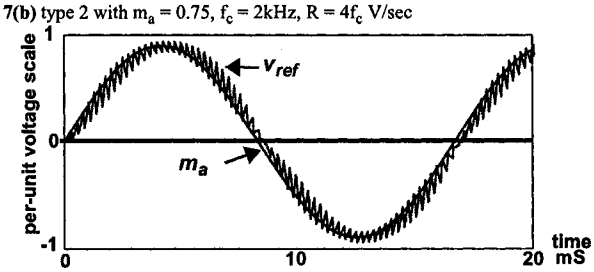
(c) For the same value of m_a, type 1 and 2 controllers generate the same waveform for v_{pwm}, see Figs. 7(a), 7(b). The main difference between the controllers is that v_{ref} has an average value of 0 for the type 2 controller.



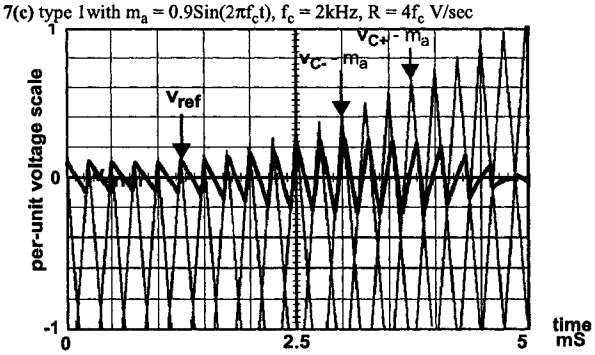
7(a) type 1 with $m_a = 0.75$, $f_c = 2$kHz, $R = 4f_c$ V/sec.



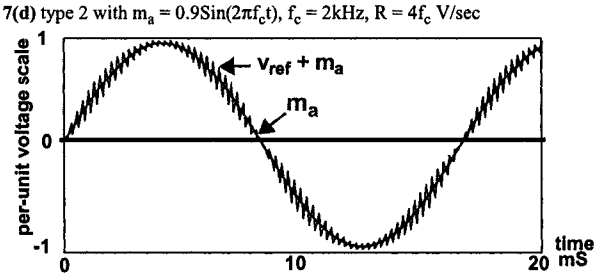
7(b) type 2 with $m_a = 0.75$, $f_c = 2$kHz, $R = 4f_c$ V/sec



7(c) type 1with $m_a = 0.9\text{Sin}(2\pi f_c t)$, $f_c = 2$kHz, $R = 4f_c$ V/sec



7(d) type 2 with $m_a = 0.9\text{Sin}(2\pi f_c t)$, $f_c = 2$kHz, $R = 4f_c$ V/sec

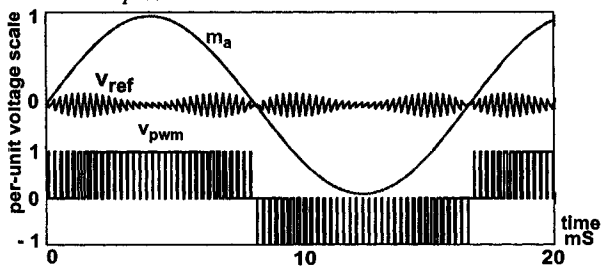


7(e) type 2 with $m_a = 0.95\text{Sin}(2\pi f_c t)$, $f_c = 2$kHz, $R = 4f_c$ V/sec

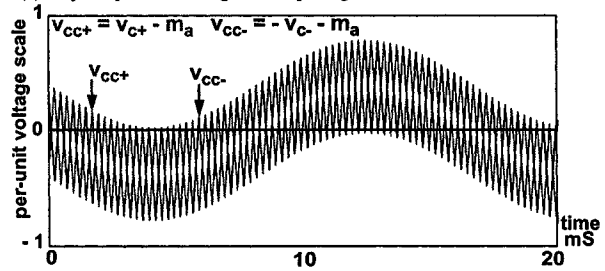
Fig. 7 Delta-Modulated Carrier-Based PWM Controller Signal Waveforms

The type 2 pwm controller, operating with the average of v_{ref} being zero see Fig. 7(d), has benefits when considering that the signal m_a is sinusoidally varying in pwm rectifier controllers. For type 1, v_{ref} varies sinusoidally with m_a and, as a result, lags m_a due the nature of the signal integrator, see Fig. 7(c). This also results in v_{pwm} lagging m_a. This phase shift is the main cause for the skewing of the i_{error} signal in 1-phase pwm rectifiers with current feedback, see Fig. 1(c).

In the type 2 pwm modulator, operating with a sinusoidal varying m_a, v_{ref} is still maintained centred on zero, see Figs 7(d) and 8(a), and no phase shift is experienced in v_{pwm} or the reconstructed signal, $v_{ref} + m_a$, see Fig. 7(e). This performance is obtained because the sawtooth carrier signal is modulated by m_a, see Fig. 8(b), and hence v_{ref} is maintained centred on zero. m_a still controls the pwm cycle-average of the output pwm waveform, v_{pwm}, see Figs. 8(a) and 8(b).



8(a) unipolar pwm and integrator output signal waveforms



8(b) carrier modulation by the reference waveform

Fig. 8 Current Controller

4 Fixed Frequency Carrier-Based Current Controller

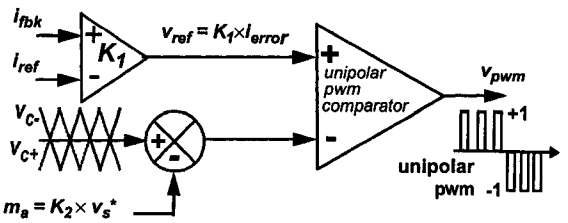
The general structure of the pwm modulators examined in sections 2 and 3, used an integrator and unipolar pwm waveforms since this matches the function of the 1-phase pwm rectifier. The signal v_{ref} is equivalent to the current-error signal with an appropriate feedback gain constant, see Fig. 9(a).

$$v_{ref} = K_1 \times i_{error} \quad \text{..... (11)}$$

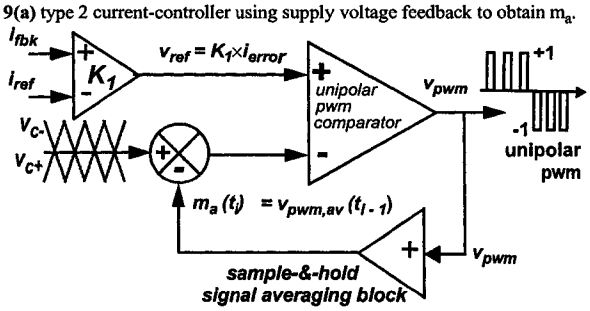
Comparing the expression for Δv_{ref} in (9) with an expression that defines the current ripple Δi_{error} obtained in pwm rectifiers, and assuming that the feedback gain factor K_1 is used to obtain p.u. values for the signal i_{error}, we get:

$$\Delta V_{ref} = m_a(1-m_a)\frac{V_{dc}}{2f_c L_s}K_1 = \frac{R}{2f_c} \times m_a(1-m_a) \quad \text{..... (12)}$$

$$R = K_1 \frac{V_{dc}}{L_s} \quad \text{..... (13)}$$



9(a) type 2 current-controller using supply voltage feedback to obtain m_a.



9(b) type 2 current-controller using sampled feedback of v_{pwm} to obtain m_a.

Fig. 9 PWM current controller based upon the type 2 carrier-based unipolar pwm delta modulator and using the current-error signal.

The results of section 3 demonstrated that:

(a) the pwm cycle-average of v_{pwm} is unaffected by R

(b) no phase shifts are introduced into v_{pwm}, hence no skewing of v_{ref}, due to the sinusoidal modulation of v_{pwm}.

In 1-phase current control of rectifiers, these characteristics are equivalent to achieving a current-error that is centred on zero, i.e. *a zero pwm cycle current-error*, with no skewing as observed in Fig. 1(c). Since the pwm generation is insensitive to variations in R, this is equivalent to the controller being insensitive to variations in the rectifier parameters such as the supply inductance, L_s, and the dc link voltage V_{dc}.

4.1 Design of the current feedback loop

A good value to choose for the constant R is 0.5, as it allows the controller to respond rapidly during transients. This produces $\Delta v_{ref} = 0.5$. This can be used to fix the scaling factor K_1 by assuming nominal values for V_{dc} and L_s and noting:

$$\Delta I = m_a(1-m_a)\frac{V_{dc}}{2f_c L_s} \quad \text{..... (14)}$$

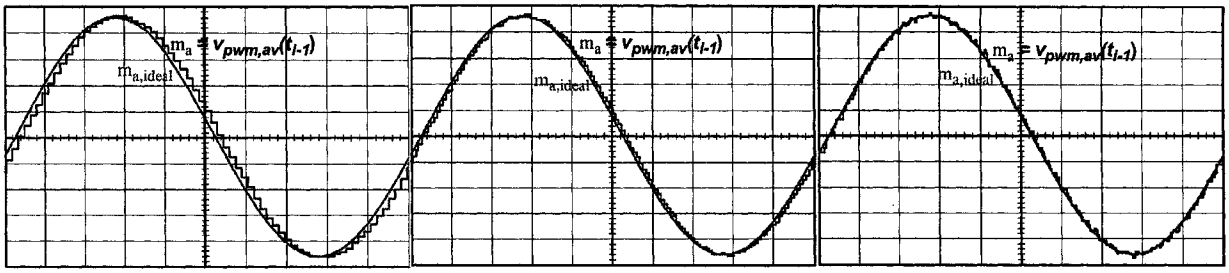
is a maximum at $m_a = 0.5$: $\Delta I_{max} = \dfrac{V_{dc}}{8f_c L_s}$ ..... (15)

So an appropriate design choice for K_1 is to pick:

$$K_1 \Delta I_{max} = 0.5 \Rightarrow K_1 = \frac{1}{2\Delta I_{max}} \quad \text{..... (16)}$$

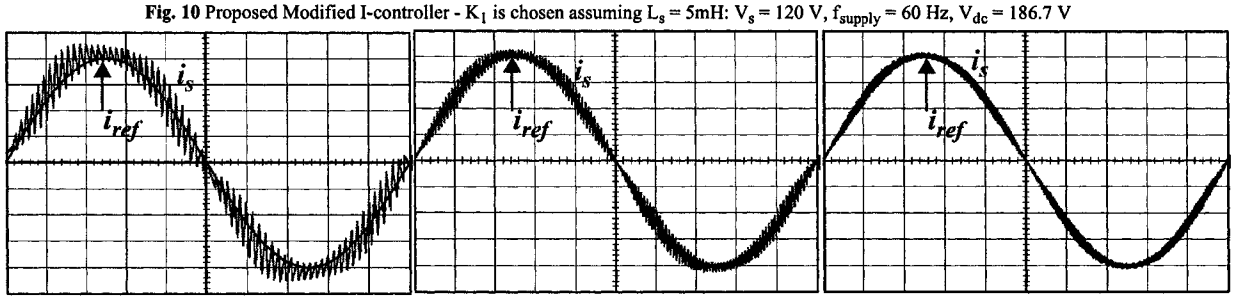
4.2 Real-time generation of m_a to eliminate voltage feedback

The current controller illustrated in Fig. 9(a), requires a reference signal m_a that represents the sinusoidal voltage required at the rectifier input terminals, V_s^*, to draw the required current level. The supply voltage cannot be used, as



10(a) f_c = 2kHz, K_1 = 0.215, L_s = 7.5mH **10(b)** f_c = 4kHz, K_1 = 0.43, L_s = 7.5mH **10(c)** f_c = 8kHz, K_1 = 0.86, L_s = 7.5mH

Fig. 10 Proposed Modified I-controller - K_1 is chosen assuming L_s = 5mH: V_s = 120 V, f_{supply} = 60 Hz, V_{dc} = 186.7 V



11(a) f_c = 2kHz, K_1 = 0.215, L_s = 2.5mH **11(b)** f_c = 4kHz, K_1 = 0.43, L_s = 2.5mH **11(c)** f_c = 8kHz, K_1 = 0.86, L_s = 2.5mH

Fig. 11 Proposed Modified I-controller - K_1 is chosen assuming L_s = 5mH: V_s = 120 V, f_{supply} = 60 Hz, V_{dc} = 186.7 V

skewing of the current-error signal may result because V_s* lags the supply voltage. V_s* is also changes with the load current level, lastly, it is difficult to obtain an accurate value for K_2. A modified controller can be used, see Fig. 9(b), where the m_a used in one half-cycle of the carrier, is determined *internal* to the controller from the average of v_{pwm} generated in the previous half-cycle: mathematically expressed as:

$$m_a(t_i) = = v_{pwm,av}(t_{i-1}) \quad \text{.....(17)}$$

m_a at time t_i (i = ith carrier half-cycle) is determined from from the average of v_{pwm} during the previous $(i\text{-}1)^{th}$ half-cycle. This modification makes it unnecessary to use the supply voltage in the generation of the pwm waveforms.

4.3 Simulation results for the proposed current controller

Simulation testing was undertaken on the current controller structure shown in Fig. 9(b) using a 1-phase pwm H-bridge rectifier and the results are shown in Figs 10 and 11. The real time generation of the amplitude modulation signal m_a is shown in Fig. 10 with updating undertaken every carrier half-cycle. Low switching frequencies were used in the simulations to illustrate that, with low carrier frequencies, a large phase angle lag in the sampled m_a can exists relative to the ideal m_a due to the half-cycle delay required to determine a value for the sampled m_a from v_{pwm}. Obviously the higher the switching frequency, the more ideal the sampled m_a signal becomes. Skewing of the supply current waveform exists at low carrier frequencies due to the phase lag in the sample m_a. This skewing and the current ripple diminishes rapidly with increasing carrier frequencies. Testing also revealed that the controller was insensitive to variations in the supply inductance (±50% variations were examined) as predicted by the controller insensitivity to the integration constant R.

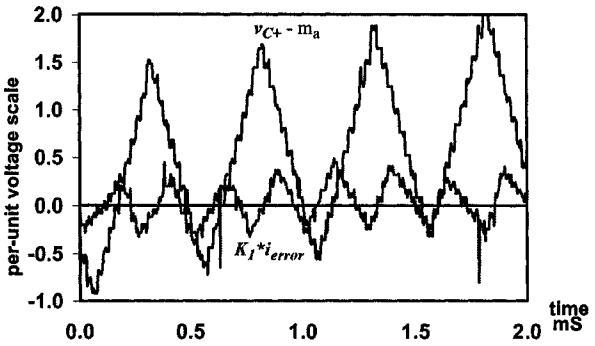
4.3 Experimental results for the proposed current controller

Testing was undertaken on a rectifier using a 5mH supply inductance and a 60Hz supply with voltages ranging from 60 to 120 V and currents varying from 3 to 10 A. The Analogue Device DSP ADSP-21992 system was used for the controller.

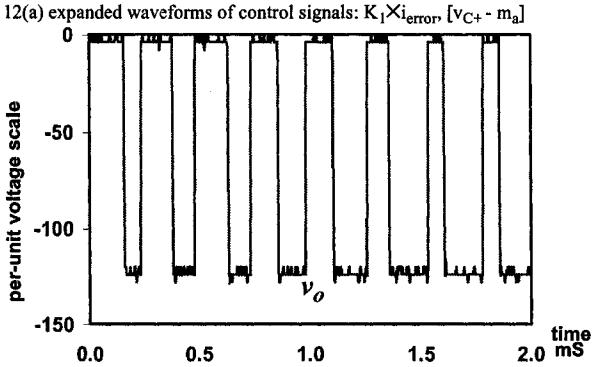
The intersections of the current-error signal with the modulated sawtooth carrier signal, see Fig. 12(a), illustrate how the unipolar pwm voltage signals were created. Fig. 12(b) shows the inverter bridge output voltage (negative unipolar voltage waveforms) associated with the signals in Fig. 12(a). The rectifier input current is sinusoidal, see Fig. 12(c), and the inverter bridge output voltage is unipolar and typical of 1-phase pwm rectifier using a H-bridge.

5 Conclusions

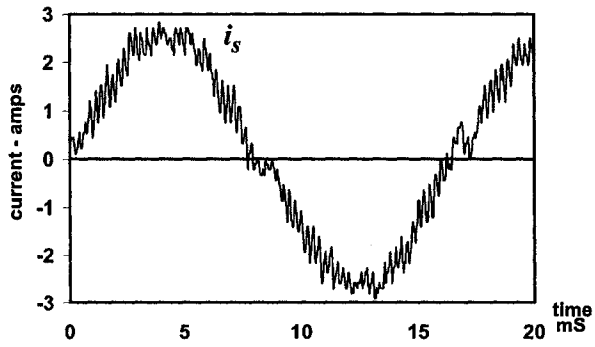
The development of a delta modulated carrier based current controller is described that generates pwm voltage waveforms for a 1-phase pwm rectifier. Examination of generic pwm modulators using a signal integrator is undertaken to show how delta modulated signals can be used with carrier signals to produce output pwm waveforms that are independent of the integrator constant. This examination is used to define an appropriate gain constant for the feedback current-error signal in a pwm current controller. The resultant current controller uses a sinusoidal amplitude modulated reference signal that is internally generated from the unipolar pwm modulator output signal. The size of the high frequency ripple in the current-error signal changes with the inductance size, but the average current-error is always kept close to zero. The carrier half-cycle delay in generating the sinusoidal amplitude modulated reference signal, introduces an average current-error at low carrier frequencies, but these errors diminish rapidly as the carrier frequency is increased.



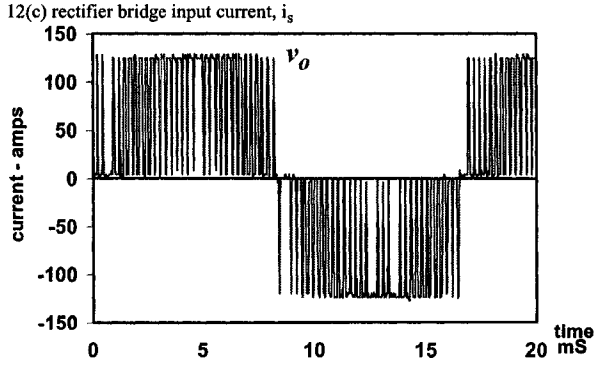
12(a) expanded waveforms of control signals: $K_1 \times i_{error}$, $[v_{C+} - m_a]$



12(b) rectifier bridge output voltage: v_o, expanded waveforms



12(c) rectifier bridge input current, i_s



12(d) rectifier bridge output voltage: v_o

Fig. 12 type 2 controller: 1ϕ pwm rectifier: E_{dc}= 120V, $I_{s,pk}$ = 3A, L_s = 5mH

6 Acknowledgments

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A hybrid carrier-based hysteresis current controller for pwm rectifiers using an internal voltage reference signal to achieve a pwm cycle zero current-error

John Salmon, Hao Zhang
Department of Electrical and Computer Engineering,
University of Alberta, Edmonton, Alberta, Canada, T6G 2V4
ph: (780) 492 7037, email: salmon@ee.ualberta.ca

Abstract

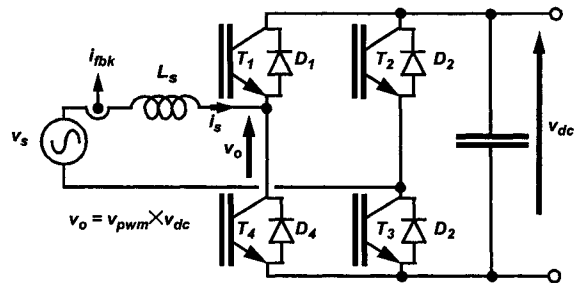
A current controller is described for 1-phase pwm rectifiers that combines the functionality of hysteresis-based and carrier based controllers. A carrier-based unipolar PWM delta modulator, using voltage reference signals, is used to illustrate how a fixed switching frequency with ramp-modulated reference signals can be integrated. When using a per-unit carrier sawtooth of magnitude ±1, this PWM modulator is also used to show how the current-error signal should be scaled to form a reference signal with an ideal maximum pk-pk magnitude of 0.5. Simulation waveforms are used to illustrate that once the current-error signal has a fixed nominal gain, the resultant current controller is insensitive to rectifier parameter changes such as the supply inductance. Finally, the current controller is implemented using an internally generated amplitude modulated reference signal so that no voltage reference signal is required.

Keywords: Converter Controllers, PWM Techniques, Modelling and Simulation, Rectifier Technology.

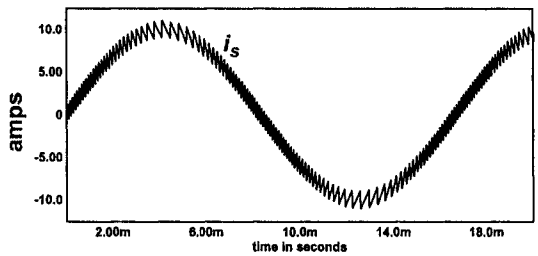
(1) Introduction

There are many important issues relating to obtaining a high quality current controller for pwm rectifiers, see Fig. 1, e.g. [1-16]. A general classification for opposite controller types can be said to be those base upon a *"fixed current-ripple hysteresis current controller"*, see Fig. 2(a) and 3(a), versus a *"fixed frequency carrier-based pwm controller"*, see Fig. 2(b) and 3(b), [7-9]. Some systems have a *"hard-to-track"* current reference with high frequency components, e.g. active filters [10-13]. PWM current controllers are also widely used in utility rectifiers [14-16]. [15] illustrates the difficulty of obtaining a zero current-error after each pwm cycle and [2] describes a scheme that can respond to a current-error after each pwm cycle.

The current controller examined was developed for a 1-phase pwm rectifier in order to achieve controller with: (a) a carrier-based modulator with a fixed switching frequency; (b) excellent current tracking similar to hysteresis-based schemes; (c) no requirement to use the voltage supply as a voltage reference, (d) merge the functionality of hysteresis controllers with that of carrier based schemes. Hysteresis controllers, see Fig. 3(a), automatically generate the required amplitude modulation depth, or m_a, but have an inherent variable switching frequency. Some adaptive hysteresis schemes have been proposed that

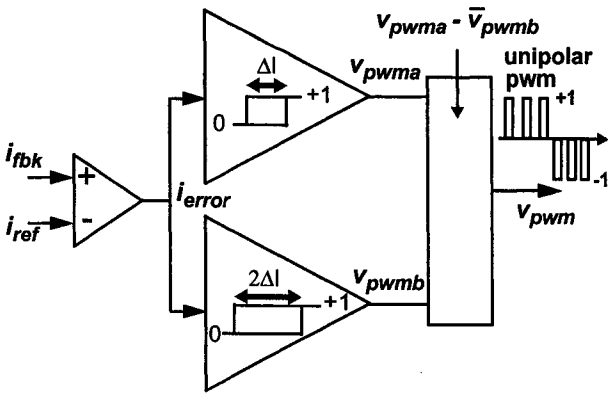


1(a) 1-phase H-bridge pwm rectifier

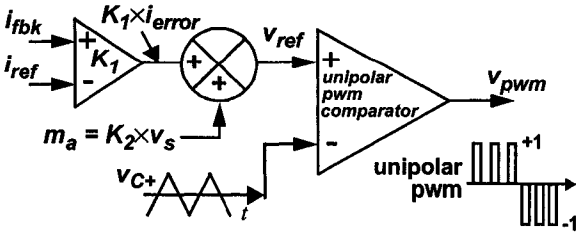


1(b) supply current using a low switching frequency

Fig. 1 Current controlled 1-phase PWM rectifier



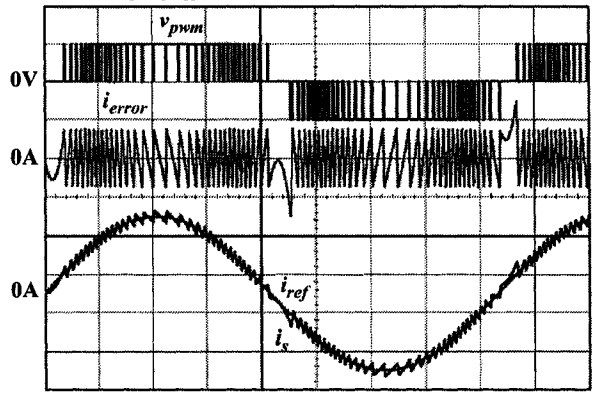
2(a) fixed current-ripple unipolar hysteresis PWM



2(b) fixed frequency unipolar carrier-based pwm controller

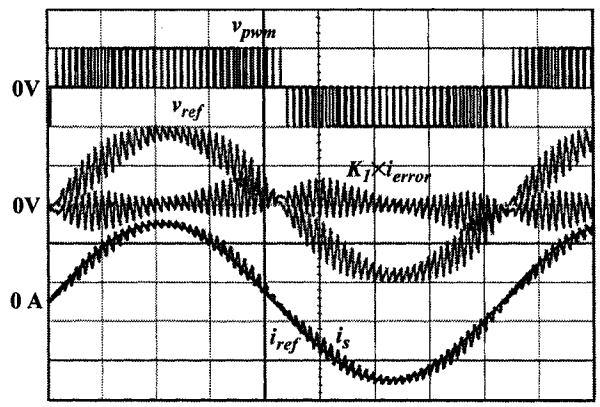
Fig. 2 Two Basic Unipolar PWM Current Controllers

control the switching frequency [7-9]. Carrier-based schemes can maintain a constant switching frequency and inherently have a variable pk-pk current ripple, Fig. 3(b). If the controller uses the supply voltage as a reference in the modulator, then the current error, i_{error}, has a variable average error over a pwm cycle, see $K_1 \times i_{error}$ in Fig. 3(a).



scales: time: 2 mS/div, v_{pwm}: 1 V/div, i_{ref}, i_s: 5A/div, i_{error}: 1 A/div

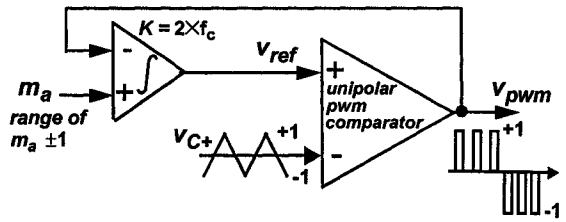
3(a) unipolar pwm hysteresis current controller: ΔI = 1.5 A



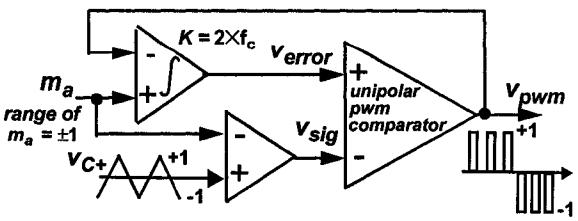
scales: time: 2 mS/div, v_{pwm}: 1V/div., v_{ref}, $K_1 * i_{error}$: 0.5 V/div i_{ref}, i_s: 5A/div, i_{error}: 1 A/div

3(b) unipolar pwm "carrier-based" current controller: f_c = 2kHz

Fig. 3 I-controller waveforms: $I_{ref,pk}$ = 10A, V_{supply} = 120V



4(a) case (a): integrator output = v_{ref}



4(b) case (b): integrator output = v_{error}

Fig. 4 Carrier-based Unipolar PWM Delta Modulator

(2) Combining hysteresis & carrier-based pwm controllers

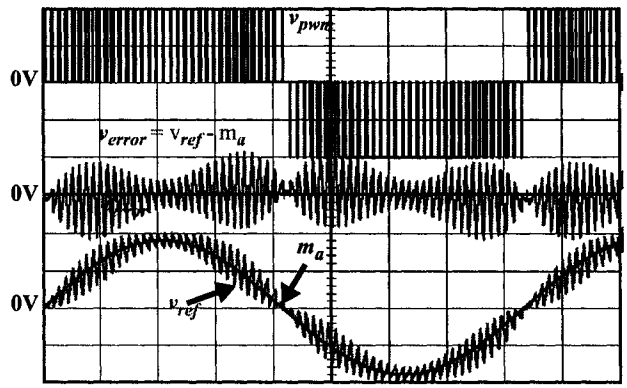
The integration function associated with the rectifier input current and supply inductor can be functionally simulated in a *"Carrier-based Unipolar PWM Delta Modulator"*, Fig. 4. m_a is a sinewave amplitude modulated signal and represents the supply voltage. The unipolar pwm voltage signal, v_{pwm}, represents the inverter output voltage. The integrator represents the rectifier inductor. This modulator can have two forms:

(a) *integrator output* = v_{ref}: v_{ref} functionally represents the rectifier input current i_s, or the signal i_{fbk} in a current controller.

***(b) integrator output* = v_{error}**: the signal m_a is subtracted from the sawtooth carrier signal, v_{C+}, and the integrator output signal functionally represents the current error signal:

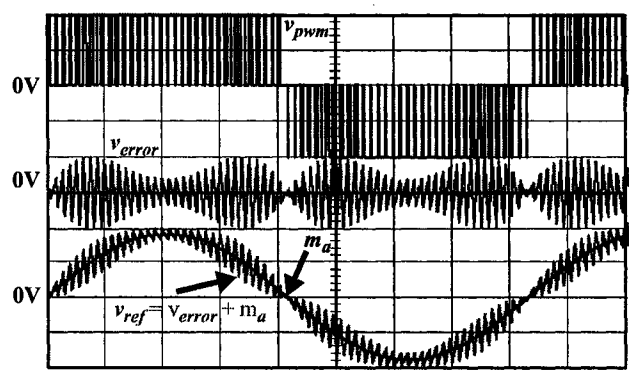
$$i_{error} = i_{fbk} - i_{ref} \quad \text{.....[1]}$$

Functionally, both schemes are similar with the exception that the integrator output has to follow the sinewave reference m_a in case (a), whilst in case (b) the integrator output is centred on zero, see Figs. 5 and 6. For case (a), this results in the v_{error} signal being lopsided with a varying cycle-error. Case (b) does not suffer from this and v_{error} has a zero cycle-error, Fig. 5(b).



scales: time: 2 mS/div, v_{pwm}, m_a, v_{ref}: 0.5 V/div, v_{error}: 0.2V /div

5(a) case (a): integrator output = v_{ref}



scales: time: 2 mS/div, v_{pwm}, m_a, v_{ref}: 0.5 V/div, v_{error}: 0.2V /div

5(b) case (b): integrator output = v_{error}

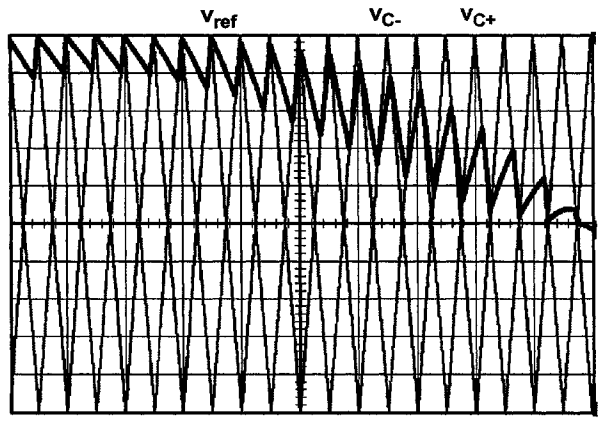
Fig. 5 Carrier-based Unipolar PWM Delta Modulator: f_c = 2kHz

Fig. 6 shows the expanded waveforms of the integrator output signal where: in case (a) v_{ref} is made to follow the sinewave reference m_a, introducing a phase-lag and resulting in a non-zero average error for v_{error} over a pwm cycle; in case (b) the integrator output, v_{error}, has a variable peak-peak output but has a zero average error over a switching cycle.

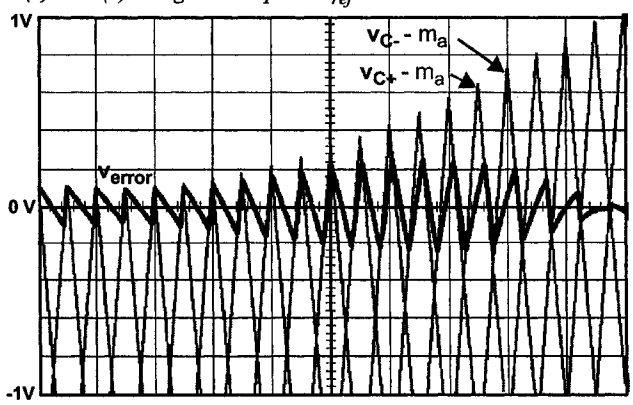
Conclusion: In a current controller, the current-error should be compared with the sawtooth reference signal and an amplitude modulated signal representing the sinewave supply voltage.

(3) Parameter setting for the hybrid pwm modulator

The delta modulator integration constant K is shown to be $2*f_c$ in Fig. 4 (f_c = carrier frequency). The waveforms shown in Fig. 7 show the integrator output signal, = v_{ref}, for case (a) using f_c = 2 kHz and several values of K. The waveforms are shown in per-unit with v_{pwm} taking the switching states [±1, 0] and the sawtooth carrier varying between ±1. The desired pwm output can be obtained over a wide range of integrator K values. The average of the pwm output depends upon m_a and not K: K affects the peak-peak magnitude of v_{ref}. As m_a approaches unity, the maximum slope of v_{ref} approaches the slope of the sawtooth carrier signals when $K = 4\times f_c$. For this case of K, the maximum peak-peak value of v_{ref} is 0.5.

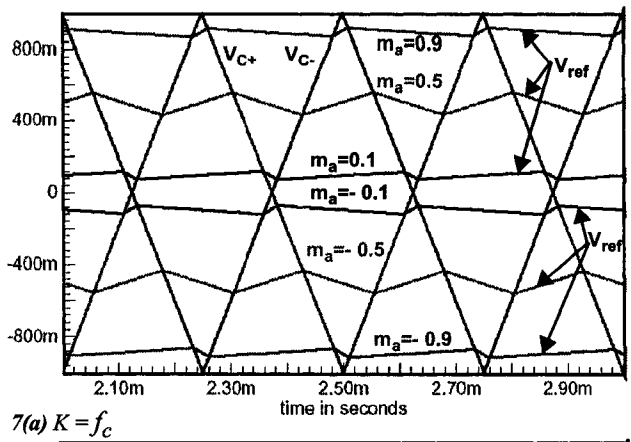


6(a) case (a): integrator output = v_{ref}

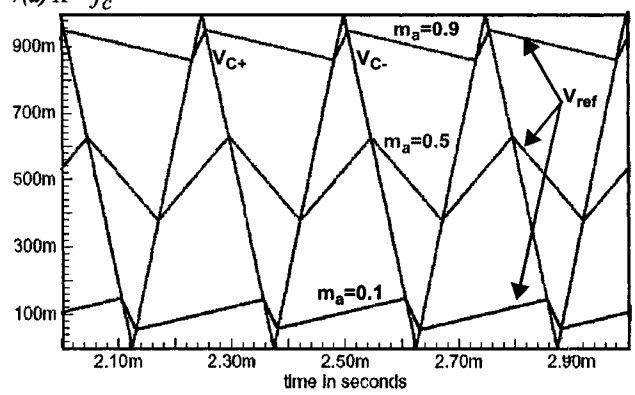


6(b) case (b): integrator output = v_{error}

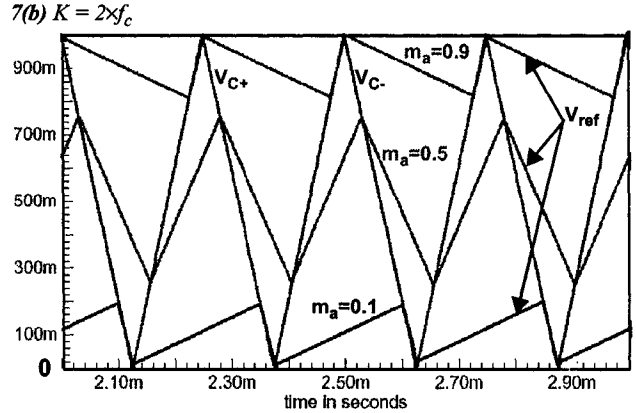
Fig. 6 Expanded signal waveforms: Carrier-based Unipolar PWM Delta Modulator: V_{C+}, V_{C-} = +ve & -ve carrier signals respectively



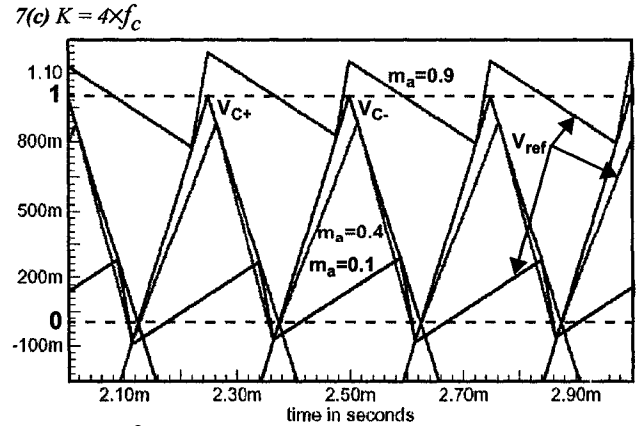
7(a) $K = f_c$



7(b) $K = 2\times f_c$

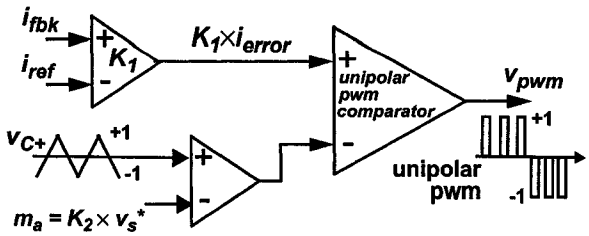


7(c) $K = 4\times f_c$

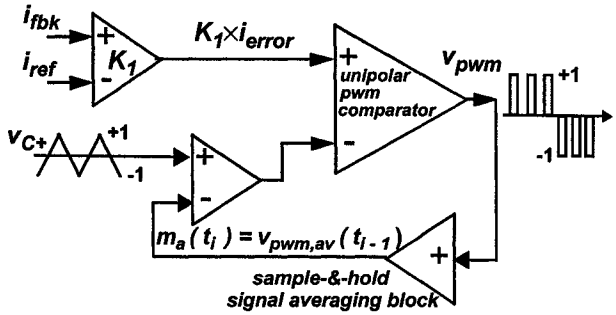


7(d) $K = 8\times f_c$

Fig. 7 Carrier-based Unipolar PWM Delta Modulator: v_{ref} for case (a)



8(a) I-controller using $m_a = K_2 \times v_s^*$



8(b) Modified I-controller using $m_a(t_l) = v_{pwm,av}(t_{l-1})$

Fig. 8 I-controller based upon the Carrier-based Unipolar PWM Delta Modulator and using the current error signal

Conclusion: Assuming per-unit values for the signals, 0.5 is a good value to use for the maximum peak-peak current-error signal in a current controller. This can be used to design the scaling factors in the current feedback loop. A pwm rectifier using unipolar pwm has:

$$\Delta I = m_a(1-m_a)\frac{V_{dc}}{2f_cL_s} \quad \text{.....[2]}$$

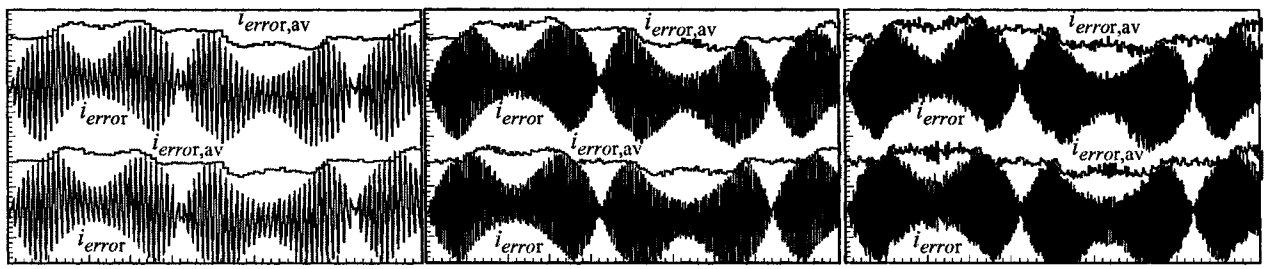
This is a maximum at $m_a = 0.5$: $\Delta I_{max} = \frac{V_{dc}}{8f_cL_s}$ .....[3]

So an appropriate design choice for the current feedback scaling factor, K_1 associated with the current error signal i_{error}, is to pick:

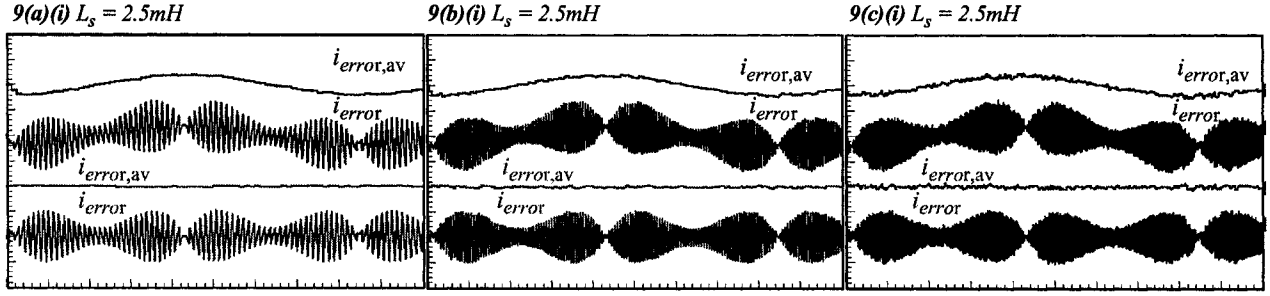
$$K_1 = \frac{0.5}{\Delta I_{max}} = \frac{4f_cL_s}{E_{dc}} \quad \text{.....[4]}$$

(4) Hybrid Current Controller

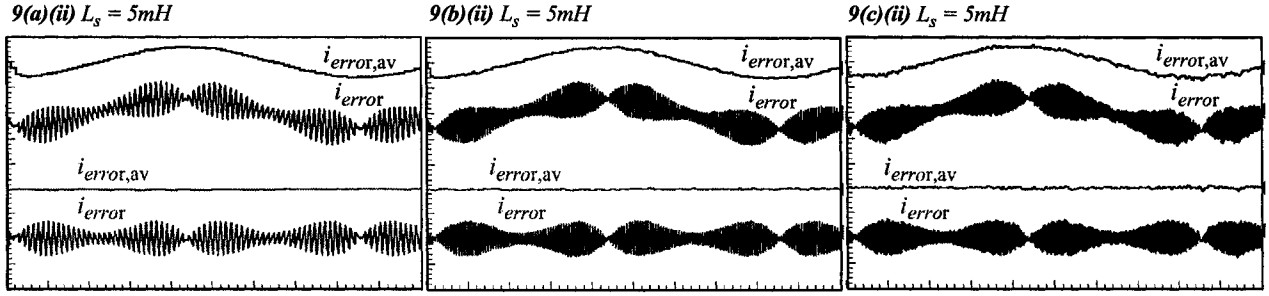
A current controller based upon the case (b) unipolar pwm delta modulator is shown in Fig. 8(a), where the reference m_a is obtained using the signal: $K_2 \times V_s^*$: V_s^* = the voltage required at the inverter terminals to obtain the desired current. Since V_s^* is hard to define accurately, the modified controller, Fig. 8(b), shows how v_{pwm} can be used to generate the desired m_a:



9(a)(i) $L_s = 2.5mH$ *9(b)(i)* $L_s = 2.5mH$ *9(c)(i)* $L_s = 2.5mH$



9(a)(ii) $L_s = 5mH$ *9(b)(ii)* $L_s = 5mH$ *9(c)(ii)* $L_s = 5mH$



9(a)(iii) $L_s = 7.5mH$ *9(b)(iii)* $L_s = 7.5mH$ *9(c)(iii)* $L_s = 7.5mH$

9(a) $f_c = 2kHz$, $K_1 = 0.215$ *9(b)* $f_c = 4kHz$, $K_1 = 43$ *9(b)* $f_c = 8kHz$, $K_1 = 0.86$

Key: top pair of waveforms: $m_a = K_1 \times v_{s,}$ **bottom pair of waveforms:** $m_a = K_1 \times v_s^*$

Fig. 9 Proposed I-controller: K_1 is chosen assuming $L_s = 5mH$: $V_s = 120$ V, $f_{supply} = 60$ Hz, $V_{dc} = 186.7$ V

$m_a(t_i) = = v_{pwm,av}(t_{i-1})$ ..... [4]

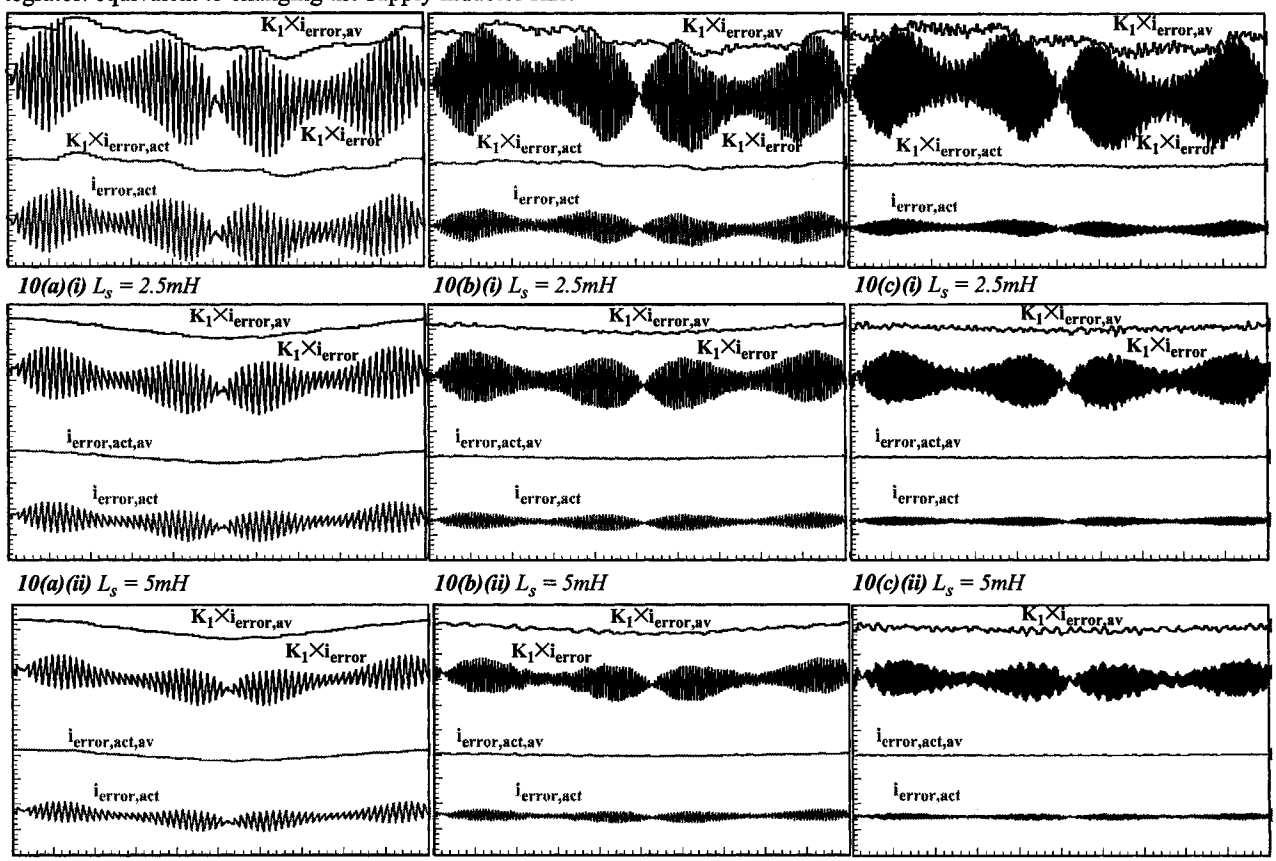
m_a at time t_i (i = ith carrier half-cycle) is determined from from the average of v_{pwm} during the previous *(i-1)th* half-cycle. This modification makes it unnecessary to use the supply voltage in the generation of the pwm waveforms.

(5) Performance of the hybrid current controller

The performance of the proposed current controller is illustrated in Fig. 9. Assuming a supply inductance of 5mH, an appropriate K_1 is chosen for each of the carrier frequencies (2,4,8 kHz). The results are obtained when: (a) the actual supply inductance is 2.5, 5 and 7.5 mH, and (b) using a reference voltage $m_a = K_2 * V_s$ and $K_2 * V_s^*$. The results show that the i_{error} and $i_{error,av}$ have a significant skewing or offset, in the case where $m_a = K_2 * V_s$. This can be attributed to m_a having a phase shift. The peak-peak current ripple varies with the supply inductance and switching frequency. In all cases where $m_a = K_2 * V_s^*$, the current error signals have a negligible average switching-cycle error. This is true even though the inductances changes +- 50%. This confirms the results from Fig. 7 where the required modulation depths were obtained irrespective of the gain of the integrator: equivalent to changing the supply inductor size.

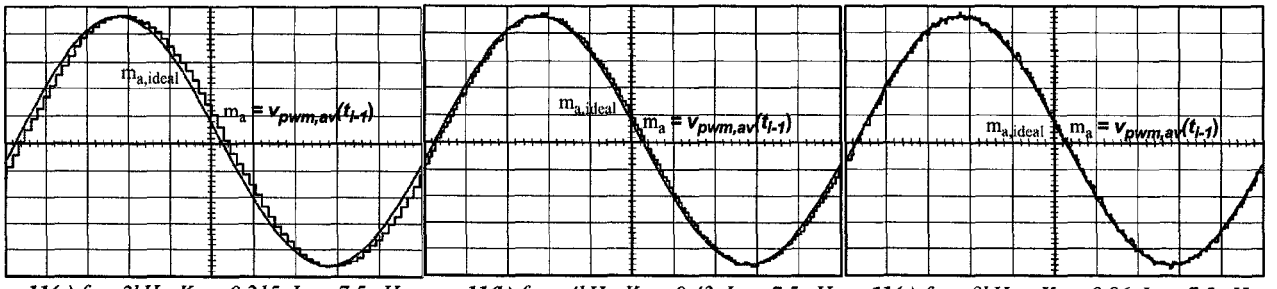
The results in Fig. 10 show the current-error and average error of the actual supply current and of the signal $K_1 * i_{error}$ using the *modified current controller*. The results again show that even if the peak-peak current error changes with switching frequency and the inductance size, the average current-error remains very close to zero with the exception of the switching frequency of 2kHz. The larger average current-error and skewing of i_{error} is caused by the phase delay in the generation of the signal m_a from v_{pwm}. A carrier half-cycle at 2kHz, represents a delay in generating m_a of 250 μS or approximately 5°. This delay in generating m_a, relative to the "ideal" reference waveform for m_a, is shown in Fig. 11 for the carrier frequencies 2, 4 and 8 kHz. At 8kHz the internally generated m_a is very close to the ideal required for the demand current.

Finally, Fig. 12 shows the actually supply current relative to the demand current using a supply inductance of 2.5 mH and a peak demand current of 10A. These results were obtained where K_1 was chosen for L_s = 5mH, and they illustrate that the current has significant errors when using a 2kHz carrier frequency, but as the switching frequency is increased these errors diminish.



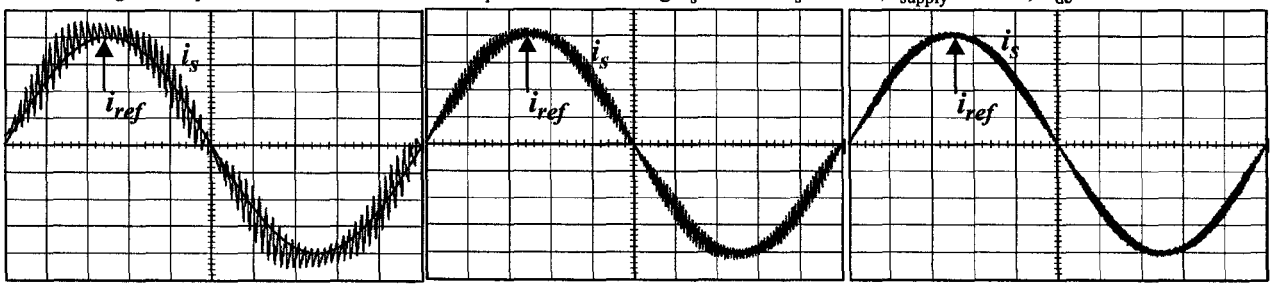
Key: top pair of waveforms: $K_1 * i_{error}$ (1 div. = 0.2V), bottom pair of waveforms: $i_{error,actual}$ in amps (1 div. = 1A), time: 2mS/div.

Fig. 10 Proposed Modified I-controller - K_1 is chosen assuming L_s = 5mH: V_s = 120 V, f_{supply} = 60 Hz, V_{dc} = 186.7 V



11(a) f_c = *2kHz,* K_1 = *0.215,* L_s = *7.5mH* *11(b)* f_c = *4kHz,* K_1 = *0.43,* L_s = *7.5mH* *11(c)* f_c = *8kHz, ,* K_1 = *0.86,* L_s = *7.5mH*

Fig. 11 Proposed Modified I-controller - K_1 is chosen assuming L_s = 5mH: V_s = 120 V, f_{supply} = 60 Hz, V_{dc} = 186.7 V



12(a) f_c = *2kHz,* K_1 = *0.215,* L_s = *2.5mH* *12(b)* f_c = *4kHz,* K_1 = *0.43,* L_s = *2mH* *12(c)* f_c = *8kHz, ,* K_1 = *0.86,* L_s = *2.5mH*

Fig. 12 Proposed Modified I-controller - K_1 is chosen assuming L_s = 5mH: V_s = 120 V, f_{supply} = 60 Hz, V_{dc} = 186.7 V

(6) Conclusions

A current controller is examined that uses the results of a carrier-based delta modulator to define an appropriate gain factor associated with the current-error signal. This current-error signal is compared with a carrier signal that is modulated by a reference voltage that is internally generated from the unipolar pwm modulator output signal. The peak-peak ripple in the current-error signal changes with the inductance size and with the switching frequency, but the average current-error is very close to zero and insensitive to these changes. The carrier half-cycle delay in generating the modulator reference signal, introduces an average current-error at low switching frequencies, with the errors diminishing at higher switching frequencies.

(7) References

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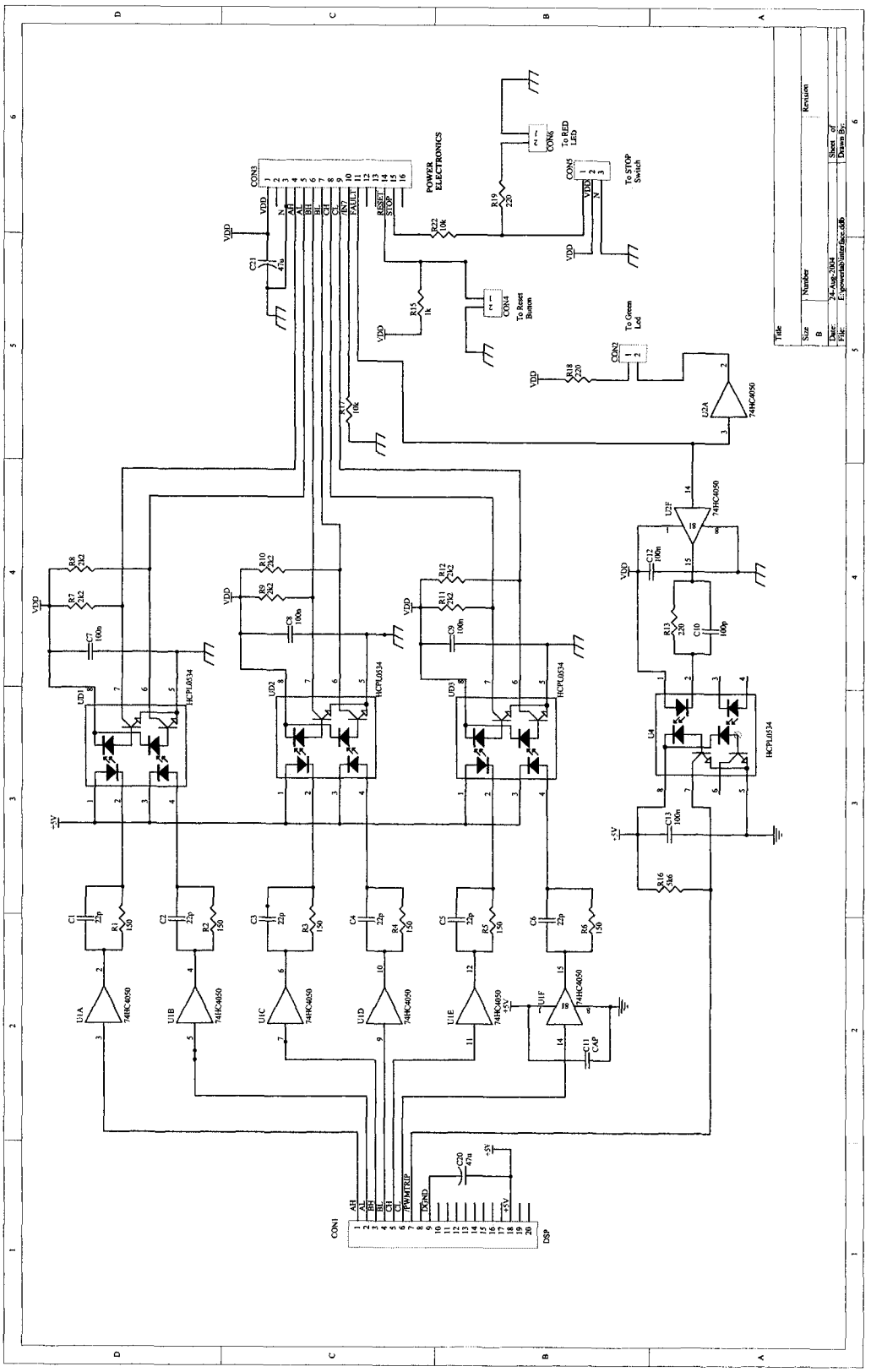
Appendix B: Schematics

The schematics for the isolation board, signal feedback board and power electronics board.



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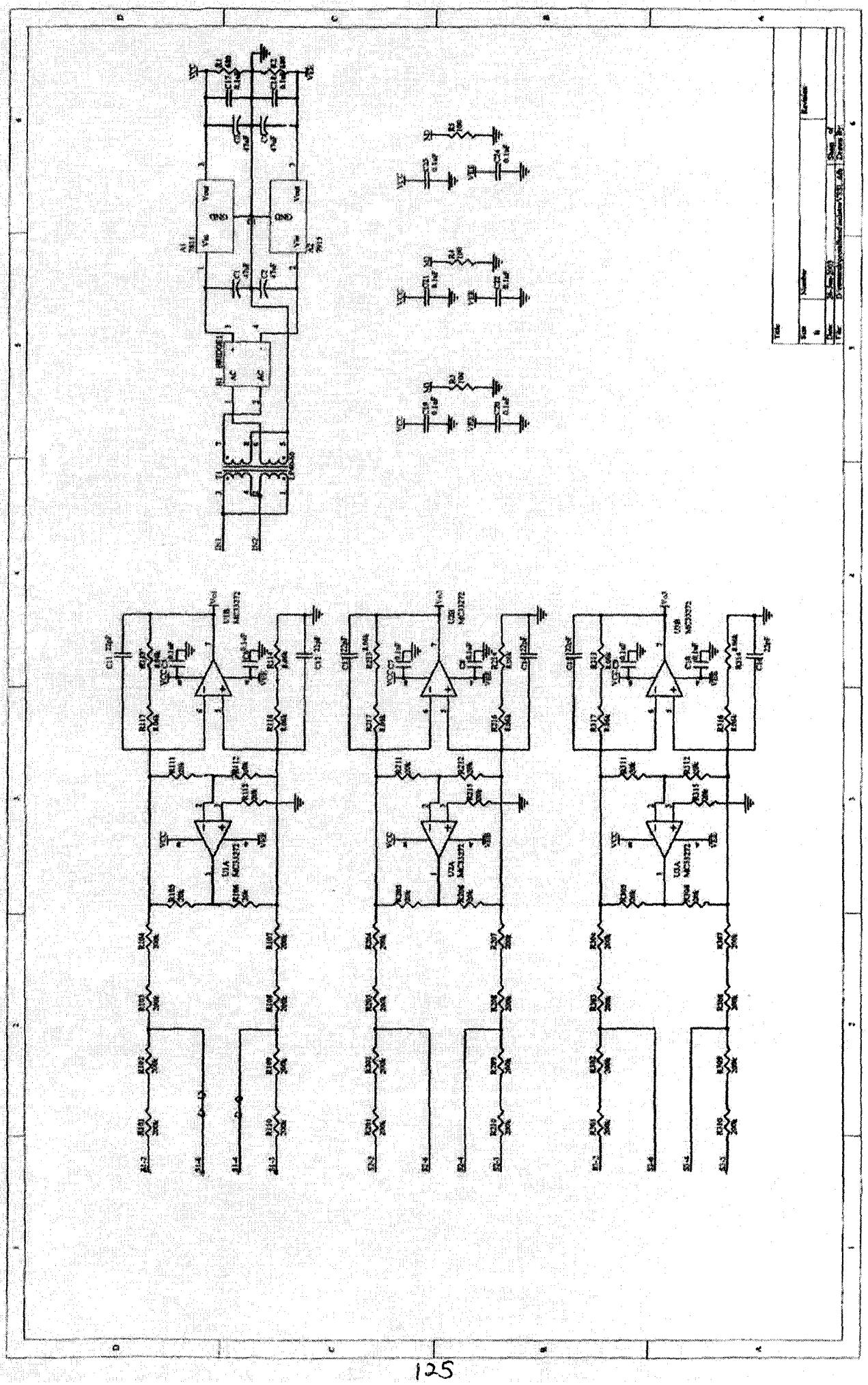

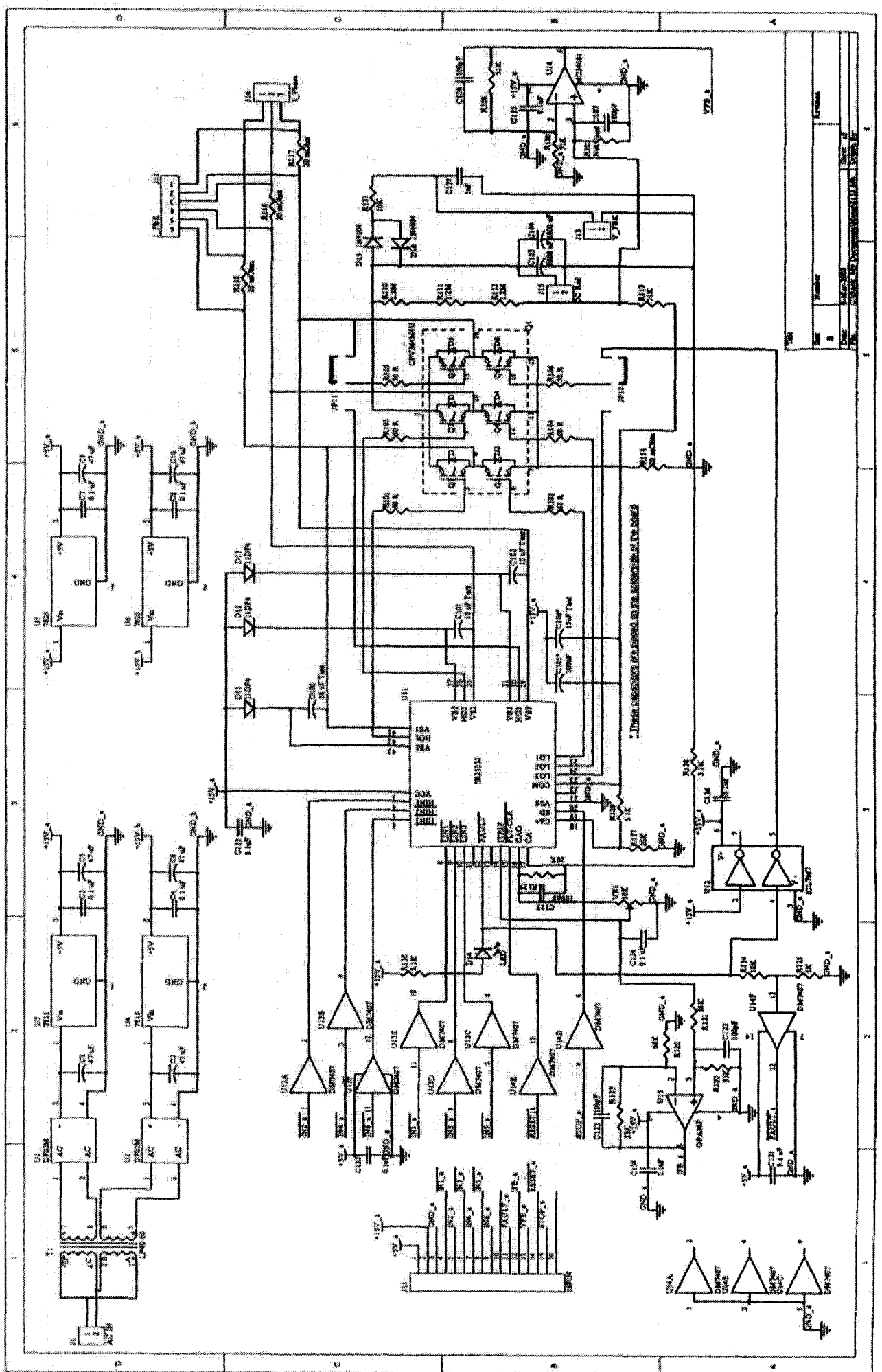

Appendix C: Control Software

```
/*************************************************************************
* Application: Generate three-phase sinewaves

* File: Main.c                                                           *
Description: main program file

* Purpose   :   Perform the new hybrid current controller

* Author    : Hao Zhang
* Version   : 1.0

* Date      : April 2004                                                 *
*************************************************************************/
* Include General System Parameters and Libraries                        *
*************************************************************************/
#include "adsp-2199x.h";
#include "signal.h";
#include "adsp-21992.h";
#include "sysreg.h";
#include "my_define.h";
#include "math.h";
/*************************************************************************
* Constants defined in this code                                         *
*************************************************************************/
#define SAW                                     1
#define Fundamental_freq        60              /*Desired fundamental frequency Hz]*/
#define PWM_Period                              H_clock*1000/2/PWM_freq
#define PWM_DT                                  Deadtime*H_clock/(1000*2)
#define PWM_TM_MAX                              ((PWM_Period/2)+PWM_DT)
#define PWM_syncwidth                           PWM_syncpulse*H_clock/1000/1000-1
#define Half_sample_rate                PWM_freq/REAL_freq/2
#define SAW_amplitude                           2*SAW
#define SAW_STEP
        (double)SAW_amplitude/((float)(Half_sample_rate));
/*************************************************************************
* Global Routines defined in this code                                   *
*************************************************************************/
        float amplitude_factor;
        float Scale_amplitude;
        float valueV,valueV1;
        float accumulator=0-SAW;
        int     switchleg=0;            //Switch A selected
        int     SAW_EDGE=0;                             //Saw-tooth increase
        int     PWM_ON,PWM_OFF;
        int     checka=0,checkb=0;
        int     ma,ma1;
        float   Pre_ma;
```

```
        float    Pre_maa1=0, Pre_maa2=0;
        float    Pre_mab1=0, Pre_mab2=0;
/*************************************************************************
***
* Global Variables defined in this code                    *
*************************************************************************
***
void   ADC_init();
void    PWM_init(int period, int DT);
void    PWM_Gen();
void    PWM_TRIP();
/*************************************************************************
* External Variables declared elsewhere
*************************************************************************/
/*************************************************************************
* Local Variables defined in this code                     *
*************************************************************************/
/*************************************************************************
* Start of program code                    *
*************************************************************************/

main()
{
        int x,i,j;
        int temp;
        float PWM_scale;

        sysreg_write(sysreg_IOPG,FIO_Page);
        io_space_write(FIO_DIR,1);

        sysreg_write(sysreg_IOPG,Clock_and_System_Control_Page);
        temp=io_space_read(PLLCTL);
        temp=temp|0x0100;                          /*bypass PLLCTL*/
        io_space_write(PLLCTL,temp);
        io_space_write(PLLCTL,0x0B50);
        for (i=0;i<512;i++) j++;
        io_space_write(PLLCTL,0xA50);       /*configure PLLCTL,
                                            HCLK=CCLK/2,CLKOUT=HCLK*/
        disable_interrupts();

        PWM_init(PWM_Period,PWM_DT);
        ADC_init();

        sysreg_write(sysreg_IOPG,IntCtrl_Page);       //Trip USR0, SYNC USR1
        x=io_space_read(IPR2);
        x=x & 0xFF00;
        x=x | 0x0001;
        io_space_write(IPR2,x);
```

```
        PWM_ON=0-(PWM_Period/2)-PWM_DT;
        PWM_OFF=(PWM_Period/2)+PWM_DT;
        ma=PWM_OFF;
        ma1=PWM_OFF;

        interrupt(SIG_INT4, PWM_TRIP);
        interrupt(SIG_INT5, PWM_Gen);

        enable_interrupts();

        while(1);
}

void PWM_init(int period, int DT)
{
        int temp;

        sysreg_write(sysreg_IOPG, PWM0_Page);

        io_space_write(PWM0_TM,PWM_Period);             /*PWM switching
                                                        frequency is 2kHz*/
        io_space_write(PWM0_DT,PWM_DT);         /*set the dead time 18.7us*/

        io_space_write(PWM0_SYNCWT,PWM_syncwidth);  /*set PWM synchronization
                                                    signal width*/
        io_space_write(PWM0_SEG,0x0003);  /*disable PWMC*/
        temp=io_space_read(PWM0_CTRL);
        temp=temp & 0xFFE7;
        temp=temp |0x0007;
        io_space_write(PWM0_CTRL,temp);   /*Enable PWM generation, PWMSYNC and
                                          double update*/
}
void ADC_init()
{
        sysreg_write(sysreg_IOPG, ADC_Page);
        io_space_write(ADC_CTRL,0x0200);  //HCLK/4
}

void PWM_TRIP()
{
        sysreg_write(sysreg_IOPG,PWM0_Page);
        io_space_write(PWM0_STAT, 0x0100);              //interrupt occurred
}

void PWM_Gen()
{
        int x,y;
        int temp, temp1;
        float feedbackV, feedbackI,valueI, valueI1,a;
```

```
float ierrora, ierrorb;
float DAC_OUTPUT,DAC_ierror;

sysreg_write(sysreg_IOPG, ADC_Page);
feedbackV=io_space_read(ADC_DATA5);          //obtain the current
                                             feedback from channel 6;
feedbackI=io_space_read(ADC_DATA1);          //obtain the voltage
                                             feedback from channel 2;
valueI1=(double)(feedbackI*2)/(float)PI;
valueV=(double)(feedbackV)/(float)PI;

ierrora=(valueI1-valueV)*2;
ierrorb=0-ierrora;

if (SAW_EDGE>0)
{
        a=accumulator-SAW_STEP;
        accumulator=a;
}
else
{
        a=accumulator+SAW_STEP;
        accumulator=a;
}
if      (SAW_EDGE==0)
{
        {       if      (accumulator<(SAW-0.1))
                {
                        {       if      (ierrora>accumulator-Pre_ma)
                                {       if      (checka==1)
                                                ma=PWM_ON;
                                        else
                                                ma=PWM_OFF;
                                }
                                else
                                {       if      (checka==1)
                                                ma=PWM_ON;
                                        else
                                        {
                                                ma=PWM_ON;
                                                checka=1;
                                                Pre_maa1=accumulator;
                                        }
                                }
                        }
                        {       if      (ierrorb>accumulator+Pre_ma)
                                        ma1=PWM_OFF;
                                else
                                {       if      (checkb==1)
```

```
                                        ma1=PWM_ON;
                                else
                                {
                                        ma1=PWM_ON;
                                        checkb=1;
                                        Pre_mab2=accumulator;
                                }
                        }
                }
                }
                else
                {
                        {       if      (ierrora>accumulator-Pre_ma)
                                {
                                        ma=PWM_OFF;
                                        checka=1;
                                        Pre_maa2=accumulator;
                                }
                                else
                                {
                                        ma=PWM_ON;
                                        checka=0;
                                }
                        }
                        {       ma1=PWM_ON;
                                checkb=0;
                        }
                SAW_EDGE=1;
                Pre_ma=0.5*(Pre_maa1-Pre_mab2);
                }
        }
}
else
{
        {       if      (accumulator>(0.1-SAW))
                {
                        {       if (ierrora<accumulator-Pre_ma)
                                        ma=PWM_ON;
                                else
                                {       if (checka==1)
                                                ma=PWM_OFF;
                                        else
                                        {
                                                ma=PWM_OFF;
                                                checka=1;
                                                Pre_maa2=accumulator;
                                        }
                                }
                        }
```

```
                        {       if (ierrorb<accumulator+Pre_ma)
                                {       if (checkb==1)
                                                ma1=PWM_OFF;
                                        else
                                                ma1=PWM_ON;
                                }
                                else
                                {       if (checkb==1)
                                                ma1=PWM_OFF;
                                        else
                                        {
                                                ma1=PWM_OFF;
                                                checkb=1;
                                                Pre_mab1=accumulator;
                                        }
                                }
                        }
                }
                else
                {
                        {       if (ierrorb<accumulator+Pre_ma)
                                {
                                        ma1=PWM_ON;
                                        checkb=1;
                                        Pre_mab2=accumulator;
                                }
                                else
                                {
                                        ma1=PWM_OFF;
                                        checkb=0;
                                }
                        }
                        {
                                ma=PWM_OFF;
                                checka=0;
                                //Pre_maa2=accumulator;
                        }
                        SAW_EDGE=0;
                        Pre_ma=0.5*(Pre_maa2-Pre_mab1);
                }
        }
}
sysreg_write(sysreg_IOPG,PWM0_Page);

io_space_write(PWM0_CHA,ma);
io_space_write(PWM0_CHB,ma1);

return;
}
```