Electromagnetic Transient Simulation of CIGRÉ DC Grid Test System with Hybrid Converter Topologies

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***Abstract*—Voltage source converter (VSC) based HVDC projects are being increasingly built and operated globally, providing the potential to construct a meshed DC supergrid. The CIGRÉ DC grid test system is a benchmark for research and analysis with power system topologies and parameters. This paper presents the electromagnetic transient simulation using detailed switching devices for the complete test system modeling composed of multiple converter topologies, including two-level (2L) converters, three-level neutral-point-clamped (3L-NPC) converters, modular multi-level converters (MMCs) with up to 401 levels, and four-quadrant (4Q) DC-DC converters in PSCAD/EMTDC®. This paper proposes the scheme to combine the piecewise linearized tangential curve fitting of IGBT and diode characteristics with the Thévenin equivalence based MMC modeling scheme to increase the accuracy, which can also present the power losses of the IGBT modules. Dynamic analyses, including AC and DC faults, are conducted presenting the results from various converter stations.**

***Index Terms*—DC-DC converter, Electromagnetic transient simulation, HVDC grid, Insulated gate bipolar transistor (IGBT), Modular multi-level converter (MMC).**

I. Introduction

With voltage-source converter (VSC) based HVDC projects increasingly operated globally, the integration of DC transmission grid becomes possible, where different DC voltage ratings and converter structures exist [1]. The higher energy efficiency, controllability and the merits of applying DC cables make DC grid a primary candidate to construct the multi-continent supergrid of the future, which provides the transmission solution for the remote on-shore and off-shore renewable resources and enhances the integration of the electricity market with higher energy efficiency.

The CIGRÉ working groups have designed a DC grid test system, as the common reference system for the study of HVDC grid [2]. The test system integrates three HVDC systems, which are either connected indirectly through AC buses at the converter stations or connected directly through DC/DC converters. In total, the test system contains 11 AC-DC converter stations, 2 DC-DC converter stations, as shown in Fig 1 [2].

Many previous works focus on the power flow of the test system using the average value model or the transient analysis of a portion of the test system [3]–[6]. Using averaged model is sufficient for testing upper-level control of converters, such as active power and reactive power control, and power flow analysis. Accurate transient analysis under faults and the verification of a complete control system including gate signal controls requires a more detailed model, where discrete switching devices, such as insulated gate bipolar transistor (IGBT) modules are modeled. In [2], all the converters are modular multi-level converters (MMCs) using the average value model. The averaged model used in [2] is not accurate and adequate for electromagnetic transient analysis due to the many simplifying assumptions, such as the perfect balance of the sub-module (SM) capacitors in MMC.

This paper proposes the scheme of applying multiple tangential curves to piece-wise linearize the output and forward characteristics of IGBT and diode, in order to increase the MMC modeling accuracy. The dynamic power losses of the IGBT modules are calculated and presented during the simulation. A discharge resistor is added in parallel with the SM capacitor in MMC. The modeled MMC contains up to 400 SMs in one arm, providing 401 levels.

The contribution of this work is to utilize discrete switching devices to model the complete CIGRÉ DC test system which contains two-level (2L) converters, three-level neutral-point-clamped (3L-NPC) converters, MMCs, and four-quadrant (4Q) DC-DC converters on PSCAD/EMTDC®. The reasons for using hybrid converter topologies are the followings:

1) The establishment of a DC grid can be accomplished by connecting existing HVDC projects step-by-step. MMC provides many advantages over other converter topologies, such as extremely low harmonics, low switching frequency, high modularity, etc.; however, due to the practical constraints of cost, reliability, maturity, etc., other HVDC converter topologies would still be constructed and operated, and can be a significant portion of the DC grid.
2) The usage of hybrid converter topologies complicates the entire system to a great extent, which creates higher demandings of upper-level control and protection of the system. The challenges prove to be an advantage for control and protection algorithm testing and verification purpose.
3) Detailed model of MMC is time-consuming on PC, even when Thévenin equivalence type scheme is applied for node elimination [7], while the execution speed for 2L, 3L-NPC is much faster. However, it should not be a barrier for using detailed model for any converter topologies, when necessary. The parallel processing al-

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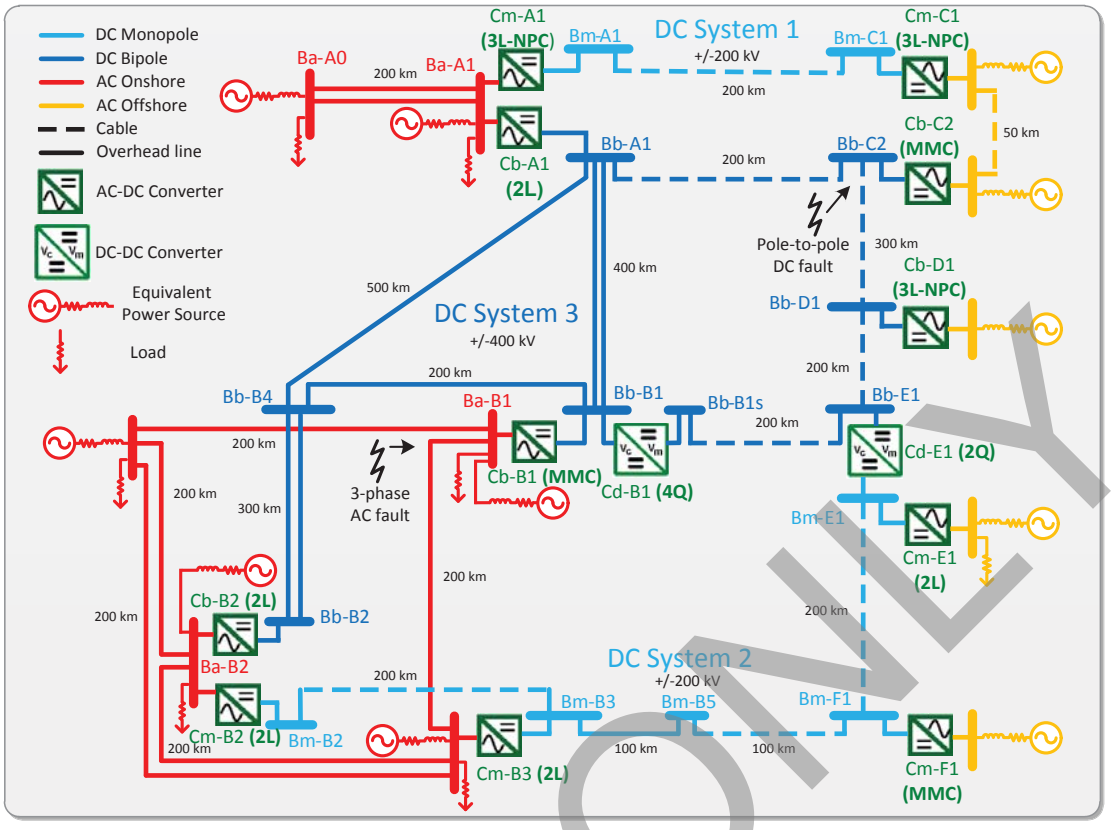

Fig. 1. Topology of CIGRÉ DC grid test system [2].

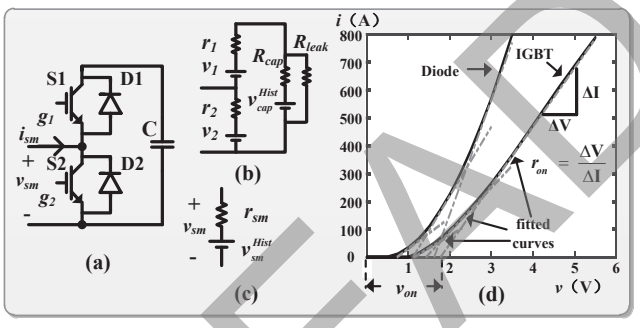

Fig. 2. SM modeling scheme: (a) half-bridge structure, (b) circuit model, (c) Thévenin equivalence model, and (d) output and forward characteristics of IGBT and diode.

gorithm along with the corresponding hardware devices can greatly accelerate the simulation speed. This work is focused on the simulation of the entire CIGRÉ DC grid test system on PSCAD/EMTDC®.

The paper is organized as follows: Section II presents the proposed MMC model in detail, the converter topologies and the control schemes briefly; Section III shows the steady-state results of MMC, and transient results and analysis of AC and DC faults, followed by the conclusions in Section IV.

II. MMC Modeling Scheme, Converter Station Topologies, and Control Strategies

Because an MMC station can contain up to thousands of SMs, the simulation by directly using discrete switching devices is extremely slow due to the numerous circuit nodes. The interface of using equivalent voltage source or a voltage source in series with a resistor for the converter arm with delay is generally used to accelerate the simulation speed [7]–[9]. With such interface, the calculation for the external circuit is similar to that of a 2L converter.

In [7], two state resistor model for IGBT module is used with the Thévenin equivalence method, which is not able to reflect output and forward characteristics of IGBT and diode, respectively, and the power losses for IGBT modules are not taking account into the simulation. For real-time hardware emulation of MMCs on FPGAs, a detailed transient electro-thermal model has also been proposed [9].

Fig. 2 (a)-(c) show the SM structure, corresponding circuit model, and the Thévenin equivalence for the proposed model. A leakage resistor R_{leak} is added in parallel with the capacitor to model the capacitor current leakage phenomenon. As shown in Fig. 2 (d), this work utilizes three tangential curves to fit the characteristic curves of FZ400R33KL2C_B5 IGBT module from the datasheet [10], which is more accurate than simply using one set of values of series-connected voltage source v_{on} and resistor r_{on} representing the threshold voltage and slope resistance. Multiple IGBT modules (5 in this work) can be connected in parallel to provide sufficient current rating.

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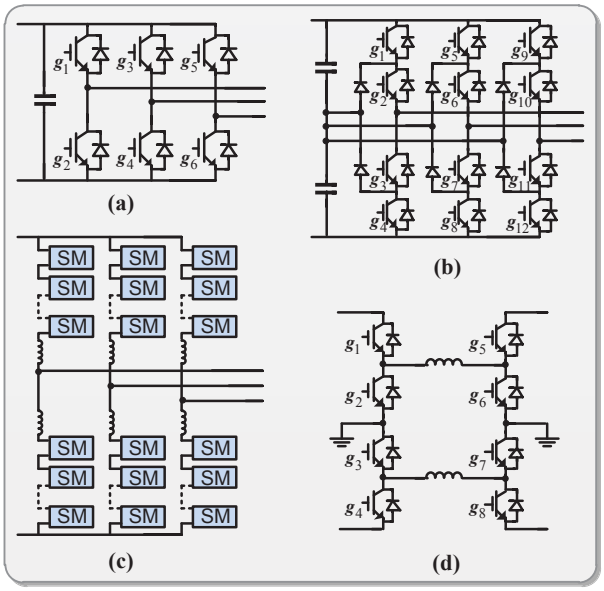

Fig. 3. Structures of power converters: (a) two-level converter, (b) three-level neutral-point-clamped converters, (c) modular multi-level converter, and (d) four-quadrant DC-DC converter.

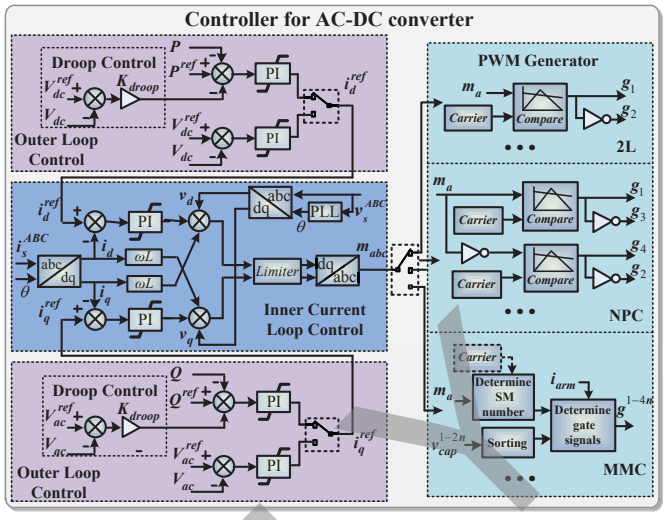

Fig. 4. Control schemes for AC-DC converters.

Taking account of the value of off-state resistance, which is determined by the leakage current of IGBT module, r_1, v_1, r_2, and v_2 for the upper and lower IGBT modules, respectively, all have four sets of values, determined by the gate signals and SM current i_{sm}. The SM output voltage $v_{sm}(t)$ is calculated as:

$$v_{sm}(t) = r_{sm} i_{sm}(t) + v_{sm}^{Hist}(t - \Delta t), \tag{1}$$

where

$$r_{sm} = \frac{r_2(r_1(R_{cap} + R_{1eak}) + R_{cap}R_{1eak})}{(r_1 + r_2)(R_{cap} + R_{1eak}) + R_{cap}R_{1eak}}, \text{and} \tag{2}$$

$$v_{sm}^{Hist}(t-\Delta t) = \frac{(v_{cap}^{Hist}(t - \Delta t) - v_1 - v_2)(R_{1eak} + R_{cap})r_2}{(r_1 + r_2)(R_{cap} + R_{1eak}) + R_{cap}R_{1eak}} + v_2, \tag{3}$$

R_{cap} and $v_{cap}^{Hist}(t - \Delta t)$ is the equivalent resistance and the history voltage term for the capacitor using Trapezoidal rule. Lookup tables are used to store the pre-calculated expressions in (2) and (3) with limited combinations for (r_1, v_1, r_2, v_2), which can effectively minimize the calculation effort during the simulation. User defined components with Fortran programming are used in PSCAD/EMTDC® to implement the proposed model. Once the arm current was obtained in PSCAD/EMTDC®, the power losses of the IGBT module, composed of one IGBT and one diode connected in anti-parallel, were calculated with the value of the threshold voltages and slope resistances.

Fig. 3 presents the converter circuit topologies of 2L, 3L-NPC, MMC AC-DC converters, and 4Q DC-DC converter. For MMC, the half-bridge topology is applied, and the inductor is connected in series with the SMs to suppress the circulating current. For the DC-DC converter, the 4Q converter topologies is used for the Station Cd-B1, which is used to control the power flow in the DC System 3 [3]. Since the power flow may reverse requiring the change of the voltage conversion between buck and boost, four-quadrant performance is required for the converter station. While for the Station Cd-E1, a 2Q converter is sufficient, which can be either the right or left part along with inductor in Fig. 3 (d). Except for the MMC explained in the previous section, all the converters are modeled exactly as the topologies shown in Fig. 3, with the IGBT and diode model provided by PSCAD/EMTDC® library. Therefore the entire system is based on the model of individual switching devices instead of averaged model for detailed and accurate transient analysis.

The control scheme for AC-DC converters is illustrated in Fig. 4, which is composed of outer loop control, the inner current loop control and the pulse width modulation (PWM) generator [1], [2], [11]. The droop control is applied to the converters connecting to slack buses for optimal power sharing. The overall upper-level control is the same for the three AC-DC converters, however, the lower level PWM signal generation processes are different. Among them, the control for MMC is the most complex due to the requirement of capacitor voltage balancing. The phase disposition method is used in this work, since it works for both low and high number of converter levels [12]. For the low-level MMC, PWM waveform for the AC voltage output can be clearly identified, while for high-level MMC, the PD-SPWM is equivalent to the staircase modulation. The control for the 4Q DC-DC converter is straightforward by using PI controller and SPWM similar to 2L converter.

III. Transient Simulation Results and Analysis of the CIGRÉ DC Grid Test System

As shown in Fig. 1 for this work, Stations Cb-B1 and Cb-C2 are using MMC with 401 levels; Station Cm-F1 is using MMC with 201 levels; Station Cm-A1, Cm-C1, and Cb-D1 are using 3L-NPC converter; Other AC-DC stations

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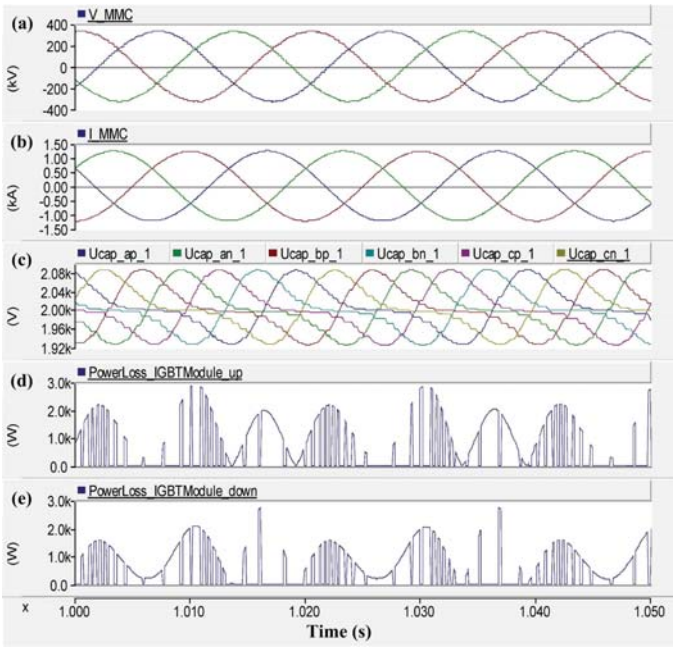

Fig. 5. Steady-state results of MMC of Station Cb-C2: (a) AC-side voltage, (b) AC-side current, (c) capacitor voltages of the first SM in 6 arms, (d) power loss of the upper IGBT module ($\mathbf{S}_1$ and $\mathbf{D}_1$) in the first SM of phase A upper arm, (e) power loss of the lower IGBT module ($\mathbf{S}_2$ and $\mathbf{D}_2$) in the first SM of phase A upper arm.

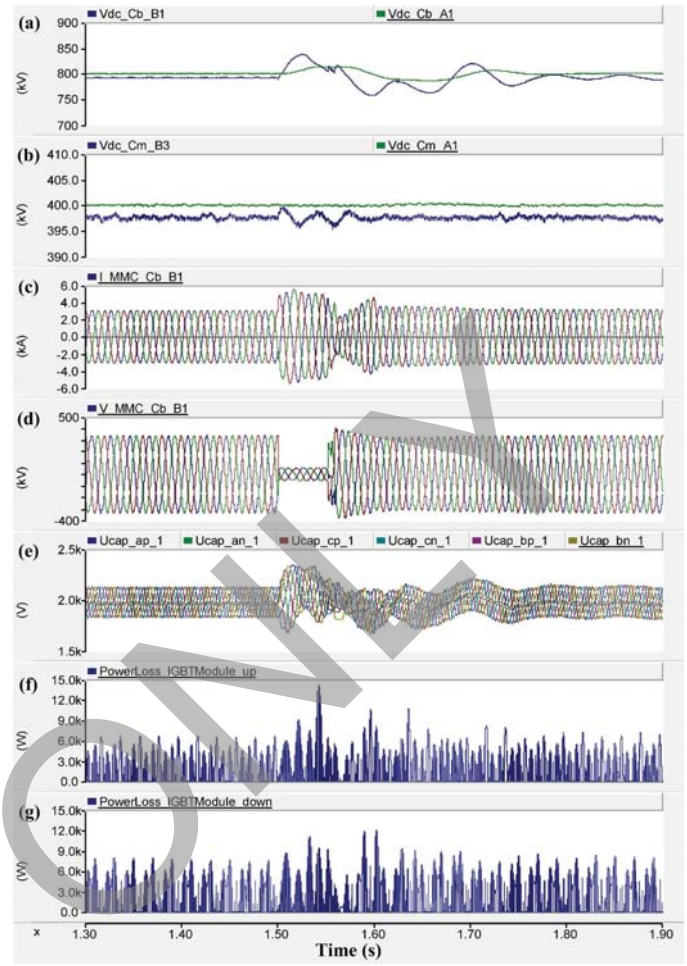

Fig. 6. AC fault results: (a) DC voltage at Stations Cb-A1 and Cb-B1, (b) DC voltage at Stations Cm-B3 and Cm-A1, (c) MMC AC-side voltage at Station Cb-B1 (d) MMC AC-side current at Station Cb-B1 (e) capacitor voltages of the first SM in 6 arms at Station Cb-B1, (f) power loss of the upper IGBT module at Station Cb-B1, and (g) power loss of the lower IGBT module at Station Cb-B1.

are using 2L converter. MMC Stations Cb-B1 and Cb-C2, are using symmetrical monopolar structure, while other converter stations in DC System 3 are using bipolar structure. The transmission lines and cables are modeled using frequency-dependent line model. It takes 89s to simulate a 1s run with 20μs as the time-step for the complete DC grid test system on PC using Intel® Xeon CPU E5-2609. The simulation results for steady-state, AC fault, DC fault of the system, especially for MMC, are presented in the following sub-sections.

A. MMC Steady-State Results

Fig. 5 presents the steady-state results of MMC at Station Cb-C2. Since the number of levels for the MMC is very high, the AC-side voltage and current waveforms are almost sinusoidal. The capacitor voltage waveforms of the first SM in all 6 arms are presented, which are close to each other with a phase-shift. One of the significant features of the proposed model is the ability to present the conduction power losses of each IGBT modules with sufficient accuracy during the simulation, which have been shown in Fig. 5 (d) and (e). Admittedly, the proposed model cannot present the switching power losses. However, since the switching frequency is normally lower for MMC, the error is small.

B. AC Fault Results

The three-phase AC fault occurs at Bus Ba-B1, lasting for 0.05s from 1.5s of the simulation. Fig. 6 (a) and (b) present the DC voltage at Stations Cb-B1, Cb-A1, Cm-B3, and Cm-A1, during the fault. As expected, the Station Cb-B1, which is closest to the fault location and displays the largest disturbance in DC voltage. The AC fault effect for Station Cm-A1 in DC System 1, which does not have a direct connection to DC System 3, is not noticeable. Station Cm-B3, which has a direct linkage to the fault location through the AC system has a smaller effect than that of the Station Cb-b1 which is connected in DC System 3. The transient waveforms of the MMC AC-side voltage and current, as well as the capacitor voltages, are also shown in Fig. 6. The steady-state performance of the MMC can be restored after 0.1s, though the DC voltage of the converter station oscillates slightly until around 1.8s. The IGBT module power losses in the first SM of phase A upper arm are shown in Fig. 6 (f) and (g).

C. DC Fault Results

The pole-to-pole DC fault happens from 1.0s of the simulation, lasting for 0.05s at Bus Bb-C2. The DC fault has the more serious effect on HVDC grid and requires a longer time to restore stability, as shown in Fig. 7. The DC fault currents at Stations Cb-C2 and Cb-D1 are very high, which

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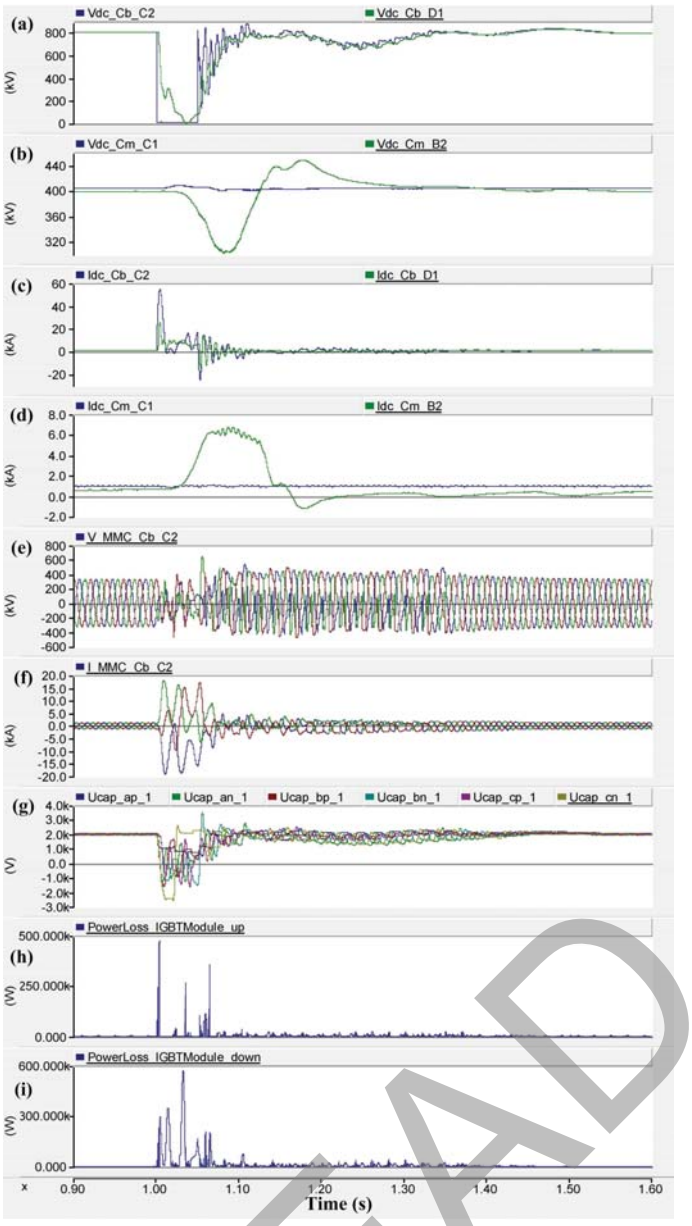

Fig. 7. DC fault results: (a) DC voltage at Stations Cb-C2 and Cb-D1, (b) DC voltage at Stations Cm-C1 and Cm-B2, (c) DC current at Stations Cb-C2 and Cb-D1, (d) DC current at Stations Cm-C1 and Cm-B2, (e) MMC AC-side voltage at Station Cb-C2, (f) MMC AC-side current at Station Cb-C2, and (g) capacitor voltages of the first SM in 6 arms at Station Cb-C2, (h) power loss of the upper IGBT module at Station Cb-C2, and (i) power loss of the lower IGBT module at Station Cb-C2.

are more than 50kA and 20kA, respectively. Station Cm-b2 in DC System 2 far away from the DC fault, is still significantly affected by the DC fault. On the other hand, the Station Cm-C1, which is 50km away connected by AC cables is effected less by the fault. This is because of the galvanic isolation provided by the transformers in both converter stations. The DC-DC converter in Station Cd-E1 using the 2Q topology does not provide the galvanic isolation between DC System 2 and DC System 3, which propagates the fault. The distortion of the capacitor voltages of SMs is also much serious compared to the case of AC fault. Fig. 7 (h) and (i) show the IGBT module power losses in the first SM of phase A upper arm. The IGBT modules may be damaged by the DC fault current and corresponding power losses. In practical design, DC circuit breaker for the converter station or the bypass switches for the SMs shall be triggered to avoid the damage.

IV. Conclusion

This work focused on the electromagnetic transient simulation of the CIGRÉ DC grid test system composed of hybrid converter topologies with detailed switching-device level model. The accurate transient waveforms for the converters, the capacitor voltages of MMCs, and the power losses of the switching devices, etc., are presented, which verifies the effectiveness of the proposed MMC model using multiple tangential curves to fit the characteristics of switching devices.

As shown in the results, AC and DC faults can seriously threaten the safe operation of the DC grid system. The simulation using accurate, detailed and complete EMT model provides a powerful tool for the further study and analysis of the DC grid, such as the performance verification of control system under faults, and threshold value setting for protection system, etc. More detailed electrical machine models as well as other elements can be added to the test system for detailed dynamic analysis in future research.

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