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Real-Time Simulation Technologies for Power Systems Design, Testing, and Analysis

IEEE PES Task Force[1] on Real-Time Simulation of Power and Energy Systems
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ABSTRACT This task force paper summarizes the state-of-the-art real-time digital simulation concepts and technologies that are used for the analysis, design, and testing of the electric power system and its apparatus. This paper highlights the main building blocks of the real-time simulator, i.e., hardware, software, input-output systems, modeling, and solution techniques, interfacing capabilities to external hardware and various applications. It covers the most commonly used real-time digital simulators in both industry and academia. A comprehensive list of the real-time simulators is provided in a tabular review. The objective of this paper is to summarize salient features of various real-time simulators, so that the reader can benefit from understanding the relevant technologies and their applications, which will be presented in a separate paper.

INDEX TERMS Digital real-time simulation (DRTS), digital simulators, hardware-in-the-loop (HIL) simulation, power engineering, power system transient simulation, real-time systems.

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NOMENCLATURE

T_e Execution time.
t_n Time step.

I. INTRODUCTION

DIGITAL real-time simulation (DRTS) of the electric power system is the reproduction of output (voltage/currents) waveforms, with the desired accuracy, that are representative of the behavior of the real power system being modeled. To achieve such a goal, a digital real-time simulator needs to solve the model equations for one time-step within the same time in real-world clock [1], [2]. Therefore, it produces outputs at discrete time intervals, where the system states are computed at certain discrete times using a fixed time-step.

DRTS is a technique for the transient simulation of power systems using digital-computer time-domain solution (e.g., using an electromagnetic transient-type approach) [3]–[6]. Systems are represented by taking advantage of the component models available in the library of the software tool using a graphical interface and simulated on a hardware platform employing parallel computation.

Two situations can arise depending on the time required by the simulation platform to complete the computation of state outputs for each time-step (Fig. 1): 1) if the execution time, T_e, for the simulation of the system is shorter or equal to the selected time-step, the simulation is considered to be real-time [Fig. 1(a)]; and 2) if T_e is greater than its time-step size for one or more time-steps, overruns occur and the simulation is considered as nonreal-time or offline. In the latter case, either the time-step can be increased or the system model can be simplified to run it in real time.

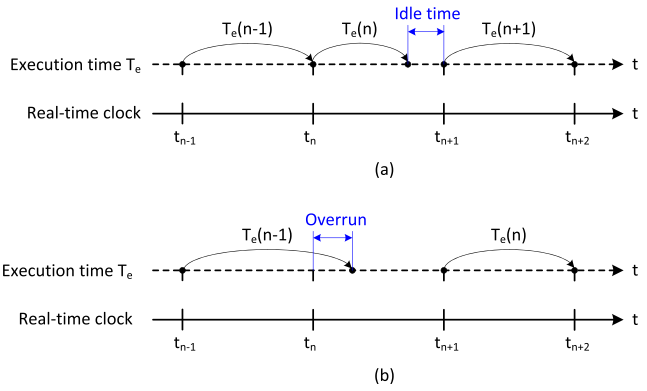

FIGURE 1. Illustration of real-time and offline simulation. (a) Real-time simulation. (b) Non-real-time simulation.

The aim of this paper, therefore, is to given an overview of the state-of-the-art in real-time simulation technologies for power systems design, testing, and analysis. The main components and concepts as well as an overview of commonly available solutions are presented in this review paper.

The rest of this paper is organized as follows. Section II introduces different categories of real-time simulators, and in Section III, their evaluation over the last few years is presented. Their computing capabilities are discussed in Section IV, followed by the description of typical

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characteristics of the systems in Section V. Finally, the conclusion is drawn in Section VI.

II. CATEGORIES OF DIGITAL REAL-TIME SIMULATION

DRTS applied to the domain of power systems can be classified into two categories: 1) fully digital real-time simulation (e.g., model-in-the-loop, software-in-the-loop, or processor-in-the-loop), and 2) hardware-in-the-loop (HIL) real-time simulation. A fully digital real-time simulation requires the entire system (including control, protection, and other accessories) to be modeled inside the simulator and does not involve external interfacing or inputs/outputs (I/Os). On the other hand, the HIL simulation refers to the condition where parts of the fully digital real-time simulation have been replaced with actual physical components. The HIL mode of the simulation proceeds with the device-under-test or hardware-under-test (HuT) connected through input-output interfaces, e.g., filters, digital-to-analog and analog-to-digital converters and signal conditioners. Limited real-time controls of the simulation can be executed with the user-defined control inputs, for example, closing or opening of switches to connect or disconnect the components in the simulated power system.

If the HIL system involves real controller hardware that interacts with the rest of the simulated system, it is called controller hardware-in-the-loop (CHIL). It is also used for rapid controller prototyping. In this method, no real power transfer takes place and the power system is modeled as a virtual system inside the simulator, and the external controller hardware exchanges controller I/Os with the system inside the simulator. In general, a newly designed/developed controller is tested using this method, where the controller takes feedback signals from the simulator and processes them to produce the required output signals, which are then sent back to the system (inside the simulator). Such a setup of a controller prototyping or CHIL arrangement is shown in Fig. 2, where a power electronic converter is modeled inside the simulator and the real controller is connected to it through I/Os.

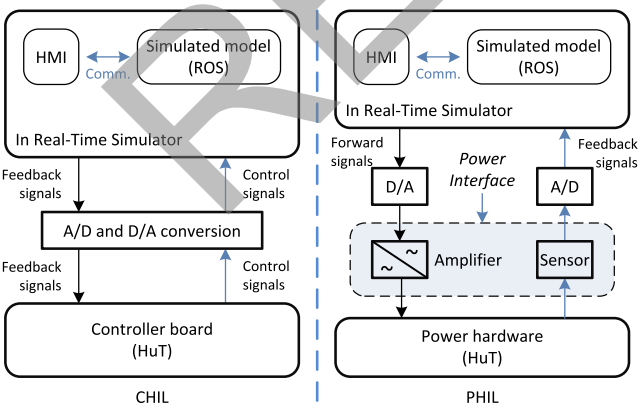

FIGURE 2. Basic HIL simulation concept for CHIL and PHIL.

Any HIL simulation involving power transfer to or from the HuT is known as power hardware-in-the-loop (PHIL) (Fig. 2). In this case, part of the power system is internally simulated and the other part is the real hardware power apparatus connected externally. A power source or sink (connected through the PHIL interface) is needed for this setup, which will either generate or absorb power. Reference signals are generated based on the solution of the virtual system inside the real-time simulator and are sent to the power amplifier that produces voltages or currents to be applied to the HuT. Feedback signals obtained from the voltage/current measurements of the HuT are appropriately scaled and brought back to the simulator to complete the simulation loop.

An example of such simulation could be the real-time testing of machines, converters [7], fault-current limiters, or any other electrical equipment. Testing of protection devices, such as relays, may require voltage or current amplifiers for HIL-based testing; however, no power is exchanged in that case [8], [9]. The use of an amplifier is mainly for the device to sense the actual voltage and/or current signals.

In general, a fully digital simulation is often used for understanding the behavior of a system under certain circumstances resulting from external or internal dynamic influences, whereas an HIL simulation is used to minimize the risk of investment through the use of a prototype once the underlying theory is established with the help of a fully DRTS.

III. EVOLUTION OF DIGITAL REAL-TIME SIMULATORS

Using parallel processor-based digital technologies and improved numerical analysis techniques with less computational burden, a number of digital real-time simulators have been proposed and tested [10]–[20]. Initial real-time simulators were based on the digital signal processor (DSP) [10]–[12], reduced instruction set computer (RISC) [13]–[16], and complex instruction set computer [17] technologies; however, the use of general-purpose processors as the computation engine has become an attractive option because of their lower cost and faster development cycle [21]. Development of a clustered system, using off-the-shelf digital processors, is based on advanced communication networks, which is becoming a growing trend for the development of the DRTS.

The first commercial real-time digital simulator (RTDS) was demonstrated by RTDS Technologies Inc. in 1991 using DSPs [13]. It was interfaced to the controller of a high voltage direct current converter to assess its performance. A combination of both analog and digital parts was used in that simulator. Since then, this simulator has evolved and become one of the widely used commercial RTDSs. The first small-scale digital real-time simulator for the real-time test of the power system equipment based on a standard multipurpose parallel-computer system, known as the digital transient network analyzer (DTNA), is presented in [16]. The DTNA could simulate electromagnetic transient phenomena up to 3 kHz, ac/dc interactions, electromechanical transients, and similar long-time phenomena. A wide variety of components, equipment, and controllers, including power electronic-based controllers, can be modeled and simulated using this simulator.

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No fully digital real-time simulator was possible in a standard computer before 1996, when Électricité de France introduced their first real-time simulator ARENE [18]. It was capable of simulating the high-frequency phenomenon in a standard, multipurpose parallel computer. Another PC-based real-time simulator, NETOMAC [19], [20] from SIEMENS, was used to simulate large power grids. Almost at the same time, another general-purpose processor-based real-time simulator from OPAL-RT Technologies Inc. [21]–[25] was introduced, which uses the MATLAB/Simulink as the main modeling tool for the simulation. Almost a similar approach of using a standard PC for real-time simulation and control was adopted by dSPACE [26], which uses general-purpose processors and MATLAB/Simulink as the modeling package, though their older generation simulators used DSPs. HYPERSIM [27]–[29] is another fully digital real-time simulator for the analysis of the electromagnetic and electromechanical transients in large and complex power systems and originally developed by IREQ, the Hydro-Quebec's research institute.

Other than the aforementioned real-time simulators, custom laboratory-scale real-time simulators have been presented in the literature. These real-time simulators use a combination of hardware and software mostly to serve specific requirements. field-programmable gate arrays (FPGAs) [30]–[35] and graphics processing unit (GPU) [43] are two such digital processors that are gaining foundation as a computation hardware for real-time simulation. User-friendly block coding, automatic code generation capability, and interfacing capability with Simulink allows these hardware to be used as an auxiliary platform of large simulators that allow to model and then to simulate a system within a time-step of nanoseconds while the main simulation runs at a larger time-step (in microseconds) [35]. These are other promising avenues for future exploration in the field of real-time simulation of the power system.

IV. COMPUTING CAPABILITIES OF REAL-TIME SIMULATORS

A real-time simulator needs to solve a grid-scale model by roughly 50 μs or a smaller time-step (for suitable resolution in 50-/60-Hz power systems) to reproduce transients faithfully. Computing capability may be defined as the product of the number of nodes/buses in the simulated power network and the number of time steps taken per second. For a 50-/60-Hz ac power network, this capability corresponds to a large node/bus count and fairly low speed; however, for power-electronic systems operating with higher switching frequencies, smaller time-steps are required. If controlled digitally, high-frequency switching circuits may operate with a microcontroller having an internal clock speed with periods of 1 μs to 10 ns. A simulation of such a system may require more computing capability and the ability to simulate with a very small time-step. Despite the high-speed internal dynamics of the power electronics-based apparatus, the system-level interactions may not require a very small time-step. For simulating fast and slow subsystem transients, a multirate cosimulation approach can be adopted.

Fig. 3 shows the relationship between computing nodes and time-step requirements for different systems. The power system simulation may be sufficient at a comparatively larger time-step, and for a constant computing power, it allows a larger system, whereas for power electronics simulation, smaller time-steps are necessary, resulting in a smaller system for the same computation power.

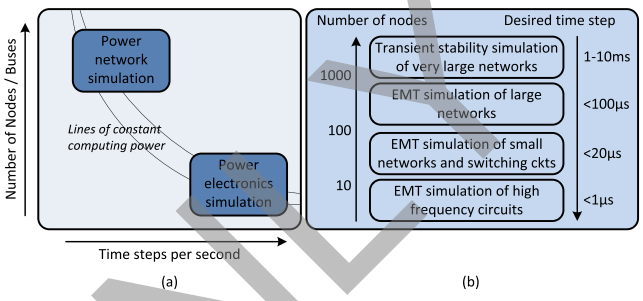

FIGURE 3. Illustration of (a) computing capability requirements for different types of systems and (b) time-step requirement for different types of simulation.

A real-time simulator is often configured to be scalable. The increment of computing power is possible by adding rack-mount units that require data communication between racks. Individual computing units operate in parallel, offering a reasonable scaling property; however, communication adds time delay. Communication bottlenecks are minimized by exploiting the traveling wave properties to decouple the solutions of the network subsystems that are separated by transmission lines of appropriate length that is consistent with the simulation step interval [13]. Power processors or other hardware such as general-purpose central processing units (CPUs) work in parallel by sharing common memories or buses to minimize the communication latencies.

V. CHARACTERISTICS OF REAL-TIME SIMULATORS

A. COMMON FEATURES OF REAL-TIME SIMULATORS

Most DRTS have the following common characteristics:

1) multiple processors operate in parallel to form the target platform on which the simulation runs in real time;
2) a host computer is used to prepare the model offline and then compile and load it on the target platform. Host computers are also used for monitoring the results of real-time simulation;
3) I/O terminals to interface with external hardware;
4) a communication network to exchange data between multiple targets when the model is split into multiple subsystems. A separate communication link is required for data exchange between the host and the target.

Hosts, targets, and communication links may sometimes be called otherwise by different vendor-specific names.

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B. LARGE-SCALE AND COMMERCIAL REAL-TIME SIMULATORS

This section describes the characteristics of two widely used large and scalable RTDSs. We refer to them as Type-A and Type-B simulators.

1) HARDWARE

For most of the simulation environments, hardware directly influences the computing capability of the simulator. Hardware for different real-time simulators evolved with time, and in this paper, an effort has been made to describe the current state-of-the-art hardware.

Fig. 4 shows the hardware architecture of a Type-A simulator [13] that employs custom hardware assembled in units called racks. The racks contain several slot-mounted processor cards known as PB5 cards, each containing two PowerPC RISC processors operating in parallel, and serves as the main computational engine. A maximum of six processor cards or 12 processors can be put into one rack and the maximum number of nodes that can be simulated using each card are 72. The processor card also allows two network solutions (each network solution requires one processor) to be included in one rack to represent two subsystems with 72 nodes each. Larger networks with more nodes/subsystems can be represented using additional racks.

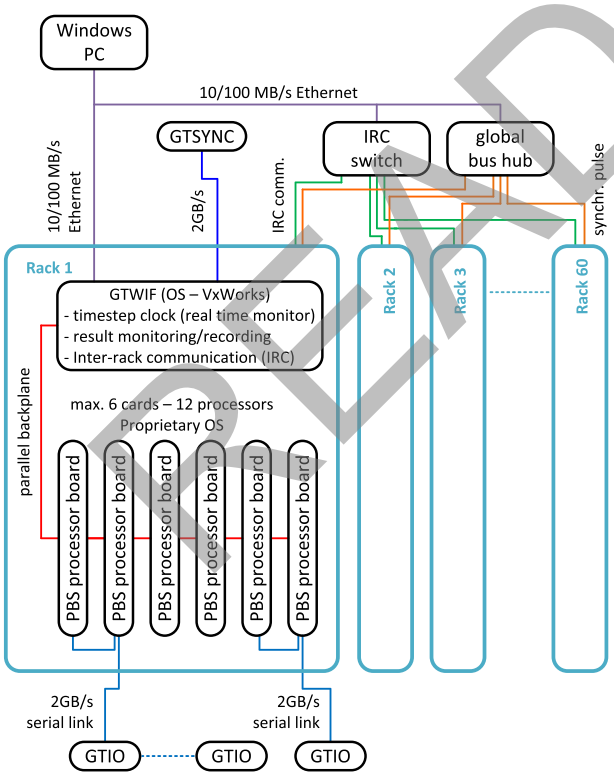

FIGURE 4. Hardware architecture of RTDS simulator.

In addition to the main processor cards, each simulator rack of this type contains a workstation interface card known as a GTWIF card. The GTWIF is an IBM PPC405-based processor card used for the Ethernet communication between the host (i.e., a Windows-based PC) and the target (i.e., the racks). The GTWIF also provides communication links between racks as well as enforces synchronization and real-time operation of the processors. A number of peripheral components are also available for this simulator. The GTSYNC card is used to synchronize the simulation time-step to an external time reference (e.g., a global position system clock, which also synchronizes the devices under test), GTIO cards to facilitate physical connections to external hardware via analogue and digital I/O, the GTNET card to provide communication via high level Ethernet protocols (e.g., IEC 61850, DNP, C37.118, and so on), the global bus hub for real-time synchronization of three racks or more, and so on. This hardware is custom designed, and detailed descriptions are available in [36]. Recently, this simulator introduced the application of FPGAs in conjunction with its main processors to perform the simulation of very high-frequency (20–100 kHz) switching circuits [37].

Another commercial off-the-shelf-component-based scalable real-time (Type-B) simulator is developed that uses general-purpose multicore multithread CPUs, such as processors from Intel Xeon or the AMD family of CPUs [38]. Using a multi-CPU motherboard, the simulator can be extended up to many cores per target system, and each core can be used to model a subsystem [38]. Fig. 5 shows how various components of the hardware are connected to form the real-time simulator. In addition to the common PC components, reconfigurable FPGAs are used for conditioning I/O signals and limited modeling environments for high-frequency components using Xilinx toolbox Xilinx System Generator (XSG). The latest trend of this simulator is to customize application-oriented systems, such as integrating FPGAs, GPUs, or a combination of other hardware components for specific industry application [39]–[41].

2) SOFTWARE

Software required for real-time simulators can be divided into two main categories: 1) operating system (OS) software and 2) application software. In general, commercially available real-time simulators run on either Windows- or Linux-based OSs. However, depending on the hardware, specialized OSs may be necessary. For most of the simulators, the OS is supplied by the vendor. For custom-made real-time simulators, hardware-specific OS may be required and normally comes with the hardware.

Application software mainly provides a platform for modeling power system networks and their controls. In general, graphical user interface (GUI)-based modeling environments are provided to drag and drop components to build the entire system. In some cases, a command line language can also be used and scripts are executed to automate the simulation. Application software uses its own built-in modeling tools and solvers to simulate the systems. However,

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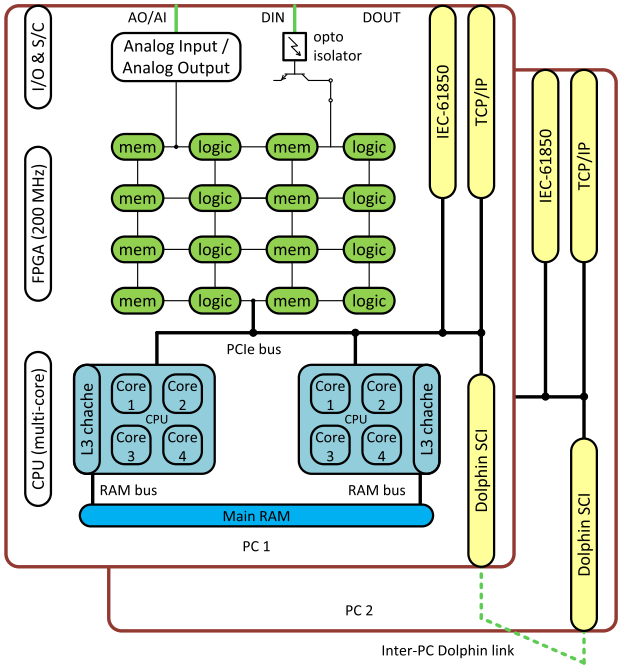

FIGURE 5. Hardware architecture of eMEGASIM real-time simulator.

the use of a custom model or custom code is possible if the provided model does not meet the user requirement.

Since the simulator described in [36] is built upon custom hardware, the GTWIF OS is based on VxWorks, but the PB5 processor card uses a proprietary bare metal OS for increased efficiency. Its application program software suite runs on a Windows-based host platform and is used to build the model, set up simulations, control, acquire data, and modify system parameters during a simulation. The other simulator [38] uses Linux-based platforms such as RedHawk, RedHat, or QNX as the OS for the targets, and modifies them to support the functionality and the performance required by complex real-time applications. One key aspect of the modified Linux is the complete core shielding, where all the cores except one are dedicated for real-time computation and are shielded from system interrupts. That particular one core performs the job of real-time operating tasks and schedules. For the host OS, it uses Windows, although Linux OS is also an option. This simulator provides a set of proprietary toolboxes to be used for modeling different types of systems.

3) COMMUNICATION AND INTERFACING

The Type-A simulator uses a common communication backplane that links all slot-mounted cards within a rack and facilitates the exchange of information. Direct card-to-card communication is also possible through the multiple fiber optic links located on the processor cards. The processor card fiber optic links are also used to connect I/O cards in parallel and/or in a daisy chain. In a multirack simulator, the backplanes function independently and in parallel, thereby reducing communication bottlenecks. Information that must be shared between racks is passed via interrack communication (IRC) channels on the GTWIF cards (point-to-point communication). For simulators with more than seven racks, an IRC switch is used to provide direct communication between as many as 60 racks (star-point communication). The communication between the simulator racks and the host computer is performed by the GTWIF cards using standard Ethernet.

Due to the fast advancement of digital technologies, including network and communication, Type-B simulators have gone through fast development phases, where various communication techniques and protocols have been used for sharing information between the host and the target nodes. To name a few that are currently used are shared memory for inter CPU communication inside the target, signal wire, InfiniBand, Gigabit Ethernet, Dolphin SCI and PCIe link for target-to-target communication and TCP/IP link for asynchronous communication with the host.

4) MODELING TOOLS/LIBRARIES

For Type-A simulators, GUI component model libraries are included as an integral part of the RSCAD suite and allow building of power system models along with the necessary control and protection. Another important feature of the suite is that it allows small time-step (1–4 μs) environment subnetworks, which can be freely constructed to represent high-frequency switching dynamics. The small-time-step-based subnetworks can be interfaced to one another through transmission line models (TLM) or to large-scale power systems models operating with the time-steps on the order of 50 μs through TLM or interface transformers. The interface technique is similar to the technique of splitting large models into multiple racks by exploiting the traveling wave delay for transmission lines with a travel time longer than one time-step. The requirements for larger or smaller time-step circuits can also be achieved using FPGA cards, where very high-frequency switching circuits can be modeled with time-steps in the order of hundreds of nanoseconds and can still be interfaced with either small time-step subnetworks or large time-step subsystems. A facility is also provided within RSCAD for the user to create new simulation components. The conversion tool that converts a PSS/E into a RSCAD model is another useful tool for utility application, especially for developing such models of larger power systems.

For Type-B variants, a MATLAB/Simulink environment is employed for the development of power and control system models. Most physical systems and their controllers can be modeled with the built-in MATLAB/Simulink toolboxes; however, the user-defined models written in MATLAB or other high-level languages, such as C/C++ or FORTRAN, can also be included through the MATLAB/Simulink S-function interface. Custom models based on VHDL coding can also be integrated with the Simulink-based models. Large and complex systems models can be divided into several subsystems and distributed over a number of parallel cores. Additional model enhancement tools, such as RT-EVENTS,

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RTDRIVE, and RT-XSG [38], are good examples of the MATLAB/Simulink environment expansion. In addition, LABView, PYTHON, and other application programming interfaces can also be incorporated for scripting and automating the simulation.

5) SOLUTION METHODOLOGY

A Type-A simulator uses Dommel's electro magnetic transients program (EMTP)-type algorithm [4], [8] to discretize all the components of the circuits, including passive elements such as breakers and faults. Active sources are modeled as equivalent sources with several types of impedances, including positive and zero sequences. The network solution performs real-time decomposition of the admittance matrix that allows continually varying conductance elements to be represented in the circuit.

On the other hand, a Type-B simulator also uses a nodal admittance-based solver called ARTEMiS-SSN [42]. In this simulator, models are built upon the Simulink and SimPowerSystems platforms, where default trapezoidal or backward Euler solver/integration algorithms available in MATLAB/Simulink for discrete solution could be used. These solvers, however, are not designed for strictly real-time simulation, because the solution time of each step varies considerably. The ARTEMiS-SSN solvers enforce strictly fixed time-step simulation for these models and are effective for networks under 100 three-phase buses [41]. ARTEMIS-SSN is a nodal admittance solver that uses a fixed-step higher order discretization/solution algorithm and uses the interpolation method, allowing very accurate detection of switching events. It also precomputes the nodal companion matrices, derived from their respective state-space equations, combined with online refactorization of the nodal admittance matrix and thereby provides a faster simulation compared with the SimPowerSystems solvers.

In addition to the EMTP-type solution, both Type-A and Type-B DRTS offer the hybrid solution technique, where part of the network in detail is solved using an EMTP-type simulation while considering its interaction with a much larger network, which is simulated using a transient stability solver. Type-B DRTS also allows the real-time phasor simulation of networks with more than 10 000 busses per core [43]. Irrespective of the simulation type (EMTP or phasor), it is required to address the synchronizing of discrete events that takes place during the time-step of simulation. Although this is a big challenge for DRTS, a number of methods have been published [44]–[47], and such simulators apply suitable methods in respective cases.

6) INPUTS AND OUTPUTS

In the Type-A simulator, various I/O cards are typically mounted on DIN rails within the simulator cubicle and connected directly to individual processor cards via optical fibers. The I/O cards provide digital and analog I/O ports for interfacing external hardware to the simulation. Alternatively, the I/O cards can be located remotely and connected using fiber lengths in the range of 75 m. Each processor card has multiple 2-GB/s optical ports to provide a very high bandwidth communication capability to support the I/O. Similarly, the Type-B simulator interfaces real hardware I/O signals of various types (analog, digital, pulsewidth modulation, timers, encoders, and so on) through the FPGA-based multichannel I/O modules. The scalable I/O terminals can detect external events at 10 ns resolution and can capture or generate multiple events within a simulation time-step to incorporate very precise timing into the model. Besides supporting the standard communication protocols such as Gigabit Ethernet, C37.118, IEC 61850, and DNP3, both simulators support many other third-party I/O boards.

C. OPEN-SOURCE OR NONCOMMERCIAL REAL-TIME SIMULATORS

Outside the proprietary world, there are many real-time simulators built in many laboratories that came out of research projects for serving an in-house purpose. One such low-cost real-time simulator known as virtual test bed (VTB-RT) was developed at the University of South Carolina. While a preliminary approach to real-time extension in VTB was proposed a few years ago [49], a new, more advanced process has been developed in collaboration with RWTH Aachen University in Germany [50]. This first real-time extension is based on exactly the same solver adopted for the desktop version, while the new version is based on a simulation method specifically developed for real-time simulations [51], [52].

From the hardware perspective, in the current generation of supported processor boards, one DSP is used as a processing node of each processor board. A companion FPGA is used for providing timing, synchronization, and coprocessing as

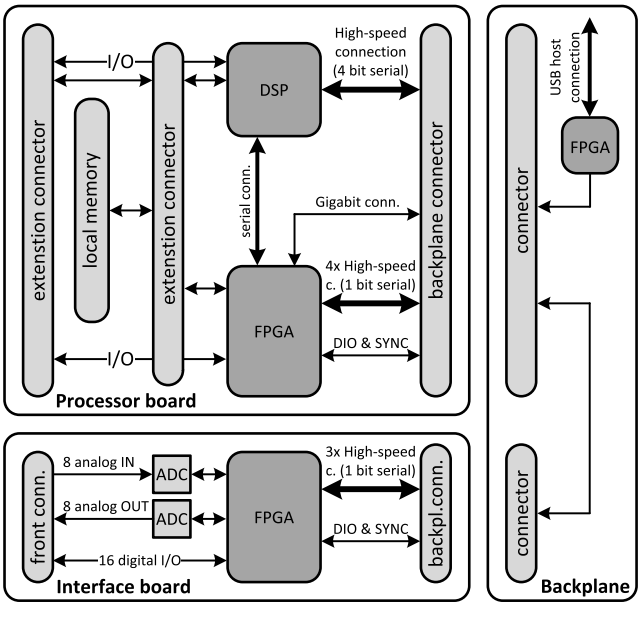

FIGURE 6. **DSP cluster-based architecture of VTB-RT simulator.**

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TABLE 1. Summary of salient features of RTDSs reported in the literature.

Real-Time Simulator	Hardware	OS and Application Software	Communication, Protocols, Interfacing and I/O	Modeling and Solution	Application	Other
RTDS from RTDS Technologies Inc. [13], [14], [36]	PowerPC RISC processors are implemented in cards (PB5), GTFPGA	Host OS: Windows Target OS: VxWorks Application software: RSCAD	Optical fiber, fast back plane, global bus hub, Gigabit Ethernet, DNP3, IEC61850, TCP/IP C37.118, analog and digital I/O, third party I/O through GTNET	EMTP -type library of component models, small time-step models for some components, Dommel's algorithm based Nodal solver	Real-time simulation of power systems, power electronics, control systems, testing of equipment through HIL simulation	Allows multi-rate simulation
eMEGAsim from OPAL-RT Technologies Inc. [23], [38]	Multi-core CPU, FPGA, commercial-of-the-shelf motherboard	Host OS: Windows Target OS: Linux based (QNX, RedHat) Application software: Matlab/Simulink, RT-Lab suite containing tools for EMTP type and Phasor analysis	Shared memory, Gigabit Ethernet, Dolphin networking, IEC61850, C37.118, DNP3, FPGA-based analog & digital I/O terminals, supports third party I/Os	Simulink and in-house tool boxes, code (C/C++, Matlab, Fortran) wrapped with S-function, discrete Simulink solvers, vendor specific solvers such as ARTEMIS-SSN	Real-time simulation of power electronics, power systems, control and automotive systems, multi-domain simulation, HIL testing and simulation	Multi-rate simulation, ePHASORsim transient stability extension available, EMT models can be implemented on FPGA cards [48], multi-domain as it supports all Simulink block-sets
HYPERSIM [27], [29]	CPUS are used with SGI's NUMAlink processors interconnect architecture, can parallelize up to 2500 cores, FPGAS can be interfaced	Host OS: Windows Target OS: Linux based Application software: Hypersim software suite	Gigabit Ethernet, IEC 61850, standard PCIe interface with DSP based A/D and D/As	GUI based component library is available through which system model is built, state-space solution method is used with multiple integration rules	Real-time simulation of power systems with power electronics, control systems, HIL testing	Implementable in eMEGAsim platform for smaller scale transmission systems, automatic task mapping to available processors
dSPACE [26]	CPU	Host OS: Windows Target OS: QNX ROS	Gigabit Ethernet, PCIe based communication with other hardware and I/O uses proprietary dSPACE protocol, IOCNET	Simulink, Stateflow, AUTOSAR, C coded models	Mainly used for real-time control and rapid prototyping for automotive engineering, aerospace, and industrial control	---
VTB [49]-[52]	DSP cluster or multi-core CPU/FPGA	Host OS: Windows Target OS: Linux	---	Modified resistive companion	Power system	Multi-physics possible
xPC Target [53]	CPU, FPGA	Host OS: Windows Target OS: Optimized Real-time Kernel	Analog and Digital I/O modules are supported through PMC, PCI, PCIe, cPCI, and PC104 protocols, serial, TCP/IP, UDP/IP, CAN, J1939, ARINC 429, and MIL-STD-1553	Simulink and Stateflow for model development, Simulink Coder, HDL coder, C	Rapid prototyping, real-time testing of applications and HIL simulation.	Multi-physics
rtX from ADI [54]	CPU	Host OS: Windows Target OS: QNX RTOS Application software: AdvantageDE	I/O interfacing through PCI, PXI, PCIe, PMC etc.	GUI based Advantage DE can be interfaced with Simulink, SystemBuild, C, Fortran, ADEPT, ALTIA	Power system simulation for avionics and maritime industries, aircraft simulation, shipboard simulation	---
Typhoon RTDs [55], [56]	FPGA	Host OS: Windows Target OS: FPGA	FPGA based Analog and Digital I/Os, IEEE 1284C, Ethernet RJ45	Typhoon schematic editor, SpiceShuttle, Matlab.	Testing of power electronics controller	---

well as communication to the attached interface board. In a minimal system, a small-scale backplane passively connects the processor board to the interface board, which utilizes an FPGA as a signal conditioning and coprocessing device for the analog and digital inputs and outputs. A pictorial view of such a system is shown in Fig. 6.

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With this new hardware implementation, the simulation of power electronics in the range of a few microseconds has been already demonstrated [50]. The key component of the new VTB feature is a C code generator. Currently, together with the DSP cluster introduced in this paper, it is possible to generate a real-time code for a PC cluster based on Linux OS.

VI. CONCLUSION

The main objective of this task force paper is to highlight the current state of the technologies used in the real-time simulation industry for power system applications. It has summarized the most salient features of real-time simulation platforms with applications related to power and energy systems. Although a number of real-time simulators are reported in Table 1, only a few of them are capable of simulating large systems. The remaining are either suitable for small systems or to serve as a real-time controller. Therefore, the characteristics of three main real-time simulators (i.e., RTDS, eMEGAsim, HYPERSIM, and VTB) are discussed in detail, whereas those of the rest of the simulators are listed in the summary table. Most of the real-time simulators are capable of interfacing external hardware to perform HIL tests and experiments.

Although designed for power systems applications, many of these real-time simulators are suitable for performing cosimulation using multirate/multiphysics simulation. With continuous customer support, these simulators can be used to accommodate any special needs of the consumers. In the next step, the task force will work on a similar paper that will summarize the applications of real-time simulators.

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