Real-Time Digital Simulation of Power Electronic Apparatus Interfaced With Digital Controllers

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***Abstract*—This paper presents a new approach for the real-time digital simulation of power electronic controllers in power systems. Digital controllers for power electronic systems present a problem when testing in real-time using a digital simulator due to the discrete nature of their outputs which are not necessarily in synchronism with the time step of the simulator. The proposed algorithm combines the variable step-size numerical integration method with linear interpolation for the synchronization of a real-time digital simulator and a digital controller. It is shown that lack of such synchronization leads to inaccurate simulation results, specifically with regard to the fundamental and harmonics of the voltage and current signals. Sampling theory is used to model the interaction between a digital simulator and a digital controller. A Pulse Width Modulated (PWM) Voltage Source Converter (VSC) based reactive power compensator system is used as an illustrative example for the simulation.**

***Index Terms*—Digital control, numerical integration, power electronics, real-time simulation.**

I. Introduction

RAPID developments in semiconductor technology and availability of low-cost and computationally powerful digital processors have been the impetus for a significant shift from conventional analog control systems to digital control systems. Digital control systems are increasingly used to control power electronic based apparatus in electric power systems at generation, transmission, distribution and utilization levels.

A digital control system, usually built around one or more digital processors, comprises of hardware and software whose basic functions include: i) data acquisition and processing, ii)communication, iii) system logic and control algorithms, iv) power circuit interface and v) auxiliary functions. Available processors for digital control systems include: i) General Purpose Processors, ii) Microcontrollers, iii) Application Specific Integrated Circuits (ASICs), iv) Field Programmable Gate Arrays (FPGAs), v) Digital Signal Processors (DSPs), vi) Reduced-Instruction-Set Computing (RISC) Processors and vii) Parallel Processors.

Prior to commissioning there is a need for rigorous performance evaluation and testing of a digital control system and its corresponding power electronic apparatus within the context of the host power system. There are three approaches to address the need.

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The first approach is based on interfacing the digital control system with a properly scaled physical simulator to represent the power electronic apparatus and the host power system. The main drawbacks of this approach are: i) requirement of excessive manpower and resources, ii) extensive time to prepare set-ups, iii) inflexibility of the simulator to accommodate various system scenarios and phenomena, and iv) inherent lack of scalability to accurately represent system parameters and nonlinearities in the simulator.

The second approach is based on off-line digital simulation. There exist powerful production grade software tools, e.g., EMTP, PSCAD/EMTDC, and NETOMAC, that can readily represent power electronic apparatus and power systems. Such tools also provide facilities to represent basic control logics and algorithms for digital controllers. However, comprehensive and uncompromised representation of all functions of a digital controller for off-line simulation studies is a formidable task and is prone to skepticism with respect to the accuracy of the results.

The third approach is based on interfacing a digital control system with a real-time (on-line) digital simulator. The simulator represents the host power system and the power electronic apparatus. With the existing development trends in semiconductor technology, real-time digital simulation is gaining momentum and becoming more attractive.

A technical issue when interfacing a digital controller with a real-time digital simulator is that the output signal of the controller for firing power electronic switches may not be in synchronism with the discrete time-step of the simulator. This causes inaccuracies or even erroneous results. This paper presents a new algorithm (Section II) which combines linear interpolation and a variable time-step method for accurately accounting switching events in real-time digital simulation of power electronic apparatus. The problem associated with the lack of synchronism is explained in Section III. Application of the proposed approach to a VSC based compensator is detailed in Section IV and its effectiveness is demonstrated in Section V. Conclusions are stated in Section VI. A subsequent paper will report hardware implementation of the proposed approach for real-time simulation of power electronic systems.

II. The Problem and Proposed Solution

Digital controllers for power electronic systems output discrete firing signals which may not necessarily be in synchronism with the time step chosen for the real-time digital simulator. The error in the solution of the system state stems from the delay introduced in the switching due to improper synchronization of the two discrete processes. Unlike the actual physical system the

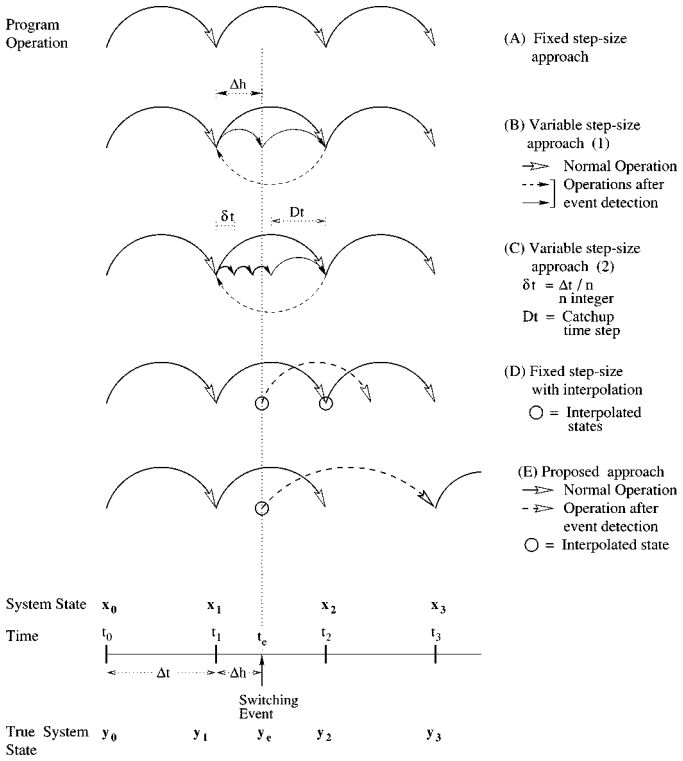

Fig. 1. Switching events in digital simulation.

digital simulator is unable to respond instantaneously to a firing signal that comes in between two calculation steps; since it can only respond at the end of a calculation step the actual switching may occur one time step too late in the worst case. Also, since the incoming firing signal does not always occur at the same instant on the time grid of the simulator, the switching is not always realized at the same moment and therefore the delay introduced is not constant. Larger the time-step of the simulator larger is the delay in switching.

Fig. 1 illustrates the problem. Let x_i, $(i = 0, 1, 2, \ldots)$ be the states of the system computed by the simulator at every time step Δt and y_i, $(i = 0, 1, 2, \ldots)$ be the true states of the system obtained by taking discrete events into account at their exact locations. The firing signal comes in at time t_e but is accounted for at time t_2 when the real-time simulator has already calculated the incorrect state x_2. The actual physical system would respond to the firing signal at time t_e with the state y_e and y_2 would be the true state of the system at time t_2.

In an off-line fixed time-step digital simulation program, such as the EMTP, [Fig. 1(a)] events that occur between two time steps are accounted in the next calculation step. The discrete event coming in at time t_e is acknowledged at time t_2 and is used to calculate state x_3 at time t_3. The traditional approach to alleviate the errors due to delay in switching is to carry out the entire simulation with a small Δt, so as to reduce the delay, but at the cost of a larger total simulation time.

In a variable time-step program [Fig. 1(b)], as the name suggests, the time-step of the simulation is changed whenever a discrete event comes in between two calculation steps. When the discrete event is detected at time t_2 the algorithm backtracks to the state x_1 at the previous time step, takes a smaller time step Δh and calculates state y_e, takes another time step $(\Delta t - \Delta h)$ and calculates state y_2, and then proceeds with a fixed time step Δt till the next discrete event is detected. The variable time-step process would involve a re-formulating of the admittance matrix during the course of program execution everytime the time-step changes. If the study system is large, this would mean a significant computational burden.

Another variation [Fig. 1(c)] of the variable time-step method is a method [6] where two time steps—one Δt another $\delta t\,(=\Delta t/n)$ an integer submultiple of Δt are maintained. When the discrete event is detected at time t_2 the algorithm backtracks to time t_1 and starts calculating states every δt so that instead of accurately pinpointing the instant t_e it is finely straddled between two calculation steps δt. Once the event has been accounted for a catch-up time step Dt is taken to time t_2. The advantage of this method is that the system admittance matrix can be pre-calculated and stored for the three time steps Δt, δt and Dt. As mentioned earlier, linear interpolation has been used effectively in off-line digital simulation programs to accurately model switching instants. Fig. 1(d) illustrates a method [1] where linear interpolation is used with a fixed step-size approach. Once the switching event is detected at time t_2 the system state is linearly interpolated at time t_e and the solution continues with the original time step Δt yielding a new solution one time-step later. An additional interpolation step between t_e and $(t_e + \Delta t)$ is taken to find the state at t_2. This second interpolation step is taken to put the solution back on the original time grid. So, there are two interpolation steps and two regular solution steps from the time the discrete event is detected at t_2 till the time the state x_3 at t_3 is calculated. This approach again has the advantage that the admittance matrix need not be re-formulated since the time step is fixed.

With regard to real-time computation the fixed step-size approach [Fig. 1(a)] with a small Δt is not feasible in the case of realistic size systems due to excessive computational speed requirement. The variable step-size approaches (1) and (2) in Fig. 1(a) and (b) also cannot be used for real-time computation for the reason that one cannot step back in real-time. The approach of Fig. 1(d) is conceptually attractive due to the fixed step-size but for real-time implementation it needs significant computer time to compute two interpolation steps and two regular solution steps.

In the proposed approach [Fig. 1(e)] a combination of variable step-size and linear interpolation are used. Once the state x_2 at time t_2 is computed, the real-time simulator acknowledges that the discrete event occurred at time t_e. Then it interpolates the system state at t_e based on states x_1 and x_2, formulates the admittance matrix based on the step-size of $(2\Delta t - \Delta h)$ and takes a regular solution step to time t_3. A correction of the state x_2 by using another interpolation step as in approach of Fig. 1(d) is not possible in real-time because that time has already passed and the simulator cannot call back the state it has already computed. The proposed approach is well-suited for real-time implementation in that in addition to the regular solution step it involves only one interpolation step and one re-formulation of the admittance matrix. Notice that the external apparent time step of the simulator is still fixed, there is only an internal adjustment of the time step whenever a discrete event is detected. The computational effort as compared to the fixed step-size approach

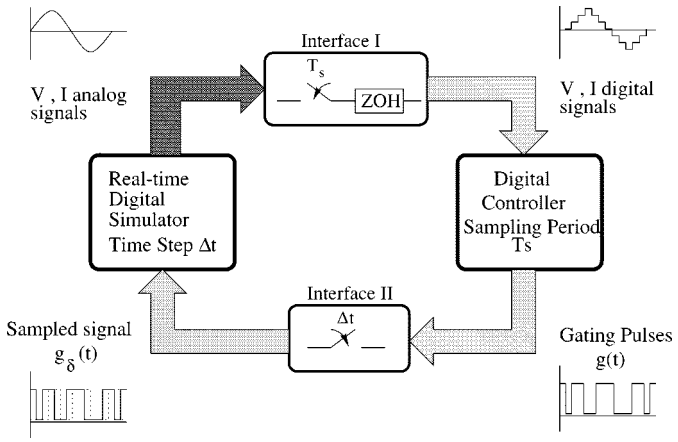

Fig. 2. A digital controller and a real-time digital simulator.

[Fig. 1(a)] would depend on the size of the system simulated. The objective is to get similar accuracy as obtained by using the fixed step-size approach with a small time step. The proposed approach takes the discrete events into account at their exact locations thereby reducing the simulation errors. The following section gives a mathematical interpretation based on sampling theory to get a better insight into the origin of simulation errors.

III. Interaction Between Real-Time Power System Simulator and a Digital Controller

Fig. 2 illustrates a Real-Time Digital Simulator (RTDS) interacting with a digital controller. The RTDS generates signals in digital form which after D/A conversion and level shifting appear at the output as the power signals such as v, i in analog form. These signals are sampled by the digital controller at a specific rate T_s which is referred to as the controller sampling period. Interface II represents this sampling action modeled by a sampler operating at a rate of T_s and a zero-order hold. The digital controller on the other hand outputs discrete signals such as PWM gating pulses to power electronic devices modeled in the simulator. The simulator can acquire these gating pulses only at finite intervals Δt due to the discrete nature of the numerical integration process that it is carrying out. Interface III represents this Δt latency on the gating signals and is modeled by another sampler with sampling rate Δt. The problem defined in Section III is related to Interface III.

Let $g(t)$ and $p(t)$ represent the gating signal in Fig. 2 and the sampling function as functions of time. In the time domain the sampled gating signal $g_p(t)$ is given by

$$g_p(t) = g(t) \cdot p(t) \tag{1}$$

where $p(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_{sg})$ is the periodic impulse train with T_{sg} as the sampling period and $\omega_{sg} = 2\pi/T_{sg}$ as the sampling frequency.

$$g_p(t) = \sum_{n=-\infty}^{\infty} g(nT_{sg}) \cdot \delta(t - nT_{sg}). \tag{2}$$

Since multiplication in time domain corresponds to convolution in the frequency domain

$$G_p(j\omega) = \frac{1}{2\pi} [G(j\omega) \star P(j\omega)] \tag{3}$$

where

$$G(j\omega) = A_0 + \sum_{n=1}^{\infty} (B_n \sin n\omega_m t + A_n \cos n\omega_m t) \tag{4}$$

is the Fourier series representation of a PWM generated gating signal and

$$P(j\omega) = \frac{2\pi}{T_{sg}} \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_{sg}). \tag{5}$$

Since convolution with an impulse simply shifts a signal, it follows that

$$G_p(j\omega) = \frac{1}{T_{sg}} \sum_{k=-\infty}^{\infty} G(j\omega - jk\omega_{sg}). \tag{6}$$

Thus, $G_p(j\omega)$ is a periodic function of ω_m consisting of a superposition of shifted replicas of $G(j\omega)$ scaled by $1/T_{sg}$. Since a PWM gating signal such as $G(j\omega)$ is not frequency band-limited, sampling such a signal at a fixed rate will result in an aliased signal according to Shannon's sampling theorem. The resulting signal $G_p(j\omega)$ thus is always an undersampled version of $G(j\omega)$. The effect of aliasing in the gating signal can be seen in the output voltage harmonics of the power electronic apparatus, a VSC for instance, specifically as an increase in the fundamental component. There are two major consequences of the aliased gating signal: a) the fundamental component of phase current of VSC increases and b) there is a crowding of the current harmonic spectrum with noncharacteristic harmonics. These effects become more pronounced as the time step of the simulator increases.

IV. Case Study: Compensator System

This section describes the time-domain model for a VSC based reactive power compensator (STATCOM) system and its digital controller. Particular emphasis is on the implementation of a sinusoidal PWM scheme in the digital simulation program. Lastly, the organization of the real-time program is explained.

A. Modeling of the STATCOM System

Fig. 3 illustrates the STATCOM power system. The utility is assumed to be a three-phase balanced voltage source with R_s and L_s comprising the equivalent circuit for the source side. L_t represents the filter and transformer leakage inductance. R_t includes the VSC and transformer conduction losses. The resistance R_p in shunt with the dc capacitor represents the switching losses in the inverter. The switches in the VSC are modeled as ideal bi-directional switches with gate turn-on and turn-off controls. The VSC model is based on discrete switching functions [7]. Taking i_a, i_b and v_{dc} as the states, the system model can be represented by three differential equations:

$$\frac{di_a}{dt} = -(R_s/L_s)i_a + (1/L_s)(v_a - e_a) \tag{7}$$

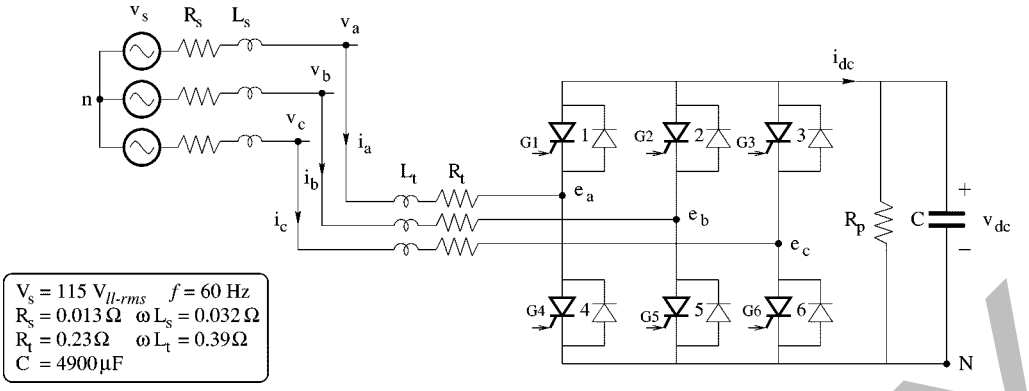

Fig. 3. STATCOM power system.

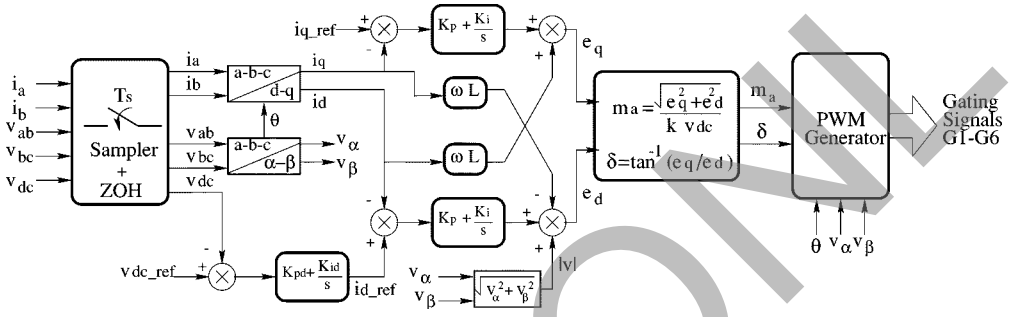

Fig. 4. Block diagram of STATCOM controller.

$$\frac{di_b}{dt} = -(R_s/L_s)i_b + (1/L_s)(v_b - e_b) \tag{8}$$

$$\frac{dv_{dc}}{dt} = -(1/C)(-i_{dc} + v_{dc/R_p}). \tag{9}$$

B. Current Control of VSC

For control purposes all voltages and currents are transformed to a synchronously rotating reference frame where the d-axis is coincident with the instantaneous ac system bus voltage and the q-axis is in quadrature angle with it. The system model in the dq frame is given by:

$$\frac{di_d}{dt} = (-R_s/L_s)i_d + \omega i_q + (1/L_s)(v_d - e_d) \tag{10}$$

$$\frac{di_q}{dt} = -\omega i_d - (R_s/L_s)i_q + (1/L_s)(v_q - e_q) \tag{11}$$

$$\frac{dv_{dc}}{dt} = \frac{3}{2}\frac{(e_d i_d + e_q i_q)}{C v_{dc}} - \frac{v_{dc}}{R_p C} \tag{12}$$

where v_d and v_q are the d- and q-axis components of the ac bus voltage. The quantities e_d and e_q are the d and q -axis components of the VSI terminal voltage.

$$e_d = k m_a v_{dc} \cos\delta \tag{13}$$

$$e_q = k m_a v_{dc} \sin\delta \tag{14}$$

where

$m_a = \sqrt{(e_d^2 + e_q^2)}/k v_{dc}$ modulation index;

$\delta = \arctan(e_q/e_d)$ phase angle;

k constant whose amplitude depends on the modulation technique used.

The inverter voltage vector is controlled as follows:

$$e_d = L_s(-x_1 + \omega i_q) + |v| \tag{15}$$

$$e_q = -L_s(x_2 + \omega i_d) \tag{16}$$

substitution of these equations into (10) and (11) yields

$$\frac{di_d}{dt} = (-R_s/L_s)i_d + x_1 \tag{17}$$

$$\frac{di_q}{dt} = (-R_s/L_s)i_q + x_2. \tag{18}$$

Equations (17) and (18) provide a decoupled control of i_d and i_q. x_1 and x_2 represent the outputs of the PI compensators regulating i_d and i_q. The dc link voltage is regulated through an additional external feedback loop that provides the real current reference $i_{d_{ref}}$. Fig. 4 shows the block diagram of the STATCOM controller [4].

C. Pulse Width Modulation

In an off-line digital simulation program, e.g., EMTP or EMTDC/PSCAD, a sinusoidal pulse width modulation scheme is implemented by comparing a carrier signal (usually triangular) with a sinusoidal control signal. Since the PWM generator is part of the entire system simulation, the carrier wave is also generated with the same universal time step Δt at which the system simulation is carried out. This method has two consequences for the speed and accuracy of the simulation:

1) It restricts the choice of Δt for the system simulation due to the fact that a smaller Δt has to be chosen so as to have a higher carrier resolution which results in a longer simulation time.

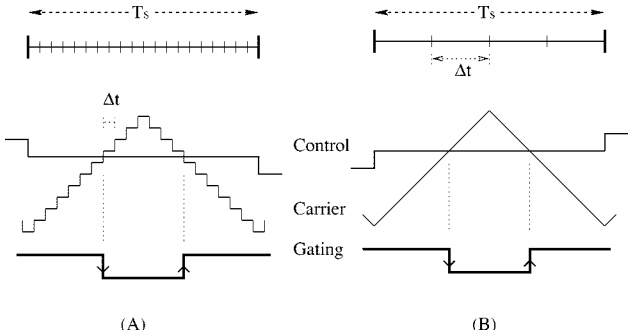

Fig. 5. Comparison of PWM implementation in digital simulation.

2) If a larger Δt is chosen the resolution of the carrier signal in the PWM generator is affected which in-turn affects the PWM output and the accuracy of the simulation.

For instance, a system simulation that normally requires only a time step of about 50 μs for capturing the required system transients would need a time step of about 5 μs or less if it includes a PWM generator with a carrier of frequency of 1 kHz or higher. So if a time step of 5 μs is chosen the entire simulation slows down considerably whereas with a time step of 50 μs the resolution of the PWM generator suffers which could yield inaccurate simulation results. The "Sampling Technique" approach [5], used in this paper, to generate the PWM gating pattern overcomes this dilemma and also takes the off-line digital simulation one step closer to the way in which digital controllers are implemented in reality. The sinusoidal reference wave is sampled only at periodic time instants T_s which is also the sampling period of the digital controller. The triangular carrier is defined using straight line segments of pre-defined slope in that sampling interval. The switching instants are computed on-line as the respective points where the triangular slope reaches the sampled reference value. Fig. 5 compares the conventional approach (A) and the proposed approach (B); in both approaches the switching frequency f_{sw} is taken equal to the controller sampling frequency $f_s = 1/T_s$. In the former PWM scheme the resolution of carrier is dependent on Δt; the only way to increase the carrier resolution is to reduce the time step Δt. In the latter PWM scheme the carrier resolution is essentially independent of Δt thereby making an infinite resolution possible; the switching frequency is however dependent on the controller sampling period T_s which is in keeping with the practical implementation of a digital controller.

D. Real-Time Program Structure

Fig. 6 shows the real-time program structure. In every time step Δt three blocks are executed: 1) Discrete Event Scheduler (DES); 2) VSC model; 3) Network Solution.

The DES performs three functions: (a) It precisely identifies the time instants when the gating signals occur; (b) determines the instant where interpolation has to be applied; (c) calculates the time step for the next network solution and handles the synchronization of the network solution with the original time grid Δt. In practical implementation of the simulator the DES has to implemented using digital hardware.

The switching function model of the VSC obviates the approach [2] of pre-calculating and storing the inverse conductance matrix for all possible conduction states of the switches, 2^6 in this case, and thereby is a more suitable model for the real-time simulator program.

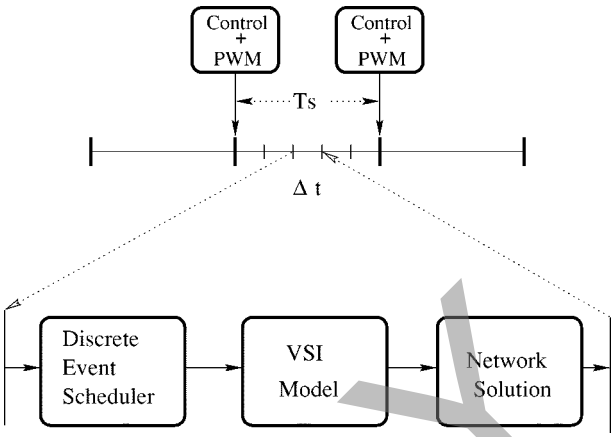

Fig. 6. Real-time program structure.

The Network Solution block uses the trapezoidal numerical integration method to convert continuous-time differential equations into discrete-time difference equations. The discrete time representation of network elements such as R, L, and C consists of conductances in parallel with current sources, and all voltage sources are represented by their Norton equivalents. The transient solution is then based on solving the nodal equations [3] for the network.

V. Digital Simulation Results

To evaluate the effectiveness of the proposed approach, open-loop and closed-loop control studies were performed on the STATCOM system. The relative performance of the proposed approach, using linear interpolation and variable step-size solution, and the fixed time-step approach are compared. In keeping with real-time requirements a time step of 50 μs is selected. As shown later $\Delta t = 50$ μs is not adequate to model switchings accurately using a fixed time-step approach. The results obtained using the proposed approach with $\Delta t = 50$ μs are comparable in accuracy to those obtained using the fixed time-step approach with a small time step $\Delta t = 5$ μs ($\sim 0.1^\circ$ on a 60 Hz cycle).

A sinusoidal PWM scheme is used in which only one half of the carrier wave is implemented in one sampling period T_s of the digital controller i.e., $T_s = (1/2)T_c$ or, $f_s = 2f_c$ where f_s is the sampling frequency and f_c is the carrier frequency (1 kHz). Normally $f_s = f_c$ in the practical implementation of the controller but in the simulation program $f_s = 2f_c$ is used to limit the number of discrete events to a maximum of two in one simulator time step.

A. Open Loop Case

Fig. 7 shows the first 30 harmonics of phase-a current under steady-state operation with $m_a = 0.8$ and $\delta = 0.0^\circ$. Fig. 7(a) compares the simulation results using the fixed time-step approach with $\Delta t = 5$ μs and $\Delta t = 50$ μs. Fig. 7(b) compares the simulation results using the fixed time-step approach with $\Delta t = 5$ μs and the proposed approach using $\Delta t = 50$ μs. Due

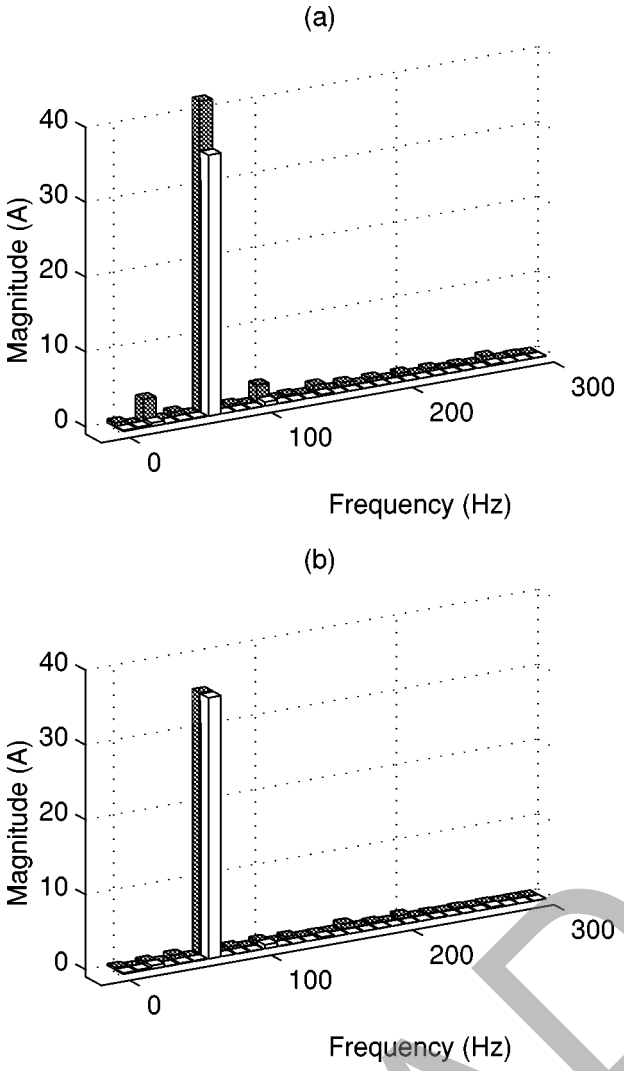

Fig. 7. Frequency spectrum of phase-a current under open-loop control. (a) Fixed time step approach using $\Delta t = 5$ μs (white) and using $\Delta t = 50$ μs (shaded). (b) Fixed time step approach using $\Delta t = 5$ μs (white) and proposed approach using $\Delta t = 50$ μs (shaded).

to aliasing effects on the gating signals the fundamental component of phase-a voltage was found to increase by 2.4% when Δt was changed from 5 μs to 50 μs using the fixed time-step approach. This increase in the VSC output voltage is reflected as an increase in the fundamental component of its phase current from 34.9 A to 41.5 A, an increase of 19%.This error tends to increase even more as the time-step is increased, for instance for $\Delta t = 100$ μs the error becomes 39%. The amplitudes of the switching harmonics were found to change little. Although there was a marked crowding of the frequency spectrum with noncharacteristic harmonics, their amplitudes remained small. This explains the surprising result that the THD($=20.95\%$) of phase-a current obtained for $\Delta t = 50$ μs was close to the THD($=20.9\%$) obtained for $\Delta t = 5$ μs. With the proposed approach using $\Delta t = 50$ μs the fundamental of phase-a current is 34.93 A which is very close to the result for the fixed time-step approach using $\Delta t = 5$ μs, a change of only 0.11%. The THD($=22.95\%$) for the proposed approach is slightly higher. This can be attributed to the fact that in the proposed approach the state x_2 (Fig. 1) is not corrected after the interpolation step

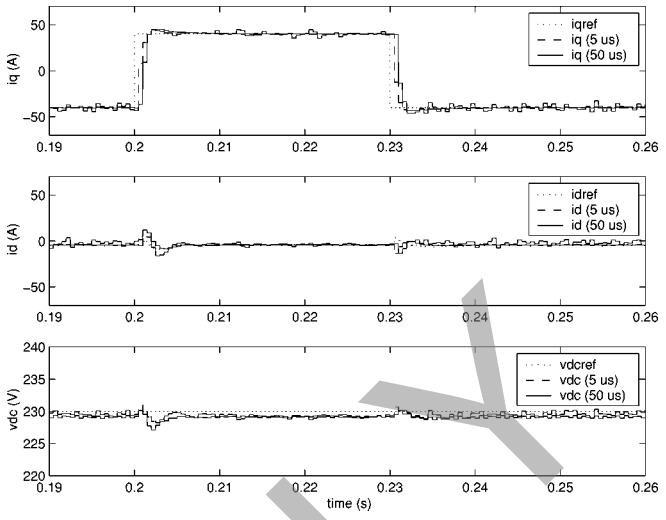

Fig. 8. Traces of STATCOM closed loop response.

since time t_2 is taken to have passed in real-time. Although the aliasing effects are also present under closed-loop control they are revealed much better under open-loop control. The reason is that under closed-loop control the current controller tends to regulate the output current and thus masks those effects. The higher accuracy derived with the proposed approach can be attributed to the precise detection of the gating signals, interpolation and the variable step-size solution.

B. Closed Loop Case

Fig. 8 shows the STATCOM closed loop response. A step response in i_q is simulated. The traces show the responses obtained using the fixed time-step algorithm with $\Delta t = 5$ μs and those obtained using the proposed algorithm with $\Delta t = 50$ μs. Clearly the responses are very similar. There is a spurious noise in the $\Delta t = 50$ μs trace and its amplitude is found to decrease as the time step Δt or the controller sampling period T_s is decreased. In the practical application of a digital controller such noise can be filtered out or in the case of an off-line simulation interpolation can also be used for the control algorithm to get nearly smooth traces. However, no attempt was made to use linear interpolation in the control algorithm since the primary objective of the study was to emulate conditions that would occur with a practical digital controller and a real-time simulator. Both fixed time-step algorithm and the proposed algorithm were tested under the same control conditions.

C. Execution Time

The proposed algorithm and the fixed step-size algorithm were coded in ANSI C and both programs were run on a 250 MHz MIPS R10000 processor running IRIX 6.4. Table I compares the cpu times for the two programs for a 1s run. Evidently the execution time for the proposed algorithm is only slightly higher than that for the fixed time step algorithm with $\Delta t = 50$ μs. To obtain similar accuracy, as with the proposed algorithm using $\Delta t = 50$ μs, the fixed step-size algorithm using $\Delta t = 5$ μs took 10.29 s for the 1 s run, a ten-fold increase in execution time. These results show that the use of linear interpolation and step-size variation as in the proposed

TABLE I
CPU TIMES FOR A 1 s SIMULATION RUN

Δt	Fixed Δt algorithm	Proposed algorithm
$50\mu s$	$1.07s$	$1.11s$
$5\mu s$	$10.29s$	-

algorithm has a negligible effect on the execution time whereas a reduction in the simulator time step using the fixed time-step algorithm to get similar accuracy results in a significant increase in execution time. With the proposed approach a single iteration took approximately 54 μs to execute. The timings obtained indicate that the proposed algorithm has the potential for use in real-time simulation on a DSP platform.

VI. CONCLUSION

Real-time simulation of switching power circuits assumes paramount importance for the testing of digital power electronic controllers. It is therefore imperative to develop techniques for simulation that give accurate results while meeting real-time implementation constraints.

This paper proposes a new method for real-time simulation of switching power circuits to be interfaced with digital controllers. This approach utilizes a variable time step numerical integration algorithm and linear interpolation to accurately account switching events and synchronize a real-time digital simulator with a digital controller. The proposed approach has been validated by open-loop and closed-loop control studies performed on the STATCOM system. The studies indicate that the method can give fairly accurate results without recourse to excessively small time steps using a fixed time-step algorithm. The proposed approach can be readily programmed into an off-the-shelf DSP system to serve as a stand-alone real-time simulator.

This paper also studies the interaction of a real-time digital simulator and a digital controller. It is shown that a fixed time-step numerical algorithm can lead to simulation errors due to its inability to account for discrete events such as switching signals that occur in between time steps.

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