University of Alberta

Low Voltage Multi-level Converters using Split-wound Coupled Inductors

by

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Abstract

In low-voltage applications, an alternative approach to multi-level capacitor-based converters can be obtained by interleaving the switching of two converters across split-wound coupled inductors. When compared to traditional capacitor-based multi-level converters, using split-wound coupled inductors can double the effective switching frequency while eliminating the problem of voltage balancing inherent to split-capacitor connections. Furthermore, the number of voltage levels, relative to the number of devices, can be maximized by using an asymmetrical half-bridge topology with the split-wound coupled inductor. This thesis focuses on the topological attributes of asymmetrical half-bridge converters that use split-wound coupled inductors as a basis for low-cost, low voltage, multi-level converters.

In three-phase dc/ac applications, the use of coupled inductors and asymmetric bridges is examined for a three-level converter. To reduce converter weight and costs, the three-phase coupled inductors can be integrated into a single three-limb coupled inductor by eliminating the common mode winding voltages present in traditional interleaved pulse-width modulation schemes. Reduced conversion quality and increased device switching frequency are identified as the challenges in the elimination of these windings voltages. These challenges are experimentally examined with a modification to the modulation of the three-level converter. A three-phase, five-level coupled inductor dc/ac converter is then presented, and space vector based analysis is used to overcome the challenges inherent to three-limb coupled inductor operation. Thus, a compact five-level dc/ac converter is enabled as a low-cost solution to loss sensitive applications, such as low-inductance electric drive systems.

Automatic voltage balancing is also identified as a topological attribute of asymmetric half-bridges employing split-wound coupled inductors. With this attribute, a

modular balancing converter is presented for the automatic balancing of serially connected voltage sources, e.g. lithium ion batteries in electric vehicles. Two modes of voltage balancing are identified, and the circuit parameters that influence the balancing currents for each mode are described. The circuit parameters are then used to size commercial transformers, and the practical considerations of the power electronics are discussed for the experimental prototype. Therefore, a balancing converter that uses modular components is enabled for low-cost, non-dissipative, voltage balancing which does not require voltage feedback for operation.

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Nomenclature

A_C - cross-sectional area of a iron core (m^2)
B_{AC} - ac flux density (T)
E - A fraction of the input voltage, V_{DC}
E_{BASE} - Base voltage (V)
E_N - Battery voltage with lower than average charge (V)
E_P - Battery voltage with higher than average charge (V)
f_C - switching frequency (Hz)
f_O - fundamental output frequency (Hz)
i_A - ac output current of phase A (A)
$i_{A,1}$ - module current of phase A, module 1 (A)
i_{CM} - common mode circulating current (A)
$i_{CW,A}$ - circulating winding current of phase A (A)
$i_{DF,A}$ - differential circulating current of phase A (A)
i_M - magnetizing current (A)
i_p - module current of 'p' device (A)
i_α - inter-bridge balancing current (A)
i_Δ - intra-bridge balancing current (A)
L_{AC} - ac filter inductance (H)
L_E - leakage inductance of a winding (H_
l_M - mean magnetic length of path M (m)
Lpu - per-unit leakage inductance of a winding
L_T - total inductance (H)
L_W - winding self-inductance (H)
M - Mutual inductance (H)
MBB_N - the N^{th} modular balancing bridge
R_{AC} - ac load resistance (Ω)
R_C - reluctance of the iron core (H^{-1})
R_{le} - reluctance of the air (H^{-1})
r_{OFF} - total resistance in the diode-on path (Ω)
r_{ON} - total resistance in the switch-on path (Ω)
T_S - switching period (s)
$V_{A,B}$ - Line voltage of phase A relative to phase B (V)
$V_{A,N}$ - Output voltage for phase A (V)
$V_{A,W}$ - Winding voltage for phase A (V)
V_{CM} - Common mode winding voltage (V)
V_D - Diode voltage drop (V)
v_D - per-unit diode voltage drop

V_{DC} - dc input voltage (V)
α - per-unit inter-bridge voltage unbalance
Δ - per-unit intra-bridge voltage unbalance
θ - electrical angle in degrees or radians
φ - flux (Wb)

Chapter 1 - Split-wound Coupled Inductors in Multi-level Converter Systems

Split-wound coupled inductors are an alternative approach to generating extra voltage states over stacked capacitors in multi-level converter systems. Combined with an asymmetric half-bridge and interleaved switching, coupled inductor based converters are particularly well suited to low voltage applications, such as three-phase drives for low-inductance electric machines, due to their high effective switching frequency and the high number of voltage levels per device. Due to current sharing within the coupled inductor, these converters are also applicable in voltage balancing for batteries. Based on the use of the asymmetric half-bridge and split-wound coupled inductors, the thesis objective and outline are presented, along with a summary of the contributions from this thesis.

1.0 Introduction

As the earth's population continues to grow and our access to non-renewable resources decreases, the need for efficient energy conversion is of paramount importance. Therefore, due to their role in energy conversion, power electronics has seen an explosion in applications since the early 1970's [1]. As an example, consider the simplified diagram of Fig. 1-1, which illustrates a typical drive-train configuration for electric vehicles [2]. In this system, power electronics play a significant role in the generator systems (in the form of AC/DC converters), the batteries (in the form on DC/DC converters) and the actual drive of the high-speed electric machine (in the form of a DC/AC converter).

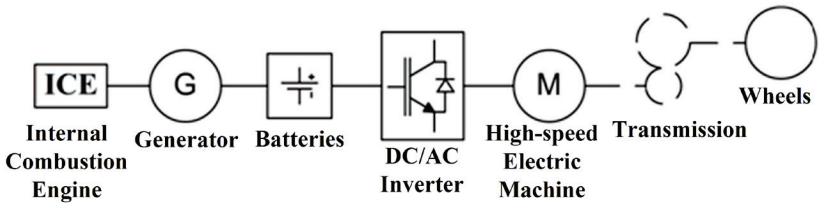


Fig. 1-1. High-level overview of a series hybrid drive train [2]

However, as power electronics have matured over the years, the focus on topological configurations has evolved into specialized converters, in an attempt to optimize the power conversion efficiency in specific applications. An example of this focus is the AC/DC converters used in on-board battery charging systems of electric vehicles. While standard AC/DC topologies can charge the battery systems, specialized converter topologies are necessary to maximize efficiency, meet reliability standards and

minimize converter weight [3]. This is just one example where the application drives a trend in the topological development of a power electronic converter.

Furthermore, while converters are becoming more specialized, another growing trend is the modularization of the power electronic units, within converters, to reduce costs [4, 5]. Additionally, modular converters can also accommodate redundant units - potentially improving the overall reliability. As an example, Fig. 1-2 illustrates the topology of a multi-modular converter, with the 'cell' (or base unit) being the commercially available half-bridge module [5].

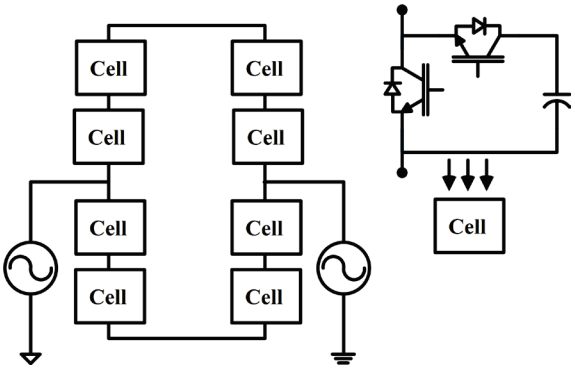


Fig. 1-2. A multi-modular converter

By employing split-wound coupled inductors over stacked capacitors, this thesis focuses on the development of low-voltage multi-level converter topologies based around the use of an asymmetric half-bridge and a split-wound coupled inductor. Two motivating examples are given for development of these multi-level converters: chemical based battery systems and high-speed flywheel battery systems.

1.1 Motivation

In chemical based batteries, such as lithium ion batteries, stacked multi-level dc/dc converters are required to balance the internal cell voltages. Likewise, in high-speed flywheel battery systems, a power electronic converter drives the electrical machine connected to the flywheel. As such, the efficiency and compactness of this battery system can be improved by using multi-level dc/ac converters. This section details the converter requirements for both applications as motivating examples to develop coupled inductor based converters.

1.1.1 Lithium ion Battery Strings

It is commonly acknowledged that one of the major limiting factors in electric vehicles is the battery system [6]. In automotive applications, high energy density, high output power, long life, operation under a wide range of temperatures, low internal

resistance, fast charging, stability, and low cost are required from the battery [6]. Currently, lithium ion polymer batteries are an attractive option to meet these requirements, but they are much less tolerant of 'abuse' than other types of batteries [6, 7].

Overcharging and overdischarging reduces the battery cell life span, and even overcharging by a few percent can lead to catastrophic failures [6]. In order to maintain safe operation for automotive applications, battery protection circuits must be designed for a given battery pack configuration. Furthermore, due to slight differences in battery cell manufacturing, each cell can have slightly difference internal parameters, affecting the distribution of charge in a series string of batteries [6]. As charging/discharging cycles tend to create further differences among the characteristics of each cell, a series connected string of these cells tends to become unbalanced over time [6]. As the total stored energy is dependant on the lowest cell voltage [6], it is imperative to balance these cells to maximize energy storage.

In Fig.1-3, a typical automotive-grade assembly of lithium polymer battery packs is depicted. As modern electric vehicle systems can run with 400V main dc levels, it is clear that the battery cell equalization technique must be applied across hundreds of cells. Therefore, this application requires low cost and reliable power electronics that are capable of multi-level converter operation across hundreds of low-voltage cells.

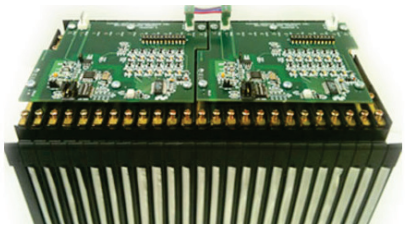
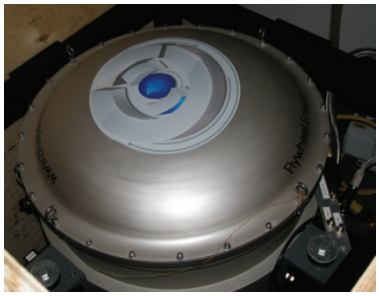


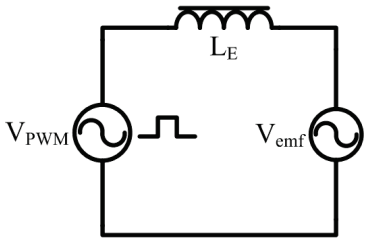
Fig. 1-3. A 24 cell lithium-ion battery pack [8]

1.1.2 High Speed Electric Machines in Flywheel Battery Systems

High speed flywheel battery systems are another emerging energy storage system that requires high performance power electronics. In these applications, mechanical energy is stored in the high speed rotation of a low inertia flywheel system, allowing much higher peak power delivery compared to chemical batteries [9]. These high speed flywheels, e.g. Fig. 1.4 a), are driven by high-speed electric machines, and due to requiring high power dynamic performance, these machines typically feature a low series inductance, i.e. small L_E in Fig. 1.4 b) [9, 10]. In transportation applications, the operational dc-voltage on the converter is kept within the low voltage region, e.g. 600-



a)



b)

Fig. 1-4. Flywheel battery system: a) example photograph and b) simplified electrical model of a permanent magnet synchronous machine. 'Vemf' is the back electromotive force of the electric machine, and 'V_{PWM}' is the pulse-width modulated converter voltage.

900V, to keep design costs low [11]. Therefore, the converters used are typically two-level, three-phase converters with inductive filters to limit the converter's impact on the high speed electric machine [9, 10].

As high-speed electric machines are at the heart of high-speed flywheel battery systems, the performance of these machines directly impact the efficiency of the battery system. More specifically, the harmonic distortion produced by standard power electronic converters can induce losses in the rotors of these high speed electric machines and potentially increase the temperature of the rotor's magnets. These losses are often difficult to remove due to the operational nature of the flywheel battery system, and can potentially cause permanent damage in the magnets of these machines [9].

Fig. 1-4 a) illustrates a 36,000 rpm flywheel battery systems intended for transit applications [11], and Fig. 1-4 b), the equivalent per-phase electrical diagram of a permanent magnet synchronous machine. Consider that for high speed electric machines, the series inductance, L_E in Fig. 1-4 b), can be low. Effectively then, this inductance provides inadequate filtering for the switched voltage harmonics produced by the power electronic converter, potentially resulting in damaged rotor components in the electric machine [9]. Thus, a series inductive filter is used to significantly reduce these induced rotor losses, but at the expense of power density of the system. By reducing the filtering requirement, i.e. by altering the power electronic topology to provide substantially better conversion quality, the converter could be directly connected to the flywheel battery system - maximizing the power density of this application.

In power electronic dc/ac converters, a topological method to increase the conversion quality is to increase the number of 'levels' used to synthesize the output ac voltage. In order to understand these concepts, a discussion on voltage sourced converter topologies is necessary, along with the basic concepts of power conversion.

1.2 General Power Electronic Converters

In general, for power electronic converters, there are two main configurations: voltage sourced and current sourced. In voltage sourced converters (or VSC), the main energy storage element is the capacitor, and the voltage conversion occurs by modulating the input dc voltage across a load. Conversely, for current sourced converters (or CSC), the main storage element is the inductor, and the conversion process occurs by pulse-width modulating the average current of this inductor into a load. In both cases, varying the amount of time of the voltage or current supplied load, is termed 'pulse-width modulation' (PWM). This section provides an overview the concept of multi-level pulse-width modulation in VSCs.

1.2.1 Multi-level Pulse-width Modulation

The voltage sourced converter topology, shown in Fig 1.5, can be sinusoidally modulated and sampled with a high frequency carrier, as in Fig. 1-6 a), which produces the voltage harmonic spectrum of Fig. 1-6 c), across the per-phase load. Consider though, that if the access to the center point of the two dc sources were available, an extra voltage stage for the pulse-width modulation would exist, as per Fig. 1-6 b). With the same sinusoidal pulse-width modulation across the per-phase load of Fig. 1-6 b), the voltage harmonic spectrum of Fig. 1-6 d) is produced.

Comparing Figs. 1-6 c) and d), it is clear that the magnitudes of the voltage harmonics have decreased - i.e. the converter produces a closer approximation to the ideal sinsoidal output. If the inductance of the load filters these harmonics, it can be visually appreciated that by increasing the number of 'dc levels' available in the conversion, the filter size would then decrease given a certain filtering requirement.

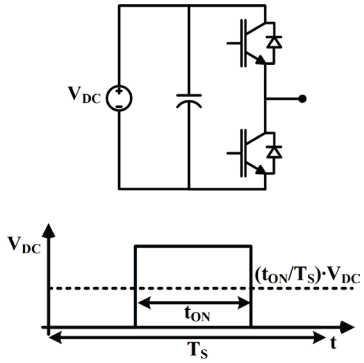


Fig. 1-5. Single-phase voltage converter topology illustrating the pulse-width modulated output of the input dc voltage, V_{DC}

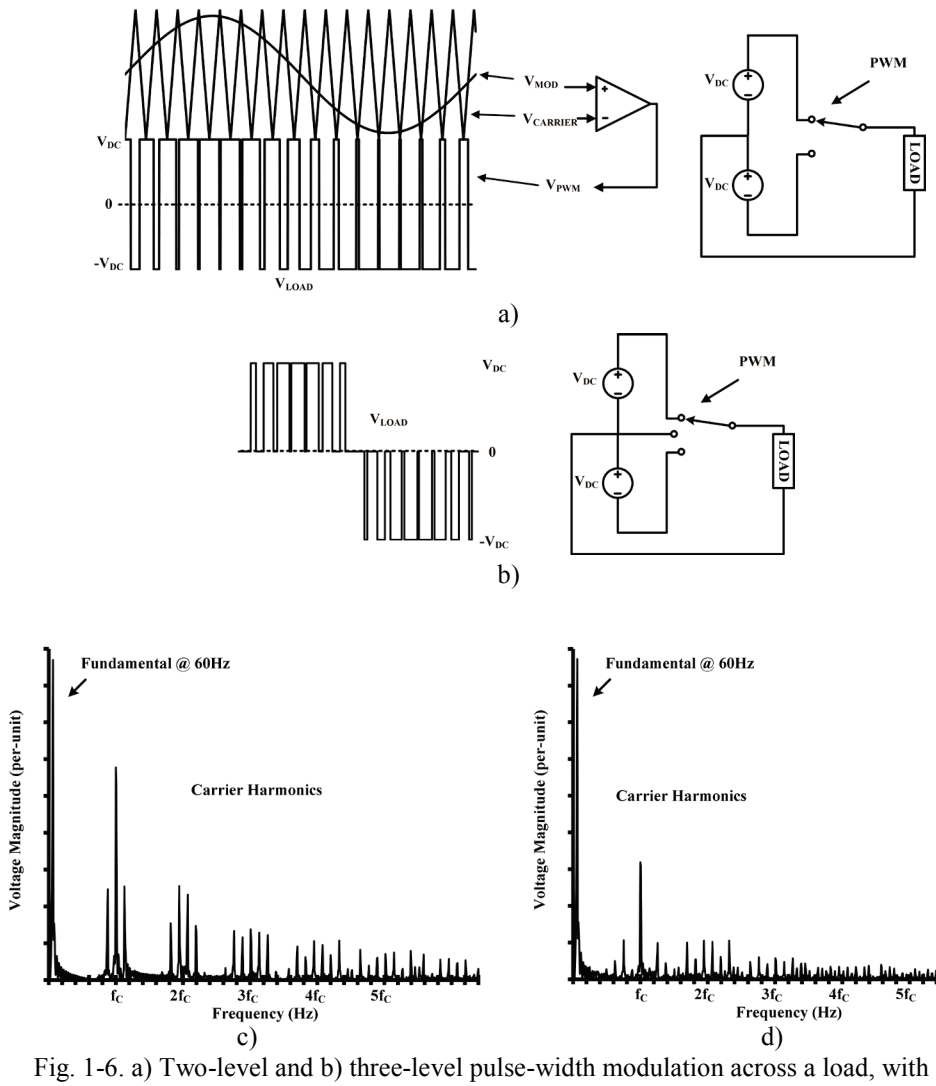


Fig. 1-6. a) Two-level and b) three-level pulse-width modulation across a load, with c) the corresponding harmonic spectrum to the two-level and d) the three-level pulse-width modulation

1.2.2 Multi-level PWM Converters

In order to provide access to an increasing number of dc voltage levels, the power electronic converter topology must increase in complexity. As an example, compared to the two-level topology of Fig. 1.5, Fig. 1-7 a) depicts a standard three-level VSC termed the neutral point clamped (NPC) topology. Note that for a three-level pulse-width modulated converter, two dc voltage sources are necessary. While multi-level pwm conversion has obvious advantages for dc/ac or ac/dc conversion, multi-level pwm dc/dc converters also exist, as depicted in the general case in Fig. 1-7 b). In these converters, the dc voltages are stacked to buck or boost the input dc voltage, with minimal inductive

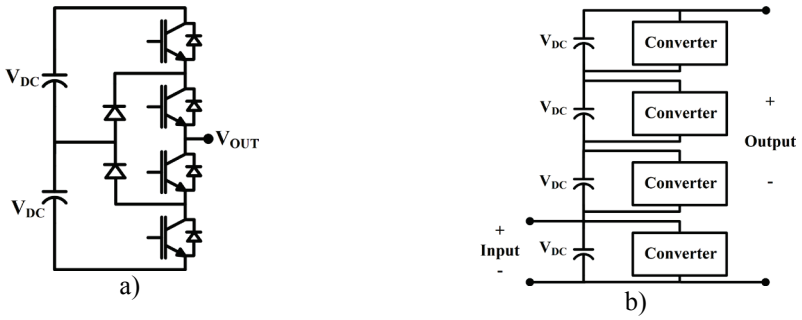


Fig. 1-7. a) Three-level voltage sourced converter (neutral point clamped), and b) general multi-level converter [12]

components required. In either case, note that the general multi-level voltage sourced converter is derived from a series of stacked capacitors.

1.3 Split-wound Coupled Inductors for Multi-level Converters

With stacked capacitors, as per Fig. 1-8 a), each capacitor provides access to a given voltage level required in the converter operation. However, an equivalent center tap can be created by a series connection of two inductors, as seen in Fig. 1-8 a). By coupling these two inductors together on a common core, as in Fig. 1-8 b), the windings can be arranged such that the fundamental ac frequency does not contribute to flux in the core - thereby keeping the coupled inductor small. Additionally, with the winding arrangement of Fig. 1.8 a), the fundamental ac output can change quickly as it is only limited by the leakage reactance of the core - giving similar transient characteristics as the stacked capacitor alternative.

Furthermore, whereas the split-capacitors provide a center tap voltage relative to the stored charge between the two capacitors, the split-wound coupled inductors inherently feature balanced output voltages as a result of voltage division in a fixed set of windings. Conversely, with split-capacitors, the topology must balance the charge stored in the capacitors - potentially at the cost of converter complexity. Additionally, due to the use of capacitors, the reliability of the converter is affected [1], a significant consideration in transportation applications.

In the low voltage application region, such as those applications given in Section 1.1, device voltages stress are not an issue. While traditional multi-level voltage sourced converters were developed to minimize device voltage stresses [1], it is therefore not obvious which topologies are ideally suited for the low voltage application region.

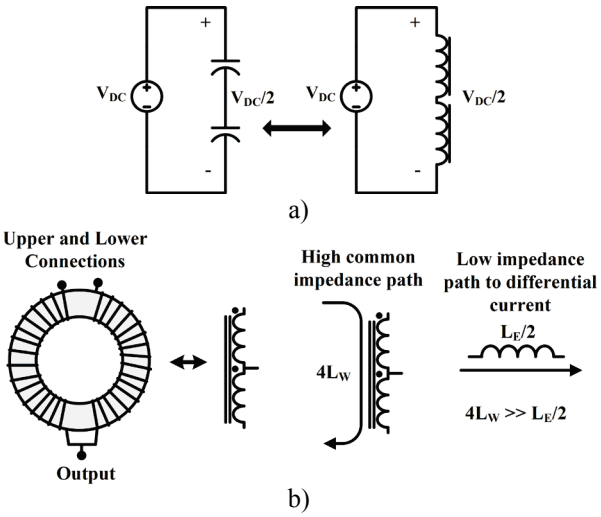


Fig. 1-8. a) Center-tapped capacitors and the equivalent center-tapped reactors providing access to half the dc-link voltage and b) split-wound coupled inductor arrangement with high ($4L_W$) and low impedance ($L_E/2$) states defined.

1.4 Thesis Objective and Outline

This thesis describes the asymmetric half-bridge combined with a split-wound coupled inductor as a basis for multi-level converter systems. This topology, as seen in Fig. 1-9, has two appealing aspects: three output voltage states ($V_{A,N}$) for two active devices and the natural balancing ability of coupled inductors due to the common core between two windings. In this thesis, the asymmetric half-bridge and split-wound coupled inductor topology is termed the *asymmetric coupled inductor bridge* (ACIB).

To clarify the operation in three-phase dc/ac applications, the ACIB is presented in Chapter 3 as a three-level, six-switch coupled inductor converter (SS-CIC). The three-phase coupled inductors can be integrated into a three-limb coupled inductor to save converter weight and costs. However, it is shown that the use of traditional interleaved PWM techniques produces inefficient converter operation due to the presence of common mode winding voltages. Therefore, to illustrate the challenges of eliminating these voltage states in the SS-CIC, a simple modification to a traditional PWM technique is discussed and experimentally examined.

While it is shown in Chapter 2 that the NPC topology is commonly applied in low voltage applications, Chapter 4 presents a NPC version of the ACIB for five-level, dc/ac converters, as seen in Fig. 1-10 a). This converter features five voltage levels with the same number of active devices as the three-level NPC - potentially allowing for low-cost, filter-less operation in applications such as flywheel battery systems. With the challenges identified in common mode winding elimination from Chapter 3, Chapter 4

uses space vector analysis to minimize these consequences to enable the use of a three-limb coupled inductor for compact operation of the five-level coupled inductor converter.

In Chapter 4, it is observed that the ACIB has a natural tendancy to balance the split-capacitor connection shown in Fig. 1-10 a). Taking advantage of this ability, the ACIB is presented in Chapter 5 as a modular balancing bridge for the automatic balancing of a series connection of batteries, as shown in Fig. 1-10 b). The balancing current produced by the ACIB is shown to be dependant on the parameters of the converter, and is related to a per-unit system for ease of design using a commercial line of transformers. Finally, these transformers are used to illustrate the balancing power relative to size possible with the ACIB-based automatic balancing converter.

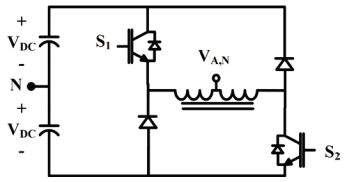


Fig. 1-9. The asymmetric half-bridge and split-wound coupled inductor

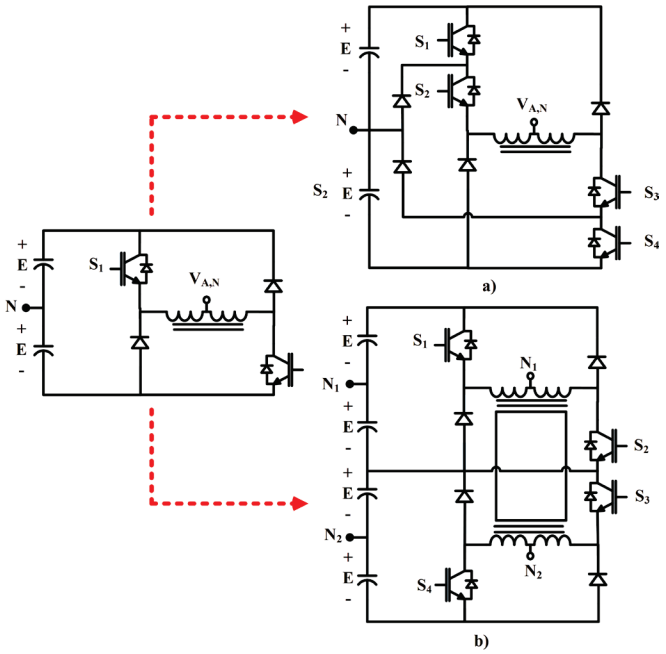


Fig. 1-10. The ACIB configured as a) a five-level, NPC, dc/ac coupled inductor converter, and b) a modular balancing bridge for voltage balancing with series connected voltage sources.

1.5 Thesis Contributions

The work presented in this thesis contributes to the development of coupled inductor based multi-level converter systems suited for low-voltage (i.e. less than 600V) applications.

The main contribution of this thesis are as follows:

- Presentation of three-limb coupled inductor operation for three-phase coupled inductor converters. The overall aim behind this contibution is to increase the power density of coupled inductor converters, and to extend the operating range to all switching frequencies.
- Identification of non-zero common mode winding states that exist when a three-limb coupled inductor is used in a three-phase coupled inductor converter, see Chapters 3 and 4.
- Presentation of a carrier-based modulation technique for the SS-CIC to highlight the challenges involved in the elimination of these common mode winding voltages, see Chapter 3.
- The development of a three-phase, five-level NPC coupled inductor converter (NPC-CIC) from the ACIB. By moving to a five-level platform, the potential to eliminate the output filter is possible, thereby increasing the power density of the multi-level converter, and lowing costs, as seen in Chapter 4.
- Based on the consequences of common mode winding elimination presented in Chapter 3 for the SS-CIC, a space vector approach is presented to minimize these consequences for the NPC-CIC, see Chapter 4.
- The development of a modular balancing bridge (MBB) based on the ACIB. The MBB can balance any number of voltage sources, independant of the characteristics of that voltage source, and without the requirement of cell voltage feedback. This low-cost approach is further enhanced by the complete modularity of the MBB, as seen in Chapter 5.
- The derivation of the balancing currents for balancing voltages internal to the MBB and for balancing voltages between MBBs to the per-unit circuit parameters. These per-unit circuit parameters are derived to aide in the design of the MBB for an arbituary number of voltage sources, and is related to a transformer size to illustrate the power density of the MBB, see Chapter 5.
- Use of the MBB as a balancing circuit for automotive applications, where the primary storage element is lithium ion (or polymer) battery strings. The MBB is presented with commercial (not custom) transformers, and without the requirement of voltage feedback or balancing co-ordination from a master battery controller, provides a low cost solution for the non-dissipative balancing of batteries.

Chapter 2 – Low Voltage Multi-level Converter Systems

In this chapter, background information is presented to place the contribution of this thesis in context. Firstly, a brief introduction to traditional three-phase, multi-level voltage source converters is given, and each topology is discussed in context to low voltage operation. Specific low-voltage multi-level pwm converter topologies are then highlighted, with research topics for both capacitor-based and inductor-based solutions identified. Secondly, a space vector modulation approach is used to reduce converter weight for the five-level coupled inductor converter presented in this thesis. Therefore, a review of multi-level pulse-width modulation is presented covering both carrier-based and space vector approaches. Lastly, since the automatic balancing feature of the ACIB is highlighted as a topological approach to balancing batteries, the state of the art in this subject area is discussed in brief.

2.1 General Three-Phase Multi-level Voltage Source Converters

Multi-level voltage source converters are widely deployed in medium voltage applications. However, some characteristics of these converter topologies are suitable for lower voltage application, a central topic of this thesis.

Historically, the first multi-level voltage sourced converter developed was the cascaded full-bridge converter, as seen in Fig. 2-1[13-19]. In this topology, each single-phase H-bridge requires separate dc power supplies, using either phase-shifted transformers [14] or individual battery cells [17]. Additionally, this topology allows for '2N+1' voltage levels – where N is the number of cells per phase – when each cell is charged to the same dc voltage, or the cascaded inverter is termed 'symmetric' [15]. Conversely, by using asymmetric voltage levels, i.e. each level has a different dc voltage, a maximum of 3^N levels can be present per-phase, but at the expense of asymmetric power losses in the converter [16].

The cascaded topology is not limited to single-phase H-bridges, and can also feature a combination of other multi-level topologies, such as the neutral point clamped inverters [19]. Such configurations are deemed 'hybrid inverters', as they mix the various topological approaches for conversion. Relative to lower voltage systems, a six-switch inverter with cascaded H-bridges has been shown for electric vehicle applications. This topology is motivated by the desire to remove the bulky inductors in the boost converter, which are often necessary to regulate the battery voltage [20]. Another variation called

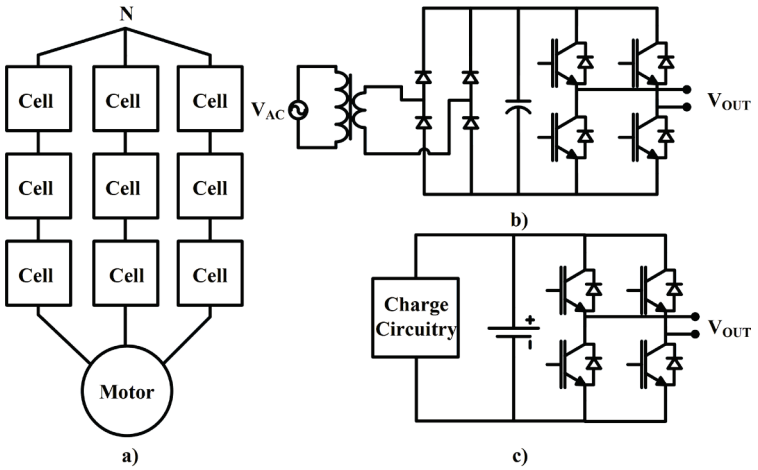


Fig. 2-1. The cascaded H-bridge topology a), with b) phase-shifted transformers and c) batteries supplying cell isolated cell

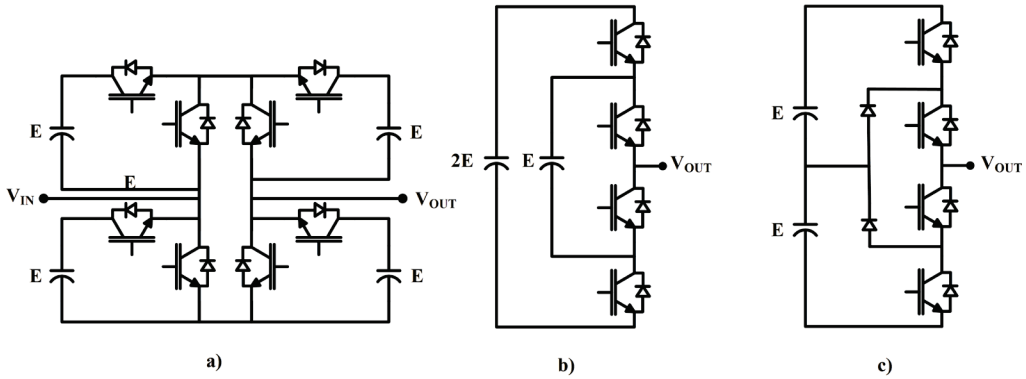


Fig. 2-2. Single-phase legs: a) multi-module converter (MMC), b) flying capacitor configuration (FC) and c) neutral point clamped based configuration (NPC)

the 'multi-module converter' or MMC, see Fig. 2.2 a), was developed in 1990 to reduce the filter requirements for high voltage, direct dc transmission systems (HVDC), but have shown to be ill-suited for variable speed drive systems [21, 22]. Overall, these topologies require either a large number of devices, or isolated power sources for each level, making low voltage application expensive.

The 'flying capacitor' configuration, Fig. 2-2 b), was invented in the late 1980s and requires only one input dc power source, but is not created from a modular concept - unlike the cascaded H-bridge converter [18, 23, 24]. Due to switching state redundancies, the floating capacitor voltage levels are regulated without external circuitry. However, this capacitor voltage regulation comes at the cost of increased device switching frequency [18]. Thus, due to the increased switching frequency, and large number of potentially unreliable capacitors being used, this topology is also not ideal for low voltage applications.

In 1982, the neutral point clamped (NPC) inverter, Fig. 2-2 c), was developed, which could also be powered by a single dc source. Additionally, for the three-level version, the split-capacitor connection can be regulated without any external circuitry or increase in device switching frequency [18, 25]. Therefore, out of the traditional medium voltage topologies, the NPC is the most suitable for low-voltage operation as it features simple modulation techniques, a small number of active devices and low switching losses (as this topology was motivated by lower the device voltage stresses).

2.2 Multi-level Voltage Sourced Converters suitable for Low Voltage

Several published works have recently highlighted the importance of using multi-level pulse-width modulated converters in low voltage applications [26]. The main topological trends in this area are described, i.e.: the neutral point clamped; T-type; and parallel converters using interleaved switching and inter-cell transformers (ICTs) or coupled inductors.

2.2.1 Neutral Point Clamped (NPC) Topologies

The three-level NPC inverter can have significant advantages over the standard two-level converter when the switching frequency is greater than 10 kHz [26-35]. This is because the switching losses are proportional to the commutation voltage, and for the NPC topology, this voltage is reduced by half [26]. Furthermore, when compared to other low voltage topologies, the actual devices can be rated for half of the input dc voltage, enabling the use of higher efficiency (but lower blocking voltage) devices.

The lower device voltage stress of the NPC topology also allows for application of either MOSFET or IGBT based devices [27-32]. As an example, at a switching frequency of 80 kHz, and an output power of approximately 6 kW, MOSFET-based three-level NPC converters have shown an improvement in efficiency of 2.5% over IGBT-based three-level NPC converters [27]. Note [27] illustrates the application of MOSFET based NPC converters, specifically for PMSM machines with low inductance, e.g. flywheel battery systems. Furthermore, [28] illustrates how MOSFET-based three-level NPC converters can be designed to incorporate floating gate driver designs - enabling a low cost, high efficiency converter option.

However, the three-level NPC topology has basic limitations in terms of loss distribution in amongst components [33-35]. Several works have investigated novel topological modifications to the three-level NPC inverter, and in particular, [33] highlights four variations, Fig. 2-3 a)-c), along with a T-type configuration. In particular,

the primary limitation of Fig. 2-3 a), i.e. the standard NPC configuration, is that the devices within a phase leg experience unequal losses, which varies with the load power factor. Thus, the active NPC topology can be used to redistribute these losses equally within the converter, enabling even higher power densities [34]. Furthermore, [33] then proposes Fig. 2-3 c), as a compromise between high asymmetric loss distribution and active device count. In this approach, the additional IGBTs do not require additional isolated power supplies, due to the common source connection with the inner IGBT pair of the NPC topology - potentially lowering the overall cost of Fig. 2-3 c).

In summary, for the low voltage region, the lower voltage stresses of the NPC topology enable the use of MOSFETs over IGBTs. While the NPC topology does experience asymmetrical losses, the advantages in higher switching frequency applications make this topology appealing as a low-voltage converter topology.

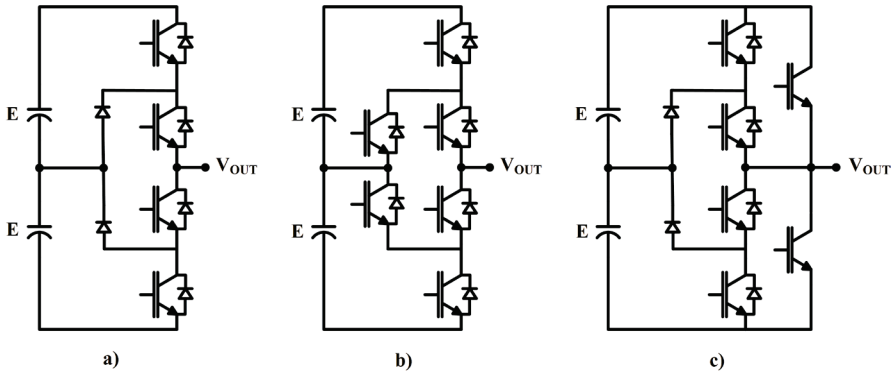


Fig. 2-3. NPC-based topologies: a) general NPC, b) Active-NPC, and c) Hybrid-Active NPC

2.2.2 T-Type Converters

In low voltage applications, the reduction in losses is of greater importance than the particular blocking voltage of the devices within a topology, motivating the 'T-type' inverter topology [35-37] – named for the characteristic appearance of each inverter leg, as seen in Fig. 2-4. While the overall device count can be similar for the T-type converter compared to the NPC topology, it is possible to eliminate one gate driver per leg (which can be comparable in cost of the actual device) [36]. However, the main advantage to this topology is the reduction of conduction losses (as compared to the NPC topology), due to a lower number of series-connected devices, and switching losses, due to the reduced commutation voltage (as compared to the standard two-level topology) [37].

However, since the main devices still must block the full input dc voltage, higher voltage devices must be used, and therefore, depending on the operating voltage and

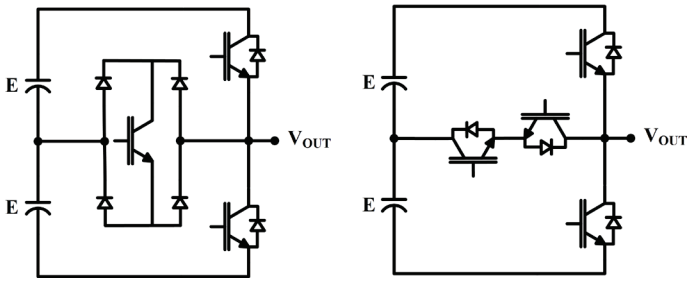


Fig. 2-4. Two T-type configurations based on bi-directional devices: a) single switch and b) dual switch, back-to-back configuration

switching frequency, the overall efficiency can be less than the NPC inverter. A further investigation of which topology is ideal under various power/switching frequencies, [33] compares the distribution of losses in a T-Type inverter and a NPC inverter. The main conclusion from [33] is that the T-type converter is ideal for medium switching frequencies (10-20 kHz, due to conduction losses dominating), with the NPC being ideal for higher switching frequencies.

2.2.3 Three-phase Paralleled Converters with Reactors

In industrial applications, paralleling three-phase converters is a common practice to cope with increasing power requirements [38]. Additionally, as in parallel dc/dc converters [39, 40], the switching of the three-phase converters can be interleaved, and with an inter-cell transformer (ICT), used to produce multi-level PWM outputs. With this approach, the required passive filter sizes are reduced and the effective switching frequency is increased [41-61]. This section explains the basic concepts in parallel three-phase converters (with interleaved switching), and highlights key research areas with these converters.

2.2.3.1 Parallel Three-phase Converters

Consider the single-phase leg in Fig. 2-5 a) and its two parallel configurations in Fig. 2-5 b) and c). Note that the output filter 'L_{AC}' has been fixed for a given phase current ripple at the output of the topologies given in Fig. 2-5 a)-c). In the paralleled configuration of Fig. 2-5 b), the output current splits between the two converter legs, reducing the current stress in each leg by half. However, to fix phase current ripple magnitude to the converter in Fig. 2-5 a), the output filters in Fig. 2-5 b) are $2L_{AC}$ (this does not imply that the filter increases in size, only that the inductance is increased). If a center-tapped coupled inductor is placed between the two converter legs, as in Fig. 2-5 c), and the pulse-width modulation is 'interleaved', a three-level voltage output is created at

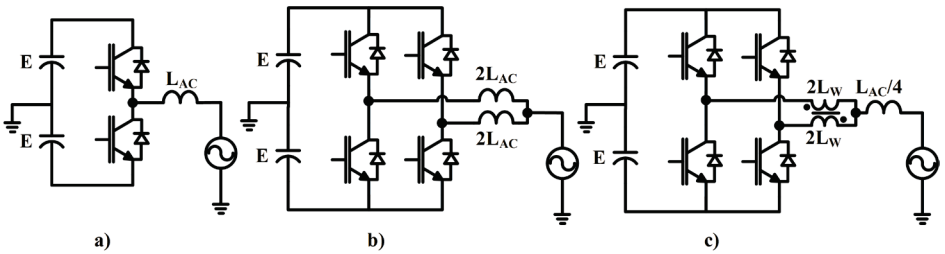


Fig. 2-5. Single phase legs of filtered VSI topologies: a) half-bridge, b) parallel half-bridges and c) parallel half-bridges with ICT and interleaved switching.

twice the carrier frequency - thereby reducing the required filter inductance to $L_{AC}/4$ [57-61].

Interleaved switching refers to the amount of carrier overlap that exists for each converter phase leg of Fig. 2-5 b) and c). Considering the parallel converter case, shown in Fig. 2-5 b), the PWM output of each converter leg is interleaved, by a time T_D, because of the phase difference in each carrier, as shown in Fig. 2-6. In this manner, the overlap of voltages between the two legs (i.e. $V_1 + V_2$) causes a component of current to flow between converters ($i_1 - i_2$, in Fig. 2-6), restrained only by the inductance common to each converter. This circulating current component is commonly referred to as the 'differential mode' circulating current [45, 48, 52]. Moreover, as the PWM voltage common to each leg is at the PWM switching frequency, these harmonic components are removed from the ac output path, doubling the effective switching frequency. Furthermore, for three or more sets of parallel converters, the effective switching frequency is similarly tripled, quadrupled, and so forth - allowing for a significant benefit for low-voltage, high current systems limited by the device switching frequency [46].

As the amount of carrier overlap increases, due to the coupling of windings in the ICT, the presence of the low frequency ac flux is increasingly reduced for the converter arrangement in Fig. 2-5 c) [50-53, 58]. To appreciate how this result is possible, note Fig. 2-7 a) and the corresponding coupled inductor models shown in b) and c) of that figure. As analyzed in [51, 52], from the common path linking port (1) to (2) in Fig. 2.7 b), the total inductance seen is $4L_1$ (if $L_1 = L_2 = M_{12}$). However, for the differential output path, i.e. (1) and (2) to (3) in Fig. 2-7 c), the effective inductance is $(L_1-M_{12})/2$ - which is half of the leakage inductance of the coupled inductor. Thus, if the switching is interleaved such that the ac output is produced by the differential of the two converters, then the ac flux does not exist in the coupled inductor - enabling a dramatic size reduction [56].

The filter mass reduction, e.g. as demonstrated in [58], is only possible with interleaved switching. In particular, with a carrier phase angle difference of 180° or $T_D =$

$T_S/2$ in Fig. 2-6 b), the interleaved switching angle produces its maximum amount of circulating differential current at the switching frequency of the converter. In addition, relative to the output, i.e. ports (1) and (2) to (3), are 180° out of phase, producing a three-level voltage at the output, i.e. $(V_1+V_2)/2$. Therefore, the output voltage step across the load is reduced by half by interleaved switching and, since the differential component is not present at the output, cancellation of the odd order switching harmonics, producing an effective filter reduction of 4 when compared to the single phase leg of Fig. 2-5 a).

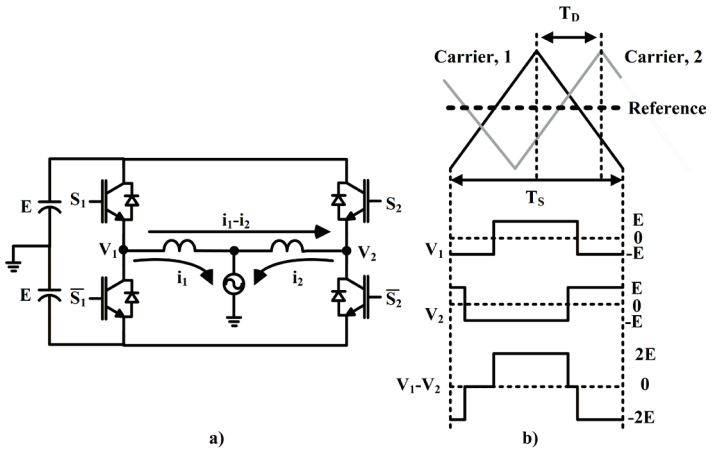


Fig. 2-6. Paralleled half-bridges a) showing the module currents i_1 and i_2 for a general interleaving period T_D and b) general interleaving time T_D between two carriers in a parallel three-phase converter with output module voltages and differential voltage labelled

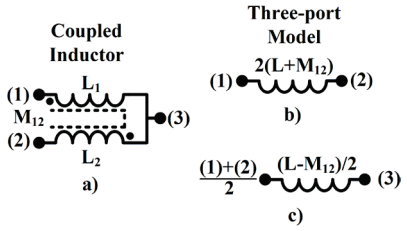


Fig. 2-7. Coupled inductor with a) general mutual coupling, M_{12}, between L_1 and L_2, with b) impedance from port (1) to (2) and c) impedance from ports (1) and (2) to port (3), due to coupling M_{12}. L is the self-inductance of a winding.

2.2.3.2 Research Trends in Three-phase Parallel Converter Systems

While parallel converters offer the potential to decrease the filter mass and improve the conversion quality/efficiency [52, 56], several issues exist relating to the 'differential mode' circulating current, as depicted in Fig. 2.6 as 'i_1- i_2'. This section highlights the limitations of paralleled three-phase converters and the research that exists to mitigate these problems.

In parallel three-phase converter systems, e.g. for utility applications, non-ideal device characteristics can cause circulating currents to exist, regardless of whether the switching is interleaved or not [36, 44, 48]. With a large number of parallel converters, these device characteristics can cause dc currents to flow, potentially saturating the filter inductors. When the switching is interleaved, non-ideal device effects can cause net drifts in the circulating current component, often with both low and high frequency components present [48]. To control the high-frequency circulating component, passive components, such as common mode chokes, are often employed [41].

The choice of the pulse-width modulator for each three-phase module also plays a significant role in the low-frequency component of the circulating current [38, 45, 48]. In [38], the power distribution of parallel modules is controlled with a fundamental phase shift, but due to the use of space vector modulation (SVM) in each converter, certain switching states can cause large circulating currents. Therefore, [38] focuses on the development of a current control regulator that allows for independent power sharing between parallel modules, but mitigates the low frequency circulating component up to certain modulation depths.

Furthermore, with discontinuous modulation, with the attractive benefit of having lower switching losses, methods for parallel converters have been the subject of much research. Like [38], the focus is on the restraint of the low frequency circulating currents that can cause excessive losses in the system [48, 49]. Additionally, the impact of the interleaving angle (i.e. not fixed at 180°) on the passive component (i.e. filter sizes) is the subject of [58-60]. In these latter works, that while the interleaving carrier angles of 180° produce the smallest ICT size, other angles can reduce the ac filter size by spreading the resultant converter switching harmonics across higher frequencies.

Finally, modulation schemes for parallel inverters have not been limited to just circulating current regulation. In parallel converters, with interleaved switching and ICTs, modulation schemes can reduce the dc-capacitor size [57], peak flux density present in the ICTs [56] and improve the conversion quality [52].

2.2.3.3 Advanced Coupled Inductor Based Topologies

While parallel converters exist in many practical industrial applications, e.g. active filters [44], novel converter topologies have also been developed with ICTs (or split-wound coupled inductors). Due to the attractive characteristics of ICT based multi-level conversion, this section details a few topologies that move outside the typical two-

module parallel converter system. While much research has been published on coupled inductors as a basic building block for filters and in converters, [62, 63]; coupled inductor based converter topologies can essentially be grouped into two categories: parallel-based, with identical modules configurations used, or hybrid topologies, which are a combination of traditional multi-level voltage sourced inverters and coupled inductors.

In parallel systems with more than two modules, e.g. four modules in Fig. 2-8 a), [64] and [50, 51] illustrate two methods of coupling the four converter legs together: electrically, Fig. 2-8 a), with single phase cores shown in Fig. 2.8 b) [64], or with combined 'monolithic' magnetic cores, as shown in Fig. 2-8 c) [50, 51]. These monolithic cores are the subject of [50], where several configurations are presented for multi-module systems. In addition, the electrical configurations of Fig. 2-8 a) is one of seven possible, as per [65]. Two such examples are the 'whiffle-tree' and the 'combinatorial shunt', as shown in Fig. 2-9 a) and b).

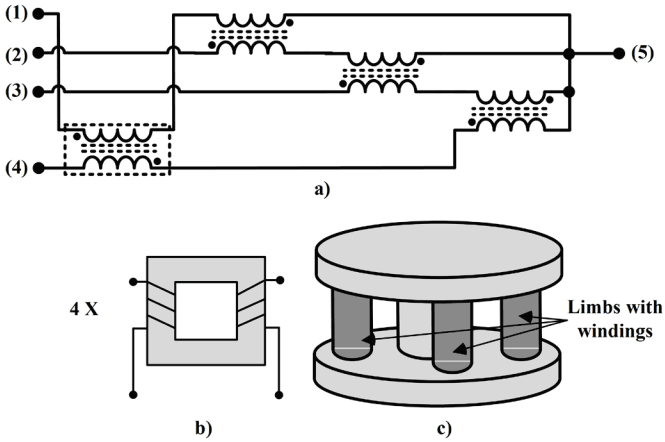


Fig. 2-8. Four winding cascaded coupled inductor a) electrical equivalent circuit as implemented with b) single phase reactors or c) monolithic reactors

In terms of parallel-based topologies, three-phase converters have been demonstrated in triplen configurations [66]. By using three-limb modules per phase, as shown in Fig 2-10 a), commercial transformer cores can be used, lowering the converter cost. With four parallel modules, as seen in Fig. 2-10 b), [67] demonstrates the operation of a five-level converter based on using the standard two-level converter and the whiffle-tree inductor arrangement of Fig. 2-9 a).

Fig. 2-10 c) and d) illustrate coupled inductor converter topologies that arise from a single-phase coupled inductor, and a traditional multi-level voltage sourced inverter configuration. As an example, Fig. 2-10 c) demonstrates an active neutral point clamped configuration that uses a coupled inductor stage at the output to create a five-

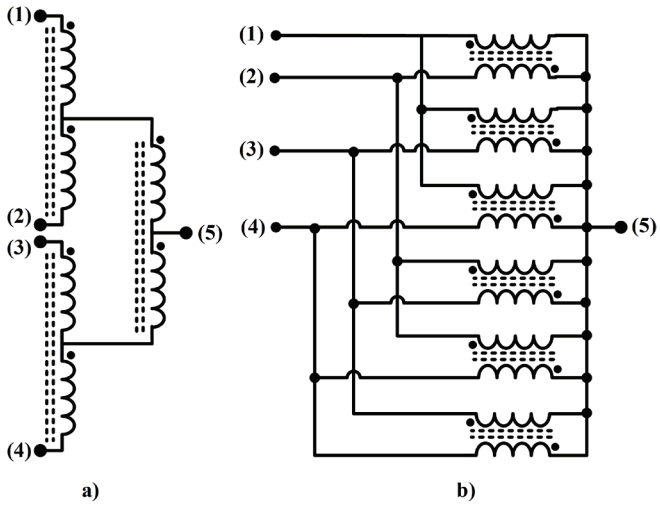


Fig. 2-9. Four winding coupled inductor configurations: a) whiffle-tree and b) combinatorial shunt configurations [67]

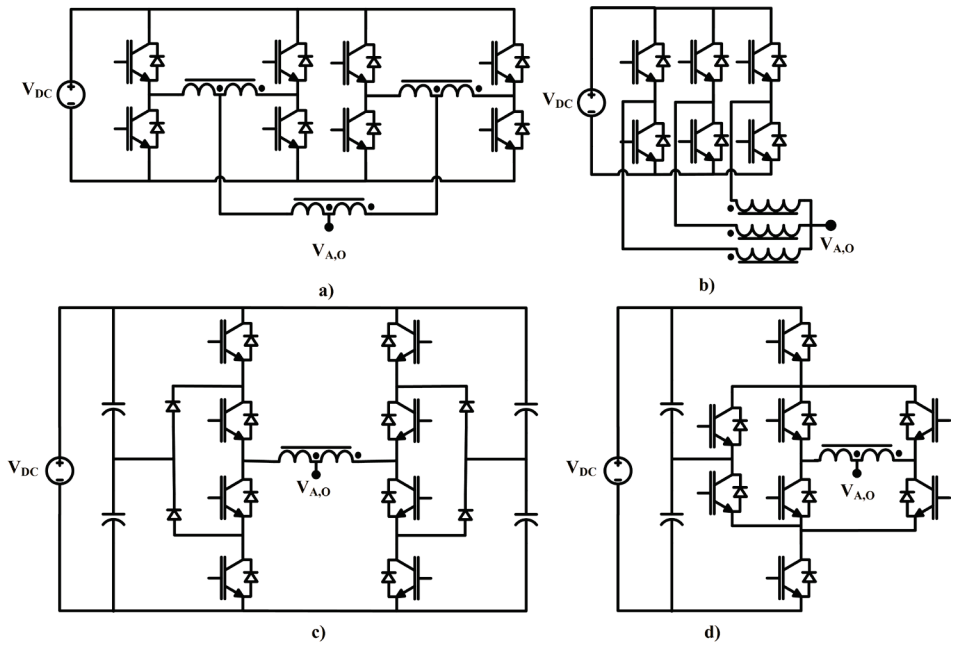


Fig. 2-10. Single phase legs for parallel-based converters a) 5-level whiffle tree based, b) 4-level six-switch per phase with three-limb coupled inductor, c) NPC-based and d) ANPC with internal coupled inductor

level inverter with eight active devices [68]. A benefit of the topology is that the 'coupled inductor' stage does not see the full dc voltage, and therefore small inductor sizes are possible. In Fig. 2-10 d), a three-level NPC converter is paralleled to create a five-level PWM converter [67], and a five-level NPC converter is paralleled to create a seven-level PWM converter. [69]. Other configurations exist which combine topological functions, i.e. a buck-boost inverter from an 'Inverse Watkins-Johnson' topology [70], or a high-

quality audio amplifier based on a standard parallel half-bridge, using a switched center point to create a single-phase five-level inverter [71].

Clearly, in the low voltage domain, a large variety of multi-level converter topologies exists, as demonstrated by the wide variety of topologies discussed in this section.

2.3 Pulse-width Modulation in Multi-level Voltage Sourced Converters

In this thesis, space vector modulation (SVM) is used to allow for an integrated three-limb coupled inductor in a five-level coupled inductor converter. Therefore, background information is presented on the concepts behind multi-level SVM to appreciate some of the contributions made by this thesis. However, basic two-level SVM must first be presented to understand the concept of multi-level SVM. In addition, terminology used for carrier-based multi-level modulation is also presented, as these schemes are used throughout the thesis.

Furthermore, as digital controllers are commonplace in commercial applications, this thesis will only consider regular sampled pulse-width modulation [72]. Regular sampled modulation refers to implementation with up/down counters with modulating reference sampled at every carrier interval.

2.3.1 Space Vector Modulation for a Two-level Voltage Sourced Converter

Developed in the mid-1980s, space vector modulation is a digital pulse-width modulation technique that improves the dc-bus utilization by 15.4% over traditional sinusoidal pulse-width modulation, while also providing better conversion quality [73]. This pulse-width modulation technique has become the standard in industrial applications today, in part due to its ease in digital implementations [73]. As an example of recent topics in this area, SVM has been extended to novel converter topologies [74], common mode voltage elimination [75], and noise reduction [76].

The operation of SVM models the three-phase inverter outputs as a state machine, e.g. {E,-E,-E}, which synthesizes the output voltage based on the nearest vectors, or states. The output of each phase leg of the three-phase converter, as seen in Fig. 1-6, can either be either 'E' or '-E', depending on the state of the power electric switch; note these outputs are given as the integer multiples of 'E' for simplicity, e.g. '1' or '-1' on Fig. 2-11. Since the application considered is a three-phase, three-wire system, the phase voltages sum to zero and therefore, one phase is a linear combination of the remaining two. Thus, two variables describe the three-phase system, and the phase output

voltages map to the real and imaginary plane, creating the complex output voltage, as per (2.1).

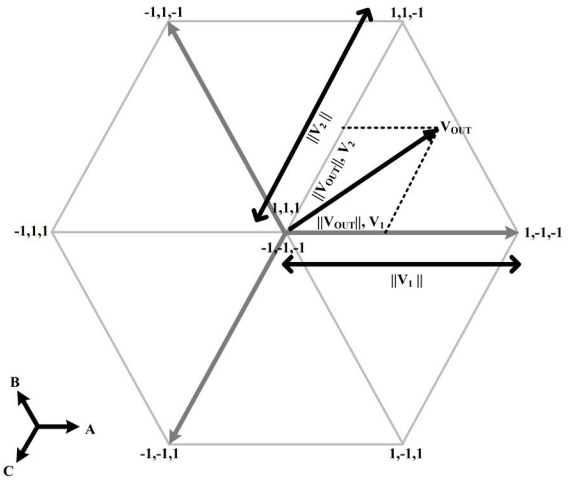


Fig. 2-11. Two-level space vector map showing phase output vectors {A,B,C} and a reference voltage vector, V_{OUT}, with vectorial lengths depicted. '$||V_{OUT}||$, V_1' refers to the length of vector V_{OUT} projected onto the vector V_1. Converter states are scaled by 'E', e.g. {E, -E, -E} to {1,-1,-1} for simplicity.

$$V_{OUT} = V_{A,N} + V_{B,N} \cdot e^{-j\frac{2\pi}{3}} + V_{C,N} \cdot e^{-j\frac{4\pi}{3}} \tag{2.1}$$

Considering the possible phase voltage combinations of the two-level VSC, the resulting 'space vector map' is depicted in Fig. 2-11. The desired output voltage, V_{OUT}, is located in Fig. 2-11, between active vectors V_1 and V_2, and the length of the vector, V_{OUT}, is relative to the maximum output voltage $V_{DC}/2$ by the modulation depth, m_A. The length of V_{OUT} can then be decomposed into components using the basis of V_1 and V_2, and then scaled by the lengths of V_1 and V_2, with the ratio denoted as d_1 and d_2. These are the active duty cycles necessary to achieve the average voltage of V_{OUT}, from the bounding vectors. As an example, in the first sextant, these duty cycles are calculated via (2.2).

$$d_1 = m_A \sin\theta, \quad d_2 = m_A \sin(\pi/3 - \theta) \tag{2.2}$$

However, to produce the correct average output voltage, the 'zero vectors', i.e. {1,1,1} and {-1,-1,-1}, which produce no voltage from phase to phase, must be switched for the remaining duration of the switching cycle, i.e. (2.3). In order to minimize distortion, the order of vectors selected should be T_Z, T_1, T_2, for half the carrier cycle, with the reverse sequence following [72]. Therefore, the duty cycles d_1, d_2 and d_Z should scale to half the switching period, $T_S/2$, to achieve the durations T_1, T_2, and T_Z, (2.4).

$$d_Z = 1 - d_1 - d_2 \tag{2.3}$$

$$T_1 = d_1 \cdot \frac{T_S}{2}, \quad T_2 = d_2 \cdot \frac{T_S}{2}, \quad T_Z = d_Z \cdot \frac{T_S}{2}, \tag{2.4}$$

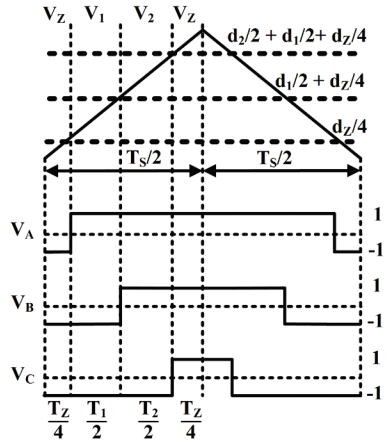


Fig. 2-12. Synthesis of V_{OUT} in Fig. 2-11, over switching period T_S, based on the vectors V_1, V_2 and V_Z in center-aligned space vector modulation

Furthermore, in order to minimize the switching frequency, Holmes *et al.* [72] states that the transition from one vector to the next should produce only one switching transition. Therefore, for 'center-aligned' space vector modulation, both zero state vectors are used, with the duration equally distributed, i.e. $d_Z/4$, per half carrier cycle. Over a switching cycle, the output voltage, V_{OUT}, is then synthesized, as demonstrated in Fig. 2-12. Over a fundamental cycle, the equivalent analog reference signal for phase A in space vector modulation is illustrated in Fig. 2-13. It has been demonstrated that the space vector implementation and carrier based schemes are equivalent, but for an offset added to the sinusoidal reference. This offset is given in (2.5), as described in [72].

$$V_{A,N}^{*} = V_{A,N} - \frac{\max(V_{A,N}, V_{B,N}, V_{C,N}) + \min(V_{A,N}, V_{B,N}, V_{C,N})}{2} \tag{2.5}$$

While the 'center-aligned' space vector modulation described above minimizes the current distortion, 'discontinuous' modulation techniques have also been developed - which sacrifice conversion quality at low modulation depth for a reduction in the average switching frequency. In discontinuous modulation, the two zero vectors, i.e. '{1,1,1}' and '{-1,-1,-1}', need not be symmetrically distributed at the beginning and end of the half-switching cycle, as shown in Fig. 2-12 [77]. Rather, discontinuous modulation techniques minimize the switching frequency by holding a device inactive for an entire 60° of a fundamental cycle, and therefore only uses one zero vector per switching cycle. With each phase reference being cyclic, this results in 120° of switch inactivity out of 360° over the fundamental cycle. As the zero voltage vectors result in zero voltage from phase to phase, the line voltage is not affected and the average voltage to the three-phase load is maintained.

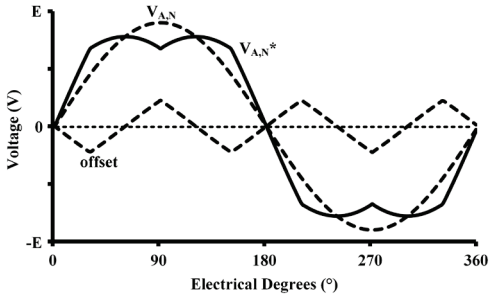


Fig. 2-13. Phase voltage reference over a fundamental cycle for SVM, with offset, at a modulation depth of 0.9.

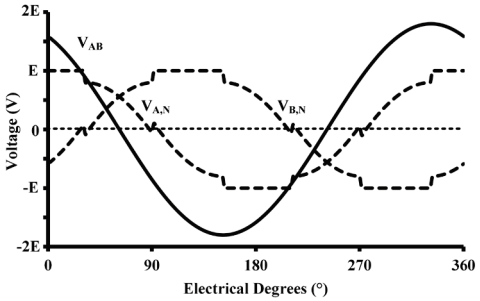


Fig. 2-14. Phases A and B references under DPWM1 with resultant line voltage, V_{AB} over a fundamental cycle

There are several methods of discontinuous modulation, varying with where the inactivity occurs in the fundamental cycle. DPWMMIN and DPWMMAX refer to using only one zero vector for the entire fundamental cycle, and therefore, each phase has a region of inactivity, where the phase voltage is clamped high or low for an entire 120° [78]. Whereas DPWM2 and DPWM3 alternate the zero vectors per 60°, but differ on when the inactivity occurs. Ideally, the switch inactivity occurs when the phase current is at its peak: reducing the switching losses by one-third. Lastly, DPWM1 clamps the phase reference at 30° around the peaks of the phase reference, and is shown in Fig. 2-14.

2.3.2 Multi-level Carrier based Techniques

While modulation techniques, such as 'phase-shifted PWM' for cascaded H-bridges exist as summarized in [73], the primary focus of this section is to introduce the carrier-based modulation concepts for the multi-level NPC converter. This focus is due to the similar modulation concepts used between coupled inductor converters (with interleaved switching) and NPC converters.

In general, the 'N' level, three-phase NPC converter is modulated by 'N-1' carriers. Furthermore, there are three main configurations of the carriers: alternative phase opposition (APOD), phase opposition disposition (POD) and phase disposition (PD) [72]. Note that the standard two-level six-switch VSC has only one carrier, and therefore all carrier schemes are equivalent for this converter.

With a five-level converter, each carrier based modulation scheme has four carriers, which occupy four different segments, as shown in Fig. 2-16. With POD modulation, in Fig. 2-15 a), the carriers above and below the zero reference are phase shifted by 180°, whereas with APOD modulation, as in Fig. 2-15 b), each carrier is 180° out of phase with its neighboring carriers. However, the best conversion quality is

obtained by using PD modulation, which has all carriers in phase for each carrier band, as illustrated in Fig. 2-15 c). While more detailed analysis of these modulation schemes exists (particularly for the wide variety of multi-level topologies), they are briefly covered here to familiarize multi-level carrier-based PWM concepts and terminology, as used in Chapter 3.

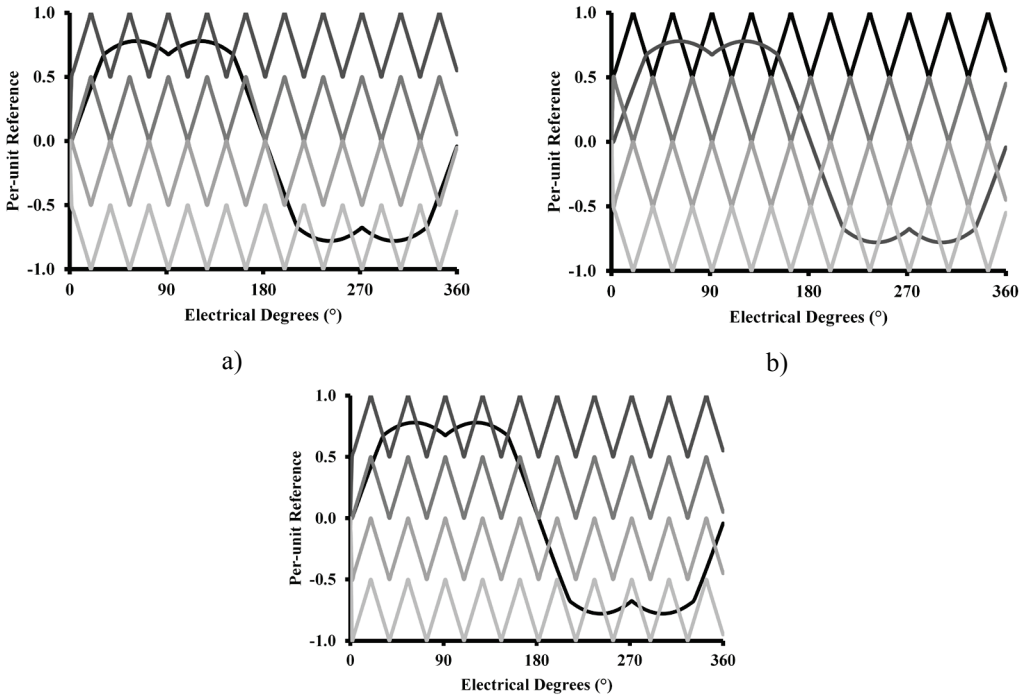


Fig. 2-15. Five-level carrier based modulation for NPC based converters with a) POD, b) APOD and c) PD arrangement of carriers

2.3.4 Space Vector Modulation for Multi-level Inverters

Multi-level SVM is extended from the two-level SVM approach. However, there are two major points of consideration: the possible switching states is substantially more when compared to the two-level VSC, and the selection of vectors now depend on modulation depth (m_A), as well as angular position of V_{OUT}. This section discusses the basic concepts of multi-level SVM as applied to a five-level three-phase NPC converter. This discussion is necessary as multi-level SVM techniques are used to eliminate unwanted voltage states in the five-level coupled inductor converter.

Using the possible phase voltage outputs and (2.1), the space vector map of a five-level NPC converter is pictured in Fig. 2-16. Note here that the maximum voltage level is denoted '2' and '-2' for simplicity over fractional values of the dc-link, i.e. instead

of '2E' and '-2E'. Compared to the two-level VSC, the five-level space vector map has 96 equilateral triangles, with a total of 512 vector combinations, resulting in 61 unique output voltage states. Whereas the two-level VSC only has one output voltage state with two redundant vectors, the five-level converter has a maximum of five redundant vectors, decreasing by 1 per level until the outside edge, as shown in Fig. 2-16.

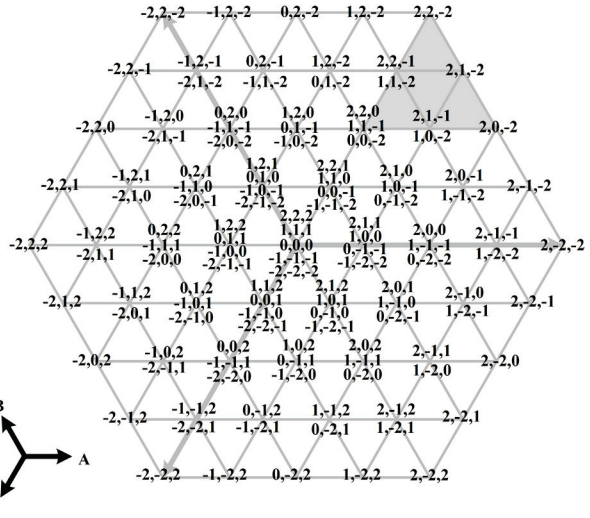


Fig. 2-16. Five-level space vector map showing phase voltage states {A, B, C} and the highlighted triangle for Fig. 2-17. Converter states, e.g. {2E, -E, -2E}, are scaled by 'E', e.g. {2,-1,-2} for simplicity.

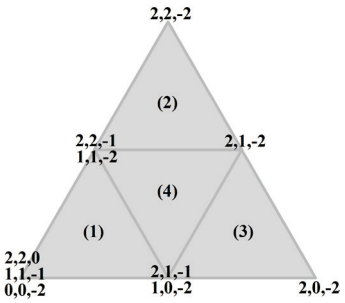


Fig. 2-17. Highlighted group of triangles from Fig. 2-17 with labelling (1)-(4)

Due to these redundant vectors, two guidelines for selecting the appropriate vectors are as follows [79]:

- Select two vectors where the number of redundant vectors will be an even number, and consequently, the remaining vector will be selected from the vertex with odd number of redundant vectors
- Select one vector from the vertex with an even number of redundant vectors, and the remaining two vectors are selected from vertices with an odd number of redundant vectors

Consider Fig. 2-17, which is the highlighted four triangles of Fig. 2-16, and their bounding vertices (as well as their redundant vector combinations). With the two conditions as per [79], and assuming center alignment of the zero vectors, triangles (1) and (4) have multiple choices for vectors used. However, knowing that only one switching cycle must occur per vector transition, and due to the neighboring vectors, these choices are eliminated to achieve an optimized operation. Note that triangles (2) and (3) only have one vector sequence: {2,2,-1}, {2,2,-2}, {2,-1,-2}, {1,1,-2} and {2,1,-1}, {2,1,-2}, {2,0,-2}, {1,0,-2} respectively.

Specifically, triangle (1) has the vector sequences:

a) {2,2,0}, {2,2,-1}, {2,1,-1}, {1,1,-1}
b) {0,0,-2}, {1,0,-2}, {1,1,-2}, {1,1,-1}
c) {2,1,-1}, {1,1,-1}, {1,1,-2}, {1,0,-2}
d) {2,2,-1}, {2,1,-1}, {1,1,-1}, {1,1,-2}

Similarly, triangle (4) has two possible sequences:

a) {2,1,-1}, {2,1,-2}, {1,1,-2}, {1,0,-2}
b) {2,2,-1}, {2,1,-1}, {2,1,-2}, {1,1,-2}

On examination of these latter two vector sequences, it is clear that these are most similar to sequences c) and d) for triangle one, but for one vector in each sequence. Therefore, to minimize the switching transitions, only c) and d) of triangle (1) and a) and b) of triangle (4) are used. According to [79], all odd vectors with greater than two redundancies will only result in one vector being used, if the lowest number of switching transitions is desired. Similarly, all even vectors greater than three will only use two vectors of even redundancy to achieve 'optimal' switching within SVM.

Unlike the two-level VSC, where the angular position of V_{OUT} determines which triangle (or bounding vectors) is to be used, the appropriate triangle in multi-level VSCs also depends on the modulation depth of V_{OUT}. As the number of voltage levels increases, the determination of this triangle location becomes increasingly computationally difficult, and therefore algorithms have been developed to simplify this procedure for a general N-level NPC converter, e.g. [80]. With the appropriate bounding vectors known, the duration of these vectors (or duty cycles) is calculated in order to synthesize the output voltage.

In [80], the multi-level SVM algorithm begins with the assumption that the line voltages of three-phase inverters sum to zero, and only two variables are needed to describe the vector locations (i.e. $V_A + V_B + V_C = 0$, thus one voltage can be expressed as

the sum as the remaining two). Therefore, a set of non-orthogonal vectors are selected as a new basis, creating a 'hexagonal' co-ordinate system as defined in (2.6). Note that these vectors are selected using the line voltages, and not the phase voltages.

$$\{\vec{g}_{(V_{AB},V_{BC},V_{CA})},\vec{h}_{(V_{AB},V_{BC},V_{CA})}\}=\{\begin{bmatrix}E\\0\\-E\end{bmatrix},\begin{bmatrix}0\\E\\-E\end{bmatrix}\} \tag{2.6}$$

The reference vector, e.g. V_{REF}, is then transformed into a two-dimensional co-ordinate system using the transformation matrix, T, as defined in (2.7), using (2.8), as developed in [80].

$$V_{REF(g,h)}=T\cdot V_{REF(V_{AB},V_{BC},V_{CA})} \tag{2.7}$$

$$T=\frac{1}{3E}\cdot\begin{bmatrix}2&-1&-1\\-1&2&-1\end{bmatrix} \tag{2.8}$$

Taking (2.7) and (2.8) and applying it to the five-level NPC converter results in the space vector map depicted in Fig. 2-18, but expressed in the hexagonal co-ordinate system (as opposed to an orthogonal co-ordinate system). After the transformation, the reference voltage is bounded by an equal-sided parallelogram, with the bounding vectors found via (2.9).

$$\begin{aligned}\vec{V}_{ul}&=\begin{bmatrix}\lceil V_{REF(g)}\rceil\\\lfloor V_{REF(h)}\rfloor\end{bmatrix}\\\vec{V}_{lu}&=\begin{bmatrix}\lfloor V_{REF(g)}\rfloor\\\lceil V_{REF(h)}\rceil\end{bmatrix}\\\vec{V}_{uu}&=\begin{bmatrix}\lceil V_{REF(g)}\rceil\\\lceil V_{REF(h)}\rceil\end{bmatrix}\\\vec{V}_{ll}&=\begin{bmatrix}\lfloor V_{REF(g)}\rfloor\\\lfloor V_{REF(h)}\rfloor\end{bmatrix}\end{aligned} \tag{2.9}$$

This parallelogram is composed of two equal-sided triangles, and the vectors V_{lu} and V_{ul} are always two of the three vectors nearest to the reference voltage. The last vector can be determined from the expression, (2.10), as per [2.69].

$$V_{REF(g)}+V_{REF(h)}-\left[\left(\vec{V}_{ul}\right)_g+\left(\vec{V}_{ul}\right)_h\right]>0 \tag{2.10}$$

If (2.10) is true, then V_{uu} is the last vector in the triangle bounding the reference vector, otherwise, V_{ll} is the vector. By knowing the co-ordinates of the bounding triangle for the reference vector, the duty cycles can easily be determined, with (2.11) being the expression if V_{ll} is the last vector of the triangle, and (2.12) otherwise.

$$\begin{aligned}d_{ul}&=V_{REF(g)}-\left(\vec{V}_{ll}\right)_g\\d_{lu}&=V_{REF(h)}-\left(\vec{V}_{ll}\right)_h\\d_{ll}&=1-d_{ul}-d_{lu}\end{aligned} \tag{2.11}$$

$$d_{ul} = -V_{REF(g)} + \left(\vec{V}_{ll}\right)_g$$
$$d_{lu} = -V_{REF(h)} + \left(\vec{V}_{ll}\right)_h \quad (2.12)$$
$$d_{uu} = 1 - d_{ul} - d_{lu}$$

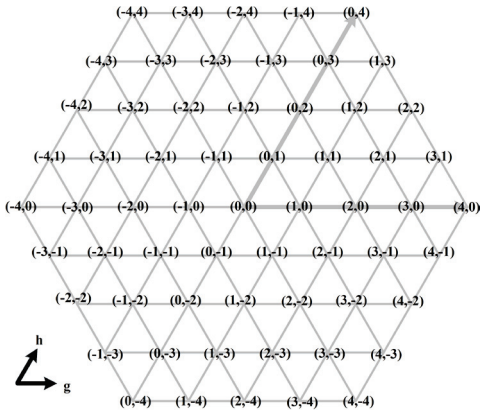


Fig. 2-18. Five-level space vector map showing phase voltage states in the {g,h} domain

2.4 Voltage Balancing Circuits

In this thesis, due to tightly coupled windings within the split-wound coupled inductor allowing for a natural balancing effect in series-connect voltage sources, a configuration of the ACIB is presented as a solution for balancing battery voltages. Therefore, to develop an appreciation for the contributions of the proposed balancing circuit, a review of the major voltage balancing methods is necessary.

The problem of balancing of voltage sources is not unique to batteries. In fact, ultra-capacitors [81], split-capacitor dc/dc converters [82], and multi-level pwm inverter systems [83] also present difficulties with unbalanced voltages. Specifically, for a five-level NPC converter, Fig. 2-19 a) illustrates a solution presented in [84] that balances the four capacitors of this converter. Unlike three-level NPC converter, which can balance the split-capacitor connection within the modulation strategy, four levels or more require an external balancing circuit for stable operation [84]. With split-capacitor dc/dc boost converters, Fig. 2-19 b) illustrates a single-switch solution that automatically balances four capacitors with no closed loop control, as per [82]. Finally, Fig. 2-19 c) is an asymmetric half-bridge, which actively balances split-capacitor connections on multi-level PWM converters, [83], and has also been applied to ultra-capacitor systems. Note that while this thesis focuses on balancing battery voltages, the ACIB-derived circuit balances arbitrary voltage sources, as the balancing property exhibited by this topology is not specific to the type of voltage source being balanced (e.g. lithium ion or nickel metal hydride batteries versus capacitors).

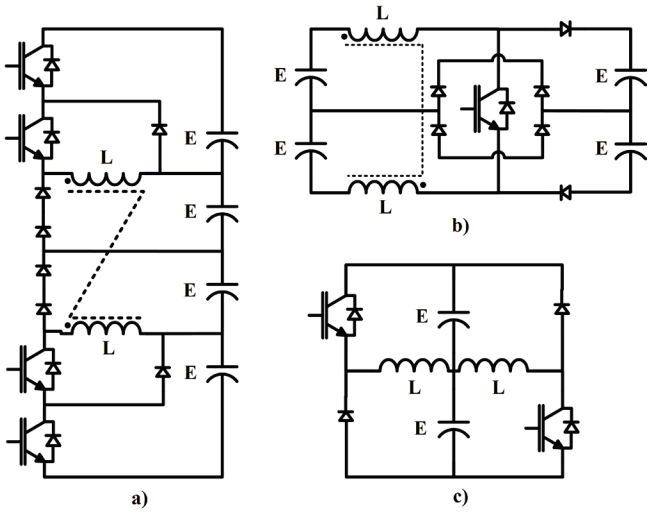


Fig. 2-19. Voltage balancing circuits a) for a five-level NPC converter [85] b) split input and output dc/dc boost converter [83] and c) fault tolerant 3-level NPC operation [84]

However, for the balancing of serially connected batteries, depending on whether energy is recovered during the balancing process, the approaches can be split into the following categories [85, 86]:

- Dissipative
- Non-dissipative

With non-dissipative circuits, i.e. circuits that do not dissipate energy as heat during the balancing procedure, the major categories are:

- Capacitor Charge Shuttling
- Current Shunting
- Converter Based Balancing

2.4.1 Dissipative Balancing Circuits

The simplest method of ensuring balanced voltages is to use a series connection of resistors across each battery cell, as per Fig. 2-20 a), as discussed in [85]. In this approach, larger cell voltages draw more current, and therefore will naturally correct for any over voltage situations. However, one of the motivations for battery balancing is due to the actual manufacturing differences, i.e. internal impedances, present between cells and therefore this approach would have limited success in ensuring precise balanced voltages within a string [85].

A common approach, used in commercial and industrial battery balancing units, is the switched resistor configuration, as shown in Fig. 2-20 b) [86]. In this approach, a battery monitoring system individually controls each cell by a power electronic device,

and the cells are switched according to their differences across the string. This approach allows smaller resister values to control the battery voltages faster. However, for both resistive approaches, the downside is clearly that the energy is wasted in the balancing.

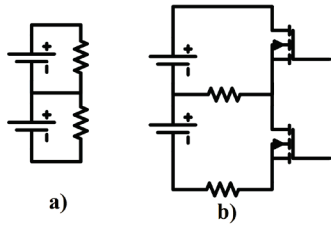


Fig. 2-20. Resistive balancing of serially connected battery cells a) resistor divider and b) switched resistor

2.4.2 Non-Dissipative - Capacitor Charge Shuttling

Whereas dissipative circuits burnt off excess energy to balance the batteries, non-dissipative circuits use the extra charge stored in those cells with the higher than average voltages, and put that charge into the cells with lower than average voltages. In this sense, the energy is not wasted in the balancing process, and instead can be used elsewhere.

Capacitor charge shuttling, as shown in Fig. 2-21, is an approach using purely capacitors to move charge along a series string of unbalanced batteries. There are two main reported configurations [87]: single tier, as shown in Fig. 2-21 a), and double tier, as shown in Fig. 2-21 b). In either configuration, the balancing occurs by switching in parallel, a capacitor that charges (limited by the lead or externally placed resistance) to the battery voltage. Once charged, this capacitor switches in parallel with another battery, and those charges equalize. This process is then repeated until the entire battery string is balanced.

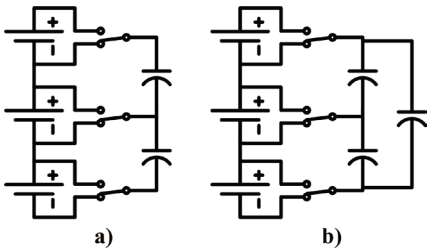


Fig. 2-21. Switched capacitor approach to balancing serially connected battery strings: a) single tier capacitors and b) double tiered capacitors

The charge shuttling technique is reportedly low in efficiency [87], and slow when balancing is required in large strings of batteries. In fact, the double-tier configuration [88], as shown in Fig. 2-21 b), is a direct attempt to improve the balancing speed of the circuit.

2.4.3 Non-Dissipative - Current Shunting

Instead of relying on the equalization time of capacitors to balance battery strings, another approach is to use the charging current to balance the string by diverting this current to lower cells as necessary [89]. This approach involves pulse-width modulating the switches, as pictured in Fig. 2-22, according to a battery management system, i.e. voltage feedback and knowledge of the battery chemistry is required.

This approach is motivated by reported research that indicates that lithium ion battery cells have the greatest potential for unbalance during the charge operation [85]. Therefore, a cost effective implementation is the unidirectional charge shunt circuit, shown in Fig. 2-22 a). Naturally, a bi-directional configuration of this circuit also exists, and this is shown in Fig. 2-22 b). However, the limitations of this circuit are that it involves two active devices per cell (bi-directional), increasing the potential for failure. Furthermore, compared to other converters which actively monitor the battery voltage, the balancing control can be complicated [86].

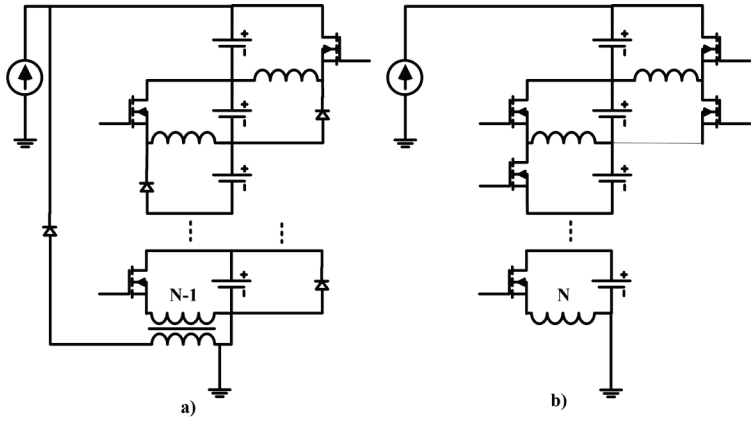


Fig. 2-22. Current shunting approach to balancing serially connected battery strings: a) unidirectional and b) bidirectional topologies

2.4.4 Non-Dissipative - Converter-based Balancing

Naturally, another common approach to battery balancing is by using various dc/dc converter topologies. Due to the scope of dc/dc converter topologies, only the general converter and a modular balancing circuit, that uses a similar approach to the ACIB in this thesis, are considered.

The simplest converter topology to use is the fly-back based topologies, as seen in Fig. 2-23. In these implementations, the total battery string can be used to excite a central transformer, and due to the fixed turns ratio on the secondaries of the transformer, balances each individual cell [85]. This approach is shown in Fig. 2-23 a), and requires

only a single active device, with no cell voltage monitoring required. On the other hand, the circuit of Fig. 2-23 a) is unable to balance in a bi-directional fashion - meaning that higher voltage cells simply do not receive charge and therefore, are not actively discharged. In this situation, if a battery cell were to become overcharged, this energy could not be used to charge a lower voltage battery cell – affecting the balancing speed.

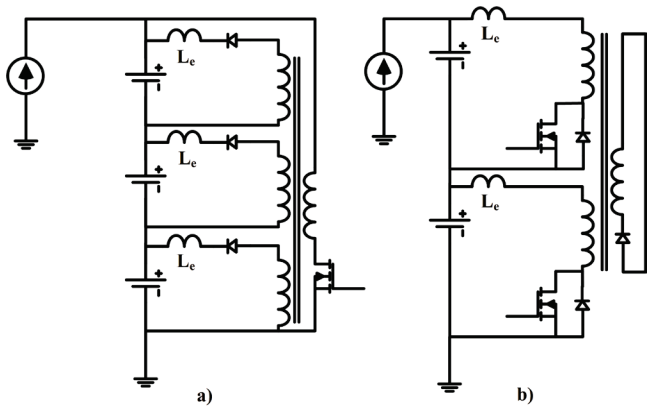


Fig. 2-23. Converter based balancing approach to serially connected battery strings: a) flyback based with single transformer and b) forward converter based with single transformer

The circuit in Fig. 2-23 b) is a forward converter version of the circuit in Fig. 2-23 a), as per [86]. Many other isolated topologies have been demonstrated, as per [86], with various differences in transformer configurations, balancing speed and active device count. However, the main limitation of the converter balancing circuits is the actual transformer used in the balancing operation. In modern electric vehicles, where battery strings can approach 100 series connected cells, an implementation of Fig. 2-23 a) or b) would require 100 secondary windings - an obvious impracticality.

Several circuits demonstrate methods to circumvent the multi-winding limitation of the converter-based circuits [86]. One approach is to place several transformers in series, [90], and have several identical transformers. However, while this remedies the transformer complexities, this configuration does not allow itself to be easily configured to different battery arrangements, e.g. one application with 96 cells against another application with 75 cells - a distinct disadvantage for a battery manufacturer.

Therefore, circuits have been demonstrated with a modular concept in mind, e.g. the four cell balancing circuit of Fig. 2-24 [91-93]. The goal behind these circuits is to have simple, high volume parts, but allow for simple adaptability to any number of battery cells. In Fig. 2-24, a flyback converter is used internally for 'intra-module' balancing, and an 'inter-module' transformer balances each module. Note the terminology used here is similar to the presentation of the ACIB based balancing circuit. A minimum

of three transformers, one pulse-width modulated switch and two solid state relays make up a balancing circuit for two battery cells. With any number of battery cells, the transformer turns ratio must be customized for the secondary 'intra-module' balancing. However, a central controller is still required for balancing the entire battery string, and the battery cells cannot be actively discharged in this approach.

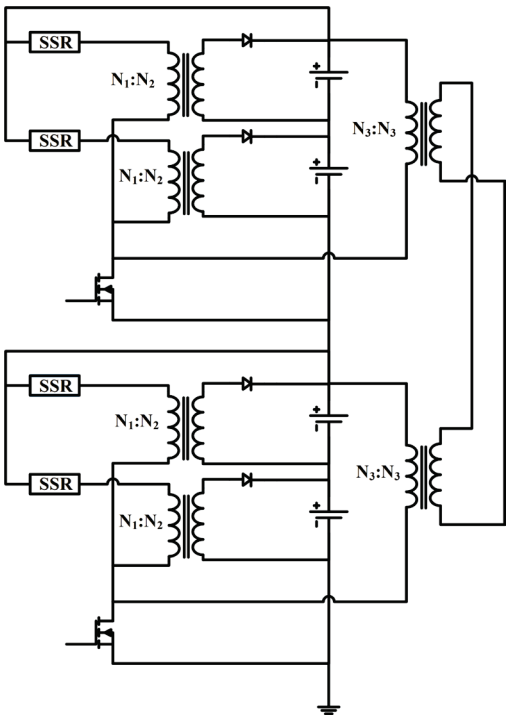


Fig. 2-24. Modular staged approach to battery balancing [94] showing converter topology for four batteries with two inter-module transformers and four intra-module transformers. SSR denotes solid-state relay.

2.5 Chapter Summary

Several topological approaches to low-voltage multi-level PWM converters were identified. One topology, three-phase parallel converters with interleaved switching, was highlighted as a common solution to increasing power levels when the device blocking voltage is not an issue. Several configurations based on the parallel converter approach were discussed, which are similar in operation to the ACIB based converters developed in this thesis. Additionally, since this thesis involves the presentation of a SVM approach for a five level coupled inductor converter (based on the ACIB), SVM is discussed in its two-level and multi-level form. Finally, as the ACIB is also presented as a balancing circuit in this thesis, a literature review of common balancing circuits was presented to provide context to the contributions of the proposed approach.

Chapter 3 – Asymmetric Coupled Inductor Bridge as a Three-Level Three-Phase Converter

In this chapter, the ACIB is employed in a three-level, three-phase dc/ac converter - motivated by the low cost aspect of having three output voltage levels per two active devices. As a three-phase dc/ac converter, the ACIB-based circuit is termed the 'six-switch coupled inductor converter' (SS-CIC), and as presented along with a parallel-based coupled inductor converter (CIC) for clarity of operation. A modulation scheme is presented to improve the power density of three-phase converters that use coupled inductors, by combining the three-phase coupled inductors into a single three-limb coupled inductor.

In more detail, the key points of this chapter are as follows:

- The operation and benefits of the SS-CIC is highlighted to familiarize key concepts in ACIB-based three-phase dc/ac converters.
- Three-limb coupled inductor operation using a carrier-based modulation approach. This approach is intended to highlight the challenges of developing a modulation scheme for three-limb coupled inductor operation for three-phase dc/ac coupled inductor converters.

3.1 Basic Operation of the Six-Switch Coupled Inductor Converter

The SS-CIC, and the parallel-based CIC are shown in Fig 3-1. Note the operation of the parallel-based CIC is given due to the familiarity of this converter thus far. This section details the switching states, interleaved switching, and simulation model for these two converters. Finally, the benefits of the SS-CIC are highlighted in terms of being a low-cost, three-level dc/ac converter.

3.1.1 Switching States within a Coupled Inductor Converter

Applying a voltage across a split-wound coupled inductor produces a mid-point voltage at the center-tap. Note however, the module current that flows, e.g. $i_{A,2}$ from Fig 3.1, for the SS-CIC is always defined as positive, in contrast to the parallel-based CIC. Therefore, a circulating winding current, i_{CW}, in the SS-CIC is the addition of the two module currents, (3.1), but in the parallel-based CIC, the circulating current is defined as the differential mode current, i_{DF}, and it is the difference between the two module currents, (3.2).

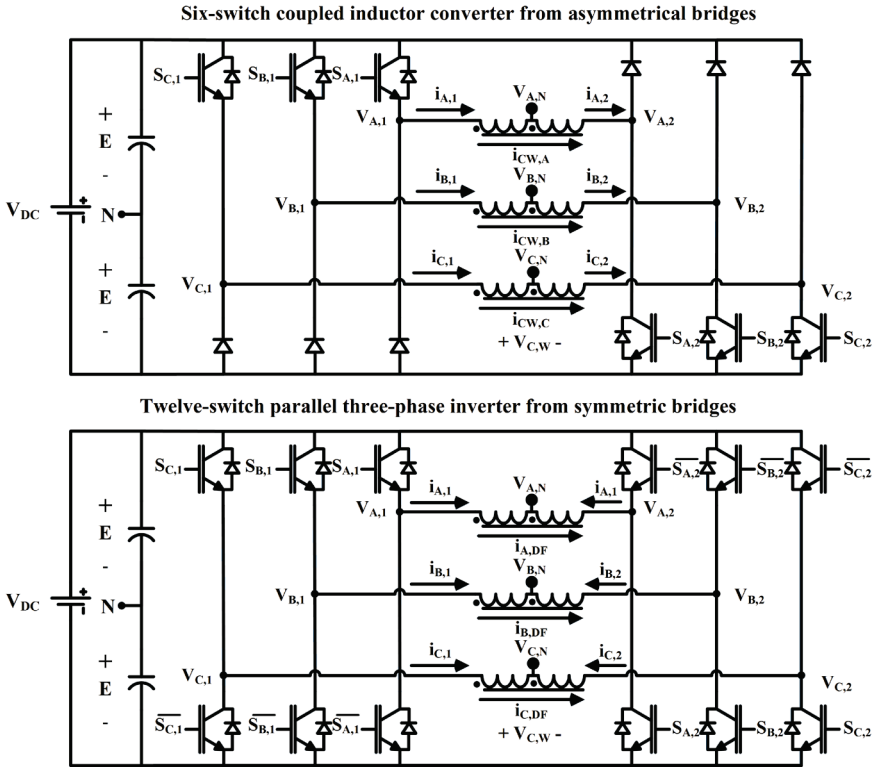


Fig. 3-1. The six-switch coupled inductor converter (SS-CIC) and the parallel-based CIC using coupled inductors with: module currents, e.g $i_{A,1}$, module voltage, e.g. $V_{A,1}$, winding voltage, e.g. $V_{A,W}$, phase output voltage, e.g. $V_{A,N}$ and circulating current, e.g. $i_{A,DF}$.

$$i_{CW,A} = (i_{A,1} + i_{A,2})/2 \ \text{(SS-CIC)} \tag{3.1}$$

$$i_{DF,A} = i_{A,1} - i_{A,2} \ \text{(Parallel-based CIC)} \tag{3.2}$$

Considering only a phase leg for each respective topology in Fig. 3-1, four switch combinations exist, $\{S_{A,1},S_{A,2}\}$ = {0,0}, {0,1}, {1,0} and {1,1}, where S is either 'on' (1) or 'off' (0). In addition, the remaining active devices within each phase leg of the parallel-based CIC are switched complimentary to avoid short circuit currents. These switching states are summarized in Fig. 3-2 a), for the SS-CIC and Fig. 3-2 b) for the parallel-based CIC, illustrating the output phase voltage and the polarity of the winding voltage with each combination. In Fig. 3-2, note that SS-CIC produces identical output voltages and winding voltages to the parallel-based CIC for each switching combination (or state).

3.1.2 Interleaved Modulation of Split-wound Coupled Inductor Converters

To produce the third voltage state, each phase reference is compared with two carriers, ideally at a phase angle difference of 180°, to minimized the size of the coupled inductor (i.e. the carriers are interleaved, see chapter 2). Assuming a sinusoidal reference

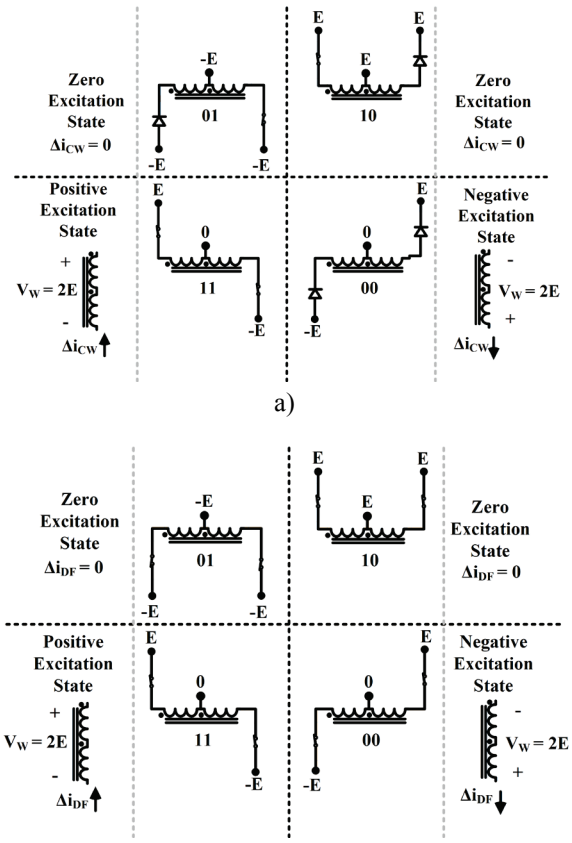


Fig. 3-2. Per phase switching states for a) SS-CIC and b) the parallel-based CIC according to state $\{S_{A,1}S_{A,2}\}$ as defined in Fig. 3-1

signal, the resulting logic signals for phase A are illustrated, i.e. $S_{A,1}$ and $S_{A,2}$, producing the phase output $V_{A,N}$ and the winding voltage $V_{A,W}$, in Fig. 3-3. Note in Fig. 3-3, the ratio between the switching frequency and fundamental frequency is intentionally low for illustrative purposes.

In Fig. 3-3, the output voltage in phase A, $V_{A,N}$, relative to 'N' in Fig. 3-1, has three voltage levels: 'E', '0', '-E', i.e. three-level PWM is achieved over the fundamental cycle. In the SS-CIC, the output voltages and winding voltages produced by sinusoidal modulation with interleaved carriers, i.e. Fig. 3-3, are identical, despite having twice as many active devices in the parallel-based CIC.

However, due to the diodes in each ACIB, the module currents of the SS-CIC are always positive, resulting in a dc offset seen in Fig. 3-4 a) compared to b). While this does increase the device current stress, note that the presence of this dc-offset in the circulating current is not necessary a negative feature of the SS-CIC. In fact, as mentioned in chapter 2, dc-offsets can exist in the circulating current of the parallel-based ICT as well. However, for the latter topology, complex current control is needed to insure

stable operation of the converter. In the SS-CIC, the asymmetric bridge in each phase causes a net negative dc offset in the winding voltage - keeping the circulating current stable without any need for closed loop control.

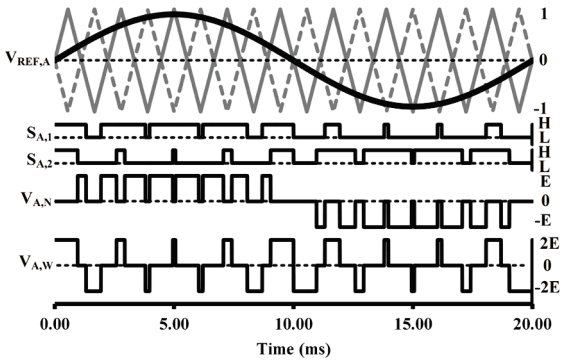


Fig. 3-3. Sinusoidal modulation with interleaved carriers for three-phase coupled inductor converters: gating signals for phase A, $S_{A,1}$ and $S_{A,2}$, output voltage for phase A (relative to N), $V_{A,N}$, and the winding voltage, $V_{A,W}$.

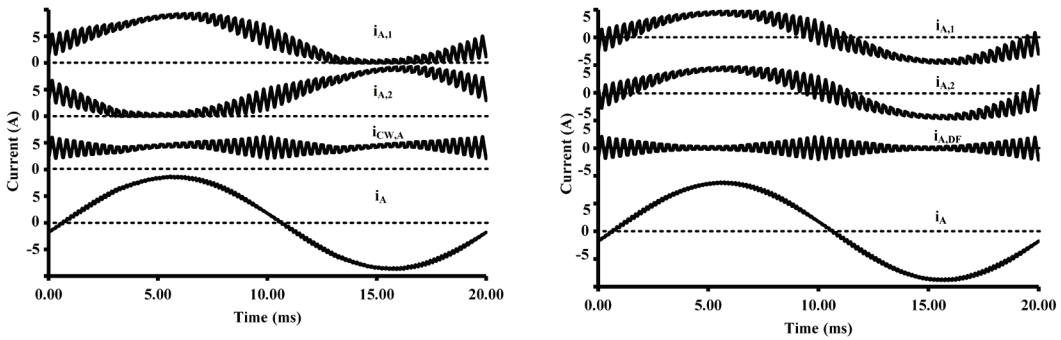


Fig. 3-4. Simulated module, circulating currents and phase currents for the a) SS-CIC and b) parallel-based CIC

3.1.3 Summary of SS-CIC Benefits

As a three-phase, three-level, dc/ac converter, the ACIB-based SS-CIC has several attractive benefits when compared to the parallel-based CIC. In the low voltage domain, at lower power levels, the cost of the converter is a significant issue. Therefore, while the SS-CIC has all the advantages of the parallel-based CIC in terms of output performance, several factors contribute to the SS-CIC potentially being more suitable as a low cost topology in the low-voltage domain, when compared to the parallel-based CIC:

- Half the number of active devices
- Half the number of required gate drivers and control signals

- No overlap protection of phase leg devices required (i.e. 'inter-lock' protection), and therefore each gate driver is reduced in complexity.
- Device voltage drops (and the device turn off time) contribute to a negative bias in the winding voltages, allowing for stable open-loop operation of the SS-CIC.

3.1.4 Simulation Models of Three-Level Coupled Inductor Converters

To aide in the development of the modulation techniques, the operation of either converter is separated into two models: the winding voltage model - which characterizes the high-frequency circulating current in each phase; and the ac output voltage model - which characterizes the ac output voltage of each converter.

A generic modulator, Fig. 3-5 a), produces the switching signals $S_{A,1}$, $S_{A,2}$, etc, resulting in the output voltage, $V_{A,N}$ ($V_{B,N}$ and $V_{C,N}$), and winding voltage $V_{A,W}$ ($V_{B,W}$ and $V_{C,W}$), as in (3.3) and (3.4) respectively.

$$V_{A,N} = \frac{V_{DC}}{2} \cdot (V_{A,1} + V_{A,2}) = E \cdot (S_{A,1} + S_{A,2} - 1) \quad \{0,1\} \in S_{A,1}, S_{A,2} \tag{3.3}$$

$$V_{A,W} = \frac{V_{DC}}{2} \cdot (V_{A,1} - V_{A,2}) = 2E \cdot (S_{A,1} - S_{A,2}) \quad \{0,1\} \in S_{A,1}, S_{A,2} \tag{3.4}$$

Therefore, a three-phase ac voltage, as per (3.3), composes the output mode of the converter, as per Fig. 3-5 c), and the winding voltages, as per (3.4), drive the three-phase circulating mode of the converter, as per Fig. 3-5 b). Note that for the circulating mode of the circuit, a coupling factor, e.g. $k_{W,AB}$, is shown - which is the coupling co-efficient between phases A and B. A zero coupling factor would mean each phase is independent from one another, i.e. phase A does not influence phase B.

In Fig. 3-5 b), the winding self-inductance, e.g. $L_{W,A}$, opposes the rate of change in the circulating currents, $i_{DF,A}$ or $i_{CW,A}$, only and is ideally independent of the phase current, i_A. Due to the tight coupling between the upper and lower windings, the total inductance in the circulating path of phase A is $4L_{W,A}$, as leakage can be ignored due to its relatively small per-unit size. Finally, in the output mode, as seen in Fig. 3-5 c), the leakage reactance of each winding can be included with the ac inductance, L_{AC}, or again ignored due to being small when compared to the ac load inductance.

3.2 Three Separate Single Phase and Combined Three-limb Coupled Inductors

Typically, for the parallel-based CIC, the three-phase coupled inductors are electrically separate, with no coupling between phases, as seen in Fig. 3-6 [52, 94]. As discussed in chapter 2, the coupled inductors can be integrated into a monolithic core

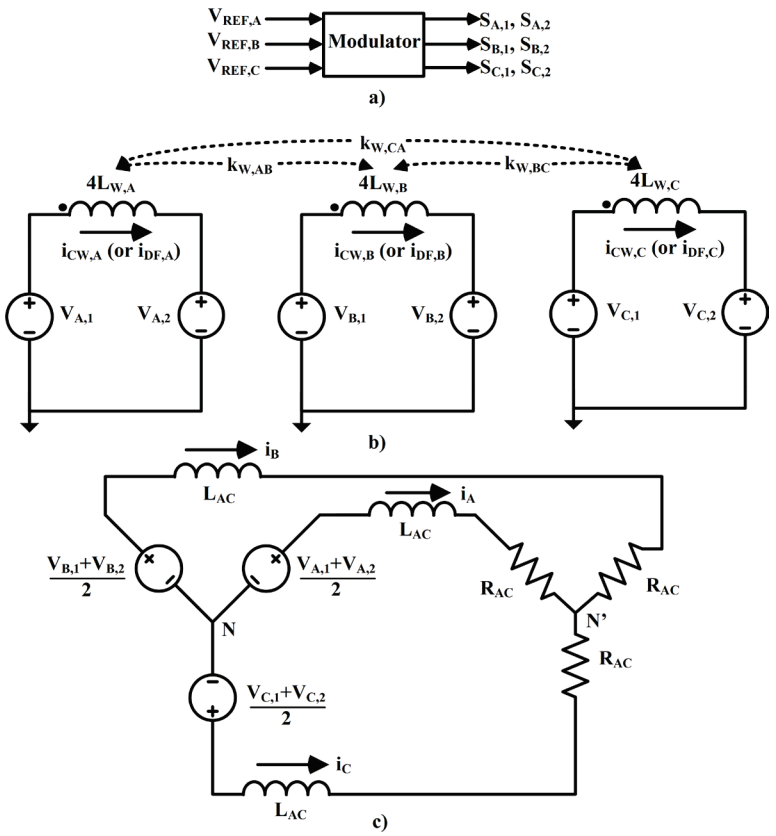


Fig. 3-5. Simulated coupled inductor converter model: a) generic modulator producing six gating signals $S_{A,1}$ to $S_{B,2}$,b) the circulating (or differential) mode and c) the ac output mode of the converter

but due to the difficulties in manufacturing these cores, this is not a common practice [51]. However, a three-limb core, as seen in Fig. 3.6, is commonly used in paralleled dc/dc converters [96], and three-phase commercial transformers. Therefore, in addition to the weight savings of using a three-limb coupled inductor, three-limb operation is also cost effective, due to their common use in industrial applications.

In addition, with a three-limb coupled inductor, the SS-CIC can operate without current control to ensure stable operation, and the dc current present in the circulating current no longer produces a large dc-flux in each coupled inductor. In Fig. 3-7 a), under dc excitation, the reluctance network for a three-limb coupled inductor is illustrated with three separate single-phase coupled inductors, Fig. 3-7 b). If the MMF in each phase were equal (i.e. equal dc currents), the dc flux is small, due to having to use the air paths (high reluctance, or low permeability) in the three-limb core to complete the magnetic circuit. Thus, operation with a three-limb core offers a significant advantage in terms of weight reduction for ACIB-based three-phase coupled inductor converters.

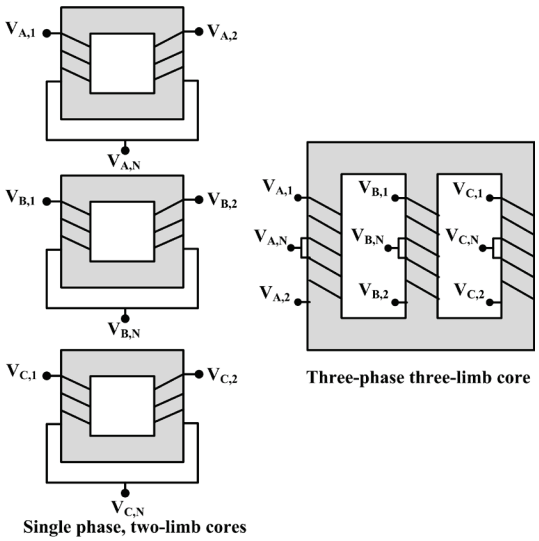


Fig. 3-6. Three separately wound single-phase cores (two-limb) on the left and a single three-phase three-limb core with three-phase windings on the right

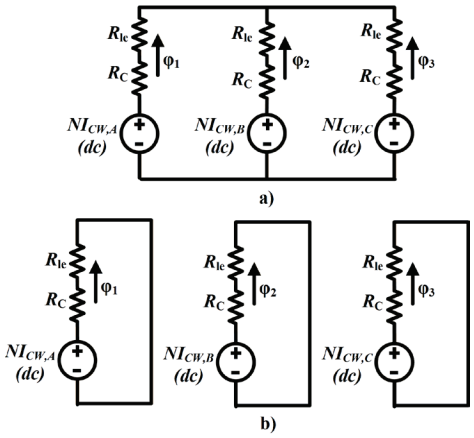


Fig. 3-7. Reluctance networks, under dc-current excitation, for a) three-limb coupled inductor core and b) three separate single-phase cores

To appreciate the approximate difference in size between the three-limb and three separate coupled inductors, consider the dimensions of the two core configurations in Fig. 3-8, under identical PWM voltage excitation, along with each phase winding having an identical number of turns, core permeability and lamination thickness. It is reasonable to assume that the dimensions H_2, H_3, W_2, and W_1 are similar between the two inductor designs, as these dimensions are dependent on the winding dimensions on each limb. Thus, the two inductors differ by the winding stack height – i.e. there are half the windings on each limb for the separate cores, reducing the winding height (H_1) by half.

Since the high frequency flux is voltage driven, the cross-sectional area is also identical for both core configurations in order to obtain the same high flux density magnitude in either core;

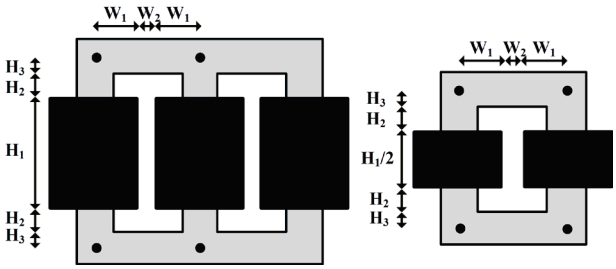


Fig. 3-8. Approximate geometric comparison of the three-limb coupled inductor and (three) single phase two-limb coupled inductors

hence, both configurations have the same iron loss density. Therefore, an expression for the approximate total volume of the iron for each core (three cores for the separate case) given in (3.5) and (3.6).

$$\mathrm{Vol}_{3L} \approx A_C \cdot [6 \cdot (H_2 + H_3) + 3 \cdot (H_1) + 4 \cdot (2W_1 + W_2)] \tag{3.5}$$

$$\mathrm{Vol}_{1L} \approx A_C \cdot [12 \cdot (H_2 + H_3) + 3 \cdot (H_1) + 6 \cdot (2W_1 + W_2)] \tag{3.6}$$

Using (3.5), consider a gap-less, three-limb core constructed from 'Thomas and Skinner' 7/8 three-phase, 6 mil laminations, wound for 12 mH total inductance with: H_1 = 5.1cm, $(2H_2 + 2H_3)$ = 3.9cm and $2W_1+W_2$=5cm. The equivalent separate inductors, from (3.8), would be 57% heavier. Therefore, under this approximate weight reduction, a coupled inductor converter with a three-limb coupled inductor, has 57% less iron weight than if it used three single-phase coupled inductors.

3.3 Challenges of Three-limb Coupled Inductor Operation

While integrating the three-phase coupled inductors into a three-limb coupled inductor saves weight, standard three-phase interleaved modulation, e.g. Fig. 3-3, is no longer applicable. This section identifies the presence of 'common mode winding voltages' in standard interleaved modulation techniques, and presents a simple modification scheme to illustrate the challenges in eliminating these common mode winding voltages. To reduce the complexity of the discussion, the terminology of the parallel-based converters is assumed (e.g. differential mode currents).

3.3.1 Common Mode Winding Voltages

With a parallel-based CIC, as in Fig. 3-1, if the output phase voltage of each inverter is defined as:

$$\text{Inverter 1: } (V_{A,1}, V_{B,1}, V_{,C,1}) \qquad \text{Inverter 2: } (V_{A,2}, V_{B,2}, V_{,C,2}) \tag{3.7}$$

Then a common-mode output voltage for each inverter can be defined as:

$$\text{Inverter 1:} \qquad V_{CM,1} = (V_{A,1} + V_{B,1} + V_{C,1})/3 \tag{3.8}$$

Inverter 2: $$V_{CM,2} = (V_{A,2} + V_{B,2} + V_{C,2})/3 \quad (3.9)$$

The voltage drop across the coupled inductor in each phase is then defined as:

$$V_{CM} = (V_{A,W} + V_{B,W} + V_{C,W})/3 = V_{CM,U} - V_{CM,L} \quad (3.10)$$

Therefore, the currents circulating between the set of three-phase inverters introduced by V_{CM}, is defined as representing a common code current, i_{CM}, flowing through the three-limb coupled inductor windings:

$$i_{CM} = (i_{A,DF} + i_{B,DF} + i_{C,DF})/3 \quad (3.11)$$

Alternatively, this means that, under the presence of a common mode winding voltage, the differential current, such as $i_{A,DF}$, has a common mode current component.

Consider the reluctance model of the three-limb and single phase coupled inductors, shown in Fig. 3-9, along with the winding voltage in each phase. Since V_{CM} is defined as the sum of the winding voltages across the three phases, it is clear that for the three-limb coupled inductor, Fig. 3-9 a), all three-limbs would then have a component of equal excitation under the presence of a common mode winding voltage. Since the sum of the fluxes at every point must equal zero, the flux produced by the common mode winding voltage must therefore not flow from phase to phase (through the high permeability iron), but instead through the low permeability air paths. However, in the case of the single-phase separate cores, see Fig. 3-9 b), each phase is independent to one another. Therefore, the presence of the common mode winding voltage would merely induce more flux in each limb in the iron (or high permeability) paths.

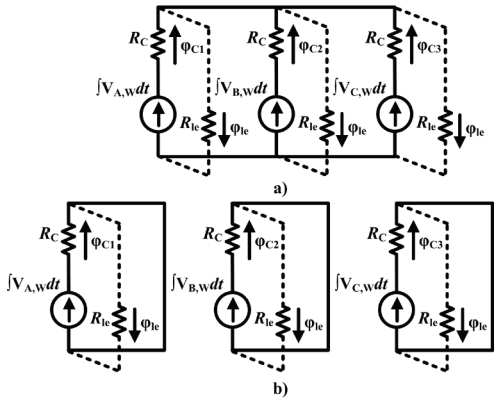


Fig. 3-9. High frequency flux (φ) paths for the a) three-limb coupled inductor core and b) the three separate single-phase cores

The process of high frequency flux leaving the core, through low permeability states, is better understood with the illustration of an interleaved discontinuous PWM scheme and its application to a three-limb coupled inductor. Consider the same interleaved carrier arrangement as Fig. 3-3, but with the three-phase modulating

references, as defined Fig. 3-10. This modulation reference is commonly called DPWM1, and is segmented in 60° sectors, as seen in Fig. 3-10 [77]. DPWM1 has only two phases active per 60° cycle, and in sector 0, these two phases are B and C.

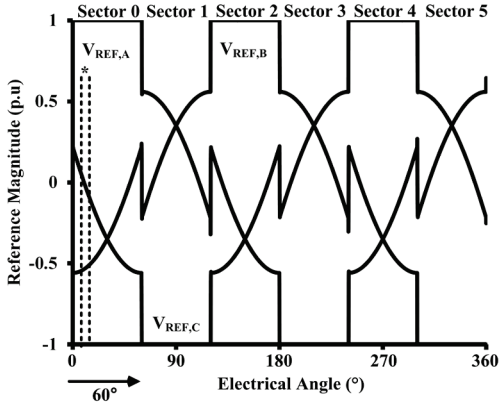


Fig. 3-10. DPWM1 three-phase references over a fundamental electric cycle at a modulation depth of 0.9/1.15, showing the switching period marked '*'.

Consider the excitation states of the parallel-based CIC under the period labelled '*' in Fig. 3-10, as shown in Fig. 3-11 a). Since the mid-level voltages depend on the magnetization of the three-phase coupled inductors, Fig. 3-11 b) illustrates the winding voltages over the same switching period marked '*'. As the three-phase winding voltages would nearly always be at the same polarity, an obvious improvement is to flip the winding voltage on phase C. Flipping the polarity of the winding voltage has no consequence on the output voltage, as per (3-3). Therefore, the resultant sum of the three-phase windings voltage is highlighted in grey along the V_{CM} axis of Fig. 3-11 b)

Fig. 3-11 c) illustrates the flux states within the three-limb core, during the switching states illustrated in Fig. 3-11 a) and b). Even by inverting the polarity of one of the winding voltages, only the switching states i) and v) maintain flux within the high permeability iron core. Otherwise, in states ii) and iv), the flux is driven outside the core, and returns through the three leakage paths (i.e. low permeability), completing the magnetic circuit. Given the self-inductance of the winding, as defined by (3.12) [97], the peak differential circulating current is high, as per (3.13), thereby significantly increasing the current stresses in each module, and reducing the converter efficiency.

$$L_W = \frac{N^2}{R}, R = \frac{l_M}{\mu A_C} \tag{3.12}$$

$$\hat{i}_{DF,A} = \frac{V_{DC}}{2L_W \cdot f_C} \tag{3.13}$$

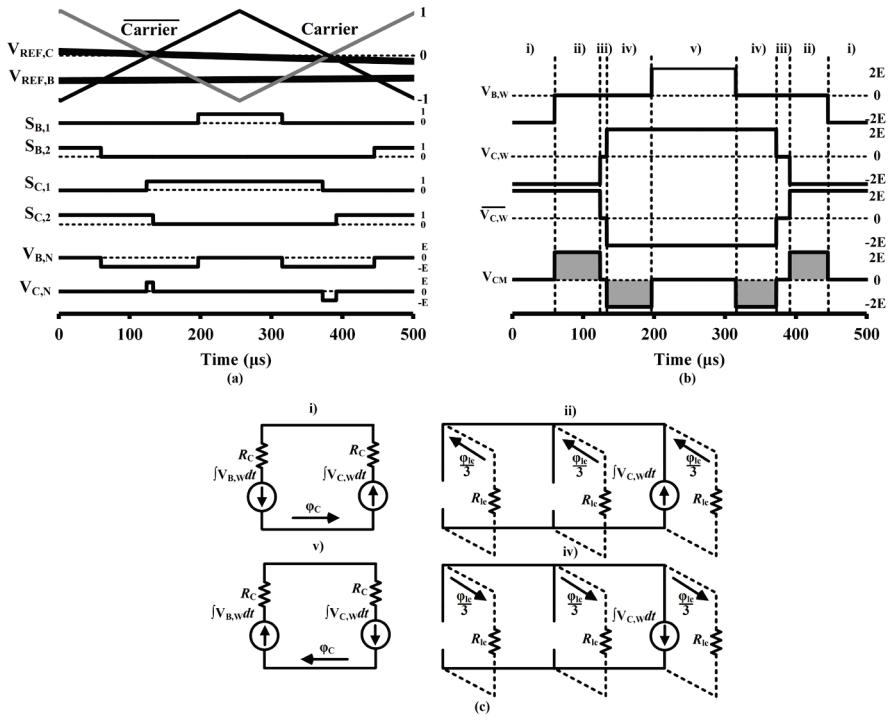


Fig. 3-11. The carrier cycle marked by '*' in Fig. 3-9 with a) the active switch gating signals and output voltages (relative to N) with A held inactive, b) the winding voltages and the inverted winding voltage for phase C producing the common mode voltage and c) the flux paths for the three-limb core produced. Note that states i) to iv) correspond to the winding voltages of b) and the flux paths identified in c). f_C = 2 kHz.

3.3.2 Modified DPWM1

The presence of common mode winding voltages in standard interleaved modulation techniques, e.g. DPWM1, limits the efficiency of the coupled inductor converter. This section describes a modification to DPWM1 to eliminate these winding voltages in coupled inductor converters. However, this scheme is mainly presented to highlight the challenges of three-limb coupled inductor operation, and therefore it is not intended to be an optimal solution.

Considering that the winding voltage, as described by (3.4), is only active when the mid-level voltage is needed, the approach to the modified DPWM1 starts with no coupled inductor switching. In the active phases, i.e. phases B and C in sector 0, see Fig. 3-10, an average reference signal can be created (V_σ) – representing output voltage states that do not involve coupled inductor excitation, as defined in (3.14). Those states that produce the 'mid-level' or '0' voltages at the output of the coupled inductor, involve the excitation of the coupled inductor, and can be defined as the differential voltage reference

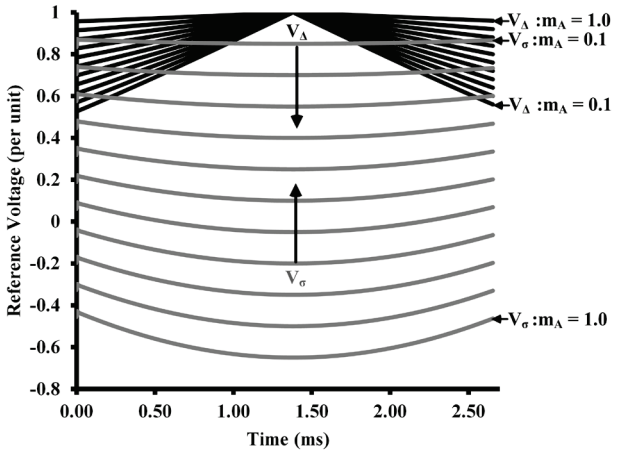


Fig. 3-12. Average (V_σ) and differential (V_Δ) phase references for sector 0 (Fig. 3-10), with increasing modulation depth from 0.1 to 1.0 in steps of 0.1. f_O = 60 Hz.

(V_Δ), as shown in (3.15). Over a 60° sector (at 60Hz, this is 2.667ms), the reference signals V_Δ and V_σ appear in Fig. 3-12 with an increasing modulation depth from 0.1 to 1.0. The low and high modulation depths of each reference signal are highlighted for clarity of operation.

$$V_\sigma = \frac{\left(V_{REF,B} + V_{REF,C}\right)}{2} \tag{3.14}$$

$$V_\Delta = 1 - \left\| \frac{V_{REF,C} - V_{REF,B}}{2} \right\| \tag{3.15}$$

By separating the reference signals in this manner - after a comparison with interleaved references - the resultant PWM represents pulses are those that excite the coupled inductor (S_Δ), and those pulses that do not (S_σ). Therefore, by altering the 'differential' pulses, the excitation periods of the coupled inductor can be modified. As altering these 'differential' pulses (S_Δ) would result in a change in the average output voltage over the switching cycle, 'average' pulses (S_σ) are added or subtracted to maintain this average. Using logic gates, e.g. from an FPGA, each differential pulse is modified such that an equal and opposite 'differential' pulse in the other active phase. Otherwise, the average pulses should pass to the gate of each switch. Essentially, this means that a switch should be high when 'the differential pulses are not active' and the 'average pulse is active' or when the 'differential pulses are active' and with a certain polarity. Using a digital logic approach, while still using sector 0 in the example, results in the expressions (3.16)-(3.19), or the diagram in Fig. 3-13. Note that the signal 'S_{POS}' represents the polarity of V_Δ, and is used to ensure opposing winding voltage polarity in the active phases, e.g. phases B and C for sector 0.

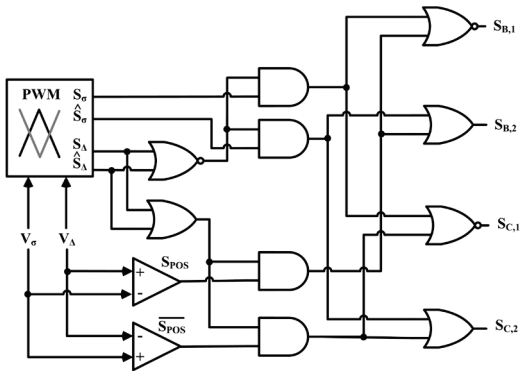


Fig. 3-13. Post modulation digital logic manipulation of the gating pulses to produce the actual gating pulses for the six-switch coupled inductor converter

$$\overline{S_{B,1}} = \overline{\left(S_\Delta + \hat{S}_\Delta\right)} \cdot S_\sigma + \left(S_\Delta + \hat{S}_\Delta\right) \cdot S_{POS} \tag{3.16}$$

$$S_{B,2} = \overline{\left(S_\Delta + \hat{S}_\Delta\right)} \cdot \hat{S}_\sigma + \left(S_\Delta + \hat{S}_\Delta\right) \cdot S_{POS} \tag{3.17}$$

$$\overline{S_{C,1}} = \overline{\left(S_\Delta + \hat{S}_\Delta\right)} \cdot S_\sigma + \left(S_\Delta + \hat{S}_\Delta\right) \cdot \overline{S_{POS}} \tag{3.18}$$

$$S_{C,2} = \overline{\left(S_\Delta + \hat{S}_\Delta\right)} \cdot \hat{S}_\sigma + \left(S_\Delta + \hat{S}_\Delta\right) \cdot \overline{S_{POS}} \tag{3.19}$$

The result of the differential/average approach, herein referred to as 'modified' DPWM1, is that in Fig. 3-14: illustrating the same carrier cycle and reference point '*' as in Fig. 3-11, but for the modified DPWM1 approach. As can be seen in Fig. 3-14, the common mode winding voltage is held at zero over the carrier cycle T_S, while the output voltages maintains three-level operation.

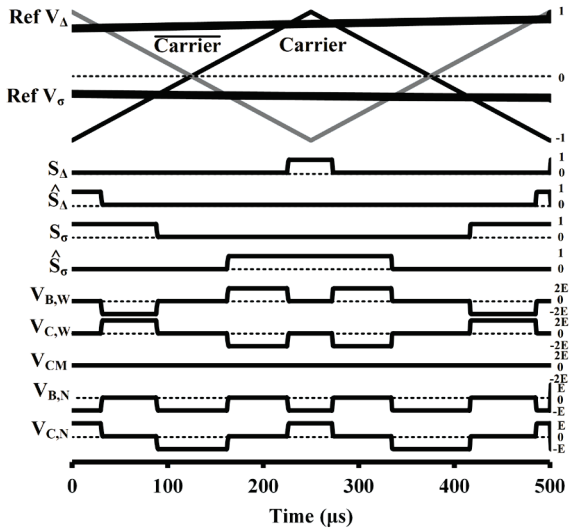
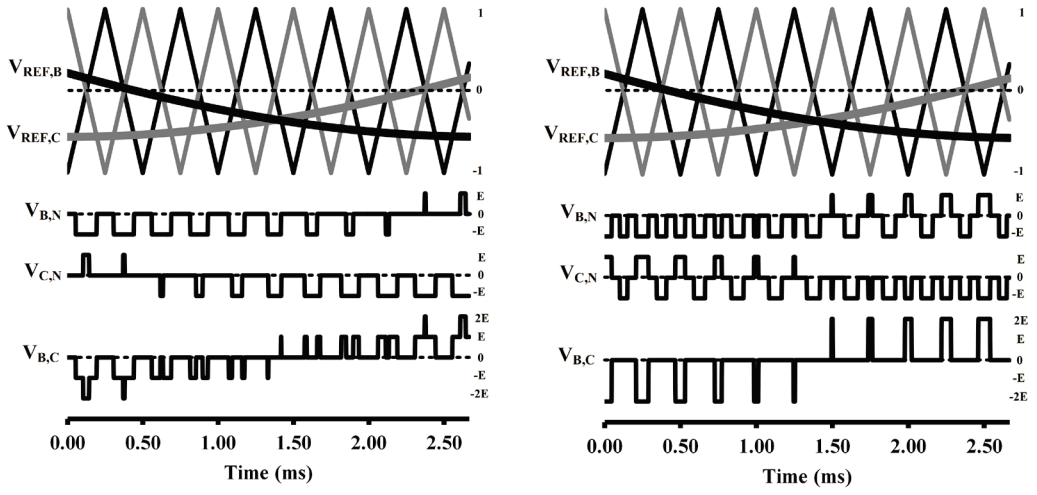


Fig. 3-14. At the reference point '*' of Fig. 3-10: gating signals produced by the average and differential reference signals, winding and corresponding common mode voltages, and output voltages (relative to N) for phases B and C. f_C = 2 kHz.

3.3.3 Consequences of Modifying DPWM1 for Common Mode Winding Voltage Elimination

The modification to interleaved DPWM1 eliminates the common mode winding voltages at every switching instant over a carrier cycle. However, as some differential pulses are eliminated in this process, the duration of the three-level voltage states is reduced, lowering the conversion quality. Furthermore, in order to keep the net average of the output the same over a switching cycle, the device switching frequency increases. This section discusses the consequences of the modified DPWM1 approach, but also demonstrates the significant benefit in terms of current stress reduction inherent to common mode winding voltage elimination (compensating the increase in device switching frequency).

In terms of the output voltage, Fig. 3-15 compares the modified DPWM1 approach to DPWM1, over sector 0, of Fig. 3-10. It is clear from Fig. 3-15 that the phase output voltage is three-level (i.e. E, 0, and -E) for each modulation approach. However, in this region, for the modified DPWM1, one of the line voltages (in this case, V_{BC}) is three-level (i.e. 2E, 0, -2E), as shown in Fig. 3-15 b), while the interleaved DPWM1 approach is five-level (i.e. 2E, E, 0, -E, -2E), as shown in Fig. 3-15 a). Although at this point in the modulation cycle, the remaining line voltage has full five-level operation, Fig. 3-15 b) highlights an important point: for common mode winding voltage elimination, the conversion quality can be impacted.



a) b)

Fig. 3-15. Sector '0' phase references (Fig. 3-10), output voltages and line voltage V_{BC} for: a) DPWM1 with interleaved carriers and b) modified DPWM1 with interleaved carriers. f_O = 60 Hz, f_C = 2 kHz.

In the modified DPWM1 approach, the average switching frequency of each active device must increase to maintain the same average output voltage as in DPWM1. As seen in Fig. 3-16, the switching signals for the active devices is shown during a switching period in sector 0 (in Fig. 3-10, where the phase A winding voltage is held inactive) and illustrates two 'high-low' transitions (this would be equivalent to turning on and of the device twice each carrier cycle). If one compares this to Fig. 3-11 a), the active device switching frequency doubles, and the switching losses could increase. Thus, there are two main challenges when eliminating the common mode winding voltages: increased device switching frequency, and decreased conversion quality.

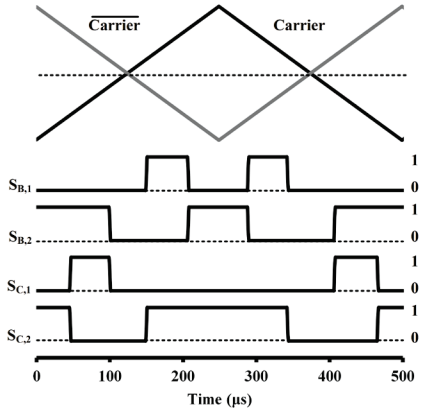


Fig. 3-16. Sector '0' (see Fig. 3-10) of the modified DPWM1 over a carrier cycle, T_S = 500 μs, illustrating the gate (or switching) signals

The main motivation to the modification of DPWM1 is to allow for three-limb coupled inductor operation - potentially allowing for a significant increase in compactness and converter weight. By eliminating the common mode winding currents, the device stresses should significantly decrease. Fig. 3-17 illustrates the differential current in phases B and C, for sector 0 in Fig. 3-10, using: DPWM1 and separately wound coupled inductors, shown in Fig. 3-17 a); modified DPWM1 with a three-limb three-phase coupled inductor, shown in Fig. 3-17 b); and DPWM1 with a three-limb three-phase coupled inductor, as shown in Fig. 3-17 c). Note that for each waveform in Fig. 3-17, the simulated magnetizing inductance is identical (L_W = 4 mH).

In the modified DPWM1 approach (using a three-limb core), the peak differential current is approximately half of that produced by DPWM1 using separately wound coupled inductors (3.5A versus 1.4A), as seen in Fig. 3-17 a) compared to Fig. 3-17 b). The frequency of the winding voltages in either of the two schemes is identical; however,

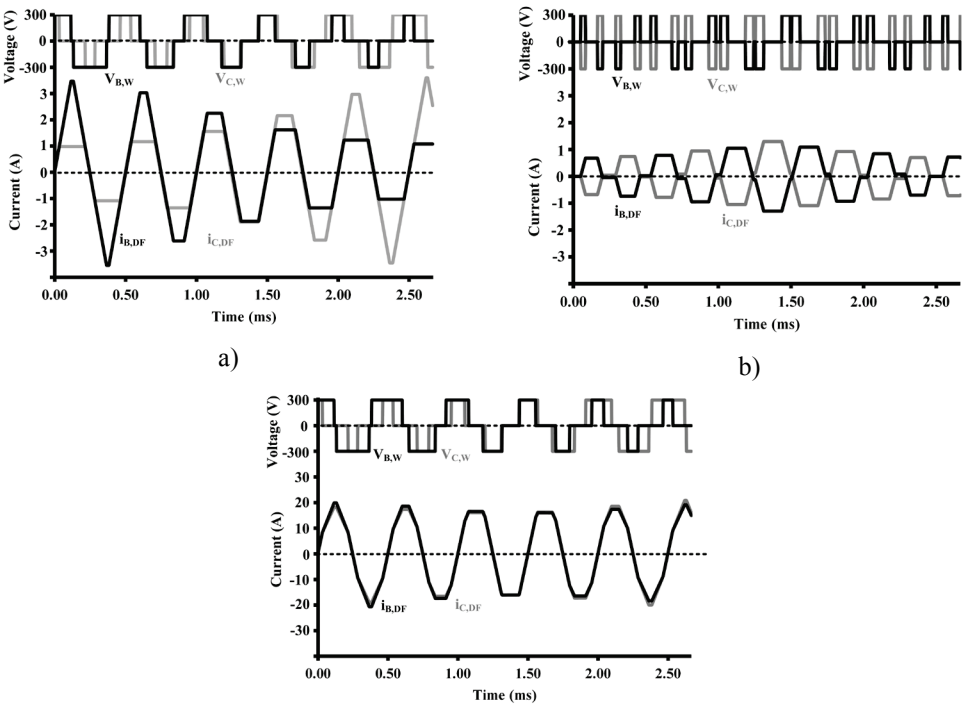
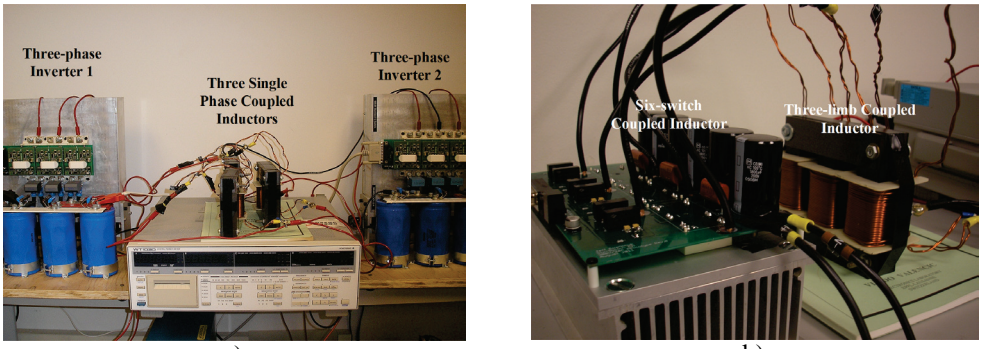


Fig. 3-17. Phase B and C winding voltages and differential currents for a) DPWM1 with interleaved carriers and three single-phase coupled inductors, b) modified DPWM1 and a single three-limb coupled inductor and c) DPWM1 with interleaved carriers and a single three-limb coupled inductor (note: L_W = 4 mH for all inductors)

due to the differential pulse reduction, the winding volt-seconds is reduced for the modified DPWM1 approach - resulting in lower peak differential currents. Illustrating the motivation for the proposed approach, in comparing Fig. 3-17 b) and Fig. 3-17 c), the differential current ripple has a peak magnitude of 19A under the standard DPWM1 scheme with a three-limb core, compared to that of 1.4A produced by the modified DPWM1 with the same core. It can also be observed from Fig. 3-17 c), that $i_{B,DF}$ and $i_{C,DF}$ are in phase with each other, and nearly identical - indicating a large common mode circulating current component, i_{CM}.

3.4 Experimental Setup

To confirm the conclusions made from simulation, two three-phase inverter testbeds were constructed to obtain the experimental results, as seen in Fig. 3-18. Dual six-switch parallel inverter modules, as seen in Fig. 3-18 a), and a SS-CIC, as seen in Fig. 3-18 b) are used to compare the two converter topologies, and present a more optimally designed SS-CIC respectively.



a) b)

Fig. 3-18. Experimental prototypes: a) parallel-based CIC with three single phase coupled inductors (60 kW six-switch modules) and b) SS-CIC prototype using commercial asymmetric half-bridge modules (20 kW)

The dual six-switch converter pictured in Fig. 3-18 a) uses SkiM306GD12E4 modules (300A, 1.2kV six-pack IGBT modules), driven by isolated gate drivers, also from SEMIKRON. A three-phase 5mH reactor and a three-phase delta connected resistive load are used with this converter configuration, giving a base power of 2.78kW, with V_{DC} = 300V at m_A = 1.15. A WT1030 power analyzer, from Yokogawa, is used for efficiency results on both modulation and core arrangements.

As the conversion efficiency of either modulation scheme is influenced by the switching behavior of the larger three-phase converter, a smaller 10 kW prototype, Fig. 3-18 b) is constructed to allow the experimental tests to be run closer to the rating of the equipment. This experimental prototype uses 600V, 50A IGBT modules (SK75GARL065W) from SEMIKRON, driven by a custom designed isolated gate driver system.

A LabView FPGA system, as shown in Fig. 3-19, generated the pulse-width modulation for either converter configuration. While the detail of the development of each LabView program exceeds the detail necessary for this chapter, the graphic nature of this program allows for easy reconstruction from discussion in this thesis. However, it is important to note that the 7851R FPGA provided the gating signals and the pulse-width modulation on a 40MHz clock (i.e. the PWM clock was 40 MHz) resolution.

In regards to the coupled inductors, 'Thomas and Skinner' 7/8 three-phase, 6-mil iron laminations are used to construct the three-limb core and wound to achieve a self-inductance of 12 mH (total dimensions: width 12cm, height: 11cm, depth: 3cm, weight: 3.5kg) [99]. The separate inductors are constructed by using a single winding on the center limb of the three-phase core. In either core configuration, the two windings are

split-wound in separate layers to reduce voltage stress on the insulation. Each coil has 36 effective series connected turns, wound in hand with two 15AWG wires.

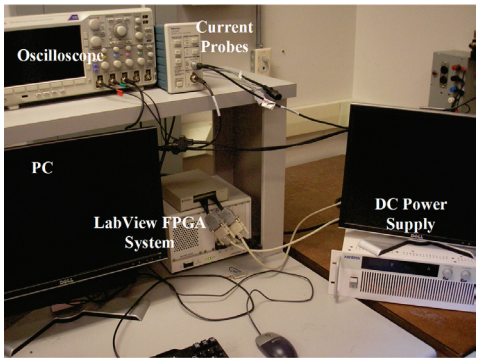


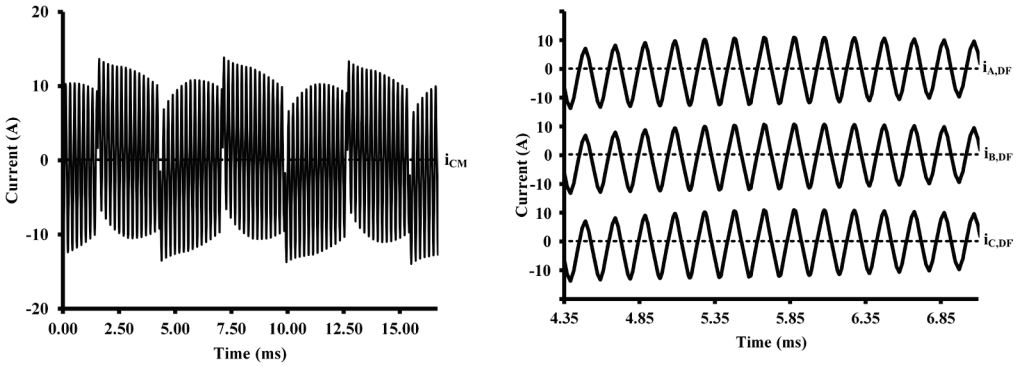
Fig. 3-19. Experimental LabView development system: pictured with oscilloscope, current probes, and 3 kW dc power supply

3.5 Experimental Results and Discussion

The experimental results are used to clarify the challenges that exist in three-limb operation for converters that use three-phase split-wound coupled inductors. It has been demonstrated that using the modified DPWM1 approach to eliminate the common mode winding voltages results in an increased device switching frequency and a decreased conversion quality. This section experimentally examines the benefits of the modified DPWM1 approach, and highlights the challenges that exist for an improved modulation scheme.

Using standard interleaved DPWM1 and a three-limb coupled inductor, Fig.3-20 highlights the impact of the common mode winding voltages on the high-frequency circulating currents in the CIC. In Fig. 3-20 b), it is clear that the differential current ripple across the three-phases is identical to one another, indicative of the presence of common mode current, as confirmed in Fig. 3-20 a). Since this common mode current ripple is only limited by the leakage reactance of the three-limb coupled inductor, the magnitude is large (10A peak), and comparable to the peak of the ac load current. Note that the 'jumps' present in the common mode current in Fig. 3-20 a), are a consequence of the symmetrical current paths present in the parallel-based CIC topology.

Furthermore, the impact of the common mode winding voltages is further examined by the experimental power conversion efficiency of the parallel-based converter under: interleaved DPWM1 with a three-limb core; interleaved DPWM1 with separate cores; and modified DPWM1 with a three-limb core, as shown in Fig. 3-21. It is



a) b)

Fig. 3-20. Experimental non-zero V_{CM}: a) common-mode currents over a fundamental cycle, and b) three-phase differential currents over a 60° period, under DPWM1. V_{DC} = 100V, m_A = 1.0, f_O = 60Hz, f_C = 5kHz, L_W = 4mH, L_{AC} = 5 mH, and R_{AC} = 42 Ω

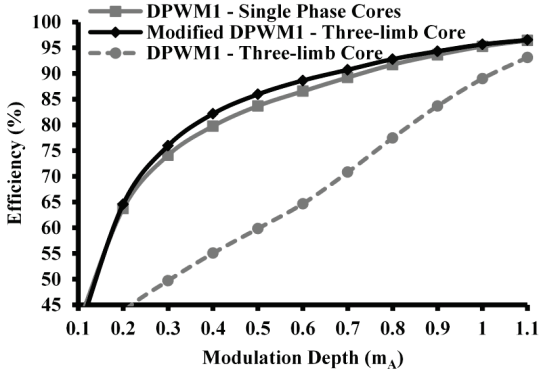
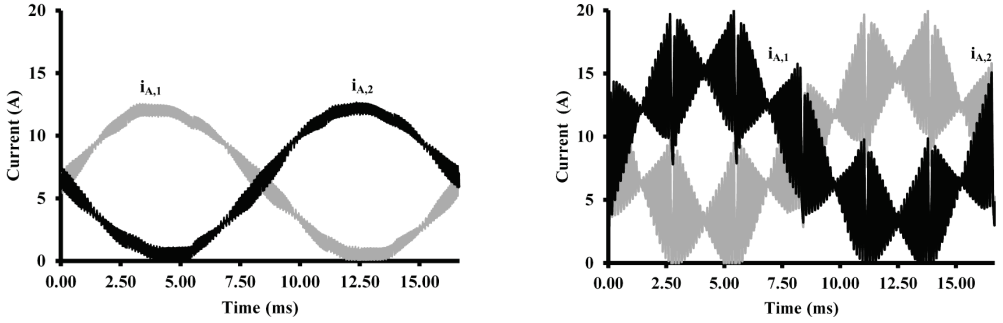


Fig. 3-21. Experimental three-phase power conversion efficiency (P_{OUT}/P_{IN}) for DPWM1 with interleaved carriers using three single-phase coupled inductors, modified DPWM1 and a three-limb coupled inductor and DPWM1 with interleaved carriers and a three-limb coupled inductor. V_{DC} = 300V, f_O = 60Hz, f_C = 5kHz, L_W = 4mH, L_{AC} = 5 mH, and R_{AC} = 42 Ω

clear from Fig. 3-21, that for efficient operation with a three-limb core, the common mode winding voltages must be eliminated.

Using the 10 kW SS-CIC prototype, as pictured in Fig. 3-18 b), the module currents produced under the modified DPWM1 scheme and the standard DPWM1 scheme (with flipped carrier excitation to limit the stress on the prototype unit) are shown in Fig. 3-22 a) and b). Comparing Fig 3-22 a) and b), the modified DPWM1 scheme lowers the peak module current from 20A to 13A. As a result, the conversion efficiency of the SS-CIC is improved throughout the modulation range, as confirmed in Fig. 3-23. Note that even with the increased device switching frequency, the lowered current stresses significantly improves the conversion efficiency, as the switching losses are approximately proportional to the device current and switching frequency in an IGBT.



a) b)

Fig. 3-22. Experimental module currents for the platform in Fig. 3-18 b), the SS-CIC, using a three-limb coupled inductor with a) modified DPWM1 and b) DPWM1 with interleaved carriers (flipped excitation). V_{DC} = 300V, m_A = 1.0, f_O = 60Hz, f_C = 5kHz, L_W = 4mH, L_{AC} = 5 mH, and R_{AC} = 42 Ω

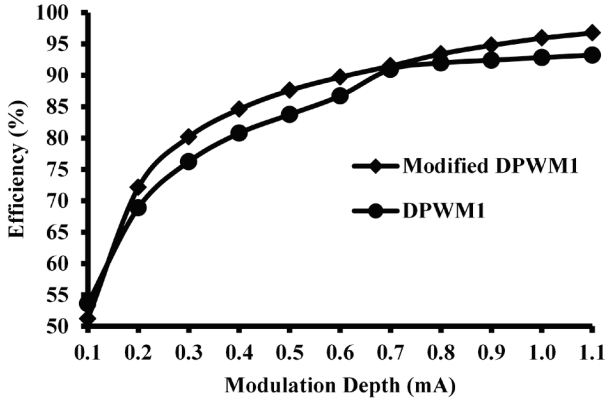
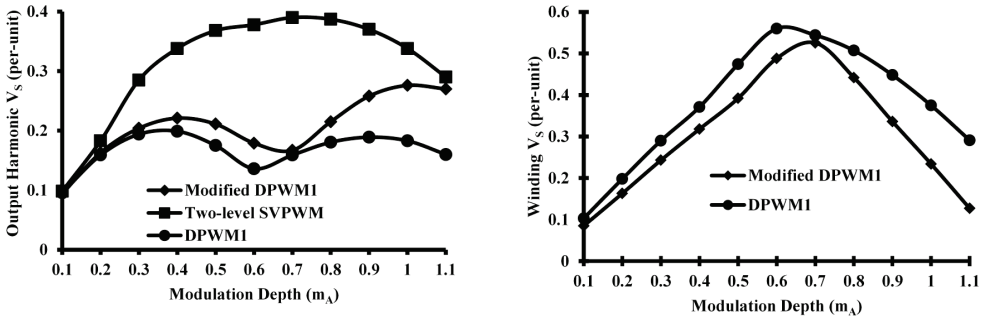


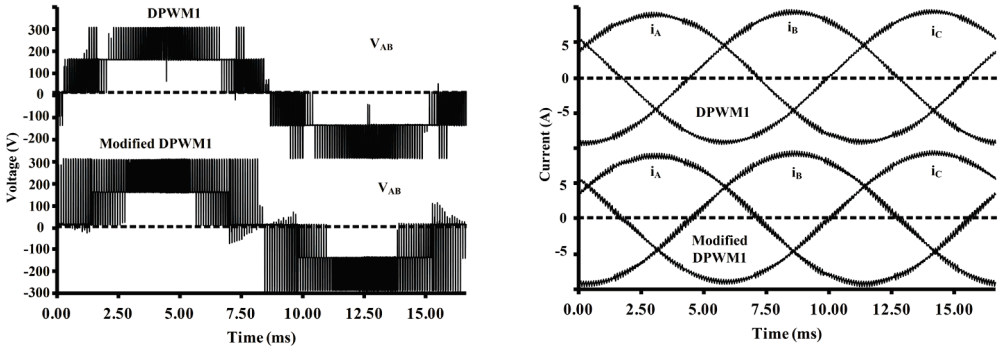
Fig. 3-23. Experimental conversion efficiency of the platform in Fig. 3-18 b), the SS-CIC, using a three-limb coupled inductor with a) modified DPWM1 and b) DPWM1 with interleaved carriers (flipped excitation).V_{DC} = 300V, f_O = 60Hz, f_C = 5kHz, L_W = 4mH, L_{AC} = 5 mH, and R_{AC} = 42 Ω

As previously mentioned, the consequence of the differential pulse modification is the reduction of mid-level voltage states in the CIC. Fig. 3-24 a) illustrates the two-level, SVPWM baseline harmonic volt-seconds, with modified and standard DPWM1 shown for comparison. While below the modulation depths of 0.8, the two three-level DPWM1 schemes are close to one another, it is clear that beyond this point, the modified DPWM1 approach becomes more two-level. Note that the use of harmonic volt-seconds is an approximate measure of the size of the ac load filter required for each modulation scheme and topology. Ergo, from the results of Fig. 3-24 a), to obtain the same conversion quality at the output of an ac filter, a converter using the modified DPWM1 would have to be larger. However, it is important to note that the use of a three-limb



a) b)

Fig. 3-24. Experimental volt-seconds (in per-unit) versus modulation depth for: a) output line voltage harmonics: modified DPWM1, two-level SVPWM, and DPWM1 with interleaved switching; b) winding voltages for modified DPWM1 and DPWM1 with interleaved switching. V_{DC} = 300V, f_O = 60Hz, f_C = 5kHz, L_W = 4mH, L_{AC} = 5 mH, and R_{AC} = 42 Ω



a) b)

Fig. 3-25. SS-CIC operation with a) Experimental line voltage, V_{AB}, and b) experimental phase currents with interleaved DPWM1 and modified DPWM1. V_{DC} = 300V, m_A = 0.9, f_O = 60Hz, f_C = 5kHz, L_W = 4mH, L_{AC} = 5 mH, and R_{AC} = 42 Ω

coupled inductor would not be feasible without eliminating the common mode winding voltages, and therefore, it is not entirely fair to suggest that ac filter should be larger.

The reduction of the differential pulses reduces the winding volt-seconds, as confirmed by Fig. 3-24 b). This result implies that despite the increase in device switching frequency with the modified DPWM1, the standard DPWM1 approach would also have to increase its switching frequency to match peak flux densities produced within a coupled inductor of similar design.

To validate converter operation, the line voltages, as shown in Fig. 3-25 a) and phase currents, as shown in Fig. 3-25 b), of the SS-CIC are illustrated under interleaved DPWM1 and modified DPWM1. As discussed in section 3.3, the line voltages under the modified DPWM1 approach has regions of 'three-level' characteristics, unlike the standard interleaved DPWM1 approach. However, due to the high per-unit ac load

inductance (12%, V_{BASE} = 208V, P_{BASE} = 2.78 kW), the differences in phase current ripple in Fig. 3-25 b) is relatively small. Finally, to verify performance as an electric drive system, the SS-CIC with a three-limb coupled inductor and modified DPWM1 is illustrated in Fig. 2-26, driving a 2HP, 1800 rpm induction machine.

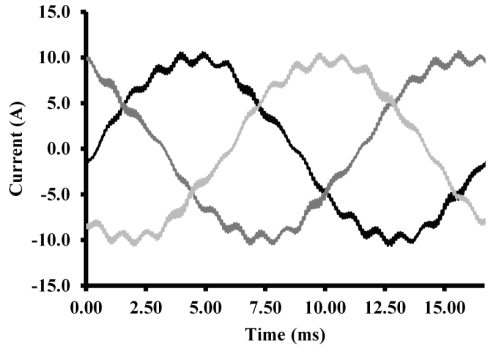


Fig. 3-26. Experimental three-phase motor currents for the SS-CIC under the modified DPWM1 scheme and a three-limb coupled inductor. V_{DC} = 300V, m_A = 1.0, f_O = 60Hz, f_C = 5kHz, L_W = 4 mH, P_{OUT} = 2HP, and n_S = 1800 rpm.

3.5 Chapter Summary

This chapter presented the ACIB as a three-phase, three-level converter system, termed the six-switch coupled inductor converter. The operation of the SS-CIC is explained and highlighted against the parallel-based CIC, and is found to achieve the same output performance with half the number of active devices. Furthermore, due to the module currents always being positive, an inherent negative dc winding voltage exists to keep the circulating currents stable in the SS-CIC. Due to these points, the ACIB when used as a three-phase dc/ac converter has advantages over the parallel-based converter in terms of cost and operational complexity.

To increase the power density, three limb coupled inductor operation for coupled inductor converters is proposed. However, the common mode winding voltages that exist in traditional interleaved modulation schemes limit the conversion efficiency of the coupled inductor converters when a three-limb coupled inductor is used. A simple modification to DPWM1 is examined with the goal of highlighting the challenges in eliminating the common mode winding voltages. It is found that simple alignment of the coupled inductor winding voltage states can increase the device switching frequency, and impact the conversion quality. Therefore, when considering a modulation approach to eliminating these common mode winding voltage states, a new form of converter analysis is required, i.e. space vector modeling of the converter.

Chapter 4 - Asymmetric Coupled Inductor Bridge as a Five-level Three-phase Converter

In this chapter, a neutral point clamped (NPC) configuration of the ACIB is presented as a five-level dc/ac converter, as seen in Fig. 4-1. A space vector approach is used to analyse the operation of the converter to select switching states that minimize the device switching frequency and the impact on conversion quality, when operated with a three-limb coupled inductor. The space vector approach is justified due to the complexity of the five-level dc/ac converter over the SS-CIC, and from the limitations identified for the DPWM1 modified approach for three-limb coupled inductor operation.

The ACIB-based NPC topology has the same number of output voltage levels as a standard 24-switch NPC converter, with the same number of devices as the three-level NPC converter. Therefore, due to the five-level output, the neutral point clamped coupled inductor converter (NPC-CIC) can potentially eliminate the filter used in certain applications, such as high-speed electric machines, with a cost effective device count. Thus, the main contributions of this chapter are as follows:

- The operation of the five-level NPC-CIC is described.
- A space vector approach to common mode winding voltage elimination is presented for the NPC-CIC to enable three-limb coupled inductor operation.

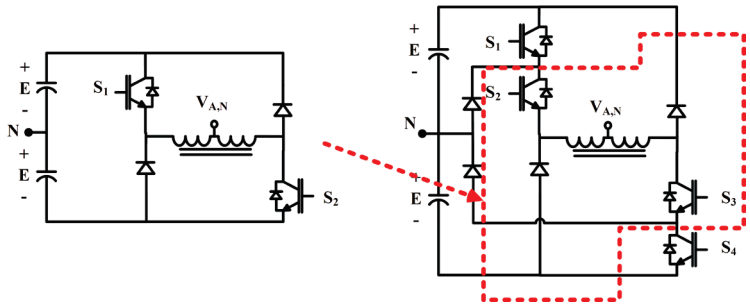


Fig. 4-1 - ACIB configuration: a three-phase neutral point clamped coupled inductor converter

Specifically, a basic description of the operation of the NPC-CIC, as shown in Fig. 4-2, and its switching states are given. A brief discussion on the weight reduction of the three-limb coupled inductor mass for the NPC-CIC is given, along with the simulation model used for the NPC-CIC. The modulation of the NPC-CIC is discussed and the impact of the common mode winding voltage is examined specifically for this converter. A space vector based approach is then presented to minimize the impact on device switching frequency and conversion quality when eliminating the common mode

winding voltages. An experimental prototype validates the modulation approach and confirms high conversion efficiency while using a three-limb coupled inductor.

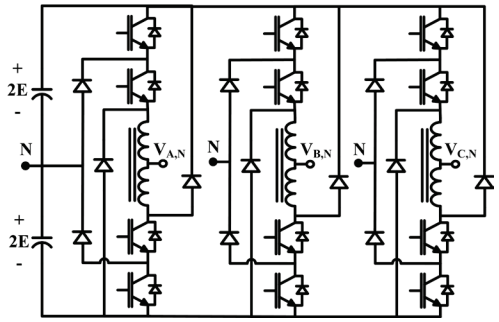


Fig. 4-2. The three-phase neutral point clamped coupled inductor converter (NPC-CIC)

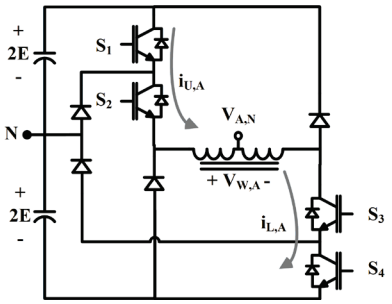


Fig. 4-3. Phase A of the NPC-CIC with the switches (S_N), upper and lower winding currents ($i_{U,A}$ and $i_{L,A}$), output voltage ($V_{A,N}$) and winding voltage ($V_{W,A}$) defined

4.1 The Five-Level Neutral Point Clamped Coupled Inductor Converter

By embedding the ACIB within the neutral point clamped converter structure, as seen in Fig. 4-2, the NPC-CIC is created. Note that the phase output voltage, for a single input dc voltage of V_{DC} has five-levels ('4E') as compared with the three-levels of the standard NPC converter ('2E'). This section details the switching states of the NPC-CIC, the coupled inductor mass reduction compared to the SS-CIC, and the simulation model used for an arbitrary modulator.

4.1.1 Switching States of the NPC-CIC

Fig. 4-3 identifies the switch, current and voltage notation for the NPC-CIC, with phase A used as an example. The four-switch phase leg of the NPC-CIC produces sixteen switching states, as seen in Fig. 4-4. Within the sixteen switch state combinations, eleven result in either positive or negative excitation of the coupled inductor. Furthermore, due to the split-capacitor configuration, switching states exist that excite the coupled inductor with either '2E' or '4E' (alternatively, half input dc voltage or the full dc voltage across the

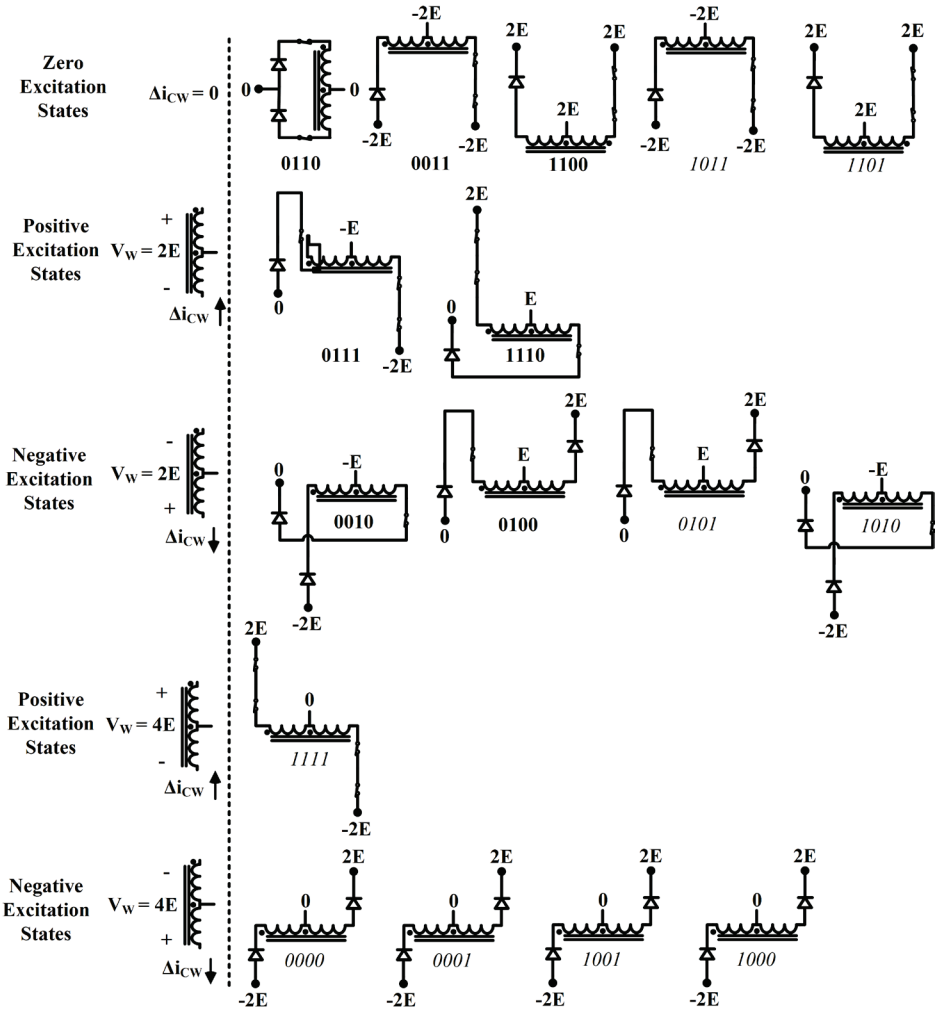


Fig. 4-4. The sixteen switching states of phase A in the NPC-CIC, with each switching state defined using the switching logic to control the on and off states as per $\{S_1S_2S_3S_4\}$, of Fig 4-3. Non-useful switching states are noted in italics.

coupled inductor of each phase). Considering these switching states, Fig. 4-4 illustrates all sixteen switching states with their respective output and winding voltages.

Upon examination of Fig. 4-4, a general expression for the output voltage and the winding voltage is expressed in (4.1) and (4.2) respectively. Note that 'S_N' refers to the switch number, as defined in Fig. 4-3, and the 'over-bar' refers to the negated logic state of that switch. Switch 'on' is defined as 'H' or '1', and switch off is defined as ' L' or '0'.

$$V_{A,N} = E \cdot (S_2 \cdot (1 + S_1) - S_3(1 + S_4)) \quad \{0,1\} \in S_N \tag{4.1}$$

$$V_{W,A} = E \cdot (S_4 + S_3 - \overline{S_2} - \overline{S_1} - S_2\overline{S_1} - S_3\overline{S_4}) \quad \{0,1\} \in S_N \tag{4.2}$$

While sixteen total switching states exist within the NPC-CIC phase leg, not every state is practical to include within a modulation scheme. Consider the output voltage, $V_{A,N}$, as defined in (4.1), in regards to the individual switching states. If the switches S_2 and S_3 are in a logic '0' state, then switches S_1 and S_4 have no influence on the

output voltage; therefore, the switching combinations $\{S_1S_2S_3S_4\}$ = {1101}, {1011}, {0101} or {1010} are redundant as they increase the number of devices that are active, without altering the output voltage of the converter. Furthermore, as one of the motivations for considering the NPC configuration is the reduction of dc voltage across the coupled inductors (thereby decreasing the size of the inductors), the switching states: $\{S_1S_2S_3S_4\}$ = {1111}, {0001}, {1001}, {1000} and {0000} can also be eliminated - reducing the number of useful switching states to seven.

As in Chapter 3 for the SS-CIC, the circulating winding current (common to each winding), $i_{CW,A}$, is defined in (4.3), according to the positive current direction of the module currents, $i_{U,A}$ and $i_{L,A}$, depicted in Fig. 4-3. Similarly, (4.4) defines the ac output current, relative to the positive module current definitions, as per Fig. 4-3.

$$i_{CW,A} = \frac{i_{U,A} + i_{L,A}}{2} \tag{4.3}$$

$$i_A = i_{U,A} - i_{L,A} \tag{4.4}$$

4.1.2 Weight Reduction of the Coupled Inductor with the NPC Topology

In addition to the increased number of voltage levels over the SS-CIC, the NPC configuration can potentially reduce the weight and losses of the three-limb coupled inductor. Note that for this claim to hold true, the switching states used within the NPC-CIC must not include those with '4E' or '-4E' magnetization, as discussed in Section 4.1.1. By eliminating these states, the three-phase coupled inductors are exposed to half the voltage stress when compared to the SS-CIC (or the parallel-based converter).

To provide some context into the size reduction when using a three-limb coupled inductor for the NPC-CIC versus the SS-CIC, spreadsheet designs were created in Table 4-1 a) and b), to compare the approximate losses and weight for 460V ($650V_{DC}$) and 208V ($280V_{DC}$) designs. These spreadsheets assume square wave switching (i.e. the worst case winding voltage scenario), with fixed copper and iron fill factors between the designs. To simplify the design process, two three-limb core configurations (E-E and E-I) were selected, and the iron loss density is approximated (at 400 Hz) by using (4.5) - obtained from the lamination manufacturer's datasheet (for 6-mil laminations) [98]. In brief, for a fixed three-limb core lamination thickness, but with a range of geometric sizes (height and width), each power rating, in Table 4-1, was iteratively matched to a cross-sectional area, and kept below an 80°C temperature rise (in the iron).

$$P_{loss} = k_1 f_c B_{ac}^b + k_2 (f_c B_{ac})^{1.5} + k_3 (f_c B_{ac})^2 \quad W/lb \tag{4.5}$$

b, k_1, k_2, k_3 are constants derived from core loss characteristics, f_C = switching frequency (15 kHz). B_{ac} = high frequency peak ac flux density and b = 2.7628, k_1 = 5.6972, k_2 = 9.9054, k_3 = 0.5298, factors from [98]

Core Geo.	E-I				E-E			
kVA	**10**	**20**	**40**	**60**	**10**	**20**	**40**	**60**
SS-CIC								
Fe Wt.	7.2	20.8	46.4	95.1	5.7	12.2	23.7	41.0
Cu Wt.	5.8	9.6	18.7	27.0	4.7	9.1	17.8	27.5
Tot. Wt.	**13.1**	**30.5**	**65.4**	**122**	**10.4**	**21.3**	**41.7**	**68.5**
Fe Loss	64.6	92.4	114.1	101.0	94.9	125.0	164.0	125.0
Cu Loss	45.8	76.0	147.6	300.1	37.0	71.4	140.2	305.1
Tot Loss	**110.0**	**168.3**	**261.6**	**400.7**	**131.9**	**196.8**	**304.2**	**430.6**
NPC-CIC								
Fe Wt.	4.1	7.4	20.8	38.1	2.5	5.7	9.3	23.7
Cu Wt.	2.7	5.7	9.6	17.2	2.5	4.6	10.1	9.8
Tot. Wt.	**6.9**	**13.2**	**30.5**	**55.4**	**5.0**	**10.3**	**19.4**	**33.6**
Fe Loss	52.8	64.5	92.4	55.7	73.2	97.7	120.5	164.0
Cu Loss	21.1	45.2	76.0	191.0	20.0	36.3	79.7	109.3
Tot Loss	**74.0**	**109.7**	**168.3**	**246.8**	**93.2**	**134.0**	**200.2**	**273.3**

a)

Core Geo.	E-I				E-E			
kVA	**10**	**15**	**20**	**25**	**10**	**15**	**20**	**25**
SS-CIC								
Fe Wt.	6.8	17.1	19.2	28.7	5.7	9.1	9.1	12.1
Cu Wt.	5.4	6.2	9.3	9.8	3.9	5.8	9.1	12.2
Tot. Wt.	**12.3**	**23.2**	**28.4**	**38.2**	**9.7**	**14.7**	**18.0**	**24.1**
Fe Loss	55.8	92.5	74.5	99.9	93.7	130.7	104.5	84.9
Cu Loss	52.1	53.7	90.9	103.6	37.9	49.5	88.9	129.6
Tot Loss	**108.0**	**146.2**	**165.4**	**203.5**	**131.6**	**180.3**	**193.3**	**214.6**
NPC-CIC								
Fe Wt.	4.1	7.2	9.4	16.6	2.9	6.3	5.9	6.4
Cu Wt.	2.3	3.5	4.8	4.6	1.4	2.7	3.9	5.1
Tot. Wt.	**6.5**	**10.6**	**14.0**	**21.1**	**4.3**	**8.9**	**9.7**	**11.4**
Fe Loss	49.6	65.0	58.0	86.5	33.0	98.4	90.7	83.6
Cu Loss	22.4	29.7	46.6	48.8	53.2	23.5	38.3	54.5
Tot Loss	**72.0**	**94.8**	**104.6**	**135.3**	**86.2**	**122.0**	**129.0**	**138.1**

b)

Table 4-1. Three-limb coupled inductor losses (in W) and weight (in lbs) for the six-switch CIC and the NPC-CIC for a) 208V designs and b) 480V designs

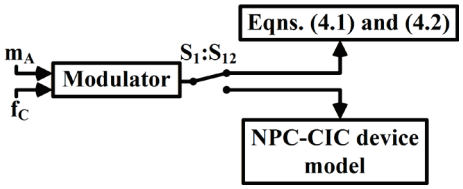


Fig. 4-5. Two simulator modes used for realization of the modulation schemes developed. A switch between the behavioral model and the actual device model used to reduce simulation time in the development procedure.

The approximate designs from Table 4-1 show that the weight of the three-limb coupled inductor, at the same power level, in the NPC-CIC is approximately half of that required in the SS-CIC. Therefore, while having the same number of active devices as the standard three-level NPC converter, the NPC-CIC requires a smaller three-limb coupled inductor as compared to the SS-CIC, with the same number of voltage levels as a 24-switch NPC converter. Thus, this converter is ideal for filter-less operation of certain applications, such as the flywheel battery system described in chapter 1.

4.1.3 Simulation Model for the NPC-CIC

A MATLAB-based simulation was used to verify the modulation schemes in this chapter. This section details the model of the NPC-CIC used outside the modulator.

Two simulation models, at a fixed switching frequency, f_C, producing twelve gating signals are employed with an arbitrary modulator: a behavioral model based on (4.1) and (4.2), and the actual device model, as shown in Fig. 4-5. The motivation behind the behavioral model is to reduce simulation time for modulation development. However, to verify stable operation (due to the presence of the split capacitors), and analyze the reduction in circulating winding current ripple, the active device model is also used.

Fig. 4-6 illustrates the twelve-switch device model, which employs ideal switching devices to shorten the compilation time. Fig. 4-7 a) and b) illustrate the three-phase, three-limb coupled inductor model as a six winding coupled inductor, with the mutual coupling co-efficient matrix (scaled by L_W) defined in Fig. 4-7 c). Within this mutual coupling co-efficient matrix, the two inter-limb windings, i.e. winding 1 and 2 from Fig. 4-7 b), have near ideal coupling, while the limb-to-limb (i.e. winding 1 to 3) coupling has a co-efficient of 0.425 (ideal is 0.5). The limb-to-limb mutual coupling of 0.425 is justified based on experimental measurements of the three-limb coupled inductor. Note that for this simulation model, a discrete solver is used with a variable time step (maximum time step is limited to 1e-6).

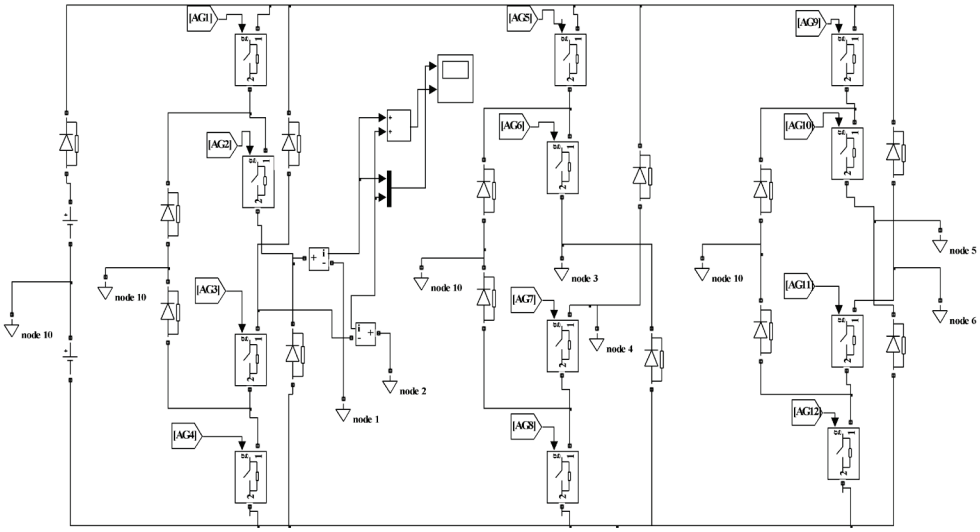
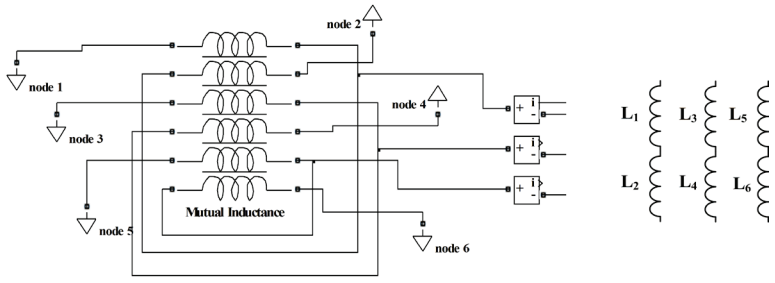


Fig. 4-6. The MATLAB/SIMULINK twelve-switch NPC-CIC device model (three-limb coupled inductor shown in Fig. 4-7).



$$\begin{bmatrix} K_1 & K_{12} & K_{13} & K_{14} & K_{15} & K_{16} \\ K_{21} & K_2 & K_{23} & K_{24} & K_{25} & K_{26} \\ K_{31} & K_{32} & K_3 & K_{34} & K_{35} & K_{36} \\ K_{41} & K_{42} & K_{43} & K_4 & K_{45} & K_{46} \\ K_{51} & K_{52} & K_{53} & K_{54} & K_5 & K_{56} \\ K_{61} & K_{62} & K_{63} & K_{64} & K_{65} & K_6 \end{bmatrix} \cdot L_W = \begin{bmatrix} 0.99 & -0.99 & -0.425 & -0.425 & -0.425 & -0.425 \\ -0.99 & -0.99 & -0.425 & -0.425 & -0.425 & -0.425 \\ -0.425 & -0.425 & 0.99 & -0.99 & -0.425 & -0.425 \\ -0.425 & -0.425 & -0.99 & 0.99 & -0.425 & -0.425 \\ -0.425 & -0.425 & -0.425 & -0.425 & 0.99 & -0.99 \\ -0.425 & -0.425 & -0.425 & -0.425 & -0.99 & 0.99 \end{bmatrix} \cdot L_W$$

c)

Fig. 4-7. The three-limb, three-phase coupled inductor model used in the device simulation mode with a) six-winding coupled inductor, b) electrical equivalent model and c) mutual coupling co-efficient (M_{XY}) of winding X to winding Y matrix with winding inductance L_W.

4.2 Interleaved Pulse-Width Modulation of the NPC-CIC

While Chapter 2 introduced several carrier-based multi-level modulation schemes, this section addresses the basic adaptation of three-level interleaved modulation for five-level, NPC-CIC operation. In addition, an interleaved DPWM1 scheme for the NPC-CIC is introduced, which reduces (but does not eliminate) the common mode winding voltages for high-switching frequency operation. The goal of this section is to

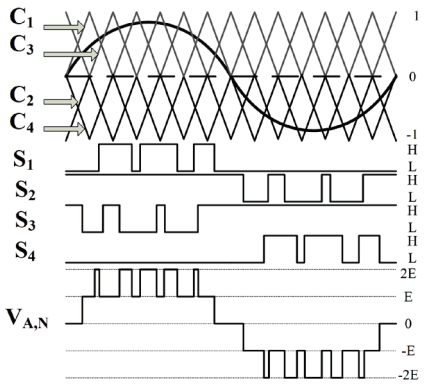


Fig. 4-8. Sinusoidal PWM, with interleaved switching based on three-level PD modulation, for the NPC-CIC with switching states and output phase voltage, $V_{A,N}$, shown.

discuss interleaved pulse-width modulation for the NPC-CIC to appreciate the space vector-based approach to common mode winding voltage elimination.

Two additional carriers are introduced to the three-level PD modulation approach, at an interleaved angle of 180°, to produce four carriers: two carriers in the upper band, and two carriers in the lower band, as shown in Fig. 4-8. Note here that switches S_1 and S_3 form an interleaved pair, while the switches S_2 and S_4 form another interleaving pair. Fig. 4-8 illustrates five output voltage levels as produced from a sinusoidal reference and a low switching to fundamental frequency ratio. However, like the three-level coupled inductor converter, for three-limb operation, co-ordination between the three phases is necessary to enable efficient operation.

4.2.1 'Flipped Carrier' DPWM with Interleaving Carriers

Consider the DPWM1 pattern, with interleaving carriers in Fig. 4-9, and recall that the winding voltage, as per (4.2), can produce the same output voltage state, as per (4.1), regardless of the excitation. A simple modification to DPWM1 is to 'flip' or invert the switch logic for one phase, reversing the winding excitation voltage for that same phase. Consequently, a flux return path is created in the three-limb core, reducing the common mode winding voltages, as described in [99]. Since the output voltages are unaffected, the conversion quality also remains unaffected at all modulation depths. Note this modulation approach is also described in Chapter 3 for the three-level coupled inductor converters.

By employing a discontinuous modulation approach, only two phases are active for a given 60° segment (or sector, as per Fig. 4-9) - leading to the three-phase coupled inductor being energized by only two-phases at any given instant. By inverting the

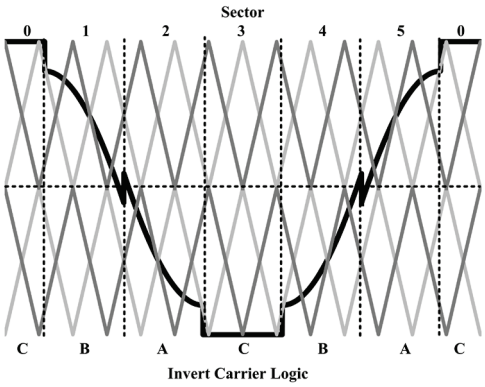


Fig. 4-9. DPWM1 with interleaved carriers over a fundamental cycle, with the 'invert carrier logic' sectors defined.

switching logic for a given phase, the net result is demonstrated in Fig. 4-10, where the winding voltages produced by the 'flipped carrier' DPWM1 approach is examined over a carrier cycle, where T_S = 333 μs. In Fig. 4-10, the inverted winding voltage for one phase causes the common mode winding voltage to sum to zero at some instances - i.e. $V_{W,A} + V_{W,B}+V_{W,C} = 0$. However, the highlighted grey sections of Fig. 4-10 illustrate the non-zero common mode winding voltage, which drives high-frequency flux outside the three-limb core. Over the carrier cycle depicted in Fig. 4-10, Fig. 4-11 identifies the corresponding high frequency flux paths within the three-limb coupled inductor.

Specifically, to emphasize how the common mode winding voltage states influence the converter efficiency for the NPC-CIC (as opposed to the SS-CIC addressed in Chapter 3), consider Fig. 4-11. The high-frequency flux paths in the three-limb core are highlighted in this figure, and for winding voltage combinations '1)' and '5)', the flux produced by the winding voltages across coils 'B' and 'C' is driven through the iron core, linking the two phases. However, for the switching states '2)' and '4)', only phase B is active, resulting in the flux produced by coil 'B' to be driven outside the core - and therefore returning through the 'leakage' paths shown in Fig. 4-11. At low switching frequencies, e.g. 3 kHz, (which might be required at higher power levels) the amount of circulating current ripple caused from this modulation approach, would cause excessive heating in the semiconductors and potentially the windings themselves.

Compared to the SS-CIC, the NPC-CIC has more switching states that produce no excitation of the coupled inductor, as seen in Fig. 4-4. Therefore, the duration of the non-zero common mode winding voltage states is generally smaller, as shown in Fig. 4-10. However, as the percent duration, relative to the switching period, is fixed and the circulating current ripple produced by the non-zero states is only limited by the leakage

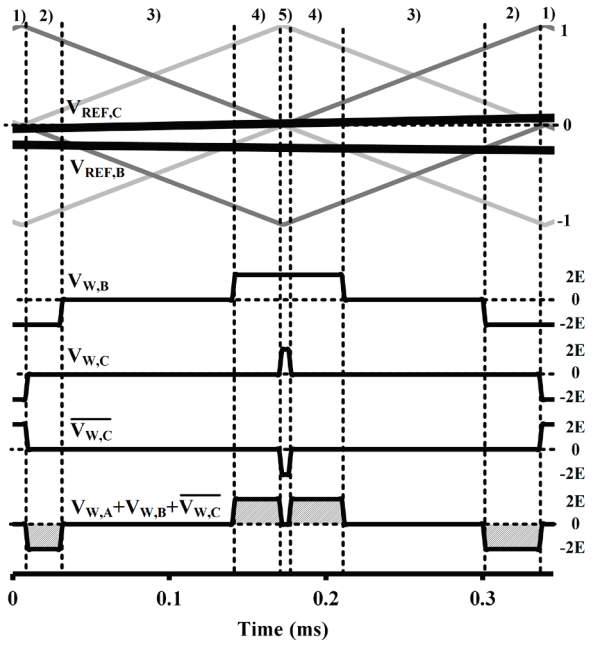


Fig. 4-10. 'Flipped carrier' DPWM1 in sector 0 of Fig. 4-9, with the winding voltages of each phase illustrated (with $V_{W,A} = 0$) where phase C has inverted switch logic, resulting in the winding voltage $V_{W,C}$. $f_C = 3$ kHz.

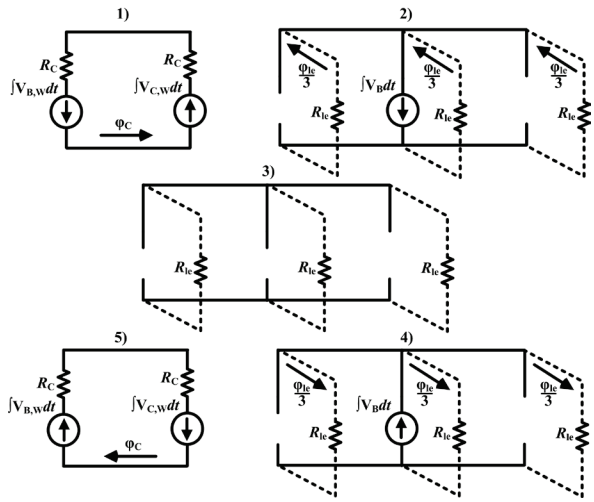


Fig. 4-11. Three-limb, three-phase coupled inductor excitation states for the NPC-CIC produced over the switching cycle highlighted in Fig. 4-10.

reactance of the coupled inductor, a relatively high switching frequency is required for efficient operation. Therefore, for a relatively low output power and high switching frequency, the 'flipped carrier' DPWM1 approach can employ a three-phase, three-limb coupled inductor with relatively high conversion efficiencies, as shown in [99].

To enable efficient conversion at a greater range of power levels (and therefore operation without a lower bound on the switching frequency) a scheme must therefore

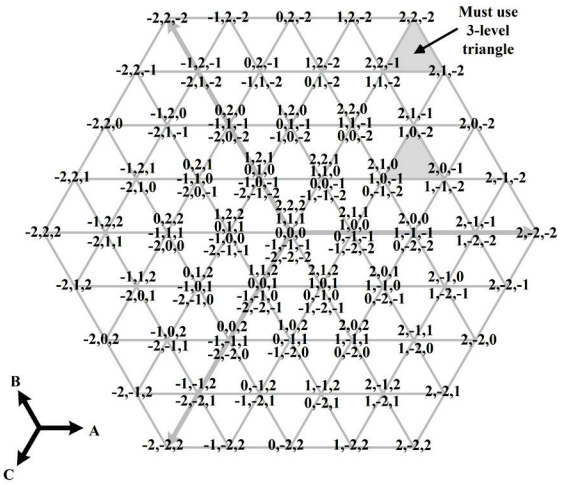


Fig. 4-12. Two-dimensional voltage output states produced by the NPC-CIC inverter considering all possible switching states.

eliminate the common mode winding voltages completely, as done in Chapter 3 for the three-level coupled inductor converters.

4.3 Elimination of the Common-mode Winding Voltages in the NPC-CIC

This section details the development of the space vector based approach to common mode winding voltage elimination. The common mode voltage states are described using space vector based analysis, and a modulation approach is detailed using well-known rules for minimizing the switching frequency and output voltage distortion. The development of this modulation approach is detailed using a MATLAB simulation and the limitations of this approach are identified.

While the number of output voltage states for the NPC-CIC increased by two over the SS-CIC, the number of possible switch combinations increases exponentially with the NPC topology. As an example, with four switches per-phase leg in the NPC-CIC, and with all possible switch combinations used, the three-phase converter has 4096 combinations, compared to 64 in the SS-CIC. Furthermore, using (4.2), each switching state can map into the complex output voltage, V_{OUT}, as per (4.6).

$$V_{OUT} = V_{A,N} + V_{B,N} \cdot e^{-j\frac{2\pi}{3}} + V_{C,N} \cdot e^{-j\frac{4\pi}{3}} \tag{4.6}$$

Considering (4.6), the NPC-CIC produces 61 unique voltage output states, compared to 18 generated by the SS-CIC, resulting in the two-dimensional space vector map in Fig. 4-12. As there are only 61 unique output vectors from 4096 switching combinations, there are a significant number of 'redundant' voltage output vectors, and these can be obtained by multiple switching states. Therefore, with the

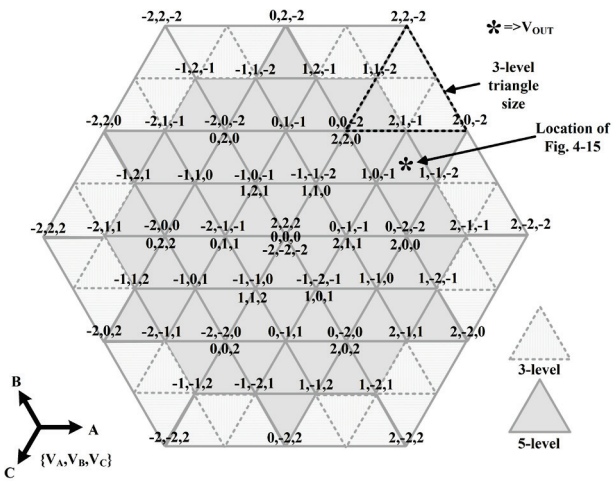


Fig. 4-13. Reduced space vector map after the application of the constraint in (4.7), on the output voltage states of the NPC-CIC

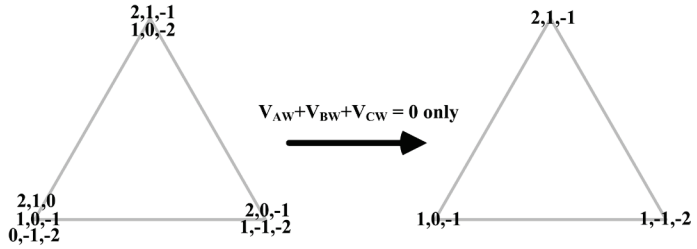


Fig. 4-14. The effect of redundant output voltage states from the constraint in (4.7), on the triangle highlighted in Fig. 4-12

consequences of the modified DPWM1 approach in mind, and the number of redundant vectors available, a space vector based approach can be used to optimize the modulation of the NPC-CIC.

The first step in the space vector approach is to eliminate each vector combination where the sum of the winding voltages, as per (4.7), is not zero. In other words, for each output vector state, the winding voltage can be determined via (4.2), and that switching combination/output vector state is eliminated if it does not satisfy (4.7). With the remaining vectors, and using (4.6), the two-dimensional output states create the space vector map of Fig. 4-13, in the same manner as Fig. 4-12.

$$V_{W,CM} = V_{W,A} + V_{W,B} + V_{W,C} = 0 \tag{4.7}$$

The net result of the constraint of (4.7) has two consequences:

- The number of redundant output voltage states is reduced
- Certain triangles are no longer bounded by any output vectors

Specifically, to appreciate the consequence of (4.7), Fig. 4-14 illustrates the reduction of the redundant output voltage states with the bounding triangle highlighted in Fig. 4-12. One can see that only the voltage vectors: {2,1,-1}, {1,0,-1} and {1,-1,-2} can

possibly satisfy (4.7), and therefore are the only bounding vectors remaining in that triangle. In each case, the bounding vectors of the triangle include **only** those vectors in which the common mode winding voltages sum to zero. Thus, the number of high-frequency flux paths in the three-limb coupled inductor is reduced to one, with each limb having opposing excitation to keep the flux within the iron core.

While the elimination of certain redundant output voltage states will have a net consequence on the average device switching frequency (but not necessarily double, as per the modified DPWM1 approach), the output vectors that have been eliminated, i.e. those vectors in Fig. 4-13, have a consequence on the modulation for the NPC-CIC. In this space vector based approach, the triangles that are bounded by eliminated vectors must use 'three-level' vectors, as shown in Fig. 4-13. As an example, for the triangle bounded by {2,2,-2}, {1,1,-2} and {2,1,-2} (as shown in Fig. 4-12), the vector state {2,1,-2} does not satisfy (4.7), and therefore is eliminated, as per Fig. 4-13. When the reference voltage is located in this triangle, the vectors used for switching must then be {2,2,-2}, {2,2,0} and {2,0,-2}, i.e. the typical three-level bounding triangle. This results in the phase voltage having a mixed 3/5-level characteristic at modulation depths beyond 0.75.

4.3.1 A Complete Picture of the Space Vector Approach to Common mode Winding Voltage Elimination in the NPC-CIC

One of the conditions for space vector modulation is that the modulator must synthesize the reference voltage based on the 'nearest three' vectors, i.e. the bounding triangles on the space vector map. Let the triangles of Fig. 4-13 that have a side length of 'E' be termed the 'five-level' triangles, and the triangles that have a side length of '2E' be termed the 'three-level' triangles. With traditional ‘center-aligned’ space vector modulation approach [79], a synthesized output voltage, V_{OUT}, in Fig. 4-13 would switch from {1,0,-1} to {1,-1,-2} to {2,1,-2} to {1,0-1}, with the reversed sequence in the next half carrier cycle, $T_S/2$. The latter vectors would be identical to the space vector switching pattern of ‘V_0-V_1-V_2-V_3-V_3-V_2-V_1-V_0’ as described in [79], but with {1,0,-1} being both V_0 and V_3 – the zero state vectors.

However, since there are two possible winding configurations for each output state (which involve coupled inductor excitation), there must also be co-ordination amongst the winding voltages within the inverter. Recall that the average voltage across an inductor must be zero over a switching cycle to avoid saturation. Therefore, if the output voltage, for a given point in the switching cycle, is created by a certain winding excitation, the equal and opposite winding excitation must occur in the second half of the

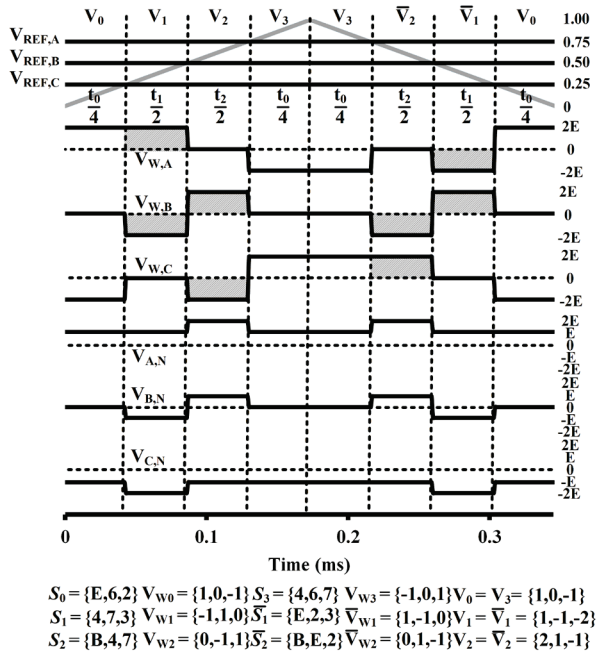


Fig. 4-15. The resultant three-phase winding voltages and output voltages over a carrier cycle, T_S = 333 μs, under the 'WCME' space vector approach for the NPC-CIC at the point 'V_{OUT}' in Fig. 4-13.

switching cycle. The latter condition must also occur for all three phases over the switching cycle, or the three-limb coupled inductor will saturate, leading to excessive winding current magnitudes.

Fig. 4-15 illustrates a switching sequence satisfying the 'nearest three' vector condition of space vector modulation, while keeping the average winding voltage per switching cycle zero, i.e. (4.7). Note the output states $\{V_{A,N},V_{B,N},V_{C,N}\}$ are included in Fig. 4-15 for clarity on which states are selected. One important note about Fig. 4-15 is that the zero state vectors, i.e. V_0 and V_3, have no need for an equal and opposite reversal, i.e. V_1 and $\overline{V_1}$, since they have equal vector output states (or are redundant combinations of that output state). Therefore, V_0 in both segments of the carrier cycle can have the same winding excitation, as it has the same timing, $t_0/4$, as V_3, which provides the equal and opposite winding excitation necessary. By reducing the number of winding voltage 'flips' the average increase in switching frequency can be reduced. Therefore, only the active vectors, i.e. V_1 and V_2, need to have inverted winding voltage excitations in the second half of the carrier cycle.

By maintaining the 'nearest three' vector sequence approach, the common mode winding voltages can be eliminated with no impact on conversion quality up to a modulation depth of 0.75. Furthermore, voltage vectors can be selected to minimize the device switching frequency during operation. Both of these points were identified as

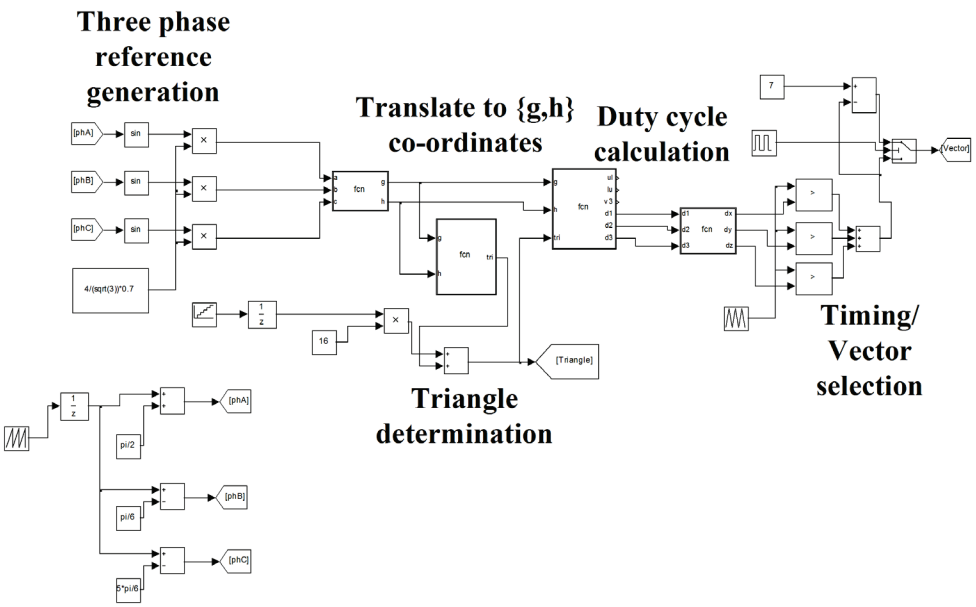


Fig. 4-16. MATLAB/SIMULINK representation of the translation of the three-phase references for triangle determination, and then calculation of duty cycles

challenges to three-limb coupled inductor operation in Chapter 3, and hence providing the motivation to use space vector analysis. To distinguish this approach against other modulation schemes mentioned thus far, the 'winding common-mode elimination space vector pulse-width modulation' is denoted 'WCME' SVPWM.

4.3.2 Implementation of 'WCME' SVPWM

This section details the selection of the 12 switching signals (or gating signals) from desired output voltage states and develops the 'WCME' space vector approach in a MATLAB/SIMULINK environment. Essentially, the space vector algorithm from [80], along with the selection of vectors, based on the optimized space vector switching presented in [79], is translated to the NPC-CIC inverter using the 'WCME' approach.

In order to implement the 'WCME' SVPWM scheme for the NPC-CIC, two stages must occur:

1. The calculation of duty cycles for each triangle in Fig. 4-12, summarized in Fig. 4-16.
2. The translation of the triangle co-ordinate vectors to actual switching states in the converter, summarized in Fig. 4-17.

The calculation of the duty cycles uses established algorithms for multi-level space vector modulation, i.e. [80] and the detailed procedure given in Section 2.4. In brief, the three-phase references are translated into a two-dimensional co-ordinate system

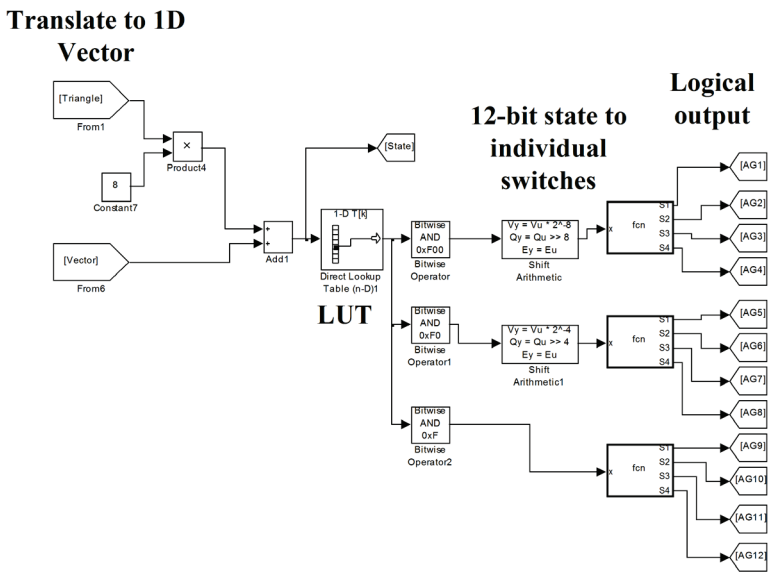


Fig. 4-17. MATLAB/SIMULINK representation of the translation of the 'triangle number' and 'vector number' to an index position for the LUT, which stores the 'switching state' for the NPC-CIC

(with axes at 60°) to locate the reference voltage in the appropriate bounding triangle, i.e. (2.7). Then, using (2.10)-(2.13), the duty cycle for each vector is calculated.

After the duty cycles are calculated, the signals d_1, d_2, d_3 are produced, corresponding to the timing of vectors V_1, V_2, and V_3 (and therefore V_0). However, this calculation does not taken into account that that the sequence should follow: i.e. V_0, V_1 and so forth. Instead, given that each duty cycle, d_N, is relative to the half period, $T_S/2$, the scaled duty cycles d_X, d_Y and d_Z are found according to (4.8), (4.9) and (4.10) respectively.

$$d_Z = d_3 / 2 \tag{4.8}$$

$$d_X = d_1 + d_3 / 2 \tag{4.9}$$

$$d_Y = d_2 + d_1 + d_3 / 2 \tag{4.10}$$

With d_X, d_Y, and d_Z calculated from (4.8) to (4.10), the net result is that the vectors will switch according to the center-aligned space vector pattern, for example, the sequence in Fig. 4.15. Additionally, by giving a numerical association to the vector number, e.g. '1' for 'V_1', a lookup table index is related to the eight vector states per triangle, as per (4.11).

$$8 \cdot \text{Triangle} + \text{Vector} = \text{Index} \tag{4.11}$$

This index is then used in the look-up table (or LUT, Fig. 4-17) composed of the switching states of the inverter, for each vector within each triangle. Therefore, the carrier essentially times out the duration of each index position, which then correspond to the duration of a certain switching state. Since there are 96 triangles in total (the transition to

'three-level triangles' will be addressed later in this section), and eight vector segments per triangle, there are 768 possible switching states over a fundamental cycle in the NPC-CIC.

The lookup table stores a 12-bit (as there are 12 switches in the NPC-CIC) number for each vector within a certain triangle, as shown in Fig. 4-17. Decomposing this number into single bits (via the appropriate 4-bit mask for each phase), the appropriate duty cycle for each switch of the NPC-CIC is found. The SIMULINK diagram in Fig. 4-17 summarizes the decomposition step of the procedure. The decision to use a lookup table approach was justified due to the ease of implementation on FPGA based control systems, such as the one used in this thesis.

The last part of the implementation is the actual population of the lookup table itself, which stores the total 768 switching states of the NPC-CIC, and satisfies (4.7), with an optimised selection of vector states. Each triangle illustrated on Fig. 4-12 is associated with an appropriate set of vectors, as selected according to the known rules for minimizing switching frequency in multi-level space vector modulation, [79]. Since each switch combination of the NPC-CIC produces a known output and winding voltage, as per (4.1) and (4.2), the appropriate switch combination needs to be selected for each triangle. Fortunately, all 96 triangle (and associated switch combinations) need not be manually selected; only the first 16 triangles of the first sextant are necessary, as each vector can be iteratively selected for the remaining sextants, as described in [72], and according to (4.12). Note in (4.12), ' θ' refers to the electrical angle of the reference voltage in the first sextant.

$$\begin{aligned} V_C(\theta + 60°) &= V_A(\theta) \\ V_A(\theta + 60°) &= V_B(\theta) \\ V_B(\theta + 60°) &= V_C(\theta) \end{aligned} \tag{4.12}$$

However, one vector state is not available in four of the triangles per sextant (i.e. the light grey triangles in Fig. 4-13), due to the winding common mode elimination condition of (4.7). Therefore, the modulator must select the larger 'three-level' triangles in these regions. Consider the five-level triangle bound by {2,2,-1}, {2,2,-2} and {2,1,-2}, as highlighted in Fig. 4-12. The vector {2,1,-2} is not possible as only one limb would be excited, and therefore it is not present in Fig. 4-13. In each of these triangles, the algorithm is modified such that the vertices are replaced with those of the equivalent three-level triangle, e.g. {2,2,0}, {2,0,-2} and {2, 2,-2}. Accordingly, the duty cycles are doubled to scale to the larger three-level triangle, such that the equivalent average voltage dwell time is obtained as if it were the five-level triangle.

With each triangle mapped with known voltage vectors, the actual switch combinations for each vector are necessary to populate the look up table. As mentioned in Section 4.1, seven switching states are used to synthesize the output voltage of a given phase, e.g. in phase A ($S_1S_2S_3S_4$): (0110) or '6', (1100) or 'C', (0011) or '3', (0010) or '2', (0111) or '7', (0100) or '4', and (1110) or 'E', which correspond to the output and winding voltages: (0, 0), (2E, 0), (-2E, 0), (-E, -2E), (-E, 2E), (E,-2E) and (E, 2E) respectively. Then, using the same starting condition for each switching cycle, e.g. positive winding voltage, the output vectors for each triangle, corresponding to a switching state, create the 12-bit value for the LUT, according to (4.13). The LUT for all 768 states is shown in the appendix of this thesis.

$$\text{For state 'N': } (S_{1\text{-}4})\cdot 16^2+(S_{5\text{-}8})\cdot 16^1+(S_{9\text{-}12})\cdot 16^0 = \text{LUT(N)} \tag{4.13}$$

4.3.3 Effect of 'WCME' SVPWM on Winding Currents and Line Voltages

By removing the winding common mode voltage in the three-limb coupled inductor, a high permeability path dictates the ripple within each winding, thereby keeping this ripple relatively low - similar to the modified DPWM1 approach in Chapter 3. However, as previously stated, the main challenge of common mode winding elimination is the consequence of these eliminated states on the average device switching frequency and the conversion quality of the coupled inductor converter.

Fig. 4-18 illustrates the upper and lower module currents for the NPC-CIC under the 'flipped carrier' DPWM1 and the 'WCME' SVPWM approach with a 3 kHz carrier frequency. Note that Fig. 4-18 demonstrates a peak ripple reduction by roughly a factor of three; however, this reduction is related to the ratio in permeability of the iron to air paths used in the simulation model. Note also that since this waveform is at a 3 kHz carrier frequency, the 'flipped carrier' DPWM1 scheme would need a 9 kHz carrier frequency, to bring the ripple close to that of the 'WCME' SVPWM - significantly favouring the 'WCME' SVPWM in terms of switching loss and electromagnetic interference reduction.

Since the 'WCME' SVPWM has full five-level switching (i.e. the line voltage step across the load is 'E'), it is important to note how this modulation approach has a mixed three/five level characteristic beyond modulation depths of 0.75. Note Fig. 4-19 where the line voltages for the 'WCME' SVPWM approach are illustrated at the modulation depths of 0.7, 0.8 and 0.9. At the modulation depth of 0.7, the line voltage is identical to a traditional five-level topology. However, with the modulation depths of 0.8

and 0.9, the duration of five-level characteristics decrease, while the three-level becomes more prominent; corresponding to the reference vector passing through the outer five-level triangle, i.e. {2,1,-1}, {2,0,-2}, and {1,-1,-2}, with decreasing duration.

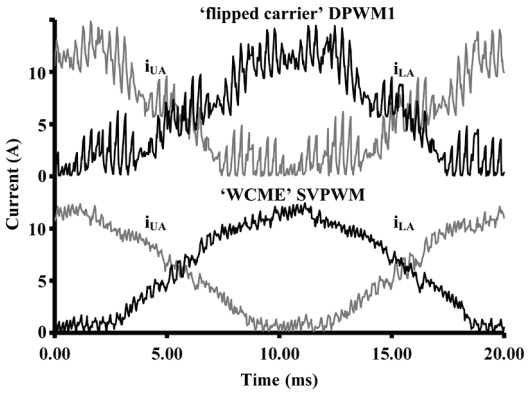


Fig. 4-18. Simulated module currents for phase A of the NPC-CIC with the 'flipped carrier' DPWM1 and 'WCME' space vector approach with f_O = 50 Hz, f_C = 3 kHz, V_{DC} = 300V, L_W = 4 mH, L_{AC} = 800 µH, and R_{AC} = 18 Ω (delta connected)

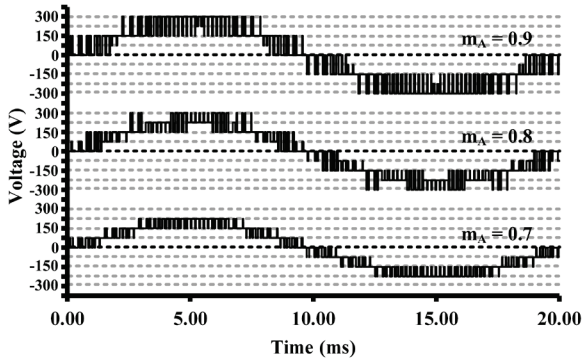


Fig. 4-19. Simulated line voltage, V_{AB}, of the NPC-CIC under the 'WCME' space vector approach showing under increasing modulation depths of 0.7, 0.8 and 0.9 with f_O = 50 Hz, f_C = 3 kHz, V_{DC} = 300V, L_W = 4 mH, L_{AC} = 800 µH, and R_{AC} = 18 Ω (delta connected)

4.3.4 Average Device Switching Frequency

According to [79], space vector modulation approaches should synthesize the 'nearest three' vectors for a given output. Furthermore, each vector transition should, at most, have one switch turning off and one switching turning on per switching cycle. This condition gives the lowest possible average device switching frequency for the highest possible output quality, e.g. center-aligned space vector modulation.

Consider Fig. 4-20, which illustrates the switching pulses for phase A of the NPC-CIC, under the 'WCME' SVPWM approach, for two modulation depths of 0.2 and 0.7, over 30° of a fundamental cycle. While the approach discussed in Section 4.2 can be

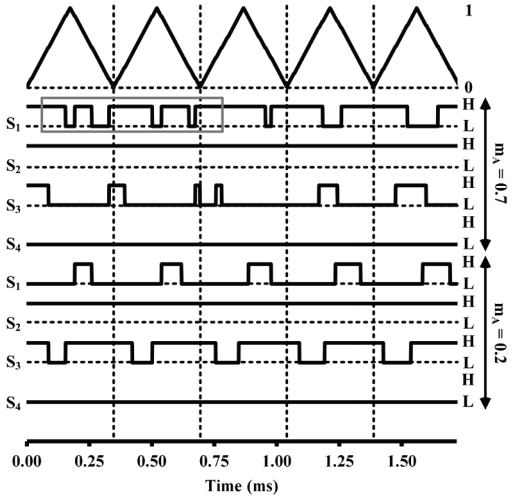


Fig. 4-20. Phase A gating signals (or switching signals) over five carrier cycles, where T_S = 333 μs, for a modulation depth of 0.7 and 0.2.

applied to a discontinuous 'space vector' approach; in this thesis, a center-aligned version of space vector modulation is used due to the emphasis on output conversion quality, and therefore, the average device switching frequency is naturally higher than the 'flipped carrier' DPWM1. Even if the proposed method uses a discontinuous approach, the redundant vector combinations are still removed due to the condition of (4.7). Thus, for some modulation depths, the remaining vectors make it impossible to have only one switch transition per vector change. However, while the average device switching frequency must increase, it does not have to increase by double (unlike chapter 3).

In Fig. 4-20, the 30° capture of the fundamental cycle for phase A is used to demonstrate the device switching frequency. With modulation depths below 0.25, there is no effective increase in the average device switching frequency, i.e. each switch is active for 180° of the fundamental cycle, and the average device frequency is effectively half the carrier frequency ($f_C/2$). On the other hand, for modulation depths over 0.5, extra switching segments occur, e.g. the highlighted section of Fig. 4-20, where the switch has two switching cycles per carrier cycle. Effectively, this occurs for 1/3 of the active switching period, and therefore the average device switching frequency is $2f_C/3$, when the modulation depth is 0.75. After this point, the average device switching frequency decreases due to the mixed 3/5-level switching, this frequency is at $f_C/2$ again.

4.3.5. Neutral Point Balancing

One significant point about any neutral point clamped (or any split capacitor connection) is the center point between the two capacitors on the dc-link, and their ability

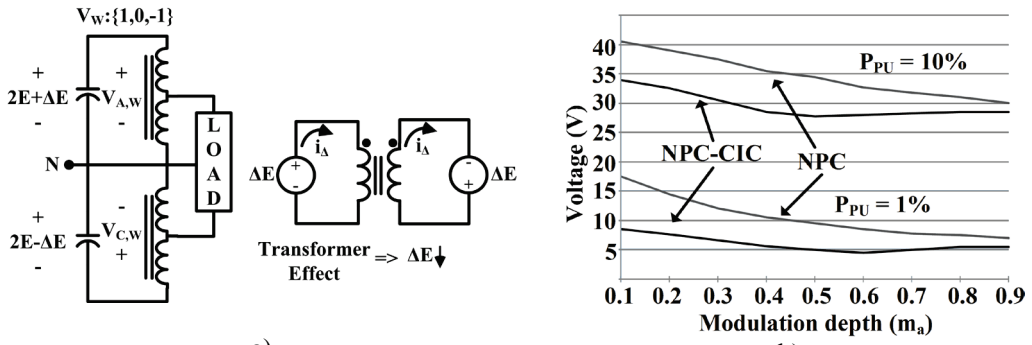


Fig. 4-21. Neutral point balancing of the NPC-CIC where a) illustrates the transformer effect present due to the three-phase coupled inductor and b) the simulated effect of the three-phase coupled inductor against the standard three-level NPC converter. The split-capacitors are unbalanced with resistances at power levels relative to the load resistance (e.g. 10% meaning the unbalancing resistance are sized to draw 10% of the power relative to the ac output power).

to maintain an even split of the applied dc voltage. This problem has been analyzed in detail, e.g. [32], and parasitic effects significantly influence the split-capacitor voltage balance, e.g. non-ideal switching behavior, and load unbalances. Thus, a closed loop controller is often used to inject a dc offset, into the modulator reference, to correct for any unbalance.

While the 'WCME' SVPWM approach does not limit the applicability of any neutral point correction scheme, since it can generate symmetric pulse-width modulation, it will also not introduce any unbalance to the split-capacitor connection. However, one of the advantages of the mutually coupled phases in the three-limb coupled inductor, is that each phase can act to balance the dc voltages of the remaining two phases. Specifically, by using a three-limb coupled inductor core, the neutral point can withstand more 'unbalanced' currents than in the three-level neutral point clamped topology.

Consider Fig. 4-21 a), which illustrates the equivalent three-phase circuit for an output voltage of {1, 0, -1}, with the three-phase coupled inductor excitation {1, 0, -1}. Since the two phases are coupled through the iron core, each capacitor can be considered to be coupled via a 1:1 turn ratio transformer, Fig. 4-21 a). Since the 'WCME' approach only uses those voltage states where the coupled inductor is excited by equal and opposite phases, this balancing effect is maximized.

If an average voltage unbalance exists of 2ΔE in the dc-link, it is equivalent to one capacitor being 2E+ΔE and the other being 2E-ΔE, Fig. 4-21 a). This unbalanced voltage would induce a balancing current to flow into the dot (left hand side of equivalent circuit), and flow out of the dot (on the right hand side), causing the unbalance ΔE to become smaller in magnitude. Positive ΔE that drives this current, reducing the energy

stored in the capacitor corresponding to this unbalance, until an equilibrium point is established.

Fig. 4-21 b) demonstrates the neutral point deviation on a 300V system (150V would be the equal split across these capacitors), under a 2:1 power unbalance on the dc-link (i.e. a resistor is used to draw twice the power from the top rail as the bottom) for both the NPC-CIC and a standard NPC inverter. Furthermore, since the load can balance the neutral point connection, two power ratios, relative to the load, of 10%, and 1% are used. At a carrier frequency of 20 kHz, the NPC-CIC is modulated with interleaved carriers, and the NPC converter is PD modulated. It can be seen from Fig. 4-18 b) that the NPC-CIC has a smaller deviation from 150V (i.e. 27V compared to 36V for $m_A = 0.5$ under a 10% per-unit unbalancing power) over the modulation range compared to the NPC inverter.

However, as this correcting factor depends on the coupling between limbs, this factor can have limitations. To get a better idea of how the coupling between limbs helps correct an unbalanced voltage, this effect is isolated and examined in detail in Chapter 5. While the circuit topology is slightly different, the natural (or automatic) correction of the unbalanced voltages in the split-capacitor is identical. Therefore, this chapter will not delve into the influence of coupling between limbs and the balancing power of the coupled inductor converters, as this is covered in Chapter 5.

4.4 Experimental Setup

A 10kW experimental prototype is constructed, as shown in Fig. 4-22, to illustrate the general performance of the NPC-CIC, and the performance of the proposed 'WCME' modulation approach.

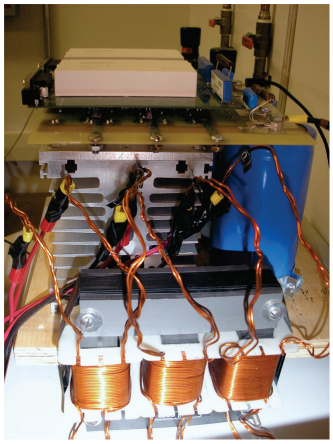


Fig. 4-22. Three-phase NPC-CIC prototype with three-phase, three-limb coupled inductor pictured

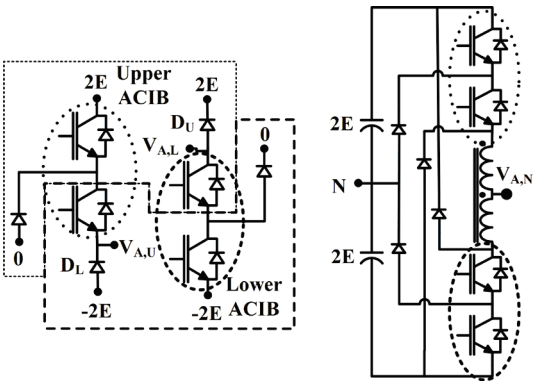


Fig. 4-23. Experimental prototype construction from two ACIB modules from Semikron [101]. Six asymmetric half-bridges are used to construct the NPC-CIC with the modules arranged as illustrated.

The organization of this section is as follows: a discussion of the construction of the NPC-CIC prototype, the three-limb coupled inductor core used, and the software environment employed to pulse width modulate the NPC-CIC.

4.4.1 Construction of a 10kW Three-phase NPC-CIC prototype

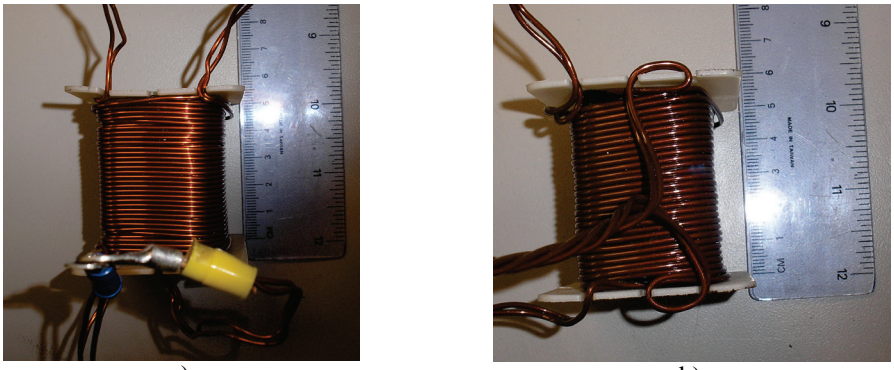
One important point for the practical implementation of the NPC-CIC is the construction of a single-phase leg, as pictured in Fig. 4-23. In this figure, the NPC-CIC is the product of six asymmetrical bridges. Note that instead of requiring 24 devices, the NPC-CIC is constructed with six modules in total, lowering the design effort. In this prototype, six modules, (asymmetric bridge pack) SK75GARL065E, are selected with the ratings: 50A (peak collector current), 600V, and a maximum switching frequency of 20 kHz. To drive the IGBTs, dual SKHI61R drivers from SEMIKRON are used, and the supporting circuitry is built according to [101].

In all the given experimental results, the switching frequency is set at 3 kHz with a 300V dc-link (controlled with a 6 kW dc supply). For the R/L load tests: a three-phase series inductor with a dc inductance of 1.5 mH (3.5% at 50 Hz), and a three-phase delta connected 42 Ω resistor bank is used to load the inverter (P_{BASE} = 3.2 kW, V_{BASE} = 208V).

4.4.2 Three-limb Coupled Inductor Core

The three-limb coupled inductor core, as in Chapter 3, uses a ‘7/8’ sized E-I core configuration is selected. The air gap of this core was kept as small as possible by clamping the ‘I’ bar to the ‘E’ core, and 6-mil laminations from [98] were selected for all tests. While one set of windings, Fig. 4-24 a), is used to obtain a measured total inductance (L_T) of 12 mH, another set of windings was also used, as shown in Fig. 4-24 b), to achieve a smaller total inductance of 4 mH. Fig. 4-22 illustrates the final

construction of the cores with the 12 mH set of windings. Note that due to one coil configuration having fewer turns, the leakage reactance between these two coils will also differ.



a) b)

Fig. 4-24. Three-phase windings used on the three-limb core: a) 128 windings per coil, with L_W = 4 mH (L_T = 12 mH), and b) 64 windings per coil, with L_W = 1 mH (L_T = 4 mH). Both coils are constructed by winding two parallel sets of wires together, but using 16 AWG in a) and 15 AWG in b).

4.4.3 Software Setup

To implement either the 'WCME' or 'flipped carrier' based modulation schemes, a graphically programmable FPGA, as pictured in Fig. 4-25, from LabView is used to minimize development time. As the MATLAB/SIMULINK models were designed to use spreadsheets, the development of the FPGA program designed around this same concept. Due to the graphic nature of LabView, the development of the programs used for this thesis can be derived from the discussion presented thus far, and therefore are not included here.

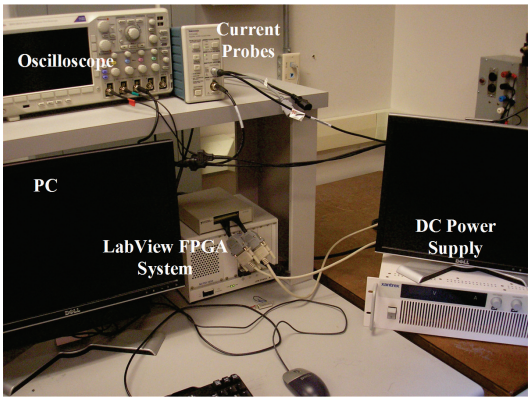


Fig. 4-25. Experimental LabView development system: pictured with oscilloscope, current probes, and 3 kW dc power supply

With either scheme, the FPGA program essentially has two tasks loops: a low frequency (i.e. at the carrier frequency) loop for calculation of the duty cycles, and pulse-

width modulation loop at the clock frequency of the FPGA unit (40 MHz). In the latter loop, the devices are controlled by active comparison of the duty cycles with a carrier wave at a 2.5ns resolution.

4.5 Experimental Results and Discussion

To verify the simulated results discussed in this chapter, the experimental results focus on two concepts: validation of the NPC-CIC as a multi-level inverter and the demonstration of the 'WCME' SVPWM as a necessary condition to allow for low switching frequencies with the three-limb coupled inductor. Therefore, the experimental results section includes a discussion to put each section into context, and these sections are as follows:

- General NPC-CIC performance (e.g. three-phase currents)
- Experimental confirmation of winding voltage elimination
- Output performance of the NPC-CIC under the 'WCME' approach

4.5.1 General NPC-CIC performance

As the general goal of the NPC-CIC development is aimed at a high-conversion quality to drive low voltage, low-inductance high speed electric machines, the first experimental demonstration deals with induction motor operation. In Fig. 4-26 a), an unloaded high-speed induction machine (with the construction details in [100]), is used to demonstrate the visual reduction of phase current ripple of the NPC-CIC against a standard two-level six-switch inverter. In Fig. 4-26 a), a standard interleaved carrier-based scheme modulates the NPC-CIC with a switching frequency of 15 kHz (due to the high electrical frequency of the electric machine).

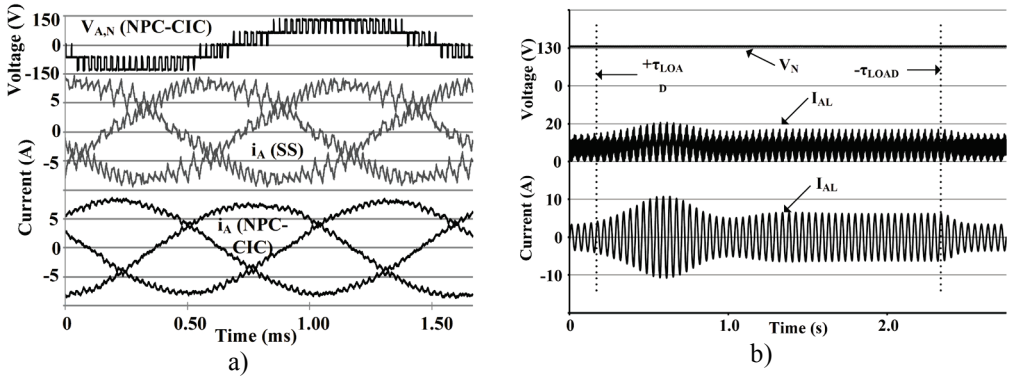
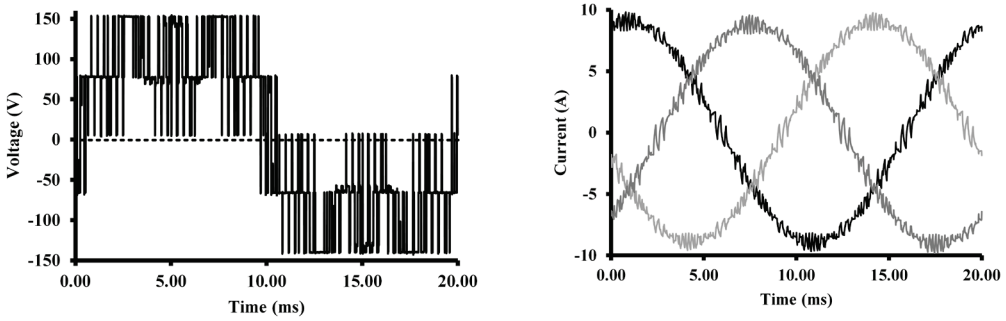


Fig. 4-26. Motor validation with a) on an unloaded 600 Hz (18,000 rpm) induction machine, illustrating the NPC-CIC phase currents (lower set) against phase currents generated by a six-switch inverter under SVPWM and b) the neutral point stability of the NPC-CIC under a step change in load on a 2HP 60Hz (1800 rpm) induction machine. f_C = 15 kHz, V_{DC} = 260V.



a) b)

Fig. 4-27. Experimental: a) phase voltage, $V_{A,N}$ and b) phase currents at a modulation depth of 0.7, f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 4 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)

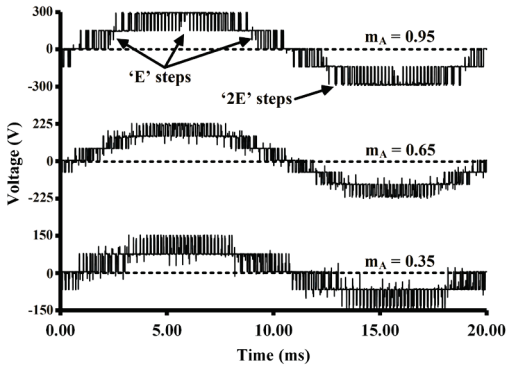


Fig. 4-28. Experimental line voltage, V_{AB}, at modulation depths 0.35, 0.65 and 0.95, f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 4 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)

To illustrate the neutral point stability of the NPC-CIC under step-load changes, the experimental prototype is tested on a 2HP hysteresis dynamometer (MAGTROL DSP 6000). A step change in power (at the synchronous speed of 1800 rpm) from unloaded to 1 HP is performed, as seen in Fig. 4-26 b), and maintains the expected voltage of 130 before and after each change in load.

In Figs. 4-27 a) and b), the general inverter performance under the 'WCME' SVPWM approach, at a modulation depth of 0.7, with the corresponding phase voltage $V_{A,N}$, and the three phase currents. Additionally, Fig. 4-28 shows the line voltage, V_{AB}, for modulation depths 0.35, 0.65 and 0.95 under the 'WCME' SVPWM approach. This figure illustrates the mixed 3/5-level PWM for modulation depths over 0.75 (denoted by '2E' and 'E' respectively), and the full five-level switching below this modulation depth. The slightly distorted appearance of the line voltages is due to inadequate decoupling capacitance across each switch to cancel the dc-link inductance within the switch path.

4.5.1 Winding Current Reduction with the 'WCME' SVPWM Approach

Using only the high permeability states within the three-limb inductor allows the module current ripple, i_L and i_U, to be as minimized as much as possible (for a given inductance). With the 1 mH coils, Fig. 4-29 is a prime example of the motivation behind the winding common mode elimination. In this figure, the circulating winding current, i_{CW}, for phase A produced by the 'WCME' SVPWM approach is compared against the same current produced by the 'flipped carrier' DPWM1 approach. Eliminating the common mode winding voltages has reduced the peak circulating winding ripple current from approximately 20A to 2.5A. Note that this reduction is importance as it is dependent on the leakage reactance of the three-limb core from phase to phase.

With the 4 mH coils, Figs. 4-30 a) and b) illustrate the circulating winding current, i_{CW}, in phase A for both modulation approaches, under the modulation depths 0.35, 0.65 and 0.95. Like Fig. 4-29, the winding current ripple for the 'WCME' approach is significantly smaller than the 'flipped carrier' DPWM1. Under these modulation depths, the ac component of the common mode winding current under the 'WCME' approach is 0.25A, 0.26A, and 0.39A while the 'flipped carrier' DPWM1 approach is 2.34A, 3.95A and 5.81A. Clearly, for both Figs. 4-29 and 4-30, the reduction in circulating current for the 'WCME' approach is significant.

Fig. 4-31 a) illustrates the common mode winding current, i_{CM} between both schemes. It is important to note the modulation depth chosen, i.e. $m_A = 0.7$, is the worst-case ripple for the 'flipped carrier' DPWM scheme. At this modulation point, the alignment by flipping the winding excitation is at its minimal point, producing large duration common mode winding voltages, resulting in the large difference in current ripple seen in Fig. 4-31. Furthermore, in regards to the 'WCME' approach, it is apparently that some common mode winding current is circulating through the inverter. The presence of this current is a consequence of the practical implementation of the scheme, i.e. the scheme depends on matching winding voltages. As active devices can have different rise and fall times for their blocking current and voltage, some winding voltages is present, as seen in Fig. 4-31 a).

Lastly, Fig. 4-31 b) illustrates the winding volt-seconds for the three-limb coupled inductor between the two three-limb applicable schemes. It is clear that the 'WCME' approach causes the three-limb inductor to experimental smaller winding voltages for the modulation depths above 0.75 – confirming the mixed three/five-level approach to this scheme. However, since the 'flipped carrier' DPWM1 scheme uses a

discontinuous approach, the winding voltage duration per fundamental cycle should naturally be lower than the 'WCME' approach at lower modulation depths.

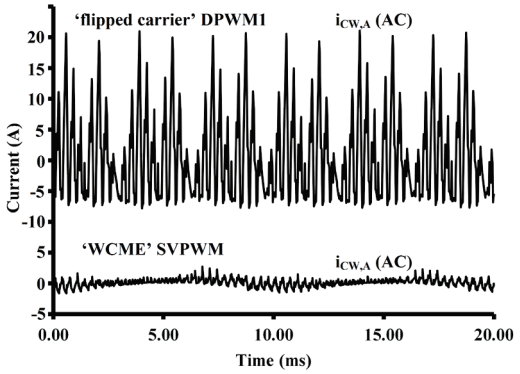
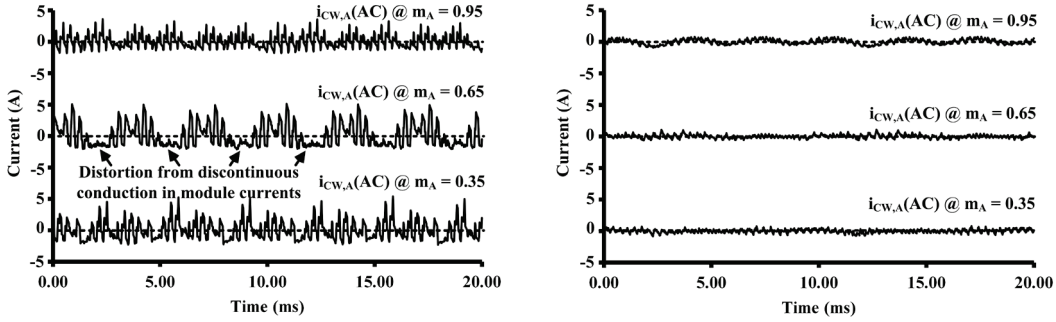
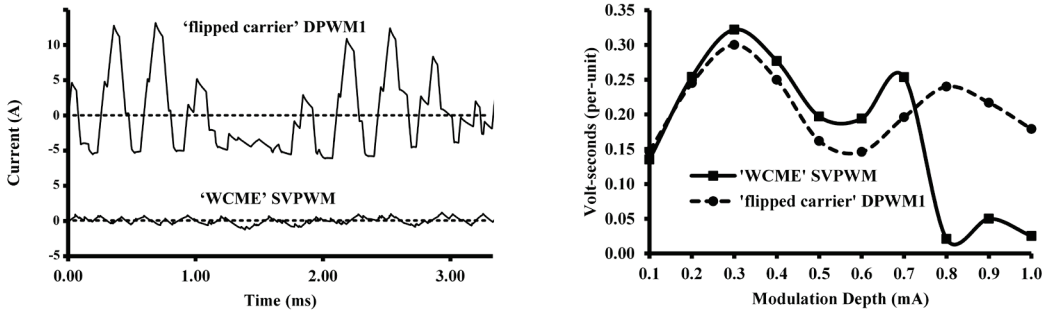


Fig. 4-29. Circulating winding current, i_{CW}, of phase A for 'flipped carrier' DPWM1 and 'WCME' SVPWM with a modulation depth of 0.7, f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 1 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)



a) b)

Fig. 4-30. Circulating winding current, i_{CW}, of phase A for a) 'flipped carrier' DPWM1 and b) 'WCME' SVPWM at the modulation depths 0.35, 0.65 and 0.95, f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 4 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)



a) b)

Fig. 4-31. Experimental 'flipped carrier' DPWM1 and 'WCME' SVPWM with a) the three-phase common mode current, i_{CM}, and b) the winding volt-seconds on phase A versus modulation depth; f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 4 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)

With a discontinuous version of the ‘WCME’ scheme, one would expect a reduction in winding volt-seconds, but the most important result from Fig. 4-31 b) is that only the modulation depth region of 0.5 to 0.75 sees a noticeable difference between the two approaches. This difference is due to the increased device switching during this region for the ‘WCME’ approach, but at its worst point, this difference is only 0.05 per-unit. The meaning from this result is that, if the winding current ripple magnitude were close between the two schemes, the iron losses induced in the core would also be similar.

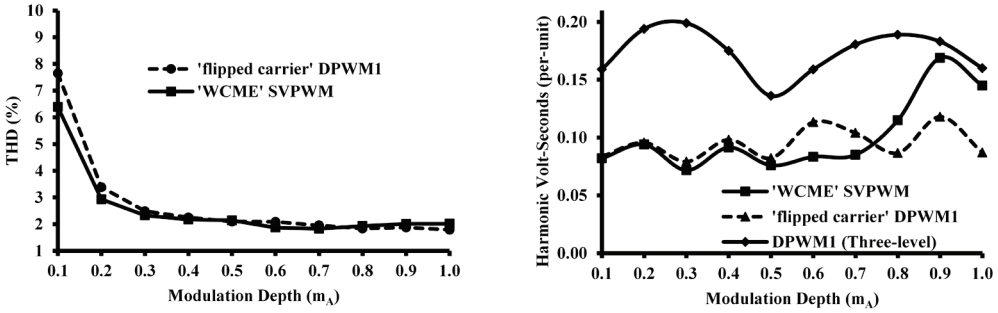
4.5.2. Performance with No Common Mode Winding Voltages

Since the condition of zero common mode winding voltages eliminates certain vectors - otherwise achievable for standard interleaved schemes using separate inductors - it is important to examine the converter performance. Fig. 4-32 a) provides the total harmonic distortion (THD) of the current between the two schemes. In this figure, the ‘WCME’ approach sees increased distortion during the mixed three/five-level PWM regions, as opposed to the purely five-level PWM produced by the ‘flipped carrier’ DPWM1 approach. Below the modulation depth of 0.75, the output distortion is generally lower for the ‘WCME’ approach, due to the use of ‘center-aligned’ space vector modulation. Note that since the filter inductance is relatively high (3.5%), and the harmonic currents produced by both schemes are small, only minor differences between the schemes were obtained in Fig. 4-32 a).

To better clarify the differences in conversion quality between the two schemes, the line voltage harmonic volt-seconds is shown in Fig. 4-32 b). This figure corresponds to the approximate size of the inductive filter needed between the two schemes to obtain a relatively undistorted sinusoidal output. Up to a modulation depth of 0.75, as expected from using the 'center-aligned' space vector approach, the harmonic volt-seconds are lower than that obtained for the 'flipped carrier' DPWM1 scheme. Furthermore, after this modulation depth, the harmonic volt-seconds for the 'WCME' approach are lower than the reference three-level results, due to the mixed three/five-level characteristics of the former approach. While the 'flipped carrier' DPWM1 results lower harmonic volt-seconds, it should be noted that this scheme has already shown to be impractical at this carrier frequency, due to the excessive module current ripple. Therefore, it is not entirely accurate to compare filter sizes between the two converters.

Finally, the most important result of the winding common mode elimination is the impact of this scheme on the efficiency of the converter. Fig. 4-33 illustrates the

efficiency over the modulation range between the two approaches, and the result is clear: the elimination of the common mode winding voltages significantly improves the efficiency over the output range of the converter. With this figure, the 'WCME' approach has met its goal: a clear improvement in efficiency when the converter is limited by switching frequency (e.g. in higher power devices), while maintaining a high dc/ac conversion quality.



a) b)

Fig. 4-32. Experimental 'flipped carrier' DPWM1 and 'WCME' SVPWM with a) the total harmonic distortion of the phase current and b) the line voltage harmonic volt-seconds of V_{AB} versus modulation depth; f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 4 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)

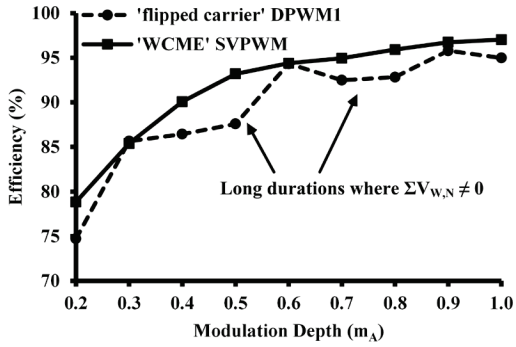


Fig. 4-33. Experimental 'flipped carrier' DPWM1 and 'WCME' SVPWM total conversion efficiency (i.e. P_{OUT}/P_{IN}) versus modulation depth; f_C = 3 kHz, V_{DC} = 300V, f_O = 50 Hz, L_W = 4 mH, L_{AC} = 1.5 mH, R_{AC} = 42 Ω (in delta)

4.6 Chapter Summary

This chapter presents the NPC-CIC as an evolution of the asymmetric bridge coupled inductor converter as applied in a three-phase, five-level, dc/ac converter system. With consideration of the examined switching states, a viable switching approach, termed 'WCME' SVPWM, is illustrated to eliminate the common mode winding voltage states, at a minimal increase in device switching frequency and decrease in conversion quality. An experimental prototype is developed and the general performance of the NPC-CIC is

presented, along with the proposed modulation scheme. The 'WCME' significantly improves the conversion efficiency, as evidenced by the experimental results, without significantly affecting the conversion quality or the device switching frequency for most of the modulation range.

Chapter 5 - Asymmetric Coupled Inductor Bridge as a Modular Balancing Bridge

In this chapter, a topological variation to the ACIB, the Modular Balancing Bridge (MBB), see Fig. 5-1, is presented for automatically balancing a series connection of voltage sources, e.g. battery cells in an electric vehicle. Analysis of the MBB is presented to predict the average balancing currents that flow under a range of voltage imbalances, and these currents are related to various circuit parameters to aide in design.

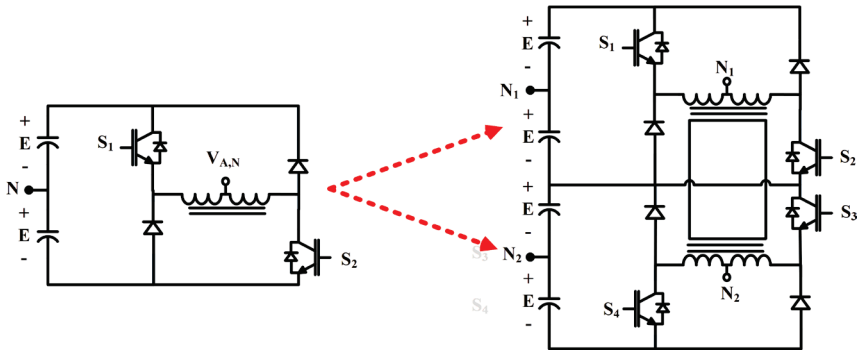


Fig. 5-1. ACIB configuration: a modular balancing bridge for balancing a series of unbalanced voltage sources

Specifically, the balancing action for two internal voltage sources within the MBB is described, and the resulting current from an internal voltage difference is derived. The balancing of voltages between MBBs is then described, along with the resulting current that flows due to these voltage unbalances. Due to the modular nature of the circuit, commercial transformers are selected to demonstrate the automatic balancing of the MBB. Using the weight of these transformers and the derived maximum power relationships, the power density is demonstrated for the MBB. Practical design considerations are presented, and experimental results confirm operation of the MBB.

5.1 The Modular Balancing Bridge

The novelty of the MBB is primarily due to its modular approach to balancing a series of voltage sources. While some patents exist for 'automatic', or balancing without voltage feedback, for split-capacitors [102, 103], the MBB is able to provide automatic voltage balancing for an arbitrary number of series connected voltage sources. This is unlike traditional balancing circuits, which require co-ordination of the battery information from the Battery Management System (BMS), as seen in Fig. 5-2, and specific control algorithms, according to the cell chemistry of the battery

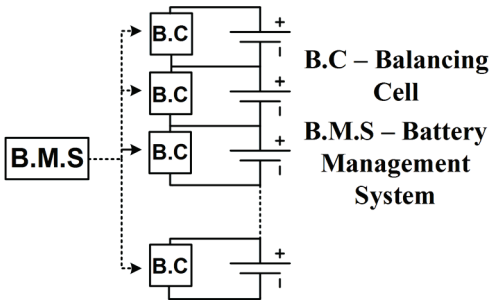


Fig. 5-2. Relationship between the battery management system and balancing cell for a series of connected battery cells

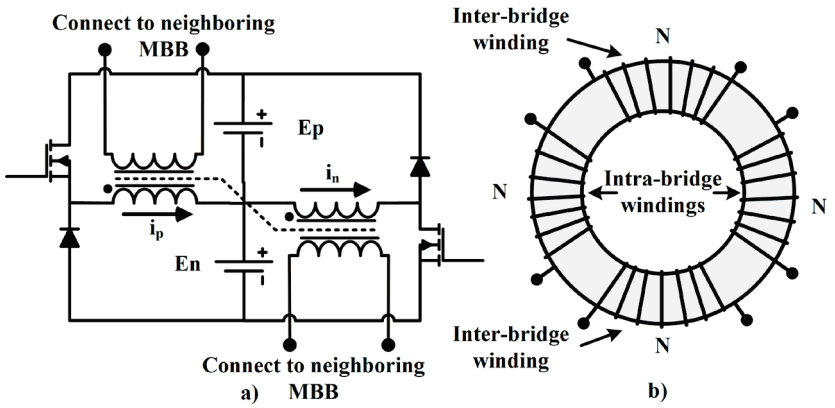


Fig. 5-3. The ACIB: a) as a single modular balancing bridge (MBB) and b) the four-winding '1:1:1:1' coupled inductor showing: inter-bridge and intra-bridge windings

selected. Unlike the works presented in [91-93], the MBB does not require custom transformer designs for different cell configurations. Furthermore, since the transformer is identical for each MBB, the overall part cost is lowered due to using commercially available transformers and through volume cost discounts.

The MBB is essentially a multi-level dc/dc converter, as seen in Fig. 5-3 a). In Fig. 5-3 b), the 1:1:1:1 transformer of the MBB has four-windings per core: two windings internal to the MBB (i.e. the intra-bridge windings), and two windings cascading one MBB to neighboring MBBs (i.e. the inter-bridge windings). This second set of windings is unique to the MBB and is required to extend the balancing action across a series of voltage sources, e.g. battery cells. Lastly, it is important to note that the components within each MBB have identical ratings, size and current/voltage stresses.

5.2 Intra-bridge Voltage Balancing of the MBB

In this section, the balancing of the two internal battery cells, Ep and En, is related to the voltage unbalance within this internal battery pair, and the resulting average balancing current. As lithium-ion batteries have complex current to terminal voltage

relationships [80], the average balancing current can be related to the circuit parameters and therefore, the intra-balancing ability of the MBB. Note that the module currents of Chapter 3 have been renamed 'i_p' and 'i_n' to help with the discussion presented in this chapter.

A SPICE simulation model of the circuit in Fig. 5-3 a) is developed, as shown in Fig. 5-4, to verify the expression developed for the intra-bridge balancing current. This model uses a realistic diode model that incorporates a series resistance and device capacitance. However, for simplicity, and since the effect of the parasitic device parameters, such as device capacitance, is described in Section 5.4, the MOSFET switch is modeled as a switched resistance, as per Fig. 5-4 - with the resistance corresponding to the on-state resistance of the device. Finally, the coupled inductor is modeled using a simple four-inductor circuit, as seen in Fig. 5-4, with a coupling co-efficient between the two windings of approximately 0.99. Note that all series resistances, i.e. winding or any other parasitic resistance, is lumped together in the coupled inductor model.

5.2.1 Basic Operation of the MBB for Unbalanced Intra-bridge Voltages

The analysis of the intra-bridge balancing is based on circuit inductances and voltage unbalance, but due to the relatively small operating power level, the parasitic device resistances are ignored in this section. As such, three basic circuit parameters are useful for predicting the balancing currents flowing in the circuit: the average voltage between a pair of battery cells, Ep and En, as per (5.1), the per-unit voltage unbalance between this pair of battery cells, as per (5.2) and the base current, as per (5.3).

$$(Ep + En)/2 = \overline{Epn} \tag{5.1}$$

$$\Delta = (Ep - En)/(Ep + En) \tag{5.2}$$

$$I_{BASE} = \frac{E_{BASE}}{L_W f_C}, \quad E_{BASE} = \overline{Epn} \tag{5.3}$$

To maximize the intra-bridge voltage balancing, the duty cycle of each switch in Fig. 5-3 a), is set to 50% - as a duty cycle less than 50% reduces the voltage balancing ability, and greater than 50% could potentially saturate the coupled inductor. Due to the coupling between the ‘p’ and ‘n’ windings (as per Fig. 5-3), the magnetizing inductance of the core is four times the winding inductance, L_W. Therefore, over a switching cycle, T_S, the magnetizing inductance, L_M, is alternatively excited by $2\overline{Epn}$ and $-2\overline{Epn}$, as in Fig. 5-5 a) and b).

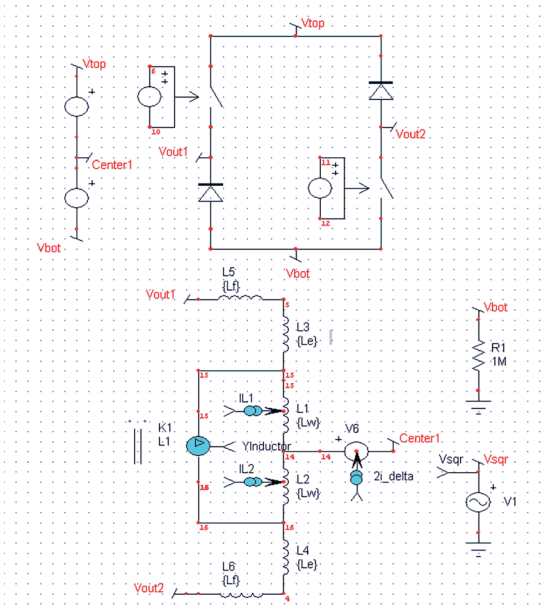


Fig. 5-4. SPICE simulation model of a single MBB to illustrate the intra-voltage balancing between two internal voltage sources

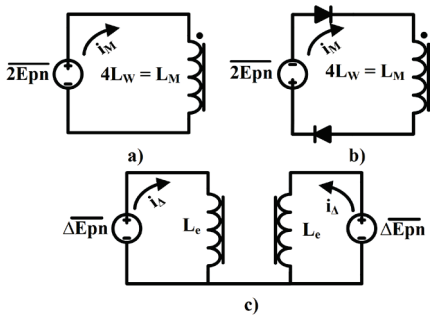


Fig. 5-5. Ideal equivalent circuits with magnetizing current paths for a) positive excitation and b) negative excitation with c) the differential current, i_Δ, equivalent circuit

If either battery voltage differs from the average voltage, as per (5.2), a differential voltage ($\Delta\overline{Epn}$) exists across the leakage inductance, L_e, of a winding within the coupled inductor. As a result, a differential current component exists, i_Δ, in addition to the magnetizing current, i_M, in each winding, as per Fig. 5.5 c). In either excitation state, a path for positive or negative differential current flows, resulting in $i_M + i_\Delta$ flowing from the cell with the higher than average voltage, i.e. $(1+\Delta)\overline{Epn}$, and $i_M - i_\Delta$ flowing from the cell with the lower than average, i.e. $(1-\Delta)\ \overline{Epn}$. Hence, a differential current of $2i_\Delta$ flows into the center tap of Ep and En, causing the voltage unbalance to reduce. Effectively, the balancing current, i_Δ, is removing charge from the cell with the higher than average voltage, and placing this charge in the cell with the lower than average voltage, until the voltage difference 'Δ' is zero. This balancing current, i_Δ, is the 'intra-bridge balancing

current', and the average of this current is related to the balancing power of the circuit for intra-bridge voltage unbalances.

To understand how the intra-bridge balancing current is influenced by the per-unit leakage inductance, L_{pu}, and the per-unit intra-bridge voltage unbalance, Δ, Fig. 5-6 a) illustrates the module currents, i_p and i_n. In Fig. 5-6 a), a per-unit intra-bridge unbalance $\Delta = 1\%$ causes an increase of i_Δ and decrease of i_Δ relative to i_M, for i_p and i_n respectively. Note that due to device conduction drops of the diodes, the conduction period is reduced by T_S/T_S', which can be related to the per-unit diode voltage drop v_D, via 5.4:

$$\frac{T_S}{T_S'} \approx \frac{2\overline{Epn}}{2\overline{Epn} + 2V_D} \equiv \frac{1}{1+v_D} \tag{5.4}$$

Furthermore, the conduction time T_d, is illustrated in Fig. 5-6 a), marking the time of positive balancing current during the diode conduction stage (i.e. the de-magnetization period, as shown in Fig. 5-6). After this point, as one of the winding currents is now zero, the balancing current decreases proportionately to $En/2L_W$ or $(1-\Delta)\,\overline{Epn}/2L_W$.

In Fig. 5-6 b), the balancing current is illustrated for both $\Delta = 1\%$ and 2%. Note in this figure during the time T_d, the balancing current is still increasing in magnitude. Therefore, the time T_d can be found by equating the peak module current in at time $T_S/2$, with the time it takes the module current to reach zero, as in (5.5). Note also that the 'n' winding is altered by $I_{BASE}\cdot(1-2\Delta/L_{pu})$ during the switch conduction period (or magnetization period), and $I_{BASE}\cdot(1+2\Delta/L_{pu})$ during the diode conduction period (or de-magnetization period).

$$T_d \approx \frac{T_S}{2}\left[\frac{1-2\Delta/L_{pu}}{1+2\Delta/L_{pu}}\right] \tag{5.5}$$

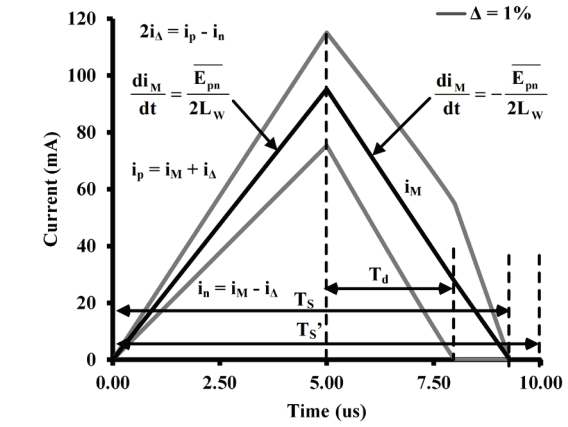
With (5.5), the average of the balancing current can be defined by knowing that the average of a triangular waveform is the peak divided by two, as shown in (5.6) and (5.7). A good design point for choosing the maximum average balancing current is such that the lower winding current is zero, while the upper winding current is twice that of the magnetizing current – a point which occurs when the ratio of the per-unit voltage unbalance, Δ, to the per-unit leakage inductance, L_{pu}, is 1:2. Thus, we can define our ideal maximum average balancing current, as defined in (5.8).

$$\overline{i_\Delta} \approx \frac{I_{BASE}}{4}\left[\frac{\Delta}{L_{pu}}\right]\cdot\left[1+\frac{2T_d}{T_S}\right]\cdot\left[\frac{1}{1+v_D}\right] \tag{5.6}$$

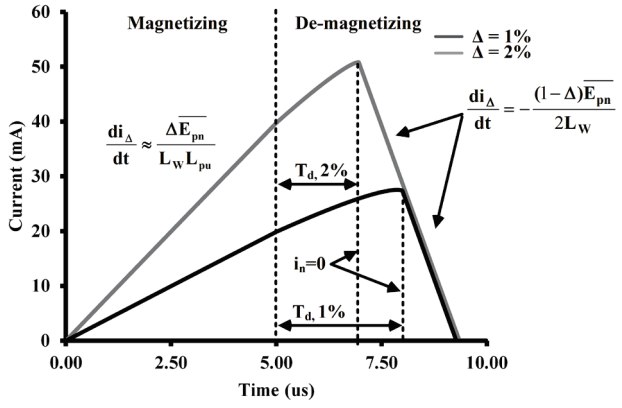
$$\therefore \text{via (4.4)}, \overline{i_\Delta} \approx \frac{I_{BASE}}{2}\left[\frac{\Delta}{L_{pu}}\right]\cdot\left[\frac{1}{1+2\Delta/L_{pu}}\right]\cdot\left[\frac{1}{1+v_D}\right] \tag{5.7}$$

$$\left(\overline{i_\Delta}\right)_{max} = I_{BASE}/8 \text{ for } \Delta/L_{pu} = 0.5 \tag{5.8}$$

The main significance of (5.8) is to provide a relationship between the maximum dc balancing current and the maximum voltage unbalance for a given per-unit leakage inductance. With the maximum voltage unbalance for a given base current, a maximum power can be calculated and used to compare the balancing ability of various commercial transformers. The approximate dc balancing current, as predicted by (5.7), is plotted against a simulation and is found to be in close agreement, as shown in Fig. 5-7. Note that (5.7) does not have any dependence on the switch or diode on-state resistances, due to the relatively small voltage drops produced by the balancing current for the base values of current chosen.



a)



b)

Fig. 5-6. Simulated a) module and magnetization currents for Δ = 1% and b) the intra-bridge balancing current i_Δ with Δ - 1% and 2%. Device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, f_C = 100 kHz, Epn = 4V, I_{BASE} = 400 mA, L_W = 100 μH and L_{pu} =10%.

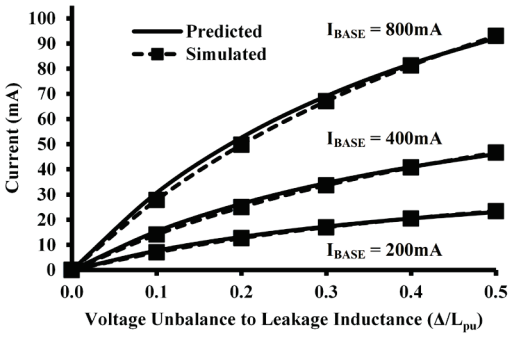


Fig. 5-7. Predicted and simulated average intra-bridge balancing current from (4.7) against the per-unit voltage unbalance to leakage inductance ratio for I_{BASE} = 200, 400 and 800 mA. Device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, Epn = 4V, L_W = 100 μH and L_{pu} =10%. Base currents are obtained with f_C = 200, 100 and 50 kHz.

5.2.2 First Order Approximation of the Device Parameter Effects

While Fig. 5-7 illustrates close agreement with the predicted dc balancing current from (5.7), the magnitude of the base current is relatively low considering the charge capacity of modern lithium polymer batteries (e.g. 20Ah), and the current rating of the MOSFET (6A). In other words, consider that for a modern lithium polymer battery, drawing 20A for an hour will use 100% of capacity. Since the voltage difference between fully charged and discharged in this battery can be 400mV (with a 4V cell) [104], the balancing circuit must use small leakage inductances to allow for large balancing currents with a relatively small per-unit voltage imbalance.

Redrawing Fig. 5-5 a)-c) with the diode voltage drops and device conduction resistances produces Fig. 5-8 a)-c). Clearly, as the intra-bridge balancing current increases in magnitude, the voltage drop across the parasitic resistances will similarly increase. As this parasitic voltage drop can alter the net voltage exciting the leakage inductance, the net balancing current can decrease. Thus, to predict the average intra-bridge balancing current at larger magnitudes of balancing current, some account of the device parameters must be considered. Since the per-unit intra-bridge voltage unbalance will effectively change during the magnetization and de-magnetization periods, a first order approximation of the voltage drops experienced across each parasitic device resistance is made to improve the prediction accuracy of the balancing current made in (5.7).

Consider the slope of the intra-bridge balancing current, with respect to time, for Fig. 5-6 b) during the magnetization period (T_S/2), with the model given in Fig. 5-8 c) to

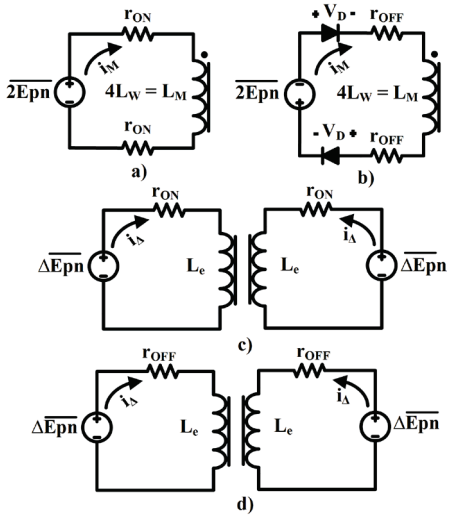


Fig. 5-8. Approximate parasitic equivalent circuits with magnetizing current paths for a) positive excitation and b) negative excitation with the differential current, i_Δ, equivalent circuit during c) the switch conduction time and d) the diode conduction time

account for the voltage drop across the series resistance, V_{ON}, as per (5.9). Although (5.9) is a solvable first-order differential equation, a first order approximation of the effect of device resistances is found to be adequate for transformer sizing requirements. Consider then the peak of the balancing current, as in (5.10), and the approximate device voltage drop across the switch, as one-half this peak balancing current multiplied by the on-state resistance, as in (5.11). Note that the on-state resistance of the windings can also be incorporated into r_{ON}, as per (5.11). By separating out the peak balancing current, as in (5.12) and (5.13), the on-state per-unit voltage unbalance is defined in (5.14).

$$\frac{di_\Delta}{dt} = \frac{\Delta\overline{Epn} - V_{ON}}{L_W L_{PU}}, \quad V_{ON} = i_\Delta r_{ON} \tag{5.9}$$

$$i_{\Delta,peak} \approx \left[\frac{\Delta\overline{Epn} - V_{ON}}{L_W L_{PU}}\right] \cdot \frac{T_S}{2} \tag{5.10}$$

$$V_{ON} = i_\Delta r_{ON} \approx \frac{i_{\Delta,peak} r_{ON}}{2} \tag{5.11}$$

$$\Rightarrow i_{\Delta,peak} \approx \left[\frac{\Delta\overline{Epn}}{L_W L_{PU}}\right] \cdot \frac{T_S}{2} - \left[\frac{i_{\Delta,peak} r_{ON}}{2L_W L_{PU}}\right] \frac{T_S}{2} \tag{5.12}$$

$$\Rightarrow \quad i_{\Delta,peak}\left(1 + \frac{r_{ON}}{4L_W L_{PU} f_S}\right) \approx \frac{\Delta\overline{Epn}}{2L_W L_{PU} f_S} \tag{5.13}$$

$$\therefore \quad \Delta_{ON} \approx \frac{\Delta}{(1 + r_{ON} / 4L_W L_{PU} f_S)} \tag{5.14}$$

During the de-magnetization state, recognizing that the series voltage drop, V_{OFF}, subtracts from the intra-bridge differential voltage, as in (5.15) and (5.16), the off-state per-unit voltage unbalance can be expressed in (5.17). For simplicity, assume that time

T_d, is defined as per (5.5), giving leading to (5.17) via the same development as in (5-12) to (5-14).

$$i_{\Delta,peak} \approx \left[\frac{\Delta\overline{Epn} - V_{OFF}}{L_W L_{pu}}\right] \cdot T_d \tag{5.15}$$

$$V_{OFF} = i_\Delta r_{OFF} \approx \frac{i_{\Delta,peak} r_{OFF}}{2} \tag{5.16}$$

$$\therefore \quad \Delta_{OFF} \approx \frac{\Delta}{1 + \frac{r_{OFF}}{4 L_W L_{pu} f_C}\left[\frac{1 - 2\Delta / L_{pu}}{1 + 2\Delta / L_{pu}}\right]} \tag{5.17}$$

With the equivalent on and off state per-unit voltage unbalances developed, as per (5.14) and (5-17), the average balancing current can be derived, taking into account the series parasitic device resistances. Using the same logic as in (5.5), the time T_d can be altered to include Δ_{ON} and Δ_{OFF}, via (5.18). Then, as three-segments with different areas are produced, the net average over the time T_S can be calculated as per (5.19), leading to the average balancing current in (5.20). Note that as in (5.7), (5.20) is modified by the on-state voltage drops produced by the diodes in the de-magnetization period.

$$T_D = \frac{T_S}{2} \cdot \frac{1 - 2\Delta_{ON} / L_{PU}}{1 + 2\Delta_{OFF} / L_{PU}} \tag{5.18}$$

$$\overline{i_\Delta} = \frac{T_S/2}{T_S}\frac{(i_{\Delta,peak@T_S/2})}{2} + \frac{T_D}{T_S}\frac{(i_{\Delta,peak@T_D} - i_{\Delta,peak@T_S/2})}{2} + \frac{T_D}{T_S}\left(i_{\Delta,peak@T_S/2}\right) + \frac{T_S - T_D - T_S/2}{T_S}\frac{(i_{\Delta,peak@T_D})}{2} \tag{5.19}$$

$$\therefore \overline{i_\Delta} = \frac{I_{BASE}}{4}\left[\frac{\Delta_{ON}}{L_{pu}}\left(1 + \frac{T_d}{T_S}\right) + \frac{\Delta_{OFF}}{L_{PU}}\left(\frac{T_d}{T_S}\right)\right] \cdot \left[\frac{1}{1 + v_D}\right] \tag{5.20}$$

With device parameters r_{ON}=30mΩ, r_{OFF}=55mΩ, V_D=0.34V and with I_{BASE} = 4A and 8A, a simulation and the predictions from (5.20) are illustrated in Fig. 5-9, along with the predictions from (5.7).

In Fig. 5-9, the predictions of the average balancing current closely matches the average current measurements obtained from simulation. While the biggest point of error is when the ratio of Δ/L_{pu} is 0.5, the remaining points are within 5% of the simulated current measurements, compared to 20% error obtained by ignoring device parameters. Therefore, the first order approximation is justified, as it improves the accuracy of the predicted currents sufficiently for design purposes.

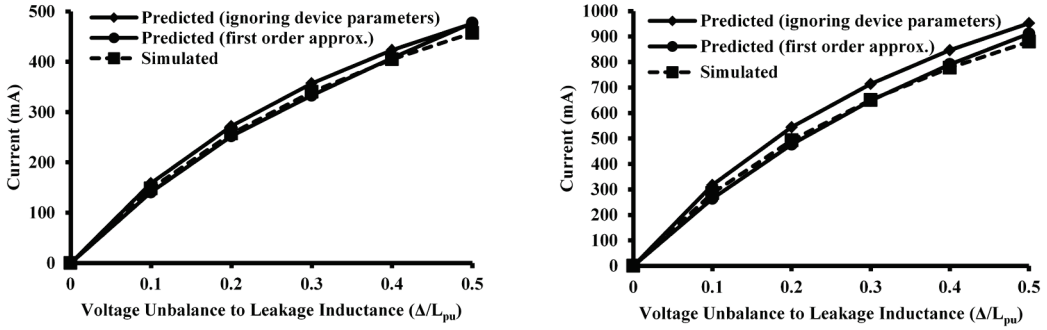


Fig. 5-9. Average intra-bridge average current: using (5.7), (5.20) and values from simulation for a) I_{BASE} = 4A, and b) I_{BASE} = 8A. Simulated device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, Epn = 4V, L_W = 5 µH and L_{pu} =10%. Base currents obtained with f_C = 100 kHz and 50 kHz.

5.2.3 Resultant Voltage Balancing

With the single MBB, as depicted in Fig. 5-4, 1 mF capacitors are used to simulate batteries to reduce simulation time. Fig. 5-10 illustrates the intra-bridge balancing operation with an initial per-unit imbalance of Δ = 4%, I_{BASE} = 800 mA, E_{BASE} = 4V, L_W = 50 µH, L_{pu} = 10% and f_C = 50 kHz. In Fig. 5-10, the capacitor voltage, without any closed loop control, naturally converges to the average voltage of 4V. In this manner, the 'automatic' or 'natural' balancing ability of the MBB is able to compensate for internal voltage imbalances, regardless of the type of voltage source.

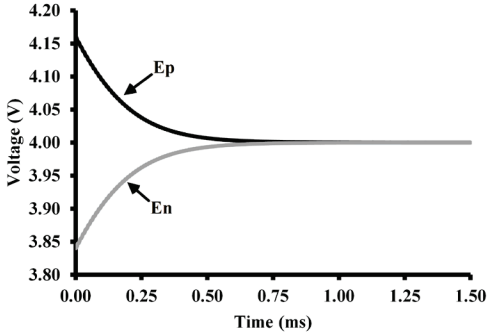


Fig. 5-10. Simulated intra-bridge voltage balancing of a pair of 1 mF capacitors with Δ = 4%. Simulated device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, f_C = 50 kHz, Epn = 4V, I_{BASE} = 800 mA, L_W = 50 µH and L_{pu} =10%.

5.3 Inter-Bridge Voltage Balancing

While the intra-bridge voltages refers to the voltages internal to the MBB, this section details the operation of the series connected MBBs, in order to balance an entire

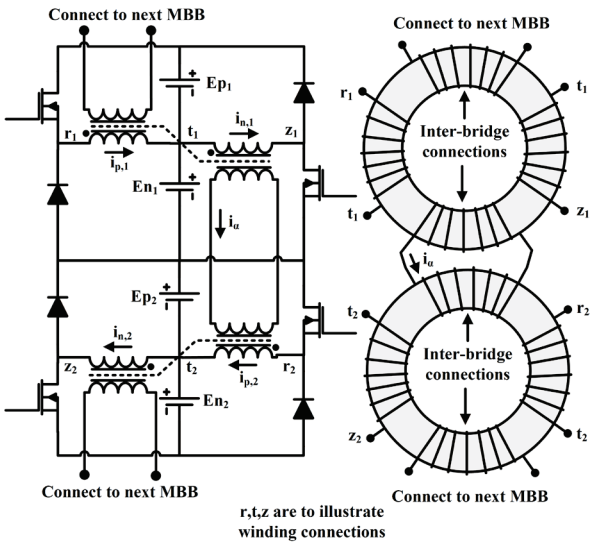


Fig. 5-10. Topological configuration of two cascaded MBBs with two four-winding toroids to illustrate the inter-bridge winding connection to adjacent MBBs

battery string. Instead of using two internal windings, as for Section 5.2, two inter-bridge windings, from Fig. 5-3 b), cascade the voltage balancing effect through 'N' number of cells with 'N/2' MBBs. Therefore, this section derives the average inter-bridge balancing current as a function of the circuit parameters used in the MBB. The discussion evolves in an identical fashion as Section 5.2, but with a focus on four battery cells (two intra-bridge and two inter-bridge) employed in the balancing operation, i.e. Fig 5-10.

With the inter-bridge windings connected to neighboring MBBs, the unbalance Δ does not impact the inter-bridge voltage balancing, as by definition, the intra-bridge balancing does not magnetize the core. However, before the detailed operation is discussed for this aspect of the balancing operation, it is important to mention the simulation model, as shown in Fig. 5-11. In the simulation model, the general MBB topology is stacked to balance four battery cells, with the same devices as used in Section 5.2. Furthermore, the four-winding coupled inductor is modeled using the same two-winding model as in Section 5.2, but with an ideal 1:1 transformer coupling those two windings to another set of windings for the opposing MBB. This four winding coupled inductor arrangement is depicted in Fig. 5-12.

5.3.1 Basic Operation of the MBB for Unbalanced Inter-bridge Voltages

The average of the two adjacent MBB battery voltages is defined as $\overline{E_{12}}$, as per (5.21), and the inter-bridge voltage unbalance, α, is therefore defined in (5.22). To explain the inter-bridge balancing, the base voltage, E_{BASE}, is set to $\overline{E_{12}}$ - although, this

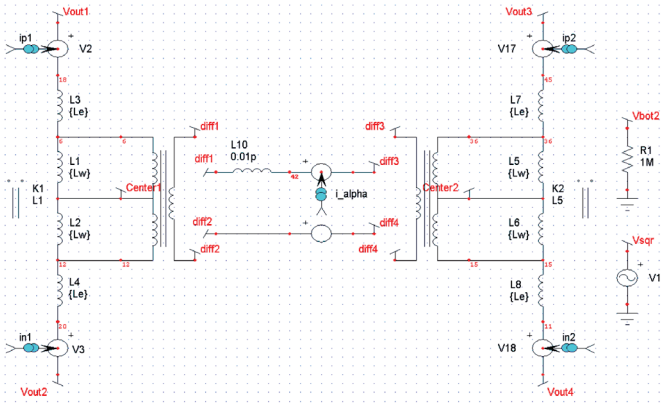


Fig. 5-12. SPICE simulation model of the two cascaded four-winding coupled inductors used in the inter-bridge balancing for the MBBs

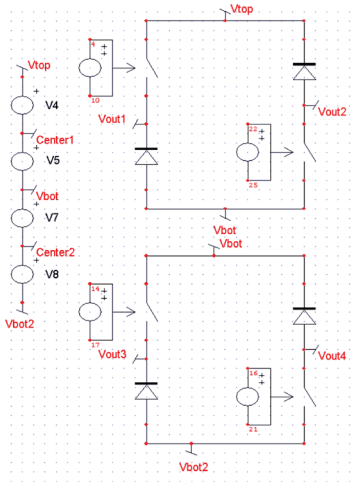


Fig. 5-11. SPICE simulation of the power electronics model for the two MBBs

base voltage should be the same average voltage as $\overline{\text{Epn}}$ (Section 5.2), given that that the base voltage is the battery cell voltage used. Since each adjacent MBB does not share the same magnetic core, i.e. Figs. 5-13 a) and b), the difference in magnetizing voltage causes a net balancing current, i_α in Fig. 5-10, which is limited by the leakage inductance of the two adjacent windings, i.e. $4L_e$, as shown in Fig. 5-13 c).

$$\overline{E_{12}} = \left(\overline{\text{Epn}_1} + \overline{\text{Epn}_2}\right)/2 \tag{5.21}$$

$$\alpha = \left(\overline{\text{Epn}_1} - \overline{\text{Epn}_2}\right)/\left(\overline{\text{Epn}_1} + \overline{\text{Epn}_2}\right) \tag{5.22}$$

The balancing current, i_α, removes charge from the MBB with the higher than average voltage, $\overline{E_{12}}(1+\alpha)$, and places the charge into the MBB with the lower than average voltage, $\overline{E_{12}}(1-\alpha)$, until the per-unit voltage unbalance, α, is reduced to zero. This resultant balancing current is termed the 'inter-bridge balancing current', i_α, and the average of this current is related to the inter-bridge balancing power.

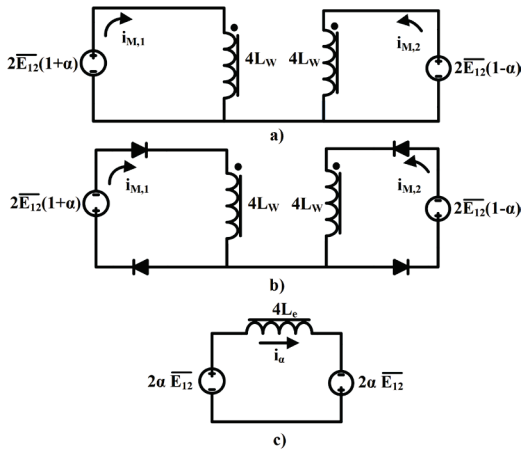


Fig. 5-13. Ideal equivalent circuits for the inter-bridge voltage balancing with magnetizing current illustrated: a) positive excitation and b) negative excitation with c) inter-bridge balancing current

Whereas in the intra-bridge case, the module currents were increased or decreased by an equal and opposite balancing current; in the inter-bridge scenario, this effect is instead present in the 'bridge' currents, i_N, associated with the MBB_N. These currents are the sum of the magnetizing and balancing current, i.e. $i_1 = i_{M,1} + i_\alpha$, and $i_2 = i_{M,2} - i_\alpha$. With this definition in mind, consider Fig. 5-14, which depicts the bridge current with an increasing inter-bridge per-unit voltage unbalance of α = 1%, 2%, and 3% and a per-unit inductance of 10%. Whereas the intra-bridge currents had a period of increasing balancing current after the switches had turned off, this is not the case for the balancing current, as seen in Fig. 5-14. Considering only the balancing current in Fig. 5-15, outside of the on-state diode voltage drop, the magnetization and de-magnetization periods excite the leakage reactance equally.

As in Section 5.2, the average inter-bridge balancing current is a function of the physical parameters of the circuit and the per-unit voltage unbalance, α. Again, using triangular area formulas, the average balancing current over a switching period, T_S, is given in (5.23). The diode voltage drop acts to reduce the duration of balancing, by the per-unit diode voltage drop, as per (5.23). Additionally, as for the intra-bridge case, the ratio of per-unit voltage unbalance to leakage inductance is set to 0.5 (as one bridge current is zero here), giving the ideal maximum dc balancing current, as in (5.24).

$$\overline{i_\alpha} \approx \frac{I_{BASE}}{4}\left[\frac{\alpha}{L_{pu}}\right].\left[\frac{1}{1+v_D}\right] \tag{5.23}$$

$$\left(\overline{i_\alpha}\right)_{max} = I_{BASE}/8 \text{ for } \alpha/L_{pu} = 0.5 \tag{5.24}$$

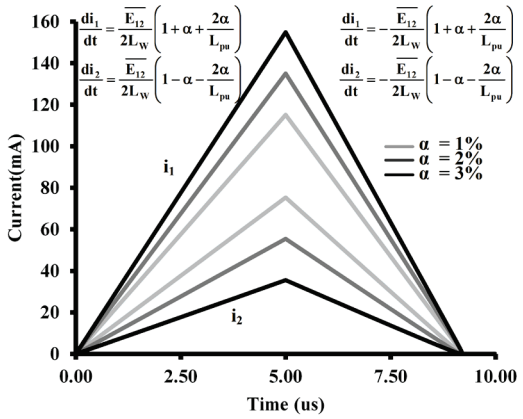


Fig. 5-14. Bridge currents for an inter-bridge unbalance α = 1, 2, and 3% for MBB_1 and MBB_2. r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, f_C = 100 kHz, E_{BASE} = 4V, I_{BASE} = 400 mA, L_W = 100 μH and L_{pu} =10%.

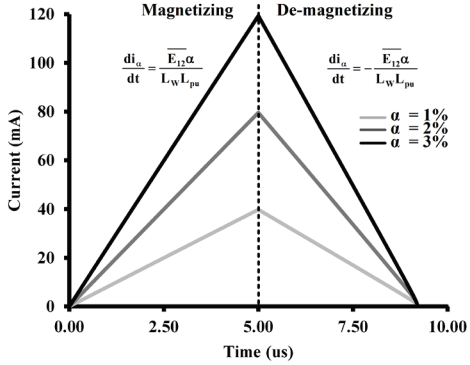


Fig. 5-15. Inter-bridge balancing current, i_α, between MBB1 and MBB2 for an inter-bridge voltage unbalance α = 1, 2, and 3%. r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, I_{BASE} = 400 mA, f_C = 100 kHz, Epn = 4V, L_W = 100 μH and L_{pu} =10%.

As a validation of (5.23), consider the plot of the predicted average balancing current produced by this equation against a simulation, as shown in Fig. 5-16. Like the lower base current value comparison in Section 5.2.1, the inter-bridge predictions are shown to follow closely the simulation, while ignoring the parasitic device resistances. However, due to the increased number of devices, these resistances have a more pronounced impact on the inter-bridge balancing characteristics than for the intra-bridge case. Therefore, while the intra-bridge balancing current had up to a 15% percent gain in accuracy at high base current values, while taking into account the device resistances, Section 5.3.2 shows an even greater impact on the inter-bridge balancing current due to these parasitic effects.

Lastly, the module currents of each respective MBB (i.e. MBB_1 and MBB_2) is shown in Fig. 5-17, with L_{pu} = 10%, α = 1%, Δ_1=Δ_2 = 1%. The average of the module

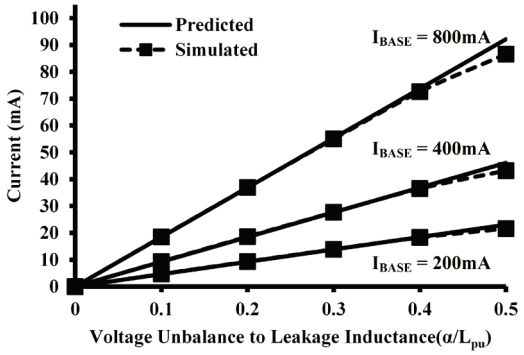


Fig. 5-16. Predicted and simulated average inter-bridge balancing current from (5.23) against the per-unit voltage unbalance to leakage inductance ratio for I_{BASE} = 200, 400 and 800 mA. Device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, E_{12} = 4V, L_W = 100 μH and L_{pu} =10%. Base currents are obtained with f_C = 200, 100 and 50 kHz.

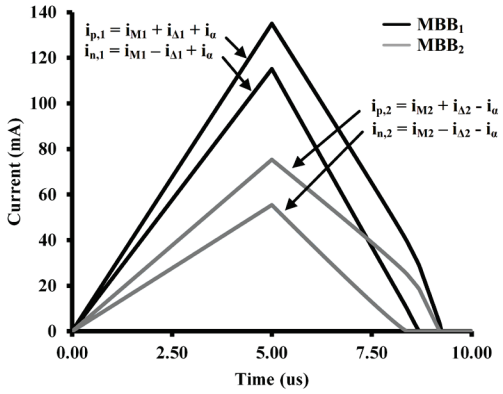


Fig. 5-17. Module currents for MBB_1 and MBB_2 with α = Δ = 1%. Device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, f_C = 100 kHz, Epn = 4V, I_{BASE} = 400 mA, L_W = 100 μH and L_{pu} = 10%.

currents, $(i_p + i_n)/2$, produce the bridge currents for each respective MBB. As the module currents are increased or decreased relative to the average bridge voltage, the intra-bridge unbalance, by definition, is not impacted by these voltage unbalances. However, Fig. 5-17 serves to illustrate that while the balancing parameters are independent of one another, the device current stresses is the result of both intra and inter-bridge voltage unbalances.

5.3.2 First Order Approximation of the Device Parameter Effects

As in the intra-bridge case, for base currents closer to the MOSFET current rating (i.e. where the device voltage drops can be significant), a simple account of the parasitic effects on the balancing performance is necessary. Moreover, it is important to understand how the parasitic device resistances affects the balancing (intra or inter-bridge), as these parameters can vary widely with the selection of devices. Therefore, this

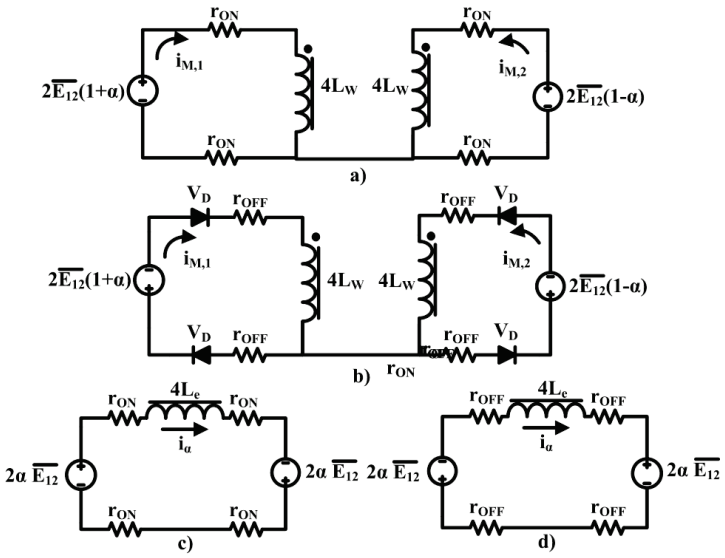


Fig. 5-18. Approximate parasitic equivalent circuits with magnetizing current paths for a) positive excitation and b) negative excitation with the differential current, i_α, equivalent circuit during c) the switch conduction time and d) the diode conduction time

section details the development of the dc inter-bridge balancing current prediction with a simple first order approximation of the device resistances.

By adding the series resistances to the balancing paths for both the magnetization and de-magnetization periods, the equivalent circuit of Fig. 5-13 is reproduced in Fig. 5-18. While the intra-bridge balancing current exist on a per module basis (meaning that $2i_\Delta$ effectively balanced the two batteries), the inter-bridge has only one path from each MBB. Consequently, the number of devices in series with the inter-bridge balancing current is increased when compared to the intra-bridge case, and therefore the effect of the parasitic device resistances is greater on the inter-bridge balancing current.

Fig. 5-18 c) illustrates the equivalent inter-bridge balancing circuit, during the magnetization period, when considering the parasitic device resistances. In the same manner as (5.9) to (5.14), the inter-bridge per-unit voltage unbalance, α_{ON}, can be expressed in (5.25). However, unlike the intra-bridge balancing current, the inter-bridge balancing current does not continue to increase in magnitude after the switch turns off; therefore, during the de-magnetization period, or the diode conduction period, the voltage drop, V_{OFF}, adds to the de-magnetization voltage, as in (5.26). Knowing that the peak balancing current is related to the diode conduction period as in (5.27), the net effect on the inter-bridge per-unit voltage unbalance, α_{OFF}, is given in (5.28).

$$\alpha_{ON} = \alpha \cdot \frac{1}{1 + r_{ON}/4L_W L_{pu} f_C} \tag{5.25}$$

$$\frac{di_\alpha}{dt} = -\left[\frac{\overline{E_{12}} + V_{OFF}}{L_W L_{pu}}\right] \tag{5.26}$$

$$\Rightarrow 0 \approx i_{\alpha,peak} - \left[\frac{\alpha\overline{E_{12}} + V_{OFF}}{L_W L_{pu}}\right]\cdot\frac{T_S}{2} \;\&\; V_{OFF} = \frac{i_{\alpha,peak} r_{OFF}}{2} \tag{5.27}$$

$$\Rightarrow \left[\frac{\alpha\overline{E_{12}}}{L_W L_{pu}}\right]\cdot\frac{T_S}{2} \approx i_{\alpha,peak} - \frac{i_{\alpha,peak} r_{OFF}}{4L_W L_{pu}}$$

$$\Rightarrow \left[\frac{\alpha\overline{E_{12}}}{L_W L_{pu}}\right]\cdot\frac{T_S}{2} \approx i_{\alpha,peak}\left(1 - \frac{r_{OFF}}{4L_W L_{pu}}\right)$$

$$\therefore \quad \alpha_{OFF} \approx \frac{\alpha}{(1 + r_{OFF}/4L_W L_{pu} f_C)} \tag{5.28}$$

However, as the balancing current is affected by the on and off state device resistance paths, key regions are necessary to derive the average of this current. Consider Fig. 5-19 and Fig. 5-20, which illustrate the bridge currents and balancing current waveforms respectively under increasing α, with device parameters: r_{ON} = 30mΩ, r_{OFF} = 55mΩ, and V_D = 0.34V. These waveforms are reproduced under a base current of 8A, rather than 400mA, as in Figs. 5-14 and 15.

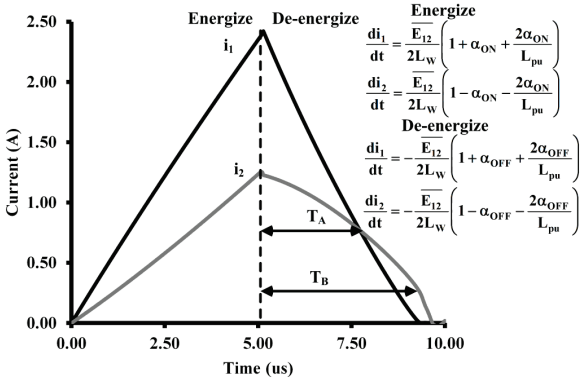


Fig. 5-19. Bridge currents for a voltage unbalance α = 1% for MBB_1 and MBB_2. Device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, f_C = 50 kHz, E_{12} = 4V, I_{BASE} = 8 A, L_W = 5 μH and L_{pu} =10%.

The first point about the influence of the series device resistances is the effect during the diode conduction state. The period marked 'T_A' in Fig. 5-19 marks the point at which the balancing current hits 0A, and the period marked 'T_B' marks the point at which the bridge current hits 0A. Region T_A is the direct result of the mismatch between on and off resistances during each respective conduction period, e.g. the device resistances differ by 30:55mΩ in Fig. 5-19. One significant difference with the inter-bridge balancing current is that this current is bipolar - i.e. negative balancing current can exist. Therefore, due to having bipolar current flow, the mismatch of device resistances

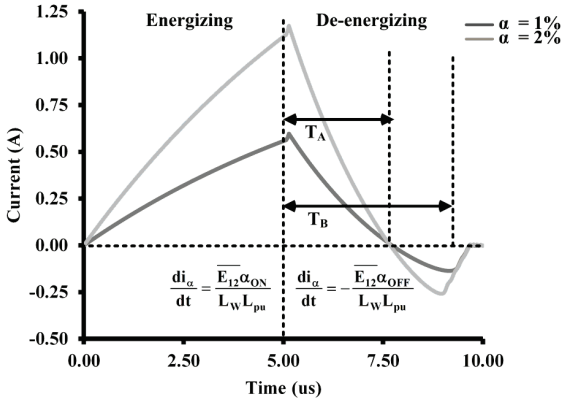


Fig. 5-20. Inter-bridge balancing current, i_α, between MBB_1 and MBB_2 for a voltage imbalance $\alpha = 1$ %. Device parameters: $r_{ON} = 30$ mΩ, $r_{OFF} = 55$mΩ, $V_D = 0.34$V, $I_{BASE} = 8$ A, $f_C = 50$ kHz, $E_{12} = 4$V, $L_W = 5$ µH and L_{pu} =10%.

can cause the inter-bridge balancing currents to reverse, as clearly possibly on examination of the equivalent circuit in Fig. 5-18 c) and d). This subtracts from the net inter-bridge balancing current, and increases until one of the bridge currents hits zero, i.e. time T_B.

Therefore, from Figs. 5-19 and 5-20, because of the effect of device resistances, conduction periods, T_A and T_B, must be taken into account for the average balancing current derivation. To simplify the equations, let 'a' and 'b' be the co-efficient that scale $T_S/2$ to each conduction period, T_A and T_B.

$$\begin{aligned}
&\frac{di_{\alpha(ON)}}{dt}\cdot\frac{T_S}{2}-\frac{di_{\alpha(OFF)}}{dt}\cdot T_A=0\\
&\frac{\alpha_{ON}\overline{E_{12}}}{L_W L_{pu}}\cdot\frac{T_S}{2}=\frac{\alpha_{OFF}\overline{E_{12}}}{L_W L_{pu}}\cdot T_A\\
&\therefore\quad T_A=\frac{\alpha_{ON}}{\alpha_{OFF}}\cdot\frac{T_S}{2}=a\cdot\frac{T_S}{2}
\end{aligned}\tag{5.29}$$

$$\begin{aligned}
&\frac{di_{2(ON)}}{dt}\cdot\frac{T_S}{2}-\frac{di_{2(OFF)}}{dt}\cdot T_B=0\\
&\frac{\overline{E_{12}}}{L_W}\cdot\frac{T_S}{2}\left(1+\alpha_{ON}+\frac{2\alpha_{ON}}{L_{pu}}\right)=\frac{\overline{E_{12}}}{L_W}\cdot T_B\left(1+\alpha_{OFF}+\frac{2\alpha_{OFF}}{L_{pu}}\right)\\
&\therefore\quad T_B=\frac{(1+\alpha_{ON}+2\alpha_{ON}/L_{pu})}{(1+\alpha_{OFF}+2\alpha_{OFF}/L_{pu})}\cdot\frac{T_S}{2}=b\cdot\frac{T_S}{2}
\end{aligned}\tag{5.30}$$

With T_A and T_B, along with the on and off time per-unit inter-bridge voltage unbalance, the average balancing current can be derived as the sum of the average waveform over the periods: 0 to $T_S/2$, $T_S/2$ to T_A, T_A to T_B, and T_B to T_S, as per (5.31).

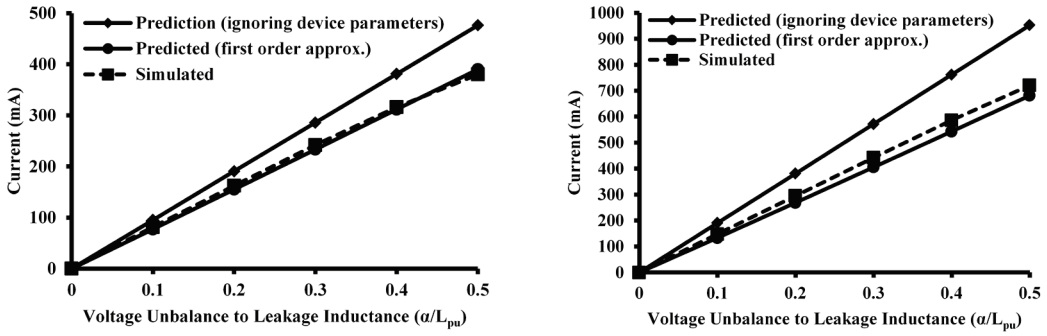
$$\overline{i_\Delta} = \frac{T_S/2}{T_S}\frac{(i_{\alpha,peak@T_S/2})}{2} + \frac{T_A}{T_S}\frac{(i_{\alpha,peak@T_S/2})}{2} + \frac{T_B - T_A}{T_S}\frac{(i_{\alpha,peak@T_B})}{2} + \frac{T_S - T_B}{T_S}\frac{(i_{\alpha,peak@T_B})}{2}$$

$$\overline{i_\Delta} = \frac{1}{2}\frac{(i_{\alpha,peak@T_S/2})}{2} + \frac{a}{2}\frac{(i_{\alpha,peak@T_S/2})}{2} + \frac{(b-a)}{2}\frac{(i_{\alpha,peak@T_B})}{2} + \frac{(1-b)}{2}\frac{(i_{\alpha,peak@T_B})}{2}$$

$$i_{\alpha,peak@T_S/2} = \frac{I_{BASE}}{2}\cdot\left[\frac{\alpha_{ON}}{L_{pu}}\right] \quad \& \; i_{\alpha,peak@T_B} = -\frac{I_{BASE}}{2}\cdot\left[\frac{\alpha_{OFF}}{L_{pu}}\right](b-a)$$

$$\therefore \quad \overline{i_\alpha} = \frac{I_{BASE}}{8}\left(\frac{\alpha_{ON}}{L_{PU}}(1+a) - \frac{\alpha_{OFF}}{L_{PU}}(b-a)(1-a)\right)\cdot\left[\frac{1}{1+v_D}\right] \tag{5.31}$$

With device parameters r_{ON}=30mΩ, r_{OFF}=55mΩ,V_D=0.34V and with I_{BASE} = 4A and 8A, a simulation and the predictions from (5.31) are illustrated in Fig. 5-21, along with the predictions from (5.23). In the case of the 4A base current case, Fig, 5-21 a), the first order approximation drops the error from a high of 30% down to 4.5%, and 33% compared to 7.5% for the 8A base current test case in Fig. 5-21 b).



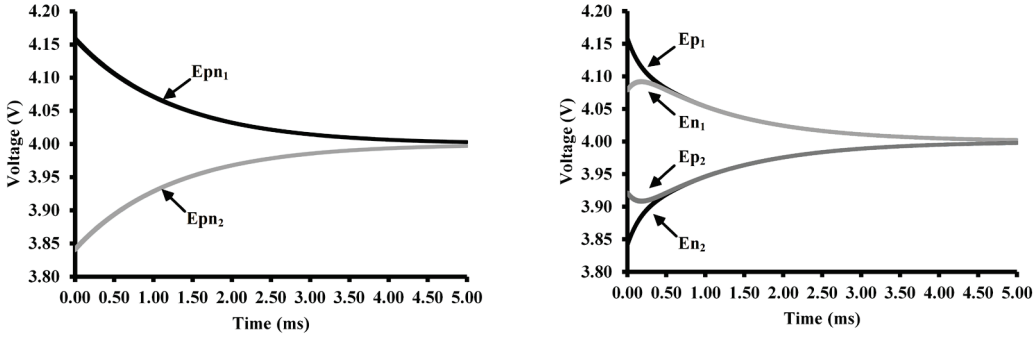
a) b)

Fig. 5-21. Average inter-bridge average current: predicted using (5.23), predicted using (5.31) and simulated values for a) I_{BASE} = 4A, and b) I_{BASE} = 8A. Simulated device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, T_S = 10 μs, Epn = 4V, L_W = 5 μH and L_{pu} =10%. Base current values are obtained for f_C = 100 kHz in a) and 50 kHz in b).

5.3.3 Resultant Voltage Balancing

With the two MBB units cascaded, as per Fig. 5-10, 1 mF capacitors were used to simulate batteries with an initial per-unit inter-bridge voltage unbalance of 4%, as per Fig. 5-22 a). These results are achieved with I_{BASE} = 800 mA, E_{BASE} = 4V, L_W = 50 μH, L_{pu} = 10% and f_C = 50 kHz. Like the intra-bridge voltage balancing case, the unbalance converges to zero. However, when compared to Fig. 5-9, the inter-bridge balancing is slower, due to having only one balancing current path (compared to two for the intra-

bridge circuit). With the same circuit parameters, this point can be further emphasized by considering the balancing rates with α = 4%, and Δ = 2%, as in Fig 5-22 b).



a) b)

Fig. 5-22. Simulated inter-bridge voltage balancing of four 1 mF capacitors with a) α= 4% and b) α = 4% and Δ = 2%. Simulated device parameters: r_{ON} = 30 mΩ, r_{OFF} = 55mΩ, V_D = 0.34V, f_C = 50 kHz, E_{12} = 4V, I_{BASE} = 800 mA, L_W = 50 μH and L_{pu} =10%.

5.4 Peak Balancing Power versus Transformer Size

In this section, the balancing power of the MBB is estimated and an approach to the sizing of a commercial transformer is presented. As the MBB is intended to be a modular, low-cost solution, a commercial transformer is selected and the minimum switching frequency for each transformer is calculated to achieve the maximum balancing power. With the commercial transformer selected, an estimate of the power density of the MBB is obtained against available transformers in the same series.

The net result of the discussion presented in Sections 5.2 and 5.3 is the development of an average balancing current expression, for both the intra-bridge and inter-bridge balancing behaviors. The ratio of the per-unit leakage inductance to the per-unit voltage imbalances sets a maximum limit for the average balancing current that can flow, which is proportional to the base current, I_{BASE}. With a given transformer and winding inductance, the maximum rms current and the peak magnetizing current is calculated. Since the inter-bridge voltage unbalance affects the magnetizing current, the peak magnetizing current is obtained using the bridge current slopes of Fig. 5-14 giving (5.32). When the ratio of per-unit leakage inductance to voltage imbalance is 1:2, one module current is essentially zero and the other is twice the magnetizing current. With the magnetizing current given in (5.32), the maximum rms module current can be calculated as in (5.33).

$$\hat{i}_M \approx \frac{I_{BASE}}{4}(1+\alpha) \tag{5.32}$$

$$i_{p,RMS} \approx \frac{I_{BASE}}{2\sqrt{2}}(1+\alpha) \tag{5.33}$$

Thus, with the use of (5.32) and (5.33), key device ratings can be calculated for the selection of the transformer and power electronics.

One of the primary benefits of the MBB is that it does not require custom designed transformers, which depend on the number of battery cells used in the system. Therefore, a six-winding transformer ('hexapath') with a 1:1 ratio for each winding, is selected from Coilcraft [105]. Using this line of transformers, with two windings connected in parallel for the intra-bridge connections (to increase the total current capability), and using (5.32) and (5.33), the circuit parameters are iteratively modified to keep within rated thermal limits. With a cell voltage of 4V, the remaining manipulated variable is the switching frequency. Therefore, while a low switching frequency maximizes the balancing capability, the switching frequency must increase to keep below rated copper losses and saturation values. To illustrate this, the 'HP' line from the 'hexapath' series from Coilcraft is selected - with six core sizes and five different air-gap lengths. With the switching frequency and magnetizing inductance given by the inductor selected, $\Delta = \alpha = 5\%$, and $L_{pu} = 10\%$ in (5.8), (5.23), (5.32) and (5.33), with $E_{BASE} = 4V$, the peak balancing power can be determined in (5.34).

$$P_{MAX} = 2E_{BASE}\left(\overline{i_\varepsilon}\right)_{max}, \text{where} \varepsilon = \alpha \text{ or } \Delta \tag{5.34}$$

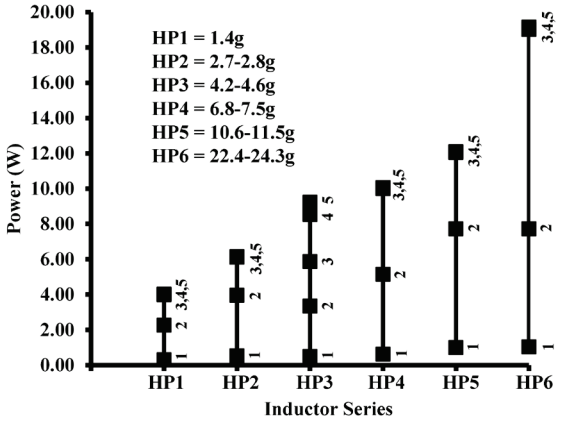


Fig. 5-23. Commercially available "hexa-path" inductors from Coilcraft [105] with peak balancing power and inductor weight shown as a function of balancing currents, i_α and i_Δ. $\Delta = \alpha = 5\%$, $L_{pu} = 10\%$. Ideal devices assumed, and power is obtained at the switches frequencies in Fig. 5-24.

In Table 5-1, with the 'HP2' series selected, the winding inductances, weight and specific current limits are illustrated. With the series HP1 to HP6, a peak power-

balancing graph is produced, as per Fig. 5-23, and the switching frequency required to obtain each power level illustrated in Fig. 5-24.

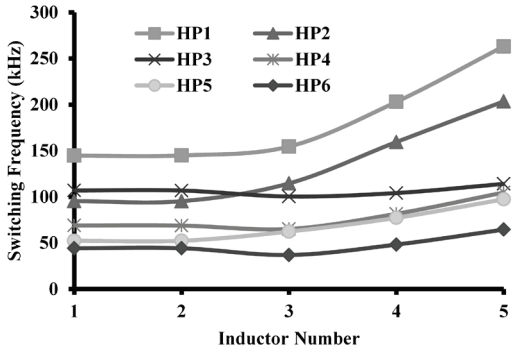


Fig. 5-24. Commercially available hexa-path inductors from Coilcraft [105] with corresponding switching frequency required to obtain the peak power illustrated in Fig. 5-23 for each inductor. $\Delta = \alpha = 5\%$, $L_{pu} = 10\%$. Ideal devices are assumed.

Inductor Number	**1**	**2**	**3**	**4**	**5**
Name	1600L	0216L	0116L	0083L	0066L
L_W (µH)	78.4	10.6	5.7	4.1	3.2
I_{SAT} (A)	-	0.770	1.60	2.10	2.50
I_{RMS} (A)	1.13	1.13	1.13	1.13	1.13
Weight (g)	2.75	2.75	2.75	2.75	2.75

Table 5-1. HP2 Series six-winding coupled inductor from Coilcraft [105]

Note that the 'inductor number' of Fig. 5-23 and 5-24 refers to the number within a given series, and compares the ideal power for each transformer size. Note also that the inductor number 1 in each series has no air-gap (and therefore no energy storage), which explains the relatively low balancing power. Using the weight of each transformer, the ideal power density (e.g. W/g) of the MBB, is capable of just under 3.5W/g.

Fig. 5-24 illustrates the required switching frequency from the power electronics to achieve the balancing power of Fig. 5-23. This figure is an important dimension to the power capability of the transformers HP1 and HP2 - as these transformers are the lightest, with the highest power density. However, from Fig. 5-24, it is clear that a significantly higher switching frequency is necessary for the higher inductor numbers compared to the other lines.

5.5 Practical Device Switching Issues

Since the automatic voltage balancing operation relies on the synchronized excitation of each four winding coupled inductor, this section details the

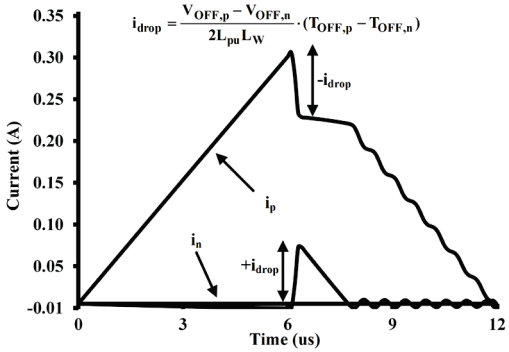


Fig. 5-25. The effect of a non-linear C_{DG} (simulated via external capacitor) on the module currents of a single MBB with $\Delta = 5\%$. $f_C = 95$ kHz, $L_W = 78.6\mu H$, $E_{12} = 4V$ and $L_{pu} = 10\%$.

non-ideal switching behavior, and its influence on the balancing behavior. Therefore, the goal of this section is to allow the designer additional considerations when selecting the power electronic components.

One non-ideal effect is the control signal delay that can exist between the gating signals of the MBBs. Essentially, this time difference causes one switch to turn off earlier, and since this is not common in both windings, a differential voltage is created across the leakage reactance of the transformer. This in turn negates the balancing current, as depicted in Fig. 5-25, shown as 'i_{drop}'. However, even with synchronized switching, a delay difference can still occur due to improper device selection. Since the MBB is a discontinuous conduction converter, the turn on current magnitude is zero. During the turn-off time though, the device sees the full module current.

With a FET device, the turn-off time is related to the charging of a capacitor, C_{GD} (realistically C_{GD}+C_{DS} [94]), as shown in Fig. 5-26 c). The voltage across C_{GD} is essentially zero when the switch is on, but charges to the blocking voltage during switch off. However, the device capacitances for a MOSFET device can be non-linear with the blocking voltage [94]. As an example, consider two device capacitance curves of two commercial MOSFETs in Figs. 5-26 a) and b). If a pair of MBB MOSFETs is blocking 8.16V and the other pair is blocking 7.84V (i.e. $\alpha = 2\%$, for $E_{BASE} = 4V$), and if the switch utilized is from Fig. 5-26 a), C_{GD} can vary from 45pF to 55pF. With each pair of devices having a slightly different C_{GD}, they will exhibit slightly different turn off times. However, if the switch selected is from Fig. 5-26 b), where C_{GD} is approximately linear in the operating range, then the two MBBs will switch in synchronism - maximizing the balancing power. Therefore, the selected power electronics should be selected to operating in a linear region of its device capacitances versus blocking voltage, i.e. close to the device's rated voltage.

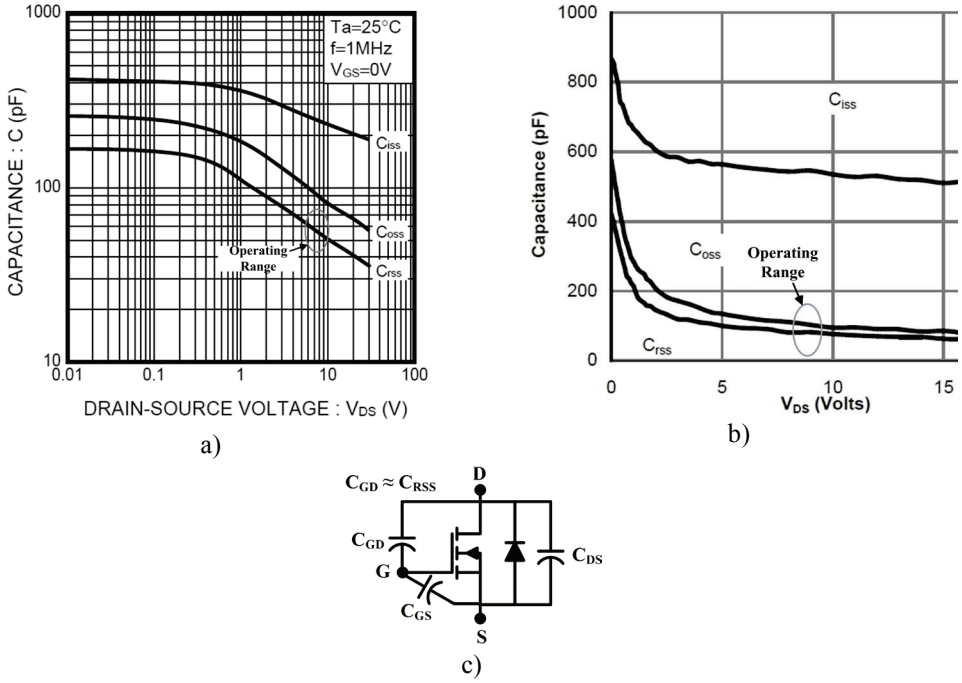


Fig. 5-26. Device blocking voltage V_{DS} versus device capacitances for two example devices: a) 30V, 5A MOSFET [106] and b) 20V, 6A MOSFET [107]. Device capacitances for MOSFETs are illustrated in c).

5.6 Experimental Setup

In order to validate conclusions made via simulation and demonstrate the MBB operation, an experimental prototype consisting of two MBBs is constructed, as in Fig. 5-27. Two HP2-0216L "hexa-path" inductors were selected as each MBB's coupled inductor, giving L_W = 10.6 µH and $L_{pu} \approx 1\%$. Each MBB had two filter inductors (L = 1.6µH) to limit the effects of switching mismatch, raising the total $L_{pu} \approx 15\%$. Additionally, to illustrate how the parasitic resistive effects can impact the balancing current, two HP2-0116L coupled inductors were also used with the parameters: L_W = 5.6 µH, and L_{pu} is designed to be 5%.

Four 20V, 5A MOSFET modules (AO3420) [107] were driven at a 50% duty cycle, from a Texas Instruments F2812 DSP unit at a switching frequency of 100 kHz for the HP2-0216L results (L_W = 10.6 µH) and 95 kHz for the HP2-0116L results. The MOSFET modules were chosen due to the operational parameters and relatively their linear device capacitances around the balancing range of the circuit. Note the device parameters for the circuit: V_D = 0.3V (schottky diodes), r_{OFF} = 60 mΩ and r_{ON} = 30 mΩ (with 10 mΩ attributed to winding/miscellaneous resistances).

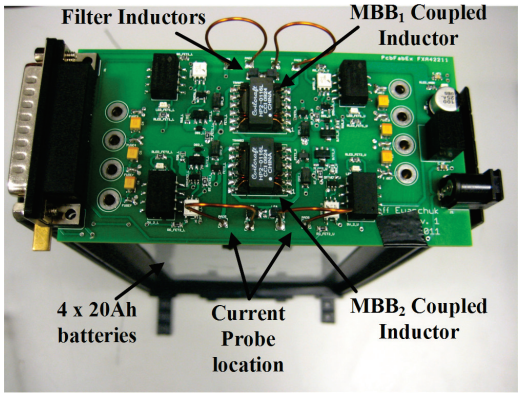


Fig. 5-27. Experimental prototype shown with four 20Ah batteries and two HP2-0116L 'hexa-winding' transformers

To demonstrate the experimental winding currents, and draw conclusions about the bridge currents, four 1mF capacitors were loaded with resistors to allow for quick manipulation of α and Δ. However, as the circuit is intended for battery operation, a prototype, Fig. 5-27, is designed around four 20Ah Li-polymer batteries ePLB-C020, from EIG [104], and the balancing operation is demonstrated using two coupled inductors with an order of magnitude difference in inductance: HP2-1600L (L_W = 78.4 μH) and the HP2-0116L (L_W = 6.8 μH). This was intended to emphasize the difference in balancing power, and both units are designed with L_{pu} = 5% in this scenario.

5.7 Experimental Results

In the experimental results, three main categories are discussed. One is the accuracy of the simulation tools relative to the measured experimental results. This is an important consideration, as the predictions from Sections 5.2 and 5.3 are verified against the simulated results. Another subject is the effect of the parasitic resistance on the balancing of the circuit. With the presented results, two test cases are given: one with little to no apparent effect of the device resistances and another with a very apparent effect on the device resistances. Finally, the MBB will be used to balance four batteries that have a inter-bridge voltage unbalance. The main point from this result is the difference between the selected coupled inductors and their effect on the balancing time of the 20Ah batteries.

The module currents, within the two MBBs, are presented for the simulated and experimental results given the high L_{pu} scenario, and the HP2-0216L inductor in Fig. 5-28 a) and b) respectively. Conversely, with the same devices, but differing L_{pu} and using the HP2-0116L inductor, the simulated and experimental results are shown for the

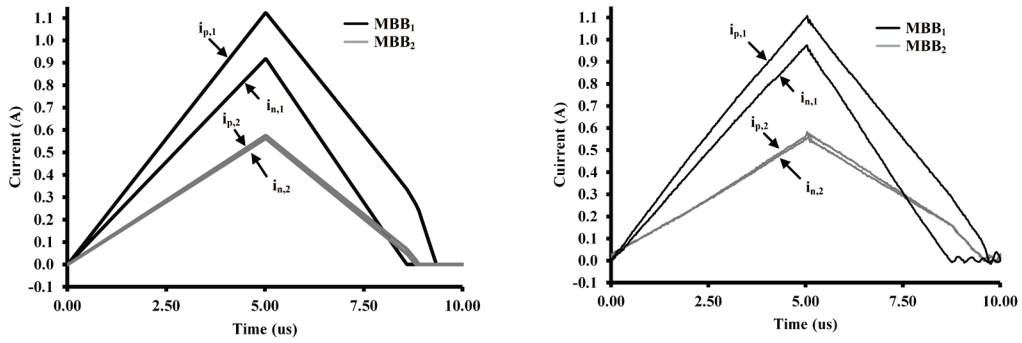
simulated and experimental results in Fig. 5-29 a) and b). These two figures illustrate the effect when the device voltage drop across the parasitic resistance in Fig. 5-28 is small, compared to a large device voltage drop, as shown in Fig. 5-29. This result is further emphasised in the bridge currents, taken with varying α, for both inductors in Fig. 5-30. Finally, the average battery voltage versus time is given in Fig. 5-31 for the lowest balancing power inductor in the HP2 line (the gap-less HP2-1600L), and the HP2-0116L.

5.8 Discussion

The module currents displayed in Figs. 5-28 and 5-29 closely match the experimental with the simulated values. However, for the case with the 5% leakage inductance, Fig. 5-29, more differences exist due to the simulated switch model and estimation of winding resistances. Furthermore, while the peak module currents are matched quite well between the simulated and experimental results, the diode conduction periods differ in terms of slope. This can be attributed to differences in the simulated diode module during the switch turn off time, compared to the actual experimental results. However, the 'rounded' waveform characteristic of the low per-unit inductance case clearly suggests the influence of device resistances, and this result is present in both the simulated and experimental cases.

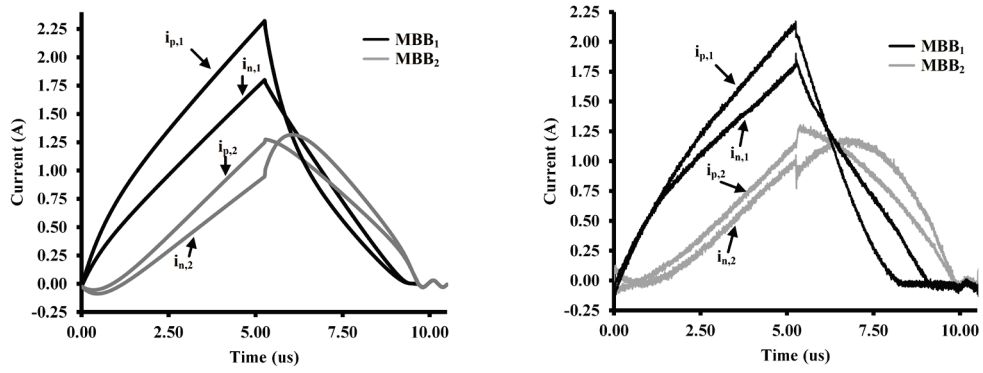
The bridge currents also emphasize the effects of device resistance. With a low per-unit leakage inductance, more balancing current flows for a given base current. With the device parameters given, the expected time period T_A is roughly 1.6 μs (approximate as the low L_{pu} case uses 95 kHz switching frequency) and 4.32 μs. The measured period T_A is roughly 1.25 μs for the low L_{pu} case and approximately 4 μs for the high L_{pu} case, confirming that the first order approximation is sufficient for design purposes. The predicted average inter-bridge balancing currents for the 2% cases are 243mA and 111mA. The actual measured average currents are 258mA and 120mA, or 6% and 7.5% error respectively. If the device resistances are ignored in the predictions, the currents are predicted to be 726mA and 117mA or 181% and 2.5% error respectively. Clearly, ignoring the device resistances will severally underestimate the inter-bridge balancing current.

Fig. 5-31 illustrates the balancing of four battery cells over time with two different inductors. It is clear from the trend line of the HP2-1600L inductor that, while



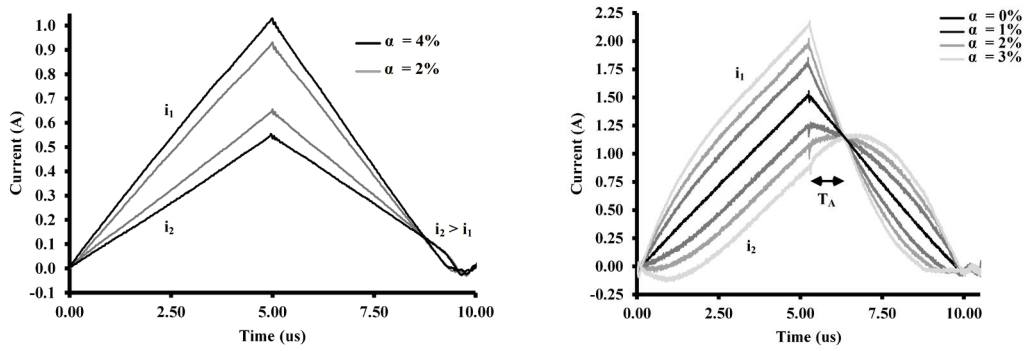
a) b)

Fig. 5-28. Module currents a) simulated versus b) experimental for MBB_1 and MBB_2 when α = 4.25%, Δ_1 = 2.4%, Δ_2=0.30%. Simulated device parameters: E_{12}=4V, f_C = 100 kHz, L_{pu} = 15% and L_W = 10.6 µH, V_D = 0.3V, r_{OFF} = 60 mΩ and r_{ON} = 30 mΩ



a) b)

Fig. 5-29. Module currents: a) simulated versus b) experimental for MBB_1 and MBB_2 when α = 1.81%, Δ_1 = 0.73%, Δ_2=0.89%. Simulated device parameters: E_{12}=4V, f_C = 95 kHz, L_{pu} = 5% and L_W = 5.6 µH, V_D = 0.3V, r_{OFF} = 60 mΩ and r_{ON} = 30 mΩ



a) b)

Fig. 5-30. Experimental bridge currents for MBB_1 and MBB_2: a) α = 2 and 4% with L_{pu} = 15%, L_W = 10.6 µH and f_C = 100 kHz, b) α = 1, 2 and 3% with L_{pu} = 5%, L_W = 5.6 µH, and f_C = 95 kHz. Simulated device parameters: E_{12}=4V, V_D = 0.3V, r_{OFF} = 60 mΩ and r_{ON} = 30 mΩ

balancing occurs, the total balancing time would take several days at the given rate. Replacing the HP2-1600L with the HP2-0116L inductor significantly increases the balancing power, and this is evident in Fig. 5-31. Note that the steady state value would be 3.84V (assuming no losses), and the initial α is 2.6%. While this might seem small, the operating range of the battery is 4.0V to 3.6V. Therefore, the initial unbalance represents nearly 50% of the total operational region of the batteries, and it is unlikely that the circuit would experience this magnitude of unbalance in practice.

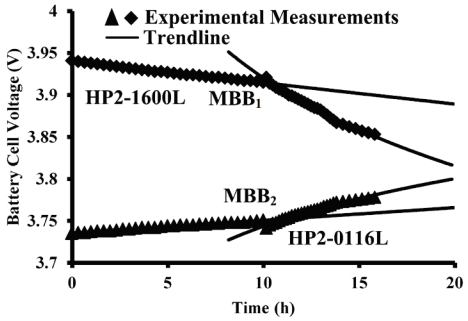


Fig. 5-31. MBB_1 and MBB_2 battery cell voltages against time (in hours) with an initial unbalance of $\alpha = 1\%$ using two 'hexa-path' transformers: HP2-1600L ($L_W = 78.6$ μH) and HP2-0116L ($L_W = 5.6$ μH) design with $L_{pu} = 5\%$ and $f_C = 95$ kHz.

5.9 Chapter Summary

A modular converter is presented that uses the natural leakage inductance of a four-winding coupled inductor to automatically control the voltage balancing of serially connected batteries. Although chosen for the presentation simplicity of using four battery cells, this circuit is intended for large battery strings, as present in modern transportation applications. This chapter demonstrated the size requirements versus the average balancing power, practical design details that limit the balancing rate and the effect of component values on the balancing power. This balancing action allows for minimized control hardware, and coupled with the modular nature of the converter system, cost effectiveness for traditionally costly non-dissipative balancing systems.

Chapter 6 - Conclusions and Future Work

The research contributions described in this thesis were in both theoretical and experimental. The suggestions for future work extends on two possible themes: possible improvements in the modulation schemes that eliminate the common mode voltages in coupled inductor converters, and improving the modular balancing bridge for balancing speed at smaller voltage differences.

6.1 Summary of Contributions

The contributions made in this thesis can be summarized as follows:

- Identification of non-zero common mode winding states that exist when a three-limb coupled inductor is used in a three-phase coupled inductor converter.
- Presentation of a carrier-based modulation technique for the SS-CIC to highlight the challenges involved in the elimination of these common mode winding voltages.
- Experimental development of a 60 kW, dual six-switch converter system. This system was used to illustrate the common mode winding voltages present in traditional modulation schemes and their resultant common mode currents.
- Experimental development of a 10 kW, asymmetric half-bridge based, SS-CIC prototype. This prototype was used to illustrate the efficiency of the converter when the load rating was similar to the rated power of the converter.
- The development of a three-phase, five-level NPC coupled inductor converter (NPC-CIC) from the ACIB. By moving to a five-level platform, the potential to eliminate the output filter is possible, thereby increasing the power density of the multi-level converter, and potentially lowering costs.
- A space vector based approach was described that eliminates the common mode winding voltages in the five-level NPC-CIC. The space vector based approach was justified on the basis of converter complexity, and the ease with which the output voltage conversion quality can be optimised with this approach. Additionally, a space vector based analysis allows for the consideration of device switching frequency - an important aspect to converter efficiency.
- Experimental development of a 10 kW, asymmetric half-bridge based NPC-CIC prototype. This converter was developed to validate the space vector based

approach against other approaches that did not eliminate the common mode winding voltages.

- The development of a modular balancing bridge (MBB) based on the ACIB. The MBB can balance any number of voltage sources, independant of the characteristics of that voltage source, and without the requirement of cell voltage feedback.
- The derivation of the balancing currents for balancing voltages internal to the MBB and for balancing voltages between MBBs to the per-unit circuit parameters. These per-unit circuit parameters are derived to aide in the design of the MBB for an arbitrary number of voltage sources, and is related to a transformer size to illustrate the power density potential of the MBB.
- Experimental validation of the MBB balancing four 20 Ah lithium ion based batteries. A custom circuit was designed and populated with two transformers to illustrate the balancing power between these two transformers. Moreover, the converter was shown to operate for over 15 hours with stable temperatures, confirming that the design discussion presented for the MBB is appropriate.

6.2 Future Work

With the ACIB-based dc/ac converters, one promising directive for future rwork is the potential for conversion quality improvement in the space vector based 'common mode winding voltage elimination' approaches. Second, improvements can also be made in the operation of the MBB, with potentially faster correction when 'small' voltage differences are remaining in the battery string.

The space vector based approach described in Chapter 4 is not limited to the five-level, NPC-CIC. In fact, this converter was selected due to its optimal properties as a high quality, low-voltage dc/ac converter. However, any coupled inductor based converter can be analyzed in the fashion presented for Chapter 4, as the concept involves applying the condition that all useable vectors must use switching states where the common mode winding voltages sum to zero. Therefore, this approach can be extended to seven-level variants of the coupled inductor converters, or the three-level converter, as presented in Chapter 3.

Moreover, the space vector based approach, described in Chapter 4, details common mode winding elimination, and uses space vector rules to minimize the effect of eliminating these states on conversion quality and device switching frequency. When the

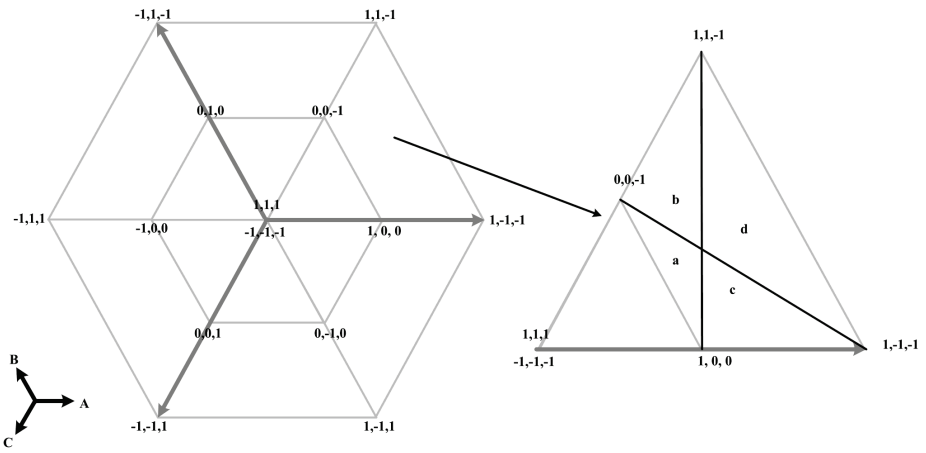


Fig. 6-1. Three-level space vector map of the SS-CIC with common mode winding voltage producing vectors eliminated. The first sextant is used as an example for segmenting the switching of vectors for regions a, b, c and d.

common mode winding voltage zero sum condition is applied, all coupled inductor converters will lose voltage output states at the outer edge of the sextant, e.g. Fig. 6-1. In this thesis, the approach justified using the larger 'three-level' triangles for the five-level converter due to the small impact on conversion quality when at higher modulation depths. However, if this same approach were applied to the SS-CIC, at modulation depths over 0.5, the switching would feature two-level voltage states - significantly reducing the conversion quality over half of the modulation cycle.

In Fig. 6-1, instead of selecting the {1,1,1} or {-1,-1,-1} vectors at modulation depths over 0.5, i.e. instead of using the 'two-level' triangle, the trapezoid can be segmented into non-equilateral triangles, as shown in Fig. 6-1. In this manner, vectors can be included to maintain three-level switching on one or more phases. Therefore, the conversion quality of coupled inductor converters that employ three-limb coupled inductors can be improved at the higher modulation depths.

However, as the segmentation of Fig. 6-1 is into triangles that are not described by 60° axes, the modulation approach would have to change significantly to incorporate these improvements. As an example, the determination of the regions 'a','b','c' or 'd' would incorporate methods not typically found in various space vector related literature. Furthermore, the calculation of the duty cycle of each vector would require a unique transformation for each segment. Lastly, as the number of available vectors is reduced at this point, the manipulation of switching states to minimize the device switching frequency would not be possible. Therefore, for the SS-CIC, the device switching frequency could increase by an appreciable amount.

With the modular balancing bridge, the designs presented in this thesis focused on a maximum assumed voltage unbalance. However, this presents a trade off for the designer: if the designed voltage unbalance is too high, the converter will compensate quickly, but as the voltage unbalance converges towards zero, the balancing speed will slow. This is because the balancing speed for the MBB has a negative exponential characteristic that depends on the starting voltage unbalance and the corresponding maximum balancing current.

However, one potential avenue for future work is enabling a 'dual' control mode in the MBB. In this manner, the MBB can be sized for a large voltage unbalance, and will automatically balance this voltage until it reaches a certain threshold. Afterwards, active control can begin to interleave the switching of the MBB units, to balance the remaining small voltages. As the interleaved cells would only see the leakage reactance, large balancing currents can flow, reducing the balancing time dramatically.

6.3 Concluding Remarks

This thesis explored the application of an asymmetrical coupled inductor bridge for solving particular limitations in emerging energy systems. The modular approach and reduced number of active devices is selected to keep system costs lower, while maintaining high power density for low-voltage applications. While battery systems are one potential application of this work, it is clear that such systems will begin to play an increased role in our world as low-energy density renewable resources replace high-energy density non-renewable resource. Therefore, it is hoped that this thesis will contribute to improving the performance of certain low-voltage applications, without influencing the cost by an appreciable amount.

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Appendix

Switch Selection Tables (with index input)

Index	Sa	Sb	Sc	Hex	Index	Sa	Sb	Sc	Hex	Index	Sa	Sb	Sc	Hex
0	6	6	6	666	257	6	6	6	666	515	2	7	6	276
1	6	2	7	627	258	2	6	7	267	516	7	2	6	726
2	4	14	6	4E6	259	6	4	14	64E	517	6	6	6	666
3	6	6	6	666	260	6	14	4	6E4	518	14	6	4	E64
4	6	6	6	666	261	7	6	2	762	519	7	2	6	726
5	14	4	6	E46	262	6	6	6	666	520	6	2	14	62E
6	6	7	2	672	263	6	14	4	6E4	521	6	3	6	636
7	6	6	6	666	264	6	12	12	6CC	522	2	3	7	237
8	5	14	6	5E6	265	6	14	4	6E4	523	6	2	14	62E
9	4	6	7	467	266	2	14	6	2E6	524	6	7	4	674
10	6	6	3	663	267	3	6	6	366	525	7	3	2	732
11	2	7	11	27B	268	3	6	6	366	526	6	3	6	636
12	7	2	11	72B	269	7	4	6	746	527	6	7	4	674
13	6	6	3	663	270	6	4	14	64E	528	6	6	12	66C
14	14	6	2	E62	271	6	12	12	6CC	529	6	2	14	62E
15	14	4	6	E46	272	2	14	6	2E6	530	2	7	6	276
16	12	4	14	C4E	273	2	6	7	267	531	3	3	6	336
17	12	6	6	C66	274	3	6	3	363	532	3	3	6	336
18	4	6	7	467	275	2	14	6	2E6	533	7	2	6	726
19	6	2	7	627	276	7	4	6	746	534	6	7	4	674
20	6	7	2	672	277	3	6	3	363	535	6	6	12	66C
21	14	6	2	E62	278	7	6	2	762	536	4	6	14	46E
22	12	6	6	C66	279	7	4	6	746	537	6	2	14	62E
23	12	14	4	CE4	280	4	12	14	4CE	538	2	7	6	276
24	4	6	7	467	281	6	4	14	64E	539	2	3	7	237
25	6	2	7	627	282	2	14	6	2E6	540	7	3	2	732
26	2	7	11	27B	283	2	6	7	267	541	7	2	6	726
27	4	6	7	467	284	7	6	2	762	542	6	7	4	674
28	14	6	2	E62	285	7	4	6	746	543	14	6	4	E64
29	7	2	11	72B	286	6	14	4	6E4	544	4	7	12	47C
30	6	7	2	672	287	14	12	4	EC4	545	4	3	14	43E
31	14	6	2	E62	288	3	4	14	34E	546	6	3	6	636
32	12	12	6	CC6	289	3	6	6	366	547	4	7	12	47C
33	12	4	7	C47	290	2	12	14	2CE	548	14	2	12	E2C
34	4	14	11	4EB	291	3	4	14	34E	549	6	3	6	636
35	6	6	3	663	292	3	14	4	3E4	550	14	3	4	E34

36	6	6	3	663	293	7	12	4	7C4	551	14	2	12	E2C
37	14	4	11	E4B	294	3	6	6	366	552	2	3	14	23E
38	12	14	2	CE2	295	3	14	4	3E4	553	4	7	12	47C
39	12	12	6	CC6	296	2	12	14	2CE	554	6	7	4	674
40	4	6	7	467	297	2	14	6	2E6	555	7	3	4	734
41	4	7	11	47B	298	3	14	2	3E2	556	2	3	14	23E
42	12	4	7	C47	299	2	12	14	2CE	557	6	2	14	62E
43	4	6	7	467	300	7	12	4	7C4	558	14	2	12	E2C
44	14	6	2	E62	301	3	4	7	347	559	7	3	4	734
45	12	14	2	CE2	302	7	4	6	746	560	2	7	12	27C
46	14	2	11	E2B	303	7	12	4	7C4	561	2	3	14	23E
47	14	6	2	E62	304	3	4	7	347	562	6	6	12	66C
48	12	6	6	C66	305	3	6	3	363	563	2	7	12	27C
49	12	2	7	C27	306	2	12	7	2C7	564	7	2	12	72C
50	4	7	11	47B	307	3	4	7	347	565	6	6	12	66C
51	6	3	11	63B	308	3	14	2	3E2	566	7	3	4	734
52	6	3	11	63B	309	7	12	2	7C2	567	7	2	12	72C
53	14	2	11	E2B	310	3	6	3	363	568	12	6	12	C6C
54	12	7	2	C72	311	3	14	2	3E2	569	4	7	12	47C
55	12	6	6	C66	312	2	14	6	2E6	570	6	7	4	674
56	12	4	7	C47	313	6	12	12	6CC	571	6	3	6	636
57	4	6	7	467	314	2	12	14	2CE	572	6	3	6	636
58	6	6	3	663	315	2	14	6	2E6	573	6	2	14	62E
59	12	4	7	C47	316	7	4	6	746	574	14	2	12	E2C
60	12	14	2	CE2	317	7	12	4	7C4	575	12	6	12	C6C
61	6	6	3	663	318	6	12	12	6CC	576	6	2	14	62E
62	14	6	2	E62	319	7	4	6	746	577	7	3	4	734
63	12	14	2	CE2	320	6	12	6	6C6	578	3	3	6	336
64	4	7	11	47B	321	2	14	6	2E6	579	6	2	14	62E
65	6	3	11	63B	322	3	4	7	347	580	6	7	4	674
66	4	6	7	467	323	6	12	6	6C6	581	3	3	6	336
67	4	7	11	47B	324	6	12	6	6C6	582	2	3	14	23E
68	14	2	11	E2B	325	3	14	2	3E2	583	6	7	4	674
69	14	6	2	E62	326	7	4	6	746	584	6	3	12	63C
70	6	3	11	63B	327	6	12	6	6C6	585	12	3	12	C3C
71	14	2	11	E2B	328	3	12	12	3CC	586	12	6	12	C6C
72	12	12	6	CC6	329	3	6	6	366	587	6	3	12	63C
73	12	6	3	C63	330	3	12	6	3C6	588	6	3	12	63C
74	12	12	3	CC3	331	3	12	12	3CC	589	12	6	12	C6C
75	6	6	3	663	332	3	12	12	3CC	590	12	3	12	C3C
76	6	6	3	663	333	3	12	6	3C6	591	6	3	12	63C

77	12	12	3	CC3	334	3	6	6	366	592	6	3	12	63C
78	12	6	3	C63	335	3	12	12	3CC	593	12	3	12	C3C
79	12	12	6	CC6	336	3	12	12	3CC	594	12	6	12	C6C
80	12	12	6	CC6	337	3	6	6	366	595	6	3	12	63C
81	12	6	3	C63	338	3	12	6	3C6	596	6	3	12	63C
82	12	12	3	CC3	339	3	12	12	3CC	597	12	6	12	C6C
83	6	6	3	663	340	3	12	12	3CC	598	12	3	12	C3C
84	6	6	3	663	341	3	12	6	3C6	599	6	3	12	63C
85	12	12	3	CC3	342	3	6	6	366	600	3	3	12	33C
86	12	6	3	C63	343	3	12	12	3CC	601	6	3	12	63C
87	12	12	6	CC6	344	3	12	6	3C6	602	3	3	6	336
88	12	6	6	C66	345	3	6	3	363	603	3	3	12	33C
89	12	3	3	C33	346	3	12	3	3C3	604	3	3	12	33C
90	12	6	3	C63	347	3	12	6	3C6	605	3	3	6	336
91	6	3	3	633	348	3	12	6	3C6	606	6	3	12	63C
92	6	3	3	633	349	3	12	3	3C3	607	3	3	12	33C
93	12	6	3	C63	350	3	6	3	363	608	3	3	12	33C
94	12	3	3	C33	351	3	12	6	3C6	609	6	3	12	63C
95	12	6	6	C66	352	3	12	6	3C6	610	3	3	6	336
96	12	6	6	C66	353	3	6	3	363	611	3	3	12	33C
97	12	3	3	C33	354	3	12	3	3C3	612	3	3	12	33C
98	12	6	3	C63	355	3	12	6	3C6	613	3	3	6	336
99	6	3	3	633	356	3	12	6	3C6	614	6	3	12	63C
100	6	3	3	633	357	3	12	3	3C3	615	3	3	12	33C
101	12	6	3	C63	358	3	6	3	363	616	6	3	12	63C
102	12	3	3	C33	359	3	12	6	3C6	617	12	3	12	C3C
103	12	6	6	C66	360	3	12	12	3CC	618	12	6	12	C6C
104	12	12	6	CC6	361	3	6	6	366	619	6	3	12	63C
105	12	6	3	C63	362	3	12	6	3C6	620	6	3	12	63C
106	12	12	3	CC3	363	3	12	12	3CC	621	12	6	12	C6C
107	6	6	3	663	364	3	12	12	3CC	622	12	3	12	C3C
108	6	6	3	663	365	3	12	6	3C6	623	6	3	12	63C
109	12	12	3	CC3	366	3	6	6	366	624	4	7	12	47C
110	12	6	3	C63	367	3	12	12	3CC	625	6	3	12	63C
111	12	12	6	CC6	368	3	4	7	347	626	2	3	14	23E
112	12	6	3	C63	369	2	12	14	2CE	627	4	7	12	47C
113	4	7	11	47B	370	3	12	6	3C6	628	14	2	12	E2C
114	12	4	7	C47	371	3	4	7	347	629	7	3	4	734
115	12	6	3	C63	372	3	14	2	3E2	630	6	3	12	63C
116	12	6	3	C63	373	3	12	6	3C6	631	14	2	12	E2C
117	12	14	2	CE2	374	7	12	4	7C4	632	3	3	12	33C

118	14	2	11	E2B	375	3	14	2	3E2	633	6	3	12	63C
119	12	6	3	C63	376	3	12	6	3C6	634	3	3	6	336
120	12	6	7	C67	377	3	6	3	363	635	3	3	12	33C
121	12	3	4	C34	378	3	12	3	3C3	636	3	3	12	33C
122	12	6	6	C66	379	3	12	6	3C6	637	3	3	6	336
123	6	3	2	632	380	3	12	6	3C6	638	6	3	12	63C
124	6	3	7	637	381	3	12	3	3C3	639	3	3	12	33C
125	12	6	6	C66	382	3	6	3	363	640	6	2	7	627
126	12	3	14	C3E	383	3	12	6	3C6	641	4	6	14	46E
127	12	6	2	C62	384	6	6	6	666	642	6	6	6	666
128	4	14	6	4E6	385	2	7	6	276	643	6	2	7	627
129	6	6	6	666	386	6	4	14	64E	644	6	7	2	672
130	2	6	7	267	387	6	6	6	666	645	6	6	6	666
131	4	14	6	4E6	388	6	6	6	666	646	14	6	4	E64
132	14	4	6	E46	389	6	14	4	6E4	647	6	7	2	672
133	7	6	2	762	390	7	2	6	726	648	12	6	6	C66
134	6	6	6	666	391	6	6	6	666	649	4	7	6	476
135	14	4	6	E46	392	4	14	12	4EC	650	6	7	2	672
136	6	4	7	647	393	6	6	12	66C	651	6	3	3	633
137	14	12	4	EC4	394	2	6	14	26E	652	6	3	3	633
138	6	12	6	6C6	395	2	7	6	276	653	6	2	7	627
139	6	14	2	6E2	396	7	2	6	726	654	14	2	6	E26
140	6	4	7	647	397	7	6	4	764	655	12	6	6	C66
141	6	12	6	6C6	398	6	6	12	66C	656	4	7	6	476
142	4	12	14	4CE	399	14	4	12	E4C	657	6	3	6	636
143	6	14	2	6E2	400	6	4	14	64E	658	4	6	14	46E
144	12	12	6	CC6	401	2	6	14	26E	659	4	7	6	476
145	4	14	11	4EB	402	3	6	6	366	660	14	2	6	E26
146	6	14	2	6E2	403	3	2	7	327	661	14	6	4	E64
147	12	12	6	CC6	404	3	7	2	372	662	6	3	6	636
148	12	12	6	CC6	405	3	6	6	366	663	14	2	6	E26
149	6	4	7	647	406	7	6	4	764	664	4	6	14	46E
150	14	4	11	E4B	407	6	14	4	6E4	665	4	7	6	476
151	12	12	6	CC6	408	2	6	14	26E	666	6	7	2	672
152	4	12	14	4CE	409	2	7	6	276	667	7	3	2	732
153	4	14	6	4E6	410	6	4	14	64E	668	2	3	7	237
154	6	4	7	647	411	2	6	14	26E	669	6	2	7	627
155	2	6	7	267	412	7	6	4	764	670	14	2	6	E26
156	7	6	2	762	413	6	14	4	6E4	671	14	6	4	E64
157	6	14	2	6E2	414	7	2	6	726	672	12	2	7	C27
158	14	4	6	E46	415	7	6	4	764	673	4	3	7	437

159	14	12	4	EC4	416	3	3	6	336	674	6	3	3	633
160	2	14	11	2EB	417	2	7	12	27C	675	12	2	7	C27
161	6	12	6	6C6	418	3	2	14	32E	676	12	7	2	C72
162	2	12	7	2C7	419	6	6	12	66C	677	6	3	3	633
163	2	14	11	2EB	420	6	6	12	66C	678	14	3	2	E32
164	7	4	11	74B	421	3	7	4	374	679	12	7	2	C72
165	7	12	2	7C2	422	7	2	12	72C	680	4	3	7	437
166	6	12	6	6C6	423	3	3	6	336	681	12	2	14	C2E
167	7	4	11	74B	424	2	6	14	26E	682	14	2	6	E26
168	4	12	7	4C7	425	3	2	14	32E	683	4	3	7	437
169	6	4	7	647	426	7	4	12	74C	684	14	3	2	E32
170	7	4	11	74B	427	2	6	14	26E	685	4	7	6	476
171	14	12	2	EC2	428	7	6	4	764	686	12	7	4	C74
172	4	12	7	4C7	429	2	14	12	2EC	687	14	3	2	E32
173	2	14	11	2EB	430	3	7	4	374	688	12	2	14	C2E
174	6	14	2	6E2	431	7	6	4	764	689	4	3	14	43E
175	14	12	2	EC2	432	6	12	12	6CC	690	6	3	6	636
176	4	14	11	4EB	433	2	14	12	2EC	691	12	2	14	C2E
177	12	12	6	CC6	434	3	4	14	34E	692	12	7	4	C74
178	4	12	7	4C7	435	3	6	6	366	693	6	3	6	636
179	4	14	11	4EB	436	3	6	6	366	694	14	3	4	E34
180	14	4	11	E4B	437	3	14	4	3E4	695	12	7	4	C74
181	14	12	2	EC2	438	7	4	12	74C	696	4	7	6	476
182	12	12	6	CC6	439	6	12	12	6CC	697	4	3	7	437
183	14	4	11	E4B	440	3	2	14	32E	698	6	3	3	633
184	6	12	6	6C6	441	3	3	6	336	699	4	7	6	476
185	6	4	7	647	442	2	6	14	26E	700	14	2	6	E26
186	7	4	11	74B	443	3	2	14	32E	701	6	3	3	633
187	3	6	11	36B	444	3	7	4	374	702	14	3	2	E32
188	3	6	11	36B	445	7	6	4	764	703	14	2	6	E26
189	2	14	11	2EB	446	3	3	6	336	704	12	6	12	C6C
190	6	14	2	6E2	447	3	7	4	374	705	12	2	14	C2E
191	6	12	6	6C6	448	2	14	12	2EC	706	14	2	6	E26
192	6	4	7	647	449	2	6	14	26E	707	6	3	6	636
193	12	12	6	CC6	450	6	12	12	6CC	708	6	3	6	636
194	4	12	7	4C7	451	2	14	12	2EC	709	4	7	6	476
195	6	4	7	647	452	7	4	12	74C	710	12	7	4	C74
196	6	14	2	6E2	453	6	12	12	6CC	711	12	6	12	C6C
197	14	12	2	EC2	454	7	6	4	764	712	12	3	3	C33
198	12	12	6	CC6	455	7	4	12	74C	713	12	3	6	C36
199	6	14	2	6E2	456	3	3	6	336	714	12	6	6	C66

200	6	12	3	6C3	457	3	3	12	33C	715	12	3	3	C33
201	3	6	11	36B	458	3	6	12	36C	716	12	3	3	C33
202	3	12	11	3CB	459	6	6	12	66C	717	12	6	6	C66
203	6	12	3	6C3	460	6	6	12	66C	718	12	3	6	C36
204	6	12	3	6C3	461	3	6	12	36C	719	12	3	3	C33
205	3	12	11	3CB	462	3	3	12	33C	720	12	3	3	C33
206	3	6	11	36B	463	3	3	6	336	721	12	3	6	C36
207	6	12	3	6C3	464	3	3	6	336	722	12	6	6	C66
208	6	12	3	6C3	465	3	3	12	33C	723	12	3	3	C33
209	3	6	11	36B	466	3	6	12	36C	724	12	3	3	C33
210	3	12	11	3CB	467	6	6	12	66C	725	12	6	6	C66
211	6	12	3	6C3	468	6	6	12	66C	726	12	3	6	C36
212	6	12	3	6C3	469	3	6	12	36C	727	12	3	3	C33
213	3	12	11	3CB	470	3	3	12	33C	728	12	3	6	C36
214	3	6	11	36B	471	3	3	6	336	729	12	3	12	C3C
215	6	12	3	6C3	472	3	6	6	366	730	12	6	12	C6C
216	12	12	3	CC3	473	3	6	12	36C	731	12	3	6	C36
217	12	12	6	CC6	474	3	12	12	3CC	732	12	3	6	C36
218	6	12	11	6CB	475	6	12	12	6CC	733	12	6	12	C6C
219	12	12	11	CCB	476	6	12	12	6CC	734	12	3	12	C3C
220	12	12	11	CCB	477	3	12	12	3CC	735	12	3	6	C36
221	6	12	11	6CB	478	3	6	12	36C	736	12	3	6	C36
222	12	12	6	CC6	479	3	6	6	366	737	12	3	12	C3C
223	12	12	3	CC3	480	3	6	6	366	738	12	6	12	C6C
224	12	12	3	CC3	481	3	6	12	36C	739	12	3	6	C36
225	12	12	6	CC6	482	3	12	12	3CC	740	12	3	6	C36
226	6	12	11	6CB	483	6	12	12	6CC	741	12	6	12	C6C
227	12	12	11	CCB	484	6	12	12	6CC	742	12	3	12	C3C
228	12	12	11	CCB	485	3	12	12	3CC	743	12	3	6	C36
229	6	12	11	6CB	486	3	6	12	36C	744	12	3	3	C33
230	12	12	6	CC6	487	3	6	6	366	745	12	3	6	C36
231	12	12	3	CC3	488	3	3	6	336	746	12	6	6	C66
232	6	12	3	6C3	489	3	3	12	33C	747	12	3	3	C33
233	3	6	11	36B	490	3	6	12	36C	748	12	3	3	C33
234	3	12	11	3CB	491	6	6	12	66C	749	12	6	6	C66
235	6	12	3	6C3	492	6	6	12	66C	750	12	3	6	C36
236	6	12	3	6C3	493	3	6	12	36C	751	12	3	3	C33
237	3	12	11	3CB	494	3	3	12	33C	752	12	2	14	C2E
238	3	6	11	36B	495	3	3	6	336	753	12	3	6	C36
239	6	12	3	6C3	496	3	6	12	36C	754	4	3	7	437
240	2	14	11	2EB	497	3	2	14	32E	755	12	2	14	C2E

241	4	12	7	4C7	498	2	14	12	2EC	756	12	7	4	C74
242	6	12	11	6CB	499	3	6	12	36C	757	14	3	2	E32
243	2	14	11	2EB	500	3	6	12	36C	758	12	3	6	C36
244	7	4	11	74B	501	7	4	12	74C	759	12	7	4	C74
245	6	12	11	6CB	502	3	7	4	374	760	12	3	6	C36
246	14	12	2	EC2	503	3	6	12	36C	761	12	3	12	C3C
247	7	4	11	74B	504	3	6	6	366	762	12	6	12	C6C
248	12	12	3	CC3	505	3	6	12	36C	763	12	3	6	C36
249	12	12	6	CC6	506	3	12	12	3CC	764	12	3	6	C36
250	6	12	11	6CB	507	6	12	12	6CC	765	12	6	12	C6C
251	12	12	11	CCB	508	6	12	12	6CC	766	12	3	12	C3C
252	12	12	11	CCB	509	3	12	12	3CC	767	12	3	6	C36
253	6	12	11	6CB	510	3	6	12	36C					
254	12	12	6	CC6	511	3	6	6	366					
255	12	12	3	CC3	512	2	7	6	276					
256	6	4	14	64E	513	4	6	14	46E					
					514	6	6	6	666					