Harmonic Mitigation of Voltage Source Converter Based High-Power Variable Frequency Drives

by

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Abstract

Voltage-Source-Converter (VSC) based high-power Variable Frequency Drives (VFDs) are widely adopted in industrial applications. To meet the grid codes and ensure the motors' proper operation, VSC based high-power VFDs are expected to produce low harmonic distortions and resist the harmonic disturbance from the load or utility grid.

This Ph.D. research focuses on harmonic mitigation of VSC based high-power VFDs. To be specific, the research includes two aspects: improving harmonic control performance for the active front end of VFD and enhancing the capacitor ripple mitigation in multilevel VFDs.

For VSC based high-power VFDs, the low switching frequency, the associated large system delay, and low sampling rate can significantly affect the harmonic control performance. To improve the harmonic control performance, virtual impedance theory and feed-forward control are employed to flexibly control the VSC output current harmonics, eliminate the cascaded multiloop controllers, and obtain fast transient. Considering the effects caused by the low sampling rate and large system delay, multi-rate sampling scheme is applied to increase the sampling rate for harmonics. As the high-power VSC with multi-rate control is a time-varying system, the multi-rate modeling method is thus applied to ensure the accurate control loop analysis and design.

On the other hand, the capacitor ripples can also cause output distortions in the multilevel VFDs. Some multilevel converters have difficulties in capacitor-

balancing, leading to large voltage ripples and low output quality, particularly at low fundamental frequencies (low motor speed). To avoid this, the PWM methods to improve floating capacitor voltage balancing and new multilevel converter topologies suitable for high-power applications are required. A new PWM method, named Stair Edge PWM (SEPWM) method, is proposed to obtain more switching states for converters without the capability to adequately control the voltage on floating capacitors. With the proposed PWM, the floating-capacitor-based multilevel converter can produce high-quality output current and voltage with the reduced requirement on the capacitance of floating capacitors. To further improve the power quality of VFD without using complicated PWM method, a novel multilevel converter topology, named seven-level hybrid-clamped (7L-HC) converter, is proposed. The proposed topology can achieve excellent capacitor voltage balancing in a wide frequency range (from 0 Hz to 60 Hz), which is typically required for VFD systems.

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List of Abbreviations

AFE	Active Front End
ANPC	Active Neutral-Point Clamped
APF	Active Power Filter
CCM	Current Control Method
CHB	Cascaded H Bridge
CFF	Current Feed-Forward
CSC	Current Source Converter
DB	Deadbeat
DFE	Diode Front End
DSP	Digital Signal Processor
FC	Flying Capacitor
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
HC	Hybrid Clamped
HCM	Hybrid Control Method
LV	Low Voltage
LPTV	Linear Periodic Time-Varying
LSPWM	Level-Shift PWM
LTI	Linear Time-Invariant
MIMO	Multiple-Input Multiple-Output
MLC	Multi-Level Converter

MMC	Modular Multilevel Converter
MPC	Multi-Point Clamped
MV	Medium Voltage
NNPC	Nested Neutral-Point-Clamped
NNPP	Nested Neutral Point Piloted
NPC	Neutral-Point-Clamped
PCC	Point of Common Coupling
PI	Proportional Integral
PR	Proportional Resonant
PWM	Pulse Width Modulation
PSPWM	Phase-Shift PWM
RC	Repetitive Controller
RSC	Resonant Controller
SEPWM	Stair-Edge Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
THDi	Total Harmonic Distortion of current
THDv	Total Harmonic Distortion of voltage
VCM	Voltage Control Method
VSC	Voltage Source Converter
VFD	Variable Frequency Drive
VFF	Voltage Feed-Forward

VVVF	Variable Voltage Variable Frequency
ZOH	Zero-Order-Hold
2L	Two-Level
3L	Three-Level
4L	Four-Level
5L	Five-Level
7L	Seven-Level
9L	Nine-Level

Chapter 1

Introduction

With the development of power electronic technology [1], high-power (from 0.5 MW to several MW) Variable Frequency Drives (VFDs) [2], are increasingly used in applications like railway traction, pumps, fans, compressors, etc., providing smooth startup/stop, speed and torque control, and other required functions for motors. The VFD system can reduce energy consumption and increase productivity [2]-[3]. As a result, the predicted market of high-power VFDs will reach 170GW in 2020 [4].

In VFD systems, harmonics can be a challenge to proper operation and efficiency [5]. The harmonic issues can be caused by the utility grid and load. In addition, if a VFD is built with multilevel topology [6] with unclamped DC-link capacitors or floating capacitors, the voltage ripples on capacitors will also cause harmonics. Therefore, different approaches should be taken according to the reason for the harmonics. The research reported in this thesis was undertaken to:

(1) improve the harmonic control and sampling scheme in VFDs to cope with the harmonics caused by the utility and loads;

(2) improve modeling methods to help obtain accurate virtual impedance design;

(3) develop PWM methods for multilevel VFD to ensure the capacitor-balancing;

(4) develop multilevel topology with the ability to balance its capacitors adequately.

The following sections in this chapter elaborate the background information of this work, introduce the objectives of this research project, and outline the structure of this thesis.

1.1 Introduction to High-Power Variable Frequency Drives

1.1.1 Topologies for High-Power VFDs

As shown in Figure 1.1, different types of high-power converter topologies can be adopted in high-power VFDs. Compared with direct conversion topologies and current source converters, the voltage source converters (VSC), including two-level (2L) VSCs and multilevel VSCs, are the most commercialized topologies [2].

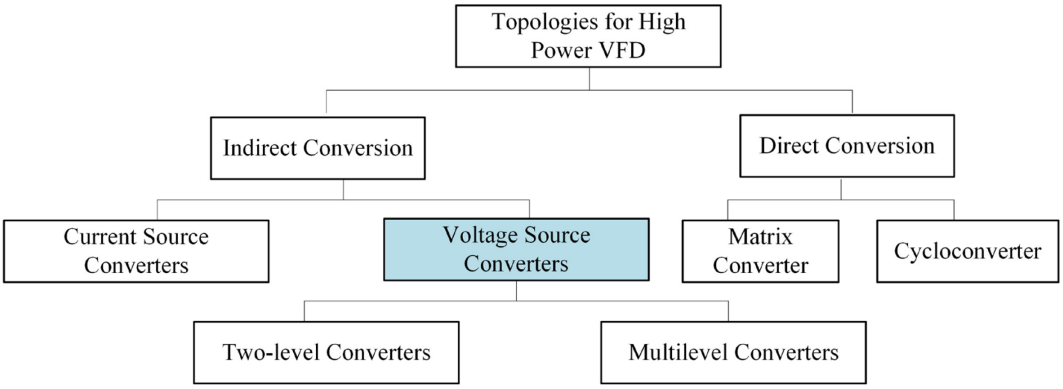

Figure 1.1 Topology classifications for high-power VFDs

To meet the various requirements, both low-voltage (LV; < 2.3 kV) and medium-voltage (MV; 2.3 kV-13.8 kV) high-power drives are commercialized. Due to the limited blocking voltage of the power semiconductors, 2L VSCs are usually adopted in LV drives, while multilevel topologies are widely used in MV drives [6].

The 2L-VSC topology, shown in Figure 1.2, features a low number of devices and a simple structure, facilitating control, manufacture, maintenance. However, the voltage stress on the power electronic switches is the same as the DC-link voltage, making it hard to apply in medium-voltage applications.

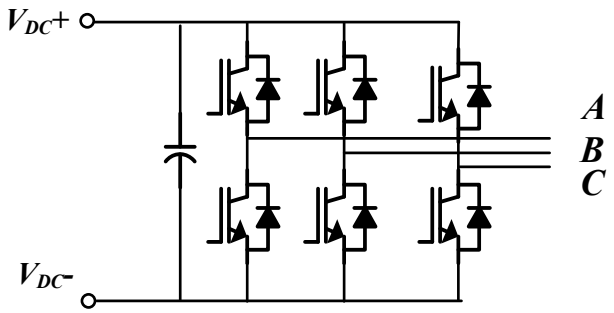

Figure 1.2 2L-VSC topology

On the other hand, MV high-power drives show lower overall cost when the motor rates more than 500 hp or the cable length is longer than 92 m [7]. The multilevel converters (MLCs) can reduce the voltage stress on their power electronic switches without series-connection, making it possible to build MV drives at a low cost [8]-[9]. Also, MLCs have lower *dv/dt* and higher equivalent switching frequency, bringing some advanced performance. Hence, some multilevel topologies, such as three-level (3L) Neutral-Point-Clamped (NPC) [10], 3L Flying Capacitor (FC) [11], five-level (5L)-Active NPC (ANPC) [12], 5L Nested-Neutral-Point-Piloted (NNPP) [13], Cascaded H-Bridge (CHB) [14], Modular Multilevel Converter (MMC) [15], etc., have been commercialized in the VFD market. The commercialized products are concluded in TABLE 1.1, and these topologies are shown in Figure 1.3.

TABLE 1.1 Industry Drives and Topologies

Converter Type	Topology	Voltage Rating	Power Rating	Examples
Two Level Converter	2L-VSC	400-690V	Up to 1.4MW	Alstom (VDM5000) Rockwell PowerFlex 755T
Multilevel Converter	3L-NPC	2.3-4.16kV	Up to 5MW	Eaton SC9000 ABB ACS1000
	3L-FC	3.3/4.16kV	0.3-8MW	Alstom (VDM6000 Symphony)
	5L-ANPC	4.16-6.9kV	0.25-2.5 MW	ABB ACS2000
	5L-NNPP	3.3-13.8kV	0.5-3MW	GE MV6
	CHB	2.4-13.8kV	0.15-60MW	Siemens GH180 Rockwell PowerFlex 6000
	MMC	3.3-7.2kV	6-13.7MW	Schneider Altivar1200 Siemens SM120

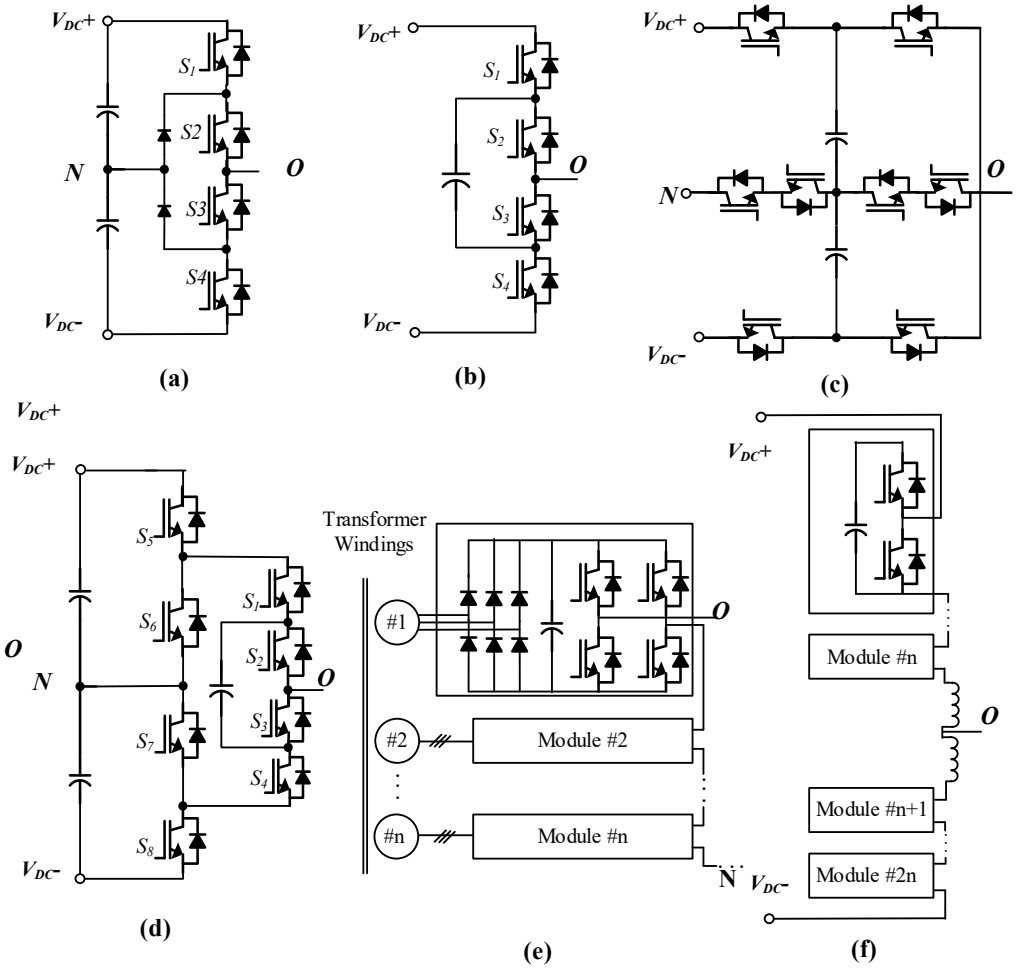

Figure 1.3 Some commercialized multilevel converters: (a) 3L-NPC; (b) 3L-FC; (c) 5L-NNPP; (d) 5L-ANPC; (e) CHB; (f) MMC

1.1.2 Structures of High Power VFD and the Power Quality

To adjust motor speed, VFDs usually require AC-DC-AC conversion to consume power from the utility grid with fixed frequency and provide voltage/current with varied frequency to motors [16]. Hence, a typical structure of the MV VFD system consists of a front end, a DC-link, and a motor-side converter, which is shown in Figure 1.4.

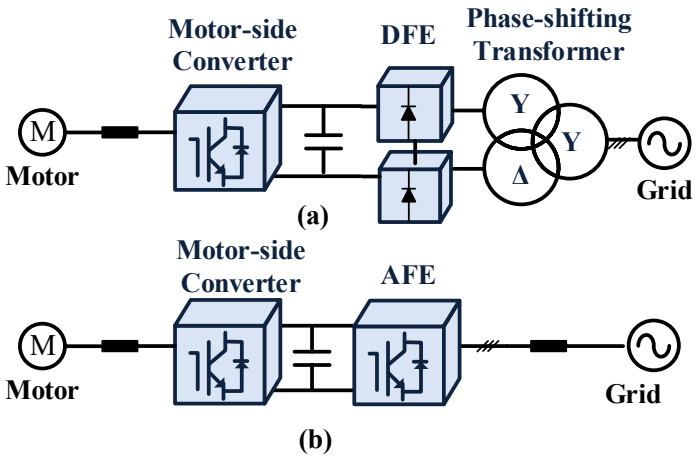

Figure 1.4 Typical structure of VFDs: (a) DFE-based VFD; (b) AFE-based VFD

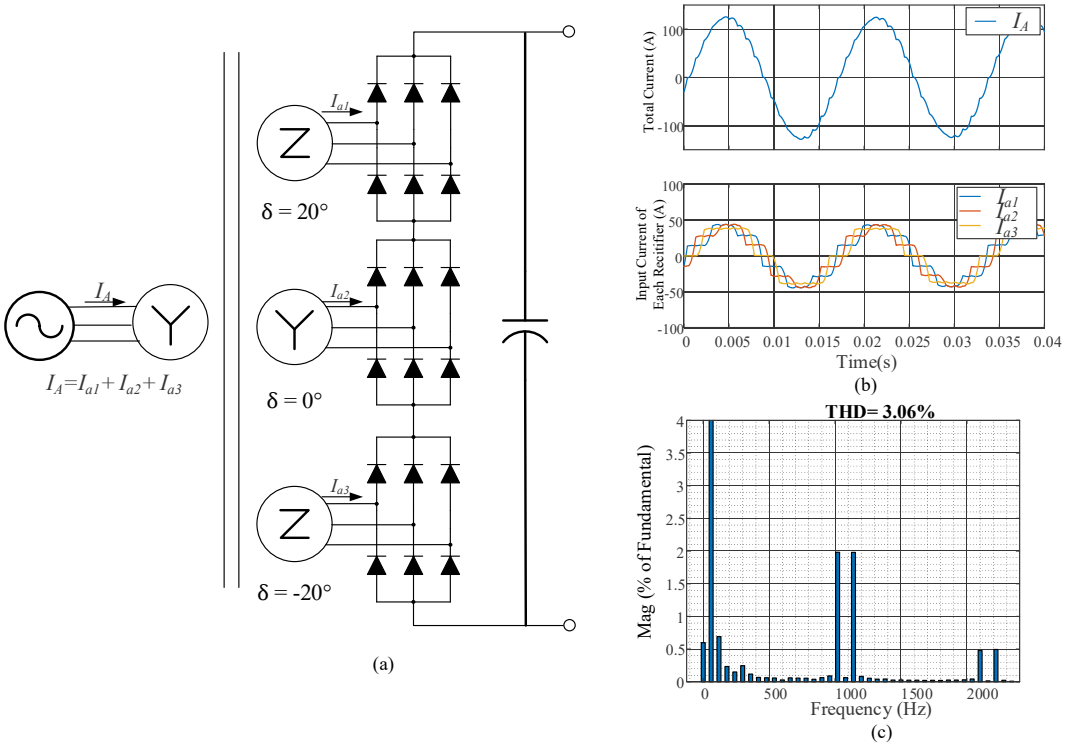

Figure 1.5 18-pulse DFE and its currents: (a) 18-pulse DFE topology; (b) current waveforms; (c) FFT analysis of the grid-side current

The front end can be built with diodes, making it a diode front end (DFE). Multi-pulse DFEs, which consist of phase-shifting transformers and diode rectifiers, are preferred due to the lower Total Harmonic Distortions (THD). An 18-pulse DFE is shown in Figure 1.5 (a) as an example. Thanks to the phase-shifting transformer, the distorted currents consumed by each rectifier can cancel low-order components,

obtaining sinusoidal frid-side currents, shown in Figure 1.5 (b). The THDs can be as low as 3.06%, as shown in Figure 1.5 (c). The THDs of grid-side current under rated conditions for different types of DFE, including 6-,12-,18-, and 24-pulse DFE, are listed in TABLE 1.2. Wherein, the grid-side currents of 18-pulse and 24-pulse DFE can fulfill harmonic standards like IEEE 519-2014 [17].

TABLE 1.2 Current THD of Different Front End at Rated Condition

Front End Type	THD of Line-Side Current
6-pulse DFE	32.7%
12-pulse DFE	8.38%
18 pulse DFE	3.06%
24-pulse DFE	1.49%

Besides multi-pulse DFE, one can use Active Front End (AFE), which uses active switches, to improve the quality of grid-side current. Also, an AFE can enable the four-quadrant operation for VFD. With AFE, the harmonics will be related to the control scheme, PWM scheme, switching frequency, and filter design. With proper design, an AFE can be of much higher power quality than a DFE and allows flexible control to further improve its functionality and performance [18].

1.2 Harmonic Issues in High-Power Variable Frequency Drives

In high-power drives, various reasons can cause the harmonics:

1) Extremely low switching frequency: when the switching frequency is smaller than nine times the fundamental frequency, low-order harmonics can be produced.
2) Filter resonance: if an LC/LCL filter is installed, harmonics can be amplified if the frequencies are close to the resonant frequency of the filter, which can be changed due to the line impedance of the utility grid.
3) Interaction between VFD and background harmonics or local nonlinear loads: the utility grid can have distorted voltage at the Point of Common Coupling (PCC). Also, the local nonlinear loads can generate harmonic currents, which will also cause distortions at PCC. The distorted voltage at PCC can cause VFDs, both DFE-based AFE-based VFDs, to produce distorted current.

4) Floating capacitor ripples: in multilevel VFDs, the output waveforms can be distorted if the floating capacitors or unclamped DC-link capacitors are not well balanced.

This thesis will focus on the load and utility grid induced harmonics, and the unclamped-capacitor-ripple-caused harmonics, i.e., reason 3) and 4).

1.2.1 Harmonic Interferences Caused by the Load and Grid

The nonlinear loads are widely installed in the distribution grid, causing background harmonics and local harmonics.

When remote nonlinear loads are installed, shown in Figure 1.6 (a), the generated harmonic currents can impact the distribution grid voltage, causing background harmonics. As a result, VFD will see a distorted voltage at PCC.

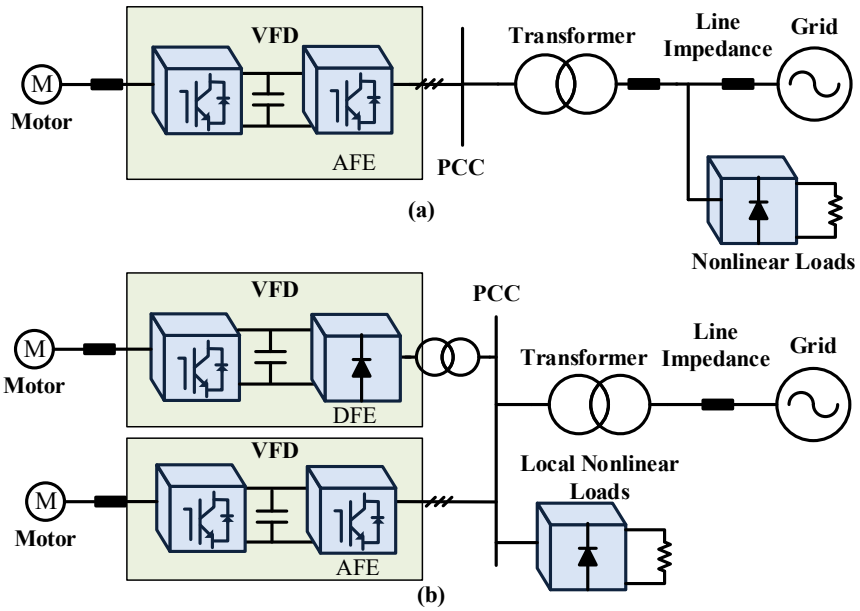

Figure 1.6 The reasons of harmonic interferences: (a) background harmonics caused by remote nonlinear loads; (b) local nonlinear loads caused by DFE-based VFD and nonlinear loads

The nonlinear loads can also cause local harmonics. As shown in Figure 1.6 (b), when a nonlinear load is installed between VFD and PCC, the distorted current can also induce the distortion in the PCC voltage when harmonic currents flow through the impedance of feeder line. Moreover, the DFE-based VFD systems also behave as nonlinear loads. Hence, when DFE-based VFDs and AFE-based VFD

are mixed, the DFE-based VFDs can also induce the AFE-based VFD to generate low-order harmonics.

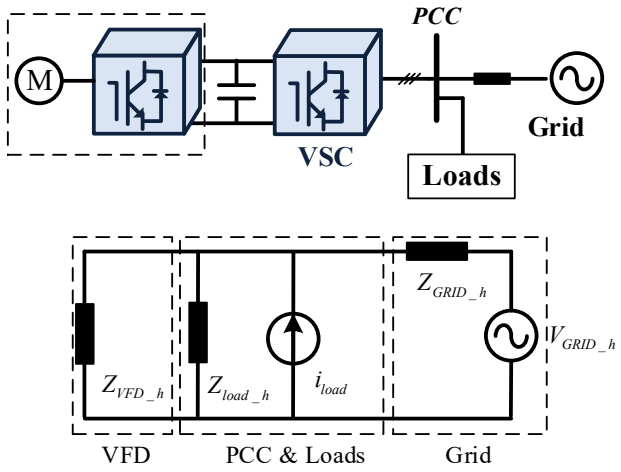

Figure 1.7 Equivalent model of VFD system at harmonic frequencies

The harmonic interactions between VFDs and nonlinear loads can be described with impedance models, shown in Figure 1.7. According to the Thevenin theorems, VFD and grid are equivalent to the voltage sources and the corresponding equivalent impedances, which is Z_{VFD} and Z_{GRID} respectively. The nonlinear load, which generates the harmonics, is modeled as a current source i_{load} and an impedance Z_{load}. However, at the harmonic frequencies, the fundamental frequency power supply shall be omitted, and the system model can be simplified as the harmonic source i_{load} and three impedance, $Z_{\text{VFD\_}h}$, $Z_{\text{load\_h}}$, and $Z_{\text{GRID\_}h}$. The background harmonics in the ground can also be seen as a voltage source $V_{\text{GRID\_h}}$. Generally, the harmonic currents are shared by both VFD and the grid, leading to distortions at VFD input and PCC.

An example is shown in Figure 1.8. Without nonlinear loads, the load current I_{load} is 0 and the PCC voltage V_{PCC}, utility side current I_{grid}, and AFE current I_{AFE}, are all of high quality. When the nonlinear load is connected at 0.05s, the harmonics are induced and appears in I_{AFE}. More importantly, V_{PCC} and I_{grid} are all distorted and can violate grid codes.

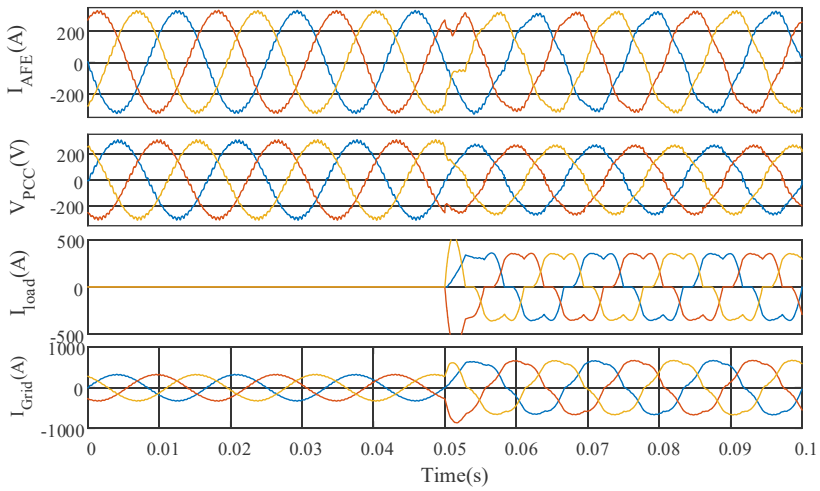

Figure 1.8 Harmonic distortions caused by local harmonics

To improve the power quality at PCC, a VFD is expected to have large impedance at harmonic frequencies to resist background harmonics. The harmonic currents will be blocked by VFD, and PCC will not suffer from harmonic pollutions. On the other hand, if the harmonics are generated by local nonlinear loads, VFDs are expected to have low impedance, absorbing all the harmonics and reducing the harmonics flowing to the grid.

The impedance of a VFD depends on the filter design and control of the AFE. To cope with the different requirements on the impedances of VFDs, harmonic control aiming at changing the equivalent impedance at harmonic frequencies should be adopted.

1.2.2 Capacitor Voltage Ripples in Multilevel VFD

In MV MLCs, the unclamped capacitors, including floating capacitors and unclamped DC-link capacitors, are widely used, as shown in Figure 1.9. A typical example of topologies with unclamped DC-link capacitors is the 3L-NPC shown in Figure 1.9(a), which requires neutral-point balancing, i.e., balancing the voltage of unclamped DC-link capacitors [19]. The unclamped DC-link capacitors also exist in T-type NPC, four-level (4L)-Hybrid Clamped (HC) (Figure 1.9(c)), 5L-Active NPC (ANPC) (see Figure 1.9(e)), etc. For topologies with floating capacitors, the well-known flying capacitor converter [20] as shown in Figure 1.9(b) is a good

example. Moreover, other topologies such as 4L-Nested NPC (NNPC) (see Figure 1.9(d)), 4L-HC, and 5L-ANPC, also have floating capacitors.

In those topologies, when the floating capacitors and unclamped DC-link capacitors cannot be adequately balanced, large ripples can present on voltages of the capacitors. The ripples can lead to low output quality and additional voltage stress on the devices [21]-[22]. Moreover, as the MV drives may be required to start the motor or operate in low motor speed, the multilevel drive converters should be able to balance the capacitors in a wide frequency range, e.g., 0-60Hz [23]. Unless the capacitors are clamped [24] or self-balanced [25], only topologies with good balancing capabilities can be adopted in drives, such as 5L-ANPC [26] and 5L-multipoint clamped (MPC) [27].

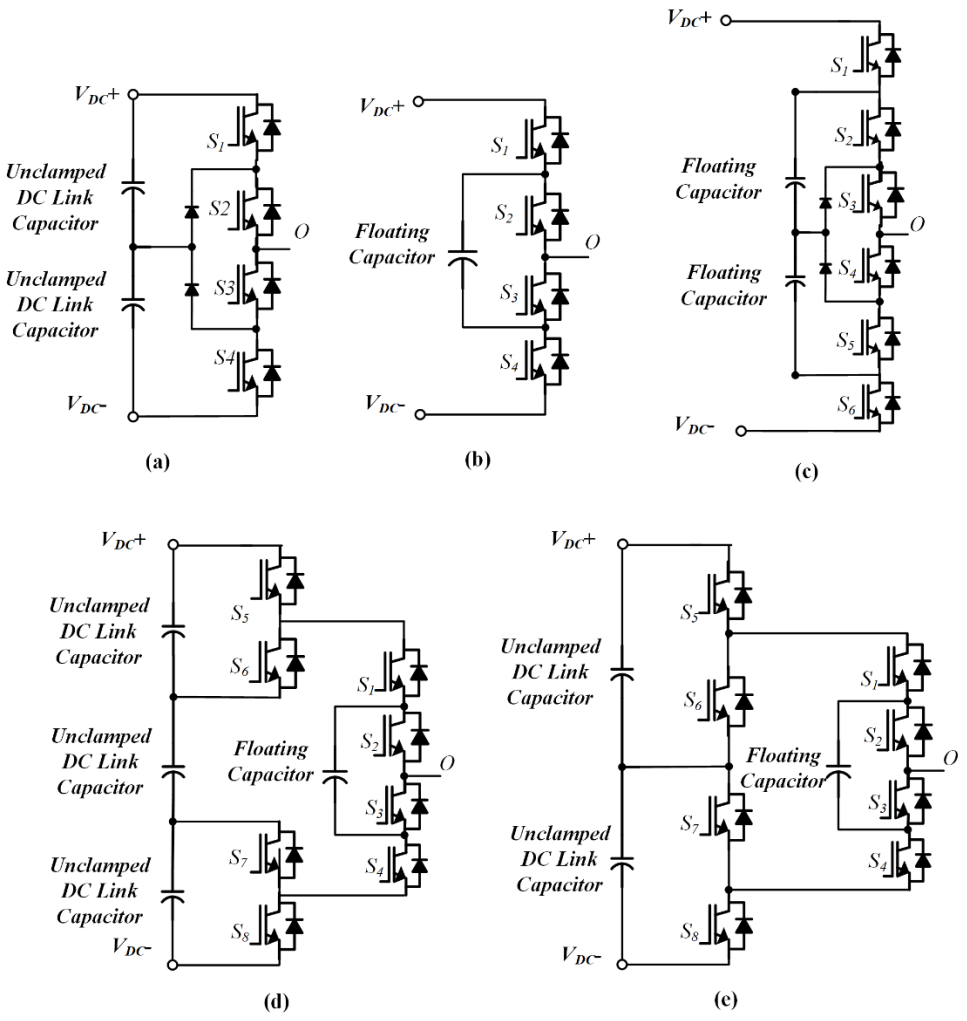

Figure 1.9 Some examples of floating capacitor topologies: (a) 3L-NPC; (b) 3L-FC; (c) 4L-NNPC; (d) 4L-HC; (e) 5L-ANPC

Therefore, the output quality of multilevel VFDs is highly dependent on the quality of capacitor voltages. For example, 5L-ANPC converters and 3L-FC converters have the complete voltage balancing capability, which means their DC-link capacitors or floating capacitors can be balanced under any current direction and any PWM period with proper utilization of the redundant switching states.

However, some topologies do not have complete voltage balancing capability. The reasons are mainly:

1) inherent topology limitation and the lack of sufficient redundant switching states for capacitor-balancing within a PWM period (such as MMC, NNPC);

2) the attempt to push the MLCs to operate with higher output levels and lose the redundant switching state because of this (such as the operation method in [28]).

As a result, the capacitors in those MLCs can only be balanced with the help of current direction change at the fundamental frequency, which is defined as the incomplete capacitor-voltage-balancing capability in this thesis. The incomplete capacitor-voltage-balancing capability leads to fundamental frequency ripples, which can affect the converter operation and increase capacitor voltage rating, increase the requirement on voltage rating, and increase the required capacitance of capacitors.

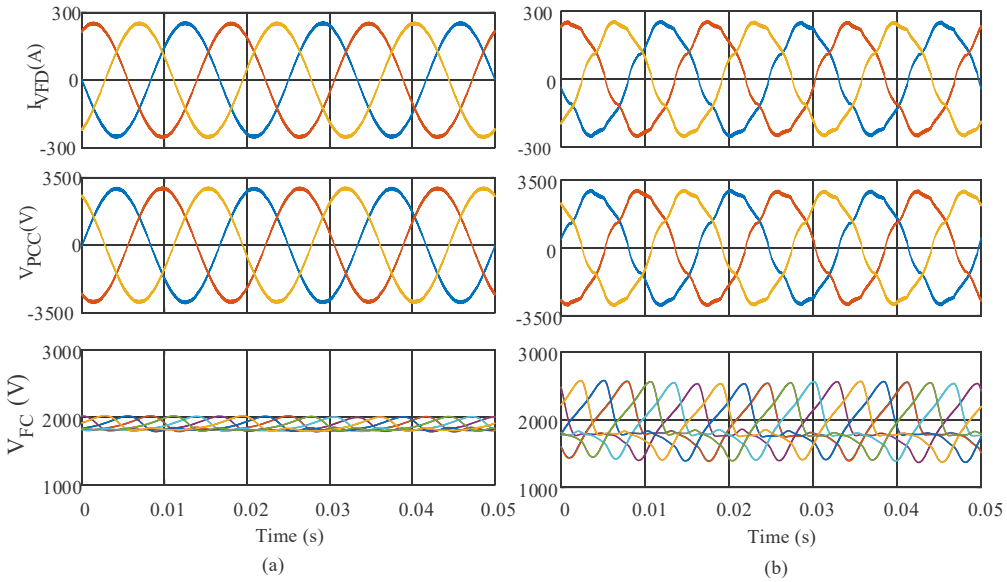

Figure 1.10 Ripple amplitude and the output quality of MMC: (a) operation under low floating capacitor ripples; (b) operation under high floating capacitor ripples

Taking MMC as an example, the impacts of voltage ripples are validated by simulation. As can be seen in Figure 1.10, with a large capacitor, the fundamental frequency ripples are well mitigated, and the high-quality voltage and current are produced. However, with lower capacitance, the ripples can significantly impact the voltage and current quality. Distortions can be easily observed.

To cope with capacitor ripples, the balancing schemes to improve capacitor-balancing for MLCs should be developed. Meanwhile, topology-based solutions, such as adding extra balancing circuits or inventing new topology, can be adopted.

1.3 Challenges to Mitigate Harmonics in VSC-Based High-Power VFD

1.3.1 Challenges to Harmonic Control with VSC-based High-Power VFDs

As discussed, mitigating the harmonics caused by background voltage harmonics and local nonlinear loads requires VFDs to control their output impedances at harmonic frequencies. However, it is challenging to control output impedance with high-power converters due to their low switching frequency, e.g., 1k-2kHz. Generally, the synchronous sampling method is used in power electronics converters and limits the sampling frequency to 1 or 2 times the switching frequency. But in this case, the sampling rate of harmonics will be insufficient, and the system delay can affect harmonic control.

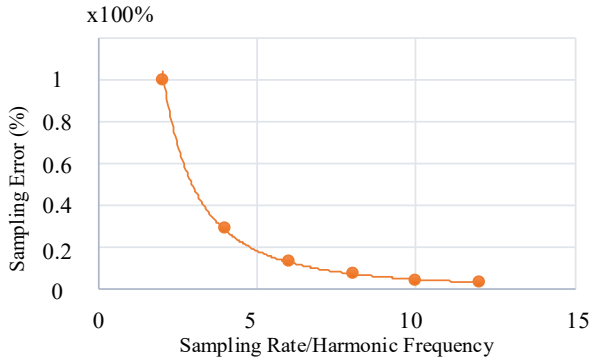

Figure 1.11 Sampling rate and sampling error under the worst-case scenario

As can be seen from Figure 1.11, the sampling error reduces as the sampling rate increases. The sampling error will decrease to ignorable level when the sampling rate is higher than ten times the harmonic frequency. However, in high-power converters, it is difficult to obtain a sampling rate at ten times the highest frequency of harmonics required to compensate. Taking 7^{th} order harmonics as an example, a 420 Hz signals requires 4.2 kHz sampling rate, which is hard to obtain in high-power converters.

Moreover, the system delay consists of the computation delay and the PWM delay. The computation delay is the same length as the sampling period. With a single-update synchronous sampling method, the computation delay is one switching period. And it will be 0.5 times of switching period in a double-update synchronous sampling method. In addition, the PWM delay is approximately half of the switching frequency. Therefore, under a synchronous sampling method, the system delay can be 1-1.5 times of switching period.

Considering the low sampling rate and large system delay, harmonic control performance can be improved by adopting a control scheme with fast transient responses. Also, the sampling method should be enhanced.

1.3.1 Challenges to Capacitor-Balancing Improvement for High-Power VFDs

Incomplete capacitor-voltage-balancing capabilities of MLCs are generally caused by the lack of redundant switching states to perform capacitor voltage control under any current direction. To have the complete capacitor-voltage-balancing capability, the converter must provide the floating capacitors with charging/discharging paths under any current directions in each switching period. As MLCs generally generate two consecutive levels in each switching period, the charging/discharging switching states should always be available in two adjacent output levels. Therefore, for topologies with incomplete capacitor-voltage-balancing capability, the ripple mitigation can be improved by either changing the topology or changing the PWM method.

Unclamped DC-link capacitors should be balanced as well. The DC-link capacitors can be balanced by using additional control loops to inject zero-sequence current, or by using redundant switching states.

When the topology contains both floating capacitors and unclamped DC-link capacitors, the balancing scheme should be carefully designed to comprehensively fulfill the balancing requirements of all the capacitors.

1.4 Thesis Objectives and Motivations

The overall objective of this thesis is to deal with the harmonic issues in LV/MV high-power VFD systems. Considering the different causes of harmonics, the research on harmonic mitigation includes the following two aspects: 1) improving the control scheme and sampling method to enable the high-power VFD to mitigate harmonics caused by the local loads or utility grid; 2) finding PWM approaches and suitable topology to help avoid floating capacitor ripples in multilevel VFDs.

A summary of the research objectives addressed in each chapter is listed here.

Chapter 2

In this chapter, a harmonic control strategy with an improved sampling scheme is proposed to enhance the harmonic control performance of high-power VFD. In VSC-based high-power VFDs, the low switching frequency causes low control bandwidth, significant system delay, and low sampling rate, affecting the harmonic control performance. The feed-forward harmonic control scheme is proposed to improve harmonic control dynamics. This control strategy can replace the cascaded multi-loop control structure. The harmonic compensation signals are fed directly to the modulation reference, improving the dynamics. To further enhance the harmonic sampling, a multi-rate sampling scheme is also proposed. This scheme performs the harmonic control at a high sampling rate while allowing the fundamental-frequency control to be at the same rate as the PWM or higher rate. The proposed method can be used for both LV and MV high-power VFDs. The performance of harmonic control under local nonlinear loads or background harmonics is verified by the experimental results.

Chapter 3

A modeling method and the corresponding analysis methods are illustrated in this chapter to achieve accurate virtual impedance control with the VSC-based high-power VFD. It is a Linear Periodic Time-Varying (LPTV) system when the multi-rate control structure is applied to a high-power VSC. The conventional discrete-time modeling method can result in modeling errors and affect the accuracy of virtual impedance. Hence, the lifting method is introduced to model the system accurately. The frequency response calculation method is accordingly introduced as well. By comparing the conventional discrete-time model and lifted model, design recommendations are given. The model accuracy is verified with experimental results.

Chapter 4

In Chapter 4, a stair-edge PWM (SEPWM) strategy is proposed to improve floating capacitor voltage balancing for multilevel MV high-power VFDs to avoid the harmonics caused by capacitor voltage ripples. The method can be widely used for all MLCs with incomplete capacitor-voltage-balancing capability (with fundamental frequency ripples on floating capacitors). This PWM method produces multiple output level in one PWM period while keeping the original *dv/dt*, output phase energy, and voltage stress on the switching devices. The method is a carrier-based method and thus very easy to implement. As a general method, the method can be applied to various kinds of MLCs with floating capacitors or unclamped DC-link capacitors. A design example using 4L-NNPC is given in this chapter. The feasibility and performance are verified by experimental results.

Chapter 5

In chapter 5, a new multilevel topology is proposed to obtain high-power quality in MV high-power VFDs. This topology can balance all of its capacitors well and ensure low voltage ripples on floating capacitors. It can, therefore, be applied to VFDs with the ability to operate in a wide speed range. Also, it can be used as an AFE with the ability to balance the DC-link capacitors. A corresponding balancing scheme is proposed to well balance all the capacitors of a seven-level

(7L)-HC VFD. The topology and the balancing scheme are verified by both simulation and experimental results.

Chapter 6

The main conclusions and contributions of this thesis are presented. Also, suggestions for future works are provided.

Chapter 2

Harmonic Sampling and Control Scheme for High-Power Active Front End[1]

Both harmonic current rejection control and harmonic voltage compensation control are required for the AFE in VFD systems. It is necessary to apply control schemes to change the output impedance of AFE flexibly. However, the existing virtual impedance control methods usually adopt cascaded multi-loop control structure, leading to poor dynamics in converters with low switching frequency. The induced significant control delay and low sampling rate can impact the harmonic control performance. Therefore, it is necessary to find suitable virtual-impedance-based harmonic control schemes for high-power AFE.

In this chapter, the existing control schemes aiming at changing output impedance of VSCs, as well as the sampling schemes for VSC control, are reviewed. A new control strategy which can ensure harmonic control performance of high-power AFE will be proposed. The sampling schemes to enhance harmonic control will also be illustrated. Besides, it is worth noting that the control and sampling schemes are applicable for not only VFDs but also all the grid-interfacing VSCs with low switching frequencies.

2.1 Existing Harmonic Control Methods and Sampling Schemes

As discussed, the AFEs should be able to control the equivalent impedance to ensure the power quality under different scenarios: 1) increase equivalent impedance to resist PCC voltage harmonics and produce high-quality output current,

[1] Publication out of this Chapter:

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defined as harmonic current rejection; 2) reduce equivalent impedance to absorb the current harmonics of local nonlinear load and ensure the PCC voltage quality, defined as harmonic voltage compensation. The following two examples illustrate the above two harmonic compensation scenarios:

Firstly, when an AFE is adopted in a high-power VFD, the background harmonics may cause the AFE to produce distorted current, violating the grid codes (such as IEEE 519). Therefore, the ability to reject the interference of background voltage harmonics is necessary for AFE in high-power VFD. The harmonic current rejection control is required in this case.

On the other hand, there could be many local harmonic sources connected to PCC. In this case, the voltage harmonics of PCC should be appropriately compensated to ensure good voltage quality. To do this, it is possible to use AFEs to compensate harmonics in PCC voltage. The harmonic voltage compensation control is required.

To control the impedance and achieve harmonic rejection /compensation control flexibly, both proper harmonic controllers and suitable control scheme should be used.

2.1.1 Harmonic Controllers

(1) Resonant Controller (RSC)

The RSC has theoretically infinite gain at the resonant frequency [29]. Merely setting the resonant frequency at the harmonic orders and connecting multiple RSCs in parallel can realize selective harmonic control [30]. The control gains of each harmonic control branch can be flexibly tuned. However, the computation burden and design complexity will be very high when a wide range of harmonics are required to mitigate. Also, the phase margin of the system becomes small when multiple RSC is applied [31]-[33]. To reduce the number of RSCs required for harmonic control, the RSCs can be applied in the synchronous frame. In this case, for example, 6^{th} order RSC can be used to control 5^{th} and 7^{th} order harmonics. As a result, the number of required RSCs can be halved [34]-[35]. Another challenge is the grid frequency variation [32]-[33], particularly in the weak grid or islanded microgrids. To resist the frequency variation, the RSC can be improved by adaptive

resonant frequency [36] or adding damping term to the denominator of the RSC [36]-[37], expanding frequency range that provides high loop gain.

(2) Repetitive Controller (RC):

The RCs, featuring simple structures, can introduce multiple resonance peaks at integer times of the center frequency in the spectrum, which enable the mitigation of wide-range of harmonics at the integer orders; odd orders [38]-[39], or even selected orders [40]-[43]. Compared to RSCs, the RC requires more memory to store delayed signals, but much less calculation time, which is quantized in [44]. The delay embedded in the controller degrades the transient performance. Moreover, it is difficult to define different loop gains at different harmonic orders, which is important to reshape harmonic impedances for harmonic sharing or stability enhancement. Similar to the RSC, racking errors of RCs are also inevitably affected by the frequency deviation, requiring frequency adoption approaches [45]-[48].

(3) Deadbeat (DB) Controller:

The DB controllers can achieve fast transient and wide-range harmonic control with no special request on calculation capacity or memory. In addition to the harmonics at specific orders, the inter-harmonics can also be controlled. However, the complexity of the DB controller in high-order systems can be a demerit, such as AFEs with LCL filters. In addition, the tracking error is influenced by the variation of system parameters, system delay, dead time, and the error between the stepwise sampling results in digital controllers and the actual continuous system outputs. To address these challenges, different researches have been done to reduce complexity [49], reduce system delay and sampling error [50], compensate the dead-time [51], avoid model mismatch [52]-[55], to name a few.

2.1.2 Existing Harmonic Control Schemes

These aforementioned controllers can be selected according to the requirements of the harmonic control. They can be implemented in three different control methods for the AFEs or any other grid-interfacing VSCs: current control method (CCM), voltage control method (VCM), and hybrid control method (HCM).

In the following text, these control options in accompany with implementation examples are explained.

A. Harmonic compensation with current control method (CCM)

The AFE with CCM has a high impedance at the fundamental frequency as the converter behaves like a current source (see Figure 2.1), and it is convenient to add harmonic controllers to mitigate harmonics [56]-[60]. With the harmonic controllers, the current reference is generated according to the control targets—harmonic current rejection and harmonic voltage compensation:

Harmonic Current Rejection: A pure sinusoidal current reference will be applied to the harmonic controllers to eliminate output current harmonics [59]-[61].

Harmonic Voltage Compensation: The AFE should be controlled as a shunt active power filter to absorb current harmonics [56]-[58], [62].

In Figure 2.1, a typical individual AFE's control block diagram with CCM harmonic compensation is shown.

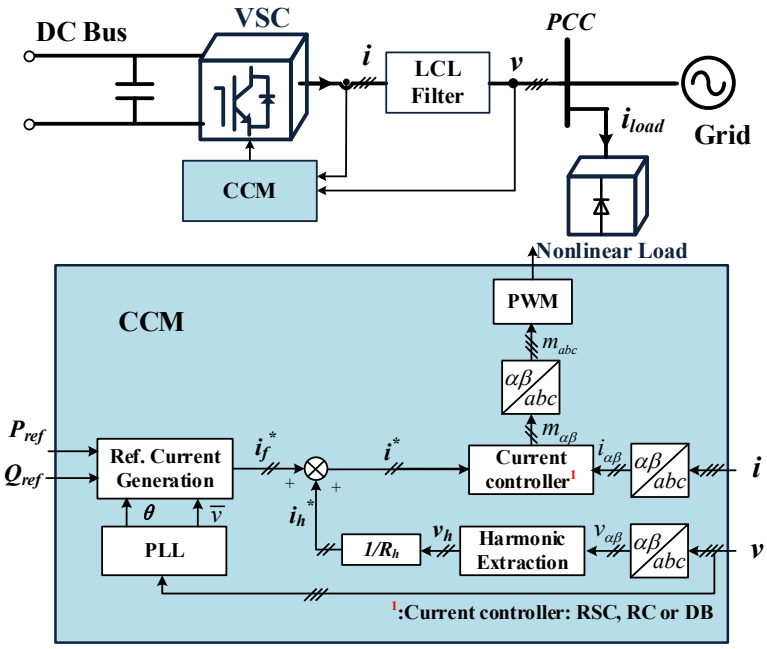

Figure 2.1 A typical VSC control block diagram with CCM harmonic compensation

In this example, the AFE connected to PCC is used to compensate harmonics with CCM. As seen in Figure 2.1, the fundamental current reference i_f^* in CCM is

derived by the output power control while the harmonic current reference i_h^* is calculated by the PCC voltage harmonics v_h and a virtual resistor R_h. Then the total current reference i^* can be calculated as follows:

$$i^* = i_f^* + i_h^* = i_f^* + v_h / R_h \tag{2.1}$$

Thus, the harmonic currents of the nonlinear loads are absorbed by the AFE to compensate the voltage harmonics of PCC. With RSC, RC, or DB controllers applied as the current controller, and the harmonic compensation reference can be executed.

Compared to directing the load harmonic current to the current reference and absorbing all the harmonic current of the nonlinear load (R_h=0), the CCM can flexibly define the harmonic compensation efforts according to available power ratings of VFDs. This also enables harmonic current sharing among multiple VFDs by tuning the R_h.

B. Harmonic compensation with voltage control method (VCM)

In the VCM-based method (see Figure 2.2), the harmonic compensation is added to the voltage feedback control. The voltage control can be applied in islanded AC systems [64]-[66], grid-connected conditions [63], [67]-[68], and in the unified control under both grid-connected and islanded conditions [69]-[71]. Another advantage of VCM-based harmonic compensation is the ability to follow given voltage amplitude and frequency references from droop controller [72]-[73] or virtual synchronous generator controller [74]-[75].

Generally, an RSC, RC, or DB controller can be used as the voltage controllers to directly regulate output voltages of AFEs. To obtain better dynamics, an inner current loop which regulates the inverter-side current can be added. However, as the grid-side current is not controlled in VCM, it is sensitive to PCC voltage disturbances. A typical individual AFE's control block diagram with voltage control method harmonic compensation is shown in Figure 2.2.

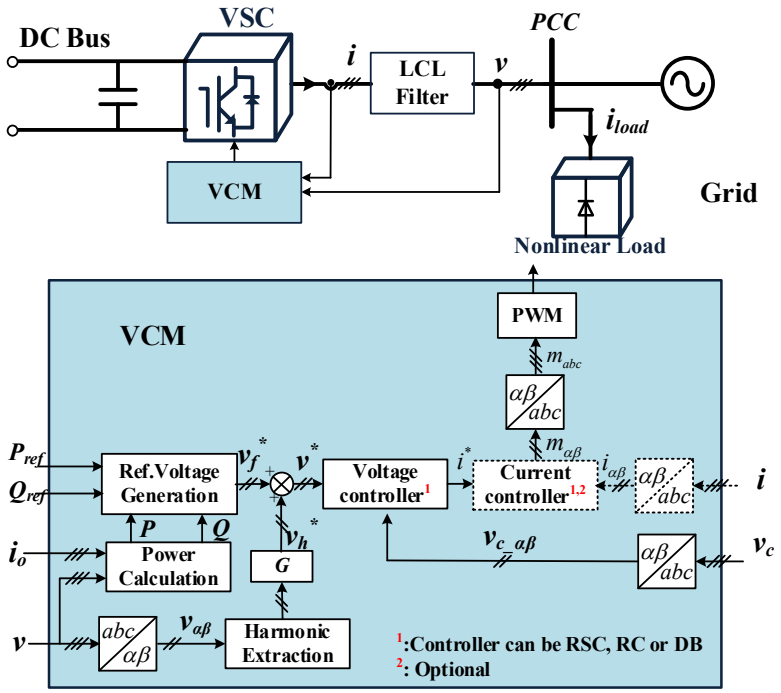

Figure 2.2 A typical individual AFE control block diagram with VCM harmonic compensation

In this example [63], voltage harmonics of PCC are feed-forwarded to the voltage control reference with a gain G. The equivalent harmonic impedance at the converter side Z_{AFE_eq} can be expressed as (2.2):

$$Z_{AFE\_eq} = Z_{AFE} / (1+G) \tag{2.2}$$

where the Z_{AFE} is the original impedance without harmonic compensation. When the feed-forward gain G is positive, the harmonic can be absorbed by AFE as its impedance is reduced. On the other hand, a negative gain G will lead to a large impedance of AFE, enforcing sinusoidal output current, like [77].

In general, when the VCM-based harmonic compensation is applied, AFE works as an L-APF (an active power filter (APF) with pure inductive output impedance) as the AFE impedance, and the grid impedances are mainly inductive at harmonic frequencies. However, it is possible to control AFE to be an R-APF (an APF with pure resistive output impedance) because G can be a real, imaginary, or complex number [78].

C. Harmonic compensation with hybrid control method (HCM)

Compared to VCM and CCM, the HCM can simultaneously control AFEs' output voltage, and current as the parallel control structure is used [79]-[80]. In general, in VCM and CCM-based harmonic compensation, the converter-side inductor current control with a proportional controller is employed as the inner loop, and the outer voltage or current control loop (assuming LCL filter; to control capacitor voltage or grid-side current) usually uses multiple RSCs (with different resonant frequency) in parallel to control the harmonics (see Figure 2.3). However, the HCM transforms the cascaded structure of double-loop controller in CCM and VCM-based harmonic compensation into a single-loop parallel structure. In detail, there are two independent control branches in parallel in the HCM: closed-loop control of AFE's output voltage (filter capacitor voltage) and closed-loop control of current.

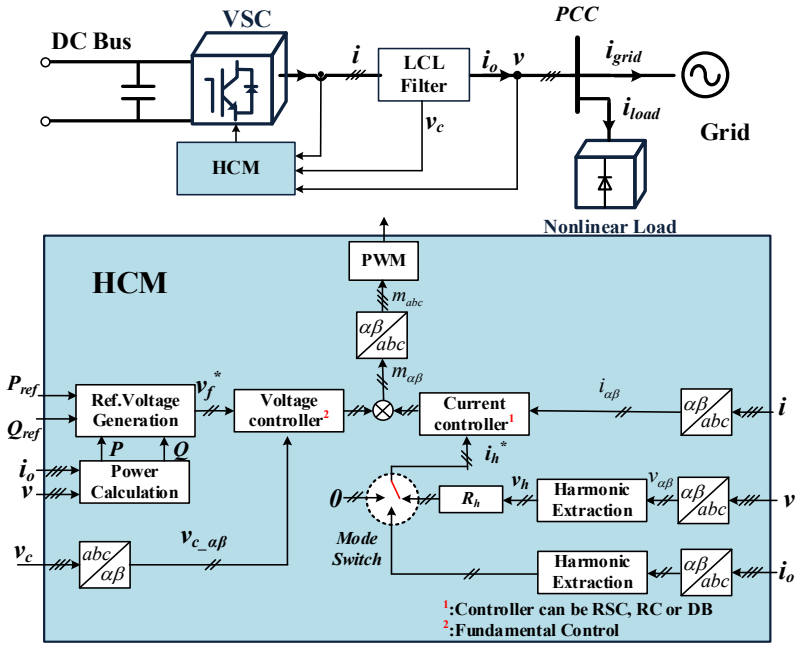

Figure 2.3 A typical individual AFE control block diagram with HCM harmonic compensation

Harmonic Voltage Compensation: If the current control reference is selected as $-H_D(s)V_{PCC}/R_V$, where R_V is the virtual resistance and $H_D(s)$ is the band-pass filter

to extract the harmonics, the PCC voltage V_{PCC} can be improved. The AFE works as an R-APF in this mode.

Harmonic Current Rejection: The control target can also be set to reject the current harmonics. The harmonic current reference should be set to zero in this mode.

2.1.3 Existing Sampling Methods for VSC Control

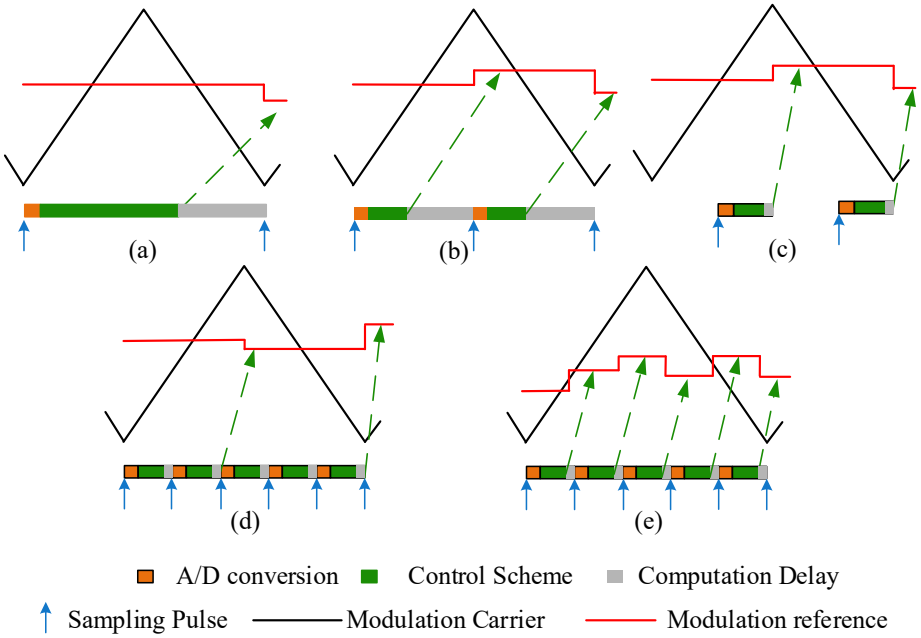

Figure 2.4 Different sampling and PWM methods: (a) synchronous sampling with single-update PWM; (b) synchronous sampling with double-update PWM; (c) real-time computation with double-update PWM; (d) oversampling with double-update PWM; (e) oversampled control and PWM

Harmonic control performance can be significantly impacted by the sampling rate and processing delay [81], particularly in high-power VSCs with low switching frequencies (e.g., 2 kHz), where the synchronous sampling methods, shown in Figure 2.4(a) and Figure 2.4(b), are used. To obtain high-performance harmonic control in low-switching-frequency converters, different sampling and PWM update methods can be adopted. The real-time computation [82]-[83](Figure 2.4(c)) can reduce the processing delay while the sampling rate of harmonics cannot be increased. The oversampling/multisampling method can simultaneously increase

the sampling rate and reduce control delay, as shown in Figure 2.4(d) and Figure 2.4(e). Modulation reference can be updated immediately [84] or updated in each PWM period [85]. However, these methods are hard to apply for a control system with high computation burden, which is common for grid-interfacing VSCs [86]-[87]. Also, the sampling methods in Figure 2.4(c)-(e) are no longer synchronous sampling methods. The average values cannot be directly sampled from the current/voltage with switching frequency ripples. The impact is significant in oversampling methods as the ripples can be sampled and cause periodic fluctuations. As a result, the inverter side current with large ripples (20%-40% of rated current) cannot be taken in the feedback loop unless extra measures are taken to obtain average values. Hence, using different sampling rate in a control system becomes an option. For example, [88]-[90] keeps the synchronous sampling for the fundamental-frequency control while uses low sampling rate for the harmonic compensation to reduce computation burden. The harmonic control performance is degraded to ensure the whole control strategy can be finished in one sampling period. However, in low-switching-frequency converters, these methods shall not be employed as the major challenge is the insufficient sampling rate and large control delay instead of the computation burden.

2.2 Proposed Feed-Forward Harmonic Control Schemes

A typical structure of AFE is shown in Figure 2.5. The DC-link of VFD is connected to the AC grid through a VSC. An LCL filter, constructed by L_1, L_2, and C, is used to filter out high-frequency harmonics. The nonlinear loads are also connected to the grid, injecting harmonics to the system. The resistors R_1 and R_2 denote parasitic resistors. R_d is the resistor for passive damping. Moreover, Z_g represents the grid impedance.

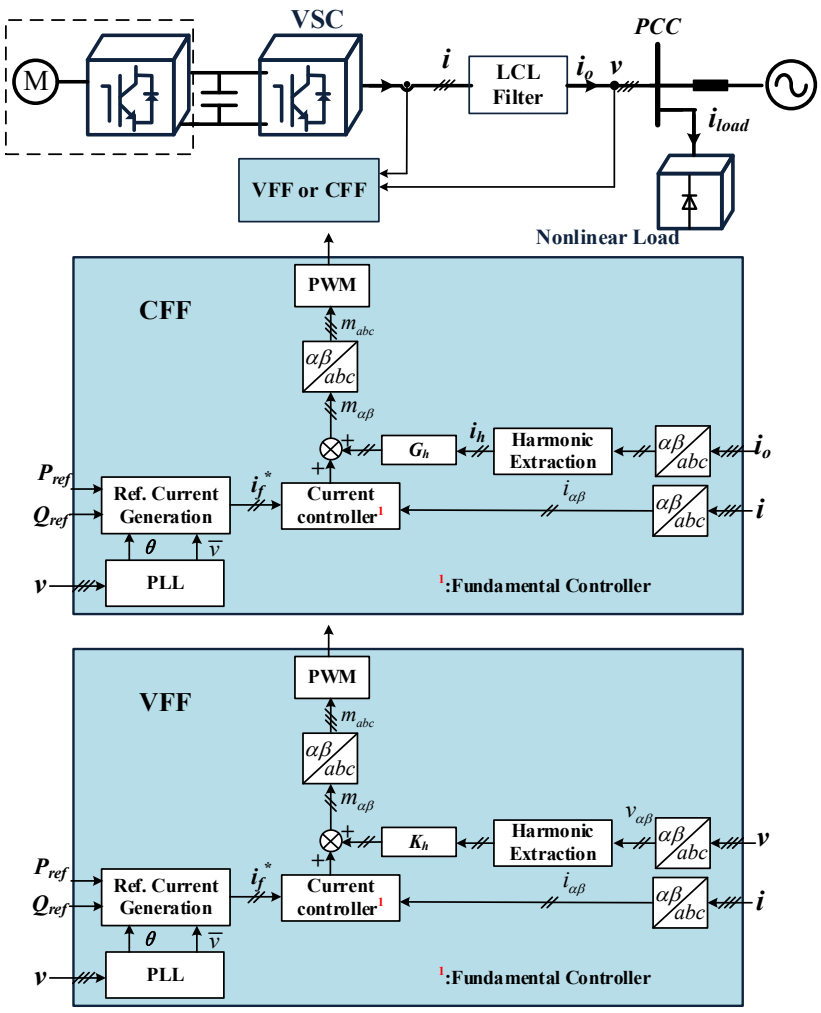

Figure 2.5 Feed-forward harmonic control schemes

Two control methods to do the harmonic control are also shown in Figure 2.5. The harmonic currents (or the harmonic voltages) are fed forward to the modulation references with designed gain G_h (or K_h). To realize the control strategies, the output currents (or PCC voltages) are transformed into the α-β orthogonal coordinate, in which it is possible to construct the complex coefficient G_h (or K_h). The harmonics in currents (or voltages) are obtained by harmonic extraction modules, which usually are band-pass filters. Then the extracted harmonics are amplified by the complex gain G_h (or K_h) and transformed back to the a-b-c stationary frame. Finally, they are added to modulation references. As the regulated signals are directly added into the modulation references, neither extension of the controller bandwidth nor extra high bandwidth controller is necessary for the feedback loop. As a result, the feed-forward control is not limited by the feedback control bandwidth.

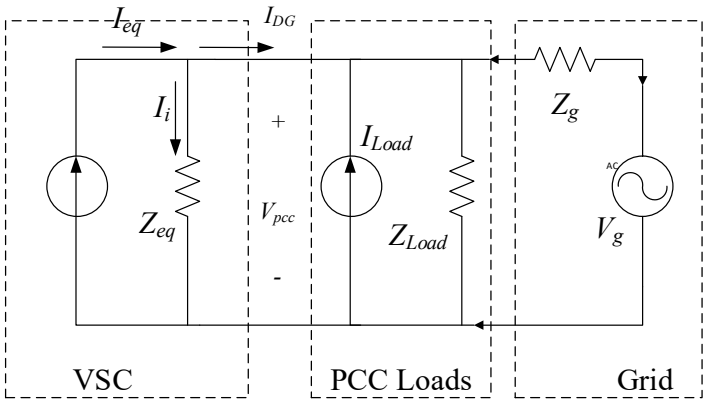

Figure 2.6 Equivalent model of a VFD system

The equivalent circuits of the VSC and the whole system are shown in Figure 2.6. Since the AFE typically employs the current control method as the inner control loop, the Norton Equivalent Method is adopted in the analysis. The nonlinear load is modeled as a harmonic current source in parallel with an impedance that accounts for fundamental frequency power [91]-[92].

Based on Norton equivalent circuit theory, the equivalent current I_{eq} and equivalent impedance Z_{eq} in Figure 2.6 can be easily obtained as in (2.3)-(2.4).

$$Z_{eq}(s) = \frac{Z_{L1}(s)Z_{L2}(s) + Z_{L1}(s)Z_C(s) + Z_{L2}(s)Z_C(s)}{Z_{L1}(s) + Z_C(s)} \tag{2.3}$$

$$I_{eq}(s) = \frac{Z_C(s)}{Z_{L1}(s)Z_{L2}(s) + Z_{L1}(s)Z_C(s) + Z_{L2}(s)Z_C(s)} V_{inv}(s) \tag{2.4}$$

where $Z_{L1}(s)$, $Z_{L2}(s)$, $Z_C(s)$ represent the impedances of the branches of L_1, L_2, C in Laplace domain respectively; $V_{inv}(s)$ can be seen as the output voltage of the three-phase bridge when averaged linear model [93] is applied.

Using current feed-forward (CFF) method, the output harmonic voltage at VSC output terminal V_{inv_h} is determined by harmonic in output current I_{O_h} and the feed-forward gain G_h, as shown in(2.5).

$$V_{inv\_h}(s) = -G_h \cdot I_{O\_h}(s) \tag{2.5}$$

However, in a low-switching-frequency VSC system, the system delay would be a significant factor that influences the current harmonic phase angle. Although

the gain of feedback fundamental-frequency control loop at harmonic frequency is small, the coupling to the output harmonic still exists. Taking these two factors into consideration, (2.5) can be rewritten as (2.6).

$$V_{inv\_h}(s) = -G_h \cdot I_{O\_h}(s) \cdot e^{-T_d s} - G_{PR}(s) \cdot e^{-T_d s} I_{O\_h}(s) \tag{2.6}$$

where T_d denotes the system delay.

Substituting (2.6) to (2.4) and modifying it to express the harmonic current I_{eq_h}, the result is as (2.7).

$$I_{eq\_h}(s) = \frac{-G_h \cdot Z_C(s) \cdot e^{-T_d s} - G_{PR} \cdot Z_C(s) \cdot e^{-T_d s}}{Z_{L1}(s)Z_{L2}(s) + Z_{L1}(s)Z_C(s) + Z_{L2}(s)Z_C(s)} I_{O\_h}(s) \tag{2.7}$$

From Figure 2.6, it is easy to find out:

$$I_{eq\_h}(s) = \frac{V_{PCC\_h}(s)}{Z_{eq}(s)} + I_{O\_h}(s) \tag{2.8}$$

Substituting (2.7) to (2.8), the equivalent harmonic impedance Z_V, or in other words, the virtual impedance of VSC can be acquired, as shown in (2.9).

$$Z_V(s) = -\frac{V_{PCC\_h}(s)}{I_{O\_h}(s)} = (1 + \frac{G_h \cdot Z_C(s) \cdot e^{-T_d s} + G_{PR}(s) \cdot Z_C(s) \cdot e^{-T_d s}}{Z_{L1}(s)Z_{L2}(s) + Z_{L1}(s)Z_C(s) + Z_{L2}(s)Z_C(s)}) Z_{eq}(s) \tag{2.9}$$

As an alternative method, when the PCC voltage is taken as the feed-forward variable, the output harmonic voltage at VSC output terminal is defined as (2.10).

$$V_{inv\_h}(s) = -K_h \cdot V_{PCC\_h}(s) \cdot e^{-T_d s} - G_{PR}(s) \cdot e^{-T_d s} \cdot I_{O\_h}(s) \tag{2.10}$$

Substituting (2.10) to (2.4), and considering that (2.8) is still applicable for VFF approach, (2.11) can then be obtained. Therefore, when the PCC voltage feed-forward method is applied, the equivalent harmonic impedance of VSC Z_V is expressed as (2.11).

$$Z_V(s) = -\frac{V_{PCC\_h}(s)}{I_{O\_h}(s)} = \frac{(1 + \frac{G_{PR}(s) \cdot Z_C(s) \cdot e^{-T_d s}}{Z_{L1}(s)Z_{L2}(s) + Z_{L1}(s)Z_C(s) + Z_{L2}(s)Z_C(s)})}{(1 + \frac{K_h \cdot Z_C(s) \cdot e^{-T_d s}}{Z_{L1}(s) + Z_C(s)})} Z_{eq}(s) \tag{2.11}$$

It can be concluded that the equivalent output impedance Z_V, i.e., the virtual impedance of the VSC, can be changed by the feed-forward gain K_h or G_h according to (2.11) and (2.9)respectively. Assuming all the harmonic currents in the system are injected by the nonlinear loads when Z_V is increased, i.e., the harmonic equivalent impedance is increased on the VSC-side, the VSC will resist the grid background harmonics and maintain the high VSC output current quality. On the other hand, when Z_V is decreased, the harmonic current will be absorbed by the VSC. In this case, the voltage at PCC will be improved even local nonlinear loads are connected. Therefore, whether to improve the VSC output current quality (harmonic rejection) or to improve the PCC voltage quality (harmonic compensation) can be flexibly determined by designing the virtual impedance, according to the system requirement.

However, the relationship derived above cannot be used to accurately design the impedance accurately as many simplifications are made: 1) continuous-time modeling is used, and the actual frequency response near Nyquist frequency will have significant errors; (2) the multi-rate sampling scheme cannot be modeled, and the system can only be treated as a system with constant delay, which mismatches the actual control system if non-synchronous sampling method is used. But still, the equations can be used to estimate the compensation or rejection performance.

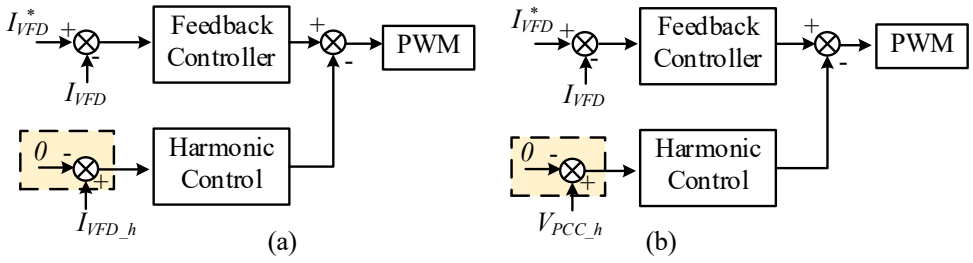

Figure 2.7 Comparisons of proposed control structures with feedback harmonic control methods: (a) current-based control; (b) voltage-based control

In addition, it is worth to note that the structures of CFF for harmonic rejection and the VFF for harmonic compensation are similar to feedback loops for harmonic control with reference as zero, as shown in Figure 2.7(a) and Figure 2.7(b) respectively. However, the physical meanings of VFF and CFF are much more

explicit than feedback control methods. With the physical meaning developed, VFF and CFF aim at changing the equivalent output impedance while the feedback control methods aim at eliminating tracking errors (tracking zero references and therefore losing the flexibility of harmonic control).

2.3 Improved Sampling Schemes

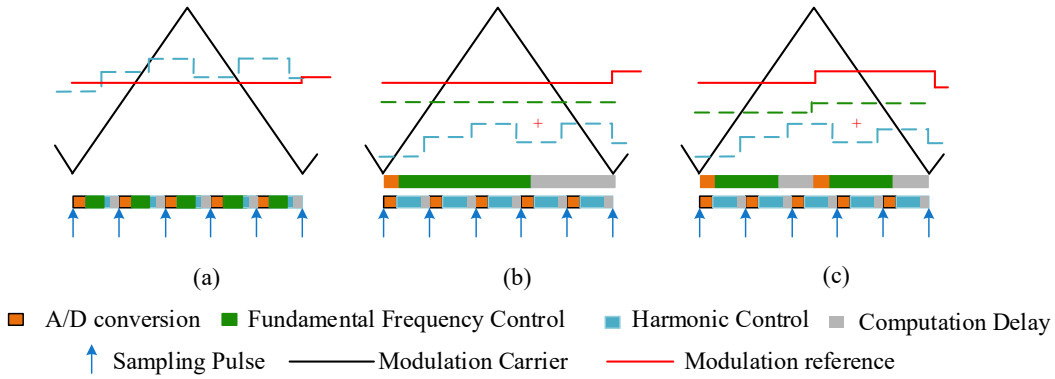

Figure 2.8 Proposed sampling schemes: (a) proposed high-rate control with regular sampled PWM; (b) proposed multi-rate sampling with single-update PWM; (c) proposed multi-rate sampling with double-update PWM

For low-switching-frequency VSCs, three sampling schemes can be used to improve the harmonic control performance. One can increase the sampling rate of both fundamental-frequency control and harmonic control while performing the low rate PWM, as shown in Figure 2.8 (a). This way can effectively reduce the processing delay and increase the sampling rate. Also, due to the regular sampled PWM is still used, the multiple switching can be avoided within one PWM period.

Considering the synchronous sampling is actually sufficient for fundamental-frequency control, the sampling rate can be reduced for the fundamental-frequency control while using high sampling rate for harmonic control, as shown in Figure 2.8(b) and Figure 2.8 (c). In this case, the fundamental-frequency control scheme can take control variables with large ripples, like converter-side current I_1, making it possible to select fundamental-frequency control schemes flexibly. On the other hand, the harmonics can be sampled with a high rate and low delay from PCC, where both the voltage and current contain low ripples.

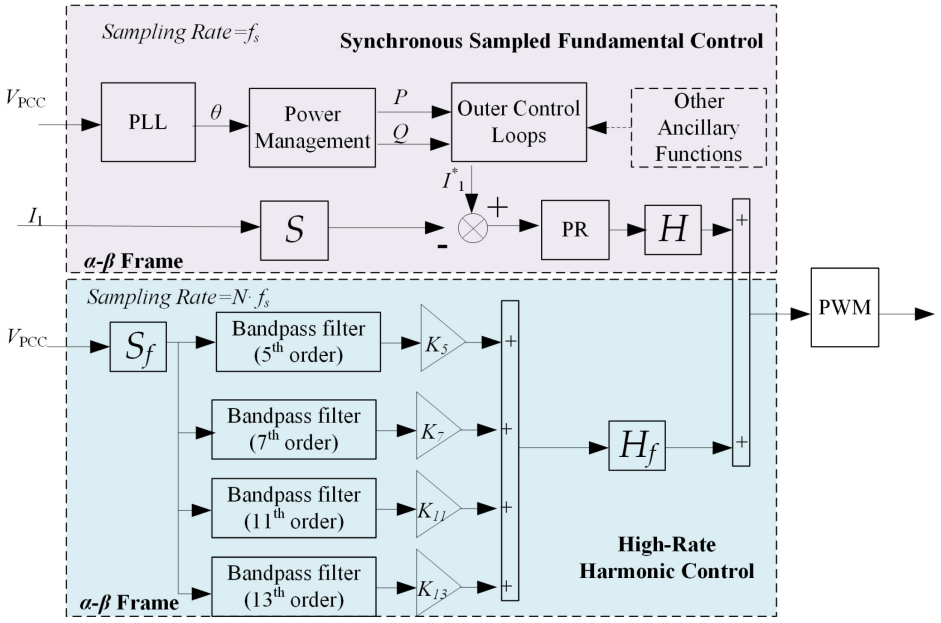

Figure 2.9 Multi-rate harmonic control scheme

As an example, the sampling method in Figure 2.8 (b) are applied to the VFF control, which is shown in Figure 2.9. The fundamental current control, which is implemented at the switching frequency, is realized in the *α-β* frame with Proportional Resonant (PR) controllers to eliminate the errors at the fundamental frequency. Thanks to the synchronous sampling, the average value of inverter side current I_1 is sampled, and the large ripples (20%-40% of rated current) can be screened for the controller. Outer loops, such as power control, droop control, can be added up to the inner current loop to achieve power control or some other ancillary functions. As the synchronous sampling can effectively fulfill the requirement of the fundamental-frequency control, keeping the fundamental-frequency control at a low sampling rate will not impact the control performance.

In this example, the sampling rate is increased to N times of the switching frequency for the harmonic control. To control up to 13th order harmonics, N is set as 5 in this work, by which 10kHz sampling can be used in a converter with 2kHz switching frequency. With LCL filter applied, both the grid-side current I_2 and voltage V_{PCC} contains low ripples, and the high rate control will not be affected by the sampled ripples. Based on the sampling results, the harmonic components in

PCC voltages are obtained by harmonic extraction modules, which are band-pass filters in this work. The extracted harmonic voltages are fed forward to the modulation references with designed gain K_h. To realize the control strategy, the AC voltages are transformed into the α-β orthogonal coordinate, in which it is possible to construct the complex coefficient K_h. The regulated harmonic control signals are transformed back to the *a*-*b*-*c* stationary frame and finally added to the modulation references. With the feed-forward control, the equivalent harmonic impedance on the VSC side can be controlled.

It is worth noting that although the sampling rate is increased for harmonic control, the low rate PWM still limits the Nyquist frequency of the whole control system. For a 2 kHz converter, the Nyquist frequency is 1 kHz if symmetrical PWM is used. When the fundamental frequency is 60Hz, the harmonic higher than 17th order harmonics (1020 Hz) cannot be controlled. Hence, in this chapter, the 2 kHz converter is used to control 5th, 7th, 11th, and 13th order harmonics to validate the improved sampling scheme.

2.4 Experiment Verification

To compare the control performance and model accuracy, a VSC prototype with 2kHz switching frequency is built, which is shown in Figure 2.10.

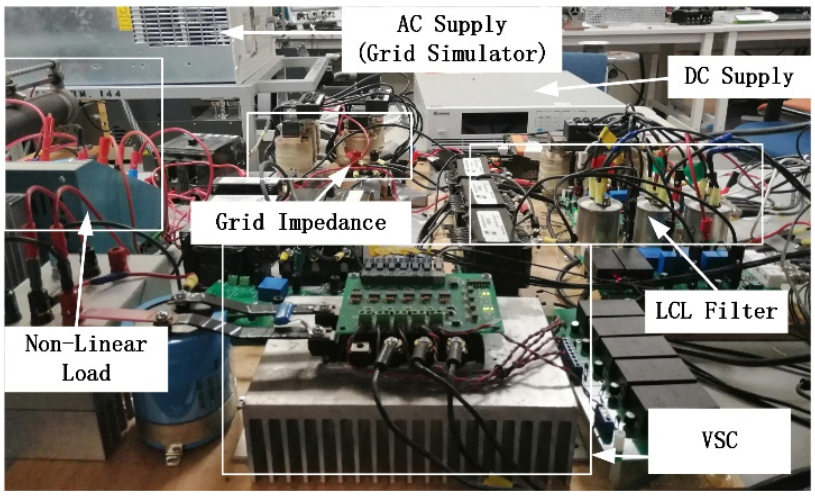

Figure 2.10 Experimental prototype

2.4.1 Verification of Control Schemes

In this part, the control performance of the VFF and CFF under different control modes are validated. The system parameters are shown in TABLE 2.1. Focusing on the control scheme, the harmonic controllers are only applied for 5th and 7th order harmonic. The control parameters applied in the experiment are shown in TABLE 2.2. Here, the sampling scheme in Figure 2.8 (a) is used.

TABLE 2.1 System Parameters Used for Control Scheme Verification

Parameters	Values
LCL Filter	L_1=2.5 mH,L_2=2.5 mH, C=40 μF, R_1=0.1 Ω, R_2=0.1 Ω, R_C=1 Ω
Grid Impedance	L_g=5 mH, R_g=0.22 Ω,
Grid Voltage	110 V/60 Hz
Switching Frequency	2 kHz

TABLE 2.2 Harmonic Control Parameters

	Operation Mode	5th order		7th order	
		Estimated Z_V	K_h or G_h	Estimated Z_V	K_h or G_h
VFF	Harmonic Rejection	80∠135°	0.6∠138°	65∠130°	0.3∠-100°
	Harmonic Compensation	1.1∠110°	5∠0°	5∠110°	1∠0°
CFF	Harmonic Rejection	80∠135°	50∠180°	60∠110°	16∠180°
	Harmonic Compensation	1.1∠120°	5.8∠-86°	5∠110°	5.5∠-70°

Figure 2.11 shows the harmonic rejection operation by VFF method. As can be seen, the transient process is very smooth when the method is applied. The distorted output current becomes sinusoidal. It is easier to observe from the zoomed-in view of these. The FFT analysis further shows the current quality improvement, which is shown in Figure 2.12. The current THD drops from 9.21% to 4.44%. Wherein, the 5th order harmonic drops from 7.8% to 1.6% and 7th order harmonic drops from 2.5% to 0.7%. The harmonic rejection is quite effective.

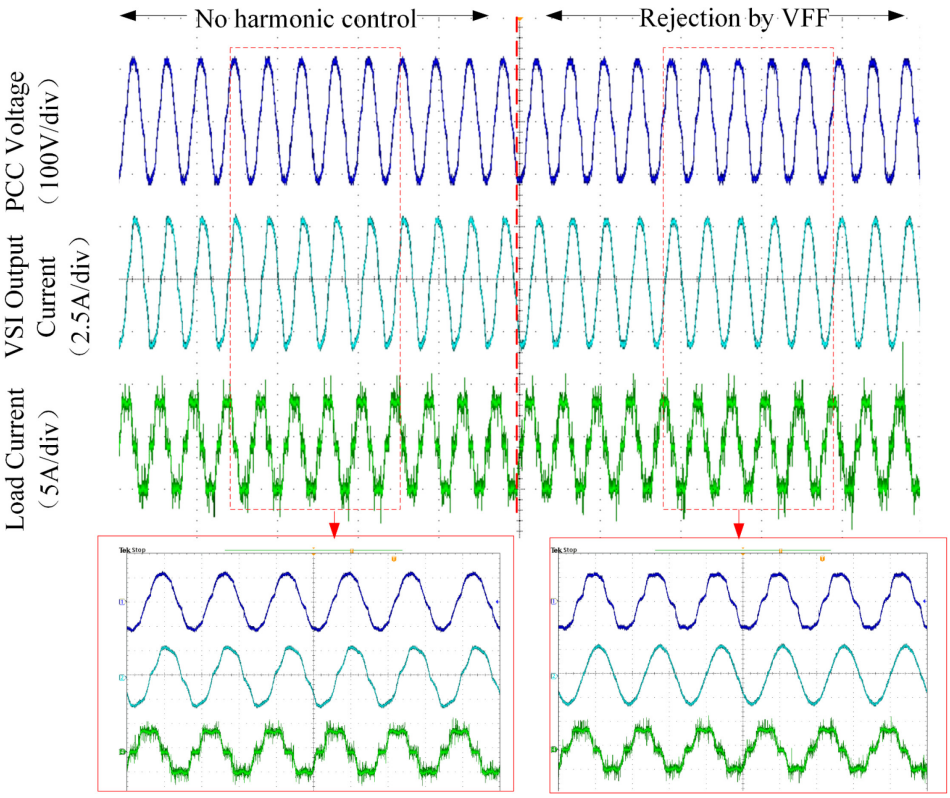

Figure 2.11 Harmonic rejection with VFF

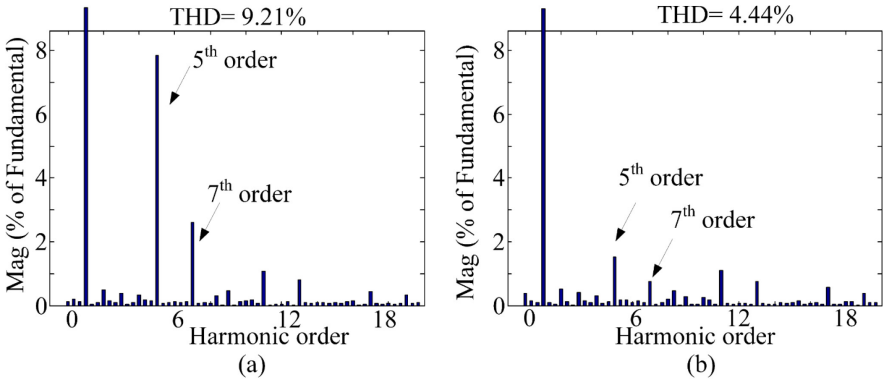

Figure 2.12 FFT analysis of output current: (a) no harmonic control; (b) harmonic rejection by VFF

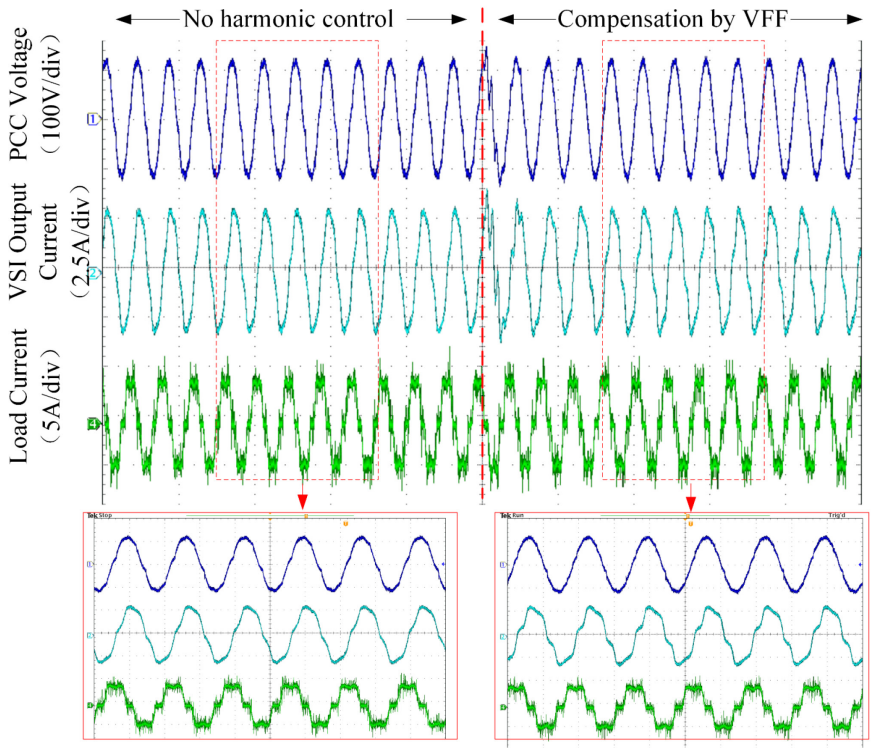

Figure 2.13 Harmonic compensation with VFF

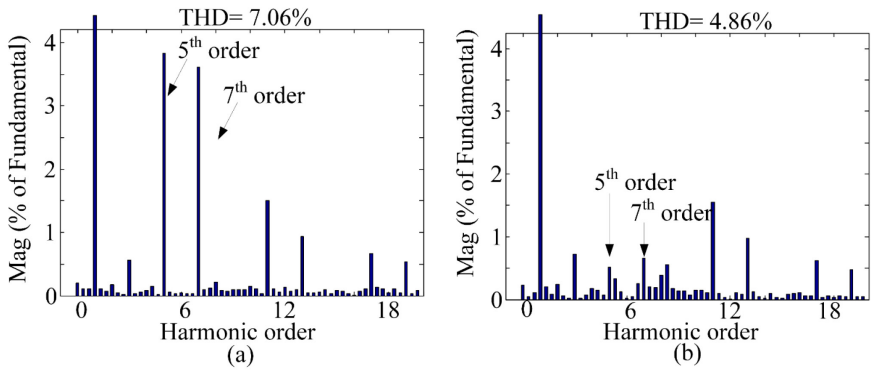

Figure 2.14 FFT analysis of the PCC voltage: (a) no harmonic control; (b) harmonic compensation by VFF

When the virtual impedance is set to be a small value, the VFF control system turns to realize harmonic compensation, i.e., improve the PCC voltage. As can be seen from Figure 2.13, the distortion of PCC voltage is reduced significantly after a short transient process. The zoomed-in view shows more distorted output currents are absorbed by the VSC so that the PCC voltages become less distorted. The FFT analysis in Figure 2.14 shows that the THD of PCC voltage is reduced from 7.06%

to 4.86% because of the 5th order harmonic and 7th order harmonic is significantly compensated. Both are reduced from nearly 4% to no more than 1%.

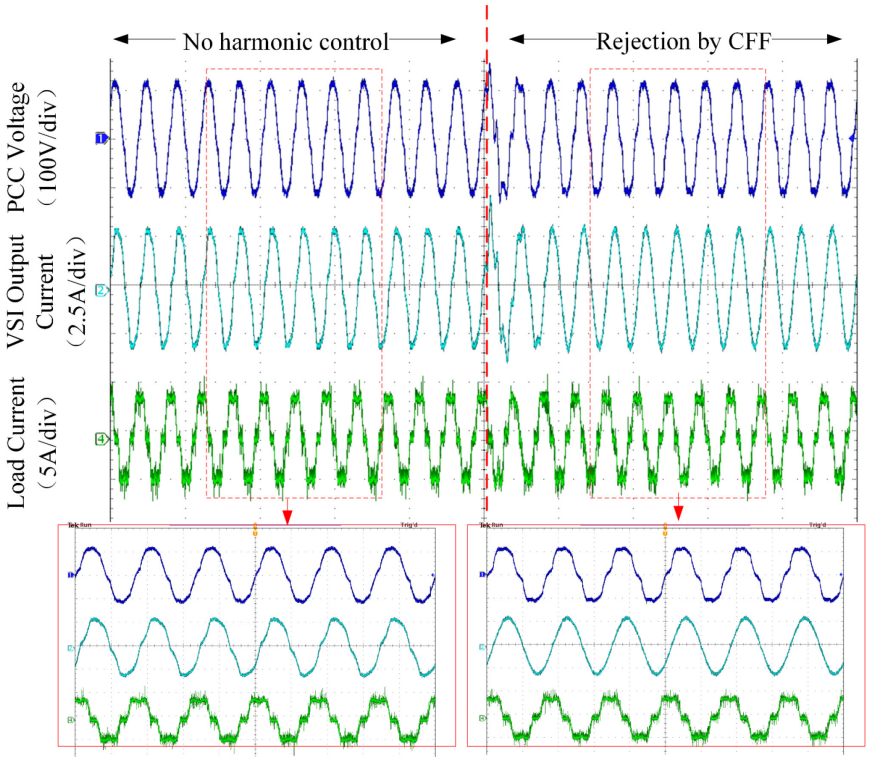

Figure 2.15 Harmonic rejection with CFF

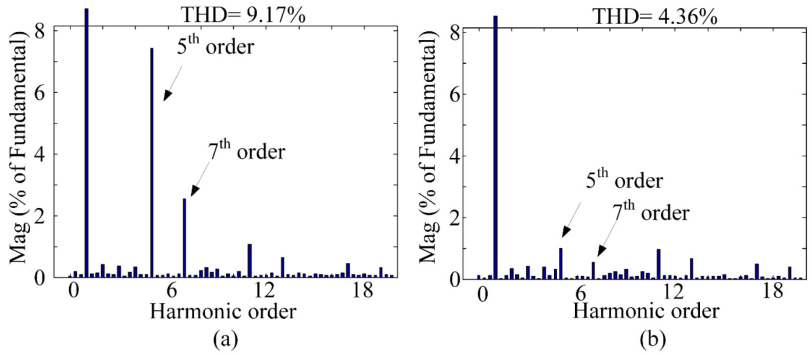

Figure 2.16 FFT analysis of output current: (a) no harmonic control; (b) harmonic rejection by CFF

CFF method has similar performance under different virtual impedance configuration. In Figure 2.15, after the CFF starts to operate, the current quality is improved by enlarging the 5th order and 7th order virtual impedance. Besides, a short regulation duration can be observed. The current quality improvement can also be

easily seen from the zoomed view in Figure 2.15. The FFT analysis in Figure 2.16 further proves the effectiveness, which shows that the 5th order harmonic is reduced from about 7.5 % to 1.2% and 7th order harmonic is reduced from 2.5% to 0.7%, improving the output current THD from 9.17% to 4.36%.

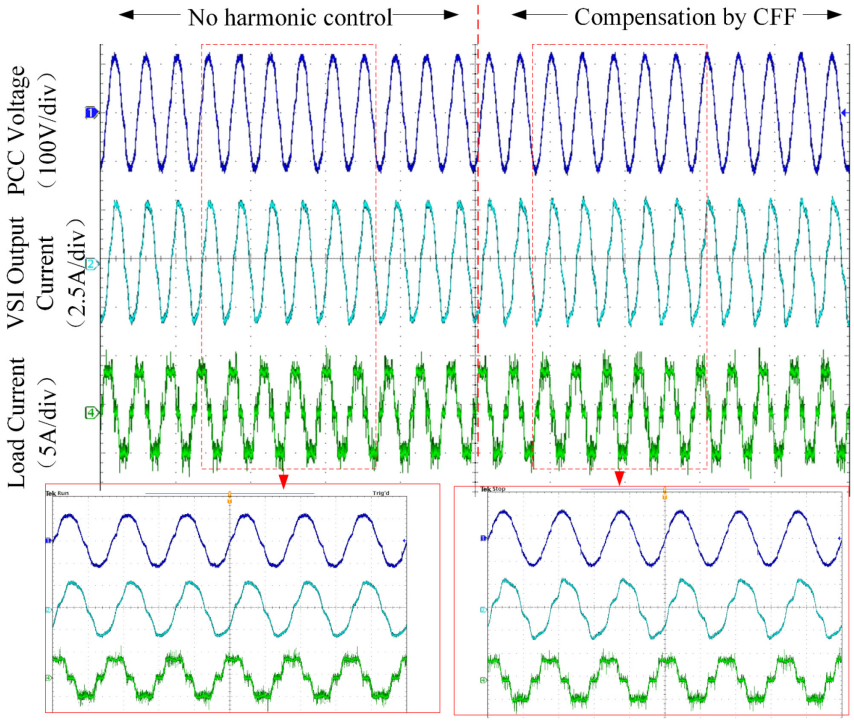

Figure 2.17 Harmonic compensation with CFF

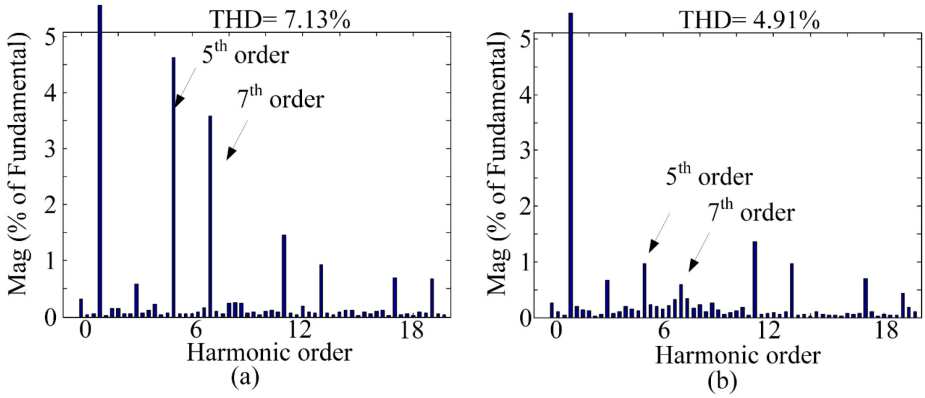

Figure 2.18 FFT analysis of the PCC voltage: (a) no harmonic control; (b) harmonic compensation by CFF

When the virtual impedance is configured to be small, CFF is also able to compensate the PCC voltage harmonics, as shown in Figure 2.17. A smooth

transient can be seen when the compensation starts. Meanwhile, the voltage quality improvement can be seen from the zoomed-in view: a sinusoidal PCC voltage appears after CFF is applied. According to the FFT analysis in Figure 2.18, the 5th and 7th order harmonics are attenuated, being decreased from around 4% to approximately 0.5%.

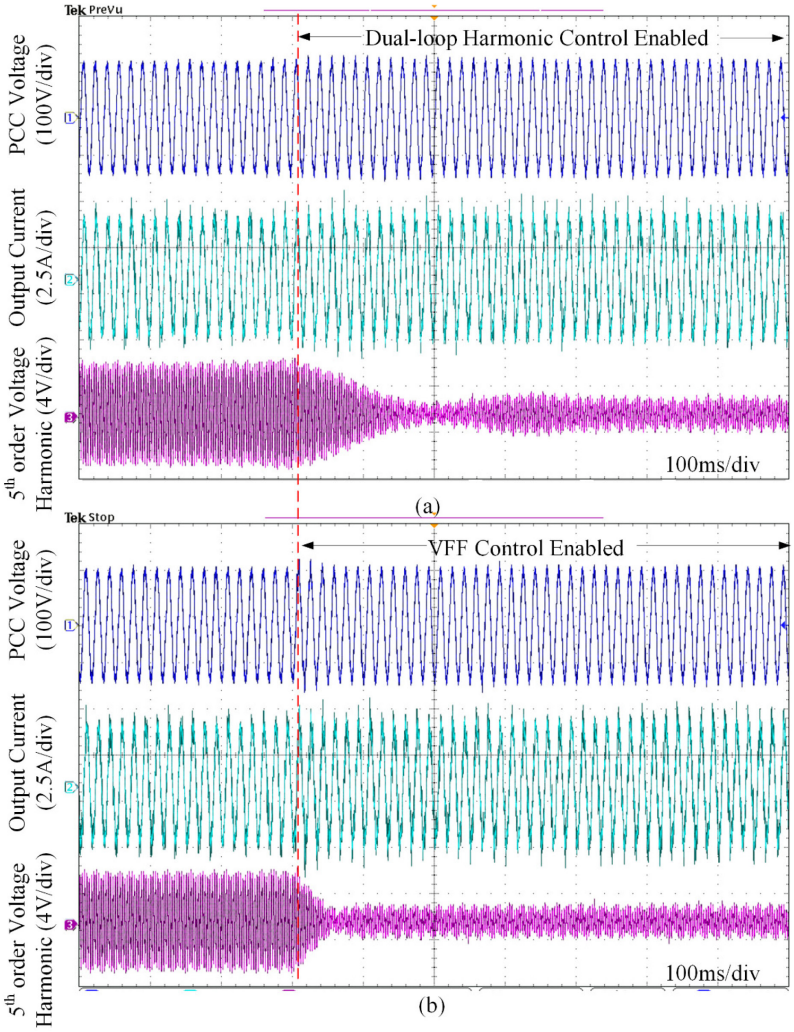

Figure 2.19 Transient response comparison: (a) conventional dual closed-loop control; (b) VFF method

From the experiments, it can be noticed that there are short transient responses under the harmonic compensation by VFF and harmonic rejection by CFF. This phenomenon indicates the system is underdamped. The reason is that: to obtain low virtual impedance by VFF or high virtual impedance by CFF, the applicable control parameters usually set the poles close to the imaginary axis, meaning the damping

ratio of the system is low. On the contrary, smooth transient can be observed under harmonic compensation by CFF and harmonic rejection by VFF. This is consistent with the analysis earlier: the CFF for harmonic compensation and VFF for harmonic rejection have better stability performance.

In addition, the comparison of the transient response between the conventional harmonic control and the proposed method is shown in Figure 2.19. The traditional voltage harmonic compensation method [63] employs multi-resonance controllers in both the inner current loop and outer voltage loop. Due to the low switching frequency, the loop gains should be limited to maintain stability for the conventional dual-loop control. Then the same loop gains are used in VFF. The amplitudes of 5^{th} order voltage harmonics under the two different methods are thus almost the same. However, as shown in Figure 2.19 (a) and Figure 2.19 (b), the transient response of VFF is much faster than the dual-loop control. The proposed methods have faster responses as the feed-forward path is employed for harmonic control.

2.4.2 Comparison of Sampling Schemes

To compare the control performance of the multi-rate sampling scheme and conventional single-rate sampling scheme, the VFF control is taken as an example. Also, to better demonstrate the benefits brought by the multi-rate samplings scheme, the LCL filter design is changed. Different from the general design, the LCL filter used here has a resonant frequency above 13^{th} order so that AFEs can effectively control the 11^{th} and 13^{th} order harmonics. The system parameters are shown in TABLE 2.3

TABLE 2.3 System Parameters Used for Sampling Scheme Comparisons

Parameters	Values
L_1	1.6 mH
L_2	1 mH
C	40 μF
Z_g	1.6mH, 0.2Ω
Switching Frequency fs	2 kHz
Sampling Frequency N·fs	10 kHz (N=5)

As the control performance of Figure 2.8(a) has been shown in the previous section, the sampling scheme in Figure 2.8 (b) is used. This scheme is expected to have the worst performance among the three schemes in Figure 2.8. Hence its performance can sufficiently prove the advantages of the proposed method over the traditional sampling schemes. To make fair comparisons, the control parameters are also the same in both the control system with multi-rate sampling and single-rate sampling. As the sampling rate of PWM still limits the maximum available bandwidth, the harmonic control is applied to harmonics from 5^{th} order to 13^{th} order. The control parameters are shown in TABLE 2.4.

TABLE 2.4 Control Parameters Used in Experiment

Parameters	Values
Fundamental PR controller K_P	3
Fundamental PR controller Kr	500
5^{th} order control gain K_5	-8
7^{th} order control gain K_7	-8
11^{th} order control gain K_{11}	-3.8
13^{th} order control gain K_{13}	-3.8

Figure 2.20 shows the steady-state waveforms under different sampling methods. As can be seen in Figure 2.20(a), when no harmonic compensation control is used, the nonlinear load can cause distortions in PCC voltage and current at both VSC-side and grid-side. The FFT analysis in Figure 2.21(a) and (b) shows that the THD of the PCC voltage is 6.6%, and the THD of the grid-side current is as high as 11.51%. With the multi-rate sampling, an AFE can generate the compensation currents, mitigating voltage distortions of PCC, as shown in Figure 2.20 (b). As a result, according to Figure 2.21 (c) and (d), the THD of PCC voltage drops to 4.32% and the grid-side current can also meet the grid code with the THD of 4.87%. The control system with single-rate sampling can also compensate the harmonics. However, distortions can be easily observed from the PCC voltage. The FFT analysis in Figure 2.21(e) and Figure 2.21 (f) reveals that the 13^{th} order harmonics are not compensated in both the PCC voltage and the grid-side current. The steady-state waveforms match the previous analysis that compared with multi-rate control.

The admittance cannot be adequately increased in single-rate control, particularly at higher orders.

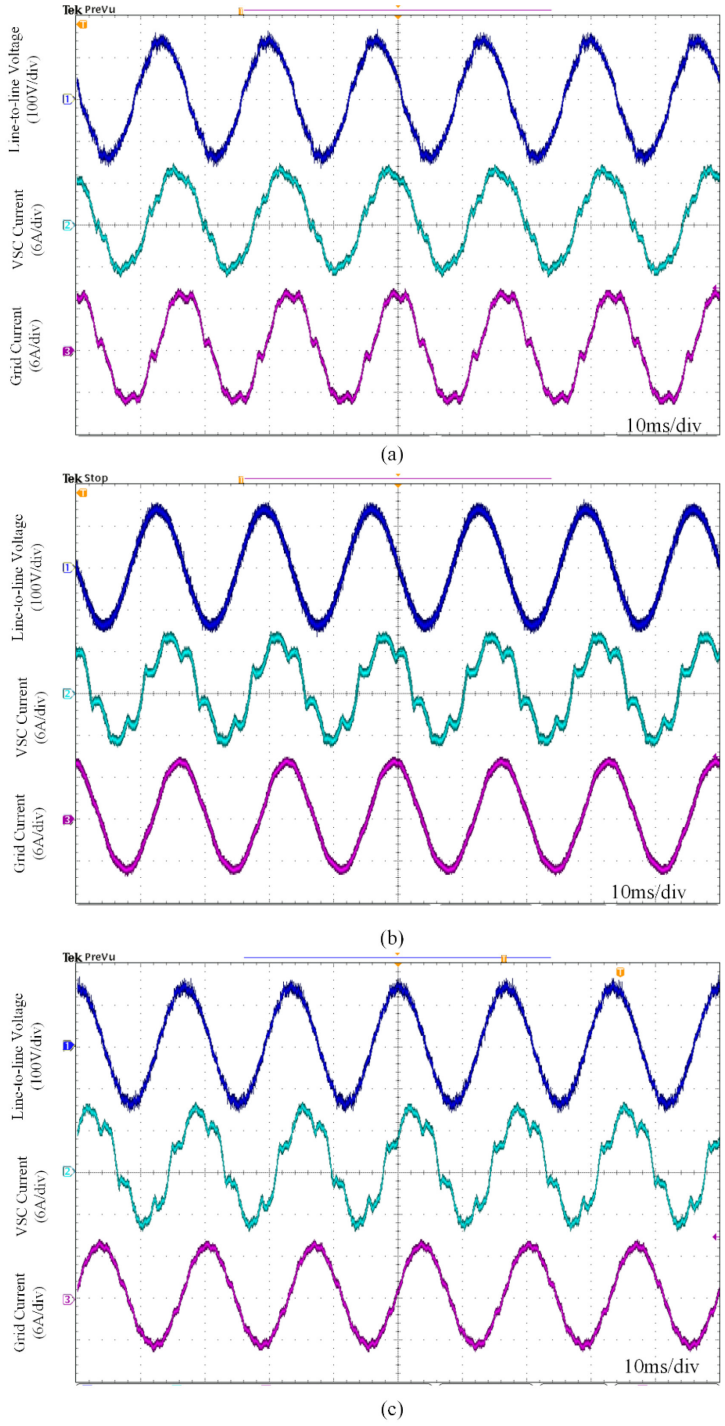

Figure 2.20 Steady-state waveforms (a) no compensation; (b) multi-rate compensation; (c) single-rate compensation

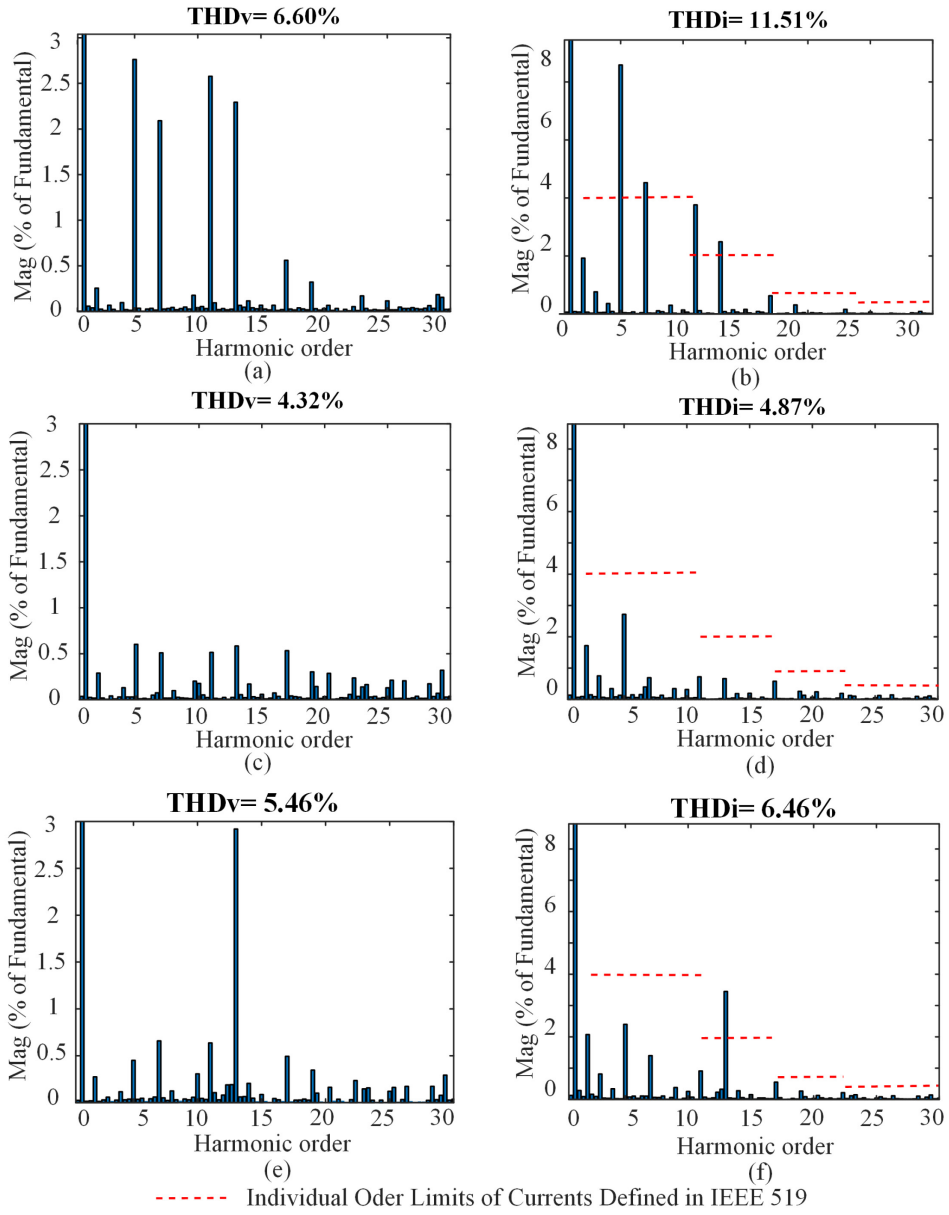

Figure 2.21 FFT analysis: (a) THDv when no compensation is conducted; (b) THDi when no compensation is conducted; (c) THDv under multi-rate compensation; (d) THDi under multi-rate compensation; (e) THDv under single-rate compensation; (f) THDi under single-rate compensation

The oversampling method is also applied to the experimental set for comparison, whose waveforms are shown in Figure 2.22 (a). As the inverter-side current contains large switching frequency ripple, the current I_2 is used in the

fundamental-frequency feedback loop. Hence the compensation performance shows some differences. It can be seen from the FFT results in Figure 2.22(b) and (c) that the harmonics are effectively compensated. Due to the different feedback current for fundamental-frequency control, the steady-state current waveforms have some differences from currents of multi-rate control. The compensation performance is similar to multi-rate control.

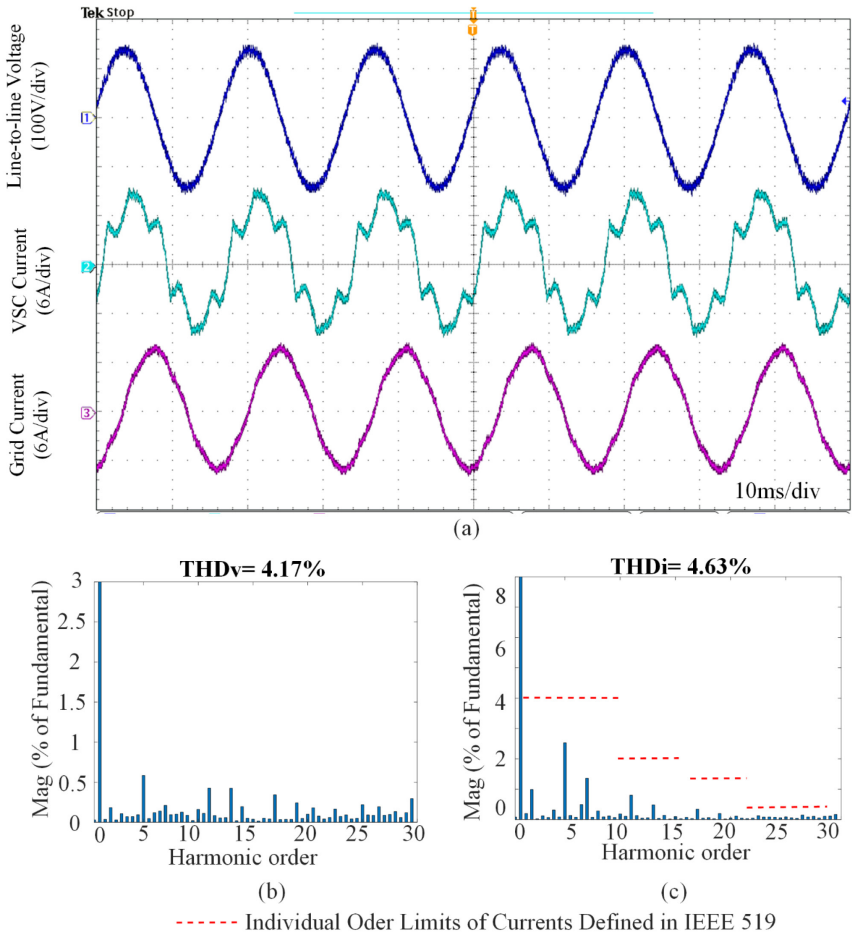

Figure 2.22 Experimental results of oversampling control with I_2 Feedback: (a) steady-state waveforms; (b) THDv under oversampling compensation; (c) THDi under oversampling compensation

To compare the computation burden, the complexity of the three different schemes are estimated and shown in TABLE 2.5. As can be seen, the computation burden of the proposed multi-rate scheme is lower than the oversampling method but higher than conventional single-rate control. It is worth to mention that only the

harmonic control paths and inner loops of the fundamental-frequency control are taken into consideration. If more functions, such as power management and other ancillary functions required in IEEE 1547 2018, are considered, the advantage of the proposed scheme can be more significant when compared with the oversampling scheme.

TABLE 2.5 Estimated Computation Burden of Different Schemes in One Switching Cycle

Scheme	Addition	Multiplication	Assignment	DSP Cycle
Single-rate Control	32	30	14	106
Proposed Multi-rate Control	112	110	44	376
Oversampling Control	152	150	60	512

Note: Only inner loops of the control schemes are considered

Hence it can be concluded that the proposed scheme can make a trade-off between high-performance harmonic control and computation burden.

Figure 2.23 shows the transient waveforms when the multi-rate (Figure 2.23(a)) and single-rate compensation control (Figure 2.23 (b)) are enabled. When the two methods are enabled, the PCC voltage quality is improved by the two methods. Also, the two methods show very similar overshoot, indicating that under the same control parameters, the system has similar damping ratios. However, the transient process lasts longer in single-rate control due to the lower sampling rate as the bandpass filter in low rate needs more time to extract the harmonics accurately.

Therefore, it can be concluded that the multi-rate control can have better steady-state and transient performance.

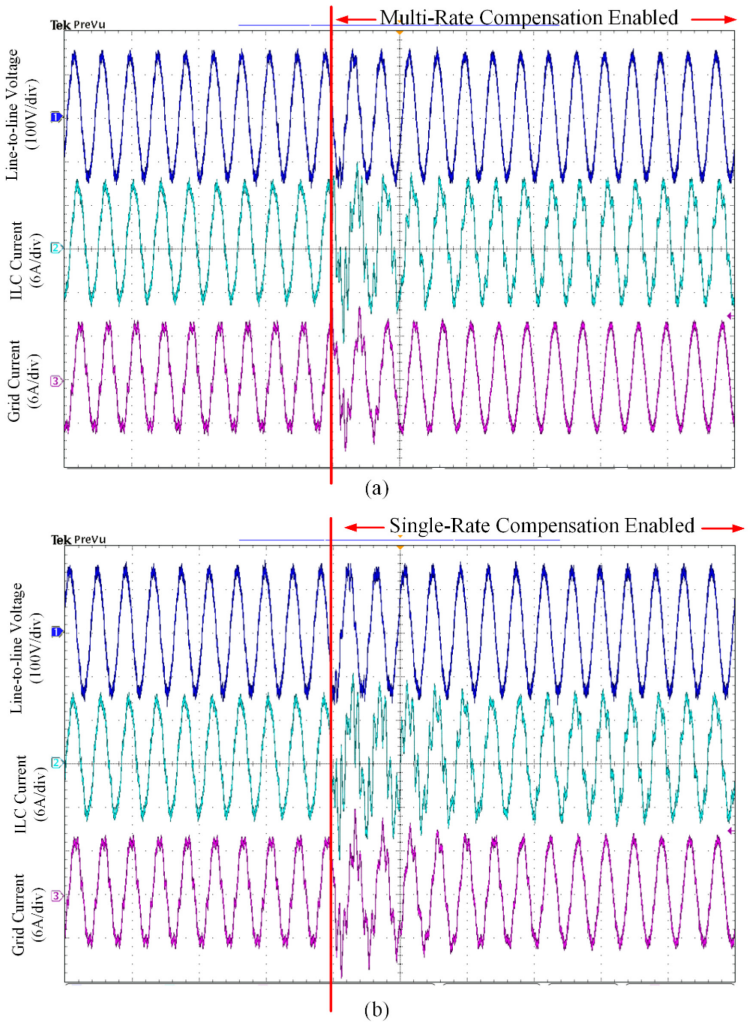

Figure 2.23 Transient waveforms: (a) multi-rate compensation; (b) single-rate compensation

To further verify the benefits of multi-rate sampling, the transient waveforms when the nonlinear load changes are shown in Figure 2.24. Thanks to the multi-rate sampling, when the nonlinear load is increased, the VSC responds to the increased load current and ensures no noticeable distortion to present at the PCC under steady-state. The load change test shows that the multi-rate control is robust enough to resist the disturbance from the nonlinear load.

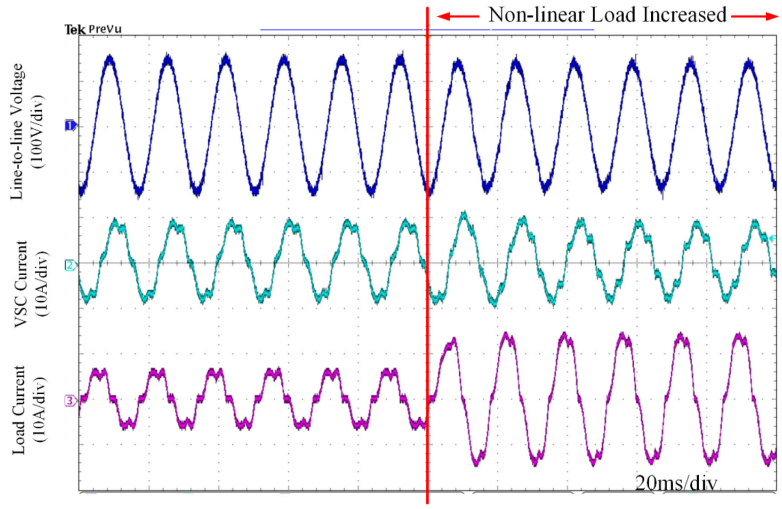

Figure 2.24 Transient waveforms when nonlinear loads are increased under multi-rate control

2.5 Conclusions

In this chapter, two virtual-impedance-based methods, the PCC voltage feed-forward method (VFF) and output current feed-forward method (CFF), are proposed to realize harmonic control through the AFE in VFD systems with low switching frequencies (e.g., 2 kHz). Harmonic rejection or compensation can be easily achieved under both two methods; thus, the control target can be flexibly set according to the grid requirements. Considering the low sampling rate and system delay brought by the low switching frequency, improved sampling schemes are proposed to increase the sampling rate of the harmonic control loop. The sampling rate of fundamental-frequency control can be selected flexibly. The effectiveness of these control methods and the benefits of the proposed sampling methods are verified by experiments.

Chapter 3

Improved Modeling Methods for Multi-Rate Virtual-Impedance-Based Harmonic Control Method[1]

In Chapter 2, two different feed-forward virtual impedance control schemes are proposed to improve the control performance of high-power AFEs. Meanwhile, the sampling scheme is also improved by applying the multi-rate control structure. The harmonic control will be performed under a high sampling rate, while the fundamental-frequency control will be performed at the switching frequency. The performance of the harmonic control and sampling scheme are verified by experimental results. However, due to the different sampling rate, a VFD will become an LPTV system. In conventional discrete-time modeling methods, such as Z-transform, only one sampling rate is allowed for the whole discrete-time system. For a system with multiple sampling rates, it is hard to design the virtual impedance accurately with the conventional methods.

Accurate virtual impedance is required in some applications. For example, when several four-quadrant VFD are paralleled, the harmonics need to be accurately shared by each AFE, requiring AFEs to have similar impedances at harmonic orders. Otherwise, more harmonics will flow to AFEs with lower impedances, which may trigger the overcurrent protection and cause higher thermal stress.

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[1] Publications out of this Chapter:

H. Tian, Y. Li and Q. Zhao, "Multi-Rate Harmonic Compensation Control for Low Switching Frequency Converters: Scheme, Modeling, and Analysis," in IEEE Transactions on Power Electronics.
doi: 10.1109/TPEL.2019.2933770.

To accurately control the virtual impedance, a multi-rate system modeling method and the corresponding analysis method are introduced for the multi-rate controlled high-power VSC in this chapter. In particular, the comparative studies between the conventional methods and the introduced methods include two aspects: 1) the modeling accuracy of impedance; 2) the stable boundary.

3.1 Model of the Multi-rate System

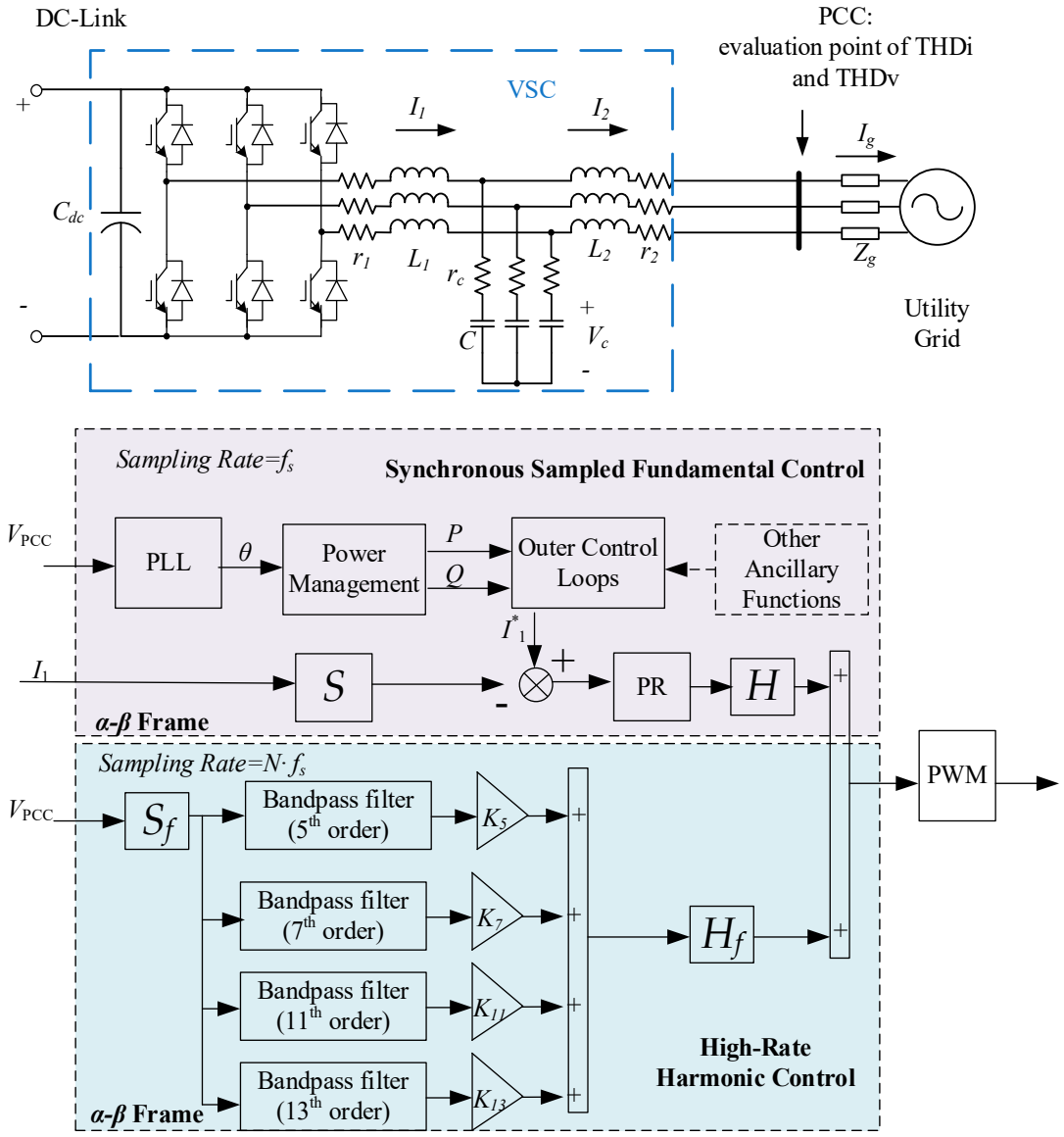


Figure 3.1 Detailed AFE circuit and multi-rate harmonic control scheme

Here, the VFF control with the improved sampling scheme in Figure 2.8 (b) is again studied as an example. The detailed scheme is redrawn here as Figure 3.1. As can be seen, the harmonic control scheme samples control variables N times the rate of the fundamental-frequency control. The generated control signals are fed to PWM as modulation references, which is sampled at the same rate of fundamental-frequency control. The different sampling rate makes the whole system an LPTV system.

To study an LPTV system, lifting technique is an effective tool to perform modeling. It transforms the LPTV system with the period of N to an N-input N-output LTI system. The dimension of the original system is thus "lifted" by N times. As the system is a periodic system with the frame frequency f_s, i.e., the switching frequency, it will be time-invariant at the frame frequency when considering all the input and output in one period. The time-invariant relationship can be established between the N input elements and N output elements in one period. In this section, the lifting technique is applied in the modeling of grid interfacing VSC. The detailed procedure will be shown in the following subsections.

3.1.1 State Space Model of the System

Firstly, the state-space models of AFEs should be obtained. A VSC is used to build AFE and connected to the grid through grid impedance and local loads. With controllers added, an AFE can be depicted as Figure 3.2(a). In Figure 3.2, S represents the sampler, while H represents a ZOH to convert the digital signal back to continuous-time. S_f is the fast rate sampler with sampling frequency $N{\cdot}f_s$. D↓ is a downsampler.

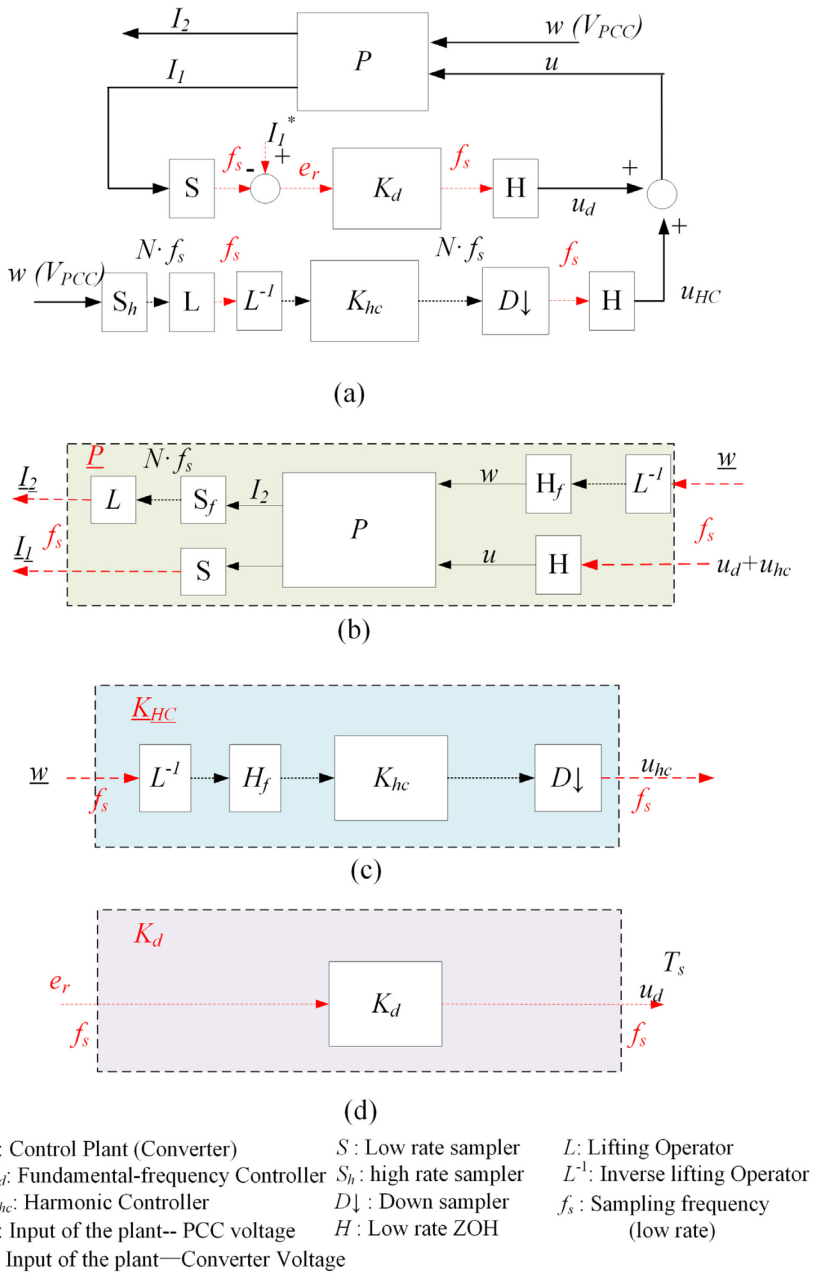


Figure 3.2 System block: (a) whole system with lifting operator applied; (b) control plant (VSC model) with lifting operators; (c) harmonic frequency control; (d) fundamental-frequency control

To model the plant part, I_1, I_2, and V_c are selected as state variables. The state-space equations can be built as:

$$\begin{pmatrix} \dot{I}_1 \\ \dot{I}_2 \\ \dot{V}_c \end{pmatrix} = \begin{pmatrix} -\frac{r_c + r_1}{L_1} & \frac{r_c}{L_1} & -\frac{1}{L_1} \\ \frac{r_c}{L_2} & -\frac{r_c + r_2}{L_2} & \frac{1}{L_2} \\ \frac{1}{C} & -\frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ V_c \end{pmatrix} + \begin{pmatrix} 0 \\ \frac{-1}{L_2} \\ 0 \end{pmatrix} V_{PCC} + \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \end{pmatrix} V_{inv} \tag{3.1}$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ V_c \end{pmatrix} \tag{3.2}$$

Define: $u=V_{inv}$, $w=V_{PCC}$, x= [I_1 I_2 V_c]', the state-space model can be expressed as:

$$\begin{aligned} \dot{x} &= Ax + B_w w + B_u u \\ \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} &= \begin{bmatrix} C_1 \\ C_2 \end{bmatrix} x \end{aligned} \tag{3.3}$$

The system defined in (1)-(2) can be simply expressed as (4):

$$P = \left[\begin{array}{c|cc} A & B_u & B_w \\ \hline C_1 & 0 & 0 \\ C_2 & 0 & 0 \end{array}\right] \tag{3.4}$$

One of the inputs for the plant is u, which is the output voltage of the three-phase VSC bridge V_{inv}. To apply an average model, V_{inv} is proportional to the control output, i.e., the modulation reference in PWM.

The fundamental-frequency controller K_d is a PR controller, whose input is the error between the output current and current reference e_r. The continuous-time state-space realization of the PR controller can be expressed as:

$$K_d^C = \left[\begin{array}{cc|c} 0 & 1 & 0 \\ -\omega^2 & 0 & 1 \\ \hline 0 & K_r & K_p \end{array}\right] \tag{3.5}$$

The discretized controller can be obtained by applying the Tustin method with pre-warping to obtain accurate gain and phase responses at the fundamental frequency ω. Then the discretized model can be defined as (3.6):

$$K_d = \left[\begin{array}{c|c} A_k & B_k \\ \hline C_k & D_k \end{array}\right] \tag{3.6}$$

which has a low sampling frequency f_s.

The feed-forward path is added to the controller to realize harmonic control, which is constructed by the harmonic extraction module and a control gain. The realization of the feed-forward controller K_{HC} in the continuous-time domain can be defined as:

$$K_{HC}^{C} = \left[\begin{array}{cc|c} 0 & 1 & 0 \\ -\omega_h^{\,2} & -\omega_h / Q & 1 \\ \hline 0 & K_h \omega_h / Q & 0 \end{array}\right] \tag{3.7}$$

The discrete-time model K_{HC} can then be obtained by discretizing (3.7), for which the sampling period is also set to be $N{\cdot}f_s$. To simplify the expression, the 5th, 7th, 11th, and 13th order harmonic controllers can be paralleled and defined as K_{HC} in (3.8):

$$K_{HC} = \left[\begin{array}{c|c} A_h & B_h \\ \hline C_h & D_h \end{array}\right] \tag{3.8}$$

Even each discretized model can be obtained with the traditional Z-transform method, the whole system model cannot be built due to the different sampling rates. The conventional approach is using the low rate to discretize the high rate models. Then the conventional discrete-time model can be obtained. This way simplifies the multi-rate control system as a single-rate control system with a low sampling rate, which obviously mismatches the real system and causes modeling errors. Hence, in this chapter, the lifting method is introduced to deal with the multi-rate LPTV system.

3.1.2 System Modeling by Lifting Method

The lifting operator is defined as follows: assume the signal is:

$$v = \{v(0) \quad v(1) \quad v(2) \quad ....\} \tag{3.9}$$

then the lifted signal will be [94]:

$$\underline{v} = \left\{ \begin{bmatrix} v(0) \\ v(1) \\ \vdots \\ v(\mathrm{n}-1) \end{bmatrix} \quad \begin{bmatrix} v(\mathrm{n}) \\ v(\mathrm{n}+1) \\ \vdots \\ v(2\,\mathrm{n}-1) \end{bmatrix} \quad \cdots \right\} \tag{3.10}$$

Define L as lifting operator, then

$$\underline{v} = Lv \tag{3.11}$$

In Figure 3.2, after applying the lifting operator L and the inverse lifting operator L^{-1}, the system is still equivalent to the original one. Then it can be split into two parts: the plant model in Figure 3.2 (b) and controller models in Figure 3.2 (c) and Figure 3.2 (d). The fast rate sampled signals are stacked to form a low rate vector.

The plant P should be discretized by the ZOH method, using the sampling period $N{\cdot}fs$. Then it can be represented as:

$$P_d = \left[\begin{array}{c|cc} A_d & B_{wd} & B_{ud} \\ \hline C_1 & D_{1w} & D_{1u} \\ C_2 & D_{2w} & D_{2u} \end{array}\right] \tag{3.12}$$

The plant model can be split into two parts as it has two independent inputs. The lifted plant model $\underline{P}$ can be obtained as:

$$\underline{P} = \begin{bmatrix} I & 0 \\ 0 & L \end{bmatrix} P \begin{bmatrix} I & 0 \\ 0 & L^{-1} \end{bmatrix} = \begin{bmatrix} SP_{I_1-u}H & SP_{I_1-u}H_f L^{-1} \\ LS_f P_{I_2-u}H & LS_f P_{I_2-w}H_f L^{-1} \end{bmatrix} \tag{3.13}$$

where the subscriptions of P are used to indicate the input port and output port. For example, $P_{I2\text{-}w}$ is the transfer function between output I_2 and input w. Then the lifted plant system in Figure 3.2(b) can be obtained as (3.14).

$$\underline{P}=\left[\begin{array}{c|cc} A_d^n & \underline{B_w} & \underline{B_u} \\ \hline C_1 & D_{1w} & D_{1u} \\ \underline{C_2} & \underline{D_{2w}} & \underline{D_{2u}} \end{array}\right]$$

$$=\left[\begin{array}{c|ccccc} A_d^n & A_d^{n-1}B_{wd} & A_d^{n-2}B_{wd} & & B_{wd} & \left(A_d^{n-1}+A_d^{n-2}+\ldots+I\right)B_{ud} \\ \hline C_1 & 0 & 0 & \ldots & 0 & 0 \\ C_2 & 0 & 0 & \cdots & 0 & 0 \\ C_2A_d & C_2B_{wd} & 0 & \cdots & 0 & C_2B_{ud} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ C_2A_d^{n-1} & C_2A_d^{n-2}B_{wd} & C_2A_d^{n-3}B_{wd} & \cdots & 0 & C_2A_d^{n-2}B_{ud}+C_2A_d^{n-3}B_{ud}+\ldots+C_2B_{ud} \end{array}\right] \tag{3.14}$$

As illustrated earlier, the control system samples the plant output at high-frequency $N*f_s$, while the harmonic control output must be downsampled with the PWM frequency f_s. Then the control system should be modeled as Figure 3.2(c). The controllers are fed with fast sampled signals while their outputs are sampled by a downsampler D↓, with slow sampling rate f_s. It is easy to prove the fact that:

$$D_{\downarrow}=SH_fS_f \tag{3.15}$$

Thus, the following equation can be obtained according to Figure 3.2(c):

$$\underline{K_{HC}}=D_{\downarrow}K_{HC}H_fL^{-1}=SH_f(S_fK_{HC}H_f)L^{-1} \tag{3.16}$$

where,

$$SH_f=\begin{bmatrix}I & 0 & \ldots & 0\end{bmatrix}L \tag{3.17}$$

Then the lifted controller can be expressed as:

$$\begin{aligned}\underline{K_{HC}}&=[\overbrace{I \quad 0 \quad \ldots \quad 0}^{N}]L(S_fK_{HC}H_f)L^{-1}\\&=[\overbrace{I \quad 0 \quad \ldots \quad 0}^{N}]LK_{HC}L^{-1}\end{aligned} \tag{3.18}$$

To sum up, the feed-forward controller K_{HC} can be lifted as:

$$\underline{K_{HC}}=\left[\begin{array}{c|c} \underline{A_h} & \underline{B_h} \\ \hline \underline{C_h} & \underline{D_h} \end{array}\right]=\left[\begin{array}{c|ccc} A_h^n & A_h^{n-1}B_h & A_h^{n-2}B_h & \cdots \quad B_h \\ \hline C_h & D_h & 0 & \cdots \quad 0 \end{array}\right] \tag{3.19}$$

For the fundamental-frequency controller, the discrete-time model K_d can be directly applied as its sampling frequency is f_s.

With the plant model and harmonic control model lifted, all the blocks are with the same sampling rate, which is f_s. The system becomes a single-rate high-dimensional LTI system from a dual-rate low-dimensional LPTV system. It is easy to construct a closed-loop state-space model for the system.

3.2 Frequency Response

In the previous section, the whole state-space model is derived. By lifting, the system becomes a Multi-Input Multi-Output (MIMO) LTI system. It is easy to derive the transfer function between each input to each output. However, the transfer function is obtained for one element of the input vector and one element of the output vector. As a result, although the lifted system becomes an LTI system, the transfer function derived directly cannot be used to obtain the actual frequency response of the original system. It is necessary to reconstruct the input and output signal to obtain the actual frequency response. For this purpose, the following procedure is performed.

The output of the system is a discrete-time sequence. Hence the Z-transform of the whole output vector *Y(z)* is:

$$Y(z)=\left[Y(z^N,0),\quad Y(z^N,1),\quad \cdots,\quad Y(z^N,N-1)\right]^T \tag{3.20}$$

where the sampling rate for z is $N{\cdot}f_{\mathrm{s}}$.

While the input can be expressed as a series of the shifted spectrum:

$$U(z^N)=\left[U(z)\quad U(z\phi^1)\quad \cdots\quad U(z\phi^{N-1})\right] \tag{3.21}$$

where

$$\phi=e^{j\frac{2\pi}{N}} \tag{3.22}$$

With these z-domain results obtained, the following relationship can be expected:

$$Y(z)=H(z)U(z) \tag{3.23}$$

Wherein, *H(z)* can be obtained from the lifted closed-loop model by calculating:

$$H(z) = \underline{C}(zI - \underline{A})^{-1}\underline{B} + \underline{D} \tag{3.24}$$

Then $H(z)$ is an N by N matrix. Let $H_{i,j}(z)$ denotes the entry in row i and column j starting from 0. Then the frequency response can be calculated by (25).

$$Y(z) = \sum_{n=0}^{N-1} U(z\phi^n)\left[\frac{1}{N}\sum_{l=0}^{N-1}\sum_{i=0}^{N-1}\phi^{in} z^{i-l} H_{l,i}(z^N)\right] \tag{3.25}$$

Define:

$$G_n(z) = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}\phi^{in} z^{j-i} H_{i,j}(z^N) \tag{3.26}$$

Rewrite (25) with the definition in (26), and (27) can be obtained:

$$Y(z) = \frac{1}{N}G_0(z)U(z) + \frac{1}{N}\sum_{n=1}^{N-1} G_n(z)U(z\phi^n) \tag{3.27}$$

The output spectrum is the sum of shifted and shaped versions of the input spectrum. This may be compared to a time-invariant system in which the output spectrum is simply a shaped version of the input spectrum, and the shaping function is called the frequency response. With the above-derived equations, one can achieve the exact frequency response of the multi-rate system.

TABLE 3.1 VSC Parameters Used in Analysis and Experiment

Parameters	Values
L_1	1.6 mH
L_2	1 mH
C	40 uF
Z_g	1.6mH, 0.2Ω
Switching Frequency fs	2 kHz
Sampling Frequency N·fs	10 kHz (N=5)

To compare the frequency responses of the multi-rate control system and single-rate control system, the system parameters in TABLE 3.1 are used in the calculation. The results are shown in Figure 3.3, which are the frequency response of the PCC voltage V_{PCC} to output current I_2 of both the proposed multi-rate control and single-rate control. The gain of the frequency response can also be seen as the

norm of VSC output admittance. As the output admittance is defined as $-I_2/V_{PCC}$, while the frequency response is I_2/V_{PCC}, the angle has a 180° difference.

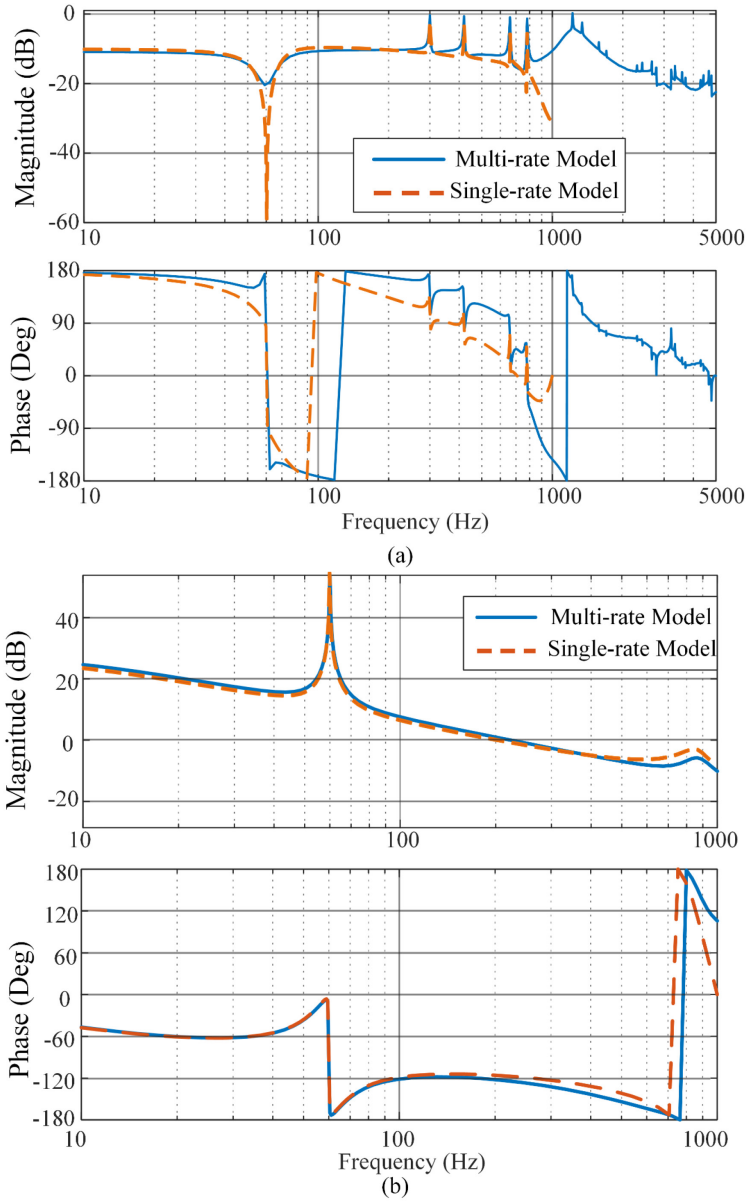


Figure 3.3 Frequency response: (a) from V_{PCC} to I_2 under different models; (b) from current reference to I_2 under different models

Firstly, the admittance can be increased at 5^{th}, 7^{th}, 11^{th}, 13^{th} order. A higher admittance (lower impedance) will ensure the VSC to absorb the harmonics and therefore improve the PCC voltage quality. A closer observation reveals that with the same control gains, the multi-rate control can obtain higher admittance than the

single-rate control, particularly at higher harmonic orders, such as 11^{th} and 13^{th} order. Also, the phase angles are different in the two models.

On the other hand, in Figure 3.3 (a), the admittance is not as low as single-rate control at the fundamental frequency when the same control parameters are used. The changes in the PCC voltages can potentially cause higher disturbances in multi-rate control. One can optimize the control parameters or add outer loops to help improve the performance. However, the effectiveness of fundamental frequency current control is similar between single-rate and multi-rate control. As can be seen from Figure 3.3 (b), which is the frequency response from the current reference to I_2, the open-loop gains at the fundamental frequency are similar. Hence for the fundamental-frequency control, the performance is very similar in the two control schemes, indicating that even the sampling scheme is different, the conventional single-rate model is good enough for analysis at the fundamental frequency.

To further investigate the differences between the multi-rate model and the single-rate model at harmonic frequencies, the frequency responses at harmonic orders with different feed-forward gains are obtained, and the differences between the two models are shown in Figure 3.4. Define S_v as the admittance of the multi-rate model and S_{sv} as the admittance of the single-rate model. The differences in admittance norms ($|S_v|$-$|S_{sv}|$) and angles ($\angle S_v$-$\angle S_{sv}$) can be easily observed. The compensation performance can be impacted by both the norm and angle. The admittance norm of multi-rate control is higher than the single-rate control under the same control gains. The differences in phase angles are also evident. The lagging angles of the output admittance can become leading under some control parameters.

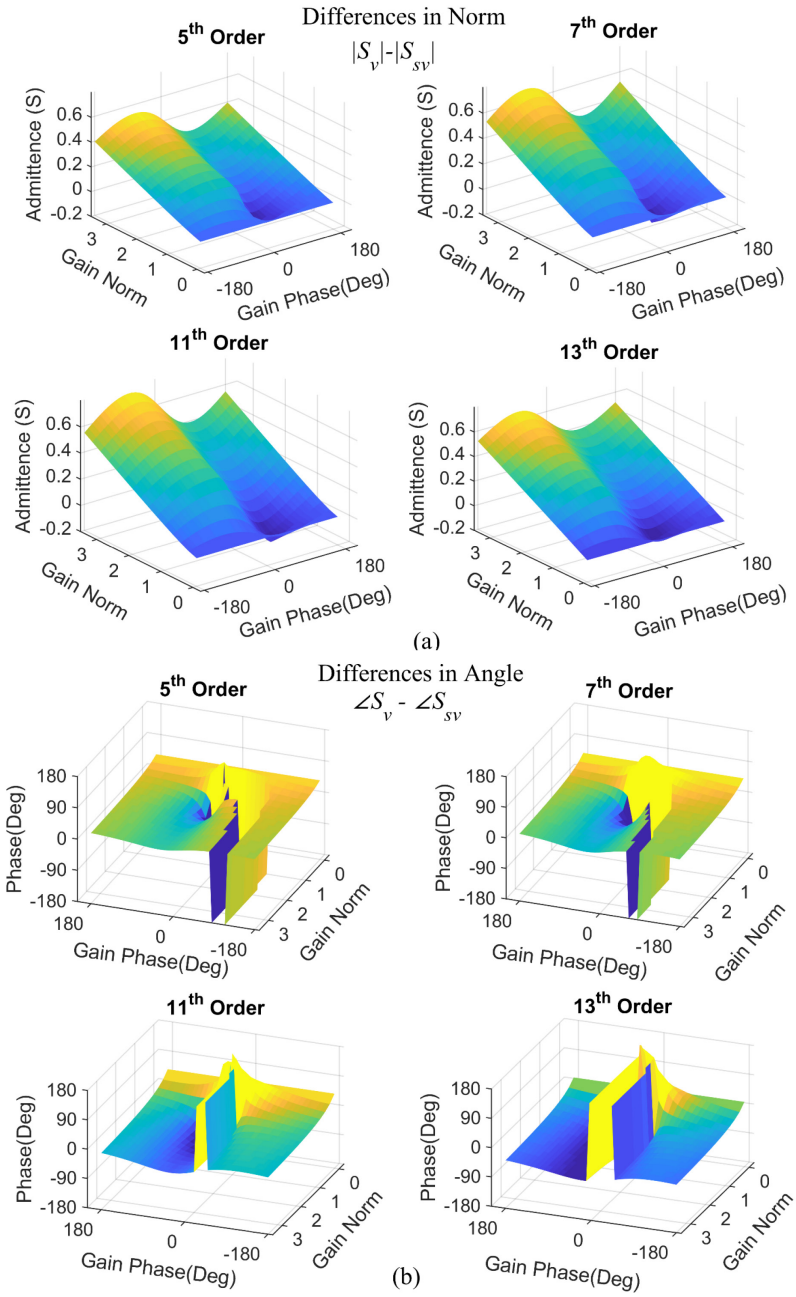


Figure 3.4 Comparison of frequency response at harmonic orders: (a) Differences in Norms of output admittance with respect to different control gains and (b) Differences in the angle of output impedance with respect to different control gains. (S_v-- Admittance obtain by lifted model; S_{sv}-- Admittance obtained by single-rate model)

The differences suggest that the lifted model and conventional discrete-time model have different accuracy. The lifted model should be more accurate as no simplification is made, and it matches the actual multi-rate control system. Therefore, in the applications requiring some specific output impedance

characteristics to do harmonic sharing or stability enhancement [95], the lifted model should be employed for the multi-rate system. This will be validated with the experimental results.

3.3 Stability Analysis

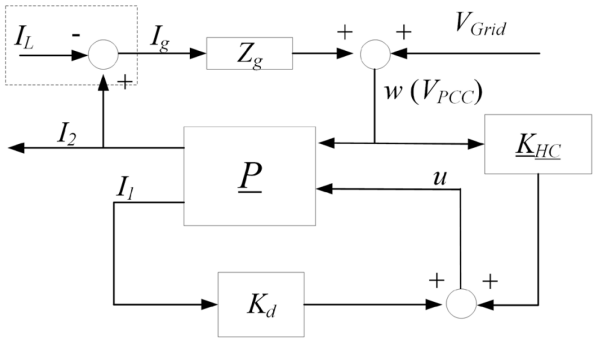


Figure 3.5 Complete closed-loop model for stability analysis

For the stability analysis, it is necessary to consider the whole system, including the grid impedance. The system model is thus modified to build a closed-loop system which includes all the factors that impact the stability, which is shown in Figure 3.5. By applying the lifting technique, the system is transformed into an LTI system without losing any information comparing to the actual LPTV system. Therefore, the stability analysis methods for linear systems (e.g., Lyapunov's first method for stability) are all applicable for the lifted model. By finding the eigenvalues of the matrix A in the closed-loop model, the stability can be investigated, which is equivalent to locate closed-loop poles. The characteristic polynomial in the discrete-time domain can be easily obtained with the closed-loop system model by (3.28):

$$\Delta(z) = \det(zI - \underline{A}) \tag{3.28}$$

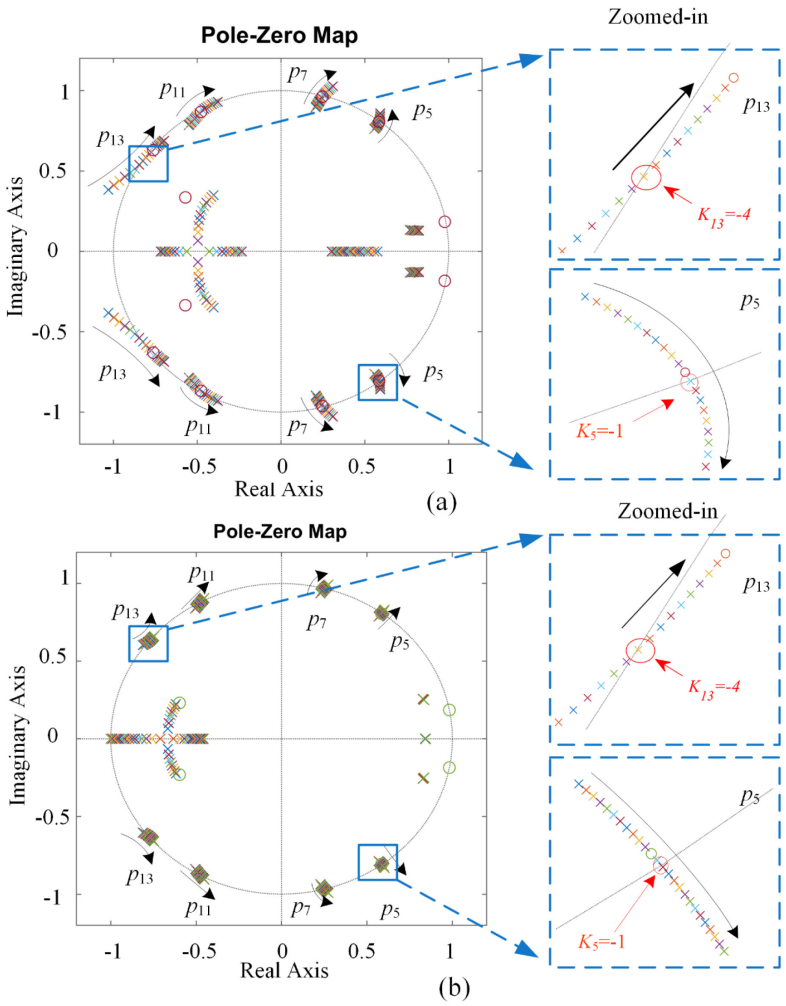


Figure 3.6 The pole-zero map of the system when the control gains increase and the zoomed-in view of 13th order related poles: (a) multi-rate system; (b) single-rate system

With the control gains changing from -10 to 15, the eigenvalues or the closed-loop poles obtained from the lifted model are shown in Figure 3.6 (a). For comparison, the poles of the conventional single-rate model are shown in Figure 3.6(b). With the control gains changing in the same range, the poles of multi-rate system change in a broader range on the complex plane. However, as shown in the zoomed-in view, the stable boundary is almost the same for the two control models. For example, for the pole p_{13}, which related to the 13th order harmonic control, the control gain should be lower than -4 to keep the system stable in the lifted model. Similarly, in the conventional discrete-time model, p_{13} will also move out of the unit circle when the gain is smaller than -4. The closer observations of the other

poles related to 5th 7th and 11th order control also show similar stable boundaries. This result reveals that the conventional discrete-time model can be used to estimate the stable boundary of the multi-rate controller, whose worst-case scenario has similar characteristics with single-rate control. The stability analysis can thus be simplified.

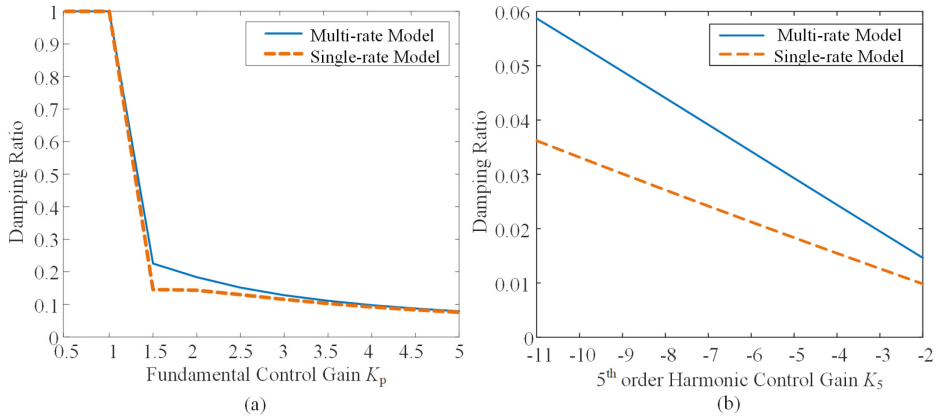


Figure 3.7 Comparisons on damping ratios under different models: (a) Fundamental-frequency control; (b) 5th order harmonic control

This conclusion can be further confirmed by the poles' damping ratio analysis. As can be seen from Figure 3.7 (a), at the fundamental frequency, the differences in damping ratios under the two different models are relatively negligible, meaning that single-rate model can be used for the fundamental-frequency controller design. However, at harmonic frequencies, the difference is significant, considering the small range of the available damping ratios, as shown in Figure 3.7 (b). Hence, it is recommended to use the multi-rate model (lifted model) to analysis the damping ratios of corresponding poles at harmonic frequencies. Besides, the same control parameter can lead to a higher damping ratio at harmonic frequencies in the multi-rate model, indicating the multi-rate control can have better transient performance at harmonic frequencies.

3.4 Recommendations on Modeling and Analysis.

The differences in the frequency response between the lifted model and conventional discrete-time model also indicate that the frequency response analysis

of a multi-rate control system cannot be estimated by conventional discrete-time models. The accurate frequency response can be used to design the output impedance/admittance, which is important for some applications requiring accurate harmonic sharing or specific impedance characteristics for better system performance.

On the other hand, the conventional discrete-time model can be applied to do the stability analysis simplifying the design procedure.

3.5 Experimental Verification.

To verify the modeling accuracy, the actual multi-rate harmonic control is applied to the experimental prototype shown in Chapter 2. The parameters are the same as the parameters shown in TABLE 3.1. Here, the 5th order harmonic voltage and 5th order harmonic current are measured under different harmonic control feed-forward gains as examples. The control parameters and the corresponding virtual impedance obtained from the experiment results and models are listed in TABLE 3.2. The control parameters are selected to maintain system stability and avoid minimal harmonic voltage or current, which may result in inaccurate measurements and calculations. To show the details of the results, the experiment results when K_5=0.25, K_5=-2, and K_5=-1j are shown as examples in Figure 3.8(a), (b) and (c) respectively.

TABLE 3.2 Comparisons of Admittance Values between Experiment Results and Numeric Models under Different Control Parameters

Control parameter	Experiment results	Lifted model	Convectional discrete-time model	The error of the lifted model	The error of the conventional discrete-time model
K_5=-0.25	0.36∠-32°	0.36∠-35°	0.32∠-76°	0∠3°	-0.04∠44°
K_5=-1	0.7∠-42°	0.62∠-45°	0.52∠-76°	0.08∠3°	0.18∠34°
K_5=-2	0.9∠-49°	0.97∠-50°	0.76∠-76°	-0.07∠1°	0.14∠27°
K_5=-j1	0.53∠-29°	0.56∠-19°	0.37∠-51°	-0.03∠-10°	0.16∠22°
K_5=-j2	0.83∠-20°	0.9∠-25°	0.58∠-13°	-0.07∠5°	0.25∠-7°
K_7=-1	0.5∠-82°	0.57∠-70°	0.41∠-100°	-0.07∠-12°	0.09∠18°
K_7=-2	0.95∠-86°	0.91∠-78°	0.62∠-100°	-0.04∠-8°	0.33∠14°

As shown in Figure 3.8(a), when the feed-forward gain K_5 is set to be a real number -0.25, the phase difference between 5th order voltage harmonic and 5th order current harmonic is about 1.37 ms, which is 148° and the amplitude of the current is 0.36 times of the voltage. Therefore, the frequency response from the PCC voltage to current (V_{PCC}/I_2) at 5th order can be seen as 0.36∠148°, which means the admittance ($-V_{PCC}/I_2$) at 5th order is 0.36∠-32°. Correspondingly, the admittance obtained by the lifted model is 0.36∠-35°, which is very close to the experimental results. The error is 0∠3°. However, the conventional discrete-time model shows 0.32∠-76°, which contains significant errors in both norm and phase. As shown in Figure 3.8 (b), when the K_5 is set to be -2, the frequency response is 0.9∠131°, then the admittance is 0.9∠-49°. The difference is -0.07∠-1° compared with the lifted model. On the other hand, the difference is 0.14∠27° for the conventional discrete-time model.

Besides the smaller errors, it is also worth noting that the lifted model matches the trends of experimental results-- the phase angle decreases as K_5 changes from -0.25 to -2. However, the conventional discrete-time model shows a constant phase angle under the same changes, indicating the single -rate cannot describe the system features accurately.

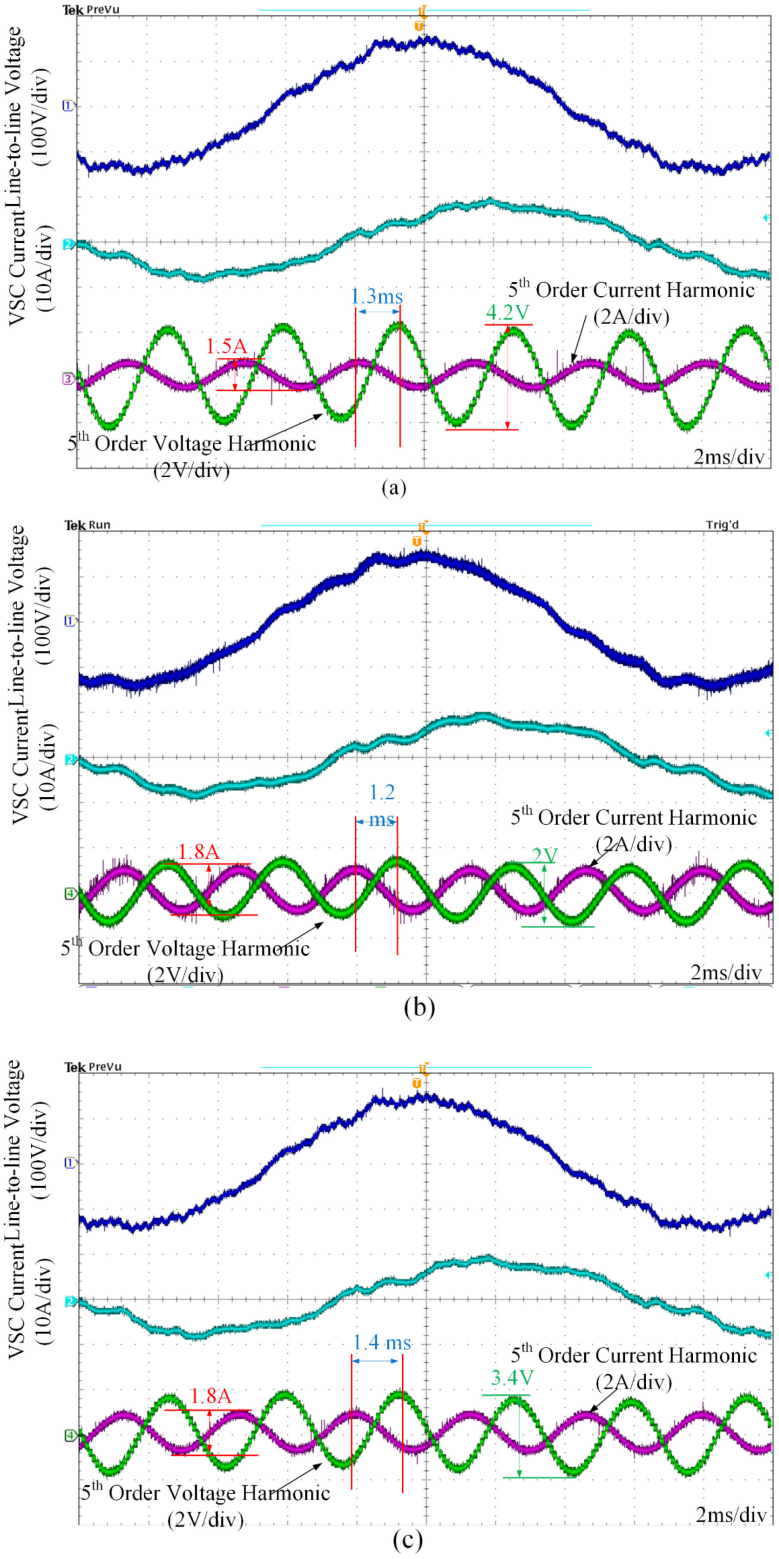


Figure 3.8 Harmonic current and voltage under different control parameters: (a) K5=-0.25; (b) K5=-2; (c) K5=-1j

Similarly, as shown in Figure 3.8(c), when K_5 is set to be a pure complex number $-j1$, the negative admittance is measured as $0.53\angle 151°$, meaning that the admittance is $0.53\angle -29°$. The lifted model shows the negative virtual admittance should be $0.56\angle -19°$, which is also very close to the experimental results with a small error of $0.03\angle -10°$. As a comparison, the conventional discrete-time model shows an error of $0.16\angle 22°$. The conventional discrete-time model also has a larger error.

The other results shown in TABLE 3.2 also verify that the lifted model is more accurate for analyzing virtual admittance values. With the precise model, it is possible to design output impedances at 5^{th} and 7^{th} orders, which is suitable for harmonic sharing or stability enhancement. However, as the 11^{th} and 13^{th} order are close to the resonant frequency of the LCL filter, the output admittance can be sensitive to the mismatch of parameters. Therefore, it is recommended to only design the 11^{th} and 13^{th} order control parameters to ensure harmonic compensation performance.

3.6 Conclusions

With the multi-rate harmonic control, an AFE is an LPTV system. To model such a system and achieve virtual impedance design accurately, the lifting technique is introduced in this work, which transforms the LPTV system to an LTI system with a higher dimension. Comparisons between the lifted model and the conventional discrete-time model reveal that the lifted model is more accurate than the conventional discrete-time model for harmonic control. While the stability ranges under both modeling methods are similar. It is therefore recommended to use lifted model to achieve the frequency response while stability analysis can be simplified by using a conventional discrete-time model. But the damping ratios can still be different in the two models. The accuracy of the lifted model is verified with experimental results.

Chapter 4

Carrier-Based Stair Edge PWM (SEPWM) for Capacitor Voltage Balancing in Multilevel Converters with Floating Capacitors1

In Chapter 2 and Chapter 3, the harmonic control schemes to help VFDs to resist the interferences from local loads or utility grid are proposed and analyzed. Besides the harmonics induced by the loads or utility grid, harmonic distortions can also be caused by the capacitor ripples of multilevel VFDs.

In high-power VFDs, if the capacitors can only be balanced at the fundamental frequency, large capacitor ripples will present at a low fundamental frequency as the ripple amplitudes will be proportional to the fundamental frequency in such kind of converters. The VFDs usually need to operate at a very low frequency (e.g., 1 Hz) to have low motor speed. If the capacitors cannot be well balanced, VFD will have to limit its operation range or have a high cost on capacitors.

In this chapter, the approaches to mitigate capacitor ripples of MLCs are reviewed. A general PWM method to help mitigate capacitor ripples is proposed. This method can ensure the MLCs to balance their capacitors at the switching frequency instead of the fundamental frequency. The design procedure and study case are given and verified by the experimental results.

[1] Publication out of this chapter:

H. Tian and Y. W. Li, "Carrier-Based Stair Edge PWM (SEPWM) for Capacitor Balancing in Multilevel Converters With Floating Capacitors," in IEEE Transactions on Industry Applications, vol. 54, no. 4, pp. 3440-3452, July-Aug. 2018..

4.1 Existing Control Approaches for Capacitor Balancing

In MLCs with unclamped DC-link capacitors or floating capacitors, the voltage balancing is mandatory to operate the converter properly and ensure the output quality. Due to the uniqueness of each topology, the measures are usually explicitly developed for one topology and hard to be generalized.

Generally, the control approaches are preferred in MLCs to achieve capacitor-balancing as no extra cost on circuitry is needed. Either extra controllers or extra procedure in PWM will be added. According to the different approaches to achieve capacitor-balancing, the approaches can be classified as: 1) feedback-control-based methods; 2) redundant-states-based methods; 3) extra-level-generation-based methods. The methods must be selected according to the natures of different topologies.

4.1.1 Feedback-Control-Based Balancing Methods

By injecting extra control signals to the modulation references, the output voltage level and the corresponding dwell time can be changed. In this case, the MLCs can obtain the chances to utilize more switching states to balance capacitors. The generated control signals to help improving the voltage balancing can be offset signals [96]-[99], zero sequence signals [100]-[102], subharmonics [103], etc.

In Figure 4.1, a widely applied zero-sequence voltage injection method to improve unclamped DC-link capacitor balancing (neutral point balancing) for 3L-NPC is shown. The voltage on the two DC-link capacitors-- V_1 and V_2, are measured, and their differences are used to do the balancing. The generated signals are added to the modulation index. As shown in Figure 4.2, thanks to the zero-sequence-signal injection, the two different DC-link capacitor voltages are changing towards each other, reducing the voltage errors. After 80 ms, the two DC-link voltages are almost the same. The steady-state voltage still contains 3rd order harmonics, but the average values are the same.

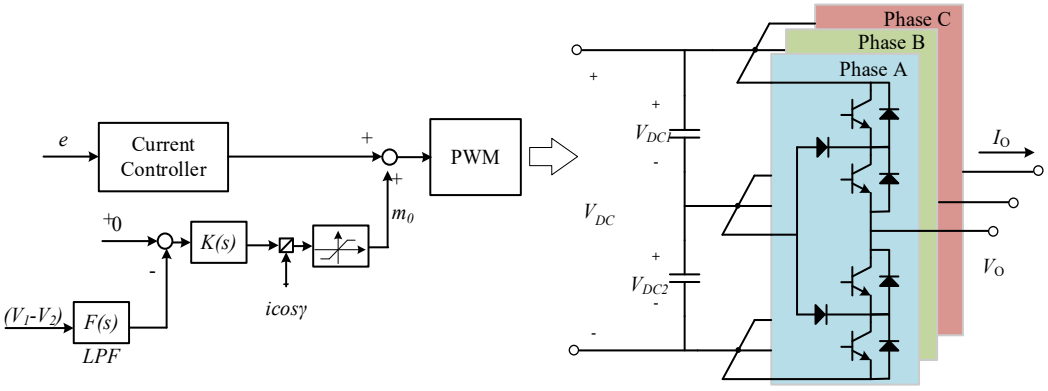


Figure 4.1 Zero sequence injection method to achieve DC-link capacitor-balancing

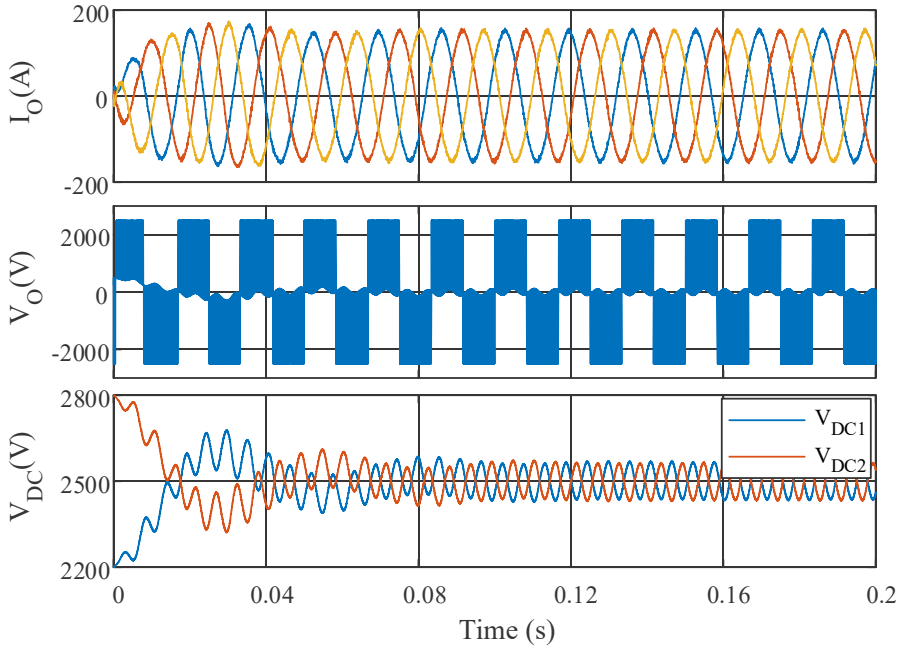


Figure 4.2 Simulation results of zero sequence injection method

4.1.2 Redundant-States-Based Balancing Methods

In some topologies, the capacitors, particularly the floating capacitors, can be balanced with the redundant states. In this case, the control and modulation can be independent of the actions for capacitor-balancing. Instead, only an extra step to select redundant switching states according to the requirements for capacitor-balancing is needed. With this approach, the balancing of capacitors can be achieved at the switching frequency [104]-[105], allowing smaller capacitance or lower ripples for this type of topologies. When multiple capacitors are required to

be balanced, cost functions which consider the voltage errors on all the capacitors [106]-[108], can be used.

An example of topology with the complete capacitor-voltage-balancing capability is 5L-ANPC, whose floating capacitor can be charge/discharge by using redundant switching states. The topology is shown in Figure 4.3, and the switching states are listed in TABLE 4.1. As can be seen, the switching state V2 can charge the floating capacitor C_f under positive current, and V3 can be used to discharge C_f. When the current is negative, the impacts of V2 and V3 are inverted. As a result, when the 5L-ANPC produces $V_{dc}/4$, C_f can be both charged and discharged under any current direction. This allows the 5L-ANPC to balance C_f at the switching frequency.

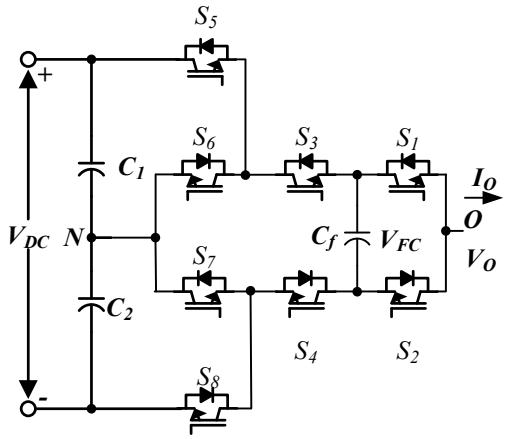


Figure 4.3 Topology of 5L-ANPC

TABLE 4.1 Switching States and the Impact to Floating Capacitor C_f

Switching States								Output	Effect on C_f		Switching
S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	Voltage	I>0	I<0	State No.
0	1	0	1	0	1	0	1	$V_{dc}/2$	n/a	n/a	V1
0	1	0	1	0	1	1	0	$V_{dc}/4$	+	-	V2
0	1	0	1	1	0	0	1	$V_{dc}/4$	-	+	V3
0	1	0	1	1	0	1	0	0	n/a	n/a	V4
1	0	1	0	0	1	0	1	0	n/a	n/a	V5
1	0	1	0	0	1	1	0	$-V_{dc}/4$	+	-	V6
1	0	1	0	1	0	0	1	$-V_{dc}/4$	-	+	V7
1	0	1	0	1	0	1	0	$-V_{dc}/2$	n/a	n/a	V8

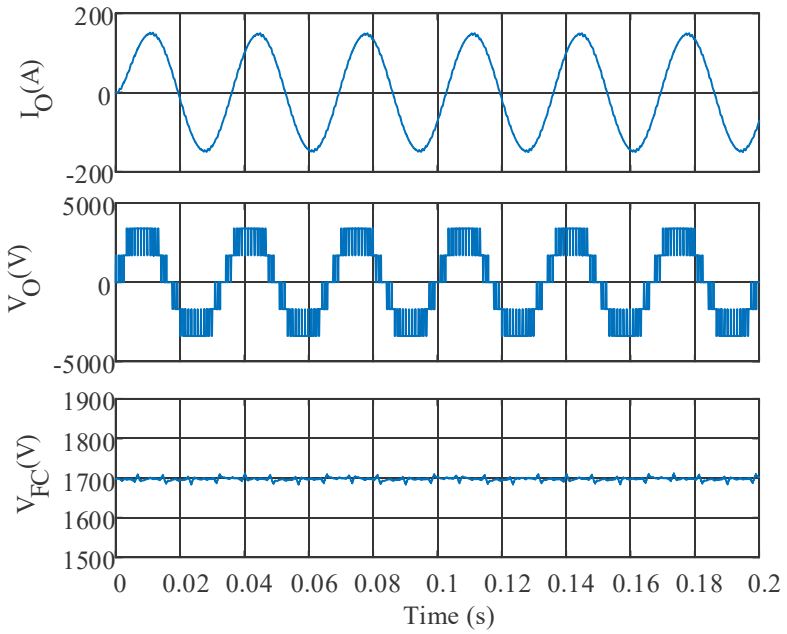


Figure 4.4 Simulation results of 5L-ANPC and its redundant-states-based capacitor-balancing

The performance of redundant-states-based capacitor-balancing is shown in Figure 4.4. The voltage on the floating capacitor, i.e., V_{FC}, is kept smooth and stable. As a result, both the output voltage V_O and output current I_O are of high quality.

The redundant-states-based methods are very effective and easy-to-implement. However, this method can only be applied to the topologies with enough switching states.

4.1.3 Extra-Level-Generation-Based Balancing Methods

When the feedback-control-based method is not applicable, and the redundant switching states are not sufficient to balance the floating capacitors, extra-level-generation-based methods can be applied. In this case, the operation of the MLCs will be redesigned to fulfill the capacitor-balancing requirements. For example, [109] designed the balancing oriented PWM for NPC converters, which generates more than two voltage levels in one switching period. The method is then developed as the quasi-2L/3L operation for converters like NPC converter [110]-[111]and MMC [112]. Moreover, the designed output voltage levels can be produced by

using virtual vectors [113] and designed carriers [114], ensuring that the switching states for capacitor-balancing can be used with desired dwell time.

As an example, the quasi-2L operation is applied to 4L-NNPC topology, shown in Figure 4.5 (a). The conventional 4L PWM, as shown in Figure 4.5 (b), only generates two output levels in each switching period. For converters lacking enough switching state to do balancing, the capacitor-balancing is hard to achieve. The quasi-2L operation, shown in Figure 4.5 (c), can generate all the output levels of the 4L-NNPC converter in one switching period. As a result, more switching states can be used to balance capacitors.

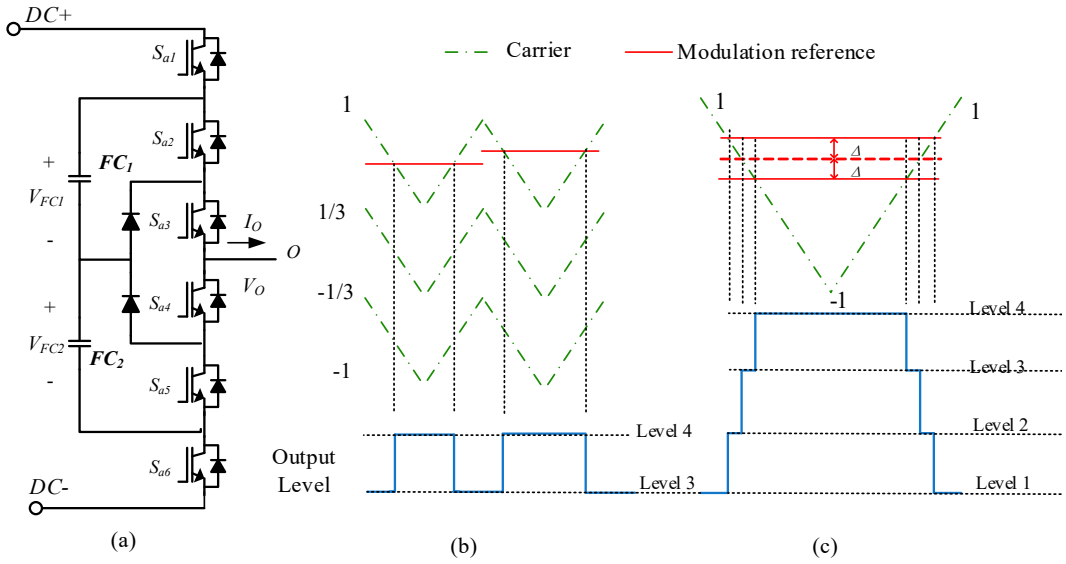


Figure 4.5 4L-NNPC topology and its PWM: (a) 4L-NNPC topology; (b) conventional 4L LSPWM; (c) quasi-2L PWM

The simulation results shown in Figure 4.6 reveals that the conventional PWM can lead to large voltage ripples on the two floating capacitors of the 4L-NNPC converter. On the other hand, when the quasi-2L operation is applied, the voltage ripples is significantly reduced. As a result, the output waveform is no longer a typical multilevel voltage.

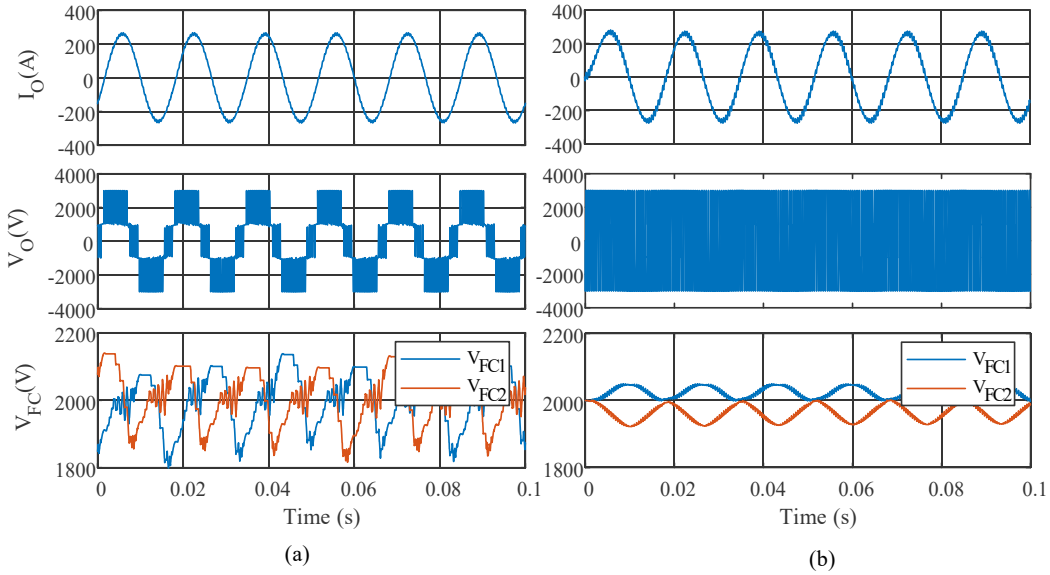


Figure 4.6 Simulation result of 4L-NNPC: (a) conventional 4L operation; (b) quasi- 2L operation

The extra level generation methods can improve the voltage balancing, but they can also lead to some side-effects, such as reduced equivalent switching frequency, larger switching loss, increased *dv/dt*, etc.

4.2 Principle of the Proposed Stair Edge PWM (SEPWM)

As discussed, the aforementioned methods are usually developed for specific topology. To obtain a general method to cope with the capacitor-ripple-induced harmonics, a new PWM approach, named stair-edge PWM (SEPWM), is proposed in this chapter. As a type of extra level generation method, the method can effectively improve capacitor-balancing for various topologies with floating capacitors or unclamped DC-link capacitors. Compared with the existing general quasi-2L method, the SEPWM allows the flexible design to improve performance based on analysis of the topology. Besides, the proposed method can ensure the equivalent output with conventional PWM methods, and low *dv/dt* of MLCs can still be achieved.

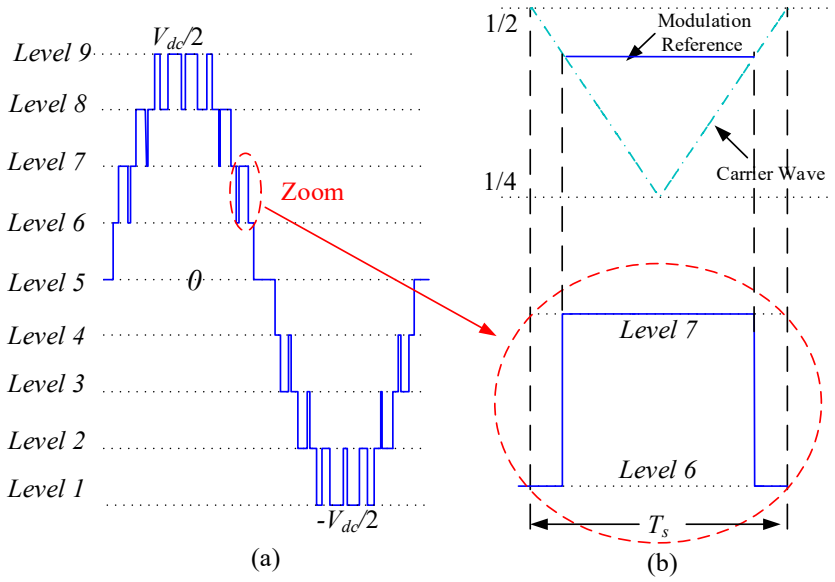


Figure 4.7 Output of normal multilevel PWM: (a) typical voltage; (b) modulation method

Figure 4.7(a) shows a typical output voltage waveform of the MLCs. In one switching period, two different voltage levels are produced, as shown in Figure 4.7(b). There may be several switching states to produce the same output level. For floating capacitors topologies, each switching state provides a different current flow path, resulting in different impacts (charge/discharge effect) on floating capacitors. Ideally, charging and discharging states are available for each PWM cycle so that the converter can operate within a wide output frequency range, e.g., 0-60Hz, without worrying about the voltage ripples on the capacitors. However, some of these floating capacitors topologies may lack enough switching states to balance the floating capacitors at switching frequency. For those MLCs with incomplete capacitor-voltage-balancing capability, the switching states with inverse impact on the capacitor are only available when the fundamental current direction changes, resulting in voltage ripples at the fundamental frequency. As a result, this kind of MLC requires larger capacitors and is not suitable for VFDs when the low-speed operation is needed.

To apply those converters with incomplete capacitor-voltage-balancing capability in VFD application, floating capacitor or unclamped DC-link capacitor voltage balancing at the switching frequency is essential. Producing the traditional multilevel output, e.g., nine-level (9L) voltage shown in Figure 4.7(a), the

balancing capability can only be enhanced by adding extra semiconductor switches to provide new current flow paths. This will cause extra system cost, lower power density, and lower reliability. To avoid adding extra switches, the MLC can generate more output levels to obtain more switching states within one switching period to do balancing, on condition that the same phase energy (voltage-second product) can be achieved.

To realize this objective, the SEPWM is proposed, whose output voltage waveform in one PWM period is shown in Figure 4.8(a). Different from the voltage waveform in conventional multilevel PWM shown in Figure 4.7(b), more than two levels are produced. The levels produced in one PWM period are classified as follows:

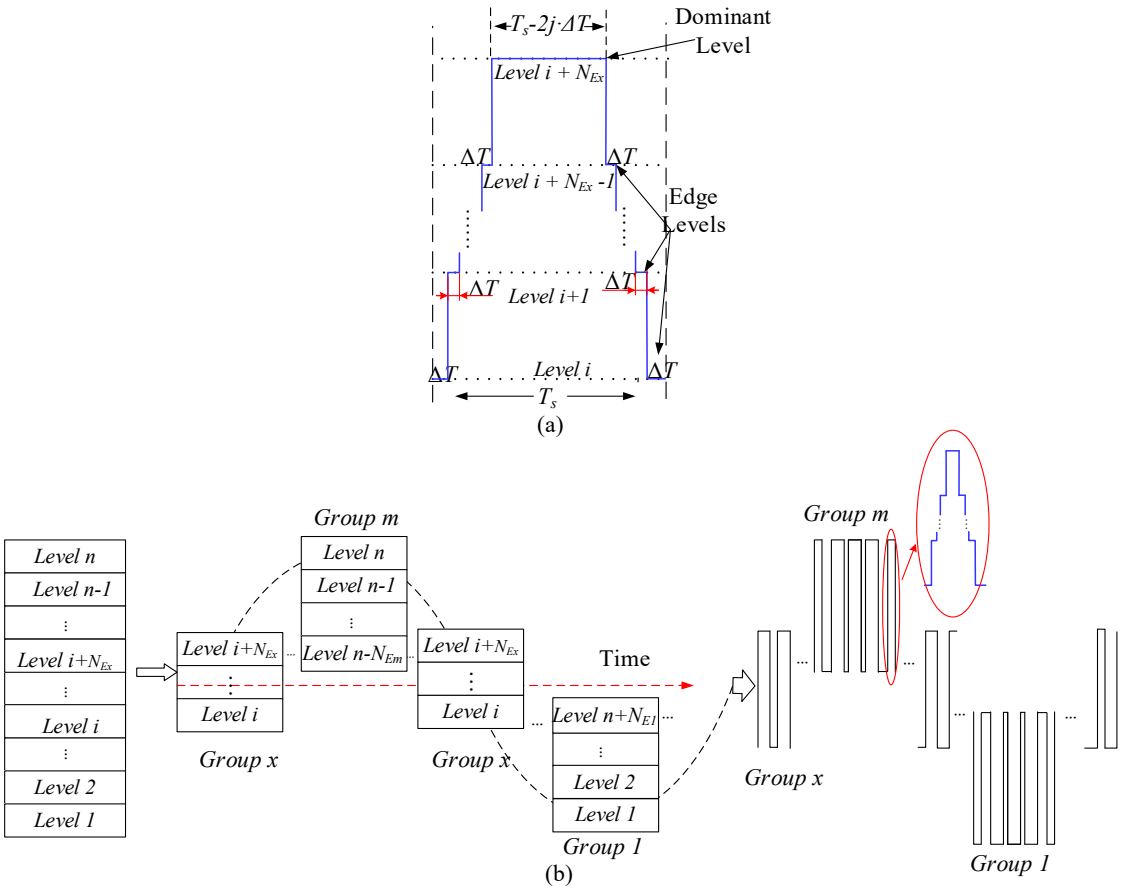


Figure 4.8 SEPWM and grouping of output levels: (a) typical output waveform of SEPWM in one PWM period; (b) level grouping and an example of the output waveform in one fundamental period

Dominant Level: Dominant levels are usually the highest or lowest levels produced in one PWM period, like Level $i+N_{Ex}$ in Figure 4.8(a). As their dwell time is not designed for balancing unclamped capacitor voltage, switching states of dominant level should either have no impact on unclamped capacitor voltage or have redundant states to balance the unclamped capacitor voltage in adjacent PWM periods. For converters with complete capacitor-voltage-balancing capability, the dominant levels are enough. The two levels produced in one PWM period in normal multilevel PWM can both be seen as dominant levels.

Edge Level: the output levels to produce the stairs in the rising and falling edge, such as *Level i* to *Level* $i+N_{Ex}$*-1* shown in Figure 4.8(a). Their dwell time is designed to achieve unclamped capacitor voltage balancing. Edge levels are not needed if a converter has the complete capacitor-voltage-balancing capacity. However, if the topology has the incomplete capacitor-voltage-balancing capability, the corresponding switching states may only be able to charge (or discharge) the unclamped capacitors while the states with the opposite impact are unavailable until the current direction changes. In this case, edge levels will be required to include enough balancing states to balance the unclamped capacitor voltage within a PWM period. When the edge levels with balancing states are not consecutive (there is more than one level step between them), some other edge levels will be inserted to ensure the output voltage to change one level voltage at one time. This is important to maintain the same *dv/dt* with normal multilevel PWM methods.

With dominant levels, edge levels, and their dwell time properly designed, SEPWM can improve the unclamped capacitor voltage balancing while producing the same voltage second product and *dv/dt* with the normal multilevel PWM. The design steps of SEPWM are as follows:

Step 1: Grouping of output Levels

In the SEPWM method, all the output levels can be assigned to several level groups. Both the number of levels in one group and the number of groups can be designed flexibly according to the unclamped capacitor voltage balancing requirements and operating conditions. E.g., in Figure 4.8(b), the output levels of an *n*-level converter are divided into *m* groups. All the levels used in one PWM

period are seen as one level group. Also, the levels in one group should be consecutive (only one level voltage difference between two adjacent states). E.g., in Figure 4.8 (a), the group contains N_{Ex}+1 levels. Hence the number of levels used in one PWM period is $N_{Ex}+1$. All the edge levels, from *Level i* to *Level* $i+N_{Ex}-1$, are produced (with dwell time ΔT) consecutively in the rising/falling edge. As a result, the output voltage only changes one level step ($V_{dc}/(n-1)$ for an *n*-level converter) at one time. The load thus sees voltage with the same *dv/dt* with the normal multilevel PWM.

To include the minimum number of levels in the group while obtaining good balancing capability, the following rules are considered for the level grouping:

1) Balancing State Rule: the group must contain the states to charge and discharge the unclamped capacitor under any current direction.

2) Dominant Level Rule: at least one and at most two dominant levels should be included in the group. The dominant level should be the highest or the lowest level in one group.

3) Consecutive Level Rule: the levels in one level group should be consecutive to avoid increasing *dv/dt*.

Following the design rules, the grouping of output levels can be done based on the analysis of switching states for different types of converters. A flexible number of groups, as well as a flexible number of levels in one group, can thus be used in different topologies. Also, it is allowed to assign levels into different groups to fulfill the group design rules. Due to the consecutive level rule, one level can only be assigned to at most two consecutive groups.

With group assigned, each group will be used in a specific modulation reference range. When the modulation reference moves to the range of a level group, all the levels in the group will be produced consecutively in the rising/falling edge. E.g., in Figure 4.8(b), when the modulation index is close to 1, group *m* is used.

Increasing the number of output levels produced in one PWM cycle can result in a higher number of switching actions. Considering the drawback, the SEPWM can be applied for the low-speed (low fundamental frequency) operation. In some drive applications, such as fan-type loads, the low-speed operation only requires

low torque and low current. In this case, the switching loss will not be significantly increased.

Step 2: Dwell Time Determination

With the output level grouped, the dwell time of each level, and the corresponding voltage can be used to calculate the voltage second product. To simplify the design, the dwell time of all the edge levels is designed to be the same within one switching period. The dominant levels will be used in the rest of the PWM period. The voltage second product in one PWM period is thus a function with respect to ΔT, as switching frequency and the level voltage are known for the given MLC. By adjusting ΔT, the voltage second product can be the same as the 2L-PWM. Using the voltage second product of 2L-PWM as the control target is more straightforward because the conventional multilevel PWM methods also produce the same voltage second product with 2L-PWM. The particular design method will be illustrated in the design example.

Step 3: Constraints of the Modulation Index

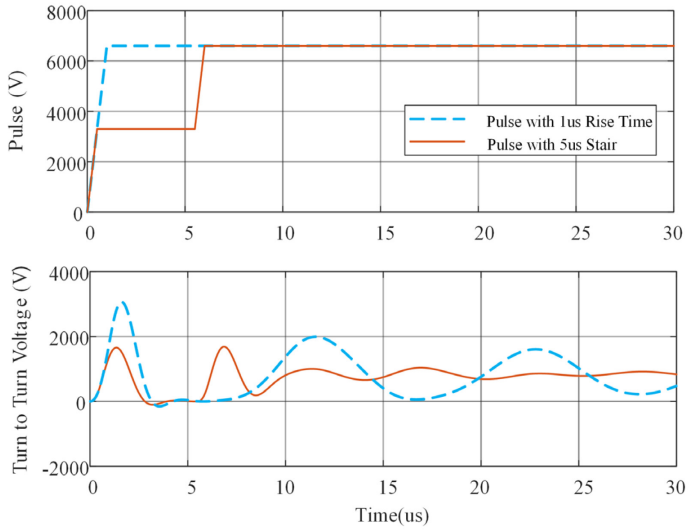


Figure 4.9 Comparison of turn-to-turn voltage of the motor winding under 1 μs rise time pulse and pulse with 5 μs stairs

For VFDs, when the converter output voltage is applied to the stator winding of the motors, the electromagnetic force will be generated by the stator winding and oscillate due to the LC circuit constructed by the parasitic capacitor and stator

inductor. The oscillate peak will add up to the voltage applied by VFD, increasing the possibility of partial discharge and leading to earlier insulation failure as a long-term consequence. Therefore, reduced *dv/dt* is a salient advantage of the MLCs comparing to the 2-L converters rated the same voltage. The dwell time of edge levels must be long enough to avoid superposing VFD output voltage over the oscillation peak on the motor winding. According to IEEE 522:2004 [119], impulses with the rising time of 1.2 μs or longer do not generally stress the turn insulation. Thμs the edge in SEPWM can be set with several microseconds dwell time for edge levels, obtaining the large safety margin for motor insulation. Considering this, the minimum ΔT can be set to be 5 μs. As can be seen from the simulation results in Figure 4.9, when a pulse with 1 μs rise time is applied to the motor winding model [120]-[121], the resonant peak of the turn-to-turn voltage can be as high as 3kV. However, when 5 μs step is added to the rising edge, the peak value of the turn-to-turn voltage is reduced by about 50%. It can also be concluded that even the minimum edge level dwell time(5 μs) can effectively avoid the superposition of the oscillation peaks for a VFD-fed medium voltage motor when SEPWM is applied.

As the ΔT is a function of modulation index and switching period, the constraints of modulation index under different switching frequency can be obtained, which will be illustrated in detail in the design example.

Step 4: PWM realization

The PWM can be realized based on the results obtained from the previous steps. It is convenient to generate edge levels by using multiple modulation references in Sinusoidal PWM (SPWM) approach. Positive/negative offsets can be added to the original modulation reference to generate levels in the level group. It is worth to note that the dwell time can be a constant or a variable with respect to the duty cycle as long as the voltage-second equivalence is maintained.

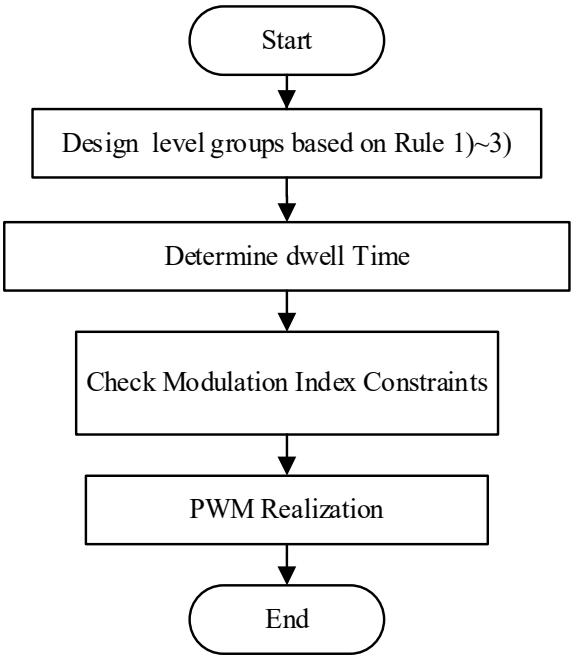


Figure 4.10 Design procedure of SEPWM

The aforementioned procedures are further summarized in the flow chart in Figure 4.10. With the procedure applied, one can improve the unclamped capacitor voltage balancing performance for unclamped capacitor topologies with incomplete capacitor-voltage-balancing capability. As carrier-based PWM approach is used, the implementation is more straightforward than those method based on SVM [122].

4.3 Design Example: Stair Edge PWM for Four-Level NNPC

To illustrate the design details of SEPWM method, a design example is given here. The proposed design rules and procedures will be applied to a 4L-NNPC converter.

The 4L- NNPC is a recently proposed multilevel topology [123]. As shown in Figure 4.11, it has 6 switches, 2 diodes and 2 unclamped capacitors in each phase leg. Its advantages are [124]: 1) all devices have the same voltage stress, i.e., one-third of DC-link voltage; 2) it has fewer components when comparing to other 4L topologies; (3) it is suitable for wide operation range: 2.4-7.2KV; (4) no series-connected switches are needed.

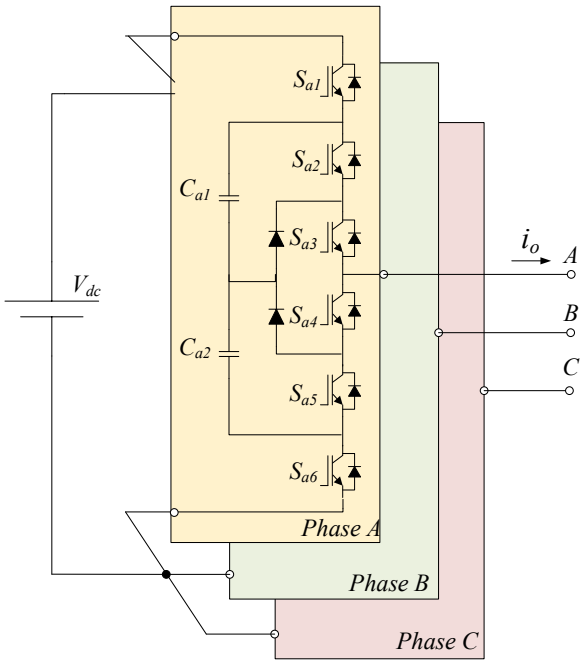


Figure 4.11 Topology of 4L-NNPC

However, like other MLCs with unclamped capacitors, its unclamped capacitor voltages need to be balanced [125]. Lacking enough redundant switch states, there is always one (out of the two) capacitor cannot be adequately controlled during each half fundamental period when normal multilevel PWM methods are applied. As a result, the voltage ripple amplitudes on these unclamped capacitors are related to fundamental frequency [126]. To be more specific, the voltage ripple is inverse-proportional to the output frequency. This will be illustrated in detail in the following section. Hence, the fundamental frequency voltage ripple is a concern when NNPC Converters are applied in VFD systems where the fundamental frequency can be very low at low speeds. To guarantee acceptable output quality may lead to large capacitance for the unclamped capacitors. If the unclamped capacitor voltage ripple can be controlled within an acceptable range even under very low fundamental frequencies, it is possible to employ this topology to build cost-effective wide speed range VFD systems.

4.3.1 Normal Multilevel PWM Method and the Voltage Balancing Difficulty in Four-Level NNPC

Generally, to generate PWM for a 4L-converter, SPWM, such as level-shift PWM (LSPWM), phase-shift PWM (PSPWM), and SVM can be used. Taking LS PWM as an example, three different carrier waves will be used, as shown in Figure 4.12. With PWM generated, state selection is necessary to guarantee proper output level and unclamped capacitor voltage balancing.

TABLE 4.2 The Switching States of 4L-NNPC and the Corresponding Impact on Floating Capacitors

Output Voltage	Output Level	State	Switching States of Power devices						Impact on C_{p1}		Impact on C_{p2}	
			S_{p1}	S_{p2}	S_{p3}	S_{p4}	S_{p5}	S_{p6}	$i_o>0$	$i_o<0$	$i_o>0$	$i_o<0$
$Vdc/2$	4	6	1	1	1	0	0	0	-	-	-	-
$Vdc/6$	3	5	0	1	1	0	0	1	D	C	D	C
		4	1	0	1	1	0	0	C	D	-	-
$-Vdc/6$	2	3	1	0	0	1	1	0	C	D	C	D
		2	0	0	1	1	0	1	-	-	D	C
$-Vdc/2$	1	1	0	0	0	1	1	1	-	-	-	-

Note: 'C' means charge, 'D' means discharge, and '-' means no impact

The applicable switching states for NNPC is shown in TABLE 4.2, in which $S_{p\#}$ (p=a, b, c and # =1, 2, 6) indicates the ON/OFF state of the power switches. From the table, it can be found that the state of S_{p1} is complementary to S_{p6}, whose relationship also applies to S_{p2} and S_{p4}, S_{p3} and S_{p5}. Theoretically, there should be 8 different states, while only 6 of them are applicable. These states have different impacts on the unclamped capacitors, making it possible to balance the unclamped capacitor at $V_{dc}/6$ to generate a 4L voltage. To achieve this, redundant switching states for unclamped capacitor voltage balancing are available for *Level 2* and *Level 3*, i.e., output voltage equals to $V_{dc}/6$ and $-V_{dc}/6$. While level 1 and level 4 have no impact on the unclamped capacitors.

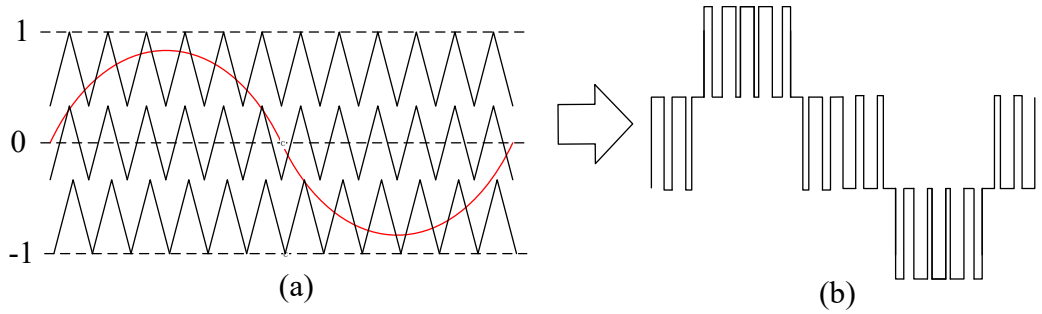


Figure 4.12 Level-shift PWM for NNPC: (a) Level shift PWM; (b) output voltage waveform

However, these redundant switching states cannot achieve complete control of the unclamped capacitor voltages. For example, assume that the output current is positive (i_o>0), and the modulation reference is also positive, *Level 3* and *Level 4* will be used to generate proper outputs in a long duration. In this condition, *State 4- 6* will be used. The upper floating capacitor C_{p1} can be either charged (*State 4*) or discharged (*State 5*). Meanwhile, *State 5* will unavoidably discharge the lower floating capacitor C_{p2} while neither state 4 nor state 6 have any impact on it. As a result, C_{p2} will always be discharged under this condition. On the contrary, when the output current is negative (i_o<0), C_{p2} can only be charged. A similar situation happens to C_{p1} when the output level switch between *Level 1* and *Level 2* in the negative half of the fundamental period. As a result, fundamental frequency voltage ripples will appear on the floating capacitors even proper switching states are used. The voltage ripple amplitude can be calculated as (4.1) [126]:

$$\Delta V_{FC} = f(m,\cos\varphi)\cdot\frac{I_{rms}}{f_O\cdot C_{FC}} \tag{4.1}$$

where I_{rms} is the r.m.s value of output current, f_O is the output frequency, and C_{FC} is the capacitance of the floating capacitors. The coefficient $f(m, \cos\varphi)$ is a function of modulation index m and output power factor $\cos\varphi$.

The capacitance can be designed to limit the fundamental frequency ripple. However, when coping with the large frequency range (e.g., 0-60Hz) operation, it is challenging to design the capacitance as the low frequency requires large capacitance to attenuate the voltage ripple. The low-frequency operation of NNPC is thus limited due to the limited voltage balancing capability.

4.3.2 SEPWM Design for Four-Level NNPC

As illustrated above, NNPC suffers from the fundamental-frequency voltage ripples on its floating capacitors when using general multilevel PWM method. The available redundant switch states within one switching period can only balance one of the floating capacitors while partially influencing the voltage on the other one. On the other hand, it is impossible to find other switching states to balance the unclamped capacitors.

To improve the voltage balancing even under very low fundamental frequency, the proposed SEPWM can be applied. Again, the switching table is shown in TABLE 4.3. It can be observed that the two unclamped capacitors (floating capacitors in this case) can both be balanced when state 2-5 are all available, producing *Level 2* and *Level 3*. Thus *Level 2* and *Level 3* are Edge levels containing balancing states. On the other hand, *Level 1* and *Level 4* have no impact on the floating capacitors, meaning they can be assigned to be dominant levels. To fulfill the design rules listed in Section II, the 4 output levels are assigned to 2 different groups, as shown in TABLE 4.3. As a result, *Group 1* consists of *Level 1- Level 3,* while *Group 2* consists of *Level 2-Level 4*. The edge levels (Level *2* and Level *3*) are assigned to both level groups to perform floating capacitors voltage balancing.

TABLE 4.3 Level Group of 4L-NNPC

Output Voltage	Output Level	State	Impact on C_{p1}		Impact on C_{p1}		Level Type	*Group 1*	*Group 2*
			$i_o>0$	$i_o<0$	$i_o>0$	$i_o<0$			
Vdc/2	4	6	-	-	-	-	Dominant Level	No	Yes
Vdc/6	3	5	D	C	D	C	Edge Level	Yes	Yes
		4	C	D	-	-			
-Vdc/6	2	3	C	D	C	D	Edge Level	Yes	Yes
		2	-	-	D	C			
-Vdc/2	1	1	-	-	-	-	Dominant Level	Yes	N

Note: 'C' means charge, 'D' means discharge, and '-' means no impact

With the group assigned, an example output voltage is shown in Figure 4.13. As can be seen, *Level 2* and *Level 3*, which offer sufficient balancing switching

states, are always used during the whole fundamental period. The floating capacitors can be balanced at the switching frequency as charge and discharge switching state for each capacitor are available under any current directions.

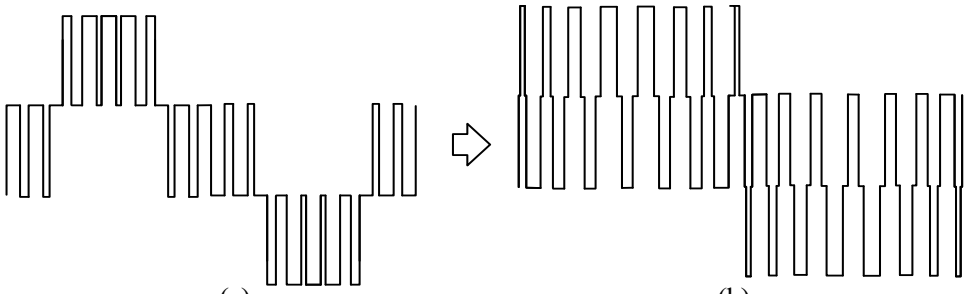


Figure 4.13 Output phase voltage waveform: (a) normal multilevel PWM; (b) SEPWM

However, simply inserting *Level 2* and *Level 3* without designing their dwell time will change the voltage-second product, influencing the actual modulation index. Taking the voltage-second product of 2L-PWM as the reference, the SEPWM should obtain the same voltage-second product. As mentioned previously, the dwell time of balancing state can be constant or variable with respect to the duty cycle. The latter is more complicated but gives the potential to obtain longer dwell time. Thus, variable dwell time design is used as an example in this chapter. The following analysis will find a relationship between SEPWM and the 2-level PWM to archive the same voltage-second product.

As shown in Figure 4.14, the 2L-PWM switching period is T_s. The dwell time of the $-V_{dc}/2$ state is T_0 , then the dwell time of $V_{dc}/2$ state is T_s-T_0. The voltage-second product of 2L-PWM in one switching period, $P_{V\text{-}S}$, can be expressed as (4.2):

$$P_{v-s} = -\frac{V_{dc}}{2} \cdot T_0 + \frac{V_{dc}}{2} \cdot (T_s - T_0) \tag{4.2}$$

In the positive half cycle (V_{ref} >0), *Group 2* will be used. Assuming the dwell time of *Level 2* and *Level 3* in SEPWM are both ΔT. Making them equal will make sure the switching states for balancing can be applied with the same interval in one switching period. Then, $P'_{V\text{-}S+}$, the voltage second product of SEPWM in one switching period in the positive half, can be expressed as:

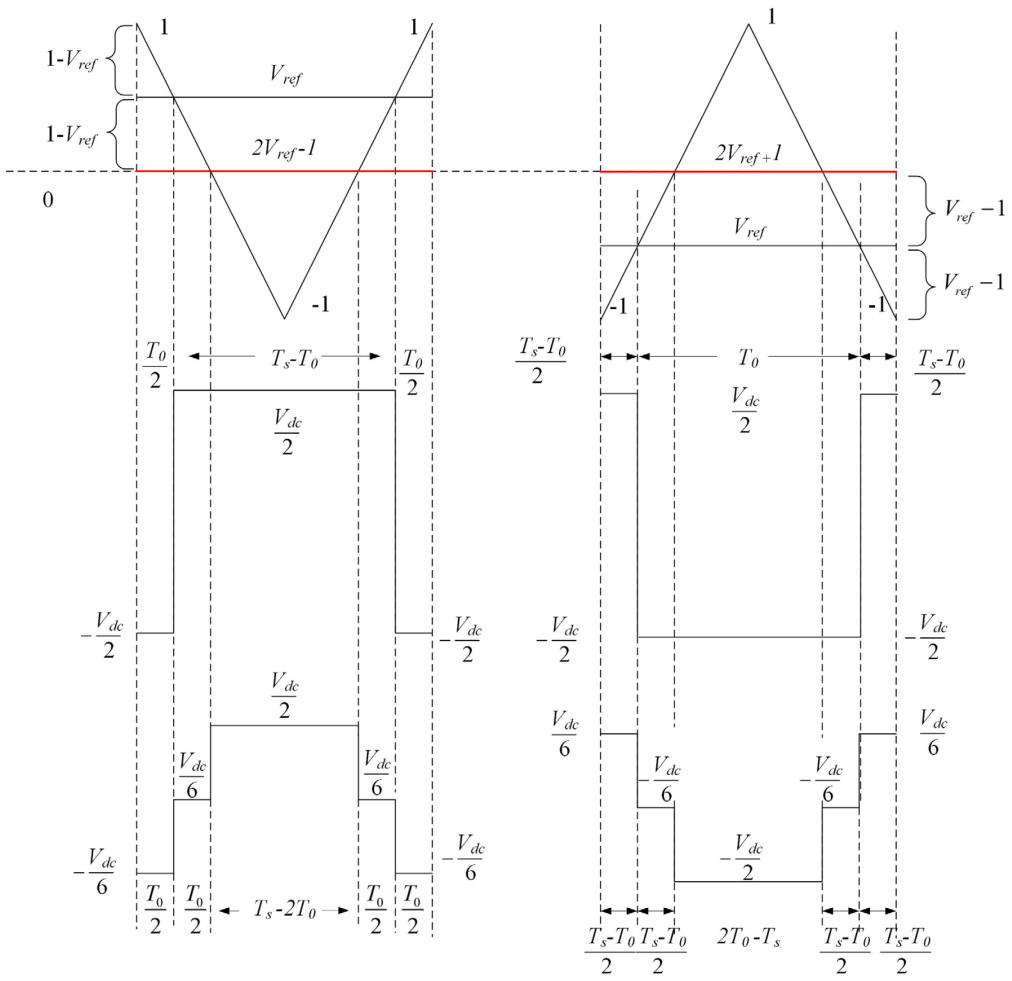


Figure 4.14 Voltage second product of 2L-PWM and SEPWM

$$P'_{V-S+} = \frac{V_{dc}}{6} \cdot \Delta T - \frac{V_{dc}}{6} \cdot \Delta T + \frac{V_{dc}}{2} \cdot (T_s - 2\Delta T) \tag{4.3}$$

For the negative half (V_{ref}<0), the volt-sec product $P'_{V\text{-}S\text{-}}$ is:

$$P'_{V-S-} = \frac{V_{dc}}{6} \cdot \Delta T - \frac{V_{dc}}{6} \cdot \Delta T - \frac{V_{dc}}{2} \cdot (T_s - 2\Delta T) \tag{4.4}$$

In order to maintain the voltage-second product, (4.5) has to be fulfilled:

$$\begin{cases} P'_{V-S+} = P_{V-S} \ (V_{ref} > 0) \\ P'_{V-S-} = P_{V-S} \ (V_{ref} < 0) \end{cases} \tag{4.5}$$

Then, the following relationship can be obtained:

$$\begin{cases} \Delta T = T_0 & (V_{ref} > 0) \\ \Delta T = T_s - T_0 & (V_{ref} < 0) \end{cases} \tag{4.6}$$

As shown in (4.6), ΔT, the dwell time of output *Level 2* and *Level 3*, is equal to the dwell time of State $-V_{dc}/2$, i.e., T_0. So, SEPWM can be modulated by modifying 2-level carrier-based modulation. It is easy to derive from Figure 4.14 that the modulation references can be set to the original reference V_{ref}, $2V_{ref}-1(V_{ref}>0)$ or $2V_{ref}+1$ $(V_{ref}<0)$, and 1 $(V_{ref}>0)$ or $-1(V_{ref}<0)$. The newly added modulation references are either simple transformations of the original reference or constants. The carrier wave is set to be a triangle wave, which is the same as 2-level PWM. The modulation waveforms are shown in Figure 4.15.

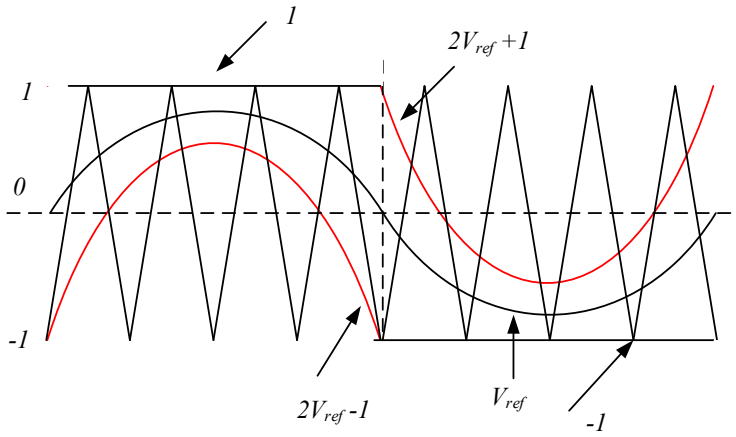


Figure 4.15 An SEPWM realization example

The proposed modulation method is straightforward for realization. Comparing to the normal PWM method, only a few simple manipulations of the modulation reference is needed. However, the balancing of the floating capacitors will be significantly improved.

4.3.3 Constraints of Modulation Index

The dwell time of edge levels must be long enough to maintain the low *dv/dt* as an MLC. As can be seen from Figure 4.16, the dwell time ΔT is related to the offset added to the modulation reference. Then the maximum modulation index should be limited to avoid over-modulation, which will lead ΔT to be smaller than expected. When the number of edge levels N_{Ex} is an odd number $2n_{Ex}+1$, the

leading/delay time of the rising/falling edge (comparing to a standard 2-level waveform) will be $(n_{Ex}+0.5)\bullet \Delta T$, and it will be $n_{Ex}\bullet \Delta T$ when the number of edge levels is an even number $2\ n_{Ex}$.

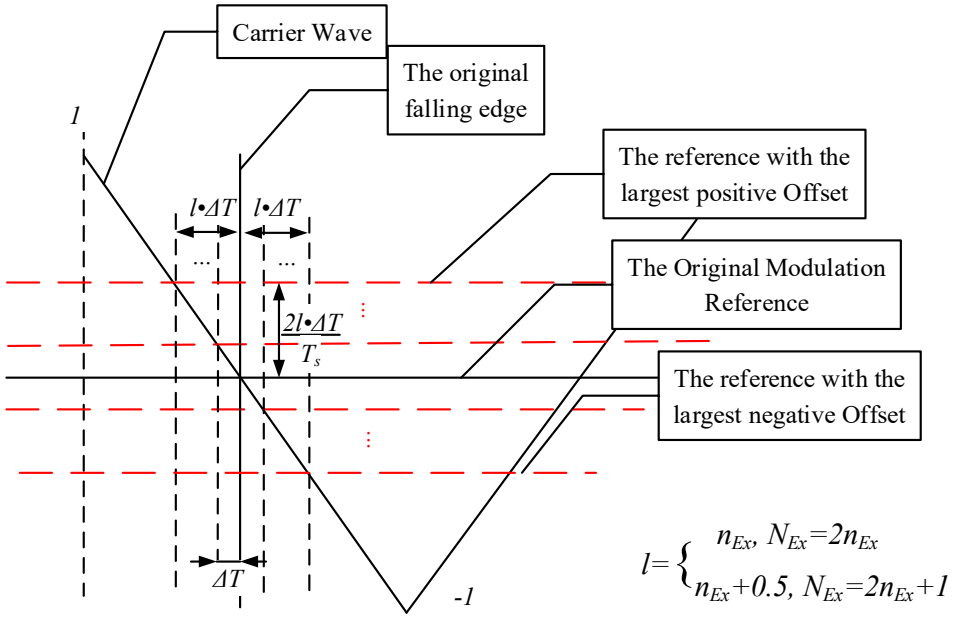


Figure 4.16 The relationship between the reference offset and the lead/delay time of the PWM signal: a zoom-in view of the modulation waveform

The total loss of one switching cycle, including both rising and falling edge, should be $2l\bullet\Delta T$, or $N_{Ex}\bullet\Delta T$, Then the loss of modulation index m_L fulfills (4.7):

$$\frac{m_L}{N_{Ex}\cdot\Delta T}=\frac{1}{T_s} \tag{4.7}$$

(4.7)can be rewritten as (4.8):

$$m_L=\frac{N_{Ex}\Delta T}{T_s} \tag{4.8}$$

Therefore, the maximum modulation index is 1-m_L in a normal SPWM method. When 3rd order harmonic injection SPWM [127] is used, where the maximum modulation index is 1.15, the maximum modulation index will be 1.15-m_L. The minimum ΔT should be several microseconds, as discussed earlier. Taking 5 μs as an example and N_{Ex}=2, the maximum modulation index in a system with 1080 Hz

switching frequency will be 0.989 and 1.139 under the two methods respectively, when the effect of dead time is neglected.

4.3.4 Active Floating Capacitor Voltage Balancing Method

As illustrated in the previous subsections, *Level 2* and *Level 3* are used with the same dwell time in one switching period. Theoretically, the capacitor voltage can be balanced naturally by only using *State 3* and *State 5*, which can charge or discharge the two capacitors with the same interval in SEPWM. However, the average charging or discharging current in one switching period is not perfectly equal, and power losses on components will also affect the capacitor voltage balancing. As a result, the active unclamped capacitor voltage balancing is still necessary, but much easier to realize than using the original multilevel PWM methods.

According to the switching states and their impacts on unclamped capacitors shown in TABLE 4.2, for the same output level, different switching states can be selected to balance the capacitor voltage. For *Level 3*, *State 4* and *State 5* can be selected to control upper capacitor C_{p1} while *State 2* and *State 3* for *Level 2* can be selected to control lower capacitor C_{p2}. According to the impacts of switching states, switching state selection for voltage balancing is summarized in TABLE 4.4.

TABLE 4.4 Switching State Selection for Voltage Balancing

Output level	Output voltage	Capacitor Voltage	Current Direction	*State*
Level 3	$+V_{dc}/6$	$V_{Cp2}>V_{dc}/3$	$i_o>0$	5
			$i_o<0$	4
		$V_{Cp2}<V_{dc}/3$	$i_o>0$	4
			$i_o<0$	5
Level 2	$-V_{dc}/6$	$V_{Cp1}>V_{dc}/3$	$i_o>0$	2
			$i_o<0$	3
		$V_{Cp1}<V_{dc}/3$	$i_o>0$	3
			$i_o<0$	2

The switching state selection is the same with normal multilevel PWM methods. However, due to *Level 2* and *Level 3* are always generated by the switching sequence, proper states can always be used to charge and discharge within one switching period. On the contrary, the normal PWM will have to wait

half of the fundamental period before it can use the absent states, making one of the two capacitor voltages keeping rising or dropping in a long interval — half of the fundamental period.

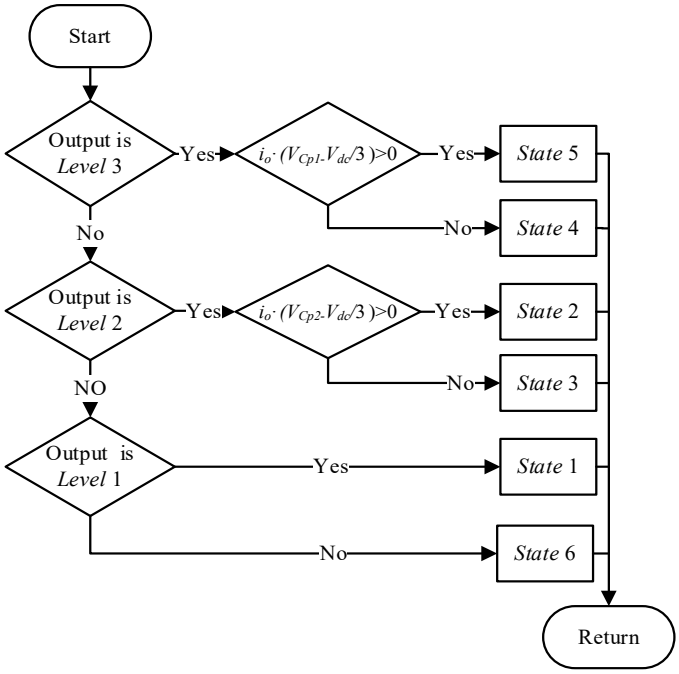


Figure 4.17 Flowchart to determine switch states for active unclamped capacitor voltage balancing in SEPWM

Figure 4.17 shows the flow chart to determine the switch states to be applied. The switch states selection for *Level 1* and *Level 4* is straightforward as no redundant states can be used. For *Level 2* and *Level 3*, two states with opposite impacts on the unclamped capacitors for each level can be used. The products of output current i_o and voltage errors, i.e., (C_{p1}-$V_{dc}/3$) and (C_{p2}-$V_{dc}/3$), are thus taken as the standard to select the proper switch state. The switch state should be selected for every applied level only once in each switching period to avoid increasing the actual switching frequency unnecessarily.

4.4 Simulation and Experiment Results

4.4.1 Simulation Verification

To compare the proposed SEPWM method and the normal multilevel PWM method (LS-PWM), an NNPC converter is built in Matlab/Simulink. The system parameters are shown in TABLE 4.5.

TABLE 4.5 System Parameters in Simulation

Parameters	Values
Rated Power	5000KVA
Rated Voltage	7200V
DC Voltage	11.7 kV
Floating Capacitor	4500 μF
Switching Frequency	1080 Hz
Output Inductor	12.1 mH
Load Resistance	9.3 Ω

Figure 4.18 and Figure 4.19 are simulation results when the modulation index is 0.45, and the fundamental frequency is set to be 1 Hz under two PWM methods. Figure 4.18 shows the operation when normal LSPWM is applied, whose modulation method is shown in Figure 4.15. The three-phase capacitor voltages suffer from large variations in every fundamental period, even though they keep stable at 3900V for half of the period due to the voltage balancing control. As a result, both the output voltage and the output current are distorted due to the large low-frequency ripples on the capacitors.

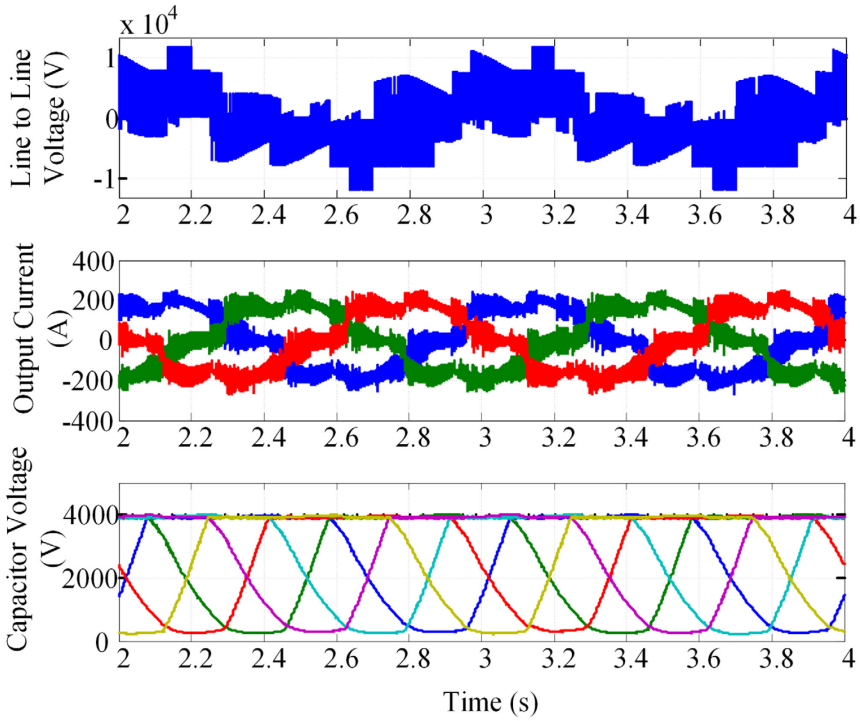


Figure 4.18 Simulation results of normal multilevel PWM at 1Hz (from upper to lower): output line-to-line voltage (V_{AB}), output current, capacitor voltage (three-phase)

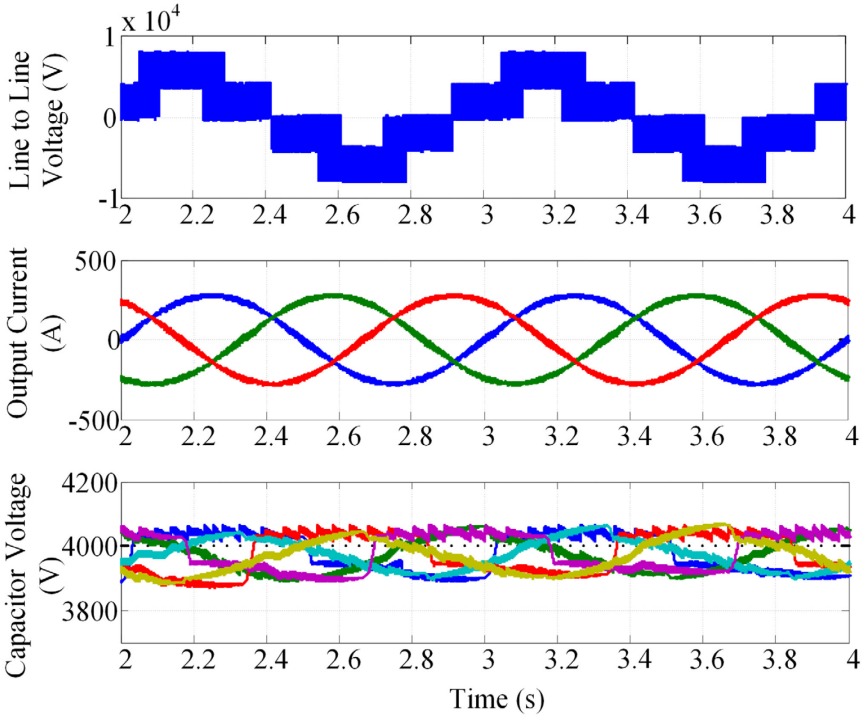
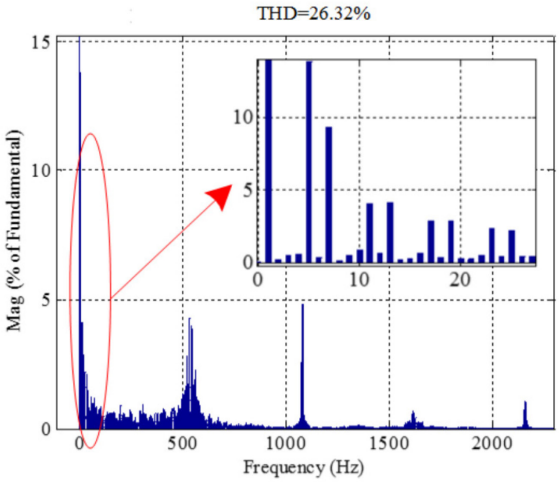
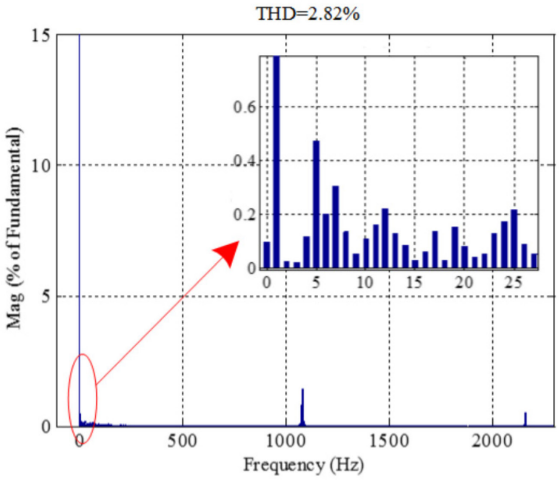


Figure 4.19 Simulation results of SEPWM at 1Hz (from upper to lower): output line-to-line voltage (V_{AB}), output current, capacitor voltage (three-phase)



(a)



(b)

Figure 4.20 FFT analysis of the output current: (a) normal PWM method; (b) SEPWM method

When the proposed SEPWM is applied, the capacitor voltage ripple is much smaller than that in LSPWM. As shown in Figure 4.19, the voltage ripple amplitude is about within 5% of the rated capacitor voltage. Hence, the output quality is maintained. The output line-to-line voltage is ideal multilevel voltage waveform, and the output current is sinusoidal with some small high-frequency ripples while no low-frequency distortion can be observed.

The FFT analysis of the output currents under the two different methods is shown in Figure 4.20, which clearly shows the output quality improvement brought by the SEPWM. As shown in Figure 4.20 (a), the output current contains lots of

harmonics, both in high orders and low orders. The 5th and 7th order harmonics are around 10% of the fundamental components, which is mainly caused by the voltage ripples of the unclamped capacitors. On the contrary, when the SEPWM method is applied, the THD under the same situation drops from 26.32% to 2.82%, as shown in Figure 4.20 (b). The low order harmonics are decreased significantly—no low order harmonic component reaches 0.5%, as the result of the reduced amplitude of unclamped capacitor voltage ripples. The reduction of low order harmonics is more important than the reduction of high-frequency harmonics as they are more challenging to filter out.

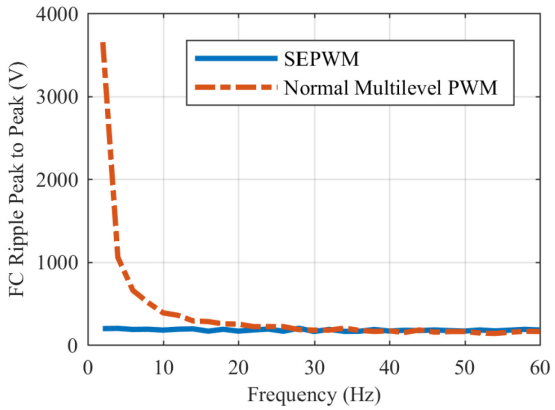
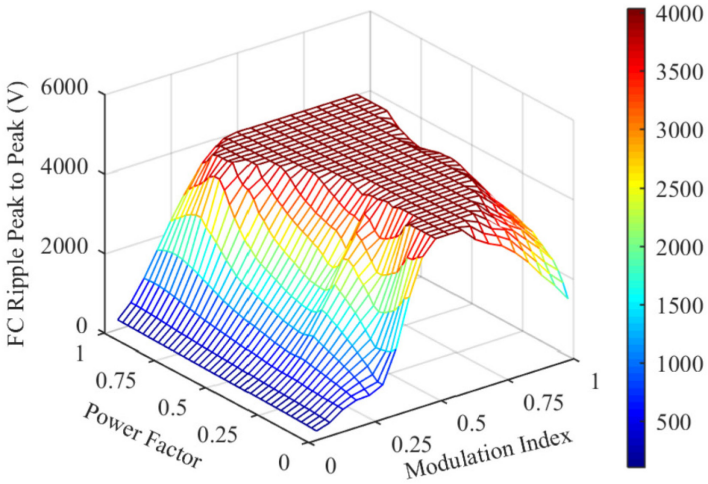


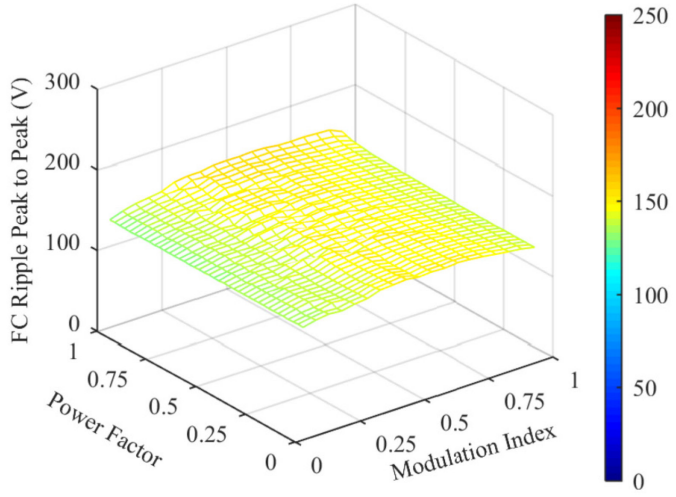
Figure 4.21 Amplitudes of voltage ripples under different fundamental frequency for 4L-NNPC with SEPWM or normal multilevel PWM

To further verify the unclamped capacitor (floating capacitor) voltage balancing performance under different frequencies, the ripple amplitude under the two methods are depicted in Figure 4.21, where the modulation index and power factor are both 0.5. As can be observed from Figure 4.21, for the normal multilevel method, when the fundamental frequency decreases, the voltage ripple increases significantly. The curve verifies that the amplitudes of voltage ripples are reciprocal to the fundamental frequency, which is indicated by (1). However, when the SEPWM is applied, the amplitudes of voltage ripples are no longer related to the fundamental frequencies. This can be seen from the flat curve of voltage ripple amplitude throughout the output frequency variation range when SEPWM is applied. As expected, the unclamped capacitor voltage ripples of NNPC under low

frequency and wide operation range can be significantly reduced by the proposed SEPWM.



(a)



(b)

Figure 4.22 The unclamped capacitor voltage ripple peak to peak under different modulation indexes and power factors at 1Hz: (a) normal multilevel PWM; (b) SEPWM

The peak to peak values of floating capacitor ripples under 1Hz normal multilevel operation and SEPWM operation with different modulation index and power factor are shown in Figure 4.22(a) and (b). As shown in Figure 4.22(a), the amplitudes of voltage ripples under multilevel operation will increase to extremely high values when the modulation index is close to 0.5, while high power factors will lead to larger modulation index range with high ripples. This matches the

results in Figure 4.18 and further proves that the normal multilevel operation cannot work under low frequencies. On the contrary, the amplitudes of floating capacitor ripples under SEPWM keep almost constant regardless of the modulation index and power factor, as shown in Figure 4.22 (b).

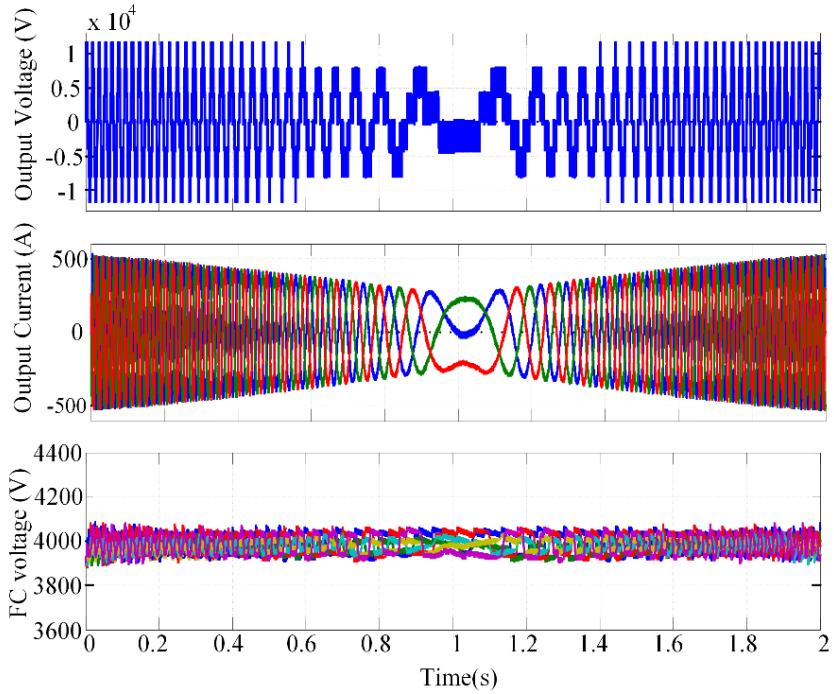


Figure 4.23 The operation of 4L-NNPC with SEPWM when fundamental frequency changes from 60Hz to 1Hz and back to 60Hz (from upper to lower): Output voltage, output current, and voltage ripple on unclamped capacitors

To verify the feasibility of SEPWM in VFD application, the converter is operated to change its output frequency and amplitude to mimic the behavior of a power converter under the variable voltage, variable frequency (VVVF) control. As shown in Figure 4.23, the fundamental frequency changes from 60Hz to 1Hz and back to 60Hz. Meanwhile, the modulation index changes from 0.8 to 0.4 and back to 0.8. During the frequency variation, the amplitudes of voltage ripples keep almost constant, and the output currents keep high quality. It is worth to note that this configuration about modulation index and frequency is not necessarily a practical combination in industrial application. The simulation is only to prove that with the proposed SEPWM, the NNPC can operate in a large frequency range with very small unclamped capacitor ripples.

4.4.2 Experimental Verification

A three-phase 4L-NNPC prototype is built for experiment verification, as shown in Figure 4.24. The control system is a DSP and FPGA platform. Current sensors and voltage sensors are added to measure the output current and unclamped capacitor voltages. The modulation index is set to 0.9. The system parameters are shown in TABLE 4.6.

TABLE 4.6 Parameters of Experimental Prototype

Parameters	Values
DC Voltage	120 V
Floating Capacitor	1000 μF
Switching Frequency	960 Hz
Output Inductor	30 mH
Load Resistance	14 Ω

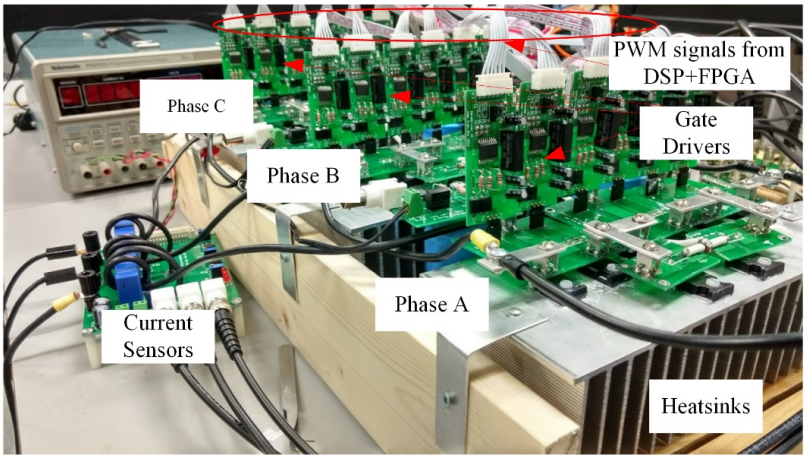


Figure 4.24 Experimental setup of 4L-NNPC

The experimental results are shown in Figure 4.25. To compare the unclamped capacitor voltage ripples, the NNPC is operated with both normal PWM method and the proposed SEPWM method. The SEPWM produces different multilevel output line voltage compared to the normal multilevel output, as shown in Figure 4.25 (a) and (b). The difference in unclamped capacitor voltage balancing can also be easily observed. As can be seen from Figure 4.25(a) and (b), both methods can perform well when the fundamental frequency is 60Hz. The amplitudes of

fundamental-frequency ripples are small, and as a result, the output voltage and current are of high quality.

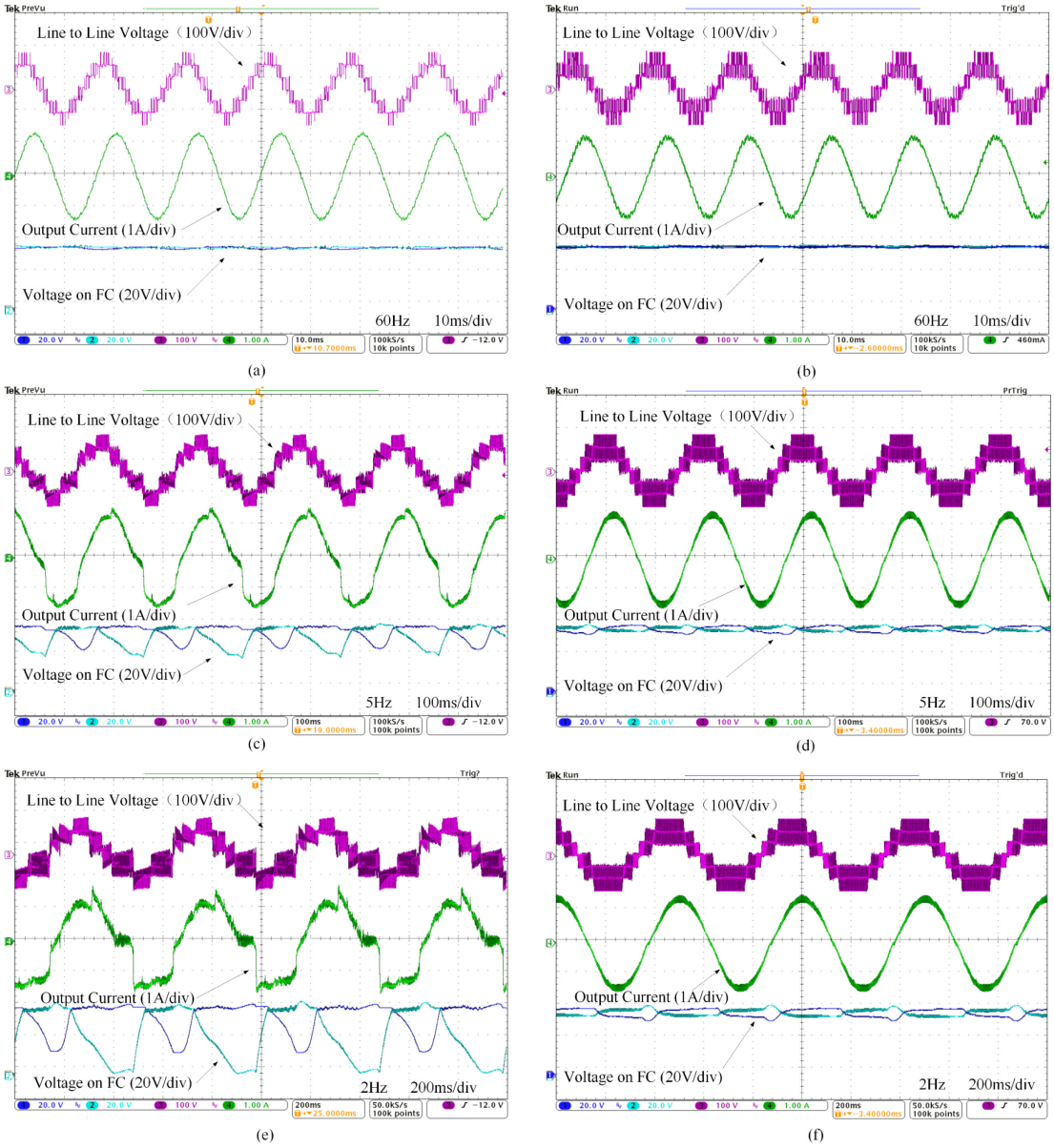


Figure 4.25 Experimental results: (a) normal multilevel PWM under 60Hz; (b) SEPWM under 60Hz; (c) normal multilevel PWM under 5Hz; (d) SEPWM under 5Hz; (e) normal multilevel PWM under 2Hz; (f) SEPWM under 2Hz

However, when the fundamental frequency reduces to 5Hz, as shown in Figure 4.25(c) and (d), large ripples on unclamped capacitors under normal PWM method have led to a significant distortion in both output voltage and current. On the other

hand, the proposed SEPWM still ensures the NNPC produces high-quality output. The voltage ripples on the unclamped capacitor are much smaller than that of normal multilevel operation.

When the NNPC converter works under very low frequencies like 2Hz, the unclamped capacitor voltage can drop close to 0V with normal multilevel PWM applied. The amplitudes of voltage ripples reach 1 p.u when taking the expected unclamped capacitor voltage as the base. On the contrary, the ripple amplitude is still much smaller when SEPWM is applied. Also, the power quality under SEPWM is still guaranteed, which can be observed from Figure 4.25(e) and (f).

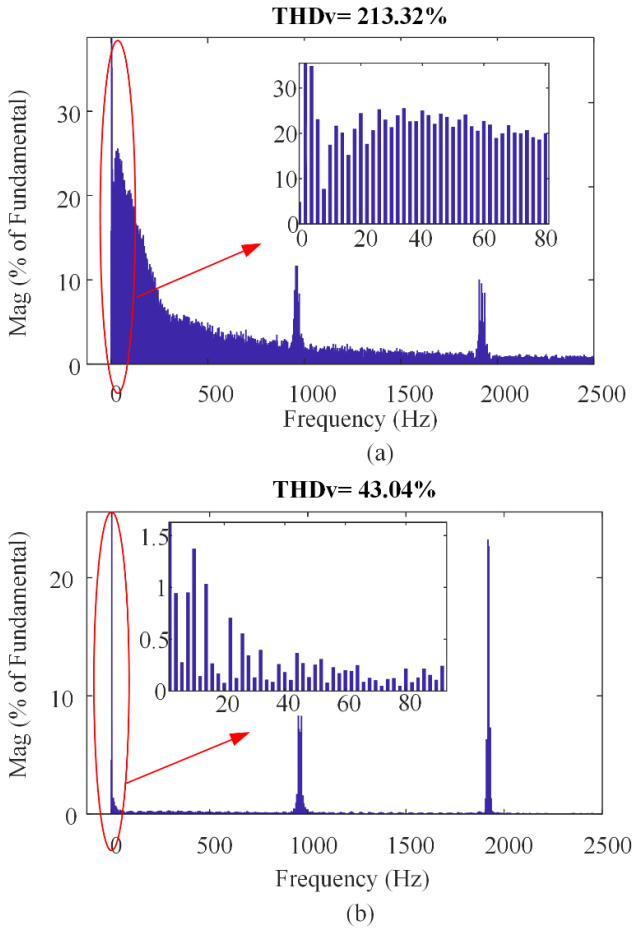


Figure 4.26 FFT analysis of the 2Hz line-to-line voltage obtained in the experiment: (a) normal multilevel PWM method; (b) SEPWM method

The different unclamped capacitor voltage balancing performance leads to significant differences in output quality, particularly under the low frequency. The

FFT analysis of line-to-line voltage produced by the NNPC converter at 2Hz is shown in Figure 4.26. The normal multilevel PWM method generates a large number of low order harmonics (see in Figure 4.26(a)) due to the large low-frequency ripples in unclamped capacitor voltage, leading THD of voltage (THDv) to be more than 200%. With SEPWM applied, the improve unclamped capacitor voltage leads to a significant reduction of low-order harmonics (see Figure 4.26(b)) and much lower THDv, which is 43%. It can also be seen that the 2kHz harmonics are increased slightly from 12% in normal multilevel PWM to 24%.

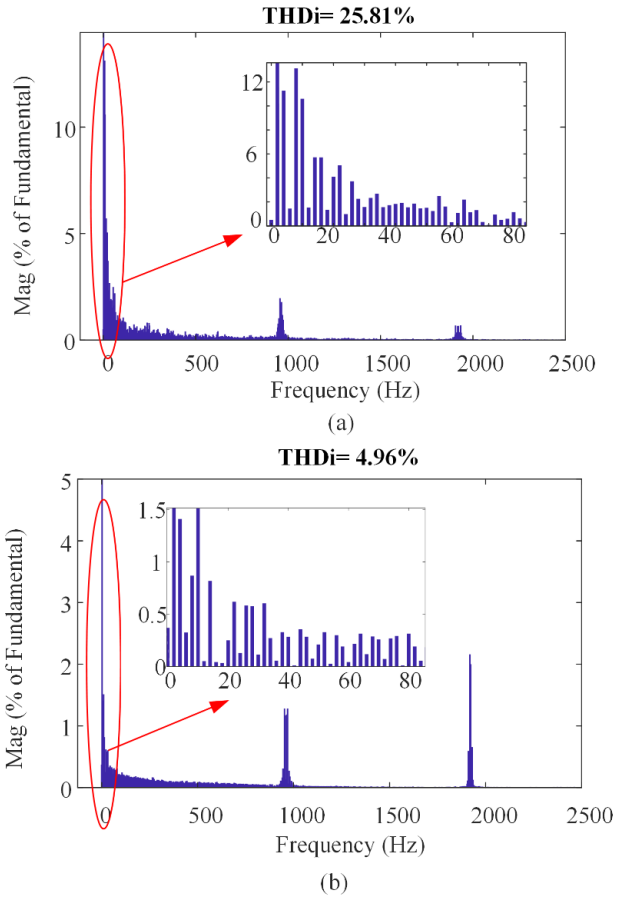


Figure 4.27 FFT analysis of the 2Hz output current obtained in the experiment: (a) normal multilevel PWM method; (b) SEPWM method

The differences in power quality are also illustrated in the FFT analysis of output current. In Figure 4.27, the output currents under 2Hz operation with both methods are analyzed. By using the normal PWM method, the THD of current

(THDi) reaches as high as 25.82%, containing large amounts of low order harmonics due to the voltage ripples on unclamped capacitors, which is consistent to the FFT result of the line-to-line voltage. On the contrast, the proposed SEPWM can maintain the THDi to be as low as 4.96% even under 2Hz operation, due to the well-balanced unclamped capacitor voltages. The high-frequency current harmonics also increases slightly. However, considering the high-frequency harmonics are easy to filter out. this will not be an issue.

Overall, the experimental results match well with simulation results, proving the unclamped capacitor voltage balancing is significantly improved by SEPWM method. With the SEPWM applied, the 4L-NNPC can operate under very low frequencies while keeping low ripple amplitude on the unclamped capacitors and thus obtaining high output quality.

4.5 Conclusions

In this chapter, a new PWM method, named Stair Edge PWM (SEPWM), is proposed to improve floating-capacitor-balancing for topologies with the incomplete capacitor-voltage-balancing capability. The incomplete capacitor-voltage-balancing capability is because the topology lacks redundant switch states to control the capacitor voltages, leading to fundamental-frequency voltage ripples on its unclamped capacitors. To improve the unclamped capacitor voltage balancing performance, the proposed PWM utilizes more available balancing switching states in one switching period to improve voltage balancing without changing voltage stress on switching devices and the *dv/dt* applied to the loads. Meanwhile, the output voltage second product is also maintained by proper design of the dwell time of each level. Taking a 4L- NNPC converter as an example, the design of the proposed SEPWM is discussed in detail. Through both theoretical analysis and simulation/experimental verifications, it shows that the proposed method can significantly improve the voltage balancing of NNPC even under low output frequencies when compared to the normal multilevel PWM method. Meanwhile, the output quality is also improved by reducing the unclamped capacitor voltage ripples.

Chapter 5

Seven Level Hybrid Clamped (7L-HC) Converter and the Capacitor-Balancing[1]

In Chapter 4, a general PWM method for MLCs is proposed to enhance the capacitor voltage balancing. This method can be applied for the topologies with incomplete capacitor-balancing capability. Alternatively, the capacitor ripple issues can also be addressed by topology-based methods, including ancillary circuits and new topologies. However, topology-based methods usually require adding more components, increasing the system cost. Hence, it is necessary to find ancillary circuits or topologies with low numbers of devices. In this chapter, a novel multilevel topology with low device count and the ability to balance all the capacitors is proposed.

5.1 Existing Topology-based Approaches for Capacitor Balancing

Besides the control approaches discussed in Chapter 4, the capacitor-balancing of the MLC can also be enhanced by adding ancillary circuits to existing topologies or inventing new topologies with complete capacitor-balancing capability.

5.1.1 Ancillary Balancing Circuits

Ancillary balancing circuits require extra costs on devices but help achieve the capacitor-balancing for topologies with difficulties to balance their capacitors. The

[1] Publication out of this chapter:

H. Tian, Y. Li and Y. W. Li, "A Novel Seven-Level Hybrid-Clamped (HC) Topology for Medium-Voltage Motor Drives," in IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5543-5547, July 2018.
H. Tian and Y.W. Li, "An Active Capacitor Voltage Balancing Method for Seven Level Hybrid Clamped (7L-HC) Converter in Motor Drives," in IEEE Transactions on Power Electronics. doi: 10.1109/TPEL.2019.2929558.

balancing circuits can transfer energy from one capacitor to another, and thus are very suitable for topologies with series-connected capacitors, particularly the DC-link capacitors. A typical balancing circuit is shown in Figure 5.1 (a), where a balancing circuit is built by a half-bridge and an inductor L[115]. The capacitor C_1 and C_2 are capacitors in the MLC. Properly controlling the switch S_{BC1} and S_{BC2}, the voltage on C_1 and C_2 can be equalized. Then the converter only needs to control the total voltage on C_1 and C_2 if the two capacitors are not clamped. When the voltage stress on the two capacitor C_1 and C_2 is high, multilevel phase-leg based balancing circuits can be used, such as the one in Figure 5.1 (b)[116]-[117]. Also, the NPC phase-leg can be used[118].

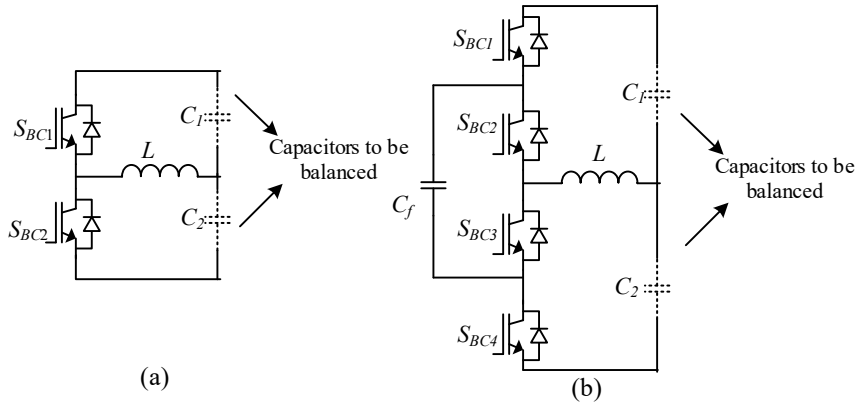


Figure 5.1 Examples of ancillary balancing circuits: (a) half-bridge based balancing circuit; (b) flying capacitor phase-leg based balancing circuit

As an example, the balancing circuits in Figure 5.1 (a) is applied to a 9L converter to help balance the floating capacitors. The topology is shown in Figure 5.2 (a). The 9L-converter only has 10 switches and two floating capacitors. The low device count results in the small number of redundant switching states for balancing. The topology itself cannot operate without the help of balancing circuits. The balancing circuits can be easily controlled by feeding 50% duty ratio PWM to the complementary switches S_{BC1} and S_{BC2}. Also, a Proportional Integral (PI) controller based control scheme can be used to obtain better voltage balancing performance, shown in Figure 5.2 (b).

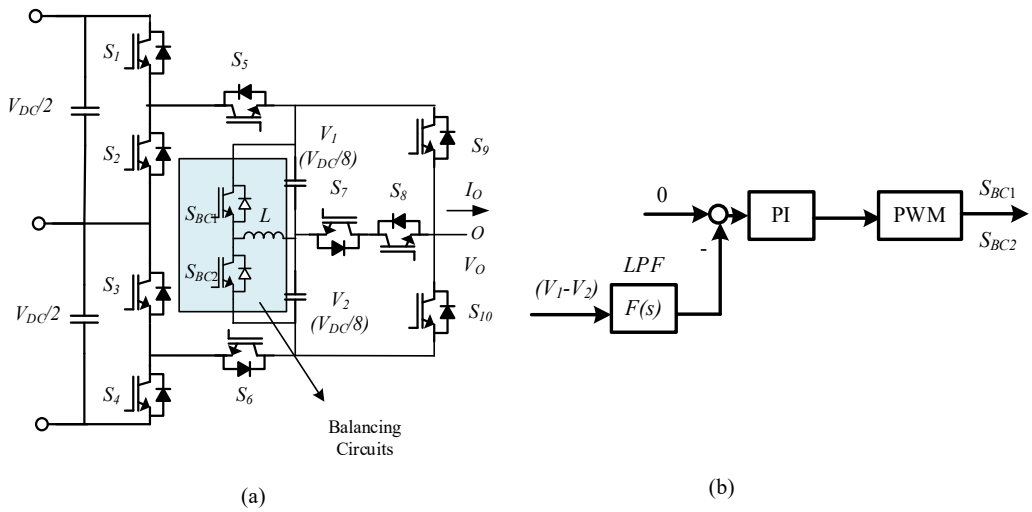


Figure 5.2 9L-converter with ancillary balancing circuits: (a) topology; (b) control scheme of balancing circuits

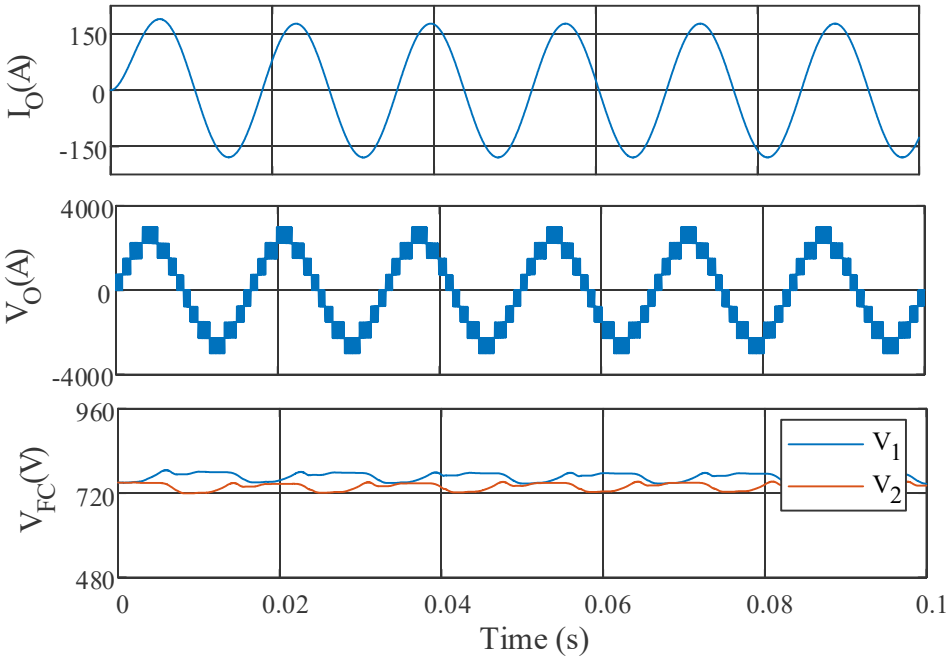


Figure 5.3 Simulation results of balancing circuits in the 9L-converter

The simulation results are shown in Figure 5.3. As can be seen, the voltage V_1 and V_2 are equalized. Controlling the two voltage to be $V_{DC}/8$, the output voltage waveforms and output current also shows high quality.

5.1.2 Topology with Complete Balancing Capability

As discussed above, the topologies with incomplete capacitor-voltage-balancing capability generally require extra efforts to achieve capacitor-balancing. However, the topologies with the complete capacitor-voltage-balancing capability can simply utilize the redundant switching state to achieve capacitor-balancing. Hence, such kind of topologies is always preferred in industry application.

However, a practical multilevel topology requires not only good balancing capability but also low device count to achieve excellent performance and low cost simultaneously. It is always challenging to find out a competitive new topology, particularly the high-level-number (>5 levels) topologies.

5.2 The Proposed Topology for High-Power VFD

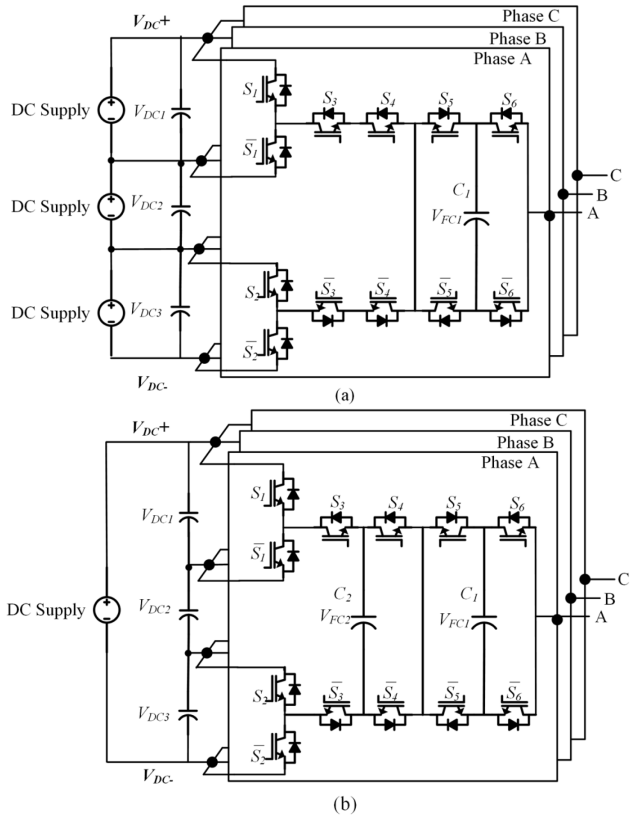


Figure 5.4 7L-HC topology: (a) simplified topology; (b) complete topology

The proposed 7L hybrid clamped (7L-HC) converter is shown in Figure 5.4. Compared with the other 7L topologies [128]-[132], it has fewer switches and

floating capacitors while it can operate in the wide frequency range. It has two variations—the simplified topology shown in Figure 5.4(a) and the complete topology shown in Figure 5.4(b). Like the other topologies with unclamped DC-link capacitors or floating capacitors, active balancing methods are needed[133].

5.3 Configurations of 7L-HC VFDs and the Requirements on Voltage Balancing

As the 7L-HC has three unclamped DC capacitors, different DFE configurations can be used in 7L-HC VFDs, resulting in different requirements on voltage balancing. Alternatively, when regeneration and high grid-side quality is required, AFEs built with 7L-HC topology can be used. In this section, different 7L-HC drive configurations are studied and compared.

5.3.1 DFE with the Simplified Topology

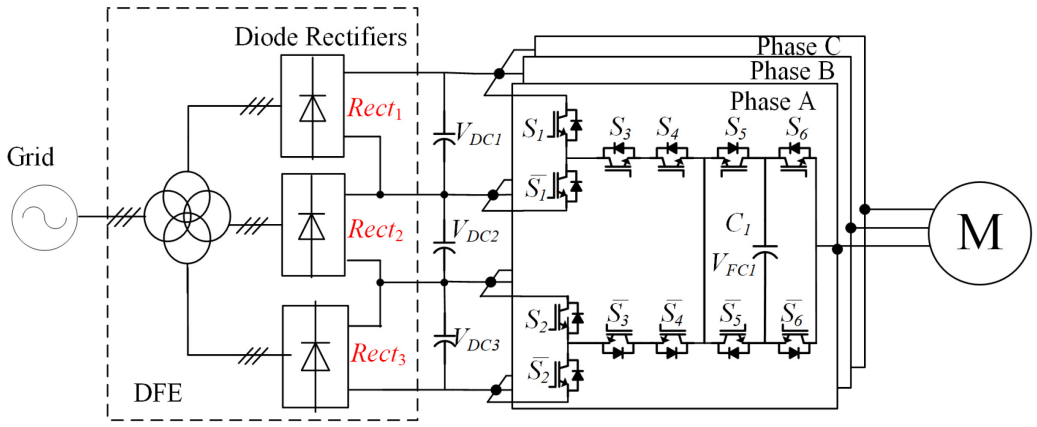


Figure 5.5 Motor drive constructed with DFE and simplified 7L-HC converter

As shown in Figure 5.5, the 7L-HC converter can be fed by three rectifiers with isolated transformer windings. The voltages of the three DC-link capacitors are clamped by the rectifiers. As discussed in [133], when the DC-link capacitors do not need balancing, only one floating capacitor C_1 is required and should be balanced in each phase. This simplifies the topology and operation.

TABLE 5.1 Applicable Switching States of the Simplified Topology

Level	Output Voltage	State No.	States (S_1-S_6)	Impact on C_1	
				$I_O>0$	$I_O<0$
1	$-V_{dc}/2$	1A	000000	–	–
2	$-V_{dc}/3$	2C	110010	C	D
		2D	000001	D	C
3	$-V_{dc}/6$	3A	110000	–	–
4	0	4C	001110	C	D
		4D	110001	D	C
5	$V_{dc}/6$	5A	001111	–	–
6	$V_{dc}/3$	6C	111110	C	D
		6D	001101	D	C
7	$V_{dc}/2$	7A	111111	–	–

Note: 'C' means charge; 'D' means discharge

As shown in TABLE 5.1, 10 applicable switching states can be used. As the ON/OFF state of S_1-S_6 are always complementary to $\overline{S}_1$- $\overline{S}_6$, the switching states can be simply presented by the state of S_1-S_6. Hence, 6-bit binaries are used to describe the switching states.

The impacts of the switching states on the only floating capacitor C_1 are also shown in TABLE 5.1, based on which the following balancing scheme can be used:

$$State = \begin{cases} nD, I_O \times (V_{C1} - V_{dc}/6) \geq 0 \\ nC, I_O \times (V_{C1} - V_{dc}/6) < 0 \end{cases} \qquad (5.1)$$
$$n = N_{Level}\ (N_{Level} = 2,\ 4,\ or\ 6)$$

Among the seven voltage levels, only the even number levels contain the redundant switching states to balance the floating capacitor C_1 under any current direction. As there are always two consecutive output levels to be produced in each switching period, the required switching state to balance C_1 can always be achieved within one switching period.

The simplified topology is attractive due to the simple structure and ease of capacitor-balancing. However, the power quality of DFE can be a concern. Generally, to meet the grid code, such as IEEE 519 [32], multi-pulse front ends are widely used as the superposition of power frequency currents with proper phase

shift can effectively mitigate the low order harmonics. However, due to the three rectifiers in DFE consume different power when the simplified topology is used, the cancellation of low order harmonics is not ideal, leading to lower power quality.

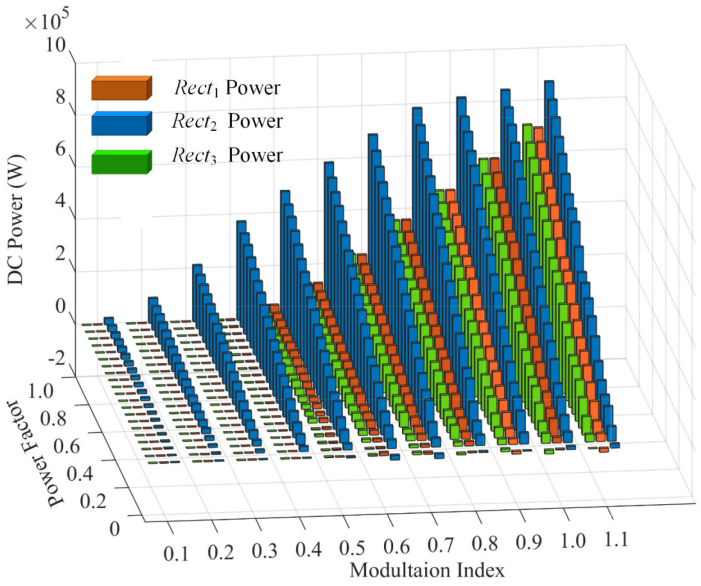


Figure 5.6 Power distribution of rectifiers when the simplified topology is used

Figure 5.6 shows the power consumption of three rectifiers when the simplified 7L-HC converter is operated under different modulation index and power factor. The uneven power distribution can be significant under high power factor or low modulation index. Considering the motor drives usually need to operate in a wide modulation index, it is challenging to ensure grid-side power quality.

Under uneven power distribution, the 18-pulse DFE suffers low power quality. As shown in Figure 5.7 (a), the current amplitude of $Rect_2$ is larger than $Rect_1$ and $Rect_3$. The superposed current is thus distorted. As shown in Figure 5.7(c), the 18-pulse transformer current contains a large number of 5^{th} and 7^{th} order harmonics. The THD reaches 7.91%, which is not acceptable in most applications.

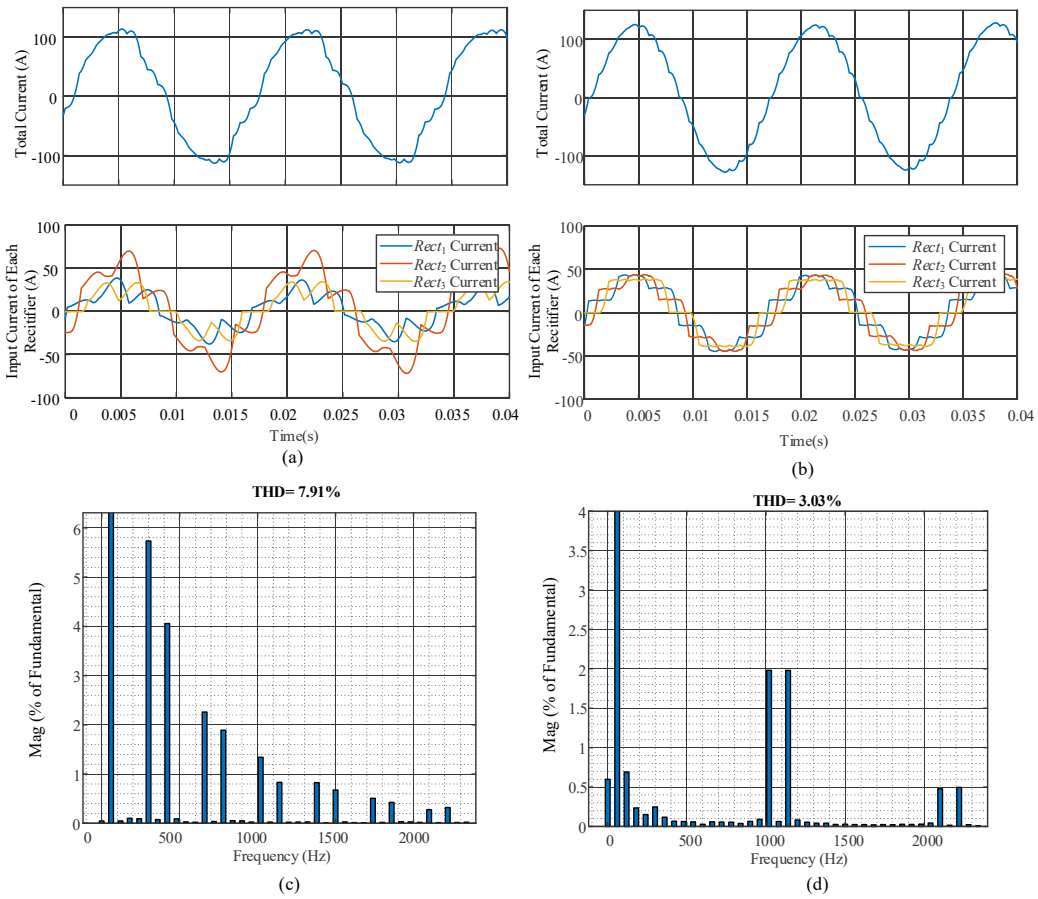


Figure 5.7 Grid side current and FFT analysis when 18-pulse DFE is used: (a) input current with clamped DC-link capacitors and simplified topology; (b) input current with unclamped DC-link capacitors and complete topology; (c) FFT analysis of total current in (a); (d) FFT analysis of total current in (b)

Therefore, the simplified 7L-HC converters are limited to the applications where the power quality can be maintained with some other measures, e.g., installing extra tuned filters or active power filters (APF).

5.3.2 DFE with the Complete Topology

The complete topology structure can avoid the uneven power consumption among the rectifiers in DFE. As shown in Figure 5.8, the rectifiers are connected in series to supply the motor-side converter. The input current of an 18-pulse DFE is shown in Figure 5.7(b) and the FFT analysis in Figure 5.7(d). When the complete topology is used, the currents of the three rectifiers are of the same amplitude,

leading to high-quality currents in the primary side of the transformer. The dominant harmonics are 17th and 19th order harmonics, which are expected in 18-pulse DFE.

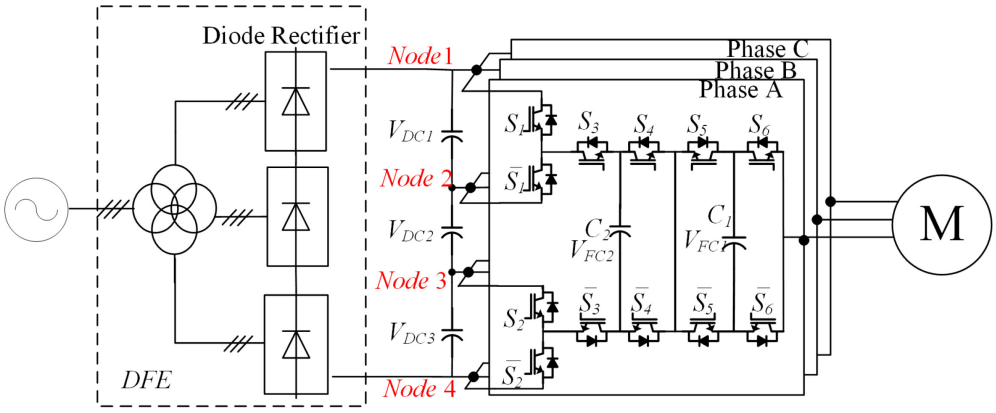


Figure 5.8 Motor drive constructed with DFE and complete 7L-HC converter

The front end with more phase-shift windings and better power quality, such as 24-pulse DFE, 36-pulse DFE, can also be applied without considering the number of DC capacitors in the DC-link. The power consumption of rectifiers is equal, achieving the desired input current of a multi-pulse front end.

However, in those cases, *Node* 2 and *Node* 3 are no longer clamped, requiring the 7L-HC converter to balance the voltage on the unclamped DC-link capacitors. The floating capacitor C_2 has to be installed in each phase to enable the DC-link capacitor-balancing capability, constructing the complete structure, as shown in Figure 5.8. In the complete structure, the number of available redundant switching states is increased to 22, which is shown in TABLE 5.2.

In this complete topology, the installation of C_2 brings more redundant switching states and the new requirement to balance C_2. As a result, the three shared unclamped DC-link capacitors and two floating capacitors C_1 and C_2 in each phase all need to be balanced in a wide frequency range. The corresponding balancing method will be proposed and analyzed in Section III and Section IV.

TABLE 5.2 Applicable Switching States of the Complete Topology

Level	Output Voltage	State No.	States (S_1-S_6)	Impact on C_1		Impact on C_2		Impact on V_{DC1}-V_{DC2}		Impact on V_{DC2}-V_{DC3}	
				I_O>0	I_O<0	I_O>0	I_O<0	I_O>0	I_O<0	I_O>0	I_O<0
1	-V_{dc}/2	1A	000000	–	–	–	–	–	–	–	–
2	-V_{dc}/3	2A	001010	C	D	C	D	↓	↑	–	–
		2B	000110	C	D	D	C	–	–	–	–
		2C	110010	C	D	–	–	–	–	↓	↑
		2D	000001	D	C	–	–	–	–	–	–
3	-V_{dc}/6	3A	110000	–	–	–	–	–	–	↓	↑
		3B	001000	–	–	C	D	↓	↑	–	–
		3C	000111	–	–	D	C	–	–	–	–
4	0	4A	111010	C	D	C	D	–	–	–	–
		4B	110110	C	D	D	C	–	–	↓	↑
		4C	001110	C	D	–	–	↓	↑	–	–
		4D	110001	D	C	–	–	–	–	↓	↑
		4E	000101	D	C	D	C	–	–	–	–
		4F	001001	D	C	C	D	↓	↑	–	–
5	V_{dc}/6	5A	001111	–	–	–	–	↓	↑	–	–
		5B	110111	–	–	D	C	–	–	↓	↑
		5C	111000	–	–	C	D	–	–	–	–
6	V_{dc}/3	6A	111001	D	C	C	D	–	–	–	–
		6B	110101	D	C	D	C	–	–	↓	↑
		6C	111110	C	D	–	–	–	–	–	–
		6D	001101	D	C	–	–	↓	↑	–	–
7	V_{dc}/2	7A	111111	–	–	–	–	–	–	–	–

Note: 'C' means charge; 'D' means discharge;'↑'means increase; '↓'means decrease

5.3.3 AFE with the Complete Topology

The power regeneration feature and high-power quality can be achieved when an AFE is used. As shown in Figure 5.9, two 7L-HC converters can be connected in back-to-back to consume power from the grid and drive the motor. With the help of common-mode chokes, isolated transformed can be removed to build a transformer-less motor drive, obtaining advantages such as low weight, low volume, and so on.

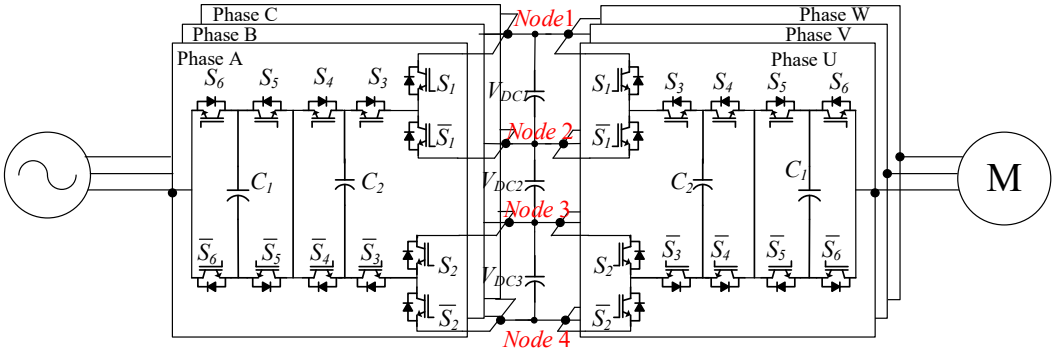


Figure 5.9 Motor drive constructed with the back-to-back 7L-HC converter

Similar to the complete topology with DFE, *Node* 2 and *Node* 3 are not clamped, requiring DC-link capacitor-balancing. The motor-side converter needs to balance the capacitors in a wide frequency range while the AFE only needs to balance its capacitors at power frequency, i.e., 50/60Hz. In this case, C_2 is needed in each phase to obtain switching states in TABLE 5.2. The balancing method is also similar to the case where DFE and complete topology are used, which will be illustrated in Section. III and Section. IV.

5.3.4 Comparisons and Recommendations

As discussed in the above subsections, when DFEs are used, the simplified topology has uneven power absorbed from the front end, leading to high-amplitude low order components, such as 5^{th} and 7^{th} order harmonics. On the other hand, when the complete topology is used, the multi-pulse transformer has even power consumption among its windings, and the low order harmonics can be canceled in the primary winding. Therefore, the complete topology is recommended when DFE is used.

When the AFE is used, the unclamped DC-link capacitor voltage must be controlled by the rectifier and inverter. In this case, the complete topology is needed.

When the complete topology is used, it is necessary to balance all the capacitors in the wide frequency range. Therefore, the corresponding balancing scheme should be developed.

5.4 Analysis of Balancing Paths Provided by the Redundant States

As shown in TABLE 5.2, the output levels have different numbers of redundant switching states with different impacts on the floating capacitor and DC-link capacitors. Based on the impacts, the output levels can be classified as: 1) levels without impacts to all the capacitors; 2) levels with impacts to all the capacitors; 3) levels without impacts to C_1.

5.4.1 Levels without Impacts to All the Capacitors

When the 7L-HC converter produces the highest and lowest level, which is *Level* 1 and *Level* 7, the voltages on DC-link capacitors and floating capacitors are not impacted. Taking *Level* 7 as an example, shown in Figure 5.10, the current flows from the positive pole of DC-link to the load. As a result, the voltages of any DC-link capacitors or floating capacitors will not be changed. There are no states to balance the capacitors, but the voltage errors will not be increased as well.

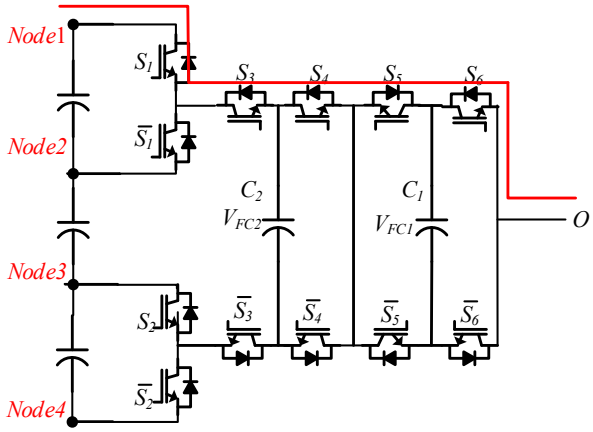


Figure 5.10 Current flow path provided by State 7A

5.4.2 Levels with Impacts to All Capacitors

Among the seven levels, all three even number levels, i.e., *Level* 2/4/6, have redundant states to change the voltage on both the DC-link capacitors and the floating capacitors. This fact ensures that the balancing states are available in any switching period as two consecutive levels are always produced in each switching period.

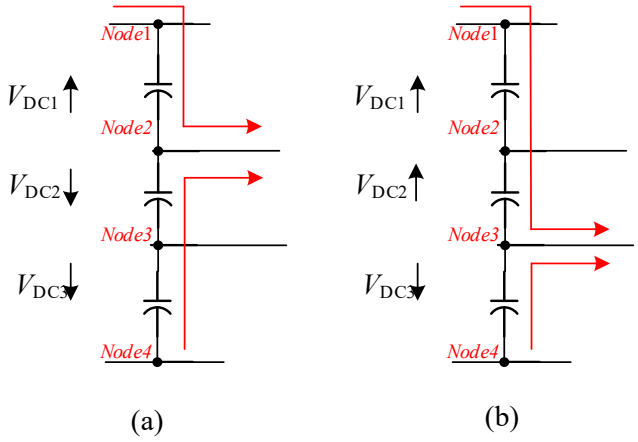


Figure 5.11 The current flow and the impacts to unclamped DC-link capacitors: (a) when the positive current flow through Node 2; (b) when the positive current flow through Node 3

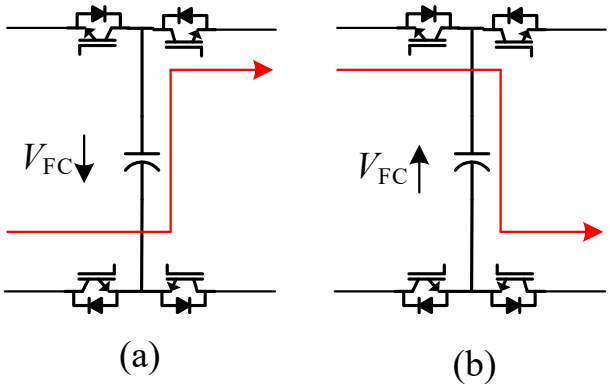


Figure 5.12 The current flow and the impacts to floating capacitors: (a) charging path when the current is positive; (b) discharging path when the current is positive

Examples of the impacts on the DC-link capacitor voltages under different current flow paths are shown in Figure 5.11. When the positive current flow through the *Node* 2, V_{DC2} and V_{DC3} will be decreased simultaneously, while V_{DC1} will increase. The impacts will be inverted if the current direction changes. Similarly, when currents flow through *Node* 3, V_{DC3} will be changed in the opposite direction of the V_{DC1} and V_{DC2}. It is easy to find that taking the (V_{DC1}-V_{DC2}), and (V_{DC2}-V_{DC3}) as the control variable is easy to carry out. Therefore, the balancing of the DC-link capacitors should be performed as equalizing their voltages.

Figure 5.12 shows examples of charging paths and discharging paths for floating capacitors. If the current flows out of the capacitor, the capacitor will be discharged. On the contrary, it will be charged if the current flows into the capacitor.

The charging and discharging effects are directly determined by the current path provided by switching states and the current directions.

However, one switching state can have impacts on several capacitors. As a result, balancing one of the capacitors can increase the voltage error of another. Taking *Level* 4 (output voltage is 0) as an example, all the 6 redundant states have impacts on more than one capacitor, as shown in Figure 5.13. When the current is positive, *State* 4A can charge both C_1 and C_2. However, if one of them needs discharging, *State* 4A can increase the voltage error. Therefore, the balancing scheme should be carefully designed to ensure the balancing of all the capacitors.

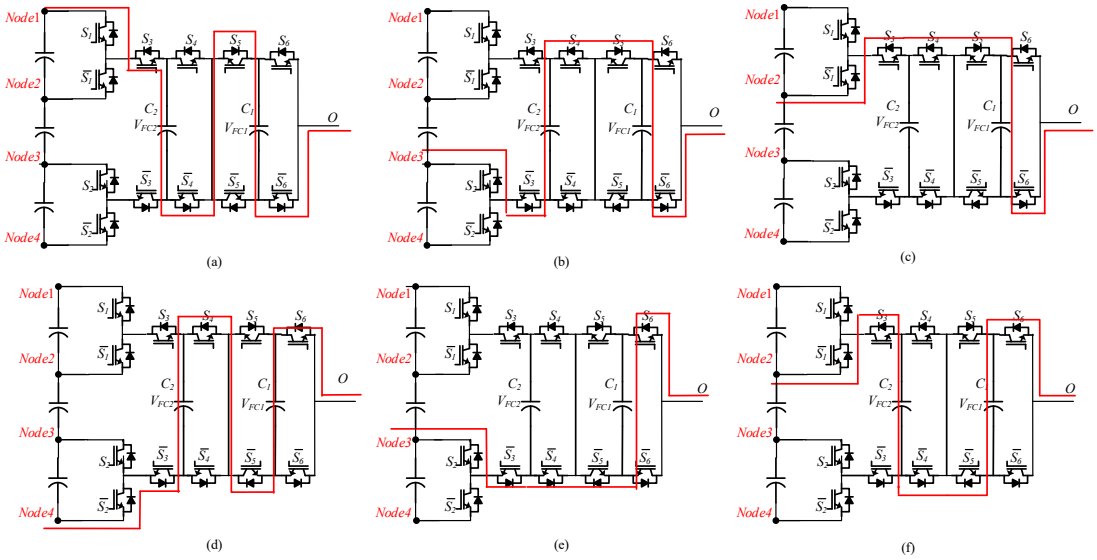


Figure 5.13 Current flow path provided by states of Level 4: (a) path of State 4A; (b) path of State 4B; (c) path of State 4C; (d) path of State 4D; (e) path of State 4E; (f) path of State 4F

5.4.3 Levels without Impacts to C_1

For *Level* 3 and *Level* 5, there are no redundant states to change the voltage of the floating capacitor C_1. Instead, the balancing of C_2 and DC-link capacitors can be performed.

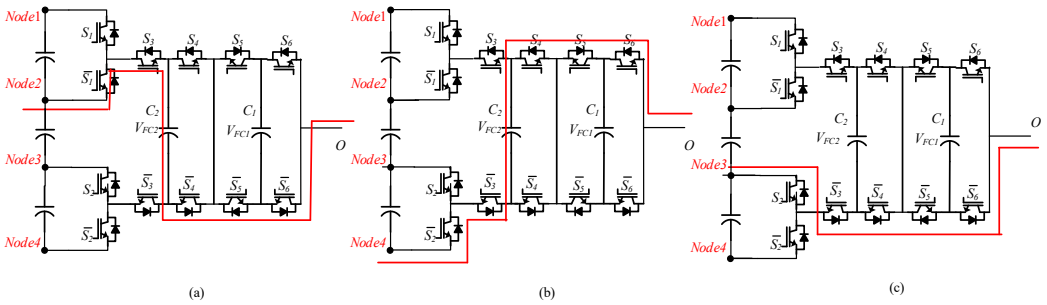


Figure 5.14 Current flow path provided by states of Level 3: (a) path of State 3A; (b) path of State 3B; (c) path of State 3C

Taking *Level* 3 as an example, the *State* 3A can impact the voltage of *Node* 3; *State* 3B can change the voltage of C_2 and *Node* 2; while only C_2 can be influenced by *State* 3C. The corresponding current flow path is shown in Figure 5.14. Similar to even number levels, *Level* 3 and *Level* 5 should also consider the impacts to multiple capacitors brought by one switching state.

When the two levels are generated, the voltage on C_1 will be constant. The voltage errors can only be corrected when some other voltage levels are generated. As discussed, two consecutive voltage levels are generated in one switching period, making it possible to reduce the voltage errors of C_1. For example, when *Level* 3 is generated, the adjacent voltage levels, both *Level* 2 and *Level* 4, have the state to balance C_1.

5.5 PWM and the Proposed Capacitor Voltage Balancing Method

As discussed above, the switching states to balance capacitors are available in every switching period while most of the switching states have impacts on more than one capacitor. As shown in TABLE 5.2, among the 22 applicable switching states, 18 of them have impacts on more than 2 capacitors. Therefore, it is necessary to determine which capacitor to balance first. To do this, as shown in Figure 5.15, the capacitor errors are sorted, based on which the priority will be given. The priorities and balancing requirements drive the switching state selection. Meanwhile, the modulation module provides the level to be produced. In practice, the priority and balancing requirements, which are based on sampling results and

calculations, are obtained in DSP. While the modulation module and the state selection, which are mainly sequential logic operation, can be easily realized by the FPGA. The details will be illustrated in the following subsections.

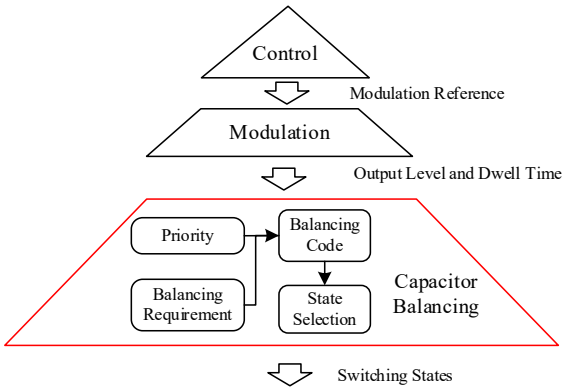


Figure 5.15 Structure of the control system for 7L-HC and the proposed balancing method

5.5.1 Modulation Method to Obtain Output Level and Dwell Time

Both carrier-based PWM method and Space-vector modulation can be used to operate 7L-HC converters. However, due to the requirement of the voltage balancing, the generated output cannot be directly used to determine the specific ON/OFF state of each switch. Instead, redundant states must be selected according to the operating conditions, i.e., current direction and capacitor voltages. Therefore, the modulation module only needs to provide the expected output level and the corresponding dwell time.

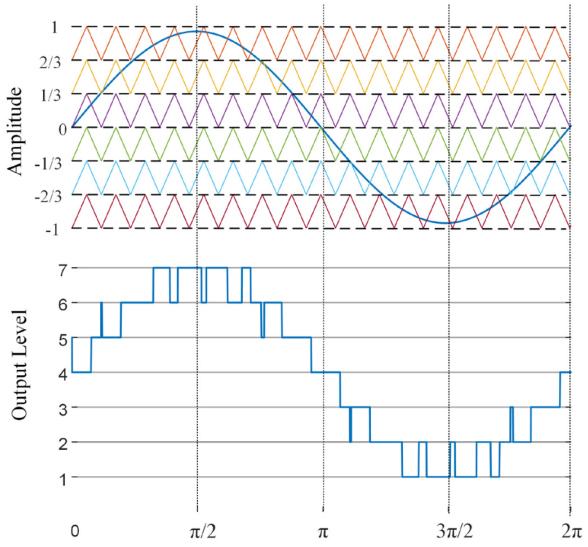


Figure 5.16 Level shift Modulation for 7L-HC

Figure 5.16 shows an example of LSPWM. The modulation reference is compared with 6 level-shifted carriers. The generated output level and dwell time will be provided to the downstream modules to determine the proper switching states.

5.5.2 Priority Determination

In the proposed strategy, different priorities are given to the capacitors so that the capacitors with the more significant voltage errors can be balanced first. In most cases, the selected switching state can fulfill the requirements of two capacitors. The priority should be evaluated by balancing errors, which can be obtained through (5.2):

$$\begin{cases} V_{d1} = (V_{DC1} - V_{DC2}) / \dfrac{V_{DC}}{3} \\ V_{d2} = (V_{DC2} - V_{DC3}) / \dfrac{V_{DC}}{3} \\ V_{dFC1} = (V_{FC1} - \dfrac{V_{dc}}{6}) / \dfrac{V_{dc}}{6} \\ V_{dFC2} = (V_{FC2} - \dfrac{V_{dc}}{3}) / \dfrac{V_{dc}}{3} \end{cases} \tag{5.2}$$

where V_{DC} is the total DC-link voltage, V_{FC1} and V_{FC2} are the voltages on floating capacitor C_1 and C_2, respectively. Please note that V_{d1}, V_{d2}, V_{dFC1}, and V_{dFC2} are the errors normalized with their rated values.

The capacitor voltage with the most significant and second significant balancing error will be considered in the state selection procedure. Therefore, it is unnecessary to sort all the errors. To do this, one example is shown in the flowchart in Figure 5.17. The C_1 and C_2 are assumed to be with the largest and second-largest errors, which are E_{max1} and E_{max2}. Then the errors of V_{d1} and V_{d2} are compared with the assumed two largest errors, respectively. During the comparisons, larger errors will be assigned to be E_{max1} or E_{max2}. The updated E_{max1} or E_{max2} should participate in the following comparisons. With only 4 times of comparison, the proper priorities can be found for one phase leg.

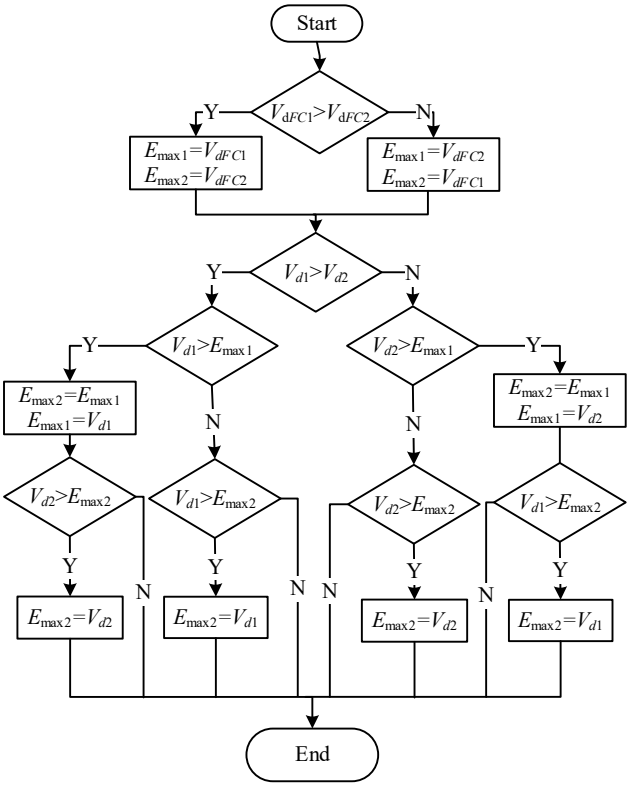


Figure 5.17 The flowchart to find the capacitors with the largest and the second-largest error

5.5.3 Balancing Requirement

To acquire the balancing requirements, the control system should sense the voltages on each capacitor and the output current direction. As there are two floating capacitors and 3 shared unclamped DC-link capacitors to balance in each phase, it is necessary to concisely represent the balancing requirement to make it easier to select the switching state. In this chapter, the balancing code is used to concisely and accurately express the balancing requirements.

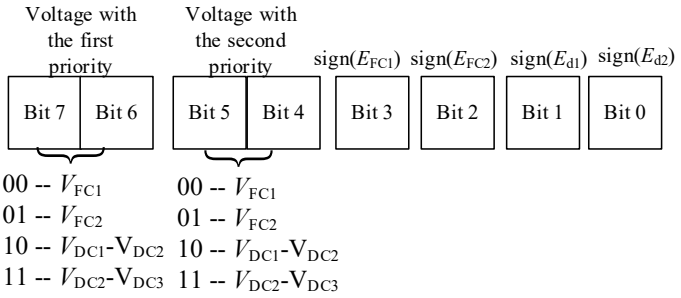


Figure 5.18 The definition of balancing code

As shown in Figure 5.18, the balancing code is an 8-bits binary number. Its highest two bits indicate the voltage with the first priority. The following two bits

show the voltage with the second priority. With the 2-bit space, the four voltages to be balanced, i.e., V_{FC1}, V_{FC2}, (V_{DC1}-V_{DC2}), and (V_{DC2}-V_{DC3}), can be indicated as 00, 01, 10, and 11 respectively. As all the switch states cannot change both (V_{DC1}-V_{DC2}), and (V_{DC2}-V_{DC3}), the combination 1011 or 1110 will never be used. In other words, at least one of the two capacitors with priorities is a floating capacitor.

With the priorities given, the lowest 4 bits can be used to indicate the balancing requirements of each voltage. Instead of the values of voltage errors, the balancing scheme only needs the polarities of the error to select switching states with the expected impacts. Due to the impacts always inverse when the current directions change, the current direction is also considered. The balancing requirement of each capacitor can be calculated by (5.3):

$$\begin{cases} E_{FC1} = (V_{C1} - \dfrac{V_{DC}}{6}) \cdot I_O \\ E_{FC2} = (V_{C2} - \dfrac{V_{DC}}{3}) \cdot I_O \\ E_{d1} = (V_{DC1} - V_{DC2}) \cdot I_O \\ E_{d2} = (V_{DC2} - V_{DC3}) \cdot I_O \end{cases} \tag{5.3}$$

Then the lowest four bits can be obtained by checking the sign of E_{FC1}, E_{FC2}, $E_{d1,}$ and E_{d2}. To indicate the sign, the function $sign(x)$ is defined as:

$$sign(x) = \begin{cases} 1, x \geq 0 \\ 0, x < 0 \end{cases}, x = [E_{FC1}, E_{FC2}, E_{d1}, E_{d2}] \tag{5.4}$$

The low 4 bits of balancing code $C_{Bal}(3{:}0)$ can be obtained as:

$$\begin{aligned} &C_{Bal}(3:0) = (sign(E_{FC1}) << 3) \,|\, (sign(E_{FC2}) << 2) \\ &|\, (sign(E_{d1}) << 1) \,|\, sign(E_{d2}) \end{aligned} \tag{5.5}$$

5.5.4 State Selection

TABLE 5.3 shows the switching states and the corresponding balancing code. The ‘x’ in the balancing code indicates the corresponding bit can are ignored. The ‘x’ can be 1 or 0 and does not count in the state selection. Once the balancing code is known, the state can be selected according to the expected output level. In TABLE 5.3,

TABLE 5.3 State Selection Based on Output Level and Balancing Codes

Output Level	State No.	Switching States	Corresponding Balancing Codes
1	1A	000000	xxxxxxxx
2	2A	001010	000100xx, 10xxx0xx, 10xxxx0x
	2B	000110	000101xx, 00100x1x, 00110xx1, 01xxx1xx
	2C	110010	00110xx0, 11xxxxx0
	2D	000001	00xx1xxx, 10xxxx1x, 11xxxxx1
3	3A	110000	11xxxxx0
	3B	001000	00xxx0xx, 01xxx0xx, 10xxxx0x
	3C	000111	00xxx1xx, 01xxx1xx, 10xxxx1x, 11xxxxx1
4	4A	111010	000100xx, 00100x1x, 00110xx1, 010000xx, 0110x01x, 0111x0xx, 10000x1x, 1001x01x, 11000xx1, 1101x0x1
	4B	110110	000101xx, 00110xx0, 010001xx, 0111x1x0, 11000xx0, 1101x1x0
	4C	001110	00100x0x, 10000x0x, 1001x10x
	4D	110001	00111xx0, 11001xx0, 1101x0x0
	4E	000101	000111xx, 00101x1x, 00111xx1, 010011xx, 0111x1x1, 0110x1xx, 10001x1x, 1001x11x, 11001xx1, 1101x1x1
	4F	001001	000110xx, 00101x0x, 010010xx, 0110x00x, 10001x0x, 1001x00x
5	5A	001111	10xxxx0x
	5B	110111	00xxx1xx, 01xxx1xx, 11xxxxx0
	5C	111000	00xxx0xx, 01xxx0xx, 11xxxxx0
6	6A	111001	000110xx, 00101x1x, 00111xx1, 01xxx0xx, 10xxxx1x, 11xxxxx1
	6B	110101	00111xx0, 01xxx1xx, 11xxxxx0
	6C	111110	00xx0xxx, 000111xx
	6D	001101	00101x0x, 10xxxx0x
7	7A	111111	xxxxxxxx

To clearly illustrate the scheme to select the switching state according to TABLE 5.3, an example is given as follows: when the output level should be *Level* 4, there are six applicable switching states-- 4A~ 4E. Then the state selection scheme will refer to the balancing code. When the floating capacitors C_1 and C_2

have the first and second priority, and C_1 needs to be discharged while C_2 needs to be charged, a balancing code '00011011' will be given. This balancing code matches one of the corresponding balancing codes of State 4F--'000110xx', then the state 4F will be selected and applied. The load will see *Level* 4; meanwhile, the voltage errors of the capacitors C_1 and C_2 will be decreased. The procedure is easy to perform in a digital control system. Also, it is worth to note that the state selection is only performed when the output level changes to avoid extra switching actions.

5.6 Detailed Implementation with Control Schemes

The proposed balancing scheme can be easily implanted with the control schemes as the balancing scheme does not modify the modulation reference generated by the controllers. Instead, the balancing scheme is achieved by selecting the redundant switching states. The control system and PWM scheme can thus be flexibly selected.

The detailed control block is shown in Figure 5.19. The same balancing scheme can be applied in both AFE or motor-side converter built with complete 7L-HC topology. In Figure 5.19, V_{FC1_a} and V_{FC2_a} denote the floating capacitor voltage V_{FC1} and V_{FC2} of phase A. The DC-link voltage V_{DC} can be obtained by adding up V_{DC1}, V_{DC2}, and V_{DC3}.

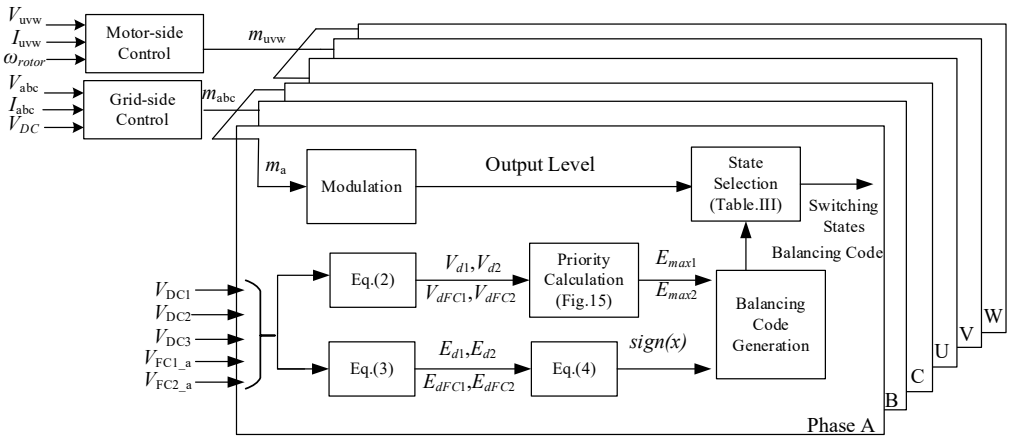


Figure 5.19 Detailed implementation of the balancing scheme

5.7 Simulation and Experimental Verifications

5.7.1 Simulation Verification

To verify the balancing method in a medium voltage drive, a 4.16 kV drive system is built in Matlab/Simulink, which consists of a back-to-back 7L-HC converter and a medium voltage motor. The system parameters are shown in TABLE 5.4.

TABLE 5.4 Parameters of 7L-HC Converter in Simulation

Parameter	Value	p.u. Value
AC voltage	4.16 kV	1.0
Power Rating	1 MW	1.0
Switching frequency	1020 Hz	-
Capacitor C_1	800 μF	0.12
Capacitor C_2	800 μF	0.12
DC Capacitors C_{dc}	2200 μF	0.34

Figure 5.20 shows the voltage of capacitors when the proposed balancing method is applied and disabled. As shown in Figure 5.20(a), the three DC voltages are kept stable and equalized. However, when the balancing scheme is disabled at 2s, V_{DC2} starts to rise while V_{DC1} and V_{DC3} start to drop. At 3s, the balancing scheme is enabled again, and the three voltages return to their rated values. Similarly, when the balancing is disabled, all the floating capacitor voltages in three phases deviate from their nominal values in a short transient, as shown in Figure 5.20(b). The V_{FC1} changes from $V_{DC}/6$ to $2V_{DC}/3$ and V_{FC2} drops from $V_{DC}/3$ to $V_{DC}/6$. However, once the 7L-HC converter starts to perform balancing, the floating capacitor voltages are controlled to become the expected values.

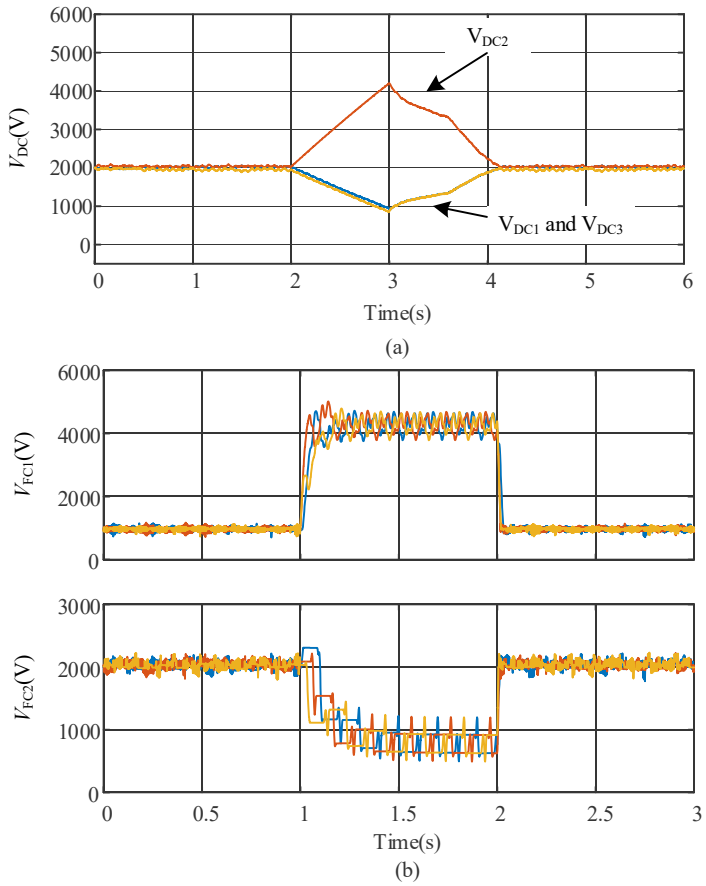


Figure 5.20 Capacitor voltage when balancing control is enabled or disabled: (a) V_{DC1}~V_{DC3}; (b) V_{FC1} and V_{FC2}

As the modulation index and power factor can impact the balancing, the voltage ripples under different modulation index and load power factor are evaluated, shown in Figure 5.21(a)-(e). The voltage ripples are normalized by the expected voltage amplitude under the corresponding modulation index, i.e., the base value is $m \cdot V_{DC}/2$. As can be seen, with the capacitance selected in TABLE 5.4, the voltage ripples can be well attenuated within 0.05 in most cases. However, large ripples can appear under the combination when the modulation index ranges between 0.3-0.5 and power factors are between 0.75-1, which is particularly true for V_{FC2}. Generally, the combination with large ripples will not be faced by motor drives as the power factor is low when the motor drive operates under a low modulation index. Also, for AFE, the modulation index is usually higher than 0.8. Operating in the large ripple area during the transient will not be a significant

challenge as the voltage errors can be corrected when the operating point moves out. Moreover, by selecting larger capacitors, the area can be further compressed.

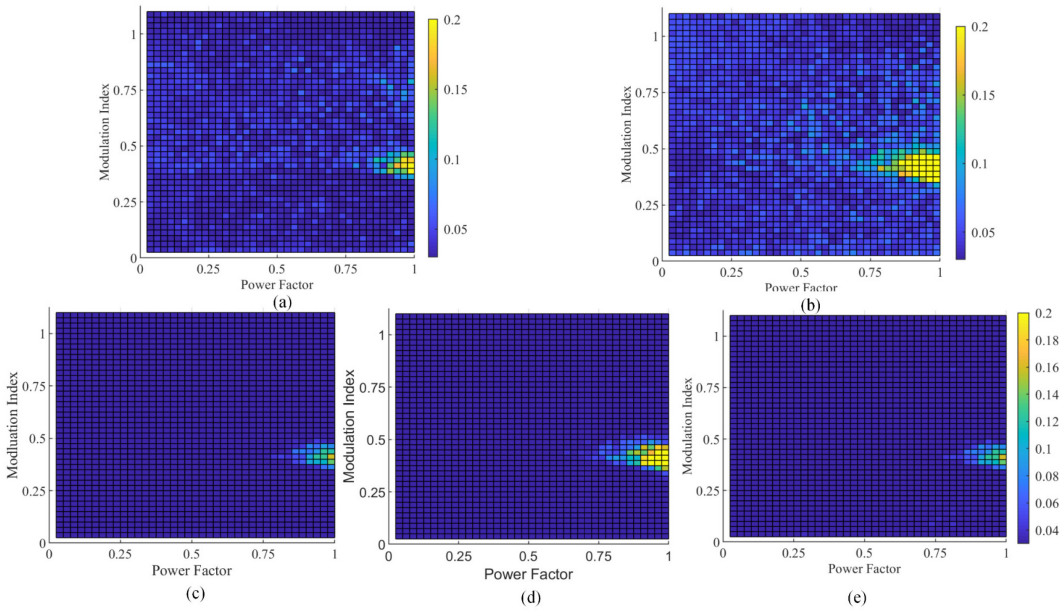


Figure 5.21 Amplitudes of capacitor voltage ripples in p.u under different modulation index and load power factor: (a) V_{FC1}; (b) V_{FC2}; (c) V_{DC1}; (d) V_{DC2}; (e) V_{DC3}

To prove the modulation and power factor combinations with large ripples will not be a significant challenge in practice, the 7L-HC converter in a medium voltage drive system is simulated. As shown in Figure 5.22, the motor drive built by 7L-HC converter drives the motor to start up. The motor speed gradually increases as the 7L-HC converter increases its modulation index and frequency. In the wide frequency range and wide modulation index range, the 7L-HC converter keeps its floating capacitor voltage stable, and the ripple amplitudes on the capacitors are remained in the acceptable range (10%). The zoomed-in view of the waveforms under steady-state is shown in Figure 5.22(b). As can be seen, with the well-balanced floating capacitor voltage and DC-link capacitor voltage, the output voltage, and current are of high quality. The typical multilevel voltage and sinusoidal current waveforms can be observed.

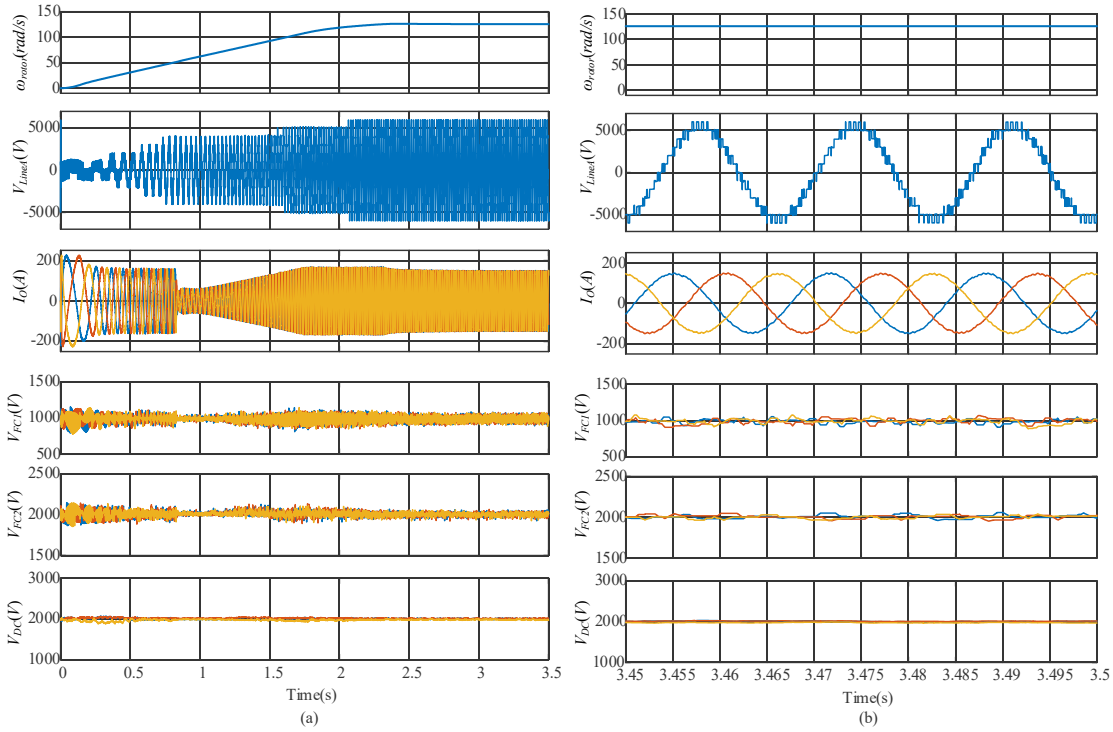


Figure 5.22 Simulation results of motor-side (from upper to lower: rotor speed, the output voltage of the converter, motor-side current, V_{FC1}, V_{FC2}, V_{DC1}~V_{DC3}): (a) full process; (b) a zoomed-in view

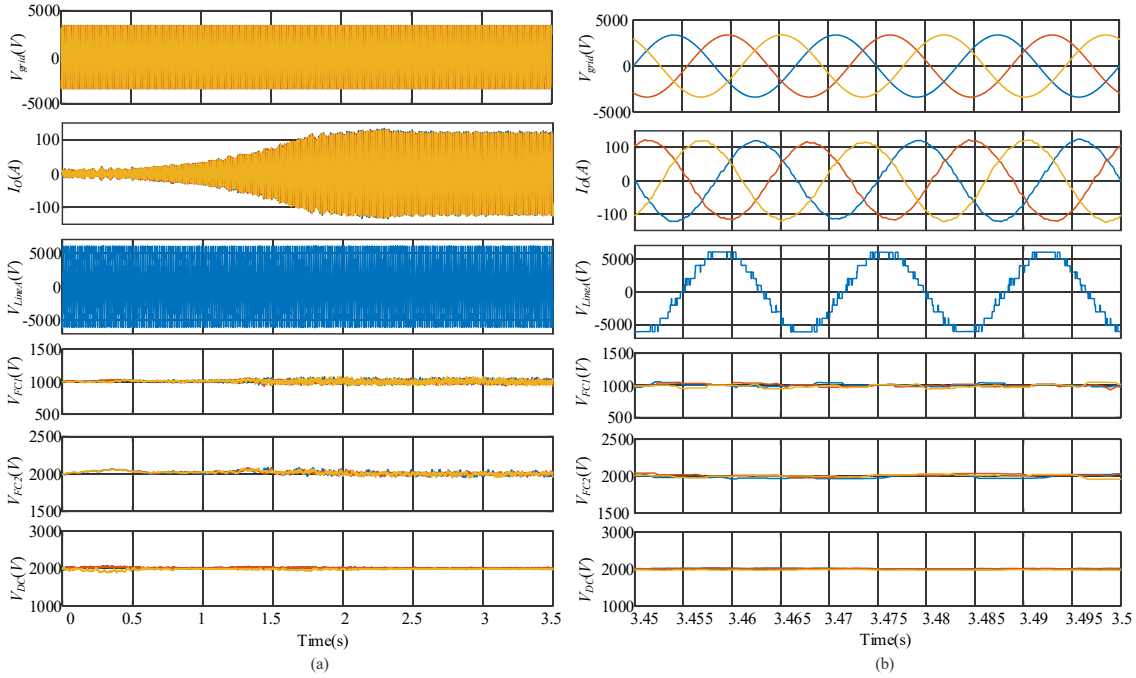


Figure 5.23 Simulation results of grid-side (from upper to lower: grid voltage, grid-side current, the output voltage of the converter, V_{FC1}, V_{FC2}, V_{DC1}~V_{DC3}): (a) full process; (b) a zoomed-in view

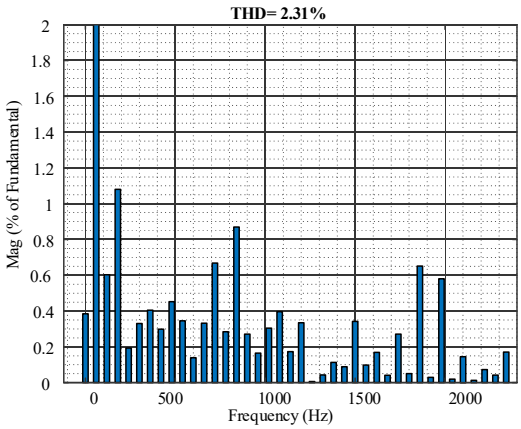


Figure 5.24 FFT results of grid-side current

Different from the motor-side converter, the grid-side converter only needs to operate at the rated frequency, i.e., 60Hz. Meanwhile, the current quality is strictly regulated by the grid codes. As can be seen from Figure 5.23, when the motor starts up, the active power absorbed by the grid-side converter increases gradually. However, as the grid voltage is constant, the modulation index of the converter does not change much, which can be observed from the multilevel line-to-line voltage of the converter. During both starts-up transient and the steady-state, the capacitor voltages are always kept stable at the expected values. This ensures high-quality voltage and current, which is shown in the zoomed-in view in Figure 5.23(b). The current waveform has a THD as low as 2.31%, as shown in Figure 5.24.

With the simulation results, it is validated that the proposed balancing scheme can effectively balance the voltage on all the capacitors when the 7L-HC converter is applied in medium voltage drive systems.

5.7.2 Experimental Verification

To further validate the balancing method, a scaled-down experimental porotype is built, which is shown in Figure 5.25. Its parameters are shown in TABLE 5.5. The low-power experimental prototype has the same p. u. value with the medium voltage system used in Simulation. The control system is constructed by DSP and FPGA.

TABLE 5.5 Parameters of 7L-HC Converter Prototype

Parameter	Value	p.u. Value
AC voltage	208 V	1.0
Power Rating	2 kW	1.0
Switching frequency	1020 Hz	-
Capacitor C_1	1000 μF	0.12
Capacitor C_2	1000 μF	0.12
DC Capacitors C_{dc}	2700 μF	0.34

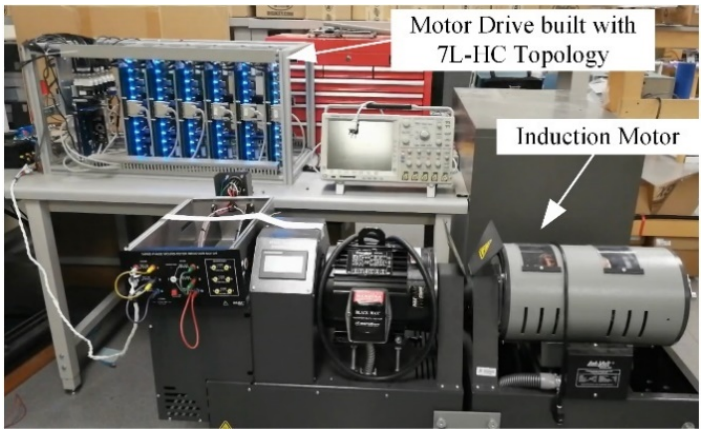


Figure 5.25 Experimental prototype: 7L-HC converter and the motor

Figure 5.26 shows the steady-state waveforms when the 7L-HC converter operates under different modulation index and frequency. Here, an RL load (L=30mH, R=14.7Ω, i.e., Power Factor=0.78 at 60Hz) is used. As shown in Figure 5.26 (a)-(c), the 7L-HC converter can produce high-quality line-to-line voltage and current waveforms at both rated frequency (60Hz) and low frequency (5Hz, 2Hz). Also, at different modulation indexes, such as 1, 0.85, 0.6, 0.5, 0.2, the waveform quality can always be ensured. In Figure 5.26(d), a step-change in frequency is applied to the 7L-HC converter, from 10Hz to 30Hz, the typical multilevel voltage waveform and sinusoidal current waveforms are still produced. The high-quality waveforms can only be obtained when the voltages of capacitors are well balanced.

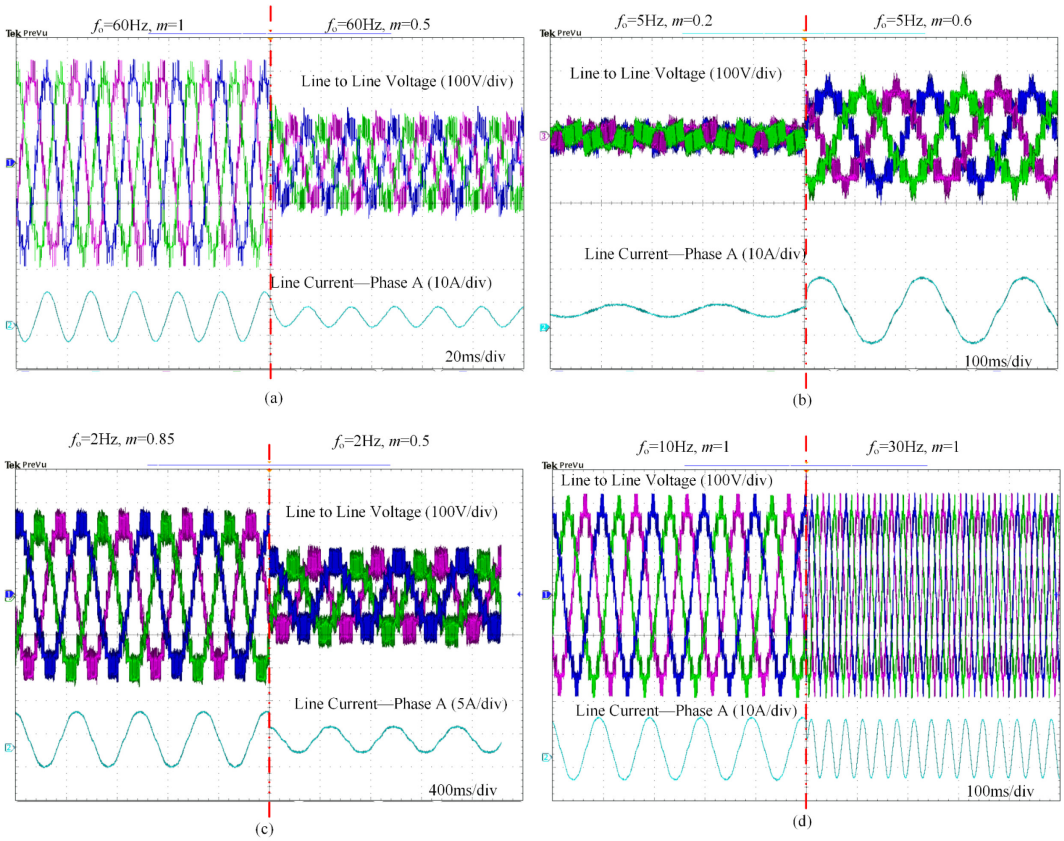


Figure 5.26 Experimental results when the 7L-HC converter operates under different output frequency f_o or modulation index m

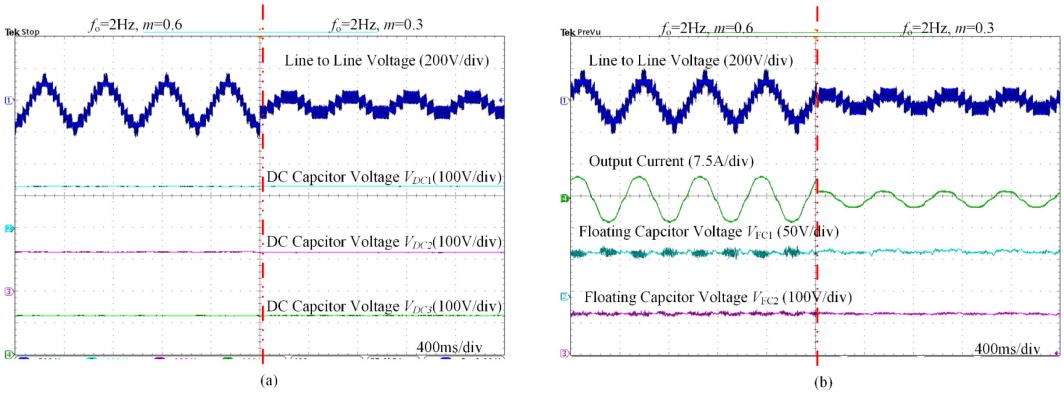


Figure 5.27 The capacitor voltages at low frequency (2Hz) with different modulation index (0.6 and 0.3): (a) voltages on three DC-link capacitors; (b) voltages on floating capacitors of phase A

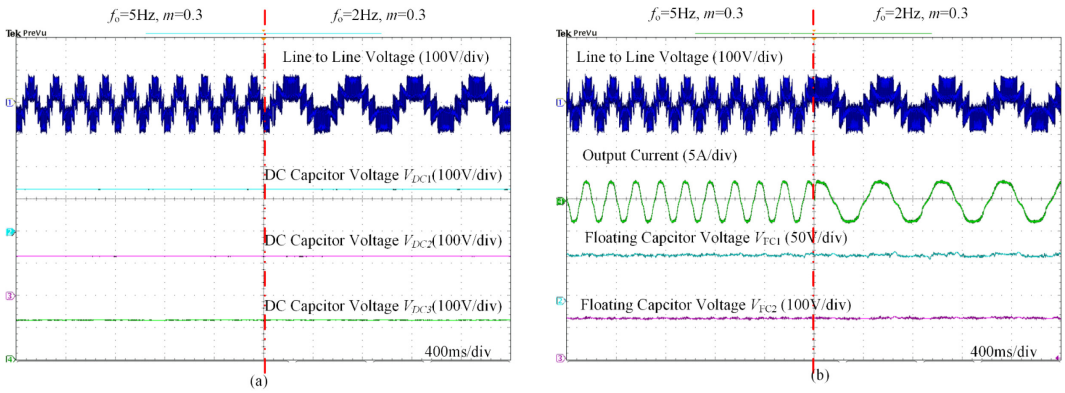


Figure 5.28 The capacitor voltages when frequency changes (5Hz, 2Hz): (a) voltages on three DC-link capacitors; (b) voltages on floating capacitors of phase A

To directly validate the voltage balancing method, the capacitor voltages are obtained under different conditions. In Figure 5.27, when the fundamental frequency is 2Hz while the modulation index changes from 0.6 to 0.3, the voltages on the capacitors, including both floating capacitors and unclamped DC-link Capacitors, are smooth and kept as the expected voltages. The voltage balancing can also be achieved when the frequency changes. The motor drives usually produce a low voltage when the frequency is low. In Figure 5.28, the modulation index is set to 0.3 when the frequency changes from 5Hz to 2Hz and the capacitors are well balanced. In Figure 5.29, the stable and smooth capacitor voltages are still well maintained when m=1, and the frequency changes from 30 Hz to 10 Hz.

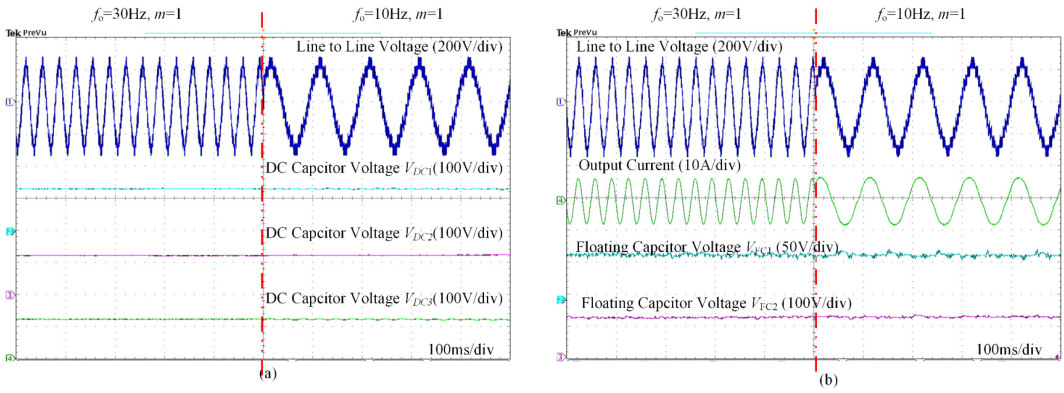


Figure 5.29 The capacitor voltages when frequency changes (30Hz, 10Hz): (a) voltages on three DC-link capacitors; (b) voltages on floating capacitors of phase A

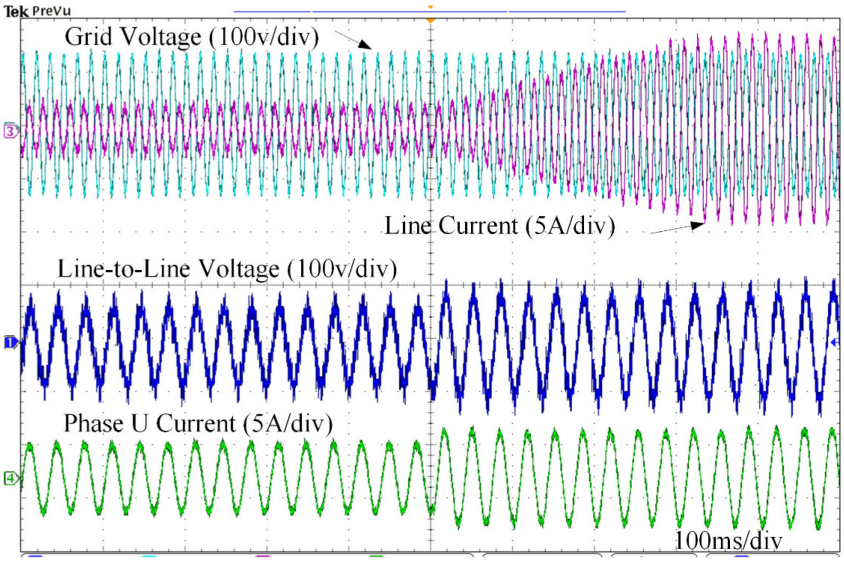


Figure 5.30 Back-to-back operation when motor-side converter operates at 30Hz and modulation index increases from 0.4 to 0.6

Figure 5.30 shows the operation of the back-to-back 7L-HC VFD. The AFE operates at 60 Hz, i.e., the frequency of the grid, while the motor-side converter operates at 30Hz. When the modulation index of motor-side converter changes from 0.4 to 0.6, both the current of the motor-side converter and grid-side current increase. The high-quality currents and voltages at both sides indicate that the capacitors are well balanced.

The waveforms of capacitor voltages are shown in Figure 5.31. As can be seen in Figure 5.31(a), the grid-side currents are controlled to be in phase with the grid voltage. When the load changes, the grid-side current increases smoothly as the DC-link voltage controller responses to the change of DC-link voltage. During the transient, both V_{FC2} and V_{DC2} are appropriately controlled. No large ripples or deviations can be observed. The steady-state waveforms in Figure 5.31(b) further validates that the grid current is properly controlled to have a unity power factor. The FFT analysis of the grid current is shown in Figure 5.32. Both the TDD (3.76%) and the amplitude of harmonics in each order can fulfill the constraints set in IEEE 519.

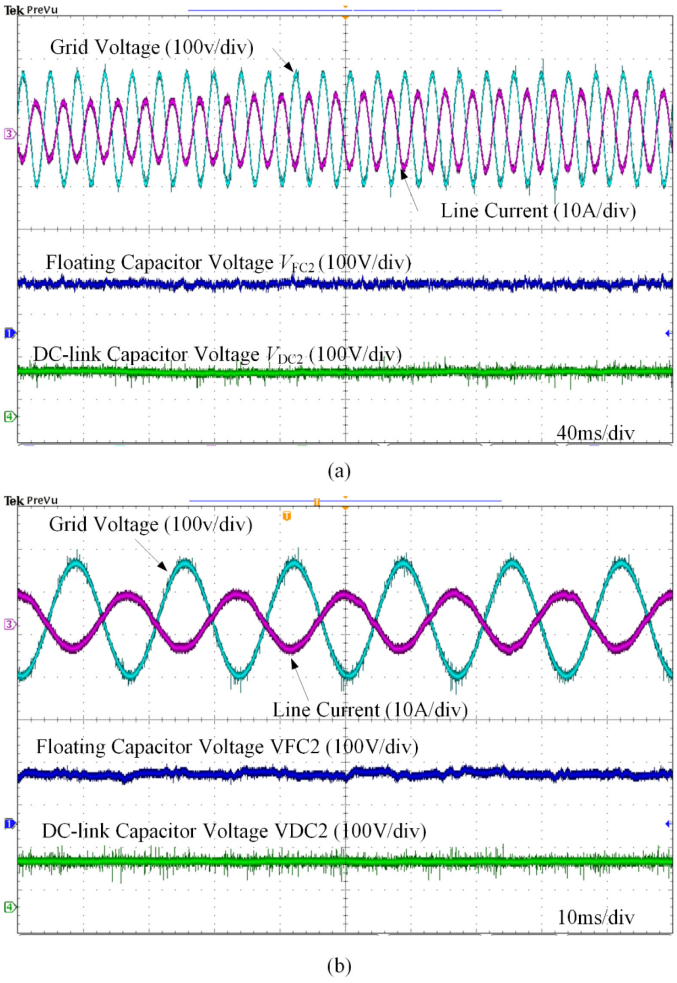


Figure 5.31 The operation of AFE: (a) transient waveforms when power increases; (b) steady-state waveforms

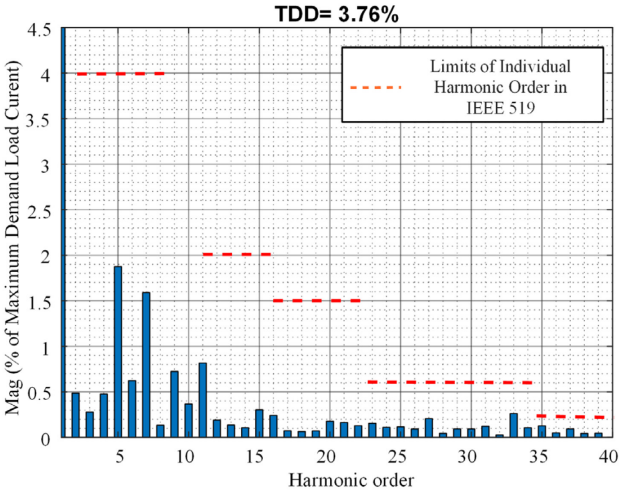


Figure 5.32 FFT analysis of the grid current obtained in the experiment

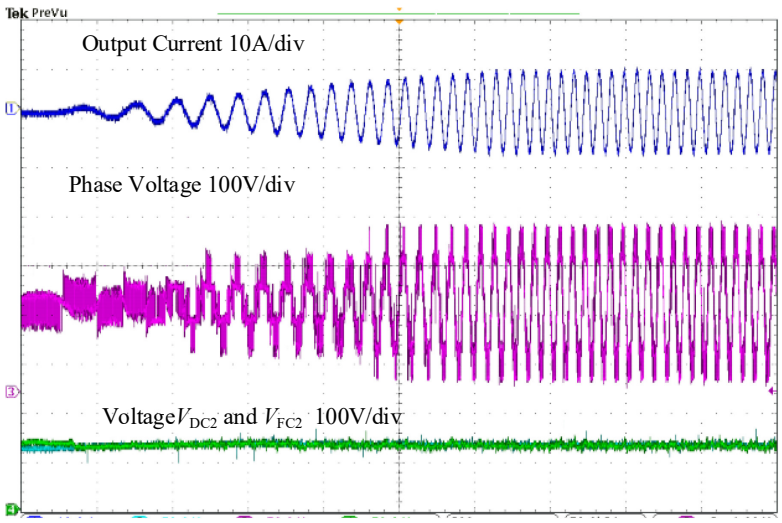


Figure 5.33 Experimental waveforms when 7L-HC converter drives a motor to start up

To further validate the performance when the 7L-HC converter is used to drive a motor under the proposed balancing method, an induction motor is used as the load. A constant voltage/frequency curve is applied to speed up the motor gradually. The power factor also changes during the start-up, which is the feature of induction motors. As shown in Figure 5.33, the 7L-HC converter increases its modulation index and output frequency to start the motor. During the process, the floating capacitor voltage V_{FC2} is kept in the expected range, and the DC voltage V_{DC2} is also well balanced when the voltage with varying frequency and amplitude is produced. V_{FC2} and V_{DC2}, which are both $V_{DC}/3$, are almost overlapped, showing they are both well balanced.

5.8 Conclusions

This chapter proposes a multilevel topology-- 7L-HC topology, and the corresponding capacitor-balancing methods. To produce high-quality current to meet the grid codes, a 7L-HC drive requires a transformer-less AFE or single DC supply built with DFE. As a result, the complete 7L-HC should be adopted as it has more switching states than the simplified topology to balance the capacitors. To coordinate the balancing, including the balancing of DC-link capacitors and floating capacitors, a complete PWM design and balancing scheme is proposed for the complete topology. The scheme gives priority to the capacitors with the most

significant errors and uses concise balancing codes to select redundant switching states. All the capacitors can thus be balanced appropriately under the various operating conditions in an MV drive. Both simulation and experimental results validate the effectiveness of the balancing scheme.

Chapter 6

Conclusions and Future Work

6.1 Thesis Conclusions and Contributions

The main objective of this thesis is to deal with the harmonic issues in VSC-based high-power LV/MV VFDs, including 2L VFDs and multilevel VFDs. Thus, both harmonic control schemes for VSC-based high-power VFDs and the capacitor ripple mitigation method for multilevel high-power VFDs are proposed to comprehensively mitigate the harmonics in VFDs. The conclusions and contributions fall into two categories:

1. Harmonic control improvement for high-power VFDs:

In order to facilitate the flexible harmonic control in VSC-based high-power VFD systems, two feed-forward virtual impedance control schemes-- voltage feed-forward method and current feed-forward method-- are proposed in Chapter 2. The control schemes can flexibly control the output impedances of VFD systems, mitigating harmonics according to the system configurations. Both harmonic rejection control and harmonic compensation control can be achieved by the control schemes. To improve control dynamics for high-power converters, the harmonic control signals are fed directly into modulation references. Also, considering that sampling schemes can impact the harmonic control performance, multi-rate sampling methods are proposed. With the proposed multi-rate sampling method, the harmonics can be sampled and controlled at high sampling rates while the fundamental-frequency control can select sampling rates flexibly. Besides VFDs, the proposed harmonic control method and sampling scheme can also be applied for all other grid-interfacing converters with low switching frequencies.

The modeling of the multi-rate harmonic control is improved in Chapter 3. The multi-rate control structure proposed in Chapter 2 can combine the advantages of synchronous sampling and high sampling rates. With this sampling scheme, VFDs

become LPTV systems. To cope with the difficulties in modeling and analysis for such an LPTV system, the lifting method and corresponding frequency response calculation are introduced. The virtual impedance control accuracy is thus improved. It is revealed that the virtual impedances at different frequencies require the multi-rate modeling and frequency response calculation method, while the stability analysis can be carried out by conventional modeling methods.

2. Capacitor ripple mitigation in multi-level high-power VFD systems:

In Chapter 4, a general capacitor-balancing method is proposed. The proposed SEPWM method can help MLCs generate extra output levels to balance their capacitors. With this method, the topologies with fundamental frequency ripples on capacitors can be significantly mitigated, enabling the converters to operate in wide frequency applications. To ensure the output is equivalent to the conventional multilevel operation, the modified modulation reference is derived. Also, design constraints are also developed to ensure low *dv/dt*.

To effectively solve the capacitor ripple problem, a topology with competitive device count and good capacitor-balancing capability is proposed. The topology can balance all floating capacitors and DC-link capacitors in a wide operation range, making it very suitable for high-power VFDs. To achieve high power quality, different configurations of the topologies-- simplified topology and complete topology-- are compared when a DFE is used, revealing that the complete topology has better power quality. The balancing scheme for the complete topology with both DFEs and AFEs is proposed. With the topology and the corresponding balancing scheme, VFDs can properly operate the motor, and avoid harmonic issues caused by capacitor ripples.

6.2 Suggestions for Future Work

The suggestions for extending this research are as follows:

1. Multi-rate harmonic control and capacitor-balancing for 7L-HC VFD

The multi-rate sampling scheme can be applied to a 7L-HC VFD system to improve the performance of harmonic control and capacitor-balancing. As the capacitor-

balancing scheme is implemented in the PWM procedures, it is feasible to use the proposed feed-forward virtual impedance control scheme to provide modulation references. In this case, the output impedance of the 7L-HC converter can be flexibly controlled to do harmonic current rejection or harmonic voltage compensation. In addition, the increased sampling rate can also improve capacitor-balancing performance as the current directions can be detected with a lower delay.

2. Direct design of the control parameters for the proposed multi-rate virtual impedance control method

The frequency response of a single-rate system is simply a shaped version of the input spectrum. However, in the multi-rate system, the output spectrum is the sum of the shaped and shifted version of the input spectrum. It is hard to directly calculate the control parameters according to the expected virtual impedances for the proposed multi-rate virtual impedance control. As a result, the design of the virtual impedances at harmonic orders is implemented by enumerating control parameters and building a look-up table in this thesis. Developing the method to design virtual impedance directly is important for reducing the design complexity.

3. Capacitor pre-charging scheme to help 7L-HC VFD start-up without ancillary pre-charging circuits

The capacitors of the 7L-HC converter need to be pre-charged to ensure the output quality during start-up and, more importantly, to ensure the voltage stress on the devices will not exceeds the allowable range. Ancillary pre-charging circuits can be used with extra costs on devices. Considering the large number of redundant switching states, it is possible to pre-charge the capacitors of 7L-HC VFD without using dedicated circuits. This approach can reduce system cost and improve reliability.

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