Control, Modulation, and Protection Strategies for Modular Multilevel Converters in Smart AC and DC Grids Applications

by

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Abstract

The technical viability of the modular multilevel converter (MMC) technology for a wide range of applications from low- to high-voltage systems has resulted in the rapid deployment of these converters in smart ac and dc grids. The features that MMCs offer, including common dc-link, modularity, voltage scalability, superior harmonic performance, and low switching losses, account for this increasing interest. However, difficulties associated with the operation and control of the MMC, such as unbalanced submodule (SM) capacitor voltages, lack of coordination or malfunction of the MMC components, and fault occurrence in the dc link and/or ac grid demand special attention.

This research work presents a new sensorless capacitor voltage balancing strategy for MMCs to effectively balance SM capacitor voltages in a wide range of switching frequencies. The proposed hierarchical permutation cyclic coding (PCC) method is developed to evenly distribute the switching gate signals among the SMs of each arm. In addition to improving reliability and computational resources, the hierarchical PCC algorithm is decoupled from other standard control loops in MMCs.

A new SM circuit is designed to facilitate fault-tolerant capability for MMCs under various internal and external faults. The proposed SM circuit can be simply integrated into conventional half bridge-based MMCs by using a switching signal adapter. A fully modular structure, enhanced internal fault management, external fault-handling capability, and ease of expandability are the key features of the designed SM circuit.

For fault-tolerant operation, a supervisory algorithm including monitoring and decision-making units is devised to detect and identify faults by analyzing the circulating currents and SM capacitor voltages. The supervisory algorithm distinguishes a fault occurring in SMs from those occurring in sensors. Fast fault identification and robust postfault restoration are the main features of the proposed fault-tolerant

framework.

The technical feasibility of the proposed strategies for MMCs in various applications is investigated. To supply a wide range of rapidly varying plug-in and wireless electric vehicles (EVs) in dc parking lots, a resilient decentralized control framework is developed to give the system plug-and-play (PnP) capability. The PnP decentralized controller guarantees precise power dc and oscillatory components management among different assets. It also ensures seamless operation mode transition without the need for communication among assets.

For smart dc homes, a decentralized cooperative control (DCC) method along with a fault segment identification (FSI) scheme is designed to achieve the control and protection objectives by using only local measurements. The DCC method ensures accurate current sharing, dc bus voltage regulation, and fast restoration after the fault clearance. The main objective of the FSI scheme is to quickly identify and isolate the faulty segment to protect the sensitive power electronic components in the dc home from the high-fault current.

Extensive case studies, based on time-domain simulations using the Matlab/Simulink and PSCAD/EMTDC, are provided to evaluate the performance of the proposed schemes when the MMC is subject to various disturbances, e.g., load change, component failure, unbalanced load, and grid fault conditions. Furthermore, real-time studies are conducted in a hardware-in-the-loop (HIL) setup to verify the feasibility and resilience of the proposed schemes. This research will be the key for control and protection methodology development of MMCs and will lay the foundation for the future smart infrastructure.

Preface

This thesis is an original work by Amin Ghazanfari. As detailed in the following, some chapters of this thesis have been published or submitted for publication as scholarly articles in which Professor Yasser Abdel-Rady I. Mohamed was the supervisory author and has contributed to concepts formation and the manuscript composition.

Chapter 2 of this thesis has been published as A. Ghazanfari and Y. A-R I. Mohamed, "A Hierarchical Permutation Cyclic Coding Strategy for Sensorless Balancing Capacitor Voltages in Modular Multilevel Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 576-588, Jun 2016.

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Dedication

To my beloved family, whose boundless love and support has been ever constant

&

To all those who encouraged me to fly toward my dreams

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Chapter 1

Introduction

1.1 Background

In recent years, modular multilevel converter (MMC) technology has attracted growing interest in many low-, medium-, and high-voltage system applications such as high-power motor drives [1–3] and high-voltage dc transmission (HVDC) systems [1, 4–11]. This increasing interest is due to the benefits that MMCs offer in terms of reduced passive filter size, superior harmonic performance, low electromagnetic interference, fault management capability, and low switching losses. Features such as a common dc-link, modularity, and voltage scalability are other primary motivations for integrating the MMC architecture into modern transmission and distribution systems. Difficulties arise, however, associated with operating and controlling of the MMC and broadening its applications, e.g., unbalanced submodule (SM) capacitor voltages, lack of coordination or malfunction of the MMC components, variation in power flow direction, fault occurrence in dc link and/or ac grid, and instability issues [4, 5, 12, 13].

To fully realize the emerging potential of MMC technologies and overcome their

technical challenges, several control objectives including control of external voltages/currents, internal currents (circulating currents), average capacitor voltages, and individual capacitor voltage balance should be fulfilled [5, 14]. This research seeks to address the most important technical issues with MMC technologies from two main viewpoints —converter- and system-level interactions.

At the converter level, one of the potential challenges accompanying the modular structure of MMCs is SM capacitor voltage balancing. The voltage distribution among SM capacitors without a control unit may be subjected to a significant degree of imbalance; therefore, the voltage among SMs should be evenly distributed to guarantee the stable operation of MMCs at various operating points [5,15–18]. Moreover, MMCs are potentially subject to various internal and external ac and dc grid faults. The widespread acceptance of MMCs calls for robust configurations that can maintain and enhance the performance of the system and reduce the downtime and power-quality issues [6, 19–23]. These objectives can be realized by introducing a new SM circuit to ensure fault-tolerant capability for MMCs under various internal and external faults. In addition, reliability is another substantial issue associated with MMCs, particularly in those with a large number of levels, where each SM may be considered as a potential point of failure. Accordingly, the higher the number of SMs, the higher the failure rate of the converter. A faulty SM produces distortion in the output voltage and current and degrades the converter performance. This problem may cause the other components in the corresponding arm to fail and lead to total system collapse [24–27]. Hence, faulty SMs need to be quickly detected and restored to reduce the downtime and address the power-quality issues.

At the system level, building a dc distribution network, such as dc parking lot, is becoming a popular solution in modern power systems due to the rapid expansion of the electrical vehicle (EV) market and its associated charging infrastructure.

The smart dc home is another popular type of dc distribution network, which is an enabling structure for incorporating intelligent control units, distributed renewable energy sources (RESs), energy storage systems (ESSs), and dc and ac loads in the presence of a growing number of dc electronic devices in buildings [28–32]. The implementation of smart control strategies contributes to a resilient system design by merging the concepts of efficient energy control and intelligent load monitoring. The dc distribution network is often interfaced with the utility grid through bidirectional interlinking converters (BICs), where precise power-sharing among distributed generations (DGs) and BICs, and accurate voltage regulation are the most imperative control objectives. An MMC, as an interlink converter, should be able to maintain the system performance when subjected to various disturbances including load change, unbalanced load, and island conditions.

1.2 Literature Review

This section provides a comprehensive review concerning the most recent advances on the operational issues of MMC technologies. It also points out emerging applications of MMCs and their associated challenges.

1.2.1 Capacitor Voltage Balancing Methods

The voltage distribution among SM capacitors without a control unit may be subjected to a significant degree of imbalance. To guarantee stable operation of MMCs at various operating points, it is important to evenly distribute voltage among SMs. The capacitor voltages balancing methods are classified into three main categories –prior, inside, and after the modulation stage [5, 14, 16, 18, 33].

The first category refers to voltage balancing method by integrating a voltage

control loop into each SM. This kind of closed-loop method modifies the calculated modulation index by the current control unit. Because the control parameters are system dependent, the current references slightly deviate from the reference values [14, 34]. To compensate for the impact on the current loop reference deviation, a compensation term is added to the upper arm and subtracted from the lower arm modulation index using two loops. The injection of a common-mode voltage into the upper and lower arms, which restricts the application to converters with a neutral-to-ground connection, is another drawback of the methods in this category [5, 21, 34].

The second category includes various types of multilevel pulse-width modulation (PWM) techniques that have been developed for MMCs. In this category, the voltage balancing algorithm is integrated into the modulation stage. Among various PWM schemes, phase-shifted carrier (PSC) modulation is the most popular technique for MMC systems because it has some distinctive features, such as even power and stress distribution and low-voltage total harmonic distortion [11,35–37]. A detailed analysis has been conducted on the principles of PSC modulation to investigate the impact of the switching frequency and displacement angle on the performance of MMC systems in terms of switching harmonics and particularly capacitor voltages [16, 18]. To avoid diverging capacitor voltages, the switching frequencies in the PSC modulation technique have been restricted to values that are non-integer multiples of the fundamental frequency. There are some other switching frequencies as non-integer multiples of the fundamental frequency that may cause the capacitor voltages to diverge.

The third category indicates the voltage balancing approaches in which the balancing unit is implemented after the modulation stage. It is so called a post-modulation balancing algorithm. The response time of these methods compared to that of the first category is usually faster [12, 34]. Some popular strategies developed for SM capacitor voltage balancing in the MMC system are sorting algorithms such as the nearest

level control (NLC) method [4, 12, 17, 33] and predictive sorting algorithms [38]. In the NLC voltage balancing algorithm, capacitors with the highest and lowest voltages are selected to be discharged and charged, respectively, depending on the arm current direction. This approach necessitates the measurement of all SM capacitor voltages and thus diminishes the reliability. Moreover, two main drawbacks of these kinds of sorting algorithms are the high equivalent switching frequency and required processing time. Some researchers have tried to develop simplified NLC methods to reduce the processing time at the implementation level [33, 39]. However, the measurement of SM capacitor voltages in each arm is intricate, especially for MMC systems with many SMs per leg. To eliminate the need for capacitor voltage measurement and achieve low capacitor voltage ripple at the low switching frequency range, a predictive sorting algorithm has been presented to manage the charge and discharge of capacitors [38, 40]. This is a powerful control strategy; however, it is computationally intensive because there are many states that must be evaluated. Moreover, any small difference between the predicted and actual voltage values may result in the divergence of SM capacitor voltages in the steady state. The main difficulty in implementing this kind of sorting algorithm is the need for high computational resources to sort the capacitor voltages in ascending or descending order. A reduced switching frequency algorithm has been presented in [41], in which it is aggregated with the PSC modulation strategy to reduce losses and enhance efficiency. Although this method distributes energy equally among the SM capacitors at low switching frequencies, it operates like the NLC method in the sense that it requires the measurement signals from all SM capacitor voltages in order to sort them.

1.2.2 Submodule Circuits

The series-connected SMs form the building block of MMCs. The SMs can be categorized based on their features such as internal fault management, low power losses, and dc and ac fault handling capabilities. The half-bridge (HB) converters are the most common type of SMs that are used in the MMC topology for industrial applications [23, 42]. The HB circuit has only two switches within each SM and inserts one switch for each ac voltage step in the current path. Accordingly, the HB-based MMC offers the highest efficiency and lowest power loss among various SM configurations. However, one of the major challenges of the HB-based MMC topologies is the lack of dc-fault-handling capability. Hence, the protection system heavily relies on the ac circuit breaker with slow dynamics to trip in the case of fault occurrence. In addition, any internal fault occurrence in the HB structure makes the corresponding SM out of service, and it should be immediately isolated from the healthy SMs [6, 43].

There are several other SM circuits presented in the literature, and among them, the full-bridge (FB) and clamped-double (CD) are the most commonly used structures in the MMC topology due to their dc fault handling capability. The capacitor voltages of the FB and CD circuits generate reverse voltages to block the ac-side currents, which can drive the dc fault current to zero [6, 23]. This feature will shorten the time required to isolate the ac and dc sides of the MMC. However, the FB-based MMC features higher power losses and cost than the HB-based MMC due to the higher number of semiconductor devices. The CD SM inserts three semiconductor switches into a conduction path. Accordingly, the CD-based MMC has higher power losses than that of the FB-based and HB-based MMCs. One way to improve the efficiency of an MMC is to employ multilevel SM structures, such as flying capacitor, neutral point clamped (NPC), and T-type cells. The implementation of these multilevel structures leads to the overall reduction in the cost and weight of the whole converter

[5, 44–46]. However, the flying capacitor-based MMC presents a compromise between the modularity and reliability. On the other hand, the complexity of control and protection systems are the main drawbacks of the flying capacitor, NPC, and T-type SMs. Several other SM structures were proposed in the literature to improve the MMC performance in terms of fault handling capability, efficiency, and power quality [6, 43, 46–49]. The main limitations of the proposed SMs include the lack of modularity, large number of required components, high power losses, high capacitor voltage ripple, lack of internal fault management, and/or loss of SM capacitor voltages balance.

1.2.3 Fault-Tolerant Strategies

Several fault detection and identification methods that utilize model-based algorithms have been developed for MMCs [24–27, 50, 51]. The model-based methods may encounter some difficulties in detecting and identifying faults because of unmodeled dynamics, parameter uncertainty, and process noise. To attain a robust model-based method, a state-observer is incorporated to estimate system states based on the system model [26, 51]. In [27], a method is proposed to detect faults by comparing the measured state variables and the estimated ones by using a sliding mode observer. In [25], a fault detection method is suggested to provide the estimated state variables by using a Kalman filter. These methods yield a robust performance against measurement inaccuracies; however, they are computationally complex and demand higher processing resources, particularly for a system with a large number of states. Another model-based method is implemented by using filters with appropriate filter gain. These filters function like a piecewise linear observer. Whenever a fault occurs, the filters indicate specific characteristics that allow the fault to be detected [24]. Artificial intelligence-based methods are other detection approaches where neural

networks or fuzzy-logic-based algorithms are applied to detect the fault point in the trained expert system [51,52]. They need to be trained by using a large number of operating points under various fault scenarios to obtain a satisfactory performance. This process may be intricate and inaccurate for an MMC with a large number of levels. A method based on high-frequency harmonic analysis has been presented to detect faulty cells in cascaded multicell converters by measuring just one voltage per output phase [53]. This method demands more processing resources than other methods and is more complicated for a converter with a high number of cells, especially in transient operation. On the other hand, several fault detection approaches have been proposed in the literature for conventional two-level voltage-source converters [26,54–56]. However, these approaches are not applicable to the MMC topology because only limited information is available to locate the failure point.

After detecting and then locating the fault, a postfault restoration scheme is employed to ensure service continuity. In terms of achieving the fault tolerance feature, postfault restoration schemes in the literature can be classified into two main groups: reconfiguration- and redundancy-based schemes. The reconfiguration-based schemes aim to reconfigure the switching pattern and control structure in order to minimize the performance degradation [57]. These schemes negatively impact the overall system performance. The redundancy-based schemes are implemented to maintain the system performance by providing some redundancy in the system [58,59]. These schemes come with an additional cost associated with the redundant modules. Hence, choosing between the reconfiguration- and redundancy-based schemes is application-dependent and demands a comprehensive performance analysis.

1.2.4 MMC for a Wide Range of Applications

In recent years, the dc distribution system concept has attracted growing interest for industrial and residential electrical system applications, aiming to enhance reliability, power quality, and efficiency. A simpler control strategy, higher efficiency and reliability, and easier interconnection of RESs and energy storages are some major advantages of the dc distribution system as compared to the ac counterpart [30, 60–62]. Furthermore, the dc system can easily integrate dc loads and EVs into the distribution network. The dc network can be interfaced with the utility grid via a BIC. Along with these gains, the most prominent challenges are the lack of standardization of the control and development of protection strategies, which hinders the implementation of dc distribution system in modern electricity networks.

The main control objectives in a dc distribution system are precise power sharing among DGs and accurate regulation of the dc bus voltage. For the grid-tied networks, another control system needs to be designed to ensure high efficiency and to enhance the power quality of the BIC. The operation mode transition could expose the system to stability problems, particularly in the presence of unbalanced ac loads. Although the BIC controllers can be separately designed to function stably in both the on- and off-grid modes, this design cannot guarantee the stability of the overall system during operation mode transition [63, 64]. In addition, oscillatory power components introduces pulsations of twice the fundamental frequency into the dc bus voltage through the single-phase and/or three-phase unbalanced loads. Accordingly, an effective control system must be designed to cope with the power oscillatory components. A crucial problem is observed, particularly when some DGs with a fast transient response are forced to supply a high portion of power oscillatory component beyond their capabilities. Consequently, this problem deteriorates the system performance, leading to a degradation in the DGs performance or even a complete system

breakdown [65–69].

The droop control method is typically used as the primary control to regulate the output voltage of individual converters by adding a virtual impedance to the voltage control loop [28]. However, the basic droop method has some drawbacks including load-dependent voltage deviation and the inability to provide coordinated performance of multiple resources. Hence, secondary and tertiary controllers are implemented to, respectively, restore the voltage and ensure precise power sharing among DGs. The supervisory centralized, distributed, and decentralized controllers are three different approaches that can be implemented with the basic droop control to address the aforementioned problems in the primary controller.

The centralized control collects information from all distributed units through communication links [70–72]. The research results in [73] showed that the leadership in energy and environmental design (LEED) buildings equipped with the centralized and static control systems may not be energy efficient. In addition, the main disadvantage of the centralized control is that any communication link failure can cause the cascading failure of other units and destabilize the entire system. As an alternative method, the distributed control simplifies the communication network and eases the scalability of the system by exchanging information only between units [74–76]. Unlike the centralized control, the distributed control is able to cope with a single point of failure. However, the main disadvantage of distributed control is its complexity associated with stability and convergence analysis of the system in practice, where communication delays and measurement errors occur. The third approach is the decentralized control, which easily coordinates units within the system without communication [77–79]. However, the lack of information from other units is this approach's main drawback, which limits the applicability of the decentralized control in its basic shape.

The dc distribution architecture is highly vulnerable to a dc fault, which can paralyze DGs and other components until the fault is totally cleared. The magnitude of the dc fault current significantly depends on the impedance characteristics, configuration, and technologies employed in the dc system. The high-magnitude fault current can completely de-energize the entire system. Hence, another main priority for the dc power systems is the design of a fast and reliable protection system. Several communication system-based protection schemes including detection and identification algorithms were developed to avoid system malfunction and reduce the fault detection time [80–82]. However, the main drawback of these approaches is their reliance on communication links. To avoid the problems associated with communications, a non-unit protection scheme was proposed based on local measurements [83]. However, this algorithm needs high computational resources to detect the faulted zones by analyzing the first- and second-order derivatives of the current. The limitations of the non-unit protection and current differential protection methods were thoroughly discussed in [84]. A handshaking method was presented to distinguish a faulted line by splitting the dc system into several zones [85]. As this method was implemented by using only local current and voltage measurements, it had high reliability. The main drawback is that the handshaking method may cause the entire system to shut down when a fault occurs. Therefore, an efficient algorithm is needed in order to cope with the aforementioned drawbacks in the previously proposed protection schemes.

1.3 Statement of the Problem and Research Objectives

As was explained in Section 1.2.1, the existing capacitor voltage balancing approaches suffer from one or more limitations/weaknesses including:

- A large amount of wiring among the voltage sensors of SMs and control units is needed.

- The balancing controller requires arm current signals to insert/bypass the SMs inside the corresponding arm based on the current direction.
- The increased number of SMs increases the processing time and complicates the hardware implementation.
- SM capacitor voltages are balanced at the expense of an increase in the device switching frequency.
- The device switching frequency becomes difficult to estimate with analytical methods because the insertion state is determined in a stochastic manner.

The first part of this research work seeks to propose a modulation algorithm that addresses the limitations/weaknesses of the previous schemes while meeting the following objectives:

1) To maintain the capacitor voltages balance with no need for additional hardware implementation to contribute to the reliability, computational resources, and simplicity of the MMC;
2) To avoid the impact of parameter variations on the system performance;
3) To achieve a narrow boundary so that all SM capacitor voltages can track their nominal values within that boundary without diverging in the steady state;
4) To develop an algorithm which can be combined with other modulation techniques and be implemented for a wide range of switching frequencies;
5) To propose an approach with the capability to be extended for MMCs with any voltage level, without the computational burden of a high-order system;
6) To devise a control block decoupled from other control loops with no need for feedback from other control parameters.

To attain these objectives, a new hierarchical permutation cyclic coding (PCC) strategy is proposed. This hierarchical strategy is implemented after the PSC modulation stage in the MMC. This post-modulation balancing algorithm is derived by

assigning a given permutation sequence within a cyclic time. Based on the PCC method, a bi-mapping is defined between the permutation sequence and switching gate signals to periodically permute the pulse pattern among the SMs of the corresponding arm.

As was explained in Section 1.2.2, MMCs equipped with conventional SM circuits or hybrid circuits suffer from one or more limitations/weaknesses including:

- The lack of modularity is a drawback, especially for MMCs with hybrid SM circuits.
- The impact of the grid and dc-link fault conditions has not been extensively studied.
- The transient studies are often performed based on a simplified model of MMCs and the host ac system.
- The details of the internal dynamics of the MMC are often neglected.
- Some SM circuits require a large number of components, leading to an increase in power losses.
- The design of control and protection systems is complicated due to the SM structure.
- Internal fault management and SM capacitor voltage balancing are lacking.

The second part of this research work proposes a new SM circuit that addresses the limitations/weaknesses of the existing SM circuits while meeting the following objectives:

1) To facilitate internal fault management;
2) To provide features including full modularity, low power losses, and ease of expandability;
3) To obtain the most efficient current path and realize inherent capacitor voltage balancing features;

4) To enable easy incorporation of new SMs into conventional HB-based MMCs;
5) To guarantee the continued operation of MMCs under switch open-circuit fault conditions without needing any mechanical bypass;
6) To analyze the internal dynamics of the MMC, including SM capacitor voltages and circulating current;
7) To maintain the system performance under various ac and dc-link fault conditions.

To attain these objectives and facilitate the fault-tolerant capability for MMCs under various internal and external fault conditions, a new SM circuit is designed and tested.

As was explained in Section 1.2.3, the existing fault-tolerant schemes suffer from one or more limitations/weaknesses including:

- System reliability is highly affected by any fault occurrence in the arm current sensors.
- A high-bandwidth monitoring system is required.
- The unnecessary over-provisioning in the monitoring system implementation leads to higher system costs.
- The capacitor voltage balancing is affected by any fault occurrence.
- Internal faults cannot be distinguished accurately from external faults and sensor breakdown.

The third part of this research work proposes a fault-tolerant framework that addresses the limitations/weaknesses of the existing schemes while meeting the following objectives:

1) To create a supervisory algorithm ensuring the coordinated operation of two monitoring and decision-making units;
2) To achieve a low-bandwidth monitoring system to reduce costs and computa-

tional burdens;

3) To distinguish the internal converter faults from the external disturbances in a brief time period from detection to identification;
4) To distinguish among different faults occurring inside the MMC architecture—i.e., in the SMs, voltage sensors, and current sensors;
5) To keep all SM capacitor voltages balanced to track their nominal values after the occurrence of multiple faults and even in the presence of faulty current sensors;
6) To diagnose simultaneous faults in an arm, guarantee resilient system operation under various open-circuit faults, and restore the system in a few milliseconds after the fault occurrence.

To attain these objectives, a resilient supervisory algorithm including two monitoring units and a decision-making unit as well as a postfault restoration block are devised.

As it was presented in Section 1.2.4, MMCs can be used in a wide range of applications. For dc distribution networks, conventional control and protection frameworks suffer from one or more limitations/weaknesses including:

- The integration of a variety of ac and dc loads and the stochastic nature of the arrival and departure of EVs can cause severe load transient and EMI issues.
- The introduction of single-phase converters and three-phase unbalanced ac loads exposes the dc system to a significant degree of unbalanced conditions.
- The power oscillatory component introduces pulsations of twice the fundamental frequency into the dc bus voltage of the system.
- The impact of the different dynamic models of DGs on the system performance is ignored.
- The operation mode transition in BICs can expose the system to stability issues.
- A more complicated communication protocol should be designed whenever the

number of electrical components becomes too large.

- Fault detection and identification approaches rely on communication links.

The fourth part of this research work develops control and protection techniques suitable for a dc distribution network with an MMC. The proposed methods address the limitations/weaknesses of the existing schemes while meeting the following objectives:

1) To integrate DGs with different dynamics into the dc system and control them in a decentralized manner;
2) To ensure accurate power oscillatory and dc components-sharing under a wide range of rapidly varying single-phase and three-phase unbalanced ac loads;
3) To guarantee the overall system performance when the BIC operates in different modes;
4) To enable the plug-and-play capability and enhance the system's ability to reconfigure once a fault occurred;
5) To ensure fast system restoration after fault clearance, effective dc bus voltage regulation, and accurate current sharing among the DGs and MMC, based on only local measurements.
6) To identify the faulty segments before the fault current can completely deenergize the entire system.

These objectives are achieved by proposing a resilient plug-and-play (PnP) decentralized control framework for dc parking lots and a decentralized cooperative control (DCC) method along with a fault segment identification (FSI) scheme for smart dc homes. The parking lot incorporates various electric components including plug-in and wireless EV charging stations, RESs, energy storage devices, and ac loads. The BICs are equipped with a switched control system to ensure the overall system performance in different modes of operation. To attain the above-mentioned objectives

for a smart dc home, the DCC and FSI methods are developed to meet the control and protection objectives by using only local measurements.

1.4 Methodology

To achieve the above research objectives, the following methodology is employed:

Model Methodology: Detailed modeling of the MMC is an essential step that enables design and verification of the proposed capacitor voltage balancing and fault-tolerant algorithms. However, the detailed switching models demand a significant increase of the required computing time. Therefore, the MMC model is developed from a number of averaged model subsystems/modules that are employed to study internal dynamics of the MMC as well as system-level interaction.

Time-domain simulation: To evaluate and validate the performance of the proposed methods and to investigate their behavior under various operating conditions, digital time-domain simulation studies are conducted on a 21-level MMC to confirm the effectiveness of the proposed algorithms in PSCAD/EMTDC or MATLAB/Simulink environment.

Hardware implementation: The proposed control strategies are implemented and tested in the FPGA-based RT-LAB real-time simulator platform to demonstrate the feasibility of hardware implementation, and validate their performance in a hardware-in-the-loop setup.

1.5 Thesis Outline

This thesis focuses on proposing new control and protection strategies, circuit design, and application areas for the MMC topology. The organization of the thesis is shown in Fig. 1.1, where the thesis consists of six chapters:

Chapter 1 presents the background and main objectives of the thesis.

Chapter 2 proposes a sensorless capacitor voltage balancing strategy for MMCs. The control objective is to effectively balance SM capacitor voltages within the upper and lower arms in a wide range of switching frequencies. The performance of the proposed hierarchical PCC strategy is evaluated based on both off-line time-domain and hardware-in-the-loop simulation test cases.

Chapter 3 develops an SM circuit to facilitate fault-tolerant capability for MMCs under various internal and external faults. A switching signal adapter is designed to provide the MMC with features such as inherent capacitor voltage balancing, internal fault management, external fault-handling capability, and ease of expandability. The MMC employs the hierarchical PCC algorithm of Chapter 2 for the capacitor voltage balancing. The MMC is also equipped with the fault tolerant strategy of Chapter 4. Off-line time-domain and real-time hardware-in-the-loop simulations demonstrate the dynamics of the MMC equipped with the proposed SM circuit.

Chapter 4 proposes a supervisory fault-tolerant algorithm integrating two monitoring and decision-making units to detect and identify SM failures by analyzing the circulating currents and SM capacitor voltages. The proposed supervisory algorithm handles the failure of multiple SMs in a very short time and guarantees a fast postfault restoration. The MMC employs the capacitor voltage balancing method developed in Chapter 2. In addition, the MMC structure integrates the proposed SM in Chapter 3 as a redundant SM into each arm. Analysis of the MMC dynamics, time-domain simulation studies in Matlab/Simulink, and hardware-in-the-loop validation studies

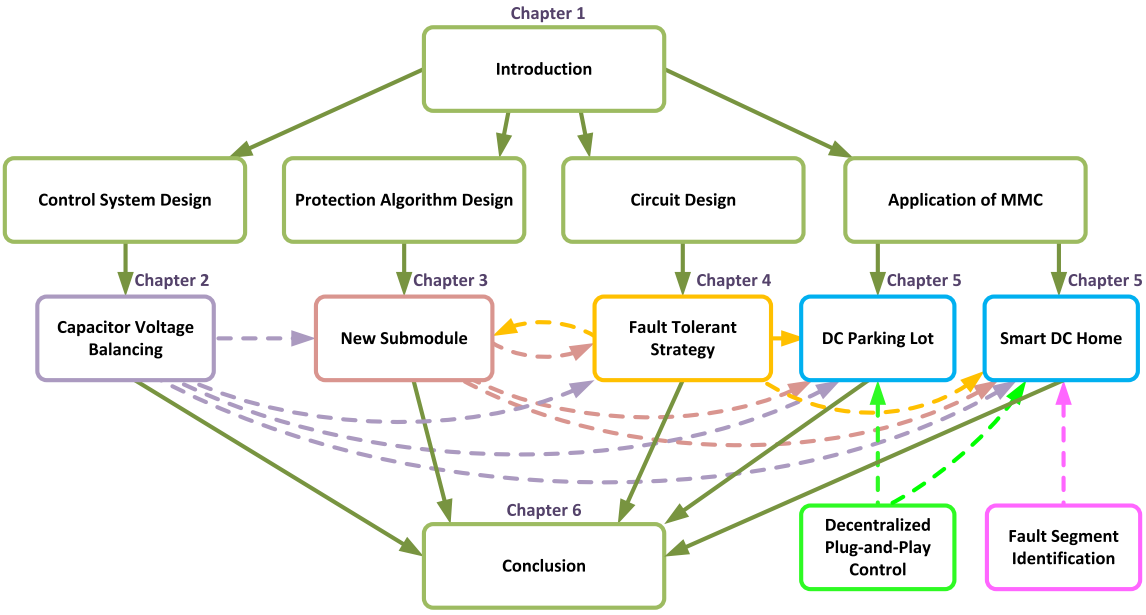


Figure 1.1: Organization of the thesis.

demonstrate the effectiveness of the proposed fault-tolerant strategy.

Chapter 5 investigates the performance of the proposed control and protection strategies in a dc parking lot and smart dc home integrating the MMC topology. The proposed control framework ensures accurate current sharing, dc bus voltage regulation, and fast restoration after the fault clearance without the need for communication among assets. The main objective of the protection scheme is to quickly identify and isolate the faulty segment by using only the information extracted from the local current sensor. Furthermore, this chapter studies the dynamics of the MMC adopting the capacitor voltage balancing method of Chapter 2, SM circuit of Chapter 3, and fault-tolerant strategy of Chapter 4. The analytical results are validated based on simulation results in PSCAD/EMTDC environment and hardware-in-the-loop setup.

Chapter 6 summarizes the major contributions of the thesis and provides future research directions.

Chapter 2

Sensorless Capacitor Voltage Balancing

This chapter develops the hierarchical PCC algorithm implemented after the PSC modulation stage in an MMC to achieve effective capacitor voltage balancing feature. The proposed technique is a post modulation balancing algorithm derived by assigning a given permutation sequence within a cyclic time, which can address the problems with previously proposed methods.

2.1 Operation Principles and Terminology of MMC

A schematic diagram of a one-phase leg of an MMC is illustrated in Fig. 2.1. Each phase unit of MMCs consists of two arms, each having a total of N SMs. The upper and lower arms are connected through one inductor and resistor. The inductor in each arm is employed to limit fault and parasitic currents and compensate for the voltage difference between the upper and lower arms. The resistor indicates the parasitic resistance of inner inductor and model converter losses. The midpoint between the

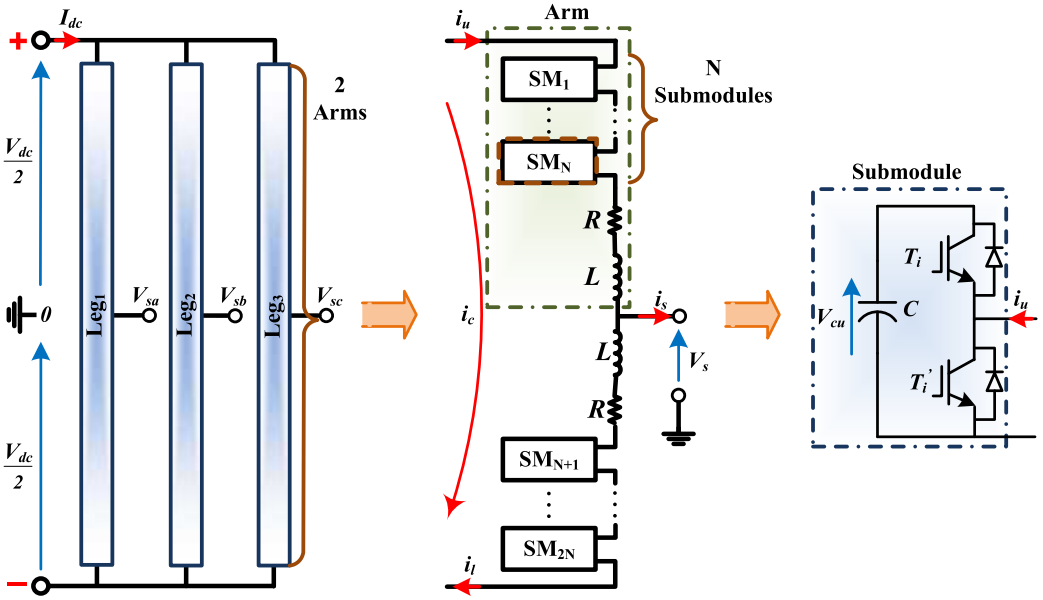


Figure 2.1: One-phase leg of the MMC topology and structure of one SM.

Table 2.1: Operation of the SM

T_i	T_i'	SM status	Arm current	Capacitor	Output voltage
ON	OFF	ON	Positive	$C \uparrow$	V_{cu}
			Negative	$C \downarrow$	V_{cu}
OFF	ON	OFF	Positive	Bypass	0
			Negative	Bypass	0

two arms is the AC terminal location. Each SM is typically an HB circuit consisting of a dc capacitor and two complementary switches. Depending on the switching status and arm current direction, the SM output voltage has only two values in normal operation (see Table 2.1). According to the states of N series-connected SMs (inserted and/or bypassed), an alternating voltage is generated in the corresponding arm, where it is composed of $N + 1$ voltage levels.

Since the MMC consists of the switched SM capacitors, it is categorized as a dynamic converter. The internal dynamics of the MMC includes the circulating current and all capacitor voltages [86]. The following equations express the characteristics of

an MMC:

$$L\frac{di_c}{dt} + Ri_c = \frac{v_{dc}}{2} - \frac{v_l + v_u}{2} \tag{2.1}$$

$$L\frac{di_s}{dt} + Ri_s = \frac{v_l - v_u}{2} - v_s \tag{2.2}$$

where the total output voltage of the upper and lower arms generated by the cascaded SMs is represented by v_u and v_l, respectively. v_{dc} is the total dc-link voltage. The circulating current, i_c, is introduced when there is any voltage difference between each leg and dc-link. It includes both dc and even-order harmonic components; the former corresponds to power exchange between legs and dc-link, and the latter increases the current stress and power loss. The upper and lower arm currents can be expressed in terms of the output current and circulating current. Accordingly, the current dynamics of the arm current of one phase of the MMC can be expressed as

$$i_u = i_c + \frac{i_s}{2} \tag{2.3}$$

$$i_l = i_c - \frac{i_s}{2} \tag{2.4}$$

where the arm currents are denoted by i_u and i_l. The subscripts u and l refer to the upper and lower arms, respectively. By assuming that the converter is lossless and harmonic components of the circulating current are eliminated, the arm currents can be expressed as

$$i_u = \frac{\sqrt{2}I_s}{4} mcos(\varphi) + \frac{I_s}{2} cos(\omega_1 t - \varphi) \tag{2.5}$$

$$i_l = \frac{\sqrt{2}I_s}{4} mcos(\varphi) - \frac{I_s}{2} cos(\omega_1 t - \varphi) \tag{2.6}$$

where m is the modulation index. I_s is the amplitude of the output current, ω_1 is the fundamental frequency, and φ is the power angle. The voltage across the capacitor

in each SM is given by [18]

$$v_{cui} = V_{0i} + \frac{1}{C}\int (S_{ui} i_c + \frac{1}{2} S_{ui} i_s) dt \tag{2.7}$$

$$v_{cli} = V_{0i} + \frac{1}{C}\int (S_{li} i_c - \frac{1}{2} S_{li} i_s) dt \tag{2.8}$$

where V_{0i} is the initial value of the SM capacitor voltage. S_{ui} and S_{li} denote the corresponding switching states of the i-th SM in the upper and lower arms, respectively. By comparing a carrier waveform corresponding to each SM with the reference waveform, each switching function is generated. The SM is inserted when the switching function equals one, and is bypassed when the switching function equals zero.

Owing to the charging and discharging of SM capacitors according to the current direction of the corresponding arm, each individual capacitor voltage includes a ripple component in addition to its direct component. The output voltages of the ith SM in the upper and lower arms by using the PSC modulation during nominal operation are given by [18]

$$v_{cui} = V_{0i} + \frac{1}{C}\int [(\frac{1 - mcos(\omega_1 t)}{2} + \sum_{a=1}^{\infty}\sum_{b=-\infty}^{\infty} A_{abui}) i_u] dt \tag{2.9}$$

$$v_{cli} = V_{0i} + \frac{1}{C}\int [(\frac{1 + mcos(\omega_1 t)}{2} + \sum_{a=1}^{\infty}\sum_{b=-\infty}^{\infty} A_{abli}) i_l] dt \tag{2.10}$$

where [87]

$$A_{abui} = \frac{2}{a\pi} J_b(\frac{m\pi a}{2}) sin[\frac{(a+b)\pi)}{2}] \times cos[a(\omega_c t + \frac{2\pi i}{N} + \alpha + \beta) + b(\omega_1 t + \pi)] \tag{2.11}$$

$$A_{abli} = \frac{2}{a\pi} J_b(\frac{m\pi a}{2}) sin[\frac{(a+b)\pi)}{2}] \times cos[a(\omega_c t + \frac{2\pi i}{N} + \alpha) + b\omega_1 t] \tag{2.12}$$

where ω_c is the angular frequency of the triangular carrier waveforms, and J_b is

the Bessel functions of the first kind. a and b refer to the harmonic order of the carrier and reference waves, respectively. α is the angular displacement between the reference and triangular carrier waveforms, and β is the angular displacement in the triangular carrier waveform between the upper and lower arms. The value of β is assigned to cancel out switching harmonics in the upper and lower arm output voltages. Accordingly, it is zero for an odd number of SMs per arm and π/N for an even number of SMs per arm to minimize the output voltage harmonics [16, 38].

To attain stable capacitor voltage during the steady state operation, two criteria should be met. First, the direct components in the second term of SM capacitor voltages in (2.9) and (2.10) should be canceled out to prevent instability. Second, any direct or fundamental frequency components in the capacitor voltage should be independent of the index i to prevent voltage divergence. By substituting arm currents in (2.9) and (2.10) with (2.5) and (2.6), there will be a sum of three terms consisting of direct and alternating components. The first term is a direct component referring to SM initial voltage. The second term is a combination of dc and alternating components independent of the index i and the switching frequency. However, the multiplication of the arm current and A_{abi} in the third term can produce any direct or fundamental frequency components which have the potential to cause capacitor voltage divergence. If ω_c is an integer multiple of ω_1, referring to (2.11) and (2.12), some of the resultant harmonic terms will dependent on index i. Consequently, these terms have different effects on different SMs inside the arm. Hence, the switching frequency as an integer multiple of the fundamental frequency should be avoided to maintain balance in the capacitor voltages. It should be noted that there are also some other frequencies that can cause the capacitor voltages to diverge [18].

The amount of charge in the capacitor of each SM inside the upper or lower arm is the integral of the arm current over the charging and discharging time intervals. De-

pending on the employed switching scheme, the charging and discharging amounts of each SM differ from time to time. Because the SMs of each arm are series-connected with the same initial voltage condition, there is a multiple-degree of freedom modulation system. The degree of freedom corresponds to a set of permutations of SMs inside the arm without repetition. Therefore, the insertion of SMs into each arm can be performed by using an algorithm aimed to distribute equal amounts of energy among SM capacitors within a given sample time. It means that the switching pattern can assign some SMs to insert and/or bypass in such a way that the SM capacitor voltages track their reference values in the steady state.

2.2 Hierarchical Permutation Cyclic Coding Strategy

Uneven distribution of the stored energy among SMs of an arm results in voltage deviation within SMs of the corresponding arm. The aim of this section is to provide a full description of the proposed capacitor voltage balancing strategy. This strategy utilizes a redundant switching state of cascaded SMs to keep the energy stored in the chopper cells capacitors balanced in a wide range of switching frequencies. The voltage balancing unit is going to be located at the output stage of the modulation unit to permute the switching gate signals among SMs of each arm at equally spaced intervals over the switching period [88].

2.2.1 Permutation Sequence

Fig. 2.2(a) indicates the permutation sequence arrangement for an MMC with five SMs per arm. The states are clustered into several five-vector groups to make the generated sequence more compact with minimal redundancy. The ring includes $(N-1)!$ segments of arcs, where N represents the number of SMs per arm. Each arc represents

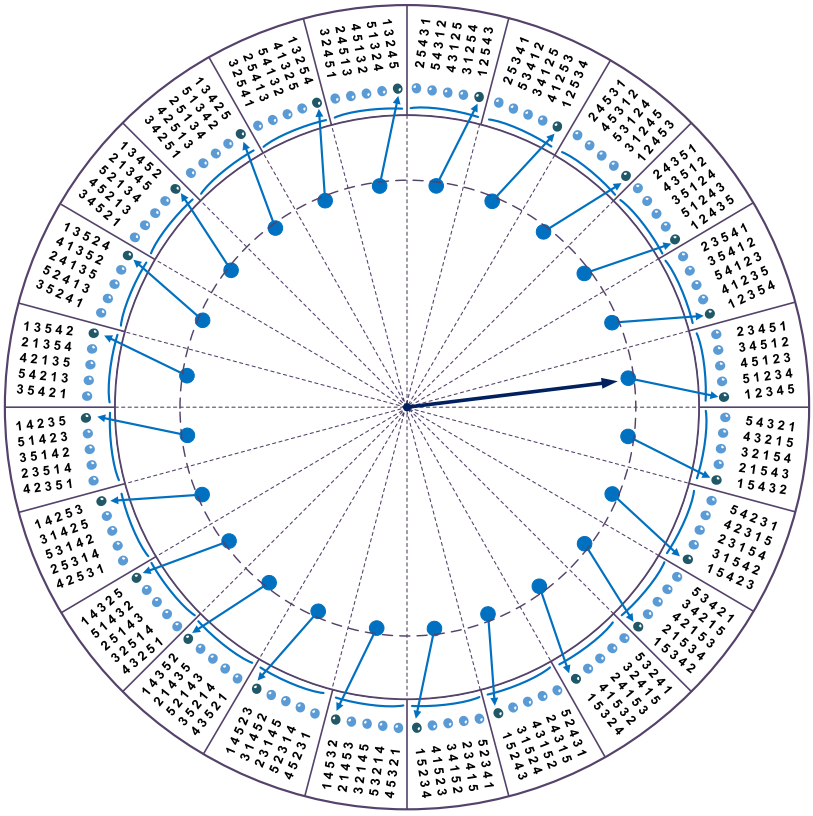
a cluster formed by cyclically right-shifting the very last permutation vector index, where shifting is executed each time by one index.

To aid in understanding the method at the basic level of the implementation, a consolidated pictorial representation of the proposed permutation sequence is shown in Fig. 2.2(b). The permutation sequence of the MMC with five SMs per arm is stored in a lookup table as a matrix with 5! rows and five columns. The balancing algorithm provides cyclic right-shifting of the permutation vectors at the specific dwell time which can be defined as a coefficient of the fundamental switching period. The dwell time refers to equally spaced intervals over the switching period to permute the switching pattern. In the basic case with five SMs per arm, there are 5! vectors, which should be sorted in the permutation table that is classified into 24 clusters of submatrices with five rows and five columns. The bilateral arrows in each row indicate the inserted SM, which corresponds to the rows of vectors in the permutation sequence stored in a matrix.

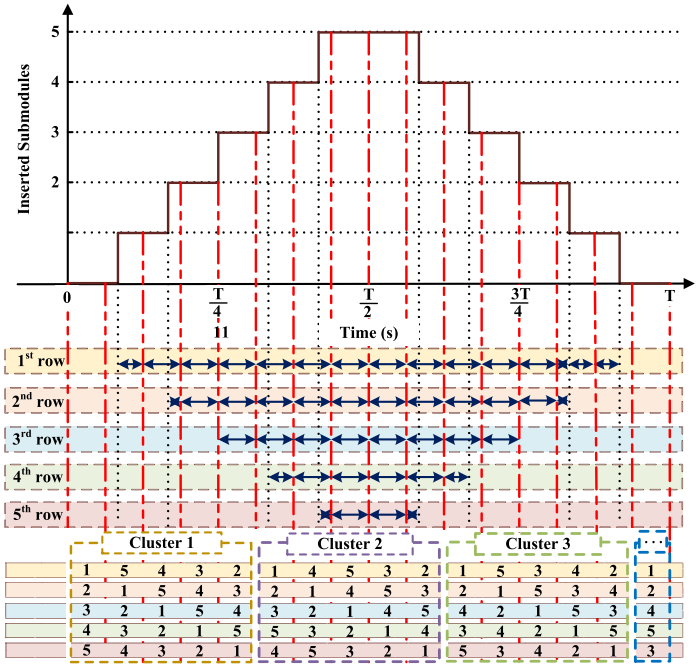
There is a simple one-to-one mapping from the switching gate signals into the permutation sequence vectors. With the permutation table designed and dwell time defined, the balancing of SM capacitor voltages is realized by using the PCC algorithm to evenly permute the switching gate signals among SMs of each arm.

2.2.2 PCC Algorithm

Fig. 2.3 presents a flowchart of the proposed PCC algorithm to balance SM capacitor voltages for an MMC with five SM per arm. First, the permutation table is loaded, and the starting point for algorithm execution is set at the zero crossing of the arm current. Then, the generated switching gate signals from the PSC modulation unit are placed into a vector form and fed as an input to the PCC unit. The permutation table is composed of 5! permutation states for five SMs per arm. To determine the



(a)



(b)

Figure 2.2: (a) Permutation sequence arrangement for the MMC with five SMs per arm. (b) Pictorial presentation of the proposed balancing algorithm for an MMC with five SMs per arm.

order of counterpart states, the 'floor' function is used to assign a real number to the largest previous integer numbers. Then, the 'mod' function is added to make the orders cyclic upon reaching the maximum number of permutation states. If the order is zero, the order equals 5!, and it is at the end of the switching sequence. Accordingly, the output signals are assigned based on the permutation sequence. For instance, the first row of the permutation matrix will be selected if the order is 1. In this case, the input of the balancing unit will be directly sent to the output. To prevent unnecessary SM switchings, the order of the permutation table should not be changed until the next dwell time.

To meet the first criterion in 2.2.1, initial capacitor voltages should be sufficiently close to avoid any extension in the boundary range of SM capacitor voltages in each arm. Swapping the switching sequences among SMs distributes the terms dependent on index i in (2.11) and (2.12) among the SMs periodically. The integral of the arm current over a specified permutation time period will be the same for all units accordingly. Therefore, the switching frequency can be defined in a wide range of integer and non-integer multiples of the fundamental frequency by virtue of the PCC unit. In addition, the stored energy and switching loss will be evenly distributed among SMs in the corresponding arm over the permutation time.

2.2.3 Implementation of Hierarchical PCC Algorithm

The increased number of SMs makes it difficult to implement the same permutation algorithm with a large number of permutation vectors and achieve stable capacitor voltage balancing. To address this concern, a hierarchical PCC algorithm is developed to handle a large number of SMs per arm. The hierarchical PCC algorithm includes two stages. At the first stage, the switching gate signals are categorized into two groups–i.e., odd and even. Then, signals are fed into two basic permutation units;

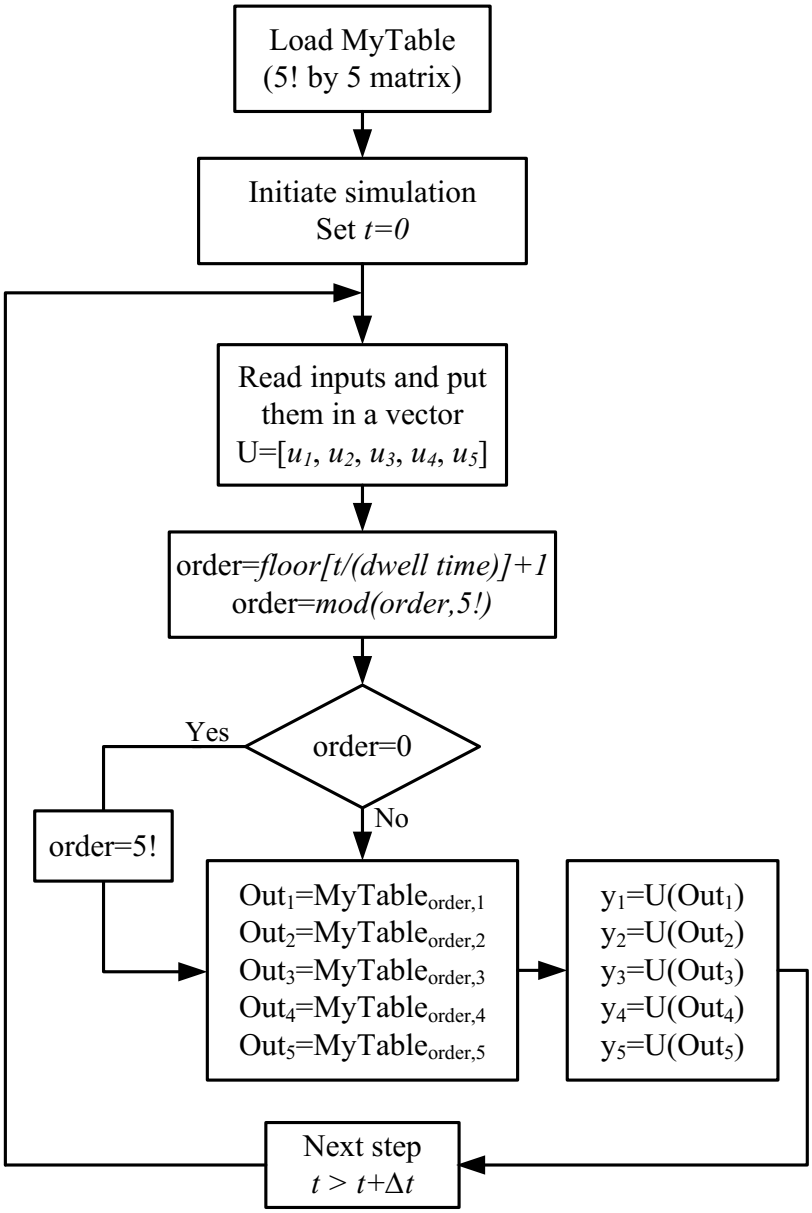


Figure 2.3: Flowchart describing the proposed PCC algorithm to balance SM capacitor voltages for the MMC with five SMs per arm.

odd signals go to one PCC unit, and even signals go to the next unit. At the second stage, the outputs of each even and odd PCC unit is assumed to be vectors composed of five switching pulses. These vectors are also categorized into two odd and even groups and then fed to the next PCC unit at the second stage. The dwell time of the second stage should be set twice of that of the first stage to yield a computationally

efficient algorithm. During the start-up process, the SM initial voltages are pre-charged to the reference voltage value. Different initial voltages of SMs may expand the boundary range of capacitor voltages in each arm.

Fig. 2.4 depicts a schematic diagram of the hierarchical PCC algorithm for an MMC with ten SMs per arm. This approach can be simply extended to an MMC with a higher number of SMs. One of the main advantages of the proposed method lies in the parallel implementation of the PCC units at each stage, which increases the speed of computation for the MMC with a large number of SMs. The final output of the hierarchical PCC algorithm is the exchanged switching gate signals, which provides even SM utilization over the permutation time. Because the proposed algorithm simply performs memory addressing, the computational requirements of the proposed algorithm are not demanding. Furthermore, it does not depend on the system parameters, which yields an inherently robust solution.

2.3 Test Cases

The effectiveness of the proposed capacitor voltage balancing strategy is validated by simulation studies performed in Matlab/Simulink. The specification of the simulated three-phase 21-level MMC is listed in Table 2.2. Fig. 2.5(a) represents the entire control structure of the simulated system. Fig. 2.5(b) shows the trigger generator block in detail. The PSC modulation technique is employed for the upper and lower arms, in which the comparison of the reference waveform with the triangular carrier after passing through the proposed hierarchical PCC algorithm generates the switching gate signals for the corresponding arm. Each leg of the simulated MMC is composed of ten SMs per arm. Simulation results are shown for the upper and lower arms of phase a.

Fig. 2.6 indicates the line-to-line output voltage; upper arm, lower arm, and circu-

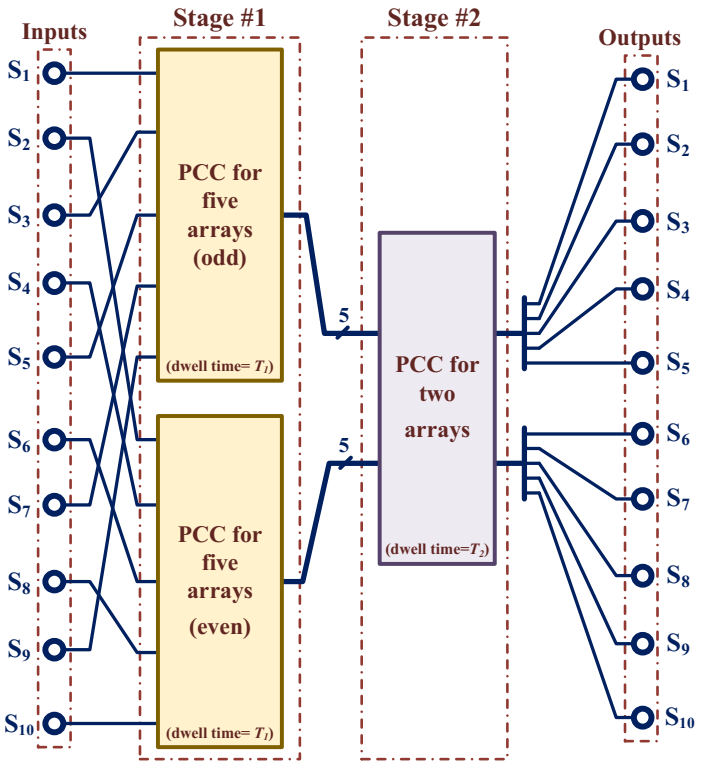


Figure 2.4: Schematic diagram of the hierarchical PCC algorithm for an MMC with ten SMs per arm.

lating currents; and output current of phase a. Because there are ten SMs per arm, the line-to-line output voltage consists of 21 voltage levels. The circulating current of the system operating with load active power of 115 kW equals 10.3 A, and the output current of phase a equals 39.13 A.

The performance of the proposed strategy is investigated at low and high switching frequencies, which may be an integer or non-integer multiples of the fundamental frequency. Furthermore, its performance under balanced and unbalanced load conditions is evaluated. For scenarios with high switching frequencies, a case study with 1950 Hz; and for low switching frequencies, a case study with 300 Hz are examined. At the first stage of the hierarchical PCC algorithm, the dwell time is the same as the fundamental time period. At the second stage of the hierarchical PCC algorithm, the dwell time should be twice the dwell time of the first stage.

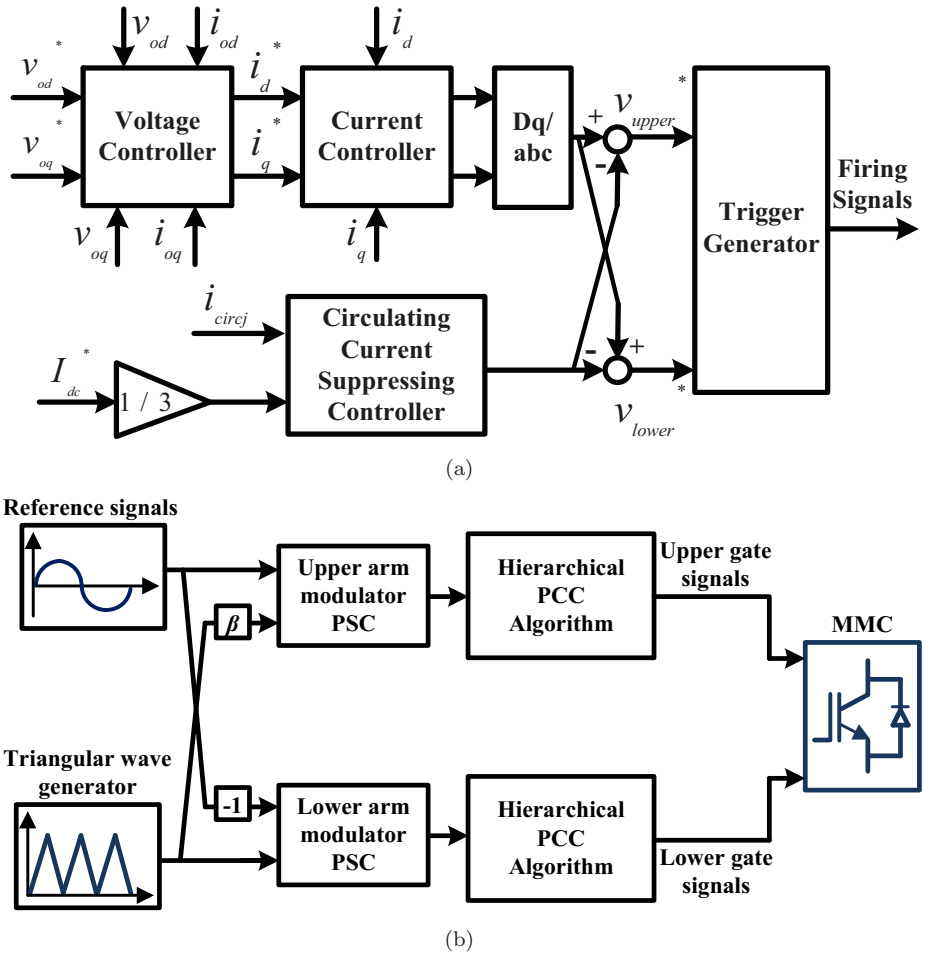


Figure 2.5: (a) Control structure of the MMC; (b) Block diagram of the PSC modulation and capacitor-voltage balancing unit.

2.3.1 High and Low Switching Frequencies

Fig. 2.7 indicates the SM capacitor-voltage waveforms of the upper and lower arms when PSC modulation is employed at a switching frequency of 1950 Hz. In this case, the switching frequency is a non-integer multiple of the fundamental frequency. However, the SM capacitor voltages in the arm may diverge because there are some frequencies that can cause the capacitor voltage divergence in the PSC modulation technique [18]. In this case, capacitor voltage balancing is unstable at 1950-Hz switching frequency when only the PSC modulation is applied.

The SM capacitor-voltage waveforms of the upper and lower arms at the 1950-Hz

Table 2.2: Circuit Parameters of The MMC System.

Parameter	Value
Number of SMs per arm	10
DC-link voltage	3750 V
Line-to-line voltage	2.4 kV
Line frequency	60 Hz
SM capacitance	9900 μF
Arm inductance	20 mH
Arm equivalent resistance	0.3 Ω

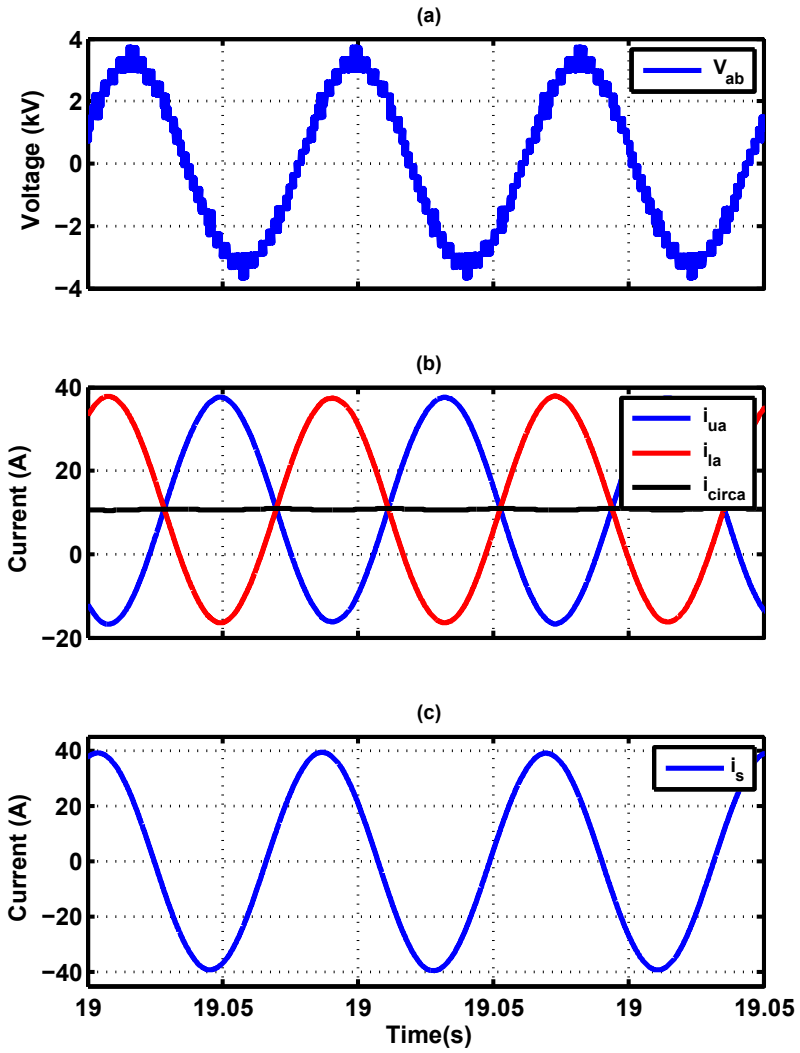


Figure 2.6: Simulation results with the proposed balancing unit: (a) Line-to-line output voltage. (b) Arm currents and circulating current. (c) Output current of phase a.

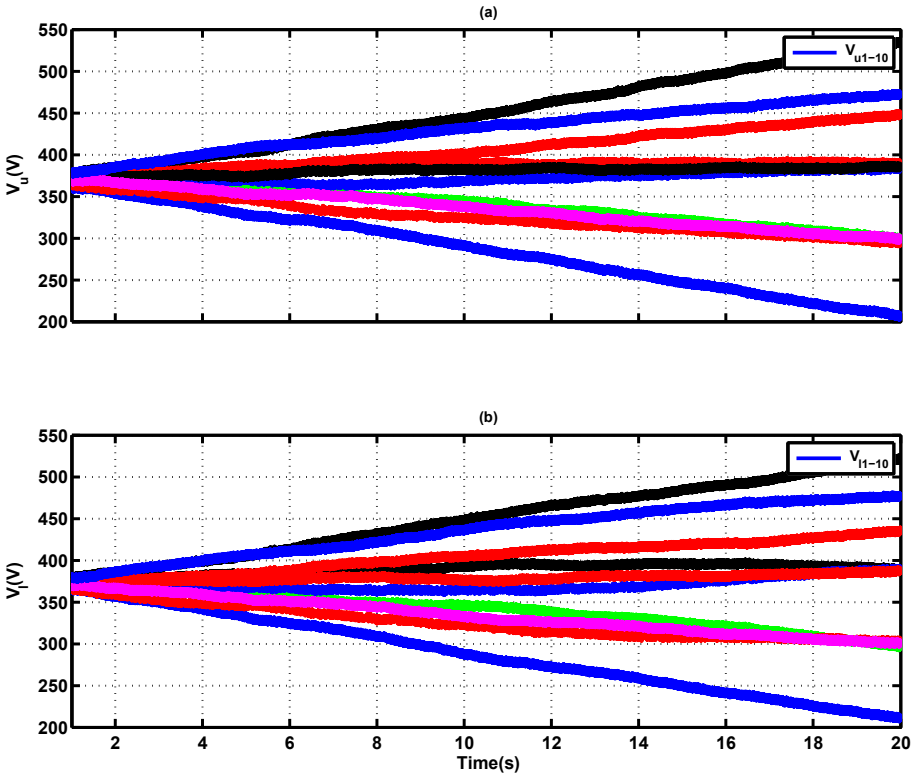


Figure 2.7: Simulated capacitor-voltage waveforms with PSC modulation at a switching frequency of 1950 Hz. The voltage waveforms of (a) upper arm capacitors, and (b) lower arm capacitors.

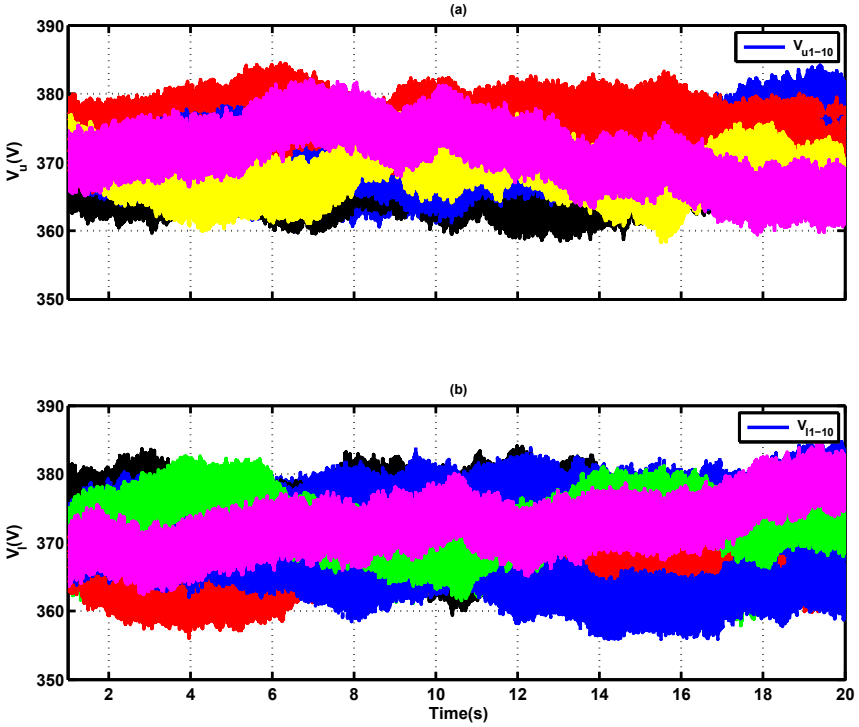
switching frequency are shown in Fig. 2.8(a), where the MMC is equipped with the proposed hierarchical PCC algorithm. In this case, the SMs capacitor voltages in the arm are bounded in a range that does not exceed 5% of the rated capacitor voltage. The proposed balancing unit balances the SM capacitor voltages during the steady-state condition. Fig. 2.8(b) demonstrates the dynamics of the capacitor voltages during a short time interval. It is found that the capacitor-voltage waveforms are stable during the steady state with the same peak-to-peak voltage ripple amplitude.

Fig. 2.9 shows the SM capacitor-voltage waveforms of the upper and lower arms when PSC modulation is employed at a switching frequency of 300 Hz. Because the switching frequency is an integer multiple of the fundamental frequency, the SM capacitor voltages gradually diverge from their nominal values.

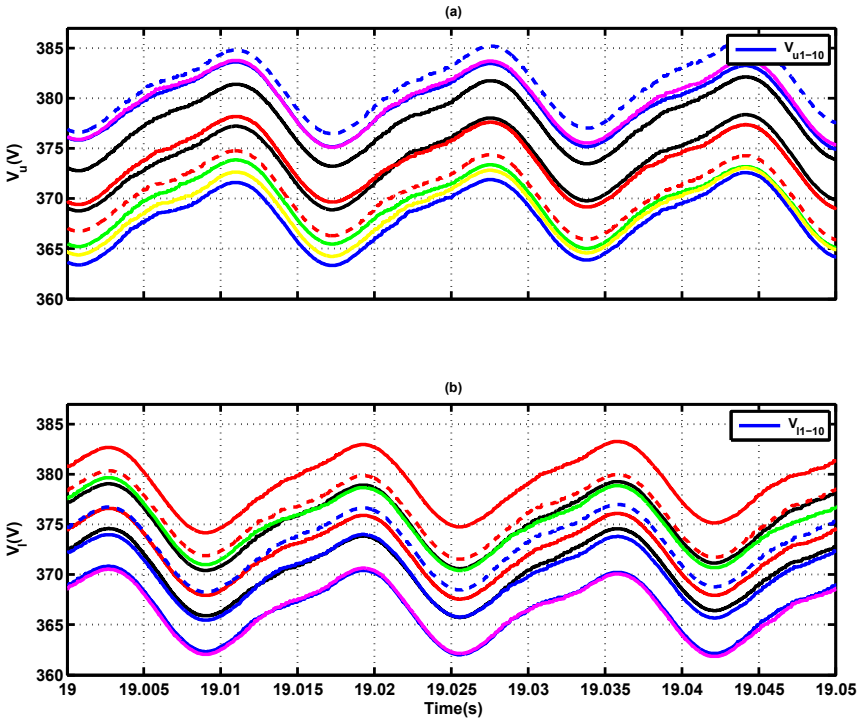
The SM capacitor-voltage waveforms of the upper and lower arms at the 300-Hz switching frequency when the MMC is equipped with the proposed hierarchical PCC algorithm are shown in Fig. 2.10(a). Similar to the previous cases with high switching frequencies, the capacitor voltage fluctuation in each SM is bounded in a very narrow band. The ripple amplitudes of the capacitor voltages are similar to the high-frequency cases. Fig. 2.10(b) shows the dynamics of the capacitor voltages during a short time interval. Because the utilization of SMs is the same over the permutation time period, the capacitor voltages are balanced with the same peak-to-peak capacitor voltage ripple amplitude.

2.3.2 Balanced and Unbalanced Load Conditions

Fig. 2.11 shows the system behavior under step changes in the load while the MMC is equipped with the proposed hierarchical PCC algorithm. The carrier frequency is set at 300 Hz–i.e., the integer multiple of the system frequency. The first step occurs at t=2 s, at which time the active power is step changed from 115 to 175



(a) Capacitor voltage waveforms of upper and lower arms.



(b) Capacitor voltage waveforms of upper and lower arms.

Figure 2.8: Simulated capacitor-voltage waveforms with the proposed hierarchical PCC algorithm at a switching frequency of 1950 Hz during (a) a long run; (b) a short time interval.

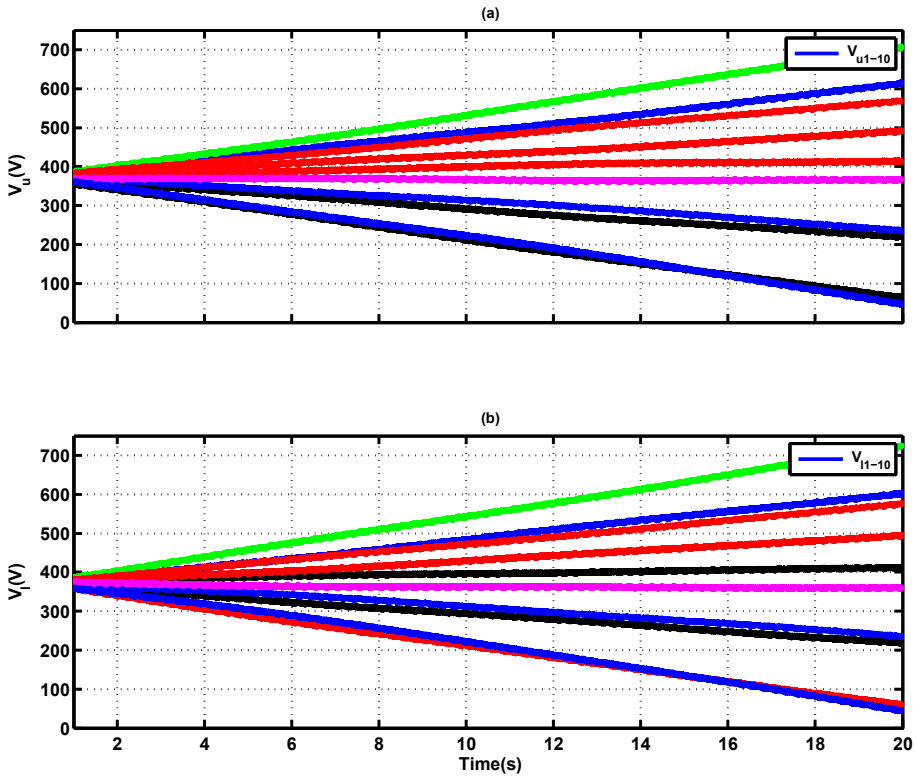
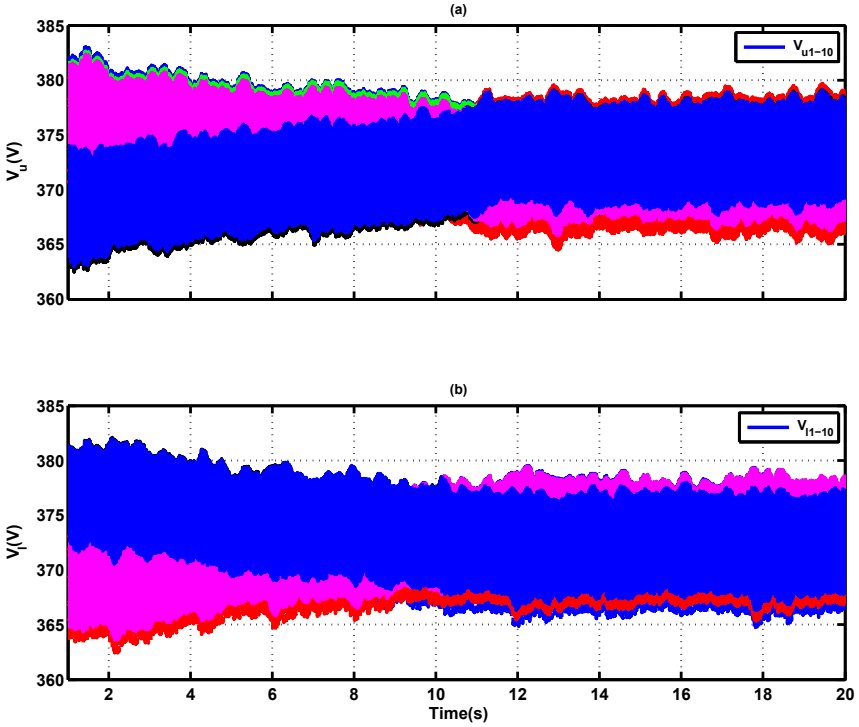
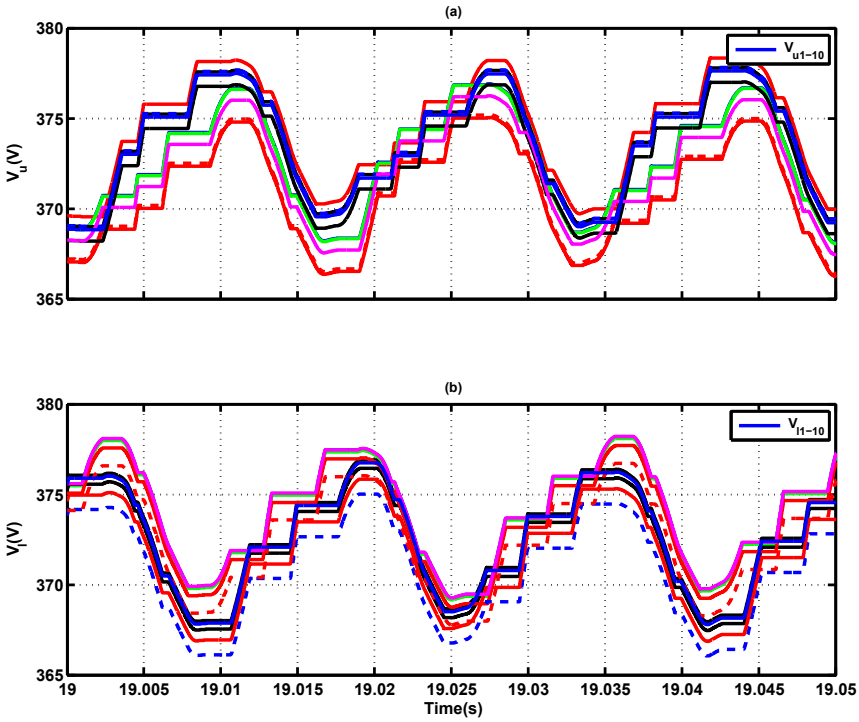


Figure 2.9: Simulated capacitor-voltage waveforms with PSC modulation at a switching frequency of 300 Hz. The voltage waveforms of (a) upper arm capacitors, and (b) lower arm capacitors.

kW. At the same time, the reactive power is step changed from 10 to 0 kVAr. The second step on the active and reactive powers is applied at t=2.5 s, at which time the active power is changed to 70 kW. At the same time, the reactive power is changed to 10 kVAr. The dynamic response to the changes in the active and reactive power references are represented in Fig. 2.11(a). Fig. 2.11(b) shows the upper and lower arms and circulating currents, in which the circulating current suppressing controller eliminates the double-frequency component of the circulating current very well. The output currents at the load side during step transient are shown in Fig. 2.11(c). It can be seen in Figs. 2.11(d) and (e) that although the step transient results in sudden disturbance of the system, the hierarchical PCC unit efficiently handles the capacitor voltage balancing under the new operation points.



(a) Capacitor voltage waveforms of upper and lower arms.



(b) Capacitor voltage waveforms of upper and lower arms.

Figure 2.10: Simulated capacitor-voltage waveforms with the proposed hierarchical PCC algorithm at a switching frequency of 300 Hz during (a) a long run; (b) a short time interval.

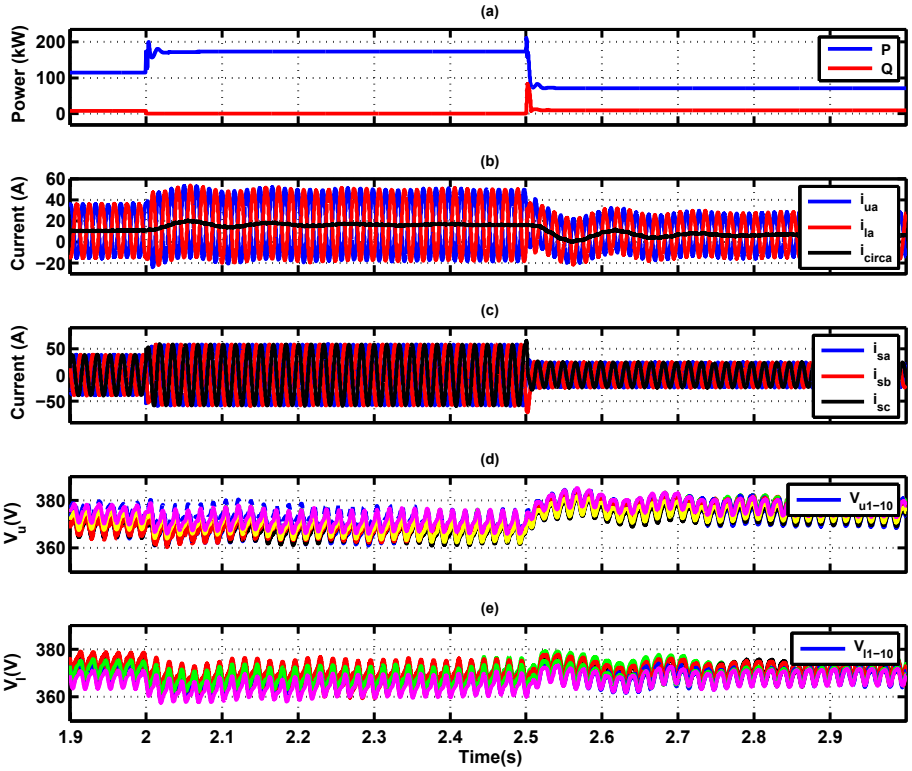


Figure 2.11: Simulation results when load power is step changed under balanced load conditions, (a) Load power (b) Arm currents and circulating current. (c) Output current at load side. (d) Voltage waveforms of upper arm capacitors. (e) Voltage waveforms of lower arm capacitors.

The system behavior when the system is step changed under an unbalanced load condition is shown in Fig. 2.12. The first step occurs at t=2 s, at which time the active power is step changed from 38 kW to 65, 69, and 60 kW in phases a, b, and c, respectively. At the same time, the reactive power is step changed from 3 to 0 kVAr on all three phases. The second step on the active and reactive powers is applied at t= 2.5 s, at which time the active power is changed to 33, 40, and 27 kW in phases a, b, and c, respectively. At the same time, the reactive power is changed to 2.5, 3, and 1.3 kVAr in phases a, b, and c, respectively. Fig. 2.12(a) shows that the active and reactive powers contain double-frequency ripple under an unbalanced load condition. The arm currents are well controlled. The double-frequency component of the circulating current is canceled out by using the circulating current suppressing controller. As

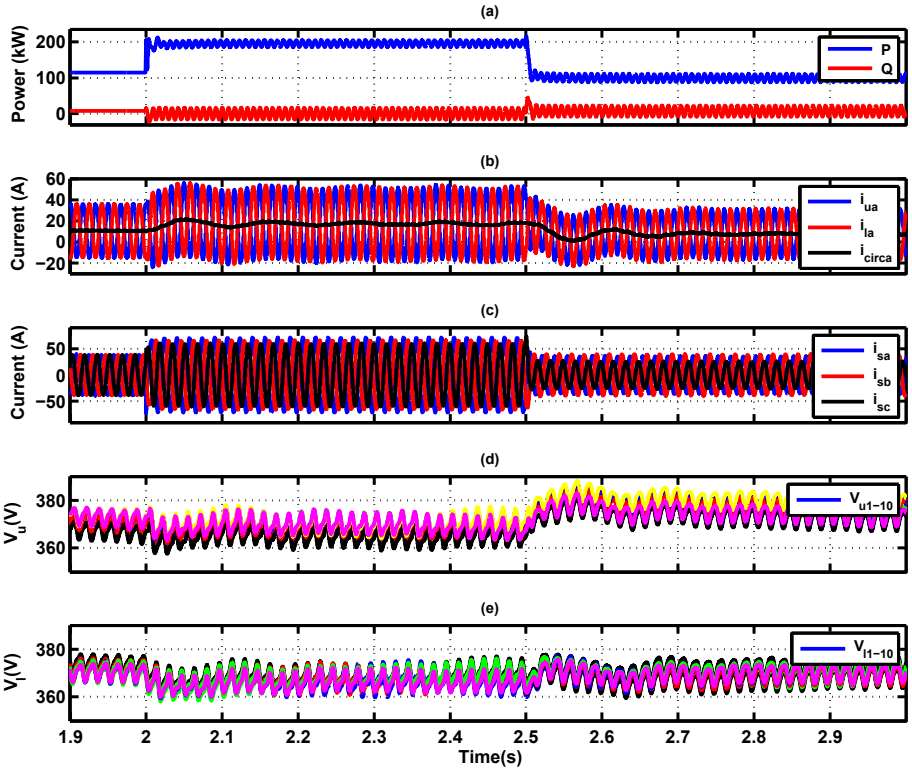
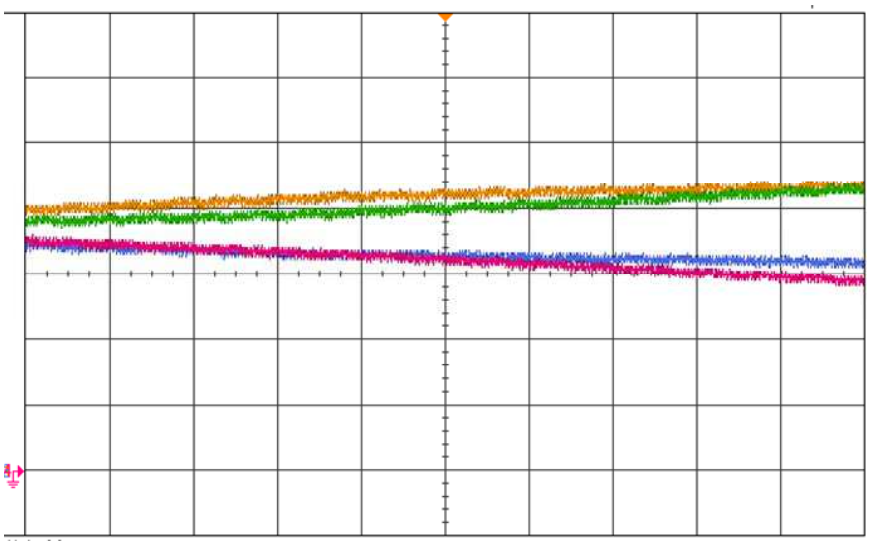


Figure 2.12: Simulation results when load power is step changed under unbalanced load conditions, (a) Load power (b) Arm currents and circulating current. (c) Output current at load side. (d) Voltage waveforms of upper arm capacitors. (e) Voltage waveforms of lower arm capacitors.

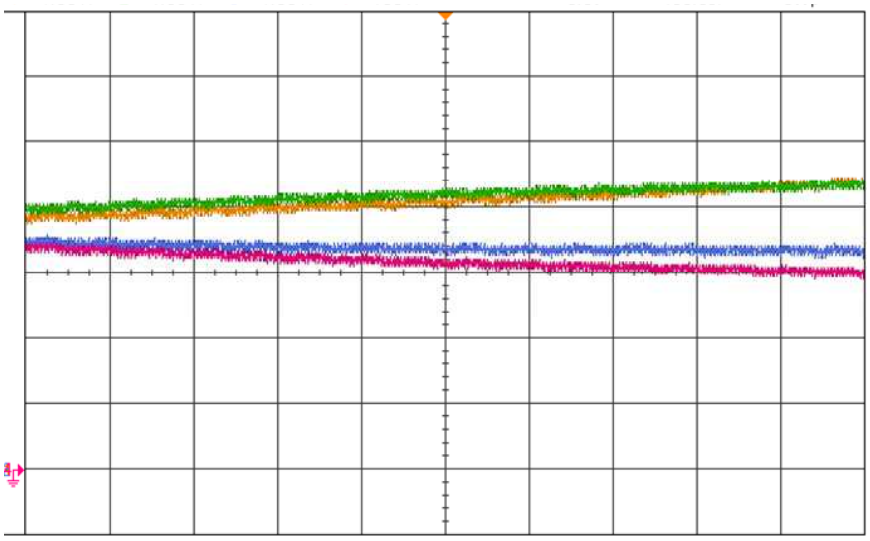
shown in Figs. 2.12(d) and (e), the hierarchical PCC unit efficiently handles capacitor voltage balancing and maintains good performance under unbalanced load conditions.

2.3.3 Hardware-in-the-Loop Verification Studies

The validity of the proposed strategy is verified by a hardware-in-the-loop setup based on the RT-LAB real-time simulation platform. The parameters of the test system are given in Table 2.2. The MMC controller is implemented in a Virtex-6 FPGA board with a cycle of 250 ns. The hierarchical PCC algorithm is implemented in the CPU with a time step of 50 μs. The switching frequency is 300 Hz, which is five times the fundamental frequency. The MMC measurements and commands are updated every 10 μs. Four SMs are randomly chosen and monitored to represent the individual



(a)



(b)

Figure 2.13: Capacitor-voltage waveforms with PSC modulation at a switching frequency of 300 Hz. Voltage waveforms of (a) upper arm capacitors, and (b) lower arm capacitors. (Time: 400 ms/div, channels 1-4:100 V/div)

capacitor voltages of SMs in the upper and lower arms.

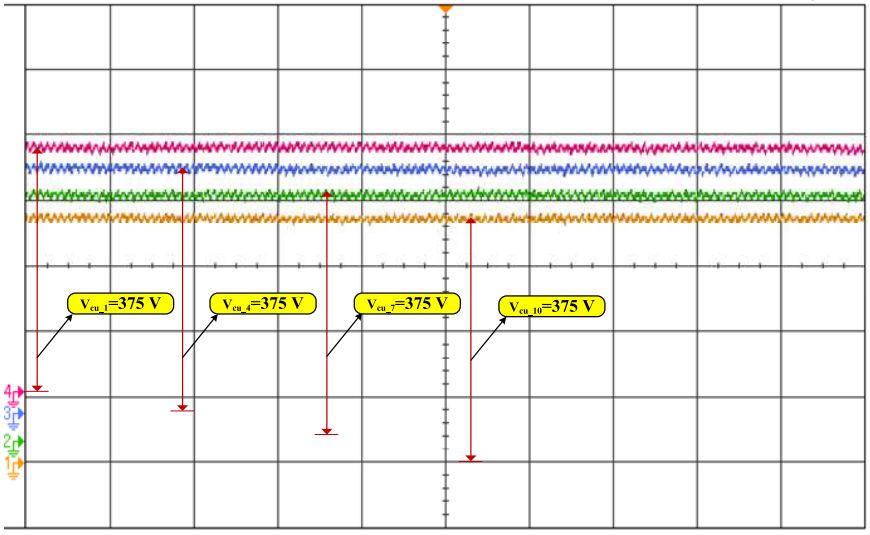
Fig. 2.13 shows the capacitor-voltage waveforms of four SMs (two of the upper arm and two of the lower arm in phase a). The SM capacitor voltages gradually diverge from their reference values because the switching frequency is an integer multiple of the fundamental frequency. Fig. 2.14 indicates the capacitor-voltage waveforms of

two SMs in the upper arm and two in the lower arm. The dc components of SM capacitor voltages follow their reference values. Fig. 2.15 shows the capacitor-voltage waveforms of the first and fourth SMs in the upper arm and the seventh and tenth SMs in the lower arm. The SM capacitor voltages are well balanced in a very narrow band that does not exceed 5% of the boundaries. The hardware-in-the-loop platform results are in excellent agreement with the simulation results.

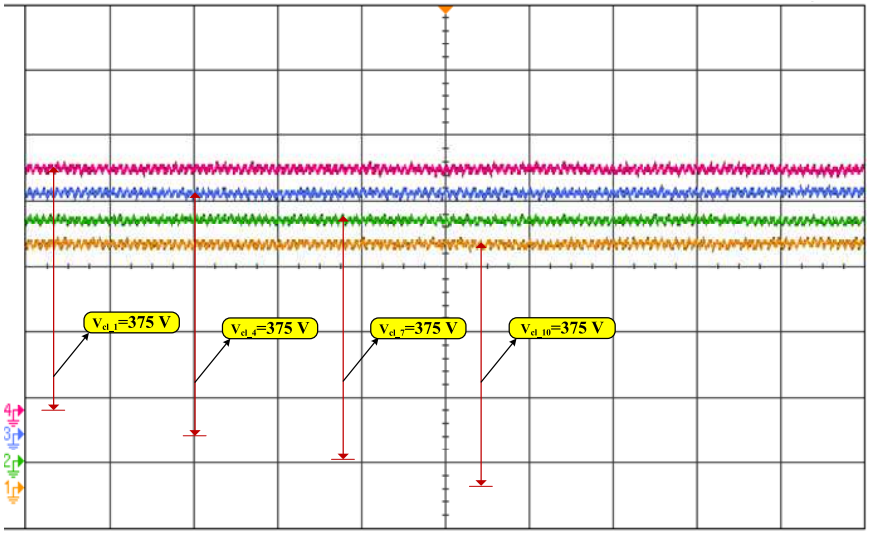
2.4 Conclusions

This chapter presents a simplified capacitor voltage balancing method in MMCs to effectively balance SM capacitor voltages in a wide range of switching frequencies. This method is realized by developing a hierarchical PCC algorithm to cycle the switching gate signals among the SMs of each arm. The balancing unit distributes the switching signal among SMs in such a way that the capacitor voltages converge to their reference values. The performance of the proposed strategy is investigated using digital time-domain simulation studies in the Matlab/Simulink platform. It is validated by an FPGA-based real-time simulator in a hardware-in-the-loop test bench to verify the main features of the proposed strategy.

The study results indicate the desired performance of the proposed framework to balance all SM capacitor voltages to track their reference values during steady-state conditions without diverging over time. The case study demonstrates 1) capacitor voltage fluctuation bounded within 5% of the rated capacitor voltage, 2) no additional hardware requirement, which enhances the reliability, computational resources, and simplicity of the system, and 3) decoupled control with no need for retuning of other control loops parameters. Most importantly, the scheme can be implemented for a wide range of switching frequencies and simply extended to MMCs with any number of levels.

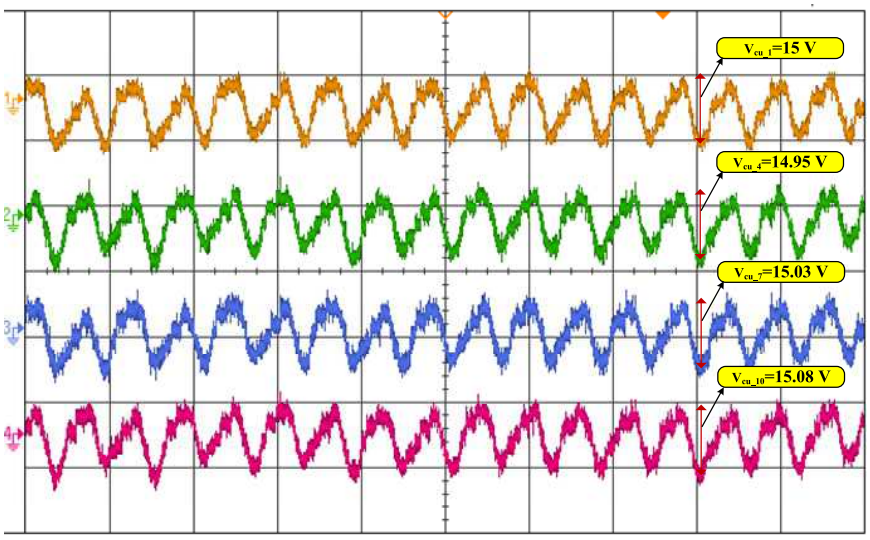


(a)

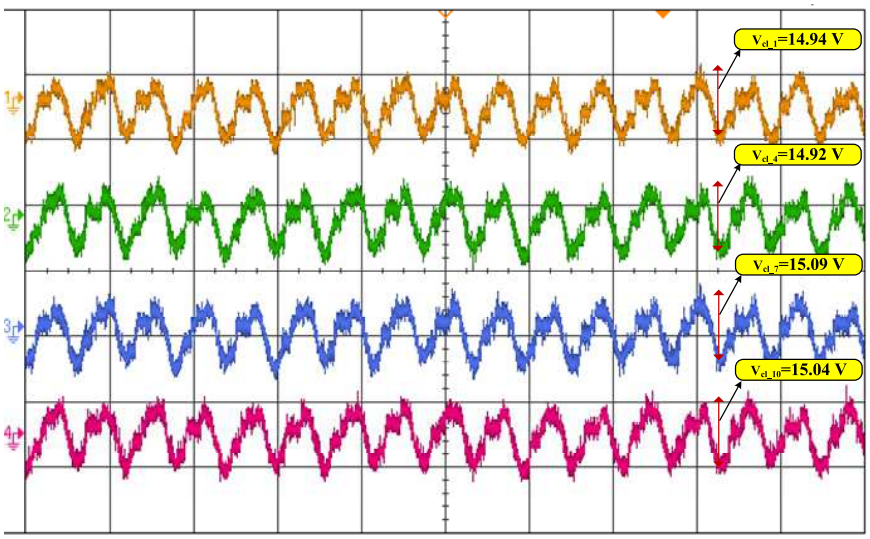


(b)

Figure 2.14: Capacitor-voltage waveforms with the proposed balancing unit at a switching frequency of 300 Hz. Voltage waveforms of (a) upper arm capacitors, and (b) lower arm capacitors. (Time: 200 ms/div, channels 1-4:100 V/div)



(a)



(b)

Figure 2.15: Capacitor-voltage waveforms with the proposed balancing unit at a switching frequency of 300 Hz during a short time interval. Voltage waveforms of (a) upper arm capacitors, and (b) lower arm capacitors. (Time: 28 ms/div, channels 1-4: 15 V/div)

Chapter 3

New SM Circuit for MMC in HVDC Systems

This chapter presents a new SM circuit to facilitate fault-tolerant capability for MMCs under various internal and external fault conditions. It can be simply integrated into conventional HB-based MMCs by using the switching signal adapter that also helps to attain the most efficient current path and inherent capacitor voltage balancing features. Furthermore, an extended version of the proposed SM circuit is developed to achieve a higher level of voltages.

3.1 Operation Principle of the Proposed Submodule Circuit

Fig. 3.1 shows the basic schematic diagram of a three-phase MMC. Each phase unit of an MMC consists of two arms, each includes a total of N identical SMs. The upper and lower arms are connected through one series inductor and resistor. The midpoint between two arms is the ac terminal location. Typically, each SM is an HB converter consisting of a dc capacitor and two complementary switches. The

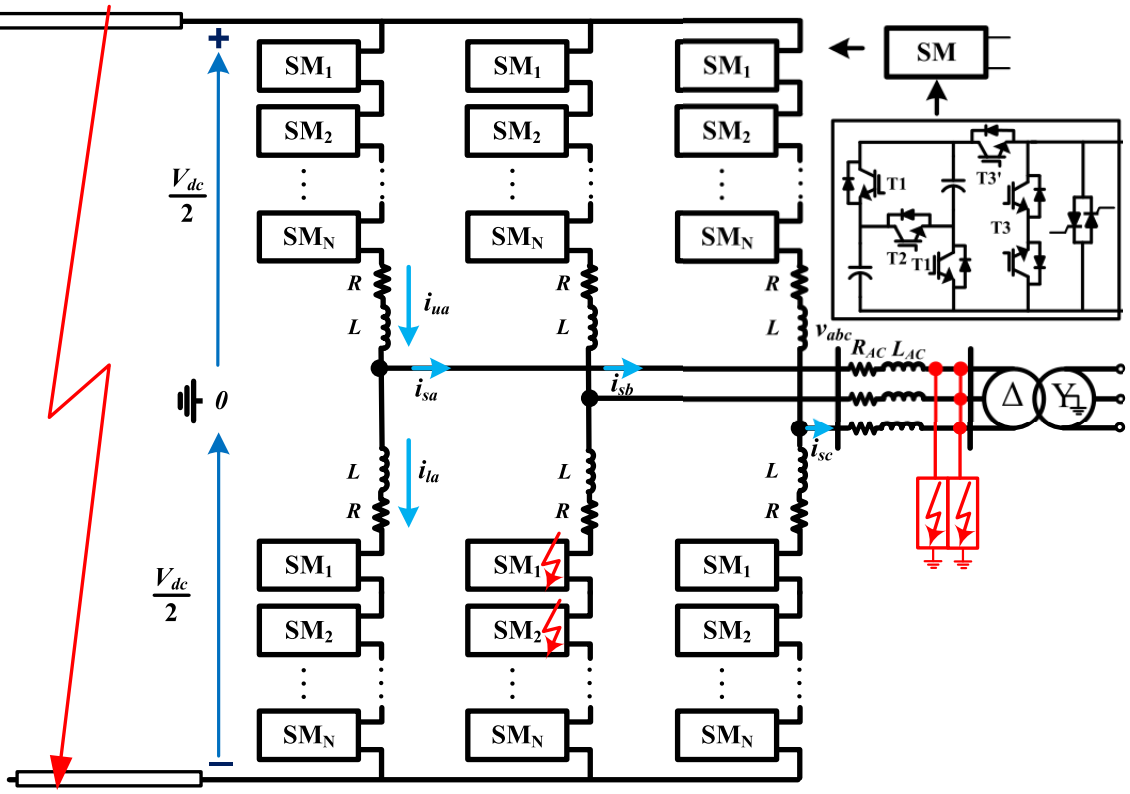


Figure 3.1: Basic schematic diagram of an MMC.

proposed SM in this Chapter operates similarly to two cascaded HB converters. The number of proposed SMs in the building block of the MMC equals half of the number of capacitors. Therefore, N series-connected SMs generate $2N + 1$ voltage levels in the ac-side terminal voltage, which the number of voltage levels is one more than the number of series-connected SM capacitors in each arm.

3.1.1 Submodule Topology

The HB SM output voltage only has two values in normal operation, which depends on the switching status and arm current direction. The switches in an HB SM are complementary, where only one switch at a time is allowed to be *on*. The output voltage will be the capacitor voltage when the upper switch in HB circuit is *on* or zero when the lower switch, S′, is *on*. The configuration of cascaded HB convert-

Table 3.1: Operation and Swithing States of The Proposed SM

T1	T2	T3	T3′	Arm current	V_{c1}	V_{c2}	Output voltage
1	0	0	1	>0	↑	↑	V_{c1} or V_{c2}
1	0	0	1	<0	↓	↓	V_{c1} or V_{c2}
0	1	0	1	>0	↑	↑	V_{c1}+V_{c2}
0	1	0	1	<0	↓	↓	V_{c1}+V_{c2}
0	0	1	0	>0	-	-	0
0	0	1	0	<0	-	-	0

ers, proposed SM, and the corresponding switching signal adapter unit are shown in Fig. 3.2. One of the salient features of the proposed SM is that the switching signals of HB-based MMC can be simply converted by using a switching signal adapter unit to generate the gating signals required for the proposed SM. This feature simplifies the implementation of the proposed SM in conventional HB-based MMCs. It also allows conventional MMCs to integrate the proposed SM circuit into their arms without a need for any change in control and modulation techniques.

As shown in Fig. 3.2, the switching signal adapter unit collects S1 and S2 as inputs and assigns the switching gate signal of the proposed SM by using a simple logic circuit. There are three possible operation modes for two series-connected HB SMs. When there is no HB SM in inserted mode, the switching signal adapter turns T3 *on* to bypass the proposed SM. If one of the series-connected HB SMs is inserted, the switching signal adapter unit employs a XOR gate to turn T1 and T3′ *on*. In this case, the capacitors in the proposed SM structure are in parallel. Accordingly, there is a parallel current path that contributes to the reduced output impedance of the circuit, enhanced efficiency, and inherent capacitor voltage balancing. The third possible mode happens when both HB SMs are inserted. In this case, the switching signal adapter unit turns T2 and T3′ *on* to insert both capacitors of the proposed SM circuit into the current path. It should be noted that T3 and T3′ are complementary switches. The detailed switching state of the proposed SM is illustrated in Table 3.1.

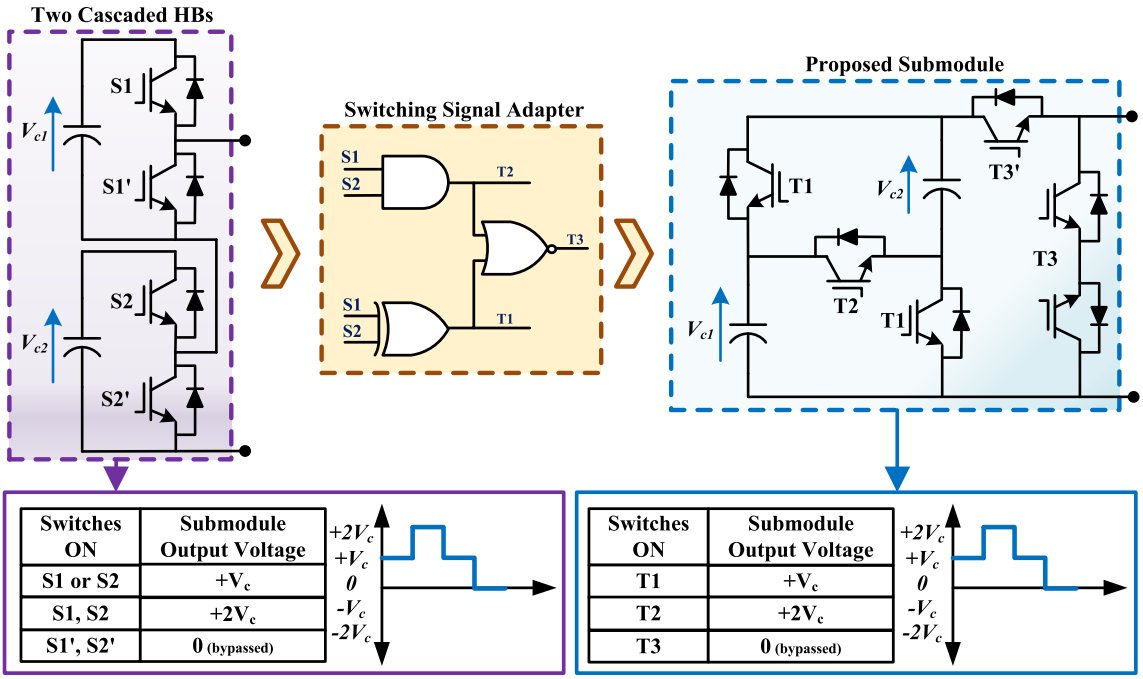


Figure 3.2: Circuit diagram and operation principles of HB and proposed SMs, including logic circuit for converting the switching signals.

3.1.2 Internal Fault Management Capability

The modularity feature of the proposed SM facilitates its integration at the intermediate nodes, generating the same voltage levels as that of two series-connected HB SMs. The proposed SM structure eliminates the need for two separated connection points and reduces the number of protective devices to one. In addition, one level of voltage of the proposed SM can be in reserved mode and added into the arm of the MMC if necessary. This process can be simply realized by changing switching status of T2. This redundancy feature of the proposed SM can enhance the robustness of the MMC and guarantee the uninterrupted performance of the system in case of internal fault conditions. The high current delivering ability and low output impedance are some of the key advantages of the proposed SM structure.

The switch open-circuit fault is one of the most common types of faults in SM structure. There are three potential types of switch open-circuit faults in HB-based

MMC topologies [25, 56]. All fault cases within the HB structure result in losing the SM capability to generate the expected voltage levels of 0 or V_c. However, the proposed SM demonstrates a superior performance in terms of internal fault management. The open-circuit fault in T1 makes the faulty SM incapable of generating voltage level V_c. However, the faulty SM still can operate as two-level SM capable of generating 0 and $2V_c$. In addition, the open-circuit fault in T2 makes the faulty SM incapable of generating voltage level $2V_c$. But, the faulty SM still can operate as two-level SM capable of generating 0 and V_c. Therefore, out of five possible single switch open-circuit faults in the proposed SM, the structure can be reconfigured in three of them to continue its operation with reduced voltage level.

3.1.3 Power Loss

The number of series-connected switches in the arm current path determines the conduction power losses of the MMC topology. In accordance with the building block of the proposed SM, the number of series-connected switches in the conduction path to generate 0, V_c, and $2V_c$ is 2, 3, 2, respectively. Therefore, the average number of switches in conduction path to generate three voltage levels is 2.33, and this number for the equivalent HB SM is 2. Although the proposed SM inserts one switch more in the conduction path in one of the states than the equivalent HB SM, the proposed SM reduces the need for protective thyristor from two to one. For FB circuit, the number of switches in conduction path to generate three levels of voltage is 4. It can be inferred that the semiconductor losses of the proposed SM are lower than the equivalent FB SM. Therefore, the MMC that adopts the proposed SM can closely retain the advantage of the HB-based MMC in terms of low power losses and full modularity of the power circuit.

3.1.4 Extension of Submodule Circuit

The proposed SM circuit has the capability of extending chain links to obtain the higher level of voltages. In order to generate a particular arm voltage level, specific number of capacitors in series should be inserted into the current path of the respective arm. Fig. 3.3 shows the block diagram of the extended version of the proposed SM that can support up to four voltage levels. Similar to the proposed SM, this structure can also be simply integrated into the HB-based MMC. The modularity allows incorporation of a redundant add-on cell into each SM to maintain complete system functionality even under multiple SM faults. The three series-connected HB SMs can be simply replaced by the proposed SM in Fig. 3.3(a) to take full advantage of the distinctive expansion feature of the proposed SM. Fig. 3.3(b) illustrates the gating signal conversion algorithm to convert the switching signals of three series-connected HB circuits to the extended version of the proposed SM. Assuming that S1, S2, and S3 represent the upper switches of three series-connected HB SMs and the capacitor voltages are kept balanced, the output voltage of the proposed SM in Fig. 3.3(a) is inspected for three different cases:

1) If one of the S1, S2, or S3 is *on*, the voltage across T3 is governed by the path through switches T3′, T1, and T5 and capacitor C1. Therefore, $v_{T3} = V_c$;
2) If two of the series-connected HB SMs are inserted, the voltage across T3 is governed by the path through switches T3′, T2, and T5 and capacitors C1 and C3. Hence, $v_{T3} = 2V_c$;
3) If S1, S2, and S3 are *on* at the same time, the voltage across T3 is governed by the path through switches T3′, T2, and T4 and capacitors C1, C2, and C3. Therefore, $v_{T3} = 3V_c$;
4) If all switches are off, the voltage across T3 is governed by the path through T3. then, $v_{T3} = 0$.

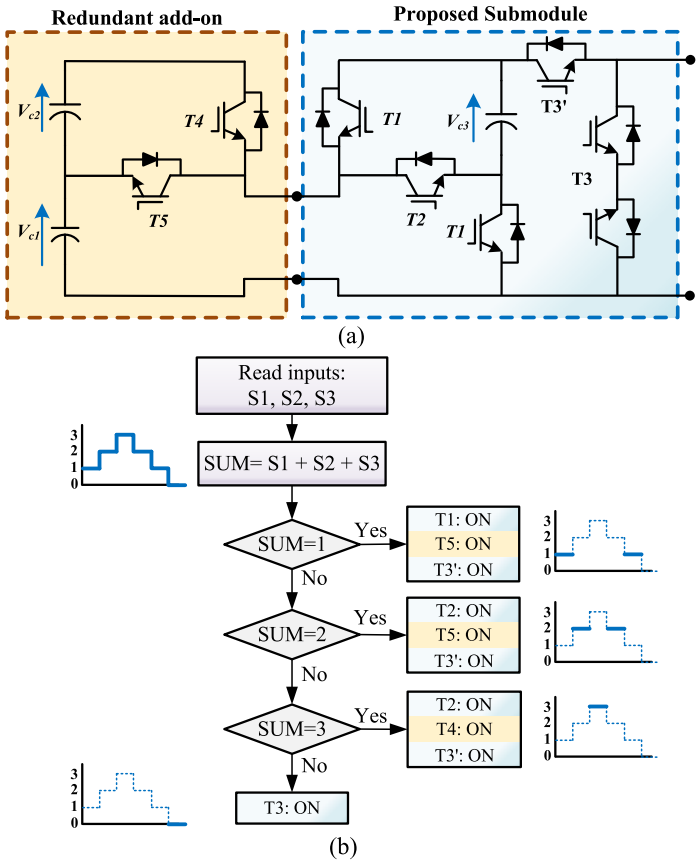


Figure 3.3: (a) Circuit diagram of the extended proposed SM that is equivalent to three series-connedted HB SMs. (b) Switching signal conversion algorithm for converting the switching signals of three series HB SMs to the extended version of the proposed SM.

The proposed SM circuit is compared with several efficient SM circuits in terms of power losses, fault-tolerant capability, and component requirement, listed in Table 3.2, to highlight the attributes of the proposed structure.

3.2 Operation Principle of the Modular Multilevel Converter

The internal dynamics of the MMC is defined by the circulating current and all capacitor voltages. The arm current of phase j is given by

$$i_{uj} = i_{cj} + \frac{i_j}{2} \tag{3.1}$$

Table 3.2: Comparison of Basic Converter Cell for MMC

Parameter	Cell topology						
	HB	FB	Clamp double	Flying capacitor	NPC	Cross connected	Proposed SM
No. of SMs per arm	2N	2N	N	N	N	N	N
Voltage levels	2N+1	2N+1	2N+1	2N+1	2N+1	2N+1	2N+1
No. of capacitors per arm	2N	2N	2N	3N	2N	2N	2N
No. of switches per arm	4N	8N	5N	4N	6N	8N	6N
No. of diodes per arm	4N	8N	7N	4N	6N	8N	6N
Max No. of switches in conduction path	2N	4N	6N	2N	2N	4N	3N
Symmetrical operation	No	Yes	No	No	No	Yes	No
Max reverse voltage per arm	-	Vdc	Vdc/2	-	-	Vdc	N/A

$$i_{lj} = i_{cj} - \frac{i_j}{2} \tag{3.2}$$

where the subscripts u and l refer to the upper and lower arms, respectively. i_j represents the converter line current of phase j. i_{cj} is the inner unbalanced current of phase j that contains the dc and even-order harmonic components. The dc component of the circulating current exchanges power between the dc-link and converter. The circulating current flowing through the upper and lower arms is expressed as

$$i_{cj} = \frac{1}{2}(i_{uj} + i_{lj}) \tag{3.3}$$

Therefore, the dynamics of the converter during normal operation are described as

$$L\frac{i_{cj}}{dt} + Ri_{cj} = \frac{V_{dc}}{2} - \frac{v_{lj} + v_{uj}}{2} \tag{3.4}$$

$$L\frac{i_j}{dt} + Ri_j = \frac{v_{lj} - v_{uj}}{2} - v_j \tag{3.5}$$

where R and L are the equivalent arm resistance and arm inductance, respectively. V_{dc} is the total dc-link voltage. The total output voltage of the upper and lower arms of phase j generated by the cascaded SMs is represented by v_{uj} and v_{lj}, respectively.

Once a dc fault occurs, it takes a short time to detect the fault and block the power switches of the MMC. The dc short-circuit fault current is mainly influenced by the

discharge of the SM capacitors in the conduction mode. Assuming that a pole-to-pole fault occurs in the dc link, the inserted voltages of each arm are given by

$$v_{uj} = -v_j - Ri_{uj} - L\frac{di_{uj}}{dt} + \frac{R_{sc}}{2}i_{sc} + \frac{L_{sc}}{2}\frac{di_{sc}}{dt} \tag{3.6}$$

$$v_{lj} = v_j - Ri_{uj} - L\frac{di_{lj}}{dt} + \frac{R_{sc}}{2}i_{sc} + \frac{L_{sc}}{2}\frac{di_{sc}}{dt} \tag{3.7}$$

where v_j is the ac-side voltage. R_{sc} and L_{sc} denote the short-circuit fault resistance and inductance including the impedance of the transmission line. By adding (3.6) and (3.7) for the three-phases and using (3.3), the dynamics of the fault current can be expressed as follows:

$$\sum (v_{uj} + v_{lj}) = (3R_{sc} + 2R)i_{sc} + (3L_{sc} + 2L)\frac{di_{sc}}{dt} \tag{3.8}$$

Subsequent to the dc fault occurrence, M series-connected capacitors in each phase immediately start discharging. The total short-circuit current is the sum of partial short-circuit currents in each of phase, that is derived as

$$i_{sc} = -\sum \frac{2C}{M}\frac{d(v_{uj} + v_{lj})}{dt} \tag{3.9}$$

where C represents the SM capacitor. By substituting (3.9) into (3.8), the characteristics of fault current before the fault detection time is deducted as

$$\frac{M}{6C}i_{sc} + (R_{sc} + \frac{2R}{3})\frac{di_{sc}}{dt} + (L_{sc} + \frac{2L}{3})\frac{d^2i_{sc}}{dt^2} = 0. \tag{3.10}$$

In HB-based MMCs, the freewheeling diodes function as uncontrolled rectifier bridges during dc faults. In addition, the diodes cannot solely manage the fault current and are subjected to thermal overstress. A parallel-connected thyristor with

diodes is a common practice to protect the diode from overcurrent [6]. In this type of architecture, the protection system heavily relies on the ac circuit breaker (ACCB) to trip in case of fault occurrence [5, 6]. Hence, in order to avoid the dc fault current path through freewheeling diodes, the intermediate connection node of the proposed SM is equipped with two switches in series pointing opposite directions. Furthermore, instead of using a single thyristor, double thyristor switches are employed to prevent the operation like uncontrolled rectifier bridges. The integration of bidirectional thyristor switches into the connection nodes of SMs helps to force the dc fault current to zero and extinguish the dc arc [89]. The thyristor switches are off during normal operation and are *on* during the dc fault occurrence. In the MMC equipped with bidirectional thyristor switches, a nonpermanent dc fault acts similar to an ac-side short circuit. During dc short-circuit fault, the ac current circulates through the MMC legs, and the dc current passes through RL branches in each arm. Accordingly, the dc fault current starts decaying to zero. Without the need for ACCB, the MMC can immediately rebuild the dc bus voltage subsequent to deblocking switching gate signals of all SMs switches and removing the gate signals for all thyristors.

3.3 Test Cases

In this section, the performance of the MMC that adopts the proposed SM is evaluated. Fig. 3.1 shows the MMC terminal of HVDC link with 50kV dc link voltage, connected to 138 kV ac grid through 35 MVA transformer. The three-phase 21-level MMC-HVDC transmission system with the SMs designed in Section 3.1.1 is established in Matlab/Simulink, and the system parameters are listed in Table 3.3. The proposed SM in Section 3.1.4 is integrated into each arm of the MMC to provide redundancy in case of internal malfunction and to guarantee the smooth fault transition and resilient system operation. The proposed MMC topology is modeled using a

Table 3.3: Circuit Parameters of MMC-HVDC

Parameter	Value
Converter nominal power	30 MVA
AC system nominal voltage	138 kV
Transformer ratio	138 kV/30 kV (Y/Δ)
Line frequency	60 Hz
AC-side inductance	5 mH
AC-side Resistance	0.03 Ω
DC-link voltage	50 kV
Number of submodules per arm	10
Arm inductance	8 mH
Arm equivalent resistance	0.3 Ω
Submodule capacitance	9 mF

detailed switch model, where there are 10 SMs including 20 capacitors per arm, and each SM capacitor voltage is rated at 2500 V.

The control objectives including control of active and reactive powers, fundamental voltage/current, circulating current, and individual capacitor voltage balance are met similar to that in [20, 21]. The hierarchical PCC modulation technique in [90] is adopted in the studied system to balance SM capacitor voltages. The rectifier station regulates the dc-link voltage and reactive power input to the converter. The command references of the dc-link and reactive power are set 50 kV and 0 MVar, respectively. The dc-link voltage is well regulated at 50 kV. The MMC in the inverter station controls the active and reactive power inputs to the converter. The command references of active and reactive power are set -20 MW and 0 MVar, respectively. Four simulation case studies are designed to validate the performance of the proposed MMC topology considering multiple SM failures, dc short-circuit fault, single-line-to-ground grid fault, and symmetric grid fault.

3.3.1 Case 1: Multiple Submodule Failures

The performance of the MMC-HVDC system in response to multiple SM failures at t = 0.5 s is shown in Fig. 3.4. An open-circuit fault happens at T3′ in SM_9 of lower arm

in phase b. Subsequent to the failure of T3′ in SM_9, its capacitor voltages cannot track their reference values. Simultaneously, an open circuit failure of T1 in SM_{10} occurs, which results in the loss of a voltage level. The MMC fault identification method in [25] is employed to immediately isolate the faulty SMs and insert the redundant SM to compensate for the lost voltage levels.

Fig. 3.4(a) shows the dynamics of the active and reactive power waveforms during the SM failure. During the switch open-circuit fault, when the arm current is positive, the capacitor voltages of faulty SMs are charged depending on the switching gate signals. Therefore, the capacitor voltages of the faulty SM_9 start increasing and deviating from the capacitor voltages of the healthy SMs in phase b. Once the faulty SM_9 is bypassed, two voltage levels are lost in the corresponding arm. In addition, another voltage level is lost due to the open circuit fault of T1 in SM_{10}. Accordingly, subsequent to identification and isolation of the faulty SMs at $t = 0.58$ s, the proposed SM in Section II-D in reserved mode is inserted to provide three lost voltage levels in the affected arm. The dynamic response of the SM capacitor voltages of the upper and lower arms is shown in Fig. 3.4(b) and (d). A comparison between the capacitor voltages of the healthy and faulty SMs in each arm indicates that the capacitor terminal voltage of faulty SMs keeps increasing after the fault occurrence.

The voltage and current waveforms on the ac side demonstrate that the system strongly maintains its performance under multiple SM failures. It can be inferred that the circulating current is quickly increased after SM failures. Consequently, the upper and lower arm current waveforms indicate a small increase in their magnitude in accordance with the change in the circulating current waveform, as shown in Fig. 3.4(f). Once the redundant SM is integrated into the affected arm, the system is restored to the normal operation state. This case result indicates that the MMC that adopts the proposed SM can safely handle the failure of multiple SMs in a very

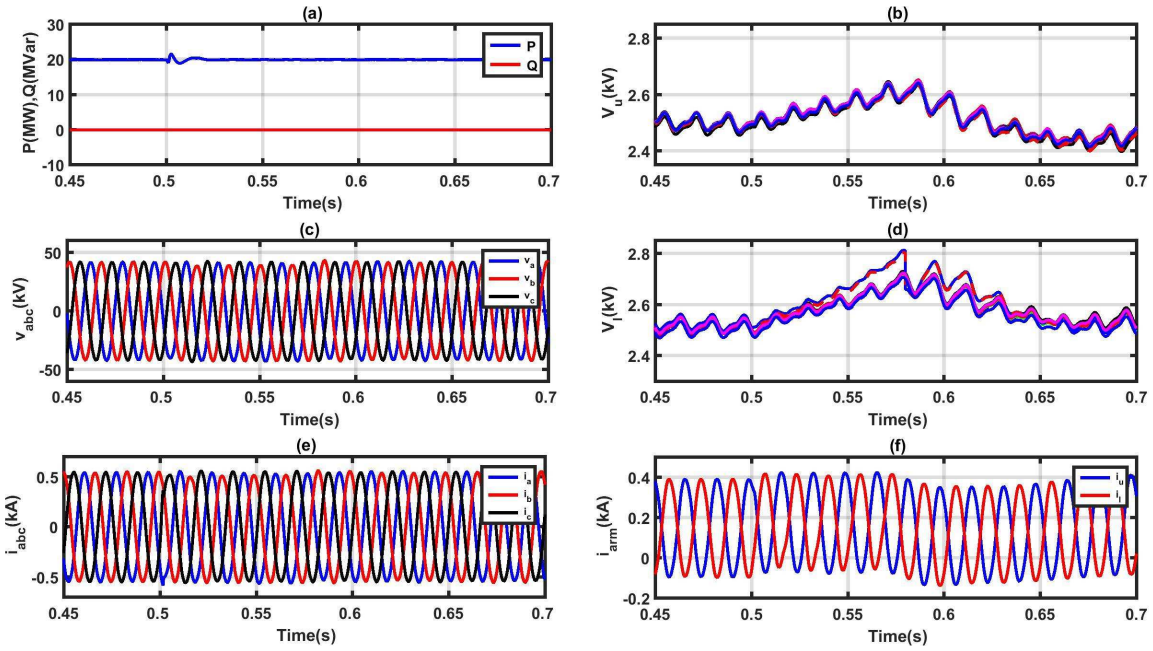


Figure 3.4: Dynamic response of the MMC-HVDC system with the proposed SMs once multiple SM failures occur. (a) Active and reactive power exchanges with the ac grid. (b) SM capacitor voltages of the upper arm of phase b. (c) AC-side voltage. (d) SM capacitor voltages of the lower arm of phase b. (e) AC-side current. (f) Arm currents of phase b.

short time.

3.3.2 Case 2: DC short-circuit fault

Fig. 3.5 demonstrates the study results of the MMC-HVDC system with the proposed SM under pole-to-pole dc short-circuit condition. The MMC adopts double thyristor switches allowing the dc fault current starts to decay. The converter station is injecting the active power of 20 MW into the ac grid under normal operation. The upper and lower arm voltages are well-balanced, and both arm currents are well-controlled during normal operation. According to the arm current waveforms, the controller effectively suppresses the oscillatory component of the circulating current. A nonpermanent pole-to-pole dc short-circuit fault is imposed at $t = 1.5$ s and cleared after 0.15 s. Subsequent to the fault occurrence, the active power transfer from the converter station into the grid immediately drops down to zero, as shown in Fig. 3.5(a).

Once the fault is detected, the detection algorithm blocks the gating signal of all switches within the MMC and turn on all bidirectional thyristors. During the fault period, the SM capacitor voltages are maintained at their nominal values as a flat value, as demonstrated in Fig. 3.5(b) and (d). It can be inferred that the current in the dc-link has dropped to zero when the converter is blocked, and there is no discharge of the SM capacitors. When the dc voltage drops to zero subsequent to the dc short-circuit fault, the ac grid starts feeding ac short-circuit current through the upper and lower arm. It can be inferred from Fig. 3.5(e) and (f) that the dc fault current decays to zero. Accordingly, there is no power exchange with grid during the fault period. After the fault clearance, the protection scheme turns off all thyristor switches to assist the MMC to rebuild the dc bus voltage. Then, the switching gate signals of all SMs switches are unblocked to permit the MMC to restore its normal operation. The results show that the system quickly recovers after the fault clearance.

3.3.3 Case 3: Single-Line-to-Ground Fault

A single-line-to-ground fault at the primary side of the Y-grounded/Δ transformer in phase b of the inverter station occurs at time $t = 2$ s, lasting for 0.15 s. This type of fault may occur due to poor connection or insulation damage. Simulation waveforms of the studied system under a single-line-to-ground fault, as a severely unbalanced condition, are shown in Fig. 3.6. The single-line-to-ground fault significantly introduces a zero-sequence component in phase current. Under unbalanced conditions, ground currents can be formed by the flow of zero sequence current into the ac grids. The increase in the number of SMs per arm can eliminate the need for a transformer, which contributes to higher flexibilities in the circuit configuration and noticeable reduction in cost. On the other hand, a transformerless MMC-HVDC system must integrate a zero-sequence controller into the control system to guarantee asymmetrical-fault ride-through capability, which may increase the complexity of the

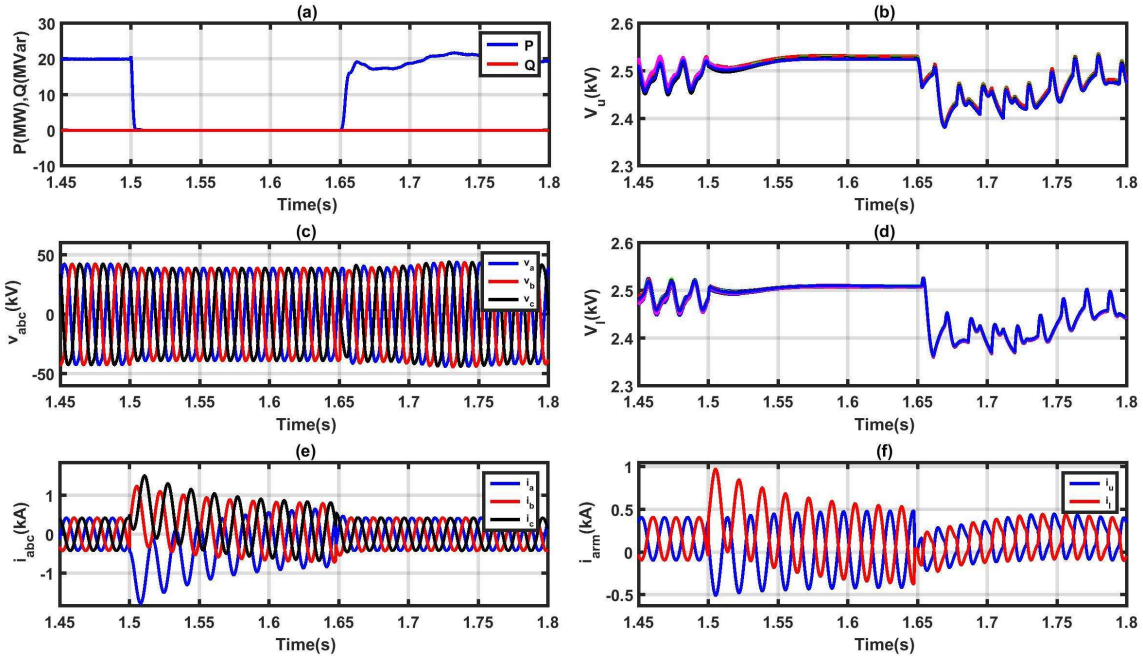


Figure 3.5: DC short-circuit fault handling of the MMC-HVDC system with the proposed SMs. (a) Active and reactive power exchanges with the ac grid. (b) SM capacitor voltages of the upper arm of phase b. (c) AC-side voltage. (d) SM capacitor voltages of the lower arm of phase b. (e) AC-side current. (f) Arm currents of phase b.

control system. In the system under study, the zero sequence current is blocked from flowing into the converter side by using a transformer with delta connection.

Fig. 3.6(a) shows the active and reactive power waveforms of the MMC during the fault, where the double-line-frequency ripples appear in the power waveforms. Based on the internal dynamics of the MMC, the single-line-to-ground fault in phase b mainly impacts the SM capacitor voltages and arm currents of the affected leg. The SM capacitor voltages in the upper and lower arms in phase b are illustrated in Fig. 3.6(b) and (d). The SM capacitor voltages of both upper and lower arms are regulated and well balanced around their reference values. The magnitude of the SM capacitor voltage ripples increases during the single-line-to-ground fault because of highly unbalanced ac current. Fig. 3.6(c) and (e) illustrate the three-phase voltage and current waveforms at the Δ-side of the converter transformer. In the presence

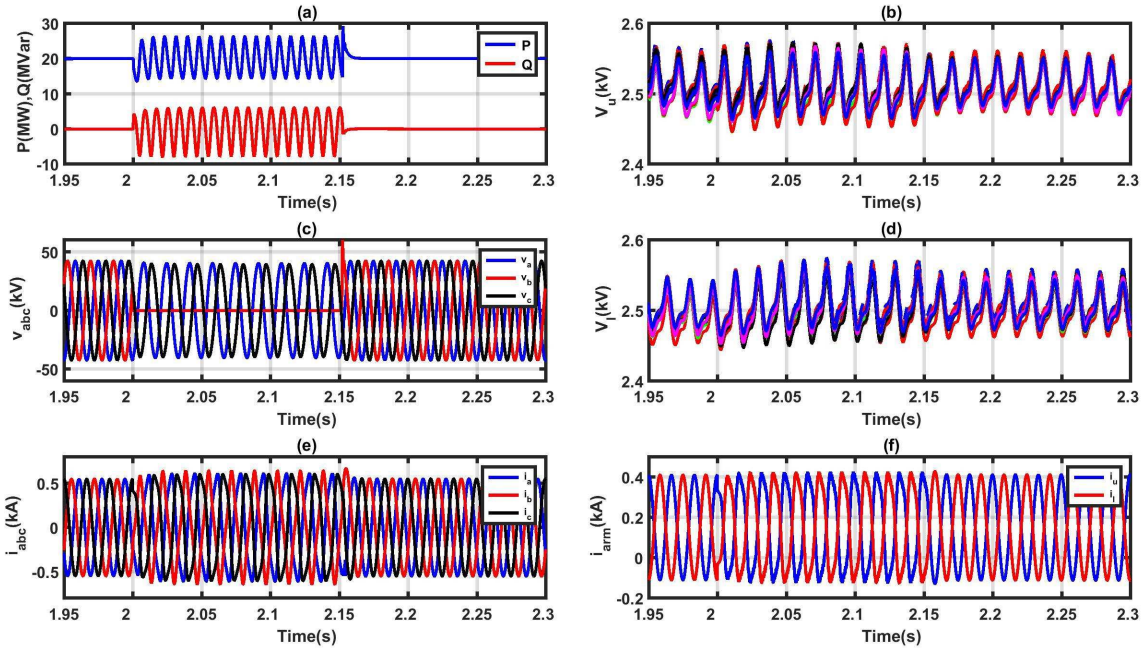


Figure 3.6: Fault-tolerant operation of the MMC-HVDC system with the proposed SMs under single-line-to-ground fault. (a) Active and reactive power exchanges with the ac grid. (b) SM capacitor voltages of the upper arm of phase b. (c) AC-side voltage. (d) SM capacitor voltages of the lower arm of phase b. (e) AC-side current. (f) Arm currents of phase b.

of negative-sequence current components, the three-phase current waveforms show a degree of unbalance during the fault. It can be seen that there is an increase in the positive-sequence current components during the fault period. Accordingly, as shown in Fig. 3.6(f), the upper and lower arm currents and ac-side three-phase currents show a higher magnitude during the fault occurrence as compared to normal operation.

3.3.4 Case 4: Symmetrical Grid Fault

Fig. 3.7 shows the performance of the MMC-HVDC system that adopts the proposed SMs in response to the three line-to-ground fault. During the fault interval from $t = 3$ s to $t = 3.15$ s, the ac side voltages collapse to zero, and as a result, the delivered active power to the grid drops to zero. Fig. 3.7(b) and (d) show the SM capacitor voltages in the upper and lower arms in phase b. Once the fault occurs, the stored energy in the dc-link starts to increase. Accordingly, the proposed SM capacitor voltages in the

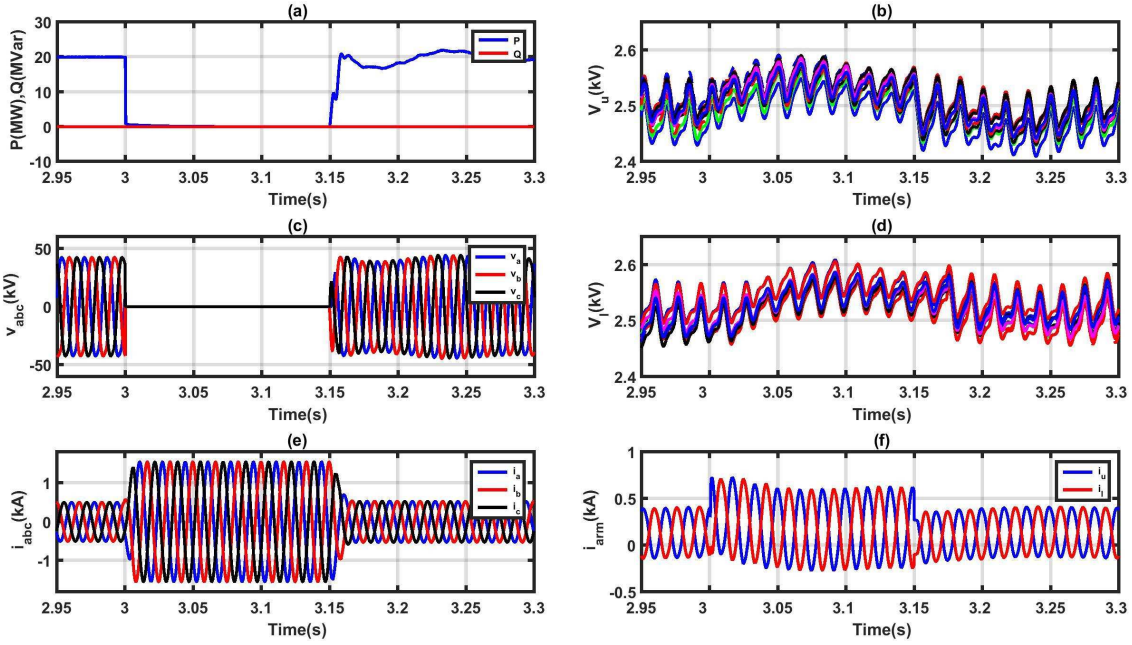


Figure 3.7: Fault-tolerant operation of the MMC-HVDC system with the proposed SMs under three line-to-ground fault. (a) Active and reactive power exchanges with the ac grid. (b) SM capacitor voltages of the upper arm of phase b. (c) AC-side voltage. (d) SM capacitor voltages of the lower arm of phase b. (e) AC-side current. (f) Arm currents of phase b.

upper and lower arms ramp up in response to the fault occurrence. After the fault clearance, the voltage balancing control unit balances the SM capacitor voltages at their reference value. Fig. 3.7(e) demonstrates the three-phase currents that cannot exceed 1.5 p.u. according to the predefined current limits. The ac components of the upper and lower arm currents are controlled based on the internal dynamics of the MMC, as shown in Fig. 3.7(f). The obtained results indicate that the MMC maintains the SM capacitor voltages balanced and effectively handles the three line-to-ground fault.

3.3.5 Hardware-in-the-Loop Validation Studies

This section presents the real-time performance of the MMC with the proposed SM in a hardware-in-the-loop setup. The test parameters listed in Table 3.3. Control, modulation, and capacitor voltage balancing units are programmed in three parallel

cores in the OPAL-RT OP5600 platform with a clock speed of 3.46 GHz. The data acquisition and I/O management are performed by using Virtex-6 FPGA chips with time steps as low as 290 ns. The hardware-in-the-loop studies demonstrate the MMC internal dynamics subsequent to multiple SM failures, dc fault, asymmetrical grid fault, and symmetrical grid fault.

Fig. 3.8 shows the dynamic response of the MMC-HVDC system in the hardware-in-the-loop setup when two simultaneous SM open-circuit faults occur. Due to the nature of the switch open-circuit fault, the capacitor voltages of faulty SMs start increasing and deviate from the capacitor voltages of healthy SMs in the corresponding leg, as can be seen in the SM capacitor voltages waveforms. In addition, the circulating and arm currents cannot accurately track their reference values after the occurrence of the SM failures. Once the capacitor voltages exceed a predefined threshold, the faulty SMs are identified to be isolated from the arm. Subsequent to fault isolation, the proposed three-level SM receives the gating signal of the isolated faulty SMs. The switching signal adapter unit provides the gating signal for the reserved SM to compensate for the lost three levels of the arm voltage.

The hardware-in-the-loop performance of the MMC-HVDC system under the pole-to-pole dc short-circuit fault is illustrated in Fig. 3.9. The MMC-HVDC system that adopts the proposed SM handles the dc fault and maintains the SM capacitor voltages balanced before and after the dc fault occurrence. The dynamic responses of the system in the hardware-in-the-loop setup during asymmetrical and symmetrical grid faults are shown in Figs. 3.10 and 3.11, respectively. The proposed SM capacitor voltages precisely track their reference values before and after grid faults. The capacitor voltages of the upper and lower arms duly operate to balance the energy between the arms. In addition, the switching signal adapter effectively assigns gating signals to help to keep SM capacitor voltages balanced. The hardware-in-the-loop results verify

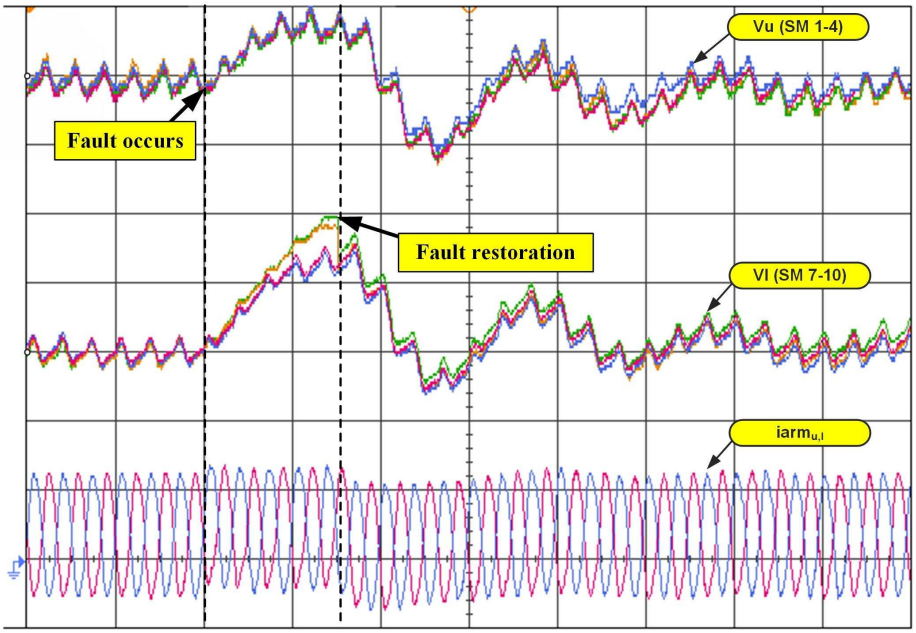


Figure 3.8: Dynamic response of the MMC during two SM failures in phase b. [Time: 50 ms/div, V_u: (SM 1-4): 100 V/div, V_l: (SM 7-10): 100 V/div, $i_{arm_{u,l}}$: 300 A/div].

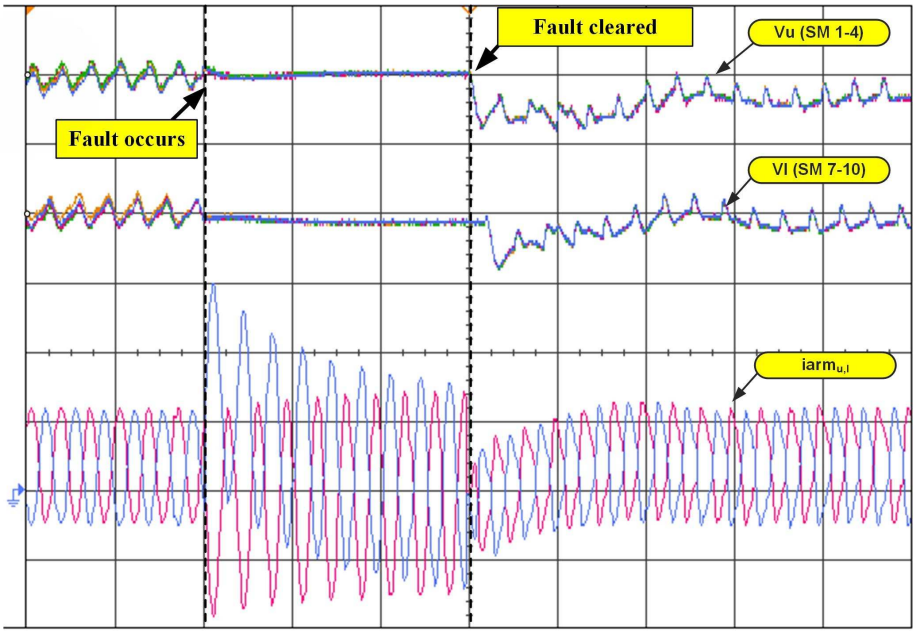


Figure 3.9: Dynamic response of the MMC during dc short circuit fault. [Time: 50 ms/div, V_u: (SM 1-4): 100 V/div, V_l: (SM 7-10): 100 V/div, $i_{arm_{u,l}}$: 300 A/div].

the theoretical analysis and are in close agreement with the simulation results.

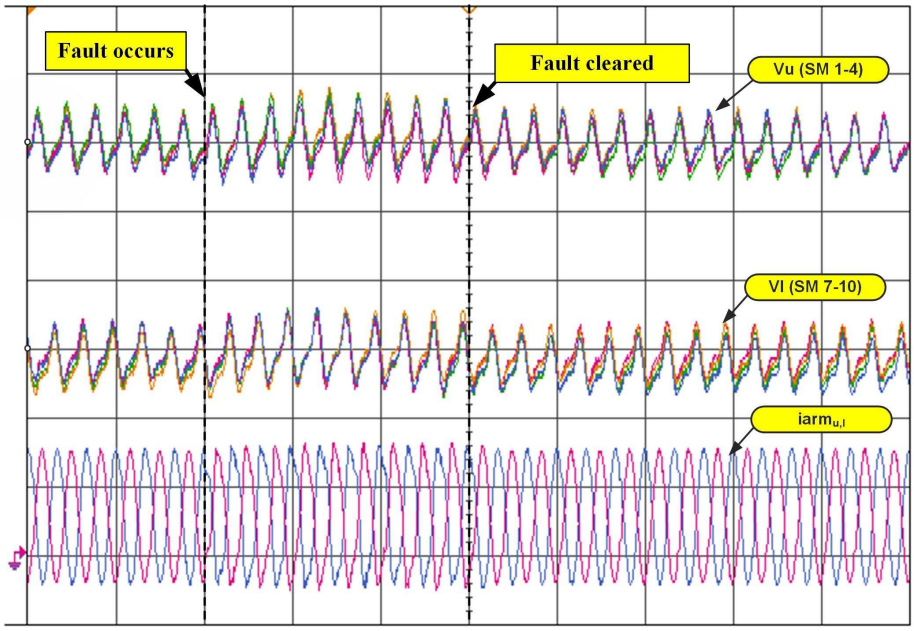


Figure 3.10: Dynamic response of the MMC during single-line-to-ground fault. [Time: 50 ms/div, V_u: (SM 1-4): 100 V/div, V_l: (SM 7-10): 100 V/div, $i_{arm_{u,l}}$: 300 A/div].

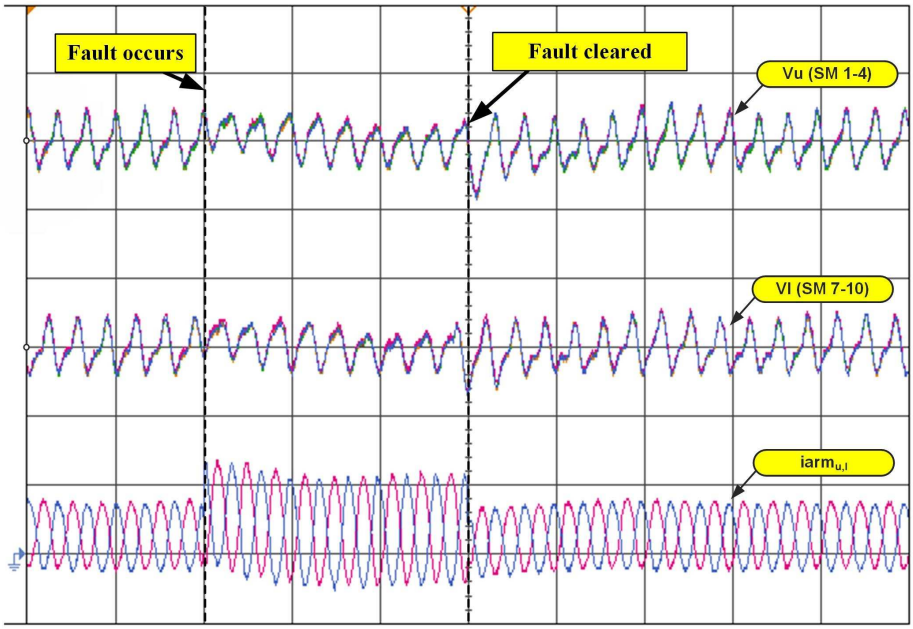


Figure 3.11: Dynamic response of the MMC during three line-to-ground fault. [Time: 50 ms/div, V_u: (SM 1-4): 100 V/div, V_l: (SM 7-10): 100 V/div, $i_{arm_{u,l}}$: 500 A/div].

3.4 Conclusion

This chapter presents a new SM circuit that facilitates fault-tolerant capability for MMCs under different internal and external fault conditions. A switching pattern

adapter is developed to simplify the implementation of the proposed SM in conventional HB-based MMCs. The configuration, operation principle, and gating signal pattern of an MMC that adopts the proposed SM are analyzed in detail. The performance of the MMC-HVDC system that adopts the proposed SM is investigated using digital time-domain simulation studies. The hardware-in-the-loop results confirm the viability of the proposed SM at device and system levels.

The study results indicate the MMC equipped with the proposed SM offers features including full modularity, low power losses, and ease of expandability. It can be reconfigured to continue its operation under some switch open-circuit fault conditions without a need for any mechanical bypass. It also enables easy incorporation of redundant cells into each SM to ensure reliable operation of the MMC-HVDC systems and obtain a higher level of voltages.

Chapter 4

Resilient Fault-Tolerant Strategy

This chapter presents an effective fault-tolerant strategy to detect fault occurrence, identify the location of the faulty component, and restore the system in a very short time. After detection and identification, the postfault restoration scheme replaces the faulty SM with the redundant one. This process adjusts the switching gate signals to minimize the impact of the failure on overall system performance.

4.1 System Operation Under Fault Conditions

One phase leg of an MMC is shown in Fig. 4.1. One of the potential problems in an MMC is SM malfunction, which can have an extreme transient impact on the system. Hence, some redundant SMs, initially operating in the bypass mode, are integrated into each arm of the MMC. The HB converter and the proposed SM are utilized, respectively, as SMs and redundant SMs in order to achieve fully modular topology. This design enhances the robustness and resiliency of the MMC and assures the uninterrupted and unchanged performance of the system.

The two most common types of faults in SMs are short- and open-circuits of

Table 4.1: Operation of a Faulty SM

Fault Type	T_i	T_i'	Arm current	Capacitor	Output voltage
I	O.C.	Healthy	Positive	$C \uparrow$	$S_i V_{cu}$
			Negative	Bypass	0
II	Healthy	O.C.	Positive	$C \uparrow$	V_{cu}
			Negative	$C \downarrow$	$S_i V_{cu}$
III	O.C.	O.C.	Positive	$C \uparrow$	V_{cu}
			Negative	Bypass	0

power-switching semiconductors. The protection devices restrain short-circuit faults to keep the power flow in the corresponding arm steady. Usually, an additional switch is implemented between the two output terminals of the SMs to bypass the faulty one [53, 56]. This chapter investigates various types of open-circuit faults in MMCs. The three types of open-circuit faults which may occur in the switching devices of an SM are shown in Table 4.1. When an open-circuit fault occurs in one of the switches, the anti-parallel diode continues working [27, 91–94]. Hence, a comparison between the capacitor voltages of the healthy and faulty SMs in each arm indicates that the capacitor terminal voltage of faulty SMs will keep increasing whenever a fault occurs. Generally, this increase occurs for all three types of the open-circuit fault. The dynamics of the capacitor voltage of the faulty SM depend mainly on the type of open-circuit fault. Accordingly, the rate of divergence of the capacitor voltage of the faulty SM from the nominal value is different for each fault type. In this research, the mentioned characteristic is utilized to effectively extract the fault feature and identify the fault type.

4.2 Fault Detection and Identification Algorithm

Fig. 4.2 shows the block diagram of the proposed detection and identification algorithm, namely the supervisory algorithm, for each leg of the MMC [90]. The proposed supervisory algorithm consists of monitoring and decision-making units to determine

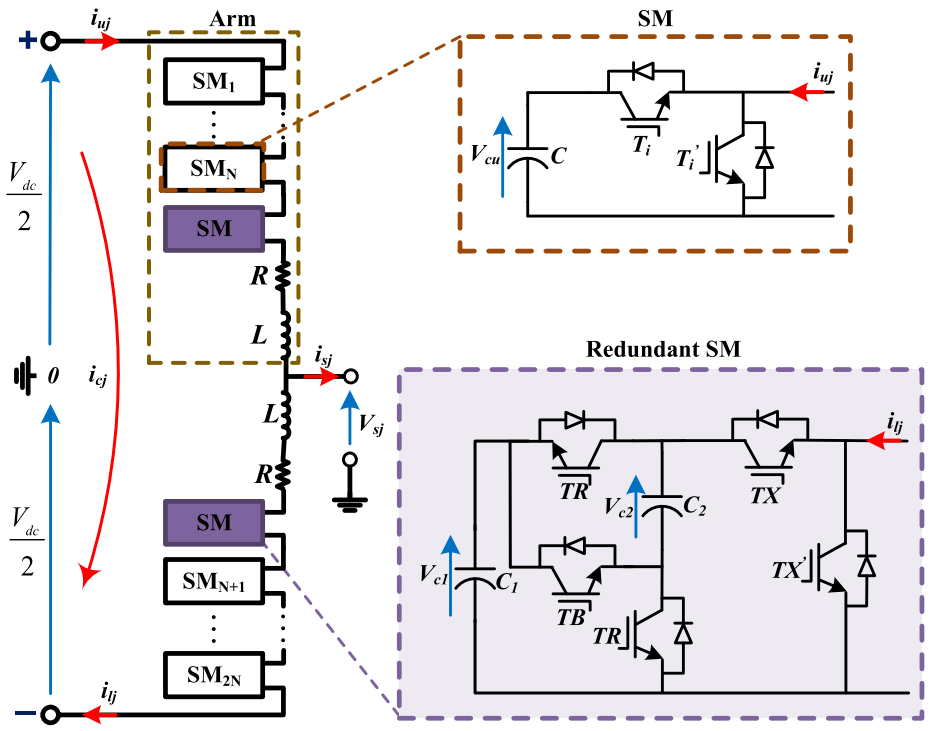


Figure 4.1: Circuit configuration of one phase leg of the MMC.

the nature of the fault and make an appropriate response. Since each fault has a unique signature, the monitoring unit aims to provide the required information to allow the decision-making unit to determine the type and location of the fault. The main idea of the monitoring unit is to compare the measured circulating current and capacitor voltages with their corresponding reference values. This comparison is made by using a hybrid structure through the coordinated operation of two subsystems that function in parallel. These subsystems independently provide the required information for the decision-making unit. The supervisory algorithm analyzes the system data, which are already available as inputs to the basic control system of an MMC. On the other hand, to reduce the calculation burden and avoid over-provisioning, the sampling frequency of the monitoring unit can be decreased, especially for an MMC with a large number of SMs.

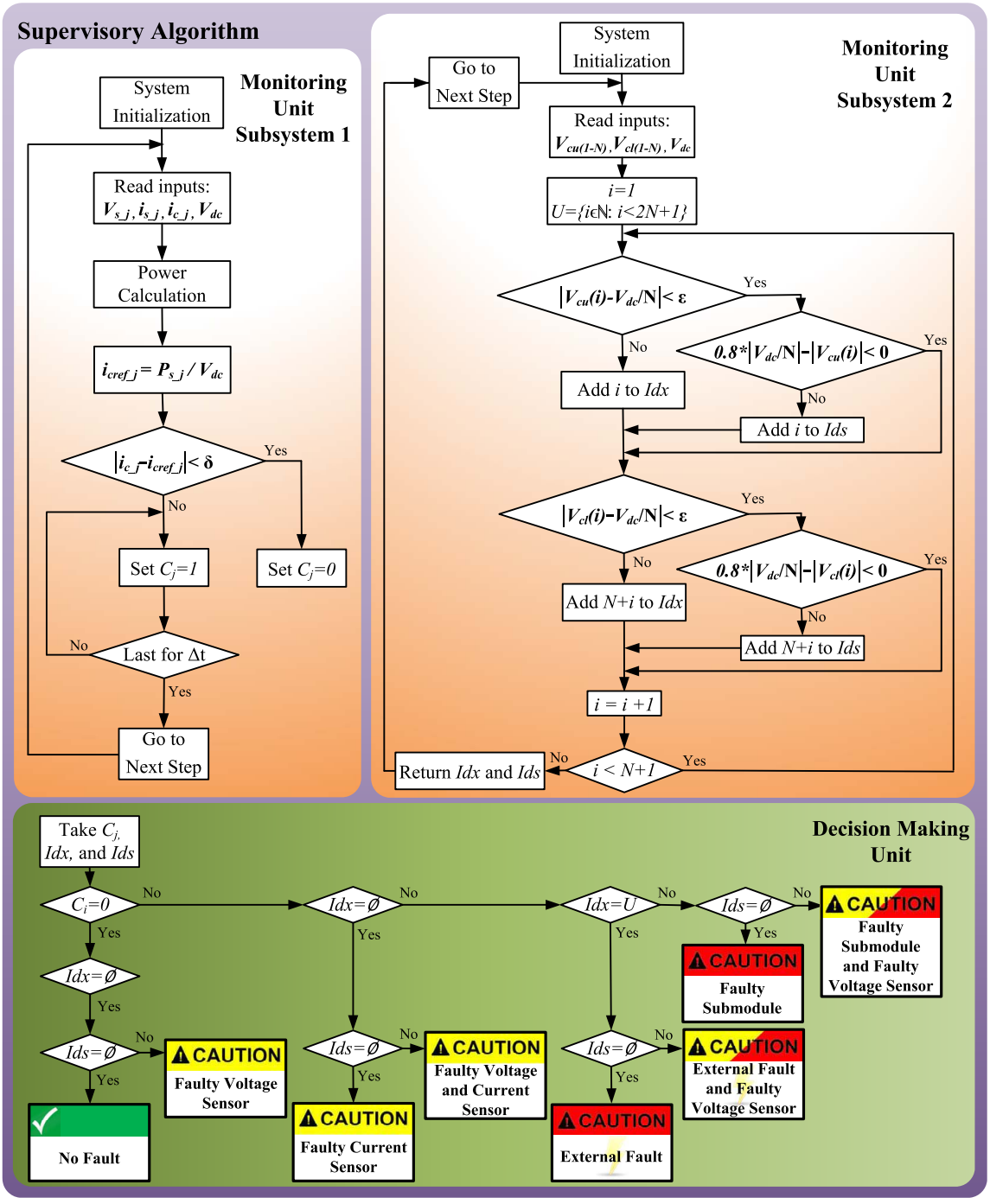


Figure 4.2: Block diagram of the proposed detection and identification algorithm including flowcharts of the monitoring and decision-making units.

4.2.1 Monitoring Unit

The first subsystem is employed to examine the dynamic response of the circulating current in each phase of the MMC. The index C_j is a binary number showing whether the conditional statement for each phase is satisfied or not. In normal operation, the measured circulating current value i_{cj} follows the reference circulating current value i_{crefj}. In this mode, the error value is definitely less than a threshold δ. Therefore, the system is indicated to be fault-free, and the current index is set to zero. Once a fault occurs, the measured inner circulating current will start deviating from the reference value. As a consequence, the error between i_{cref_j} and i_{c_j} starts increasing. If the circulating current error is greater than the threshold value, then a fault occurrence is declared in phase j of the MMC. Accordingly, the current index is set to one, which should last at least for a period of Δt. This setting provides the decision-making unit with the required time to identify the type of fault.

At the same time, the second subsystem is employed to compare the measured SM capacitor-voltages with the corresponding reference value. This comparison aims to locate the faulty component. The proposed monitoring algorithm is simultaneously applied to both the upper and lower arms in phase j of the MMC. There is a loop in which the SM capacitor voltages of phase j are stepped through index by index by comparing each voltage value with the reference value. The reference value for the SM capacitor voltages is defined as the magnitude of the dc-link voltage divided by the number of SMs per arm. The difference between the measured capacitor voltage and the reference value is compared with the upper bound threshold value, ε, to indicate which component contains the fault. In normal operation, the measured SM capacitor voltages follow the reference value. Once a fault occurs in an SM, the difference between the capacitor voltage of the faulty component and the reference value is greater than ε. Accordingly, the faulty SM vector $\boldsymbol{Idx}$ is defined as a set to

store the index number of the faulty SMs. The upper bound threshold value, defined as a percentage of the reference value, is determined according to the capability of the fault-tolerant system to support a specific number of simultaneous faults during the shortest possible identification time. Another conditional statement is incorporated into the second subsystem to identify sensor faults. Based on the dynamics of the fault in the voltage sensors, the measured voltage immediately steps down to zero. Hence, a lower bound threshold is defined in order to compare it to the difference between the reference value and SM capacitor voltage. The lower bound threshold value is set to 80% of the reference value to distinguish the transient responses from the voltage sensor fault. (See Fig. 4.2) If the second condition is satisfied, the measured SM capacitor voltage contains a voltage sensor fault. Accordingly, the index number of a faulty voltage sensor is stored in ***Ids***.

4.2.2 Decision-Making Unit

The proposed supervisory algorithm is equipped with a fault feature extraction scheme. Fig. 4.2 shows the decision-making unit, which is implemented to distinguish the fault in the SMs from that in the voltage or current sensors. In addition, this scheme can distinguish between internal and external faults.

For external faults, a conditional term is defined in the decision-making unit to effectively distinguish internal converter faults from external disturbances, e.g., grid faults and load transients. A superset defined in the second subsystem of the monitoring unit, U, includes all SM indices. All different possible sets of ***Idx*** are assumed to be a subset of this superset. Based on the nature of the external faults, if ***Idx*** includes all the SM indices, and C_j is one, the fault type is detected as an external fault.

The different types of internal faults include a faulty voltage sensor, faulty current

sensor, and faulty SM, or some combination of them. Three indices generated by the monitoring unit (i.e., C_j, ***Idx***, and ***Ids***) are fed into the decision-making unit to make a precise decision according to their values. If C_j is zero and ***Idx*** and ***Ids*** are empty, there is no fault in the system. Whenever ***Ids*** is zero, there is no voltage sensor fault. Otherwise, each element of ***Ids*** vector indicates an index of the corresponding faulty voltage sensor. A possible case of faulty current sensor is distinguished when C_j is one and ***Idx*** is empty. Finally, a possible case of faulty SM is identified when C_j is one and ***Idx*** includes some indices, but not all of them.

Once a fault occurs in one of the SMs, the corresponding arm will lose one voltage level. After detecting and identifying a faulty SM, a postfault restoration strategy is required to deal with the fault transition stage.

4.3 Postfault Restoration Scheme

This section proposes a simple postfault restoration strategy to insert the redundant SM in a very short time after a fault occurrence. Furthermore, a modified modulation scheme is presented to ensure that the capacitor voltage balances and the operation of the MMC is fault-tolerant without implementing any additional hardware. Conventional sorting algorithms cannot function properly under a current sensor fault. However, the hierarchical PCC method can effectively keep operating under any fault condition [88]. This method yields an inherently robust solution to conditions such as parameter uncertainty and transient operation when a fault occurs. The postfault restoration unit adjusts the gate switching signals based on the supervisory algorithm information to ensure service continuity. Fig. 4.3 illustrates the general modulation blocks of one phase of the 21-level MMC. It consists of three main blocks per arm: PSC modulation, hierarchical PCC, and postfault restoration units.

The aim of the postfault restoration unit is to insert the redundant SMs to maintain

the system performance after fault occurrence. The method uses the faulty component vectors as inputs. In this research, a redundant three-level SM is in the reserve mode at each arm. In the event of a component failure, the supervisory algorithm diagnoses the fault and isolates the corresponding faulty SM. Then, the postfault restoration unit activates a number of redundant SMs by adapting the gate switching signals. This adaption is realized by the transition of the switching signal from the faulty SM to a redundant one, which is triggered by ***Idx*** as a signal provided earlier by the supervisory algorithm. This transition among the gate switching signals of the faulty and redundant SMs depends on the elements of the ***Idx*** set. For example, if a fault occurs in the first SM of the upper arm, the gate switching signal of T_1 should be set to 0, and its corresponding switching state should go to T_{1_r}. Whenever the open-circuit fault occurs in any other SMs, the postfault restoration unit modifies the gate switching signals with the same approach.

4.4 Test Cases

To validate the effectiveness of the proposed framework, a typical three-phase 21-level MMC is simulated under the Matlab/Simulink environment. The control system in [21] is implemented. Each leg of the three-phase MMC is composed of ten SMs per arm.

4.4.1 Normal Operation

In order to illustrate the dynamics response of the MMC, the system is first simulated under normal operation. Fig. 4.4 demonstrates the performance of the MMC including the output voltage, arm currents, the circulating current, and capacitor voltages in phase a. Fig. 4.4(b) indicates that the monitored circulating current is closely

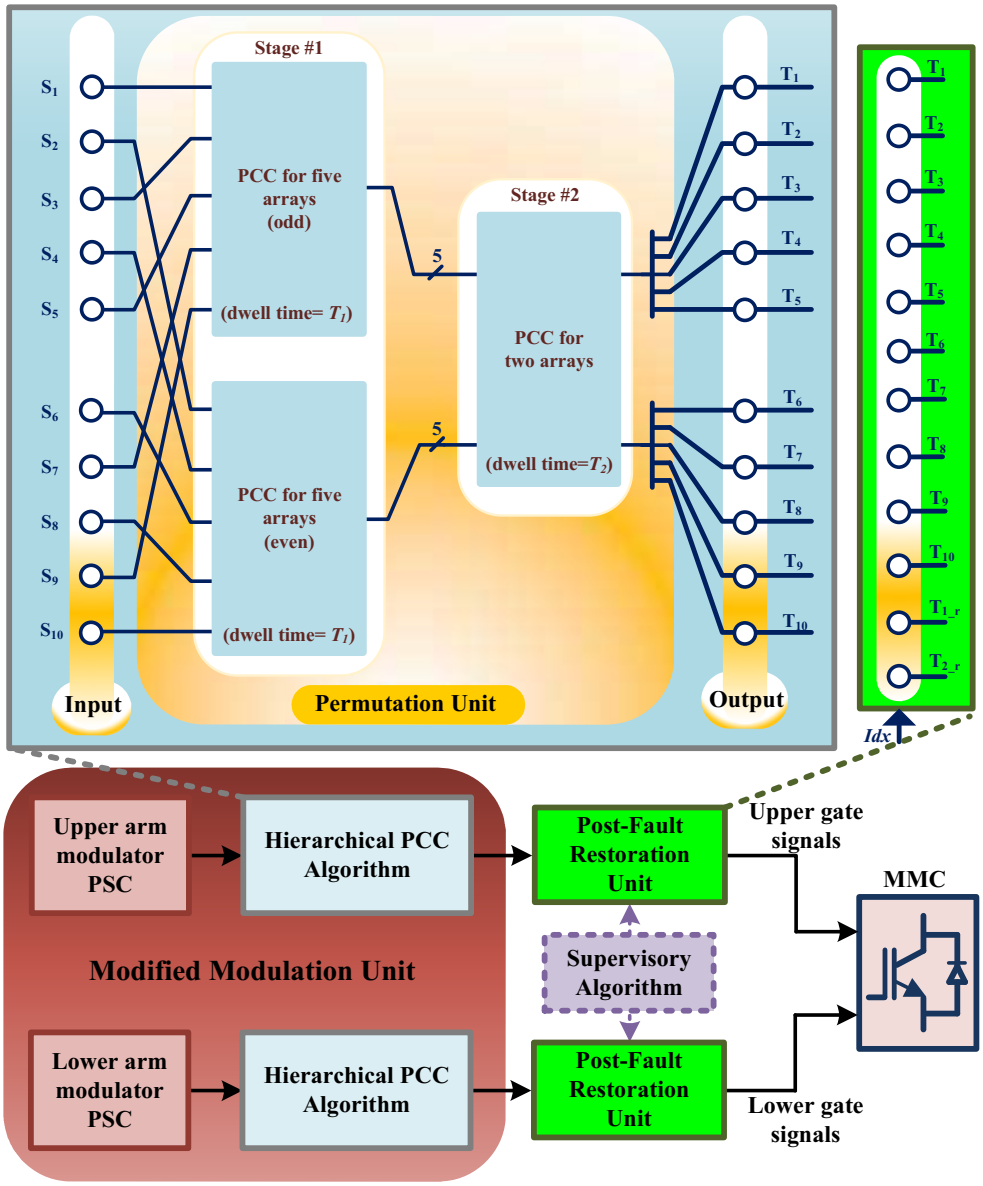


Figure 4.3: Block diagram of the modulation unit of one phase of the 21-level MMC including PSC, hierarchical PCC, and postfault restoration units.

following the reference value, which is 10.2 A. Figs. 4.4(c) and (d) show the SM capacitor voltage waveforms of the upper and lower arms. The switching frequency is an integer multiple of the fundamental frequency. However, the SM capacitor voltages do not diverge from their reference values because the MMC is equipped with the hierarchical PCC algorithm. The proposed balancing unit successfully keeps

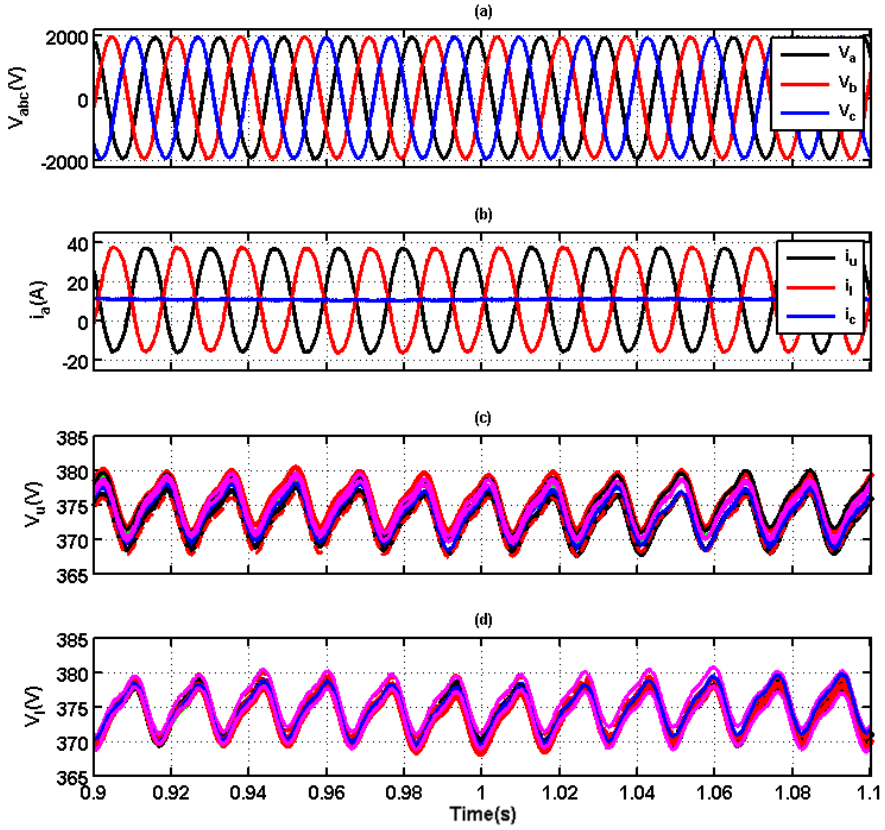


Figure 4.4: Simulated waveforms under normal operation. (a) Output voltages. (b) Arm currents and circulating current. (c) Upper arm capacitor voltages, and (d) lower arm capacitor voltages of phase a.

the SMs capacitor voltages balanced within a certain range that does not exceed 5% of the rated capacitor voltage.

4.4.2 Faulty Operation

Fig. 4.5 shows the dynamic response of the MMC during grid fault conditions to verify the effectiveness of the proposed framework in distinguishing internal converter faults from external disturbances. One-phase-to-ground asymmetrical fault occurs at t=1 s, and then a three-phase symmetrical fault occurs at t=1.5 s. Both of them are cleared after 200 ms, as shown in Fig. 4.5(a). Fig. 4.5(b) illustrates the circulating current waveforms during the grid faults, where the circulating current error is greater than

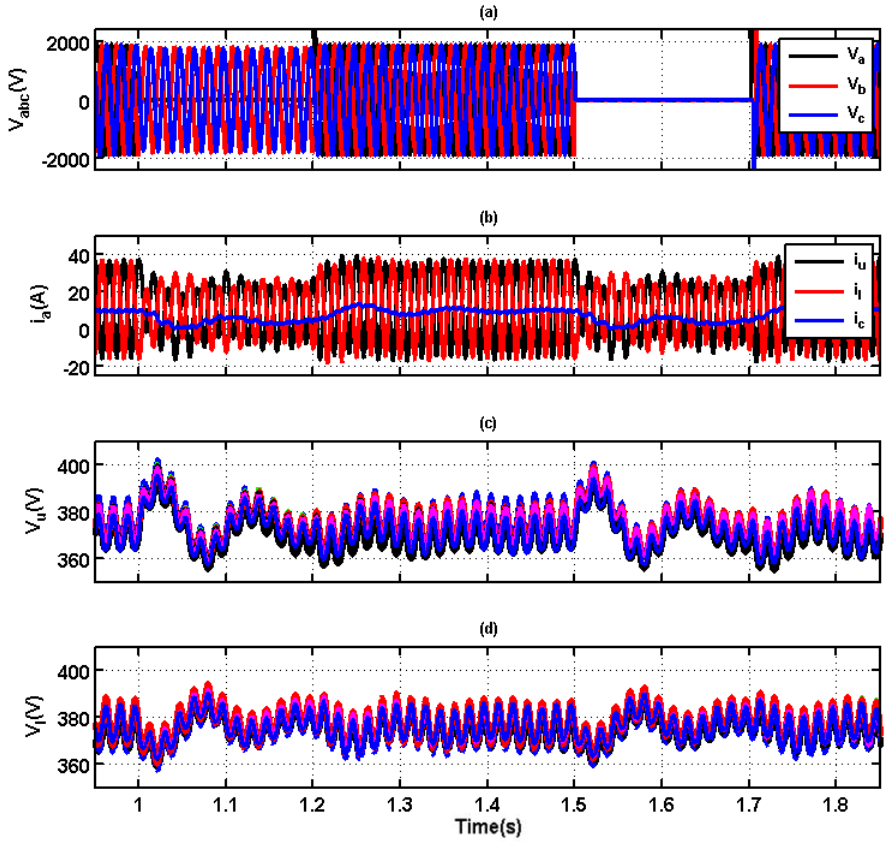


Figure 4.5: Simulated waveforms under grid fault conditions. (a) Output voltages. (b) Arm currents and circulating current. (c) Upper arm capacitor voltages; (d) lower arm capacitor voltages of phase a.

the threshold value in the first subsystem of the monitoring unit. The second subsystem is simultaneously executed to find the faulty component vector ***Idx***. During the grid faults, all SMs capacitor voltages start deviating from their corresponding reference values, as shown in Figs. 4.5(c) and (d). Therefore, ***Idx*** includes all SM indices. According to the proposed supervisory algorithm, these types of faults are detected as an external fault, and the proposed algorithm precisely distinguishes between faults in the SMs and the grid. This capability prevents unnecessary activation of the postfault restoration unit under external fault conditions. The SM capacitor voltages recover in a short time after the fault clearance.

Four scenarios are tested to analyze the performance and resiliency of the proposed

framework under open-circuit faults. The capacitor voltage of a faulty SM and the circulating current of the corresponding leg cannot track their reference values after the occurrence of an open-circuit fault. The current error threshold in all scenarios is defined as 50% of the reference circulating current value, and Δt is set to 100 ms. The voltage threshold value of the first three scenarios is set as 8% of the reference SM capacitor voltage.

Fig. 4.6 shows the performance of the MMC when a Type I open-circuit fault occurs at t=1 s. In the Type I open-circuit fault, the faulty SM is in the switching-state-dependent inserted mode when the arm current is positive. It is in the bypassed mode when the arm current is negative. Accordingly, the capacitor voltage of the faulty SM during the fault becomes higher than the capacitor voltages of the healthy SMs in the phase a. In addition, the capacitor voltages of the healthy SMs in the corresponding arm start increasing because the output voltage of the faulty SM in the charging mode directly depends on its switching state. The same happens for the opposite arm in the same leg to keep the energy between the arms balanced, as indicated in Fig. 4.6. Therefore, both the circulating current and capacitor voltages start increasing after the fault occurrence.

Fig. 4.6(a) shows that the circulating current waveform cannot track the reference value after the fault occurrence and starts increasing in a short time. Consequently, the conditional statement in the first subsystem of the monitoring unit is not satisfied. Therefore, the current index is set to one. On the other hand, Fig. 4.6(b) shows one of the SM capacitor voltages in the upper arm starts deviating from its reference value. According to the proposed supervisory algorithm, the decision-making unit locates and isolates the fault in the first SM at t=1.05 s, and the postfault restoration unit immediately inserts the redundant unit to compensate for the missing voltage level. After a few microseconds is elapsed between the detection and the identification of

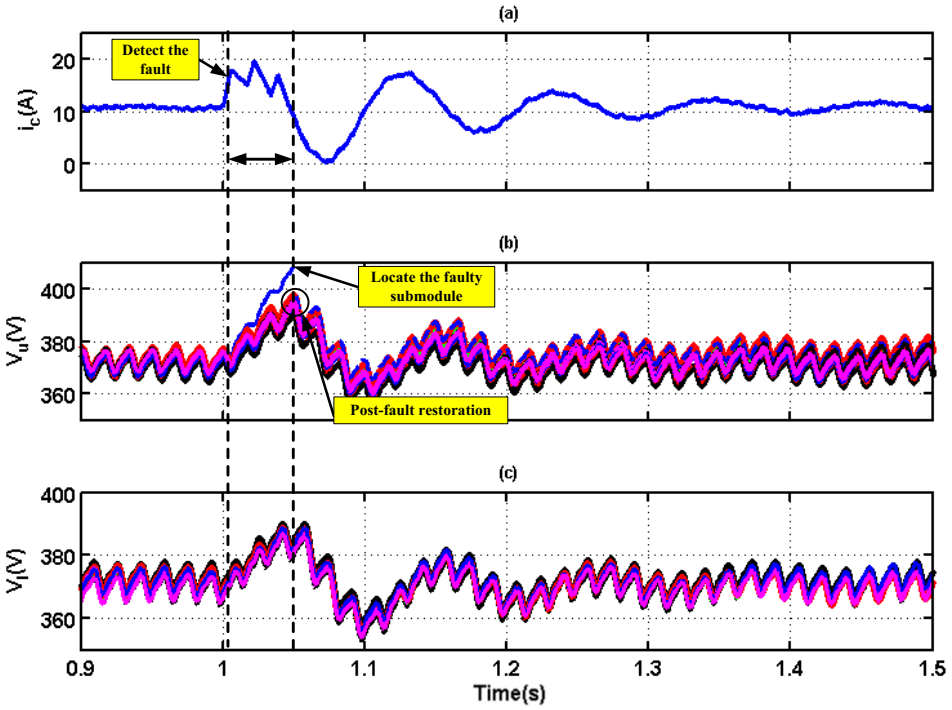


Figure 4.6: Simulated waveforms under Type I open-circuit fault in phase a. (a) Circulating current. (b) Upper arm capacitor voltages. (c) Lower arm capacitor voltages.

the faulty SM, the postfault restoration starts.

The simulation results for a Type II open-circuit fault at t=2 s are shown in Fig. 4.7. According to Table 4.1, the faulty SM capacitor is in the charge mode as long as the positive arm current flows in the leg. Consequently, the capacitor voltages of the remaining healthy SMs in the corresponding arm start to decrease. To keep the energy balanced between the arms, the same process happens for the opposite arm in the same leg. At t=2.043 s, the substitution of faulty SM by the redundant SM restores the system to its original state.

As expected, the circulating current starts to diverge as the fault occurs. When the circulating current error deviates from the pre-defined threshold, the monitoring unit considers this situation as a faulty mode. On the other hand, one of the SM capacitor voltages in the upper arm starts deviating from its reference voltage, as

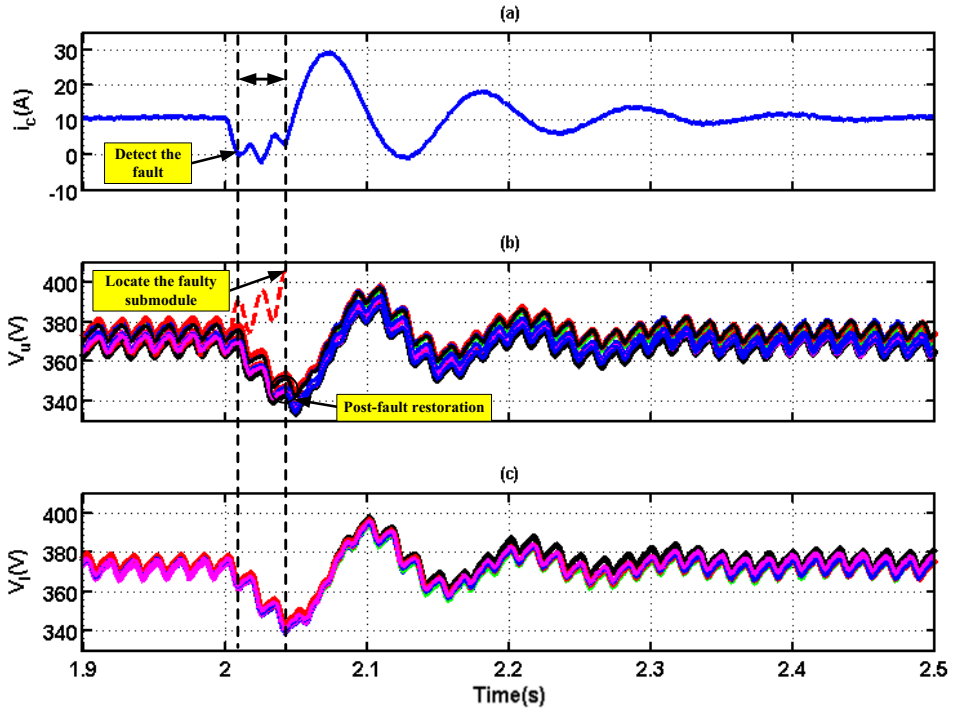


Figure 4.7: Simulated waveforms under Type II open-circuit fault in phase a. (a) Circulating current. (b) Upper arm capacitor voltages. (c) Lower arm capacitor voltages.

shown in Fig. 4.7(b). Accordingly, the decision-making unit locates and isolates the fault in the sixth SM at t=2.043 s. The postfault restoration replaces the faulty SM right away.

Fig. 4.8 shows the performance of the MMC when a Type III open-circuit fault occurs at t=3 s. Fig. 4.8(a) illustrates that the circulating current immediately starts to diverge as the fault occurs. The monitoring unit distinguishes a faulty mode when the circulating current error deviates from the predefined threshold. According to the second subsystem algorithm of the monitoring unit, one of the SM capacitor voltages in the lower arm starts deviating from its reference voltage, as shown in Fig. 4.8(c). Based on the current index and voltage vector content, the decision making unit locates and isolates the fault in the eleventh SM of the lower arm at t=3.022 s. The dynamics of the circulating current and voltage capacitor voltages in Type III faults

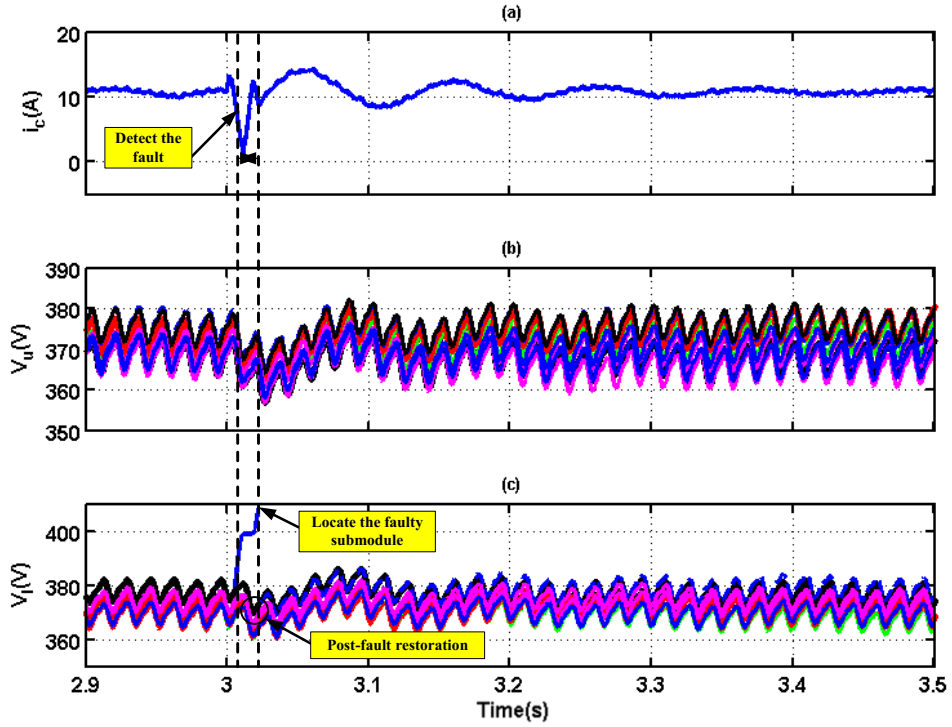


Figure 4.8: Simulated waveforms under Type III open-circuit fault in phase a. (a) Circulating current. (b) Upper arm capacitor voltages. (c) Lower arm capacitor voltages.

are similar to those in Type I. Since both switches are open, the time from detection to restoration is much shorter than the time for other types of faults.

The performance of the MMC when two Type I open-circuit faults occur simultaneously in phase a at t=4 s is shown in Fig. 4.9. As described earlier, the current error threshold is defined as 50% of the reference circulating current value and Δt=100 ms. In this scenario, two faults occurs at the same time. Hence, ε should be set at 12% of the reference SM capacitor voltage to attain the capability to diagnose the faulty SMs. Choosing a higher ε ensures an accurate fault diagnosis, especially in the case of simultaneous faults in one arm. However, the higher ε increases the identification time. Therefore, a tradeoff occurs between the capability to detect a number of simultaneous faults and to minimize the identification time. In the simulation, the elapsed time from detection to identification in the proposed approach is less than 100 ms,

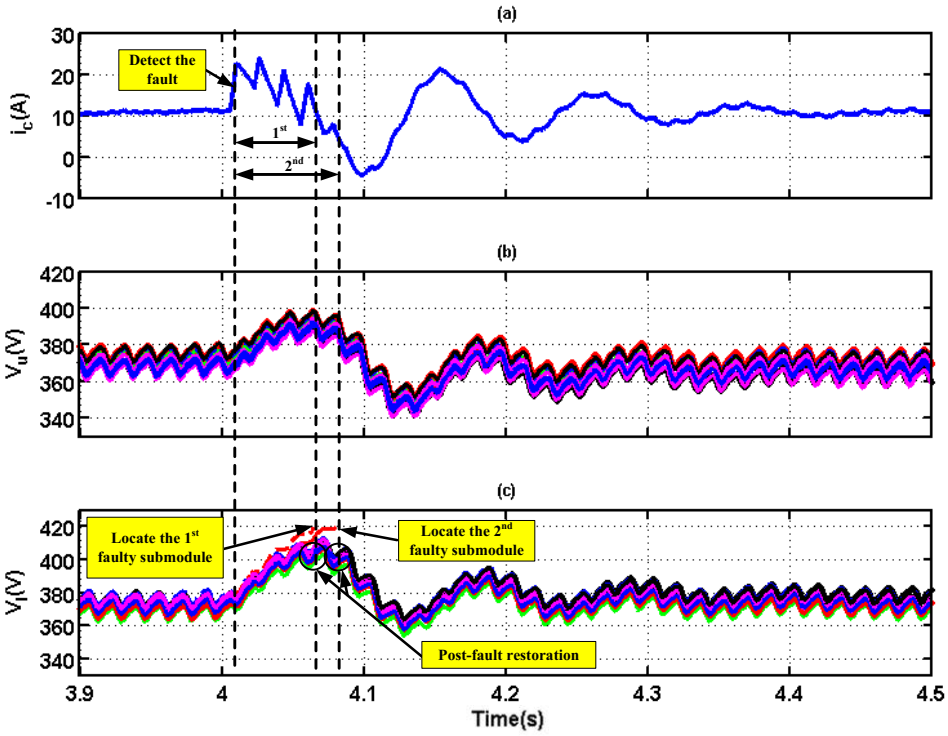


Figure 4.9: Simulated waveforms under two simultaneous Type I open-circuit faults in phase a. (a) Circulating current. (b) Upper arm capacitor voltages. (c) Lower arm capacitor voltages.

which is low compared to the elapsed time with previous methods.

Fig. 4.9(a) shows the circulating current waveform, which starts to diverge as the fault occurs. Therefore, the first subsystem of the monitoring unit detects the fault occurrence after a few microseconds. At t=4.065 s and t=4.08 s, the second subsystem of the monitoring unit identifies the faulty components, as shown in Fig. 4.9(c). At these points, the decision-making unit chronologically locates the faulty SMs in the lower arm, and the postfault restoration unit substitutes the redundant SMs for the faulty ones in the corresponding arm. Based on the operation principal of the proposed SM in Table 3.1, the faulty SMs are replaced chronologically.

4.4.3 Hardware-in-the-Loop Verification Studies

This section presents the real-time performance of the proposed resilient framework in the hardware-in-the-loop setup. The results are captured on a 500-MHz four-channel oscilloscope connected to the data-acquisition card on a Virtex-6 FPGA board with a cycle of 290 ns. The MMC controller and supervisory and postfault restoration algorithms are implemented in the CPU with a time step of 50 μs. The switching frequency is at 300 Hz. The measurements and commands are updated every 10 μs. Both the Type-I and Type-III scenarios are executed to represent the SM capacitor-voltage and circulating current waveforms in the upper and lower arms during fault occurrence.

Fig. 4.10(a) shows the dynamic response of the MMC to the Type-I open-circuit fault occurrence at one SM in the lower arm. Once the fault occurs, the circulating current and capacitor voltages start increasing. Due to the open-circuit fault features, the capacitor voltage of the faulty SM becomes higher than the capacitor voltages of the healthy SMs in the corresponding leg. Meanwhile, the supervisory unit immediately detect the fault because the circulating current error threshold is passed, and then the faulty component vector is filled with an index number. Accordingly, the decision-making algorithm locates and isolates the faulty SM after less than 50 ms. At the same time, the postfault restoration unit inserts a reserved SM to compensate for the missing voltage level.

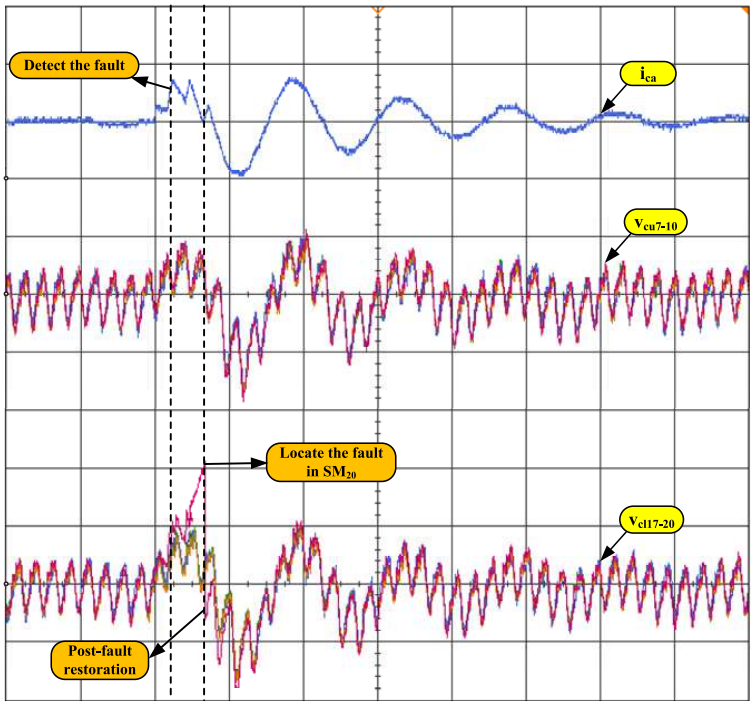
The dynamic response of the system to the Type-III open-circuit fault occurrence is illustrated in Fig. 4.10(b). The circulating current immediately starts to diverge from the corresponding reference value as the fault occurs. Once the circulating current error exceeds the predefined threshold, the first subsystem of the monitoring unit detects a faulty mode. After a short time, the second subsystem of the monitoring unit detects that one of the SM capacitor voltages in the lower arm starts deviating

from the permissible threshold. Consequently, the decision-making unit locates the faulty SM, and the postfault restoration unit inserts another level of the reserved SM. As shown in Fig. 4.10(b), the SM capacitor voltages are also well balanced in a very narrow band that does not exceed 5% of the boundaries. The hardware-in-the-loop platform results are in good agreement with the simulation results and theoretical analysis.

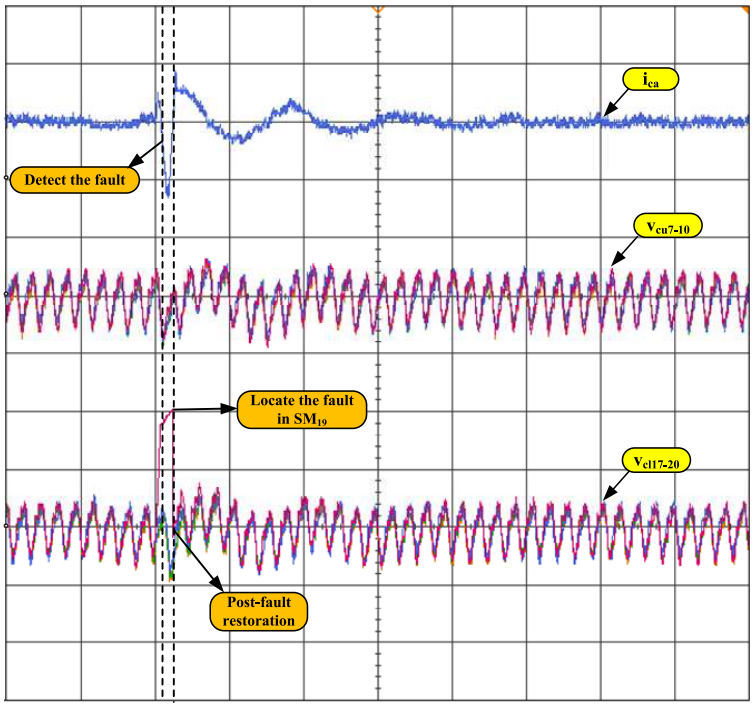
4.5 Conclusions

This chapter presents a resilient framework for fault-tolerant operation in MMCs to facilitate normal operation under internal and external fault conditions. A supervisory algorithm and a postfault restoration unit are implemented to realize the fault-tolerant algorithm. The supervisory algorithm is composed of monitoring and decision-making units to detect and identify faults. The faults are simply diagnosed by analyzing the circulating current and SM capacitor-voltage waveforms. The postfault restoration scheme is realized by virtue of the proposed SM circuit integrated into each arm of the MMC. An extensive set of time-domain simulation studies in the Matlab/Simulink platform is performed to evaluate the performance of the proposed strategy. It is implemented in FPGA-based real-time simulator in a hardware-in-the-loop test bench to verify the feasibility of the proposed scheme.

The study results indicate the desired performance of the proposed framework when the system is subject to various types of open-circuit fault. The case study demonstrates 1) superior fault diagnosis of internal and external system failure, 2) balanced capacitor voltages under fault conditions, and 3) short elapsed time from detection to identification. The proposed method distinguishes the fault occurring in the SMs from those occurring in the sensors. In addition, it restores the system with a fast response even after the occurrence of multiple faults.



(a) Type I open-circuit fault in the 20th SM



(b) Type III open-circuit faults in the 19th SM

Figure 4.10: Dynamic response of the system during fault occurrence in phase a. [Time: 70 ms/div, i_{ca}: 10 A/div, v_{cu} (channels 1-4): 15 V/div, v_{cl} (channels 1-4): 15 V/div].

Chapter 5

DC Parking Lot and Smart DC Home Applications

This chapter develops a resilient decentralized control framework with PnP capability for a modern parking lot that incorporates various electric components including plug-in and wireless EV charging stations, RESs, energy storage devices, and ac loads. The DGs including fuel cell (FC), photovoltaic (PV), and supercapacitor (SC) units with different dynamics are integrated into the parking lot. The proposed control system aims to ensures accurate dc and oscillatory power component-sharing among DGs under a wide range of rapidly varying single-phase EV chargers and three-phase unbalanced ac loads without a need for a communication link.

Furthermore, the design of DCC method and FSI scheme for a smart dc home is presented. The DCC method integrates a virtual impedance within the decentralized control loops of the DGs and interlinking converter to guarantee accurate power management, dc bus voltage regulation, and fast restoration after fault occurrence. In addition, the FSI scheme is developed to quickly identify and isolate a faulty

segment to protect sensitive assets from the high fault current by using only local measurements.

5.1 Configuration of DC Parking Lot

A single-line diagram of a dc parking lot connected to the utility grid via two BICs is shown in Fig. 5.1. This parking lot hosts five DGs, three plug-in EV charging stations, and three wireless EV charging stations. The PV and FC units are integrated into the parking lot through dc/dc converters. Moreover, bidirectional dc/dc converters are used to control the output of the SC units. Relying on the scalability and PnP capability of the proposed framework, DGs within the parking lot can be inserted or bypassed at any time. The plug-in EVs are interfaced to the dc parking lot via multi-stage converters to implement conductive charging systems. On the other hand, an inductive charging system is provided for some charging stations through a resonant converter to realize wireless power transfer.

The parking lot is connected to the utility grid via two BICs that provide a bidirectional exchange of energy between the dc bus and grid side of the converter. Implementing two BICs significantly enhances the operational reliability by providing a fault-tolerant operation with a high power rating and low thermal design burden. The dc link of each BIC is equipped with a contactor to manage the connection between the BIC and dc parking lot. This design helps to make the platform flexible enough to reconfigure the system once a fault occurs. In the grid-connected mode, the BICs function as the energy buffer to assist the dc-side power sources to meet the power demand. A variety of single-phase and balanced and unbalanced three-phase loads are connected to the ac side and normally supplied by the utility grid. Once the solid state transfer switch goes off, forming a hybrid ac/dc microgrid, the BICs should meet the ac-side load power demand. Accordingly, the DGs in the parking lot

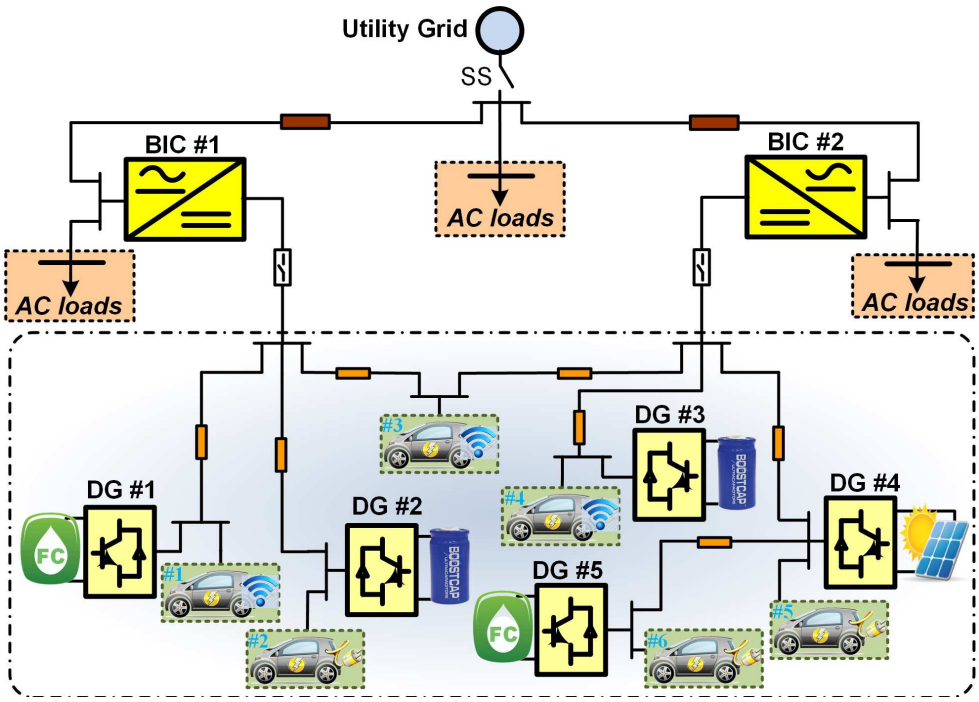


Figure 5.1: Schematic diagram of the dc parking lot connected to the utility grid through two BICs.

provide the BICs with the required dc-link power to supply power to the overhead ac loads.

The circuit diagram of an MMC-based BIC is employed to interface the dc parking lot to the utility grid. This topology offers high efficiency and a superior performance with respect to the output voltage quality. Let's derive the dynamic model of each subsystem in Fig. 5.1 to facilitate the design of a resilient PnP decentralized control framework.

DG Units

A set of PV and FC units is integrated into the parking lot to handle the power demand and maintain the dc bus voltage constant. The SC units, as short-term energy storage devices, are aggregated to improve the dynamic response of the system by dealing with transients. The FC and PV units supply the main power, and the SC

units provide a fast transient response and the oscillatory power component. The output of the FC unit is controlled through a unidirectional dc/dc boost converter to smooth the output current [32, 95, 96]. The PV unit is connected to the parking lot via a unidirectional dc/dc boost converter that operates in the maximum power point tracking mode. The solar panels in the roof of the shade at the parking lot provide clean power, save space, and reduce CO_2 emissions [97]. Due to the intermittent nature of the PV unit and the slow dynamic response of the FC units, the SC units play a key role in complementing the main power sources and assure the high performance of the overall system. A bidirectional buck-boost dc/dc converter interfaces the SC units with the dc bus. The SC units share the oscillatory power components based on their capacities and not on their distance from the oscillation source. As a consequence, this approach ensures superior peak shaving service and oscillatory power sharing at the lowest cost [98]. A combination of FC, PV, and SC ensures that the outlet current of the parking lot is drawn with low distortion.

Plug-in EV Charger

The battery charger is a critical component to provide reliable, high-quality, and efficient real power from the parking lot outlet to the battery of the plug-in EV. Typically, an onboard charger is installed inside the vehicle to address volume and cost constraints. The specific configurations of charging modes vary from location to location, depending on the frequency, voltage, and transmission standards. Hence, practices in EV charging are designed based mainly on the location and time required for charging. Level 1, Level 2, and DC fast charging are the primary options currently used for electric vehicles in North America. Level 1 functions at 120 V AC, whereas Level 2 operates at 208 or 240 V AC, and DC fast charging demands 200 to 450 V DC. Among the three plug-in EV charging approaches, Level 1 chargers are slow, and

DC fast chargers are costly. Level 2 chargers are usually preferred due to their fast charging time and standardized vehicle-to-charger connection, which requires a 240 V ac outlet. Hence, Level 2 chargers have become the most popular chargers for the installation of EV charging stations in public charging facilities [68, 99, 100].

Level 2 charging stations in dc parking lots commonly utilize a single-phase converter to generate the desired ac voltage needed for the onboard charger system. Then, the charger system transfers the required energy to charge the battery pack. The batteries of plug-in EVs can be used to inject energy into the parking lot. However, battery degradation, the need for complex communication, and the impacts on overall system performance are some limiting factors. On the other hand, unidirectional charging requires only negligible transmission investments. Accordingly, a unidirectional battery charger is typically implemented to charge the battery of the plug-in EV. Fig. 5.2 shows the basic structure of the single-phase full-bridge converter, which is deployed to interface the onboard battery charger with the parking lot.

In terms of the dynamic response, double-frequency fluctuation is introduced in the presence of single-phase plug-in EV charging stations. Therefore, the Level 2 charging system is inherently subjected to significant unbalanced conditions. Moreover, the power oscillations impose double-frequency ripples on the dc bus voltage. This is not a major problem in wireless charging stations because the inverter is a dc-to-high-frequency-ac inverter.

Wireless EV Charger

Fig. 5.3 shows a large air-gap wireless power transfer charger for EVs [101]. In the first stage, a dc-to-high-frequency-ac inverter produces a square wave of hundreds of kHz. The output terminal of the inverter is connected to the input terminal of a resonant tank network. The resonant tank network is comprised of the stationary source

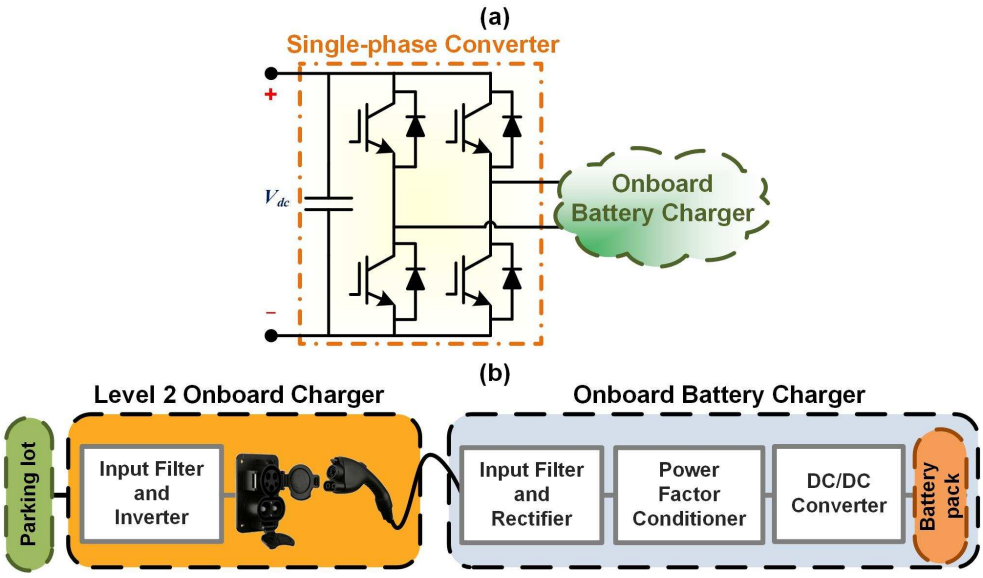


Figure 5.2: (a) Onboard unidirectional Level 2 charging system. (b) Block diagram of a plug-in charger for an EV.

resonator pad, interface electronics, and a vehicle-mounted capture resonator. The frequency of the resonant tank network is typically tuned to the switching frequency of the inverter. On the onboard battery charger side, a diode bridge rectifier is interfaced with the secondary of the resonant tank network rectifying the current to supply the battery pack. The magnitudes of the output current and voltage waveforms are controlled by adjusting the switching frequency around the resonant frequency. Accordingly, if the resonant tank frequency is set equal to the switching frequency, the dc output voltage will be equal to the dc input voltage.

The resonant tank is a two-coil system, in which energy is transferred from the primary coil across the air gap to the secondary coil. An ac-equivalent circuit can be simply derived [101]. Assuming the same leakage inductance in primary and secondary coils, the frequency-domain equations of the resonant tank network are written as [102]

$$V_1(j\omega_s) = [\frac{4V_{dc}}{\pi} sin(d\pi)]\angle 0 \tag{5.1}$$

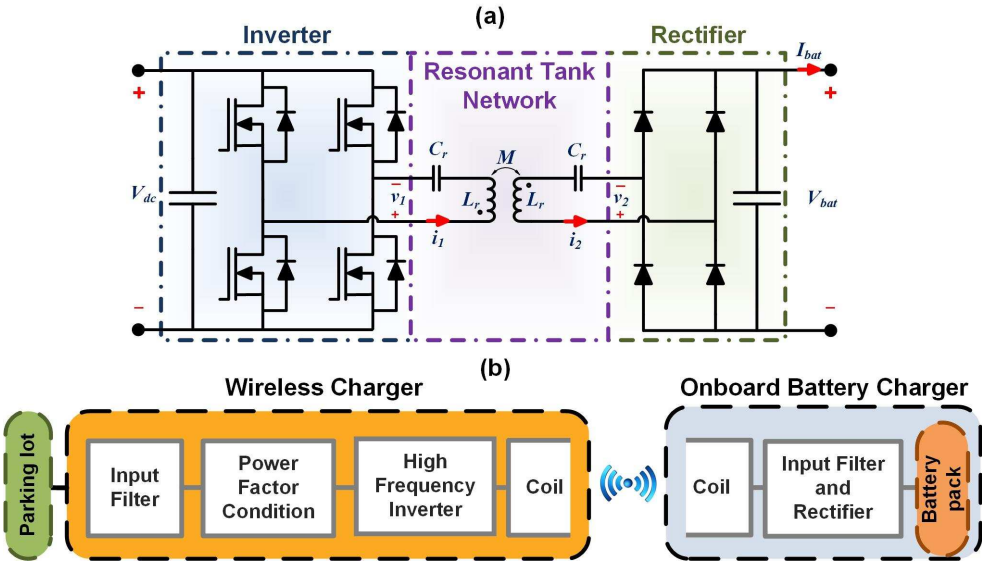


Figure 5.3: (a) Circuit diagram of the wireless charging system. (b) Block diagram of a wireless power transfer charger for an EV.

$$V_2(j\omega_s) = [\frac{4V_{bat}}{\pi}]\angle\theta \tag{5.2}$$

$$R_e = \frac{8}{\pi^2}\frac{V_{bat}}{I_{bat}} \tag{5.3}$$

where V_{bat} and I_{bat} are the voltage and current of the battery, respectively. V_1 and V_2 are the fundamental components of v_1 and v_2, respectively, and θ is the phase angle between them. ω_s is the angular switching frequency, d refers to the duty cycle of the inverter, and R_e presents the effective resistive load of the tank network.

To control the charging mode of the battery from the primary side, the input current is regulated according to the battery voltage. From the ac-equivalent circuit, the battery current can be expressed as [101]

$$I_{bat} = \frac{8\sqrt{L_r C_r}V_{dc}}{\pi^2 M} sin(d\pi) \tag{5.4}$$

where L_r is the self-inductance, C_r is the resonant capacitor, and M is the magnetizing inductance.

5.2 Resilient PnP Decentralized Control Framework

This section presents a PnP decentralized control framework for the dc parking lot that comprehensively operates in the grid-connected, hybrid, and island modes. The DGs with different dynamic models can be simply inserted or bypassed from the platform at any time according to the control commands. In the dc side, the proposed control strategy aims to share the power dc and oscillatory components under a wide range of rapidly varying EV loads. For the BICs, a decentralized control strategy is implemented by designing an effective switched control system, which controls the ac loads in the island mode and contributes to the dc parking lot in the grid-connected mode. The operation of the BICs, DGs, and charging interfaces is managed in a decentralized manner enhancing the reliability of the overall system. The proposed control strategy eliminates the need for any communication network, in which communication delay may seriously impact system stability. On the other hand, this feature diminishes the concern related to the EMI problem in the presence of wireless chargers.

5.2.1 Control of DG units

Fig. 5.4 shows the block diagram of the DGs control systems. The proposed PnP decentralized control strategy manages power among the DGs with different dynamics without reliance on communication. The interfaced power converters are controlled to ensure the perfect regulation of the dc bus voltage, fast tracking of the references, and a superb stability margin of the closed-loop system. The FC and PV units, with high energy density, operate as the main power sources, and the SC units, with high power density and fast dynamic response, act as complementary power sources. The unidirectional power flow of the FC and PV decouples the dynamics of the main power sources from the SC units. The PV unit controller operates in the maximum

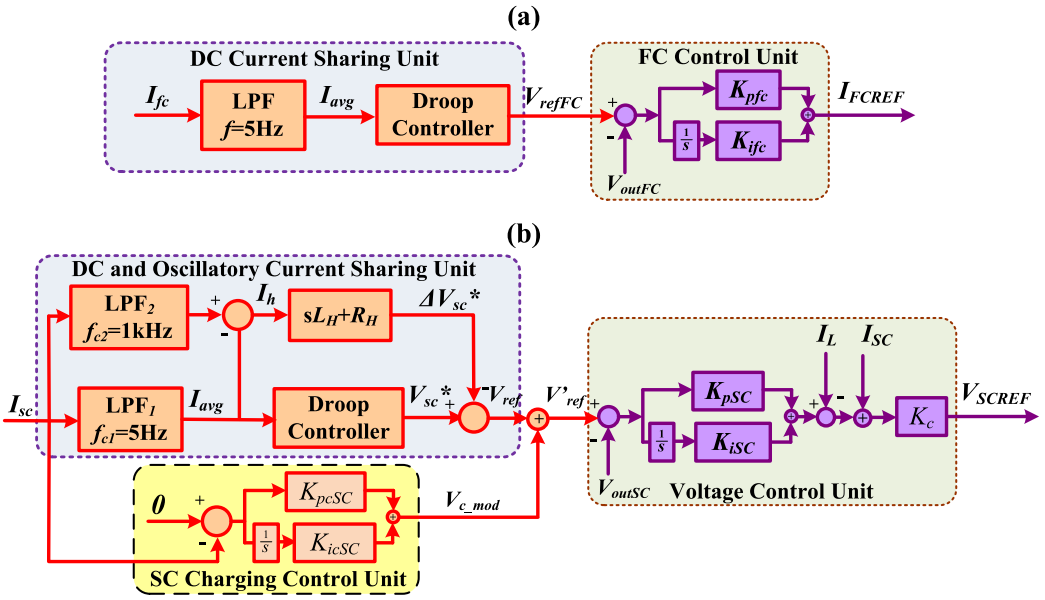


Figure 5.4: PnP decentralized control diagram of (a) the FC unit, (b) the SC unit.

power point tracking mode. Fig. 5.4(a) shows the controller of each FC unit, which includes the dc current-sharing and voltage control units. The FC current-sharing unit regulates only the dc current component, and the voltage controller employs a proportional-integral (PI) controller to meet the power demand at a regulated dc bus voltage.

The SC unit controller operates based on a simple principle, in which the SC unit is charged or discharged based on the transient power demand. As shown in Fig. 5.4(b), the block diagram of the controller includes the power-sharing, charging, and voltage control units. The power-sharing control unit for the SC converter consists of the dc and oscillatory current-sharing units. This control unit enables the SC units to supply the dc and oscillatory current components according to their rated power.

DC Current Sharing Unit

In the dc current sharing unit, a low-pass filter (LPF) with a cut-off frequency of 5 Hz is employed to eliminate the high-frequency ripples of the output current. Moreover,

the LPF provides sufficient time scale separation between the current and voltage control loops. The averaged current is then applied to the droop controller to calculate the voltage magnitude of the reference signal. The following V-I droop function is employed for the dc current sharing unit:

$$V^*(s) = V_0(s) - R_D I_{avg}(s) \tag{5.5}$$

where $V_0(s)$ is the nominal voltage of the dc microgrid, and R_D is called the static gain of the droop controller. To obtain the appropriate dc current sharing unit gain (R_D), the output voltage of the converter (V_{out}) should not exceed the allowable voltage variation when the converter injects its maximum power. Therefore, R_D is defined as

$$R_D = \frac{V_{max} - V_{min}}{I_{max}} \tag{5.6}$$

In order to augment the system reliability, the output power of the sources should be proportional to their nominal ratings. Hence, the static droop gains is tuned as

$$R_{D1} I_{nom_1} = R_{D2} I_{nom_2} = R_{Di} I_{nom_i} \tag{5.7}$$

where I_{nom_i}, is the nominal rating of the i^{th} converter. I_{avg} in (5.5) can be expressed as

$$I_{avg}(s) = \frac{\omega_{c1}}{s + \omega_{c1}} I_{SC}(s) \tag{5.8}$$

where ω_{c1} is the cut-off frequency of LPF_1. According to Fig. 5.4, the reference of the voltage control unit is calculated as

$$V_{ref}(s) = V^*_{SC}(s) - \Delta V^*_{SC}(s) \tag{5.9}$$

where $\Delta V^*_{SC}(s)$ is the output of the proposed oscillatory current sharing unit, which is explained in the following subsection.

Oscillatory Current Sharing Unit

Since the dc current sharing unit cannot individually share the oscillatory components of the loads current among the DG units, an oscillatory current sharing unit is paralleled to it. The dc and oscillatory control units specify, respectively, the amount of the dc and oscillatory current that the corresponding SC should share. Because of the slow dynamic response of the FC unit, the oscillatory current-sharing unit distributes the double-frequency and high-frequency ripples among the SC units based on their capacities. The structure of the proposed oscillatory current sharing unit is illustrated in Fig. 5.4.

The current oscillatory component stands for the current high-frequency component (from 5 Hz to 1 kHz). In other words, the current oscillatory component is the portion of current where there is no dc component. Two LPFs are employed to differentiate between the high-frequency ripples (with a frequency between 5 Hz to 1 kHz) and the dc component. To eliminate the very high-frequency ripple and noise of the current (with frequency higher than 1 kHz), the output current of SC unit is passed through a LPF with cut-off frequency 1 kHz. Then, the dc component of the filtered signal is eliminated by subtracting from the average current provided by the dc current sharing unit. Therefore, the output current with the frequency from 5 Hz to 1 kHz is extracted by the mentioned approach. The input current to the oscillatory current sharing unit can be written as

$$I_h(s) = \frac{s(\omega_{c1} - \omega_{c2})}{(s + \omega_{c1})(s + \omega_{c2})} I_{out}(s) \tag{5.10}$$

where ω_{c2} is the cut-off frequency of LPF_2. According to (5.5), (5.8), (5.9), and

(5.10), the difference between the generated voltage signals from the dc and oscillatory current sharing units provides the dc bus voltage reference value that is expressed as [69]

$$V_{ref} = V_0 - [\frac{R_D\omega_{c1}}{s+\omega_{c1}} + \frac{s(\omega_{c1}-\omega_{c2})(R_H+sL_H)}{(s+\omega_{c1})(s+\omega_{c2})}]I_{SC} \tag{5.11}$$

where V_0 is the nominal SC unit voltage, and I_{SC} is the SC unit output current. R_D, R_H, and L_H refer to the static gain of the droop controller, static gain of the oscillatory unit, and dynamic gain of the oscillatory unit, respectively. ω_{c1} and ω_{c2} are the cutoff frequencies of the LPFs with the frequencies of 5 Hz and 1 kHz, respectively.

A charging control unit is aggregated to control the state of the charge of SC units to avoid overcharge or undercharge conditions. This unit produces a modification term that is added to the generated reference voltage from the current-sharing unit. Adding the modification term assists the controller of the SC unit, in which the SC current accurately follows its reference to zero in the steady-state condition.

$$V'_{ref} = V_{ref} + V_{c-mod} \tag{5.12}$$

The voltage control block, including the inner current and outer voltage loops, regulates the dc bus voltage of the parking lot according to the reference generated by the power-sharing unit and modified by the SC charging unit. The PI controller parameters of the outer voltage loop are designed to obtain the proper stability margin and bandwidth for the closed-loop system. In the inner current loop, a positive gain is employed to improve the internal stability of the voltage controller loop and decrease the output impedance of the converter in high frequencies.

5.2.2 Control of Bidirectional Interlinking Converters

The block diagram of the proposed switched control strategy for the BICs is shown in Fig. 5.5. In the grid-connected mode, the MMC-based BICs operate in the rectifier mode and allow power transfer from the three-phase ac side end to the dc bus. They contribute to the dc parking lot by regulating the dc bus voltage. In addition, they assist the DGs to meet the demand for the dc and oscillatory power components. In the island mode, the MMC-based BICs operate in the inverter mode, allowing the power to flow from the dc bus to the three-phase ac side. They participate in the ac-side power management to supply power to the ac loads. In both operation modes, the proposed control block consists of power-sharing, outer loop voltage, and inner loop current-control units. The switching signal is activated by the islanding detection signal. Accordingly, the switched control system is designed to stably control the system in both the on- and off-grid modes. This approach can be easily extended to cover other operation modes depending on different circuit characteristics.

1) Island Mode: The power-sharing control unit generates the magnitude and frequency of the reference voltage for the inverter according to the droop coefficients. A LPF is employed to extract the average active and reactive powers from the power calculation unit. Then, a droop controller droops the output reference voltage magnitude and frequency to allow the BICs to share the desired amount of active and reactive power demand. Moreover, a restoration unit is integrated to compensate for any frequency and voltage deviation caused by using the droop method. A supplementary frequency Δf and a supplementary voltage amplitude ΔV are aggregated, respectively, with the original frequency and the voltage amplitude generated by ac-side power-sharing unit. Then, the reference generator block provides voltage references in a three-phase stationary frame. The next stage is an outer loop voltage control unit that assures the desired control characteristics of the output ac voltage. A set

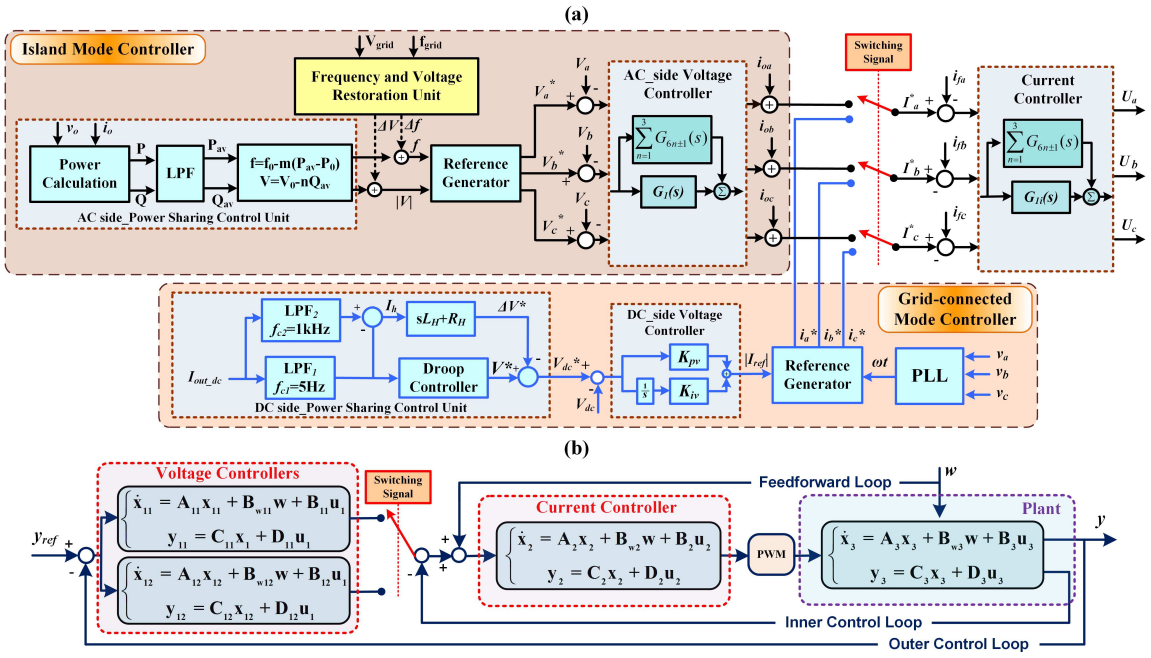


Figure 5.5: (a) Block diagram of the switched control system for the BICs. (b) Equivalent block diagram of the proposed switched control system for the BICs.

of parallel nonideal proportional-resonant (PR) controllers in the stationary frame is employed for tuning multiple harmonics with the resonant frequencies at ω_0, $5\omega_0$, $7\omega_0$, $11\omega_0$, and $13\omega_0$. The transfer functions of the nonideal PR controller is denoted by

$$G_h(s) = k_p + \sum_{h=6n\pm1} \frac{2k_{rh}\omega_c s}{s^2 + 2h\omega_c s + (h\omega_0)^2} \tag{5.13}$$

where h is the order of the harmonics. k_p and k_{rh} are the proportional gain representing the dynamic performance of the system and the resonant gain representing the phase shift of the system at the resonant frequency, respectively. ω_c is the cutoff frequency. The increase in the cutoff frequency diminishes the controller sensitivity to the frequency deviation, but also increases the tracking error. The controller coefficients are designed to meet the performance characteristics [96].

The outer loop voltage control unit provides the command references for the inner

loop current control unit. The inner loop, equipped with a set of parallel nonideal PR controllers, is aggregated to increase the internal stability of the voltage control loop and decrease the output impedance of the inverter. In addition, the output current signals are feedforwarded to the output of the voltage control unit to enhance the voltage control performance by eliminating the impact of load dynamics.

2) Grid-Connected mode: The BIC controller is designed to cooperate with the DGs in meeting the power demand of the dc side loads and regulating the dc bus voltage. Similar to the controller block diagram of the SC units, the power-sharing control consists of a dc and an oscillatory power-sharing unit. Two LPFs are employed to separate the dc and oscillatory components of the dc-link current. The dc and oscillatory power-sharing units specify, respectively, the amount of the dc and oscillatory power components that the BIC should share. The difference between the generated voltage signals from the dc and oscillatory units provides the dc bus voltage reference value, which can be given by

$$V_{dc}^{*} = V_n - [\frac{R_D\omega_{c1}}{s+\omega_{c1}} + \frac{s(\omega_{c1}-\omega_{c2})(R_H+sL_H)}{(s+\omega_{c1})(s+\omega_{c2})}]I_{out\_dc} \tag{5.14}$$

where V_n is the nominal dc voltage, and I_{out_dc} is the dc-link current. In the outer loop, the voltage control unit is equipped with a PI controller to ensure that the desired control characteristics of the dc bus voltage are obtained. The voltage control loop equation is given by

$$I_{ref} = K_p(V_{dc}^{*} - V_{dc}) + K_i \int (V_{dc}^{*} - V_{dc})dt \tag{5.15}$$

where K_p and K_i are the proportional and integral coefficients of the conventional PI controller. Then, a reference generator block is aggregated to provide the current references in the three-phase stationary frame. In addition, a PLL unit is integrated

to ensure the synchronization with the utility grid. The rest of the controller block diagram is the same as that of the controller of the island mode.

5.2.3 Stability Analysis

The main objective of this section is to analyze the asymptotic stability of the proposed switched control system for arbitrary switching signals. Fig. 5.5(b) shows the state-space model of the BIC with inner, outer, and feedforward control loops, in which there are two subsystems, i.e., subsystems in the grid-connected and hybrid ac/dc modes. The switching signal is the island detection signal, which assigns the most appropriate controller to ensure a desired behavior of the system. Based on the switched system principles, the continuous state is switched instantaneously to a new value once the system trajectory hits a switching surface.

Once the switching signal hits a switching surface, the topology of the system will change. Therefore, the new system topology has a different equilibrium point, and the trajectory of the system will be instantly driven away from the pre-switching toward post-switching equilibrium point. Then, the control strategy of the DGs and BICs detect the new condition, and the post-switching control strategy is activated to cope with it. The control framework should be able to maintain the system in the region of attraction of the equilibrium point. The transition between modes can have a detrimental and destabilizing effect on the system. Thus, the stability analysis for the switched control system is presented because the switching mechanism is either unknown or too complex.

To guarantee the asymptotic stability of a switched system for arbitrary switching signals, a necessary condition is that all of the individual subsystems should be asymptotically stable. However, this condition is not sufficient to guarantee the asymptotic stability of the overall system under arbitrary switching signals with the abrupt tran-

sition between different spaces [64]. The global uniform asymptotic stability should be obtained to ensure the asymptotic stability of a switched system for arbitrary switching signals. The most common approach is to identify a common Lyapunov function shared by the individual subsystems.

To define the closed-loop model of the system for different operating points, a state variable vector is assumed as $x = [x_1, x_2, x_3]^T$, in which the components, from right to left, are the state variable vectors of the voltage controller, current controller, and plant. All individual linear subsystems can be written by

$$\dot{x} = A_\sigma x, \quad \sigma \in \Upsilon \tag{5.16}$$

where the index set $\Upsilon = \{1, 2, ..., i\}$ is finite, and the matrices A_σ compacted in $\mathbb{R}^{n\times n}$ are stable (i.e., they are Hurwitz matrices). According to Fig. 5.5(a), the open-loop transfer functions of the system in the island and grid-tied modes are derived in (5.17) and (5.18), respectively. Theses transfer functions of the system can be converted into an equivalent state-space representation to identify the state matrix in each mode.

As shown in Fig. 5.5(b), the connection of three systems in series including a feedback loop and state models for each component can form a state model for the combined system. Therefore, according to a state model of the closed-loop system, the general form of the packed notation can be derived as follows:

$$G_1(s) = \frac{2k_{p1}k_{p2}s^4 + 4\omega_c[2k_{p1}k_{p2} + k_{p1}k_{r2} + k_{r1}k_{p2}]s^3 + 4[\omega_0^2 k_{p1}k_{p2} + 2\omega_c^2(k_{p1} + k_{r1})(k_{p2} + k_{r2})]s^2 + \underline{+4\omega_c\omega_0^2[k_{p1}k_{p2} + k_{p1}k_{r2} + k_{r1}k_{p2}]s + 2\omega_0^2 k_{p1}k_{p2}}}{(4L\omega_c + R + L)s^4 + 2(L\omega_0^2 + 2R\omega_c + 2R\omega_c^2)s^3 + (R\omega_0^2 + 4L\omega_c\omega_0^2 + 4R\omega_c^2)s^2 + \omega_0^2(L\omega_0^2 + 4R\omega_c)s + R\omega_0^4} \tag{5.17}$$

$$G_2(s) = \frac{2k_{p2}k_{pv}s^3 + (4\omega_c k_{p2}k_{pv} + 4\omega_c k_{v2}k_{pv} + 2k_{p2}k_{iv})s^2 + (4\omega_c k_{p2}k_{iv} + 4\omega_c k_{v2}k_{iv} + 2k_{p2}\omega_0)s + 2k_{p2}k_{iv}\omega_0^2}{Ls^4 + (R + 2\omega_c L)s^3 + (\omega_0^2 L + 2\omega_c R)s^2 + R\omega_0^2 s} \tag{5.18}$$

$$\mathbf{A}_\sigma = \begin{bmatrix} A_1 & 0 & -B_1C_3 \\ B_2C_1 & A_2 & -B_2\alpha - B_2D_1C_3 \\ B_3D_2C_1 & B_3C_2 & A_3 - B_3D_2\alpha - D_2D_1B_3C_3 \end{bmatrix} \tag{5.19}$$

where α is a subvector of the state vector of the plant representing a state used in the inner current feedback loop. Depending on the selected control unit (for $i = 1$, ... , n), there are a number of subsystems.

For a switched linear system, a quadratic common Lyapunov functions is naturally considered in which for some positive definite symmetric matrix, the following expression is obtained:

$$A_i^T P + P A_i = -Q \quad \forall i \in \Upsilon. \tag{5.20}$$

This formula is a system of linear matrix inequalities in P. A quadratic common Lyapunov function does not exist if and only if there are some nonnegative definite symmetric matrices satisfying (5.20), in which some should be non-zero matrices. The global uniform asymptotic stability of the switched system cannot guarantee that the common Lyapunov function is quadratic. However, a common Lyapunov function, which takes the piecewise quadratic form, always can be found to be homogeneous of degree two. An iterative procedure in [64] is used to achieve a quadratic common Lyapunov function for a finite family of commuting asymptotically stable linear systems.

The equivalent linear matrix inequality is expressed as

$$\begin{bmatrix} A_{\sigma i}^T P + P A_{\sigma i} & 0 \\ 0 & -P \end{bmatrix} < 0 \tag{5.21}$$

where P is a positive definite matrix. If there exists a quadratic common Lyapunov function that all the systems in this family share, the switched linear system in (5.16) is globally uniformly asymptotic stable. The system is characterized by the existence of a quadratic Lyapunov function.

$$V(x) = x^T P x. \tag{5.22}$$

The linear matrix inequality in (5.21) is solved by using the MATLAB Control System Toolbox to achieve the desired Lyapunov matrix P proving the quadratic stability of the system.

5.3 Test Cases

To evaluate the performance of the proposed resilient PnP decentralized control framework, the dc parking lot shown in Fig. 5.1 is simulated in PSCAD/EMTDC. Five DGs including two FC, one PV, and two SC units are integrated into the parking lot to provide the required power to the charging stations. To supply Level 2 and wireless EVs, three plug-in and three wireless charging stations are installed in the parking lot. The parameters used for the simulation studies are given in Table 5.1. The simulation studies are conducted on the parking lot during four different scenarios chronologically: connection of a DG, severe load transient, islanded from the utility grid, and disconnected from both BICs scenarios. The parameters of the controllers are listed in Table 5.2.

5.3.1 Time-Domain Simulation Results

Initially, the system is in the grid-tied state, and the three-phase unbalanced ac loads are completely supplied by the utility grid. Fig. 5.6 shows the active power wave-

Table 5.1: Parameters of DC Parking Lot

Parameter	Value
AC grid voltage	110 V
AC grid frequency	60 Hz
Rated power of BIC1	50 kVA
Rated power of BIC2	100 kVA
Switching frequency of BICs	8 kHz
Nominal dc-link voltage	400 V
Rated power of DG_1 & DG_5	50 kW
Rated power of DG_2	30 kW
Rated power of DG_3 & DG_4	15 kW

Table 5.2: Parameters of Controllers.

Controller	Parameters Value
FC Units	K_{pfc}=0.12, K_{ifc}=3
SC Units	K_c=10, K_{pSC}=0.2, K_{iSC}=200, K_{pcSC}=0.01, K_{icSC}=0.25
DC side voltage controller	K_{pv}=0.05, K_{iv}=1000
Voltage controller of BIC	k_p=1.5, k_{r1}=330, k_{r5}=1650 k_{r7}=2310, k_{r11}=3630, k_{r13}=4290, ω_c=1.5
Current controller of BIC	k_p=5.6, k_{r1}=240, k_{r5}=1200 k_{r7}=1680, k_{r11}=2640, k_{r13}=3120, ω_c=1.5
DC current sharing units static droop coefficients	R_{D1}=0.08, R_{D2}=0.16, R_{D3}=0.32 R_{D5}=0.08, R_{D-BIC1}=0.08, R_{D-BIC2}=0.04 Ω
Oscillatory current sharing units coefficients	L_{H-2}=19, L_{H-3}=60, L_{H-BIC1}=160, L_{H-BIC2}=160 μH

forms of the EV charging stations within the parking lot in four different scenarios. The active and reactive power waveforms of the three-phase unbalanced ac load are demonstrated in Fig. 5.7.

Stations 2, 5, and 6 are plug-in EV chargers, and Stations 1, 3, and 4 are wireless chargers. It can be inferred from Fig. 5.6 that the current oscillatory component (the double-frequency ripple) appears in the current waveforms of the plug-in charging systems. The double-frequency fluctuation is introduced in the presence of the single-phase plug-in EV charging stations and three-phase unbalanced ac loads. The power oscillations impose the double-frequency ripples on the dc bus voltage, as shown in Fig. 5.8. The dc bus voltage is regulated at 400 V.

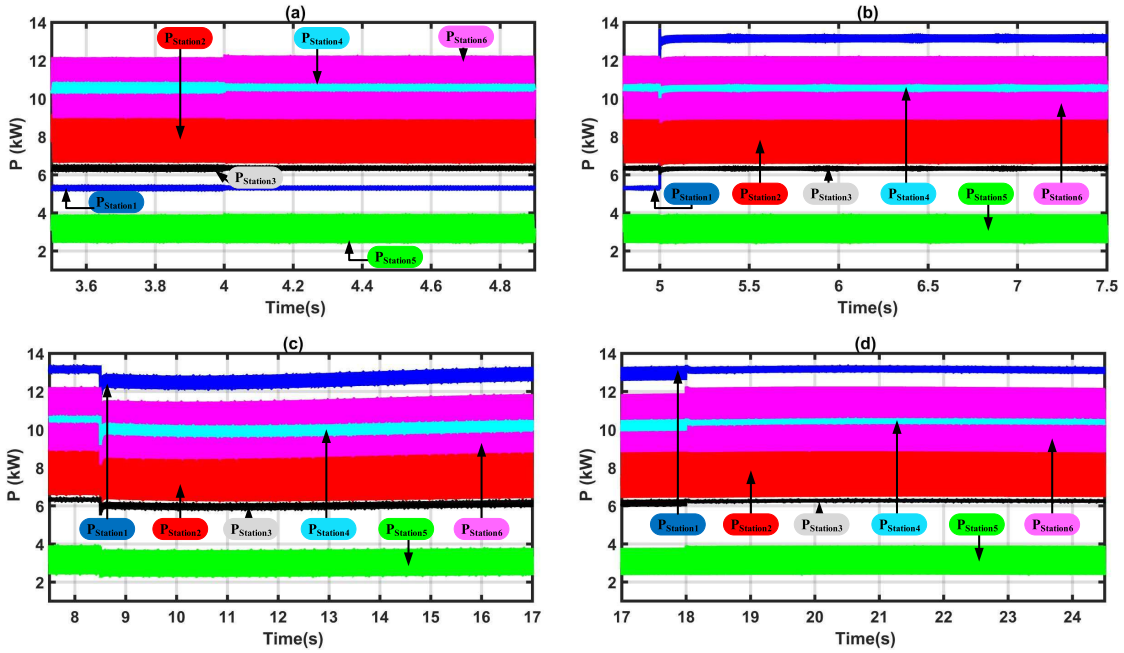


Figure 5.6: Dynamic response of the active power of the EV charging stations in different scenarios. (a) Connection of DG_3; (b) EV load change; (c) Islanding from the utility grid; and (d) Islanding from ac side.

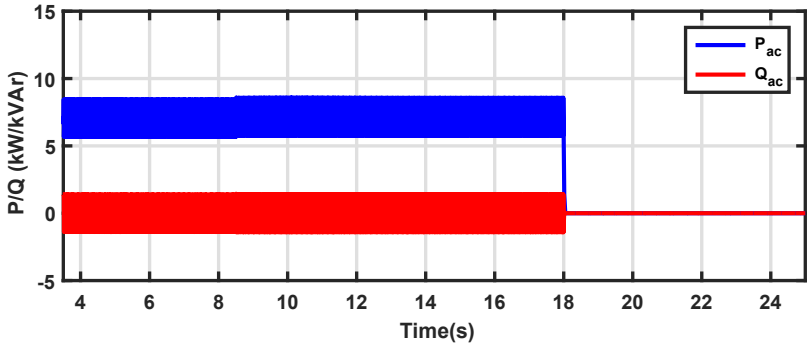


Figure 5.7: Dynamic response of the three-phase unbalanced ac loads including active and reactive power waveform.

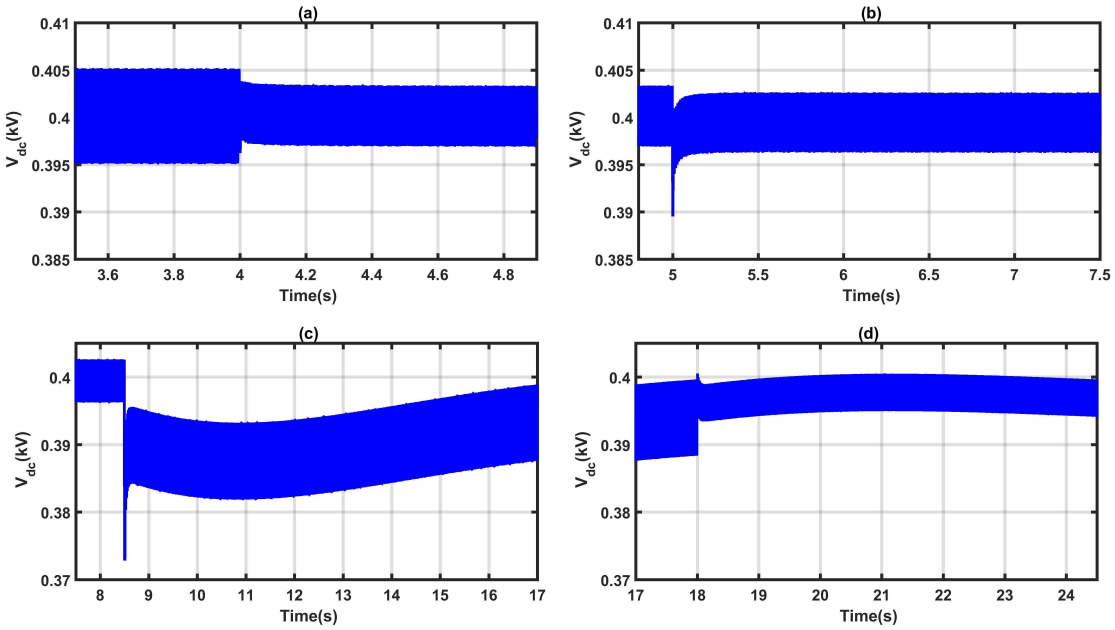


Figure 5.8: Dynamic response of the dc bus voltage in different scenarios. (a) Connection of DG_3; (b) EV load change; (c) Islanding from the utility grid; and (d) Islanding from ac side.

Figs. 5.9 and 5.10 illustrate the dynamic response of the DGs and BICs. The amount of power that the DGs release depends on their power rating, dynamic response, and the amount of power injected by the BICs. The FC units located at the DG_1 and DG_5 inject 8 kW and 7 kW into the dc bus, respectively. The SC units located at the DG_2 and DG_3 supply the demand for the power oscillatory component according to their oscillatory power-sharing coefficients. Using the maximum power point tracking technique, the PV units deliver 7 kW to the dc bus during the simulation studies. The BIC_1 and BIC_2 transfer, respectively, 6 kW and 12 kW from the utility grid to the dc bus according to the predefined droop coefficients as shown in Fig. 5.10. Although the rated power of the BIC_2 is twice that of the BIC_1, both BICs share an equal amount of the oscillatory power component based on their oscillatory power-sharing coefficients.

Scenario 1: The DG_3 is plugged into the dc parking lot at $t = 4$ s. The SC units in DG_3 play the role of auxiliary source and share the oscillatory power component.

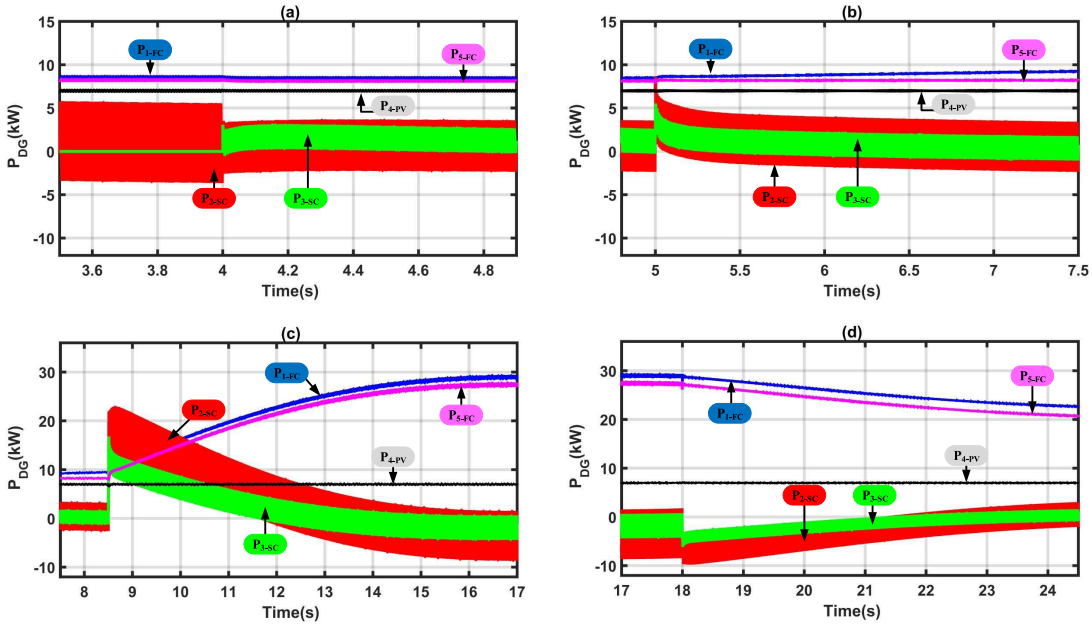


Figure 5.9: Dynamic response of the DGs including FC, PV, and SC units in different scenarios. (a) Connection of DG_3; (b) EV load change; (c) Islanding from the utility grid; and (d) Islanding from ac side.

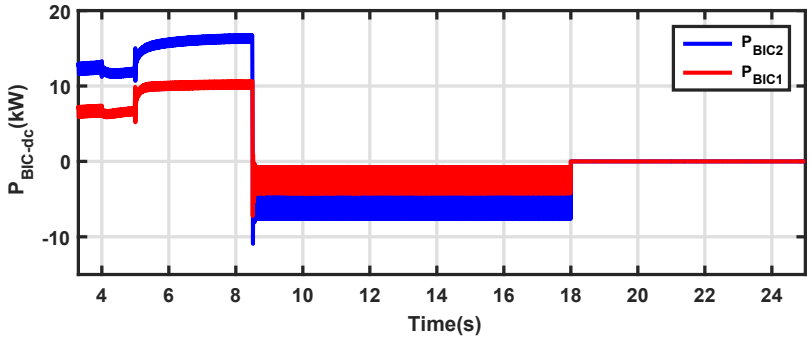


Figure 5.10: Dynamic response of injected active power of the BICs to the dc bus.

Although the dynamics of the DGs are different, the proposed control framework facilitates the PnP integration of the DGs without a need for a communication network. Once the DG_3 is connected to the parking lot power network, the dc bus voltage oscillation amplitude is reduced. In addition, the power oscillatory component is shared between DG_2 and DG_3 based on their rated power capacity. The control system is able to immediately coordinate the active power among the DGs and effectively provide dc-link voltage support.

Scenario 2: Several EVs connected to the charging station 1 are increasing the power demand from 5.3 kW to 13.2 kW at $t = 5$ s. The dc bus voltage is kept regulated in the range of less than 3% of the reference value, as shown in Fig. 5.8. Once a sudden power deficit occurs by the connection of several EVs, the proposed decentralized control strategy functions to compensate for the power mismatch. The FC units increase the output power according to their slow dynamic response. Meanwhile, the SC units are swiftly discharged to supply the power difference between the main power units and load demand. The power oscillatory component is shared mainly between the SC units, and the share of each unit is determined by the oscillatory current-sharing unit coefficients. Simultaneously, the BICs inject more power from the utility grid into the dc bus to assist in compensating for the power deficiency.

Scenario 3: The system is isolated from the utility grid at $t = 8.5$ s. The BICs alter their operation modes, and transfer a total of 7 kW from the dc bus to the ac side to supply the three-phase unbalanced ac loads. Hence, the DGs within the parking lot are required to generate more power to meet the power demand of the ac loads in addition to the charging stations. Furthermore, the dc bus voltage drops because the power generation from the utility grid is lost. The proposed control strategies for the DGs and BICs manage to keep the dc bus voltage regulated within 6% of its reference value. It is obvious that the oscillatory content of the dc bus voltage and

the DGs and BICs power waveforms are increased compared to the grid-connected mode. The FC units slowly start to increase their power level, and the SC units supply the transient power demand. The increase in the oscillatory power component is provided by the SC units, and the amount of the share depends on their capacities. In addition, the BICs share a portion of the oscillatory power component according to their rated capacities. Fig. 5.11 shows the dynamic response of the ac side of the BICs. The proposed control strategy provides a set of balanced sinusoidal voltages at the ac terminals as shown in Fig. 5.11(a). Before islanding from the utility grid, the voltage and current waveforms are balanced because the unbalanced ac loads are completely supplied by the utility grid. Once the islanding occurs, the BICs provide the power from the dc bus to the ac unbalanced loads. Figs. 5.11(b) and (c) show the current waveform of the BICs during the system isolation from the utility grid.

Scenario 4: The contactors of both BICs go off at $t = 18$ s. Accordingly, the need for power to supply the three-phase unbalanced ac loads is removed. This load disconnection reduces the power demand and a portion of the double-frequency ripples. The dc bus voltage steps up, and the FC units start to decrease their output power. The power difference between the main power sources and the EV charging stations charges the SC units. The simulation results verify the theoretical analysis and the effectiveness of the proposed control framework.

5.3.2 Hardware-in-the-Loop Verification Studies

This section presents the real-time performance of the proposed resilient PnP decentralized control framework in the hardware-in-the-loop setup, as shown in Fig. 5.12. The platform provides an interface with Matlab/Simulink for prototyping the power and controller systems in a closed-loop by using the loopback method. The detailed model of the parking lot is implemented by using the SimPowerSystems blockset and

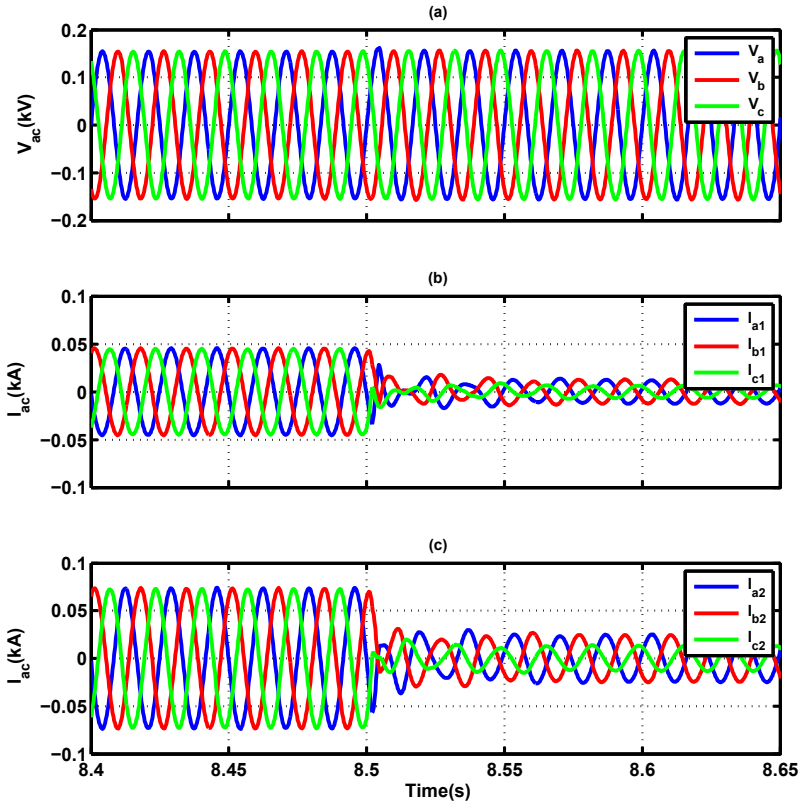


Figure 5.11: Dynamic response of the BICs. (a) Voltage waveforms of the ac side of the BICs. (b) Current waveforms of the BIC_1. (c) Current waveforms of the BIC_2.

the ARTEMiS RT plug-in. Then, the power system model is loaded on the OP5600 HIL testing equipment. A Virtex-6 FPGA chips with time steps as low as 290 ns performs the data acquisition and I/O management. The FPGA OP5142 supports the accurate embedded solvers and provides the required computational power to run power electronics models. On the other hand, the controller system is implemented in the supervision unit. The proposed control framework is implemented in the CPU with a clock speed of 3.46 GHz. The real-time control signals are exchanged between the hardware in the loop simulator and supervision unit through CAT5 cables. The results are captured on a 500-MHz four-channel oscilloscope. The measurements and commands are updated every 10 μs. The parameters of the test system are given in Table 5.1.

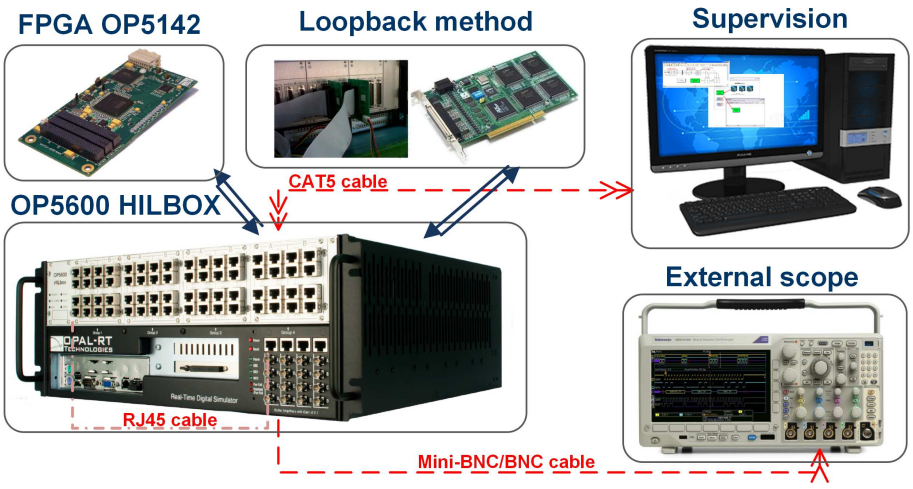


Figure 5.12: Real-time platform for dc parking lot hardware in the loop testing.

The change in the operation mode of the BICs and DGs during islanding can result in severe system voltage fluctuations and instability problems. The dynamic response of the system during transitions from the grid-tied to island state is shown in Fig. 5.13. Initially, the DGs and BICs regulate the parking lot bus voltage at 400 V in the grid-connected mode. Each SC unit provides a portion of the oscillatory power component based on its oscillatory power-sharing coefficients. The FC units inject a total amount of 19 kW into the dc bus. In addition, the PV units consistently deliver a constant power to the dc bus. The BICs transfer the power from the utility grid to the dc bus according to the predefined droop coefficients. Furthermore, the BICs share an equal amount of the power oscillatory component according to their oscillatory power-sharing coefficients.

Once the utility grid is disconnected from the main feeder, the dc bus voltage steps down. The proposed control strategy maintains the dc bus voltage deviation within 6% of its reference value. To supply the ac load power demand, the island control mode of the BICs is activated. Accordingly, the DGs need to produce more power to meet the additional power demand from the ac side. The DG_2 and DG_3 provide the transient power demand. In addition, the oscillatory component is shared between

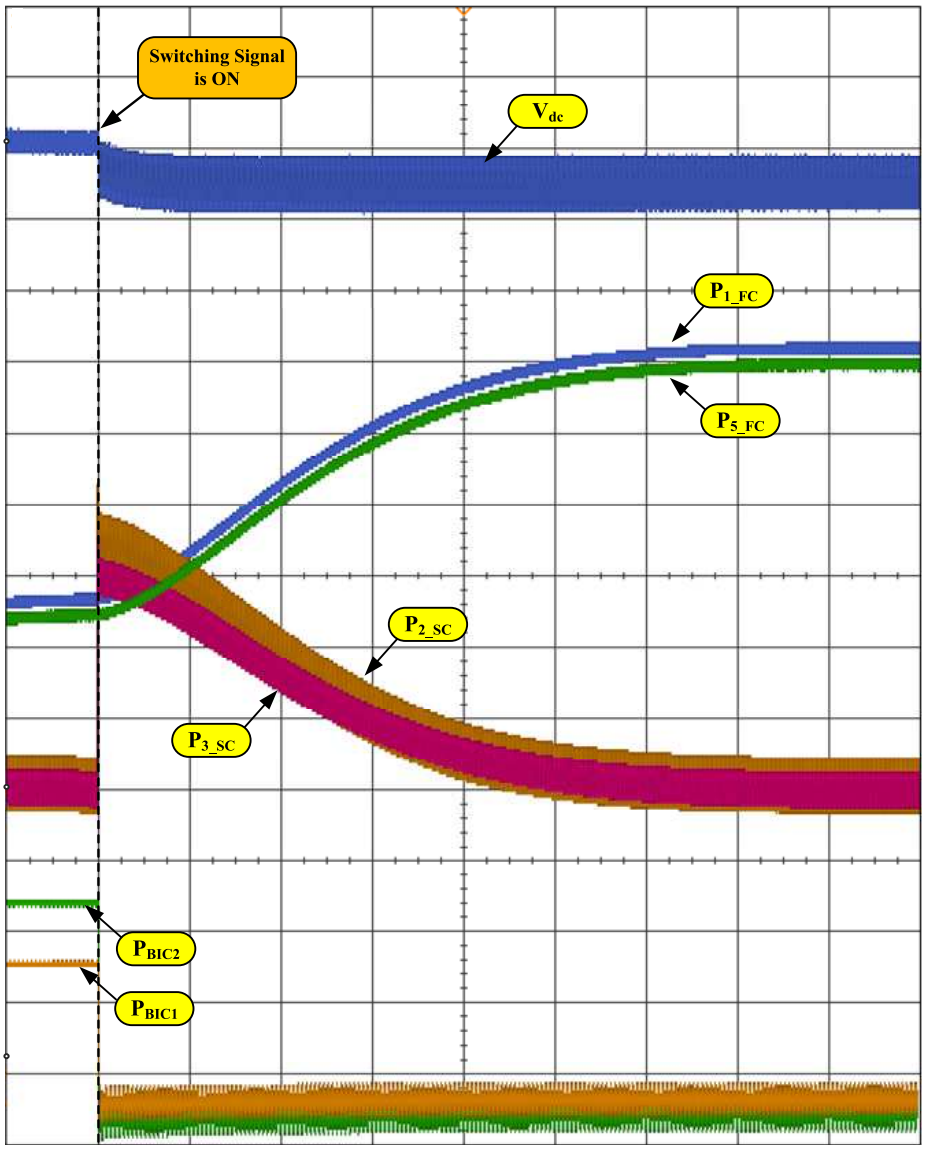


Figure 5.13: Measured results of the system during transition from grid-connected to islanded state with the proposed control framework. [Time: 1 s/div, dc-link voltage: 15 V/div, active power of the DGs (channels 1-4): 5 kW/div, active power of the BICs (channels 1-2): 10 kW/div].

them based on their oscillatory power-sharing coefficients. Meanwhile, the DG_1 and DG_5 start to increase their output power according to their slow dynamic responses. Each BIC changes its operation mode from the rectifier to inverter mode to allow the power flows from the dc bus to the ac side. Because the dc bus of the parking lot must additionally supply the unbalanced ac load in the island mode, the oscillatory

power component and, consequently, the double-frequency of the dc bus voltage are increased. The results obtained from the hardware-in-the-loop platform are in good agreement with the simulation results and theoretical analysis.

5.4 Configuration of Smart DC Home

The smart dc home under study is composed of hybrid FC/SC power sources, a rooftop PV panel, home appliances modeled as dc and ac loads, and an electric vehicle charging station. The dc home structure, as an low-voltage dc (LVDC) system basically formed around the common dc bus, is shown in Fig. 5.14. The hybrid FC/SC power system includes the FC stacks to provide the main power through a unidirectional dc/dc converter and the SC modules to support the transient response of the main power source through a bidirectional dc/dc converter. A rooftop PV unit with a unidirectional dc/dc converter is connected to the common dc bus, functioning as an auxiliary power source. The smart dc home is interfaced to the utility grid via a new fault-tolerant MMC topology providing a bidirectional exchange of energy between the dc bus and the utility grid.

An MMC equipped with fast, low-voltage, and low-resistance metal-oxide semiconductor field-effect transistors (MOSFETs) provides a superior performance in LVDC applications. Compared with conventional two- or three-level inverters, the MOSFET-based MMCs offer low filter cost and size, simple realization of redundancy, and low switching losses. According to the detailed analysis of the efficiency, the MOSFET-based MMCs demonstrate a superior performance in the low power range, so that they are the most suitable option in applications like those in smart dc homes [3, 65, 103].

A schematic diagram of the new MOSFET-based MMC is demonstrated in Fig. 5.15. Each leg of the MMC consists of two arms, and each arm hosts N identical modular

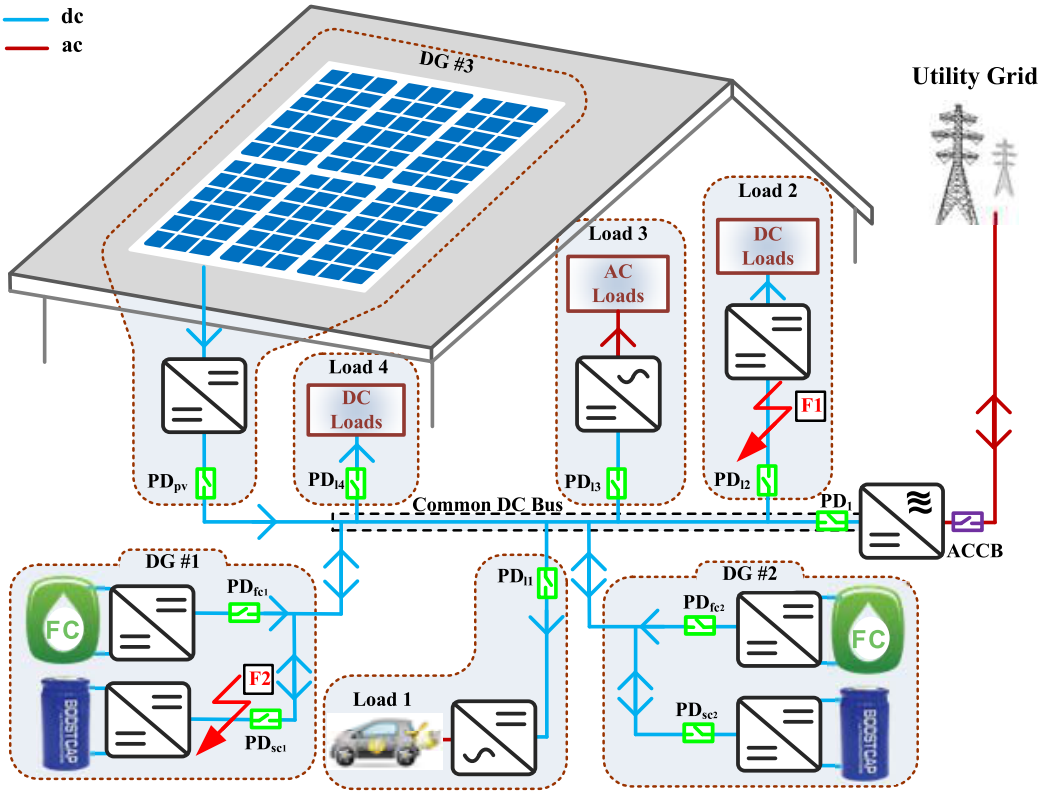


Figure 5.14: Smart dc home configuration.

SM circuits. The proposed SM offers a number of parallel current paths through the capacitors inside the converter. Accordingly, this feature decreases the output impedance of the circuit, enhances the efficiency, and ensures a high current-delivering capability [90, 104]. In addition, the proposed SM can be embedded in the MMC structure without changing the control strategy. Depending on the switching status, each SM generates up to three voltage levels. The enhanced reliability, modular design, and dc fault-handling capability of the new MMC structure contribute to the improved power quality of the dc home system.

The connection points of each segment to the common dc bus and dc-side of the MMC are equipped with protection devices (PDs), which contribute to the ability of the platform to block the faulty segment once a dc fault occurs. Large time constants and long breaker operation are some drawbacks of mechanical circuit breakers

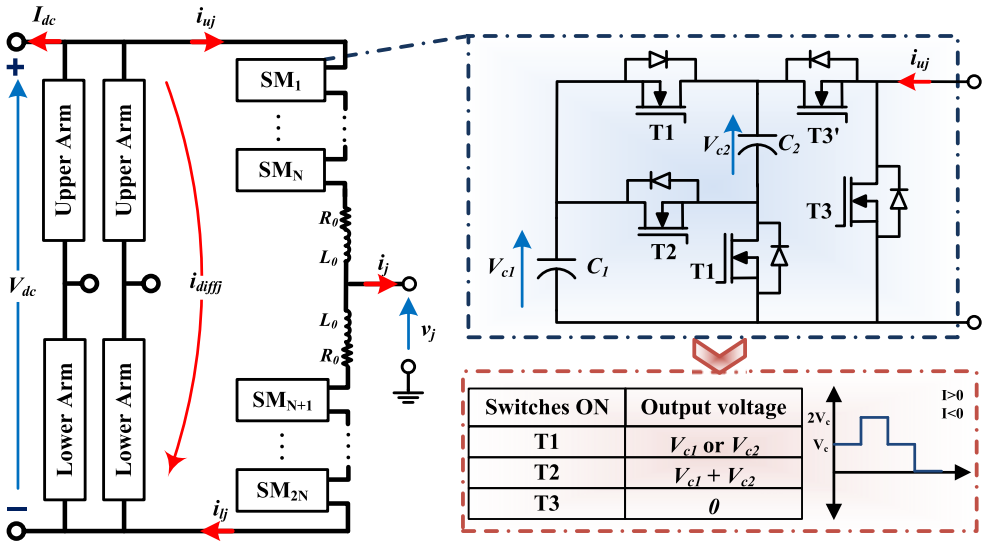


Figure 5.15: Circuit diagram of the MMC and structure of fault-tolerant SM circuit.

and fuses. A large time constant for a PD prolongs the fault-clearing time in the protection system. Therefore, fast-acting solid-state circuit breakers were designed to provide significant advantages in terms of the functionality and speed of operation, typically 50-250 μs, for use within dc systems [82, 83, 105, 106]. The behaviors of the various solid-state circuit breaker topologies have significant differences. Accordingly, choosing among the topologies is application-dependent and demands a cost-benefit analysis. A PD consists of a solid-state circuit breaker, snubber circuit, processor for setting the thresholds, and current sensor to measure the current. The PDs are controlled by the FSI technique to identify and isolate faulty segments by using the information extracted from the local current sensor.

5.5 Principles of Control and Protection Strategies

This section explains how the principles of the proposed DCC and FSI methods ensure a stable and reliable operation of the dc home in severe power unbalance and dc fault conditions.

5.5.1 Decentralized Cooperative Control Method

The control block diagram of the smart dc home is shown in Fig. 5.16. The DCC strategy based on local measurements is presented to achieve an effective power balance among the components of the dc home without the need for communication. The dc home, equipped with the DCC method, supplies the total energy demand in the off-grid mode, and effectively manages the energy consumption in both the on- and off-grid modes.

In the hybrid FC/SC unit, the FC system regulates the FC current and also controls the hydrogen flow according to the FC current. The FC converter employs a proportional-integral (PI) controller to provide the power demand at a regulated dc bus voltage. As shown in Fig. 5.16(a), the current limiter is included to ensure the operational limits and guarantee the safe operation of the FC unit. Also, a current slope limitation block is integrated into the FC control loop to avoid the fuel starvation phenomenon [107]. To control the hydrogen flow, the hydrogen reference is defined as

$$q_{H_2}^{ref} = \frac{2k_c}{U_o} I_{FC} \tag{5.23}$$

where I_{FC} is the output current of the FC stack, k_c is a modeling constant (kmol/(sA)), and U_o is the optimal fuel utilization rate, which is typically between 80% and 90%. The reformer unit is integrated to produce the required hydrogen from methanol. A PI controller is employed to control the hydrogen flow according to the FC current within the optimal fuel utilization range. In transient operations, the slow dynamic response of the FC stack poses a threat to the system performance. Hence, the SC unit in the hybrid FC/SC configuration plays the key role of the complementary power source, which is discharged or charged to compensate for the power difference between the supply and demand. Because of the high power density and fast dynamic response, the SC unit is also able to supply the high-frequency current component.

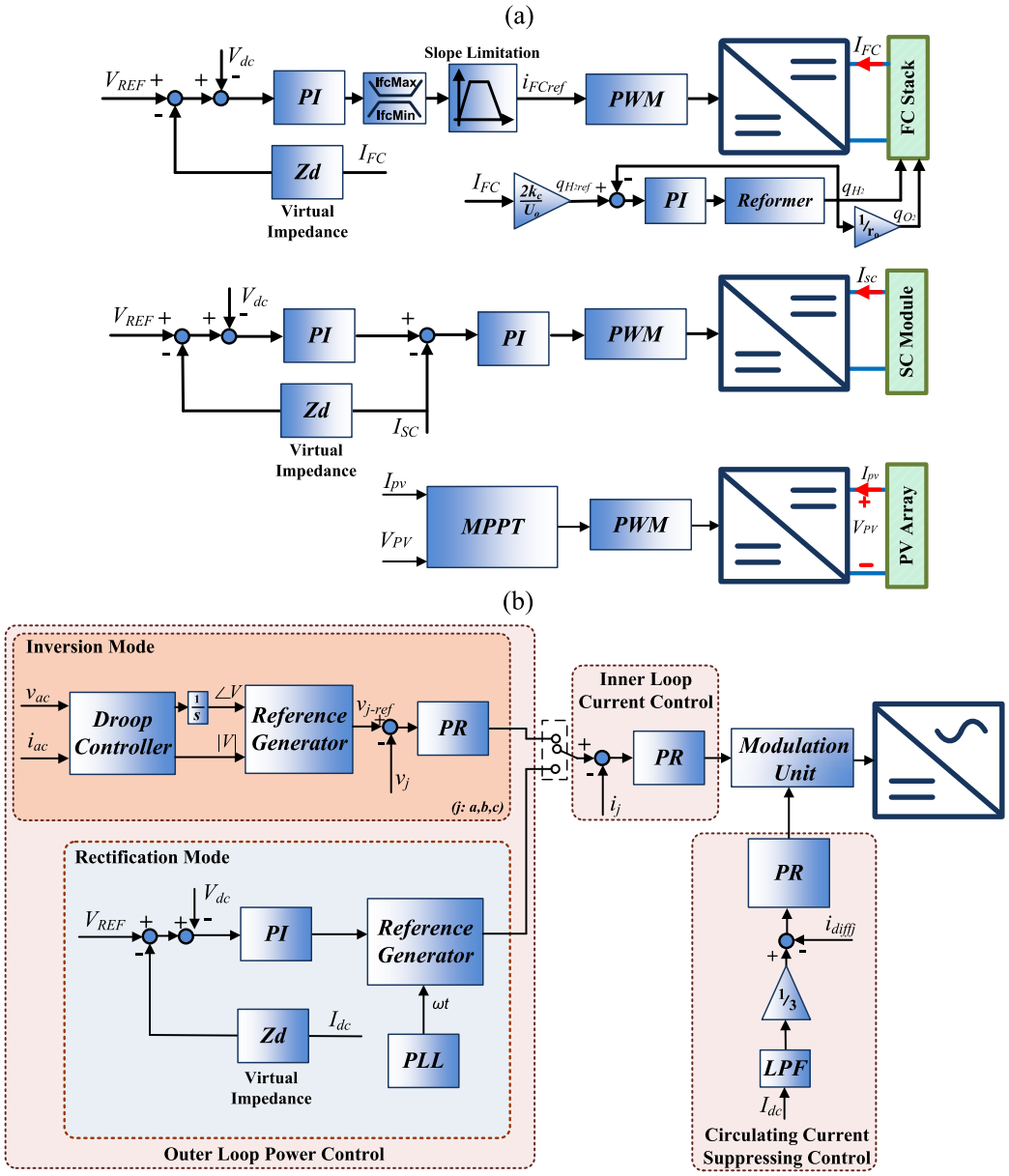


Figure 5.16: Control diagram of (a) the DGs including control blocks for hybrid FC/SC and PV units, (b) the MMC including the outer loop power, inner loop current, and circulating current suppressing controls.

A significant feature of the hybrid FC/SC power system is that the controller of each power unit is designed based on feedback from its local signals and not from the power unit next to it. As a consequence, each system can maintain its operation even if a fault occurs in each of the FC or SC units. In addition, the unidirectional

power flow of the FC converter results in decoupled dynamics for the FC and SC units. To ensure accurate current sharing among the hybrid FC/SC systems and MMC according to their nominal capacities, the voltage droop controller of the FC and SC units is equipped with virtual impedances. A virtual impedance assigns the output impedance value to each power unit to share a specific amount of the dc and high-frequency current components. The PV unit controller is designed to operate in the maximum power point tracking mode.

The block diagram of the proposed control strategy for the interlinking converter is shown in Fig. 5.16(b). The outer loop power, inner loop current, and circulating current suppressing controls are the three main control loops of the MMC controller. The outer loop power control generates the current reference for the inner loop current control block and can operate in either the inversion or rectification mode, depending on the state signal. For the outer loop power control in the inversion mode, the droop controller allows the MMC to share the power demand of the grid side by drooping its output reference voltage magnitude and frequency. The difference between the phase voltage reference and measured value is processed by a nonideal PR controller to ensure the desired control characteristics of the output ac voltage. The transfer function of the nonideal PR controller with the resonant frequency at ω is denoted by

$$G_h(s) = k_p + \frac{k_r \omega_c s}{s^2 + \omega_c s + \omega^2} \tag{5.24}$$

where ω_c is the cutoff frequency. k_p and k_r are the proportional and resonant gains at the resonant frequency, respectively. The controller coefficients are designed to meet the performance characteristics. For the outer loop power control in the rectification mode, the dc voltage controller is equipped with a virtual impedance, in which the

common dc bus voltage is given by

$$V_{dc}^{*} = V_{REF} - I_s Z_d \tag{5.25}$$

where V_{REF} is the dc bus voltage reference, I_s is the dc current of the respective power source, and Z_d is the virtual impedance of the droop control loop. The integration of the virtual impedance unit into the control loops of each converter guarantees accurate dc and high-frequency current sharing among converters. The dc bus voltage controller provides the desired control characteristics of the dc bus voltage through a PI compensator. Next, the generated current reference is fed to the inner loop current control block. The inner loop current control employs a nonideal PR controller in the stationary *abc* reference frame. To design the controller parameters, the dynamic model of the MMC plant from the inner current controller perspective is given by

$$e_j(s) - v_j(s) = \frac{L_0 s + R_0}{2} i_j(s) \tag{5.26}$$

where e_j is the inner imaginary voltage, v_j is the converter output voltage, and i_j is the line current in phase j. L_0 and R_0 denote the arm inductance and equivalent arm resistance, respectively. In the inner loop current control block, the line current is controlled by an inner imaginary voltage. Furthermore, the MMC control system is equipped with another current control loop to control the circulating current. This loop includes a LPF and PR controller. The dc bus current is processed by the LPF to eliminate the double line-frequency and high-order harmonics from the measured signal. A nonideal PR controller regulates the circulating current of each phase. From the circulating current controller perspective, the dynamic model of the MMC is expressed as

$$v_{diffj}(s) = (L_0 s + R_0) i_{diffj}(s) \tag{5.27}$$

where v_{diffj} and i_{diffj} are the inner unbalanced voltage and current of the MMC in phase j, respectively. In the circulating current suppressing control block, the inner unbalanced current is controlled by an inner unbalanced voltage. At the final stage, the modulation unit generates the switching signals for the MMC switches based on the outputs of the inner loop and circulating current suppressing controls [88]. The proposed DCC method operates as an intelligent control system to facilitate power management among different resources and the MMC without any need for communication and improves the overall performance and flexibility of the system.

5.5.2 Fault Segment Identification Scheme

A dc short circuit fault may result in the most severe conditions for the dc home system. Once a dc fault occurs, the power switches of the MMC are blocked, and the charged capacitors within the system immediately start feeding the fault. The high fault current and dc bus voltage drop happen in the presence of charged capacitors and low impedance wires in the fault path. Unlike ac systems, LVDC systems lack standards for fault protection. The International Standard IEC 61660-1 is the most widely used standard for short-circuit current characterization in dc systems [108]. According to this standard, the rectifier bridge, stationary batteries, smoothing capacitors, and dc motors are the main dc fault sources. The total short circuit current is the sum of the partial short circuit currents for each of those sources and is derived as

$$i(t) = \begin{cases} i_p \frac{1-e^{\frac{-t}{\tau_1}}}{1-e^{\frac{-t_p}{\tau_1}}}, & 0 \le t \le t_p \\ i_p[(1-\frac{I_k}{ip})e^{\frac{t_p-t}{\tau_2}} + \frac{I_k}{i_p}], & t_p \le t \le T_k \end{cases} \tag{5.28}$$

where i_p and I_k are the peak and quasi steady-state short-circuit currents, respectively. t_p is the time to peak, τ_1 is the rise time constant, and τ_2 is the decay time

constant. T_k represents the fault duration time. The International Standard IEC 61660-1 represents an approximate dc short-circuit current in auxiliary dc systems. The fault current of each source is multiplied by a correction factor to improve the conservative result of the total short-circuit current. The corrective factors of the Standard IEC 61660-1 need to be adapted for the LVDC configuration to ensure accurate calculation of the short-circuit current [109].

To protect the sensitive power electronic components from a high fault current, faults must be immediately identified and isolated before the dc bus voltage drops to zero and becomes negative. The fault current contains the required information to reveal the exact location of a faulty segment. Once a dc fault occurs in the system, the comparison among the current waveforms of different segments indicates that the current of a faulty segment will increase rapidly. The primary goal in the proposed protection algorithm is to quickly identify the faulty segment by analyzing the measured current of each segment. Accordingly, PDs continuously monitor the current of each segment to reveal the location of the faulty segment. Once a dc fault occurs in the dc home, a trip signal is sent to the PD in the corresponding segment to restrain the fault. Therefore, the power flow in the rest of the network can be maintained. Fig. 5.17 shows the equivalent circuit of a faulted network and the PD architecture, where each PD is equipped with the FSI scheme to isolate the faulty segment without the need to coordinate the PDs.

To be able to make a timely response, the FSI algorithm processing unit continuously compares the measured current value with a threshold setting. A necessary condition to define a threshold setting is that the FSI scheme must detect the fault location and isolate it before the dc fault totally de-energizes the dc bus. Furthermore, the threshold value should be large enough to avoid unnecessary trips due to other types of disturbances in the dc systems. In the proposed algorithm, the thresh-

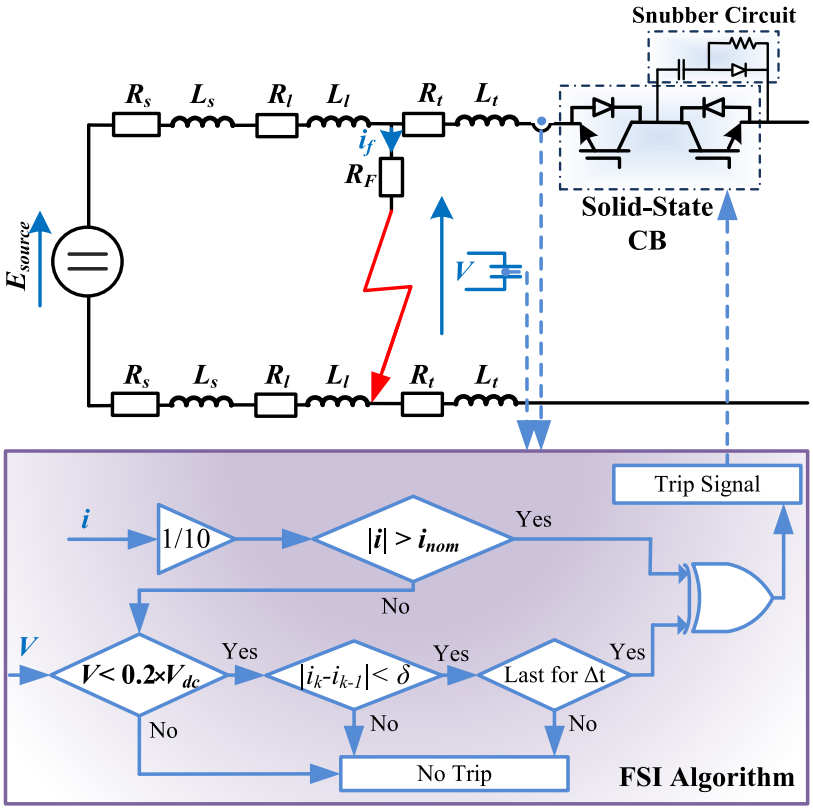


Figure 5.17: Equivalent circuit of faulted network, and PD including solid-state circuit breaker, snubber circuit, and proposed FSI algorithm processing unit.

old value is defined as ten times the maximum rated current. In normal operation, the difference between the measured current value and the maximum rated current of the system is within an acceptable range. When a dc fault occurs, the measured current will quickly exceed the threshold value. Once the instantaneous magnitude of the current in a segment is greater than the predefined threshold value, the FSI scheme determines the fault location. Accordingly, the trip signal is sent to the PD of the respective faulty segment. The proposed protection algorithm can immediately identify multiple and simultaneous faults within the dc home without the need for communication.

The proposed FSI scheme is structurally vulnerable due to its strong reliance on the information provided by the current sensor. To enhance the resilience of the PD

against any fault in the current sensor, other conditional statements are included in the FSI algorithm. The new command line assists in initiating the trip signal if a dc fault occurs within a segment, and the current sensor of the respective PD is broken. This process relies on the fact that the fault occurrence affects the current waveforms of all segments connected to the dc bus. The two possible fault cases are (1) both sensor breakdown and dc fault occurrence in the corresponding segment and (2) only a dc fault occurrence. In the former case, the instantaneous magnitude of current in the faulty segment violates the first conditional statement of the FSI algorithm. Relying on the fact that the dc fault causes rapid de-energization of the dc bus, the second conditional term will be met. After detecting severe voltage drop, the next conditional statement will show an unusual fixed current because the current sensor is broken. δ, the predefined threshold setting, is set at a small value to notify of any changes in the current magnitude of the corresponding segment. It can be inferred that the fault occurrence in a segment with a faulty current sensor shows a severe voltage drop along with an unusual fixed current. However, the current sensor of a non-faulty segment might be broken. Hence, a time delay, in order of 100 μs, is integrated into the algorithm to avoid unwanted trips. If severe voltage drop and unusual fixed current conditions continue after the specified time interval, the FSI algorithm detects the respective segment as a faulty one with a broken current sensor. This part of the proposed FSI algorithm ensures the reliable operation of the PD even when there is a faulty current sensor. In the latter case, the FSI scheme immediately determines the fault location by analyzing the segment current, and commands the corresponding PD to isolate the faulty segment.

The proposed FSI scheme eliminates the need for unreliable communication channels between the protection units. Its use of only the local measurements from the control unit reduces costs. On the other hand, the use of local measurements elim-

inates the latency in the operation of PDs. The FSI algorithm ensures the reliable operation of the PD even in the presence of a fault in the current sensor. Accordingly, the proposed protection scheme improves the service quality by making the fault isolation process significantly fast and reliable.

5.6 Test Cases

A dc home, with the structure shown in Fig. 5.14, is implemented in PSCAD/EMTDC simulation software to evaluate the performance of the proposed DCC method and FSI scheme. The ac power is transfered to dc power through the new MMC in the grid-tied mode. Furthermore, the DGs are deployed to ensure reliable power generation in the on- and off-grid modes. According to the residential building codes, a low-resistance 12 AWG is chosen for wiring most of the smart home circuits. The home is equipped with a typical 200 A breaker panel, and the nominal dc bus voltage of the dc home is regulated at 380 V. The increase in the MMC output voltage levels reduces the losses at the expense of increased complexity. Hence, an MMC with ten SMs per arm is employed to maintain the advantages over two- and three-level counterparts. The parameters of the dc home are listed in Table 5.3. Four different simulation scenarios are designed to evaluate the performance of the proposed DCC method and FSI scheme in the dc home: load change, dc fault in a load segment, dc fault in a DG segment, and transition from the grid-tied to off-grid mode.

5.6.1 Time-Domain Simulation Results

Fig. 5.18 shows the performance of the dc home when two simultaneous load changes happen at $t = 3$ s. The double-frequency current fluctuation is introduced in the presence of the single-phase converter of the EV charging station and ac loads. As

Table 5.3: System Parameters of DC Home

Representation	Parameter Value
DC bus Voltage	380 V
MPPT voltage	70-150 V
Rated Power of MMC	15 kW
Number of SMs per arm	10
Capacitance of SM capacitor	2000 μF
Arm inductance	1.5 mH
Rated power of FC unit of DG_1	12 kW
Rated power of SC unit of DG_1	14 kW
Rated power of FC unit of DG_2	12 kW
Rated power of SC unit of DG_2	12 kW
Rated power of PV unit of DG_3	8 kW
Wire resistance (per foot)	1.6 mΩ
Wire inductance (per foot)	0.35 μH
Cross-sectional area of wire	3.3 mm^2

a consequence, the load oscillations impose double-frequency ripples on the dc bus voltage, as shown in Fig. 5.18(a). Fig. 5.18(b) presents the current waveforms of the load segments in a dc home. Subsequent to the load change in load$_2$ and the disconnection of load$_3$, the magnitude of the high-frequency ripple on the dc bus voltage is reduced. The SM capacitor voltages of the upper and lower arms of the MMC under the load changes are shown in Figs. 5.18(c) and (e). The control unit ensures a highly dynamic performance with the proven capability to balance the capacitor voltages of the MMC. The dynamic responses of the MMC and DGs are demonstrated in Fig. 5.18(d). Due to the slow dynamic response of the FC stack, the DCC changes the interlinking converter power setting to meet the dc bus power demand without changing the FC operating point. Relying on the high power density and fast dynamic response of the SC units, they are charged to compensate for the power difference between the supply and demand. Due to the higher current rating of the SC$_1$, it shares more dc and high-frequency current components than the SC$_2$. The virtual impedance of the MMC is designed to contribute more to the dc current component than the high-frequency component. Fig. 5.18(f) shows the internal current

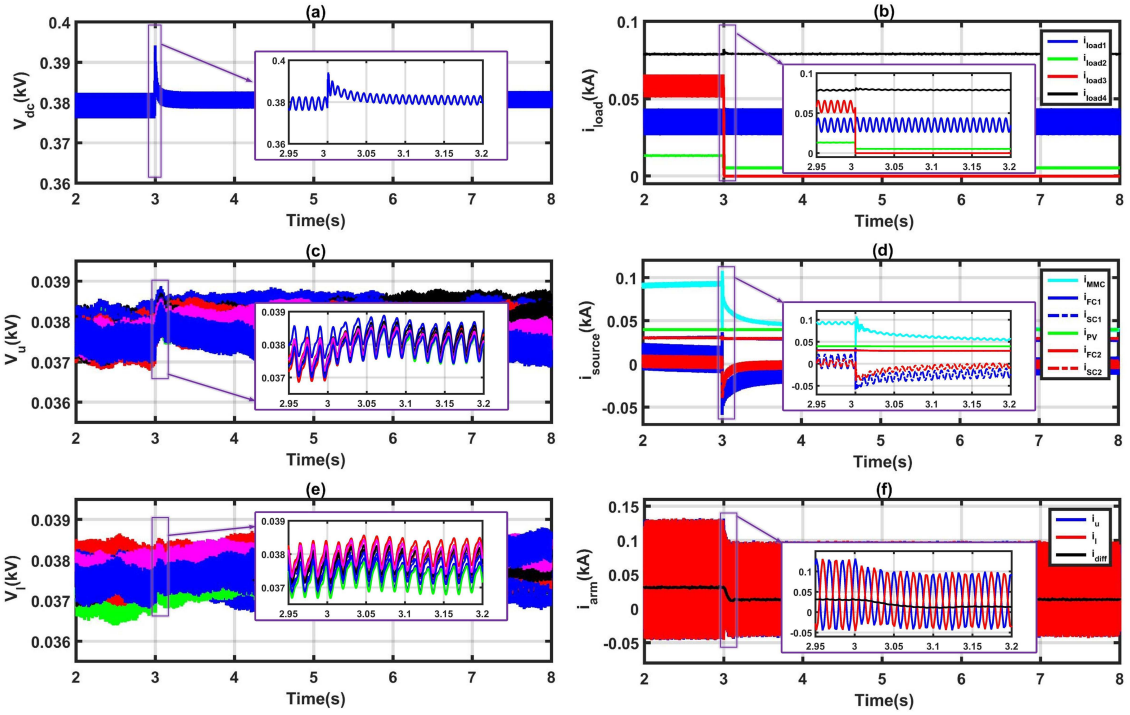


Figure 5.18: Dynamic response of the dc home subsequent to sudden load changes. (a) DC bus voltage; (b) Current of dc and ac loads; (c) SM capacitor voltages of the upper arm of phase b; (d) Output current of the MMC and DGs; (e) SM capacitor voltages of the lower arm of phase b; and (f) Waveforms of upper arm, lower arm, and circulating currents.

waveforms of phase b of the MMC. Because the power transfer from the grid to the dc bus is reduced, the circulating current and arms currents are reduced accordingly to adjust the output power of the MMC to the new setpoint.

The dynamic response of the dc home when a fault occurs in the load$_2$ segment is shown in Fig. 5.19. The dc bus voltage drops to 20 V for less than 1 ms, and a high fault current is yielded subsequent to the fault occurrence. The proposed FSI scheme is able to identify and isolate the fault location before the dc fault totally de-energizes the dc bus. The increase in the fault-clearing time can result in a larger voltage transient, which impacts the assets connected to the other feeder. Based on the FSI scheme, the current magnitude in each segment is continuously compared with the threshold setting. Once the current value in PD$_{l2}$ unit exceeds the threshold, the FSI algorithm generates a trip signal for the respective PD to isolate the fault in

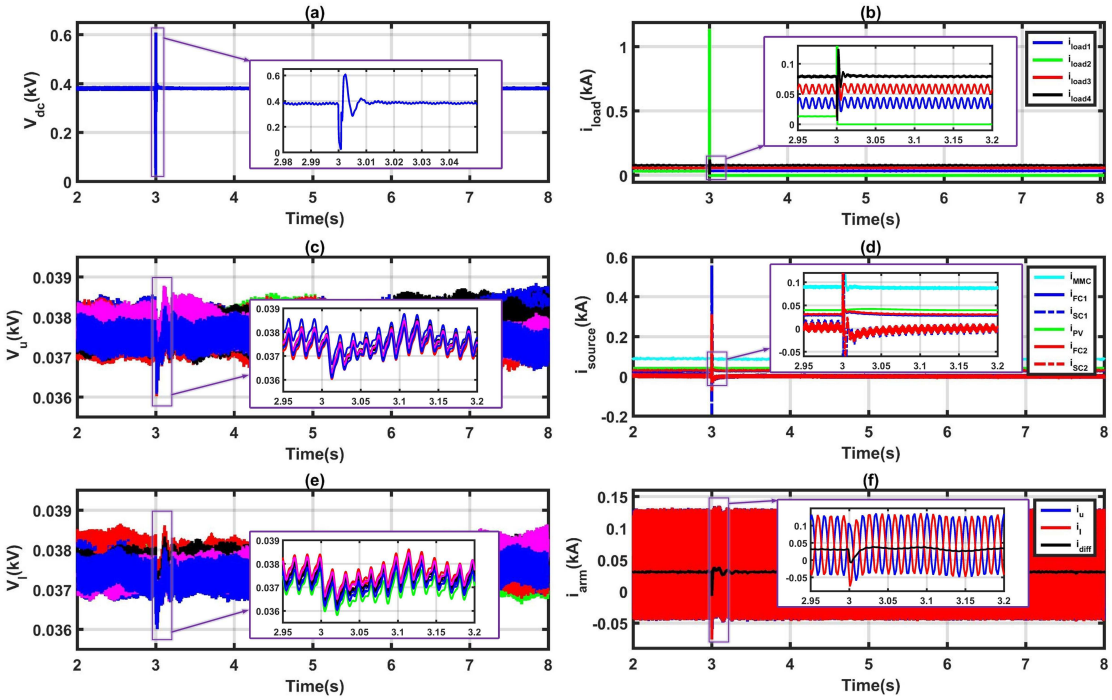


Figure 5.19: Dynamic response of the dc home in case of dc fault in load$_2$ segment. (a) DC bus voltage; (b) Current of dc and ac loads; (c) SM capacitor voltages of the upper arm of phase *b*; (d) Output current of the MMC and DGs; (e) SM capacitor voltages of the lower arm of phase *b*; and (f) Waveforms of upper arm, lower arm, and circulating currents.

the load$_2$ segment. Figs. 5.19(c), (e), and (f) show the internal dynamics of the MMC during the fault conditions. The SC units are charged to maintain the power balance in the dc home. The DCC method consistently ensures the dc bus voltage regulation and high-frequency and dc current components sharing among the DGs and MMC.

Fig. 5.20 shows the dynamic response of the dc home when a fault occurs in the DG$_1$ segment. Because the output current of the SC unit in the steady state is zero, the dc bus voltage overshoot in this scenario is less than that of the dc fault in the load segment. According to the proposed FSI scheme, when a segment output current exceeds the threshold, a trip signal is sent to the corresponding circuit breaker. Therefore, the PD$_{sc1}$, equipped with the FSI algorithm, isolates the fault in less than 1 ms, before the dc bus voltage drops to zero. Similar to the previous fault scenario in the load segment, the dc bus voltage regulation and current sharing among the

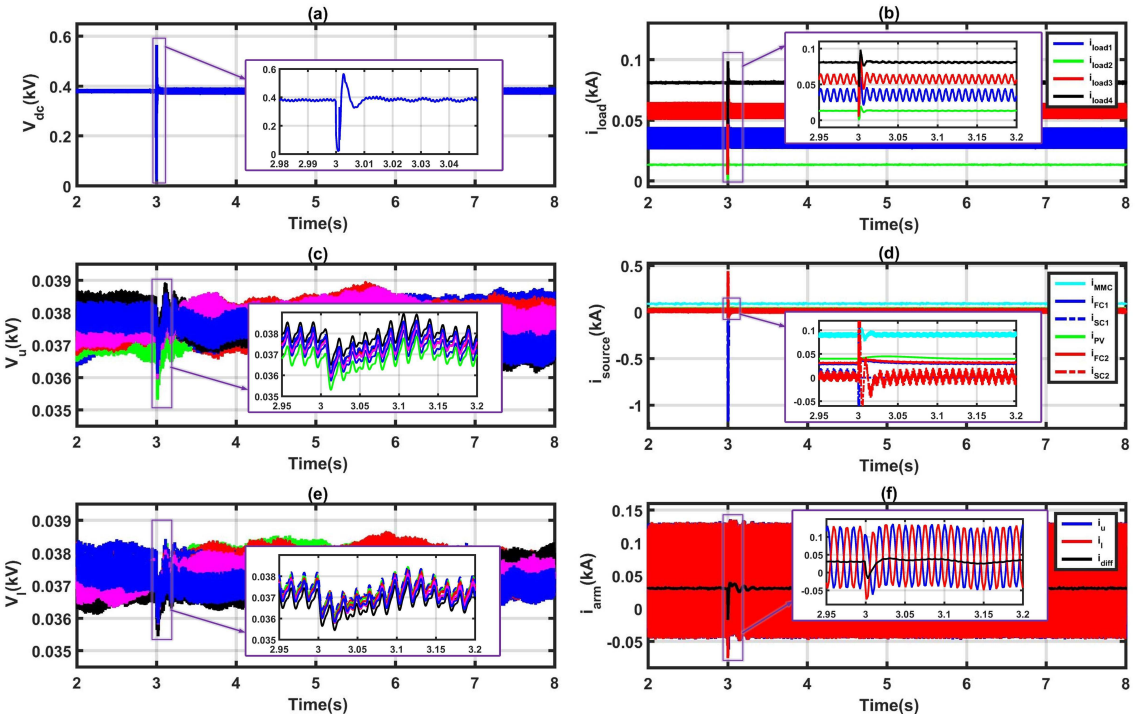


Figure 5.20: Dynamic response of the dc home in case of dc fault in DG_1 segment. (a) DC bus voltage; (b) Current of dc and ac loads; (c) SM capacitor voltages of the upper arm of phase *b*; (d) Output current of the MMC and DGs; (e) SM capacitor voltages of the lower arm of phase *b*; and (f) Waveforms of upper arm, lower arm, and circulating currents.

MMC and DGs are ensured through implementing the proposed DCC method.

The dc home is isolated from the utility grid at $t = 5$ s. Fig. 5.21(a) shows the the dc bus voltage waveform. The dc voltage slightly drops down from its nominal value because of the power loss from the utility grid. The dynamic response of the loads within the dc home is shown in Fig. 5.21(b). In the off-grid mode, the power transfer through the MMC from the grid to the dc bus is lost. Consequently, the DGs within the dc home are required to generate more power to meet the power demand. The PV unit operates in the maximum power point tracking mode. In hybrid FC/SC power systems, the FC stacks start increasing their power level to meet the dc bus power demand. Due to the slow dynamic response of the FC stack and high power density of the SC unit, the SC units in the hybrid FC/SC configuration are discharged to compensate for the power difference between the supply and demand in the transient

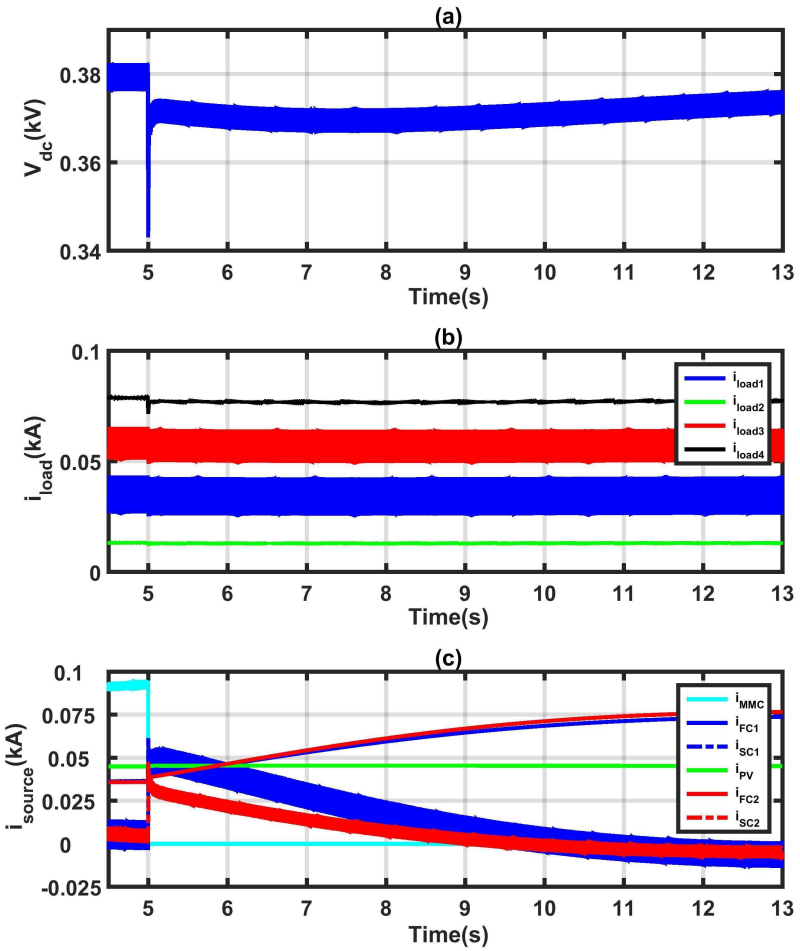


Figure 5.21: Dynamic response of the dc home during transition from the grid-tied to off-grid mode. (a) DC bus voltage; (b) Current of dc and ac loads; and (c) Output current of the MMC and DGs.

operation. The SC units also supply the total amount of the high-frequency current components. Fig. 5.21(c) shows the dynamic response of the DGs and MMC at the transition to the off-grid mode, when the DGs cooperate with each other to seamlessly maintain the service quality.

5.6.2 Hardware-in-the-Loop Verification Studies

The feasibility of hardware implementation of the smart dc home by using the proposed control and protection schemes is tested in a hardware-in-the-loop setup using

the OPAL-RT OP5600 platform. A Virtex-6 FPGA chips with time steps as low as 290 ns performs the data acquisition and I/O management. The platform provides an interface with the Matlab/Simulink software for prototyping the power and control systems in a closed-loop. The proposed control and protection schemes are implemented in the CPU with a clock speed of 3.46 GHz. The system performance is studied subsequent to a dc fault in a load segment, a dc fault in a DG segment, and the transition from the grid-tied to off-grid mode, as shown in Fig. 5.22.

First, a dc fault occurs in a load segment. According to the proposed protection algorithm, the measured current of the faulty segment quickly deviates from the maximum rated current. Next, the FSI scheme immediately identifies the fault location and sends a trip command to the respective PD_{l2}. After 200 ms, the fault is cleared, and the $load_2$ segment is reconnected to the common dc bus. Accordingly, the DCC method restores the dc bus voltage and DGs currents to their former state.

Subsequent to the dc fault in the load segment, a dc fault occurs in the DG_1 segment before PD_{sc1}. All the DGs within the dc home, particularly DG_1, which is located close to the fault location, immediately start feeding the fault current. Consequently, the difference between the measured current and maximum rated current at the SC unit in the segment of DG_1 exceeds the threshold setting. Therefore, the protection unit sends a trip signal to PD_{sc1}. The dc home equipped with the FSI scheme quickly identifies the faulty segment before the fault current de-energizes the dc home. Once the SC unit in the DG_1 segment is isolated from the dc home, the SC unit in the DG_2 segment supplies the whole high-frequency current component. After the fault clearance, the SC unit is reconnected to the dc home, and high frequency current component is shared between the SC units.

The third scenario is designed to evaluate the system performance in terms of the current sharing and dc bus voltage regulation in a transition to the off-grid mode.

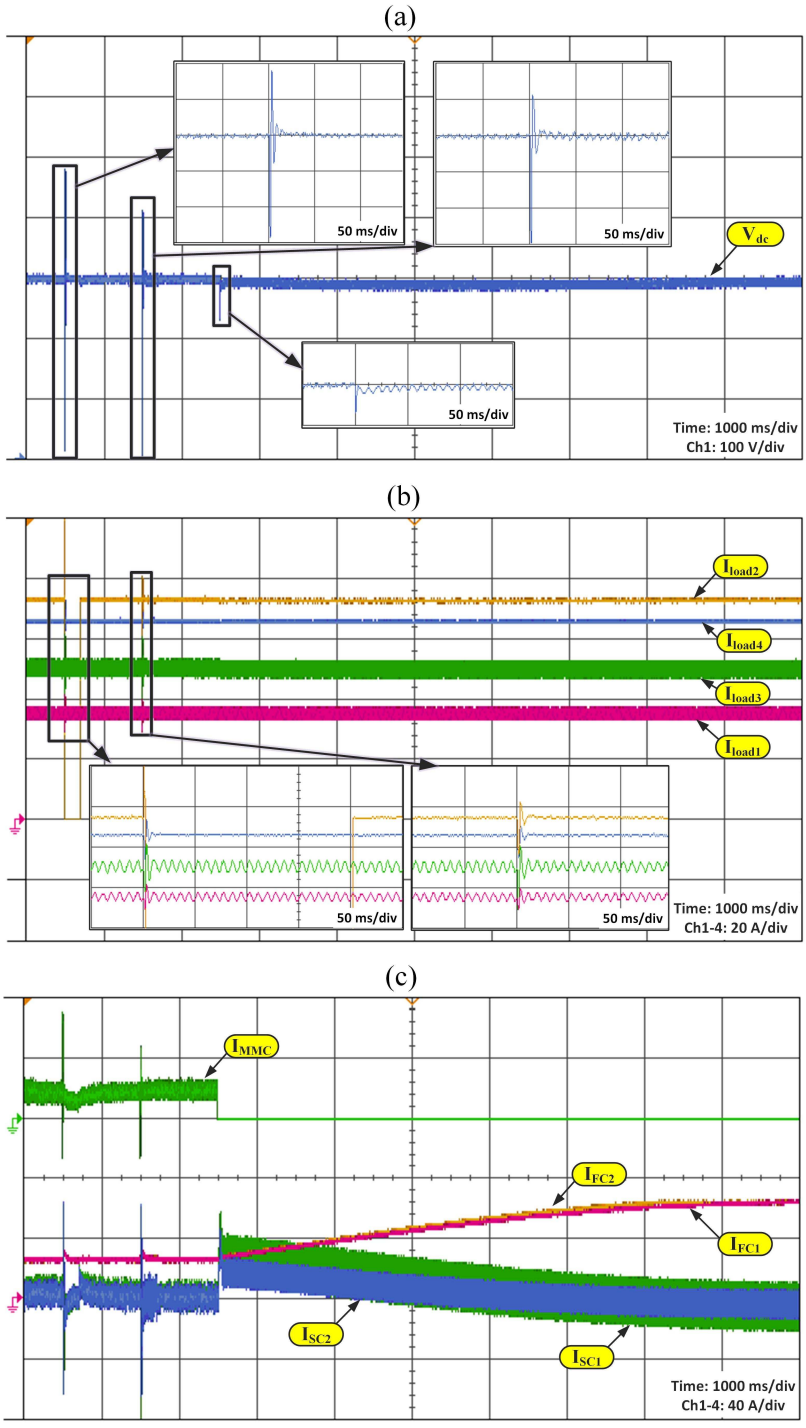


Figure 5.22: Measured hardware-in-the-loop results of the dc home equipped with the proposed control and protection schemes during, chronologically, fault in load segement, fault in DG_1 segment, and transitions from the grid-tied to off-grid mode. (a) DC bus voltage [Time: 1000 ms/div, V_{dc}: 100 V/div]; (b) Current of ac and dc loads [Time: 1000 ms/div, I_{load} (channels 1-4): 20 A/div]; and (c) Output current of the MMC and DGs [Time: 1000 ms/div, I_{FC}, I_{SC}, and I_{MMC} (channels 1-4): 40 A/div].

As shown in Fig. 5.22, the proposed DCC method robustly keeps the dc bus voltage regulated at 380 V even after the dc home transition to the off-grid mode. Furthermore, this method provides a high-quality power to the loads within the dc home. To study the behavior of the RESs and ESSs in the off-grid mode, the dynamic response of the hybrid FC/SC power sources and MMC is illustrated in Fig. 5.22(c). After the transition to the off-grid mode, the DGs need to increase their output power to provide the power demand of the dc home. Accordingly, the FC stacks, as the primary power sources, increase their output currents by increasing the Hydrogen references. The increase in the Hydrogen flow is performed by considering the optimal fuel utilization rate. As mentioned earlier, the FC stacks cannot ensure the performance of the dc home due to their slow dynamic responses. Therefore, the SC units are discharged to maintain the power balance between the supply and demand of the dc bus. The dc home equipped with the DCC method effectively regulates the dc voltage and maintains the power balance among assets. The results obtained from the hardware-in-the-loop platform are in good agreement with the simulation results and theoretical analysis.

5.7 Conclusions

The first part of this chapter presents a resilient PnP decentralized control framework suitable for dc parking lots integrating various electric components including plug-in and wireless EV charging stations, RESs, energy storage devices, and ac loads. The parking lot is interfaced with the utility grid through two BICs. The stability of the proposed switched control system is analyzed. The study results indicate the desired performance of the proposed PnP decentralized control strategy for dc parking lot to regulate the dc bus voltage and ensure an accurate sharing of the dc and oscillatory components among the DGs and BICs under unbalanced load condition. It elimi-

nates the need for a communication link among the assets and facilitates the PnP capability in the parking lot. It also guarantees smooth operation mode transition and grid support capability in the grid-connected mode. To verify the effectiveness of the scheme, simulation studies are carried out by using PSCAD/EMTDC. Furthermore, the hardware-in-the-loop studies demonstrate the feasibility of hardware implementation.

The second part of this chapter presents the DCC and FSI methods to meet the control and protection objectives in a dc home by using only local measurements. The DGs and MMC are equipped with the DCC method to cooperatively guarantee the system performance without any need for communication and ensure fast system restoration after fault clearance. The proposed FSI scheme quickly identifies the faulted segment by analyzing the local currents before the fault current could completely de-energize the entire system. Simulation studies are carried out to verify the effectiveness of the schemes. Moreover, an FPGA-based real-time study is conducted on a hardware-in-the-loop test bench to confirm the viability of the scheme.

Chapter 6

Conclusions and Future Work

6.1 Conclusions and Contributions

This chapter summarizes the main findings of the thesis and provides suggestions for future work. The technical viability of MMC technology for low- to high-voltage system applications has led to the rapid deployment of these converters in smart dc and ac grids. In this thesis, some methods were designed, developed, and implemented to solve the difficulties associated with the operation and control of the MMC, such as unbalanced SM capacitor voltages, lack of coordination or malfunction of the MMC components, and fault occurrence in the dc link and/or ac grid. The performance of the proposed strategies was investigated by using digital time-domain simulation studies. It was also validated by using an FPGA-based real-time simulator in a hardware-in-the-loop test bench.

In Chapter 2, a simplified capacitor voltage balancing method was developed to effectively balance SM capacitor voltages in a wide range of switching frequencies. This scheme was realized by developing a hierarchical PCC algorithm to cycle the switching gate signals among the SMs of each arm. The balancing unit distributes

the switching signal among SMs in such a way that the capacitor voltages converge to their reference values. The proposed method yielded the following characteristics.

1) It eliminated the hardware requirement to measure SM capacitor voltages, which enhances the reliability, computational resources, and simplicity of the MMC system.
2) It did not require retuning of the control system parameters, and it is decoupled from other control loops.
3) It balanced all SM capacitor voltages to track their reference values during steady-state conditions without diverging over time.
4) It could be implemented for a wide range of switching frequencies and simply extended to MMCs with any number of levels.
5) It effectively managed capacitor voltage fluctuation in each SM to be bounded within 5% of the rated capacitor voltage.

In Chapter 3, a new SM circuit was proposed to facilitate fault-tolerant capability for MMCs under different internal and external fault conditions. A switching pattern adapter was developed to simplify the implementation of the proposed SM in conventional HB-based MMCs. In addition, a new version of the proposed SM circuit was developed by extending its chain links to achieve a higher level of voltages. The configuration, operation principle, and gating signal pattern of an MMC that adopts the proposed SM were analyzed in detail. The proposed configuration yielded the following characteristics.

1) It facilitated internal fault management and transient performance during ac and dc network faults.
2) It offered features including full modularity, low power losses, and ease of expandability.

3) It was equipped with the switching adapter unit to attain the most efficient current path and inherent capacitor voltage balancing features.
4) It was simply integrated into conventional HB-based MMCs by using the switching signal adapter.
5) It enabled easy incorporation of redundant cells into each SM to ensure reliable operation of the MMC-HVdc systems and obtain a higher level of voltages.
6) It was reconfigured to continue its operation under some switch open-circuit fault conditions without a need for any mechanical bypass.

In Chapter 4, a resilient framework for fault-tolerant operation in MMCs was designed to facilitate normal operation under internal and external fault conditions. A supervisory algorithm and a postfault restoration unit were proposed and implemented to realize the fault-tolerant algorithm. The supervisory algorithm was composed of monitoring and decision-making units to detect and identify faults. The faults were simply diagnosed by analyzing the circulating current and SM capacitor-voltage waveforms. The proposed framework yielded the following characteristics.

1) It distinguished the internal converter faults from the external disturbances in a fully modular structure.
2) It distinguished the fault occurring in the SMs from those occurring in the sensors.
3) It kept all SM capacitor voltages balanced to track their nominal values even after the occurrence of multiple faults and faults in the current sensors.
4) It diagnosed simultaneous faults and guaranteed resilient system operation under various open-circuit faults.
5) It restored the system with a fast response in a few milliseconds where the elapsed time from detection to identification was less than 100 ms.

In Chapter 5, a resilient PnP decentralized control framework was designed which is suitable for dc parking lots integrating various electric components including plug-in and wireless EV charging stations, RESs, energy storage devices, and ac loads. The parking lot was interfaced with the utility grid through two BICs. The DGs and BICs were equipped with, respectively, the PnP decentralized control and switched control strategies to ensure the overall system performance in different modes of operation without the need for communication. The stability of the proposed switched control system was analyzed. The proposed control framework yielded the following characteristics.

1) It provided a resilient decentralized power-sharing among the DGs with different dynamic models.
2) It eliminated the need for a communication link among the assets. This advantage enhances the reliability, resiliency, and simplicity of the overall system.
3) It kept the dc bus voltage deviation within 6% of the rated value.
4) It ensured an accurate sharing of the dc and oscillatory components among the DGs and BICs under unbalanced load condition.
5) It facilitated the PnP capability in the parking lot.
6) It assured smooth operation mode transition and grid support capability in the grid-connected mode.

In addition, the DCC and FSI methods were proposed to meet the control and protection objectives in a dc home by using only local measurements. The DGs and MMC were equipped with the DCC method to cooperatively guarantee the system performance without any need for communication. The proposed FSI scheme quickly identified the faulted segment by analyzing the local currents. The proposed schemes had the following benefits for the dc home.

1) The enhanced reliability, high resiliency, and simple management of the proposed

strategies contributed to the service quality and reliability in the dc home.

2) The DCC and FSI strategies enhanced the system's ability to reconfigure the dc home once a fault occurred.
3) The DCC method ensured fast system restoration after fault clearance, effective dc bus voltage regulation, and accurate current sharing among the DGs and MMC.
4) The FSI scheme identified the faulted segments in less than 1 ms before the fault current could completely de-energize the entire system.
5) The FSI scheme used only the local measurements from the control unit, eliminating the latency of the operation of the PDs.

6.2 Directions for Future Work

The following research studies can be conducted in continuation of the work presented in this thesis.

- Developing a robust controller to mitigate undesirable interaction dynamics between MMC and host ac grid in HVDC applications.
- Evaluating the performance of the proposed control strategies for low-voltage applications such as EV charger.
- Extending fault-tolerant algorithm in different applications.
- Studying the applicability of the developed voltage balancing algorithm to other multilevel architectures.

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