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Multilevel Space Vector PWM for Multilevel Coupled Inductor Inverters

by

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To my lovely wife, Roya; I am happy that I made you proud of me and my work. Your ongoing love and support in our life journey give me the confidence to go out there and explore the world. I love you.

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Abstract

A multilevel Space Vector PWM (SVPWM) technique is developed for a 3-level 3-phase PWM Voltage Source Inverter using a 3-phase coupled inductor to ensure high performance operation. The selection of a suitable PWM switching scheme for the Coupled Inductor Inverter (CII) topology should be based on the dual requirements for a high-quality multilevel PWM output voltage together with the need to minimize high frequency currents and associated losses in the coupled inductor and the inverter switches.

Compared to carrier-based multilevel PWM schemes, the space vector techniques provide a wider variety of choices of the available switching states and sequences. The precise identification of pulse placements in the SVPWM method is used to improve the CII performance. The successful operation of the CII topology over the full modulation range relies on selecting switching states where the coupled inductor presents a low winding current ripple and a high effective inductance between the upper and lower switches in each inverter leg. In addition to these requirements, the CII operation is affected by the imbalance inductor common mode dc current. When used efficiently, SVPWM allows for an appropriate balance between the need to properly manage the inductor winding currents and to achieve harmonic performance gains.

A number of SVPWM strategies are developed, and suitable switching states are selected for these methods. Employing the interleaved PWM technique by using overlapping switching states, the interleaved Discontinuous SVPWM (DSVPWM) method, compared to other proposed SVPWM methods, doubles the effective switching frequency of the inverter outputs and, as a result, offers superior performance for the CII topology by reducing the inductor losses and switching losses.

The inverter operation is examined by means of simulation and experimental testing. The experimental performance comparison is obtained for different PWM switching

patterns. The inverter performance is affected by high-frequency inductor current ripple; the excessive inductor losses are reduced by the DSVPWM method. Additional experimental test results are carried out to obtain the inverter performance as a variable frequency drive when operated in steady-state and during transient conditions. The CII topology is shown to have great potential for variable speed drives.

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LIST OF SYMBOLS AND ABBREVIATIONS

APOD-PWM	Alternate phase opposition disposition
CII	Coupled inductor inverter
CHB	Cascade H-bridge
DPWM	Discontinuous pulse width modulation
d_x, d_y, d_z	Dwell time
EMC	Electro-magnetic compatibility
EMI	Electromagnetic interference
FOC	Field oriented control
FC	Flying capacitor
ia	Phase A current
IaU	Phase A upper winding current
iaL	Pahse A lower winding current
icm	Common mode dc current
IPD-PWM	In-phase disposition
L_l	Leakage inductance
LS-PWM	Level-shifted pulse width modulation
L_m	Magnetizing inductance
m_a	Modulation amplitude
mmf	Magnetic motive force
NPC	Neutral point clamped
PMSM	Permanent magnet synchronous machine
POD-PWM	Phase opposition disposition pulse width modulation
PS-PWM	Phase shifted pulse width modulation
PI	Proportional and integral
PWM	Pulse width modulation
L_t	Resultant magnetizing inductance
rms	Root mean square
SHE	Selective harmonic elimination
SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
T_s	PWM Switching cycle
f_c	Switching frequency
THD	Total harmonic distortion
THDi	Current total harmonic distortion
THDv	Voltage total harmonic distortion
VaCM	Phase A common mode voltage
Vref	Reference voltage vector
VSI	Voltage source inverter
V_x, V_y, Vz	voltage vectors of a given triangle with vertex V_x, V_y and V_z
Δ_1, Δ_2, Δ_3, Δ_4	Triangles in each 60º of a space vector block diagram

Chapter 1

Introduction

A number of topologies are available for the inverter stage of variable frequency drives. Commonly, a 6-switch 2-level inverter is used for low-medium power applications, and 12-switch multilevel Neutral-Point Clamped (NPC) inverter topologies are used at higher power levels [1]. The output voltage and current harmonics of these inverters can cause additional power losses in the loads, derating them and lowering their output capacities. If needed, the output of these inverters can be passed through an inductive filter to improve the current Total Harmonic Distortion (THD). However, the use of AC inductor filters can be limited by factors including the maximum switching frequency, flux densities in the magnetic cores, power losses, efficiency, and fundamental voltage drops [2]. These effects can be significantly magnified when AC inductor filters are used in high-speed applications such as flywheel energy storage systems where the fundamental frequency range changes by a few hundred Hertz [3, 4].

Pulse Width Modulation (PWM) converters also introduce some design limitations on the load, such as dv/dt stresses, common mode voltages and cable interactions between the power converter and the load, which are more pronounced in high-power applications [5]. Many studies have been conducted to improve the output quality of inverters by increasing the effective output switching frequency and the number of PWM output voltage levels [6, 7]. If the application and power level justifies the choice of multilevel topologies, these improvements can be achieved by increasing the number of switches (i.e., multilevel converters) or the number of power converter modules (i.e., multiple converter modules). The use of multilevel inverters and parallel inverter output stages coupled through interphase transformers also improves the output THD [8-11]. Unfortunately the parallel connection of inverters can present current-balancing issues since the various inductors and power converters cannot always have identical electrical characteristics; hence, the harmonic current cancellation may not be optimal. Also, the trade-off for such increased performance in multilevel inverters is a large increase in circuit components, control complexity and cost, which limits the use of these inverters to high-power applications. Thus, many low-medium power applications which could

benefit from the performance gains of multi-level converters are unattainable because of the cost.

The PWM control of standard converters uses dead-times in the PWM signal generation to avoid the DC supply voltage short-circuits when both the upper and lower switches are conducting within the same inverter leg. These dead-times are important because they provide a safety margin between the on-states of the upper and lower switches in an inverter leg. If not compensated for, the dead-times can reduce the fundamental output voltage and also produce sub-harmonics in the output voltage, lowering the output quality [12-17]. In addition, the inverter switching frequency can be limited due to the dead-times for high-performance application such as that in audio amplifiers [18].

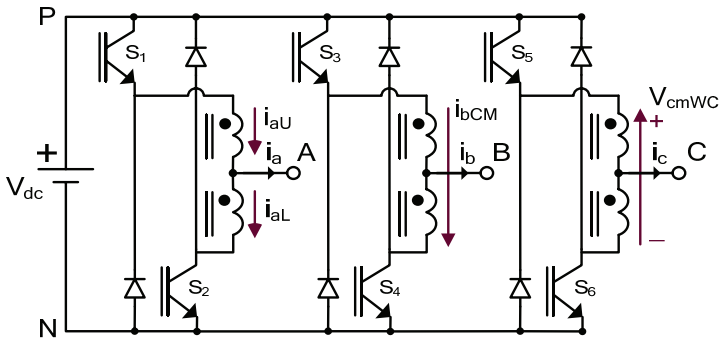


Figure 1-1: 3-phase 3-level coupled inductor inverter topology

One recent proposed alternative multilevel topology applied in low power applications is to use coupled inductors in the output stage of a 6-switch inverter, as shown in Figure 1-1 [2, 19]. Using appropriate PWM switching of the upper and the lower switches in each inverter leg, the Coupled Inductor Inverter (CII) topology produces a multilevel output from a single DC voltage level. When compared with comparable alternatives, the CII topology uses half the number of switches to generate the same number of voltage levels. In contrast to AC inductor filters, the fundamental inductor voltage drops are removed since the upper and lower coupled inductor windings are placed in one limb of the inductor core, cancelling the fundamental frequency flux produced by each other [20]. In addition, a significant advantage of the CII topology is that the requirement for the dead-times to avoid the shoot-through current is eliminated. Thus, the traditional adverse effects of the dead-times are avoided.

By lowering switching losses, the interleaved discontinuous PWM strategy is demonstrated in [2, 19] to be an effective PWM strategy for the CII topology, allowing

for higher switching frequency without degrading the output quality due to discontinuous PWM. The use of the interleaved PWM technique [21] also increases the effective output switching frequency, reducing the high frequency harmonics in the output PWM voltage and current. The improved PWM voltages can also lower the high-frequency losses in AC inductors and machine loads, with a potential improvement of the load efficiency and power density [19]. With these features, the CII topology is more suited than alternative topologies for loss-sensitive and high-frequency fundamental applications where higher frequency PWM outputs are essential.

1.1. Research Objectives

The various benefits of the CII topology can assure the future use of this structure in many high-performance applications. The CII circuit has been demonstrated to have superior output features, but the performance of the inverter together with the impact of the additional coupled inductors has not been fully investigated. The current ripple associated with the coupled inductors is one of the key parameters in determining the inverter performance. This study will demonstrate that the current ripple is linked to the coupled inductor losses. Thus, to achieve improvement in the efficiency and performance of the CII topology as main objectives of this thesis, the current ripple should be carefully considered, and the impacts of different factors on minimizing ripple should be examined.

The objectives of this dissertation can be categorized as follows:

- Investigate the factors which contribute to the winding current and output current ripples in the CII topology.
- Develop a suitable PWM switching scheme which minimizes the high frequency current ripple and allows for operation over a wide range of modulation amplitudes (m_a).
- Improve the CII inverter performance by
    a. Minimizing the inductor losses associated to high frequency current ripple.
    b. Alleviating the EMI noises by maintaining the high frequency flux inside the coupled inductor core rather the outside of the inductor core.

This thesis explores the relationship between the current ripple and various CII circuit and control parameters. The maximum high-frequency winding and output current ripples can be obtained from the inductance requirement of the coupled inductors. However,

when the coupled inductor is placed on a three-limb core, the coupled inductor current ripple in one inverter leg can be affected by both the coupled inductor windings in the same inverter leg and in the other inverter legs due to the magnetic coupling between the windings in a three-limb core. Since the coupled inductor winding configuration at each switching state can be changed with the condition of being on and off for each inverter switch, the current ripple will be dependent on the value of the effective inductance between the upper and lower switches in each inverter leg. In fact, the effective inductances mainly contribute to the expected current ramping rate for the winding current. The inductance effective size determines the maximum high frequency current peak-peak ripple.

In addition, a very simple approach is used, which considers the relationship between the time-varying voltage across the inductor with the effective inductance $L_{effective}$ and the time-varying current passing through; the duration of applying the PWM switching voltage across each inductor winding in each switching state can also impact on the current ripple. Thus, as shown in this thesis, the current ripple varies with the effective inductance in each switching state and the duration of the PWM voltage across the inductor in each switching state. Since these two parameters are characteristics of every PWM modulation scheme, the current ripple will be significantly dependent on the PWM switching technique and the PWM switching frequency.

From the fundamental operation of this topology in [2, 19], the common-mode ripple components in the winding current are given by the high-frequency switching over the coupled inductor winding; the high-frequency common mode AC ripple is the only component of the winding current, which produces (AC ripple) flux in the coupled inductor core. Since the ripple magnitude of the winding current is essentially linked to the AC ripple flux, the PWM modulation scheme with the ability to minimize the AC current ripple in the windings, lowers the coupled inductor core losses [22]. As a result, the overall performance of the inverter can be improved by reducing the coupled inductor losses.

Consequently, the selection of an optimal modulation strategy is essential to ensure the high-performance operation of the multi-level coupled inductor inverter topology. The successful operation of the CII topology over the full modulation range relies on selection of switching states and sequences where the coupled inductor presents a low winding current ripple. In addition to these requirements, when using any modulation scheme,

care must be taken to balance the common mode winding voltage (current) over the switching period for the continuous conduction operation of the coupled inductor. If discontinuous conduction were to occur, the centre-tap voltage would be undefined, resulting in high harmonic voltage distortion [18, 23].

PWM strategies used for standard inverters can be modified for use with this topology. The presence of the coupled inductors in this inverter allows interleaved PWM switching of the upper and lower switches in each inverter leg to be an effective switching scheme for this topology. Interleaved sinusoidal PWM (SPWM) [21, 24] and discontinuous PWM (DPWM1) [24] techniques adopted from 2-level standard inverters can be used to lower the size of the output AC filter and reduce the magnitude of high-frequency output current harmonics by increasing the effective switching-frequency of the output PWM waveforms above the actual switching frequency [2, 19, 25]. DPWM1 compared to SPWM generates multi-level output voltages with lower harmonic content. However, as shown in this thesis, even with high-quality output signals, the overall performance of the CII can be poor due to coupled inductor losses, and this problem is especially noticeable at low modulation depths. These modulation schemes have no freedom to select the more desirable switching states present in each switching cycle. Therefore, switching states with a low-effective winding inductance are selected, resulting in significant high-frequency current ripple in the inductor windings. This ripple generates high winding and core losses, with a high-frequency leakage flux produced outside the magnetic core.

In this thesis, a multilevel Space Vector PWM (SVPWM) strategy is developed and applied to the CII topology. The SVPWM strategy is based on those schemes developed for other multilevel inverters [5, 24, 26-36]. The multilevel SVPWM technique for the CII topology can offer superior performance over previous modulation schemes by addressing issues related to common mode dc current balance and ripple minimization. The prime benefits of SVPWM are precise identification of the pulse placement and choice between redundant switching states for each voltage vector. When used efficiently, SVPWM can allow for an appropriate balance between the need to produce a multi-level output and the proper management of the inductor winding currents and effective inductance. In addition, a careful analysis of the space vector will reveal that the winding current ripple depends on not only the selection of switching states with a high-effective inductance, but also their sequences. As shown in this thesis, the order of the voltage vectors in each sequence during a switching cycle can be arranged to minimize

the winding current ripple and output current ripple as well. If the switching states with the same current-ramp direction link together, they can increase the expected current ramp by adding the duration of the same PWM voltage across the inductor winding.

In this thesis, a number of SVPWM strategies for the CII topology are developed. The effects of the PWM schemes on the output current ripple are investigated, and the results demonstrate that, like the winding current ripple, the output current waveform is also dependent on the switching sequence, the effective output frequency and the coupled inductor leakage inductance.

Using the analysis in this thesis, an interleaved discontinuous SVPWM (DSVPWM) method is developed. The DSVPWM scheme can minimize the winding current ripple while providing high-quality outputs for a large operating range. Using the interleaved PWM switching technique in the CII topology, the effective output switching frequency can be doubled in the DSVPWM scheme. The interleaved DSVPWM strategies are categorized as DSVPWM0, DSVPWM1, DSVPWM2 and DSVPWM3. (The difference among these schemes is the position of the discontinuous period within each fundamental voltage cycle.) This thesis demonstrates that the winding current ripple is also dependent on the position of the discontinuous period in the fundamental voltage relative to the phase angle at which the magnitude of the fundamental current is maximum.

In general, the fundamental output voltage produced by carrier-based PWM techniques can be identical to that produced by SVPWM. However, the optimal sequence of pulses within the sampling interval (or the treatment of the zero space vectors) leads to the superior harmonic performance of the space-vector modulation technique. This thesis investigates whether this performance improvement is limited to the output waveforms or if it can be effectively extended to include the optimal operation of the couple inductor inverters.

A comparison between the two-modulation approaches, the interleaved carrier-based PWM and interleaved DSVPWM, indicates that the methods produce different CII performance. The interleaved DSVPWM strategy presented in this thesis for the coupled inductor inverters can reduce the inductor losses and significantly improve the performance of the inverter drive by lowering the total inverter loss. The effectiveness of the proposed approaches and the comparison of different PWM algorithms is verified by using simulation results and validated by experimental tests.

Finally, the performance of the CII topology as a machine drive is investigated through

laboratory experiments with a Permanent Magnet Synchronous Machine (PMSM). The transient response of the drive with the closed-loop speed and power control for the proposed CII drive structure are important for most industrial applications. The results will demonstrate the successful operation of the CII topology as a variable frequency drive while providing high-quality outputs, which can increase the operating efficiency of the PMSM machine.

1.2. Thesis Outline

This thesis presents a new multilevel space-vector pulse width modulation (SVPWM) technique for coupled inductor inverters. The SVPWM technique is used to improve the performance of the coupled inductor inverters by lowering the inductor losses. This dissertation consists of 6 chapters.

Chapter 2 describes the advantage of multilevel converters over conventional two-level converters and briefly reviews the attractive features and drawbacks of multilevel converters. The most popular multilevel converter topologies are reviewed. The PWM switching strategies such as carrier-based PWM, selective harmonic elimination and SVPWM for multilevel converters are explained and summarized. Finally, the use of multilevel converters in different applications is explored.

Chapter 3 describes the fundamental operation of the multilevel voltage source inverter using split-wound coupled inductors. Continuous and discontinuous conduction operation modes of the CII topology are explained, and the performance of the CII inverter is compared for these two conditions. The relationship between the winding currents, the output currents, and common mode dc current is identified. The coupled inductor is modeled with the magnetizing and leakage inductances by using a simplified equivalent transformer model. By using this model, the maximum ripple equations for the inductor winding (common mode) current and output current are given. Switching states are analyzed based on the configuration of the coupled inductor in a single inverter leg. The impacts of these switching states together with other factors such as switching turn -on and -off are explained. Finally, the inverter (switching) device rating is determined.

Chapter 4 describes the principles of two commonly used PWM techniques (the initial interleaved carrier-based PWM and newly developed multilevel space vector PWM modulation schemes) for the CII topology. The basic operation of the CII topology with these schemes and their evolutions, advantages and limitations are investigated. The

initial interleaved carrier-based PWM strategies, sinusoidal PWM and discontinuous PWM (DPWM1), are explained. The multilevel space vector PWM algorithm for this topology is developed and investigated by extracting all possible CII switching states with the examination of various 3-phase coupled inductor winding configurations. By using the SVPWM technique, the multilevel space vector block diagram is derived, and the dwell time calculation is described. The impacts of the voltage vectors corresponding to each winding configuration on the common mode current are studied for inductance requirements. The basic steps in designing a switching sequence are developed; the various parameters considered in the design stage to minimize the current ripple, select the high-effective inductance switching states and balance the common mode winding current (voltage) are explained. With the flexibility of selecting the switching states and sequences in the SVPWM technique, a number of SVPWM strategies are developed. The development stage of each strategy and the performance improvement obtained is explained, and the characteristic of the strategies are derived.

In Chapter 5, the performances of the CII topology with SPWM, DPWM1 and SVPWM modulation strategies are compared by means of simulation and experimentally verified with a RL load. This comparison examines the performance of the coupled inductor inverter by itself and also the inverter's output quality, which is investigated by using a voltage and current THD spectra comparison over the full modulation range. The winding current waveforms and THD spectra are used to evaluate the inverter performance. The results confirm the effective operation of the topology with different modulation methods. To verify the superiority of the proposed SVPWM technique, the interleaved DSVPWM method is compared with interleaved carrier-based methods through a series of experimental loss measurements, which are performed with different load conditions, various modulation indices and two different core laminations for the coupled inductors.

Finally, experimental tests including the closed loop speed and power control experiments with a PMSM are carried out to show the performance of the CII topology as a machine drive. The results will verify the potential of this topology for use in motor drive applications.

Chapter 7 summarizes the results presented in the previous chapters, concludes the work carried out, and indicates the accomplishments of this thesis. Finally, this chapter provides recommendations for future research.

Chapter 2

Multilevel Power Converters

Numerous multilevel converter topologies have been introduced during the last few years [37-41]. Among the power converters for high-power applications, the most common topologies are the Cascaded H-Bridge (CHB) converter with separate dc sources, the Neutral-Point Clamped (NPC) converter (or neutral-clamped converter), and the Flying Capacitor (FC) converter (or capacitor clamped converter). Recently, many researchers have developed new topologies and unique modulation schemes. A newly developed topology explored in this thesis is the coupled inductor inverter (CII), which is used for relatively low power 3-phase applications. Several surveys of multilevel converters have been published to introduce these topologies [1, 42-44].

This chapter describes the attractive features of multilevel power converters in general. Multilevel topologies are reviewed and the fundamental operation of these structures is also presented. The advantages and disadvantages of each topology such as its operational and technological issues are discussed. A survey of the PWM modulation techniques developed for these converters is briefly reviewed. Finally, a few applications of multilevel converters are explained.

2.1. Multilevel Power Converter Features

Recently, multilevel power converters have received a great deal of attention in numerous high-power medium-voltage industrial applications [1, 5, 42, 43, 45, 46]. A multilevel converter uses a series of power semiconductor switches to perform the power conversion by synthesizing the AC output terminal voltage from several DC voltage levels, and, as a result, staircase waveforms can be generated. Compared to standard two-level converters, multilevel converters offer great advantages such as lower harmonic distortion, lower voltage stress on loads, lower common-mode voltage, and less electromagnetic interference. By reducing filtering requirements, they not only improve the efficiency of converters, but also increase the load power and, hence, the load efficiency by improving the load voltage with a lower harmonic content.

Multilevel converters are basically developed to increase a nominal power in the

converter. The higher number of voltage levels in these topologies results in higher quality output voltages. The concept of multilevel converters was introduced in 1975 [47], and the term "multilevel" first meant "three-level" [48] but now refers to converters with more than a two-level output voltage. Multilevel topologies have been developed by increasing the number of semiconductor switches or the number of power converter modules (i.e., multiple converter modules). The trend toward a greater number of voltage levels is necessary due to the benefits of higher voltage ratings with a very low total harmonic distortion. By increasing the number of voltage levels, the converter's fundamental output voltage can be produced with a lower harmonic content, and will significantly improve the quality of the output voltage and eventually approach a desired sinusoidal waveform.

The conventional two-level converter can produce high-quality outputs for low-power applications by using a high switching frequency. However, for medium- and high-power applications, the maximum switching frequency is limited by the switching devices due to the high switching losses. In this case, multilevel converters can be used to lower the switching frequency, and a high quality output waveform can be produced. The superior features of multilevel converters over two-level converters can be briefly summarized as follows [5, 44, 49].

- They can generate output voltages with very low THD. Multilevel output PWM voltage can reduce the inverter switches blocking voltage and the dv/dt stress on the load such as a motor. The lower voltage stress on a load can reduce the number of Electro-Magnetic Compatibility (EMC) problems.
- They can produce a lower common-mode voltage. Thus, the lifetime of a motor connected to a multilevel motor drive can be increased due to the reduced stress on the bearings of the motor.
- By generating a staircase voltage waveform, they can produce lower converter input current distortion. The lower current ripple can reduce the size of a capacitor filter in a DC link.
- They are capable of operating at both a fundamental switching frequency and a high switching frequency PWM. In high-power applications, a lower switching frequency can reduce the switching loss, resulting in an efficiency increase.

However, the trade-off for such increased performance in multilevel converters is that they require a greater number of power switching devices. The number of semiconductor

switches together with their related gate drive circuits can increase the overall system cost and the control complexity. Therefore, they can be used only where the application and power level justify the choice of multilevel topologies. They have been selected as a preferred power converter topology for high-voltage and high-power applications.

2.2. Multilevel Power Converter Structures

The multilevel converters have different characteristics such as the number of components, the modularity, and the control complexity. Each converter topology can be chosen for a specific application. This section describes the major multilevel structures and focuses on three-level power converters.

2.2.1. Cascaded H-Bridges

The cascaded H-bridge inverter is composed of multiple units of single-phase H-bridge power cells as shown in Figure 2-1. For example, the 5-level CHB topology demonstrated in Figure 2-2 is obtained by cascading two CHB power cells in each phase. This type of converter topology has been used in high-power medium-voltage drives [50-55]. To achieve multilevel high-voltage output with a low THD, the AC outputs of each H-bridge inverter can be connected in series. The operating voltage level of each application and the manufacturing cost of each unit for the selected voltage level determine the number of power cells in a CHB inverter.

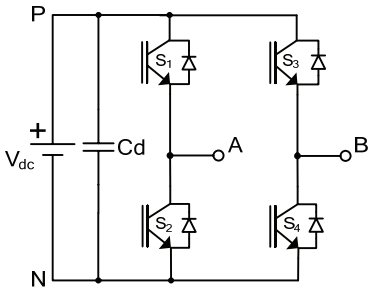


Figure 2-1: Single-phase 3-level H-bridge inverter

Each power cell in a CHB inverter requires an isolated dc supply which can be obtained from multipulse diode rectifiers [5]. Each power cell can be powered by a dc supply of equal voltage or unequal voltage. The use of identical power cells leads to a modular structure, which is cost-effective and has less control complexity than that of other structures. The modular topology provides more redundant switching states. This

feature allows for great flexibility in the PWM switching design, especially for space vector modulation schemes. However, with unequal dc voltages, more voltage steps can be obtained in the inverter output voltage waveform for a given number of power cells [56, 57]. With this configuration, the CHB inverter using unequal dc voltages is no longer modular. In addition, the PWM control complexity increases due to the reduction in the redundant switching states. Therefore, this type of inverter topology has limited industrial application.

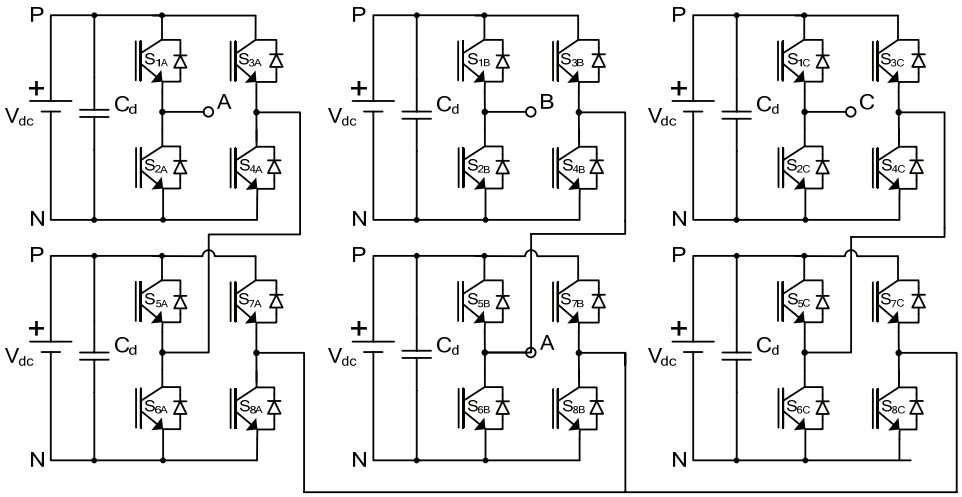


Figure 2-2: 5-level cascaded H-Bridge inverter topology

In Figure 2-1, a single-phase H-bridge inverter includes two inverter legs with two switching devices in each leg. Each H-bridge inverter level can produce three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$,by connecting the dc source to the AC output by different combinations of the four switches, S_1, S_2, S_3, and S_4. When switches S_1 and S_4 are turned on, the output voltage is $+V_{dc}$, and when switches S_2 and S_3 are turned on, $-V_{dc}$ can be obtained. By turning on S_1 and S_3 or S_2 and S_4, the output voltage is 0. Either bipolar or unipolar modulation schemes can be used for a CHB topology. However, the unipolar modulation strategy increases the effective switching frequency to double the actual switching frequency [5].

The number of PWM voltage levels in a CHB topology can be obtained by

$$N = (2C + 1), \tag{2-1}$$

where C is the number of H-bridge cells per phase leg. The voltage level N is always an odd number for the CHB inverter, but can be either an even or odd number for other

multilevel topologies such as diode-clamped inverters. The CHB inverter can be extended to any number of voltage levels, but the number of switches increases significantly. The total number of active switches used in the CHB inverters can be estimated by

$$M = 6(N - 1). \tag{2-2}$$

For example, a 7-level CHB inverter requires 36 switches with the same number of gate drivers.

Multilevel cascaded inverters have been used for several applications. Since photovoltaics or fuel cells applications provide separate dc sources, cascaded inverters are ideal for connecting renewable energy sources with an AC grid. Another application is in the main traction drive in electric vehicles where several batteries or ultracapacitors are well-suited to serve as separate dc sources [50, 51, 58].

The main benefits of the CHB multilevel inverter are its modular structure and high-voltage operation without switching devices in series, for these features eliminate the problem of equal voltage sharing for series-connected devices. The drawbacks of CHB inverters are its requirements for a large number of isolated dc supplies and a switching device count.

2.2.2. Diode-Clamped Multilevel Inverter

In 1981, the first diode-clamped converter, also called a Neutral-Point Clamped (NPC) converter, was proposed by A. Nabae, I. Takahashi, and H. Akagi in [48]. The three-level NPC topology is based on a modification of the standard two-level converter topology by adding two new switching devices per phase, as shown in Figure 2-3. The blocking voltage for each switching device of NPC is half the blocking voltage of the two-level inverters with the same dc-link voltage. The multilevel output voltage is achieved by using clamping diodes and cascaded dc capacitors. This topology is extendable to higher number of voltage levels such as four- and five-level topologies. However, the three-level NPC has found wide applications in high-power medium-voltage drives [42, 59].

In Figure 2-3, to provide a floating neutral point, the two cascaded dc capacitors split the dc input voltage of the inverter. The two diodes in each inverter leg connected to the neutral point are called the clamping diodes. When switches S_1 and S_2 are turned on and S_3 and S_4 are turned off, the inverter output terminal is connected to the positive dc-link voltage $+V_{dc}$; when switches S_1 and S_2 are turned off and S_3 and S_4 are turned on, the inverter output terminal is connected to the negative dc-link voltage $-V_{dc}$. When switches

S_2 and S_3 are turned on, the inverter output terminal is connected to the neutral point through one of the clamping diodes, depending on the direction of the load current. In this condition, the dc link capacitors (normally charged to $V_{dc}/2$) can be charged or discharged by the neutral current, causing a neutral-point voltage unbalance [60-67]. Thus, the PWM control strategy is needed to balance the neutral-point voltage deviation, making the control algorithm complex. By using proper PWM switching, the average device switching frequency can also be increased to twice the actual switching frequency.

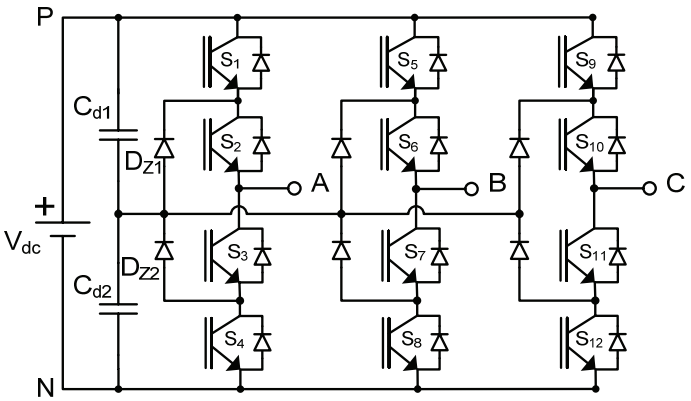


Figure 2-3: Three-level NPC inverter

The main advantages of the NPC topology are (i) the switches can be selected with lower blocking voltages and (ii) any number of voltage levels can be obtained by increasing the number of switches in this topology. The main drawbacks of this topology are the capacitor voltage deviation, the requirement for a complicated PWM switching strategy, and the different blocking voltages of the additional clamping diodes.

2.2.3. Flying Capacitor Multilevel Inverter

A Flying-Capacitor (FC) inverter was proposed by Meynard and Foch in 1992 [68]. Figure 2-4 shows a typical configuration of a 3-level flying-capacitor inverter. Compared to NPC, this topology uses dc capacitors connected to the cascaded switches instead of using clamping diodes [69, 70]. The voltage on each capacitor demonstrates the size of the voltage steps. The total capacitor voltage for each level differs from that of the next voltage level by one voltage step. (S_1, $S_{1'}$), and (S_2, $S_{2'}$) are complementary switch pairs in each of the inverter legs. For example, when switches S_1 and S_2 conduct, the inverter terminal voltage V_{AN} is $V_{dc}/2$, corresponding to the negative DC bus N. Similar to the switching state redundancies in other multilevel converters, those in this topology provide

a great flexibility for the PWM switching strategy to control and balance the charging/discharging for specific capacitors. The effective equivalent inverter switching frequency could be four times the device's actual switching frequency. However, the flying-capacitor inverter has some limitations. The inverter requires a large number of dc capacitors with pre-charge circuits needed for each one. The PWM control is complex due to the need to balance the capacitor voltages, which change with the different inverter operating conditions. The practical use of the flying-capacitor inverter is limited due to the above drawbacks.

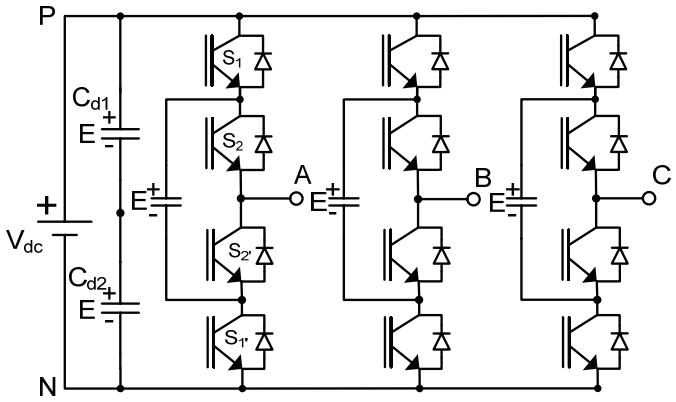


Figure 2-4: Three-level flying-capacitor inverter

2.2.4. Parallel Inverters Structure

Like the previous multilevel topologies, standard inverter modules can be connected in parallel by using interphase transformers to produce multilevel PWM output voltages. The parallel inverter topology as shown in Figure 2-5 can produce 3-level PWM output voltages with low THD [9, 10].

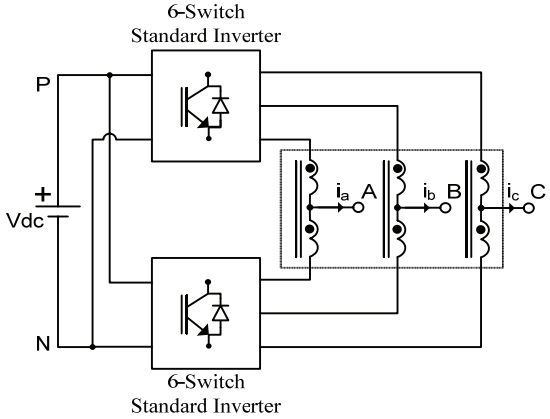


Figure 2-5: Parallel inverters using interphase transformers (current sharing reactors)

However, the main drawback of this topology is that the operation of the parallel inverters depends on the device's parameter variations. A small variations in the switch turn-off times and on-state voltage drops can create dc current drifts and circulating currents. A balanced symmetrical operation of parallel connected inverters can be obtained by using interleaved PWM controls.

2.2.5. Coupled Inductor Inverter

One recent alternative multilevel topology uses coupled inductors in the output stage of a 6-switch inverter [2, 19]. The 3-level coupled inductor inverter (CII) is shown in Figure 2-6. This topology produces multilevel output voltages from a single DC voltage supply at each inverter output terminal using a 3-phase split wound coupled inductor. The output terminal voltage V_{AN} of the CII topology can generate an extra voltage level of $½V_{DC}$ when switches S_1 and S_2 are turned on or turned off. When switch S_1 is turned on and S_2 is turned off, V_{AN} is connected to the positive dc-link voltage $+V_{dc}$; when switch S_1 is turned off and switch S_2 is turned on, V_{AN} is connected to the negative dc-link voltage $-V_{dc}$. The significant advantage of the CII topology is that the requirement for dead-time to avoid shoot-through current is eliminated since the split-wound coupled inductor is in series with the upper and lower switches. Thus, traditional adverse effects of dead-time are avoided. In addition, by using a proper PWM switching scheme, the effective switching frequency of the PWM output voltages can be doubled [2, 19].

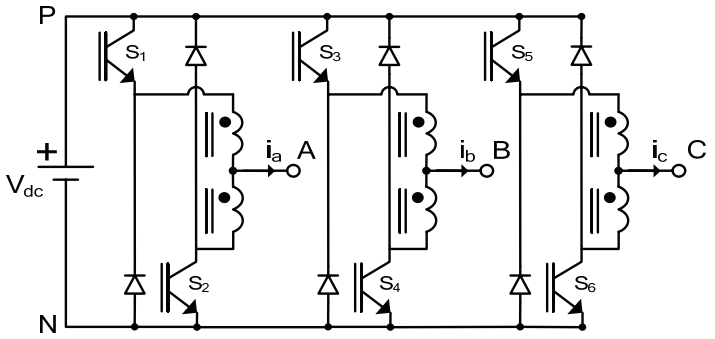


Figure 2-6: Three-phase 3-level coupled inductor inverter

With the same number of semiconductor switches, the CII topology benefits from multilevel features and advantages over standard inverters [2, 19]. This topology is also comparable to other 3-level converters (i.e., 3-level NPC) in terms of output waveform quality while uses half the number of switches to generate the same number of voltage levels. These features make this topology suitable for high-performance drives.

2.3. Multilevel Converters PWM Modulation Strategies

Pulse width modulation has been studied extensively during the past decades. PWM strategies have been developed to achieve a wide linear modulation range, less switching loss, less harmonic content in the spectrum of the PWM output waveforms, and easy implementation with less computation burden.

Recently, many studies have been conducted to modify traditional PWM strategies in order to extend them for use as a multilevel converter modulation. These schemes have become more complex due to additional power electronics devices control. However, the multilevel converters provide extra degrees of freedom in determining the PWM switching patterns by providing the switching redundancies. As a result, many modulation strategies have been developed for multilevel converters [5, 24, 61, 62, 71-84] . The three major multilevel PWM strategies can be classified as multilevel carrier-based PWM (or multi-carrier based PWM), multilevel space vector PWM, and Selective Harmonic Elimination (SHE). Depending on the switching frequency of multilevel converters for each specific application, the appropriate modulation scheme can be selected. Generally, high-power applications require low switching frequency due to the lower switching losses. Thus, the use of selective harmonic elimination and multilevel space vector PWM are preferred strategies since these methods can operate with the fundamental switching frequency. However, high-quality converter outputs can be obtained by increasing the switching frequency. In this case, the multilevel carrier-based PWM and space vector PWM can be used. These schemes are more suitable for high dynamic range applications.

Multilevel carrier-based PWM techniques, Phase-Shifted PWM (PS-PWM) and Level-Shifted PWM (LS-PWM), are developed for multilevel converter topologies by using multiple carriers [85-93]. The phase-shifted multiple carriers have been used for CHB and FC topologies to control each switch of the converter, providing an even power distribution among the power cells. For a multilevel converter with C power cells, a sinusoidal bipolar PWM or unipolar PWM reference waveform with multiple carriers phase shifted by $180^{\circ}/C$ for the CHB and by $360^{\circ}/C$ for the FC can be applied to the cells to produce a multilevel output waveform [5]. The PS-PWM method inherently reduces the input current harmonics of the CHB and balances the capacitor voltages of the FC.

The level-shifted PWM includes multiple carriers, which are shifted in amplitude for each possible output voltage level generated by the multilevel converter. The LS-PWM

strategies vary depending on the disposition of the level-shifted carriers. LS-PWM can be categorized as in-phase disposition (IPD-PWM), where all carriers are in phase; phase opposition disposition (POD-PWM), where all carriers above the zero reference are in phase, but below the zero reference are 180 phase-shifted; and alternate phase opposition disposition (APOD-PWM), where all carriers are alternatively in opposite disposition [72]. More details about PWM strategies can be found in [71, 85]. LS-PWM methods are more suited for the NPC, since each carrier signal can be easily related to each power switch.

The Space Vector PWM (SVPWM) used for the two-level standard inverter can be extended to multilevel converters. Since the number of voltage vectors is increased in multilevel converters, the computational cost and the algorithm complexity are also increased. However, the redundant switching states allow for selecting the optimal switching pattern, and this feature reduces the unbalance problems associate with multilevel converters. The degree of freedom in the selection of optimal switching states can be used to balance the capacitor voltages in NPC and FC.

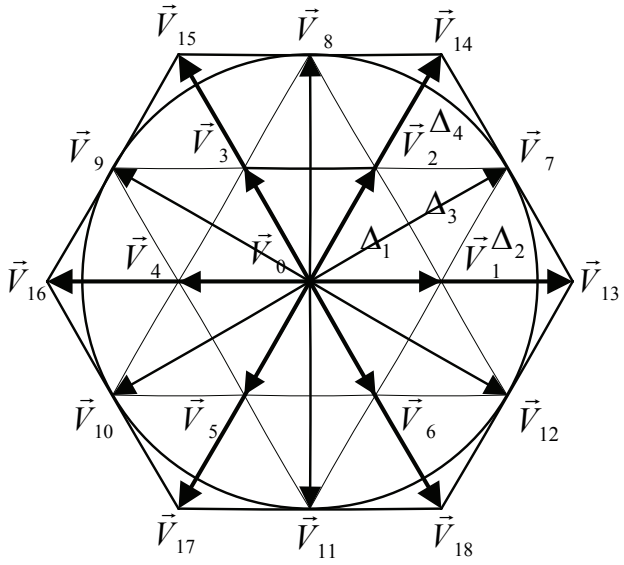


Figure 2-7: 3-level converter space vector block diagram

A space vector voltage block diagram of a three-level converter is shown in Figure 2-7. The SVPWM technique uses the three nearest voltage vectors to synthesize the reference voltage vector forming the switching sequence [94]. A linear combination of the three vectors generates an averaged output voltage equal to the reference over one switching period. A conventional multilevel SVPWM algorithm first identifies the sector and

triangle in which the reference vector falls, as shown in Figure 2-7. To find a triangle, a series of calculations involving the use of trigonometric functions is necessary. Next, by using a look-up table, the three voltage vectors can be identified. Finally, the SVPWM algorithm uses another series of trigonometric calculations to obtain the duty ratios of those vectors [5, 24].

Compared with other conventional SVPWM strategies, the recent SVPWM strategies have reduced the computational burden and the complexity of the algorithms [35, 73, 95, 96]. The triangle identification and duty cycles can be calculated by using very simple calculations. The new SVPWM does not require the calculation of trigonometric functions, or the use of look-up tables or coordinate system transformations. In addition, the algorithm can be easily extended to a higher number of the voltage levels without increasing the computational load.

Multilevel space vector control can also be used to approximate the reference voltage at the fundamental frequency by choosing the closest generable vectors since multilevel converters with a high number of voltage levels provide a high number of voltage vectors [97]. SVPWM with the natural fundamental switching frequency results in reduced switching losses for high-power application.

As an alternative, the selective harmonic elimination (SHE) method, or staircase modulation, can be applied to multilevel converters for high-power applications due to the reduction in the switching losses [98-102]. In this method, the inverter phase voltage V_{AN} is formed by a n-level staircase. The switching angles for the voltage levels are calculated to cancel the low-order harmonics. The staircase modulation is especially suitable for a CHB with several power cells. However, the complexity of the SHE schemes increases by increasing the number of voltage levels due to the increase in the number of switching angles and the corresponding number of polynomial equations which must be solved.

2.4. Multilevel Converter Applications

Many multilevel converter applications focus on industrial medium-voltage motor drives [50, 51, 70], flexible AC transmission system (FACTS) [103], and traction drive systems [51]. Multilevel converters also allow for power conversion between the utility and the renewable energy sources such as photovoltaic, wind, and fuel cells [104]. In addition, the application of multilevel converters in Hybrid Electric Vehicles (HEV) has

emerged as a very important alternative. To achieve high power and high voltage, a multilevel power converter can be used in HEV to interface with the power cell of the multiple dc voltage sources such as ultracapacitors and batteries [50].

The multilevel converter can also be used for loss-sensitive sustainable energy sources such as flywheel energy storage systems where the higher frequency PWM outputs with high-frequency fundamentals are essential to drive a high-speed machine. The minimum voltage and current THD are necessary to obtain high efficiency and a normal operation [4]. The four-level and three-level inverters were implemented for a high-speed drive system in [19, 105]. The standard inverter system with an inductor filter can be used to reduce the current THD. However, since in this type of the application, the fundamental frequency range varies by a few hundred Hertz, the AC inductor filter, which is usually designed to work with the constant fundamental frequency, cannot operate efficiently in this range and can produce a large voltage drop, which reduces the efficiency of the system. In addition, the high-power level and high-fundamental frequency limit the switching frequency. This problem can increase harmonics in the outputs. In addition, a flywheel energy storage system operating in a vacuum is very sensitive to rotor heating, which is associated with machine losses due to current (and voltage) harmonics. In [4], an increase in the switching frequency significantly improves THD and hence, lowers the stator current ripple and associated copper losses. Thus, the rotor heating caused by a temperature increase in the stator due to stator losses improves in a high-speed permanent magnet machine. By mitigating the above limitations, the CII topology is a good candidate and a suitable choice as an alternative multilevel topology for loss-sensitive applications.

2.5. Chapter Summary

This chapter presents a number of multilevel converter topologies. The basic principles of different multilevel converters are discussed, and for each multilevel topology, the three-level converter structures are explained. The coupled inductor inverter presents the superior features over standard inverters and the other 3-level inverters. A review of the various modulation techniques for multilevel converters is conducted. Finally, a few applications of multilevel converters are briefly described.

Chapter 3

Split-Wound Coupled Inductor Inverter Topology

As the primary subject of this thesis, the operation of an inverter topology using a coupled inductor (see Figure 3-1) is described. A simplified equivalent transformer model is used to clarify the operating modes of this topology. The inductor winding current and output current characteristics of the coupled inductor inverter (CII) are investigated, and related equations are derived. Winding and output current ripples are obtained from the effective inductance experienced by the coupled inductor at switching states. The continuous and discontinuous operation modes of CII are examined based on common mode current analysis. The different types of flux produced by the winding current are studied by using two types of cores: three-single cores and a three-limb core. All possible CII switching states are investigated by examining the different 3-phase coupled inductor winding configurations. The effects of these switching states and other factors like turn-on and off delays on the common mode current are explored. Finally, the ratings of CII switching devices are calculated.

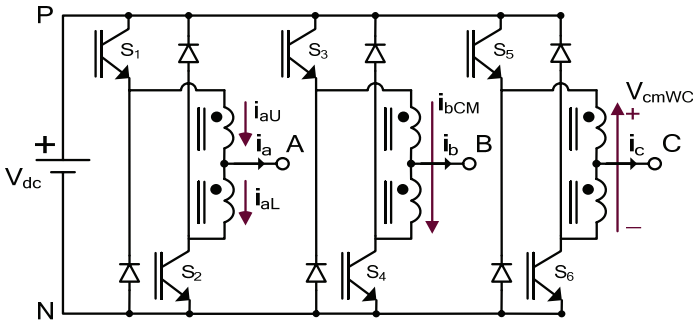


Figure 3-1: Three-phase multilevel coupled inductor inverter topology

3.1. Coupled Inductor Inverter Topology Description

The topology of the investigated 3-level coupled inductor inverter is shown in Figure 3-1 [2, 19]. Split-wound coupled inductors are placed at the inverter outputs between the upper and lower switches in each inverter leg. Each set of split-wound coupled inductors can be placed on one limb of three-single cores or a three-limb inductor core (as is the case in this research). Using a three-limb inductor core eliminates both fundamental

frequency and common mode dc flux in the core [18]. As a result, the magnetic core flux density becomes small, which produces a special core size benefit.

Unlike the standard inverters, the new topology produces a 3-level PWM output waveform from a single DC voltage level, filters output current ripples, reduces voltage stress and Electromagnetic Interference (EMI), and can double the effective output switching frequency. All these benefits improve the performance of standard inverters when using the coupled inductors. These features make this topology suitable for high-performance drives. For example, the output line-to-line voltage and phase current of this topology are depicted in Figure 3-2, which reveals that the line-to-line voltage is 3-level (0V, 150V and 300V), and the output phase current waveform is sinusoidal.

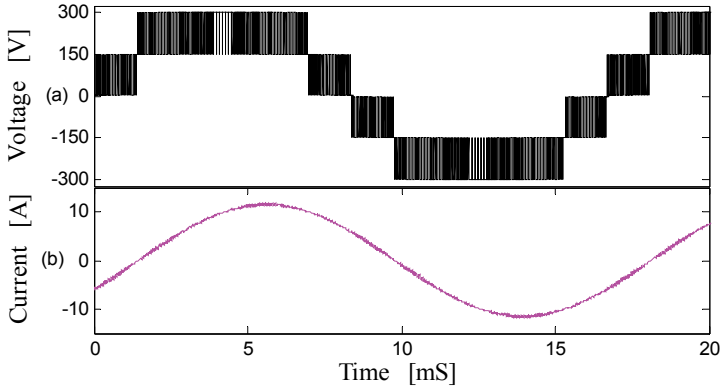


Figure 3-2: Simulated CII topology (a) line-line V_{AB} output voltage (b) phase A current (m_a=1.15, interleaved DPWM1, CII continuous conduction mode)

Since the split-wound coupled inductor is in series with the upper and lower switches, the necessity of having dead-time protection to avoid short-circuit currents in this topology is eliminated. However, standard and multilevel inverters do not provide this benefit. If the effect of dead-time protection is not compensated by using an analog or a digital PWM control unit [12, 14-16], the dead-time can reduce the per-unit phase voltage and produce potentially significant distortion over the inverter outputs [13, 17]. However, the CII topology not only enables operation without the need for dead-time compensation, but also allows for the overlapping of the upper and lower switches on-times in the PWM switching schemes. This unique property eliminates the effects of dead-time, produces an additional mid-point voltage, and can double the effective output switching frequency [2, 19]. Therefore, the modulation index for the CII topology can correspond with a higher phase voltage; harmonic distortion in the output waveforms can be improved significantly by increasing a third voltage level and doubling the effective

switching frequency.

3.2. CII Multi-Level Topology Operation

By comparing the operation of a single leg of the standard inverter with that of the CII topology, the output terminal voltage V_{AN} of the CII topology can generate an extra voltage level of $\frac{1}{2}V_{DC}$, in addition to V_{DC} and 0. In the standard inverter, the switching turn-on and off times of the upper and lower switches are complementary to avoid shorting the DC link. Each switch in one inverter leg cannot operate independently of the other one. However, in the CII inverter topology, the upper and lower switches can turn off and turn on simultaneously but not independently (this feature will be shown later in this chapter) to create the mid-voltage point.

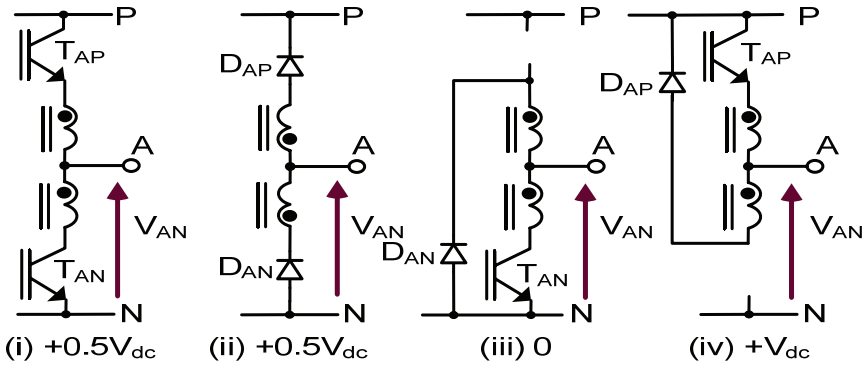


Figure 3-3: Switching states of a CII single leg

During the normal operation of the topology, both windings in the coupled inductor in each limb are conducting positive currents without crossing the zero current axes. This desirable operation mode of CII topology is called the "Continuous Conduction Mode." The inverter leg's basic switching states in the continuous conduction mode [19] are illustrated in Figure 3-3 with the 3 possible output voltage levels for V_{AN}. Basically, each leg of the three-phase inverter has four switching conditions. Both switches are on in Figure 3-3(i); both switches are off in Figure 3-3(ii); and either one switch is on while the other is off and one diode is conducting in Figure 3-3(iii) and Figure 3-3(iv). However, in the case of zero-current axis crossing, the winding current becomes zero and leads to the "Discontinuous Conduction Mode." This condition can happen for each phase when either only one diode or switch is conducting or when no device conducts. These discontinuous conditions are not suitable because one of the split-wound coupled inductor coils is not electrically wired to the circuit but magnetically is connected to the other

coils, and, as the experimental results in Figure 3-4 show, the quality of the outputs degrades, and, during the discontinuous period, the output voltage contains notches with an undefined voltage. These results demonstrate that proper PWM operation is not possible in the discontinuous conduction mode. To explore the difference between the output quality of the continuous and discontinuous modes, the fundamental rms and total harmonic distortion (THD) of the output waveforms are tabulated in Table 3-1. The results demonstrate that the rms value of the output voltage and output current is lower in the discontinuous mode. In addition, the continuous mode contains a lower harmonic content compared to that of the discontinuous mode. Thus, the discontinuous mode is not the optimal operating point of the inverter since this mode distorts the output waveforms and reduces the magnitude of the output voltage and current.

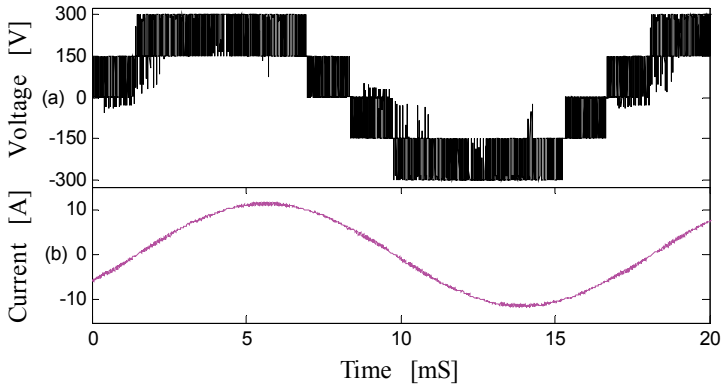


Figure 3-4 CII topology (a) line-to-line V_{AB} output voltage (b) phase A current (m_a=1.15, interleaved DPWM1, CII discontinuons conduction mode)

Table 3-1 CII fundamental rms and THD of the phase A current and V_{AB} voltage

Operating Mode	Continuous Conduction		Discontinuous Conduction	
	ia	V_{AB}	ia	V_{AB}
60 Hz	8.127 A	211.2 V	7.965 A	207 V
THD	1.60%	26.44%	1.78%	27.00%

In a three-level NPC inverter, the three-level output is obtained by using a neutral point connection to a center tapped DC link [5, 24]. However, Figure 3-3(i) and Figure 3-3(ii) illustrates that in the CII topology, the third voltage level is achieved by voltage division on the split wound inductor. When both the upper and lower switches turn on and off both simultaneously in each leg, a third voltage level of $\frac{1}{2}V_{dc}$ can be achieved. In Figure 3-3(i), when both switches are on, the total DC voltage bus, V_{dc}, is dropped across the split wound inductor, and since the coupling ratio between these two coils is one, and both coils are designed identically, the voltage splits evenly between the coils, and the

output terminal of $0.5V_{dc}$ is obtained. In the same way, in Figure 3-3(ii) when both switches are off, if the same polarity for the coupled inductor winding voltage is considered, $-V_{dc}$ is dropped across the inductor, but this time, again due to the orientation of the inductors, 0.5 V_{dc} can be obtained at the output. For the zero voltage (Figure 3-3(iii)) and V_{dc} voltage (Figure 3-3(iv)) outputs, the coupled inductor coils are shorted, and both sides of the inductor structure are tied either to the upper DC bus (P) or to the lower DC bus (N), respectively. The output terminal voltage for the various switching states (0– switch off, 1– switch on) is tabulated in Table 3-2. Each phase has 4 possible switching states. The combinations of switching states in each phase can be used to generate three-phase outputs.

Table 3-2 Switching states of the coupled inductor inverter

Switching State	Device Switching States								
	(Phase A)			(Phase B)			(Phase C)		
	S_1	S_2	V_{AN}	S_3	S_4	V_{BN}	S_5	S_6	V_{CN}
P	1	1	½V_{dc}	1	1	½ V_{dc}	1	1	½ V_{dc}
N	0	0	½V_{dc}	0	0	½ V_{dc}	0	0	½ V_{dc}
O	0	1	0	0	1	0	0	1	0
O	1	0	V_{dc}	1	0	V_{dc}	1	0	V_{dc}

3.3. CII Winding and Output Currents Equations

Based on the circuit configuration of the topology shown in Figure 3-3(i), (ii), (iii) and (iv), it can be concluded that the coupled inductor current is unidirectional and always flows from the top winding (with dot convection) to the bottom winding, indicating the presence of a positive common mode dc current. To illustrate the winding currents and output current relationships, an equivalent circuit for the coupled inductor in one limb is given in Figure 3-5.

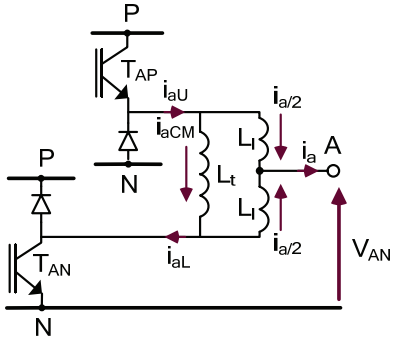


Figure 3-5: Transformer equivalent model of the coupled inductor

As Figure 3-5 reveals, the common DC current, i_{CM}, flows from the upper to the lower split-wound inductors. This current is the average of the upper and lower winding currents and is given by

$$i_{aCM} = \frac{i_{aU} + i_{aL}}{2}, \tag{3-1}$$

where i_{aU} and i_{aL} are upper and lower winding currents, respectively.

The output current is obtained by subtracting the upper and lower winding current and is given by

$$i_a = i_{aU} - i_{aL}. \tag{3-2}$$

Similarly, from equations (3-1) and (3-2), the winding currents can be rearranged based on the common mode current and output phase current as

$$i_{aU} = \frac{1}{2} i_a + i_{aCM} \tag{3-3}$$

$$i_{aL} = -\frac{1}{2} i_a + i_{aCM}. \tag{3-4}$$

To demonstrate these current relationships, the experimental results are given in Figure 3-6 and Figure 3-7. The upper and lower winding currents are illustrated in Figure 3-6. The common mode and phase A output currents are shown in Figure 3-7.

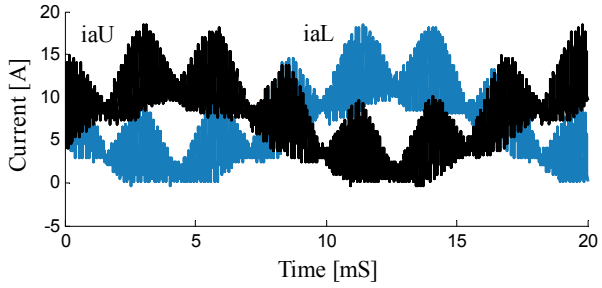


Figure 3-6: Experimental CII upper and lower winding currents (m_a= 0.9, SVPWM)

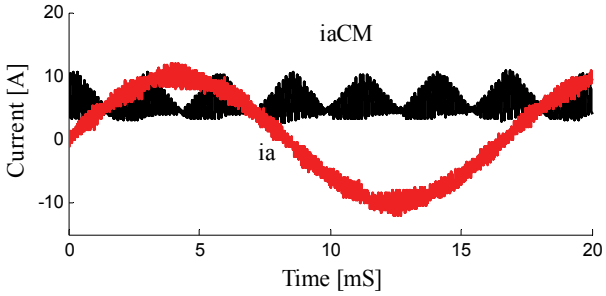


Figure 3-7: Calculated CII common mode current and experimental phase A current (m_a= 0.9, SVPWM)

In each phase, the common mode current is essentially a DC current (DC offset) with a high-frequency AC ripple at the switching frequency. The ideal winding DC offset current is approximately one-half of the maximum peak of the fundamental output current. Assuming that the winding currents are in the continuous conduction mode, equation (3-1) can be rewritten as

$$i_{aCM} = \frac{1}{2} i_{a\_peak} + i_{ac\_ripple}. \tag{3-5}$$

The value of i_{CM} can be controlled by using different operating modes and switching control algorithms. As mentioned before, the operation of the coupled inductor in the continuous conduction mode is the proper operating mode of this topology. This mode can be characterized by the symmetric winding currents waveforms depicted in Figure 3-6, where they are achieved with a satisfactory common mode current. The minimum common mode current for the continuous operating mode, as shown in Figure 3-7, is the average winding current. However, to overcome the discontinuous mode due to the variation of the high-frequency AC ripple current at the zero-current crossing, a very small DC bias is added to i_{CM}. Otherwise, if discontinuous conduction were to occur, the winding currents and the output voltage and current would be distorted.

3.4. CII Simplified Transformer Equivalent Model

The basic transformer equivalent circuit model given in Figure 3-5 is provided again in Figure 3-8. To demonstrate how the couple inductor impacts on the common mode current and output current, the model is simplified to two decoupled circuits. Figure 3-8(b) shows the output model, and Figure 3-8(c) demonstrates the circuit model between the switches.

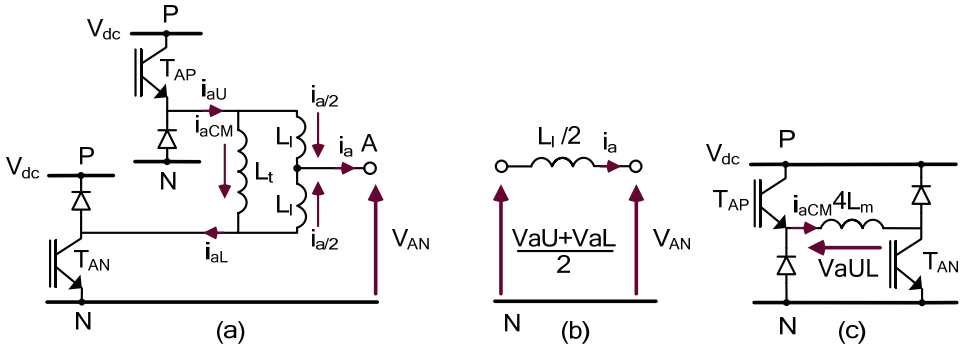


Figure 3-8: Equivalent circuits for the single phase inverter leg: (a) transformer equivalent model, (b) output model, (c) circuit model between the switches

In this model, the magnetizing inductance and leakage inductance are shown by L_m and L_l per winding, respectively. The split-wound coupled inductor is modeled with a simple transformer including magnetizing and leakage inductances as shown in Figure 3-8(a). Figure 3-8(b) shows the resultant inductance seen at the output terminal. Since the upper and lower windings are placed on one limb and tightly coupled magnetically with different polarities (dot convention), the fundamental AC magnetizing flux (inductance) in the upper winding is cancelled by that in the lower winding; only two parallel leakage fluxes (inductances) are left at the output. Thus, each winding leakage inductance contributes half of the output current. The resultant output inductance, L_s, seen in series with the output current at the 3-level output voltage, is

$$L_s = \frac{L_l}{2}. \tag{3-6}$$

On the other hand, the DC component of the split-wound inductor current, the common mode DC current, passes through the full magnetizing inductance of both windings. Because the inductance is proportional to the squared number of turns, and two winding coils with same number of turns are connected in series, the resultant magnetizing inductance, L_t, is quadruple the magnetizing inductance of one coil, L_m. This total magnetizing inductance L_t is equal to

$$L_t = 4L_m. \tag{3-7}$$

3.5. Coupled Inductor Winding and Output Current Ripples

As Figure 3-6 and Figure 3-7 reveals, in the CII topology, the coupled inductor winding currents and the output current contain high-frequency AC current ripples, and, as a result, this ripple exists in the common mode dc current. The simplified magnetizing model of the split-wound couple inductor shown in Figure 3-8 can be used to analyze these current ripples.

The high-frequency switching voltages over the total series-connected inductance of the coupled inductor produce the common mode ripple components in the winding currents (see Figure 3-6). The maximum peak-peak common mode ripple given in (3-8) is calculated when the square-wave voltage of the magnitude V_{dc} at the switching frequency f_s is across the total magnetizing inductance L_t and the sum leakage inductance $2L_l$ [23, 25]:

$$i_{ac\_peakpeak\_cm} = \frac{V_{dc}}{(L_t + 2L_l) \times 2f_s}. \tag{3-8}$$

By increasing the magnitude of the magnetizing inductance, the common mode ripple can be reduced. The required magnetizing inductance can be obtained by increasing the number of turns in the upper and lower inductor windings.

However, while in series with the PWM voltage source, the leakage inductance in each coil of the coupled inductor is conducting half of the output current. The maximum output ripple can be obtained when the inverter is switching a square wave voltage. Therefore, the output inductance including the sum of the leakage and filter inductances is exposed to a square wave with magnitude $V_{dc}/2$ at the effective switching frequency of $f_{s\_effective}$. The effective switching frequency depends on PWM schemes and can be doubled ($f_{s\_effective} = 2 \cdot fs$) by using a proper PWM switching pattern. The different PWM switching schemes will be explained in detail in chapter 4.

$$i_{ac\_peakpeak\_output} = \frac{V_{dc}/2/\sqrt{3}}{(L_s + L_{filter}) \times (2 f_{s\_effective})} = \frac{V_{dc}}{4\sqrt{3}(L_s + L_{filter}) f_{s\_effective}}. \quad (3\text{-}9)$$

Expressions (3-8) and (3-9) can now be used to predict or design the AC ripple properties of the system, based on the magnetizing and leakage inductances.

For comparison, the output current ripple when a standard inverter is used is given as

$$i_{ac\_peakpeak\_output} = \frac{V_{dc}/\sqrt{3}}{L_{filter} \times (2 f_s)} = \frac{V_{dc}}{2\sqrt{3} L_{filter} f_s}. \quad (3\text{-}10)$$

The current ripple in a standard inverter could be four times larger in magnitude and one-half the frequency of the ripple of the CII topology. If the filter inductance is required, this requirement will directly benefit the core size because of the reduced magnitude of the AC ripple flux. As well, if the same core and inductance are used, this topology provides the output waveform with a lower harmonic content and better quality than that of the standard inverter. The CII topology can reduce the power losses caused by the harmonic current and voltage and, as a result, can improve the load efficiency [19].

3.6. Split-Wound Coupled Inductor Flux

The winding current is composed of the fundamental current, common mode dc current, and high frequency AC ripple. Each of these components of the winding current can produce the flux inside the core. In total, three types of fluxes can be produced in the CII topology: the fundamental AC flux, common mode dc flux, and high-frequency AC flux.

Regardless of the type of split-wound inductor core used (i.e., three-single cores or three-lime core), since the upper and lower winding coils are placed on one limb in a core, the fundamental AC current does not produce a flux in the split-wound inductor core. The upper and lower winding each carries the half of the output current with a negative value (or opposite polarity). Thus, the upper and lower windings in each limb cancel the fundamental AC flux produced by another winding, and, as a result, the fundamental AC flux does not exist.

The common mode dc current does not contribute to the fundamental AC flux in the core but produces the dc flux in each limb in the core. This flux can be cancelled if a three-limb core is used. When the 3-phase core is chosen, the fluxes generated by the symmetrical windings on the limbs oppose each other, and so the dc flux in the core is eliminated. However, small parasitic dc magnetic fluxes can still be produced.

Since a high-frequency AC ripple current flows through the windings, a high-frequency AC flux exists in the core. This flux is generated because of the high-frequency switching voltages across the coils. The main factors contributing to the value of this flux are the switching frequency, switching sequence, switching states (or winding configuration), and the magnitude of the DC bus voltage [106]. The higher the switching frequency is, the lower the AC ripple current is.

Generally, in the CII topology, the three-phase coupled inductor can be designed by using the same design method used for linear inductors carrying a DC current with a high-frequency ripple [107, 108]. In the next section, two types of cores with their magnetic models are described. The reluctance circuit can be used to explore how the CII inverter topology operates with different types of cores.

3.7. Split-Wound Coupled Inductor Cores Types

The split-wound coupled inductor in the CII inverter topology can be placed on two types of cores [25]: a three-limb core (see Figure 3-9(a)) and three-separate cores (see Figure 3-9(b)).

A simplified reluctance equivalent circuit for each type of core is given in Figure 3-10. The main difference between the models is the flux return path in the core. Figure 3-10(a) shows the dependent flux paths in the three-phase cores. However, in Figure 3-10(b), the three-single cores' flux paths are independent.

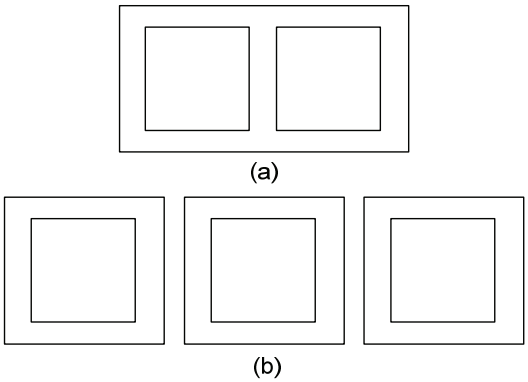


Figure 3-9: Coupled inductor core types a) three-limb core b) three-single cores

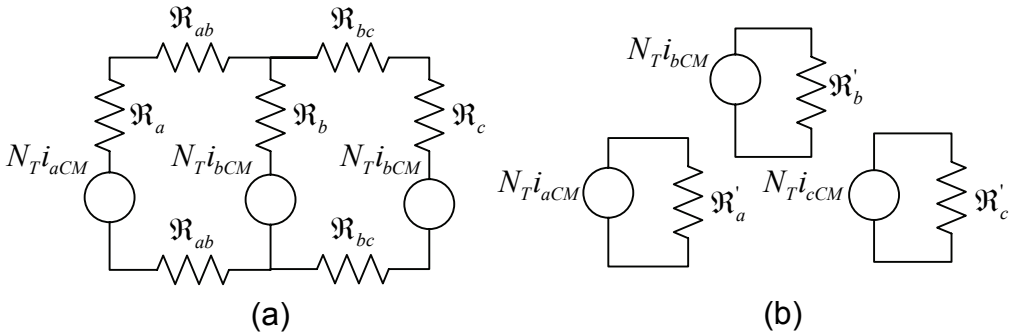


Figure 3-10: a) three-limb reluctance circuit b) three-single cores' reluctance circuit

3.7.1. Coupled Inductor Using Three-Single Cores

The three-phase coupled inductor using three-single cores and two windings per phase is shown in Figure 3-11. The flux of the separate core in each phase is independent of the flux in the other phases so that these fluxes are not mutually coupled. Thus, no interaction occurs between the phases due to the single-core coupled inductor structure. If the winding current passes through the inductor, the DC and high-frequency AC fluxes can flow through the reluctance circuit. Thus, only the common mode current including the high-frequency AC ripple produces the flux in the core.

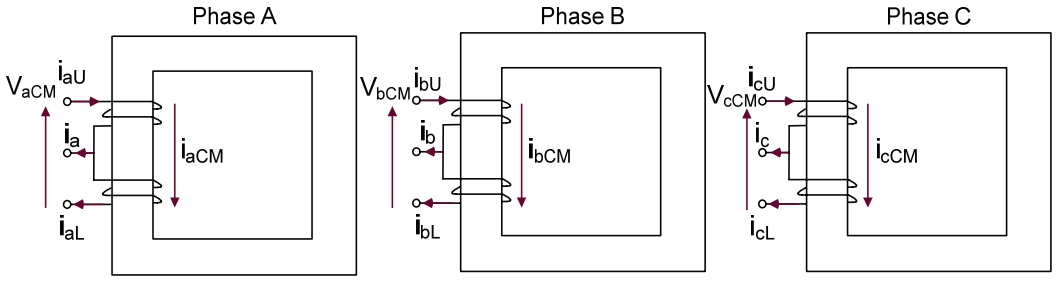


Figure 3-11: three-phase coupled inductor placed on three-single cores

In fact, when all three split wound inductors are magnetically decoupled, the relationship between the common mode voltage per phase and the corresponding magnetizing inductance that controls the common mode current ripple is given by

$$\begin{bmatrix} v_{aCM} \\ v_{bCM} \\ v_{cCM} \end{bmatrix} = \begin{bmatrix} 4L_m & 0 & 0 \\ 0 & 4L_m & 0 \\ 0 & 0 & 4L_m \end{bmatrix} \begin{bmatrix} i_{aCM} \\ i_{bCM} \\ i_{cCM} \end{bmatrix}. \tag{3-11}$$

Unfortunately, the main limitation on the size of the inductor is the DC flux in the core and inductor losses corresponding to the DC flux. The next section introduces the three-limb core and focuses on how to eliminate the DC flux that exists within with no DC flux return path.

3.7.2. Coupled Inductor Using a Three-Limb Core

The coupled inductor winding for each phase can be placed on a three-limb core structure as shown in Figure 3-9(a). The phases are mutually coupled to one another via the reluctance circuit given in Figure 3-10(a). The same number of turns is used for the upper and lower windings to produce the mid-point voltage of $V_{dc}/2$ at output. All limb reluctances and interlimb reluctances are approximately equal in Figure 3-10, and the number of turns for each phase is also the same. With this description, the DC Magnetic Motive Force (mmf) produced in each limb will be equal if the common mode winding currents are equal. As a result, DC flux will cancel out in a three-limb core. On the other hand, high-frequency AC fluxes are produced in the core due to the high-frequency AC current ripples which are not equal. Thus, the high-frequency fluxes in each limb are not the same. This situation would be catastrophic for the CII topology if all three limbs had identical high-frequency current components. In this case, the high-frequency fluxes in the core would cancel, shorting the switches in each limb and damaging of all switches [20].

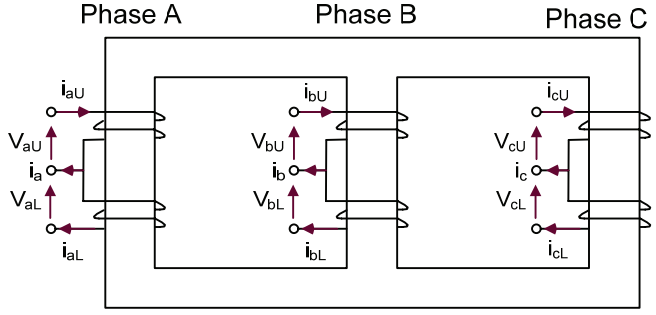


Figure 3-12: three-phase coupled inductor placed on a three-limb core

The three-phase coupled inductor using a three-limb core and two windings per phase is shown in Figure 3-12. This core geometry implies that the upper winding in phase A is coupled to all other windings, whereas with three independent cores, the upper winding in phase A is coupled only with the lower winding in phase A. With the interaction of the three phases in the three-limb core, fifteen coupling coefficients are defined such that the flux produced in one limb generates the opposite flux in each of the other two limbs. Based on the transformer model for the multiple coupled inductor windings [109-113], the relationship between the winding voltages and currents in three-limb core is given in

$$\begin{bmatrix} v_{aU} \\ v_{aL} \\ v_{bU} \\ v_{bL} \\ v_{cU} \\ v_{cL} \end{bmatrix} = \begin{bmatrix} r_{aU} & 0 & 0 & 0 & 0 & 0 \\ 0 & r_{aL} & 0 & 0 & 0 & 0 \\ 0 & 0 & r_{bU} & 0 & 0 & 0 \\ 0 & 0 & 0 & r_{bL} & 0 & 0 \\ 0 & 0 & 0 & 0 & r_{cU} & 0 \\ 0 & 0 & 0 & 0 & 0 & r_{cL} \end{bmatrix} \begin{bmatrix} i_{aU} \\ i_{aL} \\ i_{bU} \\ i_{bL} \\ i_{cU} \\ i_{cL} \end{bmatrix} + \tag{3-12}$$

$$\begin{bmatrix} M_{aUaU} & M_{aUaL} & M_{aUbU} & M_{aUbL} & M_{aUcU} & M_{aUcL} \\ M_{aLaU} & M_{aLaL} & M_{aLbU} & M_{aLbL} & M_{aLcU} & M_{aLcL} \\ M_{bUaU} & M_{bUaL} & M_{bUbU} & M_{bUbL} & M_{bUcU} & M_{bUcL} \\ M_{bLaU} & M_{bLaL} & M_{bLbU} & M_{bLbL} & M_{bLcU} & M_{bLcL} \\ M_{cUaU} & M_{cUaL} & M_{cUbU} & M_{cUbL} & M_{cUcU} & M_{cUcL} \\ M_{cLaU} & M_{cLaL} & M_{cLbU} & M_{cLbL} & M_{cLcU} & M_{cLcL} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{aU} \\ i_{aL} \\ i_{bU} \\ i_{bL} \\ i_{cU} \\ i_{cL} \end{bmatrix},$$

where r_x represent the winding resistances, M_{xx} is the self-inductance and M_{xy} is the mutual inductance coefficients (x and y are aU, aL, bU, bL, cU and cL). Since the number of turns for each winding in each phase is equal, the self-inductances are the same ($\approx 0.99\ L_t$), and the mutual inductance coefficients are equal.

Because the fundamental AC current does not produce a flux in the core, the above equation can be simplified by substituting equations (3-3) and (3-4) into (3-12). This gives three split wound inductors and a total of three windings in each phase that need coupling, as given in equation (3-13):

$$\begin{bmatrix} v_{aCM} \\ v_{bCM} \\ v_{cCM} \end{bmatrix} = \begin{bmatrix} r_a & 0 & 0 \\ 0 & r_a & 0 \\ 0 & 0 & r_b \end{bmatrix} \begin{bmatrix} i_{aCM} \\ i_{bCM} \\ i_{cCM} \end{bmatrix} + \begin{bmatrix} M_{aa} & M_{ab} & M_{ac} \\ M_{ba} & M_{bb} & M_{bc} \\ M_{ca} & M_{cb} & M_{cc} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{aCM} \\ i_{bCM} \\ i_{cCM} \end{bmatrix}, \tag{3-13}$$

where r_x represents the winding resistances, M_{xx} is the self-inductance, and M_{xy} is the mutual inductance coefficients (x and y are a, b and c).

Unlike the current in the three-single cores, the common mode current for each phase is now generated by the interaction of all three phases together. In equation (3-13), the common mode current ripple is considerably dependent to the coupling coefficient and, as a result, impacts on the winding current ripple. To illustrate this dependence, upper and lower windings and output currents are simulated in Figure 3-13 for $M_{xy} = -0.45L_t$ and in Figure 3-14 for $M_{xy} = -0.48L_t$. The results show that by changing the coupling coefficient from $-0.45L_t$ to $-0.48L_t$, (a factor of 6.25%), the winding current ripple is increased by a factor of about 3.

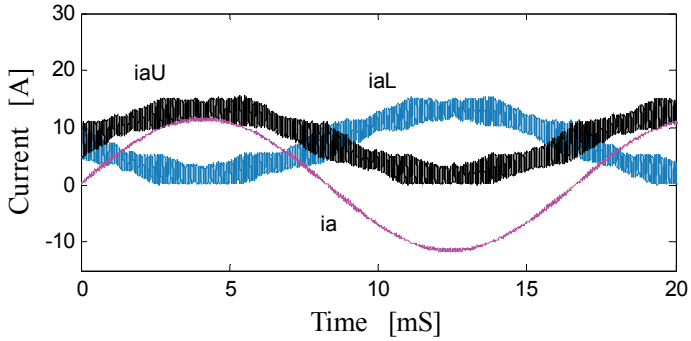


Figure 3-13: Simulated upper and lower winding currents and output current in phase A (m_a =1.15, Interleaved DPWM1, M_{xy} =-0.45L_t)

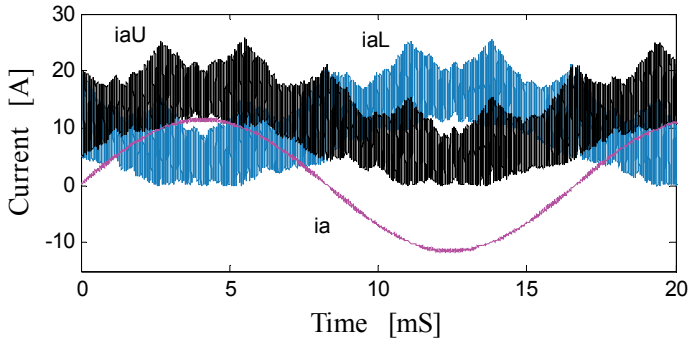


Figure 3-14: Simulated upper and lower winding currents and output current in phase A (m_a =1.15, Interleaved DPWM1, M_{xy} =-0.48L_t)

In this chapter, it has been shown that the common mode current is dependent on several factors: self-inductance, coupling inductance, and switching frequency. In chapter 5, it will be shown that this ripple depends on the modulation schemes as well.

3.8. CII Switching States

The impact of winding configurations on the effective inductance is investigated in this section. The effective inductances contribute mainly to the expected current ramping rate for the winding current and the corresponding common mode dc current in each

switching state. The effective inductance in each switching state determines the maximum high frequency current peak-peak ripple given in equation (3-8) [2]. The effective inductance does not have any significant effect on the output currents since only the leakage inductance can be seen from the output.

The 3-phase switching states of the CII topology with the 3-phase split-wound inductor using a 3-limb core are investigated. By considering the operation of all three legs of the inverter, each leg may take on one of the states given in Figure 3-3, so that the possible combinations of the switching states for all three phases are as shown in Figure 3-15. For the purposes of clarity, Figure 3-15 illustrates the split-wound inductor for each limb as a single coil, omitting the centre-tap.

Since all three coils are wound on a common three-limb core, the effective inductance of any coil is dependent on the connection of the other two coils. For example, the switching states (a) and (b) in Figure 3-15 produce the lowest effective winding inductance in all three legs, corresponding to the case when all inverter switches are either "on" or "off." Basically in these two conditions, all coils are energized or de-energized, respectively, canceling the majority of the flux in the core and producing a low effective inductance. If the core flux is eliminated, as occurs in switching states (a) and (b) in Figure 3-15, the switches can become short-circuited in each inverter leg, damaging all switches [20]. By using the same analysis, the next low-inductance switching states can be identified as cases (f) and (g) in Figure 3-15.

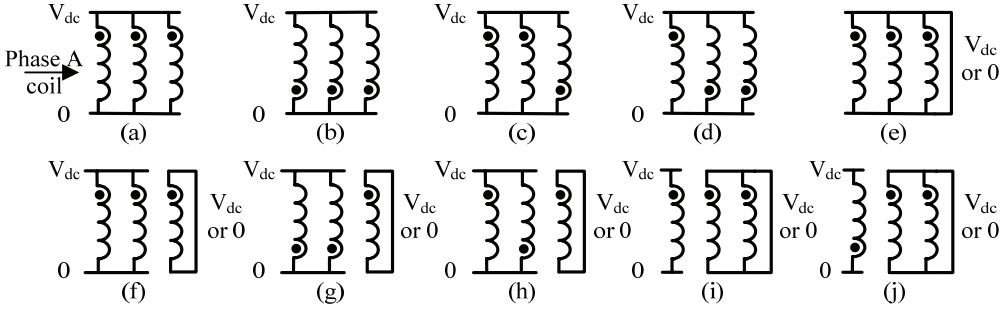


Figure 3-15: 3-phase coupled inductor configurations for various switching states

Many of the above low-inductance switching states happen when carrier-based PWM or conventional SVPWM schemes are used. For example, the switching states (a) and (b) in Figure 3-15 occur frequently when using a standard sinusoidal PWM [2]. They can be avoided by using a discontinuous PWM (DPWM1) [21, 24]. However, the switching states (f) and (g) take place in DPWM1. The aim of this research is to develop a new

switching pattern that can eliminate the effective low-inductance states and improve the winding current spectrum while providing high-quality outputs. These results will significantly reduce the winding and core losses in coupled inductors and, thereby, also can reduce the size of the core and its related cost.

3.9. Common Mode DC Current Analysis

This section describes the impact of the common mode dc current on the operation of coupled inductor inverters and explains how the switching states, turn-on and off delays, and device voltage drops affect the common mode dc current.

3.9.1. Impact of Common Mode DC Current on CII Operation

The common mode current is established by the common mode voltage across the coupled inductor. Basically, in the transient condition, the minimum common mode dc current is forced by the CII topology to the circuit, which is the average of the upper and lower winding currents. However, in the steady state, the average value of the winding common mode voltage determines the common mode DC bias. In the normal operation of this topology, the bias value is very small and close to zero. If the average winding voltage is zero, the common mode current is not biased and is marginal, but if the average winding voltage is a positive value (i.e., 0.1% of V_{dc}), then the common mode current is biased with a very small amount of DC, and this result helps to keep the operation of the CII inverter in the continuous conduction mode. To avoid the discontinuous conduction mode, a fixed DC bias is added to the common mode current by using PWM modulation schemes. In fact, the PWM switching signals using the switching states of (i) and (ii) in Figure 3-3 can significantly control the average common mode voltage. Therefore, control of the common mode current is very important to the operation of the coupled inductor inverter.

For example, the common mode current and the common mode winding voltage which appears across the coupled inductor are shown in Figure 3-16, which demonstrates that where the winding voltage is zero, the coupled inductor winding is shorted. However, the common mode current has been changed due to the coupling between the windings in the other phases. To illustrate the effect of the winding voltage, two periods of 2ms are extracted from Figure 3-16 and expanded in Figure 3-17 and Figure 3-18. Each figure shows three successive switching cycles.

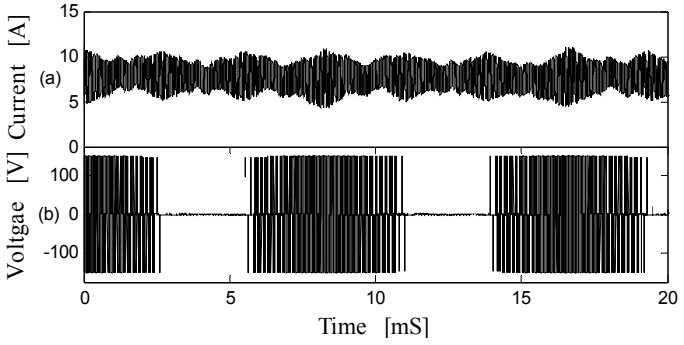


Figure 3-16: Phase A winding (a) common mode current (b) common mode winding voltage (m_a=1.15, interleaved DPWM1, f_s=15 kHz)

In Figure 3-17, the coupled inductor winding is shorted, and the common mode current varies due to the coupling effects of the other winding. However, in Figure 3-18, since the upper and lower switches' PWM signals are generated from anti-phase modulating signals, positive winding voltage occurs in the first half of the switching cycle and negative winding voltage occurs in the second half. Figure 3-18 reveals that the common mode current ramps follow the winding voltage changes in each switching cycle.

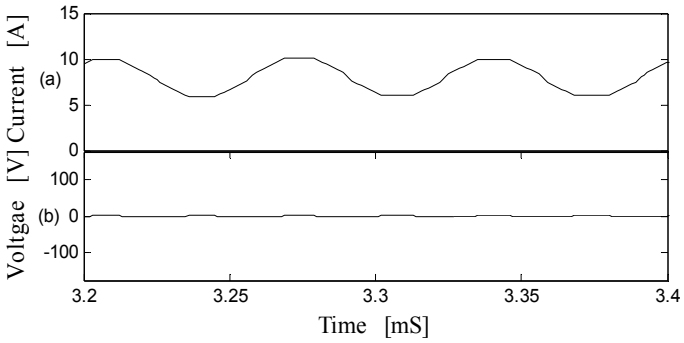


Figure 3-17: Phase A winding with the coupling effects: (a) common mode current (b) common mode winding voltage (m_a=1.15, interleaved DPWM1, f_s=15 kHz)

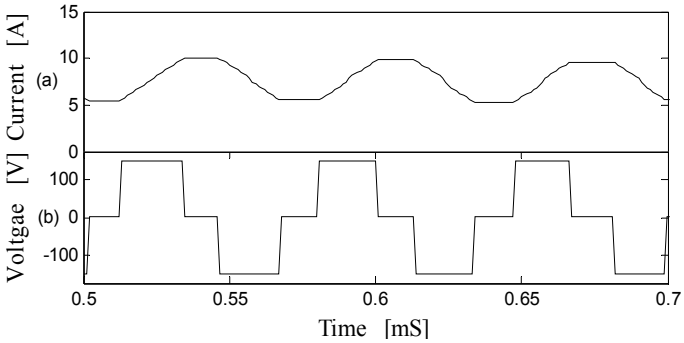


Figure 3-18: Phase A winding without the coupling effects: (a) common mode current (b) common mode winding voltage (m_a=1.15, interleaved DPWM1, f_s=15 kHz)

3.9.2. Impact of Switching States on Common Mode DC current

Four conduction modes were represented in Figure 3-3 for the continuous operation mode of (i) two-switch conduction, (ii) two-diode conduction, (iii) and (iv) one-switch conduction with one-diode conduction. The impact of the switching state on the common mode dc current is shown in Table 3-3. The switching state (i) increases and the switching state (ii) decreases the common mode dc current by applying $+V_{dc}$ and $-V_{dc}$ across the coupled inductor winding in each limb, respectively. The switching states (iii) and (iv) do not contribute to the common mode dc current since in this mode, the coupled inductors are shorted. Since the losses in the short-circuit pass are negligible during very brief periods of switching, the common mode dc current is maintained. The common mode current in one leg can be directly impacted by energizing or de-energizing the same leg, and can also be indirectly affected by coupling with the other leg when the switching states are (iii) and (iv). For instance, in cases (f) and (g) in Figure 3-15, two windings are energized or de-energized, but the third winding is shorted. The resultant flux caused by the energized or de-energized windings induces a voltage in the shorted winding. This voltage produces the current in the shorted winding, opposing the resultant flux caused by the other windings. However, if one winding is energized and the other one is de-energized, as in case (h) in Figure 3-15, the common dc current in the shorted winding is not influenced by the other windings, and its variation is negligible. In this case, the flux return pass for the energized winding is closed by the flux return pass from the de-energized winding.

Table 3-3 Switching states for phase A, together with impact on common mode dc current
(Assuming other windings are open circuit)

Switching type	S_1	S_2	V_{AN}	Circuit (Figure 3-3)	Coupled inductor winding	Common mode dc current
P	1	1	$½V_{dc}$	(i)	Energized	Increases
N	0	0	$½V_{dc}$	(ii)	De-energized	Decreases
O	0	1	0	(iii)	Short circuit	Constant
O	1	0	V_{dc}	(iv)	Short circuit	Constant

3.9.3. Impact of Switching Turn-On or Turn-Off Delays on Common Mode DC current

The magnitude of the common mode dc current can be controlled by the switching

turn-on or turn-off delays. In Figure 3-3 (i), the switch turn-off delays produce a positive voltage across the coupled inductor, generating a positive common mode dc offset. On the other hand, a turn-on delay (dead-time) causes the negative voltage to drop, producing a negative voltage across the coupled inductor. This voltage drop negates the common mode dc offset.

3.9.4. Impact of Device Voltage Drops on Common Mode DC current

In Figure 3-3(iii) and (iv), free-wheel diodes and coupled inductor resistor voltage drops decrease the common mode current gradually. For instance, for case (iv) in Figure 3-3, as the voltage at the lower winding is clamped to a positive supply through the freewheel diode, the forward voltage drop of the diode will decrease the average winding voltage, lowering the common mode current. For all cases in Figure 3-3, the average winding voltage and output voltage are lowered by device voltage drops.

3.10.Switching Device Rating Specifications

The voltage rating of each device is the same as that in the standard inverter [25]. However, the current rating for each device given by the rms of the winding current in (3-14) is smaller:

$$i_{aUrms} = i_{aLrms} = \sqrt{(\frac{i_{arms}}{2})^2 + i_{CM\,rms}^2}\,, \tag{3-14}$$

where the rms common mode current is

$$i_{CM\,rms} = \sqrt{(\frac{i_{a\_peak}}{2})^2 + i_{CM\_ripple\_rms}^2}\,, \tag{3-15}$$

and the rms value of the phase current is

$$i_{arms} = i_{apk} / \sqrt{2}\ . \tag{3-16}$$

By substituting (3-15) and (3-16) into (3-14), the rms of the winding current becomes

$$i_{aUrms} = i_{aLrms} = \sqrt{\frac{3}{8} i_{a\_peak}^2 + i_{CM,ripple,rms}^2}\ . \tag{3-17}$$

If the value of the common mode ripple is negligible, the current rating of each semiconductor switch can be reduced by 15% compared to that of the standard inverter.

3.11. Chapter Summary

The operation of the CII topology is described, and the performance is investigated. The unique operating characteristics of this inverter are explored. The continuous and discontinuous operating modes of the CII inverter are explained, and the common mode current is introduced as a main factor for controlling the operating mode. A very small dc bias is needed to establish symmetric operation of the coupled-inductor windings currents. The basic transformer model of the coupled inductor is explained by using three-single cores and a three-limb core. The three-limb core shows better performance than the three-single cores by eliminating the DC flux. Since the only inductance that can be seen at the output of this inverter is the leakage inductance, the coupled inductor is actually transparent to the output. The self and mutual magnetizing inductances can be optimized without concern for output linearity, and this feature can improve the performance of the CII inverter by reducing the size of the core and lowering the coupled inductor losses. With 3-level output line-line voltage, reduced output current ripple, lowered output THD, and dead-time free operation, the CII topology is one of the multi-level topologies that can be used for high-performance applications like high-speed drives, as is demonstrated in [19, 114].

Chapter 4

Coupled Inductor Inverter PWM Modulation Strategies

Pulse width modulation (PWM) strategies, including the discontinuous modulation schemes used for a standard inverter, can be modified and applied to the multilevel coupled inductor inverter. However, when using any modulation scheme, care must be taken to balance the common mode winding current (voltage) over the switching period for the continuous mode of operation and to generate multi-level voltages with low harmonic content [18, 19, 23, 106, 115].

The significance of various PWM modulation strategies on the performance of the CII is explored in this chapter. Carrier-based PWM schemes for the multilevel CII topologies are described and new multilevel space vector PWM methods are investigated and developed to improve the performance of the CII topology. The PWM switching techniques are categorized as follows:

- **Interleaved carrier-based PWM**
  - Sinusoidal Pulse Width Modulation (SPWM)
  - Discontinuous Pulse Width Modulation (DPWM1)
- **Multilevel Space vector PWM (SVPWM)**
  - Original SVPWM
  - SVPWM with optimal switching selection (Improved SVPWM)
  - Interleaved discontinuous SVPWM (DSVPWM)

The SVPWM methods are different in terms of switching states and sequences. The original SVPWM and improved SVPWM methods have 5-segment switching sequences, and the DSVPWM has a 9-segment switching sequence. The original and improved SVPWMs balance the common mode current (voltage) over two successive switching cycles whereas the DSVPWM balances the common mode current during one switching cycle. This feature has a significant impact on the winding current ripple in different methods. In addition, the effective switching frequency for each method varies depending on SVPWM switching states and switching sequences. The effective output switching frequency significantly contributes to the output current ripple.

4.1. The Significance of Using Different PWM Strategies

The selection of an optimal modulation strategy is essential to ensure the high-performance operation of the multi-level coupled inductor inverter topology. Successful operation of the CII topology over the full modulation range relies on selecting switching states and sequences where the coupled inductor presents a low winding current ripple and a high effective inductance between the upper and lower switches in each inverter leg (the high inductance state). As a result, a low high-frequency winding current ripple is produced, reducing the coupled inductor losses and improving the inverter's overall performance [22, 106].

Although the DC flux is removed in the three-limb core structure, the rms of the AC ripple flux increases due to the coupling between the inductors in the inverter legs compared to the three-single cores structure, which has similar effects on the core losses [20, 25]. The PWM switching with the ability to minimize the AC ripple of the high-frequency common mode current ripple allows for smaller core losses. In addition, most importantly, minimizing the peak flux density allows for core materials (such as ferrites) to be used, resulting much lower core losses than those created by core materials designed to cope with a large flux density [25, 116].

The presence of the coupled inductors in this inverter allows for the interleaved PWM switching of the upper and lower switches in each inverter leg to be an effective switching technique for this topology by increasing the effective switching frequency of the output PWM waveforms above the actual switching frequency. The interleaved PWM technique can be used to lower the size of the output AC filter and lower the high-frequency harmonics [2, 8-11, 19, 114, 117-120].

In general, the PWM modulation strategies for the CII configuration can be classified into two major categories: interleaved carrier-based PWM and multilevel space vector PWM. When using carrier-based standard PWM schemes, the switching states in each switching cycle are not selected arbitrarily but chosen by the reference waveform. Uncontrolled switching states can produce low effective inductance connections and produce a large high-frequency current ripple in the inductor windings, resulting in high winding Joule losses, core losses, and high-frequency leakage flux outside the magnetic core. Even though the output voltage and current waveforms have low harmonic content, the inverter winding current contains high harmonic distortion [22, 106]. Thus, even with high-quality output signals, the overall performance of the CII can be poor due to the

coupled inductor losses. If switching states are uncontrolled, the coupled inductor must be oversized to provide sufficient effective inductance in all switching cases.

As an alternative, the multi-level SVPWM technique for CII topology can offer superior performance and features over previous modulation schemes by particularly addressing the issues related to the common mode dc current balance and ripple minimization. Since each voltage vector can be generated by redundant switching states, the SVPWM method can be used to eliminate the low-inductance switching states in the CII that lower the high-frequency inductor winding current ripple. A careful analysis of the space vector reveals that the winding current ripple depends on not only the selection of the switching states but also their sequences. The order of voltage vectors in each sequence during a switching cycle can be arranged to minimize the winding current ripple [19, 24, 106, 115].

Consequently, by generating a multi-level output voltage waveform, SVPWM provides some choices for switching states and sequences. When used efficiently, an optimal PWM strategy allows an appropriate balance between the need to produce a multi-level output and the proper management of the inductor winding currents and effective inductance.

4.2. Interleaved Carrier-Based PWM

This section describes the interleaved switching strategy for carrier-based PWM schemes and shows how to obtain the interleaved upper- and lower-switch gate signals in the CII topology.

The interleaved switching can be achieved by using either two modulating waves of the same magnitude and frequency but 180° out of phase compared with a common triangular carrier wave or two triangular carrier waves 180° out of phase compared with a common modulating wave. This selection of references and carriers enables overlapping switch states (Figure 3-3(i) and Figure 3-3(ii)) to occur in each switching cycle, increasing the effective output switching frequency [2, 19]. As mentioned in chapter 3, section 3.9.2, overlapping switch states can control the common mode dc current as well. Thus, this feature should be considered when designing any PWM switching method for the CII topology. In the case where two references waveforms 180° out of phase are used, in order to balance the common mode dc current in each switching cycle, the instantaneous modulation signals are interleaved such that the upper and lower switches

per-unit duty cycle always sum to unity. As a result, both overlapping switch states are placed in each switching cycle with the same period, and thus, they cancel out each other's effects on the common mode dc current. As a result, at each point of time, the sum of two modulating signals is:

$$m_{Ap} + m_{An} = 1, \tag{4-1}$$

where m_{Ap} and m_{An} are the instantaneous values of the upper and lower switches reference waveforms in each switching cycle. In addition to this basic relationship, small deviations in m_{Ap} and m_{An} can allow a small dc voltage drop across the coupled inductor windings to be controlled, hence allowing control of the common mode dc current.

By using the interleaved technique, the initial interleaved carrier-based modulations—the interleaved Sinusoidal PWM (SPWM) and the Discontinuous PWM (DWPM1)—were developed and applied to the CII topology in [2, 19]. These modulation schemes are described in the following sections for this topology.

4.2.1. Interleaved Sinusoidal PWM (SPWM)

The SPWM technique is adopted from 2-level continuous PWM schemes for standard inverters. For PWM switching of one inverter leg, the SPWM modulation technique normally requires two sinusoidal modulating waves, v_{m+} and v_{m-}, which are of the same magnitude and frequency but 180° out of phase as shown in Figure 4-1. The two modulating waves are compared with a common triangular carrier wave v_{cr}, generating two gating signals, v_{g1} and v_{g3}, for the upper switches, S_1 and S_3, respectively. Figure 4-1 reveals that the upper and lower devices in one inverter leg can switch simultaneously.

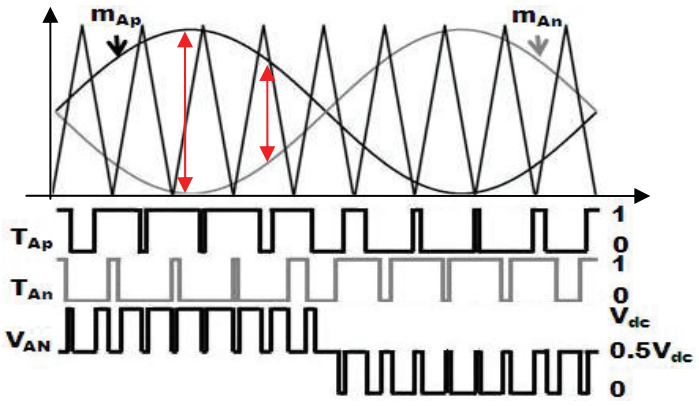


Figure 4-1: Interleaved SPWM: PWM control and gate signals, and phase A PWM voltage (m_a=0.9 and m_f=9) [19]

To increase the linear operation range, the third harmonic can be added to the reference waveform [24]. The SPWM with a third harmonic injected is used for the SPWM results presented in this thesis. In interleaved carrier-based PWM methods, the DC offset components of the upper and lower PWM signals can be controlled to give the desired dc bias level to the common mode current. Using symmetric winding offsets ensures the output current offset remains zero.

In Figure 4-2, a three-level PWM line-line voltage is demonstrated by using three-phase interleaved SPWM. The output voltage around the peak voltage is switching between 0 and ± V_{dc}, resulting in high THD of the output voltage waveforms and high dv/dt around the peak voltage. Since the three-phase switching states cannot be selected freely, low-inductance switching states of {11 11 11} and {00 00 00}, configuration (a) and (b) in Figure 3-15, occur frequently when using interleaved SPWM [2]. As shown in chapter 5, these factors cause the interleaved sinusoidal PWM method to produce excessive winding current ripples, especially when m_a is low, resulting in high winding and core losses, with a high-frequency leakage flux produced outside the magnetic core [2, 22, 106].

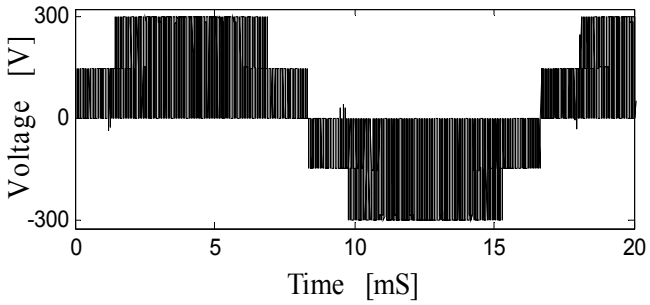


Figure 4-2: Simulated SPWM: line-line output voltage of the CII inverter (m_a =0.9, f_c=15 kHz)

4.2.2. Interleaved Discontinuous PWM (DPWM1)

The method of clamping a phase leg output voltage to the dc voltage bus is called discontinuous pulse width modulation (DPWM). The DPWM1 scheme, created by a 60º discontinuous PWM in each positive and negative peak cycle of the inverter voltage, generates a multi-level voltage with lower harmonic content and lower switching losses compared to the SPWM in the CII circuit [2, 19, 21]. The DPWM1 control method uses zero-sequence discontinuous-type signals to augment the sinusoidal reference in each switching cycle; only two inverter phase legs are switching while the third phase leg (where the selected phase after 120 degree changes in a cyclic manner over one

fundamental period) is clamped to the dc voltage bus at N or P points. Table 4-1 demonstrates the DPWM1 switching logic for each phase corresponding to the output phase voltage of the CII topology. The switching signals and related the phase PWM voltage for one inverter leg are shown in Figure 4-3. The PWM switching exists in each single phase for 120° at the fundamental cycle.

Table 4-1: Interleaved DPWM1 switching sequence [24, 25]

Reference Phase	Phase A	Phase B	Phase C
0-60	PWM	LOW	PWM
60-120	HIGH	PWM	PWM
120-180	PWM	PWM	LOW
180-240	PWM	HIGH	PWM
240-300	LOW	PWM	PWM
300-360	PWM	PWM	HIGH

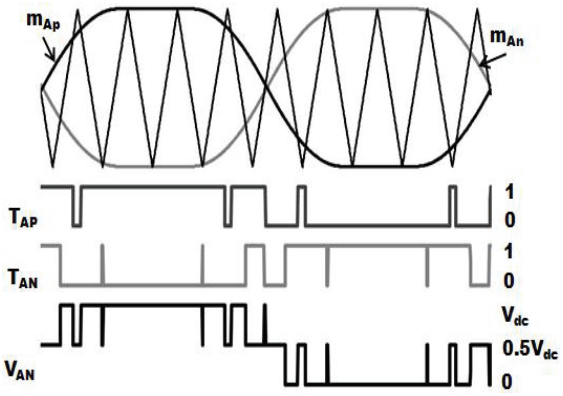


Figure 4-3: Interleaved discontinuous PWM: PWM control and gate signals, and phase A PWM voltage (m_a=1.15 and m_f=9) [19]

The DPWM1 method allows the CII structure to minimize the winding current ripple because this method eliminates the direct effects of the non-switching leg around the peak voltage and reduces the effects of the coupling between the inductor windings in a three-limb core with only two inverter legs actively PWM at a given time; the common mode ripple in the non-switching leg is indirectly affected by the other two legs because of the flux pass created by the magnetizing inductance of the windings as the non-switching leg has a flux return path. In addition, compared to SPWM, DPWM1 has a lower dv/dt at the peak line-line voltage, and this feature can reduce the output current ripple. These characteristics make the discontinuous PWM method one of the suitable PWM strategies for the CII topology.

One of the advantages of the DPWM1 method is that 60º discontinuous regions exist in the inverter's terminal voltages but not in the line-line voltages and the load phase voltages to the load neutral point. The discontinuous regions decrease the switching losses since the average switching frequency is reduced to 2/3 the instantaneous switching frequency. However, unlike discontinuous PWM methods used for standard inverters, the DPWM1 method not only does not degrade the quality of the load voltages (since the non-active regions cannot be seen in the load voltages), but also increases the output PWM frequency to double the instantaneous switching frequency. For example, Figure 4-4 demonstrates a PWM line-to-line voltage, obtained by DPWM1 with the cancellation of non-active regions in the inverter terminal voltage.

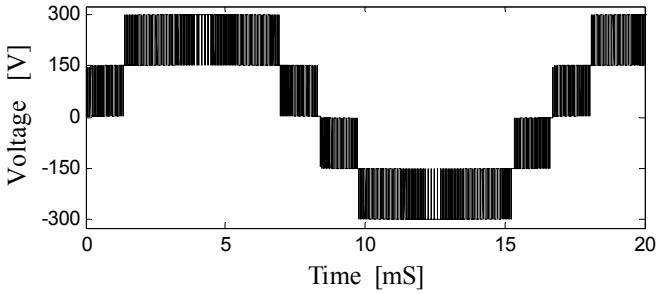


Figure 4-4: Simulated DPWM1: line-line output voltage of the CII inverter (m_a =0.9, f_c=15 kHz)

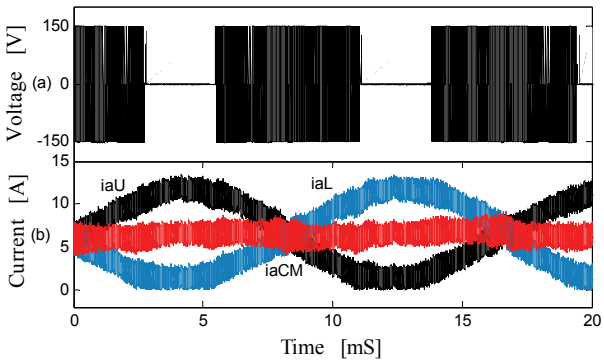


Figure 4-5: Simulated DPWM1: (a) common mode winding voltage (b) common mode current and winding currents in phase A (m_a =0.9, f_c=30 kHz)

A zero winding voltage across the split wound inductor for phase A in the 60° inactive regions is shown in Figure 4-5, which reveals that the common mode current ripple is changing while the phase A couple inductor windings are not either energized or de-energized because no switch activity is occurring. In fact, the coupling between the phases in the three-limb core is controlling the common mode ripple magnitude. Because of Faraday's law, the changing flux produced by the switch activity in the other two

phases induces a common mode voltage (in opposite polarity) across phase A's split-wound inductor structure.

Another advantage of the DPWM1 method is that the low-inductance switching states in SPWM can be avoided by using DPWM1 [2, 114]. However, careful inspection of the DPWM1 switching states in [24] demonstrates that the next low-inductance switching states {11 11 01}, {00 00 10}, and etc. (configuration (f) and (g) in Figure 3-15) take place in DPWM1. To minimize the current ripple, having a switching scheme which eliminates the low-inductance switching states is essential.

4.3. Multilevel Space Vector Modulation

When carrier-based modulations, interleaved SPWM and DPWM1, are used, the switching states are determined by the reference waveform. Thus, the switching states cannot be selected arbitrarily. The ripple and harmonic content of the coupled inductor's winding currents depend on the switching states in each of the three inverter legs [106, 115]. To obtain a lower winding current ripple, switching states with a low inductance should be avoided. However, carrier-based modulations result in frequent use of low-inductance states, which can be eliminated by using the space vector pulse width modulation (SVPWM).

SVPWM is one of the preferred real-time modulation techniques and has been widely used for multilevel inverters [5, 24]. In this section, as an alternative, the multilevel SVPWM strategy for the CII topology is presented to provide some choices over the switching states and sequences. In fact, the main benefit of SVPWM is the precise identification of pulse placement that can be used to optimize the CII operation. The operation of the CII topology can be affected by the imbalance common mode dc current and the winding current ripple [18]. When used efficiently, SVPWM allows for an appropriate balance between the need to properly manage the common mode winding currents (voltages) and to achieve harmonic performance gains while producing the multi-level output voltages. This section presents the principles of the multilevel space vector modulation for the CII inverter.

4.3.1. Switching States

The operating status of the switches in each inverter leg (Figure 3-1) can be represented by the switching states as shown in Table 4-2. Switching state 'P' denotes

that the upper and lower switches in the inverter leg are on. In this condition, the common mode current increases (ramps up). Similarly, switching state 'N' denotes that the upper and lower switches in the inverter leg are off. In this condition, the common mode current decreases (ramps down). In contrast, 'O' indicates that either the upper or lower switches are on so that the common mode current is maintained. For example, the switching state {10 00 11} corresponds to the conduction of S_1, S_5, and S_6 while S_2, S_3, and S_4 are off in the inverter legs A, B, and C, respectively.

Table 4-2: Switching states of the coupled inductor inverter
(Logic 1 means switch S_1 on, logic 0 means off)

Switching State	Device Switching States								
	(Phase A)			(Phase B)			(Phase C)		
	S_1	S_2	V_{AN}	S_3	S_4	V_{BN}	S_5	S_6	V_{CN}
P	1	1	½V_{dc}	1	1	½ V_{dc}	1	1	½ V_{dc}
N	0	0	½V_{dc}	0	0	½ V_{dc}	0	0	½ V_{dc}
O	0	1	0	0	1	0	0	1	0
O	1	0	V_{dc}	1	0	V_{dc}	1	0	V_{dc}

4.3.2. Space Vector Equations for 3-Phase Switching States

In this section, the relationship between the space voltage vectors and switching states is derived. If we assume the three-phase balanced operation of the inverter, the relationship between phase voltages A, B and C is as follows:

$$v_{AO}(t) + v_{BO}(t) + V_{CO}(t) = 0, \tag{4-2}$$

where V_{AO}, V_{BO}, and V_{CO} are the instantaneous load phase voltages. A space vector voltage can be generally expressed in terms of the α-β voltages in the stationary coordination as

$$\vec{v}(t) = v_{\alpha}(t) + jV_{\beta}(t). \tag{4-3}$$

The three-phase variables can be transformed into equivalent α-β variables by

$$\begin{bmatrix} v_{\alpha}(t) \\ V_{\beta}(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{AO}(t) \\ v_{BO}(t) \\ V_{CO}(t) \end{bmatrix}. \tag{4-4}$$

Substituting (4-4) into (4-3), we have

$$\vec{v}(t) = \frac{2}{3}(v_{AO}(t)e^{j0} + v_{BO}(t)e^{j2\pi/3} + V_{CO}(t)e^{j4\pi/3}). \tag{4-5}$$

For example, for the active switching state {10 00 11}, the generated load phase voltages are

$$v_{AO}(t) = \frac{1}{3}v_{dc},\ v_{BO}(t) = -\frac{1}{6}V_{dc},\ V_{CO}(t) = -\frac{1}{6}v_{dc}. \tag{4-6}$$

The corresponding space vector voltage, denoted as V_1, can be obtained by substituting (4-6) into (4-5):

$$\vec{V}_1 = \frac{Vdc}{3}e^0. \tag{4-7}$$

Taking into account all the switching states in the three phases, Table 4-3 illustrates the possible voltage vectors with the corresponding switching state for each winding configuration. In total, 64 possible combinations of switching states are in the CII topology as listed in Table 4-3. In addition to the switching states, the load phase voltages and the corresponding output voltage vectors in the polar coordinates are also listed in Table 4-3. The 64 switching states consists of 10 zero states and 54 active states.

4.3.3. Voltage Vectors Categories

The possible voltage vectors corresponding to the switching states in Table 4-3 with the 3-phase coupled inductor winding configuration for each switching state are depicted in Table 4-4. 64 voltage vectors are obtained from 64 switching states. Since the switching states have redundancies in generating the same voltage vector, in total there are 18 active voltage vectors plus a zero voltage vector. The voltage vectors are categorized as zero, small ($V_{dc}/3$), medium ($V_{dc}/\sqrt{3}$) and large vectors ($2V_{dc}/3$). The impact of the various switching states on the common mode currents is also shown in Table 4-4. In one or more inverter legs, the switching state type-P increases the common mode current, and the switching state type-N decreases. The switching state type-PN has both effects but on the common mode current in different phases. The switching state type-O does not affect the common mode current.

Table 4-3: Switching states corresponding to each space voltage vector

	State of Inverters' Switches						Load Phase Voltages			Output voltage	
	S_1	S_2	S_3	S_4	S_5	S_6	V_{AO}	V_{BO}	V_{CO}	Phase	Amplitude
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	1	Vdc/6	Vdc/6	-Vdc/3	60	0.3333
3	0	0	0	0	1	0	-Vdc/6	-Vdc/6	Vdc/3	-120	0.3333
4	0	0	0	0	1	1	0	0	0	0	0
5	0	0	0	1	0	0	Vdc/6	-Vdc/3	Vdc/6	-60	0.3333
6	0	0	0	1	0	1	Vdc/3	-Vdc/6	-Vdc/6	0	0.3333
7	0	0	0	1	1	0	0	-Vdc/2	Vdc/2	-90	0.5774
8	0	0	0	1	1	1	Vdc/6	-Vdc/3	Vdc/6	-60	0.3333
9	0	0	1	0	0	0	-Vdc/6	Vdc/3	-Vdc/6	120	0.3333
10	0	0	1	0	0	1	0	Vdc/2	-Vdc/2	90	0.5774
11	0	0	1	0	1	0	-Vdc/3	Vdc/6	Vdc/6	180	0.3333
12	0	0	1	0	1	1	-Vdc/6	Vdc/3	-Vdc/6	120	0.3333
13	0	0	1	1	0	0	0	0	0	0	0
14	0	0	1	1	0	1	Vdc/6	Vdc/6	-Vdc/3	60	0.3333
15	0	0	1	1	1	0	-Vdc/6	-Vdc/6	Vdc/3	-120	0.3333
16	0	0	1	1	1	1	0	0	0	0	0
17	0	1	0	0	0	0	Vdc/3	Vdc/6	Vdc/6	180	0.3333
18	0	1	0	0	0	1	-Vdc/6	Vdc/3	-Vdc/6	120	0.3333
19	0	1	0	0	1	0	-Vdc/2	0	Vdc/2	-150	0.5774
20	0	1	0	0	1	1	-Vdc/3	Vdc/6	Vdc/6	180	0.3333
21	0	1	0	1	0	0	-Vdc/6	-Vdc/6	Vdc/3	-120	0.3333
22	0	1	0	1	0	1	0	0	0	0	0
23	0	1	0	1	1	0	-Vdc/2	-Vdc/2	Vdc/2	-120	0.6667
24	0	1	0	1	1	1	-Vdc/6	-Vdc/6	Vdc/3	-120	0.3333
25	0	1	1	0	0	0	-Vdc/2	Vdc/2	0	150	0.5774
26	0	1	1	0	0	1	-Vdc/2	Vdc/2	-Vdc/2	120	0.6667
27	0	1	1	0	1	0	-Vdc/2	Vdc/2	Vdc/2	180	0.6667
28	0	1	1	0	1	1	-Vdc/2	Vdc/2	0	150	0.5774
29	0	1	1	1	0	0	-Vdc/3	Vdc/6	Vdc/6	180	0.3333
30	0	1	1	1	0	1	-Vdc/6	Vdc/3	-Vdc/6	120	0.3333
31	0	1	1	1	1	0	-Vdc/2	0	Vdc/2	-150	0.5774
32	0	1	1	1	1	1	-Vdc/3	Vdc/6	Vdc/6	180	0.3333
33	1	0	0	0	0	0	Vdc/3	-Vdc/6	-Vdc/6	0	0.3333
34	1	0	0	0	0	1	Vdc/2	0	-Vdc/2	30	0.5774
35	1	0	0	0	1	0	Vdc/2	0	Vdc/2	-60	0.3333
36	1	0	0	0	1	1	Vdc/3	-Vdc/6	-Vdc/6	0	0.3333
37	1	0	0	1	0	0	Vdc/2	-Vdc/2	0	-30	0.5774
38	1	0	0	1	0	1	Vdc/2	-Vdc/2	-Vdc/2	0	0.6667
39	1	0	0	1	1	0	Vdc/2	-Vdc/2	Vdc/2	-60	0.6667
40	1	0	0	1	1	1	Vdc/2	-Vdc/2	0	-30	0.5774
41	1	0	1	0	0	0	Vdc/2	Vdc/2	0	60	0.3333
42	1	0	1	0	0	1	Vdc/2	Vdc/2	-Vdc/2	60	0.6667
43	1	0	1	0	1	0	0	0	0	0	0
44	1	0	1	0	1	1	Vdc/2	Vdc/2	0	60	0.3333
45	1	0	1	1	0	0	Vdc/3	-Vdc/6	-Vdc/6	0	0.3333
46	1	0	1	1	0	1	Vdc/2	0	-Vdc/2	30	0.5774
47	1	0	1	1	1	0	Vdc/2	0	Vdc/2	-60	0.3333
48	1	0	1	1	1	1	Vdc/3	-Vdc/6	-Vdc/6	0	0.3333
49	1	1	0	0	0	0	0	0	0	0	0
50	1	1	0	0	0	1	Vdc/6	Vdc/6	-Vdc/3	60	0.3333
51	1	1	0	0	1	0	-Vdc/6	-Vdc/6	Vdc/3	-120	0.3333
52	1	1	0	0	1	1	0	0	0	0	0
53	1	1	0	1	0	0	Vdc/6	-Vdc/3	Vdc/6	-60	0.3333
54	1	1	0	1	0	1	Vdc/3	-Vdc/6	-Vdc/6	0	0.3333
55	1	1	0	1	1	0	0	-Vdc/2	Vdc/2	-90	0.5774
56	1	1	0	1	1	1	Vdc/6	-Vdc/3	Vdc/6	-60	0.3333
57	1	1	1	0	0	0	-Vdc/6	Vdc/3	-Vdc/6	120	0.3333
58	1	1	1	0	0	1	0	Vdc/2	-Vdc/2	90	0.5774
59	1	1	1	0	1	0	-Vdc/3	Vdc/6	Vdc/6	180	0.3333
60	1	1	1	0	1	1	-Vdc/6	Vdc/3	-Vdc/6	120	0.3333
61	1	1	1	1	0	0	0	0	0	0	0
62	1	1	1	1	0	1	Vdc/6	Vdc/6	-Vdc/3	60	0.3333
63	1	1	1	1	1	0	-Vdc/6	-Vdc/6	Vdc/3	-120	0.3333
64	1	1	1	1	1	1	0	0	0	0	0

Table 4-4(a): Zero voltage vectors with the corresponding switching states and configurations

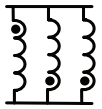
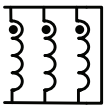
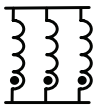
Zero Voltage Vector	NP-type  (d)	NP-type  (c)	O-type  (e)	O-type  (a)	O-type  (b)	Vector Phase Angle
$\vec{V}_0$	{11 00 00}	{00 11 11}	{01 01 01}	{11 11 11}	{00 00 00}	0
	{00 11 00}	{11 00 11}	{10 10 10}			0
	{00 00 11}	{11 11 00}				0

Table 4-4(b): Small voltage vectors with the corresponding switching states and configurations

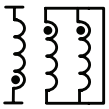
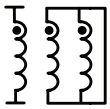
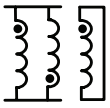
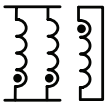
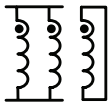
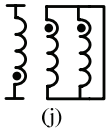
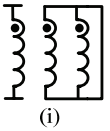
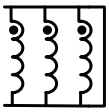
Small Voltage Vector $\frac{1}{3}Vdc$	N-type  (j)	P-type  (i)	NP-type  (h)	NP-type	N-type  (g)	P-type  (f)	Vector Phase Angle
$\vec{V}_1$	{00 01 01}	{11 01 01}	{10 00 11}	{10 11 00}	{10 00 00}	{10 11 11}	0
$\vec{V}_2$	{10 10 00}	{10 10 11}	{00 11 01}	{11 00 01}	{00 00 01}	{11 11 01}	π / 3
$\vec{V}_3$	{01 00 01}	{01 11 01}	{00 10 11}	{11 10 00}	{00 10 00}	{11 10 11}	2π / 3
$\vec{V}_4$	{00 10 10}	{11 10 10}	{01 00 11}	{01 11 00}	{01 00 00}	{01 11 11}	π
$\vec{V}_5$	{01 01 00}	{01 01 11}	{00 11 10}	{11 00 10}	{00 00 10}	{11 11 10}	4π / 3
$\vec{V}_6$	{10 00 10}	{10 11 10}	{00 01 11}	{11 01 00}	{00 01 00}	{11 01 11}	5π / 3

Table 4-4(c): Medium and large voltage vectors with the corresponding switching states and configurations

Medium Voltage Vector $\frac{1}{\sqrt{3}}Vdc$	N-type  (j)	P-type  (i)	Vector Phase Angle
$\vec{V}_7$	{10 00 01}	{10 11 01}	π / 6
$\vec{V}_8$	{00 10 01}	{11 10 01}	π / 2
$\vec{V}_9$	{01 10 00}	{01 10 11}	5π / 6
$\vec{V}_{10}$	{01 00 10}	{01 11 10}	$-5\pi/6$
$\vec{V}_{11}$	{00 01 10}	{11 01 10}	$-\pi$ / 2
$\vec{V}_{12}$	{10 01 00}	{10 01 11}	$-\pi$ / 6

Large Voltage Vector $\frac{2}{3}Vdc$	O-type  (e)	Vector Phase Angle
$\vec{V}_{13}$	{10 01 01}	0
$\vec{V}_{14}$	{10 10 01}	π / 3
$\vec{V}_{15}$	{01 10 01}	2π / 3
$\vec{V}_{16}$	{01 10 10}	π
$\vec{V}_{17}$	{01 01 10}	4π / 3
$\vec{V}_{18}$	{10 01 10}	5π / 3

4.3.4. Space Vector Block Diagram

The space vector diagram of the 3-phase 3-level CII including the switching state corresponding to each voltage vector is depicted in Figure 4-6. This diagram is similar to that of typical 3-phase 3-level inverter [5, 24] since the number of voltage levels are the same in both cases. However, the switching state required to generate similar voltage vectors is specific to each multi-level topology. In this topology, the overlapping switching states are a unique feature, eliminating dead-time considerations. The space vector block diagram in Figure 4-6 shows 19 effective voltage space vectors, including a zero voltage space vector, with the corresponding switching states for each voltage vector. The space vector block diagram has been divided into six 60 degree sectors (I, II, III, IV, V, and VI). Each sector consists of 4 triangles (Δ_1, Δ_2, Δ_3, Δ_4). The tip of the reference vector can be located within any triangle, and each triangle vertex represents a switching vector. This vector represents one or more switching states depending on its location.

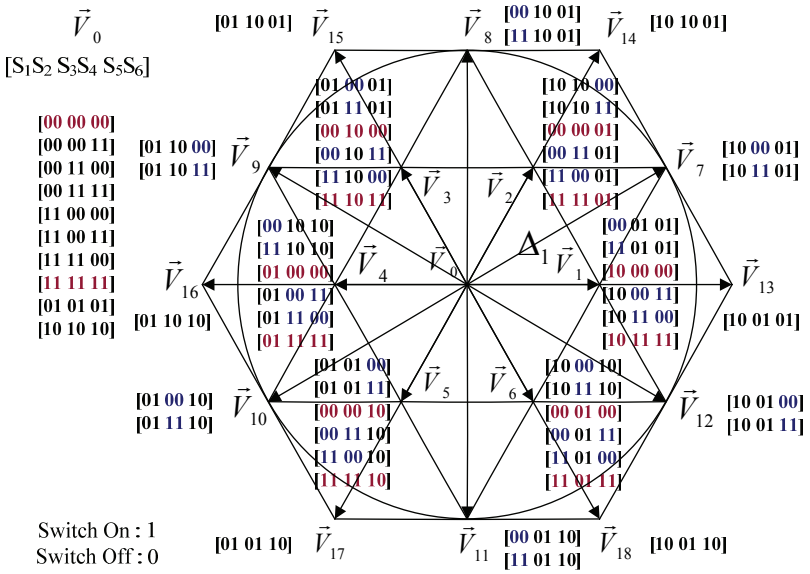


Figure 4-6: CII space vector diagram including switching states

A careful analysis of the space vector diagram reveals that the performance of the inverter depends on the selection of switching states and their sequences [22, 106, 115]. Each voltage vector has redundant switching states. By selecting an appropriate switching state for each voltage vector, winding current ripple can be reduced. The switching sequence should be designed to also decrease the current ripple while increasing the

effective output switching frequency and lowering the switching losses. These processes can lower the inverter losses by reducing the coupled inductor losses and switching losses. These properties constitute the key features of the proposed SVPWM approaches.

4.3.5. Dwell Time Calculation

Similar to the standard SVPWM algorithm for multi-level inverters, the multilevel space vector modulation for the CII inverter is also based on the "volt-second balancing" principle. To minimize the harmonic distortion in the voltage, the reference vector is approximated by the time averaging of the nearest three vectors, V_x, V_y, and V_z according to (4-8) and (4-9):

$$\vec{V}_{ref} = (d_x\vec{V}_x + d_y\vec{V}_y + d_z\vec{V}_z)/T_s \quad (4\text{-}8)$$

$$T_s = d_x + d_y + d_z, \quad (4\text{-}9)$$

where d_x, d_y, d_z are the dwell time of V_x, V_y, and V_z, respectively. The three nearest vectors and their dwell times can be determined by finding the triangle where the reference vector lies in than the hexagon [35]. V_{ref} can also be synthesized by using other space vectors instead of the "nearest three." However, doing so will cause higher harmonic distortion in the inverter output voltage, and this result is undesirable in most cases.

4.3.6. Switching Sequence Design

In each triangle in Figure 4-6, a switching sequence is formed by using the best combination among all possible switching states at the vertices for the three nearest voltage vectors. The appropriate switching states are chosen based on the effective inductance values and preferred configurations as given in Table 4-5; the switching sequences are designed to minimize the current ripple and the number of switching occurrences per cycle. Among different types of switching sequences, the most popular ones are (i) the 7-segment and (ii) the 5-segment types [5]. The 7-segment sequence is difficult to apply to the CII topology because either the switching transient in each time interval becomes more than 2 for at least one of the 6 switches, or the symmetrical PWM pulses corresponding to the middle of the switching period can not be produced. For this reason, the approach used in this thesis applies a 5-segment switching sequence as a basic structure to design the switching sequences. The basic 5-segment switching sequence is shown in Figure 4-7.

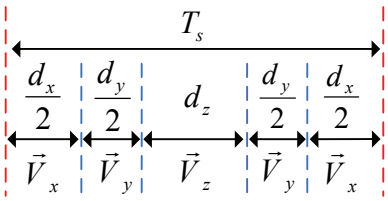


Figure 4-7: SVPWM basic 5-segment switching sequence

4.3.7. Selection of Winding Configurations for Voltage Vectors

The coupled inductor current ripple magnitude is dependent on the coupled inductor effective inductance for each switching state. Depending on each switching state, the coupled inductor configuration changes, so that the effective inductance value between the upper and lower switches in an inverter leg varies. Since effective inductance depends on the switching state, selecting the switching state with the highest possible effective inductance (the lowest current ripple) for each voltage vector results in reduced winding current harmonic distortion [22, 106, 115].

The effect of the various switching states on each voltage vector level is investigated. In Figure 4-6, the voltage vectors are categorized as zero (vectors 1), small (vectors 1 to 6), medium (vectors 7 to 12) and large vectors (vectors 13 to 18). Careful inspection of the switching states for the vectors in Figure 4-6, as well as the coil connections shown in Figure 3-15, indicates the available inductor configurations for each state as shown in

Table 4-4. Large and medium voltage vectors are generated only from specific winding configurations. A large voltage vector is possible only when the inverter output voltages are all either V_{dc} or zero, as shown in Figure 3-15(e) (type-O). Similarly, medium voltages are possible only with the inductor configurations shown in Figure 3-15(i) (type-N) and Figure 3-15(j) (type-P). Therefore, the choices of winding configurations for medium and large voltage vectors are limited; winding configurations with high inductances and low current ripple can not be freely chosen. The effective inductance affected by the winding configuration stays the same for these voltage levels.

However, for small and zero voltage vectors, various winding configurations can be chosen so that the lowest effective inductance states can be determined and eliminated from SVPWM switching sequences. For a zero voltage vector, the winding configurations shown in Figure 3-15(a) and Figure 3-15(b) have the lowest inductance. In this case, all three coupled inductors in each leg are energized or de-energized together, canceling the majority of the flux in the core and producing the lowest effective

inductance compared to all winding configurations. In Figure 3-15(e), none of the windings are energized or de-energized. Thus, the coupled inductor windings do not impact on each other. In fact, no high-frequency AC ripple current is flowing in the windings. Similarly, for small voltage vectors, the winding configurations of Figure 3-15(f) and Figure 3-15(g) have the lowest inductance since in these configurations, the coupled inductor in two legs are energized or de-energized, and the third one is shorted. The high-frequency flux due to energized or de-energized coils induces a voltage in the shorted coil. This voltage produces a high-frequency current, and, as result, a high-frequency flux generates to oppose the resulting flux of the energized or de-energized coils. Since two coils are energized or de-energized, the high-frequency current ripples in the configurations in Figure 3-15(f) and Figure 3-15(g) are larger than those in the configurations in Figure 3-15(i) and Figure 3-15(j), where the configurations have one coil energized. The winding configuration in Figure 3-15(h), in comparison with those in Figure 3-15(i) and Figure 3-15(j), has a larger effective inductance because the high-frequency flux generated by the split-wound coupled inductor flux in one leg is absorbed by split-wound coupled inductor flux in the other leg. The high-frequency flux pass is closed by two limbs in the core with high permeability compared to the air in the configurations of Figure 3-15(i) and Figure 3-15(j). Therefore, the lower reluctance and the higher inductance are achieved for configuration (h) in Figure 3-15. In addition, the shorted coil is not affected due to the other coils.

Table 4-5: Ranked switching states for each voltage level based on the effective winding inductance (Largest to smallest from left to right)

Type of vector	Winding Configuration (Figure 3-15)		
Zero Voltage	(e) (no AC flux)	(c) , (d)	(a) , (b)
Small Voltage	(h)	(i) , (j)	(f) , (g)
Medium Voltage	(i) , (j)	–	–
Large Voltage	(e) (no AC flux)	–	–

Combinations of possible inductor configurations for each size of voltage vector are presented in Table 4-5, grouped by the magnitude of the effective coil inductance; i.e., if possible, a small voltage should be obtained by using the configuration in Figure 3-15(h) in preference to those in Figure 3-15(i) and Figure 3-15(j), which are, in turn, preferable to those in Figure 3-15(f) and Figure 3-15(g). In fact, the expected current ramping rate

for the winding in each switching state is related to the effective inductance, and, as a result, the largest effective inductance minimizes the winding current and common mode dc current ripples.

4.3.8. Common Mode Current Balance

The switching states and sequences for a given vector must be chosen carefully to ensure that the average common mode voltage applied to the windings on each limb is maintained at about zero value. As the preceding discussion demonstrated, equivalent output voltages may be obtained for different switching states, which may act to either increase or decrease the common mode dc current. To ensure that the common mode dc current is not ramped excessively in one direction or the other, the proposed SVPWM scheme should alternate switching states and/or the switching sequence. To minimize the common mode current deviation, the dwell time of a given P-type and N-type switching state for the coupled inductor in each phase should be equally distributed over the sampling periods, which could be one or two successive switching cycles.

4.3.9. Even-Order Voltage Harmonic Elimination

To cancel even line-to-line voltage harmonics, half-wave symmetry is applied in the selection of switching states [5, 81]. To do so, each voltage vector in one sector is given one other voltage vector 180º apart, generating the same voltage in each leg but with an opposite polarity. This vector is placed in the same sequence with the same dwell time of the initial vector. For example, if the voltage sequence is $\{V_7V_2V_1V_2V_7\}$ in sector I-Δ_3, then in IV-Δ_3, 180º apart, the selected voltage sequence is $\{V_{10}V_5V_4V_5V_{10}\}$. V_{10}, V_5, and V_4 are complementary of V_7, V_2, and V_1, respectively, and have the same dwell time. If the upper and lower switch position of a given leg is {01}, then 180º away it is {10} and vice versa. However, if the switching position of a given leg is {00} or {11} in a sector, the switching position of the same leg is either {00} or {11}, in a sector 180º away.

To summarize, the switching sequences are selected to minimize the number of switching occurrences per switching cycle and the transitions required for V_{ref} when moving from one sector to another. The general criteria for choosing the switching states in the switching sequence are summarized as follows:

(a) Minimize the effect of the switching state on the inductor winding common mode current deviation.

(b) Select a high-effective inductance switching state wherever possible.

(c) Maintain half-wave symmetry to cancel even line-to-line voltage harmonics.

The reminder of this chapter focuses on these criteria to find an optimal switching sequence with appropriate switching states. Various SVPWM modulation schemes are developed and investigated which differ in terms of the designs of their switching sequences and switching states. The performance comparisons of the SVPWM methods with the CII topology will be demonstrated through simulation results and experimental tests in chapter 5.

4.4. Original SVPWM

The original SVPWM scheme is the initial multilevel SVPWM algorithm developed for the CII topology [106]. In this method, a switching sequence is formed by applying the appropriate switching states chosen from all possible switching states at the vertices in each triangle in Figure 4-6. The switching states are chosen based on the effective inductance values and preferred configurations as given in Table 4-5. To ensure that the common mode dc current is not ramped excessively in one direction or the other, the original SVPWM scheme alternates the switching sequence in successive switching cycles.

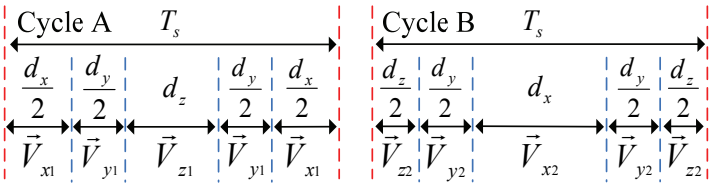


Figure 4-8: Original SVPWM switching sequence

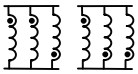
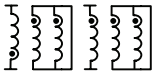
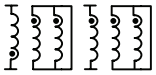
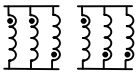
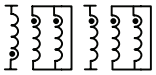
Figure 4-8 illustrates the switching sequence for this approach. *dx, dy* and *dz* are allocated dwell times for the voltage vectors of a given triangle (Figure 4-6) with vertex V_x, V_y and V_z, respectively. In the first switching cycle "A," the voltages are applied in the order x-y-z-y-x. In the following switching cycle "B," the voltages are applied in the order z-y-x-y-z. The total dwell times for each voltage vector in cycle A and B are the same. However, each voltage vector of x, y, or z in cycle B has opposite effects on the common mode dc current ramp in each limb compared with the same voltage vector in cycle A. For example, consider the case when V_x is {11 00 00} in cycle A and {00 11 11} in cycle B: the two switching states generate the same voltage vector in each inverter leg

with opposite effects on the common dc currents. This approach ensures that the common mode winding voltage in each phase is balanced over each pair of switching cycles in a given triangle. As a result, the corresponding common mode current in each leg is directly balanced by the same leg winding voltage; the effects of the coupling between the windings from other legs also are canceled due to the balanced average winding voltage for each winding over each pair of switching cycles.

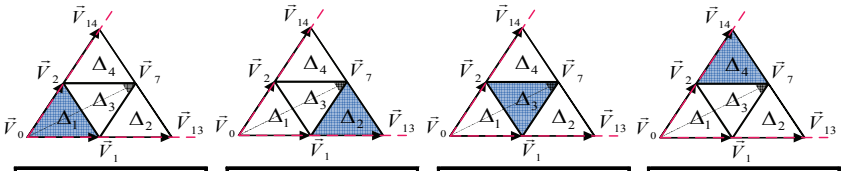
4.4.1. Implementation of Original SVPWM

By using the original SVPWM approach discussed in the pervious section, two possible 5-segment switching sequences are investigated in this section. By properly selecting the switching states, the low-inductance switching states of (a), (b), (f) and (g) in Figure 3-15 are eliminated for zero and small voltage vectors in both sequences. However, in sequence 2, the switching state of Figure 3-15(h) with a higher inductance is chosen instead of the switching states of (i) and (j) in Figure 3-15 in sequence 1. The selected switching states for each voltage level in sequences 1 and 2 are shown in Table 4-6.

Table 4-6: Original SVPWM switching states for sequence 1 and 2

Type of vector	Zero Voltage (V_0)	Small Voltage (V_1 to V_6)	Medium Voltage (V_7 to V_{12})	Large Voltage (V_{13} to V_{18})
Switching states for sequence 1	 (c) (d)	 (j) (i)	 (j) (i)	 (e)
Switching states for sequence 2	 (c) (d)	 (h)	 (j) (i)	 (e)

The switching states of sequences 1 and 2 are illustrated in segment I of the space-vector diagram in Figure 4-9 and Figure 4-11, respectively. The resulting common mode winding voltages for each phase in each triangle in sector I are plotted in Figure 4-10 and Figure 4-12. The switching sequences in Figure 4-9 and Figure 4-11 indicate the proposed method is continuous SVPWM when m_a is low (m_a<0.5) and becomes discontinuous SVPWM when m_a is high (m_a>0.5) (note that the maximum m_a is 1.0). Specifically, in sequence 1, continuous SVPWM is observed in triangle Δ_1 while discontinuous SVPWM is observed in Δ_2 for phase C and in Δ_3 , Δ_4 for phase A. In sequence 2, continuous SVPWM is observed in triangles Δ_1 and Δ_3, while discontinuous SVPWM for phases A and C is observed in Δ_2 and Δ_4, respectively.



Sector I-Δ_1	
Cycle A Vectors	
$\vec{V}_{x1}$	[11 00 00]
$\vec{V}_{y1}$	[11 00 01]
$\vec{V}_{z1}$	[11 01 01]
$\vec{V}_{y1}$	[11 00 01]
$\vec{V}_{x1}$	[11 00 00]
Cycle B Vectors	
$\vec{V}_{z2}$	[00 01 01]
$\vec{V}_{y2}$	[00 11 01]
$\vec{V}_{x2}$	[00 11 11]
$\vec{V}_{y2}$	[00 11 01]
$\vec{V}_{z2}$	[00 01 01]

Sector I-Δ_2	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 01 01]
$\vec{V}_{z1}$	[11 01 01]
$\vec{V}_{y1}$	[10 01 01]
$\vec{V}_{x1}$	[10 00 01]
Cycle B Vectors	
$\vec{V}_{z2}$	[00 01 01]
$\vec{V}_{y2}$	[10 01 01]
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 01 01]
$\vec{V}_{z2}$	[00 01 01]

Sector I-Δ_3	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 00 11]
$\vec{V}_{z1}$	[10 10 11]
$\vec{V}_{y1}$	[10 00 11]
$\vec{V}_{x1}$	[10 00 01]
Cycle B Vectors	
$\vec{V}_{z2}$	[10 10 00]
$\vec{V}_{y2}$	[10 11 00]
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 11 00]
$\vec{V}_{z2}$	[10 10 00]

Sector I-Δ_4	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 10 01]
$\vec{V}_{z1}$	[10 10 11]
$\vec{V}_{y1}$	[10 10 01]
$\vec{V}_{x1}$	[10 00 01]
Cycle B Vectors	
$\vec{V}_{z2}$	[10 10 00]
$\vec{V}_{y2}$	[10 10 01]
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 10 01]
$\vec{V}_{z2}$	[10 10 00]

Figure 4-9: Original SVPWM: switching states in sector I with the elimination of (a), (b), (f) and (g) inductor configurations for zero and small voltage vectors, sequence 1

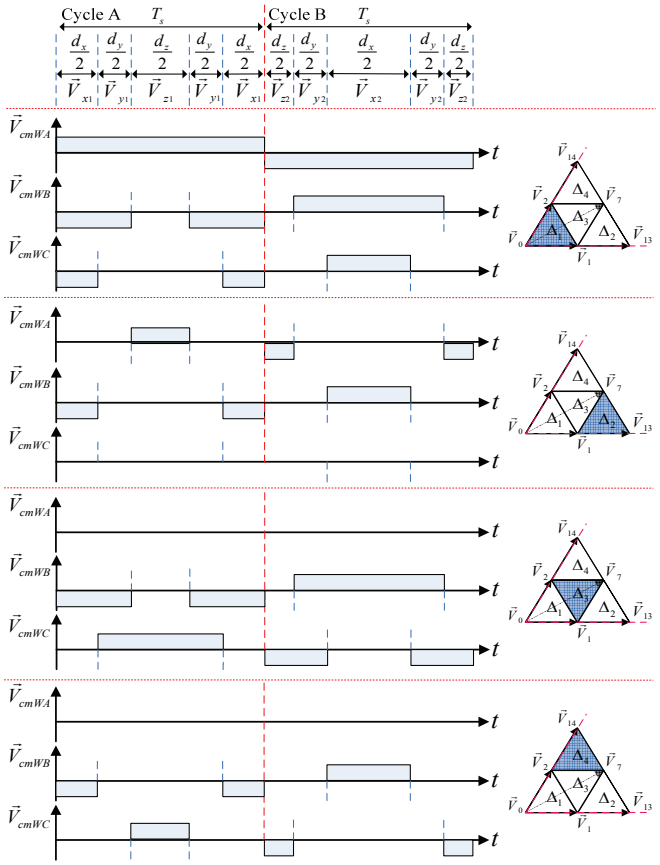
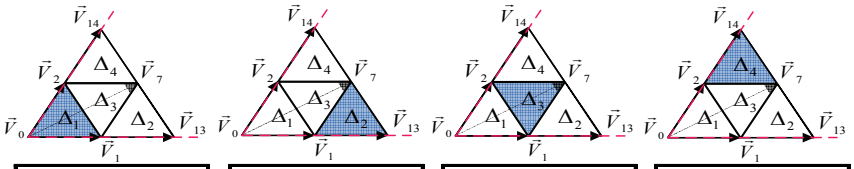


Figure 4-10: Original SVPWM: coupled inductor winding voltage in each leg based on switching states in Figure 4-9, sequence 1, (Common mode voltages are $\pm V_{DC}$)



Sector I-Δ_1	
Cycle A Vectors	
$\vec{V}_{x1}$	[11 00 11]
$\vec{V}_{y1}$	[10 00 11]
$\vec{V}_{z1}$	[00 11 01]
$\vec{V}_{y1}$	[10 00 11]
$\vec{V}_{x1}$	[11 00 11]
Cycle B Vectors	
$\vec{V}_{z2}$	[11 00 01]
$\vec{V}_{y2}$	[10 11 00]
$\vec{V}_{x2}$	[00 11 00]
$\vec{V}_{y2}$	[10 11 00]
$\vec{V}_{z2}$	[11 00 01]

Sector I-Δ_2	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 01 01]
$\vec{V}_{z1}$	[10 11 00]
$\vec{V}_{y1}$	[10 01 01]
$\vec{V}_{x1}$	[10 00 01]
Cycle B Vectors	
$\vec{V}_{z2}$	[10 00 11]
$\vec{V}_{y2}$	[10 01 01]
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 01 01]
$\vec{V}_{z2}$	[10 00 11]

Sector I-Δ_3	
Cycle A Vectors	
$\vec{V}_{x1}$	[11 00 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{z1}$	[10 11 00]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[11 00 01]
Cycle B Vectors	
$\vec{V}_{z2}$	[10 00 11]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{z2}$	[10 00 11]

Sector I-Δ_4	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 10 01]
$\vec{V}_{z1}$	[00 11 01]
$\vec{V}_{y1}$	[10 10 01]
$\vec{V}_{x1}$	[10 00 01]
Cycle B Vectors	
$\vec{V}_{z2}$	[11 00 01]
$\vec{V}_{y2}$	[10 10 01]
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 10 01]
$\vec{V}_{z2}$	[11 00 01]

Figure 4-11: Original SVPWM: switching states in sector I with the elimination of (a), (b), (f), (g), (i) and (j) inductor configurations for zero and small voltage vectors, sequence 2

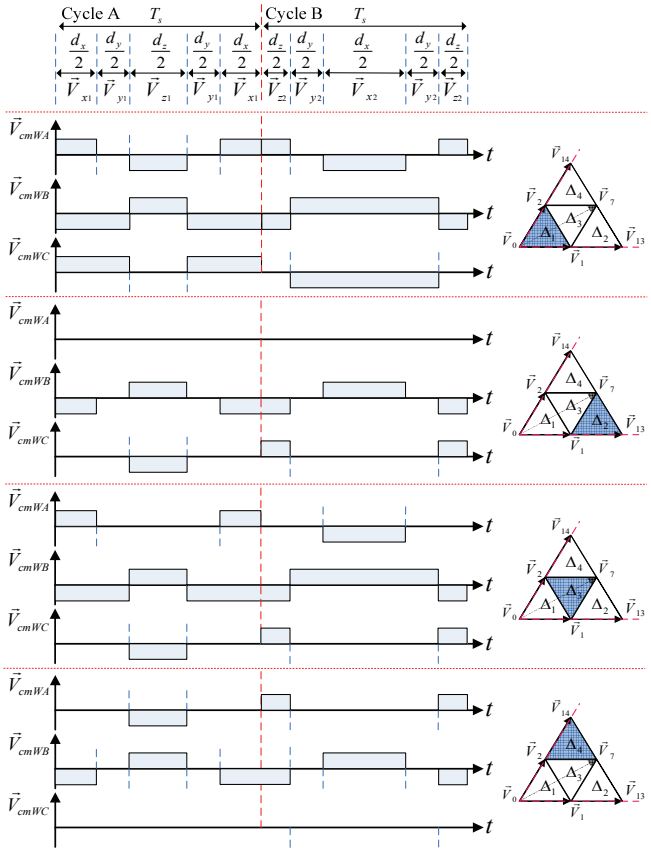


Figure 4-12: Original SVPWM: coupled inductor winding voltage in each leg based on switching states in Figure 4-11, sequence 2, (Common mode voltages are $\pm V_{DC}$)

This result has the advantage of generating a multi-shaped reference waveform that may improve the performance of the drive, especially at a low modulation depth. The effect of alternating the switching sequences from cycles A and B can also be seen in the waveforms in Figure 4-10 and Figure 4-12 and the switching tables in Figure 4-9 and Figure 4-11.

Although the nominal switching period is T_s, many of the devices switch only twice every two switching periods. As a result, the switching losses may be lower than expected from the nominal switching frequency. The winding voltage for each coil in sequence 1 changes over two successive cycles, but in sequence 2, the winding voltage changes over each cycle. As a result, the current ripple in sequence 2 is smaller than the current ripple in sequence 1. However, the average device switching has been increased in sequence 2.

4.5. SVPWM with Optimal Switching Selection (Improved SVPWM)

The SVPWM strategy with the optimal switching selection is presented [115]. This strategy is designed to minimize the winding current ripple by eliminating all the low-inductance switching states. For simplicity, this approach is called Improved SVPWM in this thesis. For this strategy, a new switching sequence as illustrated in Figure 4-13 is designed to minimize common mode current deviations over two successive switching cycles, cycle "A" and "B."

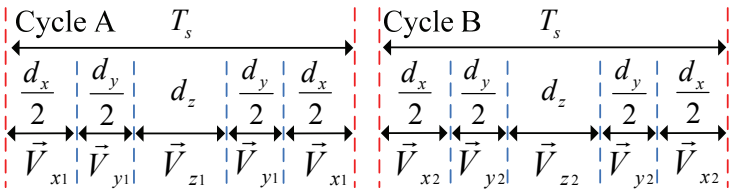


Figure 4-13: Improved SVPWM switching sequence

The switching sequence is formed by using three voltage vectors, V_x, V_y, and V_z. *dx, dy* and *dz* are allocated dwell times for V_x, V_y, and V_z voltage vectors of a given triangle (Figure 4-6), respectively. For both switching cycles, "A" and "B," the space vector voltages are applied in the same order x-y-z-y-x with the same dwell time. The voltage vectors in cycle A and B have either opposite effects (i.e., P-type and N-type) or no effects (i.e., O-type) on the common mode current in each inverter leg. To minimize the

common mode current deviation, the dwell times of a given P-type and N-type switching state in Table 4-2 are equally distributed over each pair of switching cycles. Similar to the original SVPWM, this approach ensures that the common mode winding voltage is balanced over each pair of switching cycle in a given triangle.

4.5.1. Implementation of Improved SVPWM

The original SVPWM scheme eliminates the use of low-inductance configurations of (a), (b), (f), (g), (i) and (j) in Figure 3-15 for small and zero voltage states. In this section, the improved SVPWM scheme eliminates all low-inductance switching states. Thus, the need to use the configurations of Figure 3-15(c) and Figure 3-15(d) in zero voltage states is also eliminated. This result has significant effects on the operation of the CII topology at low modulation indices. As shown in Table 4-7, the optimal switching states in Table 4-5 with minimized effects on the common dc mode current are chosen for the improved SVPWM sequence in Figure 4-13.

Table 4-7: Improved SVPWM switching states

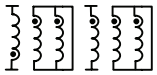
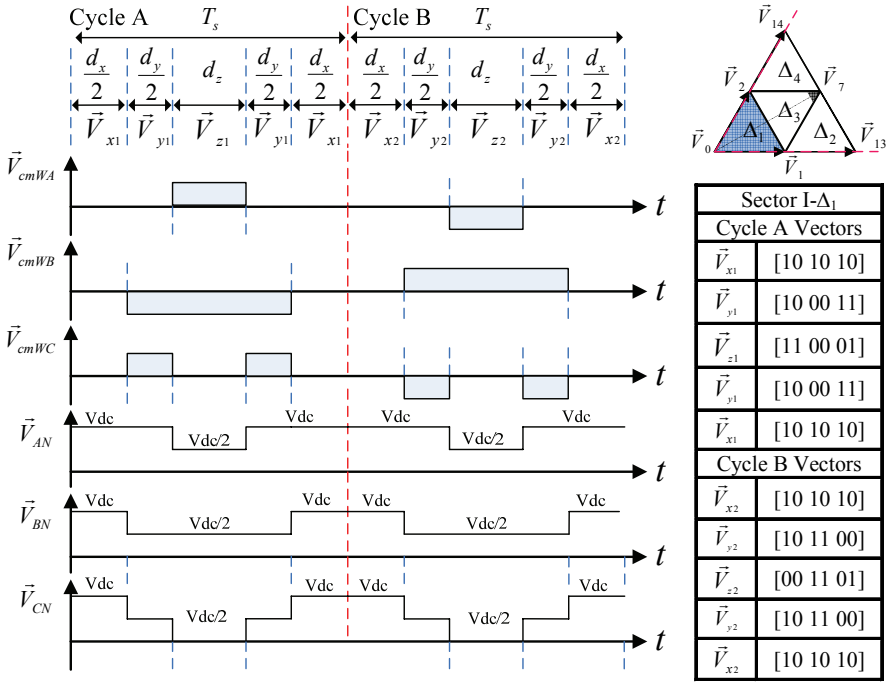
Type of vector	Zero Voltage (V_0)	Small Voltage (V_1 to V_6)	Medium Voltage (V_7 to V_{12})	Large Voltage (V_{13} to V_{18})
Optimal Switching states	 (e)	 (h)	 (j) (i)	 (e)

Figure 4-14 to Figure 4-17 show the proposed 5-segment switching sequence with corresponding winding and phase voltages for each specific switching state in cycles A and B in sector I for Δ_1, Δ_2, Δ_3 and Δ_4. These figures reveal that by properly selecting the switching states, the low-inductance switching states of (a), (b), (c), (d), (f), (g), (i) and (j) in Figure 3-15 for the zero and small voltage vectors are eliminated.

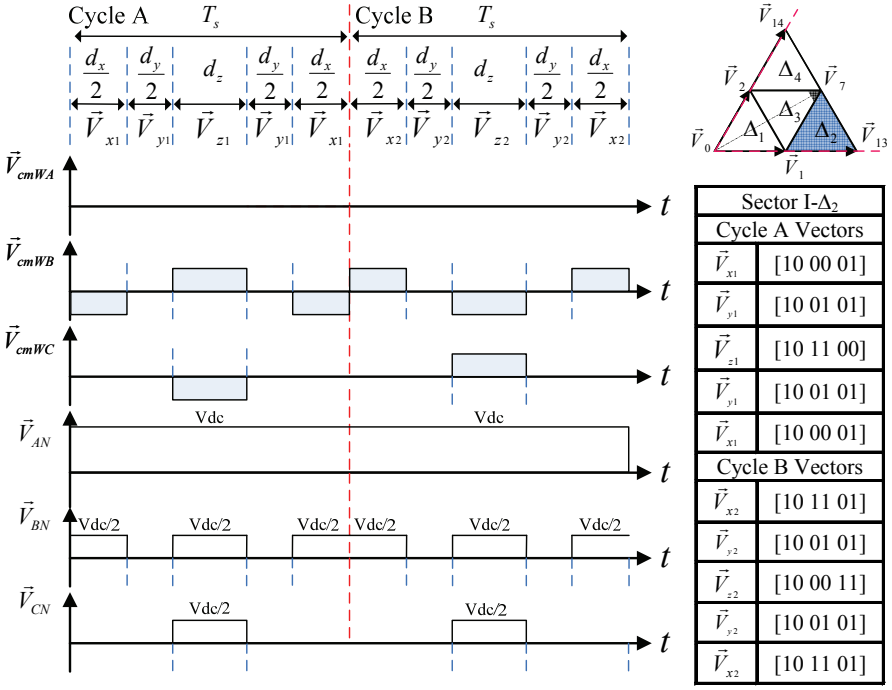
The two cycles of 5-segment switching sequences in Figure 4-14 to Figure 4-17 reveal that the average winding voltage is zero over cycles A and B. For example, in Figure 4-14, consider the case when V_{x1} is {11 00 01} in cycle A, and V_{x2} is {00 11 01} in cycle B: the two switching states generate the same voltage vector in each inverter leg with opposite effects on i_{cm} in phases A and B. The switching sequences in Figure 4-14 to Figure 4-17 indicate that the proposed method is a continuous SVPWM when m_a is lower than 0.5 and becomes discontinuous SVPWM when m_a is higher than 0.5. Continuous SVPWM is observed in triangles Δ_1 and Δ_3 while discontinuous SVPWM for phases A and C is observed in Δ_2 and Δ_4, respectively. This transition from continuous SVPWM at

low-modulation indices to discontinuous SVPWM at high-modulation indices provides the optimal use of each modulation.



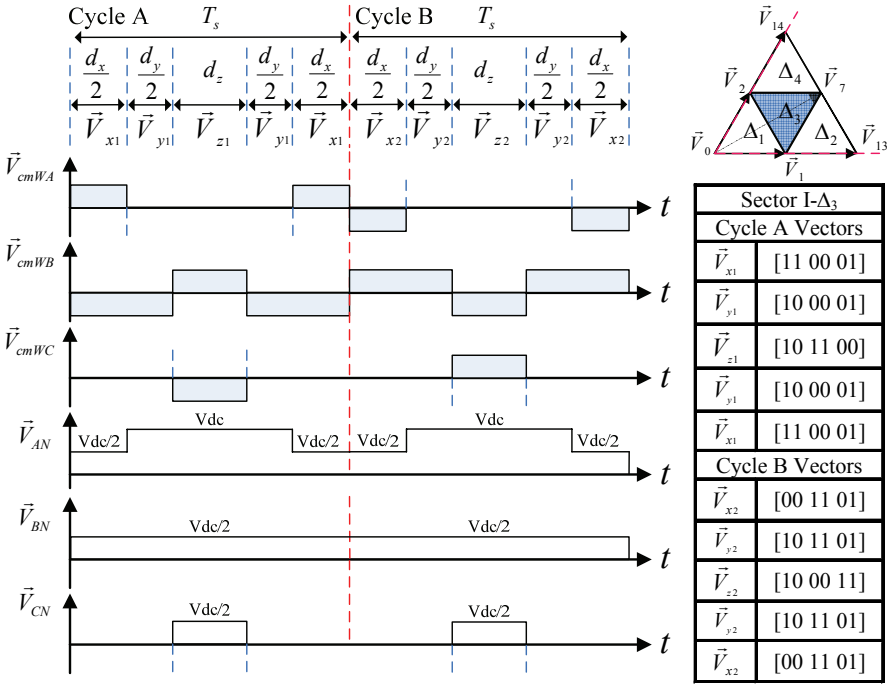
Sector I-Δ_1	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 10 10]
$\vec{V}_{y1}$	[10 00 11]
$\vec{V}_{z1}$	[11 00 01]
$\vec{V}_{y1}$	[10 00 11]
$\vec{V}_{x1}$	[10 10 10]
Cycle B Vectors	
$\vec{V}_{x2}$	[10 10 10]
$\vec{V}_{y2}$	[10 11 00]
$\vec{V}_{z2}$	[00 11 01]
$\vec{V}_{y2}$	[10 11 00]
$\vec{V}_{x2}$	[10 10 10]

Figure 4-14: Improved SVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_1, (Common mode voltages are $\pm V_{DC}$)



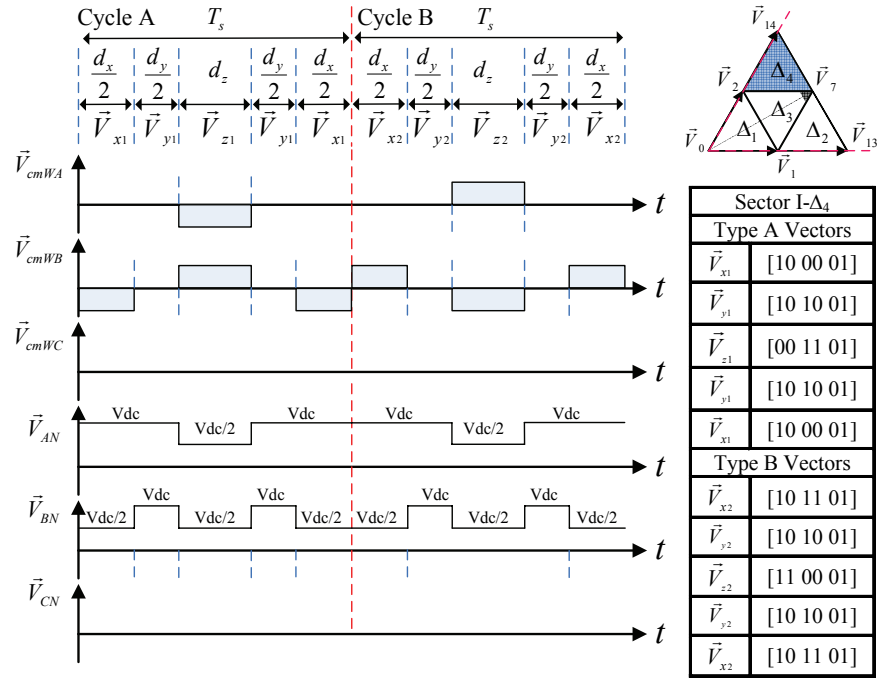
Sector I-Δ_2	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 01 01]
$\vec{V}_{z1}$	[10 11 00]
$\vec{V}_{y1}$	[10 01 01]
$\vec{V}_{x1}$	[10 00 01]
Cycle B Vectors	
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 01 01]
$\vec{V}_{z2}$	[10 00 11]
$\vec{V}_{y2}$	[10 01 01]
$\vec{V}_{x2}$	[10 11 01]

Figure 4-15: Improved SVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_2, (Common mode voltages are $\pm V_{DC}$)



Sector I-Δ_3	
Cycle A Vectors	
$\vec{V}_{x1}$	[11 00 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{z1}$	[10 11 00]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[11 00 01]
Cycle B Vectors	
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{z2}$	[10 00 11]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[00 11 01]

Figure 4-16: Improved SVPWM: coupled inductor upper winding voltage and phase voltage in each leg based on switching states in sector I-Δ_3, (Common mode voltages are $\pm V_{DC}$)



Sector I-Δ_4	
Type A Vectors	
$\vec{V}_{x1}$	[10 00 01]
$\vec{V}_{y1}$	[10 10 01]
$\vec{V}_{z1}$	[00 11 01]
$\vec{V}_{y1}$	[10 10 01]
$\vec{V}_{x1}$	[10 00 01]
Type B Vectors	
$\vec{V}_{x2}$	[10 11 01]
$\vec{V}_{y2}$	[10 10 01]
$\vec{V}_{z2}$	[11 00 01]
$\vec{V}_{y2}$	[10 10 01]
$\vec{V}_{x2}$	[10 11 01]

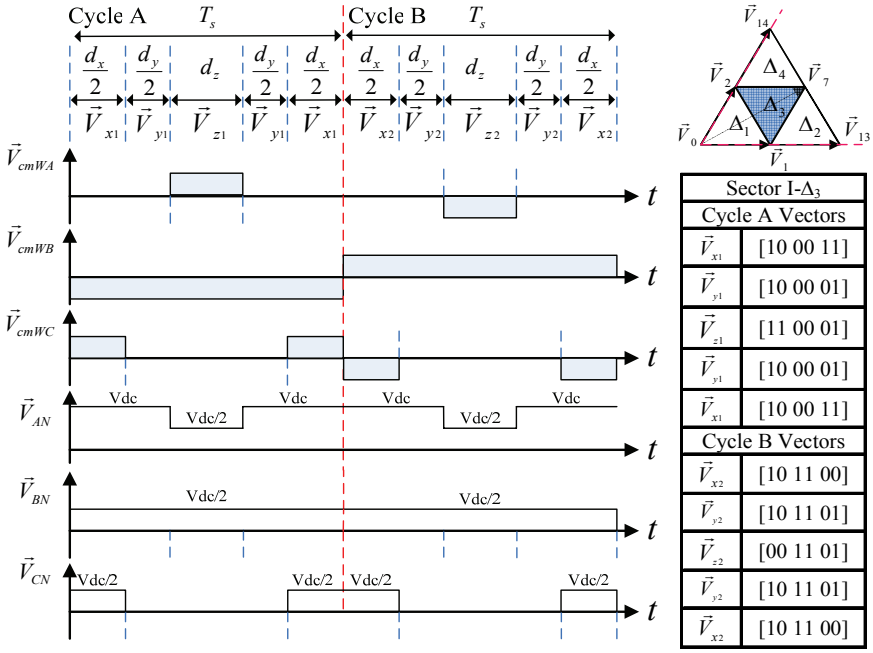
Figure 4-17: Improved SVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_4, (Common mode voltages are $\pm V_{DC}$)

Discontinuous SVPWM reduces the switching losses and improves the performance at the high-modulation indices while continuous SVPWM generates high-quality outputs at

the low-modulation indices. The effect of alternating P-type and N-type switching sequences from cycles A and B can also be seen in the waveforms and switching tables as shown in Figure 4-14 to Figure 4-17. The output terminal voltages in every two successive switching cycles are identical. Thus, the improved SVPWM maintains the output switching frequency at the nominal value.

4.5.2. Impact of Switched Pulse Positions on Winding Current

In addition to effective high inductance states, the sequence of the switching states in each switching cycle (or the order of space voltage vectors) also have significant impact on the common mode current ripple [24]. With the switching pattern shown in Figure 4-14 to Figure 4-17, the order of the P-type and N-type vectors in each cycle is chosen to minimize the current ripple in each phase, but if, for example, the switching state shown in Figure 4-16 is rearranged, the new switching state is obtained as shown in Figure 4-18. When two graphs are compared the winding voltages for phases A and C are swapped; in Figure 4-16, for the same switching frequency, the phase B winding voltage limits the current ramping rate in each cycle by alternating ± V_{dc} across the winding, while in Figure 4-18, the winding voltage cannot limit the current ramping rate by putting only + V_{dc} or -V_{dc} across the winding in one cycle. Thus, the current ripple for phase B in Figure 4-18 is the maximum.



Sector I-Δ_3	
Cycle A Vectors	
$\vec{V}_{x1}$	[10 00 11]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{z1}$	[11 00 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[10 00 11]
Cycle B Vectors	
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{z2}$	[00 11 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[10 11 00]

Figure 4-18: Improved SVPWM: alternate winding and phase voltage in sector I-Δ_3, with poorly chosen switching sequence, (Common mode voltages are either ±V_{dc})

4.6. Interleaved discontinuous SVPWM

This section first describes the concept of the interleaved switching in the multilevel SVPWM strategies. Then a new SVPWM method is designed and developed based on the interleaved switching sequence [22]. The interleaved switching states with a high effective inductance are chosen to minimize the common mode current deviations. Finally the results obtained by these switching states demonstrate the proposed SVPWM is the discontinuous SVPWM.

4.6.1. SVPWM Interleaved Switching

To easily explain and investigate the interleaved switching in SVPWM, the interleaved approach based on two carrier waveforms is adopted here. Figure 4-19 demonstrates the interleaved switching scheme when two triangular carrier waveforms, T_P and T_A, are 180° out of phase compared with m_a, the common modulation waveform value, at the switching cycle of T_s. T_{Ap} and T_{An} are the gating signals for the upper and lower switches, S_1 and S_2, respectively. The switching instances in which both the upper and lower switches overlap each other are interleaved at the beginning, middle, and end of the switching cycle. The interleaved property is obtained because of the unique characteristic of the CII topology where both the upper and lower switches can be either on "P-type" or off "N-type" at the same instant. In Figure 4-19, during the time interval of d_{AP}, both switches are on, and during the time interval of d_{An}, both switches are off. Since the value of the modulation signal is the same for both carrier signals, d_{AP} is equal to d_{An}. The P-type and N-type switching states generate the same output voltage ($V_{dc}/2$). Thus, their position in a switching cycle can be switched. If this change happens, the new interleaved switching scheme can be obtained as shown in Figure 4-20. Both interleaved switching schemes I and II produce the same output voltage. Thus, when designing a switching sequence, these interleaved switching states can be replaced whenever necessary.

The advantage of using the interleaved PWM in the CII topology is the possibility of obtaining the double effective switching frequency at the inverter outputs while balancing the common mode voltage (current) which is a significant issue for the successful operation of the CII topology. Figure 4-19 and Figure 4-20 reveal that while the actual switching frequency is f_c, the effective output voltage switching frequency is twice $2f_c$. Since the gating signals are symmetrical to the midpoint line ($T_s/2$), the output voltage in the first half cycle of the switching cycle is identical to the second half of the switching

cycle. While just one transition occurs in the gating signals from high to low or vice versa, two transitions occur in the output voltage. To obtain the double output frequency, d_{Ap} does not have to be equal to d_{An}. The main reason why these time intervals should be equal is to balance the winding voltage and, as a result, to minimize the common mode dc current deviations. The P-type and N-type switching states when equally distributed over the sampling period as demonstrated in Figure 4-19 and Figure 4-20, can cancel each other's effects on the common mode dc current.

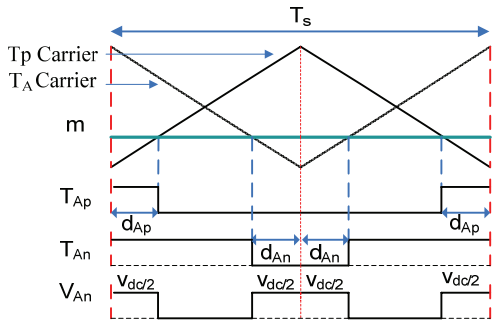


Figure 4-19: Interleaved switching scheme I (Active High)

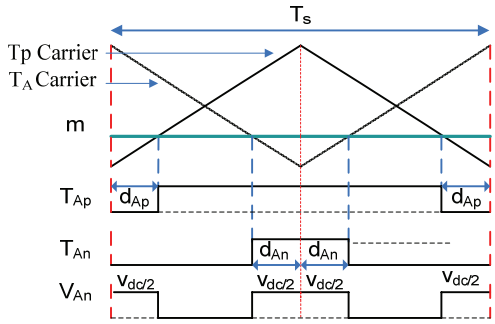


Figure 4-20: Interleaved switching scheme II (Active Low)

The question that arises here is how the interleaved SVPWM differs from the pervious interleaved SPWM and DPWM1 methods discussed in section 4.2.1. As mentioned before, the performance of the CII topology is dependent on the switching states with minimum inductor winding ripple. Since the three-phase switching states can not be freely selected, low-inductance switching states occur frequently when using standard interleaved sinusoidal PWM and DPWM1. However, the interleaved SVPWM cannot only provide the advantages of interleaved switching but also improve the performance of the inverter by eliminating the low effective inductance switching states. As well, these improvements can be achieved while SVPWM overcomes the complexity of the common mode current balancing.

4.6.2. Interleaved Discontinuous SVPWM Switching Sequence

The interleaved switching sequence for the CII topology is illustrated in Figure 4-21. The nine-segment interleaved switching sequence is formed by combining two five-segment sequences where at the intersection (see the dash-dot line in Figure 4-21), the same voltage vector is used. Each 5-segment sequence includes both the P-type and N-type switching states shown in Table 4-4. This combination of two 5-segment sequences allows the common mode current deviation to be minimized by equally distributing the dwell time of a given P-type and N-type switching state over each of the half sampling period. The interleaved sequence balances the common mode winding voltages over one switching cycle whereas the previous SVPWM methods balanced over two switching cycles. This difference has a significant effect on reducing the common mode current and winding current ripples.

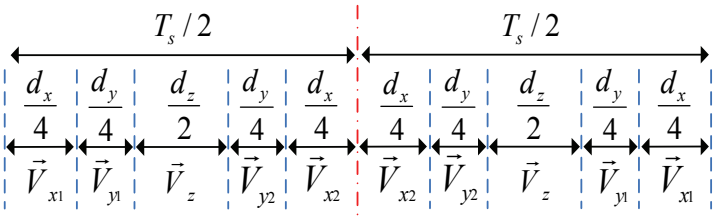


Figure 4-21: Interleaved SVPWM switching sequence

The interleaved switching sequence is formed by using three voltage vectors, V_x, V_y, and V_z. d_x, d_y and d_z are allocated dwell times for the voltage vectors of a given triangle (Figure 4-6) with vertex V_x, V_y and V_z, respectively. In the first half of the switching cycle, the space vector voltages are applied in the order x_1-y_1-z-y_2-x_2, and in the second half, the space vectors' order is x_2-y_2-z-y_1-x_1. The space vectors x_1 and x_2 with the same dwell time of (d_x/4) generate the same voltage vector in each inverter leg but with an opposite impact on the common mode current where applicable, and y_1 and y_2 act similarly. The space vector z is always produced by configuration (e) in Figure 3-15 and does not affect the common mode current. As shown in Table 4-5, the switching state (e) can produce a zero voltage vector or a large voltage vector. Switching state (e) is used in the interleaved sequence to produce a zero voltage vector when the modulation depth is lower than 0.5, and to generate a large voltage vector when the modulation depth is larger than 0.5. This approach ensures that the common mode winding voltage is balanced over each switching cycle.

Generally, to minimize harmonic distortion in the output voltage, the reference vector is approximated by the time averaging of the nearest three vectors, V_x, V_y, and V_z. The 'three nearest' vectors and their dwell times can be determined by finding the triangle where the reference vector lies in the hexagon [5, 24]. With the interleaved sequence, V_{ref} can be synthesized by the three nearest voltage vectors when its tip is located in triangles Δ_1, Δ_2 and Δ_4. However, when the tip of V_{ref} is located in triangle Δ_3 the number of switching instances per cycle increases if V_{ref} is synthesized by the nearest three voltage vectors in triangle Δ_3. As a result, the output switching frequency at twice the switching frequency cannot be possible; this condition is not desirable. With the possible switching states, in order to maintain the effective output switching frequency at twice the switching frequency, the proposed SVPWM method approximates V_{ref} by the two nearest voltage vectors in triangle Δ_3 and one large voltage vector in triangles Δ_2 or Δ_4. For example, in Figure 4-6, when the tip of V_{ref} is located in triangle Δ_3 to maintain the double frequency characteristic of the interleaved switching, the V_{ref} can be approximated with the two nearest voltage vectors from V_1, V_2 and V_7, and a large voltage vector of V_{13} or V_{14} or the combination of both these vectors. To explain this approach in more detail, the CII space voltage block diagram in Figure 4-6 is depicted in Figure 4-22 where V_{13} is used as a large voltage vector. Conventionally V_{ref} can be approximated with V_1, V_2 and V_7. However, in the new method as shown in Figure 4-23, triangle Δ_3 is divided into two new triangles of vertices V_1, V_2, V_{13} (see Figure 4-23(a)) and V_2, V_7, V_{13} (see Figure 4-23(b)); V_{ref} can be approximated with this new set of voltage vectors.

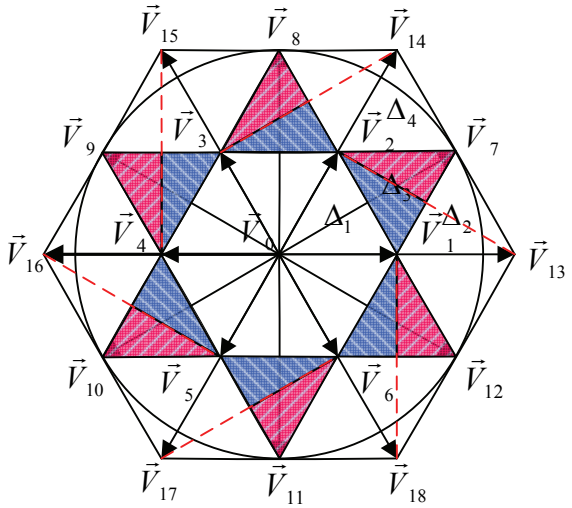


Figure 4-22: CII space vector diagram using a large voltage vector in Δ_2

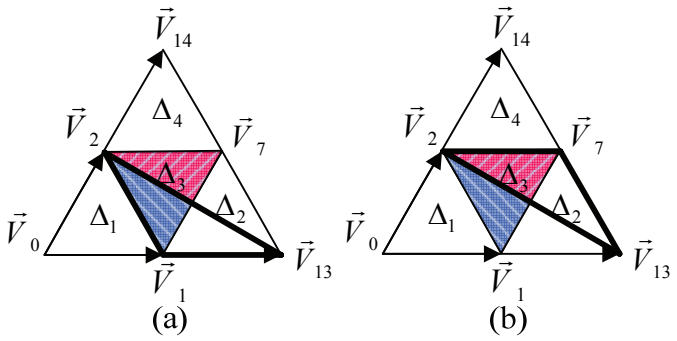


Figure 4-23: CII space vector diagram in Sector I using V_{13} in Δ_2 (a) triangle of vertices V_1, V_2 and V_{13} (b) triangle of vertices V_2, V_7, V_{13}

To find the new dwell times for the new set of voltage vectors, the eliminated voltage vector in equation (4-8) is approximated with new voltage vectors. When V_{ref} is approximated with V_1, V_2 and V_7, we have

$$\vec{V}_{ref} = (d_1\vec{V}_1 + d_2\vec{V}_2 + d_7\vec{V}_7)/T_s \tag{4-10}$$

$$T_s = d_1 + d_2 + d_3 \tag{4-11}$$

where d_1, d_2 and d_3 are allocated dwell times for the voltage vectors V_1, V_2 and V_7, respectively. Now, when V_{ref} is approximated with V_2, V_7 and V_{13}, V_1 can be calculated by

$$\vec{V}_1 = \vec{V}_2 + \vec{V}_{13} - \vec{V}_7 . \tag{4-12}$$

Substituting equation (4-12) into (4-10) we get

$$\vec{V}_{ref} = ((d_1 + d_2)\vec{V}_2 + (d_3 - d_2)\vec{V}_7 + d_2\vec{V}_{13})/T_s , \tag{4-13}$$

but when V_{ref} is approximated with V_1, V_2 and V_{13}, V_7 can be calculated by

$$\vec{V}_7 = \vec{V}_2 + \vec{V}_{13} - \vec{V}_1 . \tag{4-14}$$

Substituting equation (4-14) into (4-10) we obtain

$$\vec{V}_{ref} = ((d_1 + d_3)\vec{V}_2 + (d_2 - d_3)\vec{V}_1 + d_3\vec{V}_{13})/T_s . \tag{4-15}$$

Similarly, V_{ref} can be approximated with V_1, V_2 and V_{14} or V_1, V_7 and V_{14}. However, here the triangle Δ_3 is divided into two new triangles of vertices V_1, V_2, V_{14} and V_1, V_7, V_{14} as shown in Figure 4-24. If the combination of V_{13} and V_{14} is possible the new space vector diagram can be illustrated as in Figure 4-25. These three methods are compared in more detail in chapter 5.

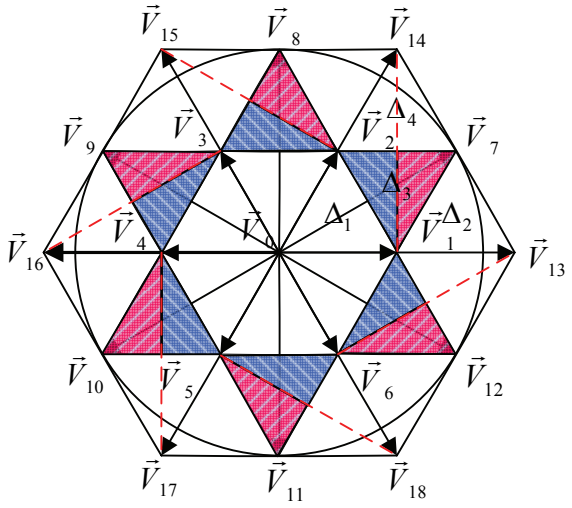


Figure 4-24: CII space vector diagram using a large voltage vector in Δ_4

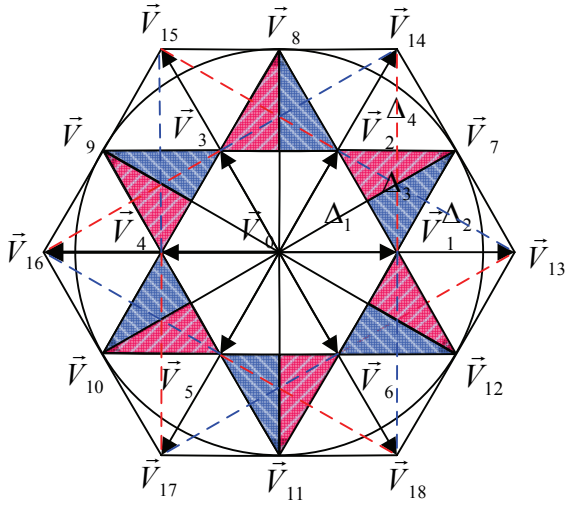
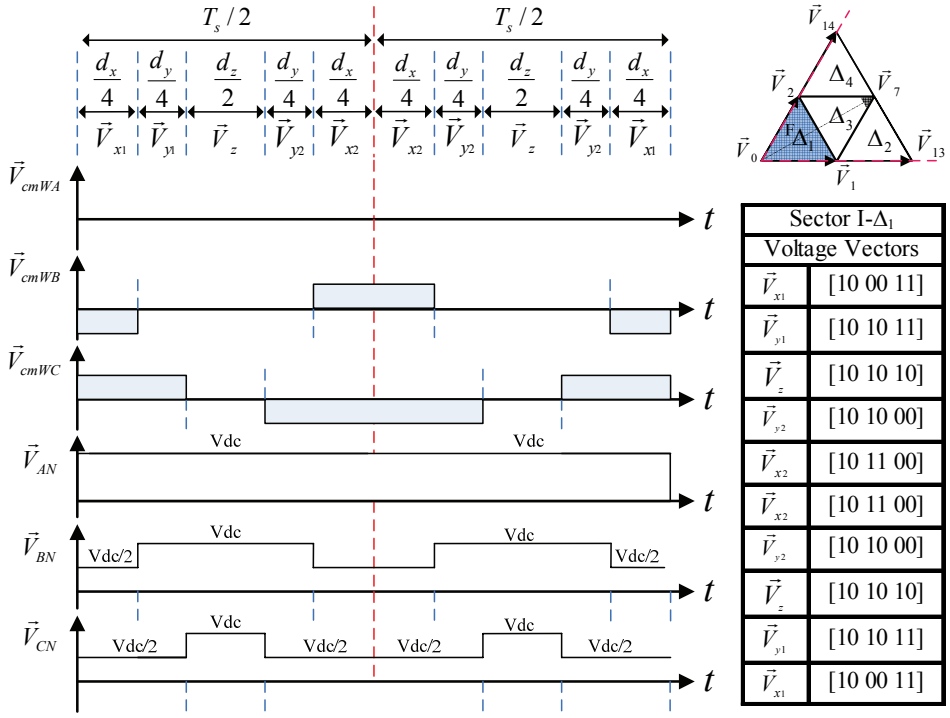


Figure 4-25: CII space vector diagram using combined voltage vectors in Δ_2 and Δ_4

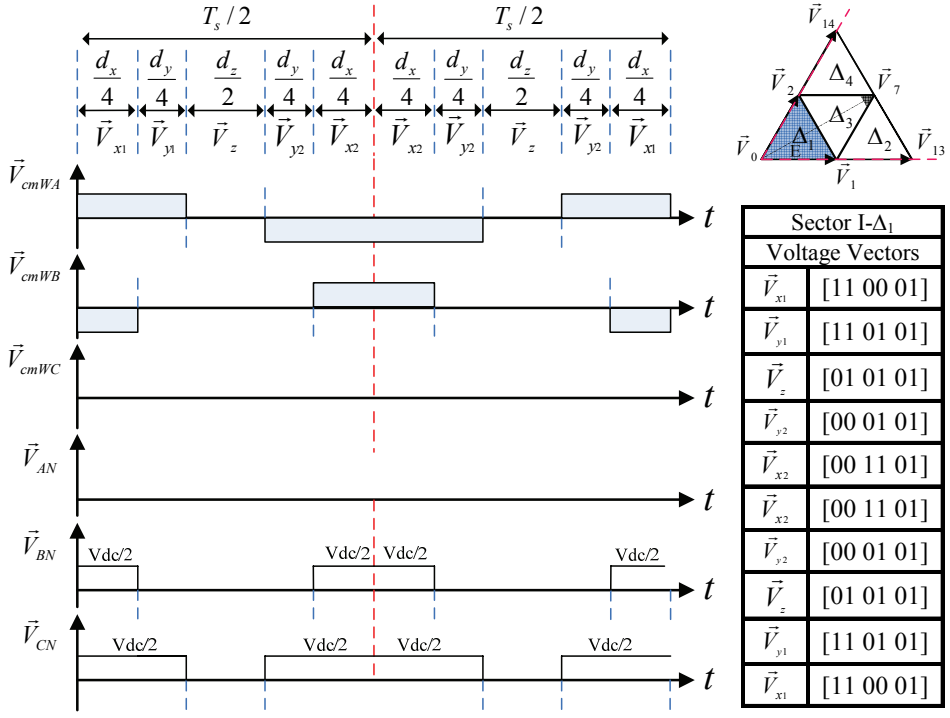
4.6.3. Implementation of Interleaved DSVPWM

Figure 4-26 to Figure 4-33 show the proposed 9-segment interleaved switching sequence with corresponding winding and phase voltages in sector I for Δ_1, Δ_2, Δ_3 and Δ_4. By properly selecting the switching states, in interleaved SVPWM, the low-inductance switching states of (a), (b), (c) and (d) in Figure 3-15 for a zero voltage vector and the switching states of Figure 3-15(f) and Figure 3-15(g) for small voltage vectors are eliminated in all the triangles Δ_1, Δ_2, Δ_3 and Δ_4. In addition, in triangles Δ_2 and Δ_4, the switching states of Figure 3-15 (i) and Figure 3-15 (j) are also avoided for small voltage vectors. However, the elimination of these configurations in triangles Δ_1 and Δ_3 is unavoidable.



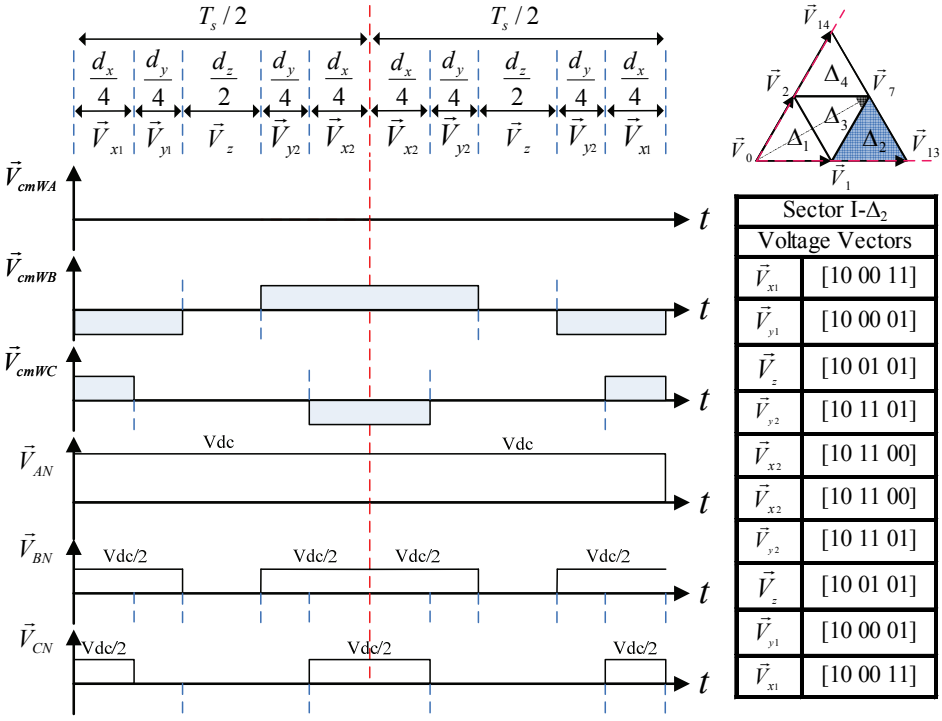
Sector I-Δ_1	
Voltage Vectors	
$\vec{V}_{x1}$	[10 00 11]
$\vec{V}_{y1}$	[10 10 11]
$\vec{V}_z$	[10 10 10]
$\vec{V}_{y2}$	[10 10 00]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{y2}$	[10 10 00]
$\vec{V}_z$	[10 10 10]
$\vec{V}_{y1}$	[10 10 11]
$\vec{V}_{x1}$	[10 00 11]

Figure 4-26: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_{1F}, (Common mode voltages are either $\pm V_{dc}$)



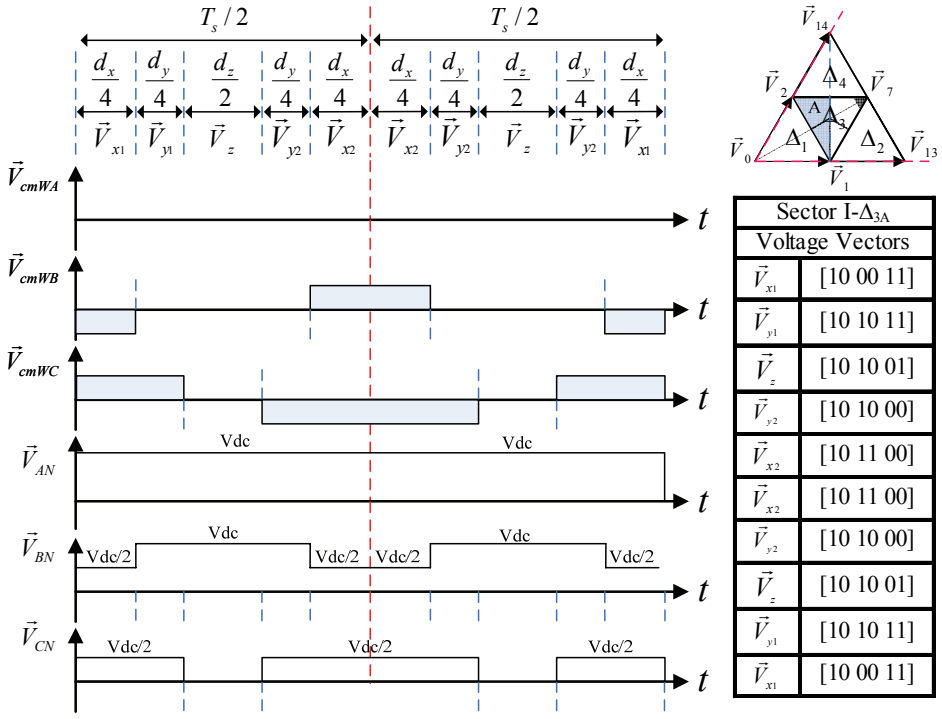
Sector I-Δ_1	
Voltage Vectors	
$\vec{V}_{x1}$	[11 00 01]
$\vec{V}_{y1}$	[11 01 01]
$\vec{V}_z$	[01 01 01]
$\vec{V}_{y2}$	[00 01 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{y2}$	[00 01 01]
$\vec{V}_z$	[01 01 01]
$\vec{V}_{y1}$	[11 01 01]
$\vec{V}_{x1}$	[11 00 01]

Figure 4-27: DSVPWM: alternative coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_{1E}, (Common mode voltages are either $\pm V_{dc}$)



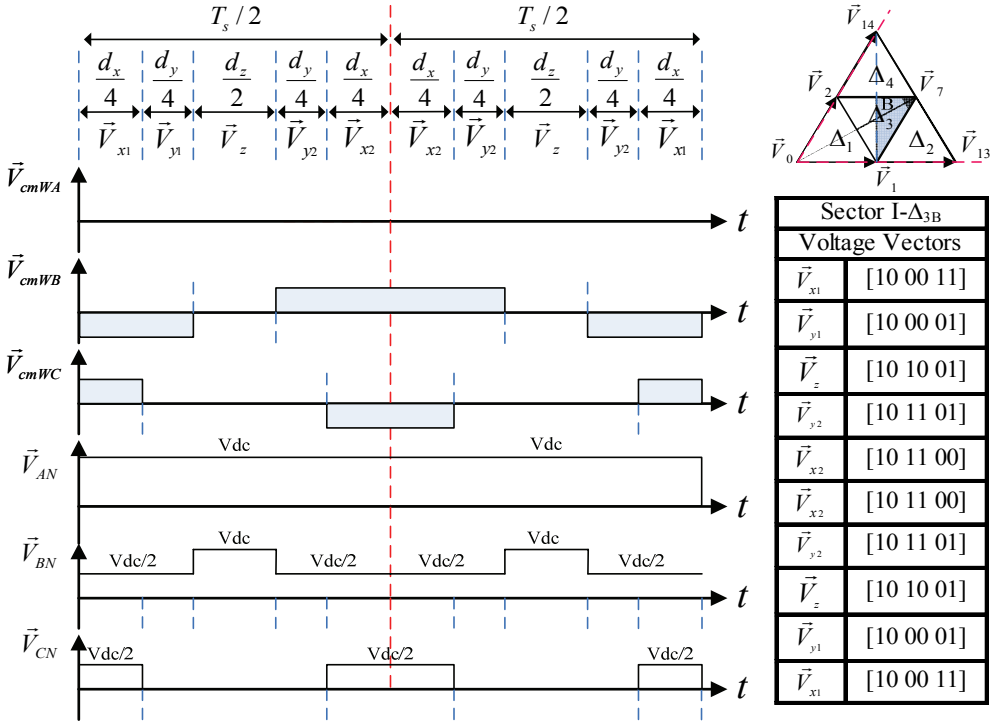
Sector I-Δ_2	
Voltage Vectors	
$\vec{V}_{x1}$	[10 00 11]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_z$	[10 01 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_z$	[10 01 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[10 00 11]

Figure 4-28: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_2, (Common mode voltages are either $\pm V_{dc}$)



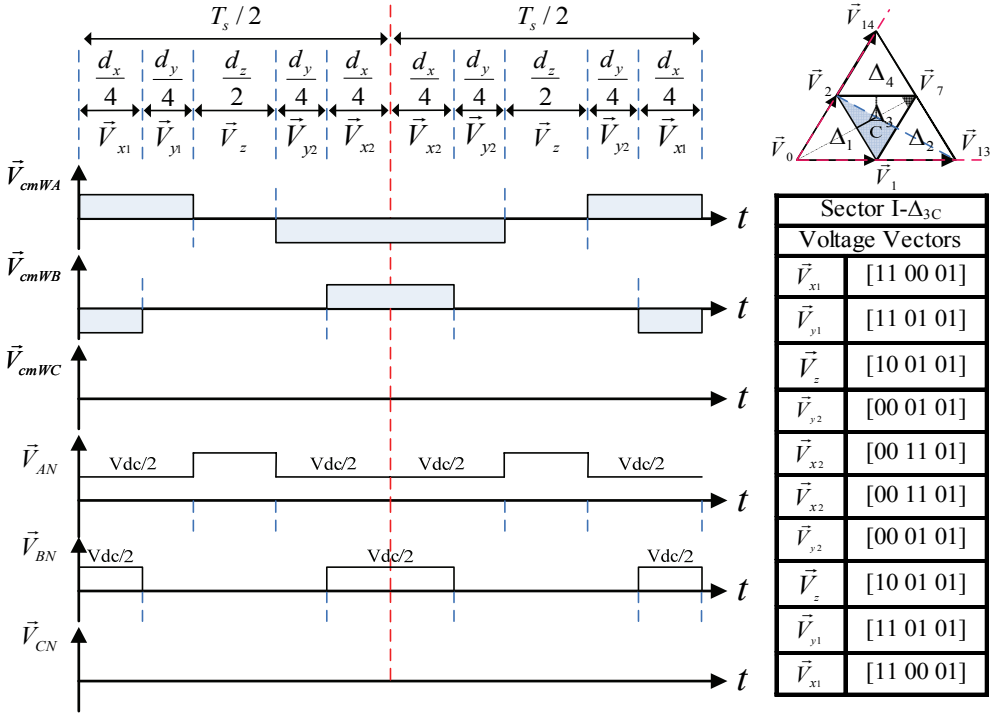
Sector I-Δ_{3A}	
Voltage Vectors	
$\vec{V}_{x1}$	[10 00 11]
$\vec{V}_{y1}$	[10 10 11]
$\vec{V}_z$	[10 10 01]
$\vec{V}_{y2}$	[10 10 00]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{y2}$	[10 10 00]
$\vec{V}_z$	[10 10 01]
$\vec{V}_{y1}$	[10 10 11]
$\vec{V}_{x1}$	[10 00 11]

Figure 4-29: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_{3A}, (Common mode voltages are either $\pm V_{dc}$)



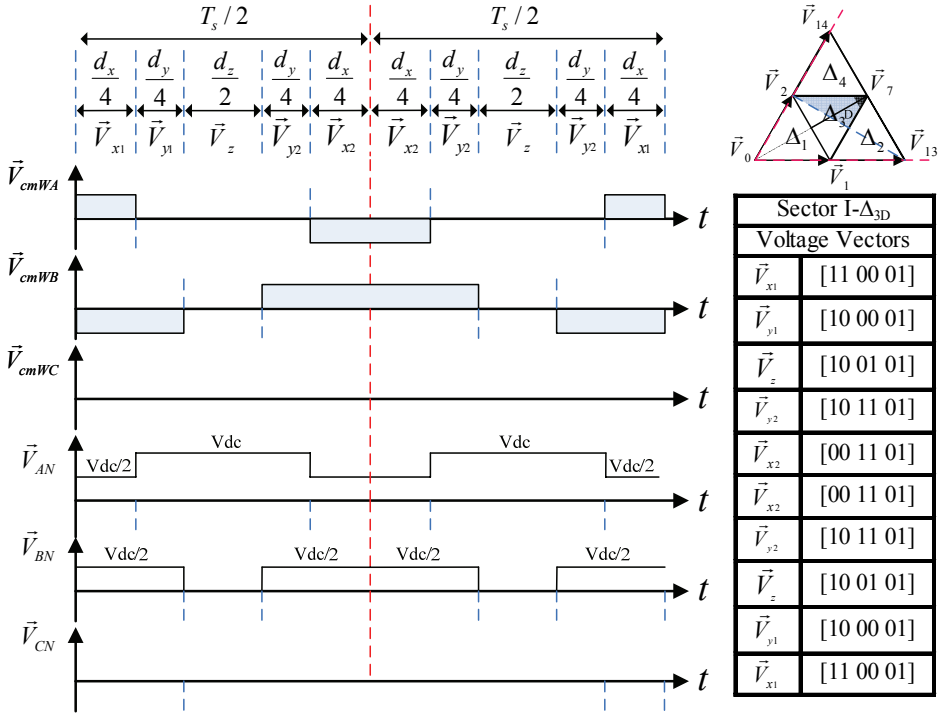
Sector I-Δ_{3B}	
Voltage Vectors	
$\vec{V}_{x1}$	[10 00 11]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_z$	[10 10 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{x2}$	[10 11 00]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_z$	[10 10 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[10 00 11]

Figure 4-30: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_{3B}, (Common mode voltages are either $\pm V_{dc}$)



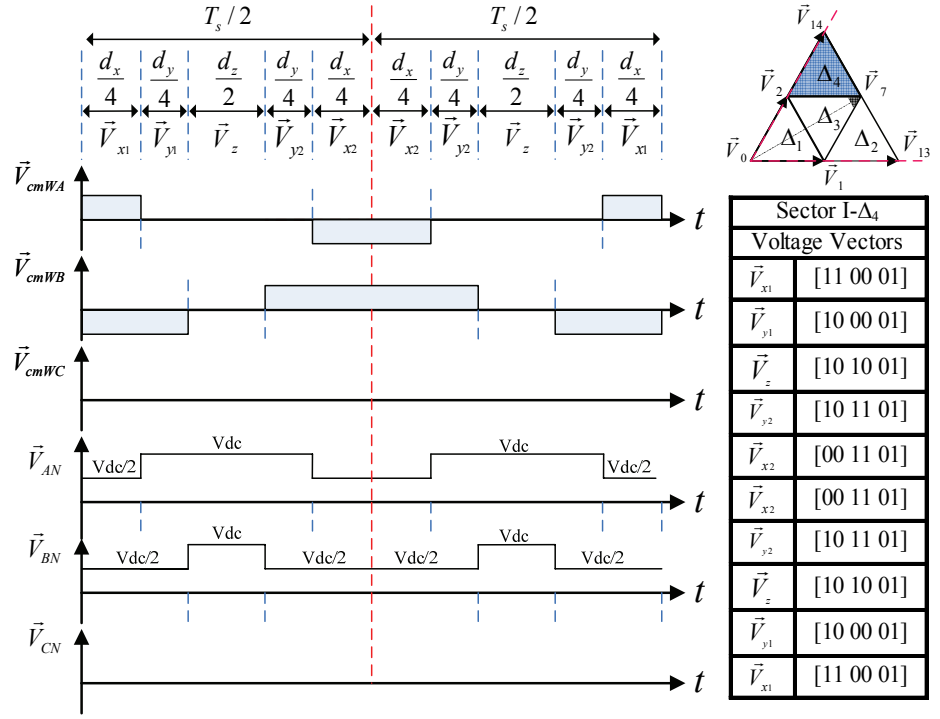
Sector I-Δ_{3C}	
Voltage Vectors	
$\vec{V}_{x1}$	[11 00 01]
$\vec{V}_{y1}$	[11 01 01]
$\vec{V}_z$	[10 01 01]
$\vec{V}_{y2}$	[00 01 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{y2}$	[00 01 01]
$\vec{V}_z$	[10 01 01]
$\vec{V}_{y1}$	[11 01 01]
$\vec{V}_{x1}$	[11 00 01]

Figure 4-31: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_{3C}, (Common mode voltages are either $\pm V_{dc}$)



Sector I-Δ_{3D}	
Voltage Vectors	
$\vec{V}_{x1}$	[11 00 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_z$	[10 01 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_z$	[10 01 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[11 00 01]

Figure 4-32: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_{3D}, (Common mode voltages are either $\pm V_{dc}$)



Sector I-Δ_4	
Voltage Vectors	
$\vec{V}_{x1}$	[11 00 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_z$	[10 10 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{x2}$	[00 11 01]
$\vec{V}_{y2}$	[10 11 01]
$\vec{V}_z$	[10 10 01]
$\vec{V}_{y1}$	[10 00 01]
$\vec{V}_{x1}$	[11 00 01]

Figure 4-33: DSVPWM: coupled inductor winding voltage and phase voltage in each leg based on switching states in sector I-Δ_4, (Common mode voltages are either $\pm V_{dc}$)

The switching sequences in Figure 4-26 to Figure 4-33 indicate the proposed method is discontinuous SVPWM over all modulation indices. In sector I, in triangles Δ_{1F} , Δ_2, Δ_{3A} and Δ_{3B}, discontinuous SVPWM is observed in phase A while in Δ_{1E} , Δ_{3C}, Δ_{3D} and Δ_4, discontinuous SVPWM is observed in phase C. Two inverter legs always have the PWM switching, and the third leg is clamped to the P or N points of the dc rail. The specific areas in triangles Δ_3 and Δ_1 are labeled by A, B, C, D, E and F. When m_a is lower than 0.5, switching patterns Δ_{1E} and Δ_{1F} provide various types of discontinuous SVPWMs such as DPWM0, DPWM1 and DPWM3 to be applicable for CII topology. Δ_{3A}, Δ_{3B}, Δ_{3C} and Δ_{3D} switching patterns are provided for when in triangle Δ_3, V_{ref} is approximated with the combination of the large vectors in triangles Δ_2 and Δ_4.

To understand how the effective double output frequency is achieved by using interleaved sequence, consider, for example, the winding and phase voltages for the switching states in triangle Δ_4 over one switching cycle in Figure 4-33. Since the output voltage level in phase A and B changes four times during the switching cycle, the switching frequency of the output voltage is double the actual switching frequency. Figure 4-33 also demonstrates that the average winding voltage is balanced over each half cycle, resulting in no net change in the common mode current.

4.6.4. Impact of Switched Pulse Positions on Output Current

Like the winding current ripple as mentioned in section 4.5.2 , the output current ripple also depends on the location of the pulses in each half switching cycle. The sequence of the voltage vectors (or the position of the pulses) within the half switching cycle affects the harmonic performance of the inverter output waveforms as well. Since the load harmonic losses are proportional to the rms value of the ripple current, minimizing the current ripple produces lower losses in the load. For example, consider V_{AN} in Figure 4-33 when the duty cycle is 50% for producing V_{dc} and $V_{dc}/2$; the load losses in the two extreme positions can differ by up to a factor of 4 [24, 121]. The interleaved DSVPWM schemes with placing their terminal voltage pulses closer to the center of each switching cycle have a superior harmonic performance compared to those schemes which do not center the voltage pulses. Overall, when one designs a SVPWM strategy, a pulse sequence is the important factor to reduce the winding and current ripple, and needs to be considered carefully.

4.7. Chapter Summary

In this chapter, interleaved SPWM and DPWM1 carrier-based PWM schemes and multilevel SVPWM schemes are developed for the CII topology. With interleaved carrier-based PWM schemes, the switching states in each switching cycle are chosen by the reference waveform. The uncontrolled switching states in the carrier-based PWM methods include low-effective inductance connections and will produce a large high-frequency current ripple in the inductor windings (as shown in chapter 5). However, SVPWM schemes are capable of eliminating the low-inductance switching states.

The main advantages of interleaved carrier-based PWM methods are that they inherently balance the common mode voltage (current) and provide the output PWM waveforms with the effective double switching frequency. In addition to providing lower switching losses than those from continuous SPWM, discontinuous PWM (DPWM1) generates multilevel output voltages and allows the effects of coupling between inverter legs on the common mode current ripple to be reduced by clamping one of the inverter legs to P or N points of the DC bus.

The multilevel SVPWM methods are developed from a very simple algorithm and improved successively. The main significance of using SVPWM is that the switching states generating a high current ripple can be eliminated. The SVPWM switching sequences were designed to balance the common mode voltage. With a 5-segment sequence the common mode voltage (current) is balanced over two switching cycles whereas with an interleaved 9-segment sequence, the common mode current is balanced over one switching cycle. In addition to the selection of switching states, the order of the switching states (or voltage vectors) in a sequence significantly impacts on common mode current.

Based on the multilevel SVPWM algorithm for the CII topology, original SVPWM, improved SVPWM and interleaved DSVPWM are developed. Compare to original SVPWM, the improved SVPWM eliminates all low-inductance switching states. The improved SVPWM is also shown that the winding current ripple is dependent to not only the selection of switching states with a high effective inductance but also the switching sequence (or the order of space voltage vectors in a switching period). In interleaved DSVPWM, most switching states with a low inductance are omitted. The effective output switching frequency is increased by interleaved DSVPWM in comparison to the original and improved SVPWMs. In addition, the interleaved DSVPWM scheme has the ability to

reduce the switching losses in the inverter, allowing for higher switching frequencies.

While multilevel SVPWM schemes increase the complexity compared to carrier-based PWM schemes, the design flexibility of selecting switching states and sequences with SVPWM schemes can improve the performance of the inverter and provide the optimal operation for this topology.

Chapter 5

Coupled Inductor Inverter Performance Comparison Using Experimental and Simulation Results

The CII drive performance with the SPWM, DPWM1 and SVPWM modulation strategies are investigated by using simulation results and experimental tests with a RL load. The operation of the CII topology with different modulation methods is examined and the resultant performances are compared. A modulation scheme which produces lower losses in the coupled inductor and provides the high-quality output waveforms is identified. In addition, the inverter operation as a variable frequency drive is validated through experimental tests using a PMSM machine. These observations allow a comprehensive analysis of whether the CII topology is a suitable choice for a high-performance drive system as its basic features suggest.

5.1. Review of PWM Schemes Examined

First, the operation of the CII topology with interleaved carrier-based PWM modulations (SPWM and DPWM1) is investigated. The superiority of DPWM1 over SPWM is validated by comparing the current ripple waveforms at various modulation indices, and voltage and current THD graphs. Then DPWM1 is chosen as a reference modulation scheme to be compared with the newly developed multilevel SVPWM based schemes. The three main multilevel SVPWM strategies explained in Chapter 4 are investigated: (1) the original SVPWM, (2) the improved SVPWM, and (3) the interleaved discontinuous SVPWM (DSVPWM). These methods show the incremental improvement in inverter performance including the magnitude of the winding current ripple and the quality of output waveforms. The later refers to the low-harmonic content waveforms with the ability to transfer the first harmonic PWM to a higher switching frequency by increasing the effective switching frequency.

The original SVPWM shows the effectiveness of the multilevel SVPWM strategy in eliminating the switching states which produce the high winding current ripple. The original SVPWM results are compared with those from DPWM1, demonstrating the

possibility of reducing the coupled inductor losses by lowering the winding current ripple. The improved SVPWM demonstrates the operation of the CII circuit with selection of all high-effective inductance switching states. The lower winding current ripple significantly improves the performance, especially at low-modulation depths, but the quality of output current waveforms is still less than that of DPWM1.

By lowering inverter losses, the interleaved DSVPWM is presented as the most efficient method. The DSVPWM strategy is used to perform DSVPWM0, DSVPWM1 and DSVPWM3 modulation schemes with SVPWM. These modulations are compared at low-modulation indices. The DSVPWM1 shows a better performance for a unity-power-factor load by additionally lowering the winding current ripple and switching losses when a 60 discontinuous period occurs at the positive and negative voltage peaks. The DSVPWM1 harmonic spectra of the voltage and current are compared to those of DPWM1. The superiority of DSVPWM is explored by using the experimental loss measurements.

The DSVPWM modulation scheme is introduced as a modulation scheme that can be used for drives applications. The closed loop performance of the CII topology with DSVPWM is accomplished with a series of experimental tests using a PMSM. The closed loop speed and power control are implemented with this drive topology. The results explore the effectiveness of the CII structure and validate the fast-response operation of the coupled inductor inverter using the DSVPWM control.

5.2. Experimental Set-up

In order to validate the proposed approach, the investigated PWM modulation algorithms are implemented using a TI TMS320F2812 DSP, and experimental tests were carried out using the small-power converter system illustrated in Figure 5-1, with the following parameters: V_{DC} = 300 V, I_{pk} = 10 A, f_c =15kHz switching frequency, the split-wound coupled inductor magnetizing inductance (L_t) = 4.7 mH.

An LC filter is used at the output of the inverter before where the load is connected. The values of the delta-connected filter capacitors are 5 uF, and those of the Y-connected filter inductances are 1 mH. The maximum load current is obtained when the load resistance was 15.625Ω. Most of the computation for multilevel SVPWM strategies is done offline and tabulated as PWM-switching look-up tables, so that on-line computation is minimized. Compared to the SPWM and DPWM1 algorithms, the SVPWM algorithms

are more computationally complex but also more flexible for selecting the switching states and sequences.

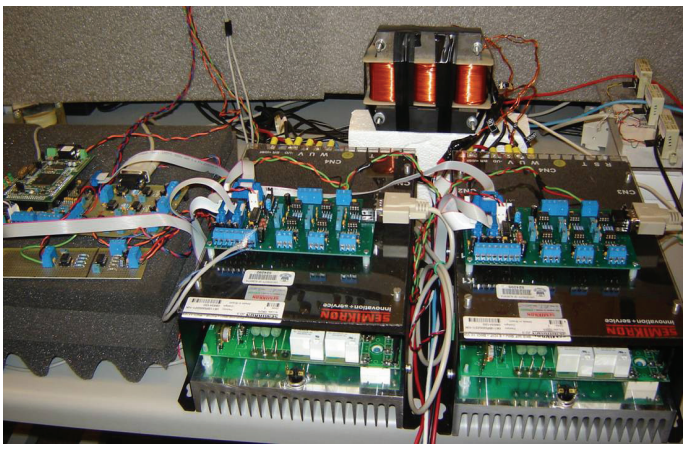


Figure 5-1: Experimental set-up of the CII inverter with combined three limb core, interface boards and a TI DSP controller

5.3. Simulations Set-up

The operation of the CII topology with the SPWM, DPWM1 and SVPWM strategies is simulated in Simulink as shown Figure 5-2. The tests are carried for a range of modulation indices, m_a, by using an inverter with 300V DC link voltage and 15 kHz switching frequency, driving a 15 Ω;1 mH 3-phase load with the fundamental frequency of 60Hz.

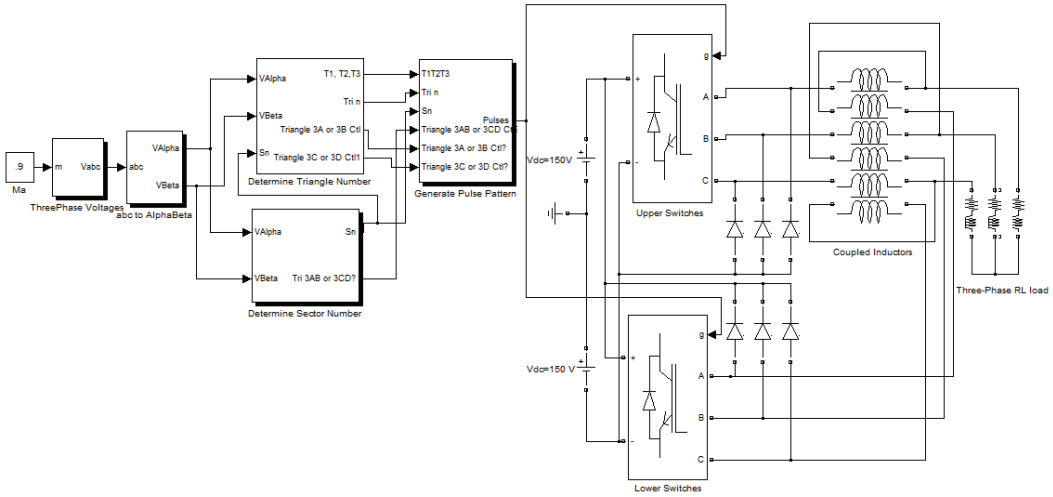


Figure 5-2: Simulation block diagram of the CII topology

To achieve a Simulink model, three split-wound inductors are considered with a total of six windings that need coupling for the interaction of the three phases in the three-limb

core. In total, fifteen coupling coefficients are defined. The coupled inductor upper and lower winding inductances are 1.5 mH each, and the coupling factor is -0.45 between phases and 0.99 in each phase winding.

5.4. CII Performance with Interleaved SPWM and DPWM1

Comprehensive simulation results are demonstrated for the SPWM and DPWM1 modulation schemes. The characteristics of each modulation method are explored. The advantages and disadvantages of each method are investigated. Finally, the experimental results are used to validate the simulation results.

5.4.1. Interleaved SPWM and DPWM1 Simulation Results

Interleaved SPWM and DPWM1 carrier-based modulations are applied to this topology in [2, 114]. The upper and lower winding currents and output current in phase A for the interleaved SPWM and DPWM1 methods described in section 4.2 are illustrated in Figure 5-3 through Figure 5-6. The plots indicate the performance at m_a values of 0.9 and 0.4 and validate that both algorithms work at various modulation depths.

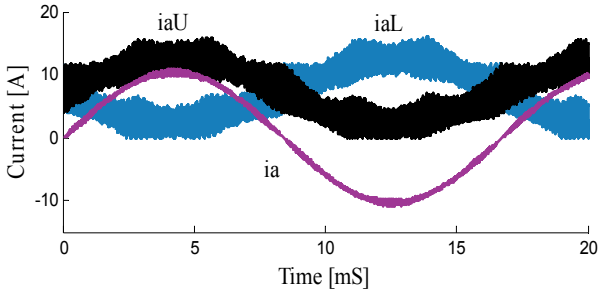


Figure 5-3: Simulated SPWM: upper and lower winding currents and output current in phase A (m_a =0.9, f_c= 15 kHz)

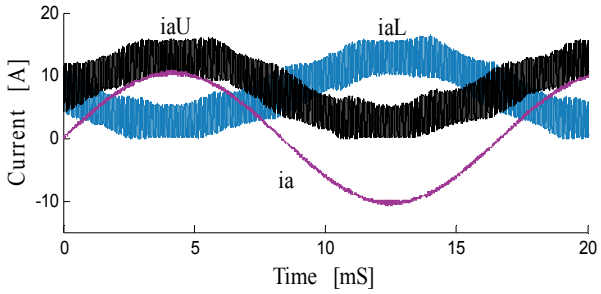


Figure 5-4: Simulated DPWM1: upper and lower winding currents and output current in phase A (m_a =0.9, f_c= 15 kHz)

Figure 5-3 and Figure 5-5 show these currents for SPWM, which includes the lowest effective inductance states of (a) and (b) in Figure 3-15 that are avoided in DPWM1,

shown in Figure 5-4 and Figure 5-6. Since these states occur at $m_a < 0.5$ for generating zero voltage vectors, the DPWM1 current ripple is reduced by a factor of approximately two at $m_a = 0.4$ when compared to the SPWM current ripple. However, the current ripple for $m_a > 0.5$ is similar for both methods.

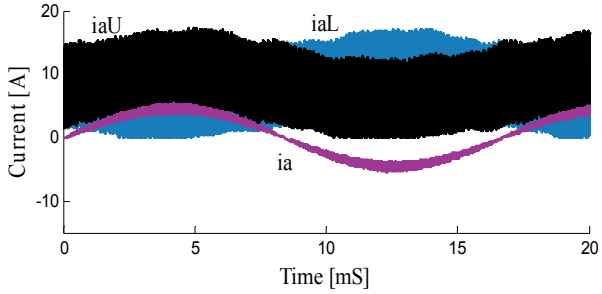


Figure 5-5: Simulated SPWM: upper and lower winding currents and output current in phase A (m_a =0.4, f_c= 15 kHz)

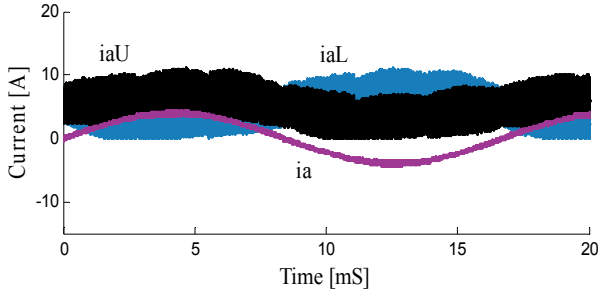


Figure 5-6: Simulated DPWM1: upper and lower winding currents and output current in phase A (m_a =0.4, f_c= 15 kHz)

In both methods, the switching states are determined by the single-shaped reference waveform. Only the magnitude of the reference waveform changes over the modulation range. The coupled inductor inverter with the interleaved PWM schemes has a fairly good performance at high-modulation depths. At low-modulation depths, as shown in Figure 5-5 and Figure 5-6, a high winding current ripple is produced, degrading the performance of the drive by possibly increasing the inductor losses. This result is due to the lack of freedom in selecting switching states in both methods, which limits the use of these methods to high-modulation depths.

5.4.2. Interleaved SPWM and DPWM1 THD Results

The spectra of the winding currents and the phase A current for the SPWM and DPWM1 methods are shown in Figure 5-7 and Figure 5-8, respectively. For a nominal switching frequency of 15 kHz, the effective switching frequency seen in the output of the interleaved SPWM and DPWM1 methods is doubled (to 30 kHz). The spectra of the

line-line voltage for the SPWM and DPWM1 methods at m_a=0.9 are shown in Figure 5-9 and Figure 5-10, respectively. As expected in section 4.2 , the voltage THD of SPWM is higher than that of DPWM1. Thus, DPWM1 can provide much lower harmonic distortion than SPWM (especially if the switching frequency is increased to match the inverter losses). For the same rms output current in Figure 5-7 and Figure 5-8, the THD difference between the SPWM and DPWM output current harmonics is smaller than that of output voltage harmonics; the difference between the upper and lower winding current THDs is about 6%.

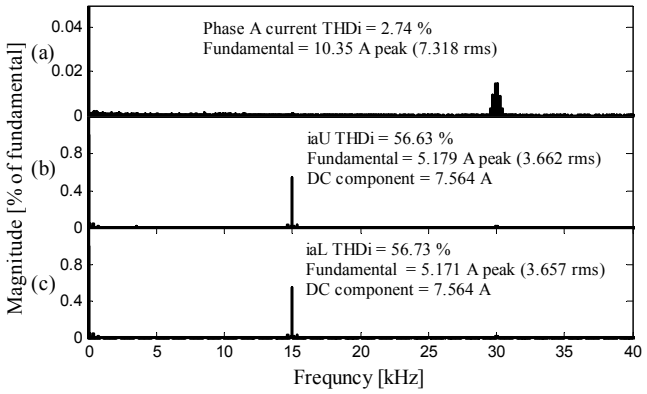


Figure 5-7: Simulated SPWM: harmonic spectrum (a) phase A current (b) upper winding current (c) lower winding current(m_a =0.9)

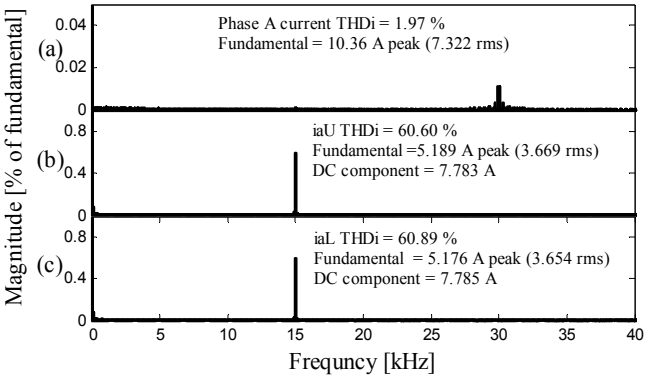


Figure 5-8: Simulated DPWM1: harmonic spectrum (a) phase A current (b) upper winding current (c) lower winding current (m_a =0.9)

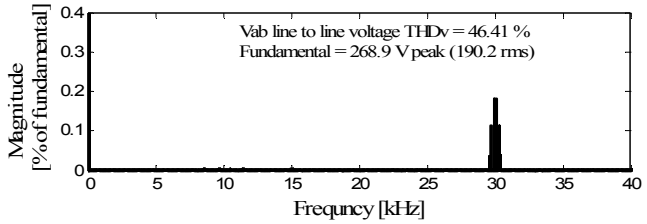


Figure 5-9: Simulated SPWM: line-line voltage harmonic spectrum (m_a =0.9)

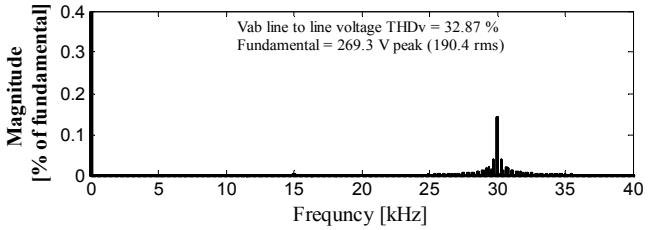


Figure 5-10: Simulated DPWM1: line -line voltage harmonic spectrum (m_a =0.9)

5.4.3. Interleaved SPWM and DPWM1 Experimental Results

The experimental results of the upper and lower winding currents and the output current in phase A for the interleaved SPWM and DPWM1 methods are illustrated in Figure 5-11 through Figure 5-14 at m_a =0.9 and 0.4. These results follow the simulation graphs given in Figure 5-3 through Figure 5-6. The winding current ripple with SPWM in Figure 5-13 is higher than that with DPWM1 in Figure 5-14 at m_a=0.4 (a low-modulation depth). This additional harmonic content can be explained by considering that with SPWM, the interaction of all three legs in the coupled inductor inverter causes excessive current ripple. However, with DPWM1, only two inverter legs switches are active at any point along the fundamental voltage cycle, minimizing the high frequency AC flux (as the common mode DC current has equal magnitude in all three limbs), and leading the common mode ripple to produce a flux in the core [25].

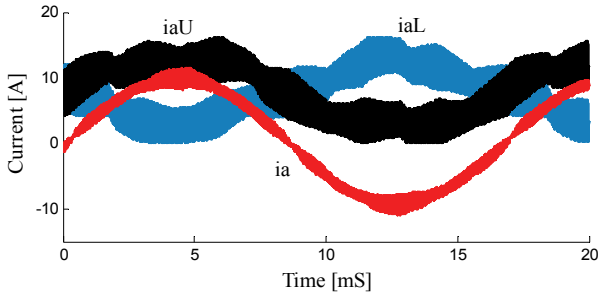


Figure 5-11: Experimental SPWM: winding currents and phase A current (m_a =0.9, f_c= 15 kHz)

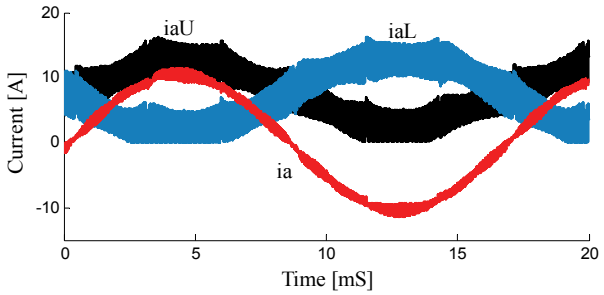


Figure 5-12: Experimental DPWM1: winding currents and phase A current (m_a =0.9, f_c= 15 kHz)

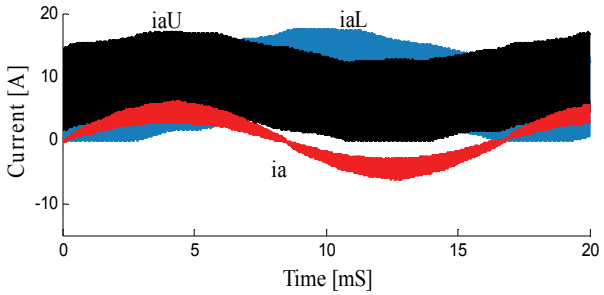


Figure 5-13: Experimental SPWM: winding current and phase A current (m_a=0.4, f_c= 15 kHz)

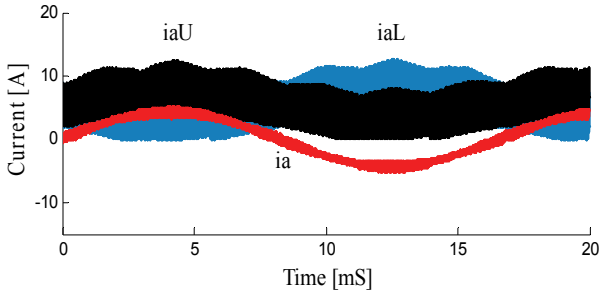


Figure 5-14: Experimental DPWM1: winding current and phase A current (m_a=0.4, f_c= 15 kHz)

Although the winding currents have large current ripples, the output current in SPWM and DPWM1 are sinusoidal with much lower current ripple. The lower output current ripple is achieved because of the interleaved switching, which increases the effective output switching to twice the actual switching frequency. Generally, compared with SPWM, DPWM1 generates multi-level output voltages (as shown in section 4.2), reduces switching losses (due to the 60º discontinuous period), and has a lower winding current ripple at low-modulation depths. However, although the quality of the output waveforms with the interleaved DPWM1 scheme is high; the overall performance of the inverter is degraded because of the inductor losses which can be produced due to the high winding current ripple.

5.5. CII Performance with Original SVPWM

Comprehensive simulation results are demonstrated for the original SVPWM scheme. The characteristic of this modulation method is explored for switching states sequence 1 and sequence 2. The experimental results are obtained to validate the simulation results.

5.5.1. Original SVPWM Simulation Results

The upper and lower winding currents and the output current in phase A for the original SVPWM sequence 1 and 2 described in section 4.4 are illustrated in Figure 5-15 through

Figure 5-20. Figure 5-15, Figure 5-17 and Figure 5-19 show these currents for switching sequence 1, which includes the low effective inductance states that are avoided in sequence 2, shown in Figure 5-16, Figure 5-18 and Figure 5-20. The plots indicate the performance at m_a values of 0.9, 0.8 and 0.4 and validate that the original SVPWM algorithm works at various modulation depths.

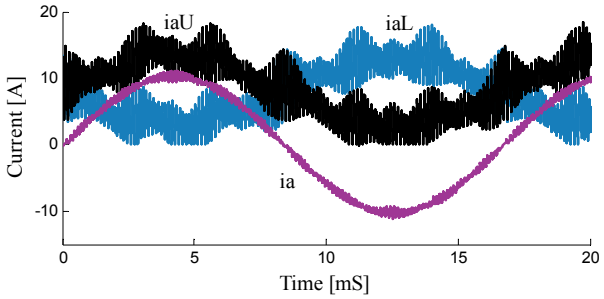


Figure 5-15: Simulated original SVPWM: winding currents, and output current in phase A, sequence 1, (m_a =0.9, f_c=15 kHz)

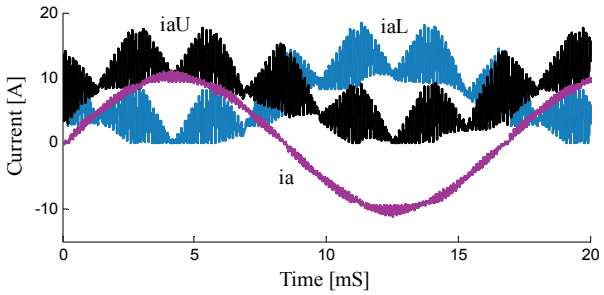


Figure 5-16: Simulated original SVPWM: winding currents, and output current in phase A, sequence 2, (m_a =0.9, f_c=15 kHz)

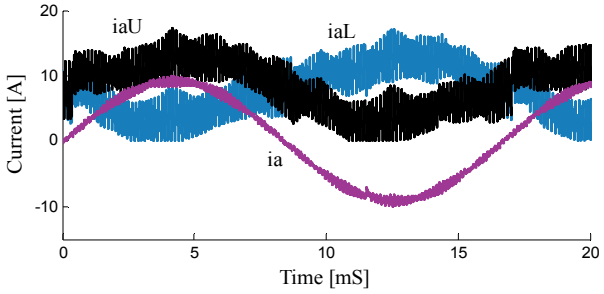


Figure 5-17: Simulated original SVPWM: winding currents and output current in phase A, sequence 1, (m_a =0.8, f_c=15 kHz)

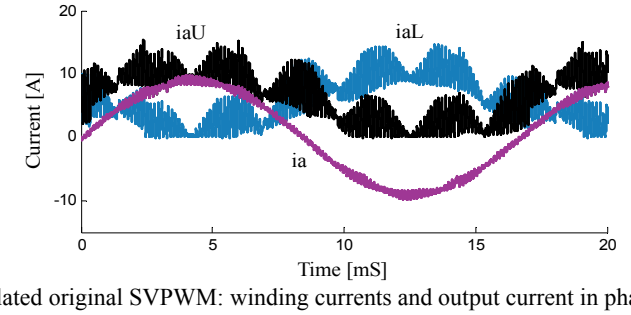


Figure 5-18: Simulated original SVPWM: winding currents and output current in phase A, sequence 2, (m_a =0.8, f_c=15 kHz)

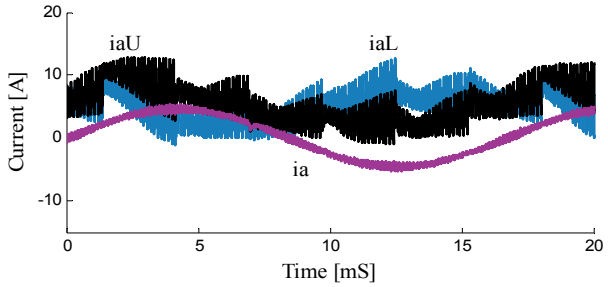


Figure 5-19: Simulated original SVPWM: winding currents and output current in phase A, sequence 1, (m_a =0.4, f_c= 15 kHz)

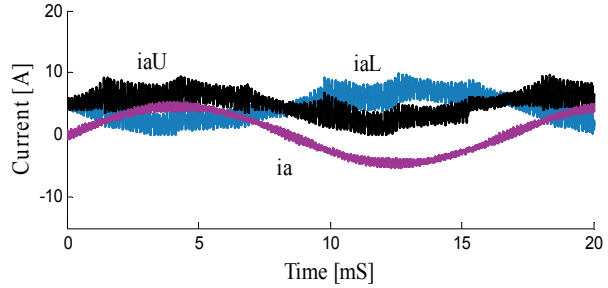


Figure 5-20: Simulated original SVPWM: winding currents and output current in phase A, sequence 2, (m_a =0.4, f_c= 15 kHz)

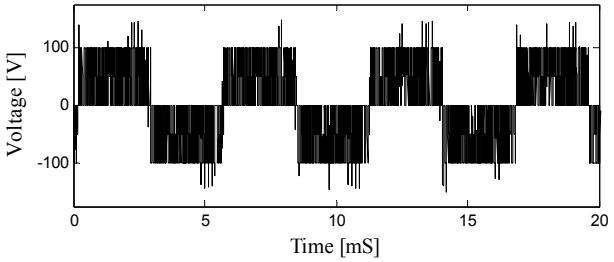


Figure 5-21: Simulated original SVPWM : common mode voltage, sequence 1

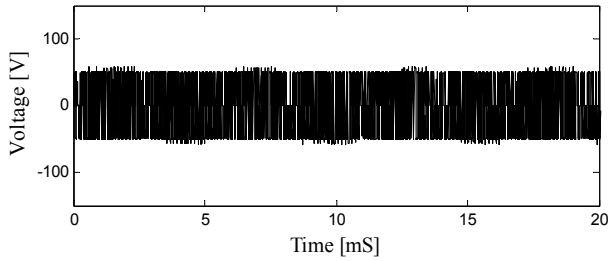


Figure 5-22: Simulated original SVPWM : common mode voltage, sequence 2

The simulated waveforms of the variation of the common mode output voltage at 60 Hz are shown in Figure 5-21 and Figure 5-22 for the two switching sequences. The results show the superiority of the switching sequence 2 since the peak value of the voltage between the DC bus midpoint and the load neutral point, which contributes to the common mode voltage, is limited to $V_{DC}/3$ for sequence 1 but $V_{DC}/6$ for sequence 2. The switching frequency ripple is the same for both cases, at $V_{DC}/6$, but the high-frequency

switching states (sequence 2) result in the voltage ripple being consistently distributed at about zero volts, whereas the lower inductance sequence (sequence 1) results in a third harmonic common mode voltage.

5.5.2. Original SVPWM THD Results

To compare the harmonic content of these two switching sequences, the spectra of the output current and upper winding current are illustrated in Figure 5-23 and Figure 5-24 for sequence 1 and sequence 2, respectively when m_a = 0.8. The DC component, fundamental rms, total rms, and THD of the two switching sequences are tabulated in Table 5-1 and Table 5-2. The simulation results demonstrate that the output current waveforms for both switching sequences are similar. However, for the winding currents, the switching pattern with low-inductance states has a larger DC component (7.39A) and larger total rms (5.7A); a lower harmonic content occurs when high-inductance states are used. These factors affect both the winding losses and the core losses in the coupled inductor, as shown later in section 5.8.2. The switching sequence that concentrates on the high-inductance states can allow the size of the core to be reduced due to the lower harmonic content and lower winding rms current. In addition, concentrating on high-inductance states may allow the redesign of the inductor to have a lower overall inductance, as the coupled inductor need not be designed to enable operation at the low effective inductance states.

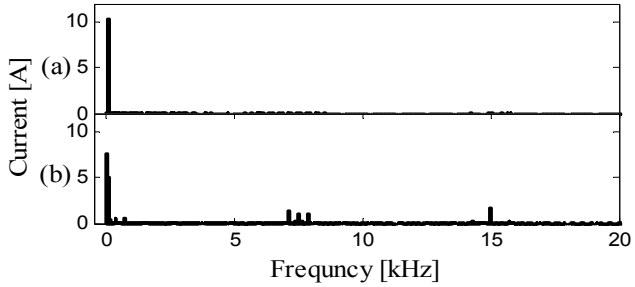


Figure 5-23: Simulated original SVPWM: harmonic spectra for (a) phase A output current (b) upper winding current, sequence 1, (m_a =0.9, f_c=15 kHz)

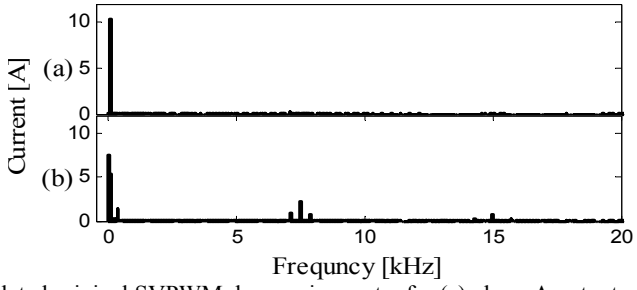


Figure 5-24: Simulated original SVPWM: harmonic spectra for (a) phase A output current (b) upper winding current, sequence 2, (m_a =0.9, f_c=15 kHz)

Table 5-1: Simulated original SVPWM harmonic content for sequence 1

	ia	iaU	iaL
DC	0.01 A	7.39 A	7.39 A
60 Hz	9.11 A	4.47 A	4.64 A
Total rms	9.334 A	5.726 A	5.899 A
THD	4.97%	64.11%	61.62%

Table 5-2: Simulated original SVPWM harmonic contents for sequence 2

	ia	iaU	iaL
DC	0.01 A	6.11 A	6.1 A
60 Hz	9.09 A	4.46 A	4.67 A
Total rms	9.317 A	5.629 A	5.853 A
THD	5.06%	59.29%	57.08%

Figure 5-25 and Figure 5-26 plot the output phase current and line-line voltage THD as a function of m_a. These plots clearly demonstrate that the two switching sequences offer similar quality output waveforms. Therefore, as expected, the selecting of switching states does not affect the inverter outputs since the only inductance seen in the output is the leakage inductance (see section 3.4). However, the quality of the output waveforms is dependent on the PWM strategies.

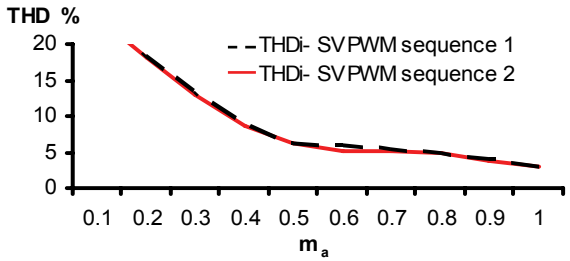


Figure 5-25: Simulated original SVPWM phase A current THD

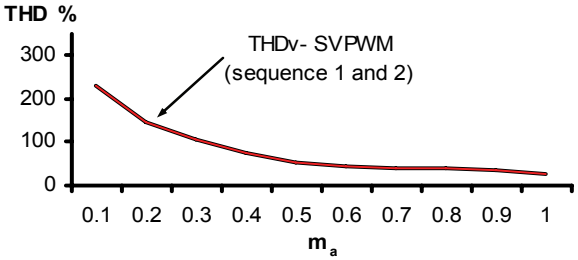


Figure 5-26: Simulated original SVPWM line-line voltage THD

Additional simulations compare the performance of the SVPWM schemes to the interleaved SPWM and DPWM1 schemes. The output line-line voltage and phase current THD are plotted as a function of m_a in Figure 5-27 and Figure 5-28, respectively. For the line-line voltage THD, the SVPWM THD is superior over the full range of m_a. However, the output phase current THD is higher for SVPWM at low m_a. One of the reasons for the relatively poor output phase current THD is that although the nominal switching

frequencies are the same, the SVPWM schemes result in a output harmonic at ½ of the switching frequency. This low harmonic occurs as a result of the opposing vector sequencing in two switching cycles.

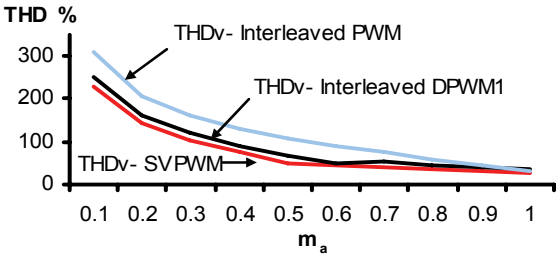


Figure 5-27: Simulated original SVPWM, DPWM1 and SPWM line-line voltage THD

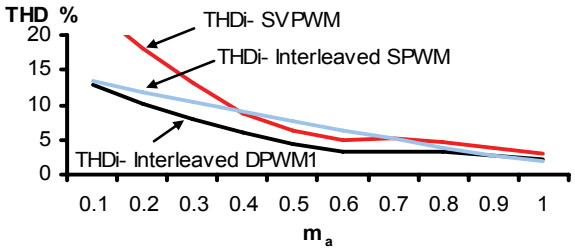


Figure 5-28: Simulated original SVPWM, DPWM1 and SPWM phase A current THD

5.5.3. Original SVPWM Experimental Results

Figure 5-29 and Figure 5-30 plot the line-line voltage (V_{AB}) and the phase A current waveforms for m_a at 1.0, 0.75, 0.5 and 0.25 with 60Hz fundamental frequency, when sequence 2 (which has high-inductance states) is used. Multi-level voltage output waveforms can be seen in Figure 5-29.

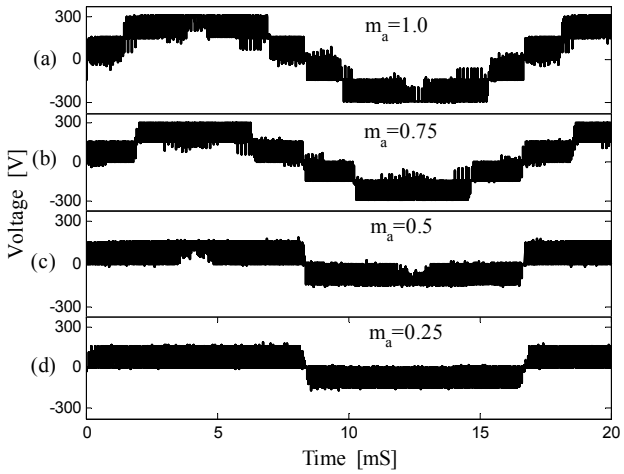


Figure 5-29: Experimental original SVPWM: line-to-line voltage (V_{ab}) for sequence 2 with (a) m_a=1.0 (b) m_a=0.75 (c) m_a=0.5 (d) m_a=0.25

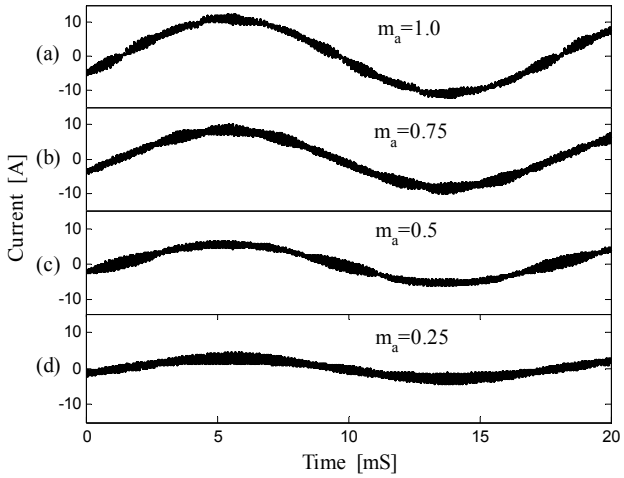


Figure 5-30: Experimental original SVPWM: phase A current for sequence 2 with (a) m_a=1.0 (b) m_a=0.75 (c) m_a=0.5 (d) m_a=0.25

The upper and lower phase A winding currents and output currents at m_a= 0.9 are plotted in Figure 5-31 to Figure 5-32 for the SVPWM sequences 1 and 2. The results plotted show clearly that the original SVPWM schemes compare well with SPWM and DPWM1 (see Figure 5-11 and Figure 5-12), especially when one considers that the nominal switching frequencies are the same but the effective switching frequency of the SVPWM schemes is lower than the nominal switching frequency.

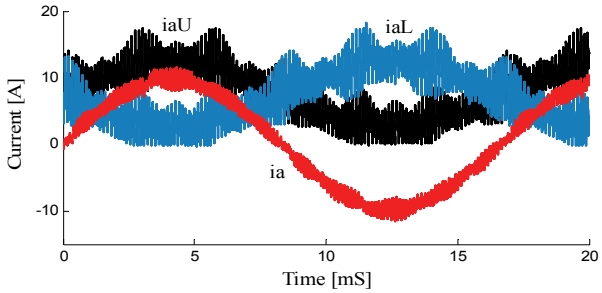


Figure 5-31: Experimental original SVPWM : winding currents and phase A current, sequence 1 (m_a =0.9, f_c= 15 kHz)

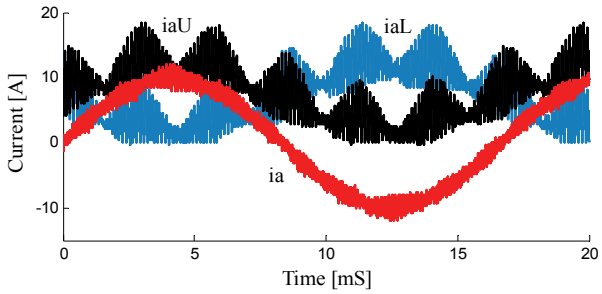


Figure 5-32: Experimental original SVPWM : winding currents and phase A current, sequence 2, (m_a =0.9, f_c= 15 kHz)

The upper and lower phase A winding currents and output currents at m_a= 0.4 are plotted in Figure 5-33 for only the original SVPWM sequence 2. The winding current ripple is lower compared with that of SPWM and DPWM1 in Figure 5-13 and Figure 5-14, respectively. The balanced common mode dc current for SVPWM with high-inductance switching states is plotted in Figure 5-34, together with the results from DPWM1 and SPWM. Under SVPWM, the total rms of the high-frequency winding current may be reduced.

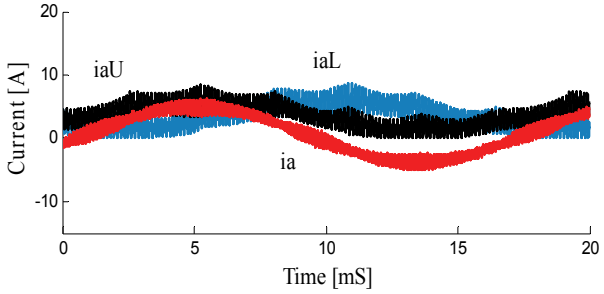


Figure 5-33: Experimental original SVPWM: winding currents and phase A current, sequence 2, (m_a=0.4, f_c= 15 kHz)

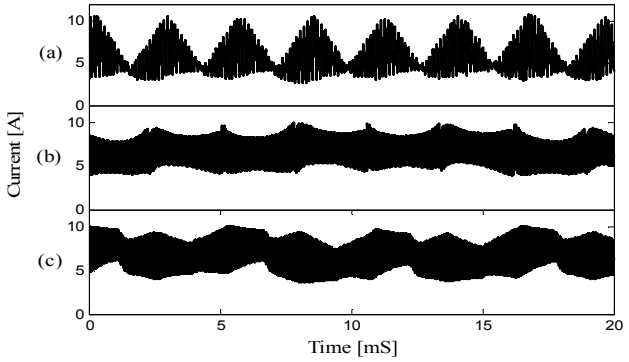


Figure 5-34: Experimental common mode dc current with (a) SVPWM (b) DPWM1 (c) SPWM plus third harmonic (m_a =0.9, f_c= 15 kHz)

5.6. CII Performance with Improved SVPWM

Comprehensive simulation results are demonstrated for the improved SVPWM scheme. The characteristic of this modulation method is explored and compared with the original SVPWM and DPWM1 schemes. The simulation results are validated by the experimental results.

5.6.1. Improved SVPWM Simulation Results

The upper and lower winding currents and the output current in phase A for the improved SVPWM are illustrated in Figure 5-35 and Figure 5-36 with m_a at 0.9 and 0.4,

respectively. The simulation results validate that this algorithm works over a wide range of modulation depths. At m_a= 0.9, the peak-to-peak current ripples in improved SVPWM are slightly higher than those of the SPWM1 and DPWM1 methods (see Figure 5-3 and Figure 5-4, respectively). However, it can be observed that at m_a =0.4, the improved SVPWM has a significantly lower peak-to-peak current ripple compared with ripples of the previous methods. The lower current ripple has been achieved with further elimination of switching states (c) and (d) in Figure 3-15 for a zero voltage vector at low-modulation depths.

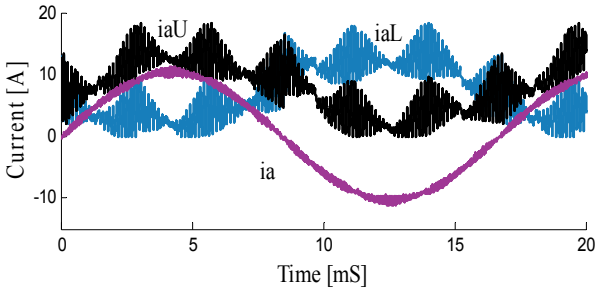


Figure 5-35: Simulated improved SVPWM: winding currents and output current in phase A (m_a =0.9, f_c=15 kHz)

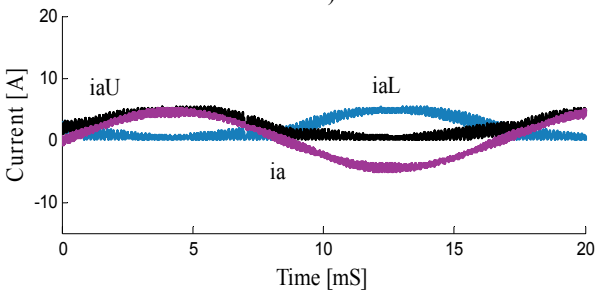


Figure 5-36: Simulated improved SVPWM: winding currents and output current in phase A (m_a =0.4, f_c=15 kHz)

5.6.2. Improved SVPWM THD Results Comparison

Additional simulations compare the harmonic spectra of the phase A current, upper and lower winding currents, and V_{ab} line-line voltage for the optimal and original SVPWM schemes (at m_a =0.9), as illustrated in Figure 5-37 to Figure 5-40. For a nominal switching frequency of 15kHz, as shown in Figure 5-7 to Figure 5-10, the effective switching frequency in the output of the interleaved SPWM and DPWM1 is doubled (to 30kHz). In contrast, in the spectra for the improved SVPWM scheme in Figure 5-37 and Figure 5-39, the switching harmonics in the output are at the nominal switching frequency (15kHz); the spectra of the original SVPWM scheme shown in Figure 5-38 and Figure 5-40 indicate that the switching frequency in the output signal is half of the nominal frequency (7.5kHz).

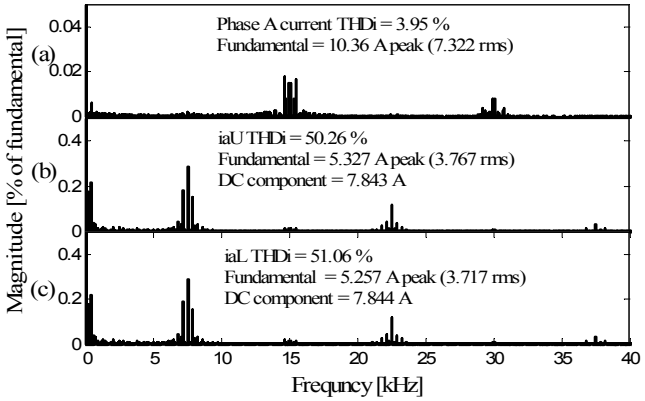


Figure 5-37: Improved SVPWM: Harmonic spectrum (a) phase A current (b) upper winding current (c) lower winding current (m_a =0.9)

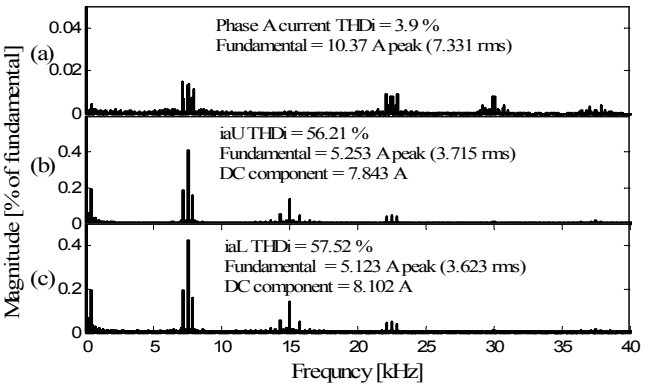


Figure 5-38: Original SVPWM : Harmonic spectrum (a) phase A current (b) upper winding current (c) lower winding current (m_a =0.9)

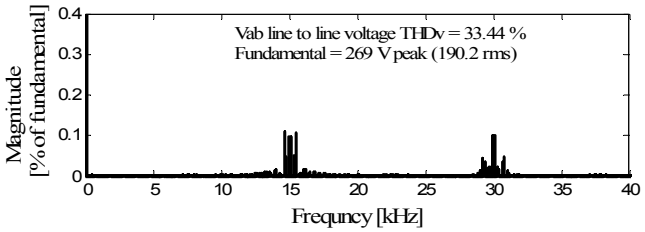


Figure 5-39: improved SVPWM: line-line voltage harmonic spectrum (m_a =0.9)

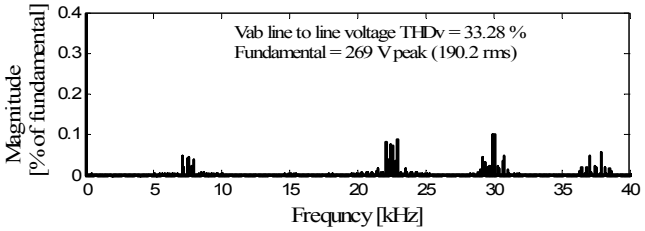


Figure 5-40: Original SVPWM: line-line voltage harmonic spectrum (m_a =0.9)

The effective average switching frequency for the SVPWM schemes in the winding current spectra is only 7.5 kHz: the choice of the switching state to minimize switching losses is such that the SVPWM schemes are on average switching at half the nominal frequency.

Unlike the original SVPWM scheme, the improved SVPWM scheme is capable of providing an output signal with the lowest switching harmonics at twice the average actual switching frequency. This performance is similar to that of the SPWM and DPWM1 schemes, although in these schemes, the effective switching frequency is equal to the nominal value. Increasing the nominal switching frequency of the SVPWM scheme may be possible to produce a signal with winding harmonics at 15kHz and output harmonics at 30kHz, if doing so is desired.

To compare the performance of SVPWM with that of SPWM and DPWM1, the harmonic spectra of the output current and output line-to-line voltage are illustrated as a function of m_a in Figure 5-41 and Figure 5-42. For the line-line voltage THD, the SVPWM THD is superior over the full range of m_a. However, the phase current THD in DPWM1 is superior over the full range of m_a. The SVPWM current THD is low at higher values of m_a, but at low m_a, the SVPWM THD is higher than the DPWM1 and SPWM THD.

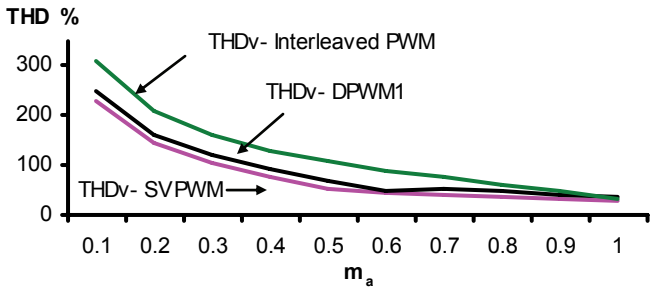


Figure 5-41: SVPWM, DPWM1 and SPWM line-line voltage THD

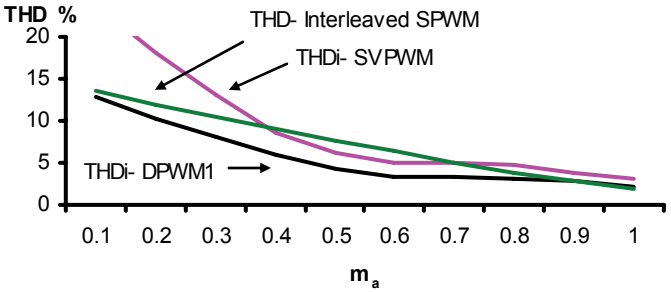


Figure 5-42: SVPWM, DPWM1 and SPWM phase A current THD

Similar to the results from the original SVPWM scheme, the THD results show that the selection of different switching states does not change the output current and voltage profile in SVPWM. The current and voltage spectra for the original and improved SVPWMs are coincident in Figure 5-41 and Figure 5-42. However, in Figure 5-43 and

Figure 5-44, the improved SVPWM with the elimination of all possible low-inductance switching states has, overall, a lower winding THD. The switching states with the effective high inductance can reduce the THD in the winding current but do not significantly affect the output current or voltage. The comparison of the upper and lower winding current THD in Figure 5-43 and Figure 5-44 verifies that the overall performance of the improved SVPWM is better than that of the original SVPWM, especially at low-modulation depths.

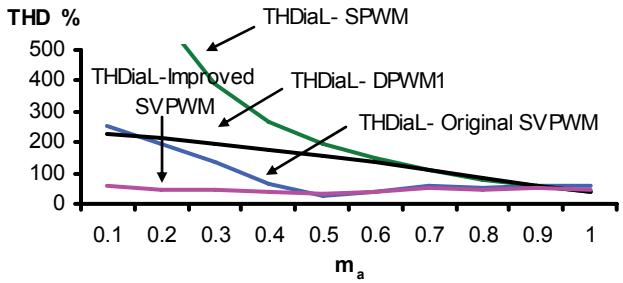


Figure 5-43: SVPWM, DPWM1 and SPWM phase A lower winding current THD

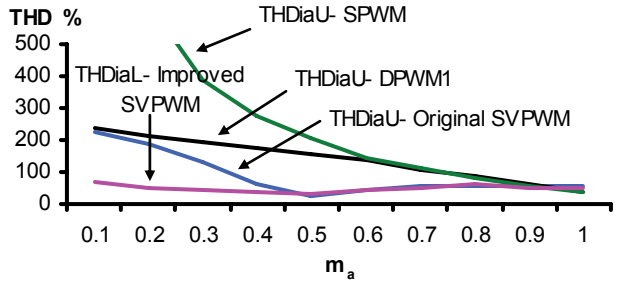


Figure 5-44: SVPWM, DPWM1 and SPWM phase A upper winding current THD

The major harmonic reduction occurs in lower m_a (m_a<0.5) due to the additional eliminating of the low-inductance switching states of (c) and (d) in Figure 3-15 for a zero voltage space vector. Since these switching states occur at modulation depths lower than 0.5, THD is also reduced in this modulation range. The windings THD in the improved SVPWM, as shown in Figure 5-43 and Figure 5-44, is significantly lower than that of DPWM1 and SPWM.

5.6.3. Improved SVPWM Experimental Results

Figure 5-45 and Figure 5-46 show the line-line voltage (V_{ab}) and the phase A current waveforms with m_a at 1.0, 0.8, 0.5 and 0.2 with the fundamental frequency of 60Hz, respectively. Multi-level voltage output waveforms can clearly be seen in Figure 5-45.

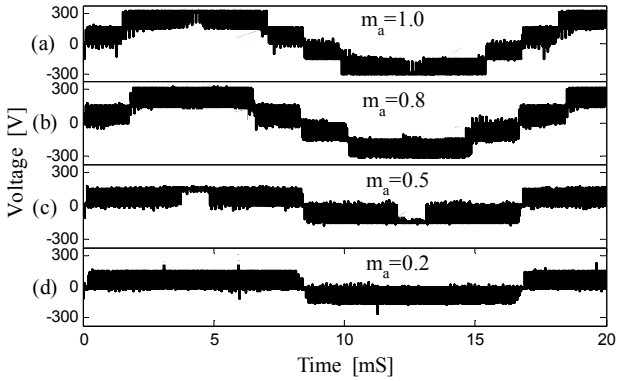


Figure 5-45: Experimental improved SVPWM: line-line voltage (Vab) with (a) m_a =1.0 (b) m_a=0.8 (c) m_a =0.5 (d) m_a =0.2

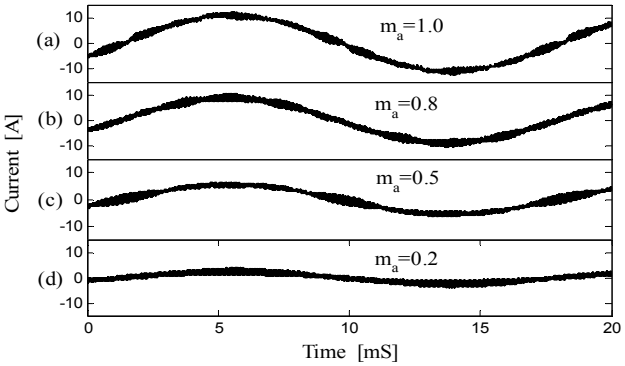


Figure 5-46: Experimental improved SVPWM: phase A current with (a) m_a =1.0 (b) m_a =0.8 c) m_a =0.5 (d) m_a =0.2

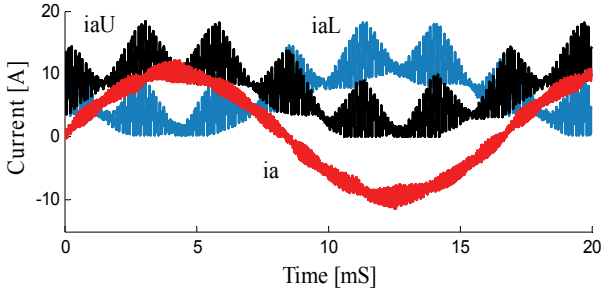


Figure 5-47: Experimental improved SVPWM: winding currents and phase A current (m_a=.9, F_c= 15 kHz)

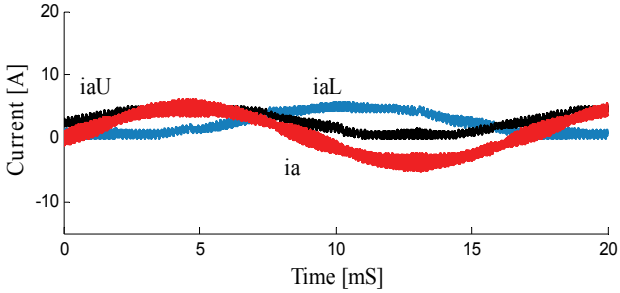


Figure 5-48: Experimental improved SVPWM: winding currents and phase A current (m_a=0.4, f_c= 15 kHz)

The upper and lower winding currents and the phase A currents for the improved SVPWM are plotted in Figure 5-47 to Figure 5-48, respectively, when m_a is 0.9 and 0.4,

respectively. These winding current waveforms are close to the simulation results for m_a=0.4 given in Figure 5-35 and Figure 5-36. For the improved SVPWM current waveforms, the peak to peak winding current ripple is significantly reduced at lower modulation depths compared with that in SPWM, DPWM1, and original SVPWM. In addition, the simulation results clearly show that the improved SVPWM scheme compares well with the original SVPWM, SPWM and DPWM1 schemes at high-modulation depths. Thus, when the full operating range is required, the proposed SVPWM provides a superior inverter performance. The improved SVPWM improves the performance at low-modulation depths by lowering the winding current ripple but not the output waveforms' quality since the effective output switching frequency is nominal.

5.7. CII Performance with Interleaved DSVPWM

The simulations results for DSVPWM0, DSVPWM1 and DSVPWM3 modulation schemes are demonstrated and compared at low-modulation indices. The DSVPWM1 simulation results are obtained for three different SVPWM methods at high-modulation indices. The characteristic of these modulation schemes are explored and compared with other PWM schemes. The simulation results are verified by the experimental results.

5.7.1. Interleaved DSVPWM Simulation Results ($m_a < 0.5$)

By using the interleaved DSVPWM strategy, a 60º discontinuous period can be distributed in each positive and negative cycle of the fundamental reference voltage over a range of modulation indices. Generalized 60º discontinuous SVPWM strategies can be categorized as interleaved DSVPWM0, DSVPWM1, and DSVPWM3. This approach can also be expanded to DSVPWM2, but since the results of this scheme for a purely resistive load (or a unity power factor load) are similar to DSVPWM0, the discussion is not explained here [24]. The following simulation results compare DSVPWM0, DSVPWM1, and DSVPWM3 methods at m_a<0.5.

The load fundamental phase voltage (V_{An1}) to the load neutral point (n) and the inverter filtered terminal voltage (V_{Ao}) to the DC bus midpoint (o) are shown at m_a = 0.4 in Figure 5-49, Figure 5-50 and Figure 5-51 for the DSVPWM0, DSVPWM1 and DSVPWM3 schemes, respectively. 60º discontinuous regions (where the terminal voltage is clamped to either $\pm V_{dc}/2$ at the positive and negative cycles) are dispread for these schemes. For a leading power factor load, the discontinuous period can be advanced by up to 30º. This is

DSVPWM0 scheme shown in Figure 5-49. Similar for lagging power factor load, the DSVPWM2 scheme can be obtained. In Figure 5-50, 60º discontinuous SVPWM is located around the peak positive and negative cycles. The resulting waveform is called the DSVPWM1 scheme. However, in Figure 5-51, the discontinuous regions are divided into two 30º discontinuous regions around the peak, indicating the proposed DSVPWM is DSVPWM3.

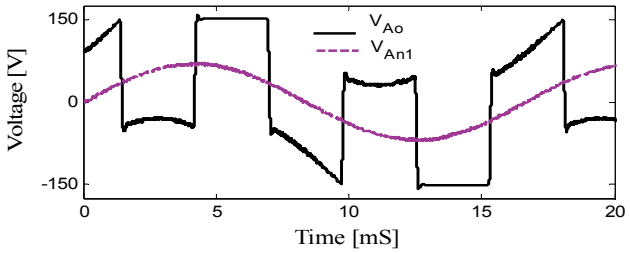


Figure 5-49: DSVPWM0 CII filtered terminal voltage (V_{Ao}) and load fundamental phase voltage (V_{An1}) (m_a =0.4)

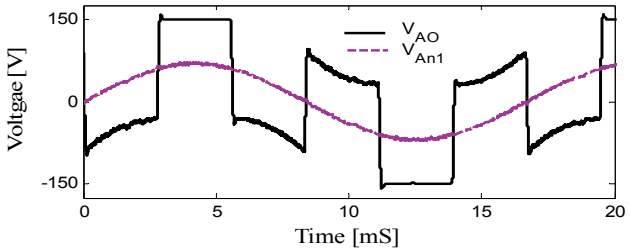


Figure 5-50: DSVPWM1 CII filtered terminal voltage (V_{Ao}) and load fundamental phase voltage (V_{An1}) (m_a =0.4)

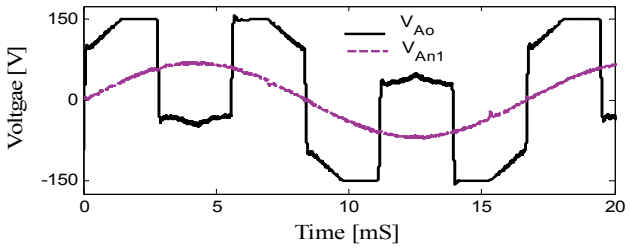


Figure 5-51: DSVPWM3 CII filtered terminal voltage (V_{Ao}) and load fundamental phase voltage (V_{An1}) (m_a =0.4)

The corresponding upper and lower winding currents and phase A currents are plotted in Figure 5-52, Figure 5-53 and Figure 5-54, respectively. With the same optimal use of the high effective inductance switching states, the 60º discontinuous PWM at the positive and negative voltage peaks in DVSPWM1 produces a lower high-frequency winding current ripple compared with that of DSVPWM0 and DSVPWM3: 1.3 and 1.5, respectively. This ripple reduction is more significant compared with that of DPWM1 (see Figure 5-6), by a factor of 2.25.

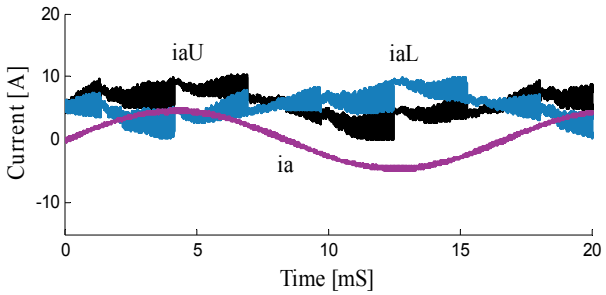


Figure 5-52: Simulated DSVPWM0: winding currents and phase A current (m_a =0.4, f_c= 15 kHz)

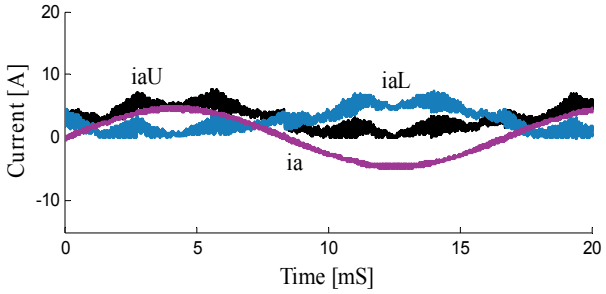


Figure 5-53: Simulated DSVPWM1: winding currents and phase A current (m_a =0.4, fc= 15 kHz)

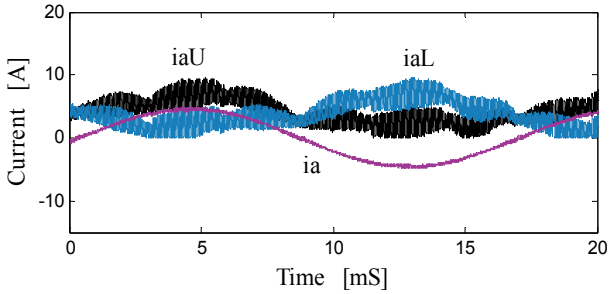


Figure 5-54: Simulated DSVPWM3: winding currents and phase A current (m_a =0.4, f_c= 15 kHz)

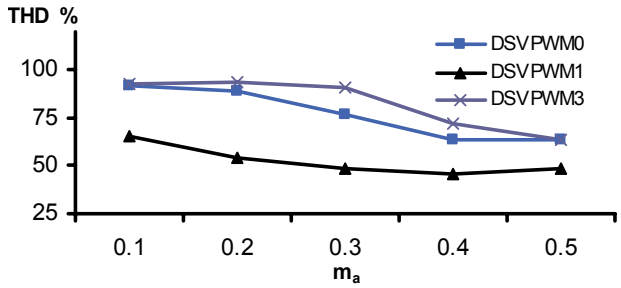


Figure 5-55: Simulated DSVPWM: phase A winding current THD for DSVPWM0, DSVPWM1 and DSVPWM3

The phase A winding current THD for the DSVPWM0, and DSVPWM1 and DSVPWM3 methods are plotted as a function of m_a (m_a<0.5) in Figure 5-55. Compared to the DSVPWM0 and DSVPWM3 THDs, the DSVPWM1 THD is the lowest for different m_a values. The difference between THD profiles indicates that the winding currents ripple in a CII is dependent on not only the selection of switching states with a

high effective inductance but also on the position of the discontinuous PWM period in the inverter output voltage. The current ripple in SVDPWM1 is lower than that in DSVPWM0 and DSVPWM3 for the following reasons.

First, the current ripple in one leg due to its own winding effect is directly minimized when the discontinuous period is located at the positive and negative voltage peak cycles. For the 60º discontinuous periods, the winding is shorted, so the current ripple is not impacted by its own winding. The 60º PWM switching periods around the voltage zero crossing, provide the minimum average winding voltage compared to that if the PWM switching period is located in other parts of the voltage waveform. Thus, the minimum average voltage allocates the most dwell time in each switching cycle for the '01' and '10' switching states (instead of the '00' and '11' switching states) in each switching sequence, which minimize the current ripple.

Second, the current ripple due to the coupling of the other windings is also indirectly minimized. For the 60º discontinuous periods, the other (active) phases with PWM switching are not at around their peak voltages. In addition, since high-inductance states are selected (i.e., the flux produced from one winding is absorbed by the other winding) the effect of the coupling is also minimized. Thus, the minimum average voltage is induced in the shorted winding, which produces the minimum current ripple. For the 60º PWM switching periods, when switching states of '01' and '10' occur in the switching cycle, the windings in the other legs have a minimum impact on the current ripple since high-inductance states are selected with the minimum average voltage. When switching states of '00' and '11' occur in the switching cycle, the windings in the other legs have no impact on the current ripple.

In addition, compared to the DSVPWM0 and DSVPWM3 scheme, the DSVPWM1 scheme also reduces inverter switching losses for a unity power factor load by eliminating PWM switching at the peak voltage when the load current is almost at the maximum value [24, 122-125].

In conclusion, compared with the previous PWM schemes, the DSVPWM1 scheme can improve the inverter performance by reducing switching losses and inductor losses (due to the lower current ripple) while producing high-quality outputs.

5.7.2. Interleaved DSVPWM Simulation Results ($m_a > 0.5$)

Based on results in the previous section, the DSVPWM scheme is developed for m_a

higher than 0.5 to place the discontinuous period around the peak positive and negative voltage cycles. The interleaved DSVPWM method when m_a is higher than 0.5 can be obtained by using three methods, which differ in terms of selecting the large voltage vector when V_{ref} is in triangle Δ_3. The large voltage vector can be selected from either triangle Δ_2 or Δ_4 or both. The corresponding line-to-line voltages at m_a =0.8 are illustrated in Figure 5-56, Figure 5-57 and Figure 5-58. Multi-level voltage is obtained by using all three methods. However, as shown in Figure 5-58, the line-to-line voltage is symmetrical only when the large vector is selected by using the combination of both the triangle Δ_2 and Δ_4 large vectors.

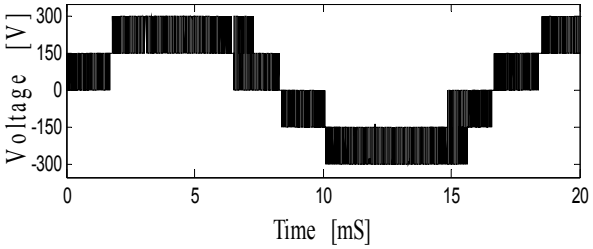


Figure 5-56: Simulated DSVPWM line-line output voltage V_{ab} using a large vector in Δ_2 (m_a =0.8)

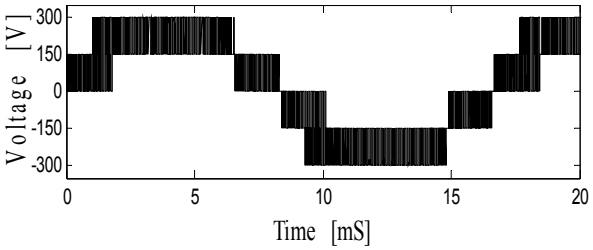


Figure 5-57: Simulated DSVPWM line-line output voltage V_{ab} using a large vector in Δ_4 (m_a =0.8)

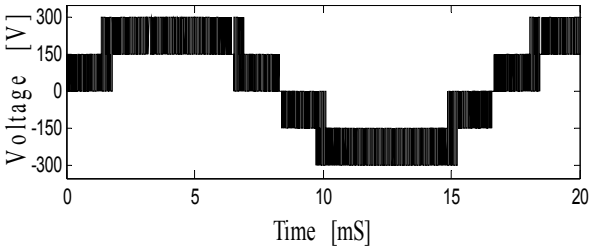


Figure 5-58: Simulated DSVPWM line-line output voltage V_{ab} using combination of large vectors in Δ_2 and Δ_4 (m_a =0.8)

The load fundamental phase voltage (V_{An1}) to the load neutral point (n) and the inverter filtered terminal voltage (V_{Ao}) to the DC bus midpoint (o) are shown for the three methods in Figure 5-59 to Figure 5-61 at m_a =0.8. The sinusoidal fundamental load voltage can be seen in the three methods. For the inverter terminal voltage in Figure 5-59, the 60º discontinuous regions are dispread in DSVPWM compared to those in DPWM1 (see Figure 4-3).

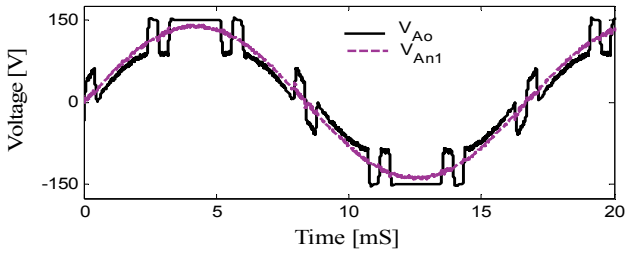


Figure 5-59: Simulated CII filtered terminal voltage (V_{Ao}) and load fundamental phase voltage (V_{An1}) using combination of large vectors in Δ_2 and Δ_4 (ma =0.8)

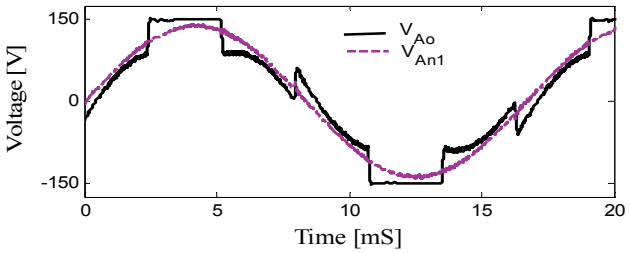


Figure 5-60: Simulated CII filtered terminal voltage (V_{Ao}) and load fundamental phase voltage (V_{An1}) using a large vector in Δ_2 (m_a =0.8)

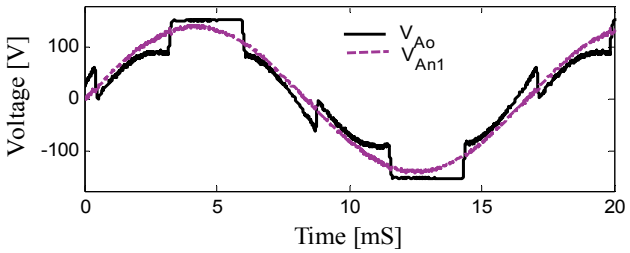


Figure 5-61: Simulated CII filtered terminal voltage (V_{Ao}) and load fundamental phase voltage (V_{An1}) using a large vector in Δ_4 (m_a =0.8)

The upper and lower winding currents and the phase A currents for the three methods are plotted at m_a=0.9 in Figure 5-62 through Figure 5-64 and at m_a=0.8 in Figure 5-65 through Figure 5-67, respectively. The graphs indicate that the performance of the three methods in terms of the winding current and output current ripple is approximately the same for the modulation indices with the value of 0.8 and 0.9.

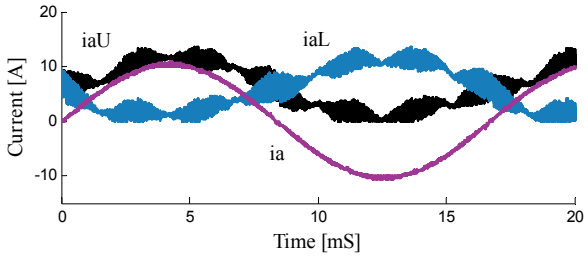


Figure 5-62: Simulated DSVPWM: winding currents and output current in phase A using combination of large vectors in Δ_2 and Δ_4 (m_a =0.9)

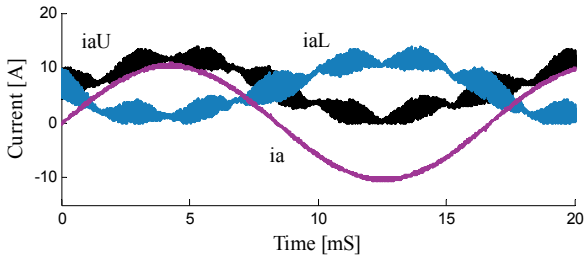


Figure 5-63: Simulated DSVPWM: winding currents and output current in phase A using a large vector in Δ_2 (m_a =0.9)

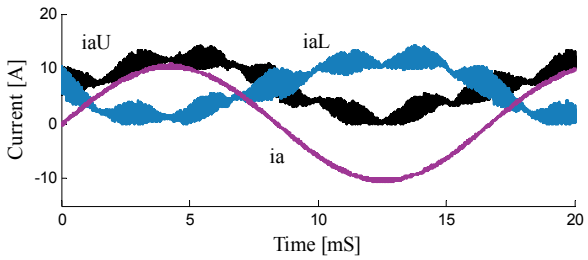


Figure 5-64: Simulated DSVPWM: winding currents and output current in phase A using a large vector in Δ_4 (m_a =0.9)

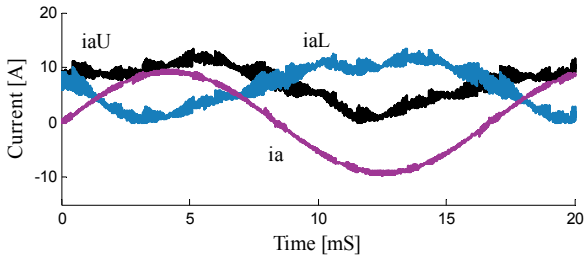


Figure 5-65: Simulated DSVPWM: winding currents and output current in phase A using combination of large vectors in Δ_2 and Δ_4 (ma =0.8)

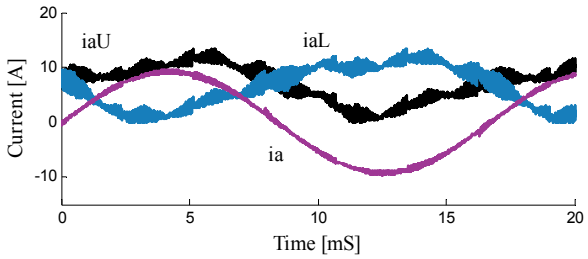


Figure 5-66 : Simulated DSVPWM: winding currents and output current in phase A using a large vector in Δ_2 (m_a =0.8)

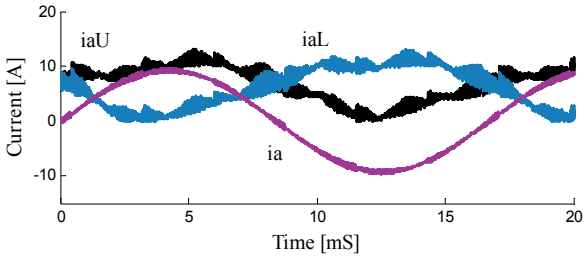


Figure 5-67: Simulated DSVPWM: winding currents and output current in phase A using a large vector in Δ_4 (m_a =0.8)

The harmonic spectra of the upper and lower winding currents and the output current for the three methods are illustrated in Figure 5-68, Figure 5-69 and Figure 5-70 at m_a = 0.9. The harmonic spectra of the line-line voltage for the three methods are shown in Figure 5-71, Figure 5-72 and Figure 5-73. The THD graphs demonstrate a very similar performance for the three methods.

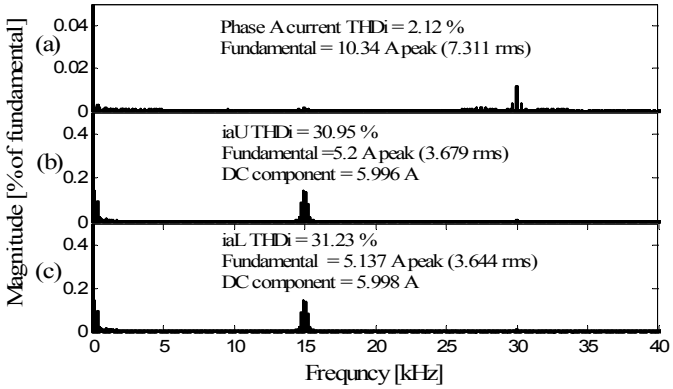


Figure 5-68: Simulated DSVPWM: harmonic spectrum: (a) phase A current (b) upper winding current(c) lower winding current using combination of large vectors in Δ_2 and Δ_4 (m_a =0.9)

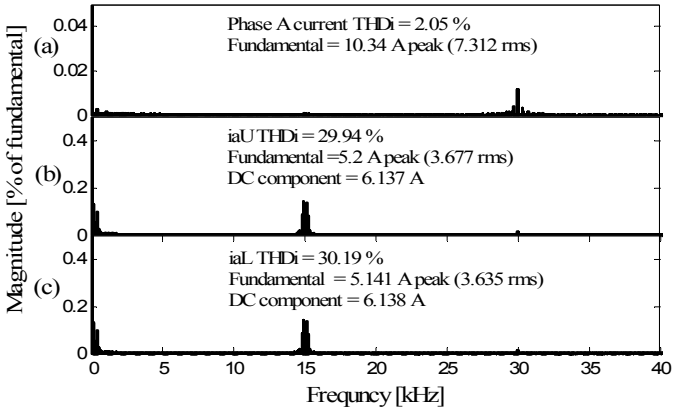


Figure 5-69: Simulated DSVPWM: harmonic spectrum (a) phase A current (b) upper winding (c) lower winding current using a large vector in Δ_2 (m_a =0.9)

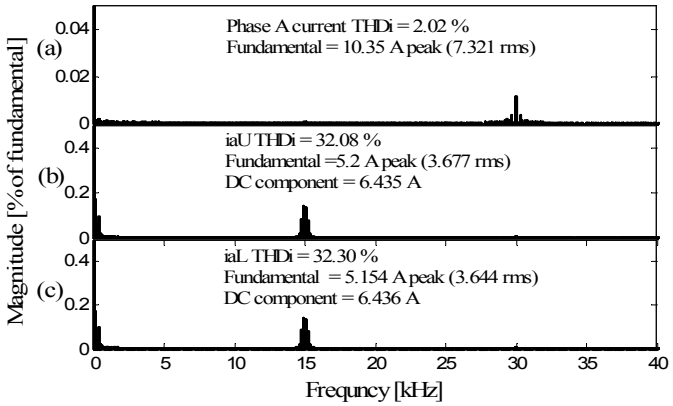


Figure 5-70 Simulated DSVPWM: harmonic spectrum (a) phase A current (b) upper winding (c) lower winding current using a large vector in Δ_4 (m_a =0.9)

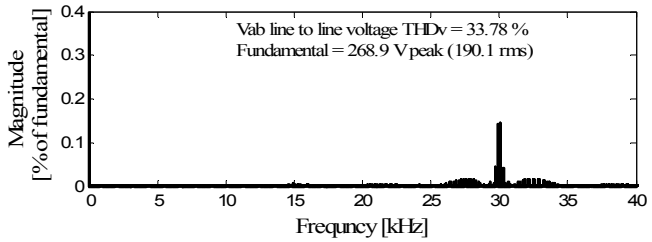


Figure 5-71: Simulated DSVPWM: harmonic spectrum V_{ab} line-line voltage using combination of large vectors in Δ_2 and Δ_4 (m_a =0.9)

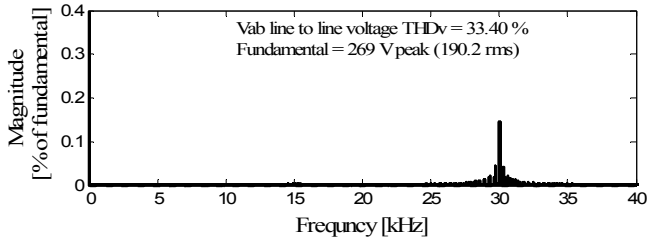


Figure 5-72: Simulated DSVPWM: harmonic spectrum V_{ab} line-line voltage using a large vector in Δ_2 (m_a =0.9)

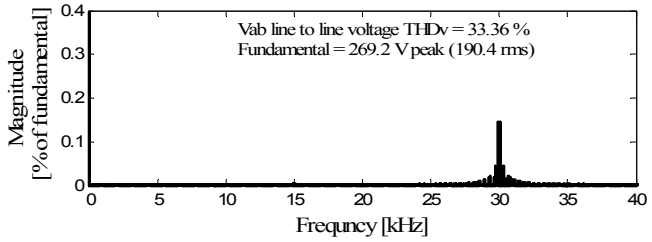


Figure 5-73: Simulated DSVPWM: harmonic spectrum V_{ab} line-line voltage using a large vector in Δ_4 (ma =0.9)

In addition, the voltage THD indicates that the first main switching harmonic (30 kHz) occurs at twice the actual switching frequency (15 kHz). As well, the side-band harmonics can be seen around this frequency. The current THD also verifies that the first switching harmonic happens at 30 kHz. The windings current THD also illustrates the main switching harmonic take places at the switching frequency, and that the other harmonics occur at the odd multiples of the actual switching frequency. Thus, similar to the interleaved DPWM1 scheme, the DSVPWM scheme has the frequency of the output PWM waveforms at twice the actual switching frequency, which has the same inherent harmonic benefits.

5.7.3. Interleaved DSVPWM Common Mode Voltage

The simulated waveforms of the variation of the common mode output voltage at 60 Hz are shown in Figure 5-74 and Figure 5-75 for DSVPWM at m_a =0.9 and m_a =0.4, respectively. The results show that the peak value of the voltage between the DC bus midpoint and the load neutral point, which contributes to the common mode voltage, is

limited to $V_{DC}/6$ at m_a =0.9 and $V_{DC}/2$ for m_a =0.4.

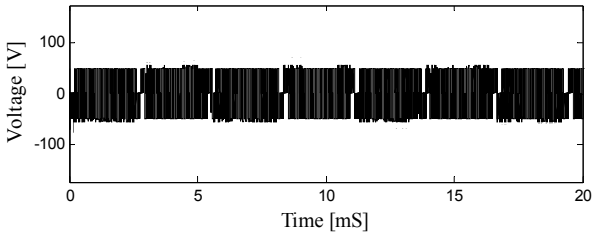


Figure 5-74: Simulated DSVPWM: common mode voltage (m_a =0.9)

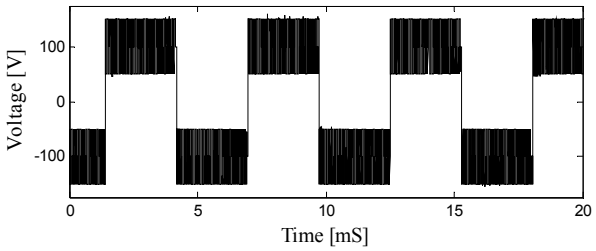


Figure 5-75: Simulated DSVPWM: common mode voltage (m_a =0.4)

5.7.4. Interleaved DSVPWM THD Results

To compare the performance of DSVPWM with that of SPWM and DPWM1, the harmonic spectra of the output current and output line-line voltage are illustrated as a function of m_a in Figure 5-76 and Figure 5-77. Similar to the THD profiles for the SVPWM schemes, the output current and voltage THD profiles for DSVPWM0, DSVPWM1 and DSVPWM3 are the same and labeled by DSVPWM in Figure 5-76 and Figure 5-77.

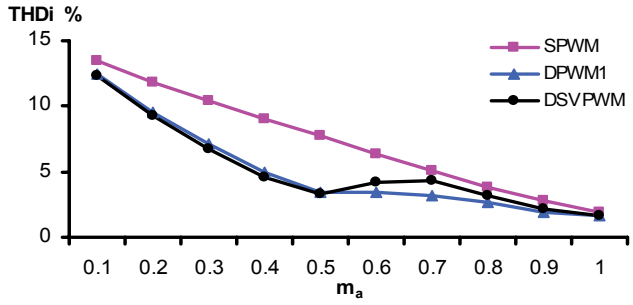


Figure 5-76: Simulated DSVPWM, DPWM1 and SPWM line to line voltage THD

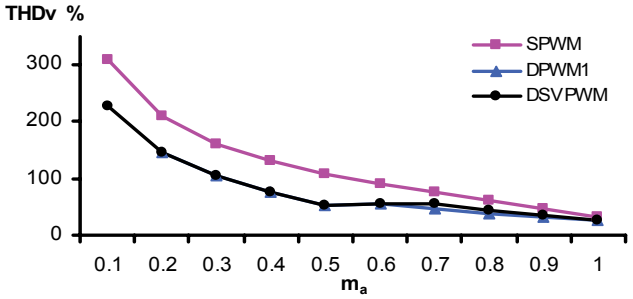


Figure 5-77: Simulated DSVPWM, DPWM1 and SPWM phase A current THD

For the phase current THD, the DPWM1 and DSVPWM THD are the same for m_a<0.5 and m_a>0.9, but the DPWM1 THD is lower than that of DSVPWM between m_a=0.5 and m_a=0.9. This difference in THD results is obtained because of small difference between DPWM1 and DSVPWM voltage THDs as shown in Figure 5-77. Overall, the line-line voltage THDs in DSVPWM and DPWM1 are close to each other for the full m_a range.

The upper winding current THD for DSVPWM1, the improved SVPWM, DPWM1 and SPWM is shown in Figure 5-78. The comparison of the upper winding current THD verifies that the overall performance of the DSVPWM1 is better than that of the other PWM schemes. The winding THD in DSVPWM1 is significantly lower compared with that of DPWM1 and SPWM. As illustrated in Figure 5-78, the DSVPWM1 THD is the same as that of the improved SVPWM for m_a<0.5, and is lower for m_a>0.5 whereas the improved SVPWM with the elimination of all possible low-inductance switching states was expected to have an overall lower winding THD. In addition to the selection of switching states with a high inductance, the time duration to limit the current ramp has a significant impact on the THD profile. DSVPWM1 limits and balances the current ramp in one switching cycle instead of the two switching cycles required in the improved SVPWM. Thus, the combined effects of the high-inductance switching states and the time duration for the current ramps lead DSVPWM1 to have an equal or even better THD performance than that of the improved SVPWM for a full m_a range.

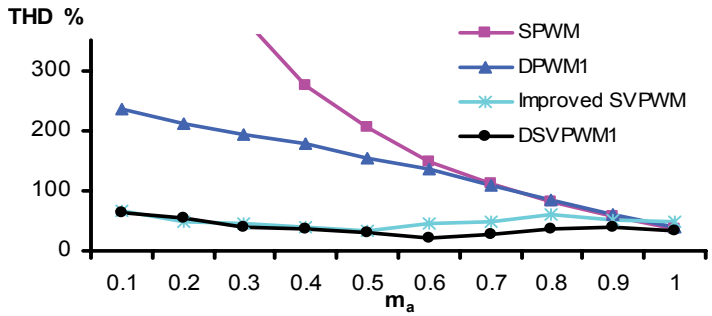


Figure 5-78: Simulated DSVPWM, improved SVPWM, DPWM1 and SPWM phase A upper winding current THD

5.7.5. Interleaved DSVPWM Experimental Results

Figure 5-79 and Figure 5-80 show the line-line voltage (V_{ab}) and phase A current waveforms at m_a values of 1.0, 0.2, 0.5 and 0.8 with the 60Hz fundamental frequency, respectively. Multi-level line-line voltage waveforms and their corresponding sinusoidal output currents can clearly be observed.

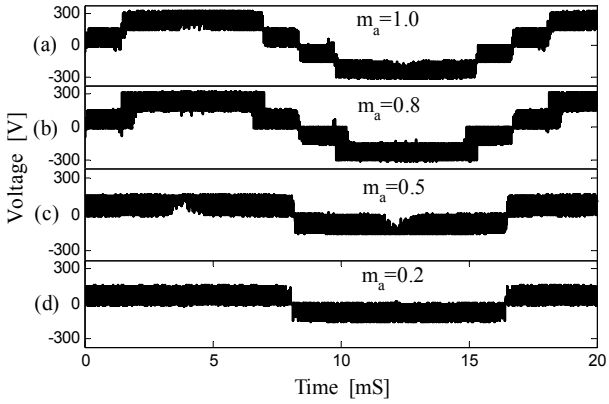


Figure 5-79: Experimental DSVPWM: line-line voltage (V_{ab}) with (a) m_a =1.0 (b) m_a =0.8 (c) m_a =0.5 (d) m_a =0.2

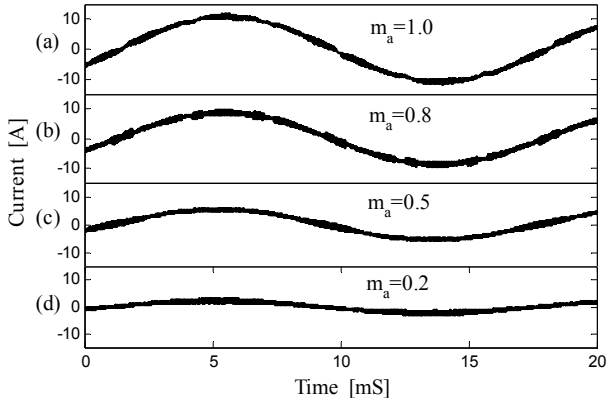


Figure 5-80: Experimental DSVPWM phase A current with (a) m_a =1.0 (b) m_a =0.8 c) m_a =0. 5 (d) m_a =0.2

For example, the upper and lower winding currents and phase A currents are plotted in Figure 5-81 for DSVPWM1 at m_a = 0.9 and in Figure 5-82 for DSVPWM3 at m_a = 0.4. Note that the ripple in the output current can be very low even if the inductor winding currents have a large ripple. The optimal use of the high effective inductance switching states in DVSPWM produces a much lower high-frequency winding current ripple compared with that of DPWM1: lower by a factor of 1.5 at m_a = 0.9 and m_a = 0.4. The current ripple difference is significantly lower by a factor of 3.5 when the winding currents ripple for DSVPWM in Figure 5-83 is compared with DPWM1 in Figure 5-84 at m_a=0.8.

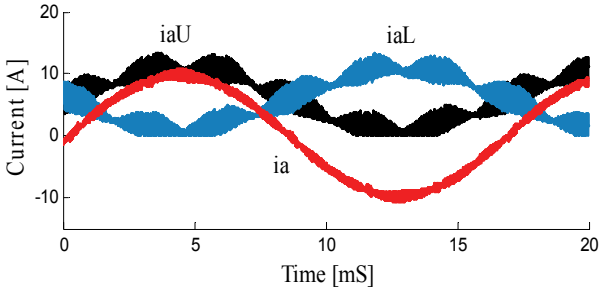


Figure 5-81: Experimental DSVPWM1: winding currents and phase A current (m_a=0.9, f_c= 15 kHz)

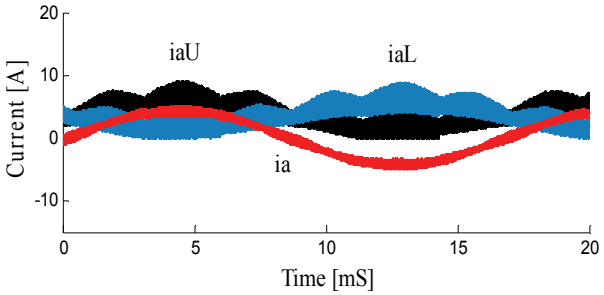


Figure 5-82: Experimental DSVPWM3: winding currents and phase A current (m_a =0.4, f_c= 15 kHz)

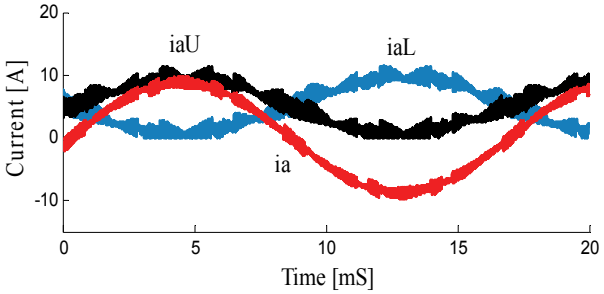


Figure 5-83: Experimental DSVPWM1: winding currents and phase A current (m_a =0.8, f_c= 15 kHz)

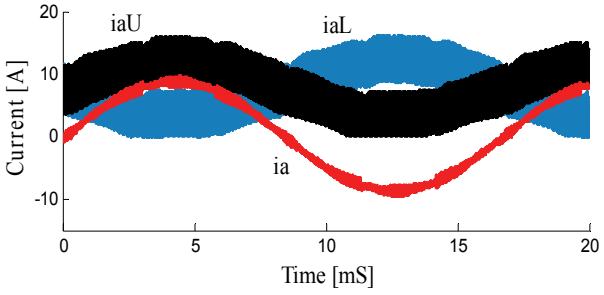


Figure 5-84: Experimental DPWM1: winding current and phase A current (m_a=0.8, f_c= 15 kHz)

The experimental spectra of the output line-line voltage and phase-A current for m_a = 0.9 and 0.4 in Figure 5-85 and Figure 5-86 validate that the proposed DSVPWM produces PWM voltages with a frequency double the effective switching frequency.

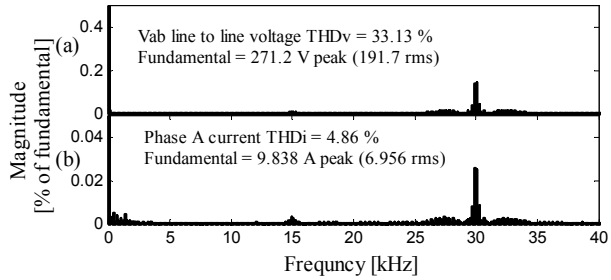


Figure 5-85: Experimental DSVPWM: harmonic spectrum: (a) V_{ab} line-line voltage (b) phase A current (m_a = 0.9, f_c= 15 kHz)

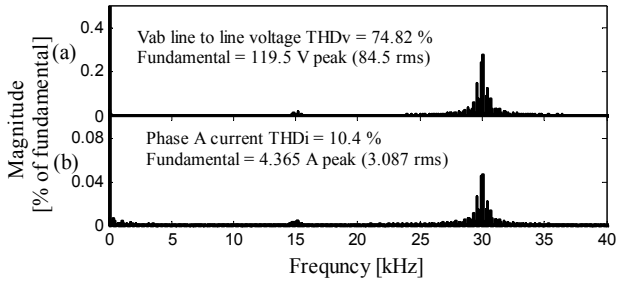


Figure 5-86: Experimental DSVPWM: harmonic spectrum: (a) V_{ab} line-line voltage (b) phase A current (ma = 0.4, f_c= 15 kHz)

Compared to all the PWM strategies described in this thesis, the interleaved DSVPWM1 strategy is demonstrated to produce a lower winding current ripple, resulting in a lower common mode current ripple. In the following section, the effects of this ripple reduction on coupled inductor losses are investigated. A lower winding current ripple produces lower rms, resulting in a lower inductor winding losses, and the lower common mode current ripple reduces the core losses, which are related to the peak of the high-frequency component of the common mode current. Thus, lower inductor losses and, as a result, lower inverter losses can be predicted.

5.8. CII Topology Power Losses Comparison

The experimentally measured power losses are presented for just the coupled inductor and also the combined losses of the inverter and inductor. Loss comparisons curves are compared when using different interleaved switching algorithms (DSVPWM, DPWM1 and SVPWM). The DSVPWM method with the combination of interleaved DSVPWM1 for m_a>0.5 and interleaved DSVPWM3 for m_a<0.5 is chosen as a reference for loss comparison with the pervious interleaved PWM methods. The DSVPWM3 for m_a<0.5 is chosen to emphasis that the DSVPWM strategy with no optimal scheme for a unity power factor load is still capable of improving performance by lowering inductor losses. Two same-sized cores but with different laminations, 4mil and 14.5mil, were used in the coupled inductor. The tests were carried out with a 3-phase RL (variable R, 1mH) load under two different conditions:

(1) The load resistance is maintained at 15.66Ω, but the modulation indices change (Figure 5-87 and Figure 5-89).

(2) The modulation depth is maintained at m_a=1.0, but the load current changes (Figure 5-88 and Figure 5-90).

5.8.1. CII Topology Inverter Power Losses Comparison

The inverter total power loss was obtained by measuring the inverter's input DC power and subtracting the inverter's three-phase output power (obtained by measuring the three-phase voltages and currents). The CII topology's total power losses are depicted as a function of m_a in Figure 5-87. For the same modulation methods but different core laminations, the total power loss when using the 14.5mil laminations core is higher than when using the 4 mil laminations, the difference being caused by the increase of high-frequency losses in the thicker 14.5mil laminations. The power loss produced by the DSVPWM method is significantly lower than that produced by the SPWM and DPWM1 methods at each m_a. This finding can be explained by the lower high-frequency current and core flux ripple produced by the DSVPWM scheme, allowing for lower inductor losses (both winding and core losses). The "shape" of the curves in Figure 5-87 and Figure 5-89 can be attributed to the core high-frequency flux losses' dependence on m_a [126, 127], which tends to peak in the mid range of m_a and to decrease as m_a drops to 0 or increases to 1.0.

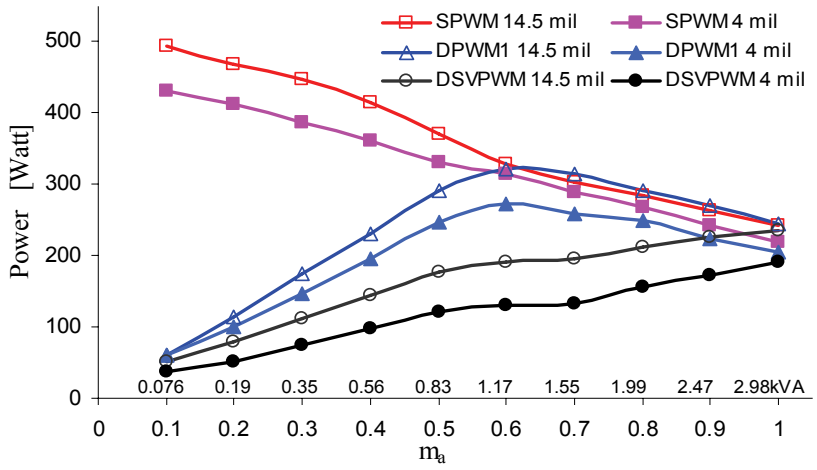


Figure 5-87: Experimental CII total losses: SPWM, DPWM1 and DSVPWM schemes with 4mil and 14.5mil laminations cores (R = 15.66Ω)

In Figure 5-88, the CII topology's total power losses are demonstrated over a range of rms load currents using a constant m_a of 1.0 with the 4mil laminations core. The differences in the power loss curves are almost the same for each m_a. The results indicate that the CII power losses in the DSVPWM and DPWM1 schemes are lower than that in the SPWM scheme, with the interleaved DSVPWM giving the lowest total power losses. For both sets of curves in Figure 5-87 and Figure 5-88, the inductor winding copper

losses increase with both m_a and the rms output current. Since m_a is constant in Figure 5-88, the core flux losses are fairly constant, and the intersection of the curves with the Y axis is a good estimate of the differences in the couple inductor core losses produced by the various modulations schemes at m_a = 1.0. The graph's linearity in Figure 5-88 indicates that the switching loss curve is in the opposite direction of the coupled inductor loss curve (which is mainly copper losses for a constant m_a). Thus, the resulting total losses become a linear line.

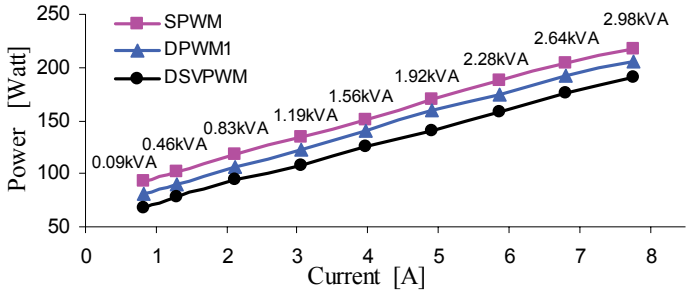


Figure 5-88: Experimental CII total losses for various load currents with SPWM and DPWM1 and DSVPWM (4 mil laminations and m_a = 1.0)

5.8.2. Coupled Inductor Power Losses Comparison

The coupled inductor power losses are averaged over a few switching cycles and calculated directly by measuring the voltage across each coil and the corresponding winding current. The corresponding coupled inductors power losses (for the CII topology's power losses shown in Figure 5-87) are demonstrated as a function of m_a in Figure 5-89.

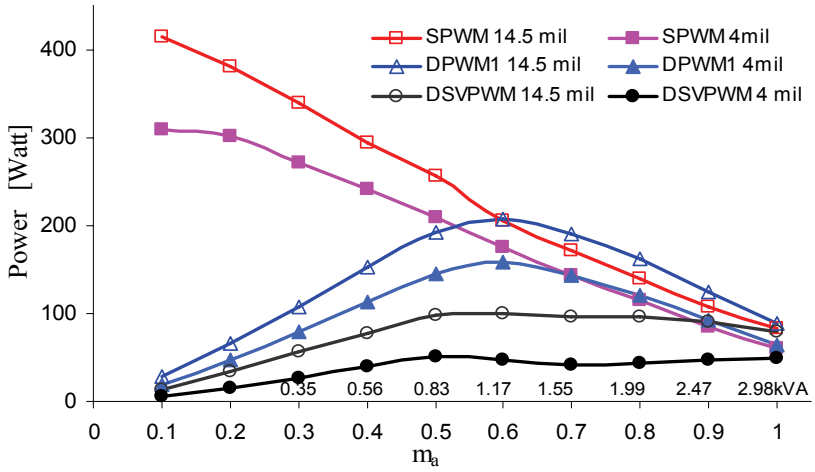


Figure 5-89: Experimental coupled inductor losses: SPWM, DPWM1 and DSVPWM with 4mil and 14.5mil laminations cores (R = 15.66Ω)

At low-modulation depths, the coupled inductor losses are decreased with DSVPWM and DPWM1. For two reasons: the core-loss dependence on m_a and the load current value decreasing with a lower m_a. In contrast, the SPWM method produces very large power losses at low modulation depths because this method produces very high winding current ripple and core flux losses. For the same laminations at each m_a, the coupled inductor losses generated by DSVPWM are the lowest. When m_a is higher than about 0.6, the coupled inductor losses produced by the SPWM scheme are lower than those produced by the DPWM1 scheme. In Figure 5-87, even when m_a is smaller than 0.9, the DSVPWM power losses with 14.5mil laminations core are lower than those of the DPWM1 and SPWM schemes with a 4mil laminations core. Therefore, a better performance is obtained with DSVPWM even when using larger laminations.

The coupled inductors power losses for the CII topology are demonstrated at various rms load currents in Figure 5-90 when using m_a=1.0 and 4 mil laminations. In Figure 5-90, the curves can be attributed to the copper losses dependent on the load current; the differences between the three power losses are almost constant for each m_a and are due mainly to core flux losses. The results also indicate that the coupled inductor power losses in the DSVPWM and DPWM1 schemes are about 10watt and 4watt lower than that in the SPWM scheme, with the DSVPWM scheme giving the lowest power losses.

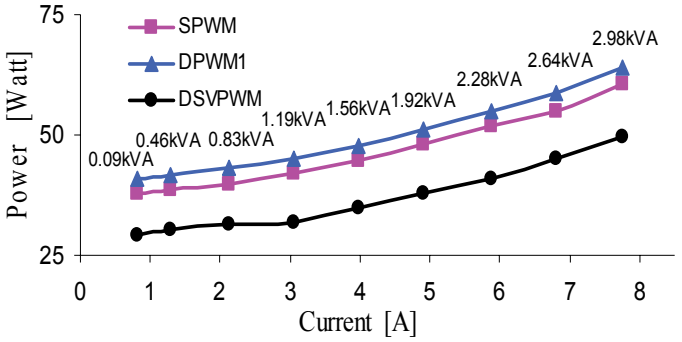


Figure 5-90: Experimental coupled inductor losses for various load currents with SPWM and DPWM1 and DSVPWM (4 mil laminations and m_a = 1.0)

The percentage increase in the coupled inductor power losses as a result of using DPWM1 and SPWM rather than the DSVPWM method is illustrated in Figure 5-91. The percentage increase in losses for DPWM1 and SPWM is well over 20% at all output current levels.

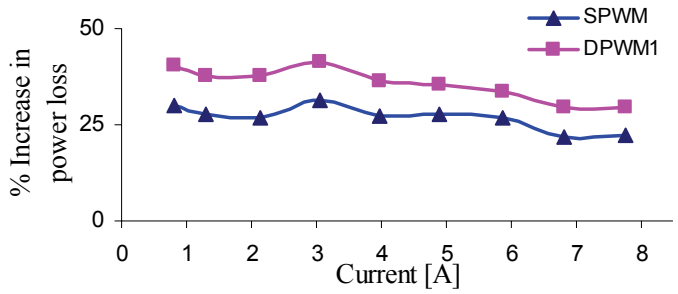


Figure 5-91: Experimental percentage increase in coupled inductor power losses with SPWM and DPWM1 schemes compared with DSVPWM scheme at different load currents (m_a = 1.0, 4 mil laminations core)

5.8.3. Coupled Inductor rms Currents Comparison

The rms winding currents (including the dc and AC components of the winding current) for different load currents with the SPWM, DPWM1 and DSVPWM schemes are compared in Figure 5-92 by using 4 mil laminations and m_a set to 1.0. DPWM1 and SPWM produce the same approximate winding rms currents whereas DSVPWM produces the lowest rms winding currents at all load currents.

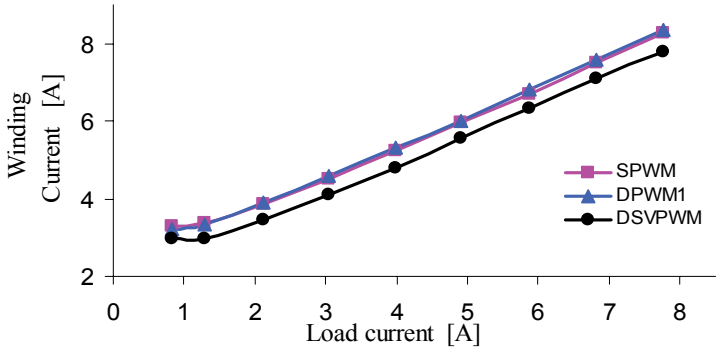


Figure 5-92: Experimental winding current for different load currents with SPWM, DPWM1 and DSVPWM schemes (m_a = 1.0, 4mil laminations)

Figure 5-93 compares the rms winding current as a function of m_a when using the SPWM, DPWM1 and DSVPWM schemes with 4mil laminations and R=15.66 Ω. The rms winding currents with the SPWM and DPWM1 methods are the same for m_a >0.6, but as m_a decreases, the SPWM winding current increases in contrast to that with DPWM1 where the rms winding current decreases. The high rms currents for SPWM at low-modulation depths are caused by the presence of very large high frequency currents. These are produced by the selection of low-inductance switching states by SPWM at low-modulation depths. The better selection of high-inductance states at all modulation depths produces much lower rms currents for the DSVPWM than those of the other two schemes.

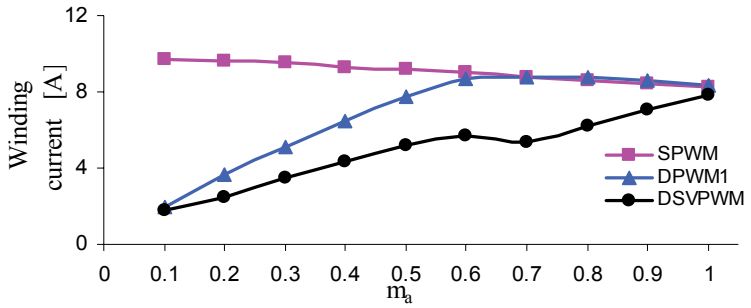


Figure 5-93: Experimental winding current as function of m_a with SPWM, DPWM1 and DSVPWM schemes (R = 15.66Ω, 4mil laminations)

5.9. CII Topology Performance as a PMSM Drive

In this section, the operation of the CII topology as a viable variable frequency drive is investigated by using several experimental tests under various operating conditions. The experimental tests are used mainly to explore the dynamic current responses for the CII topology. To illustrate the effectiveness of this approach, experimental tests are performed on a 3.5kW Permanent Magnet Synchronous Machine (PMSM), with the parameters summarized in Table 5-3. The PMSM is chosen to minimize the filtering effect of machine winding inductance on the performance of the inverter and also because fast transient responses can be obtained with a very small PMSM winding inductance (3.3 mH). The PMSM control algorithm is given in Appendix A.

Table 5-3: PMSM Specifications

Line voltage (V)	240	Torque constant K_t	0.71
Nominal current (A)	17	Voltage constant K_E	86
Maximum power (W)	3500	Winding resistance (Ω)	0.51
Rated speed (rpm)	2571	Winding inductance (mH)	3.30
Number of poles	8	Rotor inertia (Kgm^2)	0.01

5.9.1. PMSM Closed Loop Power Control Performance

The operation of the CII topology with a PMSM closed loop power control is investigated. Figure 5-94 through Figure 5-98 show the currents, voltage and speed responses of the PMSM to a step change in power. At time 0.2s, the reference output power command is changed from 250 watt to 1000 watt. Figure 5-94 and Figure 5-95 demonstrate the phase A PMSM current and the upper winding current during the transient respectively. The proposed drive structure can quickly respond to this power change. The PMSM fundamental phase rms current changes from 3.35A to 6.41A in the steady state. In addition, the operation of CII topology with the proposed DSVPWM

scheme in the continuous mode can be observed since the winding current is always greater than zero in Figure 5-95. Figure 5-96 demonstrates the line-line voltage applied to the PMSM machine. The fundamental line-line voltage changes from 44.2 rms to 91.3 rms in the steady state. Figure 5-97 and Figure 5-98 show the actual quadrature current i_q (with i_d=0) and the speed of the PMSM, respectively. The PMSM accelerates form 722 rpm to 1493rpm. The speed response follows the torque command (which is proportional to i_q).

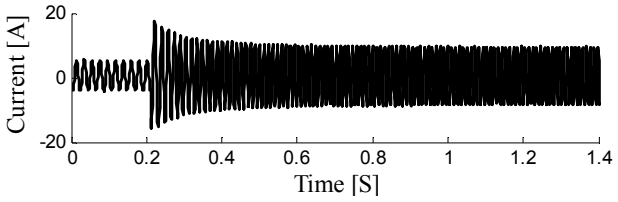


Figure 5-94: Experimental PMSM phase A current with PMSM closed loop power control

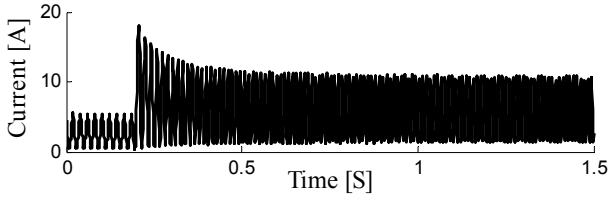


Figure 5-95: Experimental coupled inductor upper winding current with PMSM closed loop power control

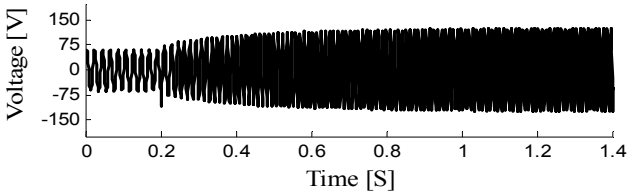


Figure 5-96: Experimental PMSM line-line voltage with PMSM closed loop power control

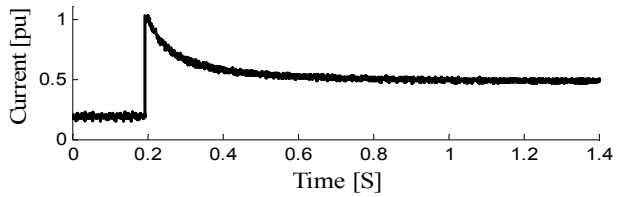


Figure 5-97: Experimental PMSM quadrature current (iq) with PMSM closed loop power control

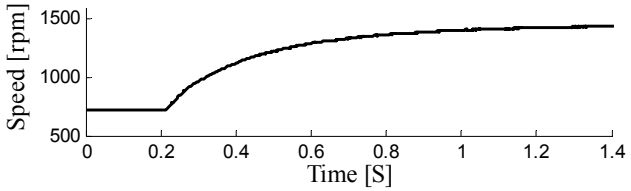


Figure 5-98: Experimental PMSM speed with PMSM closed loop power control

5.9.2. PMSM Closed Loop Speed Control Performance

A simple closed loop speed control operation of the PMSM with CII topology is implemented, and the experimental results are presented in Figure 5-99 through Figure 5-103. The reference speed at 0.2s is step-changed from 250 rpm to 1500 rpm at the no load condition. The transient response of the phase A upper winding and the phase A currents (see Figure 5-99 and Figure 5-100, respectively) illustrates that the output AC current can be changed rapidly in spite of the large inductance value of the coupled inductor. Figure 5-100 illustrates how the upper winding current can change in magnitude rapidly during a transient, containing both a fundamental AC and a corresponding dc offset component. An interesting aspect of this transient waveform is that the winding current always stays positive due to the unipolar operation of the asymmetrical half bridge used in each phase of the inverter. Figure 5-101 shows how the common mode winding current (dc offset) can change rapidly upwards and downwards as the output load changes. Figure 5-100 demonstrates the transient response of the line-line voltage applied to the PMSM machine. The fundamental line-line voltage changes from 15 rms to 89.3 rms in the steady state. Figure 5-103 illustrates the actual speed of the PMSM changed from 250rpm to 1500rpm during 0.25s.

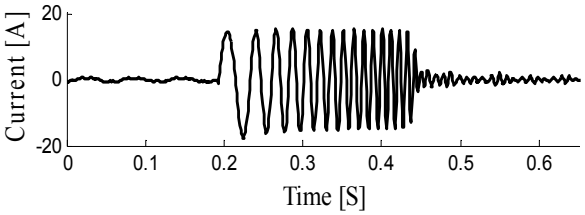


Figure 5-99: Experimental PMSM phase A current with PMSM closed loop speed control

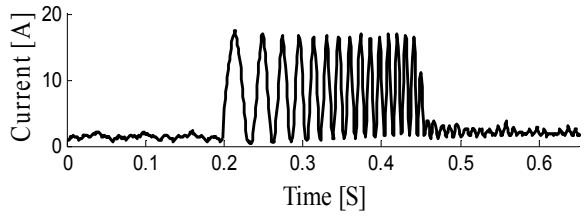


Figure 5-100: Experimental Coupled inductor upper winding current with PMSM closed loop speed control

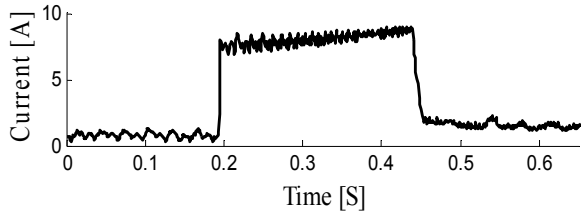


Figure 5-101: Experimental Phase A Common mode winding current with PMSM closed loop speed control

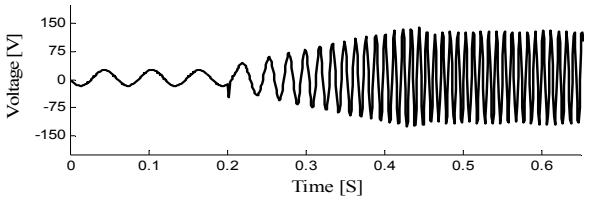


Figure 5-102: Experimental PMSM line to line Voltage with PMSM closed loop speed control

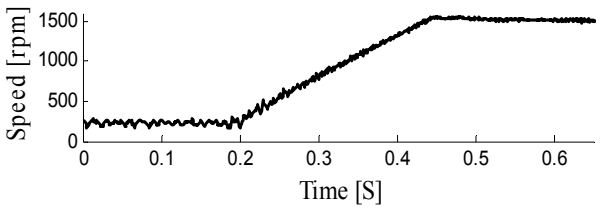


Figure 5-103: Experimental PMSM Speed with PMSM closed loop speed control

The upper winding, common mode dc, and phase A currents are shown in Figure 5-104 at a 1500 rpm steady state operating condition. Figure 5-105 shows the line-line PWM voltage applied to the PMSM. The experimental spectra of the phase-A current and the upper winding current, and the output line-line voltage of the PMSM at 1500 rpm, are demonstrated in Figure 5-106, Figure 5-107, and Figure 5-108, respectively. Figure 5-106 and Figure 5-108 validate that the DSVPWM produces a PWM voltage and output current with a frequency double the effective switching frequency. In Figure 5-106, the phase A current THD is lower than 2% when the rms current is about 10A.

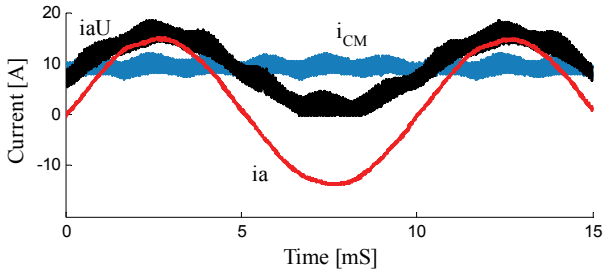


Figure 5-104: Experimental PMSM: upper winding, common mode dc and phase A currents with PMSM closed loop speed control at 1500 rpm (m_a=0.45, f_c= 15 kHz)

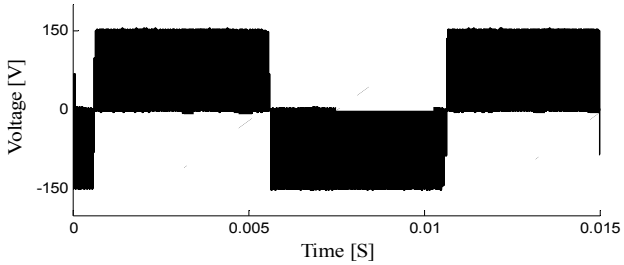


Figure 5-105: Experimental PMSM: PWM line to line Voltage with PMSM closed loop speed control at 1500 rpm (m_a=0.45, f_c= 15 kHz)

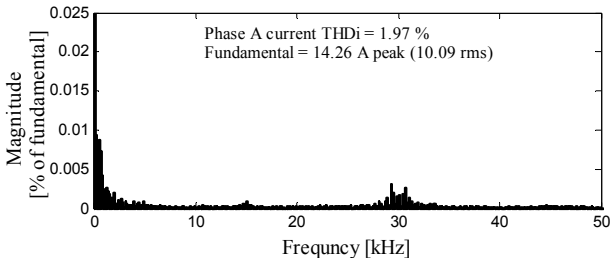


Figure 5-106: Experimental DSVPWM phase A current harmonic spectrum with PMSM at 1500 rpm (m_a=0.45, f_c= 15 kHz)

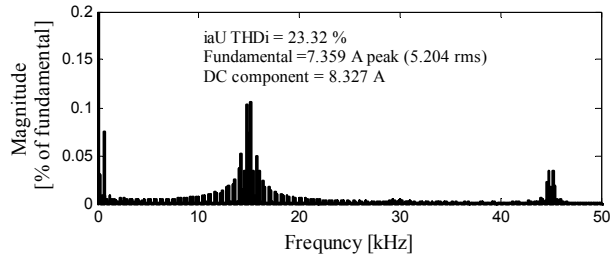


Figure 5-107: Experimental DSVPWM phase A upper winding harmonic spectrum with PMSM at 1500 rpm (m_a=0.45, f_c= 15 kHz)

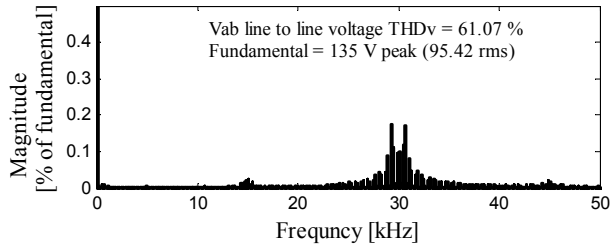


Figure 5-108: Experimental DSVPWM Vab line-line voltage harmonic spectrum with PMSM at 1500 rpm (m_a=0.45, f_c= 15 kHz)

The winding current harmonics frequencies are the odd multiple of the switching frequency. The half output current rms (about 5A rms) flows from the upper winding as shown in Figure 5-107.

5.10. Chapter Summary

The performance of the various modulation schemes developed in Chapter 4 for the CII topology are compared in this chapter by using simulation results and are validated by using experimental tests. The results demonstrate that interleaved PWM switching of the upper and lower switches in each inverter leg is an effective switching scheme for this topology. Interleaved techniques can be used to lower the size of the output AC filter and to lower the high-frequency harmonics by increasing the frequency of the output PWM waveforms above the switching frequency. However, the initial carrier-based interleaved

schemes, SPWM and DPWM1, even with high-quality output signals, have an overall poorer CII performance due to the coupled inductor losses. These modulation schemes offer no freedom to select the more desirable switching states present in each switching cycle. As a result, switching states with a low-effective winding inductance are selected, and these produce a large high-frequency current ripple in the inductor windings. This result generates high winding and core losses, with a high-frequency leakage flux produced outside the magnetic core.

As an alternative, original and optimal multilevel SVPWM schemes are developed. With the elimination of some of the low-effective inductance states in the original SVPWM and all the low-inductance states in the improved SVPWM, the multi-level SVPWMs are shown to produce lower harmonic winding currents. However, this improvement in winding current harmonic content is obtained at the expense of output current quality when compared to that of the interleaved schemes. The low output current quality is obtained because of having the lower effective output switching frequency compared to that of the interleaved methods. The effective switching frequencies of the original SVPWM and improved SVPWM methods are ½ of the switching frequency and the switching frequency, respectively.

To overcome the issues related to previous PWM strategies, an interleaved discontinuous SVPWM (DSVPWM) is developed, which combined the positive effects of the interleaved carrier-based PWMs and the SVPWMs strategies: (1) generating high-quality output with the interleaved switching and (2) minimizing the winding current ripple by using the SVPWM technique. The interleaved DSVPWM minimizes the winding current ripple by selecting the high-inductance switching states and the optimal sequence, and limiting the current ramp interval by increasing the effective switching frequency and the distributing current rises and falls during a single switching frequency.

The interleaved DSVPWM, categorized as DSVPWM0, DSVPWM1 and DSVPWM3. DSVPWM1 schemes with a 60º discontinuous period located around the peak positive and negative cycles, is also demonstrated to lower the high-frequency current ripple compared to all the PWM schemes while also reducing the switching losses. The lower winding current ripple lowers the copper losses; the lower common mode current ripple lowers the flux ripple and, thus, the core losses. Therefore, minimizing the current ripple minimizes the coupled inductor losses. The DSVPWM1 method produces minimum losses in coupled inductors and also reduces the switching losses in the inverter. The

overall performance of the coupled inductor inverter, as validated by experimental loss measurements, is improved significantly. This benefit can lead to lowering the required core size for the split-wound inductor structure and to reducing the inductor cost.

The effective inductance in each leg depends on the coupled inductor winding configuration, but the common mode current ripple depends on the effective inductance (value) and the PWM switching frequency and the PWM switching technique (the switching sequence and the location of the discontinuous period). However, the output current ripple is dependent on the modulation method and coupled inductor leakage inductance.

Finally, the multi-level CII topology is shown to have potential for motor drive applications since the coupled inductor with the interleaved DSVPWM has a good performance over all m_a ranges. The laboratory closed loop power and speed control results validated the effectiveness of the approach.

Chapter 6

Conclusions and Recommendations for Future Research

This thesis explores the operation of coupled inductor inverters with various PWM modulation strategies. The operation of CII topology with previous interleaved carrier-based PWM methods is almost impractical over a wide m_a range, especially at low modulation depths due to excessive inductor losses and high EMI noises. By using new perspectives of the fundamental principles of the multilevel Space Vector PWM, new SVPWM modulation techniques are developed for the coupled inductor inverter in this thesis. Compared to the previously published PWM schemes, the interleaved Discontinuous SVPWM method minimizes the high frequency common mode winding current ripple by selecting the effective high inductance switching states and using the interleaved switching sequences.

Comprehensive comparisons of the current ripple, THD, and the coupled inductor losses are investigated for different types of PWM schemes by using both simulations results and experimental measurements. Experimental studies are focused on the evaluation of the power loss in coupled inductors with various interleaved PWM schemes, since power loss is a key factor in machine drives that determines the drive efficiency and performance. The coupled inductor losses associated to the common mode current ripple and the EMI noises caused by the high frequency leakage flux outside the inductor core are significantly reduced. While the multilevel DSVPWM schemes increases the complexity of the implementation compared to that of the carrier-based PWM schemes, the flexibility in the design of selecting switching states and sequences with the DSVPWM schemes improves the performance of the inverter over full modulation depths and provides an optimal operation for the CII topology. Also, the proposed interleaved DSVPWM technique can be applied in designing future modulation schemes for converter topologies with split-wound coupled inductors.

Contributions made by this thesis work can be summarized as follows:

- A multilevel space vector PWM algorithm is presented with the following characteristics.
    a. Generates multi-level output voltage with a PWM switching frequency

double the effective switching frequency.

b. Balances the common mode dc voltage (current) in a 3-limb inductor core for the CII continuous mode of operation.
c. Avoids low effective inductance switching states.
d. Selects a switching sequence that minimizes current ripple in both the common mode inductor winding current and output current.
e. Generates symmetrical voltages without even harmonics.
f. Allows for high fundamental frequency operation.

- Improves the performance of the CII topology over a wide m_a range by:
  a. Minimizing the high frequency winding current and output current ripples and rms winding currents.
  b. Alleviating the EMI noises by maintaining the high frequency flux inside the inductor core rather than the outside the core.
  c. Lowering the inductor losses including copper and core losses, and inverter losses (both conduction and switching losses).
- Experimental verification of
  a. Various space vector and carrier-based PWM strategies for the CII topology.
  b. Performance improvement by measuring the high frequency current ripple, rms current and coupled inductor and inverter loss measurements.
  c. Closed loop operation of the CII topology as a potential variable frequency drive.

6.1. Summary

The advantages of multilevel converters over a conventional two-level converter are explained. The attractive features of multilevel converters in general can be briefly summarized as follows: high power quality (due to the multiplying effect of the number of voltage levels), good electro-magnetic compatibility, low switching losses, and high voltage capability. The main disadvantages of multilevel structures are that they require more switches than the 2-level inverters, and the multilevel topologies have greater control complexity. The weaknesses and strengths of the major multilevel converter topologies such as the cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped) are discussed. In

addition, the applications of multilevel converters are explored for renewable energy systems, flywheel energy storage systems, and even, in the low voltage field, motor drive, due to the high quality of the AC output. A literature review of the various modulation techniques and PWM control methods developed for multilevel converters such as carrier-based PWM, selective harmonic elimination, and multilevel SVPWM is discussed (see Chapter 2).

The fundamental operation of the multi-level voltage source inverter using split-wound coupled inductors is investigated in Chapter 3. The coupled inductors are modeled with the magnetizing and the leakage inductances by using a simplified equivalent transformer model. The magnetizing inductance varies with different winding configurations (switching states), but the leakage inductance is maintained for split-wound coupled inductors placed in a three-limb core. As the windings are tightly coupled on a single leg, the magnetizing fluxes are cancelled, and only the leakage inductance is seen by the phase current. However, the magnetizing inductance is seen only by the common mode current, the average of the upper and lower winding currents. As one of the key parameters in this inverter, the common mode current value defines the continuous or discontinuous operation mode of the inverter. Control of the DC common mode current is determined to be one of the important factors in the inverter's performance. The continuous mode of operation resulted in producing symmetrical sinusoidal winding currents and a defined multilevel output voltage with low harmonic content. In discontinuous conduction, the centre-tap voltage is undefined since the inverter terminal is not connected to the input DC supply, resulting in high harmonic voltage and winding current distortion. The possible CII switching states are investigated by examining the various 3-phase coupled inductor winding configurations. The impacts of the switching states in each leg on the common mode current are studied.

Winding and output current ripples are obtained from the inductance requirement of the coupled inductor. The DC flux is removed in the three-limb core structure, and only the rms of the AC high-frequency common mode current ripple produced an AC ripple flux in the core. Since the ripple magnitude of the winding current is linked to the AC ripple flux, the PWM switching with the ability to minimize the AC current ripple in the windings lowers the core losses and, to a lesser extent, reduces the copper losses due to the lower rms current, allowing for a smaller core size.

The high-performance operation of the multi-level coupled inductor inverter topology

is dependent on the selection of an optimal modulation strategy. The optimal modulation strategy improves the inverter performance by lowering the total inverter losses while providing high-quality outputs. The successful operation of the CII topology over the full modulation range relies on selecting switching states and sequences where (1) the coupled inductor presents a low winding current ripple, and (2) the inverter output waveforms has a low harmonic content. In addition, it is found that modulation schemes must be carefully designed to balance the common mode winding current (voltage) over one or two switching cycles for the continuous mode of operation.

The principles of two commonly used techniques, the initial interleaved carrier-based PWM and the newly developed multilevel space vector PWM modulation schemes, to generate PWM waveforms for the CII topology are described. The basic operation of the CII topology with these schemes and their evolutions, advantages, limitations, and methods of waveform generation are investigated (see Chapter 4).

The evolution of multilevel SVPWM schemes is based on the following findings obtained through the development processes. The value of the effective inductance in each leg depends on the coupled inductor winding configuration. The winding current ripple depends on the selection of switching states with a high effective inductance value, the (effective winding) PWM switching frequency, and the PWM switching technique (i.e., the switching sequence or the order of space voltage vectors in a switching period and the location of the discontinuous period). The output current ripple is dependent on only the PWM modulation method (i.e., the effective output frequency and the switching sequence) and the coupled inductor leakage inductance. The position of the PWM terminal voltage within the half switching cycle affects the output current's harmonic performance.

The performance of the CII topology with the interleaved carrier-based PWM and SVPWM modulation strategies is investigated by using the simulation results and verified by experimental tests using a RL load. The winding current ripple, the output voltage THD, and the output current THD are of special interest in the analysis, and a strategy for comparing the PWM schemes is developed. The results show the operation of the topology with the different modulation methods. In the following paragraphs, the comparison between modulation schemes is given based on the principles described in Chapter 4 and the performance results obtained in Chapter 5.

The interleaved carrier-based schemes, SPWM and DPWM1, using interleaved PWM

switching with simultaneously turning on and off of the upper and the lower switches in each inverter leg are found to be an effective switching technique for this topology by doubling the effective switching frequency of the output PWM waveforms above the actual switching frequency. While intrinsically balancing the common mode voltage (current), the interleaved PWM technique can lower the size of the output AC filter and the high-frequency output harmonics by increasing the effective output switching frequency. Compared to SPWM, DPWM1 generates multilevel output voltages, lowers switching losses, and reduces the common mode current ripple due to the effects of coupling between the inverter legs on the common mode current ripple by clamping one of the inverter legs to P or N points of the DC bus. The main disadvantage of the interleaved carrier-based PWM schemes is that the switching states in each switching cycle are chosen by the reference waveform. The uncontrolled switching states in the carrier-based PWM methods produces a large high-frequency current ripple in the inductor windings, resulting in high coupled inductor losses. Thus, even though the output voltage and current waveforms has low harmonic content, the overall performance of the CII was poor. This issue becomes more pronounced when modulation depth is low. This problem can be overcome either by oversizing the coupled inductor to provide sufficient effective inductance in all switching cases or by using a modulation scheme which eliminates the switching states generating the high current ripples. The first solution is achieved by adding more turns to the coupled inductor, which increase the size of the core and the amount of copper used. Therefore, the cost of the inverter increases. In this thesis, the second solution is performed by introducing the multilevel SVPWM algorithm for the CII topology.

By using the multilevel SVPWM technique, original SVPWM, improved SVPWM and interleaved discontinuous DSVPWM strategies are developed. The main benefits of SVPWM are found to be the precise identification of pulse placement and the choices over redundant switching states for each voltage vector. When efficiently used, this approach optimizes the PWM modulation scheme, resulting in the high-performance operation of the CII topology. Balancing the common mode dc current, the multi-level SVPWM schemes are found to be capable of minimizing the winding current ripple by using optimal switching states (i.e., the high-inductance switching states) and the switching sequences. The output current ripple is influenced only by the switching sequences and the effective switching frequency, but not the switching states. Thus, the

order of voltage vectors in each sequence during a switching cycle could be arranged to minimize the winding current ripple and output current ripple.

Compared to the original SVPWM, the improved SVPWM eliminates all the low-inductance switching states and increases the effective output switching frequency from ½ switching frequency in the original SVPWM to the actual switching frequency in the improved SVPWM. In comparison with the interleaved methods, both these schemes balanced the common mode voltage (current) in the two switching cycles. These methods are originally used to eliminate the low-inductance switching states in the CII in order to significantly lower the high-frequency winding current ripple (especially at low modulation depths) relative to that produced by the interleaved carrier-based PWMs. However, although the quality of the output voltage is comparable with that of the interleaved DPWM1, the output current quality is lowered since the effective output switching frequency is half of that of the interleaved DPWM1 scheme.

A multi-level interleaved discontinuous space vector PWM (DSVPWM) strategy is developed to overcome the problems related to the previous PWM strategies while providing both high-quality outputs (by using the interleaved SVPWM technique) and a high-performance inverter (by lowering the coupled inductor losses).

Minimizing the current ripple, DSVPWM offers superior performance and features over the previous modulation schemes. The interleaved DSVPWM minimizes the winding current ripple by selecting the high-inductance switching states and the optimal interleaved sequence. In the interleaved DSVPWM, most switching states with a low inductance are omitted. The effective output switching frequency is increased by the interleaved DSVPWM in comparison with the original and improved SVPWMs. In addition, the interleaved DSVPWM scheme has the ability to reduce the switching losses in the inverter, allowing for higher switching frequencies.

Based on the interleaved DSVPWM technique, DSVPWM0, DSVPWM1 and DSVPWM3 schemes are derived. The DSVPWM1 demonstrates the better inverter performance by additionally lowering the winding current ripple and switching losses when a 60º discontinuous period occurred at the positive and negative voltage peaks. Overall, the DSVPWM1 method demonstrates to be a good candidate to minimize the losses in the coupled inductors by significantly lowering the winding current ripple and also the switching losses in the inverter using a purely resistive load.

In the continuation of Chapter 5, a series of comparative studies of inverter loss and

coupled inductor losses are performed with different interleaved PWM schemes, load conditions, and modulation indices. In addition, a study of the losses of the coupled inductor inverter with the interleaved PWM schemes is carried out. The superiority of DSVPWM is validated by the experimental loss measurements. The DSVPWM significantly lowers the couple inductor losses over a wide m_a operating range when compared to the interleaved carrier-based PWM methods. Thus, the overall performance of the coupled inductor inverter is improved significantly by using the interleaved DSVPWM strategy. This benefit can lead to lowering the required core size for the split-wound inductor structure and, thereby, to reducing the inductor cost as well. In addition, the reduction of the inverter loss caused by DSVPWM not only increases the system's efficiency, but also simplifies the thermal management and therefore reduces the size and the weight of the inverter as well.

The DSVPWM modulation scheme is introduced as a modulation scheme that could be used for drive applications. A typical machine drive system based on a 3.5 kW a PMSM together with the loading system is developed and presented in Chapter 5. The machine controller is designed and together with the DSVPWM scheme is developed by using on a TI DSP controller. Then, the closed-loop performance of the CII topology using DSVPWM is completed with a series of experimental tests using a PMSM. The closed-loop speed and power control are implemented with this drive topology. The results shows the fast transient responses of the coupled inductor inverter using the DSVPWM control while providing the high-quality outputs. The multilevel CII topology is shown to have the potential for motor drive applications since the coupled inductor with the interleaved DSVPWM had a good performance over the entire m_a range.

6.2. Recommendations for Future Research

Several topologies are available for selection as the inverter output stage of a 3-phase machine drive. The inverter topologies create various kinds of electromagnetic stress on electrical machines due to the PWM switching voltage waveforms [128]. Moreover, the additional losses created by the current and voltage supply harmonics at multiples of the switching frequency should be considered in the machine design stage to avoid overheating. For example, in the flywheel energy storage systems, since an electrical machine operates in a vacuum system, an increase of just a few degrees in the rotor temperature due to harmonics losses can cause catastrophic failure in the system [129].

Based on the different loss measurement methods, many studies have been carried out to estimate the additional loss caused by the non-sinusoidal supply of PWM-fed inverters [130-132]. Future work could study the machine losses resulting from the use of the CII topology with DSVPWM schemes. The comprehensive study of machine performance under this drive structure will provide sufficient information for the selection of inverters, according to different applications.

Previous research using conventional inverters with discontinuous PWM predicted that if the discontinuous period coincides with the maximum load current, the lowest switching losses and the best performance of the inverter will be obtained [24, 122-125]. However, in this thesis, similar to carrier-based discontinuous schemes in [133], variants of DSVPWM (i.e., DSVPWM0, DSVPWM1 and DSVPWM3) were developed for the CII structure. Among the DSVPWM schemes, the interleaved DSVPWM1 was shown to be capable of minimizing the inverter losses by lowering the coupled inductor losses and switching losses when the inverter was connected to a unity power factor load (in which the timing of the maximum load current and the load voltage peak coincides). This result raised the question of which DSVPWM strategy would minimize the inverter losses if the load angle changed. To answer this question, an adaptive DSVPWM scheme could be developed in future work to generate the required DSVPWM scheme according to the measured load angle, to achieve the minimum inverter loss.

In future work, by using Finite Element Analysis (FEA), the coupled inductor core losses could be predicted more accurately than they are being measured currently. The loss breakdown could be obtained for both core losses and copper losses. For different coupled inductor winding configurations, the effective inductance could be estimated, and the maximum current ripple could be determined. This information can be used to investigate the size of the inductor core and to limit the losses in the coupled inductor.

The work presented in this dissertation focused on relatively small machine drive systems where the PWM switching frequency can be as high as 20 kHz. However, the operation of the CII topology for larger machine drive systems has not been investigated. The impact of a lower inverter switching frequency may have a more pronounced effect than high switching frequencies on the coupled inductor losses by increasing the current ripple. The voltage harmonics may also affect on the switching frequency losses inside larger machines with lower inductance. Therefore, it is worth investigating whether DSVPWM would cause a significant rise in inverter and machine losses at high-power

applications. A loss breakdown analysis could be carried out to extract the conduction loss and the switching loss of the inverters. Insights into the inverter loss elements at varying modulation indices and varying switching frequencies could be obtained to provide more detail about inverter performance. A new switching algorithm may have to be developed to work at very low switching frequency ratios of the fundamental frequency while providing low harmonic content outputs.

The coupled inductor can be added to the final stage of multilevel topologies using more switches (e.g., 12 and 18) to further increase the number of the inverter's output voltage levels. In the future work, the multilevel interleaved DSVPWM technique proposed in this thesis could be developed to be applied to these new multilevel inverter topologies. The new topologies, by adding more voltage levels, would increase the complexity of the system. The common mode current balancing might be an issue, and extra feedback signals might be needed for common mode current control. The successful operation of these topologies might be achieved when the new PWM modulation algorithm was capable of instantly controlling the common mode current during each switching cycle.

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Appendix A

Permanent Magnet Synchronous Machines

The Permanent Magnet Synchronous Machines (PMSM) have been widely accepted in many industrial applications, especially in flywheel energy storage systems, motion controls, and propulsion of electric vehicles. The key features of PMSMs are compactness, efficiency, robustness, reliability, and shape adaptation to the work environment [134]. High-performance permanent magnet materials with high residual flux have enabled the development of PM machines with superior power density, torque-to-inertia ratio, and efficiency when compared to classical permanent magnet and induction machines. In addition to these advantages, the position of the rotor flux in a PMSM is precisely determined by knowing the rotor position; hence, the vector control of a PMSM is much simpler in comparison with that of an induction motor.

PMSM Vector Control Model

The PMSM model is presented in the d-q reference frame fixed to the rotor. By neglecting the hystersis and eddy current losses, the rotor magnet axis is aligned with the d axis in the modeling. The rotor position angle in respect to the stator phase A is θ_r in electrical radians. The stator voltage components are obtained as

$$V_{qs}^{r} = R_s i_{qs}^{r} + \omega_r \lambda_{ds}^{r} + \frac{d\lambda_{qs}^{r}}{dt}, \tag{1}$$

$$V_{ds}^{r} = R_s i_{ds}^{r} - \omega_r \lambda_{qs}^{r} + \frac{d\lambda_{ds}^{r}}{dt}, \tag{2}$$

where i^{r}_{ds} and i^{r}_{qs} are the stator current components, R_s is the stator resistance, and ω_r is the electrical angular speed of the rotor. The stator flux components are

$$\lambda_{ds}^{r} = L_d i_{ds}^{r} + \lambda_{af}, \tag{3}$$

$$\lambda_{qs}^{r} = L_q i_{qs}^{r}, \tag{4}$$

where L_d and L_q are the d- and q- axis inductances, respectively, and λ_{af} is the permanent magnet flux. The electromagnetic torque is given by

$$\tau_{e\_pmsm} = \frac{3}{2}\frac{\mathrm{P}}{2}\left[\lambda_{af} i_{qs}^{r} - (L_{ds} - L_{qs})\, i_{qs}^{r} i_{ds}^{r}\right], \tag{5}$$

where p is the number of poles. In equation (5), the PMSM torque can be controlled by

properly controlling the i^r_{ds} and i^r_{qs} currents. One simple PMSM control can be obtained by setting the d-axis current, i^r_{ds} , command to zero. Doing so results in a linear relationship between the machine torque and the i^r_{qs} current, as shown in equation (6):

$$\tau_e = \frac{3}{2}\frac{p}{2}\lambda_{af} i^r_{qs} . \tag{6}$$

The q-axis PMSM current control is similar to that in the armature current controlled permanent magnet dc machines, where the torque is proportional to the armature current magnitude. Therefore, this type of control has been widely used in many applications because of its control simplicity [134].

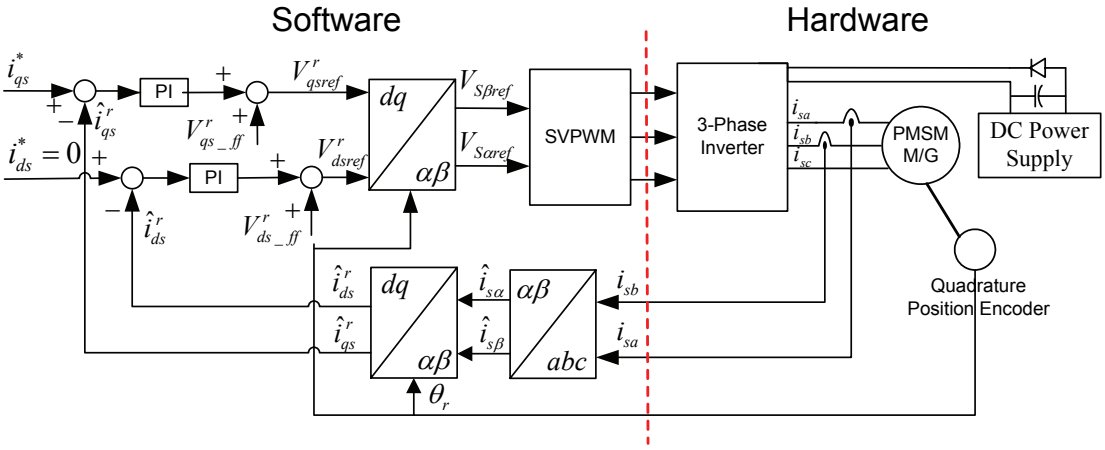

Figure 6-1: PMSM Control Block Diagram

Figure 6-1 illustrates the block diagram of the PMSM vector control scheme with a position sensor. The q-axis reference current is derived from the power control unit which is described in next section. As shown in Figure 6-1, by using the field orientation technique, the measured currents are transformed into d-q variables in a synchronous rotating rotor reference frame. Next, the PMSM currents are regulated to the commanded values by using a synchronous-frame proportional-integral (PI) regulator. The outputs of the PI current controllers are added to the feedforward terms $v^r_{ds\_ff}$, $v^r_{qs\_ff}$. The decoupling control terms are given by

$$v^r_{ds\_ff} = R_s i^{r*}_{ds} - L_s i^{r*}_{qs}\omega_r , \tag{7}$$

$$v^r_{qs\_ff} = R_s i^{r*}_{qs} + L_s i^{r*}_{ds}\omega_r + \lambda_{af}\omega_r . \tag{8}$$

The resultant outputs v^{r*}_{ds}, v^{r*}_{qs} are applied to the inverse Park transformation. The output of this block is the stator voltages in the orthogonal reference frame. These reference voltages are generated by the outputs of the SVPWM unit that drives the inverter. The

rotor position is measured by using an encoder position sensor.

PMSM Torque Control and Power Relationships

The relationship between the q-axis reference current (i^r_{qs}) and the inverter input dc current (i_{dc}) is derived based on the steady state power balance between the inverter input dc power and the inverter output AC power. The transferred power flow to the active inverter can be controlled if the PMSM torque is controlled [135]. If minor inverter losses are neglected, the inverter input power is equal to the PMSM input power:

$$P_{inv} = P_{in\_pmsm}, \tag{9}$$

where P_{inv} is the inverter input power, and $P_{in\text{-}pmsm}$ is the PMSM electrical input power. The inverter input power equation can also be obtained by

$$P_{inv} = v_{dc} i_{dc}. \tag{10}$$

By substituting equation (10) into (9), the PMSM input power is obtained as

$$P_{in\_pmsm} = v_{dc} i_{dc}. \tag{11}$$

The PMSM mechanical power is given by

$$P_{out\_mech} = \tau_{e\_pmsm} \omega_m. \tag{12}$$

By substituting the torque equation (6) into (12), the mechanical power equation is

$$P_{out\_mech} = \frac{3}{2}\frac{p}{2} \lambda_{af} i^r_{qs} \omega_m. \tag{13}$$

The PMSM electrical input power is equal to the mechanical power plus or minus (motoring or generating, respectively) any losses. If the typical machine losses (friction and windage) are neglected, the PMSM electrical input power is approximately equal to the mechanical shaft power, as shown in (14). Additionally, the eddy current and hysteresis losses are minimal in the permanent magnet machine used in this application.

$$P_{in\_pmsm} = P_{out\_mech} \tag{14}$$

Finally, the relationship between the PMSM current and the flywheel current can be derived by substituting equation (11) and (13) into (14) as in

$$i^{r^*}_{qs} = \frac{4 V_{dc} I^*_{dc}}{3 P \omega_m \lambda_{af}}. \tag{15}$$