FPGA-Based Real-Time Emulation of Power Electronic Systems With Detailed Representation of Device Characteristics

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***Abstract*—This paper presents a field-programmable gate array (FPGA)-based real-time digital simulator for power electronic apparatus based on a realistic device-level behavioral model. A three-level 12-pulse voltage source converter (VSC)-fed induction machine drive is implemented on the FPGA. The VSC model is computed at a fixed time step of 12.5 ns, allowing a realistic representation of insulated-gate bipolar transistor (IGBT) nonlinear switching characteristics and power losses. The simulator also models a squirrel-cage induction machine, a direct field-oriented control system, and a pulsewidth modulator to achieve the real-time simulation of the complete drive system. All the models have been implemented using very high speed integrated circuit hardware description language (VHDL). Real-time simulation results have been validated using the measured device-level IGBT characteristics.**

***Index Terms*—Field-programmable gate arrays (FPGAs), hardware-in-the-loop simulation, induction motor drives, pulsewidth-modulated power converters, real-time systems.**

I. Introduction

REAL-TIME digital simulators are finding wide ranging applications in the automotive, aerospace, electrical, and mechatronic industries. One of their most popular and demanding applications is the hardware-in-the-loop testing of digital controllers [1]–[6] for medium- to high-voltage ac motor drives. The modeling of insulated-gate bipolar transistor (IGBT)-based voltage source converter (VSC) remains the main challenge for real-time simulation. Specifically, the VSC model should realistically reflect the nonlinear device switching characteristics and times (often in the nanosecond range), switching and conduction losses, tailing current, and diode-reverse-recovery behavior of a realistic converter. Currently, the available real-time simulators have yet to reach such level of detail due to modeling and bandwidth limitations.

Commercial real-time digital simulators such as RTDS [7] and PC-cluster simulators based on RT-LAB [8]–[10] utilize parallel processing techniques to harness the computational power of DSPs or general-purpose processors to simulate complex systems. Although the power system modeling software used by these simulators has some commonality with off-line transient simulators such as PSCAD/EMTDC, MATLAB/SIMULINK, and EMTP, there have been significant innovations over the years to make real-time simulators accurate and efficient. In this context, the modeling of power electronic apparatus for real-time simulation needs more attention.

IGBT-based power electronic apparatus can be modeled using two types of offline [11] simulation tools: 1) system level and 2) device level. In the first category, the issues of interest are the network behavior of the power electronic apparatus and its impact on the power system, such as injected voltage and current harmonics, machine dynamics, and controller performance. All EMTP-type software and general mathematical modeling packages, such as MATLAB/SIMULINK, belong to this category. These tools utilize nodal or state-space solution of linear ordinary differential equations discretized using numerical integration rules such as the trapezoidal rule. Power electronic devices are often modeled in these tools using three types of behavioral [12] models: 1) ideal model; 2) switching function model; and 3) averaged model. All of these models have also been used for real-time simulation [8], [13], [14]. Several algorithms were developed to implement such models on DSP and PC-based real-time simulators such as those that involve network equivalents and automatic precalculation of converter states to minimize refactorization time [15] and those that provide noniterative tracking of multiple interstep switching events in real time [16]. System-level modeling is fairly fast; however, it is not able to reproduce the device nonlinear characteristics realistically.

In the second category of device-level modeling, the issues of interest are the switching transients, power losses, and thermal characteristics of the device. SABER and the family of SPICE software are examples of these types of tools, which employ simultaneous nonlinear system solution using numerical methods such as the Newton–Raphson or Katzenelson method [17]. Device-level modeling is very detailed; however, for motor drive simulation, it can be very time consuming. There are three types of device-level models [18] available for IGBT modeling: 1) analytical models; 2) behavioral models; and 3) numerical models. None of these device models have yet been used for real-time simulation mainly due to their computational complexity. The analytical models are based on semiconductor physics describing the carrier dynamics in the device.

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In this category, the two most popular models are the Hefner model [19] and the Kraus model [20], which have been implemented in SABER, as well as SPICE. Averaged models [21]–[23] that include device nonlinearities have also been proposed based on the bond graph technique to speed up long-term simulations. In the behavioral models, IGBT characteristics are fitted using different methods, and the resultant switching functions are then used in a simulator. This approach [24] has been used in an offline system-level simulation tool (EMTP) to model the device accurately. However, this model still requires very small time steps to be practically implemented in a real-time simulator based on conventional general-purpose processors or DSPs. Several other behavior models have also been proposed using the curve-fitting method to model the nonlinear device characteristics [25] and the Hammerstein configuration [26] whose parameters are obtained from physics-based models. Although these models are quite detailed, they are still difficult to implement in real time for multilevel converters due to their complexity and iterative solution.

A device-level real-time model implemented in a field-programmable gate array (FPGA), for a six-pulse IGBT-based VSC drive, is proposed in [27], which takes into account the precise switching times albeit based on linearized device characteristics. The numerical models utilize finite-element methods to model the carrier diffusion in the device, resulting in a very detailed, although computationally expensive, model.

This paper proposes a device-level behavioral model for the IGBT-based multilevel VSC suitable for real-time simulation using an FPGA. FPGAs are fast becoming the digital processors of choice for implementing computationally intensive algorithms in real time due to their high clock speed and inherently parallel hardwired architecture [27]–[31]. However, until recently, their application has been limited to the development of digital control algorithms and pulsewidth modulation (PWM) gating pattern generators, mainly due to lack of large device capacity, and intellectual property cores for the modeling of complex power electronic systems.

In this paper, we first obtain the switching characteristics of an IGBT module (CM50DU-24F from *Powerex*) from an experimental setup. The measured per-unit characteristics are then implemented in digital hardware on the ALTERA Stratix EP1S80F FPGA using Very high speed integrated circuit Hardware Description Language (VHDL). The resulting VSC model not only runs in real time but also realistically models the turn-on and turnoff nonlinear characteristics, switching and conduction losses, tailing current behavior, and diode reverse recovery. The FPGA-based real-time simulator models the complete ac drive, including a three-level 12-pulse VSC, a pulsewidth modulator, the induction machine, and the field-oriented controller. The nonlinear characteristics and losses obtained from the real-time simulator have been verified against the measured characteristics and losses from the experiment. The system-level real-time results have been verified against an offline simulation using MATLAB/SIMULINK.

The paper is structured as follows: Sections II and III explain the measurement of the IGBT characteristics and the modeling and FPGA implementation of the three-level VSC. Section IV presents the implementation of the induction machine model, the field-oriented control system, and the pulsewidth modulator. Sections V and VI show the real-time implementation details and results, respectively, followed by Section VII which gives the main conclusions of the paper.

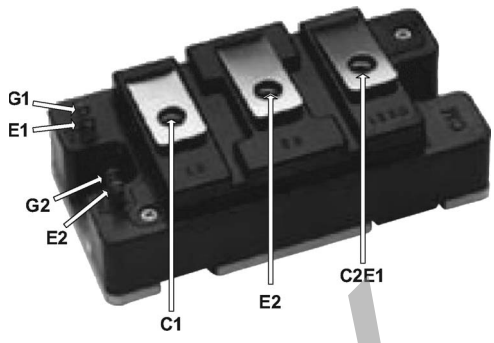

Fig. 1. CM50DU-24F IGBT module from *Powerex*.

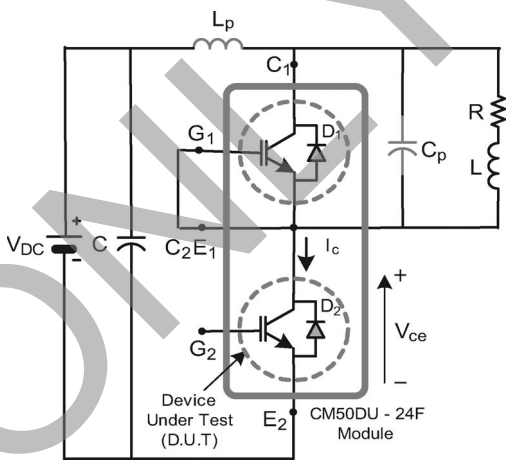

Fig. 2. Experimental test circuit to measure IGBT characteristics.

II. Experimental Measurement of IGBT Electrical Characteristics

A. IGBT and Diode Switching Characteristics

This section describes the measurement of the relevant electrical characteristics of the IGBT, which include the turn-on and turnoff switching characteristics, power losses, and the tailing current behavior. These measurements are based on hard switching of the IGBT. The measured IGBT characteristics are used in Section III to develop the three-level VSC model.

Fig. 1 shows a snapshot of the CM50DU-24F IGBT module from *Powerex*, used for the experimental setup. This module consists of two IGBTs and two antiparallel diodes rated at 1200 V and 50 A. The experimental test circuit shown in Fig. 2 utilized this module to measure the IGBT characteristics. The parasitic components measured from the diode (D_1) reverse-recovery characteristics are $L_p = 2.46$ μH and $C_p = 7.8$ nF. The inductor $L = 250$ mH dampens the oscillation between Lp and Cp during diode recovery, and the capacitor $C = 1800$ μF absorbs the energy from the diode recovery. The IGBT2 is the device under test (DUT) whose current was adjusted by selecting the load resistance from the variable resistors appropriately.

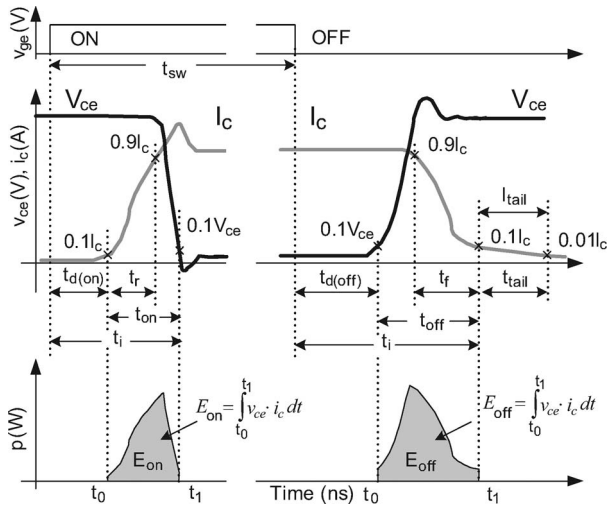

Fig. 3. Generic IGBT switching characteristics with switching times and loss definitions.

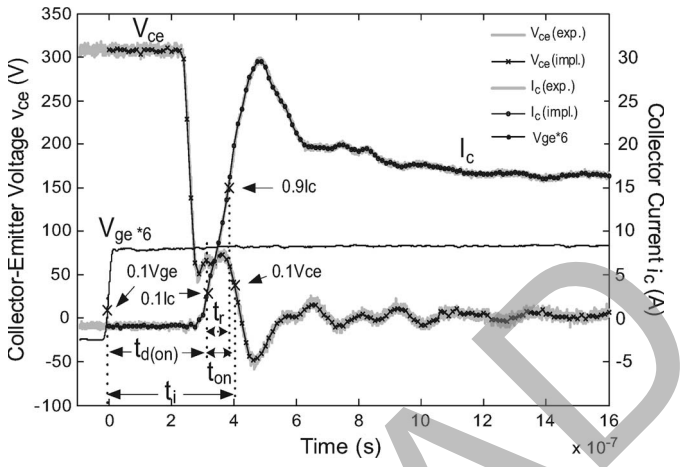

Fig. 4. Measured IGBT hard-switching turn-on transient waveforms.

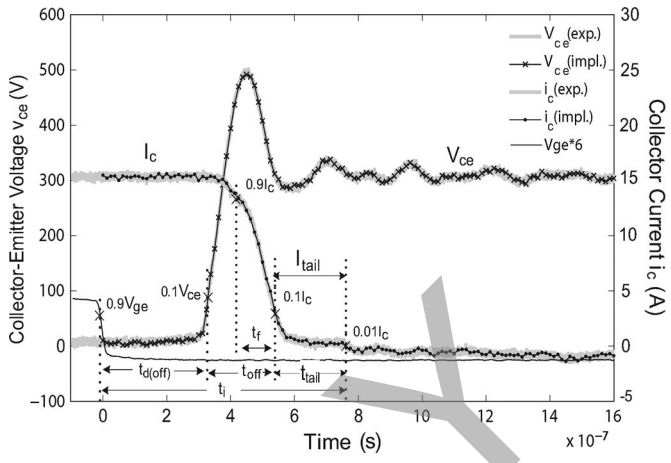

Fig. 5. Measured IGBT hard-switching turnoff transient waveforms.

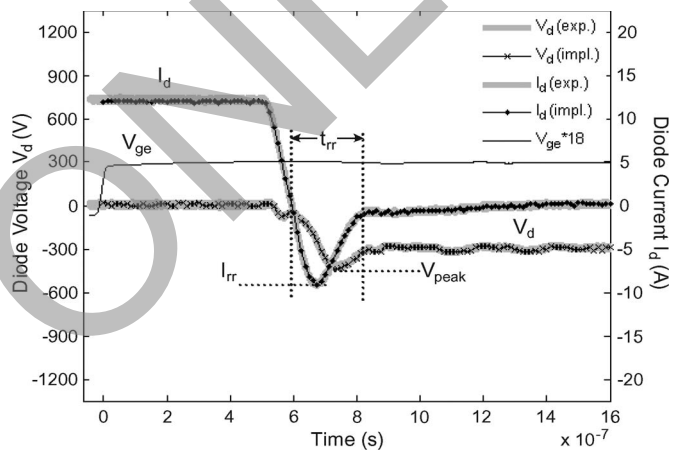

Fig. 6. Measured diode transient waveforms during IGBT hard-switching turn-on.

Fig. 3 shows the typical turn-on and turnoff $v_{ce} - i_c$ characteristics of an IGBT, along with the switching time definitions. It also shows the definitions of the power losses during switching. Fig. 4 shows the experimental data obtained for the turn-on transient. It can be seen that there is an initial delay $t_{d\,(\mathrm{on})}$ between the instant when the gate voltage v_{ge} turns on and the instant when the IGBT current i_c starts to increase (or the collector–emitter voltage of IGBT v_{ce} starts to decrease). After this delay, i_c increases to its peak value before settling to its steady-state final value. The time interval for i_c to rise from 10% to 90% of its final value I_c is denoted as t_r, whereas the time interval between 0.1 I_c and 0.1 V_{ce} is called t_{on}.

Similarly, the experimental measurements for the turnoff transient can be seen in Fig. 5. The time delay between the turnoff of v_{ge} and the instant of increase in v_{ce} defines $t_{d(\mathrm{off})}$. After this delay, v_{ce} increases to a peak value and finally settles to a steady-state value. The fall time t_f of i_c defines the interval from 90% to 10% of its final value, while t_{off} defines the interval between 0.1 V_{ce} and 0.1 I_c. The tailing current time interval is defined from 10% of I_c to 1% of I_c. Figs. 3–5 also show the current time t_i which is the time interval between the sensed gating signal and the instant when the voltage reaches 10% of its initial value during the turn-on transient and the current reaches 10% of its initial value during the turnoff transient.

Fig. 6 shows the measured characteristics for the antiparallel diode. The reverse-recovery time t_{rr} is the interval from 10% of diode voltage V_d to 10% of the diode-reverse-recovery current I_{rr}. After the turn-on delay $t_{d\,(\mathrm{on})}$ of the DUT, the diode current I_d starts to reduce until it reaches the peak of I_{rr}, and then, it reduces gradually.

The rise and fall times of the currents and voltages in the measured characteristics are relatively constant, and they are proportional to the amplitudes of the final values. Based on this behavior, the per-unit characteristics were obtained and stored in lookup tables (LUTs) in the FPGA. During the real-time simulation, these per-unit characteristics are called up and scaled by the instantaneous current and voltage amplitudes to obtain the actual switching functions. The experimental data were collected at a 0.2-ns resolution. Figs. 4 and 6 also show the data which were used for the FPGA implementation in Section III. The implemented model data were averaged over 12.5 ns for the FPGA input clock frequency of 80 MHz. Table III in the Appendix lists the measured IGBT characteristics for the CM50DU-24F against those provided by the manufacturer's data sheet. The experiment was carried out

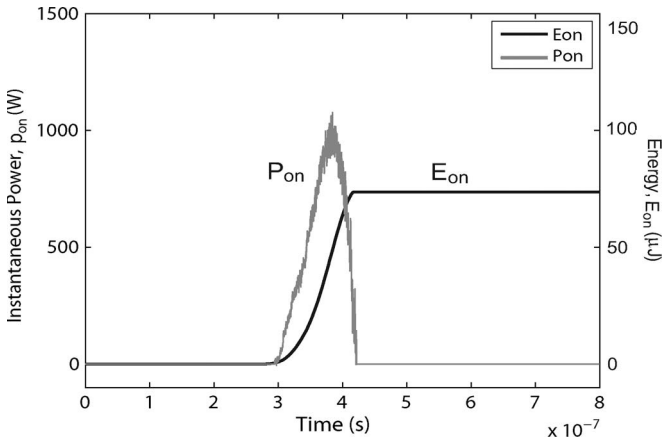

Fig. 7. Measured IGBT hard-switching turn-on power losses.

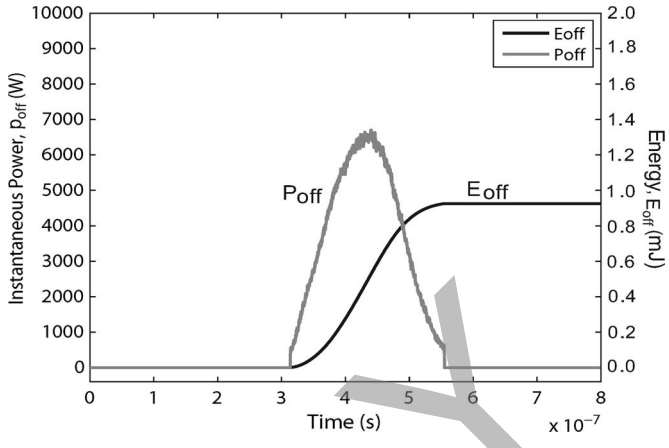

Fig. 8. Measured IGBT hard-switching turnoff power losses.

at 300 V and 15 A due to limitation on the ratings of the laboratory apparatus even though the data-sheet test conditions were measured at 600 V and 50 A. Accordingly, we can see the differences in the switching times: for example, $t_{d\,(\mathrm{on})}$ is three times higher than that of the data-sheet value under the measurement conditions. Similarly, the measured current fall time t_f is one-third of the data-sheet value. Some of the data, such as t_{on}, t_{off}, and t_i, are not provided in the data sheet.

The rise and fall times for the current and voltage appear to be constant, and they are proportional to the amplitude of the final value [24]. Therefore, the turn-on and turnoff waveforms are obtained by scaling with the final amplitude and can get the per-unit function. Based on this function, the real-time implementations in the FPGA were calculated.

B. IGBT and Diode Losses

The two most important power losses considered for modeling the IGBT in this paper are the switching and conduction losses. Switching losses are the power dissipation during the turn-on and turnoff switching transients. These losses depend on the switching frequency of the device. At a high switching frequency for the PWM converter, these losses become significant and must be considered. The switching losses are proportional to the product of the voltage across the IGBT and the current through it at the instant of switching. The experimental data for $v_{ce}(t)$ and $i_c(t)$ that we can see in Figs. 4 and 5 were multiplied point by point to obtain the instantaneous power waveforms calculated by (1) and shown in Figs. 7 and 8 for the turn-on switching loss (p_{on}) and turnoff switching loss (p_{off}) transients, respectively

$$p_{\mathrm{sw}}(t) = v_{ce}(t) \cdot i_c(t). \tag{1}$$

The area under the power waveform is the switching energy (E_{on} or E_{off}) expressed as

$$E_{\mathrm{sw}} = \int_{t_0}^{t_1} v_{ce}(t) \cdot i_c(t)\, dt \tag{2}$$

where t_0 and t_1 are the starting and ending times of turn-on or turnoff switching regimes.

Conduction losses occur when the device is between the IGBT turn-on and turnoff switching periods with the exclusion of the turn-on and turnoff transient times. From the measured data, this loss was calculated as the product of the device current $i_c(t)$ during the conducting time, not including the switching time and the forward saturation voltage $V_{ce\,(\mathrm{sat})}$ of the IGBT

$$p_{\mathrm{cond}}(t) = V_{ce\,(\mathrm{sat})} \cdot i_c(t). \tag{3}$$

The conduction energy can be calculated by

$$E_{\mathrm{cond}}(t) = p_{\mathrm{cond}}(t) \cdot t_{\mathrm{cond}} \tag{4}$$

where $t_{\mathrm{cond}} = t_{\mathrm{sw}} - t_{d(\mathrm{on})} - t_{\mathrm{on}} + t_{d(\mathrm{off})}$ is the conduction period. The time t_{sw} is the gating signal turn-on duration which depends on the switching frequency. The conduction losses are 27 W and 3.34 mJ at 15-A and 8-kHz switching frequency with a modulation index of 1.0. In most applications, the actual conduction loss will be slightly less than the calculated value; not only the IGBT saturation voltage $V_{ce(\mathrm{sat})}$ is lower than the data-sheet value but also the actual load current is less than the IGBT rated current. During the IGBT turn-on switching transient, the diode turnoff loss occurs due to the diode-reverse-recovery current. In modern IGBT modules like the CM50DU-24F, the IGBTs are freewheeled with superfast diodes [33], and the turn-on losses of the diode are negligible compared to their turnoff losses. The diode turnoff loss can be calculated using $v_d(t)$ and $i_d(t)$ in (1) and (2). It must be noted that, during the measurement of losses, the voltage and current probes modify the behavior of the DUT, which may lead to biased measurements. The fact that simulation gave realistic prediction of losses (as will be shown in Section VI) is due to the smoothing action of computing long-term average values. However, in this paper, the effect of probes and errors in measurements are ignored.

C. Tailing Current

Based on its physical structure, the IGBT can be viewed as a MOSFET cascaded by a bipolar junction transistor [34]. When the IGBT is turned on, some parts of its current $i_c(t)$ flows through the MOSFET, and the remaining portion flows through the transistor. The ratio of these two currents depends

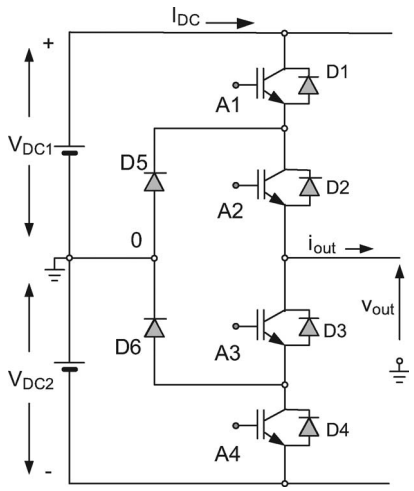

Fig. 9. One leg of the three-level VSC.

on the device construction. During the turnoff transient, the MOSFET turns off faster than the transistor, and its part of the current is quenched quickly. However, the part of current in the transistor continues to flow until the stored minority charge has fully recombined. This phenomena results in the tailing current behavior. In Fig. 8, for the turnoff transient, the tailing current $I_{\rm tail}$ between 10% and 1% of I_c can be clearly observed. The tailing time $t_{\rm tail}$ for this IGBT has been measured to be 196 ns. In general, the turnoff losses $p_{\rm off}$ are calculated for the duration of 10% of V_{ce} to 10% of I_c. If the $I_{\rm tail}$ is too long after 10% of I_c, the actual $p_{\rm off}$ is slightly higher than the calculated value. Since the duration of $I_{\rm tail}$ in Fig. 8 is less than 200 ns, the calculated IGBT losses are quite realistic.

III. Three-Level VSC Model

Using the measured IGBT characteristics from Section II, the three-level VSC model was developed first based on a single-phase leg. As shown in Fig. 9, one leg of the three-level converter consists of four IGBTs (A1, A2, A3, and A4), with four antiparallel diodes (D1, D2, D3, and D4), and two clamping diodes (D5 and D6) to clamp the output terminal voltage $v_{\rm out}$ to the neutral point. The IGBTs can be divided into two pairs A1–A3 and A2–A4. The gating signals for the IGBTs in each pair are complementary with an appropriate dead time. There are $2^4 = 16$ possible switching combinations for the four IGBTs; however, 11 of those combinations are invalid due to the following two operating limits for the three-level converter.

1) The IGBTs in each pair (A1–A3 and/or A2–A4) cannot be on simultaneously to avoid dc voltage shoot through.
2) A2 and A3 cannot be off simultaneously to avoid a floating output voltage on the phase leg.

This model does not include faulted converter states. Therefore, the following five valid states of the three-level converter are considered.

1) Switches A1 and A2 are closed, while switches A3 and A4 are open.
2) Switches A2 and A3 are closed, while switches A1 and A4 are open.
3) Switches A3 and A4 are closed, while switches A1 and A2 are open.
4) Three switches A1, A2, and A4 are open during *dead time 1* between switches A1 and A3.
5) Three switches A1, A3, and A4 are open during *dead time 2* between switches A2 and A4.

For each of these combinations, at every time step (12.5 ns) of the real-time simulation, the value of the load current $i_{\rm out}$ is used to determine whether the current will flow through the IGBTs or the clamping or antiparallel diodes.

For example, consider that, at time $t = t_1$, the gating signals for A1, A2, A3, and A4 are changed to 1, 1, 0, and 0, respectively. If the load current $i_{\rm out}$ is positive, it will flow through the diodes D3 and D4 for $t < t_1$, and the steady-state output voltage would be $v_{\rm out} = -V_{DC2} - 2V_{d(\rm sat)}$, where $V_{d(\rm sat)}$ is the voltage drop across the diode. After $t = t_1 + t_{d(\rm on)}$, A1 and A2 will start to conduct. The diode currents I_{d1} and I_{d2} will reduce until they reach the peak of the diode-reverse-recovery current $I_{\rm rr}$. Then, the load current $i_{\rm out}$ will flow through the IGBTs to reach its steady-state value of I_c. The output voltage will also rise until it reaches its steady-state value of $v_{\rm out} = V_{DC1} - 2V_{ce(\rm sat)}$. During *dead time 1*, the gating signals for A1, A2, A3, and A4 will change to 0, 1, 0, and 0, respectively, and the output voltage is $v_{\rm out} = V_{d(\rm sat)} + V_{ce(\rm sat)}$. After the time $t_{d(\rm off)}$ for A1, the collector–emitter voltage v_{ce} will increase, and collector current i_c decreases until it reaches 90% of I_c. Thereafter, the IGBT current i_c falls quickly to reach 10% of I_c, which causes the overshoot in v_{ce}. Within the tailing region, the IGBT current i_c falls slowly, becoming almost zero, and then gets replaced by the current of clamping diode D5 flowing through A2. For the gating pattern 0, 1, 1, 0, the positive current will continue to follow through D5 and A2, and $v_{\rm out} = V_{d(\rm sat)} + V_{ce(\rm sat)}$. During *dead time 2*, for the gating pattern 0, 0, 1, 0, the current will flow through the antiparallel diodes D3 and D4, and $v_{\rm out} = -V_{DC2} - 2V_{d(\rm sat)}$. When the gating pattern changes to 0, 0, 1, 1, the positive current will continue to flow through D3 and D4, when the steady-state output voltage will be $v_{\rm out} = -V_{DC2} - 2V_{d(\rm sat)}$.

On the other hand, if $i_{\rm out}$ is negative and assuming that the gating signals for A1, A2, A3, and A4 were equal to the gating pattern 1, 1, 0, 0 at time $t = t_1$, the current would flow through the diodes D1 and D2 for $t < t_1$, and at $t = t_1$, it would continue flowing through the same diodes and the forward conduction occurs, resulting in $v_{\rm out} = V_{DC1} + 2V_{d(\rm sat)}$. During *dead time 1*, with the gating pattern 0, 1, 0, 0, $v_{\rm out}$ will be same as before. For the switching pattern 0, 1, 1, 0, the negative $i_{\rm out}$ will flow through A3 and D6, resulting in $v_{\rm out} = V_{ce(\rm sat)} + V_{d(\rm sat)}$. During *dead time 2*, the output voltage $v_{\rm out}$ will remain the same as before. Finally, when the gating pattern 0, 0, 1, 1 occurs, the load current $i_{\rm out}$ will go through A3 and A4 with $v_{\rm out} = -V_{DC2} + 2V_{ce(\rm sat)}$.

When the load current $i_{\rm out}$ is equal to zero, the steady-state value for the output voltage will be V_{DC1}, 0, or $-V_{DC2}$, depending on the gating pattern.

The FPGA realization of the single leg of the three-level VSC is shown in Fig. 10. The model receives two gating signals A1 and A2 from the controller. These gating signals pass through

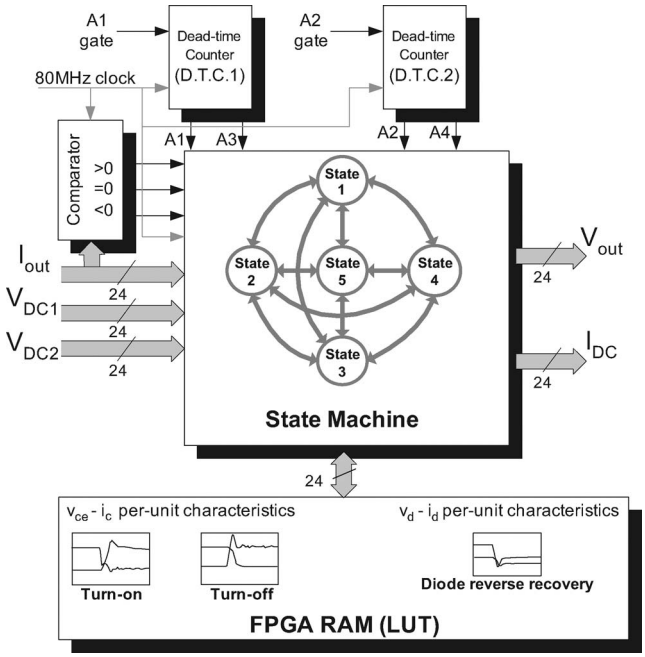

Fig. 10. Functional block diagram of the FPGA hardware realization for one three-level VSC leg.

the dead-time counters to generate their complements A3 and A4. At each time step, based on the four gating signals, the load current i_{out}, and two dc power supplies V_{DC1} and V_{DC2}, the model then implements a state machine with five valid states. The state machine interacts with the LUTs in the FPGA RAM where the per-unit device characteristics are stored at a resolution of 12.5 ns. The appropriate device characteristic is read from the LUT, and the corresponding v_{out} and I_{DC} are calculated.

The single-leg model was duplicated to make the three-phase three-level VSC model. The inputs to the VSC model are the three-phase currents, two dc voltages, and six gating signals with their complements. The outputs of the model are the three-phase voltages V_a, V_b, and V_c, and the current I_{DC}. All the model variables are chosen as signed fixed point numbers except for the gate signals which are single bits. The number format for all model voltages and currents in the FPGA implementation was 19.5, i.e., 19 b is used to represent the integer part, and 5 b is used to represent the fractional part.

IV. Induction Machine Model, Field-Oriented Control System, and Gating Signal Generation

A four-pole 50-hp 460-V squirrel-cage induction motor, which parameters are given in Table IV of the Appendix, was used in the real-time simulation. The machine representation is based on the fifth-order stationary reference frame model [32] and is described by the following state-space equations on the electrical side:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{5}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} \tag{6}$$

where $\mathbf{x} \in \mathbb{R}^4$ is the state vector composed of stator and rotor flux linkages, $\mathbf{u} \in \mathbb{R}^2$ is the input vector composed of stator voltage components, and $\mathbf{y} \in \mathbb{R}^4$ is the output vector composed of stator and rotor current components, defined as

$$\mathbf{x} = [\lambda_{\alpha s}(t) \quad \lambda_{\beta s}(t) \quad \lambda_{\alpha r}(t) \quad \lambda_{\beta r}(t)]^{\mathrm{T}} \tag{7}$$

$$\mathbf{u} = [V_{\alpha s}(t) \quad V_{\beta s}(t)]^{\mathrm{T}} \tag{8}$$

$$\mathbf{y} = [i_{\alpha s}(t) \quad i_{\beta s}(t) \quad i_{\alpha r}(t) \quad i_{\beta r}(t)]^{\mathrm{T}}. \tag{9}$$

The mechanical dynamics of the machine are represented by the following equations using rotor electrical speed ω_r as the state variable:

$$\dot{\omega_r}(t) = \frac{P}{2J}\left[T_e(t) - T_L(t)\right] \tag{10}$$

$$T_e(t) = \frac{3}{2}\frac{P}{2}\left[i_{\beta s}(t) i_{\alpha r}(t) - i_{\alpha s}(t) i_{\beta r}(t)\right] \tag{11}$$

where P is the number of poles, and J is the total rotor inertia. T_e and T_L are the electrical and load torques, respectively. The machine parameters are given in Table IV in the Appendix. The complete FPGA hardware implementation of this machine model is described in [27]. The trapezoidal rule with a time step of 10 μs is used to discretize the model that was given by (5)–(11). The DSP Toolbox from Altera was used to implement the model in MATLAB/SIMULINK, and the generated VHDL code was integrated with the remaining parts of the system. In addition to the stator and rotor current components, the model also outputs the rotor flux magnitude and position which are used to implement the field-oriented control.

Field-oriented control allows for decoupled control of the rotor flux and torque of the machine by using a dq machine representation, where the d-axis is aligned with the rotor flux space vector rotating at ω_e rad/s and the q-axis is 90° apart. The inputs to the controller are the rotor flux reference and the speed reference. The measurements are rotor speed, stator currents, and the rotor flux space vector. The torque reference is derived from the speed controller, while the current references (I_{ds}^* and I_{qs}^*) come out of the flux and torque controllers. Two independent current controllers provide the respective V_{ds}^* and V_{qs}^* control commands in the field-oriented rotor reference frame. The desired three-phase control signals for PWM v_a^*, v_b^*, and v_c^* are generated from V_{ds}^* and V_{qs}^* by the transformation to the stationary reference frame. The controller was implemented by using DSP Toolbox at a sampling period of 62.5 μs, as described in [27]

Synchronized asymmetrical regular sampling with a triangular carrier [35] is used to generate the PWM gating signals for the three-level VSC. A one-sixth third-harmonic component is injected into the fundamental control waveforms to obtain a 15% increase in modulation index. The carrier frequency for the PWM is 8 kHz, while the controller sampling frequency is 16 kHz. As shown in Fig. 11, two synchronized triangle carriers are compared with the control signals (v_a^*, v_b^*, and v_c^*) to generate the necessary switching signals. In Fig. 12, the carrier waveforms are generated at a resolution of 12.5 ns in the FPGA with the 16-b up–down counters. The *Sync* signal is used to synchronize the carrier waveform to the control waveform. The *reset* signal resets the counters at the top and bottom limits of

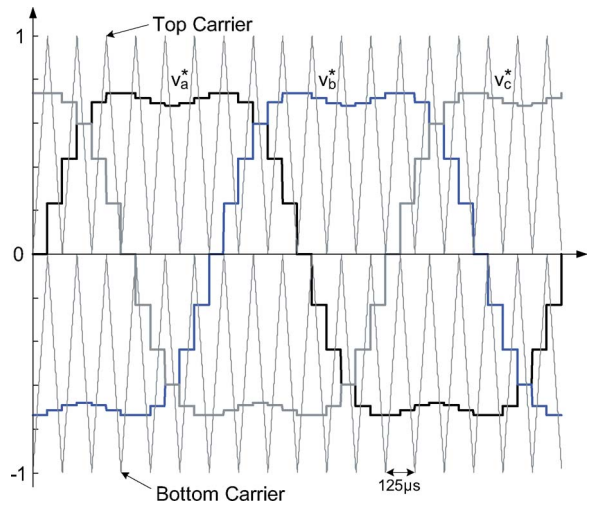

Fig. 11. Three-level asymmetrical regular sampled PWM.

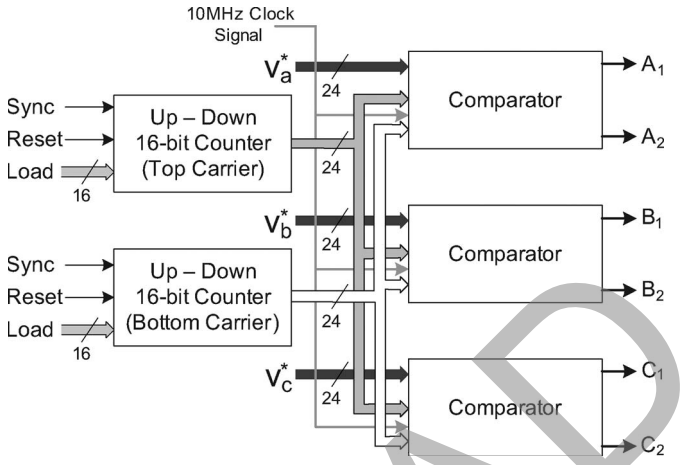

Fig. 12. Functional block diagram of the FPGA hardware realization for three-level PWM.

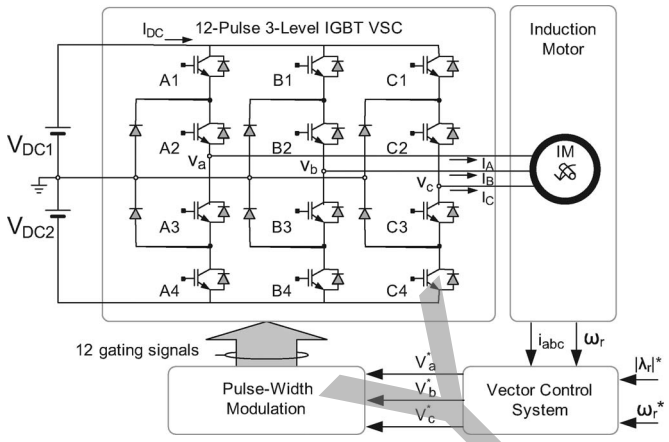

Fig. 13. System components of the three-level vector-controlled ac drive for real-time simulation.

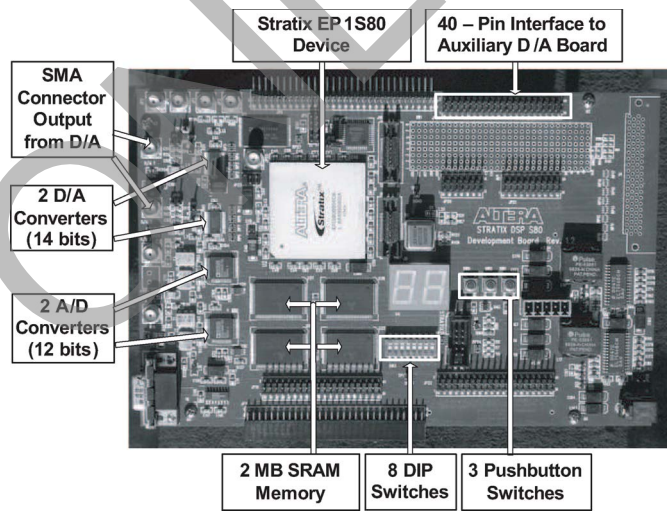

Fig. 14. Altera's Stratix FPGA Development Board used to build the real-time simulator.

the carrier signal. The comparison of the top carrier with the control signal v_a^* provides the gating signal for the IGBT A1, while the comparison of the bottom carrier with the control signal v_a^* provides the gating signal for this IGBT A2. A dead time of 2 μs is inserted (Fig. 10) to obtain the gating signal A3 from A1 and the gating signal A4 from A2. Similarly, the gating signals for the IGBTs in the other two VSC legs are generated. This PWM scheme was implemented using the Altera's DSP Blockset.

V. FPGA-Based Real-Time Simulation of Three-Level Drive System

The complete three-level VSC-fed induction machine drive shown in Fig. 13 was implemented on a single Altera Stratix FPGA available on the EP1S80 FPGA Development Board (Fig. 14), supplied by the Canadian Microelectronics Corporation. The resources available in the Stratix FPGA include 79 040 logic elements (LEs), 7 427 520 total RAM bits, 176 DSP blocks with 9-b elements, 12 phase-locked loops, and 679 maximum user I/O pins.

The FPGA Board includes an 80-MHz crystal oscillator, two 14-b 165-MHz digital-to-analog converters (DACs), and two 12-b 125-MHz analog-to-digital converters. The three push buttons are used as a human interface to the simulator: to reset the system, to change the speed reference, and to reverse the speed reference of the motor, respectively. The dual in-line package (DIP) switches are used to control the increment and decrement of speed reference and to apply the load on the motor shaft. The FPGA board was interfaced to an auxiliary 14-channel 1-MHz DAC board using an onboard 40-pin connector.

All the system models are coded in VHDL, and the configuration file defines all the signal connections between various components.

The overall system needs the following input signals: 1) two dc supply voltages (V_{DC1} and V_{DC2}); 2) reference motor speed (ω_r^*); 3) reference rotor flux magnitude ($|\lambda_r|^*$); and 4) mechanical load torque (T_L).

The VHDL code for the real-time simulation of the system was compiled using Altera's Quartus environment on an IBM IntelliStation Z Pro with Xeon 3.4-GHz processor. The generated bitstream was downloaded to the development board

TABLE I
FPGA RESOURCES UTILIZED BY SYSTEM COMPONENTS

Component	Logic Elements	DSP Blocks	Memory Bits
3-level VSC	20669 (26.2%)	40 (22.7%)	26880 (0.4%)
Ind. Mach.	21881 (27.7%)	128 (72.7%)	0
Controller	9676 (12.2%)	8 (4.6%)	0
PWM	250 (0.3%)	0	0
Conn. Sys.	350 (0.4%)	0	0
Reference	118 (0.2%)	0	0
Interface	99 (0.1%)	0	0
Total	53043 (67.1%)	176 (100%)	26880 (0.4%)

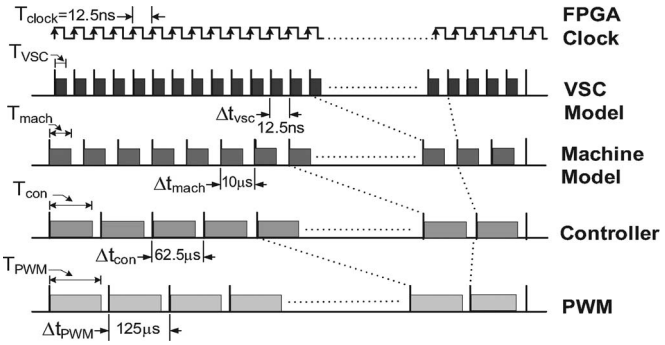

Fig. 15. Timing diagram with model time steps (Δt) and execution times (T); $T_{\rm VSC} = 11$ ns, $T_{\rm mach} = 9$ μs, $T_{\rm con} = 61$ μs, and $T_{\rm PWM} = 122$ μs.

through the JTAG interface. The FPGA resources used by the individual components of the system simulation can be seen in Table I. In this table, the Connection System refers to the final file that is necessary to connect all developed components. The entire system design occupies approximately one-third of the total LEs of the FPGA; the VSC and the induction machine model being computationally intensive take up most of the DSP blocks on the board. Only the VSC model requires the onboard RAM for the IGBT characteristic LUTs. The execution times of the various models are shown in Fig. 15.

VI. RESULTS AND DISCUSSION

This section presents the results from the FPGA-based real-time simulator. The results were captured on a 500-MHz *Tektronix* DPO7054 4-channel oscilloscope that was connected to the DACs on the Altera FPGA board and the auxiliary DAC board. The results show the details of the IGBT switching characteristics, the VSC steady-state voltage and current waveforms, and the induction machine transients.

A. IGBT and Diode Switching Characteristics and Losses

The IGBT and diode switching characteristics obtained from the real-time simulation were compared with the measured characteristics in Section II to ascertain the accuracy of the proposed FPGA-based VSC model. Figs. 16–18 show the oscilloscope traces of the switching transients during the IGBT turn-on, IGBT turnoff, and the diode-reverse-recovery characteristics, respectively. These traces were obtained by zooming into the voltage and current real-time waveforms of IGBT A1 in the three-level VSC. All the switching times shown in these figures match the measured times in Table III of the Appendix very closely.

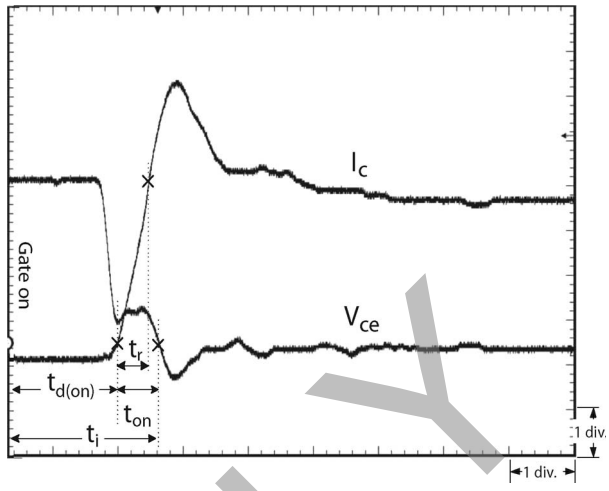

Fig. 16. Real-time simulation oscilloscope trace of IGBT hard-switching turn-on transient [scale: v_{ce}: 85 V/div, i_c: 5 A/div, and time: 200 ns/div].

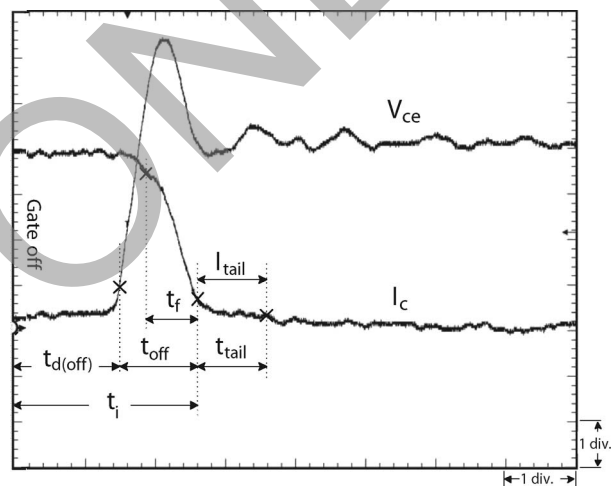

Fig. 17. Real-time simulation oscilloscope trace of IGBT during hard-switching turnoff transient [v_{ce}: 85 V/div, i_c: 5 A/div, and time: 200 ns/div].

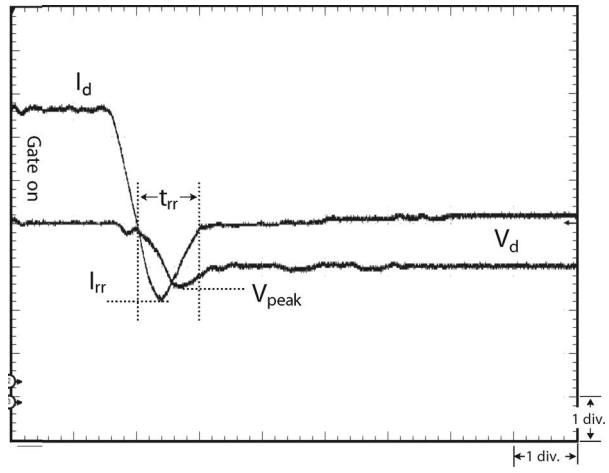

Fig. 18. Real-time simulation oscilloscope trace of diode-reverse-recovery characteristics during IGBT hard-switching turn-on [v_d: 300 V/div, i_d: 5.5 A/div, and time: 200 ns/div].

In Fig. 16, after a time $t_{d(\rm on)}$, the collector current starts to rise almost linearly, and the load current in the antiparallel diode gradually decreases at the same time and transfers to achieve

TABLE II
COMPARISON OF THE ENERGY DISSIPATIONS OF IGBT AND DIODE

	Experiment	Real-time simulation	Error
E_{on} (IGBT)	73.65μJ	73.85μJ	0.27%
E_{off} (IGBT)	0.925mJ	0.928mJ	0.32%
E_{cond} (IGBT)	3.34mJ	3.35mJ	0.29%
$E_{rev.recov}$ (Diode)	0.396μJ	0.398μJ	0.51%
E_{cond} (Diode)	3.06mJ	3.07mJ	0.33%

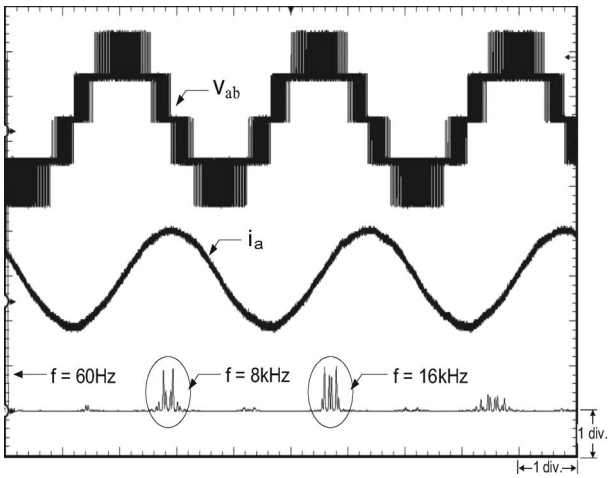

Fig. 19. Real-time simulation oscilloscope trace of the steady-state line voltage v_{ab} and line current i_a applied to the machine, and the harmonic spectrum of v_{ab} [scale: v_{ab}: 350 V/div, i_a: 20 A/div, and time: 5 ms/div].

the steady-state value. The peak value of the collector current is due to the reverse-recovery process of the antiparallel diode (Fig. 18) during the switching transition condition.

In the turnoff transient from the real-time simulation shown in Fig. 17, the tailing current can be clearly seen. The turnoff process starts at the application of the negative gate voltage v_{ge}. The input capacitance of the IGBT discharges gradually and reduces v_{ge}, but the collector–emitter voltage v_{ce} remains unchanged until v_{ge} drops enough to drive the device out of saturation. Thereafter, v_{ce} rises rapidly. The collector current, on the other hand, has a rapid fall initially followed by a more gentle drop toward extinction at time t_{tail}. The rapid fall in the collector current i_c produces the overshoot in the collector–emitter voltage v_{ce} due to the parasitic inductance of the device. Comparing Figs. 16–18 with Figs. 4–6, we can see that the real-time simulation can capture the nonlinear switching characteristics quite well. Table II shows the IGBT losses and diode-reverse-recovery losses calculated from the real-time simulation results. Comparing these losses to the ones obtained from the experimental measurement in this table, we can see that the developed real-time model can realistically predict the device losses.

B. Steady-State and Transient Results of the AC Drive

Fig. 19 shows the line-to-line voltage v_{ab} and the line current i_a once the machine has reached the steady state with $\omega_r^* = 377$ rad/s. The characteristic three-level voltage waveform can be clearly seen. In the fast Fourier transform calculated by the oscilloscope, it is possible to see the fundamental component and switching harmonics at $f = 8$ kHz and $f = 16$ kHz.

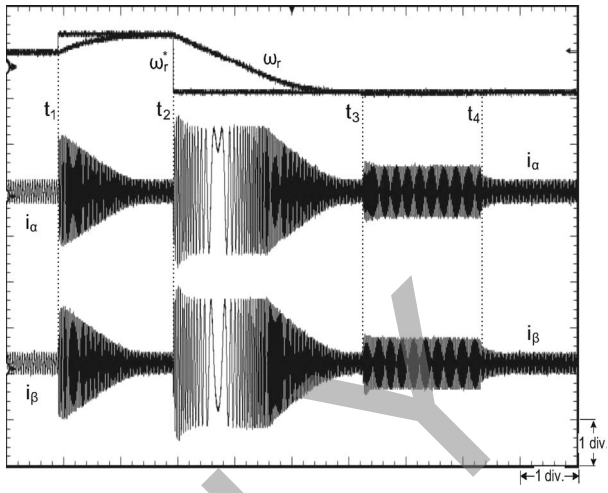

Fig. 20. Real-time simulation oscilloscope trace of the reference speed ω_r^*, machine speed ω_r, and currents i_α and i_β for the machine running at 150 rad/s and speed set-point variation to 377 rad/s at t_1, speed reversal to -377 rad/s at t_2, and the application and removal of load at t_3 and t_4 [scale: ω_r^*, ω_r: 630 rad/s/div, i_α, i_β: 150 A/div, and time: 1 s/div].

Fig. 20 shows the machine speed ω_r, speed reference ω_r^*, and the rotor current components i_α and i_β when the machine is subjected to the following four transients: 1) Machine starts with $\omega_r^* = 150$ rad/s; 2) speed reference is changed to 377 rad/s at time t_1; 3) speed reversal at -377 rad/s at time t_2; and 4) the application of a load 100 N · m at time t_3 and the removal of the load at time t_4. To get these transient results of the ac drive, the three push buttons and DIP switches on the FPGA board were applied. The smooth and fast response of the speed controller can be observed as the machine speed tracks its reference. We can also see the frequency variation in the current waveforms as the machine comes to a standstill from 377 rad/s and speeds up to -377 rad/s. No perturbation in the speed is observed when the load is applied and removed during t_3 and t_4. These results prove that the control system is working quite well. These system-level real-time results have been verified by offline simulation in MATLAB/SIMULINK.

VII. CONCLUSION

The ability to realistically model nonlinear IGBT characteristics is an important step in the effort to make a real-time drive simulator behave like the actual system. Reproducing the device nonlinear characteristics in real time has not been possible hitherto due to two reasons: first, the type of digital hardware used in real-time simulators and, second, the time frame for modeling the device characteristics. IGBT switching transients happen on a timescale of hundreds of nanoseconds, and currently available general-purpose processors and DSPs are simply not fast enough, despite their high clock frequency, to use a sufficiently small time step to model these transients in real time. Using an FPGA as the main computational engine, this paper has proposed a device-level behavioral model of the IGBT-based VSC that can realistically reproduce the nonlinear characteristics and losses. The model runs in real time at a time

TABLE III
MEASURED DATA FOR THE *Powerex* CM50DU-24F IGBT MODULE

Characteristics	Measured data at 300V, 15A	Datasheet values at 600V, 50A
$t_{d(on)}$	300ns	100ns
t_r	100ns	50ns
t_{on}	120ns	-
$t_{i(on)}$	420ns	-
$t_{d(off)}$	350ns	300ns
t_f	100ns	300ns
t_{off}	230ns	-
$t_{i(off)}$	550ns	-
$V_{ce(sat)}$	1.8V	1.8V
$V_{d(sat)}$	1.65V	1.65V

TABLE IV
INDUCTION MACHINE PARAMETERS

R_s	0.087Ω
R_r	0.228Ω
L_m	34.7mH
L_s	35.5mH
L_r	35.5mH
J	1.662Kg.m^2

step of 12.5 ns. In addition, to the three-level VSC model, the FPGA-based real-time simulator also models an induction machine, the field-oriented controller, and a pulsewidth modulator, making up the complete ac drive system. All the models were written in VHDL. The FPGA resource allocation table provides an idea of the system model complexity involved in the real-time simulator. The real-time results have been found to be in good agreement with the measured device characteristics; at the same time, the real-time simulator is able to reproduce the system-level waveforms quite well. Looking ahead, FPGAs offer the most suitable solution, due to their hardwired parallel architecture, to increasing the modeling capacity and speed of real-time simulators for the detailed modeling of multilevel and multi-pulsed-power electronic drives.

APPENDIX

The measured data for the CM50DU-24F IGBT module and the induction machine parameters are shown in Tables III and IV, respectively.

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