Multiport DC-DC-AC Modular Multilevel Converters for Hybrid AC/DC Power Systems

by

Mohammadhadi Rouhani

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Energy Systems

Department of Electrical and Computer Engineering

University of Alberta

Abstract

This thesis explores multiport modular multilevel converter (MMC) structures for hybrid connection of ac and dc systems (MP-DC2AC MMC). Salient features of MP-DC2AC MMCs are a single converter structure, single-stage dc-dc-ac power exchange, and a condensed converter station footprint. So far, little information is available on the concept of single MMC structures that can perform simultaneous dc-dc and dc-ac (hereinafter dc-dc-ac) conversions at high voltage high power applications. The purpose of this work is to fill this research gap by presenting a dynamic controller for family of MP-DC2AC MMCs and test the controller for several power flow case studies. In addition, a fair comparison of four MP-DC2AC MMCs is presented for different dc voltage steps. Based on the existing well-known MMC based topologies, four different MP-DC2AC MMC topologies are identified by reconfiguring the modular multilevel chain links. Two of these topologies are new and therefore are the major focus of the thesis. Four core topologies are compared based on technological variables and operating principles. A control system is developed in this thesis for all four converters to provide bidirectional power flow between the ports and keep capacitor voltages balanced. The controller is then explained in detail for MP-M2DC and MP-BB and extended for MP-AT and MP-DAB. To

evaluate the performance of the proposed control strategy, extensive switched-mode simulations are carried out to verify the proposed solutions for multiport hybrid connections. The MP-DC2AC MMCs are promising tools for multiport connection of future hybrid ac/dc systems and ease the hurdles for smart grid infrastructures.

To My Beloved Family

Acknowledgements

First of all, I would like to express my sincere gratitude to God for giving me the strength and providing me with the opportunity to complete this work.

I would like to thank my supervisor, Professor Gregory J. Kish for his advice and guidance improving this thesis. I would also thank members of my thesis examination committee, Professor John Salmon and Professor Hao Liang, for their time in improving this thesis.

I would like to express my most heartfelt gratefulness to my family for their everlasting love, patience, and support in all aspects of my life. I believe that I would have not been able to make this accomplishment without their support. This work along with every other step that I take in my life is dedicated to them.

Finally, a very special thank and love to my wife, Samira who was on this journey with me from the start. Thank you for being my muse, editor, proofreader, and sounding board. But most of all, thank you for being my best friend. I owe you everything.

Contents

List of Tables

List of Figures

List of Abbreviations

List of commonly used abbreviations

BESS	battery energy storage system
DAB	dual active bridge
FBSM	full-bridge submodule
HVDC	high voltage direct current
HVDC-AT	high voltage direct current autotransformer
HBSM	half-bridge submodule
LCC	line commutated converter
LVDC	low voltage direct current
M2DC	modular multilevel DC converter
MF2F	multiport front-to-front converter
MIMO	multi-input multi-output
MMC	modular multilevel converter
MP-AT	multiport HVDC autotransformer converter
MP-BB	multiport buck/boost converter
MP-DAB	multiport dual active bridge converter
MP-DC2AC	multiport DC-DC-AC converter
MP-M2DC	multiport modular multilevel dc converter
MTDC	multi-terminal direct current
MVDC	medium voltage dc
P2P	point to point
PI	proportional-integral
PLL	phase locked loop
SM	submodule
VCO	voltage controlled oscillator
VSC	voltage source converter

Chapter 1

Introduction

The need for installing more renewable energy sources to replace fossil fueled power plants is becoming a significant issue over the past decade due to the excessive amount of green house gas emissions in the atmosphere [3]. On- and Off-shore wind farms have become major sustainable renewable energy sources that can reduce a tremendous amount of carbon footprints. These massive clean sources of energy are located at remote areas and energy transmission using conventional ac system is inefficient. Medium and high voltage DC (MVDC and HVDC) systems are seen as preferred solutions to connect distant wind farms to the load centers due to their lower loss over very long distances [4].

Due to the demand for a more reliable and resilient transmission backbone for the existing ac grid, multi-terminal HVDC (MT-HVDC) systems are introduced using the technology of voltage source converters (VSCs). MT-HVDC systems are able to integrate massive renewable energy sources such as offshore and onshore wind farms and solar power plants [5]. To date, there have been significant number of point-to-point (P2P) HVDC lines for customer-specific projects. Linking these P2P dc segments together to form a unified MT-HVDC has several operational benefits (e.g. higher controllability, flexibility, reliability and less component footprints). Nevertheless, this interconnection process is challenging because of the following reasons

- There is no standard voltage level defined for dc systems and hence a variety of dc voltage levels exists
- dc corridors may be incorporated by different power industry vendors and the associated technology may not be compatible
- dc grids are based on LCC or VSC technology and certain compatibility component is required to link these systems.

Dc-dc converters have been considered as possible solutions to unify segmented P2P HVDC systems and build a backbone dc transmission system for ac grids. The term "*supergrid*" for the European future power grid has been popular for a decade due to the capabilities of MT-HVDC systems [6]. With the advent of modular multilevel converters (MMCs) in 2003, the development of dc-dc MMC is a viable option for the future supergrid because of its modularity and scalable structure [7]. MMCs require less filtering to provide a clean sinusoidal waveform on the converter ac side. Because of its high degree of controllability, MMC is found to be an efficient option for simultaneous multiport dc-dc and dc-ac (hereafter MP-DC2AC) conversion [8, 9]. This methodology is doubling the potential abilities of the existing dc-dc MMCs, to i) connect P2P HVDC lines and ii) support an external (weak) ac grid. Depending on the grounding isolation and non-isolation technology of dc systems, the dc-dc converters are grouped as i) isolated converters where there is a two-stage dc-ac and ac-dc conversion using an intermediate passive component (e.g. front-to-front [10]), and ii) non-isolated converters that are directly connected (single stage power exchange) using solely power electronics components (e.g. LCL converters [11], HVDC-autotransformer (HVDC-AT), M2DC and buck/boost MMC) [12]. A schematic of dc-dc-ac MMCs is shown in Figure 1.1 using two different grounding connections. Depending on the structure of the converter, the returning path of dc systems can be isolated (e.g. in MP-DAB using a galvanic separation) or there is common grounding for three ports (e.g. in MP-M2DC,

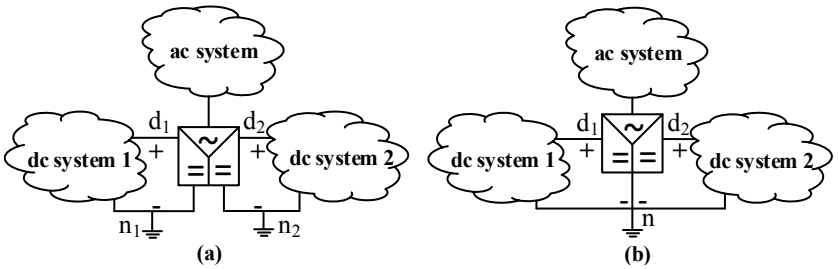

Figure 1.1: Schematic of MP-DC2AC MMCs for multiport connection of two dc and an ac systems, with (a) isolated and (b) non-isolated dc network grounding

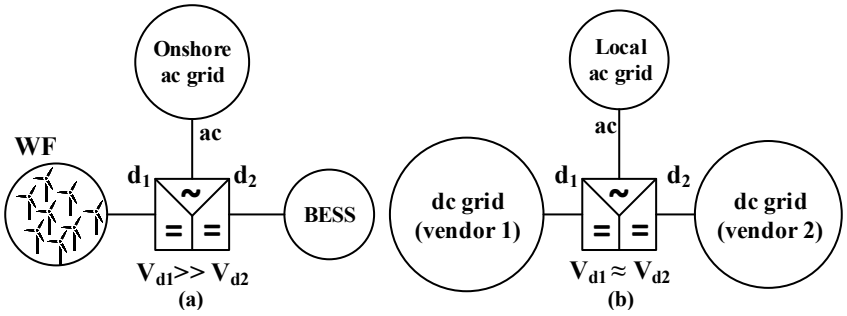

Figure 1.2: Applications of MP-DC2AC MMCs; multiport connection of (a) a windfarm (WF) and BESS at different dc voltages with local ac grid, and (b) multivendor connection of two dc grids at similar voltage levels

MP-BB, and MP-AT).

Two possible applications of MP-DC2AC MMCs are shown in Fig. 1.2(a) and (b). An offshore wind farm can be connected together with the onshore ac system and a local BESS using a MP-DC2AC MMC as depicted in Fig. 1.2(a). A MVDC collector network can be utilized for the wind farm as shown [13–15]. The BESS is designed for a lower MVDC voltage level. In contrast, Fig. 1.2(b) deploys a MP-DC2AC to interconnect two HVDC networks from two different vendors that operate at similar voltage levels. As a prerequisite for the future supergrid, dc systems from multivendors should be compatible and interconnected to allow bidirectional power flow without malicious inter-operation transients.

Upgrading the existing dc-dc converters to dc-dc-ac comes at some costs as well. Some of the associated costs are

- Semiconductor utilization to meet the capacity for nominal power ex-

change at each converter port (dc or ac) and semiconductor switch ratings

- Fault blocking capability on converter ports (dc and ac fault blocking at the same time)
- Appropriate insulation for magnetic transformer (dc and ac voltage stress on the core and windings)
- HVDC grounding return configuration for isolated and non-isolated converters (in monopolar and/or bipolar HVDC transmission systems)

Overcoming these characteristics, MP-DC2AC MMCs are key solutions for interconnection of bulk renewable energy sources and leveraging the reliability of hybrid ac/dc power system. To fill this research gap, the thesis intends to address circuit modelling and control of MP-DC2AC MMCs and show how the power flow mechanism works for dc-dc-ac conversions.

1.1 From DC-DC MMCs to DC-DC-AC MMCs

A three phase dc-ac MMC-based converter is shown in Figure 1.3. Each arm consists of a number of SMs in series (shown in Figure 1.4(e)) and using control systems, a three phase sinusoidal waveform is generated at the ac terminal of the converter. Many works have shown dc-dc converters for dc voltage matching at medium and/or high voltage levels. A comprehensive review of emerging non-isolated dc-dc converters and their applications for hybrid dc-ac systems are investigated in [9]. A comparison of existing dc transformers for HVDC grids is investigated in [16].

Several MMC-based converters are identified to operate dc-dc conversion and also have the ability to connect an external ac grid to the converter. M2DC introduced in [17, 18] is an MMC-based dc transformer using only two subconverters and a (passive) filter (F) that blocks ac components from entering the

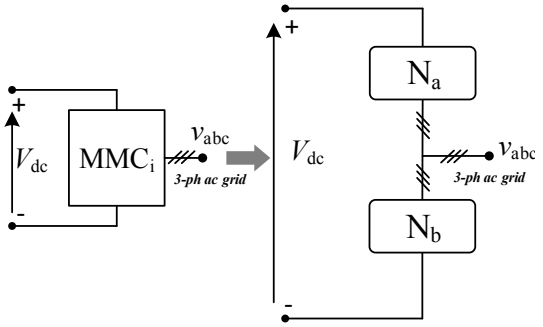

Figure 1.3: A three phase conventional dc-ac MMC

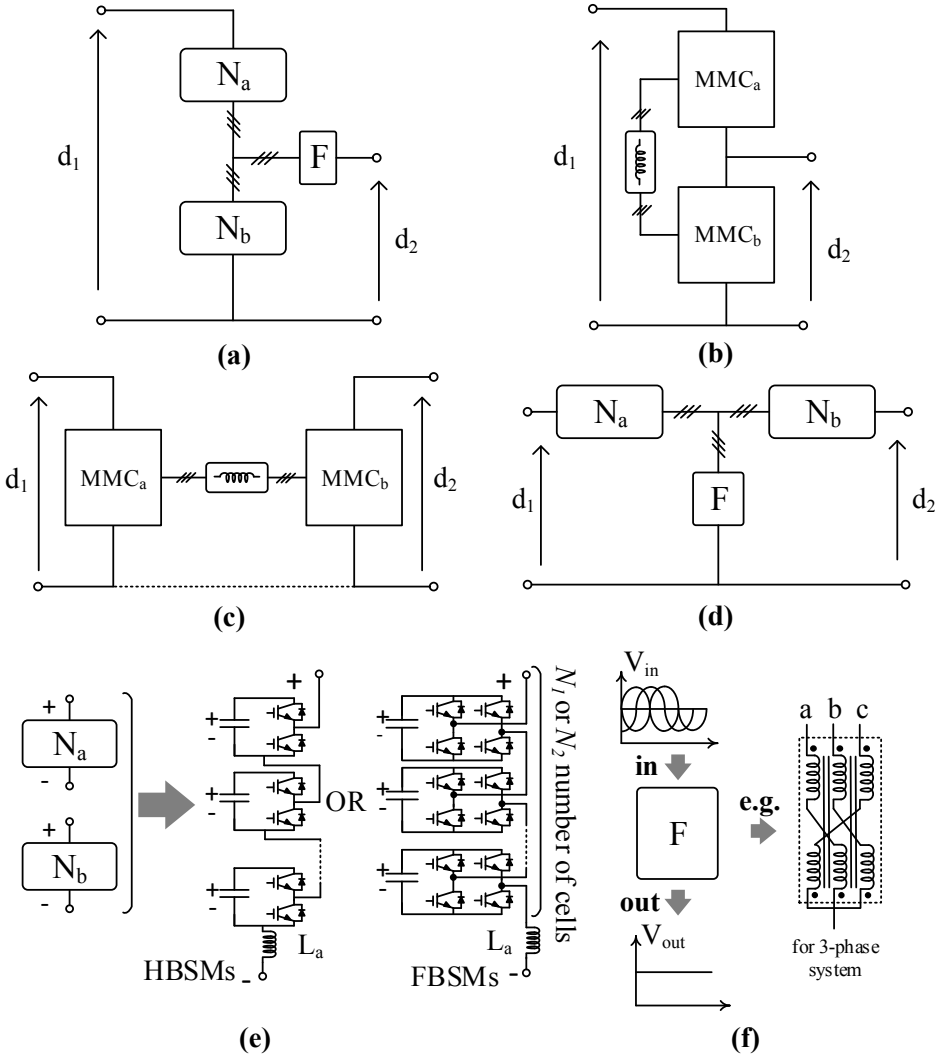

Figure 1.4: Three phase generic model of DC-DC MMCs, (a) M2DC, (b) HVDC-AT, (c) BB-MMC, (d) DAB, (e) standard arm components, and (f) s-phase filter

dc sides shown in Figure 1.4(a). Figure 1.4(f), shows a three phase zig-zag filter that blocks ac quantities from entering the dc port. This filter is necessary for dc-dc power transfer between dc ports and differentiates M2DC from conventional dc-ac MMC. Patents [19, 20] show drawings of the M2DC adapted for asymmetrical and symmetrical ac grid interfaces, respectively. However, scant information is provided on how these converters operate or can be controlled. A bipolar structure of M2DC also called dc-MMC is presented in [21, 22]. A bipolar dc-dc converter using zig-zag transformer is introduced in [23] to utilize the grounding of the transformer.

Another type of dc-dc converter where two MMCs are stacked in series with mid points connected using an ac transformer for internal circulating components is HVDC-AT that is shown in Figure1.4(b) [1, 24, 25]. The ac transformer in this converter is rated only for a portion of the nominal power transfer of the converter. It is shown that the ac grid can be linked to the converter using a tertiary winding on the core of the ac transformer converter [2, 26]. There should be a separate control loop for dc-ac beside the dc-dc power transfer control loop. In [27], an extended version of HVDC-AT is presented for dc-dc and dc-ac connections. A multitasking dc-dc and dc-ac converter is proposed in [28] where the HVDC-AT is upgraded to connect multiple dc systems with distinct dc voltage levels and an external local ac grid.

The dual active bridge (DAB) MMC is a well-known isolated dc-dc converter where two independent MMCs are connected on their ac side using an ac transformer [10, 29]. Beside dc-dc conversion, DAB MMCs shown in Figure 1.4(c) are used for other applications (e.g. HVDC transmission line power flow controller) [30, 31].

A most recent non-isolated dc-dc buck/boost (BB) MMC converter (shown in Figure 1.4(d)) that bears similarity to the DAB MMC introduced in [32] where the intermediate transformer of DAB MMC is replaced with direct cables. A passive filter similar to the one for M2DC is used to circulate ac components

within converter submodules (SMs).

Figure 1.5(a) shows one practical option for power routing between two dc systems (dc_1 and dc_2) that uses a common ac grid. In this case, two separate transformers rated at full power is required for dc-dc conversion. Using a MP-DC2AC can minimize magnetic requirements and lump two dc-ac converters into a single dc-dc-ac (isolated or non-isolated) at certain dc voltage stepping ratio.

For decades, power tapping and ac grid interface from HVDC lines have been major industrial research trends to extract a small portion (e.g. 5%) of power [33]. Series and shunt power tapping are two well-known strategies to extract power from HVDC lines [34–36]. These methods have several challenges including a very high stepping ratio conversion that makes the insulation of ac grid from HVDC system costly. Additionally, only a small amount of power can be delivered. It is shown in the literature that HVDC line tapping impacts the voltage profile of the transmission line [37]. With existing installed dc-dc MMCs, it is possible to connect an external ac grid to converter terminals using a galvanic separation (i.e. transformer) as shown in Figure 1.5(b).

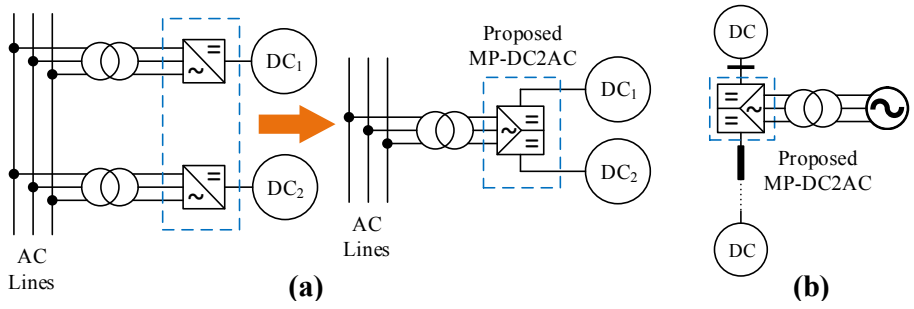

Figure 1.5: Two possible applications of MP-DC2-AC; (a) $DC_1 - DC_2$ Power routing through a common AC system, (b) AC Power Tapping from two different DC systems

The transformerless asymmetrical monopole dc-dc converter introduced in [38] and the bipolar structure in [39] are variants of HVDC-AT where the ac transformer is replaced with capacitor. The LCL dc-dc MMC introduced in [11] is actually a DAB converter where the intermediate ac transformer is re-

placed with a passive LCL filter. The converter proposed in [40] replaces the secondary MMC with an active interfacing filter. The transformerless non-isolated symmetrical monopolar converter introduced in [41] replaces the magnetic requirements in [32] with power electronic switches (MMC subconverter). A double wye dc-dc converter where the subconverter of each pole is similar to buck/boost MMC except the filter is replaced with semiconductor-based arms introduced in [42, 43]. The four core structures of dc-dc converter are the general case studies and all other mentioned dc-dc MMC are variants of these four topologies.

Comparative analysis for different types of dc-dc MMCs considering the semiconductor effort requirement is carried out based on semiconductor utilization effort, total capacitance stored energy, magnetic requirement, fault blocking capability, and efficiency [44–46].

1.2 Thesis Scope

A control modeling for multiport converters is presented that can reap the benefits of both ac and multiport dc systems by interconnecting two dc and an ac grids. This research project will initiate a grounding for further developments of hybrid dc/ac at high voltage and high power applications.

- MMC-based dc transformers are classified based on their dc voltage stepping ratio
- The semiconductor utilization (as the major cost) and magnetic requirement as well as the total energy storage of the MP converters are assessed for maximum power flow capacity and fault blocking capability using FB-SMs at each port
- The capability of MP-DC2AC MMCs in hybrid ac/dc power flow operation are examined

Chapter 2

MP-DC2AC: Topologies, Operation, and Modeling

The circuit modeling, dynamic states, and steady state power flow equations for a three phase topology of MP-DC2AC MMCS are developed and steady state equations are represented for active/reactive net power of converter arms. Phasor diagram representation is also represented to better understand the power flow mechanism of the topologies. A controller for dc-dc-ac conversion is proposed for MP-M2DC and then adapted for MP-BB, MP-AT, and MP-DAB MMCs.

2.1 Family of DC-DC MMCs with Distinct Chain Link Configurations

The four mentioned MMC-based dc transformers (namely DAB, HVDC-AT, M2DC, BB MMC shown in Figure 1.4) are identified to be the core structures of MP-DC2AC MMCs [47]. Other presented converters are partly modified versions of the four mentioned topologies, as discussed in section 1.1.

Four MP-DC2AC MMCs with the ability to exchange power between dc

ports (d_1 and d_2) and an ac port are shown in Figure 2.1. The arms are labeled with "a" and "b" comprised of SMs connected in series."F" represents a filtering component that blocks ac quantities from entering the dc ports. A three phase version of the filter is shown in Figure 1.4(f).

By rotating the MP-M2DC (ref to Figure 2.1(a)) topology and substituting the port labels, the MP-BB (ref to Figure 2.1(c)) is achieved (with the corresponding polarities being flipped). The procedure also holds for MP-DAB and MP-AT. Note that MP-AT and MP-DAB are comprised of two conventional dc-ac MMC. It is also shown in this work that the control system used for MP-M2DC can be extended for the other three topologies with minor changes.

Taking into account the dc voltage stepping ratio $G_v = V_{d2n}/V_{d1n}$, the MP-DC2AC MMCs in figure 2.1 are grouped into two types: i) buck converters where $V_{d1n} > V_{d2n}$, and ii) buck/boost converters where both $V_{d1n} > V_{d2n}$ or $V_{d1n} < V_{d2n}$ are possible. Buck converters are used to connect two dc systems with significant voltage differences, whereas buck/boost converters are utilized for dc voltage matching and for the purpose of multi-vendor compatibility.

2.2 Single Phase Leg Circuit Modeling

The single-phase representation of four core MP-DC2AC MMCs are shown in Figure 2.2. Converters arm voltages and currents are shown with circulating and terminal components that are suitable for dynamic analysis of the converter and control implementation. To transform the actual values to circulating and terminal components, the sum and difference approach is used [48, 49].

To simplify the circuit modeling, the following assumptions are made throughout the steady state analysis: i) voltages and currents of the converter contain dc and fundamental frequency components, ii) ac voltages with ideal sinusoidal waveform are generated on the converter arms, iii) the internal resistances are neglected unless otherwise indicated for a certain element, iv) output filtering

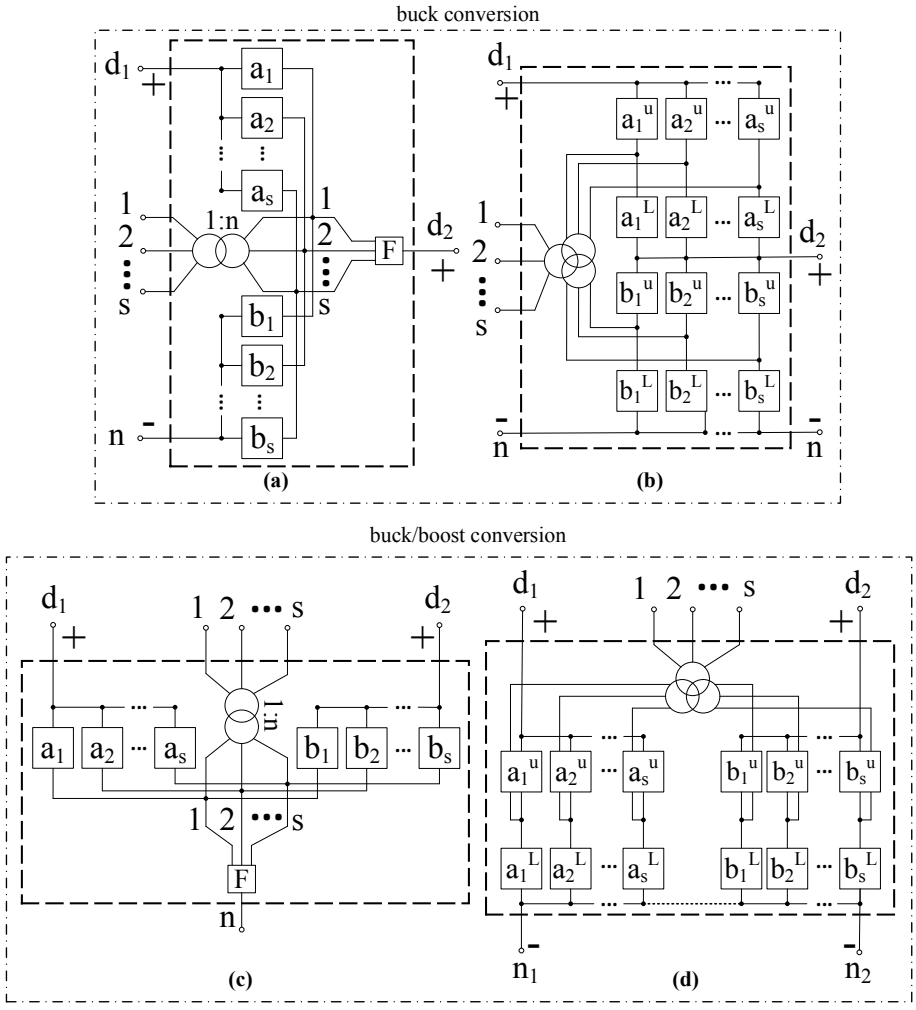

Figure 2.1: Generalized MP-DC2AC topologies; (a) MP-M2DC, (b) MP-AT [1], (c) MP-BB, and (d) MP-DAB [2]

is assumed to be ideal for both dc and ac grids, v) all converters are assumed to be balanced three phase ($\theta_j \in \{0, -2\pi/3, +2\pi/3\}$ for $j = 1, 2, 3$).

2.2.1 MP-M2DC and MP-BB

As shown in figure 2.2, transformed arm voltages and currents of MP-M2DC and MP-BB have similar functions. The transformation for the steady state arm currents is as follows

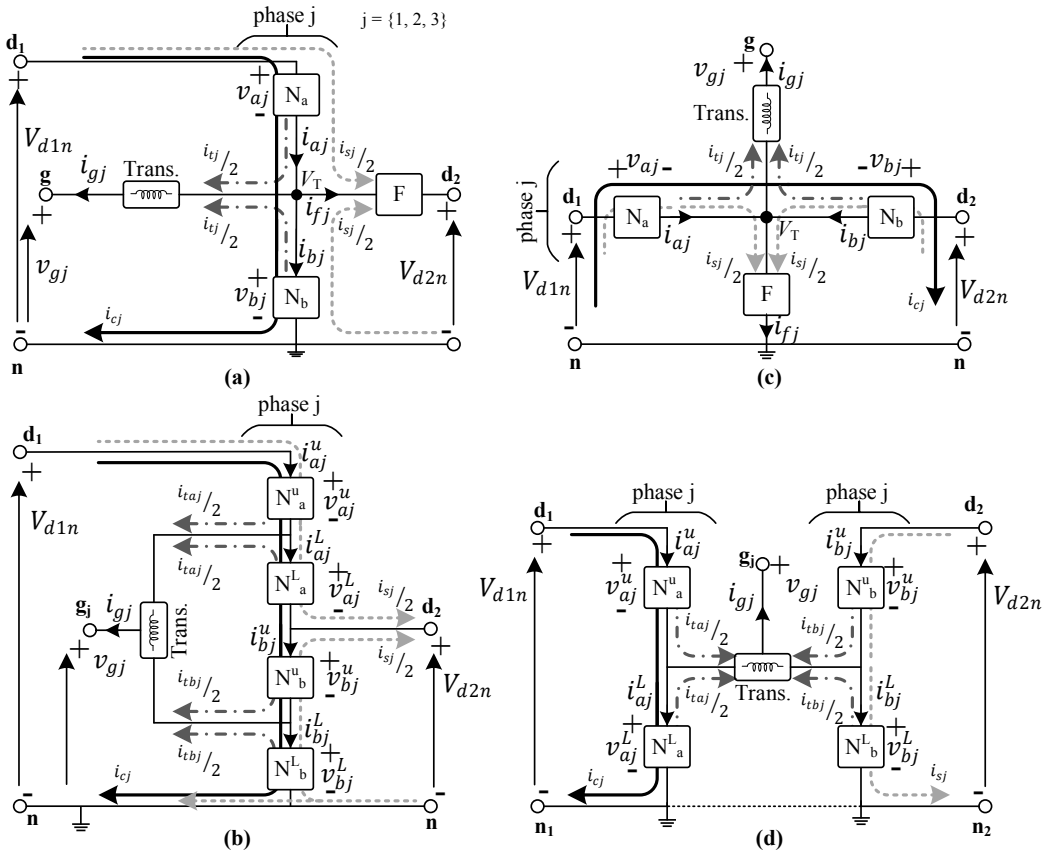

Figure 2.2: Single-phase circuit model of (a) MP-M2DC, (b) MP-AT, (c) MP-BB, (d) MP-DAB

$$\begin{bmatrix} i_{cj} \\ i_{tj} \\ i_{sj} \end{bmatrix} = \begin{cases} \begin{bmatrix} 0.5 & 0.5 & 0 \\ 1 & -1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{fj} \end{bmatrix} & \text{MP-M2DC} \\ \begin{bmatrix} 0.5 & -0.5 & 0 \\ 1 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_{aj} \\ i_{bj} \\ i_{fj} \end{bmatrix} & \text{MP-BB} \end{cases} \tag{2.1}$$

where the subscript "c" corresponds to the circulating quantities, whereas subscripts "t" and "s" are for terminal variables. Subscript "a" and "b" refers to arms and subscript "f" represents the filter variables.

Similarly for arm voltages the mapping is determined using the following transformation matrix:

$$\begin{bmatrix} v_{cj} \\ v_{tj} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \times \begin{bmatrix} v_{aj} \\ v_{bj} \end{bmatrix} \quad \text{MP-M2DC and MP-BB} \tag{2.2}$$

It should be noted that circulating current i_{cj} is generated when the signal voltage v_{cj} is imposed and likewise v_{tj} generates i_{tj} and i_{sj}. Since the DC voltage stepping ratio of MP-M2DC and MP-BB is different, the expression for DC and AC components are defined separately.

It is useful to capture all input, output, and state dynamics of an MMC-based converter. This is also helpful to derive a rapid time-domain simulation model of the converter. To address this, a dynamic model of MP-M2DC is given for a single phase converter that represents a large-signal dynamic model.

2.2.1.1 Dynamic Model Development

The average model of an individual SM in an MMC can be developed as shown in Figure 2.3, where "$v^n_{cap,kj}$" is the capacitor voltage of a SM "n", "C_{SM}" is the capacitance, "m^n_{kj}" the modulating signal associated with SM "n" in arm "k" of phase leg "j". "i_{arm}" is the current that flows in the arm. The value of "m^n_{kj}" ranges between 0 and 1 for HBSMs and for FBSMs it is -1 and 1.

Averaged arm voltage value as shown in Figure 2.3 can be approximated by a single composite arm comprised of N_{SM} connected in series. According to Figure 2.3, the capacitor voltage dynamics for a single SM, n can be expressed as follow:

$$\dot{v}^n_{cap,kj} = \frac{m^n_{kj}}{C_{SM}} i_{arm} \tag{2.3}$$

where $\dot{v}^n_{cap,kj}$ is the derivative of the capacitor voltage and summing (2.3) over

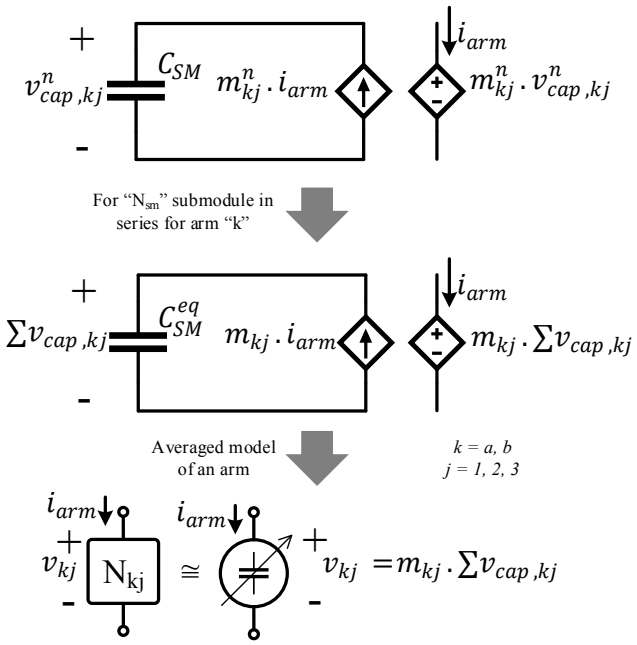

Figure 2.3: Averaged modeling of an arm built up of N_{SM} series stacked SMs with current i_{arm} and capacitor voltage $\Sigma v_{cap,kj}$ from a single SM.

n for all N_{SM} in one arm it becomes

$$\Sigma \dot{v}_{cap,kj} = \frac{m_{kj}}{C^{eq}_{SM}} i_{arm} \tag{2.4}$$

where $C^{eq}_{SM} = \frac{C_{SM}}{N_{SM}}$ is the equivalent capacitance for one arm. Equation (2.4) represents the dynamic model of an arm comprised of N_{SM} submodules in series. $\Sigma \dot{v}_{cap,kj}$ is the sum of SM capacitor voltages derivatives for arm k in phase leg j. The modulating signal is shown without a summation sign so that it reflects the conventional notation.

State equations for a single phase leg of MP-M2DC (shown in Figure 2.2(a)) are explored to capture circulating and terminal current dynamics. For this modeling the following assumptions are considered: 1) mutual inductance of zig-zag and coupling transformers are chosen to be very large, 2) switching frequency occurs at substantially higher order with respect to the fundamental frequency, 4) SM capacitor voltage sort and selection algorithm ensures voltage balancing amongst individual capacitors within each arm.

There are three independent voltage loops in Figure 2.2(a). Using Kirchhoff's Voltage Law, the converter current dynamics and their relation with arm voltages are derived. The state equations is expressed in a state space form as follows:

$$L.\dot{x}_i = A.x_i + B.u_v + N.w \tag{2.5}$$

where x_i is the current state vector, u_v is the input vector and w is the disturbance vector defined as follow:

$$x_i = [i_{aj}, i_{bj}, i_{fj}]^T \tag{2.6}$$

$$u_v = [v_{aj}, v_{bj}]^T \tag{2.7}$$

$$w = [V_{d1n}, v_{gj}, V_{d2n}]^T \tag{2.8}$$

the ac voltage v_{gj} is the rms single phase voltage of phase j. The coefficient matrices of state space equation (2.5) are given by:

$$L = \begin{bmatrix} L_a & L_a & 0 \\ L_a + 2L_T & -(L_a + 2L_T) & -2L_T \\ L_a & -L_a & L_f \end{bmatrix} \tag{2.9}$$

$$A = \begin{bmatrix} -R_a & -R_a & 0 \\ -(R_a + 2R_T) & (R_a + 2R_T) & 2R_T \\ -R_a & R_a & -R_f \end{bmatrix} \tag{2.10}$$

$$B = \begin{bmatrix} -1 & -1 \\ -1 & 1 \\ -1 & 1 \end{bmatrix} \quad N = \begin{bmatrix} 1 & 0 & 0 \\ 1 & -2 & 0 \\ 1 & 0 & -1 \end{bmatrix} \tag{2.11}$$

Equation (2.5) clearly shows the dynamic relations between the input vector u_v

and current states x_i and therefore by using appropriate controller the current state can be regulated.

For input vector u_v, it should be noted that this vector contains the capacitor voltage states. In total, the single phase modeling system has five states (three currents and two voltages). The relation between the u_v and capacitor voltage states is defined as the following:

$$u_v = diag(m).x_v \tag{2.12}$$

where

$$x_v = [\Sigma v^a_{capj}, \Sigma v^b_{capj}]^T \tag{2.13}$$

$$m = [m_{aj}, m_{bj}]^T \tag{2.14}$$

Using the sum and difference transformations defined in (2.1) and (2.2) for currents and arm voltages, respectively, the terminal and circulating components can be derived. Mapping of input vector u_v becomes:

$$L^*.\dot{x}^*_i = A^*.x^*_i + B^*.x^*_v + N.w \tag{2.15}$$

where

$$x^*_i = [i_{cj}, i_{tj}, i_{sj}]^T \tag{2.16}$$

$$x^*_v = [v_{cj}, v_{tj}] \tag{2.17}$$

and the coefficient matrices are given by

$$L^* = L.T_i^{-1} \quad A^*_{11} = A.T_i^{-1} \quad A^*_{12} = B.T_u^{-1}.M.T_u \tag{2.18}$$

T_i and T_u are the multiplication matrices defined in (2.1) and (2.2), respec-

tively

$$T_i = \begin{cases} \begin{bmatrix} 0.5 & 0.5 & 0 \\ 1 & -1 & -1 \\ 0 & 0 & 1 \end{bmatrix} & \text{MP-M2DC} \\ \\ \begin{bmatrix} 0.5 & -0.5 & 0 \\ 1 & 1 & -1 \\ 0 & 0 & 1 \end{bmatrix} & \text{MP-BB} \end{cases} \tag{2.19}$$

$$T_u = \begin{bmatrix} 0.5 & 0.5 \\ 0.5 & -0.5 \end{bmatrix} \text{ MP-M2DC and MP-BB} \tag{2.20}$$

Rearranging (2.12) and using the sum and difference matrix T_u, the transformed input vector u_v^* becomes

$$u_v^* = (T_u.diag(m).T_u^{-1})x_v^* \tag{2.21}$$

where

$$x_v^* = T_u.x_v = [v_{cj}, v_{tj}]^T \tag{2.22}$$

To make the notations consistent, the following (4×4) matrix is defined for the modulating signals:

$$M = T_u.diag(m).T_u^{-1} \tag{2.23}$$

and the transformed vector m^* is defined as follows

$$m^* = T_u.m = [m_{cj}, m_{tj}]^T \tag{2.24}$$

SM capacitor voltage dynamics can also be determined with the averaged model shown in Figure 2.3. The capacitor voltage state equation can be written as

$$\dot{x}_v = diag(m).C_{eq}.[i_{aj}, i_{bj}]^T \tag{2.25}$$

where

$$C_{eq} = \begin{bmatrix} 1/C^{eq}_{SM,a} & 0 \\ 0 & -1/C^{eq}_{SM,b} \end{bmatrix} \tag{2.26}$$

Using the transformation approach, the mapped capacitor voltage dynamics become:

$$\dot{x}^*_v = A_{21}.[i_{cj}, i_{tj}]^T \tag{2.27}$$

where

$$A_{21} = T_u.diag(m).C_{eq}.T_i^{-1} \tag{2.28}$$

Since the capacitor voltages are impacted by only two arm currents the resulting A^*_{21} which is a (3×3) matrix becomes $\begin{bmatrix} A_{21} & 0 \\ 0 & 0 \end{bmatrix}$.

Combining the current and capacitor voltage dynamics equations, the state space model for MP-M2DC becomes:

$$\begin{bmatrix} L^* & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \dot{x}^*_i \\ \dot{x}^*_v \end{bmatrix} = \begin{bmatrix} A^*_{11} & A^*_{12} \\ A^*_{21} & 0 \end{bmatrix} \begin{bmatrix} x^*_i \\ x^*_v \end{bmatrix} + \begin{bmatrix} N \\ 0 \end{bmatrix} w \tag{2.29}$$

Circulating and terminal currents take the following steady state values

based on their control principle:

$$i_{cj} = I_c/3 + \hat{I}_c cos(\omega t + \varphi_{ic} + \theta_j) \tag{2.30}$$

$$i_{tj} = \hat{I}_t cos(\omega t + \varphi_{it} + \theta_j) \tag{2.31}$$

$$i_{sj} = I_s/3 \tag{2.32}$$

For MP-M2DC the arm voltages are defined as follows

$$v_{cj} = \frac{V_{d1n}}{2} + \hat{V}_c cos(\omega t + \varphi_{vc} + \theta_j) \tag{2.33}$$

$$v_{tj} = \frac{V_{d1n}(1 - 2G_v)}{2} + V_t + \hat{V}_t cos(\omega t + \varphi_{vt} + \theta_j) \tag{2.34}$$

and for MP-BB the transformed arm voltages are given by

$$v_{cj} = \frac{(1 + G_v)V_{d1n}}{2} + V_t + \hat{V}_t cos(\omega t + \varphi_{vt} + \theta_j) \tag{2.35}$$

$$v_{tj} = \frac{V_{d1n}(1 - G_v)}{2} + \hat{V}_c cos(\omega t + \varphi_{vc} + \theta_j) \tag{2.36}$$

2.2.2 MP-DAB and MP-AT

Similar to the procedure done for MP-M2DC and MP-BB, the arm current and voltages of two topologies are transformed into a sum and difference frame that provides virtual states for analysis and control system implementation. Based on the single line diagram shown in Figures 2.2(b) and (d), respectively for MP-AT and MP-DAB the arm currents become

$$\begin{bmatrix} i_{cj} \\ i_{taj} \\ i_{tbj} \\ i_{sj} \end{bmatrix} = \begin{bmatrix} 0.25 & 0.25 & 0.25 & 0.25 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0.5 & 0.5 & -0.5 & -0.5 \end{bmatrix} \begin{bmatrix} i_a^u \\ i_a^L \\ i_b^U \\ i_b^L \end{bmatrix} \quad \text{MP-AT} \tag{2.37}$$

$$\begin{bmatrix} i_{cj} \\ i_{taj} \\ i_{tbj} \\ i_{sj} \end{bmatrix} = \begin{bmatrix} 0.5 & 0.5 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} i_a^u \\ i_a^L \\ i_b^U \\ i_b^L \end{bmatrix} \qquad \text{MP-DAB} \qquad (2.38)$$

and the arm voltages are as follow

$$\begin{bmatrix} v_{cj} \\ v_{taj} \\ v_{tbj} \\ v_{sj} \end{bmatrix} = \begin{bmatrix} 0.25 & 0.25 & 0.25 & 0.25 \\ 0.5 & -0.5 & 0 & 0 \\ 0 & 0 & 0.5 & -0.5 \\ 0.25 & 0.25 & 0.25 & 0.25 \end{bmatrix} \begin{bmatrix} v_a^u \\ v_a^L \\ v_b^u \\ v_b^L \end{bmatrix} \qquad \text{MP-AT} \qquad (2.39)$$

$$\begin{bmatrix} v_{cj} \\ v_{taj} \\ v_{tbj} \\ v_{sj} \end{bmatrix} = \begin{bmatrix} 0.5 & 0.5 & 0 & 0 \\ 0.5 & -0.5 & 0 & 0 \\ 0 & 0 & 0.5 & -0.5 \\ 0 & 0 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} v_a^u \\ v_a^L \\ v_b^u \\ v_b^L \end{bmatrix} \qquad \text{MP-DAB} \qquad (2.40)$$

Note that unlike MP-M2DC and MP-BB where their arm current and voltage states are not equal (e.g. 3 current states and 2 voltage states), MP-AT and MP-DAB have the same number of arm current and voltage states (4 current states and 4 voltage states) for four arms. Also, note that the virtual circulating and terminal currents and voltages for MP-DAB are decoupled for two MMCs due to the galvanic separation existence.

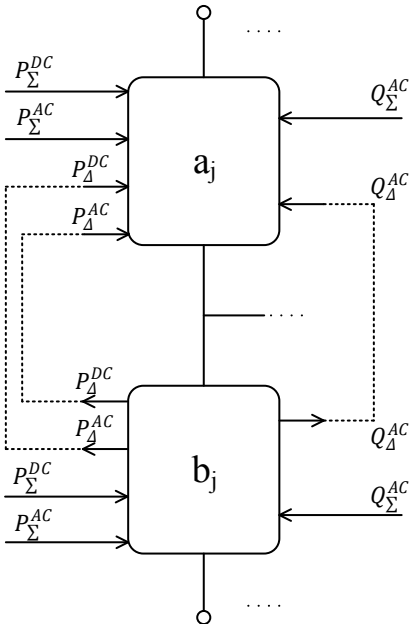

Figure 2.4: Power Flow Components of active power ((2.41), (2.42)) and reactive power ((2.47), (2.48)) equations for single phase leg of MP-M2DC

2.3 Steady State Power Flow Equations: MP-M2DC and MP-BB

Figure 2.4 illustrates the power flow directions defined for active power and reactive power components. The power flow terms are derived from the multiplication of arm voltages and currents defined in (2.1) and (2.2). A small V_t is required to generate the dc current i_s and hence it can be neglected in steady state power flow definitions. Similarly, to drive the ac component of i_c a small common voltage $\hat{V}_c$ common between both arms is needed to allow average ac power transfer and this common ac voltage can also be disregarded.

The steady state power flow equations are explained for MP-DC2AC and MP-BB and can be extended for the other two topologies. The single phase steady state active power P_{aj} and P_{bj}, respectively for arms "a" and "b" in

Figure 2.2(a) and (c) are given by

$$P_{aj} = \overbrace{P_{\Sigma}^{DC} + P_{\Sigma}^{AC}}^{DC-AC} + \overbrace{P_{\Delta}^{DC} + P_{\Delta}^{AC}}^{DC-DC} \tag{2.41}$$

$$P_{bj} = \overbrace{P_{\Sigma}^{DC} + P_{\Sigma}^{AC}}^{DC-AC} - (\overbrace{P_{\Delta}^{DC} + P_{\Delta}^{AC}}^{DC-DC}) \tag{2.42}$$

$$P_{\Sigma}^{DC} = \begin{cases} \frac{V_{d1n}}{6}[I_c + (1-2G_v)\frac{I_s}{2}] & \text{MP-M2DC} \\ \frac{V_{d1n}}{6}[(1-G_v)I_c + (1+G_v)\frac{I_s}{2}] & \text{MP-BB} \end{cases} \tag{2.43}$$

$$P_{\Delta}^{DC} = \begin{cases} \frac{V_{d1n}}{6}[(1-2G_v)I_c + \frac{I_s}{2}] & \text{MP-M2DC} \\ \frac{V_{d1n}}{6}[(1+G_v)I_c + (1-G_v)\frac{I_s}{2}] & \text{MP-BB} \end{cases} \tag{2.44}$$

$$P_{\Sigma}^{AC} = \frac{\hat{V}_t\hat{I}_t}{2}cos(\varphi_{vt} - \varphi_{it}) \tag{2.45}$$

$$P_{\Delta}^{AC} = \frac{\hat{V}_t\hat{I}_c}{2}cos(\varphi_{vt} - \varphi_{ic}) \tag{2.46}$$

The steady state reactive power relationships of the arms in both topologies are as follow

$$Q_{aj} = \overbrace{\frac{\hat{V}_t\hat{I}_c}{2}sin(\varphi_{vt} - \varphi_{ic})}^{Q_{\Delta}} + \overbrace{\frac{\hat{V}_t\hat{I}_t}{2}sin(\varphi_{vt} - \varphi_{it})}^{Q_{\Sigma}} \tag{2.47}$$

$$Q_{bj} = -\overbrace{\frac{\hat{V}_t\hat{I}_c}{2}sin(\varphi_{vt} - \varphi_{ic})}^{Q_{\Delta}} + \overbrace{\frac{\hat{V}_t\hat{I}_t}{2}sin(\varphi_{vt} - \varphi_{it})}^{Q_{\Sigma}} \tag{2.48}$$

The subscript "Σ" is used for **dc-ac** power flow equations and "Δ" is for **dc-dc** power flow relationships. The power flow principle for MP-DAB and MP-AT is extension version of the mechanism explained for MP-M2DC and is

not explained in detail.

Based on the principle that the total average power of a switch cell must be zero [50], this yields that according to (2.42), the average power absorbed by the arms must be zero to avoid capacitor charge imbalance and instability. While dc-ac average power is transferred (P_{Σ}^{AC}), a dc power (P_{Σ}^{DC}) is compensated to re-establish the charge of capacitors to maintain nominal voltage. For dc-dc power transfer (P_{Δ}^{DC}), an average power (P_{Δ}^{AC}) is exchanged between subconverters to keep capacitor voltage differences minimized.

The P_{Σ} terms represent average power that is equally absorbed by the two arms, which is associated with conventional dc-ac conversion [49]. The P_{Δ} terms represent average power that is delivered from one arm to the other, which is associated with single-stage dc-dc conversion [22, 51]. Superscripts "dc" and "ac" mean the associated P_{Σ}, P_{Δ} terms are respectively due to dc and fundamental frequency quantities. Steady-state capacitor power balance implies that $P_{\Sigma}^{dc} + P_{\Sigma}^{ac} = 0$ (dc-ac conversion) and $P_{\Delta}^{dc} + P_{\Delta}^{ac} = 0$ (dc-dc conversion).

For dc-ac conversion, P_{Σ}^{dc} is the average power transferred to both arms from the dc link, and P_{Σ}^{ac} is the average ac power absorbed by both arms from the ac grid. For dc-dc conversion, P_{Δ}^{dc} is the average power imbalance between arms caused by sending dc power from ports d_1 to d_2, and P_{Δ}^{ac} is the average ac power exchanged between arms to counteract this charge imbalance.

Equations (2.45) and (2.46) reveal that the ac components of i_{tj} and i_{cj} can be controlled to independently regulate the arm capacitor voltages for dc-ac and dc-dc conversions, respectively. As a corollary, the MP-M2DC and MP-BB can independently regulate power transfer between any combination of its three ports d_1, d_2, and ac. In (2.45) and (2.46), $\hat{V}_t$ is the ac terminal voltage synthesized by the converter.

2.4 Phasor Diagram Representation

Phasor diagram for dc-dc and dc-ac power transfer can be realized. The converter ac quantities are represented with RMS phasors assuming that i) the whole system has a constant ac frequency (50/60 Hz), ii) the dynamics are neglected during steady state operation, and iii) the three phase system is symmetrically balanced.

There are two rotating reference frames for terminal (dq) and circulating quantities ($d'q'$) that rotate at the same angular speed as shown in figure 2.5(a). Ac terminal values, such as v_t and i_t, are transformed into the reference frame that is synchronized with the ac grid voltage V_g and circulating quantities are transformed into a reference frame that rotates at the same angular speed as the terminal reference frame, but with the phase shifting of the terminal ac voltage V_t and the transformer.

Since all three phasor values are transformed into the dq0 rotating reference frame (the dc variables comprise the 0 components), the instantaneous arm currents and voltages for phase $j = 1$ are given by

$$i_{c1}(t) = I_{c0} + \overbrace{\hat{I}_c cos(\varphi_{ic})}^{I_{cd'}} cos(\omega t) - \overbrace{\hat{I}_c sin(\varphi_{ic})}^{I_{cq'}} sin(\omega t) \tag{2.49}$$

$$i_{t1}(t) = \overbrace{\hat{I}_t cos(\varphi_{it})}^{I_{td}} cos(\omega t) - \overbrace{\hat{I}_t sin(\varphi_{it})}^{I_{tq}} sin(\omega t) \tag{2.50}$$

$$i_{s1}(t) = I_{s0} \tag{2.51}$$

$$v_{c1}(t) = V_{c0} + \overbrace{\hat{V}_c cos(\varphi_{vc})}^{V_{cd'}} cos(\omega t) - \overbrace{\hat{V}_c sin(\varphi_{vc})}^{V_{cq'}} sin(\omega t) \tag{2.52}$$

$$v_{t1}(t) = V_{t0} + \overbrace{\hat{V}_t cos(\varphi_{vt})}^{V_{td}} cos(\omega t) - \overbrace{\hat{V}_t sin(\varphi_{vt})}^{V_{tq}} sin(\omega t) \tag{2.53}$$

$$v_{g1}(t) = V_{gd} cos(\omega t) \tag{2.54}$$

where V_{c0} and V_{t0} are the dc components of $v_{cj}(t)$ and $v_{tj}(t)$, respectively as represented in the former arm voltage definitions.

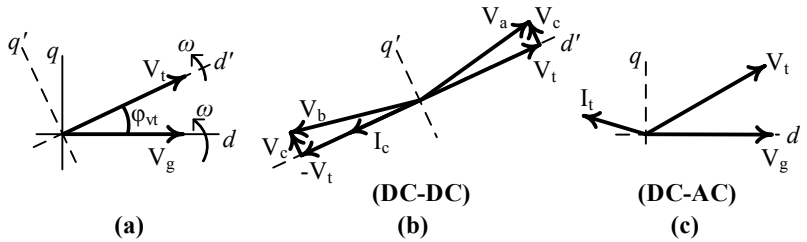

Figure 2.5: (a) MP-M2DC and MP-BB rotating reference frames dq (DC-AC conversion) and $d'q'$ (DC-DC conversion), (b) AC quantities facilitating DC-DC conversion, drawn for MP-M2DC, (c) AC quantities facilitating DC-AC conversion, drawn for MP-M2DC

To better illustrate phasor representation of MP-DC2AC MMCs, a multi-port power flow example is explained here where the ac phasors are represented for dc-dc ($d_1 \rightarrow d_2$) in Figure 2.5(b) and dc-ac power transfer ($d_1 \rightarrow ac$) shown in Figure 2.5(c).

For dc-dc power transfer, the dc component of v_{tj} (V_t) is added to one subconverter and subtracted from the other subconverter (based on the direction of the dc-dc power flow) to allow the output dc current to flow. V_t is proportional to the resistance of the arms and zig-zag filter. Since the resistances are assumed to be very small, V_t is neglected in analysis. To compensate the dc power exchanged between dc ports, a common mode ac voltage (V_c) on quadrature axis (q') is synthesized to both subconverters for internal average ac power exchange. This quadrature ac voltage injects an ac current in direct axis and allows active power transfer between arms. This power flow mechanism regulates the charge difference between arms. For dc-ac power flow, the terminal ac voltage of the converter V_t is phase shifted with respect to the secondary sided ac grid voltage V_g' and the power flow mechanism is analogous to a simple two-level VSC.

2.5 Arms Modulation

Arm modulation builds the required ac voltage to enable average power exchange between arms and the terminals (internal and external average power).

Hence for the sake of a cost efficient power transfer, the current stress of the arms should be minimized (i.e. the generated ac voltage be maximized). It is valid to reserve a satisfactory margin for the ac voltage for transient dynamics (typically 5 %).

Ac voltage magnitude of the arms is impacted by galvanic isolation of the arms. In the case of MP-DC2AC MMCs, for MP-M2DC (and MP-BB) the ac voltages for the pair of arms are equal and the number of SMs to be installed to support the ac voltage for the arms in one phase leg could therefore be equal. In contrast, for MP-DAB (and MP-AT), the ac voltage synthesized on one MMC side is galvanically separated from the secondary one due to the presence of a transformer path for ac current circulation. Therefore, galvanic separation mechanism provides a degree of freedom to independently change ac voltage of subconverter terminals.

If only HBSMs are used then the ac voltage is able to swing between zero and the maximum dc voltage supported by cells. It should be noted that the ac voltage is limited to the minimum dc voltage supported by arms in one phase leg. For instance, if in MP-M2DC the dc voltage of the upper arm in one leg supports 100 kV dc and the lower arm supports 50 kV dc, then the ac voltage that can be supported by the arms is 50 kV. Of course it is possible to increase this ac voltage by implementing FBSMs.

As discussed in section 2.2.1.1, the arm voltage is a multiplication of the modulating signal generated by the control system and the sum of capacitor voltages over a period of time. It is represented as the following

$$v_{arm}^{k} = \hat{m}^{k}.\Sigma V_{capj}^{k} \qquad k = a, b \; and \; j = 1, 2, 3 \tag{2.55}$$

v_{arm}^{k} is the arm voltage of arm k in phase leg j, $\hat{m}^{k}$ is the modulating signal that consists of dc, fundamental frequency, second harmonic and even higher terms, ΣV_{capj}^{k} is the sum of capacitor voltage of arm k in phase leg j. During

the steady state, the capacitor voltage is a constant value with some voltage ripple and therefore by controlling the modulating signal, the arm voltage is adjusted for both circulating and terminal power exchanges.

The modulating signal is composed of two components: i) circulating, $\hat{m}_{cj}^{k}$ and ii) terminal, $\hat{m}_{tj}^{k}$ variables. For certain power transfer mechanism and/or circulating harmonic suppression circulating and terminal components are generated.

2.6 Proposed Dynamic Controller

A dynamic controller is presented that can be applied for power flow between different ports and keeping the arm capacitor voltages balanced. The detailed modeling of the proposed controller is given for MP-M2DC and MP-BB.

The controller is represented for voltage stepping ratios $G_v = 0.5$ and $G_v = 1$ for MP-M2DC and MP-BB, respectively.

2.6.1 Controller for MP-M2DC and MP-BB

MP-M2DC is a unique structure and by re-configuring the topology, other MP-DC2AC MMCs can be developed. For instance, by rotating the topology and replacing the terminal connection ports (and accordingly flip the polarity of "b" arms), MP-BB is derived. In MP-AT and MP-DAB, the filter can be removed to operate akin to the conventional dc-ac MMC. By connecting two dc-ac MMCs through a galvanic separation, MP-DAB is developed and lastly series stacking two conventional dc-ac MMCs and connecting their ac terminals using a transformer MP-AT is comprised. Therefore, the controller that is used for MP-M2DC is simply modified/replicated for other three topologies and this is an interesting aspect of the proposed controller for MP-M2DC.

While ensuring capacitor voltages are balanced, a dynamic controller is proposed that can be used for both MP-M2DC and MP-BB allowing independent

power transfer between any combination of the three ports (d_1, d_2, ac). This controller is illustrated in Figure 2.6 at $G_v = 0.5$ and $G_v = 1$ for MP-M2DC and MP-BB, respectively. The control is implemented using the $dq0$ and $d'q'0$ reference frames as shown in Figure 2.5. Most of the control principles for MP-BB and MP-M2DC are in common, except the currents I_{c0} and I_{s0} have different control objectives in each topology. The control for these two currents are shown in red text in Figure 2.6 for MP-BB.

The three phase controlled currents and voltages in (2.1) and (2.2) are transformed into the rotating $dq0$ and $d'q'0$ reference frames. A phase locked loop (PLL) is utilized to synchronize with the external ac grid during normal operation for $dq0$ reference frame. A second PLL is not needed to synchronize $d'q'$ quantities (dc-dc) with ac terminal voltage $\vec{V}_t$, as this voltage is synthesized by the converter and thus the phase angle information can be readily extracted from control terms M_{td} and M_{tq}. During ac grid outage due to faults or maintenance, a VCO is utilized to provide a fixed sawtooth angle. PI controllers for currents (PI_i) and voltages (PI_v) are utilized to compensate the error of the respective variables. The controller diagram applies for MP-BB by replacing only the red variables as shown in Figure 2.6. $L^c_{d'q'}$ and L^t_{dq} are equivalent inductance and are determined as follow

$$L^c_{d'q'} = L_a \qquad L^t_{dq} = L_a/2 + L_T \tag{2.56}$$

where L_T is the ac grid interface transformer leakage inductance. Low-pass filters are used for both arm voltages and currents to attenuate switching harmonics at higher frequencies.

2.6.2 Control Objectives

To regulate the currents for power exchange between arms to: 1) transfer power between ports and 2) maintain SM capacitor voltages at their nominal values,

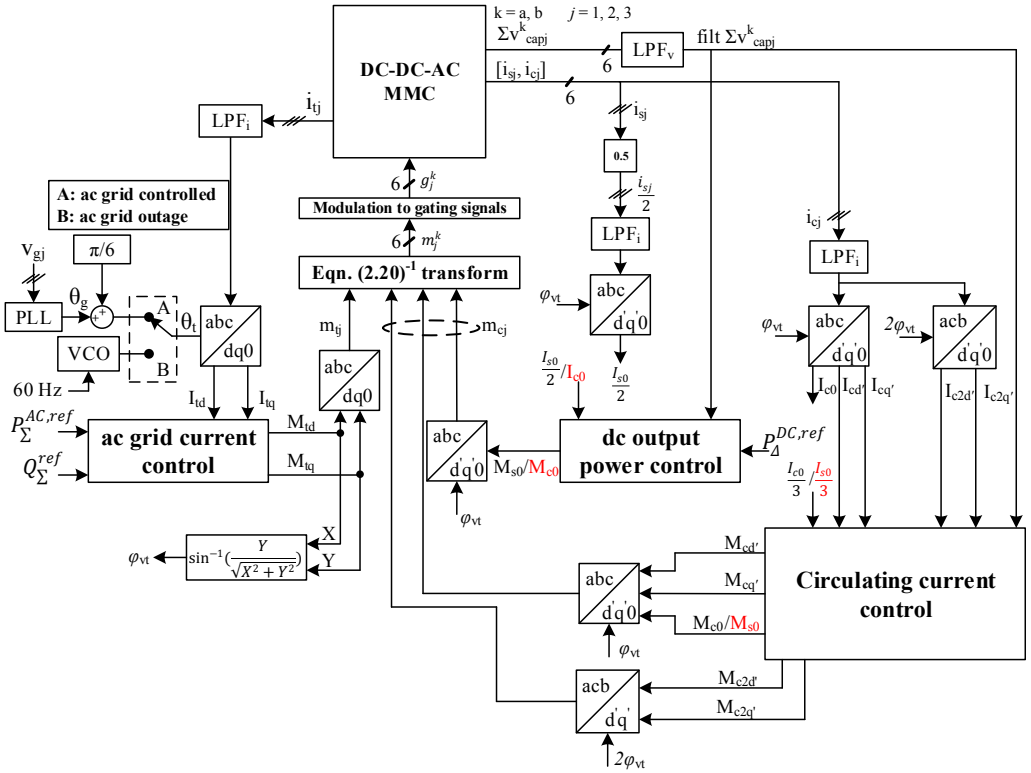

Figure 2.6: Control diagram of MP-M2DC and MP-BB for simultaneous DC-DC and DC-AC power flow, the red tags are for variables that are changed for MP-BB.

different controllers are defined. The controllers are tuned for specific control objectives. State arm capacitor voltages and currents explained in (2.29) clearly show the relationship between input variables (i.e. modulating signals) and states. To control the transformed current states shown in equation (2.1), the corresponding voltages need to be generated. The parameters associated with the circulating current controller is then derived from (2.29) for each KVL loop.

The following control objectives are considered as principle for MP-DC2AC MMCs

- Regulate the common mode component of SM capacitor voltages, ΣV_{cap},

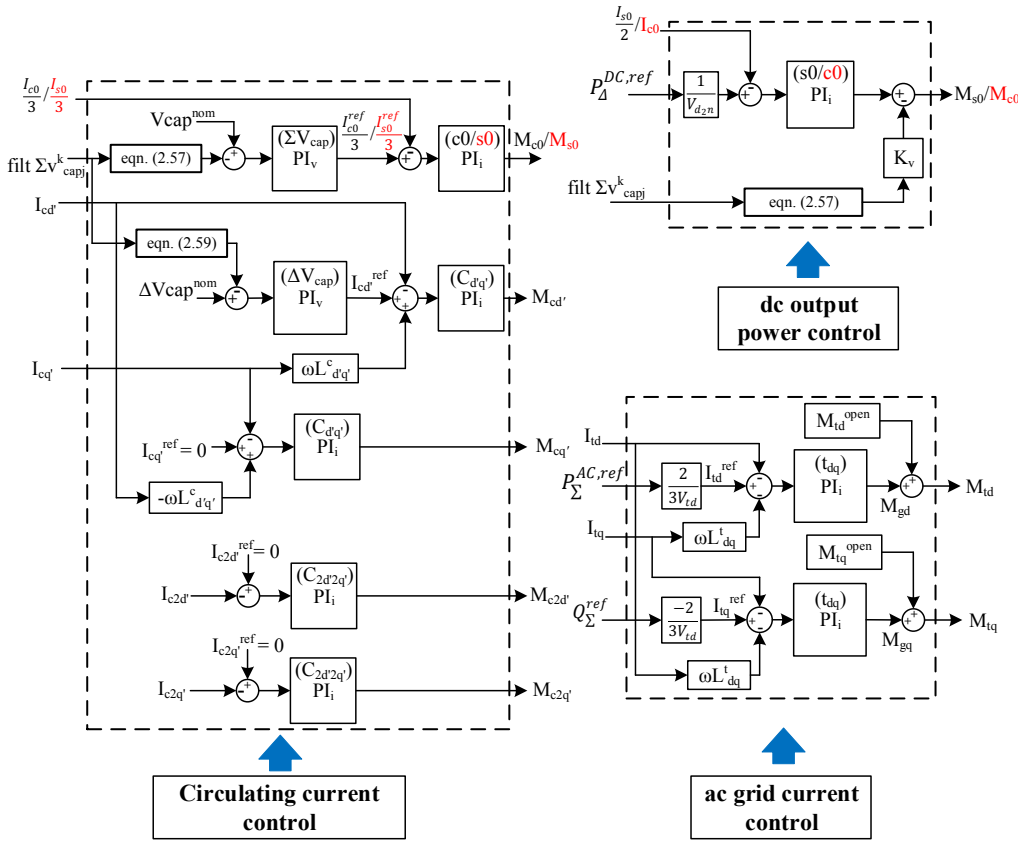

Figure 2.7: Details of utilized controllers in Figure 2.6

to its nominal value, ΣV_{cap}^{nom}, where

$$\Sigma V_{cap} = \frac{1}{6}[\sum_{j}^{1,2,3} \Sigma V_{capj}^{a} + \sum_{j}^{1,2,3} \Sigma V_{capj}^{b}] \tag{2.57}$$

$$\Sigma V_{cap}^{nom} = \frac{N_a V_{SM}^{nom} + N_b V_{SM}^{nom}}{2} \tag{2.58}$$

This is done by regulating the appropriate 0-axis current. It is assumed that "a" and "b" arms employ the same number of SMs, and that the nominal voltage of each SM capacitor is the same.

- Regulate the differential mode component of SM capacitor voltages, ΔV_{cap},

to its nominal value, ΔV_{cap}^{nom}, where

$$\Delta V_{cap} = \frac{1}{6}[\sum_{j}^{1,2,3} \Sigma V_{capj}^{a} - \sum_{j}^{1,2,3} \Sigma V_{capj}^{b}] \tag{2.59}$$

$$\Delta V_{cap}^{nom} = \frac{N_a V_{SM}^{nom} - N_b V_{SM}^{nom}}{2} \tag{2.60}$$

This is done by regulating $I_{cd'}$ to impose the requisite average ac power exchange between arms. $I_{cq'}$ is regulated to zero to avoid unecessary reactive power circulation

- Ac modulation indices M_{td} and M_{tq} provide independent control of the grid active and reactive power injections, respectively, similar to the conventional dc-ac MMC.

- Proportional gain K_v is added to improve output current dynamic response [51].

A comprehensive simulation study for different power flow scenarios is explained in Chapter 3.

2.6.3 Adapting Controller for MP-DAB and MP-AT

If we take the controller utilized for MP-M2DC and implement it for two MMCs in MP-DAB and MP-AT independently, then the converter is capable of multi-port power transfer between dc and ac ports. Note that the implementation of the controllers requires re-tuning of controller parameters based on MP-DAB and MP-AT configuration. In this case, the ac grid acts as a sink node and the control for power transfer is through the terminals of two dc systems. Detailed mathematical expression for power flow between three ports of MP-AT and MP-DAB is explained in [44].

Figure 2.8 illustrates the controller implementation for MP-DAB and MP-AT. As shown, the power transfer to each port can be shared independently

between two MMCs using the controller in Figure 2.6. Further details of power transfer capability of MP-DAB and MP-AT are presented in simulation study Chapter 3. [1]

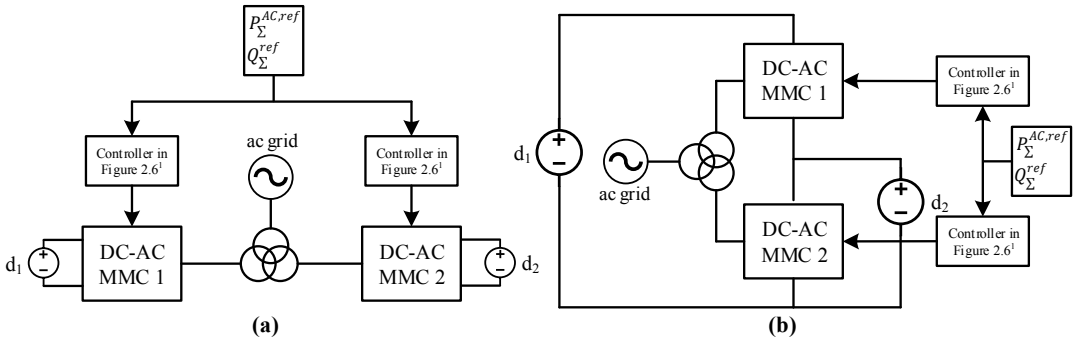

Figure 2.8: Proposed controller configuration for (a) MP-DAB and (b) MP-AT converters

[1]The controllers implemented do not have the dc output power control in Figure 2.7

Chapter 3

Simulation Results

The bidirectional power flow capability of three-phase switched models of MP-M2DC, MP-BB, MP-AT, and MP-DAB are tested in simulation platform (using PLECS) and the proposed dynamic controller is evaluated. Four different power flow scenarios are tested and arm current and voltages of converters are illustrated. A reduced size of MP-M2DC is also described and power flow simulations are presented.

3.1 Bidirectional Power Flow Validation

The converters are designed that each converter is capable of transferring rated power at all three ports (i.e. d_1, d_2, and ac). A delta-wye three phase transformer with similar structure represented in [52] is utilized to interface the ac grid. A three phase zig-zag transformer is equipped for the filter (F) block as illustrated in Figure 2.1(c) [18].

The circuit parameters of both MP-M2DC and MP-BB are given in Table 3.1. The parameters in MP-M2DC case study are chosen based on data available in the CIGRE working group B4-52 report [53]. The parameters for MP-BB are selected based on the converter design in [32]. Voltage balancing of capacitor voltages within an arm is achieved using the sorting and selection

algorithm [54].

Table 3.1: Simulation parameters for MP-M2DC and MP-BB

Parameters	MP-M2DC	MP-BB
$V_{d_1 n}$	500 kV	400 kV
V_g, n_T	300kV, 0.8	320kV, $\frac{1}{\sqrt{3}}$
G_v	0.5	1
L_a, L_{in}, L_{out}	$50, 82.73, 82.73$ mH	$75, 65.6, 65.6$ mH
R_a, R_{in}, R_{out}	$0.366, 1.33, 1.33$ Ω	$0.466, 2.66, 2.66$ Ω
ω	$2\pi \times 60$ rad/s	$2\pi \times 60$ rad/s
N_a, N_b	10, 10	20, 20
V_{SM}^{nom}, C_{SM}	50 kV, 2.4 mF	40 kV, 4 mF
X_T, X_F, I_{mT}, I_{mF}	12%, 12%, 1%, 1%	10%, 10%, 1%, 1%

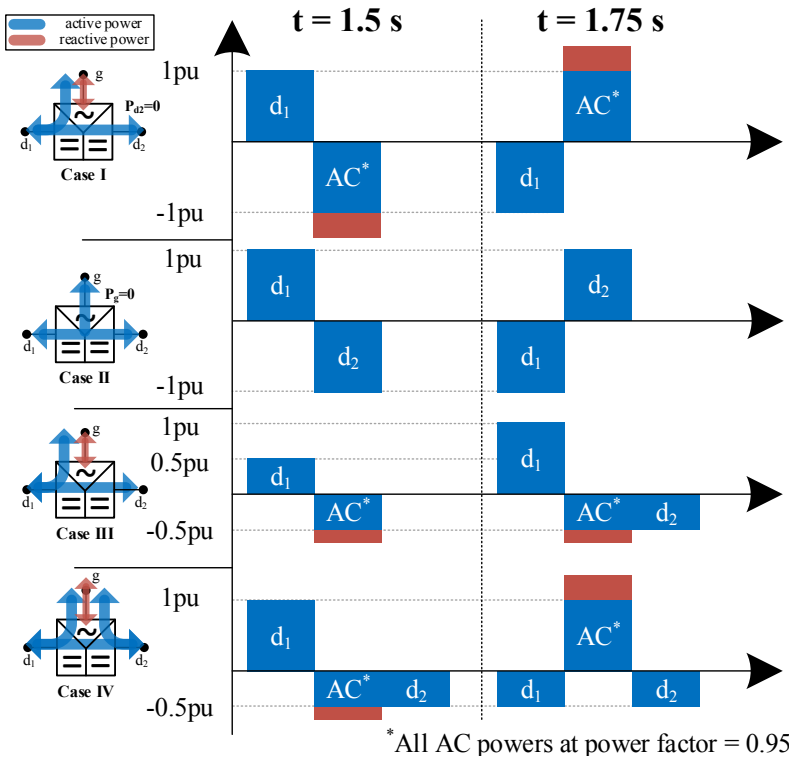

Figure 3.1: Four Case Study Scenarios for MP-DC2AC MMCS

3.1.1 Simulation results for MP-M2DC and MP-BB

Four test cases as shown in Figure 3.1 are run to test the performance of MP-M2DC and MP-BB using the proposed controller in Figure 2.6. These cases

demonstrate various possible power flows between the three ports (d_1, d_2, ac) of MP-M2DC and MP-BB to test the proposed dynamic controller. Cases I and II test solely the dc-ac and dc-dc conversion respectively, whereas in cases III and IV a combination of dc-dc and dc-ac power flow conversion is verified. The active power flow is exchanged with the ac grid at power factor of 0.95 lagging.

Figure 3.2 (case I) shows bidirectional power transfer of 1 pu between d_1 and the AC grid where at $t = 1.5s$ the direction of power is ($d_1 \rightarrow ac$), and then the direction of power flow is reversed at $t = 1.75s$ ($d_1 \leftarrow ac$). It is clear from dc port current plots that during steady state no power is delivered to d_2. Case I proves the capability of MP-DC2AC to operate dc-ac akin to a conventional dc-ac MMC.

Figure 3.3 (Case II) displays bidirectional dc-dc conversion between dc ports and since similar number of cells is equipped in each arm of a phase leg, the dynamics of capacitor voltage look symmetrical. The dynamic performance of the proposed controller is verified in Figure 3.3 for Case II as the capacitor voltages and arm current dynamics are similar to [32]. Case II proves the capability of MP-DC2AC MMC to operate purely as a dc-dc converter.

Figure 3.4 case III verifies dc-dc-ac power transfer capability of MP-DC2AC MMCs by first applying a 0.5 pu dc-ac conversion at $t = 1.5s$ from d_1 to the ac grid, and then an additional 0.5 pu power from d_1 to d_2 at $t = 1.75s$.

Figure 3.4 case IV demonstrates 1.0 pu power transfer from d_1 that is split equally between the AC grid (0.5 pu) and d_1 (0.5 pu) at $t = 1.5s$ (DC-DC-AC conversion), and then d_1 and d_2 are each commanded to deliver 0.5 pu power to the AC grid (for total of 1.0 pu) at $t = 1.75s$ (DC-DC-AC conversion). During all four cases, capacitor voltages are well balanced.

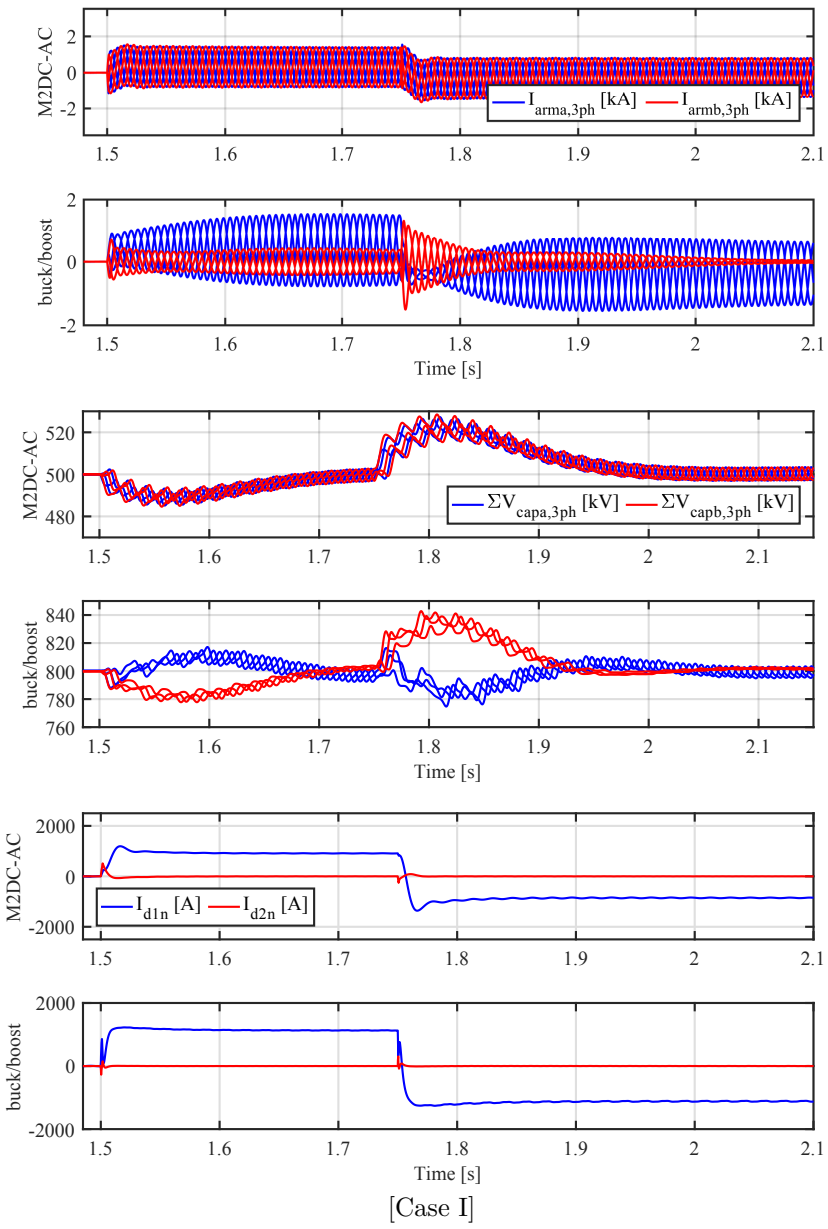

Figure 3.2: Case I Case I dc-ac: At t = 1:5s 1 pu power transfer with power factor 0.95 lagging from d1 to the ac grid, and at t = 1:75s the direction is reversed. (a) arm currents (b) sum of capacitor voltages (c) dc port currents

3.1.2 Simulation results for MP-AT and MP-DAB

In this section, the proposed controller is tested for the same power flow cases illustrated in Figure 3.1 for MP-AT ($G_v = 0.5$) and MP-DAB ($G_v = 1$). The controller is applied independently for each MMC of two converters and the power flow mechanism is similar to the one explained in [44]. Note that for

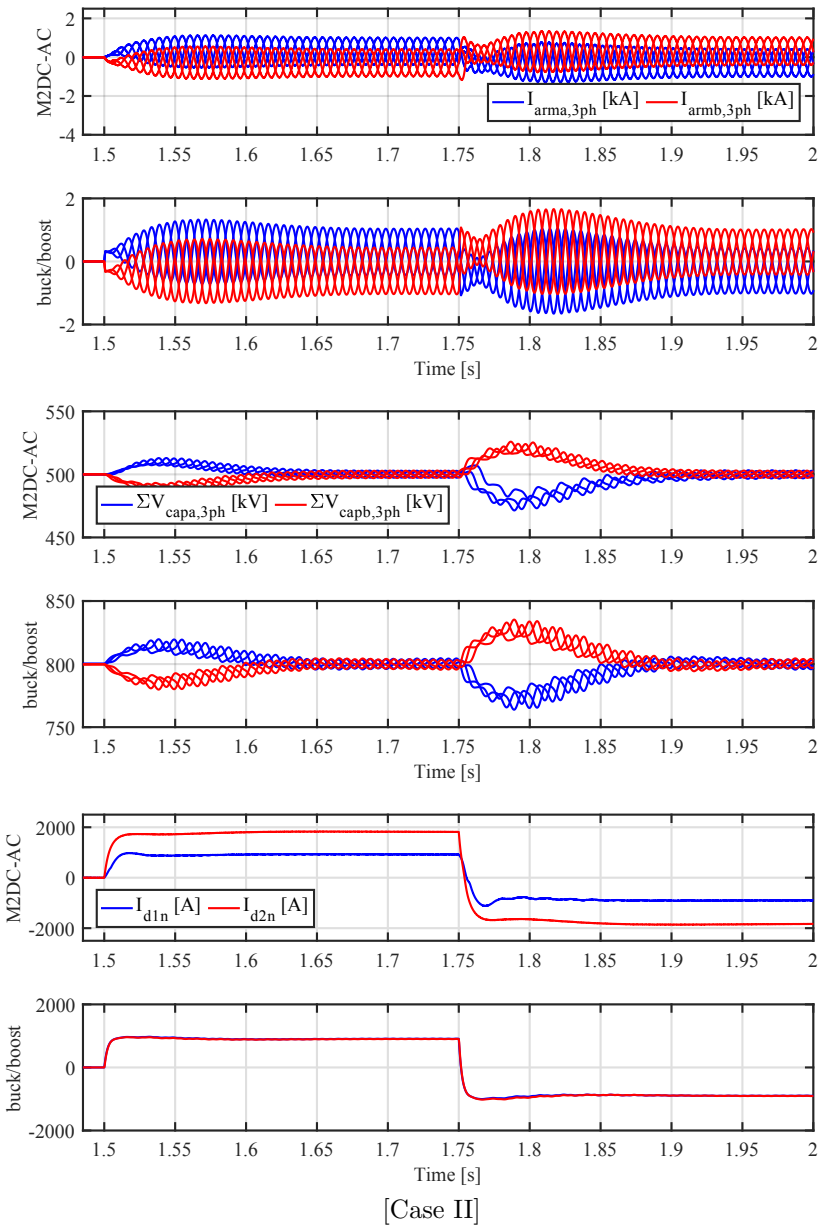

Figure 3.3: Case II dc-dc: At t = 1.5s 1 pu power transfer from d1 to d2, and at t = 1.75s the direction is reversed. (a) arm currents (b) sum of capacitor voltages (c) dc port currents

these two converters the ac grid is assumed to be the sink node and therefore there is no need for an output dc current control loop. Parameters used for MP-AT and MP-DAB is depicted in Table 3.2. The rated active power for both topologies is considered to be 450 MW.

Figure 3.6, shows case I for MP-DAB. Due to the three winding transformer, a coupling and correlation dynamics exist between three ports as shown in this

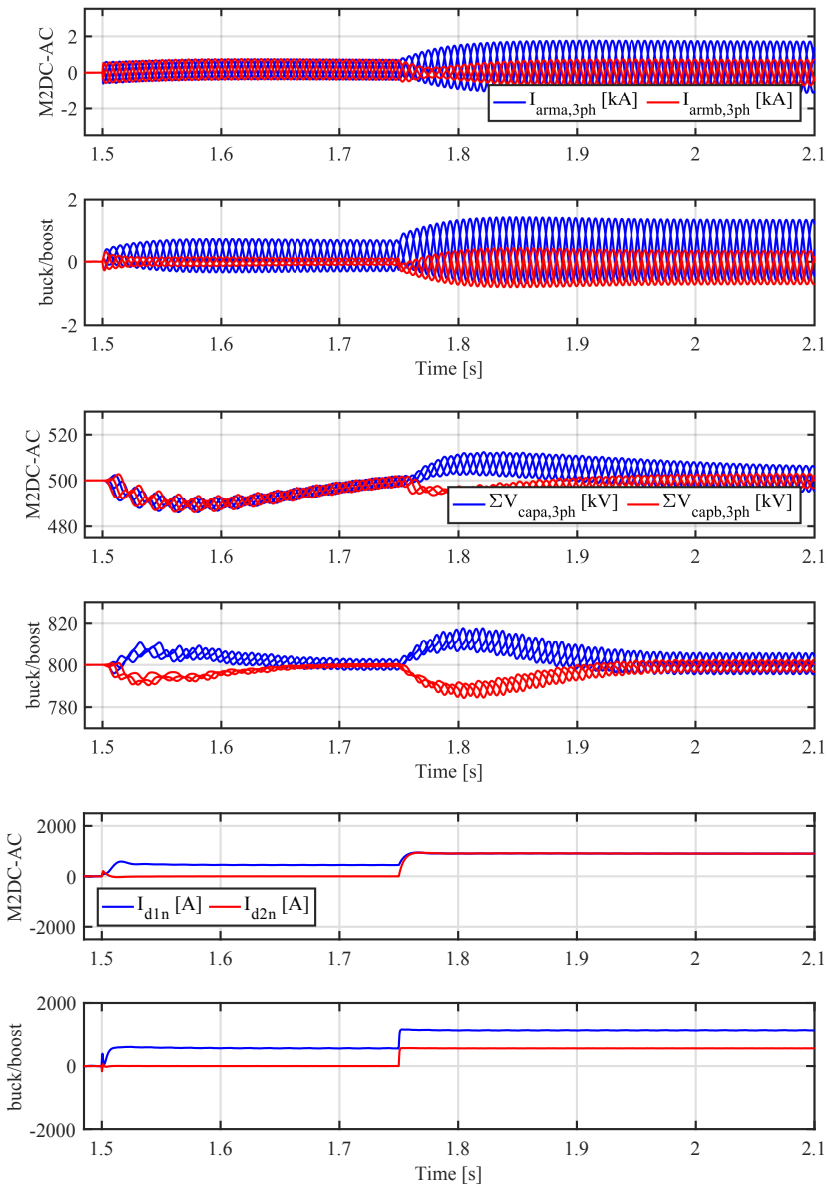

Figure 3.4: Case III dc-dc-ac: At t = 1.5s 0.5 pu power transfer with power factor 0.95 lagging from d1 to ac grid, and at t = 1.75s an additional 0.5 pu power is sent from d1 to d2 (total power injection into d1 is 1.0 pu). (a) arm currents (b) sum of capacitor voltages (c) dc port currents

figure arm current and capacitor voltages have a temporary dynamics when power step change is applied and then decays to their reference values during steady state.

In case II of MP-DAB shown in figure 3.7, two MMCs of the converter oper-

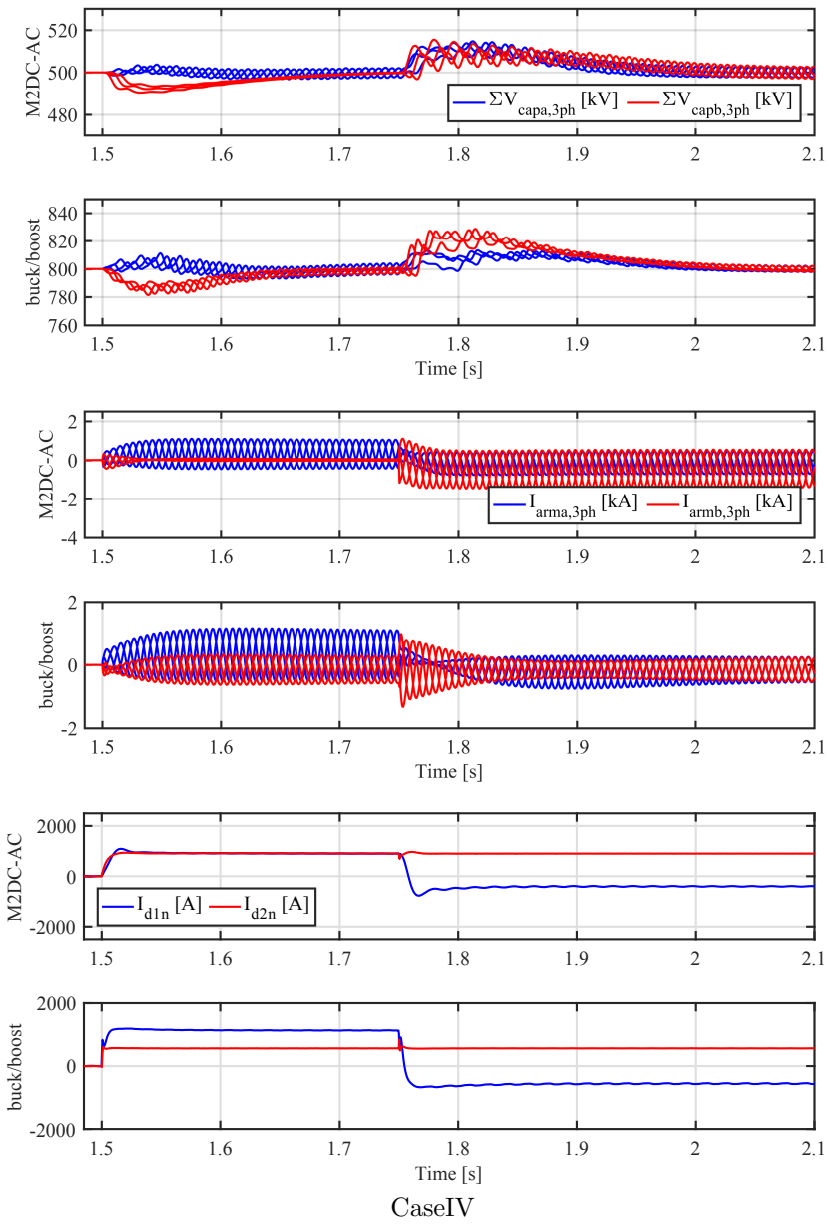

Figure 3.5: Case IV dc-dc-ac: At t = 1.5s 1 pu total power transfer into d1 is routed evenly to the ac grid (0.5 pu) and to d2 (0.5 pu), and at t = 1.75s, d1 and d2 each deliver 0.5 pu to the ac grid (for total of 1.0 pu) with power factor 0.95 lagging. (a) arm currents (b) sum of capacitor voltages (c) dc port currents

ate interchangeably and this is valid based on the symmetry of the simulation results.

Case III for MP-DAB in figure 3.8 clearly shows that the dynamics of arm currents for both time steps is similar. This is because whenever power step

Table 3.2: Simulation parameters for MP-AT and MP-DAB

Parameters	**MP-AT**	**MP-DAB**
$V_{d_1 n}$	400 kV	400 kV
V_g, n_T	300kV, 1	150kV, 1
G_v	0.5	1
L_a, L_{in}, L_{out}	50.3, 82.73, 82.73 mH	50.3, 65.6, 65.6 mH
R_a, R_{in}, R_{out}	0.366, 1.33, 1.33 Ω	0.466, 2.66, 2.66 Ω
ω	$2\pi \times 60$ rad/s	$2\pi \times 60$ rad/s
N_a, N_b	20, 20	10, 10
V_{SM}^{nom}, C_{SM}	20 kV, 4 mF	40 kV, 2.4 mF
X_T, X_F, I_{mT}, I_{mF}	12%, 12%, 1%, 1%	10%, 10%, 1%, 1%

change is applied the arm currents are changed in a similar fashion for both dc-dc and dc-ac power flow commands.

Power flows for MP-AT requires to be coordinated between primary MMC a and secondary MMC b. For instance, during power flow case I shown in Figure 3.10, both MMCs participate in transferring power to the ac grid in a similar fashion. Whereas for case II in Figure 3.11, each converter has opposite dynamic behavior because the dc current in the secondary MMC has a negative polarity with respect to the dc current in the primary MMC. This is explained in detail in [45].

3.2 Impact of arm capacitance tolerance on capacitor voltage dynamics

In this section, the transient dynamics of arms capacitor voltages are studied considering the capacitance mismatch between arms. To address this, the power flow cases in the previous section are performed with $\pm$ 25 % mismatch between arm 'a' and 'b' (i.e. capacitance of arm 'a' is 1.25 pu and arm 'b' is 0.75 pu). 1 pu capacitance is depicted considering the capacitance values in table 3.1 as base values. The transient response of the capacitor voltage is shown in Figure 3.14 for the second step change seen in simulation Figures 3.2-3.5. While

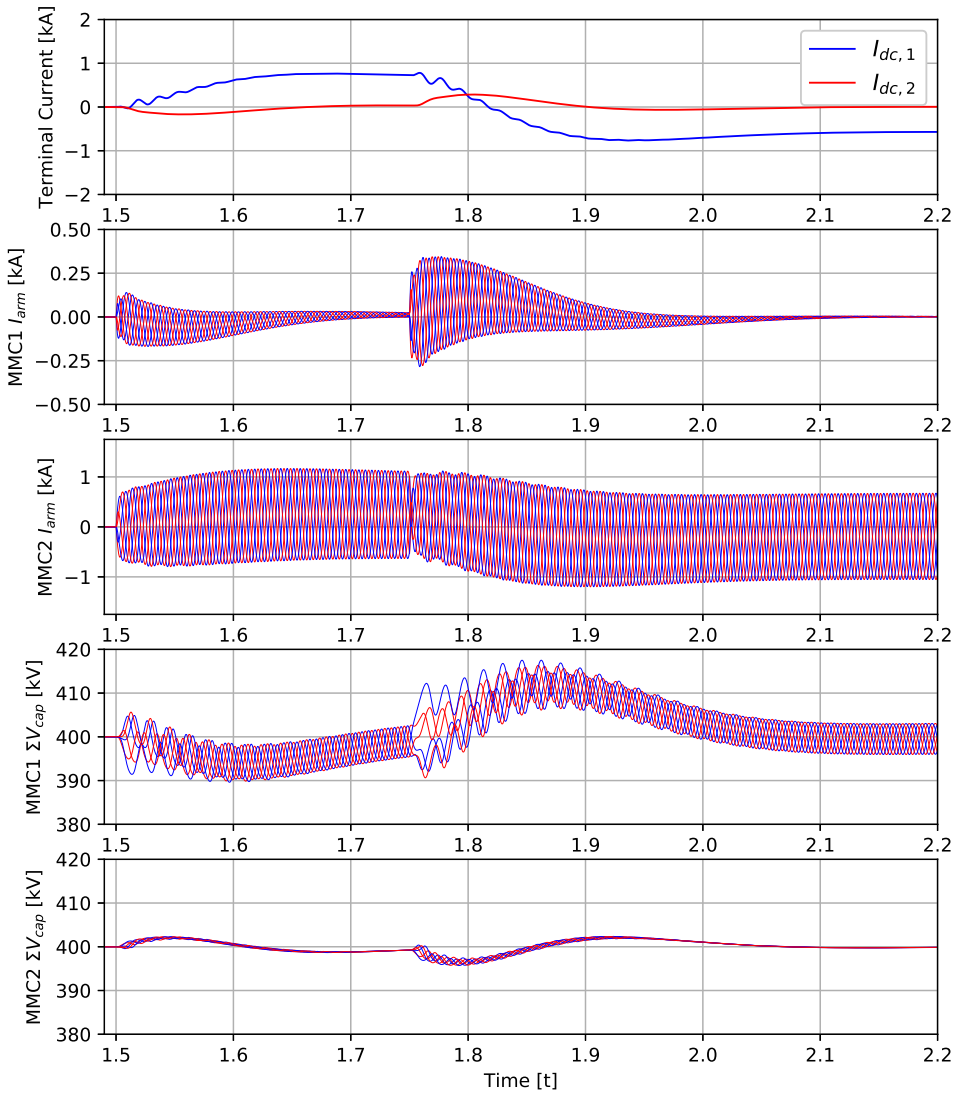

Figure 3.6: MP-DAB Case I dc-ac: At t = 1.5s 1 pu power transfer with power factor 0.95 lagging from d1 to the ac grid, and at t = 1.75s the direction is reversed.

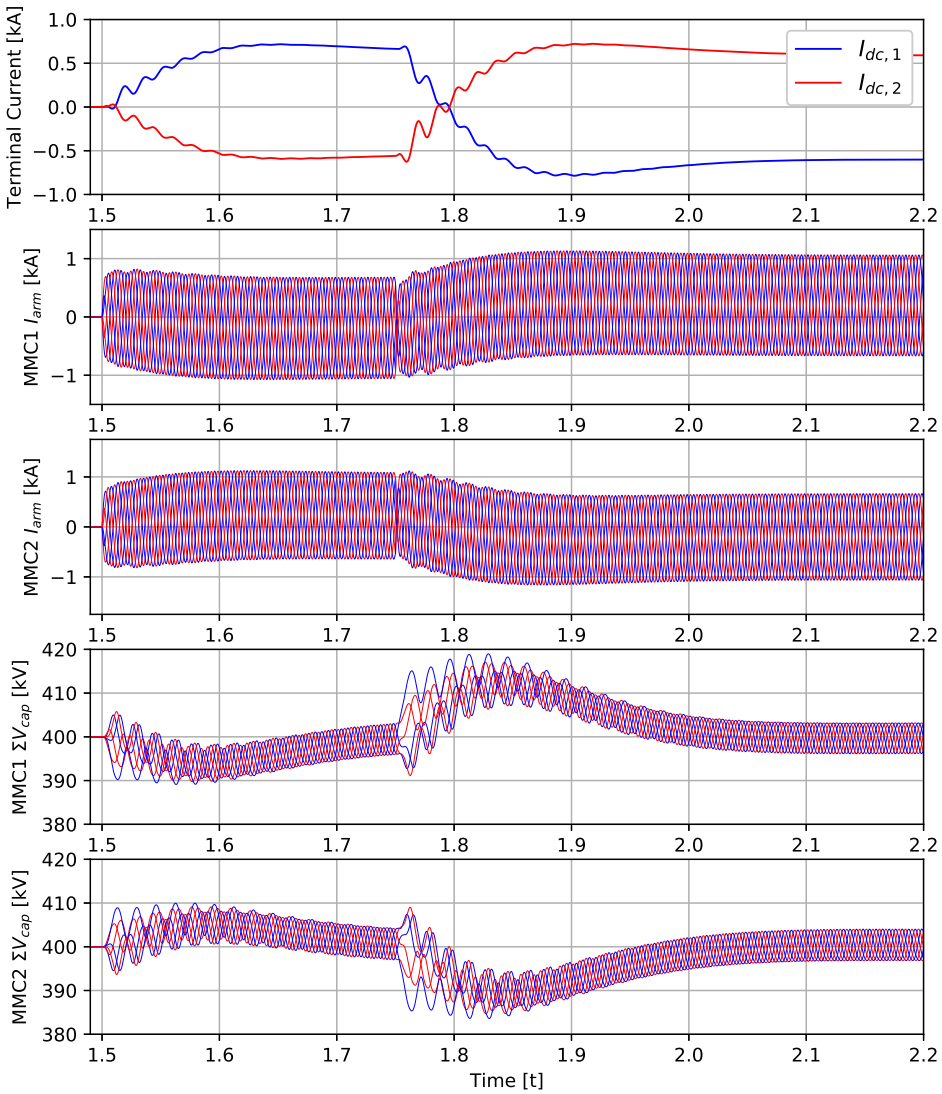

Figure 3.7: MP-DAB Case II dc-dc: At t = 1.5s 1 pu power transfer from d1 to d2, and at t = 1.75s the direction is reversed.

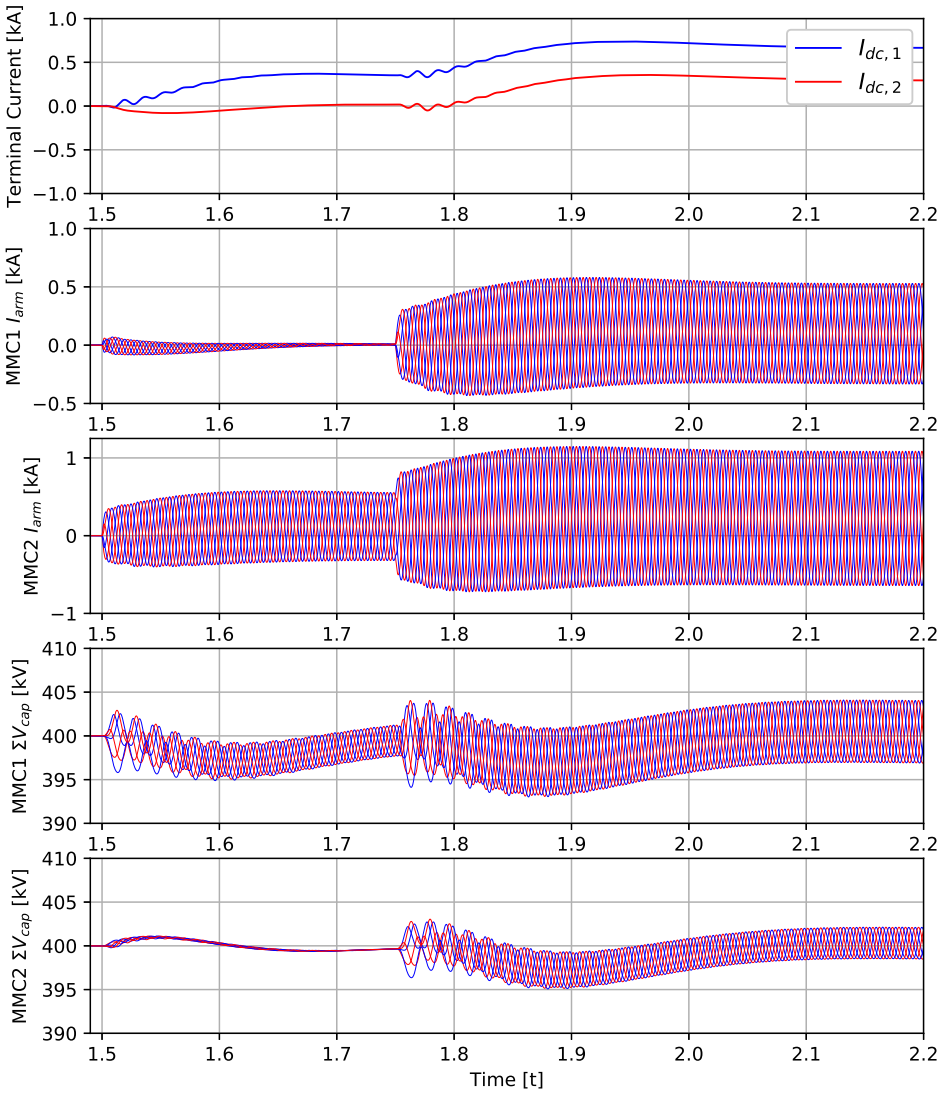

Figure 3.8: MP-DAB Case III dc-dc-ac: At t = 1.5s 0.5 pu power transfer with power factor 0.95 lagging from d1 to ac grid, and at t = 1.75s an additional 0.5 pu power is sent from d1 to d2 (total power injection into d1 is 1.0 pu).

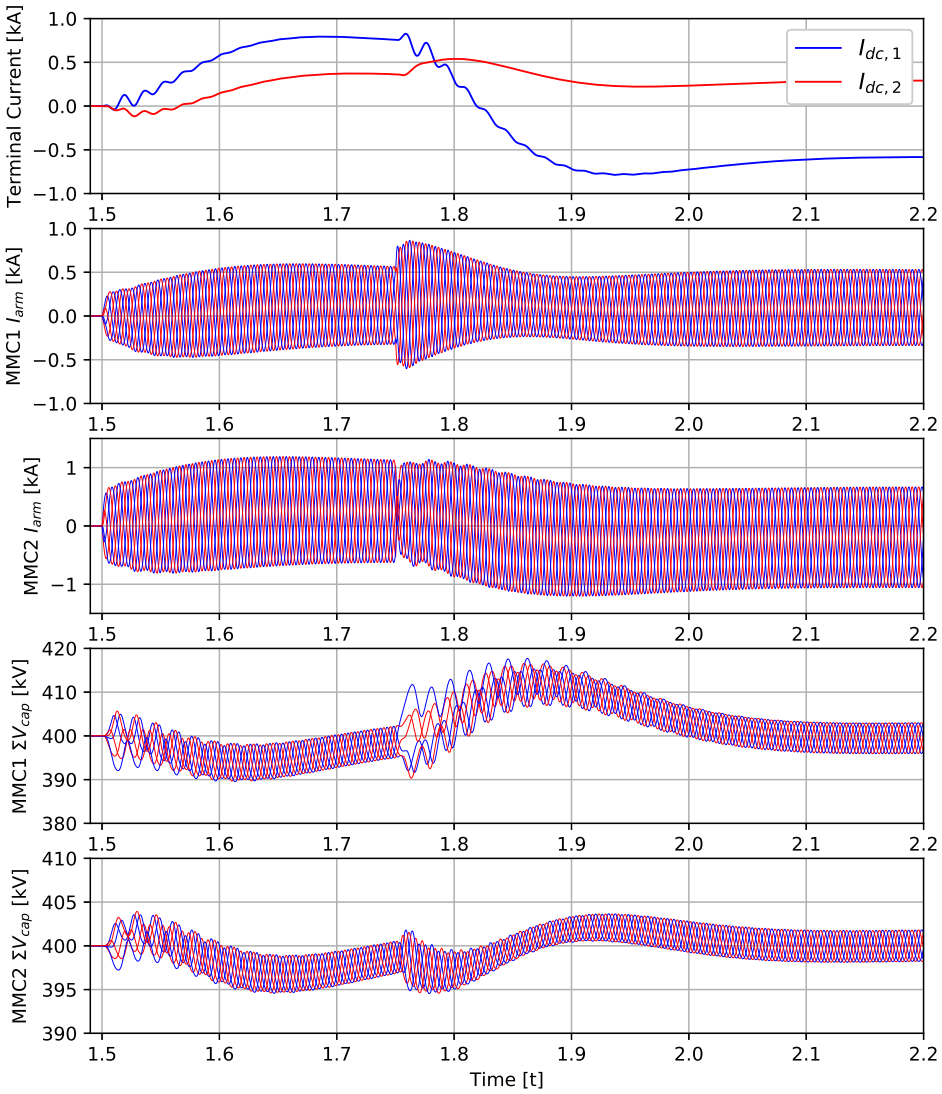

Figure 3.9: MP-DAB Case IV dc-dc-ac: At t = 1.5s 1 pu total power transfer into d1 is routed evenly to the ac grid (0.5 pu) and to d2 (0.5 pu), and at t = 1.75s, d1 and d2 each deliver 0.5 pu to the ac grid (for total of 1.0 pu) with power factor 0.95 lagging.

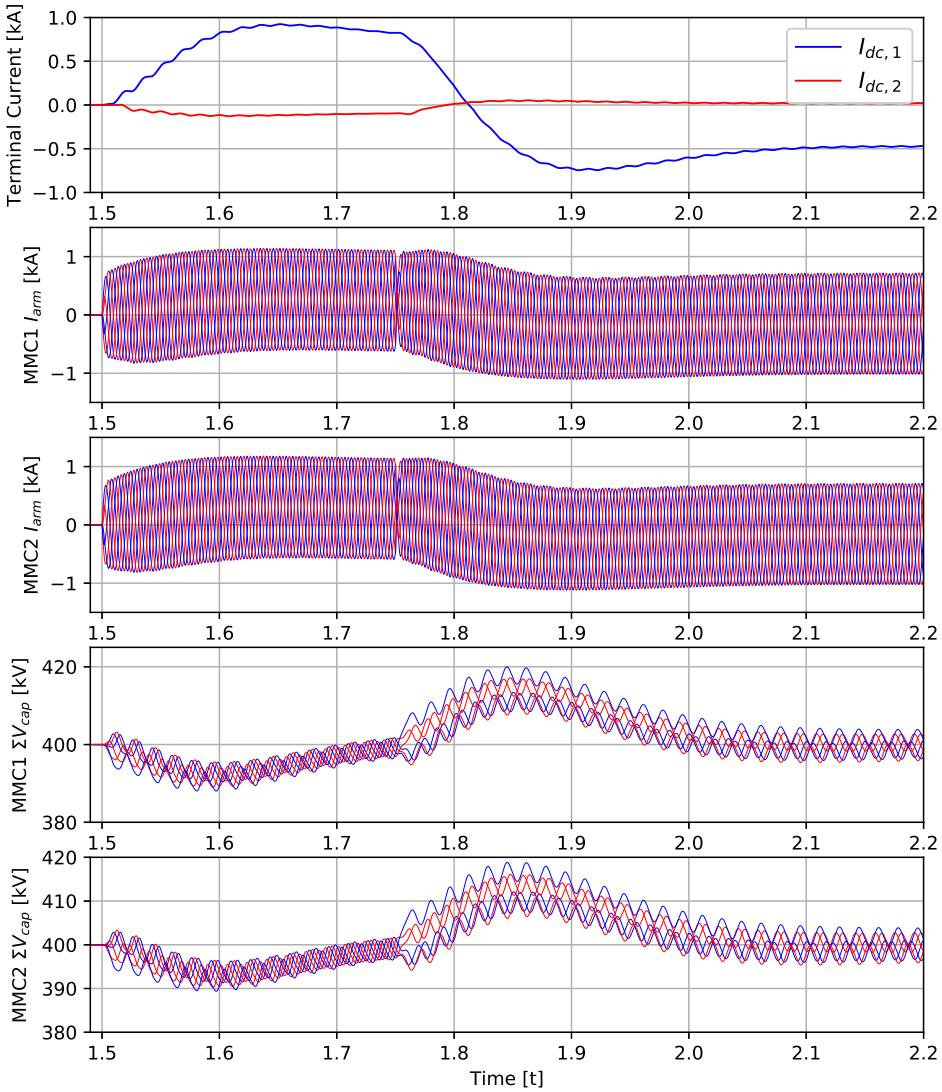

Figure 3.10: MP-AT Case I dc-ac: At t = 1.5s 1 pu power transfer with power factor 0.95 lagging from d1 to the ac grid, and at t = 1.75s the direction is reversed.

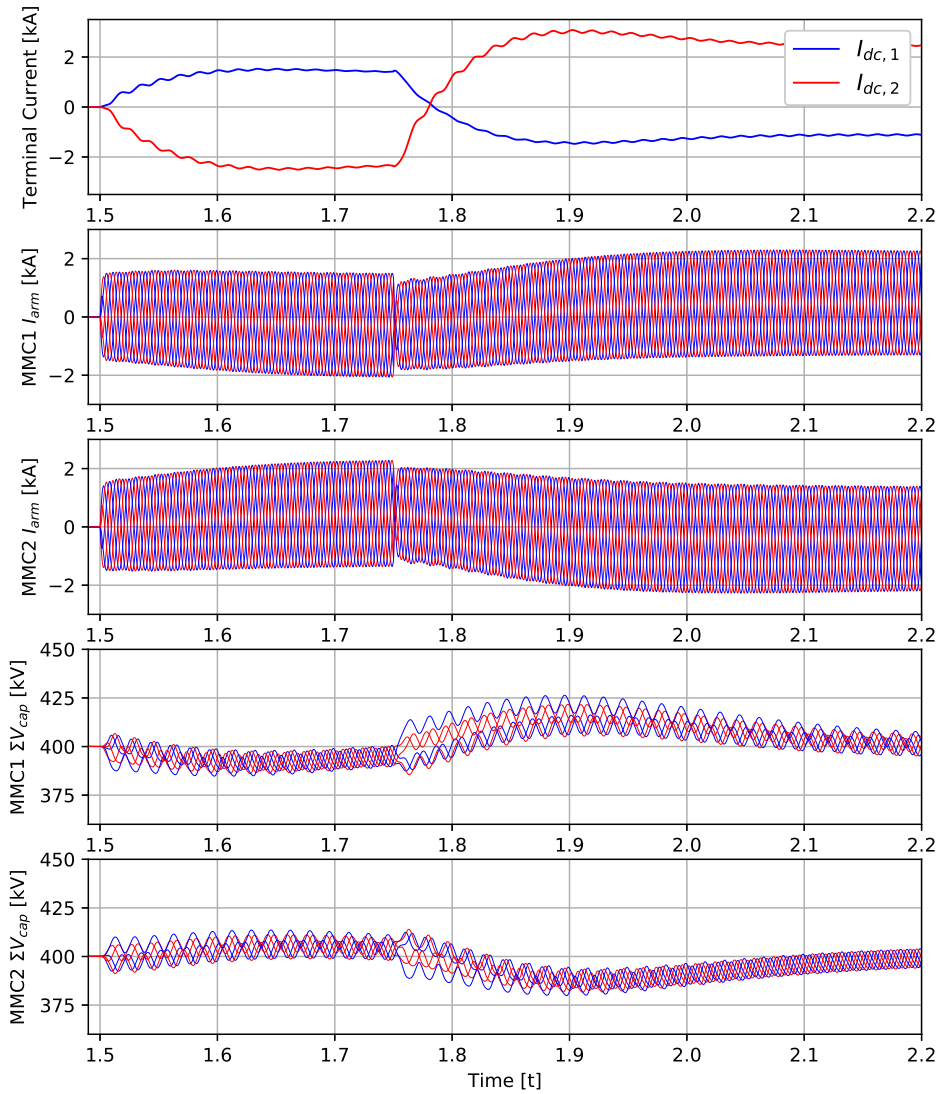

Figure 3.11: MP-AT Case II dc-dc: At t = 1.5s 1 pu power transfer from d1 to d2, and at t = 1.75s the direction is reversed.

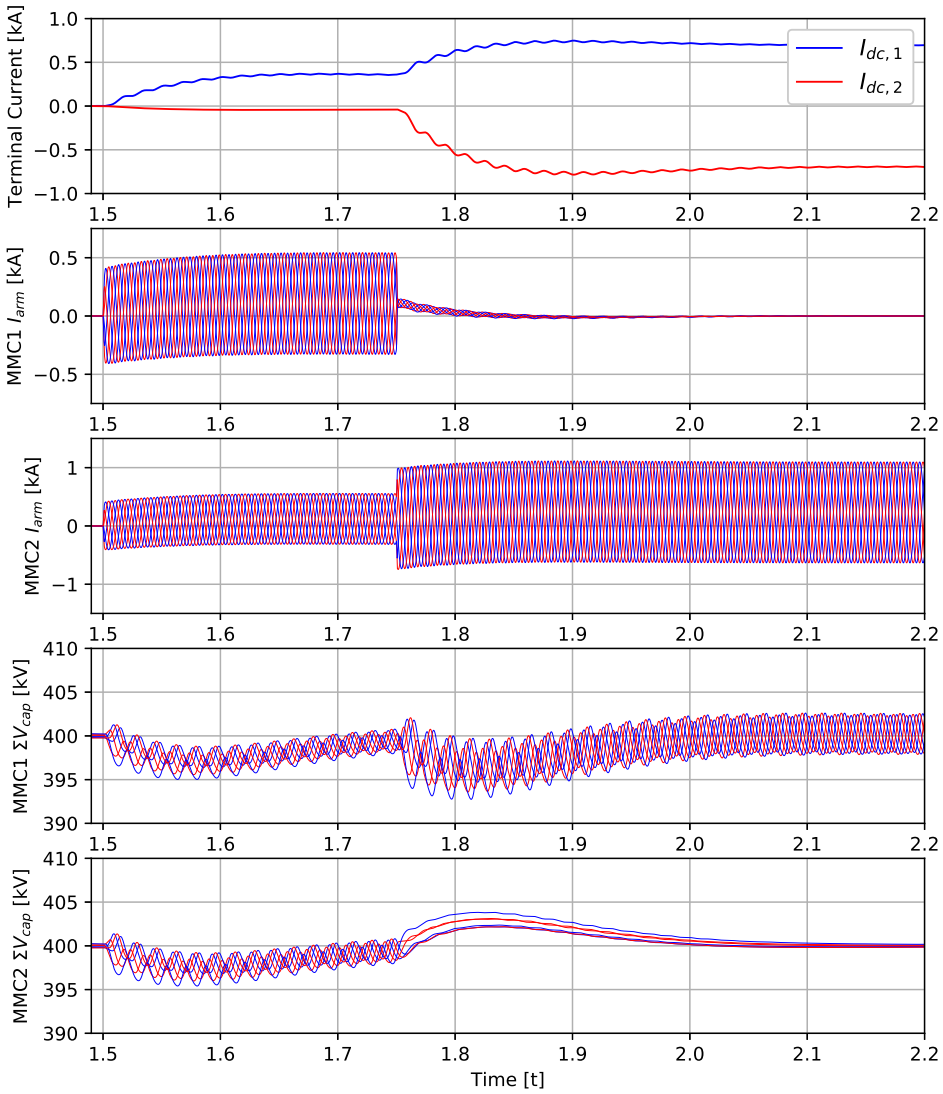

Figure 3.12: MP-AT Case III dc-dc-ac: At t = 1.5s 0.5 pu power transfer with power factor 0.95 lagging from d1 to ac grid, and at t = 1.75s an additional 0.5 pu power is sent from d1 to d2 (total power injection into d1 is 1.0 pu).

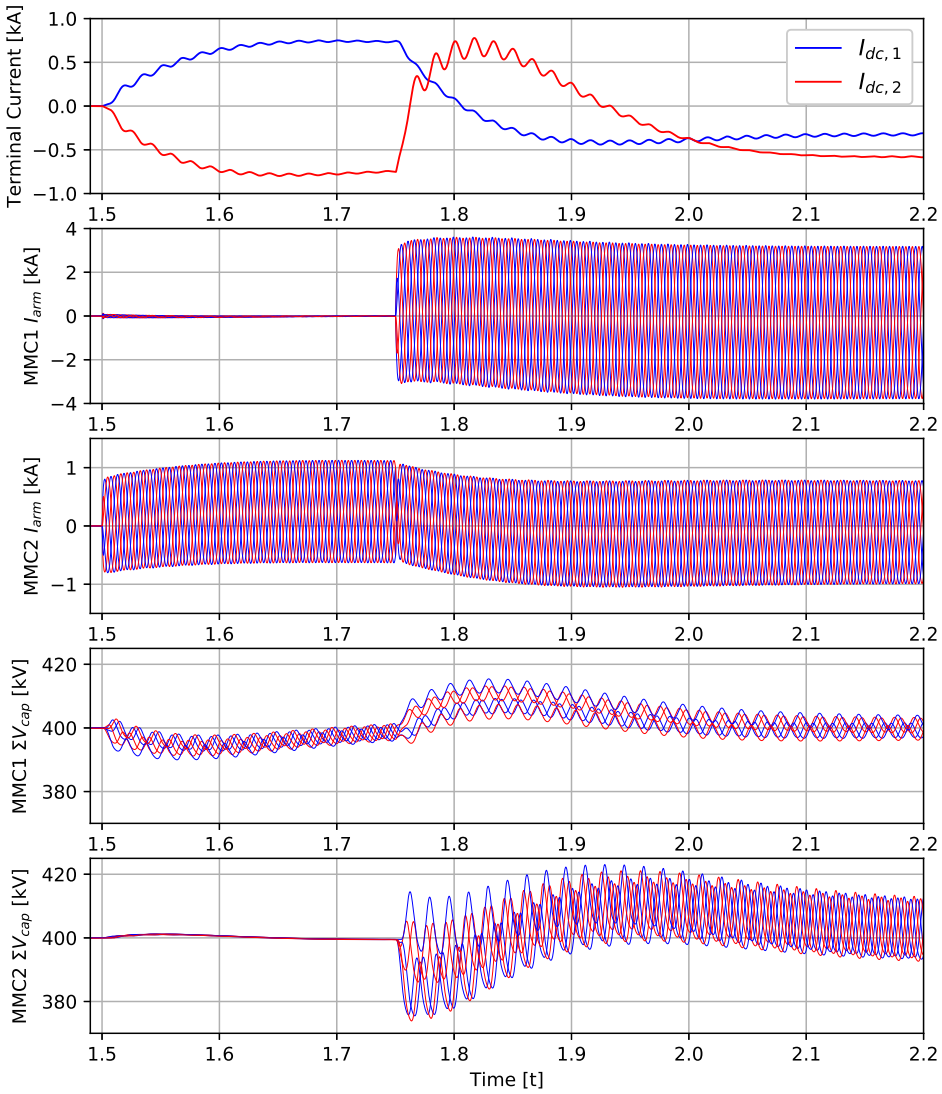

Figure 3.13: MP-AT Case IV dc-dc-ac: At t = 1.5s 1 pu total power transfer into d1 is routed evenly to the ac grid (0.5 pu) and to d2 (0.5 pu), and at t = 1.75s, d1 and d2 each deliver 0.5 pu to the ac grid (for total of 1.0 pu) with power factor 0.95 lagging.

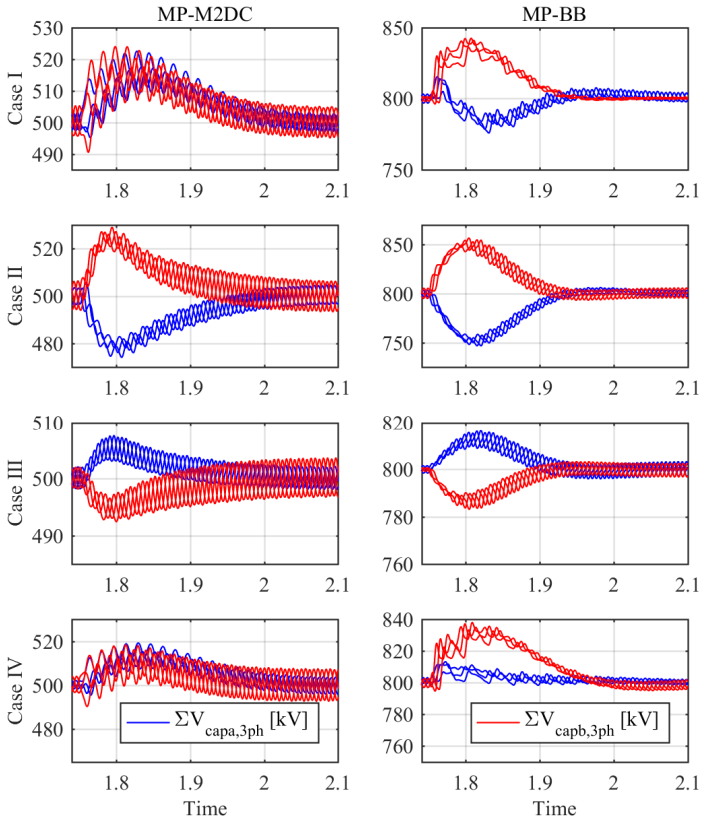

Figure 3.14: Impact of capacitance tolerance on capacitor voltage dynamics for MP-M2DC and MP-BB considering the four cases in Figure 3.1.

the magnitude of capacitor voltage ripples are impacted, the capacitor voltage balancing controls ensure the average capacitor voltages remains well regulated.

3.3 Simulation results for a reduced size of MP-M2DC

Figure 3.15, shows a modified version of MP-M2DC where the two networks interfacing magnetics are combined in one single delta/zig-zag transformer. Each dc port can be connected to independent dc systems or to one bipolar dc network and a bipolar version of this converter is tested and verified in [55]. Results shown in Figures 3.16-3.19 presents similar dynamics as for MP-M2DC cases in Figures 3.2-3.5.

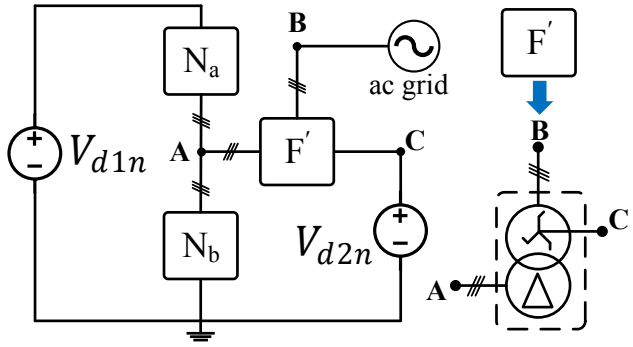

Figure 3.15: Modified MP-M2DC with delta/zig-zag transformer

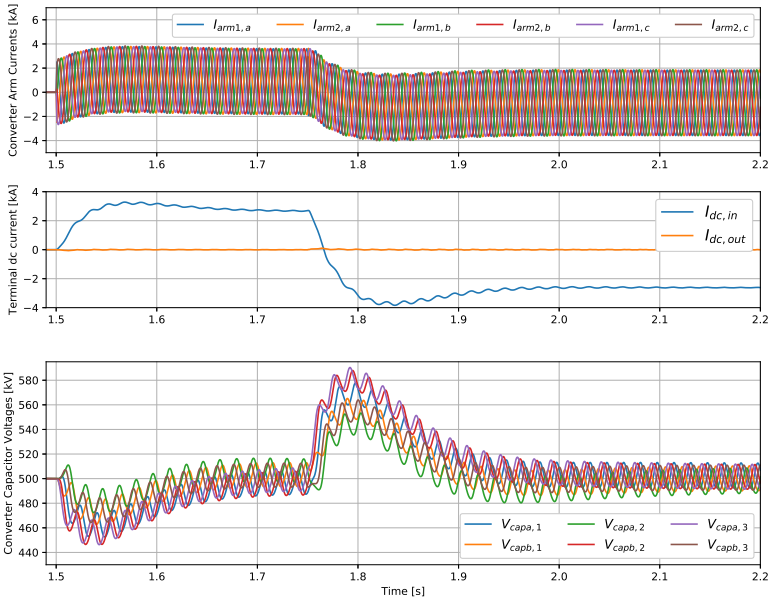

Figure 3.16: MP-M2DC shown in Figure 3.15 [Case I]

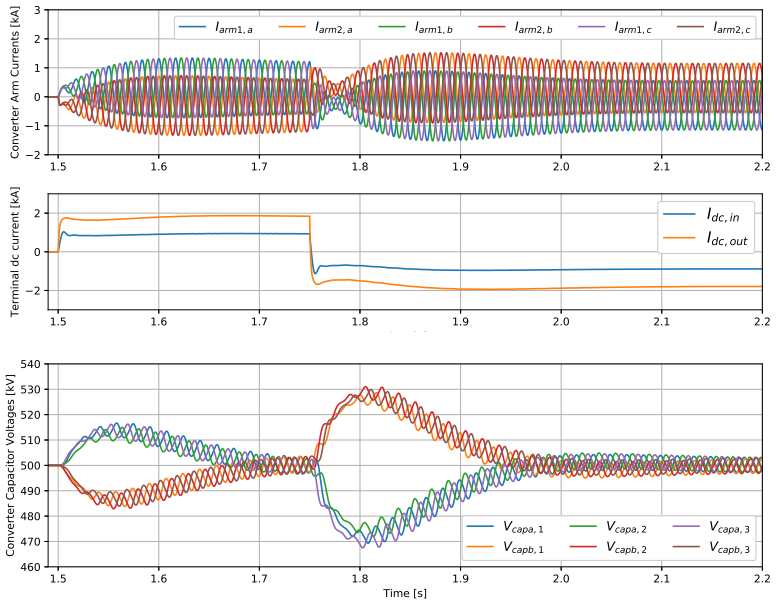

Figure 3.17: MP-M2DC shown in Figure 3.15 [Case II]

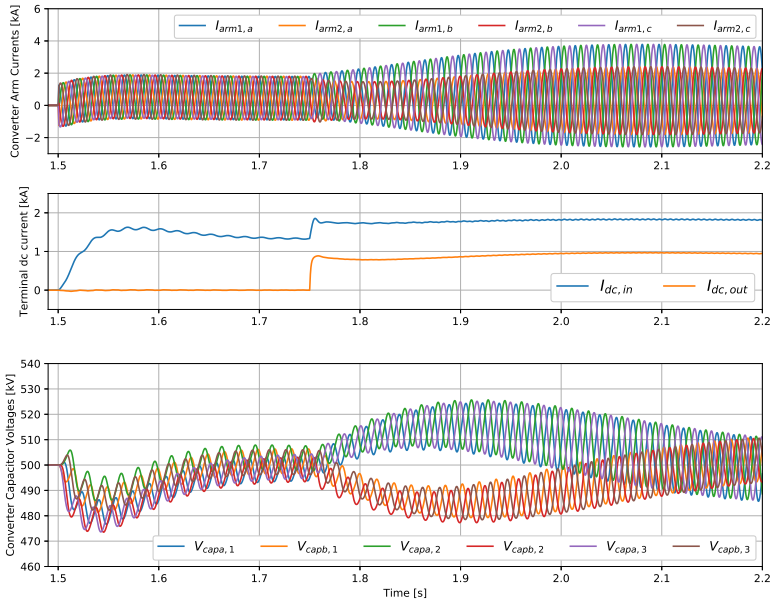

Figure 3.18: MP-M2DC shown in Figure 3.15 [Case III]

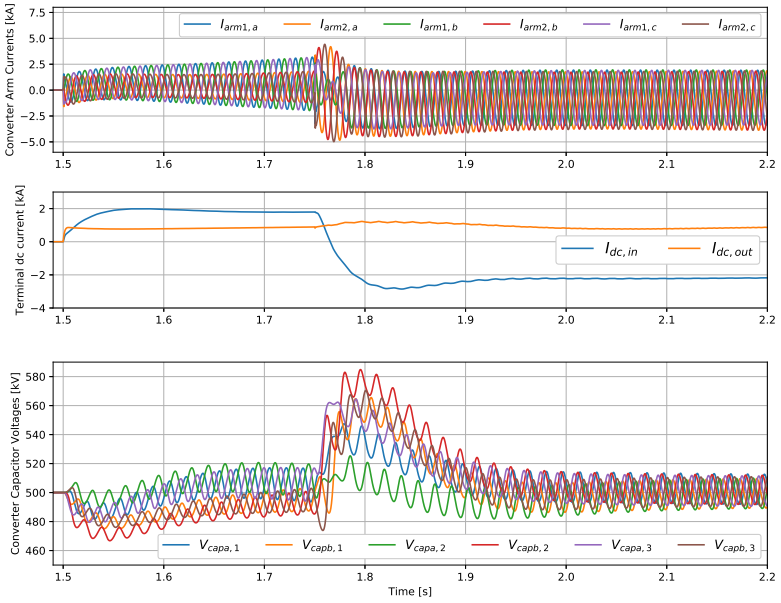

Figure 3.19: MP-M2DC shown in Figure 3.15 [Case IV]

Chapter 4

Fault Blocking Capability and Comparative Analysis

The fault blocking is explained for dc-dc-ac MMCs. Unlike certain dc-dc MMCs with inherent bidirectional fault blocking capability, the dc-dc-ac converter is incapable of blocking faults from all ports using only HBSMs. Several fault blocking cases are carried out using switched model of MP-M2DC (due to its simple architecture) to evaluate faults at different ports.

A fair comparison is provided for MP-M2DC, MP-BB, MP-AT, MP-DAB to analyze semiconductor requirements, utilization effort, efficiency, capacitive energy storage, and magnetics requirements. This comparison is useful to identify the application of certain topologies for different dc voltage step ratios.

4.1 Fault Blocking Capability

In this section, fault blocking is explained for a conventional dc-ac MMC and then requirements for bidirectional fault blocking is explained for dc-dc and dc-dc-ac MMCs and several fault blocking case studies are examined to validate fault blocking capability of MP-M2DC MMC.

4.1.1 Fault Blocking in Conventional DC-AC MMCs

Due to the severe impact of dc faults on HV power electronic components, dc circuit breakers and dc fault blocking strategies are essential to enhance HVDC transmission reliability and security. Dc circuit breakers due to their high total cost and immature technological progress are not widely accepted. In certain HVDC-MMC based systems, it is possible to inherently provide bidirectional dc fault blocking using FBSMs [56]. The conventional dc-ac MMC with HBSMs cannot tolerate the dc fault current that flows through the uncontrolled anti-parallel diodes of IGBT switches and hence the fault damages the converter switches. Using enough FBSM to inject reverse voltage enables full control over the direction of fault current by blocking switches. This comes at the cost of installing more SMs in arms leading to more investment costs and conduction losses.

Figure 4.1 shows faults on the dc port of a conventional dc-ac MMC considering HBSM (ref to Figure 4.1(a)) and FBSM (ref to Figure 4.1(b)) installed in arms, assuming switches are blocked. As a rule of thumb, by installing enough number of cells in each arm to support the healthy port voltage, the fault can be blocked if fault current direction enters capacitor voltage positive polarity. For HBSM-equipped dc-ac MMCs, bidirectional fault blocking is not applicable. Therefore, FBSMs are required to be installed in arms. Faults on the ac side of the MMC is mitigated using the MMC control system and is not a big challenge (simulation results in the latter verified controllability of ac fault currents).

Building dc-dc MMCs, such as DAB (with only HBSMs) provides a galvanic separation between dc ports and provides inherent bidirectional fault blocking capability. This is because the dc fault current has to pass through capacitors to feed the faulty node and therefore this fault current is blocked. Several works have shown the ability of MMC-based converters to block dc faults [29, 57]. When a dc-dc MMC is to be operated as a MP-DC2AC MMC (with required

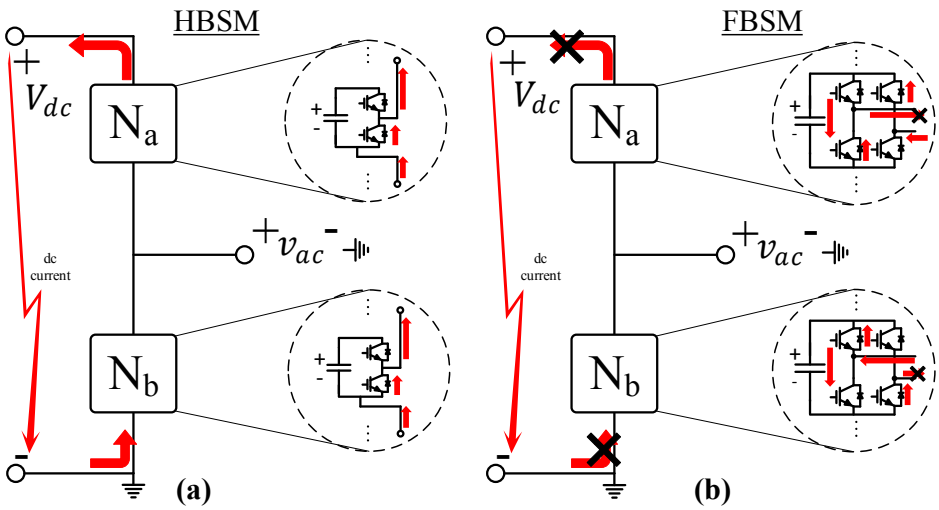

Figure 4.1: Dc pole to ground fault current direction in a dc-ac MMC equipped with (a) HBSMs that feeds the fault due to lack of reverse blocking voltage and (b) FBSMs blocks the fault current by imposing the reverse blocking voltage.

design developments), the faults on the dc ports are fed by the ac grid if HBSMs are installed, and therefore for inherent fault blocking from all ports additional FBSMs are required.

4.1.2 Fault Blocking in DC-DC MMCs

Fault blocking requirement is explained for dc-dc MMCs and dc-dc-ac MMCs. Fault blocking in different dc-dc based MMCs requires certain strategies. Buck dc-dc MMCs, such as M2DC and HVDC-AT with enough HBSMs, are able to block dc faults on dc_2. However, for dc faults on dc_1 the fault current flows through the anti parallel diodes. To resolve this, FBSMs are installed in the upper arms to support a negative dc voltage equal to the output dc voltage. For example in M2DC (similarly for HVDC-AT) with dc turns ratio G_v, the upper arms should be equipped with G_v FBSMs voltage in pu (considering the high level dc voltage as base) to block fault current fed from the low level side to the fault on the high level port and additional $(1 - G_v)$ HBSMs is required for similar scenario for faults on the low level port. The lower arm on the other hand does not require FBSMs and only needs enough HBSMs to support the

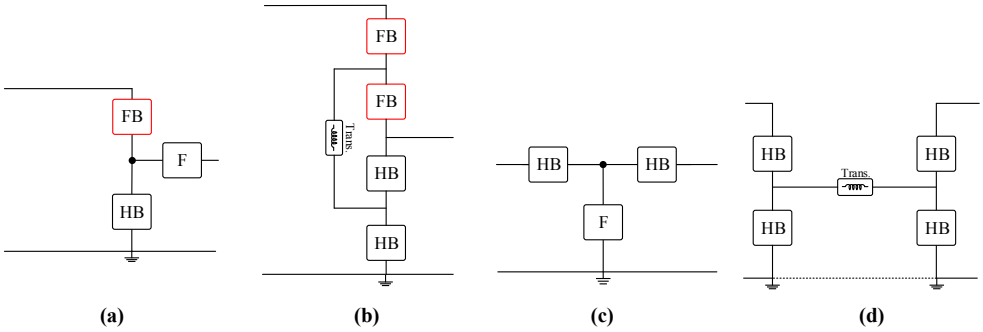

Figure 4.2: DC-DC MMCs suited for inherent DC fault blocking using FBSMs in blue arms, (a) and (b) requires G_v FBSM in upper arm (MMC), (c) and (d) both have inherent DC fault blocking capability using HBSMs

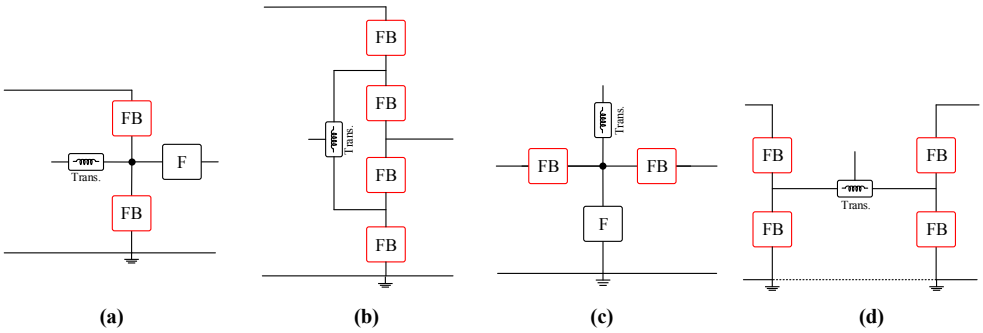

Figure 4.3: DC-DC-AC MMCs with FBSMs installed for Full Fault Blocking Capability

output dc voltage and the net ac voltage. Details on fault blocking capability of HVDC-AT is available in [1]. DAB and BB dc-dc MMCs are proven to have inherent bidirectional dc fault blocking using only HBSMs [10, 29, 32]. Figure 4.2 shows four core dc-dc MMCs with fault blocking capability.

4.1.3 Fault Blocking in MP-DC2AC MMCs

When a pole-to-ground dc fault occurs in a MP-DC2AC MMC, the fault current path not only comes from the healthy dc port, the ac grid also feeds the dc fault. Hence, certain bidirectional fault blocking dc-dc MMC topologies, such as DAB and BB MMC cannot block fault currents fed from the ac grid side with only HBSMs. As shown in Figure 4.3, all four topologies need enough FBSMs to block faults from ac and/or dc ports.

Table 4.2 shows SM voltage requirement for four MP-DC2AC MMC topolo-

gies with "fault blocking" capability. The number of switches in a single FBSM is assumed to be twice a standard HBSM. The discussion on SM voltage requirements is explained in section 4.2.1. As shown in Table 4.2, the required FBSM is equivalent to the arm/MMC dc voltage. Generally, considering all values of G_v, MP-DAB requires more FBSMs to be installed to block faults. MP-M2DC has different SM requirement around $G_v = 0.5$ because arms are interfaced with different dc voltages.

For minimum requirement of fault blocking capability, it is suggested to equip arms with a combination of HBSMs and FBSMs in series. The analysis of combined HBSMs and FBSMs is explained in the literature [58, 59] and it is outside the scope of this thesis.

In the following, several case studies for fault blocking is demonstrated to show the performance of MP-DC2AC MMCs equipped with HBSMs and/or FBSMs.

4.1.3.1 Dc to ground fault blocking Case Studies for MP-M2DC MMC Using Switched Model Simulation

To better illustrate fault blocking for MP-DC2AC, several simulation case studies are represented here. Because MP-M2DC is a core structure for all other topologies, all case scenarios are represented for this topology. The following cases are carried out using detailed switched model simulations in PSCAD. These case studies considers dc pole to ground faults on dc and three phase to ground on ac ports for different SM arrangements in arms:

- all arms equipped with HBSMs.
- all arms equipped with FBSMs.
- FBSMs in upper arms and HBSMs in lower arms.

The parameters used in these simulations are given in Table 4.1. The upper arms are labeled "1" and lower arms are shown with "2". Three phase are shown

with "a", "b", and "c" in the subsequent Figures (e.g. $I_{arm1,a}$ is the current of the upper arm for phase a).

Table 4.1: Parameters for fault blocking study in PSCAD for a three phase MP-M2DC

Parameter	Value
V_{d1n}, V_{d2n}	640 kV, 320 kV
$V_{ac}^{L-L,RMS}$	367 $[kV]$
P_{dc}^{rated}, ac grid power factor	1000 MW, 0.95 lagging
S_{base}, V_{base}	1000 MVA, 320 kV
No of SMs each arm, Capacitor nominal voltage, V_{sm}	101, 6.34 kV
SM capacitance, C_{sm}	8 mF
R_{arm}, L_{arm}	0.8 Ω, 50 mH
X_{trans}	15 %

In all cases, 1 pu power is exchanged between dc ports when a fault happens at $t = 1.50\ s$ for the duration of 300 ms and switches are blocked 80 ms after fault is detected. Figure 4.4 illustrates three fault locations for three mentioned switch arrangements in arms.

4.1.4 Simulation Results for Fault Blocking Implications for MP-M2DC

4.1.4.1 Faults on dc and ac ports of MP-M2DC with HBSMs

When a fault happens on dc_1, the current is fed to the faulty node through the diodes as shown in Figure 4.5. The current is fed to the fault on dc_1 node based on the significant current rise in arm currents which indicates that HBSMs are not applicable for fault blocking in this case.

For a fault on dc_2, even though the upper arm is not injecting current to the fault, the lower arm significantly injects current to the fault as shown in Figure 4.6. The capacitor voltages are significantly rising up due to the lack of current and lack of capacitor voltage control during this fault.

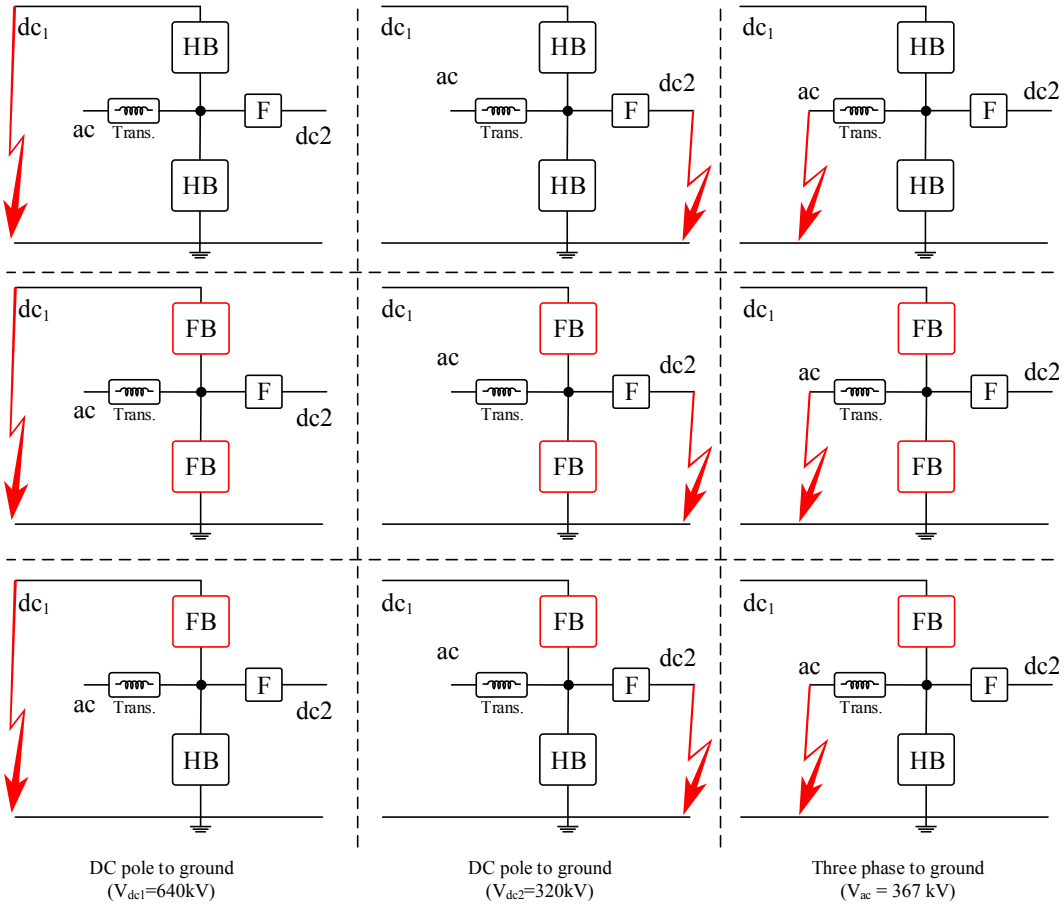

Figure 4.4: The location and type of faults considering three different switch arrangements in arms.

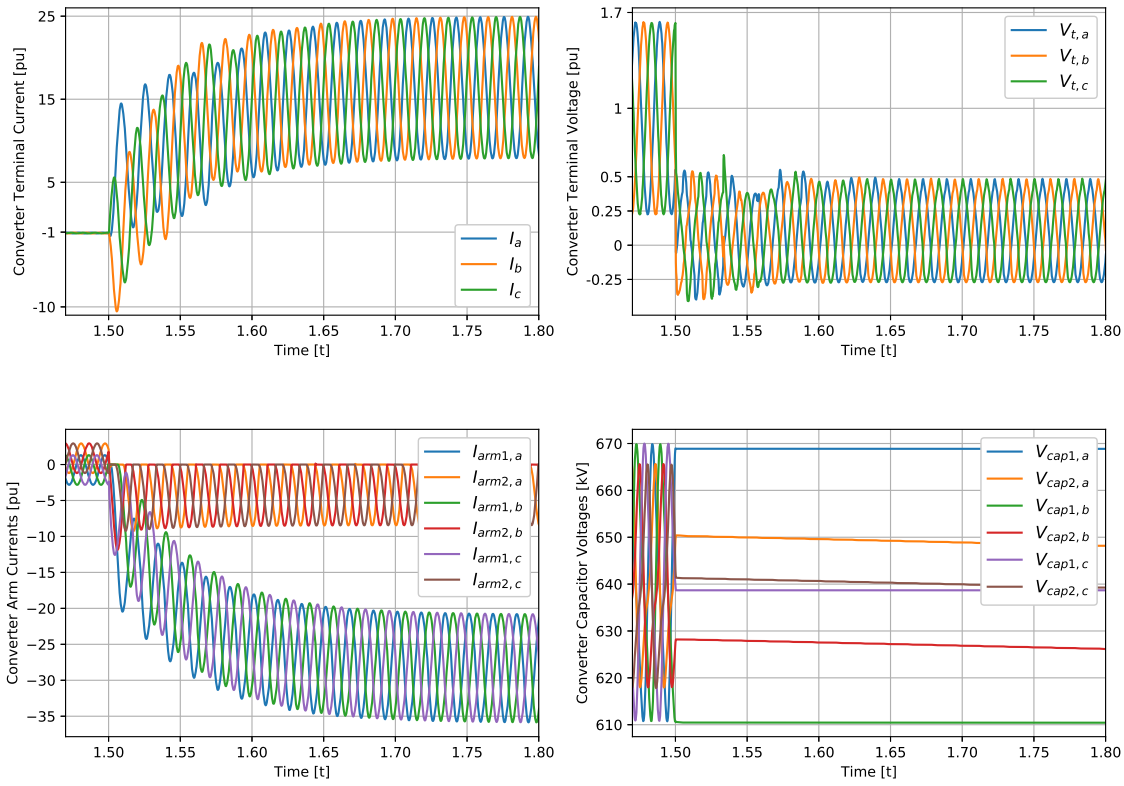

Figure 4.5: Simulation result for dc pole dc_1 : 640 $[kV]$ to ground fault when converter is equipped with HBSMs in all arms for three phase MP-M2DC [blocking action]

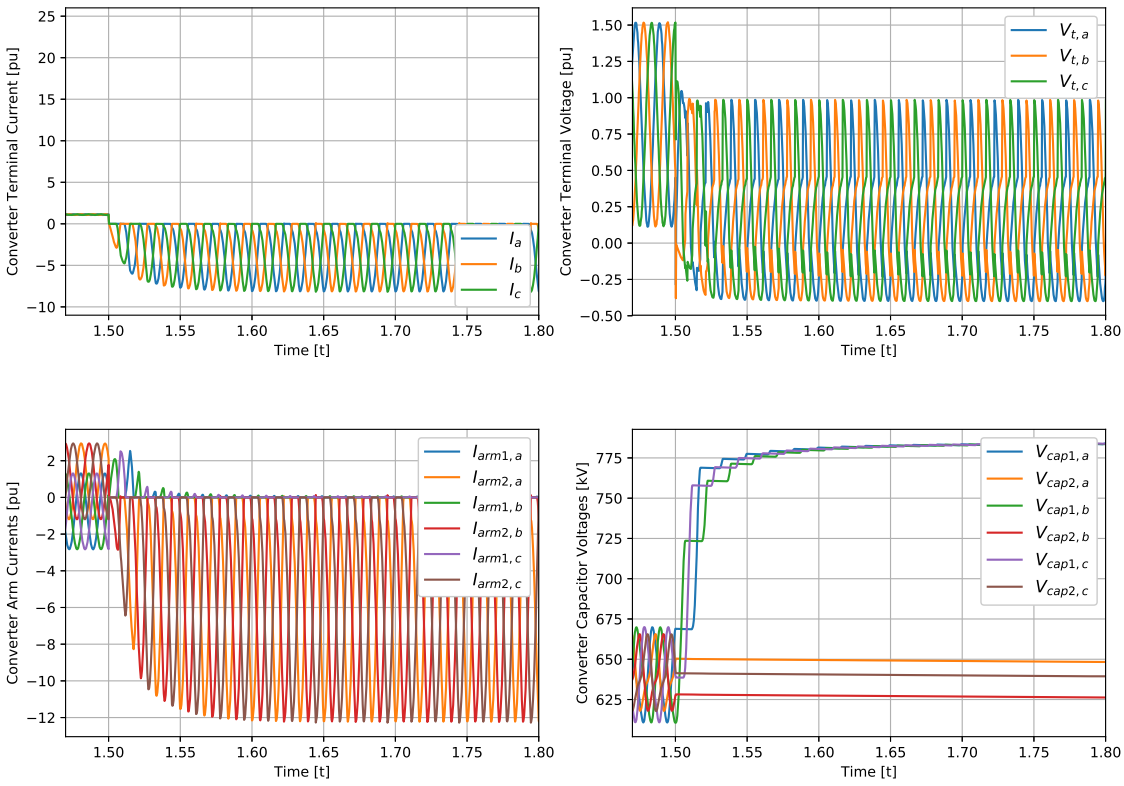

Figure 4.6: Simulation results for dc pole dc_2 : 320 $[kV]$ to ground fault when using HBSM in all arms for three phase MP-M2DC [Blocking action]

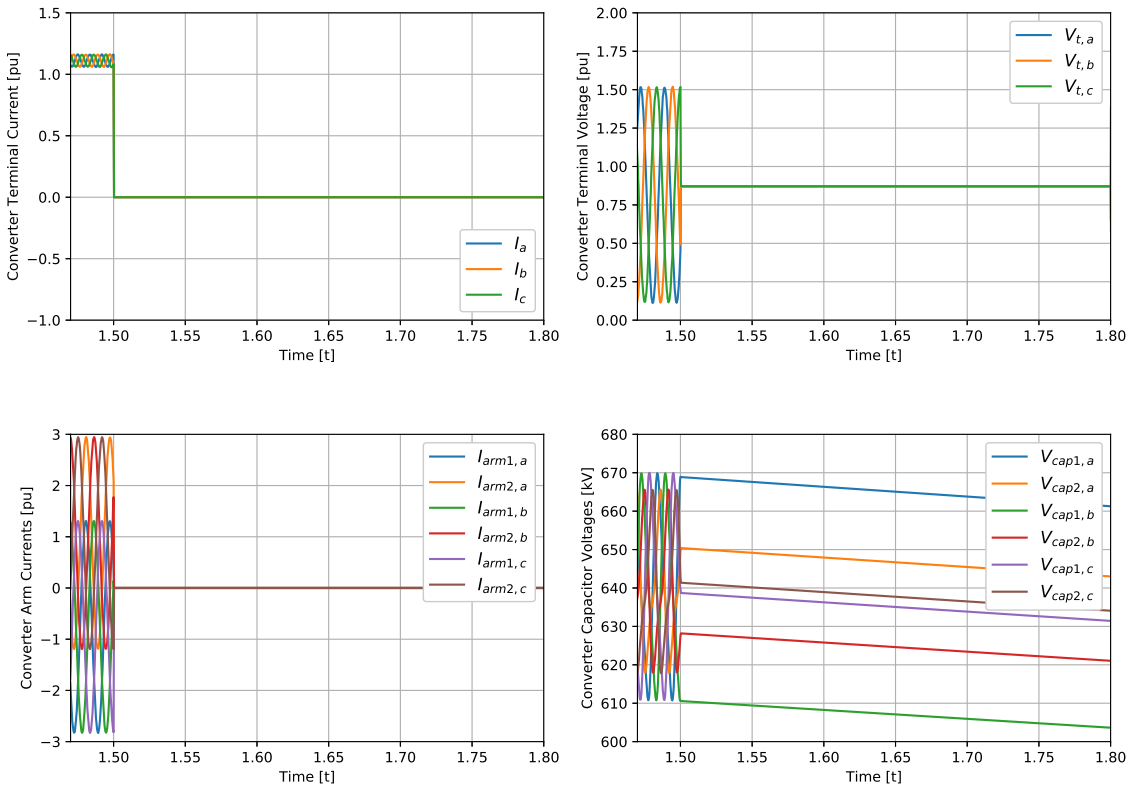

Figure 4.7: Simulation results for three phase *ac* grid to ground fault when using HBSM in all arms for three phase MP-M2DC [Blocking action]

When a fault occurs on an ac port of a MMC-based converter, the control system is capable of controlling the current flow. Here in Figure 4.7, it is shown how the current is controlled when the fault happens on the ac port. Power transfer between dc ports is interrupted when SMs are blocked. Once the fault on the ac grid is cleared the dc-dc power transfer can be resumed, it should be noted that during the fault all SMs must be blocked.

4.1.4.2 Faults on dc and ac ports of MP-M2DC with FBSMs

This is the case that the converter is equipped with sufficient FBSMs to have inherent bidirectional fault blocking capability. During a dc_1 to ground fault as shown in Figure 4.8, following the fault all switches are blocked and arm currents are suppressed to zero. Looking at converter terminal currents, when

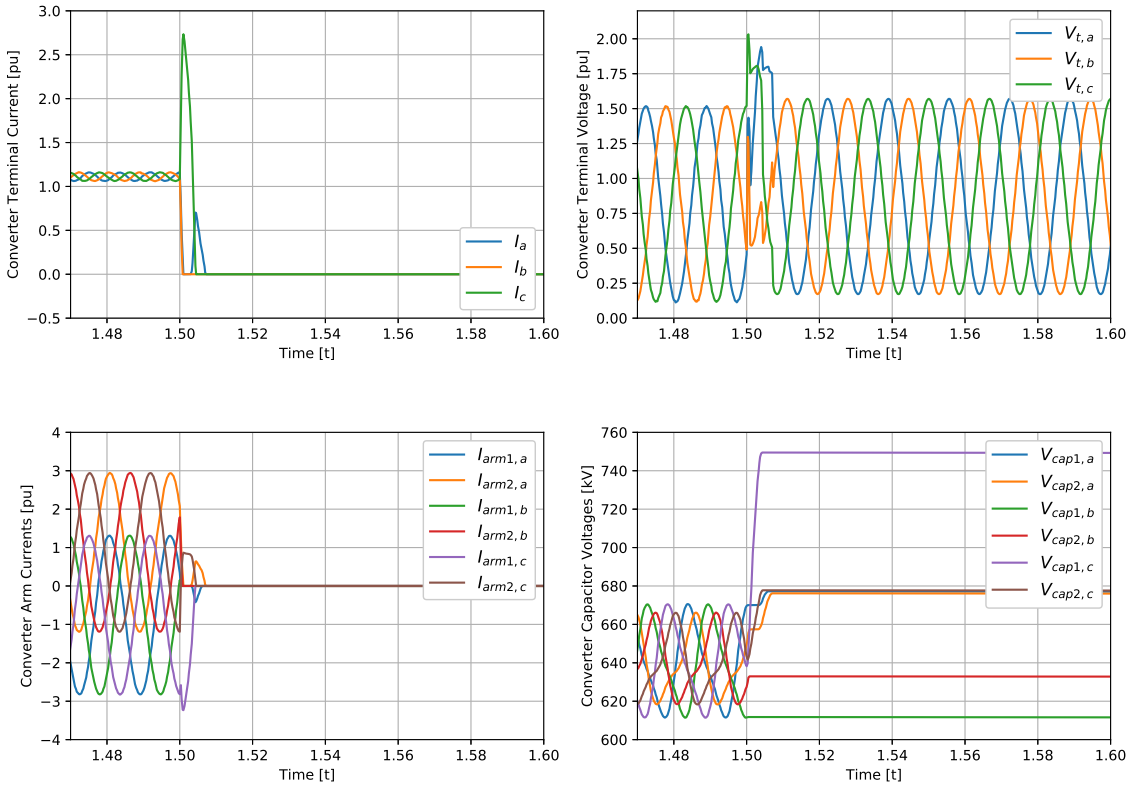

Figure 4.8: Simulation result for dc pole dc_1 : 640 $[kV]$ to ground fault when converter is equipped with FBSMs in all arms for three phase MP-M2DC [blocking action]

SMs are blocked it is as if the converter is islanded from all ports and therefore capacitors retain the converter terminal voltage through the control.

After a fault on dc_2 to ground, there is a dynamic response by the upper arms to the fault and they dissipate the trapped charges of inductors into capactiors by alleviating their voltage as shown in Figure 4.9. The converter terminal still retains its ac voltage through control, however this time it swings around zero dc voltage. Fault on the ac port has similar dynamic response to the case of a converter with HBSMs discussed earlier and simulation results are shown in Figure 4.10.

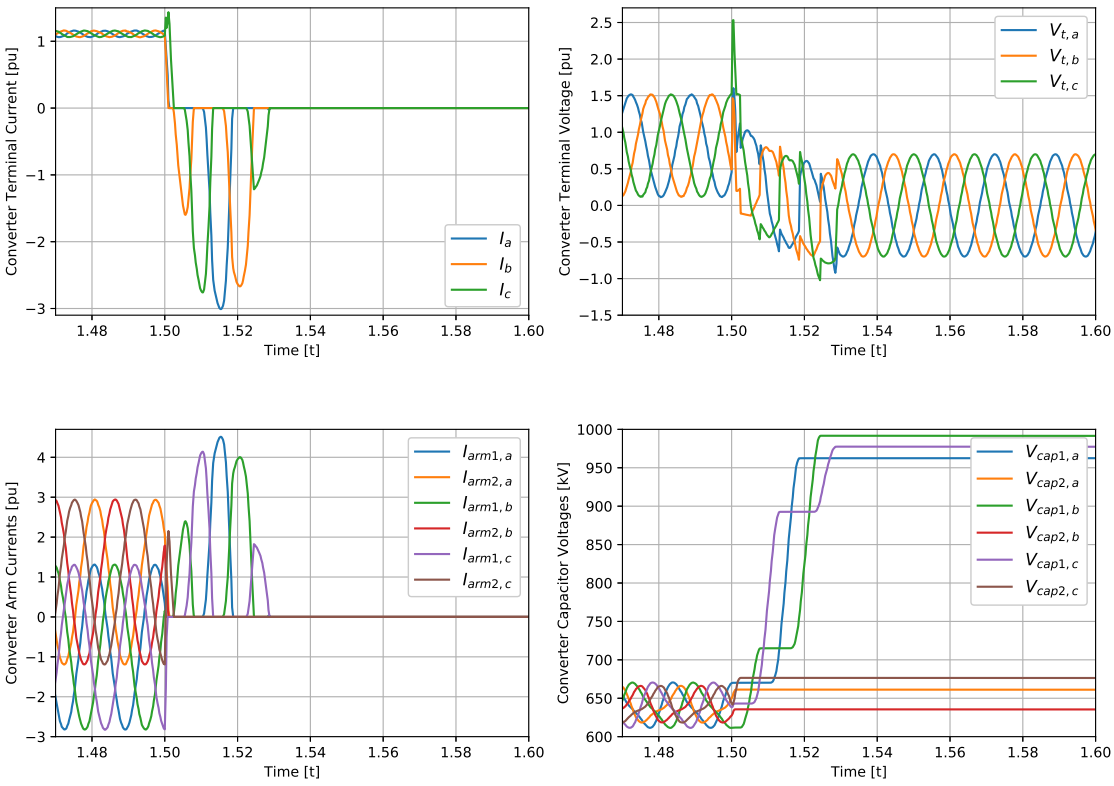

Figure 4.9: Simulation results for dc pole dc_2 : 320 $[kV]$ to ground fault when using FBSM in all arms for three phase MP-M2DC [Blocking action]

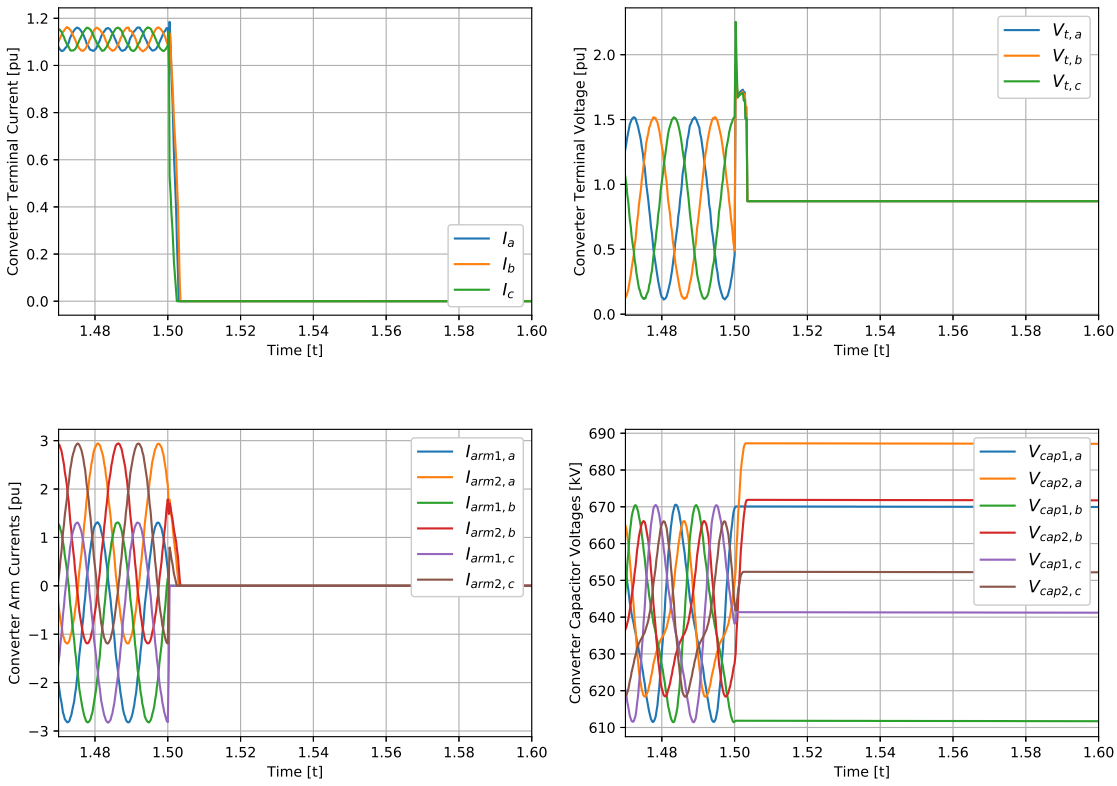

Figure 4.10: Simulation results for three phase *ac* grid to ground fault when using FBSM in all arms for three phase MP-M2DC [Blocking action]

4.1.4.3 Faults on dc and ac ports of MP-M2DC with FBSMs in arms "a" and HBSMs in arms "b"

This case is suitable for inherent bidirectional fault blocking in a dc-dc version of the converter. However, when the converters are developed for dc-dc-ac capability without modifications to semiconductor requirements, the converter is unable to provide bidirectional fault blocking. The subsequent simulation results verify this.

In Figure 4.11, it is shown that the fault on dc_1 is blocked and the converter is isolated from three ports. However, for a fault on dc_2 to ground as shown in Figure 4.12, the lower arms inject currents to the fault akin to the case shown in Figure 4.6. This is because the fault current is fed through anti parallel diodes from the common ground. Therefore, MP-M2DC with FBSMs in the upper arm is not sufficient for fault blocking capability.

Faults on the ac grid for this case is similar to the previous two cases and it is shown in Figure 4.13.

4.2 Comparative Analysis

A brief study of total semiconductor cost and efficiency is given for MP-M2DC, MP-AT, MP-BB, and MP-DAB. Certain operating characteristics, such as converter efficiency, fault blocking capability, and power transfer constraints poses limitations on the utilization of certain topologies. Semiconductor cost evaluation is taken into account as it is one of the major cost of an MMC and knowing this information is essential to understand the applications of MP-DC2AC MMCs. Then a fair comparison of converter efficiencies for similar operating conditions is explained that captures semiconductor conduction and switching losses as well as magnetics rating and losses.

First, SM requirement is explained for each topology and then the efficiency analysis of four topologies is described in detail. At the end, comparative

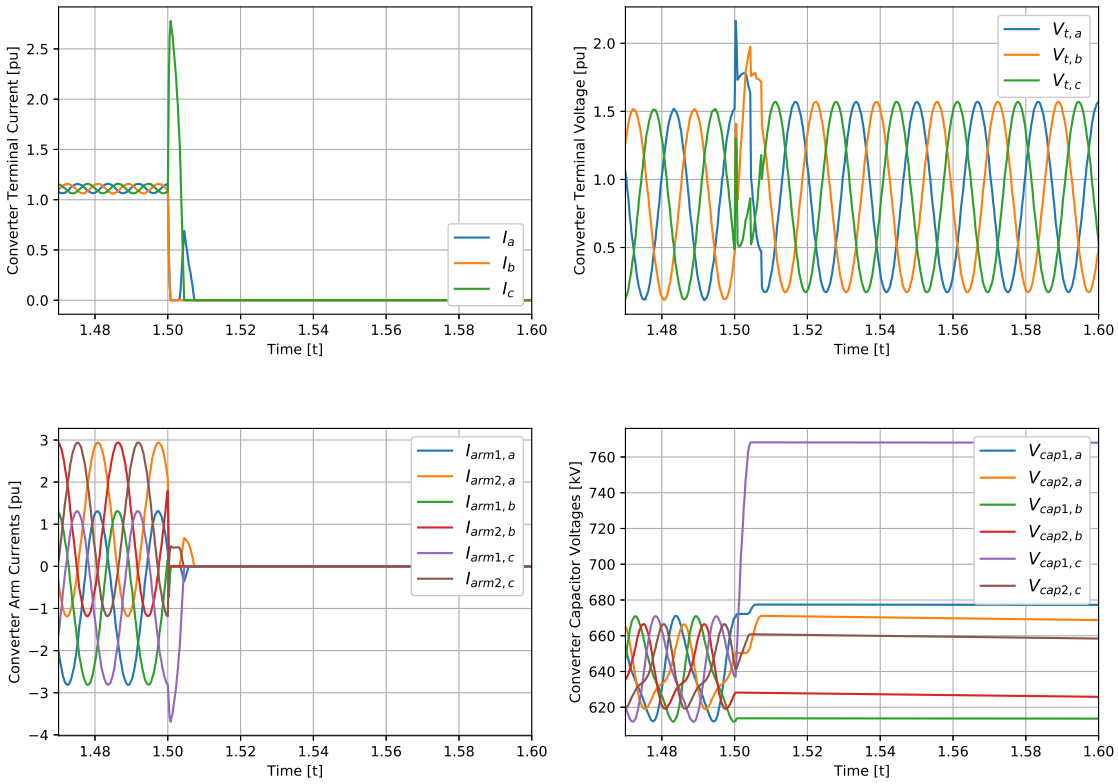

Figure 4.11: Simulation results for pole dc_1 : 640 $[kV]$ to ground fault when using FBSM in Upper arm and HBSM in lower arm in all arms for three phase MP-M2DC [Blocking action]

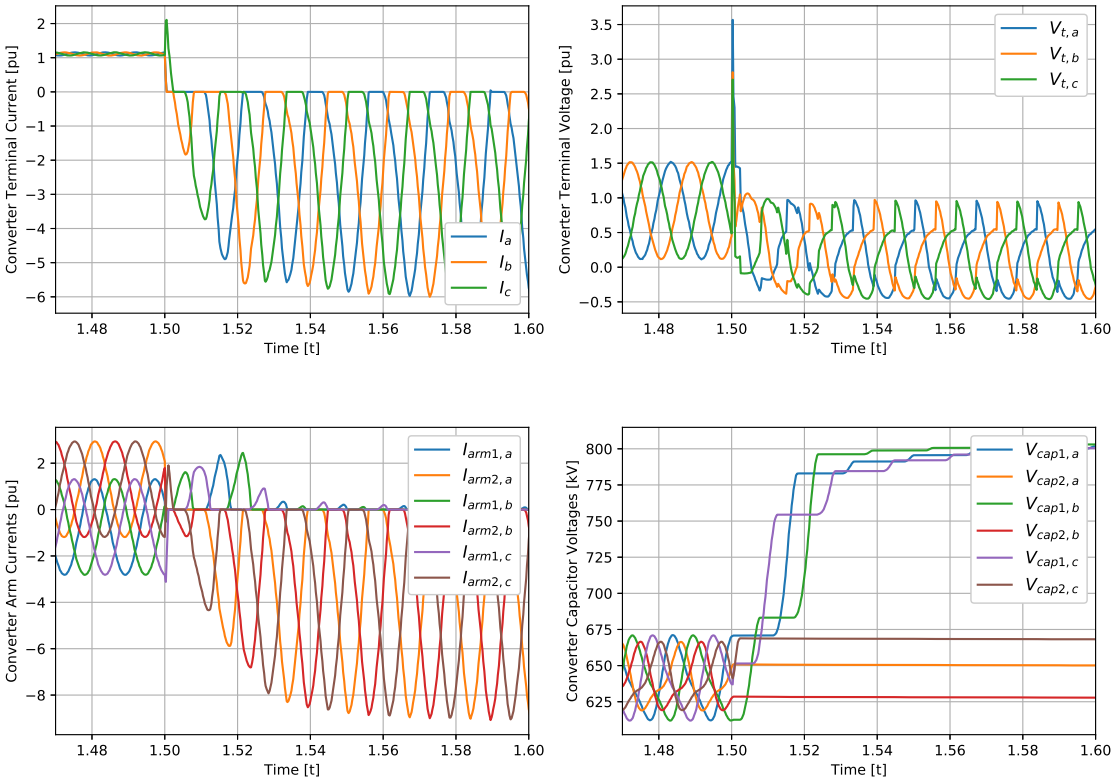

Figure 4.12: Simulation results for pole dc_2 : 320 $[kV]$ to ground when using FBSM in Upper arm and HBSM in lower arm in all arms for three phase MP-M2DC [Blocking action]

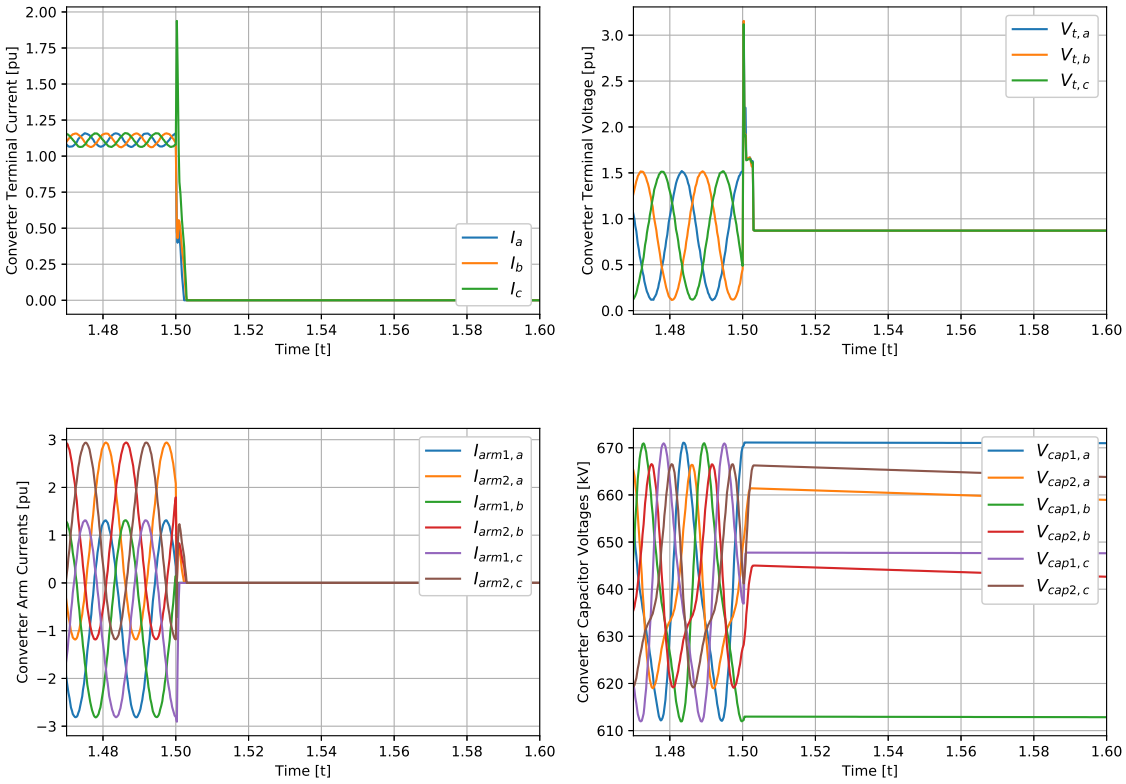

Figure 4.13: Simulation results for three phase *ac* grid to ground fault when using FBSM in Upper arm and HBSM in lower arm in all arms for three phase MP-M2DC [Blocking action]

analysis benchmark of four MP-DC2AC MMCs is presented.

4.2.1 SM Requirement

An MMC should be able to i) support the controlled voltage across the arm (i.e. certain number of SMs are stacked in series) and ii) support the current that flows into the arms (paralleling the arms to split current stress among them). Based on the two aforementioned requirements, in the following the requisite number of SMs to support maximum voltage and current stress is explained.

4.2.1.1 SM Voltage Requirement

Total required number of cells with rated capacitor voltage V_{SM}^{nom} in a single arm to support (V_{DC}^{max}) and ($\hat{V}_{AC}$) voltage is:

$$N_{SM} = \frac{V_{DC}^{max} + \hat{V}_{AC}}{V_{SM}^{nom}} \tag{4.1}$$

SM voltage requirement to support arm voltages for **normal operation** (converter ports can handle rated power flow in both directions) and **fault blocking capability** (redundant semiconductors to be installed) using HBSMs (to produce positive arm voltage) and FBSMs (to produce positive/negative voltage) is explained in the latter.

4.2.1.2 Normal Operation SM Requirement

Total installed number of SMs in a converter should be enough to operate for bidirectional multiport power flow. This means that the power (current direction) can be reversed in all SMs, but the polarity of injected voltage on the arms does not need to go negative.

To better understand SM voltage requirements for normal operation, consider the following example:

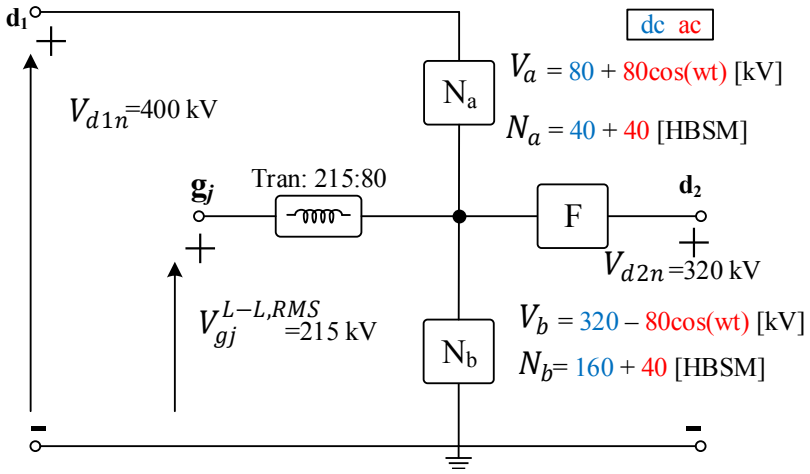

Figure 4.14: Example of SM voltage requirement for **normal operation** of a MP-M2DC using only HBSMs

Suppose we have an MP-M2DC that interconnects two dc systems at rated voltages $V_{d1n} = 400kV$ and $V_{d2n} = 320kV$, ($G_v = 0.8$) and an ac grid at voltage $V_{ac}^{L-L,RMS} = 215kV$ and the rated voltage of the SM is $V_{SM}^{nom} = 2kV$. Assuming normal operation for a lossless converter, the SM requirement for each arm to support the dc (and ac) voltage(s) are shown in Figure 4.14. Using only HBSMs, the arm voltages are always positive and the maximum ac voltage is limited to $\hat{V}_{ac} = 80kV$ [1]. To increase the peak ac voltage magnitude beyond $80kV$, the upper arm needs to generate a negative voltage which means FBSMs should be installed.

A similar practice can be done for the other three MP-DC2AC MMCs. A general expression is derived based on the previous discussion that determines the SM voltage requirement for four variants at arbitrary dc voltage ratio (G_v) which is presented in Table 4.2.

A detailed explanation of the voltage requirement for each variant is discussed in the following:

MP-M2DC Non-isolated structure of this converter forces arms to take similar ac voltage. Moreover, the peak value of the ac voltage is constrained to

[1]The impedance of arm chokes is assumed small and therefore ac arm voltage is purely differential mode, i.e., $\hat{V}_c \simeq 0$ in (2.6)

the minimum dc voltage requirement by arms at certain G_v. As shown in Table 4.2, the ac voltage of MP-M2DC for $G_v \leq 0.5$ and $G_v > 0.5$ is the minimum dc voltage supported by arm "a" and "b".

MP-BB Similar to MP-M2DC, this topology is non-isolated which means the arms ac voltage is constrained to the minimum arm dc voltage. The peak ac voltage $\hat{V}_{AC}$ for both arms is limited to $G_v V_{d1n}$.

MP-DAB Galvanic isolated MP-DAB that decouples dc ports provides independent ac voltages for two MMCs. The maximum ac voltage on each MMC can ideally reach to half of the DC port voltage[2]. In terms of voltage stress on the intermediate transformer, for symmetrical monopole HVDC systems, MP-DAB does not impose any dc voltage stress between the ac windings. In contrast, for asymmetrical monopole HVDC systems there is a dc voltage stress (equal to 50% of V_{d1n}) on the windings that makes the insulation for the AC transformer more complex and expensive.

MP-AT Although this converter is non-isolated, the ac components are circulated through an ac transformer and hence similar to MP-DAB the ac voltage of two MMCs are isolated. There is a dc voltage stress on the windings of the transformer which is equal to 50% of V_{d1n} similar to MP-DAB. Insulation of transformer windings for the dc voltage stress is a complex and costly process. Because the ac voltages of two MMCs are galvanically isolated, the ac voltages of the upper and lower MMCs are independent. That means the SM voltage requirement expression is provided for all G_v values.

4.2.1.3 Fault Blocking SM Requirement

By installing FBSMs as substitutes to HBSMs, the converter is capable of injecting negative voltage to block currents from flowing into the fault. Beside fault blocking, FBSMs can also increase the ac voltage modulation of the

[2]in practice the AC voltage is around 5 % lower than the half DC voltage to provide ample space for dynamic response

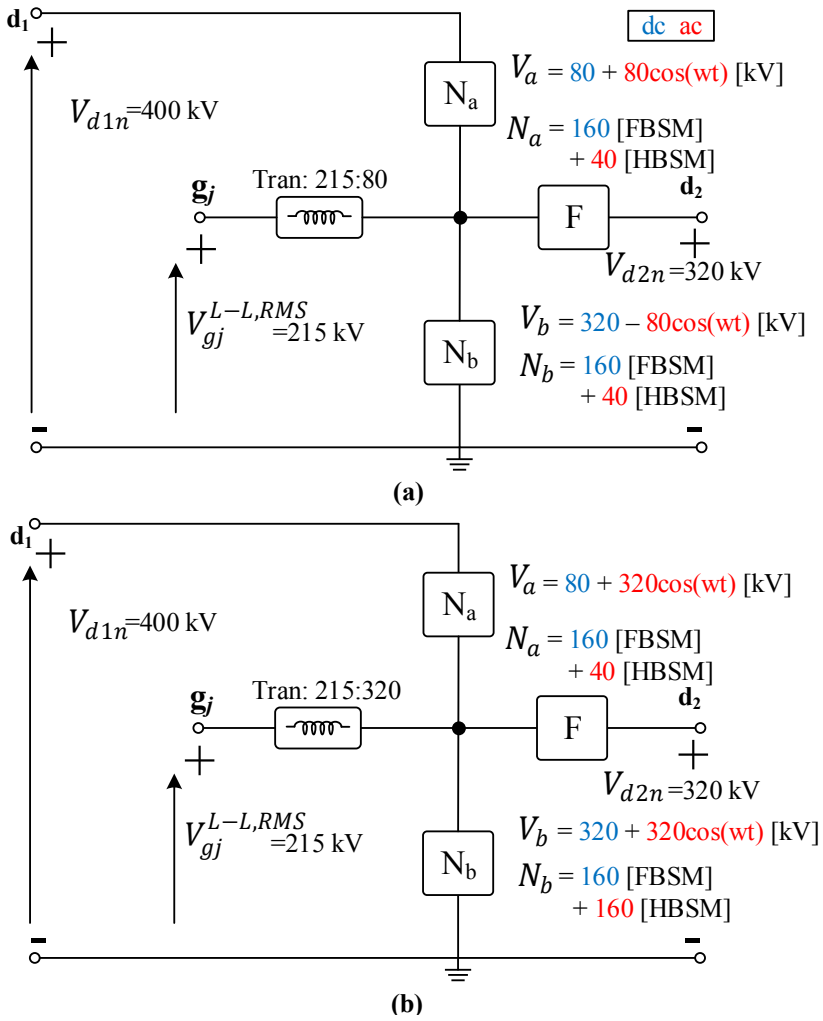

Figure 4.15: Example of SM voltage requirement for fault blocking in a MP-M2DC, considering (a) the minimum FBSM requirement and (b) maximum ac voltage utilization

converter to minimize the steady state current magnitude which is a great advantage to increase the converter efficiency and power flow capacity.

To better understand the SM voltage requirement for fault blocking using FBSMs, Figure 4.15 shows an example of MP-M2DC equipped with FBSMs. After all, utilizing FBSMs require double number of SMs compared to HBSMs and in a similar case the conduction losses of a FBSM-based converter is much higher leading to a lower efficiency. The minimum number of FBSMs to be installed in an arm or subconverter is given in Table 4.2.

Figure 4.15(a) shows the minimum FBSM requirement to block faults from

all three ports. It is shown that arm "a" requires a negative voltage equal to $V_{dc2} = 320kV$ to block current flow from d_2 to faults on d_1. For arm "b", there should be enough FBSMs to block faults on d_2.

Table 4.2: SM Voltage Requirement for Each DC-DC-AC MMC Normalized to V_{d1n}

		MP-M2DC $G_v \leq 0.5$		MP-M2DC $G_v > 0.5$	
Normal Operation		Arm a	Arm b	Arm a	Arm b
	$HBSM$	$G_v + (1 - G_v)$	$2 \times G_v$	$2 \times (1 - G_v)$	$G_v + (1 - G_v)$
Fault Blocking	$FBSM$	G_v	G_v	G_v	G_v
	$HBSM$	$(1 - G_v)$	G_v	$(1 - G_v)$	$(1 - G_v)$
		MP-BB		MP-DAB	
Normal Operation		Arm a	Arm b	MMC a	MMC b
	$HBSM$	$1 + G_v$	$2 \times G_v$	$1 + 1$	$2 \times G_v$
Fault Blocking	$FBSM$	G_v	G_v	1	G_v
	$HBSM$	1	G_v	1	G_v

		MP-AT	
Normal Operation		MMC a	MMC b
	$HBSM$	$2 \times (1 - G_v)$	$2 \times G_v$
Fault Blocking	$FBSM$	G_v	G_v
	$HBSM$	$(1 - G_v)$	G_v

Figure 4.15(b) shows MP-M2DC with fault blocking capability with maximum ac voltage. For this maximum ac voltage generation, 120 HBSMs are added to the lower arm "b" to generate a large ac voltage on the converter terminals.

4.2.2 Arm Current Stress Constraints

Another factor for SM installation in an MMC is the arm current stress limits. Essentially, the current flowing in a single arm is constrained to the rating of the switching elements installed and to alleviate the current limit (accordingly upgrade the power rating of the converter) two options exist: i) installation of chain of SMs in parallel or ii) replace the switches with higher rms current rating. Option (ii) is a viable option when power rating is to be slightly improved, however for significant power changes (doubling the rating power) option (i) is a preferred option.

4.2.2.1 DC-DC MMCs Arm Currents Stresses Rated for DC-DC Conversion

Arm current stress is explained for MP-M2DC, MP-BB, MP-AT, and MP-DAB. The differences of MP-DC2AC and conventional dc-dc MMCs based on arm current stress is highlighted. The existing dc-dc MMCs is rated to handle a dc current plus an ac current that is controlled for exchanging average power between arms. These currents are determined based on the power balance criteria explained in section 4.2.2.2. In such converters, the modulation signals are controlled so that the reactive power exchange between arms is suppressed to zero (with a minimal reactive power consumption by arm chokes) leading to minimal current stress and enhancing power flow capacity. A summary of arm current stresses for four topologies over a wide dc transformation range is shown in Table 4.3.

4.2.2.2 Arm Current Stresses Limits in MP-DC2AC MMCs

As a rule of thumb for all four MP-DC2AC topologies, maximum current stress in the arms is the sum of maximum dc current and the peak ac current during steady state power transfer. Higher currents during transients are admissible based on the rating of the power electronic switches utilized in the arms. The

nominal current stress in an arm is determined based on the characteristics of power switching cells installed. The maximum current flowing in arms of a MMC should be lower than the nominal current stress of the arm. Using power balance criteria for each arm, the total rated current stress of each arm is determined [32, 60]. The switch rating determines the nominal current stress of each arm. For example, the IGBT module "**CM1200HC-90R**" has nominal current of 1.2 kA which is the maximum tolerable rms current in the collector of the module [61].

The relationship between the average power flow components for a certain arm can be determined as explained in (2.41)-(2.42) and for reactive power flow as in (2.47)-(2.48). A unity power factor is assumed (i.e. $cos(\phi_{vt} - \phi_{it}) = 1$) and hence no reactive power is exchanged with the ac grid. Using appropriate PLL controller to synchronize the converter with the ac grid for external ac quantities (i.e. $dq0$) and the reference frame for internal ac quantities (i.e. $d'q'$), the average ac power exchange between the upper and lower arms in MP-M2DC also operates at power factor unity (i.e. $cos(\phi_{vt} - \phi_{ic}) = 1$ and no reactive power exchange between the arms). For four MP-DC2AC topologies, this mechanism applies and therefore the relationship is explained for MP-M2DC. For each arm, the net power is set to be zero and hence

$$P_{\Sigma}^{DC} + P_{\Sigma}^{AC} + P_{\Delta}^{DC} + P_{\Delta}^{AC} = 0 \qquad \text{for arm a} \tag{4.2}$$

$$P_{\Sigma}^{DC} + P_{\Sigma}^{AC} - P_{\Delta}^{DC} - P_{\Delta}^{AC} = 0 \qquad \text{for arm b} \tag{4.3}$$

By replacing the values from (2.43)-(2.46), the expression for arm currents is then developed. The maximum arm current stress in arm "a" of MP-M2DC is then determined as

$$I_{arm,a}^{max} = |\hat{I}_c + \hat{I}_t| + |I_c + \frac{I_s}{2}| = (I_c + \frac{I_s}{2})(1 + \frac{2(1 - G_v)}{3\hat{m}}) \tag{4.4}$$

where $\hat{m}$ is the modulation index of the converter defined as follows

$$m(t) = m_{dc} + \hat{m}cos(wt) \tag{4.5}$$

$$\hat{m} = \frac{\hat{V}_t}{V_{d1n}} \tag{4.6}$$

Similar approach is done for arm "b" and hence the maximum arm current stress becomes:

$$I^{max}_{arm,b} = |\hat{I}_c - \hat{I}_t| + |I_c - \frac{I_s}{2}| = (I_c - \frac{I_s}{2})(1 + \frac{2G_v}{3\hat{m}}) \tag{4.7}$$

Similar equations to (4.4) and (4.7) can be derived for other three MP-DC2AC MMCs.

In the subsequent sections, semiconductor utilization based on the maximum current stress for dc-dc and dc-dc-ac MMCs is explained for four topologies considering a unity power factor for dc-ac power transfer.

4.2.2.3 DC-DC-AC MMCs Arm Currents Rated for MP-DC2AC Conversion

Operating as a dc-dc-ac converter, the maximum current stress for MP-M2DC, MP-AT, and MP-BB can become higher than the solely dc-dc conversion under certain power flow conditions. This is because the power transfer between ports renders the current distribution among arms and therefore certain arm faces higher current stress. For instance, in MP-M2DC the lower arm current stress changes since there may be power transfer directly from port d_2 to the ac grid (i.e. no dc current flows in the upper arm). If the rated power is required to be transferred from d_2 to the ac grid then the switch rating of the lower arm should change accordingly. This is also the case for MP-M2DC at $G_v < 0.5$ for the upper arm during d_1 to ac grid power transfer that poses higher current stresses on the arm leading to the requirement for higher switch rating (or

parallel structuring).

The maximum arm current stress for four MP-DC2AC MMCs is summarized in Table 4.3.

Table 4.3: Maximum Arm Current Stress for Different Values of G_v for four DC-DC-AC MMCs Normalized to I_{d1n}

		MP-M2DC $G_v \leq 0.5$		MP-M2DC $G_v > 0.5$		MP-AT	
		arm a	arm b	arm a	arm b	MMC a	MMC b
DC-DC only	$I_{arm}^{max}[pu]$	$(\frac{2-G_v}{G_v})$	$3(\frac{1-G_v}{G_v})$	3	$(\frac{1+G_v}{G_v})$	3	$3(\frac{1-G_v}{G_v})$
MP-DC2AC	$I_{arm}^{max}[pu]$	$(\frac{2-G_v}{G_v})$	$\frac{3}{G_v}$	3	$\frac{1+G_v}{G_v(1-G_v)}$	3	$\frac{3}{G_v}$
		MP-BB		MP-DAB			
		arm a	arm b	MMC a	MMC b		
DC-DC only	$I_{arm}^{max}[pu]$	$(\frac{2+G_v}{G_v})$	$\frac{3}{G_v}$	3	$\frac{3}{G_v}$		
MP-DC2AC	$I_{arm}^{max}[pu]$	$(\frac{2+G_v}{G_v})$	$\frac{3}{G_v}$	3	$\frac{3}{G_v}$		

4.2.3 Comparative Analysis Based on Semiconductor Utilization Effort

A comparison is conducted based on the semiconductor requirements for each topology to meet the required arm voltage and current stress. An approximate semiconductor cost of each converter at a certain G_v for dc-dc-ac power flow is given. For this comparative analysis, the following assumptions are considered: i) all converters are assumed to be lossless and switching, conduction, and magnetic losses are neglected. ii) Number of SMs in each phase are the same (i.e. semiconductor utilization is calculated for one phase and multiplied by the number of phases). iii) it is assumed that the SMs internal capacitor voltage balancing is controlled using the sort and selection algorithm [54].

A parameter (λ) is defined to represent the total SM requirement to support maximum voltage on the arms and the current stress to provide rated power transfer. This parameter is an indication of the maximum power capacity to transfer rated power between different converter ports. Similar parameter is

defined in [44–46]. Having the maximum arm current stress I_{arm}^{max} and SM voltage requirement V_{SM}^{nom}, λ for different values of G_v is calculated for four topologies and considering normal operation and fault blocking capability as well as current stress limits for dc-dc and MP-DC2AC functionalities. The comparison is shown for normal and fault blocking capabilities and also to realize the necessary changes required when an existing dc-dc MMC is to be

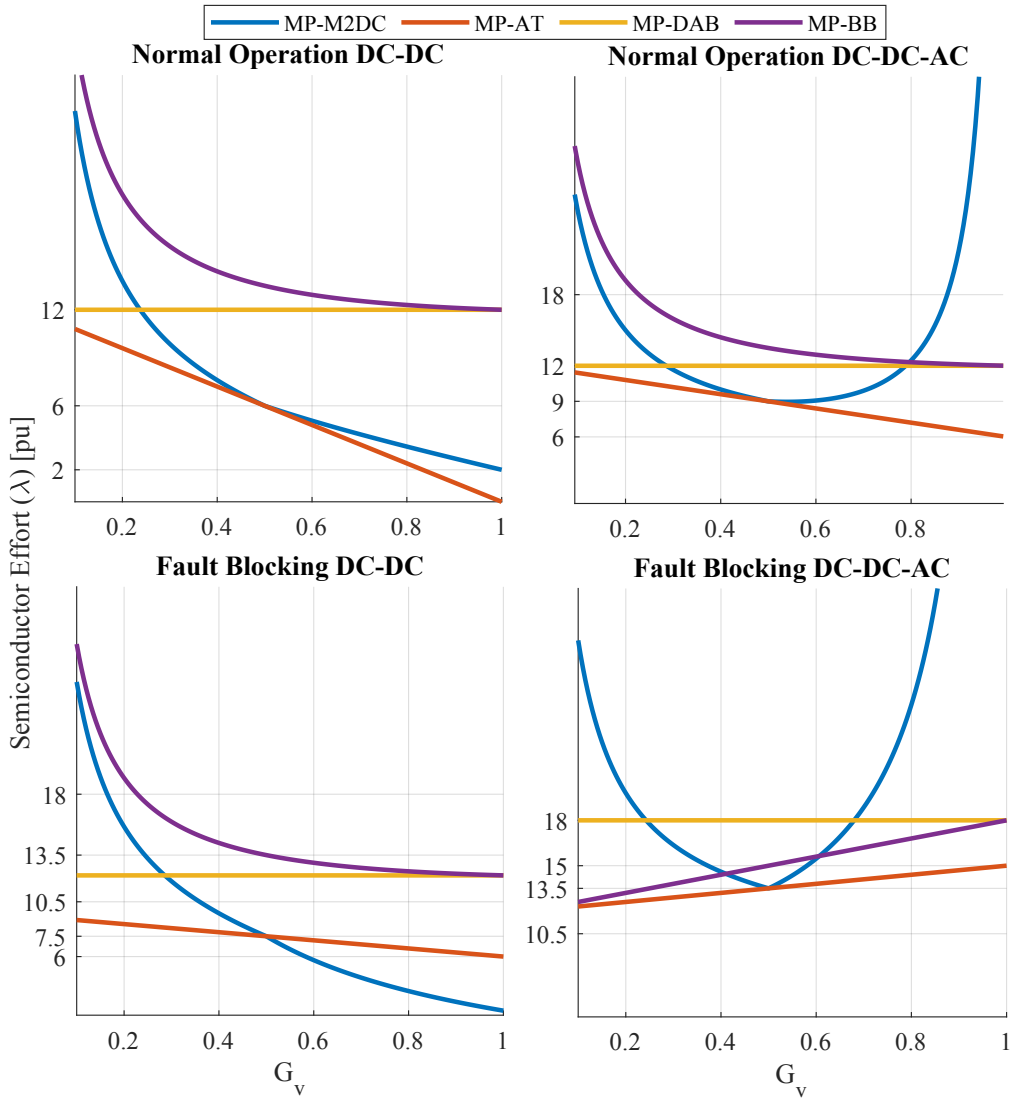

Figure 4.16: Semiconductor effort requirement for different values of G_v, where λ is normalized by $V_{d1n}.I_{d1n}$

shows the normalized value of λ vs G_v where the base power is $V_{d1n}.I_{d1n}$. For a three phase converter, λ is defined as follows:

$$\lambda = 3(N_a.V_{SM,a}^{nom}.I_{arm,a}^{max} + N_b.V_{SM,b}^{nom}.I_{arm,b}^{max}) \tag{4.8}$$

I_{arm}^{max} is the maximum current that an arm can carry based on the IGBT characteristics. The rated power delivery by the converter is determined assuming that the arms carry the maximum current. $V_{SM,k}^{nom}$ is the maximum voltage requirement for arm "a" or "b". As shown in Figure 4.16, the semiconductor effort for normal operation of MP-DC2AC is higher than that for conventional dc-dc converters for all G_v values. This is because of the higher arm current stress when an ac port is connected. Comparing fault blocking capability, MP-DC2AC requires even more SMs (FBSMs) to provide fault blocking capability which makes it even more costly compared to dc-dc MMCs. As shown, $G_v = 0.5$ is assumed to be an optimal operating condition for MP-M2DC and MP-AT which is valid according to similar implications by similar comparison practices in the literature.

4.2.4 Maximum power delivery from each port of a DC-DC MMC operating as a MP-DC2AC MMC (at the design development)

Assume a dc-dc MMC rated for dc power conversion is to be utilized for MP-DC2AC (without employing additional SMs to meet the incremented arm current stress), then the maximum power that can be delivered from each port of the converter considering the current stress limit is to be evaluated. For a MP-DC2AC, port three different power flow routing exist: i) $DC1 \leftrightarrow DC2$, ii) $DC1 \leftrightarrow AC$, and iii) $DC2 \leftrightarrow AC$. Figure 4.17 illustrates the three possible power flow directions.

If λ of the converter is determined for $DC1-DC2$ ($\lambda_{DC1-DC2}$) then at all dc

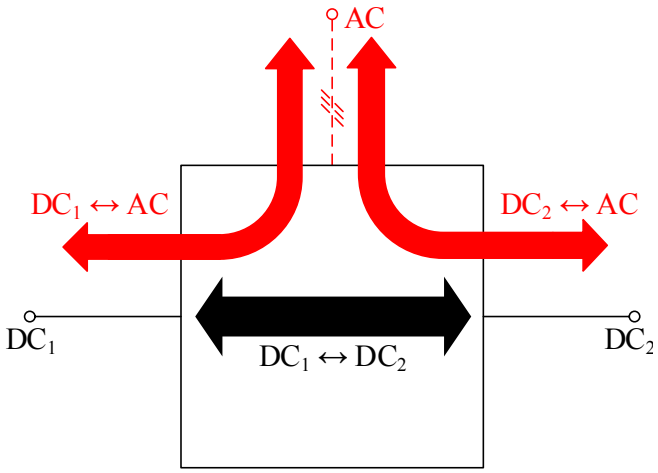

Figure 4.17: Three power flow paths between dc and ac ports of a DC-DC MMC functioning as a DC-DC-AC MMC

turns ratios (G_v) the rated power can be exchanged between two DC ports (See red lines for four topologies in Figure 4.18). For $DC1-AC$ power exchange, the value of λ that represents the semiconductor utilization (λ_{DC1-AC}) is evaluated using the procedures described in section 4.4. Therefore, the relation of $\frac{\lambda_{DC1-DC2}}{\lambda_{DC1-AC}}$ shows at what values of G_v the value of $\lambda_{DC1-DC2}$ is higher than λ_{DC1-AC} that means at certain G_v the converter is actually over utilized for $DC1-AC$ conversion and therefore it can deliver power higher than the rated value (e.g. at $G_v = 0.2$ for $DC1-AC$ in MP-M2DC $P = 1.353P_{rated}$). It is clear from Figure 4.18 that at certain dc stepping ratio (G_v) the maximum power flow capability is lower than the rated value due to under utilization of semiconductors (e.g. at $G_v = 0.8$ for $DC1-AC$ in MP-M2DC $P = 0.3382P_{rated}$).

4.2.5 Comparative Analysis Based on Efficiency and Magnetic Requirements

The previous comparison is based on semiconductor requirement of converters when multiport dc-dc-ac conversion is of interest. In the following, a fair comparison of the four MP-DC2AC MMCs is considered for two common dc stepping ratios taking into account switching, conduction, and magnetic losses

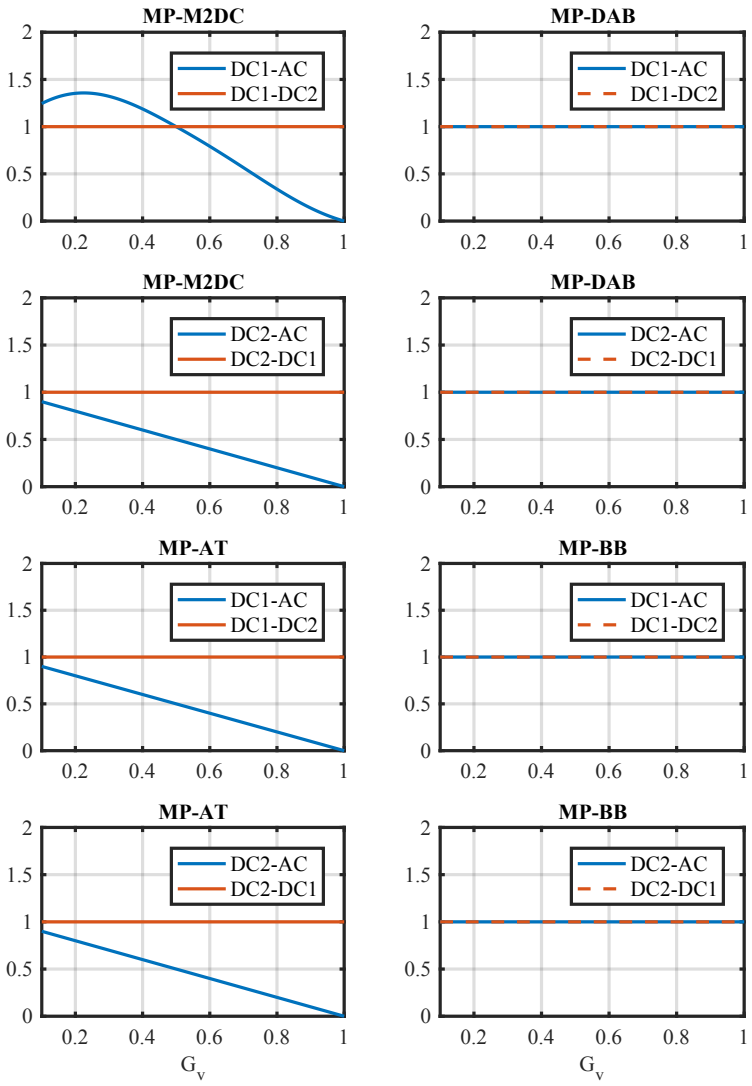

Figure 4.18: Maximum [pu] power transfer from each port of MP-DC2AC MMCs normalized to $P_{rated} = V_{d1n} \times I_{d1}$

to evaluate efficiencies. With full rated power transfer capability, magnetic requirement is also considered for the four MP-DC2AC MMCs. Note that three winding transformer for MP-DAB and MP-AT should be rated for rated power and the zig-zag transformer in MP-M2DC and MP-BB should be rated for the maximum rms line to line voltage times the maximum rms current flowing through the inductors. Representing a fair comparison of all topologies is to some extent challenging due to the different operating mechanisms. Similar comparative practice is done for dc-dc MMCs in [45] and for multiport dc

hubs in [46]. So far, no work has shown a fair comparison of the four MP-DC2AC MMCs for multiport dc-dc-ac conversion regardless of the technology of installed semiconductors.

In the following, the comparison of four topologies is represented based on the assumption that all semiconductors utilized are similar (HBSM)[3] and the comparison of hybrid connection of SMs is out of the scope of this thesis. Losses of arm chokes and transmission lines are neglected. The ac voltage of arms in four variants is maximized with HBSMs installed.

4.2.5.1 Magnetic Requirements for MP-DC2AC MMCs

As shown in Figure 2.1, all four topologies have interfacing magnetics with dc (zig-zag transformer) and ac (two or three winding transformers) grids. These magnetics should be designed at full power transfer capability.

The magnetics rating is determined based on the maximum rms voltage and current flowing through the winding and is defined as the following:

$$S^{rated,3\phi} = \begin{cases} \frac{3}{\sqrt{2}} I_{max}^{\phi,rms}.V_{max}^{\phi,rms} & \text{MP-M2DC \& MP-BB} \\ \\ \frac{9}{2} I_{max}^{\phi,rms}.V_{max}^{\phi,rms} & \text{MP-AT \& MP-DAB} \end{cases} \tag{4.9}$$

$S^{rated,3\phi}$ is the three phase MVA the magnetic to be rated, $I_{max}^{\phi,rms}$ and $V_{max}^{\phi,rms}$ are respectively the maximum single phase rms current and winding voltage in one phase of the magnetic. The coefficient $\frac{3}{\sqrt{2}}$ is to determine the three phase requirement of the magnetic considering the current flowing through two series coupled inductors and coefficient $\frac{9}{2}$ is for a three phase times three windings.

[3]Except for MP-M2DC and MP-AT at $G_v = 1$ FBSM is only utilized for average ac power exchange.

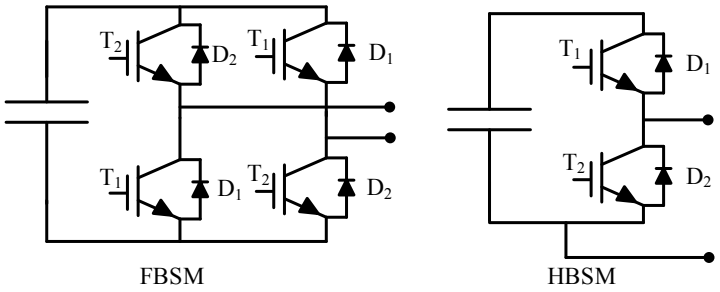

Figure 4.19: HBSM and FBSM configuration with labels representing power electronic components for better illustration of conduction and switching losses formula

4.2.5.2 Efficiency

The dominant losses in the converter are associated with switching, conduction, and magnetic losses and therefore for four topologies at certain dc voltage stepping ratio the losses are calculated and the converter efficiency obtained. In general, for power electronic losses, namely switching and conduction losses the following equations are used similar to methods developed in [32, 44, 45]. For conduction loss calculation in one SM ($P_{cond,SM}$) the following equations are used

$$P_{cond,x} = d(V_{x,0}I^{dc}_{arm,n} + R_x I^2_{arm,n,rms}) \qquad x = T_1,\ D_1 \tag{4.10}$$

$$P_{cond,y} = (1-d)(V_{y,0}I^{dc}_{arm,p} + R_y I^2_{arm,p,rms}) \qquad y = T_2,\ D_2 \tag{4.11}$$

$$P_{cond,SM} = \sum_x P_{cond,x} + \sum_y P_{cond,y} \tag{4.12}$$

d is the average duty cycle that the switch is turned on, T_1, T_2 and their antiparallel diodes D_1, D_2 are the switches in one SM (ref. Figure 4.19). n and p represent the direction in positive and negative, respectively the current flowing in the switch and $V_{x,0}$ and $V_{y,0}$ and R_x are the forward voltage drops and resistance of IGBTs and diodes.

Switching losses are calculated using the following formula

$$P_{sw} = \frac{f^{sw}}{I^{ref}V^{ref}} \begin{cases} I^{dc}_{arm,n} V_{SM}(e^{on}_T + e^{off}_T) & T_1 \\ I^{dc}_{arm,p} V_{SM} e_{D,rr} & D_1 \\ I^{dc}_{arm,p} V_{SM}(e^{on}_T + e^{off}_T) & T_2 \\ I^{dc}_{arm,n} V_{SM} e_{D,rr} & D_2 \end{cases} \tag{4.13}$$

$$P_{sw,SM} = P^{T_1}_{sw} + P^{T_2}_{sw} + P^{D_1}_{sw} + P^{D_2}_{sw} \tag{4.14}$$

e^{on}_T and e^{off}_T are the energy dissipated during turn-on and turn-off actions of IGBTs, $e_{D,rr}$ is the diode reverse recovery energy. I^{ref} and V^{ref} are the current and voltage references of the test conditions. f^{sw} is the average frequency of switching actions for each arm and can be determined using the following equation

$$f^{sw} = k^{sw}.f_m.(\frac{2\hat{V}_{ac}}{\Sigma V^{nom}_{cap}}) \tag{4.15}$$

k^{sw} is the marginal scalar quantity (it is set to 1.2), f_m is the fundamental frequency (here it is 60 Hz), $\hat{V}_{ac}$ the ac voltage of the converter.

The magnetic loss is composed of copper and core losses of the magnetic structure and it is assumed to be 0.5% of their MVA ratings [45]. The detailed derivation of magnetic losses based on the core design and winding architecture of the magnetic is not in the scope of this thesis.

4.2.5.3 Operational Comparative Case Study

To better illustrate the comparison of efficiency and losses, a case study is presented for two different dc voltage step ratios ($G_v = 0.5, 1.0$) for the MP-M2DC, MP-BB, MP-AT, and MP-DAB. Table 4.4 shows the parameters for this case study. Each topology is equipped with enough number of SMs to support full rated power transfer at all three ports (d_1, d_2, ac). Three different power flow scenarios between three ports is evaluated (dc-ac, dc-dc, and combined

dc-dc-ac conversion).

Table 4.4: Case study parameters for comparative study

Parameter	Value
V_{d1n}, V_{d2n}	400 kV, G_v×400 kV
V_{ac}^{RMS}	$95\% \times \frac{V_{d1n}}{2\sqrt{2}}$
G_v	0.5 and 1
P_{dc}^{rated}, ac grid power factor	360 MW, 0.95 lagging
S_{base}, V_{base}	360 MVA, 400 kV
Capacitor nominal voltage, V_{sm}	2 kV
SM capacitance, C_{sm}	3.2 mF

The parameters for switching and conduction losses are derived from [32] using the CM1200HC90R IGBT. Table 4.5 depicts the total magnetics rating, number of SMs for a 3ph converter structure, total semiconductor utilization effort, total capacitive energy storage, and the efficiency of four topologies considering three power flow scenarios for $G_v = 0.5$ *and* 1. The power losses for efficiency calculation considering three cases is shown in Figure 4.20. Magnetics requirement for MP-M2DC and MP-BB is the same and this is because the rated current flows into the zig-zag transformer. The previous study on the magnetic requirement for buck/boost dc-dc MMC in [32] is much lower than what is determined for MP-BB (dc-dc-ac version of buck/boost dc-dc MMC) because the current that flows through the coupled inductors is much lower. Therefore, a high magnetics installation for MP-BB is required for transferring rated power to the ac grid.

The comparison of four converters in Tables 4.5 and 4.6 conveys that for $G_v = 0.5$ applications, MP-M2DC is considered to be the best option as it has the highest efficiency considering different power flow orientations as well as the lowest semiconductor and magnetics costs among four topologies. For $G_v = 1.0$, MP-M2DC and MP-AT require FBSMs to be able to operate as FBSMs generate ac voltage (with zero dc offset) to enable power exchange

Table 4.5: Comparative analysis results for four variants for $G_v = 0.5$

		MP-M2DC	MP-BB	MP-AT	MP-DAB
	Total magnetics rating (MVA) (S_{ZigZag}+S_{Trans})	(121+379)	(121+379)	(0+568)	(0+568)
	Required SM for 3-ph converter	1800 (HBSMs)	3000 (HBSMs)	1800 (HBSMs)	2400 (HBSMs)
	Semiconductor utilization effort 3-ph (MW)	3240	4860	3240	4320
	Capacitive energy storage (kJ/MVA)	30.4	50.6	30.4	40.53
efficiency	Case I	98.77 %	98.69 %	98.77 %	98.77 %
	Case II	99.14 %	98.05 %	99.06 %	97.96 %
	Case III	99.22 %	98.82 %	99.16 %	98.66 %

with the secondary arm(MMC).

Figure 4.20, shows that for case II (dc-dc conversion) MP-DAB and MP-BB have the highest losses among converters and this is because full rated power is flown through all semiconductors (all power electronic devices are in operation). Also, in the same case MP-AT and MP-BB at $G_v = 1$ has no magnetics losses this is because no current passes through transformers.

Table 4.6: Comparative analysis results for four variants for $G_v = 1$

		MP-M2DC	MP-BB	MP-AT	MP-DAB
	Total magnetics rating (MVA) (S_{ZigZag}+S_{Trans})	(121+379)	(121+379)	(0+568)	(0+568)
	Required SM for 3-ph converter	1200 (HBSMs) + 600 (FBSMs)	2400 (HBSMs)	1200 (HBSMs) + 600 (FBSMs)	2400 (HBSMs)
	Semiconductor utilization effort 3-ph (MW)	2880	4320	2880	4320
	Capacitor energy storage (kJ/MVA)	30.4	40.53	30.4	40.53
efficiency	Case I	98.89 %	98.7 %	98.89 %	98.77 %
	Case II	99.25 %	98.63 %	99.42 %	98.26 %
	Case III	99.08 %	98.81 %	99.17 %	98.73 %

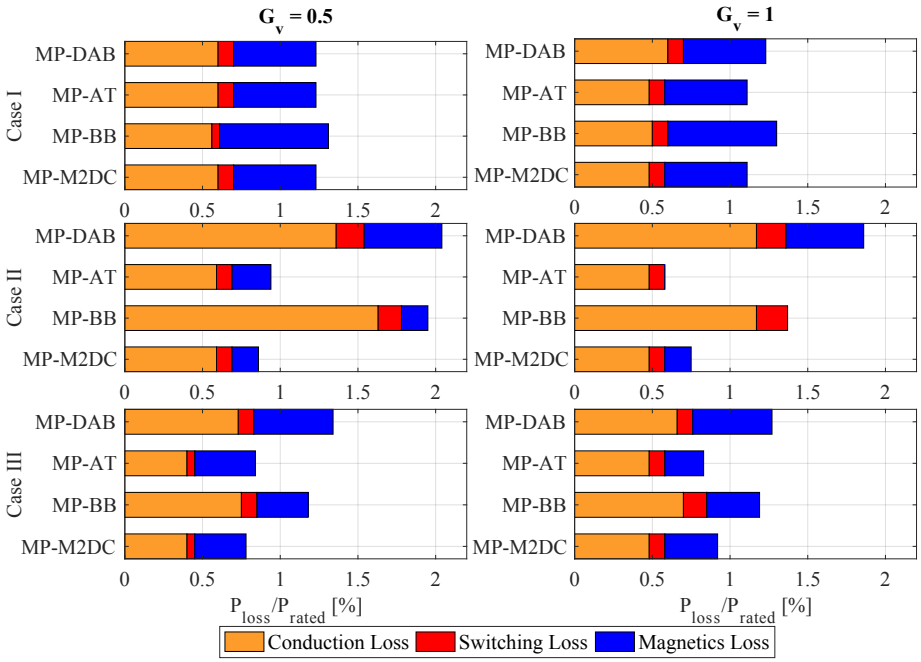

Figure 4.20: Converter losses comparison of topologies in Fig. 2.1

Chapter 5

Conclusion and Future Work

The future power grid is anticipated to comprise HVDC grids overlaid with conventional ac networks, blending the best traits of both dc and ac technologies. This hybrid dc-ac grid is capable of linking together existing two-terminal HVDC lines and MTDC systems, and interconnecting segmented ac grids. HVDC transmission will be the backbone technology although MVDC will likely also play a key role, e.g., collector networks for off-shore wind farms. The transition to a highly meshed hybrid dc-ac grid from present-day ac dominated networks (which contain a relatively sparse number of HVDC lines) offers several potential benefits, such as improved grid flexibility and security, a lower risk of cascaded blackouts, and enhancement of transient stability.

Possible topologies for multiport dc-dc-ac MMCs for hybrid ac/dc power systems are identified.

5.1 Thesis Contribution

The contributions of the thesis are summarized as follows:

- A family of four MP-DC2AC MMC topologies are presented that permit multi-directional power exchange between two dc systems and an ac network using a single converter structure, i.e., without deploying separate

dc-dc and dc-ac converter stages.

- The MP-M2DC and MP-BB topologies are analyzed in this work, which represents the first comprehensive study of these dc-dc-ac MMCs.
- Analytical equations are derived that govern the internal dc-dc and dc-ac power transfer mechanisms.
- A generalized dynamic controller is proposed for both topologies that allows independent power transfer between any combination of the three ports while keeping capacitor voltages tightly regulated.
- Converter operation and efficiency of the proposed controls are validated via time-domain simulations of detailed switched models.
- A comprehensive comparative analysis is done for all four MP-DC2AC topologies considering semiconductor count, capacitance energy storage, efficiency, magnetics, and semiconductor utilization effort.

5.2 Future Works

The proposed controller with four MP-DC2AC MMCs presented in this research work are suitable foundation for future works in both power electronics and power system analysis. A number of tentative future works are as follow:

- Experimental validation of MP-M2DC operation and control and observing arm dynamics during different power flow cases
- Examining fault blocking capability of MP-DC2AC MMCs using experimental prototype
- Study and analyze MP-DC2AC MMCs with hybrid FBSMs and HBSMs
- Derive the small signal linearized model of a three phase MP-DC2AC MMC to gain deeper understanding of converter dynamics

- Analyze the operation of MP-DC2AC MMCs in a large test system considering multiple integrated HVDC and ac systems
- Study the frequency and damping response of MP-DC2AC MMCs to transient stability on ac grid
- Provide a novel hybrid ac/dc power flow algorithm for large systems considering the presence of hybrid MP-DC2AC MMCs

Bibliography

[1] André Schön and Mark-M Bakran. A new hvdc-dc converter with inherent fault clearing capability. In *15th European Conference on Power Electronics and Applications (EPE)*, pages 1–10. IEEE, 2013.

[2] Andre Schon and Mark-M Bakran. High power hvdc-dc converters for the interconnection of hvdc lines with different line topologies. In *International Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA)*, pages 3255–3262. IEEE, 2014.

[3] Bimal K Bose. Global warming: Energy, environmental pollution, and the impact of power electronics. *IEEE Industrial Electronics Magazine*, 4(1): 6–17, 2010.

[4] Peter Lundberg, Magnus Callavik, Michael Bahrman, and Peter Sandeberg. Platforms for change: High-voltage dc converters and cable technologies for offshore renewable integration and dc grid expansions. *IEEE Power and Energy Magazine*, 10(6):30–38, 2012.

[5] Rainer Marquardt. Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications. In *International Power Electronics Conference (IPEC)*, pages 502–507. IEEE, 2010.

[6] Dirk Van Hertem and Mehrdad Ghandhari. Multi-terminal vsc hvdc for the european supergrid: Obstacles. *Renewable and sustainable energy reviews*, 14(9):3156–3163, 2010.

[7] A. Lesnicar and R. Marquardt. An innovative modular multilevel converter topology suitable for a wide power range. In *IEEE Bologna Power Tech Conference Proceedings,*, volume 3, pages 1–6, June 2003.

[8] Andre Schon and Mark-M Bakran. High power hvdc-dc converters for the interconnection of hvdc lines with different line topologies. In *International Power Electronics Conference (IPEC-Hiroshima ECCE-ASIA)*, pages 3255–3262. IEEE, 2014.

[9] G. J. Kish. On the emerging class of non-isolated modular multilevel dc–dc converters for dc and hybrid ac–dc systems. *IEEE Transactions on Smart Grid*, 10(2):1762–1771, March 2019.

[10] Stephan Kenzelmann, Alfred Rufer, Drazen Dujic, Francisco Canales, and Yales Romulo De Novaes. Isolated dc/dc structure based on modular multilevel converter. *IEEE Transactions on Power Electronics*, 30(1):89–98, 2015.

[11] Dragan Jovcic and Lu Zhang. Lcl dc/dc converter for dc grids. *IEEE Transactions on Power Delivery*, 28(4):2071–2079, 2013.

[12] Juan David Paez, David Frey, Jose Maneiro, Seddik Bacha, and Piotr Dworakowski. Overview of dc-dc converters dedicated to hvdc grids. *IEEE Transactions on Power Delivery*, 2018.

[13] WG B4.55 Cigrè Working group B4. *HVDC CONNECTION OF OFFSHORE WIND POWER PLANTS*. Cigré, 2015.

[14] Zhao Ma et al. Study on the feasibility of MVdc. In *Cigré working group WG SC C6.31*. Cigré, 2018.

[15] G. Bathurst, G. Hwang, and L. Tejwani. Mvdc - the new technology for distribution networks. In *11th IET International Conference on AC and DC Power Transmission*, pages 1–5, Feb 2015.

[16] Yi Zhang, Shaolei Shi, Rongfeng Yang, et al. Comparison and review of dc transformer topologies for hvdc and dc grids. In *8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pages 3336–3343. IEEE, 2016.

[17] J.A. Ferreira. The multilevel modular dc converter. *IEEE Transactions on Power Electronics*, 28(10):4460–4465, 2013.

[18] Staffan Norrga, Lennart Ängquist, and Antonios Antonopoulos. The polyphase cascaded-cell dc/dc converter. In *Energy Conversion Congress and Exposition (ECCE)*, pages 4082–4088. IEEE, 2013.

[19] M-M. Bakran and A. Schön (applicant: Siemens). Dc to dc converter, 9 2016.

[20] K. Konstantinos and G. Stamatiou (applicant: ABB Technology AG). Ac/dc multicell power converter for dual terminal hvdc connection,, 05 2013.

[21] Gregory J Kish and Peter W Lehn. A modular bidirectional dc power flow controller with fault blocking capability for dc networks. In *IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–7. IEEE, 2013.

[22] Gregory J Kish, Mike Ranjram, and Peter W Lehn. A modular multilevel dc/dc converter with fault blocking capability for hvdc interconnects. *IEEE Transactions on Power Electronics*, 30(1):148–162, 2015.

[23] Shenghui Cui, Joonhee Lee, Jingxin Hu, Rik W De Doncker, and Seung-Ki Sul. A modular multilevel converter with a zigzag transformer for bipolar mvdc distribution systems. *IEEE Transactions on Power Electronics*, 2018.

[24] Zhiwen Suo, Gengyin Li, Rui Li, Lie Xu, Weisheng Wang, Yongning Chi, and Wei Sun. Submodule configuration of hvdc-dc autotransformer considering dc fault. *IET Power Electronics*, 9(15):2776–2785, 2016.

[25] IA Gowaid, GP Adam, BW Williams, AM Massoud, and S Ahmed. A dc autotransformer design for medium and high voltage dc transmission systems. In *12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, pages 1–6. IEEE, 2018.

[26] W. Lin, W. Yao, J. Wen, and A. Nampally. Extended topologies and technologies of dc-dc autotransformer. In *12th IET International Conference on AC and DC Power Transmission (ACDC)*, pages 1–6, May 2016.

[27] Grain Philip Adam, Ibrahim Abdelsalam, Lie Xu, John Fletcher, Graeme Burt, and Barry Williams. Multi-tasking dc–dc and dc–ac converters for dc voltage tapping and power control in highly meshed multi-terminal hvdc networks. *IET Power Electronics*, 10(15):2217–2228, 2017.

[28] G. P. Adam, I. Abdelsalam, L. Xu, J. Fletcher, G. Burt, and B. Williams. Multi-tasking dc-dc and dc-ac converters for dc voltage tapping and power control in highly meshed multi-terminal HVdc networks. *IET Power Electronics*, 10(15):2217–2228, 2017.

[29] Dragan Jovcic and Huibin Zhang. Dual channel control with dc fault ride through for mmc-based, isolated dc/dc converter. *IEEE Transactions on Power Delivery*, 32(3):1574–1582, 2017.

[30] Feng Xu and Zheng Xu. A modular multilevel power flow controller for meshed hvdc grids. *Science China Technological Sciences*, 57(9):1773–1784, 2014.

[31] Sungmin Kim, Shenghui Cui, and Seung-Ki Sul. Modular multilevel converter based on full bridge cells for multi-terminal dc transmission. In *16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, pages 1–10. IEEE, 2014.

[32] Sunny H Kung and Gregory J Kish. A modular multilevel hvdc buck–boost converter derived from its switched-mode counterpart. *IEEE Transactions on Power Delivery*, 33(1):82–92, 2018.

[33] M. Bahram, M. Baker, J. Bowles, R. Bunch, J. Lemay, W. Long, J. McConnach, R. Menzies, J. Reeve, and M. Szechtman. Integration of small taps into (existing) hvdc links. *IEEE Transactions on Power Delivery*, 10 (3):1699–1706, July 1995.

[34] A Ekstrom and P Lamell. Hvdc tapping station: power tapping from a dc transmission line to a local ac network. In *International Conference on AC and DC Power Transmission*, pages 126–131. IET, 1991.

[35] T. Lüth, M. M. C. Merlin, and T. C. Green. Modular multilevel dc/dc converter architectures for hvdc taps. In *16th European Conference on Power Electronics and Applications*, pages 1–10, Aug 2014.

[36] Dragan Jovcic and Boon Teck Ooi. Tapping on hvdc lines using dc transformers. *Electric Power Systems Research*, 81(2):561–569, 2011.

[37] Gunnar Asplund and Andrew Williamson. A novel approach to providing on route power supplies to rural and urban communities in close proximity to the extra high voltage dc transmission line. In *Power Engineering Society Conference and Exposition in Africa*, pages 1–6. IEEE, 2007.

[38] Sixing Du, Bin Wu, Kai Tian, David Xu, and Navid R Zargari. A novel medium-voltage modular multilevel dc–dc converter. *IEEE Transactions on Industrial Electronics*, 63(12):7939–7949, 2016.

[39] Sixing Du, Bin Wu, David Xu, and Navid R Zargari. A transformerless bipolar multistring dc–dc converter based on series-connected modules. *IEEE Transactions on Power Electronics*, 32(2):1006–1017, 2017.

[40] Qiang Ren, Chi Sun, and Fei Xiao. A modular multilevel dc–dc converter topology with a wide range of output voltage. *IEEE Transactions on Power Electronics*, 32(8):6018–6030, 2017.

[41] Mohammadhadi Rouhani and Gregory J Kish. A transformerless dc-dc mmc based on symmetrically interlinked subconverters. In *IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–6. IEEE, 2017.

[42] Ricardo Vidal-Albalate, Javier Barahona, Diego Soto-Sanchez, Enerique Belenguer, Rubén S Peña, Ramon Blasco-Gimenez, and Héctor Zelaya de la Parra. A modular multi-level dc-dc converter for hvdc grids. In *42nd Annual Conference of the Industrial Electronics Society, IECON*, pages 3141–3146. IEEE, 2016.

[43] P. Klimczak, P. Blaszczyk, R. Jez, and K. Koska. Double wye modular multilevel converter - direct dc-dc topology. In *8th IET International Conference on Power Electronics, Machines and Drives (PEMD)*, pages 1–6, April 2016.

[44] André Schön and Mark-M Bakran. Comparison of modular multilevel converter based hv dc-dc-converters. In *18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, pages 1–10. IEEE, 2016.

[45] Schön Markus. *COMPARATIVE ANALYSIS OF MODULAR MULTILEVEL DC/DC CONVERTERS FOR HVDC APPLICATIONS*. Master thesis, University of Erlangen-Nuremberg, 2012.

[46] Sunny H. Kung. *Multiport DC-DC Modular Multilevel Converter for MVDC and HVDC Networks*. Master thesis, University of Alberta, 2012.

[47] Mohammadhadi Rouhani and Gregory J Kish. Multiport dc-dc-ac modular multilevel converters for hybrid ac/dc power systems. *IEEE Transactions on Power Delivery, Early Access*, 2019.

[48] Gregory J Kish and Peter W Lehn. Modeling techniques for dynamic and steady-state analysis of modular multilevel dc/dc converters. *IEEE Transactions on Power Delivery*, 31(6):2502–2510, 2016.

[49] Theodore Soong and Peter W Lehn. Internal power flow of a modular multilevel converter with distributed energy resources. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2(4):1127–1138, 2014.

[50] J. Liang, T. Jing, O. Gomis-Bellmunt, J. Ekanayake, and N. Jenkins. Operation and control of multiterminal hvdc transmission for offshore wind farms. *IEEE Transactions on Power Delivery*, 26(4):2596–2604, Oct 2011.

[51] G. J. Kish and P. W. Lehn. Linearized dc-mmc models for control design accounting for multifrequency power transfer mechanisms. *IEEE Transactions on Power Delivery*, 33(1):271–281, Feb 2018.

[52] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu. Detailed and averaged models for a 401-level mmc–hvdc system. *IEEE Transactions on Power Delivery*, 27(3):1501–1508, July 2012.

[53] Dirk Van Hertem, Oriol Gomis-Bellmunt, and Jun Liang. *HVDC grids: for offshore and supergrid of the future*, volume 51. John Wiley & Sons, 2016.

[54] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana. Circuit topologies, modeling, control schemes, and applications of modular mul-

tilevel converters. *IEEE Transactions on Power Electronics*, 30(1):4–17, Jan 2015.

[55] S. Cui, J. Lee, J. Hu, R. W. De Doncker, and S. Sul. A modular multilevel converter with a zigzag transformer for bipolar mvdc distribution systems. *IEEE Transactions on Power Electronics*, 34(2):1038–1043, Feb 2019.

[56] Rainer Marquardt. Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications. In *International Power Electronics Conference (IPEC)*, pages 502–507. IEEE, 2010.

[57] IA Gowaid, GP Adam, Ahmed M Massoud, Shehab Ahmed, Derrick Holliday, and BW Williams. Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability. *IEEE Transactions on Power Electronics*, 30(1):108–123, 2015.

[58] Jiangchao Qin, Maryam Saeedifard, Andrew Rockhill, and Rui Zhou. Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits. *IEEE Transactions on Power Delivery*, 30(1): 385–394, 2014.

[59] Rong Zeng, Lie Xu, Liangzhong Yao, and Barry W Williams. Design and operation of a hybrid modular multilevel converter. *IEEE Transactions on power electronics*, 30(3):1137–1146, 2014.

[60] Gregory Joseph Kish. *A New Class of Modular Multilevel DC/DC Converters for HVDC Systems*. PhD dissertation, university of toronto, 2016.

[61] URL `https://www.mitsubishielectric-mesh.com/products/pdf/CM1200HC-90R_n.pdf`. [Online Source].